EEPROM MEMORY PRODUCTS

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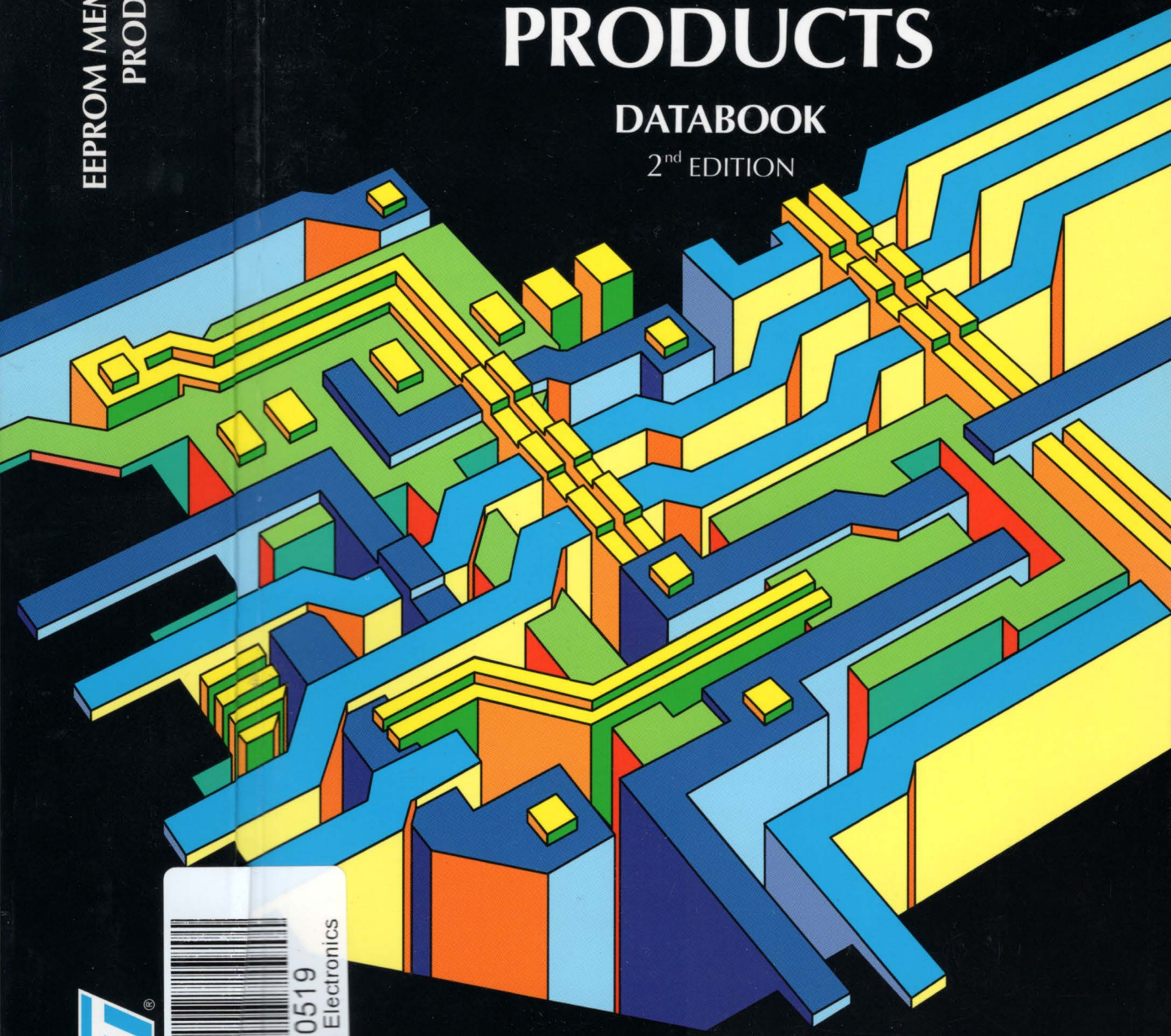
DATABOOK

2nd EDITION



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APRIL 1999

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USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED

STMicroelectronics PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF STMicroelectronics. As used herein:

1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

TABLE OF CONTENTS

EEPROM Memory Products

EEPROM (Electrically Erasable Programmable Memory) is non volatile, and can be erased and programmed a byte at a time. This is as opposed to: RAM (Random Access Memory) that is volatile, and loses its data when the power is removed; and Flash memory that, though non volatile, can only be erased on a device-wise or sector-wise basis.

The uses to which EEPROM is put, therefore, are those for which its particular mix of properties are better suited than are those of RAM or Flash memory. Examples might include the storing of set-up parameters for a piece of equipment, or data tables and persistent variables, which might need to be changed regularly, but must retained from one power-down to the next power-up sequence. (These issues are discussed in *AN997*, on page 701).

Since the previous edition of this data book, there has been a significant increase in the code size of application programs, with an associated increase in the number of non-volatile parameters that need to be retained. To cater for this trend, EEPROM devices are being introduced to market at ever increasing memory capacities. For this edition of the data book, devices of up to 1 Mbit capacity are available.

Two distinct families of EEPROM have established themselves:

- Serial Access EEPROM
- Parallel Access EEPROM

The parallel access EEPROM devices generally need one pin per address and data bit. The integrated circuit package tends to have a fairly large footprint, with at least 28 external pins.

The serial access EEPROM devices can all be placed in an 8-pin package, irrespective of their memory capacity. This is because there is always only one line (perhaps two) to carry all of the address and data bits, multiplexed one after the other.

This multiplexing involves adhering to a standard protocol. There are three of these that are currently widely adopted (as described in *AN1001*, on page 647):

– Serial I^2C Bus EEPROM
– Serial SPI Bus EEPROM
– Serial Microwire Bus EEPROM

These, then, constitute the first three sections of data sheets in this book, with parallel access EEPROM making the fourth.

A new technology from STMicroelectronics, FLASH+, allows a single chip to contain an area of Flash memory and an area of EEPROM, thereby offering footprint and electrical power advantages to many applications. These devices are included in the fifth section of this book (and are described in the application notes from page 637 to 762).

The sixth section presents a number of Application Specific Memory devices. These are devices whose cost, architecture, or other properties, have been optimized to meet specific market needs (as described in *AN1120*, on page 743).

The seventh section contains a number of application notes that have been written to describe various aspects of using EEPROM technology.

STMicroelectronics is permanently committed to extensive investment in process research, process development, and product design. As a result, it is constantly adding new products to these families, and adding new families to its portfolio. Please contact to your nearest ST Sales Office, or see the latest information in our pages on the world wide web: *www.st.com*.

Table 1. Product Overview

	Serial I^2C	Serial SPI	Serial Microwire	Parallel	FLASH+	ASM
256 bit			M93C06			
512 bit						
1 Kbit	M24C01	M95010 ST95010	M93C46 M93S46			M24LC21B M24LW21 M24FC21 M24FW21 M2201
2 Kbit	M24C02	M95020 ST95020 ST95022	M93C56 M93S56			M34C02
4 Kbit	M24C04	M95040 ST95040	M93C66 M93S66			ST24C04 ST25C04 ST24W04 ST25W04
8 Kbit	M24C08	M95080 ST95P08	M93C76			M35080 ST24C08 ST25C08 ST24W08 ST25W08
16 Kbit	M24C16	M95160	M93C86	M28C16A M28C17A M28C16B M28C17B		M24164 ST24C16 ST25C16 ST24W16 ST25W16 ST24E16 ST25E16
32 Kbit	M24C32	M95320				
64 Kbit	M24C64	M95640		M28C64 M28C64C M28C64X	M39208	
128 Kbit	M24128-B M24128	M95128				
256 Kbit	M24256-B M24256-A M24256	M95256		M28256	M39432 M39832	
512 Kbit	M24512	M95512				
1 Mbit				M28010		

EEPROM Memory Products

EEPROM Memory Products

EEPROM Memory Products

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NOTES

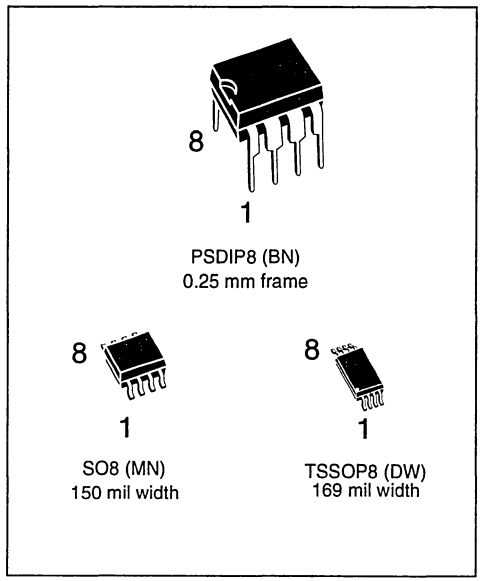
SERIAL EEPROM, I^2C BUS

NOTES

M24C16, M24C08
M24C04, M24C02, M24C01

16/8/4/2/1 Kbit Serial I²C Bus EEPROM

- Two Wire I²C Serial Interface
  Supports 400 kHz Protocol
- Single Supply Voltage:
  - 4.5V to 5.5V for M24Cxx
  - 2.5V to 5.5V for M24Cxx-W
  - 1.8V to 3.6V for M24Cxx-R
- Hardware Write Control
- BYTE and PAGE WRITE (up to 16 Bytes)
- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Behaviour
- 1 Million Erase/Write Cycles (minimum)
- 40 Year Data Retention (minimum)



DESCRIPTION

These electrically erasable programmable memory (EEPROM) devices are fabricated with STMicroelectronics' High Endurance, Single Polysilicon, CMOS technology. This guarantees an endurance typically well above one million Erase/Write cycles, with a data retention of 40 years. The memories are organised as 2048/1024 x 8 bit (M24C16, M24C08) and 512/256/128 x 8 bit (M24C04, M24C02, M24C01), and operate with a power supply down to 2.5 V (for the -W ver-

Table 1. Signal Names

E0, E1, E2	Chip Enable Inputs
SDA	Serial Data/Address Input/ Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

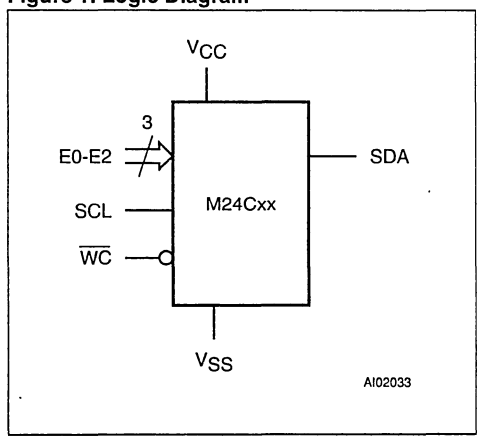
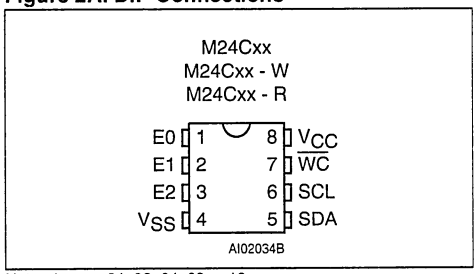
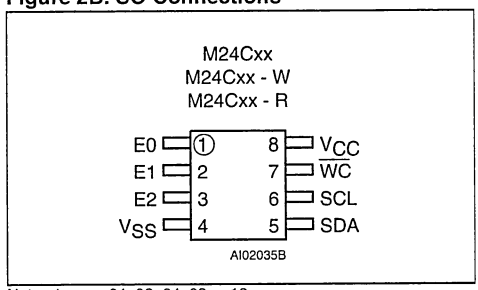


Figure 2A. DIP Connections



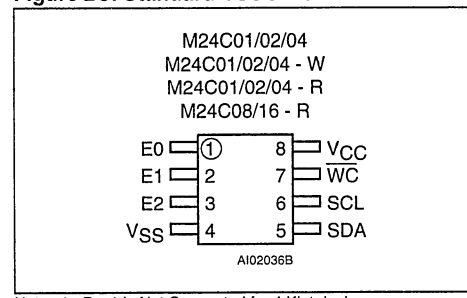
Note: 1. xx = 01, 02, 04, 08 or 16
2. Pin 1 is Not Connected for 4 Kbit devices
3. Pins 1 and 2 are Not Connected for 8 Kbit devices
4. Pins 1, 2 and 3 are Not Connected for 16 Kbit devices

Figure 2B. SO Connections



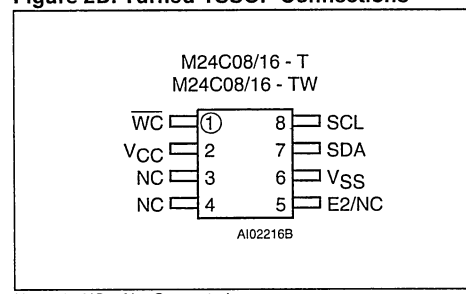
Note: 1. xx = 01, 02, 04, 08 or 16
2. Pin 1 is Not Connected for 4 Kbit devices
3. Pins 1 and 2 are Not Connected for 8 Kbit devices
4. Pins 1, 2 and 3 are Not Connected for 16 Kbit devices

Figure 2C. Standard-TSSOP Connections



Note: 1. Pin 1 is Not Connected for 4 Kbit devices
2. Pins 1 and 2 are Not Connected for 8 Kbit devices
3. Pins 1, 2 and 3 are Not Connected for 16 Kbit devices

Figure 2D. Turned-TSSOP Connections



Note: 1. NC = Not Connected
2. Pin 5 is Not Connected for 16 Kbit devices

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		-40 to 125	°C
T_{STG}	Storage Temperature		-65 to 150	°C
T_{LEAD}	Lead Temperature during Soldering	PSDIP8: 10 sec SO8: 40 sec TSSOP8: t.b.c.	260 215 t.b.c.	°C
V_{IO}	Input or Output range		-0.6 to 6.5	V
V_{CC}	Supply Voltage		-0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]		4000	V
	Electrostatic Discharge Voltage (Machine model) [3]		500	V

Note: 1 Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents
2. MIL-STD-883C, 3015.7 (100 pF, 1500 Ω)
3 EIAJ IC-121 (Condition C) (200 pF, 0 Ω)

sion of each device), and down to 1.8 V (for the -R version of each device).

The M24C16, M24C08, M24C04, M24C02, M24C01 are available in Plastic Dual-in-Line, Plastic Small Outline and Thin Shrink Small Outline packages.

These memory devices are compatible with the I^2C extended memory standard. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The memory carries a built-in 4-bit unique Device Type Identifier code (1010) in accordance with the I^2C bus definition.

The memory behaves as a slave device in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a Device Select Code and $\overline{RW}$ bit (as described in Table 3), terminated by an acknowledge bit.

When writing data to the memory, the memory inserts an acknowledge bit during the 9^{th} bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a STOP condition after an Ack for WRITE, and after a NoAck for READ.

Power On Reset: V_{CC} Lock-Out Write Protect

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The internal reset is held active until the V_{CC} voltage has reached the POR threshold value, and all operations are disabled – the device will not respond to any command. In the same way, when V_{CC} drops from the operating voltage, below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable and valid V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTION

Serial Clock (SCL)

The SCL input pin is used to strobe all data in and out of the memory. In applications where this line is used by slaves to synchronize the bus to a slower clock, the master must have an open drain output, and a pull-up resistor must be connected from the SCL line to V_{CC}. (Figure 3 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the master has a push-pull (rather than open drain) output.

Serial Data (SDA)

The SDA pin is bi-directional, and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from the SDA bus to V_{CC}. (Figure 3 indicates how the value of the pull-up resistor can be calculated).

Chip Enable (E2, E1, E0)

These chip enable inputs are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit device select code (but see the description of memory addressing, on page 5, for more details). These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code (but note that the V_{IL} and V_{IH} levels for the inputs are CMOS compatible, not TTL compatible).

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus

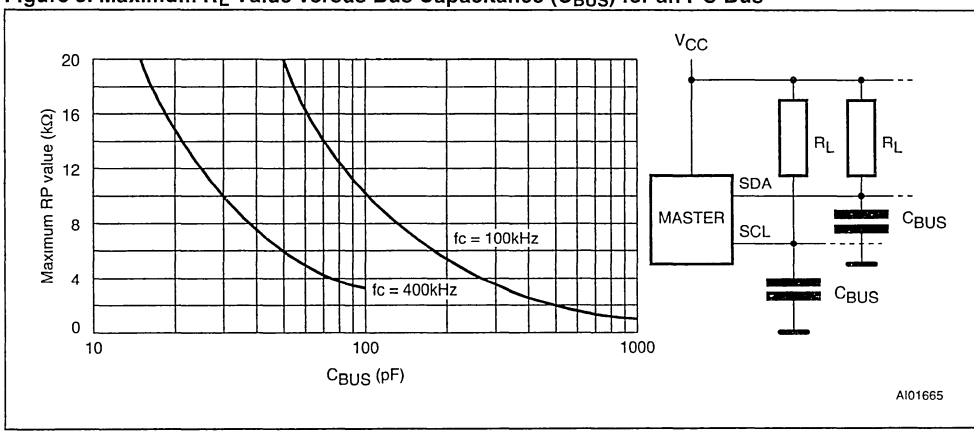
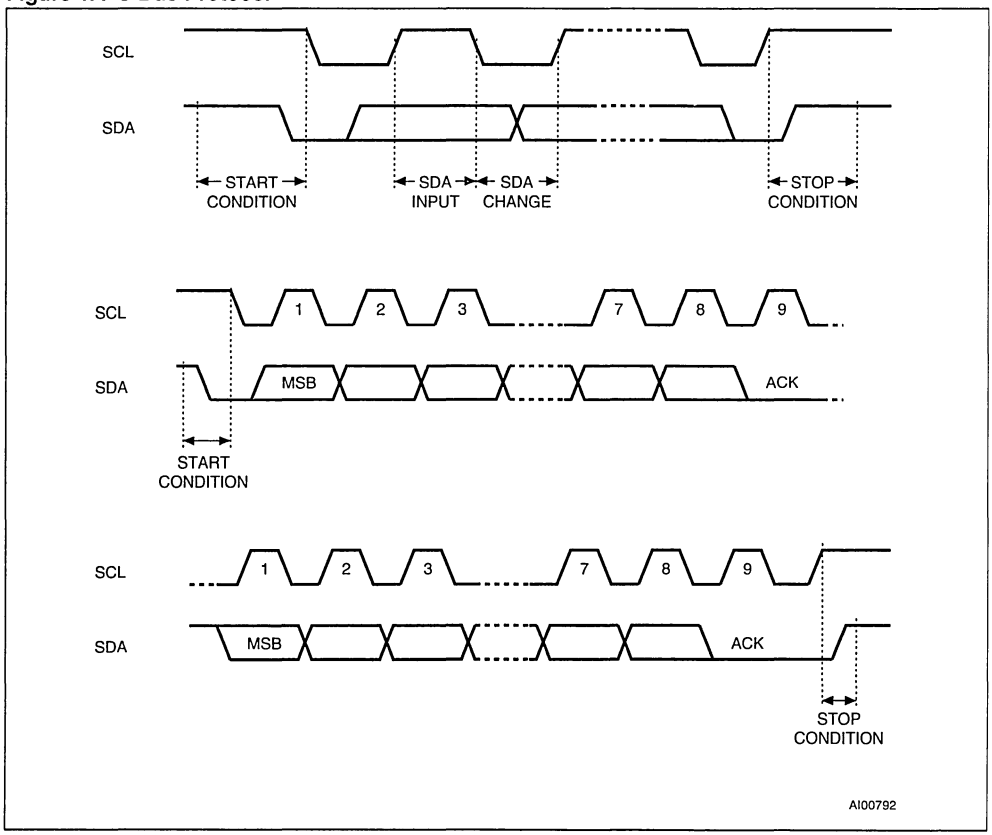


Figure 4. I²C Bus Protocol



Write Control ($\overline{WC}$)

The hardware Write Control pin ($\overline{WC}$) is useful for protecting the entire contents of the memory from inadvertent erase/write. The Write Control signal is used to enable ($\overline{WC}$=V_{IL}) or disable ($\overline{WC}$=V_{IH}) write instructions to the entire memory area. When unconnected, the $\overline{WC}$ input is internally read as V_{IL}, and write operations are allowed.

When $\overline{WC}$=1, Device Select and Address bytes are acknowledged, Data bytes are not acknowledged.

Please see the Application Note *AN404* for a more detailed description of the Write Control feature.

DEVICE OPERATION

The memory device supports the I²C protocol. This is summarized in Figure 4, and is compared with other serial bus protocols in Application Note *AN1001*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the master, and the other as the slave. A data transfer can only be initiated by the master, which will also provide the serial clock for synchronization. The memory device is always a slave device in all communication.

Start Condition

START is identified by a high to low transition of the SDA line while the clock, SCL, is stable in the high state. A START condition must precede any data transfer command. The memory device continuously monitors (except during a programming cycle) the SDA and SCL lines for a START condition, and will not respond unless one is given.

Stop Condition

STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communica-

Table 3. Device Select Code [1]

	Device Type Identifier				Chip Enable			RW
	b7	b6	b5	b4	b3	b2	b1	b0
M24C01 Select Code	1	0	1	0	E2	E1	E0	RW
M24C02 Select Code	1	0	1	0	E2	E1	E0	RW
M24C04 Select Code	1	0	1	0	E2	E1	A8	RW
M24C08 Select Code	1	0	1	0	E2	A9	A8	RW
M24C16 Select Code	1	0	1	0	A10	A9	A8	RW

Note: 1. The most significant bit, b7, is sent first
2. E0, E1 and E2 are compared against the respective external pins on the memory device.
3. A10, A9 and A8 represent high significant bits of the address

tion between the memory device and the bus master. A STOP condition at the end of a Read command, after (and only after) a NoAck, forces the memory device into its standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK)

An acknowledge signal is used to indicate a successful byte transfer. The bus transmitter, whether it be master or slave, releases the SDA bus after sending eight bits of data. During the 9th clock pulse period, the receiver pulls the SDA bus low to acknowledge the receipt of the eight data bits.

Data Input

During data input, the memory device samples the SDA bus signal on the rising edge of the clock, SCL. For correct device operation, the SDA signal must be stable during the clock low-to-high transition, and the data must change *only* when the SCL line is low.

Memory Addressing

To start communication between the bus master and the slave memory, the master must initiate a START condition. Following this, the master sends the 8-bit byte, shown in Table 3, on the SDA bus line (most significant bit first). This consists of the 7-bit Device Select Code, and the 1-bit Read/Write Designator (RW). The Device Select Code is further subdivided into: a 4-bit Device Type Identifier, and a 3-bit Chip Enable "Address" (E2, E1, E0).

To address the memory array, the 4-bit Device Type Identifier is 1010b.

If all three chip enable inputs are connected, up to eight memory devices can be connected on a single I^2C bus. Each one is given a unique 3-bit code on its Chip Enable inputs. When the Device Select Code is received on the SDA bus, the memory only responds if the Chip Select Code is the same as the pattern applied to its Chip Enable pins.

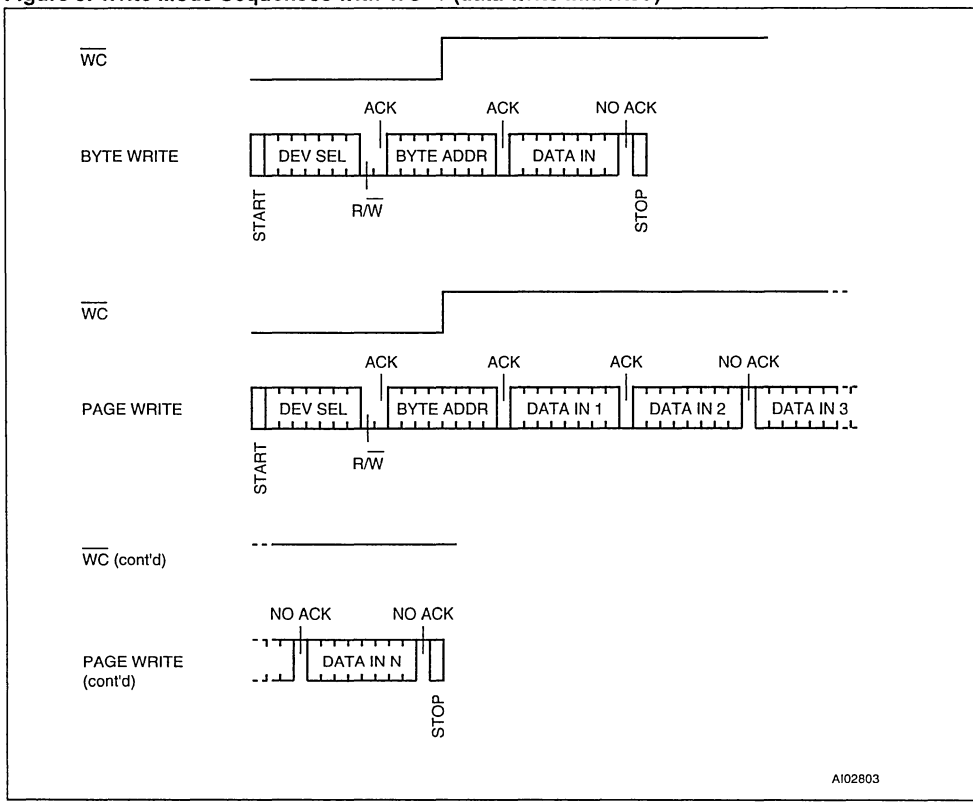
Those devices with larger memory capacities (the M24C16, M24C08) need more address bits. E0 is not available for use on devices that need to use address line A8; E1 is not available for devices that need to use address line A9, and E2 is not available for devices that need to use address line A10 (see Figure 2A to Figure 2D for details). Using the E0, E1 and E2 inputs pins, up to eight M24C02 (or M24C01), four M24C04, two M24C08 or one M24C16 device can be connected to one I^2C bus. In each case, and in the hybrid cases, this gives a total memory capacity of 16 Kbits, 2 KBytes (except where M24C01 devices are used).

Table 4. Operating Modes

Mode	RW bit	WC [1]	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, RW = '1'
Random Address Read	'0'	X	1	START, Device Select, RW = '0', Address
	'1'	X		reSTART, Device Select, RW = '1'
Sequential Read	'1'	X	≥ 1	Similar to Current or Random Address Read
Byte Write	'0'	V_{IL}	1	START, Device Select, RW = '0'
Page Write	'0'	V_{IL}	≤ 16	START, Device Select, RW = '0'

Note: 1. X = V_{IH} or V_{IL}.

Figure 5. Write Mode Sequences with $\overline{WC}$=1 (data write inhibited)



The 8th bit is the R$\overline{W}$ bit. This is set to '1' for read and '0' for write operations. If a match occurs on the Device Select Code, the corresponding memory gives an acknowledgment on the SDA bus during the 9th bit time. If the memory does not match the Device Select Code, it deselects itself from the bus, and goes into stand-by mode.

There are two modes both for read and write. These are summarized in Table 4 and described later. A communication between the master and the slave is ended with a STOP condition.

Write Operations

Following a START condition the master sends a Device Select Code with the R$\overline{W}$ bit set to '0', as shown in Table 4. The memory acknowledges this, and waits for an address byte. The memory responds to the address byte with an acknowledge bit, and then waits for the data byte.

Writing to the memory may be inhibited if the $\overline{WC}$ input pin is taken high. Any write command with $\overline{WC}$=1 (during a period of time from the START condition until the end of the address byte) will not modify the memory contents, and the accompanying data bytes will *not* be acknowledged (as shown in Figure 5).

Byte Write

In the Byte Write mode, after the Device Select Code and the address bytes, the master sends one data byte. If the addressed location is write protected by the $\overline{WC}$ pin, the memory replies with a NoAck, and the location is not modified. If, instead, the $\overline{WC}$ pin has been held at 0, as shown in

Figure 6. Write Mode Sequences with $\overline{WC}$=0 (data write enabled)

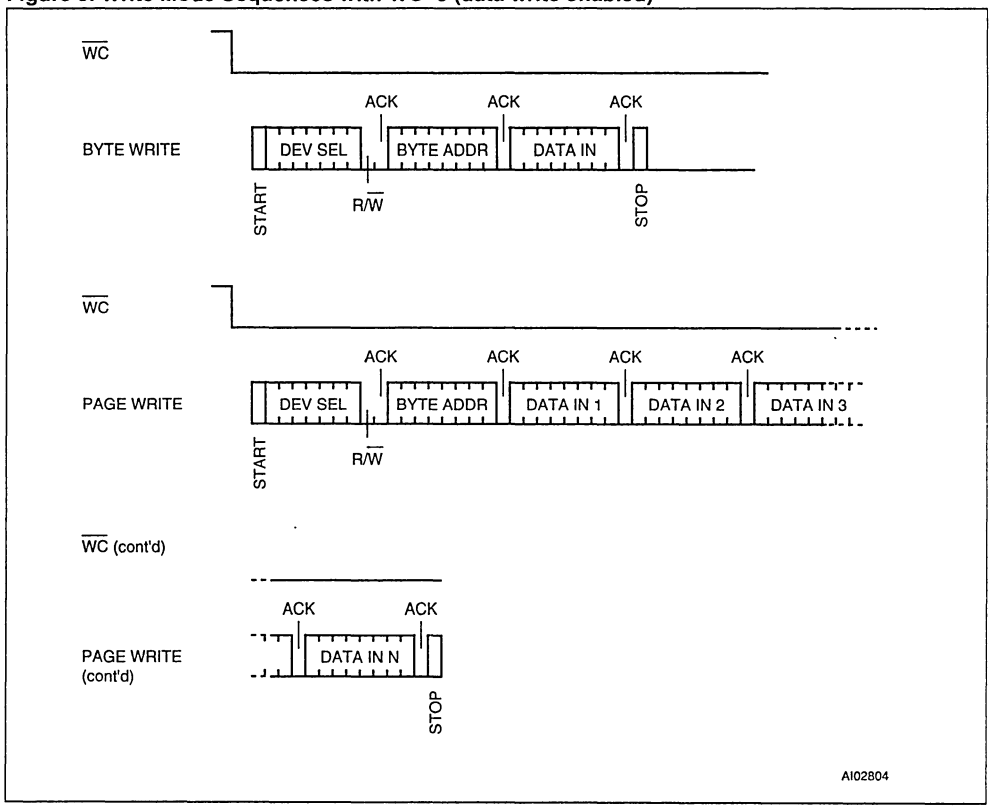


Figure 6, the memory replies with an Ack. The master terminates the transfer by generating a STOP condition.

Page Write

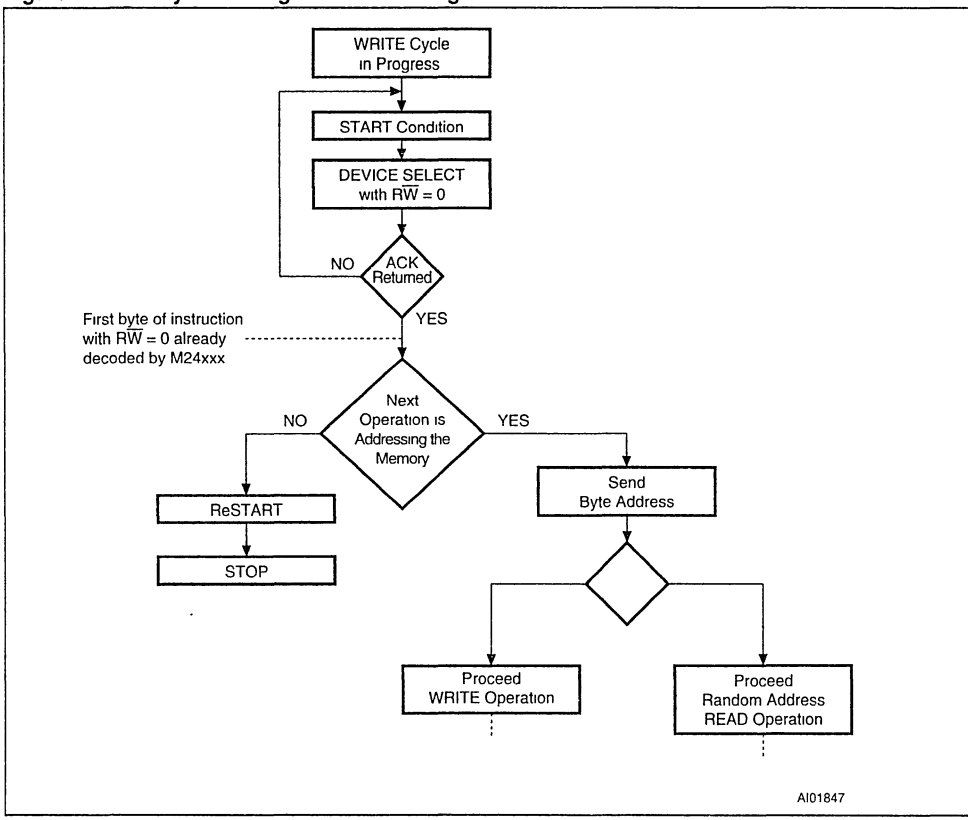
The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the most significant memory address bits are the same. If more bytes are sent than will fit up to the end of the row, a condition known as 'roll-over' occurs. Data starts to become overwritten (in a way not formally specified in this data sheet).

The master sends from one up to 16 bytes of data, each of which is acknowledged by the memory if the $\overline{WC}$ pin is low. If the $\overline{WC}$ pin is high, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck. After each byte is transferred, the internal byte address counter (the 4 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition.

When the master generates a STOP condition immediately after the Ack bit (in the "10^{th} bit" time slot), either at the end of a byte write or a page write, the internal memory write cycle is triggered. A STOP condition at any other time does not trigger the internal write cycle.

During the internal write cycle, the SDA input is disabled internally, and the device does not respond to any requests.

Figure 7. Write Cycle Polling Flowchart using ACK



Minimizing System Delays by Polling On ACK

During the internal write cycle, the memory disconnects itself from the bus, and copies the data from its internal latches to the memory cells. The maximum write time (t_W) is shown in Table 6, but the typical time is shorter. To make use of this, an Ack polling sequence can be used by the master.

The sequence, as shown in Figure 7, is:

- Initial condition: a Write is in progress.
- Step 1: the master issues a START condition followed by a Device Select Code (the first byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no Ack will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it responds with an Ack, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction having been sent during Step 1).

Read Operations

Read operations are performed independently of the state of the $\overline{WC}$ pin.

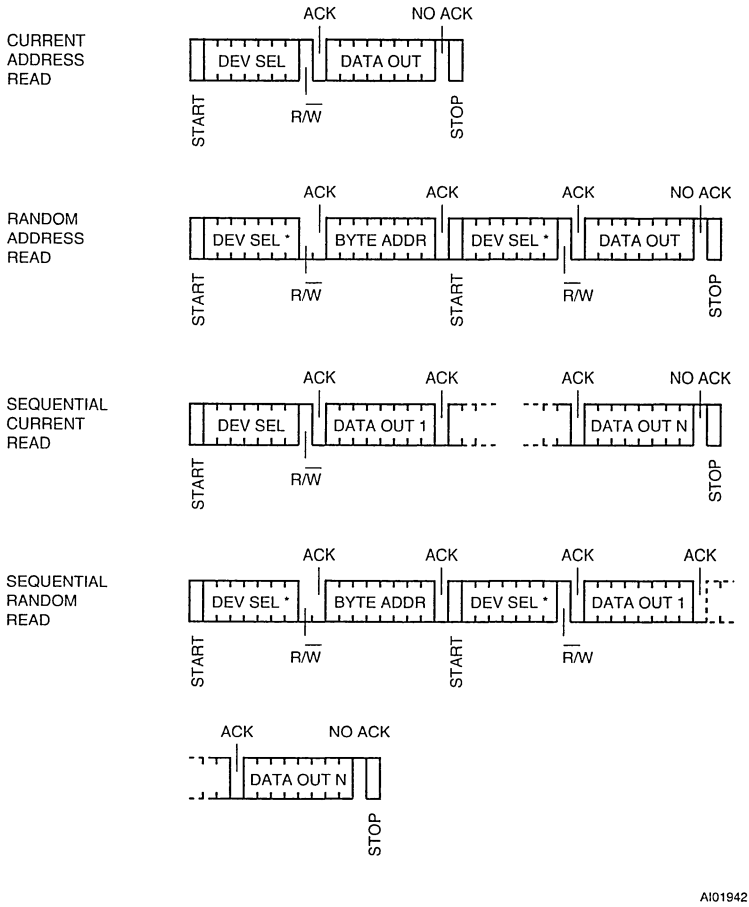
Random Address Read

A dummy write is performed to load the address into the address counter, as shown in Figure 8. Then, *without* sending a STOP condition, the master sends another START condition, and repeats the Device Select Code, with the $\overline{RW}$ bit set to '1'. The memory acknowledges this, and outputs the contents of the addressed byte. The master must *not* acknowledge the byte output, and terminates the transfer with a STOP condition.

Current Address Read

The device has an internal address counter which is incremented each time a byte is read. For the Current Address Read mode, following a START condition, the master sends a Device Select Code with the $\overline{RW}$ bit set to '1'. The memory acknowledges this, and outputs the byte addressed by the

Figure 8. Read Mode Sequences



Note: 1 The seven most significant bits of the Device Select Code of a Random Read (in the 1st and 3rd bytes) must be identical.

internal address counter. The counter is then incremented. The master terminates the transfer with a STOP condition, as shown in Figure 8, *without* acknowledging the byte output.

Sequential Read

This mode can be initiated with either a Current Address Read or a Random Address Read. The master *does* acknowledge the data byte output in this case, and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must *not* acknowledge the last byte output, and *must* generate a STOP condition.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over' and the memory continues to output data from the start of the memory block.

Acknowledge in Read Mode

In all read modes, the memory waits, after each byte read, for an acknowledgment during the 9th bit time. If the master does not pull the SDA line low during this time, the memory terminates the data transfer and switches to its standby state.

Table 5. DC Characteristics
(T_A = 0 to 70 °C, or -40 to 85 °C; V_{CC} = 4.5 to 5.5 V or 2.5 to 5.5 V)
(T_A = 0 to 70 °C, or -40 to 85 °C; V_{CC} = 1.8 to 3.6 V)

Symbol	Parameter		Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA)		$0 V \le V_{IN} \le V_{CC}$		± 2	µA
I_{LO}	Output Leakage Current		$0 V \le V_{OUT} \le V_{CC}$, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current		V_{CC}=5V, f_c=400kHz (rise/fall time < 30ns)		2	mA
		-W series:	V_{CC}=2.5V, f_c=400kHz (rise/fall time < 30ns)		1	mA
		-R series:	V_{CC}=1.8V, f_c=400kHz (rise/fall time < 30ns)		0.8[1]	mA
I_{CC1}	Supply Current (Stand-by)		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5 V		1	µA
I_{CC2}	Supply Current (Stand-by)	-W series:	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5 V		0.5	µA
I_{CC3}	Supply Current (Stand-by)	-R series:	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8 V		0.1[1]	µA
V_{IL}	Input Low Voltage (E0, E1, E2, SCL, SDA)			- 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (E0, E1, E2, SCL, SDA)			0.7V_{CC}	V_{CC}+1	V
V_{IL}	Input Low Voltage ($\overline{WC}$)			- 0.3	0.5	V
V_{IH}	Input High Voltage ($\overline{WC}$)			0.7V_{CC}	V_{CC}+1	V
V_{OL}	Output Low Voltage		I_{OL} = 3 mA, V_{CC} = 5 V		0.4	V
		-W series:	I_{OL} = 2.1 mA, V_{CC} = 2.5 V		0.4	V
		-R series:	I_{OL} = 1 mA, V_{CC} = 1.8 V		0.4[1]	V

Note: 1. This is preliminary data.

Table 6. AC Characteristics

Symbol	Alt.	Parameter	M24C16, M24C08, M24C04, M24C02, M24C01						Unit
			V_{CC}=4.5 to 5.5 V T_A=0 to 70°C or -40 to 85°C		V_{CC}=2.5 to 5.5 V T_A=0 to 70°C or -40 to 85°C		V_{CC}=1.8 to 3.6 V T_A=0 to 70°C or -40 to 85°C[4]		
			Min	Max	Min	Max	Min	Max	
t_{CH1CH2}	t_R	Clock Rise Time		300		300		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300		300		300	ns
t_{DH1DH2}[2]	t_R	SDA Rise Time	20	300	20	300	20	300	ns
t_{DL1DL2}[2]	t_F	SDA Fall Time	20	300	20	300	20	300	ns
t_{CHDX}[1]	$t_{SU\ STA}$	Clock High to Input Transition	600		600		600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		600		600		ns
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	600		600		600		ns
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		0		0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		1.3		1.3		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	100		100		100		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	600		600		600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		1.3		1.3		µs
t_{CLQV}[3]	t_{AA}	Clock Low to Data Out Valid	200	900	200	900	200	900	ns
t_{CLQX}	t_{DH}	Data Out Hold Time After Clock Low	200		200		200		ns
f_C	f_{SCL}	Clock Frequency		400		400		400	kHz
t_W	t_{WR}	Write Time		5		10		10	ms

Note: 1 For a reSTART condition, or following a write cycle
2. Sampled only, not 100% tested
3. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA
4 This is preliminary data

Table 7. AC Measurement Conditions

Input Rise and Fall Times	≤ 50 ns
Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}
Input and Output Timing Reference Voltages	0.3V_{CC} to 0.7V_{CC}

Figure 9. AC Testing Input Output Waveforms

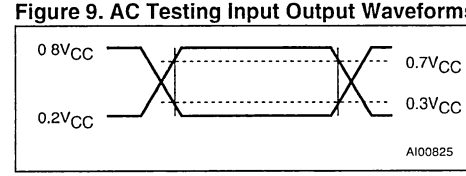


Figure 10. AC Waveforms

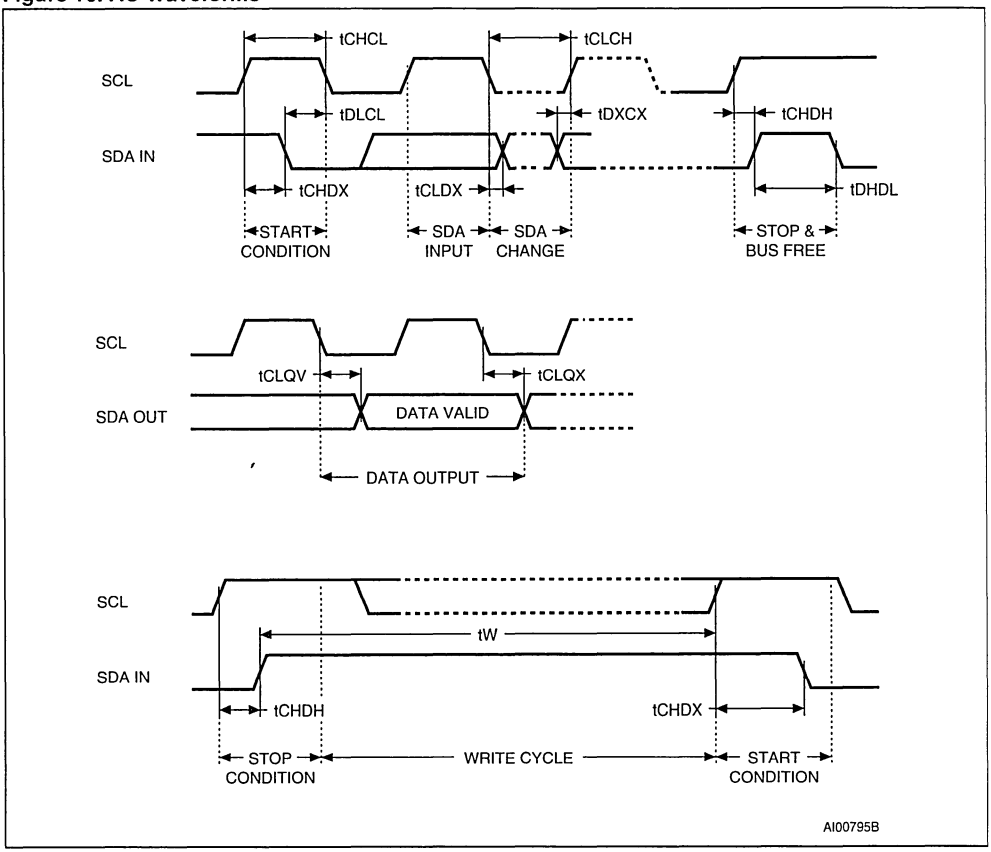


Table 8. Input Parameters[1] (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} < 0.3V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} > 0.7V_{CC}$	500		kΩ
t_{NS}	Low Pass Filter Input Time Constant (SCL and SDA)		200	500	ns

Note: 1. Sampled only, not 100% tested.

Table 9. Ordering Information Scheme

Example: M24C08 – T W DW 1 T

Memory Capacity

16	16 Kbit (2048 x 8)
08	8 Kbit (1024 x 8)
04	4 Kbit (512 x 8)
02	2 Kbit (256 x 8)
01	1 Kbit (128 x 8)

TSSOP Pin-Out

blank	Standard (as shown in Figure 2C) for: M24C01, M24C01-W, M24C01-R, M24C02, M24C02-W, M24C02-R, M24C04, M24C04-W, M24C04-R, M24C08-R, M24C16-R.
T	Turned (as shown in Figure 2D) for M24C08-T, M24C08-TW, M24C16-T, M24C16-TW

Operating Voltage

blank	4.5 V to 5.5 V
W	2.5 V to 5.5 V
R	1.8 V to 3.6 V

Option

T	Tape and Reel Packing

Temperature Range

1[1]	0 °C to 70 °C
6	–40 °C to 85 °C

Package

BN	PSDIP8 (0.25 mm frame)
MN	SO8 (150 mil width)
DW	TSSOP8 (169 mil width)

Note: 1. Temperature range 1 available only on request.

ORDERING INFORMATION

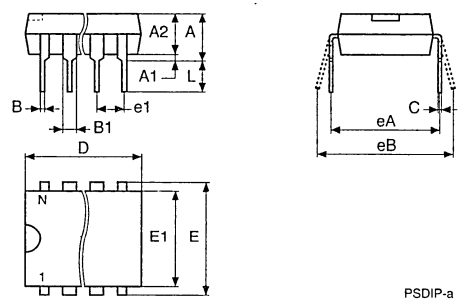
Devices are shipped from the factory with the memory content set at all '1's (FFh).

The notation used for the device number is as shown in Table 9. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 10. PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

Figure 11. PSDIP8 (BN)

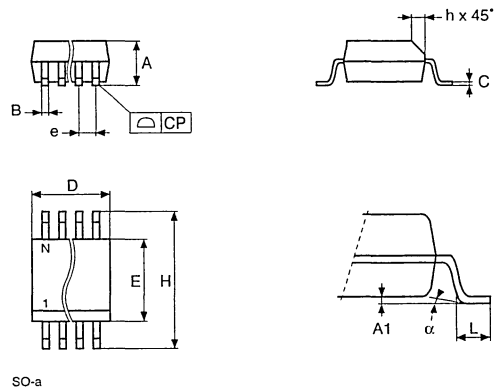


Note: 1. Drawing is not to scale

Table 11. SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

Figure 12. SO8 narrow (MN)



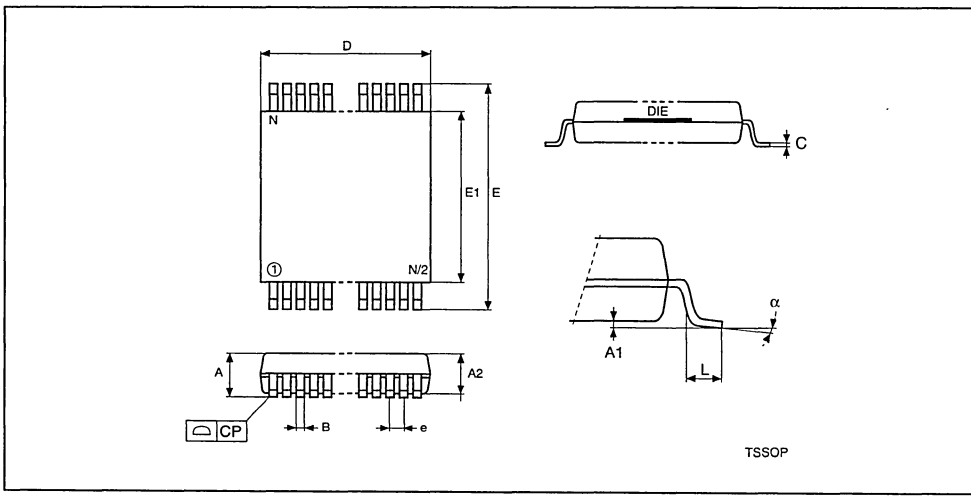
SO-a

Note. 1. Drawing is not to scale.

Table 12. TSSOP8 - 8 lead Thin Shrink Small Outline

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.10			0.043
A1		0.05	0.15		0.002	0.006
A2		0.85	0.95		0.033	0.037
B		0.19	0.30		0.007	0.012
C		0.09	0.20		0.004	0.008
D		2.90	3.10		0.114	0.122
E		6.25	6.50		0.246	0.256
E1		4.30	4.50		0.169	0.177
e	0.65	–	–	0.026	–	–
L		0.50	0.70		0.020	0.028
α		0°	8°		0°	8°
N		8			8	
CP			0.08			0.003

Figure 13. TSSOP8 (DW)

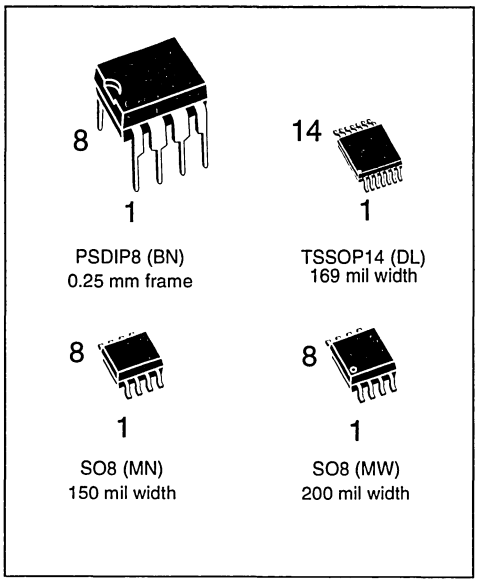


Note: 1. Drawing is not to scale.

M24C64
M24C32

64/32 Kbit Serial I²C Bus EEPROM

- Compatible with I²C Extended Addressing
- Two Wire I²C Serial Interface
  Supports 400 kHz Protocol
- Single Supply Voltage:
  - 4.5V to 5.5V for M24Cxx
  - 2.5V to 5.5V for M24Cxx-W
  - 1.8V to 3.6V for M24Cxx-R
- Hardware Write Control
- BYTE and PAGE WRITE (up to 32 Bytes)
- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Behaviour
- 1 Million Erase/Write Cycles (minimum)
- 40 Year Data Retention (minimum)



DESCRIPTION

These electrically erasable programmable memory (EEPROM) devices are fabricated with STMicroelectronics' High Endurance, Single Polysilicon, CMOS technology. This guarantees an endurance typically well above one million Erase/Write cycles, with a data retention of 40 years. The memories are organised as 8192x8 bits (M24C64) and 4096x8 bits (M24C32), and operate down to 2.5 V (for the -W version of each de-

Table 1. Signal Names

E0, E1, E2	Chip Enable Inputs
SDA	Serial Data/Address Input/ Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

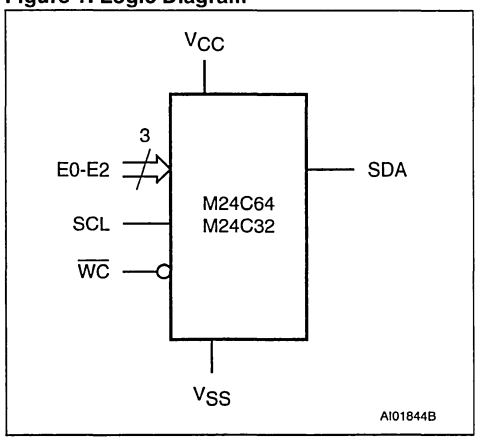


Figure 2A. DIP Connections

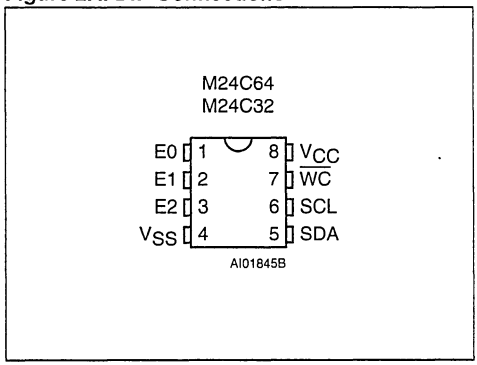
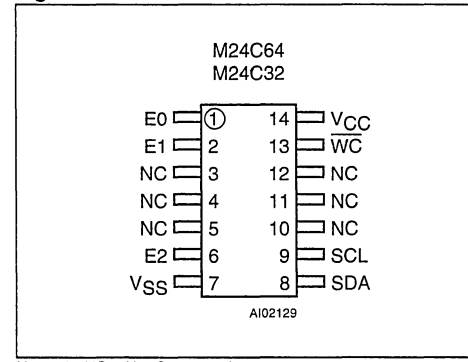
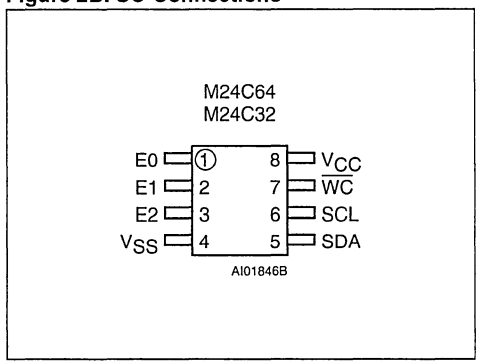


Figure 2C. TSSOP Connections



Note: 1 NC = Not Connected

Figure 2B. SO Connections



vice), and down to 1.8 V (for the -R version of each device).

The M24C64 and M24C32 are available in Plastic Dual-in-Line, Plastic Small Outline and Thin Shrink Small Outline packages.

These memory devices are compatible with the I^2C extended memory standard. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The memory carries a built-in 4-bit unique Device Type Identifier code (1010) in accordance with the I^2C bus definition.

The memory behaves as a slave device in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		-40 to 125	°C
T_{STG}	Storage Temperature		-65 to 150	°C
T_{LEAD}	Lead Temperature during Soldering	PSDIP8: 10 sec SO8: 40 sec TSSOP14: t.b.c.	260 215 t.b.c.	°C
V_{IO}	Input or Output range		-0.6 to 6.5	V
V_{CC}	Supply Voltage		-0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]		4000	V
	Electrostatic Discharge Voltage (Machine model) [3]		500	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents

2. MIL-STD-883C, 3015.7 (100 pF, 1500 Ω)
3. EIAJ IC-121 (Condition C) (200 pF, 0 Ω)

Device Select Code and $R\overline{W}$ bit (as described in Table 3), terminated by an acknowledge bit.

When writing data to the memory, the memory inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a STOP condition after an Ack for WRITE, and after a NoAck for READ.

Power On Reset: V_{CC} Lock-Out Write Protect

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The internal reset is held active until the V_{CC} voltage has reached the POR threshold value, and all operations are disabled – the device will not respond to any command. In the same way, when V_{CC} drops from the operating voltage, below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable and valid V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTION

Serial Clock (SCL)

The SCL input pin is used to strobe all data in and out of the memory. In applications where this line is used by slaves to synchronize the bus to a slower clock, the master must have an open drain output, and a pull-up resistor must be connected from the SCL line to V_{CC}. (Figure 3 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the master has a push-pull (rather than open drain) output.

Serial Data (SDA)

The SDA pin is bi-directional, and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from the SDA bus to V_{CC}. (Figure 3 indicates how the value of the pull-up resistor can be calculated).

Chip Enable (E2, E1, E0)

These chip enable inputs are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code (but note that the V_{IL} and V_{IH} levels for the inputs are CMOS compatible, not TTL compatible).

Write Control ($\overline{WC}$)

The hardware Write Control pin ($\overline{WC}$) is useful for protecting the entire contents of the memory from inadvertent erase/write. The Write Control signal is used to enable ($\overline{WC}$=V_{IL}) or disable ($\overline{WC}$=V_{IH}) write instructions to the entire memory area. When unconnected, the $\overline{WC}$ input is internally read as V_{IL}, and write operations are allowed.

When $\overline{WC}$=1, Device Select and Address bytes are acknowledged, Data bytes are not acknowledged.

Please see the Application Note *AN404* for a more detailed description of the Write Control feature.

DEVICE OPERATION

The memory device supports the I^2C protocol. This is summarized in Figure 4, and is compared with other serial bus protocols in Application Note *AN1001*. Any device that sends data on to the bus is defined to be a transmitter, and any device that

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus

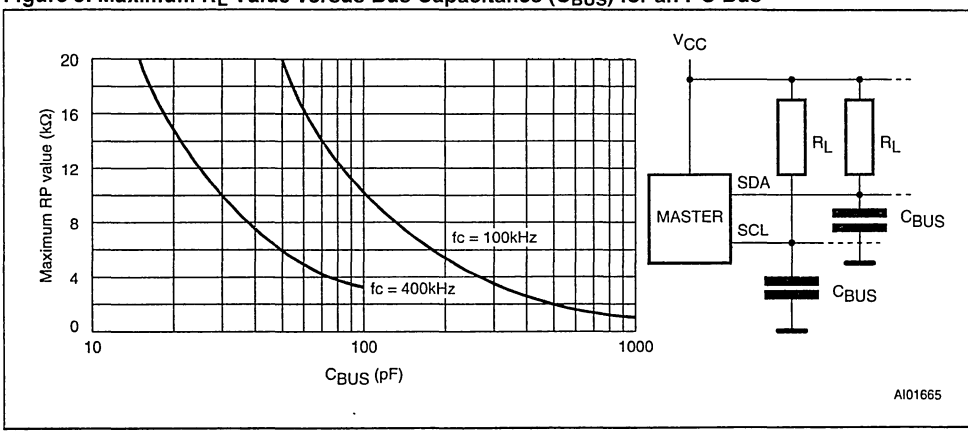
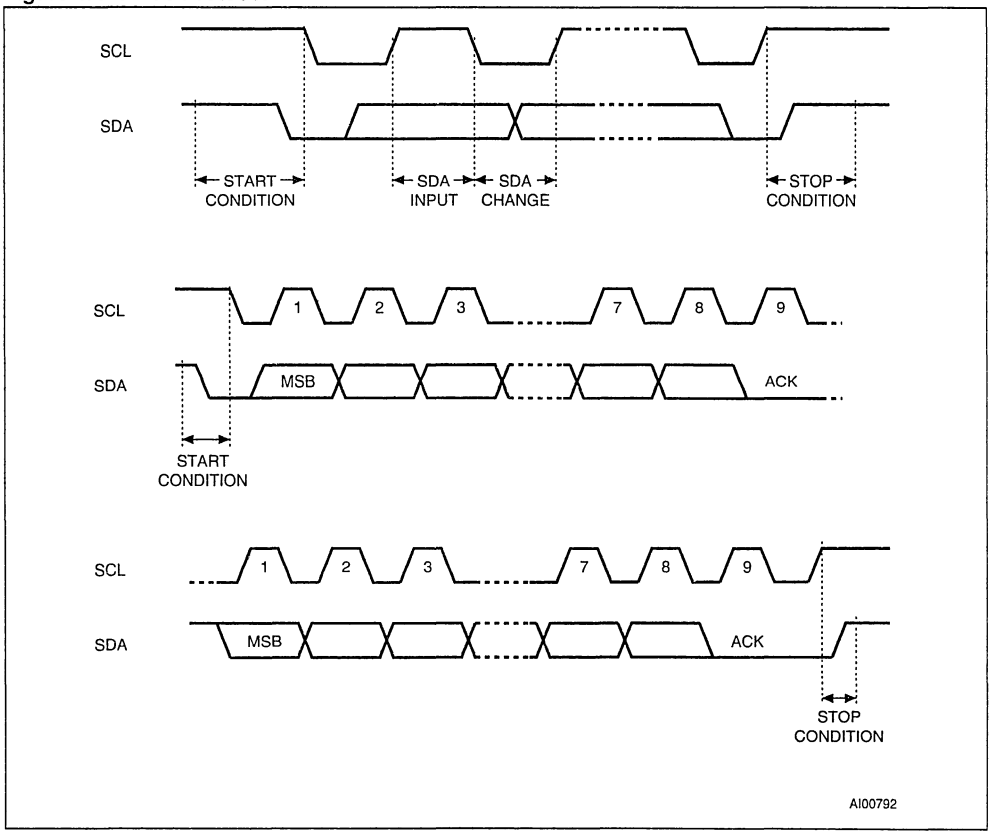


Figure 4. I²C Bus Protocol



reads the data to be a receiver. The device that controls the data transfer is known as the master, and the other as the slave. A data transfer can only be initiated by the master, which will also provide the serial clock for synchronization. The memory device is always a slave device in all communication.

Start Condition

START is identified by a high to low transition of the SDA line while the clock, SCL, is stable in the high state. A START condition must precede any data transfer command. The memory device continuously monitors (except during a programming cycle) the SDA and SCL lines for a START condition, and will not respond unless one is given.

Stop Condition

STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the memory device and the bus master. A STOP condition at the end of a Read command, after (and only after) a NoAck, forces the memory device into its standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK)

An acknowledge signal is used to indicate a successful byte transfer. The bus transmitter, whether it be master or slave, releases the SDA bus after sending eight bits of data. During the 9th clock pulse period, the receiver pulls the SDA bus low to acknowledge the receipt of the eight data bits.

Data Input

During data input, the memory device samples the SDA bus signal on the rising edge of the clock, SCL. For correct device operation, the SDA signal must be stable during the clock low-to-high transition, and the data must change *only* when the SCL line is low.

Table 3. Device Select Code [1]

	Device Type Identifier				Chip Enable			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select Code	1	0	1	0	E2	E1	E0	RW

Note: 1. The most significant bit, b7, is sent first.

Memory Addressing

To start communication between the bus master and the slave memory, the master must initiate a START condition. Following this, the master sends the 8-bit byte, shown in Table 3, on the SDA bus line (most significant bit first). This consists of the 7-bit Device Select Code, and the 1-bit Read/Write Designator (RW). The Device Select Code is further subdivided into: a 4-bit Device Type Identifier, and a 3-bit Chip Enable "Address" (E2, E1, E0).

To address the memory array, the 4-bit Device Type Identifier is 1010b.

If all three chip enable inputs are connected, up to eight memory devices can be connected on a single I^2C bus. Each one is given a unique 3-bit code on its Chip Enable inputs. When the Device Select Code is received on the SDA bus, the memory only responds if the Chip Select Code is the same as the pattern applied to its Chip Enable pins.

The 8th bit is the RW bit. This is set to '1' for read and '0' for write operations. If a match occurs on the Device Select Code, the corresponding memory gives an acknowledgment on the SDA bus during the 9th bit time. If the memory does not match the Device Select Code, it deselects itself from the bus, and goes into stand-by mode.

There are two modes both for read and write. These are summarized in Table 6 and described later. A communication between the master and the slave is ended with a STOP condition.

Each data byte in the memory has a 16-bit (two byte wide) address. The Most Significant Byte (Table 4) is sent first, followed by the Least significant Byte (Table 5). Bits b15 to b0 form the address of the byte in memory. Bits b15 to b13 are treated as a Don't Care bit on the M24C64 memory. Bits b15 to b12 are treated as Don't Care bits on the M24C32 memory.

Table 4. Most Significant Byte

b15	b14	b13	b12	b11	b10	b9	b8

Note: 1 b15 to b13 are Don't Care on the M24C64 series.
b15 to b12 are Don't Care on the M24C32 series.

Table 5. Least Significant Byte

b7	b6	b5	b4	b3	b2	b1	b0

Write Operations

Following a START condition the master sends a Device Select Code with the RW bit set to '0', as shown in Table 6. The memory acknowledges this, and waits for two address bytes. The memory responds to each address byte with an acknowledge bit, and then waits for the data byte.

Writing to the memory may be inhibited if the WC input pin is taken high. Any write command with WC=1 (during a period of time from the START condition until the end of the two address bytes) will not modify the memory contents, and the accompanying data bytes will *not* be acknowledged (as shown in Figure 5).

Byte Write

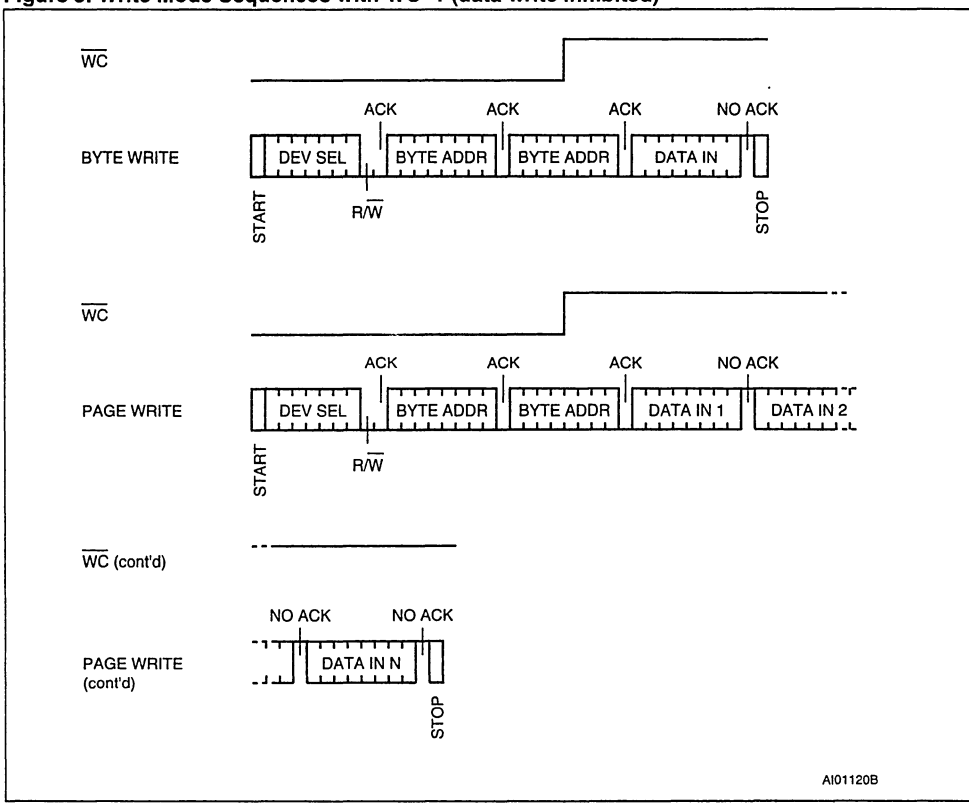
In the Byte Write mode, after the Device Select Code and the address bytes, the master sends

Table 6. Operating Modes

Mode	RW bit	WC [1]	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, RW = '1'
Random Address Read	'0'	X	1	START, Device Select, RW = '0', Address
	'1'	X		reSTART, Device Select, RW = '1'
Sequential Read	'1'	X	≥ 1	Similar to Current or Random Address Read
Byte Write	'0'	V_{IL}	1	START, Device Select, RW = '0'
Page Write	'0'	V_{IL}	≤ 32	START, Device Select, RW = '0'

Note. 1. X = V_{IH} or V_{IL}.

Figure 5. Write Mode Sequences with $\overline{WC}$=1 (data write inhibited)



one data byte. If the addressed location is write protected by the $\overline{WC}$ pin, the memory replies with a NoAck, and the location is not modified. If, instead, the $\overline{WC}$ pin has been held at 0, as shown in Figure 6, the memory replies with an Ack. The master terminates the transfer by generating a STOP condition.

Page Write

The Page Write mode allows up to 32 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the most significant memory address bits (b12-b5 for the M24C64 and b11-b5 for the M24C32) are the same. If more bytes are sent than will fit up to the end of the row, a condition known as 'roll-over' occurs. Data starts to become overwritten (in a way not formally specified in this data sheet).

The master sends from one up to 32 bytes of data, each of which is acknowledged by the memory if the $\overline{WC}$ pin is low. If the $\overline{WC}$ pin is high, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck. After each byte is transferred, the internal byte address counter (the 5 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition.

When the master generates a STOP condition immediately after the Ack bit (in the "10^{th} bit" time slot), either at the end of a byte write or a page write, the internal memory write cycle is triggered. A STOP condition at any other time does not trigger the internal write cycle.

During the internal write cycle, the SDA input is disabled internally, and the device does not respond to any requests.

Figure 6. Write Mode Sequences with $\overline{WC}$=0 (data write enabled)

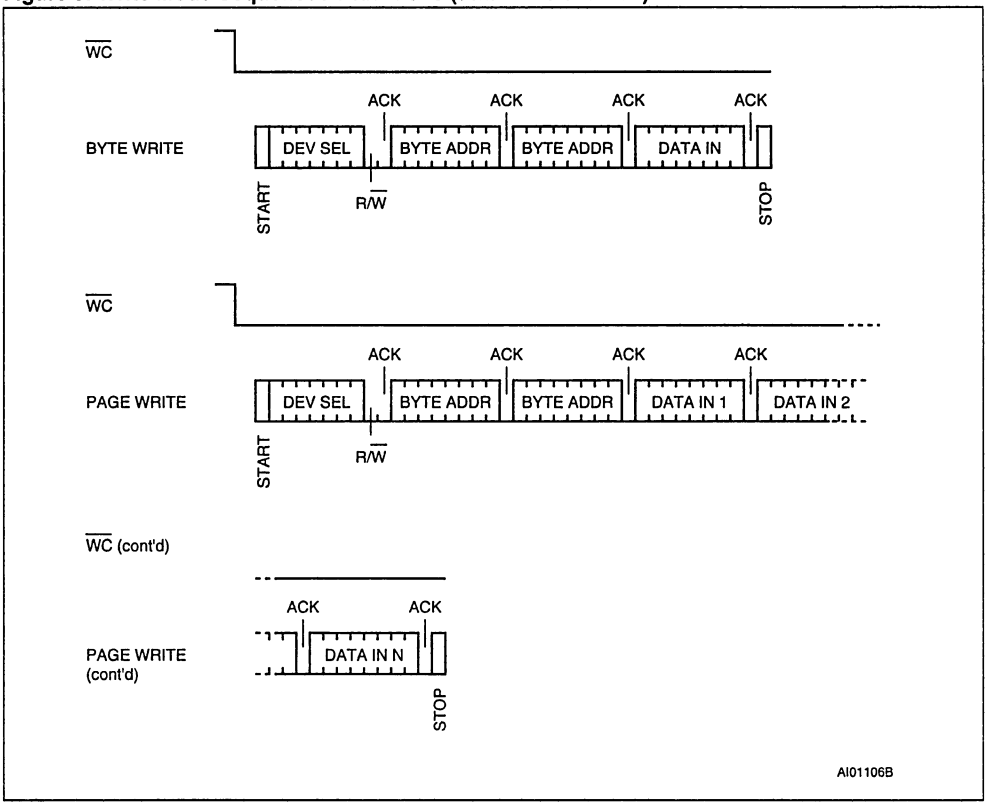
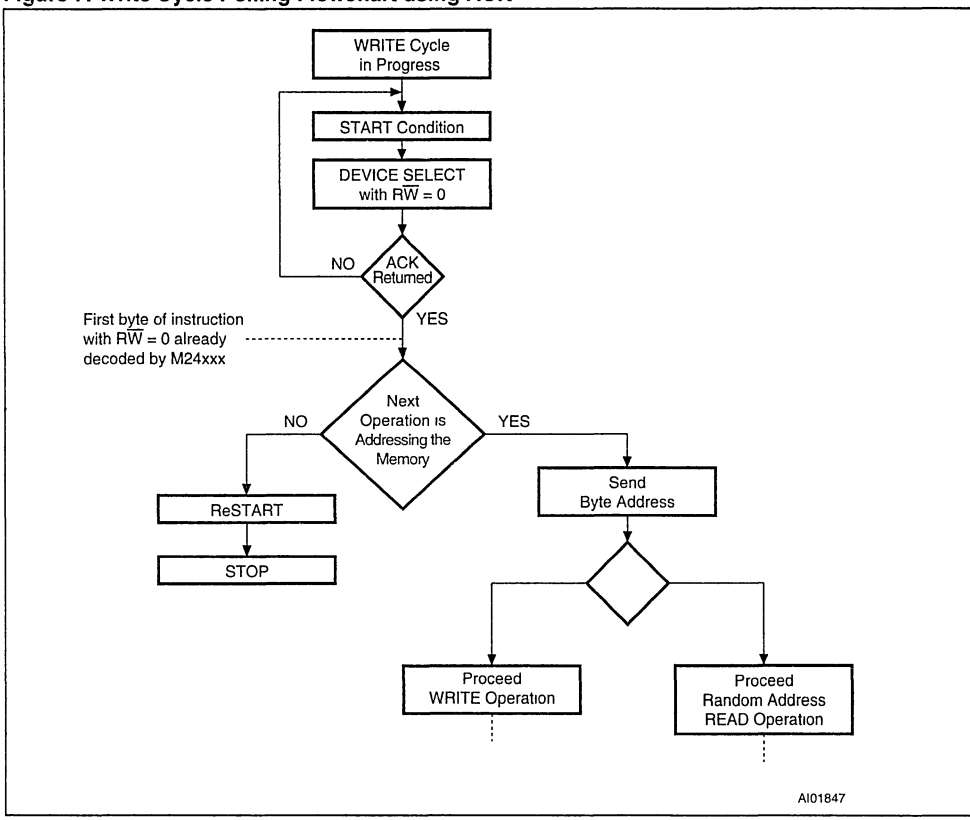


Figure 7. Write Cycle Polling Flowchart using ACK



Minimizing System Delays by Polling On ACK

During the internal write cycle, the memory disconnects itself from the bus, and copies the data from its internal latches to the memory cells. The maximum write time (t_W) is shown in Table 9, but the typical time is shorter. To make use of this, an Ack polling sequence can be used by the master.

The sequence, as shown in Figure 7, is:

- Initial condition: a Write is in progress.
- Step 1: the master issues a START condition followed by a Device Select Code (the first byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no Ack will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it responds with an Ack, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction having been sent during Step 1).

Read Operations

Read operations are performed independently of the state of the $\overline{WC}$ pin.

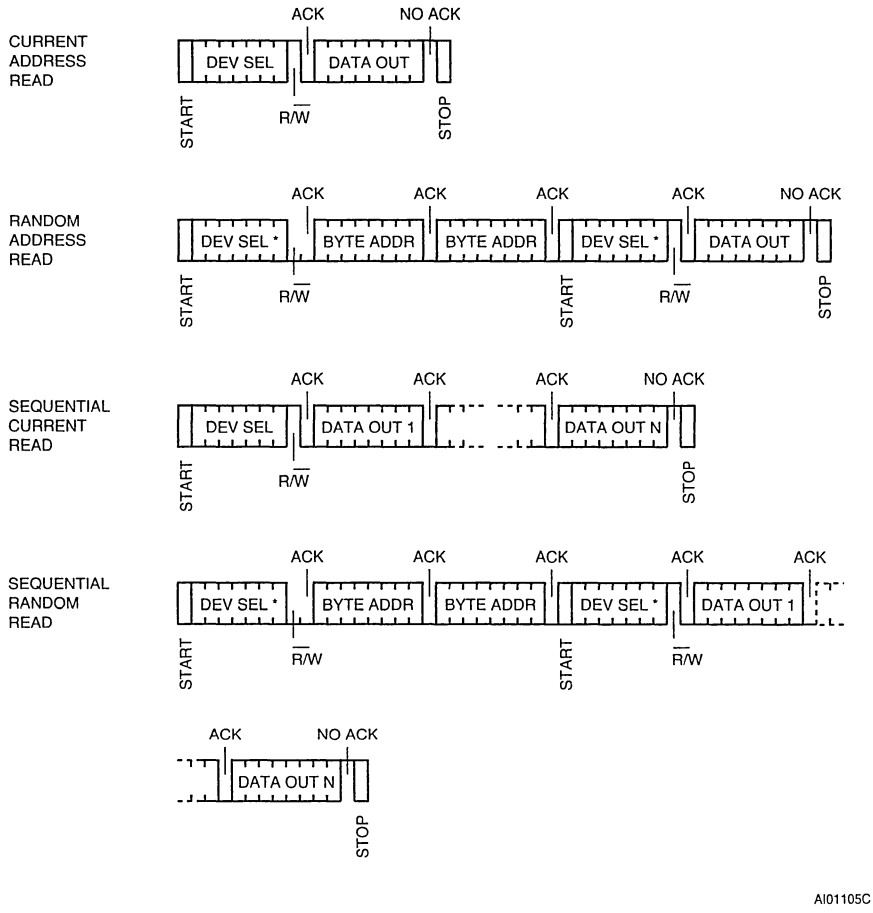
Random Address Read

A dummy write is performed to load the address into the address counter, as shown in Figure 8. Then, *without* sending a STOP condition, the master sends another START condition, and repeats the Device Select Code, with the $\overline{RW}$ bit set to '1'. The memory acknowledges this, and outputs the contents of the addressed byte. The master must *not* acknowledge the byte output, and terminates the transfer with a STOP condition.

Current Address Read

The device has an internal address counter which is incremented each time a byte is read. For the Current Address Read mode, following a START condition, the master sends a Device Select Code with the $\overline{RW}$ bit set to '1'. The memory acknowledges this, and outputs the byte addressed by the

Figure 8. Read Mode Sequences



Note: 1. The seven most significant bits of the Device Select Code of a Random Read (in the 1st and 4th bytes) must be identical

internal address counter. The counter is then incremented. The master terminates the transfer with a STOP condition, as shown in Figure 8, *without* acknowledging the byte output.

Sequential Read

This mode can be initiated with either a Current Address Read or a Random Address Read. The master *does* acknowledge the data byte output in this case, and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must *not* acknowledge the last byte output, and *must* generate a STOP condition.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over' and the memory continues to output data from the start of the memory block.

Acknowledge in Read Mode

In all read modes, the memory waits, after each byte read, for an acknowledgment during the 9th bit time. If the master does not pull the SDA line low during this time, the memory terminates the data transfer and switches to its standby state.

Table 7. DC Characteristics
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 4.5 to 5.5 V or 2.5 to 5.5 V)
(T_A = 0 to 70 °C or -20 to 85 °C; V_{CC} = 1.8 to 3.6 V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$0 V \le V_{IN} \le V_{CC}$		± 2	µA
I_{LO}	Output Leakage Current	$0 V \le V_{OUT} \le V_{CC}$, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current -W series:	V_{CC}=5V, f_c=400kHz (rise/fall time < 30ns)		2	mA
		V_{CC}=2.5V, f_c=400kHz (rise/fall time < 30ns)		1	mA
	-R series:	V_{CC}=1.8V, f_c=100kHz (rise/fall time < 30ns)		0.8[1]	mA
I_{CC1}	Supply Current (Stand-by)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5 V		10	µA
I_{CC2}	Supply Current (Stand-by)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5 V		2	µA
I_{CC3}	Supply Current (Stand-by)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8 V		1[1]	µA
V_{IL}	Input Low Voltage (E0-E2, SCL, SDA)		- 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (E0-E2, SCL, SDA)		0.7V_{CC}	V_{CC}+1	V
V_{IL}	Input Low Voltage ($\overline{WC}$)		- 0.3	0.5	V
V_{IH}	Input High Voltage ($\overline{WC}$)		0.7V_{CC}	V_{CC}+1	V
V_{OL}	Output Low Voltage -W series:	I_{OL} = 3 mA, V_{CC} = 5 V		0.4	V
		I_{OL} = 2.1 mA, V_{CC} = 2.5 V		0.4	V
	-R series:	I_{OL} = 0.15 mA, V_{CC} = 1.8 V		0.2[1]	V

Note: 1. This is preliminary data.

Table 8. Input Parameters[1] (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} < 0.3V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} > 0.7V_{CC}$	500		kΩ
t_{NS}	Low Pass Filter Input Time Constant (SCL and SDA)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 9. AC Characteristics
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 4.5 to 5.5 V or 2.5 to 5.5 V)
(T_A = 0 to 70 °C or -20 to 85 °C; V_{CC} = 1.8 to 3.6 V)

Symbol	Alt.	Parameter	M24C64 / M24C32						Unit
			V_{CC}=4.5 to 5.5 V T_A=0 to 70°C or -40 to 85°C		V_{CC}=2.5 to 5.5 V T_A=0 to 70°C or -40 to 85°C		V_{CC}=1.8 to 3.6 V T_A=0 to 70°C or -20 to 85°C[4]		
			Min	Max	Min	Max	Min	Max	
t_{CH1CH2}	t_R	Clock Rise Time		300		300		1000	ns
t_{CL1CL2}	t_F	Clock Fall Time		300		300		300	ns
t_{DH1DH2}[2]	t_R	SDA Rise Time	20	300	20	300	20	1000	ns
t_{DL1DL2}[2]	t_F	SDA Fall Time	20	300	20	300	20	300	ns
t_{CHDX}[1]	$t_{SU\ STA}$	Clock High to Input Transition	600		600		4700		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		600		4000		ns
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	600		600		4000		ns
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		0		0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		1.3		4.7		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	100		100		250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	600		600		4000		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		1.3		4.7		µs
t_{CLQV}[3]	t_{AA}	Clock Low to Data Out Valid	200	900	200	900	200	3500	ns
t_{CLQX}	t_{DH}	Data Out Hold Time After Clock Low	200		200		200		ns
f_C	f_{SCL}	Clock Frequency		400		400		100	kHz
t_W	t_{WR}	Write Time		10		10		10	ms

Note: 1. For a reSTART condition, or following a write cycle.
2. Sampled only, not 100% tested.
3. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
4. This is preliminary data.

Table 10. AC Measurement Conditions

Input Rise and Fall Times	≤ 50 ns
Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}
Input and Output Timing Reference Voltages	0.3V_{CC} to 0.7V_{CC}

Figure 9. AC Testing Input Output Waveforms

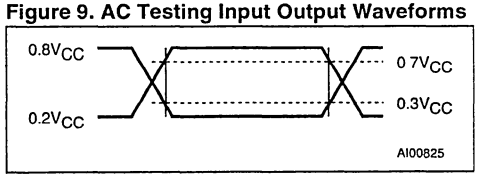


Figure 10. AC Waveforms

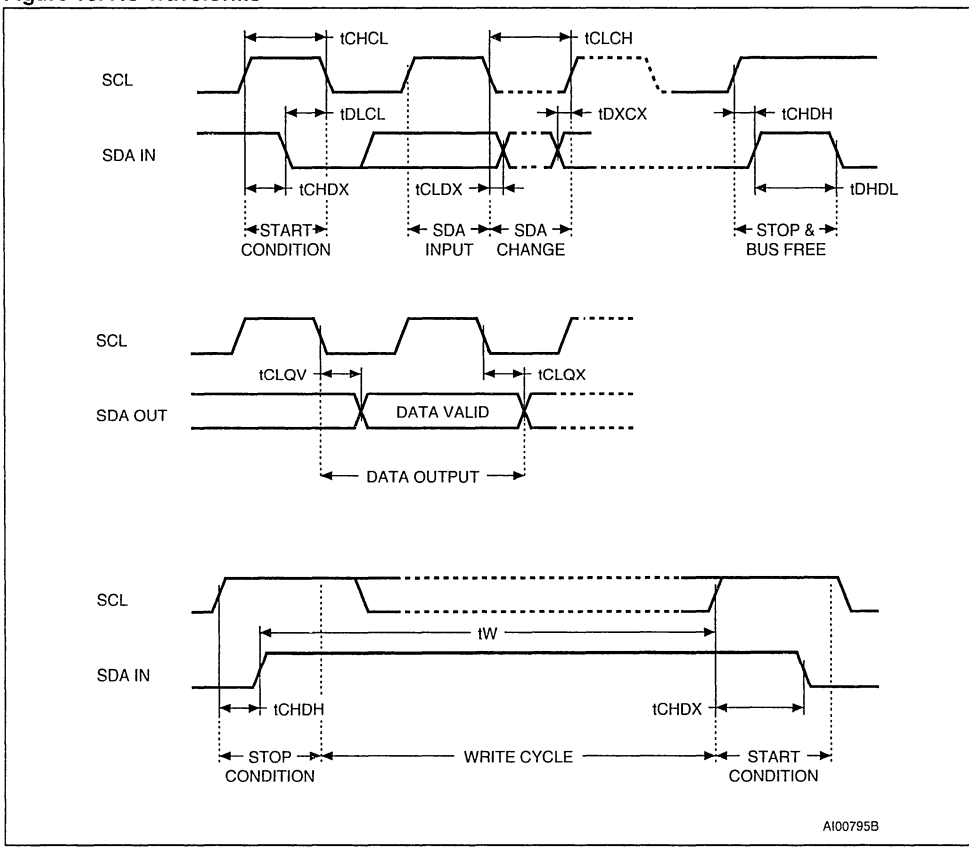


Table 11. Ordering Information Scheme

Example: M24C64 – R MN 1 T

Memory Capacity

64	64 Kbit (8K x 8)
32	32 Kbit (4K x 8)

Operating Voltage

blank	4.5 V to 5.5 V
W	2.5 V to 5.5 V
R[4]	1.8 V to 3.6 V

Package

BN	PSDIP8 (0.25 mm frame)
MN	SO8 (150 mil width)
MW	SO8 (200 mil width)
DL[1]	TSSOP14 (169 mil width)

Option

T	Tape and Reel Packing

Temperature Range

1[2]	0 °C to 70 °C
6	–40 °C to 85 °C
3[3]	–40 °C to 125 °C
5	–20 °C to 85 °C

Note: 1. For the availability of the M24C64 and M24C32 in TSSOP14, please contact the ST Sales Office nearest to you
2 Temperature range available only on request.
3 For conformity to the High Reliability Certified Flow (HRCF), please contact the ST Sales Office nearest to you
4 The -R version (V_{CC} range 1 8 V to 3.6 V) only available in temperature ranges 5 or 1.

ORDERING INFORMATION

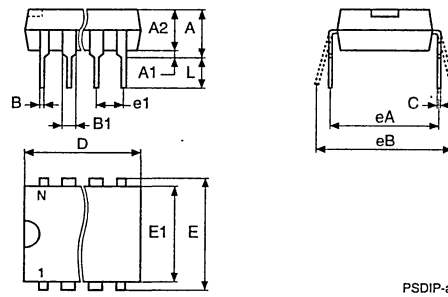
Devices are shipped from the factory with the memory content set at all '1's (FFh).

The notation used for the device number is as shown in Table 11. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 12. PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

Figure 11. PSDIP8 (BN)

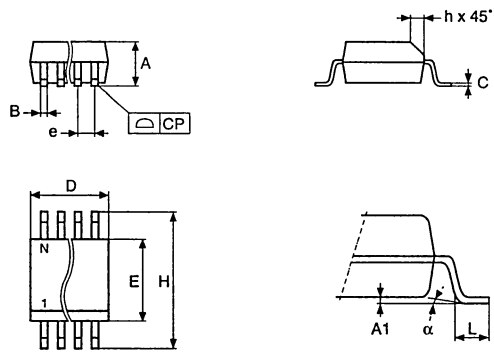


Note: 1. Drawing is not to scale.

Table 13. SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

Figure 12. SO8 narrow (MN)



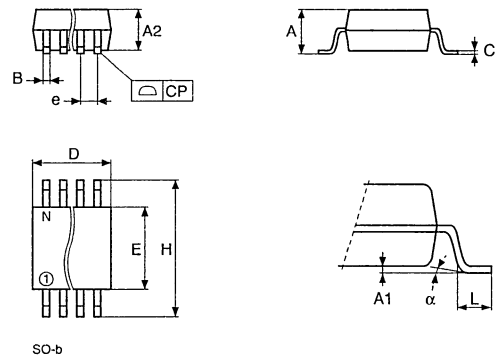
SO-a

Note: 1. Drawing is not to scale.

Table 14. SO8 - 8 lead Plastic Small Outline, 200 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			2.03			0.080
A1		0.10	0.25		0.004	0.010
A2			1.78			0.070
B		0.35	0.45		0.014	0.018
C	0.20	–	–	0.008	–	–
D		5.15	5.35		0.203	0.211
E		5.20	5.40		0.205	0.213
e	1.27	–	–	0.050	–	–
H		7.70	8.10		0.303	0.319
L		0.50	0.80		0.020	0.031
α		0°	10°		0°	10°
N		8			8	
CP			0.10			0.004

Figure 13. SO8 wide (MW)

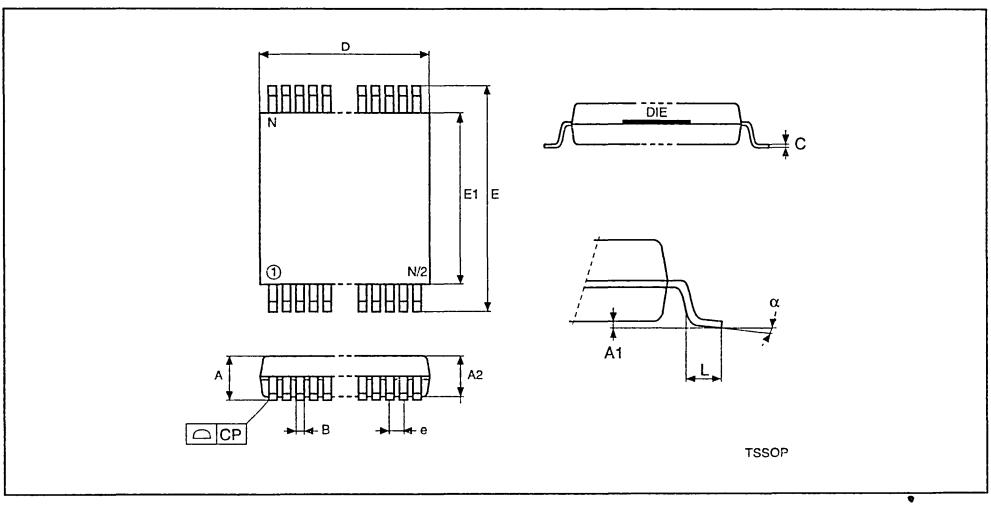


Note. 1. Drawing is not to scale.

Table 15. TSSOP14 - 14 lead Thin Shrink Small Outline

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.10			0.043
A1		0.05	0.15		0.002	0.006
A2		0.85	0.95		0.033	0.037
B		0.19	0.30		0.007	0.012
C		0.09	0.20		0.004	0.008
D		4.90	5.10		0.193	0.197
E		6.25	6.50		0.246	0.256
E1		4.30	4.50		0.169	0.177
e	0.65	–	–	0.026	–	–
L		0.50	0.70		0.020	0.028
α		0°	8°		0°	8°
N	14			14		
CP			0.08			0.003

Figure 14. TSSOP14 (DL)



Note. 1 Drawing is not to scale

M24256-A

256 Kbit Serial I^2C Bus EEPROM

PRELIMINARY DATA

- COMPATIBLE with I^2C EXTENDED ADDRESSING
- 2 CHIP ENABLE INPUTS
- TWO WIRE I^2C SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- 100,000 ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  - 4.5V to 5.5V for M24256-A
  - 2.5V to 5.5V for M24256-AW
- HARDWARE WRITE CONTROL
- BYTE and PAGE WRITE (up to 64 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH-UP PERFORMANCES

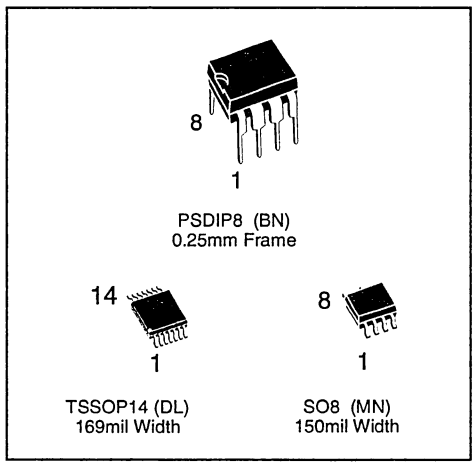
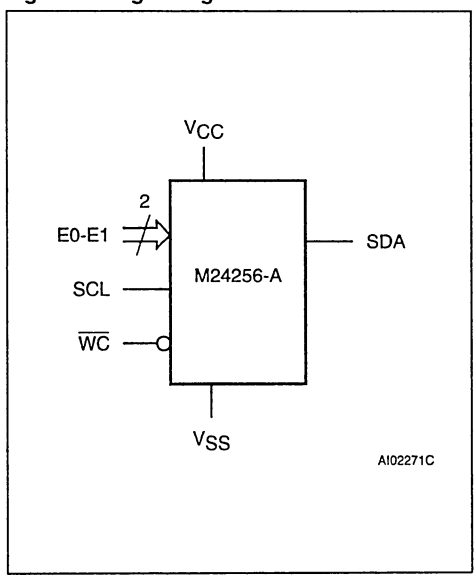


Figure 1. Logic Diagram



DESCRIPTION

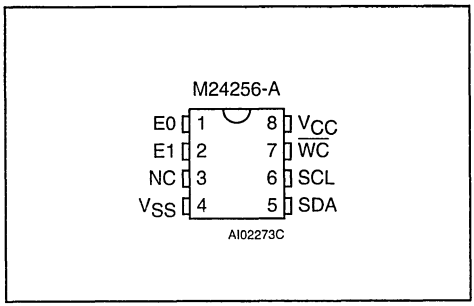
The M24256-A is a 256 Kbit electrically erasable programmable memory (EEPROM) organized as 32,768 x8 bits with two Chip Enable inputs.

The "W" versions operate with a power supply value as low as 2.5V.

Table 1. Signal Names

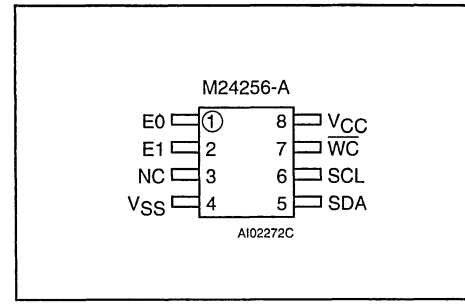
E0-E1	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections



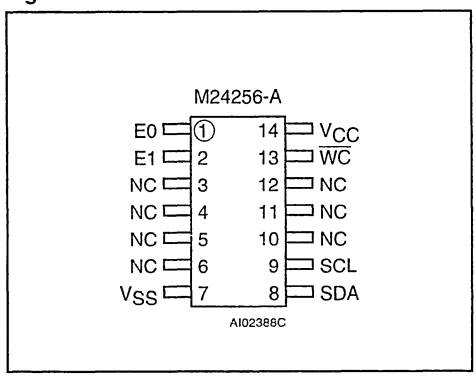
Warning: NC = Not Connected

Figure 2B. SO Pin Connections



Warning: NC = Not Connected

Figure 2C. TSOP Pin Connections



Warning: NC = Not Connected

DESCRIPTION (cont'd)

The device is compatible with the I^2C extended memory standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memory carries a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The memory behaves as a slave device in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), then 3 Chip Enable Input bits (0, E1, E0) to form a 7 bit Device Select, plus one read/write bit ($R\overline{W}$) and terminated by an acknowledge bit. Up to 4 memories may be connected to the same I^2C bus and selected individually.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature (2)			–40 to 125	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8) (PSDIP8)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.6 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (3)			4000	V
	Electrostatic Discharge Voltage (Machine model) (4)			200	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

2 Depends on range.

3 100pF through 1500Ω; MIL-STD-883C, 3015.7

4 200pF through 0Ω; EIAJ IC-121 (condition C)

Table 3. Device Select Code

	Device Code				Chip Enable			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	0	E1	E0	RW

Note: The MSB b7 is sent first

Table 4. Operating Modes

Mode	RW bit	WC	Data Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, RW = '1'
Random Address Read	'0'	X	1	START, Device Select, RW = '0', Address,
	'1'	X		reSTART, Device Select, RW = '1'
Sequential Read	'1'	X	≥ 1	As CURRENT or RANDOM Mode
Byte Write	'0'	V_{IL}	1	START, Device Select, RW = '0'
Page Write	'0'	V_{IL}	≤ 64	START, Device Select, RW = '0'

Note: 1. X = V_{IH} or V_{IL}.

When writing data to the memory, it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Chip Enable (E0, E1). These chip enable inputs are used to set the 2 least significant bits of the 7 bit device select code. They may be driven dynamically or tied to VCC or VSS to establish the device select code. When unconnected, these 2 pins are internally read as Vil (see tables 5 and 6).

Write Control (WC). The Write Control feature WC is useful to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable (WC=V_{IH}) or disable (WC=V_{IL}) the internal write protection. When the WC pin is unconnected, the WC input is internally read as V_{IL} (see Table 5).

When WC=1, Device Select and Address bytes are acknowledged, Data bytes are not acknowledged.

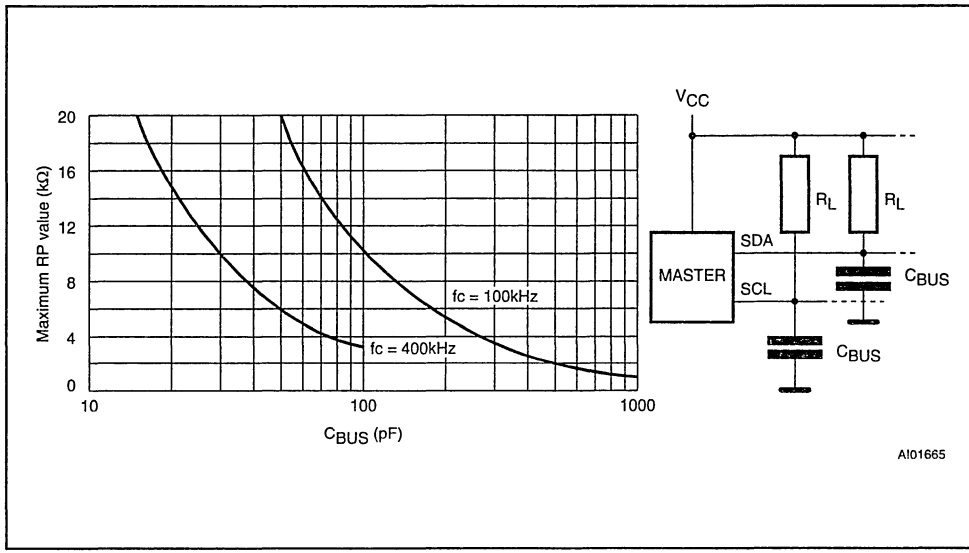
Refer to Application Note AN404 for more detailed information about Write Control feature.

DEVICE OPERATION

I^2C Bus Background

The memory supports the extended addressing I^2C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The memory is always a slave device in all communications.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus



Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the memory continuously monitors the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the memory and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the memory samples the SDA bus signal on the rising edge of the clock SCL. For correct device operation, the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Device Selection. To start communication between the bus master and the slave memory, the master must initiate a START condition. The 8 bits sent after a START condition are made up of a device select of 4 bits that identifies the device type, then 3 Chip Enable Input bits (0, E1, $\overline{E0}$) and one bit for a READ ($\overline{RW}$=1) or WRITE ($\overline{RW}$=0) operation. There are two modes both for read and write. These are summarized in Table 4 and described hereafter. A communication between the master and the slave is ended with a STOP condition.

Memory Addressing. A data byte in the memory is addressed through 2 bytes of address information. The Most Significant Byte is sent first and the Least significant Byte is sent after. Bits b15 to b0 form the address of any byte of the memory. Bit b15 is don't care on the M24256-A series.

Most Significant Byte

b15	b14	b13	b12	b11	b10	b9	b8

b15 is don't care on M24256-A series.

Least Significant Byte

b7	b6	b5	b4	b3	b2	b1	b0

Table 5. Input Parameters [1] (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_L	E1, E0, $\overline{WC}$ Input Impedance	$V_{IN} \leq 0.5V$	50	300	kΩ
Z_H	E1, E0, $\overline{WC}$ Input Impedance	$V_{IN} \geq V_{CC}$ - 0.5V	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V or 2.5 to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LI}	Input Leakage Current (E0, E1, WC)	$0V \leq V_{IN} \leq V_{CC}$		±5	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_C = 400kHz (Rise/Fall time < 30ns)		2	mA
	Supply Current (-W series)	V_{CC} = 2.5V, f_C = 400kHz (Rise/Fall time < 30ns)		1	mA
I_{CC1}	Supply Current, Standby	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		10	µA
I_{CC2}	Supply Current, Standby (-W series)	VIN = V_{SS} or V_{CC}, V_{CC} = 2.5V		2	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0, E1, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0, E1, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (-W series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V

Table 7. AC Characteristics

Symbol	Alt	Parameter	M24256-A				Unit
			V_{CC} = 4.5V to 5.5V T_A = 0 to 70°C T_A = –40 to 85°C		V_{CC} = 2.5V to 5.5V T_A = 0 to 70°C T_A = –40 to 85°C		
			Min	Max	Min	Max	
t_{CH1CH2}	t_R	Clock Rise Time		300		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300		300	ns
t_{DH1DH2} (1)	t_R	SDA Rise Time	20	300	20	300	ns
t_{DL1DL2} (1)	t_F	SDA Fall Time	20	300	20	300	ns
t_{CHDX} (2)	$t_{SU\ STA}$	Clock High to Input Transition	600		600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		600		ns
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	600		600		ns
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1300		1300		ns
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	100		100		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	600		600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1300		1300		ns
t_{CLQV} (3)	t_{AA}	Clock Low to Next Data Out Valid	200	900	200	900	ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		200		ns
f_C	f_{SCL}	Clock Frequency		400		400	kHz
t_W	t_{WR}	Write Time		10		10	ms

Notes: 1. Sampled only, not 100% tested
2. For a reSTART condition, or following a write cycle.
3. The minimum value delays the falling/rising edge of SDA away form SCL = 1 in order to avoid unwanted START and/or STOP condition.

Write Operations

Following a START condition the master sends a Device Select code with the $\overline{RW}$ bit set to '0'. The memory acknowledges this and waits for 2 bytes of address. These 2 address bytes (8 bits each) provide access to any of the memory locations. Writing in the memory may be inhibited if input pin $\overline{WC}$ is taken high.

Any write command with $\overline{WC}$=1 (during a period of time from the START condition until the end of the 2 bytes address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 9.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition.

Figure 4. AC Testing Input Output Waveforms

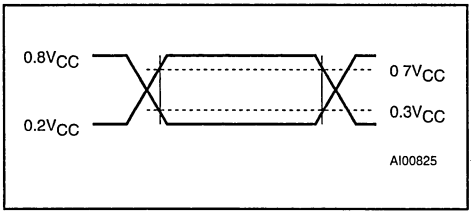


Table 8. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}
Input and Output Timing Ref. Voltages	0.3V_{CC} to 0.7V_{CC}

Figure 5. AC Waveforms

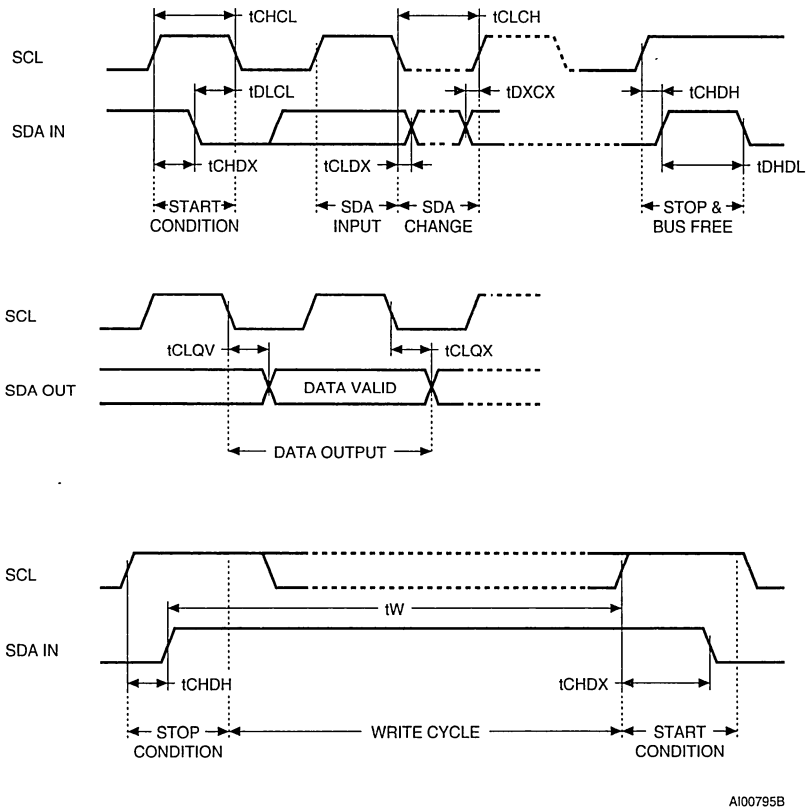
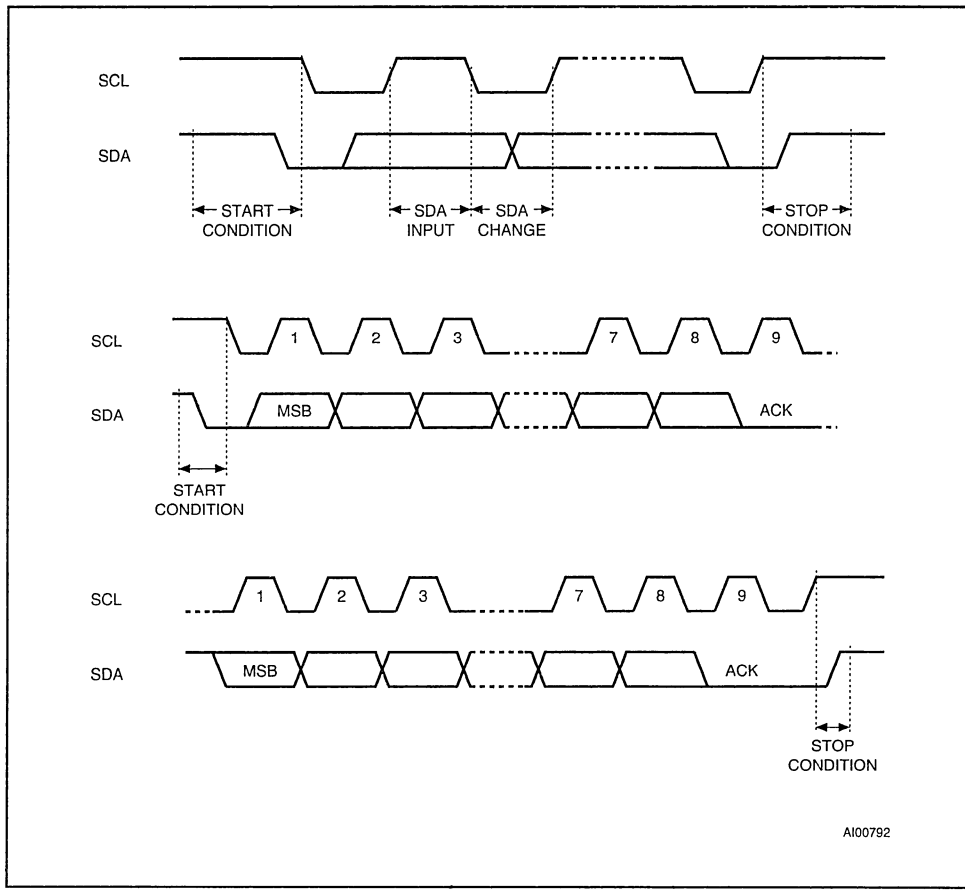


Figure 6. I²C Bus Protocol



Page Write. The Page Write mode allows up to 64 bytes to be written in a single write cycle, provided that they are all located in the same row of 64 bytes in the memory, that is the same address bits (b14-b6 for the M24256-A).

The master sends from one up to 64 bytes of data, which are each acknowledged by the memory. After each byte is transferred, the internal byte address counter (6 Least Significant Bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. This STOP condition will trigger an internal memory program cycle only if the STOP condition is internally decoded right after the ACK bit; any STOP condition decoded out of this "10th bit" time slot will not trigger the internal programming cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal Write cycle, the memory disable itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the Write time (t_W) is given in the Table 8, this timing value may be reduced by an ACK polling sequence issued by the master.

The sequence is:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
- Step 2: if the memory is internally writing, NoACK will be returned. The master goes back to Step 1. If the memory has terminated the internal writing, it will issue an ACK.
  The memory is ready to receive the second part of the instruction (the first byte of this instruction was already sent during Step 1).

Read Operations

On delivery, the memory contents is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a Device Select with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Figure 7. Write Cycle Polling using ACK

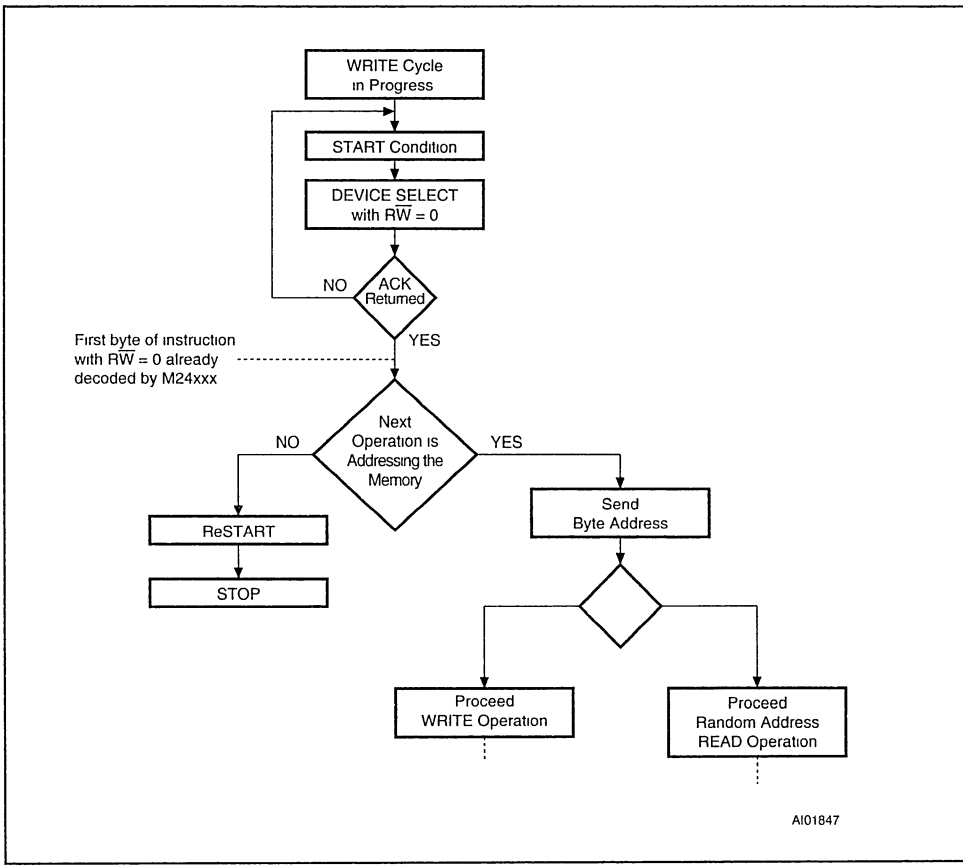
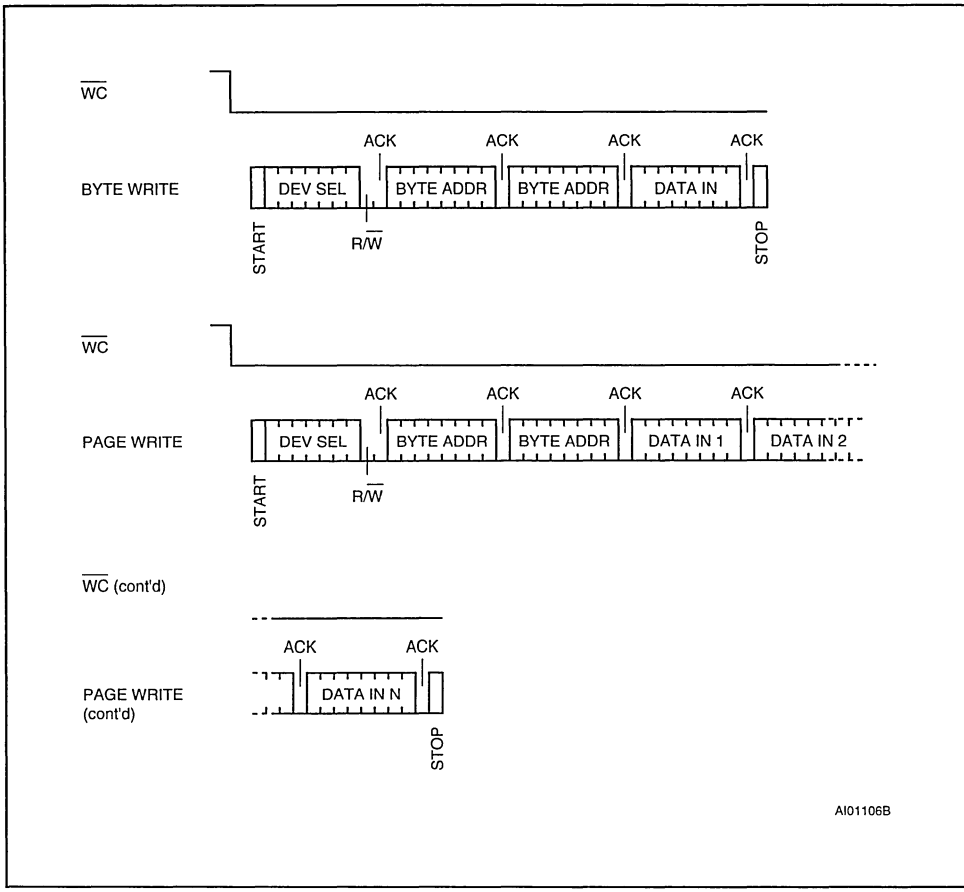


Figure 8. Write Modes Sequence with Write Control = 0



Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address repeated with the RW bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master have to NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the memory waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the memory terminates the data transfer and switches to a standby state.

Figure 9. Write Modes Sequence with Write Control = 1

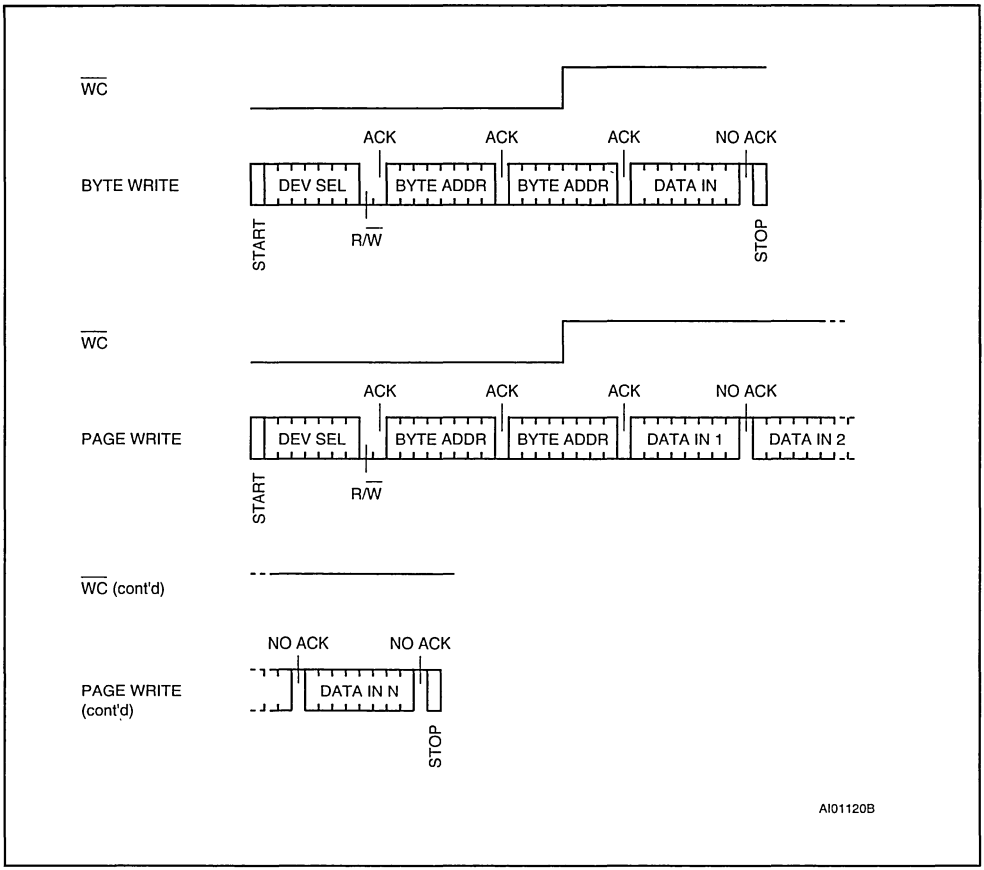
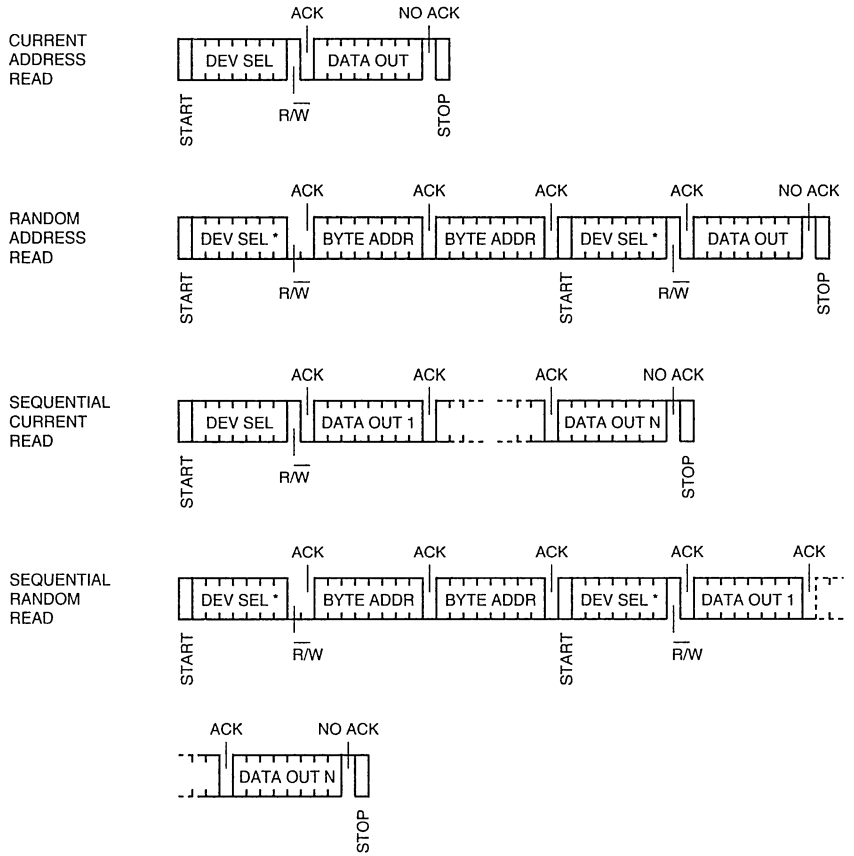
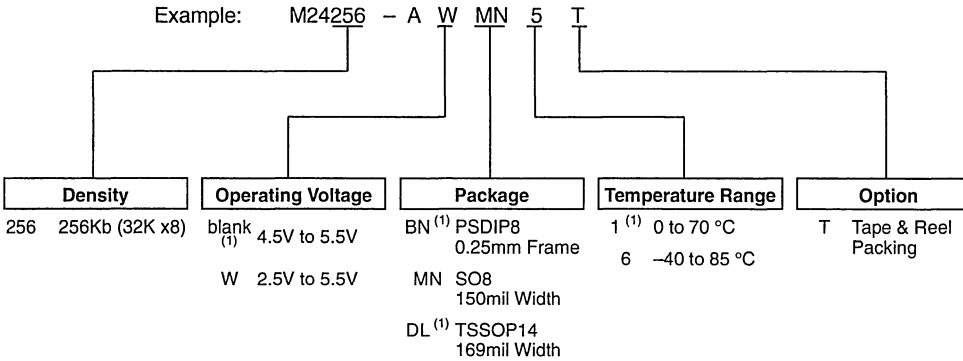


Figure 10. Read Mode Sequences



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 4th byte) must be identical.

ORDERING INFORMATION SCHEME



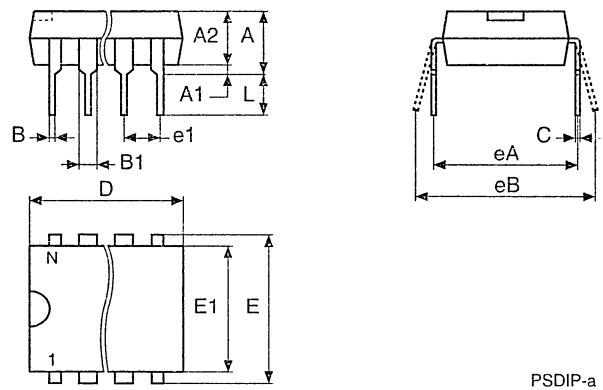
Notes: 1. On request only.

Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

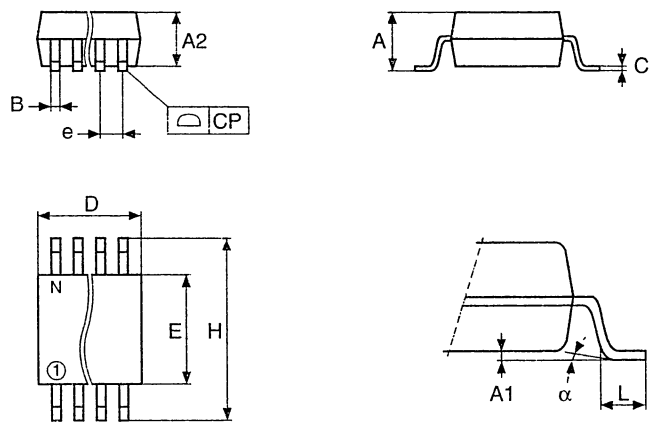


PSDIP-a

Drawing is not o scale

TSSOP14 - 14 lead Thin Shrink Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.10			0.043
A1		0.05	0.15		0.002	0.006
A2		0.85	0.95		0.033	0.037
B		0.19	0.30		0.007	0.012
C		0.09	0.20		0.004	0.008
D		4.90	5.10		0.193	0.197
E		6.25	6.50		0.246	0.256
E1		4.30	4.50		0.169	0.177
e	0.65	–	–	0.026	–	–
L		0.50	0.70		0.020	0.028
α		0°	8°		0°	8°
N	14			14		
CP			0.08			0.003

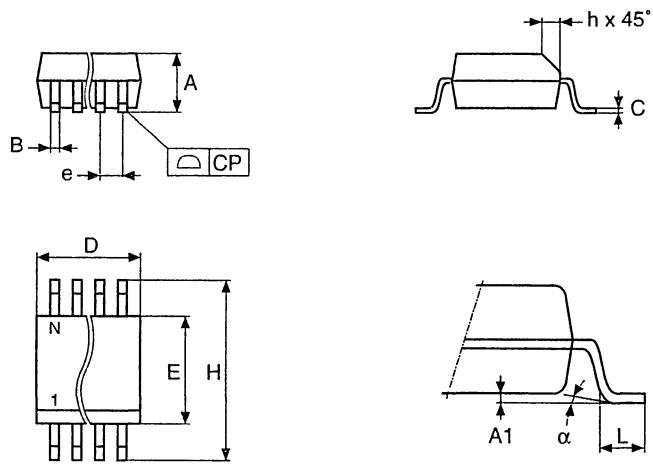


SO-b

Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0	8		0	8
N		8			8	
CP			0.10			0.004



SO-a

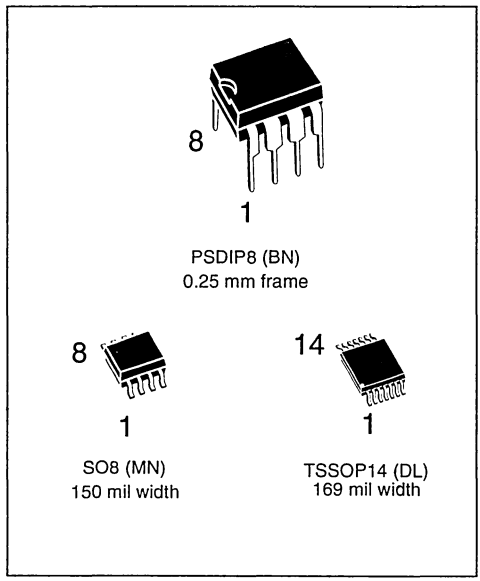
Drawing is not to scale.

M24256-B
M24128-B

256/128 Kbit Serial I²C Bus EEPROM With Three Chip Enable Lines

PRELIMINARY DATA

- Compatible with I²C Extended Addressing
- Two Wire I²C Serial Interface Supports 400 kHz Protocol
- Single Supply Voltage:
  - 4.5V to 5.5V for M24xxx-B
  - 2.5V to 5.5V for M24xxx-BW
  - 1.8V to 3.6V for M24xxx-BR
- Hardware Write Control
- BYTE and PAGE WRITE (up to 64 Bytes)
- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Behaviour
- 100000 Erase/Write Cycles (minimum)
- 40 Year Data Retention (minimum)



DESCRIPTION

These electrically erasable programmable memory (EEPROM) devices are fabricated with STMicroelectronics' High Endurance, Double Polysilicon, CMOS technology. This guarantees an endurance typically well above one hundred thousand Erase/Write cycles, with a data retention of 40 years. The memories are organised as 32Kx8 bits (M24256-B) and 16Kx8 bits (M24128-B), and operate down to 2.5 V (for the -W version

Table 1. Signal Names

E0, E1, E2	Chip Enable Inputs
SDA	Serial Data/Address Input/ Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

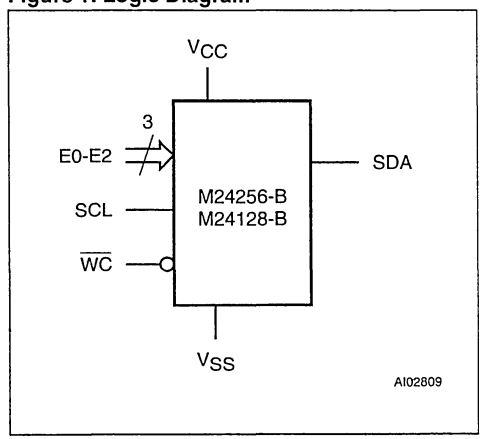


Figure 2A. DIP Connections

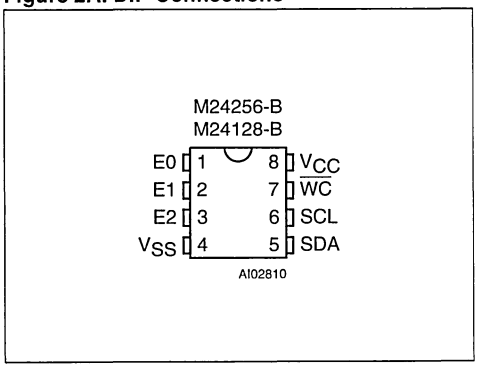
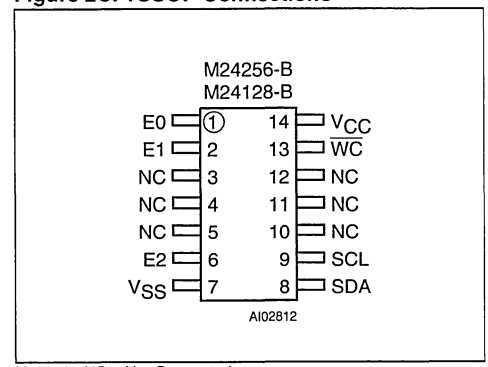
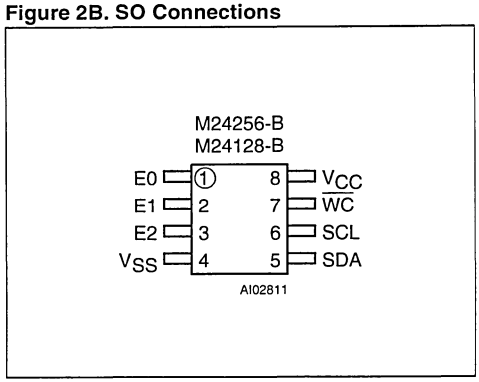


Figure 2C. TSSOP Connections



Note: 1. NC = Not Connected

Figure 2B. SO Connections



of each device), and down to 1.8 V (for the -R version of each device).

The M24256-B and M24128-B are available in Plastic Dual-in-Line, Plastic Small Outline and Thin Shrink Small Outline packages.

These memory devices are compatible with the I^2C extended memory standard. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The memory carries a built-in 4-bit unique Device Type Identifier code (1010) in accordance with the I^2C bus definition.

The memory behaves as a slave device in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		-40 to 125	°C
T_{STG}	Storage Temperature		-65 to 150	°C
T_{LEAD}	Lead Temperature during Soldering	PSDIP8: 10 sec SO8: 40 sec TSSOP14: t.b.c.	260 215 t.b.c.	°C
V_{IO}	Input or Output range		-0.6 to 6.5	V
V_{CC}	Supply Voltage		-0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]		4000	V
	Electrostatic Discharge Voltage (Machine model) [3]		500	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100 pF, 1500 Ω)
3. EIAJ IC-121 (Condition C) (200 pF, 0 Ω)

Device Select Code and R$\overline{W}$ bit (as described in Table 3), terminated by an acknowledge bit.

When writing data to the memory, the memory inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a STOP condition after an Ack for WRITE, and after a NoAck for READ.

Power On Reset: V_{CC} Lock-Out Write Protect

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The internal reset is held active until the V_{CC} voltage has reached the POR threshold value, and all operations are disabled – the device will not respond to any command. In the same way, when V_{CC} drops from the operating voltage, below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable and valid V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTION

Serial Clock (SCL)

The SCL input pin is used to strobe all data in and out of the memory. In applications where this line is used by slaves to synchronize the bus to a slower clock, the master must have an open drain output, and a pull-up resistor must be connected from the SCL line to V_{CC}. (Figure 3 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the master has a push-pull (rather than open drain) output.

Serial Data (SDA)

The SDA pin is bi-directional, and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from the SDA bus to V_{CC}. (Figure 3 indicates how the value of the pull-up resistor can be calculated).

Chip Enable (E2, E1, E0)

These chip enable inputs are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code (but note that the V_{IL} and V_{IH} levels for the inputs are CMOS compatible, not TTL compatible). When unconnected, the E2, E1 and E0 inputs are internally read as V_{IL} (see Table 7 and Table 8)

Write Control ($\overline{WC}$)

The hardware Write Control pin ($\overline{WC}$) is useful for protecting the entire contents of the memory from inadvertent erase/write. The Write Control signal is used to enable ($\overline{WC}$=V_{IL}) or disable ($\overline{WC}$=V_{IH}) write instructions to the entire memory area. When unconnected, the $\overline{WC}$ input is internally read as V_{IL}, and write operations are allowed.

When $\overline{WC}$=1, Device Select and Address bytes are acknowledged, Data bytes are not acknowledged.

Please see the Application Note *AN404* for a more detailed description of the Write Control feature.

DEVICE OPERATION

The memory device supports the I^2C protocol. This is summarized in Figure 4, and is compared with other serial bus protocols in Application Note

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus

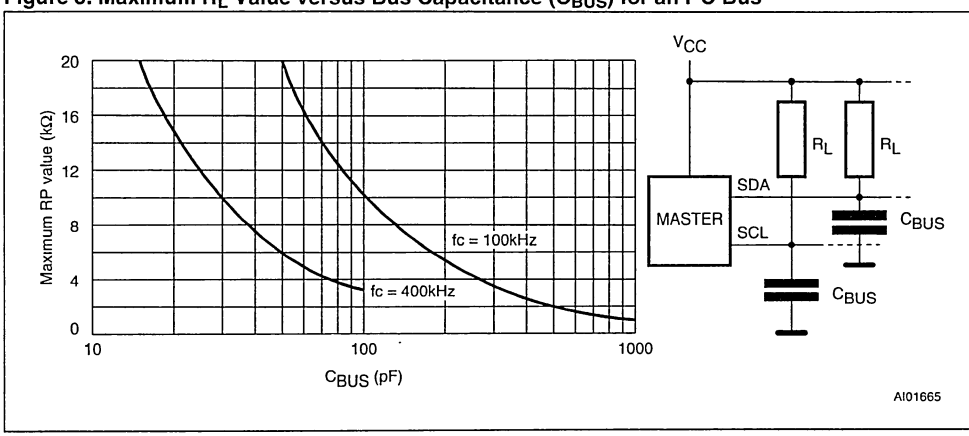
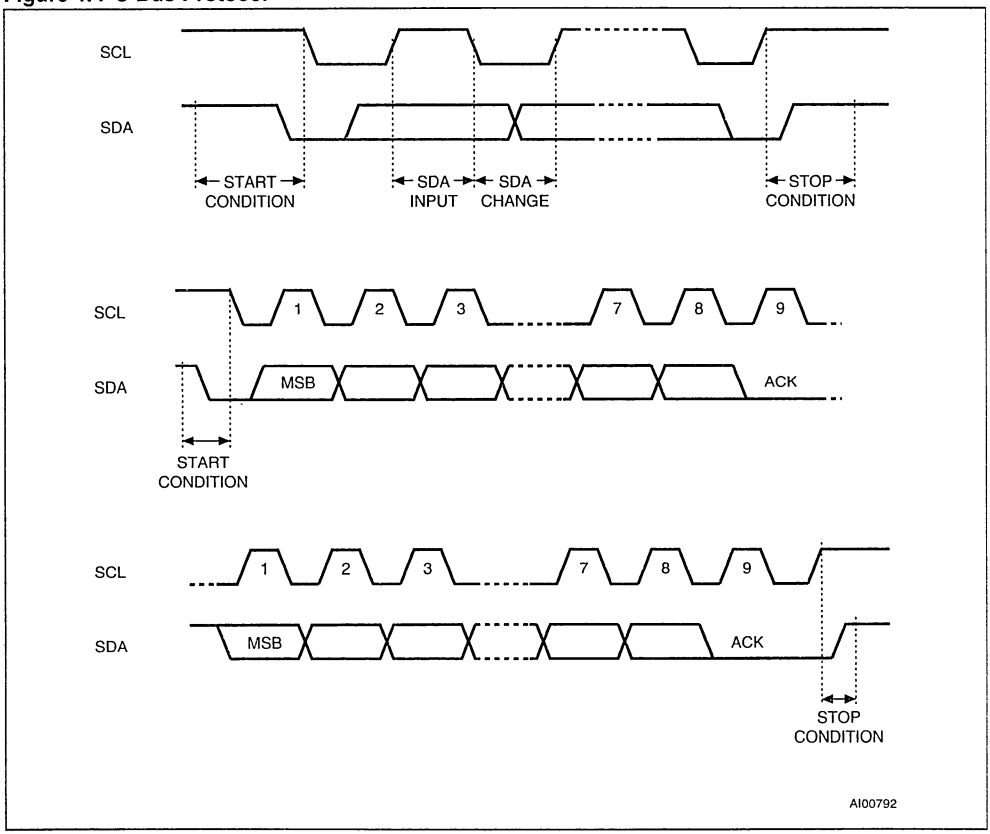


Figure 4. I²C Bus Protocol



AN1001. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the master, and the other as the slave. A data transfer can only be initiated by the master, which will also provide the serial clock for synchronization. The memory device is always a slave device in all communication.

Start Condition

START is identified by a high to low transition of the SDA line while the clock, SCL, is stable in the high state. A START condition must precede any data transfer command. The memory device continuously monitors (except during a programming cycle) the SDA and SCL lines for a START condition, and will not respond unless one is given.

Stop Condition

STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the memory device and the bus master. A STOP condition at the end of a Read command, after (and only after) a NoAck, forces the memory device into its standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK)

An acknowledge signal is used to indicate a successful byte transfer. The bus transmitter, whether it be master or slave, releases the SDA bus after sending eight bits of data. During the 9th clock pulse period, the receiver pulls the SDA bus low to acknowledge the receipt of the eight data bits.

Table 3. Device Select Code [1]

	Device Type Identifier				Chip Enable			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select Code	1	0	1	0	E2	E1	E0	RW

Note: 1. The most significant bit, b7, is sent first.

Data Input

During data input, the memory device samples the SDA bus signal on the rising edge of the clock, SCL. For correct device operation, the SDA signal must be stable during the clock low-to-high transition, and the data must change *only* when the SCL line is low.

Memory Addressing

To start communication between the bus master and the slave memory, the master must initiate a START condition. Following this, the master sends the 8-bit byte, shown in Table 3, on the SDA bus line (most significant bit first). This consists of the 7-bit Device Select Code, and the 1-bit Read/Write Designator (RW). The Device Select Code is further subdivided into: a 4-bit Device Type Identifier, and a 3-bit Chip Enable "Address" (E2, E1, E0).

To address the memory array, the 4-bit Device Type Identifier is 1010b.

If all three chip enable inputs are connected, up to eight memory devices can be connected on a single I^2C bus. Each one is given a unique 3-bit code on its Chip Enable inputs. When the Device Select Code is received on the SDA bus, the memory only responds if the Chip Select Code is the same as the pattern applied to its Chip Enable pins.

The 8th bit is the RW bit. This is set to '1' for read and '0' for write operations. If a match occurs on the Device Select Code, the corresponding memory gives an acknowledgment on the SDA bus during the 9th bit time. If the memory does not match the Device Select Code, it deselects itself from the bus, and goes into stand-by mode.

Table 4. Most Significant Byte

b15	b14	b13	b12	b11	b10	b9	b8

Note. 1. b15 is treated as Don't Care on the M24256-B series. b15 and b14 are Don't Care on the M24128-B series.

Table 5. Least Significant Byte

b7	b6	b5	b4	b3	b2	b1	b0

There are two modes both for read and write. These are summarized in Table 6 and described later. A communication between the master and the slave is ended with a STOP condition.

Each data byte in the memory has a 16-bit (two byte wide) address. The Most Significant Byte (Table 4) is sent first, followed by the Least significant Byte (Table 5). Bits b15 to b0 form the address of the byte in memory. Bit b15 is treated as a Don't Care bit on the M24256-B memory. Bits b15 and b14 are treated as Don't Care bits on the M24128-B memory.

Write Operations

Following a START condition the master sends a Device Select Code with the RW bit set to '0', as shown in Table 6. The memory acknowledges this, and waits for two address bytes. The memory responds to each address byte with an acknowledge bit, and then waits for the data byte.

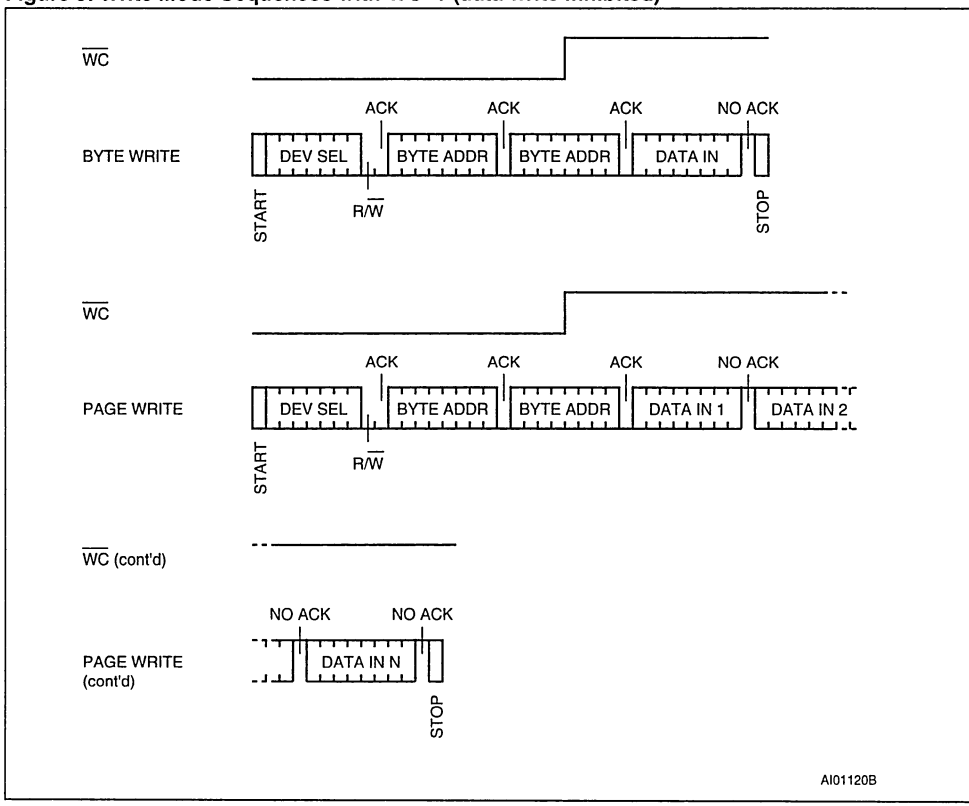
Writing to the memory may be inhibited if the WC input pin is taken high. Any write command with WC=1 (during a period of time from the START

Table 6. Operating Modes

Mode	RW bit	WC [1]	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, RW = '1'
Random Address Read	'0'	X	1	START, Device Select, RW = '0', Address
	'1'	X		reSTART, Device Select, RW = '1'
Sequential Read	'1'	X	≥ 1	Similar to Current or Random Address Read
Byte Write	'0'	V_{IL}	1	START, Device Select, RW = '0'
Page Write	'0'	V_{IL}	≤ 64	START, Device Select, RW = '0'

Note 1. X = V_{IH} or V_{IL}.

Figure 5. Write Mode Sequences with $\overline{WC}$=1 (data write inhibited)



condition until the end of the two address bytes) will not modify the memory contents, and the accompanying data bytes will *not* be acknowledged, as shown in Figure 5.

Byte Write

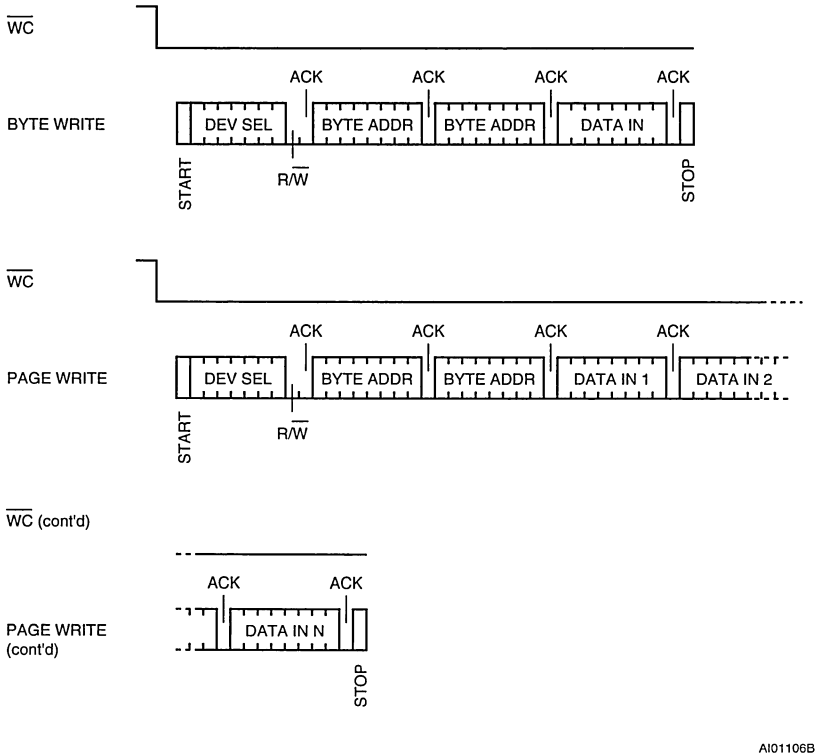
In the Byte Write mode, after the Device Select Code and the address bytes, the master sends one data byte. If the addressed location is write protected by the $\overline{WC}$ pin, the memory replies with a NoAck, and the location is not modified. If, instead, the $\overline{WC}$ pin has been held at 0, as shown in Figure 6, the memory replies with an Ack. The master terminates the transfer by generating a STOP condition.

Page Write

The Page Write mode allows up to 64 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the most significant memory address bits (b14-b6 for the M24256-B and b13-b6 for the M24128-B) are the same. If more bytes are sent than will fit up to the end of the row, a condition known as 'roll-over' occurs. Data starts to become overwritten (in a way not formally specified in this data sheet).

The master sends from one up to 64 bytes of data, each of which is acknowledged by the memory if the $\overline{WC}$ pin is low. If the $\overline{WC}$ pin is high, the con-

Figure 6. Write Mode Sequences with $\overline{WC}$=0 (data write enabled)

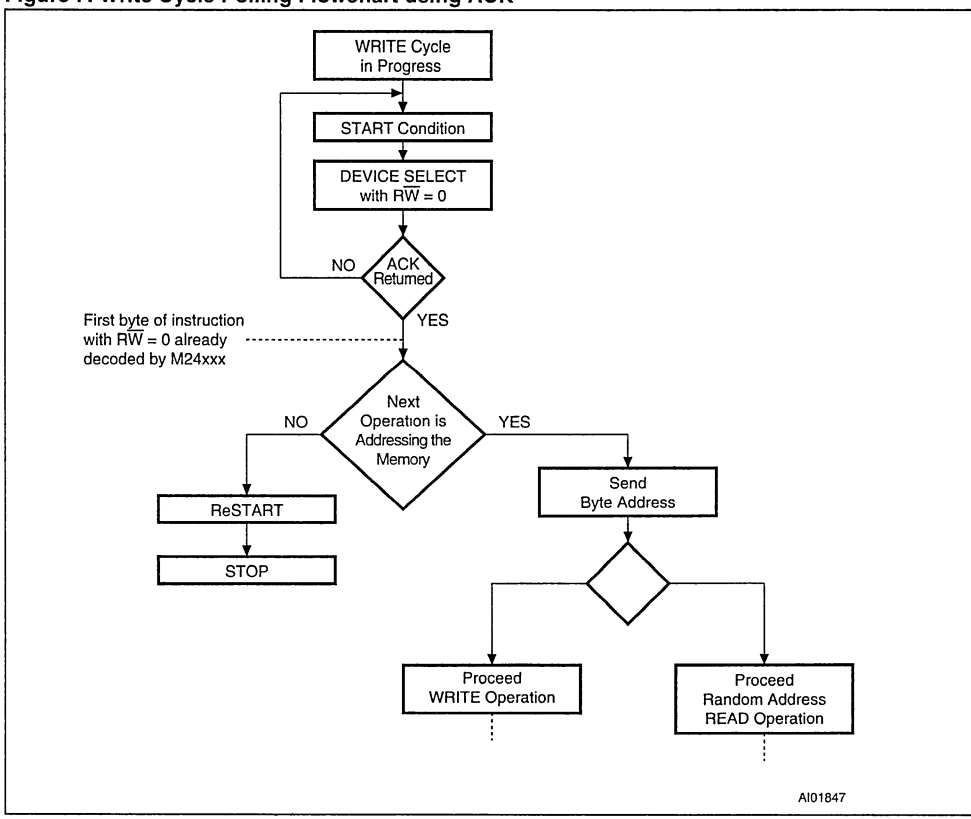


tents of the addressed memory location are not modified, and each data byte is followed by a NoAck. After each byte is transferred, the internal byte address counter (the 6 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition.

When the master generates a STOP condition immediately after the Ack bit (in the "10^{th} bit" time slot), either at the end of a byte write or a page write, the internal memory write cycle is triggered. A STOP condition at any other time does not trigger the internal write cycle.

During the internal write cycle, the SDA input is disabled internally, and the device does not respond to any requests.

Figure 7. Write Cycle Polling Flowchart using ACK



Minimizing System Delays by Polling On ACK

During the internal write cycle, the memory disconnects itself from the bus, and copies the data from its internal latches to the memory cells. The maximum write time (t_W) is shown in Table 9, but the typical time is shorter. To make use of this, an Ack polling sequence can be used by the master.

The sequence, as shown in Figure 7, is:

- Initial condition: a Write is in progress.
- Step 1: the master issues a START condition followed by a Device Select Code (the first byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no Ack will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it responds with an Ack, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction having been sent during Step 1).

Read Operations

Read operations are performed independently of the state of the $\overline{WC}$ pin.

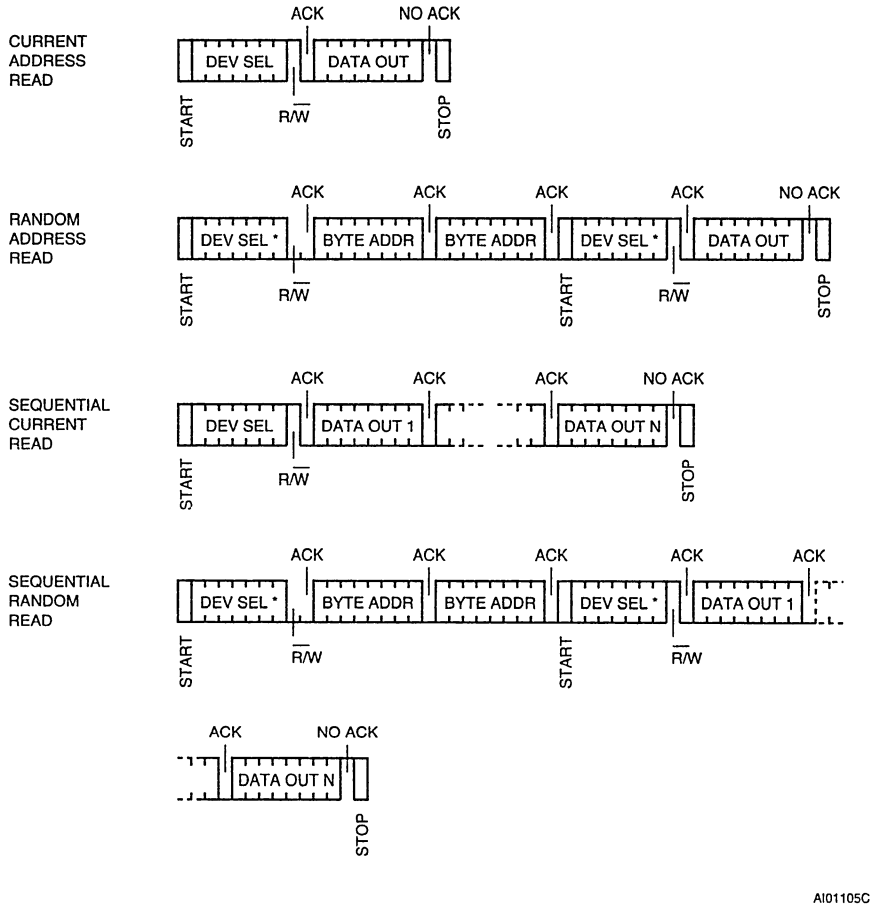
Random Address Read

A dummy write is performed to load the address into the address counter, as shown in Figure 8. Then, *without* sending a STOP condition, the master sends another START condition, and repeats the Device Select Code, with the $\overline{RW}$ bit set to '1'. The memory acknowledges this, and outputs the contents of the addressed byte. The master must *not* acknowledge the byte output, and terminates the transfer with a STOP condition.

Current Address Read

The device has an internal address counter which is incremented each time a byte is read. For the Current Address Read mode, following a START condition, the master sends a Device Select Code with the $\overline{RW}$ bit set to '1'. The memory acknowledges this, and outputs the byte addressed by the

Figure 8. Read Mode Sequences



Note: 1. The seven most significant bits of the Device Select Code of a Random Read (in the 1st and 4th bytes) must be identical.

internal address counter. The counter is then incremented. The master terminates the transfer with a STOP condition, as shown in Figure 8, *without* acknowledging the byte output.

Sequential Read

This mode can be initiated with either a Current Address Read or a Random Address Read. The master *does* acknowledge the data byte output in this case, and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must *not* acknowledge the last byte output, and *must* generate a STOP condition.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over' and the memory continues to output data from the start of the memory block.

Acknowledge in Read Mode

In all read modes, the memory waits, after each byte read, for an acknowledgment during the 9th bit time. If the master does not pull the SDA line low during this time, the memory terminates the data transfer and switches to its standby state.

Table 7. DC Characteristics
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 4.5 to 5.5 V or 2.5 to 5.5 V)
(T_A = 0 to 70 °C or -20 to 85 °C; V_{CC} = 1.8 to 3.6 V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$0 V \le V_{IN} \le V_{CC}$		± 2	µA
I_{LI}	Input Leakage Current (E2, E1, E0, $\overline{WC}$)	Device is selected	$\frac{V_{CC}}{Z(max)}$	$\frac{V_{CC}}{Z(min)}$	µA
		Device is not selected		± 2	µA
I_{LO}	Output Leakage Current	$0 V \le V_{OUT} \le V_{CC}$, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current -W series:	V_{CC}=5V, f_c=400kHz (rise/fall time < 30ns)		2	mA
		V_{CC} =2.5V, f_c=400kHz (rise/fall time < 30ns)		1	mA
	-R series:	V_{CC} =1.8V, f_c=100kHz (rise/fall time < 30ns)		0.8[1]	mA
I_{CC1}	Supply Current (Stand-by)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5 V		10	µA
I_{CC2}	Supply Current (Stand-by)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5 V		2	µA
I_{CC3}	Supply Current (Stand-by)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8 V		1[1]	µA
V_{IL}	Input Low Voltage (E0-E2, SCL, SDA)		- 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (E0-E2, SCL, SDA)		0.7V_{CC}	V_{CC}+1	V
V_{IL}	Input Low Voltage ($\overline{WC}$)		- 0.3	0.5	V
V_{IH}	Input High Voltage ($\overline{WC}$)		V_{CC} - 0.5	V_{CC}+1	V
V_{OL}	Output Low Voltage -W series:	I_{OL} = 3 mA, V_{CC} = 5 V		0.4	V
		I_{OL} = 2.1 mA, V_{CC} = 2.5 V		0.4	V
	-R series:	I_{OL} = 0.15 mA, V_{CC} = 1.8 V		0.2[1]	V

Note: 1. This is preliminary data.
2. See Table 8

Table 8. Input Parameters[1] (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z	Pull-Down Impedance of E2, E1, E0, $\overline{WC}$ inputs	Device is selected	25[2]	100[3]	kΩ
		Device is not selected	4		kΩ
t_{NS}	Low Pass Filter Input Time Constant (SCL and SDA)			100	ns

Note: 1 Sampled only, not 100% tested.
2. This is Z(min) as used in Table 7
3 This is Z(max) as used in Table 7

Table 9. AC Characteristics
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 4.5 to 5.5 V or 2.5 to 5.5 V)
(T_A = 0 to 70 °C or -20 to 85 °C; V_{CC} = 1.8 to 3.6 V)

Symbol	Alt.	Parameter	M24256-B / M24128-B						Unit
			V_{CC}=4.5 to 5.5 V T_A=0 to 70°C or -40 to 85°C		V_{CC}=2.5 to 5.5 V T_A=0 to 70°C or -40 to 85°C		V_{CC}=1.8 to 3.6 V T_A=0 to 70°C or -20 to 85°C[4]		
			Min	Max	Min	Max	Min	Max	
t_{CH1CH2}	t_R	Clock Rise Time		300		300		1000	ns
t_{CL1CL2}	t_F	Clock Fall Time		300		300		300	ns
t_{DH1DH2}[2]	t_R	SDA Rise Time	20	300	20	300	20	1000	ns
t_{DL1DL2}[2]	t_F	SDA Fall Time	20	300	20	300	20	300	ns
t_{CHDX}[1]	$t_{SU\ STA}$	Clock High to Input Transition	600		600		4700		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		600		4000		ns
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	600		600		4000		ns
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		0		0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		1.3		4.7		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	100		100		250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	600		600		4000		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		1.3		4.7		µs
t_{CLQV}[3]	t_{AA}	Clock Low to Data Out Valid	200	900	200	900	200	3500	ns
t_{CLQX}	t_{DH}	Data Out Hold Time After Clock Low	200		200		200		ns
f_C	f_{SCL}	Clock Frequency		400		400		100	kHz
t_W	t_{WR}	Write Time		10		10		10	ms

Note. 1. For a reSTART condition, or following a write cycle
2. Sampled only, not 100% tested.
3. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
4. This is preliminary data.

Table 10. AC Measurement Conditions

Input Rise and Fall Times	≤ 50 ns
Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}
Input and Output Timing Reference Voltages	0.3V_{CC} to 0.7V_{CC}

Figure 9. AC Testing Input Output Waveforms

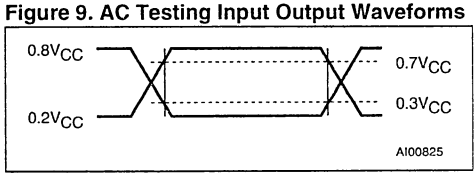


Figure 10. AC Waveforms

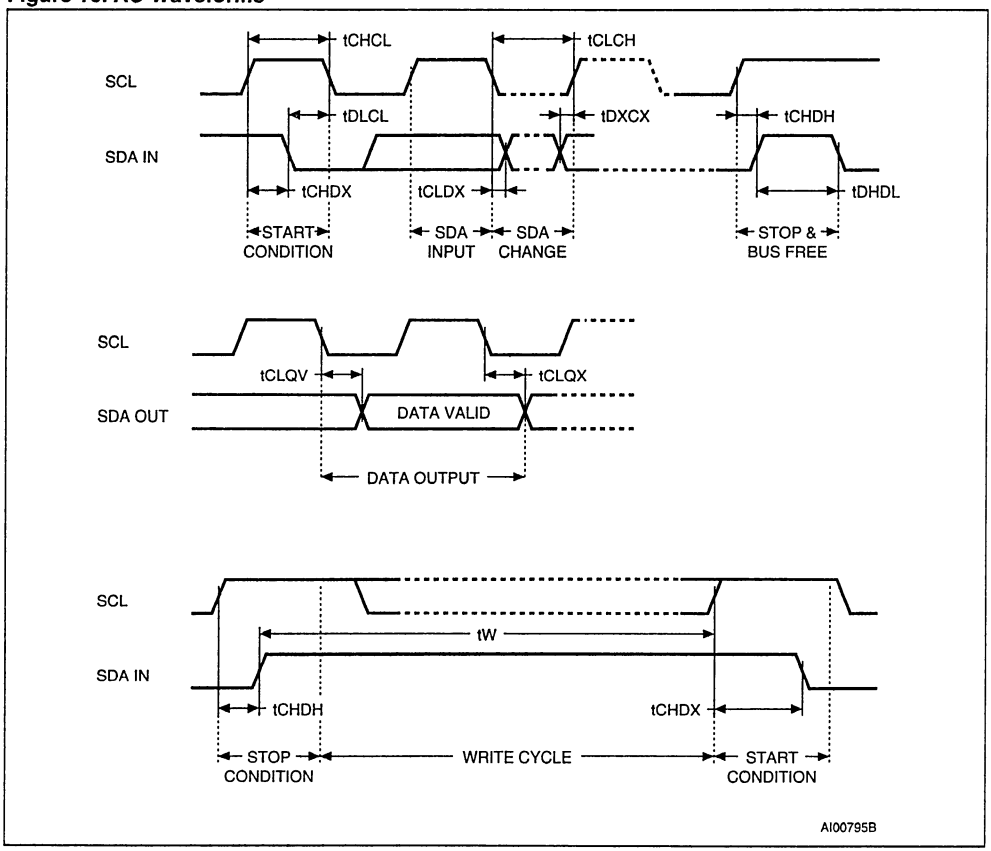


Table 11. Ordering Information Scheme

Example: M24256 – B R MN 6 T

Memory Capacity

256 256 Kbit (32K x 8)

128 128 Kbit (16K x 8)

Operating Voltage

blank 4.5 V to 5.5 V

W 2.5 V to 5.5 V

R 1.8 V to 3.6 V

Package

BN PSDIP8 (0.25 mm frame)

MN SO8 (150 mil width)

DL TSSOP14 (169 mil width)

Option

T Tape and Reel Packing

Temperature Range

1[1] 0 °C to 70 °C

6 –40 °C to 85 °C

Note: 1. Temperature range available only on request.

ORDERING INFORMATION

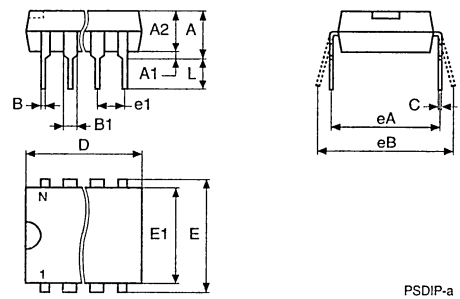
Devices are shipped from the factory with the memory content set at all '1's (FFh).

The notation used for the device number is as shown in Table 11. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 12. PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

Figure 11. PSDIP8 (BN)

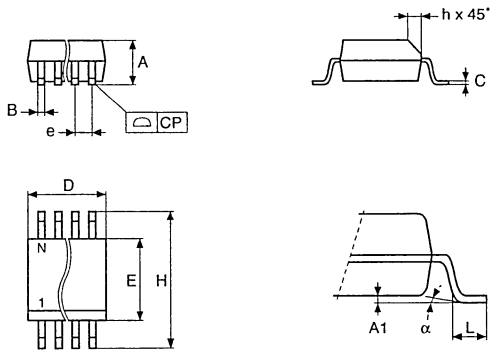


Note: 1. Drawing is not to scale.

Table 13. SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

Figure 12. SO8 narrow (MN)



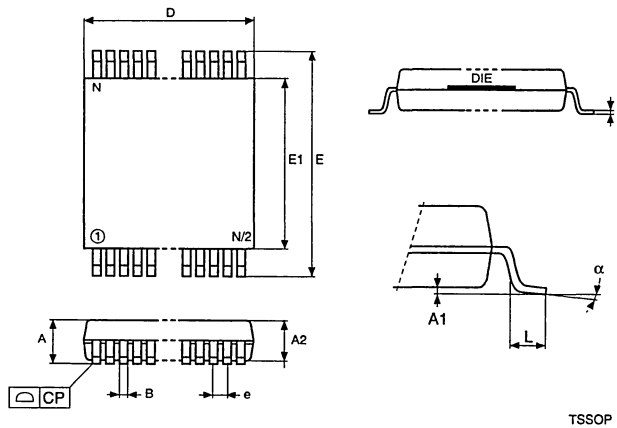
SO-a

Note: 1 Drawing is not to scale.

Table 14. TSSOP14 - 14 lead Thin Shrink Small Outline

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.10			0.043
A1		0.05	0.15		0.002	0.006
A2		0.85	0.95		0.033	0.037
B		0.19	0.30		0.007	0.012
C		0.09	0.20		0.004	0.008
D		4.90	5.10		0.193	0.197
E		6.25	6.50		0.246	0.256
E1		4.30	4.50		0.169	0.177
e	0.65	–	–	0.026	–	–
L		0.50	0.70		0.020	0.028
α		0°	8°		0°	8°
N		14			14	
CP			0.08			0.003

Figure 13. TSSOP14 (DL)



Note: 1. Drawing is not to scale.

M24256
M24128

256 Kbit/128 Kbit Serial I^2C Bus EEPROM without Chip Enable Lines

PRELIMINARY DATA

- COMPATIBLE with I^2C EXTENDED ADDRESSING
- TWO WIRE I^2C SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- 100,000 ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  - 4.5V to 5.5V for M24256 and M24128
  - 2.5V to 5.5V for M24256-W and M24128-W
  - 1.8V to 3.6V for M24256-R and M24128-R
- HARDWARE WRITE CONTROL
- BYTE and PAGE WRITE (up to 64 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH-UP PERFORMANCES

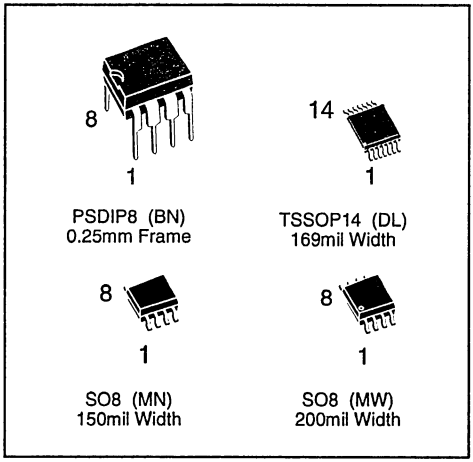
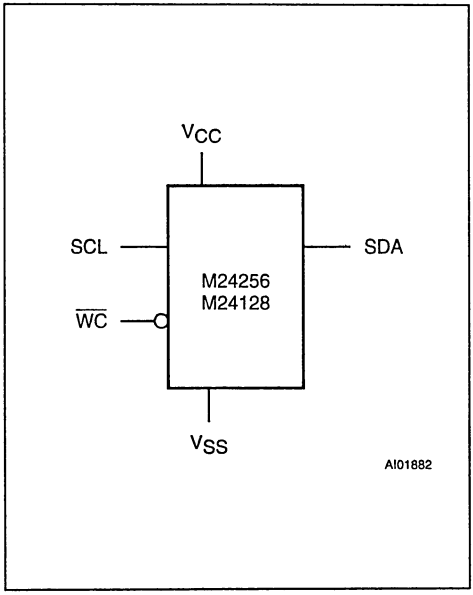


Figure 1. Logic Diagram



DESCRIPTION

The M24256 and the M24128 are a 256 Kbit and a 128 Kbit electrically erasable programmable memories (EEPROM), organized as 32,768 x8 and as 16,384 x8 bits respectively. The "-W" versions operate with a power supply value as low as 2.5V and the "-R" versions operate down to 1.8V. Plastic Dual-in-Line, Plastic Small Outline and Thin Shrink Small Outline packages are available.

Table 1. Signal Names

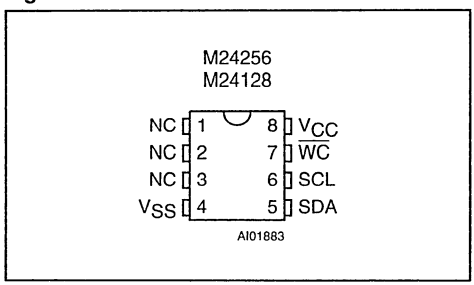
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature (2)			–40 to 125	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8) (PSDIP8)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.6 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (3)			4000	V
	Electrostatic Discharge Voltage (Machine model) (4)			200	V

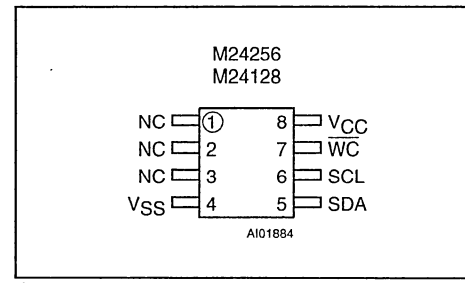
Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents
2 Depends on range.
3 100pF through 1500Ω; MIL-STD-883C, 3015 7
4. 200pF through 0Ω; EIAJ IC-121 (condition C)

Figure 2A. DIP Pin Connections



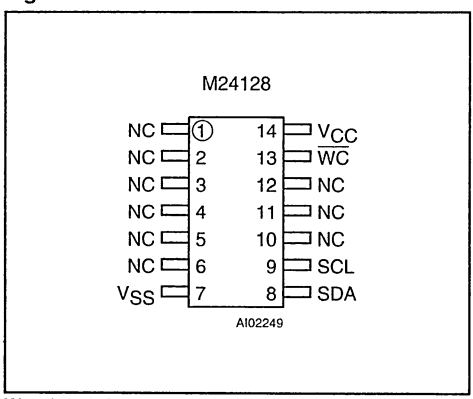
Warning: NC = Not Connected

Figure 2B. SO Pin Connections



Warning: NC = Not Connected

Figure 2C. TSSOP Pin Connections



Warning: NC = Not Connected

DESCRIPTION (cont'd)

Each memory is compatible with the I^2C extended memory standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memory carries a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The memory behaves as a slave device in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), then 3 bits (at 000) to form a 7 bit Device Select, plus one read/write bit ($R\overline{W}$) and terminated by an acknowledge bit.

Table 3. Device Select Code

	Device Code				Chip Enable			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	0	0	0	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	RW bit	WC	Data Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, RW = '1'
Random Address Read	'0'	X	1	START, Device Select, RW = '0', Address,
	'1'	X		reSTART, Device Select, RW = '1'
Sequential Read	'1'	X	≥ 1	As CURRENT or RANDOM Mode
Byte Write	'0'	V_{IL}	1	START, Device Select, RW = '0'
Page Write	'0'	V_{IL}	≤ 64	START, Device Select, RW = '0'

Note: 1. X = V_{IH} or V_{IL}.

When writing data to the memory, it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Write Control (WC). The Write Control feature WC is useful to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable (WC=V_{IH}) or disable (WC=V_{IL}) the internal write protection. When the WC pin is unconnected, the WC input is internally read as V_{IL} (see Table 5).

When WC=1, Device Select and Address bytes are acknowledged, Data bytes are not acknowledged.

Refer to Application Note AN404 for more detailed information about Write Control feature.

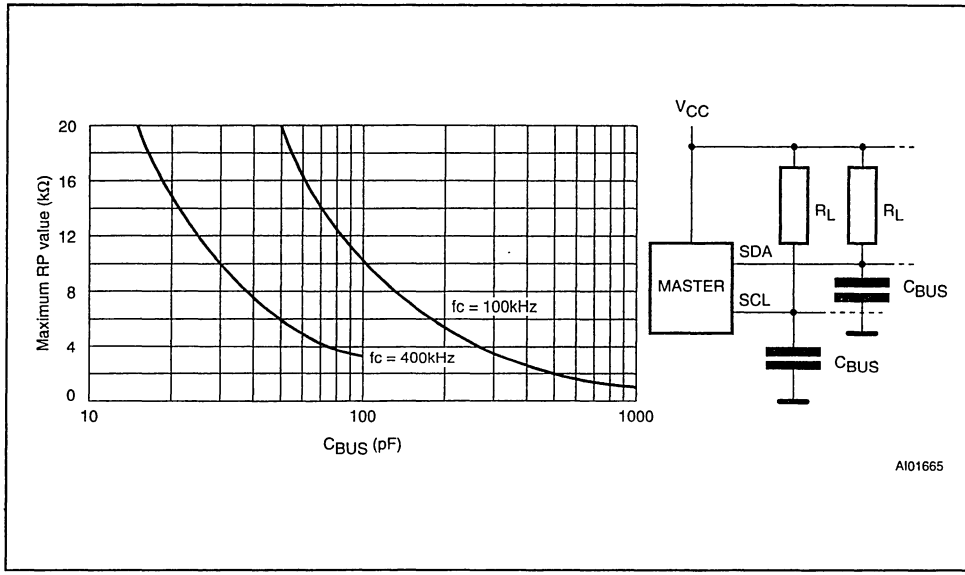
DEVICE OPERATION

I^2C Bus Background

The memory supports the extended addressing I^2C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The memory is always a slave device in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the memory continuously monitors the SDA and SCL signals for a START condition and will not respond unless one is given.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus



Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the memory and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the memory samples the SDA bus signal on the rising edge of the clock SCL. For correct device operation, the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Device Selection. To start communication between the bus master and the slave memory, the master must initiate a START condition. The 8 bits sent after a START condition are made up of a device select of 4 bits that identifies the device type, then 3 bits (at 000) and one bit for a READ ($R\overline{W}$=1) or WRITE ($R\overline{W}$=0) operation. There are two modes both for read and write. These are summarized in Table 4 and described hereafter. A communication between the master and the slave is ended with a STOP condition.

Memory Addressing. A data byte in the memory is addressed through 2 bytes of address information. The Most Significant Byte is sent first and the Least significant Byte is sent after. Bits b15 to b0 form the address of any byte of the memory. Bit b15 is don't care on the M24256 series. Bits b15 and b14 are don't care on the M24128 series.

Most Significant Byte

b15	b14	b13	b12	b11	b10	b9	b8

b15 is don't care on M24256 series.
b15 and b14 are don't care on M24128 series.

Least Significant Byte

b7	b6	b5	b4	b3	b2	b1	b0

Table 5. Input Parameters (1) (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} \le 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} \ge 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested

Table 6. DC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)
(T_A = 0 to 70 °C or –20 to 85 °C; V_{CC} = 1.8V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_C = 400kHz (Rise/Fall time < 30ns)		2	mA
	Supply Current (-W series)	V_{CC} = 2.5V, f_C = 400kHz (Rise/Fall time < 30ns)		1	mA
	Supply Current (-R series)	V_{CC} = 1.8V, f_C = 100kHz (Rise/Fall time < 30ns)		0.5	mA
I_{CC1}	Supply Current, Standby	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		10	µA
	Supply Current, Standby (-W series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		2	µA
	Supply Current, Standby (-R series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8V		1	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage ($\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage ($\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (-W series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V
	Output Low Voltage (-R series)	I_{OL} = 0.15mA, V_{CC} = 1.8V		0.2	V

Table 7. AC Characteristics

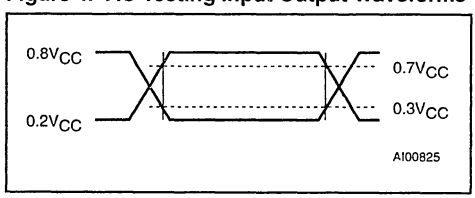
Symbol	Alt	Parameter	M24256 / M24128						Unit
			V_{CC} = 4.5V to 5.5V T_A = 0 to 70°C T_A = –40 to 85°C		V_{CC} = 2.5V to 5.5V T_A = 0 to 70°C T_A = –40 to 85°C		V_{CC} = 1.8V to 3.6V T_A = 0 to 70°C T_A = –20 to 85°C		
			Min	Max	Min	Max	Min	Max	
t_{CH1CH2}	t_R	Clock Rise Time		300		300		1000	ns
t_{CL1CL2}	t_F	Clock Fall Time		300		300		300	ns
t_{DH1DH2} (1)	t_R	SDA Rise Time	20	300	20	300	20	1000	ns
t_{DL1DL2} (1)	t_F	SDA Fall Time	20	300	20	300	20	300	ns
t_{CHDX} (2)	$t_{SU.STA}$	Clock High to Input Transition	600		600		4700		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		600		4000		ns
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	600		600		4000		ns
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		0		0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1300		1300		4700		ns
t_{DXCX}	$t_{SU.DAT}$	Input Transition to Clock Transition	100		100		250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	600		600		4000		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1300		1300		4700		ns
t_{CLQV} (3)	t_{AA}	Clock Low to Next Data Out Valid	200	900	200	900	200	3500	ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		200		200		ns
f_C	f_{SCL}	Clock Frequency		400		400		100	kHz
t_W	t_{WR}	Write Time		10		10		10	ms

Notes: 1. Sampled only, not 100% tested.
2. For a reSTART condition, or following a write cycle.
3 The minimum value delays the falling/rising edge of SDA away form SCL = 1 in order to avoid unwanted START and/or STOP condition.

Table 8. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}
Input and Output Timing Ref. Voltages	0.3V_{CC} to 0.7V_{CC}

Figure 4. AC Testing Input Output Waveforms



Write Operations

Following a START condition the master sends a Device Select code with the R$\overline{W}$ bit set to '0'. The memory acknowledges this and waits for 2 bytes of address. These 2 address bytes (8 bits each) provide access to any of the memory locations. Writing in the memory may be inhibited if input pin $\overline{WC}$ is taken high.

Any write command with $\overline{WC}$=1 (during a period of time from the START condition until the end of the 2 bytes address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 9.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition.

Figure 5. AC Waveforms

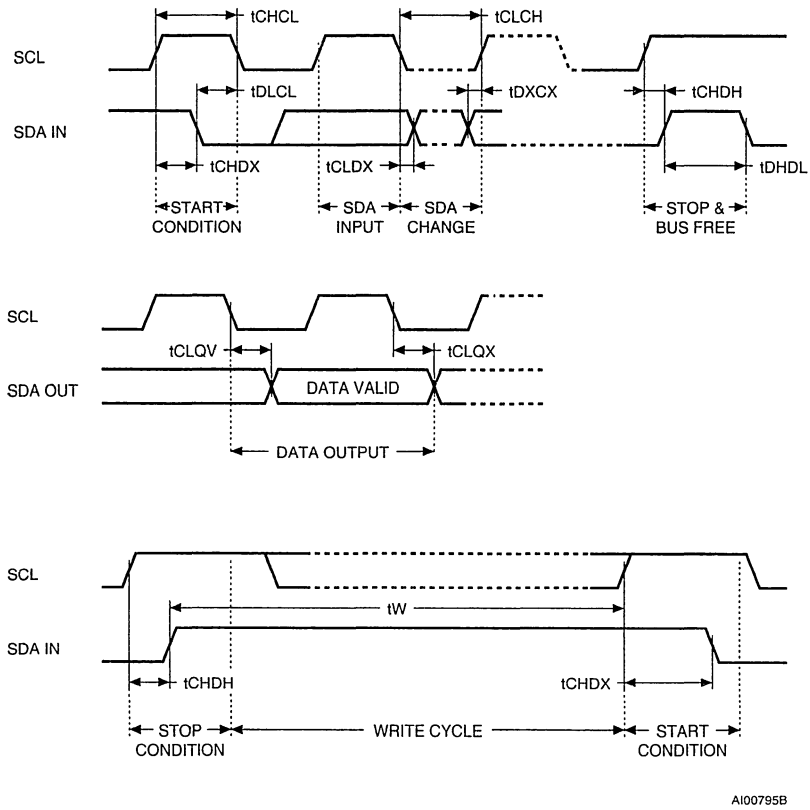
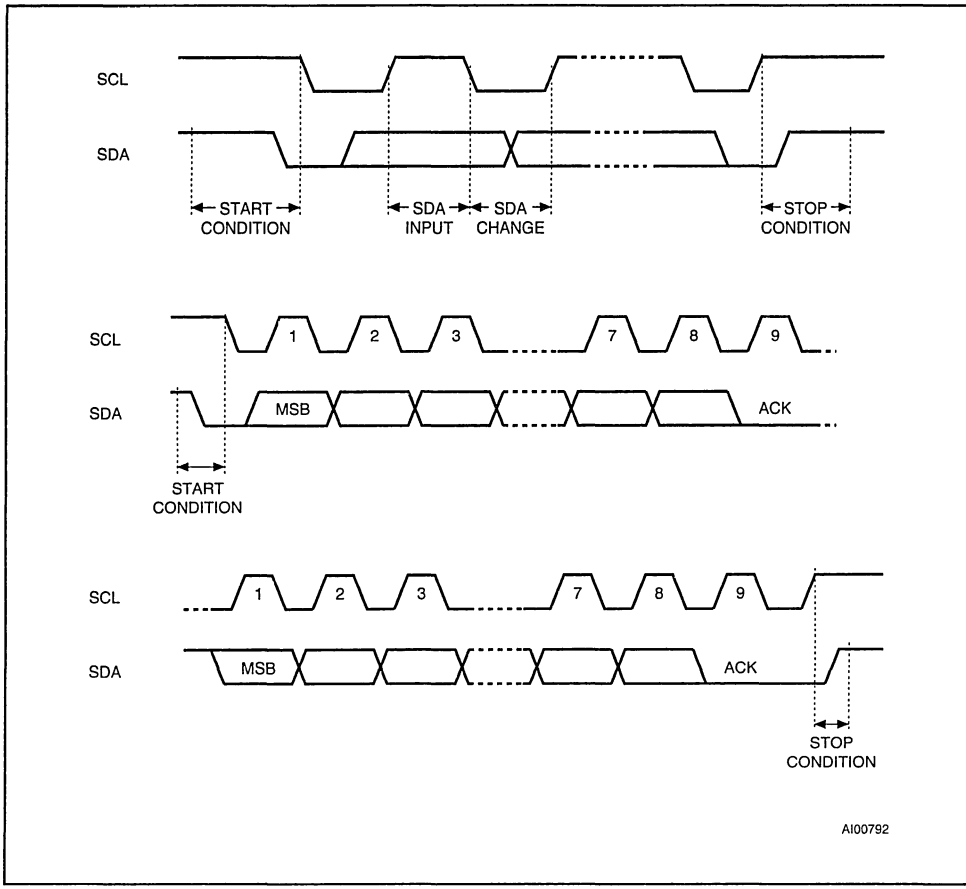


Figure 6. I²C Bus Protocol



Page Write. The Page Write mode allows up to 64 bytes to be written in a single write cycle, provided that they are all located in the same row of 64 bytes in the memory, that is the same address bits (b14-b6 for the M24256 and b13-b6 for the M24128).

The master sends from one up to 64 bytes of data, which are each acknowledged by the memory. After each byte is transferred, the internal byte address counter (6 Least Significant Bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. This STOP condition will trigger an internal memory program cycle only if the STOP condition is internally decoded right after the AC Kbit; any STOP condition decoded out of this "10th bit" time slot will not trigger the internal programming cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal Write cycle, the memory disable itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the Write time (t_W) is given in the Table 8, this timing value may be reduced by an ACK polling sequence issued by the master.

The sequence is:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
- Step 2: if the memory is internally writing, NoACK will be returned. The master goes back to Step 1. If the memory has terminated the internal writing, it will issue an ACK.
  The memory is ready to receive the second part of the instruction (the first byte of this instruction was already sent during Step 1).

Read Operations

On delivery, the memory contents is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a Device Select with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Figure 7. Write Cycle Polling using ACK

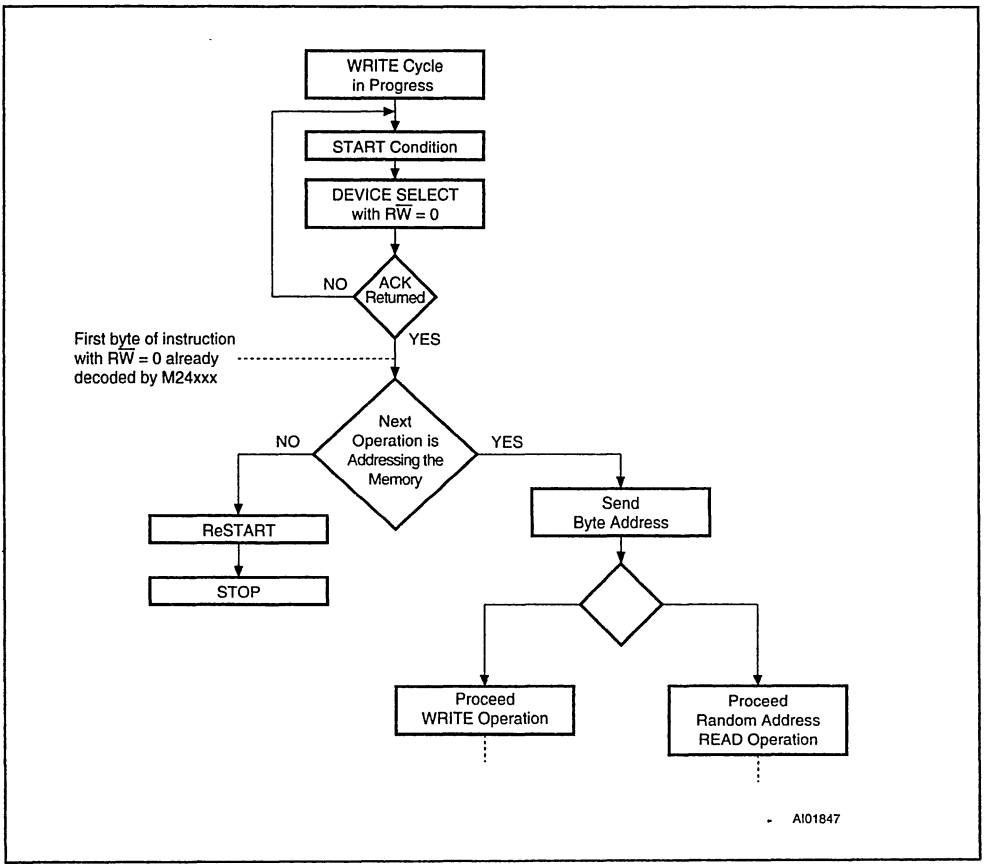
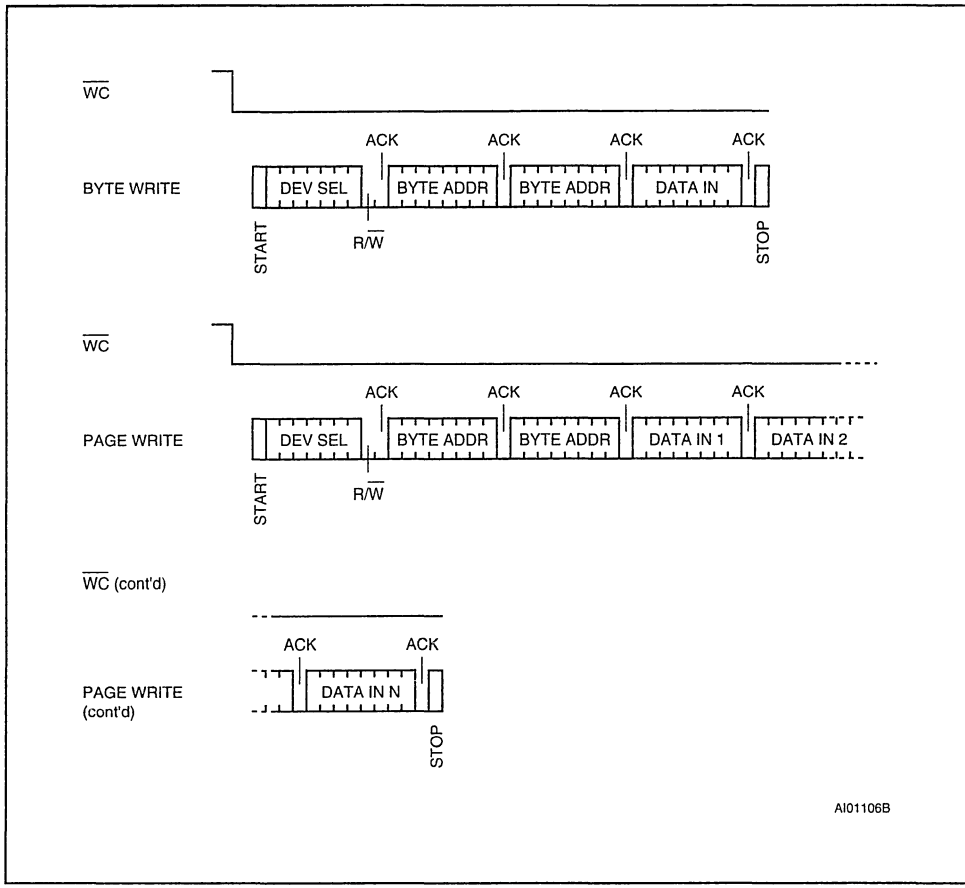


Figure 8. Write Modes Sequence with Write Control = 0



Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address repeated with the R/W bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master have to NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the memory waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the memory terminates the data transfer and switches to a standby state.

Figure 9. Write Modes Sequence with Write Control = 1

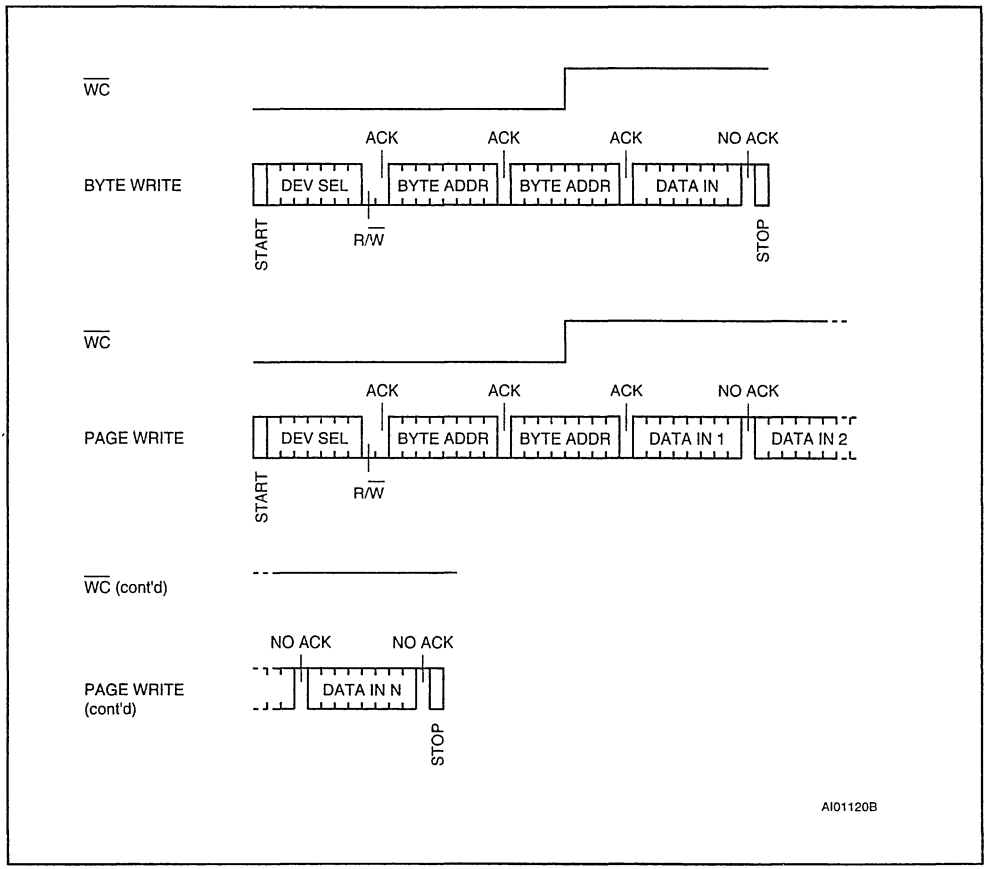
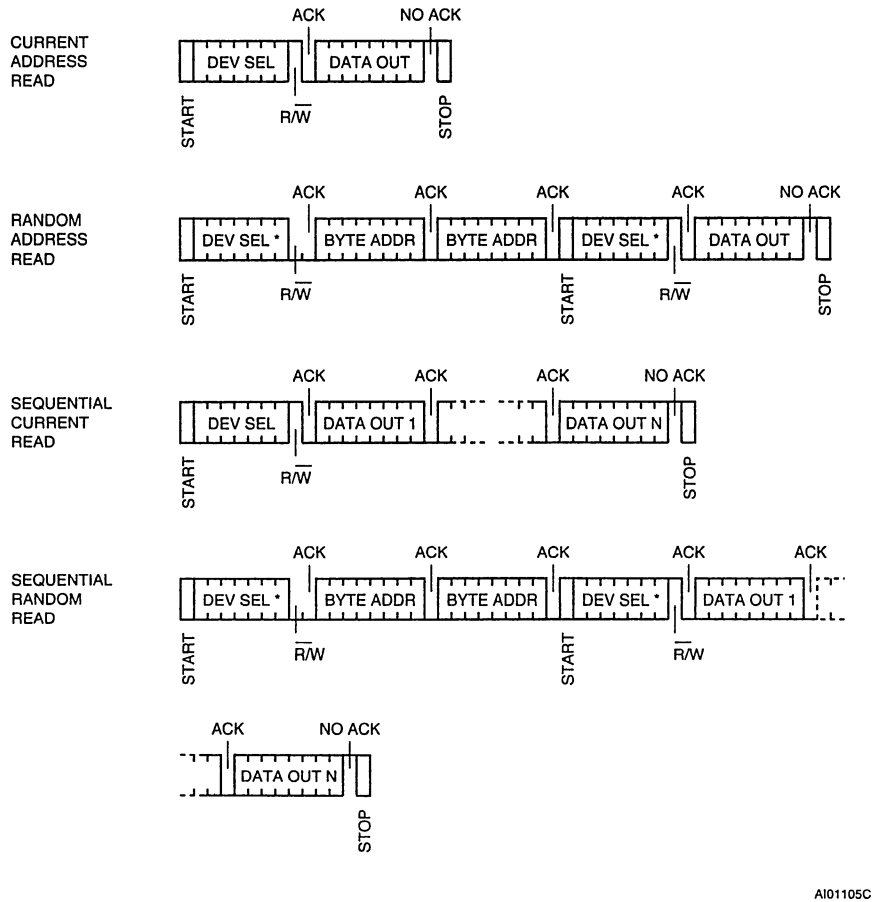
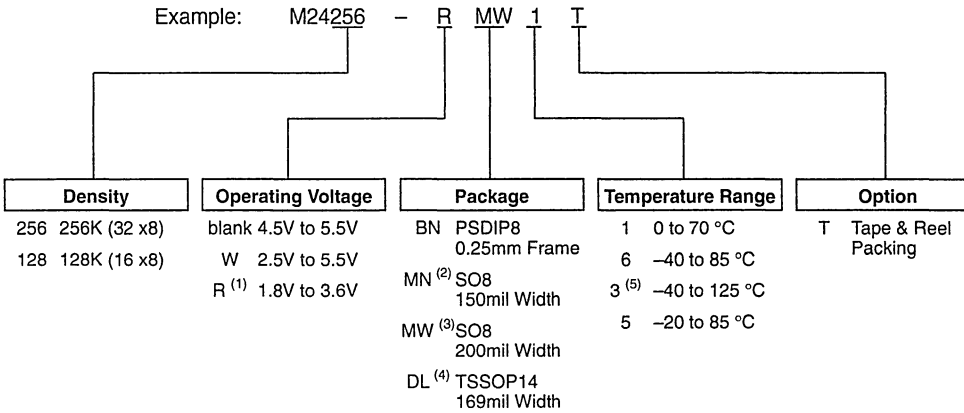


Figure 10. Read Mode Sequences



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 4th byte) must be identical.

ORDERING INFORMATION SCHEME



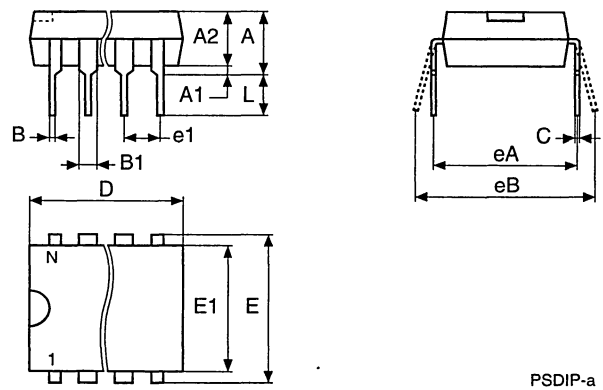
Notes: 1. -R version (1.8V to 3.6V) are only available in temperature ranges 5 or 1.
2. SO8, 150mil Width, package is available for M24128 series only.
3 SO8, 200mil Width, package is available for M24256 series only.
4. TSSOP14, 169mil Width, pakage is available for M24128 series only. Contact marketing for availability.
5. Produced with High Reliability Certified Flow (HRCF), in V_{CC} range 4.5V to 5 5V at 100kHz only.

Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

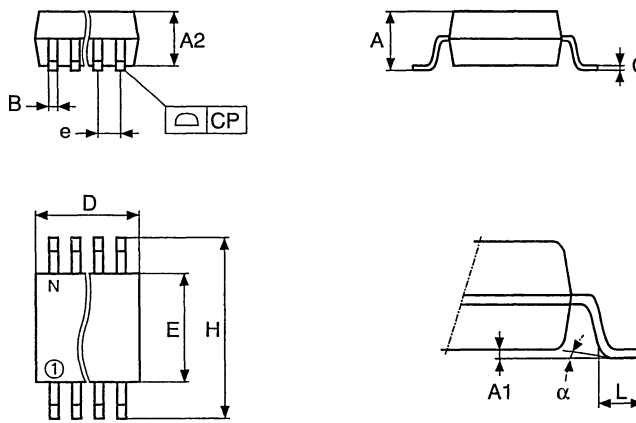


PSDIP-a

Drawing is not o scale.

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0	8		0	8
N	8			8		
CP			0.10			0.004

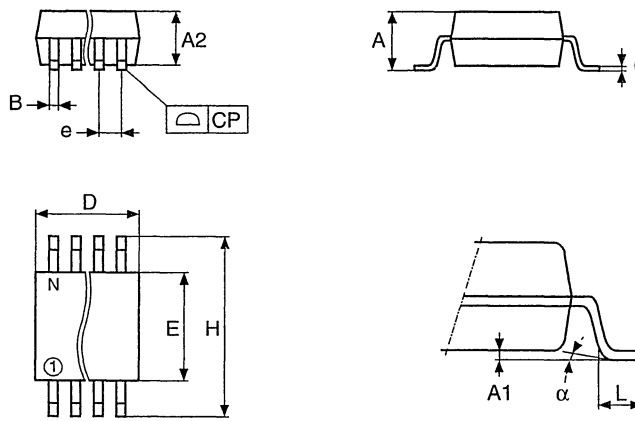


SO-b

Drawing is not to scale.

SO8 - 8 lead Plastic Small Outline, 200 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.03			0.080
A1		0.10	0.25		0.004	0.010
A2			1.78			0.070
B		0.35	0.45		0.014	0.018
C	0.20	–	–	0.008	–	–
D		5.15	5.35		0.203	0.211
E		5.20	5.40		0.205	0.213
e	1.27	–	–	0.050	–	–
H		7.70	8.10		0.303	0.319
L		0.50	0.80		0.020	0.031
α		0°	10°		0°	10°
N	8			8		
CP			0.10			0.004

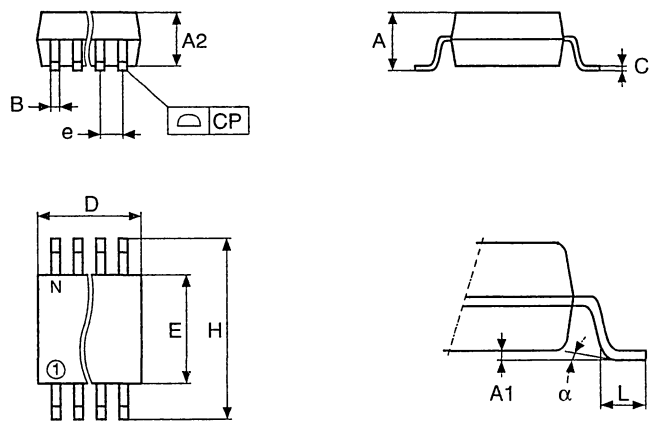


SO-b

Drawing is not to scale.

TSSOP14 - 14 lead Thin Shrink Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.10			0.043
A1		0.05	0.15		0.002	0.006
A2		0.85	0.95		0.033	0.037
B		0.19	0.30		0.007	0.012
C		0.09	0.20		0.004	0.008
D		4.90	5.10		0.193	0.197
E		6.25	6.50		0.246	0.256
E1		4.30	4.50		0.169	0.177
e	0.65	–	–	0.026	–	–
L		0.50	0.70		0.020	0.028
α		0°	8°		0°	8°
N	14			14		
CP			0.08			0.003



SO-b

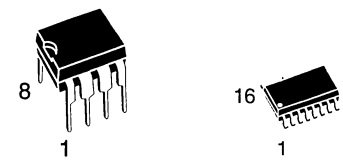
Drawing is not to scale.

M24512

512 Kbit (64Kb x8) Serial I^2C Bus EEPROM

PRODUCT PREVIEW

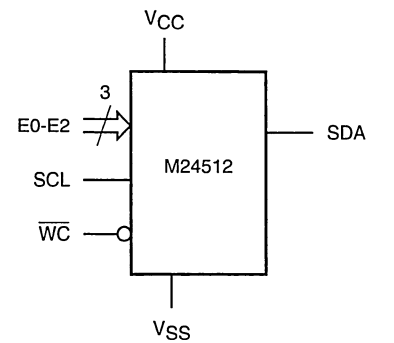
- Compatible with I^2C Extended Addressing
- Three Wire I^2C Serial Interface
  Supports 400KHz Protocol
- Single Supply Voltage:
  - 4.5V to 5.5V for M24512
  - 2.5V to 5.5V for M24512-W
  - 1.8V to 3.6V for M24512-R
- Hardware Write Control
- BYTE and PAGE WRITE (up to 128 BYTES)
- RANDOM and SEQUENTIAL READ MODES
- Self Timed Programing Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Performances
- 100,000 Erase/Write Cycles (minimum)
- 40 Year Data Retention (minimum)



PSDIP8 (BN)
0.25mm Frame

SO16 (MJ)
300mil Width

Figure 1. Logic Diagram



DESCRIPTION

The M24512 is a 512 Kbit electrically erasable programmable memory (EEPROM), organized as 65,536 x8 bits. The "-W" versions operate with a power supply value as low as 2.5V and the "-R" versions operate down to 1.8V. Plastic Dual-in-Line, Plastic Small Outline and Thin Shrink Small Outline packages are available.

Table 1. Signal Names

E0-E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

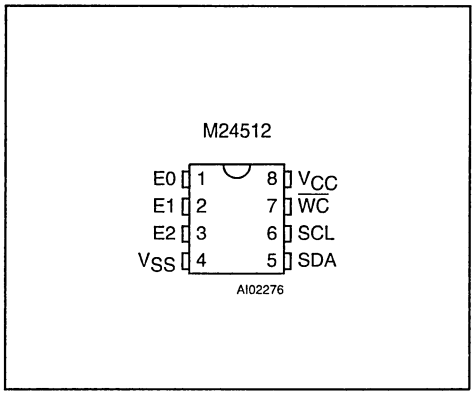
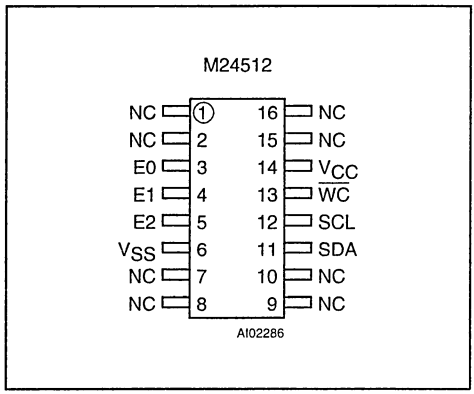


Figure 2B. SO Pin Connections



Warning: NC = Not Connected

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature (2)			–40 to 125	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO16) (PSDIP8)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.6 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (3)			4000	V
	Electrostatic Discharge Voltage (Machine model) (4)			200	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents
2. Depends on range.
3. 100pF through 1500Ω, MIL-STD-883C, 3015.7
4. 200pF through 0Ω; EIAJ IC-121 (condition C)

DESCRIPTION (cont'd)

Each memory is compatible with the I^2C extended memory standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memory carries a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The memory behaves as a slave device in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), then 3 Chip Enable Input bits (E2, E1, E0) to form a 7 bit Device Select, plus one read/write bit ($R\overline{W}$) and terminated by an acknowledge bit. Up to 8 memories may be connected to the same I2C bus and selected individually.

When writing data to the memory, it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Table 3. Device Select Code

	Device Code				Chip Enable			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	RW bit	WC	Data Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, RW = '1'
Random Address Read	'0'	X	1	START, Device Select, RW = '0', Address,
	'1'	X		reSTART, Device Select, RW = '1'
Sequential Read	'1'	X	≥ 1	As CURRENT or RANDOM Mode
Byte Write	'0'	V_{IL}	1	START, Device Select, RW = '0'
Page Write	'0'	V_{IL}	≤ 128	START, Device Select, RW = '0'

Note: 1. X = V_{IH} or V_{IL}.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Chip Enable (E0, E1, E2). These chip enable inputs are used to set the 3 least significant bits of the 7 bit device select code. They may be driven dynamically or tied to VCC or VSS to establish the device select code. When unconnected, these 3 pins are internally read as Vil (see tables 5 and 6).

Write Control (WC). The Write Control feature WC is useful to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable (WC=V_{IH}) or disable (WC=V_{IL}) the internal write protection. When the WC pin is unconnected, the WC input is internally read as V_{IL} (see Table 5).

When WC=1, Device Select and Address bytes are acknowledged, Data bytes are not acknowledged.

Refer to Application Note AN404 for more detailed information about Write Control feature.

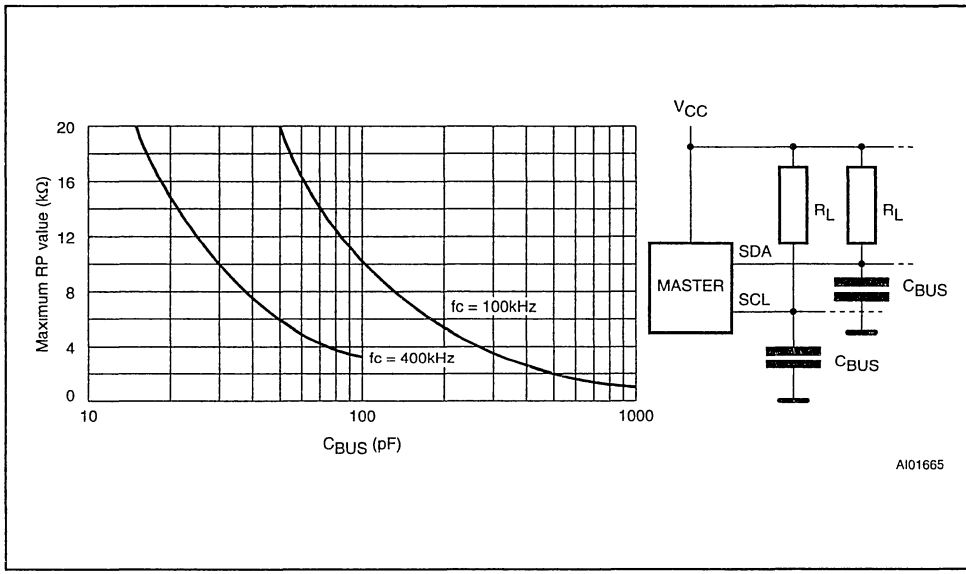
DEVICE OPERATION

I^2C Bus Background

The memory supports the extended addressing I^2C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The memory is always a slave device in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the memory continuously monitors the SDA and SCL signals for a START condition and will not respond unless one is given.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus



Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the memory and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the memory samples the SDA bus signal on the rising edge of the clock SCL. For correct device operation, the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Device Selection. To start communication between the bus master and the slave memory, the master must initiate a START condition. The 8 bits sent after a START condition are made up of a device select of 4 bits that identifies the device type, then 3 Chip Enable Input bits (E2, E1, E0) and one bit for a READ ($\overline{RW}$=1) or WRITE ($\overline{RW}$=0) operation. There are two modes both for read and write. These are summarized in Table 4 and described hereafter. A communication between the master and the slave is ended with a STOP condition.

Memory Addressing. A data byte in the memory is addressed through 2 bytes of address information. The Most Significant Byte is sent first and the Least significant Byte is sent after. Bits b15 to b0 form the address of any byte of the memory.

Most Significant Byte

b15	b14	b13	b12	b11	b10	b9	b8

Least Significant Byte

b7	b6	b5	b4	b3	b2	b1	b0

Table 5. Input Parameters (1) (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
t_{NS}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V or 2.5 to 5.5V)
(T_A = 0 to 70°C or –20 to 85°C; V_{CC} = 1.8V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current (SCL, SDA, E0, E1, E2, $\overline{WC}$)	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current -W series:	V_{CC} = 5V, f_C = 400kHz (Rise/Fall time < 30ns)		2	mA
		V_{CC} = 2.5V, f_C = 400kHz (Rise/Fall time < 30ns)		1	mA
	-R series:	V_{CC} = 1.8V, f_C = 100kHz (Rise/Fall time < 30ns)		0.8 (1)	mA
I_{CC1}	Supply Current (Stand-by)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V		10	µA
I_{CC2}	Supply Current (Stand-by)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V		2	µA
I_{CC3}	Supply Current (Stand-by)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 1.8V		1 (1)	µA
V_{IL}	Input Low Voltage (SCL, SDA, E0, E1, E2)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA, E0, E1, E2)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage ($\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage ($\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage -W series:	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
		I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V
	-R series:	I_{OL} = 0.15mA, V_{CC} = 1.8V		0.2 (1)	V

Note: 1. This is preliminary data.

Table 7. AC Characteristics

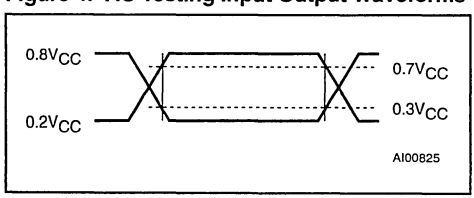
Symbol	Alt	Parameter	M24512						Unit
			V_{CC} = 4.5V to 5.5V T_A = 0 to 70°C T_A = –40 to 85°C		V_{CC} = 2.5V to 5.5V T_A = 0 to 70°C T_A = –40 to 85°C		V_{CC} = 1.8V to 3.6V T_A = 0 to 70°C T_A = –20 to 85°C		
			Min	Max	Min	Max	Min	Max	
t_{CH1CH2}	t_R	Clock Rise Time		300		300		1000	ns
t_{CL1CL2}	t_F	Clock Fall Time		300		300		300	ns
t_{DH1DH2} (1)	t_R	SDA Rise Time	20	300	20	300	20	1000	ns
t_{DL1DL2} (1)	t_F	SDA Fall Time	20	300	20	300	20	300	ns
t_{CHDX} (2)	$t_{SU\ STA}$	Clock High to Input Transition	600		600		4700		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		600		4000		ns
t_{DLCL}	$t_{HD.STA}$	Input Low to Clock Low (START)	600		600		4000		ns
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		0		0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1300		1300		4700		ns
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	100		100		250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	600		600		4000		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1300		1300		4700		ns
t_{CLQV} (3)	t_{AA}	Clock Low to Next Data Out Valid	200	900	200	900	200	3500	ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		200		200		ns
f_C	f_{SCL}	Clock Frequency		400		400		100	kHz
t_W	t_{WR}	Write Time		10		10		10	ms

Notes: 1. Sampled only, not 100% tested.
2. For a reSTART condition, or following a write cycle.
3. The minimum value delays the falling/rising edge of SDA away form SCL = 1 in order to avoid unwanted START and/or STOP condition.

Table 8. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}
Input and Output Timing Ref. Voltages	0.3V_{CC} to 0.7V_{CC}

Figure 4. AC Testing Input Output Waveforms



Write Operations

Following a START condition the master sends a Device Select code with the R$\overline{W}$ bit set to '0'. The memory acknowledges this and waits for 2 bytes of address. These 2 address bytes (8 bits each) provide access to any of the memory locations. Writing in the memory may be inhibited if input pin $\overline{WC}$ is taken high.

Any write command with $\overline{WC}$=1 (during a period of time from the START condition until the end of the 2 bytes address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 9.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition.

Figure 5. AC Waveforms

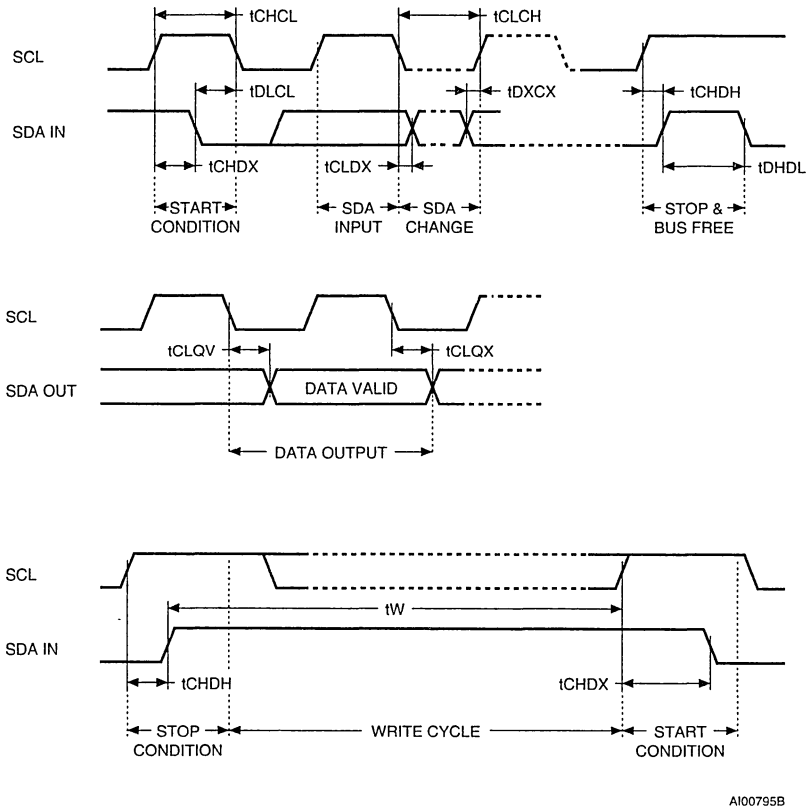
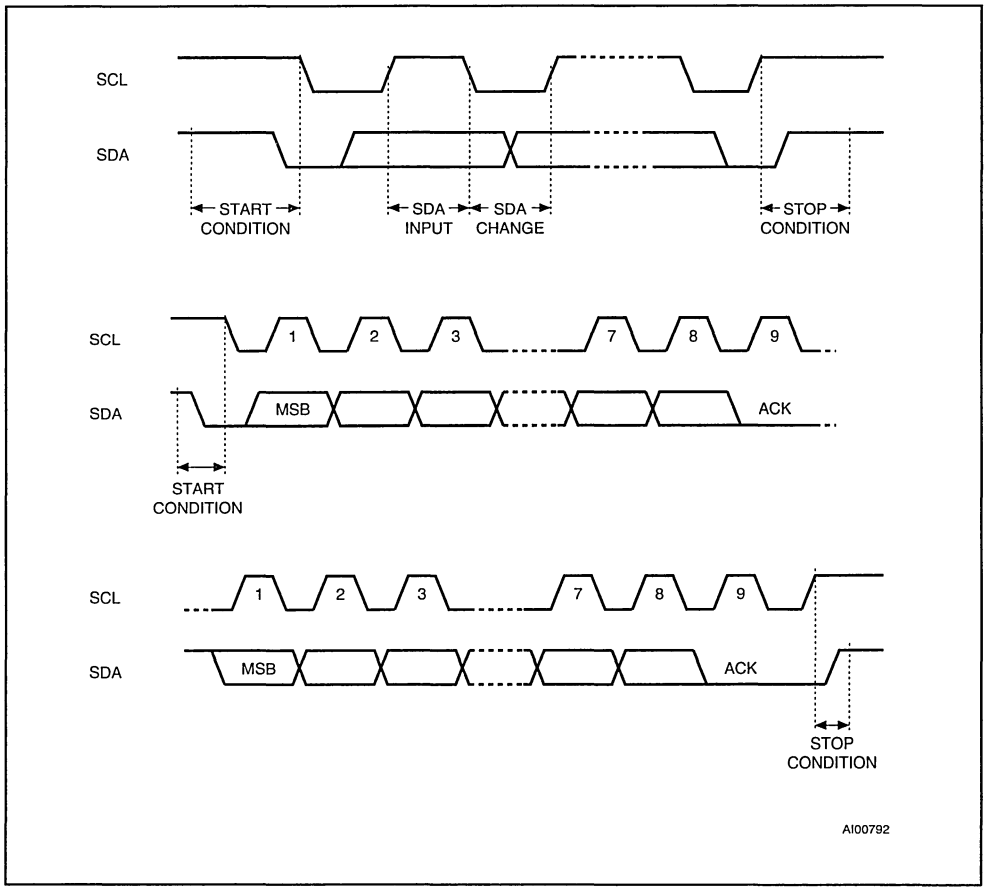


Figure 6. I²C Bus Protocol



Page Write. The Page Write mode allows up to 128 bytes to be written in a single write cycle, provided that they are all located in the same row of 128 bytes in the memory, that is the same address bits (b15-b7).

The master sends from one up to 128 bytes of data, which are each acknowledged by the memory. After each byte is transferred, the internal byte address counter (7 Least Significant Bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. This STOP condition will trigger an internal memory program cycle only if the STOP condition is internally decoded right after the AC Kbit; any STOP condition decoded out of this "10th bit" time slot will not trigger the internal programming cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal Write cycle, the memory disable itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the Write time (t_W) is given in the Table 8, this timing value may be reduced by an ACK polling sequence issued by the master.

The sequence is:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
- Step 2: if the memory is internally writing, NoACK will be returned. The master goes back to Step 1. If the memory has terminated the internal writing, it will issue an ACK.
  The memory is ready to receive the second part of the instruction (the first byte of this instruction was already sent during Step 1).

Read Operations

On delivery, the memory contents is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a Device Select with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Figure 7. Write Cycle Polling using ACK

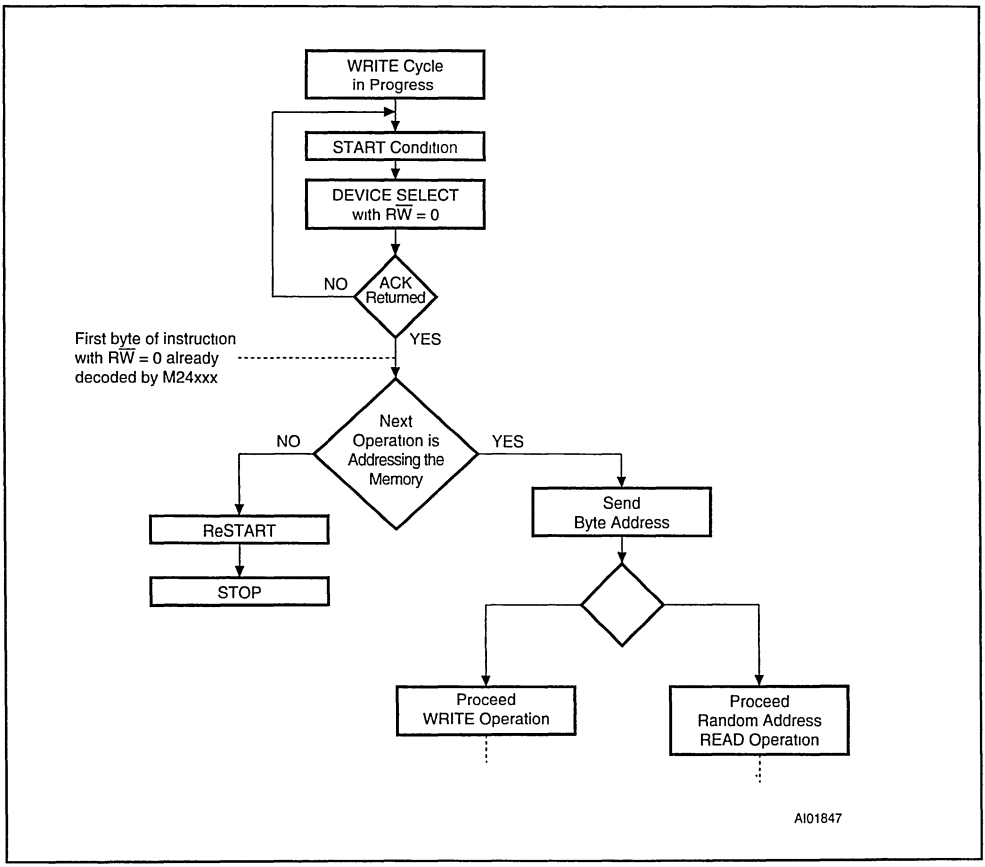
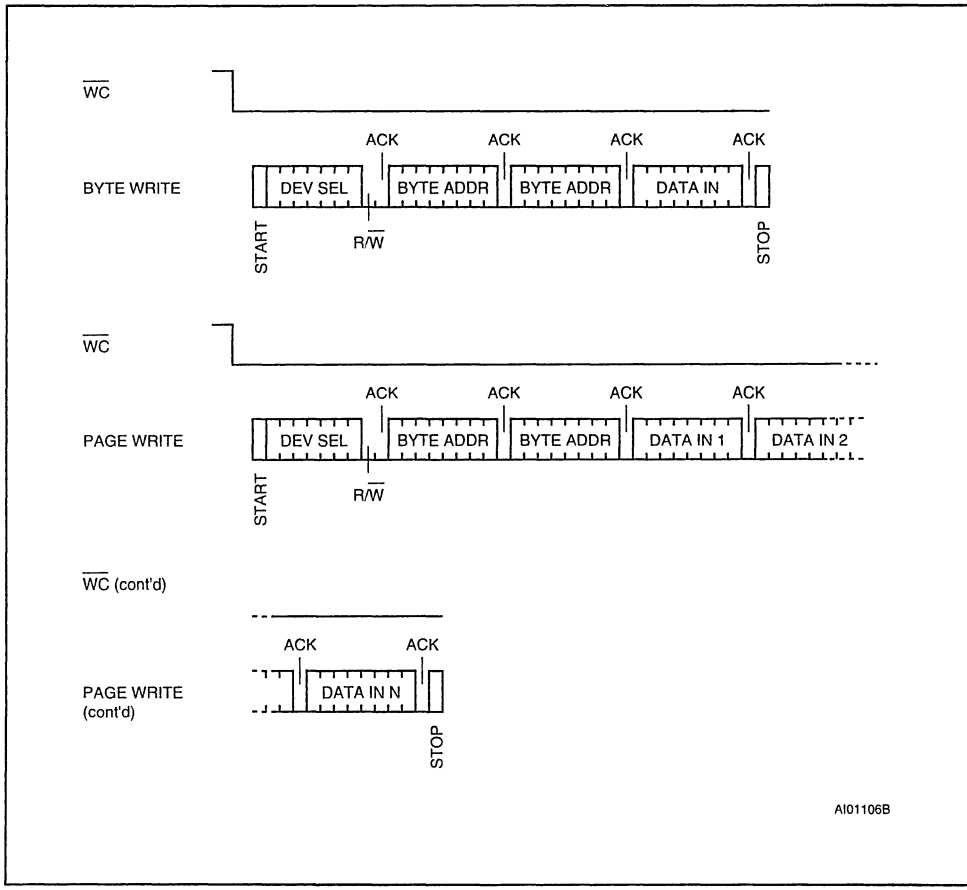


Figure 8. Write Modes Sequence with Write Control = 0



Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address repeated with the R/W bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master have to NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the memory waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the memory terminates the data transfer and switches to a standby state.

Figure 9. Write Modes Sequence with Write Control = 1

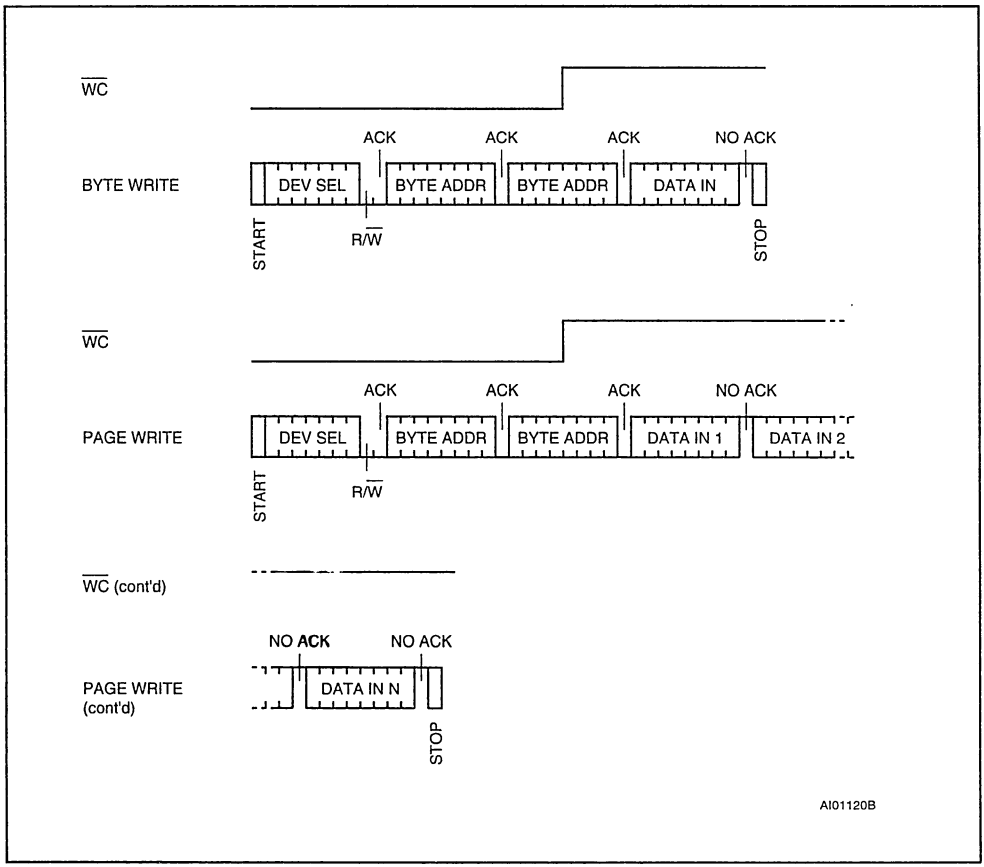
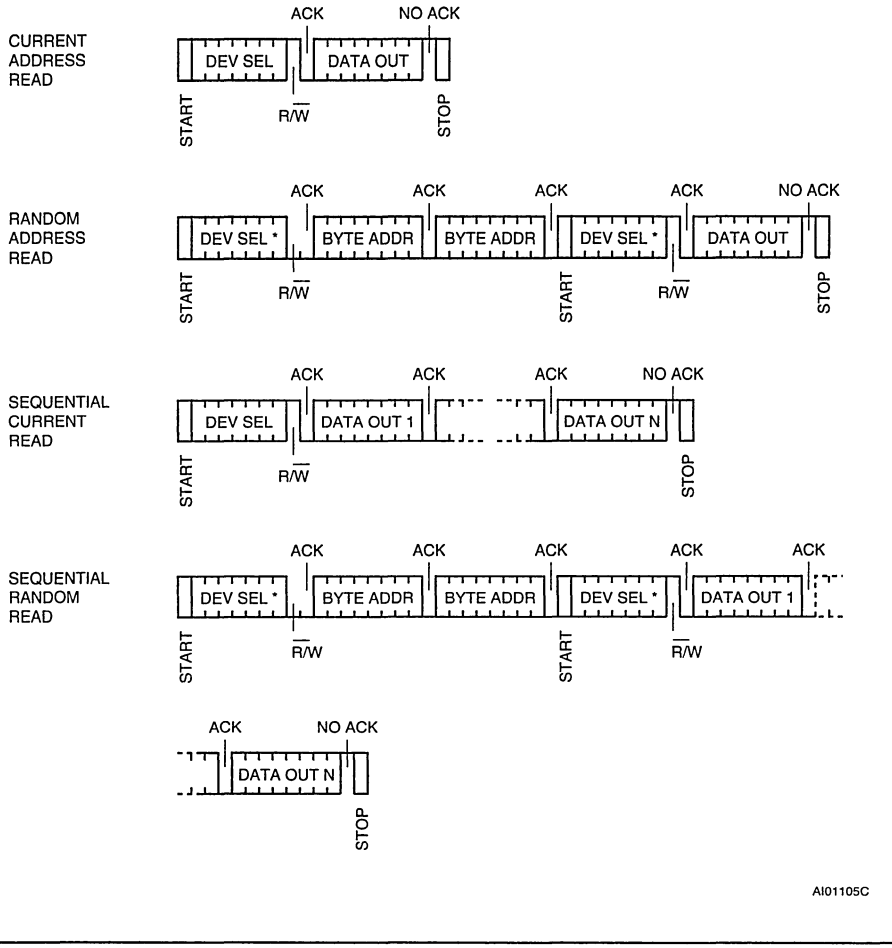
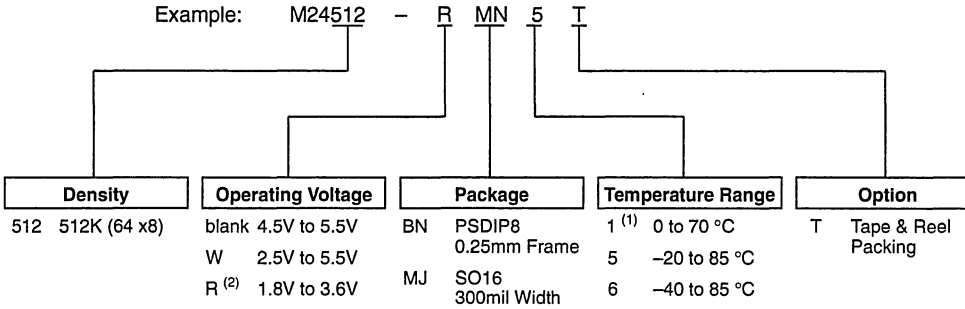


Figure 10. Read Mode Sequences



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 4th byte) must be identical.

ORDERING INFORMATION SCHEME



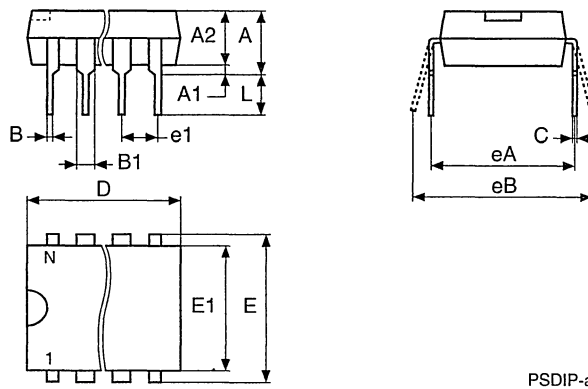
Notes: 1. Temperature range on a request only.
2. -R version (1.8V to 3 6V) are only available in temperature renge 5 or 1.

Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB		–	10.00		–	0.394
L		3.00	3.80		0.118	0.150
N	8			8		

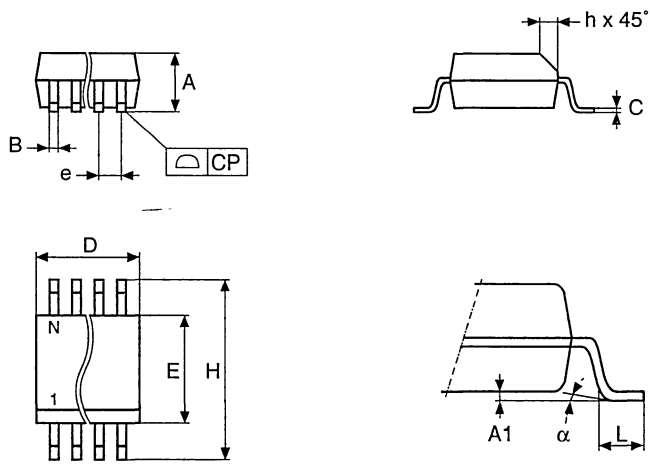


PSDIP-a

Drawing is not o scale.

SO16 - 16 lead Plastic Small Outline, 300 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.59			0.102
A1		0.10	0.30		0.004	0.012
B		0.38	0.51		0.015	0.020
C		0.23	0.25		0.009	0.010
D		10.11	10.49		0.398	0.413
E		7.44	7.54		0.293	0.297
e	1.27	–	–	0.050	–	–
H		10.16	10.41		0.400	0.410
h	0.38			0.015		
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N		16			16	
CP			0.10			0.004



SO-a

Drawing is not to scale.

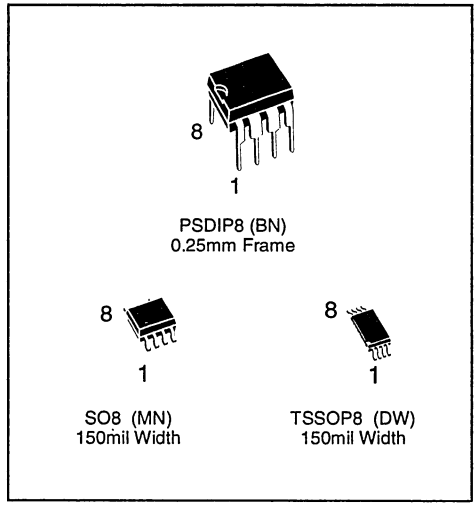
SERIAL EEPROM, SPI BUS

M95040
M95020, M95010

4K/2K/1K Serial SPI EEPROM with High Speed Clock and Positive Clock Strobe

PRELIMINARY DATA

- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  - 4.5V to 5.5V for M950x0
  - 2.5V to 5.5V for M950x0-W
  - 1.8V to 3.6V for M950x0-R
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 5 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- SUPPORTS POSITIVE CLOCK SPI MODES



DESCRIPTION

The M950x0 is a family of Electrically Erasable Programmable Memories (EEPROM) fabricated with STMicroelectronics's High Endurance Single Polysilicon CMOS technology. Each memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q).

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

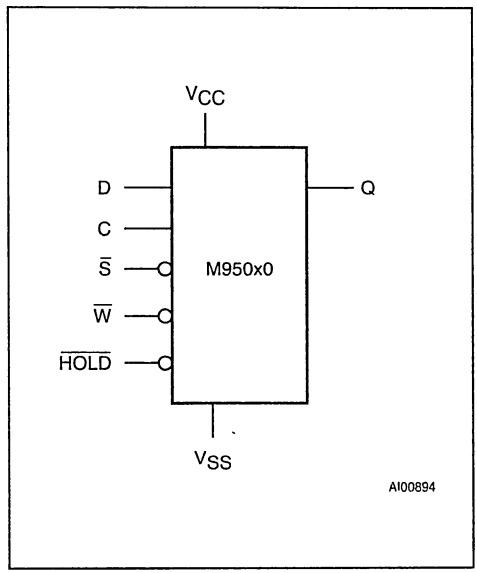


Figure 2A. DIP Pin Connections

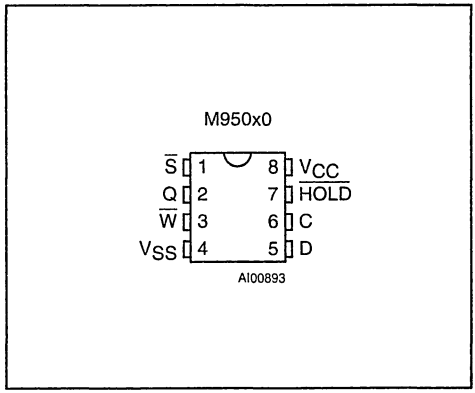


Figure 2B. SO and TSSOP Pin Connections

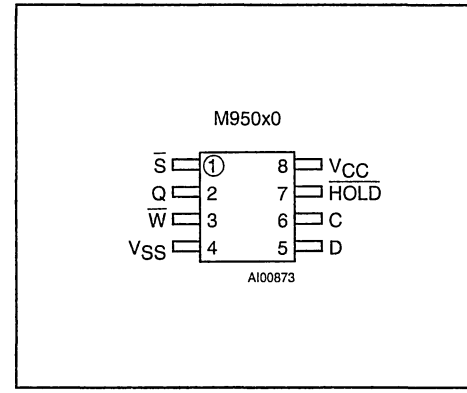


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			–40 to 125	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to V_{CC} +0.6	V
V_I	Input Voltage with respect to Ground			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents
2. MIL-STD-883C, 3015.7 (100pF, 1500Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0Ω)

DESCRIPTION (cont'd)

The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$). The write operation is disabled by a write protect input ($\overline{W}$).

Data is clocked in during the low to high transition of clock C, data is clocked out during the high to low transition of clock C.

SIGNALS DESCRIPTION

Serial Output (Q). The output pin is used to transfer data serially out of the Memory. Data is shifted out on the falling edge of the serial clock.

Serial Input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Input is latched on the rising edge of the serial clock.

Figure 3. Data and Clock Timing

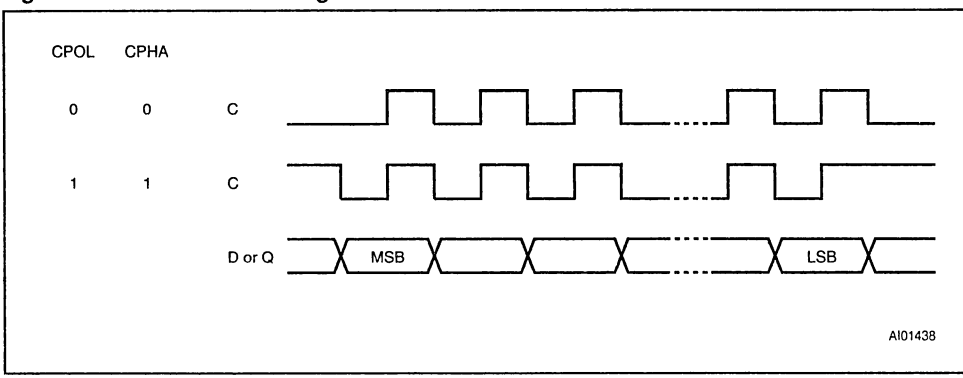
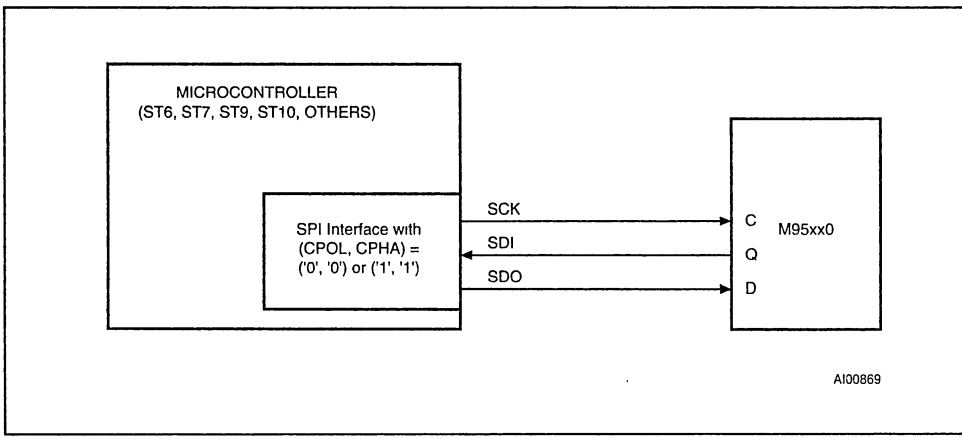


Figure 4. Microcontroller and SPI Interface Set-up



Serial Clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched on the rising edge of the clock input, while data on the Q pin changes after the falling edge of the clock input.

Chip Select ($\overline{S}$). When $\overline{S}$ is high, the Memory is deselected and the Q output pin is at high impedance and, unless an internal write operation is underway the Memory will be in the standby power mode. $\overline{S}$ low enables the Memory, placing it in the active power mode. For a safe design, it should be noted that during power up, the $\overline{S}$ input must be driven constantly high (or low) but must NOT be left floating until the supplied voltage reaches the specified V_{CC} value. After power up, a high to low transition on $\overline{S}$ is required prior to the start of any operation.

Write Protect ($\overline{W}$). This pin is for hardware write protection. When $\overline{W}$ is low, writes to the Memory are disabled but any other operations stay enabled. When $\overline{W}$ is high, all writes operations are available. $\overline{W}$ going low at any time before the last bit D0 of the data stream will reset the write enable latch and prevent programming. No action on $\overline{W}$ or on the write enable latch can interrupt a write cycle which has commenced.

Hold ($\overline{HOLD}$). The $\overline{HOLD}$ pin is used to pause serial communications with the Memory without resetting the serial sequence. To take the Hold condition into account, the product must be selected ($\overline{S}$ = 0). Then the Hold state is validated by a high to low transition on $\overline{HOLD}$ when C is low. To resume the communications, $\overline{HOLD}$ is brought high while C is low. During the Hold condition D, Q, and C are at a high impedance state.

When the Memory is under the Hold condition, it is possible to deselect the device. However, the serial communications will remain paused after a reselect, and the chip will be reset.

The Memory can be driven by a microcontroller with its SPI peripheral running in either of the two following modes: (CPOL, CPHA) = ('0', '0') or (CPOL, CPHA) = ('1', '1').

For these two modes, input data is latched in by the low to high transition of clock C, and output data is available from the high to low transition of Clock (C).

The difference between (CPOL, CPHA) = (0, 0) and (CPOL, CPHA) = (1, 1) is the stand-by polarity: C remains at '0' for (CPOL, CPHA) = (0, 0) and C remains at '1' for (CPOL, CPHA) = (1, 1) when there is no data transfer.

OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first rising edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 3 shows the instruction set and format for device operation. If an invalid instruction is sent (one not contained in Table 3), the chip is automatically deselected. For operations that read or write data in the memory array, bit 3 of the instruction is the MSB of the address, otherwise, it is a don't care.

Write Enable (WREN) and Write Disable (WRDI)

The Memory contains a write enable latch. This latch must be set prior to every WRITE or WRSR operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under the following conditions:

- $\overline{W}$ pin is low
- Power on
- WRDI instruction executed
- WRSR instruction executed
- WRITE instruction executed

As soon as the WREN or WRDI instruction is received by the memory, the circuit executes the instruction and enters a wait mode until it is deselected.

Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write to the memory operation. If a Read Status register reaches the 8th bit of the Status register, an additional 9th clock pulse will wrap around to read the 1st bit of the Status Register

The status register format is as follows:

b7							b0
1	1	1	1	BP1	BP0	WEL	WIP

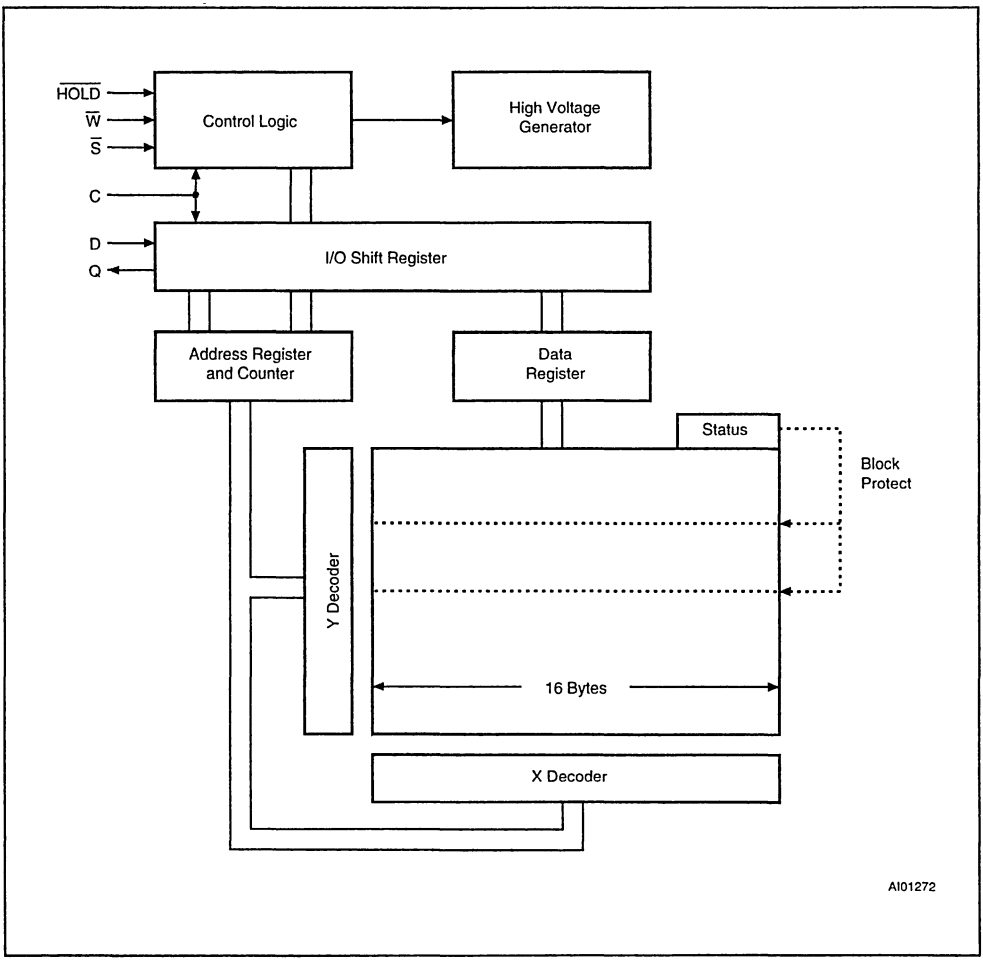
BP1, BP0. Read and write bits
WEL, WIP: Read only bits.
b7 to b4: Read only bits.

Table 3. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	0000 X110
WRDI	Reset Write Enable Latch	0000 X100
RDSR	Read Status Register	0000 X101
WRSR	Write Status Register	0000 X001
READ	Read Data from Memory Array	0000 $A_8$011
WRITE	Write Data to Memory Array	0000 $A_8$010

Notes: A_8 = 1, Upper page selected on M95040.
A_8 = 0, Lower page selected on M95040.
X = Don't care.

Figure 5. Block Diagram

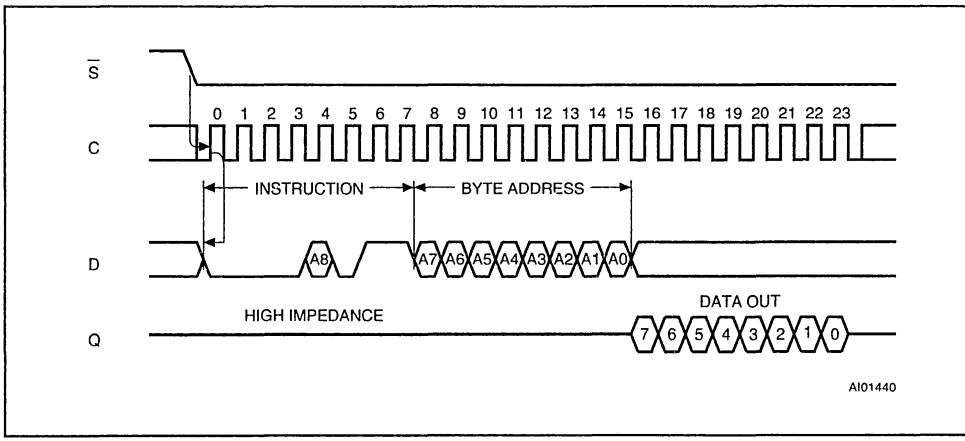


During a write to the memory operation to the memory array, all bits BP1, BP0, WEL, WIP are valid and can be read. During a write to the status register, only the bits WEL and WIP are valid and can be read. The values of BP1 and BP0 read at that time correspond to the previous contents of the status register.

The Write-In-Process (WIP) read-only bit indicates whether the Memory is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress.

The Write Enable Latch (WEL) read-only bit indicates the status of the write enable latch. When set to a '1' the latch is set, when set to a '0' the latch is reset. The Block Protect (BP0 and BP1) bits indicate the extent of the protection employed. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

Figure 6. Read Operation Sequence



Notes: A8 = A7 = X on M95010 and M95020; A8 is only active on M95040
X = Don't care.

Table 4. Write Protected Block Size

Status Register Bits		Protected Block	Array Address Protected		
BP1	BP0		M95040	M95020	M95010
0	0	none	none	none	none
0	1	Upper quarter	180h - 1FFh	C0h - FFh	60h - 7Fh
1	0	Upper half	100h - 1FFh	80h - FFh	40h - 7Fh
1	1	Whole memory	000h - 1FFh	00h - FFh	00h - 7Fh

Write Status Register (WRSR)

The WRSR instruction writes (only) the BP1 and BP0 bits allowing to define the size of protected memory. The user may read the blocks but will be unable to write within the protected blocks. The blocks and respective WRSR control bits are shown in Table 4.

When the WRSR instruction and the 8 bits of the Status Register are latched-in, the internal write cycle is then triggered by the rising edge of $\overline{S}$.

This rising edge of $\overline{S}$ must appear no later than the 16th clock cycle of the WRSR instruction of the Status Register content (it must not appear a 17th clock pulse before the rising edge of $\overline{S}$), otherwise the internal write sequence is not performed.

Read Operation

The chip is first selected by putting $\overline{S}$ low. The serial one byte read instruction is followed by a one byte address (A7-A0), each bit being latched-in during the rising edge of the clock (C). Bit 3 (see Table 3) of the read instruction contains address bit A8 (most significant address bit). Then the data stored in the memory at the selected address is shifted out on the Q output pin; each bit being shifted out during the falling edge of the clock (C).

The data stored in the memory at the next address can be read in sequence by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to 0h allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during a write cycle will be rejected and will deselect the chip.

Figure 7. Write Enable Latch Sequence

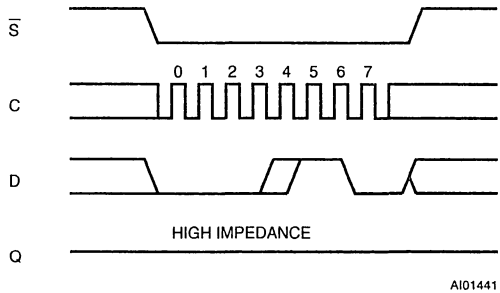
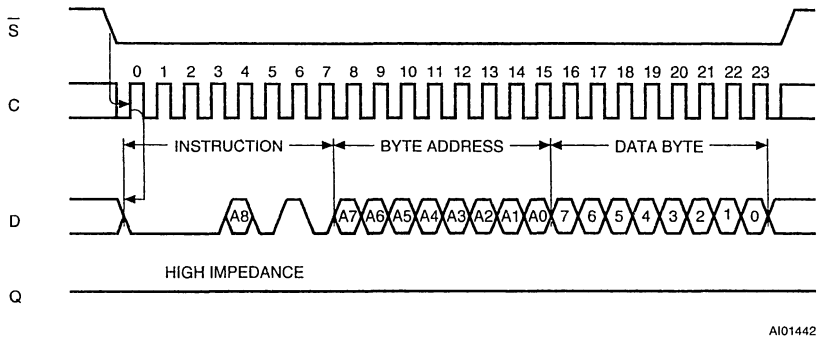
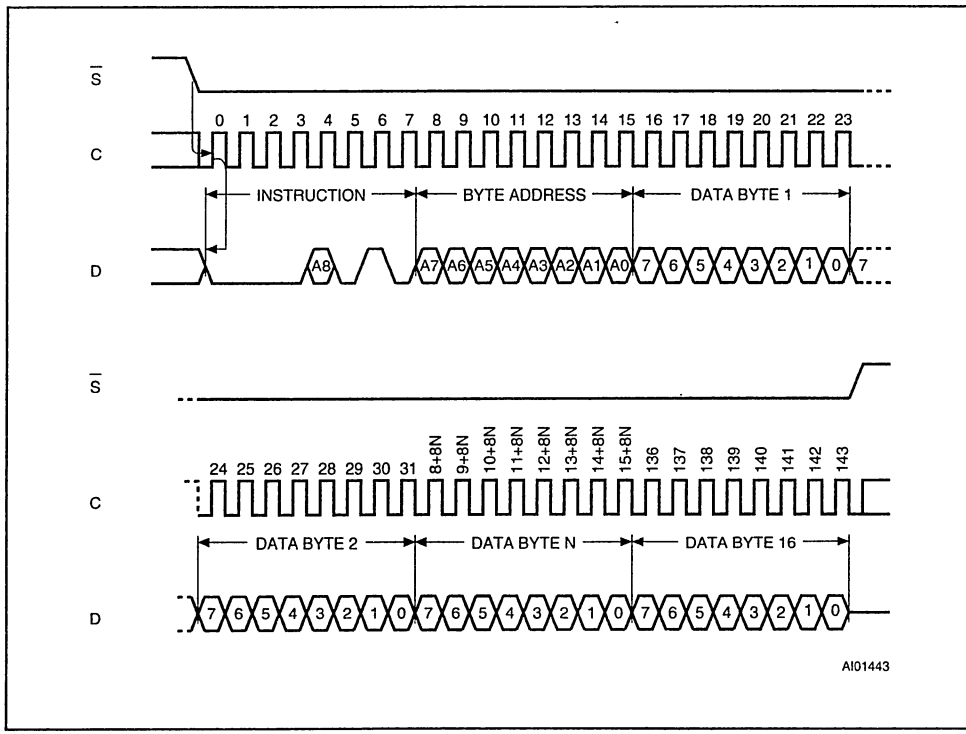


Figure 8. Byte Write Operation Sequence



Notes: A8 = A7 = X on M95010 and M95020; A8 is only active on M95040.
X = Don't care.

Figure 9. Page Write Operation Sequence



Notes: A8 = A7 = X on M95010 and M95020; A8 is only active on M95040.
X = Don't care.

Figure 10. RDSR: Read Status Register Sequence

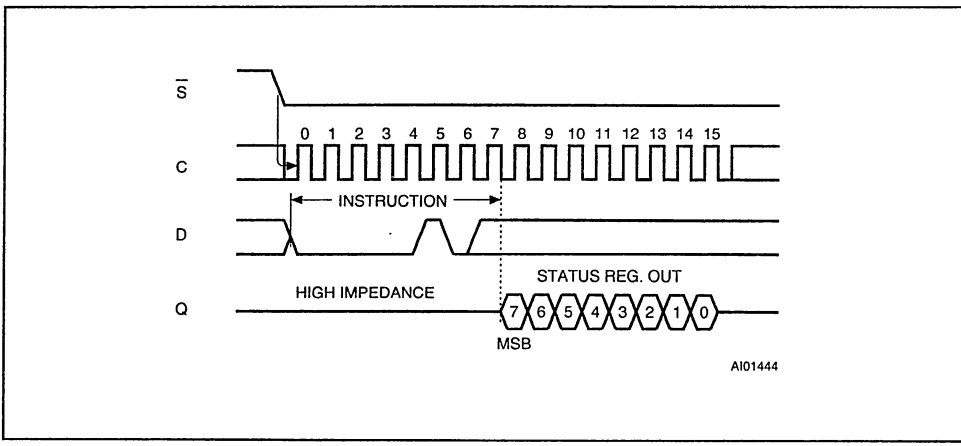
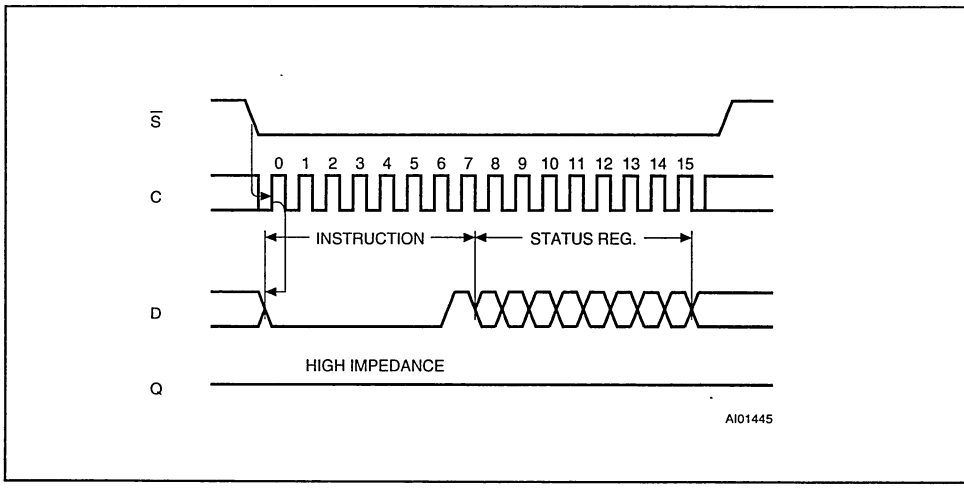


Figure 11. WRSR: Write Status Register Sequence



Byte Write Operation

Prior to any write attempt, the write enable latch must be set by issuing the WREN instruction. First the device is selected ($\overline{S}$ = low) and a serial WREN instruction byte is issued. Then the product is deselected by taking $\overline{S}$ high. After the WREN instruction byte is sent, the Memory will set the write enable latch and then remain in standby until it is deselected. Then the write state is entered by selecting the chip, issuing two bytes of instruction and address, and one byte of data.

Chip Select ($\overline{S}$) must remain low for the entire duration of the operation. The product must be deselected just after the eighth bit of data has been latched in. If not, the write process is cancelled. As soon as the product is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read to check BP1, BP0, WEL and WIP. WIP is high during the self-timed write cycle. When the cycle is completed, the write enable latch is reset.

Page Write Operation

A maximum of 16 bytes of data may be written during one non-volatile write cycle. All 16 bytes must reside on the same page. The page write mode is the same as the byte write mode except that instead of deselecting the device after the first byte of data, up to 15 additional bytes can be shifted in prior to deselecting the chip. A page address begins with address xxxx 0000 and ends with xxxx 1111. If the address counter reaches xxxx 1111 and the clock continues, the counter will roll over to the first address of the page (xxxx 0000) and overwrite any previously written data. The programming cycle will only start if the $\overline{S}$ transition occurs just after the eighth bit of data of a word is received.

POWER ON STATE

After a Power up the Memory is in the following state:

- The device is in the low power standby state.
- The chip is deselected.
- The chip is not in hold condition.

The Status Register content at power-up is:

				BP1	BP0	WEL	WIP
1	1	1	1	0	0	0	0

Figure 12. EEPROM and SPI Bus

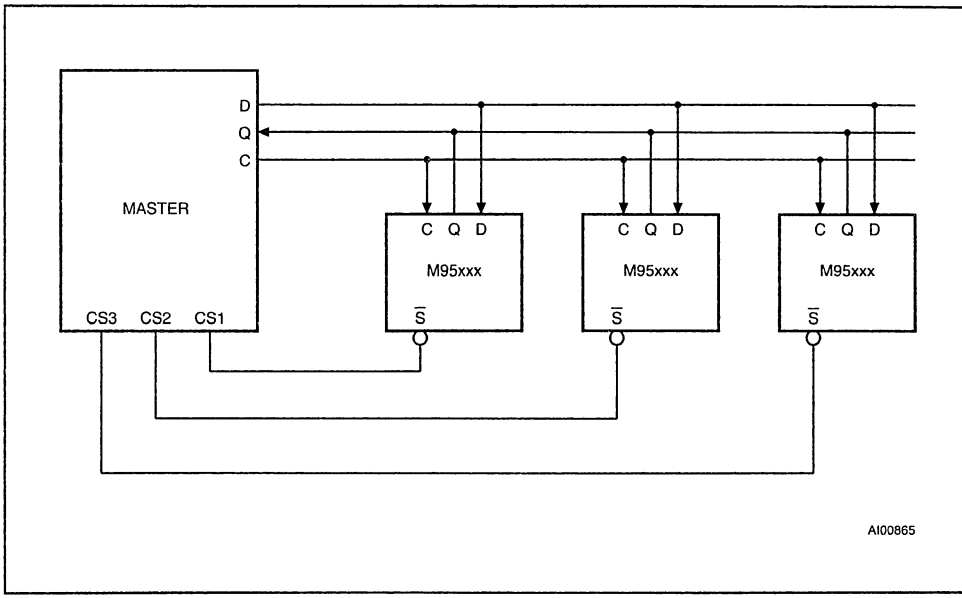


Table 5. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$
Output Load	C_L = 100pF

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 13. AC Testing Input Output Wavef.

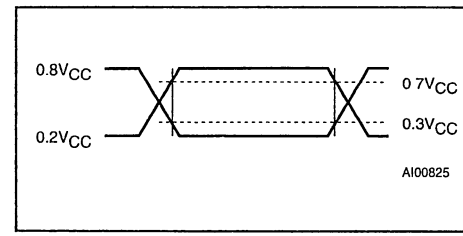


Table 6. Input Parameters (1) (T_A = 25 °C, f = 5 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (D)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF

Note: 1. Sampled only, not 100% tested.

Table 7. DC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 4.5V to 5.5V)
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.5V to 5.5V)
(T_A = 0 to 70°C or –20 to 85°C; V_{CC} = 1.8V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			±2	µA
I_{LO}	Output Leakage Current			±2	µA
I_{CC}	Supply Current	C = 0.1 V_{CC}/0.9 V_{CC}, at 5 MHz, V_{CC} = 5V, Q = Open		4	mA
		C = 0.1 V_{CC}/0.9 V_{CC}, at 2 MHz, V_{CC} = 5V, Q = Open, Note 2		4	mA
	Supply Current (W series)	C = 0.1 V_{CC}/0.9 V_{CC}, at 2 MHz, V_{CC} = 2.5V, Q = Open		2	mA
	Supply Current (R series)	C = 0.1 V_{CC}/0.9 V_{CC}, at 1 MHz, V_{CC} = 1.8V, Q = Open		2	mA
I_{CC1}	Standby Current	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V		10	µA
		$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V, Note 2		10	µA
	Standby Current (W series)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V		2	µA
	Standby Current (R series)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 1.8V		1	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{OL} (1)	Output Low Voltage	I_{OL} = 2mA, V_{CC} = 5V		0.4	V
		I_{OL} = 2mA, V_{CC} = 5V, Note 2		0.4	V
	Output Low Voltage (W series)	I_{OL} = 1.5mA, V_{CC} = 2.5V		0.4	V
	Output Low Voltage (R series)	I_{OL} = 0.15mA, V_{CC} = 1.8V		0.3	V
V_{OH} (1)	Output High Voltage	I_{OH} = –2mA, V_{CC} = 5V	0.8 V_{CC}		V
		I_{OH} = –2mA, V_{CC} = 5V, Note 2	0.8 V_{CC}		V
	Output High Voltage (W series)	I_{OH} = –0.4mA, V_{CC} = 2.5V	0.8 V_{CC}		V
	Output High Voltage (R series)	I_{OH} = –0.1mA, V_{CC} = 1.8V	0.8 V_{CC}		V

Notes: 1. The device meets output requirements for both TTL and CMOS standards.
2. Test performed at –40 to 125°C temperature range, grade 3.

Table 8A. AC Characteristics

Symbol	Alt	Parameter	M95040 / M95020 / M95010				Unit
			V_{CC} = 4.5V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		V_{CC} = 4.5V to 5.5V, T_A = –40 to 125°C		
			Min	Max	Min	Max	
f_C	f_C	Clock Frequency	D.C.	5	D.C.	2	MHz
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time	90		200		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	90		200		ns
t_{CH} (1)	t_{CLH}	Clock High Time	90		200		ns
t_{CL} (1)	t_{CLL}	Clock Low Time	90		200		ns
t_{CLCH} (2)	t_{RC}	Clock Rise Time		1		1	µs
t_{CHCL} (2)	t_{FC}	Clock Fall Time		1		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		40		ns
t_{CHDX}	t_{DH}	Data In Hold Time	30		50		ns
t_{DLDH} (2)	t_{RI}	Data In Rise Time		1		1	µs
t_{DHDL} (2)	t_{FI}	Data In Fall Time		1		1	µs
t_{HHCH}		$\overline{HOLD}$ Setup Time	70		140		ns
t_{HLCH}		Clock Low Hold Time	40		90		ns
t_{CLHL}		Clock Low Setup Time before $\overline{HOLD}$ Active	0		0		ns
t_{CLHH}		Clock Low Setup Time before $\overline{HOLD}$ Not Active	0		0		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	90		200		ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time	90		200		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	100		200		ns
t_{SHQZ} (2)	t_{DIS}	Output Disable Time		100		250	ns
t_{CLQV}	t_V	Clock Low to Output Valid		60		150	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		ns
t_{QLQH} (2)	t_{RO}	Output Rise Time		50		100	ns
t_{QHQL} (2)	t_{FO}	Output Fall Time		50		100	ns
t_{HHQX} (2)	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		50		100	ns
t_{HLQZ} (2)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		100		250	ns
t_W	t_{WP}	Write Cycle Time		10		10	ms

Notes: 1. $t_{CH} + t_{CL} \geq 1/f_C$.
2. Value guaranteed by characterization, not 100% tested in production.

Table 8B. AC Characteristics

Symbol	Alt	Parameter	M95040 / M95020 / M95010				Unit
			V_{CC} = 2.5V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		V_{CC} = 1.8V to 3.6V, T_A = 0 to 70°C, T_A = –20 to 85°C		
			Min	Max	Min	Max	
f_C	f_C	Clock Frequency	D.C.	2	D.C.	1	MHz
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time	200		400		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	200		400		ns
t_{CH} (1)	t_{CLH}	Clock High Time	200		400		ns
t_{CL} (1)	t_{CLL}	Clock Low Time	200		400		ns
t_{CLCH} (2)	t_{RC}	Clock Rise Time		1		1	µs
t_{CHCL} (2)	t_{FC}	Clock Fall Time		1		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	40		60		ns
t_{CHDX}	t_{DH}	Data In Hold Time	50		100		ns
t_{DLDH} (2)	t_{RI}	Data In Rise Time		1		1	µs
t_{DHDL} (2)	t_{FI}	Data In Fall Time		1		1	µs
t_{HHCH}		$\overline{HOLD}$ Setup Time	140		350		ns
t_{HLCH}		Clock Low Hold Time	90		200		ns
t_{CLHL}		Clock Low Setup Time before $\overline{HOLD}$ Active	0		0		ns
t_{CLHH}		Clock Low Setup Time before $\overline{HOLD}$ Not Active	0		0		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	200		400		ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time	200		400		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	200		300		ns
t_{SHQZ} (2)	t_{DIS}	Output Disable Time		250		500	ns
t_{CLQV}	t_V	Clock Low to Output Valid		150		380	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		ns
t_{QLQH} (2)	t_{RO}	Output Rise Time		100		200	ns
t_{QHQL} (2)	t_{FO}	Output Fall Time		100		200	ns
t_{HHQX} (2)	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		100		250	ns
t_{HLQZ} (2)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		250		500	ns
t_W	t_{WP}	Write Cycle Time		10		10	ms

Notes: 1. $t_{CH} + t_{CL} \geq 1/f_C$.
2. Value guaranteed by characterization, not 100% tested in production.

Figure 14. Serial Input Timing

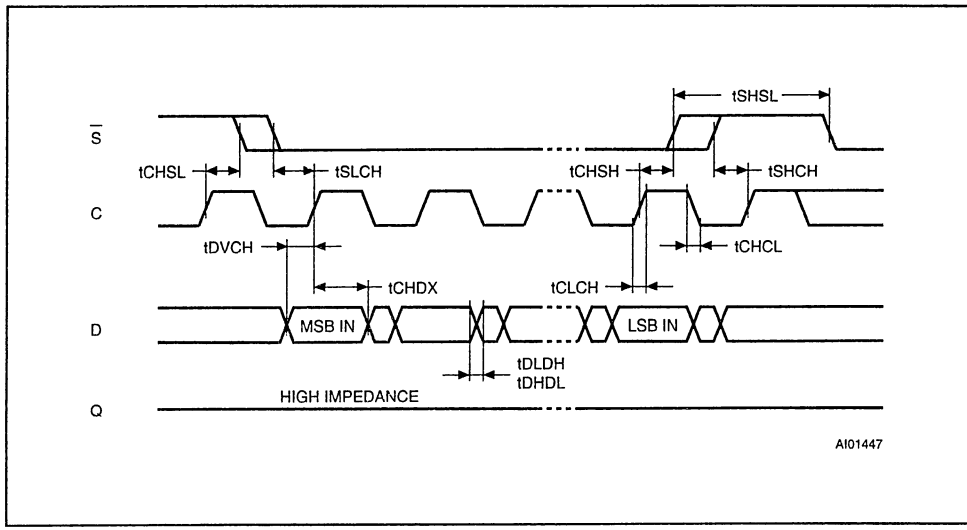


Figure 15. Hold Timing

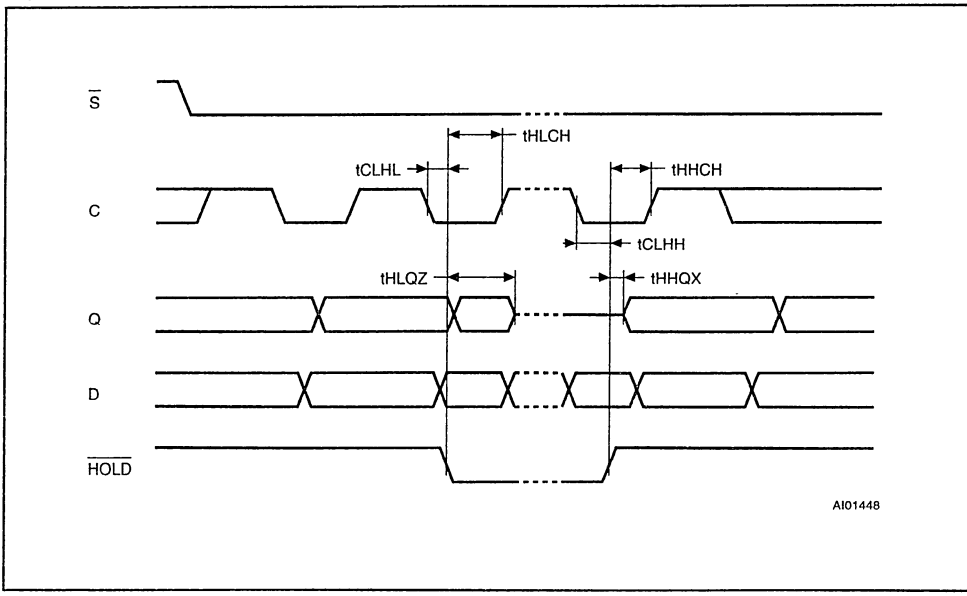
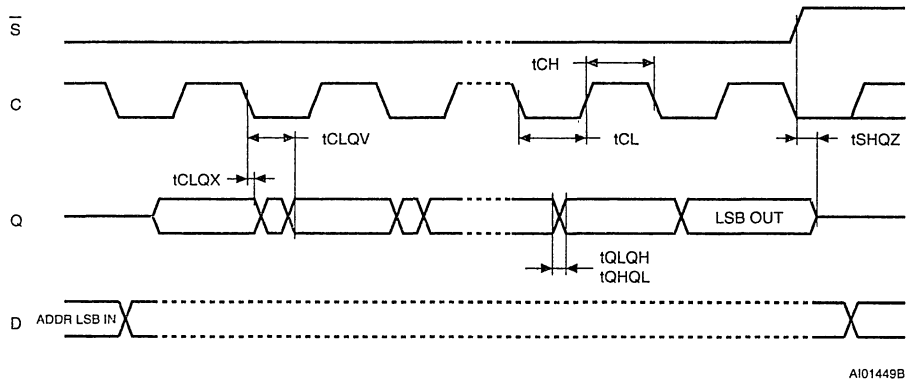
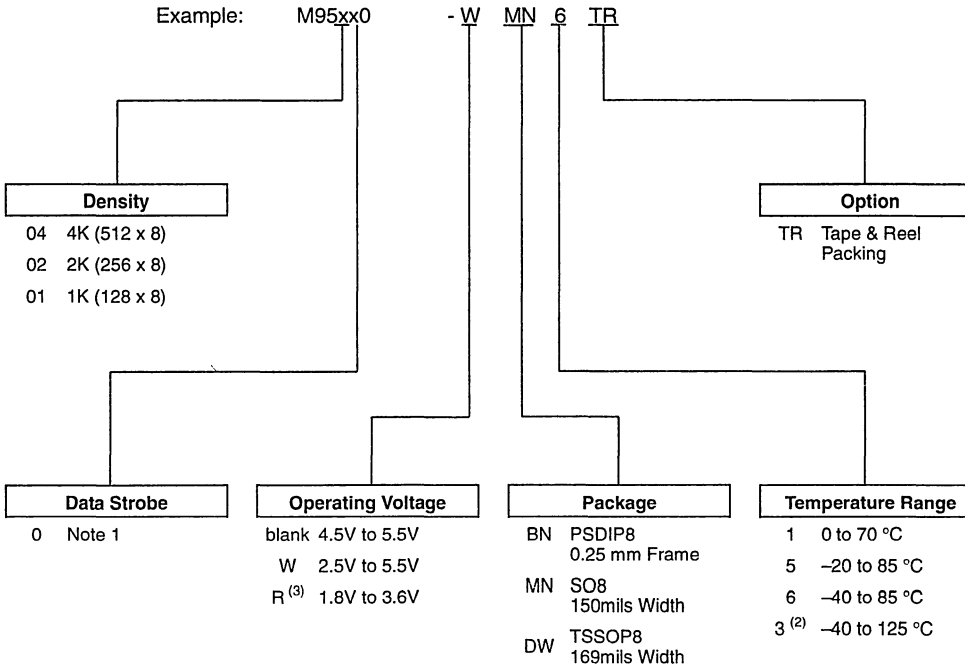


Figure 16. Output Timing



ORDERING INFORMATION SCHEME



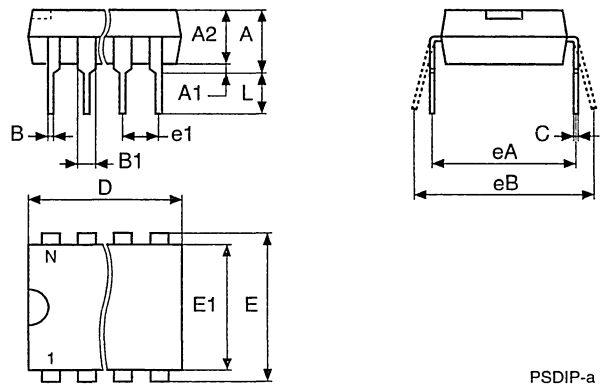
Notes: 1. Data In is strobed on rising edge of the clock (C) and Data Out is synchronized from the falling edge of the clock.
2. Temperature range on request only, 5V ± 10% only.
3. -R versions (1.8V to 3 6V) are only available in temperature range 5 or 1.

Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		
CP			0.10			0.004

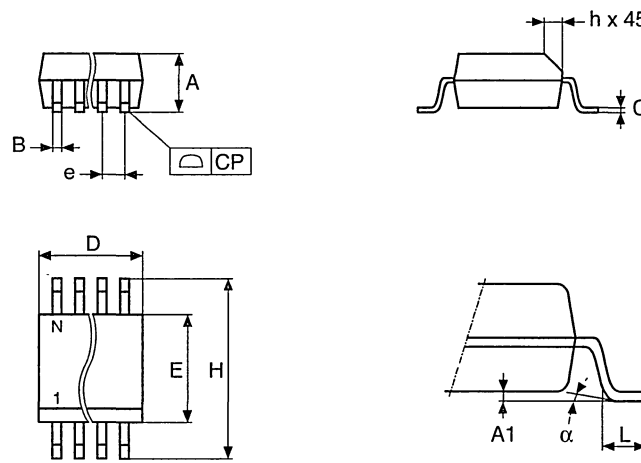


PSDIP-a

Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

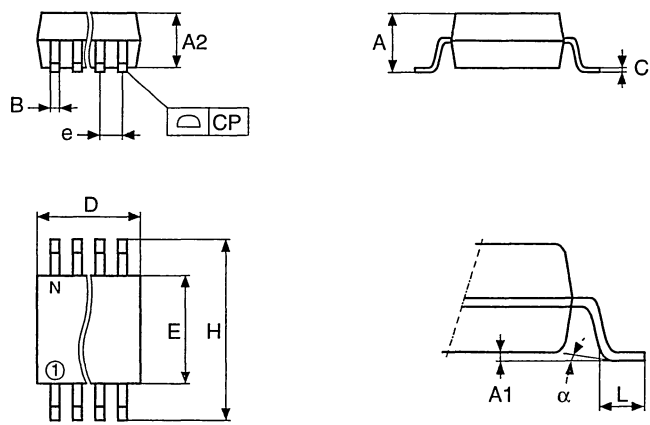


SO-a

Drawing is not to scale

TSSOP8 - 8 lead Thin Shrink Small Outline, 169 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.10			0.043
A1		0.05	0.15		0.002	0.006
A2		0.85	0.95		0.033	0.037
B		0.19	0.30		0.007	0.012
C		0.09	0.20		0.004	0.008
D		2.90	3.10		0.114	0.122
E		6.25	6.50		0.246	0.256
E1		4.30	4.50		0.169	0.177
e	0.65	–	–	0.026	–	–
L		0.50	0.70		0.020	0.028
α		0°	8°		0°	8°
N	8			8		
CP			0.08			0.003



SO-b

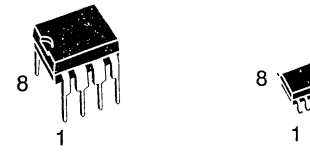
Drawing is not to scale

M95640, M95320
M95160, M95080

64K/32K/16K/8K Serial SPI EEPROM with High Speed Clock and Positive Clock Strobe

PRELIMINARY DATA

- 100,000 ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  - 4.5V to 5.5V for M95xxx
  - 2.7V to 5.5V for M95xxx-V
  - 2.5V to 5.5V for M95xxx-W
  - 1.8V to 3.6V for M95xxx-R
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 5 MHz CLOCK RATE MAX
- STATUS REGISTER
- HARDWARE PROTECTION of the STATUS REGISTER
- 32 BYTE PAGE MODE
- SIZEABLE READ ONLY EEPROM AREA
- SELF-TIMED PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- SUPPORTS POSITIVE CLOCK SPI MODES



PSDIP8 (BN)
0.25mm Frame

SO8 (MN)
150 mil Width

DESCRIPTION

The M95xxx is a family of electrically erasable programmable memories (EEPROM) fabricated with STMicroelectronics' High Endurance Double Polysilicon CMOS technology. Each memory is accessed by a simple SPI bus compatible serial interface.

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

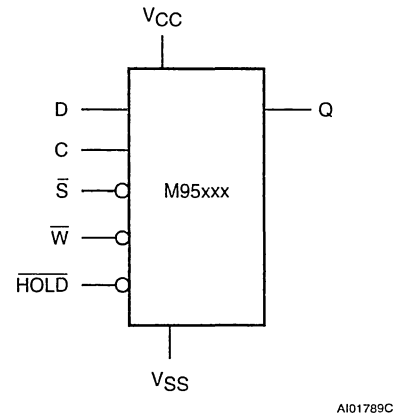


Figure 2A. DIP Pin Connections

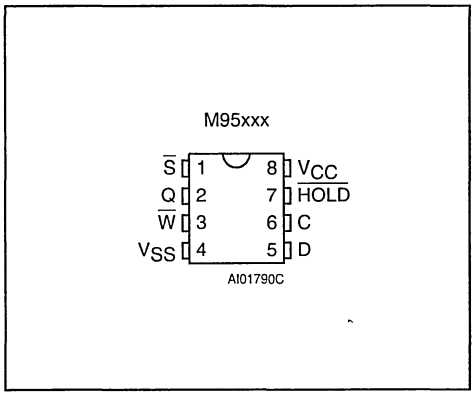


Figure 2B. SO Pin Connections

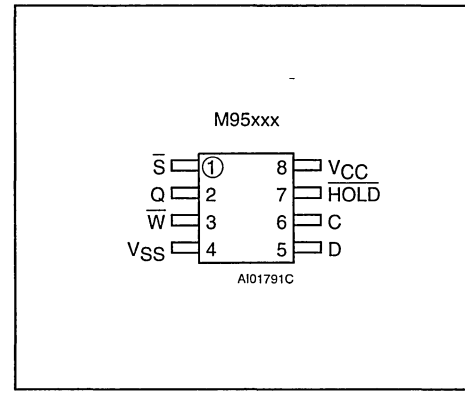


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			–40 to 125	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to V_{CC} +0.6	V
V_I	Input Voltage with respect to Ground			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			400	V

Notes: 1 Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. DMIL-STD-883C, 3015.7 (100pF, 1500Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0Ω)

DESCRIPTION (cont'd)

The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q).

The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$).

Data is clocked in during the low to high transition of clock C, data is clocked out during the high to low transition of clock C.

SIGNALS DESCRIPTION

Serial Output (Q). The output pin is used to transfer data serially out of the memory. Data is shifted out on the falling edge of the serial clock.

Serial Input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Input is latched on the rising edge of the serial clock.

Serial Clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched

Figure 3. Data and Clock Timing

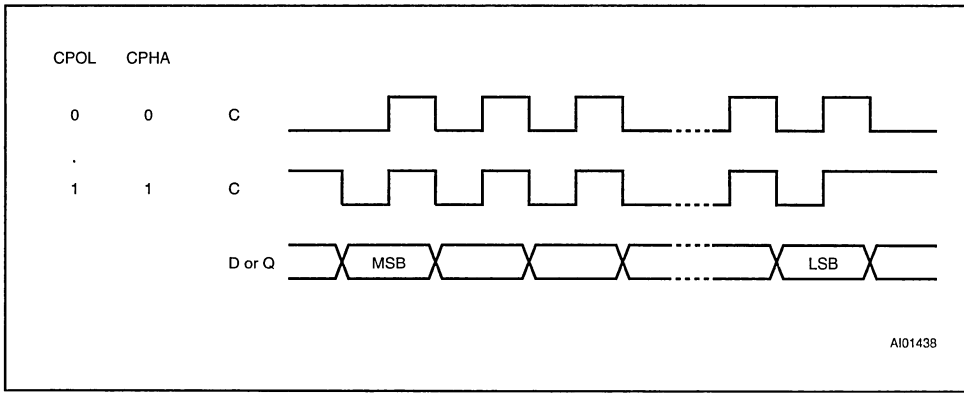
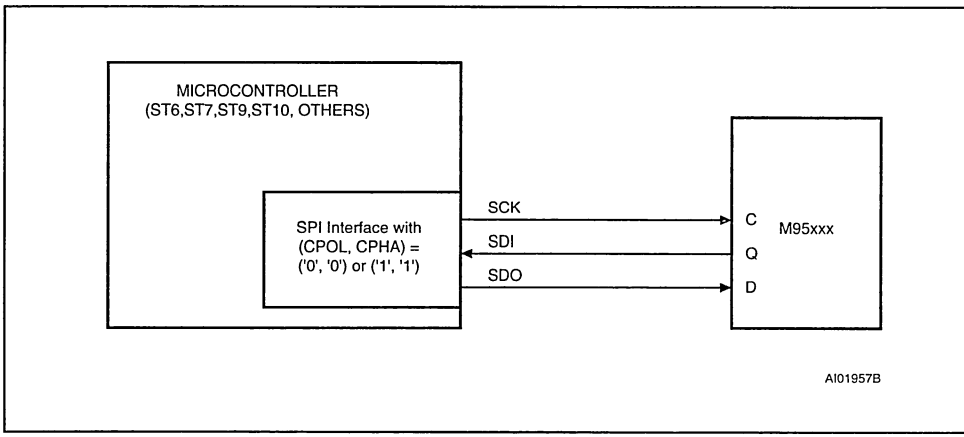


Figure 4. Microcontroller and SPI Interface Set-up



on the rising edge of the clock input, while data on the Q pin changes after the falling edge of the clock input.

Chip Select ($\overline{S}$). When $\overline{S}$ is high, the memory is deselected and the Q output pin is at high impedance and, unless an internal write operation is underway the memory will be in the standby power mode. $\overline{S}$ low enables the memory, placing it in the active power mode. It should be noted that after power-on, a high to low transition on $\overline{S}$ is required prior to the start of any operation.

Write Protect ($\overline{W}$). This pin is for hardware write protection of the status register (SR); except WIP and WEL bits. When bit 7 (SRWD) of the status register is 0 (the initial delivery state); it is possible to write the SR once the WEL (Write Enable Latch) has been set and whatever is the status of pin $\overline{W}$ (high or low).

Note: SRWD stands for; Status Register Write Disable.

Table 3. Protection Feature

$\overline{W}$	SRWD	Status Register (SR)	Data Bytes (Protected Area)	Mode	Data Bytes (Unprotected Area)
X	0	Writable after setting WEL	Software Write protected by the BPn bits of the Status Register	SPM	Writable after setting WEL
1	1	Writable after setting WEL	Software Write protected by the BPn bits of the Status Register	SPM	Writable after setting WEL
0	1	Hardware Write protected	Hardware Write protected	HPM	Writable after setting WEL

Notes: 1. SPM stands for Software Protected Mode.
2. BPn are BP0 to BP1 bits of the Status Register
3. SPM and HPM are also described in the Write Status Register (WRSR) section

SIGNALS DESCRIPTION (cont'd)

Once bit 7 (SRWD) of the status register has been set to 1; the possibility to rewrite the SR depends on the logical level present at pin $\overline{W}$:

- If $\overline{W}$ pin is high; it will be possible to rewrite the status register after having set the WEL (Write Enable Latch).
- If $\overline{W}$ pin is low; any attempt to modify the status register will be ignored by the device even if the WEL was set. As a consequence: all the data bytes in the EEPROM area protected by the BPn bits of the status register are also hardware protected against data corruption and can be seen as a Read Only EEPROM area from the microcontroller. This mode is called the Hardware Protected Mode (HPM).

It is possible to enter the Hardware Protected Mode (HPM) by setting SRWD bit after pulling down the $\overline{W}$ pin or by pulling down the $\overline{W}$ pin after setting SRWD bit.

The only way to abort the Hardware Protected Mode once entered is to pull high the $\overline{W}$ pin.

If $\overline{W}$ pin is permanently tied to high level; the Hardware Protected Mode will never be activated and the memory will only allow the user to software protect a part of the memory with the BPn bits of the status register. All protection features of the device are summarized in Table 3.

Hold ($\overline{HOLD}$). The $\overline{HOLD}$ pin is used to pause serial communications with an SPI memory without resetting the serial sequence. To take the Hold condition into account, the product must be selected ($\overline{S}$ = 0). Then the Hold state is validated by a high to low transition on $\overline{HOLD}$ when C is low. To resume the communications, $\overline{HOLD}$ is brought high while C is low. During the Hold condition D, Q, and C are at a high impedance state.

When the memory is under the Hold condition, it is possible to deselect the device. However, the serial communications will remain paused after a reselect, and the chip will be reset.

The memory can be driven by a microcontroller with its SPI peripheral running in either of the two following modes: (CPOL, CPHA) = ('0', '0') or (CPOL, CPHA) = ('1', '1').

For these two modes, input data is latched in by the low to high transition of clock C, and output data is available from the high to low transition of Clock (C).

The difference between (CPOL, CPHA) = (0, 0) and (CPOL, CPHA) = (1, 1) is the stand-by polarity: C remains at '0' for (CPOL, CPHA) = (0, 0) and C remains at '1' for (CPOL, CPHA) = (1, 1) when there is no data transfer.

OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first rising edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 4 shows the instruction set and format for device operation. If an invalid instruction is sent (one not contained in Table 4), the chip is automatically deselected.

Write Enable (WREN) and Write Disable (WRDI)

The memory contains a write enable latch. This latch must be set prior to every WRITE, WRSR operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under the following conditions:

- Power on,
- WRDI instruction completion,
- WRSR instruction completion,
- WRITE instruction completion.

As soon as the WREN or WRDI instruction is received, the circuit executes the instruction and enters a wait mode until it is deselected.

Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write to the memory operation.

As soon as the 8th bit of the status register is read out, the memory enters a wait mode (data on D is not decoded, Q is in Hi-Z) until it is deselected.

The status register format is as follows:

b7							b0
SRWD	X	X	X	BP1	BP0	WEL	WIP

BP0, BP1: Read and write bits
WEL, WIP: Read only bits
SRWD: Read and Write bit.

During a write to the memory operation: all bits BP0, BP1, WEL, WIP are valid and can be read. During a write to the status register, only the bits WEL and WIP are valid and can be read. The values of BP1 and BP0 read at that time correspond to the previous contents of the status register.

The Write-In-Process (WIP) read-only bit indicates whether the memory is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress.

The Write Enable Latch (WEL) read-only bit indicates the status of the write enable latch. When set to a '1' the latch is set, when set to a '0' the latch is reset. The Block Protect (BP0 and BP1) bits indicate the extent of the protection employed. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

Table 4. Instruction Set

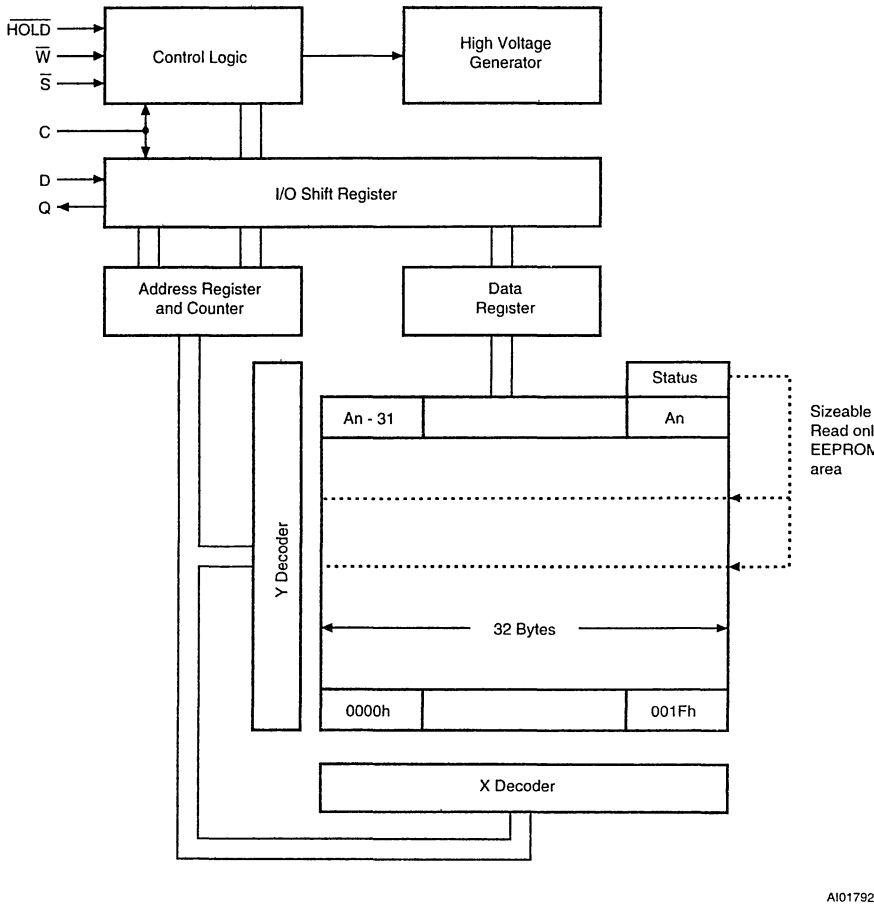
Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	0000 0110
WRDI	Reset Write Enable Latch	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read Data from Memory Array	0000 0011
WRITE	Write Data to Memory Array	0000 0010

Table 5. Address Range Bits

Device	M95080	M95160	M95320	M95640
Address Bit	A0-A9	A0-A10	A0-A11	A0-A12

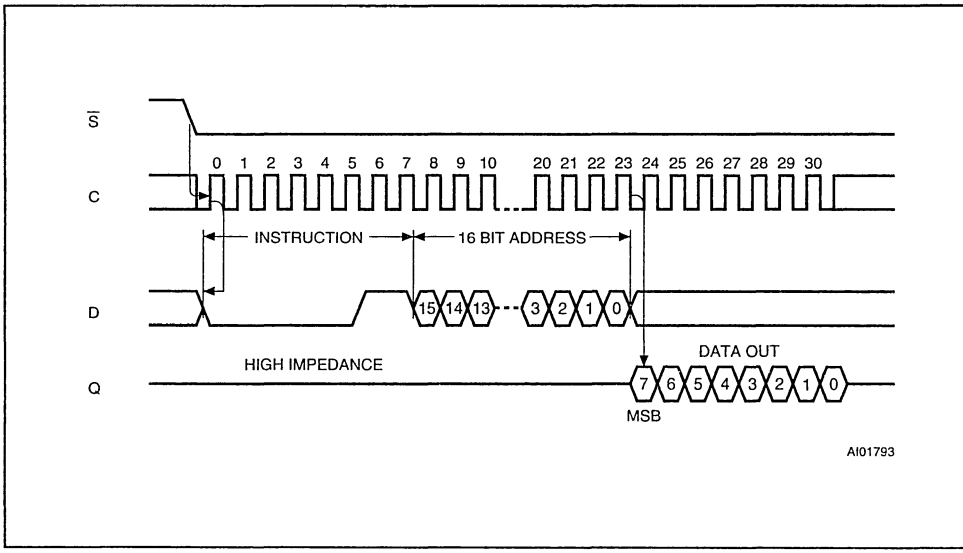
Note: Address bits up to A15 not specified are don't care.

Figure 5. Block Diagram



Note: An is the top address of the memory

Figure 6. Read EEPROM Array Operation Sequence



Note: Depending on the memory size, most significant address bits are don't care.

Table 6. Write Protected Block Size

Status Register Bits		Protected Block	Array Addresses Protected			
BP1	BP0		M95080	M95160	M95320	M95640
0	0	none	none	none	none	none
0	1	Upper quarter	0300h - 03FFh	0600h - 07FFh	0C00h - 0FFFh	1800h - 1FFFh
1	0	Upper half	0200h - 03FFh	0400h - 07FFh	0800h - 0FFFh	1000h - 1FFFh
1	1	Whole Memory	0000h - 03FFh	0000h - 07FFh	0000h - 0FFFh	0000h - 1FFFh

Write Status Register (WRSR)

When the WRSR instruction and the 8 bits of the Status Register are latched-in, the internal write cycle is then triggered by the rising edge of $\overline{S}$. This rising edge of $\overline{S}$ must appear just before the rising edge of the 17 th clock pulse (see Serial input timing Figure 14), otherwise the internal write sequence is not performed.

The WRSR instruction allows the user:

1. to select the size of the memory to be protected,
2. to choose the protection level between the SPM (Software Protected Mode) and the HPM (Hardware Protected Mode).

Size Selection. The way to select the size of the EEPROM area to be protected is common to both SPM and HPM. BP1 and BP0 bits (initial delivery states = 00; that is size = 0) of the Status Register have to be written once the data to be protected are stored in the EEPROM. The Table 6 summarizes the size selection functions of the memory.

Figure 7. Write Enable Latch Sequence

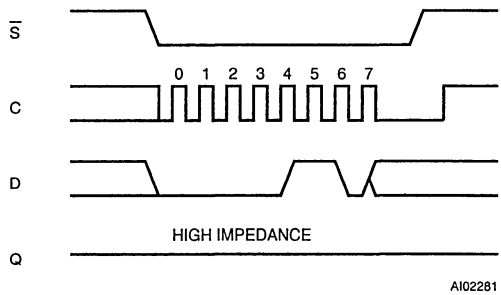
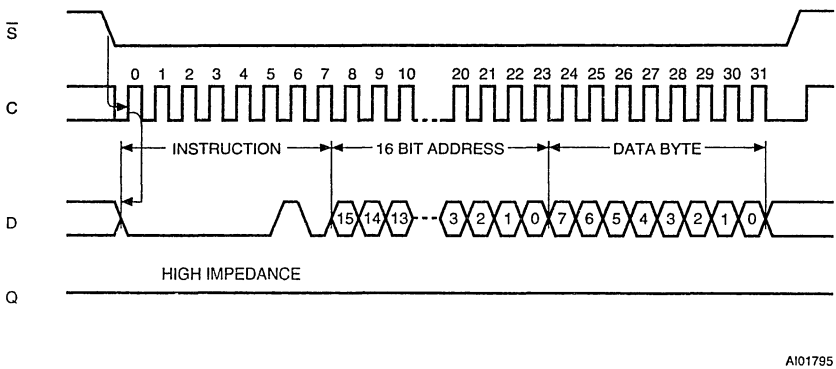
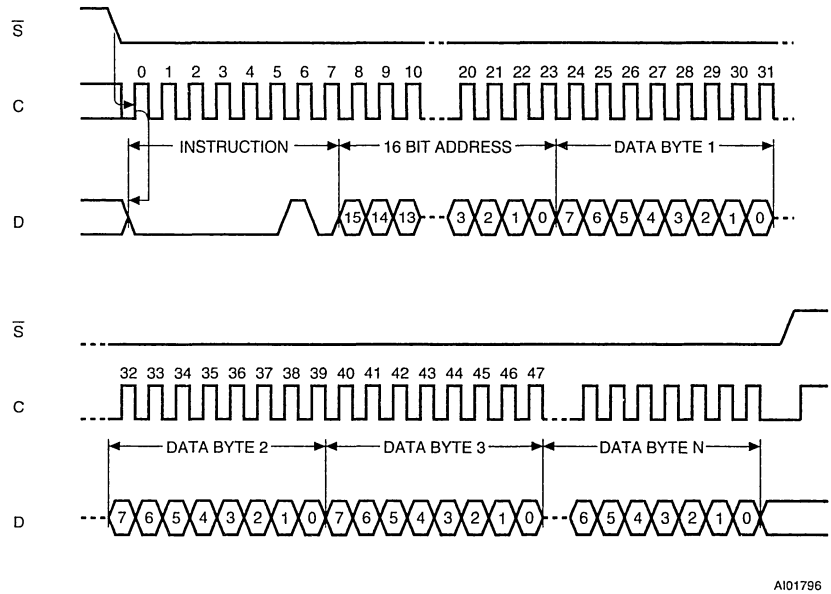


Figure 8. Byte Write Operation Sequence



Note: Depending on the memory size, most significant address bits are don't care.

Figure 9. Page Write Operation Sequence



Note: Depending on the memory size, most significant address bits are don't care

Figure 10. RDSR: Read Status Register Sequence

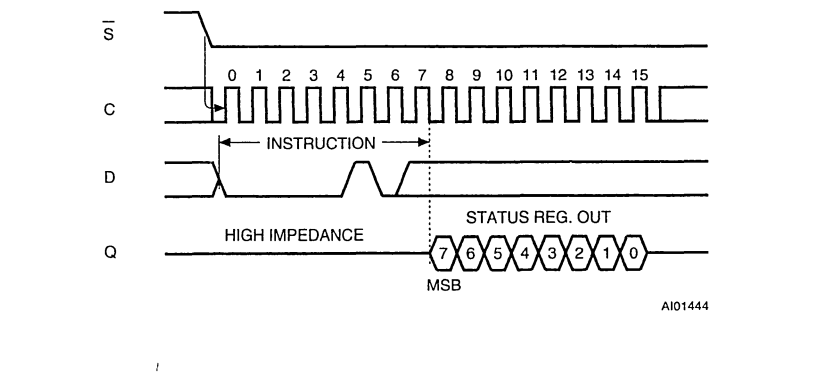
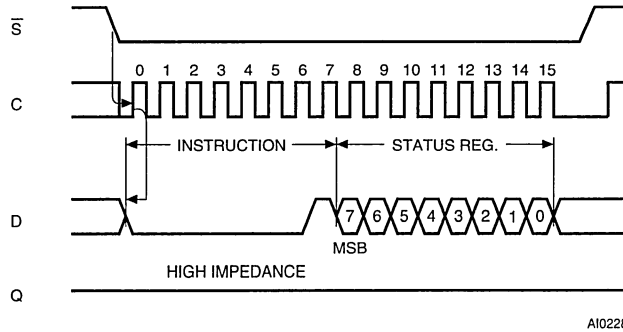


Figure 11. WRSR: Write Status Register Sequence



Selection of the Protection Level

- Once BP0 and BP1 bits are written; **the Software Protected Mode (SPM) is entered.** This means that any attempt to write a byte or a page in the protected area will be ignored even if the Write Enable Latch was set before the write instruction. In this Software Protected Mode; BP0 and BP1 bits can be rewritten with the WSR instruction after having set the WEL.
- If a higher level of protection is needed; **the Hardware Protected Mode (HPM)** can be selected. It is possible to enter the HPM by setting SRWD bit after pulling down the $\overline{W}$ pin or by pulling down the $\overline{W}$ pin after setting SRWD. In both cases, the SRWD is set by using the WSR instruction after having set the WEL bit. It should also be noted that the SRWD can be set after writing BP0 and BP1 or at the same time.
- Once the HPM is entered, the content of the Status Register and all data bytes in the protected area are Hardware Protected against write attempts. The only way to write again the status register is to abort the HPM by pulling high the $\overline{W}$ pin. Aborting the HPM will put the device in the SPM with BP0 and BP1 bits unchanged.

Note: See also the Write Protect pin ($\overline{W}$) description on page 3).

Typical Applications

- The $\overline{W}$ pin can be dynamically driven by an output port of a microcontroller but can also be connected directly or through a pull-down resistor to V_{SS}.
- With such a PCB (Printed Circuit Board):

  a) the memory in the initial delivery state can be soldered directly. After power on, the microcontroller can write data to be protected in the memory. Then write BP0, BP1 and set the SRWD to enter the HPM.

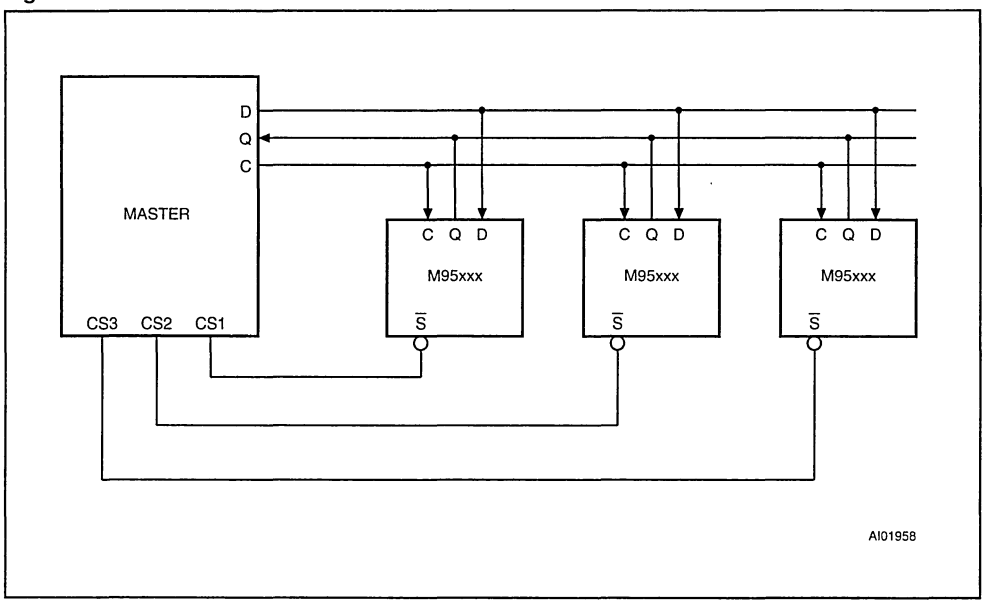
  b) data to be protected, BP0, BP1 can be written and SRWD can be set before soldering the memory. As a consequence, once soldered, the memory is immediately placed in the HPM.

  In these two cases, the only way to abort the HPM will be to remove the memory from the PCB or to apply V_{CC} on the $\overline{W}$ pin through an external equipment when a pull-down resistor is inserted between the pin and V_{SS}.

Read Operation

The chip is first selected by putting $\overline{S}$ low. The serial one byte read instruction is followed by a two bytes address (A15-A0), each bit being latched-in during the rising edge of the clock (C).

Figure 12. EEPROM and SPI Bus



Then the data stored in the memory at the selected address is shifted out on the Q output pin; each bit being shifted out during the falling edge of the clock (C). The data stored in the memory at the next address can be read in sequence by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to "0h" allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during a write cycle will be rejected and will deselect the chip.

Byte Write Operation

Prior to any write attempt, the write enable latch must be set by issuing the WREN instruction. First the device is selected ($\overline{S}$ = low) and a serial WREN instruction byte is issued. Then the product is deselected by taking $\overline{S}$ high. After the WREN instruction byte is sent, the memory will set the write enable latch and then remain in standby until it is deselected. Then the write state is entered by selecting the chip, issuing three bytes of instruction and address, and one byte of data.

Chip Select ($\overline{S}$) must remain low for the entire duration of the operation. The product must be deselected just after the eighth bit of data has been latched in. If not, the write process is cancelled. As soon as the product is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read to check BP1, BP0, WEL and WIP. WIP is high during the self-timed write cycle. When the cycle is completed, the write enable latch is reset.

Page Write Operation

A maximum of 32 bytes of data may be written during one non-volatile write cycle. All 32 bytes must reside on the same page. The page write mode is the same as the byte write mode except that instead of deselecting the device after the first byte of data, up to 31 additional bytes can be shifted in prior to deselecting the chip. Any address of the memory can be chosen as the first address to be written. If the address counter reaches the end of the page (xxxx xxx1 1111) and the clock continues, the counter will roll over to the first address of the page (xxxx xxx0 0000) and overwrite any previously written data. The programming cycle will only start if the $\overline{S}$ transition occurs just after the eighth bit of data of a word is received.

POWER ON STATE

After a Power up the memory is in the following state:

- The device is in the low power standby state.
- The chip is deselected.
- The chip is not in hold condition.
- The write enable latch is reset.
- b7 to b2 bits of the status register are unchanged (non-volatile bits).

DATA PROTECTION AND PROTOCOL SAFETY

- Non valid $\overline{S}$ and $\overline{HOLD}$ transitions are not taken into account.
- $\overline{S}$ must come high at the proper clock count in order to start a non-volatile write cycle (in the memory array or in the status register), that is the Chip Select $\overline{S}$ must rise during the clock pulse following the introduction of a multiple of 8 bits.
- Access to the memory array during non-volatile programming cycle is ignored; however, the programming cycle continues.
- After any of the operations WREN, WRDI, RDSR is completed, the chip enters a wait state and waits for a deselect.
- The write enable latch is reset upon power-up.

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state (all data set at all "1's" or FFh). The Status Register Bits are initialized to 00.

Status Register:

b7							b0
0	0	0	0	0	0	0	0

Table 7. Input Parameters (1) (T_A = 25 °C, f = 5 MHz)

Symbol	Parameter	Min	Max	Unit
C_{OUT}	Output Capacitance (Q)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF

Note: 1. Sampled only, not 100% tested.

Table 8. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$
Output Load	C_L = 100pF

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 13. AC Testing Input Output

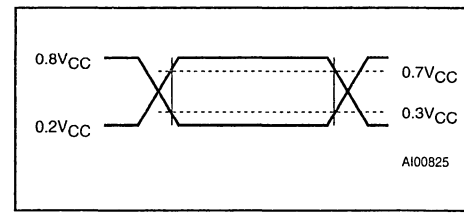


Table 9. DC Characteristics
(T_A = 0 to 70°C; –40 to 85°C or –40 to125°C; V_{CC} = 4.5V to 5.5V)
(T_A = 0 to 70°C; –40 to 85°C; V_{CC} = 2.7V to 5.5V)
(T_A = 0 to 70°C; –40 to 85°C; V_{CC} = 2.5V to 5.5V)
(T_A = 0 to 70°C; –20 to 85°C; V_{CC} = 1.8V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			±2	µA
I_{LO}	Output Leakage Current			±2	µA
I_{CC}	Supply Current	C = 0.1 V_{CC}/0.9 V_{CC}, at 5 MHz, V_{CC} = 5V, Q = Open		4	mA
		C = 0.1 V_{CC}/0.9 V_{CC}, at 2 MHz, V_{CC} = 5V, Q = Open, Note 2		4	mA
	Supply Current (V series)	C = 0.1 V_{CC}/0.9 V_{CC}, at 5 MHz, V_{CC} = 2.7V, Q = Open		3	mA
	Supply Current (W series)	C = 0.1 V_{CC}/0.9 V_{CC}, at 2 MHz, V_{CC} = 2.5V, Q = Open		2	mA
	Supply Current (R series)	C = 0.1 V_{CC}/0.9 V_{CC}, at 1 MHz, V_{CC} = 1.8V, Q = Open		2	mA
I_{CC1}	Standby Current	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V		10	µA
		$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V, Note 2		10	µA
	Standby Current (V series)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.7V		2	µA
	Standby Current (W series)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V		2	µA
	Standby Current (R series)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 1.8V		1	µA
V_{IL}	Input Low Voltage		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{OL} (1)	Output Low Voltage	I_{OL} = 2mA, V_{CC} = 5V		0.4	V
		I_{OL} = 2mA, V_{CC} = 5V, Note 2		0.4	V
	Output Low Voltage (V series)	I_{OL} = 1.5mA, V_{CC} = 2.7V		0.4	V
	Output Low Voltage (W series)	I_{OL} = 1.5mA, V_{CC} = 2.5V		0.4	V
	Output Low Voltage (R series)	I_{OL} = 0.15mA, V_{CC} = 1.8V		0.3	V
V_{OH} (1)	Output High Voltage	I_{OH} = –2mA, V_{CC} = 5V	0.8 V_{CC}		V
		I_{OH} = –2mA, V_{CC} = 5V, Note 2	0.8 V_{CC}		V
	Output High Voltage (V series)	I_{OH} = –0.4mA, V_{CC} = 2.7V	0.8 V_{CC}		V
	Output High Voltage (W series)	I_{OH} = –0.4mA, V_{CC} = 2.5V	0.8 V_{CC}		V
	Output High Voltage (R series)	I_{OH} = –0.1mA, V_{CC} = 1.8V	0.8 V_{CC}		V

Notes: 1. The device meets output requirements for both TTL and CMOS standards.
2. Test performed at –40 to 125°C temperature range, grade 3

Table 10A. AC Characteristics

Symbol	Alt	Parameter	M95640 / 320 / 160 / 080				Unit
			V_{CC} = 4.5V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		V_{CC} = 4.5V to 5.5V, T_A = –40 to 125°C		
			Min	Max	Min	Max	
f_C	f_C	Clock Frequency	D.C.	5	D.C.	2	MHz
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time	90		200		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	90		200		ns
t_{CH} (1)	t_{CLH}	Clock High Time	90		200		ns
t_{CL} (1)	t_{CLL}	Clock Low Time	90		200		ns
t_{CLCH} (2)	t_{RC}	Clock Rise Time		1		1	µs
t_{CHCL} (2)	t_{FC}	Clock Fall Time		1		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		40		ns
t_{CHDX}	t_{DH}	Data In Hold Time	30		50		ns
t_{DLDH} (2)	t_{RI}	Data In Rise Time		1		1	µs
t_{DHDL} (2)	t_{FI}	Data In Fall Time		1		1	µs
t_{HHCH}	t_{CD}	$\overline{HOLD}$ Setup Time	70		140		ns
t_{HLCH}	t_{CD}	Clock Low Hold Time	40		90		ns
t_{CLHL}	t_{HD}	$\overline{HOLD}$ Hold Time	0		0		ns
t_{CLHH}	t_{HD}	Clock Low Setup Time	0		0		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	90		200		ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time	90		200		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	100		200		ns
t_{SHQZ} (2)	t_{DIS}	Output Disable Time		100		250	ns
t_{CLQV}	t_V	Clock Low to Output Valid		60		150	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		ns
t_{QLQH} (2)	t_{RO}	Output Rise Time		50		100	ns
t_{QHQL} (2)	t_{FO}	Output Fall Time		50		100	ns
t_{HHQX} (2)	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		50		100	ns
t_{HLQZ} (2)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		100		250	ns
t_W	t_{WP}	Write Cycle Time		10		10	ms

Notes: 1. $t_{CH} + t_{CL} \geq 1/fc$
2. Value guaranteed by characterization, not 100% tested in production.

Table 10B. AC Characteristics

Symbol	Alt	Parameter	M95640 / 320 / 160 / 080						Unit
			V_{CC} = 2.7V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		V_{CC} = 2.5V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		V_{CC} = 1.8V to 3.6V, T_A = 0 to 70°C, T_A = –20 to 85°C		
			Min	Max	Min	Max	Min	Max	
f_C	f_C	Clock Frequency	D.C.	5	D.C.	2	D.C.	1	MHz
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time	90		200		400		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	90		200		400		ns
t_{CH} (1)	t_{CLH}	Clock High Time	90		200		400		ns
t_{CL} (1)	t_{CLL}	Clock Low Time	90		200		400		ns
t_{CLCH} (2)	t_{RC}	Clock Rise Time		1		1		1	µs
t_{CHCL} (2)	t_{FC}	Clock Fall Time		1	.	1		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		40		60		ns
t_{CHDX}	t_{DH}	Data In Hold Time	30		50		100		ns
t_{DLDH} (2)	t_{RI}	Data In Rise Time		1		1		1	µs
t_{DHDL} (2)	t_{FI}	Data In Fall Time		1		1		1	µs
t_{HHCH}	t_{CD}	$\overline{HOLD}$ Setup Time	70		140		350		ns
t_{HLCH}	t_{CD}	Clock Low Hold Time	40		90		200		ns
t_{CLHL}	t_{HD}	$\overline{HOLD}$ Hold Time	0		0		0		ns
t_{CLHH}	t_{HD}	Clock Low Setup Time	0		0		0		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	90		200		400		ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time	90		200		400		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	100		200		300		ns
t_{SHQZ} (2)	t_{DIS}	Output Disable Time		100		250		500	ns
t_{CLQV}	t_V	Clock Low to Output Valid		60		150		380	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		0		ns
t_{QLQH} (2)	t_{RO}	Output Rise Time		50		100		200	ns
t_{QHQL} (2)	t_{FO}	Output Fall Time		50		100		200	ns
t_{HHQX} (2)	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		50		100		250	ns
t_{HLQZ} (2)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		100		250		500	ns
t_W	t_{WP}	Write Cycle Time		10		10		10	ms

Notes: 1. $t_{CH} + t_{CL} \geq 1/fc$
2. Value guaranteed by characterization, not 100% tested in production

Figure 14. Serial Input Timing

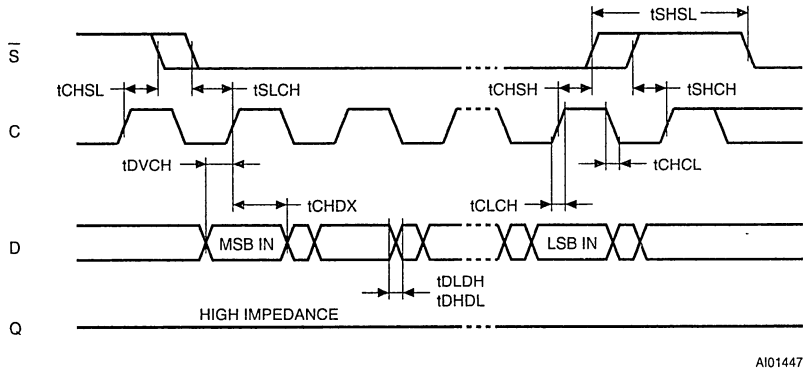


Figure 15. Hold Timing

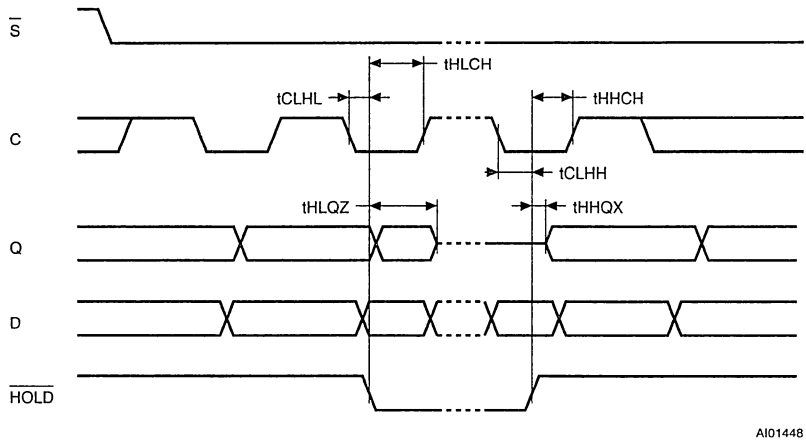
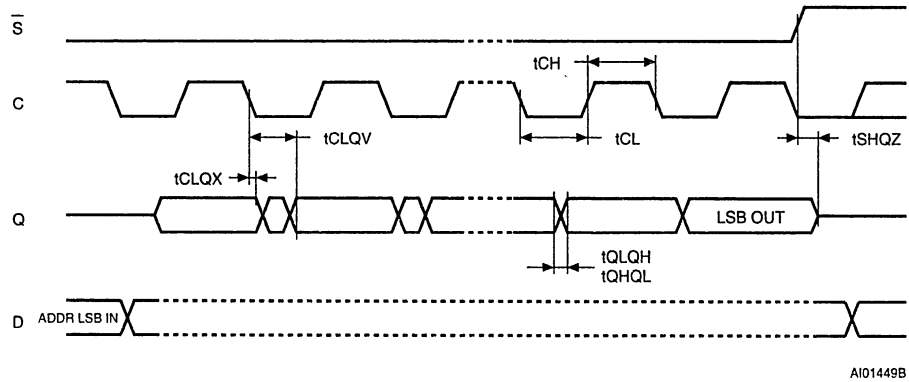
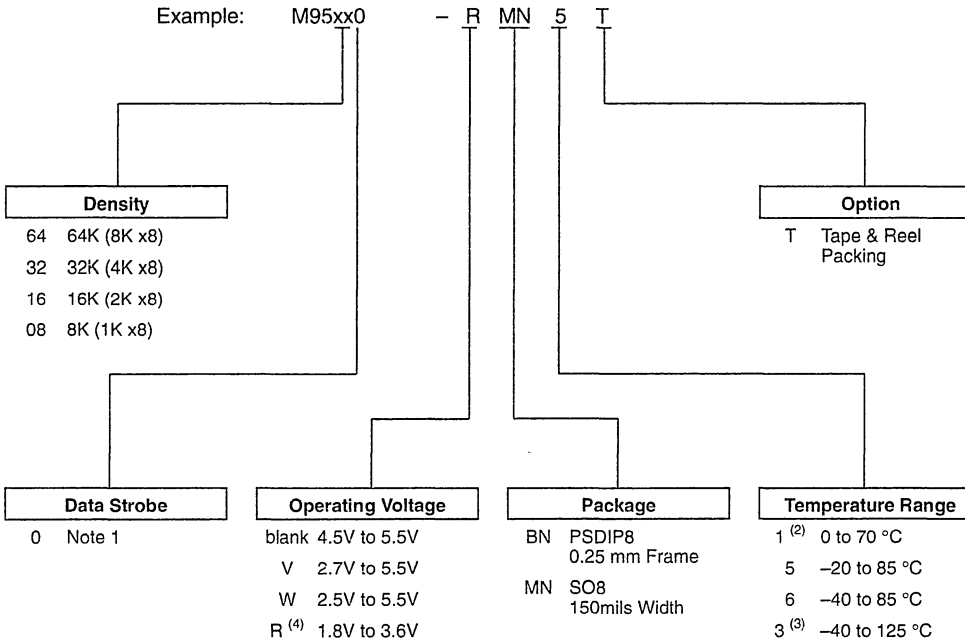


Figure 16. Output Timing



ORDERING INFORMATION SCHEME



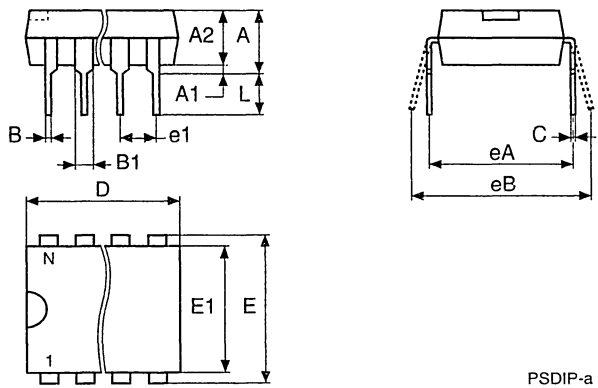
Notes: 1. Data In is strobed on rising edge of the clock (C) and Data Out is synchronized from the falling edge of the clock
2 Temperature range on request only.
3 Produced with High Reliability Certified Flow (HRCF), in V_{CC} range 4.5V to 5.5V only.
4. -R version (1.8V to 3.6V) are only available in temperature ranges 5 or 1

Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		
CP			0.10			0.004

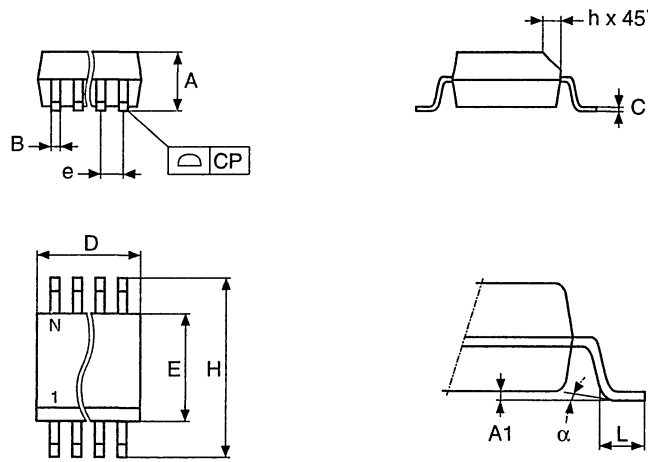


PSDIP-a

Drawing is not to scale.

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004



SO-a

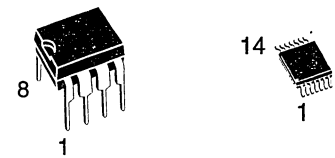
Drawing is not to scale.

M95256
M95128

256/128 Kbit Serial SPI EEPROM with High Speed Clock and Positive Clock Strobe

PRELIMINARY DATA

- 100,000 ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  - 4.5V to 5.5V for M95xxx
  - 2.5V to 5.5V for M95xxx-W
  - 1.8V to 3.6V for M95xxx-R
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 5 MHz CLOCK RATE MAX
- STATUS REGISTER
- HARDWARE PROTECTION of the STATUS REGISTER
- 64 BYTE PAGE MODE
- SIZEABLE READ ONLY EEPROM AREA
- SELF-TIMED PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- SUPPORTS POSITIVE CLOCK SPI MODES



PSDIP8 (BN)
0.25mm Frame

TSSOP14 (DL)
169mil Width

SO8 (MN)
150mil Width

SO8 (MW)
200mil Width

DESCRIPTION

The M95xxx is a family of Electrically Erasable Programmable Memories (EEPROM) fabricated with STMicroelectronics's High Endurance Double Polysilicon CMOS technology. Each Memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q).

The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$).

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

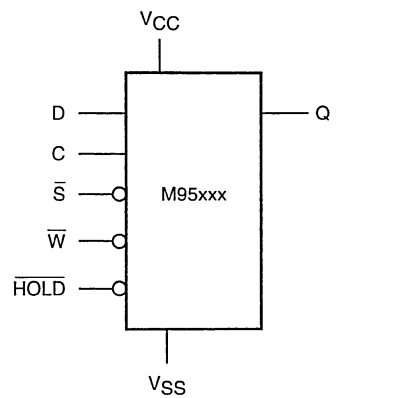


Figure 2A. DIP Pin Connections

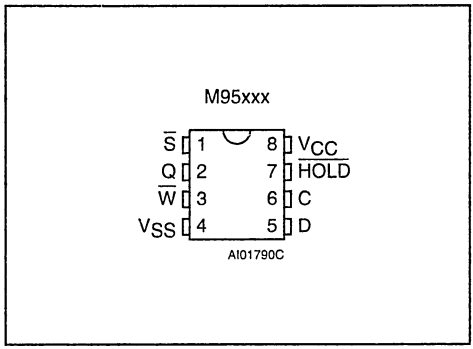


Figure 2B. SO Pin Connections

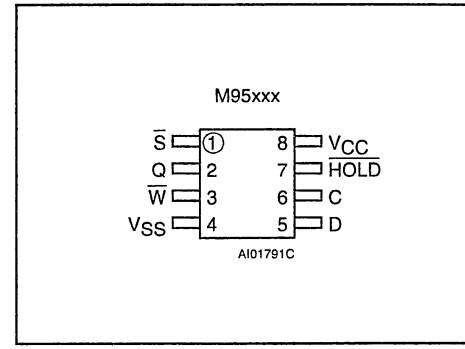
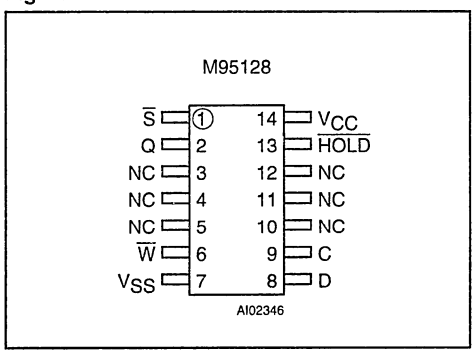


Figure 2C. TSSOP Pin Connections



DESCRIPTION (cont'd)

Data is clocked in during the low to high transition of clock C, data is clocked out during the high to low transition of clock C.

SIGNALS DESCRIPTION

Serial Output (Q). The output pin is used to transfer data serially out of the Memory. Data is shifted out on the falling edge of the serial clock.

Serial Input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Input is latched on the rising edge of the serial clock.

Table 2. Absolute Maximum Ratings (1)

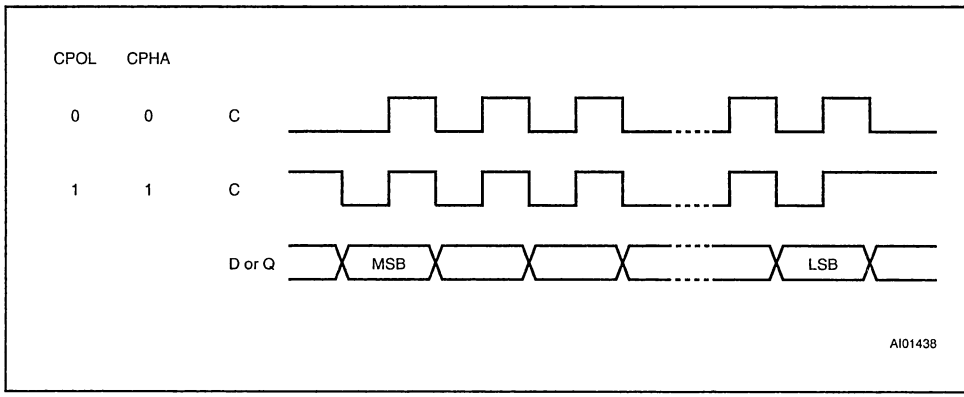
Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature:			–40 to 125	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to V_{CC} +0.6	V
V_I	Input Voltage with respect to Ground			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			400	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents

2. MIL-STD-883C, 3015.7 (100pF, 1500Ω)

3 EIAJ IC-121 (Condition C) (200pF, 0Ω)

Figure 3. Data and Clock Timing



Serial Clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched on the rising edge of the clock input, while data on the Q pin changes after the falling edge of the clock input.

Chip Select ($\overline{S}$). When $\overline{S}$ is high, the Memory is deselected and the Q output pin is at high impedance and, unless an internal write operation is underway the Memory will be in the standby power mode. $\overline{S}$ low enables the Memory, placing it in the active power mode. It should be noted that after power-on, a high to low transition on $\overline{S}$ is required prior to the start of any operation.

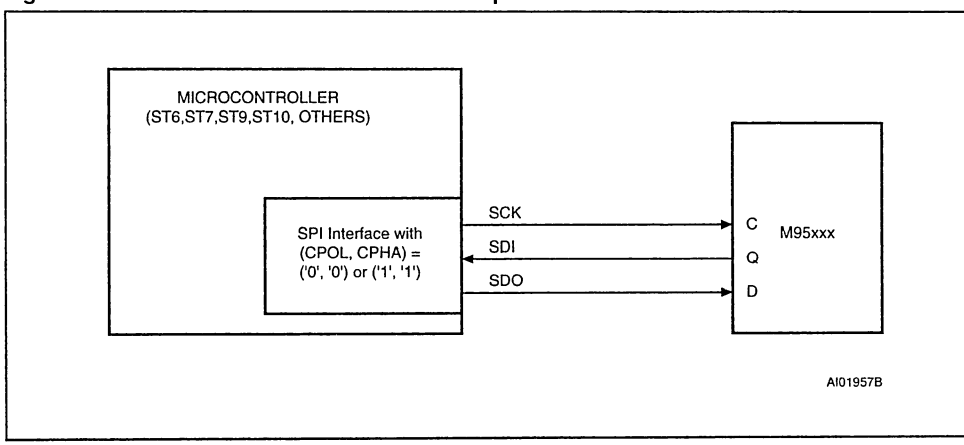
Write Protect ($\overline{W}$). This pin is for hardware write protection of the status register (SR); except WIP and WEL bits. When bit 7 (SRWD) of the status register is 0 (the initial delivery state); it is possible to write the SR once the WEL (Write Enable Latch) has been set and whatever is the status of pin $\overline{W}$ (high or low).

Note: SRWD stands for; Status Register Write Disable.

Once bit 7 (SRWD) of the status register has been set to 1; the possibility to rewrite the SR depends on the logical level present at pin $\overline{W}$:

– If $\overline{W}$ pin is high; it will be possible to rewrite the status register after having set the WEL (Write Enable Latch).

Figure 4. Microcontroller and SPI Interface Set-up



SIGNAL DESCRIPTION (cont'd)

– If $\overline{W}$ pin is low; any attempt to modify the status register will be ignored by the device even if the WEL was set. As a consequence: all the data bytes in the EEPROM area protected by the BPn bits of the status register are also hardware protected against data corruption and can be seen as a Read Only EEPROM area from the microcontroller. This mode is called the Hardware Protected Mode (HPM).

It is possible to enter the Hardware Protected Mode (HPM) by setting SRWD bit after pulling down the $\overline{W}$ pin or by pulling down the $\overline{W}$ pin after setting SRWD bit.

The only way to abort the Hardware Protected Mode once entered is to pull high the $\overline{W}$ pin.

If $\overline{W}$ pin is permanently tied to high level; the Hardware Protected Mode will never be activated and the Memory will only allow the user to software protect a part of the memory with the BPn bits of the status register. All protection features of the device are summarized in Table 3.

Hold ($\overline{HOLD}$). The $\overline{HOLD}$ pin pin is used to pause serial communications with an SPI Memory without resetting the serial sequence. To take the Hold condition into account, the product must be selected ($\overline{S}$ = 0). The Hold condition is entered by a 0 state on the $\overline{HOLD}$ pin when a 0 state is present on the CLOCK pin (see Figure 5). During the Hold condition, the Q output pin is put at high impedance and the input pins (D, C) are ignored by the memory.

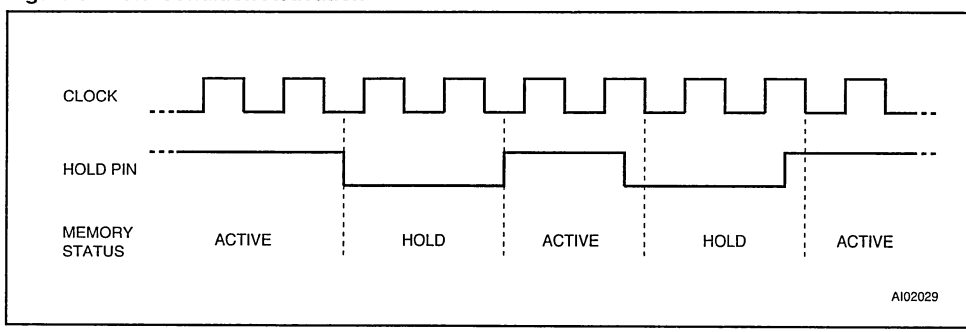
It is possible to deselect the device when it is under the Hold condition. The protocol is then reset. The memory remains on Hold as long as the $\overline{HOLD}$ pin is low. To restart communication with the device, it is necessary to both remove the Hold ($\overline{HOLD}$=1) and to SELECT the memory.

Table 3. Protection Feature

$\overline{W}$	SRWD	Status Register (SR)	Data Bytes (Protected Area)	Mode	Data Bytes (Unprotected Area)
X	0	Writable after setting WEL	Software Write protected by the BPn bits of the Status Register	SPM	Writable after setting WEL
1	1	Writable after setting WEL	Software Write protected by the BPn bits of the Status Register	SPM	Writable after setting WEL
0	1	Hardware Write protected	Hardware Write protected	HPM	Writable after setting WEL

Notes: 1. SPM stands for Software Protected Mode.
2. BPn are BP0 to BP1 bits of the Status Register.
3. SPM and HPM are also described in the Write Status Register (WRSR) section.

Figure 5. Hold Condition Activation



OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first rising edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 4 shows the instruction set and format for device operation. If an invalid instruction is sent (one not contained in Table 4), the chip is automatically deselected.

Write Enable (WREN) and Write Disable (WRDI)

The Memory contains a write enable latch. This latch must be set prior to every WRITE, WRSR operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under the following conditions:

- Power on,
- WRDI instruction completion,
- WRSR instruction completion,
- WRITE instruction completion.

As soon as the WREN or WRDI instruction is received, the circuit executes the instruction and enters a wait mode until it is deselected.

Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write to the memory operation. When a write is in progress, it is recommended to check the WIP bit before sending a new WRITE command. For this, it is possible to continuously read the Status Register value as shown in Figure 11. The status register format is as follows:

b7							b0
SRWD	X	X	X	BP1	BP0	WEL	WIP

BP0, BP1: Read and write bits
WEL, WIP: Read only bits.
SRWD: Read and Write bit.

During a write operation to the device (memory area or Status Register), all bits of the Status Register are valid and can be read with the RDSR instruction. However, it should be noted that the values of the Non Volatile bits (SRWD, BP0, BP1) read at that time correspond to the previous content of the Status Register. The updated value of these bits will be accessible through a new RDSR instruction performed after completion of the Write Cycle. As the 2 Read Only bits (WEL, WIP) are dynamically updated during internal write cycles, it is possible to continuously get their updated values as shown in Figure 11.

The Write-In-Process (WIP) read-only bit indicates whether the Memory is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress.

The Write Enable Latch (WEL) read-only bit indicates the status of the write enable latch. When set to a '1' the latch is set, when set to a '0' the latch is reset. The Block Protect (BP0 and BP1) bits indicate the extent of the protection employed. These 2 bits are non volatile and are set by the user issuing a WRSR instruction.

Table 4. Instruction Set

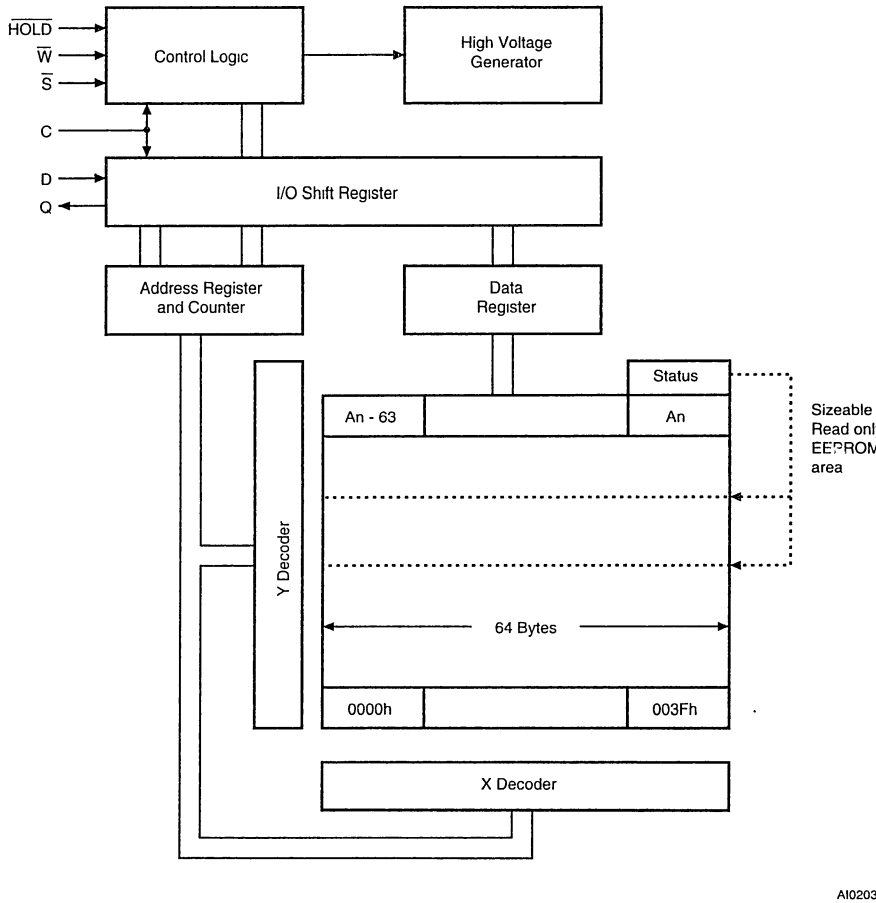
Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	0000 0110
WRDI	Reset Write Enable Latch	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read Data from Memory Array	0000 0011
WRITE	Write Data to Memory Array	0000 0010

Table 5. Address Range Bits

Device	M95128	M95256
Address Bit	A0-A13	A0-A14

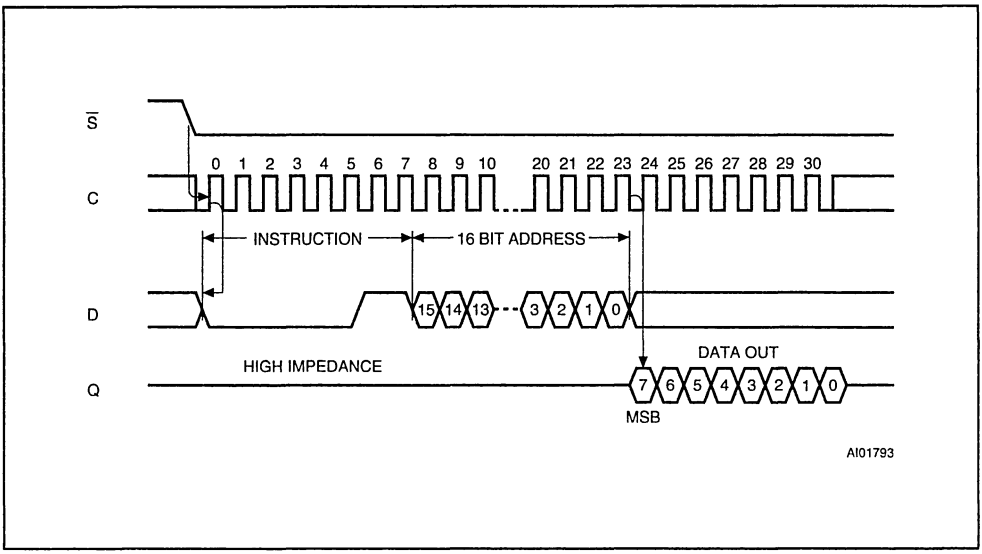
Note: Address bits up to A15 not specified are don't care.

Figure 6. Block Diagram



Note: An is the top address of the memory.

Figure 7. Read EEPROM Array Operation Sequence



Note: Depending on the memory size, most significant address bits are don't care.

Table 6. Write Protected Block Size

Status Register Bits		Protected Block	Array Addresses Protected	
BP1	BP0		M95128	M95256
0	0	none	none	none
0	1	Upper quarter	3000h - 3FFFh	6000h - 7FFFh
1	0	Upper half	2000h - 3FFFh	4000h - 7FFFh
1	1	Whole Memory	0000h - 3FFFh	0000h - 7FFFh

Write Status Register (WRSR)

When the WRSR instruction and the 8 bits of the Status Register are latched-in, the internal write cycle is then triggered by the rising edge of S. This rising edge of S must appear just before the rising edge of the 17 th clock pulse (see Serial input timing Figure 15), otherwise the internal write sequence is not performed.

The WRSR instruction allows the user:

1. to select the size of the memory to be protected,
2. to choose the protection level between the SPM (Software Protected Mode) and the HPM (Hardware Protected Mode).

Size Selection. The way to select the size of the EEPROM area to be protected is common to both SPM and HPM. BP1 and BP0 bits (initial delivery states = 00; that is size = 0) of the Status Register have to be written once the data to be protected are stored in the EEPROM. The Table 6 summarizes the size selection functions of the memory.

Figure 8. Write Enable Latch Sequence

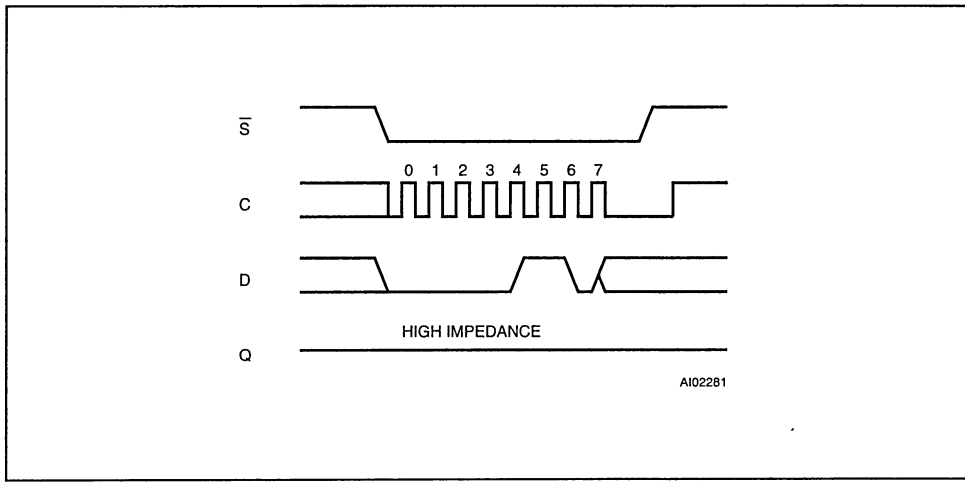
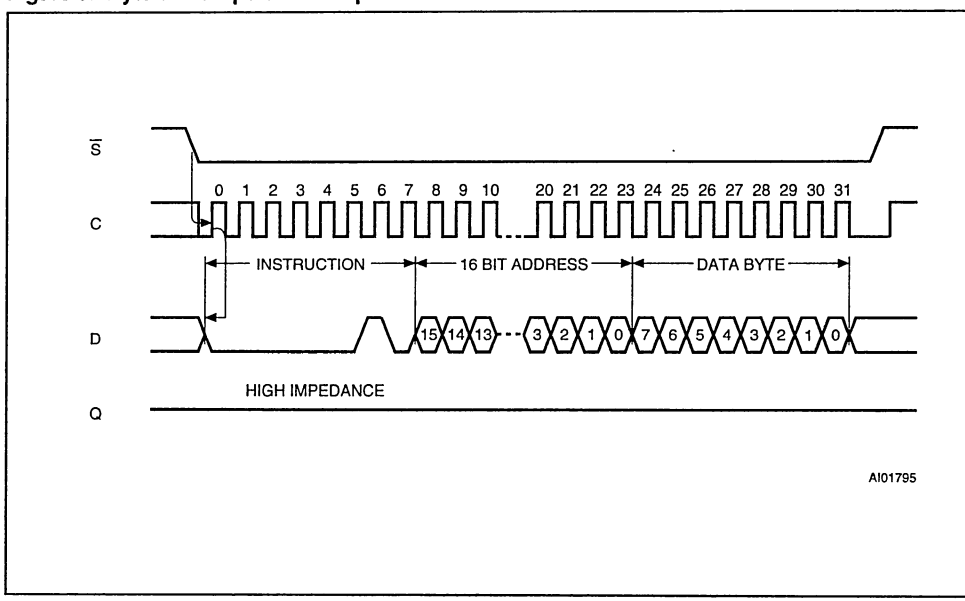
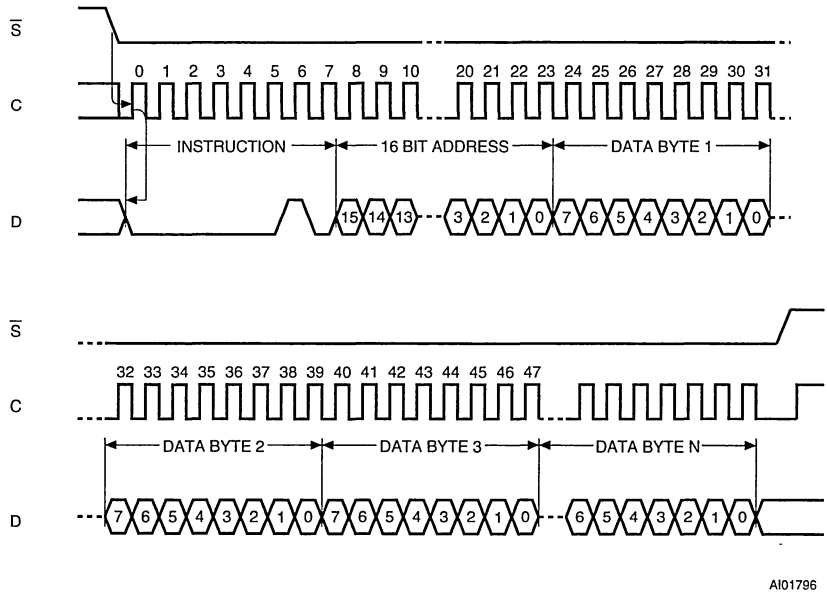


Figure 9. Byte Write Operation Sequence



Note: Depending on the memory size, most significant address bits are don't care.

Figure 10. Page Write Operation Sequence



Note: Depending on the memory size, most significant address bits are don't care.

Figure 11. RDSR: Read Status Register Sequence

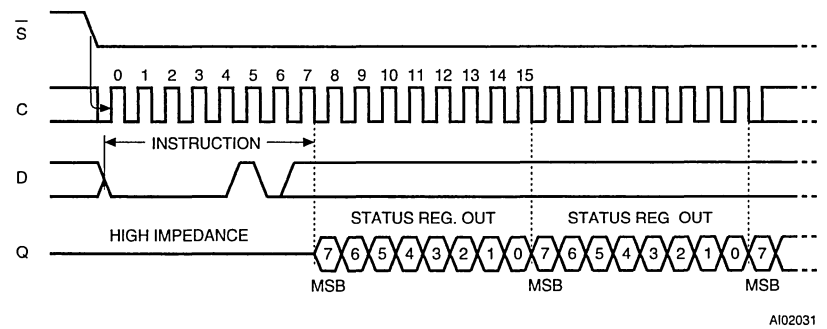
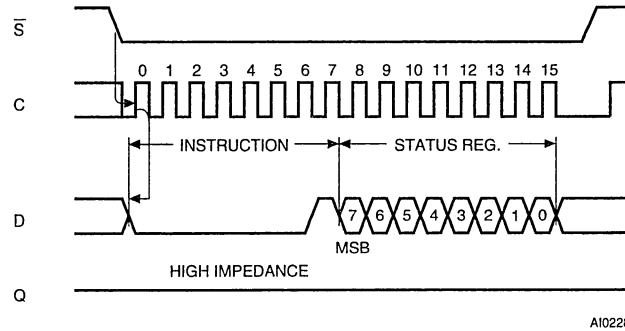


Figure 12. WRSR: Write Status Register Sequence



Selection of the Protection Level

- Once BP0 and BP1 bits are written; **the Software Protected Mode (SPM) is entered.** This means that any attempt to write a byte or a page in the protected area will be ignored even if the Write Enable Latch was set before the write instruction. In this Software Protected Mode; BP0 and BP1 bits can be rewritten with the WSR instruction after having set the WEL.
- If a higher level of protection is needed; **the Hardware Protected Mode (HPM)** can be selected. It is possible to enter the HPM by setting SRWD bit after pulling down the $\overline{W}$ pin or by pulling down the $\overline{W}$ pin after setting SRWD. In both cases, the SRWD is set by using the WSR instruction after having set the WEL bit. It should also be noted that the SRWD can be set after writing BP0 and BP1 or at the same time.
- Once the HPM is entered, the content of the Status Register and all data bytes in the protected area are Hardware Protected against write attempts. The only way to write again the status register is to abort the HPM by pulling high the $\overline{W}$ pin. Aborting the HPM will put the device in the SPM with BP0 and BP1 bits unchanged.

Note: See also the Write Protect pin ($\overline{W}$) description on page 3).

Typical Applications

- The $\overline{W}$ pin can be dynamically driven by an output port of a microcontroller but can also be connected directly or through a pull-down resistor to V_{SS}.
- With such a PCB (Printed Circuit Board):

  a) the memory in the initial delivery state can be soldered directly. After power on, the microcontroller can write data to be protected in the memory. Then write BP0, BP1 and set the SRWD to enter the HPM.

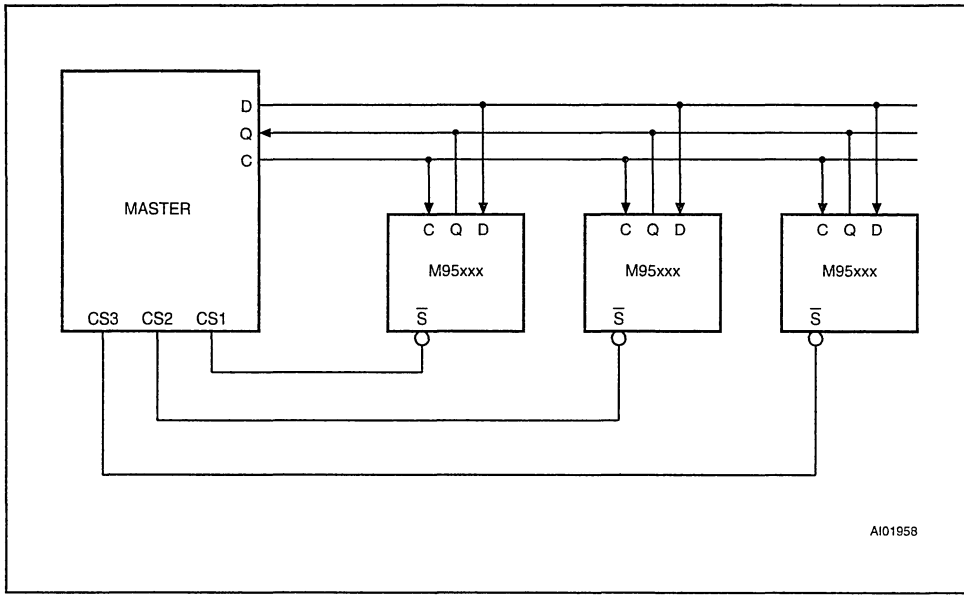
  b) data to be protected, BP0, BP1 can be written and SRWD can be set before soldering the memory. As a consequence, once soldered, the memory is immediately placed in the HPM.

  In these two cases, the only way to abort the HPM will be to remove the memory from the PCB or to apply V_{CC} on the $\overline{W}$ pin through an external equipment when a pull-down resistor is inserted between the pin and V_{SS}.

Read Operation

The chip is first selected by putting $\overline{S}$ low. The serial one byte read instruction is followed by a two bytes address (A15-A0), each bit being latched-in during the rising edge of the clock (C).

Figure 13. EEPROM and SPI Bus



Then the data stored in the memory at the selected address is shifted out on the Q output pin; each bit being shifted out during the falling edge of the clock (C). The data stored in the memory at the next address can be read in sequence by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to "0h" allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during a write cycle will be rejected and will deselect the chip.

Byte Write Operation

Prior to any write attempt, the write enable latch must be set by issuing the WREN instruction. First the device is selected ($\overline{S}$ = low) and a serial WREN instruction byte is issued. Then the product is deselected by taking $\overline{S}$ high. After the WREN instruction byte is sent, the Memory will set the write enable latch and then remain in standby until it is deselected. Then the write state is entered by selecting the chip, issuing three bytes of instruction and address, and one byte of data.

Chip Select ($\overline{S}$) must remain low for the entire duration of the operation. The product must be deselected just after the eighth bit of data has been latched in. If not, the write process is cancelled. As soon as the product is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read to check BP1, BP0, WEL and WIP. WIP is high during the self-timed write cycle. When the cycle is completed, the write enable latch is reset.

Page Write Operation

A maximum of 64 bytes of data may be written during one non-volatile write cycle. All 64 bytes must reside on the same page. The page write mode is the same as the byte write mode except that instead of deselecting the device after the first byte of data, up to 63 additional bytes can be shifted in prior to deselecting the chip. Any address of the memory can be chosen as the first address to be written. If the address counter reaches the end of the page (xxxx xx11 1111) and the clock continues, the counter will roll over to the first address of the page (xxxx xx00 0000) and overwrite any previously written data. The programming cycle will only start if the $\overline{S}$ transition occurs just after the eighth bit of data of a word is received.

POWER ON STATE

After a Power up the Memory is in the following state:

- The device is in the low power standby state.
- The chip is deselected.
- The chip is not in hold condition.
- The write enable latch is reset.
- b7 to b2 bits of the status register are unchanged (non-volatile bits).

DATA PROTECTION AND PROTOCOL SAFETY

- Non valid $\overline{S}$ and $\overline{HOLD}$ transitions are not taken into account.
- S must come high at the proper clock count in order to start a non-volatile write cycle (in the memory array or in the status register), that is the Chip Select $\overline{S}$ must rise during the clock pulse following the introduction of a multiple of 8 bits.
- Access to the memory array during non-volatile programming cycle is ignored; however, the programming cycle continues.
- After any of the operations WREN, WRDI, RDSR is completed, the chip enters a wait state and waits for a deselect.
- The write enable latch is reset upon power-up.

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state (all data set at all "1's" or FFh). The Status Register Bits are initialized to 00.

Status Register:

b7							b0
0	0	0	0	0	0	0	0

Table 7. Input Parameters (1) (T_A = 25 °C, f = 5 MHz)

Symbol	Parameter	Min	Max	Unit
C_{OUT}	Output Capacitance (Q)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF

Note: 1. Sampled only, not 100% tested.

Table 8. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$
Output Load	C_L = 100pF

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 14. AC Testing Input Output

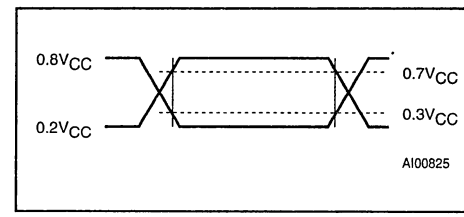


Table 9. DC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 4.5V to 5.5V)
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.5V to 5.5V)
(T_A = 0 to 70°C or –20 to 85°C; V_{CC} = 1.8V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			±2	µA
I_{LO}	Output Leakage Current			±2	µA
I_{CC}	Supply Current	C = 0.1 V_{CC}/0.9 V_{CC}, at 5 MHz, V_{CC} = 5V, Q = Open		5	mA
		C = 0.1 V_{CC}/0.9 V_{CC}, at 2 MHz, V_{CC} = 5V, Q = Open, Note 2		5	mA
	Supply Current (W series)	C = 0.1 V_{CC}/0.9 V_{CC}, at 2 MHz, V_{CC} = 2.5V, Q = Open		2	mA
	Supply Current (R series)	C = 0.1 V_{CC}/0.9 V_{CC}, at 1 MHz, V_{CC} = 1.8V, Q = Open		2	mA
I_{CC1}	Standby Current	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V		20	µA
		$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V, Note 2		20	µA
	Standby Current (W series)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V		2	µA
	Standby Current (R series)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 1.8V		2	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{OL} (1)	Output Low Voltage	I_{OL} = 2mA, V_{CC} = 5V		0.4	V
		I_{OL} = 2mA, V_{CC} = 5V, Note 2		0.4	V
	Output Low Voltage (W series)	I_{OL} = 1.5mA, V_{CC} = 2.5V		0.4	V
	Output Low Voltage (R series)	I_{OL} = 0.15mA, V_{CC} = 1.8V		0.3	V
V_{OH} (1)	Output High Voltage	I_{OH} = –2mA, V_{CC} = 5V	0.8 V_{CC}		V
		I_{OH} = –2mA, V_{CC} = 5V, Note 2	0.8 V_{CC}		V
	Output High Voltage (W series)	I_{OH} = –0.4mA, V_{CC} = 2.5V	0.8 V_{CC}		V
	Output High Voltage (R series)	I_{OH} = –0.1mA, V_{CC} = 1.8V	0.8 V_{CC}		V

Notes: 1. The device meets output requirements for both TTL and CMOS standards.
2. Test performed at –40 to 125°C temperature range, grade 3.

Table 10A. AC Characteristics

Symbol	Alt	Parameter	M95256 / M95128				Unit
			V_{CC} = 4.5V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		V_{CC} = 4.5V to 5.5V, T_A = –40 to 125°C		
			Min	Max	Min	Max	
f_C	f_C	Clock Frequency	D.C.	5	D.C.	2	MHz
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time	90		200		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	90		200		ns
t_{CH} (1)	t_{CLH}	Clock High Time	90		200		ns
t_{CL} (1)	t_{CLL}	Clock Low Time	90		200		ns
t_{CLCH} (2)	t_{RC}	Clock Rise Time		1		1	µs
t_{CHCL} (2)	t_{FC}	Clock Fall Time		1		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		40		ns
t_{CHDX}	t_{DH}	Data In Hold Time	30		50		ns
t_{DLDH} (2)	t_{RI}	Data In Rise Time		1		1	µs
t_{DHDL} (2)	t_{FI}	Data In Fall Time		1		1	µs
t_{HHCH}		$\overline{HOLD}$ Setup Time	70		140		ns
t_{HLCH}		Clock Low Hold Time	40		90		ns
t_{CHHL}		HOLD Hold Time after clock is high	60		120		ns
t_{CHHH}		$\overline{HOLD}$ Hold Time after clock is high	60		120		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	90		200		ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time	90		200		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	100		200		ns
t_{SHQZ} (2)	t_{DIS}	Output Disable Time		100		250	ns
t_{CLQV}	t_V	Clock Low to Output Valid		60		150	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		ns
t_{QLQH} (2)	t_{RO}	Output Rise Time		50		100	ns
t_{QHQL} (2)	t_{FO}	Output Fall Time		50		100	ns
t_{HHQX} (2)	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		50		100	ns
t_{HLQZ} (2)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		100		250	ns
t_W	t_{WP}	Write Cycle Time		10		10	ms

Notes: 1. $t_{CH} + t_{CL} \geq 1/f_C$.
2 Value guaranteed by characterization, not 100% tested in production

Table 10B. AC Characteristics

Symbol	Alt	Parameter	M95256 / M95128				Unit
			V_{CC} = 2.5V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		V_{CC} = 1.8V to 3.6V, T_A = 0 to 70°C, T_A = –20 to 85°C		
			Min	Max	Min	Max	
f_C	f_C	Clock Frequency	D.C.	2	D.C.	1	MHz
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time	200		400		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	200		400		ns
t_{CH} (1)	t_{CLH}	Clock High Time	200		400		ns
t_{CL} (1)	t_{CLL}	Clock Low Time	200		400		ns
t_{CLCH} (2)	t_{RC}	Clock Rise Time		1		1	µs
t_{CHCL} (2)	t_{FC}	Clock Fall Time		1		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	40		60		ns
t_{CHDX}	t_{DH}	Data In Hold Time	50		100		ns
t_{DLDH} (2)	t_{RI}	Data In Rise Time		1		1	µs
t_{DHDL} (2)	t_{FI}	Data In Fall Time		1		1	µs
t_{HHCH}		$\overline{HOLD}$ Setup Time	140		350		ns
t_{HLCH}		Clock Low Hold Time	90		200		ns
t_{CHHL}		HOLD Hold Time after Clock is High	120		250		ns
t_{CHHH}		$\overline{HOLD}$ Hold Time after Clock is High	120		250		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	200		400		ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time	200		400		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	200		300		ns
t_{SHQZ} (2)	t_{DIS}	Output Disable Time		250		500	ns
t_{CLQV}	t_V	Clock Low to Output Valid		150		380	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		ns
t_{QLQH} (2)	t_{RO}	Output Rise Time		100		200	ns
t_{QHQL} (2)	t_{FO}	Output Fall Time		100		200	ns
t_{HHQX} (2)	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		100		250	ns
t_{HLQZ} (2)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		250		500	ns
t_W	t_{WP}	Write Cycle Time		10		10	ms

Notes: 1. $t_{CH} + t_{CL} \geq 1/f_C$.
2. Value guaranteed by characterization, not 100% tested in production.

Figure 15. Serial Input Timing

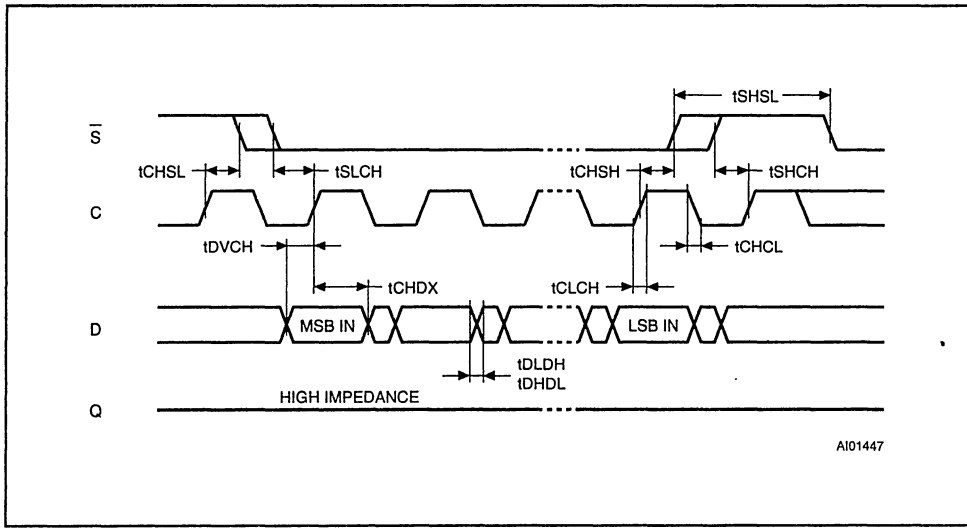


Figure 16. Hold Timing

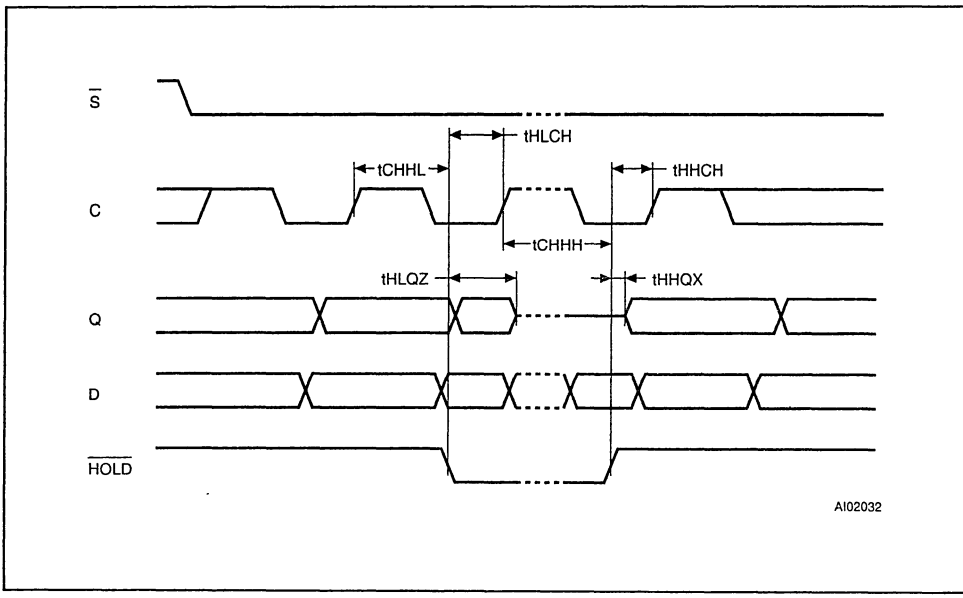
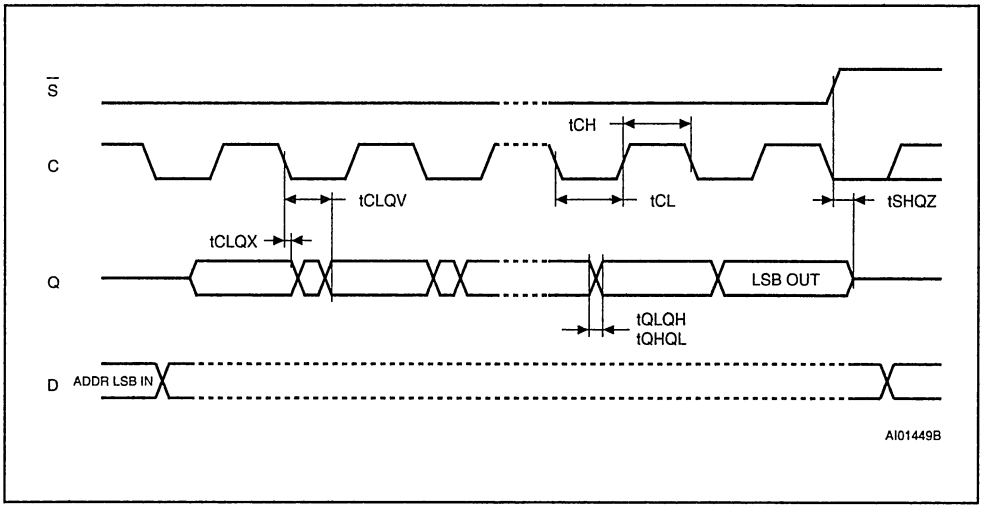
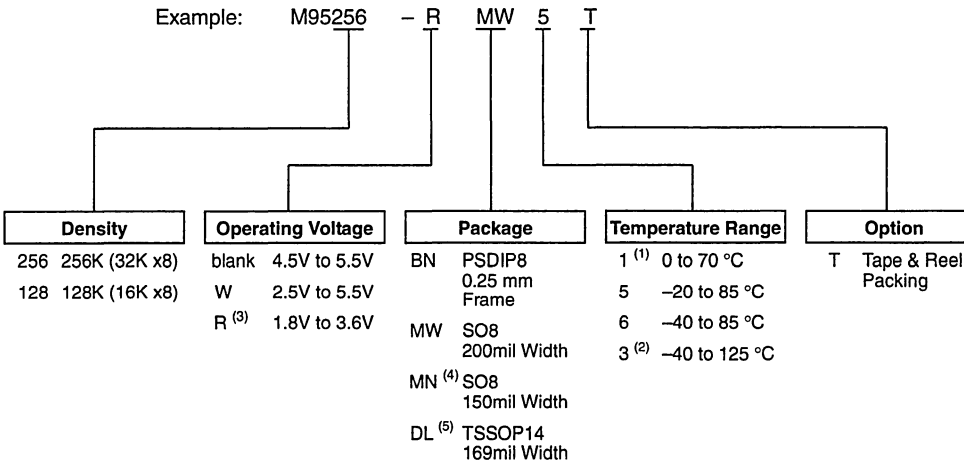


Figure 17. Output Timing



ORDERING INFORMATION SCHEME



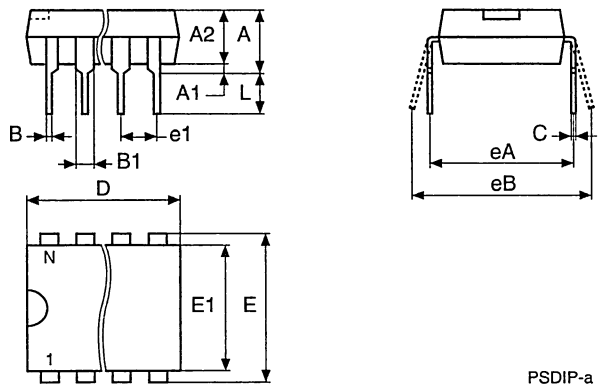
Notes: 1. Temperature range on request only.
2. Produced with High Reliability Certified Flow (HRCF), in V_{CC} range 4.5V to 5.5V only
3. -R version (1.8V to 3.6V) are only available in temperature ranges 5 or 1.
4. SO8, 150mil Width, package is available for M95128 series only
5. TSSOP14, 169mil Width, pakage is available for M95128 series only.

Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		
CP			0.10			0.004

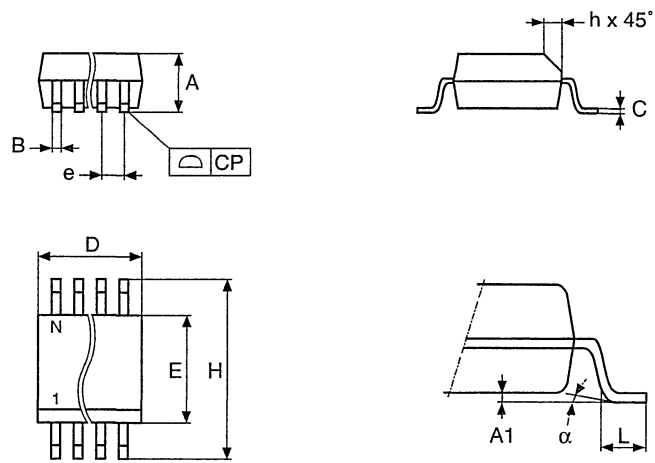


PSDIP-a

Drawing is not to scale.

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8É
N	8			8		
CP			0.10			0.004

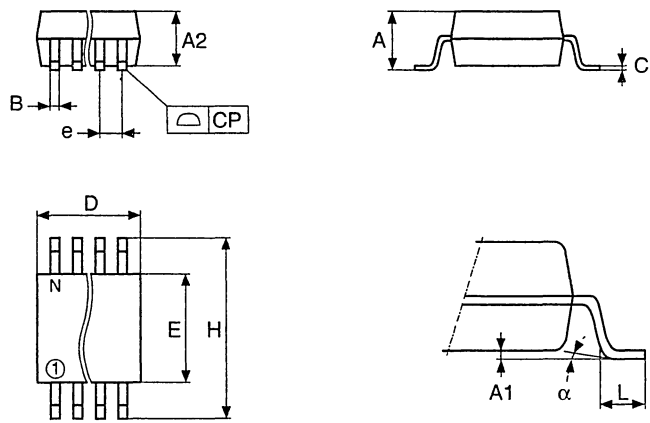


SO-a

Drawing is not to scale.

SO8 - 8 lead Plastic Small Outline, 200 mils body width

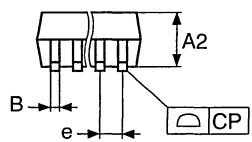
Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.03			0.080
A1		0.10	0.25		0.004	0.010
A2			1.78			0.070
B		0.35	0.45		0.014	0.018
C	0.20	–	–	0.008	–	–
D		5.15	5.35		0.203	0.211
E		5.20	5.40		0.205	0.213
e	1.27	–	–	0.050	–	–
H		7.70	8.10		0.303	0.319
L		0.50	0.80		0.020	0.031
α		0°	10°		0°	10°
N	8			8		
CP			0.10			0.004

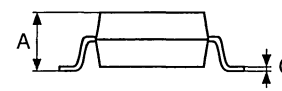


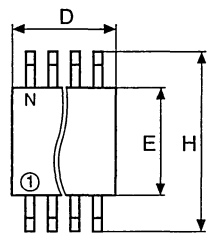
SO-b

TSSOP14 - 14 lead Thin Shrink Small Outline

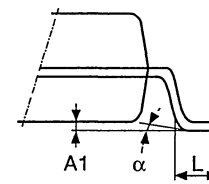
Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.10			0.043
A1		0.05	0.15		0.002	0.006
A2		0.85	0.95		0.033	0.037
B		0.19	0.30		0.007	0.012
C		0.09	0.20		0.004	0.008
D		4.90	5.10		0.193	0.197
E		6.25	6.50		0.246	0.256
E1		4.30	4.50		0.169	0.177
e	0.65	–	–	0.026	–	–
L		0.50	0.70		0.020	0.028
α		0°	8°		0°	8°
N	14			14		
CP			0.08			0.003







SO-b

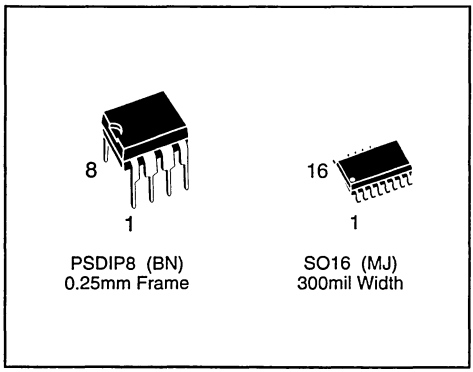


M95512

512 Kbit Serial SPI EEPROM with High Speed Clock and Positive Clock Strobe

PRODUCT PREVIEW

- 100,000 ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  - 4.5V to 5.5V for M95512
  - 2.5V to 5.5V for M95512-W
  - 1.8V to 3.6V for M95512-R
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 5 MHz CLOCK RATE MAX
- STATUS REGISTER
- HARDWARE PROTECTION of the STATUS REGISTER
- SCHMITT TRIGGER, FILTERED INPUTS FOR NOISE SUPPRESSION
- 128 BYTE PAGE MODE
- SIZEABLE READ ONLY EEPROM AREA
- SELF-TIMED PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- SUPPORTS POSITIVE CLOCK SPI MODES



PSDIP8 (BN)
0.25mm Frame

SO16 (MJ)
300mil Width

DESCRIPTION

The M95512 is an Electrically Erasable Programmable memory (EEPROM) fabricated with STMicroelectronics's High Endurance Double Polysilicon CMOS technology. Each memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q).

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

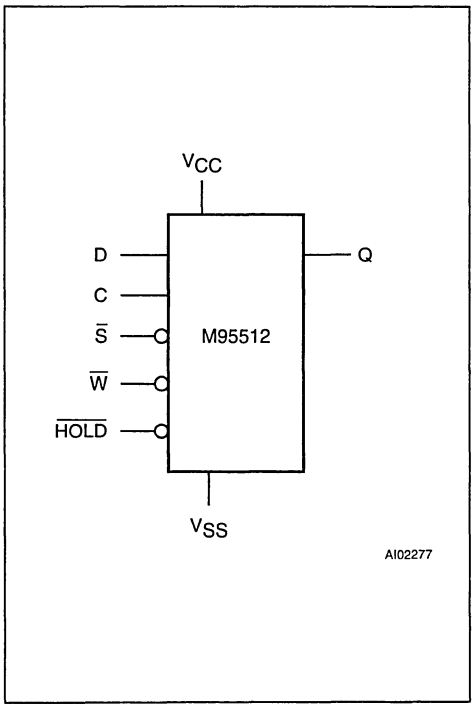


Figure 2A. DIP Pin Connections

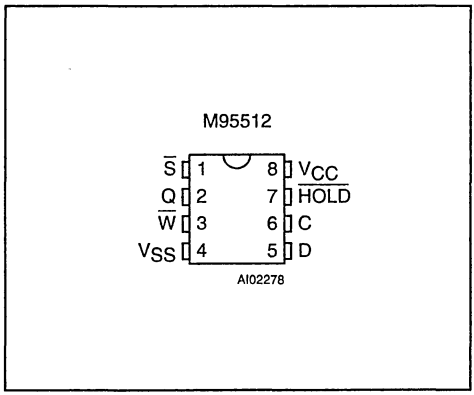


Figure 2B. SO Pin Connections

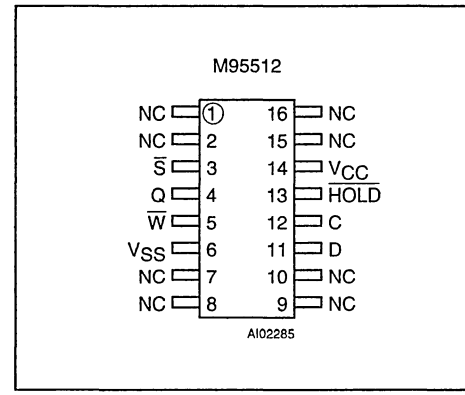


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature:			–40 to 125	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO16 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to V_{CC} +0.6	V
V_I	Input Voltage with respect to Ground			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			400	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500Ω)
3 EIAJ IC-121 (Condition C) (200pF, 0Ω)

DESCRIPTION (cont'd)

The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$).

Data is clocked in during the low to high transition of clock C, data is clocked out during the high to low transition of clock C.

SIGNALS DESCRIPTION

Serial Output (Q). The output pin is used to transfer data serially out of the memory. Data is shifted out on the falling edge of the serial clock.

Serial Input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Input is latched on the rising edge of the serial clock.

Figure 3. Data and Clock Timing

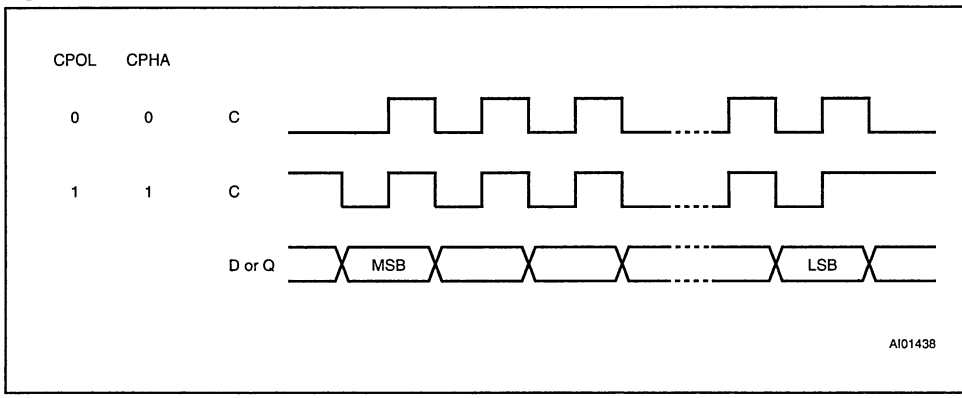
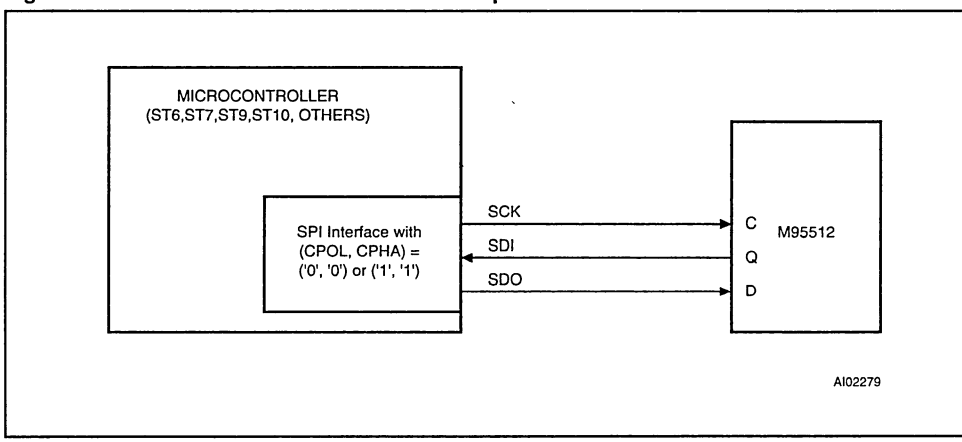


Figure 4. Microcontroller and SPI Interface Set-up



Serial Clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched on the rising edge of the clock input, while data on the Q pin changes after the falling edge of the clock input.

Chip Select ($\overline{S}$). When $\overline{S}$ is high, the memory is deselected and the Q output pin is at high impedance and, unless an internal write operation is underway the memory will be in the standby power mode. $\overline{S}$ low enables the memory, placing it in the active power mode. It should be noted that after power-on, a high to low transition on $\overline{S}$ is required prior to the start of any operation.

Write Protect ($\overline{W}$). This pin is for hardware write protection of the status register (SR); except WIP and WEL bits. When bit 7 (SRWD) of the status register is 0 (the initial delivery state); it is possible to write the SR once the WEL (Write Enable Latch) has been set and whatever is the status of pin $\overline{W}$ (high or low).

Note: SRWD stands for; Status Register Write Disable.

SIGNALS DESCRIPTION (cont'd)

Once bit 7 (SRWD) of the status register has been set to 1; the possibility to rewrite the SR depends on the logical level present at pin $\overline{W}$:

- If $\overline{W}$ pin is high; it will be possible to rewrite the status register after having set the WEL (Write Enable Latch).
- If $\overline{W}$ pin is low; any attempt to modify the status register will be ignored by the device even if the WEL was set. As a consequence: all the data bytes in the EEPROM area protected by the BPn bits of the status register are also hardware protected against data corruption and can be seen as a Read Only EEPROM area from the microcontroller. This mode is called the Hardware Protected Mode (HPM).

It is possible to enter the Hardware Protected Mode (HPM) by setting SRWD bit after pulling down the $\overline{W}$ pin or by pulling down the $\overline{W}$ pin after setting SRWD bit.

The only way to abort the Hardware Protected Mode once entered is to pull high the $\overline{W}$ pin.

If $\overline{W}$ pin is permanently tied to high level; the Hardware Protected Mode will never be activated and the memory will only allow the user to software protect a part of the memory with the BPn bits of the status register. All protection features of the device are summarized in Table 3.

Hold ($\overline{HOLD}$). The $\overline{HOLD}$ pin pin is used to pause serial communications with an SPI memory without resetting the serial sequence. To take the Hold condition into account, the product must be selected ($\overline{S}$ = 0). The Hold condition is entered by a 0 state on the $\overline{HOLD}$ pin when a 0 state is present on the CLOCK pin (see Figure 5). During the Hold condition, the Q output pin is put at high impedance and the input pins (D, C) are ignored by the memory.

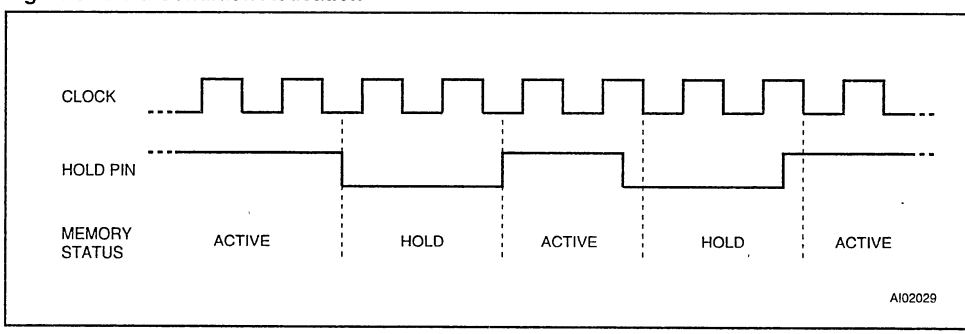
It is possible to deselect the device when it is under the Hold condition. The protocol is then reset. The memory remains on Hold as long as the $\overline{HOLD}$ pin is low. To restart communication with the device, it is necessary to both remove the Hold ($\overline{HOLD}$=1) and to SELECT the memory.

Table 3. Protection Feature

$\overline{W}$	SRWD	Status Register (SR)	Data Bytes (Protected Area)	Mode	Data Bytes (Unprotected Area)
X	0	Writable after setting WEL	Software Write protected by the BPn bits of the Status Register	SPM	Writable after setting WEL
1	1	Writable after setting WEL	Software Write protected by the BPn bits of the Status Register	SPM	Writable after setting WEL
0	1	Hardware Write protected	Hardware Write protected	HPM	Writable after setting WEL

Notes: 1. SPM stands for Software Protected Mode.
2. BPn are BP0 to BP1 bits of the Status Register.
3. SPM and HPM are also described in the Write Status Register (WRSR) section.

Figure 5. Hold Condition Activation



OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first rising edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 4 shows the instruction set and format for device operation. If an invalid instruction is sent (one not contained in Table 4), the chip is automatically deselected.

Write Enable (WREN) and Write Disable (WRDI)

The memory contains a write enable latch. This latch must be set prior to every WRITE, WRSR operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under the following conditions:

- Power on,
- WRDI instruction completion,
- WRSR instruction completion,
- WRITE instruction completion.

As soon as the WREN or WRDI instruction is received, the circuit executes the instruction and enters a wait mode until it is deselected.

Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write to the memory operation. When a write is in progress, it is recommended to check the WIP bit before sending a new WRITE command. For this, it is possible to continuously read the Status Register value as shown in Figure 11. The status register format is as follows:

b7							b0
SRWD	X	X	X	BP1	BP0	WEL	WIP

BP0, BP1: Read and write bits
WEL, WIP. Read only bits
SRWD: Read and Write bit.

During a write operation to the device (memory area or Status Register), all bits of the Status Register are valid and can be read with the RDSR instruction. However, it should be noted that the values of the Non Volatile bits (SRWD, BP0, BP1) read at that time correspond to the previous content of the Status Register. The updated value of these bits will be accessible through a new RDSR instruction performed after completion of the Write Cycle. As the 2 Read Only bits (WEL, WIP) are dynamically updated during internal write cycles, it is possible to continuously get their updated values as shown in Figure 11.

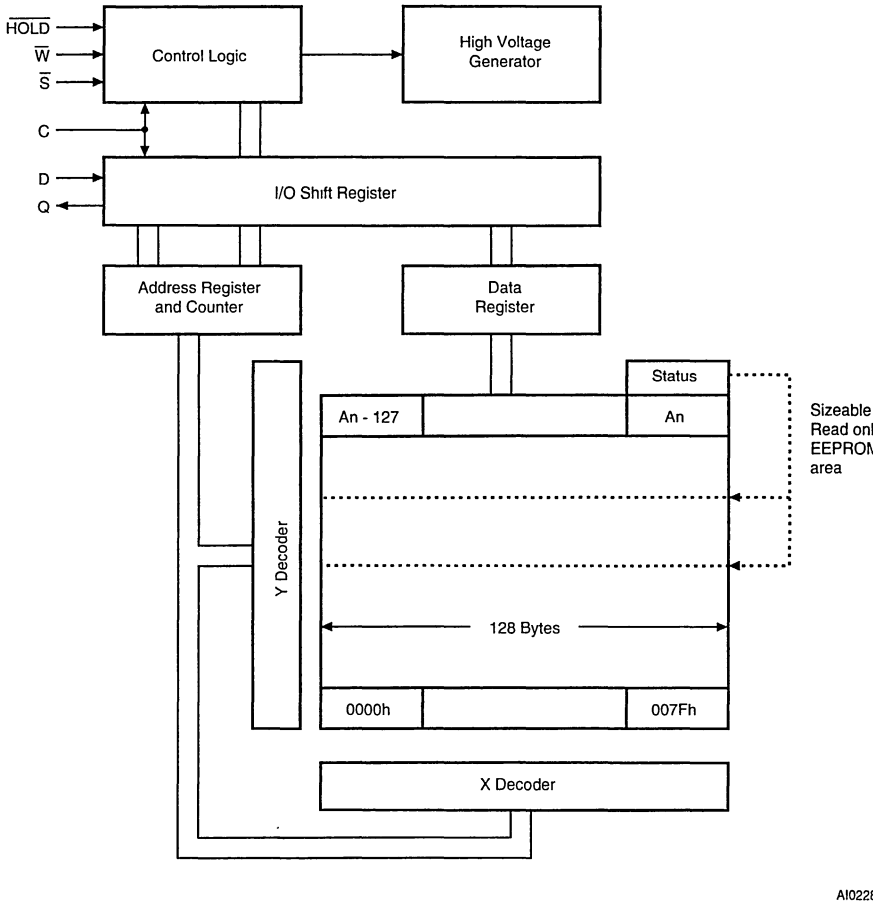
The Write-In-Process (WIP) read-only bit indicates whether the memory is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress.

The Write Enable Latch (WEL) read-only bit indicates the status of the write enable latch. When set to a '1' the latch is set, when set to a '0' the latch is reset. The Block Protect (BP0 and BP1) bits indicate the extent of the protection employed. These 2 bits are non volatile and are set by the user issuing a WRSR instruction.

Table 4. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	0000 0110
WRDI	Reset Write Enable Latch	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read Data from Memory Array	0000 0011
WRITE	Write Data to Memory Array	0000 0010

Figure 6. Block Diagram



Note: An is the top address of the memory.

Figure 7. Read EEPROM Array Operation Sequence

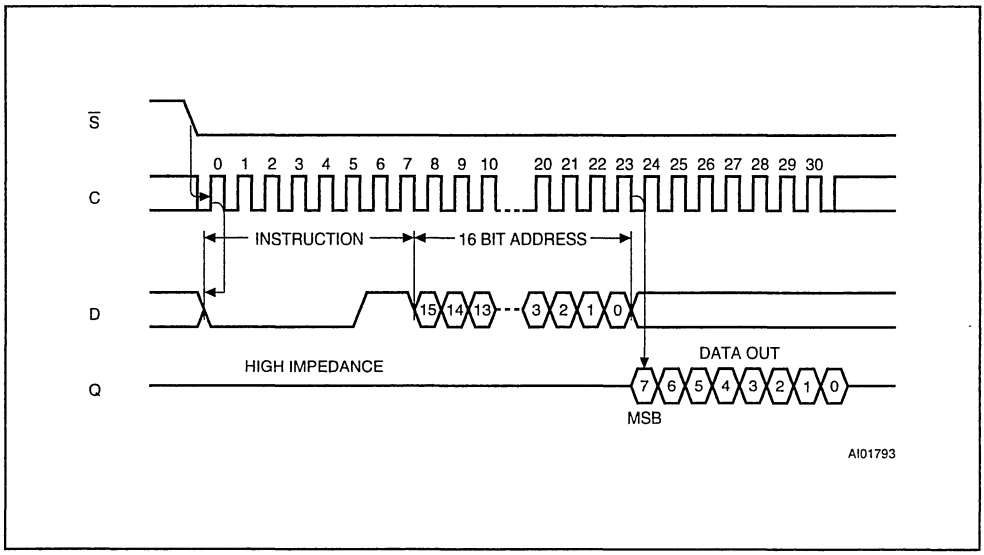


Table 5. Write Protected Block Size

Status Register Bits		Protected Block	M95512
BP1	BP0		
0	0	none	none
0	1	Upper quarter	C000h - FFFFh
1	0	Upper half	8000h - FFFFh
1	1	Whole Memory	0000h - FFFFh

Write Status Register (WRSR)

When the WRSR instruction and the 8 bits of the Status Register are latched-in, the internal write cycle is then triggered by the rising edge of $\overline{S}$. This rising edge of $\overline{S}$ must appear just before the rising edge of the 17 th clock pulse (see Serial input timing Figure 15), otherwise the internal write sequence is not performed.

The WRSR instruction allows the user:

1. to select the size of the memory to be protected,
2. to choose the protection level between the SPM (Software Protected Mode) and the HPM (Hardware Protected Mode).

Size Selection. The way to select the size of the EEPROM area to be protected is common to both SPM and HPM. BP1 and BP0 bits (initial delivery states = 00; that is size = 0) of the Status Register have to be written once the data to be protected are stored in the EEPROM. The Table 6 summarizes the size selection functions of the memory.

Figure 8. Write Enable Latch Sequence

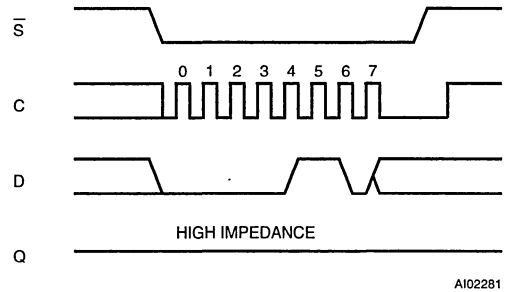


Figure 9. Byte Write Operation Sequence

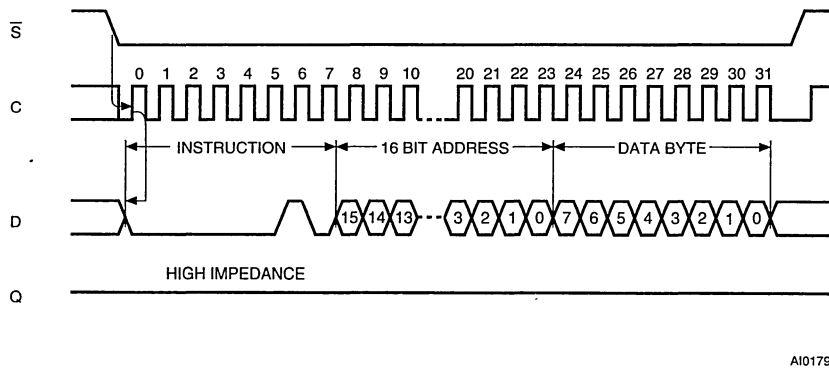


Figure 10. Page Write Operation Sequence

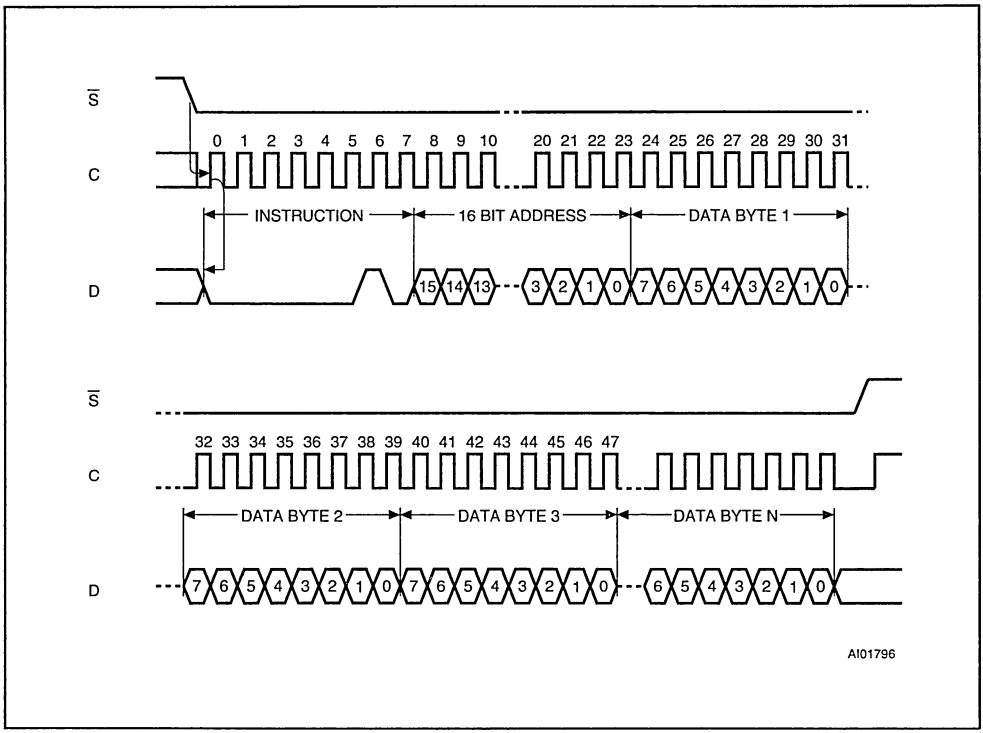


Figure 11. RDSR: Read Status Register Sequence

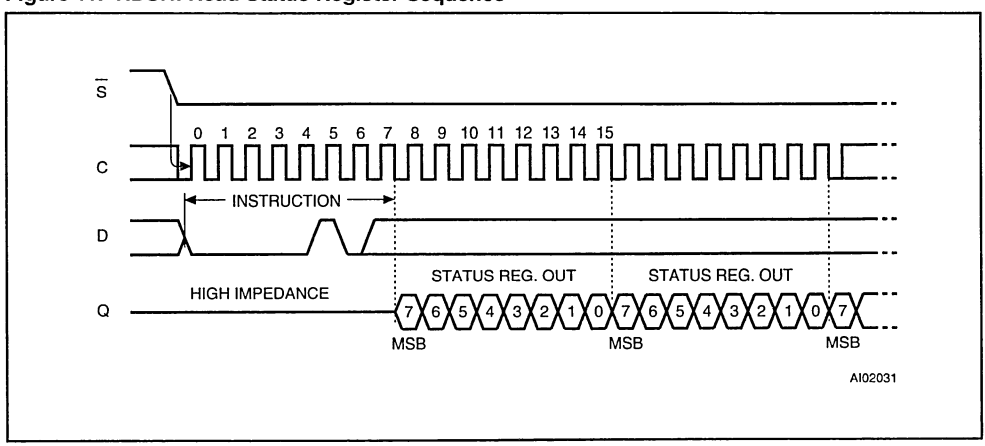
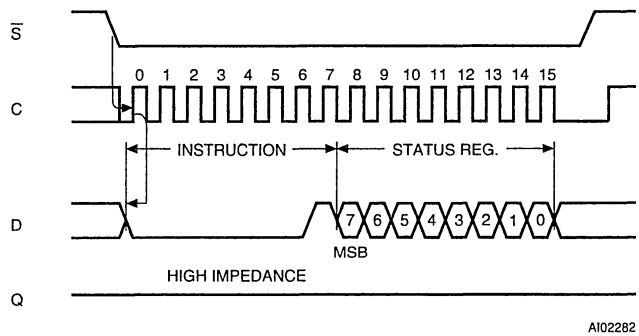


Figure 12. WRSR: Write Status Register Sequence



Selection of the Protection Level

- Once BP0 and BP1 bits are written; **the Software Protected Mode (SPM) is entered.** This means that any attempt to write a byte or a page in the protected area will be ignored even if the Write Enable Latch was set before the write instruction. In this Software Protected Mode; BP0 and BP1 bits can be rewritten with the WSR instruction after having set the WEL.
- If a higher level of protection is needed; **the Hardware Protected Mode (HPM)** can be selected. It is possible to enter the HPM by setting SRWD bit after pulling down the $\overline{W}$ pin or by pulling down the $\overline{W}$ pin after setting SRWD. In both cases, the SRWD is set by using the WSR instruction after having set the WEL bit. It should also be noted that the SRWD can be set after writing BP0 and BP1 or at the same time.
- Once the HPM is entered, the content of the Status Register and all data bytes in the protected area are Hardware Protected against write attempts. The only way to write again the status register is to abort the HPM by pulling high the $\overline{W}$ pin. Aborting the HPM will put the device in the SPM with BP0 and BP1 bits unchanged.

Note: See also the Write Protect pin ($\overline{W}$) description on page 3).

Typical Applications

- The $\overline{W}$ pin can be dynamically driven by an output port of a microcontroller but can also be connected directly or through a pull-down resistor to V_{SS}.
- With such a PCB (Printed Circuit Board):

  a) the memory in the initial delivery state can be soldered directly. After power on, the microcontroller can write data to be protected in the memory. Then write BP0, BP1 and set the SRWD to enter the HPM.

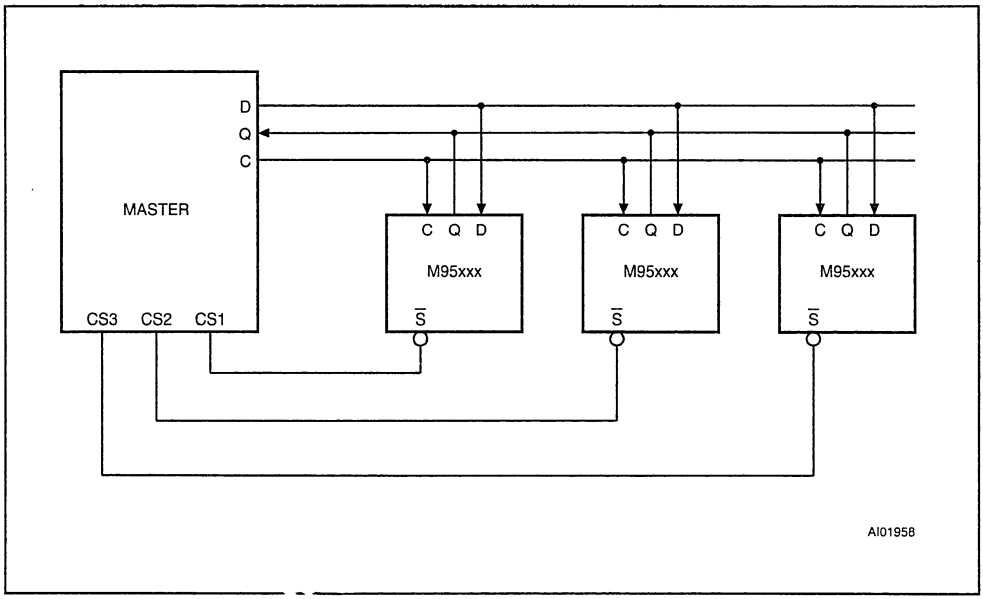
  b) data to be protected, BP0, BP1 can be written and SRWD can be set before soldering the memory. As a consequence, once soldered, the memory is immediately placed in the HPM.

  In these two cases, the only way to abort the HPM will be to remove the memory from the PCB or to apply V_{CC} on the $\overline{W}$ pin through an external equipment when a pull-down resistor is inserted between the pin and V_{SS}.

Read Operation

The chip is first selected by putting $\overline{S}$ low. The serial one byte read instruction is followed by a two bytes address (A15-A0), each bit being latched-in during the rising edge of the clock (C).

Figure 13. EEPROM and SPI Bus



Then the data stored in the memory at the selected address is shifted out on the Q output pin; each bit being shifted out during the falling edge of the clock (C). The data stored in the memory at the next address can be read in sequence by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to "0h" allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during a write cycle will be rejected and will deselect the chip.

Byte Write Operation

Prior to any write attempt, the write enable latch must be set by issuing the WREN instruction. First the device is selected ($\overline{S}$ = low) and a serial WREN instruction byte is issued. Then the product is deselected by taking $\overline{S}$ high. After the WREN instruction byte is sent, the memory will set the write enable latch and then remain in standby until it is deselected. Then the write state is entered by selecting the chip, issuing three bytes of instruction and address, and one byte of data.

Chip Select ($\overline{S}$) must remain low for the entire duration of the operation. The product must be deselected just after the eighth bit of data has been latched in. If not, the write process is cancelled. As soon as the product is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read to check BP1, BP0, WEL and WIP. WIP is high during the self-timed write cycle. When the cycle is completed, the write enable latch is reset.

Page Write Operation

A maximum of 128 bytes of data may be written during one non-volatile write cycle. All 128 bytes must reside on the same page. The page write mode is the same as the byte write mode except that instead of deselecting the device after the first byte of data, up to 127 additional bytes can be shifted in prior to deselecting the chip. Any address of the memory can be chosen as the first address to be written. If the address counter reaches the end of the page (xxxx x111 1111) and the clock continues, the counter will roll over to the first address of the page (xxxx x000 0000) and overwrite any previously written data. The programming cycle will only start if the $\overline{S}$ transition occurs just after the eighth bit of data of a word is received.

POWER ON STATE

After a Power up the memory is in the following state:

- The device is in the low power standby state.
- The chip is deselected.
- The chip is not in hold condition.
- The write enable latch is reset.
- b7 to b2 bits of the status register are unchanged (non-volatile bits).

DATA PROTECTION AND PROTOCOL SAFETY

- All inputs are protected against noise, see Table 7.
- Non valid $\overline{S}$ and $\overline{HOLD}$ transitions are not taken into account.
- $\overline{S}$ must come high at the proper clock count in order to start a non-volatile write cycle (in the memory array or in the status register), that is the Chip Select $\overline{S}$ must rise during the clock pulse following the introduction of a multiple of 8 bits.
- Access to the memory array during non-volatile programming cycle is ignored; however, the programming cycle continues.
- After any of the operations WREN, WRDI, RDSR is completed, the chip enters a wait state and waits for a deselect.
- The write enable latch is reset upon power-up.

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state (all data set at all "1's" or FFh). The Status Register Bits are initialized to 00.

Status Register:

b7							b0
0	0	0	0	0	0	0	0

Table 6. Input Parameters (1) (T_A = 25 °C, f = 5 MHz)

Symbol	Parameter	Min	Max	Unit
C_{OUT}	Ouput Capacitance (Q)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF
t_{LPF}	Input Signal Pulse Width Filtered Out		10	ns

Note: 1. Sampled only, not 100% tested.

Table 7. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$
Output Load	C_L = 100pF

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 14. AC Testing Input Output

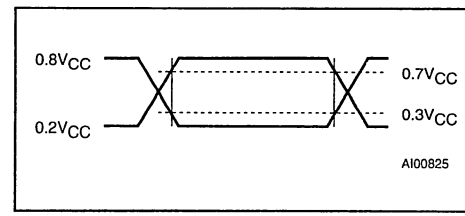


Table 8. DC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or -40 to 125°C; V_{CC} = 4.5V to 5.5V)
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.5V to 5.5V)
(T_A = 0 to 70°C or –20 to 85°C; V_{CC} = 1.8V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			2	µA
I_{LO}	Output Leakage Current			2	µA
I_{CC}	Supply Current	C = 0.1 V_{CC}/0.9 V_{CC}, @ 5 MHz, V_{CC} = 5V, Q = Open		3	mA
		C = 0.1 V_{CC}/0.9 V_{CC}, @ 2 MHz, V_{CC} = 5V, Q = Open, Note 2		3	mA
	Supply Current (W series)	C = 0.1 V_{CC}/0.9 V_{CC}, @ 2 MHz, V_{CC} = 2.5V, Q = Open		2	mA
	Supply Current (R series)	C = 0.1 V_{CC}/0.9 V_{CC}, @ tbc MHz, V_{CC} = 1.8V, Q = Open		2	mA
I_{CC1}	Standby Current	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V		20	µA
		$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V, Note 2		20	µA
	Standby Current (W series)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V		2	µA
	Standby Current (R series)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 1.8V		0.1	µA
V_{IL}	Input Low Voltage		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	Note 3	0.05 V_{CC}		V
V_{OL} (1)	Output Low Voltage	I_{OL} = 2mA, V_{CC} = 5V		0.4	V
		I_{OL} = 2mA, V_{CC} = 5V, Note 2		0.4	V
	Output Low Voltage (W series)	I_{OL} = 1.5mA, V_{CC} = 2.5V		0.4	V
	Output Low Voltage (R series)	I_{OL} = 0.15mA, V_{CC} = 1.8V		0.3	V
V_{OH} (1)	Output High Voltage	I_{OH} = –2mA, V_{CC} = 5V	0.8 V_{CC}		V
		I_{OH} = –2mA, V_{CC} = 5V, Note 2	0.8 V_{CC}		V
	Output High Voltage (W series)	I_{OH} = –0.4mA, V_{CC} = 2.5V	0.8 V_{CC}		V
	Output High Voltage (R series)	I_{OH} = –0.1mA, V_{CC} = 1.8V	0.8 V_{CC}		V

Notes: 1. The device meets output requirements for both TTL and CMOS standards.
2. Test performed at –40 to 125C temperature range, grade 3.
3. Value guaranteed by characterization, not 100% tested in production.

Table 9A. AC Characteristics

Symbol	Alt	Parameter	M95512				Unit
			V_{CC} = 4.5V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		V_{CC} = 4.5V to 5.5V, T_A = –40 to 125°C		
			Min	Max	Min	Max	
f_C	f_C	Clock Frequency	D.C.	5	D.C.	2.1	MHz
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time	100		100		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	100		100		ns
t_{CH} (1)	t_{CLH}	Clock High Time	60		200		ns
t_{CL} (1)	t_{CLL}	Clock Low Time	80		200		ns
t_{CLCH}	t_{RC}	Clock Rise Time		1		1	µs
t_{CHCL}	t_{FC}	Clock Fall Time		1		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		50		ns
t_{CHDX}	t_{DH}	Data In Hold Time	20		50		ns
t_{DLDH}	t_{RI}	Data In Rise Time		1		1	µs
t_{DHDL}	t_{FI}	Data In Fall Time		1		1	µs
t_{HHCH}	t_{HSU}	$\overline{HOLD}$ Setup Time	100		100		ns
t_{HLCH}		Clock Low Hold Time	100		90		ns
t_{CHHL} (3)		$\overline{HOLD}$ Hold Time	t.b.c		t.b.c		ns
t_{CHHH} (3)		Clock High Setup Time before Hold Active	t.b.c		t.b.c		ns
t_{CHSH}		$\overline{S}$ Active Hold Time	200		200		ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time	100		100		ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect Time	200		200		ns
t_{SHQZ}	t_{DIS}	Output Disable Time		100		150	ns
t_{CLQV}	t_V	Clock Low to Output Valid		60		300	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		ns
t_{QLQH} (2)	t_{RO}	Output Rise Time		100		100	ns
t_{QHQL} (2)	t_{FO}	Output Fall Time		100		100	ns
t_{HHQX}	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		50		100	ns
t_{HLQZ}	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		50		130	ns
t_W	t_{WP}	Write Cycle Time		10		10	ms

Notes: 1. $t_{CH} + t_{CL} \geq 1/f_C$.
2. Value guaranteed by characterization, not 100% tested in production.
3. t.b.c. stands for to be characterized.

Table 9B. AC Characteristics

Symbol	Alt	Parameter	M95512				Unit
			V_{CC} = 2.5V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		V_{CC} = 1.8V to 3.6V, T_A = 0 to 70°C, T_A = –20 to 85°C		
			Min	Max	Min	Max	
f_C	f_C	Clock Frequency	D.C.	2.1	D.C.	1	MHz
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time	100		200		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	100		200		ns
t_{CH} (1)	t_{CLH}	Clock High Time	200		400		ns
t_{CL} (1)	t_{CLL}	Clock Low Time	200		400		ns
t_{CLCH}	t_{RC}	Clock Rise Time		1		1	µs
t_{CHCL}	t_{FC}	Clock Fall Time		1		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	50		100		ns
t_{CHDX}	t_{DH}	Data In Hold Time	50		100		ns
t_{DLDH}	t_{RI}	Data In Rise Time		1		1	µs
t_{DHDL}	t_{FI}	Data In Fall Time		1		1	µs
t_{HHCH}	t_{HSU}	$\overline{HOLD}$ Setup Time	100		200		ns
t_{HLCH}		Clock Low Hold Time	90		200		ns
t_{CHHL} (3)		$\overline{HOLD}$ Hold Time	t.b.c		t.b.c		ns
t_{CHHH} (3)		Clock High Setup Time before Hold Active	t.b.c		t.b.c		ns
t_{CHSH}		$\overline{S}$ Active Hold Time	200		200		ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time	100		200		ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect Time	200		200		ns
t_{SHQZ}	t_{DIS}	Output Disable Time		150		200	ns
t_{CLQV}	t_V	Clock Low to Output Valid		300		400	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		ns
t_{QLQH} (2)	t_{RO}	Output Rise Time		100		200	ns
t_{QHQL} (2)	t_{FO}	Output Fall Time		100		200	ns
t_{HHQX}	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		100		200	ns
t_{HLQZ}	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		130		200	ns
t_W	t_{WP}	Write Cycle Time		10		10	ms

Notes: 1. $t_{CH} + t_{CL} \geq 1/f_C$.
2. Value guaranteed by characterization, not 100% tested in production.
3. t.b.c stands for to be characterized.

Figure 15. Serial Input Timing

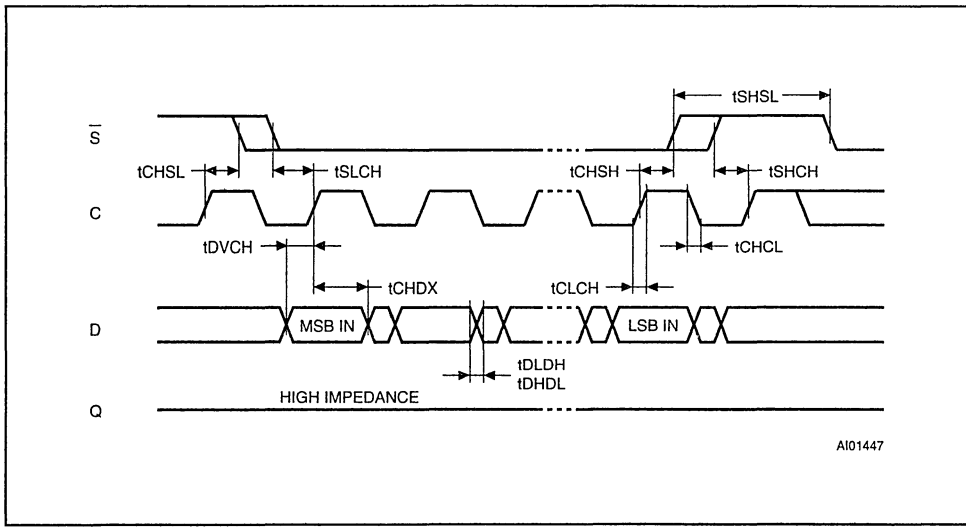


Figure 16. Hold Timing

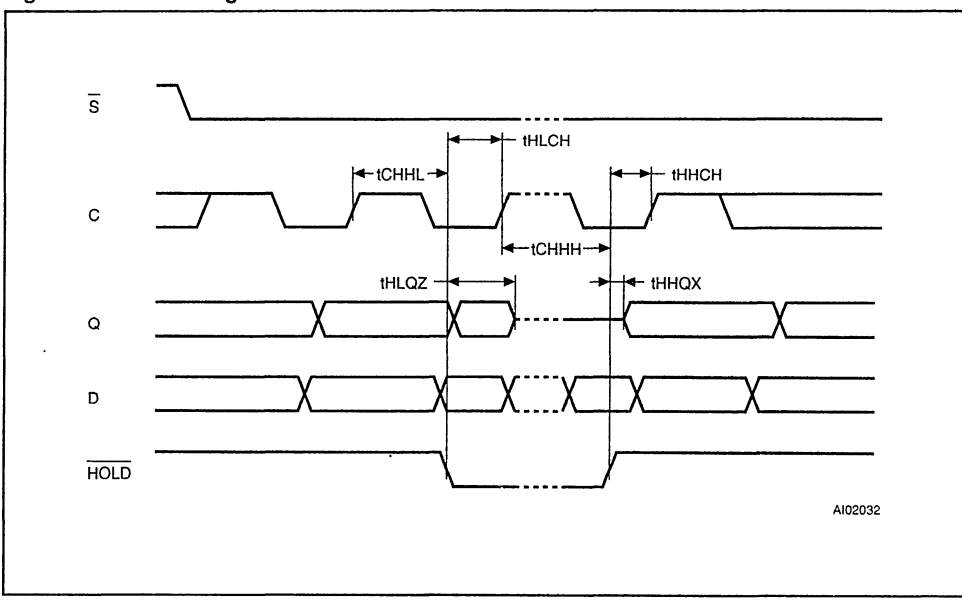
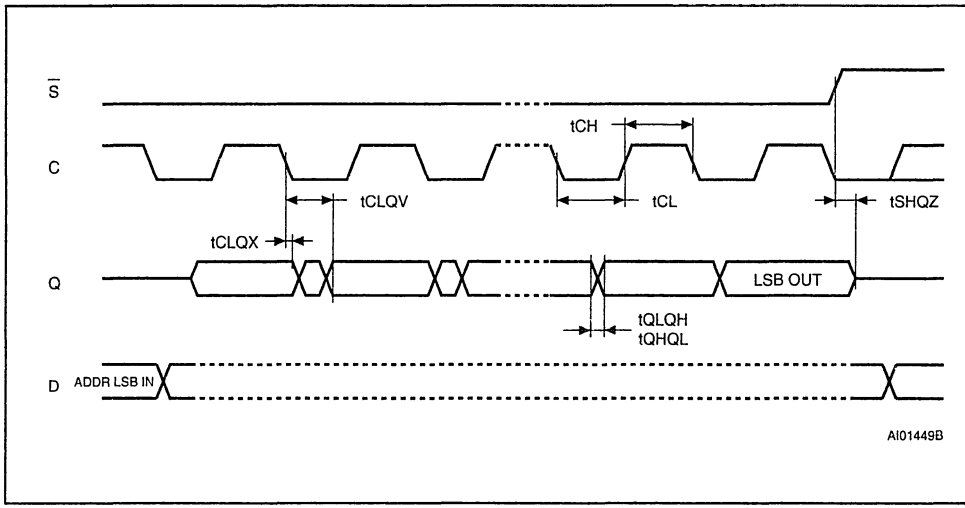


Figure 17. Output Timing



ORDERING INFORMATION SCHEME

Example: M95512 – R MJ 5 T

Density	Operating Voltage	Package	Temperature Range	Option
512 512K (64 x 8)	blank 4.5V to 5.5V	BN PSDIP8 0.25mm Frame	1 (1) 0 to 70 °C	T Tape & Reel Packing
	W 2.5V to 5.5V		6 –40 to 85 °C	
	R (2) 1.8V to 3.6V	MJ SO16 300mil Width	3 (3) –40 to 125 °C	
			5 –20 to 85 °C	

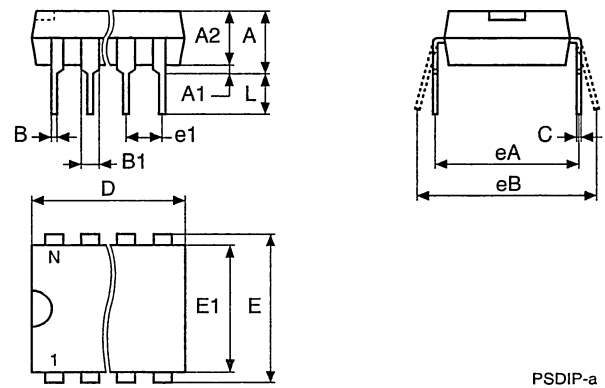
Notes: 1. Temperature range on request only,
2. -R version (1.8V to 3.6V) are only available in temperature ranges 5 or 1.
3. Produced with High Reliability Certified Flow (HRCF), in V_{CC} range 4.5V to 5.5V only.

Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB		–	10.00		–	0.394
L		3.00	3.80		0.118	0.150
N	8			8		

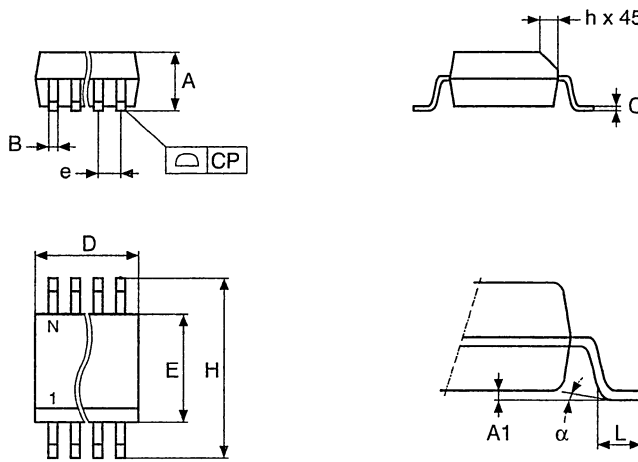


PSDIP-a

Drawing is not to scale.

SO16 - 16 lead Plastic Small Outline, 300 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.59			0.102
A1		0.10	0.30		0.004	0.012
B		0.38	0.51		0.015	0.020
C		0.23	0.25		0.009	0.010
D		10.11	10.49		0.398	0.413
E		7.44	7.54		0.293	0.297
e	1.27	–	–	0.050	–	–
H		10.16	10.41		0.400	0.410
h	0.38			0.015		
L		0.41	1.27		0.016	0.050
α		0°	8°		0°	8°
N	16			16		
CP			0.10			0.004



SO-a

Drawing is not to scale.

2 Kbit Serial SPI EEPROM with High Speed Clock

- HIGH SPEED CLOCK RATE:
  - 2.1 MHz Max
- 1,000,000 ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE 4.5V to 5.5V SUPPLY VOLTAGE
- SPI BUS COMPATIBLE SERIAL INTERFACE
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- SUPPORTS POSITIVE CLOCK SPI MODES

SO8 (M)
150mil Width

DESCRIPTION

The ST95022 is an high speed 2 Kbit Electrically Erasable Programmable Memory (EEPROM) fabricated with STMicroelectronics's High Endurance Single Polysilicon CMOS technology. The memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q).

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

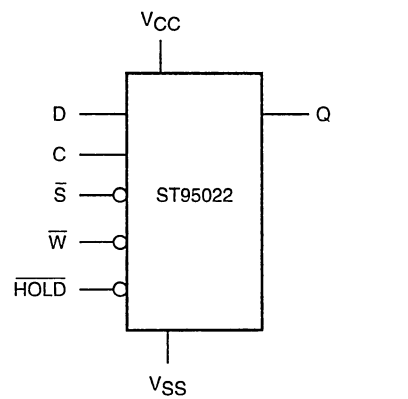
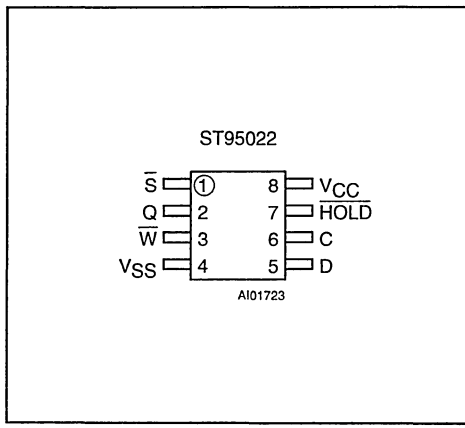


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (2)	–40 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering (SO8 package) 40 sec	215	°C
V_O	Output Voltage	–0.3 to V_{CC} +0.6	V
V_I	Input Voltage with respect to Ground	–0.3 to 6.5	V
V_{CC}	Supply Voltage	–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (3)	4000	V
	Electrostatic Discharge Voltage (Machine model) (4)	500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Depends on range.
3. MIL-STD-883C, 3015.7 (100pF, 1500Ω)
4. EIAJ IC-121 (Condition C) (200pF, 0Ω)

Figure 2B. SO Pin Connections



DESCRIPTION (cont'd)

The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$). The write operation is disabled by a write protect input ($\overline{W}$).

Data is clocked in during the low to high transition of clock C, data is clocked out during the high to low transition of clock C.

SIGNALS DESCRIPTION

Serial Output (Q). The output pin is used to transfer data serially out of the ST95022. Data is shifted out on the falling edge of the serial clock.

Serial Input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Input is latched on the rising edge of the serial clock.

Serial Clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched on the rising edge of the clock input, while data on the Q pin changes after the falling edge of the clock input.

Chip Select ($\overline{S}$). When $\overline{S}$ is high, the ST95022 is deselected and the D output pin is at high impedance and, unless an internal write operation is underway the ST95022 will be in the standby power mode. $\overline{S}$ low enables the ST95022, placing it in the active power mode. It should be noted that after power-on, a high to low transition on $\overline{S}$ is required prior to the start of any operation.

Write Protect ($\overline{W}$). This pin is for hardware write protection. When $\overline{W}$ is low, writes to the ST95022 memory are disabled but any other operations stay enabled. When $\overline{W}$ is high, all writes operations are available. $\overline{W}$ going low at any time before the last bit D0 of the data stream will reset the write enable latch and prevent programming. No action on $\overline{W}$ or on the write enable latch can interrupt a write cycle which has commenced.

Figure 3. Data and Clock Timing

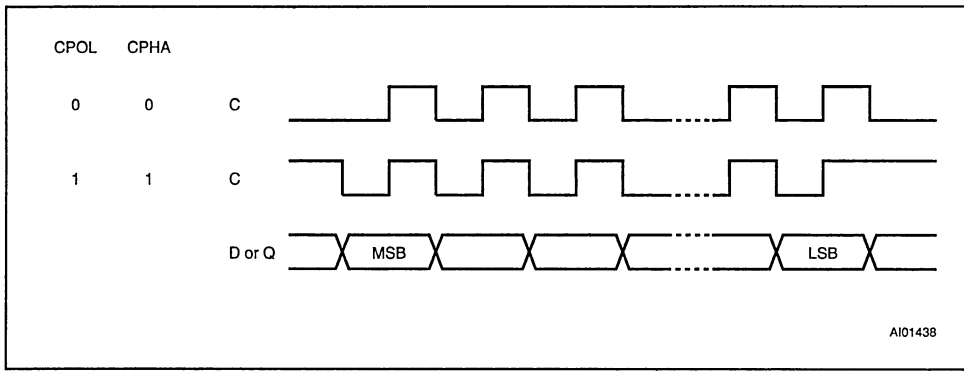
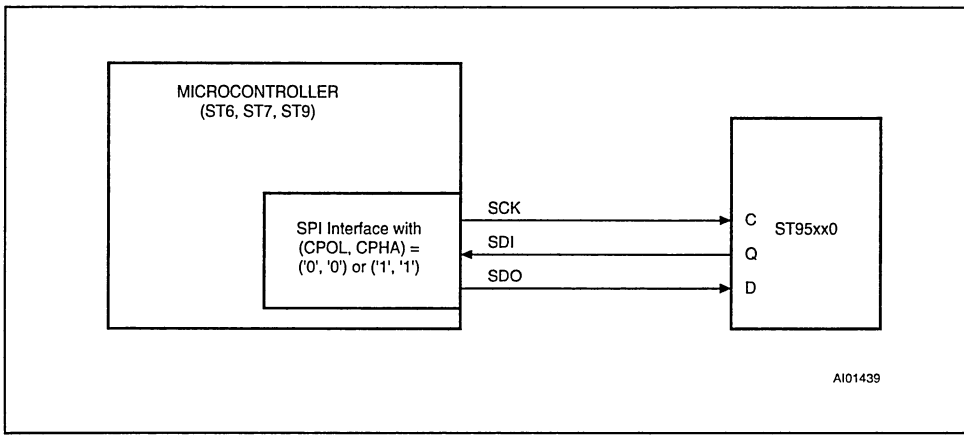


Figure 4. Microcontroller and SPI Interface Set-up



Hold ($\overline{\text{HOLD}}$). The $\overline{\text{HOLD}}$ pin is used to pause serial communications with a ST95022 without resetting the serial sequence. To take the Hold condition into account, the product must be selected ($\overline{S}$ = 0). Then the Hold state is validated by a high to low transition on $\overline{\text{HOLD}}$ when C is low. To resume the communications, $\overline{\text{HOLD}}$ is brought high while C is low. During the Hold condition D, Q, and C are at a high impedance state.

When the ST95022 is under the Hold condition, it is possible to deselect the device. However, the serial communications will remain paused after a reselect, and the chip will be reset.

The ST95022 can be driven by a microcontroller with its SPI peripheral running in either of the two following modes: (CPOL, CPHA) = ('0', '0') or (CPOL, CPHA) = ('1', '1').

For these two modes, input data is latched in by the low to high transition of clock C, and output data is available from the high to low transition of Clock (C).

The difference between (CPOL, CPHA) = (0, 0) and (CPOL, CPHA) = (1, 1) is the stand-by polarity: C remains at '0' for (CPOL, CPHA) = (0, 0) and C remains at '1' for (CPOL, CPHA) = (1, 1) when there is no data transfer.

OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first rising edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 3 shows the instruction set and format for device operation. If an invalid instruction is sent (one not contained in Table 3), the chip is automatically deselected.

Write Enable (WREN) and Write Disable (WRDI)

The ST95022 contains a write enable latch. This latch must be set prior to every WRITE or WRSR operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under the following conditions:

- $\overline{W}$ pin is low
- Power on
- WRDI instruction executed
- WRSR instruction executed
- WRITE instruction executed

As soon as the WREN or WRDI instruction is received by the ST95022, the circuit executes the instruction and enters a wait mode until it is deselected.

Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write to the memory operation. As soon as the 8th bit of the status register is read out, the ST95022 enters a wait mode (data on D is not decoded, Q is in Hi-Z) until it is deselected.

The status register format is as follows:

b7							b0
1	1	1	1	BP1	BP0	WEL	WIP

BP1, BP0: Read and write bits.
WEL, WIP: Read only bits.
b7 to b4: Read only bits

During a write to the memory operation to the memory array, all bits BP1, BP0, WEL, WIP are valid and can be read. During a write to the status register, only the bits WEL and WIP are valid and can be read. The values of BP1 and BP0 read at that time correspond to the previous contents of the status register.

The Write-In-Process (WIP) read-only bit indicates whether the ST95022 is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress.

The Write Enable Latch (WEL) read-only bit indicates the status of the write enable latch. When set to a '1' the latch is set, when set to a '0' the latch is reset. The Block Protect (BP0 and BP1) bits indicate the extent of the protection employed. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

Write Status Register (WRSR)

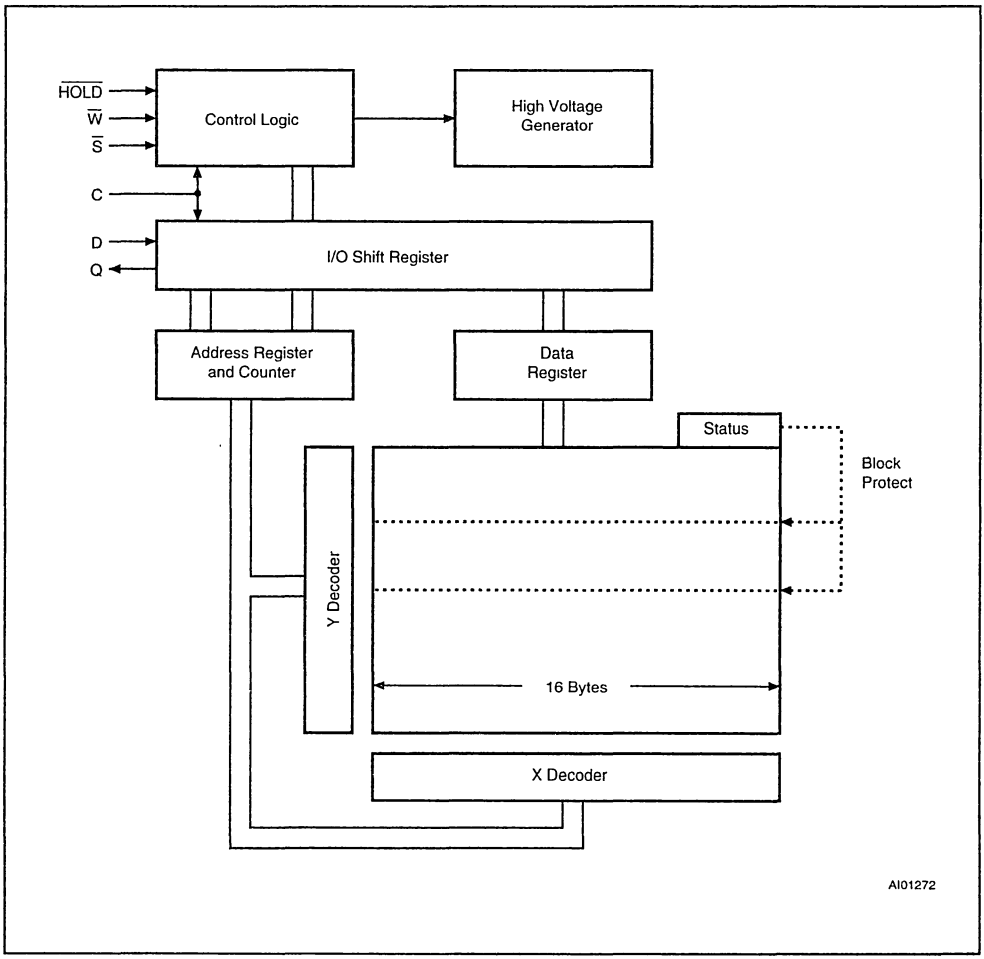
The WRSR instruction allows the user to select the size of protected memory. The ST95022 is divided into four 512 bit blocks. The user may read the blocks but will be unable to write within the pro-

Table 3. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	0000 0110
WRDI	Reset Write Enable Latch	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read Data from Memory Array	0000 0011
WRITE	Write Data to Memory Array	0000 0010

Notes: A = 1, Upper page selected
A = 0, Lower page selected

Figure 5. Block Diagram



tected blocks. The blocks and respective WRSR control bits are shown in Table 4.

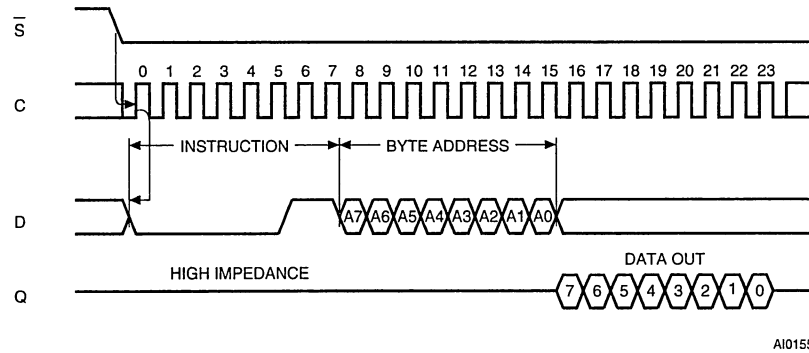
When the WRSR instruction and the 8 bits of the Status Register are latched-in, the internal write cycle is then triggered by the rising edge of $\overline{S}$.

This rising edge of $\overline{S}$ must appear no later than the 16th clock cycle of the WRSR instruction of the Status Register content (it must not appear a 17th clock pulse before the rising edge of $\overline{S}$), otherwise the internal write sequence is not performed.

Table 4. Write Protected Block Size

Status Register Bits		Array Addresses Protected	Protected Block
BP1	BP0		
0	0	none	none
0	1	C0h - FFh	Upper quarter
1	0	80h - FFh	Upper half
1	1	00h - FFh	Whole memory

Figure 6. Read Operation Sequence



Read Operation

The chip is first selected by putting $\overline{S}$ low. The serial one byte read instruction is followed by a one byte address (A7-A0), each bit being latched-in during the rising edge of the clock (C). Then the data stored in the memory at the selected address is shifted out on the Q output pin; each bit being shifted out during the falling edge of the clock (C). The data stored in the memory at the next address can be read in sequence by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to 0h allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during a write cycle will be rejected and will deselect the chip.

Byte Write Operation

Prior to any write attempt, the write enable latch must be set by issuing the WREN instruction. First the device is selected ($\overline{S}$ = low) and a serial WREN instruction byte is issued. Then the product is deselected by taking $\overline{S}$ high. After the WREN instruction byte is sent, the ST95022 will set the write enable latch and then remain in standby until it is deselected. Then the write state is entered by selecting the chip, issuing two bytes of instruction and address, and one byte of data.

Chip Select ($\overline{S}$) must remain low for the entire duration of the operation. The product must be deselected just after the eighth bit of data has been latched in. If not, the write process is cancelled. As soon as the product is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read to check BP1, BP0, WEL and WIP. WIP is high during the self-timed write cycle. When the cycle is completed, the write enable latch is reset.

Figure 7. Write Enable Latch Sequence

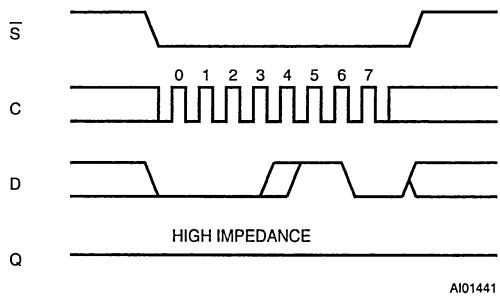


Figure 8. Byte Write Operation Sequence

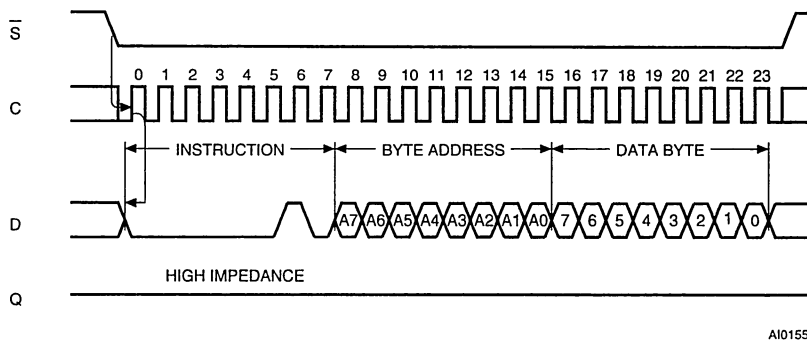


Figure 9. Page Write Operation Sequence

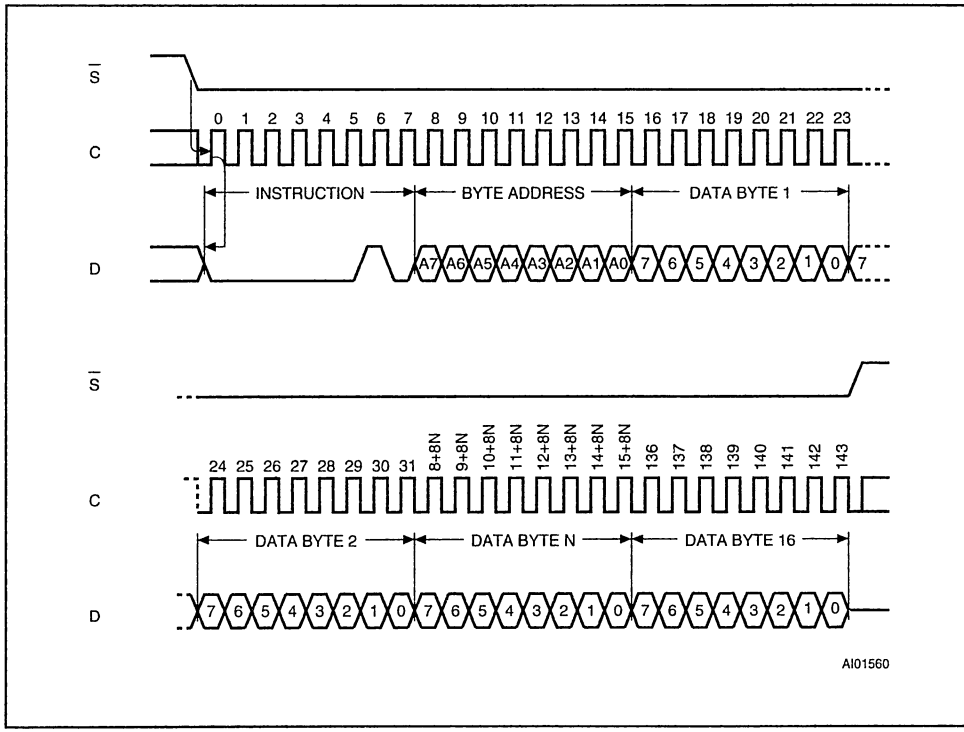


Figure 10. RDSR: Read Status Register Sequence

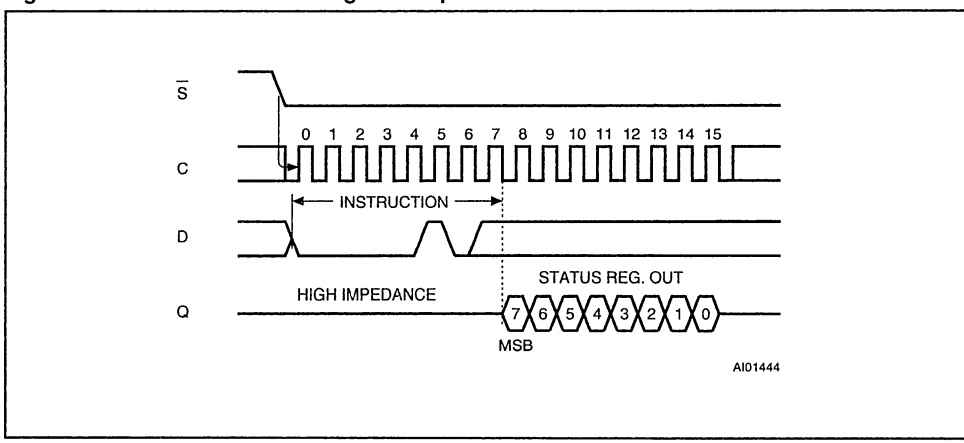
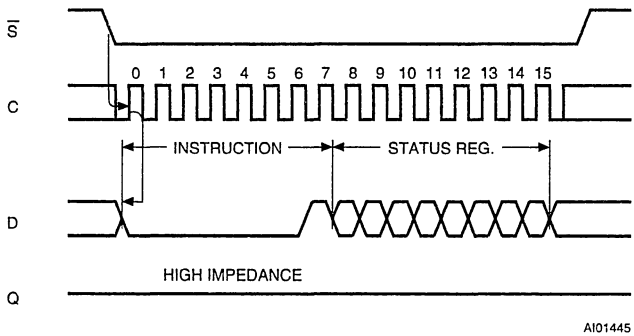


Figure 11. WRSR: Write Status Register Sequence



Page Write Operation

A maximum of 16 bytes of data may be written during one non-volatile write cycle. All 16 bytes must reside on the same page. The page write mode is the same as the byte write mode except that instead of deselecting the device after the first byte of data, up to 15 additional bytes can be shifted in prior to deselecting the chip. A page address begins with address xxxx 0000 and ends with xxxx 1111. If the address counter reaches xxxx 1111 and the clock continues, the counter will roll over to the first address of the page (xxxx 0000) and overwrite any previously written data. The programming cycle will only start if the $\overline{S}$ transition occurs just after the eighth bit of data of a word is received.

POWER ON STATE

After a Power up the ST95022 is in the following state:

- The device is in the low power standby state.
- The chip is deselected.
- The chip is not in hold condition.
- The write enable latch is reset.
- BP1 and BP0 are unchanged (non-volatile bits).

DATA PROTECTION AND PROTOCOL SAFETY

- All inputs are protected against noise, see Table 5.
- Non valid $\overline{S}$ and $\overline{HOLD}$ transitions are not taken into account.
- $\overline{S}$ must come high at the proper clock count in order to start a non-volatile write cycle (in the memory array or in the cycle status register), that is the Chip Select $\overline{S}$ must rise during the clock pulse following the introduction of a multiple of 8 bits.
- Access to the memory array during non-volatile programming cycle is ignored; however, the programming cycle continues.
- After any of the operations WREN, WRDI, RDSR is completed, the chip enters a wait state and waits for a deselect.
- The write enable latch is reset upon power-up.
- The write enable latch is reset when $\overline{W}$ is brought low.

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state (all data set at all "1's" or FFh). The block protect bits are initialized to 00.

Table 5. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$
Output Load	C_L = 100pF

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 12. AC Testing Input Output Waveforms

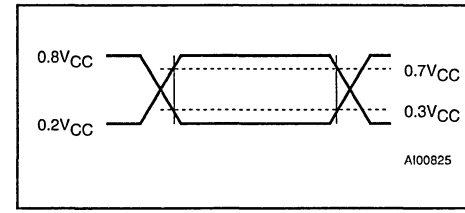


Table 6. Input Parameters (1) (T_A = 25 °C, f = 2.1 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (D)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF
t_{LPF}	Input Signal Pulse Width Filtered Out		10	ns

Note: 1. Sampled only, not 100% tested.

Table 7. DC Characteristics
(T_A = –40 to 125°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			2	µA
I_{LO}	Output Leakage Current			±2	µA
I_{CC}	V_{CC} Supply Current (Active)	C = 0.1 V_{CC}/0.9 V_{CC} , f_C = 2.1 MHz, Q = Open		2	mA
I_{CC1}	V_{CC} Supply Current (Standby)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{OL} (1)	Output Low Voltage	I_{OL} = 2mA		0.4	V
V_{OH} (1)	Output High Voltage	I_{OH} = –2mA	V_{CC} –0.6		V

Note: 1. The device meets output requirements for both TTL and CMOS standards.

Table 8. AC Characteristics
(T_A = –40 to 125°C; V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
f_C	f_C	Clock Frequency		D.C.	2.1	MHz
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time (relative to the rising edge of C)		100		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time (relative to the rising edge of C)		100		ns
t_{CH} (1)	t_{CLH}	Clock High Time		190		ns
t_{CL} (1)	t_{CLL}	Clock Low Time		190		ns
t_{CLCH}	t_{RC}	Clock Rise Time			1	µs
t_{CHCL}	t_{FC}	Clock Fall Time			1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time		50		ns
t_{CHDX}	t_{DH}	Data In Hold Time		50		ns
t_{DLDH}	t_{RI}	Data In Rise Time			1	µs
t_{DHDL}	t_{FI}	Data In Fall Time			1	µs
t_{HHCH}	t_{HSU}	$\overline{HOLD}$ Setup Time		100		ns
t_{HLCH}		Clock Low Hold Time after $\overline{HOLD}$ Active		100		ns
t_{CLHL}	t_{HH}	$\overline{HOLD}$ Hold Time		80		ns
t_{CLHH}		Clock Low Set-up Time before $\overline{HOLD}$ Inactive		100		ns
t_{CHSH}		$\overline{S}$ Active Hold Time (relative to the rising edge of C)		200		ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time (relative to the rising edge of C)		100		ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect Time		200		ns
t_{SHQZ}	t_{DIS}	Output Disable Time			150	ns
t_{CLQV}	t_V	Clock Low to Output Valid			240	ns
t_{CLQX}	t_{HO}	Output Hold Time		0		ns
t_{QLQH} (2)	t_{RO}	Output Rise Time			100	ns
t_{QHQL} (2)	t_{FO}	Output Fall Time			100	ns
t_{HHQX}	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z			100	ns
t_{HLQZ}	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z			200	ns
t_W	t_{WP}	Write Cycle Time			7	ms

Notes: 1. $t_{CH} + t_{CL} \geq 1/fc$
2. Value guaranteed by characterization, not 100% tested in production.

Figure 13. Serial Input Timing

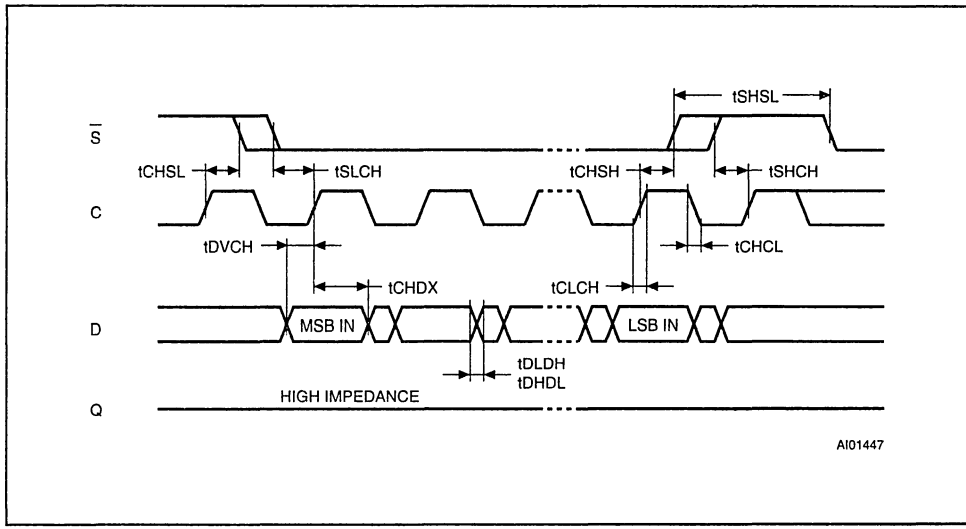


Figure 14. Hold Timing

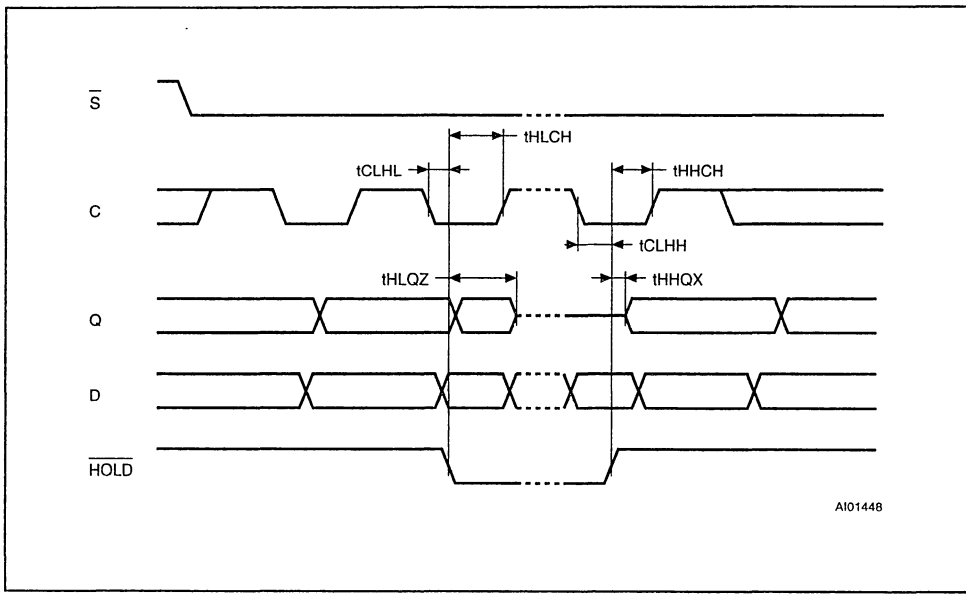


Figure 15. Output Timing

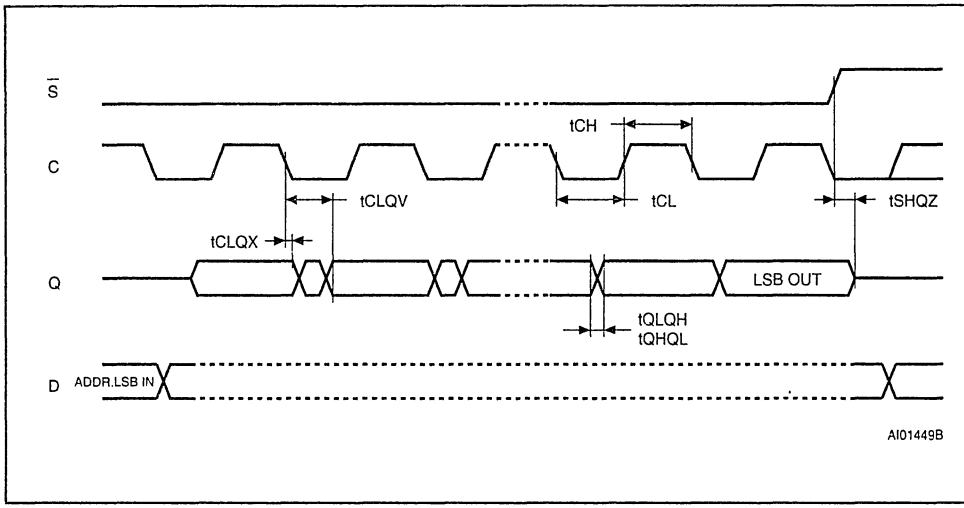
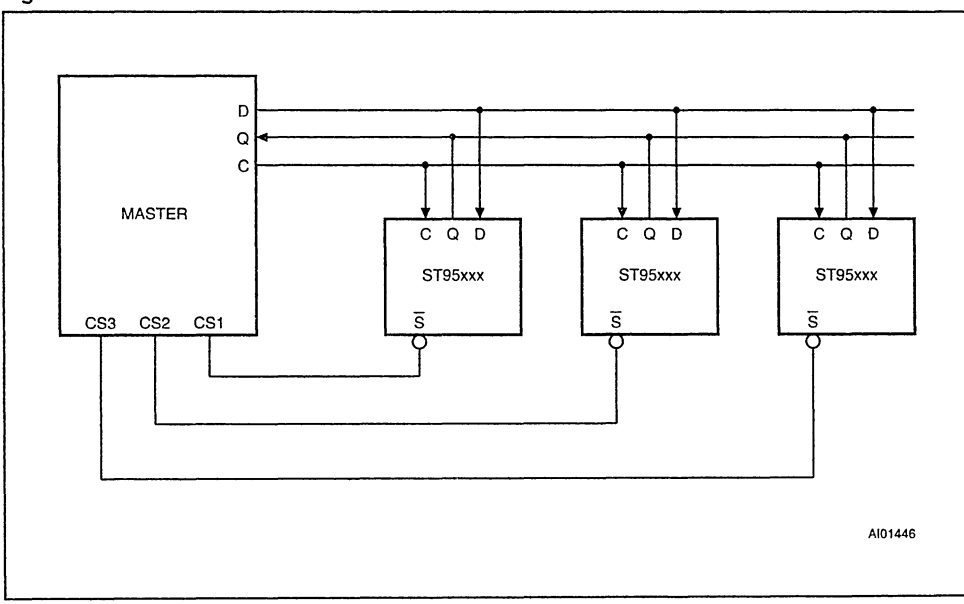
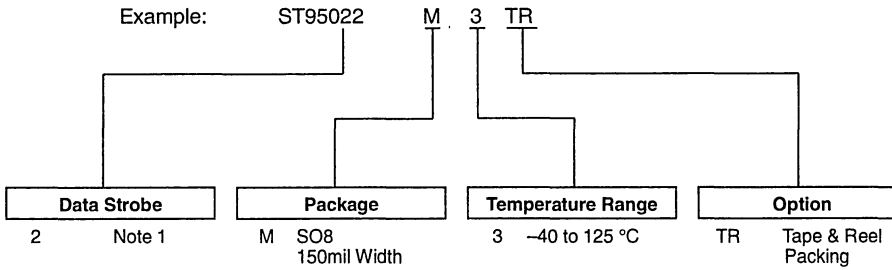


Figure 16. EEPROM and SPI Bus



ORDERING INFORMATION SCHEME



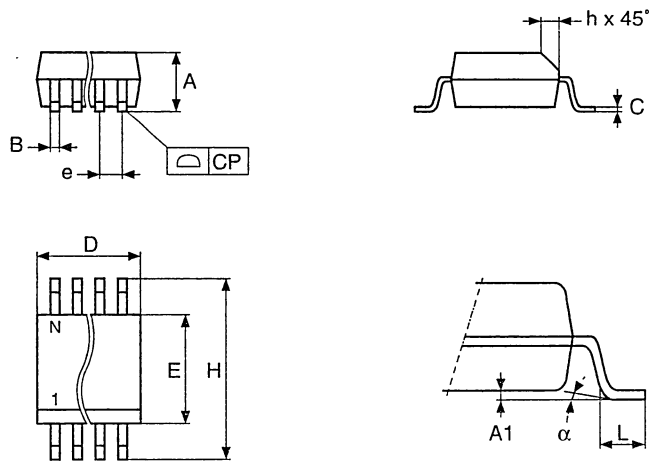
Note: 1. Data In is strobed on rising edge of the clock (C) and Data Out is synchronized from the falling edge of the clock.

Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

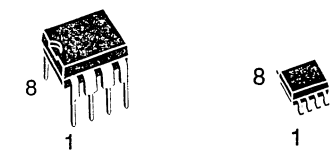


SO-a

Drawing is not to scale.

4K/2K/1K Serial SPI EEPROM with Positive Clock Strobe

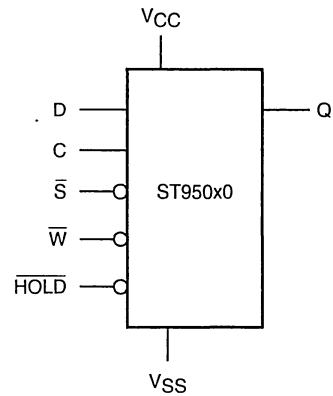
- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  - 4.5V to 5.5V for ST950x0
  - 2.5V to 5.5V for ST950x0W
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 2 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- SUPPORTS POSITIVE CLOCK SPI MODES



PSDIP8 (B)
0.25mm Frame

SO8 (M)
150mil Width

Figure 1. Logic Diagram



DESCRIPTION

The ST950x0 is a family of Electrically Erasable Programmable Memories (EEPROM) fabricated with STMicroelectronics's High Endurance Single Polysilicon CMOS technology. Each memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q).

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

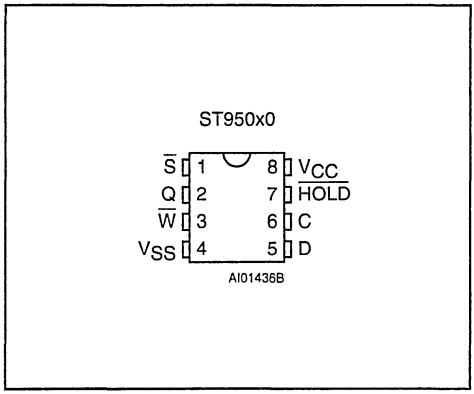


Figure 2B. SO Pin Connections

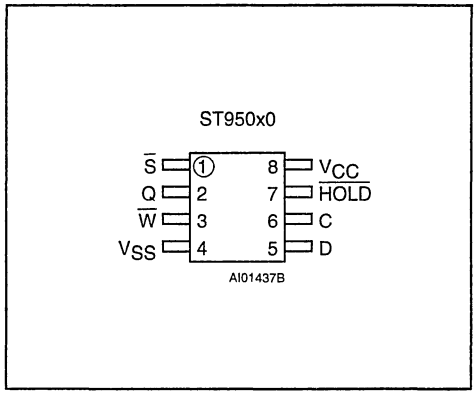


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			–40 to 125	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to V_{CC} +0.6	V
V_I	Input Voltage with respect to Ground			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0Ω)

DESCRIPTION (cont'd)

The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$). The write operation is disabled by a write protect input ($\overline{W}$).

Data is clocked in during the low to high transition of clock C, data is clocked out during the high to low transition of clock C.

SIGNALS DESCRIPTION

Serial Output (Q). The output pin is used to transfer data serially out of the Memory. Data is shifted out on the falling edge of the serial clock.

Serial Input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Input is latched on the rising edge of the serial clock.

Figure 3. Data and Clock Timing

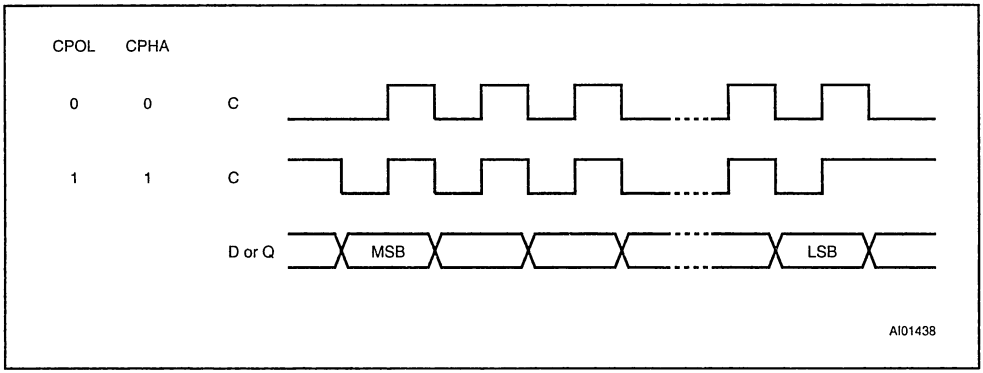
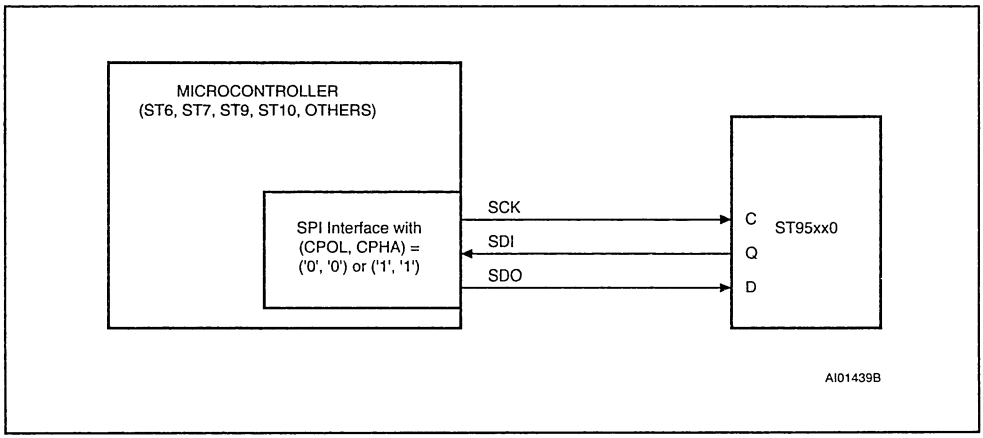


Figure 4. Microcontroller and SPI Interface Set-up



Serial Clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched on the rising edge of the clock input, while data on the Q pin changes after the falling edge of the clock input.

Chip Select ($\overline{S}$). When $\overline{S}$ is high, the Memory is deselected and the Q output pin is at high impedance and, unless an internal write operation is underway the Memory will be in the standby power mode. $\overline{S}$ low enables the Memory, placing it in the active power mode. It should be noted that after power-on, a high to low transition on $\overline{S}$ is required prior to the start of any operation.

Write Protect ($\overline{W}$). This pin is for hardware write protection. When $\overline{W}$ is low, writes to the Memory are disabled but any other operations stay enabled. When $\overline{W}$ is high, all writes operations are available. $\overline{W}$ going low at any time before the last bit D0 of the data stream will reset the write enable latch and prevent programming. No action on $\overline{W}$ or on the write enable latch can interrupt a write cycle which has commenced.

Hold ($\overline{HOLD}$). The $\overline{HOLD}$ pin is used to pause serial communications with the Memory without resetting the serial sequence. To take the Hold condition into account, the product must be selected ($\overline{S}$ = 0). Then the Hold state is validated by a high to low transition on $\overline{HOLD}$ when C is low. To resume the communications, $\overline{HOLD}$ is brought high while C is low. During the Hold condition D, Q, and C are at a high impedance state.

When the Memory is under the Hold condition, it is possible to deselect the device. However, the serial communications will remain paused after a reselect, and the chip will be reset.

The Memory can be driven by a microcontroller with its SPI peripheral running in either of the two following modes: (CPOL, CPHA) = ('0', '0') or (CPOL, CPHA) = ('1', '1').

For these two modes, input data is latched in by the low to high transition of clock C, and output data is available from the high to low transition of Clock (C).

The difference between (CPOL, CPHA) = (0, 0) and (CPOL, CPHA) = (1, 1) is the stand-by polarity: C remains at '0' for (CPOL, CPHA) = (0, 0) and C remains at '1' for (CPOL, CPHA) = (1, 1) when there is no data transfer.

OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first rising edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 3 shows the instruction set and format for device operation. If an invalid instruction is sent (one not contained in Table 3), the chip is automatically deselected. For operations that read or write data in the memory array, bit 3 of the instruction is the MSB of the address, otherwise, it is a don't care.

Write Enable (WREN) and Write Disable (WRDI)

The Memory contains a write enable latch. This latch must be set prior to every WRITE or WRSR operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under the following conditions:

- $\overline{W}$ pin is low
- Power on
- WRDI instruction executed
- WRSR instruction executed
- WRITE instruction executed

As soon as the WREN or WRDI instruction is received by the memory, the circuit executes the instruction and enters a wait mode until it is deselected.

Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write to the memory operation. If a Read Status register reaches the 8th bit of the Status register, an additional 9th clock pulse will wrap around to read the 1st bit of the Status Register

The status register format is as follows:

b7							b0
1	1	1	1	BP1	BP0	WEL	WIP

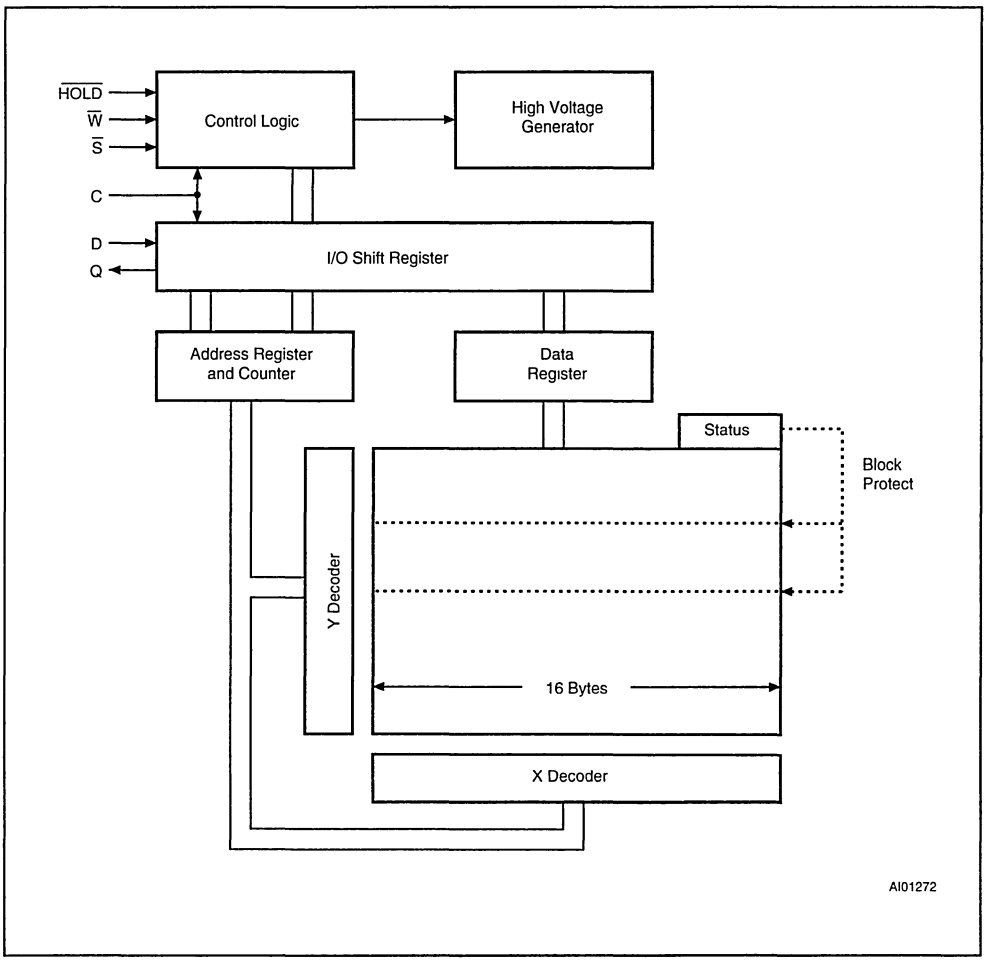
BP1, BP0: Read and write bits
WEL, WIP: Read only bits
b7 to b4: Read only bits.

Table 3. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	0000 0110
WRDI	Reset Write Enable Latch	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read Data from Memory Array	0000 $A_8$011
WRITE	Write Data to Memory Array	0000 $A_8$010

Notes: A_8 = 1, Upper page selected on ST95040
A_8 = 0, Lower page selected on ST95040.

Figure 5. Block Diagram

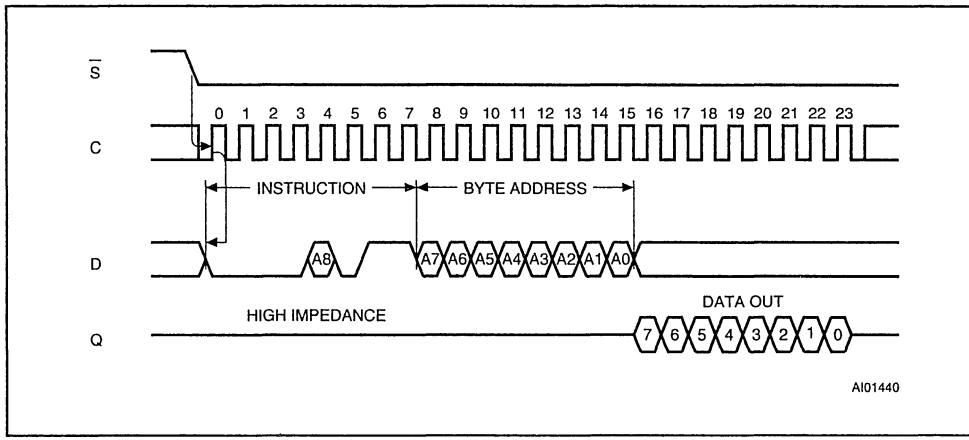


During a write to the memory operation to the memory array, all bits BP1, BP0, WEL, WIP are valid and can be read. During a write to the status register, only the bits WEL and WIP are valid and can be read. The values of BP1 and BP0 read at that time correspond to the previous contents of the status register.

The Write-In-Process (WIP) read-only bit indicates whether the Memory is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress.

The Write Enable Latch (WEL) read-only bit indicates the status of the write enable latch. When set to a '1' the latch is set, when set to a '0' the latch is reset. The Block Protect (BP0 and BP1) bits indicate the extent of the protection employed. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

Figure 6. Read Operation Sequence



Notes: A8 = A7 = 0 on ST95010, A8 = 0 on ST95020; A8 is only active on ST95040.

Table 4. Write Protected Block Size

Status Register Bits		Protected Block	Array Address Protected		
BP1	BP0		ST95040	ST95020	ST95010
0	0	none	none	none	none
0	1	Upper quarter	180h - 1FFh	C0h - FFh	60h - 7Fh
1	0	Upper half	100h - 1FFh	80h - FFh	40h - 7Fh
1	1	Whole memory	000h - 1FFh	00h - FFh	00h - 7Fh

Write Status Register (WRSR)

The WRSR instruction allows the user to select the size of protected memory. The user may read the blocks but will be unable to write within the protected blocks. The blocks and respective WRSR control bits are shown in Table 4.

When the WRSR instruction and the 8 bits of the Status Register are latched-in, the internal write cycle is then triggered by the rising edge of $\overline{S}$.

This rising edge of $\overline{S}$ must appear no later than the 16th clock cycle of the WRSR instruction of the Status Register content (it must not appear a 17th clock pulse before the rising edge of $\overline{S}$), otherwise the internal write sequence is not performed.

Read Operation

The chip is first selected by putting $\overline{S}$ low. The serial one byte read instruction is followed by a one byte address (A7-A0), each bit being latched-in during the rising edge of the clock (C). Bit 3 (see Table 3) of the read instruction contains address bit A8 (most significant address bit). Then the data stored in the memory at the selected address is shifted out on the Q output pin; each bit being shifted out during the falling edge of the clock (C). The data stored in the memory at the next address can be read in sequence by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to 0h allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during a write cycle will be rejected and will deselect the chip.

Figure 7. Write Enable Latch Sequence

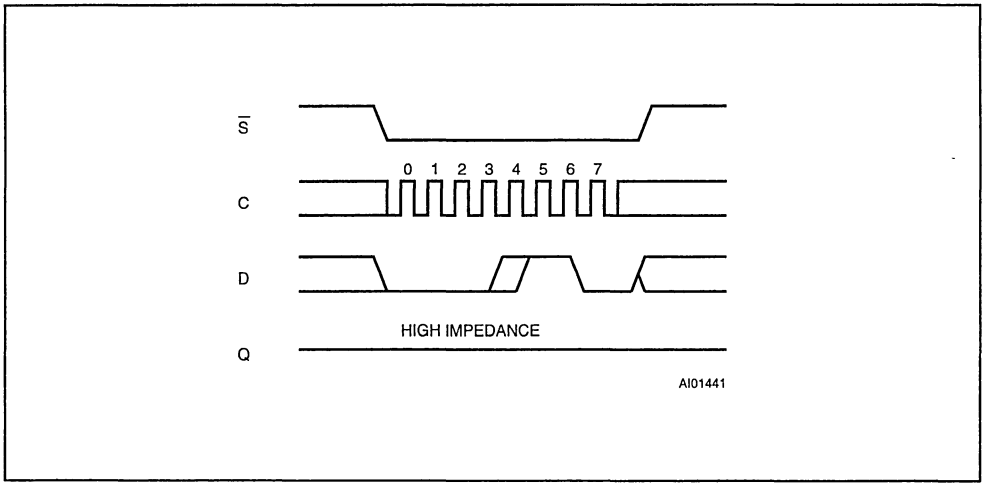
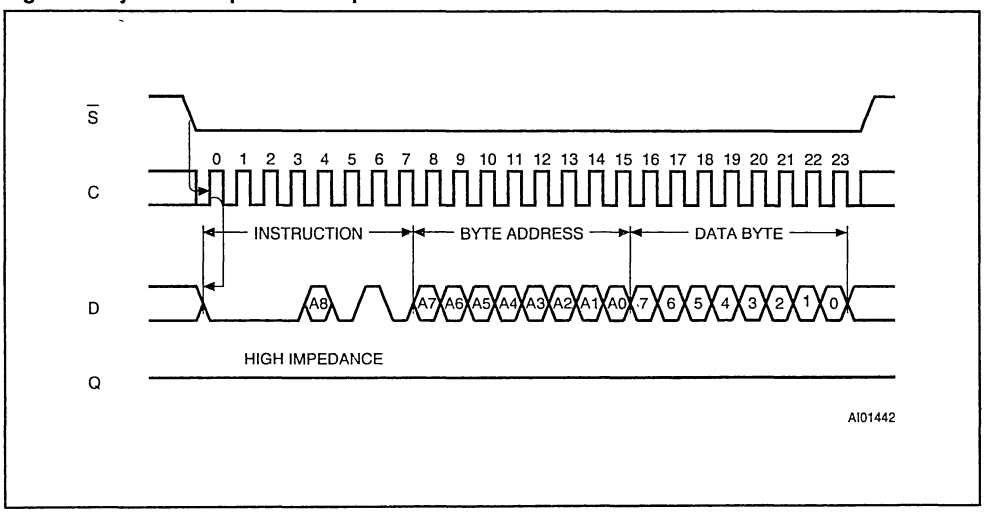
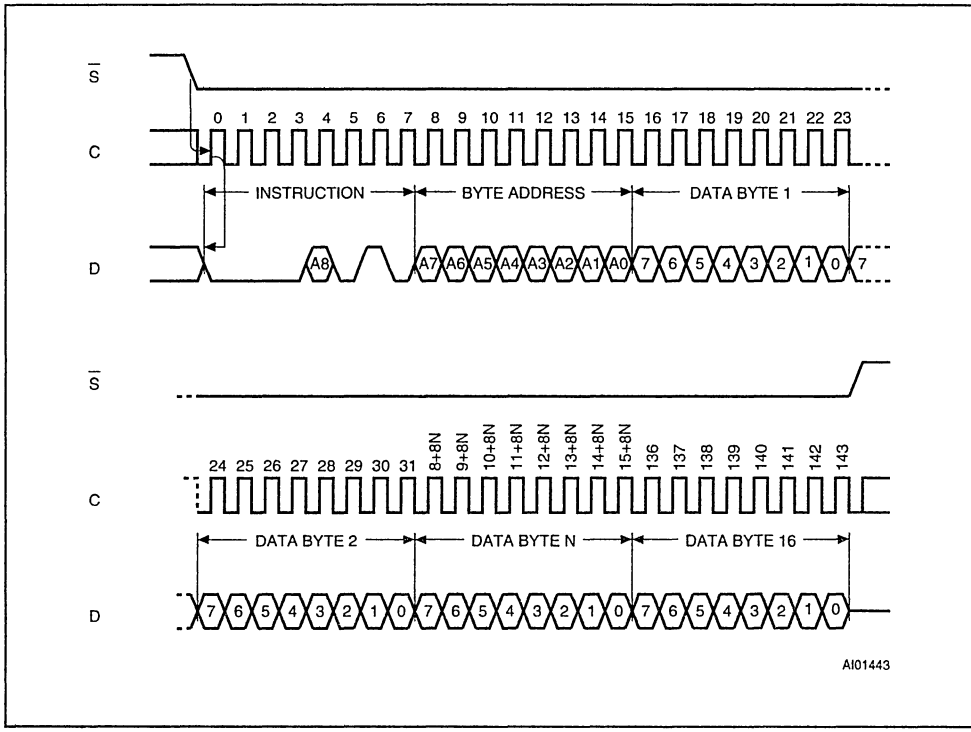


Figure 8. Byte Write Operation Sequence



Notes: A8 = A7 = 0 on ST95010; A8 = 0 on ST95020; A8 is only active on ST95040.

Figure 9. Page Write Operation Sequence



Notes: A8 = A7 = 0 on ST95010; A8 = 0 on ST95020; A8 is only active on ST95040.

Figure 10. RDSR: Read Status Register Sequence

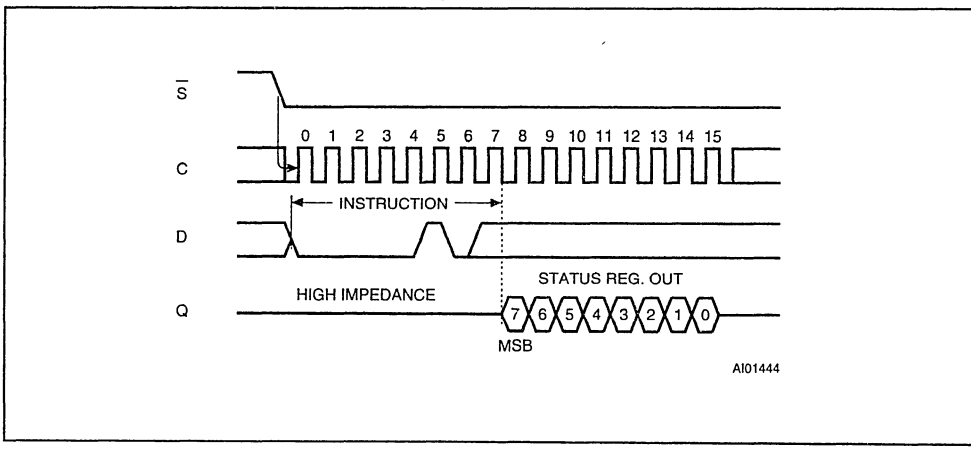
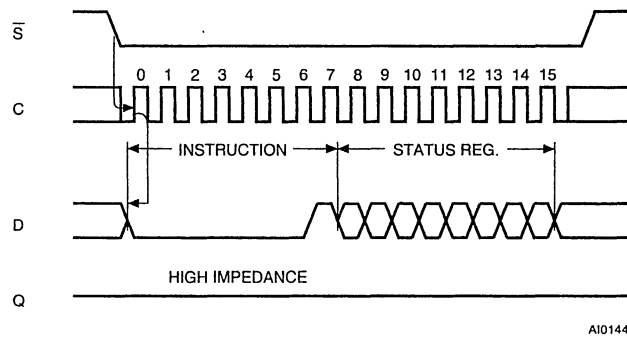


Figure 11. WRSR: Write Status Register Sequence



Byte Write Operation

Prior to any write attempt, the write enable latch must be set by issuing the WREN instruction. First the device is selected ($\overline{S}$ = low) and a serial WREN instruction byte is issued. Then the product is deselected by taking $\overline{S}$ high. After the WREN instruction byte is sent, the Memory will set the write enable latch and then remain in standby until it is deselected. Then the write state is entered by selecting the chip, issuing two bytes of instruction and address, and one byte of data.

Chip Select ($\overline{S}$) must remain low for the entire duration of the operation. The product must be deselected just after the eighth bit of data has been latched in. If not, the write process is cancelled. As soon as the product is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read to check BP1, BP0, WEL and WIP. WIP is high during the self-timed write cycle. When the cycle is completed, the write enable latch is reset.

Page Write Operation

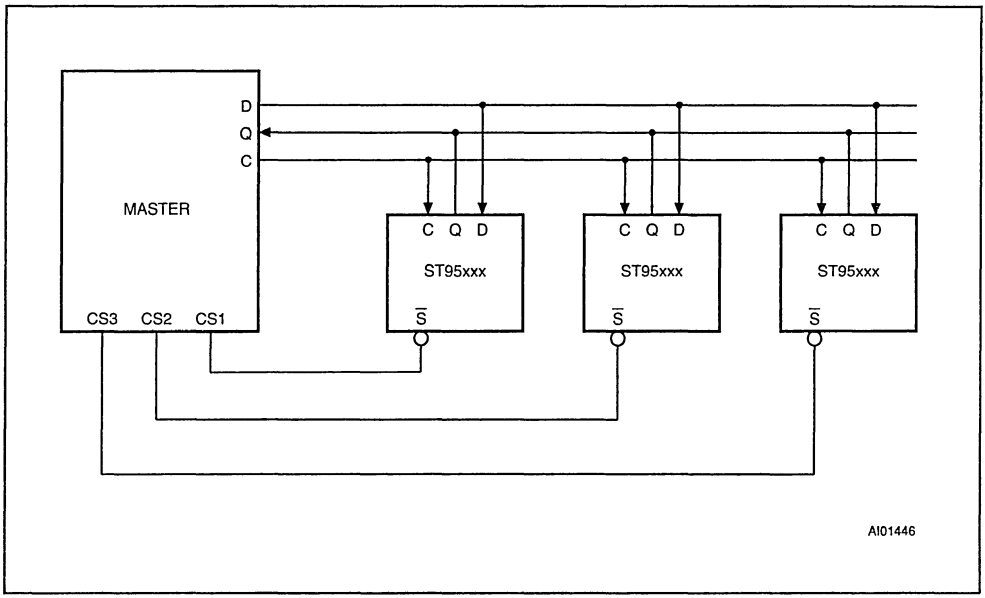
A maximum of 16 bytes of data may be written during one non-volatile write cycle. All 16 bytes must reside on the same page. The page write mode is the same as the byte write mode except that instead of deselecting the device after the first byte of data, up to 15 additional bytes can be shifted in prior to deselecting the chip. A page address begins with address xxxx 0000 and ends with xxxx 1111. If the address counter reaches xxxx 1111 and the clock continues, the counter will roll over to the first address of the page (xxxx 0000) and overwrite any previously written data. The programming cycle will only start if the $\overline{S}$ transition occurs just after the eighth bit of data of a word is received.

POWER ON STATE

After a Power up the Memory is in the following state:

- The device is in the low power standby state.
- The chip is deselected.
- The chip is not in hold condition.
- The write enable latch is reset.
- BP1 and BP0 are unchanged (non-volatile bits).

Figure 12. EEPROM and SPI Bus



DATA PROTECTION AND PROTOCOL SAFETY

- All inputs are protected against noise, see Table 6.
- Non valid $\overline{S}$ and $\overline{HOLD}$ transitions are not taken into account.
- $\overline{S}$ must come high at the proper clock count in order to start a non-volatile write cycle (in the memory array or in the status register), that is the Chip Select $\overline{S}$ must rise during the clock pulse following the introduction of a multiple of 8 bits.
- Access to the memory array during non-volatile programming cycle is ignored; however, the programming cycle continues.
- After any of the operations WREN, WRDI, RDSR is completed, the chip enters a wait state and waits for a deselect.
- The write enable latch is reset upon power-up.
- The write enable latch is reset when $\overline{W}$ is brought low.

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state (all data set at all "1's" or FFh). The block protect bits are initialized to 00.

Table 5. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$
Output Load	C_L = 100pF

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 13. AC Testing Input Output Wavef.

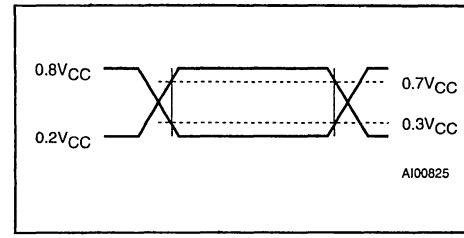


Table 6. Input Parameters (1) (T_A = 25 °C, f = 2 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (D)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF
t_{LPF}	Input Signal Pulse Width Filtered Out		10	ns

Note: 1. Sampled only, not 100% tested.

Table 7. DC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			±2	µA
I_{LO}	Output Leakage Current			±2	µA
I_{CC}	Supply Current	C = 0.1 V_{CC}/0.9 V_{CC}, @ 2 MHz, Q = Open		2	mA
		C = 0.1 V_{CC}/0.9 V_{CC}, @ 2 MHz, Q = Open, Note 2		2	mA
	Supply Current (W series)	C = 0.1 V_{CC}/0.9 V_{CC}, @ 1 MHz, V_{CC} = 2.5V, Q = Open		1.5	mA
I_{CC1}	Standby Current	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		50	µA
		$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, Note 2		50	µA
	Standby Current (W series)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V		25	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{OL} (1)	Output Low Voltage	I_{OL} = 2mA		0.4	V
		I_{OL} = 2mA, Note 2		0.4	V
	Output Low Voltage (W series)	I_{OL} = 1.5mA, V_{CC} = 2.5V		0.4	V
V_{OH} (1)	Output High Voltage	I_{OH} = –2mA	V_{CC} –0.6		V
		I_{OH} = –2mA, Note 2	V_{CC} –0.6		V
	Output High Voltage (W series)	I_{OH} = –0.4mA, V_{CC} = 2.5V	V_{CC} –0.3		V

Notes: 1. The device meets output requirements for both TTL and CMOS standards.
2. Test performed at –40 to 125°C temperature range, grade 3.

Table 8. AC Characteristics

Symbol	Alt	Parameter	ST95040 / 020 / 010						Unit
			V_{CC} = 4.5V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		V_{CC} = 4.5V to 5.5V, T_A = –40 to 125°C		V_{CC} = 2.5V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		
			Min	Max	Min	Max	Min	Max	
f_C	f_C	Clock Frequency	D.C.	2	D.C.	2	D.C.	1	MHz
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time	100		100		200		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	100		100		200		ns
t_{CH} (1)	t_{CLH}	Clock High Time	190		200		400		ns
t_{CL} (1)	t_{CLL}	Clock Low Time	200		200		400		ns
t_{CLCH}	t_{RC}	Clock Rise Time		1		1		1	µs
t_{CHCL}	t_{FC}	Clock Fall Time		1		1		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	50		50		100		ns
t_{CHDX}	t_{DH}	Data In Hold Time	50		50		100		ns
t_{DLDH}	t_{RI}	Data In Rise Time		1		1		1	µs
t_{DHDL}	t_{FI}	Data In Fall Time		1		1		1	µs
t_{HHCH}	t_{HSU}	$\overline{HOLD}$ Setup Time	100		100		200		ns
t_{HLCH}		Clock Low Hold Time	90		90		200		ns
t_{CLHL}	t_{HH}	$\overline{HOLD}$ Hold Time	80		80		200		ns
t_{CLHH}		Clock Low Set-up Time	100		100		200		ns
t_{CHSH}		$\overline{S}$ Active Hold Time	200		200		200		ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time	100		100		200		ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect Time	200		200		200		ns
t_{SHQZ}	t_{DIS}	Output Disable Time		150		150		200	ns
t_{CLQV}	t_V	Clock Low to Output Valid		240		300		400	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		0		ns
t_{QLQH} (2)	t_{RO}	Output Rise Time		100		100		200	ns
t_{QHQL} (2)	t_{FO}	Output Fall Time		100		100		200	ns
t_{HHQX}	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		100		100		200	ns
t_{HLQZ}	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		130		130		200	ns
t_W	t_{WP}	Write Cycle Time		10		10		10	ms

Notes: 1. $t_{CH} + t_{CL} \geq 1/fc$
2. Value guaranteed by characterization, not 100% tested in production.

Figure 14. Serial Input Timing

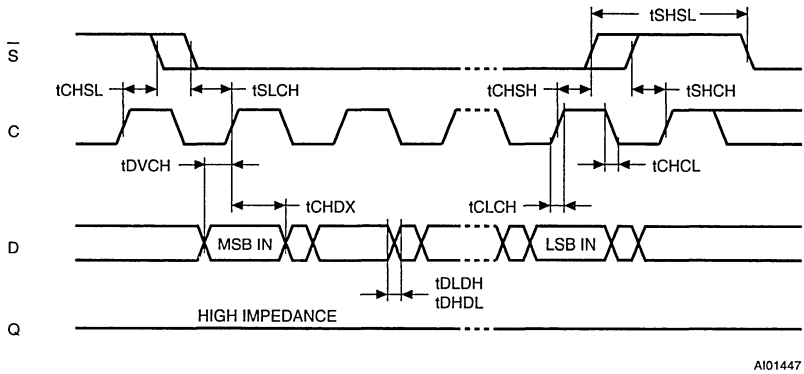


Figure 15. Hold Timing

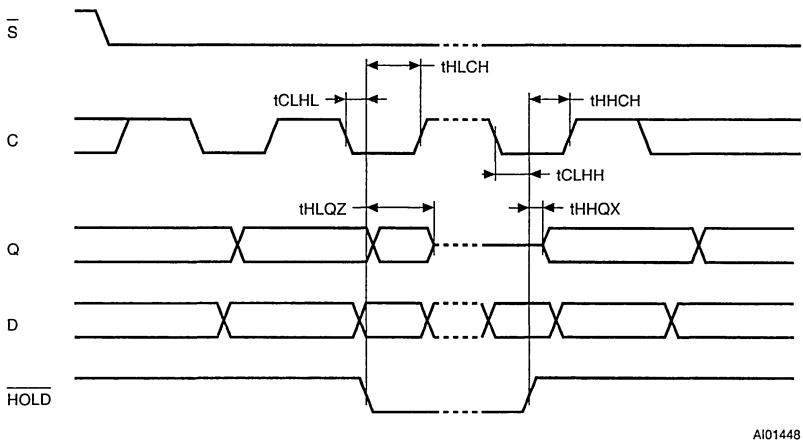
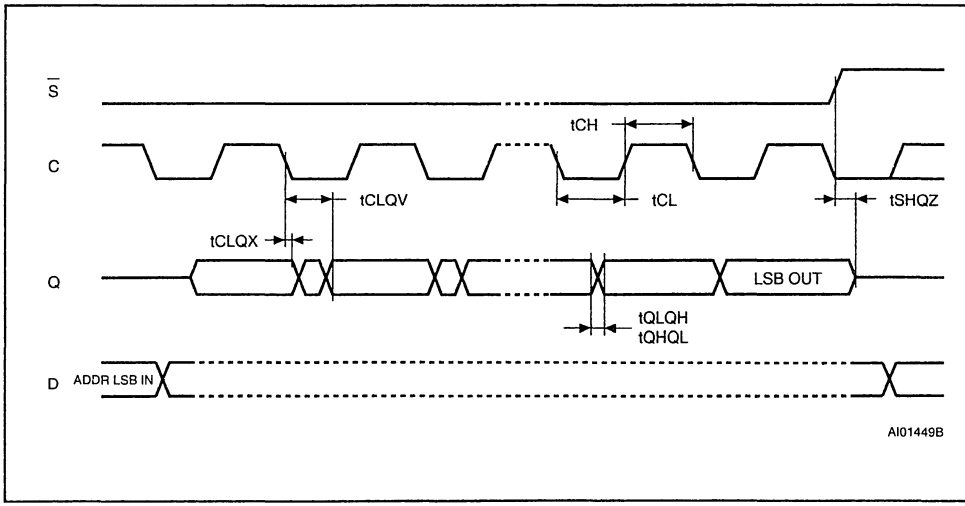
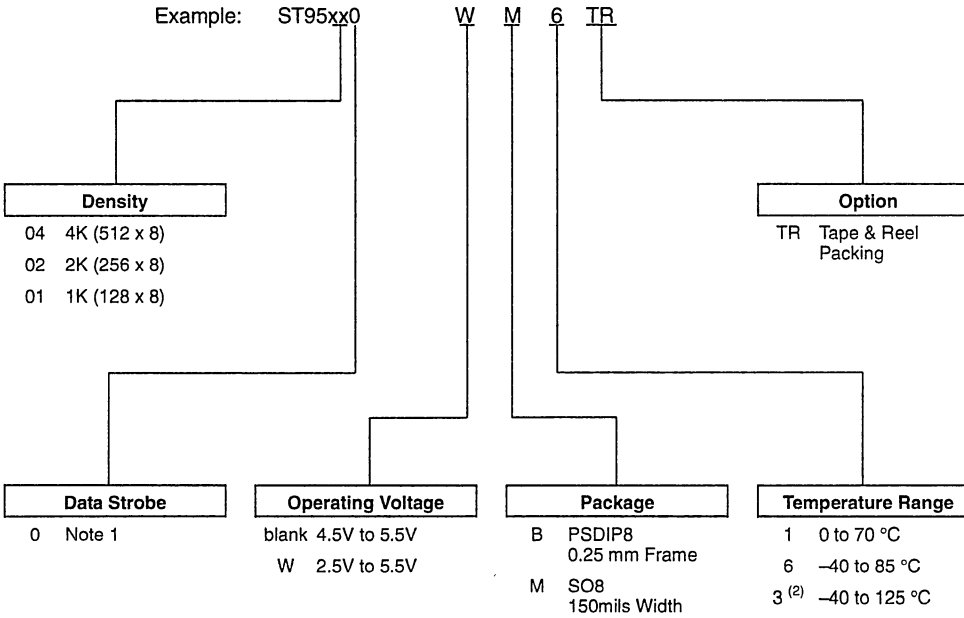


Figure 16. Output Timing



ORDERING INFORMATION SCHEME



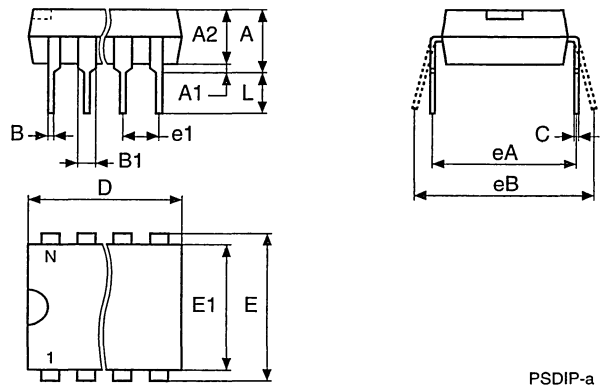
Notes: 1. Data In is strobed on rising edge of the clock (C) and Data Out is synchronized from the falling edge of the clock.
2. Temperature range on request only, 5V ± 10% only.

Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N		8			8	
CP			0.10			0.004

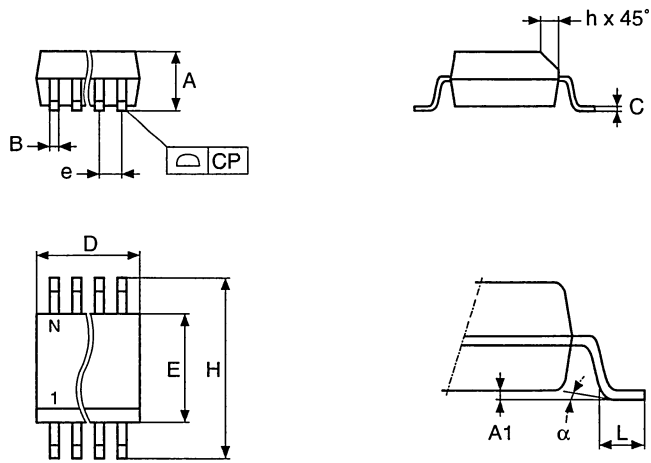


PSDIP-a

Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

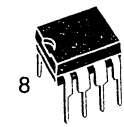


SO-a

Drawing is not to scale

8 Kbit Serial SPI EEPROM with Positive Clock Strobe

- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE 3V to 5.5V SUPPLY VOLTAGE
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 2 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- SUPPORTS POSITIVE CLOCK SPI MODES



PSDIP8 (B)
0.25mm Frame

SO8 (M)
150mil Width

DESCRIPTION

The ST95P08 is an 8 Kbit Electrically Erasable Programmable Memory (EEPROM) fabricated with STMicroelectronics's High Endurance Single Polysilicon CMOS technology. The 8 Kbit memory is organised as 64 pages of 16 bytes. The memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q). The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$). The write operation is disabled by a write protect input ($\overline{W}$).

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

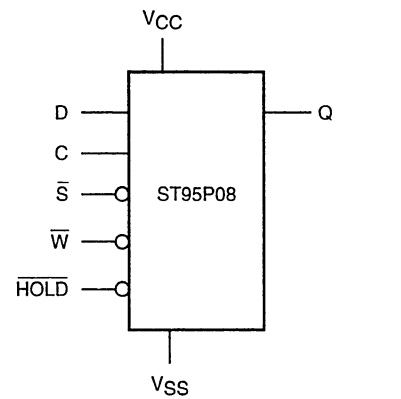


Figure 2A. DIP Pin Connections

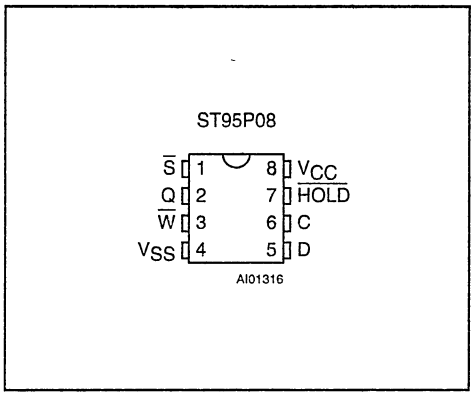


Figure 2B. SO Pin Connections

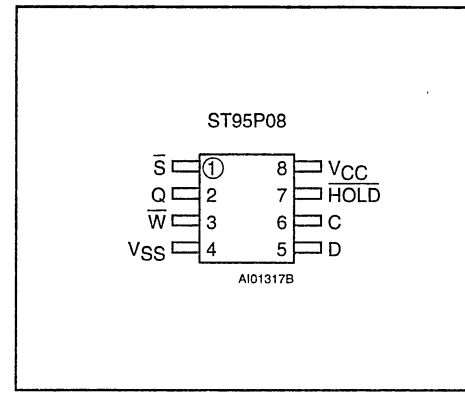


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature (2)			–40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to V_{CC} +0.6	V
V_I	Input Voltage			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (3)			4000	V
	Electrostatic Discharge Voltage (Machine model) (4)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Depends on range.
3 MIL-STD-883C, 3015.7 (100pF, 1500Ω)
4 EIAJ IC-121 (Condition C) (200pF, 0Ω)

SIGNALS DESCRIPTION

Serial Output (Q). The output pin is used to transfer data serially out of the ST95P08. Data is shifted out on the falling edge of the serial clock.

Serial Input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and data to be written. Input is latched on the rising edge of the serial clock.

Serial Clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched on the rising edge of the clock input, while data on the Q pin changes after the falling edge of the clock input.

Chip Select ($\overline{S}$). This input is used to select the ST95P08. The chip is selected by a high to low transition on the $\overline{S}$ pin when C is at '0' state. At any time, the chip is deselected by a low to high transition on the $\overline{S}$ pin when C is at '0' state. As soon as the chip is deselected, the Q pin is at high impedance state. This pin allows multiple ST95P08 to share the same SPI bus. After power up, the chip is at the deselect state. Transition of $\overline{S}$ are ignored when C is at '1' state.

Figure 3. Block Diagram

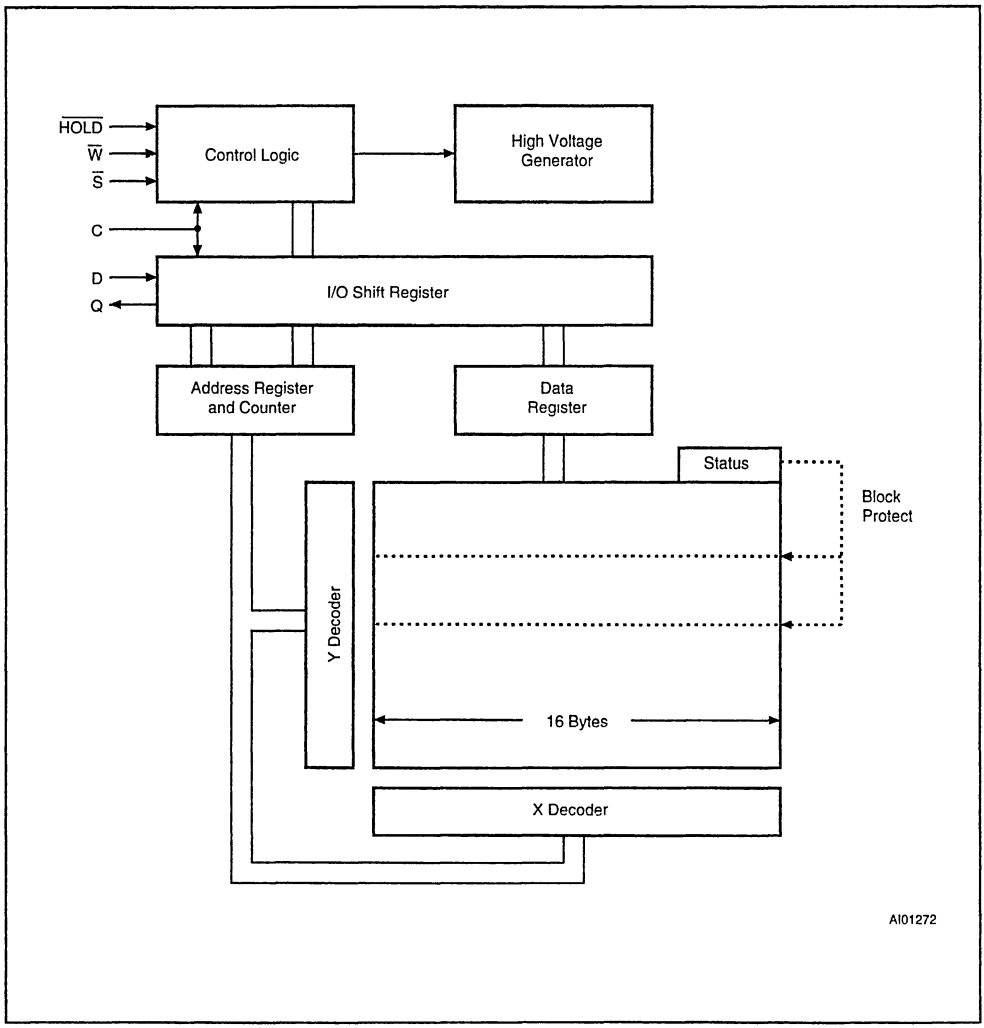


Table 3. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Input Output Waveforms

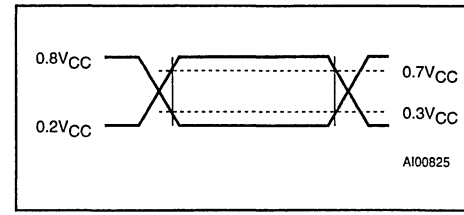


Table 4. Input Parameters (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (D)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF
t_{LPF}	Input Signal Pulse Width		10	ns

Note: 1. Sampled only, not 100% tested.

Table 5. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			2	µA
I_{LO}	Output Leakage Current			±2	µA
I_{CC}	V_{CC} Supply Current (Active)	C = 0.1 V_{CC}/0.9 V_{CC} , @ 2 MHz, Q = Open		2	mA
I_{CC1}	V_{CC} Supply Current (Standby)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5V		50	µA
		$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 3V		10	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA		0.2 V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = –2mA	0.8 V_{CC}		V

Table 6. AC Characteristics
(T_A = 0 to 70°C or −40 to 85°C; V_{CC} = 3V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
f_C	f_C	Clock Frequency		D.C.	2	MHz
t_{SLCH}	t_{SU}	$\overline{S}$ Setup Time		50		ns
t_{CLSH}	t_{SH}	$\overline{S}$ Hold Time		50		ns
t_{CH}	t_{WH}	Clock High Time		200		ns
t_{CL}	t_{WL}	Clock Low Time		300		ns
t_{CLCH}	t_{RC}	Clock Rise Time			1	µs
t_{CHCL}	t_{FC}	Clock Fall Time			1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time		50		ns
t_{CHDX}	t_{DH}	Data In Hold Time		50		ns
t_{DLDH}	t_{RI}	Data In Rise Time			1	µs
t_{DHDL}	t_{FI}	Data In Fall Time			1	µs
t_{HXCH}	t_{HSU}	$\overline{HOLD}$ Setup Time		50		ns
t_{CLHX}	t_{HH}	$\overline{HOLD}$ Hold Time		50		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	4.5V < V_{CC} < 5.5V	200		ns
			3V < V_{CC} < 4.5V	250		ns
t_{SHQZ}	t_{DIS}	Output Disable Time			150	ns
t_{QVCL}	t_V	Clock Low to Output Valid			300	ns
t_{CLQX}	t_{HO}	Output Hold Time		0		ns
t_{QLQH}	t_{RO}	Output Rise Time			100	ns
t_{QHQL}	t_{FO}	Output Fall Time			100	ns
t_{HHQX}	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z			150	ns
t_{HLQZ}	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z			150	ns
t_W (1)	t_W	Write Cycle Time			10	ms

Note: 1. Not enough characterisation data were available on this parameter at the time of issue this Data Sheet. The typical value is well below 5ms, the maximum value will be reviewed and lowered when sufficient data is available.

Figure 5. Output Timing

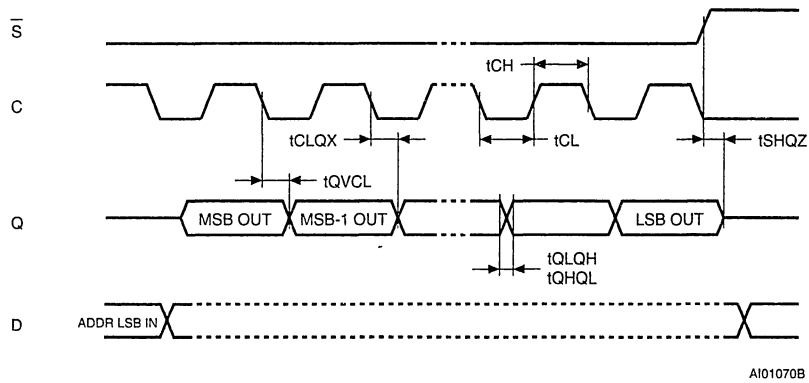


Figure 6. Serial Input Timing

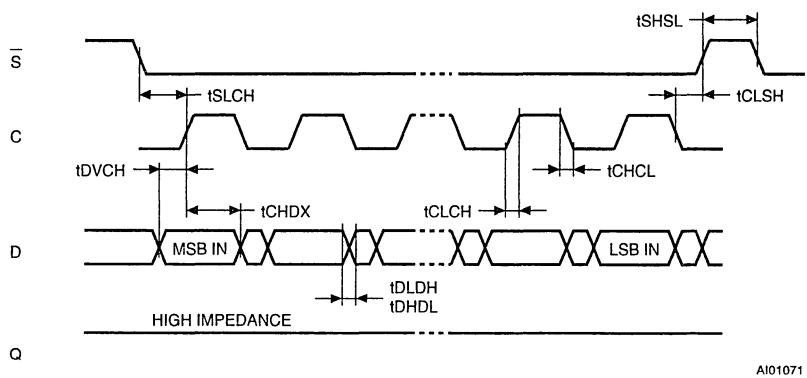
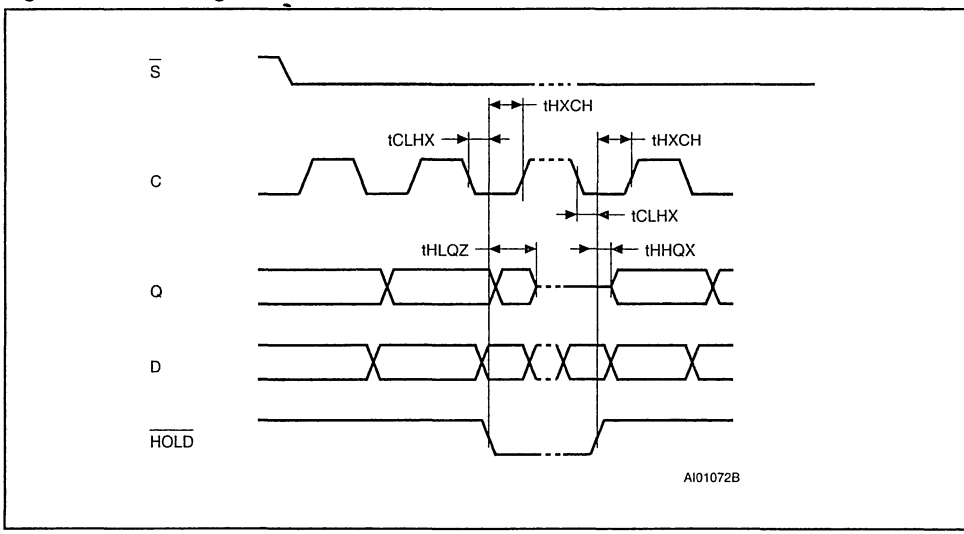


Figure 7. Hold Timing



Write Protect ($\overline{W}$). This pin is for hardware write protect. When $\overline{W}$ is low, non-volatile writes to the ST95P08 are disabled but any other operation stays enabled. When $\overline{W}$ is high, all operations including non-volatile writes are available. $\overline{W}$ going low at any time before the last bit D0 of the data stream will reset the write enable latch and prevent programming. No action on $\overline{W}$ or on the write enable latch can interrupt a write cycle which has commenced.

Hold ($\overline{HOLD}$). The $\overline{HOLD}$ pin is used to pause serial communications with a ST95P08 without resetting the serial sequence. To take the Hold condition into account, the product must be selected ($\overline{S}$ = 0). Then the Hold state is validated by a high to low transition on $\overline{HOLD}$ when C is low. To resume the communications, $\overline{HOLD}$ is brought high when C is low. During Hold condition D, Q, and C are at a high impedance state.

When the ST95P08 is under Hold condition, it is possible to deselect it. However, the serial communications will remain paused after a reselect, and the chip will be reset.

OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first rising edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 7 shows the instruction set and format for device operation. When an invalid instruction is sent (one not contained in Table 7), the chip is automatically deselected. For operations that read or write data in the memory array, bit 3 of the instruction is the MSB of the address, otherwise, it is a don't care.

Write Enable (WREN) and Write Disable (WRDI)

The ST95P08 contains a write enable latch. This latch must be set prior to every WRITE or WRSR operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under all the following conditions:

- $\overline{W}$ pin is low
- Power on
- WRDI instruction executed
- WRSR instruction executed
- WRITE instruction executed

As soon as the WREN or WRDI instruction is received by the ST95P08, the circuit executes the instruction and enters a wait mode until it is deselected.

Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a non-volatile write. As soon as the 8th bit of the status register is read out, the ST95P08 enters a wait mode (data on D are not decoded, Q is in Hi-Z) until it is deselected.

The status register format is as follows:

b7							b0
1	1	1	1	BP1	BP0	WEL	WIP

BP1, BP0: Read and write bits
WEL, WIP: Read only bits.

During a non-volatile write to the memory array, all bits BP1, BP0, WEL, WIP are valid and can be read. During a non volatile write to the status register, the only bits WEL and WIP are valid and can be read. The values of BP1 and BP0 read at that time correspond to the previous contents of the status register.

The Write-In-Process (WIP) read only bit indicates whether the ST95P08 is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress.

The Write Enable Latch (WEL) read only bit indicates the status of the write enable latch. When set to a '1' the latch is set, when set to a '0' the latch is reset.

The Block Protect (BP0 and BP1) bits indicate the extent of the protection employed. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

Write Status Register (WRSR)

The WRSR instruction allows the user to select the size of protected memory. The ST95P08 is divided into four 2048 bit blocks. The user may read the blocks but will be unable to write within the selected blocks.

The blocks and respective WRSR control bits are shown in Table 6.

When the WRSR instruction and the 8 bits of the Status Register are latched-in, the internal write cycle is then triggered by the rising edge of $\overline{S}$. This rising edge of $\overline{S}$ must appear after the 8th bit of the Status Register content (it must not appear a 17th clock pulse before the rising edge of $\overline{S}$), otherwise the internal write sequence is not performed.

Read Operation

The chip is first selected by putting $\overline{S}$ low. The serial one byte read instruction is followed by a one byte address (A7-A0), each bit being latched-in during the rising edge of the clock (C). Bit 3 and 4 of the read instruction contain address bits A9 and A8 (most significant address bits). These bits are used to select the first or second page of the device. Then, the data stored in the memory at the selected address is shifted out on the Q output pin; each bit being shifted out during the falling edge of the clock (C). The data stored in the memory at the next address can be read in sequence by continuing to provide clock pulses. The byte address is automat-

Table 7. Array Addresses Protect

Status Register Bits		Array Addresses Protected
BP1	BP0	
0	0	none
0	1	300h - 3FFh
1	0	200h - 3FFh
1	1	000h - 3FFh

Table 8. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	000X X110
WRDI	Reset Write Enable Latch	000X X100
RDSR	Read Status Register	000X X101
WRSR	Write Status Register	000X X001
READ	Read Data from Memory Array	000A A011
WRITE	Write Data to Memory Array	000A A010

Notes: A = 1, Upper page selected
A = 0, Lower page selected
X = Don't care

ically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (1FFh), the address counter rolls over to 0h allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during a non-volatile write cycle will be rejected and will deselect the chip.

Byte Write Operation

Prior to any write attempt, the write enable latch must have been set by issuing the WREN instruction. First, the device is selected ($\overline{S}$ = low) and a serial WREN instruction byte is issued. Then, the product is deselected by taking $\overline{S}$ high. After the WREN instruction byte is sent, the ST95P08 will set the write enable latch and then remain in standby until it is deselected. Then, the write state is entered by selecting the chip, issuing a one byte address (A7-A0), and one byte of data. Bits 3 and 4 of the write instruction contain address bits A9 and A8 (most significant address bits). $\overline{S}$ must remain low for the entire duration of the operation. The product must be deselected just after the eigth bit of data has been latched in. If not, the write process is cancelled. As soon as the product is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read to check BP1, BP0, WEL and WIP. WIP is high during the self-timed write cycle. When the cycle is close to completion, the write enable latch is reset.

Page Write Operation

A maximum of 16 bytes of data may be written during one non-volatile write cycle. All 16 bytes must reside on the same page. The page write mode is the same as the byte write mode except that instead of deselecting after the first byte of data, up to 15 additional bytes can be shifted in prior to deselecting the chip. A page address begins with address xxxx 0000 and ends with xxxx 1111. If the address counter reaches xxxx 1111 and the clock continues, the counter will roll over to the first address of the page (xxxx 0000) and overwrite any previous written data. The programming cycle will only start if the $\overline{S}$ transition does occur at the clock low pulse just after the eigth bit of data of a word is received.

Figure 8. Read Operation Sequence

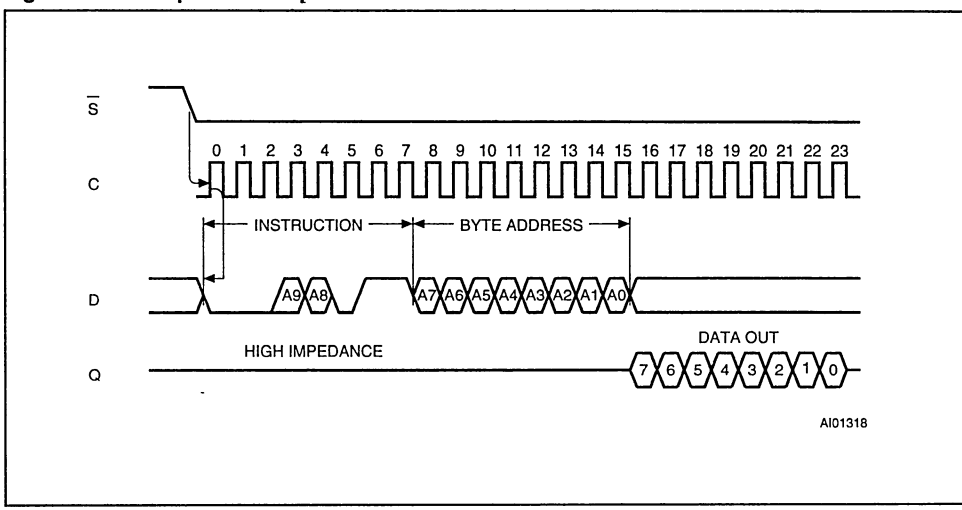


Figure 9. Write Enable Latch Sequence

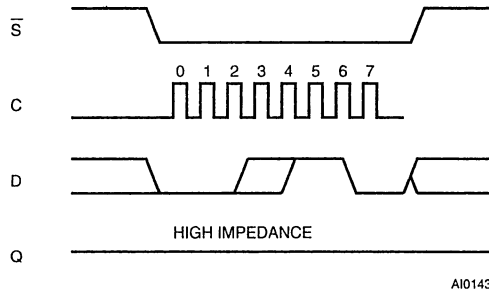


Figure 10. Write Operation Sequence

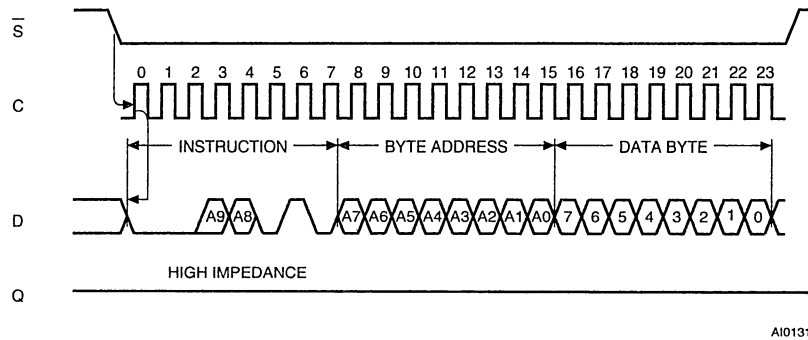


Figure 11. Page Write Operation Sequence

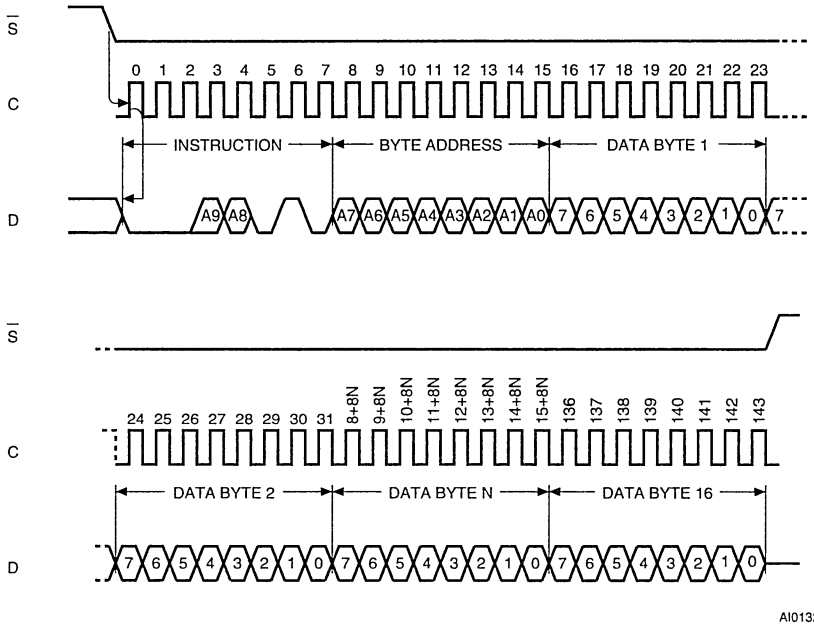


Figure 12. RDSR: Read Status Register Sequence

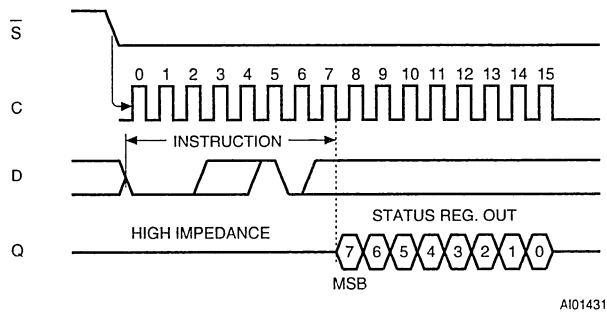
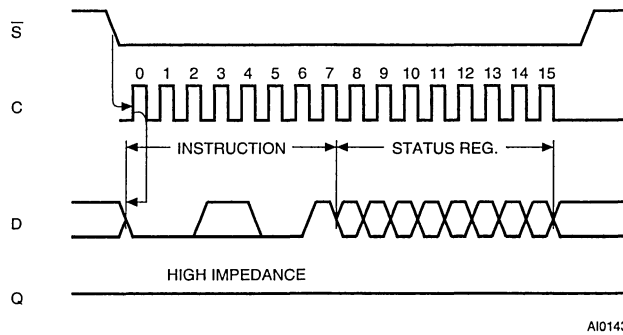


Figure 13. WRSR: Write Status Register Sequence



POWER ON STATE

After a Power up the ST95P08 is in the following state:

- The device is in the low power standby state.
- The chip is deselected.
- The chip is not in hold condition.
- The write enable latch is reset.
- BP1 and BP0 are unchanged (non-volatile bits).

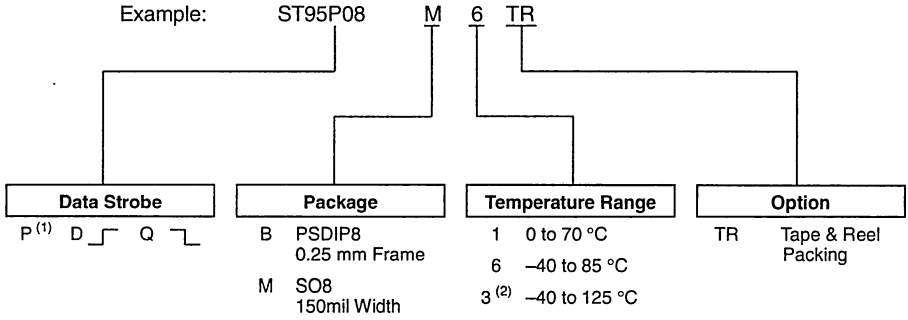
DATA PROTECTION AND PROTOCOL SAFETY

- All inputs are protected against noise, see Table 3.
- Non valid $\overline{S}$ and $\overline{HOLD}$ transitions are not taken into account.
- $\overline{S}$ must come high at the proper clock count in order to start a non-volatile write cycle (in the memory array or in the cycle status register). The Chip Select $\overline{S}$ must rise during the clock pulse following the introduction of a multiple of 8 bits.
- Access to the memory array during non-volatile programming cycle is cancelled and the chip is automatically deselected; however, the programming cycle continues.
- After either of the following operations (WREN, WRDI, RDSR) is completed, the chip enters a wait state and waits for a deselect.
- The write enable latch is reset upon power-up.
- The write enable latch is reset when $\overline{W}$ is brought low.

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state (all data set at all "1's" or FFh). The block protect bits are initialized to 00.

ORDERING INFORMATION SCHEME



Notes: 1. Data In strobed on rising edge of the clock (C) and Data Out synchronized from the falling edge of the clock
2. Temperature range on request only, 5V ± 10% only.

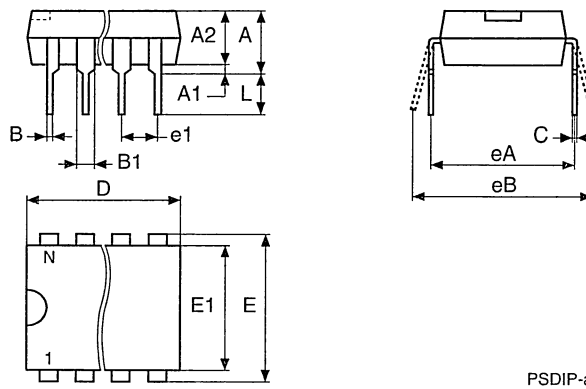
Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		
CP			0.10			0.004

PSDIP8

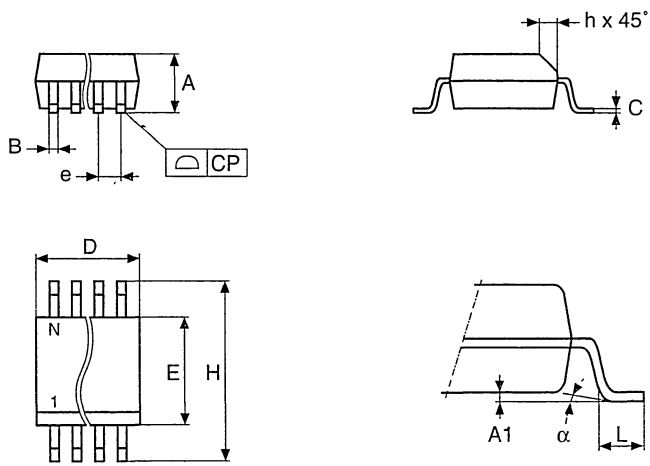


PSDIP-a

Drawing is not to scale.

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004



SO-a

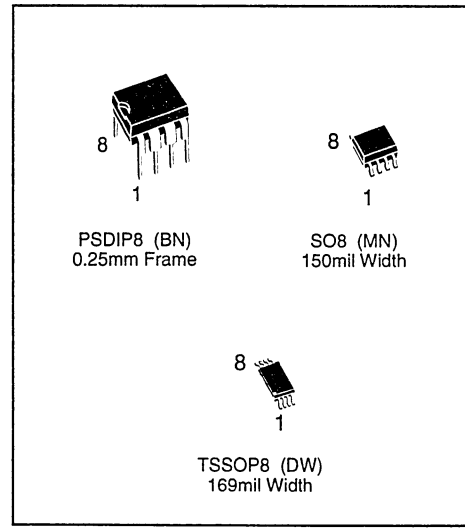
Drawing is not to scale.

SERIAL EEPROM, MICROWIRE BUS

M93C86, M93C76, M93C66
M93C56, M93C46, M93C06

16K/8K/4K/2K/1K/256 (x8/x16) Serial Microwire Bus EEPROM

- INDUSTRY STANDARD MICROWIRE BUS
- 1 MILLION ERASE/WRITE CYCLES, with 40 YEARS DATA RETENTION
- DUAL ORGANIZATION: by WORD (x16) or by BYTE (x8)
- BYTE/WORD and ENTIRE MEMORY PROGRAMMING INSTRUCTIONS
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for M93Cx6 version
  - 2.5V to 5.5V for M93Cx6-W version
  - 1.8V to 3.6V for M93Cx6-R version
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME
- ENHANCED ESD/LATCH-UP PERFORMANCES



DESCRIPTION

This M93C86/C76/C66/C56/C46/C06 specification covers a range of 16K/8K/4K/2K/1K/256 bit serial EEPROM products respectively. In this text, products are referred to as M93Cx6. The M93Cx6 is an Electrically Erasable Programmable Memory (EEPROM) fabricated with STMicroelectronics's High Endurance Single Polysilicon CMOS technology. The M93Cx6 memory is accessed through a serial input (D) and output (Q) using the MICROWIRE bus protocol.

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
ORG	Organisation Select
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

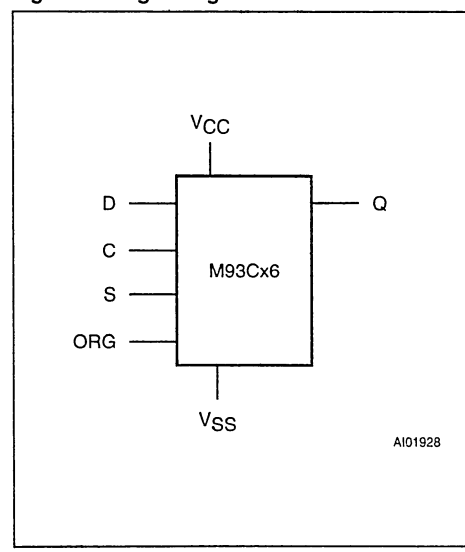
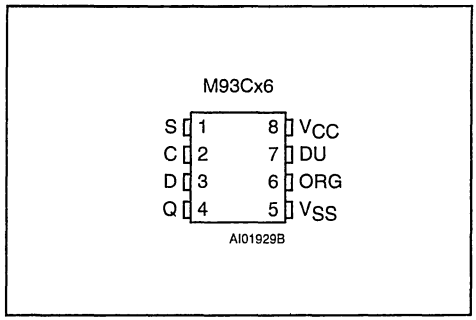
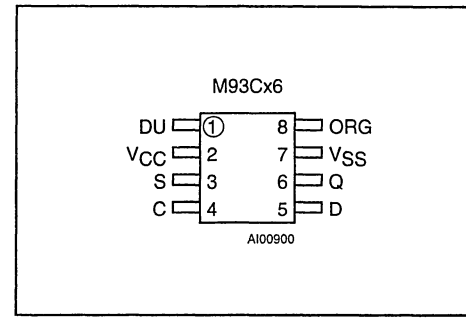


Figure 2A. DIP and SO Pin Connections



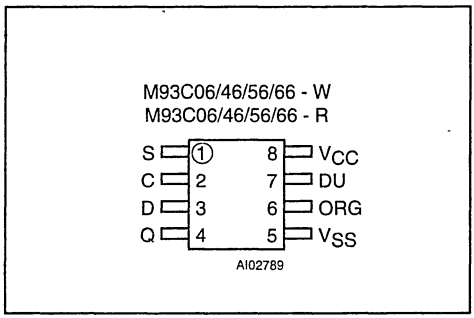
Warning: DU = Don't Use

Figure 2B. SO 90° Turn Pin Connections



Warning: DU = Don't Use

Figure 2C. TSSOP Pin Connections



Warning: DU = Don't Use

DESCRIPTION (cont'd)

The M93Cx6 specified at 5V±10%, the M93Cx6-W specified at 2.5V to 5.5V and the M93Cx6-R specified at 1.8V to 3.6V.

The M93Cx6 memory array organization may be divided into either bytes (x8) or words (x16) which may be selected by a signal applied on the ORG input. The M93C86/C76/C66/C56/C46/C06 is divided into either 2048/1024/512/256/128/32 x8 bit bytes or 1024/512/256/128/64/16 x16 bit words respectively. These memory devices are available in both PSDIP8, SO8 and TSSOP8 packages.

The M93Cx6 memory is accessed by a set of instructions which includes Read a Byte/Word, Write a Byte/Word, Erase a Byte/Word, Erase All and Write All. A Read instruction loads the address of the first byte/word to be read into an internal address pointer. The data contained at this address is then clocked out serially. The address pointer is automatically incremented after the data is output and, if the Chip Select input (S) is held High, the M93Cx6 can output a sequential stream of data bytes/words. In this way, the memory can be read as a data stream from 8 up to 16,384 bits long (for the M93C86 only), or continuously as the address counter automatically rolls over to '00' when the highest address is reached.

Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 8 or 16 bits at one time into one of the byte or word locations of the M93Cx6. After the start of the programming cycle, a Busy/Ready signal is available on the Data output (Q) when Chip Select (S) is driven High.

An internal feature of the M93Cx6 provides Power-on Data Protection by inhibiting any operation when the Supply is too low for reliable operation. The design of the M93Cx6 and the High Endurance CMOS technology used for its fabrication give an Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of 40 years.

The DU (Don't Use) pin does not affect the function of the memory. It is reserved for use by STMicroelectronics during test sequences. The pin may be left unconnected or may be connected to V_{CC} or V_{SS}. Direct connection of DU to V_{SS} is recommended for the lowest standby power consumption.

MEMORY ORGANIZATION

The M93Cx6 is organised in either bytes (x8) or words (x16). If the ORG input is left unconnected (or connected to V_{CC}) the x16 organization is selected; when ORG is connected to Ground (V_{SS}) the x8 organization is selected. When the M93Cx6 is in standby mode, the ORG input should be set to either V_{SS} or V_{CC} in order to achieve minimum power consumption. Any voltage between V_{SS} and V_{CC} applied to the ORG input pin may increase the standby current value.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			–40 to 125	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)			–0.3 to V_{CC} +0.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

Table 3. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages (M93Cxx)	0.4V to 2.4V
Input Pulse Voltages (M93Cxx-W, M93Cxx-R)	0.2V_{CC} to 0.8V_{CC}
Input Timing Reference Voltages (M93Cxx)	1.0V to 2.0V
Output Timing Reference Voltages (M93Cxx)	0.8V to 2.0V
Input and Output Timing Reference Voltages (M93Cxx-W, M93Cxx-R)	0.3V_{CC} to 0.7V_{CC}
Output Load	C_L = 100pF

Note that Output Hi-Z is defined as the point where data is no longer driven.

POWER-ON DATA PROTECTION

In order to prevent data corruption and inadvertent write operations during power-up, a Power On Reset (POR) circuit resets all internal programming circuitry and sets the device in the Write Disable mode.

- At Power-up and Power-down, the device must NOT be selected (that is, the S input must be driven low) until the supply voltage reaches the operating value V_{CC} specified in the AC and DC tables.
- When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction.

For the M93Cx6 specified at 5V, the POR threshold voltage is around 3V. For all the other M93Cx6 specified at low V_{CC} (with -W and -R V_{CC} range options), the POR threshold voltage is around 1.5V.

Figure 3. AC Testing Input Output Waveforms

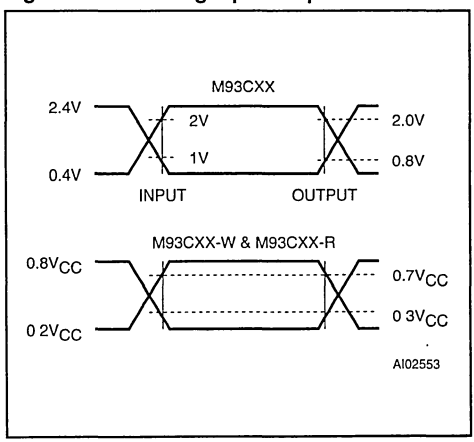


Table 4. Capacitance (1)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested.

Table 5A. DC Characteristics for M93CXX
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±2.5	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current	V_{CC} = 5V, S = V_{IH}, f = 1 MHz		1.5	mA
I_{CC1}	Supply Current (Standby)	V_{CC} = 5V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage (D, C, S)	V_{CC} = 5V ± 10%	–0.3	0.8	V
V_{IH}	Input High Voltage (D, C, S)	V_{CC} = 5V ± 10%	2	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 5V, I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 5V, I_{OH} = –400µA	2.4		V

Table 5B. DC Characteristics for M93CXX
(T_A = –40 to 125°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±2.5	µA
I_{LO}	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current	V_{CC} = 5V, S = V_{IH}, f = 1 MHz		1.5	mA
I_{CC1}	Supply Current (Standby)	V_{CC} = 5V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage (D, C, S)	V_{CC} = 5V ± 10%	–0.3	0.8	V
V_{IH}	Input High Voltage (D, C, S)	V_{CC} = 5V ± 10%	2	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 5V, I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 5V, I_{OH} = –400µA	2.4		V

Table 5C. DC Characteristics for M93CXX-W
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current (CMOS Inputs)	VCC = 5V, S = V_{IH}, f = 1 MHz		1.5	mA
		V_{CC} = 2.5V, S = V_{IH}, f = 1 MHz		1	mA
I_{CC1}	Supply Current (Standby)	VCC = 2.5V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		10	µA
V_{IL}	Input Low Voltage (D, C, S)		–0.3	0.2 V_{CC}	V
V_{IH}	Input High Voltage (D, C, S)		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 5V, I_{OL} = 2.1mA		0.4	V
		V_{CC} = 2.5V, I_{OL} = 100µA		0.2	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 5V, I_{OH} = –400µA	2.4		V
		V_{CC} = 2.5V, I_{OH} = –100µA	V_{CC} – 0.2		V

Table 5D. DC Characteristics for M93CXX-R (1)
(T_A = 0 to 70°C or –20 to 85°C; V_{CC} = 1.8V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current (CMOS Inputs)	VCC = 3.6V, S = V_{IH}, f = 1 MHz		1.5	mA
		V_{CC} = 1.8V, S = V_{IH}, f = 1 MHz		1	mA
I_{CC1}	Supply Current (Standby)	VCC = 1.8V, S = V_{SS}, C = V_{SS}, ORG = V_{SS} or V_{CC}		5	µA
V_{IL}	Input Low Voltage (D, C, S)		–0.3	0.2 V_{CC}	V
V_{IH}	Input High Voltage (D, C, S)		0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 1.8V, I_{OL} = 100µA		0.2	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 1.8V, I_{OH} = –100µA	V_{CC} – 0.2		V

Note: 1. This is preliminary data.

Table 6A. AC Characteristics

Symbol	Alt	Parameter	M93C86/76/66/56/46/06				Unit
			V_{CC} = 4.5V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		V_{CC} = 4.5V to 5.5V, T_A = –40 to 125°C		
			Min	Max	Min	Max	
t_{SHCH}	t_{CSS}	Chip Select Set-up Time M93C06, M39C46, M93C56, M93C66	50		50		ns
		Chip Select Set-up time M93C76, M93C86	100		100		ns
t_{CLSH}	t_{SKS}	Clock Set-up Time (relative to S)	100		100		ns
t_{DVCH}	t_{DIS}	Data In Set-up Time	100		100		ns
t_{CHDX}	t_{DIH}	Data In Hold Time	100		100		ns
t_{CHQL}	t_{PD0}	Delay to Output Low		400		400	ns
t_{CHQV}	t_{PD1}	Delay to Output Valid		400		400	ns
t_{CLSL}	t_{CSH}	Chip Select Hold Time	0		0		ns
t_{SLCH}		Chip Select Low to Clock High	250		250		ns
t_{SLSH} (1)	t_{CS}	Chip Select Low to Chip Select High	250		250		ns
t_{SHQV}	t_{SV}	Chip Select to Ready/Busy Status		400		400	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		200		200	ns
t_{CHCL} (2)	t_{SKH}	Clock High Time	250		250		ns
t_{CLCH} (2)	t_{SKL}	Clock Low Time	250		250		ns
t_W	t_{WP}	Erase/Write Cycle time		10		10	ms
f_C	f_{SK}	Clock Frequency	0	1	0	1	MHz

Notes: 1. Chip Select must be brought low for a minimum of tSLSH between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1/fC, therefore the sum of the timings tCHCL + tCLCH must be greater or equal to 1/fC.

Table 6B. AC Characteristics

Symbol	Alt	Parameter	M93C86/76/66/56/46/06				Unit
			V_{CC} = 2.5V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		V_{CC} = 1.8V to 3.6V,(3) T_A = 0 to 70°C, T_A = –20 to 85°C		
			Min	Max	Min	Max	
t_{SHCH}	t_{CSS}	Chip Select Set-up Time	100		200		ns
t_{CLSH}	t_{SKS}	Clock Set-up Time (relative to S)	100		100		ns
t_{DVCH}	t_{DIS}	Data In Set-up Time	100		100		ns
t_{CHDX}	t_{DIH}	Data In Hold Time	100		200		ns
t_{CHQL}	t_{PD0}	Delay to Output Low		400		700	ns
t_{CHQV}	t_{PD1}	Delay to Output Valid		400		700	ns
t_{CLSL}	t_{CSH}	Chip Select Hold Time	0		0		ns
t_{SLCH}		Chip Select Low to Clock High	250		250		ns
t_{SLSH} (1)	t_{CS}	Chip Select Low to Chip Select High	1000		1000		ns
t_{SHQV}	t_{SV}	Chip Select to Ready/Busy Status		400		700	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		200		200	ns
t_{CHCL} (2)	t_{SKH}	Clock High Time	350		800		ns
t_{CLCH} (2)	t_{SKL}	Clock Low Time	250		800		ns
t_W	t_{WP}	Erase/Write Cycle time		10		10	ms
f_C	f_{SK}	Clock Frequency	0	1	0	0.5	MHz

Notes: 1. Chip Select must be brought low for a minimum of tSLSH between consecutive instruction cycles.
2. The Clock frequency specification calls for a minimum clock period of 1/fC, therefore the sum of the timings tCHCL + tCLCH must be greater or equal to 1/fC.
3 This is preliminary data.

Figure 4. Synchronous Timing, Start and Op-Code Input

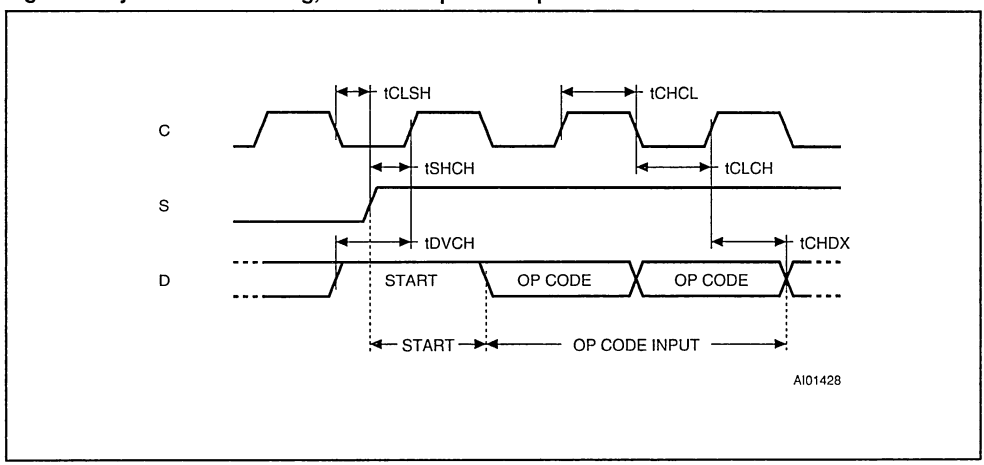
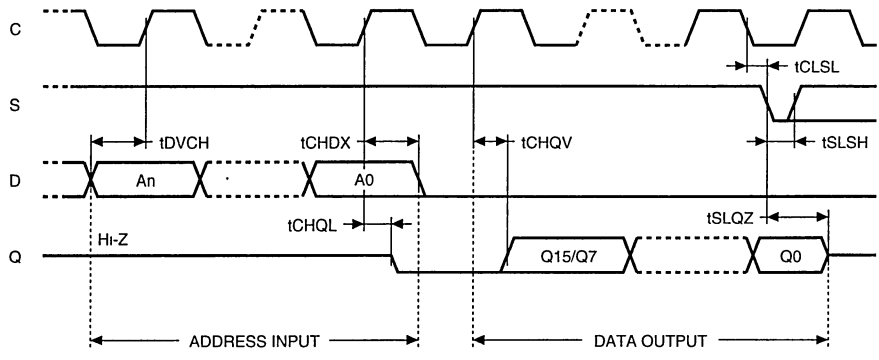
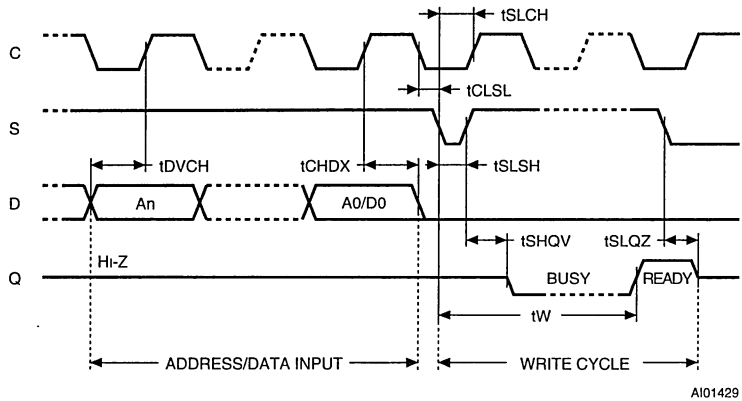


Figure 5. Synchronous Timing, Read or Write





INSTRUCTIONS

The M93C86/C76/C66/C56/C46/C06 have seven instructions, as shown in Table 7. Each instruction is preceded by the rising edge of the signal applied on the S input (assuming that the clock C is low). After the device is selected, the internal logic waits for the start bit, which defines the beginning of the instruction bit stream. The start bit is the first '1' read on the D input during the rising edge of the clock C. Following the start bit, the op-codes of the instructions are made up of the 2 following bits. Note that some instructions use only these first two bits, others use also the first two bits of the address to define the op-code. The op-code is then followed by the address of the byte/word to be accessed. For the M93C06 and M93C46, the address is made up of 6 bits for the x16 organization or 7 bits for the x8 organization (see Table 7A). For the M93C56 and M93C66, the address is made up of 8 bits for the x16 organization or 9 bits for the x8 organization (see Table 7B). For the M93C76 and M93C86, the address is made up of 10 bits for the x16 organization or 11 bits for the x8 organization (see Table 7C).

The M93Cx6 is fabricated in CMOS technology and is therefore able to run from 0Hz (static input signals) up to the maximum ratings (specified in Table 6).

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 8 bit byte or the 16 bit word with the MSB first. Output data changes are triggered by the Low to High transition of the Clock (C). The M93Cx6 will automatically increment the address and will clock out the next byte/word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between bytes/words and a continuous stream of data can be read.

Erase/Write Enable and Disable

The Erase/Write Enable instruction (EWEN) authorizes the following Erase/Write instructions to be executed. The Erase/Write Disable instruction (EWDS) disables the execution of the following Erase/Write instructions and the internal programming cycle cannot run. When power is first applied, the M93Cx6 is in Erase/Write Disable mode and all Erase/Write instructions are inhibited. When the EWEN instruction is executed, Erase/Write instructions remain enabled until an Erase/Write Disable instruction (EWDS) is executed or V_{CC} falls below the power-on reset Threshold voltage. To protect the memory contents from accidental corruption, it is advisable to issue the EWDS instruction after every write cycle. The READ instruction is not affected by the EWEN or EWDS instructions.

Erase

The Erase instruction (ERASE) programs the addressed memory byte or word bits to '1'. Once the address is correctly decoded, the falling edge of the Chip Select input (S) starts a self-timed erase cycle. If the M93Cx6 is still performing the erase cycle, the Busy signal (Q = 0) will be returned if S is driven high after the t_{SLSH} delay, and the M93Cx6 will ignore any data on the bus. When the erase cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the M93Cx6 is ready to receive a new instruction.

Write

The Write instruction (WRITE) is composed of the Op-Code followed by the address and the 8 or 16 data bits to be written. Data input is sampled on the Low to High transition of the clock. After the last data bit has been sampled, *Chip Select (S) must be brought Low before the next rising edge of the clock (C) in order to start the self-timed programming cycle*. This is important as, if S is brought low before or after this specific frame window, the addressed location will not be programmed.

If the M93Cx6 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high after the t_{SLSH} delay, and the M93Cx6 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the M93Cx6 is ready to receive a new instruction. Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle). The Write instruction includes an automatic Erase cycle before writing the data, it is therefore unnecessary to execute an Erase instruction before a Write instruction execution.

Erase All

The Erase All instruction (ERAL) erases the whole memory (all memory bits are set to '1'). A dummy address is input during the instruction transfer and the erase is made in the same way as the ERASE instruction above. If the M93Cx6 is still performing the erase cycle, the Busy signal (Q = 0) will be returned if S is driven high after the t_{SLSH} delay, and the M93Cx6 will ignore any data on the bus. When the erase cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the M93Cx6 is ready to receive a new instruction.

Table 7A. Instruction Set for the M93C06 and M93C46

Instr.	Description	Start bit	Op-Code	x8 Org Address (ORG = 0) (1, 2)	Data	Req. Clock Cycles	x16 Org Address (ORG = 1) (1, 3)	Data	Req. Clock Cycles
READ	Read Data from Memory	1	10	A6-A0	Q7-Q0		A5-A0	Q15-Q0	
WRITE	Write Data to Memory	1	01	A6-A0	D7-D0	18	A5-A0	D15-D0	25
EWEN	Erase/Write Enable	1	00	11X XXXX		10	11 XXXX		9
EWDS	Erase/Write Disable	1	00	00X XXXX		10	00 XXXX		9
ERASE	Erase Byte or Word	1	11	A6-A0		10	A5-A0		9
ERAL	Erase All Memory	1	00	10X XXXX		10	10 XXXX		9
WRAL	Write All Memory with same Data	1	00	01X XXXX	D7-D0	18	01 XXXX	D15-D0	25

Notes: 1. X = don't care bit.
2. Address bits A6 and A5 are not decoded by the M93C06.
3. Address bits A5 and A4 are not decoded by the M93C06.

Table 7B. Instruction Set for the M93C56 and M93C66

Instr.	Description	Start bit	Op-Code	x8 Org Address (ORG = 0) (1, 2)	Data	Req. Clock Cycles	x16 Org Address (ORG = 1) (1, 3)	Data	Req. Clock Cycles
READ	Read Data from Memory	1	10	A8-A0	Q7-Q0		A7-A0	Q15-Q0	
WRITE	Write Data to Memory	1	01	A8-A0	D7-D0	20	A7-A0	D15-D0	27
EWEN	Erase/Write Enable	1	00	1 1XXX XXXX		12	11XX XXXX		11
EWDS	Erase/Write Disable	1	00	0 0XXX XXXX		12	00XX XXXX		11
ERASE	Erase Byte or Word	1	11	A8-A0		12	A7-A0		11
ERAL	Erase All Memory	1	00	1 0XXX XXXX		12	10XX XXXX		11
WRAL	Write All Memory with same Data	1	00	0 1XXX XXXX	D7-D0	20	01XX XXXX	D15-D0	27

Notes: 1. X = don't care bit.
2. Address bit A8 is not decoded by the M93C56.
3 Address bit A7 is not decoded by the M93C56.

Table 7C. Instruction Set for the M93C76 and M93C86

Instr.	Description	Start bit	Op-Code	x8 Org Address (ORG = 0) (1, 2)	Data	Req. Clock Cycles	x16 Org Address (ORG = 1) (1, 3)	Data	Req. Clock Cycles
READ	Read Data from Memory	1	10	A10-A0	Q7-Q0		A9-A0	Q15-Q0	
WRITE	Write Data to Memory	1	01	A10-A0	D7-D0	22	A9-A0	D15-D0	29
EWEN	Erase/Write Enable	1	00	11X XXXX XXXX		14	11 XXXX XXXX		13
EWDS	Erase/Write Disable	1	00	00X XXXX XXXX		14	00 XXXX XXXX		13
ERASE	Erase Byte or Word	1	11	A10-A0		14	A9-A0		13
ERAL	Erase All Memory	1	00	10X XXXX XXXX		14	10 XXXX XXXX		13
WRAL	Write All Memory with same Data	1	00	01X XXXX XXXX	D7-D0	22	01 XXXX XXXX	D15-D0	29

Notes: 1. X = don't care bit.
2. Address bit A10 is not decoded by the M93C76.
3. Address bit A9 is not decoded by the M93C76.

Write All

The Write All instruction (WRAL) writes the Data Input byte or word into all the addresses of the memory device. As for the Erase All instruction, a dummy address is input during the instruction transfer.

If the M93Cx6 is still performing the write cycle, the Busy signal (Q = 0) will be returned if S is driven high after the t_{SLSH} delay, and the M93Cx6 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the M93Cx6 is ready to receive a new instruction.

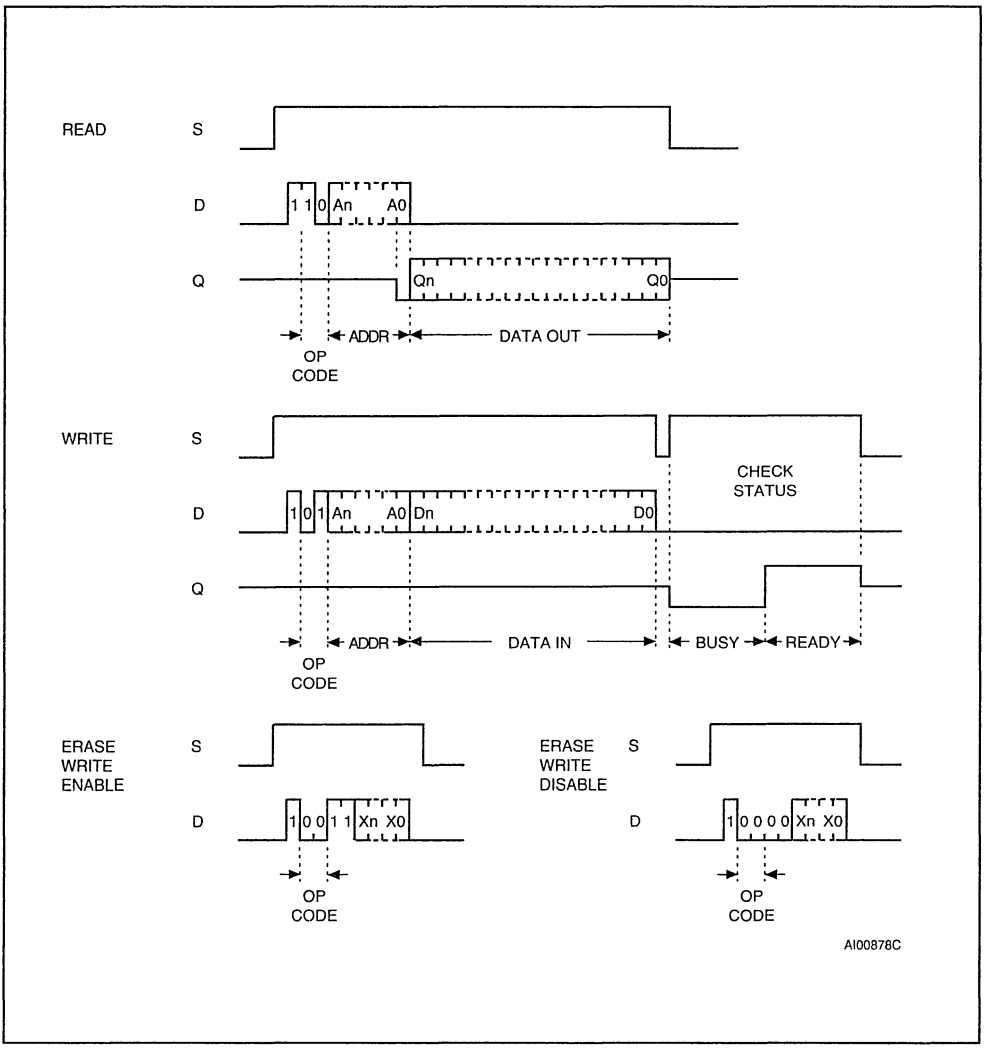
READY/BUSY Status

During every programming cycle (after a WRITE, ERASE, WRAL or ERAL instruction) the Data Output (Q) indicates the Ready/Busy status of the memory when the Chip Select is driven High. Once the M93Cx6 is Ready, the Data Output is set to '1' until a new start bit is decoded or the Chip Select is brought Low.

COMMON I/O OPERATION

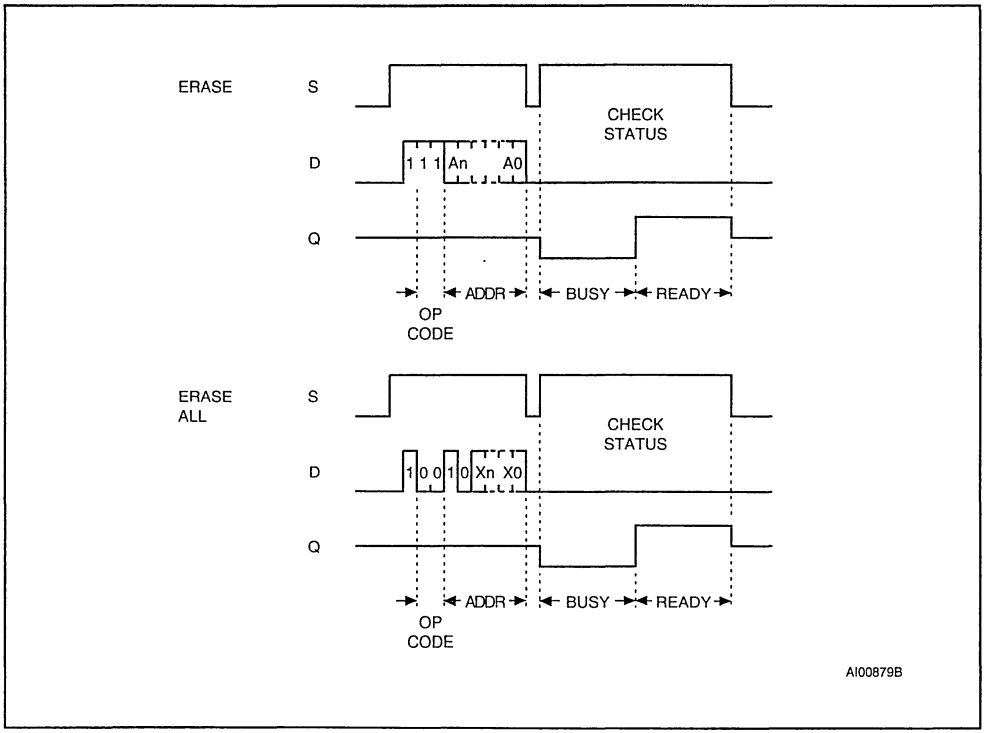
The Data Output (Q) and Data Input (D) signals can be connected together, through a current limiting resistor, to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, mostly to prevent a short circuit between the last entered address bit (A0) and the first data bit output by Q. The reader should refer to the STMicroelectronics application note AN394 "MICROWIRE EEPROM Common I/O Operation".

Figure 6. READ, WRITE, EWEN, EWDS Sequences



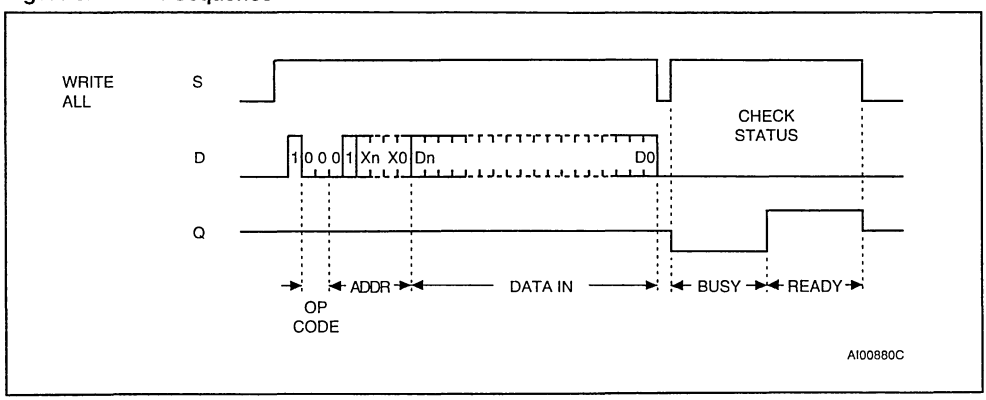
Note: An, Xn, Qn, Dn· Refer to Table 6a for the M93C06 and M93C46, to Table 6b for the M93C56 and M93C66; to Table 6c for the M93C76 and M93C86

Figure 7. ERASE, ERAL Sequences



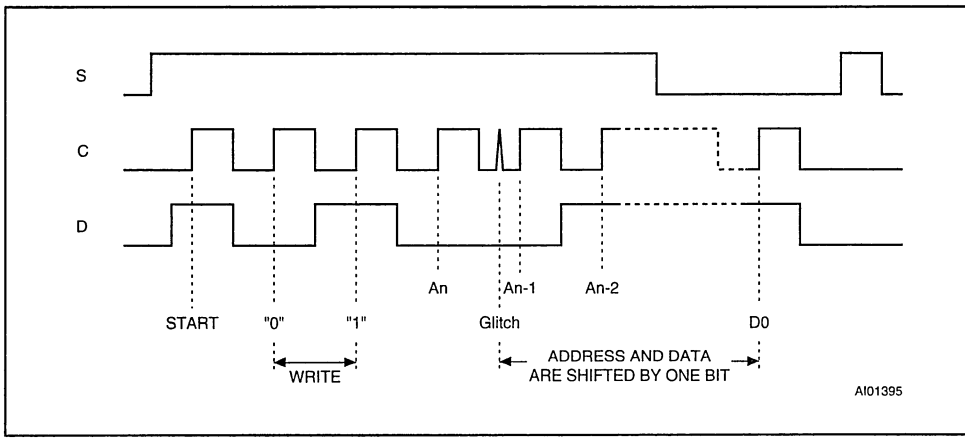
Note: An, Xn: Refer to Table 7a for the M93C06 and M93C46, to Table 7b for the M93C56 and M93C66; to Table 7c for the M93C76 and M93C86.

Figure 8. WRAL Sequence



Note: Xn, Dn· Refer to Table 7a for the M93C06 and M93C46, to Table 7b for the M93C56 and M93C66, to Table 7c for the M93C76 and M93C86

Figure 9. WRITE Sequence with One Clock Glitch



CLOCK PULSE COUNTER

The M93Cx6 offers a functional security block which filters glitches on the clock input (C), the clock pulse counter. In a normal environment, the M93Cx6 expects to receive the exact number of data bits on the D input (start bit, Op-Code, Address, Data); that is the exact amount of clock pulses on the C input.

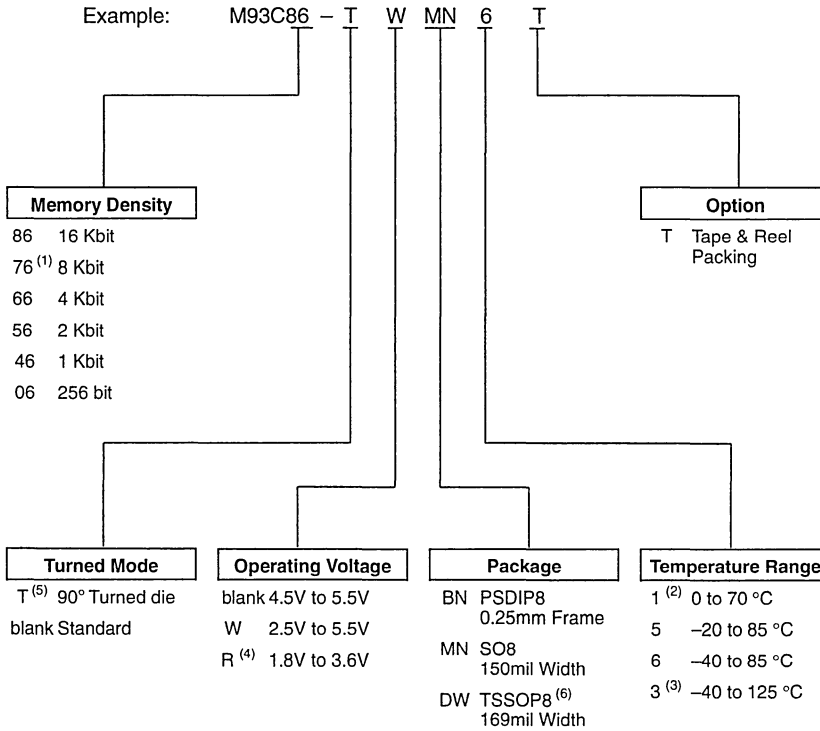
In a noisy environment, the number of pulses received (on the clock input C) may be greater than the clock pulses delivered by the Master (Microcontroller) driving the M93Cx6. In such a case, a part of the instruction can be delayed by one or more bits (see Figure 9), and may induce an erroneous write of data at an invalid address. The M93Cx6 has an on-chip counter which counts the clock pulses from the Start bit until the falling edge of the Chip Select signal.

For the WRITE instructions with a M93C56 (or M93C66), the number of clock pulses incoming to the counter must be exactly 20 (with the organisation x8) from the Start bit to the falling edge of Chip Select signal (1 Start bit + 2 Op-code bit + 9 Address bit + 8 Data bit = 20): if so, the M93C56 (or M93C66) executes the WRITE instruction; if the number of clock pulses is not equal to 20, the instruction will not be executed (and data will not be corrupted).

In the same way, when the organisation x16 is selected with the M93C56 (or M93C66), the number of clock pulses incoming to the counter must be exactly 27 (1 Start bit + 2 Op-code bit + 8 Address bit + 16 Data bit = 27) from the Start bit to the falling edge of Chip Select signal: if so, the M93C56 (or M93C66) executes the WRITE instruction; if the number of clock pulses is not equal to 27, the instruction will not be executed (and data will not be corrupted). The clock pulse counter is active on the WRITE, ERASE, ERAL and WRALL instructions.

In order to determine the exact number of clock pulses needed for all the M93Cx6 family on ERASE and WRITE instructions, refer to the Tables 7A, 7B and 7C, in the column: Requested Clock Cycles.

ORDERING INFORMATION SCHEME



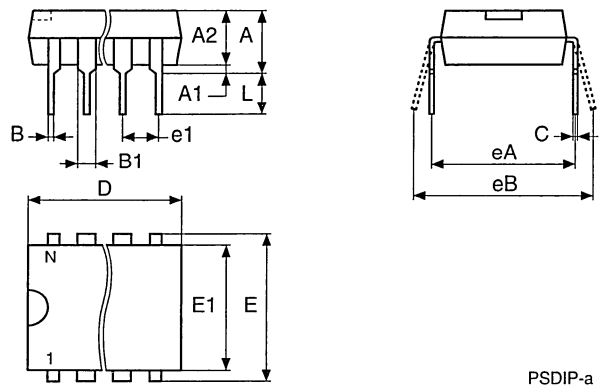
Notes: 1. This is preliminary information on a new product now in development. Details are subject to change without notice.
2. Temperature range on request only
3 Produced with High Reliability Certified Flow (HRCF), in V_{CC} range 4.5V to 5.5V at 1MHz only.
4 -R version (1.8V to 3 6V) are only available in temperature ranges 5 or 1.
5. Turned die option is not available for all devices Please contact the STMicroelectronics Sales Office nearest to you
6. TSSOP8 package available for M93C06, 46, 56, 66 low voltage (-W and -R) only.

Devices are shipped from the factory with the memory content set at all "1's" (FFFFh for x16, FFh for x8).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

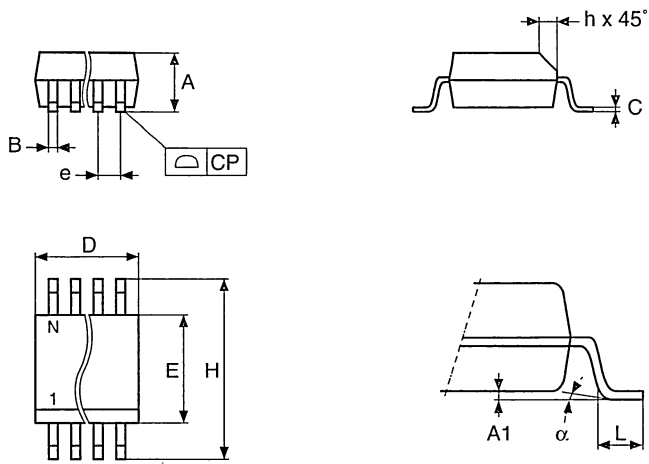


PSDIP-a

Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

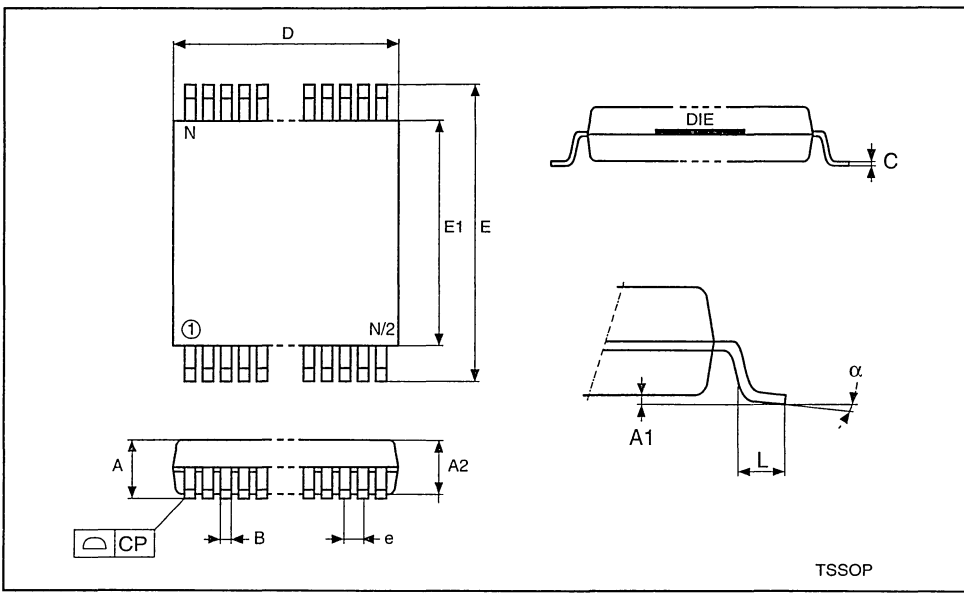


SO-a

Drawing is not to scale

TSSOP8 - 8 lead Plastic Shrink Small Outline, 169 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.10			0.043
A1		0.05	0.15		0.002	0.006
A2		0.85	0.95		0.033	0.037
B		0.19	0.30		0.007	0.012
C		0.09	0.20		0.004	0.008
D		2.90	3.10		0.114	0.122
E		6.25	6.50		0.246	0.256
E1		4.30	4.50		0.169	0.177
e	0.65	–	–	0.026	–	–
L		0.50	0.70		0.020	0.028
α		0°	8°		0°	8°
N		8			8	
CP			0.08			0.003



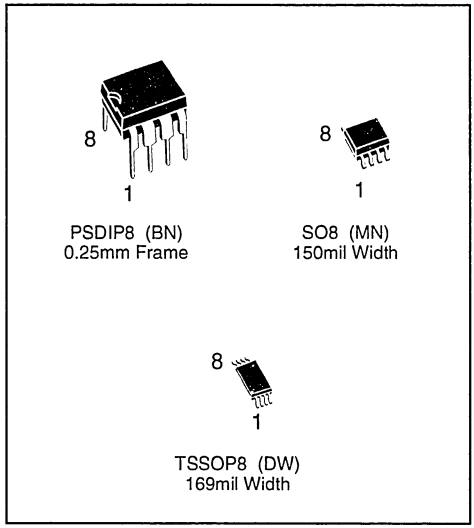
TSSOP

Drawing is not to scale

M93S66, M93S56, M93S46

4K/2K/1K (x16) Serial Microwire Bus EEPROM with Block Protection

- INDUSTRY STANDARD MICROWIRE BUS
- 1 MILLION ERASE/WRITE CYCLES, with 40 YEARS DATA RETENTION
- SINGLE ORGANIZATION by WORD (x16)
- WORD and ENTIRE MEMORY PROGRAMMING INSTRUCTIONS
- SELF-TIMED PROGRAMMING CYCLE with AUTO-ERASE
- READY/BUSY SIGNAL DURING PROGRAMMING
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for M93Sx6 version
  - 2.5V to 5.5V for M93Sx6-W version
  - 1.8V to 3.6V for M93Sx6-R version
- USER DEFINED WRITE PROTECTED AREA
- PAGE WRITE MODE (4 words)
- SEQUENTIAL READ OPERATION
- 5ms TYPICAL PROGRAMMING TIME
- ENHANCED ESD and LATCH-UP PERFORMANCES



DESCRIPTION

This M93S46/S56/S66 specification covers a range of 4K/2K/1K bit serial EEPROM products respectively. In this text, products are referred to as M93Sx6. The M93Sx6 is an Electrically Erasable Programmable Memory (EEPROM) fabricated with STMicroelectronics's High Endurance Single Polysilicon CMOS technology.

Table 1. Signal Names

S	Chip Select Input
D	Serial Data Input
Q	Serial Data Output
C	Serial Clock
PRE	Protect Enable
W	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

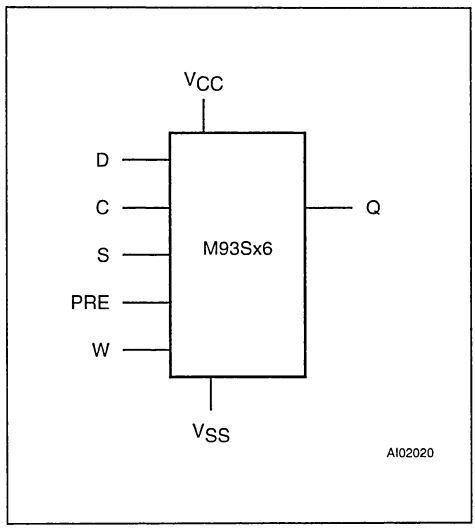


Figure 2A. DIP Pin Connections

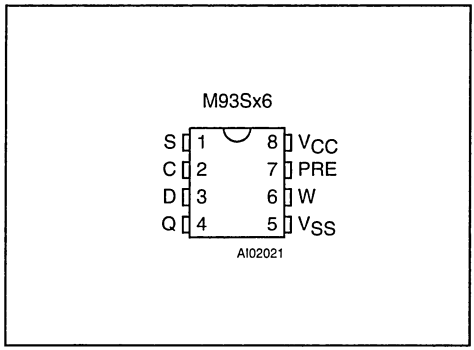


Figure 2B. SO and TSSOP Pin Connections

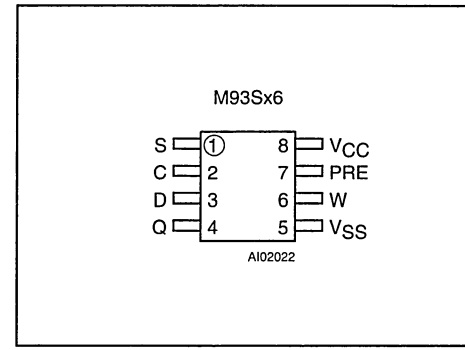


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			–40 to 125	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages (Q = V_{OH} or Hi-Z)			–0.3 to V_{CC} +0.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The M93Sx6 memory is accessed through a serial input (D) and output (Q) using the MICROWIRE bus protocol. The M93Sx6 is specified at 5V ±10%, the M93Sx6-W specified at 2.5V to 5.5V and the M93Sx6-R specified at 1.8V to 3.6V.

The M93S66/S56/S46 memory is divided into 256/128/64 x16 bit words respectively. These memory devices are available in both PSDIP8, SO8 and TSSOP8 packages.

The M93Sx6 memory is accessed by a set of instructions which includes Read, Write, Page Write, Write All and instructions used to set the memory protection. A Read instruction loads the address of the first word to be read into an internal address pointer. The data contained at this address is then clocked out serially. The address pointer is automatically incremented after the data is output and, if the Chip Select input (S) is held High, the M93Sx6 can output a sequential stream of data words. In this way, the memory can be read as a data stream from 16 to 4096 bits (for the M93S66), or continuously as the address counter automatically rolls over to '00' when the highest address is reached.

Table 3. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages (M93Sxx)	0.4V to 2.4V
Input Pulse Voltages (M93Sxx-W, M93Sxx-R)	$0.2V_{CC}$ to $0.8V_{CC}$
Input Timing Reference Voltages (M93Sxx)	1.0V to 2.0V
Output Timing Reference Voltages (M93Sxx)	0.8V to 2.0V
Input and Output Timing Reference Voltages (M93Sxx-W, M93Sxx-R)	$0.3V_{CC}$ to $0.7V_{CC}$
Output Load	C_L = 100pF

Note that Output Hi-Z is defined as the point where data is no longer driven.

Table 4. Capacitance (1)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		5	pF

Note: 1. Sampled only, not 100% tested.

Within the time required by a programming cycle (t_W), up to 4 words may be written with help of the Page Write instruction. the whole memory may also be erased, or set to a predetermined pattern, by using the Write All instruction.

Within the memory, an user defined area may be protected against further Write instructions. The size of this area is defined by the content of a Protect Register, located outside of the memory array. As a final protection step, data may be permanently protected by programming a One Time Programming bit (OTP bit) which locks the Protect Register content.

Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 16 bits at one time into one of the 256/128/64 words of the M93S46/S56/S66 respectively, the Page Write instruction writes up to 4 words of 16 bits to sequential locations, assuming in both cases that all addresses are outside the Write Protected area.

After the start of the programming cycle, a Ready/Busy signal is available on the Data output (Q) when Chip Select (S) is driven High.

An internal feature of the M93Sx6 provides Power-on Data Protection by inhibiting any operation when the Supply is too low. The design of the M93Sx6 and the High Endurance CMOS technology used for its fabrication give an Erase/Write cycle Endurance of 1,000,000 cycles and a data retention of 40 years.

Figure 3. AC Testing Input Output Waveforms

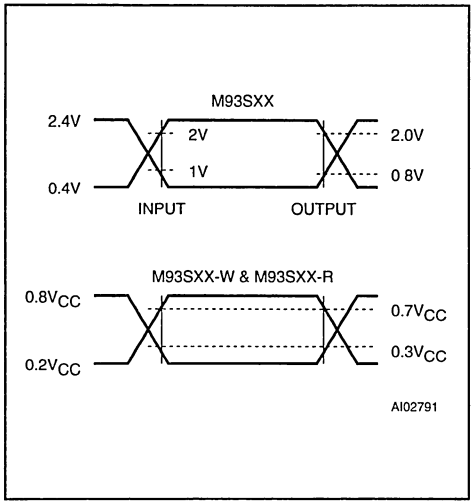


Table 5A. DC Characteristics for M93Sx6
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current	V_{CC} = 5V, S = V_{IH}, f = 1 MHz		1.5	mA
I_{CC1}	Supply Current (Standby)	V_{CC} = 5V, S = V_{SS}, C = V_{SS}, W = V_{SS} or V_{CC}, PRE = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage (D, C, S, W, PRE)		–0.3	0.8	V
V_{IH}	Input High Voltage (D, C, S, W, PRE)		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 5V, I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 5V, I_{OH} = –400µA	2.4		V

Table 5B. DC Characteristics for M93Sx6
(T_A = –40 to 125°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current	V_{CC} = 5V, S = V_{IH}, f = 1 MHz		1.5	mA
I_{CC1}	Supply Current (Standby)	V_{CC} = 5V, S = V_{SS}, C = V_{SS}, W = V_{SS} or V_{CC}, PRE = V_{SS} or V_{CC}		50	µA
V_{IL}	Input Low Voltage (D, C, S, W, PRE)		–0.3	0.8	V
V_{IH}	Input High Voltage (D, C, S, W, PRE)		2	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 5V, I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 5V, I_{OH} = –400µA	2.4		V

Table 5C DC Characteristics for M93Sx6-W
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current (CMOS Inputs)	V_{CC} = 5V, S = V_{IH}, f = 1 MHz		1.5	mA
		V_{CC} = 2.5V, S = V_{IH}, f = 1 MHz		1	mA
I_{CC1}	Supply Current (Standby)	V_{CC} = 2.5V, S = V_{SS}, C = V_{SS}, W = V_{SS} or V_{CC}, PRE = V_{SS} or V_{CC}		10	µA
V_{IL}	Input Low Voltage (D, C, S, W, PRE)		–0.3	0.2 V_{CC}	V
V_{IH}	Input High Voltage (D, C, S, W, PRE)		0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 5V, I_{OL} = 2.1mA		0.4	V
		V_{CC} = 2.5V, I_{OL} = 100µA		0.2	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 5V, I_{OH} = –400µA	2.4		V
		V_{CC} = 2.5V, I_{OH} = –100µA	V_{CC} – 0.2		V

Table 5D. DC Characteristics for M93Sx6-R (1)
(T_A = 0 to 70°C or –20 to 85°C; V_{CC} = 1.8V to3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2.5	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$, Q in Hi-Z		±2.5	µA
I_{CC}	Supply Current (CMOS Inputs)	V_{CC} = 3.6V, S = V_{IH}, f = 1 MHz		1.5	mA
		V_{CC} = 1.8V, S = V_{IH}, f = 1 MHz		1	mA
I_{CC1}	Supply Current (Standby)	V_{CC} = 1.8V, S = V_{SS}, C = V_{SS}, W = V_{SS} or V_{CC}, PRE = V_{SS} or V_{CC}		5	µA
V_{IL}	Input Low Voltage (D, C, S, W, PRE)		–0.3	0.2 V_{CC}	V
V_{IH}	Input High Voltage (D, C, S, W, PRE)		0.8 V_{CC}	V_{CC} + 1	V
V_{OL}	Output Low Voltage (Q)	V_{CC} = 1.8V, I_{OL} = 100µA		0.2	V
V_{OH}	Output High Voltage (Q)	V_{CC} = 1.8V, I_{OH} = –100µA	V_{CC} – 0.2		V

Note: 1. This is preliminary data.

Table 6A. AC Characteristics

Symbol	Alt	Parameter	M93S66/56/46				Unit
			V_{CC} = 4.5V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		V_{CC} = 4.5V to 5.5V, T_A = –40 to 125°C		
			Min	Max	Min	Max	
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High	50		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High	50		50		ns
t_{SHCH}	t_{CSS}	Chip Select Set-up Time	50		50		ns
t_{CLSH}	t_{SKS}	Clock Set-up Time (relative to S)	100		100		ns
t_{DVCH}	t_{DIS}	Data In Set-up Time	100		100		ns
t_{CHDX}	t_{DIH}	Data In Hold Time	100		100		ns
t_{CHQL}	t_{PD0}	Delay to Output Low		400		400	ns
t_{CHQV}	t_{PD1}	Delay to Output Valid		400		400	ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition	0		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition	250		250		ns
t_{CLSL}	t_{CSH}	Chip Select Hold Time	0		0		ns
t_{SLCH}		Chip Select Low to Clock High	250		250		ns
t_{SLSH} (1)	t_{CS}	Chip Select Low to Chip Select High	250		250		ns
t_{SHQV}	t_{SV}	Chip Select to Ready/Busy Status		400		400	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		200		200	ns
t_{CHCL} (2)	t_{SKH}	Clock High Time	250		250		ns
t_{CLCH} (2)	t_{SKL}	Clock Low Time	250		250		ns
t_W	t_{WP}	Erase/Write Cycle time		10		10	ms
f_C	f_{SK}	Clock Frequency	0	1	0	1	MHz

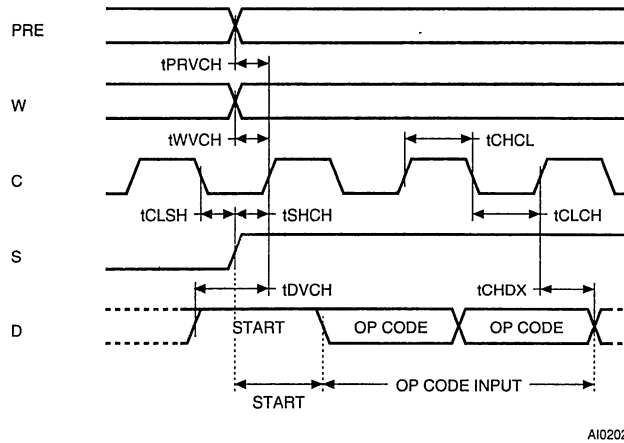
Notes: 1. Chip Select must be brought low for a minimum of tSLSH between consecutive instructions cycles
2. The Clock frequency specification calls for a minimum clock period of 1/fC, therefore the sum of the timings tCHCL+tCLCH must be greater or equal to 1/fC.

Table 6B. AC Characteristics

Symbol	Alt	Parameter	M93S66/56/46				Unit
			V_{CC} = 2.5V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		V_{CC} = 1.8V to 3.6V, (3) T_A = 0 to 70°C T_A = –20 to 85°C		
			Min	Max	Min	Max	
t_{PRVCH}	t_{PRES}	Protect Enable Valid to Clock High	50		50		ns
t_{WVCH}	t_{PES}	Write Enable Valid to Clock High	50		50		ns
t_{SHCH}	t_{CSS}	Chip Select Set-up Time	100		200		ns
t_{CLSH}	t_{SKS}	Clock Set-up Time (relative to S)	100		100		ns
t_{DVCH}	t_{DIS}	Data In Set-up Time	100		100		ns
t_{CHDX}	t_{DIH}	Data In Hold Time	100		200		ns
t_{CHQL}	t_{PD0}	Delay to Output Low		400		700	ns
t_{CHQV}	t_{PD1}	Delay to Output Valid		400		700	ns
t_{CLPRX}	t_{PREH}	Clock Low to Protect Enable Transition	0		0		ns
t_{SLWX}	t_{PEH}	Chip Select Low to Write Enable Transition	250		250		ns
t_{CLSL}	t_{CSH}	Chip Select Hold Time	0		0		ns
t_{SLCH}		Chip Select Low to Clock High	250		250		ns
t_{SLSH} (1)	t_{CS}	Chip Select Low to Chip Select High	250		1000		ns
t_{SHQV}	t_{SV}	Chip Select to Ready/Busy Status		400		700	ns
t_{SLQZ}	t_{DF}	Chip Select Low to Output Hi-Z		200		200	ns
t_{CHCL} (2)	t_{SKH}	Clock High Time	350		800		ns
t_{CLCH} (2)	t_{SKL}	Clock Low Time	250		800		ns
t_W	t_{WP}	Erase/Write Cycle time		10		10	ms
f_C	f_{SK}	Clock Frequency	0	1	0	0.5	MHz

Notes: 1. Chip Select must be brought low for a minimum of tSLSH between consecutive instructions cycles.
2. The Clock frequency specification calls for a minimum clock period of 1/fC, therefore the sum of the timings tCHCL+tCLCH must be greater or equal to 1/fC
3 This is preliminary data.

Figure 4. Synchronous Timing, Start and Op-Code Input



POWER-ON DATA PROTECTION

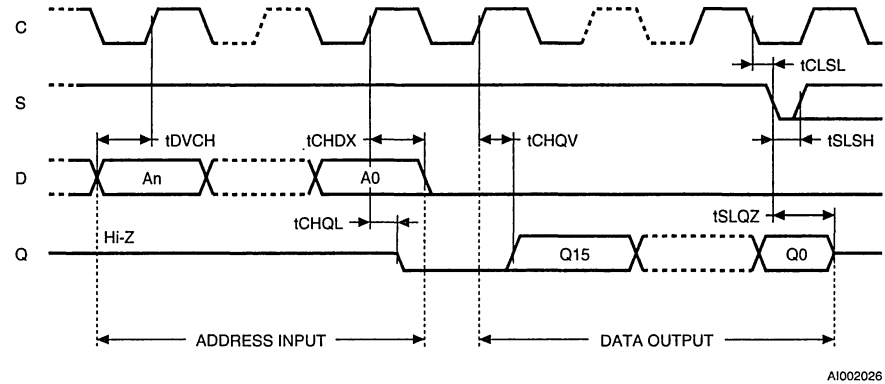
In order to prevent data corruption and inadvertent write operations during power-up and power-down, a Power On Reset (POR) circuit resets all internal programming circuitry and sets the device in the Write Disable mode.

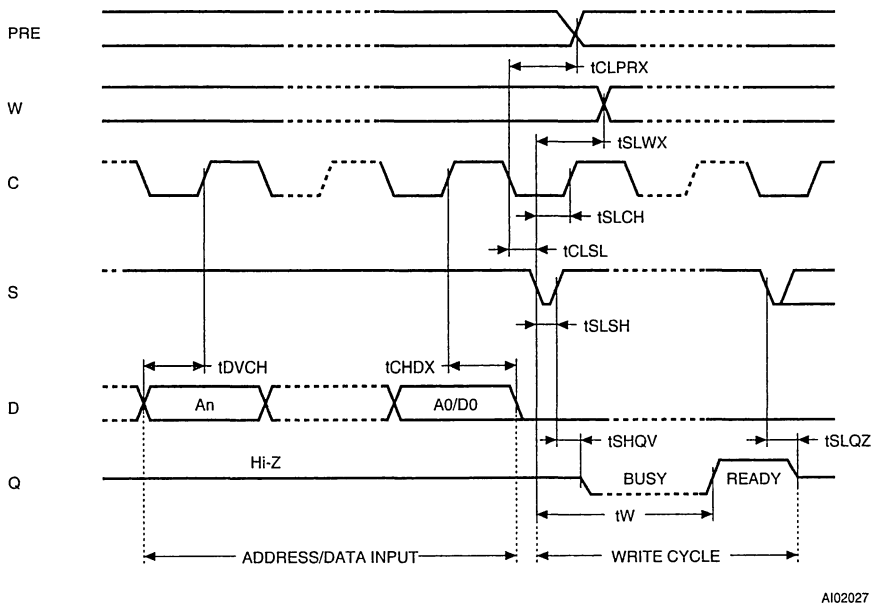
- At Power-up and Power-down, the device must NOT be selected (that is, the S input must be driven low) until the supply voltage reaches the operating value Vcc specified in the AC and DC tables.
- When V_{CC} reaches its functional value, the device is properly reset (in the Write Disable mode) and is ready to decode and execute an incoming instruction.

For the M93Sx6 specified at 5V, the POR threshold voltage is around 3V.

For all the other M93Sx6 specified at low V_{CC} (with -W and -R V_{CC} range options), the POR threshold voltage is around 1.5V.

Figure 5. Synchronous Timing, Read or Write





INSTRUCTIONS

The M93S66/S56/S46 have eleven instructions, as shown in Table 7. Each instruction is preceded by the rising edge of the signal applied on the Chip Select (S) input (assuming that the clock C is low). After the device is selected, the internal logic waits for the start bit, which define the begining of the instruction bit stream. The start bit is the first '1' read on D input during the rising edge of the clock C. Following the start bit, the op-codes of the instructions are made up of the 2 following bits. Notice that some instructions use only these first two bits, others use also the first two bits of the address to define the op-code. The op-code is then followed by the address of the word to be accessed.

For the M93S46, the address is made up of 6 bits (See Table 7a). For the M93S56 and M93S66, the address is made up of 8 bits (See Table 7b).

The M93Sx6 is fabricated in CMOS technology and is therefore able to run from zero Hz (static input signals) up to the maximum ratings (specified in Table 6).

Table 7A. Instruction Set for the M93S46

Instr.	Description	W	PRE	Start Bit	Op-Code	Address (1)	Data	Req. Clock Cycles	Additional Information
READ	Read Data from Memory	X	'0'	'1'	10	A5-A0	Q15-Q0		
WRITE	Write Data to Memory	'1'	'0'	'1'	01	A5-A0	D15-D0	25	Write is executed if the address is not inside the Protected area
PAWRITE	Page Write to Memory	'1'	'0'	'1'	11	A5-A0	N x D15-D0	9 + N x 16	Write is executed if all the N addresses are not inside the Protected area
WRALL	Write All Memory	'1'	'0'	'1'	00	01XXXX	D15-D0	25	Write all data if the Protect Register is cleared
WEN	Write Enable	'1'	'0'	'1'	00	11XXXX		9	
WDS	Write Disable	X	'0'	'1'	00	00XXXX		9	
PRREAD	Protect Register Read	X	'1'	'1'	10	XXXXXX	Q5-Q0 + Flag		Data Output = Protect Register content + Protect Flag bit
PRWRITE	Protect Register Write	'1'	'1'	'1'	01	A5-A0		9	Data above specified address A5-A0 are protected
PRCLEAR	Protect Register Clear	'1'	'1'	'1'	11	111111		9	Protect Flag is also cleared (cleared Flag = 1)
PREN	Protect Register Enable	'1'	'1'	'1'	00	11XXXX		9	
PRDS	Protect Register Disable	'1'	'1'	'1'	00	000000		9	OTP bit is set permanently

Note: 1. X = don't care bit.

Table 7B. Instruction Set for the M93S56 and M93S66

Instr.	Description	W	PRE	Start Bit	Op-Code	Address (1,2)	Data	Req. Clock Cycles	Additional Information
READ	Read Data from Memory	X	'0'	'1'	10	A7-A0	Q15-Q0		
WRITE	Write Data to Memory	'1'	'0'	'1'	01	A7-A0	D15-D0	27	Write is executed if the address is not inside the Protected area
PAWRITE	Page Write to Memory	'1'	'0'	'1'	11	A7-A0	N x D15-D0	11 + N x 16	Write is executed if all the N addresses are not inside the Protected area
WRALL	Write All Memory	'1'	'0'	'1'	00	01XXXXXX	D15-D0	27	Write all data if the Protect Register is cleared
WEN	Write Enable	'1'	'0'	'1'	00	11XXXXXX		11	
WDS	Write Disable	X	'0'	'1'	00	00XXXXXX		11	
PRREAD	Protect Register Read	X	'1'	'1'	10	XXXXXXXX	Q7-Q0 + Flag		Data Output = Protect Register content + Protect Flag bit
PRWRITE	Protect Register Write	'1'	'1'	'1'	01	A7-A0		11	Data above specified address A7-A0 are protected
PRCLEAR	Protect Register Clear	'1'	'1'	'1'	11	11111111		11	Protect Flag is also cleared (cleared Flag = 1)
PREN	Protect Register Enable	'1'	'1'	'1'	00	11XXXXXX		11	
PRDS	Protect Register Disable	'1'	'1'	'1'	00	00000000		11	OTP bit is set permanently

Notes: 1. X = don't care bit
2. Address bit A7 is not decoded by the M93S56.

Read

The Read instruction (READ) outputs serial data on the Data Output (Q). When a READ instruction is received, the instruction and address are decoded and the data from the memory is transferred into an output shift register. A dummy '0' bit is output first followed by the 16 bit word with the MSB first. Output data changes are triggered by the Low to High transition of the Clock (C). The M93Sx6 will automatically increment the address and will clock out the next word as long as the Chip Select input (S) is held High. In this case the dummy '0' bit is NOT output between words and a continuous stream of data can be read.

Write Enable and Write Disable

The Write Enable instruction (WEN) authorizes the following Write instructions to be executed. The Write Disable instruction (WDS) disables the execution of the following Write instructions and the internal programming cycle cannot run.

When power is first applied, the M93Sx6 is in Write Disable mode and all Write instructions are inhibited. When the WEN instruction is executed, Write instructions remain enabled until a Write Disable instruction (WDS) is executed or V_{CC} falls below the Power-On Reset threshold Voltage.

To protect the memory contents from accidental corruption, it is advisable to issue the WDS instruction after every write cycle. The READ instruction is not affected by the WEN or WDS instructions.

Write

The Write instruction (WRITE) is composed of the Start bit plus the Op-Code followed by the address and the 16 data bits to be written. The Write Enable signal (W) must be held high during the Write instruction. Data input (D) is sampled on the Low to High transition of the clock. After the last data bit has been sampled, Chip Select (S) must be brought Low before the next rising edge of the clock (C) in order to start the self-timed programming cycle. This is really important as, if S is brought low before or after this specific frame window, the addressed location will not be programmed, providing that the address in NOT in the protected area.

If the M93Sx6 is still performing the write cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high after the t_{SLSH} delay, and the M93Sx6 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the M93Sx6 is ready to receive a new instruction. Programming is internally self-timed (the external clock signal on C input may be disconnected or left running after the start of a Write cycle).

Page Write

A Page Write instruction (PAWRITE) contains the first address to be written followed by up to 4 data words. The Write Enable signal (W) must be held High during the PAWRITE instruction. Input address and data are sampled on the Low to High transition of the clock. After the receipt of each data word, bits A1-A0 of the internal address register are incremented, the high order bits (Ax-A2) remaining unchanged. Users must take care by software to ensure that the last word address has the same upper order address bits as the initial address transmitted to avoid address roll-over. After the LSB of the last data word, Chip Select (S) must be brought Low before the next rising edge of the Clock (C) in order to start the self-timed programming cycle. This is really important as, if S is brought low before or after this specific frame window, the addressed locations will not be programmed. The Page Write operation will not be performed if any of the 4 words is addressing the protected area. If the M93Sx6 is still performing the programming cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high, and the M93Sx6 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the M93Sx6 is ready to receive a new instruction.

Write All

The Write All instruction (WRALL) is valid only after the Protect Register has been cleared by executing a PRCLEAR (Protect Register Clear) instruction. The Write All instruction simultaneously writes the whole memory with the same data word included in the instruction. The Write Enable signal (W) must be held High before and during the Write All instruction. Input address and data are sampled on the Low to High transition of the clock. If the M93Sx6 is still performing the write cycle, the Busy signal (Q = 0) will be returned if the Chip Select input (S) is driven high after the t_{SLSH} delay, and the M93Sx6 will ignore any data on the bus. When the write cycle is completed, the Ready signal (Q = 1) will indicate (if S is driven high) that the M93Sx6 is ready to receive a new instruction.

READY/BUSY Status

During every programming cycle (after a WRITE, WRALL or PAWRITE instruction) the Data Output (Q) indicates the Ready/Busy status of the memory when the Chip Select is driven High. Once the M93Sx6 is Ready, the Data Output is set to '1' until a new start bit is decoded or the Chip Select is brought Low.

MEMORY WRITE PROTECTION AND PROTECT REGISTER

The M93Sx6 offers a Protect Register containing the bottom address of the memory area which has to be protected against write instructions. In addition to this Protect Register, two flag bits are used to indicate the Protect Register status: the Protect Flag enabling/disabling the memory protection throught the Protect Register and the OTP bit which, when set, disables access to the Protect Register and thus prevents any further modifications of this Protect Register value. The content of the Protect Register is defined when using the PRWRITE instruction, it may be read when using the PRREAD instruction. A specific instruction PREN (Protect Register Enable) allows the user to execute the protect instructions PRCLEAR, PRWRITE and PRDS. this PREN instruction being used together with the signals applied on the input pins PRE (Protect Register Enable) and W (Write Enable).

Accessing the Protect Register is done by executing the following sequence:

- WEN: execute the Write Enable instruction,
- PREN: execute the PREN instruction,
- PRWRITE, PRCLEAR or PRDS: the protection then may be defined, in terms of size of the protected area (PRWRITE, PRCLEAR) and may be set permanently (PRDS instruction).

Protect Register Read

The Protect Register Read instruction (PRREAD) outputs on the Data Output Q the content of the Protect Register, followed by the Protect Flag bit. The Protect Register Enable pin (PRE) must be driven High before and during the instruction.

As in the Read instruction a dummy '0' bit is output first. Since it is not possible to distinguish if the Protect Register is cleared (all 1's) or if it is written with all 1's, user must check the Protect Flag status (and not the Protect Register content) to ascertain the setting of the memory protection.

Protect Register Enable

The Protect Register Enable instruction (PREN) is used to authorize the use of further PRCLEAR, PRWRITE and PRDS instructions. The PREN insruction does not modify the Protect Flag bit value.

Note: A Write Enable (WEN) instruction must be executed before the Protect Enable instruction. Both the Protect Enable (PRE) and Write Enable (W) input pins must be held High during the instruction execution.

Protect Register Clear

The Protect Register Clear instruction (PRCLEAR) clears the address stored in the Protect Register to all 1's, and thus enables the execution of WRITE and WRALL instructions. The Protect Register Clear execution clears the Protect Flag to '1'. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution.

Note: A PREN instruction must immediately precede the PRCLEAR instruction.

Protect Register Write

The Protect Register Write instruction (PRWRITE) is used to write into the Protect Register the address of the first word to be protected. After the PRWRITE instruction execution, all memory locations equal to and above the specified address, are protected from writing. The Protect Flag bit is set to '0', it can be read with Protect Register Read instruction. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution.

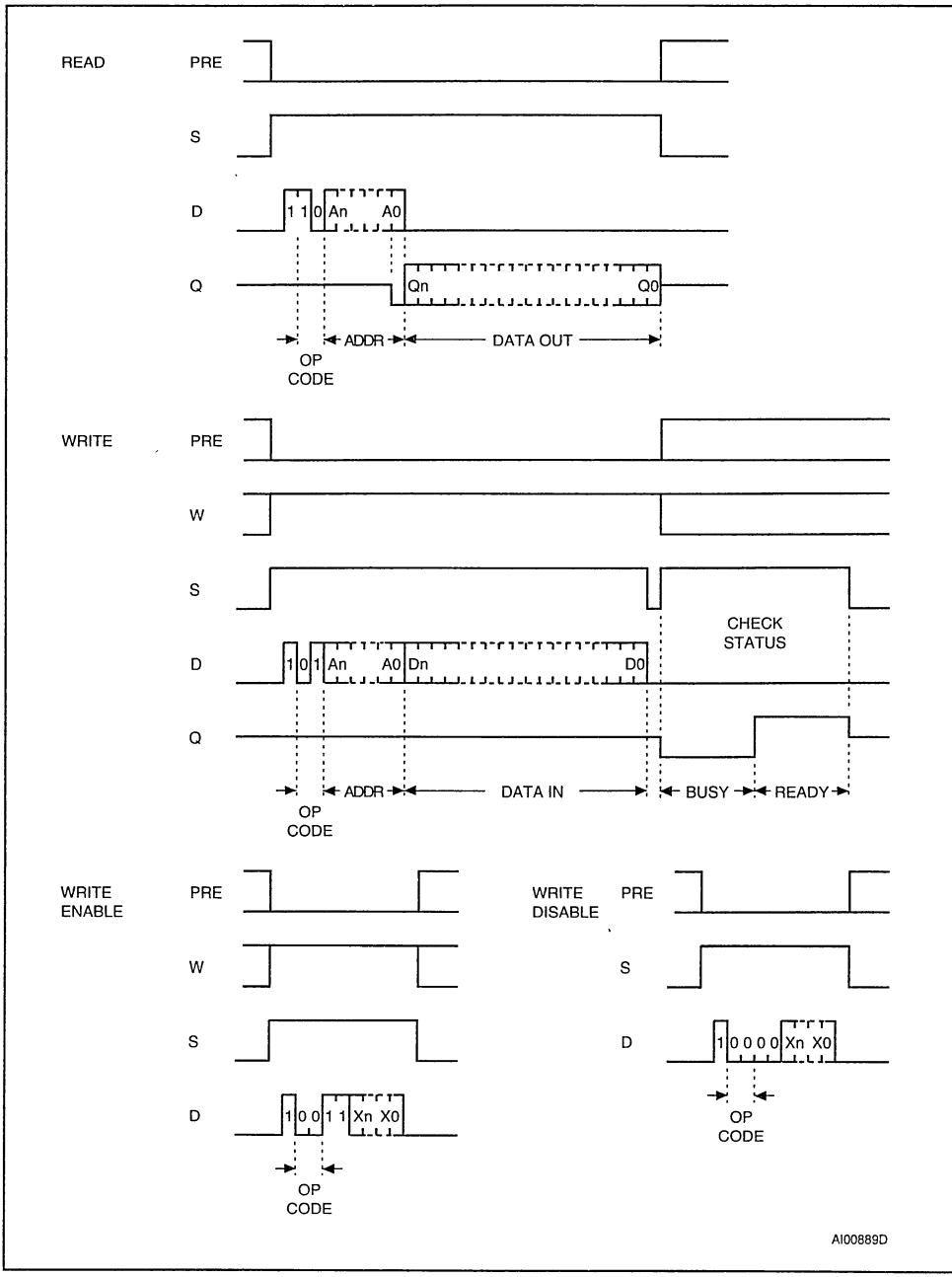
Note: A PREN instruction must immediately precede the PRWRITE instruction, but it is not necessary to execute first a PRCLEAR.

Protect Register Disable

The Protect Register Disable instruction sets the One Time Programmable bit (OTP bit). The Protect Register Disable instruction (PRDS) is a ONE TIME ONLY instruction which latches the Protect Register content, this content is therefore unalterable in the future. Both the Protect Enable (PRE) and Write Enable (W) input pins must be driven High during the instruction execution. The OTP bit cannot be directly read, it can be checked by reading the content of the Protect Register (PRREAD instruction), then by writing this same value into the Protect Register (PRWRITE instruction): when the OTP bit is set, the Ready/Busy status cannot appear on the Data output (Q). When the OTP bit is not set, the Busy status appear on the Data output (Q).

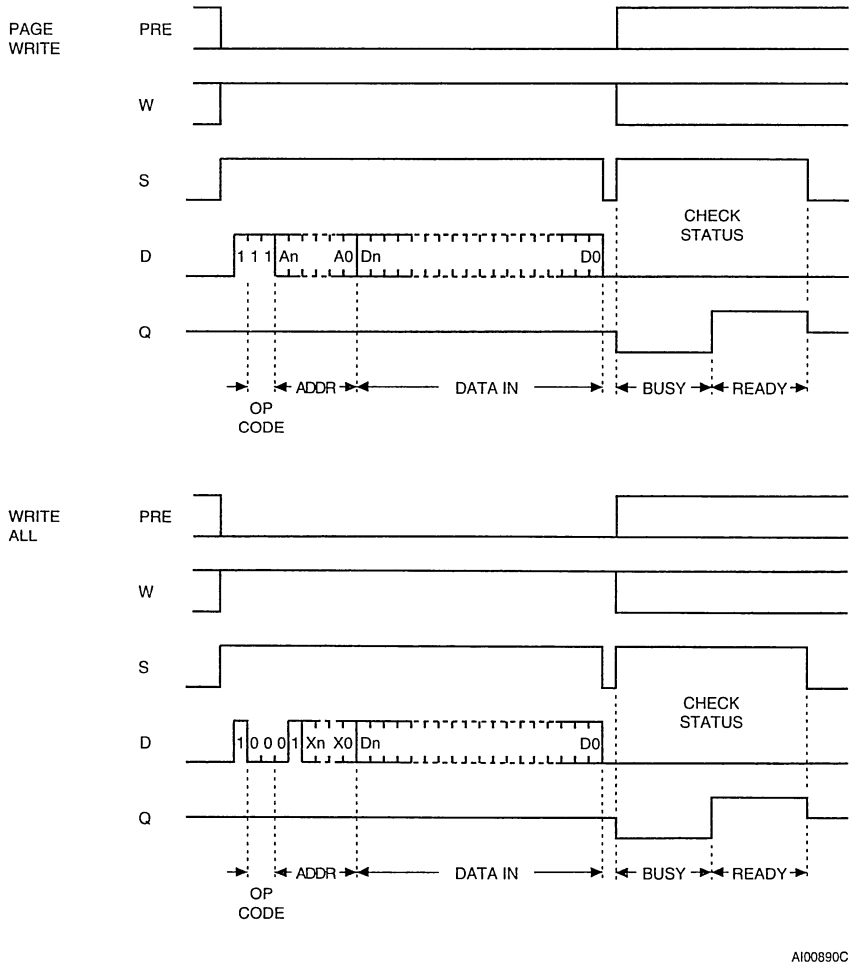
Note: A PREN instruction must immediately precede the PRDS instruction.

Figure 6. READ, WRITE, WEN, WDS Sequences



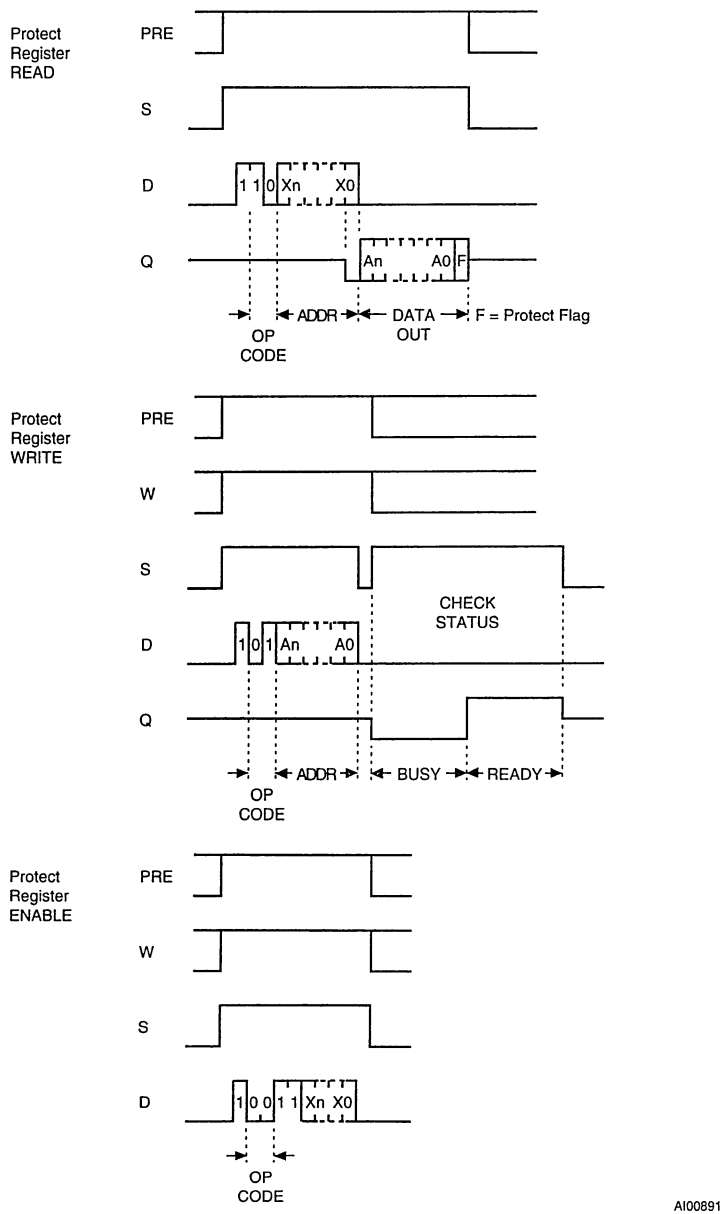
Notes: 1. An - Xn - Qn - Dn Refer to Table 7a for the M93S46.
2. An - Xn - Qn - Dn Refer to Table 7b for the M93S56 and M93S66.

Figure 7. PAWRITE, WRALL Sequences



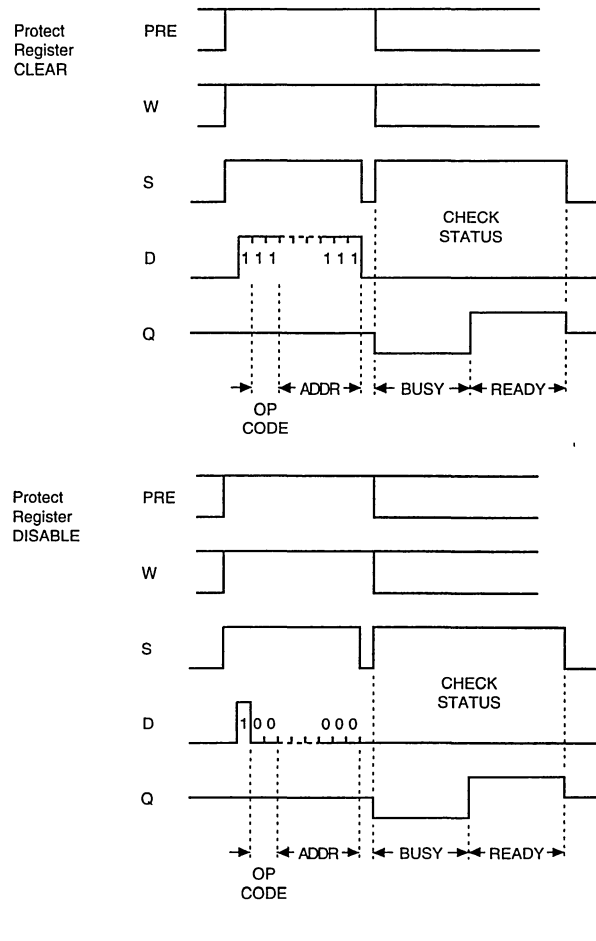
Notes: 1. An - Xn - Dn. Refer to Table 7a for the M93S46.
2. An - Xn - Dn: Refer to Table 7b for the M93S56 and M93S66.

Figure 8. PRREAD, PRWRITE, PREN Sequences



Notes: 1. An - Xn - Dn: Refer to Table 7a for the M93S46.
2. An - Xn - Dn: Refer to Table 7b for the M93S56 and M93S66.

Figure 9. PRCLEAR, PRDS Sequences



Notes: 1. An - Xn - Dn: Refer to Table 7a for the M93S46.
2. An - Xn - Dn: Refer to Table 7b for the M93S56 and M93S66.

COMMON I/O OPERATION

The Data Output (Q) and Data Input (D) signals can be connected together, through a current limiting resistor, to form a common, one wire data bus. Some precautions must be taken when operating the memory with this connection, mostly to prevent a short circuit between the last entered address bit (A0) and the first data bit output by Q. The reader should refer to the STMicroelectronics application note AN394 "MICROWIRE EEPROM Common I/O Operation".

CLOCK PULSE COUNTER

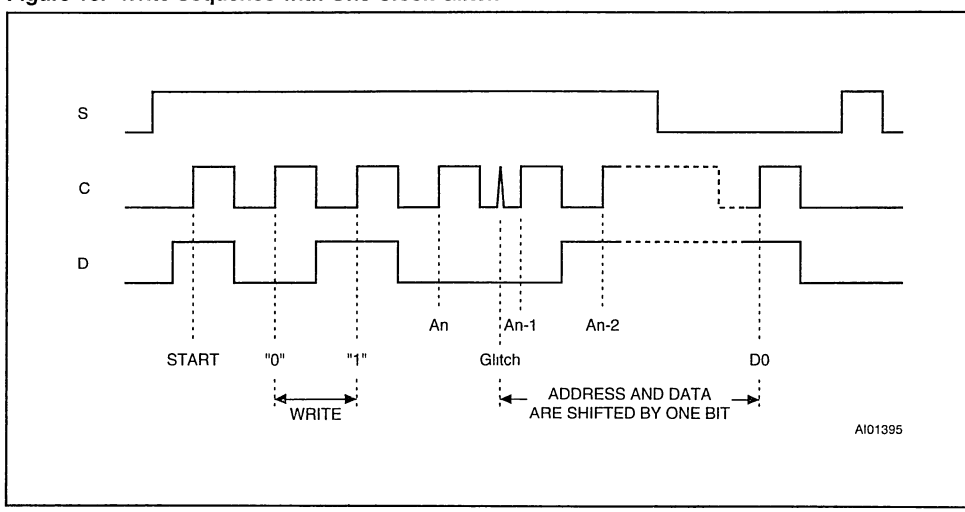
The M93Sx6 offers a functional security filtering glitches on the clock input (C), the clock pulse counter.

In a normal environment, the M93Sx6 expectes to receive the exact amount of data on the D input (start bit, Op-Code, Address, Data), that is the exact amount of clock pulses on the C input. In a noisy environment, the number of pulses received (on the clock input C) may be greater than the clock pulses delivered by the Master (Microcontroller) driving the M93Sx6. In such a case, a part of the instruction is delayed by one bit (see Figure 10), and it may induce an erroneous write of data at a wrong address. The M93Sx6 has an on-chip counter which counts the clock pulses from the Start bit until the falling edge of the Chip Select signal.

For the WRITE instructions with a M93S56 (or M93S66), the number of clock pulses incoming to the counter must be exactly 27 from the Start bit to the falling edge of Chip Select signal (1 Start bit + 2 Op-code bit + 8 Address bit + 16 Data bit = 27): if so, the M93S56 (or M93S66) executes the WRITE instruction. If the number of clock pulses is not equal to 27, the instruction will not be executed (and data will not be corrupted).

The clock pulse counter is active on WRITE, PAWRITE, WRALL, PRWRITE and PRCLEAR instructions. In order to determine the exact number of clock pulses needed for all the M93Sx6 on WRITE instructions, refer to Tables 7a and 7b, in the column: Requested Clock Cycles.

Figure 10. Write Sequence with One Clock Glitch



ORDERING INFORMATION SCHEME

Example: M93S56 – W MN 6 T

Memory Density	Operating Voltage	Package	Temperature Range	Option
66 4 Kbit	blank 4.5V to 5.5V	BN PSDIP8 0.25mm Frame	1 (1) 0 to 70 °C	T Tape & Reel Packing
56 2 Kbit	W 2.5V to 5.5V	MN SO8 150mil Width	5 –20 to 85 °C	
46 1 Kbit	R (3) 1.8V to 3.6V	DW TSSOP8 169mil Width	6 –40 to 85 °C	
			3 (2) –40 to 125 °C	

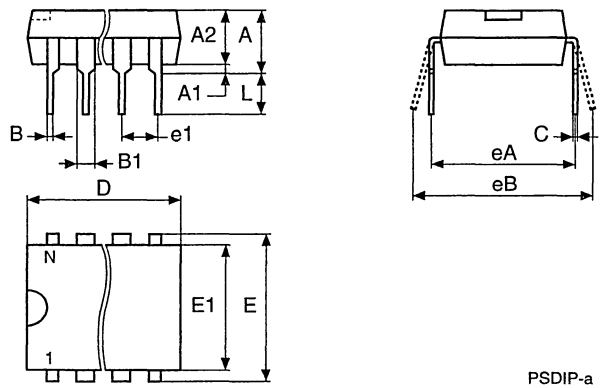
Notes: 1 Temperature range on request only
2. Produced with High Reliability Certified Flow (HRCF), in V_{CC} range 4.5V to 5.5V at 1MHz only.
3. -R version (1.8V to 3.6V) are only available in temperature ranges 5 or 1.

Devices are shipped from the factory with the memory content set at all "1's" (FFFFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

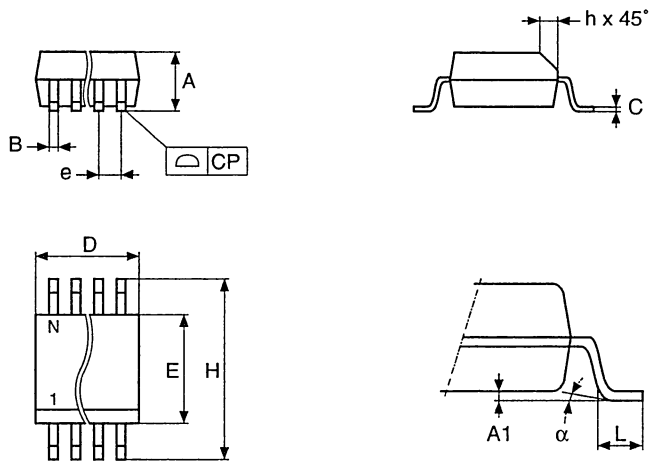


PSDIP-a

Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

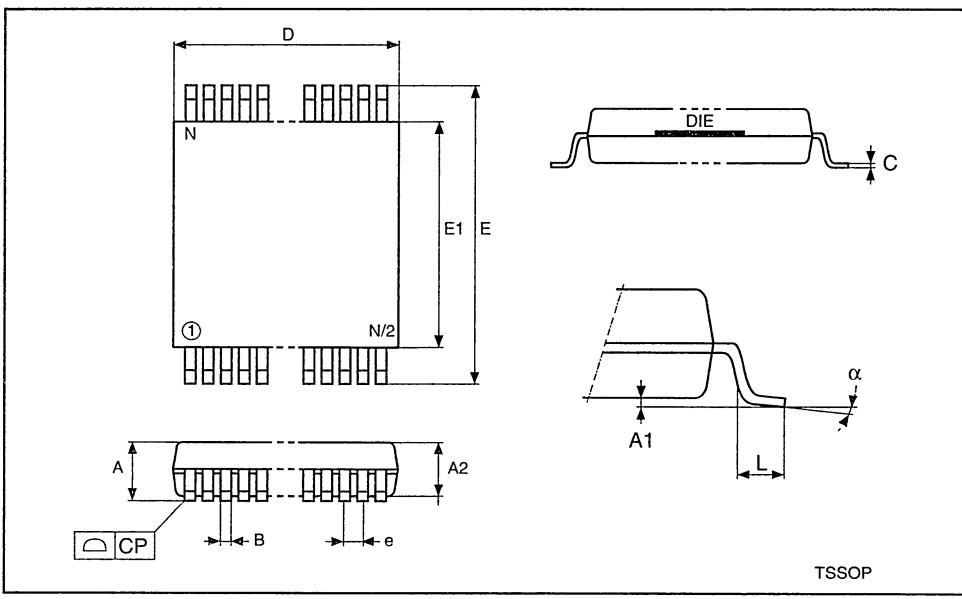


SO-a

Drawing is not to scale

TSSOP8 - 8 lead Plastic Shrink Small Outline, 169 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.10			0.043
A1		0.05	0.15		0.002	0.006
A2		0.85	0.95		0.033	0.037
B		0.19	0.30		0.007	0.012
C		0.09	0.20		0.004	0.008
D		2.90	3.10		0.114	0.122
E		6.25	6.50		0.246	0.256
E1		4.30	4.50		0.169	0.177
e	0.65	–	–	0.026	–	–
L		0.50	0.70		0.020	0.028
α		0°	8°		0°	8°
N		8			8	
CP			0.08			0.003



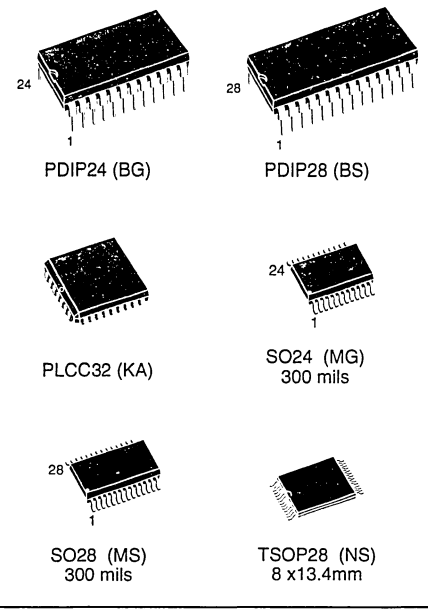
Drawing is not to scale

PARALLEL EEPROM

M28C16A
M28C17A

16 Kbit (2Kb x8) Parallel EEPROM

- FAST ACCESS TIME:
  - 150ns at 5V
  - 250ns at 3V
- SINGLE SUPPLY VOLTAGE:
  - 5V ± 10% for M28C16A and M28C17A
  - 2.7V to 3.6V for M28C16-xxW
- LOW POWER CONSUMPTION
- FAST WRITE CYCLE
  - 32 Bytes Page Write Operation
  - Byte or Page Write Cycle: 5ms
- ENHANCED END OF WRITE DETECTION
  - Ready/Busy Open Drain Output
  - Data Polling
  - Toggle Bit
- PAGE LOAD TIMER STATUS BIT
- HIGH RELIABILITY SINGLE POLYSILICON, CMOS TECHNOLOGY
  - Endurance >100,000 Erase/Write Cycles
  - Data Retention >40 Years
- JEDEC APPROVED BYTEWIDE PIN OUT



DESCRIPTION

The M28C16A and M28C17A are 2Kb x8 low power Parallel EEPROM fabricated with STMicroelectronics proprietary single polysilicon CMOS technology. The device offers fast access time with low power dissipation and requires a 5V or 3V power supply.

Table 1. Signal Names

A0-A10	Address Input
DQ0-DQ7	Data Input / Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$R\overline{B}$	Ready / Busy
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

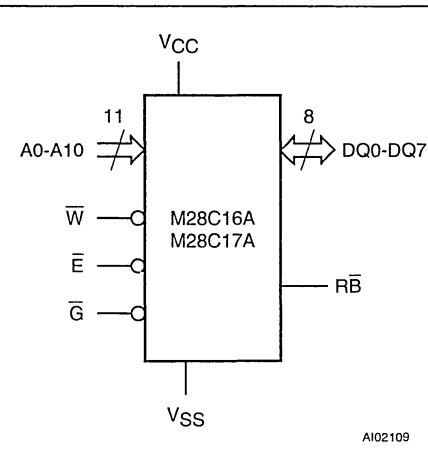
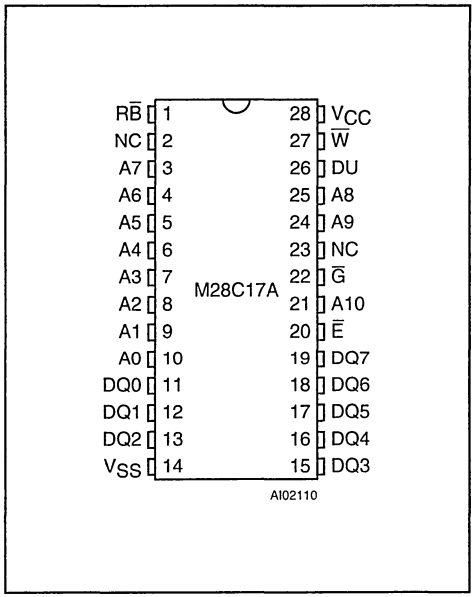
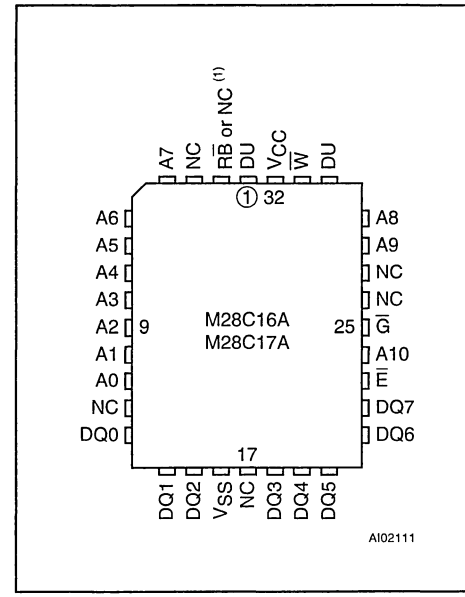


Figure 2A. DIP/SO 28 Pin Connections



Warning: NC = Not Connected, DU = Don't Use.

Figure 2B. LCC Pin Connections



Warning: NC = Not Connected, DU = Don't Use.
Note: 1. Pin 2 is either RB for M28C17A or NC for M28C16A.

Figure 2C. DIP/SO 24 Pin Connections

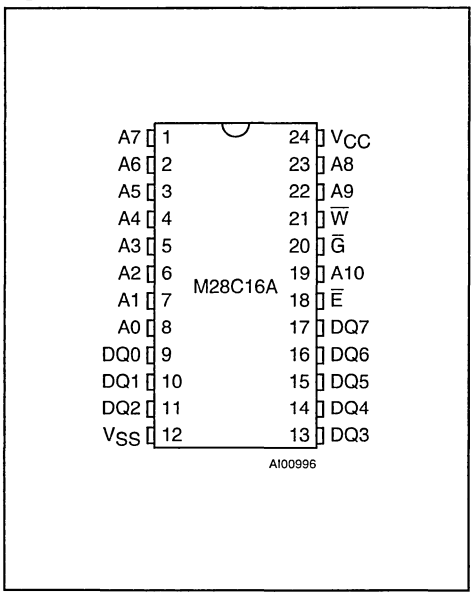
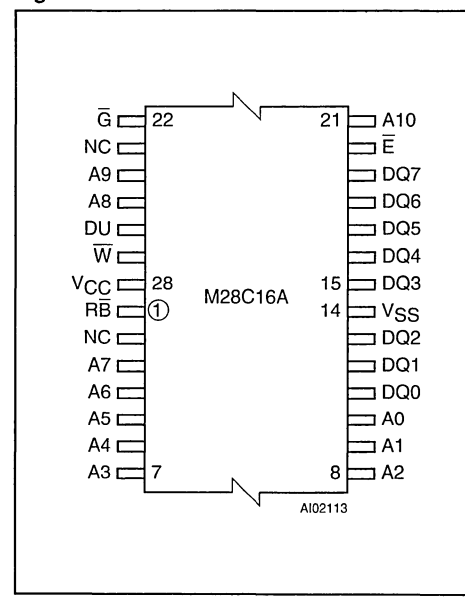


Figure 2D. TSOP Pin Connections



Warning: NC = Not Connected, DU = Don't Use.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (2)	– 40 to 85	°C
T_{STG}	Storage Temperature Range	– 65 to 150	°C
V_{CC}	Supply Voltage	– 0.3 to 6.5	V
V_{IO}	Input/Output Voltage	– 0.3 to V_{CC} +0.6	V
V_I	Input Voltage	– 0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)	3000	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Depends on range.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	Data In
Standby / Write Inhibit	V_{IH}	X	X	Hi-Z
Write Inhibit	X	X	V_{IH}	Data Out or Hi-Z
Write Inhibit	X	V_{IL}	X	Data Out or Hi-Z
Output Disable	X	V_{IH}	X	Hi-Z

Note: X = V_{IH} or V_{IL}

DESCRIPTION (cont'd)

The circuit has been designed to offer a flexible microcontroller interface featuring both hardware and software handshaking mode with Ready/Busy, Data Polling and Toggle Bit. The M28C16A/17A supports 32 byte page write operation.

PIN DESCRITPION

Addresses (A0-A10). The address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{E}$). The chip enable input must be low to enable all read/write operations. When Chip Enable is high, power consumption is reduced.

Output Enable ($\overline{G}$). The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/ Out (DQ0 - DQ7). Data is written to or read from the M28C16A/17A through the I/O pins.

Write Enable ($\overline{W}$). The Write Enable input controls the writing of data to the M28C16A/17A.

Ready/Busy ($R\overline{B}$). Ready/Busy is an open drain output that can be used to detect the end of the internal write cycle. Ready/Busy is available for the M28C17A in PDIP, PLCC and SO packages, and for the M28C16A in TSOP only.

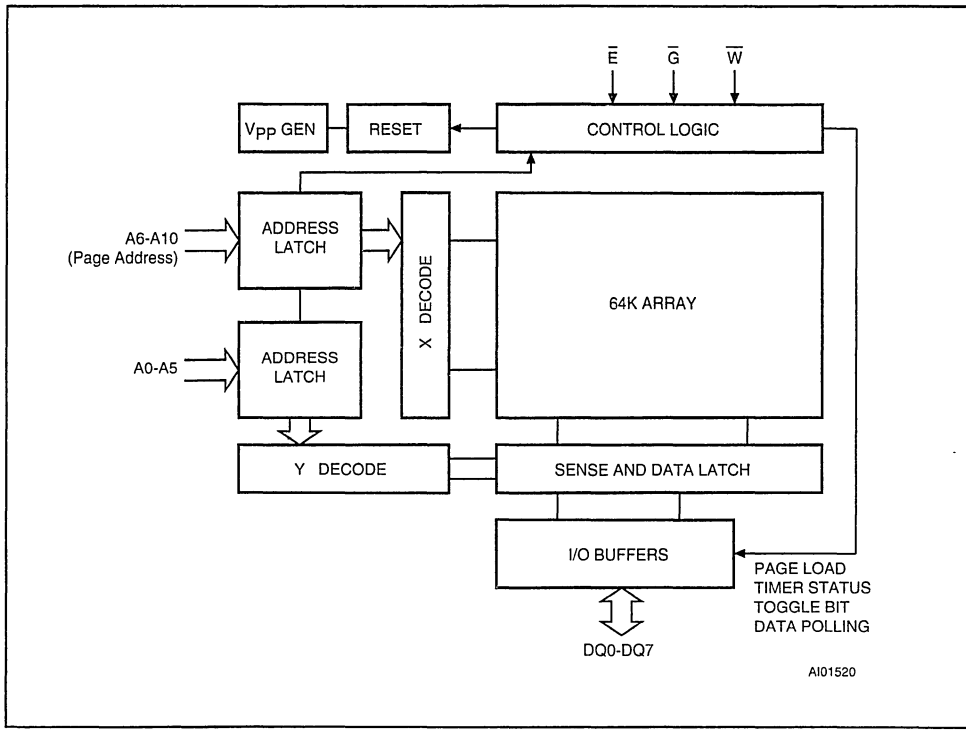
OPERATION

In order to prevent data corruption and inadvertent write operations during power-up, a Power On Reset (POR) circuit resets all internal programming cicuitry. Access to the memory in write mode is allowed after a power-up as specified in Table 7.

Read

The M28C16A/17A is accessed like a static RAM. When $\overline{E}$ and $\overline{G}$ are low with $\overline{W}$ high, the data addressed is presented on the I/O pins. The I/O pins are high impedance when either $\overline{G}$ or $\overline{E}$ is high.

Figure 3. Block Diagram



OPERATION (cont'd)

Write

Write operations are initiated when both $\overline{W}$ and $\overline{E}$ are low and $\overline{G}$ is high. The M28C16A/17A supports both $\overline{E}$ and $\overline{W}$ controlled write cycles. The Address is latched by the falling edge of $\overline{E}$ or $\overline{W}$ which ever occurs last and the Data on the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first. Once initiated the write operation is internally timed until completion.

Page Write

Page write allows up to 32 bytes to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A5 - A10 must be the same for all bytes. The page write can be initiated during any byte write operation.

Following the first byte write instruction the host may send another address and data up to a maximum of t_{WHWH} after the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first. If a transition of $\overline{E}$ or $\overline{W}$ is not detected within t_{WHWH}, the internal programming cycle will start.

Figure 4. Status Bit Assignment

DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
DP	TB	PLTS	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

DP = Data Polling
TB = Toggle Bit
PLTS = Page Load Timer Status

Microcontroller Control Interface

The M28C16A/17A provides two write operation status bits and one status pin that can be used to minimize the system write cycle. These signals are available on the I/O port bits DQ7 or DQ6 of the memory during programming cycle only, or as the $\overline{RB}$ signal on a separate pin.

Data Polling bit (DQ7). During the internal write cycle, any attempt to read the last byte written will produce on DQ7 the complementary value of the previously latched bit. Once the write cycle is finished the true logic value appears on DQ7 in the read cycle.

Table 4. AC Measurement Conditions

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven

Figure 5. AC Testing Input Output Waveforms

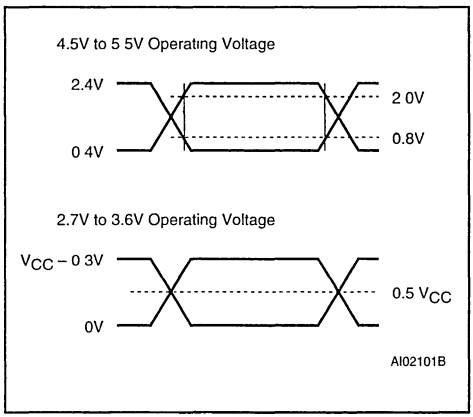


Figure 6. AC Testing Equivalent Load Circuit

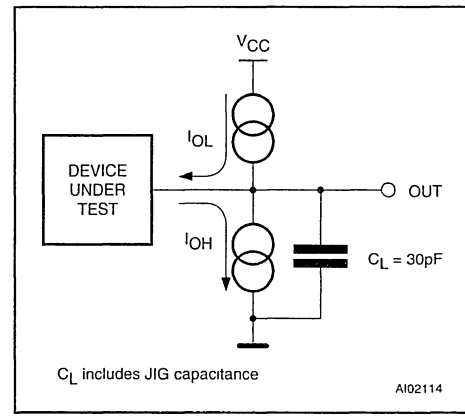


Table 5. Capacitance (1)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics for M28C16A and M28C17A
(T_A = –40 to 85°C, V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{CC} (1)	Supply Current (TTL and CMOS inputs)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL} , f = 5MHz		25	mA
I_{CC1} (1)	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2} (1)	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.3V		50	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –400 µA	2.4		V

Note: 1. All I/O's open circuit

Table 7. Power Up Timing for M28C16A and M28C17A (1)
(T_A = –40 to 85°C, V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Min	Max	Unit
t_{PUR}	Time Delay to Read Operation		1	µs
t_{PUW}	Time Delay to Write Operation (once $V_{CC} \geq V_{WI}$)		10	ms
V_{WI}	Write Inhibit Threshold	1.5	2.5	V

Note: 1. Sampled only, not 100% tested.

Table 8. Read Mode DC Characteristics for M28C16A-W
(T_A = –40 to 85°C, V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		10	µA
I_{LO}	Output Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		10	µA
I_{CC} (1)	Supply Current (TTL and CMOS inputs)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5 MHz		15	mA
I_{CC2} (1)	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.3V$		20	µA
V_{IL}	Input Low Voltage		–0.3	0.6	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.2 V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = –400 µA	0.8 V_{CC}		V

Note: 1. All I/O's open circuit

Table 9. Power Up Timing for M28C16A-W (1)
(T_A = –40 to 85°C, V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Min	Max	Unit
t_{PUR}	Time Delay to Read Operation		1	µs
t_{PUW}	Time Delay to Write Operation (once $V_{CC} \geq V_{WI}$)		10	ms
V_{WI}	Write Inhibit Threshold	1.5	2.5	V

Note: 1 Sampled only, not 100% tested

Table 10. Read Mode AC Characteristics for M28C16A and M28C17A
(T_A = –40 to 85°C, V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	M28C16A / M28C17A				Unit
				-15		-20		
				min	max	min	max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	G = V_{IL}		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		70		80	ns
t_{EHQZ} (1)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	50	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	50	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

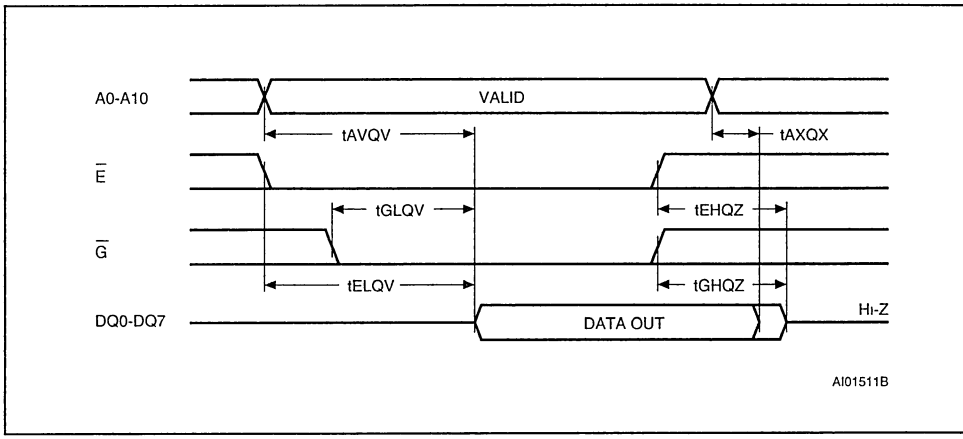
Note: 1 Output Hi-Z is defined as the point at which data is no longer driven.

Table 11. Read Mode AC Characteristics for M28C16-W
(T_A = –40 to 85°C, V_{CC} = 2.7V to 3.6V)

Symbol	Alt	Parameter	Test Condition	M28C16A / M28C17A				Unit
				-25		-30		
				min	max	min	max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		250		300	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	G = V_{IL}		250		300	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		100		100	ns
t_{EHQZ} (1)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	70	0	80	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	70	0	80	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Note: 1. Output Hi-Z is defined as the point at which data is no longer driven.

Figure 7. Read Mode AC Waveforms



Note: Write Enable ($\overline{W}$) = High

Toggle bit (DQ6). The M28C16A/17A offers another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 will toggle from "0" to "1" and "1" to "0" (the first read value is "0") on subsequent attempts to read any address in the memory. When the internal cycle is completed the toggling will stop and the device will be accessible for a new Read or Write operation.

Page Load Timer Status bit (DQ5). In the Page Write mode data may be latched by $\overline{E}$ or $\overline{W}$ up to t_{WHWH} after the previous byte. Up to 32 bytes may be input. The Data output (DQ5) indicates the status of the internal Page Load Timer. DQ5 may be read by asserting Output Enable Low (t_{PLTS}). DQ5 Low indicates the timer is running, High

Table 12. Write Mode AC Characteristics for M28C16A and M28C17A
(T_A = –40 to 85°C, V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E} = V_{IL}$	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W} = V_{IL}$	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		100		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		100		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$		1	µs
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		100		ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		200		ns
t_{WLWH}	tWP	Write Enable Low to Write Enable High		100		ns
t_{WHWH}	t_{BLC}	Byte Load Repeat Cycle Time		0.2	30	µs
t_{WHRH}	t_{WC}	Write Cycle Time			5	ms
t_{WHRL}	t_{DB}	Write Enable High to Ready/Busy Low	Note 1		100	ns
t_{EHRL}	t_{DB}	Chip Enable High to Ready/Busy Low	Note 1		100	ns
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Note: 1. With a 3 3 kΩ external pull-up resistor.

Table 13. Write Mode AC Characteristics for M28C16-W
(T_A = –40 to 85°C, V_{CC} = 2.7V to 3.6V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E}$ = V_{IL}	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W}$ = V_{IL}	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		200		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		200		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}		1	µs
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		200		ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		200		ns
t_{WLWH}	tWP	Write Enable Low to Write Enable High		200		ns
t_{WHWH}	t_{BLC}	Byte Load Repeat Cycle Time		0.4	50	µs
t_{WHRH}	t_{WC}	Write Cycle Time			5	ms
t_{WHRL}	t_{DB}	Write Enable High to Ready/Busy Low	Note 1		250	ns
t_{EHRL}	t_{DB}	Chip Enable High to Ready/Busy Low	Note 1		250	ns
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Note: 1 With a 3 3 kΩ external pull-up resistor.

Figure 8. Write Mode AC Waveforms - Write Enable Controlled

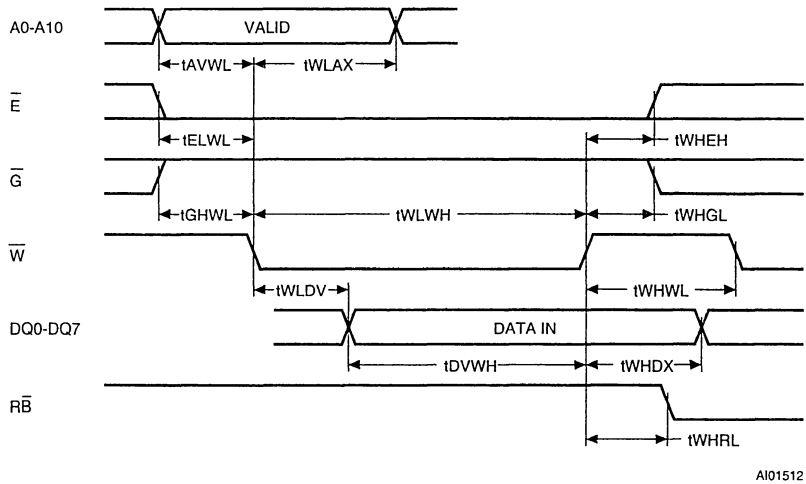


Figure 9. Write Mode AC Waveforms - Chip Enable Controlled

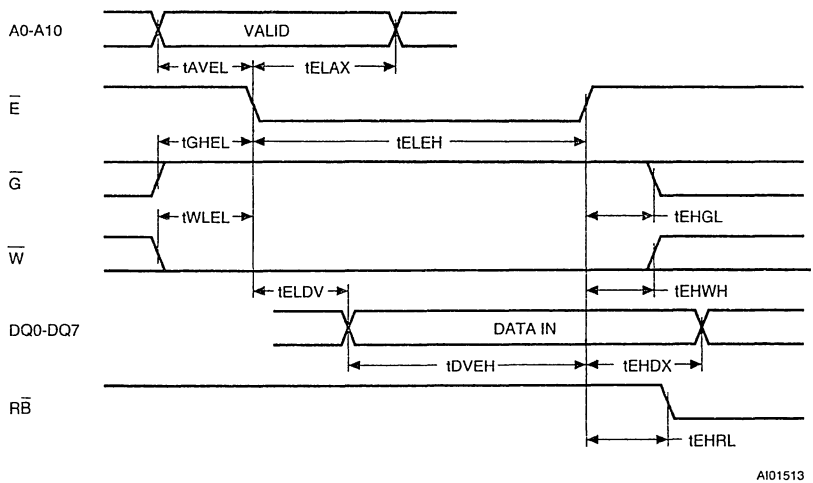


Figure 10. Page Write Mode AC Waveforms - Write Enable Controlled

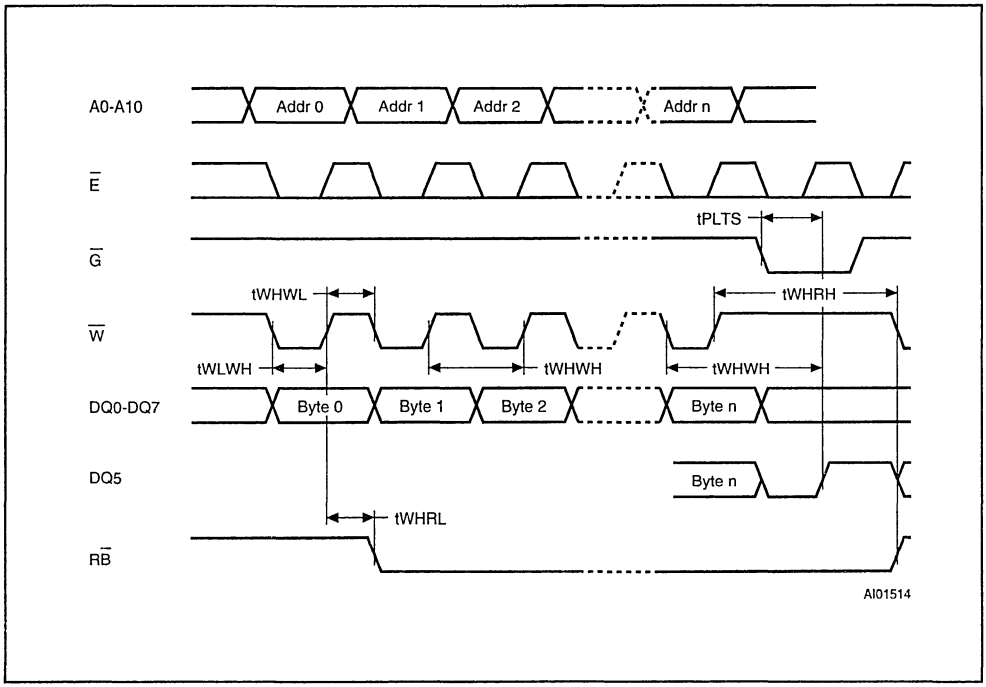


Figure 11. Data Polling Waveform Sequence

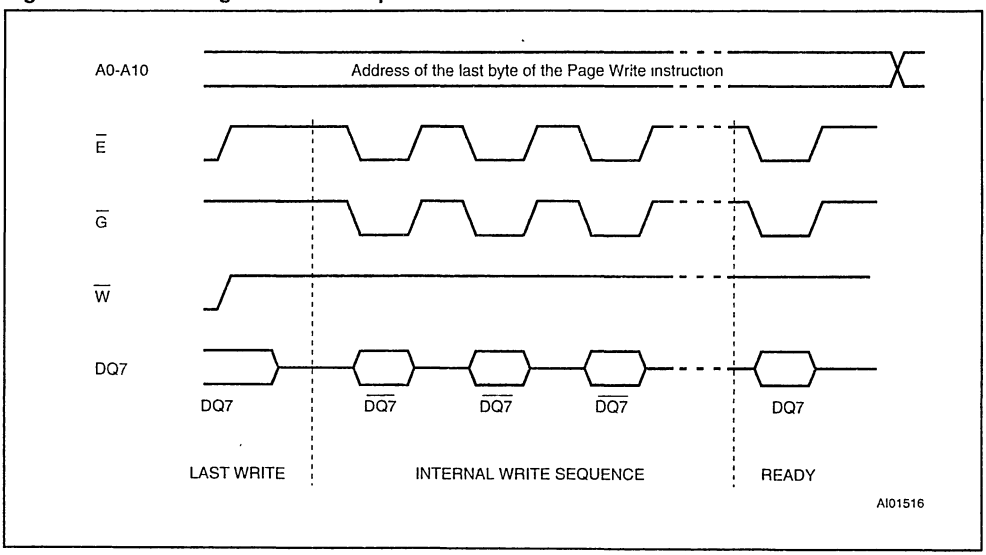
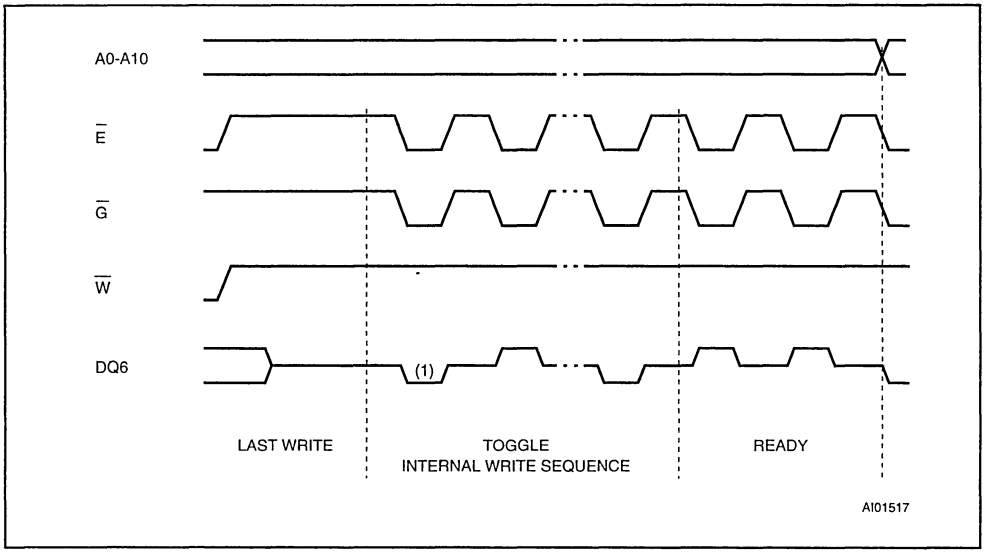
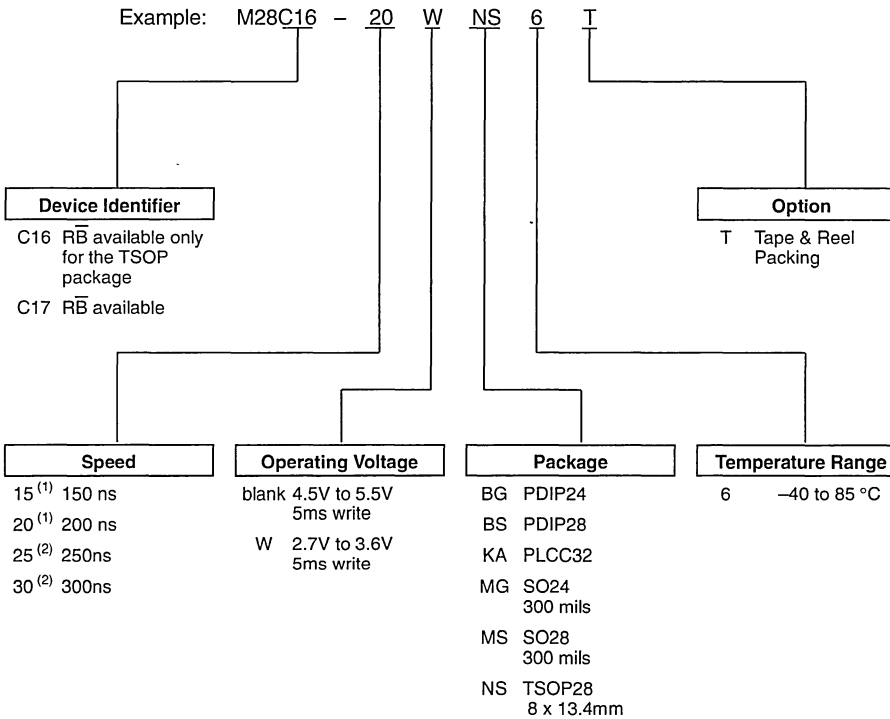


Figure 12. Toggle Bit Waveform Sequence



Note: 1. First Toggle bit is forced to '0'

ORDERING INFORMATION SCHEME



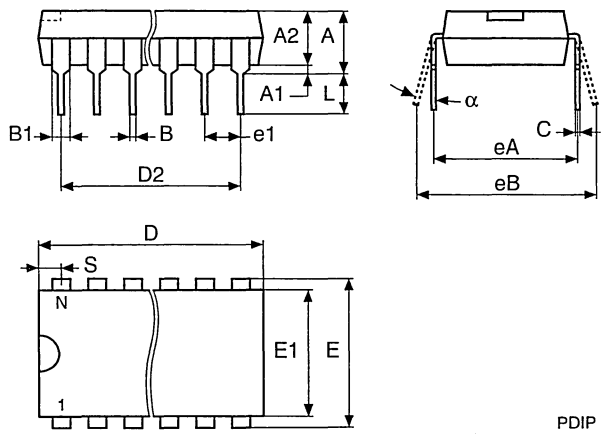
Notes: 1. Available for M28C16A and M28C17A only
2. Available for "W" Operating Voltage only.

Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PDIP24 - 24 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		–	5.08		–	0.200
A1		0.38	–		0.015	–
A2		3.56	4.06		0.140	0.160
B	0.45	–	–	0.018	–	–
B1	1.27	–	–	0.050	–	–
C		0.20	0.30		0.008	0.012
D		31.45	32.20		1.238	1.267
D2	27.94	–	–	1.100	–	–
E	15.24	–	–	0.600	–	–
E1		13.97	14.10		0.550	0.555
e1	2.54	–	–	0.100	–	–
eA	14.99	–	–	0.590	–	–
eB		15.24	17.78		0.600	0.700
L	3.30	–	–	0.130	–	–
S		1.78	2.08		0.070	0.082
α		0°	10°		0°	10°
N	24			24		

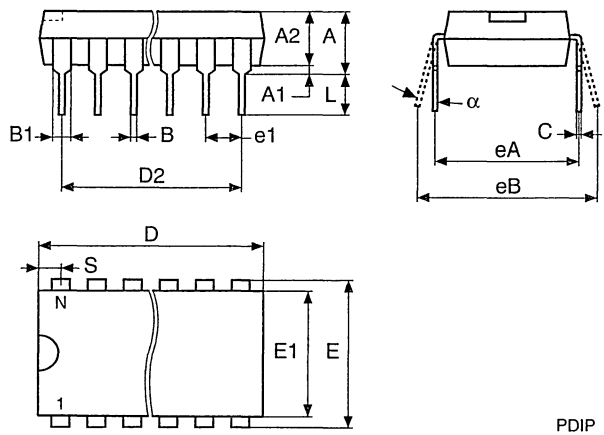


PDIP

Drawing is not to scale.

PDIP28 - 28 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		–	5.08		–	0.200
A1		0.38	–		0.015	–
A2		3.56	4.06		0.140	0.160
B		0.38	0.51		0.015	0.020
B1	1.52	–	–	0.060	–	–
C		0.20	0.30		0.008	0.012
D		36.83	37.34		1.450	1.470
D2	33.02	–	–	1.300	–	–
E	15.24	–	–	0.600	–	–
E1		13.59	13.84		0.535	0.545
e1	2.54	–	–	0.100	–	–
eA	14.99	–	–	0.590	–	–
eB		15.24	17.78		0.600	0.700
L		3.18	3.43		0.125	0.135
S		1.78	2.08		0.070	0.082
α		0°	10°		0°	10°
N	28			28		

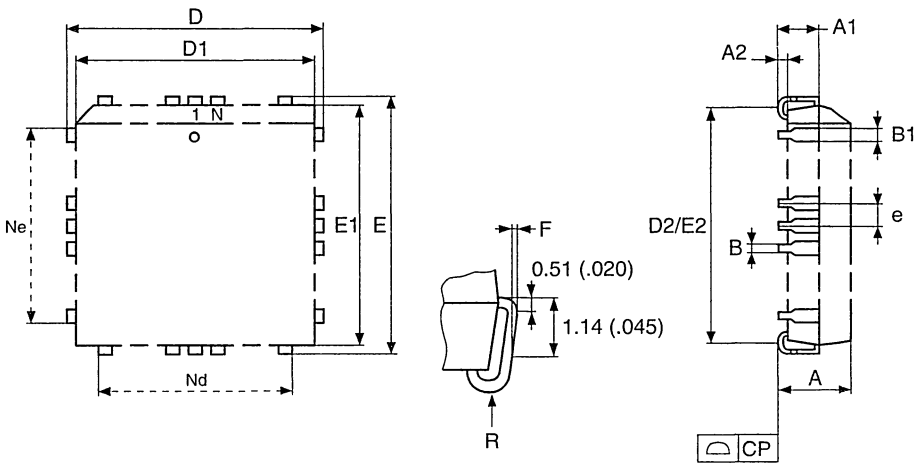


PDIP

Drawing is not to scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
A2		–	0.38		–	0.015
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
F		0.00	0.25		0.000	0.010
R	0.89	–	–	0.035	–	–
N		32			32	
Nd		7			7	
Ne		9			9	
CP			0.10			0.004

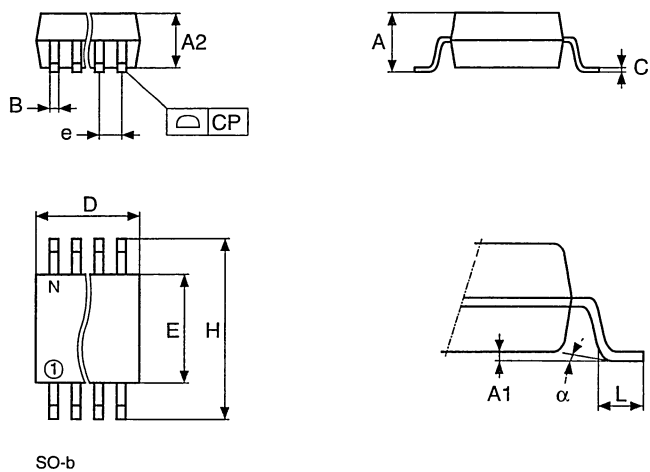


PLCC

Drawing is not to scale.

SO24 - 24 lead Plastic Small Outline, 300 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.46	2.64		0.097	0.104
A1		0.13	0.29		0.005	0.011
A2		2.29	2.39		0.090	0.094
B		0.35	0.48		0.014	0.019
C		0.23	0.32		0.009	0.013
D		15.20	15.60		0.598	0.614
E		7.42	7.59		0.292	0.299
e	1.27	–	–	0.050	–	–
H		10.16	10.41		0.400	0.410
L		0.61	1.02		0.024	0.040
α		0°	8°		0°	8°
N	24			24		
CP			0.10			0.004

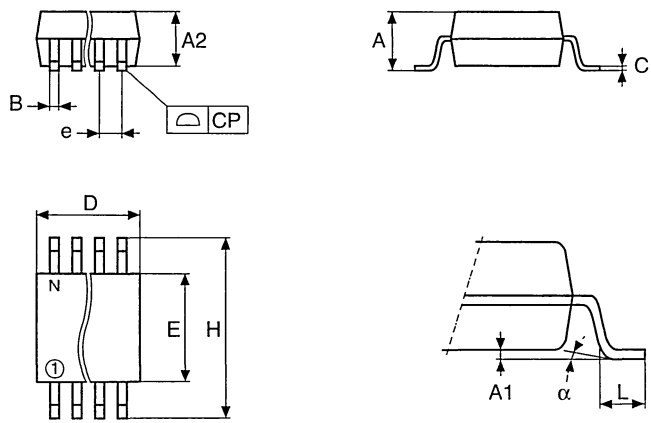


SO-b

Drawing is not to scale.

SO28 - 28 lead Plastic Small Outline, 300 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.46	2.64		0.097	0.104
A1		0.13	0.29		0.005	0.011
A2		2.29	2.39		0.090	0.094
B		0.35	0.48		0.014	0.019
C		0.23	0.32		0.009	0.013
D		17.81	18.06		0.701	0.711
E		7.42	7.59		0.292	0.299
e	1.27	–	–	0.050	–	–
H		10.16	10.41		0.400	0.410
L		0.61	1.02		0.024	0.040
α		0°	8°		0°	8°
N		28			28	
CP			0.10			0.004

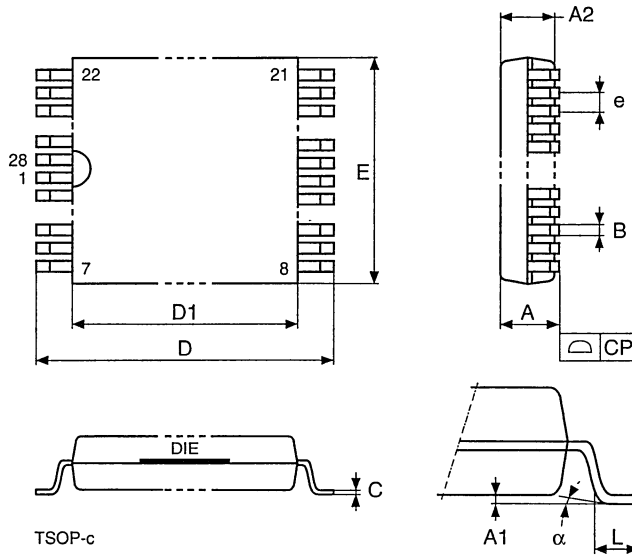


SO-b

Drawing is not to scale

TSOP28 - 28 lead Plastic Thin Small Outline, 8 x 13.4mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.25			0.049
A1			0.20			0.008
A2		0.95	1.15		0.037	0.045
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		13.20	13.60		0.520	0.535
D1		11.70	11.90		0.461	0.469
E		7.90	8.10		0.311	0.319
e	0.55	-	-	0.022	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	28			28		
CP			0.10			0.004



TSOP-c

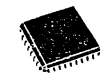
Drawing is not to scale.

M28C16B
M28C17B

16 Kbit (2K x 8) Parallel EEPROM With Software Data Protection

PRELIMINARY DATA

- Fast Access Time: 90 ns at V_{CC}=5V
- Single Supply Voltage:
  - 4.5 V to 5.5 V for M28CxxB
  - 2.7 V to 3.6 V for M28CxxB-W
- Low Power Consumption
- Fast BYTE and PAGE WRITE (up to 64 Bytes)
  - 3 ms at V_{CC}=4.5 V
  - 5 ms at V_{CC}=2.7 V
- Enhanced Write Detection and Monitoring:
  - Data Polling
  - Toggle Bit
  - Page Load Timer Status
- JEDEC Approved Bytewide Pin-Out
- Software Data Protection
- 100000 Erase/Write Cycles (minimum)
- Data Retention (minimum): 40 Years



PLCC32 (K)

DESCRIPTION

The M28C16B and M28C17B devices consist of 2048x8 bits of low power, parallel EEPROM, fabricated with STMicroelectronics' proprietary single polysilicon CMOS technology. The devices offer fast access time, with low power dissipation, and require a single voltage supply.

Table 1. Signal Names

A0-A10	Address Input
DQ0-DQ7	Data Input / Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$R\overline{B}$	Ready/Busy (M28C17B only)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

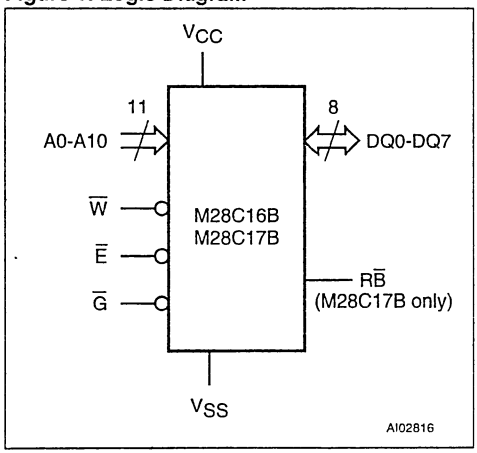
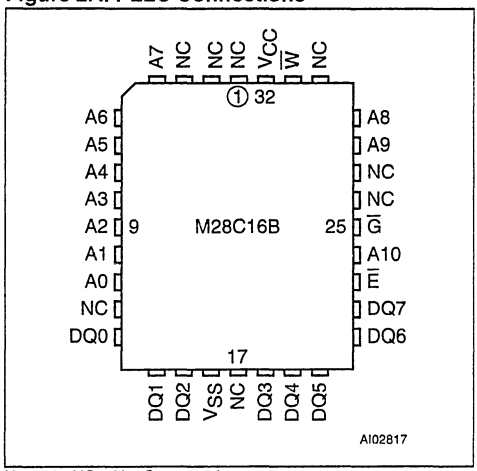
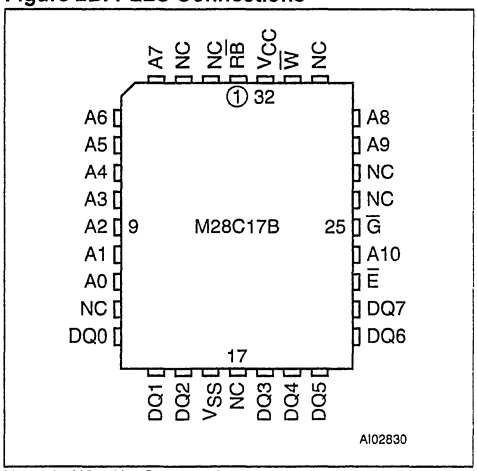


Figure 2A. PLLC Connections



Note: 1. NC = Not Connected

Figure 2B. PLLC Connections



Note: 1. NC = Not Connected

The M28C17B is like the M28C16B in every way, except that it has an extra ready/busy ($\overline{RB}$) output.

The device has been designed to offer a flexible microcontroller interface, featuring software handshaking, with Data Polling and Toggle Bit. The device supports a 64 byte Page Write operation. Software Data Protection (SDP) is also supported, using the standard JEDEC algorithm.

SIGNAL DESCRIPTION

The external connections to the device are summarized in Table 1, and their use in Table 3.

Addresses (A0-A10). The address inputs are used to select one byte from the memory array during a read or write operation.

Data In/Out (DQ0-DQ7). The contents of the data byte are written to, or read from, the memory array through the Data I/O pins.

Chip Enable ($\overline{E}$). The chip enable input must be held low to enable read and write operations. When Chip Enable is high, power consumption is reduced.

Output Enable ($\overline{G}$). The Output Enable input controls the data output buffers, and is used to initiate read operations.

Write Enable ($\overline{W}$). The Write Enable input controls whether the addressed location is to be read, from or written to.

Ready/$\overline{Busy}$ ($\overline{RB}$). Ready/$\overline{Busy}$ (on the M28C17B only) is an open drain output that can be used to detect the end of the internal write cycle.

DEVICE OPERATION

In order to prevent data corruption and inadvertent write operations, an internal V_{CC} comparator inhibits the Write operations if the V_{CC} voltage is lower than V_{WI} (see Table 4A). Once the voltage applied on the V_{CC} pin goes over the V_{WI} threshold ($V_{CC}>V_{WI}$), write access to the memory is allowed after a time-out t_{PUW}, as specified in Table 4A.

Further protection against data corruption is offered by the $\overline{E}$ and $\overline{W}$ low pass filters: any glitch, on the $\overline{E}$ and $\overline{W}$ inputs, with a pulse width less than 10 ns (typical) is internally filtered out to prevent inadvertent write operations to the memory.

Read

The device is accessed like a static RAM. When $\overline{E}$ and $\overline{G}$ are low, and $\overline{W}$ is high, the contents of the addressed location are presented on the I/O pins. Otherwise, when either $\overline{G}$ or $\overline{E}$ is high, the I/O pins revert to their high impedance state.

Write

Write operations are initiated when both $\overline{W}$ and $\overline{E}$ are low and $\overline{G}$ is high. The device supports both $\overline{W}$-controlled and $\overline{E}$-controlled write cycles (as shown in Figure 11 and Figure 12). The address is latched during the falling edge of $\overline{W}$ or $\overline{E}$ (which ever occurs later) and the data is latched on the rising edge of $\overline{W}$ or $\overline{E}$ (which ever occurs first). After a delay, t_{WLQ5H}, that cannot be shorter than the value specified in Table 10A, the internal write cycle starts. It continues, under internal timing control, until the write operation is complete. The commencement of this period can be detected by reading the Page Load Timer Status on DQ5. The

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	-40 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C
V_{CC}	Supply Voltage	-0.3 to 6.5	V
V_{IO}	Input or Output Voltage	-0.6 to V_{CC}+0.6	V
V_I	Input Voltage	-0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]	4000	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100 pF, 1500 Ω)

Figure 3. Block Diagram

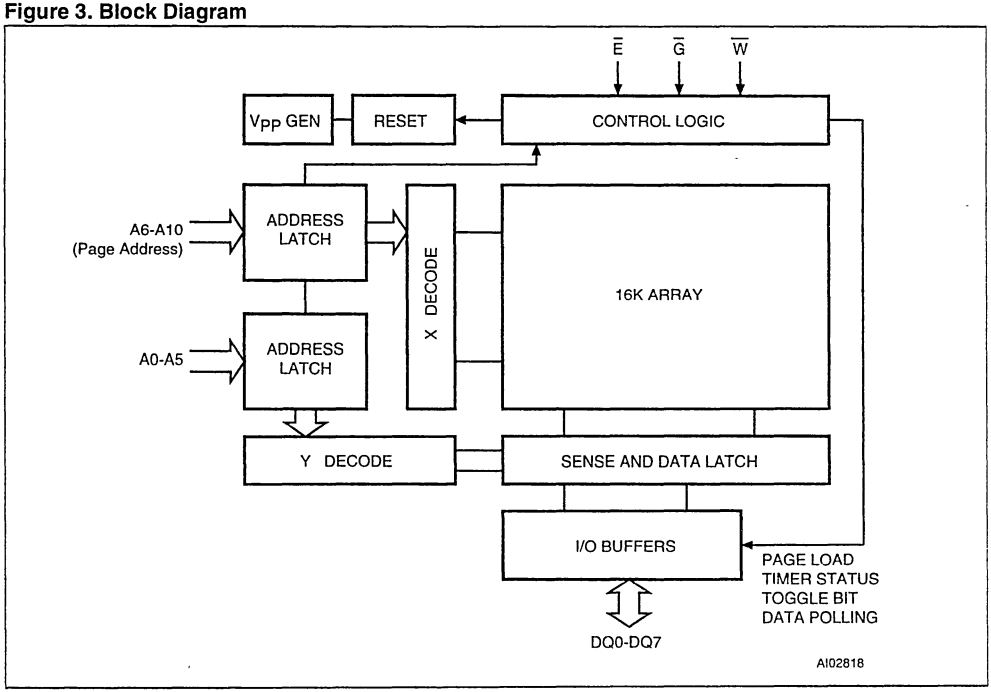


Table 3. Operating Modes [1]

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7
Stand-by	1	X	X	Hi-Z
Output Disable	X	1	X	Hi-Z
Write Disable	X	X	1	Hi-Z
Read	0	0	1	Data Out
Write	0	1	0	Data In
Chip Erase	0	V	0	Hi-Z

Note: 1. 0=V_{IL}; 1=V_{IH}; X = V_{IH} or V_{IL}; V=12V ± 5%.

end of the cycle can be detected by reading the status of the Data Polling and the Toggle Bit functions on DQ7 and DQ6.

Page Write

The Page Write mode allows up to 64 bytes to be written on a single page in a single go. This is achieved through a series of successive Write operations, no two of which are separated by more than the t_{WLQ5H} value (as specified in Table 10A).

The page write can be initiated during any byte write operation. Following the first byte write instruction the host may send another address and data with a minimum data transfer rate of:
$1/t_{WLQ5H}$.

The internal write cycle can start at any instant after t_{WLQ5H}. Once initiated, the write operation is internally timed, and continues, uninterrupted, until completion.

All bytes must be located on the same page address (A10-A6 must be the same for all bytes). Otherwise, the Page Write operation is not executed.

As with the single byte Write operation, described above, the DQ5, DQ6 and DQ7 lines can be used to detect the beginning and end of the internally controlled phase of the Page Write cycle.

Software Data Protection (SDP)

The device offers a software-controlled write-protection mechanism that allows the user to inhibit all write operations to the device. This can be useful for protecting the memory from inadvertent write cycles that may occur during periods of instability (uncontrolled bus conditions when excessive noise is detected, or when power supply levels are outside their specified values).

By default, the device is shipped in the "unprotected" state: the memory contents can be freely changed by the user. Once the Software Data Protection Mode is enabled, all write commands are

Table 4A. Power-Up Timing[1] for M28CxxB (5V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 4.5 to 5.5 V)

Symbol	Parameter	Min.	Max.	Unit
t_{PUR}	Time Delay to Read Operation		1	µs
t_{PUW}	Time Delay to Write Operation (once $V_{CC} \geq V_{WI}$)		10	ms
V_{WI}	Write Inhibit Threshold	3.0	4.2	V

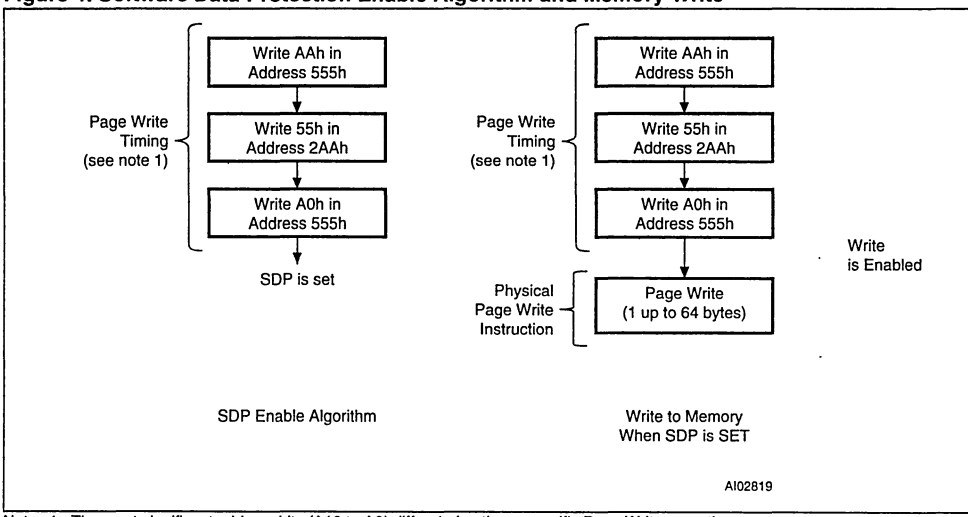
Note: 1. Sampled only, not 100% tested.

Table 4B. Power-Up Timing[1] for M28CxxB-W (3V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 2.7 to 3.6 V)

Symbol	Parameter	Min.	Max.	Unit
t_{PUR}	Time Delay to Read Operation		1	µs
t_{PUW}	Time Delay to Write Operation (once $V_{CC} \geq V_{WI}$)		15	ms
V_{WI}	Write Inhibit Threshold	1.5	2.5	V

Note: 1. Sampled only, not 100% tested.

Figure 4. Software Data Protection Enable Algorithm and Memory Write



Note: 1. The most significant address bits (A10 to A6) differ during these specific Page Write operations.

ignored, and have no effect on the memory contents.

The device remains in this mode until a valid Software Data Protection disable sequence is received. The device reverts to its "unprotected" state.

The status of the Software Data Protection (enabled or disabled) is represented by a non-volatile latch, and is remembered across periods of the power being off.

The Software Data Protection Enable command consists of the writing of three specific data bytes to three specific memory locations (each location being on a different page), as shown in Figure 4.

Similarly to disable the Software Data Protection, the user has to write specific data bytes into six different locations, as shown in Figure 6. This complex series of operations protects against the chance of inadvertent enabling or disabling of the Software Data Protection mechanism.

Figure 5. Status Bit Assignment

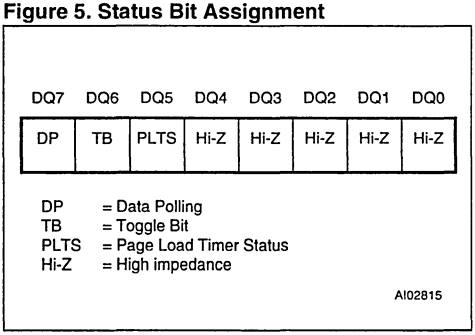


Figure 6. Software Data Protection Disable Algorithm

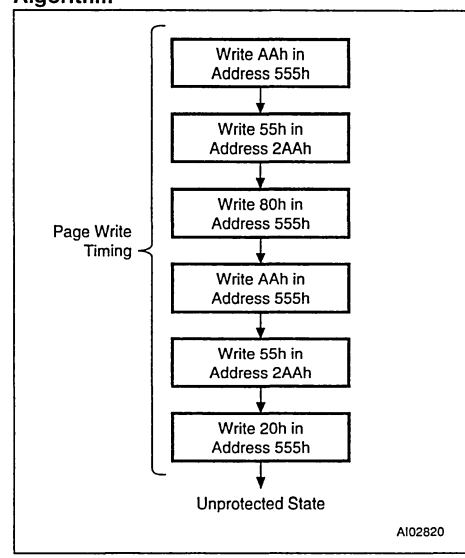


Figure 7. Chip Erase AC Waveforms

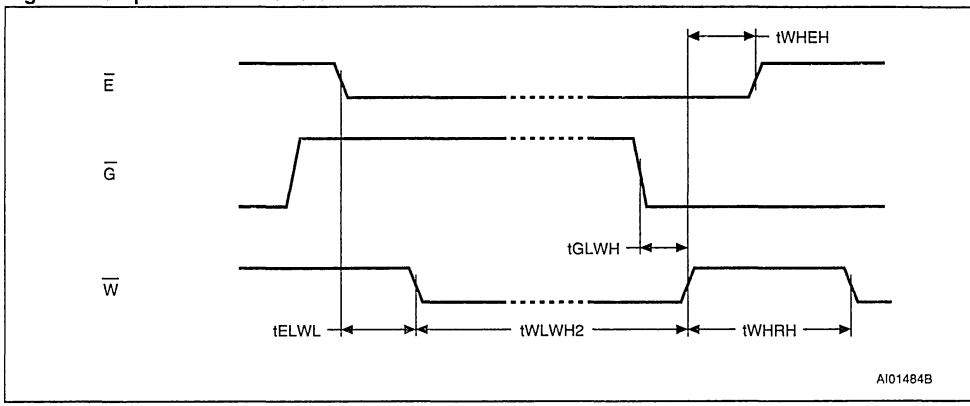


Table 5. Chip Erase AC Characteristics[1]
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 4.5 to 5.5 V or 2.7 to 3.6 V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
t_{ELWL}	Chip Enable Low to Write Enable Low	$\overline{G}$ = V_{CC} + 7V	1		µs
t_{WHEH}	Write Enable High to Chip Enable High	$\overline{G}$ = V_{CC} + 7V	0		ns
t_{WLWH2}	Write Enable Low to Write Enable High	$\overline{G}$ = V_{CC} + 7V	10		ms
t_{GLWH}	Output Enable Low to Write Enable High	$\overline{G}$ = V_{CC} + 7V	1		µs
t_{WHRH}	Write Enable High to Write Enable Low	$\overline{G}$ = V_{CC} + 7V		3	ms

Note: 1. Sampled only, not 100% tested.

When SDP is enabled, the memory array can still have data written to it, but the sequence is more complex (and hence better protected from inadvertent use). The sequence is as shown in Figure 4. This consists of an unlock key, to enable the write action, at the end of which the SDP continues to be enabled. This allows the SDP to be enabled, and data to be written, within a single Write cycle (t_{WC}).

Software Chip Erase

The contents of the entire memory are erased (set to FFh) by holding Chip Enable ($\overline{E}$) low, and holding Output Enable ($\overline{G}$) at V_{CC}+7.0V. The chip is cleared when a 10 ms low pulse is applied to the Write Enable ($\overline{W}$) signal (see Figure 7 and Table 5 for details).

Status Bits

The devices provide three status bits (DQ7, DQ6 and DQ5), for use during write operations. These allow the application to use the write time latency of the device for getting on with other work. These signals are available on the I/O port bits DQ7, DQ6 and DQ5 (but only during programming cycle, once a byte or more has been latched into the memory).

Data Polling bit (DQ7). The internally timed write cycle starts after t_{WLQ5H} (defined in Table 10A) has elapsed since the previous byte was latched in to the memory. The value of the DQ7 bit of this last byte, is used as a signal throughout this write operation: it is inverted while the internal write operation is underway, and is inverted back to its original value once the operation is complete.

Toggle bit (DQ6). The device offers another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 toggles from '0' to '1' and '1' to '0' (the first read value being '0') on subsequent attempts to read any byte of the memory. When the internal write cycle is complete, the toggling is stopped, and the values read on DQ7-DQ0 are those of the addressed memory byte. This indicates that the device is again available for new Read and Write operations.

Page Load Timer Status bit (DQ5). An internal timer is used to measure the period between suc-

Table 6A. Read Mode DC Characteristics for M28CxxB (5V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 4.5 to 5.5 V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$0 V \le V_{IN} \le V_{CC}$		10	µA
I_{LO}	Output Leakage Current	$0 V \le V_{OUT} \le V_{CC}$		10	µA
I_{CC} [1]	Supply Current (TTL inputs)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5 MHz		30	mA
	Supply Current (CMOS inputs)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5 MHz		25	mA
I_{CC1} [1]	Supply Current (Stand-by) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2} [1]	Supply Current (Stand-by) CMOS	$\overline{E} > V_{CC} - 0.3V$		100	µA
V_{IL}	Input Low Voltage		-0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Note: 1. All inputs and outputs open circuit

Table 6B. Read Mode DC Characteristics for M28CxxB-W (3V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 2.7 to 3.6 V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$0 V \le V_{IN} \le V_{CC}$		10	µA
I_{LO}	Output Leakage Current	$0 V \le V_{OUT} \le V_{CC}$		10	µA
I_{CC} [1]	Supply Current (CMOS inputs)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5 MHz, V_{CC} = 3.3V		8	mA
		$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5 MHz, V_{CC} = 3.6V		10	mA
I_{CC2} [1]	Supply Current (Stand-by) CMOS	$\overline{E} > V_{CC} - 0.3V$		20	µA
V_{IL}	Input Low Voltage		-0.3	0.6	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		0.2 V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	0.8 V_{CC}		V

Note. 1. All inputs and outputs open circuit

cessive Write operations, up to t_{WLQ5H} (defined in Table 10A). The DQ5 line is held low to show when this timer is running (hence showing that the device has received one write operation, and is waiting for the next). The DQ5 line is held high when the counter has overflowed (hence showing that the device is now starting the internal write to the memory array).

Table 7. Input and Output Parameters[1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 8. AC Measurement Conditions

Input Rise and Fall Times	≤ 20 ns
Input Pulse Voltages	0.4 V to 2.4 V
Input and Output Timing Reference Voltages	0.8 V to 2.0 V

Figure 8. AC Testing Input Output Waveforms

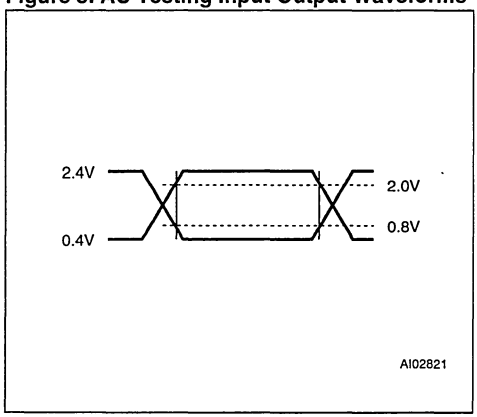


Figure 9. AC Testing Equivalent Load Circuit

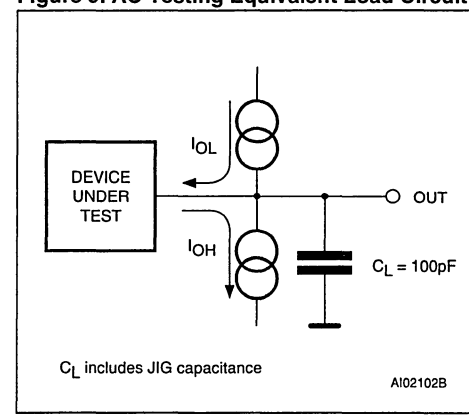


Table 9A. Read Mode AC Characteristics for M28CxxB (5V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 4.5 to 5.5 V)

Symbol	Alt.	Parameter	Test Condition	M28CxxB				Unit
				-90		-12		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		90		120	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		90		120	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		40		45	ns
t_{EHQZ}[1]	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	40	0	45	ns
t_{GHQZ}[1]	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	40	0	45	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Note: 1. Output Hi-Z is defined as the point at which data is no longer driven.

Table 9B. Read Mode AC Characteristics for M28CxxB-W (3V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 2.7 to 3.6 V)

Symbol	Alt.	Parameter	Test Condition	M28CxxB-W				Unit
				-12		-15		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120		150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120		150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		80		80	ns
t_{EHQZ}[1]	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	45	0	50	ns
t_{GHQZ}[1]	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	45	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Note: 1. Output Hi-Z is defined as the point at which data is no longer driven.

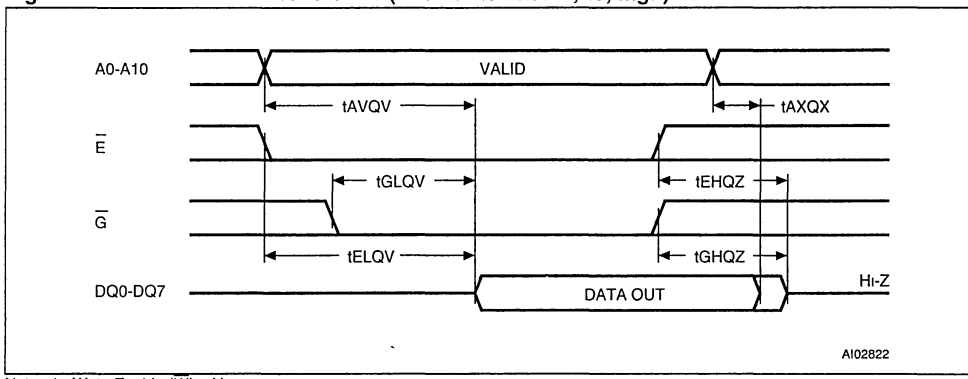
Table 10A. Write Mode AC Characteristics for M28CxxB (5V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 4.5 to 5.5 V)

Symbol	Alt.	Parameter	Test Condition	M28C17B		Unit
				Min	Max	
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E}$ = V_{IL}	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W}$ = V_{IL}	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		50		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		50		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}		1	µs
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		50		ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		50		ns
t_{WLQ5H}	t_{BLC}	Time-out After the Last Byte Write		100		µs
t_{Q5HQ5X}	t_{WC}	Write Cycle Time			3	ms
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Table 10B. Write Mode AC Characteristics for M28CxxB-W (3V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 2.7 to 3.6 V)

Symbol	Alt.	Parameter	Test Condition	M28C17B-xxW		Unit
				Min	Max	
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E} = V_{IL}$	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W} = V_{IL}$	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		100		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		100		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$		1	µs
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		100	1000	ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		50	1000	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		100		ns
t_{WLQ5H}	t_{BLC}	Time-out after the last byte write		100		µs
t_{Q5HQ5X}	t_{WC}	Write Cycle Time			5	ms
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Figure 10. Read Mode AC Waveforms (with Write Enable, $\overline{W}$, high)



Note: 1. Write Enable ($\overline{W}$) = V_{IH}

Figure 11. Write Mode AC Waveforms (Write Enable, $\overline{W}$, controlled)

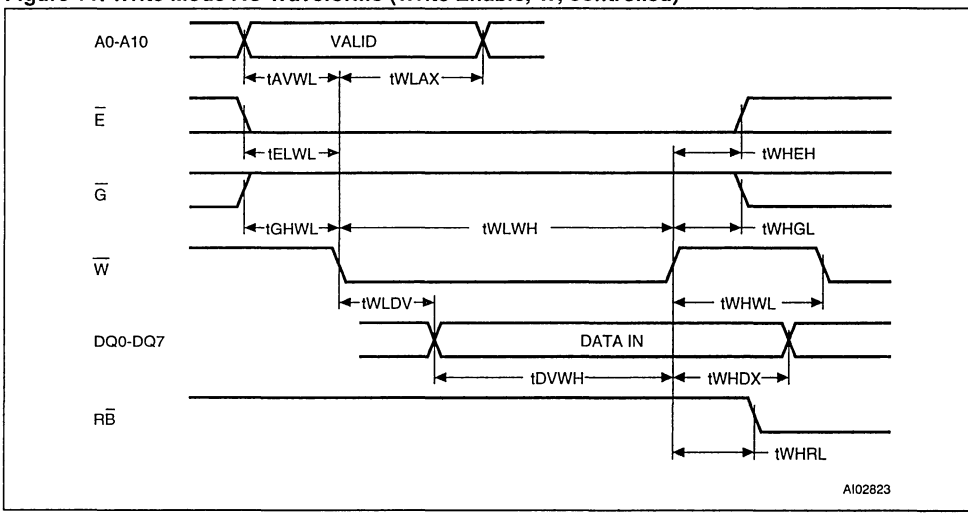


Figure 12. Write Mode AC Waveforms (Chip Enable, $\overline{E}$, controlled)

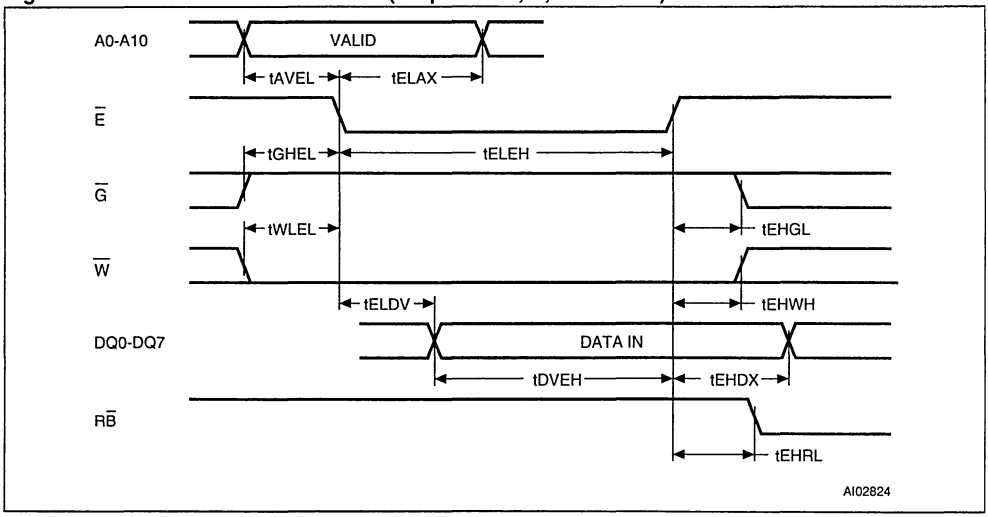


Figure 13. Page Write Mode AC Waveforms (Write Enable, $\overline{W}$, controlled)

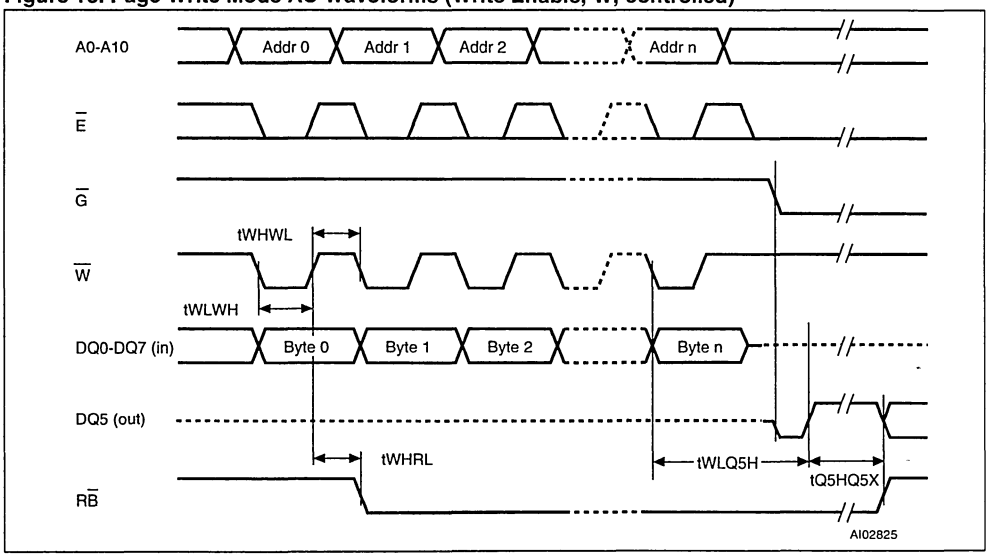
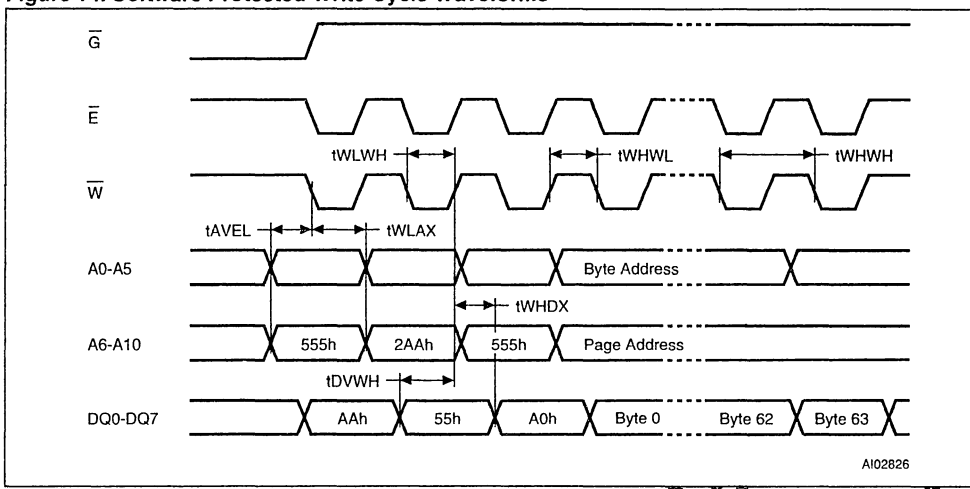


Figure 14. Software Protected Write Cycle Waveforms



Note. 1. A10 to A6 must specify the same page address during each high-to-low transition of $\overline{W}$ (or $\overline{E}$). $\overline{G}$ must be high only when $\overline{W}$ and $\overline{E}$ are both low

Figure 15. Data Polling Sequence Waveforms

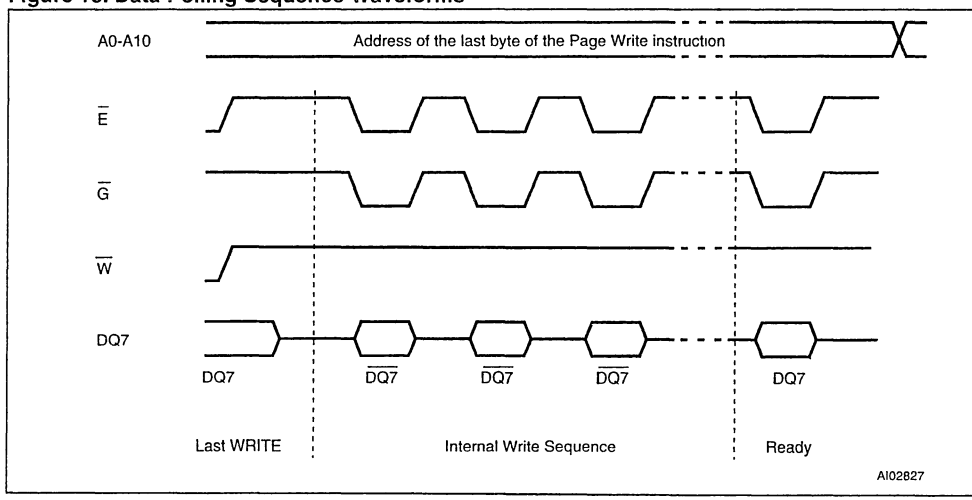
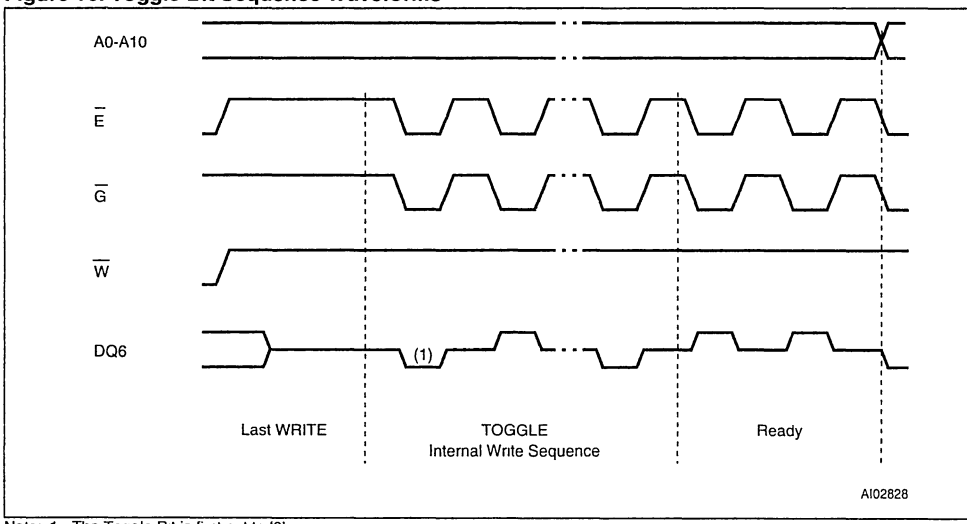


Figure 16. Toggle Bit Sequence Waveforms



Note: 1. The Toggle Bit is first set to '0'.

Table 11. Ordering Information Scheme

Example: M28C16 – 120 W K 6 TR

Ready/Busy

16 Pin 1 = Not Connected

17 Pin 1 = Ready/Busy

Speed

90 90 ns (5V range only)

120 120 ns

150 150 ns (3V range only)

Operating Voltage

blank 4.5 V to 5.5 V

W 2.7 V to 3.6 V

Option

TR Tape and Reel Packing

Temperature Range

1 0 °C to 70 °C

6 –40 °C to 85 °C

Package

K PLCC32

ORDERING INFORMATION

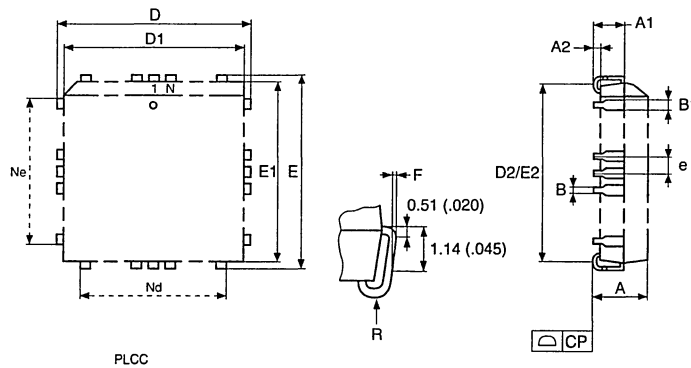
Devices are shipped from the factory with the memory content set at all '1's (FFh).

The notation used for the device number is as shown in Table 11. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 12. PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
A2		–	0.38		–	0.015
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
F		0.00	0.25		0.000	0.010
R	0.89	–	–	0.035	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

Figure 17. PLCC (K)

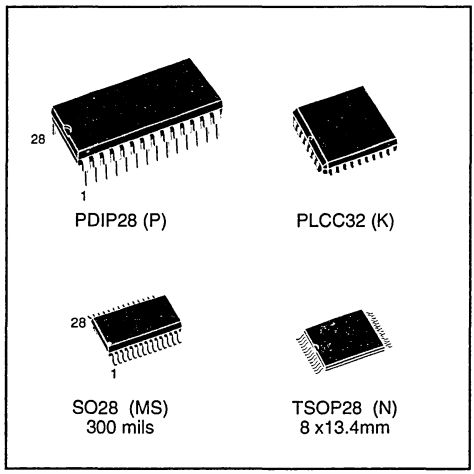


Note: 1. Drawing is not to scale.

M28C64C
M28C64X

64 Kbit (8Kb x8) Parallel EEPROM

- FAST ACCESS TIME: 150ns
- SINGLE 5V ± 10% SUPPLY VOLTAGE
- LOW POWER CONSUMPTION
- FAST WRITE CYCLE
  - 32 Bytes Page Write Operation
  - Byte or Page Write Cycle: 5ms
- ENHANCED END OF WRITE DETECTION
  - Ready/Busy Open Drain Output (for M28C64C product only)
  - Data Polling
  - Toggle Bit
- PAGE LOAD TIMER STATUS BIT
- HIGH RELIABILITY SINGLE POLYSILICON, CMOS TECHNOLOGY
  - Endurance >100,000 Erase/Write Cycles
  - Data Retention >40 Years
- JEDEC APPROVED BYTEWIDE PIN OUT



DESCRIPTION

The M28C64C is an 8 Kbit x8 low power Parallel EEPROM fabricated with STMicroelectronics proprietary single polysilicon CMOS technology. The device offers fast access time with low power dissipation and requires a 5V power supply.

The circuit has been designed to offer a flexible microcontroller interface featuring both hardware and software handshaking mode with Ready/Busy, Data Polling and Toggle Bit. The M28C64C supports 32 byte page write operation.

Table 1. Signal Names

A0 - A12	Address Input
DQ0 - DQ7	Data Input / Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$R\overline{B}$	Ready / Busy
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

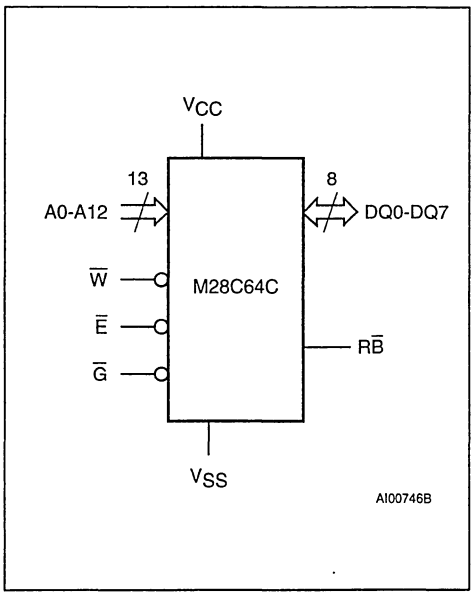
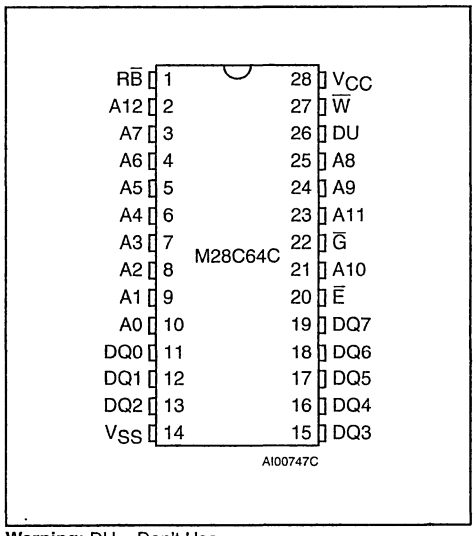
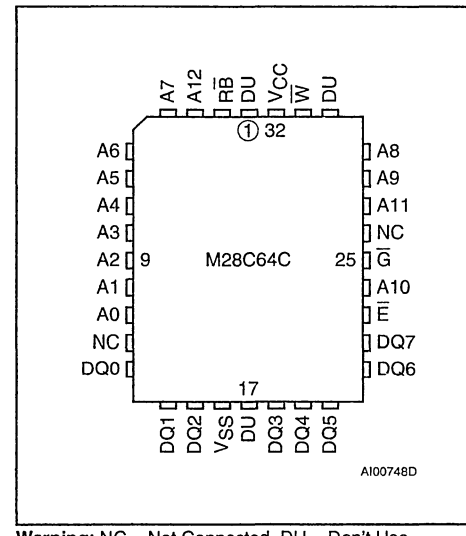


Figure 2A. DIP Pin Connections



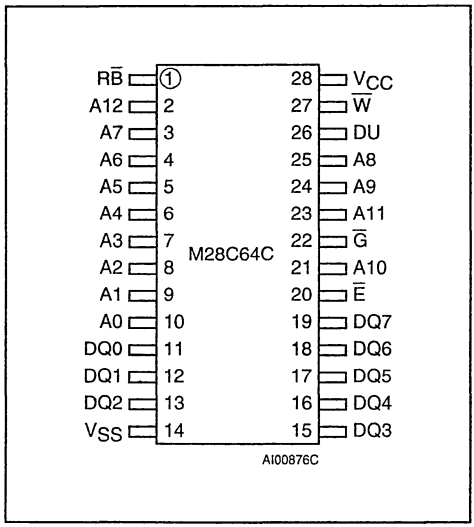
Warning: DU = Don't Use.

Figure 2B. LCC Pin Connections



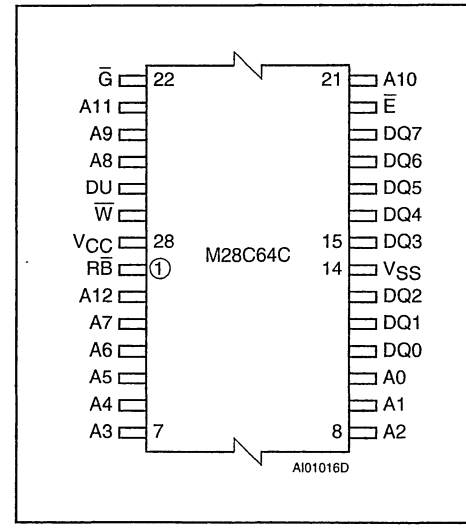
Warning: NC = Not Connected, DU = Don't Use.

Figure 2C. SO Pin Connections



Warning: DU = Don't Use.

Figure 2D. TSOP Pin Connections



Warning: DU = Don't Use.

PIN DESCRITPION

Addresses (A0-A12). The address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{E}$). The chip enable input must be low to enable all read/write operations. When Chip Enable is high, power consumption is reduced.

Output Enable ($\overline{G}$). The Output Enable input controls the data output buffers and is used to initiate read operations.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	– 40 to 125	°C
T_{STG}	Storage Temperature Range	– 65 to 150	°C
V_{CC}	Supply Voltage	– 0.3 to 6.5	V
V_{IO}	Input/Output Voltage	– 0.3 to V_{CC} +0.6	V
V_I	Input Voltage	– 0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)	2000	V

Note: Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Operating Modes

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	Data In
Standby / Write Inhibit	V_{IH}	X	X	Hi-Z
Write Inhibit	X	X	V_{IH}	Data Out or Hi-Z
Write Inhibit	X	V_{IL}	X	Data Out or Hi-Z
Output Disable	X	V_{IH}	X	Hi-Z

Note: X = V_{IH} or V_{IL}

Data In/ Out (DQ0 - DQ7). Data is written to or read from the M28C64C through the I/O pins.

Write Enable ($\overline{W}$). The Write Enable input controls the writing of data to the M28C64C.

Ready/Busy ($R\overline{B}$). Ready/Busy is an open drain output that can be used to detect the end of the internal write cycle.

OPERATION

In order to prevent data corruption and inadvertent write operations during power-up, a Power On Reset (POR) circuit resets all internal programming circuitry. Access to the memory in write mode is allowed after a power-up as specified in Table 6.

Read

The M28C64C is accessed like a static RAM. When $\overline{E}$ and $\overline{G}$ are low with $\overline{W}$ high, the data addressed is presented on the I/O pins. The I/O pins are high impedance when either $\overline{G}$ or $\overline{E}$ is high.

Write

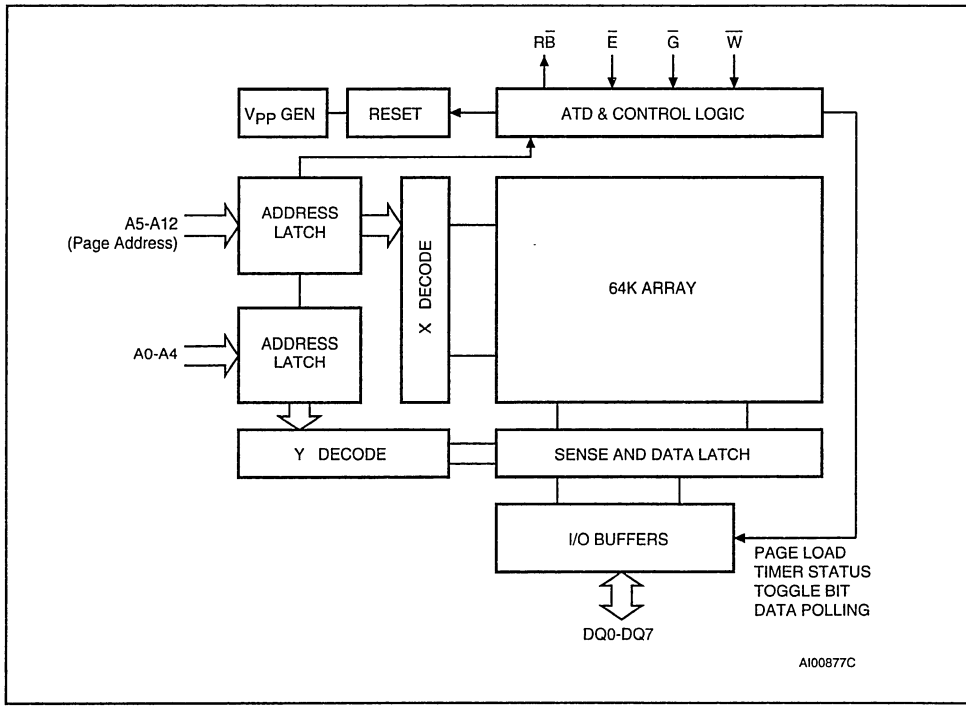
Write operations are initiated when both $\overline{W}$ and $\overline{E}$ are low and $\overline{G}$ is high. The M28C64C supports both $\overline{E}$ and $\overline{W}$ controlled write cycles. The Address is latched by the falling edge of $\overline{E}$ or $\overline{W}$ which ever occurs last and the Data on the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first. Once initiated the write operation is internally timed until completion.

Page Write

Page write allows up to 32 bytes to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A5 - A12 must be the same for all bytes. The page write can be initiated during any byte write operation.

Following the first byte write instruction the host may send another address and data up to a maximum of 100µs after the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first (t_{BLC}). If a transition of $\overline{E}$ or $\overline{W}$ is not detected within 100µs, the internal programming cycle will start.

Figure 3. Block Diagram



Microcontroller Control Interface

The M28C64C provides two write operation status bits and one status pin that can be used to minimize the system write cycle. These signals are available on the I/O port bits DQ7 or DQ6 of the memory during programming cycle only, or as the RB signal on a separate pin.

Figure 4. Status Bit Assignment

DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
DP	TB	PLTS	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

DP = Data Polling
TB = Toggle Bit
PLTS = Page Load Timer Status

Data Polling bit (DQ7). During the internal write cycle, any attempt to read the last byte written will produce on DQ7 the complementary value of the previously latched bit. Once the write cycle is finished the true logic value appears on DQ7 in the read cycle.

Toggle bit (DQ6). The M28C64C offers another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 will toggle from "0" to "1" and "1" to "0" (the first read value is "0") on subsequent attempts to read any address in the memory. When the internal cycle is completed the toggling will stop and the device will be accessible for a new Read or Write operation.

Page Load Timer Status bit (DQ5). In the Page Write mode data may be latched by E or W up to 100µs after the previous byte. Up to 32 bytes may be input. The Data output (DQ5) indicates the status of the internal Page Load Timer. DQ5 may be read by asserting Output Enable Low (t_{PLTS}). DQ5 Low indicates the timer is running, High indicates time-out after which the write cycle will start and no new data may be input.

Ready/Busy pin. The RB pin provides a signal at its open drain output which is low during the erase/write cycle, but which is released at the completion of the programming cycle.

Table 4. AC Measurement Conditions

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages	0.4V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 5. AC Testing Input Output Waveforms

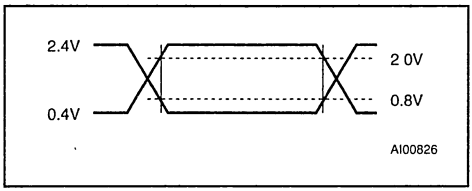


Figure 6. AC Testing Equivalent Load Circuit

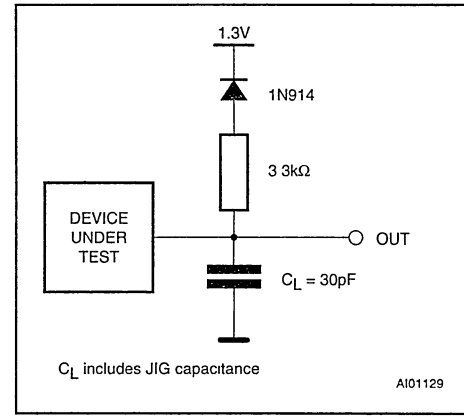


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics (T_A = 0 to 70°C or –40 to 85°C, V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{CC} (1)	Supply Current (TTL and CMOS inputs)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL} , f = 5 MHz		30	mA
I_{CC1} (1)	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		2	mA
I_{CC2} (1)	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} –0.3V		100	µA
V_{IL}	Input Low Voltage		– 0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} +0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –400 µA	2.4		V

Note: 1. All I/O's open circuit.

Table 7. Power Up Timing (1) (T_A = 0 to 70°C or –40 to 85°C, V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Min	Max	Unit
t_{PUR}	Time Delay to Read Operation	1		µs
t_{PUW}	Time Delay to Write Operation	10		ms

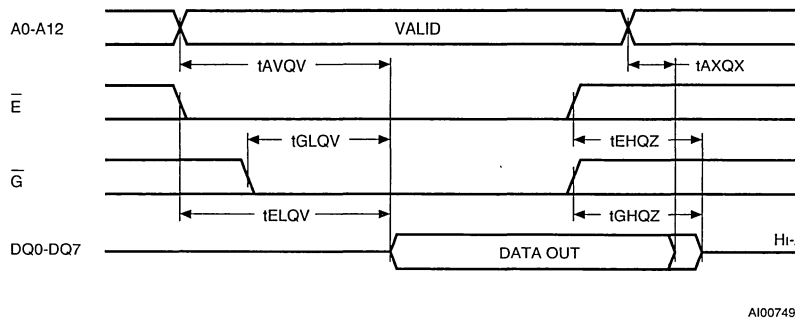
Note: 1. Sampled only, not 100% tested

Table 8. Read Mode AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C, V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	M28C64C						Unit
				-150		-200		-250		
				min	max	min	max	min	max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	G = V_{IL}		150		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		75		100		110	ns
t_{EHQZ} (1)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	50	0	60	0	65	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	50	0	60	0	65	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Note: 1. Output Hi-Z is defined as the point at which data is no longer driven.

Figure 7. Read Mode AC Waveforms



Note: Write Enable ($\overline{W}$) = High

Table 9. Write Mode AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C, V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E} = V_{IL}$	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W} = V_{IL}$	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		150		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		150		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$		1	µs
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		150		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		150		ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		10		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		10		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		200		ns
t_{WHWH}	t_{BLC}	Byte Load Repeat Cycle Time		0.35	50	µs
t_{WHRH}	t_{WC}	Write Cycle Time			5	ms
t_{WHRL}	t_{DB}	Write Enable High to Ready/Busy Low	Note 1		220	ns
t_{EHRL}	t_{DB}	Chip Enable High to Ready/Busy Low	Note 1		220	ns
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Note: 1. With a 3.3 kΩ external pull-up resistor.

Figure 8. Write Mode AC Waveforms - Write Enable Controlled

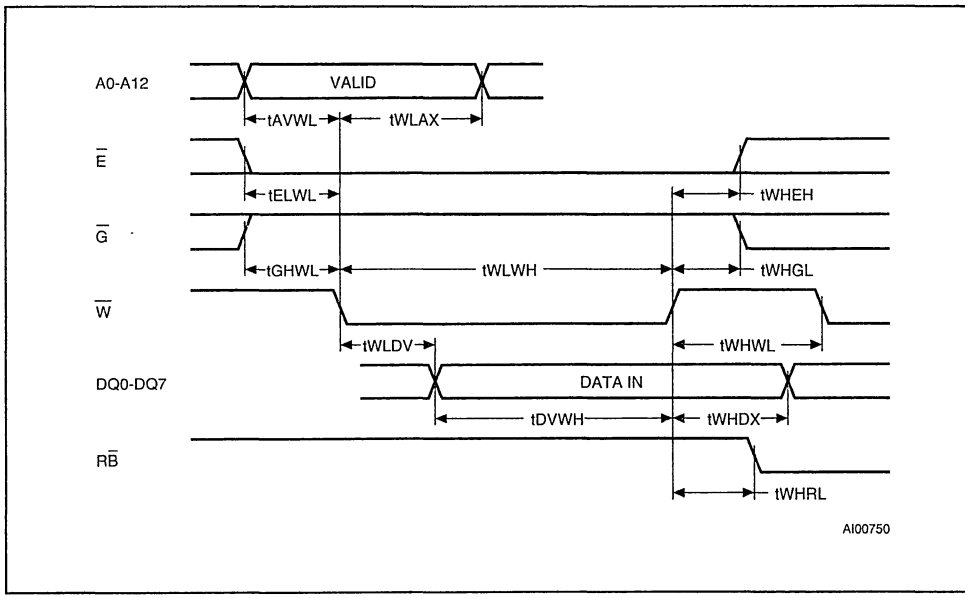


Figure 9. Write Mode AC Waveforms - Chip Enable Controlled

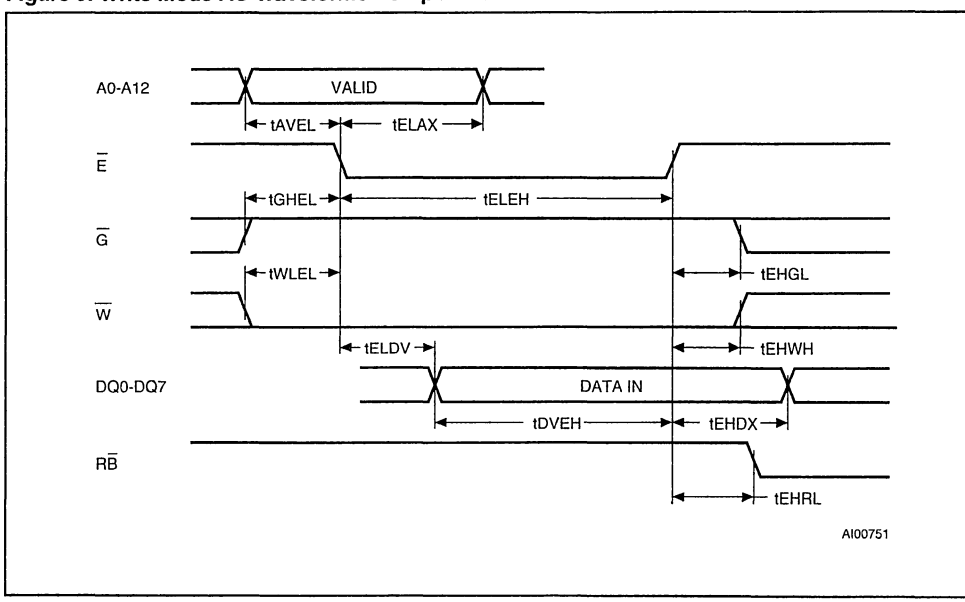


Figure 10. Page Write Mode AC Waveforms - Write Enable Controlled

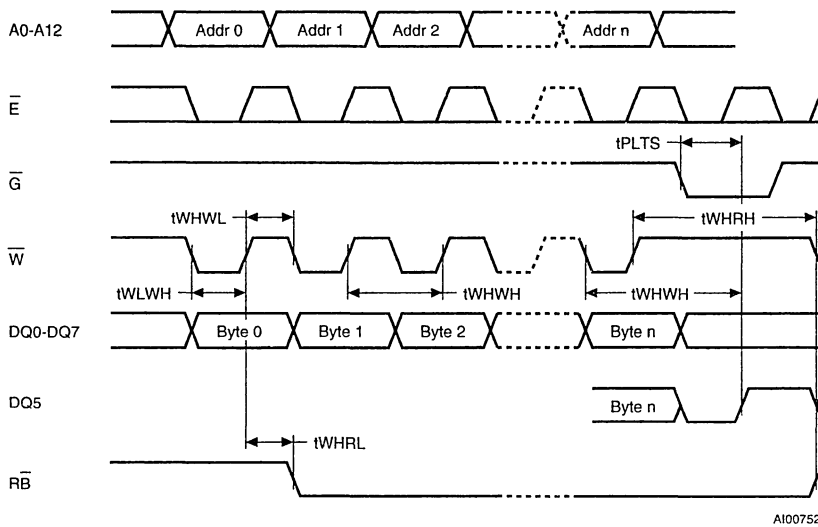


Figure 11. Data Polling Waveform Sequence

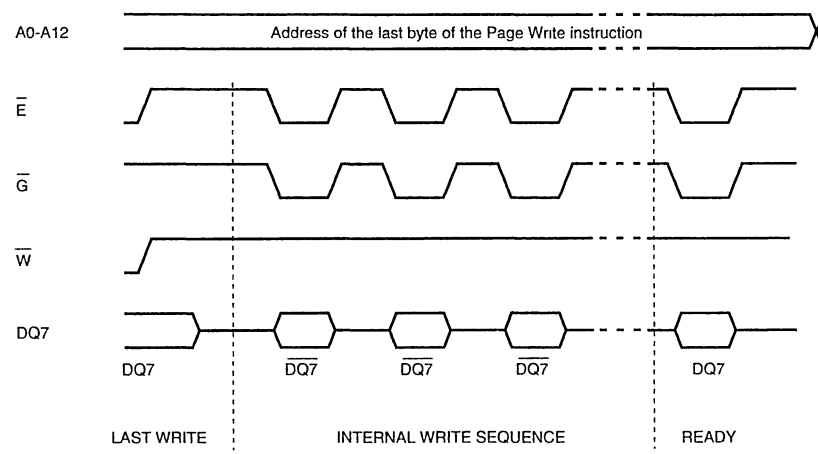
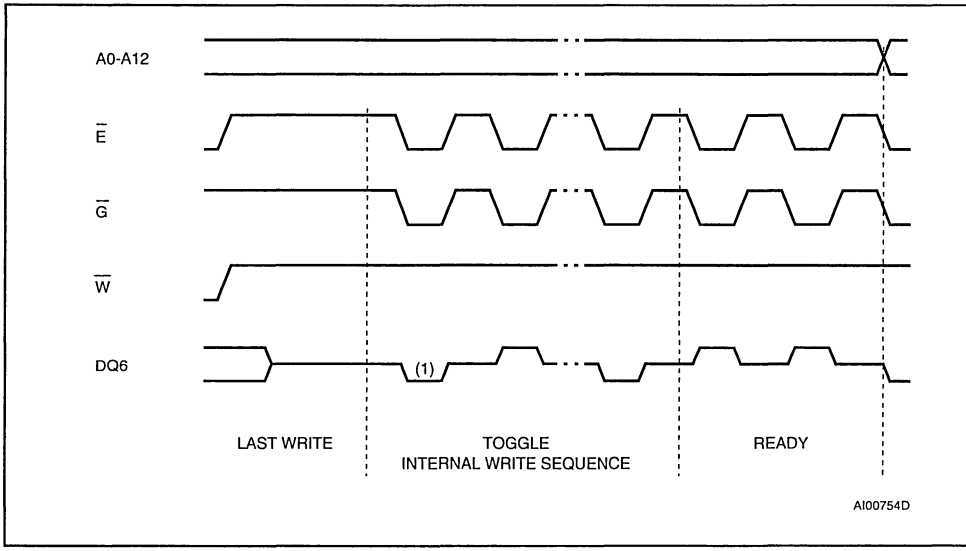


Figure 12. Toggle Bit Waveform Sequence



Note: 1. First Toggle bit is forced to '0'

ORDERING INFORMATION SCHEME

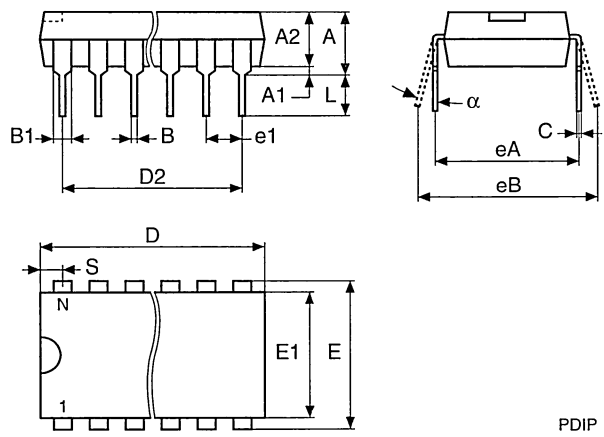
Example: M28C64C -150 K 1

Version	Speed		Package	Temperature Range
C RB available	-150	150 ns	P PDIP28	1 0 to 70 °C
X RB not bonded (pin NC)	-200	200 ns	K PLCC32	6 –40 to 85 °C
	-250	250 ns	MS SO28 300 mils	
			N TSOP28 8 x 13.4mm	

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PDIP28 - 28 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.08			0.200
A1		0.38			0.015	
A2		3.56	4.06		0.140	0.160
B		0.38	0.51		0.015	0.020
B1	1.52			0.060		
C		0.20	0.30		0.008	0.012
D		36.83	37.34		1.450	1.470
D2	33.02			1.300		
E	15.24			0.600		
E1		13.59	13.84		0.535	0.545
e1	2.54			0.100		
eA	14.99			0.590		
eB		15.24	17.78		0.600	0.700
L		3.18	3.43		0.125	0.135
S		1.78	2.08		0.070	0.082
α		0°	10°		0°	10°
N	28			28		

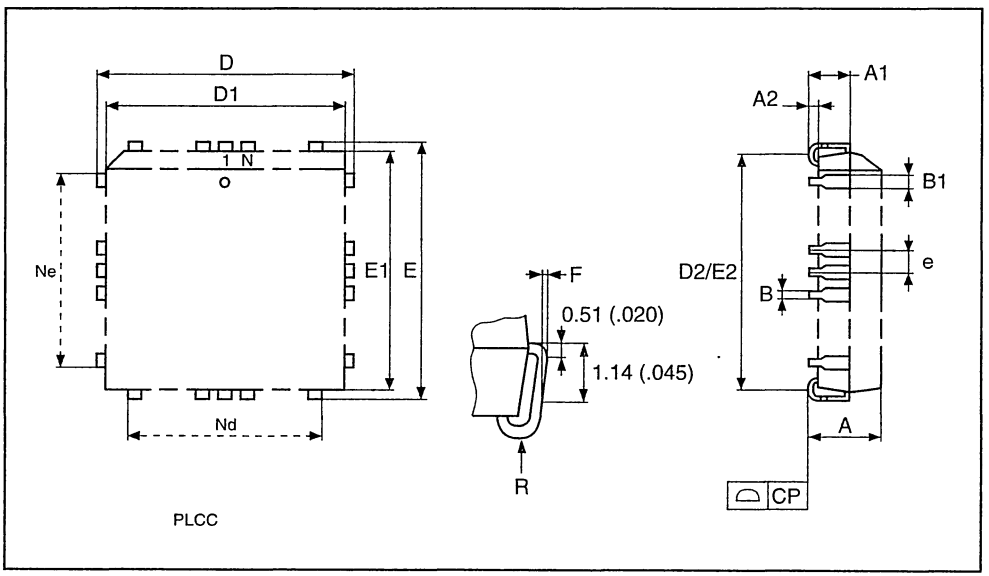


PDIP

Drawing is not to scale

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
A2		–	0.38		–	0.015
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
F		0.00	0.25		0.000	0.010
R	0.89	–	–	0.035	–	–
N		32			32	
Nd		7			7	
Ne		9			9	
CP			0.10			0.004

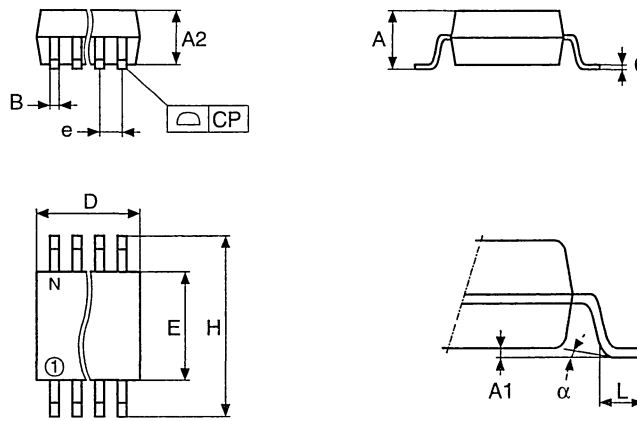


PLCC

Drawing is not to scale

SO28 - 28 lead Plastic Small Outline, 300 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.46	2.64		0.097	0.104
A1		0.13	0.29		0.005	0.011
A2		2.29	2.39		0.090	0.094
B		0.35	0.48		0.014	0.019
C		0.23	0.32		0.009	0.013
D		17.81	18.06		0.701	0.711
E		7.42	7.59		0.292	0.299
e	1.27	–	–	0.050	–	–
H		10.16	10.41		0.400	0.410
L		0.61	1.02		0.024	0.040
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

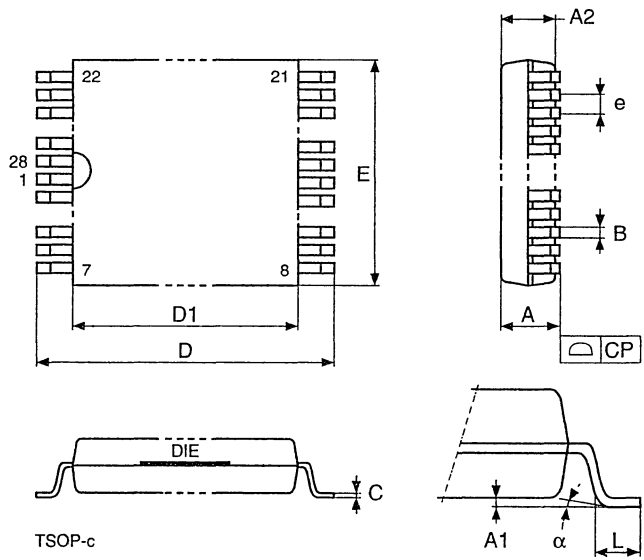


SO-b

Drawing is not to scale.

TSOP28 - 28 lead Plastic Thin Small Outline, 8 x 13.4mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.25			0.049
A1			0.20			0.008
A2		0.95	1.15		0.037	0.045
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		13.20	13.60		0.520	0.535
D1		11.70	11.90		0.461	0.469
E		7.90	8.10		0.311	0.319
e	0.55	–	–	0.022	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	28			28		
CP			0.10			0.004



TSOP-c

Drawing is not to scale.

M28C64

64 Kbit (8K x 8) Parallel EEPROM With Software Data Protection

- Fast Access Time:
  - 90 ns at V_{CC}=5 V for M28C64 and M28C64-A
  - 120 ns at V_{CC}=3 V for M28C64-xxW
- Single Supply Voltage:
  - 4.5 V to 5.5 V for M28C64 and M28C64-A
  - 2.7 V to 3.6 V for M28C64-xxW
- Low Power Consumption
- Fast BYTE and PAGE WRITE (up to 64 Bytes)
  - 1 ms at V_{CC}=4.5 V for M28C64-A
  - 3 ms at V_{CC}=4.5 V for M28C64
  - 5 ms at V_{CC}=2.7 V for M28C64-xxW
- Enhanced Write Detection and Monitoring:
  - Ready/$\overline{\text{Busy}}$ Open Drain Output
  - Data Polling
  - Toggle Bit
  - Page Load Timer Status
- JEDEC Approved Bytewide Pin-Out
- Software Data Protection
- 100000 Erase/Write Cycles (minimum)
- Data Retention (minimum):
  - 40 Years for M28C64 and M28C64-xxW
  - 10 Years for M28C64-A

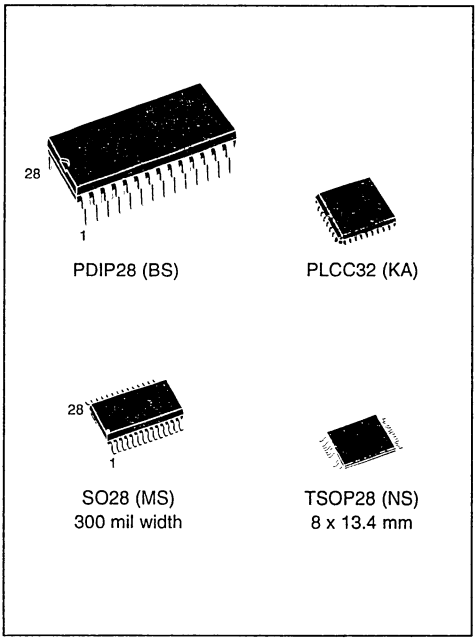


Figure 1. Logic Diagram

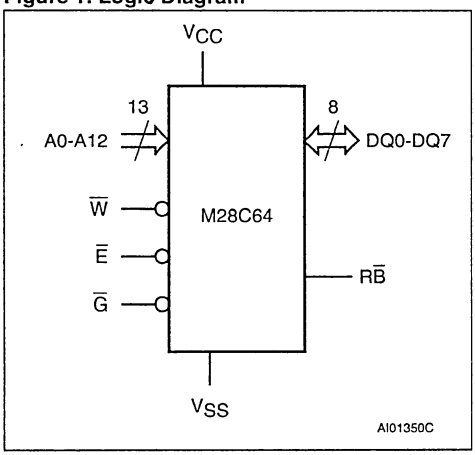
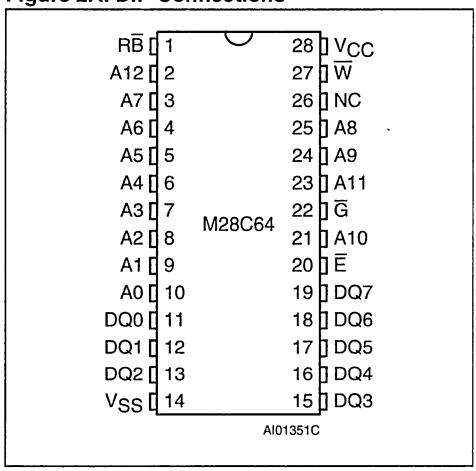


Table 1. Signal Names

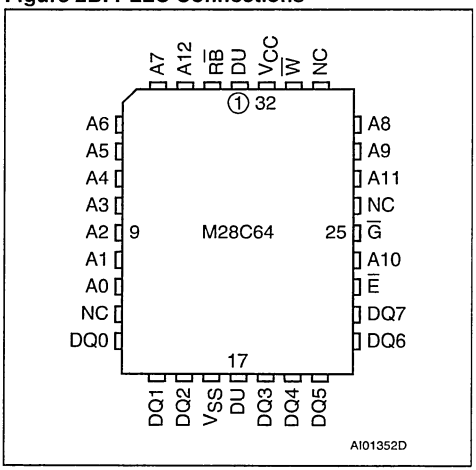
A0-A12	Address Input
DQ0-DQ7	Data Input / Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$R\overline{B}$	Ready / Busy
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Connections



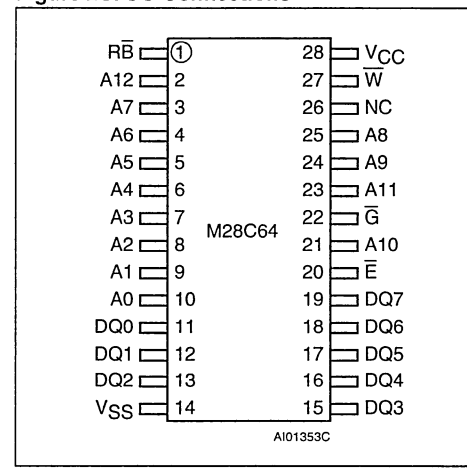
Note: 1. NC = Not Connected

Figure 2B. PLLC Connections



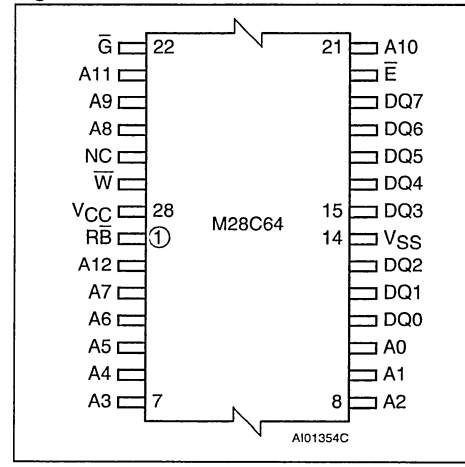
Note: 1. NC = Not Connected
2. DU = Do Not Use

Figure 2C. SO Connections



Note: 1. NC = Not Connected

Figure 2D. TSOP Connections



Note: 1. NC = Not Connected

DESCRIPTION

The M28C64 devices consist of 8192x8 bits of low power, parallel EEPROM, fabricated with STMicroelectronics' proprietary single polysilicon CMOS technology. The devices offer fast access time, with low power dissipation, and require a single voltage supply (5V or 3V, depending on the option chosen).

The device has been designed to offer a flexible microcontroller interface, featuring both hardware and software handshaking, with Ready/$\overline{\text{Busy}}$, Data Polling and Toggle Bit. The device supports a 64 byte Page Write operation. Software Data Protection (SDP) is also supported, using the standard JEDEC algorithm.

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	-40 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C
V_{CC}	Supply Voltage	-0.3 to V_{CC}+1	V
V_{IO}	Input or Output Voltage	-0.6 to V_{CC}+0.6	V
V_I	Input Voltage	-0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]	4000	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100 pF, 1500 Ω)

Figure 3. Block Diagram

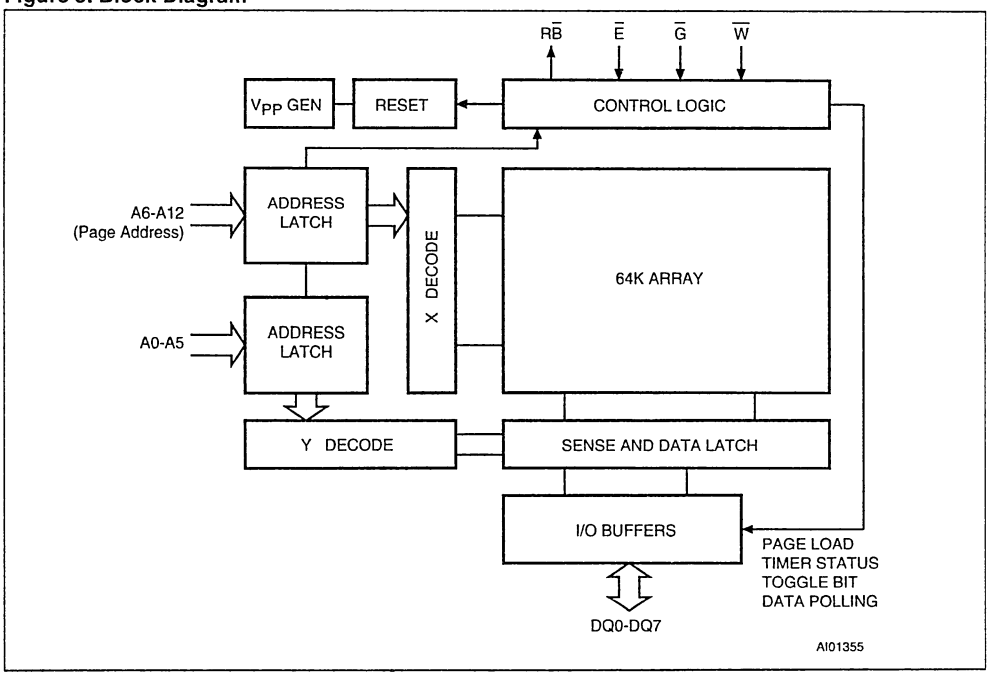


Table 3. Operating Modes [1]

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7
Stand-by	1	X	X	Hi-Z
Output Disable	X	1	X	Hi-Z
Write Disable	X	X	1	Hi-Z
Read	0	0	1	Data Out
Write	0	1	0	Data In
Chip Erase	0	V	0	Hi-Z

Note: 1. 0=V_{IL}; 1=V_{IH}; X = V_{IH} or V_{IL}; V=12V ± 5%.

SIGNAL DESCRIPTION

The external connections to the device are summarized in Table 1, and their use in Table 3.

Addresses (A0-A12). The address inputs are used to select one byte from the memory array during a read or write operation.

Data In/Out (DQ0-DQ7). The contents of the data byte are written to, or read from, the memory array through the Data I/O pins.

Chip Enable ($\overline{E}$). The chip enable input must be held low to enable read and write operations. When Chip Enable is high, power consumption is reduced.

Output Enable ($\overline{G}$). The Output Enable input controls the data output buffers, and is used to initiate read operations.

Write Enable ($\overline{W}$). The Write Enable input controls whether the addressed location is to be read, from or written to.

Ready/$\overline{Busy}$ ($\overline{RB}$). Ready/$\overline{Busy}$ is an open drain output that can be used to detect the end of the internal write cycle.

DEVICE OPERATION

In order to prevent data corruption and inadvertent write operations, an internal V_{CC} comparator inhibits the Write operations if the V_{CC} voltage is lower than V_{WI} (see Table 4A and Table 4B). Once the voltage applied on the V_{CC} pin goes over the V_{WI} threshold (V_{CC}>V_{WI}), write access to the memory is allowed after a time-out t_{PUW}, as specified in Table 4A and Table 4B.

Further protection against data corruption is offered by the $\overline{E}$ and $\overline{W}$ low pass filters: any glitch, on the $\overline{E}$ and $\overline{W}$ inputs, with a pulse width less than 10 ns (typical) is internally filtered out to prevent inadvertent write operations to the memory.

Table 4A. Power-Up Timing[1] for M28C64 (5V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 4.5 to 5.5 V)

Symbol	Parameter	Min.	Max.	Unit
t_{PUR}	Time Delay to Read Operation		1	µs
t_{PUW}	Time Delay to Write Operation (once $V_{CC} \geq V_{WI}$)		10	ms
V_{WI}	Write Inhibit Threshold	3.0	4.2	V

Note: 1. Sampled only, not 100% tested.

Table 4B. Power-Up Timing[1] for M28C64-xxW (3V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 2.7 to 3.6 V)

Symbol	Parameter	Min.	Max.	Unit
t_{PUR}	Time Delay to Read Operation		1	µs
t_{PUW}	Time Delay to Write Operation (once $V_{CC} \geq V_{WI}$)		15	ms
V_{WI}	Write Inhibit Threshold	1.5	2.5	V

Note: 1. Sampled only, not 100% tested.

Read

The device is accessed like a static RAM. When $\overline{E}$ and $\overline{G}$ are low, and $\overline{W}$ is high, the contents of the addressed location are presented on the I/O pins. Otherwise, when either $\overline{G}$ or $\overline{E}$ is high, the I/O pins revert to their high impedance state.

Write

Write operations are initiated when both $\overline{W}$ and $\overline{E}$ are low and $\overline{G}$ is high. The device supports both $\overline{W}$-controlled and $\overline{E}$-controlled write cycles (as shown in Figure 11 and Figure 12). The address is latched during the falling edge of $\overline{W}$ or $\overline{E}$ (which ever occurs later) and the data is latched on the rising edge of $\overline{W}$ or $\overline{E}$ (which ever occurs first). After a delay, t_{WLQ5H}, that cannot be shorter than the value specified in Table 10A and Table 10B, the internal write cycle starts. It continues, under internal timing control, until the write operation is complete. The commencement of this period can be detected by reading the Page Load Timer Status on DQ5. The end of the cycle can be detected by reading the status of the Data Polling and the Toggle Bit functions on DQ7 and DQ6.

Page Write

The Page Write mode allows up to 64 bytes to be written on a single page in a single go. This is achieved through a series of successive Write operations, no two of which are separated by more than the t_{WLQ5H} value (as specified in Table 10A and Table 10B).

The page write can be initiated during any byte write operation. Following the first byte write instruction the host may send another address and data with a minimum data transfer rate of: $1/t_{WLQ5H}$.

The internal write cycle can start at any instant after t_{WLQ5H}. Once initiated, the write operation is internally timed, and continues, uninterrupted, until completion.

All bytes must be located on the same page address (A12-A6 must be the same for all bytes). Otherwise, the Page Write operation is not executed.

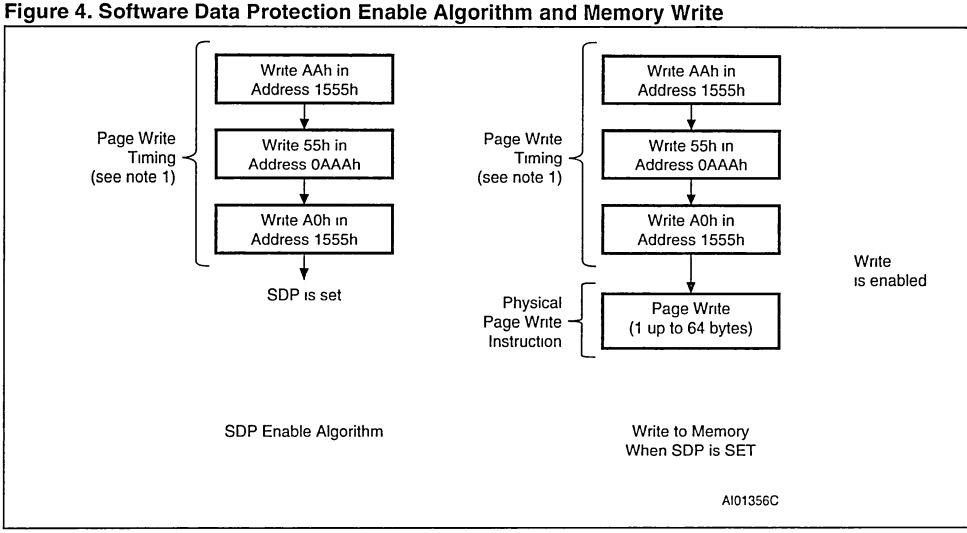
As with the single byte Write operation, described above, the DQ5, DQ6 and DQ7 lines can be used to detect the beginning and end of the internally controlled phase of the Page Write cycle.

Software Data Protection (SDP)

The device offers a software-controlled write-protection mechanism that allows the user to inhibit all write operations to the device. This can be useful for protecting the memory from inadvertent write cycles that may occur during periods of instability (uncontrolled bus conditions when excessive noise is detected, or when power supply levels are outside their specified values).

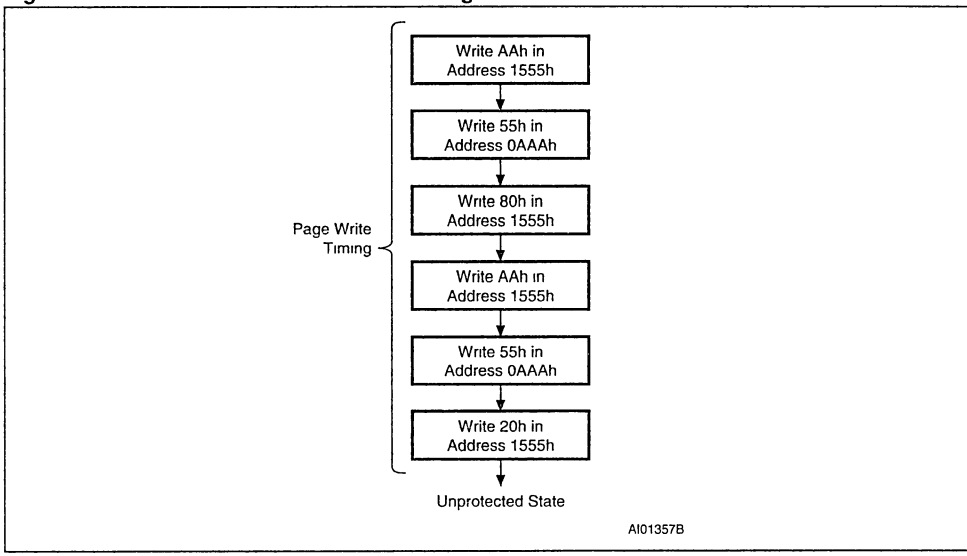
By default, the device is shipped in the "unprotected" state: the memory contents can be freely changed by the user. Once the Software Data Protection Mode is enabled, all write commands are

Figure 4. Software Data Protection Enable Algorithm and Memory Write



Note: 1. The most significant address bits (A12 to A6) differ during these specific Page Write operations.

Figure 5. Software Data Protection Disable Algorithm



ignored, and have no effect on the memory contents.

The device remains in this mode until a valid Software Data Protection disable sequence is received. The device reverts to its "unprotected" state.

The status of the Software Data Protection (enabled or disabled) is represented by a non-volatile latch, and is remembered across periods of the power being off.

The Software Data Protection Enable command consists of the writing of three specific data bytes to three specific memory locations (each location being on a different page), as shown in Figure 4.

Similarly to disable the Software Data Protection, the user has to write specific data bytes into six different locations, as shown in Figure 5. This complex series of operations protects against the chance of inadvertent enabling or disabling of the Software Data Protection mechanism.

When SDP is enabled, the memory array can still have data written to it, but the sequence is more complex (and hence better protected from inadvertent use). The sequence is as shown in Figure 4. This consists of an unlock key, to enable the write action, at the end of which the SDP continues to be enabled. This allows the SDP to be enabled, and data to be written, within a single Write cycle (t_{WC}).

Software Chip Erase

Using this function, available on the M28C64 but not on the M28C64-A or M28C64-xxW, the contents of the entire memory are erased (set to FFh) by holding Chip Enable ($\overline{E}$) low, and holding Output Enable ($\overline{G}$) at V_{CC}+7.0V. The chip is cleared when a 10 ms low pulse is applied to the Write Enable ($\overline{W}$) signal (see Figure 7 and Table 5 for details).

Status Bits

The devices provide three status bits (DQ7, DQ6 and DQ5), and one output pin ($R\overline{B}$), for use during write operations. These allow the application to use the write time latency of the device for getting on with other work. These signals are available on

Figure 6. Status Bit Assignment

DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
DP	TB	PLTS	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

DP = Data Polling
TB = Toggle Bit
PLTS = Page Load Timer Status
Hi-Z = High impedance

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Figure 7. Chip Erase AC Waveforms (M28C64 and M28C64-xxW)

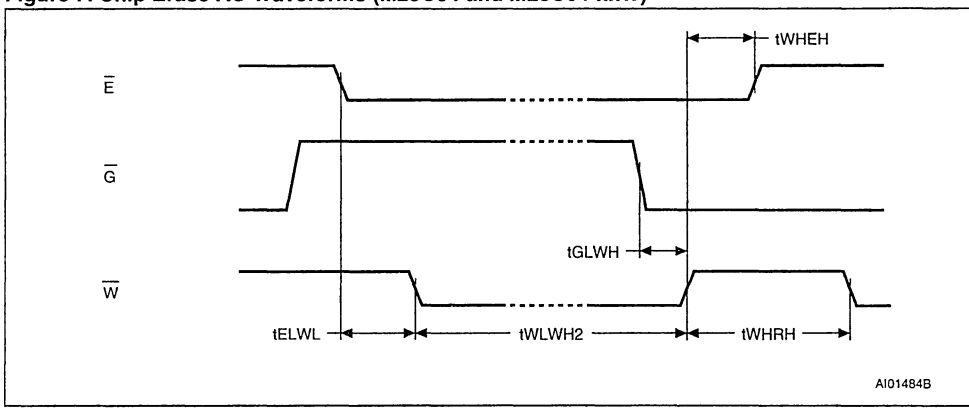


Table 5. Chip Erase AC Characteristics[1] for M28C64 and M28C64-xxW
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 4.5 to 5.5 V or 2.7 to 3.6 V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
t_{ELWL}	Chip Enable Low to Write Enable Low	$\overline{G}$ = V_{CC} + 7V	1		µs
t_{WHEH}	Write Enable High to Chip Enable High	$\overline{G}$ = V_{CC} + 7V	0		ns
t_{WLWH2}	Write Enable Low to Write Enable High	$\overline{G}$ = V_{CC} + 7V	10		ms
t_{GLWH}	Output Enable Low to Write Enable High	$\overline{G}$ = V_{CC} + 7V	1		µs
t_{WHRH}	Write Enable High to Write Enable Low	$\overline{G}$ = V_{CC} + 7V		3	ms

Note: 1. Sampled only, not 100% tested.

the I/O port bits DQ7, DQ6 and DQ5 (but only during programming cycle, once a byte or more has been latched into the memory) or continuously on the $R\overline{B}$ output pin.

Data Polling bit (DQ7). The internally timed write cycle starts after t_{WLQ5H} (defined in Table 10A and Table 10B) has elapsed since the previous byte was latched in to the memory. The value of the DQ7 bit of this last byte, is used as a signal throughout this write operation: it is inverted while the internal write operation is underway, and is inverted back to its original value once the operation is complete.

Toggle bit (DQ6). The device offers another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 toggles from '0' to '1' and '1' to '0' (the first read value being '0') on subsequent attempts to read any byte of the memory. When the internal write cycle is complete, the toggling is stopped, and the values read on DQ7-DQ0 are those of the addressed memory byte. This indicates that the device is again available for new Read and Write operations.

Page Load Timer Status bit (DQ5). An internal timer is used to measure the period between successive Write operations, up to t_{WLQ5H} (defined in Table 10A and Table 10B). The DQ5 line is held low to show when this timer is running (hence showing that the device has received one write operation, and is waiting for the next). The DQ5 line is held high when the counter has overflowed (hence showing that the device is now starting the internal write to the memory array).

Ready/$\overline{\text{Busy}}$ pin. The $R\overline{B}$ pin is an open drain output that is held low during the erase/write cycle, and that is released (allowed to float) at the completion of the programming cycle.

Table 6A. Read Mode DC Characteristics for M28C64 and M28C64-A (5V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 4.5 to 5.5 V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$0 V \le V_{IN} \le V_{CC}$		10	µA
I_{LO}	Output Leakage Current	$0 V \le V_{OUT} \le V_{CC}$		10	µA
I_{CC} [1]	Supply Current (TTL inputs)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5 MHz		30	mA
	Supply Current (CMOS inputs)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5 MHz		25	mA
I_{CC1} [1]	Supply Current (Stand-by) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2} [1]	Supply Current (Stand-by) CMOS	$\overline{E} > V_{CC} - 0.3V$		100	µA
V_{IL}	Input Low Voltage		-0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Note: 1. All inputs and outputs open circuit.

Table 6B. Read Mode DC Characteristics for M28C64-xxW (3V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 2.7 to 3.6 V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$0 V \le V_{IN} \le V_{CC}$		10	µA
I_{LO}	Output Leakage Current	$0 V \le V_{OUT} \le V_{CC}$		10	µA
I_{CC} [1]	Supply Current (CMOS inputs)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5 MHz, V_{CC} = 3.3V		8	mA
		$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5 MHz, V_{CC} = 3.6V		10	mA
I_{CC2} [1]	Supply Current (Stand-by) CMOS	$\overline{E} > V_{CC} - 0.3V$		20	µA
V_{IL}	Input Low Voltage		-0.3	0.6	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		0.2 V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	0.8 V_{CC}		V

Note: 1. All inputs and outputs open circuit.

Table 7. Input and Output Parameters[1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 8. AC Measurement Conditions

Input Rise and Fall Times	≤ 20 ns
Input Pulse Voltages (M28C64, M28C64-A)	0.4 V to 2.4 V
Input Pulse Voltages (M28C64-xxW)	0 V to V_{CC}-0.3V
Input and Output Timing Reference Voltages (M28C64, M28C64-A)	0.8 V to 2.0 V
Input and Output Timing Reference Voltages (M28C64-xxW)	0.5 V_{CC}

Figure 8. AC Testing Input Output Waveforms

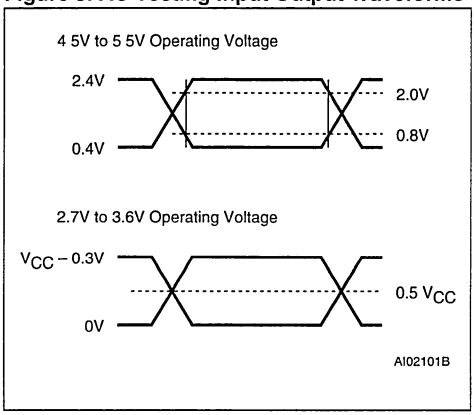


Figure 9. AC Testing Equivalent Load Circuit

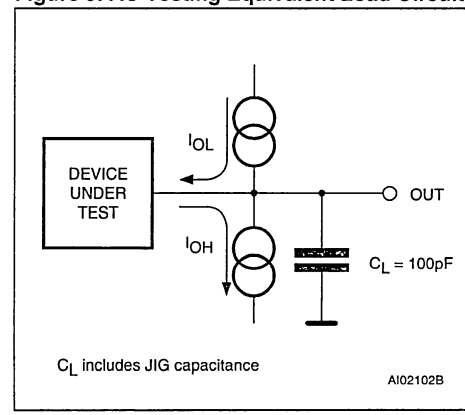


Table 9A. Read Mode AC Characteristics for M28C64 and M28C64-A (5V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 4.5 to 5.5 V)

Symbol	Alt.	Parameter	Test Condition	M28C64						Unit
				-90		-12		-15		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		90		120		150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		90		120		150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		40		45		50	ns
t_{EHQZ}[1]	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	40	0	45	0	50	ns
t_{GHQZ}[1]	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	40	0	45	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

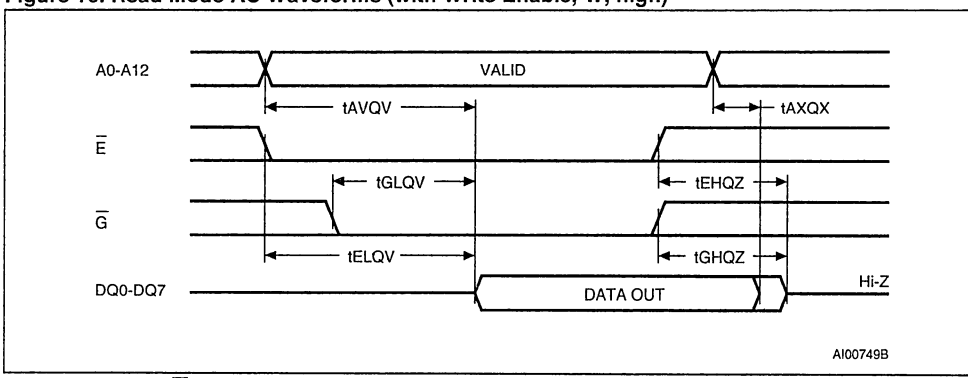
Note: 1. Output Hi-Z is defined as the point at which data is no longer driven.

Table 9B. Read Mode AC Characteristics for M28C64-xxW (3V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 2.7 to 3.6 V)

Symbol	Alt.	Parameter	Test Condition	M28C64-xxW										Unit
				-12		-15		-20		-25		-30		
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}=V_{IL}$, $\overline{G}=V_{IL}$		120		150		200		250		300	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}=V_{IL}$		120		150		200		250		300	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}=V_{IL}$		80		80		100		150		150	ns
t_{EHQZ}[1]	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}=V_{IL}$	0	45	0	50	0	55	0	60	0	60	ns
t_{GHQZ}[1]	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}=V_{IL}$	0	45	0	50	0	55	0	60	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}=V_{IL}$, $\overline{G}=V_{IL}$	0		0		0		0		0		ns

Note: 1. Output Hi-Z is defined as the point at which data is no longer driven.

Figure 10. Read Mode AC Waveforms (with Write Enable, $\overline{W}$, high)



Note: 1. Write Enable ($\overline{W}$) = V_{IH}

Table 10A. Write Mode AC Characteristics for M28C64 and M28C64-A (5V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 4.5 to 5.5 V)

Symbol	Alt.	Parameter	Test Condition	M28C64		Unit
				Min	Max	
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E}$ = V_{IL}	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W}$ = V_{IL}	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		50		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		50		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}		1	µs
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		50		ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		50	1000	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		50		ns
t_{WLQ5H}	t_{BLC}	Time-out after last byte write (M28C64)		100		µs
		Time-out after last byte write (M28C64-A)		20		µs
t_{Q5HQ5X}	t_{WC}	Write Cycle Time (M28C64)			3	ms
		Write Cycle Time (M28C64-A)			1	ms
t_{WHRL}	t_{DB}	Write Enable High to Ready/Busy Low	Note 1		150	ns
t_{EHRL}	t_{DB}	Chip Enable High to Ready/Busy Low	Note 1		150	ns
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Note: 1. With a 3.3 kΩ pull-up resistor.

Table 10B. Write Mode AC Characteristics for M28C64-xxW (3V range)
(T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 2.7 to 3.6 V)

Symbol	Alt.	Parameter	Test Condition	M28C64-xxW		Unit
				Min	Max	
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E}$ = V_{IL}	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W}$ = V_{IL}	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		100		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		100		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}		1	µs
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		100	1000	ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		50	1000	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		100		ns
t_{WLQ5H}	t_{BLC}	Time-out after the last byte write		100		µs
t_{Q5HQ5X}	t_{WC}	Write Cycle Time			5	ms
t_{WHRL}	t_{DB}	Write Enable High to Ready/Busy Low	Note 1		150	ns
t_{EHRL}	t_{DB}	Chip Enable High to Ready/Busy Low	Note 1		150	ns
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Note: 1. With a 3 3 kΩ pull-up resistor.

Figure 11. Write Mode AC Waveforms (Write Enable, $\overline{W}$, controlled)

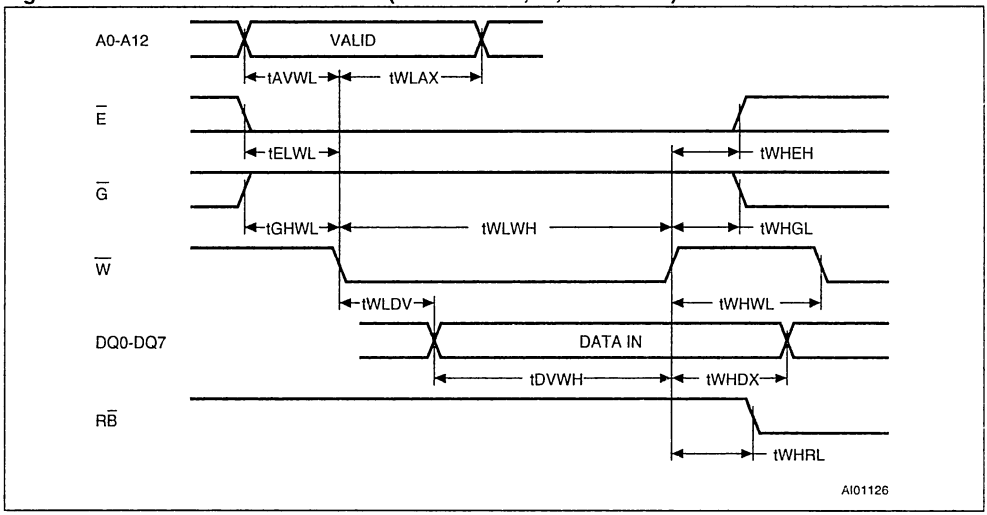


Figure 12. Write Mode AC Waveforms (Chip Enable, $\overline{E}$, controlled)

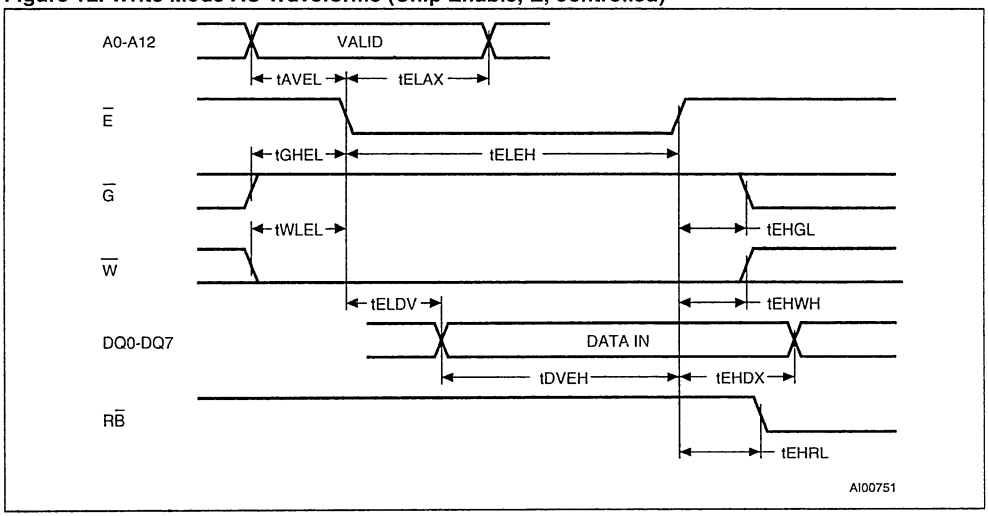


Figure 13. Page Write Mode AC Waveforms (Write Enable, $\overline{W}$, controlled)

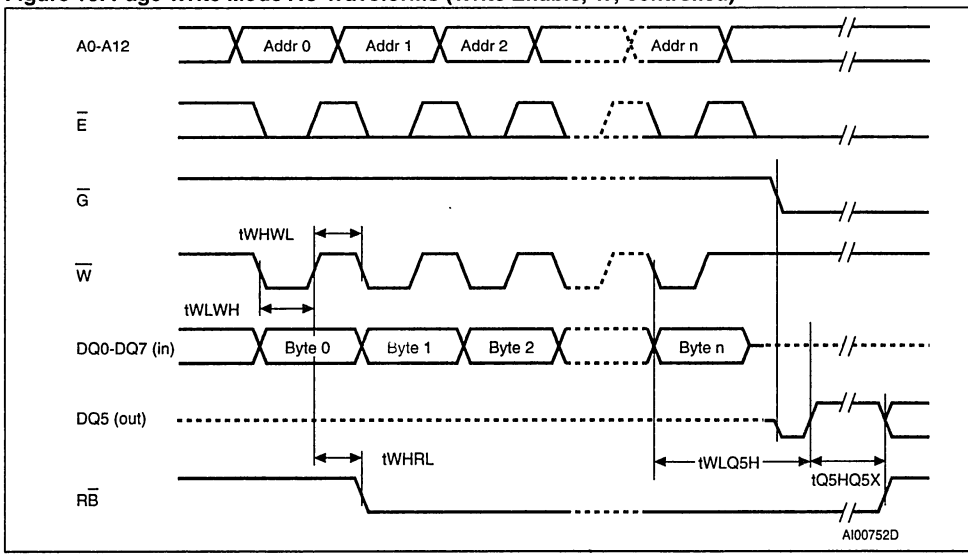
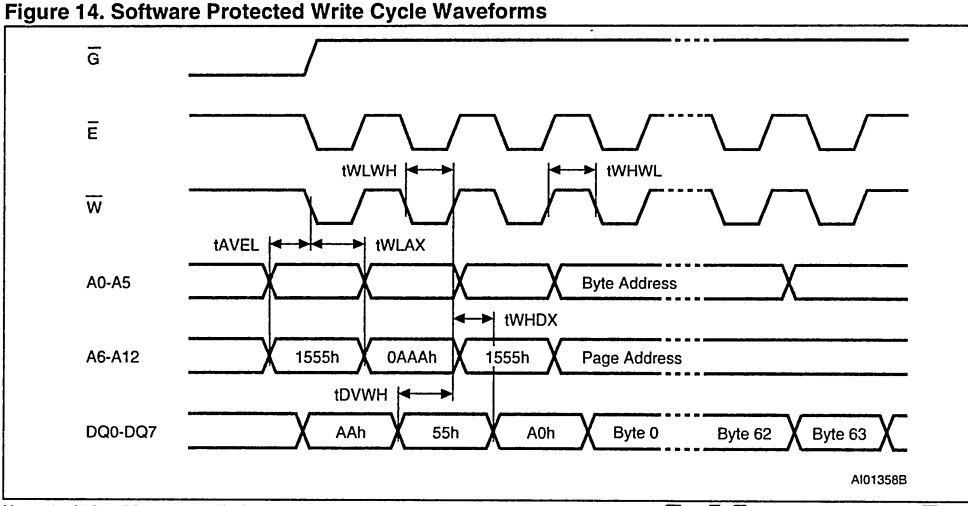


Figure 14. Software Protected Write Cycle Waveforms



Note: 1. A12 to A6 must specify the same page address during each high-to-low transition of $\overline{W}$ (or $\overline{E}$). $\overline{G}$ must be high only when $\overline{W}$ and $\overline{E}$ are both low.

Figure 15. Data Polling Sequence Waveforms

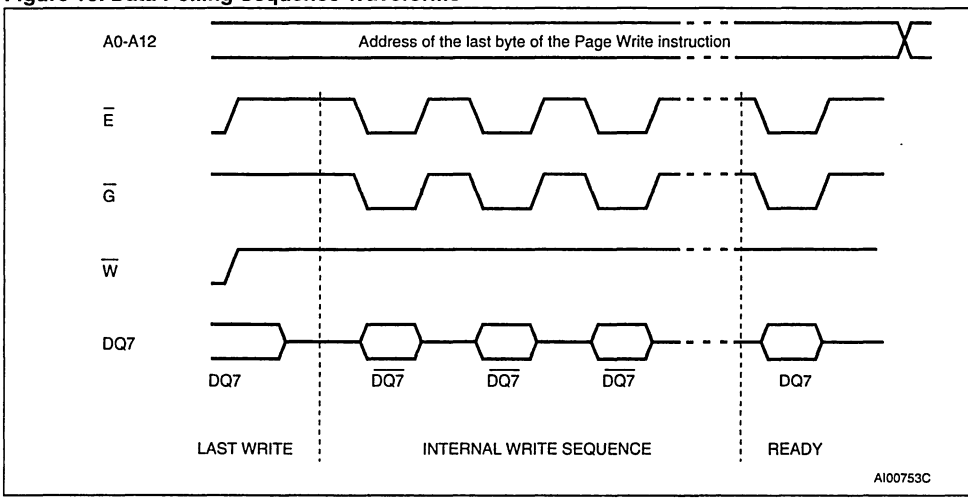
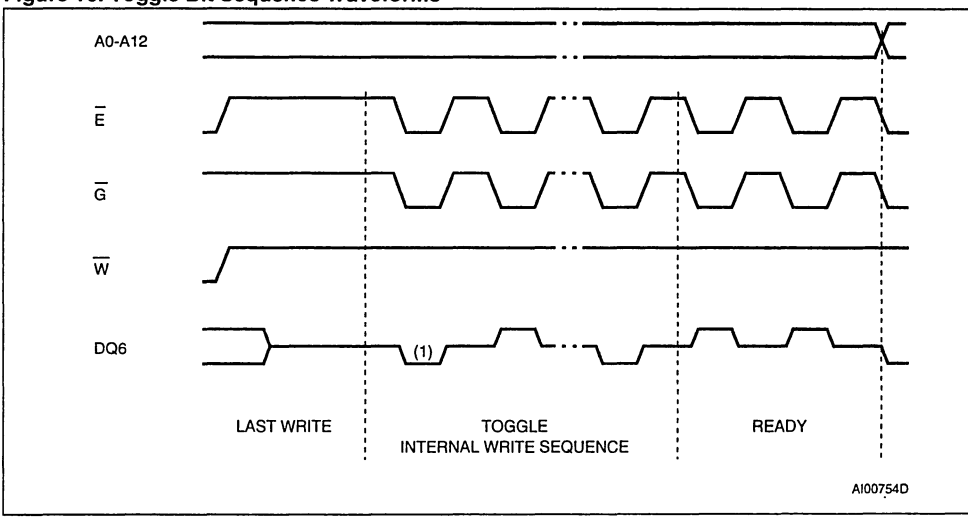


Figure 16. Toggle Bit Sequence Waveforms



Note: 1. The Toggle Bit is first set to '0'.

Table 11. Ordering Information Scheme

Example: M28C64 – A 12 BS 6 T

Write Time

blank	t_{WC} = 3 ms at 4.5V to 5.5V; t_{WC} = 5 ms at 2.7V to 3.6V
A[1]	t_{WC} = 1 ms at 4.5V to 5.5V

Speed

90[2]	90 ns
12	120 ns
15	150 ns
20[3]	200 ns
25[3]	250 ns
30[3]	300 ns

Operating Voltage

blank	4.5 V to 5.5 V
W[4]	2.7 V to 3.6 V

Option

T	Tape and Reel Packing

Temperature Range

1	0 °C to 70 °C
6	–40 °C to 85 °C

Package

BS	PDIP28
KA	PLCC32
MS	SO28 (300 mil width)
NS	TSOP28 (8 x 13.4 mm)

Note: 1. Available only with 120 ns speed (-12), 5V operating range (-blank), and -40 to 85 °C temperature range (-6).
2. Available for the M28C64 only.
3. Available for the 3V range (-xxW) only.
4. Not available for the 1 ms write time option (-A).

ORDERING INFORMATION

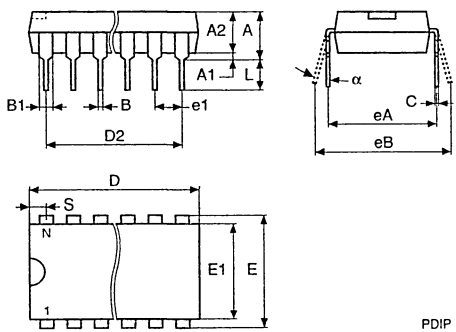
Devices are shipped from the factory with the memory content set at all '1's (FFh).

The notation used for the device number is as shown in Table 11. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 12. PDIP28 - 28 pin Plastic DIP, 600 mils width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		3.94	5.08		0.155	0.200
A1		0.38	1.78		0.015	0.070
A2		3.56	4.06		0.140	0.160
B		0.38	0.56		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.30		0.008	0.012
D		34.70	37.34		1.366	1.470
E		14.80	16.26		0.583	0.640
E1		12.50	13.97		0.492	0.550
e1	2.54	–	–	0.100	–	–
eA		15.20	17.78		0.598	0.700
L		3.05	3.82		0.120	0.150
S		1.02	2.29		0.040	0.090
α		0°	15°		0°	15°
N	28			28		

Figure 17. PDIP28 (BS)

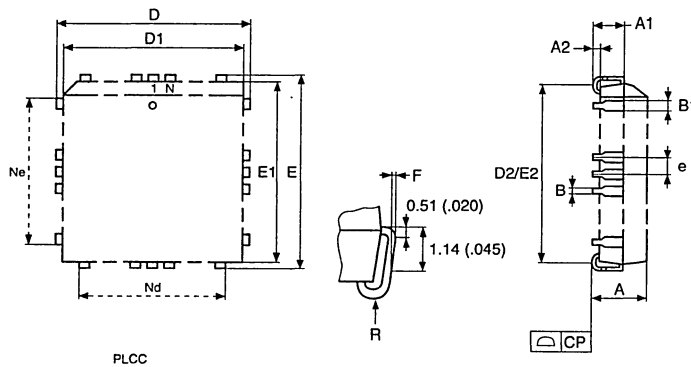


Note: 1. Drawing is not to scale

Table 13. PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
A2		–	0.38		–	0.015
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
F		0.00	0.25		0.000	0.010
R	0.89	–	–	0.035	–	–
N		32			32	
Nd		7			7	
Ne		9			9	
CP			0.10			0.004

Figure 18. PLCC (KA)

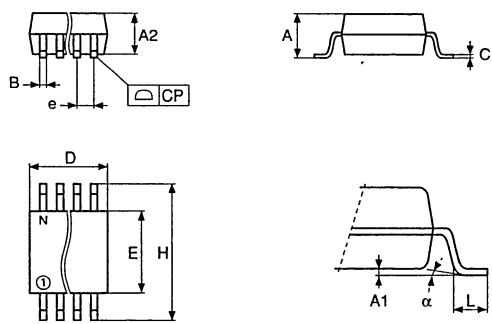


Note: 1. Drawing is not to scale.

Table 14. SO28 - 28 lead Plastic Small Outline, 300 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		2.46	2.64		0.097	0.104
A1		0.13	0.29		0.005	0.011
A2		2.29	2.39		0.090	0.094
B		0.35	0.48		0.014	0.019
C		0.23	0.32		0.009	0.013
D		17.81	18.06		0.701	0.711
E		7.42	7.59		0.292	0.299
e	1.27	–	–	0.050	–	–
H		10.16	10.41		0.400	0.410
L		0.61	1.02		0.024	0.040
α		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

Figure 19. SO28 wide (MS)



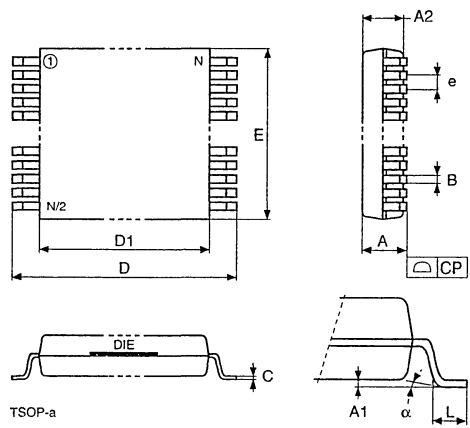
SO-b

Note: 1. Drawing is not to scale.

Table 15. TSOP28 - 28 lead Plastic Thin Small Outline, 8 x 13.4 mm

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.25			0.049
A1			0.20			0.008
A2		0.95	1.15		0.037	0.045
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		13.20	13.60		0.520	0.535
D1		11.70	11.90		0.461	0.469
E		7.90	8.10		0.311	0.319
e	0.55	–	–	0.022	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		28			28	
CP			0.10			0.004

Figure 20. TSOP32 (NS)



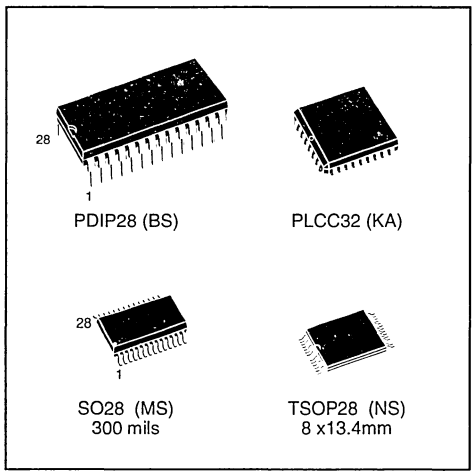
Note: 1. Drawing is not to scale.

M28256

256 Kbit (32Kb x8) Parallel EEPROM with Software Data Protection

PRELIMINARY DATA

- FAST ACCESS TIME:
  - 90ns at 5V
  - 120ns at 3V
- SINGLE SUPPLY VOLTAGE:
  - 5V ± 10% for M28256
  - 2.7V to 3.6V for M28256-xxW
- LOW POWER CONSUMPTION
- FAST WRITE CYCLE:
  - 64 Bytes Page Write Operation
  - Byte or Page Write Cycle
- ENHANCED END of WRITE DETECTION:
  - Data Polling
  - Toggle Bit
- STATUS REGISTER
- HIGH RELIABILITY DOUBLE POLYSILICON, CMOS TECHNOLOGY:
  - Endurance >100,000 Erase/Write Cycles
  - Data Retention >10 Years
- JEDEC APPROVED BYTEWIDE PIN OUT
- ADDRESS and DATA LATCHED ON-CHIP
- SOFTWARE DATA PROTECTION



DESCRIPTION

The M28256 and M28256-W are 32K x8 low power Parallel EEPROM fabricated with STMicroelectronics proprietary double polysilicon CMOS technology.

Table 1. Signal Names

A0-A14	Address Input
DQ0-DQ7	Data Input / Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

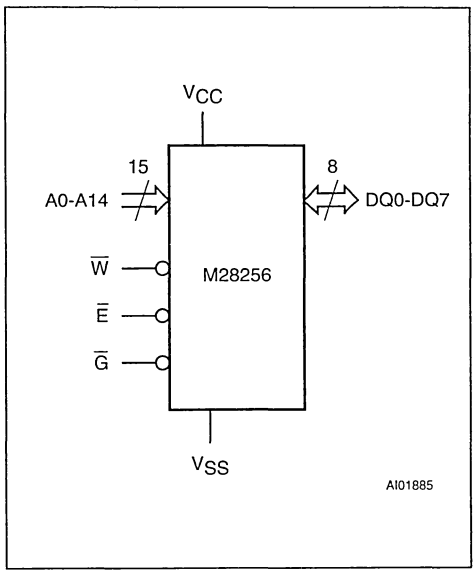


Figure 2A. DIP Pin Connections

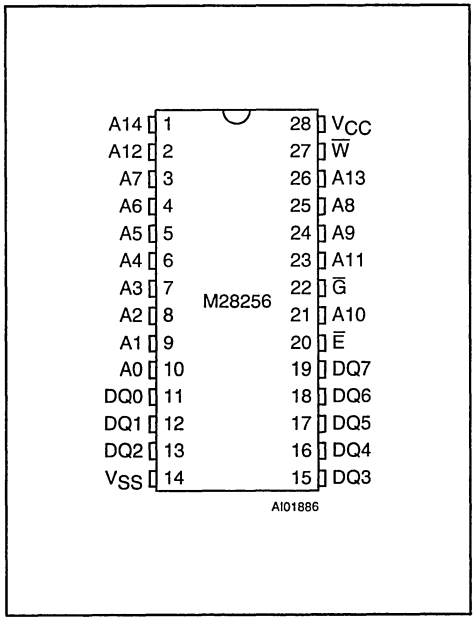
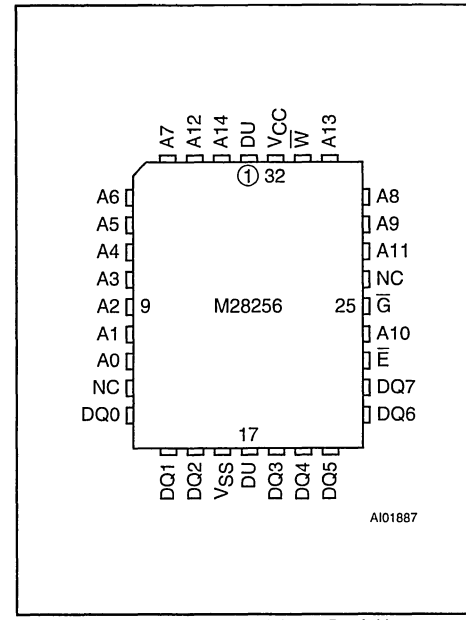


Figure 2B. LCC Pin Connections



Warning: NC = Not Connected, DU = Don't Use.

Figure 2C. SO Pin Connections

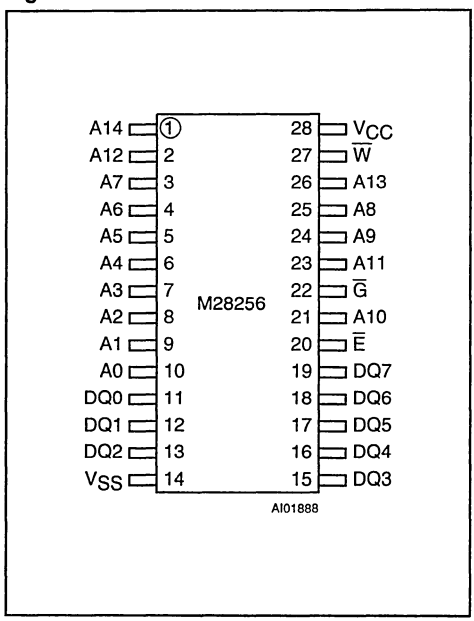


Figure 2D. TSOP Pin Connections

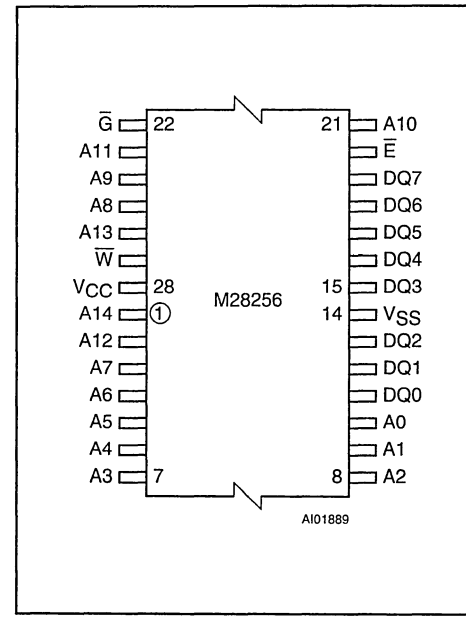


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (2)	– 40 to 85	°C
T_{STG}	Storage Temperature Range	– 65 to 150	°C
V_{CC}	Supply Voltage	– 0.3 to 6.5	V
V_{IO}	Input/Output Voltage	– 0.3 to V_{CC} +0.6	V
V_I	Input Voltage	– 0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (3)	4000	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Depends on range.
3. 100pF through 1500Ω; MIL-STD-883C, 3015.7

Figure 3. Block Diagram

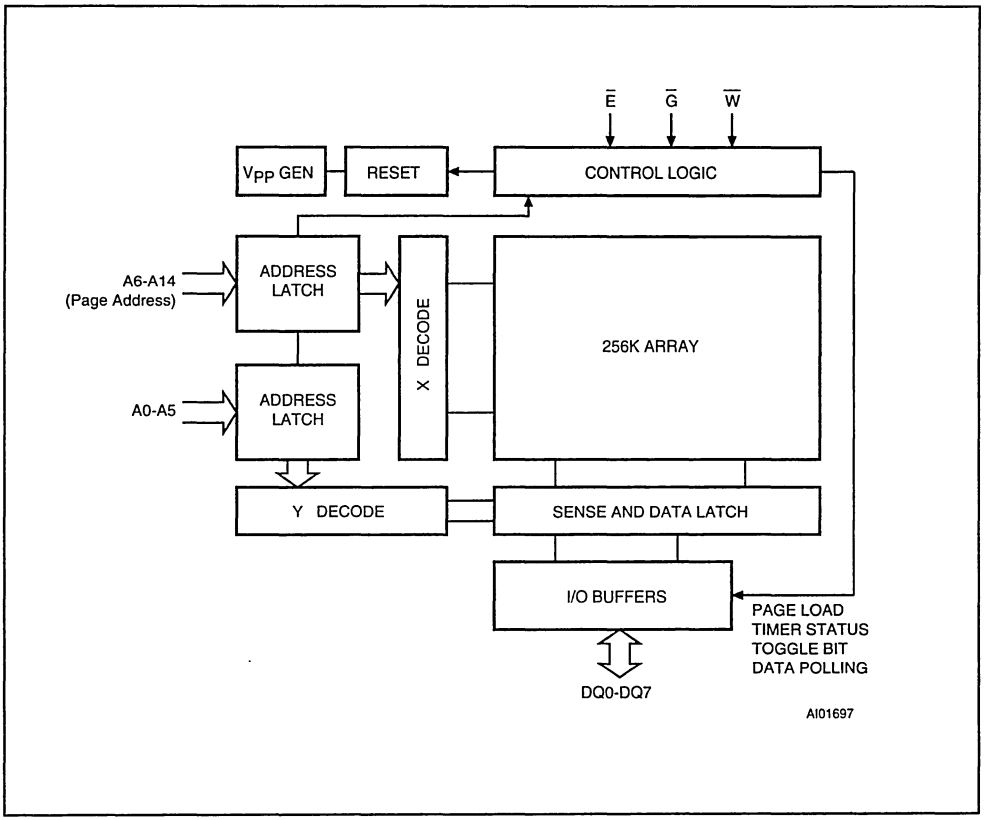


Table 3. Operating Modes (1)

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	Data In
Standby / Write Inhibit	V_{IH}	X	X	Hi-Z
Write Inhibit	X	X	V_{IH}	Data Out or Hi-Z
Write Inhibit	X	V_{IL}	X	Data Out or Hi-Z
Output Disable	X	V_{IH}	X	Hi-Z

Notes: 1. X = V_{IH} or V_{IL}

DESCRIPTION (Cont'd)

The devices offer fast access time with low power dissipation and requires a 5V or 3V power supply.

The circuit has been designed to offer a flexible microcontroller interface featuring both hardware and software handshaking with Data Polling and Toggle Bit and access to a status register. The devices support a 64 byte page write operation. A Software Data Protection (SDP) is also possible using the standard JEDEC algorithm.

PIN DESCRIPTION

Addresses (A0-A14). The address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{E}$). The chip enable input must be low to enable all read/write operations. When Chip Enable is high, power consumption is reduced.

Output Enable ($\overline{G}$). The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/ Out (DQ0- DQ7). Data is written to or read from the memory through the I/O pins.

Write Enable ($\overline{W}$). The Write Enable input controls the writing of data to the memory.

OPERATIONS

Write Protection

In order to prevent data corruption and inadvertent write operations; an internal V_{CC} comparator inhibits Write operations if V_{CC} is below VWI (see Table 7 and Table 9). Access to the memory in write mode is allowed after a power-up as specified in Table 7 and Table 9.

Read

The device is accessed like a static RAM. When $\overline{E}$ and $\overline{G}$ are low with $\overline{W}$ high, the data addressed is presented on the I/O pins. The I/O pins are high impedance when either $\overline{G}$ or $\overline{E}$ is high.

Write

Write operations are initiated when both $\overline{W}$ and $\overline{E}$ are low and $\overline{G}$ is high.The device supports both $\overline{E}$ and $\overline{W}$ controlled write cycles. The Address is latched by the falling edge of $\overline{E}$ or $\overline{W}$ which ever occurs last and the Data on the rising edge of $\overline{E}$ or $\overline{W}$ which ever occurs first. Once initiated the write operation is internally timed until completion and the status of the Data Polling and the Toggle Bit functions on DQ7 and DQ6 is controlled accordingly.

Page Write

Page write allows up to 64 bytes within the same page to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A14-A6 must be the same for all bytes; if not, the Page Write instruction is not executed. The page write can be initiated by any byte write operation.

A page write is composed of successive Write instructions which have to be sequenced with a specific period of time between two consecutive Write instructions, period of time which has to be smaller than the t_{WHWH} value (see Table 12 and Table 13).

If this period of time exceeds the t_{WHWH} value, the internal programming cycle will start. Once initiated the write operation is internally timed until completion and the status of the Data Polling and the Toggle Bit functions on DQ7 and DQ6 is controlled accordingly.

Status Register

The devices provide several Write operation status flags that can be used to minimize the application write time. These signals are available on the I/O port bits during programming cycle only.

Data Polling bit (DQ7). During the internal write cycle, any attempt to read the last byte written will produce on DQ7 the complementary value of the previously latched bit. Once the write cycle is finished the true logic value appears on DQ7 in the read cycle.

Toggle bit (DQ6). The devices offer another way for determining when the internal write cycle is completed. During the internal Erase/Write cycle, DQ6 will toggle from "0" to "1" and "1" to "0" (the first read value is "0") on subsequent attempts to read any byte of the memory. When the internal cycle is completed the toggling will stop and the data read on DQ7-DQ0 is the addressed memory byte. The device is now accessible for a new Read or Write operation.

Page Load Timer Status bit (DQ5). During a Page Write instruction, the devices expect to receive the stream of data with a minimum period of time between each data byte. This period of time (t_{WHWH}) is defined by the on-chip Page Load timer which running/overflow status is available on DQ5. DQ5 Low indicates that the timer is running, DQ5 High indicates the time-out after which the internal write cycle will start.

Figure 4. Status Bit Assignment

DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
DP	TB	PLTS	X	X	X	X	X

DP = Data Polling
TB = Toggle Bit
PLTS = Page Load Timer Status

Software Data Protection

The devices offer a software controlled write protection facility that allows the user to inhibit all write modes to the device. This can be useful in protecting the memory from inadvertent write cycles that may occur due to uncontrolled bus conditions.

The devices are shipped as standard in the "unprotected" state meaning that the memory contents can be changed as required by the user. After the Software Data Protection enable algorithm is issued, the device enters the "Protect Mode" of operation where no further write commands have any effect on the memory contents.

The devices remain in this mode until a valid Software Data Protection (SDP) disable sequence is received whereby the device reverts to its "unprotected" state. The Software Data Protection is fully non-volatile and is not changed by power on/off sequences. To enable the Software Data Protection (SDP) the device requires the user to write (with a Page Write addressing three specific data bytes to three specific memory locations, each location in a different page) as per Figure 6. Similarly to disable the Software Data Protection the user has to write specific data bytes into six different locations as per Figure 5 (with a Page Write adressing different bytes in different pages).

This complex series ensures that the user will never enable or disable the Software Data Protection accidentally.

To write into the devices when SDP is set, the sequence shown in Figure 6 must be used. This sequence provides an unlock key to enable the write action, and at the same time SDP continues to be set.

An extension to this is where SDP is required to be set, and data is to be written.

Using the same sequence as above, the data can be written and SDP is set at the same time, giving both these actions in the same Write cycle (t_{WC}).

Figure 5. Software Data Protection Enable Algorithm and Memory Write

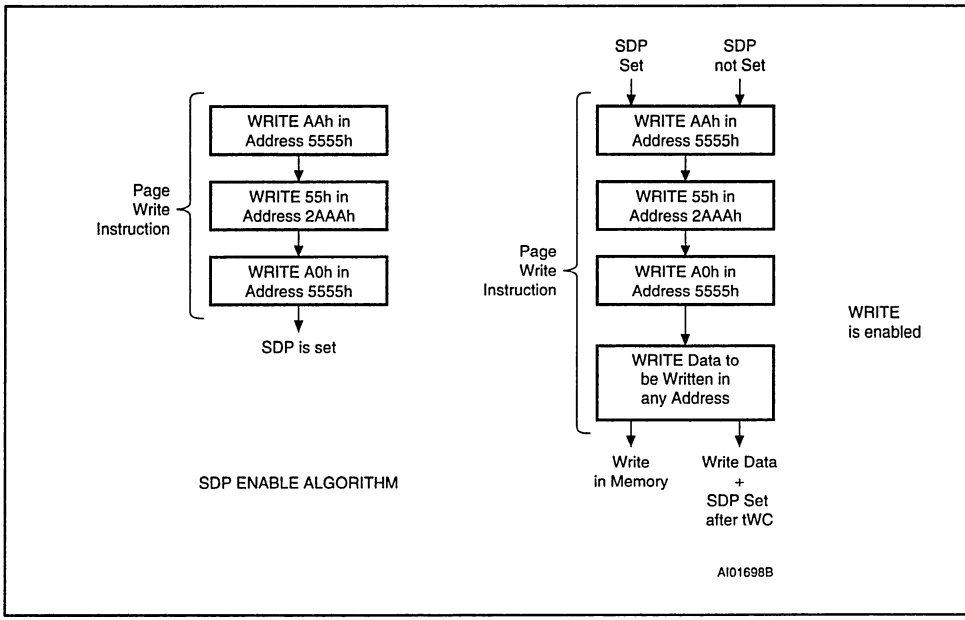


Figure 6. Software Data Protection Disable Algorithm

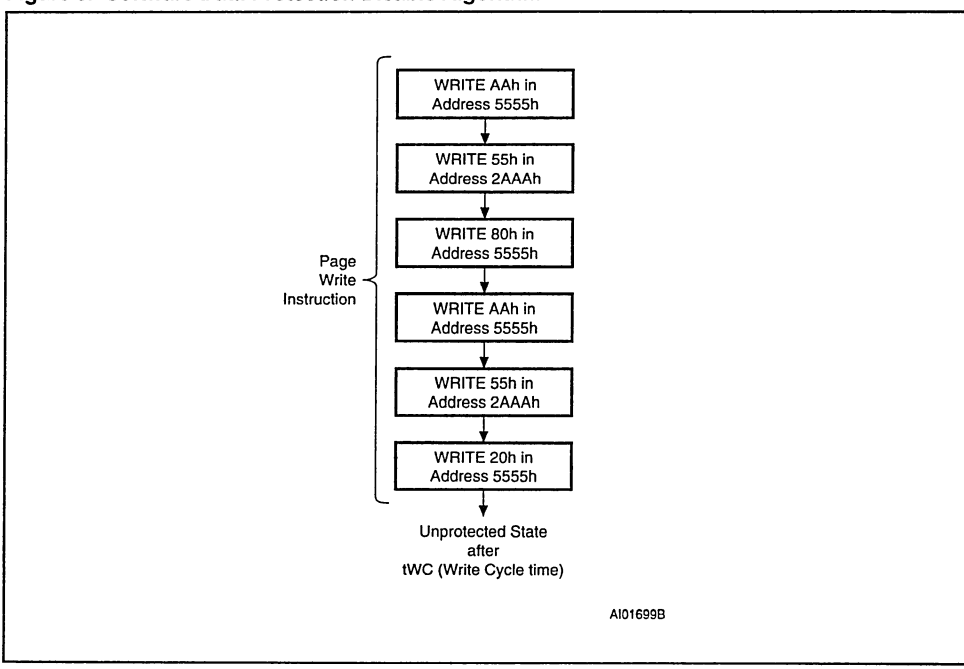


Table 4. AC Measurement Conditions

Input Rise and Fall Times	≤ 20ns
Input Pulse Voltages (M28256)	0.4V to 2.4V
Input Pulse Voltages (M28256-W)	0V to V_{CC} –0.3V
Input and Output Timing Ref. Voltages (M28256)	0.8V to 2.0V
Input and Output Timing Ref. Voltages (M28256-W)	0.5 V_{CC}

Figure 7. AC Testing Input Output Waveforms

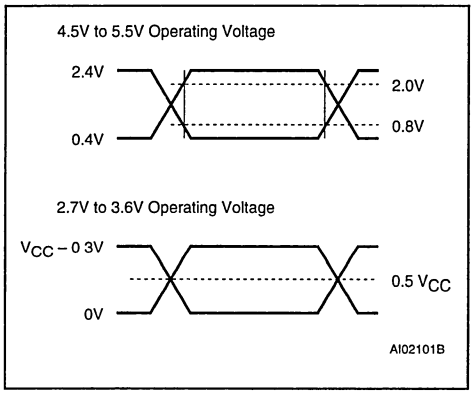


Figure 8. AC Testing Equivalent Load Circuit

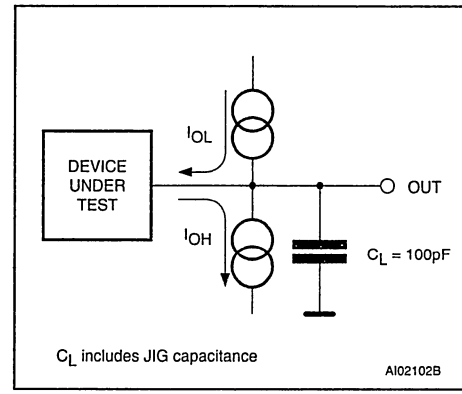


Table 5. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 6. Read Mode DC Characteristics for M28256
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{LO}	Output Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		10	µA
I_{CC} (1)	Supply Current (TTL inputs)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL} , f = 5 MHz		30	mA
	Supply Current (CMOS inputs)	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL} , f = 5 MHz		25	mA
I_{CC1} (1)	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2} (1)	Supply Current (Standby) CMOS	$\overline{E}$ > V_{CC} –0.3V		100	µA
V_{IL}	Input Low Voltage		– 0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –400 µA	2.4		

Note: 1. All I/O's open circuit.

Table 7. Power Up Timing for M28256 (1)
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Min	Max	Unit
t_{PUR}	Time Delay to Read Operation		1	µs
t_{PUW}	Time Delay to Write Operation (once $V_{CC} \geq V_{WI}$)		5	ms
V_{WI}	Write Inhibit Threshold	3.0	4.2	V

Note: 1. Sampled only, not 100% tested.

Table 8. Read Mode DC Characteristics for M28256-W
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		10	µA
I_{LO}	Output Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		10	µA
I_{CC} (1)	Supply Current (CMOS inputs)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5 MHz, V_{CC} = 3.3V		15	mA
		$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5 MHz, V_{CC} = 3.6V		15	mA
I_{CC2} (1)	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.3V$		20	µA
V_{IL}	Input Low Voltage		– 0.3	0.6	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.2 V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = –400 µA	0.8 V_{CC}		V

Note: 1. All I/O's open circuit

Table 9. Power Up Timing for M28256-W (1)
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Min	Max	Unit
t_{PUR}	Time Delay to Read Operation		1	µs
t_{PUW}	Time Delay to Write Operation (once $V_{CC} \geq V_{WI}$)		10	ms
V_{WI}	Write Inhibit Threshold	1.5	2.5	V

Note: 1. Sampled only, not 100% tested

Table 10. Read Mode AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	M28256								Unit
				-90		-12		-15		-20		
				min	max	min	max	min	max	min	max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		90		120		150		200	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	G = V_{IL}		90		120		150		200	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		40		45		50		50	ns
t_{EHQZ} (1)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	40	0	45	0	50	0	50	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	40	0	45	0	50	0	50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		0		ns

Note: 1. Output Hi-Z is defined as the point at which data is no longer driven.

Table 11. Read Mode AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7V to 3.6V)

Symbol	Alt	Parameter	Test Condition	M28256-W								Unit
				-12		-15		-20		-25		
				min	max	min	max	min	max	min	max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120		150		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	G = V_{IL}		120		150		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		45		70		80		100	ns
t_{EHQZ} (1)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	45	0	50	0	55	0	60	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	45	0	50	0	55	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		0		ns

Note: 1 Output Hi-Z is defined as the point at which data is no longer driven.

Table 12. Write Mode AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V)

Symbol	Alt	Parameter	Test Condition	M28256		Unit
				Min	Max	
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E}$ = V_{IL}	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W}$ = V_{IL}	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		50		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		50		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}		1	µs
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		50		ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		100		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		50		ns
t_{WHWH}	t_{BLC}	Byte Load Repeat Cycle Time		0.15	150	µs
t_{WHRH}	t_{WC}	Write Cycle Time			5	ms
t_{EL}, t_{WL}		$\overline{E}$ or $\overline{W}$ Input Filter Pulse Width	Note 1	10		ns
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

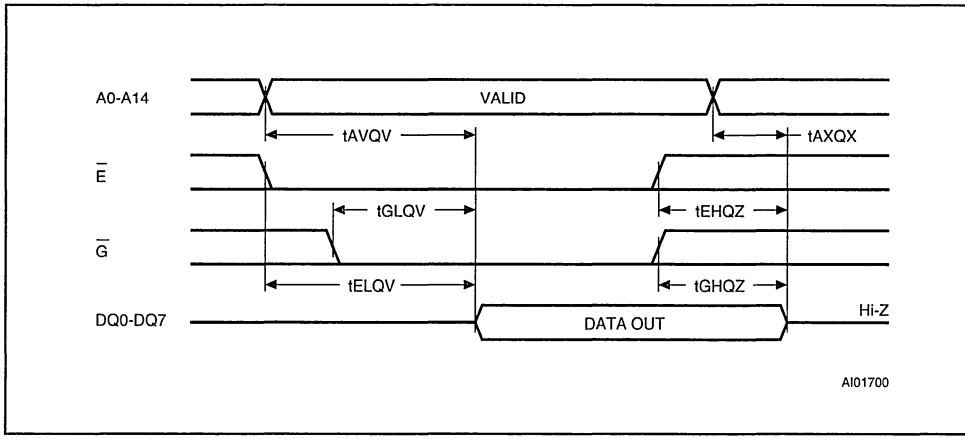
Note: 1. Characterized only but not tested in production.

Table 13. Write Mode AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7V to 3.6V)

Symbol	Alt	Parameter	Test Condition	M28256-W		Unit
				Min	Max	
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E}$ = V_{IL}	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W}$ = V_{IL}	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		70		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		70		ns
t_{WLDV}	t_{DV}	Write Enable Low to Input Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}		1	µs
t_{ELDV}	t_{DV}	Chip Enable Low to Input Valid	$\overline{G}$ = V_{IH}, $\overline{W}$ = V_{IL}		1	µs
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		100		ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		100		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		100		ns
t_{WHWH}	t_{BLC}	Byte Load Repeat Cycle Time		0.2	150	µs
t_{WHRH}	t_{WC}	Write Cycle Time			5	ms
t_{EL}, t_{WL}		$\overline{E}$ or $\overline{W}$ Input Filter Pulse Width	Note 1	10		ns
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Note: 1. Characterized only but not tested in production

Figure 9. Read Mode AC Waveforms



Note: Write Enable ($\overline{W}$) = High.

Figure 10. Write Mode AC Waveforms - Write Enable Controlled

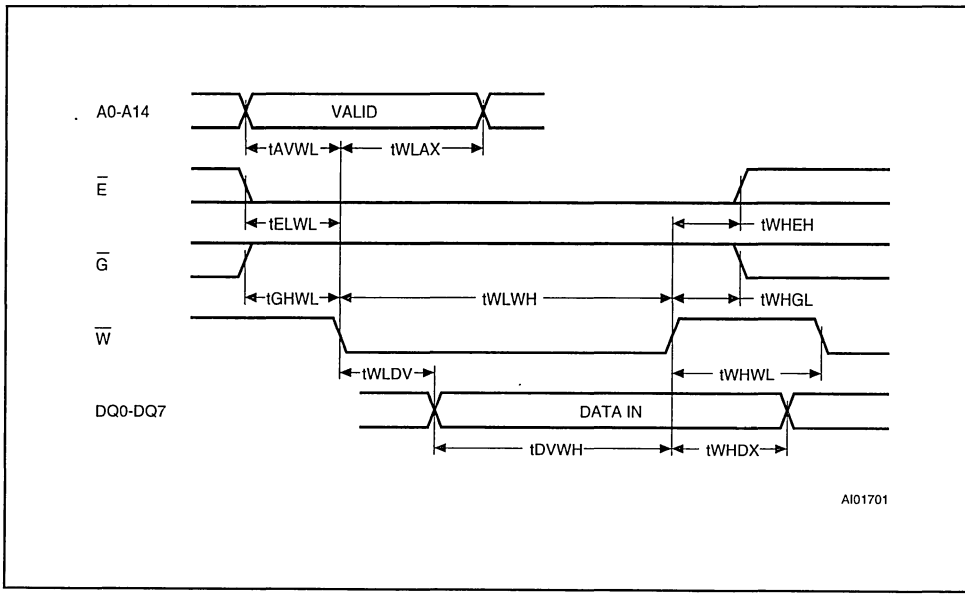


Figure 11. Write Mode AC Waveforms - Chip Enable Controlled

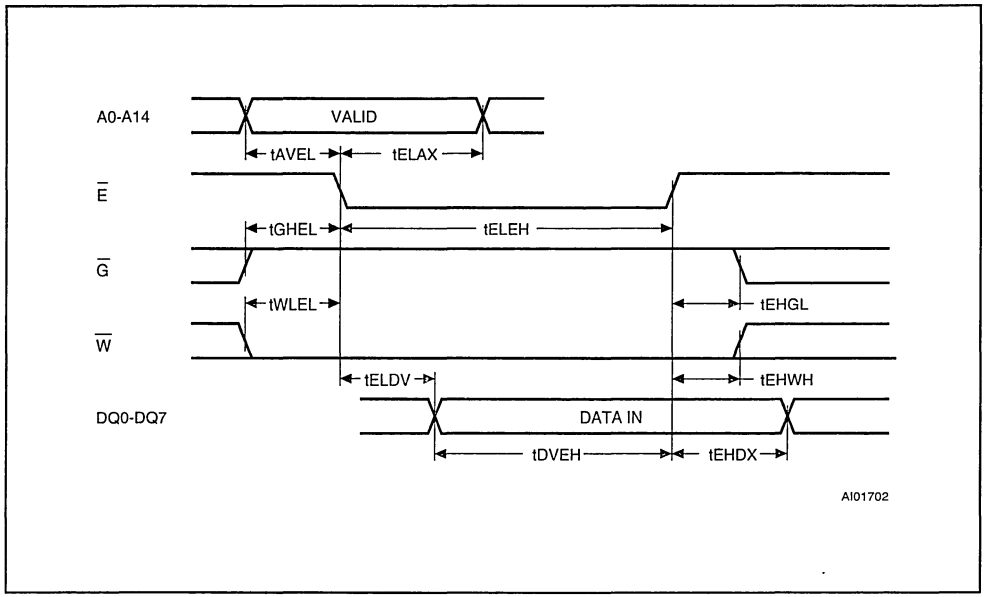


Figure 12. Page Write Mode AC Waveforms - Write Enable Controlled

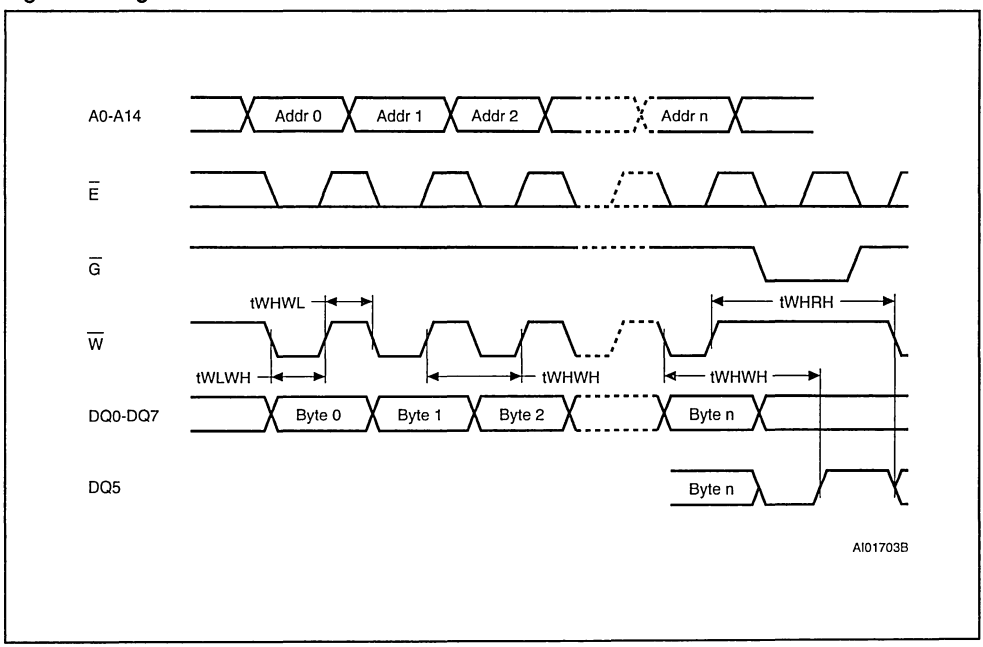
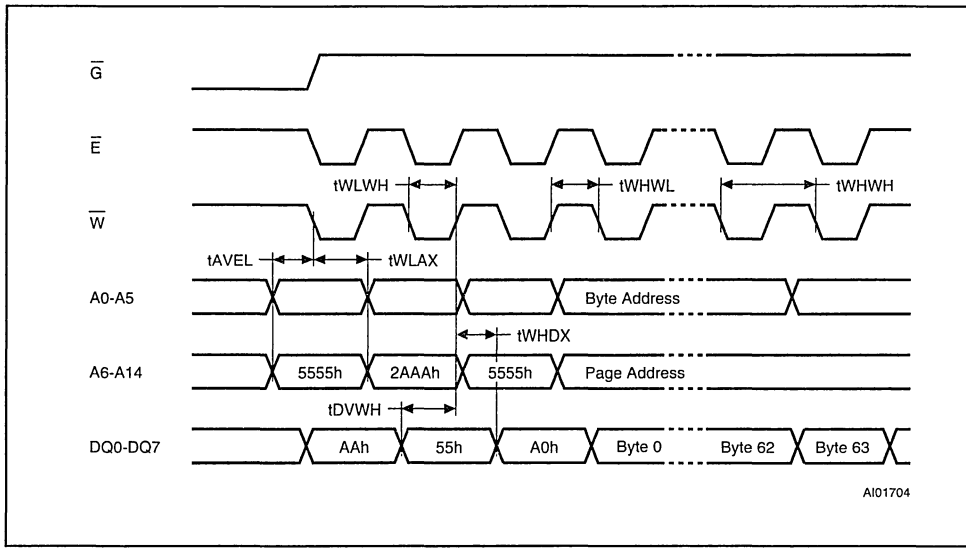


Figure 13. Software Protected Write Cycle Waveforms



Note: A6 through A14 must specify the same page address during each high to low transition of $\overline{W}$ (or $\overline{E}$) after the software code has been entered. $\overline{G}$ must be high only when $\overline{W}$ and $\overline{E}$ are both low.

Figure 14. Data Polling Waveform Sequence

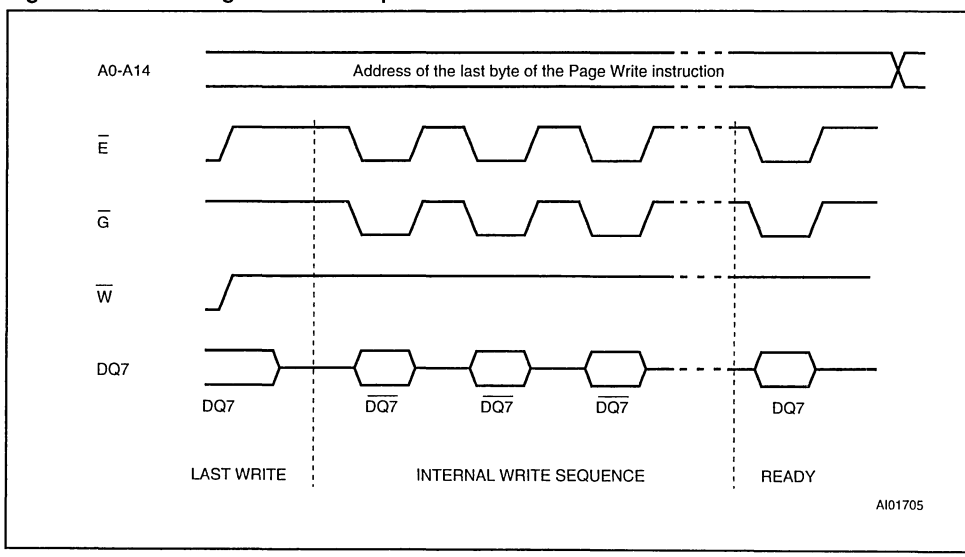
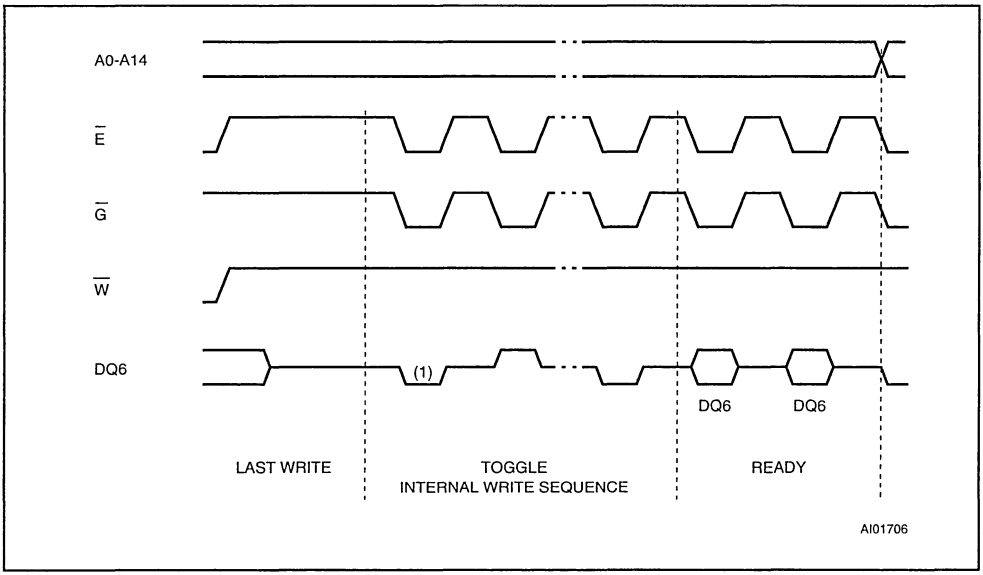


Figure 15. Toggle Bit Waveform Sequence



Note: 1. First Toggle bit is forced to '0'.

ORDERING INFORMATION SCHEME

Example: M28256 – 15 W KA 6 T

Speed		Operating Voltage		Package		Temperature Range		Option	
90 (1)	90ns	blank	4.5V to 5.5V	BS	PDIP28	1 (3)	0 to 70 °C	T	Tape & Reel Packing
12	120ns	W	2.7V to 3.6V	KA	PLCC32	6	–40 to 85 °C		
15	150ns			MS	SO28 300 mils				
20	200ns			NS	TSOP28 8 x 13.4mm				
25 (2)	250ns								

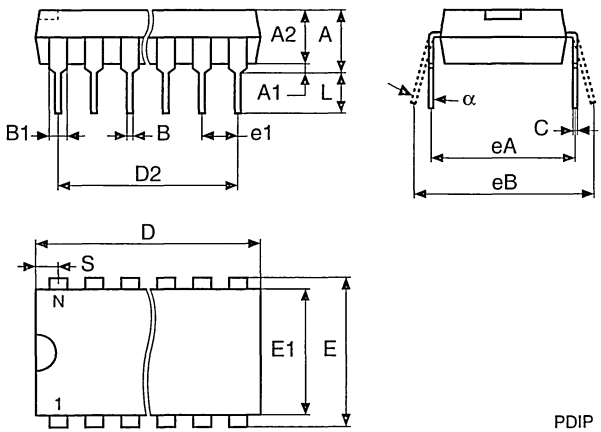
Notes: 1 Not available for "W" operating voltage.
2. Available for "W" operating voltage only
3 Temperature Range on request only

Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PDIP28 - 28 pin Plastic DIP, 600 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		–	5.08		–	0.200
A1		0.38	–		0.015	–
A2		3.56	4.06		0.140	0.160
B		0.38	0.51		0.015	0.020
B1	1.52	–	–	0.060	–	–
C		0.20	0.30		0.008	0.012
D		36.83	37.34		1.450	1.470
D2	33.02	–	–	1.300	–	–
E	15.24	–	–	0.600	–	–
E1		13.59	13.84		0.535	0.545
e1	2.54	–	–	0.100	–	–
eA	14.99	–	–	0.590	–	–
eB		15.24	17.78		0.600	0.700
L		3.18	3.43		0.125	0.135
S		1.78	2.08		0.070	0.082
α		0°	10°		0°	10°
N	28			28		

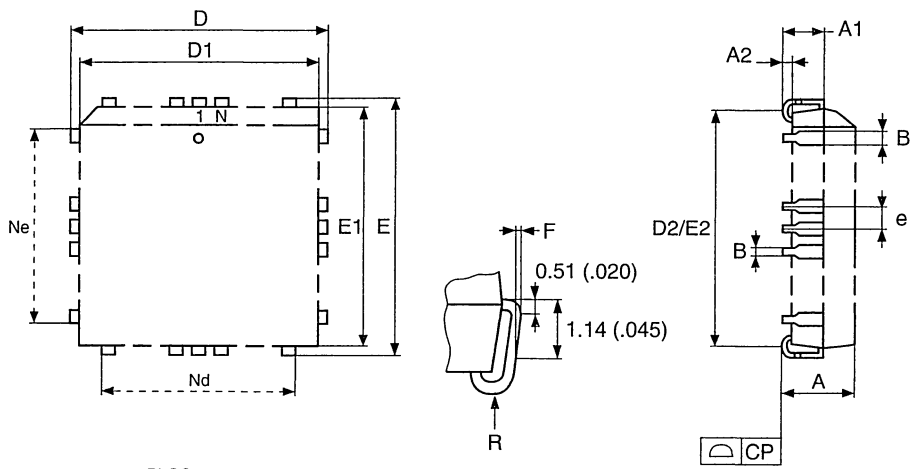


PDIP

Drawing is not to scale.

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
A2		–	0.38		–	0.015
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	-	–	0.050	–	–
F		0.00	0.25		0.000	0.010
R	0.89	–	–	0.035	–	–
N	32			32		
Nd	7			7		
Ne	9			9		

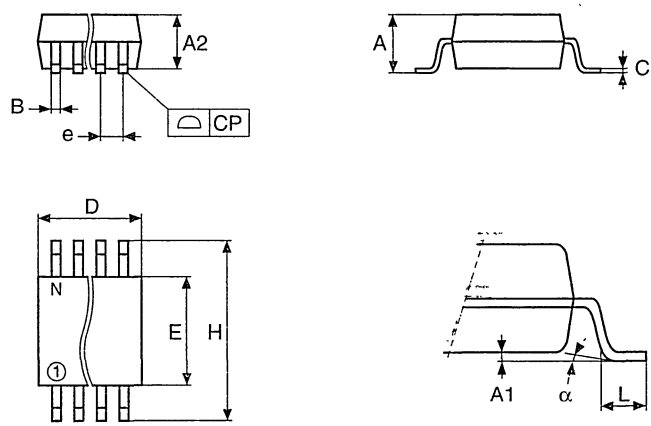


PLCC

Drawing is not to scale

SO28 - 28 lead Plastic Small Outline, 300 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.46	2.64		0.097	0.104
A1		0.13	0.29		0.005	0.011
B		0.35	0.48		0.014	0.019
C		0.23	0.32		0.009	0.013
D		17.81	18.06		0.701	0.711
E		7.42	7.59		0.292	0.299
e	1.27	–	–	0.050	–	–
H		10.16	10.41		0.400	0.410
L		0.61	1.02		0.024	0.040
α		0°	8°		0°	8°
N		28			28	
CP			0.10			0.004

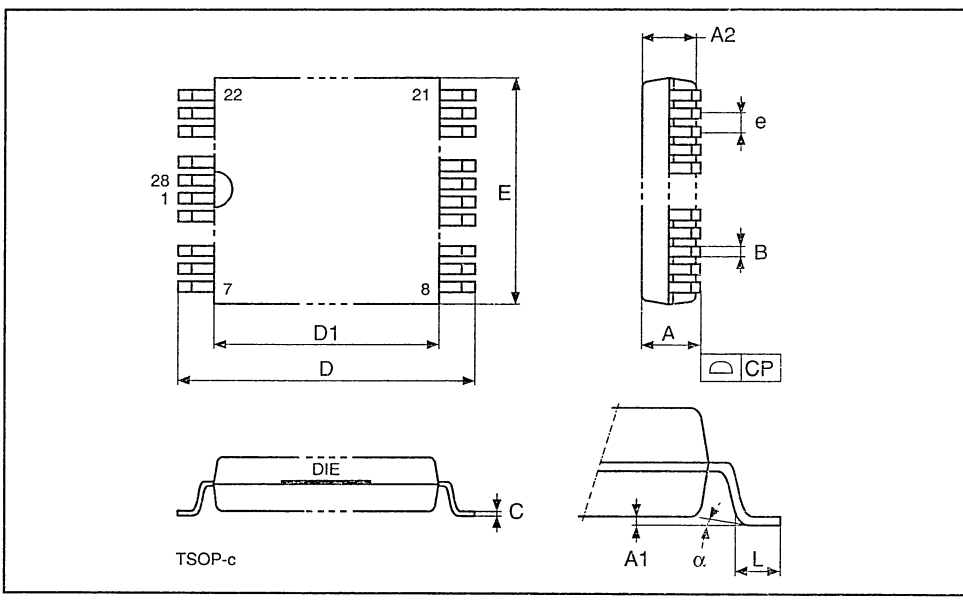


SO-b

Drawing is not to scale.

TSOP28 - 28 lead Plastic Thin Small Outline, 8 x 13.4mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.25			0.049
A1			0.20			0.008
A2		0.95	1.15		0.037	0.045
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		13.20	13.60		0.520	0.535
D1		11.70	11.90		0.461	0.469
E		7.90	8.10		0.311	0.319
e	0.55	-	-	0.022	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	28			28		
CP			0.10			0.004



TSOP-c

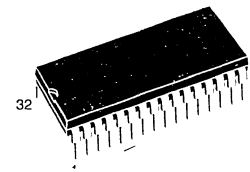
Drawing is not to scale.

M28010

1 Mbit (128K x 8) Parallel EEPROM With Software Data Protection

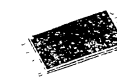
PRELIMINARY DATA

- Fast Access Time: 100 ns
- Single Supply Voltage:
  - 4.5 V to 5.5 V for M28010
  - 2.7 V to 3.6 V for M28010-W
  - 1.8 V to 2.4 V for M28010-R
- Low Power Consumption
- Fast BYTE and PAGE WRITE (up to 128 Bytes)
- Enhanced Write Detection and Monitoring:
  - Data Polling
  - Toggle Bit
  - Page Load Timer Status
- JEDEC Approved Bytewide Pin-Out
- Software Data Protection
- Hardware Data Protection
- Software Chip Erase
- 100000 Erase/Write Cycles (minimum)
- Data Retention (minimum): 10 Years



PDIP32 (BA)

PLCC32 (KA)



TSOP32 (NA)
8 x 20 mm

DESCRIPTION

The M28010 devices consist of 128Kx8 bits of low power, parallel EEPROM, fabricated with STMicroelectronics' proprietary double polysilicon CMOS technology. The devices offer fast access time, with low power dissipation, and require a single voltage supply (5V, 3V or 2V, depending on the option chosen).

Table 1. Signal Names

A0-A16	Address Input
DQ0-DQ7	Data Input / Output
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

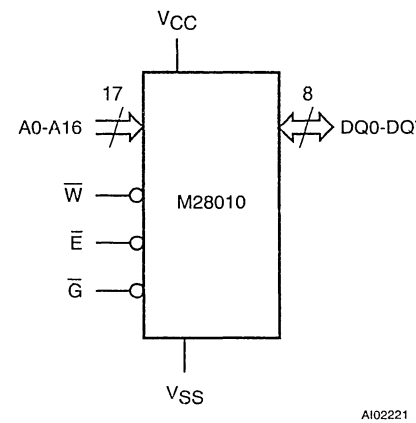
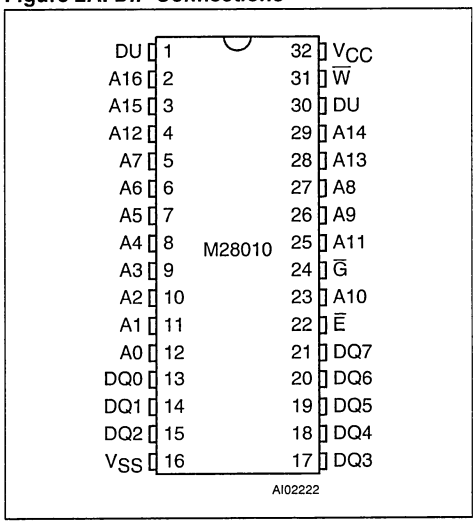
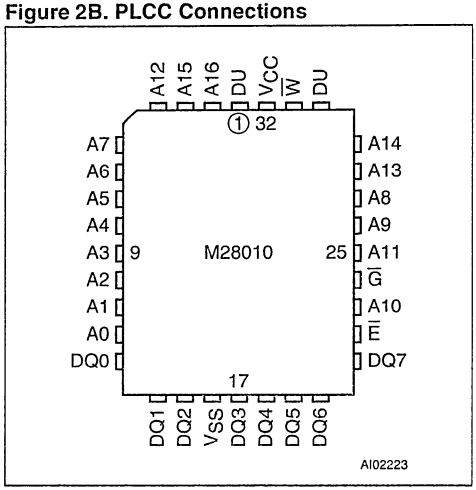


Figure 2A. DIP Connections



Note: 1. DU = Do Not Use

Figure 2B. PLCC Connections

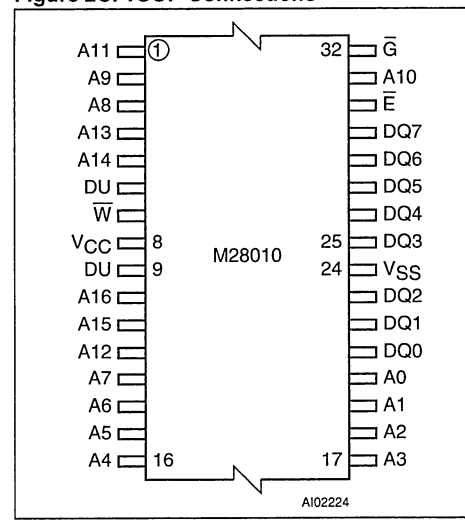


Note: 1. DU = Do Not Use

The device has been designed to offer a flexible microcontroller interface, featuring both hardware and software hand-shaking, with Data Polling and Toggle Bit. The device supports a 128 byte Page Write operation. Software Data Protection (SDP) is also supported, using the standard JEDEC algorithm.

The M28010 is designed for applications requiring as much as 100,000 write cycles and ten years of

Figure 2C. TSOP Connections



Note: 1. DU = Do Not Use

data retention. The organization of the data in a 4 byte (32-bit) "word" format leads to significant savings in power consumption. Once a byte has been read, subsequent byte read cycles from the same "word" (with addresses differing only in the two least significant bits) are fetched from the previously loaded Read Buffer, not from the memory array. As a result, the power consumption for these subsequent read cycles is much lower than the power consumption for the first cycle. By careful design of the memory access patterns, a 50% reduction in the power consumption is possible.

SIGNAL DESCRIPTION

The external connections to the device are summarized in Table 1, and their use in Table 3.

Addresses (A0-A16). The address inputs are used to select one byte from the memory array during a read or write operation.

Data In/Out (DQ0-DQ7). The contents of the data byte are written to, or read from, the memory array through the Data I/O pins.

Chip Enable ($\overline{E}$). The chip enable input must be held low to enable read and write operations. When Chip Enable is high, power consumption is reduced.

Output Enable ($\overline{G}$). The Output Enable input controls the data output buffers, and is used to initiate read operations.

Write Enable ($\overline{W}$). The Write Enable input controls whether the addressed location is to be read, from or written to.

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 85	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{CC}	Supply Voltage	–0.3 to V_{CCMAX}+1	V
V_{IO}	Input or Output Voltage (except A9)	–0.3 to V_{CC}+0.6	V
V_I	Input Voltage	–0.3 to 4.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]	2000	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100 pF, 1500 Ω)

Figure 3. Block Diagram

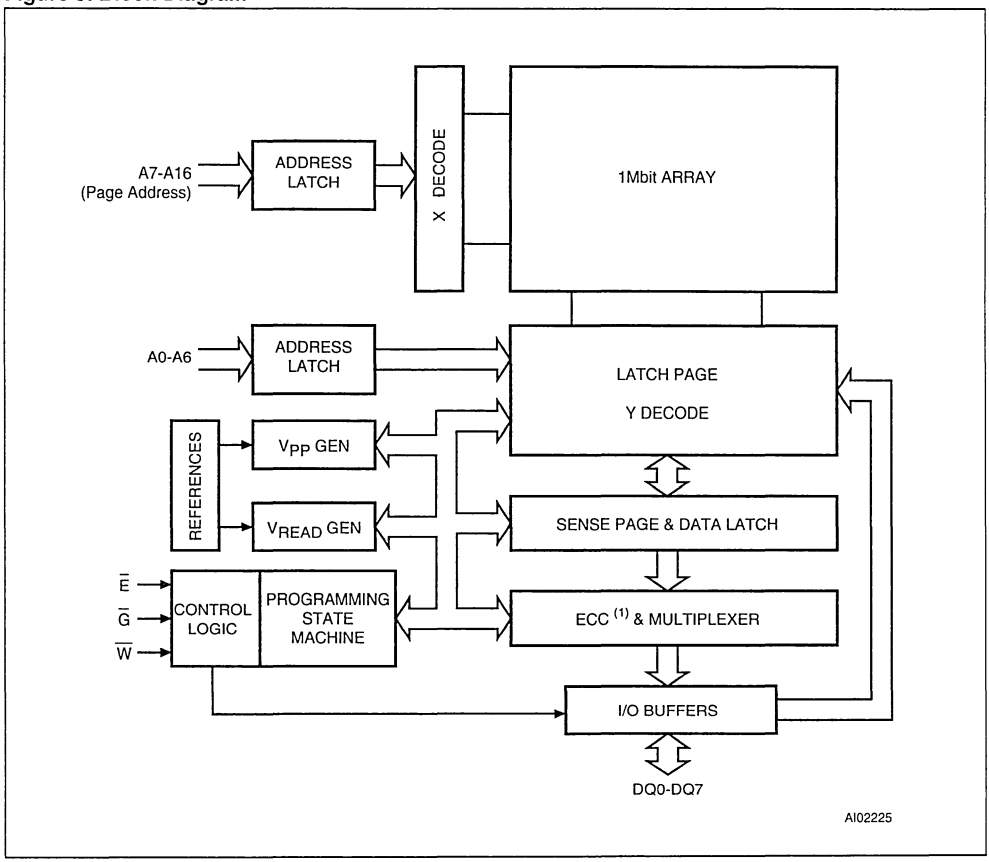


Table 3. Operating Modes [1]

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Out
Write	V_{IL}	V_{IH}	V_{IL}	Data In
Stand-by / Write Inhibit	V_{IH}	X	X	Hi-Z
Write Inhibit	X	X	V_{IH}	Data Out or Hi-Z
Write Inhibit	X	V_{IL}	X	Data Out or Hi-Z
Output Disable	X	V_{IH}	X	Hi-Z

Note: 1 X = V_{IH} or V_{IL}.

DEVICE OPERATION

In order to prevent data corruption and inadvertent write operations, an internal V_{CC} comparator inhibits the Write operations if the V_{CC} voltage is lower than V_{WI} (see Table 4A to Table 4C). Once the voltage applied on the V_{CC} pin goes over the V_{WI} threshold (V_{CC}>V_{WI}), write access to the memory is allowed after a time-out t_{PUW}, as specified in Table 4A to Table 4C.

Further protection against data corruption is offered by the $\overline{E}$ and $\overline{W}$ low pass filters: any glitch, on the $\overline{E}$ and $\overline{W}$ inputs, with a pulse width less than 10 ns (typical) is internally filtered out to prevent inadvertent write operations to the memory.

Read

The device is accessed like a static RAM. When $\overline{E}$ and $\overline{G}$ are low, and $\overline{W}$ is high, the contents of the addressed location are presented on the I/O pins.

Table 4A. Power-Up Timing[1] for M28010 (5V range)
(T_A = -40 to 85 °C; V_{CC} = 4.5 to 5.5 V)

Symbol	Parameter	Min.	Max.	Unit
t_{PUR}	Time Delay to Read Operation	5		ms
t_{PUW}	Time Delay to Write Operation (once $V_{CC} \geq V_{WI}$)	5		ms
V_{WI}	Write Inhibit Threshold	3.0	4.2	V

Note: 1 Sampled only, not 100% tested.

Table 4B. Power-Up Timing[1] for M28010-W (3V range)
(T_A = -40 to 85 °C; V_{CC} = 2.7 to 3.6 V)

Symbol	Parameter	Min.	Max.	Unit
t_{PUR}	Time Delay to Read Operation	5		ms
t_{PUW}	Time Delay to Write Operation (once $V_{CC} \geq V_{WI}$)	5		ms
V_{WI}	Write Inhibit Threshold	2.0	2.6	V

Note: 1. Sampled only, not 100% tested

Table 4C. Power-Up Timing[1] for M28010-R (2V range)
(T_A = -40 to 85 °C; V_{CC} = 1.8 to 2.4 V)

Symbol	Parameter	Min.	Max.	Unit
t_{PUR}	Time Delay to Read Operation	5		ms
t_{PUW}	Time Delay to Write Operation (once $V_{CC} \geq V_{WI}$)	5		ms
V_{WI}	Write Inhibit Threshold	1.2	1.7	V

Note: 1. Sampled only, not 100% tested.

Otherwise, when either $\overline{G}$ or $\overline{E}$ is high, the I/O pins revert to their high impedance state.

Write

Write operations are initiated when both $\overline{W}$ and $\overline{E}$ are low and $\overline{G}$ is high. The device supports both $\overline{W}$-controlled and $\overline{E}$-controlled write cycles (as shown in Figure 12 and Figure 13). The address is latched during the falling edge of $\overline{W}$ or $\overline{E}$ (which ever occurs later) and the data is latched on the rising edge of $\overline{W}$ or $\overline{E}$ (which ever occurs first). After a delay, t_{WLQ5H}, that cannot be shorter than the value specified in Table 9A to Table 9C, the internal write cycle starts. It continues, under internal timing control, until the write operation is complete. The commencement of this period can be detected by reading the Page Load Timer Status on DQ5. The end of the internal write cycle can be detected by reading the status of the Data Polling and the Toggle Bit functions on DQ7 and DQ6.

Figure 4. Software Data Protection Enable Algorithms (with or without Memory Write)

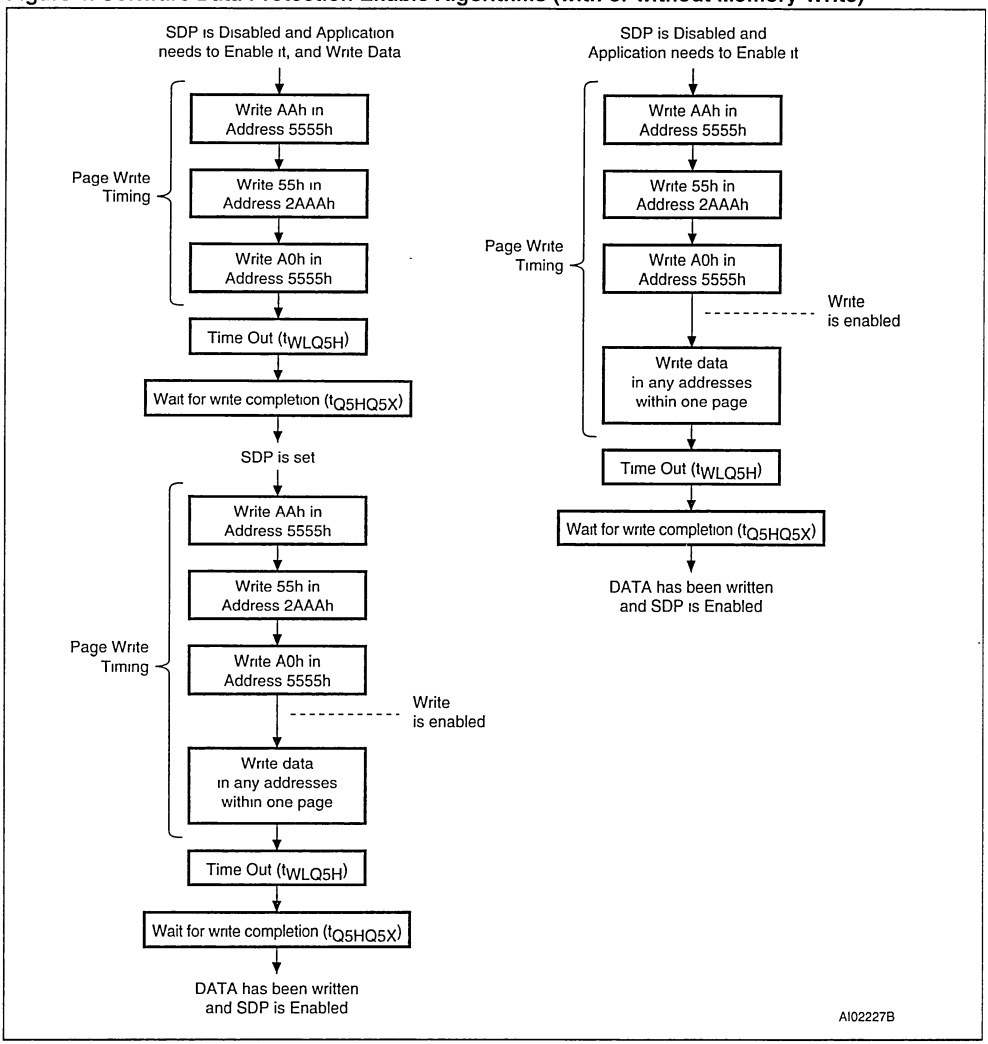
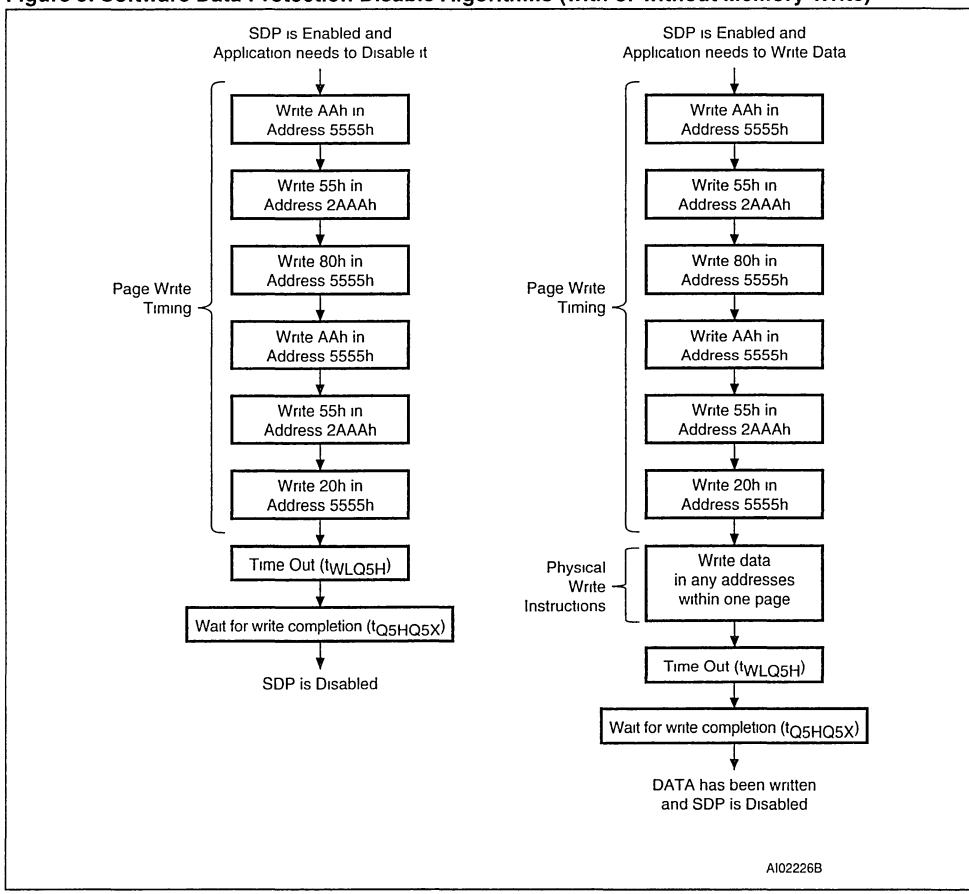


Figure 5. Software Data Protection Disable Algorithms (with or without Memory Write)



Page Write

The Page Write mode allows up to 128 bytes to be written on a single page in a single go. This is achieved through a series of successive Write operations, no two of which are separated by more than the t_{WLQ5H} value (as specified in Table 9A to Table 9C).

The page write can be initiated during any byte write operation. Following the first Byte Write instruction, the host may send another address and data with a minimum data transfer rate of:
$1/t_{WLQ5H}$.

The internal write cycle can start at any instant after t_{WLQ5H}. Once initiated, the write operation is internally timed, and continues, uninterrupted, until completion.

All bytes must be located on the same page address (A16-A7 must be the same for all bytes). Otherwise, the Page Write operation is not executed. The Page Write Abort event is indicated to the application via DQ1 (as described on page 8).

As with the single byte Write operation, described above, the DQ5, DQ6 and DQ7 lines can be used to detect the beginning and end of the internally controlled phase of the Page Write cycle.

Software Data Protection (SDP)

The device offers a software-controlled write-protection mechanism that allows the user to inhibit all write operations to the device, including chip erase. This can be useful for protecting the memory from inadvertent write cycles that may occur during periods of instability (uncontrolled bus conditions when excessive noise is detected, or when

Figure 6. Software Chip Erase Algorithm

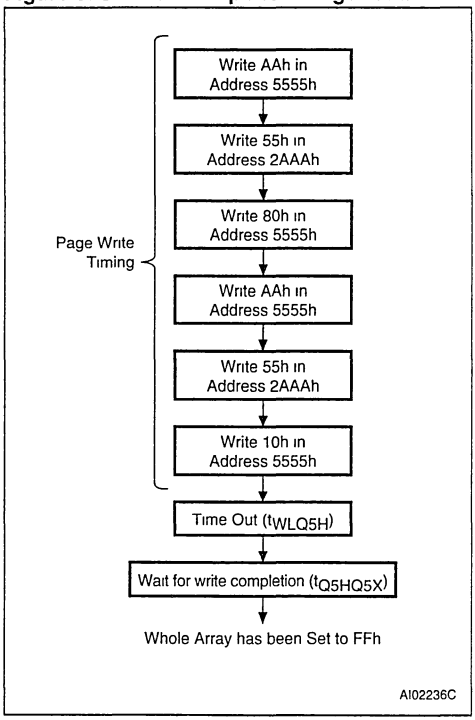


Figure 7. Status Bit Assignment

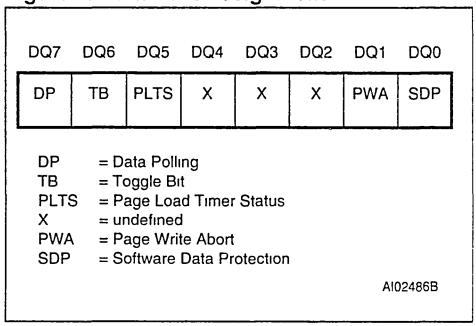
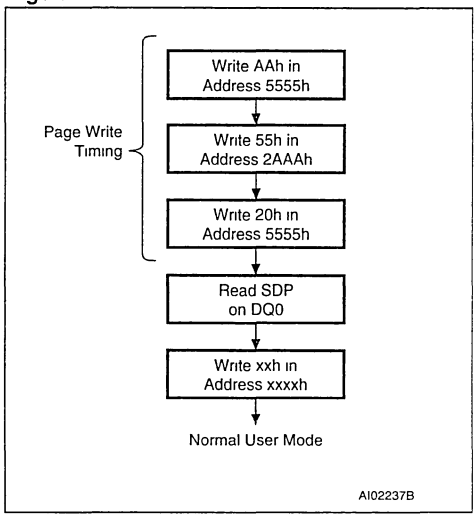


Figure 8. Software Data Protection Status Read Algorithm



power supply levels are outside their specified values).

By default, the device is shipped in the "unprotected" state: the memory contents can be freely changed by the user. Once the Software Data Protection Mode is enabled, all write commands are ignored, and have no effect on the memory contents.

The device remains in this mode until a valid Software Data Protection disable sequence is received. The device reverts to its "unprotected" state.

The status of the Software Data Protection (enabled or disabled) is represented by a non-volatile latch, and is remembered across periods of the power being off.

The Software Data Protection Enable command consists of the writing of three specific data bytes to three specific memory locations (each location being on a different page), as shown in Figure 4.

Similarly, to disable the Software Data Protection, the user has to write specific data bytes into six different locations, as shown in Figure 5. This complex series of operations protects against the chance of inadvertent enabling or disabling of the Software Data Protection mechanism.

When SDP is enabled, the memory array can still have data written to it, but the sequence is more complex (and hence better protected from inadvertent use). The sequence is as shown in Figure 5. This consists of an unlock key, to enable the write action, at the end of which the SDP continues to be enabled. This allows the SDP to be enabled, and data to be written, within a single Write cycle (t_{WC}).

Software Chip Erase

The device can be erased (with all bytes set to FFh) by using a six-byte software command code. This operation can be initiated only if the user loads, with a Page Write addressing mode, six

specific data bytes to six specific locations (as shown in Figure 6). The complexity of the sequence has been designed to guard against inadvertent use of the command.

Status Bits

The devices provide five status bits (DQ7, DQ6, DQ5, DQ1 and DQ0) for use during write operations. These allow the application to use the write time latency of the device for getting on with other work. These signals are available on the I/O port bits DQ7, DQ6, DQ5, DQ1 and DQ0 (but only during the internal write cycle, t_{Q5HQ5X}).

Data Polling bit (DQ7). The internally timed write cycle starts as soon as t_{WLQ5H} (defined in Table 9A to Table 9C) has elapsed since the previous byte was latched in to the memory. The value of the DQ7 bit of this last byte, is used as a signal throughout this write operation: it is inverted while the internal write operation is underway, and is inverted back to its original value once the operation is complete.

Toggle bit (DQ6). The device offers another way for determining when the internal write cycle is running. During the internal write cycle, DQ6 toggles from '0' to '1' and '1' to '0' (the first read value being '0') on subsequent attempts to read any byte of the memory. When the internal write cycle is complete, the toggling is stopped, and the values read on DQ7-DQ0 are those of the addressed memory byte. This indicates that the device is again available for new Read and Write operations.

Page Load Timer Status bit (DQ5). An internal timer is used to measure the period between successive Write operations, up to t_{WLQ5H} (defined in Table 9A to Table 9C). The DQ5 line is held low to show when this timer is running (hence showing that the device has received one write operation, and is waiting for the next). The DQ5 line is held high when the counter has overflowed (hence showing that the device is now starting the internal write to the memory array).

Page Write Abort bit (DQ1). During a page write operation, the A16 to A7 signals should be kept constant. They should not change while successive data bytes are being transferred to the internal latches of the memory device. If a change occurs on any of the pins, A16 to A7, during the page write operation (that is, before the falling edge of $\overline{W}$ or $\overline{E}$, which ever occurs later), the internal write cycle is not started, and the internal circuitry is completely reset.

The abort signal can be observed on the DQ1 pin, using a normal read operation. This can be performed at any time during the byte load cycle, t_{WLQ5H}, or while the $\overline{W}$ input is being held high between two load cycles. The default value of DQ1 is initially set to '0' and changes to '1' if the internal circuitry has detected a change on any of the address pins A16 to A7. This PWA bit can be checked regardless of whether Software Data Protection is enabled or disabled.

Software Data Protection bit (DQ0). Reading the SDP bit (DQ0) allows the user to determine whether the Software Data Protection mode has been enabled (SDP=1) or disabled (SDP=0). The SDP bit (DQ0) can be read by using a dedicated algorithm (as shown in Figure 8), or can be combined

Table 5A. Read Mode DC Characteristics for M28010 (5V range)
(T_A = -40 to 85 °C; V_{CC} = 4.5 to 5.5 V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$0 V \le V_{IN} \le V_{CC}$		5	µA
I_{LO}	Output Leakage Current	$0 V \le V_{OUT} \le V_{CC}$		5	µA
I_{CC} [1]	Supply Current (CMOS inputs)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 0.1 MHz		2	mA
		$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5 MHz		22	mA
		$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 10 MHz		40	mA
I_{CC1} [1]	Supply Current (Stand-by) CMOS	$\overline{E} > V_{CC} - 0.3$ V		30	µA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –400 µA	2.4		V

Note: 1. All inputs and outputs open circuit.

Table 5B. Read Mode DC Characteristics for M28010-W (3V range)
(T_A = -40 to 85 °C; V_{CC} = 2.7 to 3.6 V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$0 V \le V_{IN} \le V_{CC}$		5	µA
I_{LO}	Output Leakage Current	$0 V \le V_{OUT} \le V_{CC}$		5	µA
I_{CC} [1]	Supply Current (CMOS inputs)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 0.1 MHz		2	mA
		$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5 MHz		15	mA
		$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 10 MHz		26	mA
I_{CC1} [1]	Supply Current (Stand-by) CMOS	$\overline{E} > V_{CC} - 0.3 V$		30	µA
V_{IL}	Input Low Voltage		–0.3	0.6	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA	2.4		V

Note: 1. All inputs and outputs open circuit.

Table 5C. Read Mode DC Characteristics for M28010-R (2V range)
(T_A = -40 to 85 °C; V_{CC} = 1.8 to 2.4 V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$0 V \le V_{IN} \le V_{CC}$		5	µA
I_{LO}	Output Leakage Current	$0 V \le V_{OUT} \le V_{CC}$		5	µA
I_{CC} [1]	Supply Current (CMOS inputs)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 0.1 MHz, V_{CC} = 2.4 V		2	mA
		$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 5 MHz, V_{CC} = 2.4 V		12	mA
I_{CC1} [1]	Supply Current (Stand-by) CMOS	$\overline{E} > V_{CC} - 0.3 V$		30	µA
V_{IL}	Input Low Voltage		- 0.3	0.2	V
V_{IH}	Input High Voltage		V_{CC} - 0.3	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 0.4 mA		0.15	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA	V_{CC} - 0.15		V

Note: 1. All inputs and outputs open circuit.

with the reading of the DP bit (DQ7), TB bit (DQ6) and PLTS bit (DQ5).

Table 6. Input and Output Parameters[1] (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0 V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V		12	pF

Note: 1. Sampled only, not 100% tested.

Table 7. AC Measurement Conditions

Input Rise and Fall Times	≤ 5 ns
Input Pulse Voltages	0 V to V_{CC}
Input and Output Timing Ref. Voltages	$V_{CC}/2$

Figure 9. AC Testing Input Output Waveforms

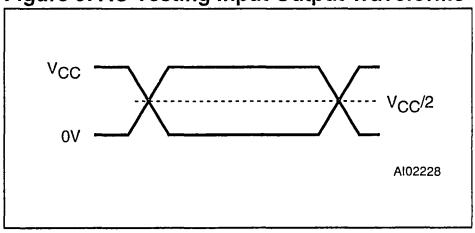


Figure 10. AC Testing Equivalent Load Circuit

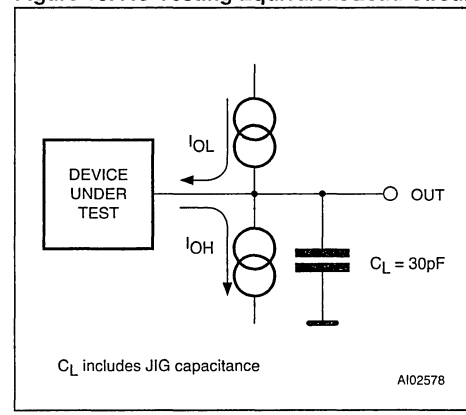


Table 8A. Read Mode AC Characteristics for M28010 (5V range)
(T_A = -40 to 85 °C; V_{CC} = 4.5 to 5.5 V)

Symbol	Alt.	Parameter	Test Condition	M28010				Unit
				-10		-12		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		40		45	ns
t_{EHQZ}[1]	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	40	0	45	ns
t_{GHQZ}[1]	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	40	0	45	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Note: 1. Output Hi-Z is defined as the point at which data is no longer driven

Table 8B. Read Mode AC Characteristics for M28010-W (3V range)
(T_A = -40 to 85 °C; V_{CC} = 2.7 to 3.6 V)

Symbol	Alt.	Parameter	Test Condition	M28010-W						Unit
				-10		-12		-15		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120		150	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120		150	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		70		80		100	ns
t_{EHQZ}[1]	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	50	0	60	0	70	ns
t_{GHQZ}[1]	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	50	0	60	0	70	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

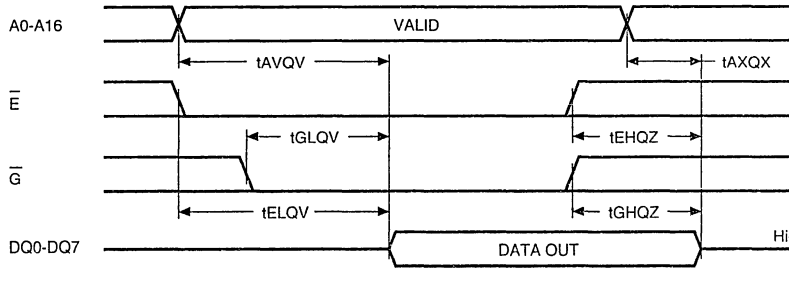
Note: 1. Output Hi-Z is defined as the point at which data is no longer driven.

Table 8C. Read Mode AC Characteristics for M28010-R (2V range)
(T_A = -40 to 85 °C; V_{CC} = 1.8 to 2.4 V)

Symbol	Alt.	Parameter	Test Condition	M28010-R				Unit
				-20		-25		
				Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		200		250	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		200		250	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		80		90	ns
t_{EHQZ}[1]	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	50	0	60	ns
t_{GHQZ}[1]	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	50	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		ns

Note: 1. Output Hi-Z is defined as the point at which data is no longer driven.

Figure 11. Read Mode AC Waveforms (with Write Enable, $\overline{W}$, high)



Note: 1. Write Enable ($\overline{W}$) = V_{IH}

Table 9A. Write Mode AC Characteristics for M28010 (5V range)
(T_A = -40 to 85 °C; V_{CC} = 4.5 to 5.5 V)

Symbol	Alt.	Parameter	Test Condition	M28010		Unit
				Min	Max	
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G}$ = V_{IH}, $\overline{W}$= V_{IL}	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E}$ = V_{IL}	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W}$ = V_{IL}	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		70		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		70		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		100		ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		100		ns
t_{WLQ5H}	t_{BLC}	Time-out after the last byte write		150		µs
t_{Q5HQ5X}	t_{WC}	Byte Write Cycle time			5	ms
		Page Write Cycle time (up to 128 bytes)			10	ms
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Table 9B. Write Mode AC Characteristics for M28010-W (3V range)
(T_A = -40 to 85 °C; V_{CC} = 2.7 to 3.6 V)

Symbol	Alt.	Parameter	Test Condition	M28010-W		Unit
				Min	Max	
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G}$ = V_{IH}, $\overline{W}$= V_{IL}	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E}$ = V_{IL}	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W}$ = V_{IL}	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G}$ = V_{IH}	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		70		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		70		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		100		ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		50		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		100		ns
t_{WLQ5H}	t_{BLC}	Time-out after the last byte write		150		µs
t_{Q5HQ5X}	t_{WC}	Byte Write Cycle time			5	ms
		Page Write Cycle time (up to 128 bytes)			10	ms
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		50		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		50		ns

Table 9C. Write Mode AC Characteristics for M28010-R (2V range)
(T_A = -40 to 85 °C; V_{CC} = 1.8 to 2.4 V)

Symbol	Alt.	Parameter	Test Condition	M28010-R		Unit
				Min	Max	
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	0		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	$\overline{G} = V_{IH}$, $\overline{W} = V_{IL}$	0		ns
t_{ELWL}	t_{CES}	Chip Enable Low to Write Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{GHWL}	t_{OES}	Output Enable High to Write Enable Low	$\overline{E} = V_{IL}$	0		ns
t_{GHEL}	t_{OES}	Output Enable High to Chip Enable Low	$\overline{W} = V_{IL}$	0		ns
t_{WLEL}	t_{WES}	Write Enable Low to Chip Enable Low	$\overline{G} = V_{IH}$	0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition		120		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition		120		ns
t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High		120		ns
t_{WHEH}	t_{CEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low		0		ns
t_{EHWH}	t_{WEH}	Chip Enable High to Write Enable High		0		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition		0		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low		100		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High		120		ns
t_{WLQ5H}	t_{BLC}	Time-out after the last byte write		150		µs
t_{WHRH}	t_{WC}	Byte Write Cycle time			5	ms
		Page Write Cycle time (up to 128 bytes)			10	ms
t_{DVWH}	t_{DS}	Data Valid before Write Enable High		120		ns
t_{DVEH}	t_{DS}	Data Valid before Chip Enable High		120		ns

Figure 12. Write Mode AC Waveforms (Write Enable, $\overline{W}$, controlled)

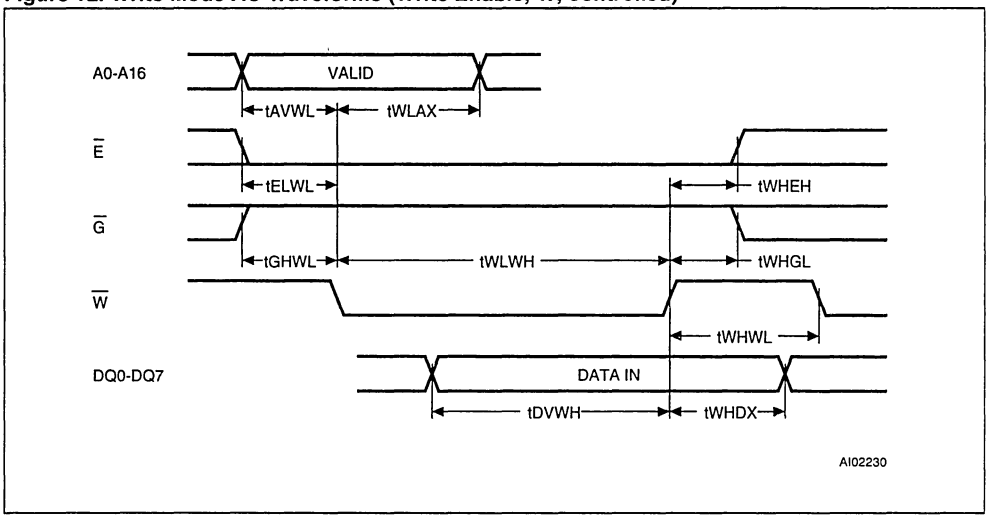


Figure 13. Write Mode AC Waveforms (Chip Enable, $\overline{E}$, controlled)

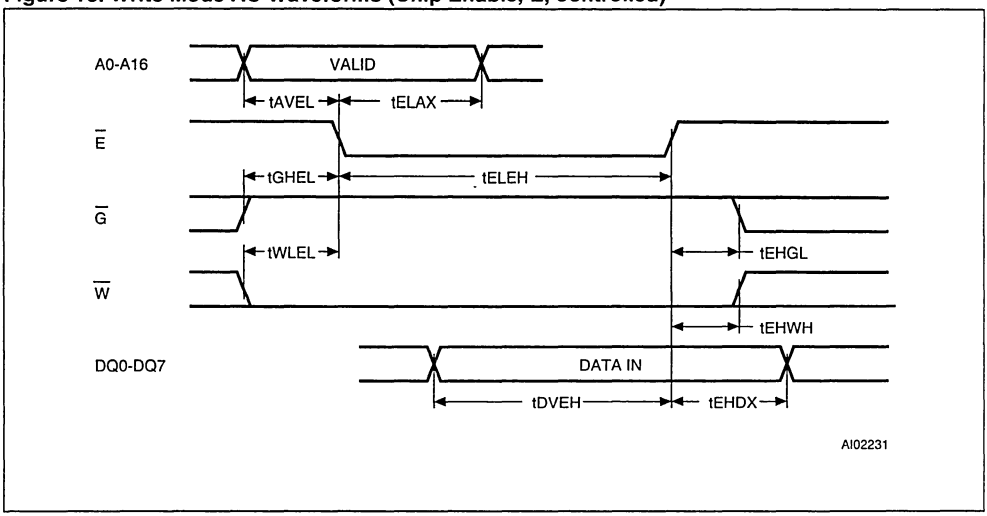


Figure 14. Page Write Mode AC Waveforms (Write Enable, $\overline{W}$, controlled)

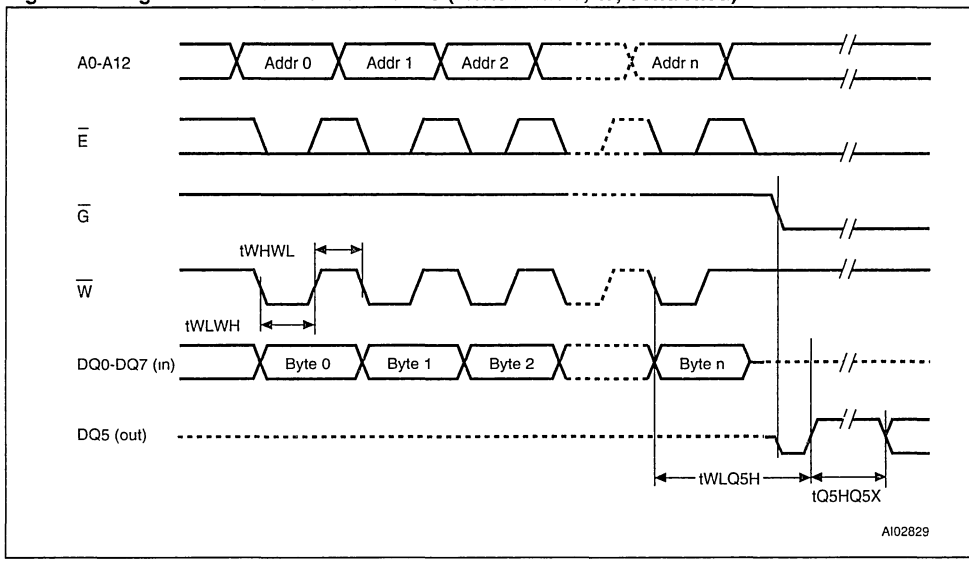
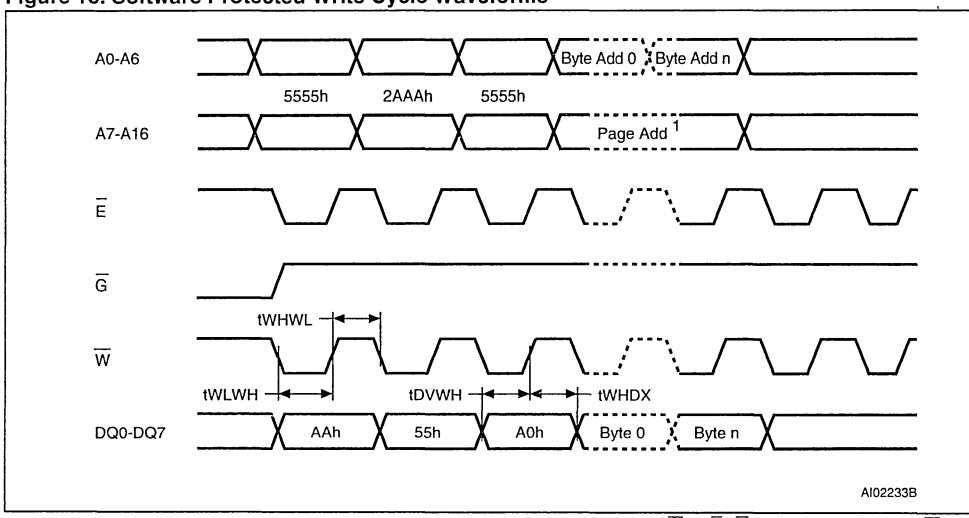


Figure 15. Software Protected Write Cycle Waveforms



Note 1. A16 to A7 must specify the same page address during each high-to-low transition of $\overline{W}$ (or $\overline{E}$). $\overline{G}$ must be high only when $\overline{W}$ and $\overline{E}$ are both low

Figure 16. Data Polling Sequence Waveforms

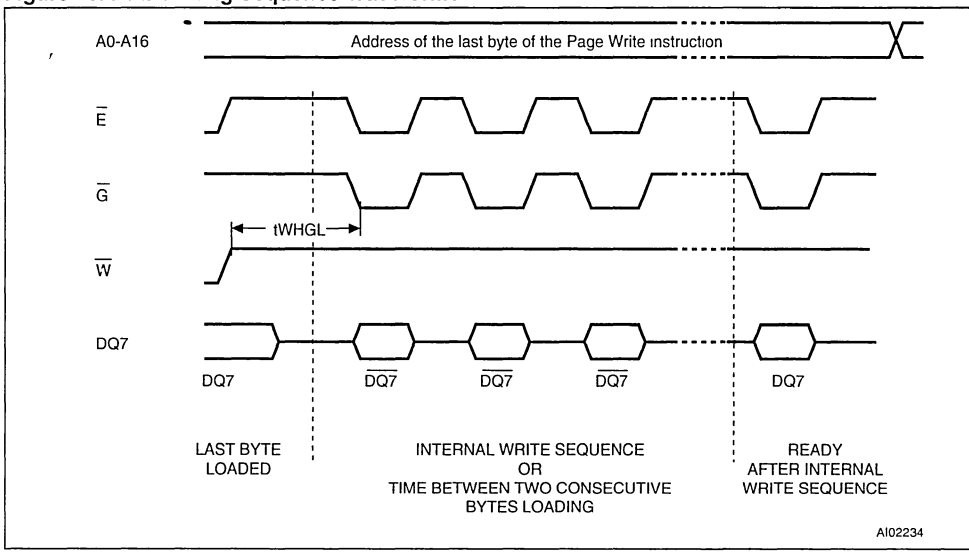
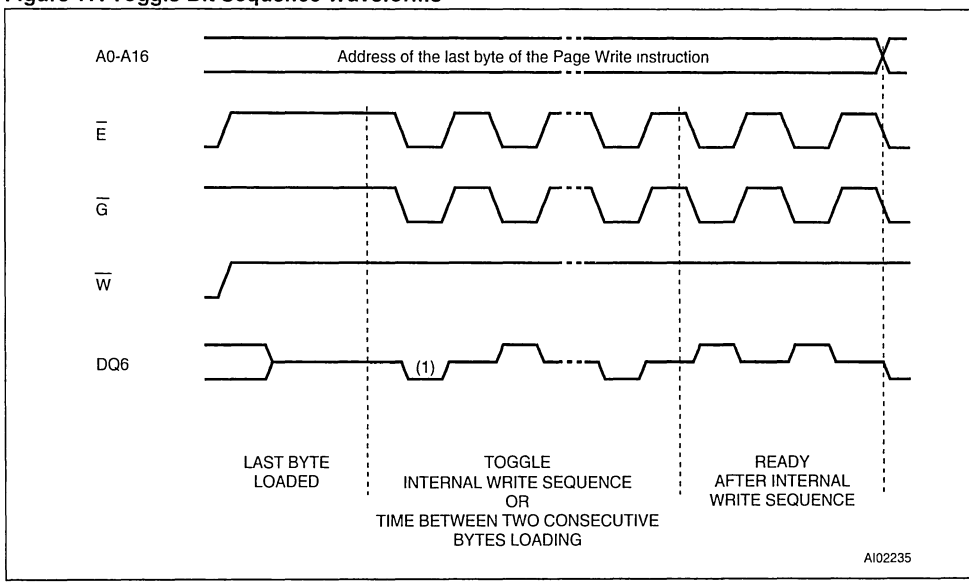
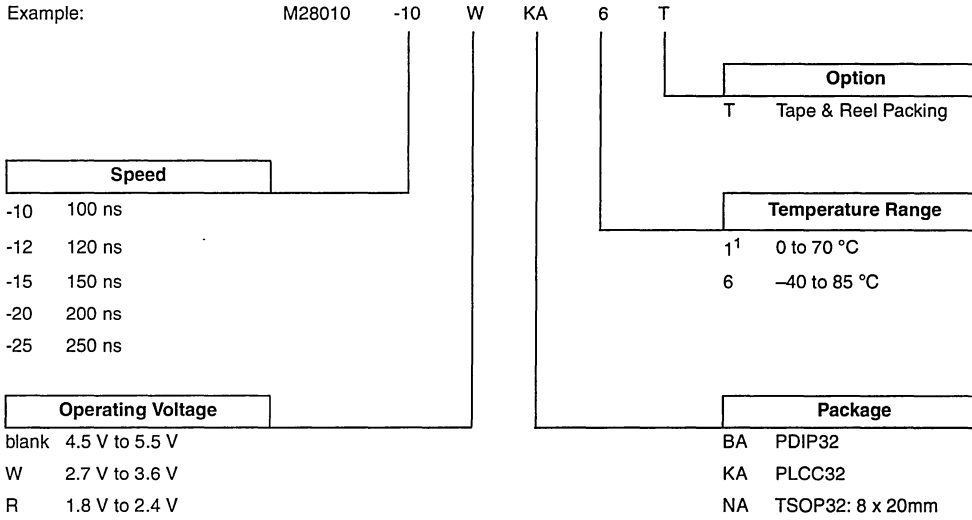


Figure 17. Toggle Bit Sequence Waveforms



Note: 1. The Toggle Bit is first set to '0'.

Table 10. Ordering Information Scheme



Note: 1. This temperature range on request only.

ORDERING INFORMATION

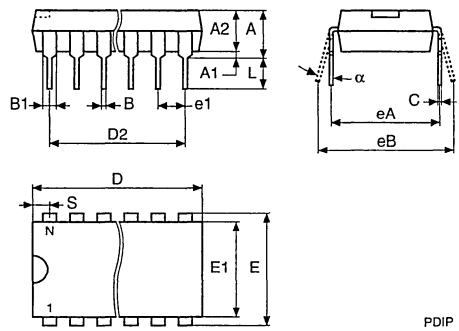
Devices are shipped from the factory with the memory content set at all '1's (FFh).

The notation used for the device number is as shown in Table 10. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 11. PDIP32 - 32 lead Plastic DIP, 600 mils width, Package Mechanical Data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		–	5.08		–	0.200
A1		0.38	–		0.015	–
A2		3.56	4.06		0.140	0.160
B		0.38	0.51		0.015	0.020
B1	1.52	–	–	0.060	–	–
C		0.20	0.30		0.008	0.012
D		41.78	42.04		1.645	1.655
D2	38.10	–	–	1.500	–	–
E	15.24	–	–	0.600	–	–
E1		13.59	13.84		0.535	0.545
e1	2.54	–	–	0.100	–	–
eA	15.24	–	–	0.600	–	–
eB		15.24	17.78		0.600	0.700
L		3.18	3.43		0.125	0.135
S		1.78	2.03		0.070	0.080
α		0°	10°		0°	10°
N	32			32		

Figure 18. PDIP32 (BA)

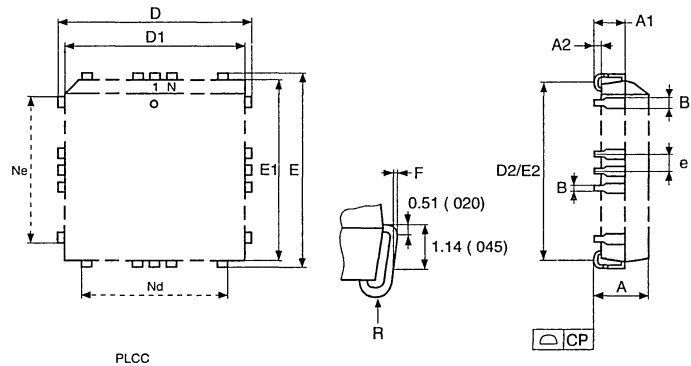


Note: 1. Drawing is not to scale

Table 12. PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
A2		–	0.38		–	0.015
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
F		0.00	0.25		0.000	0.010
R	0.89	–	–	0.035	–	–
N		32			32	
Nd		7			7	
Ne		9			9	
CP			0.10			0.004

Figure 19. PLCC32 (KA)

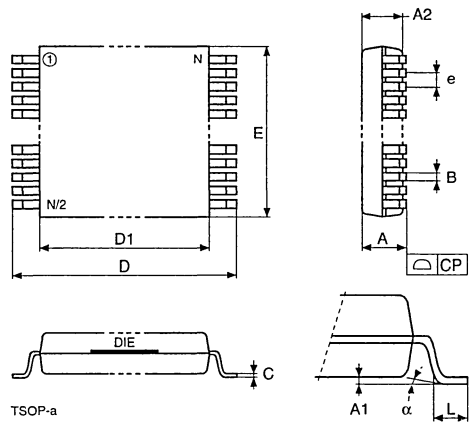


Note: 1 Drawing is not to scale.

Table 13. TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 20mm, Package Mechanical Data

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.20			0.047
A1		0.05	0.17		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		32			32	
CP			0.10			0.004

Figure 20. TSOP32 (NS)



Note: 1 Drawing is not to scale.

FLASH+

Single Chip 2 Mbit Flash and 64 Kbit Parallel EEPROM Memory

PRELIMINARY DATA

- 2.7V to 3.6V SUPPLY VOLTAGE for PROGRAM, ERASE and READ OPARATIONS
- 100ns ACCESS TIME (Flash and EEPROM blocks)
- WRITE, PROGRAM and ERASE STATUS BITS
- CONCURRENT MODE (Read Flash while writing to EEPROM)
- 100,000 ERASE/WRITE CYCLES
- 10 YEARS DATA RETENTION
- LOW POWER CONSUMPTION
  - Stand-by mode: 60µA
  - Automatic Stand-by mode
  - Deep Power Down mode
- 64 bytes ONE TIME PROGRAMMABLE MEMORY
- STANDARD EPROM/OTP MEMORY PACKAGE
- EXTENDED TEMPERATURE RANGES

TSOP32 (NA)
8 x 20 mm

TSOP32 (NB)
8 x 14 mm

DESCRIPTION

The M39208 is a memory device combining Flash and EEPROM into a single chip and using single supply voltage. The memory is mapped in two blocks: 2 Mbit of Flash memory and 64 Kbit of EEPROM memory. Each space is independant for writing, in concurrent mode the Flash Memory can be read while the EEPROM is being written.

Table 1. Signal Names

A0-A17	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{EE}$	EEPROM Block Enable
$\overline{EF}$	Flash Block Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

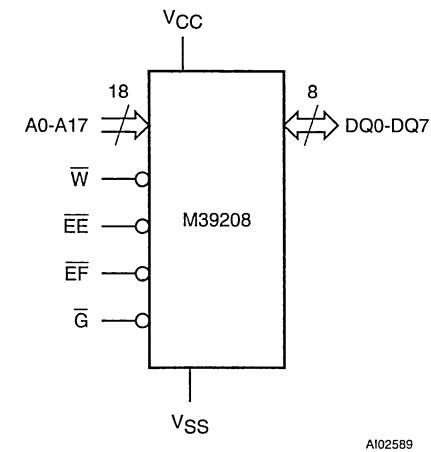
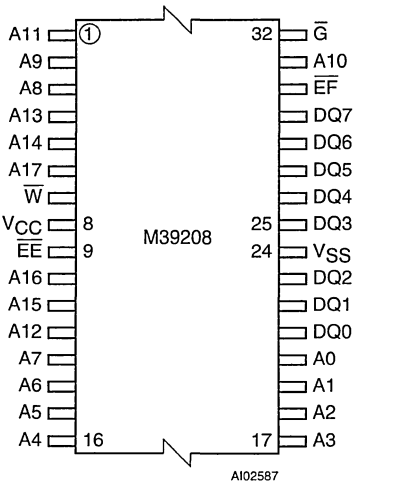


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 85	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages	–0.6 to 5	V
V_{CC}	Supply Voltage	–0.6 to 5	V
V_{A9}, V_G, V_{EF} (2)	A9, $\overline{G}$, $\overline{EF}$ Voltage	–0.6 to 13.5	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.

Figure 2. TSOP Pin Connections



DESCRIPTION (Cont'd)

An additional 64 bytes of EPROM are One Time Programmable.

The M39208 EEPROM memory block may be written by byte or by page of 64 bytes and the integrity of the data can be secured with the help of the Software Data Protection (SDP).

The M39208 Flash Memory block offers 4 sectors of 64 Kbytes, each sector may be erased individually, and programmed Byte-by-Byte. Each sector can be separately protected and unprotected against program and erase. Sector erasure may be suspended, while data is read from other sectors of the Flash memory block (or EEPROM memory block), and then resumed.

During a Program or Erase cycle in the Flash memory block or during a Write in the EEPROM memory block, the status of the M39208 internal logic can be read on the Data Outputs DQ7,DQ6, DQ5 and DQ3.

PIN DESCRIPTION

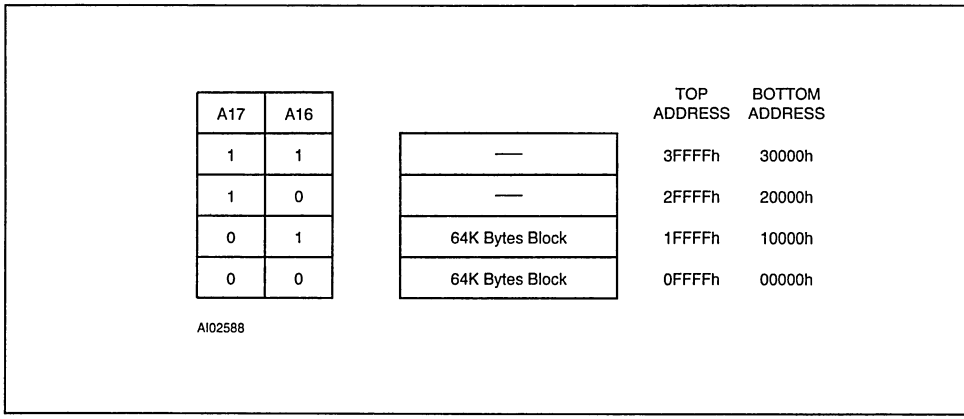
Address Inputs (A0-A17). The address inputs for the memory array are latched during a write operation. A0-A12 access locations in the EEPROM memory block A0-A17 access locations in the Flash memory block. The memory block selected is given by the state on the $\overline{E}$ and $\overline{EF}$ inputs respectively.

When a specific voltage (V_{ID}) is applied on the A9 address input, additional specific areas can be accessed: Read the Manufacturer identifier, Read the Flash block identifier, Read/Write the EEPROM block identifier, Verify the Flash Sector Protection Status.

Data Input/Output (DQ0-DQ7). A write operation inputs one byte which is latched when $\overline{E}$ (or $\overline{EF}$) and Write Enable $\overline{W}$ are driven active.

Data read is valid when one Chip Enable (Chip Enable Flash or Chip Enable EEPROM) and Output Enable are driven active. The output is high

Figure 3. Flash Block Sectors



impedance when the chip is deselected (both $\overline{EE}$ and $\overline{EF}$ driven high) or the outputs are disabled ($\overline{G}$ driven high).

Read operations are used to output the contents from the memory, the Manufacturer identifier, the Flash Sector protection Status, the Flash block Identifier, the EEPROM identifier or the OTP row content.

Memory Block Enable ($\overline{EE}$ and $\overline{EF}$). The Memory Block Enable ($\overline{EE}$ or $\overline{EF}$) activates the memory control logic, input buffers, decoders and sense amplifiers. When the $\overline{EE}$ input is driven high, the EEPROM memory block is not selected; when the $\overline{EF}$ input is driven high, the Flash memory block is not selected. Attempts to access both EEPROM and Flash blocks ($\overline{EE}$ low and $\overline{EF}$ low) are forbidden. Switching between the two memory block enables ($\overline{EE}$ and $\overline{EF}$) must not be made on the same clock cycle, a delay of greater than t_{EHFL} must be inserted.
The M39208 is in standby when both $\overline{EF}$ and $\overline{EE}$ are High (when no internal Erase or programming is running). The power consumption is reduced to the standby level and the outputs are in the high impedance state, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

After 150ns of inactivity and when the addresses are driven at CMOS levels, the chip automatically enters a pseudo standby mode where consumption is reduced to the CMOS standby value, while the outputs continue to drive the bus.

Output Enable ($\overline{G}$). The Output Enable gates the outputs through the data buffers during a read operation. The data outputs are in the high impedance state when the Output Enable $\overline{G}$ is High.

During Sector Protect and Sector Unprotect operations, the $\overline{G}$ input must be forced to V_{ID} level (12V + 0.5V) (for Flash memory block only).

Write Enable ($\overline{W}$). Addresses are latched on the falling edge of $\overline{W}$, and Data Inputs are latched on the rising edge of $\overline{W}$.

OPERATIONS

The M39208 memory is addressed through 18 inputs A0-A17 and provides data on eight Data Inputs/Outputs DQ0-DQ7 with the help of four control lines: Chip Enable EEPROM ($\overline{EE}$), Chip Enable Flash ($\overline{EF}$), Output Enable ($\overline{E}$) and Write Enable ($\overline{W}$) inputs.

An operation is defined as the basic decoding of the logic level applied to the control input pins ($\overline{EF}$, $\overline{EE}$, $\overline{G}$, $\overline{W}$) and the specified voltages applied on the relevant address pins. These operations are detailed in Table 3.

Read. Both Chip Enable and Output Enable (that is $\overline{EF}$ and $\overline{G}$ or $\overline{EE}$ and $\overline{G}$) must be low in order to read the output of the memory.

Read operations are used to output the contents from the Flash or EEPROM block, the Manufacturer identifier, the Flash Sector protection Status, the Flash block Identifier, the EEPROM identifier or the OTP row content.

Notes:

- The Chip Enable input mainly provides power control and should be used for device selection. The Output Enable input should be used to gate data onto the output in combination with active $\overline{EF}$ or $\overline{EE}$ input signals.
- The data read depends on the previous instruction entered into the memory (see Table 4).

Table 3. Basic Operations

Operation	$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Read in Flash Block
	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Read in EEPROM Block
Write	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Write in Flash Block
	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Write in EEPROM Block
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
	V_{IH}	V_{IL}	V_{IH}	X	Hi-Z
Standby	V_{IH}	V_{IH}	X	X	Hi-Z

Note: X = V_{IL} or V_{IH}.

Write. A Write operation can be used for two goals:

- either write data in the EEPROM memory block
- or enter a sequence of bytes composing an instruction.

The reader should note that Programming a Flash byte is an instruction (see Instructions paragraph).

Writing data requires:

- the Chip Enable (either $\overline{EE}$ or $\overline{EF}$) to be Low
- the Write Enable ($\overline{W}$) to be Low with Output Enable (G) High.

Addresses in Flash block (or EEPROM block) are latched on the falling edge of $\overline{W}$ or $\overline{EF}$ ($\overline{EE}$) whichever occurs last; the data to be written in Flash block (EEPROM block) is latched on the rising edge of $\overline{W}$ or $\overline{EF}$ ($\overline{EE}$) whichever occurs first.

Specific Read and Write Operations. Device specific data is accessed through operations decoding the V_{ID} level applied on A9 (V_{ID} = 12V + 0.5V) and the logic levels applied on address inputs (A0, A1, A6). These specific operations are:

- Read the Manufacturer identifier
- Read the Device identifier
- Define the Flash Sector protection
- Read the EEPROM identifier
- Write the EEPROM identifier

Note: The OTP row (64 bytes) is accessed with a specific software sequence detailed in the paragraph "Write in OTP row".

Instructions

An instruction is defined as a sequence of specific Write operations. Each received byte is sequentially decoded (and not executed as standard Write operations) and the instruction is executed when the correct number of bytes are properly received and the time between two consecutive bytes is shorter than the time-out value.

The sequencing of any instruction must be followed exactly, any invalid combination of instruction bytes or time-out between two consecutive bytes will reset the device logic into a Read memory state (when addressing the Flash block) or directly decoded as a single operation when addressing the EEPROM block.

The M39208 set of instructions includes:

- Program a byte in the Flash block
- Read a Flash sector protection status
- Erase instructions: Flash Sector Erase, Flash Block Erase, Flash Sector Erase Suspend, Flash Sector Erase Resume
- EEPROM power down
- Deep power down
- Set/Reset the EEPROM software write protection (SDP)
- OTP row access
- Reset and Return
- Read identifiers: read the manufacturer identifier, Read the Flash block identifier

These instructions are detailed in Table 4.

For efficient decoding of the instruction, the two first bytes of an instruction are the coded cycles and are followed by a command byte or a confirmation byte. The coded cycles consist of writing the data AAh at address 5555h during the first cycle and data 55h at address 2AAAh during the second cycle.

In the specific case of the Erase instruction, the instruction expects confirmation by two additional coded cycles.

Table 4. Instructions (1)

Instruction	$\overline{EE}$	$\overline{EF}$	Cycle 1	Cycle 2	Cycle 3	Cycle 4	Cycle 5	Cycle 6	Cycle 7
Read Manufacturer Identifier (2)	1	0	AAh @5555h	55h @2AAAh	90h @5555h	Read Identifier with (A0,A1,A6) at (0,0,0)			
Read Flash Identifier (2)	1	0	AAh @5555h	55h @2AAAh	90h @5555h	Read identifier with (A0,A1,A6) at (1,0,0)			
Read OTP Row	0	1	AAh @5555h	55h @2AAAh	90h @5555h	Read byte 1	Read byte 2		Read byte N
Read Block Protection Status (2)	1	0	AAh @5555h	55h @2AAAh	90h @5555h	Read Identifier with (A0,A1,A6) at (0,1,0)			
Program a Flash Byte	1	0	AAh @5555h	55h @2AAAh	A0h @5555h	Data @address			
Erase one Flash Block	1	0	AAh @5555h	55h @2AAAh	80h @5555h	AAh @5555h	55h @2AAAh	30h @Sector address	30h @Sector address(3)
Erase the Whole Flash	1	0	AAh @5555h	55h @2AAAh	80h @5555h	AAh @5555h	55h @2AAAh	10h @5555h	
Suspend Block Erase	1	0	B0h @any address						
Resume Block Erase	1	0	30h @any address						
EEPROM Power Down	0	1	AAh @5555h	55h @2AAAh	30h @5555h				
Deep Power Down	1	0	20h @5555h						
SDP Enable (EEPROM)	0	1	AAh @5555h	55h @2AAAh	A0h @5555h	Write byte 1	Write byte 2		Write byte N
SDP Disable (EEPROM)	0	1	AAh @5555h	55h @2AAAh	80h @5555h	AAh @5555h	55h @2AAAh	20h @5555h	
Write in OTP Row	0	1	AAh @5555h	55h @2AAAh	B0h @5555h	Write byte 1	Write byte 2		Write byte N
Return (from OTP Read or EEPROM Power Down)	0	1	F0h @ any address						
Reset	1	0	AAh @5555h	55h @2AAAh	F0h @any Address				
Reset (short instruction)	1	0	F0h @any address						

Notes: 1. AAh @5555h means Write byte AAh at address 5555h.
2. This instruction can also be performed as a simple Read operation with A9=V_{ID} (refer to READ chapter).
3. Additional blocks to be erased must be entered within 80µs.

Table 5. Device Identifiers

Identifier	$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A9	Other Addresses	DQ0 - DQ7
Read the Manufacturer Identifier	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{ID}	Don't Care	20h
Read the Flash Block Identifier	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	Don't Care	t.b.d.
Read the EEPROM Block Identifier	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	V_{IL}	V_{ID}	Don't Care	64 bytes user defined

Note: X = Don't Care.

POWER SUPPLY and CURRENT CONSUMPTION

EEPROM Power Down. The M39208 can be set with the EEPROM in power down with the help of the EEPROM power down instruction (see Table 4). Once the EEPROM power down instruction is decoded, the EEPROM block cannot be accessed unless a further Return instruction is decoded.

Deep Power Down. The M39208 can be set in the lowest I_{CC} consumption mode with the help of the Deep Power Down instruction (see Table 4). Once the instruction is decoded, the device is set in a sleep mode until a Reset instruction is decoded.

Power Up. The M39208 internal logic is reset upon a power-up condition to Read memory status. Any Write operation in EEPROM is inhibited during the first 5 ms following the power-up.

Either $\overline{EF}$, $\overline{EE}$ or $\overline{W}$ must be tied to V_{IH} during Power-up for the maximum security of the data contents and to remove the possibility of a byte being written on the first rising edge of $\overline{EF}$, $\overline{EE}$ or $\overline{W}$. Any write cycle initiation is locked when Vcc is below V_{LKO}.

READ

Read operations and instructions can be used to:

- read the contents of the Memory Array (Flash block and EEPROM block)
- read the Memory Array (Flash block and EEPROM block) status and identifiers.

Read data (Flash and EEPROM blocks)

Both Chip Enable $\overline{EF}$ (or $\overline{EE}$) and Output Enable ($\overline{G}$) must be low in order to read the data from the memory.

Read the Manufacturer Identifier

The manufacturer's identifier can be read with two methods: a Read operation or a Read instruction.

Read Operation. The manufacturer's identifier can be read with a Read operation with specific logic levels applied on A0, A1, A6 and the V_{ID} level (V_{ID} = 12V + 0.5V) on A9 (see Table 5).

Read Instruction. The manufacturer's identifier can also be read with a single instruction composed of 4 operations: 3 specific Write operations (see Table 4) and a Read which outputs the Manufacturer identifier, the Flash block identifier or the Flash sector protection status.

Read the Flash Block Identifier

The Flash block identifier can be read with two methods: a Read operation or a Read instruction.

Read Operation. The Flash block identifier (t.b.d.) can be read with a single Read operation with specific logic levels applied on A0, A1, A6 and the V_{ID} level on A9 (see Table 5).

Read Instruction. The Flash block identifier can also be read with an instruction composed of 4 operations: 3 specific Write operations and a Read (see Table 4).

Table 6. Status Bit

	$\overline{EF}$	$\overline{EE}$	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Flash	V_{IL}	V_{IH}	Data Polling	Toggle Flag	Error Flag	X	Erase Time-out	X	X	X
EEPROM	V_{IH}	V_{IL}	Data Polling	Toggle Flag	X	X	X	X	X	X

Note: X = Not guaranteed value, can be read either '1' or '0'.

Read the EEPROM Block Identifier

The EEPROM block identifier (64 bytes, user defined) can be read with a single Read operation with A6 = '0' and A9 = V_{ID} (see Table 5).

Read the OTP Row

The OTP row is mapped in the EEPROM block ($\overline{EE}$ = '0', $\overline{EF}$ = '1'). Read of the OTP row (64 bytes) is by an instruction (see Table 4) composed of three specific Write operations of data bytes at three specific memory locations (each location in a different page) before reading the OTP row content.

When accessing the OTP row, only the LSB addresses (A6 to A0) are decoded where A6 must be '0'.

Each Read of the OTP row has to be followed by the Return instruction (see Table 4).

Read the Flash Sector Protection Status

Reading the Flash sector protection status is by an instruction similar to the Read Manufacturer identifier instruction, the only difference being the value of the logic levels applied on A0, A1, A6, while A16 and A17 define the Flash sector whose protection has to be verified. Such a read instruction will output a 01h if the Flash sector is protected and a 00h if the Flash sector is not protected.

The Flash sector protection status can also be verified with a Read operation (see chapter: Flash block specific features), with V_{ID} on A9.

Read the Status Bits

The M39208 provides several Write operation status flags which may be used to minimize the application write (or erase or program) time. These signals are available on the I/O port bits when programming (or erasing) are in progress.

Data Polling flag, DQ7. When Erasing or Programming into the Flash block (or when Writing into the EEPROM block), bit DQ7 outputs the complement of the bit being entered for Programming/Writing on DQ7. Once the Program instruction or the Write operation is performed, the true logic value is read on DQ7 (in a Read operation).

Flash memory block specific features:

- Data Polling is effective after the fourth W pulse (for programming) or after the sixth W pulse (for Erase). It must be performed at the address being programmed or at an address within the Flash sector being erased.
- During an Erase instruction, DQ7 outputs a '0'. After completion of the instruction, DQ7 will output the last bit programmed (that is a '1' after erasing).
- if the byte to be programmed is in a protected Flash sector, the instruction is ignored.
- If all the Flash sectors to be erased are protected, DQ7 will be set to '0' for about 100µs, and then return to the previous addressed byte. No erasure will be performed.
- if all sectors are protected, a Bulk Erase instruction is ignored.

Toggle flag, DQ6. The M39208 also offers another way for determining when the EEPROM write or the Flash memory Program instruction is completed. During the internal Write operation, the DQ6 will toggle from '0' to '1' and '1' to '0' on subsequent attempts to read any byte of the memory, when either $\overline{G}$, $\overline{EE}$ or $\overline{EF}$ is low.

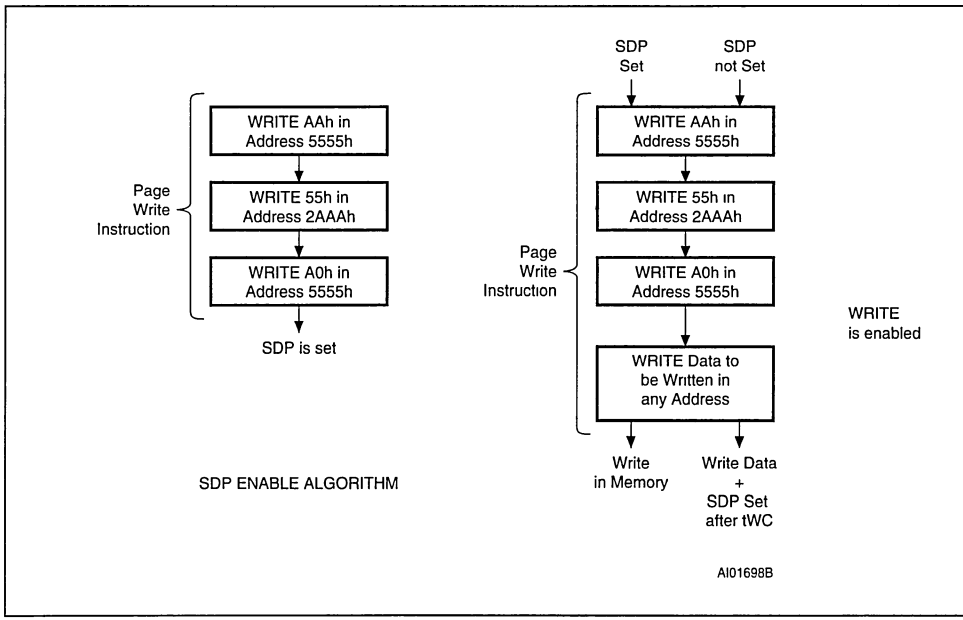
When the internal cycle is completed the toggling will stop and the data read on DQ0-DQ7 is the addressed memory byte. The device is now accessible for a new Read or Write operation. The operation is completed when two successive reads yield the same output data.

Flash memory block specific features:

a. the Toggle bit is effective after the fourth $\overline{W}$ pulse (for programming) or after the sixth $\overline{W}$ pulse (for Erase).

b. If the byte to be programmed belongs to a protected Flash sector, the instruction is ignored and:

Figure 4. EEPROM SDP Enable Flowcharts



– if all the Flash sectors selected for erasure are protected, DQ6 will toggle to '0' for about 100µs, and then return to the previous addressed byte.
– if all sectors are protected, the Bulk Erase instruction is ignored.

Error flag, DQ5 (Flash block only). This bit is set to '1' when there is a failure during either a Flash byte programming or a Sector erase or the Bulk Erase.

In case of error in Flash sector erase or byte program, the Flash sector in which the error occurred or to which the programmed byte belongs, must not be used any longer (other Flash sectors may still be used). The Error bit resets after Reset instruction.

During a correct Program or Erase, the Error bit will set to '0'.

Erase Time-out flag, DQ3 (Flash block only). The Erase Timer bit reflects the time-out period allowed between two consecutive Sector Erase instructions. The Erase timer bit is set to '0' after a Sector Erase instruction for a time period of 100µs ±20% unless an additional Sector Erase instruction is decoded. After this time period or when the additional Sector Erase instruction is decoded, DQ3 is set to '1'.

WRITE a BYTE (or a PAGE) in EEPROM

It should be noticed that writing in the EEPROM block is an operation, it is not an instruction (as for Programming a byte in the Flash block).

Write a Byte in EEPROM Block

A write operation is initiated when Chip Enable $\overline{EE}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Addresses are latched on the falling edge of $\overline{W}$, $\overline{EE}$ whichever occurs last.

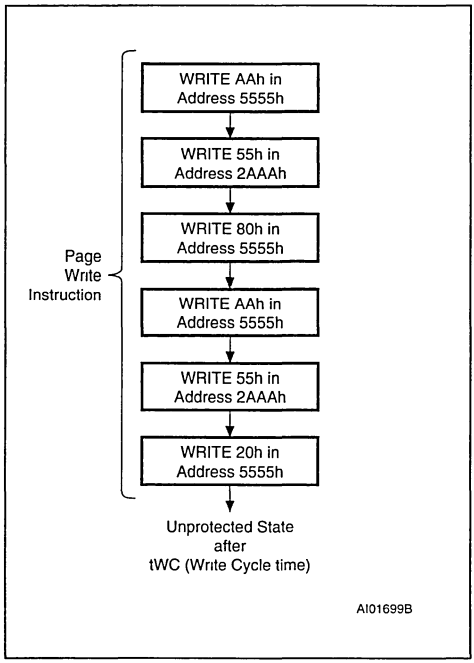
Once initiated, the write operation is internally timed until completion, that is during a time t_W.

The status of the write operation can be found by reading the Data Polling and Toggle bits (as detailed in the READ chapter) or the Ready/Busy output. This Ready/Busy output is driven low from the write of the byte being written until the completion of the internal Write sequence.

Table 7. Write the EEPROM Block Identifier

$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	A6	A9	Other Addresses	DQ0 - DQ7
V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	Don't Care	64 bytes User Defined

Figure 5. SDP disable Flowchart



Write a Page in EEPROM Block

The Page write allows up to 64 bytes within the same EEPROM page to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A6-A12 must be the same for all bytes. Once initiated, the Page write operation is internally timed until completion, that is during a time t_{WC}.

The status of the write operation can be seen by reading the Data Polling and Toggle bits (as detailed in the READ chapter).

A Page write is composed of successive Write instructions which must be sequenced within a time period (between two consecutive Write operations) that is smaller than the t_{WLWL} value. If this period of time exceeds the t_{WLWL} value, the internal programming cycle will start.

EEPROM Block Software Data Protection

A protection instruction allows the user to inhibit all write modes to the EEPROM block: the Software Data Protection (referenced as SDP in the following). The SDP feature is useful for protecting the EEPROM memory from inadvertent write cycles that may occur during uncontrolled bus conditions.

The M39208 is shipped as standard in the unprotected state meaning that the EEPROM memory contents can be changed by the user. After the SDP enable instruction, the device enters the Protect Mode where no further write operations have any effect on the EEPROM memory contents.

The device remains in this mode until a valid SDP disable instruction is received whereby the device reverts to the unprotected state.

To enable the Software Data Protection, the device has to be written (with a Page Write) with three specific data bytes at three specific memory locations (each location in a different page) as shown in Figure 4. This sequence provides an unlock key to enable the write action, and, at the same time, SDP continues to be set. Any further Write in EEPROM when the SDP is set will use this same sequence of three specific data bytes at three specific memory locations followed by the bytes to write. The first SDP enable sequence can be directly followed by the bytes to written.

Similarly, to disable the Software Data Protection the user has to write specific data bytes into six different locations with a Page Write addressing different bytes in different pages, as shown in Figure 5.

The Software Data Protection state is non-volatile and is not changed by power on/off sequences. The SDP enable/disable instructions set/reset an internal non-volatile bit and therefore will require a write time t_{WC}, This Write operation can be monitored only on the Toggle bit (status bit DQ6).

Figure 6. Data Polling Flowchart

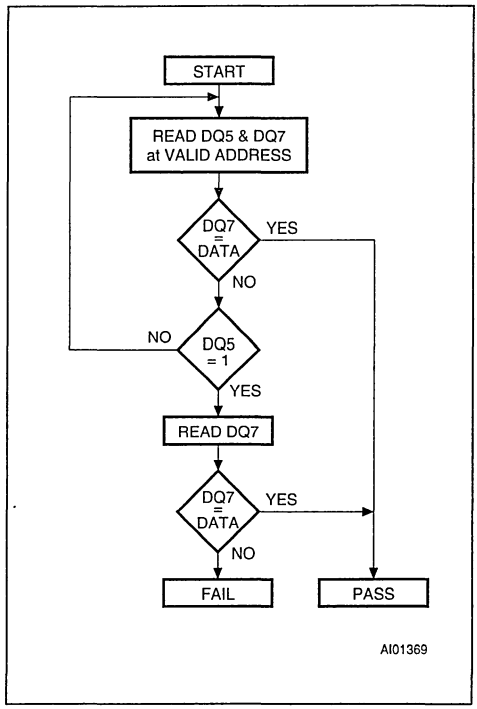
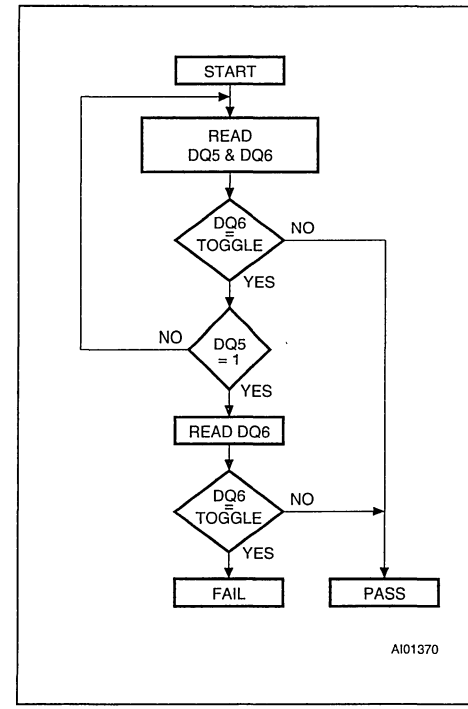


Figure 7. Data Toggle Flowchart



Write OTP Row

Writing (only one time) in the OTP row (64 bytes) is enabled by an instruction. This instruction is composed of three specific Write operations of data bytes at three specific memory locations (each location in a different page) followed by the the data to store in the OTP row (refer to Table 4).

When accessing the OTP row, the only LSB addresses (A6 to A0) are decoded, with A6 = '0'.

Write the EEPROM Block Identifier

The EEPROM block identifier can be written with a single Write operation with specific logic levels applied on A6 and the V_{ID} level on A9 (see Table 7).

PROGRAM in the Flash BLOCK

It should be noted that writing data into the EEPROM block and the Flash block is not performed in a similar way: the Flash memory requires an instruction (see Instruction chapter) for Erasing and another instruction for Programming one (or more) byte(s), the EEPROM memory is directly written with a simple operation (see Operation chapter).

Program Instuction. During the execution of the Program instruction, the Flash block memory will not accept any further instructions.

The Flash block memory can be programmed byte-by-byte. The program instruction is a sequence of three specific Write operations followed by writing the address and data byte to be programmed into the Flash block memory (see Table 4). The M39208 automatically starts and performs the programming after the fourth write operation.

During programming, the memory status may be checked by reading the status bits DQ5, DQ6 and DQ7, as detailed in the following sections.

Data Polling. Polling on DQ7 is a method of checking whether a Program or an Erase instruction is in progress or completed (see Figure 6). When a Program instruction is in progress, data bit DQ7 is the complement of the original data bit 7; when DQ7 is identical to the old data and the Error bit DQ5 is still '0', the instruction is complete. To determine if DQ7 is valid, each poll must store the original data for comparison, and if they are the same, it can be considered that the operation was successful. The Error bit DQ5 is checked to ensure timing limits have not exceeded.

When an Erase operation is in progress, DQ7 is always '0', and will be '1' when finished, so long as DQ5= '0'.

In all cases, when DQ5 is '1', DQ7 should be checked again, in case DQ7 changed simultaneously with DQ5. If DQ7 = true data (Program) or DQ7 = '1' (Erase), the operation is successful and execution should return to the caller. A suggested second read will provide all true data (Program) or all FFh (Erase). Otherwise, this should be flagged as an error, and the device should be Reset.

Data Toggle. Checking the Toggle bit DQ6 is an alternative method of checking if Program or Erase operations are in progress or completed (see Figure 7). When an operation is in progress, data bit DQ6 constantly toggles for successive read operations. When DQ6 no longer toggles and the Error bit DQ5 is '0', the operation is completed. To determine if DQ6 has toggled, each polling action requires 2 consecutive read operations of the data, and if the data read is the same, it can be considered that the operation was successful. The Error bit DQ5 is checked to ensure timing limits have not been exceeded. In all cases, when DQ5 is '1', DQ6 should be checked again, in case DQ6 has changed simultaneously with DQ5. If DQ6 has stopped toggling, the operation is successful and execution should return to the caller. A suggested second read will provide all true data (Program) or all FFh (Erase). Otherwise, this event should be flagged as an error, and the device should be Reset.

ERASE in the Flash BLOCK

It should be noted that:

a. Programming any byte of one Flash sector (or bulk) requires that the Flash sector (or bulk) has been previously erased (once for all bytes within the sector or bulk) with the correct instruction (see Instructions chapter).

b. Writing in the EEPROM memory is an operation triggering an automatic sequencing of byte erase followed by a byte write. Writing in EEPROM does not require a specific erase operation before writing.

Bulk Erase Instruction. The Bulk Erase instruction uses six write operations followed by Read operations of the status register bits, as described in Table 4. If any byte of the Bulk Erase instruction is wrong, the Bulk Erase instruction aborts and the device is reset to the Read Flash memory status.

During a Bulk Erase, the memory status may checked by reading the status bits DQ5, DQ6 and DQ7, as detailed in the "PROGRAM in the Flash BLOCK" chapter. The Error bit (DQ5) returns a '1' if there has been an Erase Failure (maximum number of erase cycles have been executed).

It is not necessary to program the array with 00h, the M39208 will automatically do this before erasing to FFh.

During the execution of the Bulk Erase instruction, the Flash block logic does not accept any instruction.

Sector Erase in Flash Block. The Sector Erase instruction uses six write operations, as described in Table 4. Additional Flash Sector Erase confirm commands and Flash sector addresses can written subsequently to erase other Flash sectors in parallel, without further coded cycles, if the additional instruction is transmited in a shorter time than the timeout period to end of period. The input of a new Sector Erase instruction will restart the time-out period.

The status of the internal timer can be monitored through the level of DQ3 (Erase time-out bit), if DQ3 is '0' the Sector Erase instruction has been received and the timeout is counting; if DQ3 is '1', the timeout has expired and the M39208 is erasing the Flash sector(s). Before and during Erase timeout, any instruction different than Erase suspend and Erase Resume will abort the instruction and reset the device to read array mode.
It is not necessary to program the Flash sector with 00h as the M39208 will do this automatically before erasing (byte = FFh).

During a Sector Erase, the memory status may be checked by reading the status bits DQ5, DQ6 and DQ7, as detailed in the "Program instruction" chapter. During the execution of the erase instruction, the Flash block logic accepts only the Reset and Erase Suspend instructions (erasure of one Flash sector may be suspended, in order to read data from another Flash sector, and then resumed).

Table 8. Flash Sector Protection

$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A9	A12	A16	A17	DQ0 - DQ7
V_{IL}	V_{IH}	V_{ID}	V_{IL}	X	X	X	V_{ID}	X	SA	SA	Protection Activation
V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{ID}	X	SA	SA	Verify the protection status: when DQ0= 1, the sector is protected

Notes: X = Don't care.
SA = Software Address.

Table 9. Flash Unprotection

$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A9	A12	A15	A16	A17	DQ0 - DQ7
V_{ID}	V_{IH}	V_{ID}	V_{IL}	X	X	X	V_{ID}	V_{IH}	V_{IH}	X	X	Activation of Unprotected Mode
V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	X	X	SA	SA	Verify the protection status: when 00h, the sector is unprotected

Notes: X = Don't care.
SA = Software Address.

Erase Suspend Instruction. When a Flash Sector Erase operation is in progress, the Erase Suspend instruction may suspend the operation by writing B0h at any address (see Table 4). This allows reading of data from another Flash sector while erase is in progress. Erase suspend is accepted only during the Flash Sector Erase instruction execution and defaults to read array mode. An Erase Suspend instruction entered during an Erase timeout will, in addition to suspending the erase, terminates the timeout.

The Toggle bit DQ6 stops toggling when the M39208 internal logic is suspended. The Toggle bit status must be monitored at an address out of the Flash sector being erased. Toggle bit will stop toggling between 0.1µs and 15µs after the Erase Suspend instruction has been written. The M39208 will then automatically be set into Read Flash Block Memory Array mode.

When erase is suspended, Reading from Flash sectors being erased will output invalid data, a Read from Flash sector not being erased is valid. During an Erase Suspend, the Flash memory will respond only to Erase Resume and Reset instructions.

A Reset instruction will definitively abort erasure and can leave invalid data in the Flash sectors being erased.

Erase Resume Instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by this instruction. The Erase Resume instruction consists of writing 30h at any address (see Table 4).

FLASH BLOCK SPECIFIC FEATURES

Flash Sector Protection. Each Flash sector can be separately protected against Program or Erase. Flash Sector Protection provides additional data security, as it disables all program or erase operations. This mode is activated when both A9 and $\overline{G}$ are set to V_{ID} (12V + 0.5V) and the Flash sector address is applied on A16 and A17, as shown in Figure 8 and Table 8.

Flash sector protection is programmed with the help of a specific sequence of levels applied on $\overline{EF}$, $\overline{EE}$, $\overline{G}$, A0, A1, A6, A9, A16 and A17; this sequence includes a verification of the Protection status on DQ0 as shown in Table 8.

Any attempt to program or erase a protected Flash sector will be ignored by the device.

Remarks:

- The Verify operation is a read with a simulated worst case conditions. This allows a guarantee of the retention of the Protection status
- During the application life, the Sector protection status can be accessed with a regular Read instruction without applying a "high voltage" V_{ID} on A9. This instruction is detailed in Table 4.

Figure 8. Sector Protection Flowchart

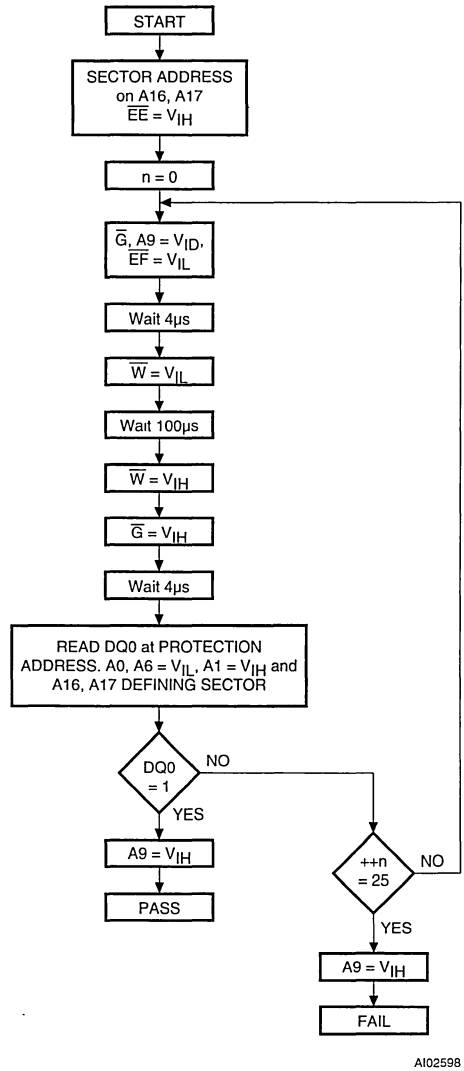
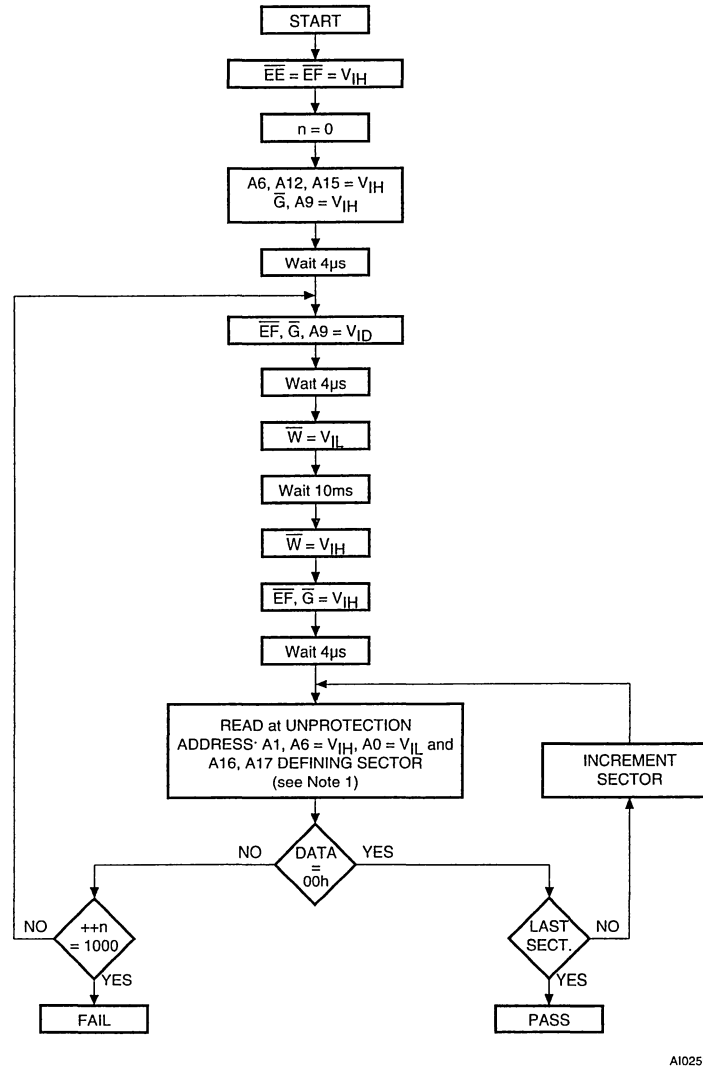


Figure 9. Sector Unprotecting Flowchart



Note: 1 A6 is kept at V_{IH} during unprotection algorithm in order to secure best unprotection verification. During all other protection status reads, A6 must be kept at V_{IL}.

Table 10. AC Measurement Conditions

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input Timing Ref. Voltages	0.8V and 2V
Output Timing Ref. Voltages	1.5V

Figure 10. AC Testing Input Output Waveform

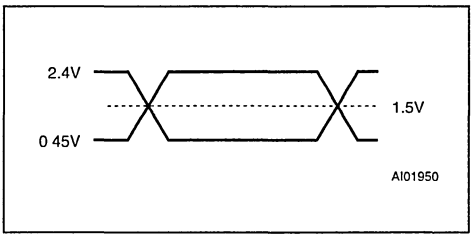


Figure 11. Output AC Testing Load Circuit

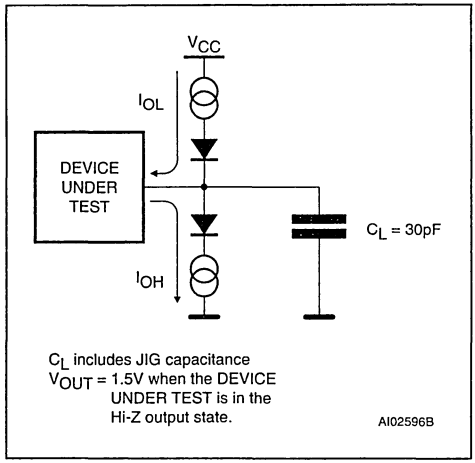


Table 11. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested

Flash Sector Unprotection. Flash sectors can be unprotected to allow updating of their contents. Note that the Sector Unprotection unprotects all sectors (sector 0 up to sector 7).

Flash Sector Unprotection is activated with a specific sequence of levels applied on $\overline{EF}$, $\overline{EE}$, $\overline{G}$, A0, A1, A6, A9, A12 and A15; this sequence includes a verification of the Protection status on DQ0-DQ7 as shown in Figure 9 and Table 9.

This allows a guarantee of the retention of the Protection status.

Remarks:

– The Verify operation is a read with a simulated worst case conditions. This allows a guarantee of the retention of the Protection status

– During the application life, the Sector protection status can be accessed with a regular Read instruction without "high voltage" V_{ID} on A9. This instruction is detailed in Table 4.

Reset Instruction. The Reset instruction resets the device internal logic in a few µs. Reset is an instruction of either one write operation or three write operations (refer to Table 4).

Supply Rails. Normal precautions must be taken for supply voltage decoupling, each device in a system should have the V_{CC} rail decoupled with a 0.1µF capacitor close to the V_{CC} and V_{SS} pins. The printed circuit board trace width should be sufficient to carry the V_{CC} program and erase currents required.

Table 12. DC Characteristics
(T_A = 0 to 70°C or –20 to 85°C or –40 to 85°C; V_{CC} = 2.7 V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC1} (1)	Supply Current (Read Flash) TTL	$\overline{EE} = V_{IH}$, $\overline{EF} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz		15	mA
I_{CC2}	Supply Current (Read EEPROM) TTL	$\overline{EE} = V_{IL}$, $\overline{EF} = V_{IH}$, $\overline{G} = V_{IH}$, f = 6MHz		15	mA
I_{CC3}	Supply Current (Standby) CMOS	$\overline{EF} = \overline{EE} = V_{CC} \pm 0.2V$		60	µA
I_{CC4}	Supply Current (Flash Block Program or Erase)	Byte program, Sector or Chip Erase in progress		20	mA
I_{CC5}	Supply Current (EEPROM Write)	During t_{WC}		20	mA
I_{CC6}	Supply Current in Deep Power Down Mode	After a Deep Power Down instruction (see Table 4)		2	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}	VCC + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.8mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{CC} –0.4		V
V_{ID}	A9 High Voltage		11.5	12.5	V
I_{ID}	V_{ID} Current	A9 = V_{ID}		100	µA
V_{LKO}	V_{CC} Minimum for Write, Erase and Program		2	2.3	V

Note: 1. When reading the Flash block when an EEPROM byte(s) is under a write cycle, the supply current is $I_{CC1} + I_{CC5}$

GLOSSARY

Block: EEPROM block (64 Kbit) or Flash block (2 Mbit)

Bulk: the whole Flash block (2 Mbit)

Sector: 64 Kbyte of Flash memory

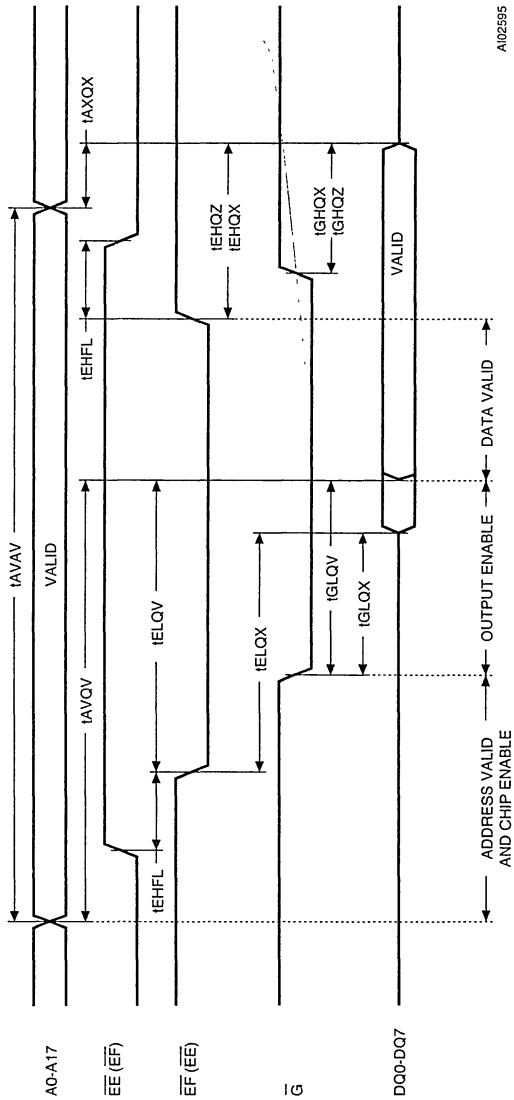
Page: 64 bytes of EEPROM

Write and Program: Writing (into the EEPROM block) and programming (the Flash block) is not performed in a similar way:

- the Flash memory requires an instruction (see Instruction chapter) for Erasing and another instruction for Programming one (or more) byte(s)
- the EEPROM memory is directly written with a simple operation (see Operation chapter).

SDP: Software Data Protection. Used for protecting the EEPROM block against false Write operations (as in noisy environments).

Figure 12. Read Mode AC Waveforms



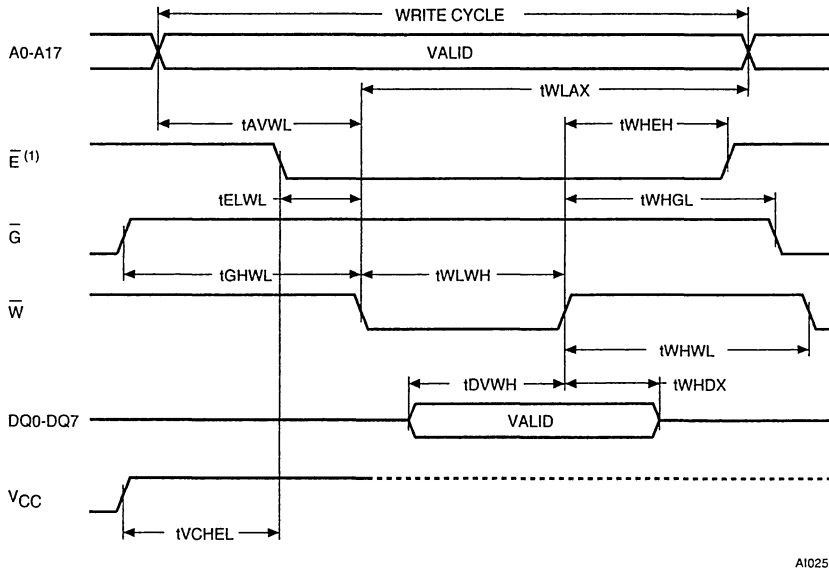
Note: Write Enable ($\overline{W}$) = High

Table 13. Read AC Characteristics
(T_A = 0 to 70°C or –20 to 85°C or –40 to 85°C; V_{CC} = 2.7 V to 3.6V)

Symbol	Alt	Parameter	Test Condition	M39208						Unit
				-100		-120		-150		
				Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(\overline{EE}, \overline{EF}) = (V_{IH}, V_{IL})$, $\overline{G} = V_{IL}$	100		120		150		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(\overline{EE}, \overline{EF}) = (V_{IH}, V_{IL})$, $\overline{G} = V_{IL}$		100		120		150	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	0		0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		100		120		150	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(\overline{EE}, \overline{EF}) = (V_{IH}, V_{IL})$	0		0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(\overline{EE}, \overline{EF}) = (V_{IH}, V_{IL})$		40		55		55	ns
t_{EHQX}	t_{OH}	Chip Enable High to Output Transition	$\overline{G} = V_{IL}$	0		0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$		30		40		40	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(\overline{EE}, \overline{EF}) = (V_{IH}, V_{IL})$	0		0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(\overline{EE}, \overline{EF}) = (V_{IH}, V_{IL})$		30		40		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(\overline{EE}, \overline{EF}) = (V_{IH}, V_{IL})$, $\overline{G} = V_{IL}$	0		0		0		ns
t_{EHFL}	t_{CED}	$\overline{EE}$ ($\overline{EF}$) Active to $\overline{EF}$ ($\overline{EE}$)		100		100		100		ns

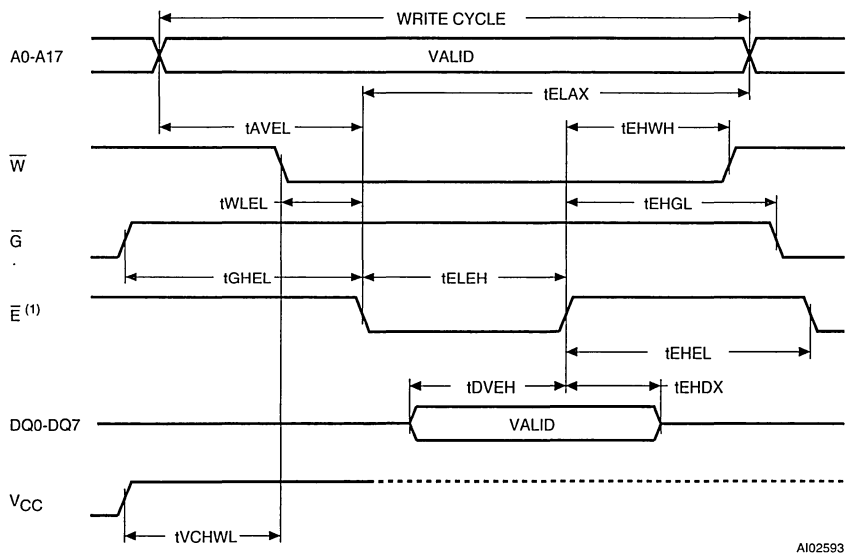
Notes: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to $t_{ELQV} - t_{GLQV}$ after the falling edge of $\overline{EE}$ (or $\overline{EF}$) without increasing t_{ELQV}.

Figure 13. Write AC Waveforms, $\overline{W}$ Controlled



Notes: Address are latched on the falling edge of $\overline{W}$, Data is latched on the rising edge of $\overline{W}$.
$\overline{E}$ is either $\overline{EF}$ when $\overline{EE}$ = V_{IH} or $\overline{EE}$ when $\overline{EF}$ = V_{IH}.

Figure 14. Write AC Waveforms, $\overline{E}$ Controlled



Notes: Address are latched on the falling edge of $\overline{E}$, Data is latched on the rising edge of $\overline{E}$.
$\overline{E}$ is either $\overline{EF}$ when $\overline{EE} = V_{IH}$ or $\overline{EE}$ when $\overline{EF} = V_{IH}$

Table 14. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C or –20 to 85°C or –40 to 85°C; V_{CC} = 2.7 V to 3.6V)

Symbol	Alt	Parameter	M39208						Unit
			-100		-120		-150		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	100		120		150		ns
t_{ELWL} (2)	t_{CS}	Chip Enable Low to Write Enable Low	0		0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		50		65		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		65		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		0		ns
t_{WHEH} (2)	t_{CH}	Write Enable High to Chip Enable High	0		0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		30		35		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	50		50		65		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		0		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		50		µs
t_{WHQV1} (1)		Write Enable High to Output Valid (Program)	8		8		8		µs
t_{WHQV2} (1)		Write Enable High to Output Valid (Sector Erase)	0.5	30	0.5	30	0.5	30	sec
t_{WHWL0}		Time Out between 2 consecutive Section Erase		80		80		80	µs
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		0		ns

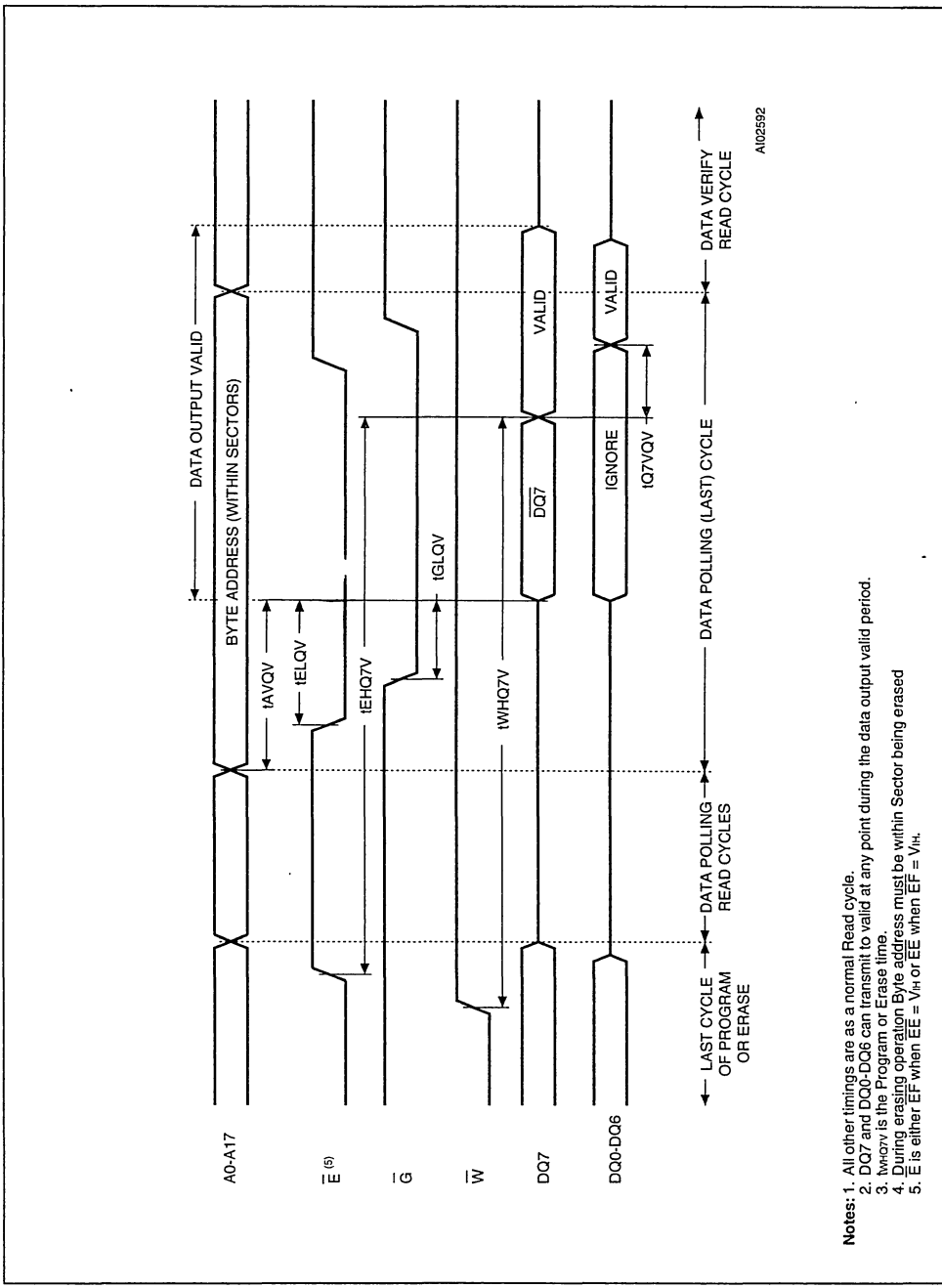
Notes: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$
2. Chip Enable means $(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(\overline{EE}, \overline{EF}) = (V_{IH}, V_{IL})$.

Table 15. Write AC Characteristics, $\overline{E}$ or $\overline{EF}$ Controlled
(T_A = 0 to 70°C or –20 to 85°C or –40 to 85°C; V_{CC} = 2.7 V to 3.6V)

Symbol	Alt	Parameter	M39208						Unit
			-100		-120		-150		
			Min	Max	Min	Max	Min	Max	
t_{WLWL}	t_{BLC}	Time-out after the Last Byte Write	150		150		150		µs
t_{WC}		Write Cycle Time (EEPROM)		10		10		10	ms
t_{AVAV}		Address Valid to Next Address Valid	100		120		150		ns
t_{WLEL}	t_{WS}	Write Enable Low to Memory Block Enable Low	0		0		0		ns
t_{ELEH}	t_{CP}	Memory Block Enable Low to Memory Block Enable High	50		50		65		ns
t_{DVEH}	t_{DS}	Input Valid to Memory Block Enable High	50		50		65		ns
t_{EHDX}	t_{DH}	Memory Block Enable High to Input Transition	0		0		0		ns
t_{EHWH}	t_{WH}	Memory Block Enable High to Write Enable High	0		0		0		ns
t_{EHEL}	t_{CPH}	Memory Block Enable High to Memory Block Enable Low	30		30		35		ns
t_{AVEL}	t_{AS}	Address Valid to Memory Block Enable Low	0		0		0		ns
t_{ELAX}	t_{AH}	Memory Block Enable Low to Address Transition	50		50		65		ns
t_{GHEL}		Output Enable High to Memory Block Enable Low	0		0		0		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		50		µs
t_{EHQV1} (1)		Memory Block Enable High to Output Valid (Program)	8		8		8		µs
t_{EHQV2} (1)		Memory Block Enable High to Output Valid (Sector Erase)	0.5	30	0.5	30	0.5	30	sec
t_{EHGL}	t_{OEH}	Memory Block Enable High to Output Enable Low	0		0		0		ns

Notes: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$.

Figure 15. Data Polling DQ7 AC Waveforms



Notes: 1. All other timings are as a normal Read cycle.
2. DQ7 and DQ0-DQ6 can transmit to valid at any point during the data output valid period.
3. t_{WHQ7V} is the Program or Erase time.
4. During erasing operation Byte address must be within Sector being erased
5. $\overline{E}$ is either $\overline{EF}$ when $\overline{EE} = V_{IH}$ or $\overline{EE}$ when $\overline{EF} = V_{IH}$.

Table 16. Data Polling and Toggle Bit AC Characteristics (1)
(T_A = 0 to 70°C or –20 to 85°C or –40 to 85°C; V_{CC} = 2.7 V to 3.6V)

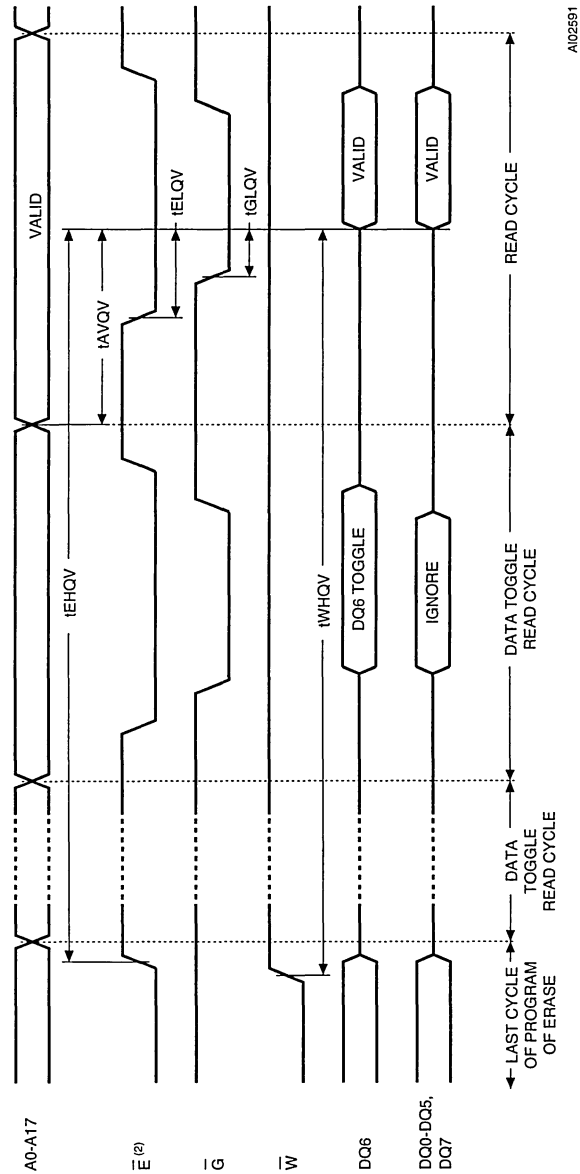
Symbol	Test Conditions	Parameter	M39208						Unit
			-100		-120		-150		
			Min	Max	Min	Max	Min	Max	
t_{WHQ7V1}	$\overline{EF}$ = 0 $\overline{EE}$ = 1	Write Enable High to DQ7 Valid (Program, $\overline{W}$ Controlled)	10		10		10		µs
t_{WHQ7V2}	$\overline{EF}$ = 0 $\overline{EE}$ = 1	Write Enable High to DQ7 Valid (Sector Erase, $\overline{W}$ Controlled)	1.5	30	1.5	30	1.5	30	sec
t_{EHQ7V1}	$\overline{EF}$ = 0 $\overline{EE}$ = 1	Flash Block Enable High to DQ7 Valid (Program, $\overline{EF}$ Controlled)	10		10		10		µs
t_{EHQ7V2}	$\overline{EF}$ = 0 $\overline{EE}$ = 1	Flash Block Enable High to DQ7 Valid (Sector Erase, $\overline{EF}$ Controlled)	1.5	30	1.5	30	1.5	30	sec
t_{Q7VQV}	$\overline{EF}$ = 0 $\overline{EE}$ = 1	Q7 Valid to Output Valid (Data Polling)		40		50		55	ns

Notes: 1. All other timings are defined in Read AC Characteristics table.

Table 17. Program, Erase Times and Program, Erase Endurance Cycles (Flash Block)
(T_A = 0 to 70°C or –20 to 85°C or –40 to 85°C; V_{CC} = 2.7 V to 3.6V)

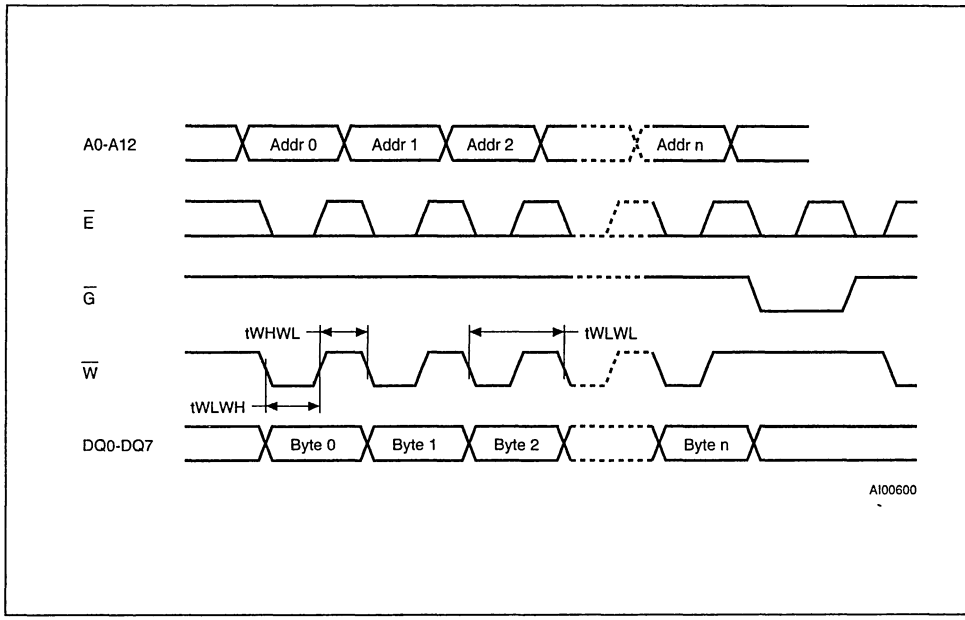
Parameter	M39208			Unit
	Min	Typ	Max	
Chip Program (Byte)		8		sec
Chip Erase (Preprogrammed)		3	30	sec
Chip Erase		10		sec
Sector Erase (Preprogrammed)		1	30	sec
Sector Erase		2		sec
Byte Program		10		µs
Program/Erase Cycles (per Sector)	100,000			cycles

Figure 16. Data Toggle DQ6 AC Waveforms

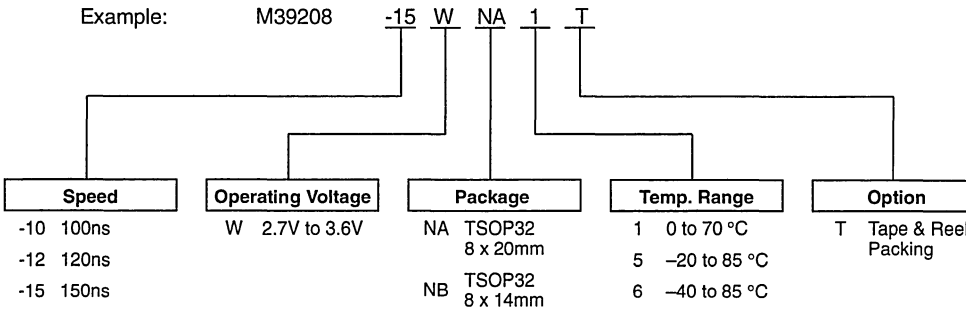


Notes: 1. All other timings are as a normal Read cycle.
2. $\overline{E}$ is either $\overline{EF}$ when $\overline{EE}$ = V_{IH} or $\overline{EE}$ when $\overline{EF}$ = V_{IH}

Figure 17. EEPROM Page Write Mode AC Waveforms, $\overline{W}$ Controlled



ORDERING INFORMATION SCHEME

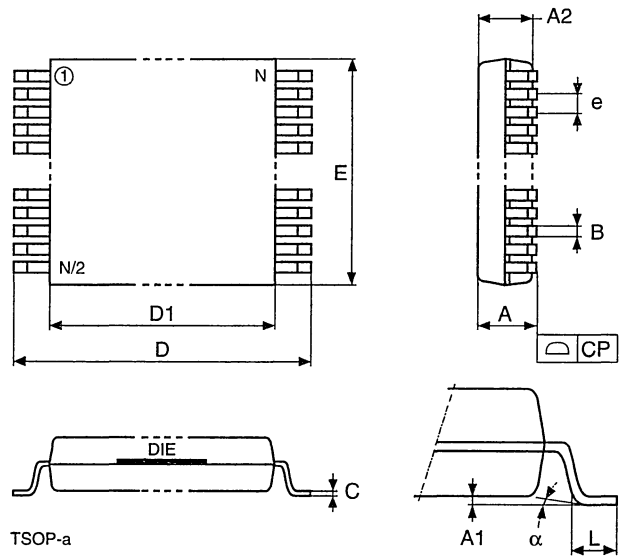


Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 14mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		13.80	14.20		0.543	0.559
D1		12.30	12.50		0.484	0.492
E		7.90	8.10		0.311	0.319
e	0.50	-	-	0.020	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N		32			32	
CP			0.10			0.004

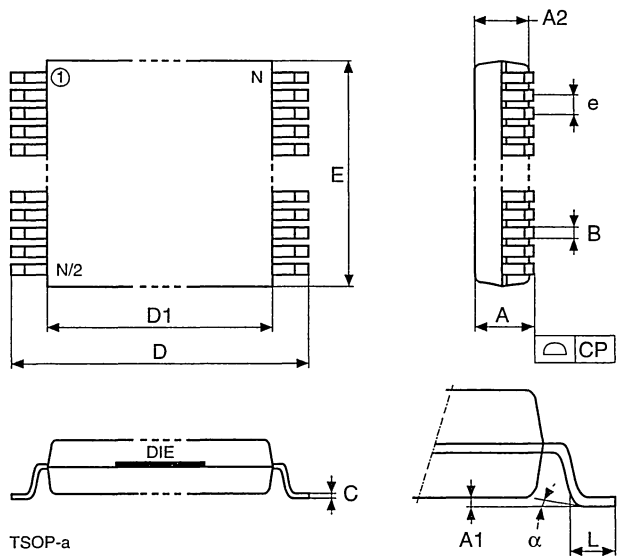


TSOP-a

Drawing is not to scale.

TSOP32 - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.007
A2		0.95	1.05		0.037	0.041
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	-	-	0.020	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	32			32		
CP			0.10			0.004



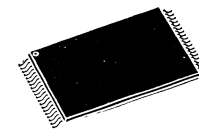
TSOP-a

Drawing is not to scale.

M39432

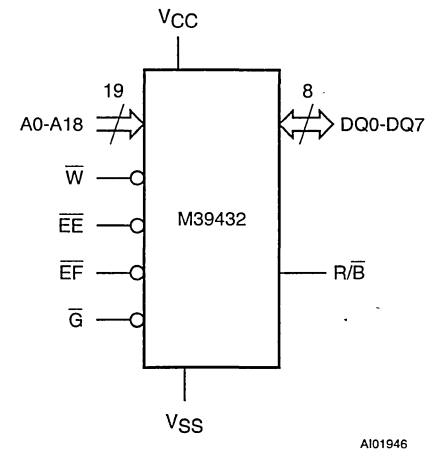
Single Chip 4 Mbit Flash and 256 Kbit Parallel EEPROM Memory

- 3.3V±10% SUPPLY VOLTAGE for PROGRAM, ERASE and READ OPARATIONS
- 120ns ACCESS TIME (Flash and EEPROM blocks)
- WRITE, PROGRAM and ERASE STATUS BITS
- CONCURRENT MODE (Read Flash while writing to EEPROM)
- 100,000 ERASE/WRITE CYCLES
- 10 YEARS DATA RETENTION
- LOW POWER CONSUMPTION
  - Stand-by mode: 40µA
  - Automatic Stand-by mode
  - Deep Power Down mode
- 64 bytes ONE TIME PROGRAMMABLE MEMORY
- STANDARD EPROM/OTP MEMORY PACKAGE
- EXTENDED TEMPERATURE RANGES



TSOP40 (NC)
10 x 20 mm

Figure 1. Logic Diagram



DESCRIPTION

The M39432 is a memory device combining Flash and EEPROM into a single chip and using single supply voltage. The memory is mapped in two blocks: 4 Mbit of Flash memory and 256 Kbit of EEPROM memory. Each space is independant for writing, in concurrent mode the Flash Memory can be read while the EEPROM is being written.

Table 1. Signal Names

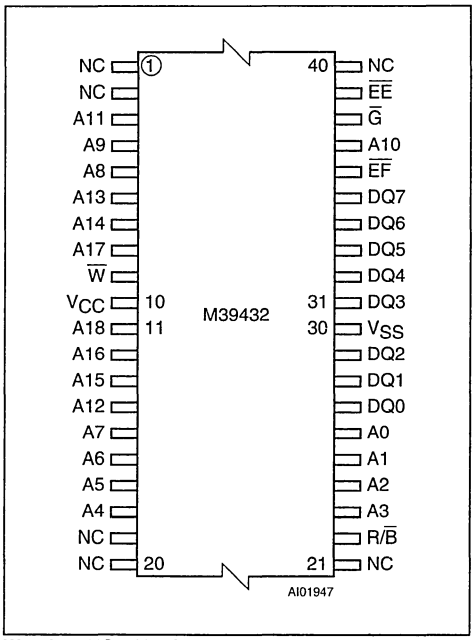
A0-A18	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{E}$	EEPROM Block Enable
$\overline{EF}$	Flash Block Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
R/$\overline{B}$	Ready/Busy Output
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 85	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages	–0.6 to 7	V
V_{CC}	Supply Voltage	–0.6 to 7	V
V_{A9}, V_G, V_{EF} (2)	A9, $\overline{G}$, $\overline{EF}$ Voltage	–0.6 to 13.5	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.

Figure 2. TSOP Pin Connections



Warning: NC = Not Connected.

DESCRIPTION (Cont'd)

An additional 64 bytes of EPROM are One Time Programmable.

The M39432 EEPROM array may be written by byte or by page of 64 bytes and the integrity of the data can be secured with the help of the Software Data Protection (SDP).

The M39432 Flash Memory array offers 8 blocks of 64 Kbytes, each sector may be erased individually, and programmed Byte-by-Byte. Each block can be separately protected and unprotected against program and erase. Block erasure may be suspended, while data is read from other blocks of the Flash array (or EEPROM memory block), and then resumed. The Flash array is functionally compatible with the M29W040 4 Mbit Single Voltage Flash Memory.

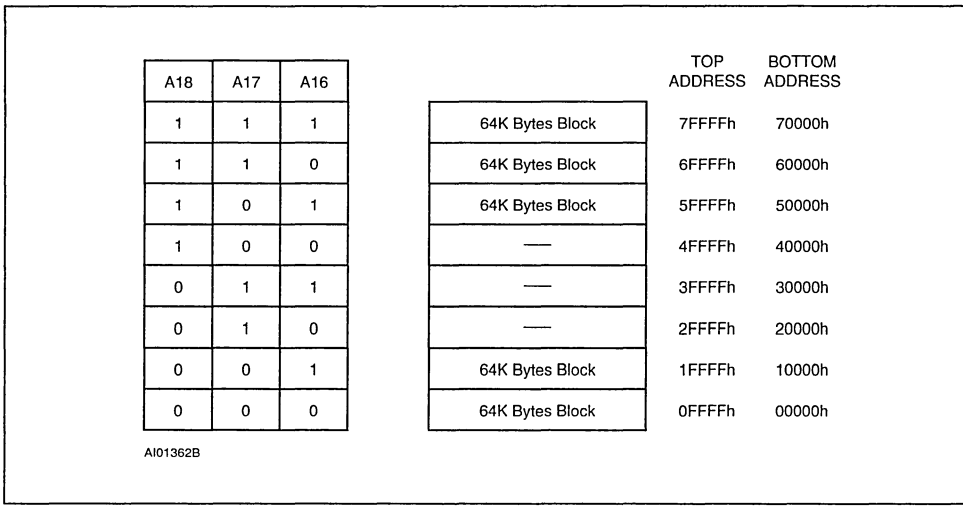
During a Program or Erase cycle in the Flash array or during a Write in the EEPROM memory block, the status of the M39432 internal logic can be read on the Data Outputs DQ7,DQ6, DQ5 and DQ3.

PIN DESCRIPTION

Address Inputs (A0-A18). The address inputs for the memory array are latched during a write operation. A0-A14 access locations in the EEPROM memory block A0-A18 access locations in the Flash memory block. The memory block selected is given by the state on the $\overline{EE}$ and $\overline{EF}$ inputs respectively.

When a specific voltage (V_{ID}) is applied on the A9 address input, additional specific areas can be accessed: Read the Manufacturer identifier, Read the Flash block identifier, Read/Write the EEPROM block identifier, Verify the Flash Block Protection Status.

Figure 3. Flash Memory Map and Block Address Table



A18	A17	A16		TOP ADDRESS	BOTTOM ADDRESS
1	1	1	64K Bytes Block	7FFFFh	70000h
1	1	0	64K Bytes Block	6FFFFh	60000h
1	0	1	64K Bytes Block	5FFFFh	50000h
1	0	0	—	4FFFFh	40000h
0	1	1	—	3FFFFh	30000h
0	1	0	—	2FFFFh	20000h
0	0	1	64K Bytes Block	1FFFFh	10000h
0	0	0	64K Bytes Block	0FFFFh	00000h

AI01362B

Data Input/Output (DQ0-DQ7). A write operation inputs one byte which is latched when $\overline{EE}$ (or $\overline{EF}$) and Write Enable $\overline{W}$ are driven active.

Data read is valid when one Chip Enable (Chip Enable Flash or Chip Enable EEPROM) and Output Enable are driven active. The output is high impedance when the chip is deselected (both $\overline{EE}$ and $\overline{EF}$ driven high) or the outputs are disabled ($\overline{G}$ driven high).

Read operations are used to output the contents from the memory, the Manufacturer identifier, the Flash Sector protection Status, the Flash block Identifier, the EEPROM identifier or the OTP row content.

Memory Block Enable ($\overline{EE}$ and $\overline{EF}$). The Memory Block Enable ($\overline{EE}$ or $\overline{EF}$) activates the memory control logic, input buffers, decoders and sense amplifiers. When the $\overline{EE}$ input is driven high, the EEPROM memory block is not selected; when the $\overline{EF}$ input is driven high, the Flash memory block is not selected. Attempts to access both EEPROM and Flash blocks ($\overline{EE}$ low and $\overline{EF}$ low) are forbidden. Switching between the two memory block enables ($\overline{EE}$ and $\overline{EF}$) must not be made on the same clock cycle, a delay of greater than t_{EHFL} must be inserted.

The M39432 is in standby when both $\overline{EF}$ and $\overline{EE}$ are High (when no internal Erase or programming is running). The power consumption is reduced to the standby level and the outputs are in the high impedance state, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

After 150ns of inactivity and when the addresses are driven at CMOS levels, the chip automatically enters a pseudo standby mode where consumption is reduced to the CMOS standby value, while the outputs continue to drive the bus.

Output Enable ($\overline{G}$). The Output Enable gates the outputs through the data buffers during a read operation. The data outputs are in the high impedance state when the Output Enable $\overline{G}$ is High.

During Sector Protect and Sector Unprotect operations, the $\overline{G}$ input must be forced to V_{ID} level (12V + 0.5V) (for Flash memory block only).

Write Enable ($\overline{W}$). Addresses are latched on the falling edge of $\overline{W}$, and Data Inputs are latched on the rising edge of $\overline{W}$.

Ready/Busy (R/$\overline{B}$). The Ready/Busy pin outputs the status of the device when the EEPROM memory block is under the write condition

- R/$\overline{B}$ = '0': internal writing is in process,
- R/$\overline{B}$ = '1': no internal writing in in process.

It should be noted that the Ready/Busy pin does not reflect the status of Programming/Erasing in the Flash memory.

This status bit can be used when reading (or fetching opcodes) in the Flash memory block.

The Ready/Busy output uses an open drain transistor, allowing therefore the use of the M39432 in multi-memory applications with all Ready/Busy outputs connected to a single Ready/Busy line (OR-wired with an external pull-up resistor).

Table 3. Basic Operations

Operation	$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Read in Flash Block
	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Read in EEPROM Block
Write	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Write in Flash Block
	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Write in EEPROM Block
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	Hi-Z
	V_{IH}	V_{IL}	V_{IH}	X	Hi-Z
Standby	V_{IH}	V_{IH}	X	X	Hi-Z

Note: X = V_{IL} or V_{IH}.

OPERATIONS

The M39432 memory is addressed through 19 inputs A0-A18 and provides data on eight Data Inputs/Outputs DQ0-DQ7 with the help of four control lines: Chip Enable EEPROM ($\overline{EE}$), Chip Enable Flash ($\overline{EF}$), Output Enable ($\overline{E}$) and Write Enable ($\overline{W}$) inputs.

An operation is defined as the basic decoding of the logic level applied to the control input pins ($\overline{EF}$, $\overline{EE}$, $\overline{G}$, $\overline{W}$) and the specified voltages applied on the relevant address pins. These operations are detailed in Table 3.

Read. Both Chip Enable and Output Enable (that is $\overline{EF}$ and $\overline{G}$ or $\overline{EE}$ and $\overline{G}$) must be low in order to read the output of the memory.

Read operations are used to output the contents from the Flash or EEPROM block, the Manufacturer identifier, the Flash Sector protection Status, the Flash block Identifier, the EEPROM identifier or the OTP row content.

Notes:

- The Chip Enable input mainly provides power control and should be used for device selection. The Output Enable input should be used to gate data onto the output in combination with active $\overline{EF}$ or $\overline{EE}$ input signals.
- The data read depends on the previous instruction entered into the memory (see Table 4).

Write. A Write operation can be used for two goals:

- either write data in the EEPROM memory block
- or enter a sequence of bytes composing an instruction.

The reader should note that Programming a Flash byte is an instruction (see Instructions paragraph).

Writing data requires:

- the Chip Enable (either $\overline{EE}$ or $\overline{EF}$) to be Low
- the Write Enable ($\overline{W}$) to be Low with Output Enable (G) High.

Addresses in Flash block (or EEPROM block) are latched on the falling edge of $\overline{W}$ or $\overline{EF}$ ($\overline{EE}$) whichever occurs last; the data to be written in Flash block (EEPROM block) is latched on the rising edge of $\overline{W}$ or $\overline{EF}$ ($\overline{EE}$) whichever occurs first.

Specific Read and Write Operations. Device specific data is accessed through operations decoding the V_{ID} level applied on A9 (V_{ID} = 12V + 0.5V) and the logic levels applied on address inputs (A0, A1, A6). These specific operations are:

- Read the Manufacturer identifier
- Read the Device identifier
- Define the Flash Sector protection
- Read the EEPROM identifier
- Write the EEPROM identifier

Note: The OTP row (64 bytes) is accessed with a specific software sequence detailed in the paragraph "Write in OTP row".

Instructions

An instruction is defined as a sequence of specific Write operations. Each received byte is sequentially decoded (and not executed as standard Write operations) and the instruction is executed when the correct number of bytes are properly received and the time between two consecutive bytes is shorter than the time-out value.

The sequencing of any instruction must be followed exactly, any invalid combination of instruction bytes or time-out between two consecutive bytes will reset the device logic into a Read memory state (when addressing the Flash block) or directly decoded as a single operation when addressing the EEPROM block.

Table 4. Instructions (1)

Instruction	$\overline{EE}$	$\overline{EF}$	Cycle 1	Cycle 2	Cycle 3	Cycle 4	Cycle 5	Cycle 6	Cycle 7
Read Manufacturer Identifier (2)	1	0	AAh @5555h	55h @2AAAh	90h @5555h	Read Identifier with (A0,A1,A6) at (0,0,0)			
Read Flash Identifier (2)	1	0	AAh @5555h	55h @2AAAh	90h @5555h	Read identifier with (A0,A1,A6) at (1,0,0)			
Read OTP Row	0	1	AAh @5555h	55h @2AAAh	90h @5555h	Read byte 1	Read byte 2		Read byte N
Read Block Protection Status (2)	1	0	AAh @5555h	55h @2AAAh	90h @5555h	Read Identifier with (A0,A1,A6) at (0,1,0)			
Program a Flash Byte	1	0	AAh @5555h	55h @2AAAh	A0h @5555h	Data @address			
Erase one Flash Block	1	0	AAh @5555h	55h @2AAAh	80h @5555h	AAh @5555h	55h @2AAAh	30h @Sector address	30h @Sector address(3)
Erase the Whole Flash	1	0	AAh @5555h	55h @2AAAh	80h @5555h	AAh @5555h	55h @2AAAh	10h @5555h	
Suspend Block Erase	1	0	B0h @any address						
Resume Block Erase	1	0	30h @any address						
EEPROM Power Down	0	1	AAh @5555h	55h @2AAAh	30h @5555h				
Deep Power Down	1	0	20h @5555h						
SDP Enable (EEPROM)	0	1	AAh @5555h	55h @2AAAh	A0h @5555h	Write byte 1	Write byte 2		Write byte N
SDP Disable (EEPROM)	0	1	AAh @5555h	55h @2AAAh	80h @5555h	AAh @5555h	55h @2AAAh	20h @5555h	
Write in OTP Row	0	1	AAh @5555h	55h @2AAAh	B0h @5555h	Write byte 1	Write byte 2		Write byte N
Return (from OTP Read or EEPROM Power Down)	0	1	F0h @ any address						
Reset	1	0	AAh @5555h	55h @2AAAh	F0h @any Address				
Reset (short instruction)	1	0	F0h @any address						

Notes: 1. AAh @5555h means Write byte AAh at address 5555h.
2. This instruction can also be performed as a simple Read operation with A9=V_{ID} (refer to READ chapter).
3. Additional blocks to be erased must be entered within 80µs.

Table 5. Device Identifiers

Identifier	$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A9	Other Addresses	DQ0 - DQ7
Read the Manufacturer Identifier	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{ID}	Don't Care	20h
Read the Flash Block Identifier	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	Don't Care	0E3h
Read the EEPROM Block Identifier	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	V_{IL}	V_{ID}	Don't Care	64 bytes user defined

Note: X = Don't Care.

The M39432 set of instructions includes:

- Program a byte in the Flash block
- Read a Flash sector protection status
- Erase instructions: Flash Sector Erase, Flash Block Erase, Flash Sector Erase Suspend, Flash Sector Erase Resume
- EEPROM power down
- Deep power down
- Set/Reset the EEPROM software write protection (SDP)
- OTP row access
- Reset and Return
- Read identifiers: read the manufacturer identifier, Read the Flash block identifier

These instructions are detailed in Table 4.

For efficient decoding of the instruction, the two first bytes of an instruction are the coded cycles and are followed by a command byte or a confirmation byte. The coded cycles consist of writing the data AAh at address 5555h during the first cycle and data 55h at address 2AAAh during the second cycle.

In the specific case of the Erase instruction, the instruction expects confirmation by two additional coded cycles.

POWER SUPPLY and CURRENT CONSUMPTION

EEPROM Power Down. The M39432 can be set with the EEPROM in power down with the help of the EEPROM power down instruction (see Table 4). Once the EEPROM power down instruction is decoded, the EEPROM block cannot be accessed unless a further Return instruction is decoded.

Deep Power Down. The M39432 can be set in the lowest I_{CC} consumption mode with the help of the Deep Power Down instruction (see Table 4). Once the instruction is decoded, the device is set in a sleep mode until a Reset instruction is decoded.

Power Up. The M39432 internal logic is reset upon a power-up condition to Read memory status. Any Write operation in EEPROM is inhibited during the first 5 ms following the power-up.

Either $\overline{EF}$, $\overline{EE}$ or $\overline{W}$ must be tied to V_{IH} during Power-up for the maximum security of the data contents and to remove the possibility of a byte being written on the first rising edge of $\overline{EF}$, $\overline{EE}$ or $\overline{W}$. Any write cycle initiation is locked when Vcc is below V_{LKO}.

READ

Read operations and instructions can be used to:

- read the contents of the Memory Array (Flash block and EEPROM block)
- read the Memory Array (Flash block and EEPROM block) status and identifiers.

Read data (Flash and EEPROM blocks)

Both Chip Enable $\overline{EF}$ (or $\overline{EE}$) and Output Enable ($\overline{G}$) must be low in order to read the data from the memory.

Read the Manufacturer Identifier

The manufacturer's identifier can be read with two methods: a Read operation or a Read instruction.

Read Operation. The manufacturer's identifier can be read with a Read operation with specific logic levels applied on A0, A1, A6 and the V_{ID} level (V_{ID} = 12V + 0.5V) on A9 (see Table 5).

Read Instruction. The manufacturer's identifier can also be read with a single instruction composed of 4 operations: 3 specific Write operations (see Table 4) and a Read which outputs the Manufacturer identifier, the Flash block identifier or the Flash sector protection status (depending on the levels applied on A0, A1, A6, A16, A17 and A18.

Table 6. Status Bit

	$\overline{EF}$	$\overline{EE}$	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Flash	V_{IL}	V_{IH}	Data Polling	Toggle Flag	Error Flag	X	Erase Time-out	X	X	X
EEPROM	V_{IH}	V_{IL}	Data Polling	Toggle Flag	X	X	X	X	X	X

Note: X = Not guaranteed value, can be read either '1' or '0'.

Read the Flash Block Identifier

The Flash block identifier can be read with two methods: a Read operation or a Read instruction.

Read Operation. The Flash block identifier (E3h) can be read with a single Read operation with specific logic levels applied on A0, A1, A6 and the V_{ID} level on A9 (see Table 5).

Read Instruction. The Flash block identifier can also be read with an instruction composed of 4 operations: 3 specific Write operations and a Read (see Table 4).

Read the EEPROM Block Identifier

The EEPROM block identifier (64 bytes, user defined) can be read with a single Read operation with A6 = '0' and A9 = V_{ID} (see Table 5).

Read the OTP Row

The OTP row is mapped in the EEPROM block ($\overline{EE}$ = '0', $\overline{EF}$ = '1'). Read of the OTP row (64 bytes) is by an instruction (see Table 4) composed of three specific Write operations of data bytes at three specific memory locations (each location in a different page) before reading the OTP row content.

When accessing the OTP row, only the LSB addresses (A6 to A0) are decoded where A6 must be '0'.

Each Read of the OTP row has to be followed by the Return instruction (see Table 4).

Read the Flash Sector Protection Status

Reading the Flash sector protection status is by an instruction similar to the Read Manufacturer identifier instruction, the only difference being the value of the logic levels applied on A0, A1, A6, while A16, A17 and A18 define the Flash sector whose protection has to be verified. Such a read instruction will output a 01h if the Flash sector is protected and a 00h if the Flash sector is not protected.

The Flash sector protection status can also be verified with a Read operation (see chapter: Flash block specific features), with V_{ID} on A9.

Read the Status Bits

The M39432 provides several Write operation status flags which may be used to minimize the application write (or erase or program) time. These signals are available on the I/O port bits when programming (or erasing) are in progress. It should be noted that the Ready/Busy pin also reflects the status of the EEPROM Write (the Ready/Busy pin does not reflect the status of the Flash Programming/Erasing).

Data Polling flag, DQ7. When Erasing or Programming into the Flash block (or when Writing into the EEPROM block), bit DQ7 outputs the complement of the bit being entered for Programming/Writing on DQ7. Once the Program instruction or the Write operation is performed, the true logic value is read on DQ7 (in a Read operation).

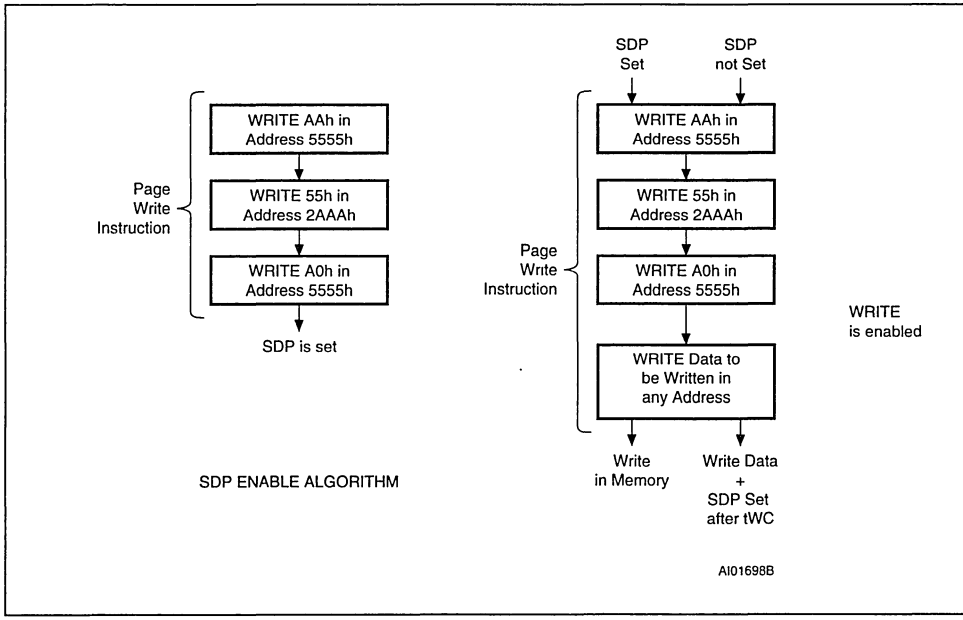
Flash memory block specific features:

- Data Polling is effective after the fourth W pulse (for programming) or after the sixth W pulse (for Erase). It must be performed at the address being programmed or at an address within the Flash sector being erased.
- During an Erase instruction, DQ7 outputs a '0'. After completion of the instruction, DQ7 will output the last bit programmed (that is a '1' after erasing).
- if the byte to be programmed is in a protected Flash sector, the instruction is ignored.
- If all the Flash sectors to be erased are protected, DQ7 will be set to '0' for about 100µs, and then return to the previous addressed byte. No erasure will be performed.
- if all sectors are protected, a Bulk Erase instruction is ignored.

Toggle flag, DQ6. The M39432 also offers another way for determining when the EEPROM write or the Flash memory Program instruction is completed. During the internal Write operation, the DQ6 will toggle from '0' to '1' and '1' to '0' on subsequent attempts to read any byte of the memory, when either $\overline{G}$, $\overline{EE}$ or $\overline{EF}$ is low.

When the internal cycle is completed the toggling will stop and the data read on DQ0-DQ7 is the addressed memory byte. The device is now accessible for a new Read or Write operation. The operation is completed when two successive reads yield the same output data.

Figure 4. EEPROM SDP Enable Flowcharts



Flash memory block specific features:

a. The Toggle bit is effective after the fourth $\overline{W}$ pulse (for programming) or after the sixth $\overline{W}$ pulse (for Erase).

b. If the byte to be programmed belongs to a protected Flash sector, the instruction is ignored and:

- if all the Flash sectors selected for erasure are protected, DQ6 will toggle to '0' for about 100µs, and then return to the previous addressed byte.
- if all sectors are protected, the Bulk Erase instruction is ignored.

Error flag, DQ5 (Flash block only). This bit is set to '1' when there is a failure during either a Flash byte programming or a Sector erase or the Bulk Erase.

In case of error in Flash sector erase or byte program, the Flash sector in which the error occurred or to which the programmed byte belongs, must not be used any longer (other Flash sectors may still be used). The Error bit resets after Reset instruction.

During a correct Program or Erase, the Error bit will set to '0'.

Erase Time-out flag, DQ3 (Flash block only). The Erase Timer bit reflects the time-out period allowed between two consecutive Sector Erase instructions. The Erase timer bit is set to '0' after a Sector Erase instruction for a time period of 100µs ±20% unless an additional Sector Erase instruction is decoded. After this time period or when the additional Sector Erase instruction is decoded, DQ3 is set to '1'.

WRITE a BYTE (or a PAGE) in EEPROM

It should be noticed that writing in the EEPROM block is an operation, it is not an instruction (as for Programming a byte in the Flash block).

Write a Byte in EEPROM Block

A write operation is initiated when Chip Enable $\overline{EE}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Addresses are latched on the falling edge of $\overline{W}$, $\overline{EE}$ whichever occurs last.

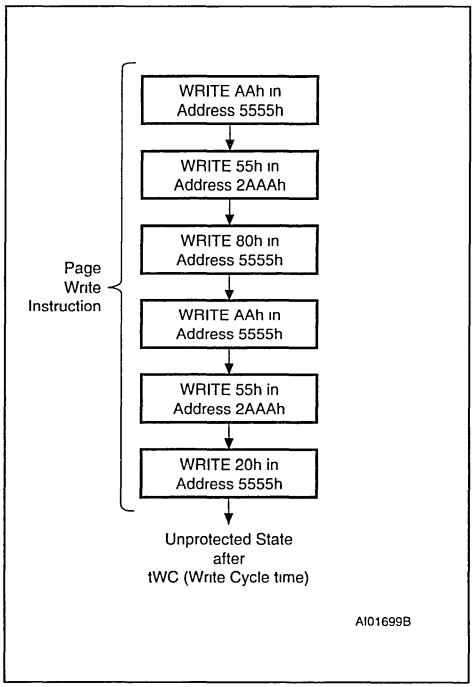
Once initiated, the write operation is internally timed until completion, that is during a time t_W.

The status of the write operation can be found by reading the Data Polling and Toggle bits (as detailed in the READ chapter) or the Ready/Busy output. This Ready/Busy output is driven low from the write of the byte being written until the completion of the internal Write sequence.

Table 7. Write the EEPROM Block Identifier

$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	A6	A9	Other Addresses	DQ0 - DQ7
V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	Don't Care	64 bytes User Defined

Figure 5. SDP disable Flowchart



Write a Page in EEPROM Block

The Page write allows up to 64 bytes within the same EEPROM page to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A6-A14 must be the same for all bytes. Once initiated, the Page write operation is internally timed until completion, that is during a time t_{WC}.

The status of the write operation can be seen by reading the Data Polling and Toggle bits (as detailed in the READ chapter) or the Ready/Busy output. This Ready/Busy output is driven low from the write of the first byte to be written until the completion of the internal Write sequence.

A Page write is composed of successive Write instructions which must be sequenced within a time period (between two consecutive Write operations) that is smaller than the t_{WLWL} value. If this period of time exceeds the t_{WLWL} value, the internal programming cycle will start.

EEPROM Block Software Data Protection

A protection instruction allows the user to inhibit all write modes to the EEPROM block: the Software Data Protection (referenced as SDP in the following). The SDP feature is useful for protecting the EEPROM memory from inadvertent write cycles that may occur during uncontrolled bus conditions.

The M39432 is shipped as standard in the unprotected state meaning that the EEPROM memory contents can be changed by the user. After the SDP enable instruction, the device enters the Protect Mode where no further write operations have any effect on the EEPROM memory contents.

The device remains in this mode until a valid SDP disable instruction is received whereby the device reverts to the unprotected state.

To enable the Software Data Protection, the device has to be written (with a Page Write) with three specific data bytes at three specific memory locations (each location in a different page) as shown in Figure 4. This sequence provides an unlock key to enable the write action, and, at the same time, SDP continues to be set. Any further Write in EEPROM when the SDP is set will use this same sequence of three specific data bytes at three specific memory locations followed by the bytes to write. The first SDP enable sequence can be directly followed by the bytes to written.

Similarly, to disable the Software Data Protection the user has to write specific data bytes into six different locations with a Page Write addressing different bytes in different pages, as shown in Figure 5.

The Software Data Protection state is non-volatile and is not changed by power on/off sequences. The SDP enable/disable instructions set/reset an internal non-volatile bit and therefore will require a write time t_{WC}, This Write operation can be monitored only on the Toggle bit (status bit DQ6) and the Ready/Busy pin. The Ready/Busy output is driven low from the first byte to be written (that is the first Write AAh, @5555h of the SDP set/reset sequence) until the completion of the internal Write sequence.

Figure 6. Data Polling Flowchart

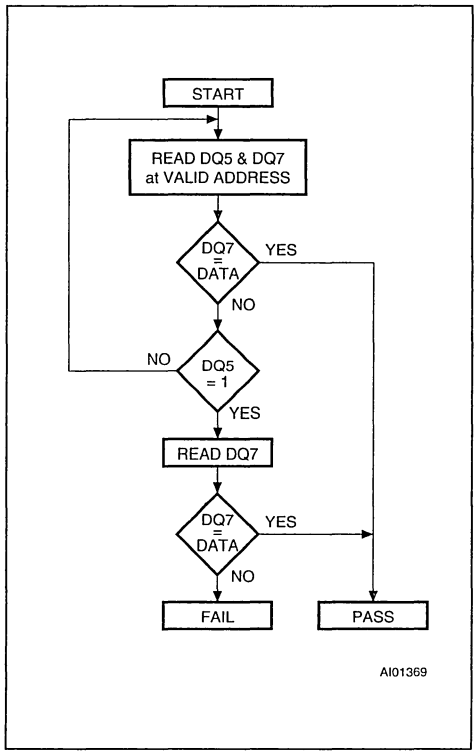
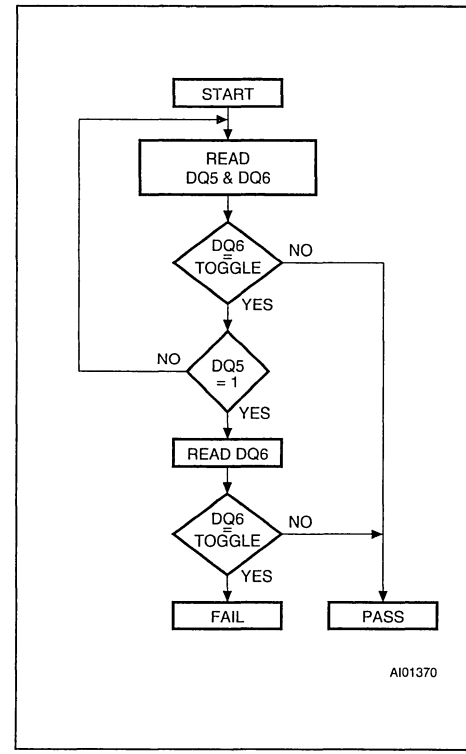


Figure 7. Data Toggle Flowchart



Write OTP Row

Writing (only one time) in the OTP row (64 bytes) is enabled by an instruction. This instruction is composed of three specific Write operations of data bytes at three specific memory locations (each location in a different page) followed by the the data to store in the OTP row (refer to Table 4).

When accessing the OTP row, the only LSB addresses (A6 to A0) are decoded, with A6 = '0'.

Write the EEPROM Block Identifier

The EEPROM block identifier can be written with a single Write operation with specific logic levels applied on A6 and the V_{ID} level on A9 (see Table 7).

PROGRAM in the Flash BLOCK

It should be noted that writing data into the EEPROM block and the Flash block is not performed in a similar way: the Flash memory requires an instruction (see Instruction chapter) for Erasing and another instruction for Programming one (or more) byte(s), the EEPROM memory is directly written with a simple operation (see Operation chapter).

Program Instuction. During the execution of the Program instruction, the Flash block memory will not accept any further instructions.

The Flash block memory can be programmed byte-by-byte. The program instruction is a sequence of three specific Write operations followed by writing the address and data byte to be programmed into the Flash block memory (see Table 4). The M39432 automatically starts and performs the programming after the fourth write operation.

During programming, the memory status may be checked by reading the status bits DQ5, DQ6 and DQ7, as detailed in the following sections.

Data Polling. Polling on DQ7 is a method of checking whether a Program or an Erase instruction is in progress or completed (see Figure 6). When a Program instruction is in progress, data bit DQ7 is the complement of the original data bit 7; when DQ7 is identical to the old data and the Error bit DQ5 is still '0', the instruction is complete. To determine if DQ7 is valid, each poll must store the original data for comparison, and if they are the same, it can be considered that the operation was successful. The Error bit DQ5 is checked to ensure timing limits have not exceeded.

When an Erase operation is in progress, DQ7 is always '0', and will be '1' when finished, so long as DQ5= '0'.

In all cases, when DQ5 is '1', DQ7 should be checked again, in case DQ7 changed simultaneously with DQ5. If DQ7 = true data (Program) or DQ7 = '1' (Erase), the operation is successful and execution should return to the caller. A suggested second read will provide all true data (Program) or all FFh (Erase). Otherwise, this should be flagged as an error, and the device should be Reset.

Data Toggle. Checking the Toggle bit DQ6 is an alternative method of checking if Program or Erase operations are in progress or completed (see Figure 7). When an operation is in progress, data bit DQ6 constantly toggles for successive read operations. When DQ6 no longer toggles and the Error bit DQ5 is '0', the operation is completed. To determine if DQ6 has toggled, each polling action requires 2 consecutive read operations of the data, and if the data read is the same, it can be considered that the operation was successful. The Error bit DQ5 is checked to ensure timing limits have not been exceeded. In all cases, when DQ5 is '1', DQ6 should be checked again, in case DQ6 has changed simultaneously with DQ5. If DQ6 has stopped toggling, the operation is successful and execution should return to the caller. A suggested second read will provide all true data (Program) or all FFh (Erase). Otherwise, this event should be flagged as an error, and the device should be Reset.

ERASE in the Flash BLOCK

It should be noted that:

a. Programming any byte of one Flash sector (or bulk) requires that the Flash sector (or bulk) has been previously erased (once for all bytes within the sector or bulk) with the correct instruction (see Instructions chapter).

b. Writing in the EEPROM memory is an operation triggering an automatic sequencing of byte erase followed by a byte write. Writing in EEPROM does not require a specific erase operation before writing.

Bulk Erase Instruction. The Bulk Erase instruction uses six write operations followed by Read operations of the status register bits, as described in Table 4. If any byte of the Bulk Erase instruction is wrong, the Bulk Erase instruction aborts and the device is reset to the Read Flash memory status.

During a Bulk Erase, the memory status may checked by reading the status bits DQ5, DQ6 and DQ7, as detailed in the "PROGRAM in the Flash BLOCK" chapter. The Error bit (DQ5) returns a '1' if there has been an Erase Failure (maximum number of erase cycles have been executed).

It is not necessary to program the array with 00h, the M39432 will automatically do this before erasing to FFh.

During the execution of the Bulk Erase instruction, the Flash block logic does not accept any instruction.

Sector Erase in Flash Block. The Sector Erase instruction uses six write operations, as described in Table 4. Additional Flash Sector Erase confirm commands and Flash sector addresses can written subsequently to erase other Flash sectors in parallel, without further coded cycles, if the additional instruction is transmited in a shorter time than the timeout period to end of period. The input of a new Sector Erase instruction will restart the time-out period.

The status of the internal timer can be monitored through the level of DQ3 (Erase time-out bit), if DQ3 is '0' the Sector Erase instruction has been received and the timeout is counting; if DQ3 is '1', the timeout has expired and the M39432 is erasing the Flash sector(s). Before and during Erase timeout, any instruction different than Erase suspend and Erase Resume will abort the instruction and reset the device to read array mode.
It is not necessary to program the Flash sector with 00h as the M39432 will do this automatically before erasing (byte = FFh).

During a Sector Erase, the memory status may be checked by reading the status bits DQ5, DQ6 and DQ7, as detailed in the "Program instruction" chapter. During the execution of the erase instruction, the Flash block logic accepts only the Reset and Erase Suspend instructions (erasure of one Flash sector may be suspended, in order to read data from another Flash sector, and then resumed).

Table 8. Flash Sector Protection

$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A9	A12	A16	A17	A18	DQ0 - DQ7
V_{IL}	V_{IH}	V_{ID}	V_{IL}	X	X	X	V_{ID}	X	SA	SA	SA	Protection Activation
V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{ID}	X	SA	SA	SA	Verify the protection status: when DQ0= 1, the block is protected

Notes: X = Don't care.
SA = Software Address.

Table 9. Flash Unprotection

$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A9	A12	A16	A17	A18	DQ0 - DQ7
V_{ID}	V_{IH}	V_{ID}	V_{IL}	X	X	X	V_{ID}	V_{IH}	V_{IH}	X	X	Activation of Unprotected Mode
V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	X	SA	SA	SA	Verify the protection status: when 00h, the block is unprotected

Notes: X = Don't care.
SA = Software Address.

Erase Suspend Instruction. When a Flash Sector Erase operation is in progress, the Erase Suspend instruction may suspend the operation by writing B0h at any address (see Table 4). This allows reading of data from another Flash sector while erase is in progress. Erase suspend is accepted only during the Flash Sector Erase instruction execution and defaults to read array mode. An Erase Suspend instruction entered during an Erase timeout will, in addition to suspending the erase, terminates the timeout.

The Toggle bit DQ6 stops toggling when the M39432 internal logic is suspended. The Toggle bit status must be monitored at an address out of the Flash sector being erased. Toggle bit will stop toggling between 0.1µs and 15µs after the Erase Suspend instruction has been written. The M39432 will then automatically be set into Read Flash Block Memory Array mode.

When erase is suspended, Reading from Flash sectors being erased will output invalid data, a Read from Flash sector not being erased is valid. During an Erase Suspend, the Flash memory will respond only to Erase Resume and Reset instructions.

A Reset instruction will definitively abort erasure and can leave invalid data in the Flash sectors being erased.

Erase Resume Instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by this instruction. The Erase Resume instruction consists of writing 30h at any address (see Table 4).

FLASH BLOCK SPECIFIC FEATURES

Flash Sector Protection. Each Flash sector can be separately protected against Program or Erase. Flash Sector Protection provides additional data security, as it disables all program or erase operations. This mode is activated when both A9 and $\overline{G}$ are set to V_{ID} (12V + 0.5V) and the Flash sector address is applied on A16, A17 and A18, as shown in Figure 8 and Table 8.

Flash sector protection is programmed with the help of a specific sequence of levels applied on $\overline{EF}$, $\overline{EE}$, $\overline{G}$, A0, A1, A6, A9, A16, A17 and A18; this sequence includes a verification of the Protection status on DQ0 as shown in Table 8.

Any attempt to program or erase a protected Flash sector will be ignored by the device.

Remarks:

- The Verify operation is a read with a simulated worst case conditions. This allows a guarantee of the retention of the Protection status
- During the application life, the Sector protection status can be accessed with a regular Read instruction without applying a "high voltage" V_{ID} on A9. This instruction is detailed in Table 4.

Flash Sector Unprotection. Flash sectors can be unprotected to allow updating of their contents. Note that the Sector Unprotection unprotects all sectors (sector 0 up to sector 7).

Flash Sector Unprotection is activated with a specific sequence of levels applied on $\overline{EF}$, $\overline{EE}$, $\overline{G}$, A0, A1, A6, A9, A12, A16, A17 and A18; this sequence includes a verification of the Protection status on DQ0-DQ7 as shown in Figure 9 and Table 9.

Figure 8. Block Protection Flowchart

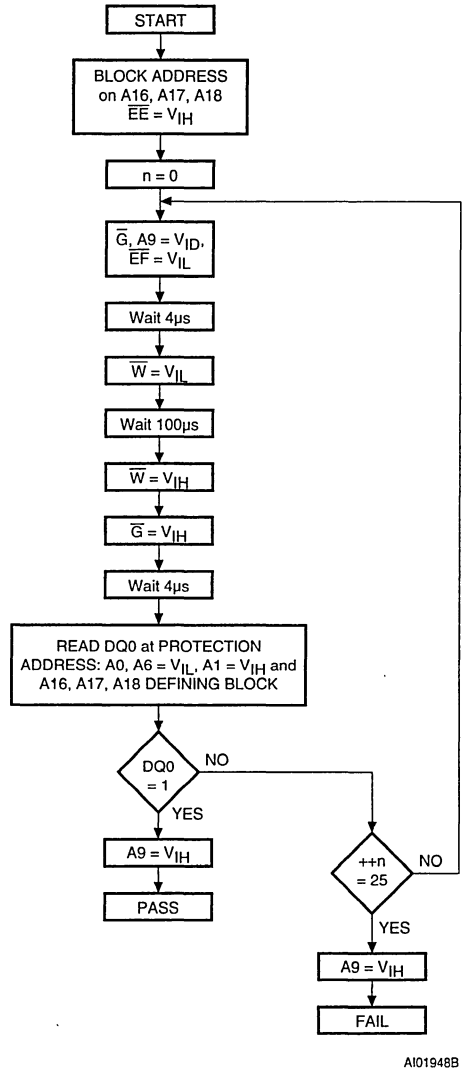
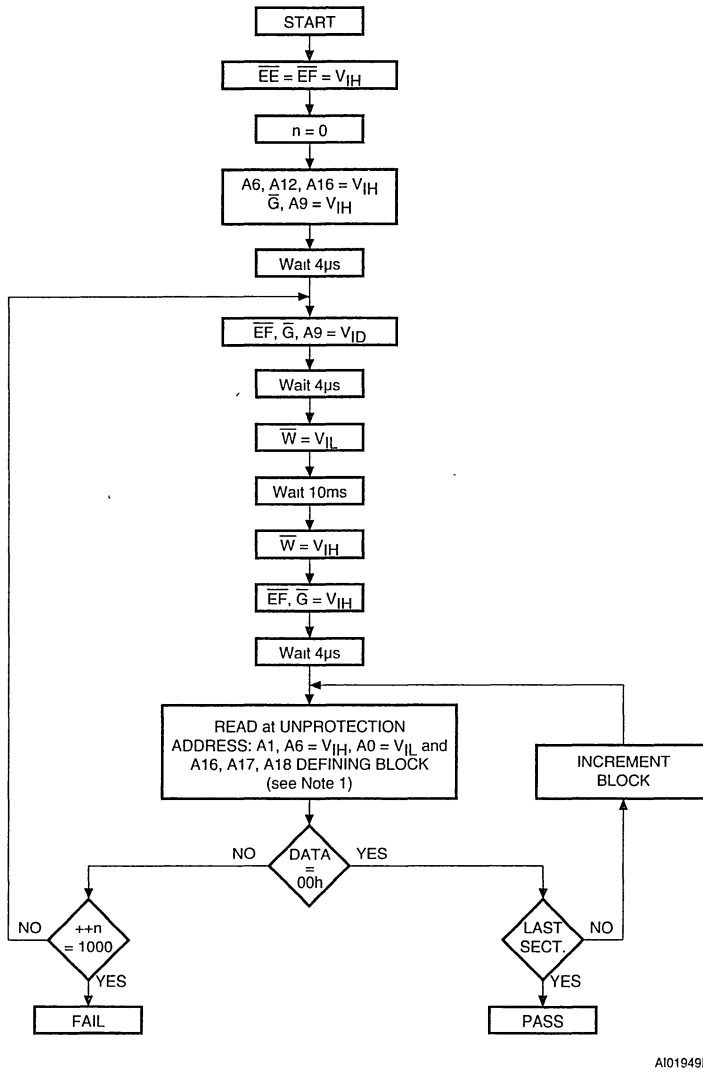


Figure 9. Block Unprotecting Flowchart



Note: 1. A6 is kept at V_{IH} during unprotection algorithm in order to secure best unprotection verification. During all other protection status reads, A6 must be kept at V_{IL}.

Table 10. AC Measurement Conditions

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.45V to 2.4V
Input Timing Ref. Voltages	0.8V and 2V
Output Timing Ref. Voltages	1.5V

Figure 10. AC Testing Input Output Waveform

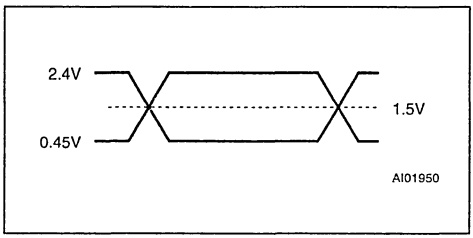


Figure 11. Output AC Testing Load Circuit

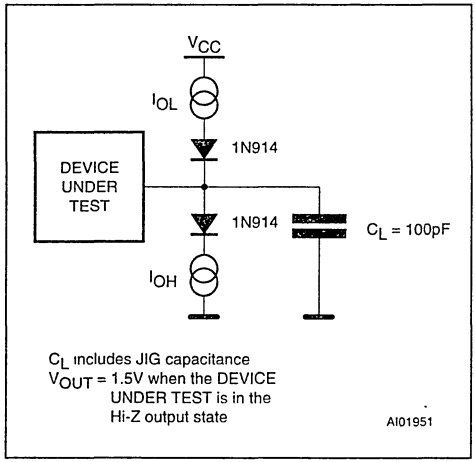


Table 11. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

FLASH BLOCK SPECIFIC FEATURES (cont' d)

This allows a guarantee of the retention of the Protection status.

Remarks:

- The Verify operation is a read with a simulated worst case conditions. This allows a guarantee of the retention of the Protection status
- During the application life, the Sector protection status can be accessed with a regular Read instruction without "high voltage" V_{ID} on A9. This instruction is detailed in Table 4.

Reset Instruction. The Reset instruction resets the device internal logic in a few µs. Reset is an instruction of either one write operation or three write operations (refer to Table 4).

Supply Rails. Normal precautions must be taken for supply voltage decoupling, each device in a system should have the V_{CC} rail decoupled with a 0.1µF capacitor close to the V_{CC} and V_{SS} pins. The printed circuit board trace width should be sufficient to carry the V_{CC} program and erase currents required.

GLOSSARY

Block: EEPROM block (256 Kbit) or Flash block (4Mbit)

Bulk: the whole Flash block (4Mbit)

Sector: 64 Kbyte of Flash memory

Page: 64 bytes of EEPROM

Write and Program: Writing (into the EEPROM block) and Programming (the Flash block) is not performed in a similar way:

- the Flash memory requires an instruction (see Instruction chapter) for Erasing and another instruction for Programming one (or more) byte(s)
- the EEPROM memory is directly written with a simple operation (see Operation chapter).

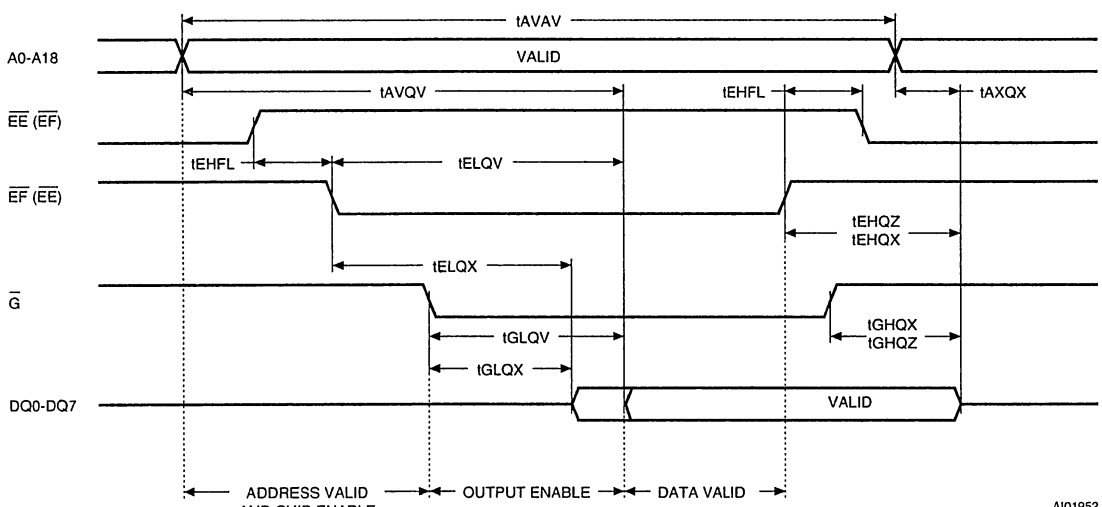
SDP: Software Data Protection. Used for protecting the EEPROM block against false Write operations (as in noisy environments).

Table 12. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3.3V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC1} (1)	Supply Current (Read Flash) TTL	$\overline{EE} = V_{IH}$, $\overline{EF} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz		15	mA
I_{CC2}	Supply Current (Read EEPROM) TTL	$\overline{EE} = V_{IL}$, $\overline{EF} = V_{IH}$, $\overline{G} = V_{IH}$, f = 6MHz		15	mA
I_{CC3}	Supply Current (Standby) CMOS	$\overline{EF} = \overline{EE} = V_{CC} \pm 0.2V$		40	µA
I_{CC4}	Supply Current (Flash Block Program or Erase)	Byte program, Sector or Chip Erase in progress		20	mA
I_{CC5}	Supply Current (EEPROM Write)	During t_{WC}		20	mA
I_{CC6}	Supply Current in Deep Power Down Mode	After a Deep Power Down instruction (see Table 4)		2	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{CC} –0.4		V
		I_{OH} = –2mA	0.85 V_{CC}		V
V_{ID}	A9 High Voltage		11.5	12.5	V
I_{ID}	V_{ID} Current	A9 = V_{ID}		50	µA
V_{LKO}	V_{CC} Minimum for Write, Erase and Program		1.9	2.2	V

Note: 1. When reading the Flash block when an EEPROM byte(s) is under a write cycle, the supply current is $I_{CC1} + I_{CC5}$

Figure 12. Read Mode AC Waveforms



Note: Write Enable ($\overline{W}$) = High

Table 13A. Read AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3.3V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	M39432				Unit
				-120		-150		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(\overline{EE}, \overline{EF}) = (V_{IH}, V_{IL})$, $\overline{G} = V_{IL}$	120		150		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(\overline{EE}, \overline{EF}) = (V_{IH}, V_{IL})$, $\overline{G} = V_{IL}$		120		150	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		120		150	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(\overline{EE}, \overline{EF}) = (V_{IH}, V_{IL})$	0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(\overline{EE}, \overline{EF}) = (V_{IH}, V_{IL})$		55		55	ns
t_{EHQX}	t_{OH}	Chip Enable High to Output Transition	$\overline{G} = V_{IL}$	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$		40		40	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(\overline{EE}, \overline{EF}) = (V_{IH}, V_{IL})$	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(\overline{EE}, \overline{EF}) = (V_{IH}, V_{IL})$		40		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$(\overline{EE}, \overline{EF}) = (V_{IL}, V_{IH})$ or $(\overline{EE}, \overline{EF}) = (V_{IH}, V_{IL})$, $\overline{G} = V_{IL}$	0		0		ns
t_{EHFL}	t_{CED}	$\overline{EE}$ ($\overline{EF}$) Active to $\overline{EF}$ ($\overline{EE}$)		100		100		ns

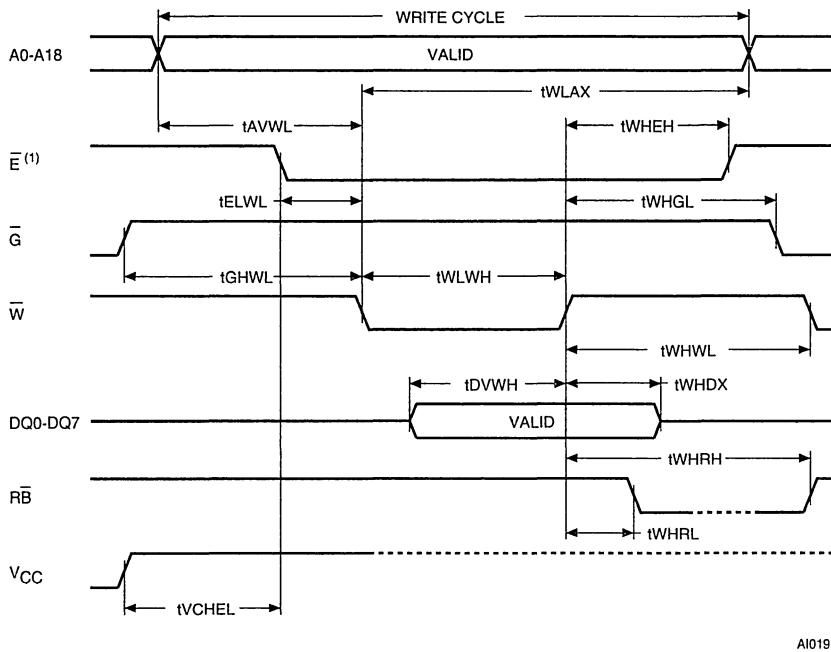
Notes: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{EE}$ (or $\overline{EF}$) without increasing t_{ELQV}.

Table 13B. Read AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3.3V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	M39432				Unit
				-200		-250		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$(\overline{E}, \overline{EF})$ = (V_{IL}, V_{IH}) or ($\overline{E}$, $\overline{EF}$) = (V_{IH}, V_{IL}), $\overline{G}$ = V_{IL}	200		250		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$(\overline{E}, \overline{EF})$ = (V_{IL}, V_{IH}) or ($\overline{E}$, $\overline{EF}$) = (V_{IH}, V_{IL}), $\overline{G}$ = V_{IL}		200		250	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		200		250	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$(\overline{E}, \overline{EF})$ = (V_{IL}, V_{IH}) or ($\overline{E}$, $\overline{EF}$) = (V_{IH}, V_{IL})	0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$(\overline{E}, \overline{EF})$ = (V_{IL}, V_{IH}) or ($\overline{E}$, $\overline{EF}$) = (V_{IH}, V_{IL})		70		120	ns
t_{EHQX}	t_{OH}	Chip Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		50		60	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$(\overline{E}, \overline{EF})$ = (V_{IL}, V_{IH}) or ($\overline{E}$, $\overline{EF}$) = (V_{IH}, V_{IL})	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$(\overline{E}, \overline{EF})$ = (V_{IL}, V_{IH}) or ($\overline{E}$, $\overline{EF}$) = (V_{IH}, V_{IL})		50		60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$(\overline{E}, \overline{EF})$ = (V_{IL}, V_{IH}) or ($\overline{E}$, $\overline{EF}$) = (V_{IH}, V_{IL}), $\overline{G}$ = V_{IL}	0		0		ns
t_{EHFL}	t_{CED}	$\overline{E}$ ($\overline{EF}$) Active to $\overline{EF}$ ($\overline{E}$)		100		100		ns

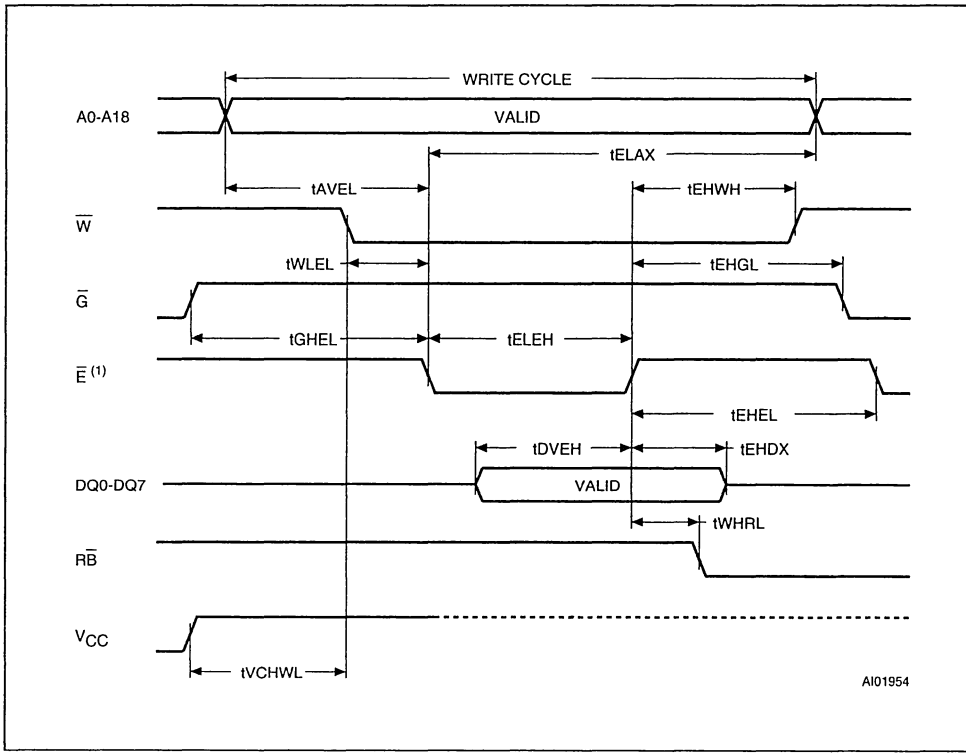
Notes: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ (or $\overline{EF}$) without increasing t_{ELQV}.

Figure 13. Write AC Waveforms, $\overline{W}$ Controlled



Notes: Address are latched on the falling edge of $\overline{W}$. Data is latched on the rising edge of $\overline{W}$.
$\overline{E}$ is either $\overline{EF}$ when $\overline{EE}$ = V_{IH} or $\overline{EE}$ when $\overline{EF}$ = V_{IH}.

Figure 14. Write AC Waveforms, $\overline{E}$ Controlled



Notes: Address are latched on the falling edge of $\overline{E}$, Data is latched on the rising edge of $\overline{E}$.
$\overline{E}$ is either $\overline{EF}$ when $\overline{EE}$ = V_{IH} or $\overline{EE}$ when $\overline{EF}$ = V_{IH}

Table 14. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3.3V ± 0.3V)

Symbol	Alt	Parameter	M39432								Unit
			-120		-150		-200		-250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	120		150		200		150		ns
t_{ELWL} (2)	t_{CS}	Chip Enable Low to Write Enable Low	0		0		0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		65		80		50		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		65		80		50		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		0		0		ns
t_{WHEH} (2)	t_{CH}	Write Enable High to Chip Enable High	0		0		0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		35		35		20		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	50		65		65		50		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		0		0		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		50		50		µs
t_{WHQV1} (1)		Write Enable High to Output Valid (Program)	15		15		15		10		µs
t_{WHQV2} (1)		Write Enable High to Output Valid (Sector Erase)	2.0	30	2.0	30	2.0	30	1.0	30	sec
t_{WHWL0}		Time Out between 2 consecutive Section Erase		80		80		80		80	µs
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		0		0		ns
t_{WHRL} (3)	t_{DB}	Write Enable High to Ready/Busy Output Low		150		150		150		150	ns

Notes: 1 Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$
2. Chip Enable means ($\overline{EE}$, $\overline{EF}$) = (V_{IL}, V_{IH}) or ($\overline{EE}$, $\overline{EF}$) = (V_{IH}, V_{IL}).
3. With a 3.3KΩ pull-up resistor.

Table 15. Write AC Characteristics, $\overline{EE}$ or $\overline{EF}$ Controlled
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3.3V ± 0.3V)

Symbol	Alt	Parameter	M39432								Unit
			-120		-150		-200		-250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{WLWL}	t_{BLC}	Byte Load Cycle (EEPROM)	0.2	150	0.2	150	0.2	150	0.2	150	µs
t_{WHRH}	t_{WC}	Write Cycle Time (EEPROM)		10		10		10		10	ms
t_{AVAV}		Address Valid to Next Address Valid	120		150		200		150		ns
t_{WLEL}	t_{WS}	Write Enable Low to Memory Block Enable Low	0		0		0		0		ns
t_{ELEH}	t_{CP}	Memory Block Enable Low to Memory Block Enable High	50		65		80		50		ns
t_{DVEH}	t_{DS}	Input Valid to Memory Block Enable High	50		65		80		50		ns
t_{EHDX}	t_{DH}	Memory Block Enable High to Input Transition	0		0		0		0		ns
t_{EHWH}	t_{WH}	Memory Block Enable High to Write Enable High	0		0		0		0		ns
t_{EHEL}	t_{CPH}	Memory Block Enable High to Memory Block Enable Low	30		35		35		20		ns
t_{AVEL}	t_{AS}	Address Valid to Memory Block Enable Low	0		0		0		0		ns
t_{ELAX}	t_{AH}	Memory Block Enable Low to Address Transition	50		65		65		50		ns
t_{GHEL}		Output Enable High to Memory Block Enable Low	0		0		0		0		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		50		50		µs
t_{EHQV1} (1)		Memory Block Enable High to Output Valid (Program)	15		15		15		10		µs
t_{EHQV2} (1)		Memory Block Enable High to Output Valid (Sector Erase)	2.0	30	2.0	30	2.0	30	1.0	30	sec
t_{EHGL}	t_{OEH}	Memory Block Enable High to Output Enable Low	0		0		0		0		ns
t_{EHRL} (2)	t_{DB}	EEPROM Block Enable High to Ready/Busy Output Low		150		150		150		150	ns

Notes: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$.
2. With a 3 3KΩ pull-up resistor

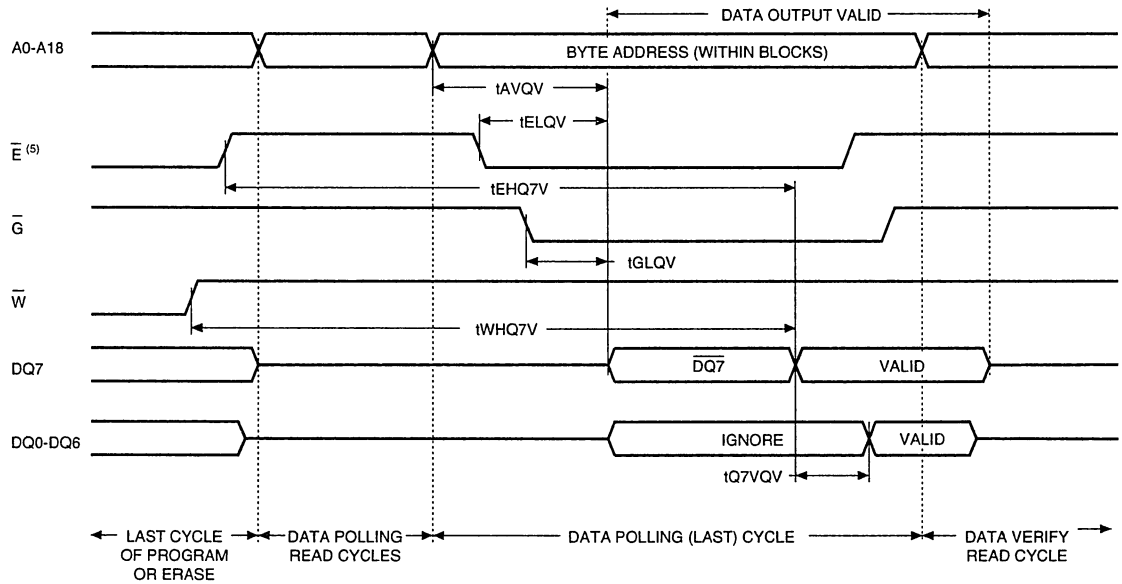


Figure 15. Data Polling DQ7 AC Waveforms

Notes: 1. All other timings are as a normal Read cycle.
2. DQ7 and DQ0-DQ6 can transmit to valid at any point during the data output valid period.
3. t_{WHQ7V} is the Program or Erase time.
4. During erasing operation Byte address must be within Blocks being erased.
5. $\overline{E}$ is either $\overline{EF}$ when $\overline{EE} = V_{IH}$ or $\overline{EE}$ when $\overline{EF} = V_{IH}$.

Table 16. Data Polling and Toggle Bit AC Characteristics (1)
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3.3V ± 0.3V)

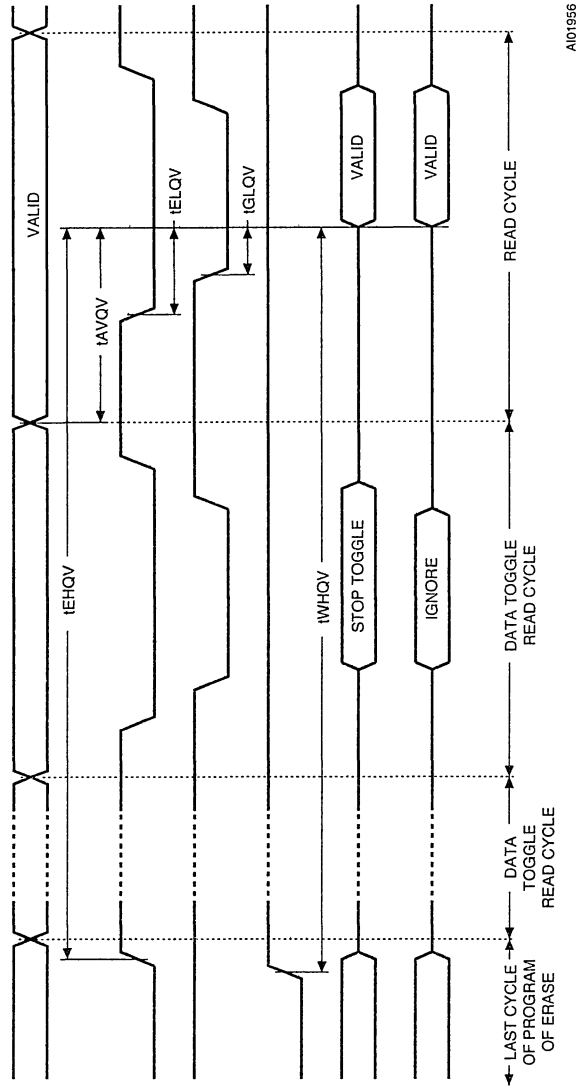
Symbol	Alt	Parameter	M39432								Unit
			-120		-150		-200		-250		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{WHQ7V1} (2)		Write Enable High to DQ7 Valid (Program, W Controlled)	10		10		10		10		µs
t_{WHQ7V2} (2)		Write Enable High to DQ7 Valid (Sector Erase, W Controlled)	1.5	30	1.5	30	1.5	30	1.5	30	sec
t_{EHQ7V1} (2)		Flash Block Enable High to DQ7 Valid (Program, EF Controlled)	10		10		10		10		µs
t_{EHQ7V2} (2)		Flash Block Enable High to DQ7 Valid (Sector Erase, EF Controlled)	1.5	30	1.5	30	1.5	30	1.5	30	sec
t_{Q7VQV}		Q7 Valid to Output Valid (Data Polling)		50		55		70		55	ns
t_{WHQV1}		Write Enable High to Output Valid (Program)	10		10		10		10		µs
t_{WHQV2}		Write Enable High to Output Valid (Sector Erase)	1.5	30	1.5	30	1.5	30	1.5	30	sec
t_{EHQV1}		Flash Block Enable High to Output Valid (Program)	10		10		10		10		µs
t_{EHQV2}		Flash Block Enable High to Output Valid (Sector Erase)	1.5	30	1.5	30	1.5	30	1.5	30	sec

Notes: 1. All other timings are defined in Read AC Characteristics table.
2. t_{WHQ7V} is the Program or Erase time.

Table 17. Program, Erase Times and Program, Erase Endurance Cycles (Flash Block)
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 3.3V ± 0.3V)

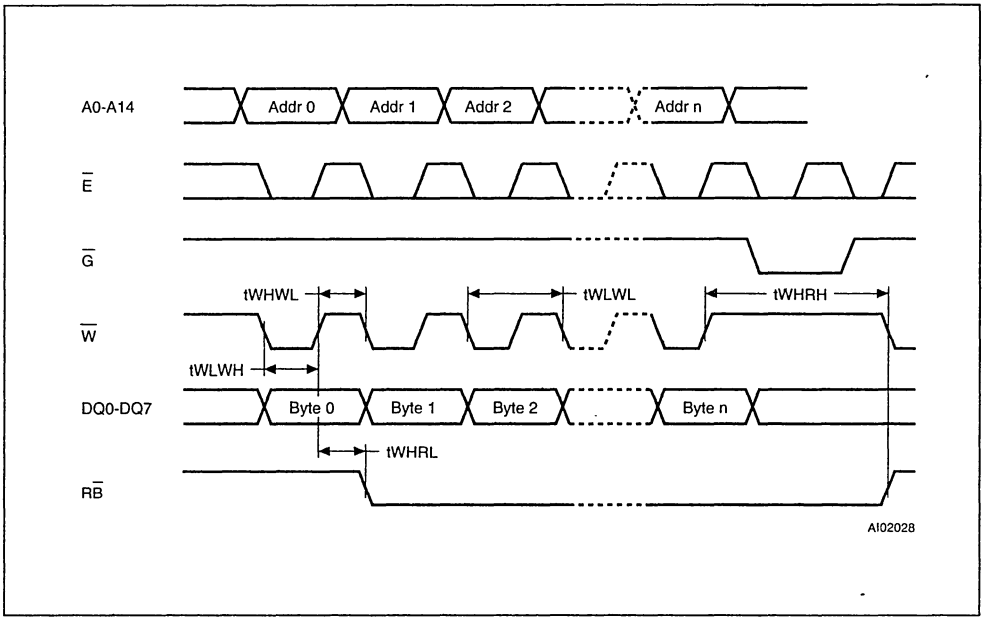
Parameter	M39432			Unit
	Min	Typ	Max	
Chip Program (Byte)		8		sec
Chip Erase (Preprogrammed)		3	30	sec
Chip Erase		10		sec
Sector Erase (Preprogrammed)		1	30	sec
Sector Erase		2		sec
Byte Program	10		1200	µs
Program/Erase Cycles (per Sector)	100,000			cycles

Figure 16. Data Toggle DQ6 AC Waveforms

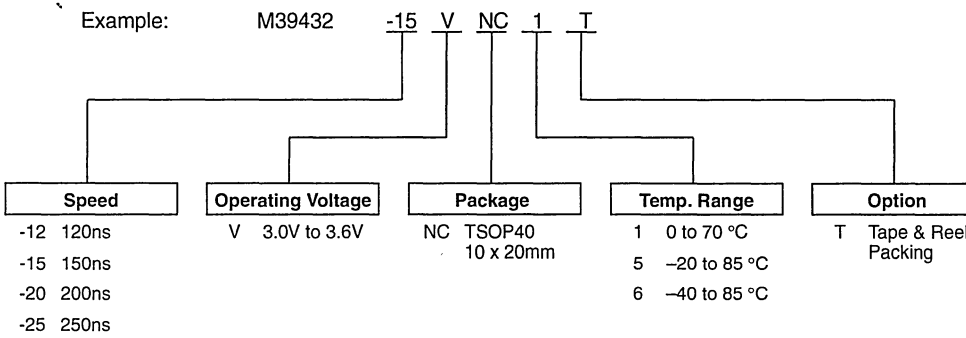


Notes: 1. All other timings are as a normal Read cycle.
2. Ē is either EF when EE = V_{IH} or EE when EF = V_{IH}.

Figure 17. EEPROM Page Write Mode AC Waveforms, $\overline{W}$ Controlled



ORDERING INFORMATION SCHEME

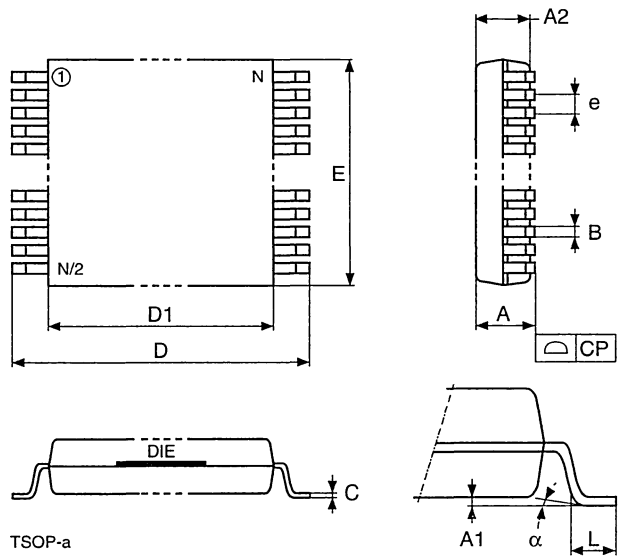


Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

TSOP40 - 40 lead Plastic Thin Small Outline, 10 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		9.90	10.10		0.390	0.398
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0	5		0	5
N	40			40		
CP			0.10			0.004



TSOP-a

Drawing is not to scale

M39832

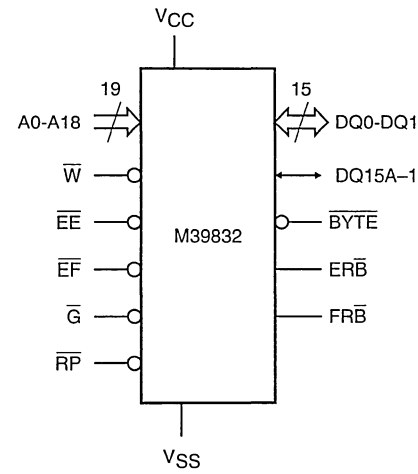
Single Chip 8 Mbit (1Mb x8 or 512Kb x16) Flash and 256 Kbit Parallel EEPROM Memory

PRELIMINARY DATA

- 2.7V to 3.6V SUPPLY VOLTAGE for PROGRAM, ERASE and READ OPARATIONS
- FLASH ARRAY
  - Boot block (Top or Bottom location)
  - Parameter and Main blocks
  - Selectable x8/x16 Data Bus ($\overline{BYTE}$ pin).
- EEPROM ARRAY
  - x8 Data Bus only.
- 120ns ACCESS TIME (Flash and EEPROM array)
- WRITE, PROGRAM and ERASE STATUS BITS
- CONCURRENT MODE (Read Flash while writing to EEPROM)
- 100,000 ERASE/WRITE CYCLES
- 10 YEARS DATA RETENTION
- LOW POWER CONSUMPTION
  - Stand-by mode: 100µA
  - Automatic Stand-by mode
- 64 bytes ONE TIME PROGRAMMABLE MEMORY (x8 Data Bus only)
- STANDARD EPROM/OTP MEMORY PACKAGE
- EXTENDED TEMPERATURE RANGES

TSOP48 (NE)
12 x 20 mm

Figure 1. Logic Diagram



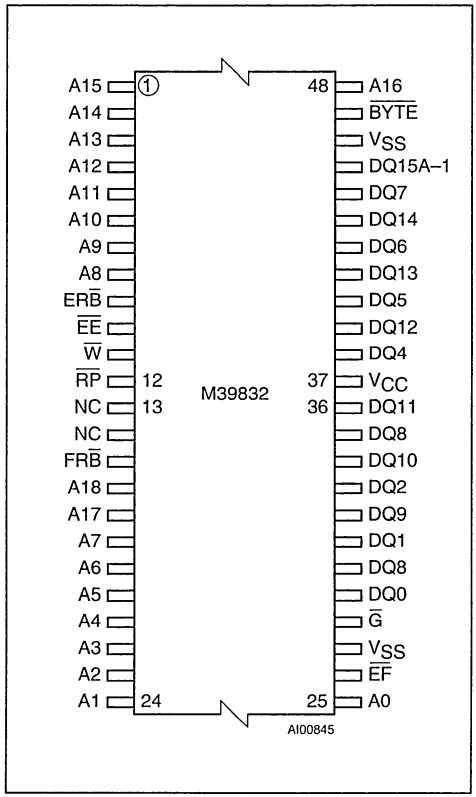
DESCRIPTION

The M39832 is a memory device combining Flash and EEPROM into a single chip and using single supply voltage. The memory is mapped in two arrays: 8 Mbit of Flash memory and 256 Kbit of EEPROM memory. Each space is independant for writing, in concurrent mode the Flash Memory can be read while the EEPROM is being written.

An additional 64 bytes of EPROM are One Time Programmable.

The M39832 EEPROM memory array is organized in byte only (regardless on the $\overline{BYTE}$ pin). It may be written by byte or by page of 64 bytes and the integrity of the data can be secured with the help of the Software Data Protection (SDP).

Figure 2. TSOP Pin Connections



Warning: NC = Not Connected.

Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ7	Data Input/Outputs, Commands Input
DQ8-DQ14	Data Input/Outputs
DQ15A–1	Data Input/Outputs or Address Input
$\overline{EE}$	EEPROM Array Enable
$\overline{EF}$	Flash Array Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Block Temporary Unprotect
$\overline{ERB}$	EEPROM Ready/Busy Output
$\overline{FRB}$	Flash Ready/Busy Output
$\overline{BYTE}$	Flash Array Byte/Word Organization
V_{CC}	Supply Voltage
V_{SS}	Ground

DESCRIPTION (cont'd)

The M39832 Flash Memory array can be configured as 1Mb x8 or 512Kb x16 with the $\overline{BYTE}$ input pin. The M39832-T and M39832-B feature asymetrically blocked architecture providing system memory integration. Both M39832-B and M39832-T devices have a Flash array of 19 blocks, one Boot Block of 16 KBytes or 8 KWords, two Parameter Blocks of 8 KBytes or 4 KWords, one Main Block of 32 KBytes or 16 KWords and fifteen Main Blocks of 64 KBytes or 32 KWords. The M39832-T has the Boot Block at the top of the memory address space and the M39832-B locates the Boot Block starting at the bottom. The memory maps are showed in Figures 3A and 3B. Each block can be erased separately,any combination of blocks can be specified for multi-block erase or the entire chip may be erased. The Erase operations are managed automatically. The block erase operation can be suspended in order to read from or program to any block not being ersased, and then resumed. Block protection provides additional data security. Each block can be separately protected or unprotected against Program or Erase on programming equipment. All previously protected blocks can be temporarily unprotected in the application. The Flash memory array is functionally compatible with the M29W800 Single Voltage Flash Memory device.

During a Program or Erase cycle in the Flash array or during a Write in the EEPROM array, status bits available on certain DQn pins provide information on the M39832 internal logic.

PIN DESCRIPTION

Byte/Word Organization Select ($\overline{BYTE}$). The $\overline{BYTE}$ input selects the output configuration for the Flash array: Byte-wide (x8) mode or Word-wide (x16) mode. The EEPROM array and the 64 Bytes OTP Row are always accessed Byte-wide (x8).

When $\overline{BYTE}$ is High, the Word-wide mode is selected for the Flash array (x16) and the data are read and programmed on DQ0-DQ15. The Flash array is accessed with A0-A18 Adrress lines. In this mode, data in the EEPROM array (x8) are read and programmed on DQ0-DQ7 and the array is accessed with A0-A14. The 64 bytes OTP are read and programmed on DQ0-DQ7 and are accessed with A0-A5 and A6 = 0.

When $\overline{BYTE}$ is Low, the Byte-wide mode is selected for the Flash array (x8) and the data are read and

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	–40 to 85	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages	–0.6 to 5	V
V_{CC}	Supply Voltage	–0.6 to 5	V
V_{A9}, V_G, V_{EF} (2)	A9, $\overline{G}$, $\overline{EF}$ Voltage	–0.6 to 13.5	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns

programmed on DQ0-DQ7. In this mode, DQ8-DQ14 are at high impedance and DQ15A–1 is the LSB address bit, making the Flash array to be accessed with A–1-A18 Adress lines. In this mode, data in the EEPROM array (x8) are read and programmed on DQ0-DQ7 and the array is accessed with A–1-A13. The 64 bytes OTP are read and programmed on DQ0-DQ7 and are accessed with A-1 - A4 and A6 = 0.

Address Inputs (A0-A18). The address inputs for the memory array are latched during a write operation on the falling edge at Chip Enable ($\overline{EE}$ or $\overline{EF}$) or Write Enable $\overline{W}$. In Word-wide organisation the address lines are A0-A18, in Byte-wide organisation DQ15A–1 acts as an additional LSB address line. When A9 is raised to V_{ID}, either a Read Electronic Signature Manufacturer or Device Code, Block Protection Status or a Write Block Protection or Block Unprotection is enabled depending on the combination of levels on A0, A1, A6, A12 and A15.

Data Input/Output (DQ0-DQ7). These Inputs/Outputs are used in the Byte-wide and Word-wide organisations. The input is data to be programmed in the memory array or a command to be written. Both are latched on the rising edge of Chip Enable ($\overline{EE}$ or $\overline{EF}$) or Write Enable $\overline{W}$. The output is data from the Memory Array, the Electronic Signature Manufacturer or Device codes, the Block Protection Status or the Status register Data Polling bit DQ7, the Toggle Bits DQ6 and DQ2, the Error bit DQ5 or the Erase Timer bit DQ3. Outputs are valid when Chip Enable ($\overline{EE}$ or $\overline{EF}$) and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled and when $\overline{RP}$ is at a Low level.

Data Input/Outputs (DQ8-DQ14 and DQ15A–1). These Inputs/Outputs are additionally used in the Word-wide organisation. When $\overline{BYTE}$ is High DQ8-DQ14 and DQ15A–1 act as the MSB of the Data Input or Output, functioning as described for DQ0-DQ7 above, and DQ8 - DQ15 are 'don't care' for command inputs or status outputs. When $\overline{BYTE}$ is Low, DQ8-DQ14 are high impedance, DQ15A–1 is the Address A–1 input.

Memory Array Enable ($\overline{EE}$ and $\overline{EF}$). The Memory Array Enable ($\overline{EE}$ or $\overline{EF}$) activates the memory control logic, input buffers, decoders and sense amplifiers. When the $\overline{EE}$ input is driven high, the EEPROM memory array is not selected; when the $\overline{EF}$ input is driven high, the Flash memory array is not selected. Attempts to access both EEPROM and Flash arrays ($\overline{EE}$ low and $\overline{EF}$ low) are forbidden. Switching between the two memory array enables ($\overline{EE}$ and $\overline{EF}$) must not be made on the same clock cycle, a delay of greater than t_{EHFL} must be inserted.
The M39832 is in standby when both $\overline{EF}$ and $\overline{EE}$ are High (when no internal Erase or programming is running). The power consumption is reduced to the standby level and the outputs are in the high impedance state, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

After 150ns of inactivity and when the addresses are driven at CMOS levels, the chip automatically enters a pseudo standby mode where consumption is reduced to the CMOS standby value, while the outputs continue to drive the bus.

Output Enable ($\overline{G}$). The Output Enable gates the outputs through the data buffers during a read operation. The data outputs are in the high impedance state when the Output Enable $\overline{G}$ is High.

During Block Protect and Block Unprotect operations, the $\overline{G}$ input must be forced to V_{ID} level (12V + 0.5V) (for Flash memory array only).

Figure 3A. Top Boot Block Memory Map and Block Address Table

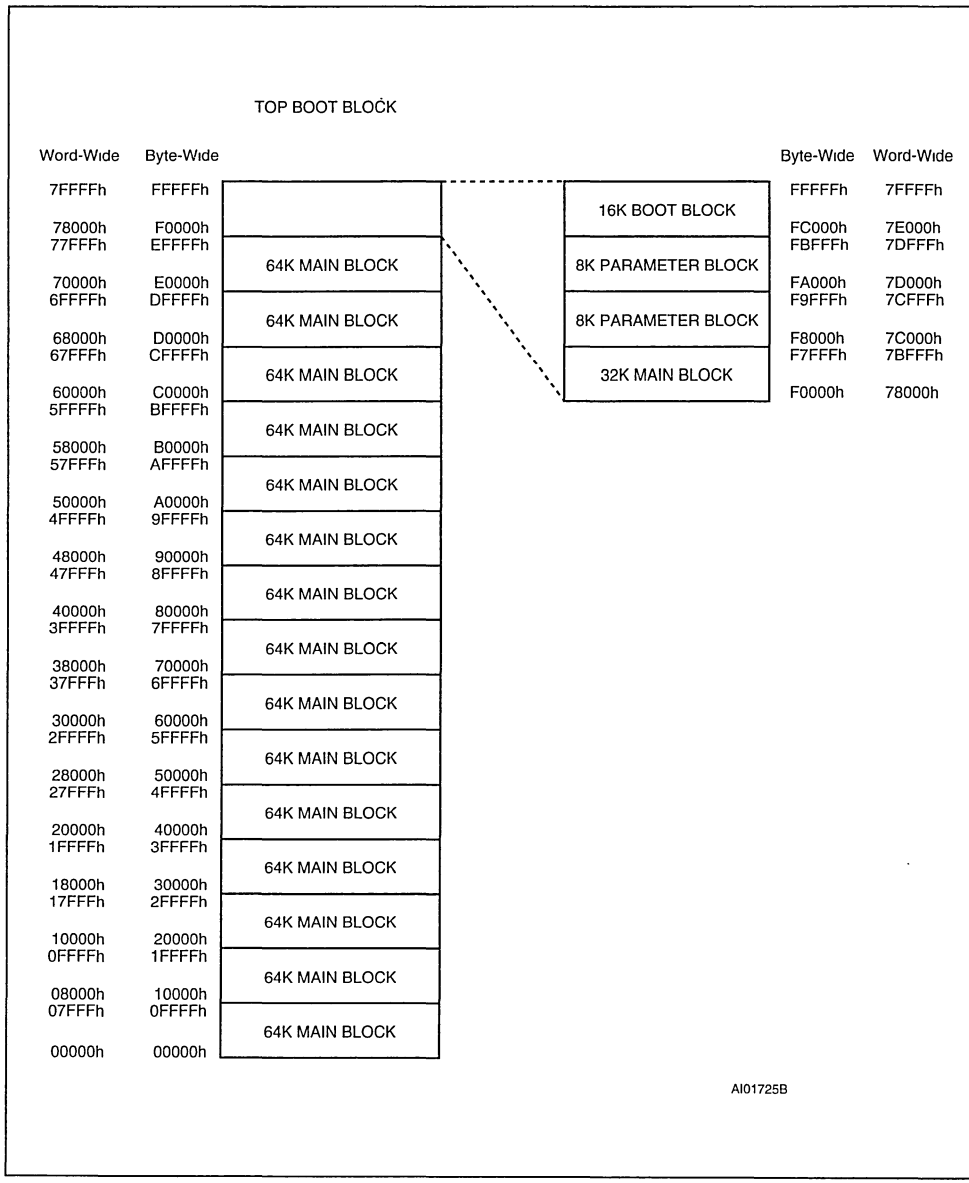


Figure 3B. Bottom Boot Block Memory Map and Block Address Table

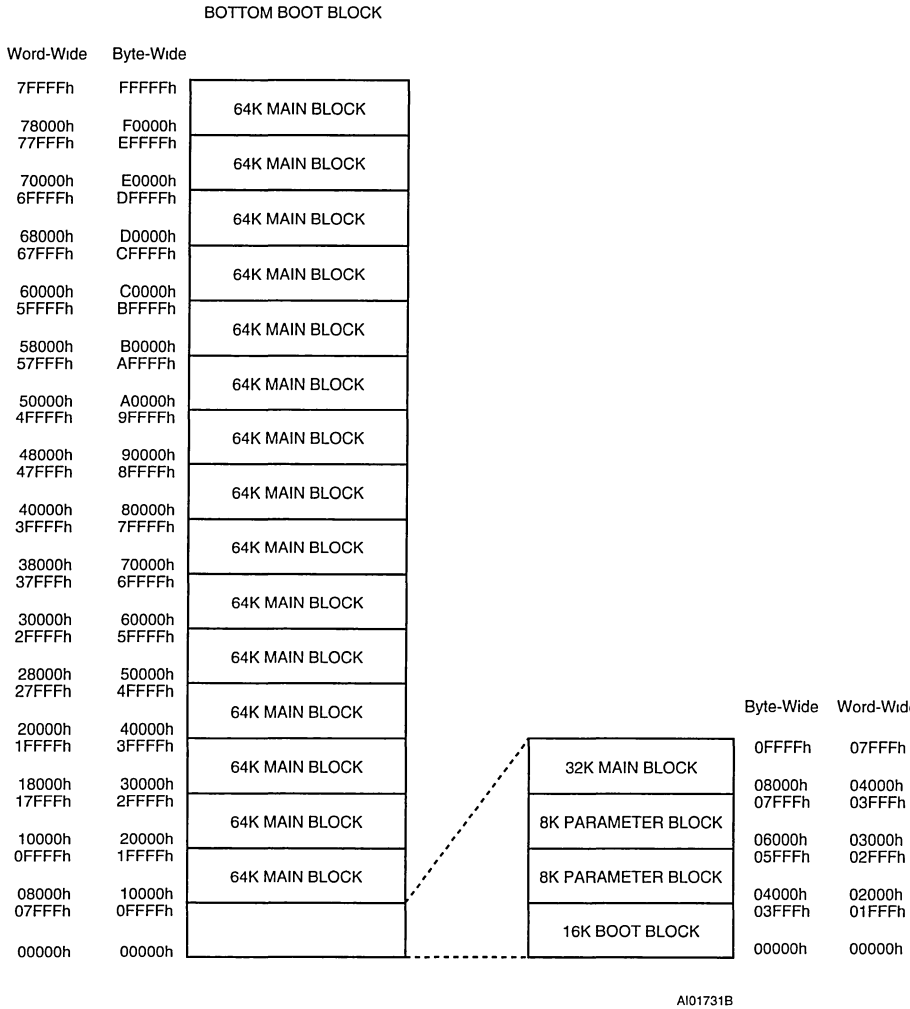


Table 3A. M39832-T Block Address Table

Address Range (x8)	Address Range (x16)	A18	A17	A16	A15	A14	A13	A12
00000h-0FFFFh	00000h-07FFFh	0	0	0	0	X	X	X
10000h-1FFFFh	08000h-0FFFFh	0	0	0	1	X	X	X
20000h-2FFFFh	10000h-17FFFh	0	0	1	0	X	X	X
30000h-3FFFFh	18000h-1FFFFh	0	0	1	1	X	X	X
40000h-4FFFFh	20000h-27FFFh	0	1	0	0	X	X	X
50000h-5FFFFh	28000h-2FFFFh	0	1	0	1	X	X	X
60000h-6FFFFh	30000h-37FFFh	0	1	1	0	X	X	X
70000h-7FFFFh	38000h-3FFFFh	0	1	1	1	X	X	X
80000h-8FFFFh	40000h-47FFFh	1	0	0	0	X	X	X
90000h-9FFFFh	48000h-4FFFFh	1	0	0	1	X	X	X
A0000h-AFFFFh	50000h-57FFFh	1	0	1	0	X	X	X
B0000h-BFFFFh	58000h-5FFFFh	1	1	1	1	X	X	X
C0000h-CFFFFh	60000h-67FFFh	1	1	0	0	X	X	X
D0000h-DFFFFh	68000h-6FFFFh	1	1	0	1	X	X	X
E0000h-EFFFFh	70000h-77FFFh	1	1	1	0	X	X	X
F0000h-F7FFFh	78000h-7BFFFh	1	1	1	1	0	X	X
F8000h-F9FFFh	7C000h-7CFFFh	1	1	1	1	1	0	0
FA000h-FBFFFh	7D000h-7DFFFh	1	1	1	1	1	0	1
FC000h-FFFFFh	7E000h-7FFFFh	1	1	1	1	1	1	X

Table 3B. M39832-B Block Address Table

Address Range (x8)	Address Range (x16)	A18	A17	A16	A15	A14	A13	A12
00000h-03FFFh	00000h-01FFFh	0	0	0	0	0	0	X
04000h-05FFFh	02000h-02FFFh	0	0	0	0	0	1	0
06000h-07FFFh	03000h-03FFFh	0	0	0	0	0	1	1
08000h-0FFFFh	04000h-07FFFh	0	0	0	0	1	X	X
10000h-1FFFFh	08000h-0FFFFh	0	0	0	1	X	X	X
20000h-2FFFFh	10000h-17FFFh	0	0	1	0	X	X	X
30000h-3FFFFh	18000h-1FFFFh	0	0	1	1	X	X	X
40000h-4FFFFh	20000h-27FFFh	0	1	0	0	X	X	X
50000h-5FFFFh	28000h-2FFFFh	0	1	0	1	X	X	X
60000h-6FFFFh	30000h-37FFFh	0	1	1	0	X	X	X
70000h-7FFFFh	38000h-3FFFFh	0	1	1	1	X	X	X
80000h-8FFFFh	40000h-47FFFh	1	0	0	0	X	X	X
90000h-9FFFFh	48000h-4FFFFh	1	0	0	1	X	X	X
A0000h-AFFFFh	50000h-57FFFh	1	0	1	0	X	X	X
B0000h-BFFFFh	58000h-5FFFFh	1	0	1	1	X	X	X
C0000h-CFFFFh	60000h-67FFFh	1	1	0	0	X	X	X
D0000h-DFFFFh	68000h-6FFFFh	1	1	0	1	X	X	X
E0000h-EFFFFh	70000h-77FFFh	1	1	1	0	X	X	X
F0000h-FfFFFh	78000h-7FFFFh	1	1	1	1	X	X	X

Table 4. Basic Operations

$\overline{EF}$	$\overline{EE}$	$\overline{G}$	$\overline{W}$	Operation
V_{IL}	V_{IH}	V_{IL}	V_{IH}	Read in Flash Array
V_{IH}	V_{IL}	V_{IL}	V_{IH}	Read in EEPROM Array
V_{IL}	V_{IH}	V_{IH}	V_{IL}	Write in Flash Array
V_{IH}	V_{IL}	V_{IH}	V_{IL}	Write in EEPROM Array
V_{IL}	V_{IH}	V_{IH}	V_{IH}	Output Disable, DQn = Hi-Z
V_{IH}	V_{IL}	V_{IH}	V_{IH}	Output Disable, DQn = Hi-Z
V_{IH}	V_{IH}	X	X	Standby, DQn = Hi-Z

Note: X = V_{IL} or V_{IH}.

Write Enable ($\overline{W}$). Addresses are latched on the falling edge of $\overline{W}$, and Data Inputs are latched on the rising edge of $\overline{W}$.

EEPROM Ready/Busy ($ER\overline{B}$). The EEPROM Ready/Busy pin outputs the status of the device when the EEPROM memory array is under the write condition

- $ER\overline{B}$ = '0': internal writing is in process,
- $ER\overline{B}$ = '1': no internal writing in in process.

This status pin can be used when reading (or fetching opcodes) in the Flash memory array.

The EEPROM Ready/Busy output uses an open drain transistor, allowing therefore the use of the M39832 in multi-memory applications with all Ready/Busy outputs connected to a single Ready/Busy line (OR-wired with an external pull-up resistor).

Flash Ready/Busy ($FR\overline{B}$). Flash Ready/Busy is an open-drain output and gives the internal state of Flash array. When $FR\overline{B}$ is Low, the Flash array is Busy with a Program or Erase operation and it will not accept any additional program or erase instructions except the Erase Suspend instruction. When $FR\overline{B}$ is High, the Flash array is ready for any Read, Program or Erase operation. The $FR\overline{B}$ will also be High when the Flash array is put in Erase Suspend or Standby modes.

Reset/Block Temporary Unprotect Input ($\overline{RP}$). The $\overline{RP}$ Input provides hardware reset of the Flash array and temporary unprotection of the protected Flash block(s). Reset of the Flash array is acheived by pulling $\overline{RP}$ to V_{IL} for at least t_{PLPX}. When the reset pulse is given while the Flash array is in Read or Standby modes, it will be available for new operations in t_{PHEL} after the rising edge of $\overline{RP}$. If the Flash array is in Erase, Erase Suspend or Program modes the reset will take t_{PLYH} during which the $FR\overline{B}$ signal will be held at VIL. The end of the Flash array reset will be indicated by the rising edge of $FR\overline{B}$. A hardware reset during an Erase or Program operation will corrupt the data being programmed or the block(s) being erased. See Table 14 and Figure 9. Temporary block unprotection is made by holding $\overline{RP}$ at V_{ID}. In this condition, previously protected blocks can be programmed or erased. The transition of $\overline{RP}$ from V_{IH} to V_{ID} must be slower than t_{PHPHH}. See Table 15 and Figure 9. When $\overline{RP}$ is returned from V_{ID} to V_{IH} all blocks temporarily unprotected will be again protected.

OPERATIONS

An operation is defined as the basic decoding of the logic level applied to the control input pins ($\overline{EF}$, $\overline{EE}$, $\overline{G}$, $\overline{W}$) and the specified voltages applied on the relevant address pins. These operations are detailed in Table 3.

Read. Both Chip Enable and Output Enable (that is $\overline{EF}$ and $\overline{G}$ or $\overline{EE}$ and $\overline{G}$) must be low in order to read the output of the memory.

Read operations are used to output the contents from the Flash or EEPROM array, the Manufacturer identifier, the Flash Block protection Status, the Flash Identifier, the EEPROM identifier or the OTP row content.

Notes:

- The Chip Enable input mainly provides power control and should be used for device selection. The Output Enable input should be used to gate data onto the output in combination with active $\overline{EF}$ or $\overline{EE}$ input signals.
- The data read depends on the previous instruction entered into the memory.

Table 5A. Flash Instructions ($\overline{EF}$=0, $\overline{EE}$=1)

Mne.	Instr.	Cyc.			1st Cyc.	2nd Cyc.	3rd Cyc.	4th Cyc.	5th Cyc.	6th Cyc.	7th Cyc.
RD (2,4)	Read/Reset Memory Array	1+	Addr. (3,7)		X	Read Memory Array until a new write cycle is initiated.					
			Data		F0h						
		3+	Addr. (3,7)	Byte	AAAAh	5555h	AAAAh	Read Memory Array until a new write cycle is initiated.			
				Word	5555h	2AAAh	5555h				
			Data		AAh	55h	F0h				
AS (4)	Auto Select	3+	Addr. (3,7)	Byte	AAAAh	5555h	AAAAh	Read Electronic Signature or Block Protection Status until a new write cycle is initiated. See Note 5 and 6.			
				Word	5555h	2AAAh	5555h				
			Data		AAh	55h	90h				
PG	Program	4	Addr. (3,7)	Byte	AAAAh	5555h	AAAAh	Program Address	Read Data Polling or Toggle Bit until Program completes.		
				Word	5555h	2AAAh	5555h				
			Data		AAh	55h	A0h	Program Data			
BE	Block Erase	6	Addr. (3,7)	Byte	AAAAh	5555h	AAAAh	AAAAh	5555h	Block Address	Additional Block (8)
				Word	5555h	2AAAh	5555h	5555h	2AAAh		
			Data		AAh	55h	80h	AAh	55h	30h	30h
FAE	Flash Array Erase	6	Addr. (3,7)	Byte	AAAAh	5555h	AAAAh	AAAAh	5555h	AAAAh	Note 9
				Word	5555h	2AAAh	5555h	5555h	2AAAh	5555h	
			Data		AAh	55h	80h	AAh	55h	10h	
ES (10)	Erase Suspend	1	Addr. (3,7)		X	Read until Toggle stops, then read all the data needed from any Block(s) not being erased then Resume Erase.					
			Data		B0h						
ER	Erase Resume	1	Addr. (3,7)		X	Read Data Polling or Toggle Bits until Erase completes or Erase is suspended another time					
			Data		30h						

Notes: 1. Commands not interpreted in this table will default to read array mode.
2. A wait of t_{PLYH} is necessary after a Read/Reset command if the memory was in an Erase or Program mode before starting any new operation (see Table 14 and Figure 9).
3. X = Don't Care.
4. The first cycles of the RD or AS instructions are followed by read operations. Any number of read cycles can occur after the command cycles.
5. Signature Address bits A0, A1, at V_{IL} will output Manufacturer code (20h). Address bits A0 at V_{IH} and A1, at V_{IL} will output Flash code.
6. Block Protection Address: A0, at V_{IL}, A1 at V_{IH} and A15-A18 within the Block will output the Block Protection status
7. For Coded cycles address inputs A11-A18 are don't care.
8. Optional, additional Blocks addresses must be entered within the erase timeout delay after last write entry, timeout status can be verified through DQ3 value (see Erase Timer Bit DQ3 description) When full command is entered, read Data Polling or Toggle bit until Erase is completed or suspended
9. Read Data Polling, Toggle bits or $\overline{FRB}$ until Erase completes.
10. During Erase Suspend, Read and Data Program functions are allowed in blocks not being erased.

Table 5B. EEPROM Instructions ($\overline{EE}$=0, $\overline{EF}$=1)

Mne.	Instr.	Cyc.			1st Cyc.	2nd Cyc.	3rd Cyc.	4th Cyc.	5th Cyc.	6th Cyc.	7th Cyc.
WOTP (2)	Write OTP Row	>3	Addr.	Byte	5555h	2AAAh	5555h	Addr 1	Addr 2	Addr 3	Addr 4
				Word	5555h	2AAAh	5555h				
			Data		AAh	55h	B0h	Byte 1	Byte 2	Byte 3	Byte 4
ROTP (2)	Read OTP Row	>3	Addr.	Byte	5555h	2AAAh	5555h	Addr 1	Addr 2	Addr 3	Addr 4
				Word	5555h	2AAAh	5555h				
			Data		AAh	55h	90h	Byte 1	Byte 2	Byte 3	Byte 4
RT	Return from OTP Read	1	Addr.		X (1)						
			Data		F0h						
SSDP (4)	SDP Enable	≥3	Addr.	Byte	5555h	2AAAh	5555h				
				Word	5555h	2AAAh	5555h				
			Data		AAh	55h	A0h				
SSDP (5)	SDP Disable	6	Addr.	Byte	5555h	2AAAh	5555h	5555h	2AAAh	5555h	
				Word	5555h	2AAAh	5555h	5555h	2AAAh	5555h	
			Data		AAh	55h	80h	AAh	55h	20h	

Notes: 1. X = Don't Care.
2. Once the WOTP has been initiated (first 3 Cycles), from 1 up to 64 bytes can be written in one single write cycle (See Write OTP chapter in following pages).
3. Once the ROTP has been initiated (first 3 Cycles), from 1 up to 64 bytes of the OTP can be read (See Read OTP chapter in following pages). The RT (Return) instruction MUST be sent to the device to exit ROTP mode.
4. Once SDP is set (SSDP instruction sent once), it is necessary to send SSDP prior to any byte or page to be written in the EEPROM array (See Figure 4 and EEPROM array Software Data Protection chapter in following pages).
5. See Figure 5 and EEPROM array Software Data Protection chapter in following pages.

Table 6. User Bus Operations (1)

Operation	$\overline{EE}$	$\overline{EF}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$\overline{BYTE}$	A0	A1	A6	A9	A12	A15	DQ15 A–1	DQ8-DQ14	DQ0-DQ7
Block Protection(2,4)	V_{IH}	V_{IL}	V_{ID}	V_{IL} Pulse	V_{IH}	X	X	X	X	V_{ID}	X	X	X	X	X
Blocks Unprotection(4)	V_{IH}	V_{ID}	V_{ID}	V_{IL} Pulse	V_{IH}	X	X	X	X	V_{ID}	V_{IH}	V_{IH}	X	X	X
Block Protection Verify(2,4)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	V_{ID}	A12	A15	X	X	Block Protect Status (3)
Block Unprotection Verify(2,4)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	V_{IH}	V_{ID}	A12	A15	X	X	Block Protect Status (3)
Block Temporary Unprotection	V_{IH}	X	X	X	V_{ID}	X	X	X	X	X	X	X	X	X	X
Write the EEPROM Identifier (5)	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	A0	A1	V_{IL}	V_{ID}	X	X	A–1	X	64 Bytes User Defined
			V_{IH}	V_{IL}	V_{IH}	V_{IH}	A0	A1	V_{IL}	V_{ID}	X	X	X	X	64 Bytes User Defined
Read the EEPROM Identifier (5)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	A0	A1	V_{IL}	V_{ID}	X	X	A–1	X	64 Bytes User Defined
			V_{IL}	V_{IH}	V_{IH}	V_{IH}	A0	A1	V_{IL}	V_{ID}	X	X	X	X	64 Bytes User Defined

Notes: 1. X = V_{IL} or V_{IH}
2. Block Address must be given on A12-A18 bits.
3. See Table 8.
4. Operation performed on programming equipment.
5. The 65 Bytes User defined EEPROM Identifier are accessed on DQ0-DQ7 with A0 to A5 when $\overline{BYTE}$ = 1 (x16) or with A–1 to A4 when $\overline{BYTE}$ = 0 (x8)

Table 7. Read Electronic Signature (following AS instruction or with A9 = V_{ID})

Org.	Code	Device	$\overline{EE}$	$\overline{EF}$	$\overline{G}$	$\overline{W}$	$\overline{BYTE}$	A0	A1	Other Addresses	DQ15 A–1	DQ8-DQ14	DQ0-DQ7
Word-wide	Manufacturer		V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	Don't Care	0	00h	20h
	Flash	M39832-T	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	Don't Care	0	00h	D7h
		M39832-B	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	Don't Care	0	00h	5Bh
Byte-wide	Manufacturer		V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Don't Care	Don't Care	Hi-Z	20h
	Flash	M39832-T	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Don't Care	Don't Care	Hi-Z	D7h
		M39832-B	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Don't Care	Don't Care	Hi-Z	5Bh

Table 8. Read Block Protection with AS Instruction ($\overline{EF}$ = 0, $\overline{EE}$ = 1)

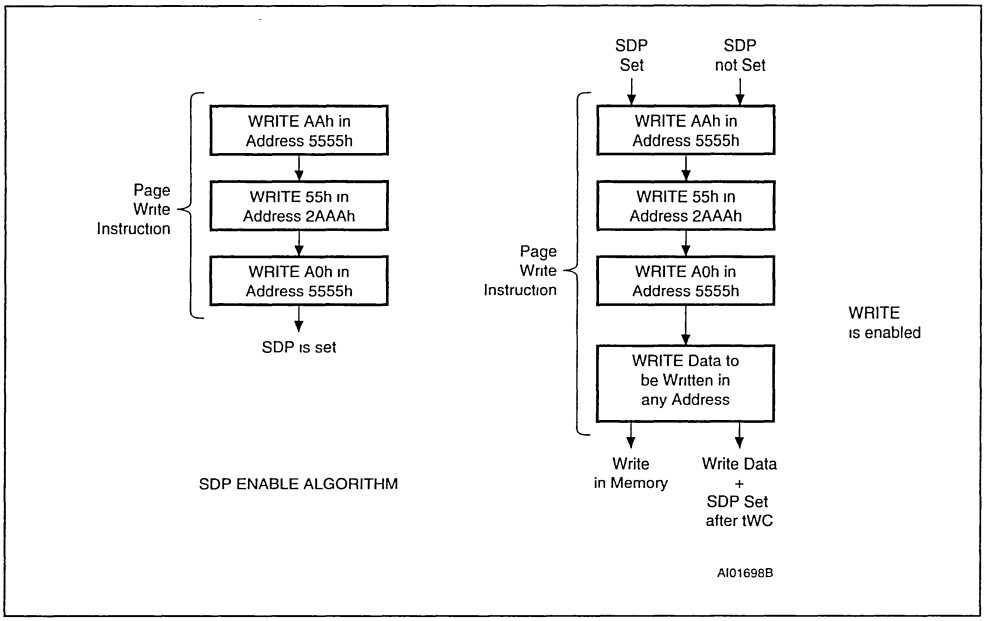
Code	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	A12-A18	Other Addresses	DQ0-DQ7
Protected Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Block Address	Don't Care	01h
Unprotected Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Block Address	Don't Care	00h

Table 9. Status Bit

DQ	Name	Logic Level	Definition	Note
7	Data Polling	'1'	Erase Complete or erase block in Erase Suspend	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.
		'0'	Erase On-going	
		DQ	Program Complete or data of non erase block during Erase Suspend	
		$\overline{DQ}$	Program On-going	
6	Toggle Bit	'-1-0-1-0-1-0-1-'	Erase or Program On-going	Successive reads output complementary data on DQ6 while Programming or Erase operations are on-going. DQ6 remains at constant level when P/E.C. operations are completed or Erase Suspend is acknowledged.
		DQ	Program Complete	
		'-1-1-1-1-1-1-1-1-'	Erase Complete or Erase Suspend on currently addressed block	
5	Error Bit	'1'	Program or Erase Error	This bit is set to '1' in the case of Programming or Erase failure.
		'0'	Program or Erase On-going	
4	Reserved			
3	Erase Time Bit	'1'	Erase Timeout Period Expired	P/E.C. Erase operation has started. Only possible command entry is Erase Suspend (ES).
		'0'	Erase Timeout Period On-going	An additional block to be erased in parallel can be entered to the P/E.C.
2	Toggle Bit	'-1-0-1-0-1-0-1-'	Chip Erase, Erase or Erase Suspend on the currently addressed block. Erase Error due to the currently addressed block (when DQ5 = '1').	Indicates the erase status and allows to identify the erased block
		1	Program on-going, Erase on-going on another block or Erase Complete	
		DQ	Erase Suspend read on non Erase Suspend block	
1	Reserved			
0	Reserved			

Notes: Logic level '1' is High, '0' is Low. -0-1-0-0-0-1-1-1-0- represent bit value in successive Read operations

Figure 4. EEPROM SDP Enable Flowcharts



Write. A Write operation can be used for two goals:

- either write data in the EEPROM memory array
- or enter a sequence of bytes or word composing an instruction.

The reader should note that Programming a Flash byte or word is an instruction (see Instructions paragraph).

Writing data requires:

- the Chip Enable (either $\overline{E}\overline{E}$ or $\overline{E}\overline{F}$) to be Low
- the Write Enable ($\overline{W}$) to be Low with Output Enable (G) High.

Addresses in Flash array (or EEPROM array) are latched on the falling edge of $\overline{W}$ or $\overline{E}\overline{F}$ ($\overline{E}\overline{E}$) whichever occurs last; the data to be written in Flash array (EEPROM array) is latched on the rising edge of $\overline{W}$ or $\overline{E}\overline{F}$ ($\overline{E}\overline{E}$) whichever occurs first.

Specific Read and Write Operations. Device specific data is accessed through operations decoding the V_{ID} level applied on A9 and the logic levels applied on address inputs (A0, A1, A6). These specific operations are:

- Read the Manufacturer identifier
- Read the Flash identifier
- Define and Read the Flash Block protection status
- Read the EEPROM identifier
- Write the EEPROM identifier

Note: The OTP row (64 bytes) is accessed with a specific software sequence detailed in the paragraph "Write in OTP row".

Instructions

An instruction is defined as a sequence of specific Write operations. Each received byte or word is sequentially decoded (and not executed as standard Write operations) and the instruction is executed when the correct number of bytes or word are properly received and the time between two consecutive bytes or words is shorter than the time-out value.

The sequencing of any instruction must be followed exactly, any invalid combination of instruction bytes or word or time-out between two consecutive bytes or word will reset the device logic into a Read memory state (when addressing the Flash array) or directly decoded as a single operation when addressing the EEPROM array.

For efficient decoding of the instruction, the two first bytes or words of an instruction are the coded cycles and are followed by a command confirmation byte or word.

Figure 5. EEPROM SDP disable Flowchart

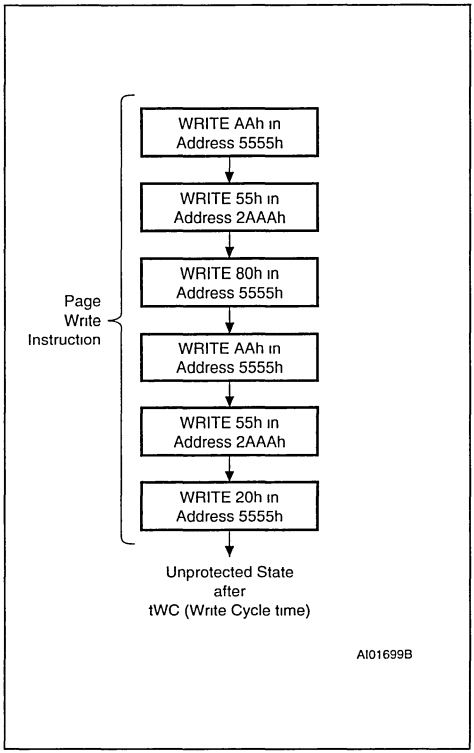
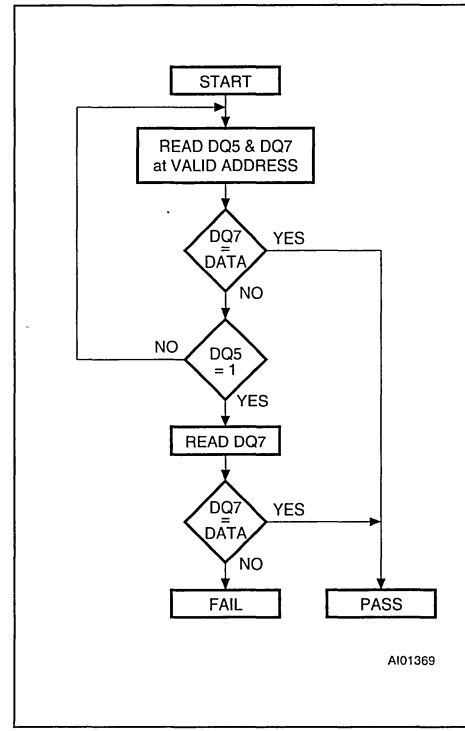


Figure 6. EEPROM and Flash Data Polling Flowchart



READ

Read operations and instructions can be used to:

- read the contents of the Memory Array (Flash and EEPROM)
- read the status bits and identifiers.

Read data (Flash and EEPROM)

Both Chip Enable $\overline{E}$ (or $\overline{EE}$) and Output Enable ($\overline{G}$) must be low in order to read the data from the memory.

Read the Manufacturer Identifier

The manufacturer's identifier can be read with two methods: a Read operation or a Read instruction.

Read Operation. The manufacturer's identifier can be read with a Read operation with specific logic levels applied on A0, A1, A6 and the V_{ID} level on A9 (See Table 7).

Read Instruction. The manufacturer's identifier can also be read with a single read operation immediatly following the AS instruction (See Table 5A and Table 7).

Read the Flash Identifier

The Flash identifier can be read with two methods: a Read operation or a Read instruction.

Read Operation. The Flash identifier can be read with a single Read operation with specific logic levels applied on A0, A1, A6 and the V_{ID} level on A9 (See Table 7).

Read Instruction. The Flash identifier can also be read with a single read operation immediatly following the AS instruction (See Table 5A and Table 7).

Read the EEPROM Identifier

The EEPROM identifier (64 bytes, user defined) can be read with a single Read operation with A6 = '0' and A9 = V_{ID} (See Table 6).

When accessing the 64 Bytes of EEPROM Identifier, the only LSB addresses are decoded. The LSB addresses are A0 to A5 when $\overline{BYTE}$ = '1' (x16) and A–1 to A4 when $\overline{BYTE}$ = '0' (x8). Each Byte of the EEPROM identifier can be individually accessed in read or write mode.

Read the OTP Row

The OTP row is mapped in the EEPROM array ($\overline{EE}$ = '0', $\overline{EF}$ = '1'). Read of the OTP row (64 bytes) is by an instruction (ROTP) composed of three specific Write operations of data bytes at three specific memory locations (each location in a different page) before reading the OTP row content (See Table 5B).

When accessing the OTP row, only the LSB addresses are decoded and A6 must be '0'. The LSB addresses are A0 to A5 when $\overline{BYTE}$ = '1' (x16) and A–1 to A4 when $\overline{BYTE}$ = '0' (x8).

Each Read of the OTP row has to be followed by the (RT) Return instruction (See Table 5B).

Read the Flash Block Protection Status

Reading the Flash block protection status is by a read operation immediatly following the AS instruction (See Table 5A and Table 8). A12-A18 define the Flash block whose protection has to be verified. This Read operation will output a 01h if the Flash block is protected and a 00h if the Flash block is not protected.

The Flash block protection status can also be verified with a single Read operation (see chapter: Flash array specific features), with V_{ID} on A9 (See Table 6 and Table 8).

Read the Status Bits

The M39832 provides several Write operation status flags which may be used to minimize the application write (or erase or program) time. These signals are available on the I/O port bits when programming (or erasing) are in progress. It should be noted that the Ready/Busy pins also reflects the status of the EEPROM Write and the Flash Programming/Erasing.

Data Polling flag, DQ7. When Erasing or Programming into the Flash block (or when Writing into the EEPROM block), bit DQ7 outputs the complement of the bit being entered for Programming/Writing on DQ7. Once the Program instruction or the Write operation is performed, the true logic value is read on DQ7 (in a Read operation).

Flash memory block specific features:

- Data Polling is effective after the fourth W pulse (for programming) or after the sixth W pulse (for Erase). It must be performed at the address being programmed or at an address within the Flash sector being erased.
- During an Erase instruction, DQ7 outputs a '0'. After completion of the instruction, DQ7 will output the last bit programmed (that is a '1' after erasing).
- if the byte to be programmed is in a protected Flash sector, the instruction is ignored.
- If all the Flash sectors to be erased are protected, DQ7 will be set to '0' for about 100µs, and then return to the previous addressed byte. No erasure will be performed.
- if all sectors are protected, a Bulk Erase instruction is ignored.

Toggle flag, DQ6. The M39832 also offers another way for determining when the EEPROM write or the Flash memory Program instruction is completed. During the internal Write operation, the DQ6 will toggle from '0' to '1' and '1' to '0' on subsequent attempts to read any byte of the memory, when either $\overline{G}$, $\overline{EE}$ or $\overline{EF}$ is low.

When the internal cycle is completed the toggling will stop and the data read on DQ0-DQ7 is the addressed memory byte. The device is now accessible for a new Read or Write operation. The operation is completed when two successive reads yield the same output data.

Flash memory block specific features:

a. The Toggle bit is effective after the fourth $\overline{W}$ pulse (for programming) or after the sixth $\overline{W}$ pulse (for Erase).

b. If the byte to be programmed belongs to a protected Flash sector, the instruction is ignored and:

- if all the Flash sectors selected for erasure are protected, DQ6 will toggle to '0' for about 100µs, and then return to the previous addressed byte.
- if all sectors are protected, the Bulk Erase instruction is ignored.

Figure 7A. Data Toggle Flowchart

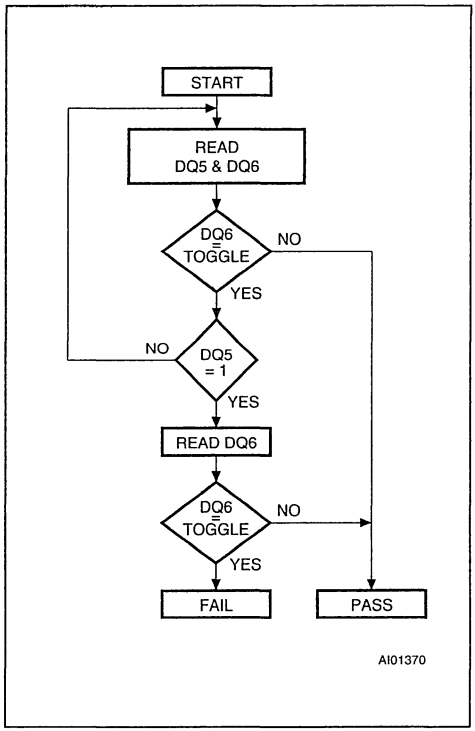
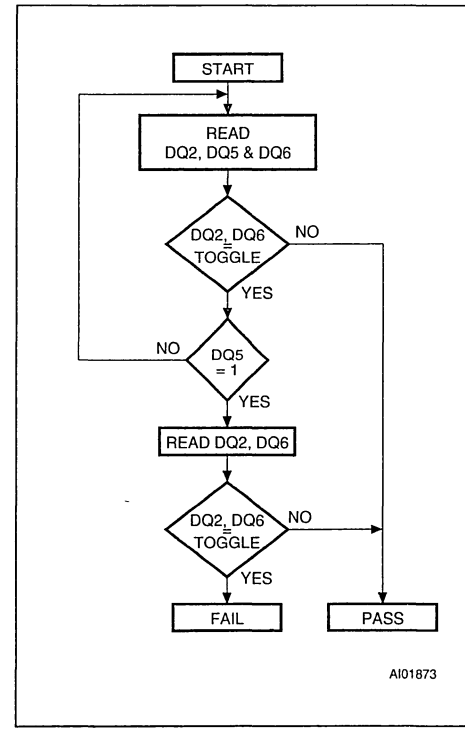


Figure 7B. Flash ata Toggle Flowchart



Toggle Bit, DQ2 (Flash array only). This toggle bit, together with DQ6, can be used to determine the device status during the Erase operations. It can also be used to identify the block being erased. During Erase or Erase Suspend a read from a block being erased will cause DQ2 to toggle. A read from a block not being erased will set DQ2 to '1' during erase and to DQ2 during Erase Suspend. During Flash Array Erase, a read operation will cause DQ2 to toggle as all blocks are being erased. DQ2 will be set to '1' during program operation and when erase is complete. After erase completion and if the error bit DQ5 is set to '1', DQ2 will toggle if the faulty block is addressed.

Error flag, DQ5 (Flash block only). This bit is set to '1' by the internal logic when there is a failure of programming, block erase, or chip erase that results in invalid data in the memory block. In case of an error in block erase or program, the block in which the error occured or to which the programmed data belongs, must be discarded. The DQ5 failure condition will also appear if a user tries to program a '1' to a location that is previously programmed to '0'. Other Blocks may still be used. The error bit resets after a Read/Reset (RD) instruction. In case of success of Program or Erase, the error bit will be set to '0' . when A0 is High with A1 Low.

Erase Timer Bit, DQ3 (Flash array only). This bit is set to '0' by internal logic when the last block Erase command has been entered to the Command Interface and it is awaiting the Erase start. When the erase timeout period is finished, after 50ms to 90ms, DQ3 returns to '1'.

WRITE a BYTE (or a PAGE) in EEPROM

It should be noticed that writing in the EEPROM array is an operation, it is not an instruction (as for Programming a byte in the Flash array).

Write a Byte in EEPROM Array

A write operation is initiated when Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output

Enable $\overline{G}$ High. Addresses are latched on the falling edge of $\overline{W}$, $\overline{EE}$ whichever occurs last.

Once initiated, the write operation is internally timed until completion, that is during a time tw.

The status of the write operation can be found by reading the Data Polling and Toggle bits (as detailed in the READ chapter) or the $\overline{ERB}$ output. This Ready/Busy output is driven low from the write of the byte being written until the completion of the internal Write sequence.

Write a Page in EEPROM Array

The Page write allows up to 64 bytes within the same EEPROM page to be consecutively latched into the memory prior to initiating a programming cycle. All bytes must be located in a single page address, that is A6-A14 when $\overline{BYTE}$ is high (x16) or A5-A13 when $\overline{BYTE}$ is low (x8) must be the same for all bytes. Once initiated, the Page write operation is internally timed until completion, that is during a time t_{WC}.

The status of the write operation can be seen by reading the Data Polling and Toggle bits (as detailed in the READ chapter) or the $\overline{ERB}$ output. This Ready/Busy output is driven low from the write of the first byte to be written until the completion of the internal Write sequence.

A Page write is composed of successive Write operations which must be sequenced within a time period (between two consecutive Write operations) that is smaller than the t_{WLWL} value. If this period of time exceeds the t_{WLWL} value, the internal programming cycle will start.

EEPROM Array Software Data Protection

A protection instruction allows the user to inhibit all write modes to the EEPROM array: the Software Data Protection (referenced as SDP in the following). The SDP feature is useful for protecting the EEPROM memory from inadvertent write cycles that may occur during uncontrolled bus conditions.

The M39832 is shipped as standard in the unprotected state meaning that the EEPROM memory contents can be changed by the user. After the SDP enable instruction, the device enters the Protect Mode where no further write operations have any effect on the EEPROM memory contents.

The device remains in this mode until a valid SDP disable instruction is received whereby the device reverts to the unprotected state.

To enable the Software Data Protection, the device has to be written (with a Page Write) with three specific data bytes at three specific memory locations (each location in a different page) as shown in Figure 4 and Table 5B. This sequence provides an unlock key to enable the write action, and, at the same time, SDP continues to be set. Any further Write in EEPROM when the SDP is set will use this same sequence of three specific data bytes at three specific memory locations followed by the bytes to write. The first SDP enable sequence can be directly followed by the bytes to written.

Similarly, to disable the Software Data Protection the user has to write specific data bytes into six different locations with a Page Write addressing different bytes in different pages, as shown in Figure 5 and Table 5B.

The Software Data Protection state is non-volatile and is not changed by power on/off sequences. The SDP enable/disable instructions set/reset an internal non-volatile bit and therefore will require a write time t_{WC}, This Write operation can be monitored only on the Toggle bit (status bit DQ6) and the $\overline{ERB}$ pin. The Ready/Busy output is driven low from the first byte to be written (that is the first Write AAh, @5555h of the SDP set/reset sequence) until the completion of the internal Write sequence.

Write OTP Row

Writing (only one time) in the OTP row (64 bytes) is enabled by an instruction (WOTP). This instruction is composed of three specific Write operations of data bytes at three specific memory locations (each location in a different page) followed by the the data to store in the OTP row (refer to Table 5B).

When accessing the OTP row, the only LSB addresses are decoded and A6 must be '0'. The LSB addresses are A0 to A5 when $\overline{BYTE}$ = '1' (x16) and A–1 to A4 when $\overline{BYTE}$ = '0' (x8). Once at least one Byte of the OTP row has been written (even with FFh), the whole row becomes Read only.

Write the EEPROM Block Identifier

The EEPROM block identifier (64 Bytes) can be written with a single Write operation with A6 = '0' and the V_{ID} level on A9 (see Table 6). When accessing the 64 Bytes of EEPROM Identifier, the only LSB addresses are decoded. The LSB addresses are A0 to A5 when $\overline{BYTE}$ = '1' (x16) and A-1 to A4 when $\overline{BYTE}$ = '0' (x8). Each Byte of the EEPROM identifier can be individually accessed in read or write mode.

PROGRAM in the Flash ARRAY

It should be noted that writing data into the EEPROM array and the Flash array is not performed in a similar way: the Flash memory requires an instruction (see Instruction chapter) for Erasing and another instruction for Programming one (or more) byte(s) or word(s), the EEPROM memory is directly written with a simple operation (see Operation chapter).

Program (PG) Instruction. This instruction uses four write cycles. Both for Byte-wide configuration and for Word-wide configuration. The Program command A0h is written to address AAAAh in the Byte-wide configuration or to address 5555h in the Word-wide configuration on the third cycle after two Coded cycles. A fourth write operation latches the Address on the falling edge of $\overline{W}$ or $\overline{EF}$ and the Data to be written on the rising edge and starts the internal operation. Read operations output the Status Register bits after the programming has started. Memory programming is made only by writing '0' in place of '1'. Status bits DQ6 and DQ7 determine if programming is on-going and DQ5 allows verification of any possible error. Programming at an address not in blocks being erased is also possible during erase suspend. In this case, DQ2 will toggle at the address being programmed.

Auto Select (AS) Instruction. This instruction uses the two Coded cycles followed by one write cycle giving the command 90h to address AAAAh in the Byte-wide configuration or address 5555h in the Word-wide configuration for command set-up. A subsequent read will output the manufacturer code and the device code or the block protection status depending on the levels of A0 and A1. The manufacturer code is output when the addresses lines A0 and A1 are Low, the Flash code for Top Boot or Bottom Boot is output when A0 is High with A1 Low.

The AS instruction allows access to the block protection status. After giving the AS instruction, A0 is set to V_{IL} with A1 at V_{IH}, while A12-A18 define the address of the block to be verified. A read in these conditions will output a 01h if the block is protected and a 00h if the block is not protected.

The ERASE in the Flash ARRAY

Flash Array Erase (FAE) Instruction. This instruction uses six write cycles. The Erase Set-up command 80h is written to address AAAAh in the Byte-wide configuration or the address 5555h in the Word-wide configuration on the third cycle after the two Coded cycles. The Flash Array Erase Confirm command 10h is similarly written on the sixth cycle after another two Coded cycles. If the second command given is not an erase confirm or if the Coded cycles are wrong, the instruction aborts and the device is reset to Read Array. It is not necessary to program the array with 00h first as it will be done automatically before erasing it to FFh. Read operations after the sixth rising edge of $\overline{W}$ or $\overline{EF}$ output the Status Register bits. During the execution of the erase, Data Polling bit DQ7 returns '0', then '1' on completion. The Toggle bits DQ2 and DQ6 toggle during erase operation and stop when erase is completed. After completion, the Status Bit DQ5 returns '1' if there has been an Erase Failure.

Block Erase (BE) Instruction. This instruction uses a minimum of six write cycles. The Erase Set-up command 80h is written to address AAAh in the Byte-wide configuration or address 5555h in the Word-wide configuration on third cycle after the two Coded cycles. The Block Erase Confirm command 30h is similarly written on the sixth cycle after another two Coded cycles. During the input of the second command an address within the block to be erased is given and latched into the memory. Additional block Erase Confirm commands and block addresses can be written subsequently to erase other blocks in parallel, without further Coded cycles. The erase will start after the erase timeout period (see Erase Timer Bit DQ3 description). Thus, additional Erase Confirm commands for other blocks must be given within this delay. The input of a new Erase Confirm command will restart the timeout period. The status of the internal timer can be monitored through the level of DQ3, if DQ3 is '0' the Block Erase Command has been given and the timeout is running, if DQ3 is '1', the timeout has expired and the Block(s) are being erased. If the second command given is not an erase confirm or if the Coded cycles are wrong, the instruction aborts, and the device is reset to Read Array. It is not necessary to program the block with 00h as it will be done automatically before erasing it to FFh. Read operations after the sixth rising edge of $\overline{W}$ or $\overline{EF}$ output the Status Register bits.

During the execution of the erase , the memory accepts only the Erase Suspend ES and Read/Reset RD instructions. Data Polling bit DQ7 returns '0' while the erasure is in progress and '1' when it has completed. The Toggle bit DQ2 and DQ6 toggle during the erase operation. They stop when erase is completed. After completion the Status bit DQ5 returns '1' if there has been an erase failure. In such a situation, the Toggle bit DQ2 can be used to determine which block is not correctly erased. In the case of erase failure, a Read/Reset RD instruction is necessary in order to reset the memory.

Figure 8. Block Protection Flowchart

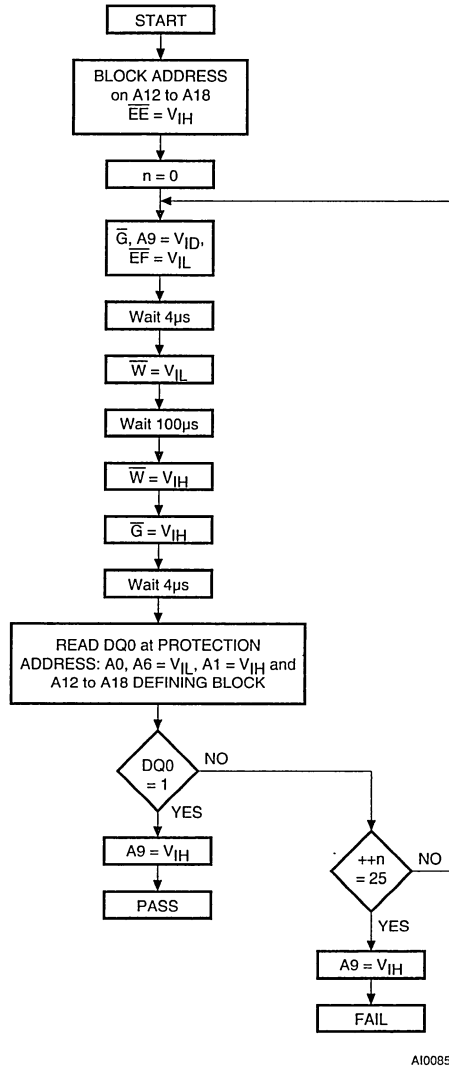
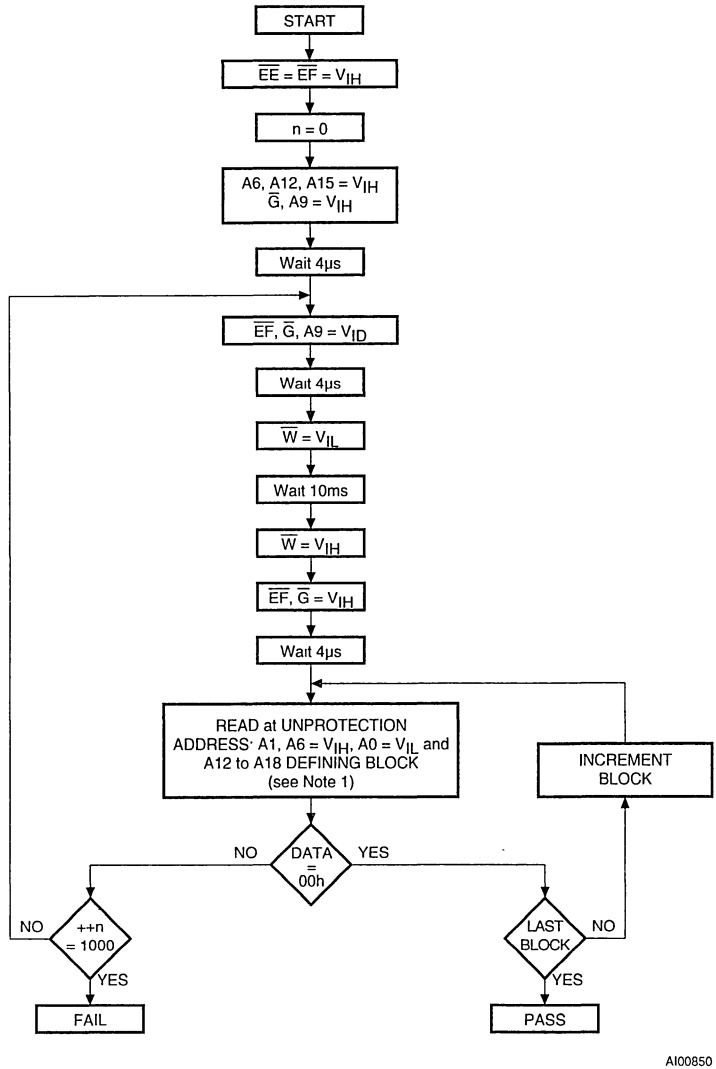


Figure 9. Block Unprotecting Flowchart



Note: 1 A6 is kept at V_{IH} during unprotection algorithm in order to secure best unprotection verification. During all other protection status reads, A6 must be kept at V_{IL}.

Table 10. AC Measurement Conditions

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0.V to V_{CC}
Input and Output Timing Ref. Voltages	V_{CC} / 2

Figure 10. AC Testing Input Output Waveform

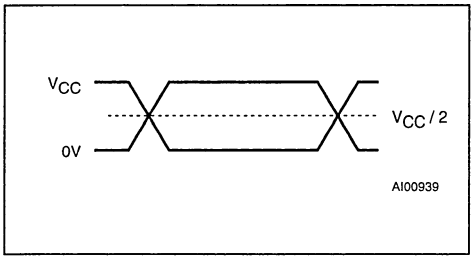


Figure 11. Output AC Testing Load Circuit

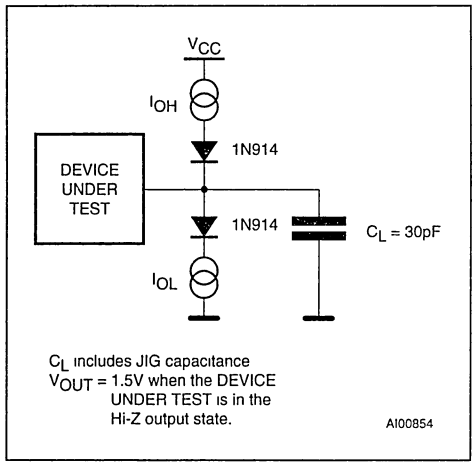


Table 11. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested

Erase Suspend (ES) Instruction. The Block Erase operation may be suspended by this instruction which consists of writing the command B0h without any specific address. No Coded cycles are required. It permits reading of data from another block and programming in another block while an erase operation is in progress. Erase suspend is accepted only during the Block Erase instruction execution. Writing this command during Erase timeout will, in addition to suspending the erase, terminate the timeout. The Toggle bit DQ6 stops toggling when erase is suspended. The Toggle bits will stop toggling between 0.1ms and 15ms after the Erase Suspend (ES) command has been written. The device will then automatically be set to Read Memory Array mode. When erase is suspended, a Read from blocks being erased will output DQ2 toggling and DQ6 at '1'. A Read from a block not being erased returns valid data. During suspension the memory will respond only to the Erase Resume ER and the Program PG instructions.

A Program operation can be initiated during erase suspend in one of the blocks not being erased. It will result in both DQ2 and DQ6 toggling when the data is being programmed. A Read/Reset command will definitively abort erasure and result in invalid data in the blocks being erased.

Erase Resume (ER) Instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command 30h, at any address, and without any Coded cycles.

FLASH ARRAY SPECIFIC FEATURES

Block Protection (See Figure 8). Each block can be separately protected against Program or Erase on programming equipment. Block protection provides additional data security, as it disables all program or erase operations. This mode is activated when both A9 and G are raised to V_{ID} and an address in the block is applied on A12-A18. Block protection is initiated on the edge of W falling to V_{IL}. Then after a delay of 100ms, the edge of W rising to V_{IH} ends the protection operations. Block protection verify is achieved by bringing G, $\overline{EF}$, A0 and A6 to V_{IL} and A1 to V_{IH}, while W is at V_{IH} and A9 at V_{ID}.

Under these conditions, reading the data output will yield 01h if the block defined by the inputs on A12-A18 is protected. Any attempt to program or erase a protected block will be ignored by the device.

Remarks:

- The Verify operation is a read with a simulated worst case conditions. This allows a guarantee of the retention of the Protection status
- During the application life, the block protection status can be accessed with a regular Read instruction without applying a "high voltage" V_{ID} on A9. This instruction is detailed in Table 5 and Table 8.

Blocks Unprotection (See Figure 9). All protected blocks can be unprotected simultaneously on programming equipment to allow updating of bit contents. All blocks must first be protected before the unprotection operation. Block unprotection is activated when A9, $\overline{G}$ and $\overline{E}$ are at V_{ID} and A12, A15 at V_{IH}. Unprotection is initiated by the edge of $\overline{W}$ falling to V_{IL}. After a delay of 10ms, the unprotection operation will end. Unprotection verify is achieved by bringing $\overline{G}$ and $\overline{E}$ to V_{IL} while A0 is at V_{IL}, A6 and A1 are at V_{IH} and A9 remains at V_{ID}. In these conditions, reading the output data will yield 00h if the block defined by the inputs A12-A18 has been succesfully unprotected. Each block must be separately verified by giving its address in order to ensure that it has been unprotected.

Remarks:

- The Verify operation is a read with a simulated worst case conditions. This allows a guarantee of the retention of the Protection status
- During the application life, the Block protection status can be accessed with a regular Read instruction without "high voltage" V_{ID} on A9. This instruction is detailed in Table 5 and Table 8.

Block Temporary Unprotection. Any previously protected block can be temporarily unprotected in order to change stored data. The temporary unprotection mode is activated by bringing RP to V_{ID}. During the temporary unprotection mode the previously protected blocks are unprotected. A block can be selected and data can be modified by executing the Erase or Program instruction with the RP signal held at V_{ID}. When RP is returned to VIH, all the previously protected blocks are again protected.

Read/Reset (RD) Instruction. The Read/Reset instruction consists of one write cycle giving the command F0h. It can be optionally preceded by the two Coded cycles. Subsequent read operations will read the memory array addressed and output the data read. A wait state of 10ms is necessary after Read/Reset prior to any valid read if the memory was in an Erase mode when the RD instruction is given.

GLOSSARY

Array: EEPROM array (256 Kbit) or Flash array (8 Mbit)

Block: part of the Flash array (See Figure 3A and 3B).

Page: 64 bytes of EEPROM

Write and Program: Writing (into the EEPROM array) and programming (the Flash array is not performed in a similar way:

- the Flash memory requires an instruction (see Instruction chapter) for Erasing and another instruction for Programming one (or more) byte(s) or word(s)
- the EEPROM memory is directly written with a simple operation (see Operation chapter).

SDP: Software Data Protection. Used for protecting the EEPROM array against false Write operations (as in noisy environments).

POWER SUPPLY and CURRENT CONSUMPTION

Power Up. The M39832 internal logic is reset upon a power-up condition to Read memory status. Any Write operation in EEPROM is inhibited during the first 5 ms following the power-up.

Either $\overline{EF}$, $\overline{EE}$ or $\overline{W}$ must be tied to V_{IH} during Power-up for the maximum security of the data contents and to remove the possibility of a byte being written on the first rising edge of $\overline{EF}$, $\overline{EE}$ or $\overline{W}$. Any write cycle initiation is locked when Vcc is below V_{LKO}.

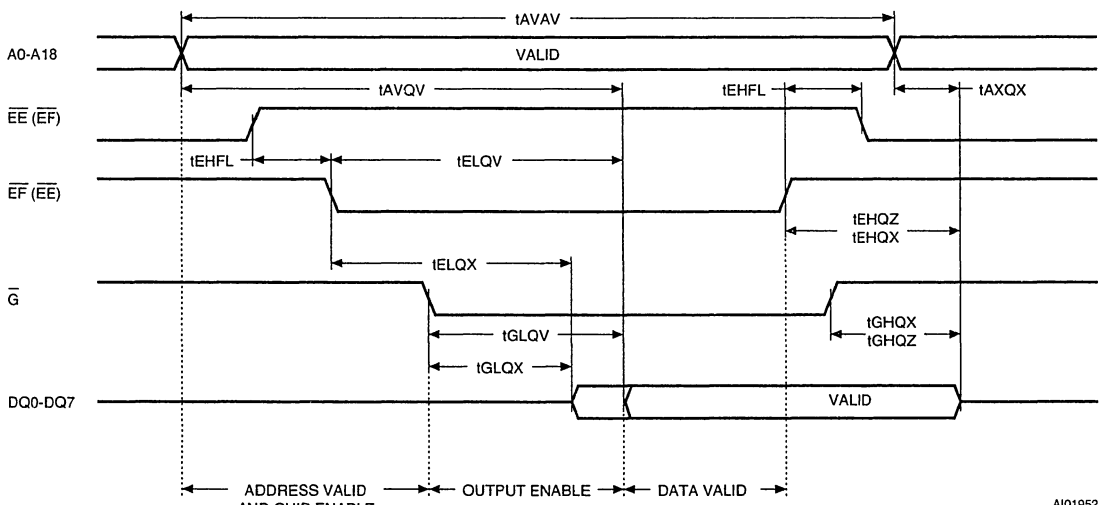
Supply Rails. Normal precautions must be taken for supply voltage decoupling, each device in a system should have the V_{CC} rail decoupled with a 0.1µF capacitor close to the V_{CC} and V_{SS} pins. The printed circuit board trace width should be sufficient to carry the V_{CC} program and erase currents required.

Table 12. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7 to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC1} (1)	Supply Current (Read Flash)	$\overline{EE} = V_{IH}$, $\overline{EF} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz		10	mA
I_{CC2}	Supply Current (Read EEPROM)	$\overline{EE} = V_{IL}$, $\overline{EF} = V_{IH}$, $\overline{G} = V_{IH}$, f = 6MHz		10	mA
I_{CC3}	Supply Current (Standby)	$\overline{EF} = \overline{EE} = V_{CC} \pm 0.2V$		100	µA
I_{CC4}	Supply Current (Flash Block Program or Erase)	Byte program, Sector or Chip Erase in progress		20	mA
I_{CC5}	Supply Current (EEPROM Write)	During t_{WC}		20	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}	VCC + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.8mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{CC} –0.4		V
V_{ID}	A9 High Voltage		11.5	12.5	V
I_{ID}	V_{ID} Current	A9 = V_{ID}		100	µA
V_{LKO}	V_{CC} Minimum for Write, Erase and Program		1.9	2.3	V

Note: 1. When reading the Flash block when an EEPROM byte(s) is under a write cycle, the supply current is I_{CC1} + I_{CC5}

Figure 12. Read Mode AC Waveforms



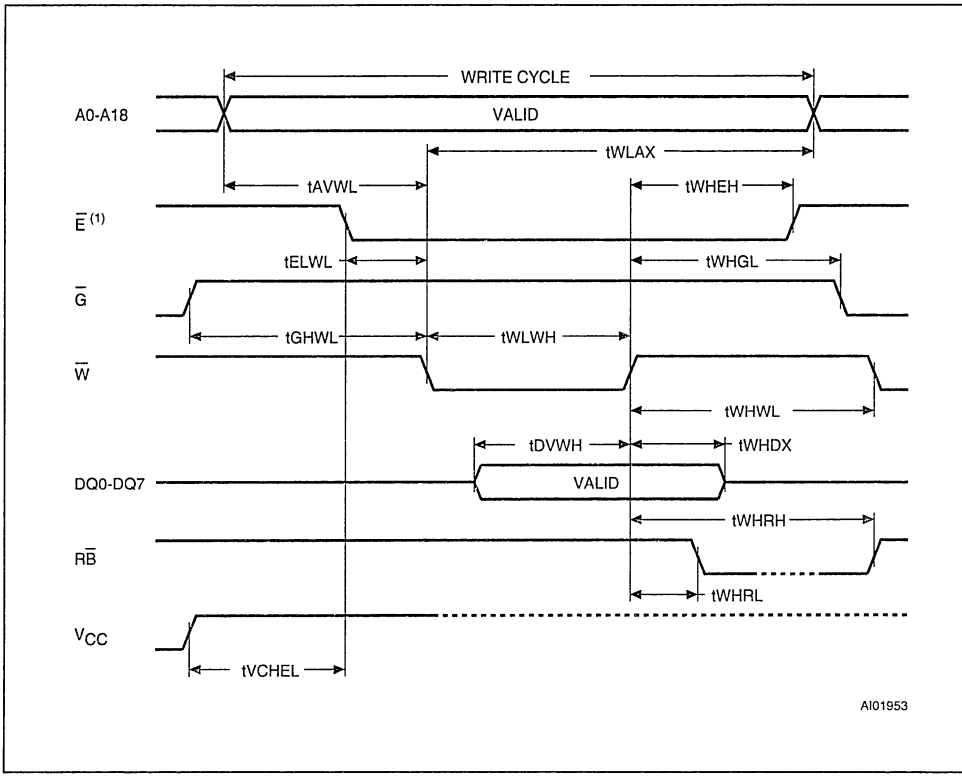
Note: Write Enable ($\overline{W}$) = High

Table 13. Read AC Characteristics
(T_A = 0 to 70°C or –20 to 85°C; V_{CC} = 3.3V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	M39832				Unit
				-120		-150		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$(\overline{EE}, \overline{EF})$ = (V_{IL}, V_{IH}) or (EE, EF) = (V_{IH}, V_{IL}), $\overline{G}$ = V_{IL}	120		150		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$(\overline{EE}, \overline{EF})$ = (V_{IL}, V_{IH}) or (EE, EF) = (V_{IH}, V_{IL}), $\overline{G}$ = V_{IL}		120		150	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120		150	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$(\overline{EE}, \overline{EF})$ = (V_{IL}, V_{IH}) or (EE, EF) = (V_{IH}, V_{IL})	0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$(\overline{EE}, \overline{EF})$ = (V_{IL}, V_{IH}) or (EE, EF) = (V_{IH}, V_{IL})		55		55	ns
t_{EHQX}	t_{OH}	Chip Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		40		40	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$(\overline{EE}, \overline{EF})$ = (V_{IL}, V_{IH}) or (EE, EF) = (V_{IH}, V_{IL})	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$(\overline{EE}, \overline{EF})$ = (V_{IL}, V_{IH}) or (EE, EF) = (V_{IH}, V_{IL})		40		40	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$(\overline{EE}, \overline{EF})$ = (V_{IL}, V_{IH}) or (EE, EF) = (V_{IH}, V_{IL}), $\overline{G}$ = V_{IL}	0		0		ns
t_{EHFL}	t_{CED}	$\overline{EE}$ ($\overline{EF}$) Active to $\overline{EF}$ ($\overline{EE}$)		100		100		ns

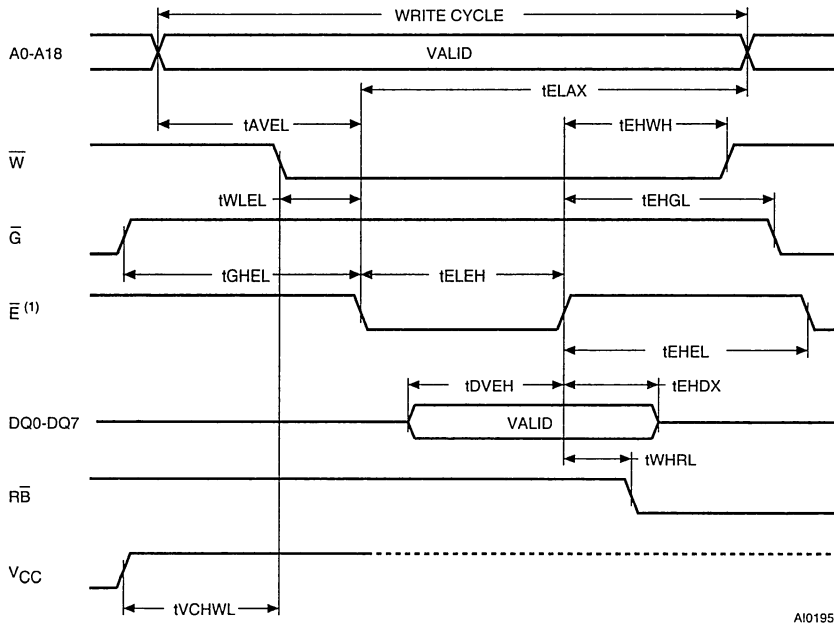
Notes: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{EE}$ (or $\overline{EF}$) without increasing t_{ELQV}.

Figure 13. Write AC Waveforms, $\overline{W}$ Controlled



Notes: Address are latched on the falling edge of $\overline{W}$, Data is latched on the rising edge of $\overline{W}$
$\overline{E}$ is either $\overline{EF}$ when $\overline{EE}$ = V_{IH} or $\overline{EE}$ when $\overline{EF}$ = V_{IH}.

Figure 14. Write AC Waveforms, $\overline{E}$ Controlled



Notes: Address are latched on the falling edge of $\overline{E}$, Data is latched on the rising edge of $\overline{E}$.
$\overline{E}$ is either $\overline{EF}$ when $\overline{EE}$ = V_{IH} or $\overline{EE}$ when $\overline{EF}$ = V_{IH}.

Table 14. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7V to 3.6V)

Symbol	Alt	Parameter	M39832				Unit
			-120		-150		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	120		150		ns
t_{ELWL} (2)	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		65		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		65		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		ns
t_{WHEH} (2)	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	30		35		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	50		65		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		µs
t_{WHQV1} (1)		Write Enable High to Output Valid (Program)	15		15		µs
t_{WHQV2} (1)		Write Enable High to Output Valid (Sector Erase)	2.0	30	2.0	30	sec
t_{WHWL0}		Time Out between 2 consecutive Section Erase		80		80	µs
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		ns
t_{WHRL} (3)	t_{DB}	Write Enable High to Ready/Busy Output Low		150		150	ns

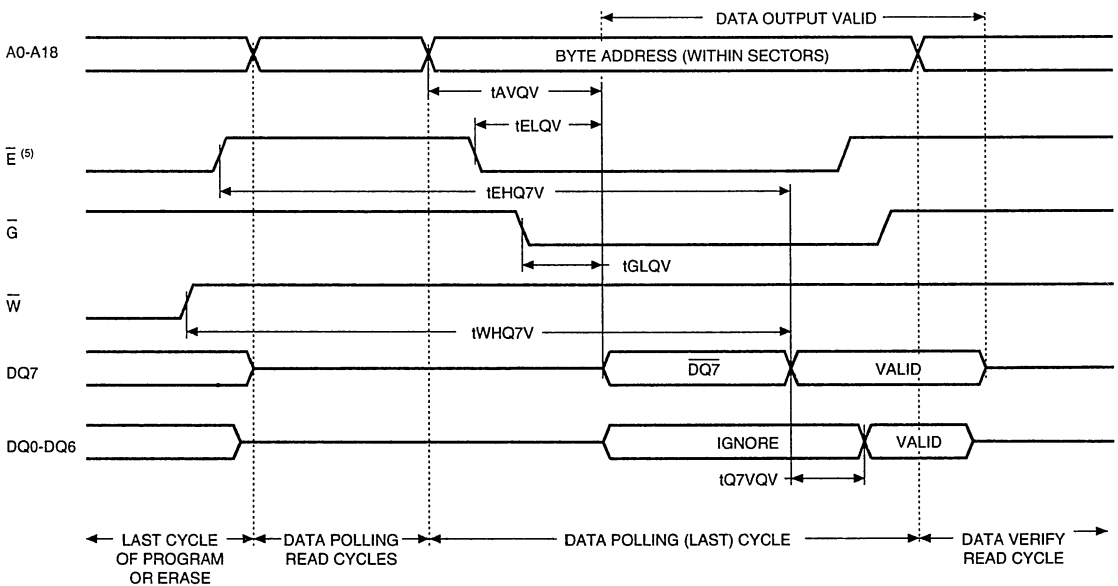
Notes: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$
2 Chip Enable means ($\overline{EE}$, $\overline{EF}$) = (V_{IL}, V_{IH}) or ($\overline{EE}$, $\overline{EF}$) = (V_{IH}, V_{IL})
3 With a 3 3KΩ pull-up resistor.

Table 15. Write AC Characteristics, $\overline{EE}$ or $\overline{EF}$ Controlled
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7V to 3.6V)

Symbol	Alt	Parameter	M39832				Unit
			-120		-150		
			Min	Max	Min	Max	
t_{WLWL}	t_{BLC}	Byte Load Cycle (EEPROM)	0.2	150	0.2	150	µs
t_{WHRH}	t_{WC}	Write Cycle Time (EEPROM)		10		10	ms
t_{AVAV}		Address Valid to Next Address Valid	120		150		ns
t_{WLEL}	t_{WS}	Write Enable Low to Memory Block Enable Low	0		0		ns
t_{ELEH}	t_{CP}	Memory Block Enable Low to Memory Block Enable High	50		65		ns
t_{DVEH}	t_{DS}	Input Valid to Memory Block Enable High	50		65		ns
t_{EHDX}	t_{DH}	Memory Block Enable High to Input Transition	0		0		ns
t_{EHWH}	t_{WH}	Memory Block Enable High to Write Enable High	0		0		ns
t_{EHEL}	t_{CPH}	Memory Block Enable High to Memory Block Enable Low	30		35		ns
t_{AVEL}	t_{AS}	Address Valid to Memory Block Enable Low	0		0		ns
t_{ELAX}	t_{AH}	Memory Block Enable Low to Address Transition	50		65		ns
t_{GHEL}		Output Enable High to Memory Block Enable Low	0		0		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		µs
t_{EHQV1} (1)		Memory Block Enable High to Output Valid (Program)	15		15		µs
t_{EHQV2} (1)		Memory Block Enable High to Output Valid (Sector Erase)	2.0	30	2.0	30	sec
t_{EHGL}	t_{OEH}	Memory Block Enable High to Output Enable Low	0		0		ns
t_{EHRL} (2)	t_{DB}	EEPROM Block Enable High to Ready/Busy Output Low		150		150	ns

Notes: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$.
2. With a 3 3KΩ pull-up resistor.

Figure 15. Data Polling DQ7 AC Waveforms



Notes: 1. All other timings are as a normal Read cycle.
2. DQ7 and DQ0-DQ6 can transmit to valid at any point during the data output valid period.
3. t_{WHQ7V} is the Program or Erase time.
4. During erasing operation Byte address must be within Sector being erased.
5. $\overline{E}$ is either $\overline{EF}$ when $\overline{EE} = V_{IH}$ or $\overline{EE}$ when $\overline{EF} = V_{IH}$.

Table 16. Data Polling and Toggle Bit AC Characteristics (1)
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.7V to 3.6V)

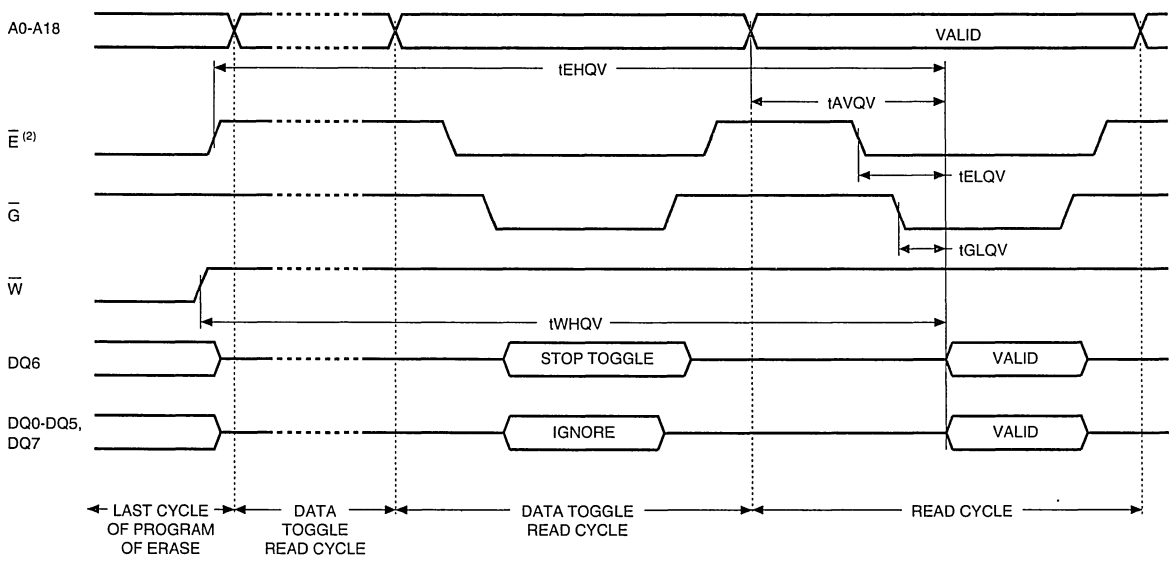
Symbol	Parameter	M39832				Unit
		-120		-150		
		Min	Max	Min	Max	
t_{WHQ7V1} (2)	Write Enable High to DQ7 Valid (Program, W Controlled)	10		10		µs
t_{WHQ7V2} (2)	Write Enable High to DQ7 Valid (Sector Erase, W Controlled)	1.5	30	1.5	30	sec
t_{EHQ7V1} (2)	Flash Block Enable High to DQ7 Valid (Program, EF Controlled)	10		10		µs
t_{EHQ7V2} (2)	Flash Block Enable High to DQ7 Valid (Sector Erase, EF Controlled)	1.5	30	1.5	30	sec
t_{Q7VQV}	Q7 Valid to Output Valid (Data Polling)		50		55	ns

Notes: 1. All other timings are defined in Read AC Characteristics table.
2. t_{WHQ7V} is the Program or Erase time.

Table 17. Program, Erase Times and Program, Erase Endurance Cycles (Flash Block)
(T_A = 0 to 70°C; V_{CC} = 2.7V to 3.6V)

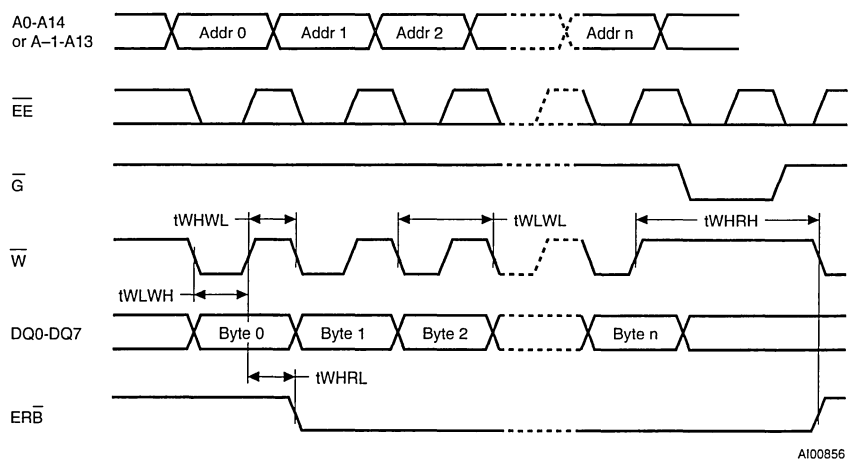
Parameter	M39832				Unit
	Min	Typ	Typical after 100k W/E Cycles	Max	
Flash array Erase (Preprogrammed)		5	5		sec
Flash array Erase		12	12		sec
Flash array Block Erase		2.4			sec
Parameter Block Erase		2.3			sec
Main Block (32Kb) Erase		2.7			sec
Main Block (64Kb) Erase		3.3		15	sec
Chip Program (Byte)		8	8		sec
Byte Program		10	10		µs
Word Program		20	20		µs
Program/Erase Cycles (per Block)	100,000				cycles

Figure 16. Data Toggle DQ6 AC Waveforms

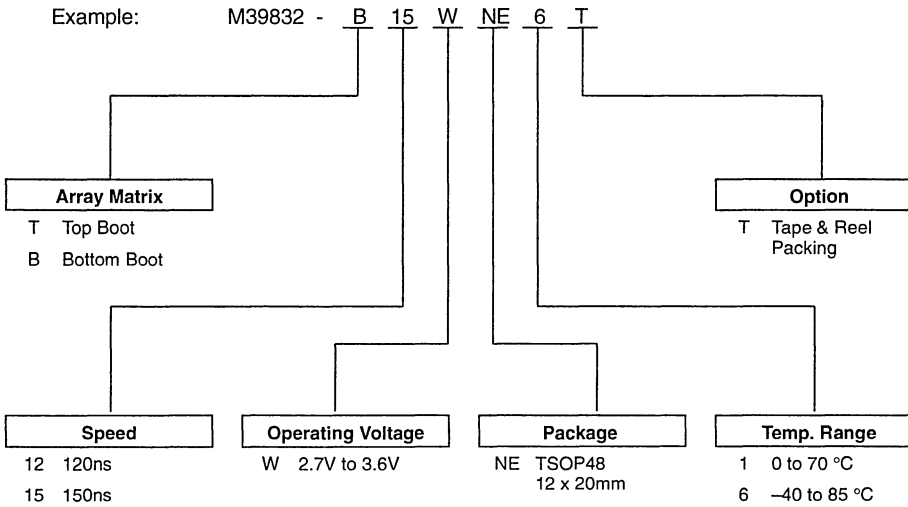


Notes: 1 All other timings are as a normal Read cycle.
2. E is either EF when EE = V_{IH} or EE when EF = V_{IH}.

Figure 17. EEPROM Page Write Mode AC Waveforms, $\overline{W}$ Controlled



ORDERING INFORMATION SCHEME

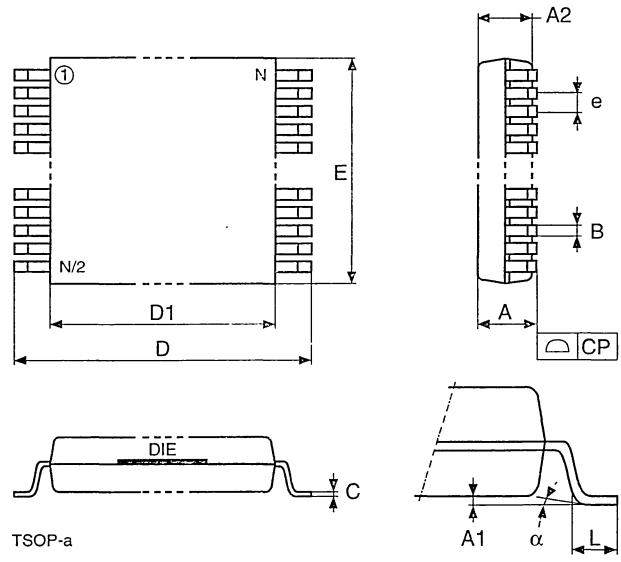


Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

TSOP48 - 48 lead Plastic Thin Small Outline, 12 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		11.90	12.10		0.469	0.476
e	0.50	-	-	0.020	-	-
L		0 50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	48			48		
CP			0.10			0.004



TSOP-a

Drawing is not to scale.

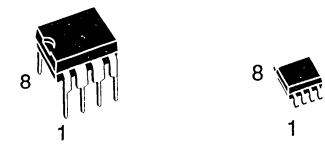
APPLICATION SPECIFIC MEMORIES

M24164

16 Kbit Serial I²C BUS EEPROM

PRELIMINARY DATA

- TWO WIRE I²C SERIAL INTERFACE SUPPORTS 400kHz PROTOCOL
- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- 2ms TYPICAL PROGRAMMING TIME
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for M24164
  - 2.5V to 5.5V for M24164-W
  - 1.8V to 5.5V for M24164-R
- HARDWARE WRITE CONTROL
- BYTE and PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH-UP PERFORMANCES



PSDIP8 (BN)
0.25mm Frame

SO8 (MN)
150mil Width

DESCRIPTION

The M24164 is a 16 Kbit EEPROM. The memory is an electrically erasable programmable memory (EEPROM) fabricated with STMicroelectronics's High Endurance Single Polysilicon CMOS technology which guarantees an endurance typically well above one million erase/write cycles with a data retention of 40 years. The "-W" version operate with a power supply value as low as 2.5V and the "-R" version operate down to 1.8V.

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Figure 1. Logic Diagram

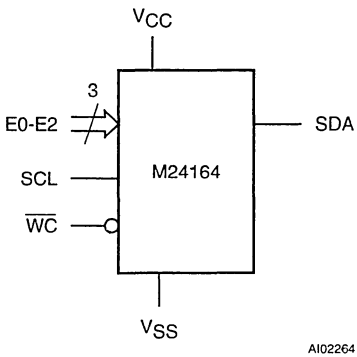


Table 1. Signal Names

E0-E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient OperatingTemperature(2)			–40 to 125	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(PSDIP8 package) (SO8 package)	10 sec 40 sec	260 215	°C
V_{IO}	Input or Output Voltages			–0.6 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (3)			4000	V
	Electrostatic Discharge Voltage (Machine model) (4)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2 Depends on range
3. MIL-STD-883C, 3015.7 (100pF, 1500 Ω)
4. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

Figure 2A. DIP Pin Connections

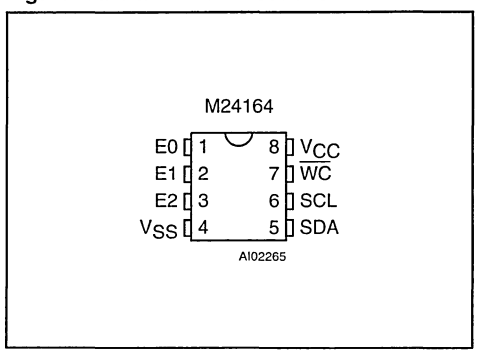
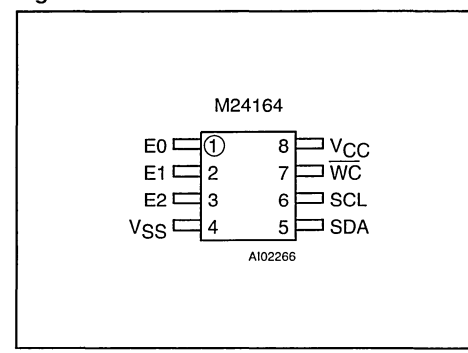


Figure 2B. SO Pin Connections



DESCRIPTION (cont'd)

The memory is compatible with the two wire serial interface which uses a bi-directional data bus and serial clock. The memory offers 3 chip enable inputs (E2, $\overline{E1}$, E0) so that up to 8 x 16K devices may be attached to the bus and selected individually. The memory behaves as a slave device with all memory operations synchronized by the serial clock.

Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits, plus one read/write bit and terminated by an acknowledge bit (see Table 3). When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent any possible data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

Table 3. Device Select Code

		Chip Enable			MSB Address			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	E2	$\overline{E1}$	E0	A10	A9	A8	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes (1)

Mode	RW bit	WP	Data Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, RW = '1'
Random Address Read	'0'	X	1	START, Device Select, RW = '0', Address,
	'1'	X		reSTART, Device Select, RW = '1'
Sequential Read	'1'	X	≥ 1	As CURRENT or RANDOM Mode
Byte Write	'0'	V_{IL}	1	START, Device Select, RW = '0'
Page Write	'0'	V_{IL}	≤ 16	START, Device Select, RW = '0'

Note: 1. X = V_{IH} or V_{IL}.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Chip Enable (E2 - E0). These chip enable inputs are used to set 3 bits (b6, b5, b4) of the 7 bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Write Control ($\overline{WC}$). A hardware Write Control pin ($\overline{WC}$) is provided on pin 7 of the memory. This feature is useful to protect the entire contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$=V_{IL}) or disable ($\overline{WC}$=V_{IH}) write instructions to the entire memory area. When unconnected, the $\overline{WC}$ input is internally read as V_{IL} and write operations are allowed. When $\overline{WC}$=1, Device Select and Address bytes are acknowledged, Data bytes are not acknowledged.

Refer to Application Note AN404 for more detailed information about Write Control feature.

DEVICE OPERATION

I^2C Bus Background

The memory supports the I^2C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The memory is always a slave device in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the memory continuously monitors the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the memory and the bus master. A STOP condition at the end of a Read sequence, after and only after a No-Acknowledge, forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the memory samples the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation, the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave memory, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the Device Select code (7 bits) and a READ or WRITE bit.

Three out of the four most significant bits of the Device Select code are the Device Select bits (b6, b5, b4). They are matched to the chip enable signals applied on pins E2, $\overline{E1}$, E0. Thus up to 8 x 16K memories can be connected on the same bus giving a memory capacity total of 128 Kbits.

After a START condition any memory on the bus will identify the device code and compare the 3 bits to its chip enable inputs E2, $\overline{E1}$, E0. The 8th bit sent is the read or write bit ($\overline{RW}$).

This bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time. If the memory does not match the Device Select code, it will self-deselect from the bus and go into standby mode.

Write Operations

Following a START condition the master sends a Device Select code with the $\overline{RW}$ bit set to '0'. The memory acknowledges it and waits for a byte address, which provides access to the memory area. After receipt of the byte address, the memory again responds with an acknowledge and waits for the data byte. Writing in the Memory may be inhibited if input pin $\overline{WC}$ is taken high.

Any write command with $\overline{WC}$=1 (during a period of time from the START condition until the Acknowledge of the last Data byte) will not modify the memory content and will NOT be acknowledged on data bytes, as shown in Figure 9.

Byte Write. In the Byte Write mode, after the Device Select code and the address, the master sends one data byte. If the addressed location is write protected by the $\overline{WC}$ pin, the memory send a NoACK and the location is not modified. If the $\overline{WC}$ pin is tied to 0, after the data byte the memory sends an ACK. The master terminates the transfer by generating a STOP condition.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus

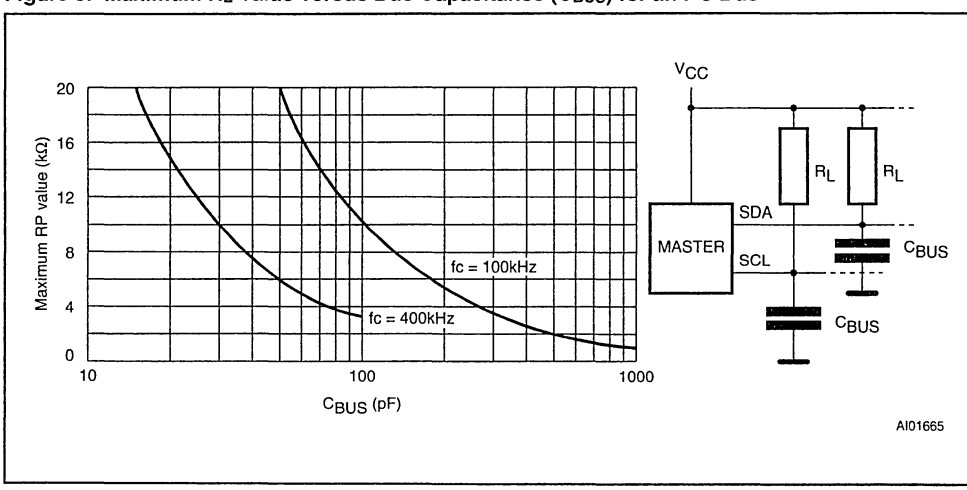


Table 5. Input Parameters [1] (T_A = 25°C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)		200	500	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V, 2.5V to 5.5V or 1.8V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_C = 400kHz (Rise/Fall time < 30ns)		2	mA
	Supply Current (-W series)	V_{CC} = 2.5V, f_C = 400kHz (Rise/Fall time < 30ns)		1	mA
	Supply Current (-R series)	V_{CC} = 1.8V, f_C = 100kHz (Rise/Fall time < 30ns)		0.8	mA
I_{CC1}	Supply Current, Standby	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		20	µA
I_{CC2}	Supply Current, Standby (-W series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		1	µA
I_{CC3}	Supply Current, Standby (-R series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8V		0.1	µA
V_{IL}	Input Low Voltage (SCL, SDA, E2, E1, E0)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA, E2, E1, E0)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage ($\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage ($\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (-W series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V
	Output Low Voltage (-R series)	I_{OL} = 0.15mA, V_{CC} = 1.8V		0.2	V

Table 7. AC Characteristics

Symbol	Alt	Parameter	M24164						Unit
			V_{CC} = 4.5V to 5.5V T_A = 0 to 70°C T_A = –40 to 85°C		V_{CC} = 2.5V to 5.5V T_A = 0 to 70°C T_A = –40 to 85°C		V_{CC} = 1.8V to 5.5V T_A = 0 to 70°C T_A = –40 to 85°C		
			Min	Max	Min	Max	Min	Max	
t_{CH1CH2}	t_R	Clock Rise Time		300		300		1000	ns
t_{CL1CL2}	t_F	Clock Fall Time		300		300		300	ns
t_{DH1DH2} (1)	t_R	SDA Rise Time	20	300	20	300	20	1000	ns
t_{DL1DL2} (1)	t_F	SDA Fall Time	20	300	20	300	20	300	ns
t_{CHDX} (2)	$t_{SU.STA}$	Clock High to Input Transition	600		600		4700		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		600		4000		ns
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	600		600		4000		ns
t_{CLDX}	$t_{HD.DAT}$	Clock Low to Input Transition	0		0		0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		1.3		4.7		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	100		100		250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	600		600		4000		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		1.3		4.7		µs
t_{CLQV} (3)	t_{AA}	Clock Low to Next Data Out Valid	200	900	200	900	200	3500	ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		200		200		ns
f_C	f_{SCL}	Clock Frequency		400		400		100	kHz
t_W	t_{WR}	Write Time		5		10		10	ms

Notes: 1. Sampled only, not 100% tested.
2. For a reSTART condition, or following a write cycle.
3. The minimum value delays the falling/rising edge of SDA away form SCL = 1 in order to avoid unwanted START and/or STOP condition.

Table 8. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}
Input and Output Timing Ref. Voltages	0.3V_{CC} to 0.7V_{CC}

Figure 4. AC Testing Input Output Waveforms

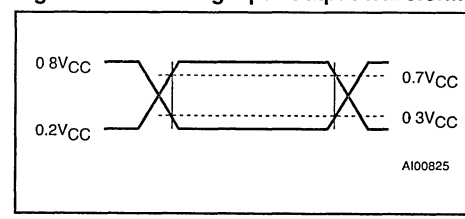
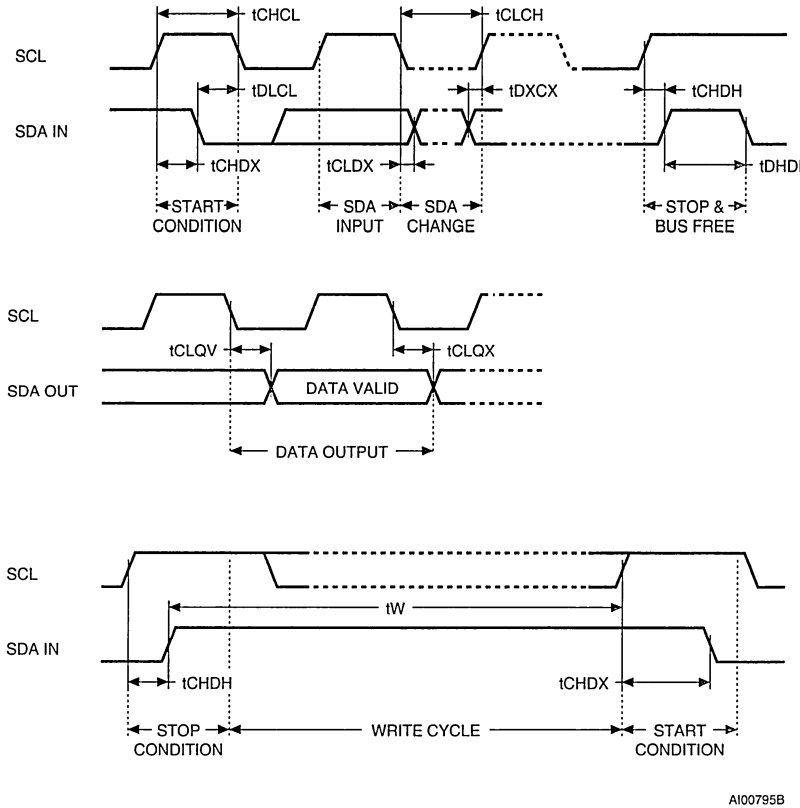
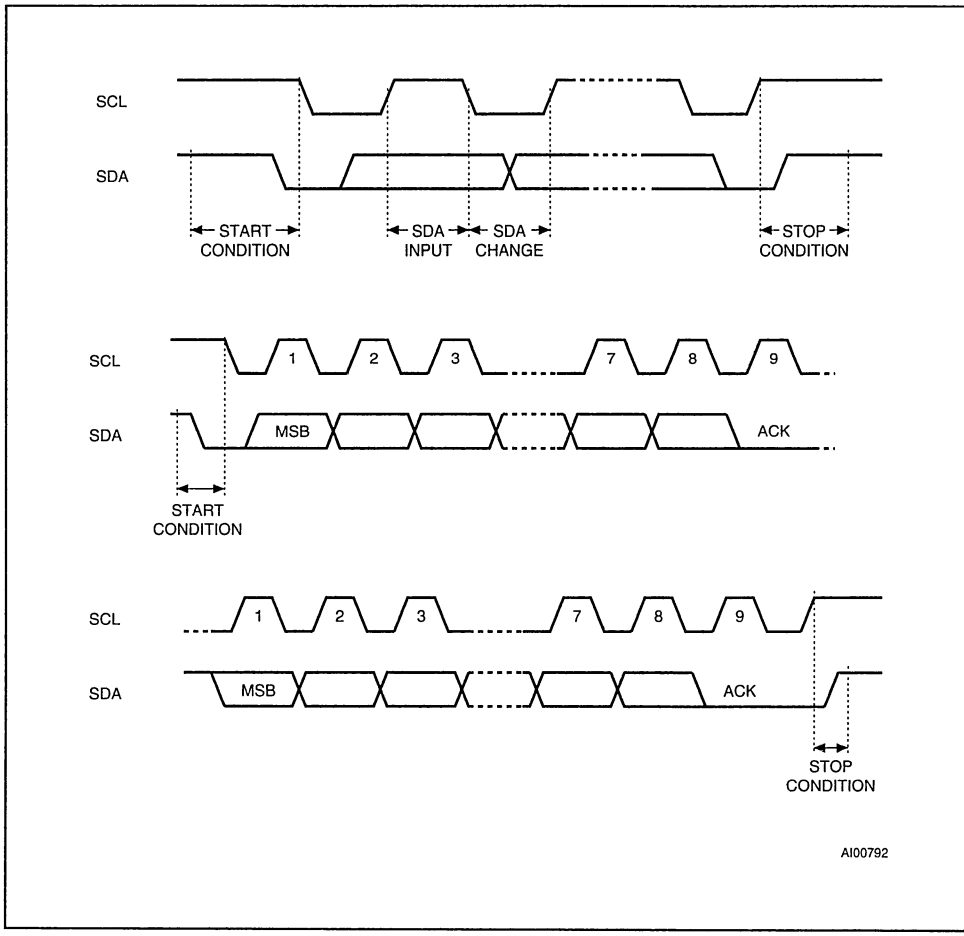


Figure 5. AC Waveforms



Page Write. The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the most significant memory address bits are the same. The master sends from one up to 16 bytes of data, each of which is acknowledged by the memory if the $\overline{WC}$ pin is low. If the $\overline{WC}$ pin is high, each data byte is followed by a NoACK and the location will not be modified. After each byte is transferred, the internal byte address counter (4 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any byte or page write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Figure 6. I²C Bus Protocol



Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (tw) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master. The sequence is:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, NoACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the incoming instruction (the first byte of this instruction was already sent during Step 1).

Figure 7. Write Cycle Polling using ACK

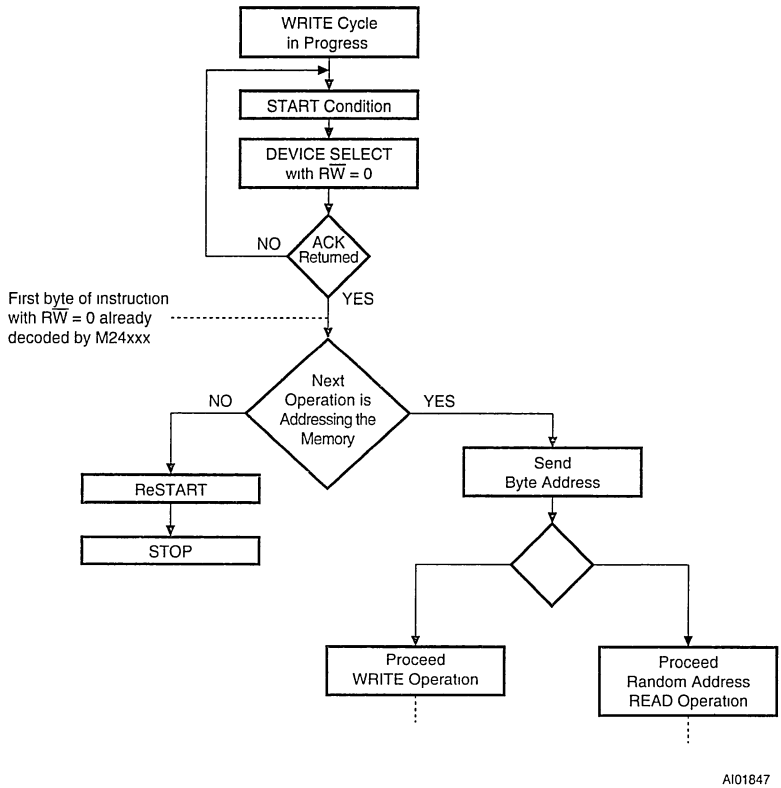
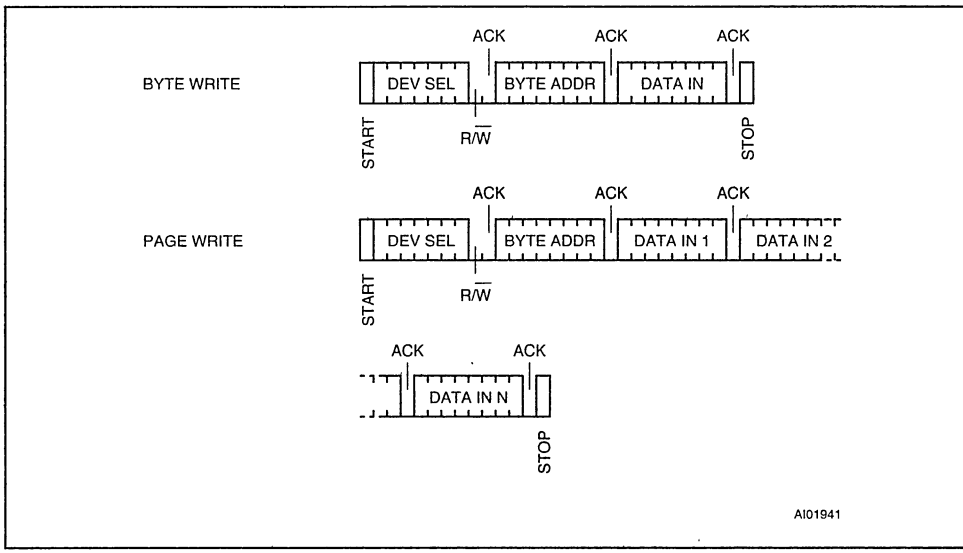


Figure 8. Write Modes Sequence



Read Operations

Read operations are independent from the state of the $\overline{WC}$ input pin. On delivery, the memory contents is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a Device Select code with the $R\overline{W}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master have to NOT acknowledge the byte output and terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the memory address into the address counter, see Figure 10. This is followed by another START condition from the master and the Device Select code is repeated with the $R\overline{W}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master have to NOT acknowledge the byte output and terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output and MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the memory wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the memory terminate the data transfer and switches to a standby state.

Figure 9. Write Modes Sequence with Write Control = 1

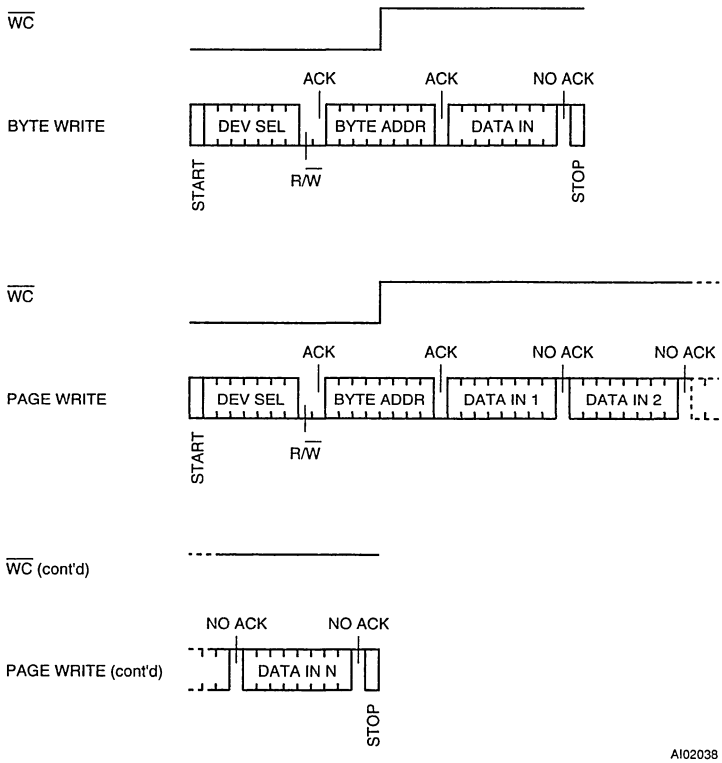
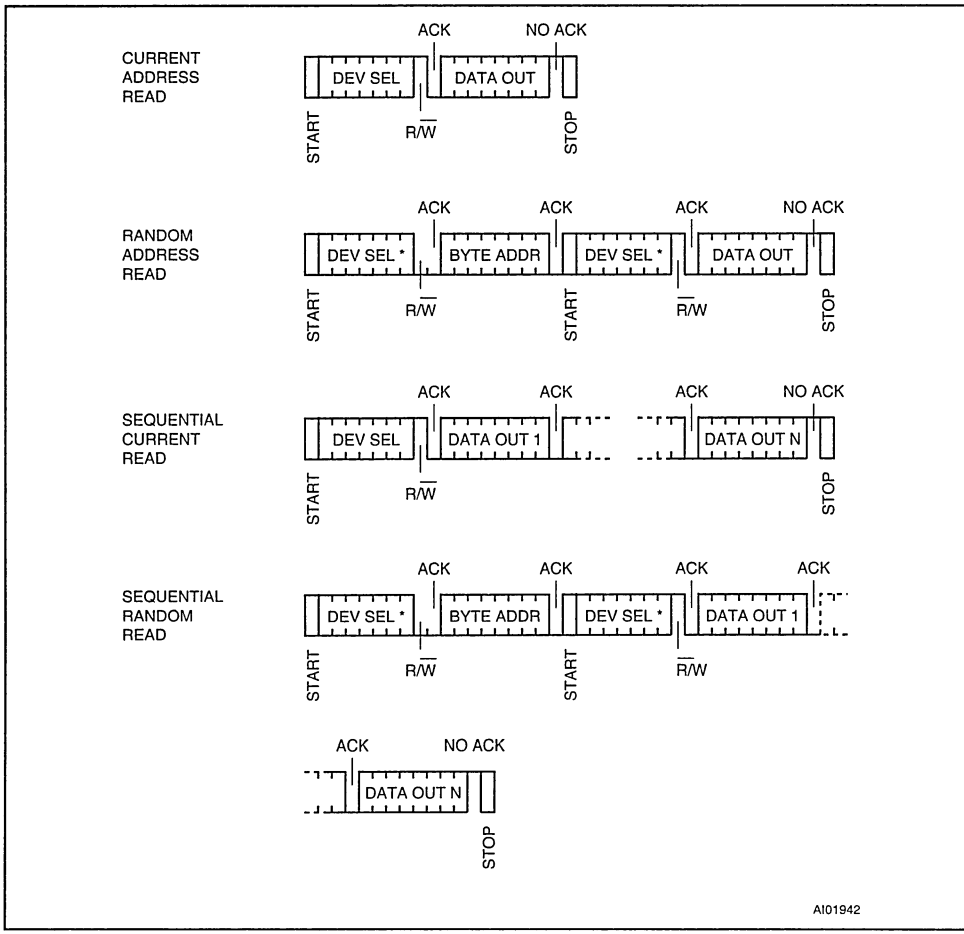
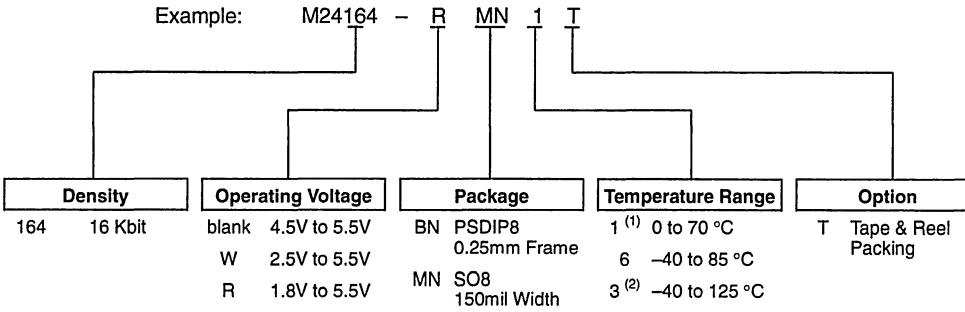


Figure 10. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical.

ORDERING INFORMATION SCHEME



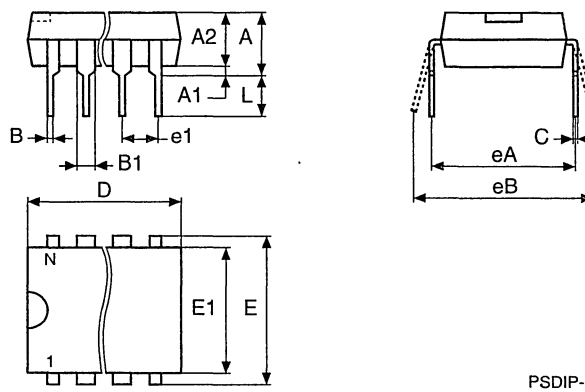
Notes: 1. Temperature range on request only.
2. Produced with High Reliability Certified Flow (HRCF), in V_{CC} range 4.5V to 5.5V at 100kHz only.

Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB		–	10.00		–	0.394
L		3.00	3.80		0.118	0.150
N	8			8		

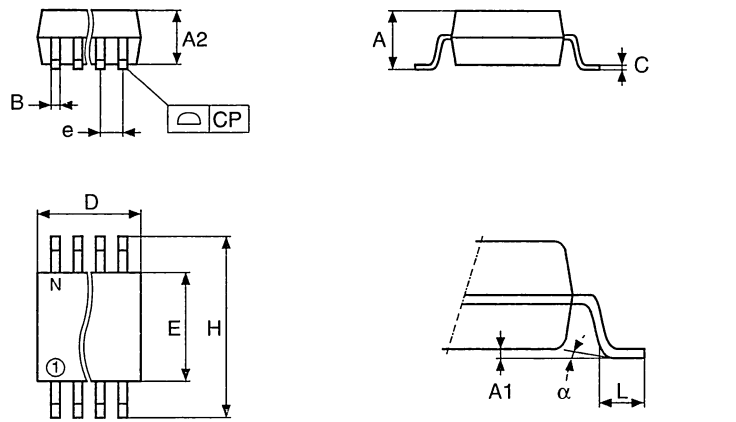


PSDIP-a

Drawing is not to scale.

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0	8		0	8
N	8			8		
CP			0.10			0.004



SO-b

Drawing is not to scale.

2 Kbit Serial EEPROM for DIMM Serial Presence Detect

- TWO WIRE I^2C SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for M34C02
  - 2.5V to 5.5V for M34C02-W
  - 1.8V to 3.6V for M34C02-R
- SOFTWARE WRITE PROTECTION FOR LOWER 128 BYTES
- HARDWARE WRITE PROTECTION FOR ENTIRE ARRAY
- BYTE and PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD and LATCH-UP PERFORMANCES

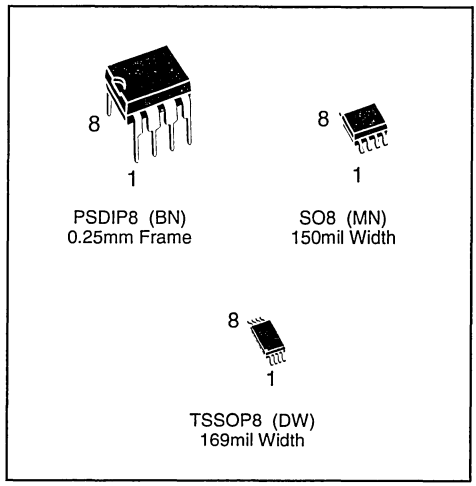
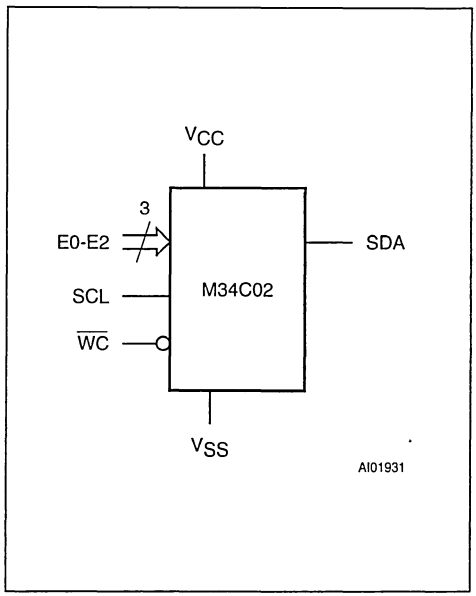


Figure 1. Logic Diagram



DESCRIPTION

The M34C02 is a 2 Kbit electrically erasable programmable memory (EEPROM), organized as 256 x8 bits, designed for use as the Serial Presence Detect Memory for new DRAM DIMM modules.

The M34C02 includes a software write protection feature for the bottom half of the memory area. By sending the device a specific sequence, the first

Table 1. Signal Names

E0-E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

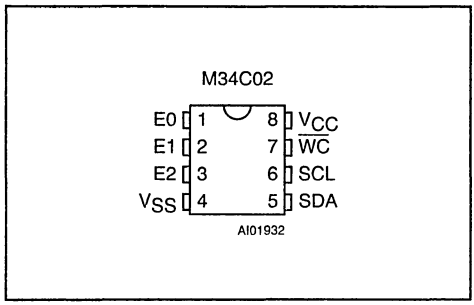


Figure 2B. SO and TSSOP Pin Connections

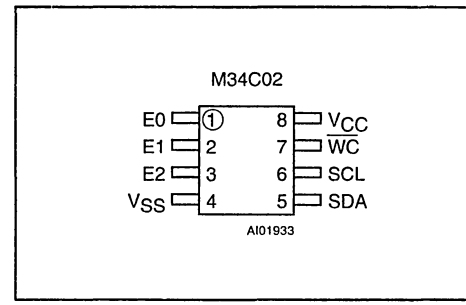


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient OperatingTemperature			–40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(PSDIP8 package) (SO8 package) (TSSOP8 package)	10 sec 40 sec t.b.c.	260 215 t.b.c.	°C
V_{IO}	Input or Output Voltages			–0.6 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			5000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

128 bytes of the memory can be permanently write protected. Care must be taken when using this sequence as it cannot be reversed. The M34C02 include also a $\overline{WC}$ input which, when tied to V_{CC}, allows the entire memory area to be write protected.

The M34C02 is manufactured in STMicroelectronics's Hi-Endurance Advanced CMOS technology. The memories operate with a power supply value as low as 1.8V for the M34C02-R. Plastic Dual-in-Line, Plastic Small Outline and Thin Shrink Small Outline Packages are available.

The memory is compatible with the I^2C standard, two-wire serial interface which uses a bi-directional data bus and serial clock. The memories carry two built-in 4 bit device identification codes: '1010' which corresponds to the I^2C bus definition to access the memory area and '0110' to access the additional Protect Register. This is used together with 3 chip enable inputs (E2, E1, E0) so that up to eight 2K devices may be attached to the I^2C bus and selected individually. The memory behaves as a slave device in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code '1010' or '0110' followed by the 3 chip enable bits), plus one read/write bit ($R\overline{W}$) and terminated by an acknowledge bit.

When writing data to the memory, it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition after an Ack for WRITE and after a NoAck for a READ.

Table 3. Device Select Code

	Device Type Identifier				Chip Enable			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Device Select Code	1	0	1	0	E2	E1	E0	RW
Protect Register Device Select Code	0	1	1	0	E2	E1	E0	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes (1)

Mode	RW bit	WC	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, RW = '1'
Random Address Read	'0'	X	1	START, Device Select, RW = '0', Address,
	'1'	X		reSTART, Device Select, RW = '1'
Sequential Read	'1'	X	≥ 1	Similar to Current or Random Mode
Byte Write	'0'	V_{IL}	1	START, Device Select, RW = '0'
Page Write	'0'	V_{IL}	16	START, Device Select, RW = '0'

Note: 1. X = V_{IH} or V_{IL}

Power On Reset: V_{CC} lock out write protect.

In order to prevent any possible data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented.

Until the V_{CC} voltage has risen to the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Chip Enable (E2 - E0). These chip enable inputs are used to set the 3 least significant bits (b3, b2, b1) of the 7 bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Write Control (WC). A hardware Write Control pin (WC) is provided on pin 7 of the M34C02. This feature is useful to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable (WC=V_{IL}) or disable (WC=V_{IH}) write instructions to the entire memory area and the protect register.

When WC is tied to V_{SS} or left unconnected, the write protection of the first half of the memory is determined by the status of the software protect register.

DEVICE OPERATION

I²C Bus Background

The M34C02 supports the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The M34C02 is always a slave device in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the M34C02 continuously monitors the SDA and SCL signals for a START condition and will not respond unless a START condition is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the M34C02 and the bus master. A STOP condition at the end of a Read sequence, after and only after a No-Acknowledge, forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the M34C02 samples the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation, the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave M34C02, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit.

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I²C bus definition. For this memory the 4 bits are fixed as 1010b to access the memory area and as 0110b to access the Protect Register. The following 3 bits identify the specific memory on the bus. They are matched to the chip enable signals E2, E1, E0. Thus up to eight 2K memories can be connected on the same bus giving a maximum memory capacity total of 16 Kbits. After a START condition any memory on the bus will identify the device code and compare the following 3 bits to its chip enable inputs E2, E1, E0.

The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time. If the memory does not match the device select code, it will self-deselect from the bus and go in standby mode.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I²C Bus

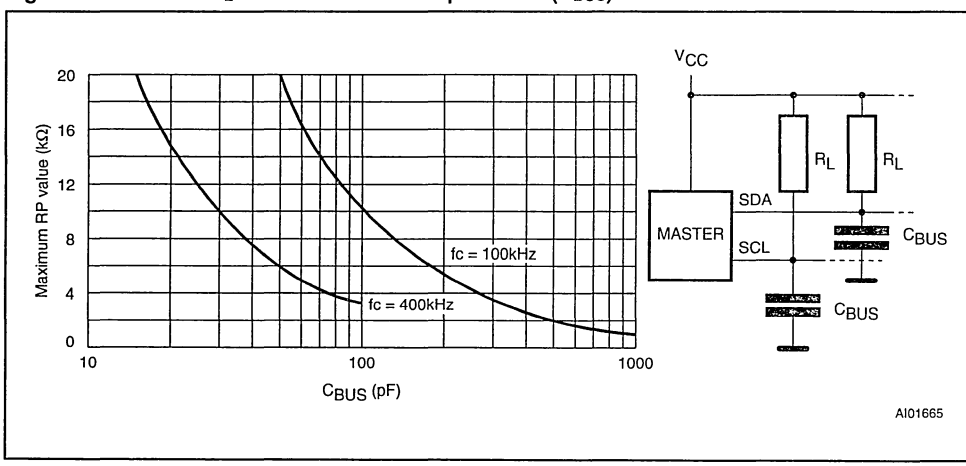


Table 5. Input Parameters (1) (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)		200	500	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5V to 5.5V, 2.5 to 5.5V)
(T_A = 0 to 70°C or –20 to 85°C; V_{CC} = 1.8V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_C = 400kHz (Rise/Fall time < 30ns)		2	mA
	Supply Current (-W series)	V_{CC} = 2.5V, f_C = 400kHz (Rise/Fall time < 30ns)		1	mA
	Supply Current (-R series)	V_{CC} = 1.8V, f_C = 400kHz (Rise/Fall time < 30ns)		0.5	mA
I_{CC1}	Supply Current, Standby	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		1	µA
I_{CC2}	Supply Current, Standby (-W series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		0.5	µA
I_{CC3}	Supply Current, Standby (-R series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8V		0.1	µA
V_{IL}	Input Low Voltage (SCL, SDA, E2, E1, E0)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (E2, E1, E0)		0.7 V_{CC}	V_{CC} + 1	V
	Input High Voltage (SCL, SDA)	$4.5V \le V_{CC} \le 5.5V$	0.7 V_{CC}	VCC + 1	V
		$V_{CC} < 4.5V$	0.7 V_{CC}	5.7	V
V_{IL}	Input Low Voltage ($\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage ($\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (-W series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V
	Output Low Voltage (-R series)	I_{OL} = 0.15mA, V_{CC} = 1.8V		0.2	V

Table 7. AC Characteristics

Symbol	Alt	Parameter	M34C02						Unit
			V_{CC} = 4.5V to 5.5V T_A = 0 to 70°C T_A = –40 to 85°C		V_{CC} = 2.5V to 5.5V T_A = 0 to 70°C T_A = –40 to 85°C		V_{CC} = 1.8V to 3.6V T_A = 0 to 70°C T_A = –20 to 85°C (4)		
			Min	Max	Min	Max	Min	Max	
t_{CH1CH2}	t_R	Clock Rise Time		300		300		1000	ns
t_{CL1CL2}	t_F	Clock Fall Time		300		300		300	ns
t_{DH1DH2} (1)	t_R	SDA Rise Time	20	300	20	300	20	1000	ns
t_{DL1DL2} (1)	t_F	SDA Fall Time	20	300	20	300	20	300	ns
t_{CHDX} (2)	$t_{SU\ STA}$	Clock High to Input Transition	600		600		4700		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		600		4000		ns
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	600		600		4000		ns
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		0		0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1300		1300		4700		ns
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	100		100		250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	600		600		4000		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1300		1300		4700		ns
t_{CLQV} (3)	t_{AA}	Clock Low to Next Data Out Valid	200	900	200	900	200	3500	ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		200		200		ns
f_C	f_{SCL}	Clock Frequency		400		400		100	kHz
t_W	t_{WR}	Write Time		5		10		10	ms

Notes: 1. Sampled only, not 100% tested
2 For a reSTART condition, or following a write cycle.
3. The minimum value delays the falling/rising edge of SDA away form SCL = 1 in order to avoid unwanted START and/or STOP condition.
4. This is preliminary data.

Figure 4. AC Testing Input Output Waveforms

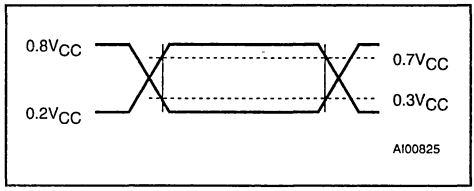


Table 8. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}
Input and Output Timing Ref. Voltages	0.3V_{CC} to 0.7V_{CC}

Write Operations

Following a START condition the master sends a device select code with the $\overline{RW}$ bit set to '0'. The memory acknowledges it and waits for a byte address, which provides access to the 256 bytes of the memory area. After receipt of the byte address, the memory again responds with an acknowledge and waits for the data byte.

For the M34C02, any write command with $\overline{WC}$=1 will not modify the memory content.

Byte Write. In the Byte Write mode, after the device select code and the address, the master sends one data byte. If the addressed location is in a write protected area, the memory send a NoACK and the location is not modified. If the addressed location is not write protected, the memory will send an ACK. The master terminates the transfer by generating a STOP condition.

Depending on the 4 MSBs of the device select code, the Byte Write instruction can be used to modify a memory location (device select code 1010b) or can be used to access to the Protect Register contents (device select code 0110b).

Page Write. The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 4 most significant memory address bits (A7-A4) are the same. The master sends from one up to 16 bytes of data, which are each acknowledged by the memory if the addressed row is not write protected. If the addressed row is write protected, each data byte is followed by a NoACK and the locations will not be modified. After each byte is transferred, the internal byte address counter (4 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any byte or page write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table. Since the typical time is shorter, the time seen by the system may be reduced by a polling sequence on ACK, issued by the master.

The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the master issues a START condition followed by a device select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, NoACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the incoming instruction (the first byte of this instruction was already sent during Step 1).

Figure 5. AC Waveforms

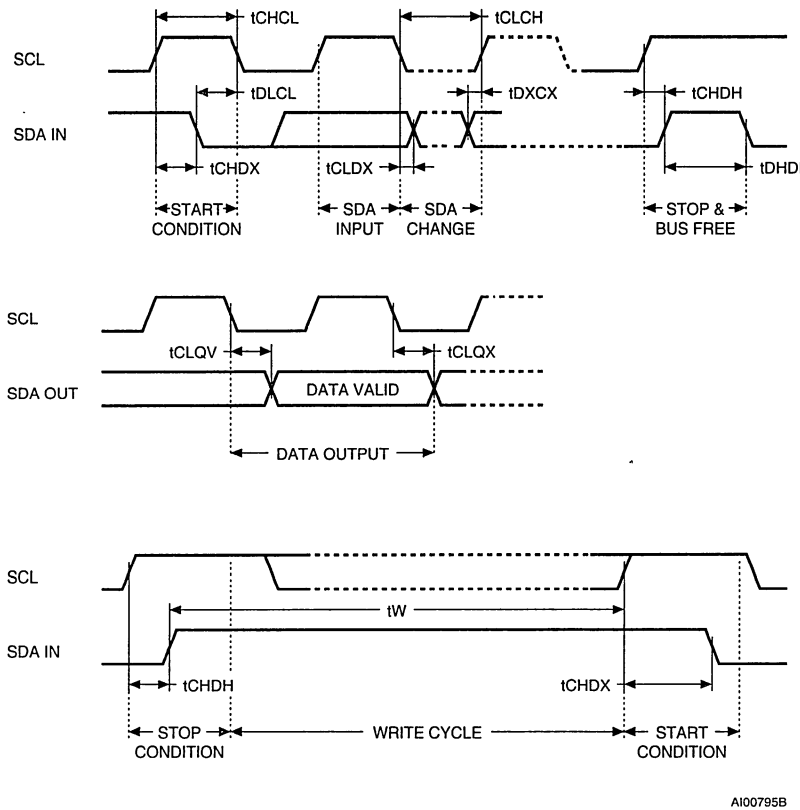
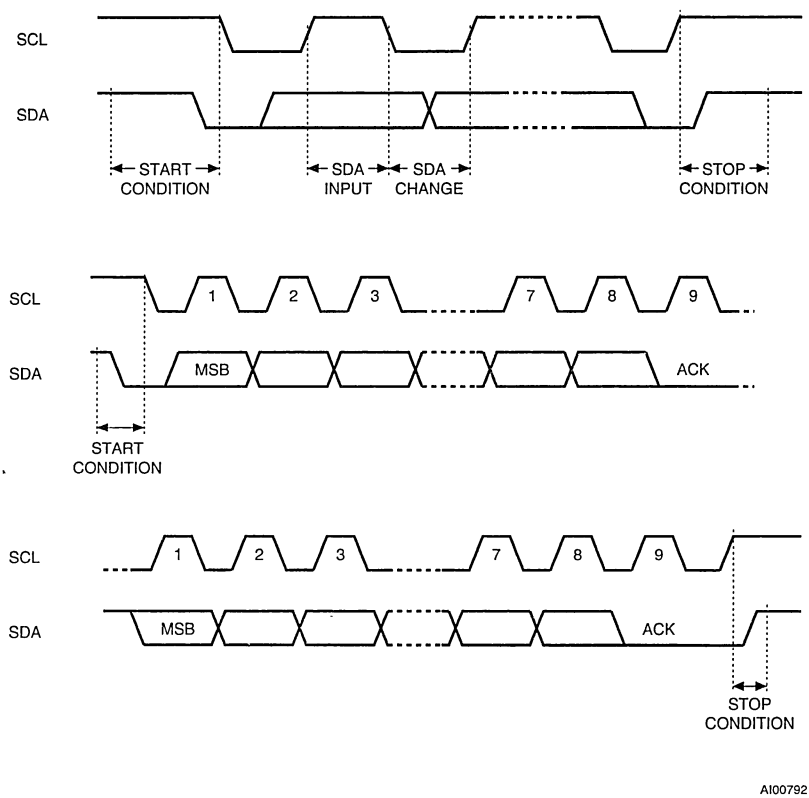


Figure 6. I²C Bus Protocol



Set the Protection using the Protect Register. The M34C02 provides a software write protection function, with the use of a Protect Register.

This allows the bottom half of the memory area (addresses 00h to 7Fh) to be permanently write protected. To activate the write protection feature, the protect register must be accessed once in write mode with the $\overline{WC}$ input tied to V_{SS}. At this time, it is automatically set in order to protect the first 128 bytes of the memory.

The Protect Register is accessed by sending a write command with the 4 device type identifier bit of the device select code set to 0110b (see Figure 9), the E2-E1-E0 bits as applied on the E2-E1-E0 pins and the $\overline{WC}$ input tied to V_{SS}. The address and data bytes must be sent but their value are don't care. Once the protect register has been written, the write protection of the first 128 bytes of the memory is enabled and it will be not possible to unprotect the memory, even if the device is powered off and on and regardless the state of the $\overline{WC}$ input.

When the protect register has been written, the M34C02 will no longer respond at all to the device type identifier 0110b in both read and write mode.

Figure 7. Write Cycle Polling using ACK

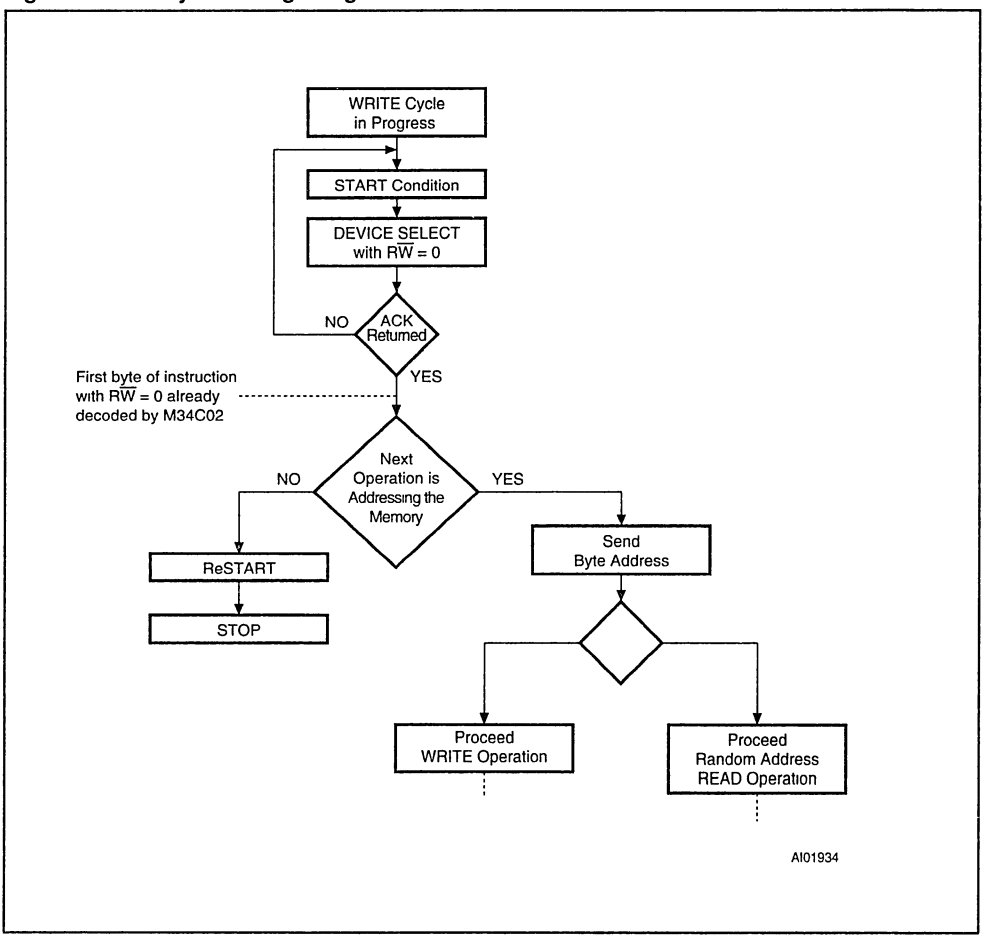


Figure 8. Memory Protection

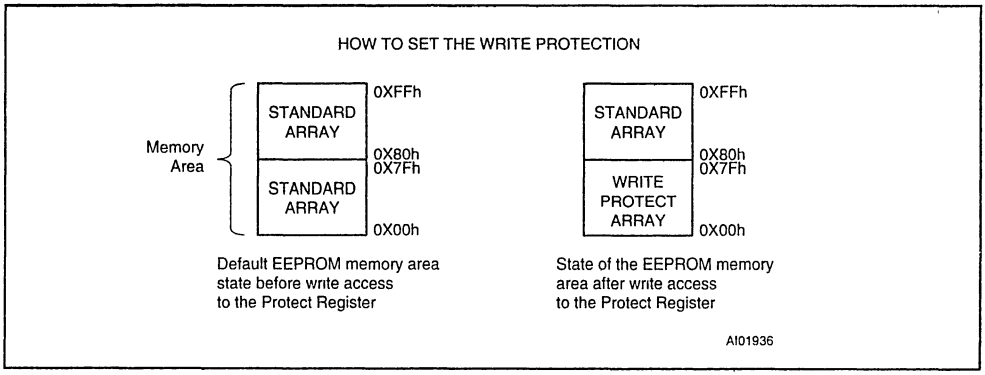


Figure 9. Setting the Write Protect Register ($\overline{WC}$ = 0)

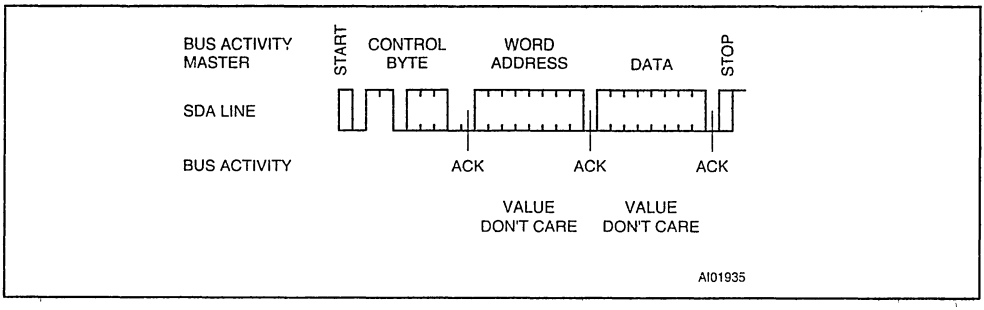


Figure 10. Write Modes Sequence

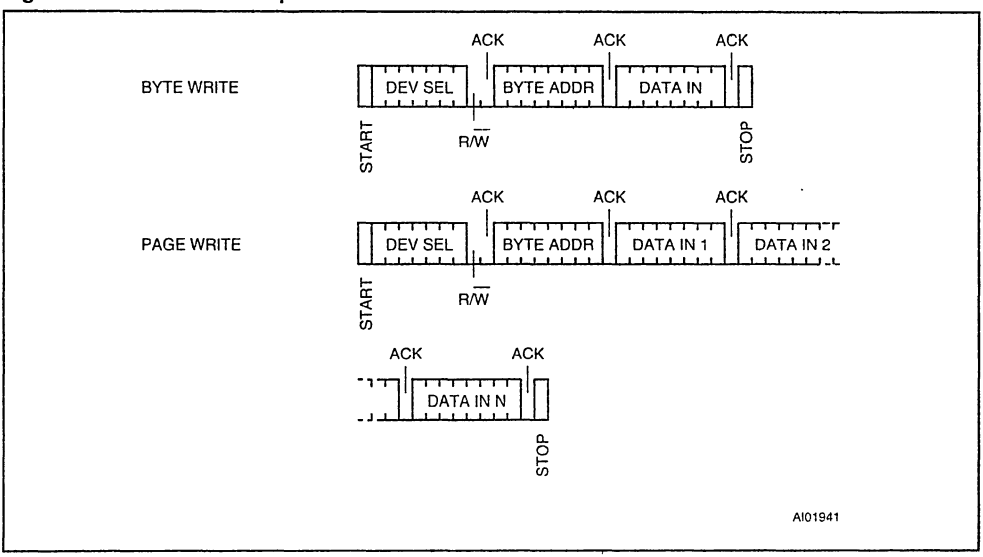
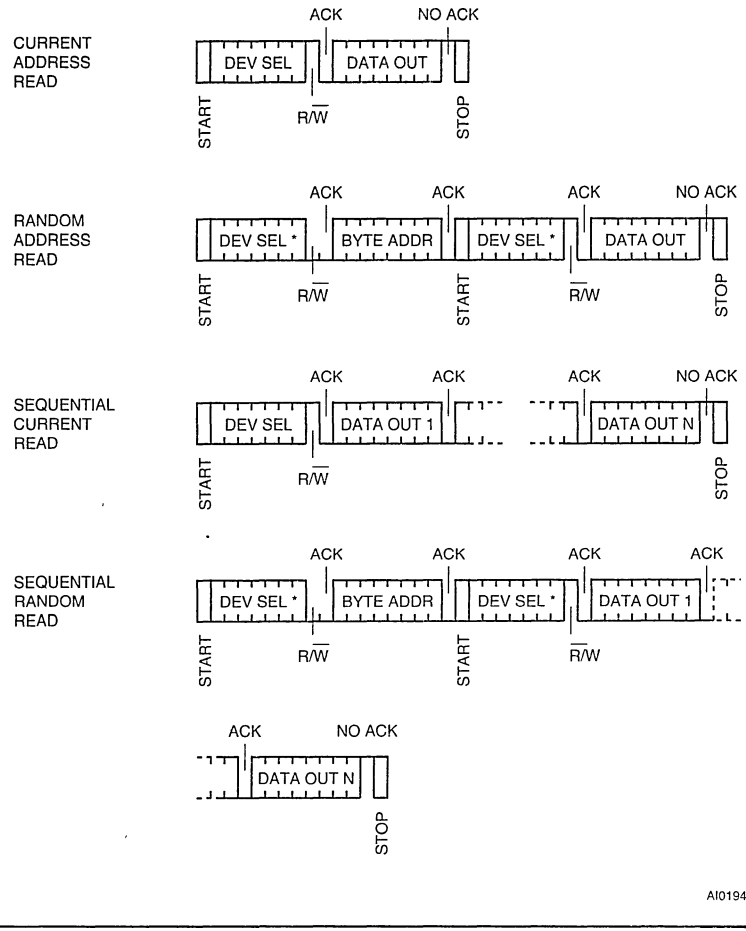


Figure 11. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical

Read Operations

Read operations are independent from the state of the Protect Register. On delivery, the memory contents is set at all "1's" (or FFh)

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a device select code with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master must NOT acknowledge the byte output and must terminate the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the memory address into the address counter, see Figure 11. This is followed by another START condition from the master and the device select code is repeated with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master must NOT acknowledge the byte output and must terminate the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output and MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the M34C02 waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the M34C02 terminates the data transfer and switches to a standby state.

Table 9. 168 Pin DRAM DIMM Module Connections

DIMM Position	E2 (pin 167)	E1 (pin 166)	E0 (pin 165)
0	V_{SS}	V_{SS}	V_{SS}
1	V_{SS}	V_{SS}	V_{CC}
2	V_{SS}	V_{CC}	V_{SS}
3	V_{SS}	V_{CC}	V_{CC}
4	V_{CC}	V_{SS}	V_{SS}
5	V_{CC}	V_{SS}	V_{CC}
6	V_{CC}	V_{CC}	V_{SS}
7	V_{CC}	V_{CC}	V_{CC}

M34C02 in DRAM DIMM Application.

The M34C02 meets the Serial Presence Detect needs for the new DRAM DIMM modules. Its purpose is to contain all information concerning the DRAM module configuration (access time, density, organisation, ...). It is a 2K serial EEPROM memory with a specific feature that provides permanent locking of the first half of the area (from location 00h to 7Fh) where the data is stored.

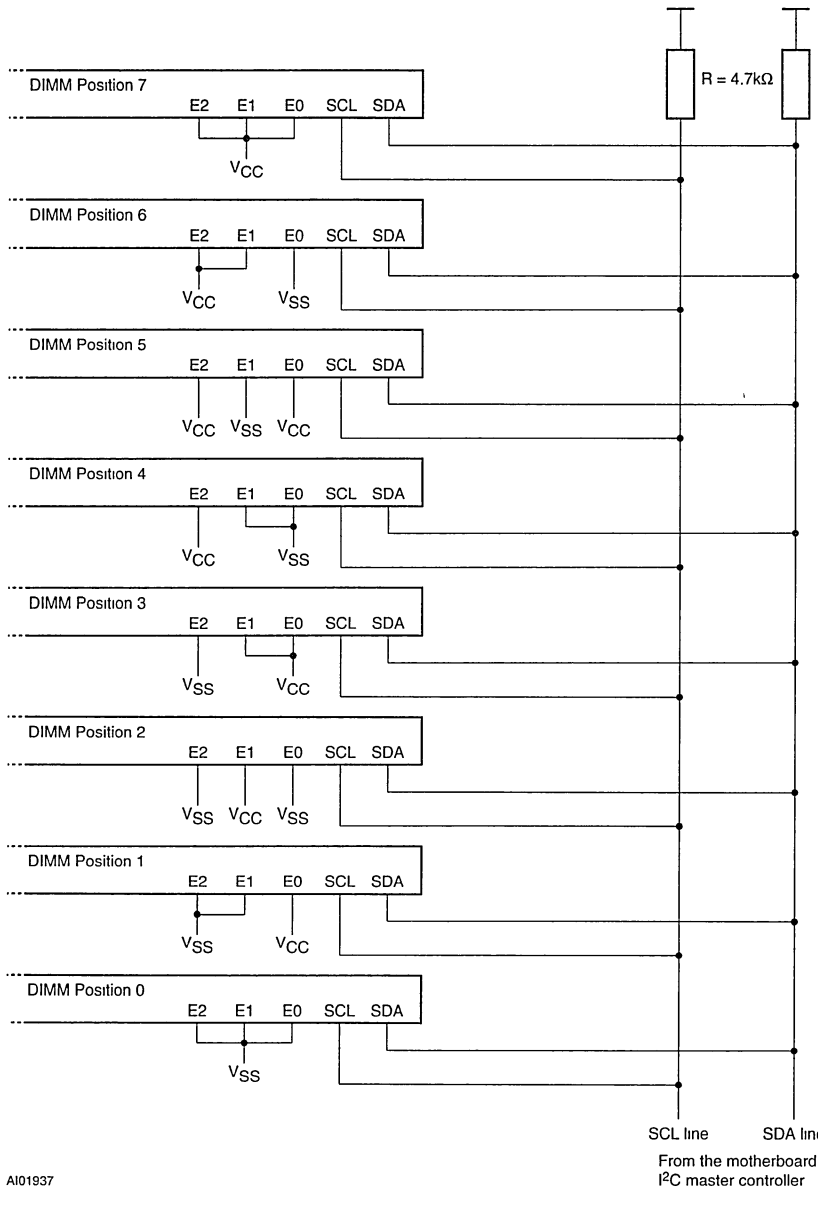
In the application, the M34C02 is soldered directly on the DRAM PCB module.

The 3 Chip Enables (pin 1, 2, 3) of the M34C02 are connected to respectively pins 165, 166, 167 of the 168 pins DRAM DIMM module (see Table 9). They will be wired at V_{CC} or V_{SS} through the DIMM socket. The I/O pins SCL (pin 6) and SDA (pin 5) are connected respectively to pins 83 and 82 of the memory module. The pull-up resistors needed for normal behaviour of the I^2C bus should be connected on the Motherboard I^2C bus (see Figure 12). The Write Control $\overline{WC}$ (pin 7) of the M34C02 can be left unconnected but it is recommended to connect this pin to V_{SS} in order to keep the top half of the memory accessible in read and write mode.

How to Program the M34C02

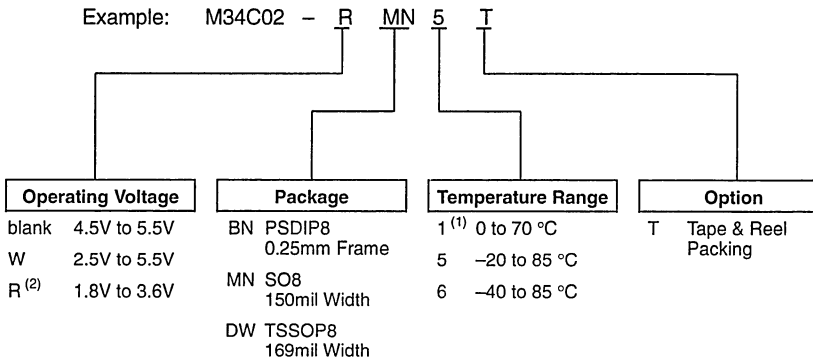
When delivered, all the M34C02 memory area is accessible in read and write. First, it is recommended that the test equipment writes and verifies the module data (configuration, access time, ...) starting from the first memory location of the M34C02. When the data is validated, the test equipment will send a Write command to the protect register using the device select code '01100000b' followed by an address and data byte (don't care values) as shown in Figure 9. After this sequence, the first 128 bytes of the memory area will be write protected and the M34C02 will no longer respond to the specific device select code '0110000xb'. It is not possible to reverse this sequence.

Figure 12. Serial Presence Detect Block Diagram



Notes: 1. E0-E2 are wired at each DIMM socket in a binary sequence for a maximum of 8 devices
2. Common clock and common data are shared across all position.
3. Pull-up resistor (4.7kΩ typical) are required on all SDA and SCL bus lines due to open drain interface.

ORDERING INFORMATION SCHEME



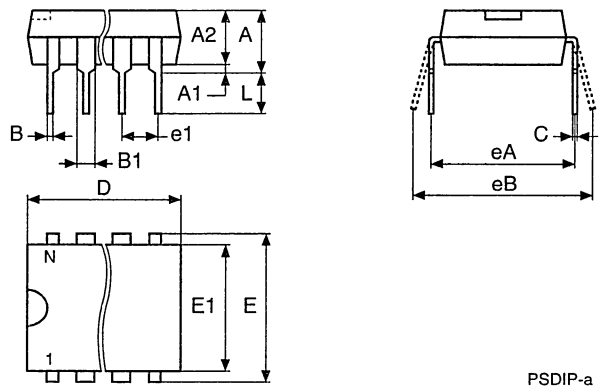
Notes: 1. Temperature range on request only.
2. -R version (1 8V to 3.6V) are only available in temperature ranges 5 or 1.

Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

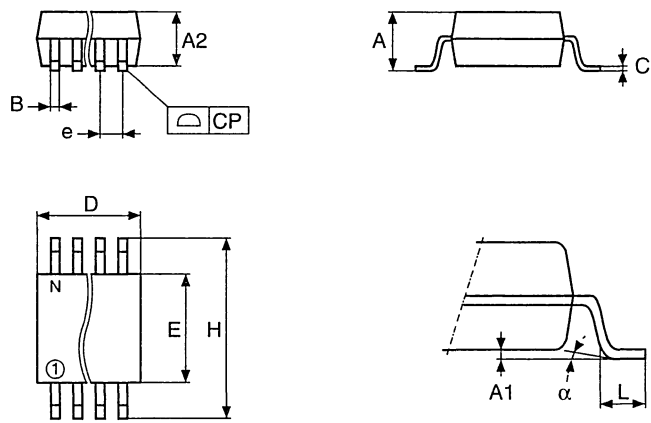


PSDIP-a

Drawing is not to scale.

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

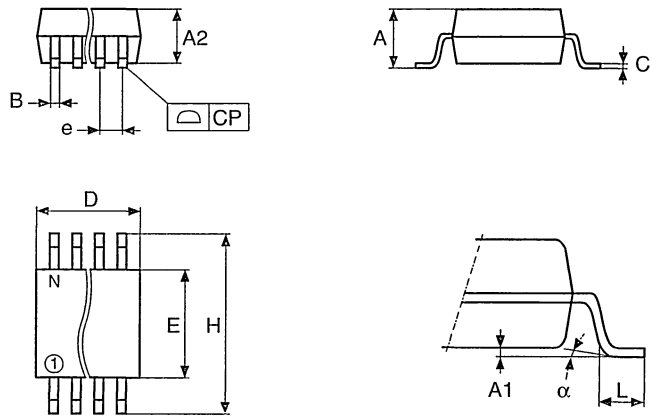


SO-b

Drawing is not to scale.

TSSOP8 - 8 lead Thin Shrink Small Outline

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.10			0.043
A1		0.05	0.15		0.002	0.006
A2		0.85	0.95		0.033	0.037
B		0.19	0.30		0.007	0.012
C		0.09	0.20		0.004	0.008
D		2.90	3.10		0.114	0.122
E		4.30	4.50		0.169	0.177
e	0.65	–	–	0.026	–	–
H		6.25	6.50		0.246	0.256
L		0.50	0.70		0.020	0.028
α		0°	8°		0°	8°
N	8			8		
CP			0.08			0.003



SO-b

Drawing is not to scale.

M35080

8 Kbit Serial SPI Bus EEPROM With Unidirectional Counters

- Compatible with SPI Bus Serial Interface (Positive Clock SPI Modes)
- Single Supply Voltage: 4.5 V to 5.5 V
- 5 MHz Clock Rate (maximum)
- Sixteen 16-bit Unidirectional Counters
- 32 Byte PAGE MODE (except for the Incremental Registers)
- Self-Timed Programming Cycle
- Hardware Protection of the Status Register
- Resizeable Read-Only EEPROM Area
- 4000 V E.S.D. Protection (minimum)
- 1 Million Erase/Write Cycles (minimum)
- 40 Year Data Retention (minimum)

SO8 (MN)
150 mil Width

DESCRIPTION

The M35080 devices consist of 1024x8 bits of low power, serial EEPROM, fabricated with STMicroelectronics' proprietary High Endurance Double Polysilicon CMOS technology. The device is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q).

The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low.

Data is clocked in during the low to high transition of clock C, data is clocked out during the high to low transition of clock C.

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

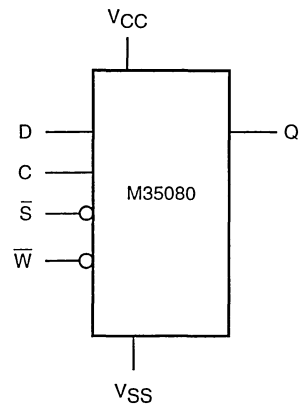
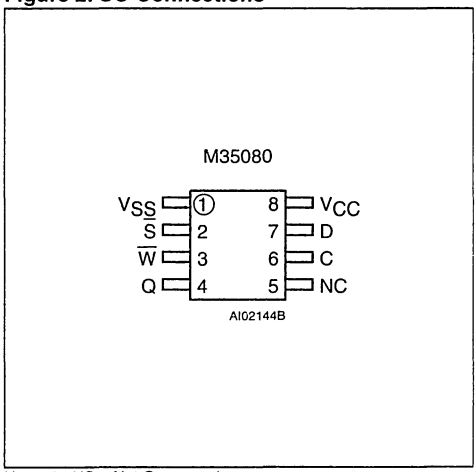


Figure 2. SO Connections



Note: 1. NC = Not Connected

The memory is organized in pages of 32 bytes. However, the first page is treated specially, and is not treated in the same way as the other pages.

The first page is considered to consist of sixteen 16-bit counters. Each counter can be modified using the conventional write instructions, but the new value will only be accepted if it is greater than the value currently held in the counter. Thus, each counter is restricted to counting monotonically upwards.

This is useful in applications where it is necessary to protect the counter from fraudulent tampering (such as in a car odometer, an electricity meter, or a counter of credit remaining).

ORDERING INFORMATION

Devices are shipped from the factory with the memory content set at all '1's (FFh).

The notation used for the device number is as shown in Table 2. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 2. Ordering Information Scheme

Example: M35080 – MN 6 T

Package

MN SO8 (150 mil width)

Temperature Range

1 0 °C to 70 °C

6 –40 °C to 85 °C

3[1] –40 °C to 125 °C

Option

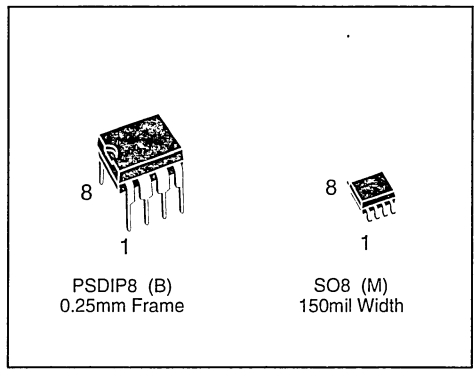
T Tape and Reel Packing

Note. 1. Temperature range available only on request

ST24LC21B, ST24LW21
ST24FC21, ST24FW21

1 Kbit (x8) Dual Mode Serial EEPROM for VESA PLUG & PLAY

- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- 3.6V to 5.5V SINGLE SUPPLY VOLTAGE
- HARDWARE WRITE CONTROL (ST24LW21 and ST24FW21)
- TTL SCHMITT-TRIGGER on VCLK INPUT
- 100k / 400k Hz COMPATIBILITY with the I^2C BUS BIT TRANSFER RANGE
- TWO WIRE SERIAL INTERFACE I^2C BUS COMPATIBLE
- I^2C PAGE WRITE (up to 8 Bytes)
- I^2C BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES
- ERROR RECOVERY MECHANISM (ST24FC21 and ST24FW21) VESA 2 COMPATIBLE



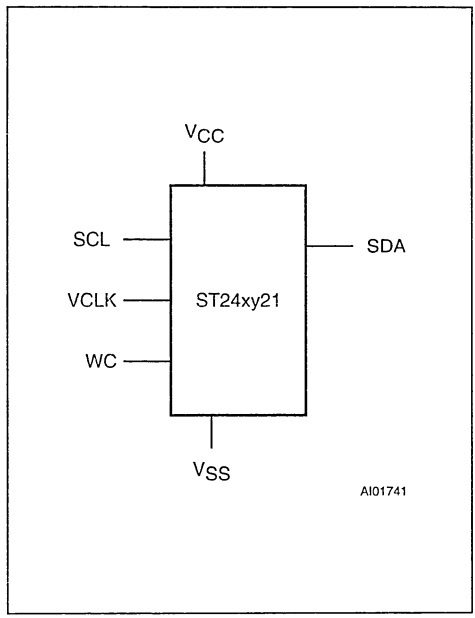
DESCRIPTION

The ST24LC21B, ST24LW21, ST24FC21 and ST24FW21 are 1K bit electrically erasable programmable memory (EEPROM), organized in 128x8 bits. In the text, products are referred as ST24xy21, where "x" is either "L" for VESA 1 or "F" for VESA 2 compatible memories and where "y" indicates the Write Control pin connection: "C" means WC on pin 7 and "W" means WC on pin 3.

Table 1. Signal Names

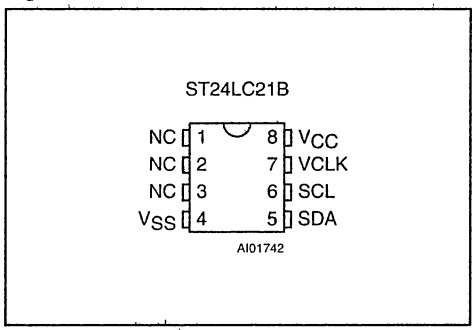
SDA	Serial Data Address Input/Output
SCL	Serial Clock (I^2C mode)
V_{CC}	Supply Voltage
V_{SS}	Ground
VCLK	Clock Transmit only mode
WC	Write Control

Figure 1. Logic Diagram



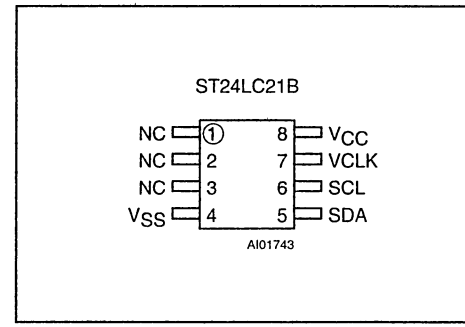
Note: WC signal is only available for ST24LW21 and ST24FW21 products

Figure 2A. DIP Pin Connections



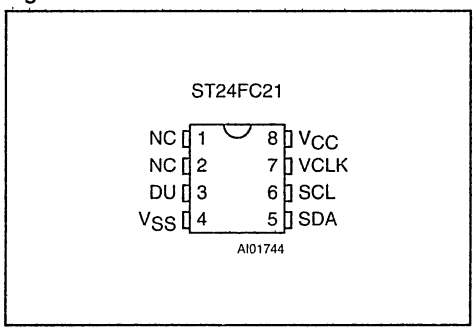
Warning: NC = Not Connected.

Figure 2B. SO Pin Connections



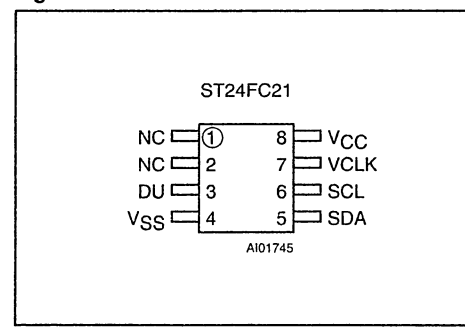
Warning: NC = Not Connected.

Figure 2C. DIP Pin Connections



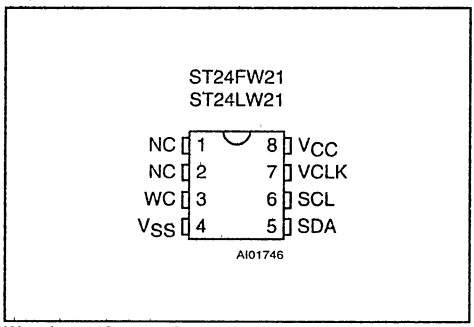
Warning: NC = Not Connected. DU = Don't Use, must be left open or connected to V_{CC} or V_{SS}.

Figure 2D. SO Pin Connections



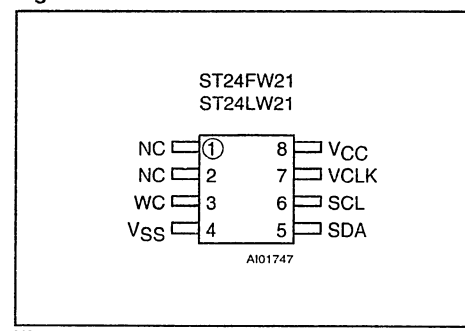
Warning: NC = Not Connected. DU = Don't Use, must be left open or connected to V_{CC} or V_{SS}.

Figure 2E. DIP Pin Connections



Warning: NC = Not Connected.

Figure 2F. SO Pin Connections



Warning: NC = Not Connected.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			–40 to 85	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

Table 3. Device Select Code

	Device Code				Chip Enable			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	X	X	X	RW

Note: The MSB b7 is sent first.
X = 0 or 1.

DESCRIPTION (cont'd)

The ST24xy21 can operate in two modes: Transmit-Only mode and I^2C bidirectional mode. When powered, the device is in Transmit-Only mode with EEPROM data clocked out from the rising edge of the signal applied on VCLK.

The device will switch to the I^2C bidirectional mode upon the falling edge of the signal applied on SCL pin. When in I^2C mode, the ST24LC21B (or the ST24LW21) cannot switch back to the Transmit Only mode (except when the power supply is removed). For the ST24FC21 (or the ST24FW21), after the falling edge of SCL, the memory enter in a transition state which allowed to switch back to the Transmit-Only mode if no valid I^2C activity is observed. The device operates with a power supply value as low as +3.6V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Transmit Only Mode

After a Power-up, the ST24xy21 is in the Transmit Only mode. A proper initialization sequence (see Figure 3) must supply nine clock pulses on the VCLK pin (in order to internally synchronize the device). During this initialization sequence, the SDA pin is in high impedance. On the rising edge of the tenth pulse applied on VCLK pin, the device will output the first bit of byte located at address 00h (most significant bit first).

A byte is clocked out (on SDA pin) with nine clock pulses on VCLK: 8 clock pulses for the data byte and one extra clock pulse for a Don't Care bit.

As long as the SCL pin is held high, each byte of the memory array is transmitted serially on the SDA pin with an automatic address increment.

When the last byte is transmitted, the address counter will roll-over to location 00h.

Figure 3. Transmit Only Mode Waveforms

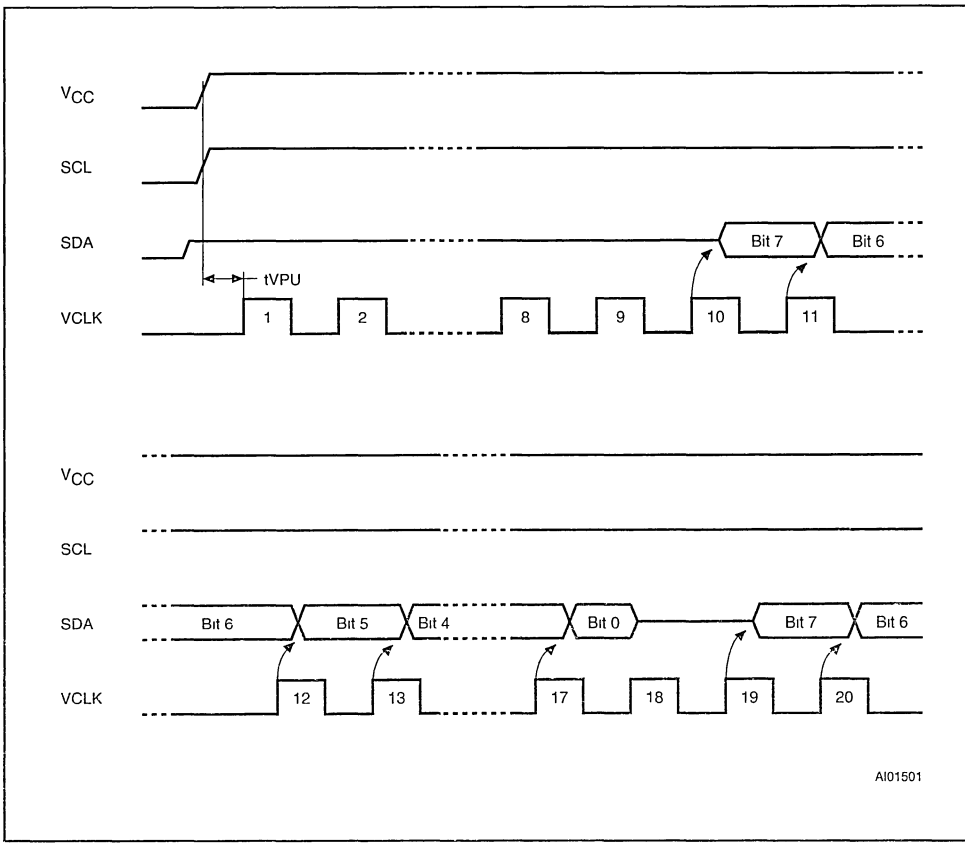
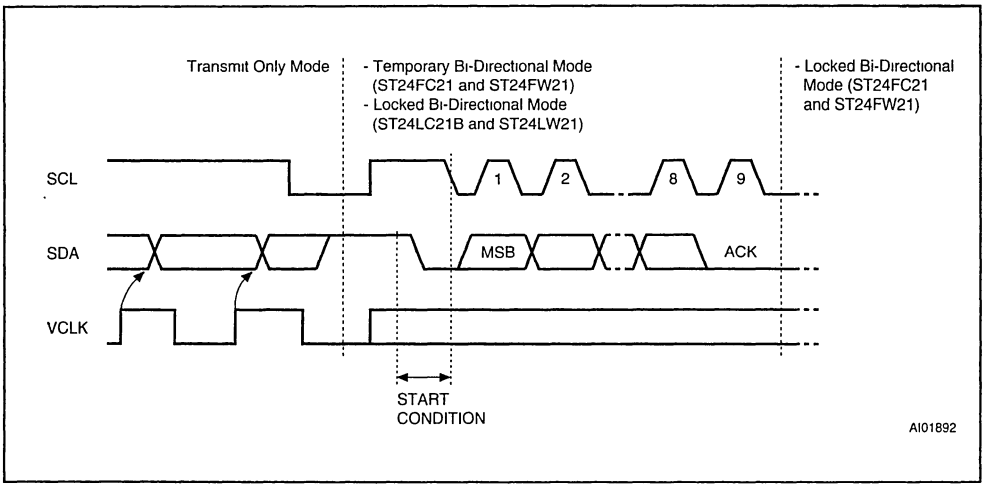


Table 4. I²C Operating Modes

Mode	R/W bit	ST24LC21B ST24FC21 VCLK	ST24LW21 ST24FW21 WC	Bytes	Initial Sequence
Current Address Read	'1'	X	X	1	START, Device Select, R/W = '1'
Random Address Read	'0'	X	X	1	START, Device Select, R/W = '0', Address,
	'1'	X	X		reSTART, Device Select, R/W = '1'
Sequential Read	'1'	X	X	1 to 128	Similar to Current or Random Mode
Byte Write	'0'	V_{IH}	V_{IH}	1	START, Device Select, R/W = '0'
Page Write	'0'	V_{IH}	V_{IH}	8	START, Device Select, R/W = '0'

Note: X = V_{IH} or V_{IL}

Figure 4. Transition from Transmit Only (DDC1) to Bi-directional (DDC2B) Mode Waveforms



I²C Bidirectional Mode

The ST24xy21 can be switched from Transmit Only mode to I²C Bidirectional mode by applying a valid high to low transition on the SCL pin (see Figure 4).

- When the ST24LC21B (or the ST24FC21) is in the I²C Bidirectional mode, the VCLK input (pin 7) enables (or inhibits) the execution of any write instruction: if VCLK = 1, write instructions are executed; if VCLK = 0, write instructions are not executed.
- When the ST24LW21 (or the ST24FW21) is in the I²C Bidirectional mode, the Write Control (WC on pin 3) input enables (or inhibits) the execution of any write instruction: if WC = 1, write instructions are executed;if WC = 0, write instructions are not executed.

The ST24xy21 is compatible with the I²C standard, two wire serial interface which uses a bidirectional data bus and serial clock. The device carries a built-in 4 bit, unique device identification code (1010) named Device Select code corresponding to the I²C bus definition.

The ST24xy21 behaves as a slave device in the I²C protocol with all memory operations synchronized by the serial clock SCL. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (Device Select code 1010XXX), plus one read/write bit and terminated by an acknowledge bit.

When data is written into the memory, the ST24xy21 responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it must acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition (see READ and WRITE descriptions in the following pages).

Power On Reset: V_{CC} lock out write protect

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value (around 3V), the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

Figure 5. Error Recovery Mechanism Flowchart for the ST24FC21 and ST24FW21 products

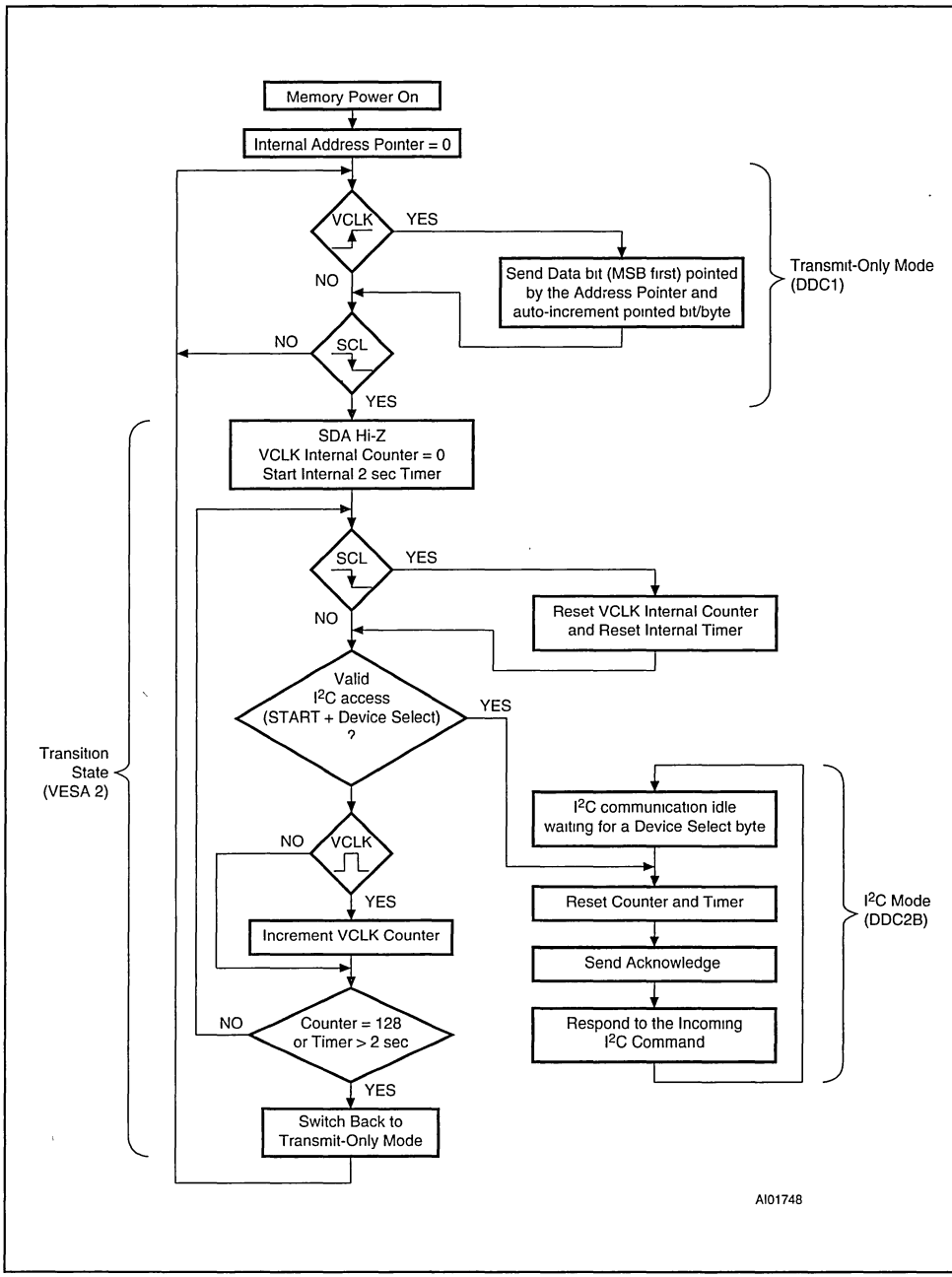
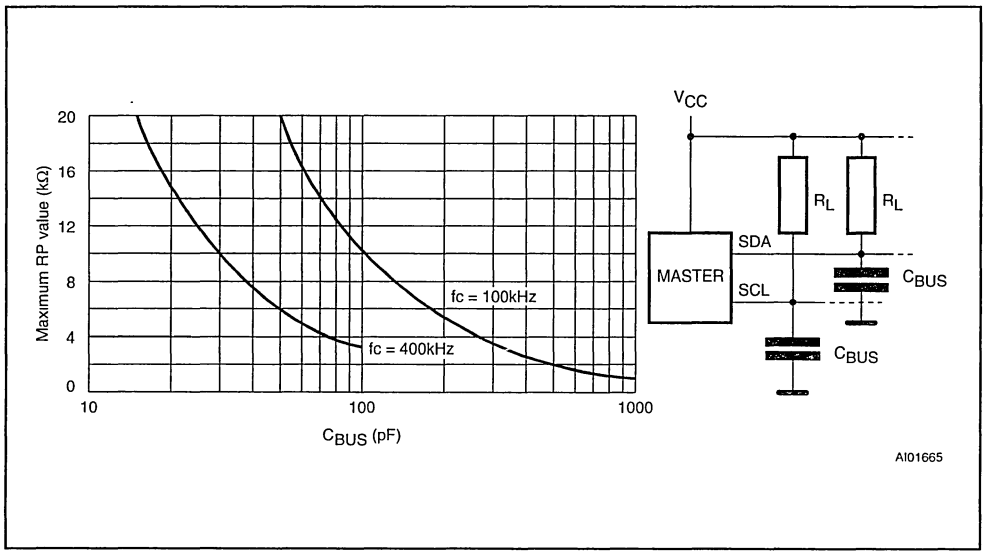


Figure 6. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus



Error Recovery Modes available in the ST24FC21 and the ST24FW21

When the ST24FC21 (or the ST24FW21) first switches to the I^2C mode (VESA DDC2B mode), it enters a transition state which is functionally identical to I^2C operation. But, if the ST24FC21 (or the ST24FW21) does not received a valid I^2C sequence, that is a START condition followed by a valid Device Select code (1010XXX $R\overline{W}$), within either 128 VCLK periods or a period of time of $t_{RECOVERY}$ (approximately 2 seconds), the ST24FC21 (or the ST24FW21) will revert to the Transmit-Only mode (VESA DDC1 mode).

If the ST24FC21 (or the ST24FW21) decodes a valid I^2C Device Select code, it will lock into I^2C mode. Under this condition, signals applied on the VCLK input will not disturb READ access from the ST24FC21 (or the ST24FW21). For WRITE access, refer to the Signal Description paragraph.

When in the transition state, the count of VCLK pulses and the internal 2 seconds timer are reset by any activity on the SCL line. This means that, after each high to low transition on SCL, the memory will re-initialise its transition state and will switch back to Transmit-Only mode only after 128 more VCLK pulses or after a new $t_{RECOVERY}$ delay.

SIGNAL DESCRIPTIONS

I^2C Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 6).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 6).

Transmit Only Clock (VCLK). The VCLK input pin is used to synchronize data out when the ST24xy21 is in Transmit Only mode.

For the ST24LC21B and the ST24FC21 Only, the VCLK offers also a Write Enable (active high) function when the ST24LC21B and the ST24FC21 are in I^2C bidirectional mode.

Write Control (WC). An hardware Write Control feature (WC) is offered only on ST24LW21 and ST24FW21 on pin 3. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable (WC = V_{IL}) or disable (WC = V_{IH}) the internal write protection. When unconnected, the WC input is internally tied to V_{SS} by a 100k ohm pull-down resistor and the memory is write protected.

Table 5. Input Parameters (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)		200	500	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = –40 to 85 °C; V_{CC} = 3.6V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current	V_{CC} = 5V, f_C = 400kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current	V_{CC} = 3.6V, f_C = 400kHz		1	mA
I_{CC1}	Supply Current (Standby)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V, f_C = 0		100	µA
		V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V, f_C = 400kHz		300	µA
I_{CC2}	Supply Current (Standby)	V_{IN} = V_{SS} or V_{CC}, V_{CC} = 3.6V, f_C = 0		30	µA
		V_{IN} = V_{SS} or V_{CC}, V_{CC} = 3.6V, f_C = 400kHz		100	µA
V_{IL}	Input Low Voltage (SCL, SDA, WC)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA, WC)		0.7 V_{CC}	V_{CC} + 1	V
V_P	High Level Threshold Voltage (Schmitt Trigger on VLCK)	V_{CC} = 5.5V	1.4	2.1	V
		V_{CC} = 4.5V	1.2	1.9	V
		V_{CC} = 3.6V	1	1.7	V
V_N	Low Level Threshold Voltage (Schmitt Trigger on VLCK)	V_{CC} = 5.5V	0.6	1.4	V
		V_{CC} = 4.5V	0.5	1.2	V
		V_{CC} = 3.6V	0.4	1	V
V_H	Hysteresis Voltage (Schmitt Trigger on VLCK)	V_{CC} = 5.5V	0.4	1.5	V
		V_{CC} = 4.5V	0.4	1.4	V
		V_{CC} = 3.6V	0.35	1.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3mA, V_{CC} = 3.6V		0.4	V
		I_{OL} = 6mA, V_{CC} = 5V		0.6	V

Table 7. AC Characteristics, I^2C Bidirectional Mode for Clock Frequency = 400kHz
(T_A = –40 to 85 °C; V_{CC} = 3.6V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2} (1)	t_R	Clock Rise Time		300	ns
t_{CL1CL2} (1)	t_F	Clock Fall Time		300	ns
t_{DH1DH2} (1)	t_R	SDA Rise Time	20	300	ns
t_{DL1DL2} (1)	t_F	SDA Fall Time	20	300	ns
t_{CHDX} (2)	$t_{SU\ STA}$	Clock High to Input Transition	600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	600		ns
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	100		ns
t_{CHDH}	$t_{SU.STO}$	Clock High to Input High (STOP)	600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid	200	900	ns
t_{CLQX}	t_{DH}	Clock Low to Data Out Transition	200		ns
f_C	f_{SCL}	Clock Frequency		400	kHz
t_W	t_{WR}	Write Time		10	ms

Notes: 1. Sampled only, not 100% tested.
2. For a reSTART condition, or following a write cycle.

DEVICE OPERATION

I^2C Bus Background

The ST24xy21 supports the I^2C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24xy21 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24xy21 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24xy21 and the bus master. A STOP condition at the end of a Read command (after the No ACK) forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input, the ST24xy21 sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Table 8. AC Characteristics, I^2C Bidirectional Mode for Clock Frequency = 100kHz
(T_A = –40 to 85 °C; V_{CC} = 3.6V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV} (2)	t_{AA}	Clock Low to Next Data Out Valid	0.2	3.5	µs
t_{CLQX}	t_{DH}	Data Out Hold Time	200		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_W	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. The minimum value delays the falling/rising edge of SDA away from SCL = 1 in order to avoid unwanted START and/or STOP conditions.

Table 9. AC Characteristics, Transmit-only Mode
(T_A = –40 to 85 °C; V_{CC} = 3.6V to 5.5V)

Symbol	Alt	Parameter	Min	Max	Unit
t_{VCHQX}	t_{VAA}	Output Valid from VCLK		500	ns
t_{VCHVCL}	t_{VHIGH}	VCLK High Time	600		ns
t_{VCLVCH}	t_{VLOW}	VCLK Low Time	1.3		µs
t_{CLQZ}	t_{VHZ}	Mode Tansition Time		500	ns
t_{VPU} (1,2)		Transmit-only Power-up Time	0		ns
t_{VH1VH2} (2)	t_R	VCLK Rise Time		1	µs
t_{VL1VL2} (2)	t_F	VCLK Fall Time		1	µs
$t_{RECOVERY}$ (2)		Recovery Time	1.5	3.5	sec

Notes: 1. Refer to Figure 3.
2. Sampled only, not 100% tested.

Figure 7. AC Waveforms

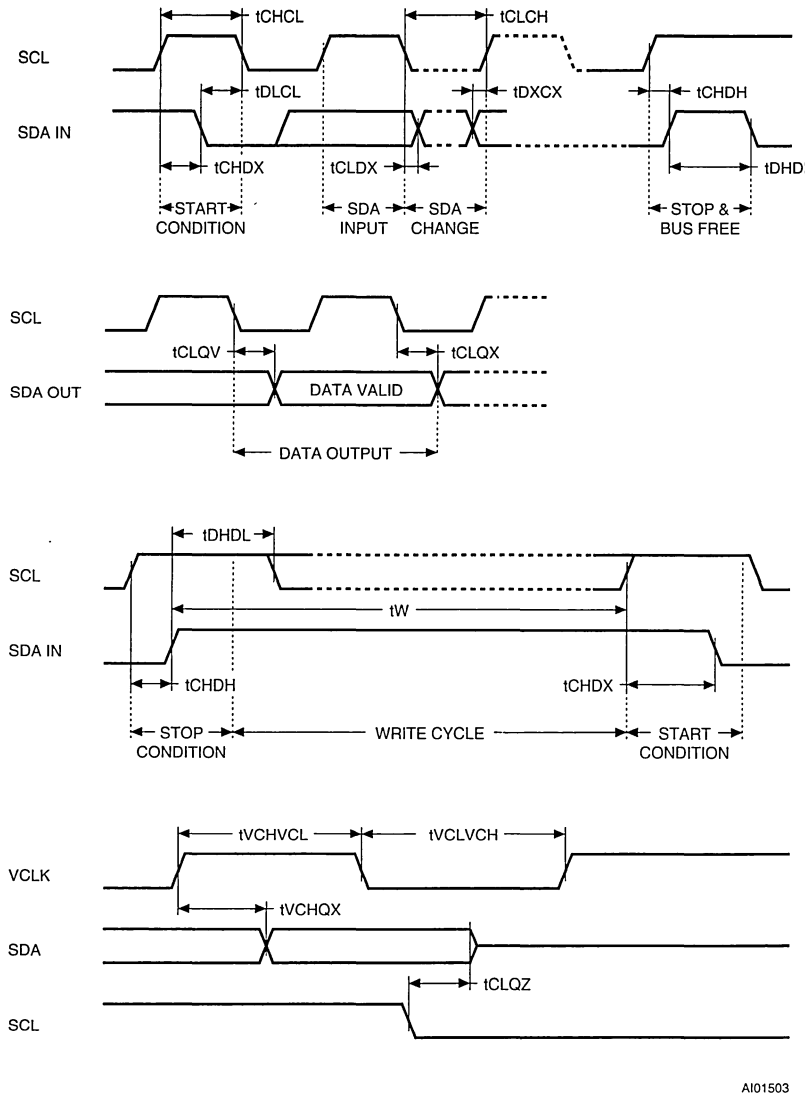


Table 10. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages SDA, SCL	$0.2V_{CC}$ to $0.8V_{CC}$
Input Pulse Voltages V_{CLK}	0.4V to 2.4V
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 8. AC Testing Input Output Waveforms

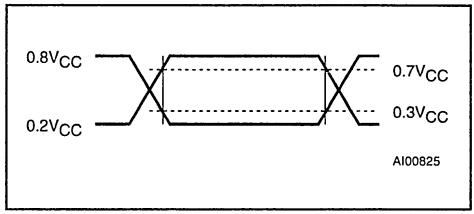


Figure 9. I^2C Bus Protocol

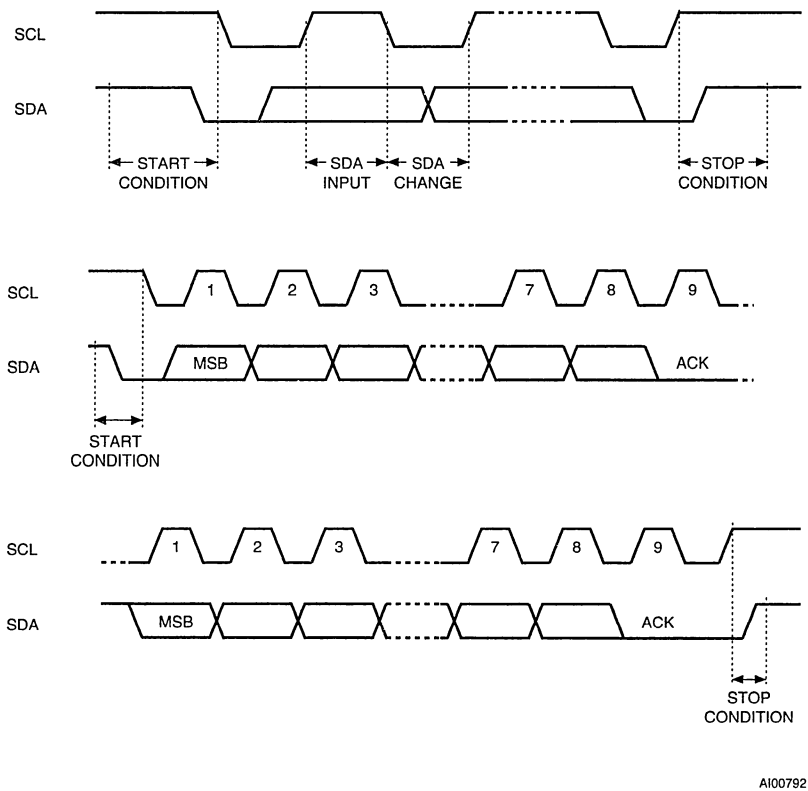
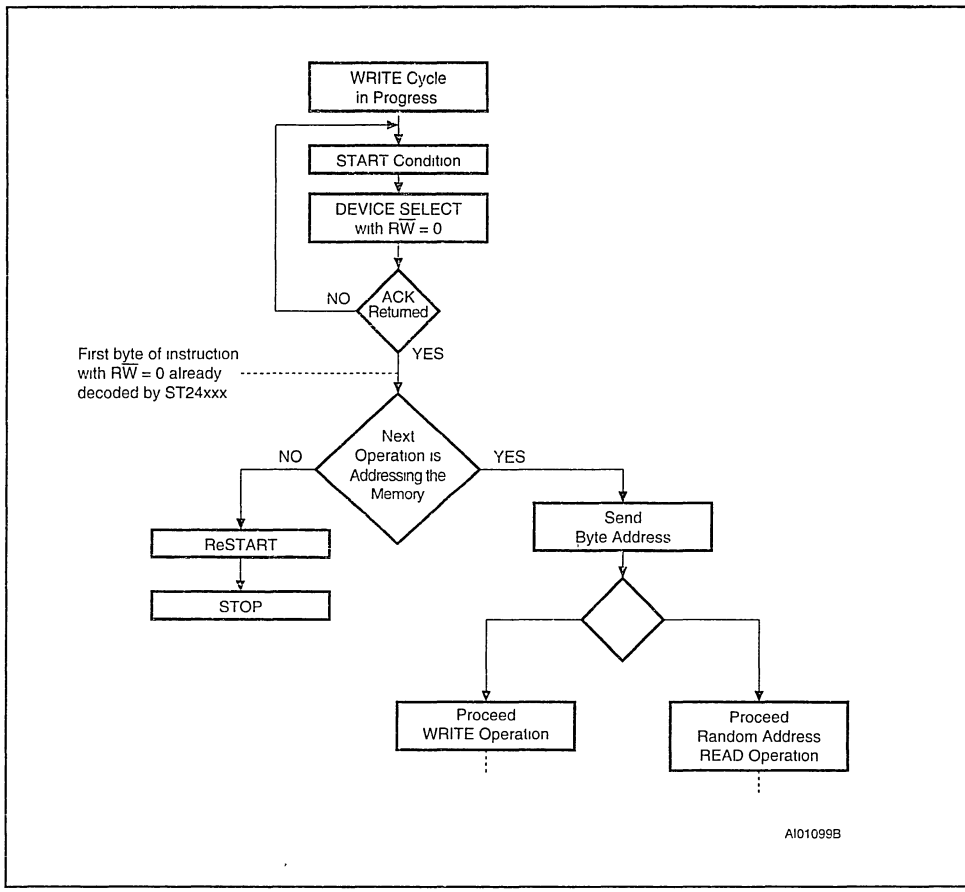


Figure 10. Write Cycle Polling using ACK



Memory Addressing. To start communication between the bus master and the slave ST24xy21, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the Device Select code (7 bits) and a READ or WRITE bit. The 4 most significant bits of the Device Select code are the device type identifier, corresponding to the I^2C bus definition. For these memories the 4 bits are fixed as 1010b. The following 3 bits are Don't Care. The 8th bit sent is the read or write bit ($\overline{RW}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

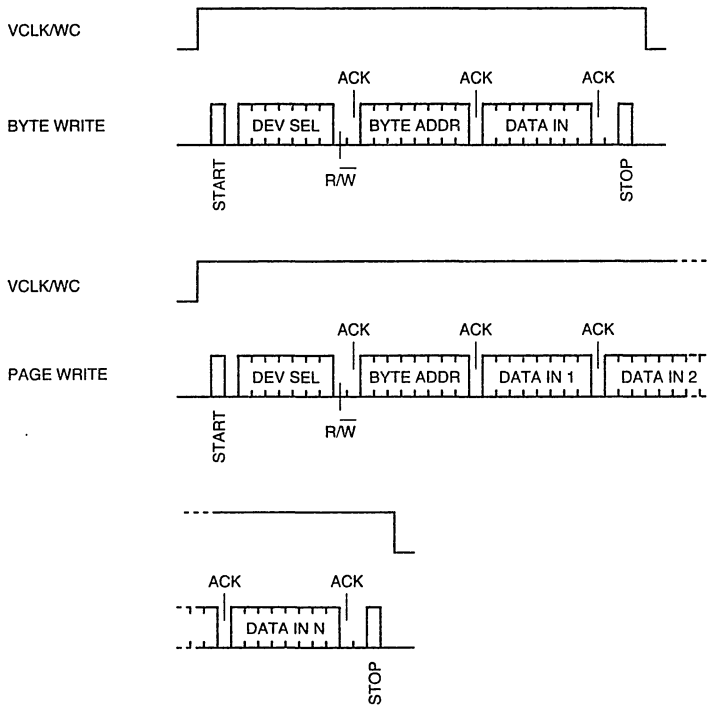
Write Operations

Following a START condition the master sends a Device Select code with the $\overline{RW}$ bit set to '0'. The memory acknowledges this and waits for a byte address. After receipt of the byte address the device again responds with an acknowledge.

In I^2C bidirectional mode, any write command with VCLK=0 (for the ST24LC21B and ST24FC21) or with WC=0 (for the ST24LW21 and ST24FW21) will not modify data and will be acknowledged on data bytes, as shown in Figure 12.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition.

Figure 11. Write Modes Sequence



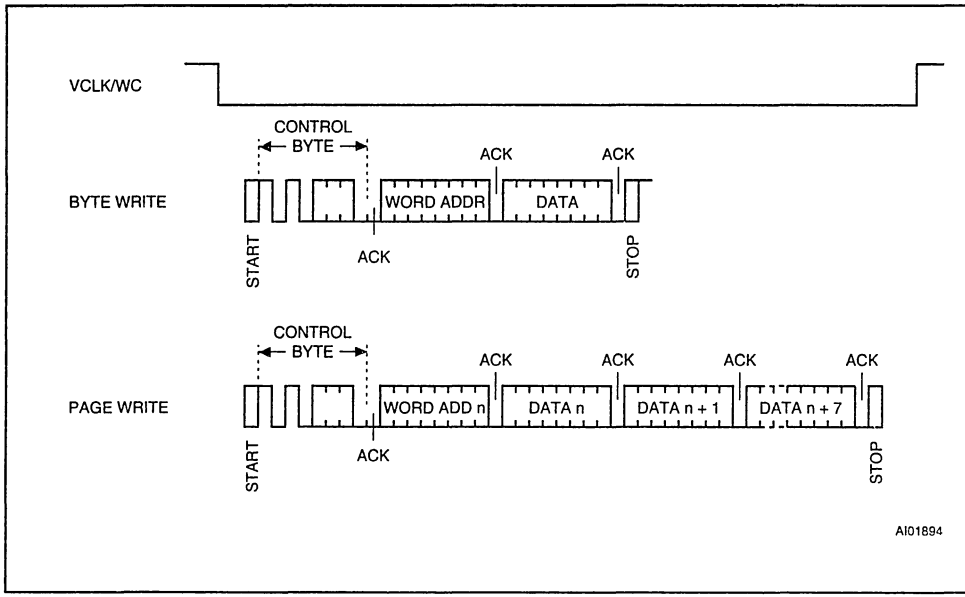
Page Write. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the most significant memory address bits are the same. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory.

After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master. The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 10).
- Step 1: the Master issues a START condition followed by a Device Select byte (1st byte of the new instruction).

Figure 12. Inhibited Write when VCLK/WC = 0



– Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the instruction (the first byte of this instruction was already sent during Step 1).

Read Operations

On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends the Device Select code with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the data byte addressed by the internal byte address counter. This counter is then incremented. The master must NOT acknowledge the data byte output and terminates the transfer with a STOP condition.

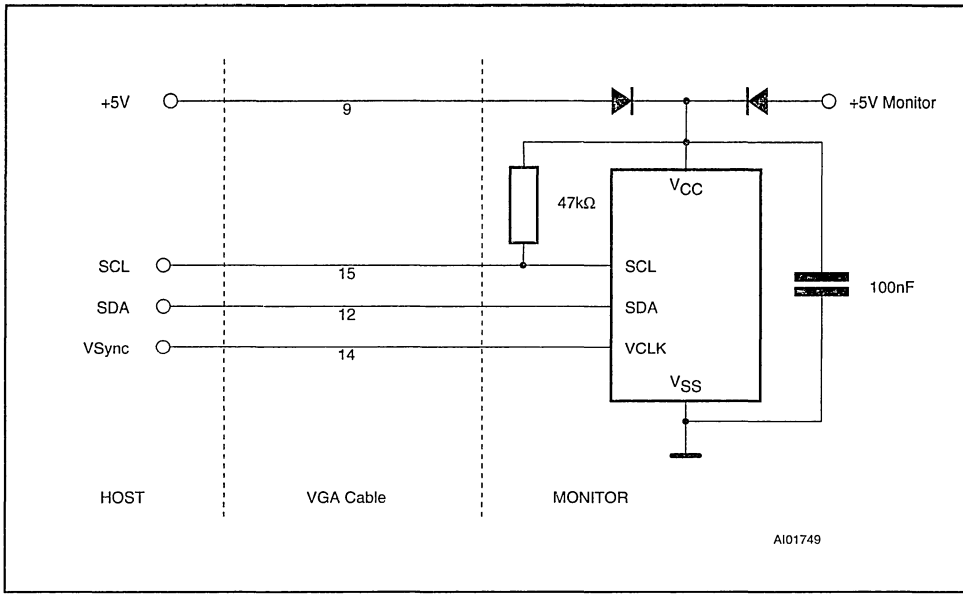
Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 14. This is followed by a Re-START condition send by the master and the Device Select code is repeated with the RW bit set to '1'. The memory acknowledges this and outputs the addressed data byte. The master must NOT acknowledge the data byte output and terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last data byte output, and MUST generate a STOP condition.

The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST24xy21 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24xy21 terminate the data transfer and switches to a standby state.

Figure 13. Recommended Schematic for VESA 2.0 Specification



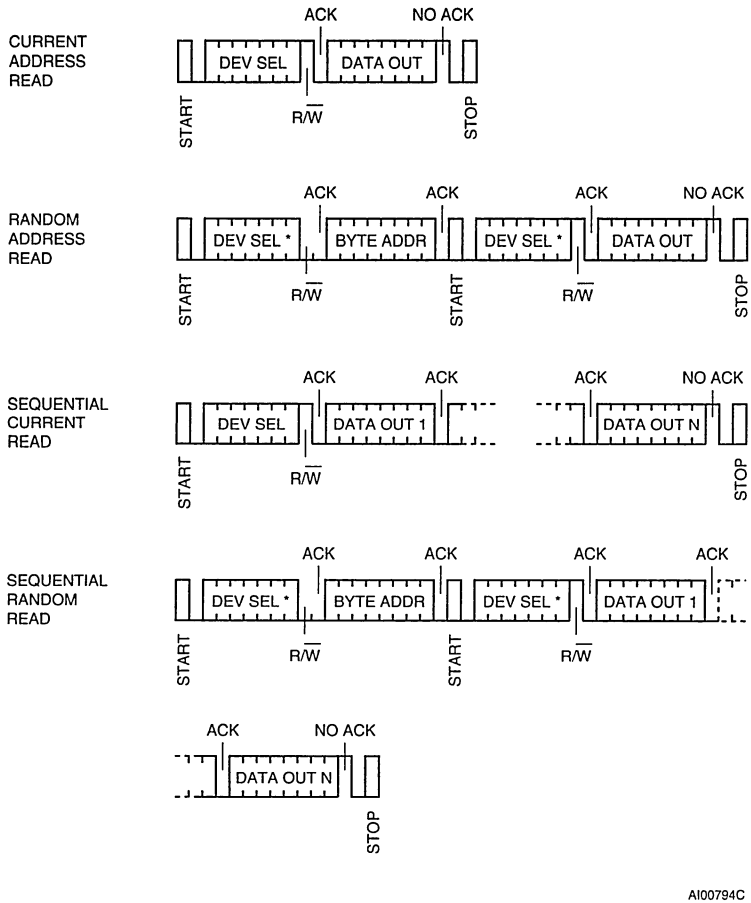
NOTE CONCERNING THE POWER SUPPLY VOLTAGE IN THE VESA 2.0 SPECIFICATION

According to the VESA 2.0 specification, the ST24xy21 can be supplied by either the MONITOR or by the HOST (using +5V on the VGA cable pin 9) power supply. The easyest way to implement this is to use 2 diodes as described in the following schematic. The ST24xy21 supply voltage will be decreased by 0.6V, which is the diode forward voltage drop, and will be below 4.5V. Nevertheless, the ST24xy21 remains operational and no input will be damaged if the applied voltage on any input complies with the Absolute Maximum Ratings values.

Under this condition, the threshold voltage of the Schmitt-Trigger (pin 7) will be decreased (as in Table 6).

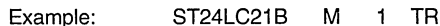
Refer to the AN627 Application Note for more detailed information regarding the use and the protection of the ST24xy21 in a Monitor application.

Figure 14. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical.

ORDERING INFORMATION SCHEME



Family Range		Package		Temperature Range		Option	
ST24LC21B	VESA 1 WC on pin 7	B	PSDIP8 0.25mm Frame	1	0 to 70 °C	TR	Tape & Reel Packing
ST24LW21	VESA 1 WC on pin 3	M	SO8 150mil Width	6	–40 to 85 °C		
ST24FC21	VESA 2 WC on pin 7						
ST24FW21	VESA 2 WC on pin 3						

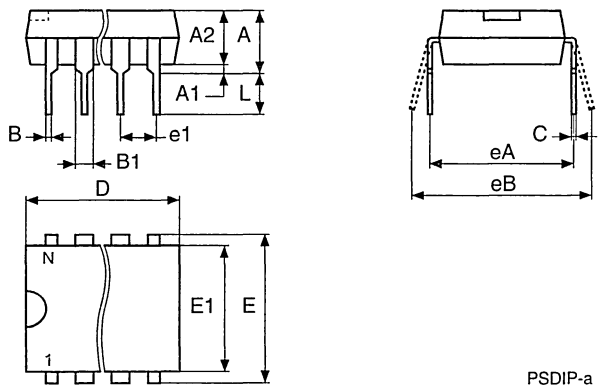
Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8



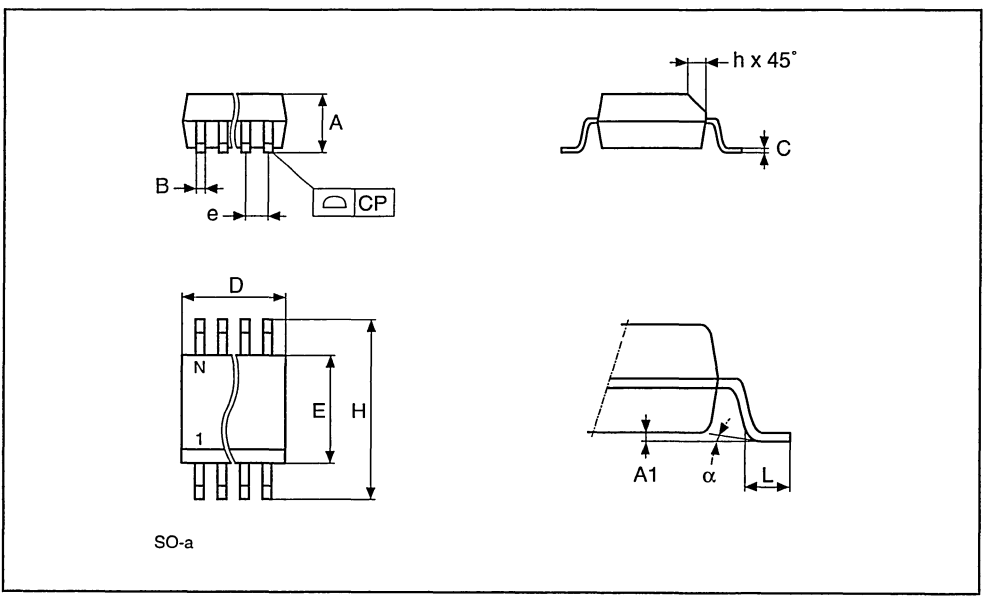
PSDIP-a

Drawing is not to scale.

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N		8			8	
CP			0.10			0.004

SO8



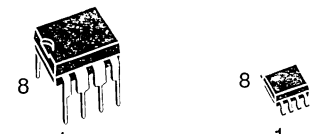
SO-a

Drawing is not to scale.

ST24C04, ST25C04
ST24W04, ST25W04

4 Kbit Serial I^2C Bus EEPROM with User-Defined Block Write Protection

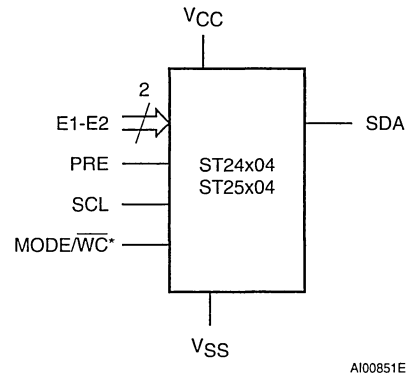
- 1 MILLION ERASE/WRITE CYCLES with 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24x04 versions
  - 2.5V to 5.5V for ST25x04 versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W04 and ST25W04
- PROGRAMMABLE WRITE PROTECTION
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 4 BYTES)
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES



PSDIP8 (B)
0.25mm Frame

SO8 (M)
150mil Width

Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W04 products

DESCRIPTION

This specification covers a range of 4 Kbits I^2C bus EEPROM products, the ST24/25C04 and the ST24/25W04. In the text, products are referred to as ST24/25x04, where "x" is: "C" for Standard version and "W" for hardware Write Control version.

Table 1. Signal Names

PRE	Write Protect Enable
E1-E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

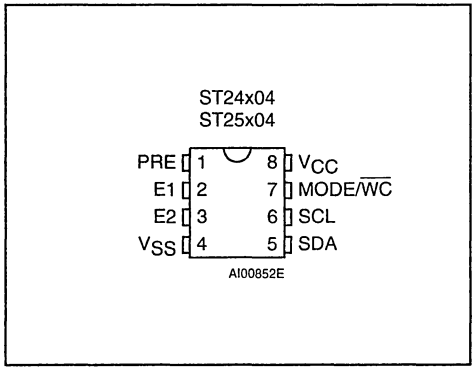


Figure 2B. SO Pin Connections

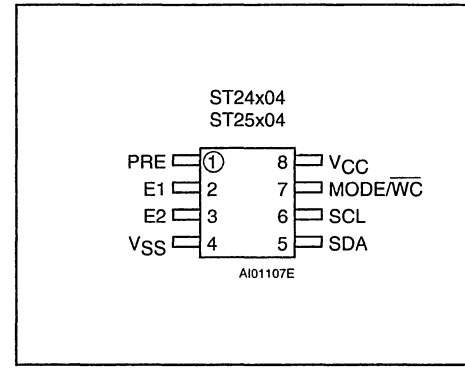


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		–40 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V_{IO}	Input or Output Voltages		–0.6 to 6.5	V
V_{CC}	Supply Voltage		–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents
2. MIL-STD-883C, 3015 7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The ST24/25x04 are 4 Kbit electrically erasable programmable memories (EEPROM), organized as 2 blocks of 256 x8 bits. They are manufactured in STMicroelectronics's Hi-Endurance Advanced CMOS technology which guarantees an endurance of one million erase/write cycles with a data retention of 40 years.

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. This is used together with 2 chip enable inputs (E2, E1) so that up to 4 x 4K devices may be attached to the I^2C bus and selected individually. The memories behave as a slave device in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code 1010), plus one read/write bit and terminated by an acknowledge bit.

Table 3. Device Select Code

	Device Code				Chip Enable		Block Select	$R\overline{W}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	A8	$R\overline{W}$

Note: The MSB b7 is sent first.

Table 4. Operating Modes (1)

Mode	$R\overline{W}$ bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, $R\overline{W}$ = '1'
Random Address Read	'0'	X	1	START, Device Select, $R\overline{W}$ = '0', Address,
	'1'			reSTART, Device Select, $R\overline{W}$ = '1'
Sequential Read	'1'	X	1 to 512	Similar to Current or Random Mode
Byte Write	'0'	X	1	START, Device Select, $R\overline{W}$ = '0'
Multibyte Write (2)	'0'	V_{IH}	4	START, Device Select, $R\overline{W}$ = '0'
Page Write	'0'	V_{IL}	8	START, Device Select, $R\overline{W}$ = '0'

Notes: 1. X = V_{IH} or V_{IL}
2 Multibyte Write not available in ST24/25W04 versions.

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Chip Enable (E1 - E2). These chip enable inputs are used to set the 2 least significant bits (b2, b3) of the 7 bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Protect Enable (PRE). The PRE input pin, in addition to the status of the Block Address Pointer bit (b2, location 1FFh as in Figure 7), sets the PRE write protection active.

Mode (MODE). The MODE input is available on pin 7 (see also $\overline{WC}$ feature) and may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. When unconnected, the MODE input is internally read as V_{IH} (Multibyte Write mode).

Write Control ($\overline{WC}$). An hardware Write Control feature ($\overline{WC}$) is offered only for ST24W04 and ST25W04 versions on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ = V_{IH}) or disable ($\overline{WC}$ = V_{IL}) the internal write protection. When unconnected, the $\overline{WC}$ input is internally read as V_{IL} and the memory area is not write protected.

SIGNAL DESCRIPTIONS (cont'd)

The devices with this Write Control feature no longer support the Multibyte Write mode of operation, however all other write modes are fully supported.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

DEVICE OPERATION

I²C Bus Background

The ST24/25x04 support the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25x04 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25x04 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25x04 and the bus master. A STOP condition at the end of a Read command, after and only after a No Acknowledge, forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25x04 sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24/25x04, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I²C Bus

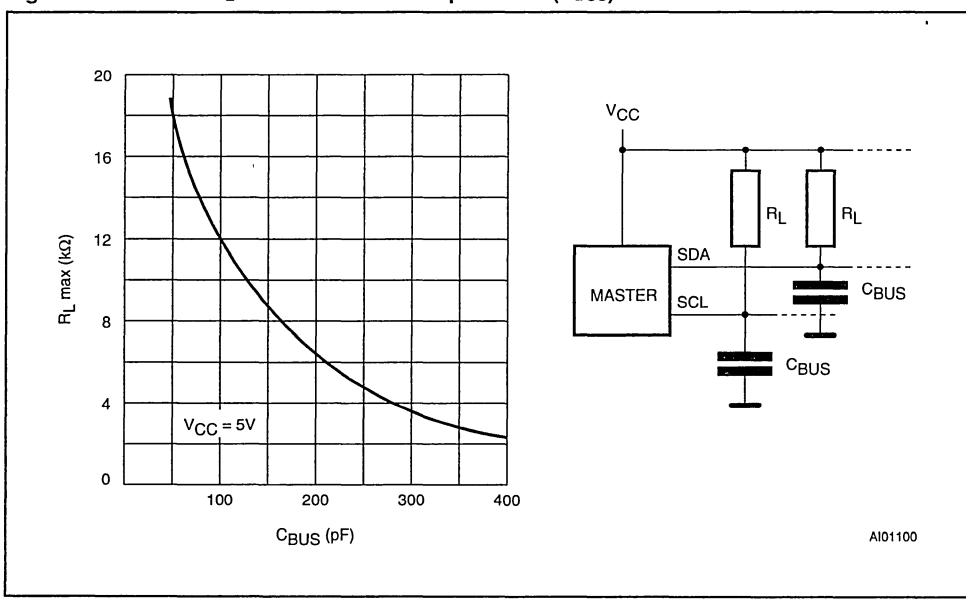


Table 5. Input Parameters [1] (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance (ST24/25W04)	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance (ST24/25W04)	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current (ST24 series)	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2.5V, f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby) (ST24 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 100kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E1-E2, PRE, MODE, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E1-E2, PRE, MODE, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage (ST24 series)	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V

Table 7. AC Characteristics
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

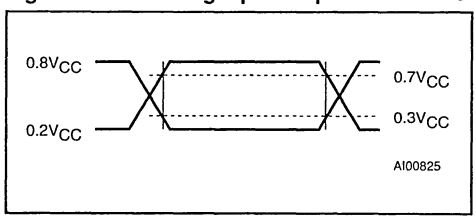
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV} (2)	t_{AA}	Clock Low to Next Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Data Out Hold Time	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_W (3)	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle
2. The minimum value delays the falling/rising edge of SDA away from SCL = 1 in order to avoid unwanted START and/or STOP conditions.
3. In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (6 address MSB are not constant) the maximum programming time is doubled to 20ms

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms

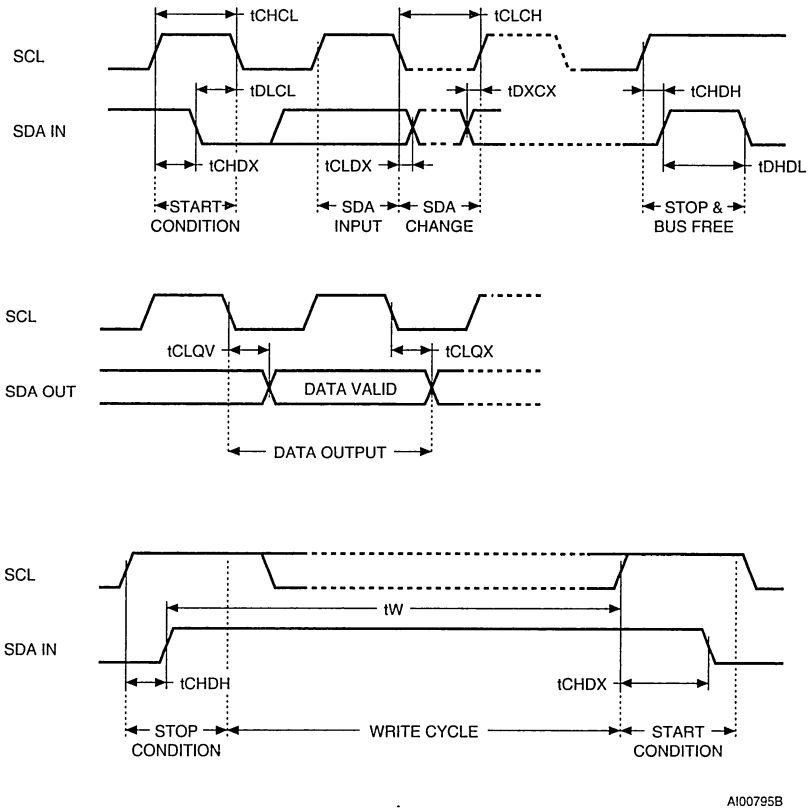


DEVICE OPERATION (cont'd)

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For these memories the 4 bits are fixed as 1010b. The following 2 bits identify the specific memory on the bus. They are matched to the chip enable signals E2, E1. Thus up to 4 x 4K memories can be connected on the same bus giving a memory capacity total of 16 Kbits. After a START condition any memory on the bus will identify the device code and compare the following 2 bits to its chip enable inputs E2, E1.

The 7th bit sent is the block number (one block = 256 bytes). The 8th bit sent is the read or write bit ($\overline{RW}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Figure 5. AC Waveforms



Write Operations

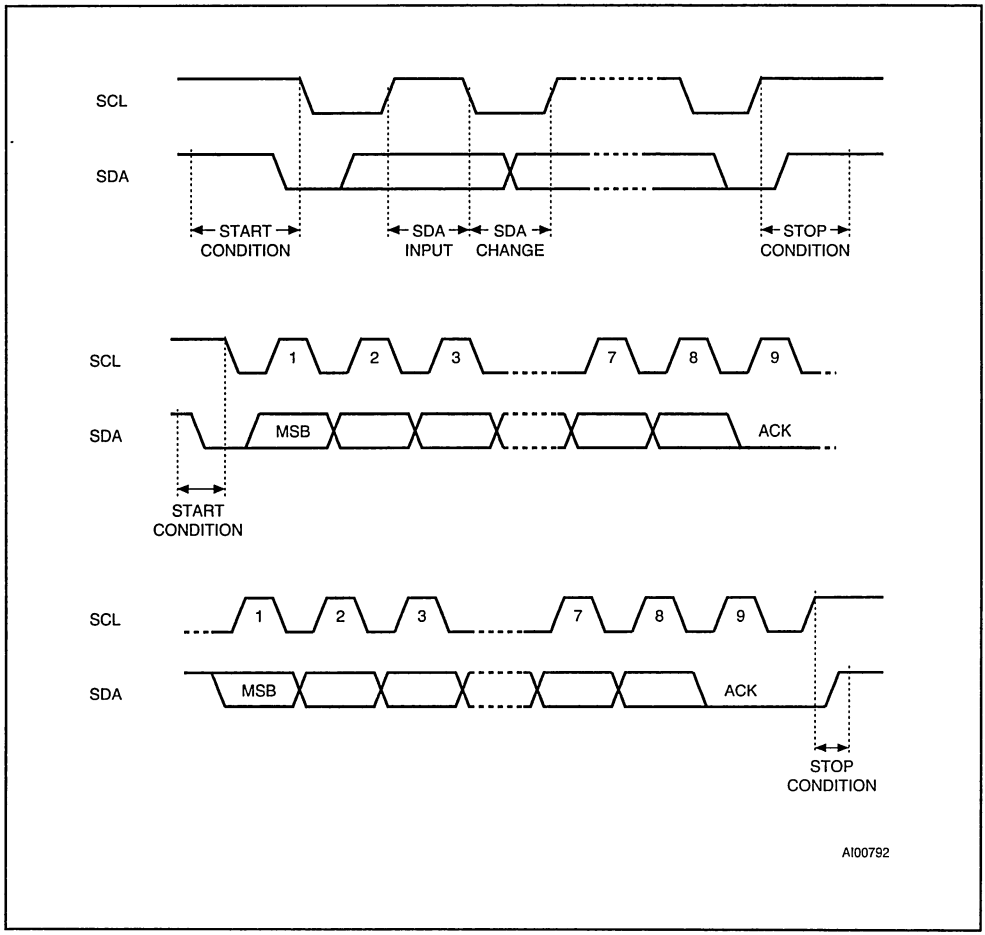
The Multibyte Write mode (only available on the ST24/25C04 versions) is selected when the MODE pin is at V_{IH} and the Page Write mode when MODE pin is at V_{IL}. The MODE pin may be driven dynamically with CMOS input levels.

Following a START condition the master sends a device select code with the $\overline{RW}$ bit reset to '0'. The memory acknowledges this and waits for a byte address. The byte address of 8 bits provides access to one block of 256 bytes of the memory. After receipt of the byte address the device again responds with an acknowledge.

For the ST24/25W04 versions, any write command with $\overline{WC}$ = 1 will not modify the memory content.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition. The Write mode is independant of the state of the MODE pin which could be left floating if only this mode was to be used. However it is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL}, to minimize the stand-by current.

Figure 6. I²C Bus Protocol



Multibyte Write. For the Multibyte Write mode, the MODE pin must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 4 bytes of data, which are each acknowledged by the memory. The transfer is terminated by the master generating a STOP condition. The duration of the write cycle is t_W = 10ms maximum except when bytes are accessed on 2 rows (that is have different values for the 6 most significant address bits A7-A2), the programming time is then doubled to a maximum of 20ms. Writing more than 4 bytes in the Multibyte Write mode may modify data bytes in an adjacent row (one row is 8 bytes long). However, the Multibyte Write can properly write up to 8 consecutive bytes as soon as the first address of these 8 bytes is the first address of the row, the 7 following bytes being written in the 7 following bytes of this same row.

Page Write. For the Page Write mode, the MODE pin must be at V_{IL}. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant mem-

ory address bits (A7-A3) are the same inside one block. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master.

Figure 7. Memory Protection

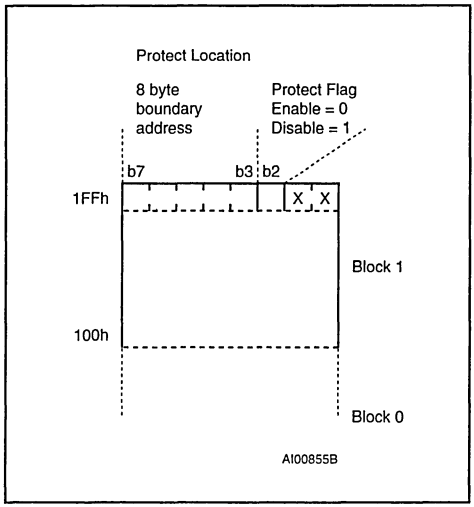


Figure 8. Write Cycle Polling using ACK

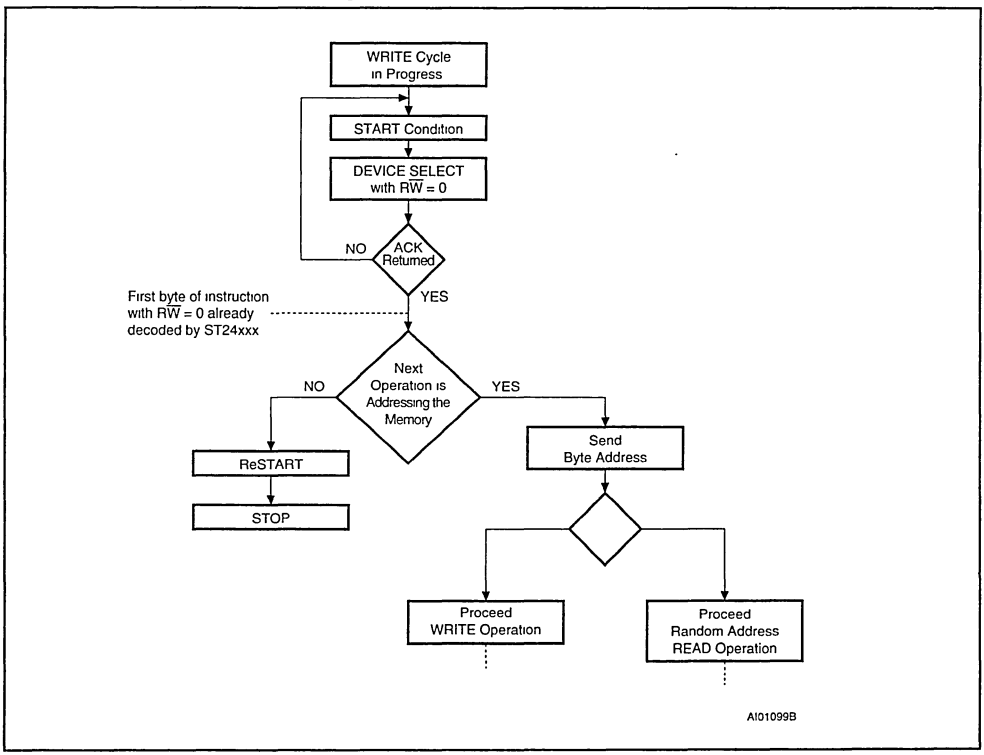
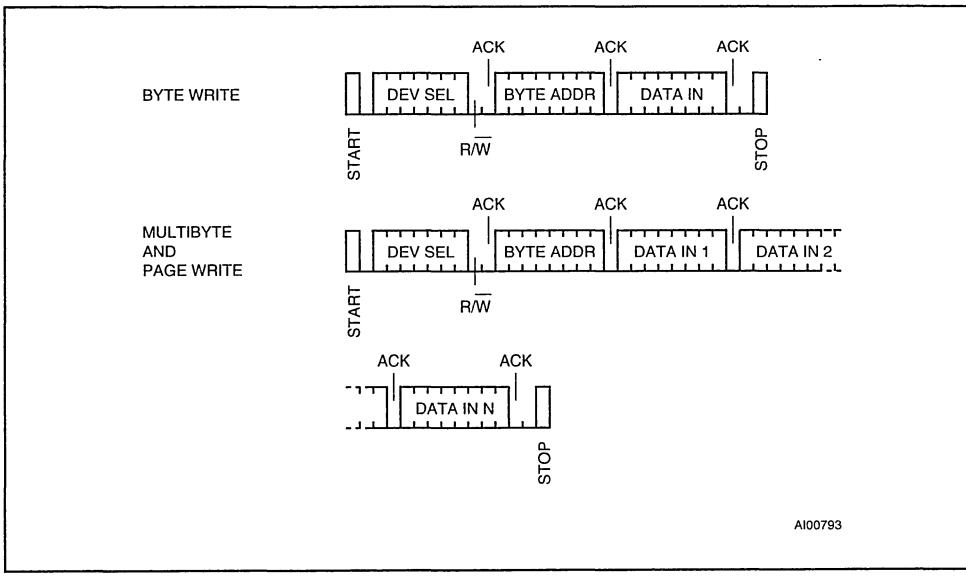


Figure 9. Write Modes Sequence (ST24/25C04)



DEVICE OPERATION (cont'd)

The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 8).
- Step 1: the Master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

Write Protection. Data in the upper block of 256 bytes of the memory may be write protected. The memory is write protected between a boundary address and the top of memory (address 1FFh) when the PRE input pin is taken high and when the Protect Flag (bit b2 in location 1FFh) is set to '0'. The boundary address is user defined by writing it in the Block Address Pointer. The Block Address Pointer is an 8 bit EEPROM register located at the address 1FFh. It is composed by 5 MSBs Address Pointer, which defines the bottom boundary address, and 3 LSBs which must be programmed at '0'. This Address Pointer can therefore address a boundary in steps of 8 bytes.

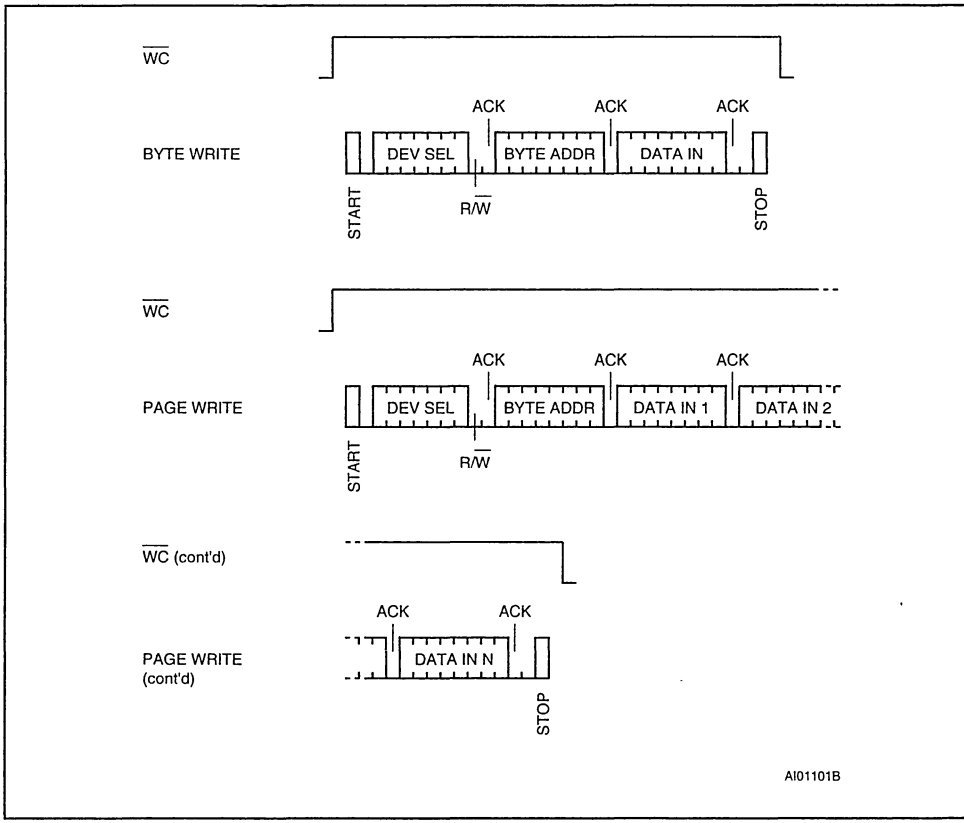
The sequence to use the Write Protected feature is:

- write the data to be protected into the top of the memory, up to, but not including, location 1FFh;
- set the protection by writing the correct bottom boundary address in the Address Pointer (5 MSBs of location 1FFh) with bit b2 (Protect flag) set to '0'. Note that for a correct fonctionality of the memory, all the 3 LSBs of the Block Address Pointer must also be programmed at '0'.

The area will now be protected when the PRE input pin is taken High. While the PRE input pin is read at '0' by the memory, the location 1FFh can be used as a normal EEPROM byte.

Caution: Special attention must be used when using the protect mode together with the Multibyte Write mode (MODE input pin High). If the Multibyte Write starts at the location right below the first byte of the Write Protected area, then the instruction will write over the first 3 bytes of the Write Protected area. The area protected is therefore smaller than the content defined in the location 1FFh, by 3 bytes. This does not apply to the Page Write mode as the address counter 'roll-over' and thus cannot go above the 8 bytes lower boundary of the protected area.

Figure 10. Write Modes Sequence with Write Control = 1 (ST24/25W04)



Read Operations

Read operations are independent of the state of the MODE pin. On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the R$\overline{W}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 11. This is followed by another START condition from the master and the byte address is repeated with the R$\overline{W}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master have to NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

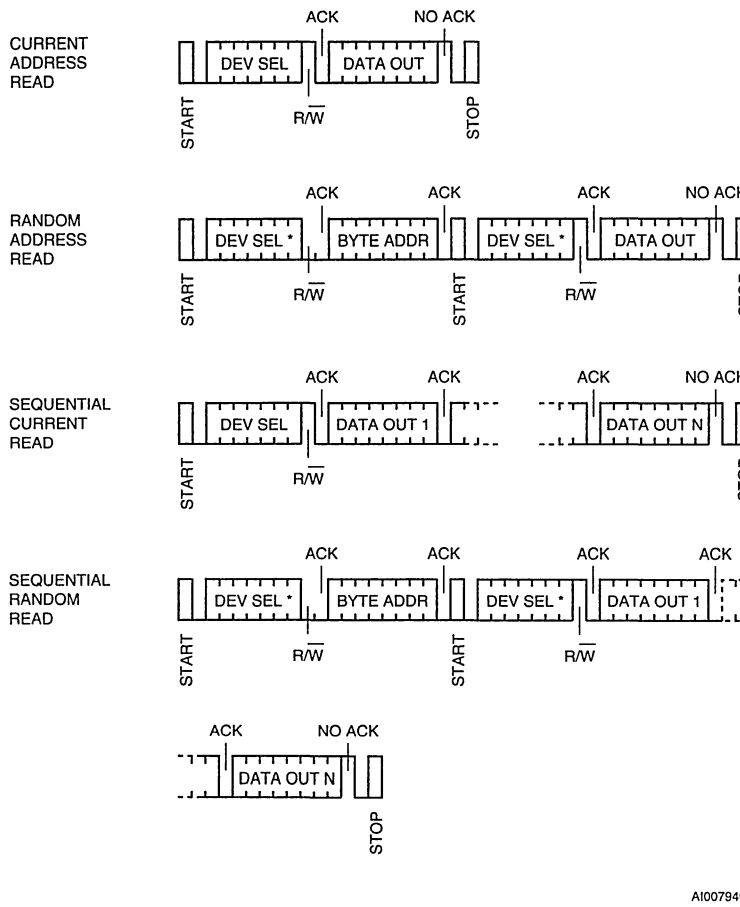
Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte out-

DEVICE OPERATION (cont'd)

put, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll- over' and the memory will continue to output data.

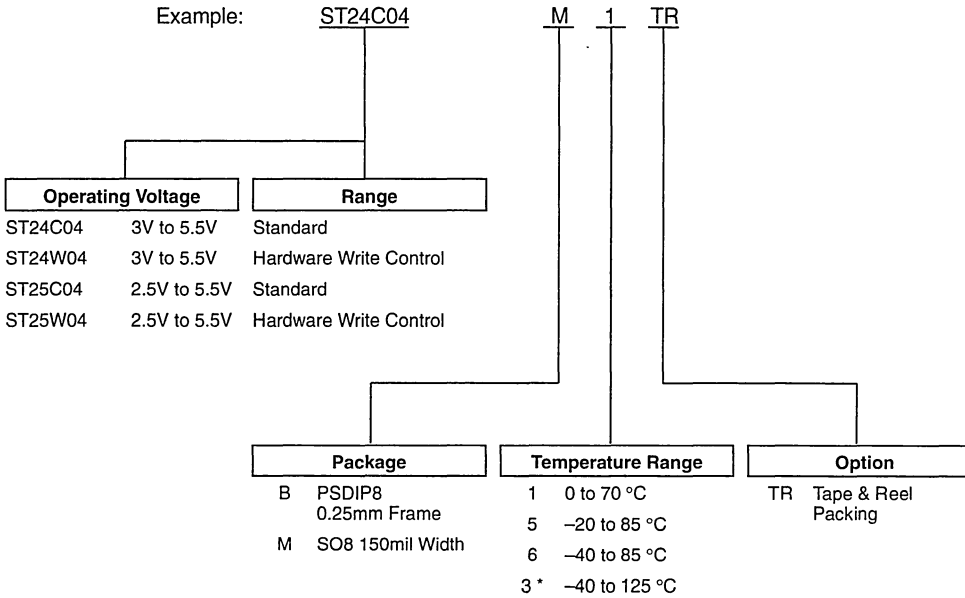
Acknowledge in Read Mode. In all read modes the ST24/25x04 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25x04 terminate the data transfer and switches to a standby state.

Figure 11. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical.

ORDERING INFORMATION SCHEME



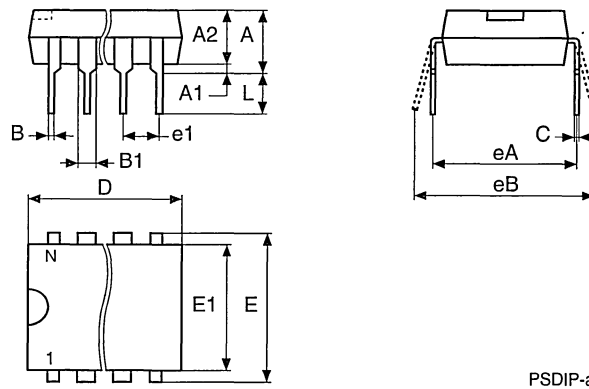
Notes: 3 * Temperature range on special request only

Parts are shipped with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Range, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB		–	10.00		–	0.394
L		3.00	3.80		0.118	0.150
N	8			8		

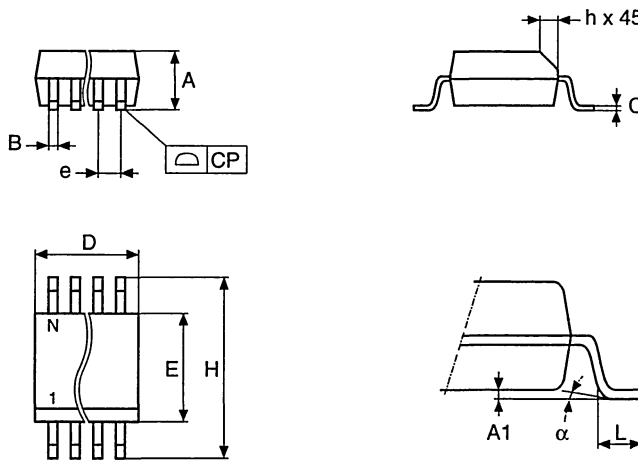


PSDIP-a

Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004



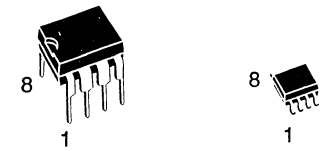
SO-a

Drawing is not to scale

ST24C08, ST25C08
ST24W08, ST25W08

8 Kbit Serial I^2C Bus EEPROM with User-Defined Block Write Protection

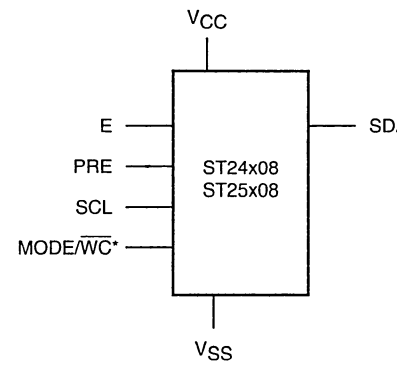
- 1 MILLION ERASE/WRITE CYCLES with 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24x08 versions
  - 2.5V to 5.5V for ST25x08 versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W08 and ST25W08
- PROGRAMMABLE WRITE PROTECTION
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 8 BYTES)
- PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES



PSDIP8 (B)
0.25mm Frame

SO8 (M)
150mil Width

Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W08 products

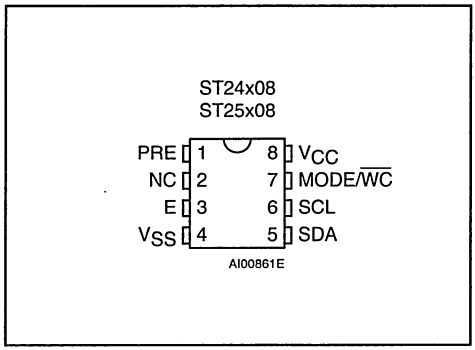
DESCRIPTION

This specification covers a range of 8 Kbits I^2C bus EEPROM products, the ST24/25C08 and the ST24/25W08. In the text, products are referred to as ST24/25x08, where "x" is: "C" for Standard version and "W" for Hardware Write Control version.

Table 1. Signal Names

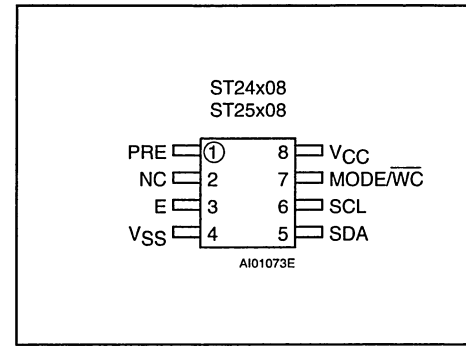
PRE	Write Protect Enable
E	Chip Enable Input
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections



Warning: NC = Not Connected.

Figure 2B. SO Pin Connections



Warning: NC = Not Connected.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		–40 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V_{IO}	Input or Output Voltages		–0.6 to 6.5	V
V_{CC}	Supply Voltage		–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The ST24/25x08 are 8 Kbit electrically erasable programmable memories (EEPROM), organized as 4 blocks of 256 x8 bits. They are manufactured in STMicroelectronics's Hi-Endurance Advanced CMOS technology which guarantees an endurance of one million erase/write cycles with a data retention of 40 years.

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. This is used together with 1 chip enable input (E) so that up to 2 x 8K devices may be attached to the I^2C bus and selected individually. The memories behave as a slave device in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code 1010), plus one read/write bit and terminated by an acknowledge bit.

Table 3. Device Select Code

	Device Code				Chip Enable	Block Select		$\overline{RW}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E	A9	A8	$R\overline{W}$

Note: The MSB b7 is sent first

Table 4. Operating Modes (1)

Mode	$\overline{RW}$ bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, $R\overline{W}$ = '1'
Random Address Read	'0'	X	1	START, Device Select, $R\overline{W}$ = '0', Address,
	'1'			reSTART, Device Select, $R\overline{W}$ = '1'
Sequential Read	'1'	X	1 to 1024	Similar to Current or Random Mode
Byte Write	'0'	X	1	START, Device Select, $R\overline{W}$ = '0'
Multibyte Write (2)	'0'	V_{IH}	8	START, Device Select, $R\overline{W}$ = '0'
Page Write	'0'	V_{IL}	16	START, Device Select, $R\overline{W}$ = '0'

Notes: 1. X = V_{IH} or V_{IL}
2. Multibyte Write not available in ST24/25W08 versions

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Chip Enable (E). This chip enable input is used to set one least significant bit (b3) of the device select byte code. This input may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Protect Enable (PRE). The PRE input pin, in addition to the status of the Block Address Pointer bit (b2, location 3FFh as in Figure 7), sets the PRE write protection active.

Mode (MODE). The MODE input is available on pin 7 (see also $\overline{WC}$ feature) and may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. When unconnected, the MODE input is internally read as a V_{IH} (Multibyte Write mode).

Write Control ($\overline{WC}$). An hardware Write Control ($\overline{WC}$) feature is offered only for ST24W08 and ST25W08 versions on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ = V_{IH}) or disable ($\overline{WC}$ = V_{IL}) the internal write protection. When unconnected, the $\overline{WC}$ input is internally read as V_{IL} and the memory area is not write protected.

SIGNAL DESCRIPTIONS (cont'd)

The devices with this Write Control feature no longer support the Multibyte Write mode of operation, however all other write modes are fully supported.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

DEVICE OPERATION

I²C Bus Background

The ST24/25x08 support the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25x08 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25x08 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25x08 and the bus master. A STOP condition at the end of a Read command, after and only after a No Acknowledge, forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25x08 sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24/25x08, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I²C Bus

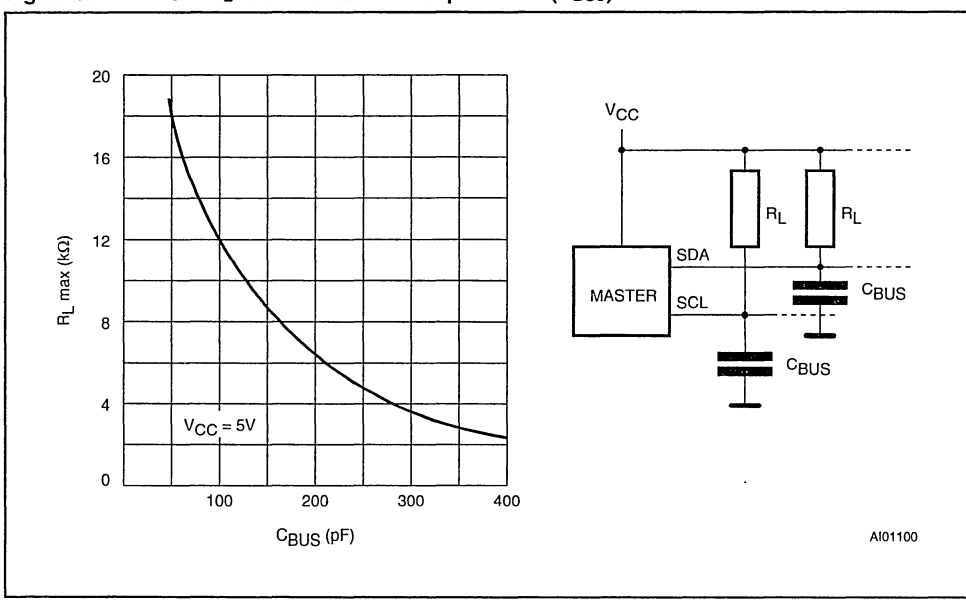


Table 5. Input Parameters (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance (ST24/25W08)	$V_{IN} \le 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance (ST24/25W08)	$V_{IN} \ge 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current (ST24 series)	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2.5V, f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby) (ST24 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 100kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E, PRE, MODE, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E, PRE, MODE, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage (ST24 series)	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V

Table 7. AC Characteristics
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C; V_{CC} = 3V to 5.5V or 2.5V to 5.5V)

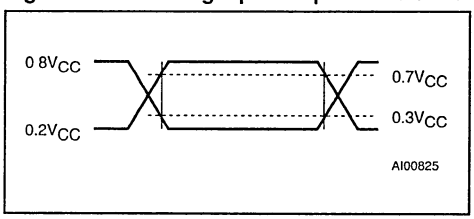
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD.STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU\cdot STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV} (2)	t_{AA}	Clock Low to Next Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Data Out Hold Time	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_W (3)	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. The minimum value delays the falling/rising edge of SDA away from SCL = 1 in order to avoid unwanted START and/or STOP conditions
3. In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (6 address MSB are not constant) the maximum programming time is doubled to 20ms

Table 8. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}
Input and Output Timing Ref. Voltages	0.3V_{CC} to 0.7V_{CC}

Figure 4. AC Testing Input Output Waveforms

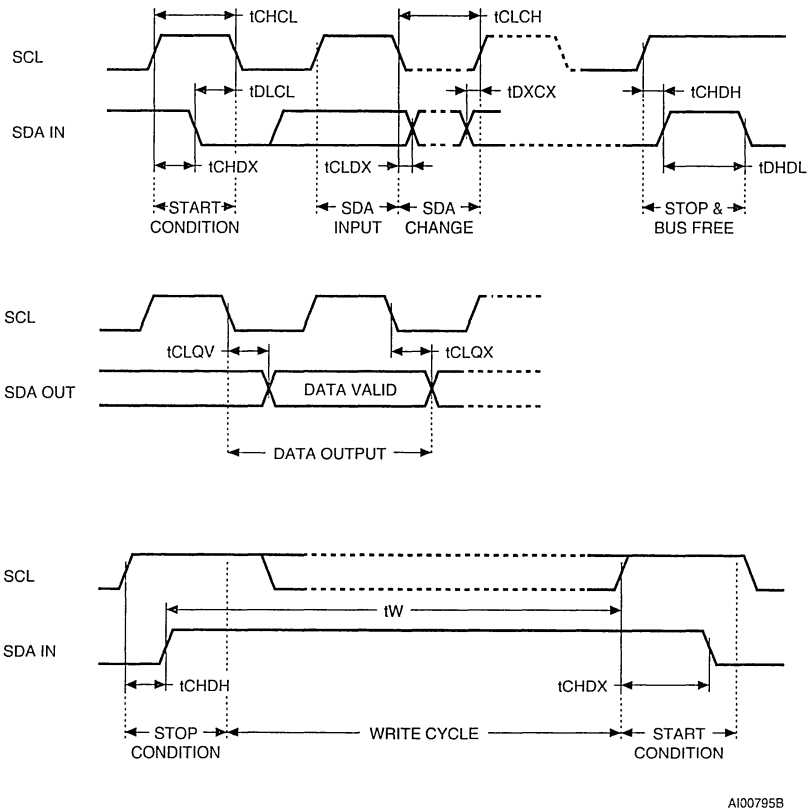


DEVICE OPERATION (cont'd)

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For these memories the 4 bits are fixed as 1010b. The following bit identifies the specific memory on the bus. It is matched to the chip enable signal E. Thus up to 2 x 8K memories can be connected on the same bus giving a memory capacity total of 16 Kbits. After a START condition any memory on the bus will identify the device code and compare the following bit to its chip enable input E.

The 6th and 7th bits sent, select the block number (one block = 256 bytes). The 8th bit sent is the read or write bit ($\overline{RW}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Figure 5. AC Waveforms



Write Operations

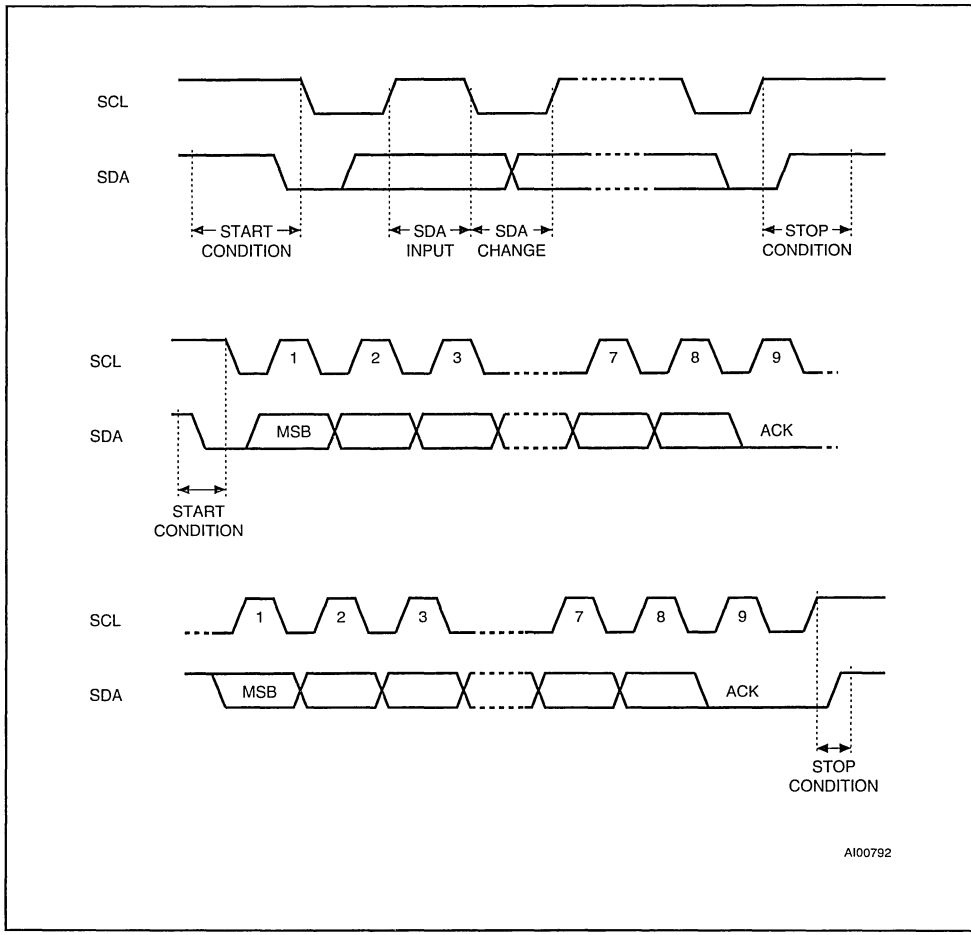
The Multibyte Write mode (only available on the ST24/25C08 versions) is selected when the MODE pin is at V_{IH} and the Page Write mode when MODE pin is at V_{IL}. The MODE pin may be driven dynamically with CMOS input levels.

Following a START condition the master sends a device select code with the $\overline{RW}$ bit reset to '0'. The memory acknowledges this and waits for a byte address. The byte address of 8 bits provides access to one block of 256 bytes of the memory. After receipt of the byte address the device again responds with an acknowledge.

For the ST24/25W08 versions, any write command with $\overline{WC}$ = 1 will not modify the memory content.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition. The Write mode is independant of the state of the MODE pin which could be left floating if only this mode was to be used. However it is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL}, to minimize the standby current.

Figure 6. I²C Bus Protocol



Multibyte Write. For the Multibyte Write mode, the MODE pin must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory. The transfer is terminated by the master generating a STOP condition. The duration of the write cycle is t_W = 10ms maximum except when bytes are accessed on 2 rows (that is have different values for the 5 most significant address bits A7-A3), the programming time is then doubled to a maximum of 20ms. Writing more than 8 bytes in the Multibyte Write mode may modify data bytes in an adjacent row (one row is 16 bytes long). However, the Multibyte Write can properly write up to 16 consecutive bytes only if the first address of these 16 bytes is the first address of the row, the 15 following bytes being written in the 15 following bytes of this same row.

Page Write. For the Page Write mode the MODE pin must be at V_{IL}. The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 4 most significant memory address bits (A7-A4) are the same inside one block. The master sends from one up to 16 bytes

of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (4 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master.

Figure 7. Memory Protection

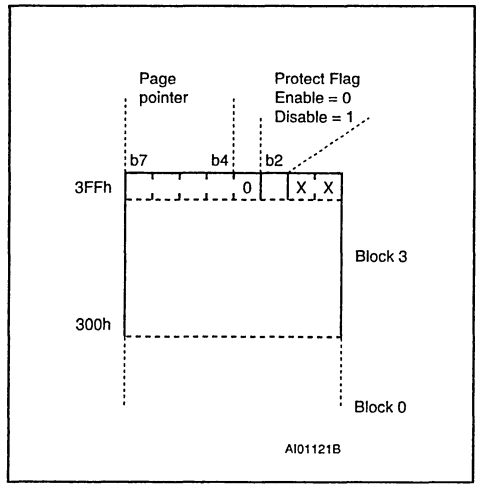


Figure 8. Write Cycle Polling using ACK

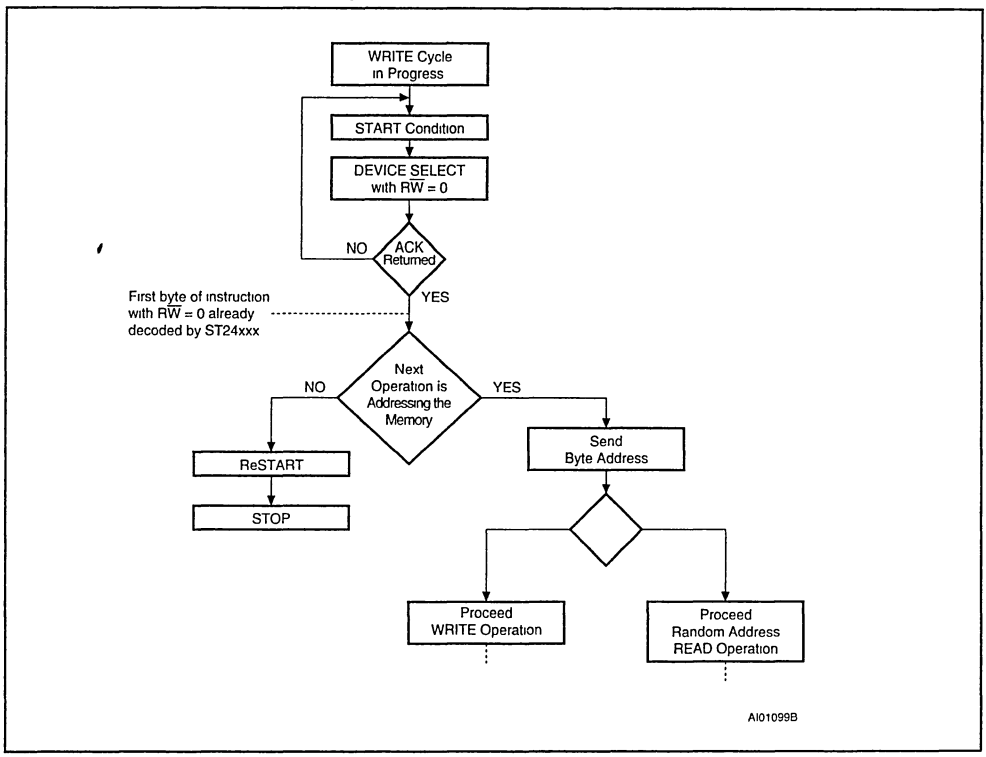
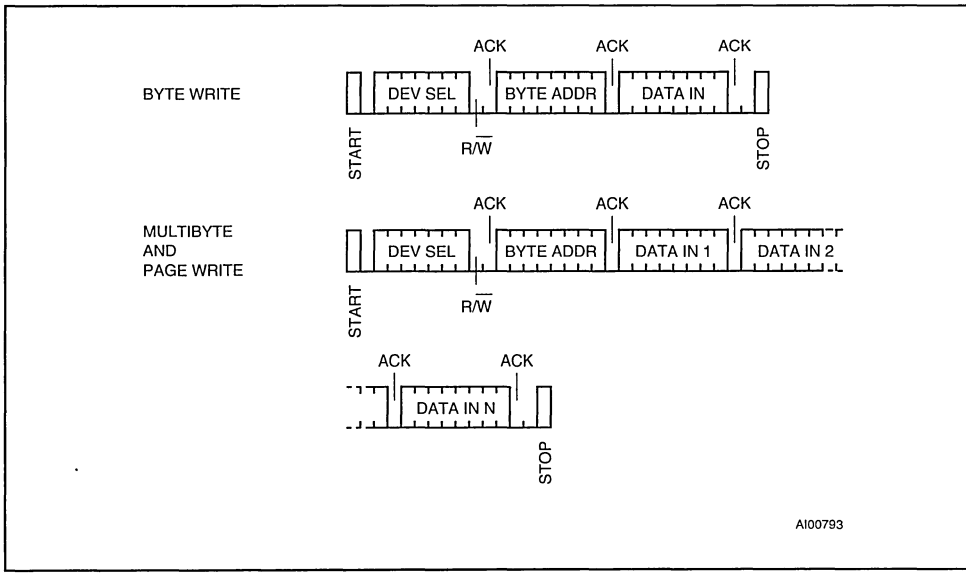


Figure 9. Write Modes Sequence (ST24/25C08)



DEVICE OPERATION (cont'd)

The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 8).
- Step 1: the Master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

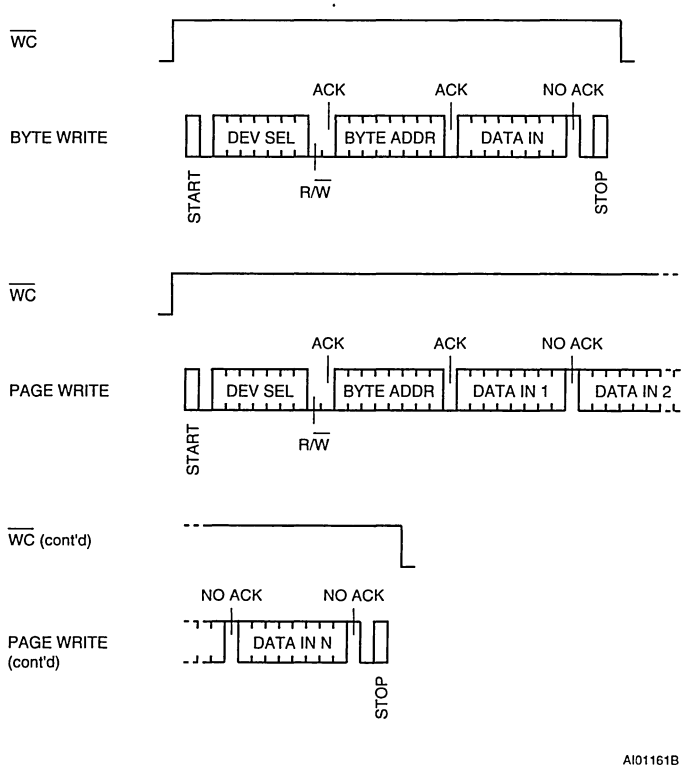
Write Protection. Data in the upper block of 256 bytes of the memory may be write protected. The memory is write protected between a boundary address and the top of memory (address 3FFh) when the PRE input pin is taken high and when the Protect Flag (bit b2 in location 3FFh) is set to '0'. The boundary address is user defined by writing it in the Block Address Pointer. The Block Address Pointer is an 8 bit EEPROM register located at the address 3FFh. It is composed by 4 MSBs Address Pointer, which defines the bottom boundary address, and 4 LSBs which must be programmed at '0'. This Address Pointer can therefore address a boundary in steps of 16 bytes. The sequence to use the Write Protected feature is:

- write the data to be protected into the top of the memory, up to, but not including, location 3FFh;
- set the protection by writing the correct bottom boundary address in the Address pointer (4 MSBs of location 3FFh) with the bit b2 (Protect flag) set to '0'.

Note that for a correct fonctionality of the memory, all the 4 LSBs of the Block Address Pointer must also be programmed at '0'. The area will now be protected when the PRE input pin is taken High. While the PRE input pin is read at '0' by the memory, the location 3FFh can be used as a normal EEPROM byte.

Caution: Special attention must be used when using the protect mode together with the Multibyte Write mode (MODE input pin High). If the Multibyte Write starts at the location right below the first byte of the Write Protected area, then the instruction will write over the first 7 bytes of the Write Protected area. The area protected is therefore smaller than the content defined in the location 3FFh, by 7 bytes. This does not apply to the Page Write mode as the address counter 'roll-over' and thus cannot go above the 16 bytes lower boundary of the protected area.

Figure 10. Write Modes Sequence with Write Control = 1 (ST24/25W08)



Read Operations

Read operations are independent of the state of the MODE pin. On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the R/W bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter (see Figure 11). This is followed by another START condition from the master and the byte address is repeated with the R/W bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master have to NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

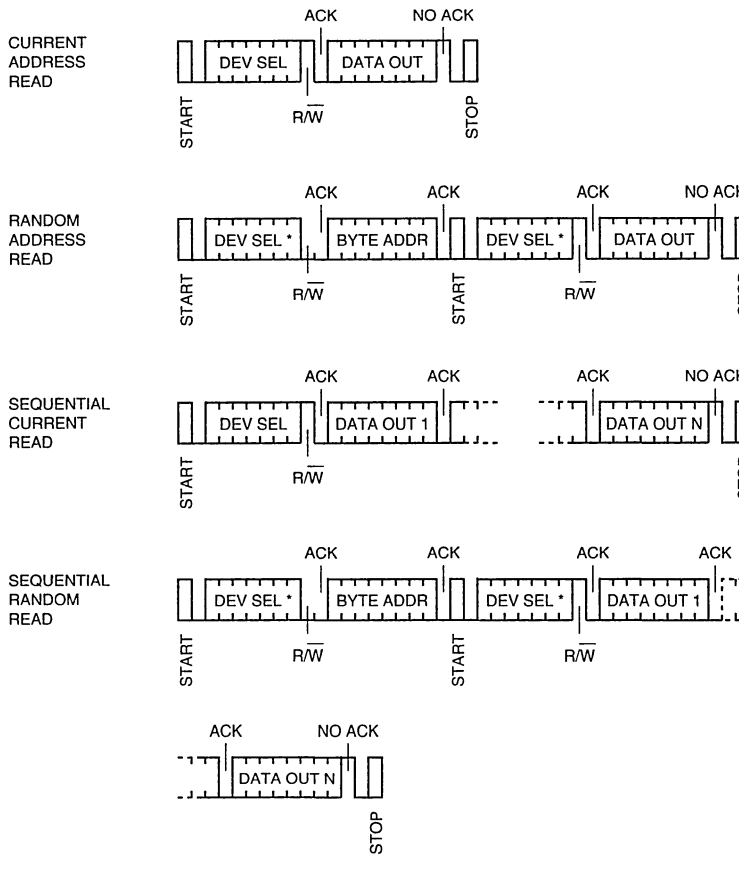
Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the

DEVICE OPERATION (cont'd)

master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

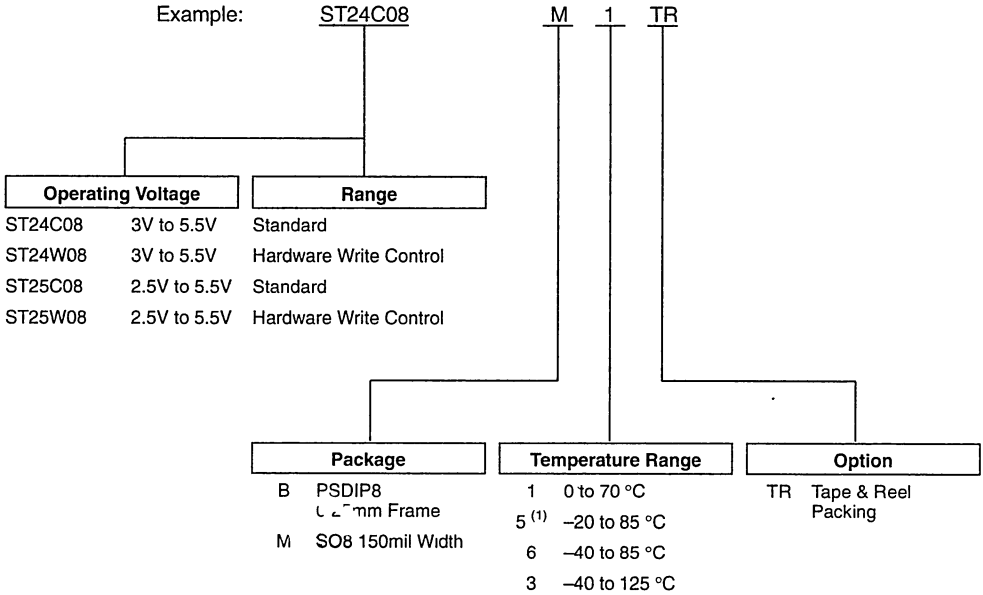
Acknowledge in Read Mode. In all read modes the ST24/25x08 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25x08 terminate the data transfer and switches to a standby state.

Figure 11. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical.

ORDERING INFORMATION SCHEME



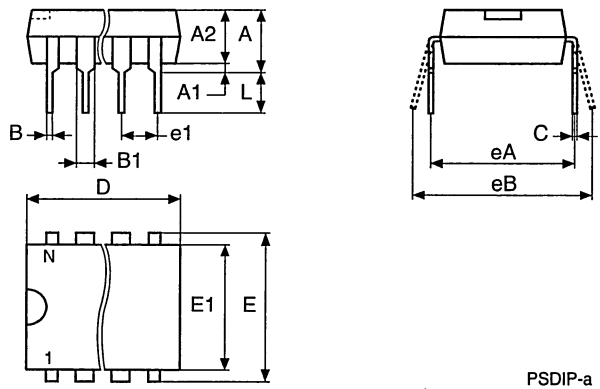
Notes: 1. Temperature range on special request only.

Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you. to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB		–	10.00		–	0.394
L		3.00	3.80		0.118	0.150
N	8			8		

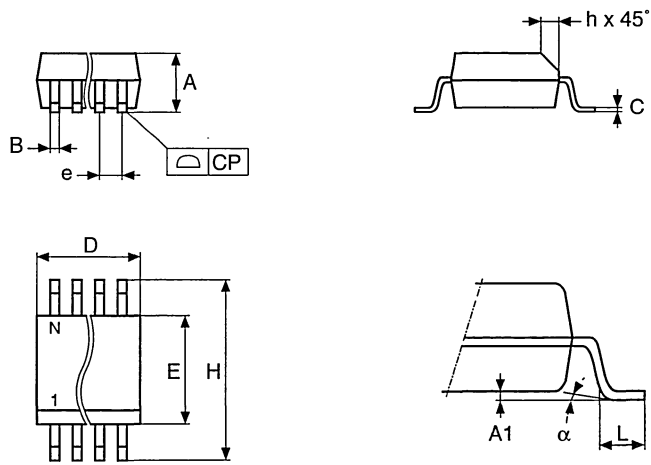


PSDIP-a

Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N		8			8	
CP			0.10			0.004



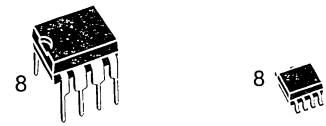
SO-a

Drawing is not to scale

ST24C16, ST25C16
ST24W16, ST25W16

16 Kbit Serial I^2C Bus EEPROM with User-Defined Block Write Protection

- 1 MILLION ERASE/WRITE CYCLES, with 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for ST24x16 versions
  - 2.5V to 5.5V for ST25x16 versions
- HARDWARE WRITE CONTROL VERSIONS: ST24W16 and ST25W16
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 8 BYTES) for the ST24C16
- PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES



PSDIP8 (B)
0.25mm Frame

SO8 (M)
150mil Width

DESCRIPTION

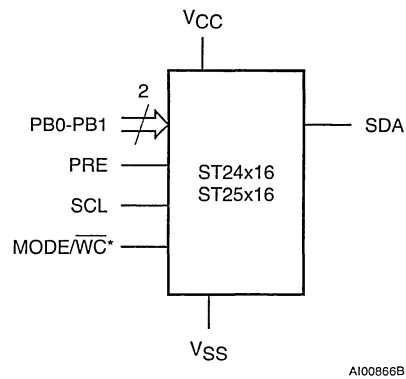
This specification covers a range of 16 Kbit I^2C bus EEPROM products, the ST24/25C16 and the ST24/25W16. In the text, products are referred to as ST24/25x16 where "x" is: "C" for Standard version and "W" for hardware Write Control version.

The ST24/25x16 are 16 Kbit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 256 x8 bits. These are manufactured in STMicroelectronics's Hi-Endurance Advanced CMOS technology which guarantees an endur-

Table 1. Signal Names

PRE	Write Protect Enable
PB0, PB1	Protect Block Select
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multybyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W16 products.

Figure 2A. DIP Pin Connections

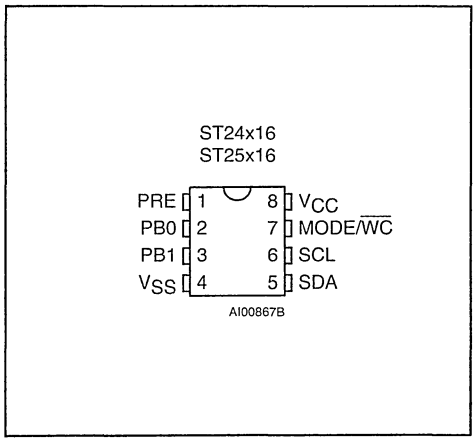


Figure 2B. SO8 Pin Connections

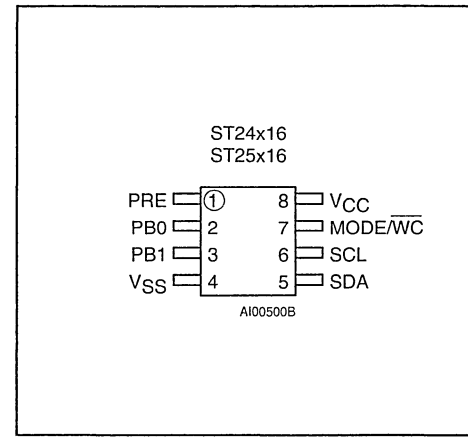


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			–40 to 125	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8) (PSDIP8)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.6 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. 100pF through 1500Ω, MIL-STD-883C, 3015.7
3. 200pF through 0Ω, EIAJ IC-121 (condition C)

DESCRIPTION (cont'd)

ance of one million erase/write cycles with a data retention of 40 years. The ST25x16 operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The memories behave as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 block select bits, plus one read/write bit and terminated by an acknowledge bit. When writing data to the

Table 3. Device Select Code

	Device Code				Memory MSB Addresses			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	A10	A9	A8	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes

Mode	RW bit	MODE pin	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, RW = '1'
Random Address Read	'0'	X	1	START, Device Select, RW = '0', Address,
	'1'			reSTART, Device Select, RW = '1'
Sequential Read	'1'	X	1 to 2048	As CURRENT or RANDOM Mode
Byte Write	'0'	X	1	START, Device Select, RW = '0'
Multibyte Write	'0'	V_{IH}	8	START, Device Select, RW = '0'
Page Write	'0'	V_{IL}	16	START, Device Select, RW = '0'

Note: X = V_{IH} or V_{IL}.

memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Data in the 4 upper blocks of the memory may be write protected. The protected area is programmable to start on any 16 byte boundary. The block in which the protection starts is selected by the input pins PB0, PB1. Protection is enabled by setting a Protect Flag bit when the PRE input pin is driven High.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Untill the V_{CC} voltage has reached the POR threshold value, the internal reset is active: all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNALS DESCRIPTION

Serial Clock (SCL). The SCL input signal is used to synchronise all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA signal is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Protected Block Select (PB0, PB1). PB0 and PB1 input signals select the block in the upper part of the memory where write protection starts. These inputs have a CMOS compatible input level.

Protect Enable (PRE). The PRE input signal, in addition to the status of the Block Address Pointer bit (b2, location 7FFh as in Figure 7), sets the PRE write protection active.

Mode (MODE). The MODE input is available on pin 7 (see also $\overline{WC}$ feature) and may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. When unconnected, the MODE input is internally read as V_{IH} (Multibyte Write mode).

Write Control ($\overline{WC}$). An hardware Write Control feature is offered only for ST24W16 and ST25W16 versions on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ at V_{IH}) or disable ($\overline{WC}$ at V_{IL}) the internal write protection. When unconnected, the $\overline{WC}$ input is internally read as V_{IL}. The devices with this Write Control feature no longer supports the Multibyte Write mode of operation, however all other write modes are fully supported.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus

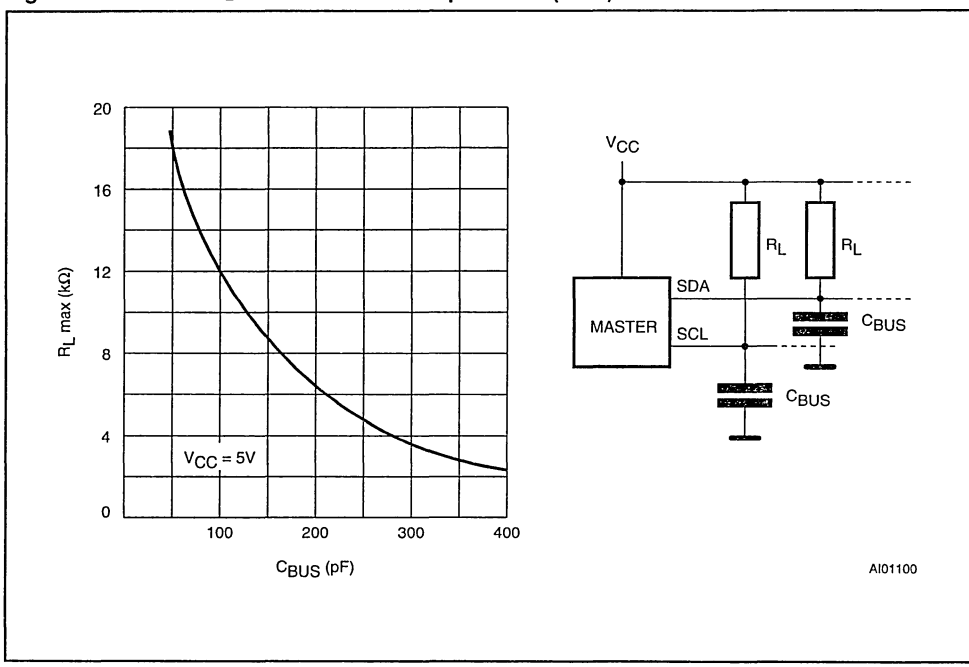


Table 5. Input Parameters (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance (ST24/25W16)	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance (ST24/25W16)	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current (ST24 series)	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2.5V, f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby) (ST24 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 100kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (PB0 - PB1, PRE, MODE, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (PB0 - PB1, PRE, MODE, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage (ST24 series)	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V

Table 7. AC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

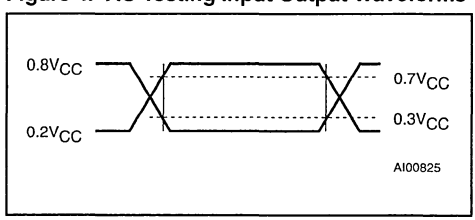
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU\ STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU\ DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV} (2)	t_{AA}	Clock Low to Next Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Data Out Hold Time	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_W (3)	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. The minimum value delays the falling/rising edge of SDA away from SCL = 1 in order to avoid unwanted START and/or STOP conditions.
3 In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (5 address MSB are not constant) the maximum programming time is doubled to 20ms

Table 8. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}
Input and Output Timing Ref. Voltages	0.3V_{CC} to 0.7V_{CC}

Figure 4. AC Testing Input Output Waveforms



DEVICE OPERATION

I²C Bus Background

The ST24/25x16 support the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25x16 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25x16 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Figure 5. AC Waveforms

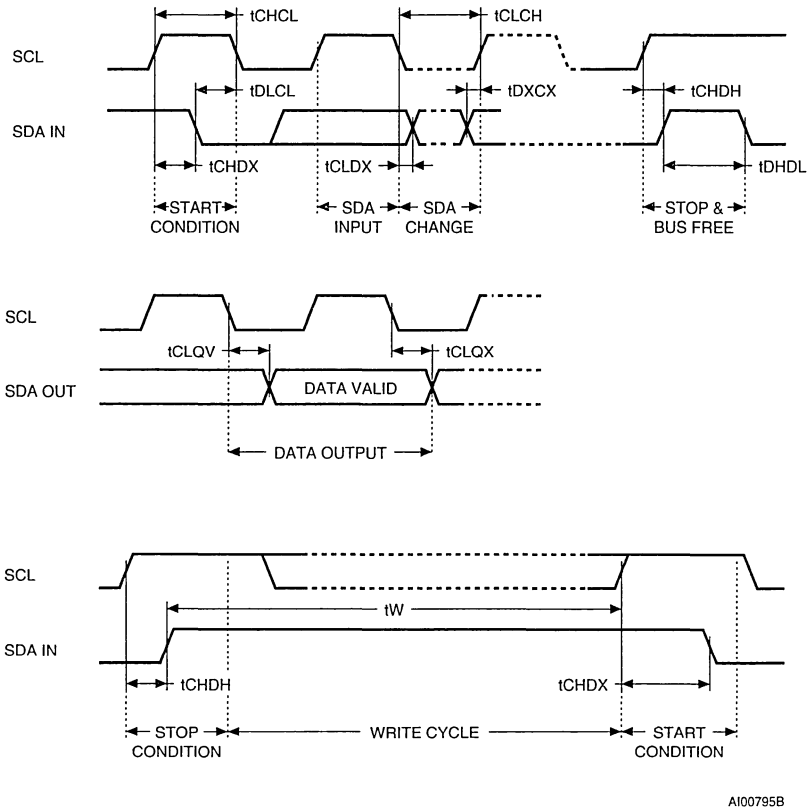
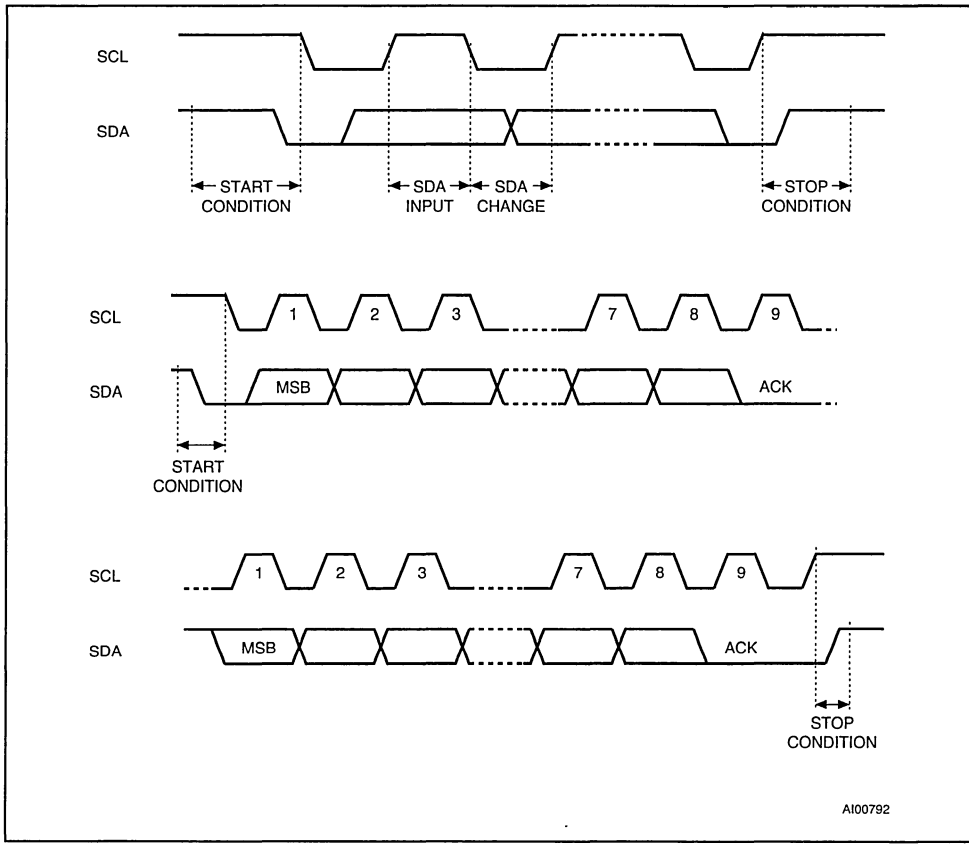


Figure 6. I²C Bus Protocol



Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25x16 and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

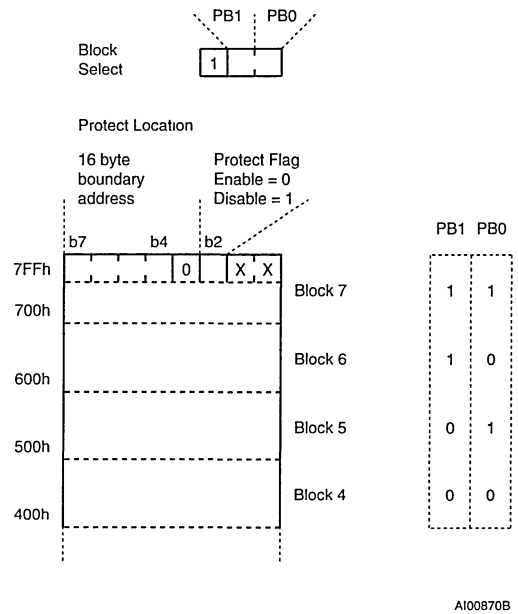
Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25x16 samples the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24/25x16, the master must initiate a START condition. The 8 bits sent after a START condition are made up of a device select of 4 bits that identifie the device type (1010), 3 Block select bits and one bit for a READ ($R\overline{W}$ = 1) or WRITE ($R\overline{W}$ = 0) operation.

There are three modes both for read and write. They are summarised in Table 4 and described hereafter. A communication between the master and the slave is ended with a STOP condition.

Figure 7. Memory Protection



Write Operations

The Multibyte Write mode (only available on the ST24/25C16 versions) is selected when the MODE pin is at V_{IH} and the Page Write mode when MODE pin is at V_{IL}. The MODE pin may be driven dynamically with CMOS input levels.

Following a START condition the master sends a device select code with the $\overline{RW}$ bit reset to '0'. The memory acknowledges this and waits for a byte address. The byte address of 8 bits provides access to any of the 256 bytes of one memory block. After receipt of the byte address the device again responds with an acknowledge.

For the ST24/25W16 versions, any write command with $\overline{WC}$ = '1' (during a period of time from the START condition untill the end of the Byte Address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 10.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition. The Write mode is independant of the state of the MODE pin which could be left floating if only this mode was to be used. However it is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL}, to minimize the stand-by current.

Multibyte Write (ST24/25C16 only). For the Multibyte Write mode, the MODE pin must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory. The transfer is terminated by the master generating a STOP condition. The duration of the write cycle is t_W = 10ms maximum except when bytes are accessed on 2 contiguous rows (one row is 16 bytes), the programming time is then doubled to a maximum of 20ms. Writing more than 8 bytes in the Multibyte Write mode may modify data bytes in an adjacent row (one row is 16 bytes long). However, the Multibyte Write can properly write up to 16 consecutive bytes only if the first address of these 16 bytes is the first address of the row, the 15 following bytes being written in the 15 following bytes of this same row.

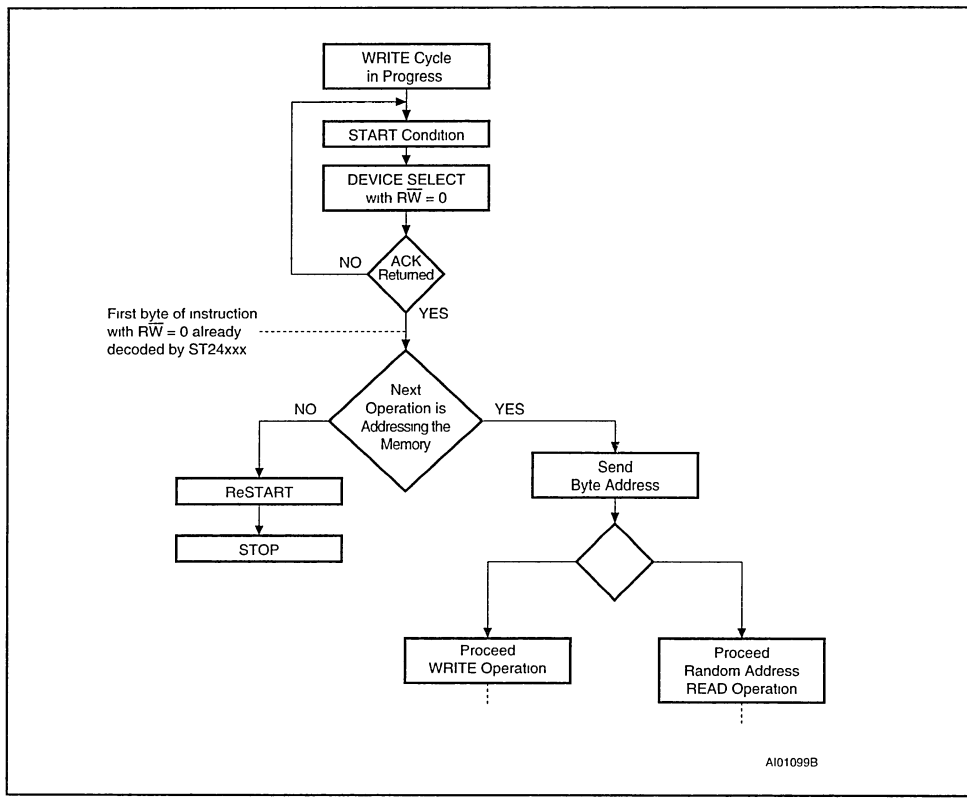
Page Write. For the Page Write mode, the MODE pin must be at V_{IL}. The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the same Block Address bits (b3, b2, b1 of Device Select code in Table 3) and the same 4 MSBs in the Byte Address. The master sends one up to 16 bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (4 Least Significant Bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delay by Polling On ACK. During the internal Write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the Write time (t_W) is given in the AC Characteristics table, this timing value may be reduced by an ACK polling sequence issued by the master.

The sequence is:

- Initial condition: a Write is in progress (see Figure 8).
- Step 1: the Master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
- Step 2: if the memory is internally writing, no ACK will be returned. The Master goes back to Step1. If the memory has terminated the internal writing, it will issue an ACK indicating that the memory is ready to receive the second part of the instruction (the first byte of this instruction was already sent during Step 1).

Figure 8. Write Cycle Polling using ACK



Write Protection. Data in the upper four blocks of 256 bytes of the memory may be write protected. The memory is write protected between a boundary address and the top of memory (address 7FFh).The boundary address is user defined by writing it in the Block Address Pointer (location 7FFh).

The Block Address Pointer is an 8 bit EEPROM register located at the address 7FFh. It is composed by 4 MSBs Address Pointer, which defines the bottom boundary address, and 4 LSBs which must be programmed at '0'. This Address Pointer can therefore address a boundary by page of 16 bytes.

The block in which the Block Address Pointer defines the boundary of the write protected memory is defined by the logic level applied on the PB1 and PB0 input pins:

- PB1 ='0'and PB0 ='0' select block 4
- PB1 ='0'and PB0 ='1' select block 5
- PB1 ='1'and PB0 ='0' select block 6
- PB1 ='1'and PB0 ='1' select block 7

The following sequence should be used to set the Write Protection:

- write the data to be protected into the top of the memory, up to, but not including, location 7FFh;
- select the block by hardwiring the signals PB0 & PB1;
- set the protection by writing the correct bottom boundary address in the Address Pointer (4 MSBs of location 7FFh) with bit b2 (Protect Flag) set to '0'.

Note that for a correct fonctionality of the memory, all the 4 LSBs of the Block Address Pointer must also be programmed at '0'. The area will be protected when the PRE input is taken High.

Remark: The Write Protection is active if and only if the PRE input pin is driven High and the bit 2 of location 7FFh is set to '0'. In all the other cases, the memory Block will not be protected. While the PRE input pin is read at '0' by the memory, the location 7FFh can be used as a normal EEPROM byte.

Caution: Special attention must be used when using the protect mode together with the Multibyte Write mode (MODE input pin High). If the Multibyte Write starts at the location right below the first byte of the Write Protected area, then the instruction will write over the first 7 bytes of the Write Protected area. The area protected is therefore smaller than the content defined in the location 7FFh, by 7 bytes. This does not apply to the Page Write mode as the address counter 'roll-over' and thus cannot go above the 16 bytes lower boundary of the protected area.

Figure 9. Write Modes Sequence (ST24/25C16)

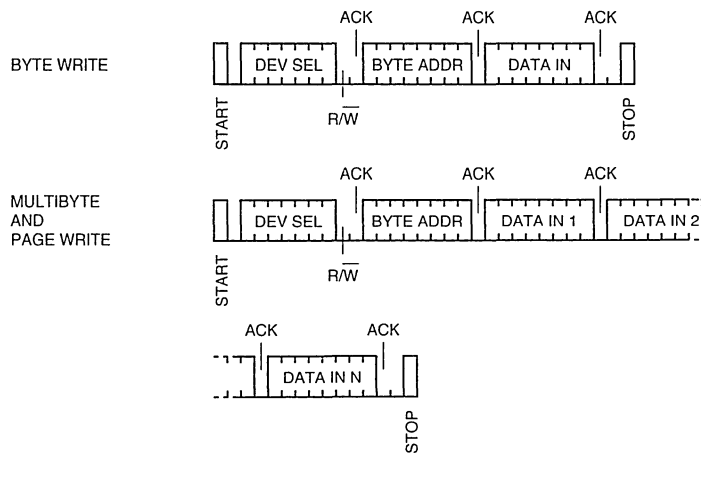
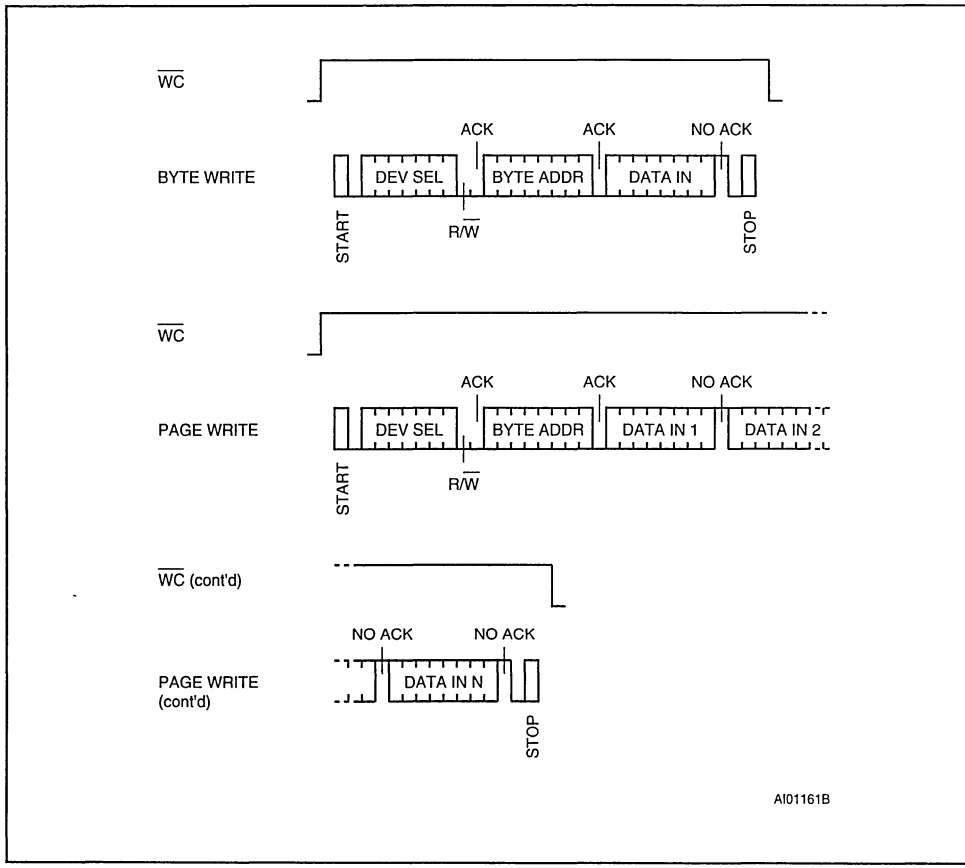


Figure 10. Write Modes Sequence with Write Control = 1 (ST24/25W16)



Read Operation

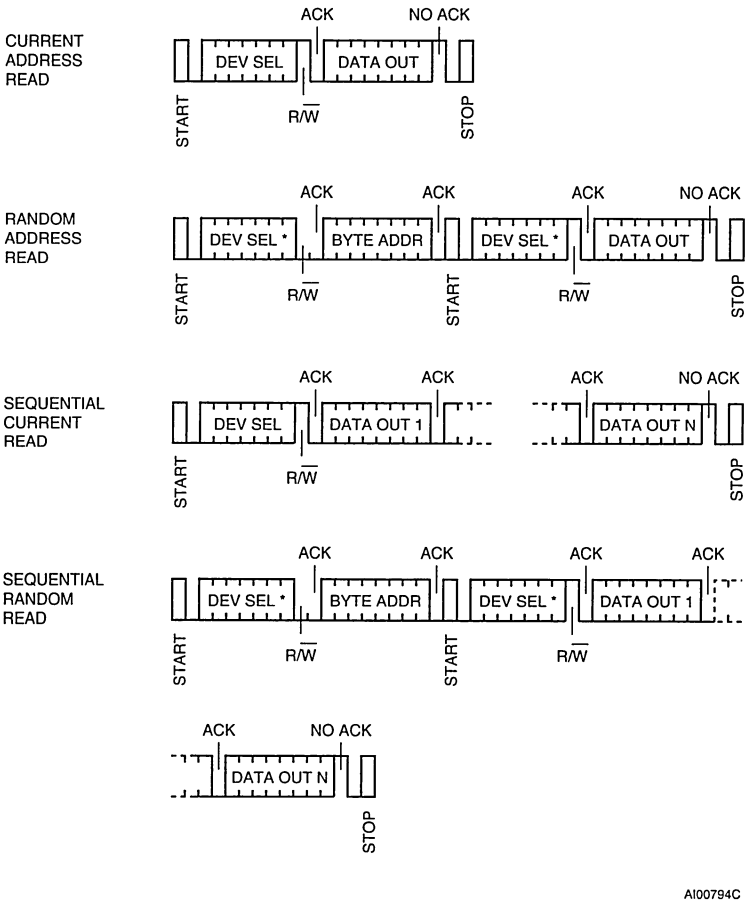
Read operations are independent of the state of the MODE signal. On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the R/W bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter (see Figure 11). This is followed by another START condition from the master and the byte address repeated with the R/W bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte out-

Figure 11. Read Modes Sequence

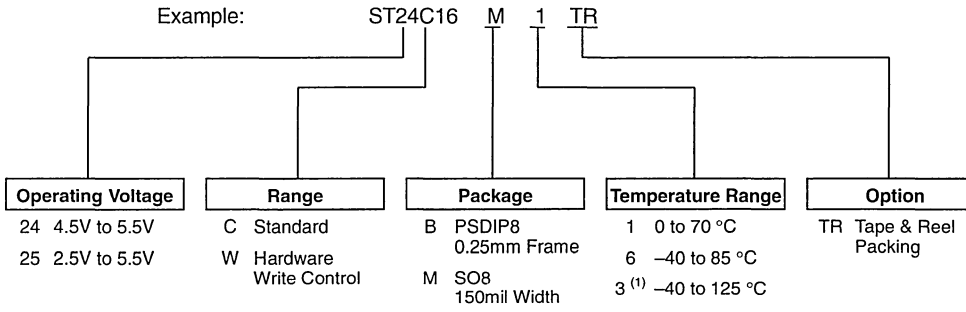


Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical.

put, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll- over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST24/25x16 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25x16 terminate the data transfer and switches to a standby state.

ORDERING INFORMATION SCHEME



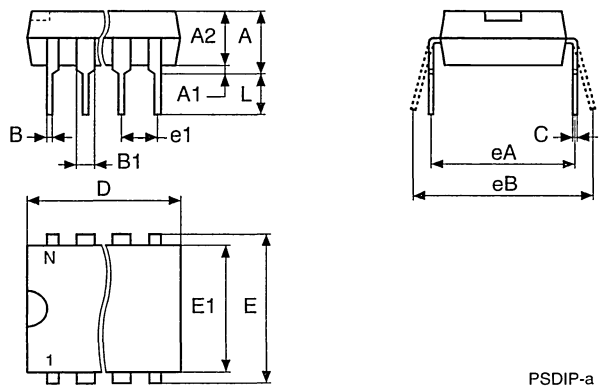
Note: 1. Temperature range on special request only.

Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB		–	10.00		–	0.394
L		3.00	3.80		0.118	0.150
N	8			8		

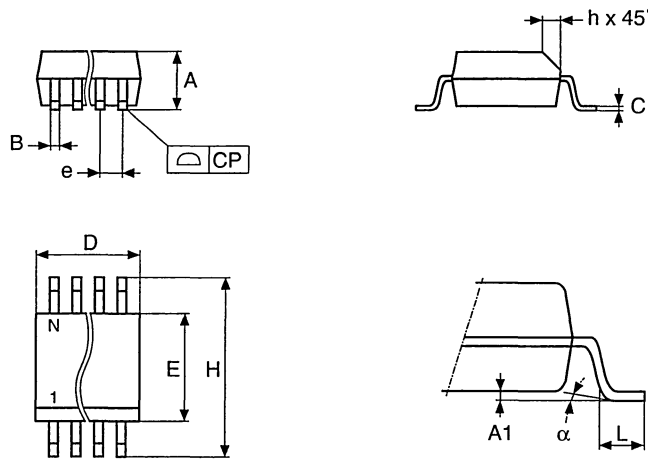


PSDIP-a

Drawing is not to scale.

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004



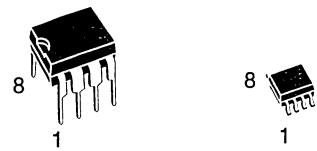
SO-a

Drawing is not to scale.

ST24E16
ST25E16

16 Kbit Serial I^2C EEPROM with Extended Addressing

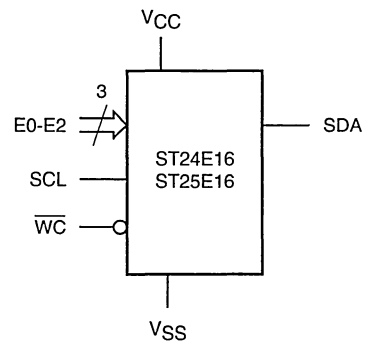
- COMPATIBLE with I^2C EXTENDED ADDRESSING
- TWO WIRE SERIAL INTERFACE, SUPPORTS 400kHz PROTOCOL
- 1 MILLION ERASE/WRITE CYCLES, OVER the FULL SUPPLY VOLTAGE RANGE
- 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  - 4.5V to 5.5V for ST24E16 version
  - 2.5V to 5.5V for ST25E16 version
- WRITE CONTROL FEATURE
- BYTE and PAGE WRITE (up to 16 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES



PSDIP8 (B)
0.25mm Frame

SO8 (M)
150mil Width

Figure 1. Logic Diagram



DESCRIPTION

The ST24/25E16 are 16 Kbit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 256 x8 bits. It is manufactured in STMicroelectronics's Hi-Endurance Advanced CMOS technology which guarantees an endurance of one million erase/write cycles over the full supply voltage range, and a data retention of over 40 years. The ST25E16 operates with a power supply value as low as 2.5V.

Table 1. Signal Names

E0 - E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections

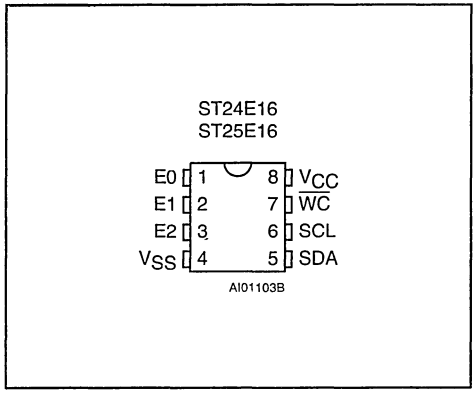


Figure 2B. SO Pin Connections

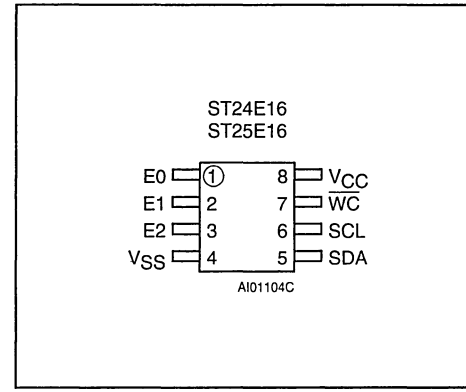


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			–40 to 125	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8) (PSDIP8)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.6 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability Refer also to the STMicroelectronics SURE Program and other relevant quality documents
2. 100pF through 1500Ω, MIL-STD-883C, 3015 7
3 200pF through 0Ω; EIAJ IC-121 (condition C)

DESCRIPTION (cont'd)

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

Each memory is compatible with the I^2C extended addressing standard, two wire serial interface which uses a bi-directional data bus and serial clock. The ST24/25E16 carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. The ST24/25E16 behave as slave devices in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 bit Chip Enable input to form a 7 bit Device Select, plus one read/write bit and terminated by an acknowledge bit.

Table 3. Device Select Code

	Device Code				Chip Enable			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	RW

Note: The MSB b7 is sent first

Table 4. Operating Modes

Mode	RW bit	Bytes	Initial Sequence
Current Address Read	'1'	1	START, Device Select, RW = '1'
Random Address Read	'0'	1	START, Device Select, RW = '0', Address,
	'1'		reSTART, Device Select, RW = '1'
Sequential Read	'1'	1 to 2048	As CURRENT or RANDOM Mode
Byte Write	'0'	1	START, Device Select, RW = '0'
Page Write	'0'	16	START, Device Select, RW = '0'

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way.

Data transfers are terminated with a STOP condition. In this way, up to 8 ST24/25E16 may be connected to the same I^2C bus and selected individually, allowing a total addressing field of 128 Kbit.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Untill the V_{CC} voltage has reached the POR threshold value, the internal reset is active: all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNALS DESCRIPTION

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3)

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

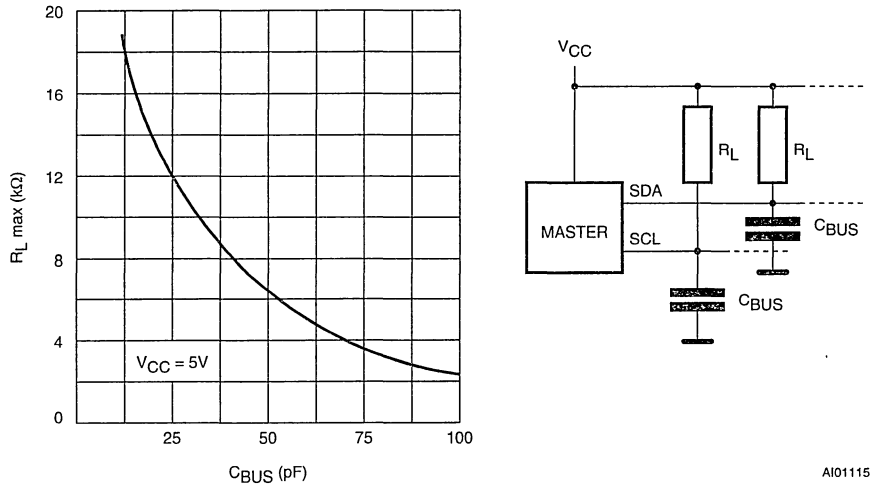
Chip Enable (E0 - E2). These chip enable inputs are used to set the 3 least significant bits of the 7 bit device select code. They may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code. Note that the V_{IL} and V_{IH} levels for the inputs are CMOS, not TTL compatible.

Write Control ($\overline{WC}$). The Write Control feature $\overline{WC}$ is useful to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ at V_{IH}) or disable ($\overline{WC}$ at V_{IL}) the internal write protection. The devices with this Write Control feature no longer supports the multibyte mode of operation. When unconnected, the $\overline{WC}$ input is internally read as V_{IL} (see Table 5).

When $\overline{WC}$ = '1', Device Select and Address bytes are acknowledged; Data bytes are not acnowledged.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus, f_C = 400kHz



DEVICE OPERATION

I^2C Bus Background

The ST24/25E16 support the extended addressing I^2C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver.The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25E16 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25E16 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25E16 and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25E16 sample the SDA bus signal on the rising edge of the clock SCL. For correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Device Selection. To start communication between the bus master and the slave ST24/25E16, the master must initiate a START condition. The 8 bits sent after a START condition are made up of a device select of 4 bits that identifies the device type, 3 Chip Enable bits and one bit for a READ ($R\overline{W}$ = 1) or WRITE ($R\overline{W}$ = 0) operation. There are two modes both for read and write. These are summarised in Table 4 and described hereafter. A communication between the master and the slave is ended with a STOP condition.

Table 5. Input Parameters [1] (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	$V_{IN} \leq 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	$V_{IN} \geq 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70 ° or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current (SCL, SDA, E0-E2)	$0V \leq V_{IN} \leq V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current (ST24 series)	f_C = 400kHz (Rise/Fall time < 30ns)		2	mA
	Supply Current (ST25 series)			1	mA
I_{CC1}	Supply Current (Standby) (ST24 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 400kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 400kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0-E2, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0-E2, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage (ST24 series)	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V

Table 7. AC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.5V to 5.5V)

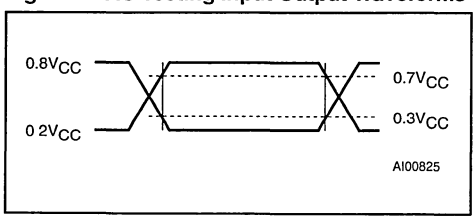
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2} (1)	t_R	SDA Rise Time	20	300	ns
t_{DL1DL1} (1)	t_F	SDA Fall Time	20	300	ns
t_{CHDX} (2)	$t_{SU\ STA}$	Clock High to Input Transition	600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		ns
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	600		ns
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		µs
t_{DXCX}	$t_{SU.DAT}$	Input Transition to Clock Transition	100		ns
t_{CHDH}	$t_{SU.STO}$	Clock High to Input High (STOP)	600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		µs
t_{CLQV} (3)	t_{AA}	Clock Low to Next Data Out Valid	200	1000	ns
t_{CLQX}	t_{DH}	Data Out Hold Time	200		ns
f_C	f_{SCL}	Clock Frequency		400	kHz
t_W	t_{WR}	Write Time		10	ms

Notes: 1. Sampled only, not 100% tested.
2. For a reSTART condition, or following a write cycle
3. The minimum value delays the falling/rising edge of SDA away from SCL = 1 in order to avoid unwanted START and/or STOP conditions.

Table 8. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}
Input and Output Timing Ref. Voltages	0.3V_{CC} to 0.7V_{CC}

Figure 4. AC Testing Input Output Waveforms



DEVICE OPERATION (cont'd)

Memory Addressing. A data byte in the memory is addressed through 2 bytes of address information. The Most Significant Byte is sent first and the Least significant Byte is sent after. The Least Significant Byte addresses a block of 256 bytes, bits b10,b9,b8 of the Most Significant Byte select one block among 8 blocks (one block is 256 bytes).

Most Significant Byte

X	X	X	X	X	b10	b9	b8

X = Don't Care.

Least Significant Byte

b7	b6	b5	b4	b3	b2	b1	b0

Figure 5. AC Waveforms

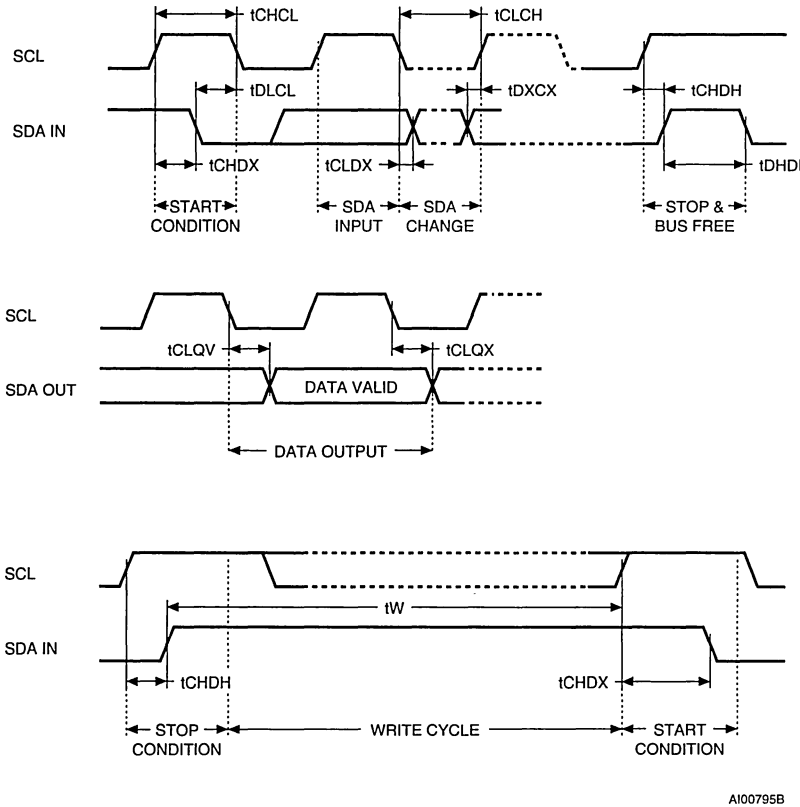
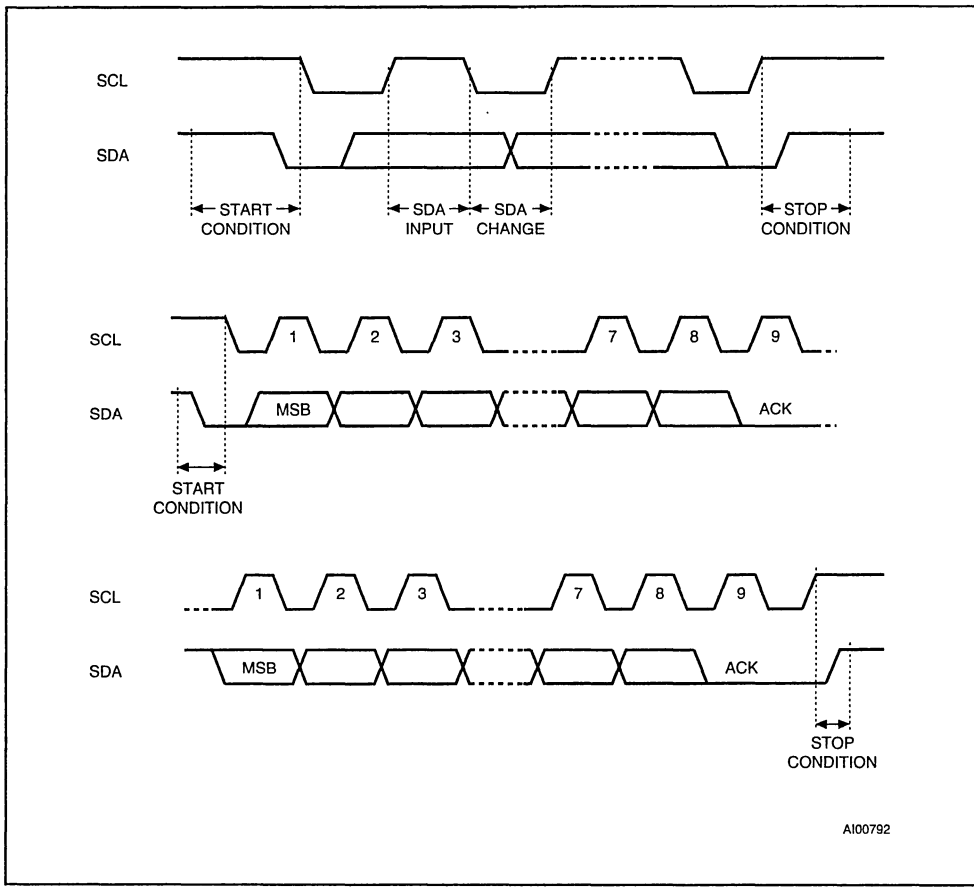


Figure 6. I²C Bus Protocol



Write Operations

Following a START condition the master sends a device select code with the R$\overline{W}$ bit reset to '0'. The ST24/25E16 acknowledge this and waits for 2 bytes of address. These 2 address bytes (8 bits each) provide access to any of the 8 blocks of 256 bytes each. Writing in the ST24/25E16 may be inhibited if input pin $\overline{WC}$ is taken high.

For the ST24/25E16 versions, any write command with $\overline{WC}$ = '1' (during a period of time from the START condition untill the end of the 2 Bytes Address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 9.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the ST24/25E16. The master then terminates the transfer by generating a STOP condition.

Page Write. The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same row of 16 bytes in the memory, that is the same Address bits (b10-b4). The master sends one up to 16 bytes of data, which are each acknowledged by the ST24/25E16. After each byte is transfered, the internal byte address counter (4 Least Significant Bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which

could result in data being overwritten. Note that for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the ST24/25E16 will not respond to any request.

Minimizing System Delay by Polling On ACK. During the internal Write cycle, the ST24/25E16 disable itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the Write time (t_W) is given in the AC Characteristics table, this timing value may be reduced by an ACK polling sequence issued by the master.

The sequence is:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the Master issues a START condition followed by a Device Select byte. (1st byte of the new instruction)
- Step 2: if the ST24/25E16 are internally writing, no ACK will be returned. The Master goes back to Step1. If the ST24/25E16 have terminated the internal writing, it will issue an ACK. The ST24/25E16 are ready to receive the second part of the instruction (the first byte of this instruction was already sent during Step1).

Figure 7. Write Cycle Polling using ACK

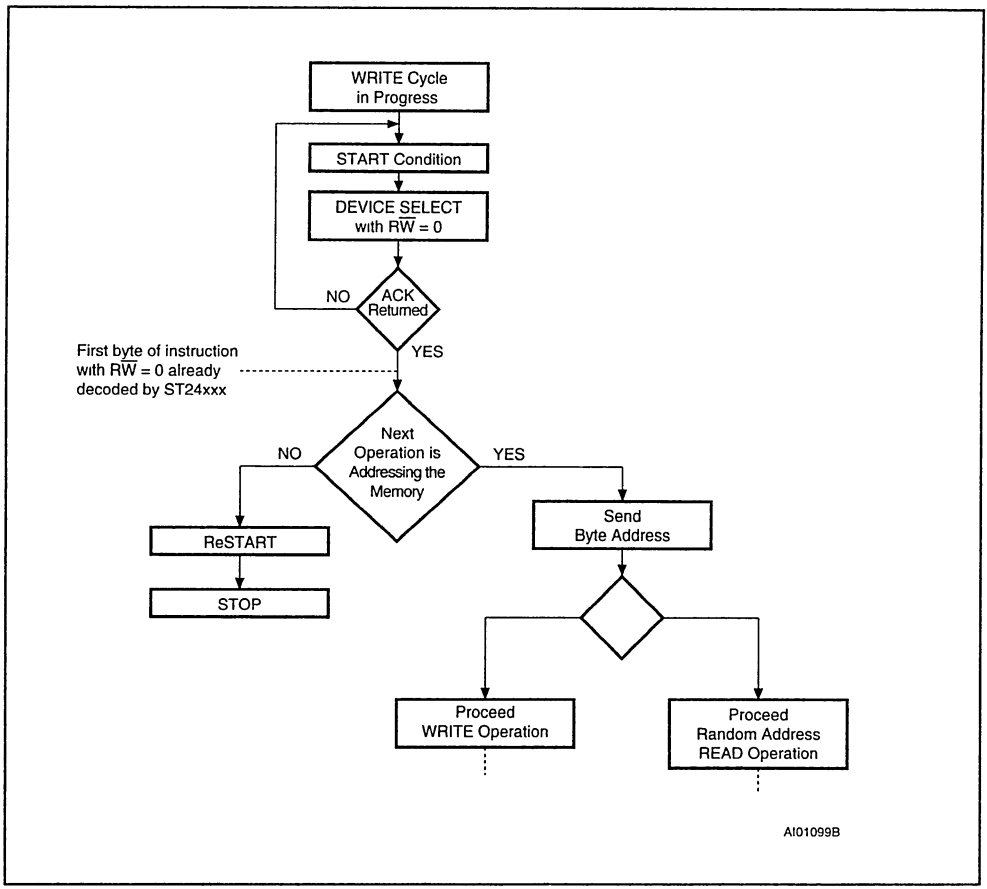
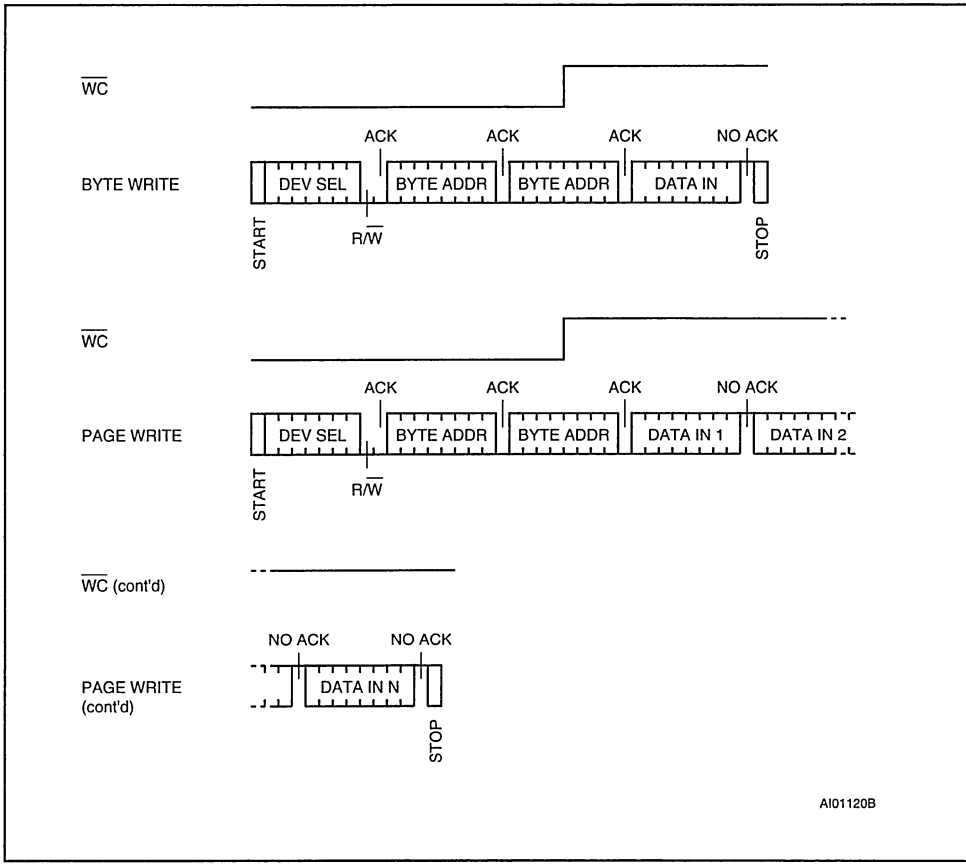


Figure 8. Write Modes Sequence with Write Control = 0



Read Operations

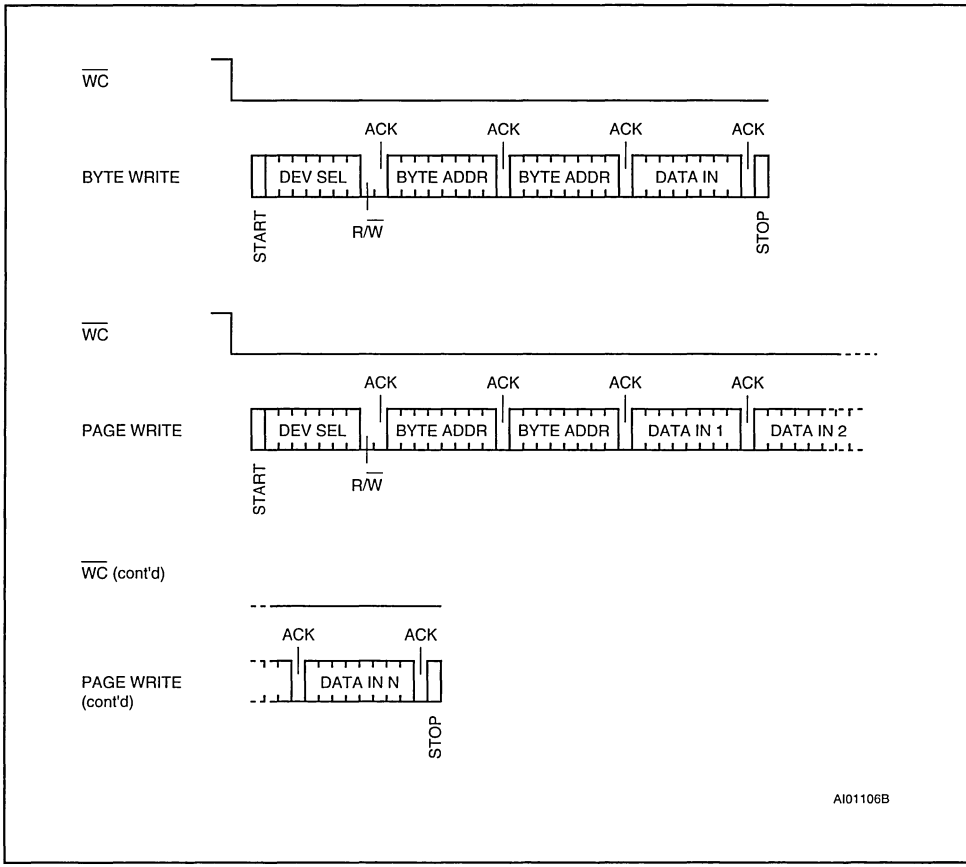
On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The ST24/25E16 have an internal 11 bits address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a Device Select with the R/W bit set to '1'. The ST24/25E16 acknowledge this and outputs the byte addressed by the internal address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address repeated with the R/W bit set to '1'. The ST24/25E16 acknowledge this and outputs the byte addressed. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the ST24/25E16 continue to output the next byte in

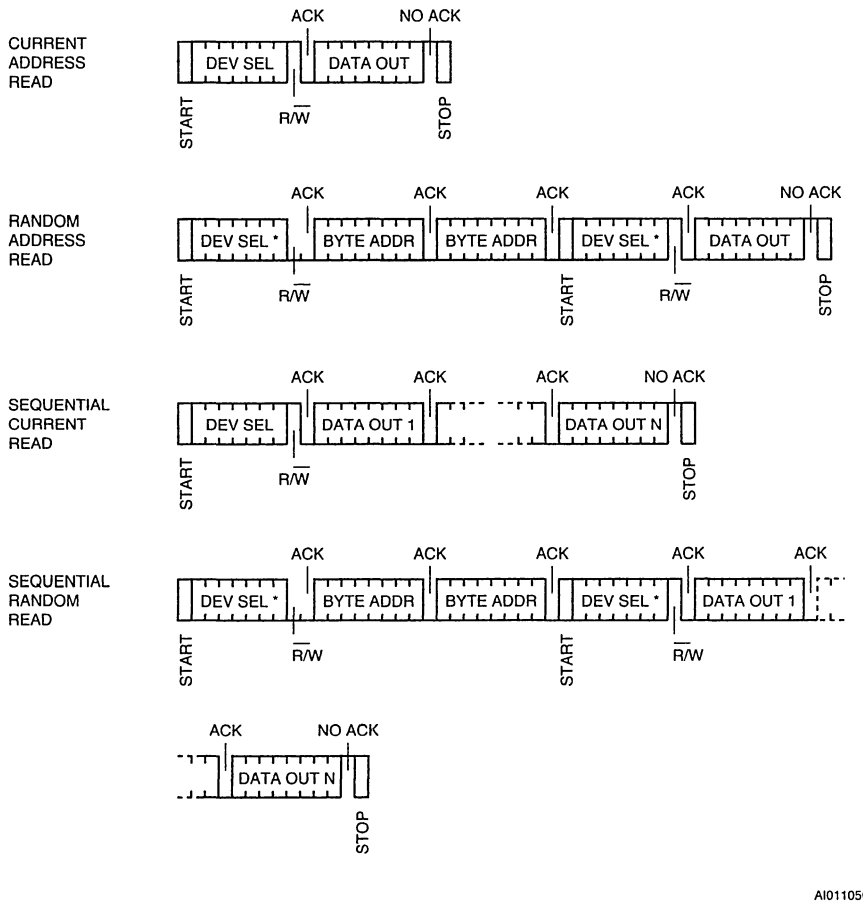
Figure 9. Write Modes Sequence with Write Control = 1



sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data.

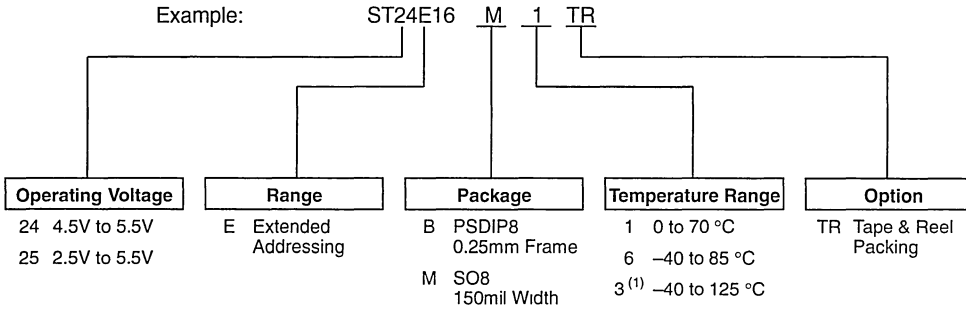
Acknowledge in Read Mode. In all read modes the ST24/25E16 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25E16 terminate the data transfer and switch to a standby state.

Figure 10. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 4th byte) must be identical.

ORDERING INFORMATION SCHEME



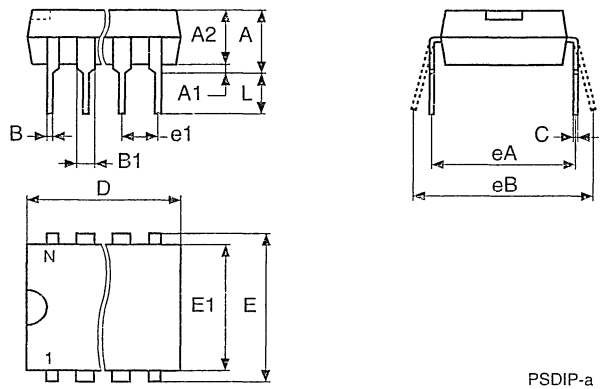
Note: 1. Temperature range on special request only

Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9 20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB		–	10.00		–	0.394
L		3.00	3.80		0.118	0.150
N	8			8		

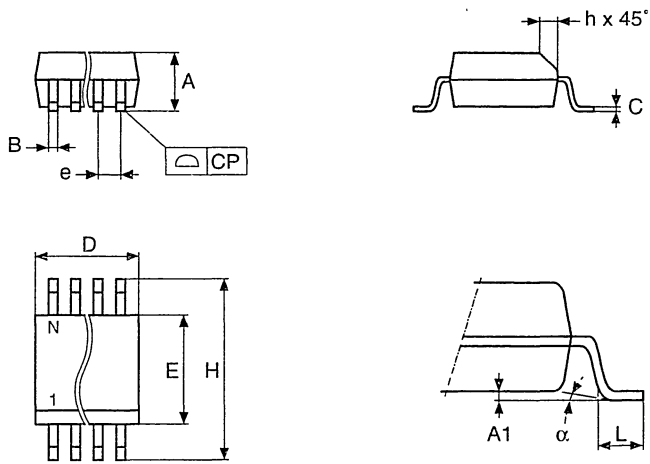


PSDIP-a

Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004



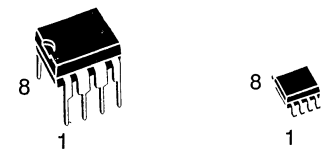
SO-a

Drawing is not to scale

M2201

2-Wires 1 Kbit (x8) Serial EEPROM

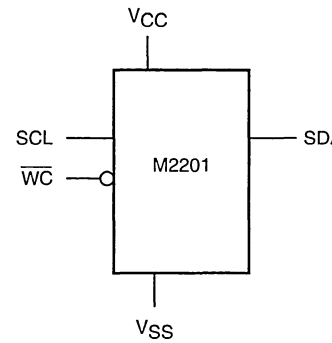
- TWO WIRE SERIAL INTERFACE
- 100.000 ERASE/WRITE CYCLES with 100 YEARS DATA RETENTION at 55°C
- SINGLE SUPPLY VOLTAGE:
  - 4.5V to 5.5V for M2201 version
  - 2.7V to 5.5V for M2201V version
- HARDWARE WRITE CONTROL
- 100 KBIT TRANSFER RATE
- BYTE WRITE
- PAGE WRITE (up to 4 BYTES)
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP



PSDIP8 (B)
0.25mm Frame

SO8 (M)
150mil Width

Figure 1. Logic Diagram



DESCRIPTION

The M2201 is a simplified 2-wire bus 1 Kbit electrically erasable programmable memory (EEPROM), organized as 128 x8 bits. It is manufactured in STMicroelectronics's Hi-Endurance Advanced CMOS technology which guarantees a data retention of 100 years at 55°C.

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

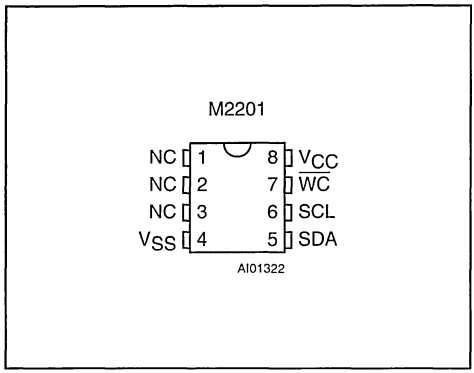
The memory is compatible with a two wire serial interface which uses a bi-directional data bus and serial clock. Read and write operations are initiated by a START condition generated by the bus master and ended by a STOP condition.

Address bits and R$\overline{W}$ bit are defined in one single byte, instead of two (or three) bytes for the standard I^2C protocol.

Table 1. Signal Names

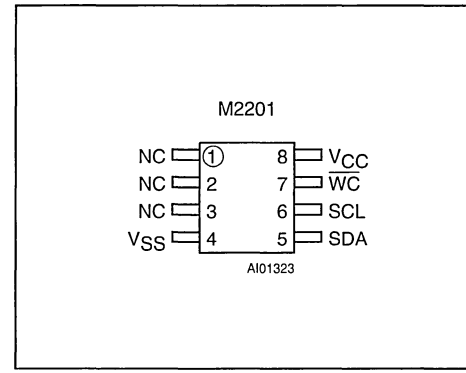
SDA	Serial Data Input/Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. DIP Pin Connections



Warning: NC = Not Connected.

Figure 2B. SO Pin Connections



Warning: NC = Not Connected.

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		–40 to 85	°C
T_{STG}	Storage Temperature		–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V_O	Output Voltage		–0.6 to 6.5	V
V_I	Input Voltage		–0.6 to 6.5	V
V_{CC}	Supply Voltage		–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		500	V

Notes: 1 Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω)

DESCRIPTION (cont'd)

When writing data to the memory, it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Write Control ($\overline{WC}$). An hardware Write Control feature ($\overline{WC}$) is offered on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable ($\overline{WC}$ = V_{IH}) or disable ($\overline{WC}$ = V_{IL}) the internal write protection. When unconnected, the $\overline{WC}$ input is internally read as V_{IL} ($\overline{WC}$ is disabled).

DEVICE OPERATION

The device that controls the data transfer is known as the master. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The M2201 is always a slave device in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the M2201 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the M2201 and the bus master. A STOP condition at the end of a Read command forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the M2201 sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS})

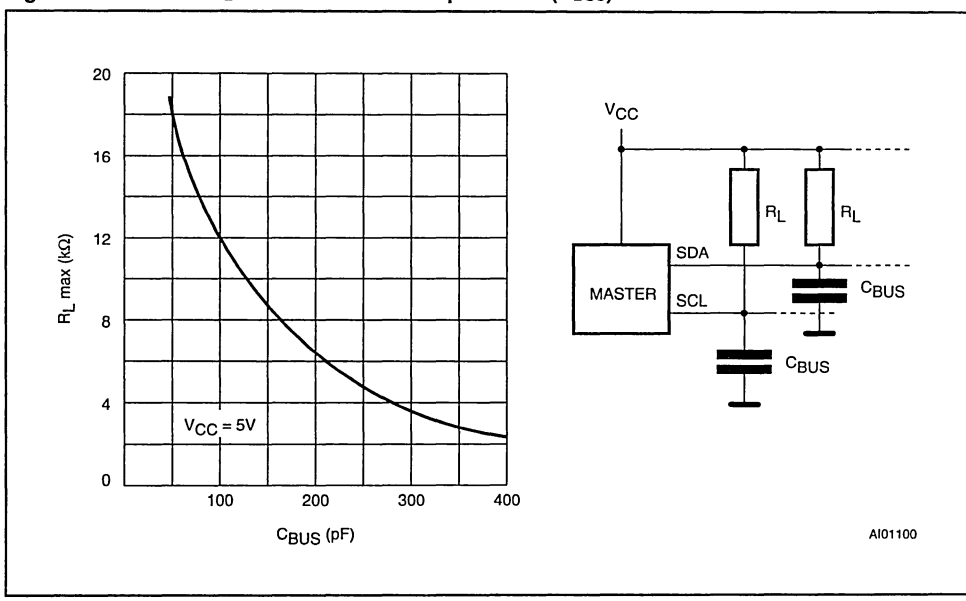


Table 3. Input Parameters (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL} (1)	$\overline{WC}$ Input Impedance	$V_{IN} \le 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH} (1)	$\overline{WC}$ Input Impedance	$V_{IN} \ge 0.7\ V_{CC}$	500		kΩ
t_{LP} (1)	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. The results come from simulation, actual results may vary. These figures are not guaranteed.

Table 4. DC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.7V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current (M2201)	V_{CC} = 5V; f_C = 100kHz (Rise/Fall time < 30ns)		2	mA
	Supply Current (M2201V)	V_{CC} = 2.7V; f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby) (M2201)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
I_{CC2}	Supply Current (Standby) (M2201V)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.7V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.7V; f_C = 100kHz		50	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage ($\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage ($\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage (M2201)	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (M2201V)	I_{OL} = 2mA, V_{CC} = 2.7V		0.4	V

Table 5. AC Characteristics
(T_A = 0 to 70 °C or –40 to 85 °C; V_{CC} = 4.5V to 5.5V or 2.7V to 5.5V)

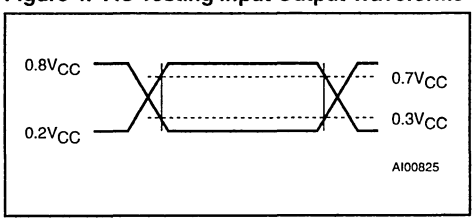
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU.STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD\ STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD\ DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU\cdot DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU\ STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV} (2)	t_{AA}	Clock Low to Next Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Data Out Hold Time	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_W	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. The minimum value delays the falling/rising edge of SDA away from SCL = 1 in order to avoid unwanted START and/or STOP conditions.

Table 6. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}
Input and Output Timing Ref. Voltages	0.3V_{CC} to 0.7V_{CC}

Figure 4. AC Testing Input Output Waveforms

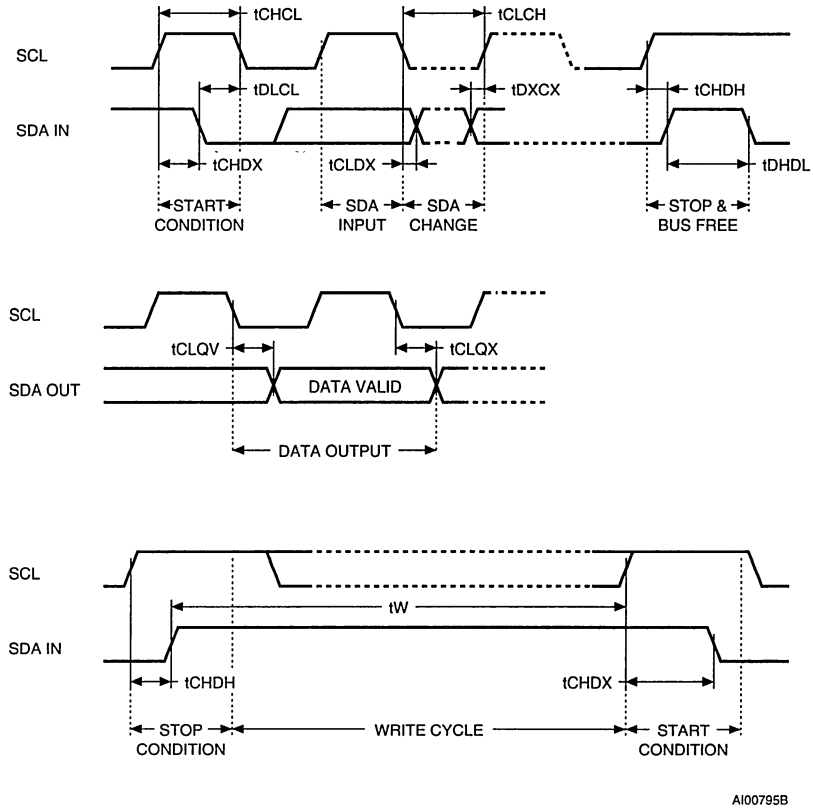


Memory Addressing. To start communication between the bus master and the slave M2201, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the 7th bit byte-address and a READ or WRITE bit. This 8th bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Write Operations

Following a START condition the master sends the byte address with the R$\overline{W}$ bit reset to '0'. The memory acknowledges this and waits for a data byte. Any write command with $\overline{WC}$ = 1 (during a period of time from the START condition until the end of the Byte Address) will not modify data and will NOT be acknowledged on data bytes, as in Figure 8.

Figure 5. AC Waveforms



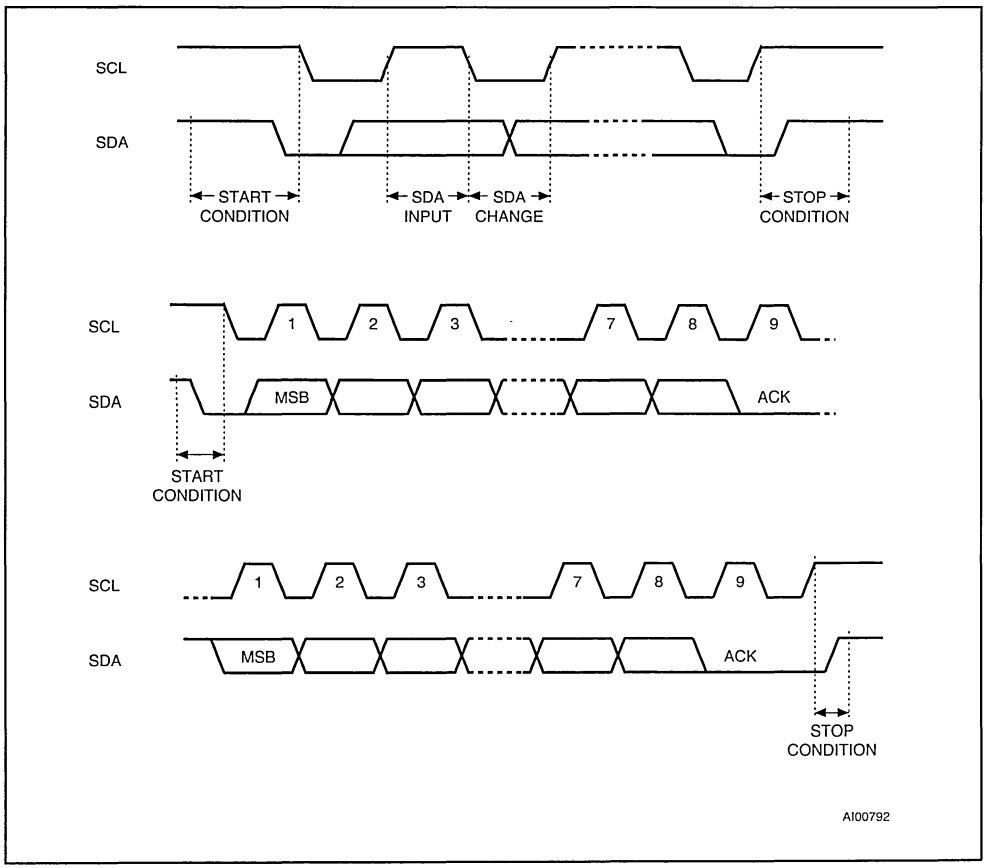
Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition.

Page Write. The Page Write mode allows up to 4 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A6-A2) are the same. The master sends from one up to four bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (2 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten.

It must be noticed that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be re-

Figure 6. I²C Bus Protocol

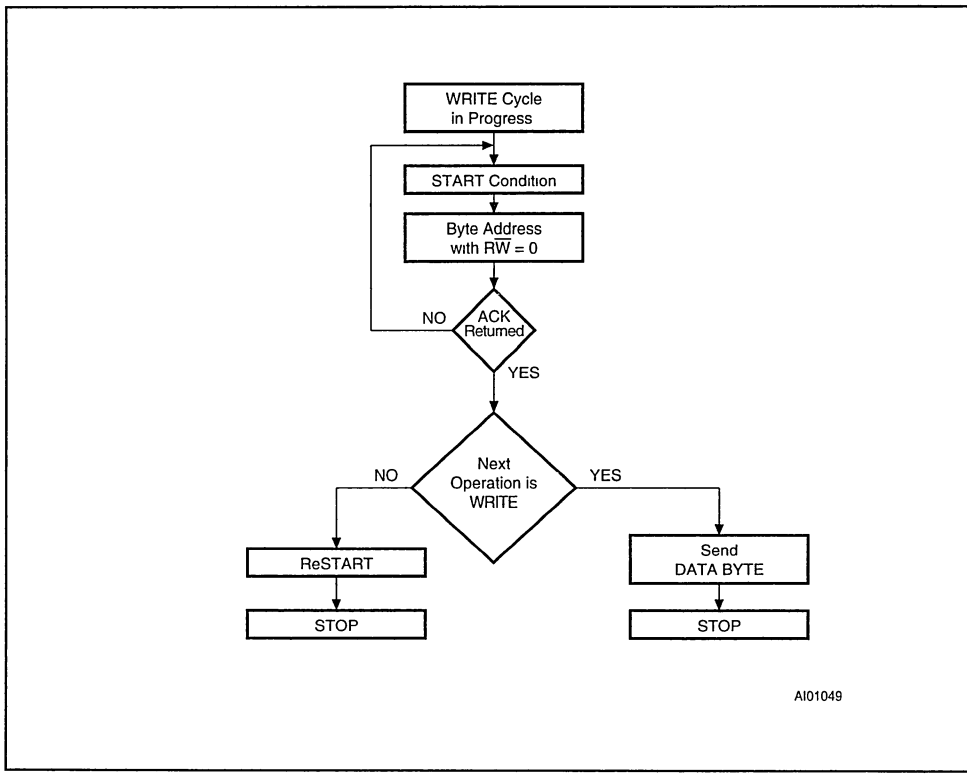


DEVICE OPERATION (cont'd)

duced by an ACK polling sequence issued by the master. The sequence is as follows:

- Initial condition: a Write is in progress (see Figure 7).
- Step 1: the Master issues a START condition followed by a Device Select byte (1st byte of the new instruction).
- Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

Figure 7. Write Cycle Polling using ACK



Read Operation

Byte Read. The master sends a START condition followed by seven bits of address and the R$\overline{W}$ bit (set to '1'). The M2201 acknowledges it and outputs the corresponding data byte. The read operation is terminated by a STOP condition issued by the master (instead of the ACK bit).

Sequential Read. The master sends a START condition followed by seven bits of address and the R$\overline{W}$ bit (set to '1'). The M2201 acknowledges it and outputs the corresponding data byte. The master does acknowledge this byte and reads the next data byte (at address + 1). The read operation is terminated by a STOP condition issued by the master (instead of the ACK bit). The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll-over to address '00' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the M2201 waits for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the M2201 terminates the data transfer and switches to a standby state.

Figure 8. Write Modes Sequences with Write Control = 1 (M2201 and M2201V)

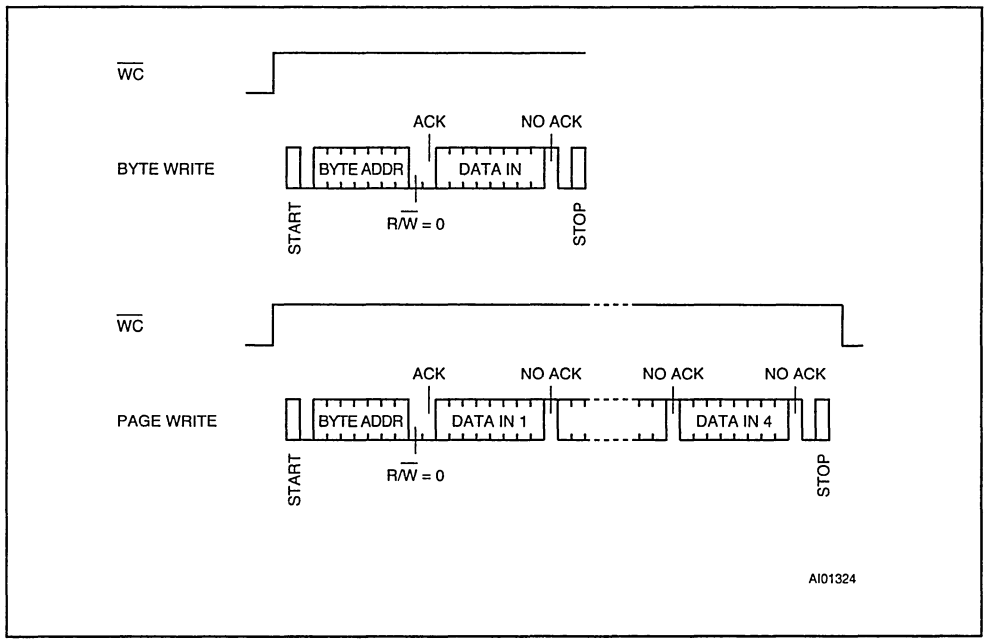


Figure 9. Write Modes Sequences (M2201 and M2201V)

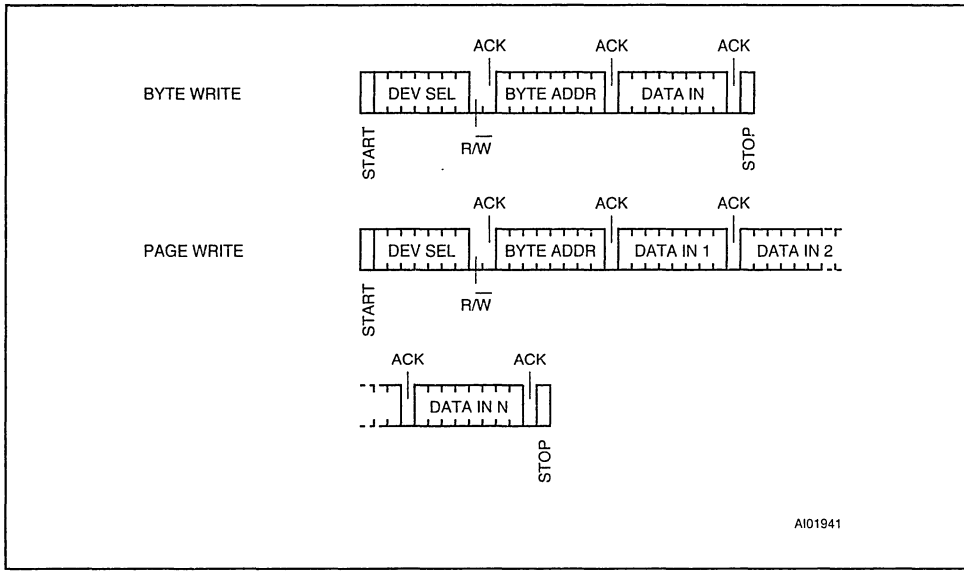
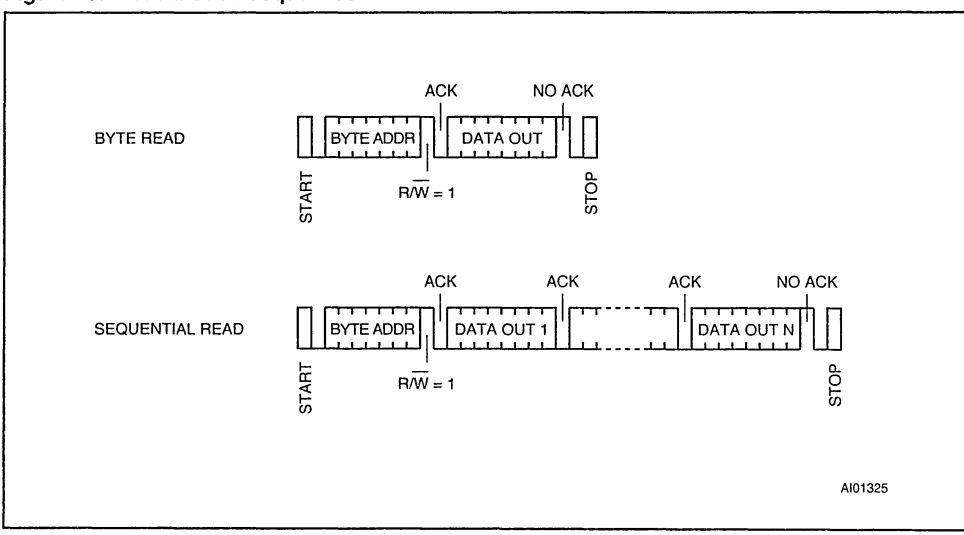
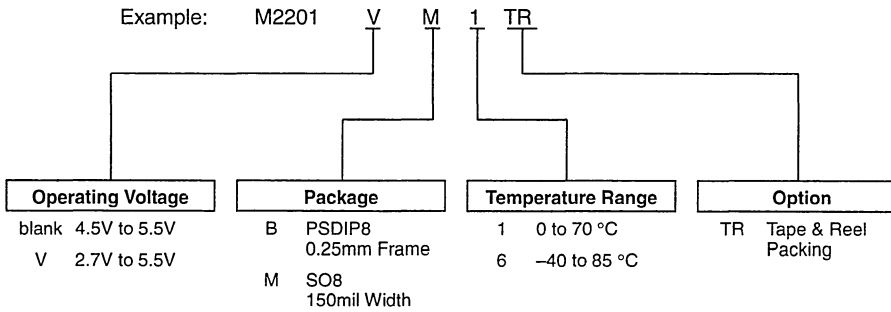


Figure 10. Read Modes Sequences



ORDERING INFORMATION SCHEME

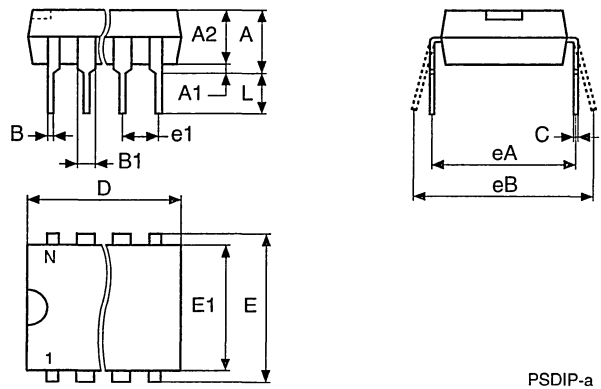


Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

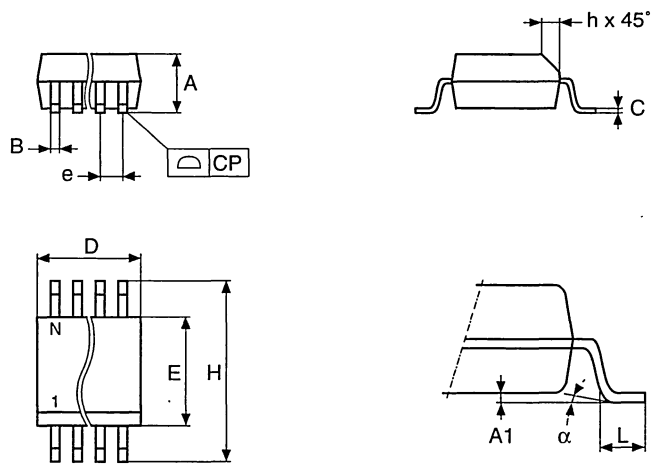


PSDIP-a

Drawing is not to scale.

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004



SO-a

Drawing is not to scale.

APPLICATION NOTES

AN626
APPLICATION NOTE

EEPROM Product Numbering

The product numbering strategy, on ST EEPROM parts, has been rationalized. Previously, the numbering strategy had had to cater many different ranges of products, when the separate groups were united to form the company. The new numbering strategy is being adopted on all forthcoming products, ranges and families, and will remain constant for the foreseeable future.

The new product numbering scheme is being introduced gradually, with no immediate effect on existing orders. Product numbers are being changed only when a device upgrade is made (such as a die shrink) or when a new product is introduced. (All major product changes are announced with a Product Change Notice.)

The new product numbers consist of a 14 digit ordering code (e.g. M28256-12WKA6T), grouped into eight fields (A to H) as shown in Table 1.

Table 1.

Digit	Field	Use
1st	A	Product line ("M" = memory)
2nd	B	Product family
3rd		
4th	C	Memory capacity
5th		
6th		
7th	-	Dash, to separate the product number identifiers from the product option designators
8th	D	Operating speed or product options
9th		
10th	E	V_{CC} range
11th	F	Package type
12th		
13th	G	Temperature range
14th	H	Tape and reel packaging

An additional solidus, "/", and two digits are used by ST to aid traceability, and might appear on some documents. These can be ignored as far as the product type and specification are concerned.

The "ST" at the start of the product number, to indicate SGS-THOMSON Microelectronics, is now being phased out.

Table 2. Field A, 1st character, Product line

M	Memory

Table 3. Field B, 2nd and 3rd characters, Product family

93	Non-Volatile Memory	MICROWIRE ®
24		I^2C ™ (including XI^2C)
25		SPI ≥ 1 Mb
95		SPI < 1 Mb
28		Parallel
33	Application Specific Memory	MICROWIRE
34		I^2C
35		SPI
37		EPROM
38		Parallel EEPROM or Dual Voltage Flash
39		Flash+

Table 4. Field C, 4th, 5th and 6th characters, Memory capacity

C01	e.g. M24C01	1 Kb I^2C serial EEPROM
C64	e.g. M24C64	64 Kb bit I^2C serial EEPROM
128	e.g. M24128	128 Kb bit I^2C serial EEPROM
etc.		
010	e.g. M95010	1 Kb SPI serial EEPROM
640	e.g. M95640	64 Kb SPI serial EEPROM
128	e.g. M95128	128 Kb SPI serial EEPROM
etc.		

The "-" character is used to separate the product identifiers from the product options.

Table 5. Field D, 8th and 9th characters (optional), Operating speed (or product options)

30	Parallel Interface Products	300 ns
25		250 ns
20		200 ns
18		180 ns
15		150 ns
12		120 ns
10		100 ns
90		90 ns
etc.		That is, for speeds less than 100 ns, the actual value is used
xx	Serial and Application Specific Memories	Maximum of two characters describing specific product options

Table 6. Field E, 10th character, V_{CC} range

"blank"	Serial devices	4.5 V to 5.5 V
V		3.0 V to 5.5 V
W		2.5 V to 5.5 V
R		1.8 V to 3.6 V
"blank"	Parallel devices	4.5 V to 5.5 V
W		2.7 V to 3.6 V

Table 7. Field F, 11th and 12th characters, Package (two letters used in every case)

BN	PSDIP8 standard
BG	PDIP24 standard
BS	PDIP28 standard
KA	PLCC32 standard
NS	TSOP28 standard
NC	TSOP40 standard
DW	TSSOP8
DL	TSSOP14
MN	SO8 narrow 0.150 mils
MW	SO8 wide 0.200 mils
ML	SO14
MJ	SO14 wide
MS	SO28
MG	SO24

Table 8. Field G, 13th character, Temperature range

1	0 °C to 70 °C
3	-40 °C to +125 °C, with a certified reliability flow tailored for the automotive industry
5	-20 °C to +85 °C
6	-40 °C to +85 °C

Table 9. Field H, 14th character, Tape and Reel packaging

"blank"	Discrete packaging
T	Tape and Reel packaging

For complete details of the correct product number, and ordering codes, for a specific product, please contact your nearest ST sales office or distributor, or the technical support centre at the electronic mail address given on the next page.

AN397
APPLICATION NOTE

Timing Specifications for Memory Products

STMicroelectronics has, for many years, committed itself to the JEDEC naming convention for the timing parameters of its memory products. Historically, timing parameter names had tended towards describing the function that was being performed during the time interval, for example:

- t_{AH} to represent the Address Hold time
- t_{DH} to represent the Data Hold time
- t_{ACC} to represent the Access time

However, these names are ambiguous. They do not specify which signals are used to indicate the start and end events, and they do not specify which transitions are involved. For example, t_{ACC} does not specify, whether this is the time from addresses becoming valid, or from the Chip Enable becoming enabled, or from the Chip Enable ceasing to be disabled.

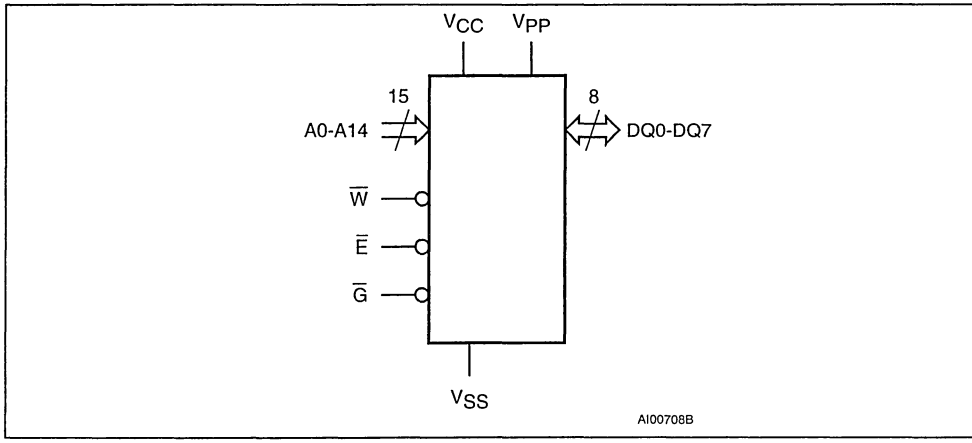
Under the JEDEC system, timing parameter names are composed from the names of the signals involved, and their corresponding logic transitions. They take the general form, t_{1234}, where 1 and 3 specify two signal names, and 2 and 4 specify the logic transitions. Each timing period consists of a start event, as specified by a given logic transition-2 on signal-1, and an end event, as specified by a given logic transition-4 on signal-3.

To help in keeping the names of the timing periods consistent between designers, there are conventions on how the signal names, 1 and 3, should be chosen, and on how the transition names, 2 and 4, should be specified. The core of the signal naming system is as follows:

- Q to represent a Data Output
- D to represent a Data Input
- A to represent an Address Line
- E to represent a Chip Enable Input
- G to represent a, Output Enable Input
- W to represent a Write Enable Input

These are shown in use for the example memory device in Figure 1.

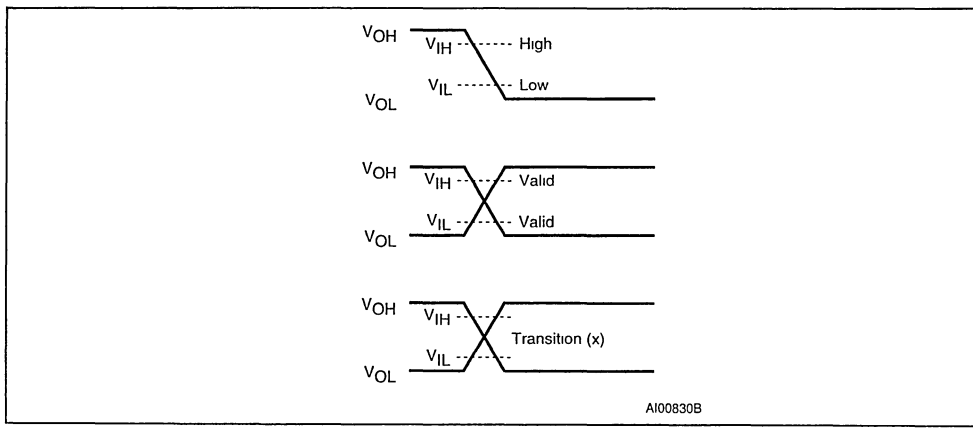
Figure 1. Signal Names on an Example Memory Device



The naming convention for the transitions is as follows:

- H indicates the earliest moment at which the signal can be considered to be driven in the high logic state (for example, as a result of a low-to-high transition).
- L indicates the earliest moment at which the signal can be considered to be driven in the low logic state (for example, as a result of a high-to-low transition).
- V indicates the earliest moment at which the signal can be considered to be driven in a valid logic state, either high or low (for example, as a result of coming out of a high-to-low, or low-to-high transition, passing through the invalid state in between).
- X indicates the earliest moment at which the signal can be considered to be driven in the invalid logic state (between V_{IL} and V_{IH} in Figure 2), neither high nor low (for example, as a result of going into a high-to-low, or low-to-high transition, passing through the invalid state in between).
- Z indicates earliest moment at which the signal can be considered to be undriven, and left floating in its high impedance state.

Figure 2. Logic State Transitions on Example Input and Output Waveforms



EXAMPLES

The parameter t_{AVQV} specifies a time interval: starting from the instant when the address lines are below V_{IL} (for signals at, or going to a logic Low level) *or* above V_{IH} (for those at, or going to a High logic level); and ending at the instant when the data output signals are all below V_{IL} or above V_{IH}.

The parameter t_{EHQZ} specifies a time interval: starting from the instant when the Chip Enable input goes above V_{IH}; and ending at the instant when the data output is no longer driven.

The parameter t_{AXQX} specifies a time interval: starting from the instant when any single address line goes outside its stable, valid level; and ending at the instant when any data output line transition passes these levels, and is consequently no longer valid.

Some further examples are shown in the first column of Table 1. The second column indicates the old style of name for the same parameter. As can be seen in some of the names, the inversion bar is always omitted from signals that use negative logic. For example, $\overline{E}$ from Figure 1 appears as E in t_{ELQX} in Table 1.

Table 1. Timing Characteristics Example

Symbol	Alt.	Parameter
tAVAV	tRC	Read Cycle Time
tAVQV	tACC	Address Valid to Output Valid
tELQX	tLZ	Chip Enable Low to Output Transition
tELQV	tCE	Chip Enable Low to Output Valid
tGLQX	tOLZ	Output Enable Low to Output Transition
tGLQV	tOE	Output Enable Low to Output Valid
tEHQZ		Chip Enable High to Output Hi-Z
tGHQZ	tDF	Output Enable High to Output Hi-Z
tAXQX	tOH	Address Transition to Output Transition

Notes: 1. These are taken from the FLASH Memory data sheets.

MEASUREMENT CONDITIONS

There are a few other parameters that need to be included in the data sheets, to make the specification complete. Firstly, the limits on the output levels, as used in Figure 2, need specifying:

$$V_{OH} \geq 0.8\ V_{CC}$$

$$V_{OL} \leq 0.2\ V_{CC}$$

Next, the thresholds recognized by the input buffers, again as used in Figure 2, need specifying:

$$V_{IH} \geq 0.7\ V_{CC}$$

$$V_{IL} \leq 0.3\ V_{CC}$$

Finally, the reference voltages for the timing measurements need specifying. Let us call them V_{RH} and V_{RL}, here, but note that, because these are not physical parameters of the hardware, they are not generally given explicit names in the data sheet. However, they do appear in the "AC Measurement Conditions" table, and in the accompanying "AC Testing Input Output Waveforms" diagram. Generally, they set at V_{IH}(min) and V_{IL}(max), respectively. That is, the measurement equipment is set to recognize the logic thresholds at the same voltages as are recognized by the input buffers of the chip.

$$V_{RH} = 0.7\ V_{CC}$$

$$V_{RL} = 0.3\ V_{CC}$$

Notice, though, that this is by definition, and is not itself a measured parameter (hence the "equal" sign, rather than the "less than or equals" or "greater than or equals" sign for the bounded value.

Although, in theory, no timings depend on the rise and fall times of signals, some products may have characteristics which vary with the slew rate of the input. For an ST EPROM device, the data sheet might state "Input rise and fall times are 20 ns (max)".

As a further point of definition, the data sheets might state that "a signal is defined as Hi-Z (high impedance) when it is not driving or being driven".

TIMING DIAGRAMS

The JEDEC convention leads to clearer, less ambiguous timing specifications. Also, it allows a substantial simplification to be made to timing diagrams, and hence to an increase in their clarity. Since the voltage reference levels (V_{RH} and V_{RL}) are specified explicitly in the data sheet, as described in the section above, these levels do not need to be spelled out precisely each time on the timing diagram. Instead, it is sufficient to depict, diagrammatically, the timing events starting and ending at the midpoints of logic transitions, and to let the name of the parameter indicate which of the reference levels are involved.

For example, the data sheet might specify the measurement conditions, with V_{CC}=5 V, as follows:

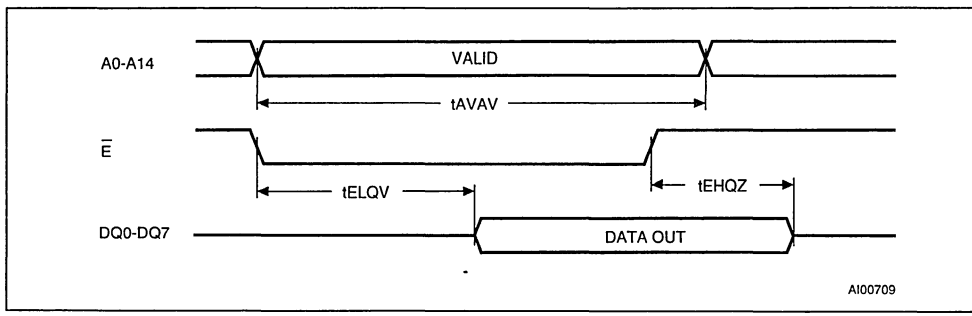
- Input Voltage levels are V_{OL}=1 V and V_{OH}=4 V
- Input and Output timing reference levels are 1.5 V and 3.5 V
- Output Hi-Z is the point where the signal is no longer driving

The parameters in the timing diagram (Figure 3) would then be interpreted as follows:

- t_{AVAV} is measured from the point where all address lines are either above 3.5 V or below 1.5 V, to the point of similar conditions at the end of the cycle.
- t_{ELQV} is measured from $\overline{E}$ being below 1.5 V, to the point when all data lines are either above 3.5 V or below 1.5 V.
- t_{EHQZ} is measured from $\overline{E}$ being above 3.5 V, to the point when the data outputs are no longer driving the signal lines.

Note that, in Figure 3, the t_{ELQV} timing, for example, is shown diagrammatically not from a "low" point on the $\overline{E}$ falling edge, but from the center, and is shown not to a "high/low" point on the Data Output but again to the center.

Figure 3. Timing Diagram (an Example)

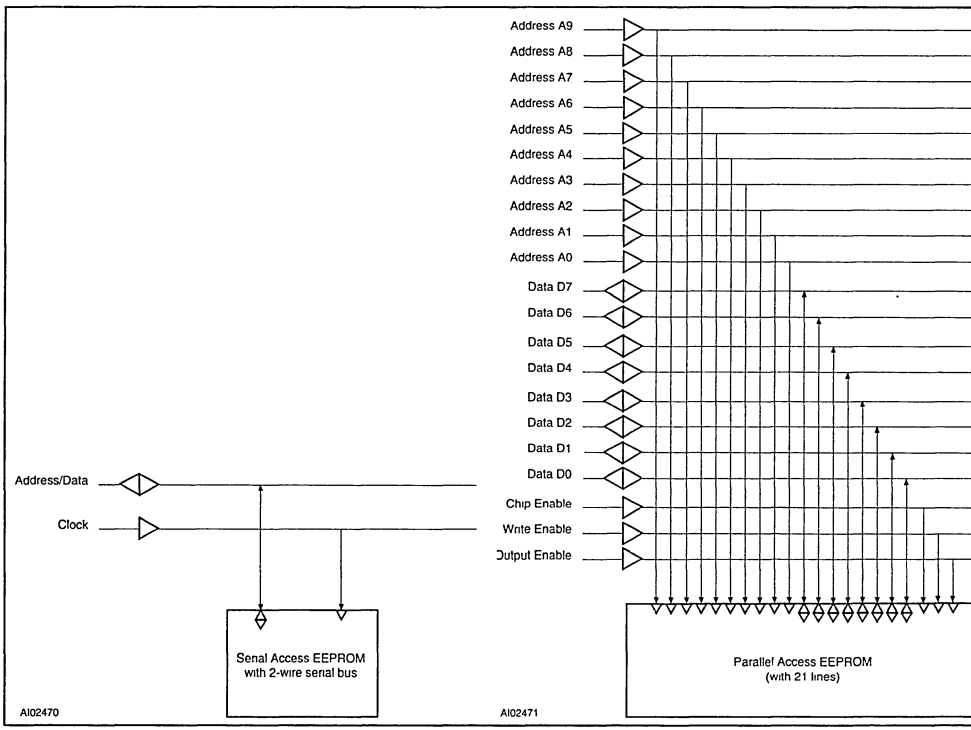


AN1001
APPLICATION NOTE

Choice of Serial EEPROMs Requires Understanding of Bus Differences

Serial access memory devices offer many advantages over their parallel access counterparts. The list on the next page assumes the use of 10-bit addressing, as depicted in Figure 1. The differential becomes even greater as the address space is increased.

Figure 1. Serial Access versus Parallel Access



The advantages of serial access to the EEPROM, or other slave devices, over parallel access, can be listed as follows:

- Fewer interconnect lines and PCB tracks:
  - A factor of 1/18th compared to the PCB area that is taken up by the ten address and eight data lines
- Fewer line buffers:
  - A factor of 1/18th comparing the PCB area that is taken up by address and data buffers
  - A factor of between 1/8th and 1/18th of the cost of address and data buffers (remembering that the address buffers of the parallel memory can be simple unidirectional devices)
- Fewer control lines:
  - A factor of 1/3rd, say, of the PCB area taken up by the control line pins of the chip
- Fewer interconnect pins:
  - A factor of 1/5th, say, of the PCB area taken up by the pins of the chip, and hence its footprint
- Fewer on-chip buffers: A factor of between 1/8th and 1/18th of the silicon area taken up by pads and I/O buffers for the address and data lines:
  - Therefore, serial access memory devices have more silicon area available for increasing the memory capacity, appearing on the market earlier than parallel access memory devices using comparable technology.

The greatest disadvantage of serial access memory, of course, is access time.

- Lower data rate, due to the serial multiplexing of the single data line:
  - A factor of between 1/8th and 1/10th (depending on the number of stop and acknowledge bits) of the data transfer rate, during the data transfer cycles.
  - An even worse factor for the address transfer rate, partly because of the 10-bit address width, and partly because of the prefix instruction required to put the memory in its address-mode.

For many applications, though, the access times of parallel access memory devices represent "overkill" – being unnecessarily fast for the requirements of the application. EEPROM is not used like RAM, and is used, in many applications, mainly for system parameter tables. These do not require very high speed access to the data for reading or writing, so serial bus speeds of 100 kHz to 1 MHz are more than adequate.

COMPARISON OF THE FOUR MAJOR SERIAL ACCESS STANDARDS

Having decided that serial access EEPROM is an appropriate choice for the application, the next design problem faced by the engineer is one of choosing the most appropriate serial bus standard. There are four main ones to choose from, each one available in STMicroelectronics memory products, and each offering differing capabilities in terms of bus size, bus protocol, noise immunity and access time.

- I^2C bus
- XI^2C bus
- SPI bus
- MICROWIRE bus

This document discusses these four standards, and the design trade-offs with which the application designer is faced when choosing between them.

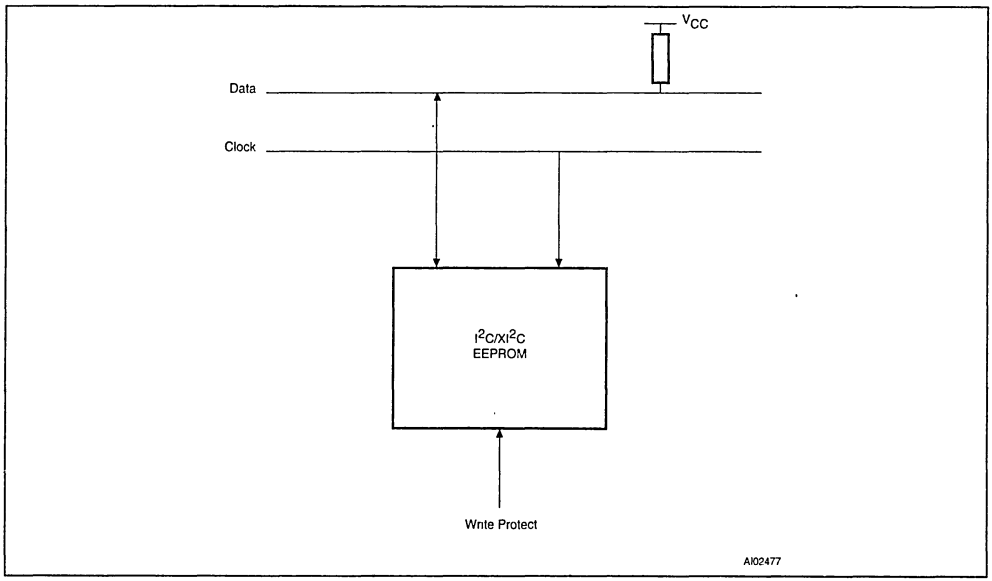
I²C AND XI²C BUSES

Perhaps the most popular of the four standards is the I²C bus, designed by Philips. It was initially aimed at consumer applications market. A wide spectrum of devices is available today, not only memory devices.

The I²C standard specifies a two-wire bus, as shown in Figure 2. Its sophisticated protocol allows systems to support many devices on the bus, with the capability even of allowing multiple masters, as well as multiple slaves.

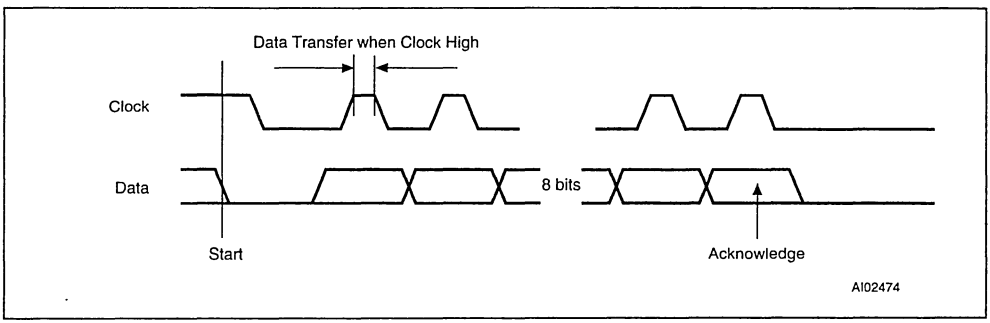
The original I²C standard only allowed an address space of up to 16 Kbit of memory, but the subsequent XI²C (extended I²C) bus standard, has extended this to 4 Mbit. The bus speed is limited to 100 kHz for I²C and 400 kHz for XI²C. The noise immunity in both cases is good.

Figure 2. I²C and XI²C Bus Block Diagram



Bus transfers start when the clock line is high on the falling edge of the data, as shown in Figure 3. Transfers are always 8 bits, followed by a ninth – an acknowledge bit from the bus receiver. Data is transferred when the clock signal is high. The data line is wired "or" with an external pull-up resistor to V_{CC}.

Figure 3. I²C and XI²C Bus Timing

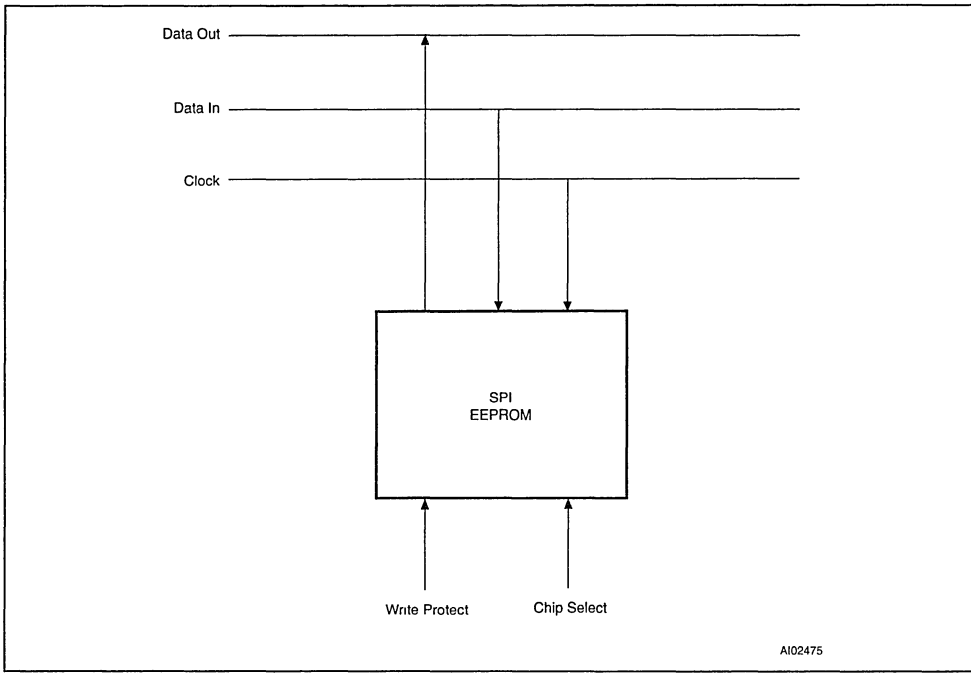


SPI BUS

The SPI standard was first proposed by Motorola, for its microcomputers, but is now offered by ST and other companies, integrated as a peripheral into their MCUs, and is rapidly gaining support.

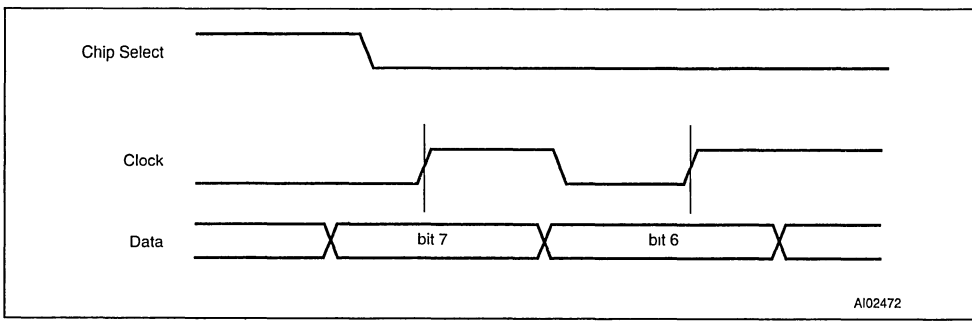
Memories using this bus have four signal wires (data input, data output, clock and chip select), as shown in Figure 4. Each device on the bus must have its own, separate, chip select line. This means there is no limit to the number of slaves on one SPI bus, but each increase demands another MCU I/O line. The maximum bus speed is 5 MHz, and the noise immunity is very good.

Figure 4. SPI Bus Block Diagram



Bus transfers start after the chip select goes low, as shown in Figure 5. Transfers are always 8 bit, and each bit is detected on the rising edge of the clock. A write protect input is provided.

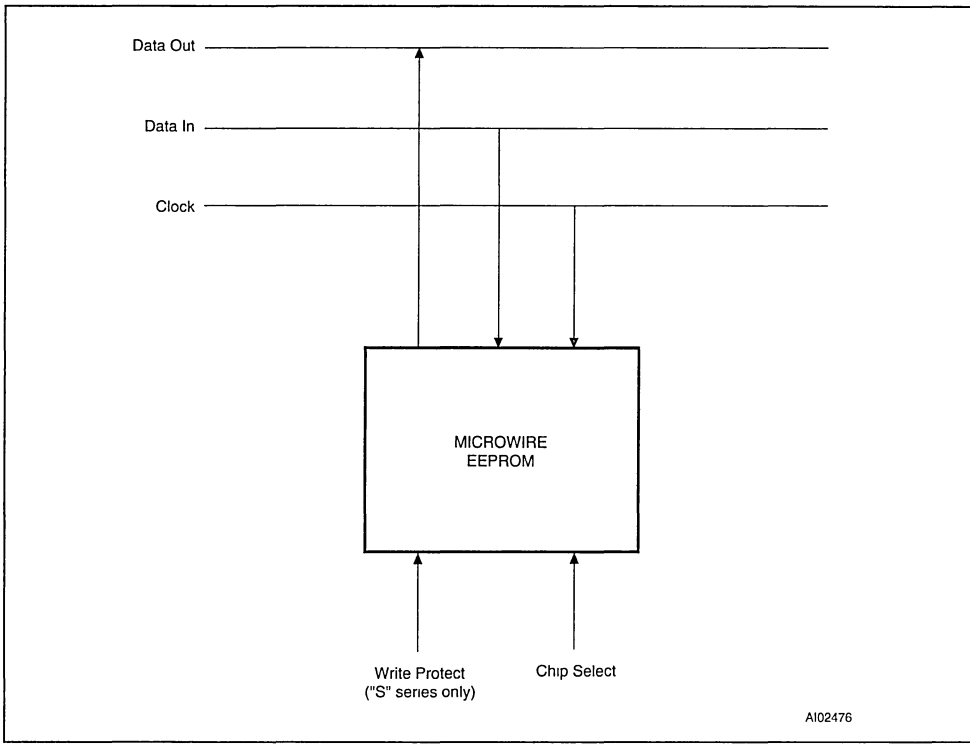
Figure 5. SPI Bus Timing



MICROWIRE™

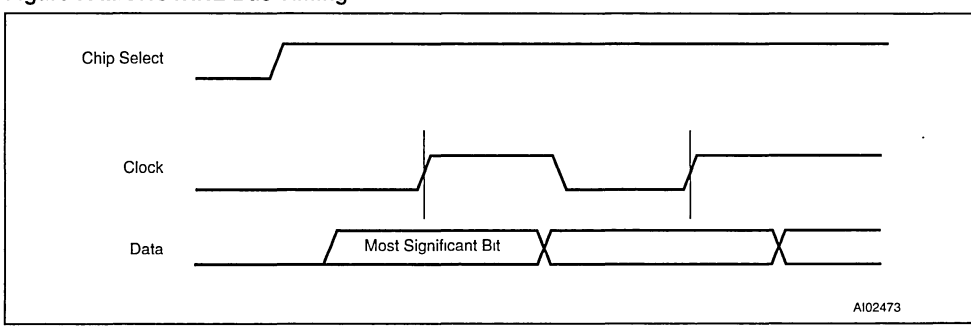
The MICROWIRE bus is based on the system that was developed for the MCU products of National Semiconductor. However, market support for this bus no longer appears to be growing. Like the SPI bus, it uses four wires and requires a chip select for each device on the bus, as shown in Figure 6. The maximum bus speed is quite high, at 1 MHz.

Figure 6. MICROWIRE Bus Block Diagram



Bus transfers start after chip select goes high. Each data bit is detected on the rising edge of the clock, as shown in Figure 7. A Write Enable input is provided on the "S" series devices.

Figure 7. MICROWIRE Bus Timing



THE BUS CHOICES

The choice of appropriate bus standard revolves round the following four major concerns:

- The number of interface pins on the MCU:
  - Here the I^2C or XI^2C buses are clear winners, since they need only two lines.
- The system communication protocol:
  - For simple read or writes to the memory by an MCU, any of the bus types offers the same potential, but in a system where many different types of circuit are connected to the bus, or where a complex system of multi-masters/multi-slaves is used, only the I^2C or XI^2C can provide the necessary resources.
- Speed:
  - This is not a primary concern in many EEPROM applications, but where it is important, the SPI and MICROWIRE buses are favoured.
- Noise immunity, data security and protection from data corruption:
  - These concerns are not completely determined by the choice of bus standard. Large differences exist between different manufacturers, and even between the different products from one manufacturer. However, this issue is discussed further on the next page.

DATA TRANSFER SPEED AND WRITE COMPLETION POLLING

The read data transfer speed of the serial buses varies from:

- one byte every 1.6 µs for the SPI with a 5 MHz clock
- one byte every 8 µs for the MICROWIRE with a 1 MHz clock
- one byte every 22.5 µs for the XI^2C with a 400 kHz clock.
- one byte every 90 µs for the I^2C with a 100 kHz clock.

All four standards support a burst mode, or sequential read mode, in which a contiguous block of any size can be read, one byte after another. I^2C and XI^2C types also support page write operations, allowing between 8 and 32 consecutive bytes to be written in 5 to 10 ms. The SPI standard is similar, but only the newer "CS" series of MICROWIRE devices offer a page write of 4 words (4x16 bits).

The ST specification, for all families of serial EEPROM, states a maximum write time of 10 ms. However, the actual value, which is managed automatically and internally, is typically much faster than this. To take advantage of the faster typical write time in systems, designers use memory polling to detect when the write sequence has finished.

The I^2C and XI^2C bus devices offer a very efficient polling system by detecting a memory acknowledge signal (a single bit that is sent by the EEPROM, or other bus receiver, in the ninth bit time after the memory is addressed or data is exchanged). Thus to poll the I^2C devices, it is sufficient to send a single one byte address to the memory and to check the acknowledge bit that is sent response.

For the SPI bus, the polling technique requires that an internal status register be read to check a write-in-progress bit. This requires a read sequence of only two bytes' length.

The MICROWIRE devices can be polled by simply placing the chip select line high. A data output low indicates that writing is still in progress.

NOISE IMMUNITY AND DATA SECURITY

Some defences, against noise and corrupt write commands, are applied automatically, internally within the device:

- A *low-pass filter* on each input pin allows noise glitches to be ignored.
- *Clock counting* allows the device to time-out if the validity of the write operation becomes dubious (such as if it has exceeded the maximum specified duration).

Other defences can be applied only at the command of the external circuitry. This is potentially the strongest defence since the external circuitry can be designed to monitor for quite elaborate conditions that are specific to the particular application.

- The *Write Control* pin (WC) can be used to disable write sequences completely when conditions are unstable.
- The user-defined Read-Only Area, along with a previously set-up address pointer in the memory, can be used to make the selected block behave like ROM.

It is possible to overlap the effects of the internal and external defences. For example, de-assertion of the WC pin, during a write cycle on some devices, causes the internal write cycle to be aborted. This is a useful fail-safe defence if the source of the glitch on the WC line is also injecting noise on the data lines.

Table 1 shows the different memory ranges, capacities and features of ST's serial EEPROMs.

Table 1. ST Serial EEPROMs (in production or for release in 1995)

Bus Type	Series	Capacity	Sequential Read	Page Write	Write Control	Write Protection
I^2C	ST24Cxx	1 Kbit-16 Kbit	x	x		4 Kbit-16 Kbit
	ST24Wxx	1 Kbit-16 Kbit	x	x		4 Kbit-16 Kbit
	M24Cxx	1 Kbit-16 Kbit	x	x	x	
XI^2C	M24xxx	16 Kbit-256 Kbit	x	x	x	
SPI	M95xxx	1 Kbit-64 Kbit	x	x	x	x
MICROWIRE	M93Cxx	256 bit-4 Kbit	x	x		
	M93Sxx	1 Kbit-4 Kbit	x	x		x

Because of its better clock counting protocol, the XI^2C standard offers good noise immunity. Each 8-bit data transfer is accompanied by a ninth bit acknowledge by the device on the bus which is the current data receiver. Moreover, a memory write cycle can only be triggered after both a correct series of acknowledges and a corresponding correct count of clock pulses. Products that include an external write control input give added protection to the memory, especially during power up.

These EEPROMs are designed to function even when V_{CC} has dropped to 1.8 V, and can be functional as low as 1.5 V. However, because the MCU is not necessarily guaranteed to be functional at these voltages, random signals from the MCU can trigger spurious write cycles. This can be prevented by holding the write control inputs low, along with the MCU reset signal, until the bus signals are stable. Both I^2C ("W" series) and XI^2C ("E" series) products from ST feature write control inputs. In addition, the XI^2C types include an input filter on the data lines which rejects pulses narrower than 50 ns, thus filtering short noise glitches.

The I^2C EEPROMs ("ST24Cxx" and "ST24Wxx" series, 4 Kbit to 16 Kbit capacities) also offer software programmed data protection. Up to half of the memory can be made to behave like ROM. A non-volatile register is set up to point to the address at which the write protection begins.

Of the two higher speed buses, SPI and MICROWIRE, SPI offers the better noise immunity and the greater data protection. The SPI protocol reads instructions, addresses and data from the bus by sampling on the rising edge of the clock. Since all transfers are in 8-bit format, this allows an internal counter to inhibit writing to the memory should the chip select go high, to indicate the start of a write cycle, when the count is not a multiple of eight. Additional immunity is provided by the instruction set which includes commands to enable a write control latch before a write cycle can begin. Lastly, detection of an incorrect command instruction will automatically de-select the chip.

Data protection in the SPI products is provided by both an external write protect input, like the I^2C and XI^2C devices, plus a programmable, non-volatile block protection scheme that allows zero, 25%, 50% or 75% of the total memory array to be write protected.

The protocol of the MICROWIRE bus has several features that allow protection against spurious glitches on data or clock lines. Two families of MICROWIRE products offer different levels data protection. The "S" family offers both a write enable input and programmable block write protection, in addition to the data protection features that were already provided in the older "C" family.

THE MEMORY ENDURANCE

A final consideration when choosing an EEPROM device is its reliability after repeated write/erase cycles. All types of non-volatile memory using floating-gate technology suffer from a gradual wear-out of the oxide. This leads to a deterioration of the cells' ability to store a "1" or a "0", and hence to malfunction and loss of data.

The endurance of the memory depends on the quality of the CMOS manufacturing process, the technology and the memory cell design. ST EEPROMs use a unique and very successful cell layout and process technology which is able to offer a performance of over one million write/erase cycles for medium capacity memory devices (up to 16 Kbit). This is ten times better than competitive products, and even if not called for in the specific application, it can be viewed as an additional "noise protection", as it guarantees much better security of memory retention during the lifetime of the equipment.

AN995
APPLICATION NOTE

Changing from the ST24xxx and ST25xxx to the M24xxx In Your Application

This document is written for users of the following ranges of EEPROM device:

Table 1. ST24xxx and ST25xxx Devices

Vcc = 4.5 to 5.5 V		Vcc = 2.5 to 5.5 V	
ST24C01	ST24W01	ST25C01	ST25W01
ST24C02	ST24W02	ST25C02	ST25W02
ST24C04	ST24W04	ST25C04	ST25W04
ST24C08	ST24W08	ST25C08	ST25W08
ST24C16	ST24W16	ST25C16	ST25W16
ST24164		ST25164	
ST24E32		ST25E32	
ST24E64		ST25E64	

The above devices, in all variations of package and temperature range, are to be discontinued. They can be replaced by equivalents in the more advanced M24xxx range:

Table 2. M24xxx Devices

Vcc = 4.5 to 5.5 V	Vcc = 2.5 to 5.5 V
M24C01	M24C01-W
M24C02	M24C02-W
M24C04	M24C04-W
M24C08	M24C08-W
M24C16	M24C16-W
M24164	M24164-W
M24C32	M24C32-W
M24C64	M24C64-W

For the majority of applications, the M24xxx devices can be treated as pin compatible and functionally equivalent to the ST24xxx and ST25xxx devices, as listed in the first two columns of the following table. There are some exceptional cases, though. For these, the third column of the table makes reference to the notes on the next page.

Table 3. Approximate Equivalents

Capacity	Previous device	Eagle range replacement	Exceptions
1 Kbit	ST24C01	M24C01	see note 2
	ST24W01	M24C01	
	ST25C01	M24C01-W	see note 2
	ST25W01	M24C01-W	
2 Kbit	ST24C02	M24C02	see note 2
	ST24W02	M24C02	
	ST25C02	M24C02-W	see note 2
	ST25W02	M24C02-W	
4 Kbit	ST24C04	M24C04	see notes 1 & 2
	ST24W04	M24C04	see note 1
	ST25C04	M24C04-W	see notes 1 & 2
	ST25W04	M24C04-W	see note 1
8 Kbit	ST24C08	M24C08	see notes 1 & 3
	ST24W08	M24C08	see note 1
	ST25C08	M24C08-W	see notes 1 & 3
	ST25W08	M24C08-W	see note 1
16 Kbit	ST24164	M24164	
	ST24C16	M24C16	see notes 1 & 3
	ST24W16	M24C16	see note 1
	ST25164	M24164-W	
	ST25C16	M24C16-W	see notes 1 & 3
	ST25W16	M24C16-W	see note 1
32 Kbit	ST24E32	M24C32	
	ST25E32	M24C32-W	
64 Kbit	ST24E64	M24C64	
	ST25E64	M24C64-W	

NOTE 1: USE OF THE PROTECT ENABLE (PRE) PIN

If, in the circuit, the PRE pin (pin 1) is always held low, the M24xxx family can be used as a direct replacement for the original device. If, though, the PRE pin is held high, or is allowed to vary, the replacement is not so direct, and the designer is advised to contact the ST local sales office for technical support (or to e-mail the technical support electronic mail address: *ask.memory@st.com*).

NOTE 2: USE OF THE MODE (MODE) PIN FOR ACCESSING MORE THAN 4 BYTES

If, in the circuit, the MODE pin (pin 7) is always held low, the M24xxx family can be used as a direct replacement for the original device. If, though, the MODE pin is held high, or is allowed to vary, the device is being used to make multibyte accesses. If no more than 4 bytes are manipulated at a single write access of any given page, then the direct replacement can still be made.

However, if multibyte write accesses of more than 4 bytes per page ever occur, the replacement is not so direct, and the designer is advised to contact the ST local sales office for technical support (or to e-mail the technical support electronic mail address: *ask.memory@st.com*).

NOTE 3: USE OF THE MODE (MODE) PIN FOR WRITING MORE THAN 8 BYTES

This exception is identical to that described in note 2, except that up to 8 bytes in any one write access are tolerated by the M24xxx replacement, allowing the direct replacement still to be made.

Extending the I²C Bus — XI²C

The I²C (Inter Integrated-Circuit) standard was designed for applications that need to be highly efficient of board space. It has been adopted almost universally by consumer equipment makers for internal communication between the digital ICs in their products. It is also gaining popularity in other types of equipment.

The standard uses a two wire bus: respectively the serial data line (SDA) and the serial clock line (SCL). Each line is configured for use in a wired-or arrangement, with one external pull-up resistor each. Data on SDA is synchronous with respect to SCL.

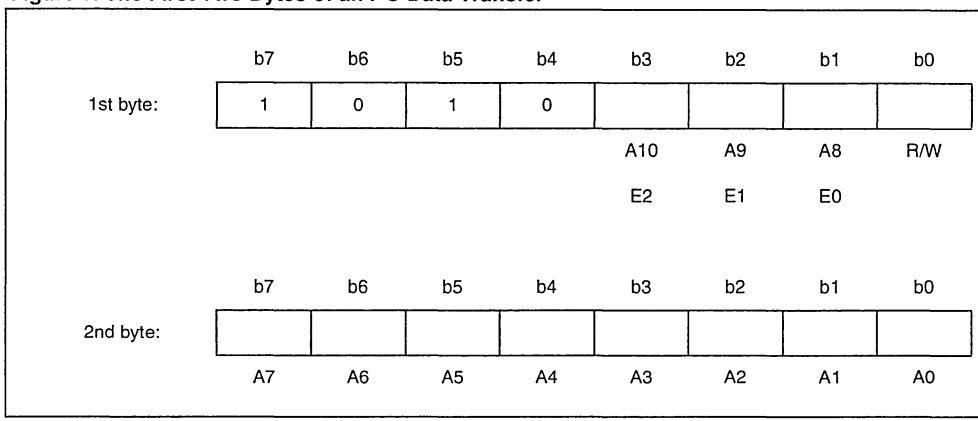
Specific combinations of data and clock signals are used to mark the Start or Stop of a data transfer. Devices on the bus can act as transmitters or receivers of data. Their action can also be described as being initiators (masters) or responders (slaves) of the data transfer.

Each type of circuit connected to the bus has a unique "device select code". For example, all memory devices have the four bit code "1010" and will only respond if they detect this code.

I²C BUS

Figure 1 shows how the first byte of a data transfer contains the EEPROM select code "1010", the chip enable E2-E0 or address bits A10-A8, and the read/write operation bit. The second byte contains the address bits A7 to A0.

Figure 1. The First Two Bytes of an I²C Data Transfer



Addresses on the I²C bus, therefore, are limited to 11 bits, and hence to an address space of 2 Kbyte. In the case of a 2 Kbyte memory chip, the address is decoded directly from the A10 to A0 settings. In the case of a 256 byte memory chip, only address bits A7 to A0 are used. This leaves the bits in the first byte available for use as chip select bits, E2 to E0. The 256 byte memory chip will only respond to the address in bits A7 to A0 if the pattern in the E2 to E0 bits is the same as that which has been hard-wired on the E2

to E0 pins of the chip itself. In this way, it is possible to select between as many as eight 256 byte memory chips, and hence an address space still of the maximum 2 Kbyte capacity.

Between these two extremes, it is also possible to implement a memory capacity of 2 Kbyte using two 1 Kbyte memory chips, or four 512 byte memory chips. The four possible configuration, therefore, are as follows:

- 1 chip containing 2 Kbyte, 16 Kb, of memory (addresses A10-A8 in the first byte, A7-A0 in the second)
- 2 chips containing 1 Kbyte (one chip enable, E, to select between them, and address bits A9-A8 in the first byte, A7-A0 in the second)
- 4 chips containing 512 bytes (two chip enables, E2-E1, to select between them, and address bit A8 in the first byte, A7-A0 in the second)
- 8 chips containing 256 bytes (three chip enables, E2-E0, in the first byte to select between them, and address bits A7-A0 in the second)

THE EXTENDED I^2C BUS

The I^2C bus suffers from two limitations built into its specification:

- It allows a maximum of 11 bit addressing, giving a memory limit of 2 Kbyte (16 Kb).
- It offers a maximum transfer rate of 100 Kb/second.

As equipment was needing ever larger amounts of EEPROM for parameter storage, it became apparent that a new standard was required. In January 1992, a new specification was published for the I^2C bus which increased the speed up to 400 Kb/second, and added an option for extending the slave-select (chip enable) bits to 10 bits (E0 to E9), thus allowing up to 1024 slave devices to be connected to the bus.

Upon receiving the special four bit code "1111", in place of the usual "1010", the hardware would switch from the default I^2C mode, and would expect the next eleven bits (3 bits in the current byte, and 8 in the next) to contain a leading 0 followed by E9 to E0.

However, SGS-THOMSON was not happy with this proposal as it is not backward compatible with the previous standard. ***This format is not supported by ST's EEPROM devices.***

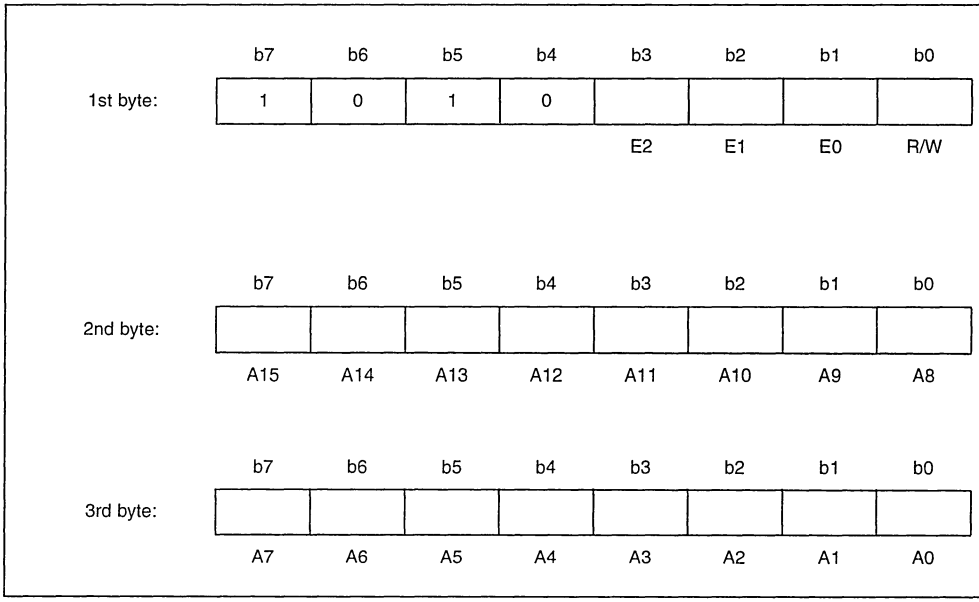
Instead, SGS-THOMSON took the initiative to request a further change to the I^2C bus. The aim was to extend the memory addressing itself, rather than just the number of chip enable lines, by using two address bytes instead of one. This would allow up to three bits for chip enable selection E2-E0 (or addresses A18-A16) and a full 16 bit address A15 to A0. Memory addresses could thereby be extended from eight blocks of 256 bytes to eight blocks of 64 Kbytes (a total capacity of 512 Kbyte, 4 Mb). This request was granted, and gave rise to the Extend I^2C format, otherwise known as "XI^2C". The format is depicted in Figure 2.

A further feature of this format is that, if bits b3-b1 of the first byte are used for chip enable E2-E0, it is possible to implement a system that addresses a mixture of I^2C and XI^2C devices.

400 K BITS PER SECOND

The main implications of changing to faster clocking rates are felt not only by the bus interface, in which the timing schedule needs adaptation, but also by the spike suppression circuitry in the memory chip. Each input must be able to reject noise pulses of up to 50 ns in width, and each output must be able to sink up to 6 mA at VOL = 0.6 V, and to have a output fall time of no more than 250 ns.

Figure 2. The First Three Bytes of an XI²C Data Transfer



NEW PRODUCTS

The first devices to use the XI²C standard are listed in Table 1. The total theoretical capacity is 4 Mb, so future ST product growth is assured for many years to come.

Table 1. Members of the M24xxx Eagle Range

Product	Description
M24C32	32 Kb XI²C EEPROM, organised as 4 Kbyte
M24C64	64 Kb XI²C EEPROM, organised as 8 Kbyte
M24128	128 Kb XI²C EEPROM, organised as 16 Kbyte
M24256	256 Kb XI²C EEPROM, organised as 32 Kbyte
M24512	512 Kb XI²C EEPROM, organised as 64 Kbyte

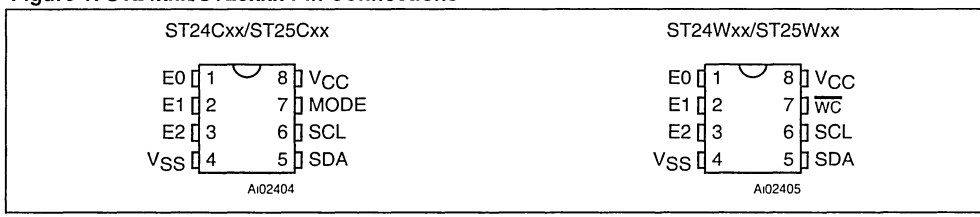
AN1006
APPLICATION NOTE

The Write Control Feature on I²C EEPROM

The ST24xxx/ST25xxx EEPROM devices are fully compatible with the I²C ™ standard. Some, though, have the extra feature of offering a hardware write control (WC) line. The purpose of this document is to highlight the advantages of this facility.

On the ST24Cxx/ST25Cxx I²C EEPROM devices, pin 7 is used to select between the multibyte and page-write modes. On the ST24Wxx/ST25Wxx I²C EEPROM devices, this is replaced by the WC line, as shown in Figure 1.

Figure 1. ST24xxx/ST25xxx Pin Connections



WC is an active-low signal. When it is held low, erase and write commands are executed; when it is held high, erase and write operations are inhibited (and any erase or write commands issued by the master device are ignored).

This feature has been designed to be used by the application hardware whenever there is any question as to the validity of the data. The device can thereby reject the data, and wait for the master device to send it again. In particular, the ST24W/25Wxx series, in combination with suitable hardware design, can offer better data protection against the following conditions:

- during power-up and power-down sequences, when voltage levels are wandering out of specification
- whenever high levels of electrical noise are detected, and the validity of the received data becomes questionable
- whenever the I²C bus is shared by devices using other protocols, and unexpected conflicts arise
- under other detectable fault conditions, specific to the application.

For specific examples of the use of this feature, please see Application Notes *AN404* and *AN627*.

AN1116
APPLICATION NOTE

Changing from the ST95P08 to the M95080 in Your Application Using a Simple Software Recognition Method

The members of the new M95xxx, SPI serial-bus, EEPROM chips offer features that were not available with the ST95xxx family. Table 1 summarizes the main differences between the new 8 Kbit M95080 memory, and the ST95P08, by way of example.

This document is aimed at helping the designer to convert designs from using the ST95P08 to using the M95080. It concludes by indicating a simple algorithm that can be used in the application software to detect which of the two devices is being used.

Table 1. Differences and Improvements (Functional and Electrical) Between the ST95P08 and the M95080

	ST95P08	M95080
Memory capacity	8 Kbit	8 Kbit
Supply range (V_{CC})	3 V to 5.5 V	4.5 V to 5.5 V 2.5 V to 5.5 V 1.8 V to 3.6 V
Clock frequency (f_{MAX})	2 MHz	5 MHz
Temperature range	-40 to 85 °C	-40 to 85 °C (6) -20to 85 °C (5) -40 to 125 °C (3)
Page size	16 Bytes	32 Bytes
Number of address bytes	1	2
Block protection (BP1,BP0)	yes	yes
I_{CC} stand-by	50 µA at 5.5 V 10 µA at 3 V	10 µA at 5 V 2 µA at 2.5 V 1 µA at 1.8 V
I_{CC} operating	2 mA at 2 MHz	4 mA at 2 or 5 MHz at 5 V 2 mA at 2 MHz at 5 V 2 mA at 1 MHz at 1.8 V
$\overline{W}$ feature (write control)	Hardware write protection of the entire memory array.	Hardware write protection of the BPn protected area, and of the status register
Status register format	1 1 1 1 BP1 BP0 WEL WIP	SRWD XXX BP1 BP0 WEL WIP
Write cycle time (max.)	10 ms	10 ms
Instruction format	0 0 0 X_2 X_1 I_2 I_1 I_0	0 0 0 0 0 I_2 I_1 I_0

The $\overline{W}$ feature

Both the ST95P08 and M95080 support the software protection mode using the BP1 and BP0 status register bits. However, their behaviors are different with the use of the $\overline{W}$ pin.

On the ST95P08, the $\overline{W}$ pin controls the write access to the memory array:

- $\overline{W}$=1: write enabled throughout the entire memory array that is not software write-protected
- $\overline{W}$=0: write disabled throughout the entire memory array

On the M95080, the $\overline{W}$ pin provides hardware write protection of the status register (SR), except for the WIP and WEL bits. When bit 7 (SRWD, the Status Register Write Disable bit) of the status register is '0' (the initial delivery state), it is possible to write to the status register once the WEL (Write Enable Latch) has been set, and regardless of the status of pin $\overline{W}$ (high or low).

Once bit 7 (SRWD) of the status register has been set to '1', the possibility to rewrite the SR depends on the logical level present at pin $\overline{W}$:

- If $\overline{W}$ pin is high, it is possible to write to the status register after setting the WEL (Write Enable Latch).
- If $\overline{W}$ pin is low, any attempt to modify the status register is ignored by the device, even if the WEL is set. Consequently, all the data bytes in the EEPROM area that are protected by the BPn bits of the status register, are also hardware protected against data corruption, and become a Read Only EEPROM area from the microcontroller. This mode is called the Hardware Protected Mode (HPM).

It is possible to enter the Hardware Protected Mode (HPM) by setting the SRWD bit after pulling down the $\overline{W}$ pin, or by pulling down the $\overline{W}$ pin after setting SRWD bit.

The only way to return from the Hardware Protected Mode, once entered, is to pull the $\overline{W}$ pin high.

If the $\overline{W}$ pin is permanently tied high, the Hardware Protected Mode cannot be activated, and the Memory only allows the user to software-protect a part of the memory using the BPn bits of the status register. The protection features of the device are summarized in Table 2.

Table 2. Write Protection Control on the M95080

$\overline{W}$	SRWD Bit	Mode	Status Register	Data Bytes	
				Protected Area	Unprotected Area
1	0	Software Protected (SPM)	Writeable after setting WEL	Software write protected by the BPn of the status register	Writeable after setting the WEL
0	0				
1	1				
0	1	Hardware Protected (HPM)	Hardware write protected	Hardware write protected	Writeable after setting the WEL

Instruction code

Using the two standard address bytes, M95080 instructions take the following format:

0 0 0 0 0 I_2 I_1 I_0

(where I_2, I_1 and I_0 are the instruction bits).

The ST95P08, on the other hand, does not support the standard two byte addressing mode for high densities. Instead, the A8 and A9 address bits are placed beside the instruction bits, according to the following format:

0 0 0 X_2 X_1 I_2 I_1 I_0

(where X_2 and X_1 are respectively A9 and A8 for Read and Write operations, and are Don't Care bits for others).

SOFTWARE RECOGNITION ALGORITHM

This last difference can be used by the application software to differentiate between the two types of memory device. (For a further summary, please see the comparison of the instruction formats of the two devices, in Table 3).

The WREN instruction is used, prior to any write attempt to the memory, to set an internal logical bit of the status register which has to be set to 1 to try a write access to the memory.

As described above in the "instruction format" section, 0001 1101 is a valid WREN instruction code for the ST95P08, and is not a valid WREN instruction for the M95080.

The following algorithm is short, and easy to insert in the MCU code. It is also safe to use, inasmuch that it does not attempt to write to any non volatile bits.

- Master sends the WREN instruction "0001 1110" to the memory (note that b3 and b4 are "1").
- Master sends the RDSR instruction "0000 0101" to the memory (note that b3 and b4 are "0" to avoid the High-Z state on the Q-bus during WEL bit read) and stores the value of the WEL bit in a variable that we will refer to as WEL1.
- Master sends the WRDI instruction "0001 1100" to the memory (note that b3 and b4 are "1").
- Master sends the RDSR instruction "0000 0101" to the memory (again, b3 and b4 are "0" to avoid the High-Z state on the Q-bus during WEL bit read) and stores the value of the WEL bit in a variable that we will refer to as WEL2.
- If (WEL1,WEL2)= (1,0)

  then the EEPROM device is a ST95P08

  else the EEPROM device is an M95080

Table 3. Differences Between the ST95P08 and the M95080 Instruction Formats

Instruction	Description	Instruction Format	
		ST95P08	M95080
WREN	Set Write Enable Latch	000X X110	0000 0110
WRDI	Reset Write Enable Latch	000X X100	0000 0100
RDSR	Read Status Register	000X X101	0000 0101
WRSR	Write Status Register	000X X001	0000 0001
READ	Read Data from Memory Array	000A A011	0000 0011
WRITE	Write Data to Memory Array	000A A010	0000 0010

Notes: 1. A = 1 indicates that the upper page is selected; A = 0 indicates that the lower page is selected
2. X = Don't Care

MICROWIRE EEPROM COMMON I/O OPERATION

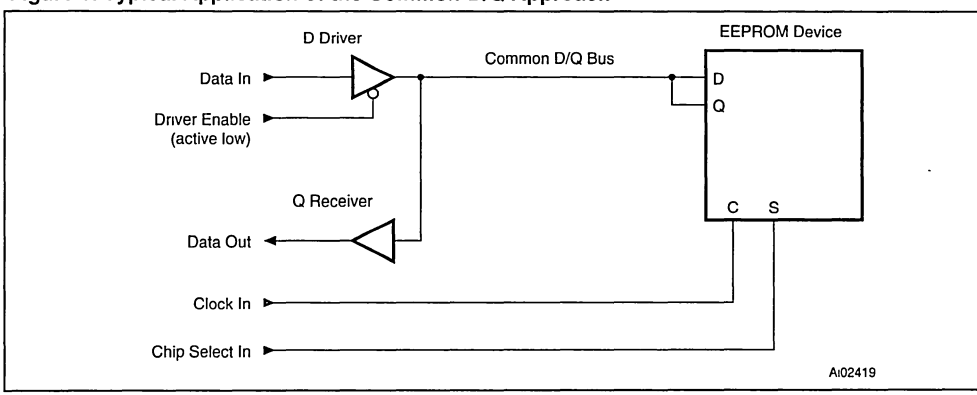
Within STMicroelectronics' broad spectrum of different types of serial access EEPROM product, the MICROWIRE® family is based on a 4-wire interface. The four lines consist of: the Clock Input (C), the Chip Select Input (S), the Serial Data Input (D), and the Serial Data Output (Q).

Some microprocessor chips, such as ST's microcontroller series, include an on-chip Serial Peripheral Interface (SPI). The MICROWIRE interface is ideally suited to use with these devices. However, the MICROWIRE EEPROM devices can also be used with any general purpose microcontroller, provided that care is taken not to allow signal conflicts to result. This document discusses how to avoid such conflicts when tying the D and Q lines together as a single bus.

While commands, addresses or data are being shifted into the D serial input of the EEPROM device, the Q output is held in the high impedance state. It should be possible, therefore, to tie the D and Q pins together to provide a common D/Q bus, as depicted in Figure 1. The device can, indeed, operate correctly in this configuration, provided that appropriate design rules are followed.

The potentially troublesome situations are during commands which activate the Q output (such as READ,WRITE, ERASE, WRAL and ERAL). This document considers these cases, and recommends the most conservative solution to each problem. In order to provide the designer with a safe design guide, all calculations are based on worst case values, as found in the data sheets for these EEPROM devices.

Figure 1. Typical Application of the Common-D/Q Approach

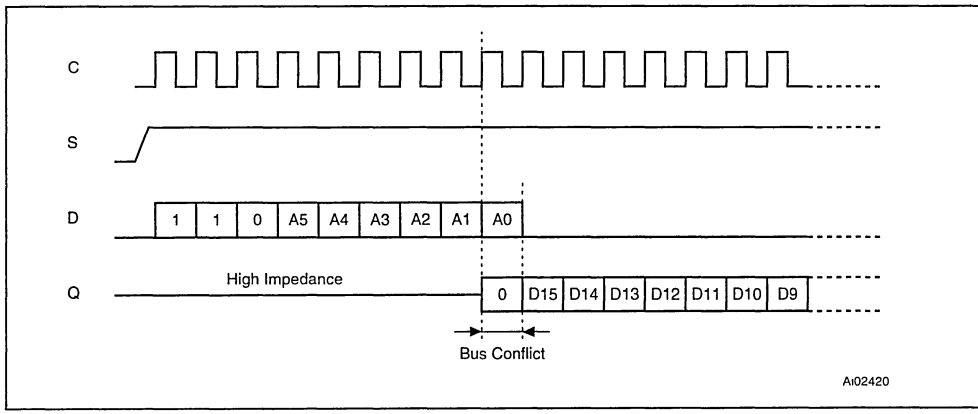


READ INSTRUCTION

The D driver and the Q receiver, in Figure 1, can be discrete logic, or part of a microcontroller I/O port, or any equivalent circuitry. The READ command and its address bits are clocked into the chip, through the D pin, on the rising edges of the C clock. Each bit must be kept valid for a minimum hold time (tDVCH) as specified in the data sheet for the memory device. The device holds the Q pin in the high impedance state during most of the input operation. However, as Figure 2 shows, the Q pin is taken out of this state at the

start of the last address bit (A0) of the instruction (signalled by the rising edge of C), and starts to output the leading zero that precedes the 16-bit data string. The data sheets specify the maximum delay (tCHQL) between the rising edge of C and the leading zero data bit.

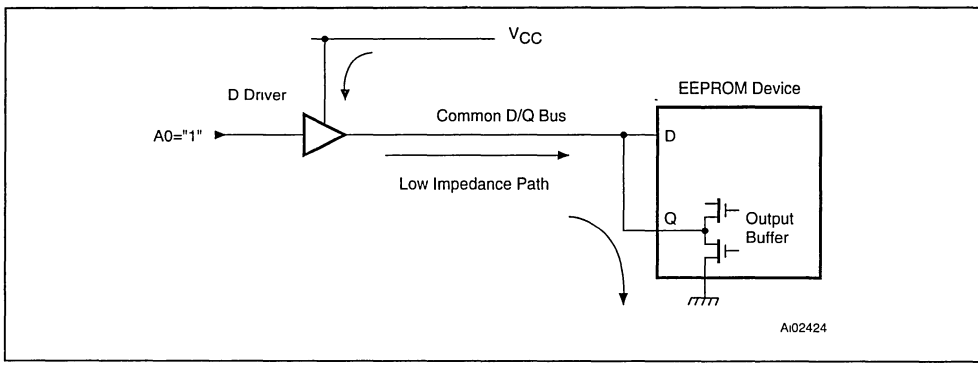
Figure 2. Timing Sequence for a Read Instruction



Since the D driver must remain enabled with the A0 bit for a minimum of tDVCH (the hold time), a bus conflict occurs whenever the A0 bit is a "1", as it would be for all odd addressed registers). The consequences are:

- A low impedance path is created between Vcc and ground through the D driver and the on-chip Q output buffer (as depicted in Figure 3). This short-circuit may produce glitches on the power supply which can disturb all the circuits on the board.
- The logic level on the D/Q bus is not well-defined: the potential divider chain, so created, can end up producing a voltage level anywhere between Vcc and 0 V. Thus access to the odd addressed registers will probably be impossible.

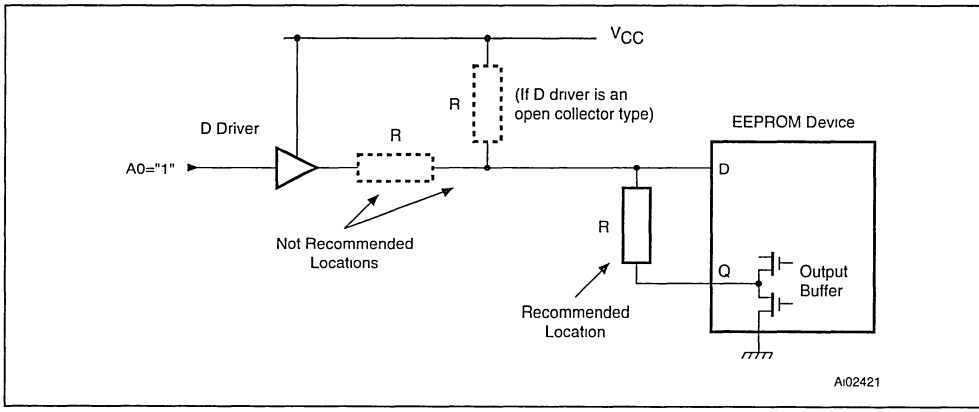
Figure 3. Short-Circuit Created Between Vcc and Ground



This problem can be avoided by inserting a current limiting resistor in the current sink path. Figure 4 shows some possible locations for this resistor. However, the best location is between the Q output and the D/Q bus for the following reasons:

- During the overlap time, only the D driver is providing useful information. The Q driver simply outputs a constant zero. By placing the resistor in this position, the D driver overrides the Q driver at setting the logic level on the D/Q bus, thereby allowing the last address bit to be presented on the D pin for the specified hold time (tDVCH).
- The R resistor slows down the propagation time of the Q output signals on the D/Q bus, as discussed later in this document. In this position, the resistor only slows down the transmission of the 16 bits of data during a READ operation. If R were in series with the D driver, all operations would be slowed down.

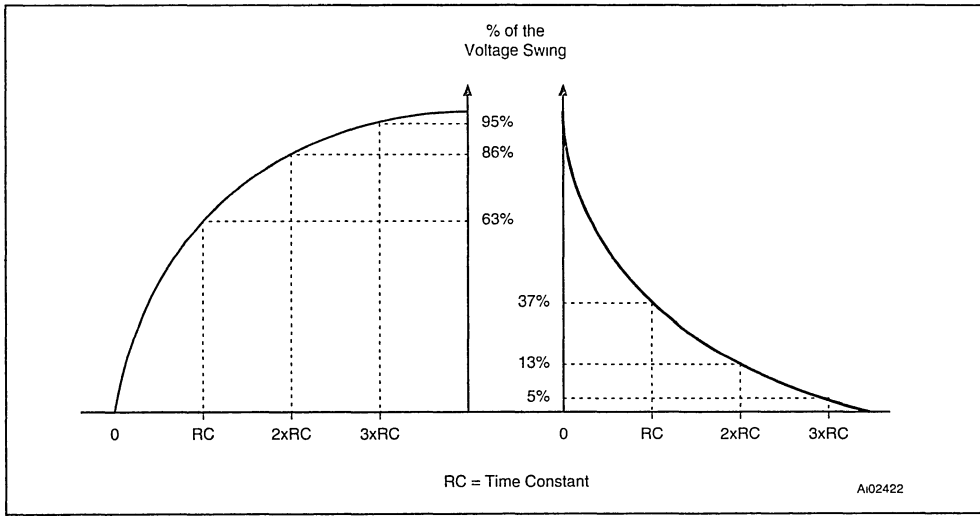
Figure 4. Possible Locations for the Current Limiting Resistor



The R resistor does not have any effect as long as Q is in its high impedance state. During the execution of a READ instruction, R sinks some current from the D driver during the short overlap time. Then the D driver is disabled and Q output takes control of the D/Q bus through the R resistor.

Because of the bus capacitance, C, the signals are distorted, as shown in Figure 5 (on the next page): the rising and falling edges of the Q output are transformed into exponential curves whose shape depends on the time constant RC.

Figure 5. Exponential Charge and Discharge of the Bus Capacitance



As a consequence, the logic level on the D/Q bus is not stable until some time after the rising edge of the C clock. The delay in reading the bus should be at least 3xRC.

In a typical data sheet for a 5 V device, VOH(min) = 2.4 V and VOL(max) = 0.4 V, so giving a voltage swing of 2 V. Using the 3xRC approximation, the D/Q bus levels will be:

– logical "1" = 2.3 V minimum after a delay of 3xRC

– logical "0" = 0.5 V maximum after the C rising edge

It might be necessary to reduce the C clock frequency, when shifting the 16 data bits out from the EEPROM during a READ operation, by an amount that is directly related to the RC time constant of the D/Q bus. All other operations can be performed at the nominal clock rate.

Figures 6, 7, 8 show some experimental examples, plotted from the oscilloscope, with different values of R and C. In the last example, the maximum clock frequency is: 1/(3xRC) = 100 kHz, assuming that the D/Q bus is sampled by the Q receiver circuitry just before the rising edge of the C clock.

Figure 6. Oscilloscope Plot, R = 10 kΩ, C = 100 pF, RC = 1 µs

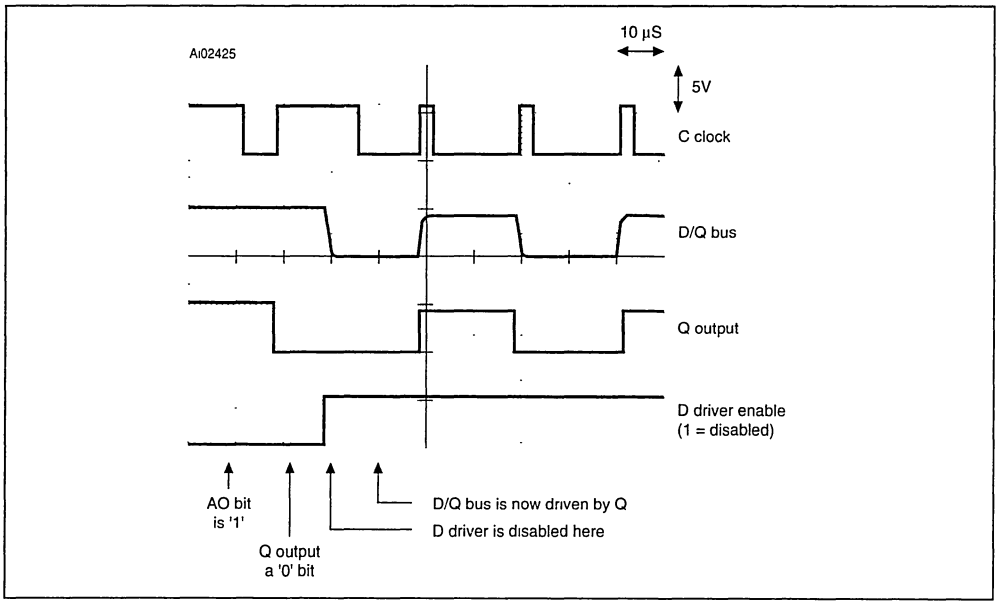


Figure 7. Oscilloscope Plot, R = 5 kΩ, C = 100 pF, RC = 500 ns

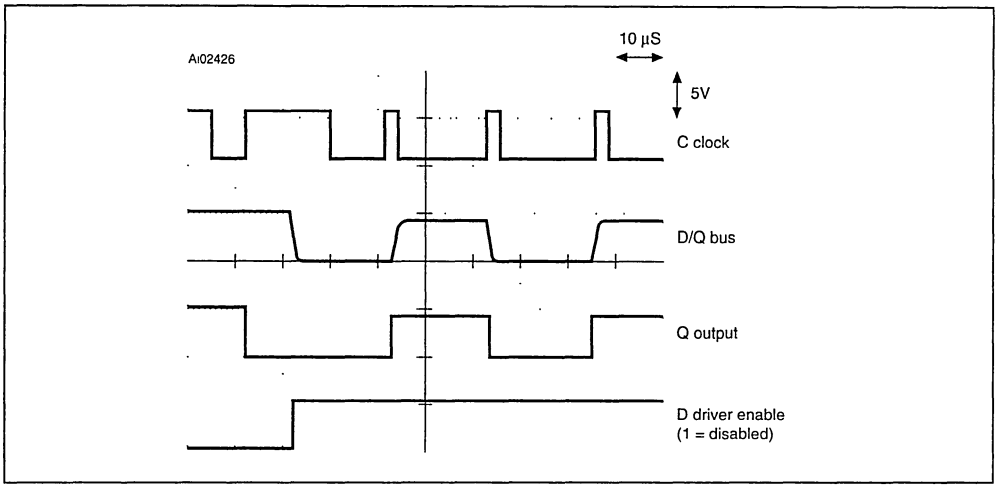
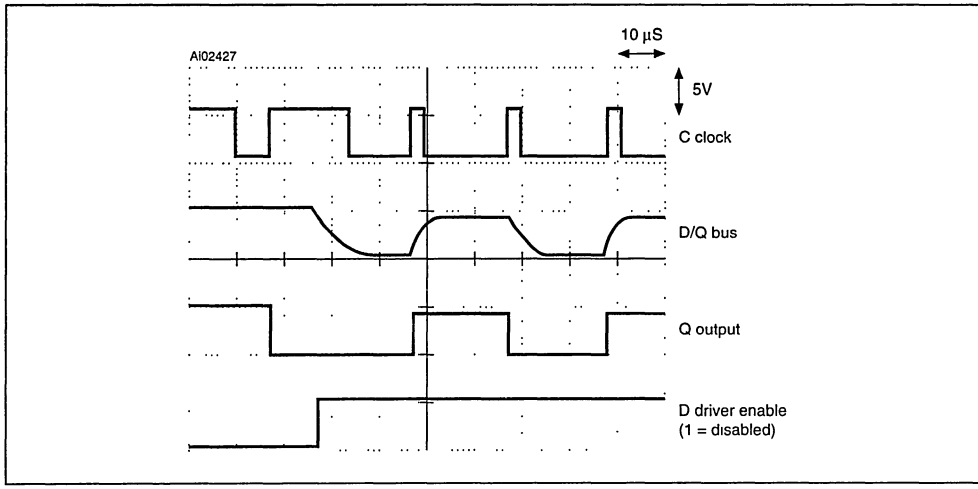


Figure 8. Oscilloscope Plot, R = 10 kΩ, C = 330 pF, RC = 3.3 µs



In order to avoid over reducing the clock frequency, the following techniques can be used to minimize the R and C values:

- To minimize the bus capacitance:
  - the EEPROM device should be position as close as possible to the D-driver/Q-receiver circuitry (the capacitance is proportional to the surface area of the bus line).
  - As few devices as possible should share the D/Q bus (the capacitance is proportional to the number of input gates connected to the bus).
- To minimize the resistor value:
  - Find, from the data sheet, the maximum current that the D driver can source, and divide this value into the value of Vcc.
  - Find the maximum transient current that the power supply can source without glitches being introduced on to the power lines, and divide this value into the value of Vcc.
  - It is up to the designer to decide the best trade-off, based upon his specific application's requirements, but the resistor value should not be less than the higher of the two values calculated above.

INTERFACE WITH CMOS CIRCUITS

The MICROWIRE EEPROM specification makes these devices compatible with TTL input/output levels. When interfacing these devices to CMOS circuits, however, some precautions must be taken, to ensure the correct interpretation of the logic levels.

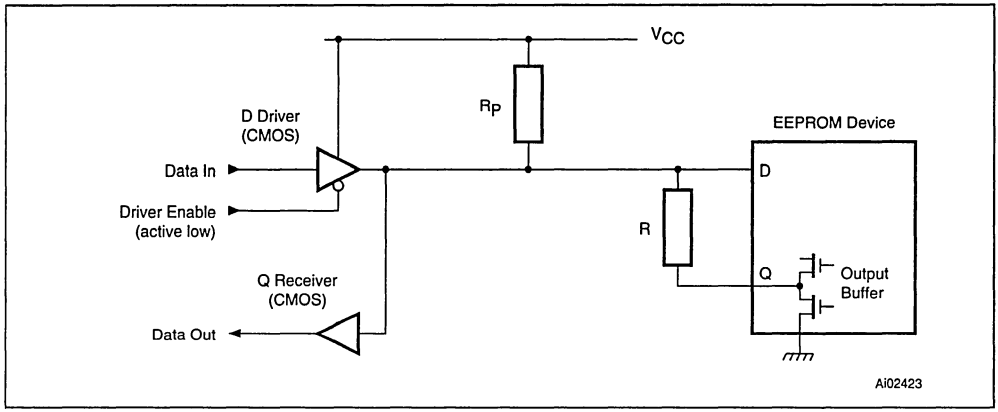
Since the output-high level is close to VCC, and the output-low level is close to 0 V, there are no difficulties in driving the D, S and C inputs of the EEPROM devices.

For the Q output, though, the minimum output-high level is specified as being 2.4 V, which is lower than the minimum input-high level of CMOS (3.5 V for Vcc = 5 V). A common practice is to connect a pull-up resistor, Rp, between the Q output and Vcc.

This solution works well when D and Q are separate. However, it raises some difficulties when D and Q are tied together.

When the Q output is at a "zero" level (VOL= 0.4 V), during the overlap period, the R and Rp resistors form a potential divider chain, as shown in Figure 9. Rp must have a resistance greater than 5 times that of R. This means that the "zero" level on the D/Q bus is: 0.4 V + (5 V -0.4 V) x R / (R + Rp) = 1.17 V. Although this value is 330 mV below the 1.5 V maximum input-low level for CMOS, it does mean losing the wide noise margin that is traditionally associated with the CMOS specification.

Figure 9. D/Q Bus Configuration with Pull-up Resistor (Rp)



For a high to low transition, the Q on-chip output buffer has to discharge the bus capacitance through the R resistor and to sink some current from Vcc through the Rp resistor. The new time constant, when compared to that calculated earlier in this document, is reduced by 17%, because of the parallel combination of R and Rp. However, the steady low level is not 0.4 V, as had been assumed for TTL levels, but 1.17 V, as calculated above for Rp = 5xR. Despite this smaller time constant, the voltage swing between high and low is greater in this case, as described later in this document, so it is advisable to keep the same delay (3xRC) between the C clock rising edge and the first sampling of the data line.

A greater problem is faced during the low to high transition, though. At first, the bus capacitance is charged by the Q output through R, and from the Vcc power supply via Rp, again leading to a time constant for Rp connected in parallel with R. But once the D/Q bus reaches the Q output voltage level, the Q on-chip buffer automatically turns off, and the Rp resistor remains the only contributor to the charge of the bus capacitance. This results in a much higher time constant: RpxC =5xRC.

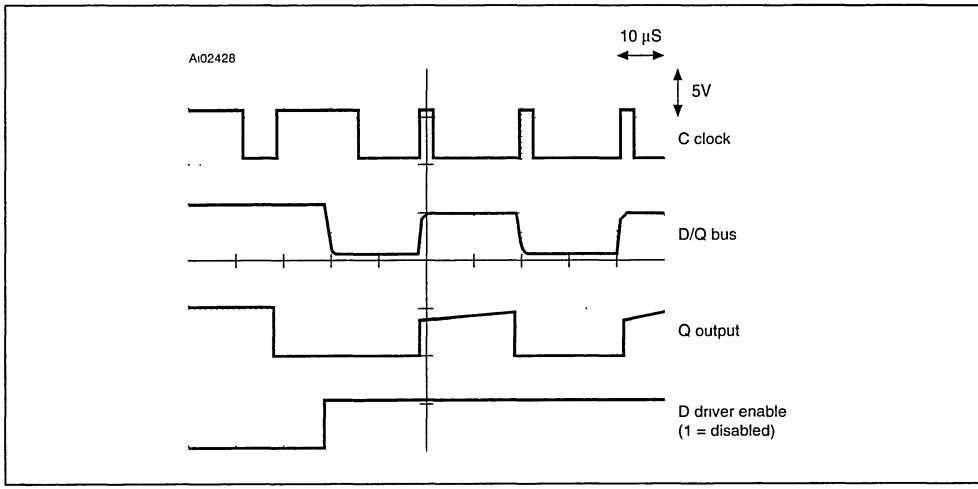
For the worst case output-high level for Q (VOH= 2.4 V), combined with the minimum input-high level for CMOS, the charging delay, after the Q driver cuts out, needs to be at least 0.55xRpC: that is, 2.75xRC. This is still assuming Vcc = 5 V, and allowing for a noise margin of 300 or 400 mV.

As a result, the minimum delay between the rising edge of C and the sampling of the D/Q bus should be 2 or 3 times longer than the one we have found for the TTL levels (without Rp), and the clock frequency must be reduced accordingly. (A typical oscilloscope plot is shown in Figure 10).

It is possible to avoid this situation by using a TTL-compatible CMOS device as the Q receiver circuit, and thereby to remove the need for the Rp resistor. Suitable devices include:

- members of the 74HCTXXX family
- a CMOS microcontroller that provides an option for "TTL input levels" on its I/O ports, such as the ST9 series.

Figure 10. Oscilloscope Plot, R = 10 kΩ, C = 100 pF, Rp = 50 kΩ

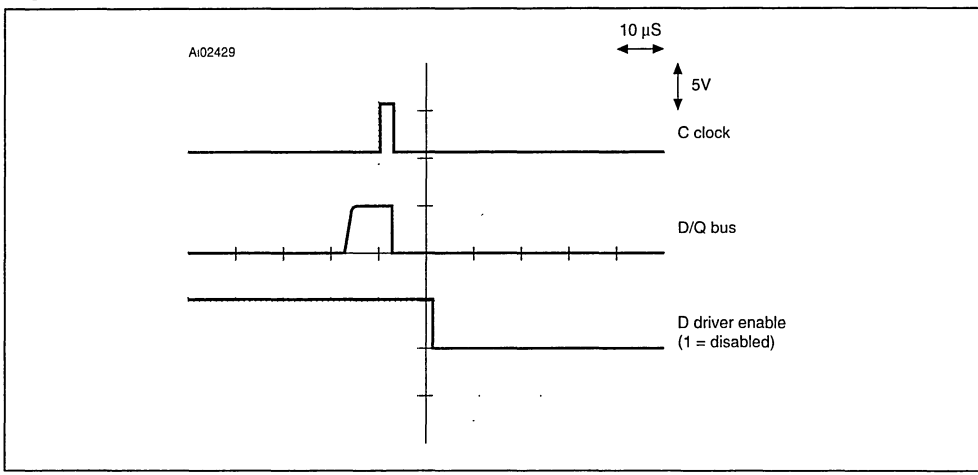


PROGRAMMING MODE: ACKNOWLEDGEMENT OF READY/BUSY STATUS

During a self-timed programming cycle, MICROWIRE EEPROM devices use the Q output to indicate the ready/busy status of the chip. This occurs during the execution of commands such as: WRITE, ERASE, WRAL and ERAL.

The self-timed programming cycle begins with the falling edge of S, at the end of a programming command. The S pin must be kept low for a minimum of tSLSH (as described in the data sheet). The Q output remains in its high impedance state as long as S is low. If S is brought high for clocking-in a new command, Q comes out of its high impedance state, and indicates the Ready/Busy status of the chip (0 = Busy, 1 = Ready).

Figure 11. Acknowledgement of the Ready/Busy Signal on the Q Output



In applications where D and Q are tied together, this may again create bus conflicts. Therefore, it is recommended that this status signal be cancelled as soon as possible: this can be achieved very simply by applying a single clock pulse on the C input while S is high, as depicted in Figure 11.

The operation is scheduled as follows:

– shift the write command into the chip
– bring S low for the minimum period of tSLSH
– bring S high
– monitor the D/Q bus until a high level (Ready) is detected
– clock C once
– bring S low
– the chip is now ready to accept the next instruction

It should also be noted that, on power-up, the Ready/Busy status be initially in the active state. Therefore, it is recommended to clock C once (with S = 1) prior to the issue of the first command.

IMPROVING ON THE CALCULATIONS IN THIS DOCUMENT

This document has discussed how MICROWIRE devices can be used in a configuration in which the D and Q lines are tied together as a single bus. For safety, and for generality, the worst case and most conservative conditions have been assumed in all calculations.

In particular circumstances, however, it might be possible for the designer to do better than this. In the designer's own particular application, it might be reasonable to rule out some worst-case situations as never occurring, and to adapt the calculations accordingly.

AN1119
APPLICATION NOTE

Correct Power-On and Power-Off for the M93Cxx and M93Sxx

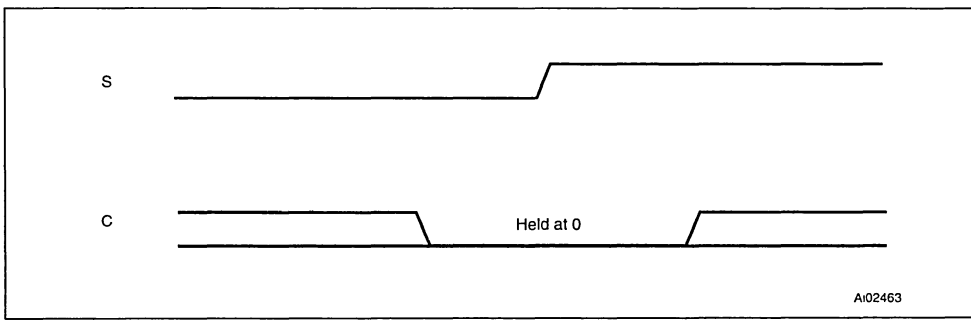
This document has been written for those users who have become used to using the members of the ST93C/CSxx and M93C/Sxx family outside of their specifications.

Table 1. Members of the ST93C/CSxx and M93Cxx Family

Earlier Members	Later members
ST93C06	M93C06
ST93C46, ST93CS46	M93C46, M93S46
ST93C56, ST93CS56	M93C56, M93S56
ST93C66, ST93CS66	M93C66, M93S66
	M93C86, M93S86

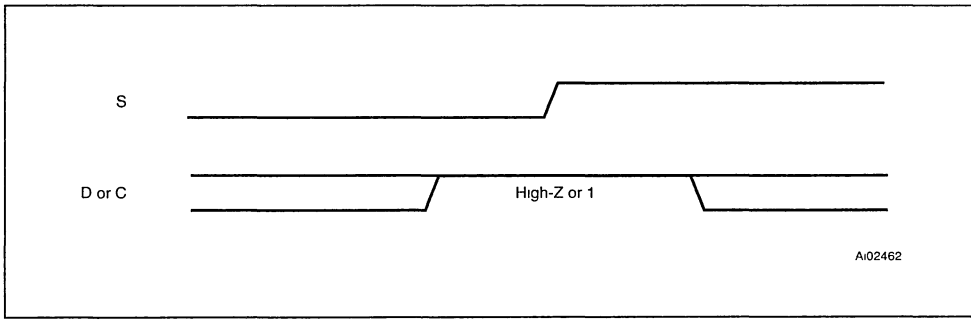
It is very important to use each of these devices only in the way specified in the data sheets. In particular, as shown in Figure 1, it is important for the C input (clock) to be held low whenever there is a rising edge on the S input (chip-select).

Figure 1. Correct Sequence



If a rising edge of the S input is allowed to occur while either the D (data-in) or the C input is high or high-impedance, as shown in Figure 2, the behavior of the device becomes unpredictable.

Figure 2. Hazardous Sequence



MAIN SOURCES OF ERROR: POWER-UP AND MCU RECOVERY START-UP

There are two main causes of users using these devices outside their specifications:

- Uncontrolled inputs during Power-Up and Power-Down
- Uncontrolled inputs during Microcontroller Recovery Start-up Time

Uncontrolled Inputs During Power-Up and Power-Down

During power-up, all three lines (C, D and S) start in their uncharged state, and might well be undriven. There is no control of low-to-high transitions being picked up from noise. Also, there is no guarantee that if drive is later applied simultaneously to the three signals, that the S line will cross the low-to-high threshold before either of the other two.

During power-down, the problem of noise pick-up on undriven lines returns as the main source of hazard.

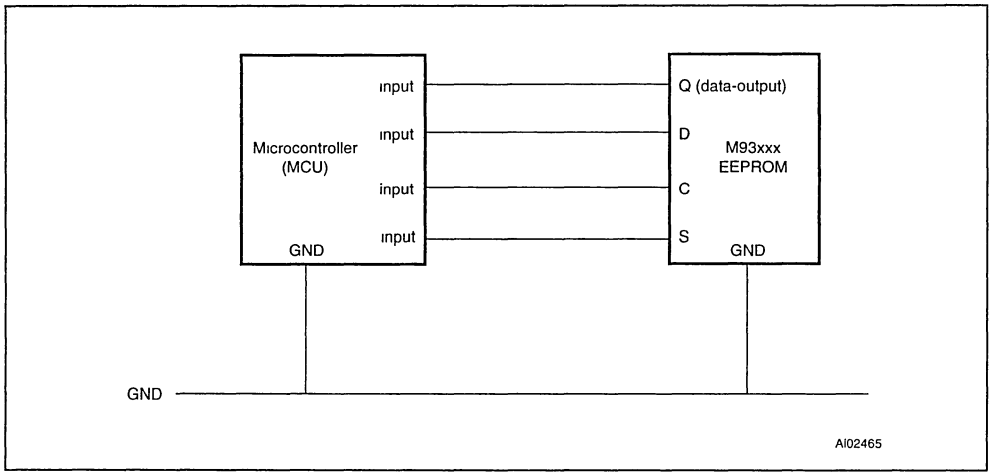
Most microcontrollers will attempt to avoid these problems by going into a Microcontroller Recovery Start-up Mode when the V_{CC} line is outside its specified range. However, as discussed next, this does not completely resolve the problems.

Uncontrolled Inputs During Microcontroller Recovery Start-up Time

During the Microcontroller Recovery Start-up Time, which is typically several milliseconds in duration, some microcontrollers configure all I/O lines in their input mode, as shown in Figure 3. That is, they are all set to their high-impedance state. Under these conditions, with inputs C, D and S all undriven, each line behaves like a small antenna, and can pick up electromagnetic noise radiation. It is not impossible for there to be a rising edge on the S line while C or D is floating high.

Alternatively, some microcontrollers configure all I/O lines as outputs during the Microcontroller Recovery Start-up Time, and drive the lines high. As soon as S crosses the low-to-high threshold, the EEPROM is enabled, and will decode whatever enters its D and C inputs. If these are acting outside the specification, the behavior of the EEPROM becomes unpredictable.

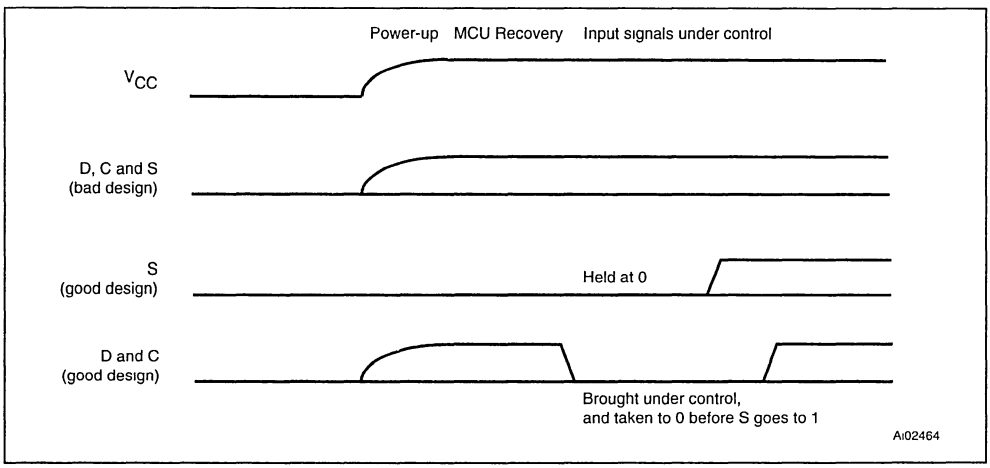
Figure 3. All Signals Being Treated as Inputs



CORRECT POWER-UP AND MICROCONTROLLER RECOVERY

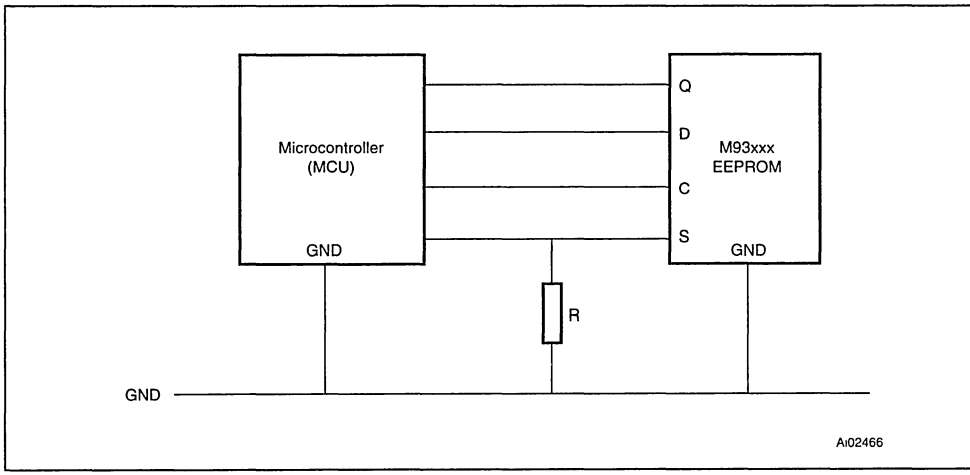
The critical line is the S line. For safety, it can be tied low by a pull-down resistor, so that it does not float high when the input is undriven.

Figure 4. Signal Transients of Bad and Good Design



While input S is held low, the chip is not selected, and it does not matter what signals occur on the other lines (provided that they remain within the specified safe range). It is only necessary, therefore, for the S line to be tied low by a pull-down resistor, as shown in Figure 5, so that it never goes high when it is undriven, as confirmed in Figure 4.

Figure 5. Safe Design with a Pull-Down Resistor on the Chip-Select (S) Line

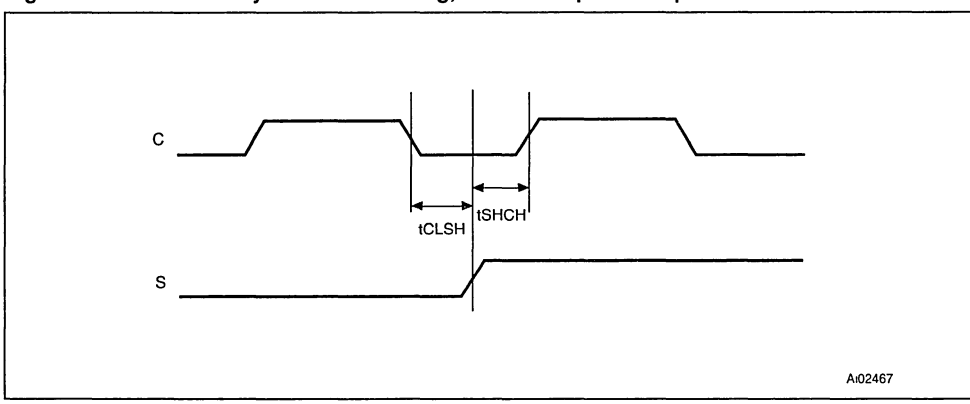


The value for the pull-down resistor can be calculated from the minimum logic '1' input voltage, V_{IH}, that is recognized by the M93xxx, and the maximum source current, I_{OH}, that can be sustained by the microcontroller. The resistance must be greater than the quotient of these two values: $R > V_{IH(M93xxx)}/I_{OH(MCU)}$.

INPUT SIGNALS UNDER CONTROL

Once the application power-up and power-down are properly controlled, it is next important to check that the specification is adhered to for all normal uses of the chip-select signal (as indicated in Figure 4). The data sheet specifies that there is a minimum chip-select set-up time, tCLSH, and a minimum chip-select hold time, tSHCH (as shown in Table 6 of the M93C06/46/56/66/76/86 data sheet). That is, the clock must be held low for at least tCLSH before S is allowed to go from low to high, and to continue to be held low for at least tSHCH after the rising edge of S (as shown in Figure 6, which is an extract from Figure 4 of the M93C06/46/56/66/76/86 data sheet).

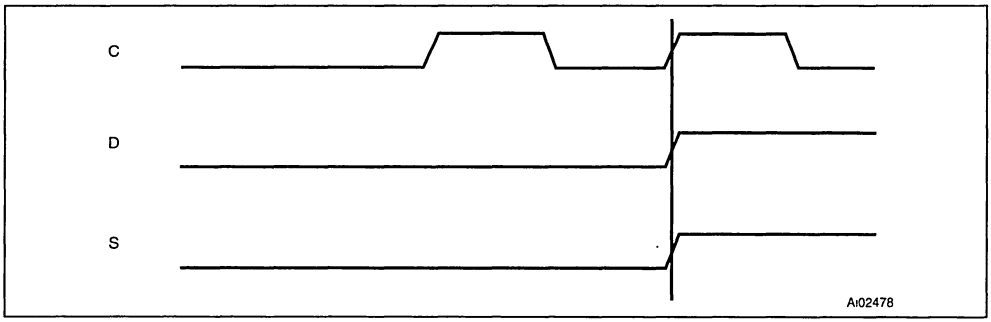
Figure 6. Extract from: Synchronous Timing, Start and Op-Code Input"



INCORRECT CONTROL OF THE INPUT SIGNALS

Figure 7 shows an example of incorrect use of the input signals. The designer has assumed, incorrectly, that it is safe for all three signals (C, D and S) to rise at the same time. However, the interpretation of this event is undefined, and will be decoded randomly as being a {Select} event, or a {Select, D=0} event, or a {Select, D=1} event. The last of these being interpreted, therefore, as a start bit. It is for this reason that this sort of sequence is forbidden, and recognized as being a use of the device outside of its specification.

Figure 7. Incorrect Sequence



FLASH+: The End of the Emulation Compromise

Designers are constantly under pressure to reduce the size of printed circuit boards, and are frequently faced with the EEPROM emulation dilemma: in a system that requires both Flash and EEPROM memory functions, is it necessary to use separate EEPROM and Flash memory chips? In theory the answer is 'no' because with appropriate software part of the Flash memory can be made to emulate an EEPROM. in practice, however, the benefits of this approach are often outweighed by severe performance penalties.

An exciting new memory concept promises to end this dilemma once and for all by allowing EEPROM functionality to be selectively added to a Flash memory array - a major breakthrough as the Flash cell structure is much more cost-effective than conventional EEPROM technology. STMicroelectronics has fully industrialized the concept, and manufactures products that combine 2, 4 or 8 Mbit of Flash memory and 64 or 256 Kbit of EEPROM on the same chip.

The new memory concept is called FLASH+. Using essentially the same process that is used for standard Flash memories, FLASH+ allows a hardware emulation of the EEPROM function to be performed. This uses a double metal process that is only a little more complex than the standard single metal EEPROM process, but allows much smaller cell sizes to be used. However, the benefits of FLASH+ go much further because the EEPROM functionality can be selectively implemented on the die, resulting in a device that combines a conventional Flash memory and a full-featured EEPROM on the same chip.

Before this breakthrough, designers who needed Flash and EEPROM in their systems either had to accept the cost and space over-heads of using two separate devices or had to use a software emulation technique to simulate the EEPROM in a Flash memory.

The software emulation technique was developed to get round the fact that a Flash cell can only be programmed once between sector-erase cycles. If the application stored parameters and variables in fixed Flash locations, the Flash sector would have to be erased every time a variable changed value - and with sector erase times being typically more than one second, this would slow down performance intolerably.

The solution was to write each new parameter value in a fresh Flash location and to maintain a string of address pointers to allow the latest value to be found. When the sector is full, the latest values are copied across to a second sector, and the first sector is erased ready to start the process again.

This approach is very straightforward, but the first software emulations to adopt this approach suffered from the major disadvantage that the microprocessor could not read its program code from the Flash memory while a sector was being erased. Amongst other effects, this gave a worst-case interrupt response time of over a second. Newer Flash architectures such as "Fast Suspend to Read" and "Simultaneous Read/Write" have greatly reduced the interrupt latency problem, but still cannot address the most important disadvantage of software emulation, which is the large and unpredictable access time and the corresponding increase in power consumption.

REMOVING THE LONG AND UNPREDICTABLE ACCESS TIMES

When the processor wants to access a parameter stored in "simulated EEPROM", it has to begin at the initial location and follow the chain of address pointers, tracing through every updated value until it reaches the current one (the one most recently written). Depending on the number of parameters, and the average

number of updates between sector erases, this can take anything from six to more than 8000 times longer than a simple Flash read-cycle. A detailed explanation of this result can be found in Application Note *AN931*.

Of course, for some applications, like a remote data logger that only has to make occasional measurements, the designer might not be too worried about a worst-case access time measured in milliseconds. However, most designers would prefer a fixed access time that is of the same order as that of a standard Flash memory. This is particularly important in applications such as mobile phones where the processor often has to scan through long lists of data such as user directories or call routing preferences, and users will not tolerate noticeable operating delays.

Thanks to FLASH+, there is now a new solution that eliminates the need for compromise. The new M39xxx, the family of FLASH+ products, is a single 3V supply device that appears to the host processor as a two separate memory types, a standard multi-Mbit Flash block and a standard multi-Kbit block of parallel EEPROM. The two memory functions share common address and data buses, and operate concurrently, exactly as if they were implemented as separate Flash and EEPROM chips.

FLASH+ is an excellent example of how ST has leveraged its expertise in memory technologies to create innovative new solutions. With its advanced technology, and with a dedicated Flash fabrication facility ramping up in Italy, the company is greatly strengthening its position in the commodity Flash market.

Another example is shown where the mobile communications industry has been crying out for Flash memories that can read at supply voltages down to 1.8 V (the voltage available from two almost fully discharged batteries). ST has won the race to meet this demanding target. The M29R800 (organized as x8/x16) and M29R008 (organized as x8) are 8 Mbit devices that are hardware and software compatible with AMD, and hardware compatible with Intel products, but allow data to be read with supply voltages ranging from 1.8 V to 3.6 V. This is as opposed to the 2.2 V and 2.7 V minimum supply for corresponding products from other suppliers. Both devices feature fast access times of 80 ns at 2.7 V (180 ns at 1.8 V) and allow a transparent hardware upgrade path from standard 2.7 V devices.

Emulating the Unification of Flash and EEPROM: A Glossary

Many microcontroller applications need both Flash memory and EEPROM. This document summarises the relevant issues and terminology involved in designing efficient systems with the two types of memory.

The subjects are arranged in alphabetical order, in the form of a glossary. Cross-references are shown in **bold face**.

The aim of this document is to highlight the advantages of the M39432: a new memory device that is fabricated by ST using a new dual memory technology called FLASH+™. This device contains 4 Mb of single-voltage Flash memory, and 256 Kb of parallel-access EEPROM, fabricated together on a single chip.

ACCESS TIME

The access time depends on the value of Vcc. Presently, the M39432 is available with a voltage range of 3.0 V to 3.6 V, and an access time of 120 ns at Vcc = 3.0 V. Later versions of the M39432 will have a voltage range of 2.7 to 3.6 V, and an expected access time of 150 ns at 2.7 V.

APPLICATIONS

With FLASH+, dual memories (one Flash memory and one EEPROM) can be fabricated together, thereby reducing the number of memory packages on the PCB, and also reducing the system **Power Consumption**. The technology is, therefore, ideally suited for use in the portable applications market, notably for:

- mobile telephones
- cordless telephones
- electronic notebooks
- hand held meters
- electronic personal assistants
- portable PCs with very long periods away from the mains.

CONCURRENT OPERATION

Write and erase operations in the EEPROM area are managed internally. Although this requires a few milliseconds, the Flash memory remains accessible during this time. In particular, instruction fetches from the Flash memory can continue uninterrupted while the EEPROM area is still updating itself.

EMULATION OF EEPROM

There are three main techniques, as described more fully in *AN931*, for emulating EEPROM in an area of flash memory.

The first method is to use a single bank of flash memory, and to write software that traps addresses aimed at some of the memory sectors, and makes them behave like EEPROM memory. This **External Software Emulation of EEPROM (ESE)** technique, though, suffers from a number of disadvantages. At run-time, accesses to the memory are slowed down enormously by the need to execute the emulation software. The development-time, too, is greatly extended by the need to fine-tune the application software to work with the emulation software.

The second method is to use a device with two banks of flash memory: one to be accessed as flash memory, the other to be accessed as if it were EEPROM. This avoids the need for much, but not all, of the emulation software, and also allows **Read While Write (RWW)** operations, thereby reducing access latency. However, these devices still require some emulation software, for the management of the linked list that allows byte-wise write operations to be emulated in flash memory, and for managing the flash memory sector-erase operation.

The third method is to integrate all of the necessary hardware logic on the chip, and to perform **on-chip hardware emulation of EEPROM (OHE)**. This is the technique that is used in FLASH+ technology, as used for implementing the M39432. The emulated EEPROM, in the Flash memory block, can be accessed as a true EEPROM, with a byte or page write cycle of less than 10 ms.

ERASING THE FLASH MEMORY

The M39432 has a bulk-erase function, to erase the entire 4 Mb of Flash memory in one go. It also has a sector-erase function, to erase selected sectors (of which there are eight, each one 64 Kbytes in size).

EXTERNAL SOFTWARE EMULATION OF EEPROM (ESE)

Flash memory and EEPROM can both be read in a bytewise fashion. Flash memory, though, only allows bytewise writing to bytes that have previously been erased, with the erase operation only being able to be performed in a sectorwise (or devicewise) fashion.

To emulate the bytewise update capability of EEPROM in flash memory, each emulated byte is represented as a linked list within a newly erased sector of flash memory. A second sector is reserved for taking over when the first sector becomes full, and is erased in readiness. Each data byte is accompanied by a two-byte address pointer whose initial value is 'null' (erased). Each write operation involves adding an element on to the end of the linked-list of the byte that is being addressed.

ESE is costly in terms of performance. Each read operation in the emulated EEPROM involves finding the first entry for the byte that is being addressed, and then tracing down through the linked-list until the end of the list is reached. The read operation, therefore, can involve a very long sequence of read cycles. The access time of any one byte is proportional to the number of elements in the linked list, and hence to the number of times that the particular byte has been updated.

ESE is also costly in terms of memory. If the linked lists are to be allowed to grow to an average length of five elements between sector erases, and given that every data byte is accompanied by a two-byte pointer, two 16 Kbyte sectors of flash memory can only emulate an EEPROM of a thirtieth of that capacity (just over 1 Kbyte). A further 16 Kbyte of flash memory is occupied by the emulation software. Moreover, around 4 Kbyte of external RAM must also be provided, for caching some of the emulation software.

IDENTIFIERS

The M39432 supports three different identifiers:

- The manufacturer identifier (1 byte, whose value is 20h)
- The Flash memory block identifier (1 byte, whose value is 0E3h)
- The EEPROM block identifier (64 bytes, whose contents are user defined).

A further 64 byte **One-Time-Programmable Row (OTP)** is provided, as described on page 3.

ON-CHIP HARDWARE EMULATION OF EEPROM (OHE)

ST's FLASH+ technology has been developed expressly to support the on-chip hardware **Emulation of EEPROM**. It is used to implement the functionality of multiple memory: two memory devices, one Flash memory and one EEPROM, within a single package.

ONE-TIME-PROGRAMMABLE ROW (OTP)

The M39432 contains a 64 byte OTP row, distinct from the EEPROM block **Identifier** that is described on page 2. The OTP row can be *written once*, using a dedicated multi-byte instruction (see the application note *AN999*, or Table 4 of the M39432 data sheet). This row can be used for any user-defined purpose (such as for the holding of serial numbers, fabrication parameters, and other tags for identification and traceability). The first write operation (whether it be a byte or page write) to the OTP row will freeze the whole row against any further writes.

PACKAGE

The M39432 is packaged in a TSOP40 (10x20 mm) format. The 40-pin arrangement is forward-compatible with (that is, an extended form of) that of the 32-pin M29F040 Flash memory.

The footprint of the M39432 allows significant savings in circuit board space when compared to the alternative of using two discrete packages. An M39432 in a single TSOP40 occupies about 40% less area of PCB than a standard 4 Mb TSOP32 Flash memory device and a 256 Kb TSOP28 EEPROM device.

POWER CONSUMPTION

The M39432 is particularly well suited for portable equipment applications where the power consumption in both operating and stand-by modes are critical parameters. The stand-by current can be as low as 5 µA over the full voltage and temperature ranges when the device is set in the Deep Power-Down mode.

Because the stand-by current is so small, it is largely negligible in calculations of the typical energy consumption of the system. These calculations are dominated by the size of the operating current. For the M39432, though, the operating current is required only during the processor's read and write cycles. For **ESE**, each read or write operation is composed of a very long sequence of microprocessor read and write cycles (possibly several hundred of them in each sequence). The full operating current is therefore required for shorter periods using the M39432 than it is for the ESE technique, and so its energy consumption is proportionately much lower.

PROGRAMMING THE MEMORY

See **Writing to the device**.

PROTECTION

The whole EEPROM area and each Flash sector can be protected against spurious writes. (See **Software Data Protection (SDP)** and **Sector Protection**).

READY/$\overline{\text{BUSY}}$ (R/$\overline{\text{B}}$)

The Ready/$\overline{\text{Busy}}$ output pin (R/$\overline{\text{B}}$) indicates the status of the EEPROM, and operates completely independently of the status of the Flash memory. It is normally held high, and only goes low to indicate when the EEPROM is performing an internal write operation.

READ WHILE WRITE (RWW)

Read While Write is a type of **Concurrent Operation.** It is a feature of the technique for the **Emulation of EEPROM** using a dual-bank of flash memory.

SOFTWARE DATA PROTECTION (SDP)

The EEPROM area of the M39432 can be protected from inadvertent writes. Two specific multi-byte instructions are provided (see the application note *AN999*, or Table 4 of the M39432 data sheet) for protecting and un-protecting the EEPROM. By being composed of a specific sequence of bytes, the probability is reduced of the instruction being issued inadvertently.

The Flash memory area can also be protected, as described for **Sector Protection**.

SECOND SOURCE

The M39432 is compatible with an other competitor devices announced as available on the market for early 1997.

SECTOR PROTECTION

Each Flash sector of the M39432 can be protected separately against programming or erasure. Flash sector protection is programmed with a specific sequence (see Figure 8 and Table 8 of the M39432 data sheet). Any attempt to program or erase a protected Flash sector will be ignored by the device. Reading the Flash protection status allows the user to know which sectors of the Flash area are protected or not protected. Flash sectors can only be unprotected together by using a specific sequence (see Figure 9 and Table 9 of the M39432 data sheet).

The EEPROM area can also be protected, as described under the **Software Data Protection (SDP)** heading.

TECHNOLOGY

FLASH+ technology is implemented using a standard 0.6 micron Flash memory process.

WRITING TO THE DEVICE

The EEPROM area can be written to in a bytewise or pagewise fashion (64 bytes at a time). In either case, two successive operations are performed (internally and automatically): a byte-erase or a page-erase cycle followed by a byte-write or a page-write cycle. This takes less than 10 ms to complete for a page write, and significantly less for a byte write.

The Flash memory area can only be written in a bytewise fashion. This operation uses a dedicated multi-byte instruction (see the application note *AN999*, or Table 4 of the M39432 data sheet), and takes less than 10 µs for each byte.

FURTHER READING

Table 1 lists all the application notes that describe FLASH+ technology and the M39432 memory device.

Table 1. Bibliography of the Application Notes on FLASH+ Technology

Application Note	Content	Title
AN997	Introduction	M39432: a FLASH+™ Multiple Memory Device
AN931	Greater detail	On-Chip Hardware EEPROM Emulation versus Flash Memory Software Solutions
AN996	Glossary	Emulating the Unification of Flash and EEPROM: a Glossary
AN998	Technology	FLASH+™ Multiple Memory Technology
AN999	Drivers	Software Drivers for the M39432 FLASH+™ Multiple Memory

AN931
APPLICATION NOTE

On-Chip Hardware EEPROM Emulation Versus Flash Memory Software Solutions

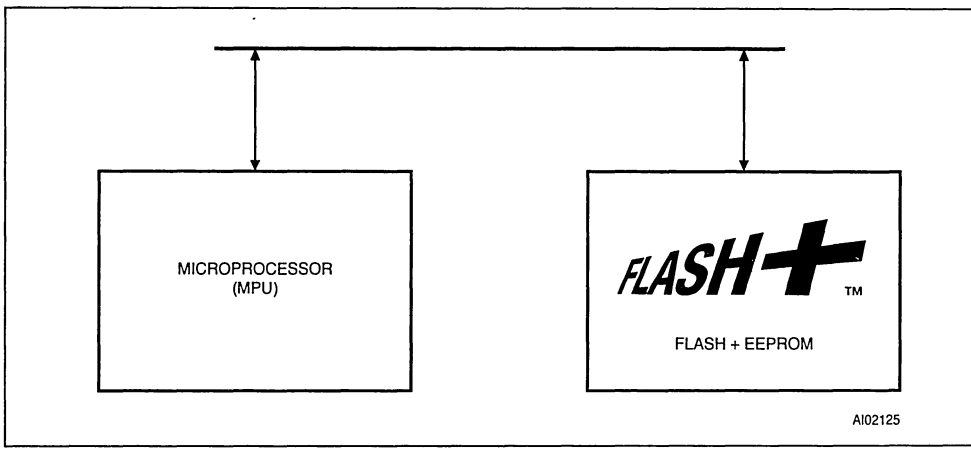
FLASH+ technology, from STMicroelectronics, was developed to allow the advantages of EEPROM and those of Flash memory to be obtained from a single device, fabricated on a single chip. Based on Flash memory technology, the devices integrate all the control logic to provide a large block of Flash memory, and a smaller block which is able to emulate *in hardware* the functionality of EEPROM.

The FLASH+ family is modular, and offers Flash blocks from 1 Mbit to 8 Mbit, and EEPROM blocks from 64 Kbit to 256 Kbit. The first product in this FLASH+ family was the M39432. This features a single supply 4 Mbit Flash memory (512K x 8) combined with a 256 Kbit EEPROM (32K x 8), in a TSOP40 package.

The alternative approach of using software algorithms to emulate the EEPROM in Flash memory (as described on the next page) suffers from considerable disadvantages when compared to the full hardware emulation technique used by FLASH+ devices. The EEPROM block of FLASH+ offers the cell density of Flash memory with the functionality of EEPROM, with the ability to re-write the memory at the byte level, with a write (Erase + Write) operation that takes under 10 ms.

Moreover, with FLASH+, the two memory blocks can be addressed in a concurrent mode, so that the EEPROM block can continue its internal algorithm while the Flash block is being read. This enables parameter data to be updated in the EEPROM concurrently with program execution in the Flash memory, thus offering the same functionality as separate Flash and EEPROM devices. This is an advantage which the software emulation technique is unable to offer.

Figure 1. The FLASH+ Solution



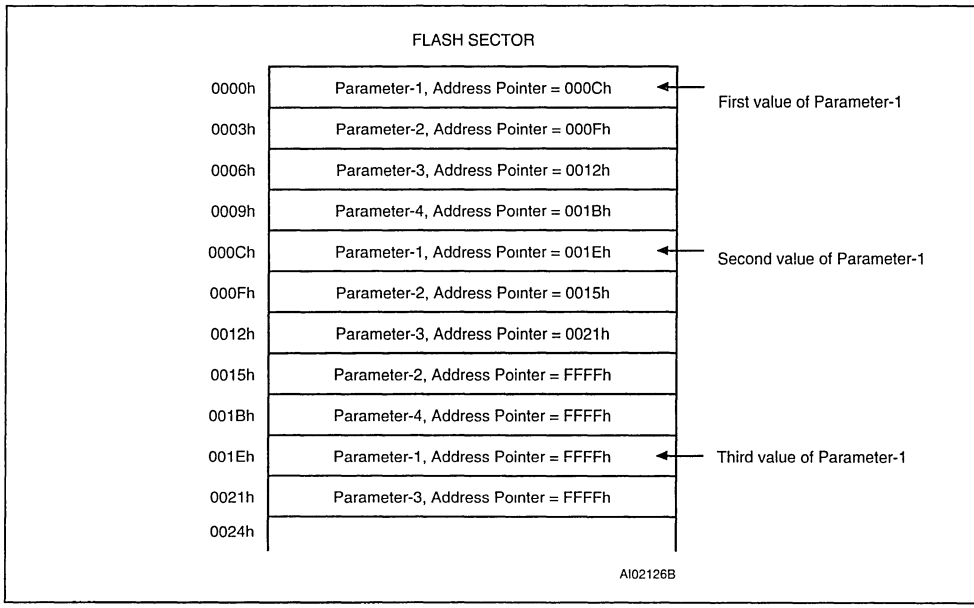
This document compares the FLASH+ family to the alternatives, starting with the technique of emulating a block of EEPROM within a Flash memory device, using external software emulation.

FLASH MEMORY WITH EXTERNAL SOFTWARE EMULATION OF EEPROM

This solution uses one large Flash memory, split logically into two areas: the executable code is stored in one area, and the remaining memory (typically, two sectors) is dedicated to EEPROM emulation.

Flash memory may be written byte-by-byte, but cannot be erased, and so cannot be re-written at the byte level. Flash memory can only be erased by sector, sector sizes in general ranging from 8 KByte up to the whole chip size. The inflexibility of the sector erase limitation can be overcome by writing data sequentially into one sector, and making a 'clean' copy of it in the second sector whenever the first sector becomes full. The byte program and sector erase operation, in the Flash memory, run concurrently, thereby allowing the second sector to take over from the first, while the first is being erased. However, these operations do not run currently with other operations, and so the program code in the Flash memory is not available for reading while these operations are proceeding.

Figure 2. Example of a Flash Memory Sector being used to Emulate EEPROM



In more detail, at first power-up, the two sectors are erased (to FFh since it is Flash memory). Whenever the application needs to update one of its parameters, stored in the emulated EEPROM, the emulation software writes three bytes: a 16 bit pointer to the new value and the new Parameter-1 value itself.

Each parameter, then, is stored in a linked list, with The content of the Flash memory sector is a stack of three byte values or parameter/address pointer pairs, forming a linked list whose last value is the latest update of the parameter.

This is shown in Figure 2. Parameter-1 was first programmed at location 0000h of Sector-1. It was then modified and re-programmed at location 000Ch. Its third, and latest, value was programmed at 001Eh. The emulator knows that the value at location 001Eh is the latest update because the 16-bit address pointer, associated with it, is still blank (the value FFFFh is stored at locations 001Fh and 0020h).

Similarly, Parameter-2 was programmed at first at location 0003h, then at 000Fh and then at 0015h. Parameter-3 was programmed at 0006h, 0012h and 0021h; Parameter-4 was programmed at 0009h and 001Bh.

During the application's life time, the parameters will be updated many times, and Sector-1 of the Flash memory will be soon filled. When this happens, the application software must copy the latest values of each parameter into Sector-2, and to start using Sector-2 instead of Sector-1. Meanwhile, Sector-1 can be erased, so as to be ready for when Sector-2 become filled, and the process needs to be reversed again.

System Requirements

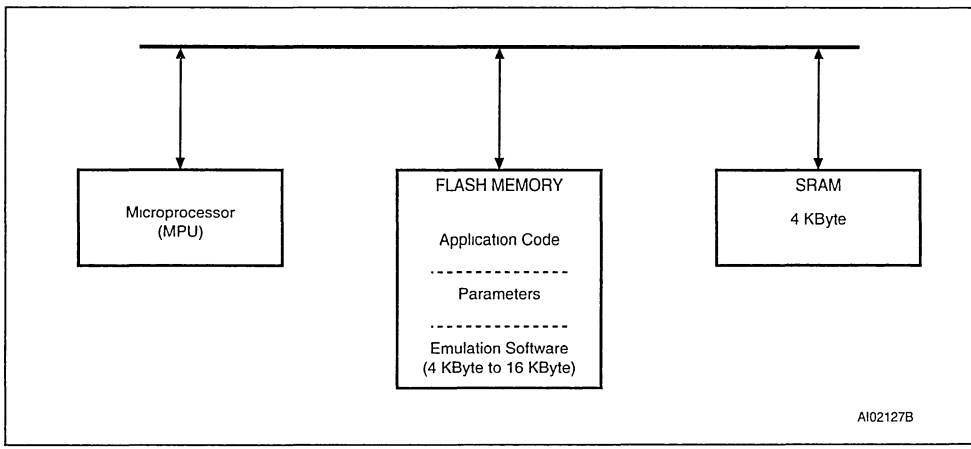
Flash memory cannot be read while another part, even in a completely different sector, is being programmed or erased. This is because the internal algorithms of the Flash memory are busy controlling the program or erase cycle. This means that the software code for the EEPROM emulation has to be stored *outside* the Flash memory itself.

This means the application hardware design must include an additional memory, often a small SRAM, from which to fetch and execute the device drivers for the emulator.

The initial copy of the executable code, of the EEPROM emulation, is stored in the Flash memory. This includes all the code for sequencing the emulation process, including the specific "program a byte in Flash memory" driver. This must be copied to the SRAM before execution.

Typically, as shown in Figure 3, the EEPROM emulation software code is 16 KByte, and the part that needs to be "cached" in the SRAM is 4 KByte.

Figure 3. Memories Required for the External Software Emulation of EEPROM in Flash Memory



HARDWARE VERSUS SOFTWARE EMULATION

EEPROM can be emulated in Flash memory in two ways:

- Using hardware EEPROM emulation based on Flash memory technology, as used in FLASH+ devices
- Using software EEPROM emulation in two Flash memory sectors, with a small external SRAM device

In the comparison that follows, hardware emulation is referred to as OHE (On-chip Hardware Emulation) and software emulation as ESE (External Software Emulation).

ACCESS TIME

The access times for the two different emulations are not the same. Moreover, that for ESE varies with the number of times the parameter has previously been updated.

OHE Access Times

Read and write times for On-chip Hardware Emulation are the same as the access times for standard parallel-access EEPROM. That is, t_{READ} is one MPU cycle, and t_{WRITE} is one MPU cycle plus a write latency of 10 ms during which the EEPROM performs its internal write cycle (and during which the Flash memory may continue to be read).

So the OHE access time is constant, and is not weighted by the number of previous updates of each parameter. The 10 ms latency between byte writes can be significantly ameliorated using the Page Write Mode, which allows up to 64 bytes to be written during a single 10 ms write cycle.

ESE Access Times

For ESE, as shown in Figure 2, each parameter byte is associated with a two byte address pointer in a linked list. Each Read or Write involves a sequence of MPU read cycles to find the end of the relevant parameter list. Thus, for example, the time to read the last value of the Parameter-1 involves the following operations:

```
read the first address pointer at 0001h and 0002h
if this pointer is not FFFFh, then
       read the second pointer at 000Dh and 000Eh
       if this pointer is not FFFFh, then
              read the third pointer at 001Fh and 0020h
              if this pointer is not FFFFh, then
              ...and so on...
else read the latest parameter-1 value
```

From this example the general rule for the access time can be derived:

Time to read last value in list = $(2N+1)$*MPU_read_cycles + N *MPU_conditional_test

where N is the number of times the parameter has been updated. Table 1 summarizes the access times for a few extreme cases of sector configuration.

Table 1. ESE Access Times

	1 EEPROM byte	100 EEPROM bytes	2730 EEPROM bytes[1]
Maximum number of updates possible[2], N	2730	27	1
tREAD (N): read time for one byte	(2*N*+1)*MPU_read_cycles + *N* *MPU_cond_test	(2*N*+1)*MPU_read_cycles + *N* *MPU_cond_test	(2*N*+1)*MPU_read_cycles + *N* *MPU_cond_test
tWRITE (N): write time for one byte	tREAD(N) + 3 write cycles	tREAD(N) + 3 write cycles	tREAD(N) + 3 write cycles
Time to swap last update to new Flash memory sector[3]	tREAD(2730) + 3 write cycles	tREAD(27) + 3 write cycles	tREAD(1) + 3 write cycles

Notes: 1. 2730 is the maximum number of bytes that can be emulated with a Flash memory sector of 8 KBytes.
2. Assuming each byte is updated the same number of times.
3. When swapping data, additional time is required to down-load the executable drivers to the SRAM, and to perform the sector erase.

Table 1 shows the cases for an application with only one parameter, for 100 parameters and for the maximum that can be stored in a Flash memory sector of 8 Kbytes (8 Kbytes/3 bytes per parameter = 2730). If the application MPU can perform a Read or Write in 200 ns, and conditional test in 200 ns, and if the Flash memory byte write time is 10 µs, then we get the following expressions for the access times:

For one parameter, the first parameter update times are as follows:

tREAD = (2*N*+1)*MPU_read_cycles + *N* *MPU_conditional_test = 0.8 µs

tWRITE = (2*N*+1)*MPU_read_cycles + *N* *MPU_conditional_test + 3 *write = 30.8 µs

The 2730th parameter update times are as follows:

tREAD = 1.638 ms

tWRITE = 1.668 ms

After every 2730th update, the application software has to copy the last updated values to the second sector. The sector erase operation takes about 1 second at the beginning of the device's life, but becomes longer with successive erase/write cycles. Consequently, the application will freeze for some seconds after every 2730th update.

If the Flash memory is, instead, used to handle 100 parameters, the first parameter update times are as follows:

tREAD = 0.8 µs

tWRITE = 30.8 µs

The 27th parameter update times are as follows:

tREAD = 16.4 µs

tWRITE = 46.4 µs

In this case, the application software has to copy the last updates to the second sector after only 27 updates. The application freezes for some seconds to erase the Flash memory sector after 27 updates of each parameter.

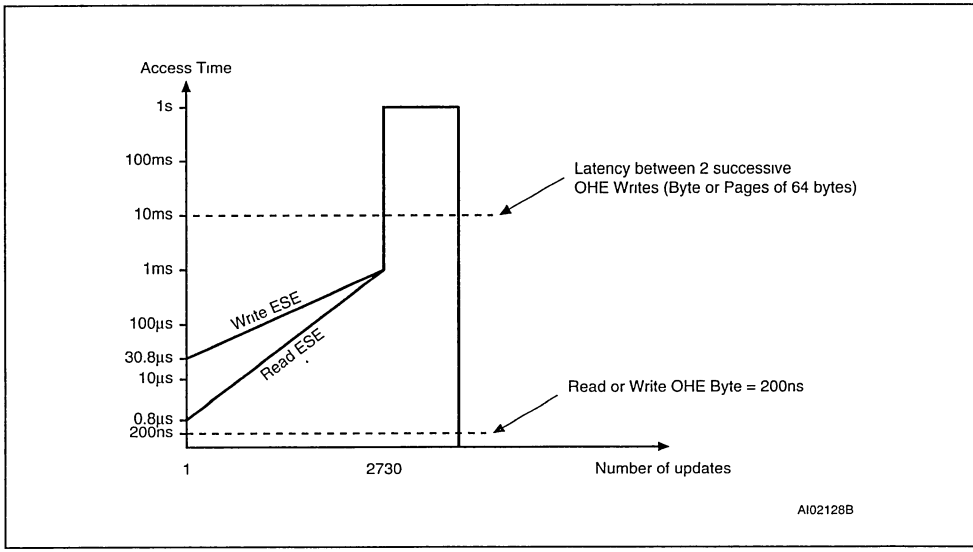
For 2730 parameters the read and write times are absurdly high as each update means using a new Flash memory sector and freezing the application for some seconds to erase the other one.

The read and write times for ESE are always larger than for OHE, with the worst case occurring as the sector approaches being full. The long read access time is a major weakness of the ESE approach, as opposed to the 200 ns read access time (as for parallel access EEPROM) that is offered by OHE.

In addition, the ESE Flash memory sector erase causes the entire application to be frozen for several seconds. The sector erase can be suspended and resumed, but this requires external drivers in the additional SRAM, and prolongs the operation.

Either way, this is still particularly inappropriate in an application where interrupt requests have to be serviced within a very short time. If the interrupt request rate is high, and parameter refresh is also high, it is possible to reach the point where the first emulated EEPROM sector has not completed erasing when the second sector becomes full. The emulation then grinds to a complete standstill.

Figure 4. Access Times plotted against the Number of Updates



POWER CONSUMPTION

The power consumption of any single power supply memory is dependent on three parameters: the I_{CC} operating current, the I_{CC} standby current, and the proportion of time spent in each of these states.

A device needs to be active (I_{CC} = operating current) whenever it is accessed. The access time of ESE is usually several times longer than it is for OHE, for the reasons stated in the previous section. Consequently, the active time for ESE is much larger than for OHE. As the standby current value is much less than the operating current, the ratio of power consumption between OHE and ESE concepts depends mostly on the operating current values and active times.

Table 2 shows that the ESE access time can be between 6 and 8000 times longer than the OHE access time. Thus the ESE technique is considerably more energy consumptive than the OHE technique.

Table 2. Read and Write Times after Several Updates

Number of Updates	1	27	2730
tREAD	0.8 µs	16.4 µs	1.638 ms
tWRITE	30.8 µs	46.4 µs	1.668 ms

MEMORY SIZE FOR EMULATION

Two factors are important when comparing the External Software Emulation and the On-chip Hardware Emulation solutions: the number of parameters to be stored, and the number of updates.

For OHE, the memory size chosen is simply determined by the number of parameters to be stored. The number of updates, that can be made, is determined by the technology. This is able to sustain over 100,000 re-write cycles for the emulated EEPROM.

For ESE, the choice is not so simple. First is the case where the data is updated a few times, say 1 to 10 times. Most applications that modify data only a few times might be expected to accept that they will be frozen every once in a while, for a few seconds, while sector erase is in progress. During the freeze, they will offer limited functionality, with most interrupts disabled, and no real time operations. Table 3 shows the memory size requirements for this case.

Table 3. Memory Size Required for Infrequent Updates

Emulated EEPROM Size		16 Kbit	64 Kbit	256 Kbit
ESE solution	ESE Size[1]	3*2*16 Kbit = **96 Kbit**	3*2*64 Kbit = **384 Kbit**	3*2*256 Kbit = **1.536 Mbit**
	SRAM Size	32 Kbit	32 Kbit	32 Kbit
OHE solution	**OHE Size**	**16 Kbit**	**64 Kbit**	**256 Kbit**
	SRAM Size	none	none	none

Notes: 1. For ESE, one EEPROM byte requires 3 Flash memory bytes, doubled into 2 Flash memory sectors

If the number of updates is higher, in the range of 100 to 1000 times, the application probably needs a more flexible access to the EEPROM. The main concern is to spread the long Flash memory sector erase time over many small Erase Suspend/Resume slots in such a way that this operation does not impact on the application's other real time tasks. If we consider an application that cannot afford to be slowed down by the Erase Suspend/Resume operation, except after each 10^{th} parameter update, then this will have to emulate the EEPROM in a Flash memory sector that is ten times larger than the data size in order to offer fast access time for the first 10 updates. The values are shown in Table 4.

Table 4. Memory Size Required for Frequent Updates, Delay at each 10th Update

Emulated EEPROM Size		16 Kbit	64 Kbit	256 Kbit
ESE solution	ESE Size[1]	10*3*2*16 Kbit = **960 Kbit**	10*3*2**64 Kbit = **3.84 Mbit**	10*3*2*256 Kbit = **15.36 Mbit**
	SRAM Size	32 Kbit	32 Kbit	32 Kbit
OHE solution	**OHE Size**	**16 Kbit**	**64 Kbit**	**256 Kbit**
	SRAM Size	none	none	none

Notes: 1. For ESE, each EEPROM byte needs to be stored 10 times, each time needing 3 Flash memory bytes, doubled into 2 Flash memory sectors.

In the last case where the parameters are updated thousands of times, say 1000 to 100,000, the application is typically one that requires fast data acquisition of at least 100 parameter updates before it can be slowed to erase the Flash memory sector. In this case to Flash memory sector emulating the EEPROM

has to be 100 times larger than the EEPROM memory. This results in huge and impractical Flash memory size requirements (up to 153.6 Mbit to emulate an EEPROM of just 256 Kbit).

In all cases, the OHE solution requires just the straight EEPROM size specified by the application.

EMULATION SOFTWARE DRIVERS

No software drivers are needed for the OHE solution. The EEPROM part of the FLASH+ device is accessed directly in the memory address space, for both Read and Write operations. The ESE solution requires software drivers, which must be stored in the Flash memory and downloaded to an SRAM (of the order of 4 KBytes to 16 KBytes in size).

HARDWARE ENVIRONMENT AND CONCURRENT MODE

The ESE solution cannot access both the Flash memory and the ESE blocks concurrently. A Write to the ESE has to be controlled by software running outside the Flash memory in the external SRAM.

The OHE solution, however, allows reading the Flash memory during the internal EEPROM write cycle. It does not require any additional, external memory.

CONCLUSION

When developing new applications, requiring parameter storage, two important issues have to be taken into account: the access time, and the number of parameter updates expected during the application's life. When these two parameters are known, the designer can evaluate the two competing solutions, according to the concerns summarized in Table 5. The ESE solution will be found to be suitable only for those applications where the software development costs can be spread over a large volume production, where the updates are small (less than 100) and occasional freezing of the application for one or more seconds is acceptable. The OHE solution has none of these restrictions, and can be the ideal solution for all types of application.

Table 5. Summary of the ESE and OHE Solutions

	ESE Technique	OHE Technique
Read access time	Increases in proportion to the number of updates	Fixed, one MPU read cycle
Write time	30 µs in addition to the read access time	10 ms for between 1 and 64 bytes
Energy consumption	$V_{CC}*I_{CC}*t_{ESE}$ (where $6*t_{OHE} < t_{ESE} < 8000*t_{OHE}$)	$V_{CC}*I_{CC}*t_{OHE}$
Memory size	Flash memory at least 6 times larger than EEPROM that is being emulated	Equal to EEPROM size
Software drivers	Flash memory around 16 KBytes + SRAM around 4 KBytes	None
Additional hardware requirements	SRAM of around 4 KBytes	None

AN997
APPLICATION NOTE

M39432: a FLASH+™ Multiple Memory Device

The new FLASH+ technology, from ST, allows Flash memory and EEPROM to be fabricated together on a single die. Significant cost, speed and power consumption advantages are gained over designs that previously used two separate memories, or that previously used software to emulate the effect of having the two types of memory in a single package. This document briefly considers some of these alternative techniques, and highlights the advantages of the FLASH+ technology solution, as used in the M39432 product.

ADVANTAGES AND DISADVANTAGES OF EACH TYPE OF MEMORY

Electronic memory is usually classified under two main headings: *volatile* (losing its contents when the power supply is removed), or *non-volatile* (retaining its contents even when disconnected from an external power supply). Non-volatile memory can be further subdivided into the following technology families:

- ROM (read only, not erasable, mask programmable at time of manufacture)
- EPROM (bytewise electrically programmable, devicewise UV erasable or not erasable)
- Flash memory (bytewise electrically programmable, blockwise electrically erasable)
- EEPROM (bytewise electrically re-programmable, bytewise electrically erasable)

The key advantages and disadvantages of each family are summarized in Table 1. In general, the cell size increases as the inconvenience of erasing is decreased. Since the chip size depends on the cell size, the cost of the memory is proportional to its ease of erasure. Choosing the most appropriate compromise for the application becomes an important design decision within any project.

Table 1. Key Advantages and Disadvantages of Each Family of Non-volatile Memory

Memory Type	Advantages	Disadvantages
ROM	Very small cell size	Cannot be modified except at high cost (a new mask set)
EPROM	Small cell size	The application must be taken out of service for UV erase
FLASH	Medium cell size; electrical erase	Erase only in blocks (sectors)
EEPROM	Bytewise re-programming	Cell size too large for cost effective megabit memories

APPLICATIONS USING A MICROCONTROLLER CHIP AND ONE EXTERNAL MEMORY TYPE

Most microcontroller systems need at least two types of memory:

- a relatively large amount of program memory that does not need to be changed very often
- a small area of scratch memory, for the temporary storage of transient data.

Many microcontroller systems also need an area of non-volatile memory to be set aside for storing persistent data (data that is changed from time to time, but that must be retained from one power-on period to the next). These three areas of memory can be implemented as summarised in the table on the following page.

Table 2. Suitable Memory Technology for Each of the Different Data Types

Data Type	Suitable Technology
Executable program instructions, and large tables of fixed data	ROM, EPROM or Flash memory
Persistent data	Flash memory or EEPROM
Transient data and cache storage	RAM or register banks within the microcontroller chip itself

The demands on all three areas is growing annually. To take a typical example, such as a digital cellular phone, the current requirements, versus those of the near future, are as follows:

- Flash memory, for the executable program
  - currently: 4 Mb (512 Kx8) with a 5 V power supply
  - required soon: 8 Mb (512 Kx16) with a 3 V power supply
- EEPROM, for storing fabrication parameters, user set-up parameters, tables, directories
  - currently: Parallel, 64 Kb with a 5 V power supply
  - required soon: Serial (to reduce package size), 64 Kb with a 3 V power supply
  - There is already a very large market for low capacity, serial EEPROMs, and the market for larger capacity EEPROMs is growing steadily, with a trend to ever greater capacities. When the I^2C™ bus was first developed, 16 Kb was considered adequate as an upper limit for the address space. However, this limit has long been exceeded by applications in robotics, mobile telephones, test equipment and industrial controllers. Microcontroller applications routinely require 256 Kb EEPROMs, and will soon require 1 Mb and even 4 Mb products. This was, of course, anticipated by the introduction of the extended I^2C bus, allowing addressing up to 4 Mb.
- SRAM, for holding transient data, for use as DSP scratch-pad memory and for storing voice messages
  - currently: 64 Kb, or more, with minimum power consumption, and access times of 100 ns
  - required soon: 256 Kb or 1 Mb, or more, with minimum power consumption, and access times of 70 ns

For a more modestly sized application, one possible arrangement is to use just two chips:

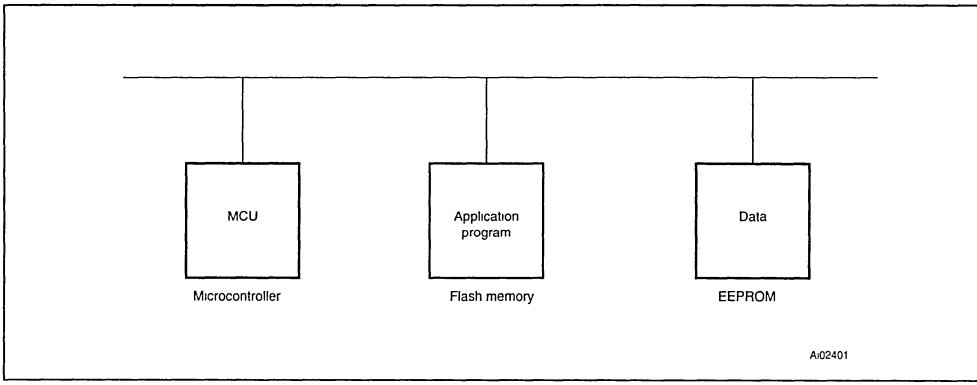
1. one microcontroller (complete with scratch memory areas)
2. one flash memory, to hold the executable code and persistent data.

This arrangement has the advantage of compactness and simplicity, but is not always an acceptable solution. Flash memory allows bytewise writing to bytes that have previously been erased, but the erase operation can only be performed in a sectorwise (or devicewise) fashion. (Sector sizes can be 8 Kbyte, or more, depending on the manufacturer).

APPLICATIONS USING A MICROCONTROLLER CHIP AND TWO EXTERNAL MEMORIES

Due to the widespread market-availability of EEPROM and flash memory, this solution, depicted in Figure 1, is the one that is frequently adopted. The main disadvantage of this approach is the need to have two memory packages, and consequently the relatively large PCB area that is occupied.

Figure 1. Application Based on Separate Flash Memory and EEPROM



COMBINING THE FUNCTIONALITY OF FLASH MEMORY AND EEPROM IN A SINGLE PACKAGE

It would be preferable not to have to include several memory chips on the PCB, but to have the functionality of each of the types of memory combined in a single package. This would, in fact, be advantageous to all microcontroller applications. For those that previously could not justify the cost of having different types of memory in the system, the increased functionality becomes available at little or no extra cost. For applications that previously needed separate integrated circuit packages for each memory type, multi-function memory either offers the opportunity to incorporate more functionality within the same area of PCB, or offers the advantages of reducing the PCB area and chip count, as summarized in the following list:

- miniaturization, due to smaller PCBs
- reduced component purchasing and assembly costs
- faster testing (or more thorough testing)
- increased system reliability
- better use of silicon area through the sharing of common functions
- increased system quality
- lower power consumption.

The appearance of having flash memory and EEPROM, fabricated together on a single chip, can be emulated by either of the following strategies:

1. by fabricating a large EEPROM device, and using a part of it as Flash memory
2. by fabricating a large Flash memory device, and using a part of it as EEPROM.

The first approach is not economically viable: the standard EEPROM process is based on a two-transistor cell, whereas Flash memory uses a single transistor memory cell (as described in Application Note, *AN998*). Since today's applications demand large Flash memory capacities, of 4 Mb or more, this two-fold bloating of the required silicon area is too high a price to pay for the increased functionality.

The second approach is more attractive, and can be undertaken in either of the following ways:

a. emulation in software of the EEPROM area (ESE)

b. emulation in hardware of the EEPROM area.

APPLICATIONS USING EMULATION IN SOFTWARE OF THE EEPROM AREA

This technique takes one large flash memory, and splits it into two functional areas:

i. one area is used as normal flash memory, for holding the executable program

ii. the remaining area (typically two sectors in size) is used for the emulation of the EEPROM.

To emulate the bytewise update capability of EEPROM in flash memory, each emulated byte is represented as a linked list within a newly erased sector of flash memory. A second sector is reserved for taking over when the first sector becomes full, and is erased in readiness. Each data byte is accompanied by a two-byte address pointer whose initial value is 'null' (the erased state). Each write operation involves adding an element on to the end of the linked-list for the byte that is being addressed.

Each read operation in the emulated EEPROM involves finding the first entry for the byte that is being addressed, and then tracing down through the linked-list until the end of the list is reached. The read operation, therefore, can involve a very long sequence of read cycles.

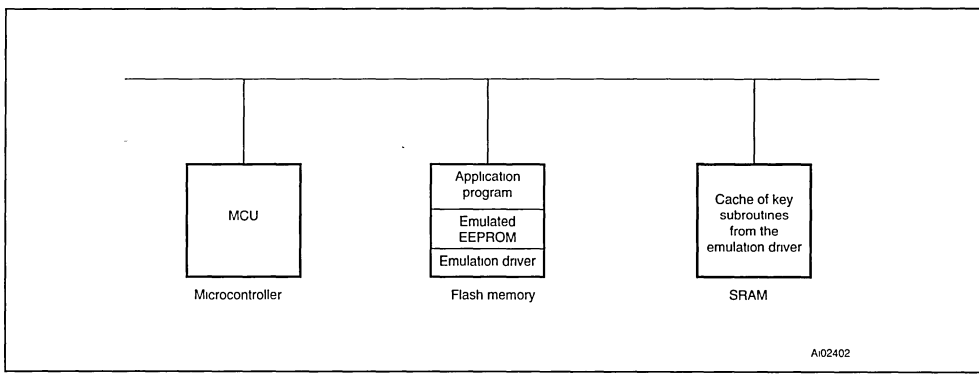
When the sector becomes full, the last element of each linked list (the most recent value of each stored byte) is copied across to the second sector, and that sector takes over as the current state of the emulated EEPROM. The first sector is erased, in readiness for taking over again, once the linked lists have grown too large in the second sector.

In applications where the data are changed frequently, the read access time of the emulated EEPROM can be hundreds of times longer than the read access time of a true EEPROM. This would be a major concern for applications in which the processor has to perform frequent data searches.

Another problem is that flash memory cannot perform simultaneous reads and writes, even to addresses in unrelated sectors. This limitation, of course, applies to all single-ported memory. However, it is particularly significant in this case: every read and write to the emulated sectors of the flash memory involves a long sequence of instruction fetches for the emulator software. These instructions, therefore, need to be stored in another memory device (usually in an external static RAM chip) if the fetching of each one is not to interfere with normal user-access of the flash memory.

Figure 2 depicts the partitioning of the various memory regions. The emulation driver generally takes up 16 Kbytes of the flash memory, but only 1 to 4 Kbytes of this needs to be copied into SRAM at any one time. The emulated EEPROM takes a further two sectors from the flash memory, leaving the remainder available for use as normal flash memory (for the application program, for example).

Figure 2. Application Based on a Single Bank of Flash Memory



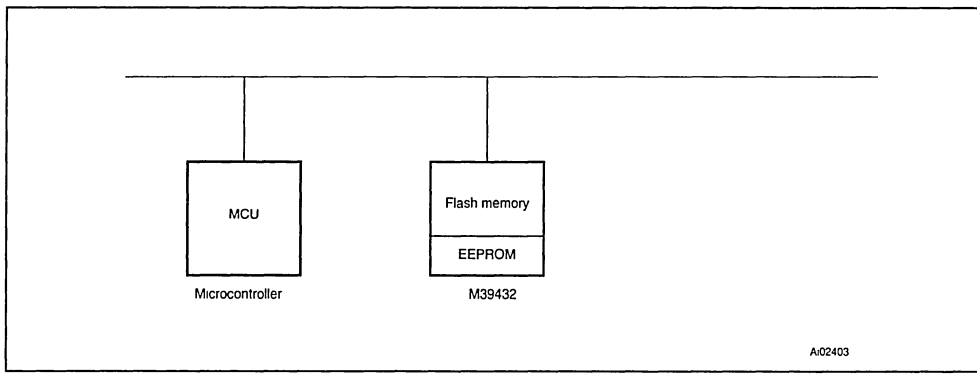
The drawbacks of the ESE approach include:

1. extra software complexity, caused by the emulation software
2. the need for a data buffer for the sector that is being changed
3. the long write time
4. all other memory operations are suspended, including instruction fetch, during the long write time
5. the need, still, for two types of memory chip to be included on the PCB.

APPLICATIONS USING EMULATION IN HARDWARE OF THE EEPROM AREA

ST's FLASH+ technology provides EEPROM functionality that is emulated using conventional Flash technology. A key benefit is that the host controller can read the Flash memory while an EEPROM write cycle is in progress; the EEPROM block manages its write cycle internally once the host controller has issued the program command.

Figure 3. Application Based on the M39432 Device



FLASH+ offers the power-consumption and footprint advantages of the single memory package solution, along with the speed advantages of the dual memory device solution. It is particularly well suited for use in the portable-applications market, as highlighted by the numbered points that follow.

1. Small footprint:

   FLASH+ brings savings in PCB size, fabrication steps and a consequent improved overall product quality. An M39432 in a single TSOP40 occupies about 40% less PCB area than a standard 4 Mb TSOP32 Flash memory, plus a 256 Kb TSOP28 parallel EEPROM.

   Within the FLASH+ device, the Flash memory and EEPROM blocks share the same data, address and control lines. The only extra overhead is the distinction between $\overline{EF}$ (Enable Flash) and $\overline{EE}$ (Enable EEPROM), and the R/$\overline{B}$ (Ready/$\overline{Busy}$) output (as depicted in the functional block diagram of Figure 4).

   The 40-pin TSOP40 arrangement (as shown in Figure 5) is forward-compatible with (that is, an extended form of) the 32-pin M29W040 Flash memory. Pins 3 to 18 and 23 to 38 correspond exactly with the pins of the M29W040 device.

2. Low power consumption:

   There is a single supply voltage, across the Vcc and Vss pins. The stand-by current can be as low as 5 µA, over the full voltage and temperature ranges, when the device is in its Deep-Power-Down mode.

Though much higher than this, the full operating current is required only during processor read and write cycles. This gives the FLASH+ device a much lower power consumption than is possible with the ESE technique: under ESE, each read or write cycle is composed of a sequence of microprocessor read and write cycles (often, several hundreds of them), the full operating current is required for longer periods than it is for the FLASH+ device.

3. High speed:

   When the application is running, the processor fetches executable instructions from the Flash memory, and data from the EEPROM, occasionally writing data to the EEPROM. The EEPROM region of the FLASH+ device can be read or written a byte at a time, or a 64-byte page at a time.

   Although writing to the EEPROM region requires a few milliseconds, the FLASH+ device is accessed as two independent memories. This *concurrent mode* of operation allows the Flash memory to continue to service read requests, such as instruction fetches, even while the EEPROM is in the middle of performing a write or erase operation.

4. Short program development time:

   Using FLASH+, the designer does not need to write EEPROM emulation software, or to fine-tune existent emulation software for the pattern of read, write, erase and interrupt requests that occur in the particular application in hand.

5. Traceability and tagging:

   The M39432 contains a 64 byte OTP row (one-time-programmable). This can be *written once*, using a dedicated multi-byte instruction (see Table 4 of the M39432 data sheet). The OTP row can be used for any user-defined purpose (such as for the holding of serial numbers, fabrication parameters, and other tags for identification and traceability). The first write operation (whether it be a byte or page write) to the OTP row will freeze the whole row against any further writes.

6. Large memory:

   The FLASH+ device is ideally suited to applications that need a large array of executable code and a medium/large array of persistent, but changeable, data.

   The two independent blocks of memory are each organized on an 8-bit bus. For the M39432, for example, one block consists of 4 Mb of Flash memory (arranged as 512 K by 8 bits), and the other of 256 Kb of parallel EEPROM (arranged as 32 K by 8 bits).

FURTHER READING

Table 3 lists the application notes that describe ST's FLASH+ technology and M39432 memory device.

Table 3. Bibliography of the Application Notes on FLASH+ Technology

Application Note	Content	Title
AN997	Introduction	M39432: a FLASH+™ Multiple Memory Device
AN931	Greater detail	On-Chip Hardware EEPROM Emulation versus Flash Memory Software Solutions
AN996	Glossary	Emulating the Unification of Flash and EEPROM: a Glossary
AN998	Technology	FLASH+™ Multiple Memory Technology
AN999	Drivers	Software Drivers for the M39432 FLASH+™ Multiple Memory

SUMMARY OF THE FEATURES OF THE M39432 FLASH+ DEVICE

- Uniform access time: 120 ns (Flash memory and EEPROM)
- Single, uniform supply voltage: 3.0 V to 3.6 V (for read, program and erase operations)
- Low stand-by current: 5 µA in deep power-down
- Automatic stand-by and deep power-down modes
- Device-type and memory-type identifier
- Write, program and erase status bits
- Data retention: 10 years
- Standard memory package: TSOP40 (10 x 20 mm)
- Extended temperature range: -40 °C to +85 °C

FLASH MEMORY BLOCK (IDENTICAL TO THE M29W040 FLASH MEMORY)

Programming time: 10 ms per byte

Flash sector erase

- Erase time: 1.5 seconds per sector
- 8 Sectors of 64 Kbytes each
- Sector protection
- Multi-sector erase
- Erase suspend and resume

10,000 Program/Erase cycles per sector

EEPROM BLOCK

- 512 pages of 64 bytes
- Additional 64 byte one-time-programmable (OTP) page

Writing features

- 64 byte page-write or single byte-write: 10 ms (maximum)
- Ready/$\overline{\text{Busy}}$ output pin
- Software data protection

100,000 write cycles

Figure 4. Functional Block Diagram

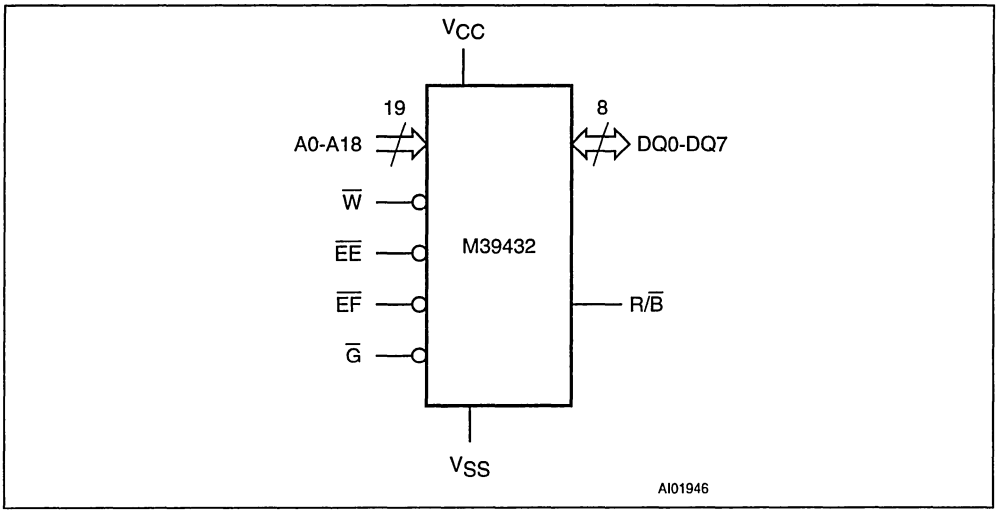
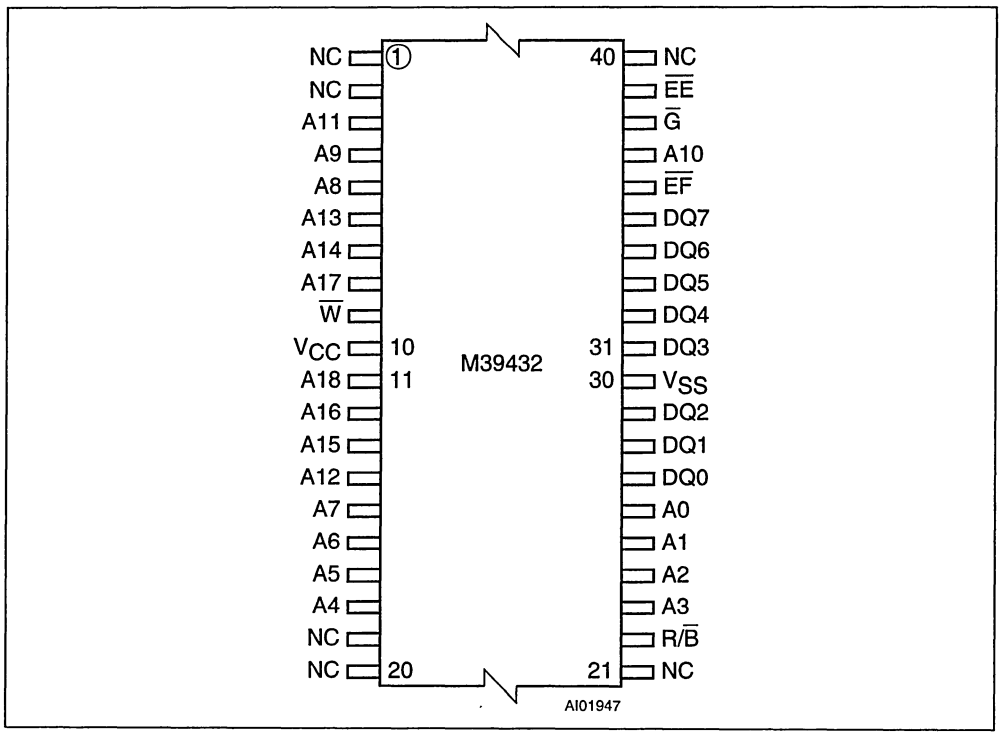


Figure 5. M39432 TSOP40 Pin-out



AN998
APPLICATION NOTE

FLASH+™ Multiple Memory Technology

EPROM, Flash and EEPROM devices all use the same basic floating-gate mechanism to store data, but they use different techniques for reading and writing. This application note discusses the similarities and differences between these technologies, and introduces ST's new FLASH+ multiple memory technology.

In each technology mentioned above, the memory cell consists of an MOS transistor with two gates:

- a control gate that is connected to the read/write control circuitry
- a floating-gate (located between the control gate and the MOSFET channel) that is completely surrounded by an insulating layer of silicon dioxide.

Because the floating-gate is very close to the MOSFET channel, even a small electrical charge on it has a readily detectable effect on the threshold voltage of the transistor. This mechanism is usually used to store a single bit, which is read by comparing the present threshold voltage with a reference value. (With more sophisticated read/write techniques it is possible to distinguish between more than two charge states, thus allowing two or more bits to be represented on each floating-gate.)

Several techniques are available for moving electrons to and from the electrically isolated floating-gate:

1. Channel Hot Electron injection (CHE)
2. High energy light rays
3. Electron tunnelling

The first method is used in EPROM and flash memory devices, for charging the floating gate. The MOSFET channel is filled with high energy electrons by applying relatively high voltages to the control gate and the drain. Some of these "hot" electrons have sufficient energy to cross the potential barrier between the channel and the floating-gate. When the high voltages are removed, these electrons remain trapped on the floating-gate.

In EPROM devices, the discharging of the floating-gates is achieved in parallel by flooding the entire memory array with ultra-violet light. The high energy light rays penetrate the chip structure and impart enough energy to the trapped electrons to allow them to escape from the floating-gate. As well as being simple and effective, this method is immune to problems of over-erasure: continuing to expose the gate to UV light, after it has already been discharged, does not discharge it further to some non-operative region.

The third method, used in EEPROM devices, relies on a quantum-mechanical effect called *tunnelling*. A voltage is applied to the source that is sufficient to cause electrons to "tunnel" across the insulating oxide layer. This effect can be used both to charge or discharge the floating-gate, according to the polarity of the applied tunnelling voltage.

For an EPROM device, the thickness of the oxide layer that separates the floating-gate from the source is typically 20 to 25 nm (200 to 250 Angstroms). For EEPROM, though, the number of electrons that can tunnel across in a given time depends on the thickness of the layer and the value of the applied voltage. Consequently, in order to meet realistic voltage-level and erase-time constraints, the insulating layer has to be

very thin, typically 10 to 13 nm (100 to 130 Angstroms). The quality of this oxide layer has a profound effect on the performance and reliability of the device.

Table 1. Summary of Methods for Charging and Discharging the Floating-gate

Technology	Charge	Discharge
EPROM	channel hot electron	ultra-violet light
Flash memory	channel hot electron	tunnelling
EEPROM	tunnelling	tunnelling

From the summary in Table 1, it can be seen that flash memory is programmed like an EPROM and erased like an EEPROM. It therefore inherits many of the performance and reliability limitations of both EPROMs and EEPROMs. On the other hand, flash memory avoids the main disadvantages of both: it has the electrical erasability of EEPROM at a packing density close to that of EPROM. The high packing density is made possible by a compromise in which, unlike EEPROM, flash memory is erased a sector at a time.

This, however, brings its own technological problems. A special erase algorithm is implemented, in hardware, that first writes to all the cells in the sector, to ensure that every floating-gate is fully charged, and then applies a short erase pulse to all of the cells simultaneously. The algorithm tests the state of the cells in the sector, and repeats the erase-test cycle until all of the cells have been erased.

A problem may occur, however, if one cell discharges too quickly. The erase pulse will continue to be applied to it, until all the other cells have been erased, so causing the problem cell not only to be discharged further, but to become increasingly charged at the opposite polarity. Charged with a surfeit of holes (over depleted of electrons) the transistor will be placed in its depletion mode of operation. The problem cell will exhibit a "stuck at" fault. The entire chip will thereby be rendered useless.

This problem can be easily prevented in low density EEPROMs by design techniques that are not feasible in multi-megabit flash devices. The solution is to combine optimized circuit design with a meticulously tuned process that ensures a uniform and tightly controlled distribution of cell characteristics. For example, increasing the thickness of the oxidation around the corners of the floating-gates prevents the occurrence of high, local electric fields that can accelerate discharge. Special test modes and structures can also be built into the devices to assist in process monitoring.

THE NEED FOR MULTI-TYPE MEMORY DEVICES

The reason that all three technologies survive, and continue to be supported, is that they each have their own advantages. EEPROM is the most versatile of the non-volatile memory technologies, but is also the most expensive. Since cells can be erased individually, or on a bytewise basis, each cell must include a switch to enable it to be isolated from its neighbours. There must be as many switches to do this as there are cells in the memory device. The most efficient EEPROM device, therefore, needs a two transistor cell.

EPROM, on the other hand, does not need transistors to isolate the individual bytes during the erase cycle, and so can be implemented with a one transistor cell. EPROM is, therefore, the cheapest of the non-volatile memory technologies discussed here. Large areas of storage that do not need to be changed often are more effectively implemented in EPROM than in EEPROM.

Flash memory attempts to achieve the advantages of both, and the disadvantages of neither. With a single transistor cell, it achieves most of the advantages of EPROM, allowing it to be used for large, unchanging storage, such as for holding the microcontroller's executable program. However, this is made possible by

limiting its erase operation only to whole sectors at a time. Flash memory, therefore, does not quite achieve the flexibility of EEPROM.

For some applications, where the flexibility of EEPROM is required, it is necessary to include two memory chips:

- one for the large executable program
- one for the frequently changing non-volatile data (data that needs to be retained from one power-on period to another, but which can change often during any one power-on period).

To get round this problem, techniques are available that can emulate the flexible behaviour of EEPROM in flash memory, thus allowing a single chip to be used for both types of memory. These techniques are introduced in *AN997*, and analysed in more detail in *AN931*. A glossary for these techniques is available in *AN996*. These application notes, listed in Table 2, are written to highlight the advantages offered by the M39432 memory, implemented in ST's new FLASH+™ technology.

Table 2. Bibliography of the Application Notes on FLASH+ Technology

Application Note	Content	Title
AN997	Introduction	M39432: a FLASH+™ Multiple Memory Device
AN931	Greater detail	On-Chip Hardware EEPROM Emulation versus Flash Memory Software Solutions
AN996	Glossary	Emulating the Unification of Flash and EEPROM: a Glossary
AN998	Technology	FLASH+™ Multiple Memory Technology
AN999	Drivers	Software Drivers for the M39432 FLASH+™ Multiple Memory

FLASH+ TECHNOLOGY

FLASH+ technology uses the same 0.6 micron process that is used for our standard Flash memories. The main difference is the use of a thinner tunnel oxide layer. The result is a "double poly/double metal" process that is a little more complex than the industry standard "double poly/single metal" EEPROM process, but provides significantly greater memory densities. For example, a 1 Mb parallel EEPROM complete with error correction circuitry could be built with a cell size less than that of a 256 Kb serial EEPROM built with the industry standard process.

Because this new technology is so closely related to flash, it has opened up the possibility of integrating both types of memory on a single chip. This, in turn, leads to further efficiency, since much of the support circuitry (such as charge pumps for on-chip generation of the programming voltage, address logic, state machine and I/O buffers) can all be shared.

The M39432 features all of the following on a single chip:

- 4 Mb array of Flash memory, with:
  - sector protection
  - erase suspend/resume features
- 256 Kb array of full-featured EEPROM, with:
  - software data protection
  - 64-byte page-mode
  - enhanced end-of-write detection.

Software Drivers for the M39432 FLASH+™ Multiple Memory

This document describes the primitive software drivers for use with the M39432. (The M39432 is a single-chip memory device containing a 4 Mb block of single-voltage Flash memory, and a 256 Kb block of Parallel EEPROM.) These routines have been developed on an evaluation board that was configured as follows:

- 1 ST10 microcontroller running at 40 MHz (compatible with SIEMENS 80C16X)
- 2 Mb SRAM (256 Kx8) occupying addresses 0H to 03FFFFH
- 1 M39432
  - EEPROM (32 Kx8) occupying addresses 40000H to 47FFFH
  - FLASH (512 Kx8) occupying addresses 80000H to FFFFFH
- 1 asynchronous serial interface for communication with a PC.

Once compiled and linked, the software routines were down-loaded to the static RAM (SRAM) of the evaluation board, via the asynchronous serial interface. A high level language debugger (HLLD) was then run on the processor of the evaluation board.

These routines were written in the C programming language, and can be easily adapted to many other different processor environments.

Most of the routines are extremely simple, but involve multiple operations on the device. For instance, to write a byte of data to the Flash memory area, the byte itself must be preceded by the "PROGRAM BYTE" command (hexadecimal AA,55,A0 written to three specific addresses). For the command to be recognised, the consecutive writes must be within a certain timing window of each other. The time between consecutive writes is called tWHWH, and must be no shorter than 0.2 µs (for physical reasons), and no longer than 80 µs (otherwise the command would be timed-out by an internal timer).

The sections that follow take each of the routines in turn, describing the constraints, and showing the C program solution.

Routine to Read a Byte from the M39432 Device

As indicated above, the EEPROM and Flash memory areas of the M39432 are mapped to distinct areas of the address space. For example:

- EEPROM addresses run from 40000H to 47FFFH
- FLASH addresses run from 80000H to FFFFFH

The Byte-Read operation is performed in the conventional manner, just as it would for a byte at any other address in main memory.

```
function READ(address);
  begin
    READ = *address
  end
```

Routine to Write a Byte to the M39432 Device

Similarly, there is a Write-Byte operation, for sending a byte of data or command to the device.

The write cycle time of the M39432 is guaranteed to be less than 10 ms. Even so, since the microcontroller is capable of executing a large number of instructions in this time, it might be desirable to call a CONTROL function to set internal control flags, thereby registering that a write operation is in progress, and allowing concurrent execution to be planned accordingly.

```
function WRITE(address,byte)
 begin
  *address = byte
  CONTROL ( if implemented )
 end
```

However, it must be emphasised that writing a byte to an address in the EEPROM or Flash memory area does not necessarily lead to the byte being stored at the given location. A central idea of non-volatile memory is that the device may be protected from casual write operations.

The above function is used for sending command bytes to the M39432 device, to put it in a specific mode of operation, as well as for sending data bytes to it, for storage. One of these commands is discussed next: the command for writing a byte in the Flash memory area.

Routine to Program a Single Byte in the Flash Memory Area

To write a single byte to the Flash memory, three command bytes (hexadecimal AA,55,A0) must first be written to three specific addresses. This is then followed by the byte that is to be written to the desired address. A function for doing this appears as follows:

```
function BYTE_WRITE_FLA (address,byte)
 begin
  WRITE (@05555h,AAH)
  WRITE (@02AAAH,55H)
  WRITE (@05555H,A0H)
  WRITE (@address,byte)
  CONTROL ( if implemented )
 end
```

Once the final write operation has been initiated, the Flash memory takes over its own internal management, and will not accept any further operations until the previous one is completed.

Routine to Write a Byte in the EEPROM Area

The writing of a byte in the EEPROM area can be made to resemble the writing of a byte in RAM, or the writing of a byte in Flash memory, depending on the level of protection required. When the software data protection (SDP) mode is disabled, writing a byte into the EEPROM area is simply a matter of executing a single WRITE operation, giving the address of the desired cell within the EEPROM area. The function to do this is shown earlier, but is repeated here for completeness.

```
function WRITE(address,byte)
 begin
  *address = byte
  CONTROL ( if implemented )
 end
```

When the SDP mode is enabled, writing a byte into the EEPROM area resembles the process of programming a byte in the Flash memory area, as shown in the following function:

```
function SDP_BYTE(address,byte)
 begin
  WRITE (@05555H,AAH)
  WRITE (@02AAAH,55H)
  WRITE (@05555H,A0H)
  WRITE (address,byte)
  CONTROL ( if implemented )
 end
```

Routines to Enable and Disable Software Data Protection of the EEPROM Area

The purpose of the software data protection (SDP) mode is to offer some defence against inadvertent writes to the EEPROM area. When the mode is enabled, bytes in the EEPROM area can only be overwritten if the data write is preceded by the appropriate three byte command.

By default, the M39432 is delivered in the unprotected mode. The routine to enable SDP involves sending the (AA,55,A0) command on its own, as shown in the following function:

```
function SDP
 begin
  WRITE (@05555H,AAH)
  WRITE (@02AAAH,55H)
  WRITE (@05555H,A0H)
 end
```

The routine to disable SDP involves sending a six byte command (hexadecimal AA,55,80,AA,55,20) as shown in the following function:

```
function DIS_SDP
 begin
  WRITE (@05555H,AAH)
  WRITE (@02AAAH,55H)
  WRITE (@05555H,80H)
  WRITE (@05555H,AAH)
  WRITE (@02AAAH,55H)
  WRITE (@05555H,20H)
 end
```

Routine to Erase the Whole Flash Memory Area

The execution of the following six specific write operations (hexadecimal AA,55,80,AA,55,10) causes a bulk erase of the whole Flash memory.

```
function BULK
 begin
  WRITE (@05555H,AAH)
  WRITE (@02AAAH,55H)
  WRITE (@05555H,80H)
  WRITE (@05555H,AAH)
  WRITE (@02AAAH,55H)
  WRITE (@05555H,10H)
  CONTROL ( if implemented )
 end
```

Routine to Erase a Sector of the Flash Memory Area

The Flash memory is divided into eight sectors, each one 64 Kbytes in size. These can be erased together, as indicated in the previous section, or independently, as shown in this section. The operation involves the writing of five specific bytes (hexadecimal AA,55,80,AA,55) to put the device into the command mode, followed by a write of the value 30H to any address in each sector that is to be erased. An internal timer in the M39432 allows the device to recognise the end of the sector-erase operation: the device reverts back to normal mode when the last write operation is followed by a period of silence of 80 µs, or more. (The routine to handle the timer control is described in the next section.)

```
function SECTOR_ERASE (sector_address)
 begin
  WRITE (@05555H,AAH)
  WRITE (@02AAAH,55H)
  WRITE (@05555H,80H)
  WRITE (@05555H,AAH)
  WRITE (@02AAAH,55H)
  WRITE (@sector_i_address,30H)
  WRITE (@sector_j_address,30H)
  /* and so on for each sector to be erased */
  CONTROL ( if implemented )
 end
```

Writing B0H at any address in the Flash memory area will suspend the erase operation.

Routing to Handle the Timer Control

The DQ3 status bit, known as the *erase time-out flag*, is reset when a sector-erase operation has been initiated on the device. This can be read, and used, by the CONTROL function:

a. checking that DQ3 is still reset, indicating that the device is still receptive of erase commands (the command 30H, sent to an address in the chosen sector, as described in the previous section)

b. checking that DQ3 has reverted to being set, indicating that the device has finished processing the last erase operation at the end of the SECTOR_ERASE function (as described in the previous section).

An example of the handling of this status bit is given in the following program fragment:

```
begin
  flag_timer= 1
  count= 0
  do
    begin
      read DQ3
      count= count+1
    end
  while (DQ3==0) and (count =< value)
  if count =< value then flag_timer= 0 (sector erase is processed, no more
    sector addresses can be sent)
  else flag_timer remains 1 (memory fail)
  return flag_timer
end
```

Routine to Handle the EEPROM Toggle-bit Control

When a new value has been written to the EEPROM area, there is a minimum time before the memory can accept the next operation. This delay can be hidden by allowing the processor to get on with other useful work, and later to poll the EEPROM to find out if it is still busy. The DQ6 status bit, known as the *toggle flag*, toggles between 0 and 1 on successive reads, until the erase/write cycle is complete. The state of completion, therefore, is indicated when two successive read operations of DQ6 return the same value.

The following program fragment implements the required algorithm:

```
begin
  n_bit= 6
  count6= 0
  flag_toggle= 1
  do
    begin
      first read of DQ6
      second read of DQ6
      count6= count6+1
    end
  while (first read of DQ6 != second read of DQ6) and (count6 =< max)
  if min=<count6=<max then flag_toggle= 0 (byte written OK)
  else flag_toggle= 1 (memory fail)
end
```

The completion of EEPROM erase/write cycles can alternatively be detected by controlling the DQ7 status bit, by a process known as *data polling*, as described next.

Routine to Handle the Data Polling Bit Control of the Flash Memory

The DQ7 status bit, known as the *data polling flag*, is an indicator for the end of byte-program and sector-erase operations in the Flash memory area. Data polling is effective after the fourth W pulse (for programming) or after the sixth W pulse (for erase). It must be performed at the address being programmed or at an address within the Flash sector being erased. When erasing or programming the Flash memory area, or when writing to the EEPROM area, bit DQ7 is held at the complement of the value that the processor wrote to it. Once the operation is completed, the bit is complemented again, back to its correct value.

In the following program fragment, the DQ5 status bit, known as the error flag, is also checked. A logic level '1' on this bit indicates a failure of the byte-programming, sector-erase or a bulk-erase operation. Any sector, in which an error of this type has occurred, must not be used any more. Other sectors may continue to be used.

```
begin
  flag_data_polling=1
  last_bit_dq7=last_byte&0x80 (bit 7 to be written in FLASH)
  do
    begin
      read DQ7
      read DQ5
    end
  while (DQ7!=last_bit_dq7) and (error_bit_dq5=0)
  if error_bit_DQ5=0 then flag_data_polling=0
  else
    begin
      read DQ7
      if data_polling_dq7=last_bit_dq7
      then flag_data_polling=0
      else
        begin
          flag_toggle=1
          RESET
        end
    end
  return flag_data_polling
end
```

When set, the error bit must be reset with the *reset* or *short reset* instruction (as described in the next section).

Routine to Reset the Flash Memory

This function must be run each time an error is detected on the error bit of the status register. It involves the writing of three specific bytes (hexadecimal AA,55,F0). A minimum delay of 5 µs is required before the next operation can be performed on the memory.

```
void RST
  begin
    WRITE (@05555H,AAH)
    WRITE (@02AAAH,55H)
    WRITE (address,F0)
    wait 5us
  end
```

Writing F0H at any address in the Flash memory area, known as a *short reset*, is equivalent to the above sequence.

```
void SHORT_RST
  begin
    WRITE (address,F0)
    wait 5us
  end
```

FURTHER READING

Table 1 lists the application notes that introduce ST's FLASH+ technology and the M39432 device.

Table 1. Bibliography of the Application Notes on FLASH+ Technology

Application Note	Content	Title
AN997	Introduction	M39432: a FLASH+™ Multiple Memory Device
AN931	Greater detail	On-Chip Hardware EEPROM Emulation versus Flash Memory Software Solutions
AN996	Glossary	Emulating the Unification of Flash and EEPROM: a Glossary
AN998	Technology	FLASH+™ Multiple Memory Technology
AN999	Drivers	Software Drivers for the M39432 FLASH+™ Multiple Memory

SOFTWARE EXAMPLES

The following three program fragments show examples of how the drivers can be used. The source files can be downloaded from the server. They are respectively: SCEE9701.C, SCEE9702.C and SCEE9703.C.

Example of a Program Using the Bulk Erase Function

This program fragment erases all the Flash memory sectors by using the *bulk erase function*. It also demonstrates the use of the RESET and CONTROL_DATA_POLLING_FLA functions.

```
/* FLASH+ ; M39432 DRIVER SOURCE CODE : FLASH BULK ERASE                    */
/* Version: 1.01                                                            */

/****************************************************************************/
/*         Copyright (c) 1997 SGS-THOMSON Microelectronics.                 */
/*                                                                          */
/* This program is provided "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER    */
/* EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO, THE IMPLIED WARRANTY */
/* OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. THE ENTIRE RISK */
/* AS TO THE QUALITY AND PERFORMANCE OF THE PROGRAM IS WITH YOU. SHOULD THE */
/* PROGRAM PROVE DEFECTIVE, YOU ASSUME THE COST OF ALL NECESSARY SERVICING, */
/* REPAIR OR CORRECTION.                                                    */
/****************************************************************************/

/*************************************************************/
/*                                                           */
/*      This program executes the bulk erase function.       */
/*      All the sectors in the flash will be erased.         */
/*                                                           */
/*      input variable :        none                         */
/*      internal variable :     bulk_ok,=0 when the bulk     */
/*                              erase is ok                  */
/*      output variable :       none                         */
/*                                                           */
/*                                                           */
/*************************************************************/
#define byte1 0xaa
#define byte2 0x55
#define byte_erase 0x80
#define byte_confirm 0x10
#define byte_rst 0xf0

#define prog_code1 0x85555
#define prog_code2 0x82aaa
```

```
                        /* DECLARATION OF FUNCTIONS */

 /* write and read functions*/
 void WRITE(char xhuge *,char );
 char READ_BIT(char, char xhuge * );
 char READ(char xhuge *addr);

 /* erase function*/
 char BULK_ERASE(void);

 /* control function*/
char CONTROL_DATA_POLLING_FLA(char,char xhuge *);

 /* reset function*/
 void RST(char xhuge *);

                        /* MAIN STARTS HERE */
 void main (void)   {
 char bulk_ok=1;

       bulk_ok = BULK_ERASE();
}
                        /* END OF MAIN */

/**FUNCTION BULK_ERASE: FLASH***********************************/
/*                                                             */
/*      input variable :        none                           */
/*                                                             */
/*      output variable :       flag_polling_dq7,receives the  */
/*                              result of the data polling, if */
/*                              this flag=0 the erase is       */
/*                              complete.                      */
/*  this function issues the bulk erase command                */
/*  all the sectors in the flash will be erased                */
/*************************************************************/

char BULK_ERASE(void)  {

 char xhuge *addr;
 char byte, flag_polling_dq7=1,last_byte=0xff;

/* coded cycle */
 addr= prog_code1;/* write 0xaa at @5555H IN FLASH (base=80000) */
 byte=byte1;
```

```
 WRITE(addr,byte);

 addr= prog_code2;/* write 0x55 at @2AAAH IN FLASH (base=80000) */
 byte=byte2;
 WRITE(addr,byte);

/*  erase command */
 addr=prog_code1;/* write 0x80 at @5555H IN FLASH (base=80000)  */
 byte=byte_erase;
 WRITE(addr,byte);

/* coded cycle */
 addr= prog_code1;/* write 0xaa at @5555H IN FLASH (base=80000) */
 byte=byte1;
 WRITE(addr,byte);

 addr= prog_code2;/* write 0x55 at @2AAAH IN FLASH (base=80000) */
 byte=byte2;
 WRITE(addr,byte);

/*bulk erase confirm */
 addr=prog_code1;/* write 0x10 at @5555H IN FLASH (base=80000)  */
 byte=byte_confirm;
 WRITE(addr,byte);
 flag_polling_dq7= CONTROL_DATA_POLLING_FLA(last_byte,addr);
 return(flag_polling_dq7);
}

/**FUNCTION WRITE: TO WRITE A BYTE IN FLASH MEMORY***************/
/*                                                               */
/*      input variable :        addr, write address              */
/*                              byte                             */
/*      output variable :       none                             */
/*                                                               */
/*  this function writes a byte at the given address             */
/*****************************************************************/

void WRITE(char xhuge *addr,char byte)  {

        *addr=byte;
}

/**FUNCTION READ: TO READ A BYTE FROM FLASH MEMORY***************/
/*                                                               */
```

```
/*      input variable :        addr, read address              */
/*                                                              */
/*      output variable :       read, read byte                 */
/*                                                              */
/*  this function reads a byte at the given address             */
/****************************************************************/

char READ(char xhuge *addr) {
char read;

      read = *addr;
      return(read);
}

/**FUNCTION CONTROL_DATA_POLLING_FLA (FLASH)********************/
/*                                                              */
/*      input variable :        addr, read address              */
/*                              last_byte, last byte written    */
/*                                                              */
/*  internal variables :        read bits from the status       */
/*                              register:data_polling_bit_dq7   */
/*                                                              */
/*  When a programming operation is in progress, this bit       */
/*  outputs the complement of the bit being programmed on dq7.  */
/*  During an Erase operation, it outputs '0' then '1' after    */
/*  Erase completion.                                           */
/*                                                              */
/*  error_bit_dq5 outputs 1 when there is an error              */
/*  during programming or erasing.                              */
/*                                                              */
/*   last_bit_dq7 variable which stores the value of the last   */
/*   bit dq7 being programmed is set to 0FFH before the erasing.*/
/*   n_bit, bit number to be read.                              */
/*                                                              */
/*   output variable :  flag_data_polling, returns 0 when       */
/*                      the read bit = last_bit written         */
/*                      or when dq7=1 for erasure.              */
/*                      It returns 1 if :                       */
/*                      - error_bit_dq5=1 (memory fail) and     */
/*             and      - read bit is the complement of the bit */
/*                      being programmed or erased              */
/*                                                              */
/*  This function controls the data polling during              */
/*  programming or erasing                                      */
```

```
/*****************************************************************/

char CONTROL_DATA_POLLING_FLA(char last_byte,char xhuge *addr)
{
char flag_data_polling=1,data_polling_bit_dq7;
char n_bit,last_bit_q7,error_bit_dq5;
int count7=0;

 last_bit_q7=last_byte&0x80;
 do
 {
 n_bit=7;
 data_polling_bit_dq7 = READ_BIT(n_bit,addr);
 n_bit=5;
 error_bit_dq5=READ_BIT(n_bit,addr);
 count7++;
 }
 while ((data_polling_bit_dq7!=last_bit_q7)&&(error_bit_dq5==0));
 if(error_bit_dq5==0) flag_data_polling=0;
 else
 {
 n_bit=7;
 data_polling_bit_dq7=READ_BIT(n_bit,addr);
 if(data_polling_bit_dq7==last_bit_q7) flag_data_polling=0;
 else RST(addr);
 }
 return(flag_data_polling);
}

/**FUNCTION READ_BIT: TO READ A BIT(x) FROM A FLASH BYTE*********/
/*                                                               */
/*      input variable :        addr, read address               */
/*                              n_bit, bit number                */
/*      output variable :       bit_dqx                          */
/*      this function reads a byte at the given address          */
/*      makes a mask on the byte and returns the value           */
/*      of the bit                                               */
/*****************************************************************/

char READ_BIT(char n_bit, char xhuge *addr ) {
char read,bit_dqx;

        read = READ(addr);
        switch(n_bit)
```

```
        {
        case 0: bit_dqx= read&0x01;
                break;
        case 1: bit_dqx= read&0x02;
                break;
        case 2: bit_dqx= read&0x04;
                break;
        case 3: bit_dqx= read&0x08;
                break;
        case 4: bit_dqx= read&0x10;
                break;
        case 5: bit_dqx= read&0x20;
                break;
        case 6: bit_dqx= read&0x40;
                break;
        case 7: bit_dqx= read&0x80;
                break;
        }
        return(bit_dqx);
}

/**FUNCTION RST: TO RESET THE FLASH MEMORY**********************/
/*                                                             */
/*      input variable :        addr, write address            */
/*                              byte=0xf0                      */
/*      output variable :       none                           */
/*                                                             */
/*  This function resets the flash, after a wait state of 5us. */
/*  Subsequent read operations will read the memory array      */
/*  addressed and output the read byte.                        */
/*************************************************************/

void RST(char xhuge *addr) {
char byte,count=0;

 byte=byte_rst;
 WRITE(addr, byte);
 while(count++<100);

}
```

Example of a Program Using the Single Sector Erase and Byte Program Functions

This program fragment erases one sector of Flash memory, and then writes the value 04H throughout the sector using the byte programming operation. It also demonstrates the use of the RESET and CONTROL_DATA_POLLING_FLA functions.

```
/* FLASH+ ; M39432 DRIVER SOURCE CODE : SECTOR ERASE AND BYTE PROGRAMMING   */
/* Version: 1.01                                                            */

/****************************************************************************/
/*         Copyright (c) 1997 SGS-THOMSON Microelectronics.                 */
/*                                                                          */
/* This program is provided "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER    */
/* EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO, THE IMPLIED WARRANTY */
/* OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. THE ENTIRE RISK */
/* AS TO THE QUALITY AND PERFORMANCE OF THE PROGRAM IS WITH YOU. SHOULD THE */
/* PROGRAM PROVE DEFECTIVE, YOU ASSUME THE COST OF ALL NECESSARY SERVICING, */
/* REPAIR OR CORRECTION.                                                    */
/****************************************************************************/

/*****************************************************************/
/*                                                               */
/*  This program calls the functions SECTOR_ERASE and BYTE_WRI_FLA */
/*  input variable :    none                                     */
/*  internal variable : array, which contains the sector numbers */
/*                      n, number of sector to be erased         */
/*                      erase_ok, flag which indicates if        */
/*                      the erase is ok                          */
/*                      addr_flash_appli, address to program the */
/*                      application in the flash                 */
/*                      byte, byte to program                    */
/*  output variable :  none                                      */
/*  erase_ok=0 when the erase of sectors is successful           */
/*  write_ok=0 when the write in the flash is successful         */
/*****************************************************************/
#define byte1 0xaa
#define byte2 0x55
#define byte_prog 0xa0
#define byte_erase 0x80
#define byte_confirm 0x10
#define byte_sector_erase_confirm 0x30
#define byte_rst 0xf0
#define page 64
#define prog_code1 0x85555
#define prog_code2 0x82aaa
```

```
                        /* DECLARATION OF FUNCTIONS */

                        /* write function*/
 char BYTE_WRITE_FLA(char xhuge *,char);
 void WRITE(char xhuge *,char );
                        /* erase function*/
 char SECTOR_ERASE(char,char []);
                        /* control status register functions */
 char CONTROL_DATA_POLLING_FLA(char,char xhuge *);
 char CONTROL_TIMER(char xhuge *,char);
                        /* read functions */
 char READ_BIT(char, char xhuge * );
 char READ(char xhuge *);
                        /* reset function */
 void RST(char xhuge *);

 char xhuge * SELECT_SECTOR (char);

                       /* MAIN STARTS HERE */

void main(void)
{
char erase_ok=1,array[8],n;
char byte,write_ok_byte=1;
int i=0;

char xhuge *addr_flash_appli;

addr_flash_appli = 0x90000;

/* init array  */
        array[0]=1;
        n=1;
/***************/

        erase_ok = SECTOR_ERASE(n,array);

/* init of variables */

  byte=0x04;
/*********************/

  for(i=0;i<=8192;i++)
```

```
 {
 write_ok_byte=BYTE_WRITE_FLA((addr_flash_appli + i),byte);
 }

}
                          /* END OF MAIN */

/**FUNCTION SECTOR_ERASE : TO ERASE SECTORS OF FLASH MEMORY******/
/*                                                               */
/*   input variable :   n, number of sectors to be erased.      */
/*                      array, contains the sector addresses     */
/*                      (0 to 7) to be erased.                   */
/*                                                               */
/*   internal variables :  erase_timer_bit_dq3, this bit from    */
/*                         the status register gives information*/
/*                         about the erase timeout period. This */
/*                         bit = 0 when the timeout is not      */
/*                         expired.                             */
/*                         flag_timer_dq3, this flag=0 when the */
/*                         internal erase cycle has started.    */
/*                         flag_polling_dq7, receives the result*/
/*                         of the data polling. This flag=0     */
/*                         when the erase is complete           */
/*                         n_sector, sector number              */
/*                         n_bit, bit number                    */
/*                                                               */
/*      output variable :  erase_ok                              */
/*                                                               */
/*  This function issues the sector erase command.               */
/*  All the sectors mentioned in the array are erased.           */
/*  This function returns 0 when there is a successful erase     */
/***************************************************************/

char SECTOR_ERASE(char n,char array[])  {

 char xhuge *addr;
 char byte, flag_polling_dq7=1,erase_timer_bit_dq3
 char n_bit=3,n_sector,i=0,flag_timer_dq3;
 char erase_ok=1, last_byte= 0xff;

/* coded cycle */
 addr= prog_code1;/* write 0xaa at @5555H IN FLASH (base=80000) */
 byte=byte1;
 WRITE(addr,byte);
```

```
 addr= prog_code2;/* write 0x55 at @2AAAH IN FLASH (base=80000) */
 byte=byte2;
 WRITE(addr,byte);

/* erase command */
 addr=prog_code1;/* write 0x80 at @5555H IN FLASH (base=80000)  */
 byte=byte_erase;
 WRITE(addr,byte);

/* coded cycle */
 addr= prog_code1;/* write 0xaa at @5555H IN FLASH (base=80000) */
 byte=byte1;
 WRITE(addr,byte);

 addr= prog_code2;/* write 0x55 at @2AAAH IN FLASH (base=80000) */
 byte=byte2;
 WRITE(addr,byte);
/*sector erase confirm */
do
   {
   n_sector=array[i];
   addr=SELECT_SECTOR(n_sector);     /* write 0x10 at @5555H   */
                                     /* IN FLASH (base=80000)  */
   byte=byte_sector_erase_confirm;
   WRITE(addr,byte);
   erase_timer_bit_dq3=READ_BIT(n_bit,addr);
   i++;
   }
while((i<n)&&(!erase_timer_bit_dq3));

if(!erase_timer_bit_dq3)flag_timer_dq3 = CONTROL_TIMER(addr,n_bit);

flag_polling_dq7= CONTROL_DATA_POLLING_FLA(last_byte,addr);

if((!flag_timer_dq3)&&(!flag_polling_dq7)) erase_ok=0;
return(erase_ok);
}

/**FUNCTION READ: TO READ A BYTE FROM FLASH MEMORY***************/
/*                                                               */
/*      input variable :        addr, read address               */
/*                                                               */
/*      output variable :       read, read byte                  */
```

```
/*                                                                  */
/*  this function reads a byte at the given address                 */
/*******************************************************************/

char READ(char xhuge *addr) {
char read;

      read = *addr;
      return(read);
}

/**FUNCTION CONTROL_DATA_POLLING_FLA (FLASH)*********************/
/*                                                                  */
/*      input variable :        addr, read address                  */
/*                              last_byte, last byte written        */
/*                                                                  */
/*  internal variables :        read bits from the status           */
/*                              register:data_polling_bit_dq7       */
/*                                                                  */
/*  When a programming operation is in progress, this bit           */
/*  outputs the complement of the bit being programmed on dq7.      */
/*  During an Erase operation, it outputs '0' then '1' after        */
/*  Erase completion.                                               */
/*                                                                  */
/*  error_bit_dq5 outputs 1 when there is an error                  */
/*  during programming or erasing.                                  */
/*                                                                  */
/*   last_bit_dq7 variable which stores the value of the last       */
/*   bit dq7 being programmed is set to 0FFH before the erasing.*/
/*   n_bit, bit number to be read.                                  */
/*                                                                  */
/*   output variable :  flag_data_polling, returns 0 when           */
/*                      the read bit = last_bit written             */
/*                      or when dq7=1 for erasure.                  */
/*                      It returns 1 if :                           */
/*                      - error_bit_dq5=1 (memory fail) and         */
/*              and     - read bit is the complement of the bit     */
/*                      being programmed or erased                  */
/*                                                                  */
/*  This function controls the data polling during                  */
/*  programming or erasing                                          */
/*******************************************************************/

char CONTROL_DATA_POLLING_FLA(char last_byte,char xhuge *addr)
```

```
{
char flag_data_polling=1,data_polling_bit_dq7;
char n_bit,last_bit_q7,error_bit_dq5;
int count7=0;

 last_bit_q7=last_byte&0x80;
 do
 {
 n_bit=7;
 data_polling_bit_dq7 = READ_BIT(n_bit,addr);
 n_bit=5;
 error_bit_dq5=READ_BIT(n_bit,addr);
 count7++;
 }
 while ((data_polling_bit_dq7!=last_bit_q7)&&(error_bit_dq5==0));
 if(error_bit_dq5==0) flag_data_polling=0;
 else
 {
 n_bit=7;
 data_polling_bit_dq7=READ_BIT(n_bit,addr);
 if(data_polling_bit_dq7==last_bit_q7) flag_data_polling=0;
 else RST(addr);
 }
 return(flag_data_polling);
}

/**FUNCTION READ_BIT: TO READ A BIT(x) FROM A FLASH BYTE*********/
/*                                                               */
/*      input variable :        addr, read address               */
/*                              n_bit, bit number                */
/*      output variable :       bit_dqx                          */
/*      this function reads a byte at the given address          */
/*      makes a mask on the byte and returns the value           */
/*      of the bit                                               */
/***************************************************************/

char READ_BIT(char n_bit, char xhuge *addr ) {
char read,bit_dqx;

        read = READ(addr);
        switch(n_bit)
        {
        case 0: bit_dqx= read&0x01;
                break;
```

```
        case 1: bit_dqx= read&0x02;
                break;
        case 2: bit_dqx= read&0x04;
                break;
        case 3: bit_dqx= read&0x08;
                break;
        case 4: bit_dqx= read&0x10;
                break;
        case 5: bit_dqx= read&0x20;
                break;
        case 6: bit_dqx= read&0x40;
                break;
        case 7: bit_dqx= read&0x80;
                break;
        }
        return(bit_dqx);
}

/**FUNCTION RST: TO RESET THE FLASH MEMORY**********************/
/*                                                             */
/*      input variable :        addr, write address            */
/*                              byte=0xf0                      */
/*      output variable :       none                           */
/*                                                             */
/*  This function resets the flash, after a wait state of 5æs. */
/*  Subsequent read operations will read the memory array      */
/*  addressed and output the read byte.                        */
/*************************************************************/

void RST(char xhuge *addr) {
char byte,count=0;

 byte=byte_rst;
 WRITE(addr, byte);
 while(count++<100);

}

/**FUNCTION SELECT_SECTOR***************************************/
/*                                                             */
/*  input variable :  n_secteur, sector to be selected.        */
/*  output variable : addr, base address of the selected sector */
/*                                                             */
/*  This function receives the number of the sector selected   */
```

```
/*  and returns its base address                                    */
/*****************************************************************/

char xhuge * SELECT_SECTOR (char n_secteur) {
char xhuge *addr;
        switch(n_secteur)
          {
        case 0: addr= 0x80000;
                break;
        case 1: addr= 0x90000;
                break;
        case 2: addr= 0xa0000;
                break;
        case 3: addr= 0xb0000;
                break;
        case 4: addr= 0xc0000;
                break;
        case 5: addr= 0xd0000;
                break;
        case 6: addr= 0xe0000;
                break;
        case 7: addr= 0xf0000;
                break;
        }
        return(addr);
}

/**FUNCTION CONTROL_TIMER:(memory flash)************************/
/*                                                              */
/*   input variable : addr,  read address                       */
/*                    n_bit, the number of the bit to be        */
/*                           controlled                         */
/*   output variable : flag_timer, return 0 erase timer bit = 1 */
/*                     return 1 if the count is overflow.       */
/*  This function awaits the start of the internal flash erase  */
/*  cycle. When the last sector erase command has been entered, */
/*  the P/E.C. sets the erase bit timer to '0'.                 */
/*  The wait period is finished after 80 to 120us.              */
/*  When the internal erase cycle starts : the erase bit        */
/*  timer = 1 and the function return 0.                        */
/*  If an error occurs (count is overflow the function return 1)*/
/*****************************************************************/

char CONTROL_TIMER(char xhuge *addr,char n_bit) {
```

```
char flag_timer=1,bit_timer;
int count=0;
   do
   {
   bit_timer = READ_BIT(n_bit,addr);
   count++;
   }
   while ((bit_timer != 0x20)&&(count<=100));  /*while dq5 != 1*/
   if(count<=400) flag_timer = 0 ;
   return(flag_timer);
}

/**FUNCTION BYTE_WRITE_FLA: TO WRITE A BYTE IN FLASH & CONTROL***/
/*                                                               */
/*      input variable :        addr, write address              */
/*                              byte                             */
/*      output variable :       flag_data_polling_dq7            */
/*                                                               */
/*  This function writes a byte at the given address and         */
/*  controls the toggle bit.                                     */
/*  return flag_timer_dq6,=0 if byte write is successful         */
/***************************************************************/

char BYTE_WRITE_FLA(char xhuge *addr,char byte)  {
char  flag_data_polling_dq7=1;

/* this block enables the writes in the memory */
       {
char xhuge *address;
char bytes;
address= prog_code1;/*write 0xaa at @5555H IN FLASH (base=80000)*/
bytes=byte1;
WRITE(address,bytes);

address= prog_code2;/*write 0x55 at @2AAAH IN FLASH (base=80000)*/
bytes=byte2;
WRITE(address,bytes);

address=prog_code1;/*write 0xa0 at @5555H IN FLASH (base=80000)*/
bytes=byte_prog;
WRITE(address,bytes);
        }
```

```
        WRITE(addr,byte);
        flag_data_polling_dq7 = CONTROL_DATA_POLLING_FLA(byte,addr);
        return(flag_data_polling_dq7);
}
```

Example of a Program Using the SDP Enable, SDP Disable and SDP Byte Write Functions

This program fragment enables the software data protection function, and then continues to write values into the EEPROM area by using the SDP_BYTE function. Finally, it disables the software data protection function. It also demonstrates the use of the CONTROL_TOGGLE_EE function.

```
/*   FLASH+ ; M39432 DRIVER SOURCE CODE : SDP IN EEPROM BLOCK                */
/* Version: 1.01                                                             */

/*****************************************************************************/
/*         Copyright (c) 1997 SGS-THOMSON Microelectronics.                  */
/*                                                                           */
/* This program is provided "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER     */
/* EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO, THE IMPLIED WARRANTY */
/* OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. THE ENTIRE RISK */
/* AS TO THE QUALITY AND PERFORMANCE OF THE PROGRAM IS WITH YOU. SHOULD THE */
/* PROGRAM PROVE DEFECTIVE, YOU ASSUME THE COST OF ALL NECESSARY SERVICING, */
/* REPAIR OR CORRECTION.                                                     */
/*****************************************************************************/

/*************************************************************/
/*                                                           */
/*      This program calls three functions:                  */
/*      SDP :           enable data protection               */
/*      WRITE_SDP :     write a byte and control the toggle bit */
/*                      when the eeprom is protected         */
/*      DIS_SDP :       disable the data protection          */
/*                                                           */
/*      input variable : none                                */
/*      internal variable :     addr, address to be written  */
/*                              byte, byte to be written     */
/*                              write_ok_byte                */
/*                              free, =0 when the internal   */
/*                              programming cycle is finished */
/*                              (result of the toggle bit)   */
/*      output variable : none                               */
/*                                                           */
/*  write_ok_byte=0 when the write operation is successful   */
/*************************************************************/

#define byte1 0xaa
#define byte2 0x55
#define byte_sdp 0xa0
#define byte3 0x80
#define byte4 0x20
```

```
#define addr1 0x45555
#define addr2 0x42aaa

/* control status register function */
char CONTROL_TOGGLE_EE(char xhuge *);

/* write and read functions */
char READ_BIT(char, char xhuge *);
void WRITE(char xhuge *,char);
char SDP_BYTE(char xhuge *,char);
char READ(char xhuge *);

/* set and disable data protection function */
void SDP(void);
void DIS_SDP(void);

                                    /* MAIN STARTS HERE */
/****************/
/* main program */
/****************/

void main (void)  {

char write_ok_byte=1,free=1 ;
char byte;
char xhuge *addr;

/* INIT THE ADDRESS TO WRITE IN THE EEPROM AND THE DATA   */
addr = 0x40040;
byte = 0xaa;

       SDP();
/* the memory is protected */
       free= CONTROL_TOGGLE_EE(addr);
/* wait the end of the internal write cycle */
       if(free==0);
       {
       write_ok_byte = SDP_BYTE(addr,byte);
       }
       DIS_SDP();

/* the memory is not protected */
```

```
}                                       /* END OF MAIN */

/**FUNCTION WRITE: TO WRITE A BYTE IN EEPROM*********************/
/*                                                               */
/*      input variable :        addr, address to be written      */
/*                              byte, byte to be written         */
/*      output variable :       none                             */
/*                                                               */
/* this function writes a byte at the given address              */
/*****************************************************************/

void WRITE(char xhuge *addr,char byte)  {

        *addr=byte;
}

/**FUNCTION READ: TO READ A BYTE FROM EEPROM*********************/
/*                                                               */
/*      input variable : addr, read address                      */
/*                                                               */
/*      output variable : read, read byte                        */
/*  this function reads a byte at the given address              */
/*****************************************************************/

char READ(char xhuge *addr) {
char read;

      read = *addr;
      return(read);
}

/**FUNCTION WRITE_SDP : TO WRITE A BYTE IN EEPROM WITH CONTROL***/
/*                                                               */
/*      input variable :        addr, address to be written      */
/*                              byte, byte to be written         */
/*      output variable :       flag_toggle_dq6                  */
/*      .                                                        */
/*  this function writes a byte at the given address and         */
/*  controls the toggle bit.                                     */
/*  return flag_toggle_dq6,=0 if the byte write is successful    */
/*****************************************************************/

char SDP_BYTE(char xhuge *addr,char byte)  {
char  flag_toggle_dq6=1;
```

```
/* this block enables the write in the memory */
       {
char xhuge *address;
char bytes;
    address=addr1;/* write 0xaa at @5555H IN EEPROM (base=40000) */
    bytes=byte1;
    WRITE(address,bytes);

    address=addr2;/* write 0x55 at @2AAAH IN EEPROM (base=40000) */
    bytes=byte2;
    WRITE(address,bytes);

    address=addr1;/* write 0xa0 at @5555H IN EEPROM (base=40000) */
    bytes=byte_sdp;
    WRITE(address,bytes);
        }

    WRITE(addr,byte);
    flag_toggle_dq6 = CONTROL_TOGGLE_EE(addr);
    return(flag_toggle_dq6);
}
/**FUNCTION CONTROL_TOGGLE_EE (EEPROM)**************************/
/*                                                             */
/*      input variable :        addr, read address             */
/*      internal variable :     first_bit_dq6, first read      */
/*                              (from the status register) of  */
/*                              bit dq6                        */
/*                              second_bit_dq6, second read    */
/*                              (       "       ) of bit d6    */
/*                                                             */
/*      output variable :       flag_toggle, returns 0 when the */
/*                              toggle bit stops               */
/*                              (the internal write cycle is   */
/*                              finished) and return 1 if the  */
/*                              count is overflow or less than */
/*                              we expected                    */
/*              this function controls the toggle bit          */
/*************************************************************/

char CONTROL_TOGGLE_EE(char xhuge *addr) {
char first_bit_dq6,second_bit_dq6,flag_toggle=1,n_bit=6;
int count6=0;
       do
```

```
        {
        first_bit_dq6=READ_BIT(n_bit,addr);
        second_bit_dq6=READ_BIT(n_bit,addr);
        count6++;
        }
        while ((first_bit_dq6!=second_bit_dq6)&&(count6<=200));
        if ((count6>=34)&&(count6<=200)) flag_toggle=0;
        return(flag_toggle);
}

/**FUNCTION READ_BIT: TO READ A BIT(x) FROM AN EEPROM BYTE*******/
/*                                                              */
/*      input variable :        addr, read address              */
/*                              n_bit, number of the bit        */
/*      output variable :       bit_dqx                         */
/*      this function reads a byte at the address,              */
/*      makes a mask on the byte and returns the bit value      */
/****************************************************************/

char READ_BIT(char n_bit, char xhuge *addr ) {
char read,bit_dqx;

        read = READ(addr);
        switch(n_bit)
        {
        case 0: bit_dqx= read&0x01;
                break;
        case 1: bit_dqx= read&0x02;
                break;
        case 2: bit_dqx= read&0x04;
                break;
        case 3: bit_dqx= read&0x08;
                break;
        case 4: bit_dqx= read&0x10;
                break;
        case 5: bit_dqx= read&0x20;
                break;
        case 6: bit_dqx= read&0x40;
                break;
        case 7: bit_dqx= read&0x80;
                break;
        }
        return(bit_dqx);
}
```

```
/**FUNCTION SDP: SET SDP(EEPROM)*********************************/
/*                                                               */
/*      input variable :        none                             */
/*      output variable :       none                             */
/*                                                               */
/*       This function enables the data protection               */
/*****************************************************************/

void SDP(void) {
char xhuge *addr;
char byte;

    addr=addr1;/* write 0xaa at @5555H IN EEPROM (base=40000) */
    byte=byte1;
    WRITE(addr,byte);

    addr=addr2;/* write 0x55 at @2AAAH IN EEPROM (base=40000) */
    byte=byte2;
    WRITE(addr,byte);

    addr=addr1;/* write 0xa0 at @5555H IN EEPROM (base=40000) */
    byte=byte_sdp;
    WRITE(addr,byte);

}

/**FUNCTION DIS_SDP:  DISABLE SDP(EEPROM)***********************/
/*                                                               */
/*      input variable :        none                             */
/*      output variable :       none                             */
/*                                                               */
/*        This function disables the data protection             */
/*****************************************************************/

/* DISABLE SDP */

void DIS_SDP(void) {
char xhuge *addr;
char byte;

    addr=addr1;/* write 0xaa at @5555H IN EEPROM (base=40000) */
    byte=byte1;
    WRITE(addr,byte);
```

```
    addr=addr2;/* write 0x55 at @2AAAH IN EEPROM (base=40000) */
    byte=byte2;
    WRITE(addr,byte);

    addr=addr1;/* write 0x80 at @5555H IN EEPROM (base=40000) */
    byte=byte3;
    WRITE(addr,byte);

    addr=addr1;/* write 0xaa at @5555H IN EEPROM (base=40000) */
    byte=byte1;
    WRITE(addr,byte);

    addr=addr2;/* write 0x55 at @2AAAH IN EEPROM (base=40000) */
    byte=byte2;
    WRITE(addr,byte);

    addr=addr1;
    byte=byte4;/* write 0x20 at @5555H IN EEPROM (base=40000) */
    WRITE(addr,byte);
}
```

AN1120
APPLICATION NOTE

EEPROM-Based Application Specific Memories

Although the bulk of memory devices shipped today are standard commodity products, there is a rapidly growing market for Application Specific Memories (ASMs). These are devices that are specifically optimized for particular applications. These include both custom devices, and standard products that are designed to perform a specific function. Although the general concept of ASM is applicable to any type of memory, the greatest activity today involves devices that include non-volatile memories, such as Flash, OTP or EEPROM.

Although the concept of ASM is not new, recent advances in technology, manufacturing efficiency and design re-use have made it possible to develop and produce ASMs at previously unobtainable levels of price-to-performance and with very short design times. This is opening up a huge range of innovative potential applications that were not previously feasible on technical, economic or time-to-market grounds.

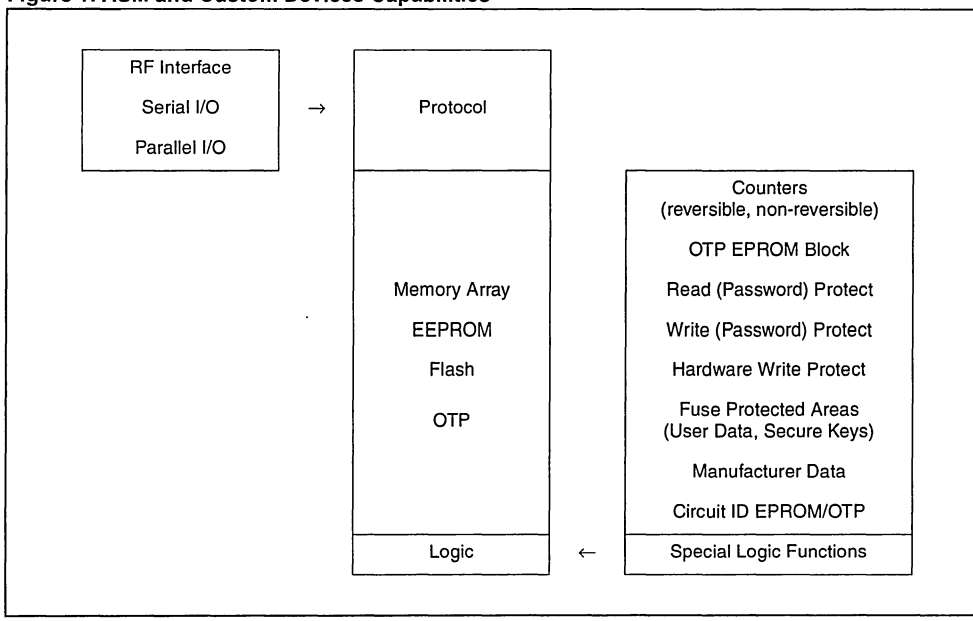
One of the first application specific memory devices was the phonecard chip, which ST began manufacturing over 20 years ago. Today's phonecard chips are considerably more sophisticated, but still retain the same basic requirements: they are non-volatile memories with special protection features, and they must be produced at extremely low cost. Many ASM applications need devices with the same characteristics, with the result that the techniques developed to meet the economic and technical demands of the phonecard market can be successfully applied to other areas.

The two main benefits of ASM technology are cost reduction through the use of fewer packages, and the protection of stored data or intellectual property. Reducing component count can be achieved either by mounting different memory chips in a single package or by implementing different memory functions on the same chip. A wide range of protection functions is available, including:

- read and write control mechanisms, both hardware and software
- OTP (one-time programmable) areas
- logic functions
- transport codes, anti-tearing functions, issuer keys, and other sophisticated mechanisms developed for the smartcard and phonecard markets.

Figure 1 illustrates the general structure of an ASM, and the variety of building blocks that are available. Typically, the core of the ASM is an EEPROM array. EEPROM is ideal for ASMs because of its byte-level programmability, its high write-cycle endurance and – increasingly important – its ability to operate at low voltage, and with very low standby currents. The EEPROM can also be complemented by other types of memory, such as EPROM (for OTP functions) and Flash memory (for large scale program code storage).

Figure 1. ASM and Custom Devices Capabilities



The full range of I/O protocols is available for ASM devices, including parallel access, 2-line serial bus access, 3-line serial bus access, and RF contactless interface schemes (not only loyalty cards, transport tickets, and contactless phonecards, but also in many different electronic tagging applications).

The versatility of ASM is a result of its great array of optional supporting features, as shown on the right hand side of Figure 1. Many of these are already widely used in smartcard chips but they are equally applicable to non-volatile memories designed to be embedded in any other type of objects. This wide choice of building blocks allows the customer to choose the optimum trade-off between the security mechanisms employed and the cost of the ASM. This is essential because many ASM applications are extremely cost-sensitive, and the target device costs can be as low as tens of cents in very high volumes.

The following examples illustrate some of the ways in which ASM technology is currently being applied to improve security, to enhance functionality and to lower costs in all of the major equipment segments, including the computer, telecommunications, consumer and automotive markets.

STANDARD ASMS

To illustrate how effective the concept is, consider the following ASMs. These have been developed for a highly specific market that is more conventionally handled as part of the standard applications market.

For example, standard ASMs have been developed for a number of applications, including Plug & Play monitors and DIMM memory modules that use the Serial Presence Detect (SPD) function.

Plug & Play peripherals contain an embedded non-volatile memory that holds information that allows the host PC to identify the peripheral. Once the PC has identified the peripheral, it can configure its subsystems and select appropriate software drivers. ST offers a range of EEPROMs (ST24xy21) specifically designed for use in Plug & Play monitors, where the standard access bus is the VESA Data Display Channel. The VESA specification requires the EEPROMs to have a standard I^2C interface augmented by an

additional VCLK input that is used to allow the PC to receive the display identification and operating parameter data.

The ST24xy21 devices are organized as 128 x 8-bits and are fully compatible with the VESA Data Display Channel (DDC) standards, communicating both in DDC1 (Transmit Only) and DDC2B (I^2C Bidirectional) modes. These devices allow a direct connection between the PC host and the monitor using the standard video cable and 15-pin VGA connector.

Although the ST24xy21 devices were developed from the first ST24LC21 1 Kbit EEPROM, they include specific enhancements, such as a Schmitt-Trigger input on the VCLK pin for better noise immunity, and a higher power-on reset value of 3 V. The range includes devices with a write control input, on pin 3, to improve data corruption rejection; and devices that offer full VESA 2.0 compatibility, including the error recovery mechanism that allows an automatic return to Transmit-Only mode in the event of invalid activity on the I^2C bus.

Another family of standard ASMs is illustrated by the M34C02, a serial EEPROM specifically designed to enhance the reliability of the Serial Presence Detect (SPD) function in DIMM DRAM modules. In the JEDEC SPD standard, the specifications of the DRAM module, including information such as DRAM type, speed, organization and manufacturer, is stored in an on-board non-volatile memory, and used by the PC during system configuration. SPD is mandatory for all new 168-pin and 200-pin DRAM modules for PCs and workstations and will also be used in DRAM Modules for new PC VGA cards.

The M34C02 offers a superior solution to the standard 2 Kbit I^2C serial EEPROM. Because the SPD data is critical to the reliability of the system, the EEPROM needs to be immune to both accidental data corruption and tampering by the user. Standard EEPROMs offer good security against accidental data corruption but can obviously provide no protection against tampering as they are designed to support repeated erase/program cycles. This problem is solved with the M34C02 by making the bottom half of the memory array permanently lockable. This means that after programming the SPD data in the DIMM, the manufacturer can issue an irreversible command to write-protect the first 128 bytes of the memory area, still leaving the upper half free for scratch-pad use.

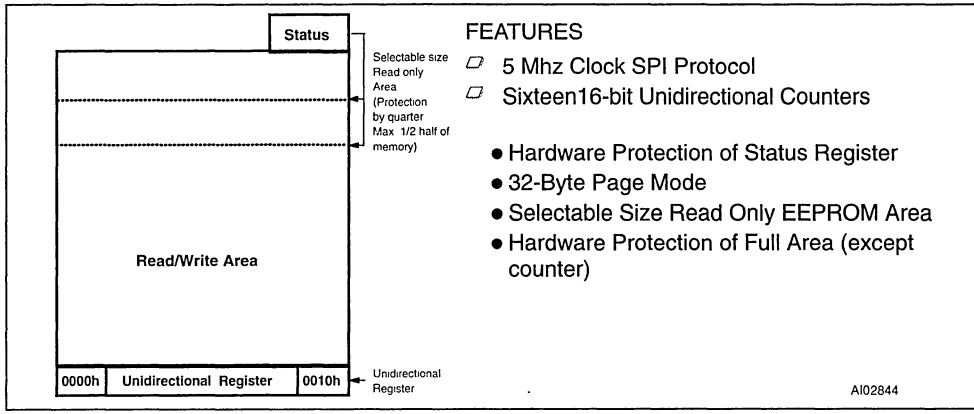
Of course, an ASM specifically designed for one application may still be useful in others. For example, the concept of software-lockable EEPROM has wider applications than DIMM modules and the M34C02 has given rise to a range of devices offering this facility, including the M34Wxx devices, in which the user can select the position (top or bottom of memory array) and size of the protected block.

TAMPER-PROOF COUNTING

There are many applications where it is necessary to keep an incorruptible count of the number of times a particular event has occurred. Many photocopiers, for example, keep a count of the number of copies made, and this information is often used to calculate rental or service charges or to investigate warranty claims. For example, if the number of copies recorded is significantly greater than the number of copies expected from a toner cartridge, this could indicate that the user has refilled the cartridge (perhaps with an inferior toner) and this could, in turn, affect the warranty. Clearly, the end user should not be able to modify the data stored in the photocopier's non-volatile memory.

An application where tamper-proof counting is even more important is in the car odometer. The value of a used car is greatly affected by its total mileage, and so the illegal practice of "turning back the clock" is as old as the used car market. The M35080 is a new ASM developed to provide an ideal solution to this problem. As shown in Figure 2, the M35080 is derived from the M95080, an 8 Kbit EEPROM with an SPI interface. The main difference is the addition of comparators and control logic to govern the write operations in the first 32 bytes of the EEPROM array. This allows the write operation to proceed in this area only if the new value for each 16-bit word is greater than the data already stored there. As a result, the first 32 bytes of the EEPROM array emulate an array of 16 unidirectional 16-bit counters.

Figure 2. M35080 block diagram



The particularly demanding requirements of this application would not have been met by the typical EEPROM endurance of 100K erase/write cycles and ten year data retention (both of which would have been too low). The M35080, therefore, is built with ST's high endurance double polysilicon CMOS technology. For the M35080, one million erase/write cycles and a 40-year data retention are guaranteed over a temperature range of -40 °C to +85 °C, ensuring that the odometer will function correctly throughout the lifetime of the car.

EMBEDDING ASMS IN OBJECTS

In the examples considered so far, the ASM is incorporated into equipment subsystems, but there is also currently an enormous interest in embedding ASMs in objects. Often, the reason is to enhance the functionality of the object, or to provide protection against cloning, misuse or similar undesirable activities.

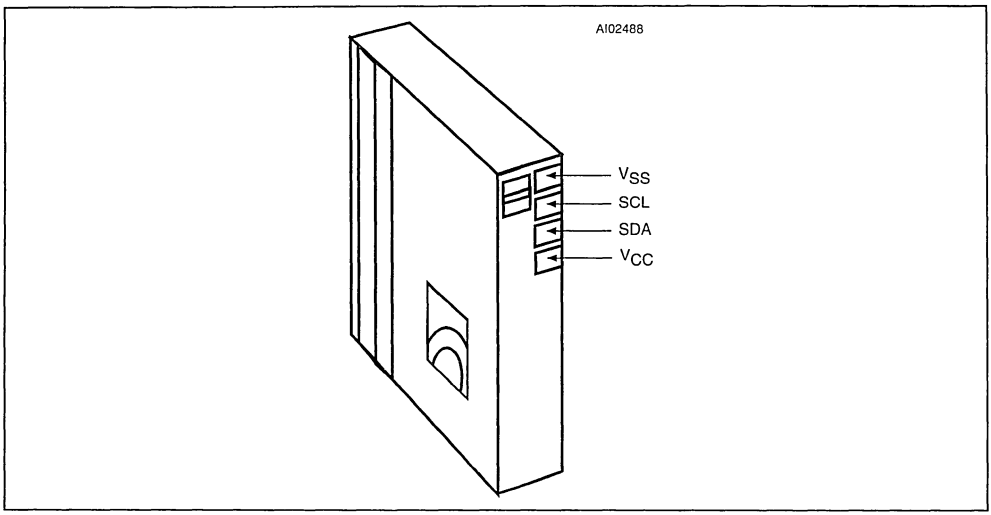
A simple example of how ASMs can enhance the functionality of equipment is provided by the "smart" digital video cassette recorder (digital VCR). In a standard VCR, users often need to find a particular part of the tape, such as the beginnings and ends of the recordings that have been strung together on a single cassette tape. This can often involve frustrating and time-consuming winding and rewinding. Storing this information in a non-volatile memory in the VCR would make the equipment more user-friendly (allowing the machine to position the tape quickly at the required location) but would become invalid if the cassette were changed.

The functionality of the VCR can be considerably enhanced by incorporating the memory in the cassette rather than in the equipment. Because each cassette then carries its own data, cassettes can be removed and the subsequently reloaded into the same machine or into a different machine, without losing any of the stored information.

If the object does not normally contain a PCB, a means must be found for incorporating the ASM so that it is electrically accessible, and in the form that can be engineered for minimum cost and space. For example, for the VCR application, ST has developed memory modules that consist of a small PCB, on which an EEPROM memory is mounted, and a Transil device to protect the memory against voltage transients (encountered when the module is brought into electrical contact with the VCR).

The modules are electrically compatible with standard I^2C EEPROMs, such as the M24xxx series. The PCB provides four contact pads for the V_{CC}, ground, serial clock and serial data lines (as shown in Figure 3). Consequently, these modules are equally applicable to a wide range of other applications, and are currently shipping in large volumes.

Figure 3. Memory-in-Cassette Module



SMART CONSUMABLES

One of the most interesting classes of ASM applications involves embedding non volatile (NV) memories in replacement parts or consumables. The motivation for doing this could be:

- for technical reasons, to ensure that only replacement parts meeting particular specifications are accepted by the equipment. For example, in an inkjet printer, the use of inks that do not exactly match the physical and chemical properties, for which the head was designed, may cause physical damage to the print head.
- or for commercial reasons. For example, if an equipment manufacturer can be sure of being the sole supplier of the equipment's consumables, it would have the option of shifting some of its profit margin to the consumables, thereby reducing the purchase price to give it a competitive marketing edge.

ASMs can provide an effective solution in either case. By embedding a low-cost ASM in the replacement part, the equipment can be made to identify and authenticate the part, to determine whether or not it is officially approved and to take an appropriate action. One of the major advantages of this approach is that information stored in a memory chip is subject to the same copyright and trademark laws as information published on paper, or in other ways. This means that while there may be no legal impediment to producing clone parts that are electrically and mechanically compatible with the official parts, the clone manufacturer will not be able to duplicate the entire contents of the ASM without breaking laws that protect intellectual property.

In terms of the specific implementation, each "smart consumable" application has its own set of economic and engineering parameters. Sometimes these are compatible with "standard" ASMs such as the MIC modules, in which case the customer can use an off-the-shelf solution. In other cases, the best solution may be a custom device developed in partnership with ST's ASM Business Unit, which brings together the technical and marketing resources needed to develop solutions rapidly to problems that involve the combination of non-volatile memory blocks and any other functions. As an example, the odometer application described earlier took just six months to implement fully, from the first customer enquiry to the start of volume production.

AN627
APPLICATION NOTE

Serial EEPROM Compatible With Plug-and-Play VESA Display Data Channel (Versions 1.0 and 2.0)

The ST products whose names are of the form ST24xy21 are Application Specific Memory devices (ASM). As well as containing 1 Kb of EEPROM, organized as 128 x 8, they are fully compatible with the VESA Data Display Channel (VDDC) modes, DDC1 and DDC2B. When installed in a Plug-and-Play PC display, the device can work in DDC1 mode, using only a 2 wire bus, or in both DDC1 and DDC2B modes, using a 3 wire bus.

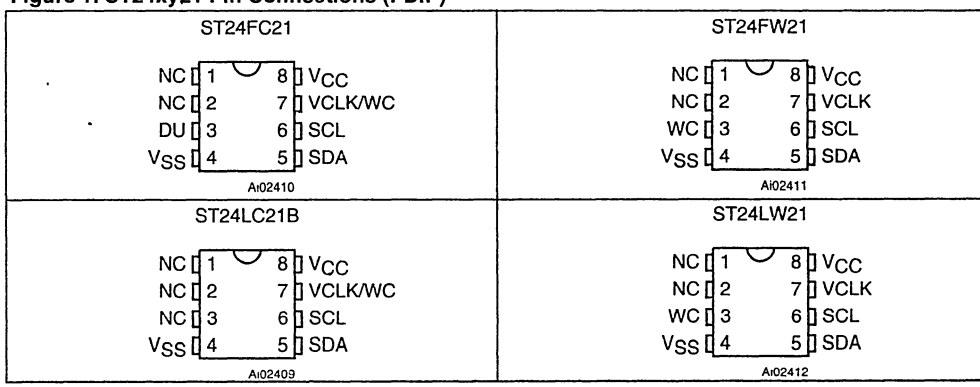
- DDC1: a unidirectional data channel from the display to the host PC, continuously transmitting Extended Display Identification, EDID, information.
- DDC2B: a bidirectional data channel based on the I^2C ™ protocol. The host PC can request Extended Display Identification information, EDID, or Video Display Interface information, VDIF, over the DDC2B channel. In addition to this, the DDC2B channel can act as a transparent channel for ACCESS.bus ™ communication, allowing the direct replacement to be made.

Table 1. Members of the ST24xy21 Family

	Write Control on VCLK (pin 7)	Write Control on pin 3
Conformance to VDDC Version 2.0	ST24FC21	ST24FW21
Conformance to VDDC Version 1.0	ST24LC21B	ST24LW21

Table 1 summarizes the ST24xy21 naming convention. Those products whose names are of the form ST24Ly21 conform to version 1.0 of the VDDC specification. Those products whose names are of the form ST24Fy21 conform to the more recent (March 1996) version 2.0. Those products whose names are of the form ST24xC21 use the VCLK line as the Write Control input, as described on page 7, and those of the form ST24xW21 have a separate Write Control input. All ST24xy21 devices are available in 8-pin PDIP and SO packages. Figure 1 summarizes the pin-out for PDIP.

Figure 1. ST24xy21 Pin Connections (PDIP)



DEVICE DESCRIPTION

The functionality of the ST24xy21 family greatly simplifies the design of the PC graphics board, and allows a direct connection between the display and the host PC using a standard video cable. Each member of the family has a standard I^2C interface, including the SCL and SDA lines, and an additional clock input, VCLK, as required by the V.D.D.C. specification. This additional clock input allows the host PC to receive, from the display, all information required to configure the graphics board and the display's software driver. ST24xy21 serial communication runs at 400 kHz in both DDC1 and DDC2B modes, with a supply voltage between 3.6 V and 5.5 V.

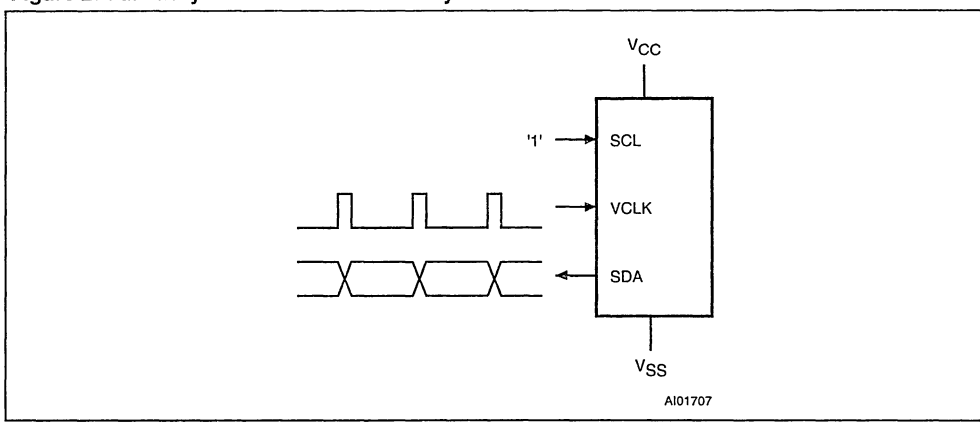
Each member of the ST24xy21 family operates in the two modes of the VDDC specification. The "Transmit Only" mode of the ST24xy21 corresponds to the "DDC1" mode of the VDDC, and the "I^2C Bidirectional" mode corresponds to the "DDC2B" mode.

All members of the ST24xy21 family power-up in DDC1 mode. The device will switch to the DDC2B mode upon the falling edge of the signal applied on SCL pin. Once in the DDC2B mode, the ST24LC21B and ST24LW21 cannot switch back to the DDC1 mode, except by first removing the power supply. However, the ST24FC21 and ST24FW21 enter a transition state after the falling edge of SCL, during which the device will switch back to the DDC1 mode if no valid I^2C activity is observed.

DDC1: Transmit Only Mode

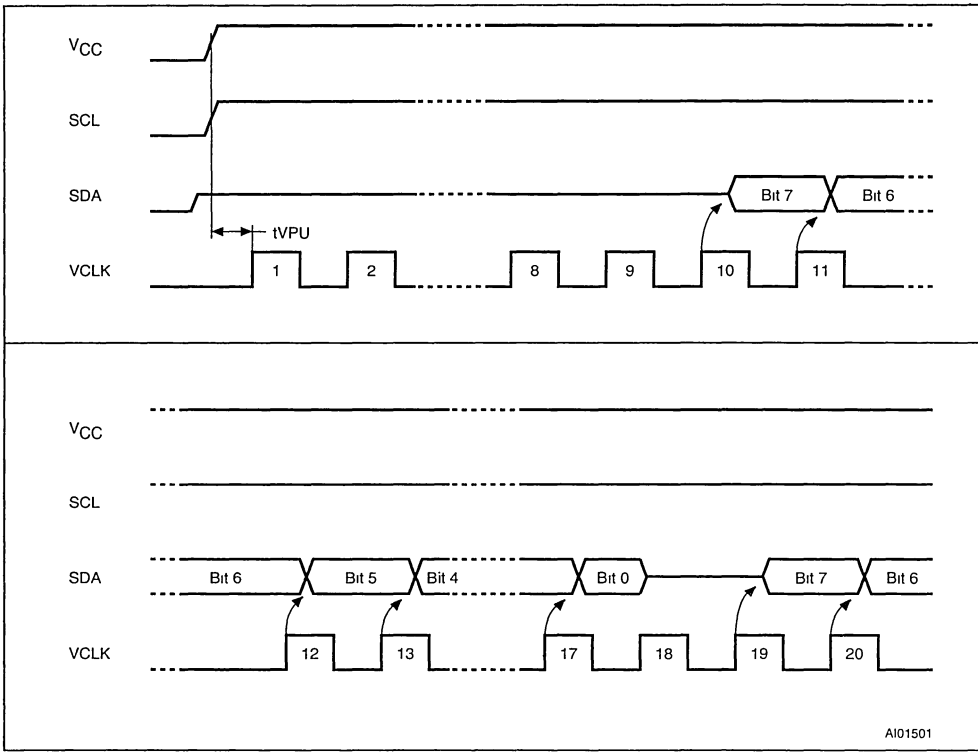
Figure 2 shows how, in the DDC1 mode, the ST24xy21 uses the VCLK input as a clock and the SDA line for data output. The EEPROM data are clocked out on the rising edge of VCLK signal (pin 7). The SCL input must be held high.

Figure 2. Summary of the Use of the ST24xy21 in the DCC1 Mode



First, though, the device passes through an initial, internal, synchronization sequence, as depicted in Figure 3. VCLK is given nine free clock cycles, during which the SDA pin is held in its high impedance state. On the rising edge of the tenth VCLK pulse, the device starts to output, on the SDA line, the data byte that is located at address 00h. This is transmitted serially, during the next nine clock cycles. The first eight cycles are used for transmitting the data bits themselves, with the most significant bit first. During the ninth cycle, the SDA line is held in its high impedance state. This last bit, therefore, is readable as a logic '1' due to the pull-up resistor on the SDA line.

Figure 3. Timing Diagram for the DDC1 Mode



The internal address register is incremented automatically, and the data at the next location is transmitted during the next nine clock periods. This cycle continues indefinitely, so long as the SCL line is held high, with the address wrapping round from 7Fh (the 127th byte) back to 00h.

Unlike the DDC2B mode, the DDC1 mode does not provide for the issuing of instructions or commands to the memory, and does not provide for the writing of data.

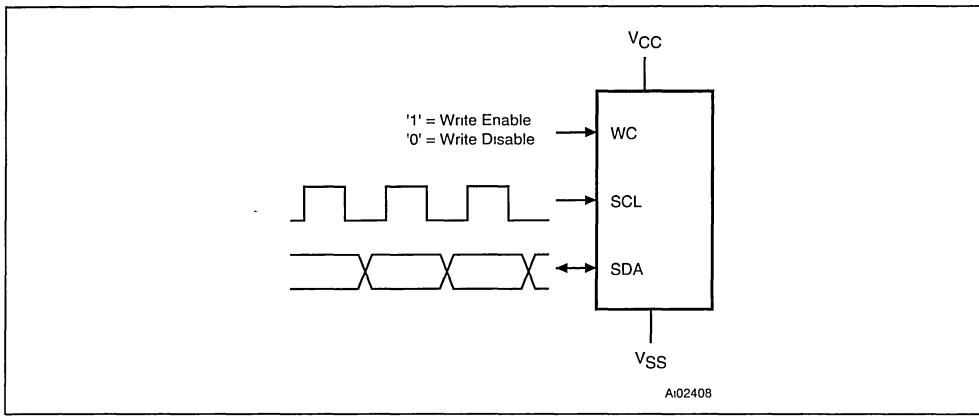
The detection of a logic '0' for the ninth bit indicates that the memory has lost synchronization, and that the data are no longer valid. It is then necessary to re-synchronize the communication by turning off the power to the memory, and then back on again, or by checking the synchronization block of data written in the ST24xy21 device.

DDC2B: I²C Bidirectional Mode

The I²C standard two-wire serial interface includes a bidirectional data line (SDA) and a serial clock (SCL), as indicated in Figure 4. In addition, the whole ST24xxx and ST25xxx family offers a write control feature, as described in Application Notes *AN404* and *AN1006*. For the ST24xy21 family, this is appears as described in the following list:

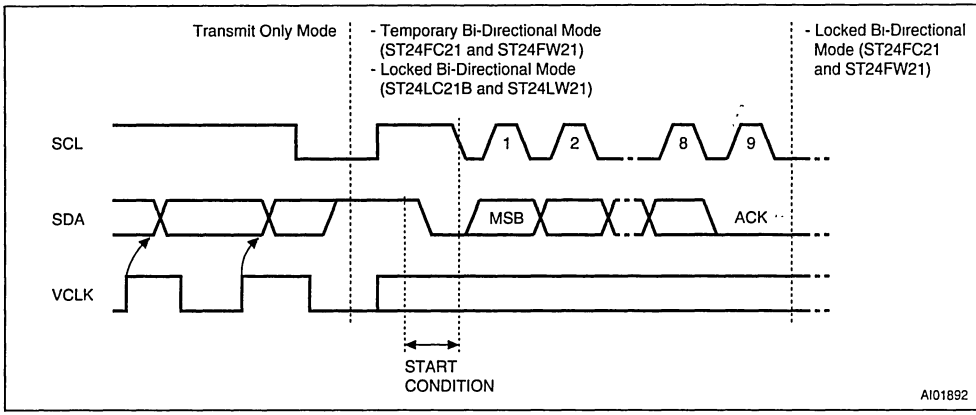
- When the ST24LC21B or ST24FC21 is in the DDC2B mode, the VCLK input (pin 7) acts as the write enable/$\overline{\text{disable}}$ control.
  - When VCLK = 1, write instructions are permitted
  - When VCLK = 0, write instructions are ignored.
- When the ST24LW21 or ST24FW21 is in the DDC2B mode, the Write Control input (WC), pin 3, acts as the write enable/$\overline{\text{disable}}$ control.
  - When WC = 1, write instructions are permitted
  - When WC = 0, write instructions are ignored.

Figure 4. Summary of the Use of the ST24xy21 in the DCC2B Mode



The ST24xy21 is switched from the DDC1 mode to the DDC2B mode by taking the SCL pin low, as indicated in Figure 5.

Figure 5. Timing for the Transition from DDC1 Mode to DDC2B Mode



The ST24xy21 takes the role of the slave device in the I^2C protocol, with all memory operations synchronized by the serial clock, SCL. The VCLK input (pin 7) is ignored during read accesses, but for the ST24FC21 and ST24LC21B, it has an effect on write accesses, as described on page 7.

Table 2 shows that all read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 device select bits (transmitted with the most significant bit first), plus one read/write bit, and is terminated by an acknowledge bit.

Table 2. Device Operations

Mode	R/$\overline{W}$ bit	ST24LC21B ST24FC21 VCLK/WC[1]	ST24LW21 ST24FW21 WC[1]	Bytes	Initial sequence
Current address read	1	X	X	1	START, device select, R$\overline{W}$ = 1
Random address read	0	X	X	1	START, device select, R$\overline{W}$ = 0, address
	1	X	X		reSTART, device select, R$\overline{W}$ = 1
Sequential read	1	X	X	≥ 1	Similar to current or random read
Byte write	0	VIH	VIH	1	START, device select, R$\overline{W}$ = 0
Page write	0	VIH	VIH	8	START, device select, R$\overline{W}$ = 0

1. X = Don't Care = VIH or VIL

Table 3 shows how the stream of 7 device select bits is composed of the 4 bit Device Select code (built-in with the value 1010) followed by 3 Don't Care bits (X indicating that the bit can be either '0' or '1').

Table 3. Device Select Code in the DDC2B Mode

	Device code				Chip enable			$R\overline{W}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device select	1	0	1	0	X	X	X	$R\overline{W}$

When the bus master writes data to the memory, the ST24xy21 responds to the eight received data bits by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it must acknowledge the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition (as described in descriptions of the READ and WRITE sequences in the *ST24XY21* data sheet).

CONTROL OF THE WRITE OPERATION

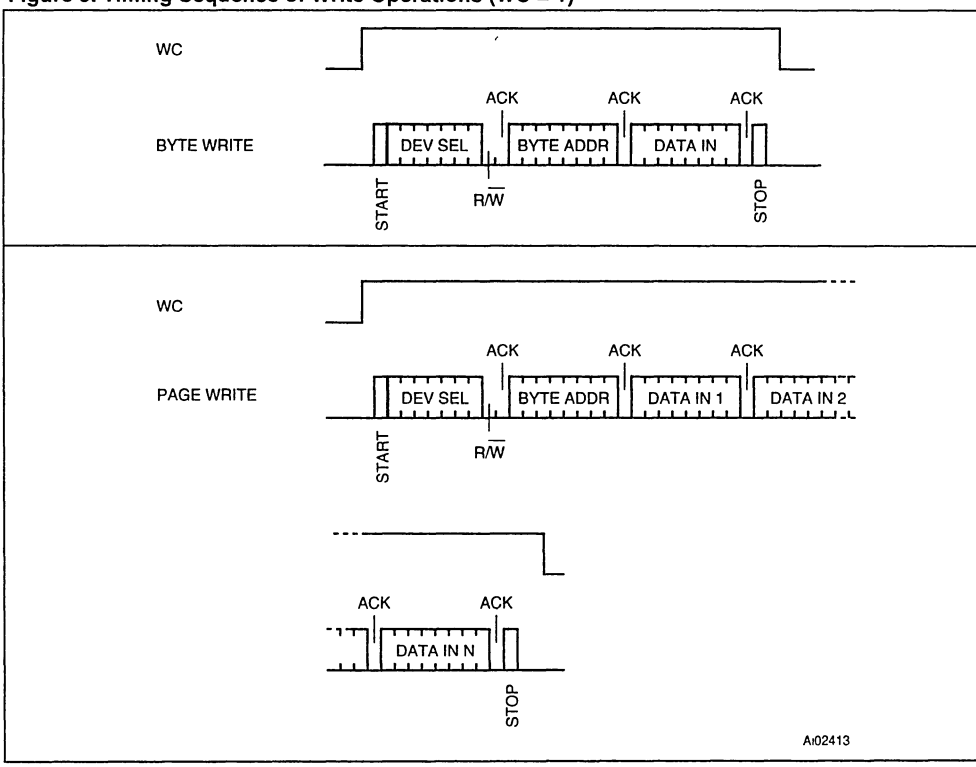
Hardware control of the write operation, using the WC input, is a useful facility for protecting the contents of the memory from inadvertent erase/write cycles (in the DDC2B mode). Not only does the device ignore the write operation if WC is not high at the start of the operation, but it aborts the operation if WC ceases to be held high, perhaps because of a noise glitch on the WC line. That is, the device errs on the side of safety, and protects itself against writing if there is any question as to the validity of the incoming data.

Table 4. Availability of the Write Control Input

	ST24FC21 ST24LC21B	ST24FW21 ST24LW21
DDC2B, I^2C Bidirectional Mode	pin 7 = WC	pin 7 = Don't Care pin 3 = WC
DDC1, Transmit Only Mode	pin 7 = VCLK	pin 7 = VCLK pin 3 = Don't Care

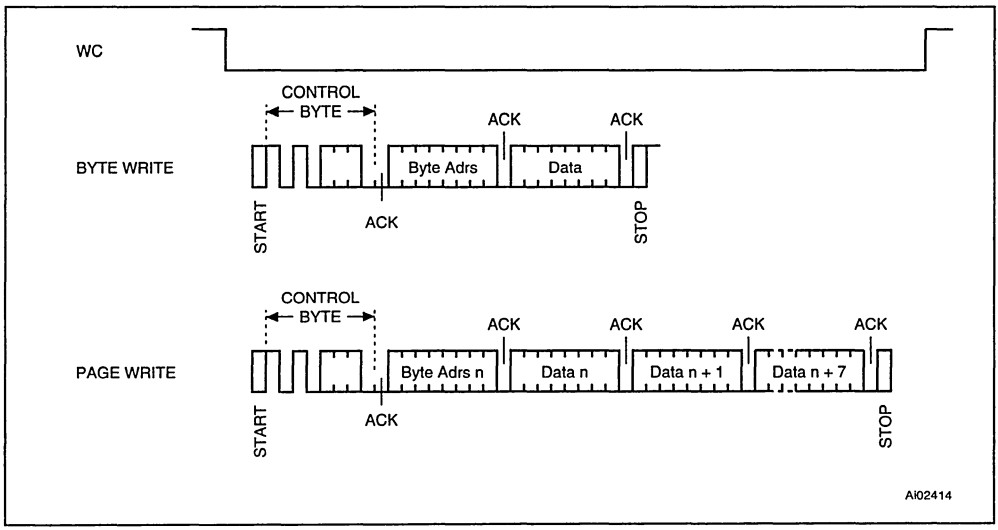
The availability of the WC input is summarized in Table 4. Writing is enabled when WC is held at VIH, and disabled when it is held at VIL. Figure 6 shows the timing of the byte-write and page-write operations, and shows how the level on the WC input must be taken high before commencing the START condition, and must be held high until after the STOP condition has finished.

Figure 6. Timing Sequence of Write Operations (WC = 1)



Write operations are ignored when WC is taken low, as depicted in Figure 7. However, the timing remains the same, with nine clock cycles per data byte, including an acknowledge bit at the end of each.

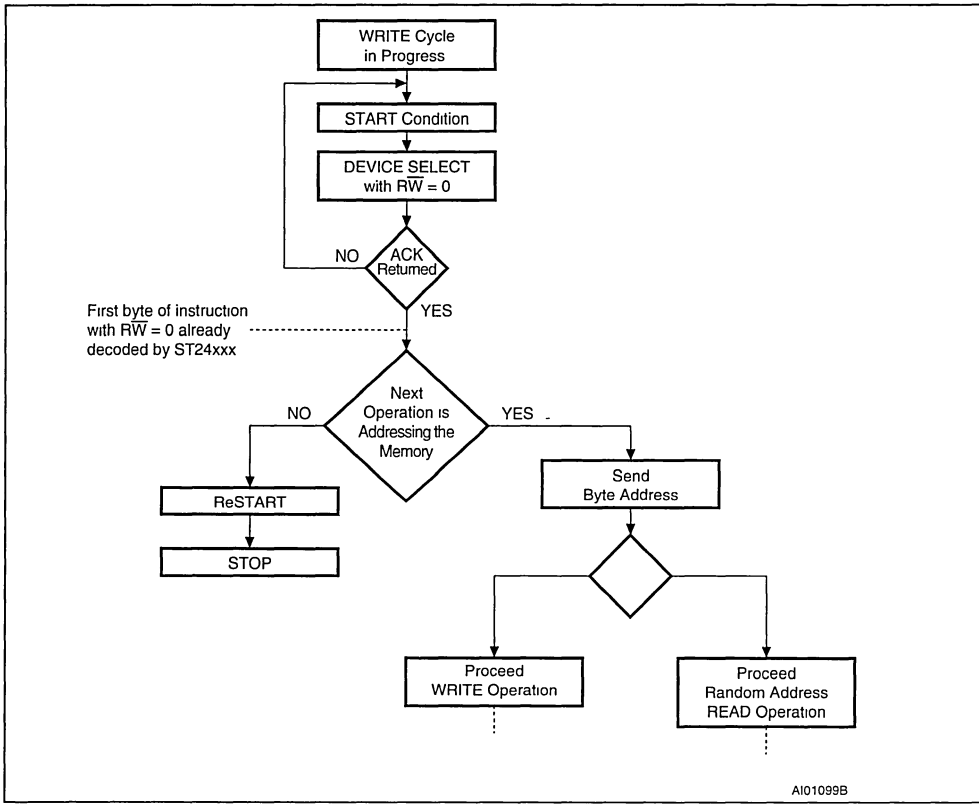
Figure 7. Timing Sequence of Inhibited Write Operations (WC = 0)



Because the device is designed to abort from a write operation if there is any question as to the validity of the incoming data, it is recommended that the status of the write operation be checked at completion.

The algorithm in Figure 8 shows an algorithm in which a test is made at the start of the write operation, to check that device has been correctly initiated. If the memory sends back the acknowledge after the first loop, no write cycle is in progress. This means that either the write sequence was corrupted by glitches or the signal applied on WC was not stable at VIH during the write sequence. This ACK polling algorithm must be used just after the write sequence because the memory will not send back the acknowledge while the internal write cycle is in progress.

Figure 8. The ACK Polling Algorithm (to check that the write cycle has started correctly)



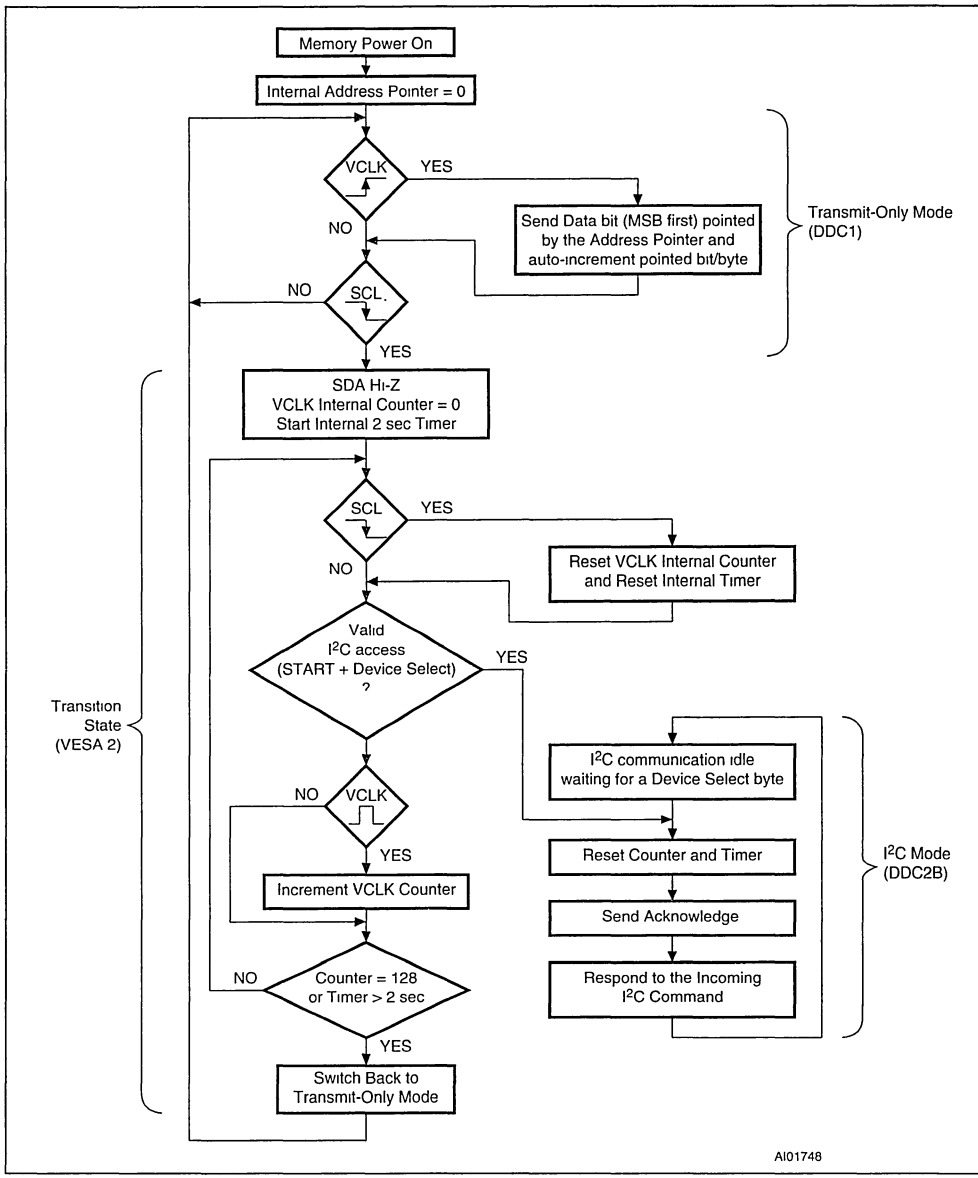
ERROR RECOVERY MODES (AVAILABLE ON ST24FC21 AND ST24FW21)

When the ST24FC21 or ST24FW21 first switches to the DDC2B mode, it enters a transition state, as shown in Figure 9.

If the device does not receive a valid I^2C sequence, that is a START condition followed by a valid Device Select code (1010XXX RW), within either 128 VCLK periods or a period of time of tRECOVERY (approximately 2 seconds), the device will return to the DDC1 mode. Whenever there is a high to low transition on the SCL input, the counter of the VCLK line and the tRECOVERY watchdog timer are both reset. If more than 128 VCLK pulses or tRECOVERY elapses between successive high to low transitions of SCL, the device returns to the DDC1 mode.

If, though, the device receives a valid I^2C sequence, it locks itself in the DDC2B mode.

Figure 9. Error Recovery Mechanism Flowchart (for the ST24FC21 and ST24FW21)



TYPICAL APPLICATION SCHEMATIC

The ST24xy21 is used in a Plug-and-Play PC display to transmit all the display information needed by the host PC in the DDC1 and DDC2B modes. In particular, during the PC boot-up and configuration process, the system software interrogates the display as to its capabilities and operating parameters.

The physical specification for the connector, between the display and the host PC graphics controller, is backward compatible to that of the standard 15-pin, VGA-type, connector. The pin-out of the VGA connector is described in Table 5. This shows how the host PC and the display connections vary, depending on the VDDC standard available in the host PC graphics controller.

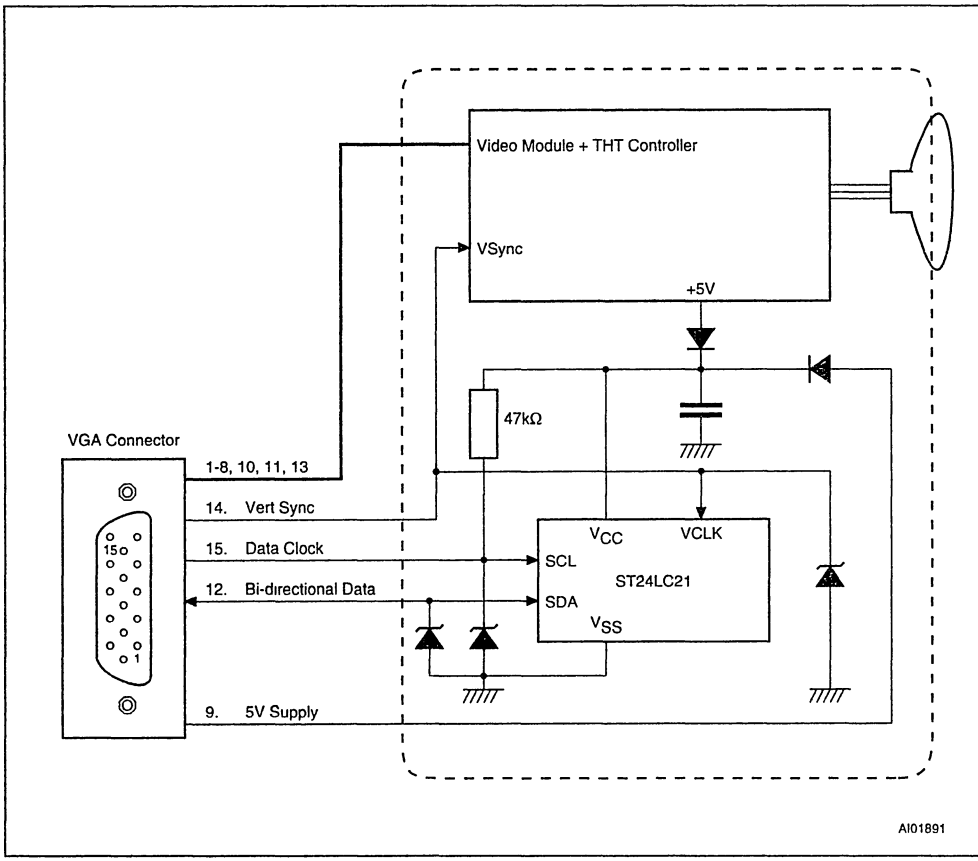
Table 5. 15-pin VGA Connector Pin-out Description

Pin	Standard VGA	DDC1 host PC	DDC2B host PC	DDC1/2B display
1	Red video	Red video	Red video	Red video
2	Green video	Green video	Green video	Green video
3	Blue video	Blue video	Blue video	Blue video
4	Display ID bit 2	Display ID bit 2	Display ID bit 2	Optional
5	Test (ground)	Return	Return	Return
6	Red video return	Red video return	Red video return	Red video return
7	Green video return	Green video return	Green video return	Green video return
8	Blue video return	Blue video return	Blue video return	Blue video return
9	no connection (mechanical key)	5 V supply	5 V supply	5 V supply
10	Sync return	Sync return	Sync return	Sync return
11	Display ID bit 0	Display ID bit 0	Display ID bit 0	Optional
12	Display ID bit 1	Data from display	Bidirectional data (SDA)	Bidirectional data (SDA)
13	Horizontal sync	Horizontal sync	Horizontal sync	Horizontal sync
14	Vertical sync	Vertical sync (VCLK output)	Vertical sync	Vertical sync (VCLK output)
15	Display ID bit 3	Display ID bit 3	Data clock (SCL)	Data clock (SCL)

According to Version 2.0 of the VESA Data Display Channel specification, the host PC graphics controller board needs to provide a 2.2 kΩ pull-up resistor on the bidirectional data line (SDA), and on the data clock line (SCL), to ensure correct switching between the DDC1 and DDC2B modes. The display PCB board also needs to provide a 47 kΩ pull-up resistor on the data clock line (SCL).

Figure 10 depicts a typical PC display application schematic using a member of the ST24xy21 family. The DDC1 clock signal, VCLK, is connected to pin 14 of the VGA connector. The data clock line, SCL, used for the DDC2B mode, is connected to pin 15 and the bi-directional data line, SDA, is connected to pin 12.

Figure 10. Schematic of a Typical PC Display Application



For the VESA 2.0 specification, a +5V supply voltage generated by the host PC is available on the pin 9 of the VGA connector (used for the ACCESS.bus protocol). This +5 V supply voltage may be used to supply the Vcc voltage of the ST24xy21. This allows a proper power-up sequence, driven only by the host PC. If the host PC and the display are powered-on asynchronously, the first to come on will power the ST24xy21 inside the display.

The SCL (the DDC2B clock) and SDA (data) pins of the ST24xy21 can be directly connected to the VGA connector. An ESDA6V1 transil array may be used in order to improve the memory protection against electrostatic discharge (ESD) and latch-up.

Diode protection is advisable on the signals that connect directly between the ST24xy21 and the external VGA connector. However, it is not necessary to provide external protection against slow rise and fall times or bounces, since the members of the ST24xy21 already contain TTL-compatible Schmitt-Triggers on these inputs.

POWER SUPPLY VOLTAGE IN THE VESA 2.0 SPECIFICATION

According to the VESA 2.0 specification, the ST24xy21 can be supplied by either the display or by the host PC power supply (using the +5 V line, pin 9, on the VGA cable). The easiest way to implement this is to use two diodes, as shown in Figure 10.

The ST24xy21 supply voltage is decreased by the diode forward voltage drop (about 0.6 V) and hence below 4.5 V. Nevertheless, the ST24xy21 remains operational, and no input will be damaged if the applied voltage on each input complies with the Absolute Maximum Ratings values. However, the threshold voltage of the Schmitt-Trigger (pin 7) needs to be decreased in this case (as described in the *ST24xy21* data sheet).

NOTES

ALPHABETIC INDEX

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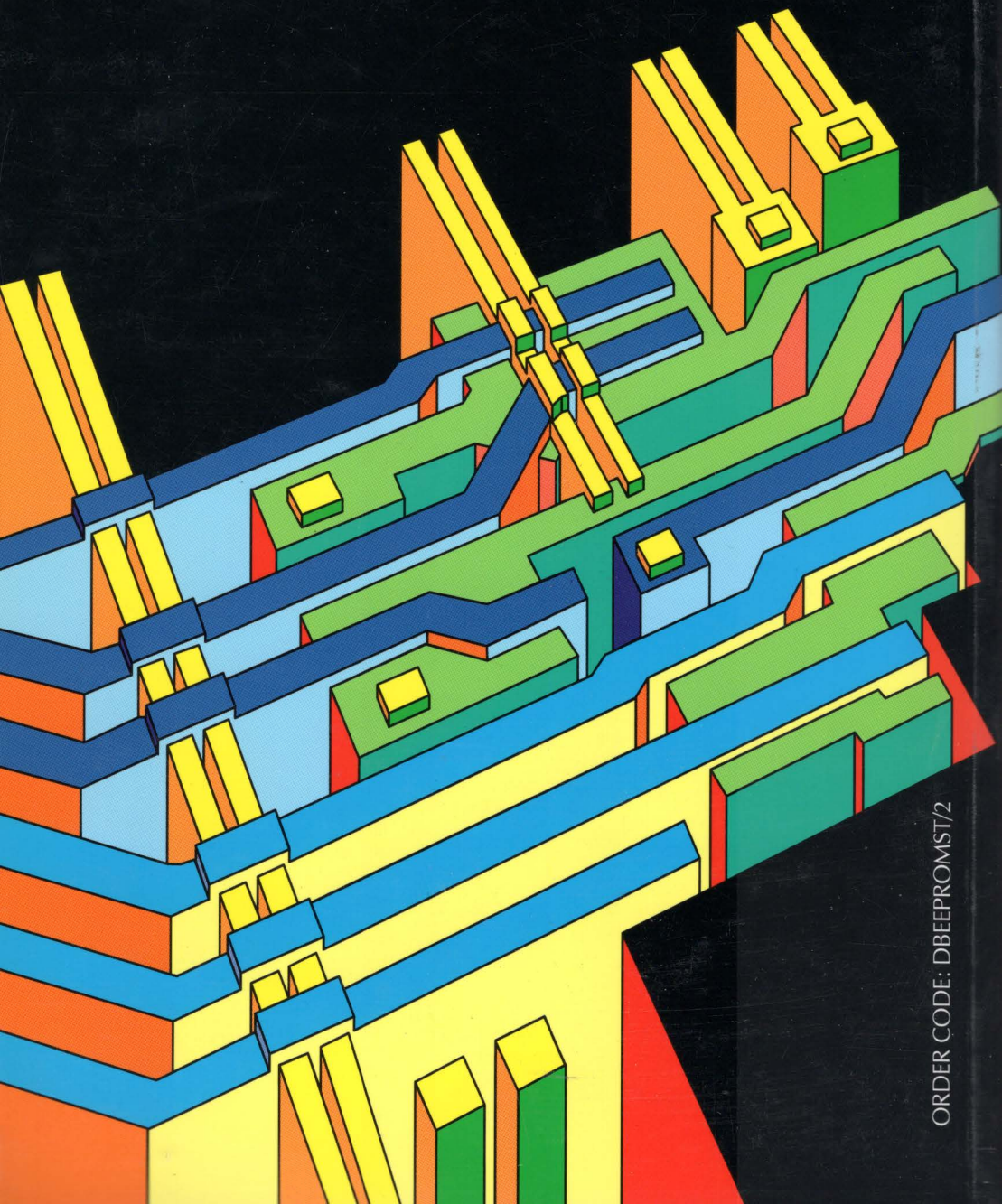

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