signetics

MICROPROCESSOR
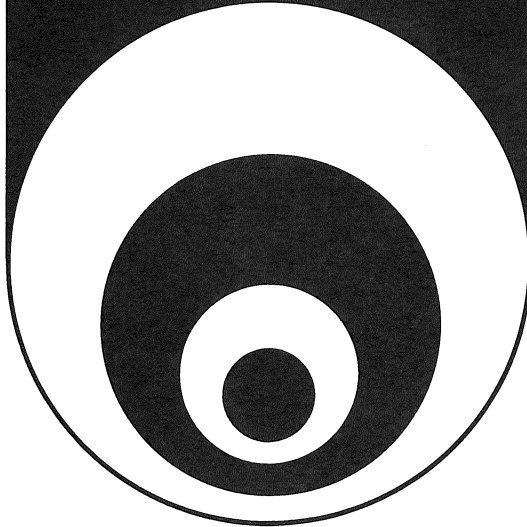
SERIAL INPUT/OUTPUT...............AS50

INTRODUCTION

The Sense/Flag capability of the Signetics 2650 microprocessor can be used for serial I/O interfaces. The Sense input pin is directly connected to a bit in the microprocessor's Program Status Word. A high level on the Sense pin appears as a binary one while a low level appears as a binary zero. The Sense bit in the PSW can be stored or tested by the program. The Flag bit in the PSW is a simple latch that drives the Flag output pin. A program can set the Flag bit to a binary one, which causes a high level, one TTL load on the flag output pin. Setting the Flag bit to binary zero causes a low level on the Flag output pin.

APPLICATIONS

The most common use for the Sense/Flag capability would be in interfacing to a keyboard based terminal where the data is received or transmitted as bit serial. All bit manipulation and timings such as 8-bit serial-to-parallel conversion can be done by software running on the 2650. The software works by storing or setting the two bits in the Program Status Word which reflect or control the levels at the pins of the chip. External hardware is required simply to interface with line levels. No clock synchronization or address decoding hardware is necessary, since the Sense and Flag pins are independent of the normal I/O bus structure.

Two examples of device interfaces and software are given below; for a 1200 baud RS232-type CRT terminal and for a 110 baud Teletype. Figure 1 shows the RS232 interface. Half of the Signetics 8T15 dual line driver is used to transmit to the terminal from the Flag pin, while half of a

FIGURE I
RS-232 INTERFACE

Signetics 8T16 dual line receiver is used to receive from the device into the Sense pin. The interface to a Teletype model 33 is shown in Figure II. A TTL open collector gate is used to provide the 20 milli-amp loop to the TTY

FIGURE II
TTY MODEL 33 INTERFACE FULL DUPLEX
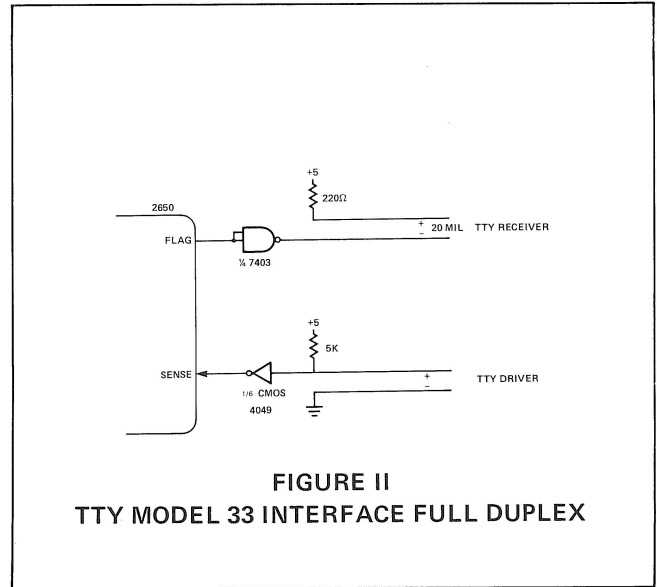
receiver. For receiving from the TTY a CMOS gate is used to provide the necessary noise immunity.

SOFTWARE

All definitions of baud rate, character formats, and line characteristics are done in the software. For these examples, communication is asynchronous bit-serial over a full duplex line. Figure III shows the format of a 8-bit character (seven bits plus parity) headed by a start bit and followed by stop bits. The line levels are:

    low = start bit or binary zero
    high = stop bit or binary one

FIGURE III
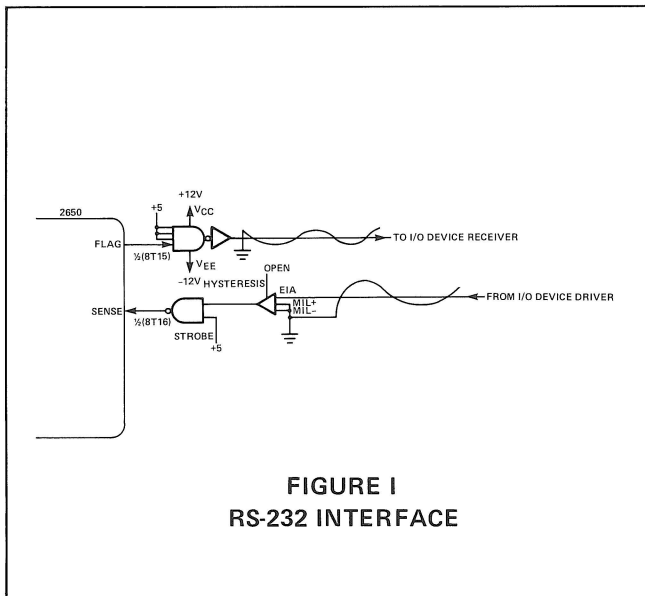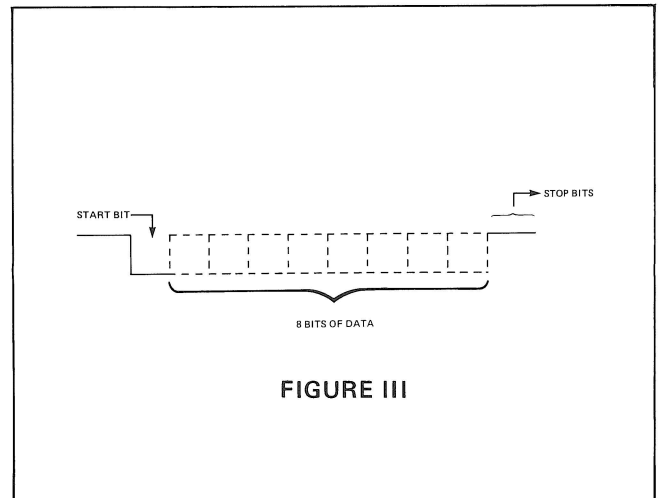
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PIP ASSEMBLER VERSION 2 LEVEL 1                           PAGE    1
LINE  ADDR  LABL  B1 B2 B3 B4 ERROR SOURCE

 1          0001              *
 2          0002              P      EQU      1
 3          0000              N      EQU      2
 4          0002              Z      EQU      0
 5          0002              CCOM   EQU      H'02'       LOGICAL COMPARE
 6          0001              CAR    EQU      H'01'       CARRY
 7          0080              SENS   EQU      H'80'       SENSE
 8          0040              FLAG   EQU      H'40'       FLAG
 9          0020              II     EQU      H'20'       INTERRUPT INHIBIT
10          0020              IDC    EQU      H'20'       INTER DIGIT CARRY
11          0004              OVF    EQU      H'04'       OVEFFLOW
12          0000              R0     EQU      0
13          0001              R1     EQU      1
14          0002              R2     EQU      2
15          0003              R3     EQU      3
16          0003              UN     EQU      3
17          0000              EQ     EQU      0
18          0002              LT     EQU      2
19          0001              GT     EQU      1
20          0008              WC     EQU      H'08'
21          0010              RS     EQU      H'10'
22                            ORG      H'500'
23  0500    0500  76 40       CHIO   PPSU     FLAG        INPUT WITH A BIT BY BIT ECHO
24  0502          75 08              CPSL     WC
25  0504          05 00              LODI,R1  0
26  0506          06 08              LODI,R2  8
27  0508    0508  12          TEST   SPSU                 LOOP TESTS FOR THE START BIT
28  0509          1A 7D              BCTR,LT  TEST
29  050B          3F 05 29           BSTA,UN  DLY         HALF A DELAY TO MIDDLE OF BIT
30  050E          74 40              CPSU     FLAG
31  0510    0510  3F 05 2D    BIT    BSTA,UN  DLAY        DELAY, THEN READ THE NEXT BIT
32  0513          12                 SPSU
33  0514          44 80              ANDI,R0  H'80'
34  0516          51                 RRR,R1
35  0517          61                 IORZ     R1
36  0518          C1                 STRZ     R1
37  0519          1A 04              BCTR,LT  ZERO        ECHO THE BIT
38  051B          74 40              CPSU     FLAG
39  051D          1B 02              BCTR,UN  NEXT
40  051F    051F  76 40       ZERO   PPSU     FLAG
41  0521    0521  FA 6D       NEXT   BDRR,R2  BIT
42  0523          3F 05 2D           BSTA,UN  DLAY
43  0526          45 7F              ANDI,R1  H'7F'
44  0528          17                 RETC,UN
45
46                            *  TIMING DELAY FOR 1200 BAUD RS232 TERMINAL
47  0529    0529  04 3A       DLY    LODI,R0  H'3A'
48  052B          1B 02              BCTR,UN  DL1
49  052D    052D  04 59       DLAY   LODI,R0  H'59'
50  052F    052F  F8 7E       DL1    BDRR,R0  $
51  0531          17                 RETC,UN
52                            *  TIMING DELAY FOR 110 BAUD TELETYPE
```

```
PIP ASSEMBLER VERSION 2 LEVEL 1                           PAGE    2
LINE  ADDR  LABL  B1 B2 B3 B4 ERROR SOURCE

53  0532    0532  20          TDLA   EORZ     R0
54  0533          F8 7E              BDRR,R0  $
55  0535          F8 7E              BDRR,R0  $
56  0537    0537  F8 7E       TDLY   BDRR,R0  $
57  0539          04 E5              LODI,R0  H'E5'
58  053B          F8 7E              BDRR,R0  $
59  053D          17                 RETC,UN
60                            END


TOTAL ASSEMBLER ERRORS =     0
```

FIGURE IV

The internal logic of the program shown in Figure IV (the program listing) is to sense each incoming bit of the character and to output the bit in turn for the full duplex line. The Sense input is tested in the loop at 'TEST' for the transition to zero indicating the start bit. The program then delays one half of a bit time to the center of the start bit. At this point the echoing of the character starts by clearing the Flag bit which outputs the start bit transition. At 'BIT' the program then delays one full bit time to the center of the data bit. The Sense line is tested and that bit value is rotated into register one. The bit value is then used to set or clear the Flag bit for the echo. At 'NEXT' is the test that controls the loop to get only eight bits. Figure V is a picture of the levels and timings when echoing a 'U'.

The bit timing is done by a subroutine which simply counts cycles for the appropriate baud rate. The example program shows both a 1200 baud delay at 'DLAY' and a 110 baud delay at 'TLAY'. The conversion from instruction cycles to milliseconds is based on a 1MHz clock rate. Clock stability is only moderately important since each character involves only nine sample times and each start bit redefines the base line for all timings.
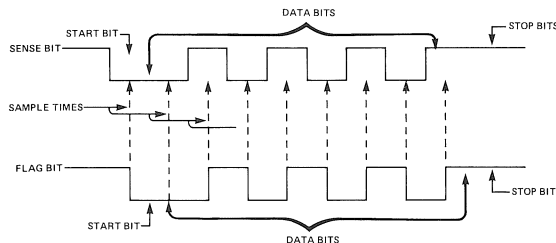

FIGURE V

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