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2650 EVALUATION PRINTED CIRCUIT BOARD LEVEL SYSTEM (PC1001)....................SP50

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2650 EVALUATION PRINTED CIRCUIT BOARD (PC1001)

SP50

APPLICATIONS MEMO

GENERAL

The PC1001 is an evaluation and design tool for the 2650 microprocessor. Each PC1001 board has a 2650 microprocessor, 1k bytes of RAM, 1k bytes of PROM loaded with PIPBUG*, a crystal clock, and sufficient additional logic to allow the user to exercise all aspects of the 2650 microprocessor. There is a serial I/O port on the board that can be used to drive a current loop driven terminal or an RS232 type terminal. The PC1001 provides the system engineer with a very flexible design tool from which he can easily develop a pre-production prototype of his product designed around the 2650 microprocessor.

FEATURES

The PC1001 has many features that make it a valuable design aid. The most noteworthy features are:

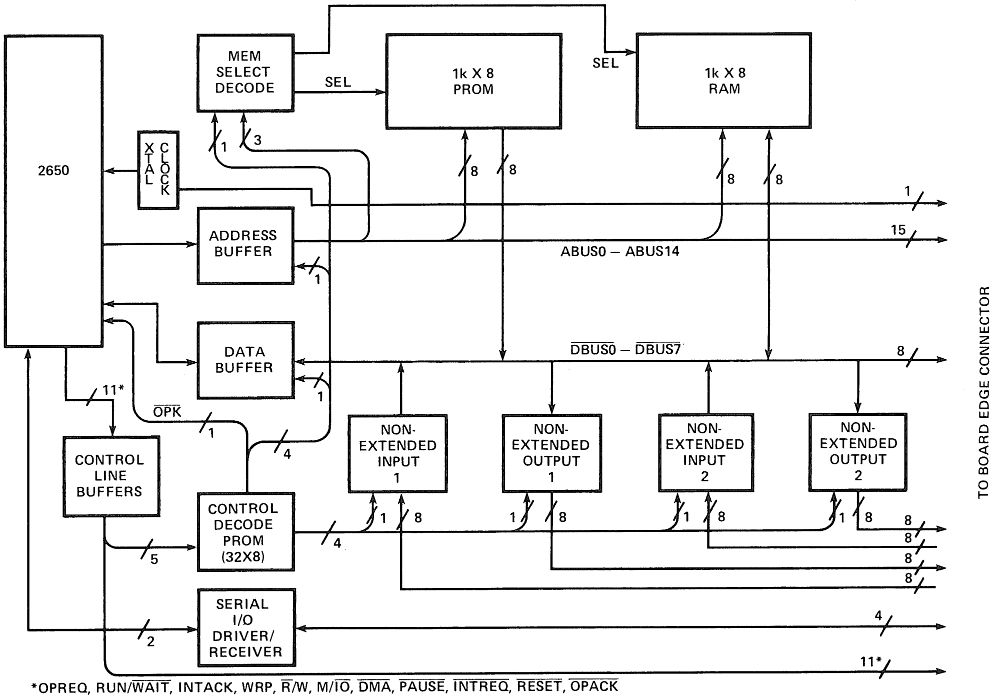
- The Signetics 2650 N-MOS, 8-bit microprocessor
- 1k – bytes of RAM memory
- 1k – bytes of PROM memory
- A 1MHz crystal oscillator
- A serial I/O channel
- Two Non-Extended 8-bit parallel input ports
- Two Non-Extended 8-bit parallel output ports
- Buffered address, data, and control lines for implementing additional 8-bit parallel I/O ports or expanded memory
- Direct Memory Access (DMA) capability, including the memory on the PC1001 board
- Display indicators on the board for the RUN/$\overline{\text{WAIT}}$, OPREQ, M/$\overline{\text{IO}}$, R/$\overline{\text{W}}$ control lines, and the Non-Extended output ports
- Vectored interrupts
- A program debug module (called PIPBUG) written for use with the 2650

*PIPBUG – a program debug module

DESCRIPTION

The PC1001 is configured as a very flexible, general purpose microprocessor board to allow the system designer to easily expand memory, implement input/output functions and execute programs written for the 2650. A functional description of the PC1001 is given in this section. A functional block diagram of the PC1001 is shown in Figure 1.

PC 1001 BLOCK DIAGRAM



*OPREQ, RUN/$\overline{\text{WAIT}}$, INTACK, WRP, $\overline{\text{R}}$/W, M/$\overline{\text{IO}}$, $\overline{\text{DMA}}$, $\overline{\text{PAUSE}}$, $\overline{\text{INTREQ}}$, $\overline{\text{RESET}}$, $\overline{\text{OPACK}}$

FIGURE 1

CPU

The 2650 is the heart of the PC1001, executing instructions from memory and controlling the I/O functions. The address, data, and control lines of the 2650 are buffered and available at the edge connector of the PC1001. The onboard bus drivers allow the user to build a microprocessor system around the PC1001 without additional buffering. The tri-state function of the 2650 address and data busses is transferred to the buffer gates which drive the lines used by the system designer. The address and data bus buffers are in the tri-state mode whenever the OPREQ line from the 2650 is a logic ZERO.

MEMORY

The 1024 bytes of read only memory are implemented with 82S129 256X4 bipolar PROM's. The PROM's are accessed by addressing the first 1024 bytes of the address space (locations 0_{16} – $3FF_{16}$). The PROM's are mounted in sockets on the PC1001 board and are loaded with the PIPBUG debug program. The sockets on the PC1001 board allow the user to put different 82S129 PROM's in the first 1k bytes of the memory address space when developing a prototype system.

The 1024 bytes of random access memory are implemented with 2606 256X4 MOS RAM's. The RAM's are accessed by addressing the second 1024 bytes of the address space (locations 400_{16} – $7FF_{16}$).

PARALLEL I/O

The buffered address, data, and control lines available to the user of the PC1001 allow any of the 2650 parallel I/O modes to be implemented, or to expand memory beyond the 2k bytes already on the board. The extended I/O instructions provide device select capability for 256 I/O functions by decoding the least significant 8-bits of the address bus (ABUS 0 – ABUS 7). The buffered data bus is a bi-directional tri-state bus so that input devices may use the data bus by driving it with tri-state drivers.

If the Non-Extended I/O instructions are used, two latched output ports and two gated input ports are already provided on the PC1001, and no control line decoding is necessary.

When the 2650 executes memory reference instructions or Non-Extended I/O instructions, the control decode PROM generates the operation acknowledge signal ($\overline{\text{OPACK}}$) in response to operation request (OPREQ). When the 2650 executes Extended I/O instructions, the selected I/O device must generate $\overline{\text{OPACK}}$. By requiring the I/O device to return the $\overline{\text{OPACK}}$ signal, the PC1001 gives the user the flexibility of connecting peripheral functions that may require more than one microsecond to respond to an I/O request. If the Extended I/O functions are all faster than one microsecond they will not slow down the 2650, and $\overline{\text{OPACK}}$ may be tied to logic ZERO.

SERIAL I/O

The 2650 is equipped with a SENSE input and a FLAG output. These two functions provide a serial I/O data path directly into the 2650. Part of the PIPBUG PROM program is dedicated to implementing an asynchronous serial communications port for the PC1001. The program checks the SENSE line for a start bit from the serial device to achieve synchronization. Once a start bit is detected, the 2650 shifts the next eight character bits into register R0. The PC1001 is designed for full duplex serial I/O, and will echo the transmitted character back to the serial device using the FLAG output. The timing loops that determine when to sample a character bit are written for a ten character per second serial data rate (110 baud), but the 2650 is capable of handling much higher serial data rates.

The serial I/O device used with the PC1001 may be a 20 milliamp current loop device, or it may be RS232 compatible (voltage driven). A current loop driver and receiver, and an RS232 driver and receiver are on the PC1001 board. The type of driver and receiver is selected with a wire jumper. If the RS232 driver and receiver is used, external ±15 volt power supplies are required. If the current loop driver and receiver is used, the PC1001 requires only a single +5 volt power supply.

The PIPBUG debug program includes a read paper tape control function. The program sets a bit in the output register of Non-Extended I/O port C (WRTC instruction) to advance the tape reader one character at a time. This function can be used by modifying a standard teletype to include a tape reader control relay and driving it with the TTY TAPE READER OUT SIGNAL.

It should be pointed out that the tape reader control bit and bit 7 of the Non-Extended I/O port (OPC7) are the same and caution should be exercised to avoid a conflict between the two functions.

CLOCK

The clock circuit on the PC1001 is a hybrid circuit crystal oscillator that runs at a frequency of 1.000 MHz. Instruction loops are used to determine bit times and the crystal controlled clock minimizes errors due to changes in the system clock.

The clock input to the 2650 that is driven by the crystal controlled clock (pin 38) is available at the edge connector of PC1001. If the user chooses to drive the PC1001 with an external clock he must first remove the crystal clock circuit. The clock input to the 2650 is fully TTL compatible and requires no special drive circuitry.

DISPLAYS

Minature LED indicator displays are driven by the three basic control lines (OPREQ, $M/\overline{IO}$, and $R/\overline{W}$), and the Non-Extended output latches. A logic ONE state on the control lines, or in the output latches, "lights" the corresponding LED. The minature LED's are mounted on the PC1001 board and are shown in Figure 2.

PRINTED CIRCUIT BOARD LAYOUT

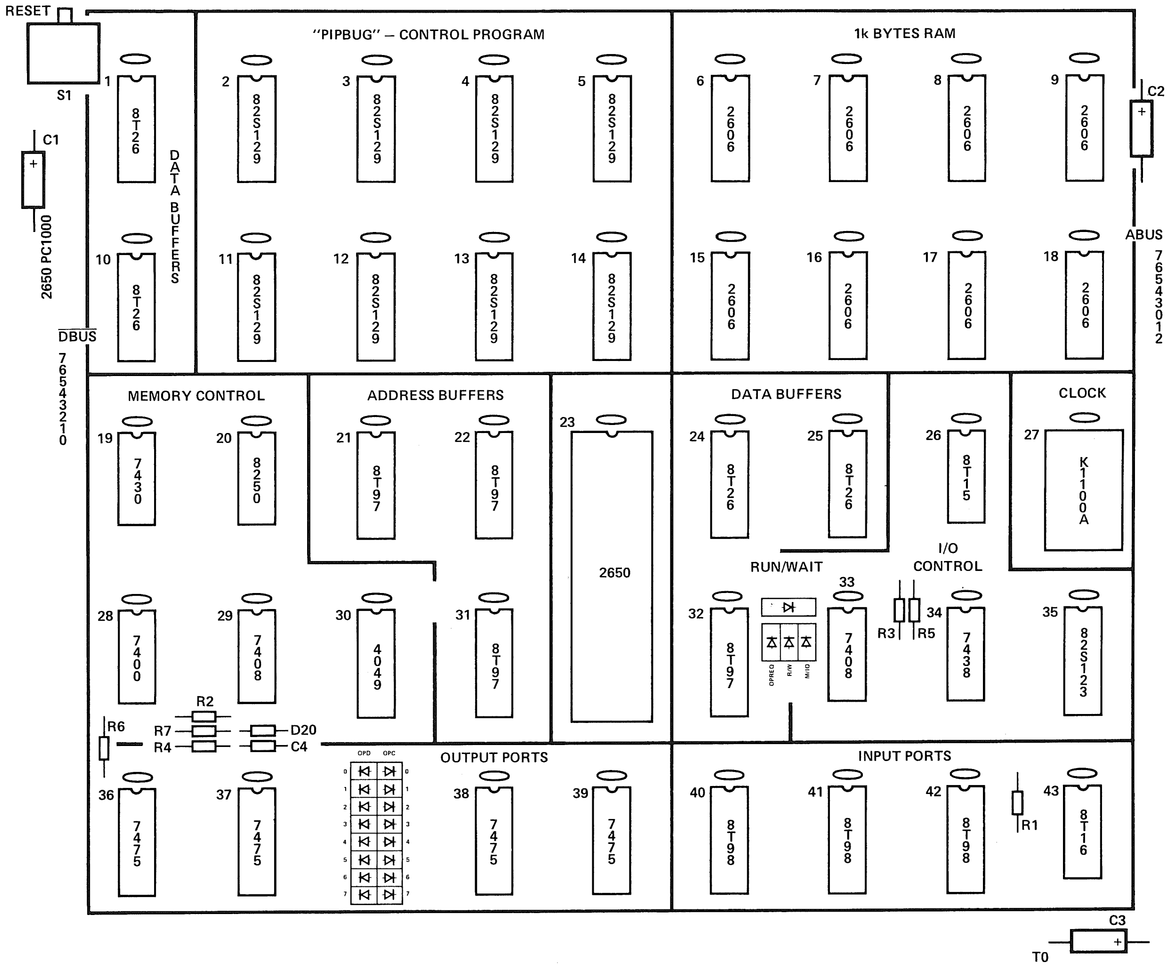


FIGURE 2

DMA

Direct access to memory by an external device (DMA) is easily accomplished with the PC1001. An input to the board is provided for direct memory access and the signal name of that input is DMA (PC1001 pin 14). When DMA is pulled "low" the 2650 finishes executing the current instruction and enters the wait state. To avoid interrupting a memory or I/O transfer in progress the DMA line should not be pulled "low" while OPREQ is "high". When the RUN/WAIT lines goes "low" the external device may drive the address, data, and control lines (except OPREQ, and RUN/WAIT) to accomplish the necessary DMA transfer.

An external operation request line (OPEX) is provided for DMA transfers to the memory on the PC1001 board. Since OPREQ is only driven by the 2650, and is used in the memory select decoders, the user must drive OPEX to access the memory on the PC1001.

Because the DMA function is implemented with the pause feature of the 2650, and since the 2650 is a static device, the length of time that the DMA device may be active for any one transfer is limited only by the other processing responsibilities of the 2650.

INTERRUPTS

The 2650 has a true vectored interrupt system. The user must first drive the interrupt line (INTREQ) on the PC1001, then wait to be acknowledged (INTACK), and finally drive the data bus with a 7-bit signed displacement relative to page zero, location zero. The displacement vector may also indicate indirect addressing, allowing the interrupt service sub-routine to be located anywhere in the 32k-byte address space.

INTERRUPTS (Continued)

The $\overline{\text{INTREQ}}$ line may be driven by several interrupting devices in a "wired OR" configuration. When a priority exists between the various interrupting devices, and to prevent confusion from multiple simultaneous interrupts, the user must arrange the interrupt hardware to resolve priority and simultaneity conflicts.

The PC1001 board comes with PIPBUG stored in the first 1k-bytes of ROM and therefore the user cannot store an interrupt service subroutine or an indirect address in this part of the memory address space. But the interrupt displacement vector may be a negative number referring to the last 64 locations in page zero (1FBF$_{16}$ to 1FFF$_{16}$). If an indirect address or interrupt service subroutine is placed in one of the last 64 locations of page zero, the user must also provide external memory at the locations used (the PC1001 has only 2k-bytes of memory on the board).

There is another way to accomplish a "link" to an interrupt service subroutine through the ROM on the PC1001. It is possible that PIPBUG instructions themselves could provide an indirect address to the second 1k-bytes of RAM on the PC1001 board. An example of a very useable indirect address to an interrupt service routine may be found at locations 8$_{16}$ and 9$_{16}$ of PIPBUG. If these locations are used as an indirect address, the program would branch to location 477$_{16}$ where it would expect to find a subroutine to service the active interrupt.

A timing diagram for interrupt processing is shown in Figure 3, as well as the format for the displacement vector.

LOGIC

The logic on the PC1001 board is uncomplicated and very general purpose. It includes:

1. 2650 CPU and memory
2. Address bus, and data bus drivers and receivers
3. Control line drivers and receivers
4. Control line decode
5. Memory select decode
6. Serial I/O transmitter and receiver
7. Non-Extended parallel I/O latches and receivers

The PC1001 logic drawing will be referred to during this description and is shown in Figure 4. The integrated circuit numbers used in Figure 4 may be cross-correlated to those used on Figure 2 for locating an integrated circuit on the PC1001 board.

CPU and MEMORY

CPU – The address bus, and the data bus from the 2650 are buffered for easy system expansion. With the exception of the address tri-state control line ($\overline{\text{ADREN}}$) and the data bus tri-state control line ($\overline{\text{DBUSEN}}$), all of the control lines from the 2650 are also buffered. The $\overline{\text{ADREN}}$ and $\overline{\text{DBUSEN}}$ lines are tied "low" on the PC1001 board, and the tri-state function of the address, data, and control lines is fulfilled by the buffers.

The clock input is driven directly from the K1100A clock circuit (IC #27). The clock output is available off-board on PC1001 pin 23 (the signal name is CLOCK). The K1100 clock circuit has a frequency stability of ±.01% and will drive 10 standard TTL (7400 series) unit loads. The 2650

INTERRUPT TIMING

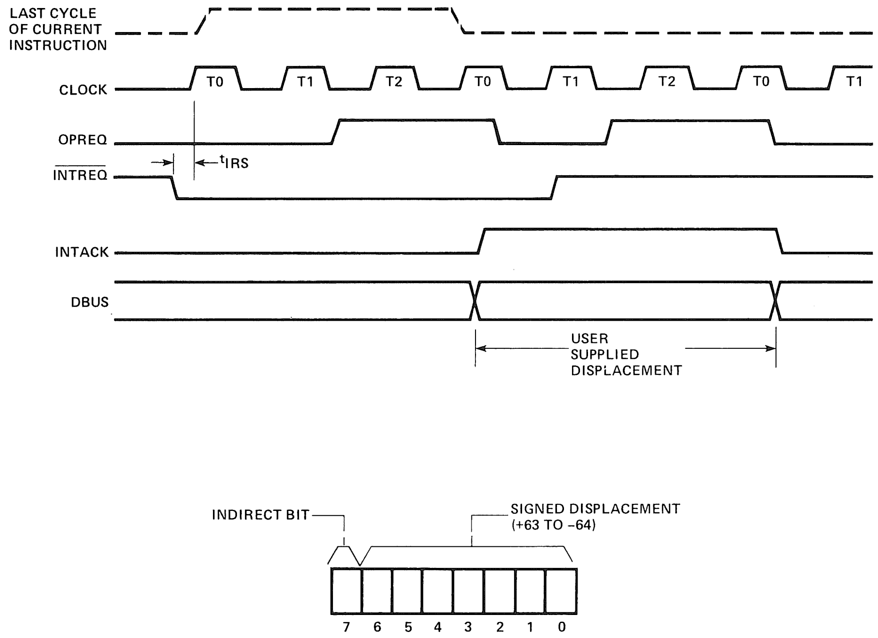
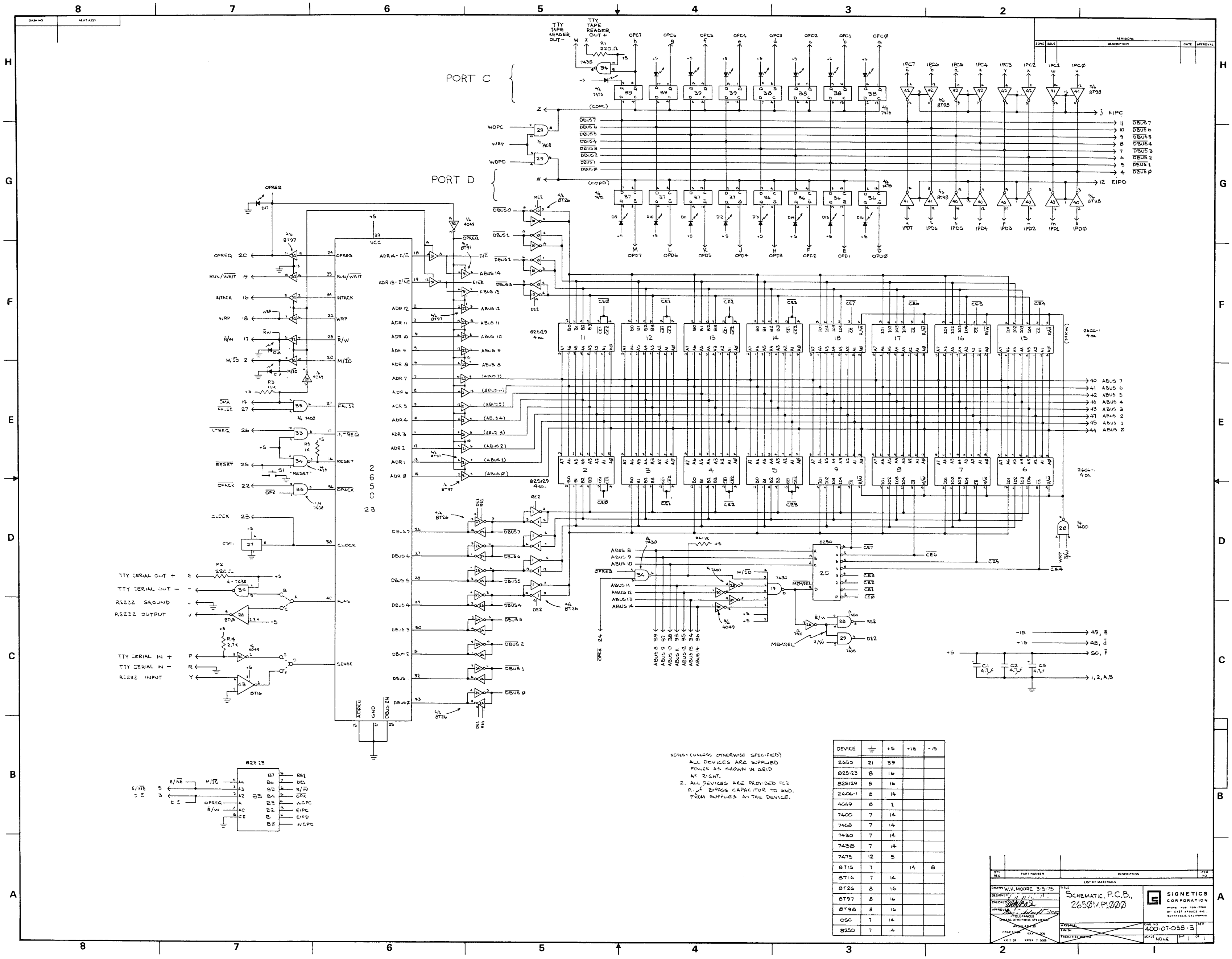

LAST CYCLE OF CURRENT INSTRUCTION
CLOCK
T0
T1
T2
T0
T1
T2
T0
T1
OPREQ
$\overline{\text{INTREQ}}$
t_{IRS}
INTACK
DBUS
USER SUPPLIED DISPLACEMENT
INDIRECT BIT
SIGNED DISPLACEMENT (+63 TO -64)
7
6
5
4
3
2
1
0

FIGURE 3

PC1001 LOGIC DIAGRAM



NOTES: (UNLESS OTHERWISE SPECIFIED)
ALL DEVICES ARE SUPPLIED POWER AS SHOWN IN GRID AT RIGHT.
2. ALL DEVICES ARE PROVIDED FOR 0.1μf BYPASS CAPACITOR TO GND. FROM SUPPLIES AT THE DEVICE.

DEVICE	⏚	+5	+15	−15
2650	21	39		
825123	8	16		
825129	8	16		
2606-1	8	14		
4049	8	1		
7400	7	14		
7408	7	14		
7430	7	14		
7438	7	14		
7475	12	5		
8T15	7		14	8
8T16	7	14		
8T26	8	16		
8T97	8	16		
8T98	8	16		
OSC	7	14		
8250	7	14		

QTY REQ	PART NUMBER	DESCRIPTION	ITEM NO

LIST OF MATERIALS

DRAWN W.H. MOORE 3-5-75
DESIGNER
CHECKED
APPROVED
TOLERANCES UNLESS OTHERWISE SPECIFIED
ANGULAR ± 30'
FRAC ± 1/64 XXX ± .005
XX ± .01 XXXX ± .0005
TITLE Schematic, P.C.B., 2650MP1000
MATERIAL
FINISH
FACILITIES JOB NO
SIGNETICS CORPORATION
PHONE 408 739-7700
811 EAST ARQUES AVE., SUNNYVALE, CALIFORNIA
DWG NO 400-07-058-3
REV
SCALE NONE
SHT 1 OF 1

FIGURE 4

CPU and MEMORY (Continued)

is the only load the clock must drive on the PC1001, using only 10 μamps of its drive capability.

Memory — The memories are of two types: 82S129 256X4 PROMs, and 2606 256X4 RAMs. All 16 memory IC's (IC's 2-9, and 11-18) are addressed by the least significant 8-bits of the buffered address bus. The memories drive and receive the data bus through 8T26 tri-state transceivers to prevent an expanded system from presenting too great a capacitive load for the MOS memories.

The PROM memories (IC's 2-5, and IC's 11-14) are plugged into sockets and come programmed with PIPBUG. Any user's program may be stored in these PROM locations if PIPBUG is not required.

When the PC1001 is used to develop programs, and PIPBUG is resident in the first 1k-bytes of memory space, all of the 1k-bytes of RAM memory is available for use except the first 64 bytes (400_{16} to $43F_{16}$). The 64 locations are used by PIPBUG for temporary storage.

ADDRESS AND DATA BUS DRIVERS AND RECEIVERS

The data bus (DBUS0 - DBUS7) is buffered with 8T26 quad tri-state transceivers (IC's 24 and 25). These transceivers are inverting, and therefore the data bus transferred off of the PC1001 board is negative true ($\overline{\text{DBUS0}}$ - $\overline{\text{DBUS7}}$). The tri-state transceivers are controlled by RE1 (receiver control) and DE1 (driver control) from the control decode PROM (IC 35). The receiver control RE1 is a negative true signal (active "low") and has the following logic equation:

$$\text{RE1} = \overline{\text{OPREQ} \bullet \text{R}/\overline{\text{W}}}$$

The driver control DE1 is a positive true signal and has the following logic equation:

$$\text{DE1} = \text{OPREQ} \bullet \overline{\text{R}}/\text{W}$$

The logic equations reflect the fact that the 2650 drives the external data bus ($\overline{\text{DBUS0}}$ - $\overline{\text{DBUS7}}$) during all write operations (memory or I/O), and receives the external data bus during all read operations. But, when OPREQ is not a "high" the external data bus transceivers are in the tri-state mode.

The memory on the PC1001 board is buffered from the user's data bus ($\overline{\text{DBUS0}}$ - $\overline{\text{DBUS7}}$) with 8T26 quad tri-state transceivers. These transceivers are inverting so that information stored in memory is not complimented relative to the 2650. These transceivers are controlled by RE2 (receiver control) and DE2 (driver control) from the memory select decode logic. The logic for these control lines is shown below IC 20 (IC's 28 and 29) in Figure 4 and they have the following logic equations:

$$\text{RE2} = \text{MEMSEL} \bullet \overline{\text{R}}/\text{W}$$
$$\text{DE1} = \text{MEMSEL} \bullet \text{R}/\overline{\text{W}}$$

The RE2 control line is a negative true signal and is active when the memory on the PC1001 is selected to be written into. The DE1 control line is positive true and active when the memory on the PC1001 is selected to be read from.

The address bus is buffered with 8T97 tri-state buffers (IC's 21, 22, and 31). These buffers are in the tri-state mode whenever OPREQ is inactive.

CONTROL LINE DRIVERS AND RECEIVERS

The two control lines OPREQ and RUN/$\overline{\text{WAIT}}$ are buffered with 8T97 tri-state buffers (IC 32), but are never placed in the tri-state mode.

The control lines INTACK, WRP, $\overline{\text{R}}$/W, and M/$\overline{\text{IO}}$ are also driven by 8T97 tri-state buffers (IC 32), and are switched to the tri-state mode when the $\overline{\text{DMA}}$ line is pulled "low". The pause input to the 2650 may be activated by driving the $\overline{\text{DMA}}$ line (PC1001 pin 14) or the $\overline{\text{PAUSE}}$ line (PC1001 pin 27) "low".

The interrupt request line and the reset line to the 2650 are buffered by TTL AND gates (IC 33). The reset switch on the PC1001 (upper left corner of Figure 2) is "wire ORed" with the $\overline{\text{RESET}}$ line to the PC1001 board (PC1001 pin 25).

The operation acknowledge line to the 2650 ($\overline{\text{OPACK}}$) is buffered with a TTL AND gate (IC 33), and has as its inputs an external acknowledge ($\overline{\text{OPACK}}$, PC1001 pin 22) and an internal acknowledge (OPK). The internal acknowledge is generated for all memory access cycles and Non-Extended I/O cycles initiated by the 2650. For Extended I/O cycles the external device must generate the external operation acknowledge ($\overline{\text{OPACK}}$).

CONTROL LINE DECODE

A control line decoder is implemented with a 32X8 PROM (82S123) to generate secondary control lines used by the logic supporting the 2650. The primary control lines from the 2650 ($\overline{\text{R}}$/W, OPREQ, M/$\overline{\text{IO}}$ E/$\overline{\text{NE}}$, and D/$\overline{\text{C}}$) are used to address the PROM, and each address represents one combination of the primary control lines. Stored at each memory location are eight bits, each one of which represents the logical state of a secondary control line. There are five address inputs to the PROM, and the 32 (2^5) possible addresses exhaust all of the logical combination of the primary control lines. The secondary control lines, their logic equations, and their functions are given in Table 1. Table 2 shows the contents of each of the 32 locations of the PROM. The control line decode PROM is shown in Figure 4 (IC 35).

MEMORY SELECT DECODE

The memory select decode logic is shown in Figure 4 (IC's 19, 20, 28, 29, 30 and 34). The 2k-bytes of memory are implemented with 256X4 bit memory chips. The memory chips are arranged into eight 256-byte sections.

The ninth, tenth, and eleventh bits of the address bus (ABUS8-ABUS10) are decoded to select one of the eight 256-byte sections of memory. The one-of-eight decoder (IC 20) is enabled by MEMSEL, which has the following logic equations:

$$\overline{\text{MEMSEL}} = (\text{OPREQ} + \text{OPEX}) \bullet \text{M}/\overline{\text{IO}} \bullet \overline{\text{ABUS11}} \bullet \overline{\text{ABUS12}} \bullet \overline{\text{ABUS13}} \bullet \overline{\text{ABUS14}}$$

The MEMSEL line is also used to enable the 8T26 quad tri-state transceivers that buffer the memory on the PC1001 from the external data bus ($\overline{\text{DBUS0}}$-$\overline{\text{DBUS7}}$).

SERIAL I/O TRANSMITTER AND RECEIVER

A serial I/O port is implemented on the PC1001 with the flag and sense line of the 2650. The PIPBUG program handles the serial I/O using software timing loops to sample the SENSE input and build eight bit ASCII characters. The PC1001 is capable of interfacing to a current loop type terminal, or an RS232 compatible terminal.

The current loop driver uses an open collector NAND gate (IC 34) as the switching element. The 20 milliamp source is a 220Ω resistor connected to +5 volts on the PC1001 (PC1001 pin S), and the open collector NAND gate either provides a return path for the 20 milliamps (NAND output "on") or it does not (NAND output "off"). The current loop receiver is a CMOS hex inverter (IC 30) with the input pulled to +5 volts through a 2.7kΩ resistor (PC1001 pin P). The teletype transmitter is a contact closure and connects the input of the CMOS inverter to the receiver return line (PC1001 pin R), which is tied to ground on the PC1001 board.

The RS232 driver is an 8T15 EIA Line Driver (IC 26), and the RS232 receiver is an 8T16 EIA Line Receiver (IC 43). The 8T15 is the only chip on the PC1001 that does not operate on the +5 volt power supply, and ±15 volt power supplies are specified for this driver.

CONTROL LINE DECODE PROM DESCRIPTION

SIGNAL NAME	OUTPUT	PIN #	LOGIC EQUATION	FUNCTION
WOPD	B0	1	$\text{WOPD} = \text{OPREQ} \bullet \overline{\text{M}/\overline{\text{IO}}} \bullet \overline{\text{E}/\overline{\text{NE}}} \bullet \text{D}/\overline{\text{C}} \bullet \overline{\text{R}}/\text{W}$	LOADS NON-EXTENDED OUTPUT LATCH, PORT D
EIPD*	B1	2	$\overline{\text{EIPD}} = \text{OPREQ} \bullet \overline{\text{M}/\overline{\text{IO}}} \bullet \overline{\text{E}/\overline{\text{NE}}} \bullet \text{D}/\overline{\text{C}} \bullet \overline{\overline{\text{R}}/\text{W}}$	ENABLES NON-EXTENDED INPUT GATES, PORT D
EIPC*	B2	3	$\overline{\text{EIPC}} = \text{OPREQ} \bullet \overline{\text{M}/\overline{\text{IO}}} \bullet \overline{\text{E}/\overline{\text{NE}}} \bullet \overline{\text{D}/\overline{\text{C}}} \bullet \overline{\overline{\text{R}}/\text{W}}$	ENABLES NON-EXTENDED INPUT GATES, PORT C
WOPC	B3	4	$\text{WOPC} = \text{OPREQ} \bullet \overline{\text{M}/\overline{\text{IO}}} \bullet \overline{\text{E}/\overline{\text{NE}}} \bullet \overline{\text{D}/\overline{\text{C}}} \bullet \overline{\text{R}}/\text{W}$	LOADS NON-EXTENDED OUTPUT LATCH, PORT C
OPK*	B4	5	$\overline{\text{OPK}} = \text{OPREQ}\ [(\text{M}/\overline{\text{IO}}) + (\overline{\text{M}/\overline{\text{IO}}} \bullet \text{E}/\overline{\text{NE}})]$	RETURNS $\overline{\text{OPACK}}$ FOR ALL OPREQ EXCEPT EXTENDED I/O
R/$\overline{\text{W}}$	B5	6	$\text{R}/\overline{\text{W}} = \overline{\overline{\text{R}}/\text{W}}$	INVERTS $\overline{\text{R}}$/W
DE1	B6	7	$\text{DE1} = \text{OPREQ} \bullet \overline{\text{R}}/\text{W}$	DRIVES EXTERNAL DATA BUS ($\overline{\text{DBUS0}}$ – $\overline{\text{DBUS7}}$)
RE1*	B7	9	$\overline{\text{RE1}} = \text{OPREQ} \bullet \overline{\overline{\text{R}}/\text{W}}$	ENABLES RECEIVERS OF EXTERNAL DATA BUS ($\overline{\text{DBUS0}}$ – $\overline{\text{DBUS7}}$)

*NEGATIVE TRUE SIGNALS

TABLE 1

CONTROL LINE DECODE PROM

ADDRESS	INPUT					OUTPUT								OUTPUT_{16}
	A4	A3	A2	A1	A0	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	1	0	1	1	0	1	1	0	B6
1	0	0	0	0	1	1	0	0	1	0	1	1	0	96
2	0	0	0	1	0	0	0	1	0	0	0	1	0	22
3	0	0	0	1	1	1	1	0	0	1	1	1	0	CE
4	0	0	1	0	0	1	0	1	1	0	1	1	0	B6
5	0	0	1	0	1	1	0	0	1	0	1	1	0	96
6	0	0	1	1	0	0	0	1	0	0	1	0	0	24
7	0	0	1	1	1	1	1	0	0	0	1	1	1	C7
8	0	1	0	0	0	1	0	1	1	0	1	1	0	B6
9	0	1	0	0	1	1	0	0	1	0	1	1	0	96
10	0	1	0	1	0	0	0	1	1	0	1	1	0	36
11	0	1	0	1	1	1	1	0	1	0	1	1	0	D6
12	0	1	1	0	0	1	0	1	1	0	1	1	0	B6
13	0	1	1	0	1	1	0	0	1	0	1	1	0	96
14	0	1	1	1	0	0	0	1	1	0	1	1	0	36
15	0	1	1	1	1	1	1	0	1	0	1	1	0	D6
16	1	0	0	0	0	1	0	1	1	0	1	1	0	B6
17	1	0	0	0	1	1	0	0	1	0	1	1	0	96
18	1	0	0	1	0	0	0	1	0	0	1	1	0	26
19	1	0	0	1	1	1	1	0	0	0	1	1	0	C6
20	1	0	1	0	1	1	0	0	1	0	1	1	0	B6
21	1	0	1	0	1	1	0	0	1	0	1	1	0	96
22	1	0	1	1	0	0	0	1	0	0	1	1	0	26
23	1	0	1	1	1	1	1	0	0	0	1	1	0	C6
24	1	1	0	0	0	1	0	1	1	0	1	1	0	B6
25	1	1	0	0	1	1	0	0	1	0	1	1	0	96
26	1	1	0	1	0	0	0	1	0	0	1	1	0	26
27	1	1	0	1	1	1	1	0	0	0	1	1	0	C6
28	1	1	1	0	0	1	0	1	1	0	1	1	0	B6
29	1	1	1	0	1	1	0	0	1	0	1	1	0	96
30	1	1	1	1	0	0	0	1	0	0	1	1	0	26
31	1	1	1	1	1	1	1	0	0	0	1	1	0	C6
	M/$\overline{\text{IO}}$	E/$\overline{\text{NE}}$	D/$\overline{\text{C}}$	OPREQ	$\overline{\text{R}}$/W	REI	DEI	R/$\overline{\text{W}}$	OPK	WOPC	EIPC	EIPD	WOPD	

TABLE 2

The current loop driver/receiver pair or the RS232 driver/receiver pair is selected by a hardwire jumper on the PC1001 board. The connection of these jumpers is described in Table 3, and shown in Figure 4 (2650 pin 40/FLAG, 2650 pin 1/SENSE).

SERIAL I/O DRIVER/RECEIVER MODE

2650 FUNCTION	JUMPER	DESCRIPTION
FLAG	A-B	CURRENT LOOP DRIVER
FLAG	A-C	RS232 DRIVER
SENSE	E-D	CURRENT LOOP RECEIVER
SENSE	F-D	RS232 RECEIVER

TABLE 3

PARALLEL I/O LATCHES AND RECEIVERS

The logic used to implement the two parallel I/O ports on the PC1001 is identical. The output ports are 7475 quad bistable latches (IC's 36, 37, 38, and 39), and are loaded when a Non-Extended write I/O instruction is executed (WRTC, WRTD). The input ports use 8T98 tri-state high speed hex inverters (IC's 40, 41, and 42), and are gated on the external data bus ($\overline{\text{DBUS0}}$ - $\overline{\text{DBUS7}}$) when a Non-Extended read I/O instruction is executed (REDC, REDD).

The control signals used to activate the tri-state gates (EIPD, and EIPC) are generated by the control line decode PROM (IC 35).

The control signals used to load the output latches are designated COPC and COPD, and have the following logic equations:

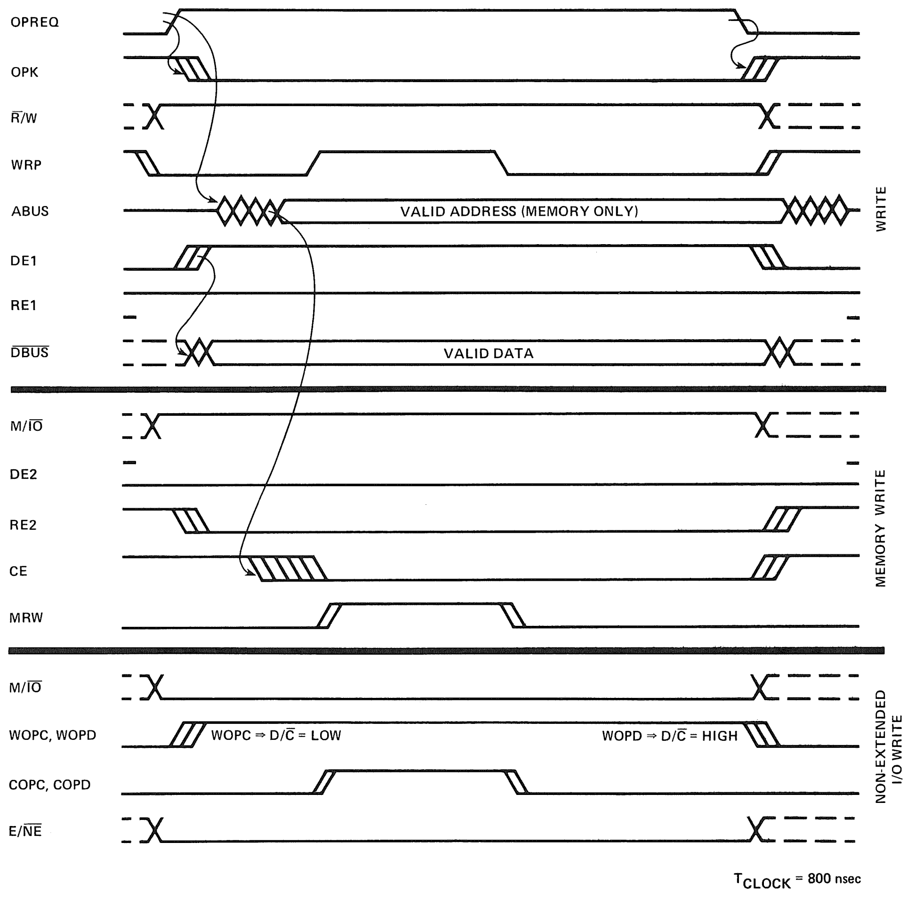
COPD = WRP • WOPD
COPC = WRP • WOPC

The WRP signal is the "write pulse" from the 2650, while the WOPD and WOPC signals are generated by the control line decode PROM (IC 35).

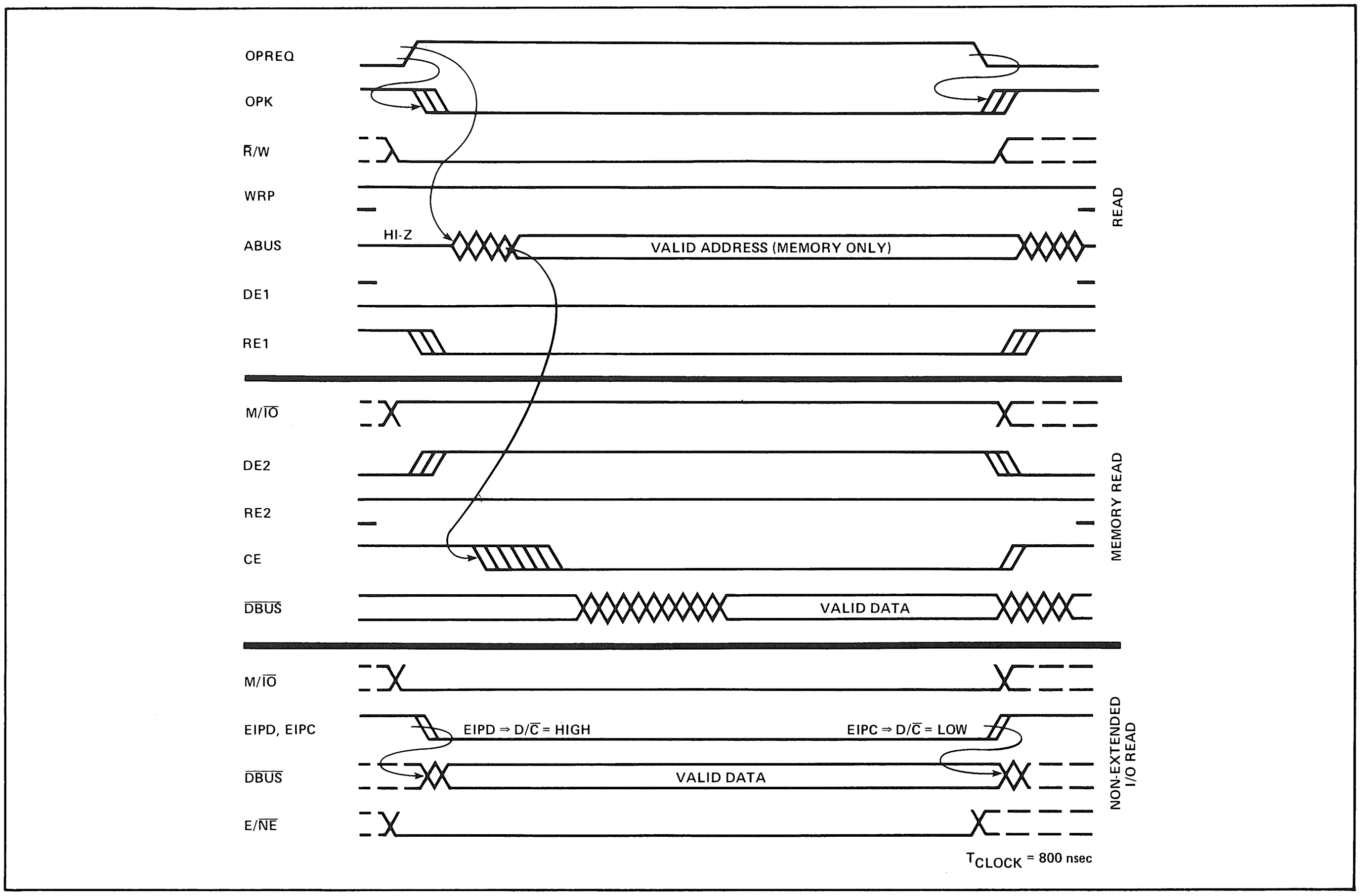
The output latches drive LED's on the PC1001 board. A logic ONE from the 2650 lights the corresponding LED. The output latches are loaded from the external data bus ($\overline{DBUS0}$ - $\overline{DBUS7}$), and to obtain the required inversion at the latch output (OPD0 - OPD7, and OPC0 - OPC7) the $\overline{Q}$ pin is used.

APPENDIX

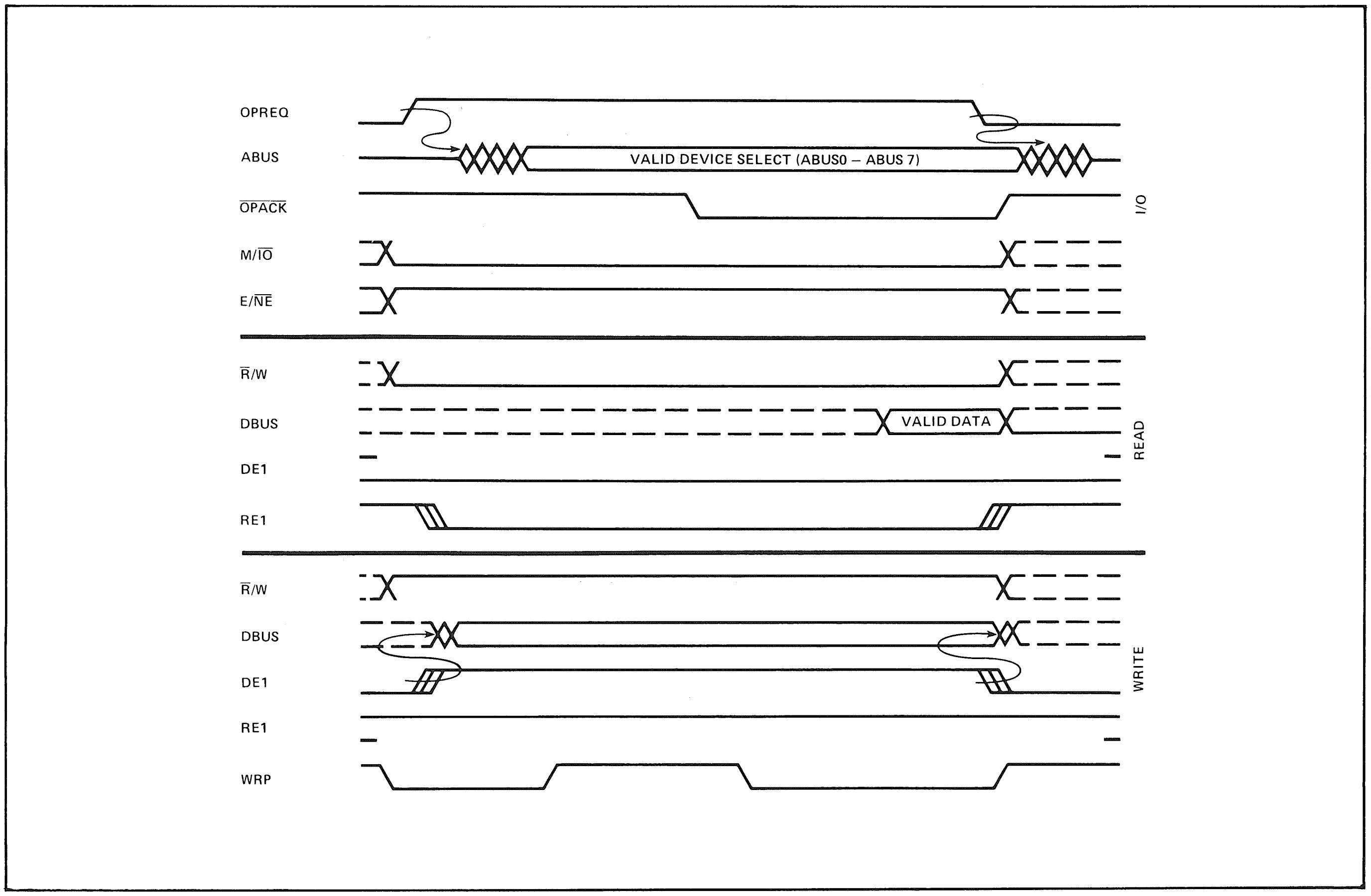
WRITE TIMING



READ TIMING



EXTENDED I/O TIMING



POWER REQUIREMENTS

+5 VOLT POWER SUPPLY:
LINE REGULATION – 0.1%
LOAD REGULATION – 0.1%
RIPPLE – 10 millivolts (MAX)
RESPONSE – 30μsec (MAX)
CURRENT – 2 amps

±15 VOLT POWER SUPPLIES:
LINE REGULATION – 0.1%
LOAD REGULATION – 0.1%
RIPPLE – 10 millivolts (MAX)
RESPONSE – 30μsec (MAX)
CURRENT – 50 milliamps

PARTS LIST

IC #	PART #	TYPE	QTY
28	7400	QUAD 2-INPUT NAND	1
29, 33	7408	QUAD 2-INPUT AND	2
19	7430	8-INPUT NAND	1
34	7438	QUAD 2-INPUT NAND OPEN COLLECTOR	1
36, 37, 38, 39	7475	QUAD BISTABLE LATCH	4
26	8T15	E1A DRIVER (RS232)	1
43	8T16	E1A RECEIVER (RS232)	1
1, 10 24, 25	8T26	QUAD BUS DRIVER/RECEIVER	4
40, 41, 42	8T98	HEX HIGH SPEED INVERTER	3
20	8250	1 OF 8 DECODER	1
6, 7, 8, 9 15, 16, 17, 18	2606	256X4 NMOS RAM	8
30	4049	HEX INVERTER (CMOS)	1
35	82S123	32X8 BIPOLAR PROM	1
2	82S129	PIPBUG PROM CK267	1
11	82S129	PIPBUG PROM CK268	1
3	82S129	PIPBUG PROM CK269	1
12	82S129	PIPBUG PROM CK270	1
4	82S129	PIPBUG PROM CK271	1
13	82S129	PIPBUG PROM CK272	1
5	82S129	PIPBUG PROM CK273	1
14	82S129	PIPBUG PROM CK274	1
23	2650	MICROPROCESSOR	1
27	MOTOROLA K1100A	XTAL OSCILLATOR	1
D20	IN914	DIODE	1
D1-D19	DIALCO 555-3007	LED INDICATOR	19
S1	GREYHILL 39-201	MINIATURE, PUSH BUTTON SWITCH	1
(IC 23)*	VERMON H23-20302	40-PIN DIP SOCKET	1
(IC 2, 3 4, 5, 11, 12, 13, 14)	AMPHENOL 821-25011-164	16-PIN DIP SOCKET	8

*#'s in parenthesis indicate the IC's that are plugged into the listed socket.

PARTS LIST (Continued)

IC #	PART #	TYPE	QTY
(IC 27)	AMPHENOL 821-25011-144	14-PIN DIP SOCKET	1
C1, C2 C3	230-1250-004-230	4.7μ FARAD CAP	3
–	EMCON 5021ES50RD104M	0.1μ FARAD CAP	45
C4		0.047μ FARAD CAP	1
R4	230-0910-332-230	51Kr, ¼ WATT RES	1
R3		10Kr, ¼ WATT RES	1
R7		7.4Kr, ¼ WATT REST	1
R5, R6	230-0910-297-230	1Kr, ¼ WATT RES	1
R1, R2	230-0910-282-230	220r, ¼ WATT RES	2
	AMPHENOL 225-804-50	100 PIN P.C. EDGE CONNECTOR	1

RS232C STANDARD CONNECTOR

The RS232 Electronic Industries Association (EIA) standard for "interface between terminals and communications equipment using serial binary data interchange" describes a commonly used signal definition and connector pin assignment. The table below lists the pin numbers and signal names most frequently used by. data terminals.

PIN #	DESCRIPTION
1	PROTECTIVE GROUND
2	TRANSMITTED DATA
3	RECEIVED DATA
5	CLEAR TO SEND
6	DATA SET READY
7	SIGNAL GROUND
8	RECEIVED LINE SIGNAL DETECTOR
20	DATA TERMINAL READY

Transmitted Data (pin 2) is received by the PC1001, therefore pin 2 of the RS232 connector is routed to the SENSE input of the 2650. Received Data (pin 3) is transmitted from the PC1001, therefore pin 3 of the RS232 is routed to the FLAG output of the 2650.

The signals on pins 5, 6, 8, and 20 are used between data terminals and communications MODEMs. Since the PC1001 does not provide these "handshake" lines they can be simulated by shorting them all together. In this configuration the Data Terminal Ready line drives the other 3 lines to the proper state for enabling the communication channel. This is not required for all data terminals (not teletypes), but is required for some.

Further information on RS232C specifications can be obtained from the EIA RS-232-C Standard available from the Electronic Industries Association in Washington D.C.

The type of connector commonly used for RS232 compatible data terminals is a 25-pin TRW Cinch type connector of the DB25 series.

TELETYPE CONNECTION

Connection to a teletype may be made at the terminal strip inside of the teletype. The pin numbers and signal names are listed in the table below.

PIN #	DESCRIPTION
6	RECEIVER – (TTY SERIAL IN –)
7	RECEIVER + (TTY SERIAL IN +)
3	TRANSMITTER – (TTY SERIAL OUT –)
4	TRANSMITTER + (TTY SERIAL OUT +)

The teletype is a 20 milliamp current loop type of receiver and a contact closure type of transmitter. The PIPBUG debug program on the PC1001 board communicates with the teletype in a full duplex mode, echoing characters as they are received.

EDGE CONNECTOR SIGNAL LIST

PIN #	FUNCTION	PIN #	FUNCTION
1	GND	A	GND
2	GND	B	GND
3	NC*	C	NC
4	$\overline{\text{DBUS0}}$	D	OPD 0
5	$\overline{\text{DBUS1}}$	E	OPD 1
6	$\overline{\text{DBUS2}}$	F	OPD 2
7	$\overline{\text{DBUS3}}$	H	OPD 3
8	$\overline{\text{DBUS4}}$	J	OPD 4
9	$\overline{\text{DBUS5}}$	K	OPD 5
10	$\overline{\text{DBUS6}}$	L	OPD 6
11	$\overline{\text{DBUS7}}$	M	OPD 7
12	EIPD	N	COPD
13	D/$\overline{\text{C}}$	P	TTY SERIAL IN +
14	$\overline{\text{DMA}}$	R	TTY SERIAL IN –
15	E/$\overline{\text{NE}}$	S	TTY SERIAL OUT +
16	INTACK	T	TTY SERIAL OUT –
17	$\overline{\text{R}}$/W	U	RS232 GROUND
18	WRP	V	RS232 OUTPUT
19	RUN/$\overline{\text{WAIT}}$	W	TTY TAPE READER OUT –
20	OPREQ	X	TTY TAPE READER OUT +
21	M/$\overline{\text{IO}}$	Y	RS232 INPUT
22	$\overline{\text{OPACK}}$	Z	COPC
23	CLOCK	a	OPC 0
24	$\overline{\text{OPEX}}$	b	OPC 1
25	$\overline{\text{RESET}}$	c	OPC 2
26	$\overline{\text{INTREQ}}$	d	OPC 3
27	$\overline{\text{PAUSE}}$	e	OPC 4
28	NC*	f	OPC 5
29	NC*	g	OPC 6
30	NC*	h	OPC 7
31	NC*	j	EIPC
32	NC*	k	IPD 0
33	ABUS 11	m	IPD 1
34	ABUS 13	n	IPD 2
35	ABUS 12	p	IPD 3
36	ABUS 14	r	IPD 4
37	ABUS 9	s	IPD 5
38	ABUS 10	t	IPD 6
39	ABUS 8	u	IPD 7
40	ABUS 7	v	IPC 0
41	ABUS 6	w	IPC 1
42	ABUS 5	x	IPC 2
43	ABUS 3	y	IPC 3
44	ABUS 0	z	IPC 4
45	ABUS 1	$\overline{\text{a}}$	IPC 5
46	ABUS 4	$\overline{\text{b}}$	IPC 6
47	ABUS 2	$\overline{\text{c}}$	IPC 7
48	+15V	$\overline{\text{d}}$	+15V
49	–15V	$\overline{\text{e}}$	–15V
50	+5V	$\overline{\text{f}}$	+5V

*NC = NO CONNECTION

TABLE 4

signetics 811 EAST ARQUES AVENUE ■ SUNNYVALE, CALIFORNIA ■ 94086 ■ TEL: (408) 739-7700