INTEGRATED CIRCUITS

DATA HANDBOOK

Signetics FAST Logic

Signetics
Philips Components

PHILIPS

Signetics

FAST Products

Data Handbook

FAST: The World's Leading High-Performance TTL Family

Signetics reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Signetics assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified. Applications that are described herein for any of these products are for illustrative purposes only. Signetics makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

LIFE SUPPORT APPLICATIONS

Signetics Products are not designed for use in life support appliances, devices, or systems where malfunction of a Signetics Product can reasonably be expected to result in a personal injury. Signetics customers using or selling Signetics' Products for use in such applications do so at their own risk and agree to fully indemnify Signetics for any damages resulting from such improper use or sale.

Signetics registers eligible circuits under
the Semiconductor Chip Protection Act.

Preface

FAST Products

Signetics would like to thank you for your interest in our FAST product line. Because of its wide customer acceptance, FAST has become the preferred high performance logic family. We are proud to participate in and contribute to the dynamic growth of this product family. With over 220 products in production, Signetics offers the widest selection of FAST products and an emphasis on integrated MSI and LSI solutions.

Each data sheet contained in this Handbook is designed to stand alone and reflect the latest DC and AC specification for a particular product. Each commercial 74F product is specified over a 10% V_{CC} range, both for AC and DC parameters. Additionally, DC specifications for V_{OH} and V_{OL} are provided over the 5% V_{CC} range.

All reference to military product has been deleted, specifically, to reflect government requirements imposed by Revision C of MIL–STD 883, including the general provisions of Paragraph 1.2. Specifications for military grade FAST products are available from your nearest Signetics sales office, sales representative, or authorized distributor.

This 1989 FAST Handbook updates the 1987 Data Manual and consolidates information published in the March 1988 and September 1988 Updates to the 1987 Data Manual.

Other features of this data handbook include:

- Updated Availability and Functional Selection Guides
- An expanded Circuit Characteristics Section
- A User's Guide
- Six new Application Notes
- An expanded chapter on Surface Mounted Devices (SMD) and an Application Note on Thermal Considerations in SMD
- An updated section on package outlines

New FAST part types are being released continuously. As you see new product announcements, please contact your nearest Signetics sales office, sales representative, or authorized distributor for the latest information.

In addition to FAST, Signetics Standard Products Group offers the industry's broadest line of commercially available Logic Products, spanning a wide speed/power spectrum from ECL (100K/10K) to TTL (74, 74LS, 74S, 74ALS, 8T, and 8200) to CMOS (4000 Series, 74HC/HCT, 74AC/ACT). Information on these product lines is also available from your nearest Signetics sales office, sales representative, or authorized distributor.

Signetics Standard Products Group – Logic Products

Product Status

FAST Products

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Signetics

Contents

FAST Products

Contents

Contents

Contents

Contents

Contents

Section 7 -FAST Application Notes

74F FAST TTL
Introduction

THE HIGH-SPEED LOGIC OF THE '80s

Product Description

Signetics has combined advanced oxide-isolated fabrication techniques with standard TTL functions to create a new family designed for the '80s. The high operating speeds of FAST can push system operating speeds into areas previously reserved for 10K ECL, but with simple TTL design rules and single 5V power supplies. Low input loading allows the user to mix LS, ALS, and HCMOS in the same system without the need for translators and restrictive fanout requirements.

FAST circuits are pin-for-pin replacements for 74S types, but offer dissipation 3-4 times lower and higher operating speeds. Existing systems can achive much lower power and improved performance by replaceing the 74S types with the corresponding FAST devices.

The input structure provides better noise immunity because of higher thresholds, while the oxide-isolation and new circuit techniques create devices that have less variaton with temperature or supply voltage than existing TTL logic families. Signetics guarantees all AC parameters under realistic system conditions – across the supply voltage spread and the temperature range, and with heavy 50pF output loads.

The use of high-capacitance PNP inputs has been avoided, and clamping diodes have been added to both the inputs and outputs to prevent negative overshoots. High input breakdown voltages allow unsued inputs to be tied directly to V_{CC} without pull-up resistors.

Multiple sources and a complete family of powerful circuits combine to make Signetics FAST the logic choice of the '80s.

FEATURES

- **3ns propagation delays**
- **4mW/gate power dissipation**
- **Guaranteed AC performance over temperature and extended V_{CC} Range: 5V ± 10%**
- **High impedance NPN base input structure on many types for reduced bus loading in LOW state (I_{IL} = 20μA)**
- **Standard TTL functions and pinouts**
- **Replacement for "S" types...1/4 the power**
- **Designer's choice for new system designs**

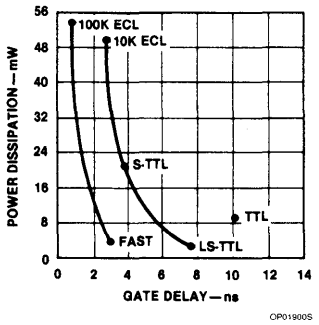


Figure 1. The Speed/Power Spectrum

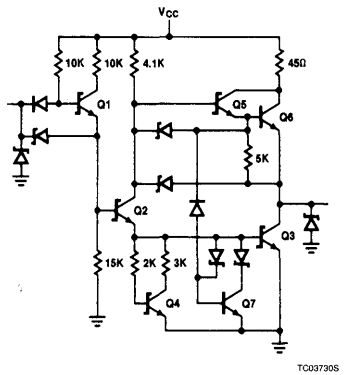


Figure 2. Basic FAST Gate

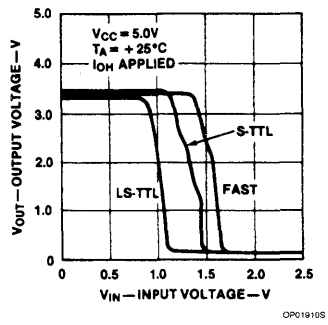
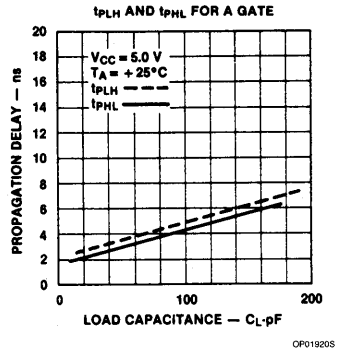
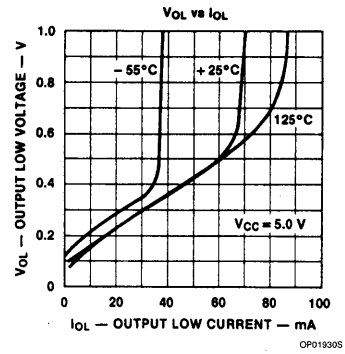


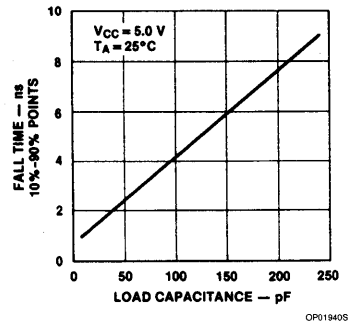
Figure 3. Transfer Functions At Room Temperature



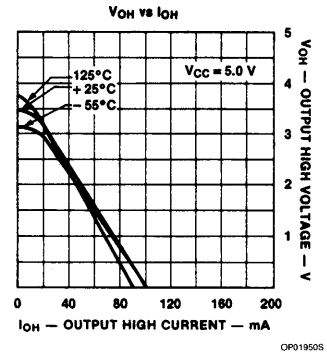
'F00
Figure 4. Propagation Delay VS Load Capacitance



'F00
Figure 5. Output LOW Characteristics



'F00
Figure 6. Fall Time VS Load Capacitance



'F00
Figure 7. Output HIGH Characteristics

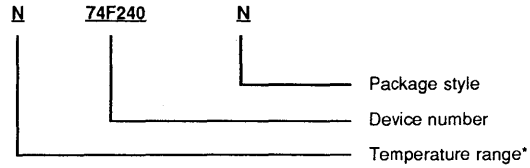
Ordering Information

FAST Products

Signetics commercial FAST products are generally available in both standard dual–in–line and surface mounted options. The ordering code specifies temperature range, device number, and package style as shown below. For commercial product, the standard temperature range is 0 to 70°C. Available package options are shown on individual data sheets in the "Ordering Code" block. For surface mounted devices the SO plastic dual–in–line package is supplied up to and including 28 pins. Above 28 pins, the plastic leaded chip carrier is utilized.

A wide variety of functions and package options are available for military products. Information on military products is available from the nearest Signetics sales office, sales representative, or authorized dealer. The Signetics Military Products Data Manual contains specifications, package, and ordering information for all military–grade products.

ORDERING CODE EXAMPLES



TEMPERATURE RANGE	DEVICE NUMBER	PACKAGE STYLE
Commercial Range 0°C to 70°C	74XXX	N = Plastic Dip D = Plastic SO Dip (surface mounted) A = Plastic Leaded Chip Carrier (PLCC)
Military Range –55°C to 125°C	See Military Products Data Manual	

* Please note that the temperature range prefix "N" is omitted on the package due to dimensional constraint

Signetics

FAST Products

Section 1
Indices

INDEX

Signetics Availability Guide

FAST Products

DEVICE	NO. OF PINS	DESCRIPTION	AVAILABILITY	
			DIP	SMD
74F00	14	Quad 2-Input NAND Gate	A	SO
74F02	14	Quad 2-Input NOR Gate	A	SO
74F04	14	Hex Inverter	A	SO
74F06	14	Hex Inverter Buffer/Driver (OC)	A	SO
74F07	14	Hex Buffer/Driver (OC)	A	SO
74F08	14	Quad 2-Input AND Gate	A	SO
74F10	14	Triple 3-Input NAND Gate	A	SO
74F11	14	Triple 3-Input AND Gate	A	SO
74F13	14	Dual 4-Input NAND Schmitt Trigger	A	SO
74F14	14	Hex Inverter Schmitt Trigger	A	SO
74F20	14	Dual 4-Input NAND Gate	A	SO
74F27	14	Triple 3-Input NOR Gate	A	SO
74F30	14	8-Input NAND Gate	A	SO
74F32	14	Quad 2-Input OR Gate	A	SO
74F37	14	Quad 2-Input NAND Buffer (OC)	A	SO
74F38	14	Quad 2-Input NAND Buffer	A	SO
74F40	14	Dual 4-Input NAND Buffer	A	SO
74F51	14	Dual 2-Wide 2-Input, 2-Wide3-Input AND-OR-INVERT Gate	A	SO
74F64	14	4-2-3-2 Input AND/OR Gate	A	SO
74F74	14	Dual D-Type Flip-Flop	A	SO
74F83	16	4-Bit Binary Adder With Fast Carry (Center Pin 74F283)	A	SO
74F85	16	4-Bit Magnitude Comparator	A	SOL
74F86	14	Quad 2-Input Exclusive-OR Gate	A	SO
74F109	16	Dual $J\overline{K}$ Positive Edge Triggered Flip-Flop	A	SO
74F112	16	Dual JK Negative Edge Triggered Flip-Flop	A	SO
74F113	14	Dual JK Negative Edge Triggered Flip-Flop Without Reset	A	SO
74F114	14	Dual JK Negative Edge Triggered Flip-Flop	A	SO
74F125	14	Quad Buffer	A	SO
74F126	14	Quad Buffer	A	SO
74F132	16	Quad 2-Input NAND Schmitt Trigger	A	SO
74F133	16	13-Input NAND Gate	A	SO
74F138	16	1-of-8 Decoder/Demultiplexer	A	SO
74F139	16	Dual 1-of-4 Decoder/Demultiplexer	A	SO
74F148	16	8 Line to 3 Line Priority Encoder	A	SO
74F151	16	8-Input Multiplexer	A	SO
74F151A	16	8-Input Multiplexer	A	SO
74F153	16	Dual 4-Input Multiplexer	A	SO
74F154	14	1-of-16 Decoder/Demultiplexer	A	SO
74F157	16	Quad 2-Input Data Selector/Multiplexer, NINV	A	SO
74F157A	16	Quad 2-Input Data Selector/Multiplexer, NINV	A	SO
74F158	16	Quad 2-Input Data Selector/Multiplexer, INV	A	SO
74F158A	16	Quad 2-Input Data Selector/Multiplexer, INV	A	SO
74F160A	16	BCD Decade Counter, Asynchronous Reset	A	SO
74F161A	16	4-Bit Binary Counter, Asynchronous Reset	A	SO
74F162A	16	BCD DecadeCounter, Synchronous Reset	A	SO
74F163A	16	4-Bit Binary Counter, Synchronous Reset	A	SO
74F164	14	8-Bit Serial/Parallel-In, Serial Out Shift Register	A	SO
74F166	16	8-BitBidirectional Universal Shift Register	A	SO
74F168	16	4-Bit Up/Down BCD Decade Synchronous Counter	A	SO
74F169	16	4-Bit Up/Down BCD Binary Synchronous Counter	A	SO
74F173	16	Quad D Flip-Flop (3-state)	A	SO
74F174	16	Hex D Flip-Flop With Master Reset	A	SO
74F175	16	Quad D Flip-Flop Wth Master Reset	A	SO
74F181	24	4-Bit Arithmetic Logic Unit	A	SOL
74F182	16	Look Ahead Carry Generator	A	SO

Availability Guide

DEVICE	NO. OF PINS	DESCRIPTION	AVAILABILITY	
			DIP	SMD
74F189A	16	64 Bit Random Access Memory, INV(3-state)	Q3 89	
74F190	16	Asynchronous Presettable Up/Down BCD Decade Counter	A	SO
74F191	16	Asynchronous Presettable Up/Down BCD Binary Counter	A	SO
74F192	16	Up/Down BCD Decade Counter With Separate Up/Down Clocks	A	SO
74F193	16	Up/Down BCD Binary Counter With Separate Up/Down Clocks	A	SO
74F194	16	4-Bit Bidirectional Universal Shift Register	A	SO
74F195	16	4-Bit Parallel Access Shift Register	A	SO
74F198	24	8-Bit Bidirectional Universal Shift Register	A	SOL
74F199	24	8-Bit Parallel Access Shift Register	A	SOL
74F219A	16	64 Bit Random Access Memory, NINV(3-state)	Q3 89	
74F224	16	16 X 4 Synchronous FIFO (3-state)	Q3 89	
74F225	20	16 X 5 Asynchronous FIFO (3-state)	Q3 89	
74F227	20	16 X 4 Synchronous FIFO With Ready Enables (3-state)	Q3 89	
74F240	20	Octal Inverter Buffer, INV (3-state)	A	SOL
74F241	20	Octal Buffer, NINV (3-state)	A	SOL
74F242	14	Octal Bus Transceiver, INV (3-state)	A	SO
74F243	14	Octal Bus Transceiver, NINV(3-state)	A	SO
74F244	20	Octal Buffer, NINV (3-state)	A	SOL
74F245	20	Octal Transceiver, (3-state)	A	SOL
74F251	16	8-Input Multiplexer (3-state)	A	SO
74F251A	16	8-Input Multiplexer (3-state)	A	SO
74F253	16	Dual 4-Input Multiplexer	A	SO
74F256	16	Dual Addressable Latch	A	SO
74F257	16	Quad 2-Line To 1-Line Selector/Multiplexer, NINV (3-state)	A	SO
74F257A	16	Quad 2-Line To 1-Line Selector/Multiplexer, NINV (3-state)	A	SO
74F258	16	Quad 2-Line To 1-Line Selector/Multiplexer, INV (3-state)	A	SO
74F258A	16	Quad 2-Line To 1-Line Selector/ Multiplexer, INV (3-state)	A	SO
74F259	16	8-Bit Addressable Latch	A	SO
74F260	14	Dual 5-Input NOR Gate	A	SO
74F269	24	8-Bit Bidirectional Binary Counter (3-state)	A	SO
74F273	20	Octal D Flip-Flop	A	SOL
74F280A	14	9-Bit Odd/Even Parity Generator/Checker	A	SO
74F280B	14	9-Bit Odd/Even Parity Generator/Checker (Higher speed 74F280A)	A	SO
74F283	16	4-Bit Binary Adder With Fast Carry	A	SO
74F298	16	Quad 2-Input Multiplexer with Storage	A	SO
74F299	20	8-Bit Universal Shift/Storage Register (3-state)	A	SOL
74F322	20	8-Bit Serial/Parallel Register With Sign Extend (3-state)	A	SOL
74F323	20	8-Bit Universal Shift/Storage Register With Sync Reset And Common I/O Pins (3-s)	A	SOL
74F350	16	4-Bit Shifter	A	SO
74F352	16	Dual 4-Input Multiplexer (Inverted 74F153)	A	SO
74F353	16	Dual 4-Input Multiplexer (Inverted 74F253)	A	SO
74F365	16	Hex Buffer Driver (3-state)	A	SO
74F366	16	Hex Inverter (3-state)	A	SO
74F367	16	Hex Buffer Drivert (3-state)	A	SO
74F368	16	Hex Inverter Driver (3-state)	A	SO
74F373	20	Octal Transparent Latch (3-state)	A	SO
74F374	20	Octal D Flip-Flop (3-state)	A	SO
74F377	20	Octal D Flip-Flop With Enable	A	SO
74F378	16	Hex D Flip-Flop With Enable	A	SO
74F379	16	Quad D Flip-Flop With Enable	A	SO
74F381	20	4-Bit Arithmetic Logic Unit	A	SOL
74F382	20	4-Bit Arithmetic Logic Unit	A	SOL
74F385	20	Quad Serial Adder/Subtractor	A	SOL
74F393	16	Dual 4-Bit Binary Ripple Counter	A	SO
74F395	16	4-Bit Cascadable Shift Register (3-state)	A	SO

Availability Guide

DEVICE	NO. OF PINS	DESCRIPTION	AVAILABILITY	
			DIP	SMD
74F398	20	Quad 2-Port Register With True And Complementary Outputs	A	SOL
74F399	16	Quad 2-Port Register	A	SO
74F410	18	Register Stack-16X4 RAM 3-State Output Register (3-state)	A	
74F412	24	Octal Multi-Mode Buffered Latch, NINV (3-state)	A	SOL
74F432	24	Octal Multi-Mode Buffered Latch, INV (3-state)	A	SOL
74F455	24	Octal Buffer With Parity Generator Checker, INV (3-state)	A	SOL
74F456	24	Octal Buffer With Parity Generator Checker, NINV (3-state)	A	SOL
74F521	20	Octal Identity Comparator	A	SOL
74F524	20	8-Bit Register Comparator (OC +3-state)	A	SOL
74F533	20	Octal Transparent Latch, INV (3-state)	A	SOL
74F534	20	Octal D Flip-Flop, INV (3-state)	A	SOL
74F537	20	1-of-10 Decoder (3-state)	A	SOL
74F538	20	1-of-8 Decoder (3-state)	A	SOL
74F539	20	Dual 1-of-4 Decoder (3-state)	A	SOL
74F540	20	Octal Inverted Buffer (3-state) (Broadside Pinout of 74F240)	A	SOL
74F541	20	Octal Buffer (3-state) (Broadside Pinout of 74F244)	A	SOL
74F543	24	Octal Registered Transceiver, NINV (3-state)	A	SOL
74F544	24	Octal Registered Transceiver, INV (3-state)	A	SOL
74F545	20	Octal Bidirectional Transceiver With 3-State Inputs/Outputs, NINV	A	SOL
74F547	20	Octal Decoder/Demultiplexer With Addresss Latches And Acknowledge (OC)	A	SOL
74F548	20	Octal Decoder/Demultiplexer With Acknowledge (OC)	A	SOL
74F552	28	Octal Registered Transceiver With Parity And Status Flags, NINV (3-state)	A	SOL
74F563	20	Octal Transparent Latch (3-state) (Broadside Pinout of 74F533)	A	SOL
74F564	20	Octal D Flip-Flop (3-state) (Broadside Pinout of 74F534)	A	SOL
74F568	20	4-Bit Bidirectional Decade Synchronous counter	A	SOL
74F569	20	4-Bit Bidirectional Binary Synchronous counter	A	SOL
74F573	20	Octal Transparent Latch (3-state) (Broadside Pinout of 74F373)	A	SOL
74F574	20	Octal D Flip-Flop (3-state) (Broadside Pinout of 74F374)	A	SOL
74F579	20	8-Bit Bidirectional Binary counter (3-state)	A	SOL
74F582	24	4-Bit BCD Arithmetic Logic Unit	A	SOL
74F583	16	4-Bit BCD Adder	A	SOL
74F588	20	Octal Bidirectional Transceiver with IEEE-488 Termination Resistors (3-s I/O)	A	SOL
74F595	16	8-Bit Shift Register With Output LatchES (3-state)	A	SO
74F597	16	8-Bit Shift Register With Input Latches	Q3 89	
74F598	20	8-Bit Shift Register With Input Latches (3-state)	Q3 89	
74F604	28	Dual Octal Register (3-state)	A	SOL
74F605	28	Dual Octal Register (OC)	A	SOL
74F620	20	Octal Bus Transceiver, INV (3-state)	A	SOL
74F621	20	Octal Bus Transceiver, NINV (OC)	A	SOL
74F622	20	Octal Bus Transceiver, INV (OC)	A	SOL
74F623	20	Octal Bus Transceiver, NINV (3-state)	A	SOL
74F640	20	Octal Bus Transceiver, INV (3-state)	A	SOL
74F641	20	Octal Bus Transceiver With Common Output Enable, NINV (OC)	A	SOL
74F642	20	Octal Bus Transceiver With Common Output Enable, INV (OC)	A	SOL
74F646	24	Octal Bus Transceiver/Register, NINV (3-state)	A	SOL
74F646A	24	Octal Bus Transceiver/Register, NINV (3-state)	Q3 89	
74F647	24	Octal Bus Transceiver/Register, NINV (OC)	A	SOL
74F648	24	Octal Bus Transceiver/Register, INV (3-State)	A	SOL
74F648A	24	Octal Bus Transceiver/Register, INV (3-state)	Q3 89	
74F649	24	Octal Bus Transceiver/Register, INV (OC)	A	SOL
74F651	24	Octal Bus Transceiver/Register, INV (3-state)	A	
74F651A	24	Octal Bus Transceiver/Register, INV (3-state)	Q3 89	
74F652	24	Octal Bus Transceiver/Register, NINV (3-state)	A	
74F652A	24	Octal Bus Transceiver/Register, NINV (3-state)	Q3 89	
74F653	24	Octal Bus Transceiver/Register, INV (3-state + OC)	A	

Availability Guide

DEVICE	NO. OF PINS	DESCRIPTION	AVAILABILITY	
			DIP	SMD
74F654	24	Octal Bus Transceiver/Register, NINV (3-state + OC)	A	
74F655A	24	Octal Buffer/Driver With Parity, INV (3-state)	A	SOL
74F656A	24	Octal Buffer/Driver With Parity, NINV (3-state)	A	SOL
74F657	24	Octal Transceiver With 8-Bit Parity Generator/Checker (3-state)	A	SOL
74F657A	24	Octal Transceiver With 8-Bit ParityGenerator/Checker (3-state)	HOLD	
74F670	16	4X4 Register File	A	SOL
74F674	24	16-Bit Serial/Parallel-In, Serial-OutShift Register (3-state)	A	SOL
74F676	24	16-Bit Parallel-In, Serial-Out Shift Register (3-state)	A	SOL
74F711	20	Quint 2-to-1 Data Selector Multiplexer (3-state)	A	SOL
74F711-1	20	Quint 2-to-1 Data Selector Multiplexer With 30 Ohm Series Termination Resistors	A	
74F712	24	Quint 3-to-1 Data Selector Multiplexer (3-state)	Q3 89	
74F712-1	24	Quint 3-to-1 Data Selector Multiplexer With 30 Ohm Series Termination Resistors	A	
74F723	24	Quad 3-to-1 Data Selector Multiplexer (3-state)	Q3 89	
74F723-1	24	Quad 3-to-1 Data Selector Multiplexer With 30 Ohm Series Termination Resistors	A	
74F725	24	Quad 4-to-1 Data Selector Multiplexer (3-state)	Q3 89	
74F725-1	24	Quad 4-to-1 Data Selector Multiplexer With 30 Ohm Series Termination Resistors	A	
74F732	20	Quad Data Multiplexer, NINV	A	SOL
74F733	20	Quad Data Multiplexer, INV	A	SOL
74F755	24	Octal MailBox Register With Ready Flag (3-state)	A	SOL
74F756	20	Octal Inverter Buffer INV (Open Collector 'F240)	A	SOL
74F757	20	Octal Buffer, NINV (OpenCollector 'F241)	A	SOL
74F760	24	Octal Buffer, NINV (OpenCollector 'F244)	A	SOL
74F764	40	DRAM Dual Ported Controller With Latch	A	PLCC
74F764-1	40	DRAM Dual Ported Controller With Latch	A	PLCC
74F765	40	DRAM Dual Ported Controller Without Latch	A	PLCC
74F765-1	40	DRAM Dual Ported Controller Without Latch	A	PLCC
74F776	28	Octal Bidirectional Latched Pi-Bus Transceiver (3-state + OC)	A	SOL/P
74F779	16	8-Bit Bidirectional Counter (3-state)	A	SOL
74F786	16	4-Input Asynchronous Bus Arbiter	A	SOL
74F791	16	Programmable Pulse Generator	HOLD	
74F804	20	Hex 2-Input NAND Driver	A	SOL
74F805	24	Hex 2-Input NOR Driver	A	SOL
74F807	28	Octal Shift/Count Transceiver With Adder And Parity		
74F808	20	Hex 2-Input AND Driver	Q3 89	
74F821	20	10-Bit Interface Register, NINV (3-state)	A	SOL
74F822	24	10-Bit Interface Register, INV (3-state)	A	SOL
74F823	24	9-Bit Interface Register, NINV (3-state)	A	SOL
74F824	24	9-Bit Interface Register, INV (3-state)	A	SOL
74F825	24	8-Bit Interface Register, NINV (3-state)	A	SOL
74F826	24	8-Bit Interface Register, INV (3-state)	A	SOL
74F827	24	10-Bit Buffer/Line Driver, NINV (3-state)	A	SOL
74F828	24	10-Bit Buffer/Line Driver, INV (3-state)	A	SOL
74F832	20	Hex 2-Input OR Driver	Q3 89	
74F835	24	8-Bit Shift Register With 2:1 Multiplexer-In, Latched "B" Inputs And Serial-Out	A	SOL
74F838	40	Cascadable 32-State Microprogram Sequencer Controller	HOLD	SOL
74F841	20	10-Bit Bus Interface Latch, NINV (3-state)	A	SOL
74F842	24	10-Bit Bus Interface Latch, INV (3-state)	A	SOL
74F843	24	9-Bit Bus Interface Latch, NINV (3-state)	A	SOL
74F844	24	9-Bit Bus Interface Latch, INV (3-state)	A	SOL
74F845	24	8-Bit Bus Interface Latch, NINV (3-state)	A	SOL
74F846	24	8-Bit Bus Interface Latch, INV (3-state)	A	SOL
74F861	24	10-Bit Bus Transceiver, NINV (3-state)	A	SOL
74F862	24	10-Bit Bus Transceiver, INV (3-state)	A	SOL
74F863	24	9-Bit Bus Transceiver, NINV (3-state)	A	SOL
74F864	24	9-Bit Bus Transceiver,INV (3-state)	A	SOL

Availability Guide

DEVICE	NO. OF PINS	DESCRIPTION	AVAILABILITY	
			DIP	SMD
74F881	24	4-Bit Arithmetic Logic Unit/Function Generator	A	SOL
74F882	24	Look-Ahead Carry Generator	A	SOL
74F899	28	9-Bit Dual Latch Transceiver With 8-Bit Parity Generator/Checker (3-state)	Q4 89	
74F1240	20	Octal Inverter Buffer (3-state), Light Load 74F240	A	SOL
74F1241	20	Octal Buffer (3-state), Light Load 74F241	A	SOL
74F1242	14	Quad Transceiver (3-state)(Light Load 74F242)	A	SOL
74F1243	14	Quad Transceiver (3-state)(Light Load 74F243)	A	SOL
74F1244	20	Octal Buffer (3-state)(Light Load 74F244)	A	SOL
74F1245	20	Octal Bus Transceiver (3-state)(Light Load 74F245)	A	SOL
74F1604	28	Dual Octal Latch	A	SOL
74F1760	64	4-Way Latched Address Controller		
74F1761	48	DRAM And Interrupt Vector Controller	1989	
74F1762	40	4 MBit Memory Address Controller	A	PLCC
74F1763	48	1 MBit Intelligent DRAM Controller	Q3 89	
74F1764	48	1 MBit DRAM Dual Ported Controller With Latch	A	PLCC
74F1764-1	48	1 MBit DRAM Dual Ported Controller With Latch	A	
74F1765	48	1 MBit DRAM Dual Ported Controller Without Latch	A	PLCC
74F1765-1	48	1 MBit DRAM Dual Ported Controller Without Latch	Q3 89	
74F1766	48	Burst Mode DRAM Controller		
74F1779	16	8-Bit Up/Down Counter, Common I/O(3-state), (Extended function of 74F779)	A	SOL
74F1804	20	Hex 2-Input NAND Driver(Center Power Pin 74F804)	A	SOL
74F1805	20	Hex 2-Input NOR Driver (Center Power Pin 74F805)	A	SOL
74F1808	20	Hex 2-Input AND Driver (Center Power Pin 74F808)	Q3 89	
74F1832	20	Hex 2-Input OR Driver (Center Power Pin 74F832)	Q3 89	
74F2952	24	Octal Transceiver, NINV (3-state)	A	SOL/PLCC
74F2953	24	Octal Transceiver, INV (3-state)	A	SOL/PLCC
74F3037	16	Quad 2-Input 30Ω Line Driver, NINV	A	SOL
74F3038	16	Quad 2-Input 30Ω Line Driver, NINV (OC)	A	SOL
74F3040	16	Dual 4-Input 30Ω Line Driver, NINV	A	SOL
74F3893	20	Quad Futurebus Backplane Transceiver (3-state + OC)	Q3 89	
74F5074	14	Synchronizing Dual D-Type Flip-Flop	Q3 89	
74F5300	8	LED Driver		
74F8960	28	Octal Latched Bidirectional Future bus Transceiver INV (OC)	Q3 89	
74F8961	28	Octal Latched Bidirectional Future bus Transceiver NINV (OC)	A	SOL/PLCC
74F30240	24	Octal 30Ω Transmission Line/Backplane Driver, INV (OC)	A	
74F30244	24	Octal 30Ω Transmission Line/Backplane Driver, NINV (OC)	A	
74F30245	24	Octal 30Ω Transmission Line/Backplane Driver, INV	A	
74F30640	24	Octal 30Ω Transmission Line/Backplane Driver, NINV	A	
74F50109	16	Synchronizing Dual D-Type Flip-Flop	Q3 89	
74F50728	14	Synchronizing Cascaded Dual D-Type Flip-Flop	Q3 89	
74F50729	16	Synchronizing Dual D-Type Flip-Flop With Edge Triggered Set And Reset	Q3 89	

Signetics

FAST Products

Function Selection Guide

GATES

FUNCTION		DEVICE NUMBER
Inverters	Hex Inverter Hex Inverter Schmitt Trigger	74F04 74F14
NAND	Quad 2-Input Triple 3-Input Dual 4-Input, Schmitt Trigger Dual 4-Input 8-Input Quad 2-Input, Schmitt Trigger 13-Input	74F00 74F10 74F13 74F20 74F30 74F132 74F133
AND	Quad 2-Input Triple 3-Input	74F08 74F11
NOR	Quad 2-Input Triple 3-Input Dual 5-Input	74F02 74F27 74F260
OR	Quad 2-Input	74F32
Exclusive-OR	Quad 2-Input	74F86
Combination Gates	Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-Invert 4-2-3-2 Input AND-OR	74F51 74F64

GATES

FUNCTION	DEVICE NUMBER	CLOCK EDGE	SET	RESET	METASTABLE IMMUNITY
Dual D	74F74	↑	Low	Low	
Dual D	74F5074	↑	Low	Low	Yes
Dual D	74F50728	↑	Low	Low	Yes
Dual D	74F50729	↑	High	High	Yes
Dual J$\overline{K}$	74F109	↑	Low	Low	
Dual J$\overline{K}$	74F50109	↑	Low	Low	Yes
Dual JK	74F112	↓	Low	Low	
Dual JK	74F113	↓	Low	Low	
Dual JK	74F114	↓	Low	Low	

MULTIPLE FLIP-FLOPS

FUNCTION	DEVICE NUMBER	CLOCK EDGE	RESET	OUTPUT
Quad D	74F173	↑	High	NINV
Quad D with Master Reset	74F175	↑	Low	NINV INV
Quad D with Enable	74F379	↑		NINV INV
Hex D with Master Reset	74F174	↑	Low	NINV
Hex D with Enable	74F378	↑		NINV
Qctal D	74F273	↑	Low	NINV
Qctal D, 3-state	74F374	↑		NINV
Qctal D, 3-state	74F534	↑		INV
Qctal D with Enable	74F377	↑		NINV
Qctal D, 3-state	74F564	↑		INV
Qctal D, 3-state	74F574	↑		NINV

Function Selection Guide

OTHER REGISTERS, REGISTER FILES

FUNCTION	DEVICE NUMBER	CLOCK EDGE	PARALLEL ENTRY	BITS
Quad 2 Port, NINV, INV	74F398	↑	2D (Mux)	4 X 2
Quad 2 Port, NINV	74F399	↑	2D (Mux)	4 X 2
Octal MailBox with Ready Flag, 3-state	74F755	↑	8D	8
Dual Octal, 3-state	74F604	↑	8D	8
Dual Octal, OC	74F605	↑	8D	8
Register File	74F670	↑	2D	4 X 4
10-Bit, NINV, 3-state	74F821	↑	2D	10
10-Bit, INV, 3-state	74F822	↑	2D	10
9-Bit, NINV, 3-state	74F823	↑	2D	9
9-Bit, INV, 3-state	74F824	↑	2D	9
8-Bit, NINV, 3-state	74F825	↑	2D	8
8-Bit, INV, 3-state	74F826	↑	2D	8

LATCHES

FUNCTION	DEVICE NUMBER	ENABLE LEVEL	RESET LEVEL	OUTPUT
Dual Addressable	74F256	1 (Low)	Low	NINV
Dual Octal Latch	74F1604	1 (Low)		NINV
Octal Transparent, 3-state	74F373	1 (High)		INV
Octal Transparentl, 3-state (Broadside version of 74F373)	74F533	1 (High)		INV
Octal Transparent, 3-state	74F563	1 (High)		NINV
Qctal Transparent, 3-state (Broadside version of 74F373)	74F573	1 (High)		NINV
Multi-Mode, Buffered, 3-state	74F412	1 (Low), 3(High)	Low	NINV
Multi-Mode, Buffered, 3-state	74F432	1 (Low), 2(High)	Low	INV
8-Bit Addressable	74F259	1 (High)	Low	NINV
8-Bit Interface, 3-state	74F845	1 (High)	Low	NINV
8-Bit Interface, 3-state	74F846	1 (High)	Low	INV
9-Bit Interface, 3-state	74F843	1 (High)	Low	NINV
9-Bit Interface, 3-state	74F844	1 (High)	Low	INV
10-Bit Interface, 3-state	74F841	1 (High)		NINV
10-Bit Interface, 3-state	74F842	1 (High)		INV

MULTIPLEXERS

FUNCTION	DEVICE NUMBER	ENABLE LEVEL	SELECT INPUTS	OUTPUT
Dual 4-Input	74F153	2 (Low)	2(High)	NINV
Dual 4-Input	74F352	2 (Low)	2(High)	INV
Dual 4-Input, 3-state	74F253		2(High)	NINV
Dual 4-Input, 3-state	74F353		2(High)	INV
Quad 2-Input	74F157/157A	1 (Low)	1(High)	NINV
Quad 2-Input	74F158/158A	1 (Low)	1(High)	INV
Quad 2-Input, 3-state	74F257/257A		1(High)	NINV
Quad 2-Input, 3-state	74F258/258A		1(High)	INV
Quad 2-Input	74F298		1(High)	INV
Quad 3-Input	74F732		3(High)	NINV
Quad 3-Input	74F733		3(High)	INV
Quad 3-Input	74F712/712-1		2(High)	NINV
Quad 3-Input	74F723/723-1	1 (High)	2(High)	NINV
Quad 4-Input	74F725/725-1		2(High)	NINV
Quint 2-Input	74F711/711-1		1(High)	NINV
8-Input	74F151/151A	1 (Low)	3(High)	NINV, INV
8-Input, 3-state	74F251/251A		3(High)	NINV, INV

Function Selection Guide

DECODER/MULTIPLEXERS

FUNCTION	DEVICE NUMBER	ADDRESS INPUTS	ENABLE LEVEL	OUTPUT
Dual 1-of-4	74F139	2 + 2	1(Low) + 1(Low)	4(Low) + 4(Low)
Dual 1-of-4	74F539	2 + 2	1(Low) + 1(Low)	4(High) + 4(High)
1-of-8	74F138	3	2(Low), 1(High)	8(Low)
1-of-8	74F538	3	2(Low), 2(High)	8(High)
1-of-10	74F537	4	1(Low), 1(High)	10(High
1-of-16	74F154	4	2(Low)	16(Low)
Octal with Address Storage Latches and Acknowledge	74F547	3	1(Low), 2(High)	8(Low)
Octal with Acknowledge	74F548	3	2(Low), 2(High)	8(Low)

BUFFERS, DRIVERS, AND TRANSCEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Dual 4-Input NAND Transmission Line Driver	74F3040	INV
Dual 4-Input NAND Buffer	74F40	INV
Quad 2-Input NAND Buffer	74F37	INV
Quad 2-Input NAND Buffer, OC	74F38	INV
Quad 2-Input NAND Transmission Line Driver	74F3037	INV
Quad 2-Input Transmission Line Driver	74F3038	NINV
Quad FutureBus Backplane Transceiver, OC + 3-state	74F3893	NINV
Hex Inverter Buffer/ Driver, OC	74F06	INV
Hex Inverter Buffer/ Driver, OC	74F07	INV
Hex 2-Input NAND Driver, OC (Corner V_{CC} and GND)	74F804	INV
Hex 2-Input NAND Driver, OC (Center V_{CC} and GND)	74F1804	INV
Hex 2-Input NOR Driver, OC (Corner V_{CC} and GND)	74F805	INV
Hex 2-Input NOR Driver, OC (Center V_{CC} and GND)	74F1805	INV
Hex 2-Input AND Driver, OC (Corner V_{CC} and GND)	74F808	INV
Hex 2-Input AND Driver, OC (Center V_{CC} and GND)	74F1808	INV
Hex 2-Input OR Driver, OC (Corner V_{CC} and GND)	74F832	INV
Hex 2-Input OR Driver, OC (Center V_{CC} and GND)	74F1832	INV
Octal Inverter Buffer, OC	74F756	INV
Octal Buffer, OC	74F757	NINV
Octal Buffer/, OC	74F760	NINV
Octal 30Ω Transmission Line/Backplane Driver, OC	74F30240	INV
Octal 30 Transmission Line/Backplane Driver, OC	74F30244	NINV
Octal 30 Transmission Line/Backplane Transceiver, OC with Enable + 3-state	74F30245	NINV
Octal 30 Transmission Line/Backplane Transceiver, OC with Enable + 3-state	74F30640	INV
Octal Transceiver, OC	74F621	NINV
Octal Transceiver, OC	74F623	NINV
Octal Transceiver, OC	74F641	NINV
Octal Transceiver, OC	74F642	INV
Octal Transceiver/Register, OC	74F647	NINV
Octal Transceiver/Register, OC	74F649	INV
Octal Transceiver/Register, OC + 3-state	74F653	INV
Octal Transceiver/Register, OC + 3-state	74F654	NINV
Pi-Bus Transceiver (Octal Bidirectional Latched Transceiver), OC	74F776	NINV
Octal Latched Bidirectional Futurebus Transceiver, OC	74F8960	INV
Octal Latched Bidirectional Futurebus Transceiver, OC	74F8961	NINV

Function Selection Guide

SHIFT REGISTERS

FUNCTION	DEVICE NUMBER	BITS	SERIAL ENTRY	PARALLEL ENTRY	CLOCK EDGE
Serial-In/Parallel-Out	74F164	8	D_{sa}, D_{sb}		↑
Serial-In/Parallel-Out Output latch, 3-state	74F595	8	D_S		↑
Serial-In/Parallel-In/Serial-Out, Parallel-Out	74F195	4	J,K	4D	↑
Serial-In/Parallel-In/Parallel-Out, Shift Right	74F199	8	J,K	8D	↑
Serial-In/Parallel-In/Serial-Out, Parallel-Out	74F598	8	D_{s0}, D_{s1}	8 I/O	↑
Serial-In/Parallel-In/Serial-Out	74F674	16	SI/O	SI/O, 16D	↓
Serial-In/Parallel-In/Serial-Out	74F676	16	SI	16D	↑
Serial-In/Parallel-In/Serial-Out, 10/9 Bit	74F847	10/9	D_S	10D	↑
Serial-In/Parallel-In/Parallel-Out, Shift Right, 3-state	74F395	4	D_S	4D	↑
Serial-In/Parallel-In/Serial-Out, Parallel-Out, 3-state	74F322	8	D_0, D_1	8 I/O	↑
Serial-In/Parallel-In/Parallel-Out	74F194	4	D_{sr}, D_{sl}	4D	↑
Serial-In/Parallel-In/Parallel-Out, Shift Right	74F199	8	J, $\overline{K}$		↑
Serial-In/Parallel-In/Serial-Out	74F166	8	D_S		↑
Serial-In/Parallel-In/Parallel-Out, Bidirectional	74F198	8	D_{sr}, D_{sl}	8D	↑
Serial-In/Parallel-In/Serial-Out, Parallel-Out, 3-state	74F299	8	D_{s0}, D_{s7}	8 I/O	↑
Serial-In/Parallel-In/Serial-Out, Parallel-Out, 3-state	74F323	8	D_{s0}, D_{s7}	8 I/O	↑
Parallel-In/Serial-In/Serial-Out, Multiplexed Inputs	74F539	8	D_S, D_{na}, D_{nb}	8D	↑
Parallel-In/Serial-In/Serial-Out, 2:1 Multiplexed Inputs	74F835	8	D_S, D_{na}, D_{nb}	8D	↑
Parallel-In/Serial-Out, Input Latch	74F597	8	D_S	8D	↑
Parallel-In/Parallel-Out, 3-state	74F350	4	SI/O	4Y	↑
Parallel-In/Parallel-Out, 3-state	74F604	16		A_0-A_7, B_0-B_7	↑
Parallel-In/Parallel-Out, OC	74F605	16	I_{-3}, I_{+3}	A_0-A_7, B_0-B_7	↑
Parallel-In/Parallel-Out, True and Complement Output	74F398	8	S	I_{0a}-I_{0d}, I_{1a}-I_{1d}	↑
Parallel-In/Parallel-Out	74F399	8	S	I_{0a}-I_{0d}, I_{1a}-I_{1d}	↑

COUNTERS

FUNCTION	DEVICE NUMBER	MODULUS	PRESETTABLE	PARALLEL ENTRY	CLOCK EDGE
Synchronous (Asynchronous Reset)	74F160A	10	X	Synchronous	↑
Synchronous (Asynchronous Reset)	74F161A	16	X	Synchronous	↑
Synchronous (Synchronous Reset)	74F162A	10	X	Synchronous	↑
Synchronous (Synchronous Reset)	74F163A	16	X	Synchronous	↑
Up/Down, Decade	74F168	10	X	Synchronous	↑
Up/Down, Binary	74F169	16	X	Synchronous	↑
Up/Down, BCD Decade	74F190	10	X	Asynchronous	↑
Up/Down, BCD Binary	74F191	16	X	Asynchronous	↑
Up/Down, BCD Decade	74F192	10	X	Asynchronous	↑
Up/Down, BCD Binary	74F193	16	X	Asynchronous	↑
Bidirectional, Binary	74F269	256	X	Synchronous	↑
Up/Down, 3-state	74F568	10	X	Synchronous	↑
Up/Down, 3-state	74F569	16	X	Synchronous	↑
Up/Down	74F579	256	X	Synchronous (I/O)	↑
Up/Down, 3-state Multiplexed	74F779	256	X	Synchronous (I/O)	↑
Up/Down, 3-state Multiplexed	74F1779	256	X	Synchronous (I/O)	↑
Ripple counter	74F393	10	X		↓

Function Selection Guide

THREE-STATE BUFFERS, DRIVERS, AND TRANSCEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Quad Buffer	74F125	NINV
Quad Buffer	74F126	INNV
Quad Bus Transceiver	74F242	INV
Quad Bus Transceiver	74F243	NINV
Quad Bus Transceiver	74F1242	INV
Quad Bus Transceiver	74F1243	NINV
Hex Buffer	74F365	NINV
Hex Inverter	74F366	INV
Hex Buffer, 4-Bit and 2-Bit	74F367	INNV
Hex Inverter, 4-Bit and 2-Bit	74F368	INV
Octal Buffer	74F240	INV
Octal Buffer	74F241	NINV
Octal Buffer	74F244	NINV
Octal Buffer	74F1240	INV
Octal Buffer	74F1241	NINV
Octal Buffer	74F1244	NINV
Octal Buffer with Parity	74F455	INV
Octal Buffer with Parity	74F456	NINV
Octal Buffer with Parity	74F655A	INV
Octal Buffer with Parity	74F656A	NINV
Octal Driver	74F540	INV
Octal Driver	74F541	NINV
Octal Transceiver	74F245	NINV
Octal Transceiver	74F545	NINV
Octal Transceiver with IEEE-488 Termination Resistors	74F588	NINV
Octal Transceiver	74F620	INV
Octal Transceiver	74F622	INV
Octal Transceiver	74F640	INV
Octal Transceiver	74F1245	NINV
Octal Transceiver with Parity	74F657/657A	NINV
Octal Transceiver/Register	74F646/646A	NINV
Octal Transceiver/Register	74F648/648A	INV
Octal Transceiver/Register	74F651/651A	INV
Octal Transceiver/Register	74F652/652A	NINV
10-Bit Buffer	74F827	NINV
10-Bit Buffer	74F828	INV
10-Bit Transceiver	74F861	NINV
10-Bit Transceiver	74F862	INV
9-Bit Transceiver	74F863	NINV
9-Bit Transceiver	74F864	INV
Octal Registered Transceiver	74F543	NINV
Octal Registered Transceiver	74F544	INV
8-Bit Registered Transceiver	74F2952	NINV
8-Bit Registered Transceiver	74F2953	INV
Octal Registered Transceiver with Parity and Status Flags	74F552	INV
Octal Shift/Count Transceiver with Adder and Parity	74F807	INV

Function Selection Guide

PRIORITY ENCODERS

FUNCTION	DEVICE NUMBER	ENABLE LEVEL	INPUT/OUTPUT LEVEL
8-to-3	74F148	Low	Active Low

ARITHMETIC FUNCTIONS

FUNCTION	DEVICE NUMBER
4-Bit ALU	74F181
4-Bit ALU	74F381
4-Bit ALU with Overflow Output for Two's Complement	74F382
ALU Function Generator	74F881
4-Bit Binary Full Adder with Ripple Carry	74F83
4-Bit Binary Full Adder with Fast Carry	74F283
Look Ahead Carry Generator	74F182
Look Ahead Carry Generator	74F882
Quad Serial Adder/Subtractor	74F285
4-Bit BCD Arithmetic Logic Unit	74F582
4-Bit BCD Adder	74F583

COMPARATORS

FUNCTION	DEVICE NUMBER
4-Bit Identity Comparator	74F85
8-Bit Comparator	74F521
8-Bit Register Comparator	74F524

PARITY

FUNCTION	DEVICE NUMBER
9-Bit Odd/Even Parity Generator/Checker	74F280A/280B

SPECIAL FUNCTIONS

FUNCTION	DEVICE NUMBER
16 X 4 Synchronous FIFO With Ready Enables (3-state)	74F222
16 X 4 Synchronous FIFO (3-state)	74F224
16 X 5 Asynchronous FIFO (3-state)	74F225
64-Bit RAM	74F189A/219A
Register Stack-16 X 4 RAM 3-State Output Register	74F410
DRAM Dual-Ported Controller with Refresh	74F764
DRAM Dual-Ported Controller without Latch	74F765
4-Bit Asynchronous Bus Arbitor	74F786
DRAM Interrupt Vector Controller	74F1761
1 MBit Memory Address Controller	74F1762
1 MBit Intelligent DRAM Controller	74F1763
1 MBit DRAM Dual Ported Controller with Latch	74F1764
1 MBit DRAM Dual Ported Controller without Latch	74F1765
Burst Mode DRAM Controller	74F1776
1 MBit Intelligent DRAM Controller	74F4763
LED Driver	74F5300

Signetics

Section 2
Quality and Reliability

FAST Products

FAST Products

QUALITY ASSURANCE PROGRAMS

SIGNETICS'QUALITY PROGRAM

In 1979, Signetics recognized that quality was becoming a major competitive issue, not only in the semiconductor business, but also in other industries. Increases in the volume of products imported from the Far East (steel, automobiles, and consumer electronics) sent strong signals that new competitive forces were at work.

Signetics quickly began to investigate a variety of quality programs. The company realized that quality improvement would require a contribution from all employees. Management commitment and participation, however, was recognized as the primary prerequisite for this program to work successfully. Resources required for the resolution of defects were under management control.

In 1980, Signetics developed a program which focused on quality management. Rearranging previous quality control philosophies, Signetics developed a decentralized, distributed quality organization and simultaneously installed a quality improvement process based on the 14-Step improvement program advocated by Phil Crosby. The process was formally begun company-wide in 1981.
Since then, substantial progress has been made in every aspect of Signetics' operations. From incoming raw material conformance to improvements in administrative clerical errors — every department and individual is involved and striving for Zero Defects. Zero Accept sampling plans and Zero Defects warranties are evidence of Signetics' ongoing commitment and progress in quality.

Today, Signetics' quality improvement process has had a far-reaching impact on all aspects of our business. Signetics provides its customers with products of refined electrical and mechanical quality. And through continual use and modification of the Crosby program, Signetics is providing itself with a well-defined method of managing ongoing improvement efforts.

SIGNETICS' ZERO DEFECTS WARRANTY

In recent years, American industry has demanded increased product quality of its IC suppliers in order to meet growing international competitive pressure. As a result of this quality focus, it is becoming clear that what was once thought to be unattainable — Zero Defects — is, in fact, achievable.

Signetics offers a Zero Defects Warranty which states that it will take back an entire lot if a single defective part is found. This precedent setting warranty has effectively ended the IC industry's "war of the AQLs" (Acceptable Quality Levels). The ongoing efforts of IC suppliers to reduce PPM (Parts Per Million) defect levels is now a competitive customer service measure.This intense commitment to quality provides an advantage to today's electronics OEM. That advantage can be summed up in four words: ***Reduced Cost of Ownership***

As IC customers look beyond purchase price to the total cost of doing business with a vendor, it is apparent that a quality-conscious supplier, like Signetics, represents a viable cost reduction resource. Consistent high-quality circuits reduce requirements for expensive test equipment and personnel, and allow for smaller inventories, less rework, and fewer field failures

SIGNETICS' STATISTICAL PROCESS CONTROL (SPC)

Although application of statistics in our process development and manufacturing activities goes back to the early 1970's, the corporate-wide emphasis on Statistical Process Control (SPC) did not come about until mid-1984.

A natural evolution of our quality process made introduction of SPC and other related programs an inevitable event. SPC was, therefore, introduced under the quality umbrella.

The objective of the SPC program is to introduce a systematic and scientific approach to business and manufacturing activities. This approach utilizes sound statistical theory. Managers are expected to be able to turn data into information, and make decisions solely based on data (not perceptions).

The most critical and challenging aspect of implementing SPC is establishment of a discipline within the operating areas so that decision making is fundamentally based on verifiable data, and actions are documented. The other is realization of the fact that statistical tools merely point out the problems and are not solutions by themselves. The burden of action on the process is still on the implementers' shoulders. In order to implement SPC effectively, three steps are continually followed:

Documenting and understanding the process, using process flow charts and component diagrams.

Establishing data collection systems, and using SPC tools to identify process problems and opportunities for improvement.

Acting on the process, and establishing guidelines to monitor and maintain process control.

Repeating steps 1-3 again.

These fundamentals are the basis of establishing Signetics' specifications and operating philosophy with respect to SPC. Signetics believes a solid foundation creates a permanent system and accelerates our quality improvement process.

SIGNETICS QUALITY PERFORMANCE

Signetics Quality Improvement Program has influenced our entire production cycle — from the purchase of raw materials to the shipment of finished product. The involvement of all areas of the company has resulted in impressive quality improvements. A traditional quality gauge is final product electrical and visual-mechanical defect levels as measured upon first submittal results at Signetics outgoing Quality Assurance gates; Estimated Process Quality (This is the PPM Level at our first outgoing inspection for all ac-

Quality And Reliability

cepted and rejected lots.) (Figures I and II). Current product shipments routinely record below 20 PPM (Parts Per Million) electrical defect levels and 150 PPM visual-mechanical defect levels. Since Signetics utilizes zero accept sampling on all finished product inspection, any lot with one or more rejects is 100 percent retested.

The most meaningful measure of our product quality is how we measure up to our customers' expectations. Many customers routinely send us incoming inspection data on our products. One major mainframe manufacturer has reported zero defects in electrical, visual-mechanical, and hermeticity and has reported a 100 percent lot acceptance rate on Signetics' Standard Products products for over a year. Due to this type of performance, an increasing number of our customers are eliminating expensive incoming inspection testing and have begun implementation of Signetics' Ship-to-Stock program.

SIGNETICS' SHIP-TO-STOCK PROGRAM

Ship-to-Stock is a formal program developed at the request of our customers to help them reduce their costs by eliminating incoming test and inspection. Through close work with these customers in our quality improvement program, they became confident that our defect rates were so low that the redundancy of incoming inspections and testing was not only expensive, but unnecessary. They also saw that added component handling

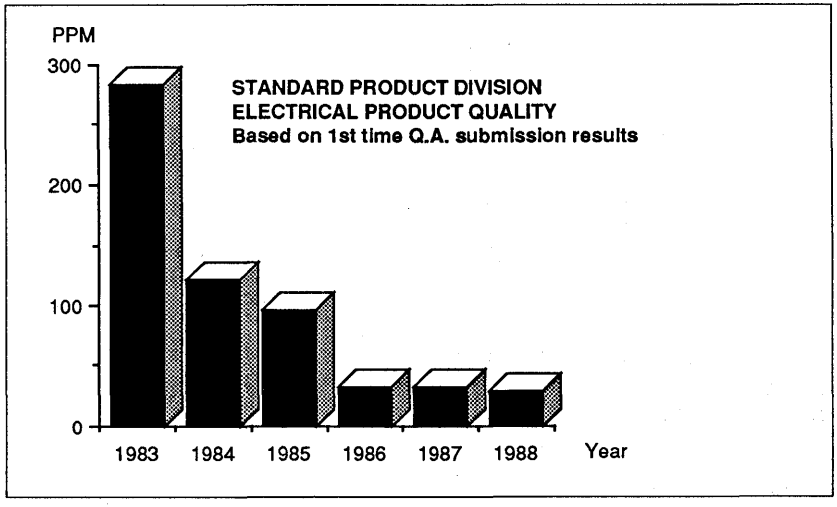


Figure I

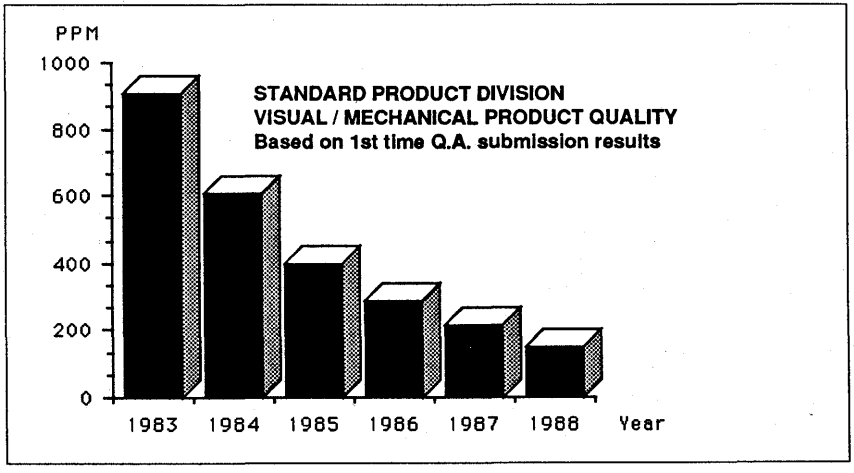


Figure II

increased the potential of causing defects.

Ship-to-Stock is a joint program between Signetics and a customer which formally certifies specific parts to go directly into the customer's assembly line or inventory. This program was developed at the request of several major manufacturers after they had worked with us and had a chance to experience the data exchange and joint corrective action occurring as part of our quality improvement program.

Manufacturers using large volumes of ICs, those who are evaluating Just-in-Time delivery programs, or those who want to reduce or avoid high-cost incoming inspection are strongly encouraged to participate in this worthwhile program. Contact your local Signetics' sales representative for further assistance and information on how to participate in this program.

SUMMARY

The Signetics Quality Improvement Program has had a far-reaching impact on all aspects of our business. It has, of course, provided our customers with products of improved electrical and mechanical quality and has provided Signetics with a method of managing product reliability improvement to ensure that Signetics' products continue to perform as specified.

The corrective action teams that work to eliminate the cause of defects in Signetics' products are committed to producing highly reliable integrated circuits and, as demonstrated by our continually improved product reliability performance, we are well on the way to achieving our objective, **ZERO DEFECTS.**

RELIABILITY ASSURANCE PROGRAMS

FOCUS ON PRODUCT RELIABILITY

During the period from 1981 to 1984, continuing improvements in process and material quality had a significant impact on product reliability.

Since 1984, Signetics has intensified its efforts to markedly improve product reliability. Corporate Reliability Engineering, Division and Plant Reliability Units, Philips Research Labs-Sunnyvale, and Manufacturing Engineering work jointly on numerous improvement activities. These focused activities enhance the reliability of Signetics future products by providing improved methods for reliability assessment, increased understanding of failure physics, advanced analytical techniques, and aid in the development of materials and processes.

RELIABILITY MEASUREMENT PROGRAMS

Signetics has developed comprehensive product and process qualification programs to assure that its customers are receiving highly reliable products for their critical applications. Additionally, ongoing reliability monitoring programs, SURE III and Product Monitor, sample standard production product on a regularly established basis (see Table I below).

DESCRIPTION OF STRESSES

SHTL — Static High Temperature Life: SHTL stressing applies static DC bias to the device. This has specific merit in detecting ionic contamination problems which require continuous uninterrupted bias to drive contaminants to the silicon surface. The voltage bias must be main-

Table I Reliability Assurance Programs

Reliability Function	Typical Stress	Frequency
New Process Qualification	High Temperature Operating Life Temperature-Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle	Each new wafer fab process
New Product Qualification	High Temperature Operating Life Temperature-Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle Eletrostatic Discharge Characterization	Each new product family
SURE III	High Temperature Operating Life Temperature-Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle Thermal Shock	Each fab process family, every four weeks
Product Monitor	Pressure Pot Thermal Shock	Each package type and technology family at each assembly plant, every week

tained until the devices are cooled down to room temperature from the elevated life test temperature. DHTL stressing is not as effective in detecting such problems because the bias continuously changes, intermittently generating and healing the problem. For this reason, SHTL has typically been used as the accelerated life stress for Standard Products products.

HTSL — High Temperature Storage Life: This stress exposes the parts to elevated temperatures (150°C-175°C) with no applied bias. For plastic packages, 175°C is the high end of its safe temperature region without accelerating untypical failure mechanisms. This test is intended to accelerate mechanical package-related failure mechanisms such as Gold-Aluminum bond integrity and other process instabilities.

THBS — Temperature-Humidity, Biased, Static: This accelerated temperature and humidity bias stress is performed at 85°C and 85% relative humidity (85°C/85% RH). In general, the worst case bias condition is the one which minimizes the device power dissipation and maximizes the applied voltage. Higher power dissipations tend to lower the humidity level at the chip surface and lessen the corrosion susceptibility.

TMCL — Temperature Cycling, Air-to-Air: The device is cycled between the specified upper and lower temperature without power in an air or nitrogen environment. Normal temperature extremes are -65°C and +150°C with a minimum 10 minute dwell and 5 minute transition per Mil-STD-883C, Method 1010.5, Condition C. This is a good test to measure the overall package to die mechanical compatibility, because the thermal expansion coefficients of the plastic are normally very much higher than those of the die and leadframe. However, for large die the stress may be too severe and induce failures that would not be expected in a real application.

PPOT — Pressure Pot: This stress exposes the devices to saturated steam at elevated temperature and pressure. The standard condition is 20 PSIG which occurs at a temperature of 127°C and 100% RH. The stress is used to test the moisture resistance of plastic encapsulated devices. The plastic encapsulant is not a moisture barrier and will saturate with moisture within 72 hours. Since the chip is not powered up the chip temperature and relative humidity will be the same as the autoclave once equilibrium is reached. Because the steam environment has an unlimited supply of moisture and ample temperature to catalyze thermally activated events, it is effective at detecting corrosion problems, contamination induced leakage problems, and general glassivation stability and integrity. It is also a good test for both package integrity (cracks in the package), and for die cracks (the moisture swells the plastic enough to stress the die — also the moisture causes leakage paths in the crack itself).

TMSK — Thermal Shock, Liquid-to-Liquid: Similar to TMCL, except that, heating and cooling are done by immersing the units in hot and cold inert liquid. Temperature extremes are -65°C to +150°C with a minimum 5 minute dwell and less than 10 second transition per Mil-STD-883C, Method 1011.4, Condition C. Since heat transfer by conduction is generally much faster than by convection, the liquid-based thermal shock causes more rapid temperature changes in the part. Also, as the part is rapidly changing in temperature all its mass will not be in equilibrium and the temperature gradients across the part will produce additional mechanical stress. For chip-out under bond these factors combine to give an acceleration of 1.5X over TMCL. For ball neck break (wire creep) failures, acceleration of 10X has been observed. To date, there is no reasonable explanation for why the relative accelerations in TMCL and TMSK are so variable and dependent on the failure mechanism.

PRODUCT AND PROCESS QUALIFICATIONS

Qualification activity is centered around new products and processes and changes in products and processes. The goal is to assure that the products can meet the qualification requirements prior to general release, and on an ongoing basis to demonstrate conformance to those requirements. The nature and extent of reliability stressing required depends on the type of change and the amount of applicable reliability data available.

A full qualification may include Early Failure Rate (EFR), Intrinsic Failure Rate (IFR), and Environmental Endurance Stressing. Such stress plans are reserved for introductions or changes that involve new or untested material or processes and, as such should be subjected to the maximum reliability interrogation. This normally entails a full range of biased and unbiased temperature and humidity stresses along with thermo-mechanical stresses.

For changes that are of limited scope, the full range of qualification stressing may not be warranted. In these instances, the nature and extent of the change is examined and only those stresses which provide a valuable measure of the change, or those which will detect potential weaknesses, are performed.

SIGNETICS' SELF-QUAL PROGRAM (SSQP)

Self-Qual is a joint program between Signetics and a customer which formally communicates Signetics' qualification activities for a new or changed product, process, or material. The Signetics Self-Qual process provides our customer's engineering groups an opportunity to participate in the development of the qualification plan. During the qualification process, customers may audit the project, and can receive interim updates of qualification progress. Upon completion, formal detailed engineering reports are provided.

The major impact to the customer comes from the reduced workload on the component engineering and qualification groups. These engineering resources generally divide their time between routine qualification activity and problem resolution on critical components. By eliminating the need to perform qualification for some of the basic vendor changes the customer component engineer can spend more of his time resolving the critical product issues. In addition, the total amount of stress hardware needed to perform qualification life tests and other environmental evaluations can be reduced, saving the customer facility costs and reducing operating expense.

Quality And Reliability

Self-Qual is a no-risk proposition for the customer. Each Self-Qual proposal provides a detailed description of what we are changing and why. It includes a detailed plan of what we intend to do to establish the reliability of the products affected. If the customer wishes to have products added to the plan, or select some additional stresses, or prefers alternative stress conditions, Signetics will do everything possible to accommodate those requests. After that, if the customer is still uncomfortable with the recommended change, they are under no obligation to accept our data, and they may perform their own qualification program in addition to Signetics.

Customers who are interested in participating in this program should contact their local Signetics sales representative or Signetics' Corporate Reliability Engineering department directly.

SURE III RELIABILITY MONITORING PROGRAM

In order to implement an improvement program, a standard measure of performance was needed. Signetics uses the results from the SURE III Reliability Monitoring Program as its basic ongoing measure of product reliability performance. This program samples all generic families of products manufactured by Signetics, and utilizes standardized stress methods and test procedures. This system is augmented by new product and process qualification activities and infant mortality monitoring programs.

Signetics adopted a measurement philosophy based on the premise of continual improvement toward our performance standard of zero defects.

We also increased our standard Pressure Pot stress conditions from 15 PSIG/121°C to 20 PSIG/127°C. This reduced stress duration from 168 hours to 72 hours, and increased high volume sampling, which increased sensitivity to low defect levels.

Our standard monitoring program, SURE III, includes the stress conditions as described in Table II:

PRODUCT MONITOR

In addition to the SURE III program, each Signetics assembly plant performs Pressure Pot (20 PSIG, 127°C, 72 Hours) and Thermal Shock (-65°C to +150°C, 300 Cycles) reliability monitors on a weekly basis for each molded package type by pin count. The purpose of this program is to monitor the consistency of the assembly operations for such attributes as molding quality and die attach and wire bond integrity. These data are reported back to manufacturing operations and corporate and divisional reliability and quality assurance departments by electronic mail each week.

Table II SURE III Reliability Monitoring Programs

Reliability Function	Stress Conditions
Static HighTemperature Operating Life (SHTL)	$T_j \geq 150°C$, T_a = 125°C to 150°C, Bias condition = Static, V_{CC} = MAX, Duration = 1000 hours
High Temperature Storage Life (HTSL)	T_a = 150°C, Bias condition = None, Duration = 1000 hours
Temperature-Humidity, Biased, Static (THBS)	T_a = 85°C ± 3°C, Humidity = 85% RH ± 5% Bias condition = Static, V_{CC} = MAX, Duration = 1000 hours
Temperature Cycling (TMCL)	T_a = -65°C (+0°C - 10°C) to +150°C (+10°C - 0°C), Air-to-Air, Dwell time = 10 minutes minimum each extreme Bias condition = None, Duration = 1000 cycles for plastic package = 300 cycles for ceramic package
Pressure Pot	T_a =127°C ±2°C , 20 PSIG ±0.5 PSIG (PPOT), 100% saturated steam, Bias condition = None, Duration = 72 hours
Thermal Shock (TMSK)	T_a = -65°C (+0°C - 10°C) to +150°C (+10°C - 0°C), Liquid-to-Liquid, Dwell time = 5 minutes minimum each extreme Bias condition = None

NOTE 1: V_{CC}= MAX is generally equal to V_{CC}= MAX as specified in Data Manual .

Quality And Reliability

RELIABILITY EVALUATIONS

In addition to the product performance monitors encompassed in the SURE III program, Signetics' Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering process are:

Evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities, and subcontractors.

Device or generic group failure rate studies.

Advanced environmental stress development.

Failure mechanism characterization and corrective action/prevention reporting.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE III program, however, more highly-accelerated conditions and extended durations typify these engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity, are often included in some evaluation programs.

STRESS FACILITY QUALITY

Signetics quality improvement has reached all functional areas of the company, and the reliability stress laboratories are no exception. Corporate Reliability Laboratory (CRL) is one of the many areas where the benefits of the quality improvement process pays repeated dividends.

CRL utilizes stresses which accelerate failure rates hundreds to thousands of times, requiring precision and control to make reliability data meaningful. Stress loading schedules are maintained with absolute regularity and chambers are never off-line beyond scheduled loading plans. Board currents are recorded prior to and at each interval on biased stresses, and monitoring of in-oven currents is conducted daily.

Thermal modeling of both Thermal Shock and Temperature Cycling systems has been accomplished and all loads are carefully weighed to ensure that thermal ramps are consistent.

Pressure Pot and Biased Pressure Pot systems utilize microprocessor controllers, and are accurate to within 0.1 degree centigrade. Saturation is guaranteed via automatic timing circuits, and a host of fail-safe controls ensure that test groups are never damaged.

Electrostatic discharge (ESD) handling precautions are standard procedures in the laboratories, and the occurrences of devices lost, zapped, or overstressed have become almost non-existent.

RELIABILITY IMPROVEMENT PROGRAMS

Currently, Signetics is involved in a number of reliability improvement programs intended to enhance product reliability performance. A series of activities are currently addressing failure rate reduction in thermal cycling stresses, particularly on large die. Other reliability improvement programs involve the use of Silicon Nitride and other technologically advanced passivation systems to increase the high humidity resistance of sensitive products.

Reducing early life failures has become a major focus at Signetics. Numerous corrective action teams are in the process of establishing high volume monitors capable of accurately describing parts per million (PPM) level infant failure rates. From data produced via these monitors, improvement in wafer fabrication process and assembly process technologies are developed to minimize integrated circuit defect levels.

RELIABILITY PUBLICATIONS

Data from all of these activities is made available to all Signetics customers in a variety of publications:

PRODUCT RELIABILITY SUMMARIES and QUARTERLY UPDATES

Yearly, each Product Division's SURE III monitoring data is summarized and published in a Product Reliability Summary. A quarterly update is also published.

SSQP - SIGNETICS SELF-QUAL PROGRAM

In addition to the regular publications of reliability monitor results, a special program for the publication of qualification proposals and final engineering reports has been in place since January of 1984.

SMD RELIABILITY

In support of Signetics' leadership in Surface Mount Device (SMD) technology, we have published in-depth studies and evaluations on the reliability of numerous combinations of SMD packages and IC process technologies. These reports cover not only the basic product performance, but also evaluate products after exposure to the unique environments created by the various SMD soldering and cleaning processes.

SPECIAL RELIABILITY REPORTS

In addition to our standard reports, special reliability evaluation results are available on a wide variety of Signetics' products and processes. Custom reports can be generated to meet specific customer needs and the most accurate failure rate estimates can be prepared for your specific system application and environment.

DATA AVAILABILITY

The previously referenced documents are available to all Signetics customers. Many are available in your local Signetics sales office, or:

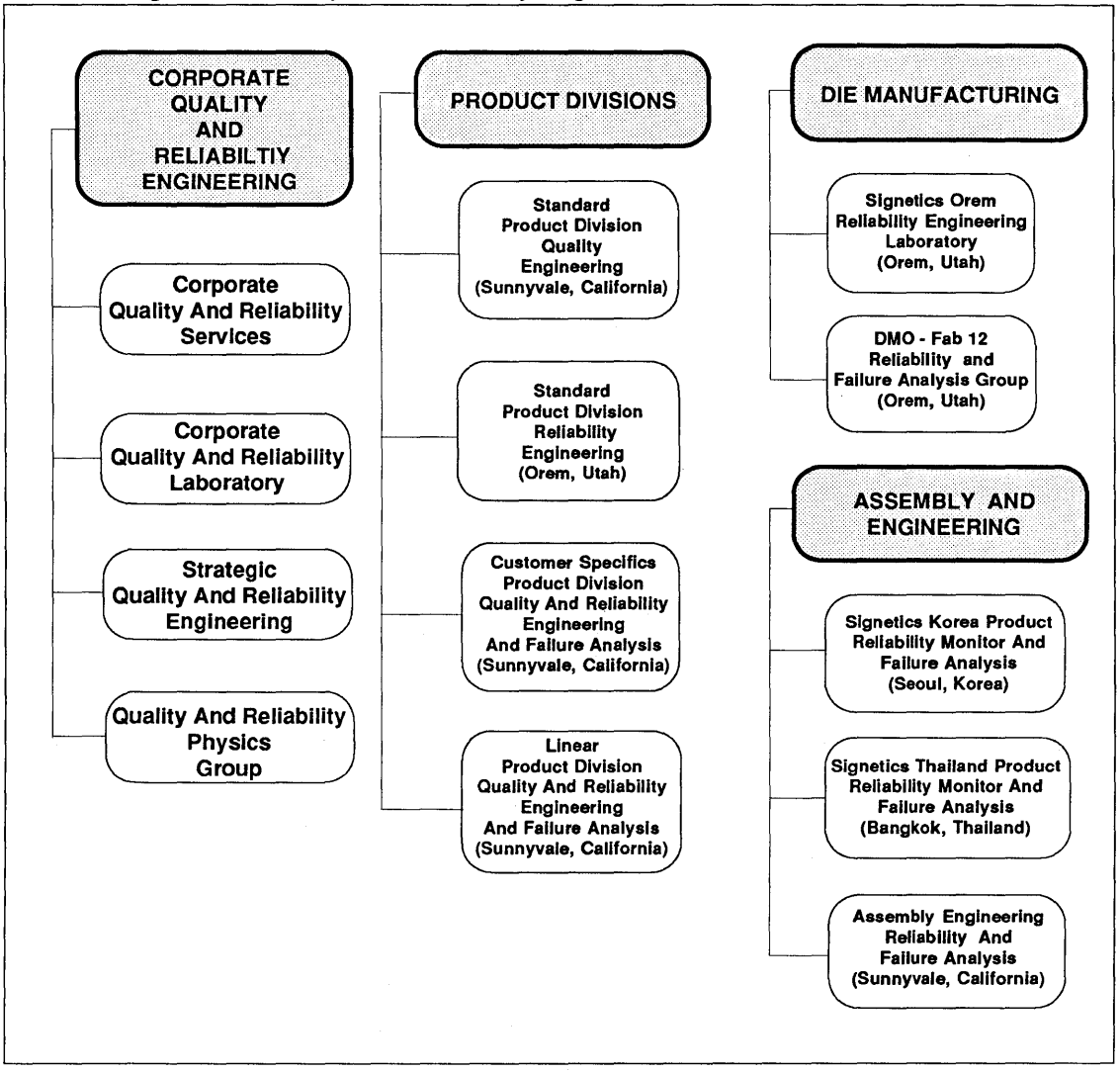
Corporate Reliability Services
Reliability Publications Group
Department 9605, Mail Stop #34
Arques Avenue
Box 3409
Sunnyvale, CA 94088-3409

where you can be placed on a standard mailing list for all documentation which meet your specific requirement(s).

Quality And Reliability

TheTable III below depicts the current organization for Signetics' Quality and Reliability Group.

Table III Signetic's Quality And Reliability Organization Chart



Quality And Reliability

SIGNETICS' MANUFACTURING FACILITIES

Signetics, as part of a multinational corporation, utilizes manufacturing facilities for wafer fabrication, package assembly, and test in three states and three overseas countries as shown in Table XII. All wafer fabrication is performed in Signetics operated fabs which report to the Vice President of Die Manufacturing Operations (DMO) in Sunnyvale. Similarly, Signetics Assembly operations in Utah, Korea, and Thailand, report to the Vice President of Assembly Manufacturing Operations (AMO). Assembly subcontractors, Pebei and Anam, are scheduled and controlled through the AMO organization. Assembly subcontractors process all product to Signetics' specifications and materials. Signetics has on-site quality assurance personnel at each subcontractor to audit assembly processes and procedures.

All Signetics products are electrically tested in Signetics operated facilities. These facilities report to the manufacturing organization (DMO or AMO) operating the facility at which they are located.

Table IV Signetic's Product Manufacturing Facilities

Facilities	Designation	Location	Process or Package Families
Wafer Fabrication	Fab 01	Sunnyvale, California	Bipolar Junction Isolated
	Fab 16	Orem, Utah	Oxide Isolated
	Fab 21	Sunnyvale, California	Bipolar Gold Doped, Schottky, Oxide Isolated, (ECL)
	Fab 22	Albuquerque, New Mexico	ACMOS
Assembly	Sigkor	Seoul, Korea	DIP, SO and PLCC
	SigThai	Bangkok, Thailand	DIP and CERDIP
	Orem	Orem, Utah	Military Final Test and Quality Assurance
	Pebei	Kaomsiung, Taiwan	SO
	Anam	Seoul, Korea	SO and Metal Can
Test	TA03	Sunnyvale, California	Wafer Sort, Final Test and Quality Assurance
	SigKor	Seoul, Korea	Final Test and Quality Assurance
	SigThai	Bangkok, Thailand	Final Test and Quality Assurance

TYPICAL IC MANUFACTURING FLOW

The manufacturing process for Integrated Circuits begins with wafer fabrication. The wafers are then electrically sorted, assembled, and tested prior to customer shipment. Quality assurance inspections are utilized throughout the manufacturing process. Table IV contains a typical manufacturing flow for Signetics' ICs.

Table V I.C. Manufacturing Flow For Bipolar Junction Isolated Product

Facilities	Manufacturing Flow	Facilities	Manufacturing Flow
Wafer Fab	Initial Oxidation Buried Laer Diffusion Epitaxial Layer Isolation Diffusion Base Diffusion Emitter Diffusion Contact Mask Metallization #1 Dielectric Glass Layer Metallization #2 Nitride Passivation	Assembly	Saw Scribe and Break Die Sort Visual Acceptance Die Attach to Leadframe Wire Bonding Pre-Seal Visual Acceptance Encapsulation Topside Symboiization Leadframe Trim and Form Solder Coat Mechanical/Visual Acceptance
Wafer Sort	Wafer Electrical Test Wafer Visual Acceptance	Test	Final Electrical Test Burn-In (Optional) Product Assurance Test
		Shipping	Pack-Out Outgoing Quality Control Acceptance Shipping

Table VI Package Construction

ITEMS	PDIP	SO/PLCC	CERDIP
Lead Frame	Copper, 194 Alloy	Copper, 194 or PMC102	Alloy-42
Lead Finish	Tin/Lead Solder Dip (60/40)	Tin/Lead Solder Dip (60/40) or Solder Plate (80/20)	Tin/Lead Solder Dip (60/40)
Bond Area Finish	Silver Spot	Silver Spot	Silver Spot
Die Attach	Silver filled Polymide or Thermoplastic	Silver Filled Polymide or Thermoplastic	Silver Filled Glass
Bond Wire	Gold, 1.0-1.3 mil Diameter	Gold, 1.0-1.3 mil Diameter	Aluminum, 1.0 mil Diameter
Wire Bonding Die Lead Frame	Thermosonic Ball Stitch	Thermosonic Ball Stitch	Ultrasonic Stitch Stitch
Package Material	Novolac Epoxy	Novolac Epoxy	Ceramic

Table VII Package Code Definition

Pin Count	PDIP	SO	PLCC	CERDIP
8	NE	DE	-	FE
14	NH	DH	-	FH
16	NJ	DJ	-	FJ
18	NK	-	-	FK
20	NL	DL	AL	FL
22	NM	-	-	FM
24	NN	DN	-	FN
28	NQ	-	AQ	FQ
-	-	AA	-	

Signetics

Section 3
Circuit Characteristics

FAST Products

INPUT STRUCTURES

There are three types of input structures used in FAST circuits: diffusion diode, PNP vertical transistor, and NPN transistor. Each of these are discussed below.

The diffusion diode input is most often used with FAST circuits. The input diode is labeled as D1 in Figure 1. There can be more than one if NAND logic is to be performed. In the oxide-isolated processes these are base-collector diffusions. Each input pin also has a Schottky clamp diode D2. This diode is standard for most TTL circuits, and is included to limit negative input voltage excursions that are generally the result of inductive undershoot.

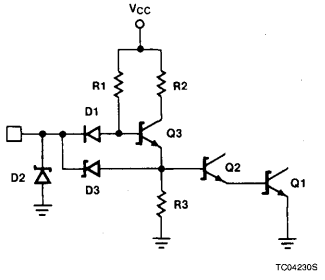


Figure 1. Diode Input

The static diode input function of voltage versus current is shown in Figure 2. If the pin voltage is negative, most of the relatively high negative current flows through the clamp Schottky D2. At 0V the current flows from V_{CC} through R1 and D1 to the pin. Switching from a logic Low level to a logic High level occurs when the input pin voltage rises high enough to force the current from the D1 path to the Q3 – Q2 – Q1 path. This happens when the base voltage of transistor Q3 is at three base-emitter drops ($3V_{BE}$), and the pin is at $2V_{BE}$, which is the standard FAST threshold switching voltage. At this voltage the input current is very small, just the leakage currents of diodes D1, D3, and clamp diode D2. The current remains at this small, positive value until breakdown voltage is reached.

Transistor Q3 and resistor R2 provide a current gain by increasing the amount of current available to Q2 and Q1 when the pin voltage is high. R3 bleeds current off the base of Q2 to pull it low when the pin voltage is low. D3 speeds up this process during the High-to-Low pin transition. When the switching transients are over, D3 is reverse biased.

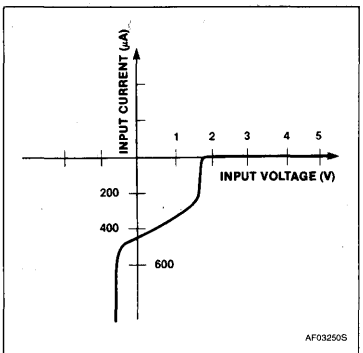


Figure 2. Static Diode Input Function of Voltage VS Current

The current of Figure 2 is scaled for the case where the pin is required to pull down a single 10KΩ resistor R1 (20μA maximum in the High state and 0.6mA maximum in the Low state), which is defined as a standard FAST Unit Load (UL). For some parts, pin current can exceed a UL, especially in the logic Low state. This will happen if the pin must sink the current from more than one R1 resistor, or if the value of R1 is less than 10KΩ, which will be the case if the capacitance at the base of the transistor Q3 is too large for the required switching speed. In this event, the actual number of ULs is listed for each input in the specification sheet for the part. Note: UL, as defined here, is less than the normally defined Schottky TTL Unit Load. The correlation is one Schottky Unit Load = 1.67 ULs. This is an important point to remember for fan-in and fan-out calculations in systems that mix FAST with other TTL families.

The PNP vertical transistor has found wide acceptance in its various forms in low power Schottky logic because it provides a high-impedance input which is usually desirable. It was not used with early FAST circuits because the original oxide-isolated processes did not provide a fully suitable PNP vertical structure. It is now frequently the input of choice for new parts built with improved processes. The PNP transistor Q3 is fabricated with the P-type substrate as the grounded collector, the N-type Epi as the base, and the P-type normal base diffusion as the emitter. The process must be tailored to provide a suitable current gain for this vertical structure and must have provision to remove the considerable substrate current without an appreciable rise in substrate voltage. Referring to Figure 3, Q3 functions as an emitter follower for pin voltages low enough to provide an emitter-base forward bias. This occurs at an emitter voltage below the $3V_{BE}$ value provided by the D3 – Q2 – Q1 stack, and gives the desired $2V_{BE}$ pin threshold. At pin voltages above this value, Q3 turns off and the current through R1 is directed to Q2 – Q1 through D3. The Schottky diode D2 speeds up the High to Low transition if the pin voltage falls more rapidly than the base of Q2; otherwise, D2 is off. The PNP input characteristics are shown in Figure 4. If the input voltage is negative with respect to ground, a large clamp current flows through D_1. As the voltage rises, D_1 turns off and the input current falls to the base current of Q3; for the usual values of R_1, this is in the range of about 10μA. This decreases as the lead voltage rises. At threshold, Q3 turns off and the input current drops to a low value determined by the leakage of D_1, D_2, and Q3. The current remains at this low value until the onset of breakdown. Since all PNP inputs are protected with ESD structures, the breakdown current is set by this, and not the actual PNP device.

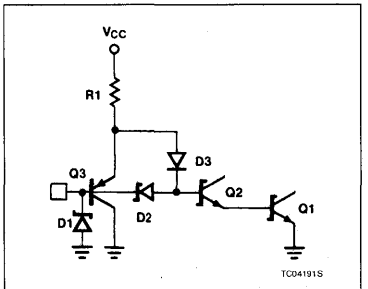


Figure 3. PNP Input

The NPN input is shown with two variations in Figures 5 and 6. It has limited use in standard TTL circuits, and is used in selected FAST devices, especially where its superior high-impedance input characteristics are useful. A typical plot of static input current versus input voltage is shown in Figure 7. There are some significant differences between this function and that of the diffusion diode input shown in Figure 2, the most important being the much lower input current in the region from 0V to

Circuit Characteristics

threshold and the controlled increase of input current above V_{CC}.

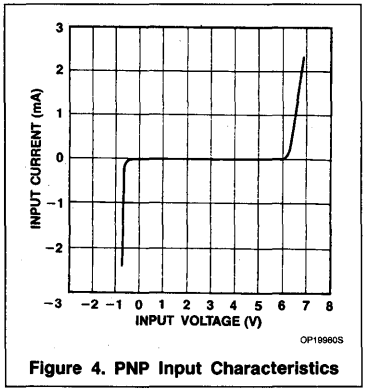


Figure 4. PNP Input Characteristics

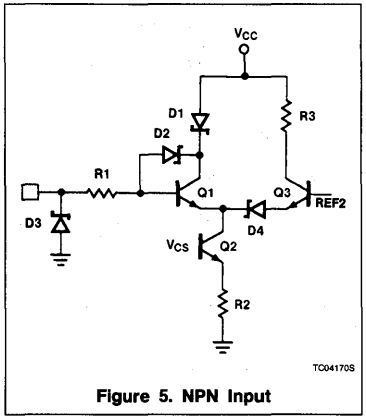


Figure 5. NPN Input

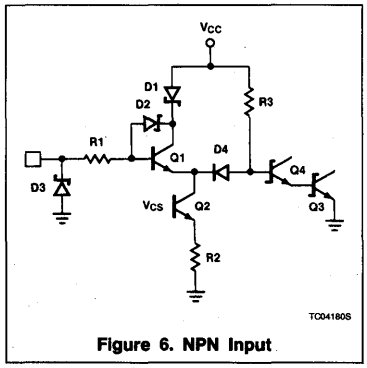


Figure 6. NPN Input

When the pin voltage is negative, the large negative clamp current is supplied through the clamp Schottky diode D3. For positive voltages, from 0V to the switching threshold of $2V_{BE}$, Q1 is off, and the input current I_{IL} is very small, just the leakage current of Q1, D2, and D3 with low reverse bias. As the input voltage rises above $2V_{BE}$, Q1 turns on, and the current that had been flowing through D4 now flows through Q1, blocking Schottky diode D1 to V_{CC}. The value of this current is determined by the current source transistor Q2 with its base connected to voltage reference V_{CS}, and by the size of the emitter resistor R2. The current is nearly constant within the normal operating range of input voltages and has a typical value of 0.1mA to 1.0mA. The pin must supply only a small fraction of this bias current, the ratio of Q1 collector current to base current being the bipolar β factor. Typically, I_{IH} base input current is less than 20μA in the voltage range from 0V to V_{CC}. This value is the specification for a standard FAST NPN Unit Load. As in the diode input case, if larger currents are needed to reduce delay times or to provide for multiple-input transistors connected to the same pin, the specification sheet for the particular device will identify the input pins which have NPN ULs larger than one, and will list their values.

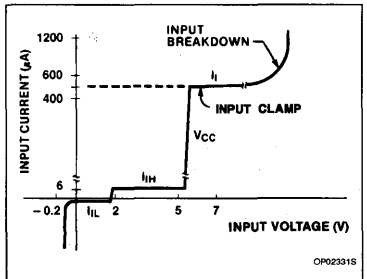


Figure 7. NPN Input Characteristics (Not to Scale)

In normal operation, the pin voltage will be limited in the negative direction by the diode clamp D3, and will be less than V_{CC} in the positive direction. The actual input voltage may exceed V_{CC} for three reasons: there may be inductive overshoot in badly terminated systems; the V_{CC} pin may be floating or grounded; or the input pin may be forced high by electrostatic discharge or incoming inspection testing.

For the inductive overshoot case, when the pin voltage exceeds V_{CC}, part of the Q1 collector current begins to flow from the pin through limiting resistor R1 and Schottky diode D2. The current from V_{CC} through D1 decreases by exactly this amount, since Q2 is a constant current source. As the voltage continues to rise, D1 becomes reverse biased and prevents high currents flowing from the pin into V_{CC}. All the Q2 current flows into the pin through the R1 – D2 – Q1 – Q2 – R2 path to ground. As stated before, this current is typically small, in the range of 0.1mA to 1.0mA, and nearly independent of pin voltage, as shown by the I_I plateau in Figure 7. I_I provides a clamping action to ground for pin voltages in excess of V_{CC}, which is usually desirable to reduce overshoot.

For the case where V_{CC} is grounded or floating, the input current is nearly zero for positive voltages between zero and approximately 7V. The conducting path through R1 – D2 – Q1 is available, but the current source Q2 will be shut off because, without V_{CC} drive, the Q2 base reference V_{CS} will be at 0V. This is the specified standard setup for incoming inspection. For the incoming inspection testing case where V_{CC} is connected to a 5V source, the response is shown in Figure 7. The current remains on the Q2-limited plateau until the pin voltage is high enough to cause non-destructive collector-emitter reach-through of Q2. At this point, input current increases as the pin voltage rises, and R1 functions to limit this current and prevent damage to Q2.

The electrostatic discharge case is similar to the incoming inspection case except that Q2 may be off if the V_{CC} pad is floating, in which case it breaks down at a slightly higher voltage. The NPN input produces reach-through at a relatively low voltage compared with the diode input. The effect of this non-destructive reach-through is to greatly increase the ability of the device to survive electrostatic discharge. The discharge current is passed through the chip at a relatively low power dissipation, and this is shared by elements R1, D2, Q1, Q2 and R2, so that none of them dissipate enough power to do damage. By way of contrast, with a diode input, the clamp Schottky diode breaks down at high voltage with high dissipation in a localized area, and may suffer damage.

Another advantage of the NPN input is its ability to interface on the chip to either a conventional TTL interior design, or to the increasingly popular current-mode interior logic. The conventional TTL interface is shown in Figure 6. In this case the Q2 current source is designed to provide sufficient current to insure that in the Low state, with current flowing through the R3 – D4 – Q2 path, the base-emitter stack of Q3 – Q4 is shut off. The $2V_{BE}$ input threshold is set by the forward drops of Q1, D4, Q4 and Q3.

The current-mode logic interface is shown in Figure 5. The output voltage is the drop across R3, and is referenced to V_{CC} (or some on-chip regulated voltage lower than V_{CC}) as is required for current-mode logic. For this case, voltage reference REF2 is normally fixed at $2V_{BE}$ + 1 Schottky drop to provide a pin threshold voltage of $2V_{BE}$. In fact, REF2 can be tailored to set the switching threshold voltage to any desirable level; it can be set to something other than an integral number of

Circuit Characteristics

base emitter drops, or it can be designed to reduce the sometimes undesirable temperature variations of input threshold.

INPUT CONSIDERATIONS

Static Input Current

A comparison of input current for various input voltage ranges for each of the three types of inputs is shown in Figure 8.

The majority of FAST devices available to date have diode inputs and supply current to their drivers that may be as large as 600μA at V_{IN} of 0.5V for a single unit load input. If a driver cannot sink the necessary current for a particular number of loads, the system designer must either add a buffer circuit designed to drive with higher current, or switch to devices that have high-impedance inputs. These are available on many Signetics FAST designs, and are specified to have input current less than 20μA over the full switching range from 0V to V_{CC}. Typical input current for the NPN structure at room temperature is less than 1μA below switching threshold voltage and 3μA above threshold. Typical PNP input current is less than 10μA below threshold voltage and 1μA above threshold.

Input Capacitance

Input capacitance, measured using a small-signal variation about a static DC operating point, is usually the least for the NPN. When one includes the added capacitance of the elements common to each input, such as the pin, pad, bond wire, and clamp Schottky diode, the percentage difference for total static input capacitance for any of the three types of inputs is not very large.

Dynamic Input Current

In many applications the total current an input pin draws during a switching transition is a more important consideration than its input capacitance. This dynamic input current is often larger than the value of static capacitance would predict because each of the three types of input structure normally includes some sort of speed-up mechanism, usually a "kicker" Schottky diode, connected to an internal node of the circuit. The kickers deliver current, related in a non-linear way to input edge-rates. High-dynamic input current does not always equate to fast circuit switching. NPN inputs are usually faster than diode or PNP inputs, but in general have the lowest total dynamic current. The percentage differences for dynamic current tend to be larger than the respective differences for static capacitance.

Switching Threshold Voltage

The FAST input switching threshold voltage is set quite high for TTL at two base-emitter junction forward-bias drops. FAST input structures have enough gain that the voltage range in which they switch from one state to the other, as shown by a static DC transfer function curve, is completed within about 100mV of the $2V_{BE}$ threshold. For a typical part at room temperature, V_{BE} is about 800mV, and the switching threshold is nominally at 1.6V; the static transfer range uncertainty of about 100mV gives a nominal threshold for solid Lows and Highs of about 1.55V and 1.65V respectively. The FAST threshold voltage was chosen higher than other TTL families to give a larger noise margin with respect to ground, and to be more nearly centered in the region where a FAST output driver stage switches with maximum edge rates, which occurs between about 0.6V and 2.6V.

INPUT VOLTAGE RANGE	INPUT CURRENT		
	Diode	PNP	NPN
Below Ground	Schottky Clamp	Schottky Clamp	Schottky Clamp
Ground to V_T	High (to 600μA)	Low (to 20μA)	Leakage
V_T to V_{CC}	Leakage	Leakage	Low (to 20μA)
Above V_{CC}	Leakage	Leakage	Clamp 100 to 1000μA

Figure 8. Input Current for Input Voltage Ranges

Because the FAST threshold is set by the base-emitter junction voltage, it is dependent on junction temperature and current density. V_{BE} increases by about 1.2mV for each degree C drop in junction temperature; current density changes by about a decade for a 60mV change in V_{BE}. The total variation due to processing differences, temperature, and current density is about 150mV per junction, or 300mV total change in input threshold to give limits of 1.25V Low and 1.95V High. The FAST V_{IL} and V_{IH} limits are 0.8V and 2.0V respectively, a tight spec for V_{IH}.

HYSTERESIS CONSIDERATIONS

Hysteresis has frequently been added to the inputs of TTL circuits in the past. The purpose is to increase noise immunity, which is accomplished by adjusting threshold voltages in a direction to reinforce an input level once a critical value has been reached. The procedure works well for slow circuits where the likelihood of slow, noisy inputs is high. It does not accomplish what is intended for FAST parts. There are several reasons: FAST threshold is already high and well centered so noise problems are automatically minimized. Inductive ground bounce, which is discussed at length later, causes problems with fast edge rates that completely swamp the typical benefits of hysteresis. It thus becomes a further complication in an already complicated picture and is more apt to hurt noise margin than to help it. Because of this, the two major supplies of FAST have eliminated hysteresis from all circuits except those specifically designed as Schmidt triggers; the 'F13, 'F14, and 'F132.

ELECTRO-STATIC DISCHARGE (ESD) CONSIDERATIONS

It is universally true that no bipolar integrated circuit process can provide devices with such high breakdown voltages that they are able to withstand ESD without some structure punching through or breaking down. The necessary condition for survival when this occurs is that the energy dissipation in any volume of the chip must be kept low enough so that neither the silicon nor the interconnecting metal can melt. This can be accomplished in two ways: the breakdown voltage should be as low as practical, consistent with normal circuit operation, and the energy should be dissipated in as large a volume as is possible. Circuit components that are particularly sensitive to charge damage must be protected by structures that are less fragile. All Signetics FAST parts are designed with these requirements in mind, and although, as a rule of thumb, a sophisticated oxide isolated process used to fabricate these parts tends to be more ESD damage-prone than a junction isolated process, FAST is about as rugged as other TTL families in general. If FAST parts are handled with the same care afforded any other high-technology parts, they will not be damaged.

ESD sources usually fit into one of two categories: people or other objects that have accumulated static charge and touch the parts; or, they generate their own charge, as is the case when a circuit makes sliding contact with an insulator. In the first instance, static voltages tend to be high, over 10000V, and discharge is usually limited by relatively high series resistance. In the second case, voltages are lower, around 200V, but there is very little series resistance to limit discharge current. Both possibilities are simulated with discharge models that are used in the majority of the test setups, and parts are designed in a way to improve survival for both ESD conditions.

Circuit Characteristics

Experience has shown that inputs of TTL circuits are much more likely to suffer ESD damage than outputs. Since negative voltages are discharged through clamp ground diodes with low chip dissipation, only voltages positive with respect to substrate ground are apt to produce input damage.

Circuits with diode inputs have a positive voltage breakdown in the relatively high range of from 15V to 25V. Schottky diodes connected to an input pin usually break down before junction diodes, and if they are stressed beyond their limits the Schottky diodes usually sustain damage in the corners. A diffusion guard-ring around the diode increases the uniformity of the breakdown, and as a result maximizes the dissipation volume at breakdown and increases the ability of the device to survive ESD. All Signetics FAST circuits have guard-rings on Schottky diodes that connect to input or output pins.

NPN inputs are designed to have low holdoff voltage for positive voltages in excess of V_{CC}. Under static discharge the input structure forward biases, and the current-source transistor conducts the ESD current to substrate with a relatively low collector-emitter reach-through voltage. The input current for normal operation is low enough that a series limiting resistor can be added; this limits ESD current, especially for the case where the ESD source has no appreciable series resistance itself.

As processes improve, it is often possible to improve ESD protection. Most new releases and many parts that have been recently redesigned onto new processes have specific ESD structures included which protect up to 2000V for the standard resistance limited case — the human body model.

FLOATING INPUTS

FAST inputs should not be allowed to float. All unused inputs, even those on unused gates, should be tied to a voltage source of relatively low impedance that will get them out of the logic picture and out of trouble. For a Low input this can be ground, or the output of a permanently low driver. For a High input this can be V_{CC}, protected by a series resistor if circuit damaging voltage spikes are possible in the system, or a permanently high driver.

Properly tied High or Low inputs will not pick up enough spurious noise to cause problems. If they are allowed to float, the results can be disastrous. Floating diode inputs usually pull to within a few Mv of $3V_{BE}$ above ground, a V_{BE} above threshold. The input voltage will fall about 1V per 0.1mA of current that is capacitively coupled from an adjacent Low-going pin. Since pin-to-pin input capacitance is in the order of one pF for an IC in a PC environment, an adjacent pin falling at 1.0V/ns couples in about 1.0mA of current, enough to switch the input to a Low state for as long as the current lasts. The normal FAST circuit response will be to switch or oscillate. The problem is even worse for high-impedance low-capacitance NPN or PNP inputs. In this case the static voltage to which they float is determined in part by leakage, and is not predictable.

To reiterate, FAST inputs must not be allowed to float. To do so is to invite serious system problems.

OUTPUT CONSIDERATIONS

The purpose of the output stage is to supply current to a load to force it to a High state or to sink current from the load to force it to a Low state. The speed at which the load can be switched from one state to the other depends on how much supply current or sink current is available from the output driver. There must be an amount in excess of that which is required to maintain the static load voltage, and it is the excess current that is available to charge or discharge the load capacitance. Most FAST circuits are designed to fit into one of those categories, based on output drive capability; the normal output stage, the buffer driver which can supply approximately twice as much current, and the high current drivers designed to drive low-impedance terminations.

Both normal drivers and buffers may be 3-State, which means that, in addition to Low and High states, they can be forced to a high-impedance OFF state as a third possible choice. This allows multiple components to be connected to a bus simultaneously, with only the single-selected device providing actual drive capability.

The basic components of an output stage are shown in Figure 9.

The pull-down driver components sink load currents to force a Low state at the output pin; the pull-up driver components supply current to force a High state. The control components turn on the selected driver and turn off the nonselected driver in response to the logic input signal. For 3-State parts, the control components turn off both drivers if the 3-State control signal is active. The output Schottky clamp is included to suppress inductive undershoots, and is a part of every FAST circuit. The load requires a static current to keep it in either a logic High or Low state. The drivers must also charge and discharge the load capacitance C_L, which is generally one of the major factors that influence switching speed.

Since, to a large extent, they function independently of each other, the pull-up driver, pull-down driver, and control blocks are discussed independently.

PULL-UP DRIVERS

Open-Collector

The simplest pull-up driver consists of no more than a fixed pull-up resistor tied to V_{CC}. For this case, the control stage interacts only with the pull-down driver. In the Low state, this must sink the current from both the pull-up resistor and load. In the High state, the pull-up resistor must supply all of the load current. Most often, the pull-up resistor is not physically part of the integrated circuit chip itself, but is added externally. In this case the only circuit element connected to the output pad (in addition to the ever-present Schottky clamp) is the collector of the pull-down driver transistor, hence the name "Open-Collector." Parts with this output stage can be tied together for bus applications. If any of the connected pull-down stages is active, it will pull the bus Low; only if all of them are off can the external resistor pull the bus High. This action provides a "wired" logical function that is free in the sense that no additional components are required to achieve it. Some Open-Collector FAST parts also have 3-State inputs that serve to disable output pull-down stages regardless of the action of the normal logic function.

The Open-Collector output voltage depends on the load, the value of the pull-up resistor, and the voltage to which this is connected. If the resistor value is low, the output will rise to nearly the full value of the pull-up source voltage; in particular, the Open-Collector output can rise to V_{CC}, a voltage higher than that obtainable with a standard Darlington totem-pole pull-up.

High-drive Open-Collector parts are ideal as drivers for terminated transmission lines. In this application the line is terminated at the receiving end with a resistor network that provides the proper impedance and an equivalent source voltage of about 3V. The circuit pull-down drive sinks the termination current through the line at relatively low chip power dissipation when it is on. When it is turned off, the line pulls the output high, charging the stray capacitance from an impedance equal to the line characteristic impedance. Since the current is supplied by the line, the chip power dissipation falls. Very fast rise times approaching 1ns can be obtained with this scheme. Rise times, in general, for open-collector outputs are determined by the RC product of the pull-up resistor and the stray capacitance, and are limited only by the ability of the chip to pull the load low.

Signetics has a new family of parts designed specifically for driving heavy loads in termi-

Circuit Characteristics

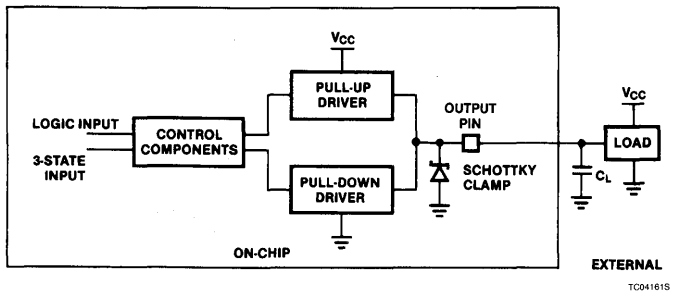


Figure 9. Output Stage Basic Components

nated or unterminated environments. The majority of these are Open-Collector functions. They are discussed in detail later.

Standard Darlington

Most FAST pull-up drivers use dual transistors, connected as shown in Figure 10, with the emitter of the first device Q_b delivering current to the base of the driver Q_a. This configuration is called a Darlington circuit and provides a composite current gain nearly as large as the product of the current gains of Q_b and Q_a.

The major advantage of the Darlington pull-up, as compared to the Open-Collector, is that the pin is actively pulled high by the emitter-follower action of Q_a which is capable of supplying large currents to quickly charge output capacitance. Despite the large output current that is available, the drive requirements of Q_b are low, so that the voltage drop across R_c is small, and the pad will pull up to a voltage nearly as high as $V_{CC} - 2V_{BE}$.

For the case where the output pin voltage is High, the phase-splitter transistor Q_c is off, and the base of Q_b is pulled high by resistor R_c. The current which flows through R_c is just sufficient to provide base drive to Q_b. The base voltage of Q_b will be just slightly below V_{CC}, and the output pin voltage will be less

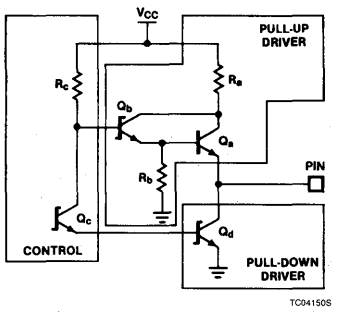


Figure 10. Basic Darlington Pull-Up

than this by the sum of the V_{BE} drops of Q_b and Q_a, both of which are on. Most of the base current for Q_a and the current through pull-down resistor R_b is supplied from V_{CC} through R_a and Q_b. Q_b has a Schottky clamp to prevent saturation when the current through R_a is large. Resistor R_a limits the amount of current flowing from V_{CC} through Q_a to a value small enough that Q_a will not be damaged if the output pin is accidentally grounded for a short period of time. This short circuit output current is called I_{OS}, and its value is approximately the maximum current available to charge the output capacitance at the beginning of a Low-to-High transition. The minimum current available when the pin has reached the minimum guaranteed high voltage V_{OH} is called output high current (I_{OH}), and is specified to be either 1mA or 3mA, depending on the type of driver. The maximum output voltage that the pull-up driver can achieve occurs at maximum V_{CC}, and at high temperatures with corresponding low values of transistor V_{BE} and high current gain. Conversely, the minimum high voltage occurs at low V_{CC} and low temperatures.

In the Low state, the pull-down driver Q_d is on and the pin voltage is the Q_d saturation voltage V_{SAT}. Q_c is on and its collector resistor R_c is pulled down to $V_{BE} + V_{SAT}$; the V_{BE} of Q_d, V_{SAT} of Q_c. Q_b is also on, with its emitter at V_{SAT}, and the current through R_b is low. The base-emitter voltage of Q_a is nearly zero and Q_a is off.

The rate at which the pull-up driver can force a Low-to-High transition depends on a number of factors. The first, and obvious, consideration is that the control components must turn off the pull-down driver very quickly. During the short time that both pull-up and pull-down are on, there is a large feed-through current spike that is wasted as far as switching the load is concerned; it also increases chip power dissipation and produces undesirable voltage spikes in V_{CC} and ground. Assuming the pull-down is off, the Low-to-High transition speed is governed by: 1) the rate at which R_c can pull-up the base of Q_b; 2) the amount of pin current required to drive the load and charge the load capacitance; 3) the value of R_a; 4) the physical size and current gain of Q_a; and 5) the amount of Q_a base drive current that is lost through R_b to ground. The amount of R_b drive current lost can be reduced by connecting R_b to the output pin instead of ground, and this is done in a number of FAST parts. For this case, the static current through R_b with the pin high is less than if R_b is grounded, but switching feed-through current spike for a High-to-Low transition may be increased because R_b cannot effectively pull-down the base of Q_a until after the pin voltage falls.

The pin can be driven above its maximum high value by an external pull-up or by positive reflections from a transmission line. When this happens, Q_a and Q_b do not have sufficient base-emitter drive to keep them on. If the pin voltage rises significantly above V_{CC}, Q_a will begin to leak current into V_{CC}. For the case where R_b is tied to the pin instead of ground, the reverse transistor action of Q_a allows a high pin-to-V_{CC} current. This is not usually a problem in normal operation, but should be avoided in system applications where the V_{CC} pin may be intentionally grounded.

3-State

For all 3-State FAST parts, the leakage paths to a grounded V_{CC} pin are blocked with Schottky diodes. A typical 3-State pull-up is shown in Figure 11. S_a is the series Schottky blocking diode. 3-State Schottkys S_{t1} and S_{t2} serve to simultaneously turn off the pull-up and pull-down drivers. The 3-State control is active when it is pulled low to within V_{SAT} of ground. In this state it sinks all the available drive current for Q_b and Q_c, and pulls their bases down to ($V_{SAT} + V_{Schottky}$), which is essentially one V_{BE}. The voltage drop across R_c is large and 3-State power dissipation is typically high. Q_a and Q_b are off for normal TTL voltage ranges of the output pin; a negative undershoot large enough to drive the pin about one V_{BE} below ground will allow them to turn on and supply current from V_{CC}; this action aids the clamping Schottky diode in preventing the pin voltage from falling lower.

Circuit Characteristics

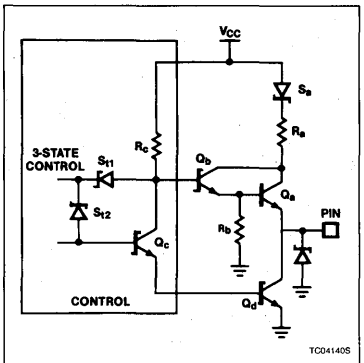


Figure 11. Basic 3-State Pull-Up

PULL-DOWN DRIVERS

The basic FAST pull-down driver is shown in Figure 12. Q_d is the pull-down driver transistor, a big Schottky-clamped device capable of sinking large currents. C_d is the stray base-collector capacitance of Q_d, and its unavoidable presence has an important effect on the performance of the pull-down driver. Q_c is the Schottky-clamped phase splitter. It functions as a current-limited, low-impedance driver for Q_d when the logic input voltage V_{IN} is high, and as an inverting driver for pull-up Q_b by virtue of the current through R_c when V_{IN} is low and Q_C is off. Z_d is the pull-down impedance network which insures that Q_d is off when V_{IN} is low.

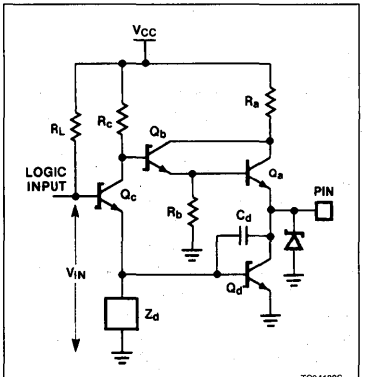


Figure 12. Basic FAST Pull-Down

Switching to the logic Low state occurs when V_{IN} is larger than the V_{BE} drops of Q_c plus Q_d, both of which are initially on. Part of the total emitter current available from Q_c comes from R_c, which has a voltage drop of $V_{CC} - V_{BE} - V_{SAT}$. The remainder of the Q_c emitter current is supplied through its base Schottky clamp or by other components not shown in Figure 12 but discussed in the section on control components. A portion of the total Q_c emitter current is lost in the pull-down network Z_d; the remainder is available as base current for pull-down driver Q_d. The amount of current Q_d can sink depends on its base drive, its current gain, and its collector voltage. This current is specified on a per-part basis in the data sheets at output low voltage (V_{OL}) of 0.5V. The current which Q_d can sink in the switching range with the pin voltage at 2.5V is called available current (I_{AVL}), and is usually at least 70mA for FAST. The manner in which this current varies as the pin voltage decreases from 2.5V to V_{OL} is not specified as a FAST family parameter, since it is critically dependent on circuit design for a particular part, but is included as a specification for selected parts, especially those tailored to drive transmission lines. Several innovative circuit improvements that increase I_{AVL} by increasing the drive current for Q_d are shown in Figures 19a and 19b. Speed-up Schottky diodes S_{s1} and S_{s2} have been added to the standard pull-down circuit as shown in Figure 13a. Both are reverse-biased and off in the High state, since R_c pulls the collector of Q_c nearly to V_{CC}. Both connect the collector of Q_c to nodes that need to be discharged during a High-to-Low transition. S_{s1} to the base of Q_a, S_{s2} to the pin. They will conduct if these node voltages are higher than $V_{BE} + V_{SAT} + V_{Schottky}$, or approximately $2V_{BE}$; they are quite effective above $2V_{BE}$. Other networks are available which function down to lower voltages; these are especially useful for transmission line drivers. Figure 13b shows a dynamic kicker that gives an impulse of current which is especially useful in discharging high capacitive loads.

The network of elements labeled Z_d in Figure 12 is the pull-down impedance which insures that Q_d is off when the value of V_{IN} falls below $2V_{BE}$. When the voltage at the base of Q_d is being pulled high by Q_c or low by Z_d, the output pin voltage responds by moving in the opposite direction. This produces a change in voltage across C_d, which is the sum of the base voltage change and the collector voltage change, so the amount of charge required by C_d is magnified by a factor which is larger than unity.

This well-known Miller-effect causes the apparent value of C_d, as perceived by the drivers, to be a factor of about five times larger than the already large physical junction capacitance, all of which means that the drivers Q_c and Z_d need to supply or sink much more current during an output transition than is necessary to maintain static conditions. When static conditions do exist internally in the circuit, noise voltage spikes on the output pin, V_{CC}, or ground can momentarily force the base of Q_d in the direction to produce a serious output glitch, and the drivers must respond quickly to counter this coupled noise.

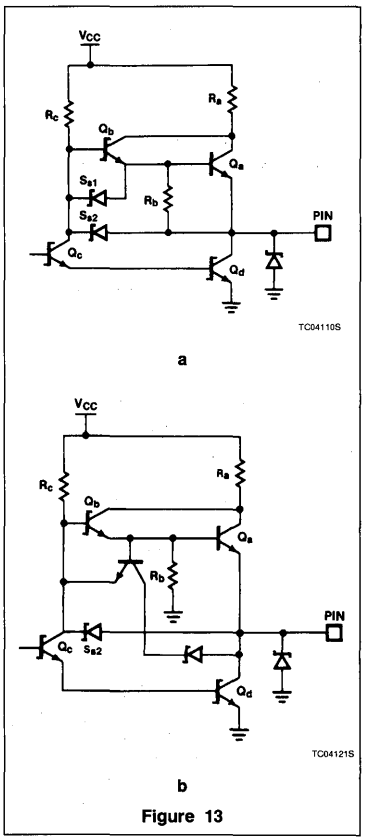


Figure 13

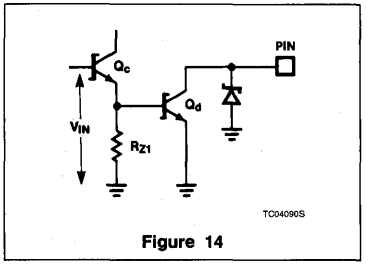


Figure 14

The simplest Z_d element is a resistor R_{Z1} tied to ground, as shown in Figure 14. It will pull the base of Q_d all the way down to 0V if V_{IN} is less than one V_{BE}. This provides good immunity to coupled noise, but slows down the High-to-Low pad transition somewhat because the base of Q_d must rise a full V_{BE} before the output can begin to change. The value of R_{Z1} needs to be relatively large to prevent a serious loss of base drive current when Q_d is on, which makes it easier to

Circuit Characteristics

capacitively couple voltage spikes to the base of Q_d and, in part, nullifies the good noise immunity the full V_{BE} swing provides.

The addition of a series Schottky diode solves most of the problems. This is shown in Figure 15. The Q_d base voltage cannot pull below a Schottky drop, so the switching speed is unimpaired. The value of R_{Z2} can be less than R_{Z1} for the same current when the base is high, so the effect of coupled charge is less and the noise margin is acceptable.

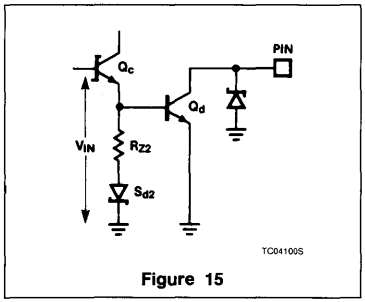


Figure 15

The circuit of Figure 16 is standard with many TTL families. It pulls the base of Q_d down even less than does $R_{Z2} - S_{d2}$, but it has a relatively high dynamic impedance and is somewhat noise sensitive. It has the advantage that it tends to "square up" the input voltage-to-output voltage transfer function, hence its popular name "squaring circuit." It is frequently used in simple gates where the shape of the transfer function may be important. For more complicated circuits, where there are one or more stages of logic with gain between input and output pins, the squaring ability is pretty much lost; in fact, it is likely that high-gain, multiple-logic-level FAST circuits will oscillate if the input voltage is held at near threshold for any length of time.

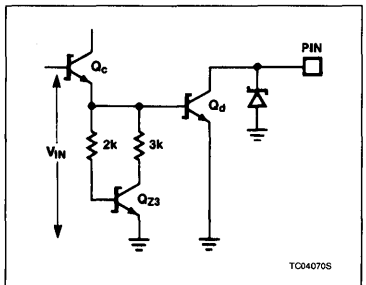


Figure 16

Figure 17 shows a popular dynamic circuit that is used in conjunction with a resistor or squaring circuit pull-down, and which insures that C_d cannot couple enough charge to the base of Q_d to slow down a Low-to-High transition. In operation, as the emitter of Q_b rises, charge is coupled through C_{Z4} into the base of Q_{Z4} which turns on and shunts the Miller current flowing through C_d to ground. When the transition is finished, the current through C_{Z4} stops and Q_{Z4} turns off. When the High-to-Low transition of Q_b occurs, C_{Z4} discharges through S_{d4}. Because Q_{Z4} reduces the problems associated with Miller current, the circuit is called a "Miller Killer."

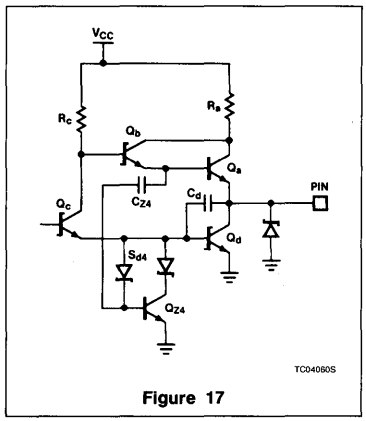


Figure 17

Figure 18 shows an active pull-down for the base of Q_d. The drive for Q_{Z5} (not shown) must be generated from the same signal that drives the base of Q_c. When Q_c is on, Q_{Z5} must be off, and when Q_c is off, Q_{Z5} turns on to hold the base of Q_d low. The impedance is very low, eliminating the capacitive-coupling noise problem.

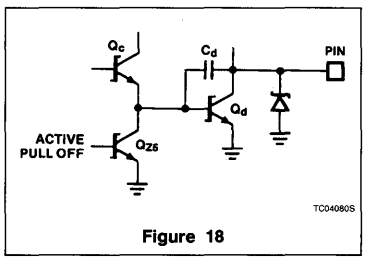


Figure 18

CONTROL COMPONENTS

This section covers 3-State control drivers, special 3-State problems, and V_{CC} turn-on current and 3-State glitches during power-up.

3-State Control Drivers

The normal TTL 3-State scheme is shown in Figure 11. The 3-State control voltage in the OFF state is high enough that S_{t1} and S_{t2} are reverse-biased; in the active state the control voltage is low, usually V_{sat}, so that the $Q_a - Q_b$ base emitter stack is off, as is the $Q_c - Q_d$ stack. In the 3-State mode, R_c is dissipating maximum power. Blocking Schottky diode S_a prevents current from flowing backwards through Q_a if the V_{CC} pin is grounded; the output pin high voltage can be about 4.5V before there is any significant 3-State leakage current. The only exception to this general rule with FAST is for the diode input transceiver function, where the same pin acts as an input or an output. In this case, the pin supplies one or more normal FAST unit loads of current if it is Low, and tends to pull to $2V_{BE}$ if it is floating. NPN and PNP input transceivers have normal low 3-State leakage.

There are several innovative improvements to the basic 3-State circuit, as shown in Figure 19. The addition of inverter $Q_{c2} - R_{c2}$ with a blocking Schottky S_{c2} allows the addition of feedback diodes S_{s1} and S_{s2} to increase I_{AVL}; S_{c2} cannot be included in series with R_{c1} because its forward voltage drop would lower V_{OH}. 3-State power is not increased, since only one R_{c1} is pulled low. The current through Q_{c2} is available as added base drive to Q_d, so nothing is wasted. An additional transistor may be paralleled with Q_{c1} and Q_{c2} to control an active pull-down version of impedance Z_d which, discussed in a previous section, eliminates the Miller turn-on problem of Q_d.

I_{CC} Considerations

There is no formal family specification that limits the amount of V_{CC} current a FAST circuit may draw during turn-on as V_{CC} rises from zero to 4.5V. However, for most new designs, and especially for circuits that have high I_{CC} requirements, an effort has been made to limit maximum turn-on I_{CC} to 110% of I_{CCmax}. This precaution prevents an undesirable system situation where the V_{CC} power supply is large enough to drive the devices, but can't power them up. The major component of turn-on current is V_{CC} to ground feedthrough of output stages. Unless specific steps are taken to prevent it, the pull-up Darlington turns on if V_{CC} is greater than $2V_{BE}$, and remains on until the on-chip voltage is high enough to set the phase splitter solidly in one or the other of its two states. The solution is to incorporate extra circuit components that will set the phase splitter at voltages nearly as low as $2V_{BE}$, or turn off the top device with a separate 3-State type structure which activates at low V_{CC} voltages and becomes inoperative when V_{CC} is high.

The amount of current that can be fed from an output pin back into a grounded V_{CC} pin, or through the chip to ground for an open V_{CC} pin, depends on the design. Generally, 3-State feedback current is specifically limited to low values which are leakage or breakdown related. Other parts have medium to high current. Those with Darlington pull-downs connected to the output pin conduct the most.

Some 3-State parts, especially selected buffer functions, have additional circuit elements

Circuit Characteristics

to insure that as they power on they source or sink no appreciable output current, provided that the 3-State control pins are in the active state as V_{CC} rises. This means that V_{CC} can be turned on or off at will in the system to conserve power, and bus voltages will not be affected. Parts with this capability are identified in the specific data sheets.

GROUND VOLTAGE AND OTHER NOISE PROBLEMS

Ground Voltage As A Serious Problem

Excessive ground noise voltage in a system usually produces serious degradation of switching speed. It may also produce unwanted glitches on outputs, or spurious clocks which cause flip-flops to lose data, or relaxation oscillations that completely disrupt a system. It is, without doubt, one of the major causes of logic systems failure ... difficult to accommodate, and difficult to eliminate.

The problem is not unique with FAST, but is greatly aggravated by the high transition rates and large currents for which FAST is designed. Because of this, FAST can optimally replace other TTL families only in systems that have been carefully designed at the PC board level. Well planned layout is vital, and multilayer boards with ground and V_{CC} planes are often necessary. Great care must be taken to insure adequate bypassing for V_{CC}. The problems are not trivial, but they can be solved satisfactorily to yield systems whose performance is not exceeded in the TTL world.

Sources Of Ground Noise

Ground lead inductance is the source of most ground noise voltage; it causes a voltage drop proportional to the rate at which the current through it changes.

Inductance is a measure of the amount of energy stored in the magnetic field associated with a current. Low values of inductance imply low energy, which means low voltage required to affect a change in current. As a general rule, inductance decreases as current is allowed to spread out in space, and current interactions decrease. The inductance of a thin wire far removed from the return current path is high; that of a large conductor coaxially encircled by the return path is low. Inductance tends to increase faster than linearly with conductor length, but only approximately logarithmically with decreasing cross-section dimensions. From a logic system viewpoint, ground planes are better than ground traces; wide lines are better than narrow lines; close spacing to planes is good; loops that allow magnetic flux linkages are bad; wire lengths of fractions of inches count; and sockets with long pins add significant inductance to a PC card.

Ground noise voltage is increased by feed-through current spikes. These occur when both top and bottom devices of the output totem-pole driver are on simultaneously, and heavy currents are allowed to flow directly from V_{CC} to ground. They can be minimized in one of two ways: drive the devices such that one is turned off before the other can turn on, or more commonly, drive them together, but very fast, so the feed-through current can flow for only a short time.

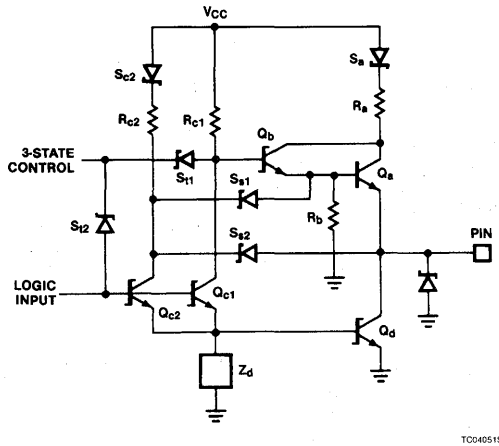


Figure 19. Improved 3-State Circuit

Although most ground noise results from ground inductance, resistance also contributes. Static ground offsets unrelated to rates of current change occur, and add to the total ground voltage. Generally speaking, those measures which reduce ground inductance also reduce ground resistance.

Estimating The Magnitude Of Ground Noise

The accurate modeling of ground noise-related problems in logic design is a complex procedure that requires numerical analysis to determine system currents and voltages as a function of time. This can only be accomplished in a satisfactory manner if one has reasonable electrical models, especially for input stages and output drivers of the integrated circuits used in the system. These data are available on request for many of the FAST logic functions. Signetics is prepared to assist customers in solving the sometimes formidable problems associated with large system simulation.

The following discussion derives the minimum peak-value of ground noise that will occur as an integrated circuit discharges a capacitor through ground lead inductance. It points out the minimum problems that will exist. In the real world, the peak ground voltage will always be larger than the simple derivation predicts.

The load capacitor C and its discharge path are shown in Figure 20. The capacitor has been previously charged to a positive voltage, and is discharging through pull-down transistor Q_d and lead ground inductance L_g. As the current changes, it develops a ground voltage V_g across L_g that is equal to the product of L_g times the rate at which it changes.

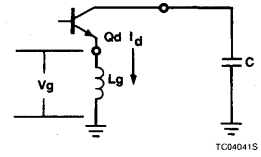


Figure 20

The discharge current I_d will vary with time; starting from zero, it will increase to a maximum value, and then eventually return to zero. There are an infinite number of ways I_d can vary, depending on how the transistor allows charge to flow at any instant in time, but each of the possible current-vs-time discharge curves must define the same area, equal in value to the total charge Q that is removed from the capacitor as its voltage falls by an amount V.

The voltage drop V_g across the inductor at any instant in time will be determined by the

Circuit Characteristics

slope of the current-vs-time curve, that is, by the rate at which current is changing. The unique curve that has the required area and minimum slope is triangular, as shown in Figure 21. The ground voltage for this case is a square wave as shown in Figure 22. It will be positive while the current is increasing, and negative when the current is decreasing.

The equations of interest in estimating V_g are:

$$\text{Charge} = Q = CV = I_{MAX}\frac{T}{2} = \text{triangle area}$$

$$\text{Ground voltage} = V_g = (\text{triangle slope})(L)$$

$$= \frac{2\ I_{MAX}\ L}{T}$$

Combining the two equations to eliminate I_{MAX} gives:

$$V_g = \frac{4CVL}{T^2}$$

This lower limit of peak ground voltage will always be exceeded in the real world, where ground voltages are usually spikes, not square waves. If a spike is large enough and long enough, the chip will erroneously recognize it as a valid input, and respond either by glitching, slowing down, clocking incorrectly, or oscillating.

An example using values typical for a FAST circuit in a 16-pin DIP illustrates the potential for trouble. If the circuit discharges one standard FAST load of 50pF in 2ns with a voltage change of 3V through a ground inductance of 10nH, the minimum ground voltage will be:

$$V_g = \frac{4 \times 50 \times 10^{-12} \times 3 \times 10 \times 10^{-9}}{(2 \times 10^{-9})^2}$$

$$= 1.5V$$

This value is high, and suggests that if transition times are not to be seriously degraded, inductances must be kept as small as possible, and loads must be minimized.

Effects Of Ground Noise On Input Stages

FAST TTL input voltages are referenced to system ground as illustrated in Figure 23 which shows an equivalent input and output stage. The equivalent input circuit is represented by R_{IN} and the four diodes D1 through D4. These components establish an input switching threshold voltage of 2 V_{BE} relative to chip ground. The on-chip voltage V_{IN} must be different from this value by a margin large enough to guarantee a static Low or High with sufficient overdrive to insure switching speed. The on-chip voltage V_{IN} that is actually available is the difference between the input pin voltage V_{PIN} and the total ground voltage noise V_g. V_g is the sum of the steady state voltage due to ground current flowing through R_g, and the inductive voltage drop across L_g. The inductive voltage is usually the larger of the two, and since it depends on current changes, it will have both positive and negative polarities for each switching cycle. This means that either Low or High input voltages which are too close to switching threshold will allow the noise margin to be exceeded, and if the ground voltage noise persists long enough, the input will switch erroneously. The result of this depends on the chip function. Combinatorial logic usually slows down or produces output glitches. Latches and flip-flops may be clocked inadvertently, and stored data will be lost. Complex circuits that have multiple outputs may oscillate, particularly if one polarity of ground noise results in a rapid change of ground current that produces the opposite polarity ground noise.

Ground noise adds a dimension of difficulty in measuring input threshold voltage. FAST parts are guaranteed to have input thresholds between the limits 0.8V and 2.0V. A typical method of verifying this is to determine the voltage at which the input actually switches. This requires some care, since the true threshold voltage is masked by any noise voltage contributed by the test system or ground inductance. For accurate results, the input pin voltage should approach the switching threshold slowly and smoothly. At threshold the input will switch. Sensing this point is easy for those circuits where an output also switches, glitches, or oscillates. It is much harder to sense this point for those circuits where an input change produces no output change, for example, with flip-flops which change state only when clocked. The input switch point for these devices can be inferred by measuring the input current as a function of input voltage. Clocking the part may produce enough ground noise to distort the measurement, even if the output doesn't switch.

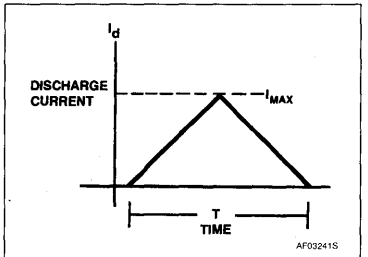


Figure 21

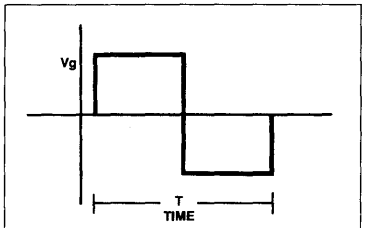


Figure 22

Effects Of Ground Noise On Output Stages

The most obvious effect that ground noise has on output stages is to directly change the voltage available to force discharge current through the pull-down device. If the only source of ground voltage is from the particular output of interest, the ground and output pin inductances will always slow down a High-to-Low transition. They produce a voltage in opposition to the output pin voltage at the

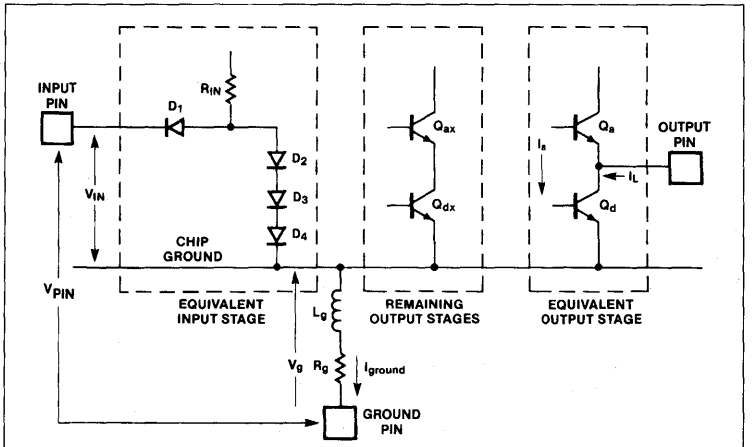


Figure 23. Equivalent Input and Output Stage

Circuit Characteristics

beginning of the discharge when currents tend to be high and voltage changes rapidly. As discharge continues, the available drive decreases, and currents increase less rapidly. Eventually the current begins to fall, and the ground voltage reverses polarity, which tends to limit the rate at which the current decreases. If currents have been high, and the inductances are large, there may be substantial undershoot at the end of the switching cycle which can drive the output pin below ground.

If multiple outputs are switching simultaneously, the total ground noise needs to be considered to determine the result for a particular output. For this case, it can happen that ground noise will, in fact, speed up an output; on the other hand, it may introduce delays that are much larger than those possible with single output switching. This behavior makes it difficult to predict, except on a case by case basis, what the actual effects of multiple output switching will be. Curves of delay vs multiple switching have been published, but these serve only as rough guides to indicate potential problems, and need to be backed up with actual analysis for any particular application.

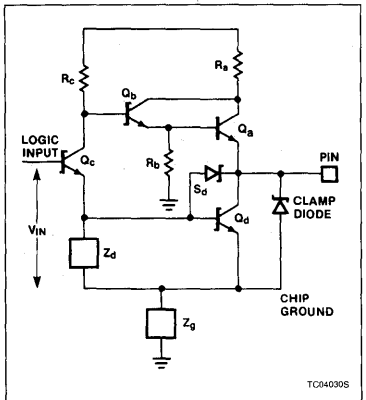


Figure 24

In addition to the direct influence on discharge voltage, excessive ground noise can affect the operation of the control components, and alter both rise and fall times by driving pull-up or pull-down stages incorrectly. One example of this can be understood with reference to Figure 24. The scenario is that the output pin is Low, but on the verge of switching High, with V_{IN} falling and Q_c ready to turn off. A problem occurs if, at the instant before the pull-up transistor Q_a turns on to pull the output pin high, the voltage from output pin to chip ground falls. This can happen as a result of inductive undershoot driving the output pin down, or by a rise in ground voltage caused by currents completely unrelated to the output of interest. The low output-pin-to-chip-ground voltage pulls down the emitter of Q_c through Schottky clamp diode S_d, and if V_{IN} is not low enough to counteract this, Q_c will not turn off. The net result is that R_c cannot rise, and the transition is delayed until the noise voltage from output to ground disappears.

V_{CC} Noise As An Additional Problem

Inductance in the V_{CC} lead produces noise in the on-chip V_{CC} voltage that is entirely analogous to ground voltage. The effects of V_{CC} noise can be nearly as harmful as those produced by ground noise, the only significant difference being the fact that TTL input voltages are referenced to ground instead of V_{CC}.

The first symptom of excessive V_{CC} inductive voltage drop is a change in the edge rate for a Low-to-High transition. This will decrease if the on-chip V_{CC} falls, and increase if it rises. If the ground to V_{CC} voltage falls below a minimum value, internal circuit delays or glitches can occur, and functions with flip-flops or other storage elements may lose data. As is the case with excessive ground noise, FAST circuits may break into relaxation oscillation.

Because V_{CC} to ground voltage must remain above a minimum value to avoid logic errors and glitches, it is absolutely vital that V_{CC} to ground bypassing is adequate. This requires low inductance V_{CC} and ground PC traces, and low inductance bypass capacitors. FAST parts are guaranteed to function properly for low V_{CC} of 4.5V. This means that pin voltages must not fall below this value for any appreciable time: fractions of nanoseconds. V_{CC} system voltage should be close to the maximum guaranteed value for safe system design.

Designing To Reduce The Effects Of Ground Noise

The typical 1.5V minimum value for ground noise, calculated in the preceeding example, points out the possibility of noise-related problems when only one standard 50pF load is being driven by an output stage. Simultaneous switching of more than one such load obviously increases the risk of trouble, and raises the question of how an octal part can work at all. Fortunately, the real world, with careful PC layout, is not usually so grim.

The standard 50pF load is a lot of capacitance, chosen so one can estimate the chip response for a single output switching under conditions that approach worst case. On a modern PC board a wire trace that has 50pF stray capacitance is several feet long and looks like a resistive delay line instead of a lumped capacitor.

Traces on a PC card must be short to behave like lumped capacitance for an output stage. For this case, a major contributor to driver current is the load presented by the input stages of the driven circuits, and the associated stray capacitance. As previously mentioned, the input current for FAST parts is related to edge rates, and is generally larger than the measured static value of input capacitance would predict. Because of this, the useful fan-out of FAST circuits may be more dependent on ground noise of drivers with heavy capacitive loads than on the amount of current available to a static DC load, which is the guaranteed data sheet value.

Most of Signetics' FAST parts are available in surface mount packages, and these have lower ground inductance than the standard DIP parts.

Inductance of output signal pins reduces the rate at which associated ground current can change, and this reduces ground noise voltage without a corresponding reduction of static output voltage. This inductance may be intentionally increased by adding trace length on the PC board; one needs to be careful, and anticipate the increase in output ringing during switching transitions.

In summary, there are many potential problems that one can anticipate in logic systems with fast edge rates. Some of these are dependent on the available components and their respective packages, and the system designer must be certain that the demands made of them are not more than they can handle. A second major consideration is the system layout, especially from the standpoint of ground, V_{CC}, and signal lead inductance. If one is careful with PC design and layout, and chooses components wisely, FAST systems deliver performance second to none in the TTL world.

Heavy Current Drivers

Signetics has a new family of parts defined that are capable of driving currents much larger than those achieved with standard FAST parts.
The parts presently available are:

F3037	Quad 2 – Input NAND
F3038	Quad 2 – Input NAND Open-Collector
F3040	Dual 4 – Input NAND
F30240	Octal Line Driver, Open-Collector
F30244	Octal Line Driver, Open-Collector
F30245	Octal Transceiver, Open-Collector
F30640	Octal Transceiver, Open-Collector

Others are in the planning stage.

Circuit Characteristics

The drivers are husky enough to assure incident wave-switching driving transmission lines with impedance levels as low as 30Ω. They are the best choice available for applications that need the ultimate in speed and drive capability.

All the parts use multiple center ground and V_{CC} pins. Special precautions have been taken to insure minimum feed-through current during switching, and this, coupled with the low V_{CC} and ground inductance, results in minimum V_{CC} and ground noise, and allows maximum edge-rate and speed.

The parts are available on several different packages, including ceramic. Because the power dissipation is application dependent, the user needs to choose a package and an environment carefully to be sure the maximum temperature ratings are not exceeded. These maximum ratings are part of the individual data sheets.

Signetics

Section 4
FAST User's Guide

FAST Products

INDEX

Signetics

FAST Products

Data Sheet Specification Guide

INTRODUCTION

Signetics FAST data sheets have been configured for quick usability.

They are self contained and should require minimum reference to other sections for amplifying information.

All references to military products have been deleted from this manual, specifically to reflect recent government requirements imposed via Revision C of MIL-STD-883, including the general provisions of Paragraph 1.2. Specifications for military-grade FAST products are included in the Military Products Data Manual available from the nearest Signetics Sales Office or Sales Representative.

TYPICAL PROPAGATION DELAY AND SUPPLY CURRENT

The typical propagation delays listed at the top of the data sheets are the average between t_{PLH} and t_{PHL} for the most significant data path through the part.

In the case of clocked product, this is sometimes the maximum frequency of operation. In any event, this number is under the operating conditions of V_{CC} = 5.0V and T_A = 25 °C.

The typical I_{CC} currrent shown in that same specification block is the average current (in the case of gates, this will be the average of the I_{CCH} and I_{CCL} currents) at V_{CC} = 5.0V and T_A = 25°C. It represents the total current through the package, not the current through the individual functions.

LOGIC SYMBOLS

There are two types of logic symbols. The conventional one, "Logic Symbol", explicitly shows the internal logic (except for complex logic). The other is "Logic Symbol (IEEE/IEC)" as developed by the IEC and IEEE. The International Electrotechnical Commission (IEC) has developed a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without explicitly showing the internal logic. Internationally, Working Group 2 of IEC Technical Committee TC-3 is preparing a new document (Publication17-12) that will consolidate the original work started in the mid-1960's and published in 1972 (Publication117-15), and the amendments and supplements that have followed. Similarly, for the U.S.A., IEEE Committee SCC 11 has revised the publication IEEE Std 91/ANSI Y32. 14-1973.

The updated version IEEE Standard Graphic Symbols for Logic Functions ANSI/IEEE Std 91-1984 (Revision of ANSI/IEEE Std-1973 (ANSI Y32. 14-1973] can be ordered through:

IEEE Service Center
445 Hoes Lane
Piscataway, New Jersey
Phone (201) 981-0060

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings table carries the maximum limits to which the part can be subjected without damaging it. There is no implication that the part will function at these extreme conditions. Thus, specifications such as the most negative voltage that may be applied to the outputs only guarantees that if less than -0.5V is applied to the output pin, after the voltage is removed, the part will not have been shorted.

Input and output voltage specifications in this table reflect the device breakdown voltages in the positive direction (+7.0V) and the effect of the clamping diodes in the negative direction (-0.5V).

Absolute Maximum Ratings imply that any transient voltages, currents, and temperatures will not exceed the maximum ratings. Absolute Maximum Ratings are shown in Table 1.

RECOMMENDED OPERATING CONDITIONS

The Recommended Operating Conditions table has dual purposes. It sets environmental conditions (operating free-air temperature), and it sets the conditions under which the limits set forth in the DC Electrical Characteristics table and AC Electrical Characteristics table will be met. Another way of looking at this table is to think of it not as a set of limits guaranteed by Signetics, but as the conditions Signetics uses to test the parts and guarantee that they will then meet the limits set forth in DC and AC Electrical Characteristics tables.

Some care must be used in interpreting the numbers in these tables. Signetics feels strongly that the specifications set forth in a data sheet should reflect as

Table 1

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Cuurent applied to output in Low output state	Standard outputs	40	mA
		3-state outputs	48	mA
		All buffer outputs	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

accurately as possible the operation of the part in an actual system. In particular, the input threshold values of V_{IH} and V_{IL} can be tested by the user with parametric test equipment. If V_{IH} and V_{IL} are applied to the inputs, the outputs will be at the voltage guaranteed by DC Electrical Characteristics table. There is a tendency on the part of some users to use V_{IH} and V_{IL} as conditions applied to the inputs to test the part for functionallity in a "truth table exerciser" mode. This frequently causes problems because of the noise present at the test head of automated test equipment. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, on the order of milliseconds, and any noise present at the inputs has settled out before the outputs are measured. But in functionality testing, the outputs are examined much faster, before the noise on the inputs has settled out and the part has assumed its final and correct output state. Thus, V_{IH} and V_{IL} should never be used in testing the functionality of any FAST part type. For these types of tests, input voltages of +4.5V and 0.0V should be used for the High and Low states, respectively.

In no way does this imply that the devices are noise sensitive in the final system. The use of "hard" Highs and Lows during functional testing is done primarily to reduce the effects of the large amounts of noise typically present at the test heads of automated test equipment with cables that may at times reach several feet. The situation in a system on a PC board is less severe than in a noisy production environment. Typical recommended operating conditions are shown in Table 2.

DC ELECTRICAL CHARACTERISTICS

This table reflects the DC limits used by Signetics during their testing operations conducted under the conditions set forth in the Recommended Operating Conditions table. V_{OH}, for example, is guaranteed to be no less than 2.7V when tested with V_{CC} = +4.7V, V_{IH} = 0.8v across the temperature range of O°C to +70°C,and with an output current of I_{OH} =-1.0mA. In this table, one sees the heritage of the original junction isolated Schottky family- V_{OL} = 0.5V at I_{OL} = 20mA. This gives the user a guaranteed worst-case Low-state noise immunity of 0.3V. In the High state the noise immunity is 0.7V worst case. Although at first glance it would seem one sided to have greater noise immunity in the High state than in the Low state, more noise immunity is a useful state of affairs. Because the impedance of an output in the High state is generally much higher than in the Low state, more noise immunity in the High state is needed. This is because the noise source couple noise onto the output connection of the device. That output tries to pull the noise source down by sinking the energy to ground or to V_{CC} depending on the state. The ability of the output to do that is determined by its output impedance. The lower half of the output stage is a very low-impedance transistor which can effectively pull the noise source down. Because of the higher impedance of the upper stage of the output, it is not as effective as shunting the noise energy to V_{CC}, so that an extra 0.4V of noise immunity in the High state compensates for the higher impedance. The result is a nice balance of sink-and-drive current capabilities with the optimum amount of noise immunity in both states.

V_{OH} and V_{OL} values may vary depending on whether 5% or 10% V_{CC} swings are specified. The type of output structure, standard: 3-state, or buffer will also affect the value of V_{OH} and V_{OL}. Generally, as the output current and V_{CC} variation increase, the guaranteed minimum V_{OH} decreases and the maximum V_{OL} increases. Signetics specifies and tests V_{OH} and V_{OL} for both 5% and 10% V_{CC} swing.

I_I, the maximum input current at maximum input voltage, is a measure of the input leakage current at a guaranteed minimum input breakdown voltage. The test conditions for I_I vary according to the type of input structured being tested. Diode inputs are tested with the V_{CC}=MAX and

Table 2 RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
V_{OH}	High-level output voltage	Open collector			4.5	V
I_{OH}	High-level output current	Standard			-1	mA
		3-state			-3	mA
		Buffer			-15	mA
I_{OL}	Low-level output current	Standard			20	mA
		3-state			24	mA
		Buffer			64	mA
T_A	Operating free-air temperature range		0		70	°C

7.0V at the input. NPN inputs are tested with V_{CC}=0.0V and 7.0V at the input. It is necessary to turn off V_{CC} off for the NPN input test to measure leakage. Otherwise, the current source is on and the leakage is undetectable.When I_I is being measured on transceiver I/O pins, both V_{CC} and the input voltage is 5.5V. The reduced input voltage is necessary becaause of the output structure connected to the input structure. Output structure break down sooner than input structures and it is impossible to test the input without testing the output also.

I_{IH} for both Diode and NPN input structures is less than 20μA typically. I_{IL} is less than 20μA for NPN inputs and less than 600μA for Diode inputs. If multiple structures are tied together in the design, then the input current values also multiply. The fan-out for the devices with NPN inputs is 30 times greater than those with Diode inputs. This means the output current sinking ability of the device driving the input to the Low state could be 30 times less when driving NPN devices. For transceivers I/O pins the outputs are in the high-impedance srtate when the inputs are tested. Therefore, a maximum of 50μA extra leakage is allowed and combined with the I_{IH} and I_{IL} values. These tests are called I_{IH}+ I_{OZH} and I_{IL} + I_{OZL} to more accurately describe the true measurement being made.

I_{OZH} is tested only on Open collector outputs as a leakage test with setup conditions that would put the output in the High state if it were not in the 3-state high impedance condition. I_{OZL} is similar except the setup condition is for the Low state.

I_{OH} is tested only on Open collector outputs as leakage test for the lower output transistor structure. Both V_{CC} and V_{OH} are at the same value so that there is not a current path to or from V_{CC} that would mask the leakage path.

Short circuit output current is a parameter that has appeared on digital data sheets since the inception of integrated circuit logic devices, but the meaning and implications of that specification has totally changed. Originally, I_{OS} was an attempt to reassure the user that if a stray oscilloscope probe accidently shorted an output to ground, the device would not be damaged. In this manner an extremely long time was associated with the I_{OS} test. However, thermally induced malfunctions could occur after several seconds of sustained test.

Over a period of time, I_{OS} became a measure of the ability of an output to charge line capacitance. Assume a device is driving a long line and is in the Low state. When the output is switched High, the rise time of the output waveform is limited by the rate at which the line capacitance can be charged to the new state of V_{OH}. At the instant the output switches, the line capacitance looks like a short to ground. I_{OS} is the current demanded by the capacitive load as the voltage begins to rise and the demand decreases. We now reach the critical point in our discussion. The full value or I_{OS} need only be supplied for a few hundred microseconds at most, even with 1.0μF of line capacitance tied to thhe output, a load that is unrealistically high by several order of magnitude.

The effect of a large I_{OS} surge through the relatively small transistors that make up the upper part of the output stage is not serious- AS LONG AS THAT CURRENT IS LIMITED TO A SHORT DURATION. If the hard short is allowed to remain, the full I_{OS} current will flow through the output state and may cause functional failure or damage to the structure. As test induced failure may occur if the I_{OS} test time is excessive. As long as the condition is brief, typically 50ms or less with ATE equipment, the local heating does not reach the point where damage or functional failures may occur. As we have already seen, this is considerably longer than the time of the effective current surge that must be supplied by the device in the case of charging the capacitance. The Signetics data sheet limits for I_{OS} reflect the conditions that the part will see in the system- full I_{OS} spikes for extremely short periods of time. Problems could occur if slow test equipment of test methods ground an output for too long a time, causing functional failure or damage. DC electrical characteristics are shown in Table 3.

AC ELECTRICAL CHARACTERISTICS

The AC Electrical Characteristics table (see Table 4) contains the guasranteed limits when tested under the conditions set forth in the AC Test Circuits and Waveforms section. In some cases, the test conditions are further defined by the AC setup requirements (see Table 5)- this is generally the case with counters and flip-flops where setup and hold times are involved.

All of the AC Characteristics are guaranteed with 50pF load capacitance. The reason for choosing 50pF over 15pF as load capacitance is that it allows more leeway in dealing with stray capacitance, and also loads the device during rising or falling output transitions, which more closely resembles the loading to be expected in average applications, thus giving the designer more useful delay figures.

Although the 50pF load capacitance will increase the propagation delay by an average of about 1ns for FAST devices, it will increase several ns for standard Schottky devices.

The load resistor of 500Ω is conveniently specified as both a pull-up and pull-down load resistor.

FAST produucts are being released in the surface mounted SO package as a commercial option. Because of the reduced inductance inherent in this package,

Data Sheet Specification Guide

Table 3
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]	LIMITS			UNIT	V_{CC}[4]
					Min	Typ[2]	Max		
V_{IH}	High-level input voltage			Recognized as a High signal over recommended V_{CC} and T_A range	2.0			V	
V_{IL}	Low-level input voltage			Recognized as a Low signal over recommended V_{CC} and T_A range			0.8	V	
$V_{IK}(V_{CD})$	Input clamp diode voltage			I_{IN} = -18mA			-1.2	V	MIN
V_{OH}	High-level output voltage	Standard[5]	±10%V_{CC}	I_{OH} = -1mA	2.5	3.4		V	MIN
			±5%V_{CC}		2.7	3.4		V	MIN
		3-state	±10%V_{CC}	I_{OH} = -3mA	2.4	3.3		V	MIN
			±5%V_{CC}		2.7	3.3		V	MIN
		Buffers	±10%V_{CC}	I_{OH} = -15mA	2.0	3.2		V	MIN
			±5%V_{CC}		2.0	3.1		V	MIN
V_{OL}	Low-level output voltage	Standard[5]	±10%V_{CC}	I_{OL} = 20mA		0.30	0.5	V	MIN
			±5%V_{CC}			0.30	0.5	V	MIN
		3-state	±10%V_{CC}	I_{OL} = 24mA		0.35	0.5	V	MIN
			±5%V_{CC}			0.35	0.5	V	MIN
		Buffers	±10%V_{CC}	I_{OL} = 48mA		0.38	0.55	V	MIN
			±5%V_{CC}	I_{OL} = 64mA		0.42	0.55	V	MIN
I_I	High-level current breakdown test	Diode inputs		V_{IN} = 7.0V			100	µA	MAX
		NPN inputs		V_{IN} = 7.0V			100	µA	0.0V
		Transceiver I/O pins		V_{IN} = 5.5V			1.0	mA	5.5V
I_{IH}	High-level input current			V_{IH} = 2.7V (20µA X n High U.L.)			n(20)	µA	MAX
I_{IL}	Low-level input current	Diode inputs		V_{IL} = 0.5V (-0.6mA X n Low U.L.)			n(-0.6)	mA	MAX
		NPN inputs		V_{IL} = 0.5V (-20µA X n Low U.L.)			n(-20)	µA	MAX
$I_{IH}+I_{OZH}$	High-level input current (I/O pins)			V_{IH} = 2.7V (20µA X n High U.L.)			n(20) +50	µA	MAX
$I_{IL}+I_{OZH}$	Low-level input current (I/O pins)	Diode inputs		V_{IL} = 0.5V (-0.6mA X n Low U.L.)			n(-0.6)	mA	MAX
		NPN inputs		V_{IL} = 0.5V (-20µA X n Low U.L.)			n(-20) -50	µA	MAX
I_{OZH}	3-state, High-level OFF current			V_{OUT} = 2.7V			50	µA	MAX
I_{OZL}	3-state, Low-level OFF current			V_{OUT} = 0.5V			-50	µA	MAX
I_{OH}	Open collector output leakage			V_{OH} = 4.5V			250	µA	MIN
I_{OS}	Output short-circuit current	Standard[5], 3-state		V_{OUT} = 0V	-60		-150	mA	MAX
		Buffer driver			-100		-225	mA	MAX
I_{CEX}	Output High leakage current			V_{OUT} = 5.5V, not tested on NPN transceivers and Open Collector outputs			250	µA	MAX
I_{ZZ}	Bus drainage test			V_{OUT}= 5.5V, 3-state			500	µA	0.0V

NOTES:
1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. Unless otherwise stated on individual data sheets.
3. Typical characteristics refer to V_{CC} = 5V, T_A = 25°C.
4. MIN and MAX refer to the values listed in the data sheet table of recommended operating conditions.
5. Standard refers to the totem-pole pull-up circuitry commonly used for the particular family, as distinguished from buffers, line drivers or 3-state outputs.
6. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

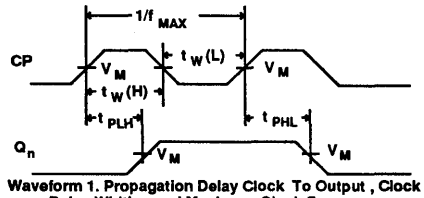
Table 5 AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F373	Waveform 3	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n		Waveform 2	5.0 3.0	9.0 4.0	11.5 7.0	5.0 3.0	13.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	5.0 5.6	11.0 7.5	2.0 2.0	12.0 8.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	4.5 3.8	6.5 5.0	2.0 2.0	7.5 6.0	ns ns
f_{MAX}	Maximum Clock frequency	74F374	Waveform 1	100			70		ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	9.0 5.3	11.5 7.5	2.0 2.0	12.5 8.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	5.3 4.3	7.0 5.5	2.0 2.0	8.0 6.5	ns ns

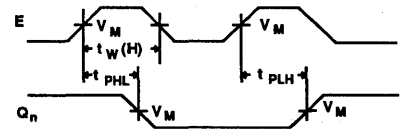
Table 6 AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time D_n to E	74F373	Waveform 4	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to E		Waveform 4	3.0 3.0			3.0 3.0		ns
$t_w(H)$	E Pulse width, High		Waveform 1	6.0			6.0		ns
$t_s(H)$ $t_s(L)$	Set-up time D_n to CP	74F374	Waveform 5	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP		Waveform 5	2.0 2.0			2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1	7.0 6.0			7.0 6.0		ns

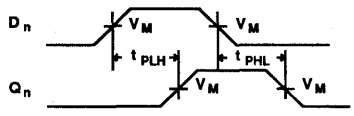
AC WAVEFORMS



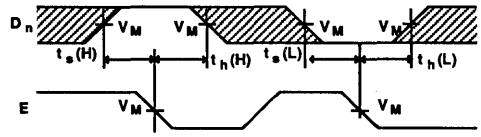
Waveform 1. Propagation Delay Clock To Output , Clock Pulse Widths, and Maximum Clock Frequency



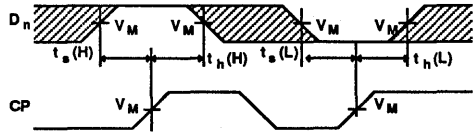
Waveform 2. Propagation Delay,Enable to Outputs And Enable Pulse Width



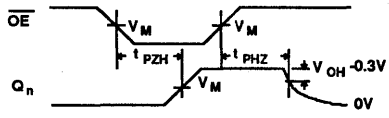
Waveform 3. Propagation Delay, Data To Outputs



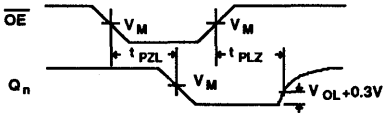
Waveform 4. Data Setup And Hold Times



Waveform 5. Data Setup And Hold Times



Waveform 6. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 7. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

minimum propagation delays are being derated by 0.2ns. This is reflected by a note at the bottom of Table 4.

TEST CIRCUITS AND WAVEFORMS

The 500Ω load resistor, R_L to ground, as described in Figure 1, acts as a ballast to slightly load the totem-pole pull-up and limit the quiescent High-state voltage to about +3.5V. Otherwise, an output would rise quickly to about +3.5V, but then continue to rise slowly up to about +4.4V. On the subsequent High-to-Low transition, the observed t_{PHL} would vary slightly with duty cycle, depending on how long the output voltage was allowed to rise before switching to the Low state. Perhaps more importantly, the 500Ω load to ground can be a high frequency, passive probe for a sampling scope, which costs much less than the equivalent high impedance probe. Alternately, the 500Ω load to ground can be simply be a 450Ω resistor feeding into a 50Ω coaxial cable leading to a sampling scope input connector, with the internal 50Ω termination of the scope completing the path to ground. Note that with this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a 50Ω termination for the pulse generator that supplies the input signal.

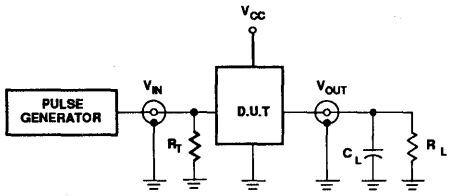
Figure 2, Test Circuit for 3-state outputs, shows a second 500Ω resistor from the device output to switch. For most measurements this switch is open; it is closed for measuring a device with Open collector outputs and for measuring one set of the enable/disable parameters (Low-to-OFF and OFF-to-Low) of a 3-state output. With the switch closed, the pair of 500Ω resistors and the +7.0V supply establish a quiescent High level of +3.5V, which correlates with the High-level discussed in the preceding paragraph.

As shown in Figure 3, AC Waveforms for FAST 74F373, 74F374, the disable times are measured at the point where the output voltage has risen or fallen by 0.3V from the quiescent level (i.e., Low for t_{PLH}^2 or High for t_{PHL}^2).

Since the rising or falling waveform is RC-controlled, 0.3V of change is more linear and is less susceptible to exrternal influences.

More importantly, from the system designer's point of view, 0.3V is adequate to ensure that a device output has turned OFF. It also gives system designers more realistic delay times to use in calculating minimum cycle times.

Good, high frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths. Input signals should have rise and fall times of 2.5ns, and signal swing of 0V to +3.0V, 1.0MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{MAX}. Two pulse generators are usually required for testing such parame-



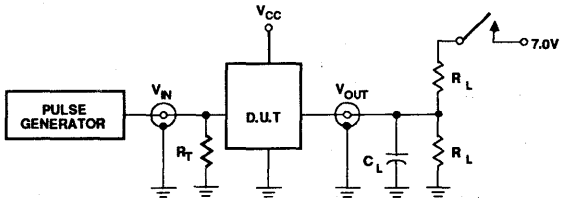
DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Figure 1. Test Circuit For Totem-Pole Outputs



SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Figure 2. Test Circuit For 3-State Outputs

DC SYMBOLS AND DEFINITIONS

Voltages - All voltages are referenced to ground. Negative voltage limits are specified as absolute values (i.e., -10V is greater than -1.0V).

V_{CC} **Supply voltage**: The range of power supply voltage over which the device is guaranteed to operate within the specified range.

V_{IKMAX} **Input clamp diode voltage**: The most negative voltage at an input when the specified current is forced out of that input terminal. This parameter guarantees the integrity of the input diode intended to clamp negative ringing at the input terminal.

V_{IH} **High-level input voltage**: The range of input voltages recognized by the device as a logic High.

V_{IHMIN} **High-level Minimum input voltage**: This value is the guaranteed input High threshold for the device. The minimum allowed input High in a logic system.

V_{IL} **Low-level input voltage**: The range of input voltages recognized by the device as a logic Low.

V_{ILMAX} **Low-level Maximum input voltage**: This value is the guaranteed input Low threshold for the device. The maximum allowed input Low in a logic system.

V_M **Measurement voltage**: The reference voltage level on AC waveforms for determining AC performance. Usually specified as 1.5V for the FAST family.

V_{OHMIN} **High-level output voltage**: The minimum guaranteed High voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.

V_{OLMAX} **Low-level output voltage**: The maximum guaranteed Low voltage at an output terminal sinking the sopecified load current I_{OL}.

V_{T+} **Positive-going threshold voltage**: The input voltage of a variable threshold device which causes operation according to specification at the input transition rises from below V_{T-} (Min).

V_{T-} **Negative-going threshold voltage**: The input voltage of a variable threshold device which causes operation according to specification at the input transition falls from from above V_{T+} (Max)

Currents - Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

I_{CC} **Supply current**: The current flowing into the V_{CC} supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst-case opertation unless specified.

I_I **Input leakage current**: The current flowing into an input when the maximum allowed voltage is applied to to the input.

I_{IH} **High-level input current**: The current flowing into an input when a specified High level voltage is applied to that input.

I_{IL} **Low-level input current**: The current flowing out of an input when a specified Low-level voltage is applied to that input.

I_O **Output current**: The output current that is approximately one half of the short-circuit output current (I_{OS})

I_{OH} **High-level output current**: The leakage current flowing into a turned off open collector output with a specified High-level output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the High-level state.

I_{OH1} **High-level output current**: The current necessary to guarantee the Low to High transition in a 30 ohm transmission line on the incident wave.

I_{OL} **Low-level output current**: The flowing into an output which is the Low-level state.

I_{OL1} **Low-level output current**: The current necessary to guarantee the High to Low transition in a 30 ohm transmission line on the incident wave.

I_{OS} **Short-circuit output current**: The current flowing out of an output which is in the High-level state when that output is short circuit to ground.

I_{OZH} **OFF-state output current High**: The current flowing into a disabled 3-state output with a specified High level output voltage applied.

I_{OZL} **OFF-state output current Low**: The current flowing out of a disabled 3-state output with a specified Low level output voltage applied.

Data Sheet Specification Guide

AC SYMBOLS AND DEFINITIONS

f_{MAX} **Maximum clock frequency**: The maximum input frequency at a clock input for predictable performance. Above this frequency the device may cease to function.

t_{PLH} **Propagation delay time**: The time between specified reference points on the input and the output waveforms with the output changing from the defined Low- level to High- level.

t_{PHL} **Propagation delay time**: The time between specified reference points on the input and the output waveforms with the output changing from the defined High- level to Low- level.

t_{PHZ} **Output Disable time from High level to a 3-state output**: The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the High- level to a high impedance "OFF" state.

t_{PLZ} **Output Disable time from Low level of a 3-state output**: The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the Low- level to a high impedance "OFF" state.

t_{PZL} **Output Enable time to a Low level of a 3-state output**: The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high impedance "OFF" state to a High- level.

t_{PZL} **Output Enable time to a Low level of a 3-state output**: The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high impedance "OFF" state to a Low level.

t_s **Setup time**: The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_h **Hold time**: The interval immediately following the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_w **Pulse width**: The time between the reference point on the leading and trailing edges of a pulse.

t_{REC} **Recovering time**: The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.

t_{TLH} **Transition time, Low to High**: The time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from Low to High.

t_{THL} **Transition time, High to Low**: The time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from High to Low.

t_r, t_f **Clock input and rise and fall times**: 10% and 90% value.

Signetics

Design Considerations

FAST Products

INTRODUCTION

The properties of high-speed FAST logic circuits dictate that care be taken in the design and layout of a system.

Some general design considerations are included in this section. This is not intended to be a thorough guideline for designing FAST systems, but a reference for some of the constraints and techniques to be considered when designing a high-speed system.

HANDLING PRECAUTIONS

As described in the circuit characteristics section, FAST devices are susceptible to damage from electrostatic discharge (ESD).

- Signetics FAST devices are shipped in conducting foam or anti-static tubes and foil-lined boxes to minimize ESD during shipment and unloading.
- Before opening the shipment of FAST devices, make sure that the individual is grounded and all handling means (such as tools, fixtures, and benches) are grounded.
- After removal from the shipping material, the leads of the FAST devices should always be grounded. In other words, FAST devices should be placed leads-down on a grounded surface, since ungrounded leads will attract static charge.
- Do not insert or remove devices in sockets with power applied. Ensure that power supply transients, such as occur during power turn on-off, do not exceed absolute maximum ratings.
- After assembly on PC boards, ensure that ESD is minimized during handling, storage or maintenance.
- FAST inputs should never be left floating on a PC board. This precaution applies to any TTL family. As a temporary measure, a resistor with a resistnace greater than 10 kΩ should be soldered on the input. The resistor will limit accidental damage if the PC board is removed and brought into contact with static-generating material.

INPUT CLAMPING

FAST circuits are provided with clamp diodes on the device inputs to minimize negative ringing effects. These diodes should not be used to clamp negative DC voltages or long duration, negative pulses. Certain FAST part types with the NPN base input structure also provide clamping of positive overshoots.

UNUSED INPUTS

Proper design rules dictate that all unused inputs on TTL devices be tied either High or Low. This is especially important with FAST logic.

Electrically open inputs can degrade AC noise immunity as well as the switching speed of the device. Small geometries make FAST more susceptible to damage by ESD than other TTL families. Tying inputs to V_{CC} or GND, directly or through a resistor, protects the device from in-circuit electrostatic damage. Additionally, while most unconnected TTL floats High, FAST devices with NPN inputs float Low.

FAST devices do not require an input resistor to tie the input High. Inputs can be connected directly to V_{CC} as well as ground.

Possible ways of handling unused inputs are:

1. Unused active-High NAND or AND inputs to V_{CC}. The inputs should be maintained at a voltage greater than 2.7V, but should not exceed the absolute maximum rating.
2. Connect unused active-High NOR or OR inputs to ground.
3. Tie unused active-High NAND or AND inputs to a used input of the same gate, provided that the High-level fanout of the driving circuit is not impaired.
4. Connect the unused active-High NAND or AND inputs to the output of an unused gate that is forced High.

MIXING FAMILIES WITH OTHER TTL FAMILIES

Mixing the slower TTL families such as 74 and 74LS with the higher speed families such as 74F is possible but must be done with caution. Each family of TTL devices has unique input and output characteristics optimized to achieve the desired speed or power features.

The unique speed/power characteristics of FAST devices are achieved partially by the internal fast rise and fall times, as well as those at input and output modes. These fast transitions can cause noise of various types in a system. Power and ground line noise are generated by the faster transitions of the current in the output load capacitance. Signal line noise can also be generated by the fast output transitions.

The noise generated by 74F devices can be minimized in systems designed with shorter signal lines, good ground planes, well-bypased power distribution networks, layouts that minimize adjacent signal lines that run parallel, and improved impedance matching in signal lines to reduce transmission line type reflections.

INPUT-OUTPUT LOADING AND FAN-OUT TABLE

For convenience in system design, the input-output loading and fan-out charactristics of each circuit are specified in terms of unit load and actual load value. One FAST Unit Load (U.L.) in the High state is defined as 20μA; thus both the input leakage current, I_I, and output High current-sourcing capability, I_{OH}, are normalized to 20μA.

Similarly, one FAST Unit Load (U.L.) in the Low state is defined as 0.6mA and both the input Low current, I_{IL}, and input Low current-sinking capability, I_{OL}, are normalized to 0.6mA.

For added convenience, the actual load value in amperes is listed in the column adjacent to U.L..

On some FAST devices, high-impedance NPN base input structure has been utilized. With this structure, the Low level input current, I_{IL}, has been reduced to 20μA. This characteristics is 30 times lower than the requirement of devices using the conventional input structure. This feature improves fan-out in the Low state and can help reduce part count in system design by eliminating buffers in some applications.

CLOCK PULSE REQUIREMENTS

All FAST clock inputs are buffered to increase their tolerance of slow postive-clock edges and heavy ground noise. Nevertheless, the rise time on positive-edge-triggered devices should be less than the nominal clock-to-output delay

Table 1 LOADING COMPARISONS

DRIVING DEVICE FAMILY	I_{OL}(Min)	DRIVEN DEVICE FAMILY						
		74F	74F(NPN)	74LS	74	74S	8200/9300	82S00
		I_{IL} (Max)						
		0.6mA	20μA	0.4mA	1.6mA	2.0mA	1.6mA	0.4mA
		Maximum Number of Loads Driven						
74F	20mA	33	1,000	50	12.5	10	12	50
74F(NPN)	64mA	106	3200	160	40	32	40	160
74LS	8mA	13	400	20	5	4	5	20
74LS Buffer	24mA	40	1,200	60	15	12	15	60
74	16mA	26	800	40	10	8	10	40
74Buffer	40mA	78	2,400	120	30	24	30	120
74S	20mA	33	1,000	50	12.5	10	12	50
74S Buffer	60mA	100	3,000	150	37.5	30	37	150

measured betwween 0.8 to 2.0V levels of the clock driver for added safety margin against heavy ground noise. Not only a fast rising, clean clock pulse is required, but the path between the clock drive and clock input of the device should be well shielded from electromagnetic noise.

INPUT LOADING AND OUTPUT DRIVE COMPARISON

The logic levels of all TTL products are fully compatible with each other. However, the input loading and the output drive characteristics of each family are different and must be taken into consideration when mixing them in a system. Table 1 shows the relative drive capabilities of each family for commercial temperature and voltage ranges.

FAST OUTPUTS TIED TOGETHER

The only FAST outputs that are designed to be tied together are open collector and 3-state outputs. Standard FAST outputs should not be tied together unless their logic levels will always be the same; either High or Low. When connecting open collector or 3-state outputs together, some general guidelines must be observed.

OPEN COLLECTOR OUTPUT

These devices must be used whenever two or more OR-tied outputs will be at opposite logic levels at the same time. These devices must have pull-up resistor (or resistors) added between the OR-tie connector and V_{CC} to establish an active-High level. Only special high voltage buffers can be tied to a higher voltage than V_{CC}. The minimum amd maximum size of the pull-up resistor is determined

$$R(Min) = \frac{V_{CC}(Max)-V_{OL}}{I_{OL}-N_2\ (I_{IL})}$$

$$R(Max) = \frac{V_{CC}(Min)-V_{OL}}{N_1(I_{OH})-N_2\ (I_{IH})}$$

where:

I_{OL} = Minimum I_{OL} guarantee or OR tie elements

$N_2(I_{IL})$ = Cumulative maximum input Low current for all inputs tied to OR-tie connection.

$N_1(I_{OH})$ = Cumulative maximum output High leakage current for all outputs tied to OR-tie connection.

$N_1(I_{IH})$ = Cumulative maximum input High leakage current for all outputs tied to OR-tie connection.

If a resistor divider network is used to provide the High level, the R (Max) must be decreased enough to provide the required [V_{OH}/R (pull-down)] current

3-STATE OUTPUTS

3-state outputs are designed to be tied together, but are not designed to be active simultaneously. In order to minimize noise and protect the outputs from excessive power dissipation, only one 3-state output should be active any time. This generally requires that the output enable signals be non-overlapping. When TTL decoders are used to enable 3-state outputs, the decoder should be disabled while the address is being changed. Since all TTL decoder outputs are subject to decoding spikes, non-overlapping signals cannot normally guarantee when the address is changing.

Since most 3-state output enable signals are active-Low, shift register or edge-triggered storage registers provide good output enable buffers. Shift registers with one circulating Low bit, such as the 'F164 or'F194, are ideal for sequential enable signals. The 'F174 or 'F273 can be used to buffer enable signals from TTL decoders or microcode (ROM) devices. Since the outputs of these registers will change from Low-to-High faster than from High-to-Low, the selection of one device at a time is assured.

GND

Good system design starts with a well thought out ground layout. Try to use ground plane if possible. This will save headaches later on. If ground strip is used, try to reduce ground path in order to minimize ground inductance. This prevents crosstalk problems. Quite often, jumper wire is used for connecting to ground at the breadboarding stage, but a solid ground must be used even at the breadboarding stage.

V_{CC}

Typical dynamic impedance of un-bypassed V_{CC} runs from 50Ω to 100Ω. depending on V_{CC} and GND configuration. This is why a sudden current demand, due to an IC output switching, can cause momentary reduction in V_{CC} unless a bypass (decoupling) capacitor is located near V_{CC}.

Not only is there a sudden current demand due to output switching transient, there is also a heavy current demand by the buffer driver. Assuming the buffer output sees a 50Ω dynamic load and the buffer Low-to-High transition is 2.5V, the current demand is 50mA per buffer. If it is an octal buffer, the current demand could be 0.4mA per package in 3ns time!

The next step is to figure out the capacitance requirement for each bypass capacitor. Using the previously-mentioned octal buffer and assuming the V_{CC} droop is 0.1V,
then C is:

$C = 0.4A \times 3 \times 10^{-9}$ sec/0.1V
$= 12 \times 10F^{-9}$

This formula is derived as follows:

$cQ = CV$

by differentiation:

$\Delta Q/\Delta t = C\Delta V/\Delta t$

since

$\Delta Q/\Delta t = i$

the equation becomes

$i = C\Delta V/\Delta t$

hence

$C = i\Delta t/\Delta V$

Select the C bypass ≥0.02μF and try to use a high quality RF capacitor. Place one bypass capacitor for each buffer and one bypass capacitor every two other types of IC packages. Make sure that the leads are cut as short as possible.
In addition, place bypass capacitors on a board to take care of board-level current transients.

CROSS-TALK

The best way to handle cross-talk is to prevent it from occuring in the first place; quick-fixes are troublesome and costly. To prevent cross-talk, maximize spacing between signal lines and minimize spacing between signal lines and ground lines.

Preferably, place ground lines between signals. For added precaution, add a ground trace alongside either the potential cross-talker or the cross listener.

For back-plane or wire-wrap, use twisted pair for sensitive functions such as clocks, asynchronous set or reset, or asynchronous parallel load. In flat cable, make every other conductor ground.

For multilayer P.C. boards, run signal lines in adjacent planes perpendicular to prevent magnetic coupling, and limit capacitive coupling. Use power shield (V_{CC} or ground plane) in between signal planes.

Since any voltage change, noise or otherwise, arriving at the unterminated end of transmission lines double in amplitude, even a partially terminated line reduces the amplitude of the signal (noise or otherwise) appearing at the end of the line; therefore, using a terminating resistor whose value is equal to the line characteristics impedance will help reduce cross talk.

Signetics

Section 5
Military Information

FAST Products

Signetics Military Information

FAST Products

INTRODUCTION

Effective January 1, 1985, this section has been superceded by the 1985 Military Product Data Manual. Information regarding the manual can be obtained from the Military Division in Sacramento. (916) 925-6700.

MILITARY STANDARD PRODUCTS

The Signetics Military product line offering includes JAN Qualified Class S and B, and Class B vendor standard products. These products are designed to offer our customers the optimum of quality, reliability, delivery and cost. The benefits of these products provide our customers:

- Industry wide standardization
- Fewer custom specifications.
- Cost savings associated with larger lots.
- Better lead times by reducing specifica tion negotiation time and allowing off-the-shelf procurement.
- Industry standard marking.

JAN QUALIFIED PRODUCT

JAN qualified products are offered to give our customers the highest quality and reliability. The JAN processing levels (Class S and B) are a result of the Governments product standardization programs, and our JAN production lines are certified by the qualifying activity, the Defence Electronics Supply Center (DESC). Signetics strongly recommends the use of JAN products, which are listed on the MIL-M-38510 Qualified Products List (QPL).

JAN qualified products are fabricated, assembled, tested, and inspected in U.S. Government certified facilities in Sunnyvale, California (wafer fab); Orem Utah (wafer fab, assembly; and in Sacramento, California (burn-in, test, quality conformance inspection).

Testing and inspection to MIL-M-38510 is monitored by resident Government Source Inspection (GSI) personnel representing the Defense Contract Administration Services (DCAS).

DESC prohibits any customer imposed additions, deviations, omissions, or waivers on procurement of JAN products. Products must conform to Government specifications prior to shipment and are verified by Signetics Quality Control. A Cerificate Conformance and Procurement Traceabilty is supplied with each lot shipped.

JAN Qualified products are listed in QPL-38510, issued periodically by DESC. For current QPL information, customers may contact their local sale represenattive, Military Marketing in Sacramento, or directly with DESC EQM at (513) 296-6355. The JAN products listed herein should be considered valid only on its date of publication.

These categories of product conform to Qualilty Levels A and B of MIL-HDBK-217 (πQ=0.5 Class S, 1.0 for Class B).

The example at the bottom of this page illustrates the part numbering system for JAN products, the part number is per MIL-M-38510.

SIGNETICS CLASS B STANDARD PRODUCT (RB)

Signetics Class B Standard product is offered for use when no JAN product is qualified on the QP, DESC Drawing product is not available, or when program requirements allow the use of vendor standard product.

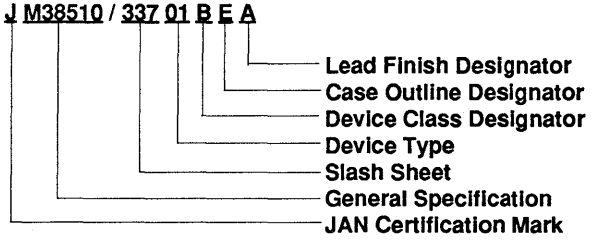
Class B standard product conforms to MIL-STD-883, general provisions Paragraph 1.2.1 (and its sub-paragraphs), except where noted. (See Product Noncompliance Section of Miltary Data Book and/or Hand Book). No other claims, expressed or implied, are made of equivalence to JAN product or to MIL-38510. Signeticcs compliant product also conforms with JEDEC Publication 101, except for marking content.

Electronic test requirements are as stated in the most current **Signetics Military Data Manual only.**

- 100% final electrical tests include all Data Manual parameter limits, test conditions, and temperature applicable to Subgroups 1, 2, 3, 7, and 9 of MIL-STD-883, Method 5004 for digital products, or to Subgroups 1, 2, 3, 3, and 9 for Linear Products.
- Group A sample electrical inspection tests include all final electrical subgroups as well as all othe Data Manual parameters with specified minimum or maximum limits.
- End point electrical tests used for QCI inspection sampling (Groups C and D) are those Data Manual parameter limits, test conditions, and temperatures applicable to Group A Subgroups 1, 2, annd 3 per MIL-STD-883, Method 5005, or to Subgroup 1 for Linear Products.

Data Manual parameters which have no specified minimum of maximum limits (typical performance only) are not tested. Parameters which have limits specified at 25°C only, are tested only at that temperature. Detailed parameter assignment to subgroups and other test detail are contained in documented Signetics internal Product Electrical specifications, and are available upon request. Actual test program symbolics area availble for customer review at the factory, but are considered proprietary and will not be copied or otherwise distributed outside of Signetics.

QCI Groups A and B testing are performed on all products and packages per MIL-M-38510and MIL-STD-883, Method 5005. Signetics utilize inline Group A and alternate Group B for all lines.



Military Information

QCI Groups C and D are routinely performed on all compliant families and package types.

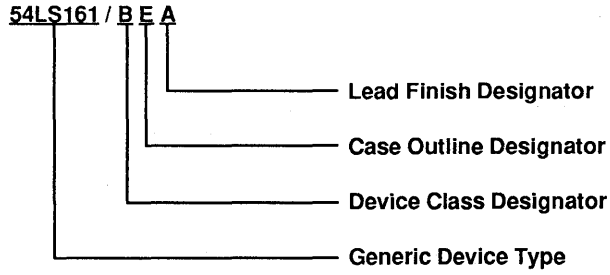
Waivers, deviations, or exceptions of any kind deemed necessary in the course of the contracts must be issued in accordance with DOD–STD–480. Should Signetics have knowledge of the need for waivers at the time of response to quote (RFQ) or order entry, that information will be transmitted prior to order entry.

Package types which do not have case outline letters assigned in MIL–M–38510, Appendix C, will be assigned case outline letters per JEDEC Publication 101.

The Signetics Standard Product Assurance Plan documentation is available for customer review at the factory, and is considered proprietary.

This category of product conforms to quality level B–2 of MIL–HD–BK–217 (πQ=6.5).

For Class B Standard Product, the part number is listed as follows:



Signetics

Section 6
74F Series Data Sheets

FAST Products

Signetics

FAST 74F00 Gate

Quad 2-Input NAND Gate

FAST Products

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F00	3.4 ns	4.4 mA

FUNCTION TABLE

INPUTS		OUTPUT
D_{na}	D_{nb}	$\overline{Q}_n$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

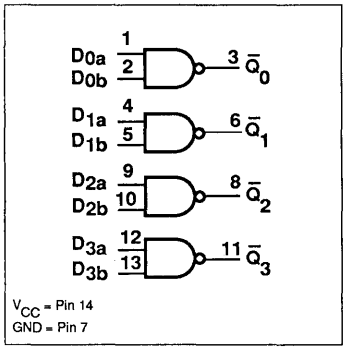
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F00N
14-Pin Plastic SO	N74F00D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

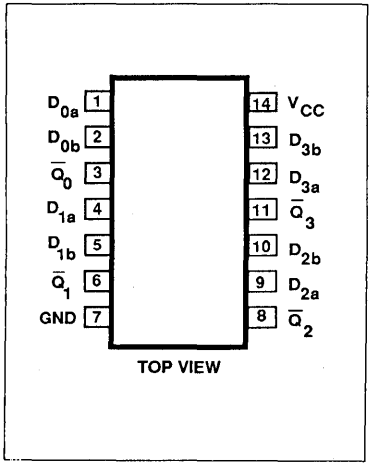
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}_n$	Data output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

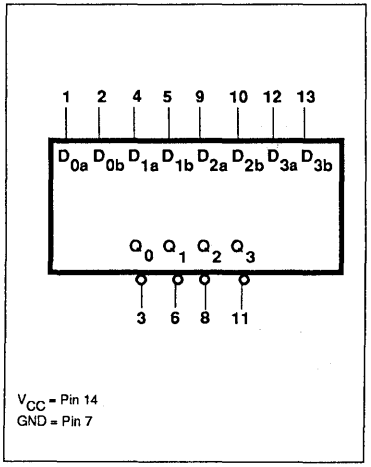
LOGIC DIAGRAM



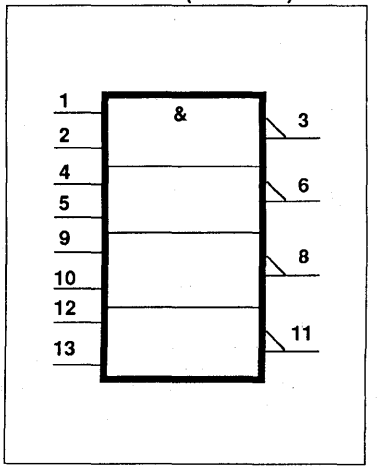
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} =GND		1.9	2.8	mA
		I_{CCL}		V_{IN} =4.5V		6.8	10.2	mA

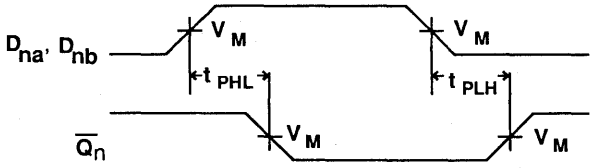
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to $\overline{Q}_n$	Waveform 1	2.4 2.0	3.7 3.2	5.0 4.3	2.4 2.0	6.0 5.3	ns

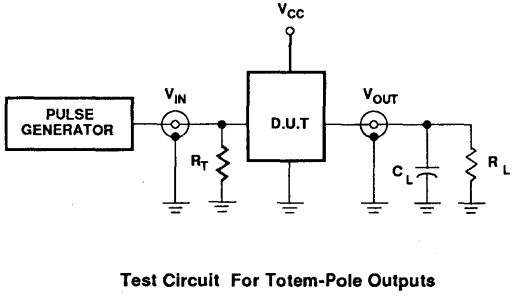
AC WAVEFORMS



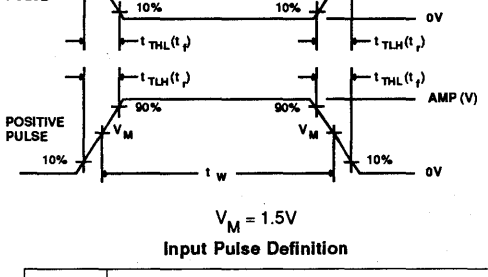
Waveform 1.
For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F02 Gate

Quad Two-Input NOR Gate

FAST Products

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F02	3.4 ns	4.4 mA

FUNCTION TABLE

INPUTS		OUTPUT
D_{na}	D_{nb}	$\overline{Q}_n$
L	L	H
L	H	L
H	L	L
H	H	L

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

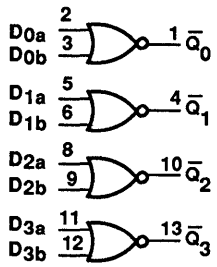
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F02N
14-Pin Plastic SO	N74F02D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}_n$	Data output	50/33	1.0mA/20mA

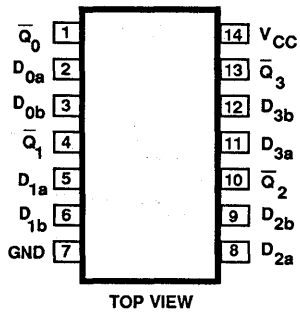
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC DIAGRAM



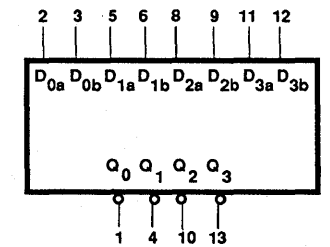
V_{CC} = Pin 14
GND = Pin 7

PIN CONFIGURATION



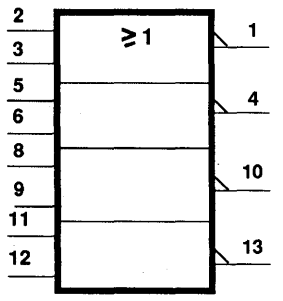
TOP VIEW

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]	I_{CCH}	V_{CC} = MAX			3.0	5.6	mA
		I_{CCL}				7.0	13.0	mA

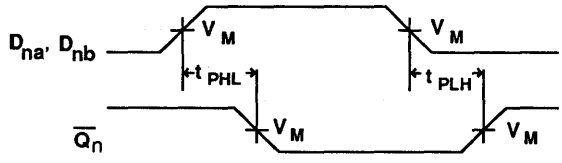
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs open.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to $\overline{Q}_n$	Waveform 1	2.5 2.0	4.4 3.2	5.5 4.3	2.5 2.0	6.5 5.3	ns

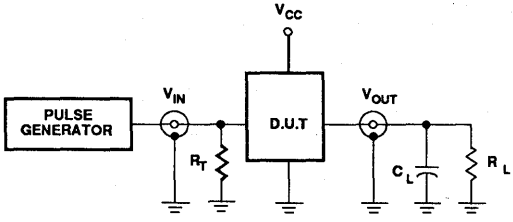
AC WAVEFORMS



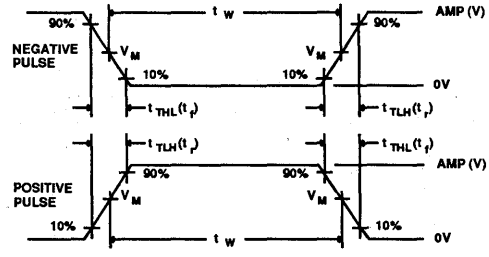
Waveform 1.
For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F04 Inverter

Hex Inverter

FAST Products

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F04	3.5 ns	6.9 mA

FUNCTION TABLE

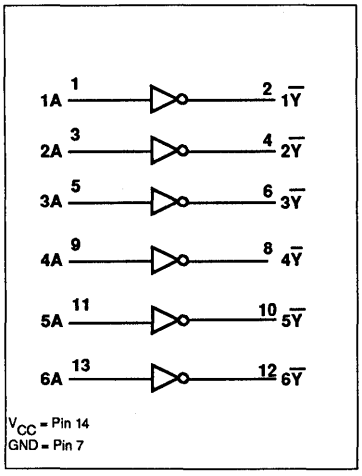
INPUT	OUTPUT
A	$\overline{Y}$
L	H
H	L

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F04N
14-Pin Plastic SO	N74F04D

LOGIC DIAGRAM

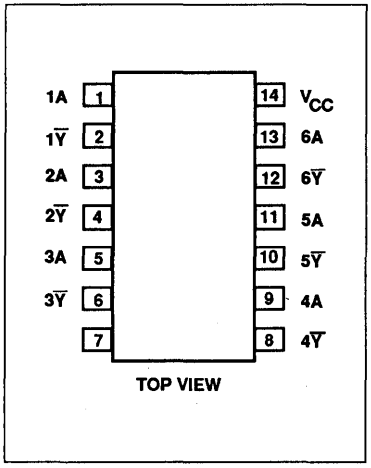


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

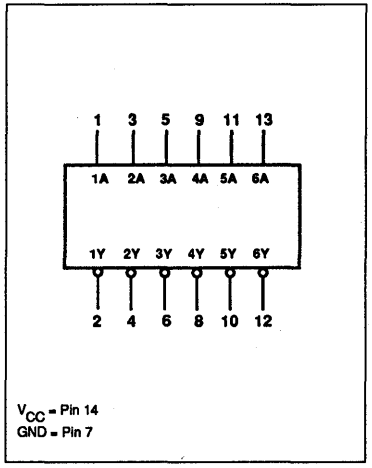
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA	Data input	1.0/1.0	20µA/0.6mA
n$\overline{Y}$	Data Output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

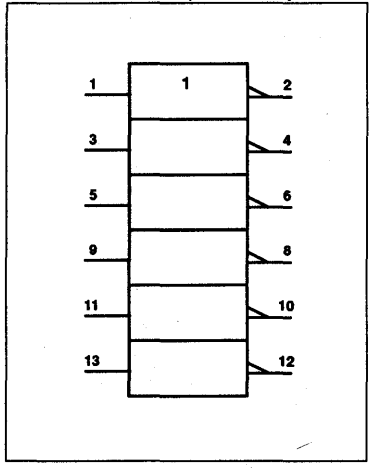
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN}=GND		2.8	4.2	mA
		I_{CCL}		V_{IN}=4.5V		10.2	15.3	mA

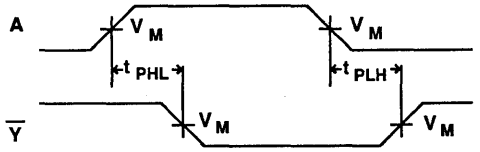
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A to $\overline{Y}$	Waveform 1	2.4 1.5	3.7 3.2	5.0 4.3	2.4 1.5	6.0 5.3	ns

AC WAVEFORMS

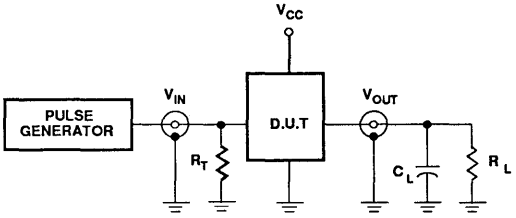


Waveform 1.

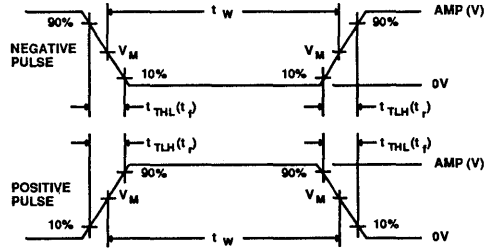
Propagation Delay for Input to Output

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F06, 74F07 Inverter/Buffer/Drivers

74F06 Hex Inverter Buffer/Driver (Open Collector)
74F07 Hex Buffer/Driver (Open Collector)

FAST Products

Product Specification

FEATURES

- **Open Collector output drive 64mA**
- **High speed**
- **12V output termination voltage**
- **Symmetrical propagation delays**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F06	3.5ns	18mA
74F07	4.5ns	21mA

ORDERING INFORMATION

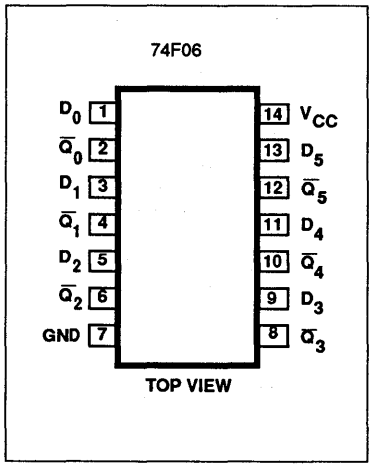
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F06N, N74F07N
14-Pin Plastic SO	N74F06D, N74F07D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

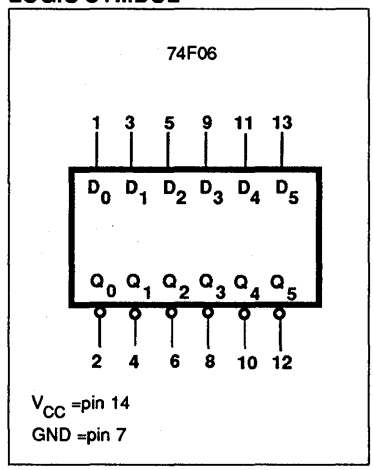
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_n	Data input	1.0/1.0	20µA/0.6mA
$\overline{Q}_n$	Data output ('F06)	OC/106.7	OC/64mA
Q_n	Data output ('F07)	OC/106.7	OC/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
2. OC = Open Collector.

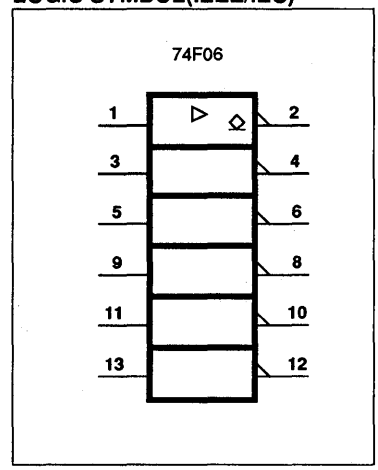
PIN CONFIGURATION



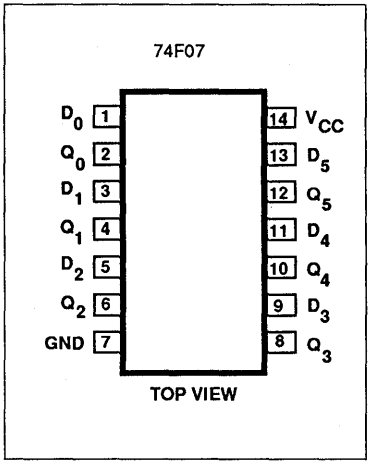
LOGIC SYMBOL



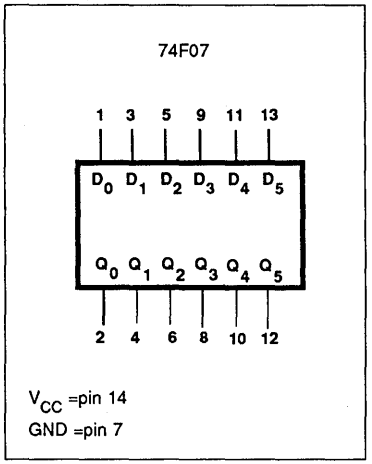
LOGIC SYMBOL(IEEE/IEC)



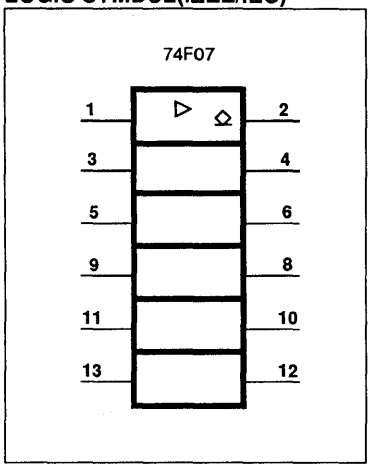
PIN CONFIGURATION



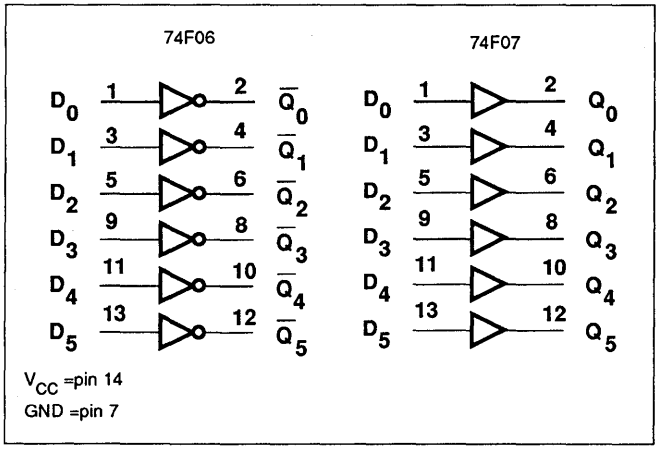
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS	OUTPUTS	
	74F06	74F07
D_n	$\overline{Q}_n$	Q_n
L	H	L
H	L	H

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +12	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	High-level output voltage			12	V
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

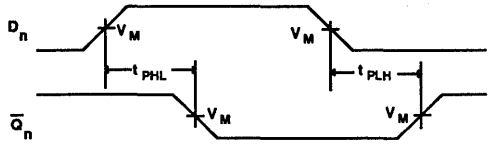
SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
I_{OH}	High-level output current			V_{CC} = MIN, V_{IL} = MAX, V_{OH} =MAX, V_{IH} = MIN					250	µA
V_{OL}	Low-level output current			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} =MAX	±10%V_{CC}			0.55	V
						±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{CC}	Supply current [total]	74F06	I_{CCH}	V_{CC} = MAX				5.0	8.0	mA
			I_{CCL}					30	43	mA
		74F07	I_{CCH}					10	14	mA
			I_{CCL}					32	45	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

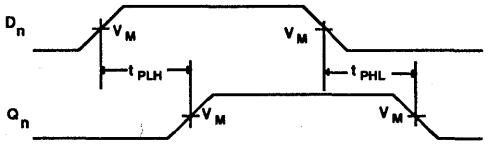
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 100Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 100Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	74F06	Waveform 1	2.0 1.5	3.5 3.0	6.0 5.5	1.5 1.0	6.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F07	Waveform 2	2.0 3.0	4.0 5.0	6.0 7.0	2.0 2.5	6.5 7.5	ns

AC WAVEFORMS



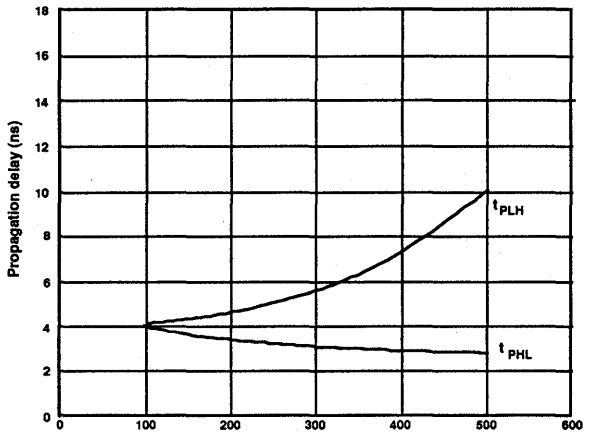
Waveform 1. Propagation Delay For Inverting outputs



Waveform 2. Propagation Delay For non-inverting outputs

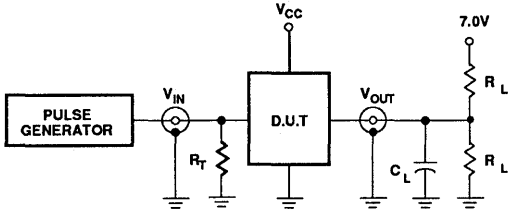
NOTE: For all waveforms, V_M = 1.5V.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



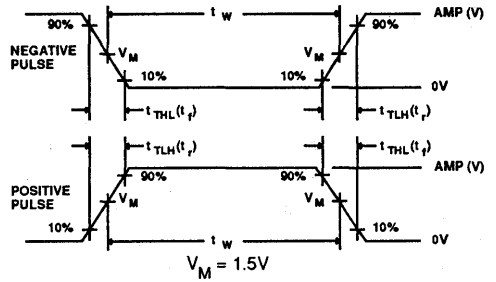
Test Circuit for Open Collector Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F08 Gate

Quad Two-Input AND Gate

FAST Products

Product Specification

FUNCTION TABLE

INPUTS		OUTPUT
D_{na}	D_{nb}	Q_n
L	L	L
L	H	L
H	L	L
H	H	H

H = High voltage level
L = Low voltage level

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F08	4.1 ns	7.1 mA

ORDERING INFORMATION

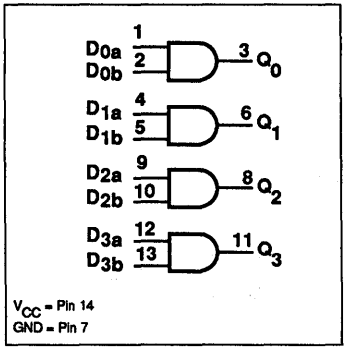
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F08N
14-Pin Plastic SO	N74F08D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

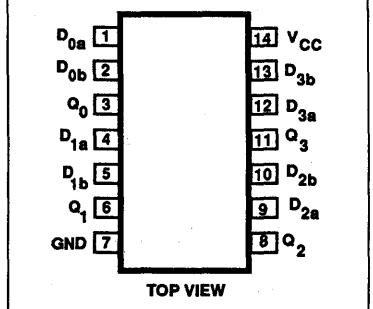
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}	Data inputs	1.0/1.0	20µA/0.6mA
Q_n	Data output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

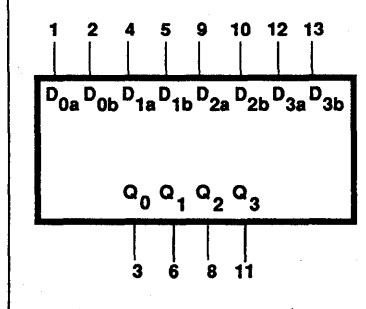
LOGIC DIAGRAM



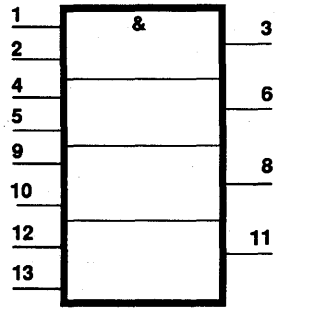
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN}=4.5V		5.5	8.3	mA
		I_{CCL}		V_{IN}=GND		8.6	12.9	mA

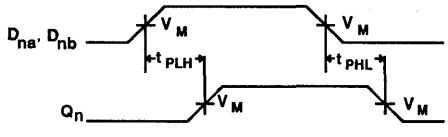
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to Q_n	Waveform 1	3.0 2.5	4.2 4.0	5.6 5.3	3.0 2.5	6.6 6.3	ns

AC WAVEFORMS

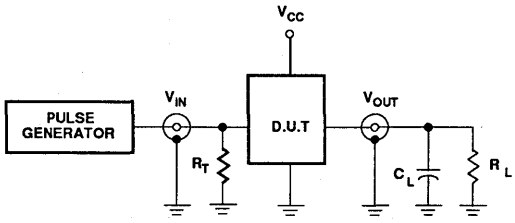


Waveform 1.

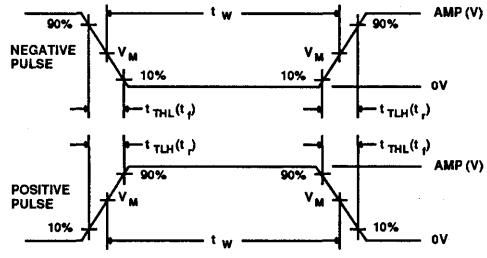
For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST Products

FAST 74F10, 74F11 Gates

74F10 Triple 3-Input NAND Gate
74F11 Triple 3-Input AND Gate

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F10	3.5ns	3.3mA
74F11	4.2ns	5.3mA

ORDERING INFORMATION

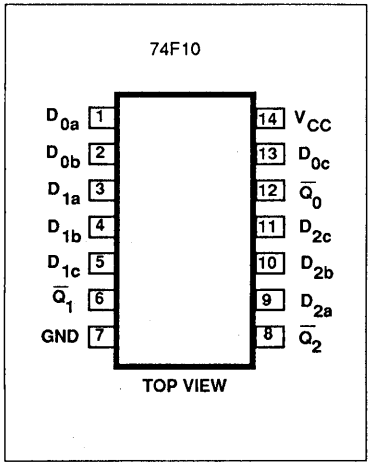
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F10N, N74F11N
14-Pin Plastic SO	N74F10D, N74F11D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

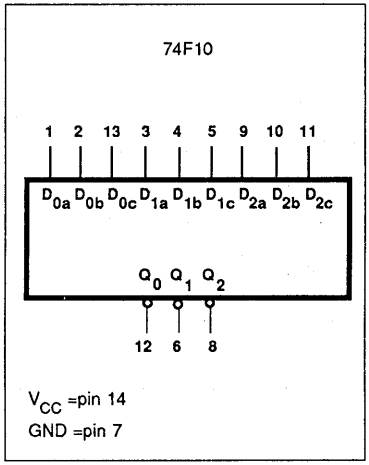
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}, D_{nc}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}_n$	Data output ('F10)	50/33	1.0mA/20mA
Q_n	Data output ('F11)	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

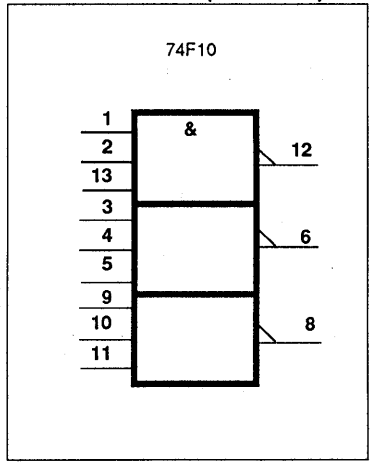
PIN CONFIGURATION



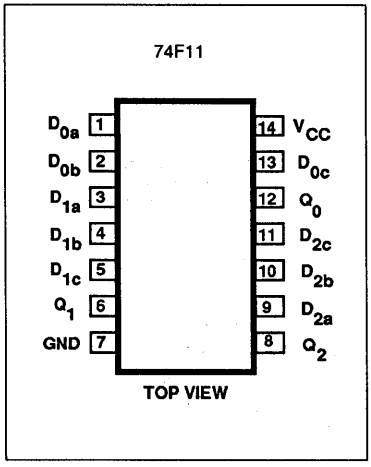
LOGIC SYMBOL



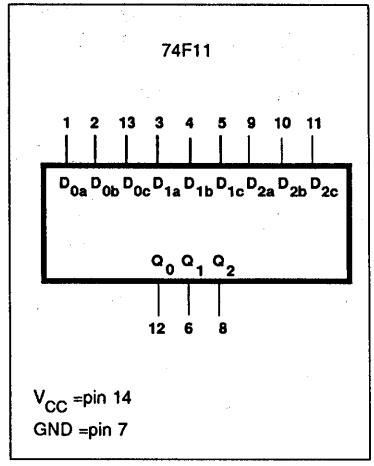
LOGIC SYMBOL(IEEE/IEC)



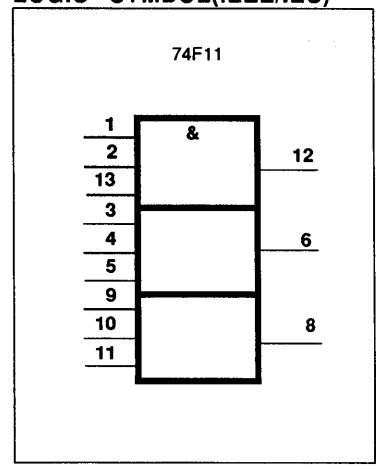
PIN CONFIGURATION



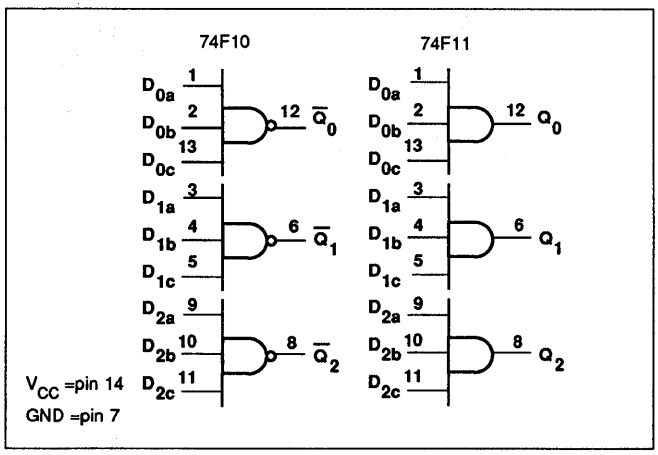
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	
			74F10	74F11
D_{na}	D_{nb}	D_{nc}	$\overline{Q}_n$	Q_n
L	L	L	H	L
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	L	H

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to + 7.0	V
V_{IN}	Input voltage	-0.5 to + 7.0	V
I_{IN}	Input current	-30 to + 5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to + V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to + 70	°C
T_{STG}	Storage temperature	-65 to + 150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
				V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
				V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current			V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	'F10	I_{CCH}	V_{CC} = MAX	V_{IN}=GND		1.8	2.1	mA
			I_{CCL}		V_{IN}=4.5V		6.0	7.7	mA
		'F11	I_{CCH}		V_{IN}=4.5V		4.7	6.2	mA
			I_{CCL}		V_{IN}=GND		7.2	9.7	mA

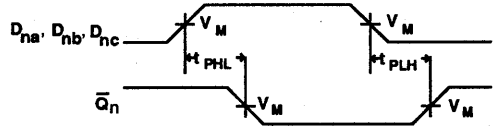
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

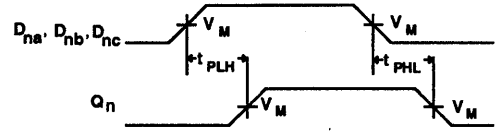
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to $\overline{Q}_n$	74F10	Waveform 1	2.4 1.5	3.7 3.2	5.0 4.3	2.4 1.5	6.0 5.3	ns
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to Q_n	74F11	Waveform 2	3.0 2.5	4.2 4.1	5.6 5.5	3.0 2.5	6.6 6.5	ns

AC WAVEFORMS



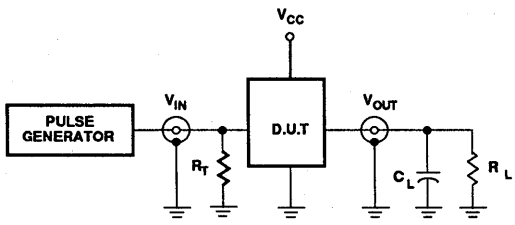
Waveform 1. For Inverting Outputs ('F10)



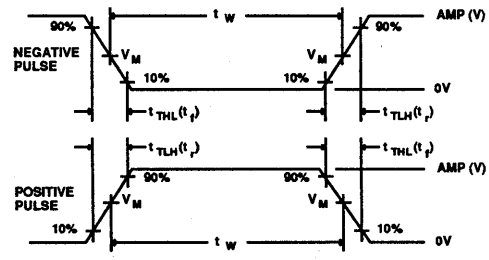
Waveform 2. For Non-Inverting Outputs ('F11)

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F13
Schmitt Trigger

Dual 4-Input NAND Schmitt Trigger

FAST Products

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F13	7.8 ns	5.5 mA

DESCRIPTION

The 74F13 contains two 4-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates. Each circuit contains a 4-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mv) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as three inputs remain at a more positive voltage than VT_{+MAX}, the gate will respond in the transition of the other input as shown in Waveform 1.

ORDERING INFORMATION

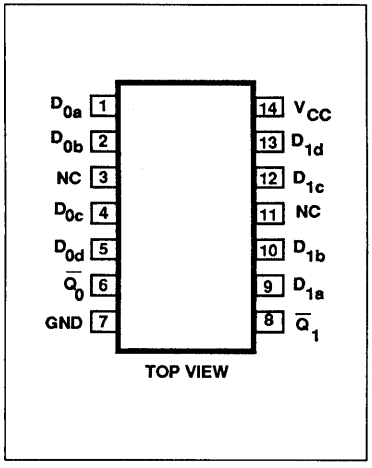
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F13N
14-Pin Plastic SO	N74F13D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}, D_{nc}, D_{nd}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}_0$, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

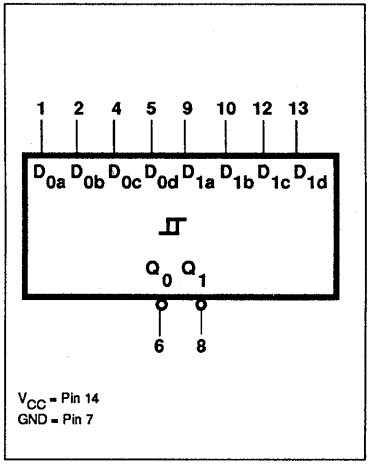
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



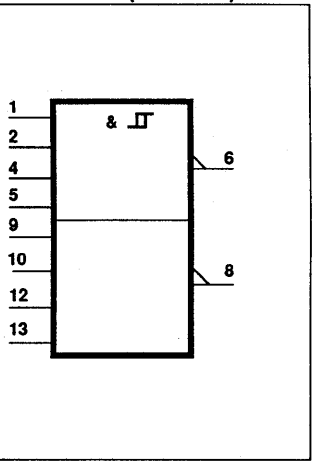
TOP VIEW

LOGIC SYMBOL

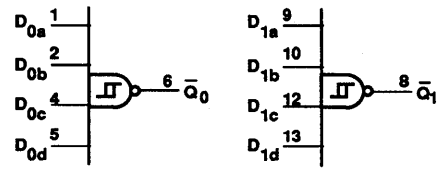


V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = pin 14
GND = pin 7

FUNCTION TABLE

INPUTS				OUTPUT
D_{na}	D_{nb}	D_{na}	D_{nb}	$\overline{Q}_n$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

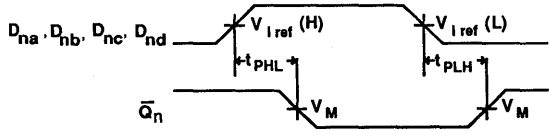
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{T+}	Positive-going threshold		V_{CC} =5.0V		1.5	1.7	2.0	V
V_{T-}	Negative-going threshold		V_{CC} =5.0V		0.7	0.9	1.1	V
ΔV_T	Hysteresis (V_{T+} - V_{T-})		V_{CC} =5.0V		0.4	0.8		V
V_{OH}	High-level output voltage		V_{CC} =MIN,	±10%V_{CC}	2.5			V
			V_I=V_{T-MIN}, I_{OH} =MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} =MIN,	±10%V_{CC}		0.30	0.50	V
			V_I=V_{T+MAX}, I_{OL} =MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_{T+}	Input current at positive-going threshold		V_{CC} =5.0V, V_I = V_{T+}			0		µA
I_{T-}	Input current at negative-going threshold		V_{CC} =5.0V, V_I = V_{T-}			-350		µA
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} =MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} =MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} =MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} =MAX	V_{IN}=GND		4.5	8.5	mA
		I_{CCL}		V_{IN}=4.5V		7.0	10.0	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd} to $\overline{Q}_n$	Waveform 1	4.0 9.0	5.5 11.0	7.0 13.5	4.0 9.0	8.0 13.5	ns

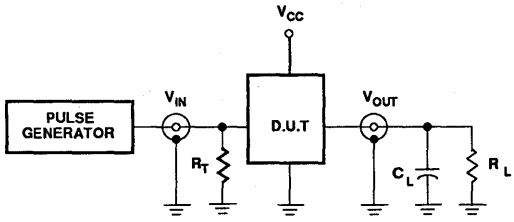
AC WAVEFORMS



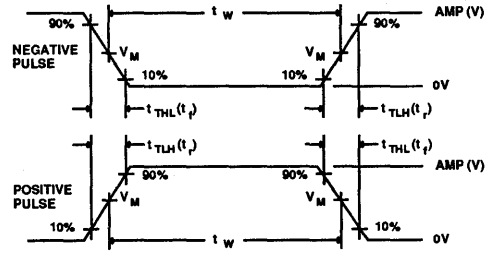
Waveform 1. For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F14
Schmitt Trigger
Hex Inverter Schmitt Trigger

FAST Products

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F14	5.0 ns	18 mA

DESCRIPTION

The 74F14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional inverters. Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive-going and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mv) is determined internally by reisistor ratios and is insensitive to temperature and supply voltage variations.

ORDERING INFORMATION

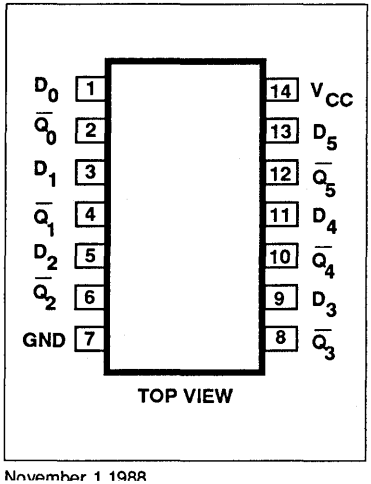
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F14N
14-Pin Plastic SO	N74F14D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_n	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}_n$	Data outputs	50/33	1.0mA/20mA

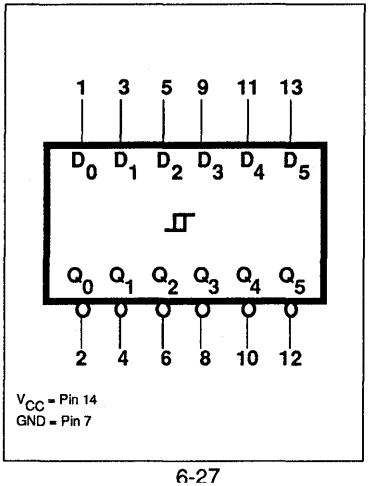
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

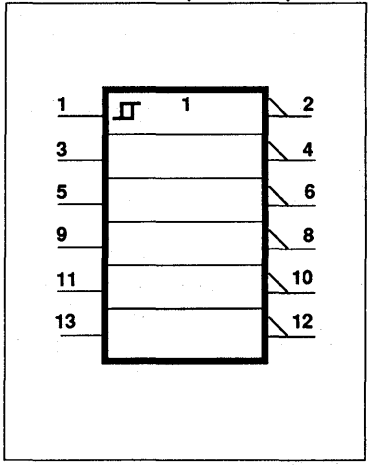


TOP VIEW

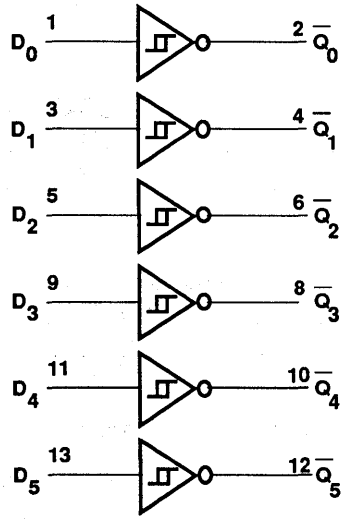
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = pin 14
GND = pin 7

FUNCTION TABLE

INPUT	OUTPUT
D_n	$\overline{Q}_n$
L	H
H	L

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{T+}	Positive-going threshold		V_{CC} =5.0V		1.4	1.7	2.0	V
V_{T-}	Negative-going threshold		V_{CC} =5.0V		0.7	0.9	1.1	V
ΔV_T	Hysteresis (V_{T+} - V_{T-})		V_{CC} =5.0V		0.4	0.8		V
V_{OH}	High-level output voltage		V_{CC} =MIN,	±10%V_{CC}	2.5			V
			V_I=V_{T-MIN}, I_{OH} =MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} =MIN,	±10%V_{CC}		0.30	0.50	V
			V_I=V_{T+MAX}, I_{OL} =MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_{T+}	Input current at positive-going threshold		V_{CC} =5.0V, V_I = V_{T+}			0		µA
I_{T-}	Input current at negative-going threshold		V_{CC} =5.0V, V_I = V_{T-}			-175		µA
I_I	Input current at maximun input voltage		V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} =MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} =MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} =MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} =MAX	V_{IN}=GND		13	22	mA
		I_{CCL}		V_{IN}=4.5V		23	32	mA

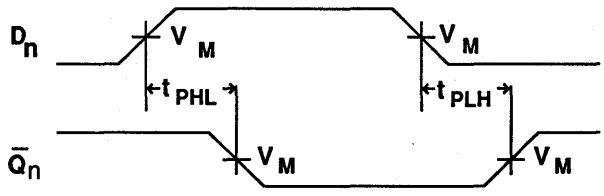
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	Waveform 1	4.0 3.5	6.5 5.0	8.5 6.5	4.0 3.5	9.5 7.0	ns

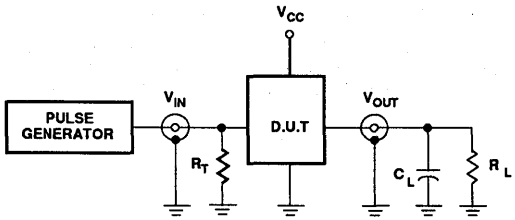
AC WAVEFORMS



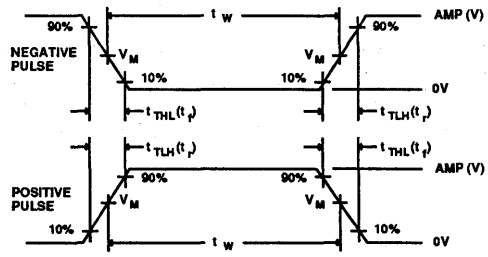
Waveform 1. For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F20 Gate

Dual 4-Input NAND Gate

FAST Products

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F20	3.5 ns	2.2 mA

ORDERING INFORMATION

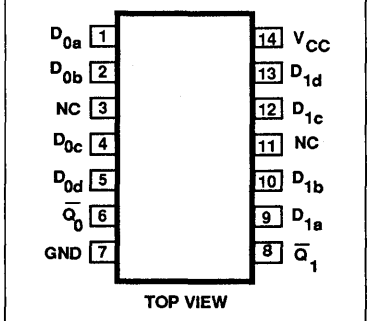
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F20N
14-Pin Plastic SO	N74F20D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}, D_{nc}, D_{nd}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}_0$, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

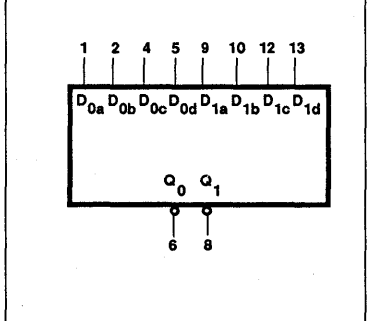
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



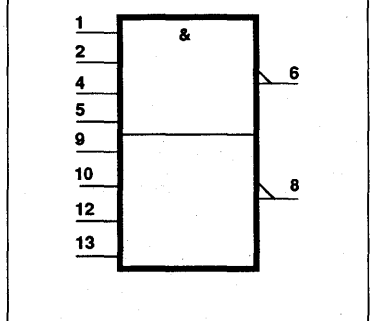
TOP VIEW

LOGIC SYMBOL

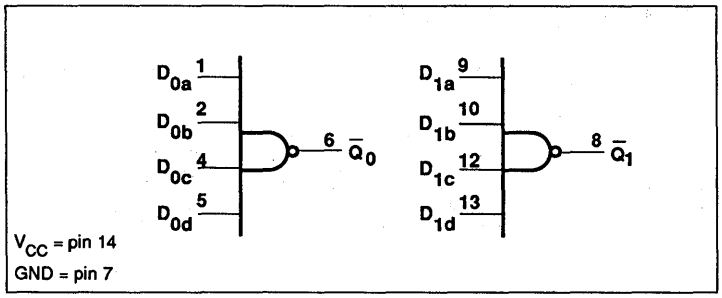


V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT
D_{na}	D_{nb}	D_{nc}	D_{nd}	$\overline{Q}_n$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

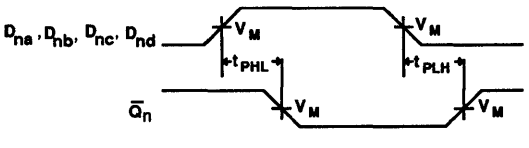
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN}=GND		0.9	1.4	mA
		I_{CCL}		V_{IN}=4.5V		3.4	5.1	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	LIMITS T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd} to $\overline{Q}_n$	Waveform 1	2.4 2.0	3.7 3.2	5.0 4.3	2.4 2.0	6.0 5.3	ns

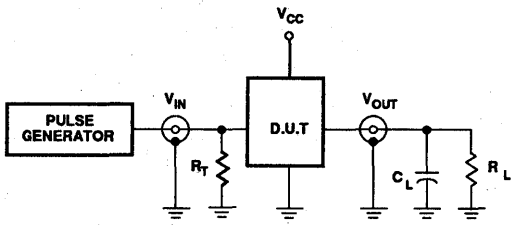
AC WAVEFORMS



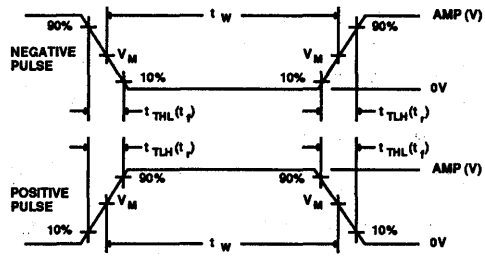
Waveform 1. For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAST 74F27 Gate

Triple 3-Input NOR Gate

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F27	3.0ns	6.5mA

ORDERING INFORMATION

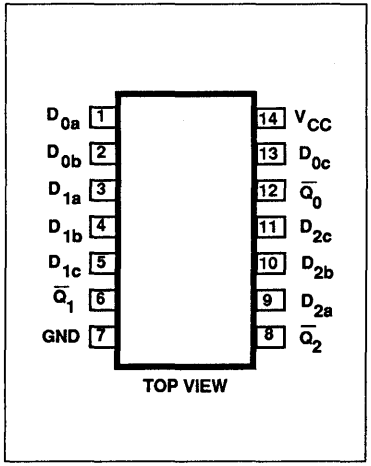
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F27N
14-Pin Plastic SO	N74F27D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

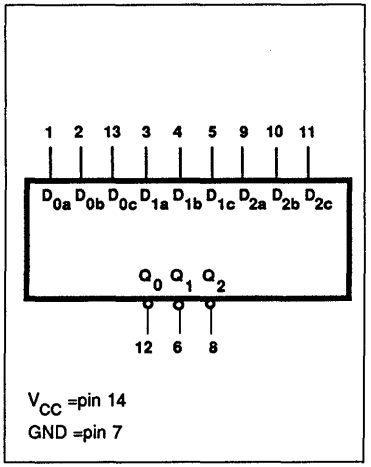
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}, D_{nc}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}_n$	Data output	50/33	1.0mA/20mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

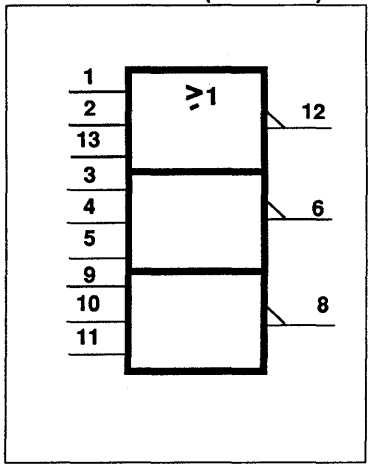
PIN CONFIGURATION



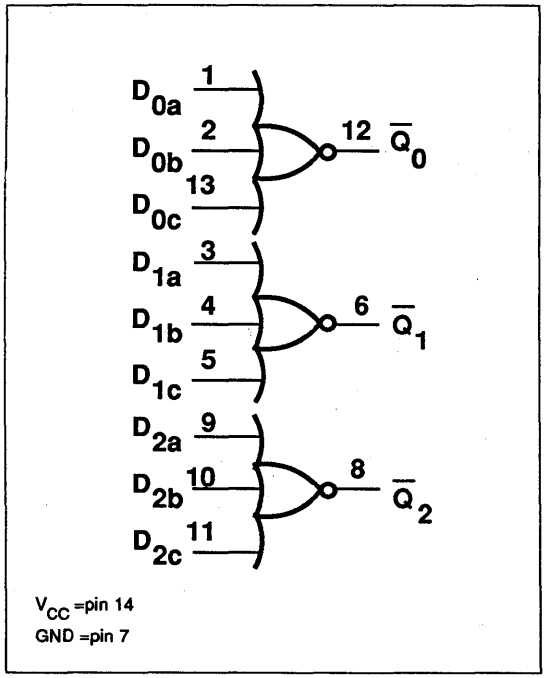
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS
D_{na}	D_{nb}	D_{nc}	$\overline{Q}_n$
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN}=GND		4.0	5.5	mA
		I_{CCL}		V_{IN}=4.5V		8.5	12.0	mA

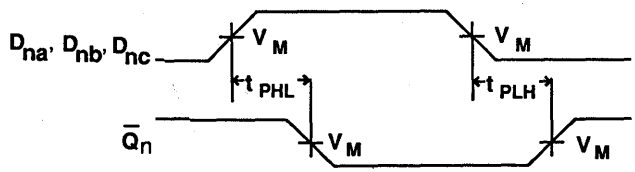
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to $\overline{Q}_n$	Waveform 1	2.0 1.0	3.5 2.5	5.0 4.5	1.5 1.0	5.5 4.5	ns

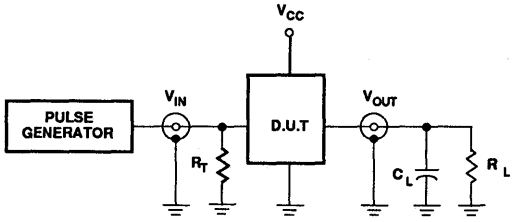
AC WAVEFORMS



Waveform 1. For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



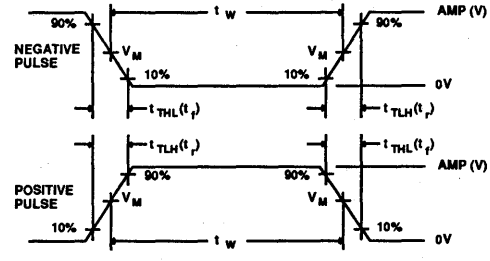
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F30 Gate

8-Input NAND Gate

FAST Products

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F30	3.2 ns	1.7 mA

ORDERING INFORMATION

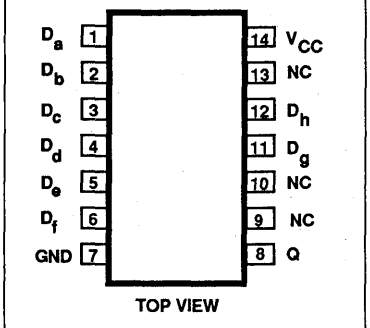
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F30N
14-Pin Plastic SO	N74F30D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_n	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}$	Data output	50/33	1.0mA/20mA

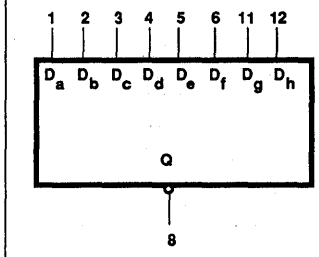
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



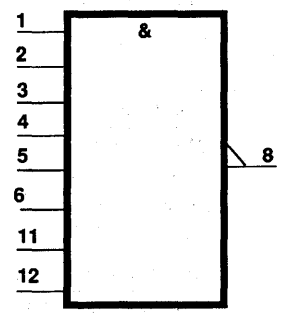
TOP VIEW

LOGIC SYMBOL

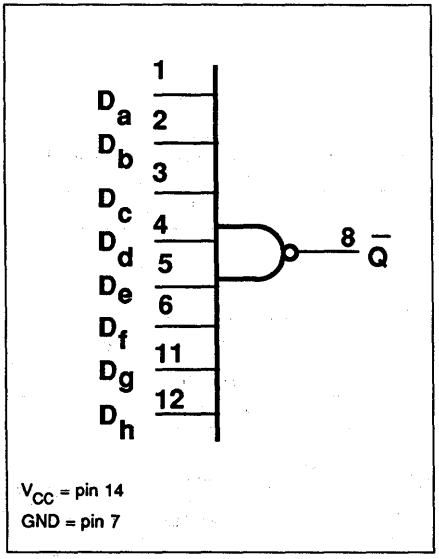


V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = pin 14
GND = pin 7

FUNCTION TABLE

INPUTS								OUTPUT
D_a	D_b	D_c	D_d	D_e	D_f	D_g	D_h	$\overline{Q}$
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

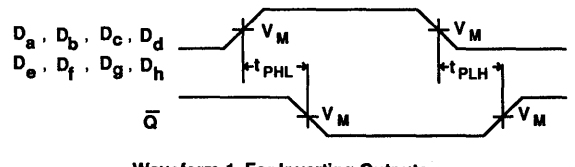
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN}=GND		0.6	1.5	mA
		I_{CCL}		V_{IN}=4.5V		2.8	4.0	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_a, D_b, D_c, D_d, D_e, D_f, D_g, D_h to $\overline{Q}$	Waveform 1	1.5 1.0	3.5 3.0	5.0 4.5	1.5 1.0	5.5 5.0	ns

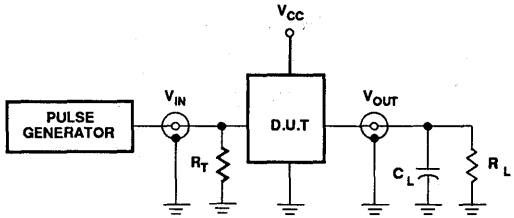
AC WAVEFORMS



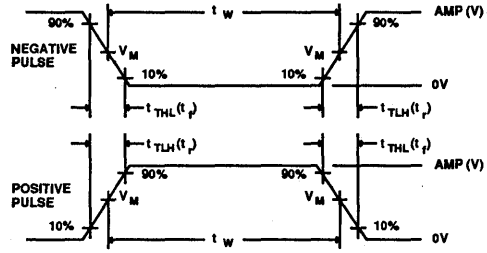
Waveform 1. For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F32 Gate

Quad Two-Input OR Gate

FAST Products

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F32	4.1 ns	8.2 mA

FUNCTION TABLE

INPUTS		OUTPUT
D_{na}	D_{nb}	Q_n
L	L	L
L	H	H
H	L	H
H	H	H

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

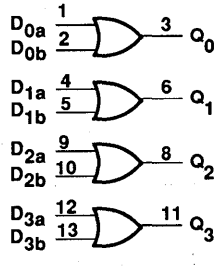
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F32N
14-Pin Plastic SO	N74F32D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

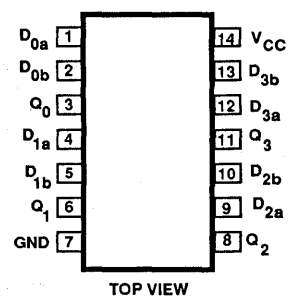
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}	Data inputs	1.0/1.0	20µA/0.6mA
Q_n	Data output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

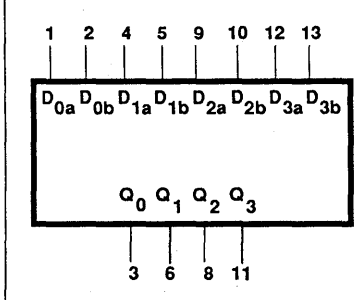
LOGIC DIAGRAM



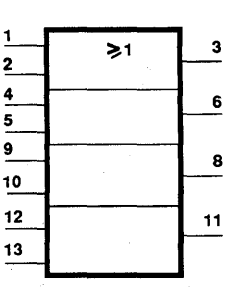
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN}=4.5V		6.1	9.2	mA
		I_{CCL}		V_{IN}=GND		10.3	15.5	mA

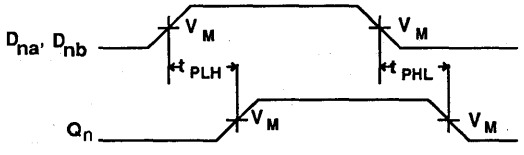
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to Q_n	Waveform 1	3.0 3.0	4.2 4.0	5.6 5.3	3.0 3.0	6.6 6.3	ns

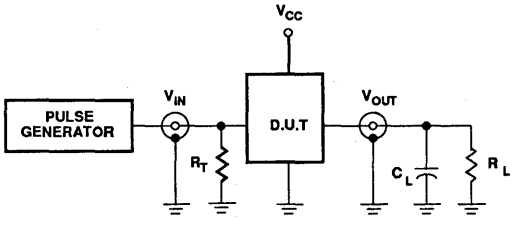
AC WAVEFORMS



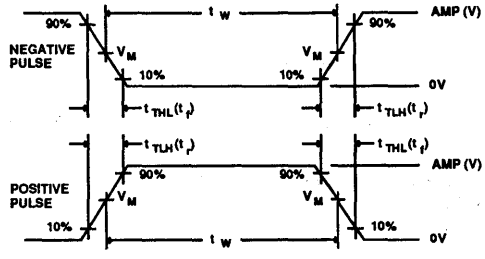
Waveform 1. For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F37 Buffer

Quad 2-Input NAND Buffer

FAST Products

Product Specification

FUNCTION TABLE

INPUTS		OUTPUT
D_{na}	D_{nb}	$\overline{Q}_n$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F37	3.5 ns	13 mA

ORDERING INFORMATION

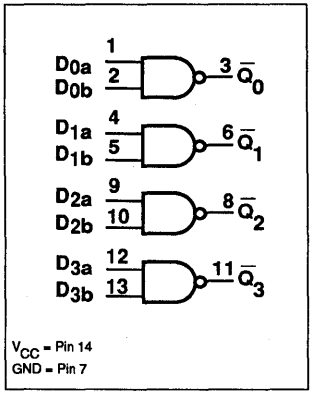
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F37N
14-Pin Plastic SO	N74F37D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

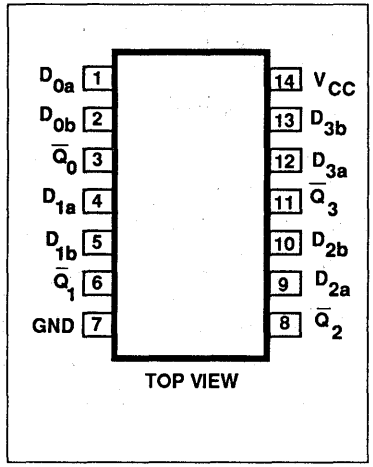
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}	Data inputs	1.0/2.0	20µA/1.2mA
$\overline{Q}_n$	Data output	750/106.6	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

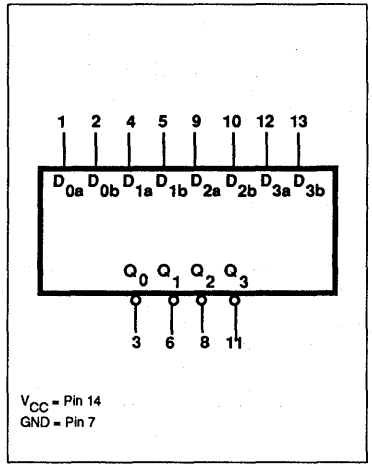
LOGIC DIAGRAM



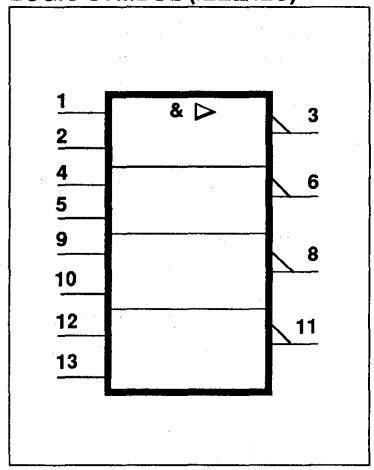
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}= -1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH}= -15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}= MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short circuit output current		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX		V_{IN}= GND		3.0	6.0	mA
		I_{CCL}			V_{IN}= 4.5V		23	33	mA

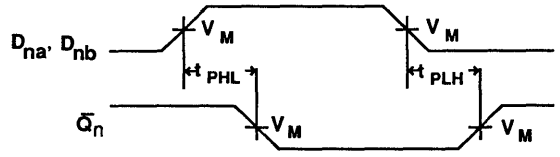
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to $\overline{Q}_n$	Waveform 1	2.5 1.5	3.5 2.5	5.5 4.5	2.0 1.5	6.5 5.0	ns

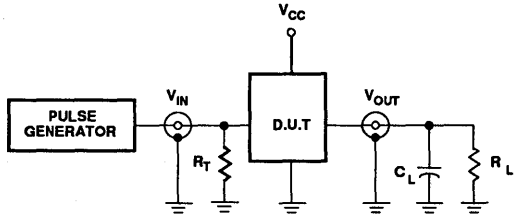
AC WAVEFORMS



Waveform 1.For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



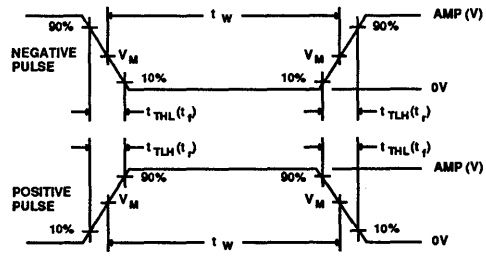
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F38 Buffer

Quad Two-Input NAND Buffer (Open Collector)

FAST Products

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F38	7.0 ns	13 mA

ORDERING INFORMATION

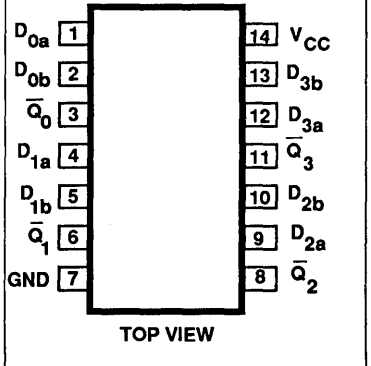
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F38N
14-Pin Plastic SO	N74F38D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}	Data inputs	1.0/2.0	20μA/1.2mA
Q_n	Data outputs	OC/106.7	OC/64mA

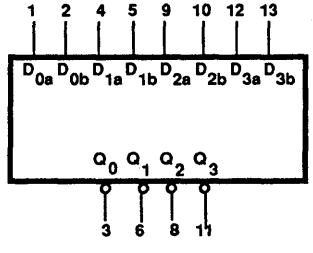
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC = Open Collector

PIN CONFIGURATION



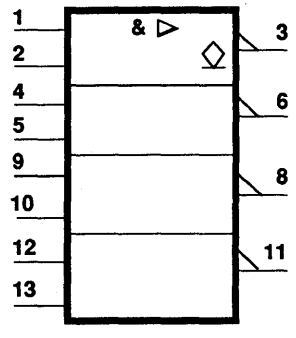
TOP VIEW

LOGIC SYMBOL

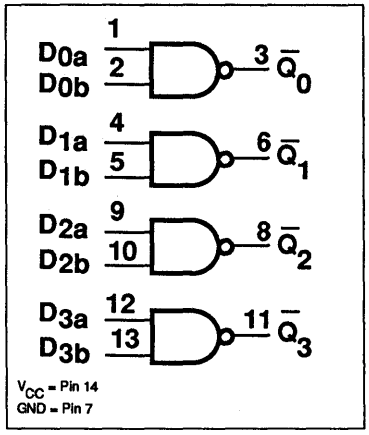


V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
D_{na}	D_{nb}	$\overline{Q}_n$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

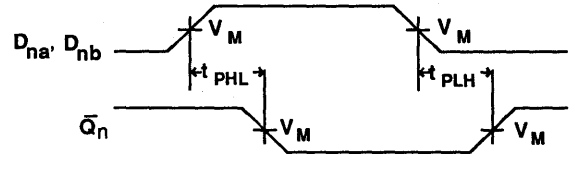
SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OL}	Low-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}= 48mA	±10%V_{CC}		.38	.55	V
				I_{OL}= 64mA	±5%V_{CC}		.42	.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-1.2	mA
I_{CC}	Supply current [total]	I_{CCH}	V_{CC} = MAX		V_{IN} =GND		4.0	7.0	mA
		I_{CCL}			V_{IN} = 4.5V		22	30	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to $\overline{Q}_n$	Waveform 1	7.5 1.5	10.0 3.0	12.5 5.0	7.5 1.5	13.0 5.5	ns

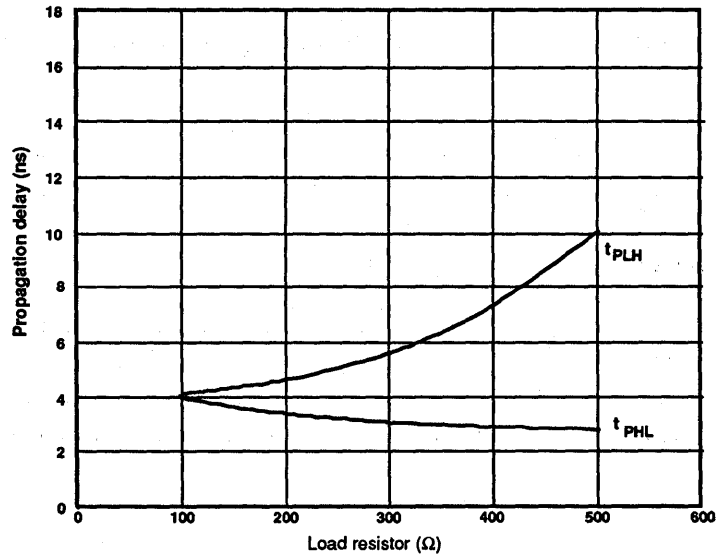
AC WAVEFORMS



Waveform 1.For Inverting Outputs

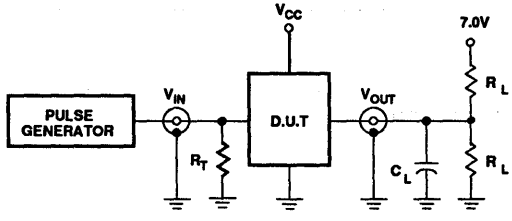
NOTE: For all waveforms, V_M = 1.5V.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

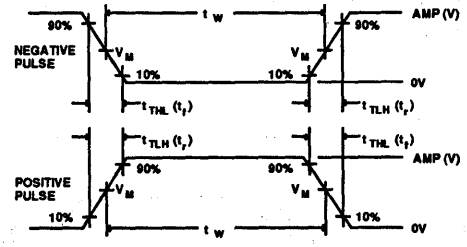


NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F40 Buffer

Dual 4-Input NAND Buffer

FAST Products

Product Specification

FUNCTION TABLE

INPUTS				OUTPUT
D_{na}	D_{nb}	D_{nc}	D_{nd}	$\overline{Q}_n$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	X	H
H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F40	3.5 ns	6 mA

ORDERING INFORMATION

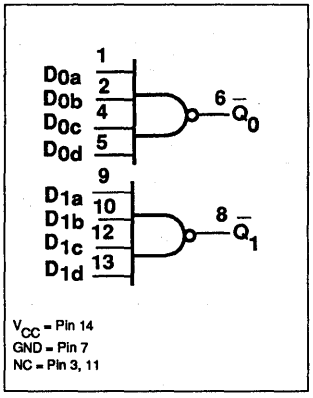
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F40N
14-Pin Plastic SO	N74F40D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

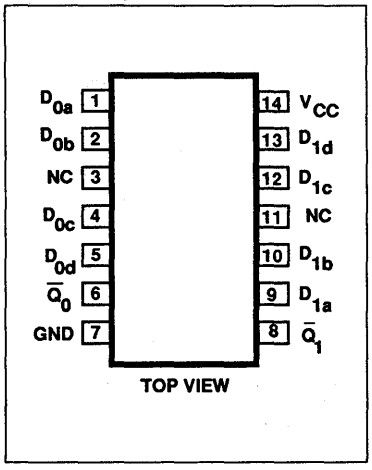
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}, D_{nc}, D_{nd}	Data inputs	1.0/2.0	20µA/1.2mA
$\overline{Q}_0$, $\overline{Q}_1$	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

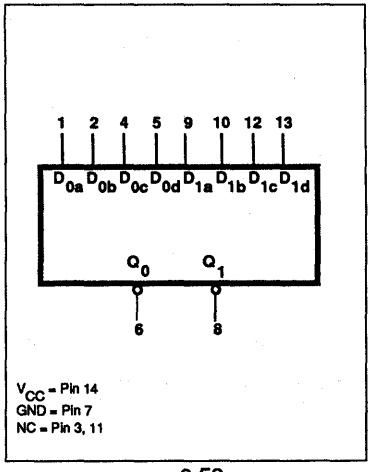
LOGIC DIAGRAM



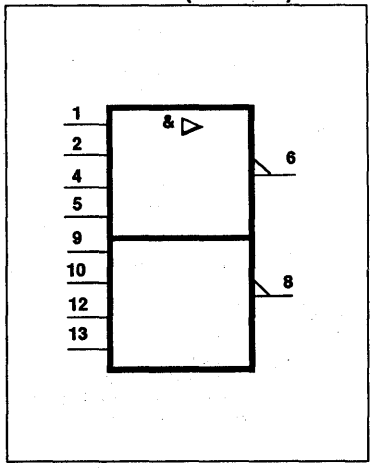
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = -15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-1.2	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX		V_{IN} = GND		1.75	4.0	mA
		I_{CCL}			V_{IN} = 4.5V		11	17	mA

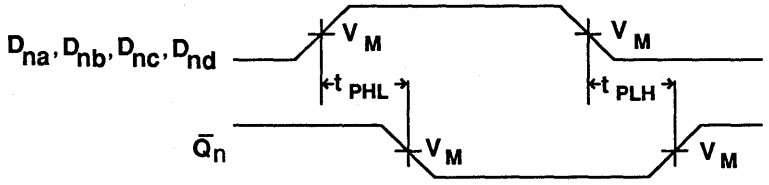
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd} to $\overline{Q}_n$	Waveform 1	2.0 1.5	4.0 3.0	6.0 5.0	1.5 1.0	7.0 5.5	ns

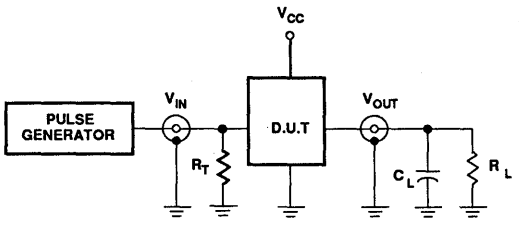
AC WAVEFORMS



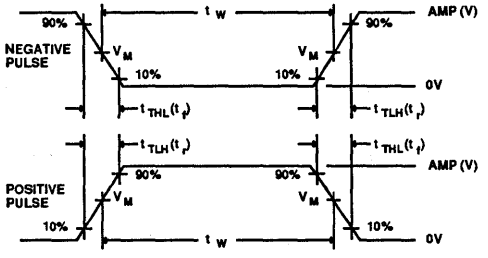
Waveform 1. For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAST 74F51 Gate

Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-Invert Gate

FAST Products

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F51	3.0 ns	3.5 mA

ORDERING INFORMATION

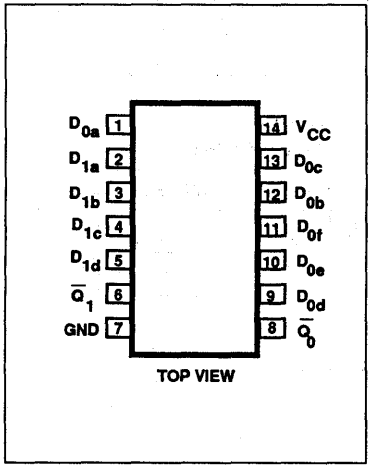
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F51N
14-Pin Plastic SO	N74F51D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

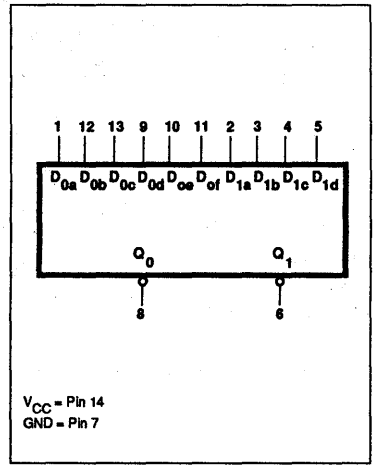
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}, D_{nc}, D_{nd}, D_{ne}, D_{nf}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}_0$, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

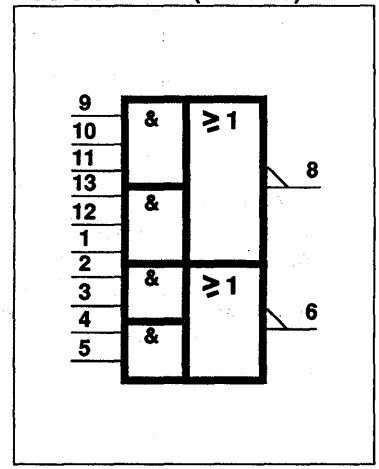
PIN CONFIGURATION



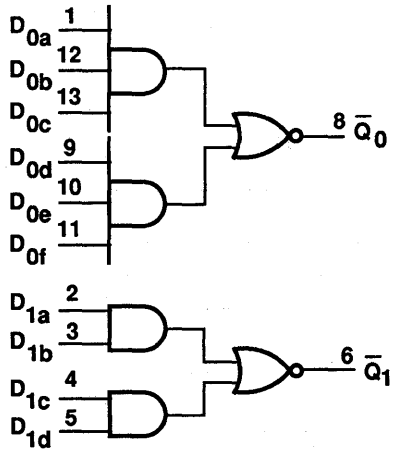
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = pin 14
GND = pin 7

FUNCTION TABLE for 3-Input Gates

INPUTS						OUTPUT
D_{0a}	D_{0b}	D_{0c}	D_{0d}	D_{0e}	D_{0f}	$\overline{Q}_0$
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE for 2-Input Gates

INPUTS				OUTPUT
D_{1a}	D_{1b}	D_{1c}	D_{1d}	$\overline{Q}_1$
H	H	X	X	L
X	X	H	H	L
All other combinations				H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

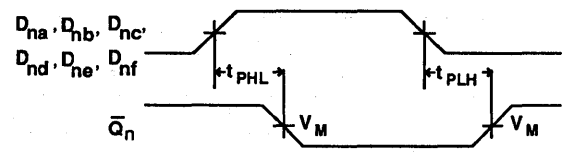
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN}=GND		1.8	3.0	mA
		I_{CCL}		V_{IN}=4.5V		5.5	7.5	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS: T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	LIMITS: T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH}	Propagation delay	Waveform 1	2.0	3.5	5.5	1.5	6.5	ns
t_{PHL}	D_{na}, D_{nb}, D_{nc}, D_{nd}, D_{ne}, D_{nf} to $\overline{Q}_n$		1.0	2.5	4.0	1.0	4.5	

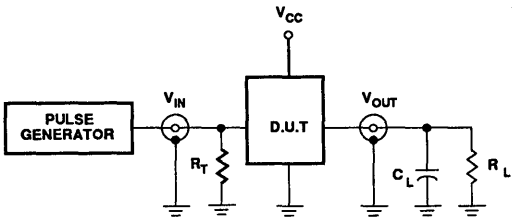
AC WAVEFORMS



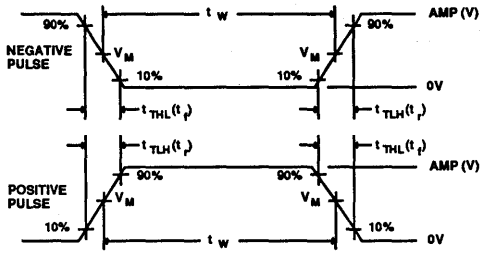
Waveform 1. For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAST 74F64 Gate

Four-Two-Three-Two-Input AND-OR-Invert Gate

FAST Products

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F64	4.0 ns	2.5 mA

ORDERING INFORMATION

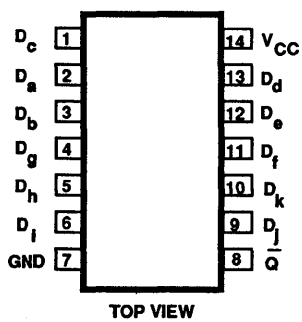
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F64N
14-Pin Plastic SO	N74F64D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

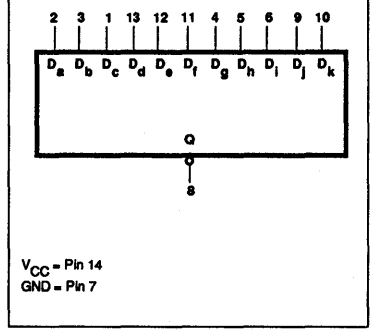
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_n	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}$	Data output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

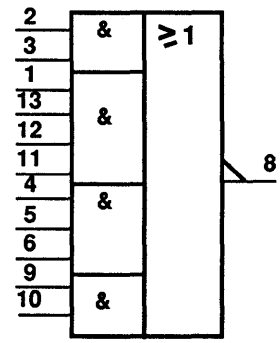
PIN CONFIGURATION



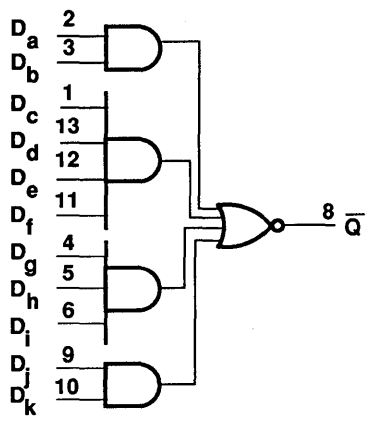
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = pin 14
GND = pin 7

FUNCTION TABLE

INPUTS											OUTPUT
D_a	D_b	D_c	D_d	D_e	D_f	D_g	D_h	D_i	D_j	D_k	$\overline{Q}$
H	H	H	X	X	X	X	X	X	X	X	L
X	X	H	H	H	H	X	X	X	X	X	L
X	X	X	X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	X	X	X	H	H	L
All other combinations											H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

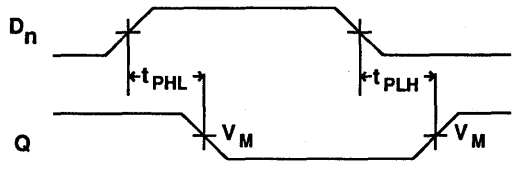
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN}=GND		1.9	2.8	mA
		I_{CCL}		V_{IN}=4.5V		3.1	4.7	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	LIMITS T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH}	Propagation delay D_n to $\overline{Q}$	Waveform 1	2.5	4.6	6.0	2.5	7.0	ns
t_{PHL}			2.0	3.2	4.5	2.0	5.5	

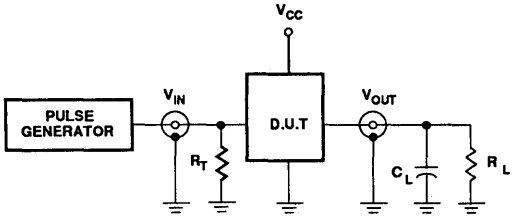
AC WAVEFORMS



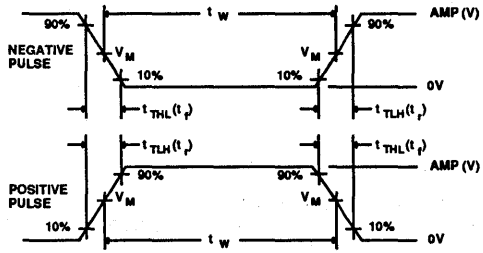
Waveform 1. For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F74 FLIP-FLOP

Dual D-Type Flip-Flop

FAST Products

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F74	125 MHz	11.5mA

DESCRIPTION

The 74F74 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also true and complementary outputs.

Set (SD) and Reset (RD) are asynchronous active-Low inputs and operate independently of the Clock (CP) input.

Set (SD) and Reset (RD) are synchronously

active Low inputs and operate independently of the clock (CP). When Set and Reset are inactive (High), Data at the D input is transferred to the Q and $\overline{Q}$ outputs on the Low-to-High transition of the Clock. Data must be stable just one setup time prior to the Low-to-High transition of the clock for predictable operation.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D input may be changed without affecting the levels of the output.

ORDERING INFORMATION

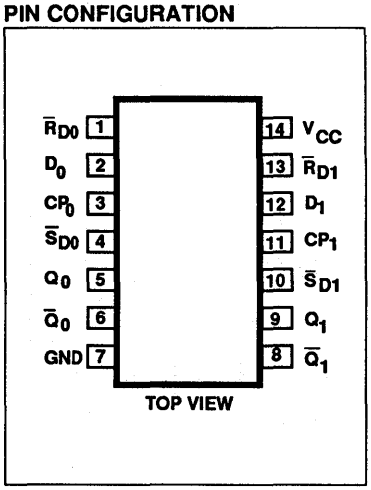
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F74N
14-Pin Plastic SO	N74F74D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

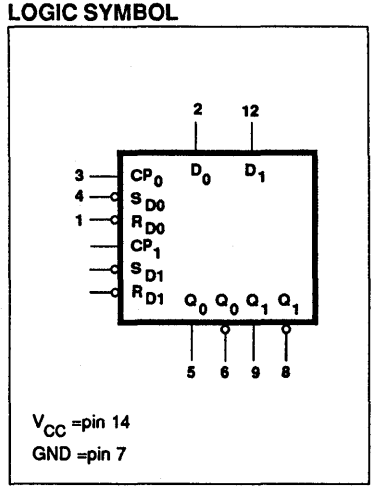
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0, D_1	Data inputs	1.0/1.0	20µA/0.6mA
CP_0, CP_1	Clock inputs (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{S}_{D0}$, $\overline{S}_{D1}$	Set inputs (active Low)	1.0/3.0	20µA/1.8mA
$\overline{R}_{D0}$, $\overline{R}_{D1}$	Reset inputs (active Low)	1.0/3.0	20µA/1.8mA
Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

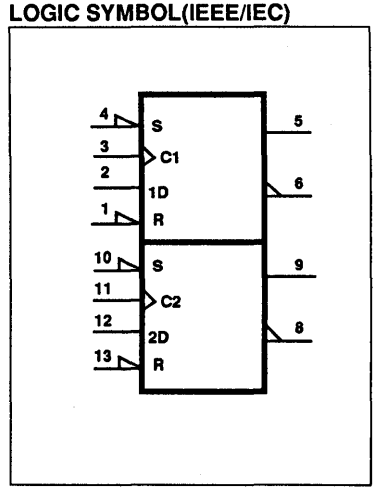
PIN CONFIGURATION



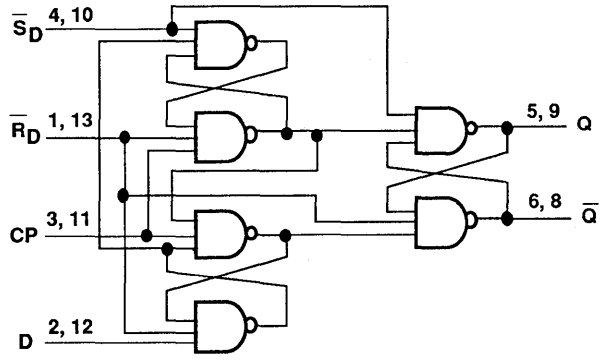
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} =pin 14
GND =pin 7

FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$	
L	H	X	X	H	L	Asynchronous Set
H	L	X	X	L	H	Asynchronous Reset
L	L	X	X	H	H	Undetermined*
H	H	↑	h	H	L	Load "1"
H	H	↑	l	L	H	Load "0"
H	H	L	X	NC	NC	Hold

H = High voltage level
h = High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
NC =No change from the previous setup
* =This setup is unstable and will change when either Set or Reset return to the High level.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} =MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} =MAX	±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	D_n, CP_n	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{S}_{Dn}$, $\overline{R}_{Dn}$					-1.8	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			11.5	16	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs High in turn.

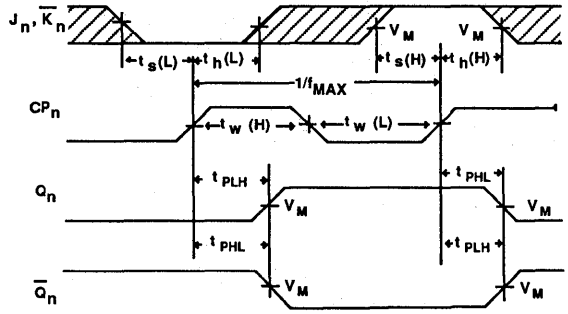
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveform 1	3.8 4.4	5.3 6.2	6.8 8.0	3.8 4.4	7.8 9.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_{Dn}$ to Q_n or $\overline{Q}_n$	Waveform 2	3.2 3.5	4.6 7.0	6.1 9.0	3.2 3.5	7.1 10.5	ns

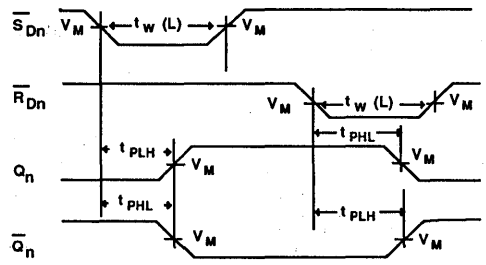
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 1	2.0 3.0			2.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 1	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	$\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ Pulse width, Low	Waveform 2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to CP	Waveform 3	2.0			2.0		ns

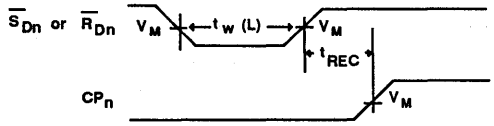
AC WAVEFORMS



Waveform 1. Propagation Delay For data to output, data setup time and hold times, clock width, and maximum clock frequency



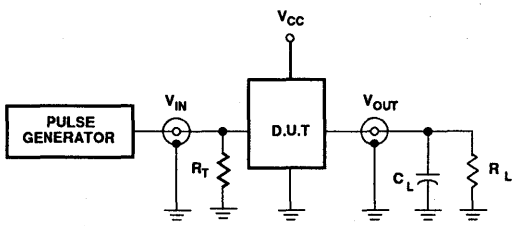
Waveform 2. Propagation Delay for set and reset to output, set and reset pulse width



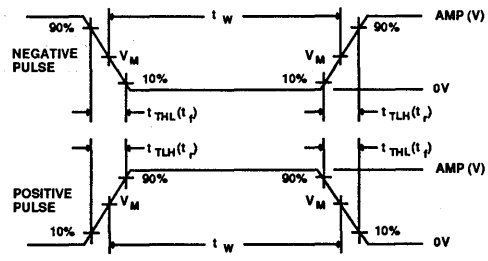
Waveform 3. Reset pulse width, and recovery time for reset to clock

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F83
4-Bit Adder

FAST Products

Product Specification

FEATURES

- **High speed 4-bit binary addition**
- **Cascadable in 4-bit increments**
- **Functional equivalent to 'F283 but with center power pins**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F83	7.0ns	36mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F83N
16-Pin Plastic SOL	N74F83D

DESCRIPTION

The 74F83 adds two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the sum outputs (Σ_0-Σ_3) and the outgoing carry (C_{OUT}) according to the equation:

$C_{IN} + 2^0(A_0 + B_0) + 2^1(A_1 + B_1) + 2^2(A_2 + B_2) + 2^3(A_3 + B_3)$

$= \Sigma_0 + 2\Sigma_1 + 4\Sigma_2 + 8\Sigma_3 + 16C_{OUT}$

where (+) = plus

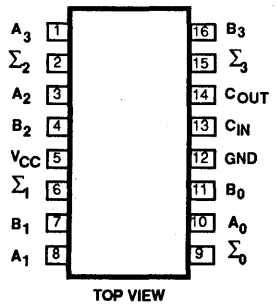
Due to the symmetry of the binary add function, the 'F83 can be used with either all active-High operands (positive logic) or with all active-Low operands (negative logic). See Function Table. With active-High inputs, C_{IN} cannot be left open; it must be held Low when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus A_0, B_0, C_{IN} can arbitrarily be assigned to pins 10, 11, 13, etc.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	A operand inputs	1.0/2.0	20µA/1.2mA
B_0 - B_3	B operand inputs	1.0/2.0	20µA/1.2mA
C_{IN}	Carry input	1.0/1.0	20µA/0.6mA
C_{OUT}	Carry output	50/33	1.0mA/20mA
Σ_0 - Σ_3	Sum outputs	50/33	1.0mA/20mA

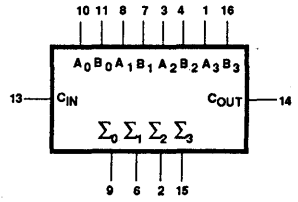
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



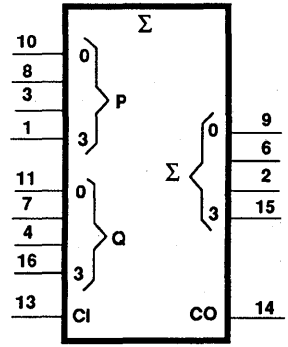
TOP VIEW

LOGIC SYMBOL

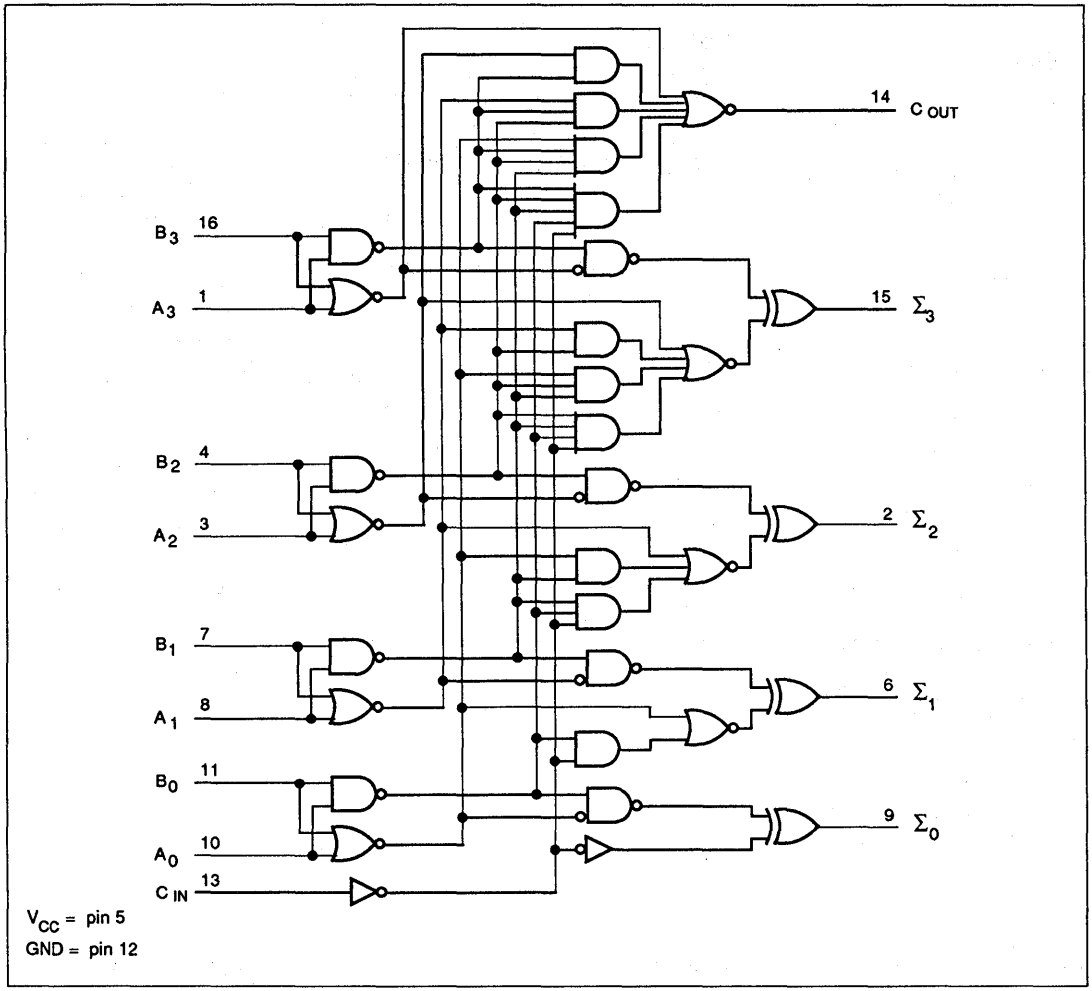


V_{CC} = Pin 5
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

PINS	C_{IN}	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	Σ_0	Σ_1	Σ_2	Σ_3	C_{OUT}
Logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active High	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active Low	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Example:
1001
1010
10011
(10+9=19)
(carry+5+6=12)

H = High voltage level
L = Low voltage level

Due to pin limitations, the intermediate carries of the 'F83 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage.

Figure a shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A_3, B_3) Low makes Σ_3 dependent only on, and equal to, the carry from the third adder.

Using somewhat the same principle, Figure b shows a way of dividing the 'F83 into a 2-bit and a 1-bit adder. The third stage adder (A_2, B_2, Σ_2) is used as means of getting a carry (C_{10}) signal into the fourth stage (via A_2 and B_2) and bringing out the carry from the second stage on Σ_2. Note that as long as A_2 and B_2 are the same, whether High or Low, they do do not influence Σ_2. Similarly, when A_2 and B_2 are the same, the carry into the third stage does not influence the carry out of the third stage.

Figure c shows a method of implementing a 5-input encoder where the inputs are equally weighted. The outputs Σ_0, Σ_1 and Σ_2 present a binary number equal to the number of inputs I_0 - I_4 that are true.

Figure d shows one method of implementing a 5-input majority gate. When three or more of the inputs I_0 - I_4 are true, the output M_4 is true.

APPLICATIONS

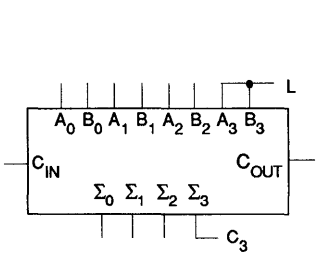


Figure a 3-bit adder

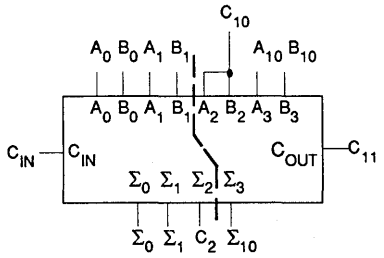


Figure b 2-bit and 1-bit adder

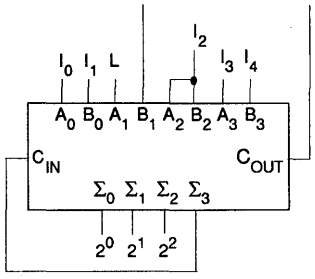


Figure c 5-input Encoder

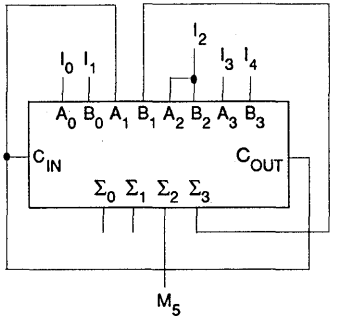


Figure d 5-input majority Gate

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	C_{IN} only	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		A_n, B_n					-1.2	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			36	55	mA

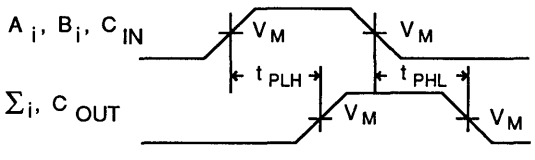
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

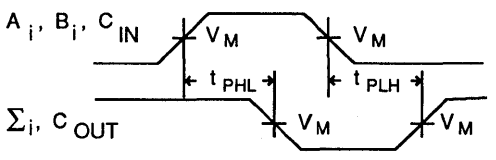
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_i	Waveform 1, 2	3.5 4.0	7.0 7.0	9.5 9.5	3.0 3.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to Σ_i	Waveform 1, 2	3.5 3.5	7.0 7.0	9.5 9.5	2.5 3.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to C_{OUT}	Waveform 2	3.5 3.0	5.7 5.4	7.5 7.0	3.5 2.5	8.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to C_{OUT}	Waveform 1, 2	3.5 2.5	5.7 5.3	7.5 7.0	3.0 2.5	8.5 8.0	ns

AC WAVEFORMS



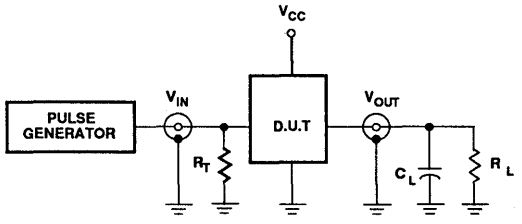
Waveform 1. Propagation Delay
Operands and Carry inputs to Outputs



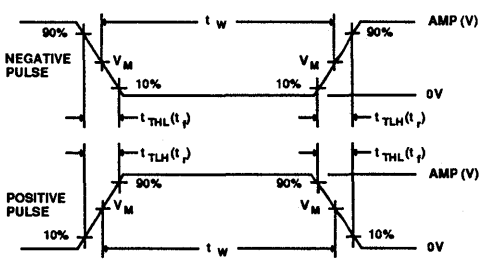
Waveform 2. Propagation Delay
Operands and Carry inputs to Outputs

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F85
Comparator

FAST Products

4-Bit Magnitude Comparator

Product Specification

FEATURES

- **High-impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Magnitude comparison of any binary words**
- **Serial of parallel expansion without extra gating**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F85	7.0ns	40mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F85N
16-Pin Plastic SO	N74F85D

DESCRIPTION

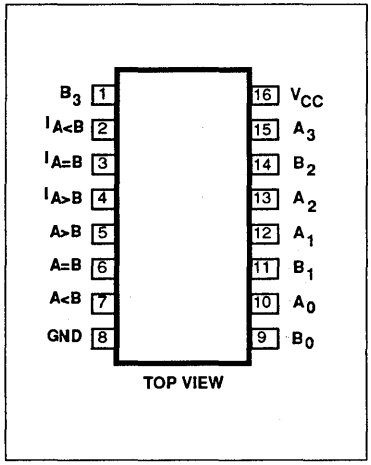
The 74F85 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted (A_0-A_3) and (B_0-B_3) where A_3 and B_3 are the most significant bits. The operation of the 74F85 is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exists in the parallel expansion scheme. The expansion inputs $I_{A>B}$, $I_{A=B}$ and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the A>B, A=B and A<B outputs of the least significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$ and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation the expansion inputs of the least significant word should be tied as follows: $I_{A>B}$=Low, $I_{A=B}$=High and $I_{A<B}$=Low.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

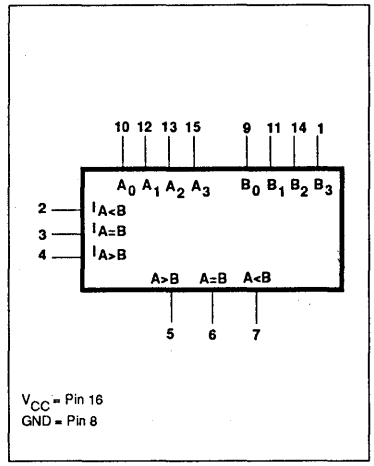
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_3	Comparing inputs	1.0/0.033	20μA/20μA
B_0- B_3	Comparing inputs	1.0/0.033	20μA/20μA
$I_{A<B}$, $I_{A=B}$, $I_{A>B}$	Expansion inputs (active Low)	1.0/0.033	20μA/20μA
A<B, A=B, A>B	Data outputs (active Low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

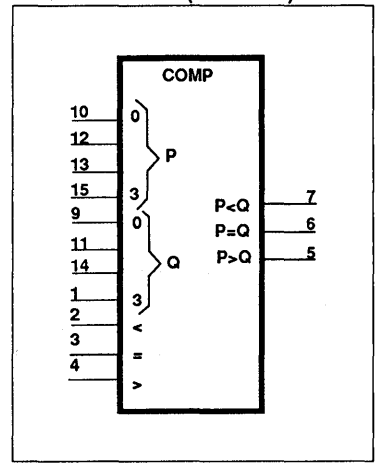
PIN CONFIGURATION



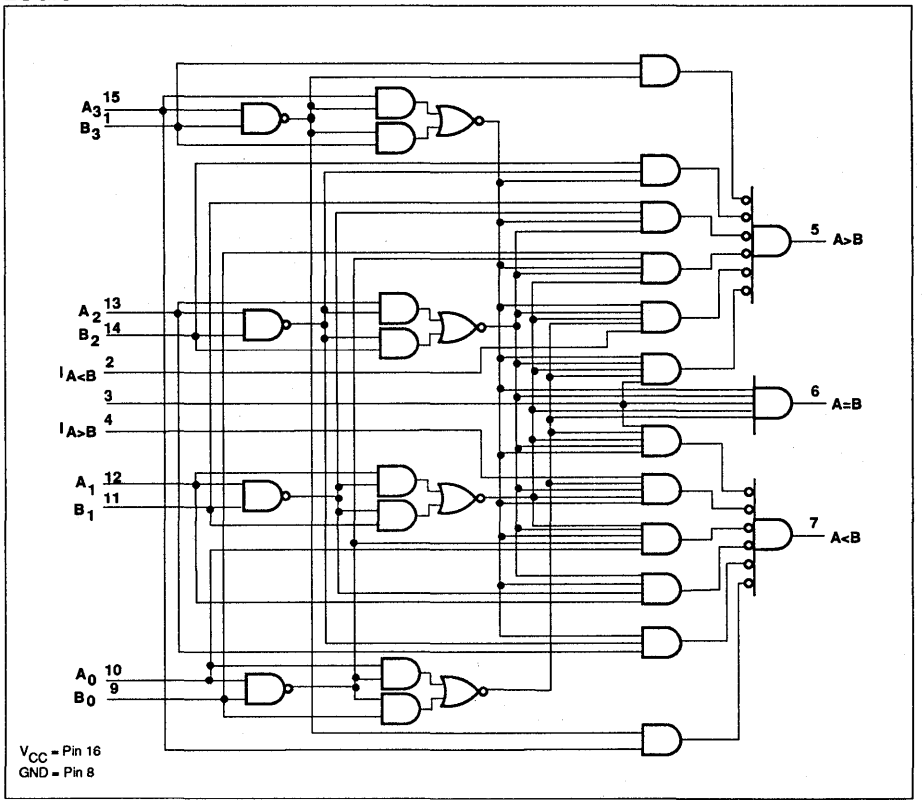
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

COMPARING INPUTS				EXPANSION INPUTS			OUTPUTS		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A>B	A<B	A=B
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

APPLICATION

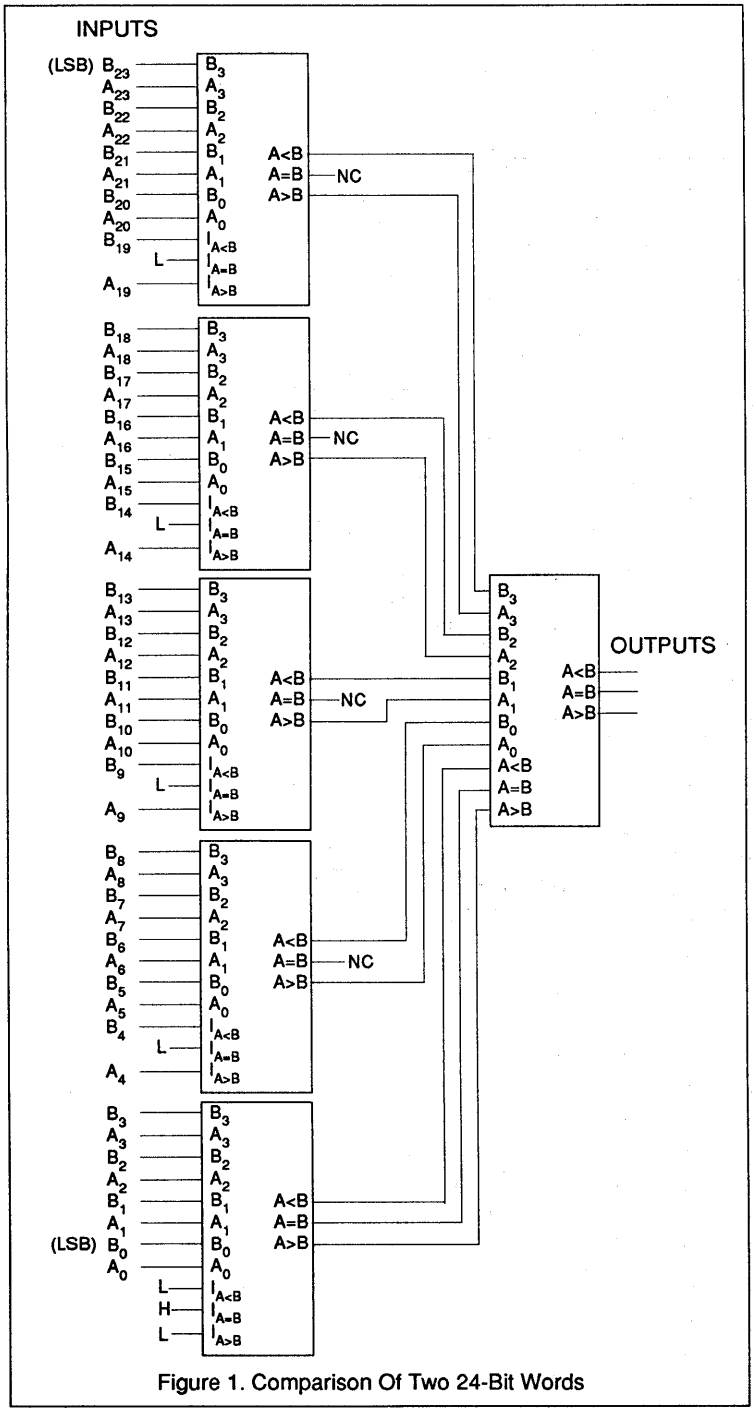


Figure 1. Comparison Of Two 24-Bit Words

The parallel expansion scheme shown in Figure 1 demonstrates the most efficient general use of these comparators. The expansion inputs can be used as a fifth input bit position except on the least significant device which must be connected as in the serial scheme.The expansion inputs used by labeling $I_{A>B}$ as an "A" input, $I_{A<B}$ as an "B" input and setting $I_{A=B}$=Low. The 'F85 can be used as 5-bit comparator only when the outputs are used to drive the (A_0-A_3) and (B_0-B_3) inputs of another 'F85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

Table1

WORD LENGTH	NUMBER OF PACKAGES	TYPICAL SPEEDS 74F
1-4 Bits	1	12ns
5-24 Bits	2-6	22ns
25-120 Bits	8-31	34ns

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN}=GND		36	50	mA
		I_{CCL}		A_n=B_n=$I_{A=B}$=GND, $I_{A>B}$=$I_{A<B}$=4.5V		40	54	mA

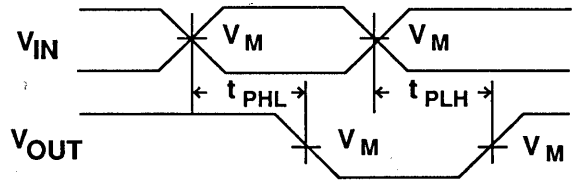
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B to A<B, A>B	Waveform 1 3 logic levels	6.0 7.0	8.5 9.5	11.0 14.0	5.5 6.5	13.0 15.5	ns
t_{PLH} t_{PHL}	Propagation delay A or B to A=B	Waveform 1 4 logic levels	6.5 7.0	9.0 9.5	11.5 14.0	6.0 6.5	14.0 14.5	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A<B}$ and $I_{A=B}$ to A>B	Waveform 1 1 logic level	3.0 3.0	5.0 6.0	7.5 9.0	2.5 2.5	9.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A=B}$ to A=B	Waveform 1 2 logic levels	2.5 3.5	4.5 7.5	7.0 10.0	2.0 2.5	9.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A>B}$ and $I_{A=B}$ to A<B	Waveform 1 1 logic level	3.0 3.0	5.0 6.0	8.0 9.0	3.0 2.0	9.5 9.5	ns

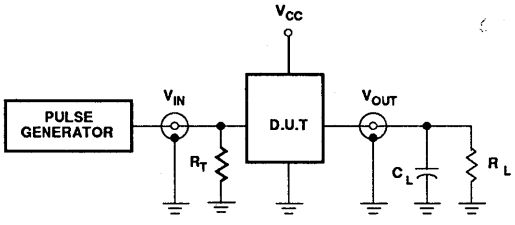
AC WAVEFORMS



Waveform 1. Propagation Delay Input To Output

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



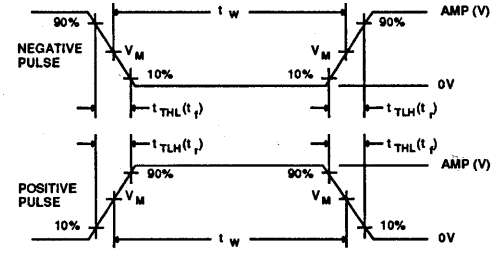
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F86 Gate

Quad Two-Input Exclusive-OR Gate

FAST Products

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F86	4.3 ns	16.5 mA

FUNCTION TABLE

INPUTS		OUTPUT
D_{na}	D_{nb}	Q_n
L	L	L
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

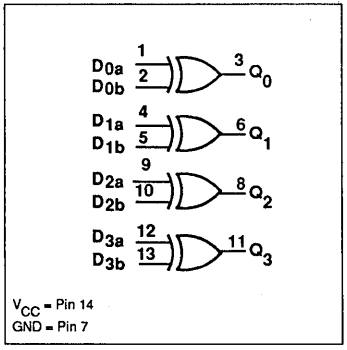
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F86N
14-Pin Plastic SO	N74F86D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

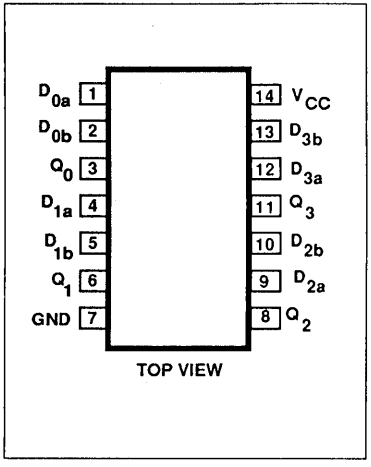
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}	Data inputs	1.0/1.0	20µA/0.6mA
Q_n	Data output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

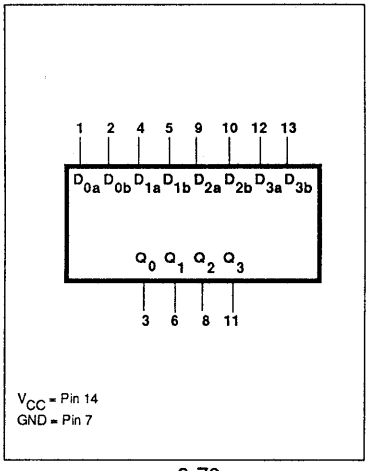
LOGIC DIAGRAM



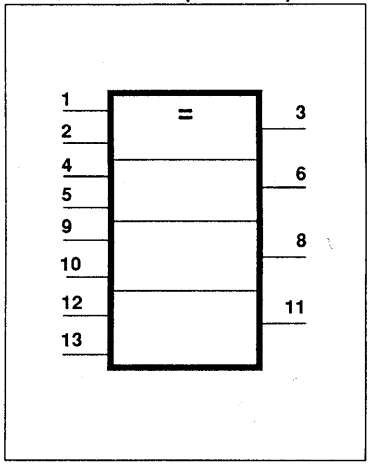
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	D_{0a}=GND, D_{0b}=4.5V		15	23	mA
		I_{CCL}		V_{IN}=4.5V		18	28	mA

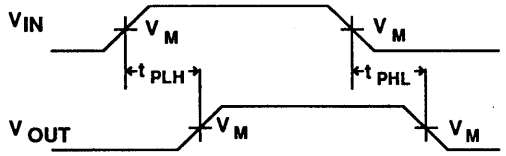
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

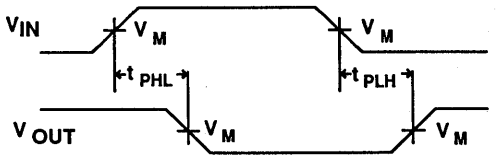
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na} or D_{nb} to Q_n (Other input Low)	Waveform 1	3.0 3.0	4.0 4.2	5.5 5.5	3.0 3.0	6.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay D_{na} or D_{nb} to Q_n (Other input High)	Waveform 2	3.5 3.0	5.3 4.7	7.0 6.5	3.5 3.0	8.0 7.5	ns

AC WAVEFORMS



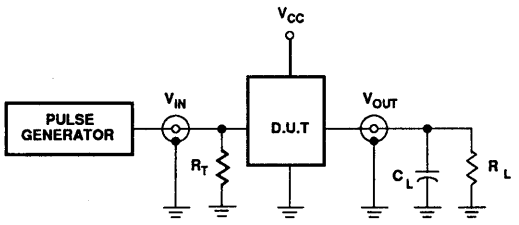
Waveform 1.
For Non-Inverting Outputs



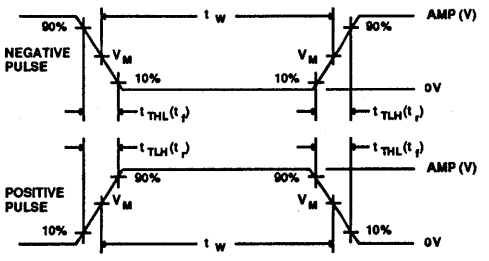
Waveform 2
For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

74F109
FLIP-FLOP

Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flops

Product Specification

FAST Products

DESCRIPTION

The 74F109 is a dual positive edge-triggered JK-type flip-flop featuring individual J, $\overline{K}$, Clock, Set and Reset inputs; also true and complementary outputs.
Set ($\overline{S}_p$) and Reset ($\overline{R}_p$) are asynchronous active-Low inputs and operate independently of the Clock (CP) input.
The J and $\overline{K}$ are edge-triggered inputs which control the state changes of the flip-flops as described in the Function Table.
Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition of the positive-going pulse.
The J and $\overline{K}$ inputs must be stable just one setup time prior to the Low-to-High transition of the clock for predictable operation.
The J$\overline{K}$ design allows operation as a D flip-flop by tying J and $\overline{K}$ inputs together.
Although the clock input is level sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock to output delay time for reliable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F109	125 MHz	12.3mA

ORDERING INFORMATION

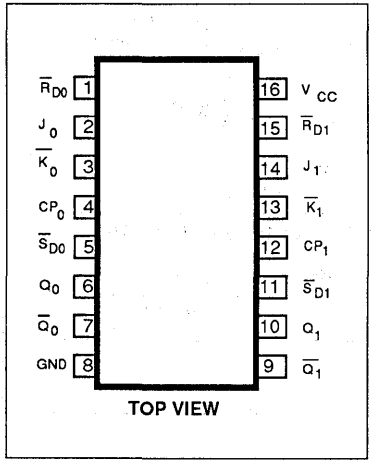
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F109N
16-Pin Plastic SO	N74F109D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOADVALUE HIGH/LOW
J_0, J_1	J inputs	1.0/1.0	20µA/0.6mA
$\overline{K}_0$, $\overline{K}_1$	K inputs	1.0/1.0	20µA/0.6mA
CP_0, CP_1	Clock inputs (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{S}_{D0}$, $\overline{S}_{D1}$	Set inputs (active Low)	1.0/3.0	20µA/1.8mA
$\overline{R}_{D0}$, $\overline{R}_{D1}$	Reset inputs (active Low)	1.0/3.0	20µA/1.8mA
Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

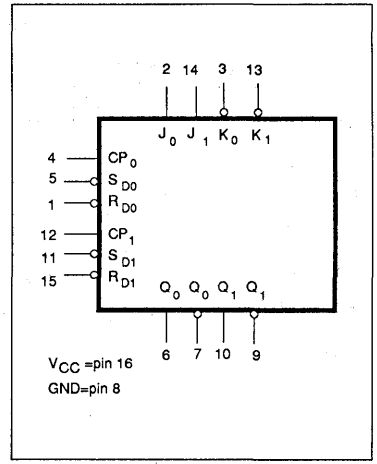
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

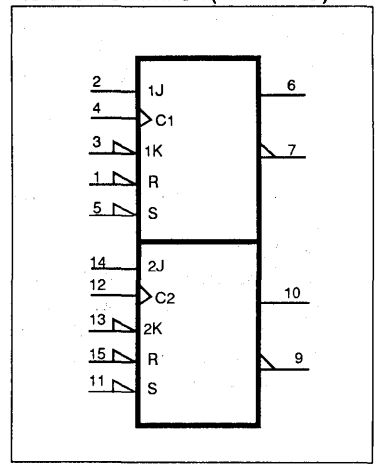


TOP VIEW

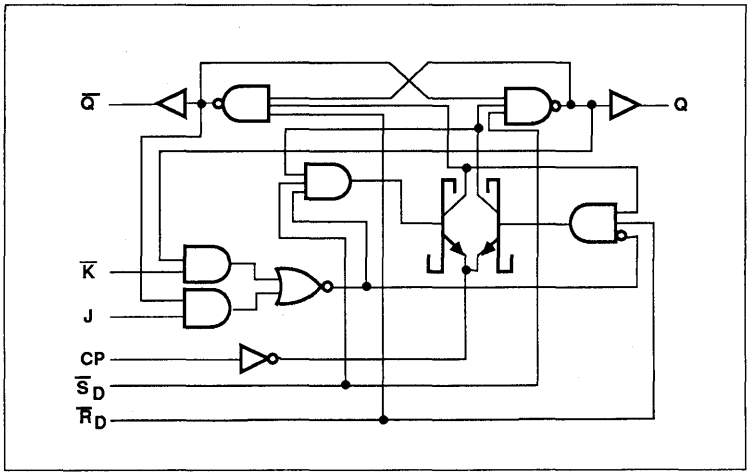
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
$\overline{S}_D$	$\overline{R}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$	
L	H	X	X	X	H	L	Asynchronous Set
H	L	X	X	X	L	H	Asynchronous Reset
L	L	X	X	X	H	H	Undetermined (Note)
H	H	↑	h	l	$\overline{q}$	q	Toggle
H	H	↑	l	l	L	H	Load "0" (Reset)
H	H	↑	h	h	H	L	Load "1" (Set)
H	H	↑	l	h	q	$\overline{q}$	Hold "no change"

H = High voltage level
h = High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
q=Lower case indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
Note =Both outputs will be High if both $\overline{S}_D$ and $\overline{R}_D$ go Low simultaneously.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} =MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} =MAX	±10%V_{CC}		0.30	0.50	V
			±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current $J, \overline{K}, CP_n$	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
	Low-level input current $\overline{S}_{Dn}, \overline{R}_{Dn}$					-1.8	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			12.3	17	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs High in turn.

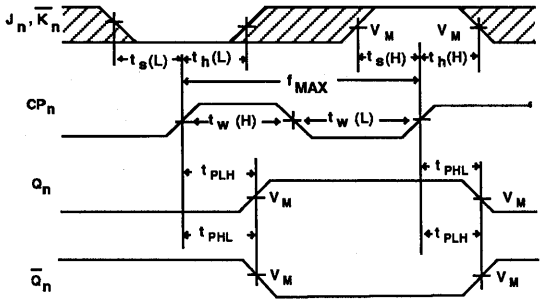
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	90	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveform 1	3.8 4.4	5.3 6.2	7.0 8.0	3.8 4.4	8.0 9.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_{Dn}$ to Q_n or $\overline{Q}_n$	Waveform 2	3.2 3.5	5.2 7.0	7.0 9.0	3.2 3.5	8.0 10.5	ns

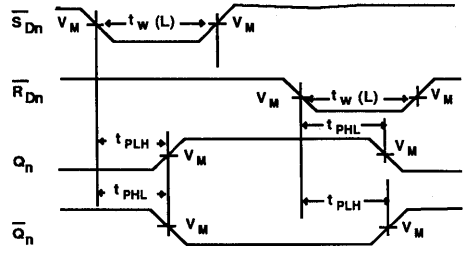
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J_n, $\overline{K}_n$ to CP	Waveform 1	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J_n, $\overline{K}_n$ to CP	Waveform 1	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	$\overline{S}_D$ or $\overline{R}_D$ Pulse width, Low	Waveform 2	4.0			4.0		ns
t_{rec}	Recovery time $\overline{S}_D$ or $\overline{R}_D$ to CP	Waveform 3	2.0			2.0		ns

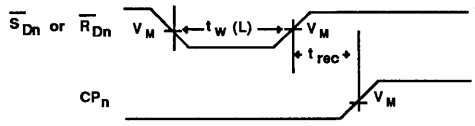
AC WAVEFORMS



Waveform 1. Propagation Delay For data to output, data setup time and hold times, and clock width



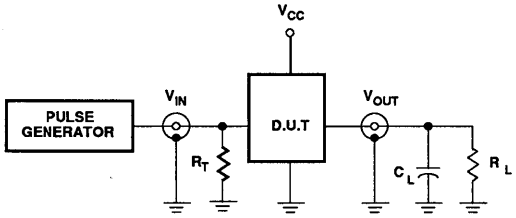
Waveform 2. Propagation Delay for set and reset to output, set and reset pulse width



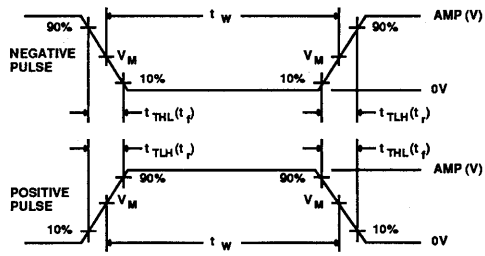
Waveform 3. Propagation Delay for reset to output, reset pulse width, and recovery time for reset to clock

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F112
Flip-Flop

Dual J-K Negative Edge-triggered Flip-Flop
Product Specification

FAST Products

DESCRIPTION

The 74F112, Dual Negative Edge-Triggered JK-Type Flip-Flop, features individual J, K, Clock ($\overline{CP}_n$), Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) inputs, true (Q_n) and complementary ($\overline{Q}_n$) outputs.

The $\overline{S}_D$ and $\overline{R}_D$ inputs, when Low, set or reset the outputs as shown in the Function Table regardless of the level at the other inputs.

A High level on the clock ($\overline{CP}_n$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}_n$ is High and flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output changes are initiated by the High-to-Low transition of the $\overline{CP}_n$.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F112	100MHz	15mA

ORDERING INFORMATION

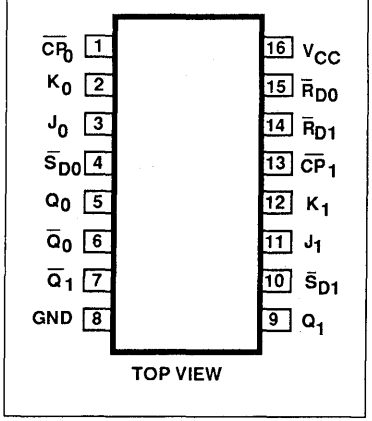
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F112N
16-Pin Plastic SO	N74F112D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_0, J_1	J inputs	1.0/1.0	20µA/0.6mA
K_0, K_1	K inputs	1.0/1.0	20µA/0.6mA
$\overline{S}_{D0}$, $\overline{S}_{D1}$	Set inputs (active Low)	1.0/5.0	20µA/3.0mA
$\overline{R}_{D0}$, $\overline{R}_{D1}$	Reset inputs (active Low)	1.0/5.0	20µA/3.0mA
$\overline{CP}_0$, $\overline{CP}_1$	Clock Pulse input (active falling edge)	1.0/4.0	20µA/2.4mA
Q_0,$\overline{Q}_0$; Q_1,$\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

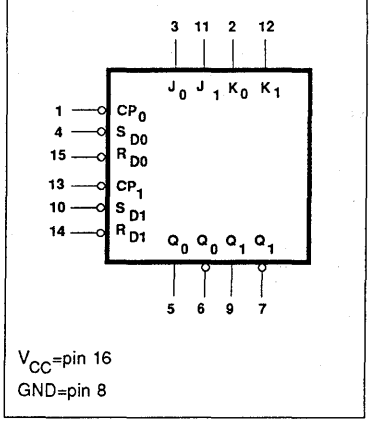
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



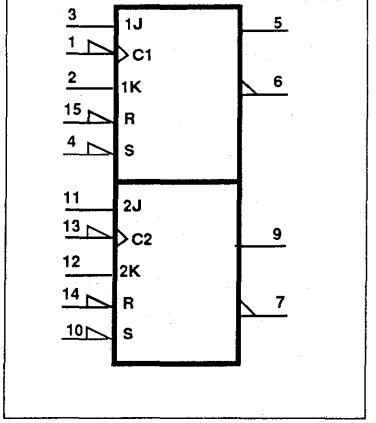
TOP VIEW

LOGIC SYMBOL

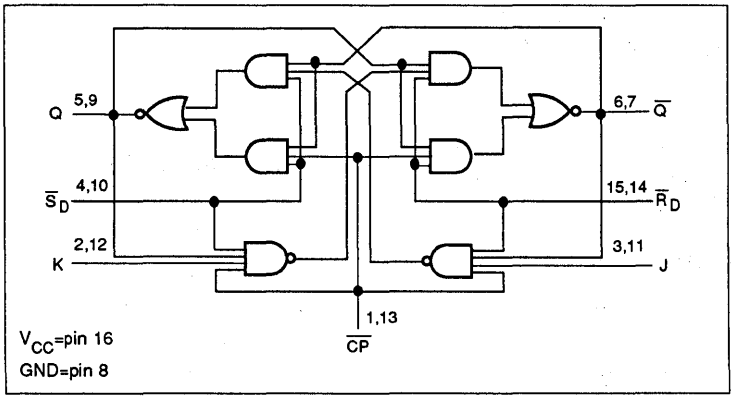


V_{CC}=pin 16
GND=pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	$\overline{K}$	Q	$\overline{Q}$	
L	H	X	X	X	H	L	Asynchronmous Set
H	L	X	X	X	L	H	Asynchronous Reset
L	L	X	X	X	H*	H*	Undetermined *
H	H	↓	h	h	$\overline{q}$	q	Toggle
H	H	↓	l	h	L	H	Load "0"(Reset)
H	H	↓	h	l	H	L	Load "1" (Set)
H	H	↓	l	l	q	$\overline{q}$	Hold "no change"
H	H	H	X	X	Q	$\overline{Q}$	Hold "no change"

H = High voltage level
h = High voltage level one setup time prior to High-to-Low clock transition
L = Low voltage level
l = Low voltage level one setup time prior to High-to-Low clock transition
q=Lower case letters indicate the state of the referenced output prior to the High-to-Low clock transition
X = Don't care
↓= High-to-Low clock transition
* =Both outputs will be High while both $\overline{S}_D$ and $\overline{R}_D$ are Low, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go High simultaneously.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	J_n, K_n	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{CP}_n$					-2.4	mA
		$\overline{S}_{Dn}$, $\overline{R}_{Dn}$					-3.0	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			15	21	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, with the Q and $\overline{Q}$ outputs High in turn.

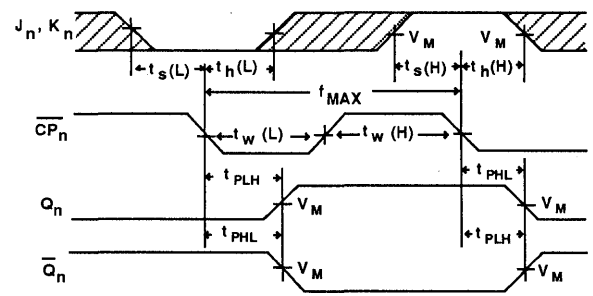
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	85	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	5.0 5.0	6.5 6.5	2.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_{Dn}$ to Q_n or $\overline{Q}_n$	Waveform 2,3	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	7.5 7.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J_n, K_n to $\overline{CP}_n$	Waveform 1	4.0 3.5			5.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J_n, K_n to $\overline{CP}_n$	Waveform 1	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	$\overline{CP}_n$ Pulse width, High or Low	Waveform 1	4.5 4.5			5.0 5.0		ns
$t_w(L)$	$\overline{S}_D$ or $\overline{R}_D$ Pulse width, Low	Waveform 2,3	4.5			5.0		ns
t_{REC}	Recovery time $\overline{S}_D$ or $\overline{R}_D$ to $\overline{CP}_n$	Waveform 2,3	4.0			5.0		ns

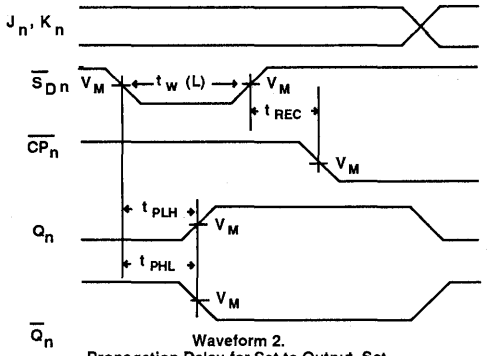
AC WAVEFORMS



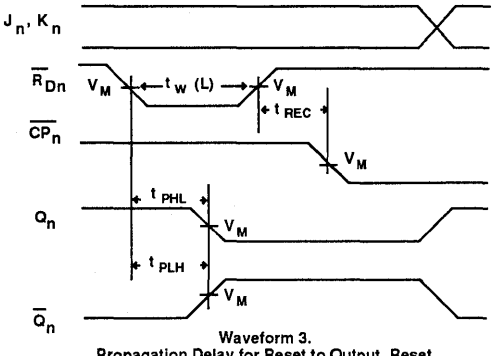
Waveform 1. Propagation Delay For data to output, data setup time and hold times, and clock pulse width

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

AC WAVEFORMS



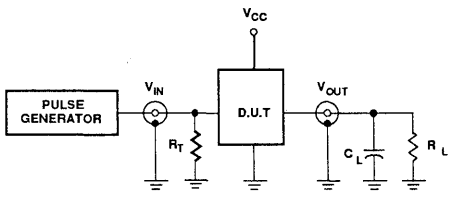
Waveform 2.
Propagation Delay for Set to Output, Set
Pulse Width, and Recovery Time for Set to Clock



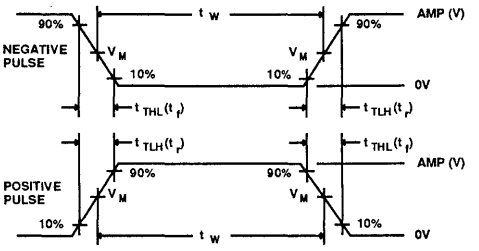
Waveform 3.
Propagation Delay for Reset to Output, Reset
Pulse Width, and Recovery Time for Reset to Clock

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F113
Flip-Flop

Dual J-K Negative Edge-Triggered Flip-Flops Without Reset
Product Specification

FAST Products

DESCRIPTION

The 74F113, Dual Negative Edge-Triggered JK-Type Flip-Flop, features individual J, K, Clock ($\overline{CP}$) and Set ($\overline{S}_D$) inputs, true and complementary outputs.

The asynchronous $\overline{S}_D$ input, when Low, forces the outputs to the steady state levels as shown in the Function Table regardless of the level at the other inputs.

A High level on the clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is High and flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output changes are initiated by the High-to-Low transition of the $\overline{CP}$.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F113	100MHz	15mA

ORDERING INFORMATION

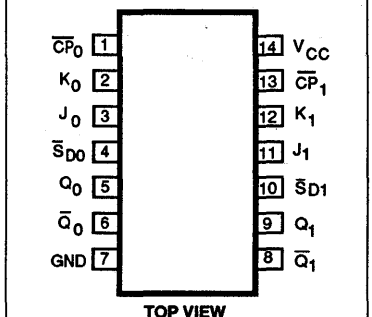
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F113N
16-Pin Plastic SO	N74F113D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_0, J_1	J inputs	1.0/1.0	20µA/0.6mA
K_0, K_1	K inputs	1.0/1.0	20µA/0.6mA
$\overline{S}_{D0}$, $\overline{S}_{D1}$	Set inputs (Active Low)	1.0/5.0	20µA/3.0mA
$\overline{CP}_0$, $\overline{CP}_1$	Clock Pulse inputs (Active rising edge)	1.0/4.0	20µA/2.4mA
Q_0, $\overline{Q}_0$, Q_1, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

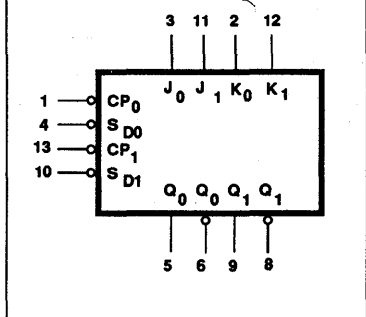
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



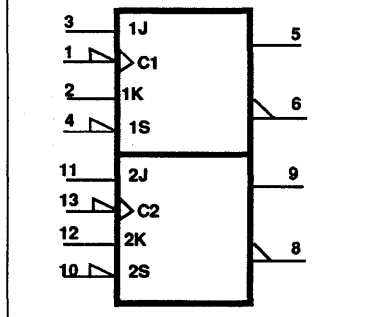
TOP VIEW

LOGIC SYMBOL

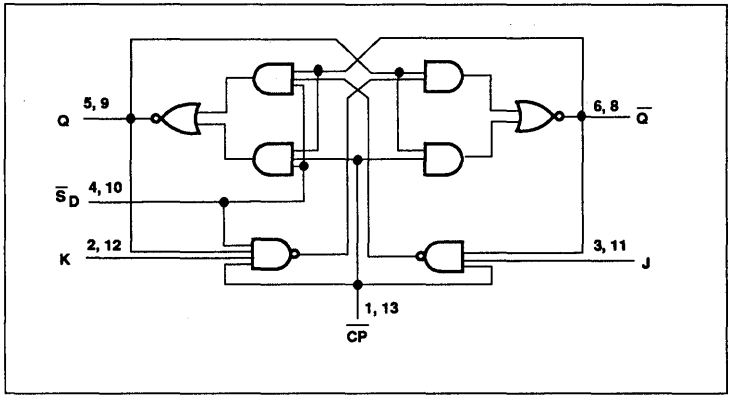


V_{CC} = pin 14
GND = pin 7

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{S}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$	
L	X	X	X	H	L	Asynchronous Set
H	↓	h	h	$\overline{q}$	q	Toggle
H	↓	l	h	L	H	Load "0"(Reset)
H	↓	h	l	H	L	Load "1" (Set)
H	↓	l	l	q	$\overline{q}$	Hold "no change"

H = High voltage level
h-= High voltage level one setup time prior to High-to-Low clock transition
L = Low voltage level
l = Low voltage level one setup time prior to High-to-Low clock transition
q=Lower case letters indicate the state of the referenced output prior to the High-to-Low clock transition
X = Don't care
↓= High-to-Low clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	J_n, K_n	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{CP}_n$					-2.4	mA
		$\overline{S}_{Dn}$					-3.0	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			15	21	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, with the Q and $\overline{Q}$ outputs High in turn.

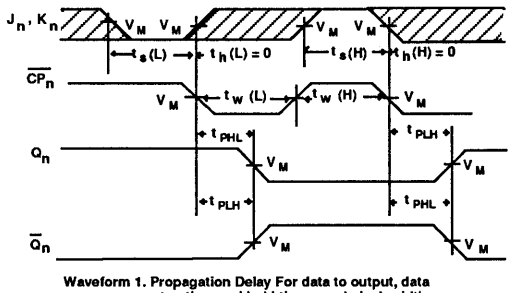
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	85	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	4.0 4.0	6.0 6.0	2.0 2.0	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	Waveform 2	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	7.5 7.5	ns

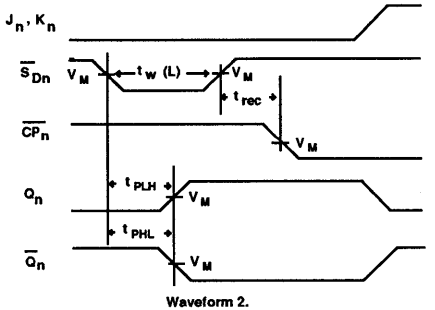
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J_n, K_n to $\overline{CP}_n$	Waveform 1	4.0 3.5			5.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J_n, K_n to $\overline{CP}_n$	Waveform 1	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	$\overline{CP}_n$ Pulse width, High or Low	Waveform 1	4.5 4.5			5.0 5.0		ns
$t_w(L)$	$\overline{S}_{Dn}$ Pulse width, Low	Waveform 2	4.5			5.0		ns
t_{REC}	Recovery time $\overline{S}_{Dn}$ to $\overline{CP}_n$	Waveform 2	4.5			5.0		ns

AC WAVEFORMS



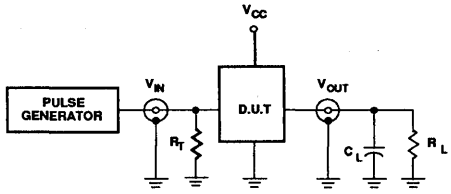
Waveform 1. Propagation Delay For data to output, data setup time and hold times, and clock width



Waveform 2.
Propagation Delay for set to output, set pulse width, and recovery time for set to clock

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable operation.

TEST CIRCUIT AND WAVEFORMS



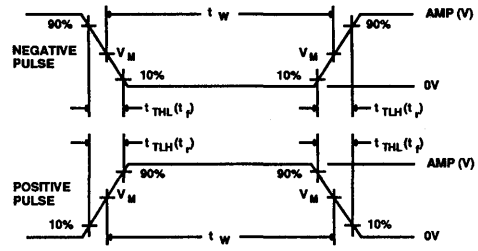
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F114
Flip-Flop

Dual J-K Negative Edge-Triggered Flip-Flop
With Common Clock And Reset
Product Specification

FAST Products

DESCRIPTION

The 74F114, Dual Negative Edge-Triggered JK-Type Flip-Flop with common clock and reset inputs, features individual J, K, Clock ($\overline{CP}$), Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) inputs, true and complementary outputs.
The $\overline{S}_D$ and $\overline{R}_D$ inputs, when Low, set or reset the outputs as shown in the Function Table regardless of the level at the other inputs.
A High level on the clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is High and flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output changes are initiated by the High-to-Low transition of the $\overline{CP}$.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F114	100MHz	15mA

ORDERING INFORMATION

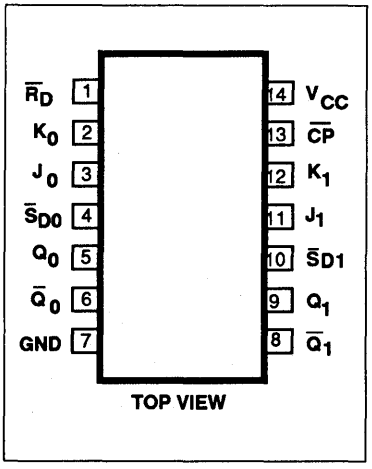
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F114N
14-Pin Plastic SO	N74F114D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_0, J_1	J inputs	1.0/1.0	20µA/0.6mA
K_0, K_1	K inputs	1.0/1.0	20µA/0.6mA
$\overline{S}_{D0}$, $\overline{S}_{D1}$	Set inputs (active Low)	1.0/5.0	20µA/3.0mA
$\overline{R}_D$	Reset input (active Low)	1.0/10.0	20µA/6.0mA
$\overline{CP}$	Clock Pulse input (active falling edge)	1.0/8.0	20µA/4.8mA
Q_0,$\overline{Q}_0$; Q_1, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

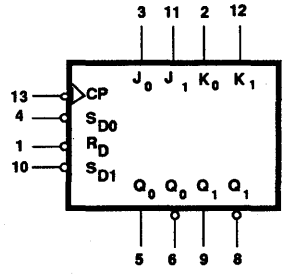
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



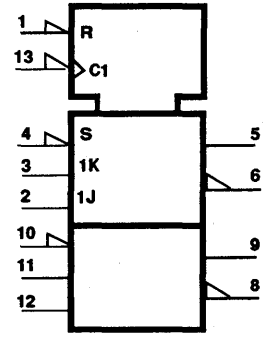
TOP VIEW

LOGIC SYMBOL

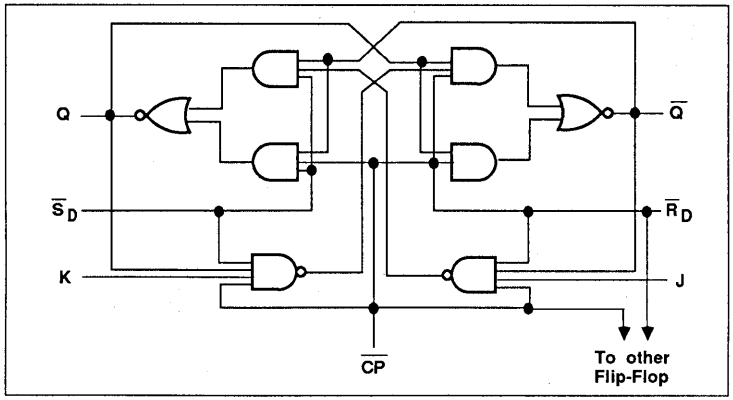


V_{CC} = pin 14
GND = pin 7

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$	
L	H	X	X	X	H	L	Asynchronous Set
H	L	X	X	X	L	H	Asynchronous Reset
L	L	X	X	X	H*	H*	Undetermined *
H	H	↓	h	l	$\overline{q}$	q	Toggle
H	H	↓	l	l	L	H	Load "0"(Reset)
H	H	↓	h	l	H	L	Load "1" (Set)
H	H	↓	l	l	q	$\overline{q}$	Hold "no change"

H = High voltage level
h = High voltage level one setup time prior to High-to-Low clock transition
L = Low voltage level
l = Low voltage level one setup time prior to High-to-Low clock transition
q=Lower case letters indicate the state of the referenced output prior to the High-to-Low clock transition
X = Don't care
↓= High-to-Low clock transition
Asynchronous inputs: Low input to $\overline{S}_D$ sets Q to High level, Low input to $\overline{R}_D$ sets Q to Low level
Set and Reset are independent of clock
Simultaneous Low on both $\overline{S}_D$ and $\overline{R}_D$ makes both Q and $\overline{Q}$ High
* =Both outputs will be High while both $\overline{S}_D$ and $\overline{R}_D$ are Low, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go High simultaneously.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	J_n, K_n	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{CP}$					-4.8	mA
		$\overline{S}_{Dn}$					-3.0	mA
		$\overline{R}_D$					-6.0	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			15	21	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, with the Q and $\overline{Q}$ outputs High in turn.

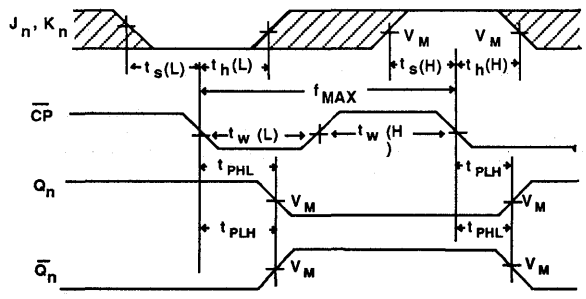
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	85	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	5.0 5.5	6.5 7.5	2.0 2.0	7.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_D$ to Q_n or $\overline{Q}_n$	Waveform 2,3	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	7.5 7.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J_n, $\overline{K}_n$ to $\overline{CP}$	Waveform 1	4.0 3.5			5.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J_n, $\overline{K}_n$ to $\overline{CP}$	Waveform 1	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse width High or Low	Waveform 1	4.5 4.5			5.0 5.0		ns
$t_w(L)$	$\overline{S}_{Dn}$, $\overline{R}_D$ Pulse width Low	Waveform 2,3	4.5			5.0		ns
t_{REC}	Recovery time $\overline{S}_{Dn}$, $\overline{R}_D$ to $\overline{CP}$	Waveform 2,3	4.5			5.0		ns

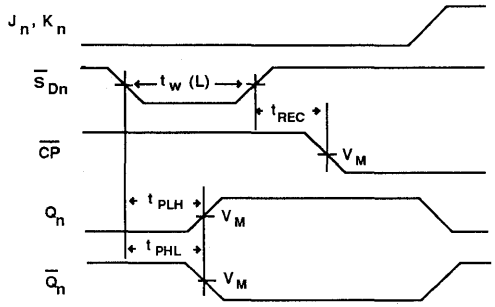
AC WAVEFORMS



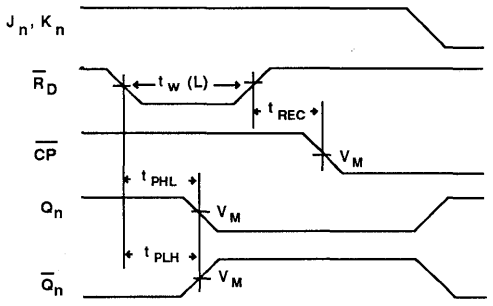
Waveform 1. Propagation Delay for Data to Output, Data Setup Time and Hold Times, and Clock Width

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

AC WAVEFORMS



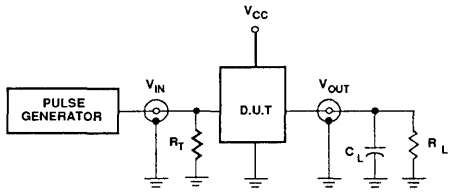
Waveform 2.
Propagation Delay for Set to Output, Set Pulse Width, and Recovery Time for Set to clock



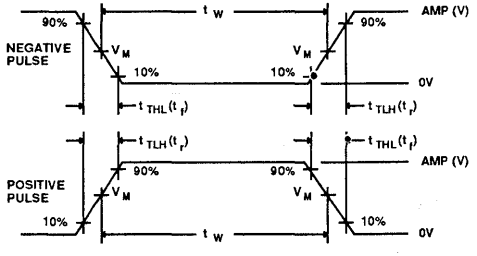
Waveform 3.
Propagation Delay forReset to Output, Reset Pulse Width, and Recovery Time for Reset to Clock

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F125, 74F126
Buffers

FAST Products

74F125 Quad Buffer (3-State)
74F126 Quad BUffer (3-State)

Product Specification

FEATURES
- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F125	5.0ns	23mA
74F126	5.0ns	26mA

ORDERING INFORMATION

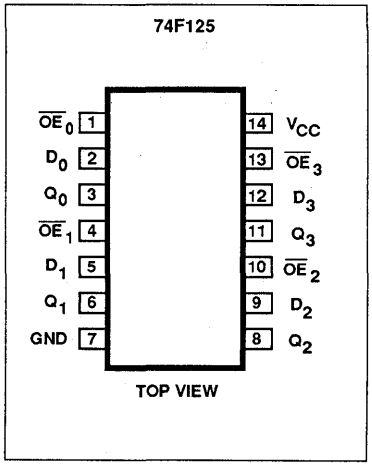
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F125N, N74F126N
14-Pin Plastic SO	N74F125D, N74F126D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

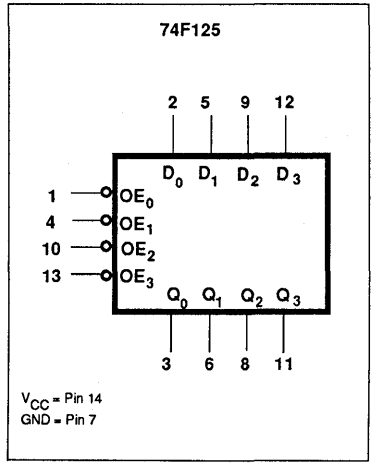
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0-D_3	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_0$-$\overline{OE}_3$	Output Enable inputs (active Low) , F125	1.0/0.033	20μA/20μA
OE_0-OE_3	Output Enable inputs (active High) , F126	1.0/0.033	20μA/20μA
Q_0-Q_3	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

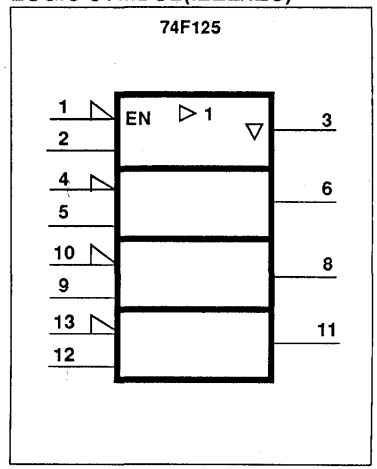
PIN CONFIGURATION



LOGIC SYMBOL

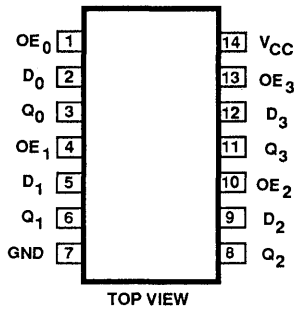


LOGIC SYMBOL(IEEE/IEC)



PIN CONFIGURATION

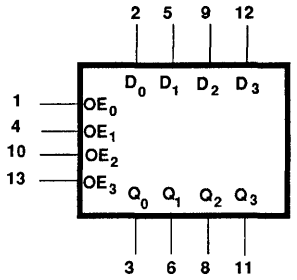
74F126



TOP VIEW

LOGIC SYMBOL

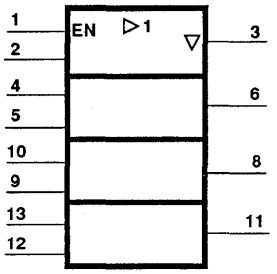
74F126



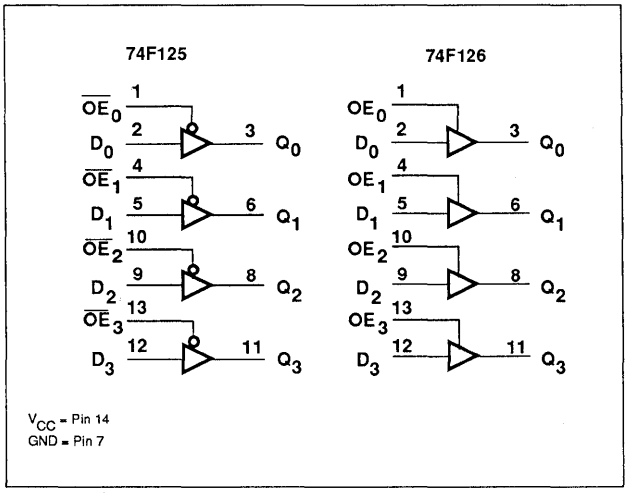
V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL(IEEE/IEC)

74F126



LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

FUNCTION TABLE, 74F125

INPUTS		OUTPUT
$\overline{OE}_n$	D_n	Q_n
L	L	L
L	H	H
H	X	Z

FUNCTION TABLE, 74F126

INPUTS		OUTPUT
OE_n	D_n	Q_n
H	L	L
H	H	H
L	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

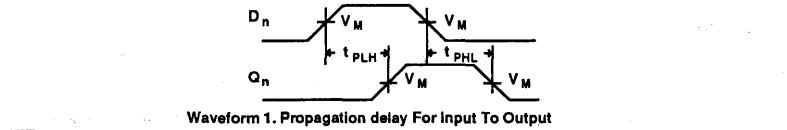
SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.3		V
			I_{OH}=-15mA	±10%V_{CC}	2.0			V
				±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}			0.55	V
				±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum Input voltage	V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_I	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-20	mA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O= 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = MAX, V_O= 0.5V					-50	µA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F125	I_{CCH}	V_{CC} = MAX, $\overline{OE}_n$ = GND, D_n=4.5V		17	24	mA
			I_{CCL}	V_{CC} = MAX, $\overline{OE}_n$ = D_n=GND		28	40	mA
			I_{CCZ}	V_{CC} = MAX, $\overline{OE}_n$ = D_n=4.5V		25	35	mA
		'F126	I_{CCH}	V_{CC} = MAX, OE_n = D_n=4.5V		20	30	mA
			I_{CCL}	V_{CC} = MAX, OE_n = 4.5V, D_n=GND		32	48	mA
			I_{CCZ}	V_{CC} = MAX, OE_n = GND, D_n=4.5V		26	39	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

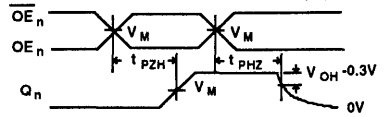
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F125	Waveform 1	2.0 3.0	4.0 5.5	6.0 7.5	2.0 3.0	6.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 2 Waveform 3	3.5 4.0	5.5 6.0	7.5 8.0	3.5 4.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 2 Waveform 3	1.5 1.5	3.5 3.5	5.0 5.5	1.5 1.5	6.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F126	Waveform 1	2.0 3.0	4.0 5.5	6.5 8.0	2.0 3.0	7.0 8.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 2 Waveform 3	4.0 4.0	6.0 6.0	7.5 8.0	3.5 3.5	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 2 Waveform 3	2.0 3.0	4.5 5.5	6.5 7.5	2.0 3.0	7.5 8.0	ns

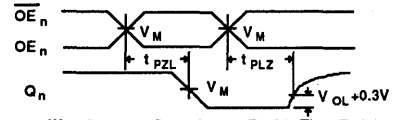
AC WAVEFORMS



Waveform 1. Propagation delay For Input To Output



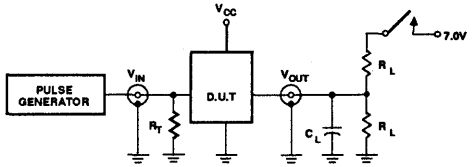
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

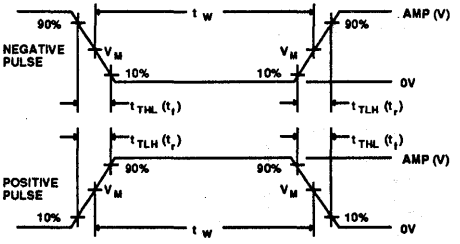
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F132
Schmitt Trigger

Quad 2-Input NAND Schmitt Trigger

FAST Products

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F132	6.3 ns	13 mA

DESCRIPTION

The 74F132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates. Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mv) is determined by reisistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as three inputs remain at a more positive voltage than V_{T+MAX}, the gate will respond in the transition of the other input as shown in Waveform 1.

ORDERING INFORMATION

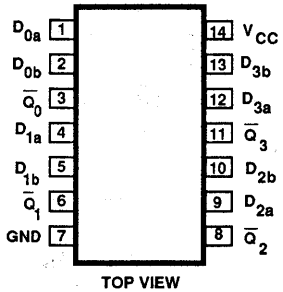
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F132N
14-Pin Plastic SO	N74F132D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}_n$	Data output	50/33	1.0mA/20mA

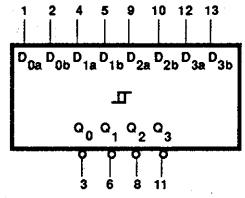
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



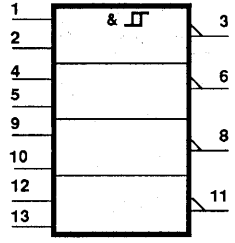
TOP VIEW

LOGIC SYMBOL

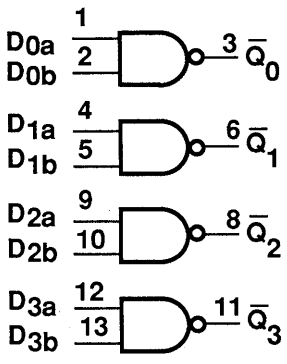


V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = pin 14
GND = pin 7

FUNCTION TABLE

INPUTS		OUTPUT
D_{na}	D_{nb}	$\overline{Q}_n$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

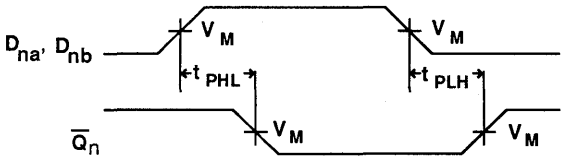
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{T+}	Positive-going threshold		V_{CC} =5.0V		1.5	1.7	2.0	V
V_{T-}	Negative-going threshold		V_{CC} =5.0V		0.7	0.9	1.1	V
ΔV_T	Hysteresis (V_{T+} - V_{T-})		V_{CC} =5.0V		0.4	0.8		V
V_{OH}	High-level output voltage		V_{CC} =MIN,	±10%V_{CC}	2.5			V
			V_I=V_{T-MIN}, I_{OH} =MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} =MIN,	±10%V_{CC}		0.30	0.50	V
			V_I=V_{T+MAX}, I_{OL} =MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_{T+}	Input current at positive-going threshold		V_{CC} =5.0V, V_I = V_{T+}			0		µA
I_{T-}	Input current at negative-going threshold		V_{CC} =5.0V, V_I = V_{T-}			-350		µA
I_I	Input current at maximun input voltage		V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} =MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} =MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} =MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} =MAX	V_{IN}=GND		8.5	12.0	mA
		I_{CCL}		V_{IN}=4.5V		13.0	19.5	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to $\overline{Q}_n$	Waveform 1	4.0 5.5	5.5 7.0	7.0 8.5	3.5 5.0	8.5 9.0	ns

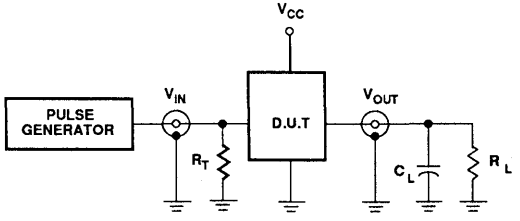
AC WAVEFORMS



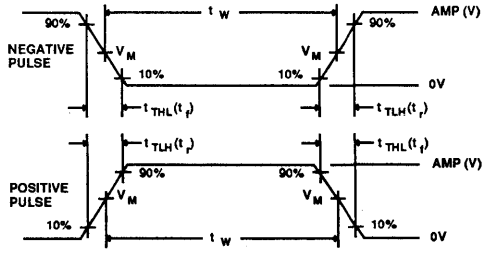
Waveform 1.
For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F133 Gate

13-Input NAND Gate

FAST Products

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F133	4.0 ns	2.0 mA

ORDERING INFORMATION

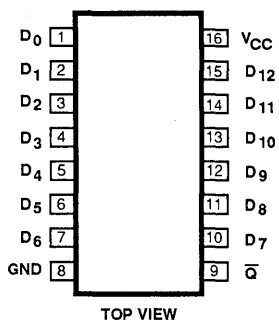
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F133N
14-Pin Plastic SO	N74F133D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0-D_{14}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}$	Data Output	50/33	1.0mA/20mA

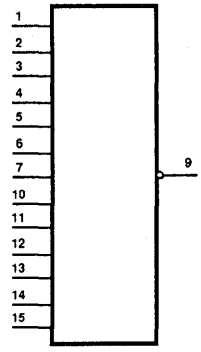
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



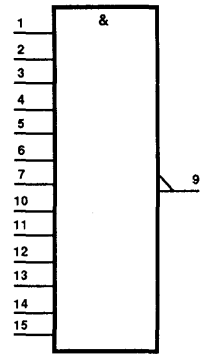
TOP VIEW

LOGIC SYMBOL

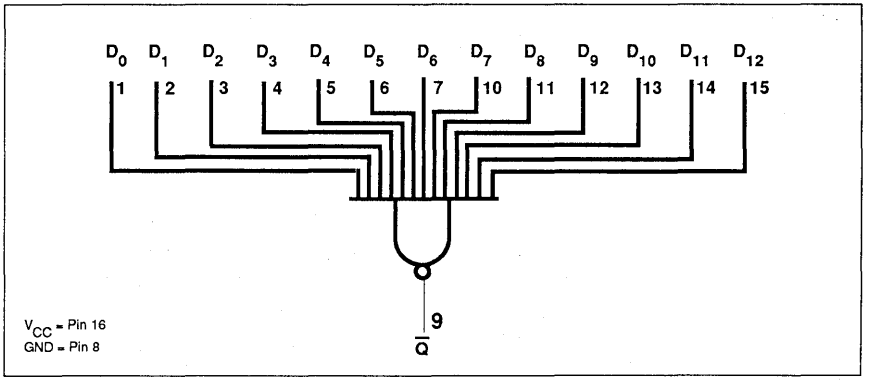


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS													OUTPUT
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	$\overline{Q}$
H	H	H	H	H	H	H	H	H	H	H	H	H	L
Any one input = L													H

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

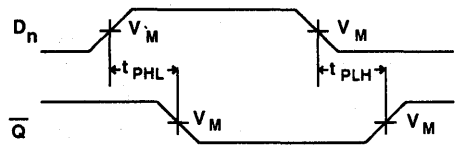
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			1.0	2.0	mA
		I_{CCL}				2.5	4.0	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	LIMITS T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}$	Waveform 1	2.0 2.5	4.0 4.5	7.0 7.5	1.5 2.0	7.5 8.0	ns

AC WAVEFORMS

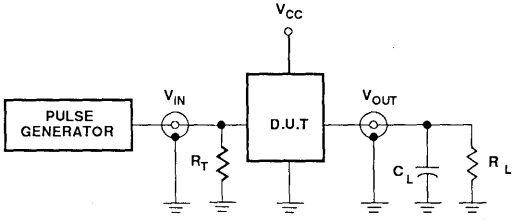


Waveform 1.

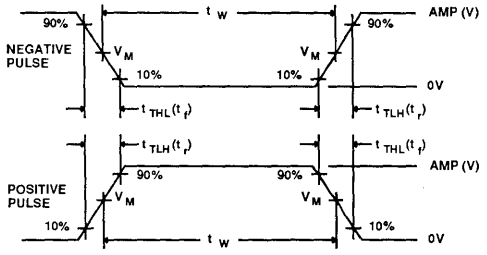
Propagation Delay for Data to Output

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F138
Decoder/Demultiplexer

FAST Products

1-Of-8 Decoder/Demultiplexer

Product Specification

FEATURES
- **Demultiplexing capability**
- **Multiple input enable for easy expansion**
- **Ideal for memory chip select decoding**
- **High speed replacement for Intel 3205**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F138	5.8ns	13mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F138N
16-Pin Plastic SO	N74F138D

DESCRIPTION

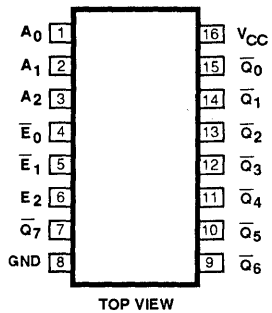
The 74F138 decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled, provides eight mutually exclusive, active-Low outputs ($\overline{O}_0$-$\overline{O}_7$). The device features three Enable inputs; two active-Low($\overline{E}_0$,$\overline{E}_1$) and one active High(E_2). Every output will be HIgh unless $\overline{E}_0$ and $\overline{E}_1$ are Low and E_2 is High. This multiple enable function allows easy parallel expansion of the device to 1-of-32 (5 lines to 32 lines) decoder with just four 'F138s and one inverter. The device can be used as an eight output demultiplexer by using one of the active-Low Enable inputs as the Data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active-High or active-Low state.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

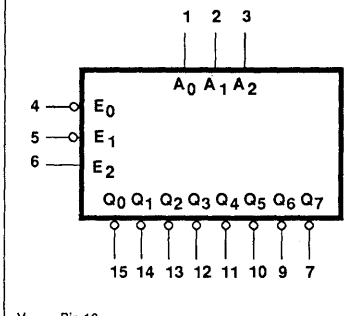
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_2	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_0$, $\overline{E}_1$	Enable inputs (active Low)	1.0/1.0	20µA/0.6mA
E_2	Enable input (active High)	1.0/1.0	20µA/0.6mA
$\overline{O}_0$-$\overline{O}_7$	Data outputs (active Low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

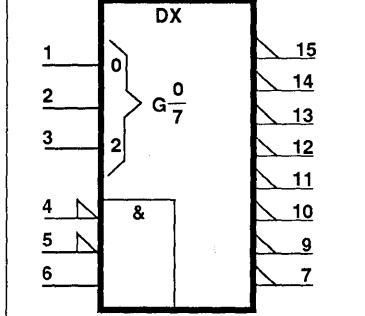
PIN CONFIGURATION



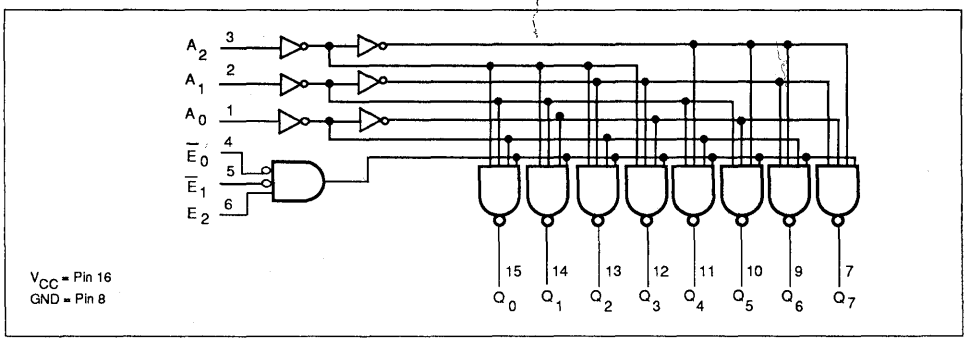
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM

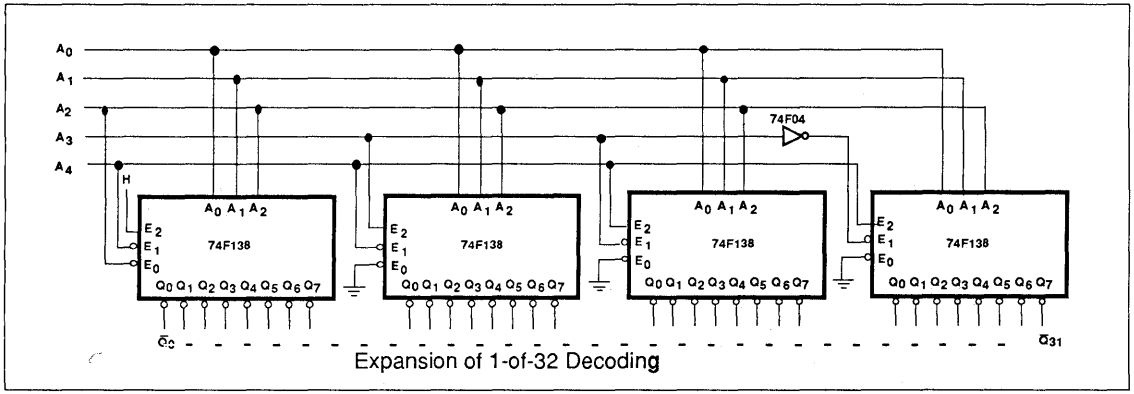


DECODER FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_0$	$\overline{E}_1$	E_2	A_0	A_1	A_2	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

APPLICATION



Expansion of 1-of-32 Decoding

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]	V_{CC} = MAX			13	20	mA

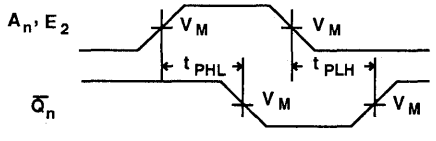
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. To measure I_{CC}, outputs must be open, V_{IN} on all inputs=4.5V.

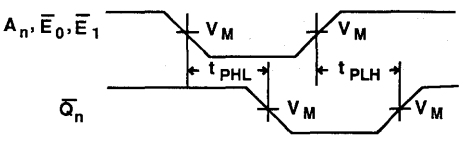
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Q}_n$	Waveform 1, 2	3.5 4.0	5.6 6.1	7.0 8.0	3.5 4.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$ or $\overline{E}_1$ to $\overline{Q}_n$	Waveform 2	3.5 3.0	6.4 5.3	7.0 7.0	3.5 3.0	8.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay E_2 to $\overline{Q}_n$	Waveform 1	4.0 3.5	6.2 5.6	8.0 7.5	4.0 3.5	9.0 8.5	ns

AC WAVEFORMS



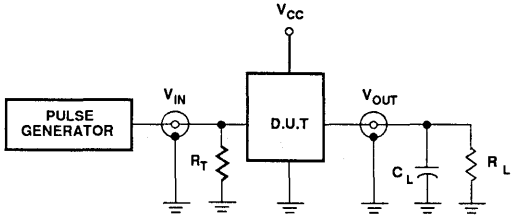
Waveform 1. For Inverting Outputs



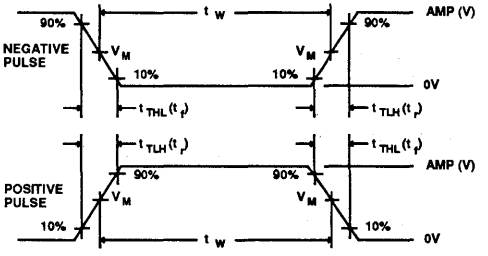
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F139
Decoder/Demultiplexer

FAST Products

Dual 1-of-4 Decoder//Demultiplexer

Product Specification

FEATURES
- **Demultiplexing capability**
- **Two independent 1-of-4 decoders**
- **Multifunction capability**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F139	5.3ns	13mA

DESCRIPTION

The 74F139 is a high speed, dual 1-of-4 decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (A_{0n}, A_{1n}) and providing four mutually exclusive active-Low outputs ($\overline{Q}_{0n}$ - $\overline{Q}_{3n}$). Each decoder has an active-Low Enable ($\overline{E}$). When $\overline{E}$ is High, every output is forced High. The Enable can be used as the Data input for a 1-of-4 demultiplexer application.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F139N
16-Pin Plastic SO	N74F139D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_{na}, A_{nb}	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_a$, $\overline{E}_b$	Enable inputs (active Low)	1.0/1.0	20µA/0.6mA
$\overline{Q}_{0n}$- $\overline{Q}_{3n}$	Data outputs (active Low)	50/33	1.4mA/20mA

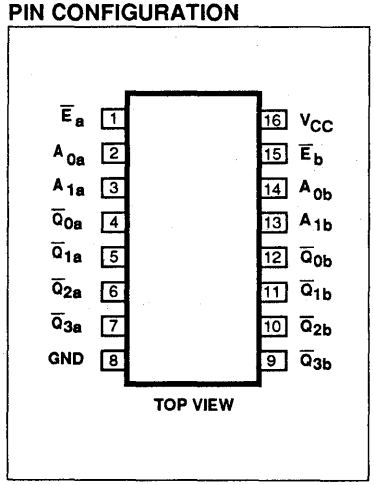
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

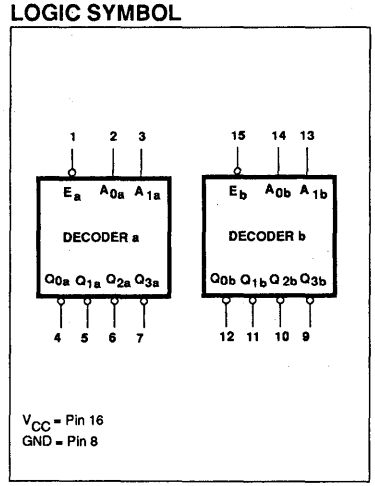
H = High voltage level
L = Low voltage level
X = Don't care

PIN CONFIGURATION



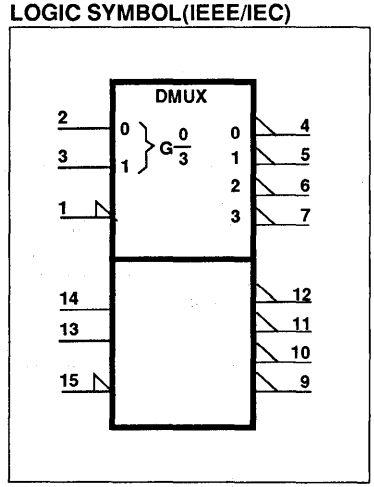
TOP VIEW

LOGIC SYMBOL

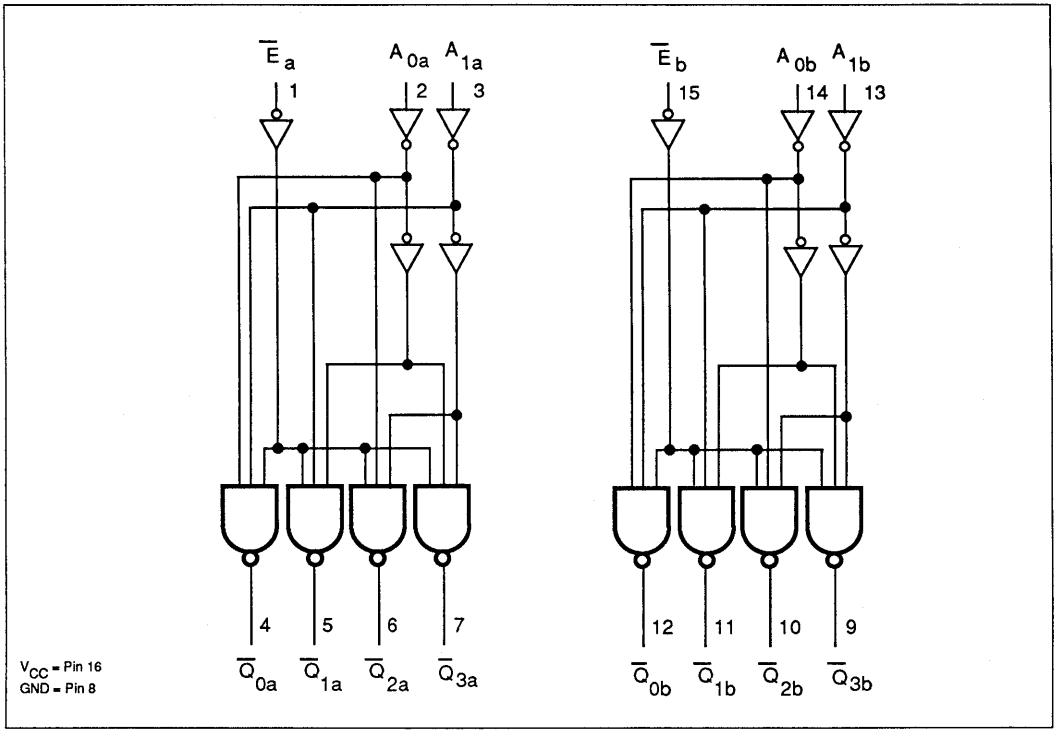


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			13	20	mA

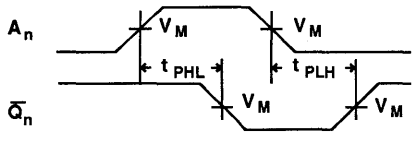
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

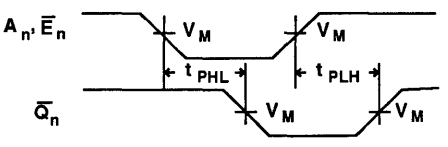
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_0 or A_1 to $\overline{Q}_{na}$, $\overline{Q}_{nb}$	Waveform 1 , 2	3.5 4.0	5.3 6.1	7.0 8.0	3.0 4.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to $\overline{Q}_{na}$, $\overline{Q}_{nb}$	Waveform 2	3.5 3.0	5.4 4.7	7.0 6.5	3.5 3.0	8.0 7.5	ns

AC WAVEFORMS



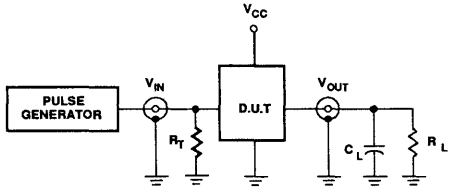
Waveform 1. For Inverting Outputs



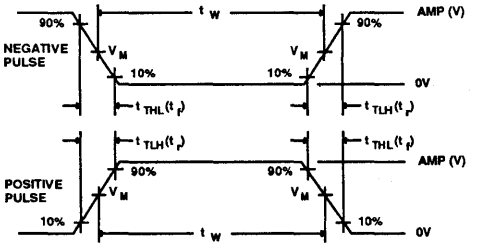
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F148
Encoder

FAST Products

8-Input Priority Encoder

Product Specification

FEATURES

- **Code conversions**
- **Multi-channel D/A converter**
- **Decimal-to-BCD converter**
- **Cascading for priority encoding of "N" bits**
- **Input enable capability**
- **Priority encoding-automatic selection of highest priority input line**
- **Output enable-active Low when all inputs are High**
- **Group signal output-active when any input is Low**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F148	6.0ns	23mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F148N
16-Pin Plastic SO	N74F148D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

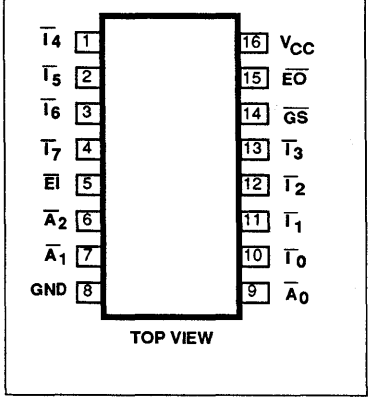
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{I}_1$-$\overline{I}_7$	Priority inputs (active Low)	1.0/2.0	20µA/1.2mA
$\overline{I}_0$	Priority input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{EI}$	Enable input (active Low)	1.0/2.0	20µA/1.2mA
$\overline{EO}$	Enable output (active Low)	50/33	1.0mA/20mA
$\overline{GS}$	Group select output (active Low)	50/33	1.0mA/20mA
$\overline{A}_0$-$\overline{A}_2$	Address outputs (active Low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

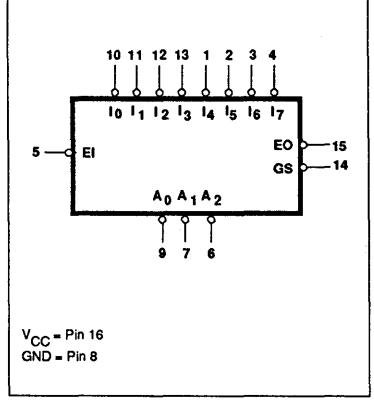
The 74F148 8-input priority encoder accepts data from eight active-Low inputs and provides a binary representation on the three active-Low outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line $\overline{I}_7$ having the highest priority. A High on the Enable Input ($\overline{EI}$) will force all outputs to the inactive (High) state and allow new data to settle without producing erroneous information at the outputs. A Group Signal ($\overline{GS}$) output and an Enable Output ($\overline{EO}$) are provided with the three data outputs. The $\overline{GS}$ is active-Low when any input is Low: this indicates when any input is active. The $\overline{EO}$ is active-Low when all inputs are High. Using the Enable Output along with the Enable Input allows priority encoding of N input signals. Both $\overline{EO}$ and $\overline{GS}$ are active-High when the Enable Input is High.

PIN CONFIGURATION



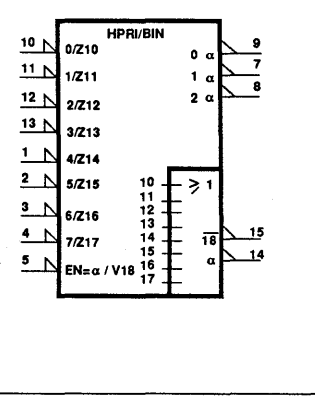
TOP VIEW

LOGIC SYMBOL

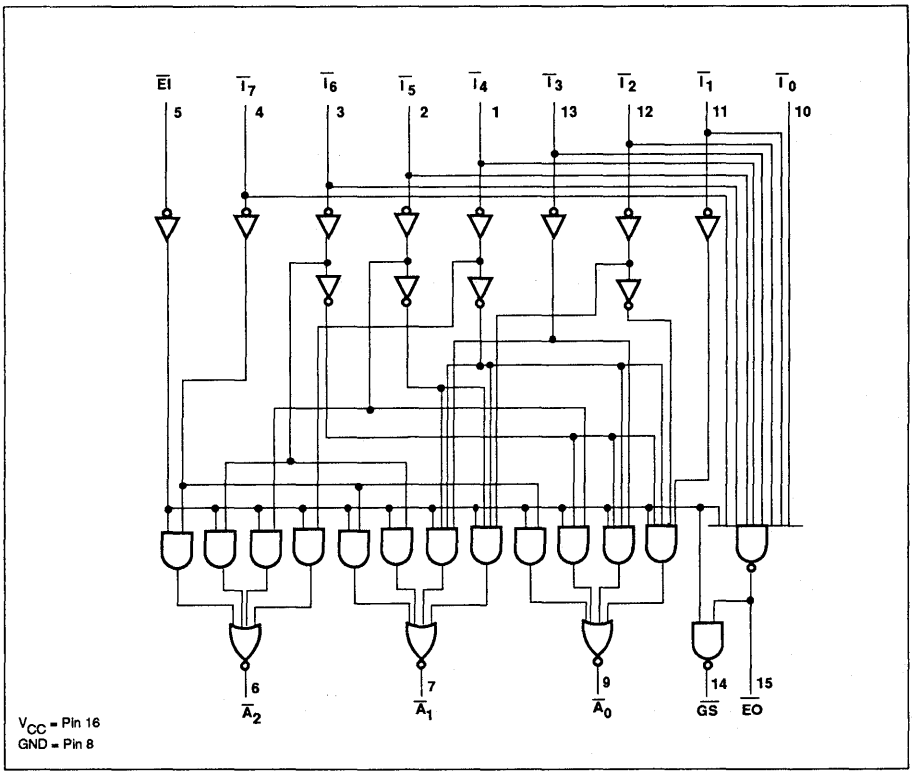


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM

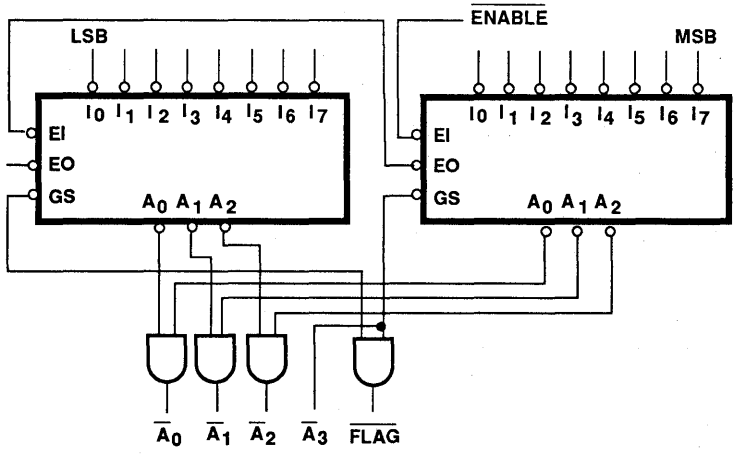


FUNCTION TABLE

INPUTS								OUTPUTS				
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	$\overline{GS}$	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = High voltage level
L = Low voltage level
X = Don't care

APPLICATION



16-Input priority Encoder

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

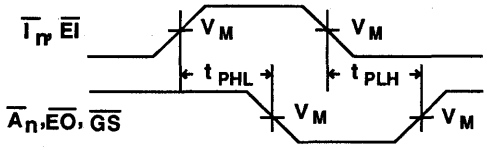
SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
			±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current $\overline{I}_0$	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
	Low-level input current $\overline{I}_1$-$\overline{I}_7$, $\overline{EI}$					-1.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]	V_{CC} = MAX			23	35	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. To measure I_{CC}, outputs must be open, V_{IN} on all inputs=4.5V.

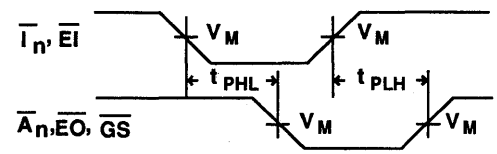
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\overline{I}_n$ to $\overline{A}_n$	Waveform 2	3.5 4.0	6.0 6.0	9.0 10.5	3.5 4.0	10.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{I}_n$ to $\overline{EO}$	Waveform 1	2.0 2.5	3.5 4.5	6.5 7.5	2.0 2.5	7.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{I}_n$ to $\overline{GS}$	Waveform 2	2.0 2.0	4.0 6.0	9.0 8.0	2.0 2.0	10.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ to $\overline{A}_n$	Waveform 2	3.5 3.0	6.0 5.5	8.5 8.0	3.5 3.0	9.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ to $\overline{GS}$	Waveform 2	2.5 3.0	4.5 5.5	7.0 7.5	2.5 3.0	8.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ to $\overline{EO}$	Waveform 2	3.0 4.5	5.0 7.0	7.0 10.5	3.0 4.5	8.0 12.0	ns

AC WAVEFORMS



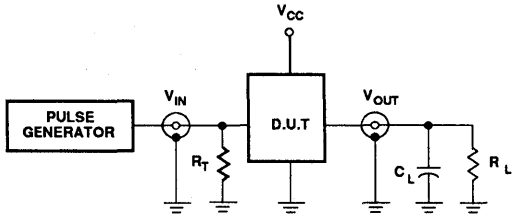
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M =1.5V

TEST CIRCUIT AND WAVEFORMS



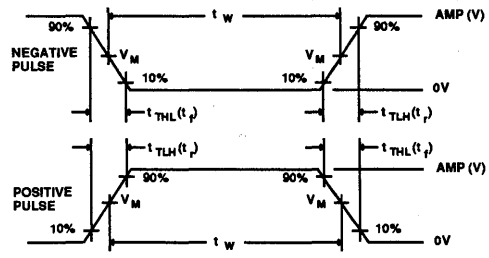
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F151, 74F151A
Multiplexers

FAST Products

74F151 8-input Multiplexer
74F151A 8-input Multiplexer
Product Specification

FEATURES
- **High speed 8-to-1 multiplexing**
- **On chip decoding**
- **Multifunction capability**
- **Complementary outputs**
- **See 'F251/'F251A for 3-state version**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F151	5.5ns	13.5mA
74F151A	4.5ns	17mA

DESCRIPTION

The 74F151 and 74F151A are logic implementations of a single-pole, 8-position switch with the switch position controlled by the state of three Select (S_0, S_1, S_2) inputs. True(Y) and complementary ($\overline{Y}$) outputs are both provided. The Enable input ($\overline{E}$) is active Low. When $\overline{E}$ is High, the $\overline{Y}$ output is High and the Y output is Low, regardless of all other inputs. In one package the 74F151 or 74F151A provides the ability to select from eight sources of data or control information. The device can provide any logic function of four variables and the negation with correct manipulation.

74F151A is the faster version of 74F151.

ORDERING INFORMATION

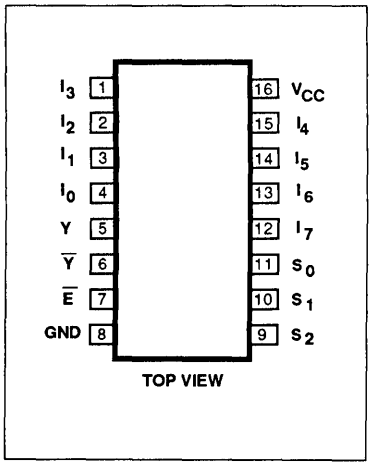
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F151N, N74F151AN
16-Pin Plastic SO	N74F151D, N74F151AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

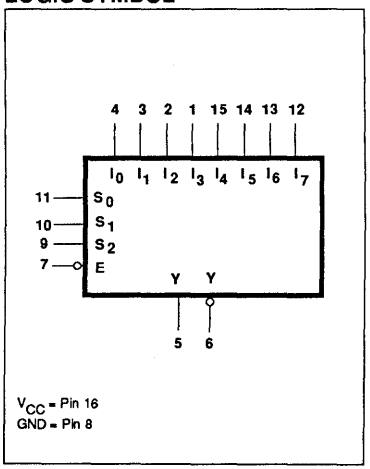
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0- I_7	Data inputs	1.0/1.0	20µA/0.6mA
S_0- S_2	Select inputs	1.0/1.0	20µA/0.6mA
$\overline{E}$	Enable input (active Low)	1.0/1.0	20µA/0.6mA
Y, $\overline{Y}$	Data outputs	150/33	3mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

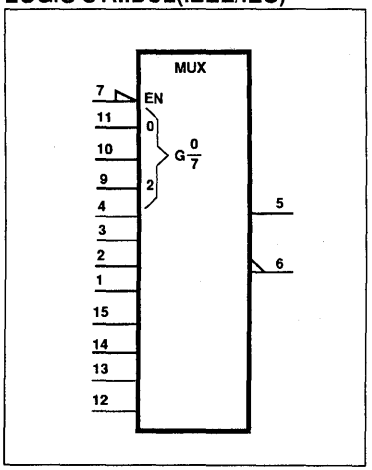
PIN CONFIGURATION



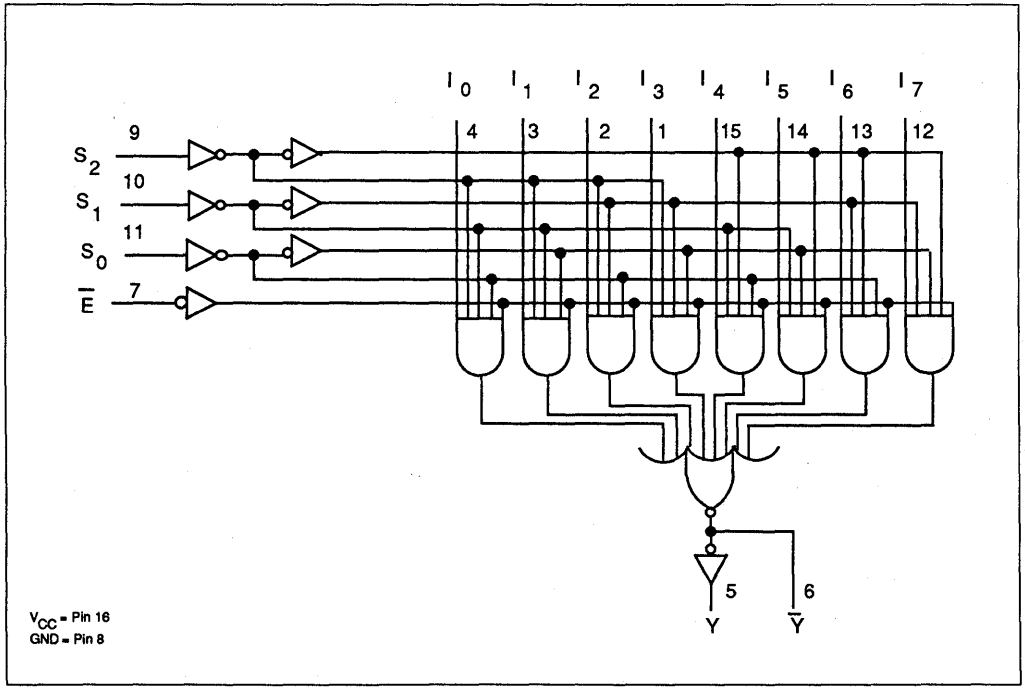
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
S_2	S_1	S_0	$\overline{E}$	Y	$\overline{Y}$
X	X	X	H	L	H
L	L	L	L	I_0	$\overline{I}_0$
L	L	H	L	I_1	$\overline{I}_1$
L	H	L	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
H	L	L	L	I_4	$\overline{I}_4$
H	L	H	L	I_5	$\overline{I}_5$
H	H	L	L	I_6	$\overline{I}_6$
H	H	H	L	I_7	$\overline{I}_7$

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
				V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
				V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]			V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	74F151	V_{CC} = MAX			13	18	mA
		I_{CCL}					15	20	mA
		I_{CCH}	74F151A	V_{CC} = MAX			18	25	mA
		I_{CCL}					17	25	mA

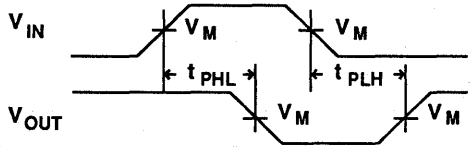
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

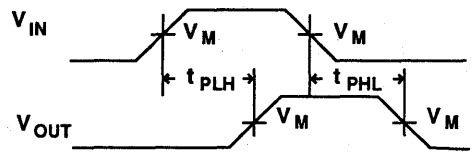
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	74F151	Waveform 1	3.0 3.0	4.5 4.5	6.5 6.5	2.5 3.0	9.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$		Waveform 2	2.0 1.0	4.0 2.5	6.0 4.0	2.0 1.0	7.0 5.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y		Waveform 1,2	4.0 4.5	7.0 7.0	9.5 9.0	4.0 4.5	12.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$		Waveform 1,2	4.0 2.0	6.5 4.5	9.0 7.0	3.5 2.0	10.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y		Waveform 1	6.0 4.0	8.0 5.5	10.0 7.0	5.5 4.0	11.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}$		Waveform 1	3.5 4.0	5.0 5.5	6.5 7.5	3.5 4.0	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y	74F151A	Waveform 1	2.5 2.5	4.5 4.5	7.0 7.0	2.5 2.5	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$		Waveform 2	2.0 1.0	4.0 2.0	7.0 4.5	2.0 1.0	7.5 5.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y		Waveform 1,2	4.5 4.0	6.5 6.0	10.0 8.5	4.0 3.5	11.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$		Waveform 1,2	3.5 2.5	5.5 4.5	8.5 7.0	3.0 2.0	9.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y		Waveform 1	4.0 3.0	6.5 5.0	9.0 7.0	3.5 3.0	9.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}$		Waveform 1	2.5 2.0	4.5 3.5	6.5 5.5	2.5 1.5	7.0 6.0	ns

AC WAVEFORMS



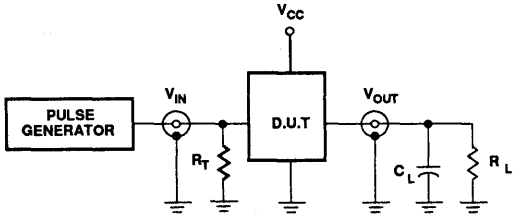
Waveform 1. For Inverting Outputs



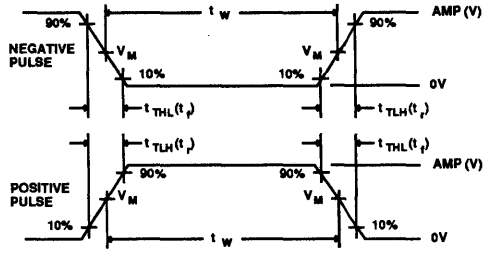
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F153
Multiplexer

FAST Products

Dual 4-Line to 1-Line Multiplexer

Product Specification

FEATURES
- **Non-inverting outputs**
- **Separate enable for each section**
- **Common select inputs**
- **See 'F253 for 3-state version**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F153	7.0ns	12mA

DESCRIPTION

The 74F153 is a dual 4-input multiplexer that can select 2 bits of data from up to four sources selected by common Select inputs (S_0,S_1). The two 4-input multiplexer circuits have individual active-Low Enables ($\overline{E}_a$,$\overline{E}_b$) which can be used to strobe the outputs independently. Outputs (Y_a, Y_b) are forced Low when the corresponding Enables ($\overline{E}_a$,$\overline{E}_b$) are High.

The 'F153 is the logic implementation of a 2-pole, 4-position switch where the switch is determined by the logic levels supplied to the common select inputs.

ORDERING INFORMATION

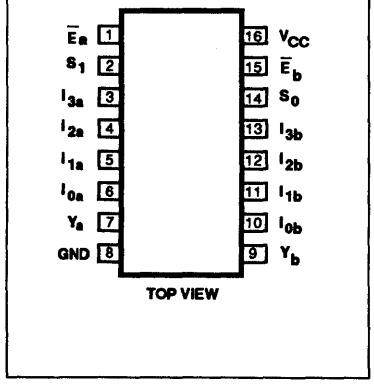
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F153N
16-Pin Plastic SO	N74F153D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

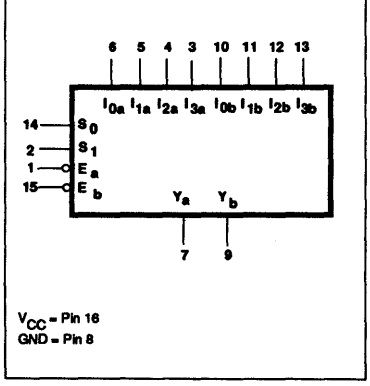
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0a}- I_{3a}	Port A data inputs	1.0/1.0	20µA/0.6mA
I_{0b}- I_{3b}	Port B data inputs	1.0/1.0	20µA/0.6mA
S_0, S_1	Common Select inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_a$	Port A Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{E}_b$	Port B Enable input (active Low)	1.0/1.0	20µA/0.6mA
Y_a, Y_b	Port A, B data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

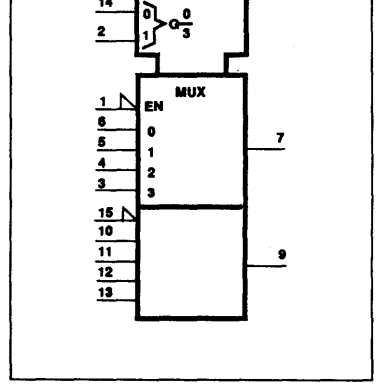
PIN CONFIGURATION



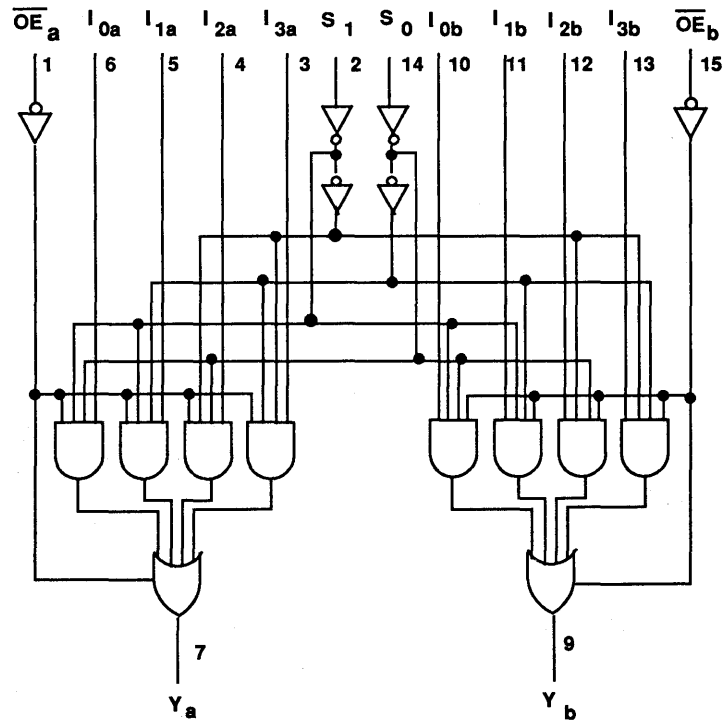
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUT
S_0	S_1	$\overline{E}_n$	I_{0n}	I_{1n}	I_{2n}	I_{3n}	Y_n
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{E}_n$=GND, S_n=I_n=4.5V		12	20	mA
		I_{CCL}		$\overline{E}_n$=S_n=I_n=GND		12	20	mA

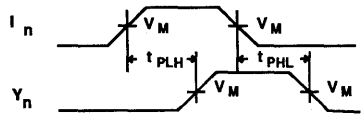
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

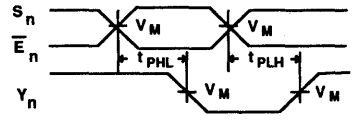
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	Waveform 1	3.0 3.0	4.5 5.0	7.0 7.5	2.5 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y_n	Waveform 2	5.0 5.0	8.0 8.0	10.5 10.5	4.5 4.5	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Y_n	Waveform 2	5.0 4.0	7.5 5.5	9.0 7.0	4.5 3.5	10.5 8.0	ns

AC WAVEFORMS



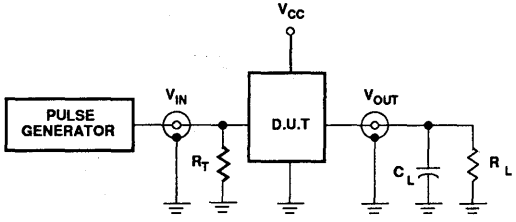
Waveform 1. Propagation Delay, Data to Output



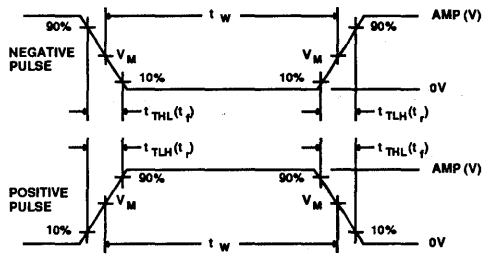
Waveform 2. Propagation Delay, Enable and Select to Output

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F154
Decoder/Demultiplexer

FAST Products

1-of-16 Decoder/Demultiplexer
Product Specification

FEATURES
- **16-line demultiplexing capability**
- **Mutually exclusive outputs**
- **2-input enable gate for strobing or expansion**

DESCRIPTION

The 74F154 decoder accepts four active High binary address inputs and provides 16 mutually exclusive active Low outputs. The 2-input Enable ($\overline{E}_0$, $\overline{E}_1$) gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for expansion of the decoder. The Enable gate has two AND'ed inputs which must be Low to enable the outputs.

The 74F154 can be used as a 1-of-16 demultiplexer by using one of the Enable inputs as the multiplexed data input. When the other Enable is Low, the addressed output will follow the state of the applied data.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F154	5.5 ns	26mA

ORDERING INFORMATION

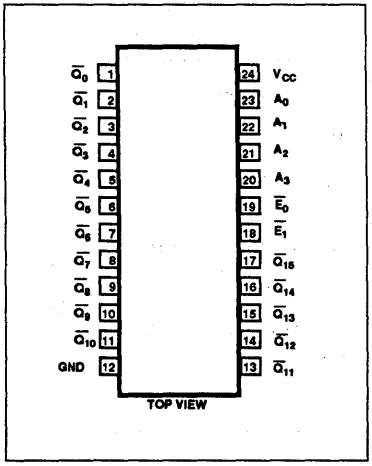
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F154N
24-Pin Plastic SOL	N74F154D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

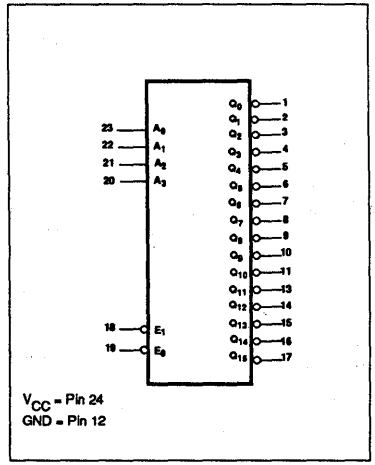
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_0$, $\overline{E}_1$	Enable inputs	1.0/1.0	20µA/0.6mA
$\overline{O}_0$ - $\overline{O}_{15}$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

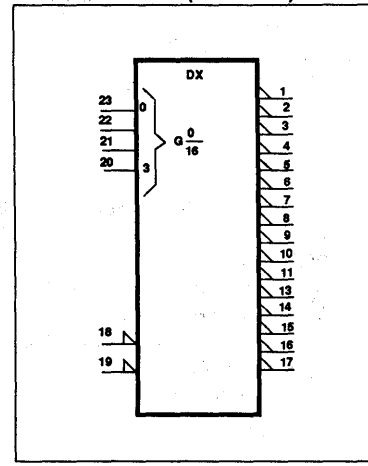
PIN CONFIGURATION



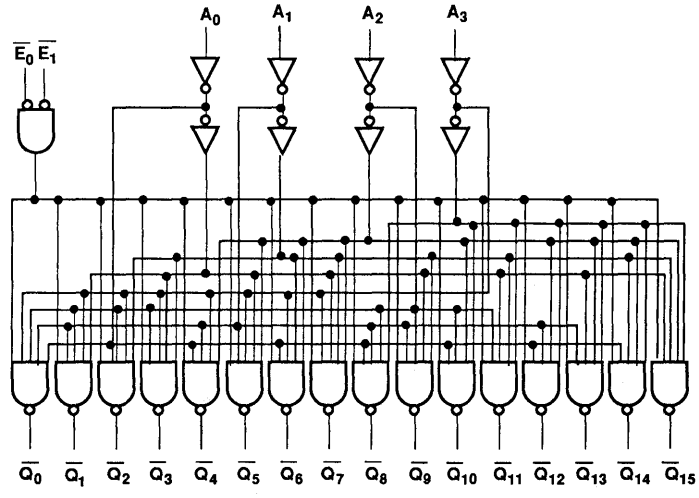
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC}=pin 24
GND=pin 12

FUNCTION TABLE

INPUTS						OUTPUTS													
$\overline{E}_0$	$\overline{E}_1$	A_0	A_1	A_2	A_3	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$	$\overline{Q}_8$	$\overline{Q}_9$	$\overline{Q}_{10}$	$\overline{Q}_{11}$	$\overline{Q}_{12}$	$\overline{Q}_{13}$	$\overline{Q}_{14}$	$\overline{Q}_{15}$
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

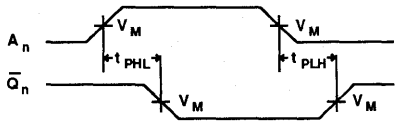
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			26	40	mA
		I_{CCL}				35	45	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

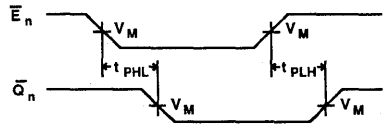
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Q}_n$	Waveform 1	2.0 3.5	5.0 6.5	9.5 10.0	1.5 3.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to $\overline{Q}_n$	Waveform 2	2.0 4.0	4.0 6.0	7.5 9.0	1.5 3.5	8.0 9.5	ns

AC WAVEFORMS



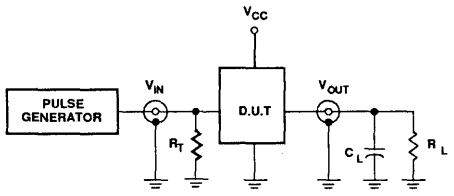
Waveform 1. Propagation Delay For Address To Output



Waveform 2. Propagation Delay For Enable To Output

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



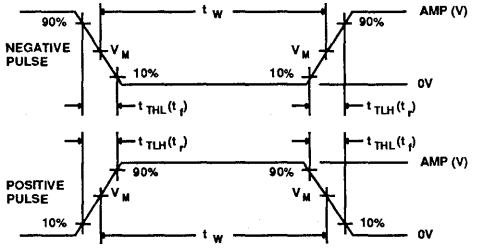
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F157, 74F157A 74F158, 74F158A

Data Selectors/Multiplexers

FAST Products

74F157/157A Quad 2-Input Data Selector/ Multiplexer, Non-Inverting
74F158/158A Quad 2-Input Data Selector/Multiplexer, Inverting

Product Specification

DESCRIPTION

The 74F157/74F157A is a high speed Quad 2-input multiplexer which selects 4 bits of data from one of two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active when Low. When $\overline{E}$ is High, all of the outputs (Y_n) are forced Low regardless of all other input conditions.

Moving data from two registers to a common output bus is a common use of the 'F157/157A. The state of the Select input determines the particular register from which the data comes.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

The 74F158/74F158A is similar but has inverting outputs ($\overline{Y}_n$).

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F157	4.6ns	15mA
74F158	3.7ns	10mA
74F157A	4.6ns	15mA
74F158A	3.7ns	10mA

ORDERING INFORMATION

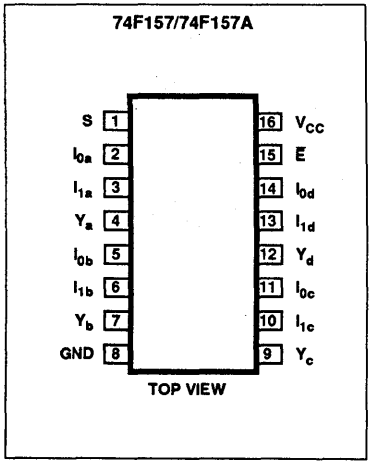
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-pin Plastic DIP	N74F157N, N74F157AN, N74F158N, N74F158AN
16-pin Plastic SO	N74F157D, N74F157AD, N74F158D, N74F158AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

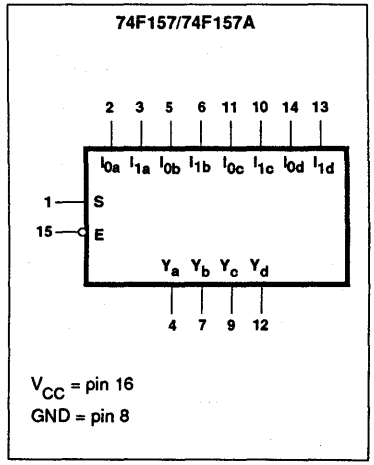
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{na}, I_{nb}, I_{nc}, I_{nd}	Data inputs	1.0/1.0	20µA/0.6mA
S	Select input	1.0/1.0	20µA/0.6mA
$\overline{E}$	Enable input	1.0/1.0	20µA/0.6mA
Y_a - Y_d	Data outputs ('F157/'F157A)	50/33	1.0mA/20mA
$\overline{Y}_a$ - $\overline{Y}_d$	Data outputs ('F158/'F158A)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

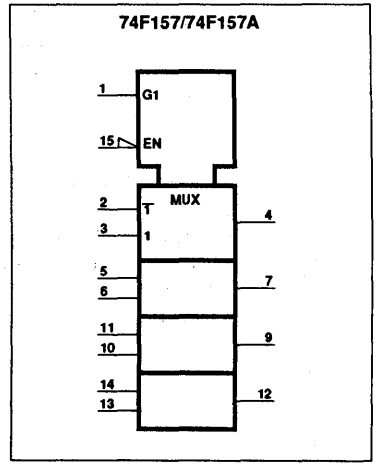
PIN CONFIGURATION



LOGIC SYMBOL

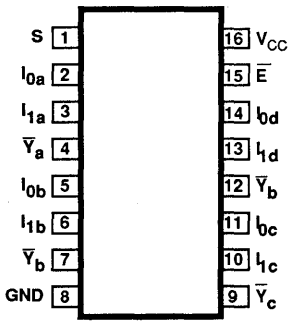


LOGIC SYMBOL(IEEE/IEC)



PIN CONFIGURATION

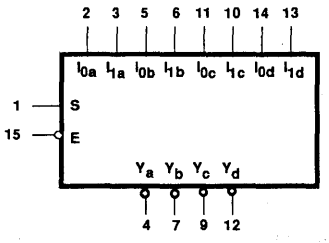
74F158/158A



TOP VIEW

LOGIC SYMBOL

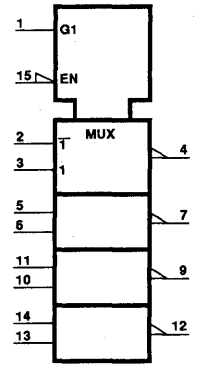
74F158/158A



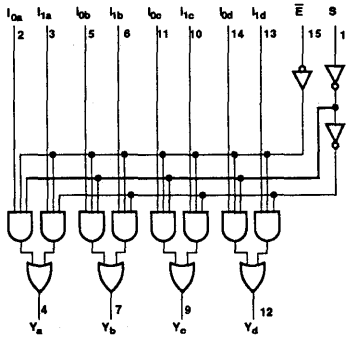
V_{CC} = pin 16
GND = pin 8

LOGIC SYMBOL(IEEE/IEC)

74F158/158A

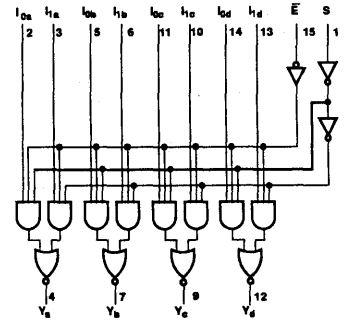


LOGIC DIAGRAM, 74F157/157A



V_{CC} = pin 16
GND = pin 8

LOGIC DIAGRAM, 74F158/158A



V_{CC} = pin 16
GND = pin 8

FUNCTION TABLE, 74F157/157A

INPUTS				OUTPUT
$\overline{E}$	S	I_{0n}	I_{1n}	Y_n
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE, 74F158/158A

INPUTS				OUTPUT
$\overline{E}$	S	I_{0n}	I_{1n}	$\overline{Y}_n$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[4] (total)	'F157/157A	V_{CC} = MAX			15.0	23.0	mA
		'F158/158A				14.0	19.0	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

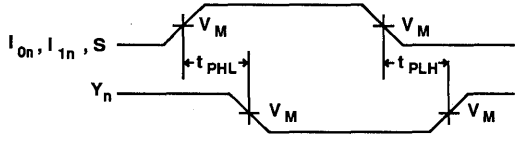
AC ELECTRICAL CHARACTERISTICS for 74F157 and 74F158

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_{0n}, I_{1n} to Y_n	74F157	Waveform 1	3.5 2.5	4.5 3.5	7.0 5.5	3.0 1.5	8.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y_n		Waveform 3	5.0 3.8	7.5 5.0	10.0 7.0	5.0 3.8	11.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S to Y_n		Waveform 1	4.5 3.5	8.0 6.0	13.0 8.0	4.5 3.5	15.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay I_{0n}, I_{1n} to $\overline{Y}_n$	74F158	Waveform 2	3.0 1.5	4.0 2.5	5.9 4.5	2.5 1.0	7.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}_n$		Waveform 4	4.5 3.5	6.0 5.5	8.0 8.5	4.0 3.5	9.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}_n$		Waveform 2	4.0 4.0	6.5 5.5	8.5 9.0	4.0 3.5	9.5 10.5	ns

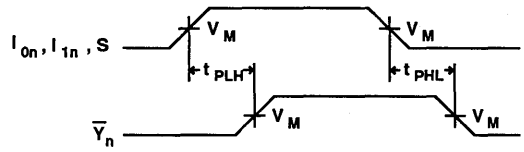
AC ELECTRICAL CHARACTERISTICS for 74F157A and 74F158A

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_{0n}, I_{1n} to Y_n	74F157A	Waveform 1	3.5 2.5	4.5 3.5	6.5 5.0	3.0 1.5	7.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Y_n		Waveform 3	6.0 4.0	7.5 5.0	9.0 6.5	5.5 4.0	10.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay S to Y_n		Waveform 1	5.5 4.5	7.5 6.0	10.0 7.5	5.0 4.0	11.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay I_{0n}, I_{1n} to $\overline{Y}_n$	74F158A	Waveform 2	3.0 1.5	4.0 2.5	6.0 4.0	2.5 1.0	7.0 4.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $\overline{Y}_n$		Waveform 4	4.5 5.0	5.5 6.0	7.0 7.5	4.0 5.0	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}_n$		Waveform 2	4.5 4.0	6.5 5.5	8.5 7.5	4.0 3.5	9.5 8.0	ns

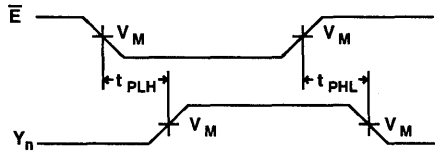
AC WAVEFORMS



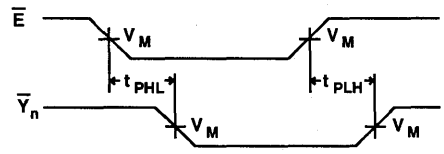
Waveform 1. Propagation Delay For Data And Select To Output



Waveform 2. Propagation Delay For Data And Select To Output



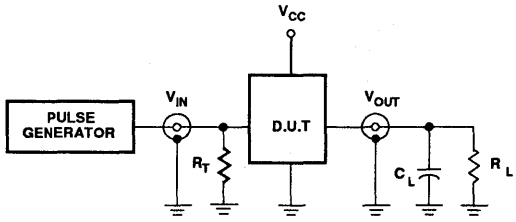
Waveform 3. Propagation Delay For Enable To Output



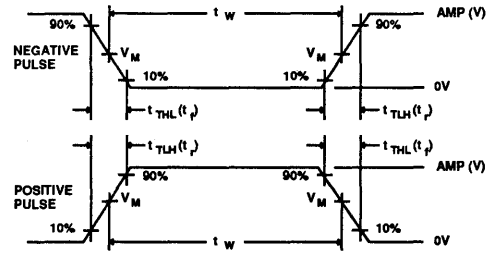
Waveform 4. Propagation Delay For Enable To Output

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F160A,74F161A 74F162A,74F163A Counters

'F160A, 'F162A BCD Decade Counter
'F161A, 'F163A 4-Bit Binary Counter
Product Specification

FAST Products

FEATURES

- **Synchronous counting and loading**
- **Two count enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Asynchronous Master Reset ('F160A, 'F161A)**
- **Synchronous Reset ('F162A, 'F163A)**
- **High speed synchronous expansion**
- **Typical count rate of 130MHz**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F160A,74F161A 74F162A,74F163A	130MHz	46mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic Dip	N74F160AN, N74F161AN, N74F162AN, N74F163AN
16-Pin Plastic SO	N74F160AD, N74F161AD, N74F162AD, N74F163AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
CEP	Count Enable Parallel input	1.0/1.0	20µA/0.6mA
CET	Count Enable Trickle input	1.0/2.0	20µA/1.2mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/2.0	20µA/1.2mA
$\overline{MR}$	Asynchronous Master Reset input (active Low) for 'F160A and 'F161A	1.0/1.0	20µA/0.6mA
$\overline{SR}$	Synchronous Reset input (active Low) for 'F162A and 'F163A	1.0/1.0	20µA/0.6mA
TC	Terminal count output	50/33	1.0mA/20mA
Q_0 - Q_3	Flip-flop outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

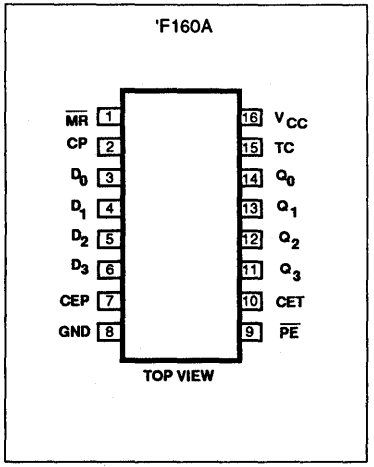
DESCRIPTION

Synchronous presettable decade ('F160A, 'F162A) and 4-bit binary('F161A, 'F163A) counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The clock input is buffered.

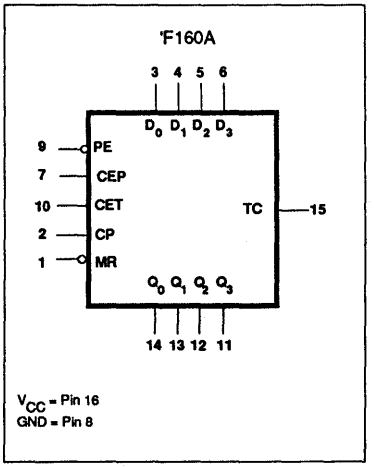
The outputs of the counters may be preset to High or Low level. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D_0-D_3 inputs to be loaded into the counter on the positive-going edge of the clock (provided that the setup and hold requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Master Reset ($\overline{MR}$) input sets all the four outputs of the flip-flops (Q_0-Q_3) in 'F160A and 'F161A to Low levels, regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function). For the 'F162A/'F163A the clear function is synchronous. A Low level at the Synchronous Reset ($\overline{SR}$) input sets all four outputs of the flip-flops (Q_0-Q_3) to Low levels after the next positive-going transition on the clock (CP) input (provided that the setup and hold time requirements for $\overline{SR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. The synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure A). The carry look-ahead simpli-

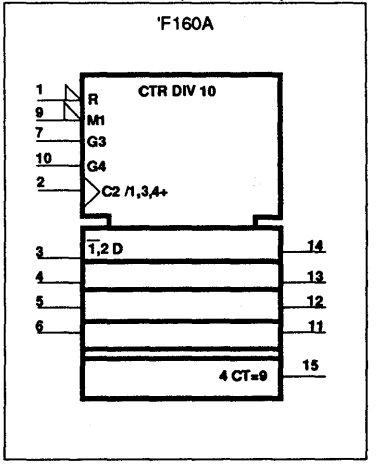
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

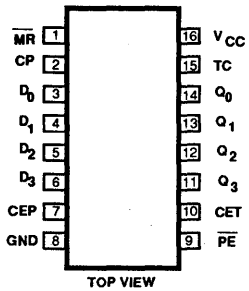


Counters

FAST 74F160A,74F161A,74F162A,74F163A

PIN CONFIGURATION

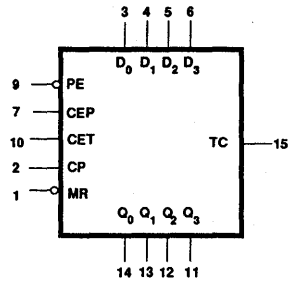
'F161A



TOP VIEW

LOGIC SYMBOL

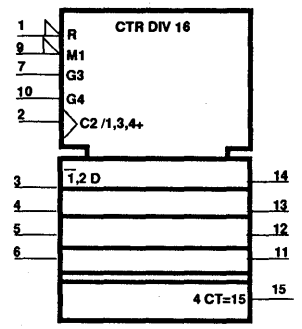
'F161A



V_{CC} = Pin 16
GND = Pin 8

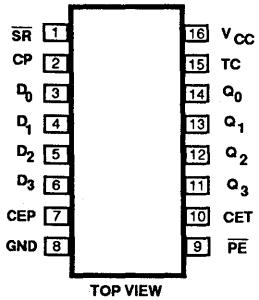
LOGIC SYMBOL(IEEE/IEC)

'F161A



PIN CONFIGURATION

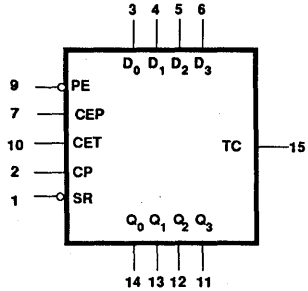
'F162A



TOP VIEW

LOGIC SYMBOL

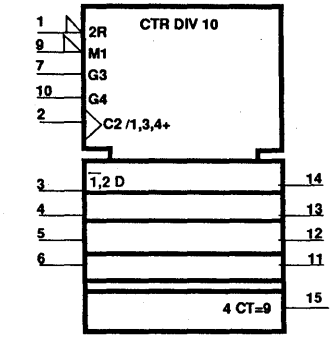
'F162A



V_{CC} = Pin 16
GND = Pin 8

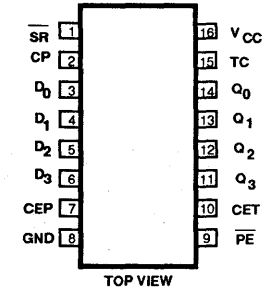
LOGIC SYMBOL(IEEE/IEC)

'F162A



PIN CONFIGURATION

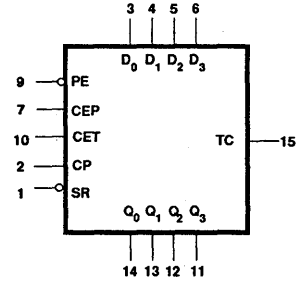
'F163A



TOP VIEW

LOGIC SYMBOL

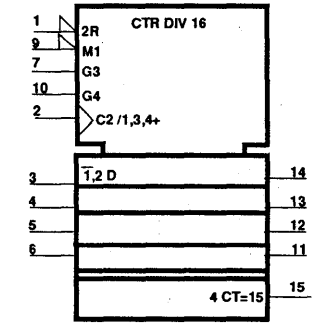
'F163A



V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)

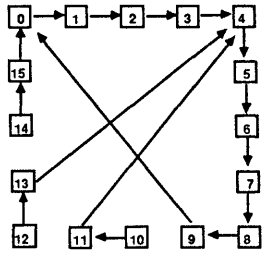
'F163A



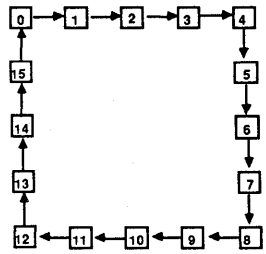
fies serial cascading of the counters. Both Count Enable (CEP and CET) inputs must be High to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q_0. This pulse can be used to enable the next cascaded stage (see Figure B). The TC output is subjected to decoding spikes due to internal race conditions. Therefore, it is not recommended for use as clock or asynchronous reset for flip-flops, registers, or counters.

STATE DIAGRAM

Logic equations: Count Enable=CEP•CET•$\overline{PE}$
$TC=Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3 \cdot CET$
'F160A, 'F162A



Logic equations: Count Enable=CEP•CET•$\overline{PE}$
$TC=Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CET$
'F161A,'F163A



APPLICATIONS

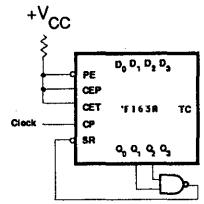


Fig. A Maximum count modifying scheme
Terminal count = 6

H H = Enable count
or
L L = Disable count

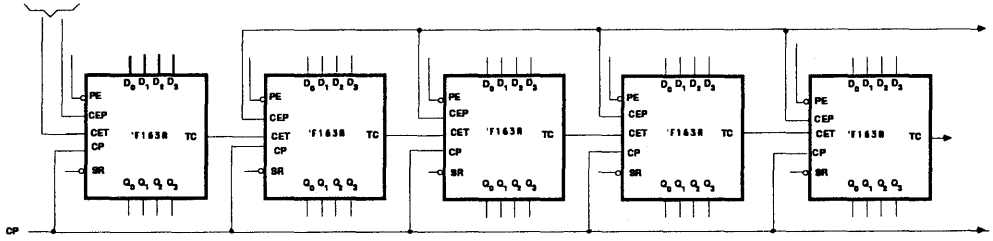


Fig. B Synchronous multistage counting scheme

MODE SELECT-FUNCTION TABLE for 'F160A, 'F161A

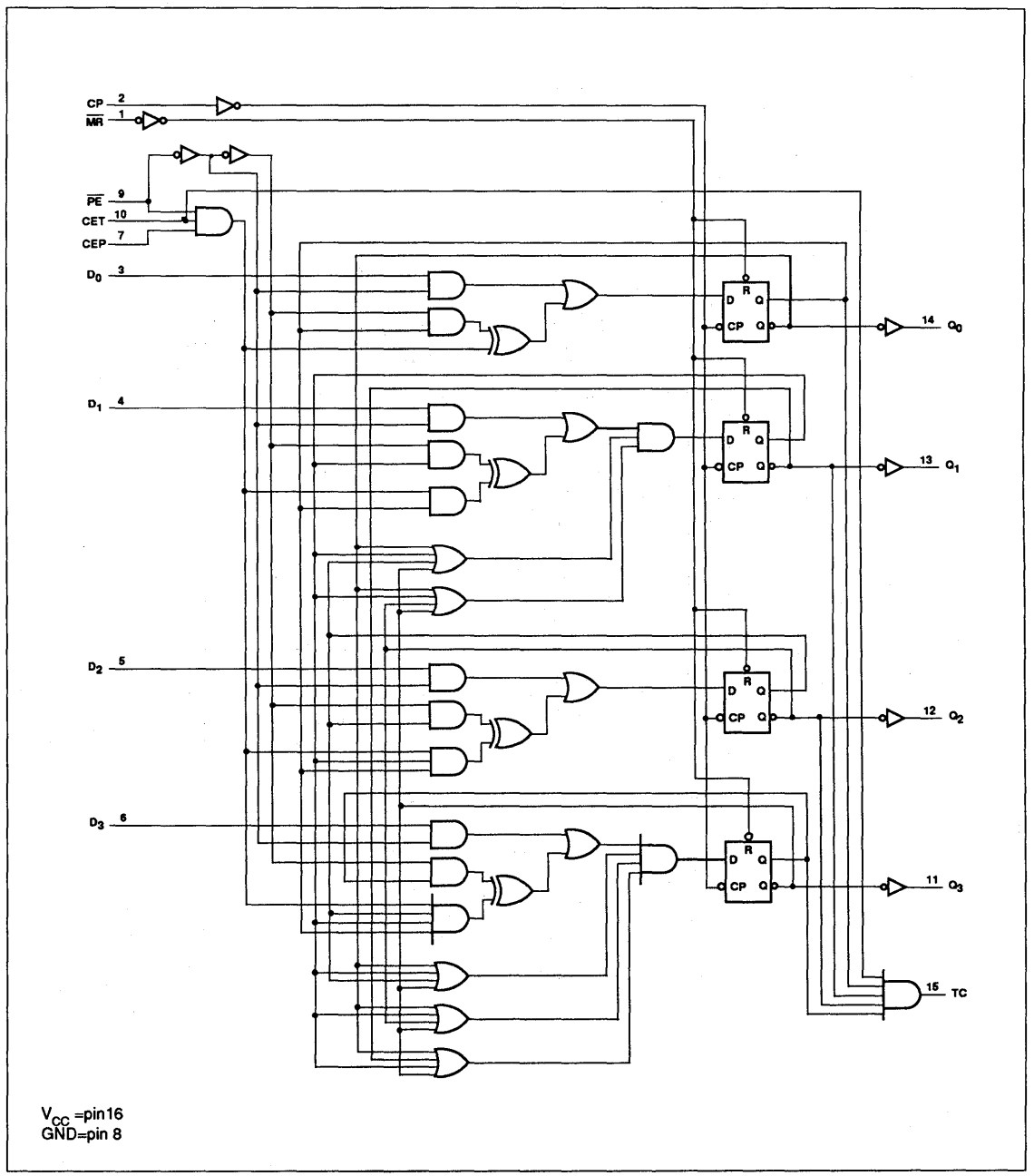
INPUTS						OUTPUTS		OPERATING MODE
$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC	
L	X	X	X	X	X	L	L	Reset (clear)
H	↑	X	X	l	l	L	L	Parallel load
H	↑	X	X	l	h	H	(1)	
H	↑	h	h	h	X	count	(1)	Count
H	X	l	X	h	X	q_n	(1)	Hold (do nothing)
H	X	X	l	h	X	q_n	L	

MODE SELECT-FUNCTION TABLE for 'F162A, 'F163A

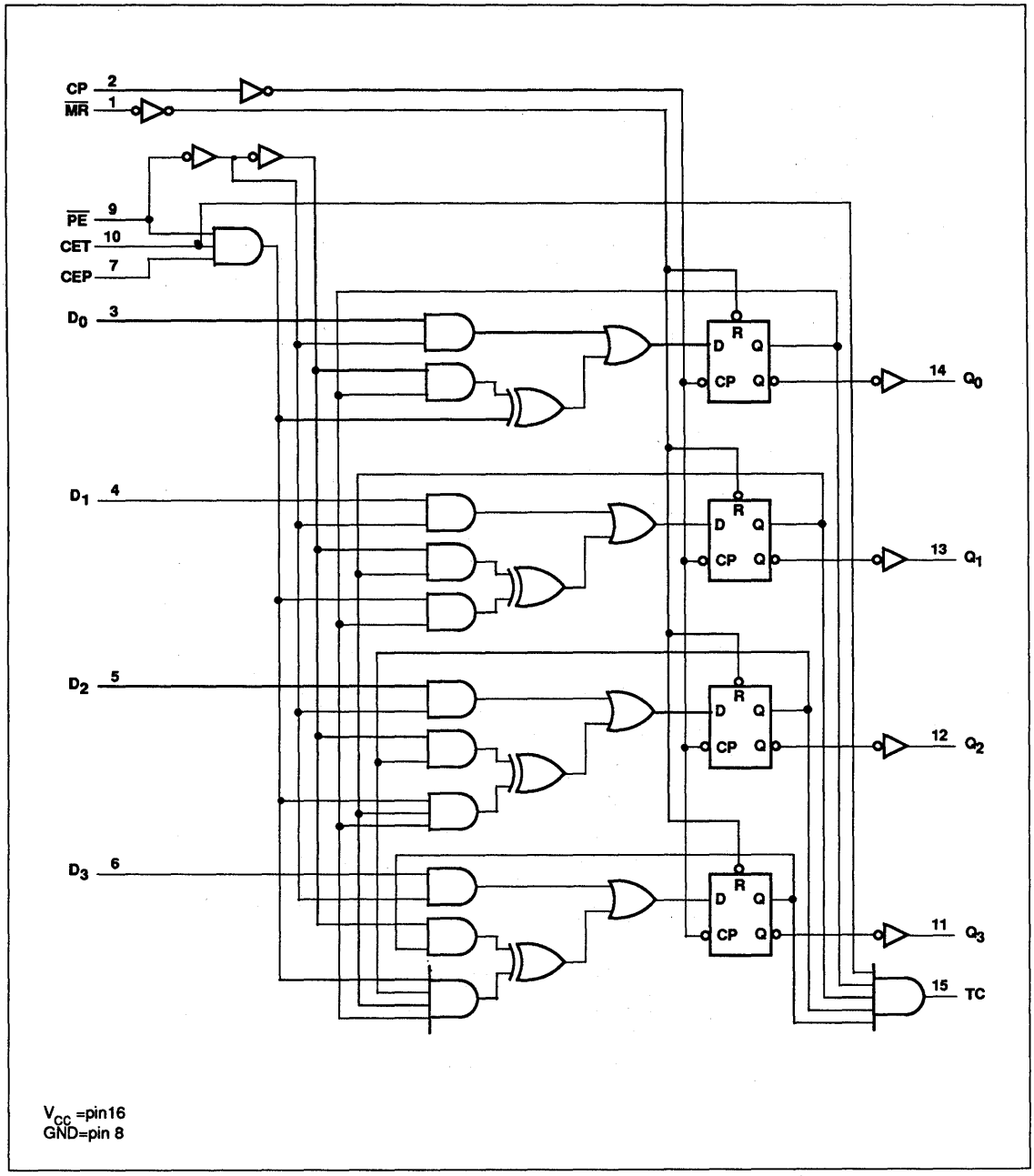
INPUTS						OUTPUTS		OPERATING MODE
$\overline{SR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC	
l	↑	X	X	X	X	L	L	Reset (clear)
h	↑	X	X	l	l	L	L	Parallel load
h	↑	X	X	l	h	H	(2)	
h	↑	h	h	h	X	count	(2)	Count
h	X	l	X	h	X	q_n	(2)	Hold (do nothing)
h	X	X	l	h	X	q_n	L	

H = High voltage level
h = High voltage level one setup prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup prior to the Low-to-High clock transition
q_n = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
(1) = The TC output is High when CET is High and the counter is at Terminal Count (HLLH for 'F160A and HHHH for 'F161A)
(2) = The TC output is High when CET is High and the counter is at Terminal Count (HLLH for 'F162A and HHHH for 'F163A)

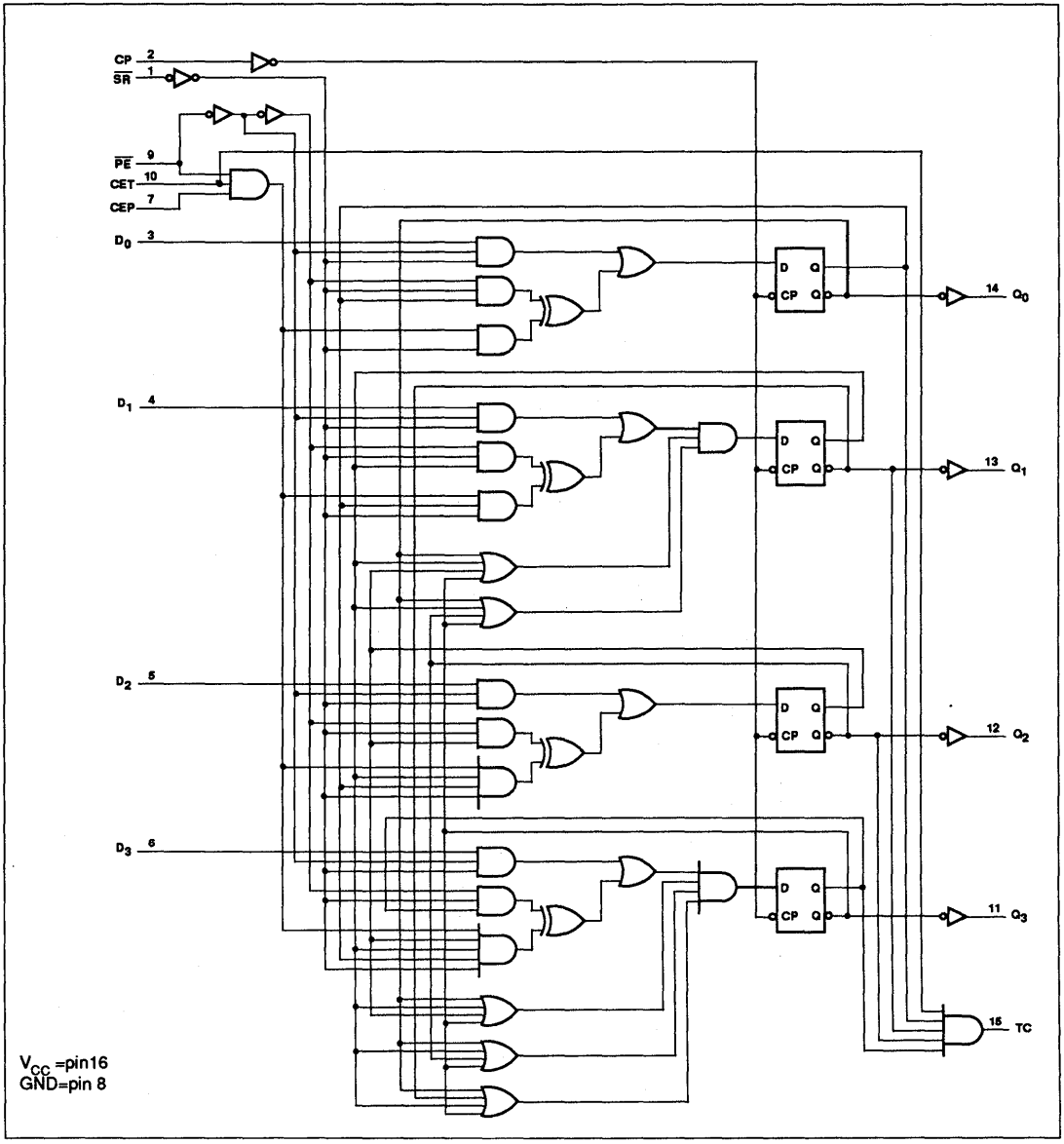
LOGIC DIAGRAM for 'F160A



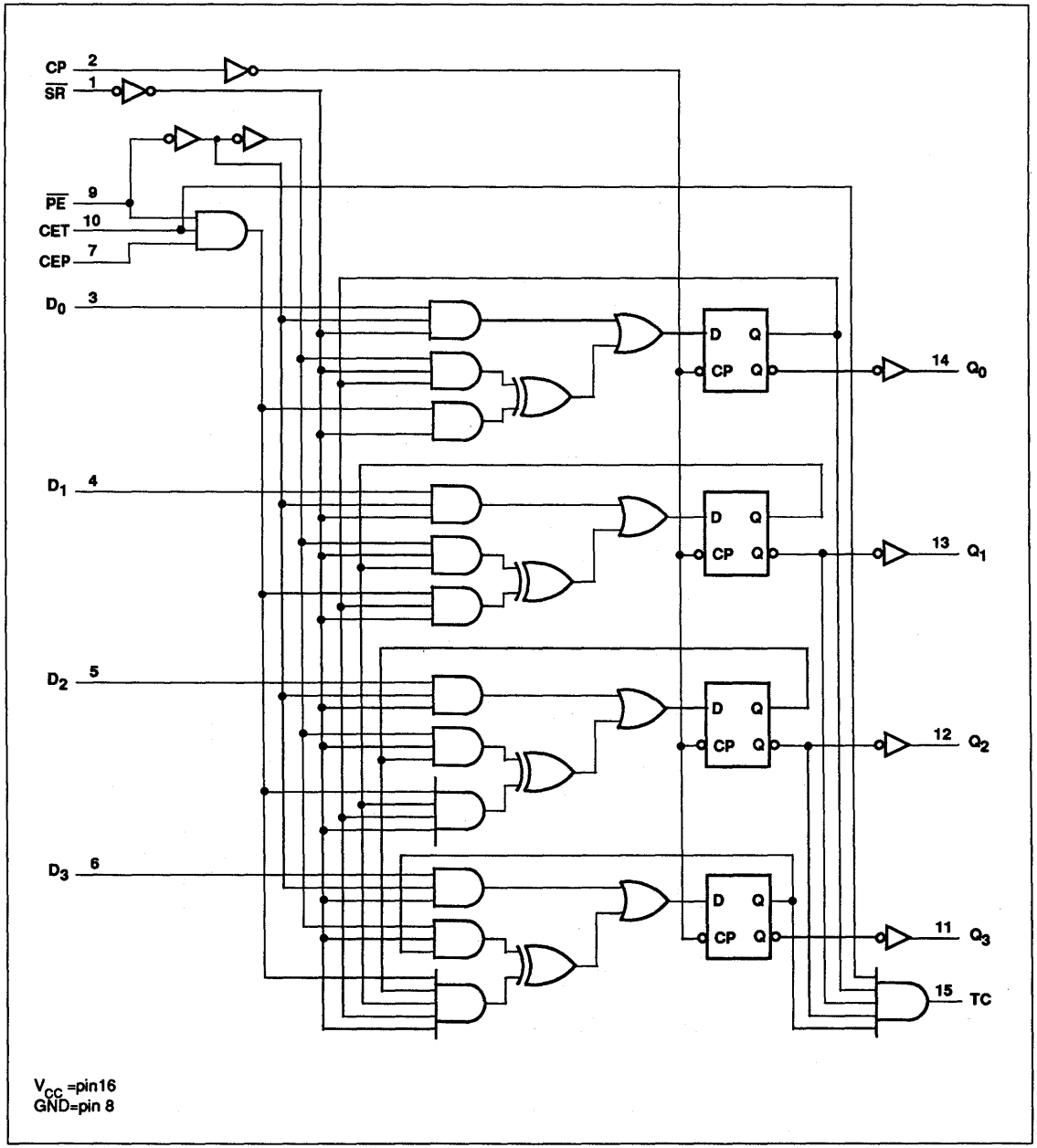
LOGIC DIAGRAM for 'F161A



LOGIC DIAGRAM for 'F162A



LOGIC DIAGRAM for 'F163A



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	CET, $\overline{PE}$	V_{CC} = MAX, V_I = 0.5V				-1.2	mA
		others					-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			42	55	mA
		I_{CCL}				49	65	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 74F160A and 74F162A

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	100	130		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$=High)		Waveform 1	2.0 4.0	4.5 7.0	7.0 10.0	2.0 4.0	8.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$= Low)		Waveform 1	2.0 4.0	4.5 6.0	7.5 8.5	2.0 4.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		Waveform 1	4.5 4.5	8.0 7.5	10.5 9.5	4.5 4.5	11.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC		Waveform 2	1.5 2.5	4.0 5.0	6.5 7.0	1.5 2.5	7.0 7.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	'F160A	Waveform 3	6.5	9.0	12.0	6.5	13.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	'F160A	Waveform 3	6.0	8.0	10.0	5.5	11.0	ns

AC SETUP REQUIREMENTS for 74F160A and 74F162A

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP		Waveform 6	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP		Waveform 6	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	11.0 7.0			11.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low CET or CEP to CP		Waveform 4	11.0 6.0			11.0 7.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CET or CEP to CP		Waveform 4	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width (Load) High or Low		Waveform 1	4.0 5.0			4.0 6.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width (Count) High or Low		Waveform 1	4.0 5.5			4.0 6.5		ns
$t_w(L)$	$\overline{MR}$ pulse width,Low	'F160A	Waveform 3	5.0			5.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	'F160A	Waveform 3	5.0			6.0		ns

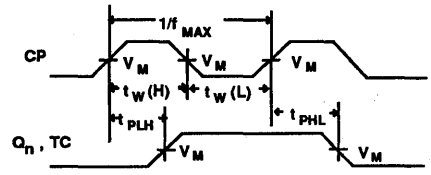
AC ELECTRICAL CHARACTERISTICS for 74F161A and 74F163A

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	100	130		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$=High)		Waveform 1	2.0 4.0	4.0 6.5	6.5 10.0	2.0 4.0	7.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$= Low)		Waveform 1	2.0 3.5	4.5 5.5	6.5 8.5	2.0 3.5	7.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		Waveform 1	5.0 4.5	7.5 7.5	10.5 10.5	5.0 4.0	11.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC		Waveform 2	1.5 2.5	3.5 5.0	6.5 7.5	1.5 2.5	7.0 8.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	'F161A	Waveform 3	6.0	8.5	12.0	5.5	13.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	'F161A	Waveform 3	5.0	8.5	10.0	5.0	11.0	ns

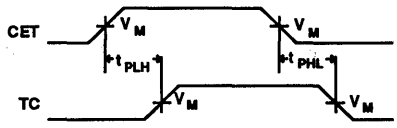
AC SETUP REQUIREMENTS for 74F161A and 74F163A

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP		Waveform 6	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP		Waveform 6	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	9.0 6.5			9.5 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP		Waveform 5 or 6	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low CET or CEP to CP		Waveform 4	10.5 6.0			10.5 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CET or CEP to CP		Waveform 4	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP pulse width (Load) High or Low		Waveform 1	4.0 5.0			4.0 5.5		ns
$t_w(H)$ $t_w(L)$	CP pulse width (Count) High or Low		Waveform 1	4.0 6.0			4.0 7.0		ns
$t_w(L)$	$\overline{MR}$ pulse width,Low	'F161A	Waveform 3	4.5			4.5		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	'F161A	Waveform 3	6.0			6.5		ns

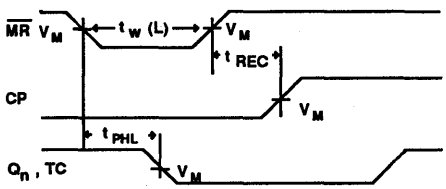
AC WAVEFORMS



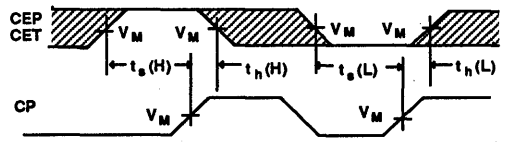
Waveform 1.
Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



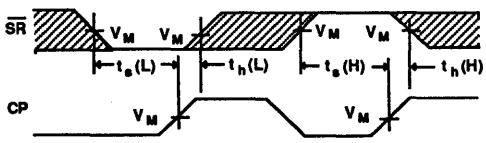
Waveform 2.
Propagation Delay, CET Input to TC Output



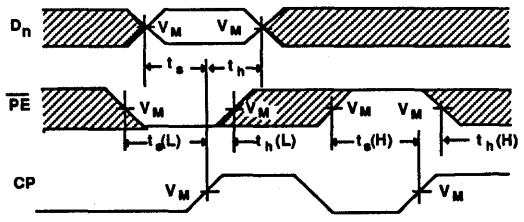
Waveform 3.
Master Reset pulse width, Master Reset to Output Delay and Master Reset to Recovery Time



Waveform 4.
CEP and CET Reset Setup and Hold Times



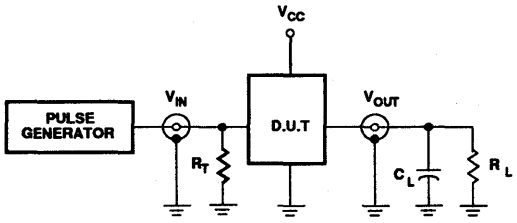
Waveform 5.
Synchronous Reset Setup and Hold Times



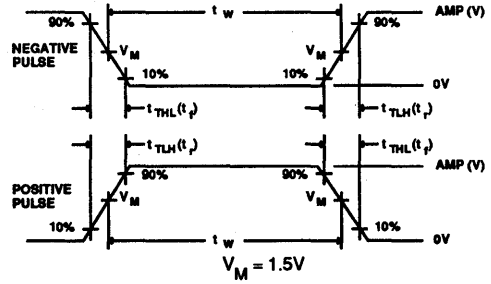
Waveform 6.
Parallel Data and Parallel Enable Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F164
Shift Register

FAST Products

8-Bit Serial-In Parallel-Out Shift Register
Product Specification

FEATURES
- **Gated serial data inputs**
- **Typical shift frequency of 100MHz**
- **Asynchronous Master Reset**
- **Fully buffered clock and data inputs**
- **Fully synchronous data transfers**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F164	100MHz	33mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F164N
14-Pin Plastic SOL	N74F164D

DESCRIPTION

The 74F164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered through one of two inputs (D_{sa}, D_{sb}); either input can be used as an active High enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied High.

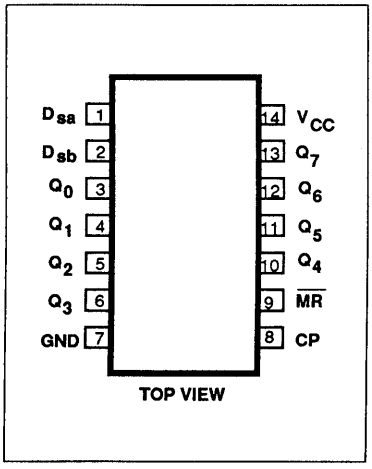
Data shifts one place to the right on each Low-to-High transition of the Clock (CP) input, and enters into Q_0 the logical AND of the the two data inputs (D_{sa}, D_{sb}) that existed one setup time before the rising clock edge. A Low level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

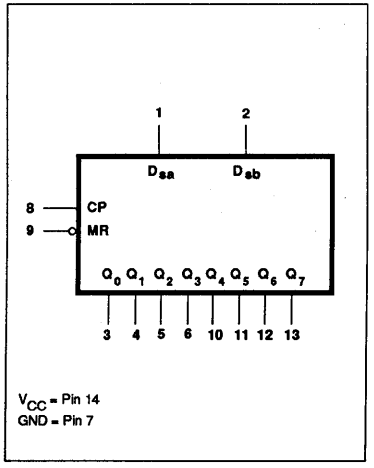
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{sa}, D_{sb}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

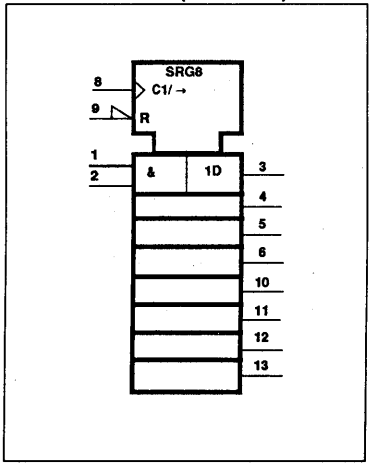
PIN CONFIGURATION



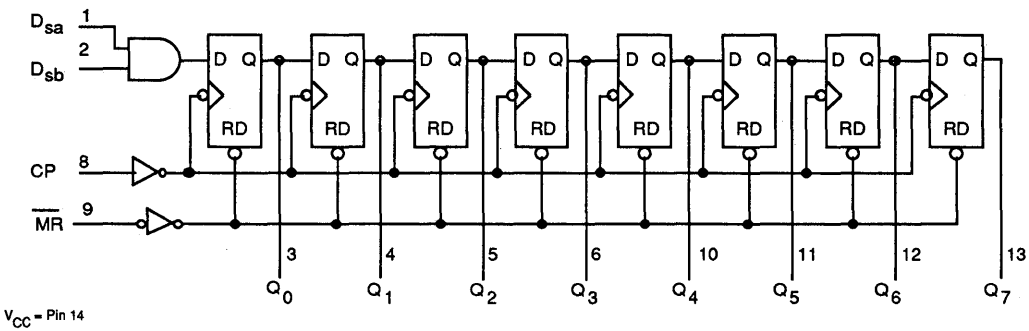
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS			OPERATING MODE
$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	Q_1 ---- Q_7		
L	X	X	X	L	L	L	Reset (clear)
H	↑	l	l	L	q_0	q_6	Shift
H	↑	l	h	L	q_0	q_6	
H	↑	h	l	L	q_0	q_6	
H	↑	h	h	H	q_0	q_6	

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
q_n = Lower case letters indicate the state of the referenced input (or output) on setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

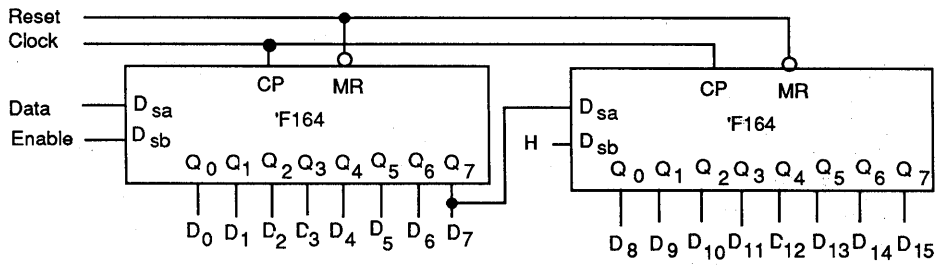
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]	V_{CC} = MAX			33	55	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. Measure I_{CC} with the serial inputs grounded , the clock input at 2.4 V, and a momentary ground, then 4.5V applied to Master Reset, and all outputs open.

APPLICATION



NOTE: The 'F164 can be cascaded to form synchronous shift registers of longer length. Here, two 'F164 are combined to form a 16 bit shift register.

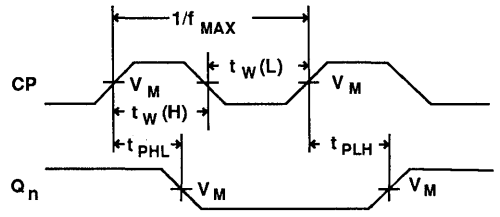
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.0 5.0	5.0 7.0	8.0 10.0	2.5 5.0	9.0 11.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	4.0	7.5	10.5	4.0	11.5	ns

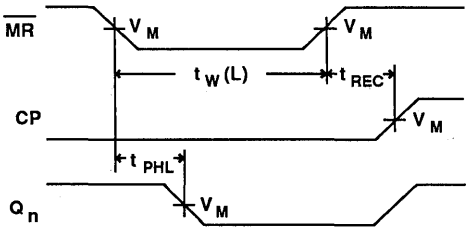
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to CP	Waveform 3	7.0 7.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to CP	Waveform 3	1.0 1.0			2.0 2.0		ns
t_w(H) t_w(L)	CP Pulse width High or Low	Waveform 1	4.0 7.0			4.0 7.0		ns
t_w(L)	$\overline{MR}$ Pulse width Low	Waveform 2	7.0			7.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	7.0			7.0		ns

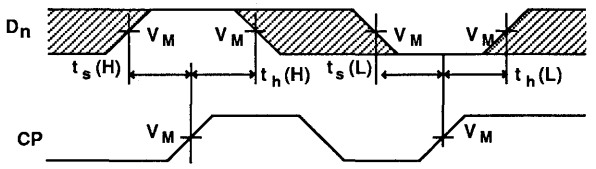
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

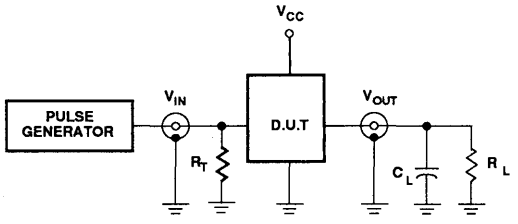


Waveform 3. Data Setup And Hold Times

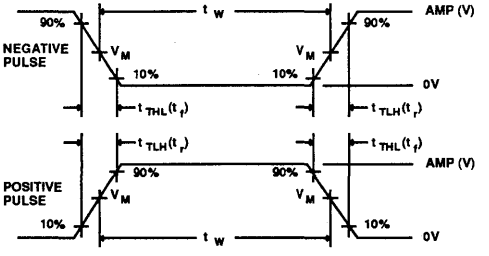
NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F166
Shift Register

FAST Products

8-Bit Bidirectional Universal Shift Register
Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F166	175MHz	50mA

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Synchronous parallel to serial applications**
- **Synchronous serial data input for easy expansion**
- **Clock enable for "do nothing" mode**
- **Asynchronous Master Reset**
- **Expandable to 16 bits in 8-bit increments**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F166N
16-Pin Plastic SO	N74F166D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

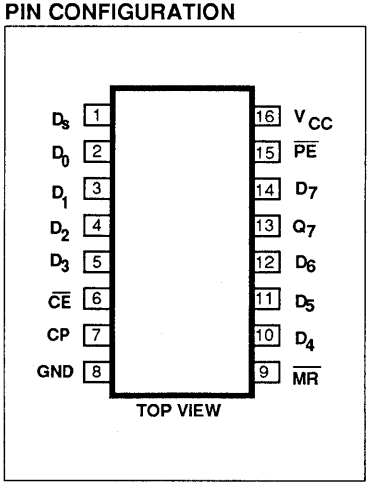
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0-D_7	Parallel data inputs	1.0/0.033	20μA/20μA
D_S	Serial data input (Shift Right)	2.0/0.066	40μA/40μA
CP	Clock input (Active rising edge)	1.0/0.033	20μA/20μA
$\overline{CE}$	Clock Enable input (Active Low)	1.0/0.033	20μA/20μA
$\overline{PE}$	Parallel Enable input (Active Low)	1.0/0.033	20μA/20μA
$\overline{MR}$	Master Reset input (Active Low)	2.0/0.066	40μA/40μA
Q_7	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

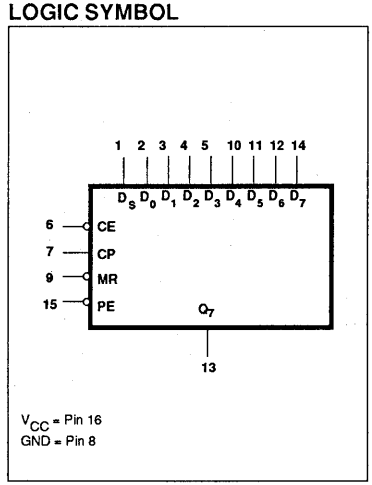
DESCRIPTION

The 74F166 is a high speed 8-bit shift register that has fully synchronous serial parallel data entry selected by an active Low Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ is Low one setup time before the Low-to-High clock transition, parallel data is entered into the register. When $\overline{PE}$ is High, data is entered into internal bit position Q_0 from serial data input (D_s), and the remaining bits are shifted one place to the right (Q_0-Q_1-Q_2, etc.) with each positive going clock transition. For expansion of the register in parallel to serial converters, the Q_7 output is connected to the D_s input of the succeeding stage. The clock input is gated OR structure which allows one input to be used as an active-Low Clock Enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The Low-to-High transition of $\overline{CE}$ input should only take place while the CP is High for predictable operation. A Low on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a Low state.

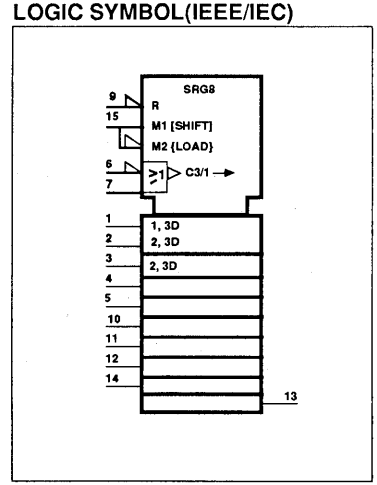
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

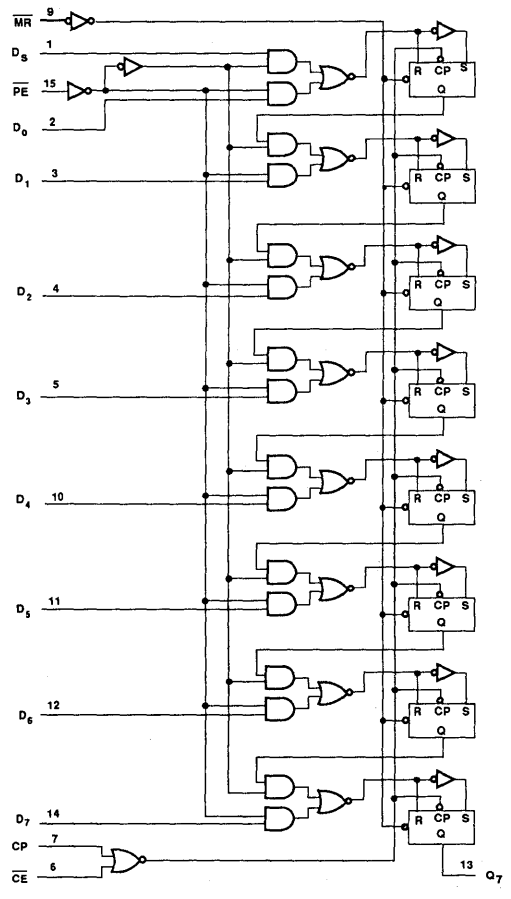


FUNCTION TABLE

INPUTS					Q_n REGISTER		OUTPUT	OPERATING MODE
$\overline{PE}$	$\overline{CE}$	CP	D_s	D_0 - D_7	Q_0	Q_1 - Q_6	Q_7	
l	l	↑	X	l - l	L	L - L	L	Parallel load
l	l	↑	X	h - h	H	H - H	H	
h	l	↑	l	X - X	L	q_0 - q_5	q_6	Serial shift
h	l	↑	h	X - X	H	q_0 - q_5	q_6	
X	h	X	X	X - X	q_0	q_1 - q_6	q_7	Hold (do nothing)

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
q_n = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



V_{CC} = pin 16
GND = pin 8

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V				100	µA
		$\overline{CE}$, CP[3]						
I_{IH}	High-level input current	others	V_{CC} = MAX, V_I = 2.7V				20	µA
		$\overline{MR}$, D_s					40	µA
I_{IL}	Low-level input current	others	V_{CC} = MAX, V_I = 0.5V				-20	µA
		$\overline{MR}$, D_s					-40	µA
I_{OS}	Short circuit output current[4]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX, $\overline{PE}$= $\overline{CE}$=D_n=GND, $\overline{MR}$=D_S=4.5V, CP=↑			50	70	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. When testing CP, $\overline{CE}$ must remain in High state, whereas CP must remain in High state when testing $\overline{CE}$.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

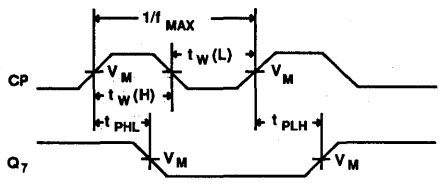
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	135	175		110		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_7	Waveform 1	5.0 4.0	7.5 6.0	10.0 8.0	5.0 3.5	12.0 9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_7	Waveform 2	4.0	6.5	8.5	4.0	9.5	ns

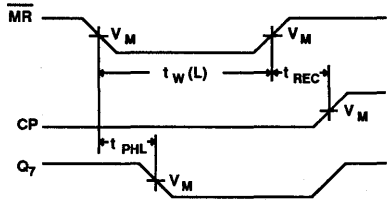
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n, D_s to CP, $\overline{CE}$	Waveform 3	3.0 2.5			4.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n, D_s to CP	Waveform 3	0 0			1.0 0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n, D_s to $\overline{CE}$	Waveform 3	1.5 0			2.0 0		ns
$t_sL)$	Setup time, Low $\overline{CE}$ to CP	Waveform 3	5.0			6.0		ns
$t_h(H)$	Hold time, High $\overline{CE}$ to CP	Waveform 3	0			0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP, $\overline{CE}$	Waveform 3	3.0 3.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP, $\overline{CE}$	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	3.0 4.5			3.5 5.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	4.0			4.5		ns

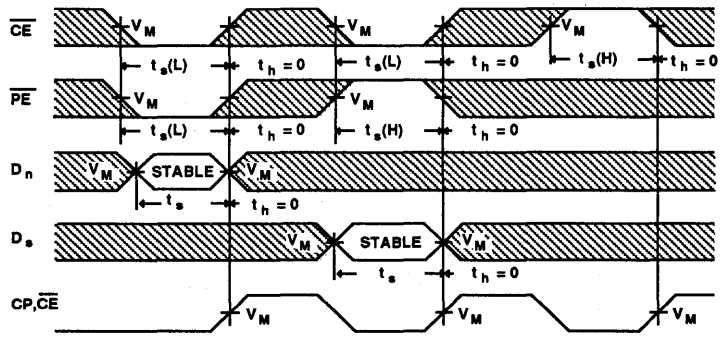
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths, and Maximum Clock Frequency



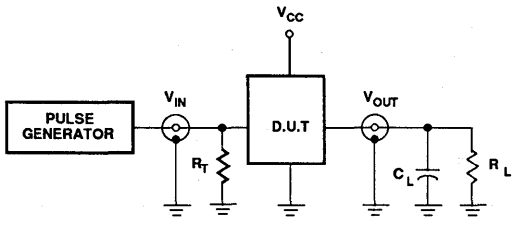
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



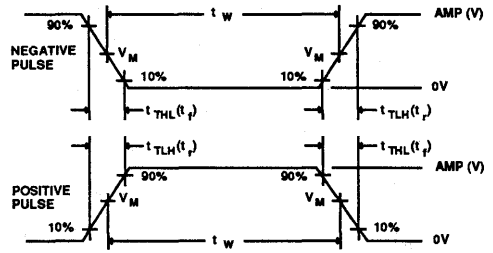
Waveform 3. Setup Time and Hold Time

NOTES: 1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.
3. $\overline{CE}$ may change only from High to Low while CP is Low

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F168, 74F169 Counters

74F168 4-Bit Up/Down Decade Synchronous Counter
74F169 4-Bit Up/Down Binary Synchronous Counter
Product Specification

FAST Products

FEATURES

- **Synchronous counting and loading**
- **Up/down counting**
- **BCD decade counter- 'F168**
- **Modular 16 binary counter- 'F169**
- **Two Count Enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Built-in lookahead carry capability**
- **Presettable for programmable operation**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F168	115MHz	35mA
74F169	115MHz	35mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic Dip	N74F168N, N74F169N
16-Pin Plastic SO	N74F168D, N74F169D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Parallel data inputs	1.0/1.0	20µA/0.6mA
$\overline{CEP}$	Count Enable parallel input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/2.0	20µA/1.2mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/1.0	20µA/0.6mA
U/$\overline{D}$	Up/Down count control input	1.0/1.0	20µA/0.6mA
Q_0 -Q_3	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{TC}$	Terminal count output (active Low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

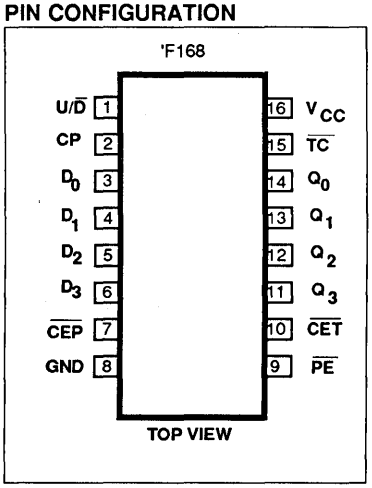
The 74F168 and 74F169 are 4-bit synchronous Up/Down Counters. The 74F168 is a synchronous, presettable BCD Decade Up/Down Counter featuring an internal carry look-ahead for applications in high speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the flip-flops on the Low-to-High transition of the clock. The counter is fully programmable; that is, the outputs may be preset to either level.

Presetting is synchronous with the clock and takes place regardless of the levels of the Count Enable inputs. A Low level on the Parallel Enable ($\overline{PE}$) input disables the counter causes the data at the D_n input to be loaded into the counter on the next Low-to-High transition of the clock.

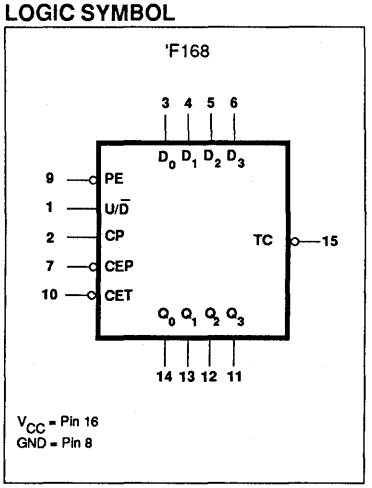
The direction of the counting is controlled by the by the Up/Down (U/$\overline{D}$) input; a High will cause the count to increase, a Low will cause the count to decrease.

The carry look ahead circuitry is provided for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enables($\overline{CEP}$, $\overline{CET}$) inputs and a Terminal Count ($\overline{TC}$) output. Both Count Enable inputs must be Low to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output thus enabled will produce a Low output pulse with a duration approximately equal the High level portion of Q_0 output. The Low level $\overline{TC}$ pulse is used to enable successive cascaded stages. See Figure 1 for the fast synchronous multistage counting connections. The 74F169 is identical except that it is a Modula 16 counter.

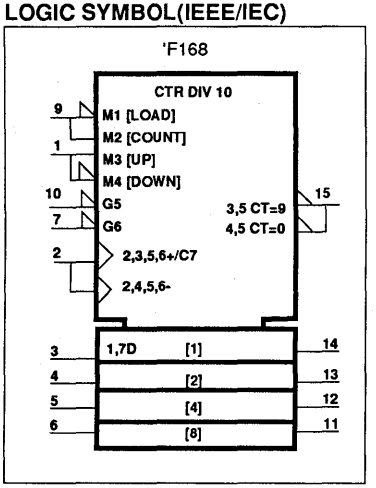
PIN CONFIGURATION



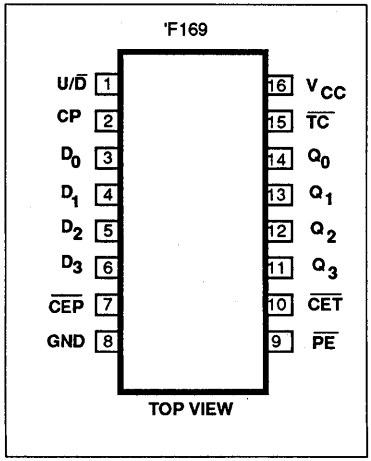
LOGIC SYMBOL



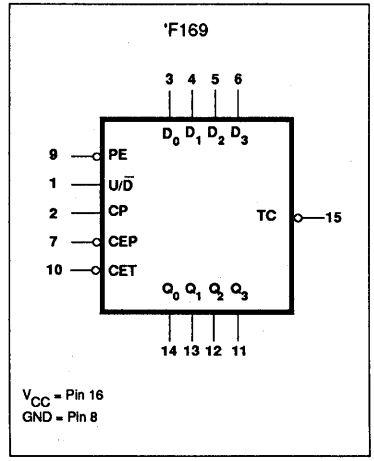
LOGIC SYMBOL(IEEE/IEC)



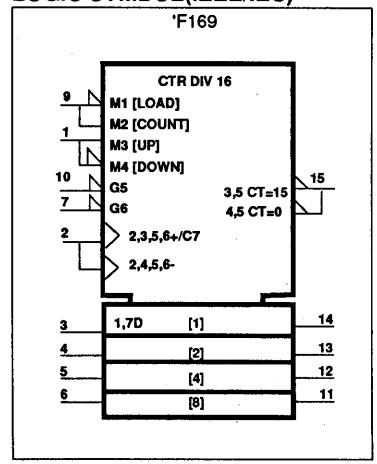
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



FUNCTIONAL DESCRIPTION

The 'F168 and 'F169 use edge triggered J-K type flip-flops and have no constraints on changing the control or data input signals in either state of the clock. The only requirement is that the various inputs attain the desired state at least a set-up time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedance over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is Low, the data on the D_0-D_3 inputs enter the flip-flops on the next rising edge of the clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be Low and $\overline{PE}$ must be High; the U/$\overline{D}$ input determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally High and goes Low, provided that $\overline{CET}$ is Low. When a counter reaches zero in the count down mode or reaches 9 (15 for 'F169) in the count up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel($\overline{CEP}$) input level. The $\overline{TC}$ output of the 'F168 decade counter can also be Low in the illegal states 11, 13, 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the 'F168 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (See logic equations below).

1) Count Enable= $\overline{CEP}\cdot\overline{CET}\cdot\overline{PE}$
2) Up: $\overline{TC}=Q_0\cdot Q_3\cdot(U/\overline{D})\cdot\overline{CET}$
3) Down: $\overline{TC}=\overline{Q_0}\cdot\overline{Q_1}\cdot\overline{Q_2}\cdot\overline{Q_3}\cdot(U/\overline{D})\cdot\overline{CET}$

MODE SELECT-FUNCTION TABLE

INPUTS						OUTPUTS		OPERATING MODE
CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$	
↑	X	X	X	l	l	L	(1)	Parallel load (Dn → Qn)
↑	X	X	X	X	X	H	(1)	
↑	h	l	l	h	X	Count up	(1)	Count up (increment)
↑	l	l	l	h	X	Count down	(1)	Count down (decrement)
↑	X	h	X	h	X	q_n	(1)	Hold (do nothing)
↑	X	X	X	h	X	q_n	H	

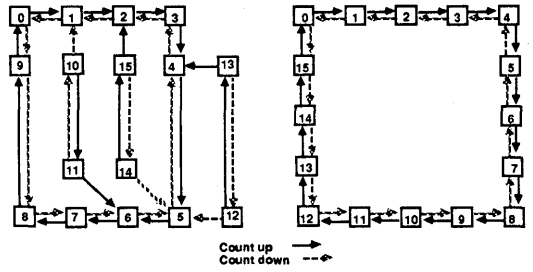
H = High voltage level
h = High voltage level one setup prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup prior to the Low-to-High clock transition
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
(1) = $\overline{TC}$ is Low when $\overline{CET}$ is Low and the counter is at Terminal Count.
The Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL) for 'F168.
The Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for 'F169.

MODE SELECT TABLE

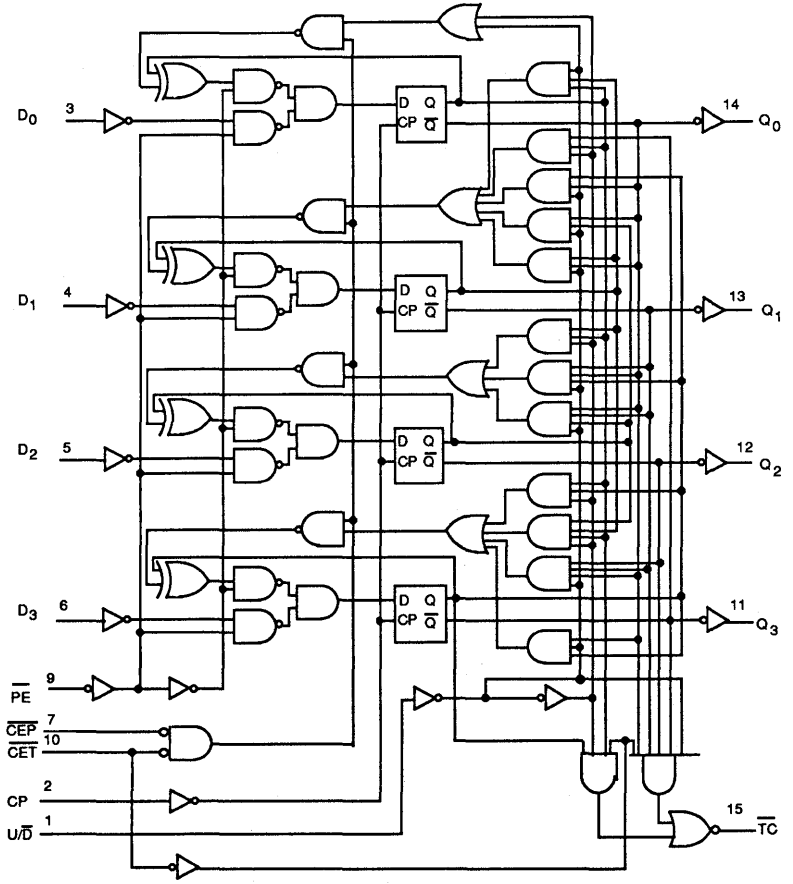
INPUTS				OPERATING MODE
$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	
L	X	X	X	Load (Dn → Qn)
H	L	L	H	Count up (increment)
H	L	L	L	Count down (decrement)
H	H	X	X	No change (Hold)
H	X	H	X	No change (Hold)

H = High voltage level
L = Low voltage level
X = Don't care

STATE DIAGRAM

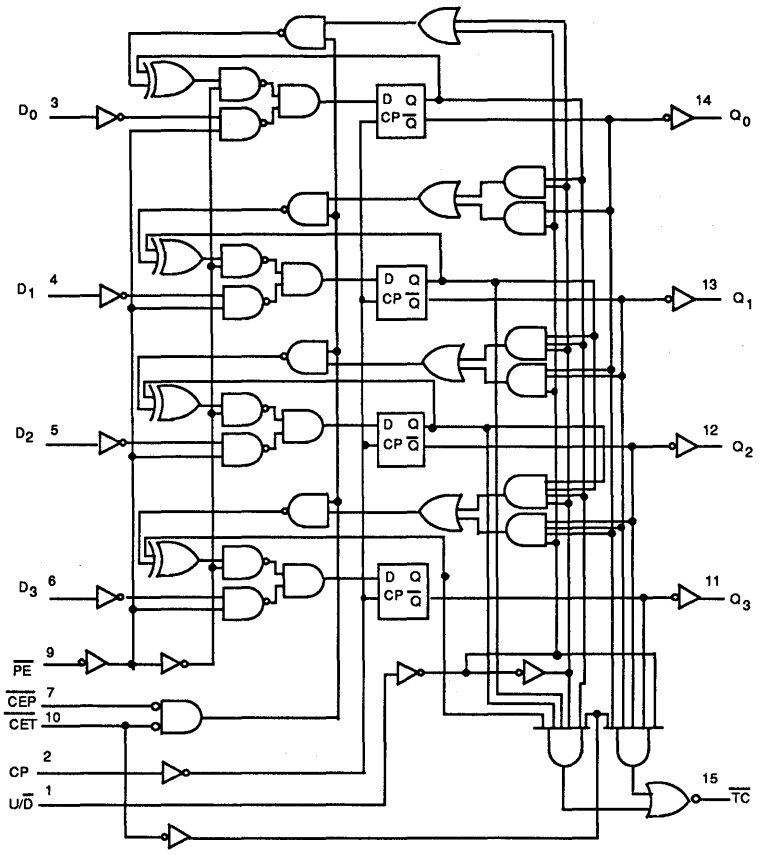


LOGIC DIAGRAM for'F168



V_{CC} =pin16
GND=pin 8

LOGIC DIAGRAM for 'F169



V_{CC} =pin16
GND=pin 8

APPLICATION

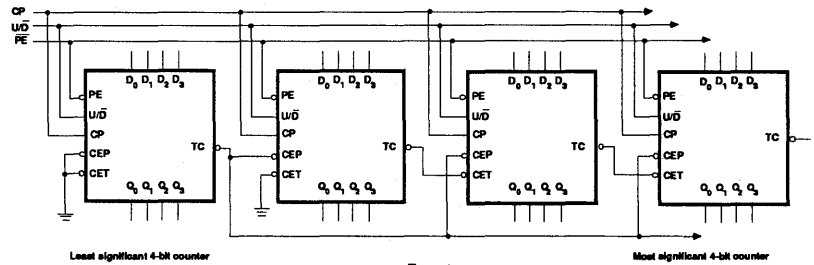


Figure 1
Synchronous multistage counting scheme

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	$\overline{CET}$	V_{CC} = MAX, V_I = 0.5V				-1.2	mA
		others					-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			35	52	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with after applying a momentary 4.5V, then ground to the clock input with all other inputs grounded and all outputs open.

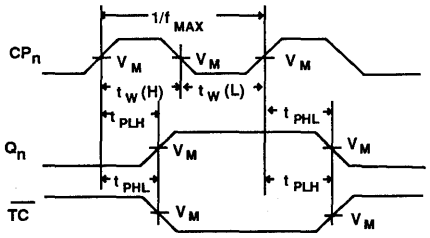
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$, High or Low)		Waveform 1	3.0 4.0	6.5 9.0	8.5 11.5	3.0 4.0	9.5 13.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$		Waveform 1	5.5 4.0	12.0 8.5	15.5 11.0	5.5 4.0	17.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$		Waveform 2	2.5 2.5	4.5 6.0	6.0 8.0	2.5 2.5	7.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	'F168	Waveform 3	3.5 4.0	8.5 12.5	11.0 16.0	3.5 4.0	12.5 17.5	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	'F169	Waveform 3	3.5 4.0	8.5 8.0	15.0 10.5	3.5 4.0	15.5 12.0	ns

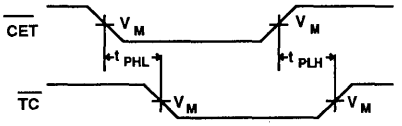
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP		Waveform 4	4.0 4.0			4.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP		Waveform 4	3.0 3.0			3.5 3.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP		Waveform 5	5.0 5.0			5.5 5.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP		Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP		Waveform 4	8.0 8.0			9.0 9.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP		Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/$\overline{D}$ to CP	'F168	Waveform 6	11.0 16.5			12.5 18.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/$\overline{D}$ to CP	'F169	Waveform 6	11.0 7.0			12.5 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low U/$\overline{D}$ to CP		Waveform 6	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP_U or CP_D Pulse width, High or Low		Waveform 1	5.0 5.0			5.5 5.5		ns

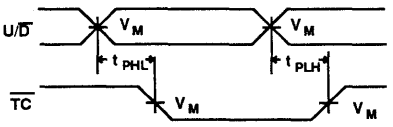
AC WAVEFORMS



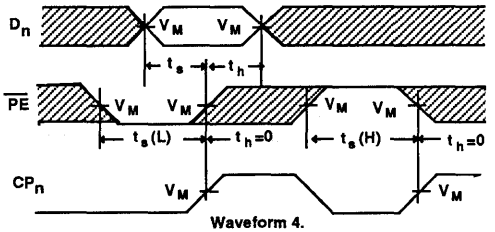
Waveform 1.
Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



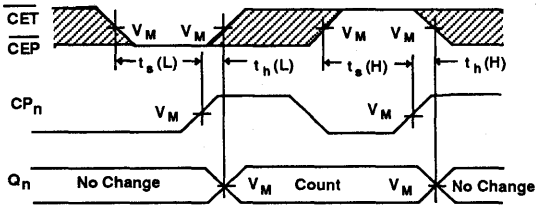
Waveform 2.
Propagation Delay, $\overline{CET}$ input to Terminal Count Output



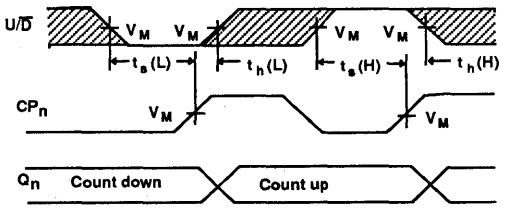
Waveform 3.
Propagation Delay, U/$\overline{D}$ input to Terminal Count Output



Waveform 4.
Data Parallel Data And Parallel Enable Setup And Hold Times



Waveform 5.
Count Enable Data Setup And Hold Times

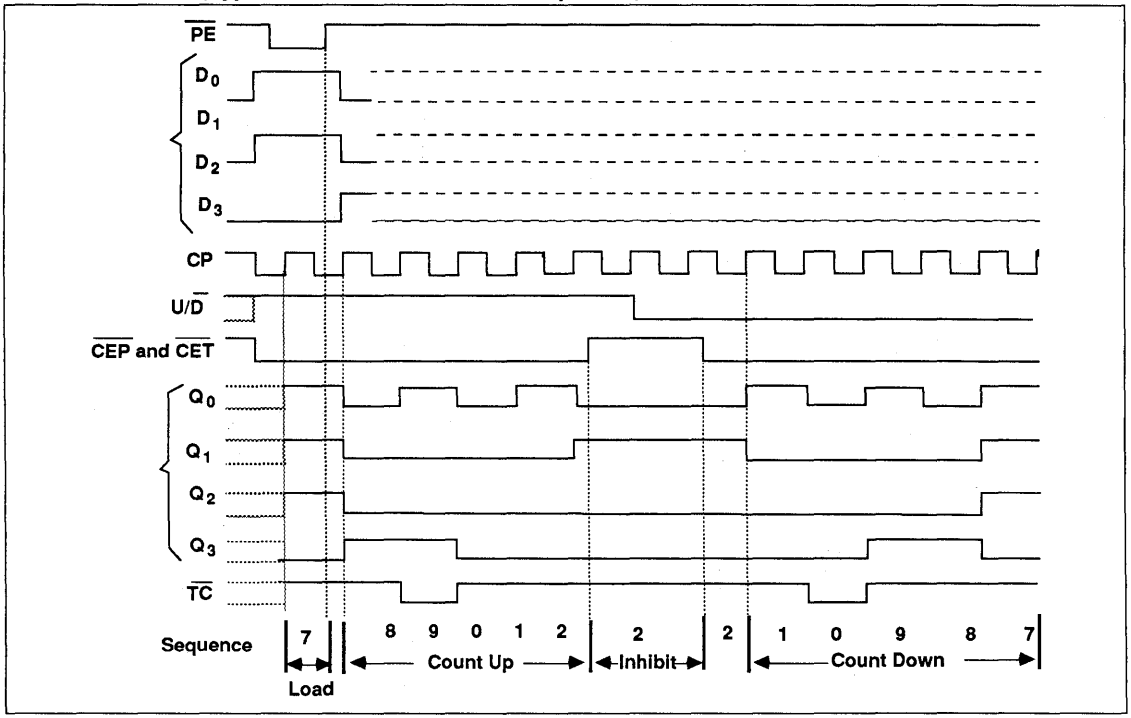


Waveform 6.
Up/Down Control Setup And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

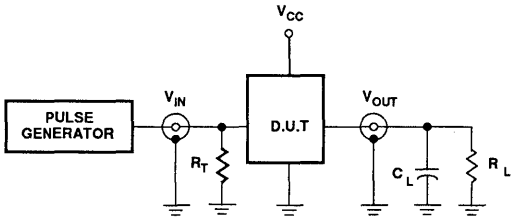
TIMING DIAGRAM (Typical clear, load, and count sequence) for 'F168



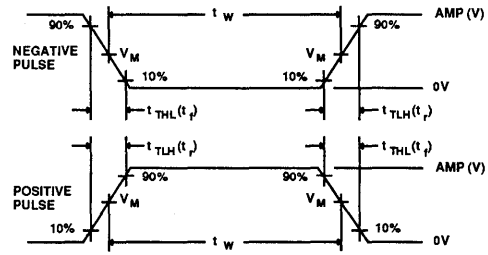
NOTES: Illustrated above is the sequence for the 'F168. The operation of the 'F169 is similar.

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum),zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine eightm and seven

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F173
Quad D-Type Flip-Flop (3-State)

FAST Products

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F173	125MHz	23mA

FEATURES

- **Edge-triggered D-type register**
- **Gated Clock Enable for hold "do nothing" mode**
- **3-state ouput buffers**
- **Gated Output Enable control**
- **Speed upgrade of N8T10 and current sink upgrade**
- **Controlled output edges to minimize ground bounces**
- **48mA sinking capability**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F173N
16-Pin Plastic SO	N74F173D

DESCRIPTION

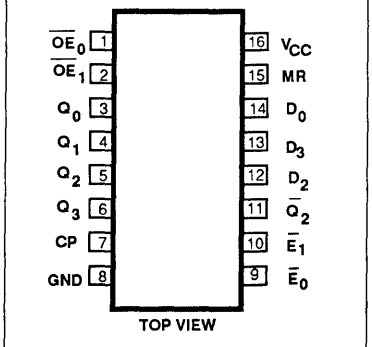
The 74F173 is a high speed 4-bit parallel load register with clock enable control, 3-state buffered outputs, and Master Reset (MR). When the two clock Enable ($\overline{E}_0$ and $\overline{E}_1$) inputs are Low, the data on the D inputs is loaded into the register simultaneously with Low-to-High CLock (CP) transition. When one or both Enable inputs are High one setup time before the Low-to-High clock transition, the register retains the previous data. Data inputs and Clock Enable inputs are fully edge-triggered and must be stable only one setup time before the Low-to-High clock transition.The Master Reset(MR) is an active-High asynchronous input. When the MR is High, all four flip-flops are reset (cleared) independently of any other input condition.The 3-state output buffers are controlled by a 2-input NOR gate. When both Output Enable ($\overline{OE}_0$ and $\overline{OE}_1$) inputs are Low, the data in the register is presented at the Q output. When one or both $\overline{OE}$ inputs are High, the outputs are forced to a high impedance "off" state. The 3-state output buffers are completely independent of the register operation; the $\overline{OE}$ transition does not affect the clock and reset operations.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input	1.0/1.0	20µA/0.6mA
$\overline{E}_0$, $\overline{E}_1$	Clock Enable inputs	1.0/1.0	20µA/0.6mA
MR	Master Reset input	1.0/1.0	20µA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable inputs	1.0/1.0	20µA/0.6mA
Q_0 - Q_4	Data outputs	750/80	15mA/48mA

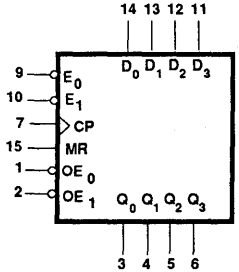
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



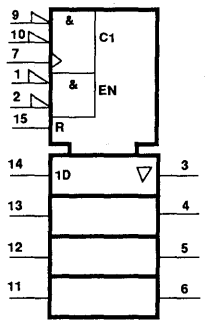
TOP VIEW

LOGIC SYMBOL



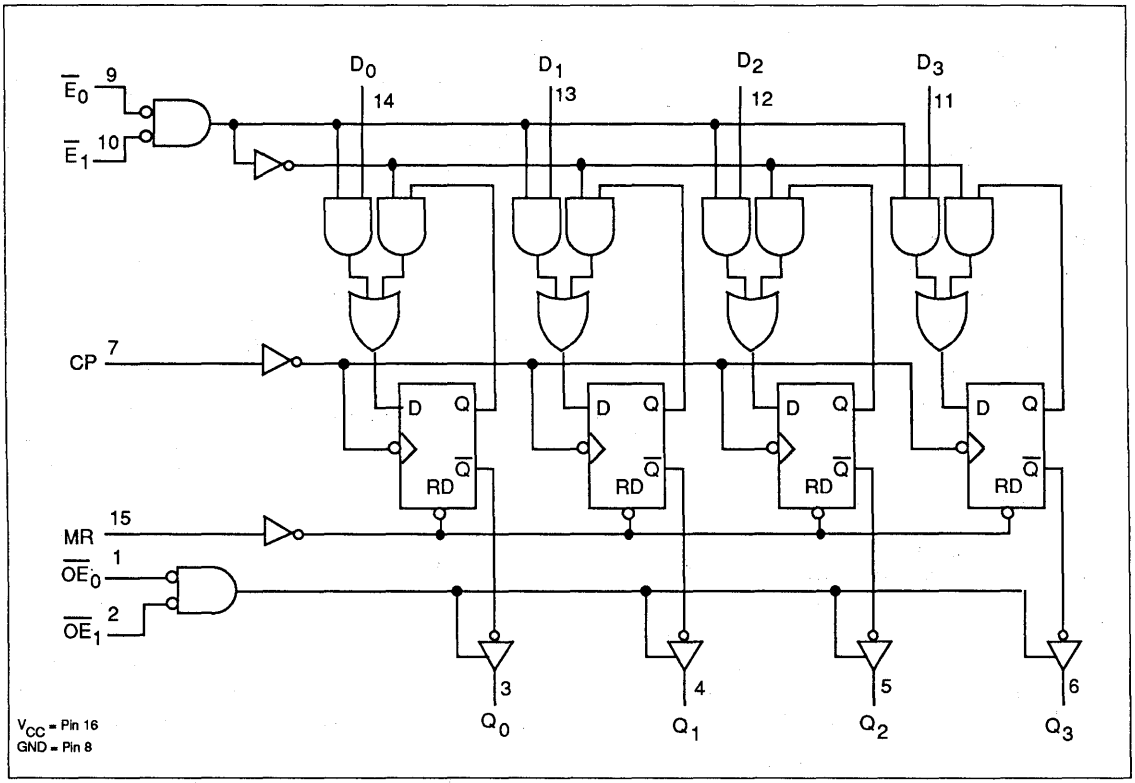
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



853-1160-94990

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUT	OPERATING MODE
MR	CP	$\overline{E}_0$	$\overline{E}_1$	D_n	Q_n(Register)	
H	X	X	X	X	L	Reset (clear)
L	↑	l	l	l	L	Parallel load
L	↑	l	l	h	H	
L	X	h	X	X	q_n	Hold (do nothing)
L	X	X	h	X	q_n	

H = High voltage level
h = High voltage level one setup prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup prior to Low-to-High clock transition
q_n = Lower case letters indicate the state of the referenced input (or output) on setup time priorn to the Low-to-High clock transition
X = Don't care
↑ =Low-to-High clock transition

FUNCTION TABLE

INPUTS			OUTPUT	OPERATING MODE
Q_n(Register)	$\overline{OE}_0$	$\overline{OE}_1$	Q_n	
L	L	L	L	Read
H	L	L	H	
X	H	X	Z	Disabled
X	X	H	Z	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	96	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = -15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0	3.1		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX		±10%V_{CC}		0.38	0.55	V
					±5%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				19	26	mA
		I_{CCL}					27	37	mA
		I_{CCZ}					23	32	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed lasty.

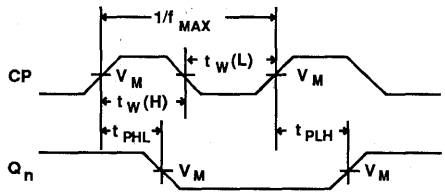
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	4.5 6.0	6.5 8.0	9.0 10.5	4.0 5.5	10.0 11.5	ns
t_{PHL}	Propagation delay MR to Q_n	Waveform 2	6.5	8.5	11.5	6.0	12.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 4 Waveform 5	3.5 5.5	5.0 7.0	8.0 10.0	2.5 4.5	8.5 11.0	ns
t_{PZH} t_{PZL}	Output Disable time to High or Low level	Waveform 4 Waveform 5	1.5 3.0	3.5 5.0	7.0 8.5	1.0 2.5	8.0 9.0	ns
t_{THL} t_{TLH}	Transition time 10% to 90%, 90% to 10%	Waveform 5 Waveform 4	2.0 4.0	5.0 7.5	8.0 10.0	2.0 4.0	8.5 11.0	ns

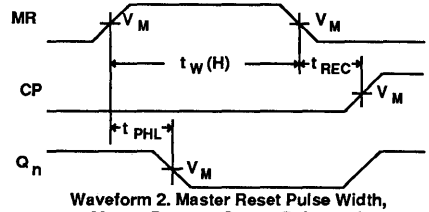
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 3	2.5 2.5			3.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{E}_n$ to CP	Waveform 3	4.5 7.5			5.0 8.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{E}_n$ to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	3.0 6.0			3.0 6.0		ns
$t_w(H)$	MR Pulse width, High	Waveform 2	3.5			3.5		ns
t_{REC}	Recovery time, MR to CP	Waveform 2	4.5			5.5		ns

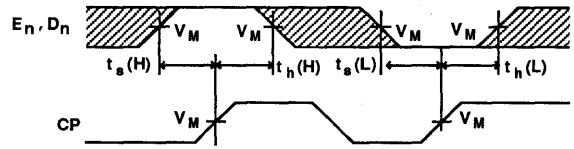
AC WAVEFORMS



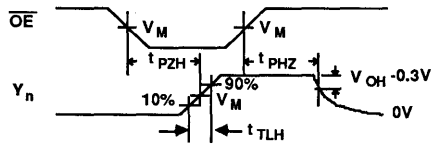
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



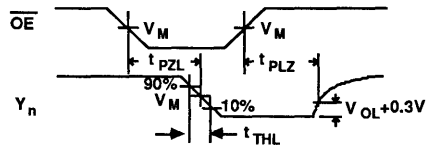
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 3. Data And Enable Setup And Hold Times



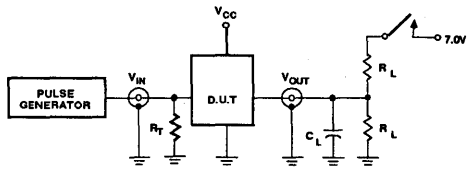
Waveform 4. 3-State Output Enable Time To High Level, Output Disable Time From High Level And Transition Time To High Level



Waveform 5. 3-State Output Enable Time To Low Level , Output Disable Time From Low Level And Transition Time To Low level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

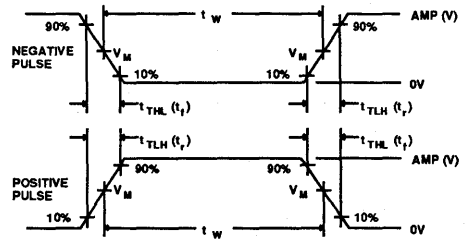
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

74F174
Flip-Flop

FAST Products

Hex D Flip-Flops

Product Specification

FEATURES

- **Six edge-triggered D-type flip-flops**
- **Buffered common Clock**
- **Buffered, asynchronous Master Reset**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F174	100 MHz	35 mA

DESCRIPTION

The 74F174 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced Low independent of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where true outputs only are required, and the Clock and Master Reset are common to all storage elements.

ORDERING INFORMATION

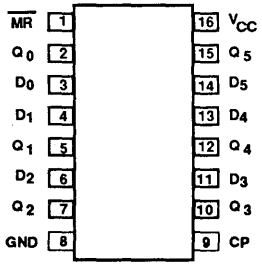
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F174N
16-Pin Plastic SO	N74F174D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

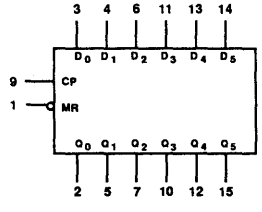
PINS	DESCRIPTION	74ALS(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_5	Data inputs	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active-Low)	1.0/1.0	20µA/0.6mA
Q_0-Q_5	Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

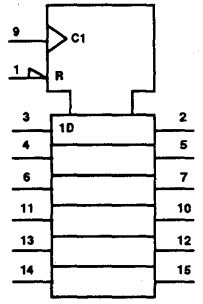


LOGIC SYMBOL

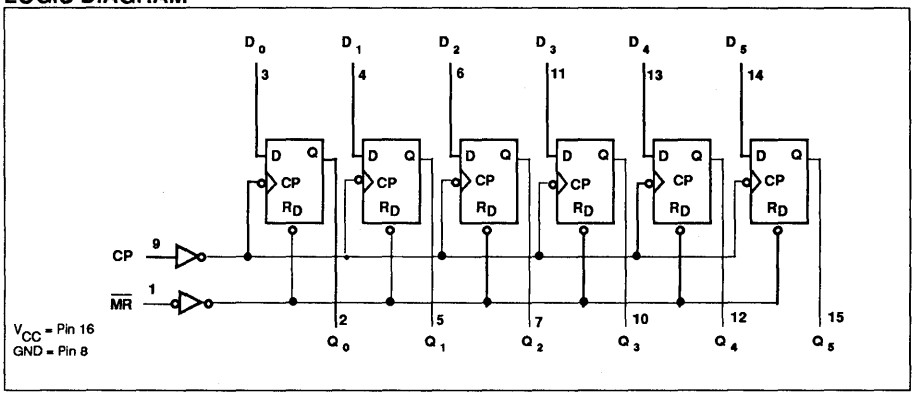


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{MR}$	CP	D	Q_n	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"

H = High voltage level
L = Low voltage level
X = Don't care
↑= Low-to-High Clock transition
h =High voltage level one set-up time prior to the Low-to-High Clock transition.
l = Low voltage level one set-up time prior to the Low-to-High Clock transition.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, D_n=$\overline{MR}$=4.5V, CP=↑			35	45	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

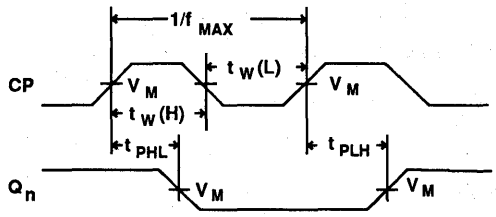
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS: T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			LIMITS: T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.5 4.5	5.5 6.0	8.0 10.0	3.5 4.5	9.0 11.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	5.0	8.5	14.0	5.0	15.0	ns

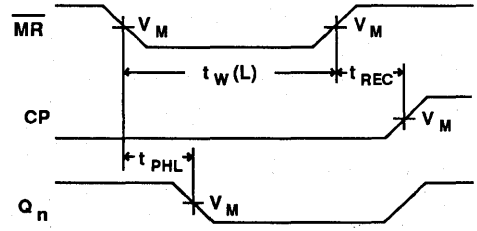
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS: T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			LIMITS: T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 3	4.0 4.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	5.0			5.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 2	5.0			5.0		ns

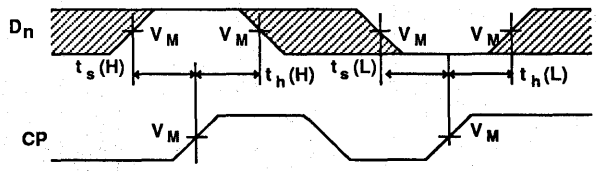
AC WAVEFORM



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



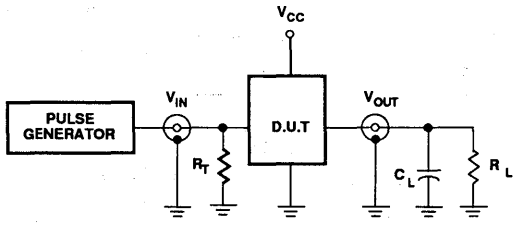
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



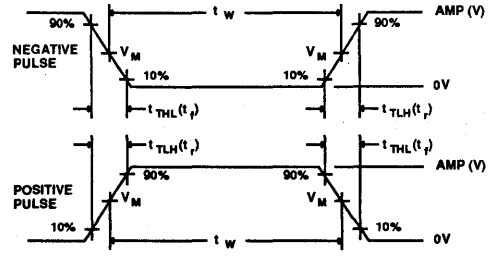
Waveform 3. Data Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F175
Flip-Flop

Quad D Flip-Flop

FAST Products

Product Specification

FEATURES

- **Four edge-triggered D-type flip-flops**
- **Buffered common clock**
- **Buffered asynchronous Master Reset**
- **True and complementary outputs**

TYPE	TYPICAL fMAX	TYPICAL SUPPLY CURRENT (TOTAL)
74F175	140MHz	25mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F175N
16-Pin Plastic SO	N74F175D

DESCRIPTION

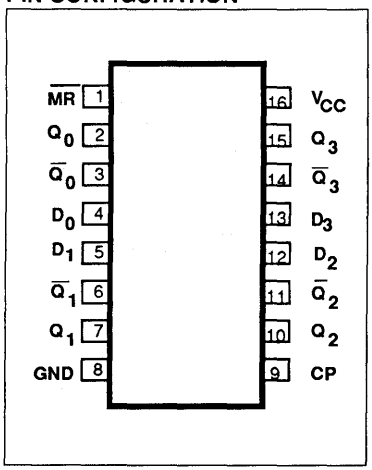
The 74F175 is a quad, edge-triggered D-type flip-flop with individual D inputs and both Q and $\overline{Q}$ outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously. The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output. All Q outputs will be forced Low independently of clock or data inputs by Low voltage level on the $\overline{MR}$ input. The device is useful for applications where both true and complementary outputs are required and the CP and $\overline{MR}$ are common to all storage elements.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

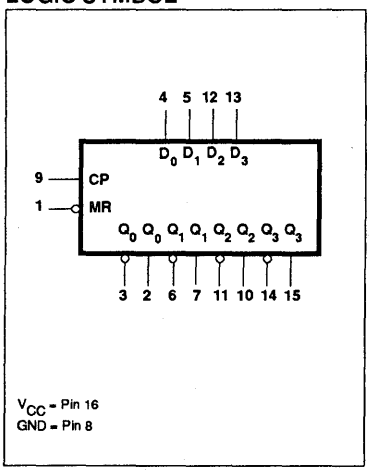
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
Q_0 - Q_3	True outputs	50/33	1.0mA/20mA
$\overline{Q}_0$ - $\overline{Q}_3$	Complementary outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

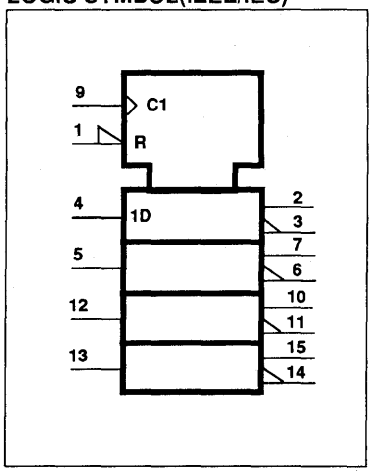
PIN CONFIGURATION



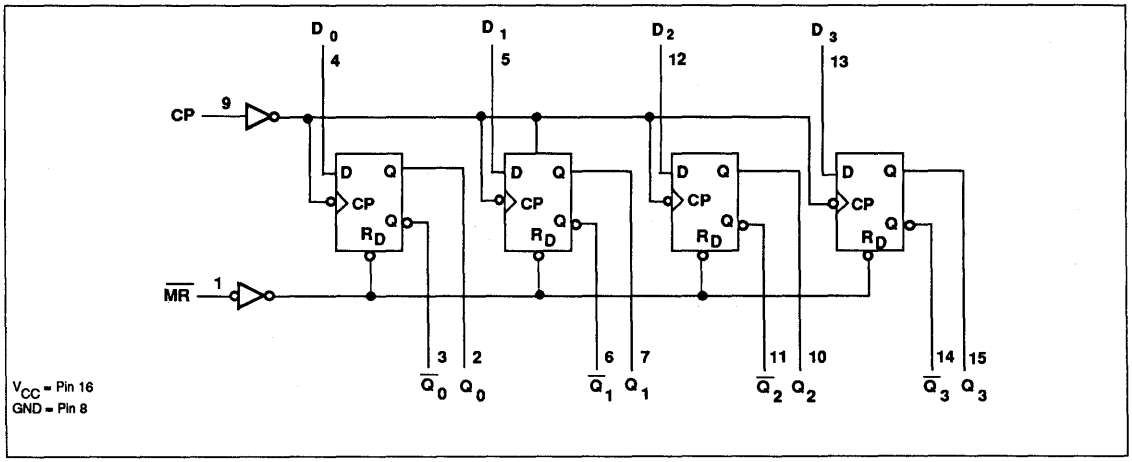
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS		OPERATING MODE
$\overline{MR}$	CP	D	Q_n	$\overline{Q}_n$	
L	X	X	L	H	Reset (clear)
H	↑	h	H	L	Load "1"
H	↑	l	L	H	Load "0"

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, D_n=$\overline{MR}$=4.5V, CP=↑			25	34	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

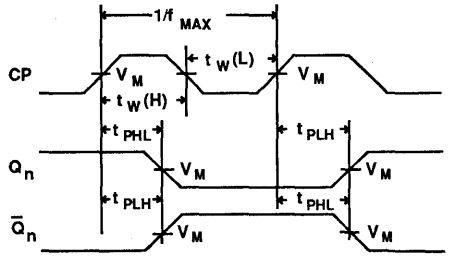
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	140		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveform 1	4.0 4.0	5.0 6.5	6.5 8.5	4.0 4.0	7.5 9.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 3	4.5	9.0	11.5	4.5	13.0	ns
t_{PLH}	Propagation delay $\overline{MR}$ to $\overline{Q}_n$	Waveform 3	4.0	6.5	8.0	4.0	9.0	ns

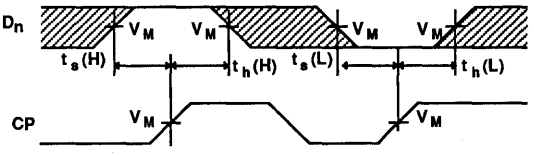
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 3	5.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 3	5.0			5.0		ns

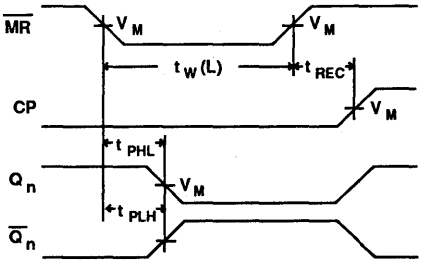
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



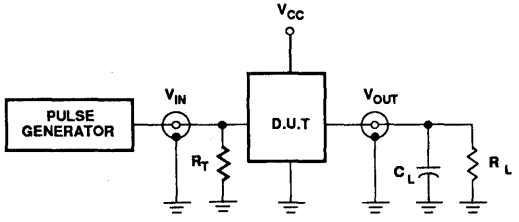
Waveform 2. Data Setup And Hold Times



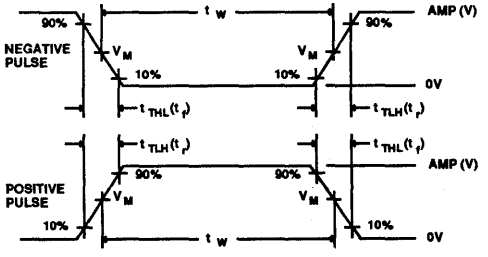
Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F181
Arithmetic Logic Unit

FAST Products

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F181	7.0 ns	43mA

FEATURES

- **Provides 16 arithmetic operations: add, subtract, compare, and double; plus 12 other arithmetic operations**
- **Provides all 16 logic operations of two variables:Exclusive-OR, Compare, AND, NAND, NOR, OR plus 10 other logic operations**
- **Full look-ahead carry for high speed arithmetic operation on long words**
- **40% faster than 'S181 with only 30% 'S181 power consumption**
- **Available in 300 mil-wide Slim 24 pin Dip package**

DESCRIPTION

The 74F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S_0-S_3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active-High or active-Low operands. The Function Table lists these operations.

ORDERING INFORMATION

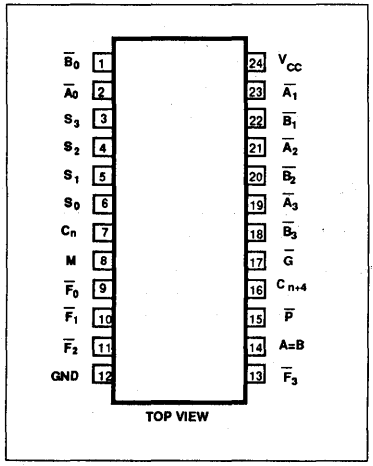
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300 mil)	N74F181N
24-Pin Plastic SOL	N74F181D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

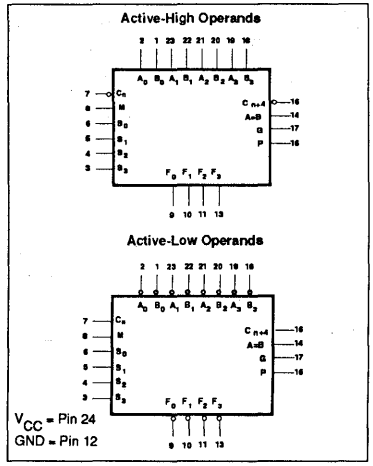
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{A}_0$-$\overline{A}_3$	A operand inputs	1.0/3.0	20µA/1.8mA
$\overline{B}_0$-$\overline{B}_3$	B operand inputs	1.0/3.0	20µA/1.8mA
M	Mode control input	1.0/1.0	20µA/0.6mA
S_0-S_3	Function select input	1.0/4.0	20µA/2.4mA
C_n	Carry input	1.0/5.0	20µA/3.0mA
C_{n+4}	Carry output	50/33	1.0mA/20mA
$\overline{P}$	Carry Propagate output	50/33	1.0mA/20mA
$\overline{G}$	Carry Generate output	50/33	1.0mA/20mA
A=B	Compare output	OC/33	OC/20mA
$\overline{F}_0$-$\overline{F}_3$	Outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state. OC=Open Collector

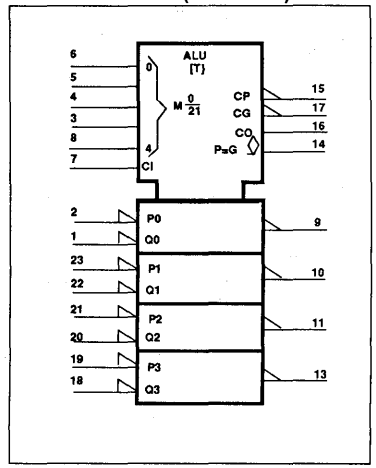
PIN CONFIGURATION



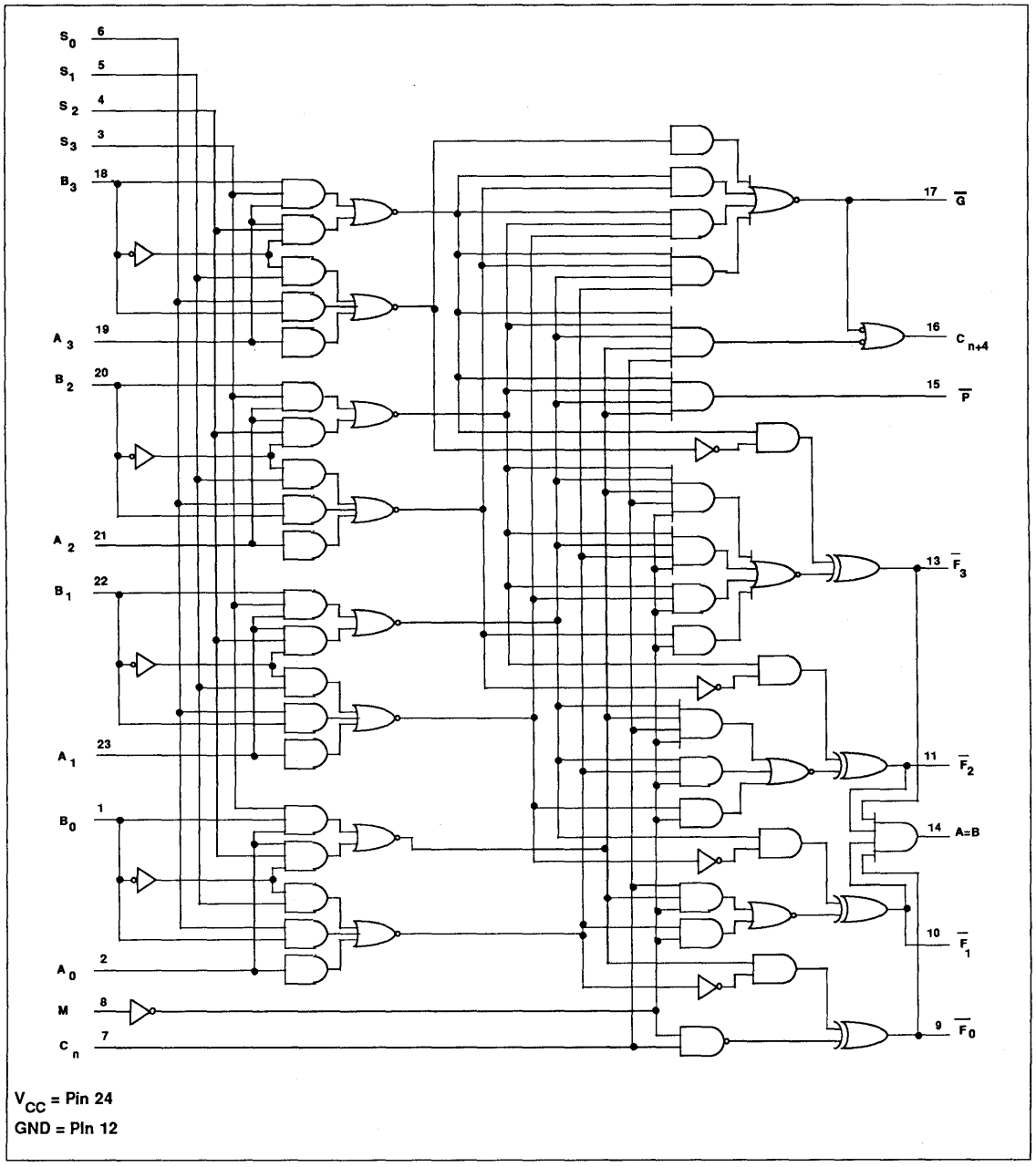
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12

When the Mode Control input (M) is High, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is Low, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry look-ahead and provides for either ripple carry between device using the C_{n+4} output, or for carry look-ahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input(C_n) of the next unit. For high-speed operation the device is used in conjunction with the 'F182 carry look-ahead circuit. One carry look-ahead package is required for each group of four 'F181 devices. Carry look-ahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A=B output from the device goes High when all four F outputs are High and can be used to indicate logic equivalence over 4-bits when the unit is in the subtract mode. The A=B output is open-collector and can be wired-AND with other A=B outputs to give a comparison for more than 4 bits. The A=B signal can also be used with the C_{n+4} signal to indicate A>B and A<B. The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus select code LHHL generates A minus B minus 1 (two's complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (one's complement), a carry out means borrow; thus, a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active-Low inputs producing active-Low outputs or with active-High inputs producing active High outputs. For either case, the table lists the operations that are performed to the operands labled inside the logic symbol.

MODE-SELECT FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE HIGH INPUTS & OUTPUTS		ACTIVE LOW INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	Logic (M=H)	Arithmetic** (M=L) (C_n=H)	Logic (M=H)	Arithmetic** (M=L) (C_n=L)
L	L	L	L	$\overline{A}$	A	$\overline{A}$	A minus 1
L	L	L	H	$\overline{A+B}$	A+B	$\overline{AB}$	AB minus 1
L	L	H	L	$\overline{A}B$	A+$\overline{B}$	$\overline{A}$+B	A$\overline{B}$ minus 1
L	L	H	H	Logical 0	minus 1	Logical 1	minus 1
L	H	L	L	$\overline{AB}$	A plus A$\overline{B}$	$\overline{A+B}$	A plus (A+$\overline{B}$)
L	H	L	H	$\overline{B}$	(A+B) plus A$\overline{B}$	$\overline{B}$	AB plus (A+$\overline{B}$)
L	H	H	L	A$\oplus$B	A minus B minus 1	$\overline{A \oplus B}$	A minus B minus 1
L	H	H	H	A$\overline{B}$	AB minus 1	A+$\overline{B}$	A + $\overline{B}$
H	L	L	L	$\overline{A}$+B	A plus AB	$\overline{A}$B	A plus (A+B)
H	L	L	H	$\overline{A \oplus B}$	A plus B	A$\oplus$B	A plus B
H	L	H	L	B	(A+$\overline{B}$) plus AB	B	A$\overline{B}$ plus (A+B)
H	L	H	H	AB	AB minus 1	A+ B	A+B
H	H	L	L	Logical 1	A plus A*	Logical 0	A plus A*
H	H	L	H	A+$\overline{B}$	(A+B) plus A	A$\overline{B}$	AB plus A
H	H	H	L	A+B	(A+$\overline{B}$) plus A	AB	A$\overline{B}$ plus A
H	H	H	H	A	A minus 1	A	A

H = High voltage level
L = Low voltage level
* = Each bit is shifted to the next more significant position.
** = Arithmetic operations expressed in two's complement notation.

SUM MODE TEST TABLE I

FUNCTION INPUTS: $S_0=S_3=4.5V$, $S_1=S_2=M=0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH}, t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH}, t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH}, t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

DIFF MODE TEST TABLE II

FUNCTION INPUTS: $S_1=S_2=4.5V$, $S_0=S_3=M=0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	$\overline{G}$
t_{PLH}, t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	$\overline{G}$
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A=B
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A=B
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}
t_{PLH}, t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}
t_{PLH}, t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	Any $\overline{F}$ or C_{n+4}

LOGIC MODE TEST TABLE III

FUNCTION INPUTS: $S_1=S_2=M=4.5V$, $S_0=S_3=0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	$\overline{F}_i$

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_K	Input clamp current				-18	mA
V_{OH}	High level output voltage	A=B only			4.5	V
I_{OH}	High-level output current	Any output except A=B			-1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current	A=B only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OH}	High-level output voltage	Any output except A=B	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	M	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		$\overline{A_0}$-$\overline{A_3}$, $\overline{B_0}$-$\overline{B_3}$						-1.8	mA
		S_0-S_3						-2.4	mA
		C_n						-3.0	mA
I_{OS}	Short-circuit output current[3]	Any output except A=B	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	S_0-S_3=M=$\overline{A}_0$-$\overline{A}_3$=4.5V, $\overline{B}_0$-$\overline{B}_3$=C_n=GND			43	65	mA
		I_{CCL}		S_0-S_3=M=4.5V, $\overline{B}_0$-$\overline{B}_3$=C_n=$\overline{A}_0$-$\overline{A}_3$=GND			43	65	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

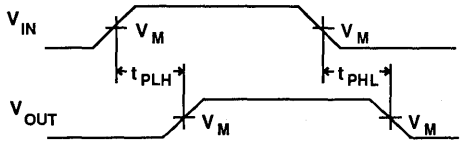
SYMBOL	PARAMETER	TEST CONDITIONS				LIMITS					UNIT
						T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
		Mode	Table	Wave form	Condition	Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	Sum Diff	I II	1	M=0V	3.0 2.5	5.0 5.0	8.0 8.0	3.0 2.5	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4}	Sum	I	2	$M=S_1=S_2=0V$, $S_0=S_3=4.5V$	5.0 5.0	9.0 8.0	12.0 12.0	5.0 5.0	13.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4}	Diff	II	2	$M=S_0=S_3=0V$, $S_1=S_2=4.5V$	5.0 5.0	9.5 8.0	13.0 12.0	5.0 5.0	14.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}_n$	Diff Sum	II I	1	M=0V	3.0 3.0	5.0 5.0	8.0 8.0	3.0 2.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	Sum	I	1	$M=S_1=S_2=0V$, $S_0=S_3=4.5V$	3.0 3.0	5.0 5.0	7.5 7.5	2.5 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	Diff	II	2	$M=S_0=S_3=0V$, $S_1=S_2=4.5V$	3.0 3.0	4.5 5.0	8.0 8.5	2.5 2.5	9.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	Sum	I	2	$M=S_1=S_2=0V$, $S_0=S_3=4.5V$	2.5 3.0	4.0 4.5	7.0 7.5	2.0 2.5	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	Diff	II	1, 2	$M=S_0=S_3=0V$, $S_1=S_2=4.5V$	2.5 3.0	4.0 5.0	7.5 8.5	2.0 2.5	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Sum	I	1, 2	$M=S_1=S_2=0V$, $S_0=S_3=4.5V$	3.0 3.0	4.5 4.5	7.5 7.5	2.5 3.0	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Diff	II	1, 2	$M=S_0=S_3=0V$, $S_1=S_2=4.5V$	3.0 3.0	4.5 5.0	8.5 8.5	2.5 3.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to F_n	Sum		1, 2		3.5 3.5	6.0 5.5	10.0 9.5	3.0 3.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to F_n	Diff		1, 2		4.0 4.5	6.5 7.0	10.5 10.5	3.5 4.5	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Logic	III	1, 2	M=4.5V	3.5 3.5	5.5 5.5	9.0 10.0	3.0 3.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to A=B	Diff	II	1, 2	$M=S_0=S_3=0V$, $S_1=S_2=4.5V$	10.0 6.0	14.0 8.5	19.0 12.5	9.5 5.5	20.5 12.5	ns

NOTE: "$\overline{A}_n$ or $\overline{B}_n$ to F_n" means any $\overline{A}$ or any $\overline{B}$ to any $\overline{F}$ and "$\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$" means $\overline{A}_1$, $\overline{B}_1$ to $\overline{F}_1$; $\overline{A}_2$, $\overline{B}_2$ to $\overline{F}_2$ (the subscripts must be the same).

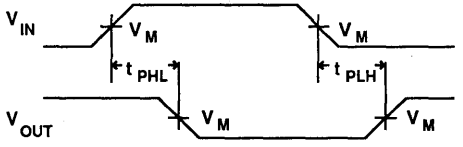
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
		Mode	Waveform	Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay S_i to $\overline{F}_i$ (Inv)		1	3.5 3.5	5.5 5.0	8.0 8.0	3.0 3.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay S_i to $\overline{F}_i$ (Non-Inv)		2	3.0 3.0	5.5 5.5	8.5 8.5	3.0 3.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S_i to A=B (Inv)		1	10.5 6.0	16.5 8.0	22.5 11.0	10.5 6.0	24.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay S_i to A=B (Non-Inv)		2	10.0 5.5	15.0 8.5	19.0 12.5	10.0 5.0	21.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay S_i to C_{n+4} (Inv)		1	3.5 3.0	7.0 5.5	11.0 10.0	3.0 2.5	12.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay S_i to $\overline{G}$ (Non-Inv)		2	2.5 2.5	5.0 4.0	7.5 7.5	2.5 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S_i to $\overline{P}$ (Non-Inv)		2	2.5 2.5	4.0 4.5	6.5 7.0	2.5 2.5	7.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_i$ (Inv)	Sum	1	3.5 3.5	6.0 6.0	8.5 8.5	3.5 3.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_i$ (Non-Inv)	Sum	2	4.5 4.0	7.0 6.0	10.0 9.5	4.5 4.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_i$ (Inv)	Diff	1	3.5 3.5	6.0 6.0	8.5 8.5	3.5 3.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_i$ (Non-Inv)	Diff	2	4.0 4.0	7.0 6.0	10.0 9.5	4.0 4.0	11.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay M to A=B (Inv)	Sum	1	12.0 6.5	16.0 8.0	20.0 11.0	11.0 6.0	22.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay M to A=B (Non-Inv)	Sum	2	13.0 6.5	17.0 8.0	21.0 10.5	12.0 6.0	24.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay M to A=B (Inv)	Diff	1	11.5 6.0	16.0 8.0	20.0 10.5	10.5 6.0	22.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay M to A=B (Non-Inv)	Diff	2	13.0 6.0	17.0 8.0	21.5 11.0	12.5 6.0	24.0 11.5	ns

AC WAVEFORMS



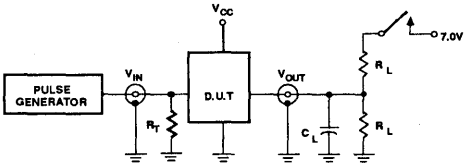
Waveform 1. Propagation Delay for Non-Inverting paths



Waveform 2. Propagation Delay for Inverting paths

NOTE: For all waveforms, $V_M = 1.5V$

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs

SWITCH POSITION

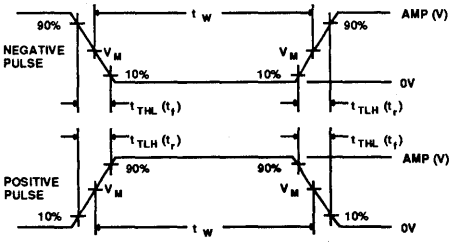
TEST	SWITCH
Open Collector	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F182
Look-Ahead Carry Generator

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F182	5.0ns	21mA

FEATURES

- **Provides carry look-ahead across a group of four ALU's**
- **Multi-level look-ahead for high speed arithmetic operation over long word lengths**

DESCRIPTION

The 74F182 is a high speed carry look-ahead generator. It accepts up to four pairs of active-Low Carry Propagate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$) and Carry Generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$) signals and an active-High Carry input (C_n) and provides anticipated active-High carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The 'F182 also has active-Low Carry Propagate ($\overline{P}$) Carry Generate ($\overline{G}$) outputs which may be used for further levels of look-ahead.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$

$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$

$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$

$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$

$$\overline{P} = P_3P_2P_1P_0$$

The 'F182 can also be used with binary ALU's in an active-Low or active-High input operand mode. The connections to and from the ALU to the carry look-ahead generator are identical in both cases.

ORDERING INFORMATION

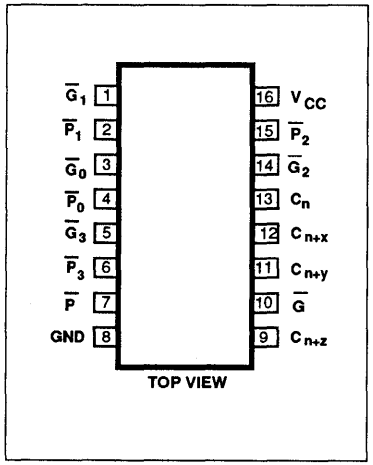
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F182N
16-Pin Plastic SO	N74F182D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

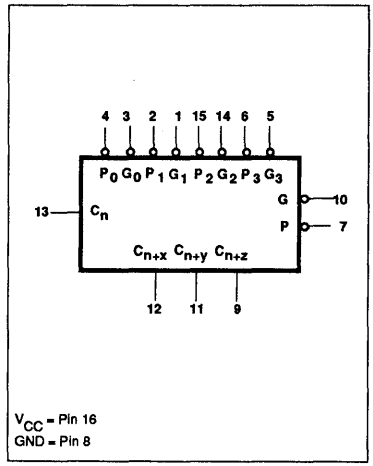
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
C_n	Carry input	1.0/2.0	20µA/1.2mA
$\overline{G}_0$, $\overline{G}_2$	Carry generate inputs (active-Low)	1.0/14.0	20µA/8.4mA
$\overline{G}_1$	Carry generate input (active-Low)	1.0/16.0	20µA/9.6mA
$\overline{G}_3$	Carry generate input (active-Low)	1.0/8.0	20µA/4.8mA
$\overline{P}_0$, $\overline{P}_1$	Carry propagate inputs (active-Low)	1.0/8.0	20µA/4.8mA
$\overline{P}_2$	Carry propagate input (active-Low)	1.0/6.0	20µA/3.6mA
$\overline{P}_3$	Carry propagate input (active-Low)	1.0/4.0	20µA/2.4mA
C_{n+x} - C_{n+z}	Carry outputs	50/33	1.0mA/20mA
$\overline{G}$	Carry generate output (active-Low)	50/33	1.0mA/20mA
$\overline{P}$	Carry propagate output (active-Low)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

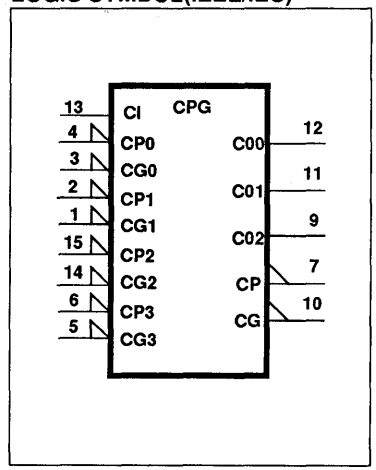
PIN CONFIGURATION



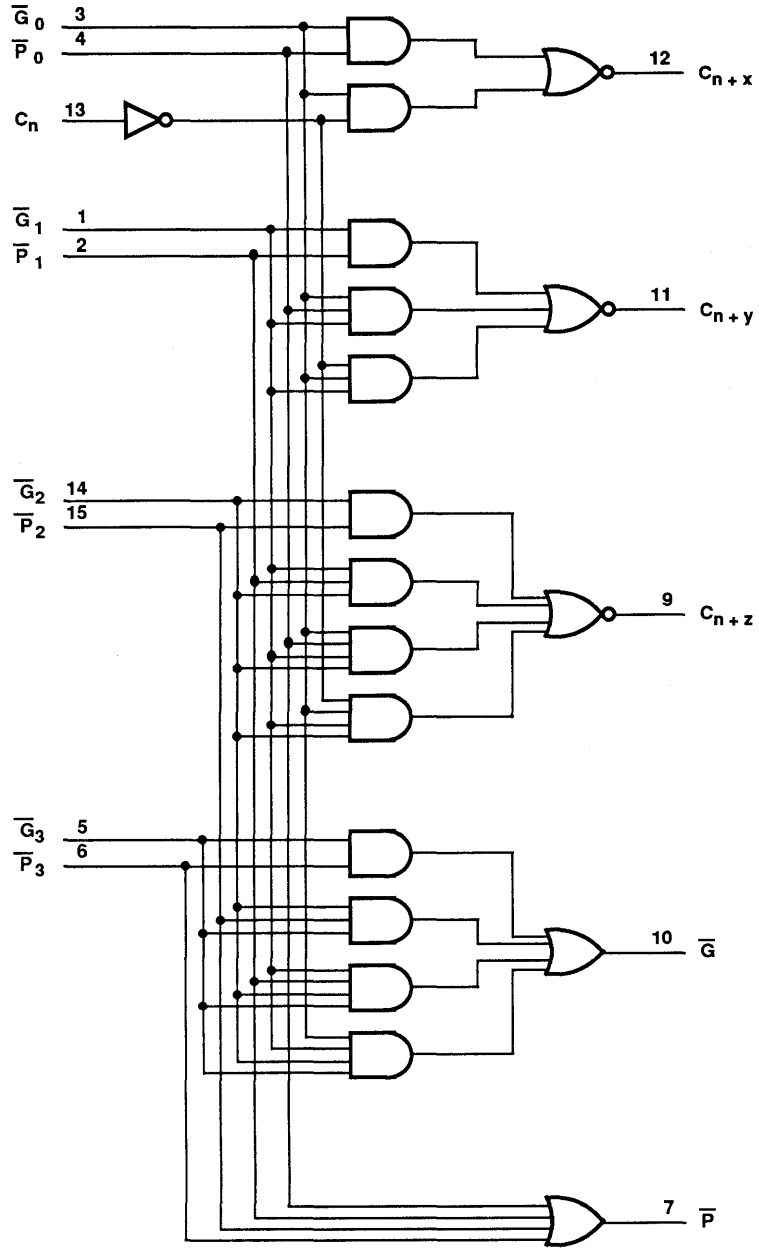
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



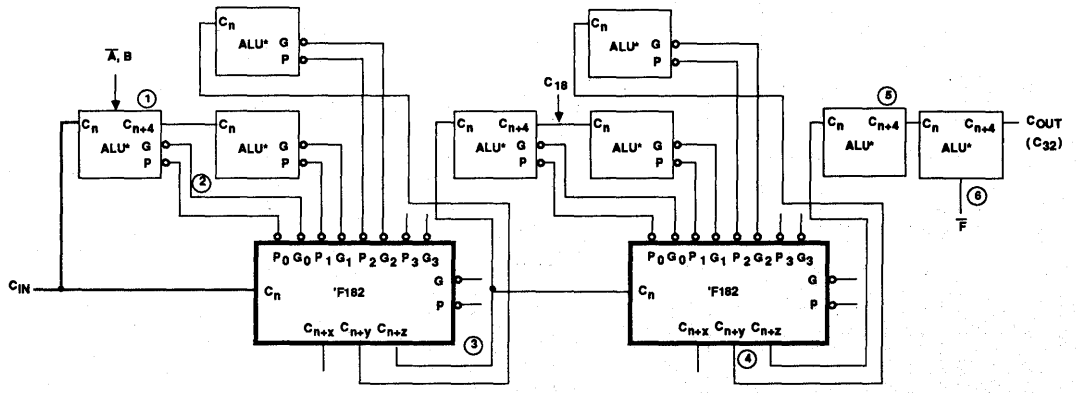
V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	P
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = High voltage level
L = Low voltage level
X = Don't care

APPLICATION



32-Bit ALU With Ripple Carry Between 16-Bit Look-Ahead ALUs
(*ALU's may be either 'F181 or 'F381)

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	C_n	V_{CC} = MAX, V_I = 0.5V					-1.2	mA
		$\overline{G}_0$, $\overline{G}_2$						-8.4	mA
		$\overline{G}_1$						-9.6	mA
		$\overline{G}_3$, $\overline{P}_0$, $\overline{P}_1$						-4.8	mA
		$\overline{P}_2$						-3.6	mA
		$\overline{P}_3$						-2.4	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				18	28	mA
		I_{CCL}					24	36	mA

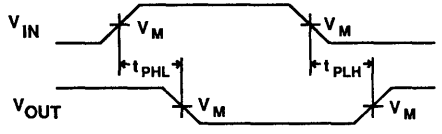
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

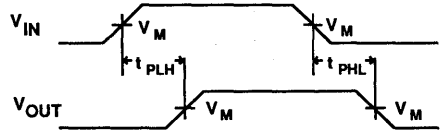
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+x}, C_{n+y}, C_{n+z}	Waveform 2	2.5 2.5	5.0 5.0	8.0 7.5	2.5 2.5	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{P}_0$, $\overline{P}_1$ or $\overline{P}_2$ to C_{n+x}, C_{n+y}, C_{n+z}	Waveform 1	2.0 1.5	5.0 3.5	7.0 5.0	1.5 1.5	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{G}_{0,1,2}$ to C_{n+x}, C_{n+y}, C_{n+z}	Waveform 1	1.5 1.5	4.0 3.0	7.5 5.0	1.5 1.5	8.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{P}_{1,2,3}$ to $\overline{G}$	Waveform 2	2.0 3.0	7.0 5.0	10.0 7.0	1.5 2.5	11.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{G}_n$ to $\overline{G}$	Waveform 2	1.5 3.0	5.0 5.0	7.0 7.0	1.5 2.5	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{P}_n$ or $\overline{P}$	Waveform 2	1.5 2.5	3.5 4.0	6.0 6.0	1.5 2.5	7.5 6.5	ns

AC WAVEFORMS



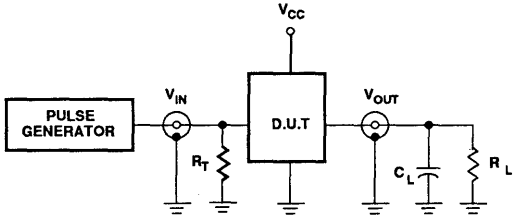
Waveform 1. Propagation Delay for Inverting Outputs



Waveform 2. Propagation Delay for Non-Inverting outputs

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



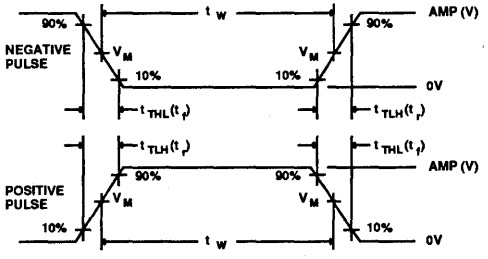
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F189A

64-Bit TTL Bipolar RAM, Inverting (3-State)

Preliminary Specification

FAST Products

TYPE	TYPICAL ACCESS TIME	TYPICAL SUPPLY CURRENT (TOTAL)
74F189A	10ns	50mA

FEATURES

- **Address access time: 10 ns**
- **Power dissipation: 4.3 mW/bit typ**
- **Schottky clamped TTL**
- **One chip enable**
- **Inverting outputs (For non-inverting outputs see 74F189A)**
- **I/O**
  - **Inputs: PNP Buffered**
  - **Outputs: 3-state**

APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Push down stacks**
- **Control store**

DESCRIPTION

The 74F189A is a high speed , 64-Bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are in High impedance state whenever the Chip Enable ($\overline{CE}$) is High. The outputs are active only in the READ mode ($\overline{WE}$ = High) and the output data is the complement of the stored data.

ORDERING INFORMATION

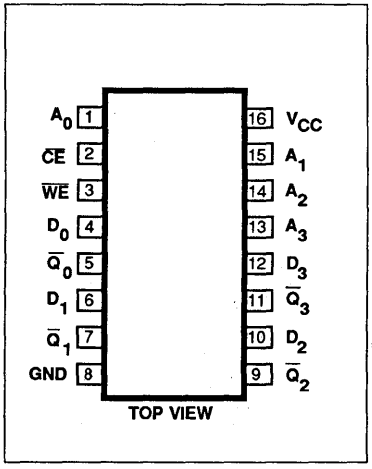
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F189AN
16-Pin Plastic SO	N74F189AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

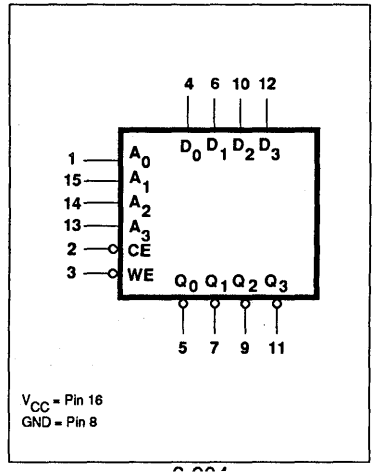
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0- D_3	Data inputs	1.0/1.0	20µA/0.6mA
A_0- A_3	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{CE}$	Chip Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{WE}$	Write Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{O}_0$- $\overline{O}_3$	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

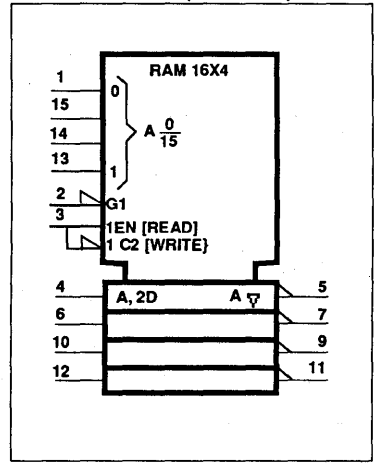
PIN CONFIGURATION



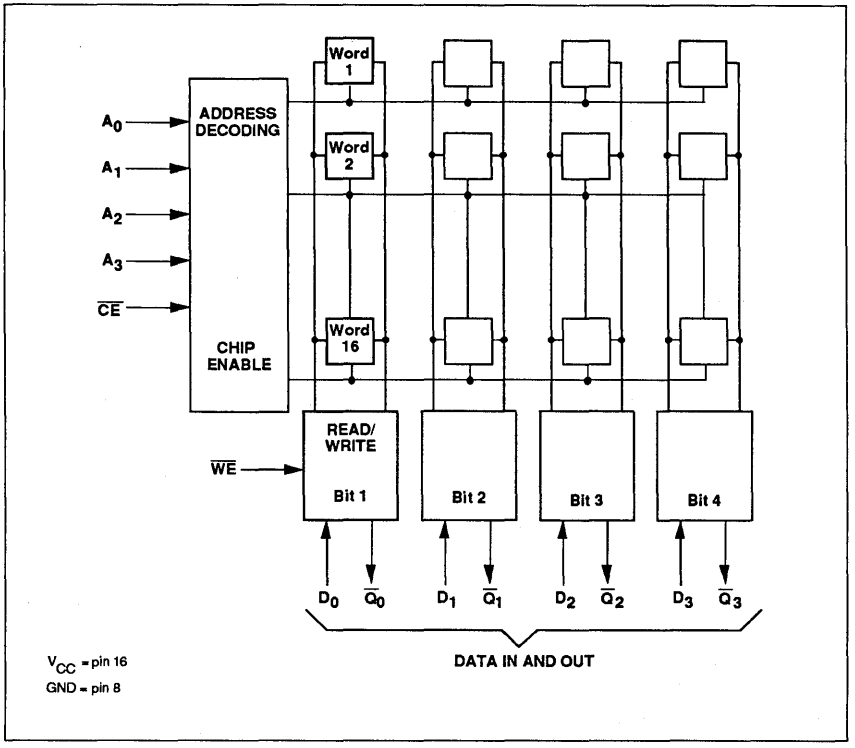
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUT	OPERATING MODE
$\overline{CE}$	$\overline{WE}$	D_n	$\overline{Q}_n$	
L	H	X	Complement of stored data	Read
L	L	L	High impedance	Write "0"
L	L	H	High impedance	Write "1"
H	X	X	High impedance	Disable Input

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current High-level voltage applied	V_{CC} = MAX, V_O = 2.7V				50	mA
I_{OZL}	Off-state output current Low-level voltage applied	V_{CC} = MAX, V_O= 0.5V				-50	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, $\overline{CE}$ = $\overline{WE}$ = GND				70	mA
C_{IN}	Input capacitance	V_{CC} = MAX, V_{IN} = 2.0V			5		pF
C_{OUT}	Output capacitance	V_{CC} = MAX, V_{OUT} = 2.0V			8		pF

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

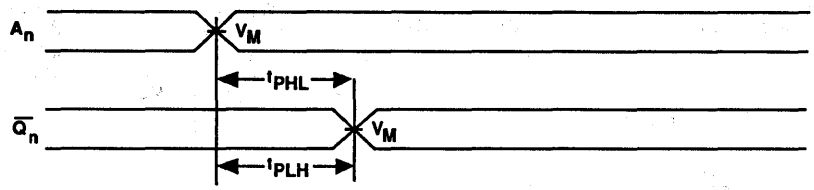
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Access time	Propagation delay A_n to $\overline{Q}_n$	Waveform 1					10.0	ns
t_{PZH} t_{PZL}		Enable time $\overline{CE}$ to $\overline{Q}_n$	Waveform 2					7.5	ns
t_{PHZ} t_{PLZ}	Disable time $\overline{CE}$ to $\overline{Q}_n$		Waveform 3					7.5	ns
t_{PZH} t_{PZL}	Response time	Enable time $\overline{WE}$ to $\overline{Q}_n$	Waveform 4					8.5	ns
t_{PHZ} t_{PLZ}	Write Recovery time	Disable time $\overline{WE}$ to $\overline{Q}_n$	Waveform 4					7.5	ns

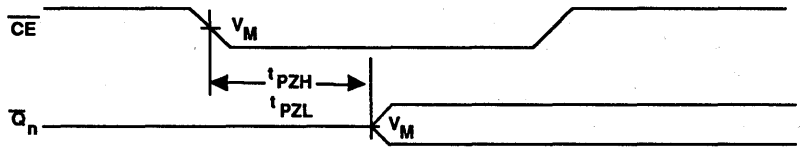
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time $\overline{WE}$ to A_n	Waveform 4				0 0		ns
$t_h(H)$ $t_h(L)$	Hold time $\overline{WE}$ to A_n	Waveform 4				0.5 0.5		ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{WE}$ to D_n	Waveform 4				5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time $\overline{WE}$ to D_n	Waveform 4				0 0		ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{WE}$ to $\overline{CE}$	Waveform 4				4.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold time $\overline{WE}$ to $\overline{CE}$	Waveform 4				4.0 4.0		ns
$t_w(L)$	Pulse width, Low $\overline{WE}$	Waveform 4				6.5		ns

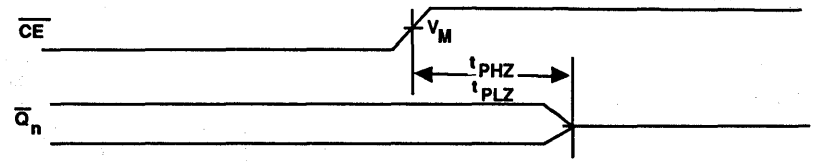
AC WAVEFORMS



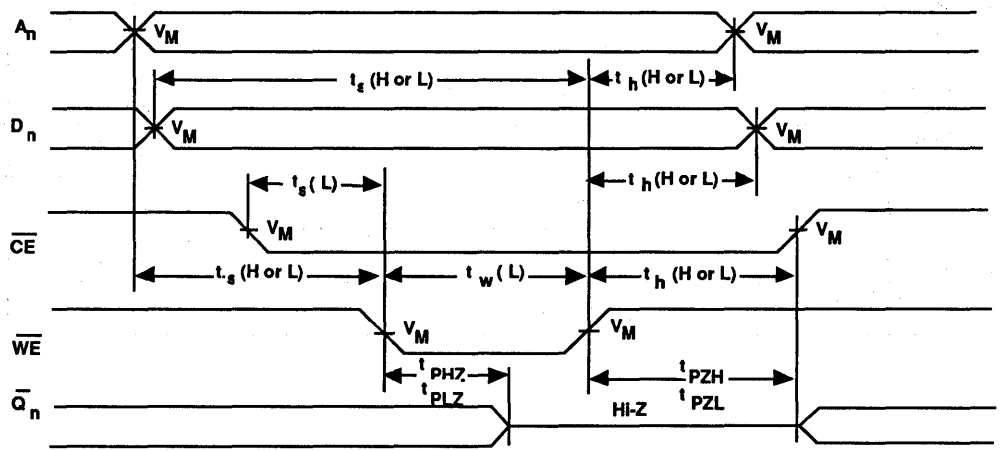
Waveform1. Read Cycle, Address Access Time



Waveform 2. Read Cycle, Chip Enable Access Time



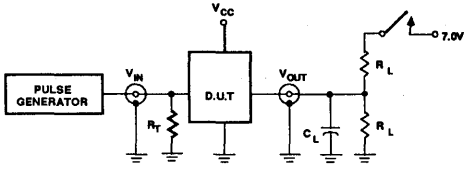
Waveform 3. Read Cycle, Chip Disable Time



Waveform 4. Write Cycle

NOTES: 1. For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

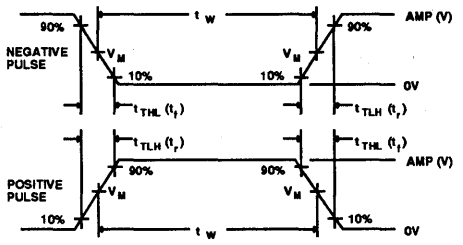
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F190, 74F191 Counters

'F190 Up/Down Decade Counter With Reset and Ripple Clock
'F191 Up/Down Binary Counter With Reset and Ripple Clock
Product Specification

FAST Products

FEATURES

- **High speed-125 MHz typical f_{MAX}**
- **Synchronous, reversible counting**
- **BCD/Decade-'F190**
  4-Bit Binary-'F191
- **Asynchronous parallel load capability**
- **Cascadable without external logic**
- **Single up/down control input**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F190	125MHz	40mA
74F191	125MHz	40mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic Dip	N74F190N, N74F191N
16-Pin Plastic SO	N74F190D, N74F191D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{CE}$	Count enable input (active Low)	1.0/3.0	20µA/1.8mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{PL}$	Asynchronous parallel load control input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{U}$/D	Up/Down count control input	1.0/1.0	20µA/0.6mA
Q_0 -Q_3	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{RC}$	Ripple clock output (active Low)	50/33	1.0mA/20mA
TC	Terminal count output	50/33	1.0mA/20mA

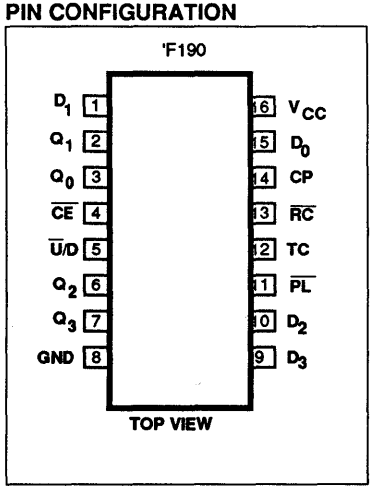
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

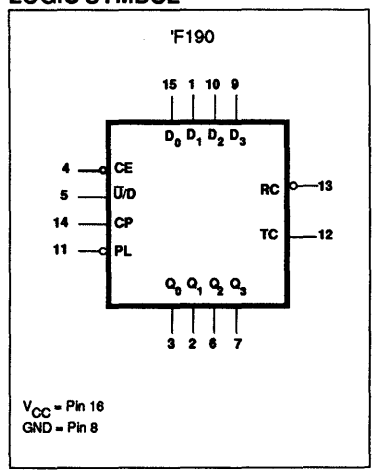
The 74F190 is a presettable Up/Down BCD Decade Counter. The 74F191 is a 4-bit Binary Counter. Both the 'F190 and the 'F191 contain four edge-triggered master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count up and count down operations. Asynchronous parallel load capability permits the counter to preset to any desired number. Information present on the parallel data inputs (D_0-D_3) is loaded into the counter and appears on the outputs when the parallel load ($\overline{PL}$) input is Low. This operation overrides the counting function. Counting is inhibited by a High level on the count enable ($\overline{CE}$) input. When $\overline{CE}$ is Low, internal state changes are initiated. Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{RC}$).

The TC output is normally Low and goes High when: 1) the count reaches zero in the count-down mode or 2) reaches "9" for the 'F190 or "15" for the 'F191 in the count up mode. The TC output will remain High until a state change occurs, either by counting or presetting, or until $\overline{U}$/D is changed. TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{RC}$ output,. When TC is High and $\overline{CE}$ is Low, fthe $\overline{RC}$ follows the clock pulse. The $\overline{RC}$ output essentially duplicates the Low clock pulse width, although delayed in time by two gate delays.

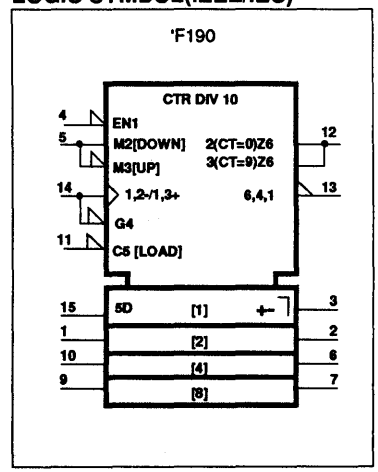
PIN CONFIGURATION



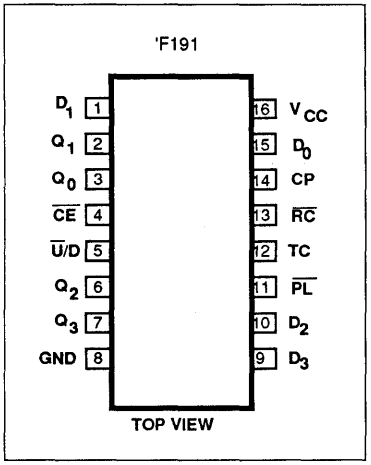
LOGIC SYMBOL



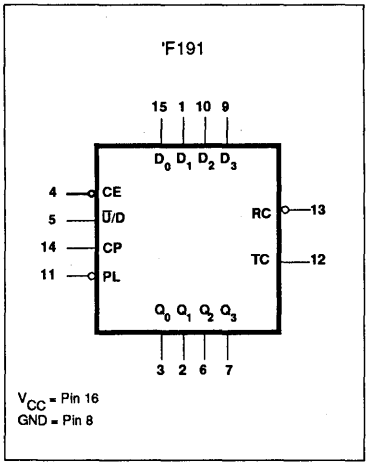
LOGIC SYMBOL(IEEE/IEC)



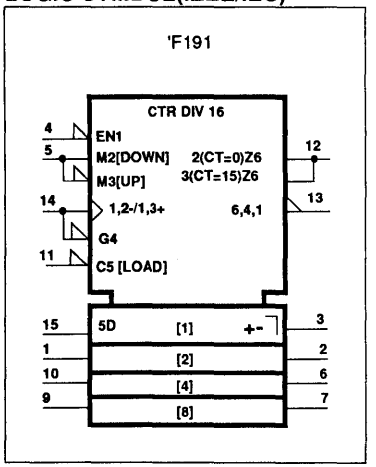
PIN CONFIGURATION



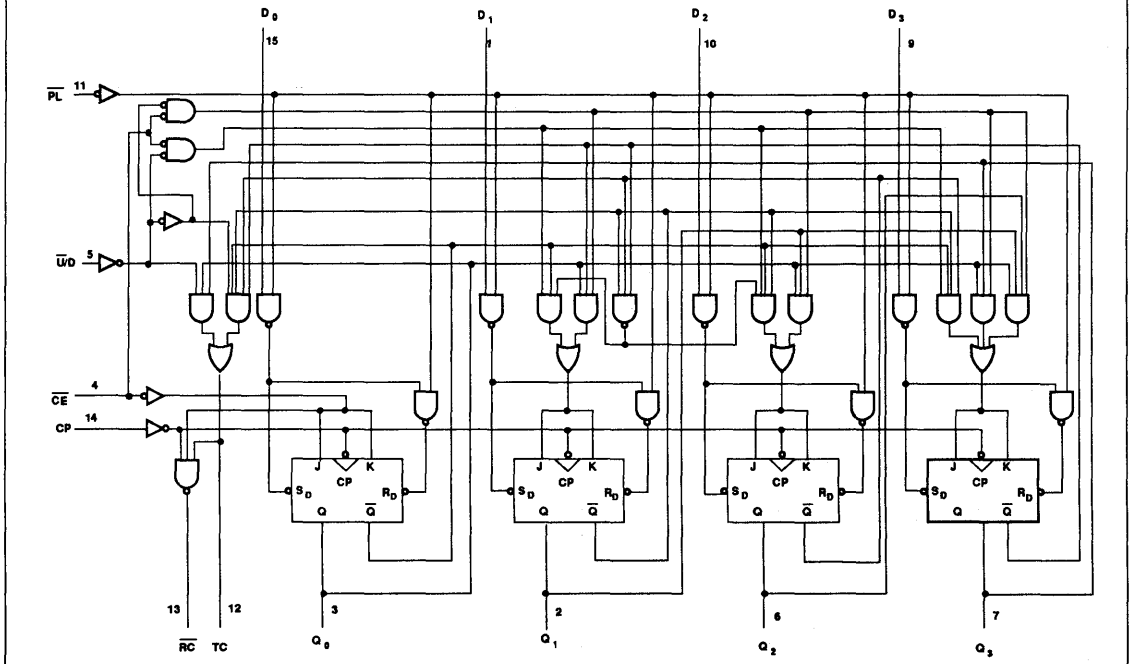
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

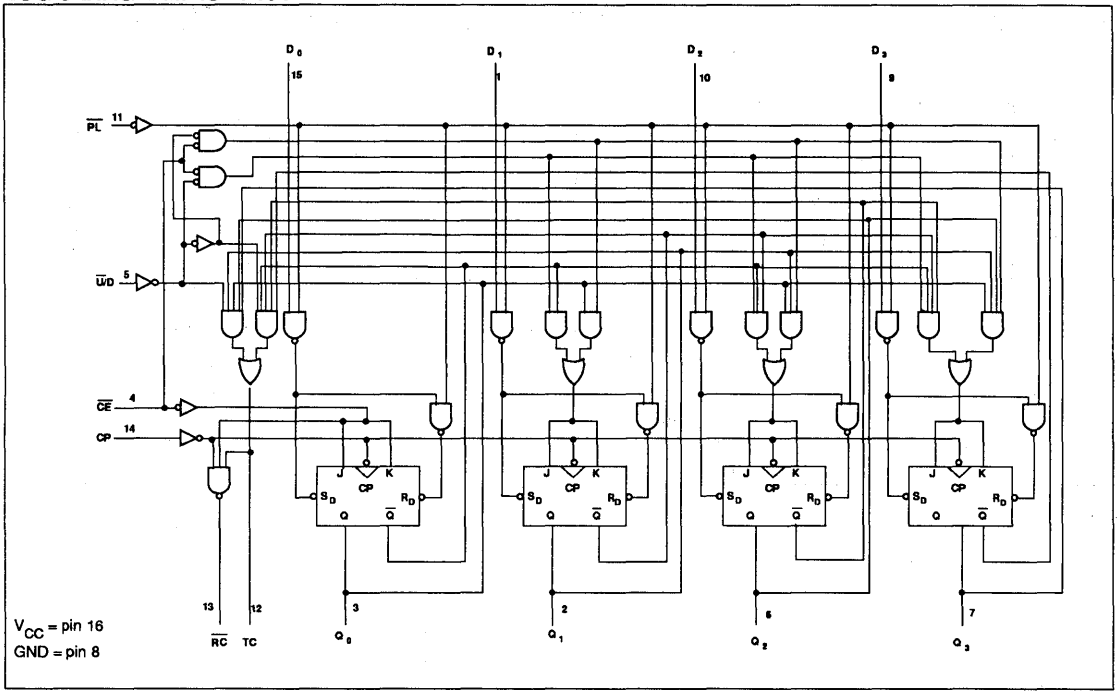


LOGIC Diagram for 'F190



V_{CC} = pin 16
GND = pin 8

LOGIC DIAGRAM for 'F191



MODE SELECTION FUNCTION TABLE

INPUTS					OUTPUT	OPERATING MODE
$\overline{PL}$	$\overline{U}$/D	$\overline{CE}$	CP	D_n	Q_n	
L	X	X	X	L	L	Parallel load
L	X	X	X	H	H	
H	L	l	↑	X	Count up	Count up
H	H	l	↑	X	Count down	Count down
H	X	H	X	X	No change	Hold (do nothing)

TC and $\overline{RC}$ FUNCTION TABLE for 'F190

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}$/D	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⊔	H	X	X	H	H	⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	H	⊔

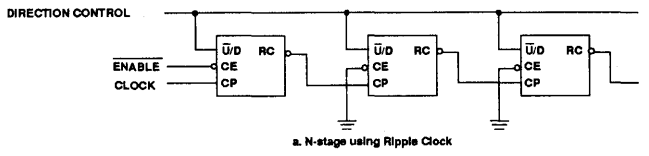
H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
⊔ = Low pulse

TC and $\overline{RC}$ FUNCTION TABLE for 'F191

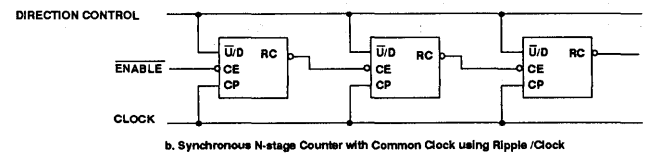
INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}$/D	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊔	H	H	H	H	H	⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	H	⊔

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
⊔ = Low pulse

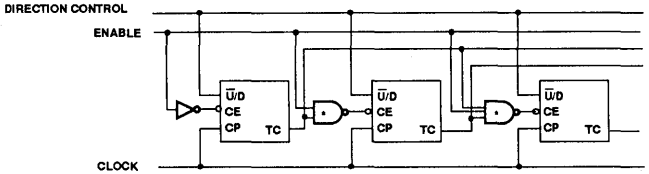
APPLICATIONS



a. N-stage using Ripple Clock



b. Synchronous N-stage Counter with Common Clock using Ripple /Clock



c. Synchronous N-stage Counter with Common Clock and Parrallel Gated Terminal Count

* = Carry Gate

Figure 1

The 'F 190/191 simplifies the design of multi-stage counters, as indicated in Figures 1a and 1b. In Figure 1a, each $\overline{RC}$ output is used as the clock input for the next higher stage. When the clock input source has limited drive capability this configuration is particulary advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a High signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first stage and the last stages is represented by the cumulative delay of the clock as it ripples-through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure 1b shows a method of causing state changes to occur simultaneously in all stages.The $\overline{RC}$ output signals propagate in ripple fashion and all clock inputs are driven in parallel. The Low state duration of the clock in this configuration must be long enough to allow the negative going edge of the $\overline{RC}$ signal to ripple through to the last stage before the clock goes High. Since the $\overline{RC}$ output of any packages goes High shortly after its clock input goes High, there is no restriction on the High state duration of the clock.

In the Figure 1c, the configuration shown avoids ripple delays and their associated restrictions. The combined TC signals from all the preceding stages forms the $\overline{CE}$ input signal for given stage. An enable signal signal must also be included in each carry gate in order to inhibit counting. Since the TC output of a given stage is not affected by its own $\overline{CE}$, and therefore, the simple scheme of Figure 1a and 1b does not apply.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	$\overline{CE}$	V_{CC} = MAX, V_I = 0.5V				-1.8	mA
		others					-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			40	55	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. Measure I_{CC} all inputs grounded and all outputs open.

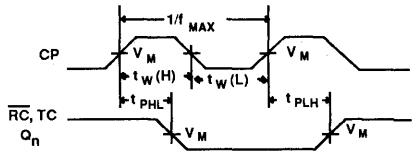
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	74F190, 74F191					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	to Q_n outputs	Waveform 1	100	125		90		MHz
		to $\overline{RC}$ output		85	95		75		
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	2.5 5.0	4.5 7.5	8.0 11.5	2.0 5.0	8.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		Waveform 1	6.5 6.0	9.0 8.0	12.5 11.0	6.0 6.0	13.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		Waveform 2	2.5 3.0	4.5 5.0	7.5 7.5	2.0 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		Waveform 2	2.0 3.0	4.0 5.0	7.0 7.5	2.0 3.0	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}/D$ to $\overline{RC}$		Waveform 2	8.0 4.5	11.0 7.5	16.0 10.5	8.0 4.0	17.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}/D$ to TC		Waveform 4	4.0 3.0	6.5 6.0	9.5 9.5	3.0 3.0	10.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		Waveform 3	2.0 6.5	4.0 9.0	7.0 12.0	1.5 6.5	7.5 13.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		Waveform 3 Waveform 4	5.5 6.5	9.5 9.5	13.0 13.0	5.0 6.0	14.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		Waveform 3 Waveform 4	6.0 6.0	14.0 11.0	18.0 13.5	6.0 6.0	19.5 15.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		Waveform 5	4.5 5.5	6.5 8.0	9.5 11.5	4.0 5.0	10.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		Waveform 5	5.5 6.0	8.5 10.5	12.0 13.5	5.5 6.0	13.0 14.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		Waveform 5	8.5 7.5	16.0 10.0	18.5 13.0	8.5 7.0	21.0 13.5	ns

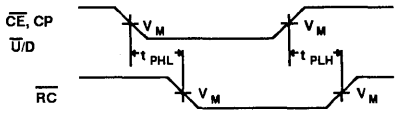
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	74F190, 74F191					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{PL}$	Waveform 6	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$	Waveform 6	2.0 2.0			2.0 2.0		ns
$t_s(L)$	Setup time, Low $\overline{CE}$ to CP	Waveform 6	10.0			10.0		ns
$t_h(L)$	Hold time, Low $\overline{CE}$ to CP	Waveform 6	0			0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{U}/D$ to CP	Waveform 6	12.0 12.0			12.0 12.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{U}/D$ to CP	Waveform 6	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	3.5 6.0			3.5 6.0		ns
$t_w(L)$	$\overline{PL}$ Pulse width, Low	Waveform 5	6.0			6.0		ns
t_{REC}	Recovery time $\overline{PL}$ to CP	Waveform 5	6.0			6.0		ns

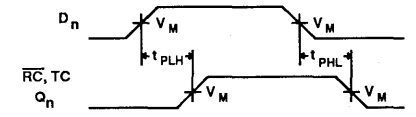
AC WAVEFORMS



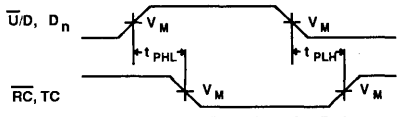
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



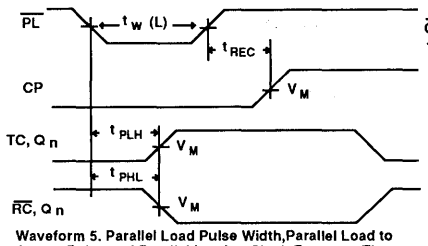
Waveform 2. Propagation Delay, Clock, Clock Enable or Up/Down to Ripple Clock Output



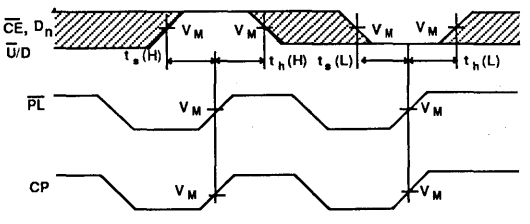
Waveform 3. Propagation Delay, Non-Inverting Path



Waveform 4. Propagation Delay, Inverting Path



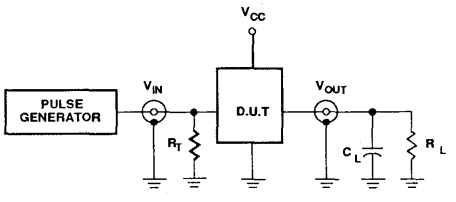
Waveform 5. Parallel Load Pulse Width,Parallel Load to Output Delay and Parallel Load to Clock Recovery Time



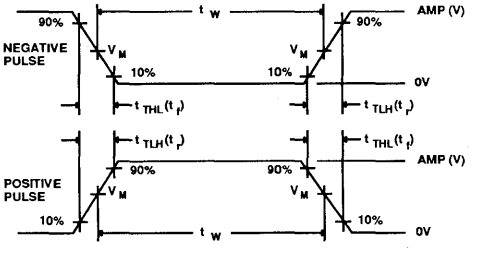
Waveform 6. Data Setup And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F192, 74F193 Counters

'F192 Up/Down Decade Counter With Separate Up/Down Clocks
'F193 Up/Down Binary Counter With Separate Up/Down Clocks
Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F192	125MHz	32mA
74F193	125MHz	32mA

FEATURES

- **Synchronous, reversible 4-bit counting**
- **Asynchronous parallel load capability**
- **Asynchronous reset (clear)**
- **Cascadable without external logic**

DESCRIPTION

The 74F192 and 74F193 are 4-bit synchronous Up/Down Counters. The 74F192 counts in BCD mode and 74F193 counts in the binary mode. Separate up/down clocks, CP_U and CP_D, respectively simplify operation. The outputs change state synchronously with the Low-to-High transition of either clock input. If the CP_U clock is pulsed while CP_D is held HIgh, the device will count up. If the CP_D clock is pulsed while CP_U is held HIgh, the device will count down The device can be cleared at any time by the asynchronous reset pin. It may also be loaded in parallel by activating the asynchronous parallel load pin. Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, asynchronous preset, load, and synchronous count up and count down functions. Each flip-flop contains JK feedback from slave to master such that a Low-to-High transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one. One clock should be held High while counting with the other, because the circuit will either count by twos or not at all depending on the state of the first JK flip-flop, which cannot toggle as long as either clock input is Low. Applications requiring reversible operation must make the reversing decision while the activating clock is High to avoid erroneous counts.The terminal count up ($\overline{TC}_U$) and terminal count down ($\overline{TC}_D$) outputs are normally High. When the circuit has reached the maximum count state (9 for the 'F192 and 15 for the 'F193), the next High-to-Low transition of CP_U will cause $\overline{TC}_U$ to go Low. $\overline{TC}_U$ will stay Low until CP_U goes High again, duplicating the count up clock, although delayed by two gate delays. Likewise, the $\overline{TC}_D$ output will go Low when the circuit is in the zero

ORDERING INFORMATION

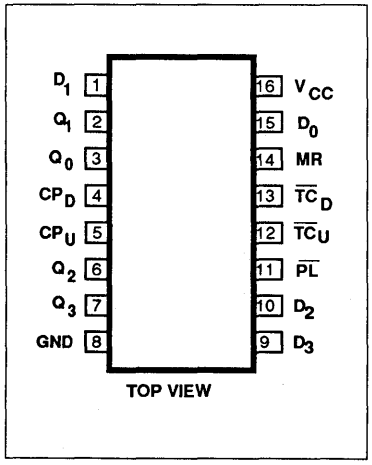
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic Dip	N74F192N, N74F193N
16-Pin Plastic SO	N74F192D, N74F193D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

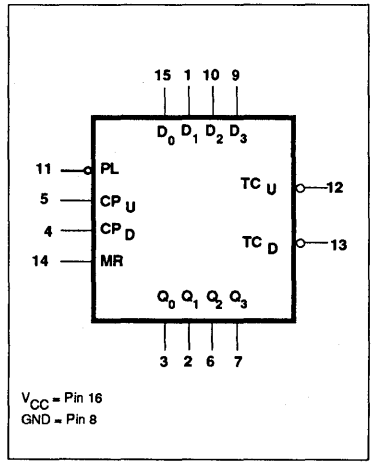
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
CP_U	Count up clock input (active rising edge)	1.0/3.0	20µA/1.8mA
CP_D	Count down clock input (active rising edge)	1.0/3.0	20µA/1.8mA
$\overline{PL}$	Asynchronous parallel load control input (active Low)	1.0/1.0	20µA/0.6mA
MR	Asynchronous Master Reset input	1.0/1.0	20µA/0.6mA
Q_0 -Q_3	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{TC}_U$	Terminal count up (carry) output (active Low)	50/33	1.0mA/20mA
$\overline{TC}_D$	Terminal count down (borrow) output (active Low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

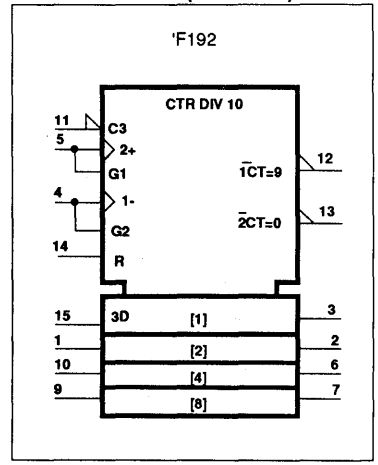
PIN CONFIGURATION



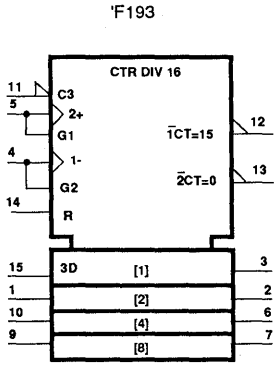
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

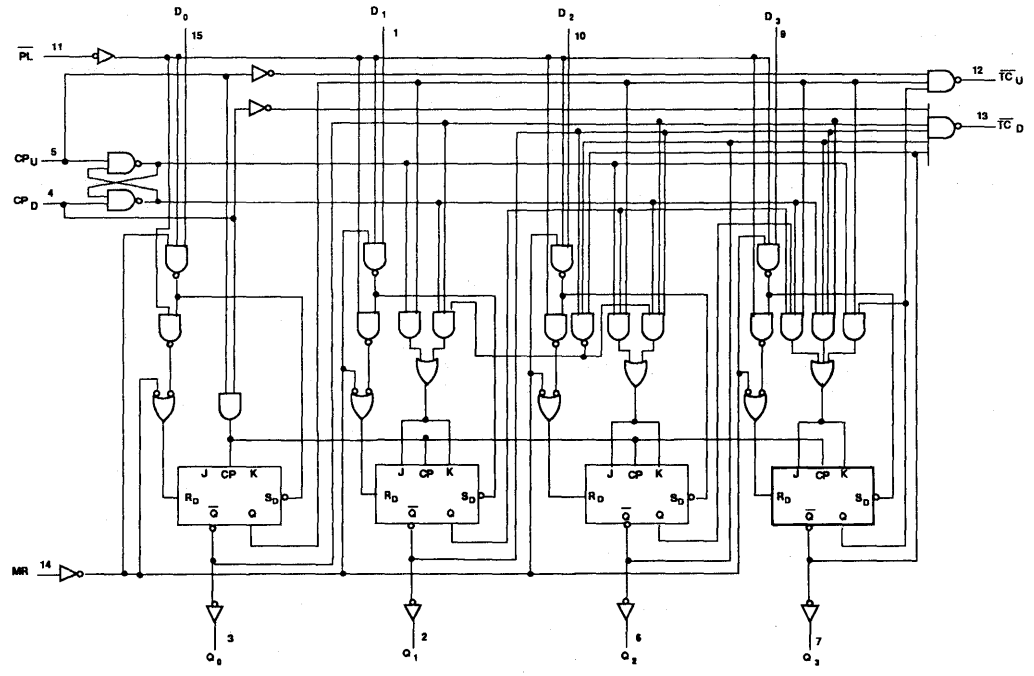


LOGIC SYMBOL(IEEE/IEC)



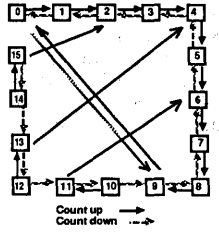
state and CP_D goes Low. The $\overline{TC}$ outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous since there is a two-gate delay time difference added for each stage that is added. The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D_0-D_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs when the Parallel Load ($\overline{PL}$) input is Low. A High level on the Master Reset (MR) input will disable the parallel load gates, override both clock inputs, and sets all Q outputs Low. If one of the clock inputs is Low during and after a reset or load operation, the next Low-to-High transition of the clock will be interpreted as legitimate signal and will be counted.

LOGIC Diagram for 'F192



V_{CC} =pin16
GND=pin 8

STATE DIAGRAM for 'F192



Logic equation for ternminal count

$\overline{TC}_U = Q_0 \cdot Q_3 \cdot \overline{CP}_U$

$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$

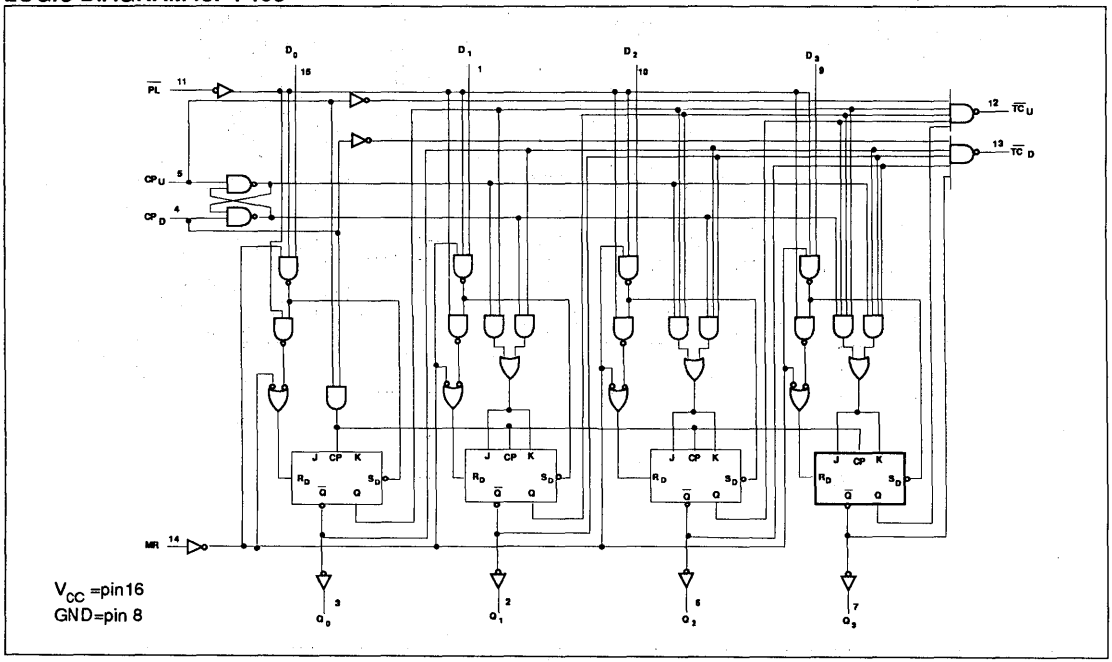
FUNCTION TABLE for ' F192

INPUTS								OUTPUTS						OPERATING MODE
MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$	
H	X	X	L	X	X	X	X	L	L	L	L	H	L	Reset
H	X	X	H	X	X	X	X	L	L	L	L	H	H	
L	L	X	L	L	L	L	L	L	L	L	L	H	L	Parallel load
L	L	X	H	L	L	L	L	L	L	L	L	H	H	
L	L	L	X	H	X	X	H	$Q_n=D_n$				L	H	
L	L	H	X	H	X	X	H	$Q_n=D_n$				H	H	
L	H	↑	H	X	X	X	X	Count up				H[1]	H	Count up
L	H	H	↑	X	X	X	X	Count down				H	H[2]	Count down

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

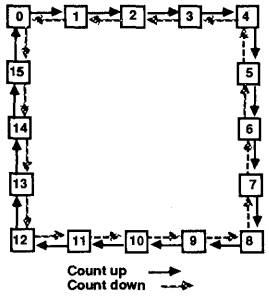
NOTES: 1. $\overline{TC}_U = CP_U$ at terminal count up (HLLH)
2. $\overline{TC}_D = CP_D$ at terminal count down (LLLL)

LOGIC DIAGRAM for 'F193



V_{CC} =pin16
GND=pin 8

STATE DIAGRAM for 'F193



Logic equation for ternminal count

$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$

$\overline{TC}_D = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_D$

FUNCTION TABLE for ' F193

INPUTS								OUTPUTS						OPERATING MODE
MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$	
H	X	X	L	X	X	X	X	L	L	L	L	H	L	Reset
H	X	X	H	X	X	X	X	L	L	L	L	H	H	
L	L	X	L	L	L	L	L	L	L	L	L	H	L	Parallel load
L	L	X	H	L	L	L	L	L	L	L	L	H	H	
L	L	L	X	H	H	H	H	H	H	H	H	L	H	
L	L	H	X	H	H	H	H	H	H	H	H	H	H	
L	H	↑	H	X	X	X	X	Count up				H^1	H	Count up
L	H	H	↑	X	X	X	X	Count down				H	H^2	Count down

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

NOTES: 1. $\overline{TC}_U = CP_U$ at terminal count up (HHHH)
2. $\overline{TC}_D = CP_D$ at terminal count down (LLLL)

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	CP_U, CP_D	V_{CC} = MAX, V_I = 0.5V				-1.8	mA
		others					-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			32	50	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with parallel load and Master reset inputs grounded, all other inputs at 4.5V and and all outputs open.

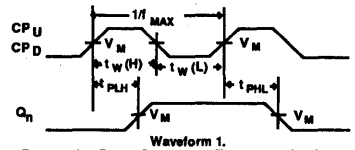
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 2	2.5 3.0	5.5 5.0	8.5 8.0	2.5 3.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to Q_n	Waveform 1	2.5 5.0	5.5 8.5	8.5 12.0	2.5 5.0	9.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 4	2.0 6.0	4.0 9.5	7.0 13.5	1.5 6.0	8.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n	Waveform 3	4.5 5.5	6.5 8.5	10.0 12.0	4.0 5.0	11.0 13.0	ns
t_{PHL}	Propagation delay MR to Q_n	Waveform 5	5.0	7.5	11.0	5.0	12.0	ns
t_{PLH}	Propagation delay MR to $\overline{TC}_U$	Waveform 5	6.0	8.5	12.0	5.5	13.0	ns
t_{PHL}	Propagation delay MR to $\overline{TC}_D$	Waveform 5	5.0	7.5	11.0	5.0	12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 3	6.0 6.0	9.5 9.0	13.5 12.0	6.0 6.0	15.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 4	5.5 4.5	9.0 8.5	13.0 12.5	5.0 4.5	14.0 13.5	ns

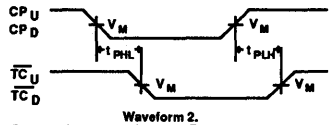
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{PL}$	Waveform 6	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$	Waveform 6	2.0 2.0			2.0 2.0		ns
$t_w(L)$	$\overline{PL}$ Pulse width Low	Waveform 3	6.0			6.0		ns
$t_w(H)$ $t_w(L)$	CP_U or CP_D Pulse width High or Low	Waveform 1	3.5 5.0			3.5 5.0		ns
$t_w(L)$	CP_U or CP_D Pulse width, Low (Change of direction)	Waveform 1	10.0			10.0		ns
$t_w(H)$	MR Pulse width High	Waveform 5	6.0			6.0		ns
t_{REC}	Recovery time $\overline{PL}$ to CP_U or CP_D	Waveform 3	6.0			6.0		ns
t_{REC}	Recovery time MR to CP_U or CP_D	Waveform 5	4.0			4.0		ns

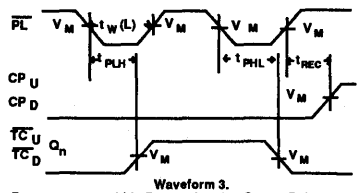
AC WAVEFORMS



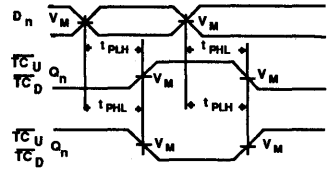
Waveform 1.
Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



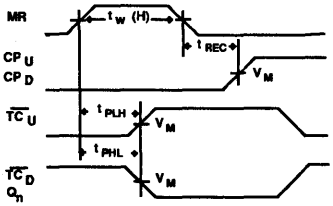
Waveform 2.
Propagation Delay, Clock to Terminal Count



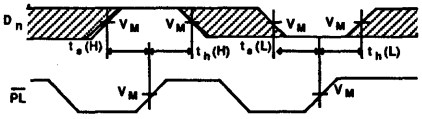
Waveform 3.
Parallel poulse width, Parallel Load to Output Delays, and Parallel Load to Clock Recovery Time



Waveform 4.
Propagation delay, Data to Flip-flop outputs, Terminal Count and Down Outputs



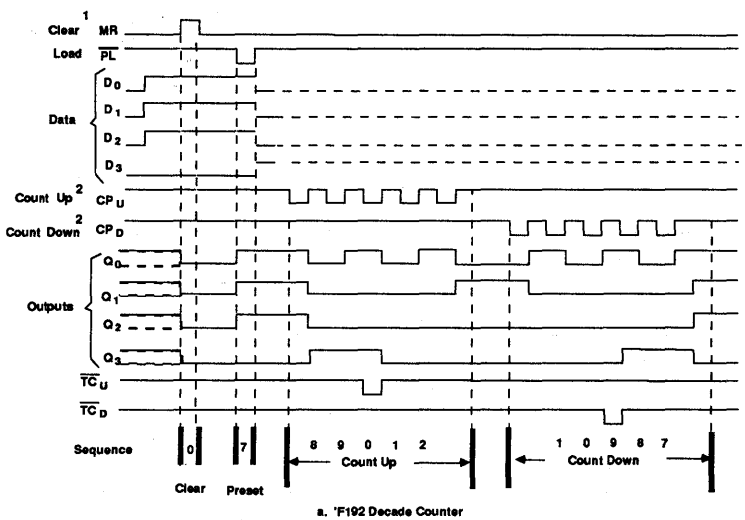
Waveform 5.
Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 6.
Data Setup And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

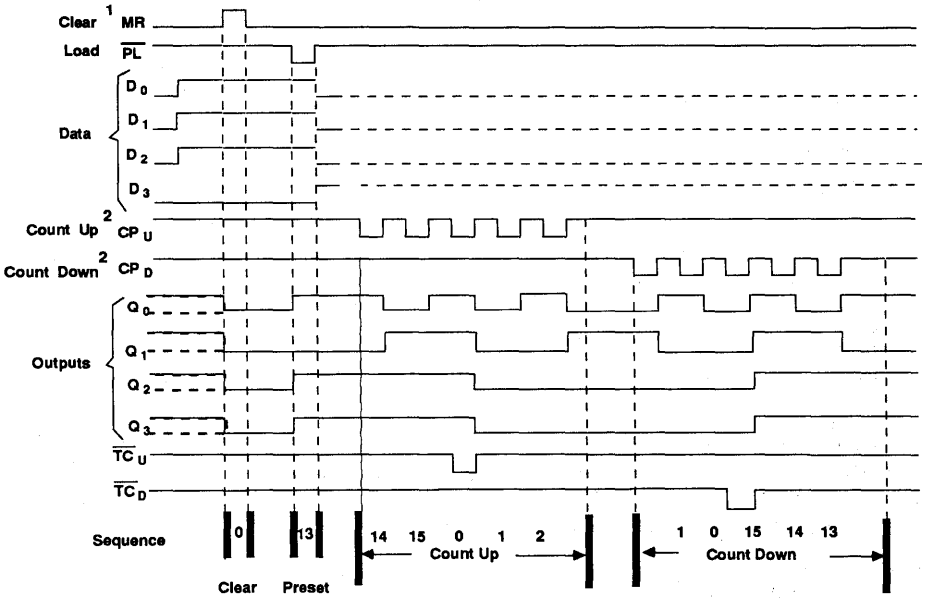
TIMING DIAGRAM (Typical clear, load, and count sequence) for 'F192



a. 'F192 Decade Counter

NOTES: 1. Clear overrides load data and count inputs.
2. When counting up, count down input must be High; when counting down, count up must be High.

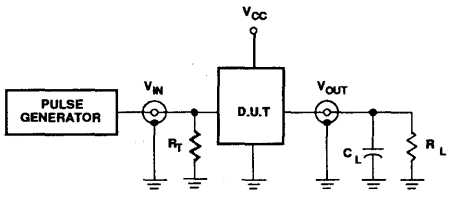
TIMING DIAGRAM (Typical clear, load, and count sequence) for 'F193



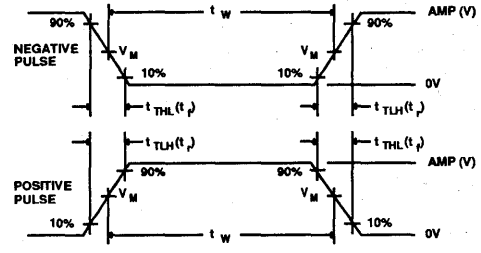
b. 'F193 Binary Counter

NOTES: 1. Clear overrides load data and count inputs.
2. When counting up, count down input must be High; whern counting down, count up must be High.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F194
Shift Register

FAST Products

FEATURES

- **Shift right and shift left capability**
- **Synchronous parallel and serial data transfer**
- **Easily expanded for both serial and parallel operation**
- **Asynchronous Master Reset**
- **Hold (do nothing) mode**

4-Bit Bidirectional Universal Shift Register
Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F194	150MHz	33mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F194N
16-Pin Plastic SO	N74F194D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Parallel data inputs	1.0/1.0	20µA/0.6mA
D_{SR}	Serial data input (Shift Right)	1.0/1.0	20µA/0.6mA
D_{SL}	Serial data input (Shift Left)	1.0/1.0	20µA/0.6mA
S_0, S_1	Mode Select inputs	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Asynchronous Master Reset input (Active Low)	1.0/1.0	20µA/0.6mA
Q_0 - Q_3	Data outputs	50/33	1.0mA/20mA

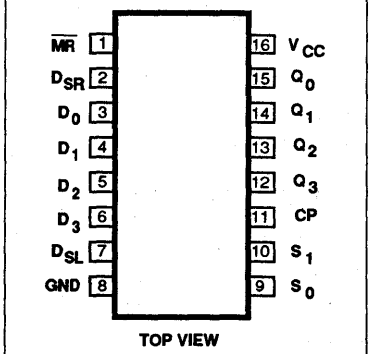
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

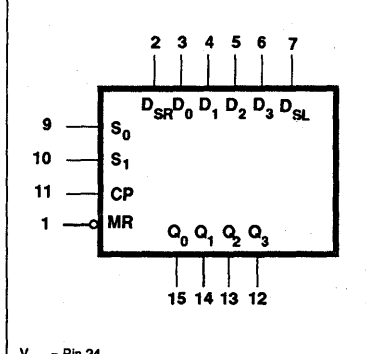
The functional characteristics of the 74F194 4-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Function Table. The register is fully synchronous, with all operations taking place in less than 9ns (typical) for 74F, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

The 'F194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S_0 and S_1. As shown in the Mode Select-Function Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.), or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.), or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S_0 and S_1 are Low, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data inputs (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation. Mode Select and data inputs on the 'F194 are edge-triggered, responding only to the Low-to-High transition of the Clock (CP). Therefore, the only timing restriction is that the Mode Select and selected data inputs must be stable one setup time prior to the Low-to-High transition of the clock pulse. Signals on the the Mode Select, Parallel Data (D_0 -D_3) and Serial Data (D_{SR}, D_{SL}) can change when the clock is in either state, provided only the recommended setup and hold times, with respect to the clock rising edge, are observed. The four Parallel Data inputs (D_0 -D_3) are D-type inputs. Data appearing on (D_0 -D_3) inputs when S_0 and S_1 are High is transferred to the Q_0 -Q_3 outputs respectively, following the next Low-to-High transition of the clock. When Low, the asynchronous Master Reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs Low.

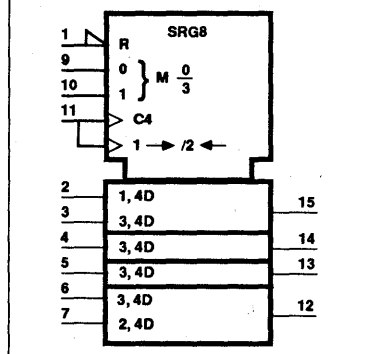
PIN CONFIGURATION



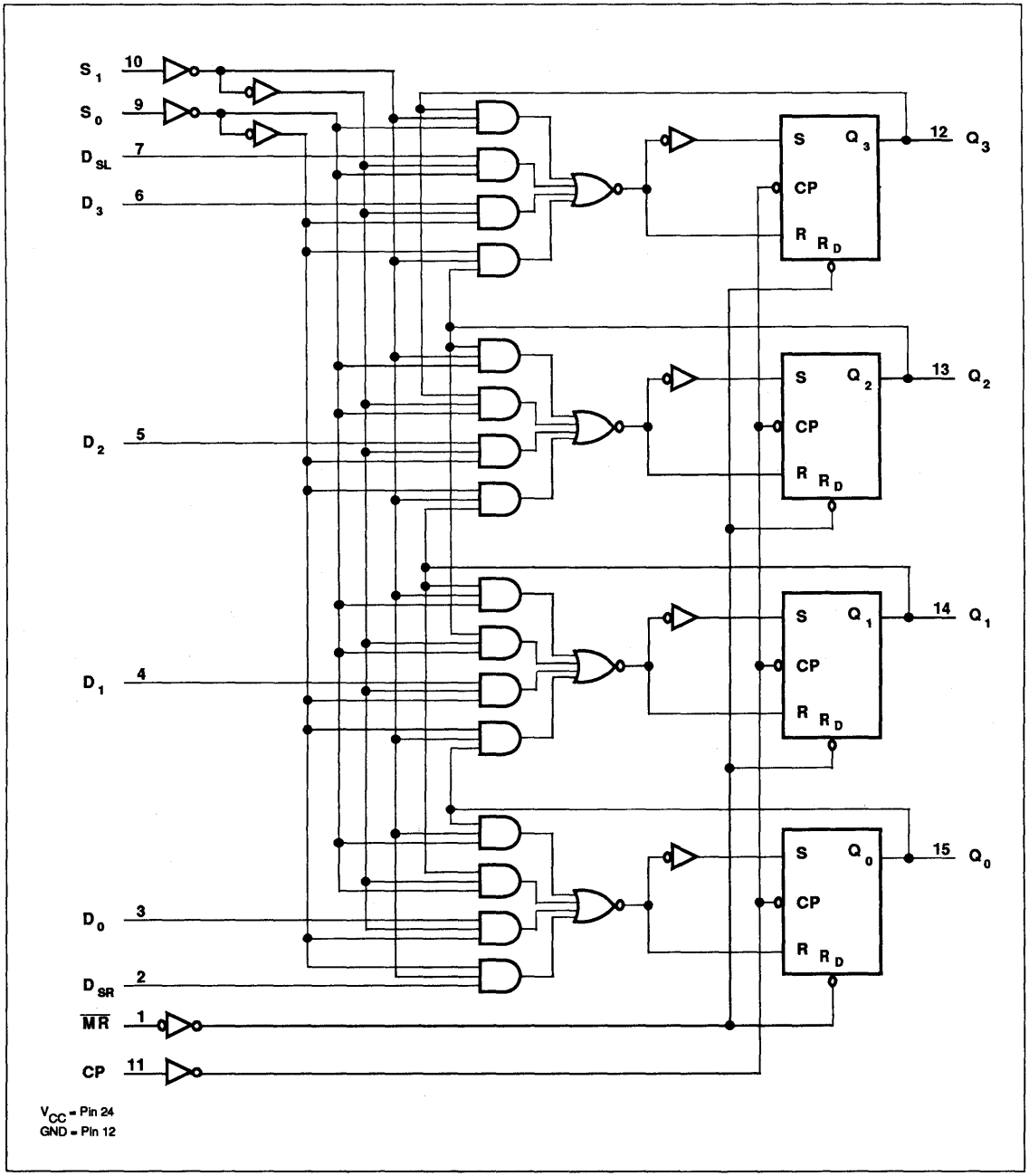
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS				OPERATING MODES
CP	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3	
X	L	X	X	X	X	X	L	L	L	L	Reset (clear)
X	H	l	l	X	X	X	q_0	q_1	q_2	q_3	Hold (do nothing)
↑	H	h	l	X	l	X	q_1	q_2	q_3	L	Shift left
↑	H	h	l	X	h	X	q_1	q_2	q_3	H	
↑	H	l	h	l	X	X	L	q_0	q_1	q_2	Shift right
↑	H	l	h	h	X	X	H	q_0	q_1	q_2	
↑	H	h	h	X	X	d_n	d_0	d_1	d_2	d_3	Parallel load

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage[3]	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[4]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[5] (total)	V_{CC} = MAX			33	46	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Output High state will change to Low state if an external voltage of less than 0.0V is applied.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
5. With all outputs open, D_i inputs grounded and a 4.5V applied to S_0, S_1, MR and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5V applied to CP.

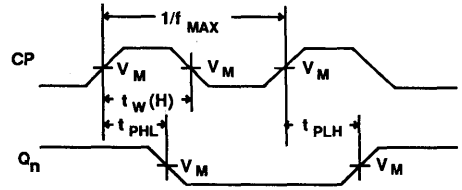
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	105	150		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.5 3.5	5.2 5.5	7.0 7.0	3.5 3.5	8.0 8.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	4.5	8.6	12.0	4.5	14.0	ns

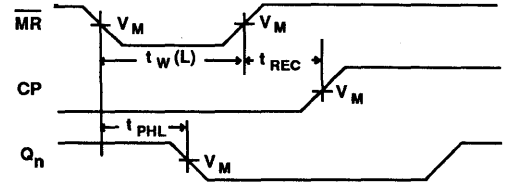
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n, D_{SL}, D_{SR} to CP	Waveform 3	4.0 4.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n, D_{SL}, D_{SR} to CP	Waveform 3	0 0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_n to CP	Waveform 3	8.0 8.0			9.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_n to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$	CP Pulse width, High	Waveform 1	5.0			5.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	5.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	7.0			8.0		ns

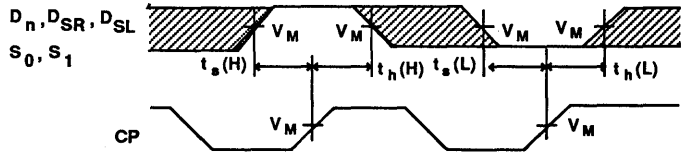
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



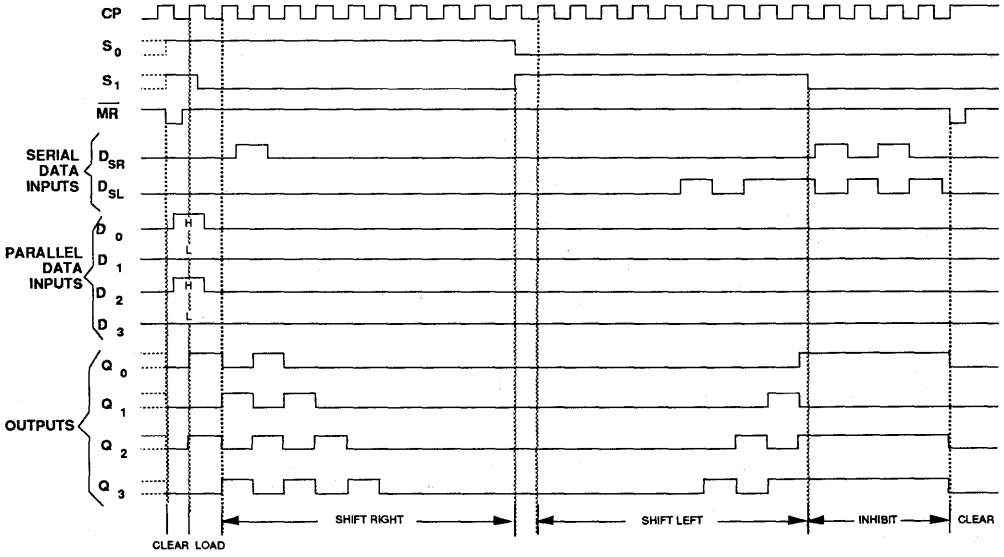
Waveform 2. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



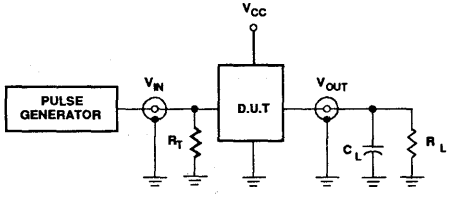
Waveform 3. Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

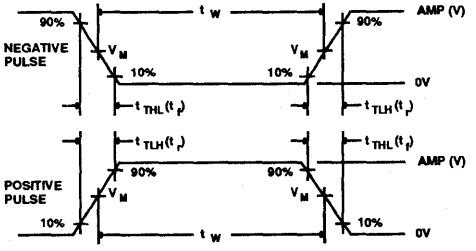
TIMING DIAGRAM (Typical Clear, Load, Shift-Right, Shift-Left and Inhibit Sequence)



TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F195
Shift Register

4-Bit Parallel-Access Shift Register
Product Specification

FAST Products

FEATURES
- **High-impedance NPN base inputs for reduced loading (20μA in Low and High states)**
- **Shift right and parallel load capability**
- **J - $\overline{K}$(D) inputs to first stage**
- **Complement output from last stage**
- **Asynchronous Master Reset**

DESCRIPTION

The 74F195 is a 4-bit Parallel Access Shift Register and its functional characteristics are indicated in the Logic diagram and Function Table. The device is useful in a variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The 74F195 operates in two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is High, and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each Low -to-High clock transition.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F195	115MHz	45mA

ORDERING INFORMATION

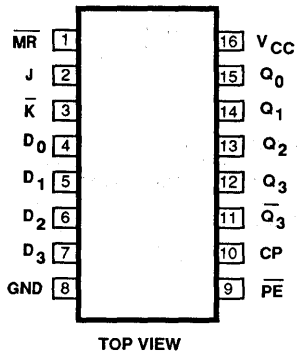
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F195N
16-Pin Plastic SO	N74F195D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Parallel data inputs	1.0/0.033	20μA/20μA
J, $\overline{K}$	J - K or D type serial inputs	1.0/0.033	20μA/20μA
$\overline{PE}$	Parallel Enable input	1.0/0.033	20μA/20μA
CP	Clock Pulse input (Active rising edge)	1.0/0.033	20 A/20 μA
$\overline{MR}$	Master Reset input (Active Low)	2.0/0.066	40μA/40μA
Q_0 - Q_3, $\overline{Q}_3$	Data outputs	50/33	1.0mA/20mA

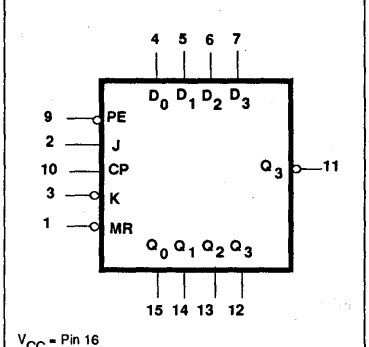
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

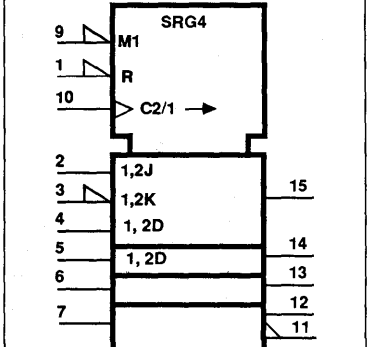


TOP VIEW

LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Shift Register | FAST 74F195

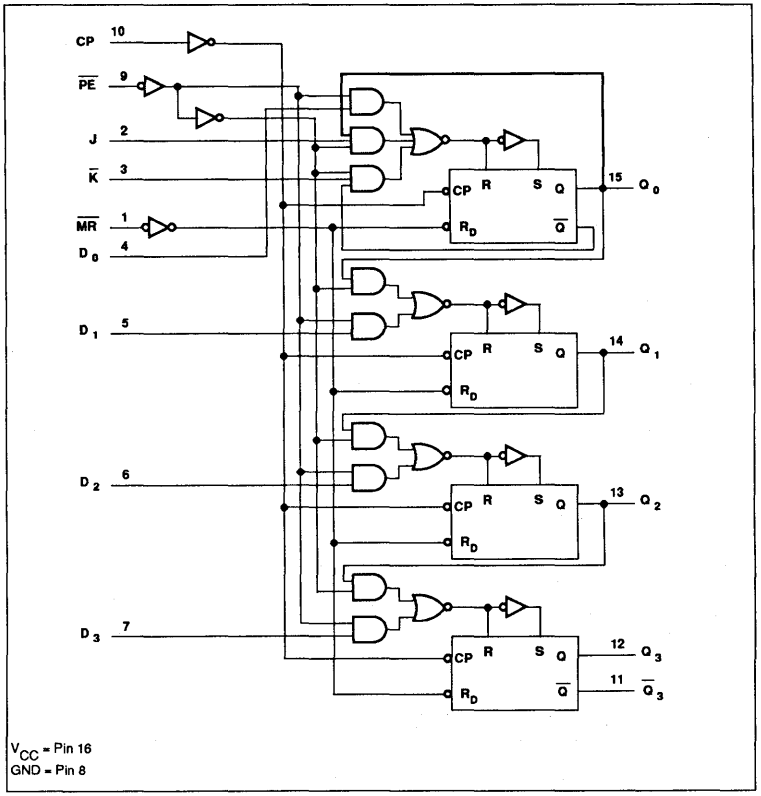
The J and $\overline{K}$ inputs provide the flexibility of the J-$\overline{K}$ type input for special applications, and by tying the two together the simple D-type input is made for general applications.

The device appears as four common clocked D flip-flops when the $\overline{PE}$ input is Low. After the Low-to-High clock transition, data on the parallel inputs (D_0 - D_3) is transferred to the respective Q_0 - Q_3 outputs. Shift left operation (Q_3 - Q_2) can be achieved by tying the Q_n outputs to the D_{n-1} inputs and holding the $\overline{PE}$ input Low.

All parallel and serial data transfers are synchronous, occurring after each Low-to-High clock transition. The 74F195 utilizes edge-triggering, therefore there is no restriction on the activity of the J, $\overline{K}$, D_n, and $\overline{PE}$ inputs for logic operation, other than the set-up and hold time requirements.

A Low on the asynchronus Master Reset ($\overline{MR}$) input sets all Q outputs Low, independent of any other input condition.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS					OPERATING MODES
$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$	
L	X	X	X	X	X	L	L	L	L	H	Reset (clear)
H	↑	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$	Shift, set First stage
H	↑	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$	Shift, reset First stage
H	↑	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$	Shift, toggle First stage
H	↑	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$	Shift, retain First stage
H	↑	l	X	X	d_n	d_0	d_1	d_2	d_3	$\overline{d}_3$	Parallel load

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} =MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} =MAX	±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current	others	V_{CC} = MAX, V_I = 2.7V				20	µA
		$\overline{MR}$					40	µA
I_{IL}	Low-level input current	others	V_{CC} = MAX, V_I = 0.5V				-20	µA
		$\overline{MR}$					-40	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			45	58	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

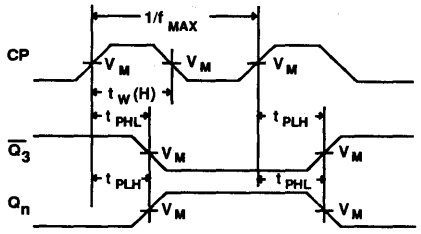
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	$\overline{PE}$ mode	Waveform 1	120	130		110		MHz
		Toggle mode		100	115		90		
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	4.0 4.0	6.5 6.5	9.5 9.0	4.0 4.0	10.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_3$		Waveform 1	7.0 4.5	10.0 7.0	13.0 9.0	7.0 4.0	13.5 9.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n		Waveform 2	5.0	7.5	10.5	5.0	11.0	ns
t_{PLH}	Propagation delay $\overline{MR}$ to $\overline{Q}_3$		Waveform 2	7.0	10.0	13.5	7.0	14.0	ns

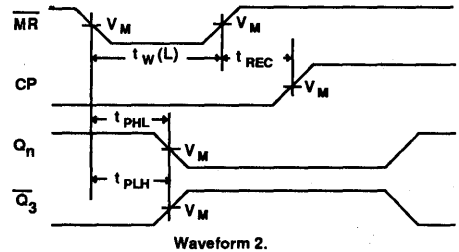
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J, $\overline{K}$ and D_n to CP	Waveform 3	4.0 4.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J, $\overline{K}$ and D_n to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 4	3.0 4.0			3.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 4	0 0			0 0		ns
$t_w(H)$	CP Pulse width, High	Waveform 1	6.0			6.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	5.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	6.0			6.0		ns

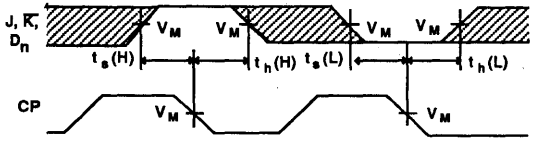
AC WAVEFORMS



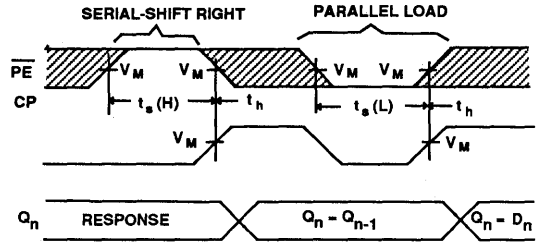
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2.
Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



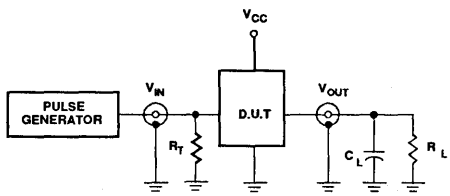
Waveform 3. Data Setup And Hold Times



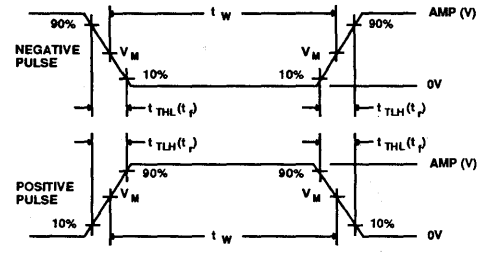
Waveform 4. Setup And Hold Times, Parallel Enable To Clock

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F198
Shift Register

8-Bit Bidirectional Universal Shift Register
Product Specification

FAST Products

FEATURES
- **Buffered clock and control inputs**
- **Shift right, shift left, and parallel load capability**
- **Asynchronous Master Reset**

DESCRIPTION

The 74F198, Bidirectional Universal Shift Register is designed to incorporate virtually all of the features a system designer may want in a shift register. This circuit features parallel inputs and outputs, shift right and shift left serial inputs, operating mode select inputs, and a direct overriding master reset input. The register has four distinct modes of operation:

Parallel (broadside) load
Shift right (in the direction Q_0 toward Q_7)
Shift left (in the direction Q_7 toward Q_0)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the 8 bits of data and taking both mode control inputs, S_0 and S_1, High. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F198	95MHz	73mA

ORDERING INFORMATION

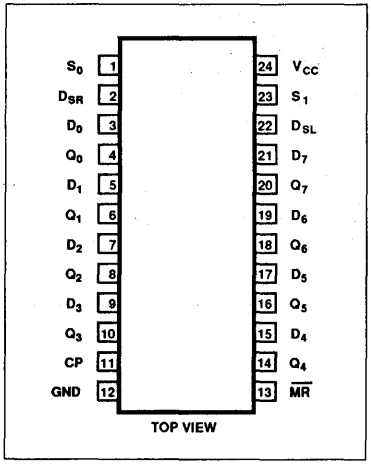
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F198N
24-Pin Plastic SOL	N74F198D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

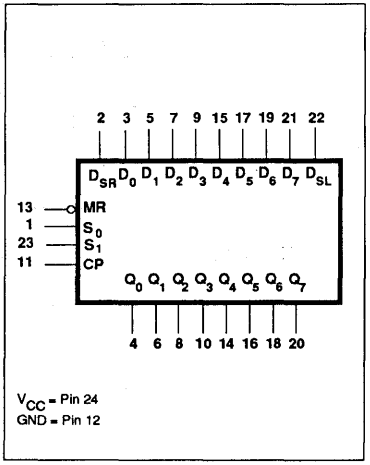
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Parallel data inputs	1.0/1.0	20µA/0.6mA
D_{SR}	Serial data input (Shift Right)	1.0/1.0	20µA/0.6mA
D_{SL}	Serial data input (Shift Left)	1.0/1.0	20µA/0.6mA
S_0 - S_1	Mode Select inputs	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (Active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (Active Low)	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

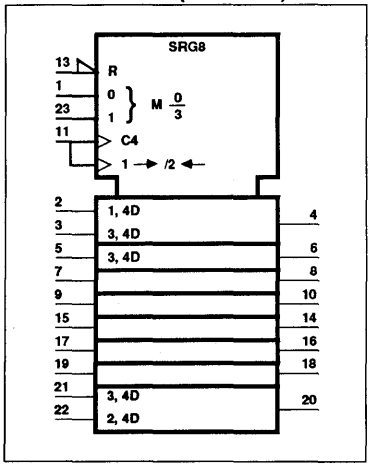
PIN CONFIGURATION



LOGIC SYMBOL



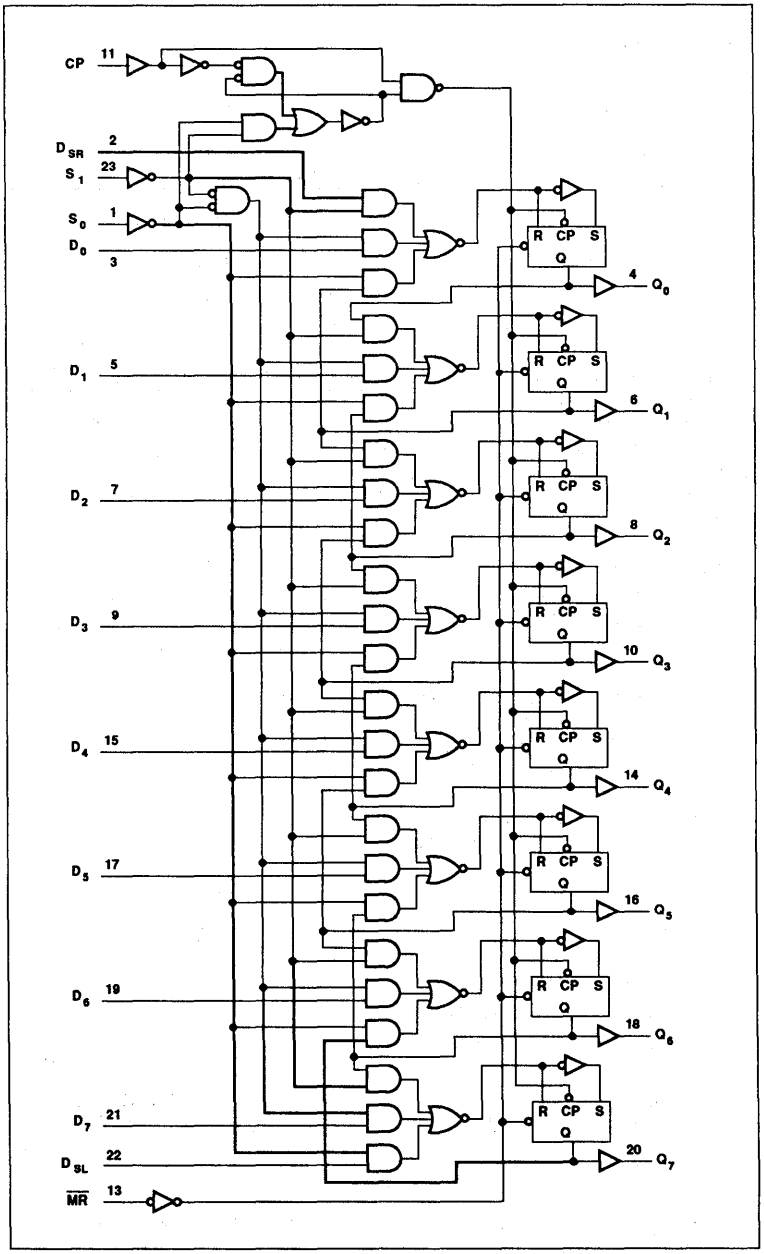
LOGIC SYMBOL(IEEE/IEC)



Shift right is accomplished synchronously, with the rising edge of the clock pulse when S_0 is High and S_1 is Low. Serial data for this mode is entered at the right data input (D_{SR}). When S_0 is Low and S_1 is High, data shifts left synchronously and new data is entered at the shift-left serial input (D_{SL}).

Clocking of the flip-flops is inhibited when both mode control inputs are Low.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS				
$\overline{MR}$	Mode		CP	Serial		Parallel	Q_0	Q_1	...	Q_6	Q_7
	S_0	S_1		Left	Right	0...7					
L	X	X	X	X	X	X	L	L		L	L
H	X	X	L	X	X	X	Q_{00}	Q_{10}		Q_{60}	Q_{70}
H	H	H	↑	X	X	0...7	0	1		6	7
H	H	L	↑	X	H	X	H	Q_{0n}		Q_{5n}	Q_{6n}
H	H	L	↑	X	L	X	L	Q_{0n}		Q_{5n}	Q_{6n}
H	L	H	↑	H	X	X	Q_{1n}	Q_{2n}		Q_{7n}	H
H	L	H	↑	L	X	X	Q_{1n}	Q_{2n}		Q_{7n}	L
H	L	L	X	X	X	X	Q_{00}	Q_{10}		Q_{60}	Q_{70}

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High transition of designated input
0...7 = The level of steady input at inputs 0 through 7, respectively.
Q_{00}, Q_{10}, Q_{60}, Q_{70} = The level of Q_0, Q_1, Q_6, Q_7, respectively, before the indicated steady state input conditions were established.
Q_{0n}, Q_{1n}, Q_{6n}, Q_{7n} = The level of Q_0, Q_1, Q_6, Q_7, respectively, before the most recent Low-to-High clock transition.

ABSOLUTE MAXIMUM RATINGS

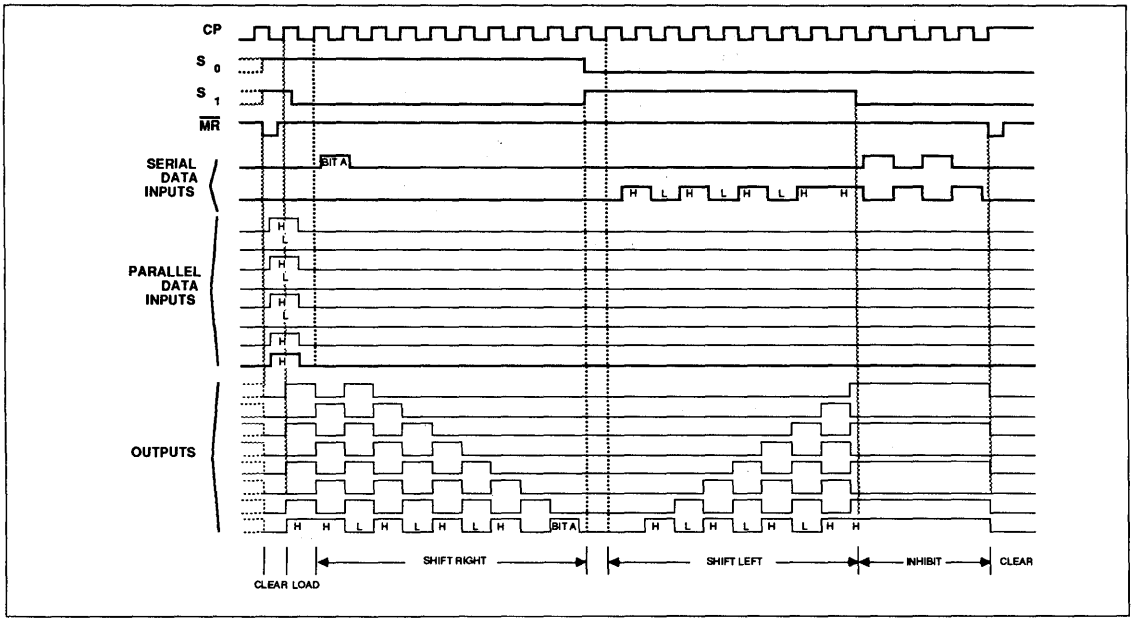
(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

TYPICAL TIMING DIAGRAM



DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			70	100	mA
		I_{CCL}				75	110	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

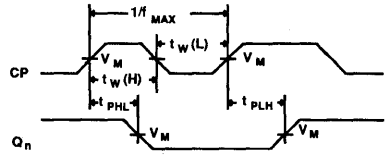
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	95		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	5.0 6.0	7.5 8.5	10.0 11.0	4.5 5.5	11.0 12.0	ns
t_{PHL}	Propagation delay	Waveform 3	5.0	7.5	10.0	4.5	11.0	ns

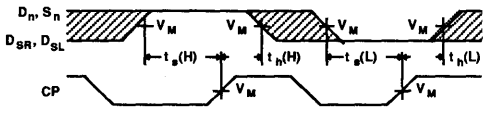
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2	0.0 3.0			0.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2	0.0 3.5			1.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_{SR}, D_{SL} to CP	Waveform 2	0.0 3.0			0.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_{SR}, D_{SL} to CP	Waveform 2	0.0 2.5			0.0 3.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_n to CP	Waveform 2	9.0 6.0			10.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_n to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	5.0 5.0			6.0 6.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 3	5.0			5.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 3	5.0			6.0		ns

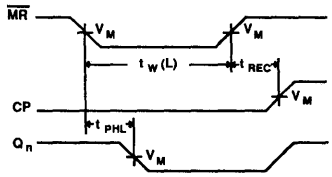
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths, and Maximum Clock Frequency



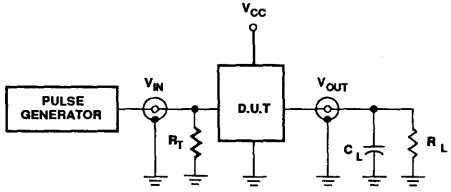
Waveform 2. Setup Time and Hold Time



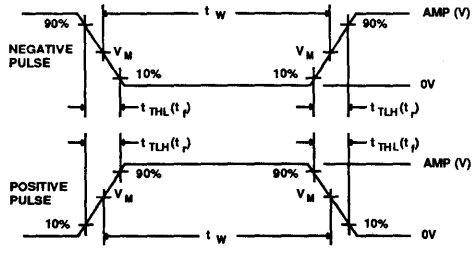
Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F199
Shift Register

8-Bit Parallel-Access Shift Register

FAST Products

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F199	95MHz	70mA

FEATURES

- Buffered clock and control inputs
- Shift right and parallel load capability
- Fully synchronous data transfers
- J - $\overline{K}$(D) inputs to first stage
- Clock enable for hold (do nothing) mode
- Asynchronous Master Reset

DESCRIPTION

The 74F199 is an 8-bit Parallel Access Shift Register and its functional characteristics are indicated in the Logic diagram and Function Table. The device is useful in a variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The 74F199 operates in two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is High, and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2$ following each Low-to-High clock transition.

ORDERING INFORMATION

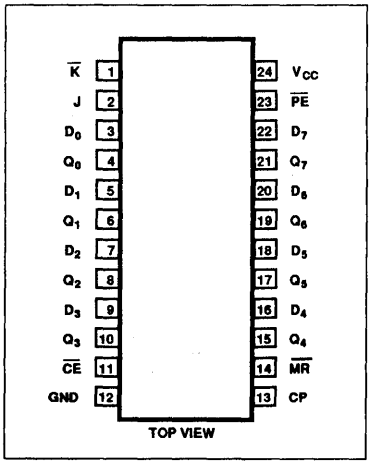
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F199N
24-Pin Plastic SOL	N74F199D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

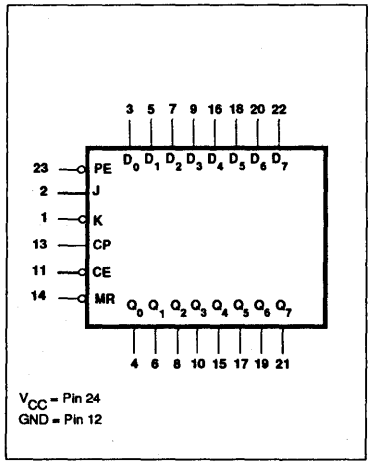
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Parallel data inputs	1.0/1.0	20µA/0.6mA
J, $\overline{K}$	J and K inputs	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input	1.0/1.0	20µA/0.6mA
$\overline{CE}$	Clock Enable input	1.0/1.0	20µA/0.6mA
CP	Clock Pulse inputs (Active rising edge)	1.0/1.0	20 A/0.6mA
$\overline{MR}$	Master Reset input (Active Low)	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

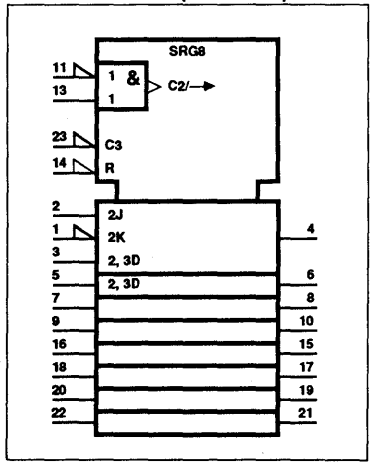
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



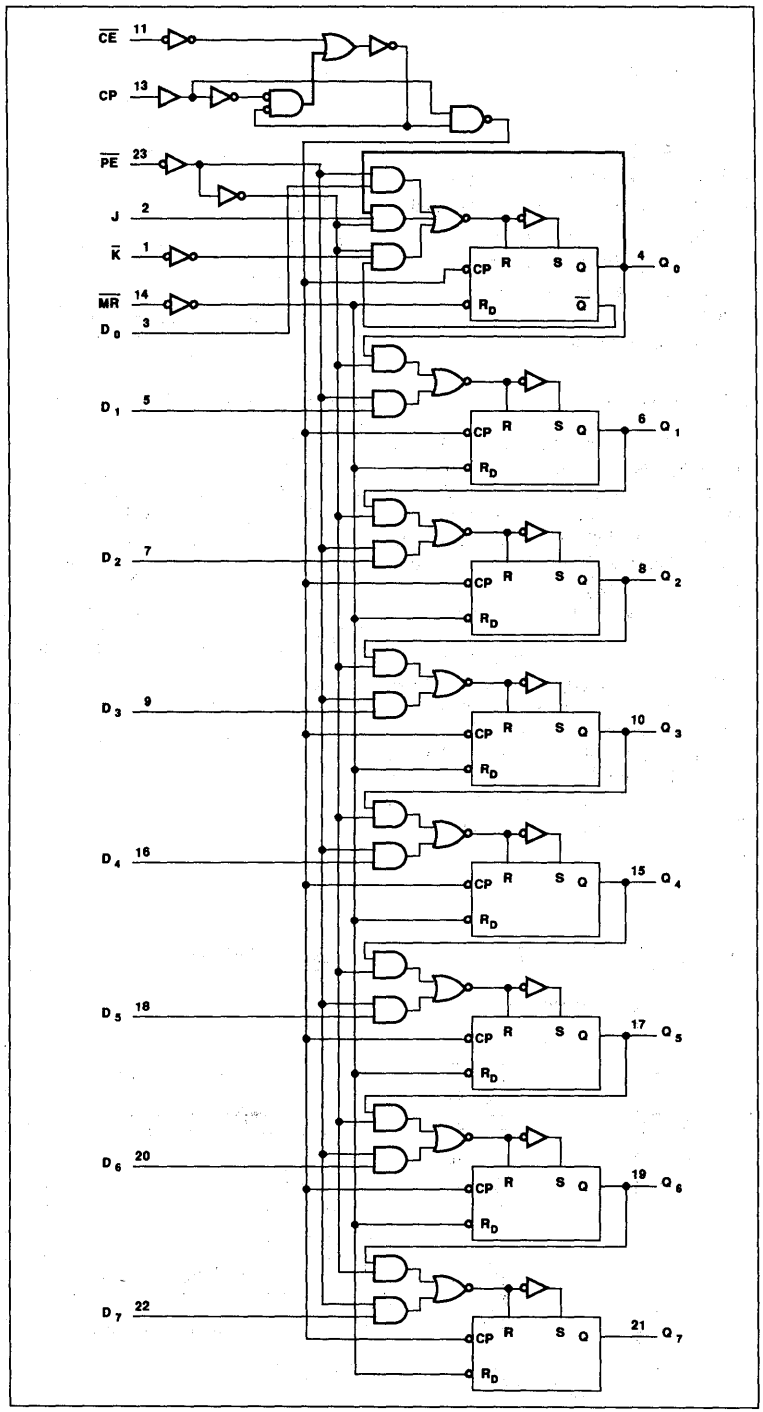
The J and $\overline{K}$ inputs provide the flexibility of the J-$\overline{K}$ type input for special applications, and by tying the two together the simple D-type input is made for general applications.

The device appears as eight common clocked D flip-flops when the $\overline{PE}$ input is Low. After the Low-to-High clock transition, data on the parallel inputs (D_0 - D_7) is transferred to the respective Q_0 - Q_7 outputs.

All parallel and serial data transfers are synchronous, occurring after each Low-to-High clock transition. The 74F199 utilizes edge-triggered, therefore there is no restriction on the activity of the J, $\overline{K}$, Dn, and $\overline{PE}$ inputs for logic operation, other than the set-up and hold time requirements.

A Low on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously forcing all bit positions to a Low state.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS					OPERATING MODES
$\overline{MR}$	CP	$\overline{CE}$	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0	Q_1	...	Q_6	Q_7	
L	X	X	X	X	X	X	L	L	...	L	L	Reset (clear)
H	↑	l	h	h	h	X	H	q_0	...	q_5	q_6	Shift, set First stage
H	↑	l	h	l	l	X	L	q_0	...	q_5	q_6	Shift, reset First stage
H	↑	l	h	h	l	X	$\overline{q}_0$	q_0	...	q_5	q_6	Shift, toggle First stage
H	↑	l	h	l	h	X	q_0	q_0	...	q_5	q_6	Shift, retain First stage
H	↑	l	l	X	X	d_n	d_0	d_1	...	d_6	d_7	Parallel load
H	↑	h	X	X	X	X	q_0	q_1	...	q_6	q_7	Hold (do nothing)

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

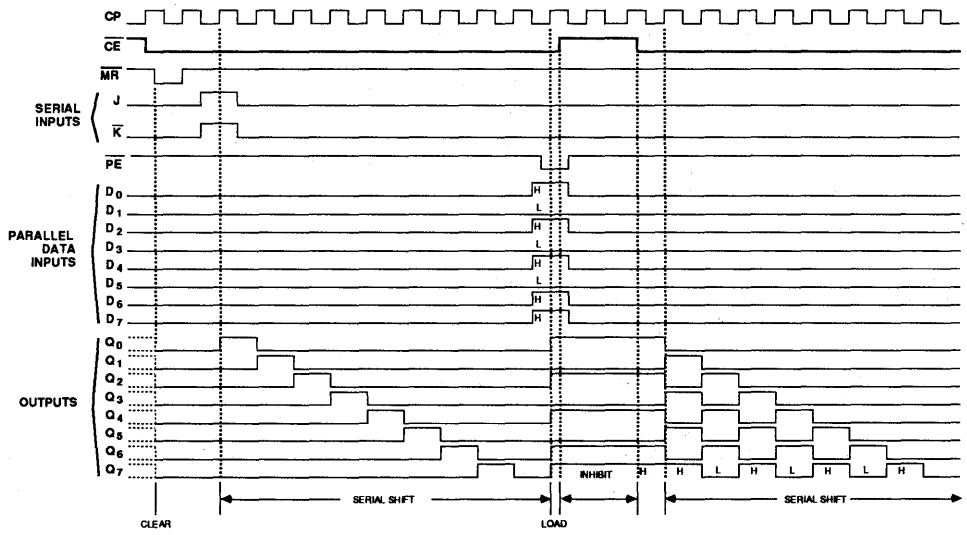
(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

TYPICAL TIMING DIAGRAM



Typical Load, Serial-Shift, Inhibit And Clear Sequences

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			65	90	mA
		I_{CCL}				75	105	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

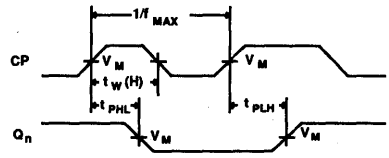
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	95		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	5.5 6.5	8.0 9.5	11.0 12.5	4.5 3.5	12.0 13.5	ns
t_{PHL}	Propagation delay, $\overline{MR}$ to Q_n	Waveform 2	5.5	8.0	10.5	5.0	12.0	ns

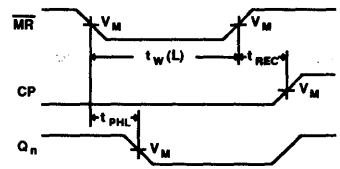
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 3	0.0 1.5			0.0 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 3	2.0 4.5			2.5 5.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low J, $\overline{K}$ to CP	Waveform 3	0.0 2.5			0.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J, $\overline{K}$ to CP	Waveform 3	0.0 3.5			0.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CE}$ to CP	Waveform 3	0.0 2.5			0.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP	Waveform 3	0.0 4.5			0.0 5.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 3	8.0 8.0			9.0 9.0		ns
$t_h(H)$ $t_h(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_w(H)$	CP Pulse width, High	Waveform 1	4.5			5.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	4.0			4.5		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 2	5.5			6.5		ns

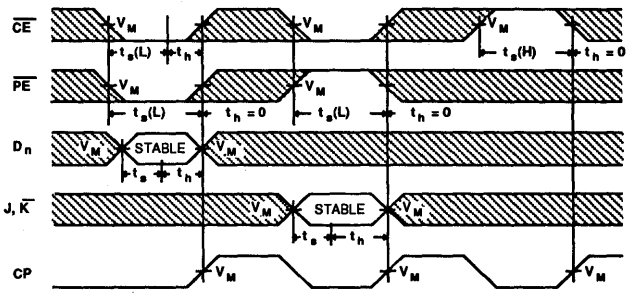
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths, and Maximum Clock Frequency



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

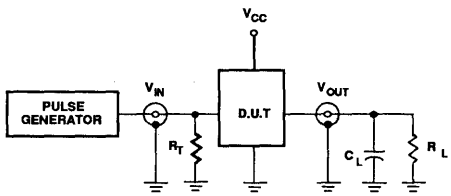


Waveform 3. Setup Time and Hold Time

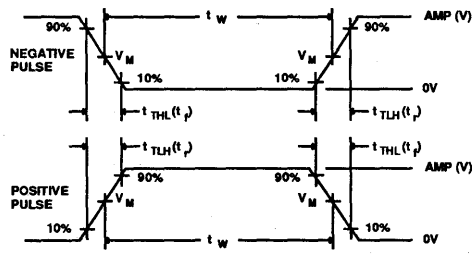
NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F219A

64-Bit TTL Bipolar RAM, Non-Inverting (3-State)

FAST Products

Preliminary Specification

FEATURES

- **Address access time: 10 ns**
- **Power dissipation: 4.3 mW/bit typ**
- **Schottky clamped TTL**
- **One chip enable**
- **Non-inverting outputs (For inverting outputs see 74F189A)**
- **I/O**
  - **Inputs: PNP Buffered**
  - **Outputs: 3-state**

APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Push down stacks**
- **Control store**

DESCRIPTION

The 74F219A is a high speed , 64-Bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are in High impedance state whenever the Chip Enable ($\overline{CE}$) is High. The outputs are active only in the READ mode ($\overline{WE}$ = High) and the output data is the same polarity as of the stored data.

TYPE	TYPICAL ACCESS TIME	TYPICAL SUPPLY CURRENT (TOTAL)
74F219A	10ns	50mA

ORDERING INFORMATION

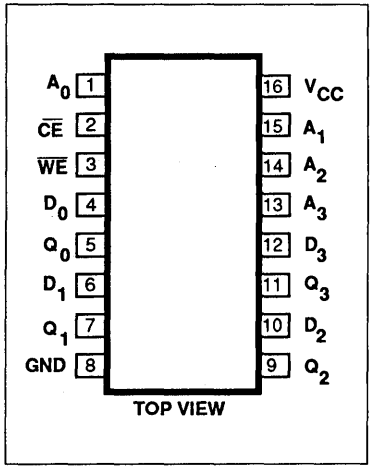
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F219AN
16-Pin Plastic SO	N74F219AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

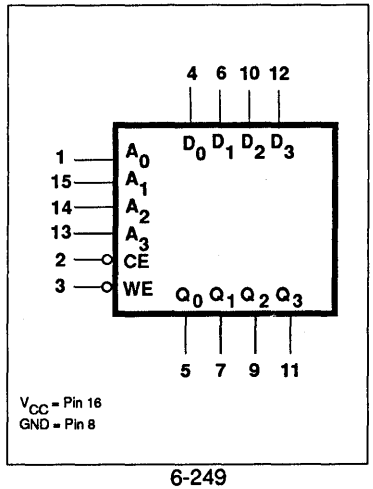
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0- D_3	Data inputs	1.0/1.0	20µA/0.6mA
A_0- A_3	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{CE}$	Chip Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{WE}$	Write Enable input (active Low)	1.0/1.0	20µA/0.6mA
Q_0- Q_3	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

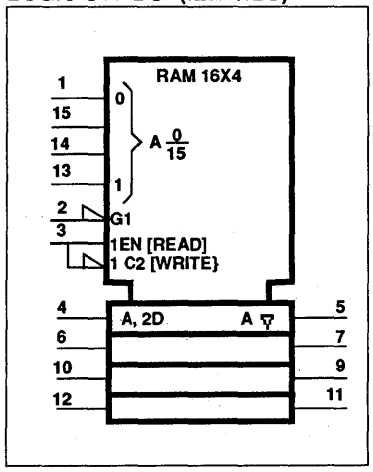
PIN CONFIGURATION



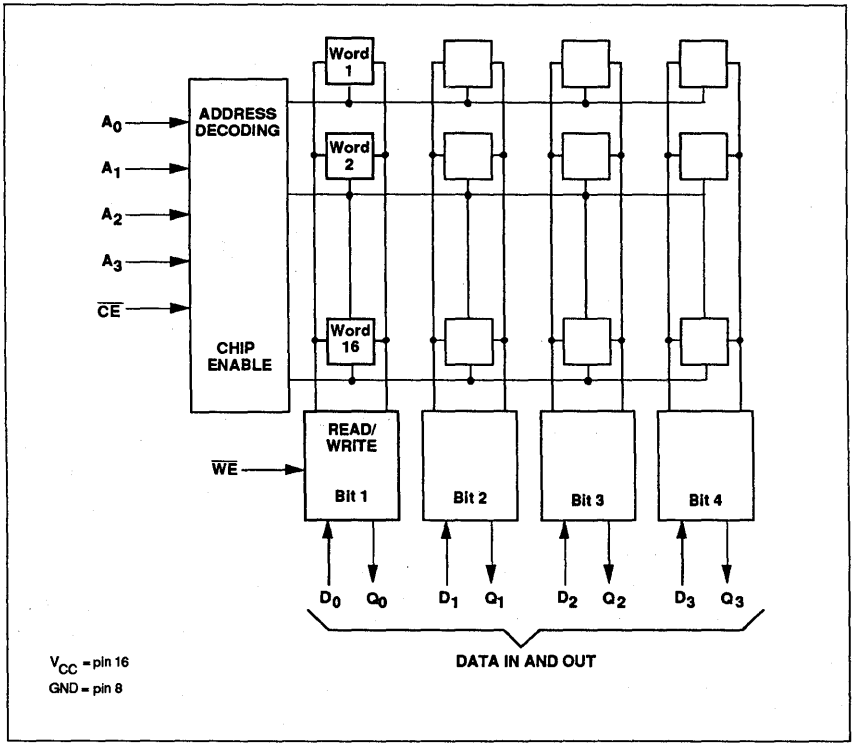
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUT	OPERATING MODE
$\overline{CE}$	$\overline{WE}$	D_n	Q_n	
L	H	X	Stored data	Read
L	L	L	High impedance	Write "0"
L	L	H	High impedance	Write "1"
H	X	X	High impedance	Disable Input

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current High-level voltage applied	V_{CC} = MAX, V_O = 2.7V				50	mA
I_{OZL}	Off-state output current Low-level voltage applied	V_{CC} = MAX, V_O= 0.5V				-50	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, $\overline{CE}$ = $\overline{WE}$ = GND				70	mA
C_{IN}	Input capacitance	V_{CC} = MAX, V_{IN} = 2.0V			5		pF
C_{OUT}	Output capacitance	V_{CC} = MAX, V_{OUT} = 2.0V			8		pF

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

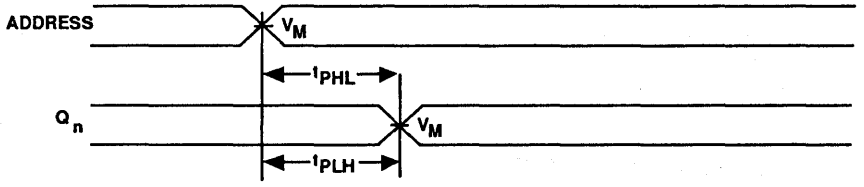
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Access time	Propagation delay A_n to Q_n	Waveform 1					10.0	ns
t_{PZH} t_{PZL}		Enable time $\overline{CE}$ to Q_n	Waveform 2					7.5	ns
t_{PHZ} t_{PLZ}	Disable time $\overline{CE}$ to Q_n		Waveform 3					7.5	ns
t_{PZH} t_{PZL}	Response time (Enable time) $\overline{WE}$ to Q_n		Waveform 4					8.5	ns
t_{PHZ} t_{PLZ}	Write Recovery time (Disable time) $\overline{WE}$ to Q_n		Waveform 4					7.5	ns

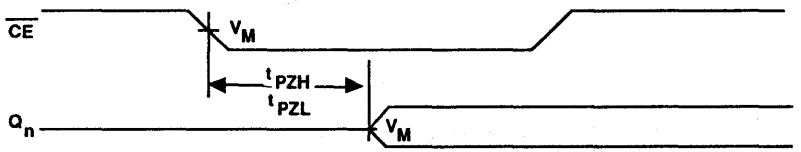
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time $\overline{WE}$ to A_n	Waveform 4				0 0		ns
$t_h(H)$ $t_h(L)$	Hold time $\overline{WE}$ to A_n	Waveform 4				0.5 0.5		ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{WE}$ to D_n	Waveform 4				5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time $\overline{WE}$ to D_n	Waveform 4				0 0		ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{WE}$ to $\overline{CE}$	Waveform 4				4.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold time $\overline{WE}$ to $\overline{CE}$	Waveform 4				4.0 4.0		ns
$t_w(L)$	Pulse width, Low $\overline{WE}$	Waveform 4				6.5		ns

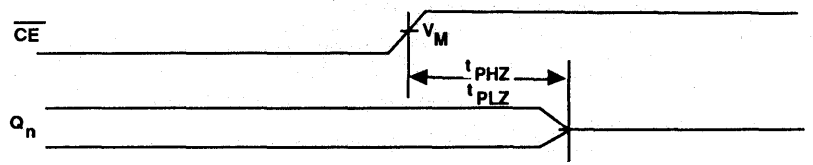
AC WAVEFORMS



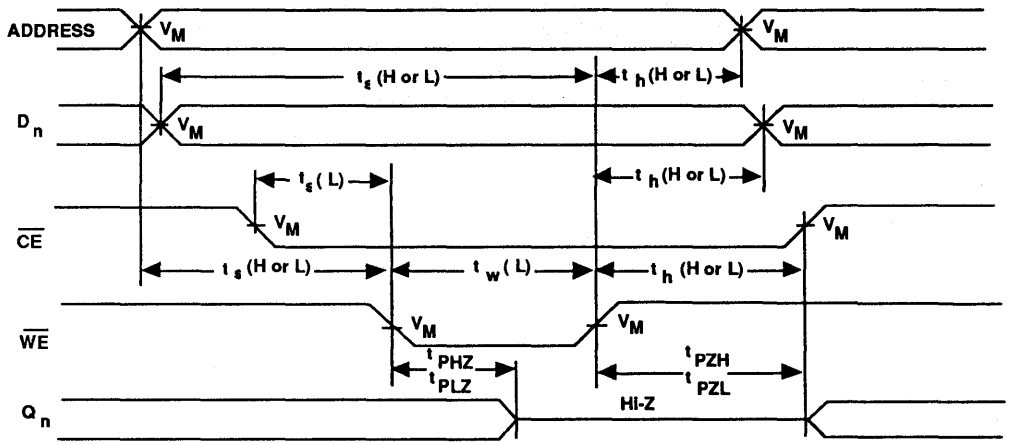
Waveform1. Read Cycle, Address Access Time



Waveform 2. Read Cycle, Chip Enable Access Time



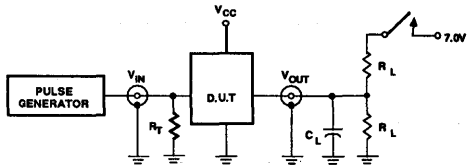
Waveform 3. Read Cycle, Chip Disable Time



Waveform 4. Write Cycle

NOTES: 1. For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

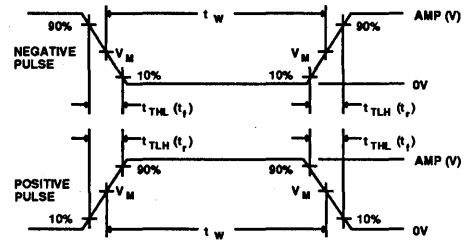
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F222

16X4 Synchronous FIFO With Ready Enables (3-State)

Preliminary Specification

FAST Products

FEATURES

- **Independent synchronous inputs and outputs**
- **Organized as 16-words of 4 bits**
- **DC to 50MHz data rate**
- **3-state outputs**
- **Cascadable in word-width and depth direction**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F222	50MHz	90mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	74F222N
20-Pin Plastic SOL	74F222D

DESCRIPTION

This 64-bit active element First-In-First-Out (FIFO) is a monolithic Schottky-clamped transistor-transistor logic (STTL) array organized as 16-words of 4-bits each. A memory system using the 'F222 can be easily expanded in multiples of 15m+1 words or of 4n bits, or both, (where n is the number of packages in the vertical array and m is the number of packages in the horizontal array) and no external gating is required. The 3-state outputs controlled by a single enable input (OE) make bus connection and multiplexing easy. The 'F222 processes data in a parallel format at any desired clock rate from DC to 50MHz.

Reading or writing is done independently utilizing separate synchronous data clocks. Data may be written into the array on the High-to-Low transition of the load clock (LDCP) input. Data may be read out of the array on the low-to-high transition of the unload clock (UNCP). The FIFO is full when the number of words clocked in exceeds the number of words clocked out by 16. When the FIFO is full, LDCP signals have no effect. When the FIFO is empty, UNCP signals have no effect.

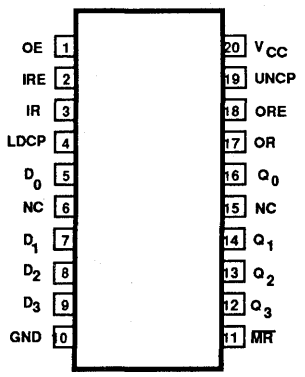
Status of the 'F222 is provided by two outputs. Input Ready (IR) monitors the status of the last word location and signifies when the FIFO is full. This output is high whenever the FIFO is available to accept new data and LDCP input is low. Output Ready (OR), is high when the first word location contains valid data and UNCP is high. Both IR and OR outputs are enabled by Input Ready Enable (IRE) and Output Ready Enable (ORE) inputs respectively. The first word location is defined as the location from which data is provided to the outputs.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
LDCP	Load clock input	1.0/1.0	20µA/0.6mA
D_0-D_3	Data inputs	1.0/1.0	20µA/0.6mA
OE	Output enable input (active High)	1.0/1.0	20µA/0.6mA
UNCP	Unload clock input	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Clear (active Low) input	1.0/1.0	20µA/0.6mA
IRE/ORE	Input Ready / Output Ready enable inputs	1.0/1.0	20µA/0.6mA
IR	Input Ready output	55/33	1.0mA/20mA
Q_0-Q_3	Data outputs	55/33	1.0mA/20mA
OR	Output Ready output	55/33	1.0mA/20mA

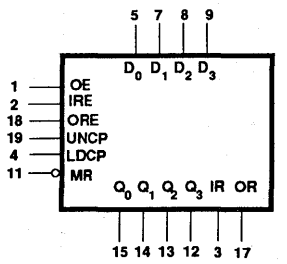
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



TOP VIEW

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

Signetics

FAST 74F224

16X4 Synchronous FIFO (3-State)

FAST Products

Preliminary Specification

FEATURES

- **Independent synchronous inputs and outputs**
- **Organized as 16 words of 4 bits**
- **DC to 50MHz data rate**
- **3-state outputs**
- **Cascadable in word-width and depth direction**

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F224	50MHz	90mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	74F224N
16-Pin Plastic SOL	74F224D

DESCRIPTION

This 64-bit active element First-In-First-Out (FIFO) is a monolithic Schottky-clamped transistor-transistor logic (STTL) array organized as 16 words of 4 bits each. A memory system using the 'F224 can be easily expanded in multiples of 15m+1 words or of 4n bits, or both, (where n is the number of packages in the vertical array and m is the number of packages in the horizontal array). However, some external gating is required (see Figure 1). For longer words using the 'F224, the IR signals of the first-rank packages and OR signals of the last-rank packages must be ANDed for proper synchronization. The 3-state outputs controlled by a single enable input (OE) make bus connection and multiplexing easy. The 'F224 processes data in a parallel format at any desired clock rate from DC to 50Mhz.

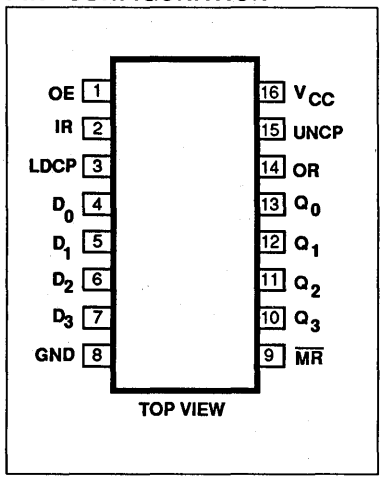
Reading or writing is done independently utilizing separate synchronous data clocks.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

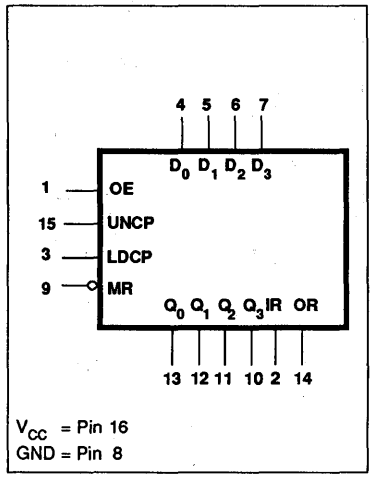
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
LDCP	Load clock input	1.0/1.0	20µA/0.6mA
D_0-D_3	Data inputs	1.0/1.0	20µA/0.6mA
OE	Output enable input (active High)	1.0/1.0	20µA/0.6mA
UNCP	Unload clock input	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset (active Low) input	1.0/1.0	20µA/0.6mA
IR	Input Ready output	55/33	1.0mA/20mA
Q_0-Q_3	Data outputs	55/33	1.0mA/20mA
OR	Output Ready output	55/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

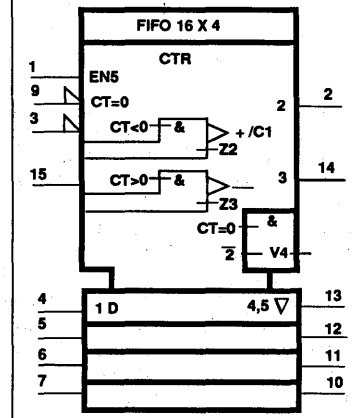
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



16X4 Synchronous FIFO (3-State) FAST 74F224

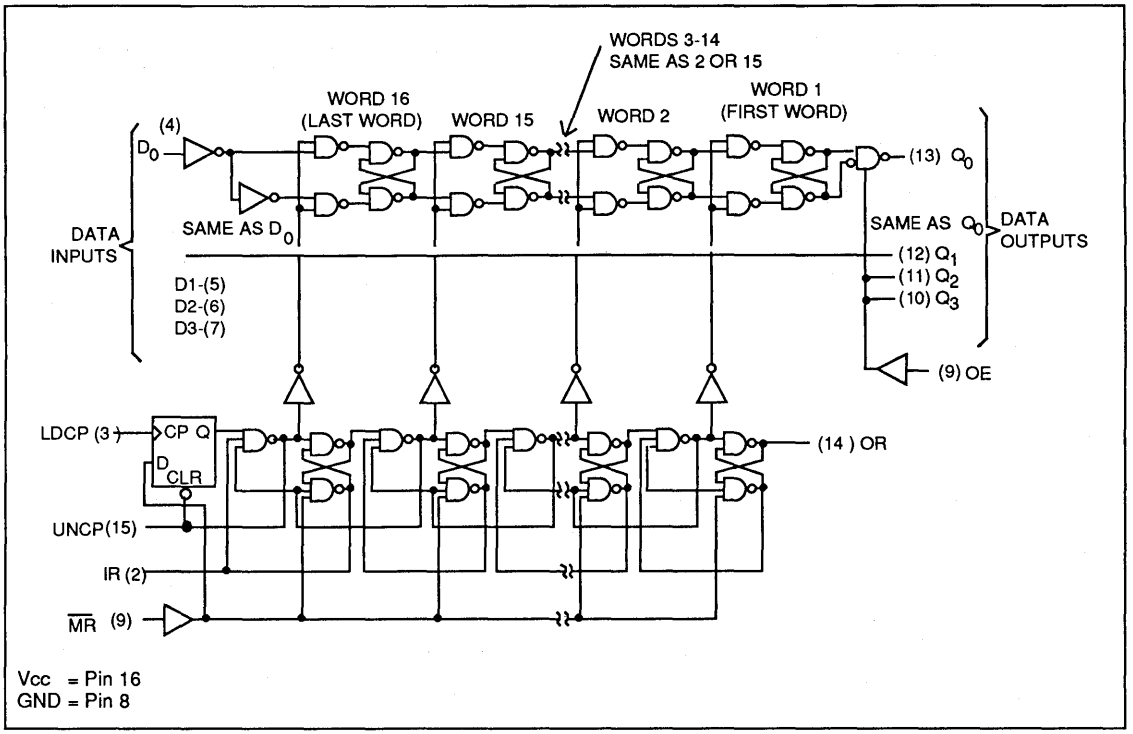
Data may be written into the array on the High-to-Low transition of the load clock (LDCP) input. Data may be read out of the array on the Low-to-High transition of the unload clock (UNCP). The FIFO is full when the number of words clocked in exceeds the number of words clocked out by 16. When the FIFO is full, LDCP signals have no effect. When the FIFO is empty, UNCP signals have no effect.

Status of the 'F224 is provided by two outputs. Input Ready (IR) monitors the status of the last word location and signifies when the FIFO is full. This output is high whenever the FIFO is available to accept new data and LDCP input is Low. Output Ready (OR), is High when the first word location contains valid data and UNCP is High. The first word location is defined as the location from which data is provided to the outputs.

The data outputs are noninverting with respect to the data inputs and are 3-stated when OE input is Low. OE does not affect the IR and OR outputs.

A low level at the Master Reset ($\overline{MR}$) input resets the internal stack control counters and also sets IR High and OR Low to indicate that old data remaining at the data outputs is invalid.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			55	80	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

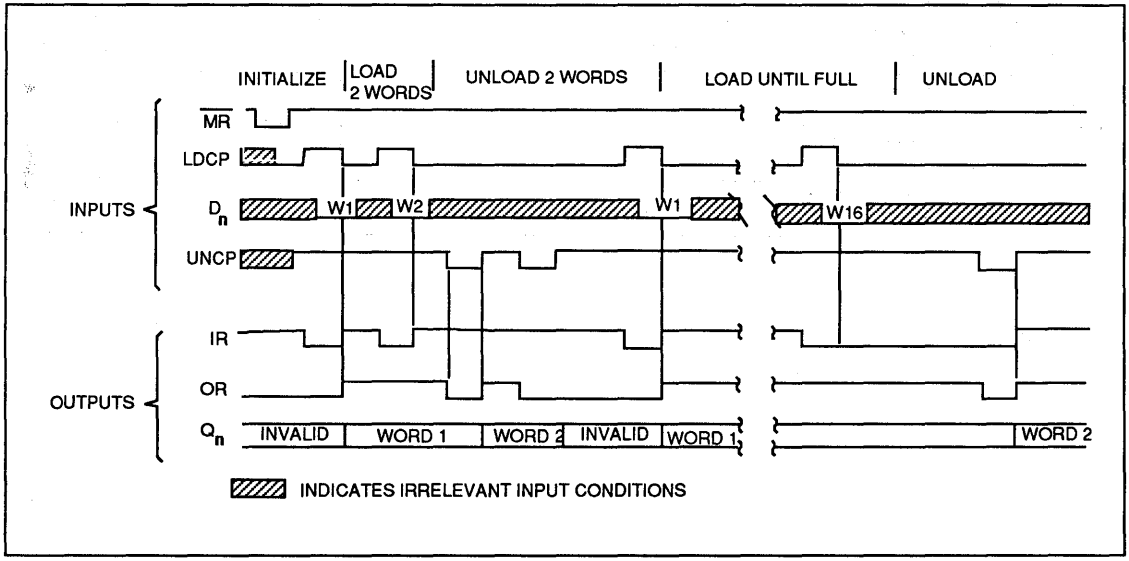
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency LDCP	Waveform 3						MHz
f_{MAX}	Maximum clock frequency UNCP	Waveform 3						MHz
t_{PHL}	Propagation delay LDCP(↑) to IR	Waveform 3						ns
t_{PLH}	Propagation dela LDCP(↓) to I	Waveform 4						ns
t_{PLH}	Propagation dela LDCP(↓) to OR	Waveform 2						ns
t_{PLH} t_{PHL}	Propagation delay LDCP(↓) to Q_n	Waveform 2						ns
t_{PLH}	Propagation delay UNCP(↑) to OR	Waveform 2						ns
t_{PHL}	Propagation delay UNCP(↓) to OR	Waveform 4						ns
t_{PLH} t_{PHL}	Propagation delay UNCP(↑) to Q_n	Waveform 4						ns
t_{PLH}	Propagation dela $\overline{MR}$(↓) to IR	Waveform 3						ns
t_{PHL}	Propagation delay $\overline{MR}$(↓) to OR	Waveform 3						ns
t_{PLH}	Propagation delay UNCP(↑)to IR	Waveform 3						ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 5, C_L=5.0pF						ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 5, C_L=5.0pF						ns

AC SET-UP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(L)$	Setup time, High or Low LDCP to UNCP	Waveform 1						ns
$t_s(H)$	Setup time, High or Low UNCP to LDCP	Waveform 1						ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_0- D_4 to LDCP	Waveform 1						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_0- D_4 to LDCP	Waveform 1						ns
$t_w(H)$ $t_w(L)$	LDCP Pulse width High or Low	Waveform 1						ns
$t_w(H)$ $t_w(L)$	UNCP Pulse width High or Low	Waveform 1						ns
$t_w(L)$	$\overline{MR}$ Pulse width Low	Waveform 1						ns

TYPICAL TIMING DIAGRAM



16X4 Synchronous FIFO (3-State) FAST 74F224

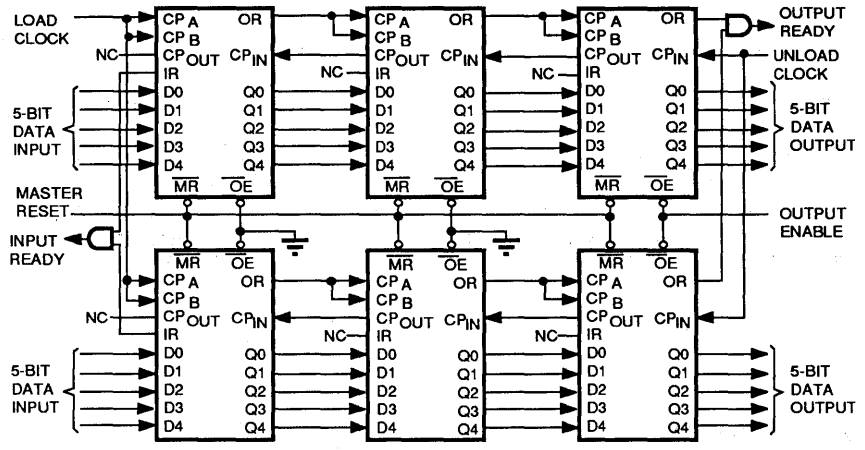
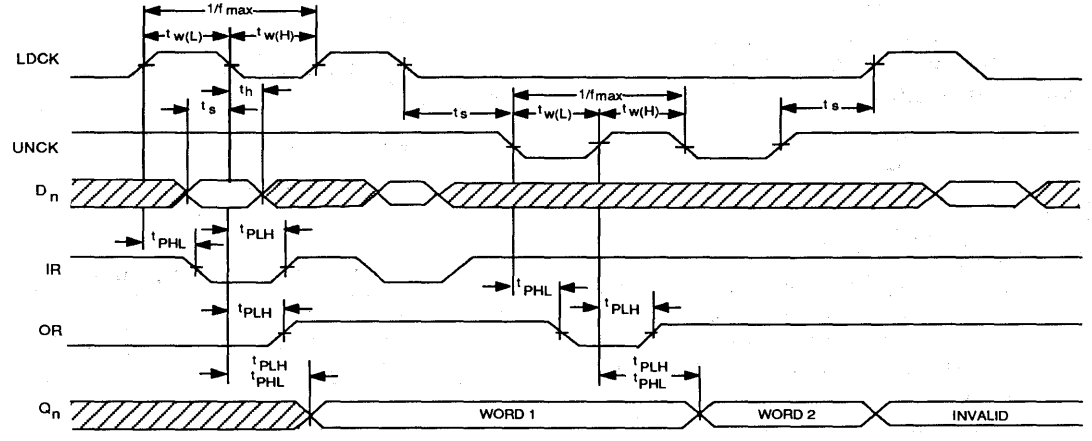
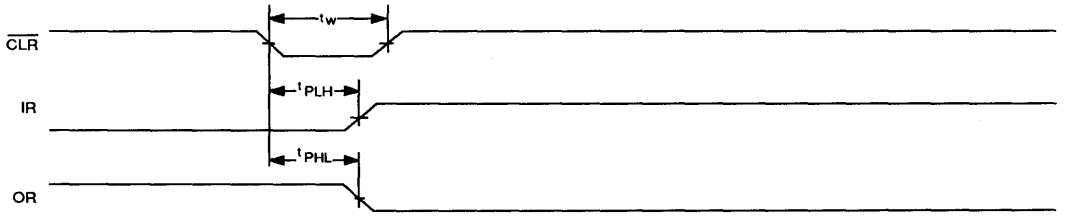


Figure 1. Expanding The 'F225 FIFO (48 words of 10 bits)

AC WAVEFORMS

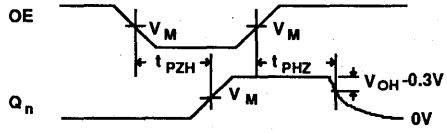


Waveform 1. Read and Write Cycle Timing.

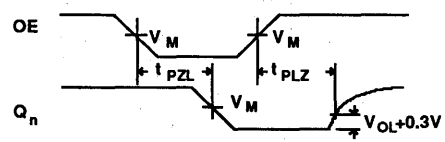


Waveform 2. $\overline{MR}$ Input Pulse- Width and IR and OR Delays

AC WAVEFORMS



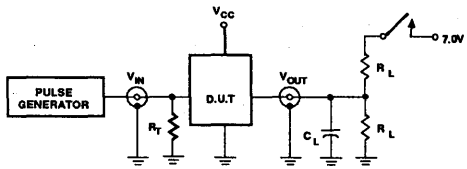
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

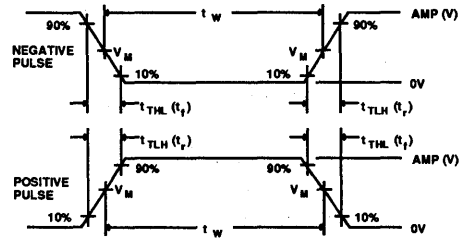
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F225

16X5 Asynchronous FIFO (3-State)

Preliminary Specification

FAST Products

FEATURES

- **Independent synchronous inputs and outputs**
- **Organized as 16 words of 5 bits**
- **DC to 50Mhz data rate**
- **3-state outputs**
- **Cascadable in word-width and depth direction**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F225	50MHz	95mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	74F225N
20-Pin Plastic SOL	74F225D

DESCRIPTION

This 80-bit active element First-In-First-Out (FIFO) is a monolithic Schottky-clamped transistor-transistor logic (STTL) array organized as 16-words of 5-bits each. A memory system using the 'F225 can be easily expanded in multiples of 16-words or of 5-bits as shown in Figure 2. The 3-state outputs controlled by a single enable input ($\overline{OE}$) make bus connection and multiplexing easy. The 'F225 processes data in a parallel format at any desired clock rate from DC to 50Mhz.

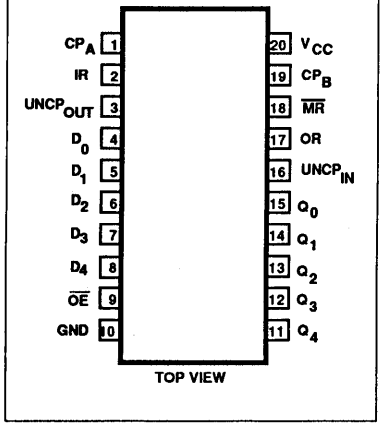
Reading or writing is done independently utilizing separate synchronous data clocks. Data may be written into the array on the low-to-high transition of either load clock (CP_A or CP_B) input. Data may be read out of the array on the low-to- high transition of the unload clock ($UNCP_{IN}$).When writing data into the FIFO, one of the load clock inputs must be held high while the other strobes

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

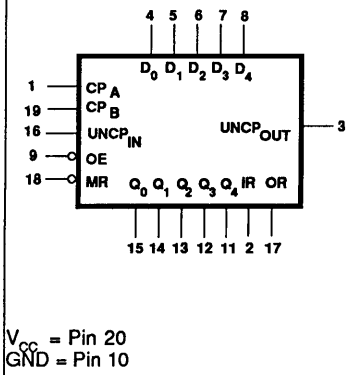
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOADVALUE HIGH/LOW
CP_A, CP_B	Load clock A and Load clock B inputs	1.0/1.0	20µA/0.6mA
D_0-D_4	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20µA/0.6mA
$UNCP_{IN}$	Unload clock input	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
IR	Input Ready output	55/33	1.0mA/20mA
$UNCP_{OUT}$	Unload clock output (active Low)	55/33	1.0mA/20mA
Q_0-Q_4	Data outputs	55/33	1.0mA/20mA
OR	Output Ready output	55/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

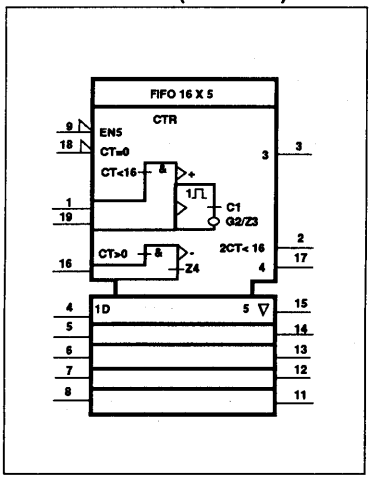
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



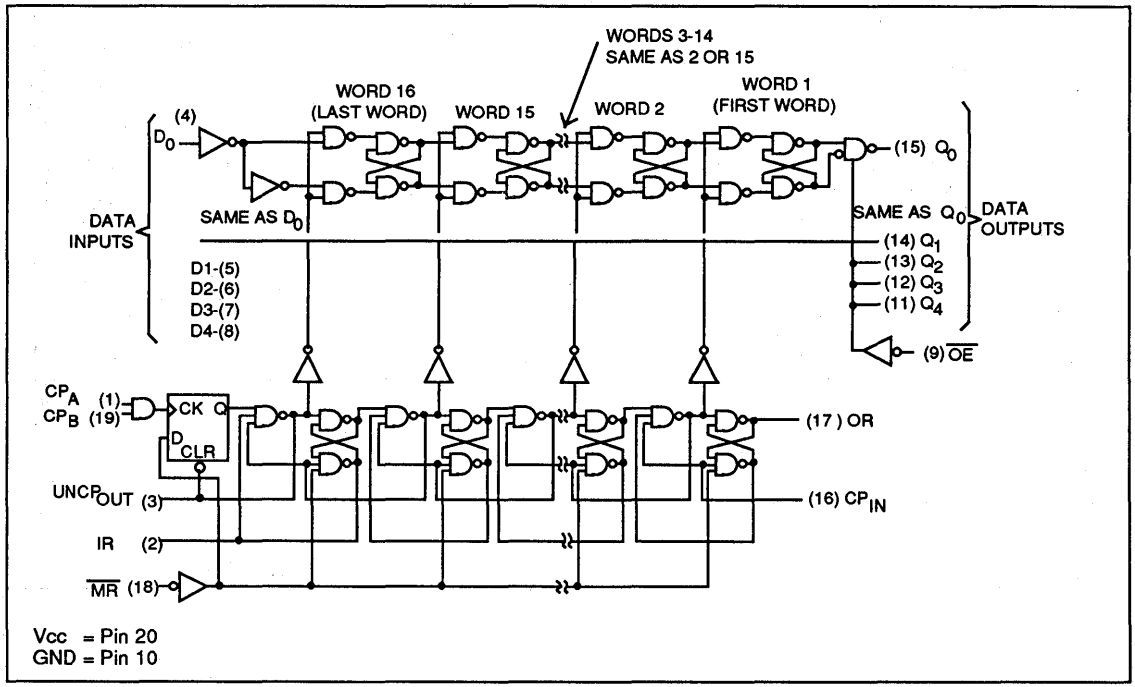
16X5 Asynchronous FIFO (3-State) FAST 74F225

data into the FIFO. This arrangement allows either load clock to function as an inhibit for the other. Status of the 'F225 is provided by three outputs. Input Ready (IR) monitors the status of the last word location and signifies when the FIFO is full. This output is high whenever the FIFO is available to accept new data. The unload clock output ($UNCP_{OUT}$) also monitors the last word location. This output generates a low-logic-level pulse (synchronized to the internal clock pulse) when the location is vacant. The third status output, Output Ready (OR), is high when the first word location contains valid data and unload clock input is high. When unload clock input goes low, OR will go low and remain low until new valid data is in the first word location. The first word location is defined as the location from which data is provided to the outputs.

The data outputs are noninverting with respect to the data inputs and are 3-stated when $\overline{OE}$ input is high. When $\overline{OE}$ is low, the data outputs are enabled to function as totem-pole outputs.

A high-to-low transition on the Master Reset ($\overline{MR}$) input invalidates all data stored in the FIFO by clearing the control logic and setting OR low. This high-to-low transition on the $\overline{MR}$ input does not effect the data outputs but since OR is driven low, it signifies invalid data on the outputs.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			55	80	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

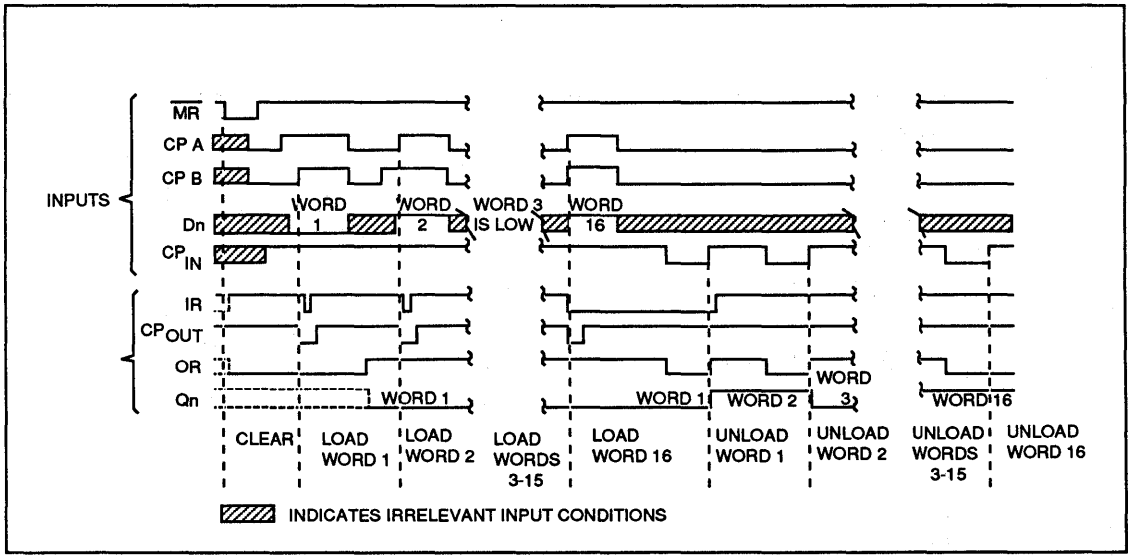
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency CP_A	Waveform 3	50			50		MHz
f_{MAX}	Maximum clock frequency CP_B	Waveform 3	50			50		MHz
f_{MAX}	Maximum clock frequency CP_{IN}	Waveform 2	50			50		MHz
t_{PLH} t_{PHL}	Propagation delay CP_{IN} to Q_n	Waveform 2			15 25		20 20	ns
t_{PLH}	Propagation delay CP_A or CP_B to OR	Waveform 4			100		150	ns
t_{PLH} t_{PHL}	Propagation delay CP_{IN} to OR	Waveform 2			25 15		30 20	ns
t_{PHL}	Propagation delay $\overline{MR}$ to OR	Waveform 3			15		30	ns
t_{PHL}	Propagation delay CP_A or CP_B to CP_{OUT}	Waveform 4			20		30	ns
t_{PHL}	Propagation delay CP_A or CP_B to IR	Waveform 3			20		30	ns
t_{PLH}	Propagation delay CP_{IN} to IR	Waveform 2			100		150	ns
t_{PHL}	Propagation delay $\overline{MR}$ to IR	Waveform 3	0		10	0	20	ns
t_{PLH}	Propagation delay Q_n to OR	Waveform 4			15	0	20	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 5			10 10		20 20	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 6, C_L=5.0pF			10 15		20 25	ns

AC SET-UP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_0- D_4 to CP_A or CP_B	Waveform 1	1.0 1.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_0- D_4 to CP_A or CP_B	Waveform 1	15.0 15.0			15.0 15.0		ns
$t_h(H)$ $t_h(L)$	Setup time, High or Low $\overline{MR}$ to CP_A or CP_B	Waveform 1	5.0 5.0			5.0 5.0		ns
$t_w(H)$ $t_w(L)$	CP_A or CP_B Pulse width High or Low	Waveform 1	10.0 10.0			10.0 10.0		ns
$t_w(L)$	$UNCP_{OUT}$ Pulse width Low	Waveform 4	4.0			4.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width Low	Waveform 1	10.0			10.0		ns

TYPICAL TIMING DIAGRAM



16X5 Asynchronous FIFO (3-State) FAST 74F225

APPLICATION

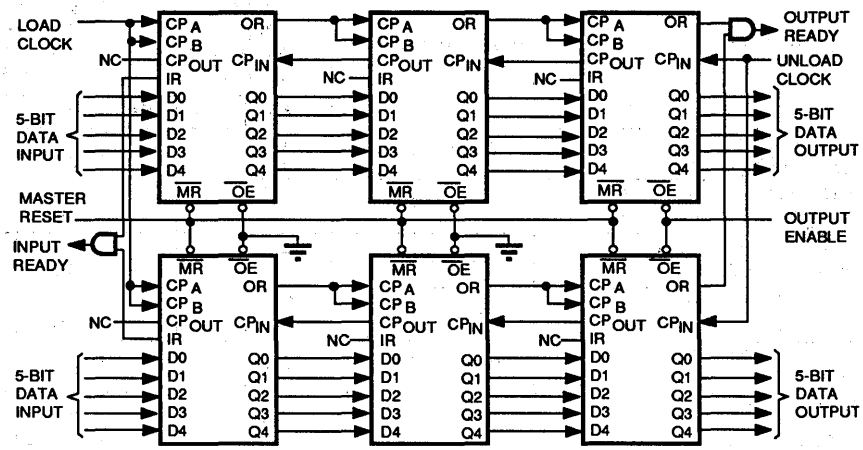
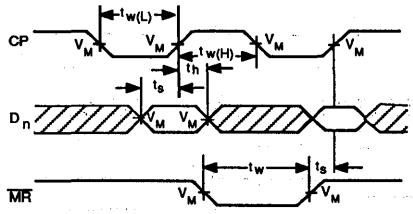
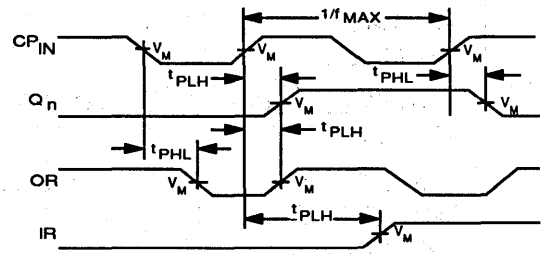


Figure 1. Expanding The 'F225 FIFO (48 words of 10 bits)

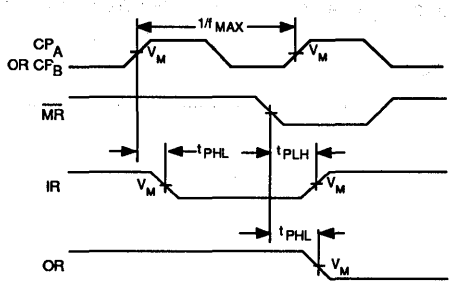
AC WAVEFORMS



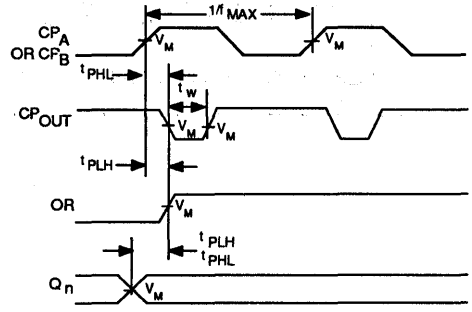
Waveform 1. $\overline{MR}$ and Clock Pulse Widths, Data Set-up and Hold Times and $\overline{MR}$ to Clock Set-up Time



Waveform 2. CP_{IN} to Output Delays



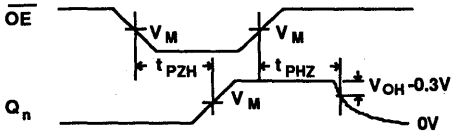
Waveform 3. CP_A or CP_B to IR Delay and $\overline{MR}$ to IR and OR Delay



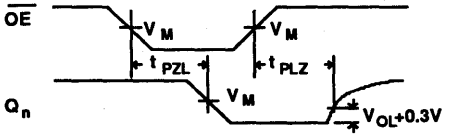
Waveform 4. CP_A or CP_B to CP_{OUT} and OR Delay, CP_{OUT} Pulse Width and Q_n to OR Delay

NOTE: For all waveforms, $V_M = 1.5V$.

AC WAVEFORMS



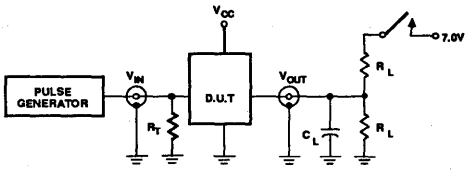
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

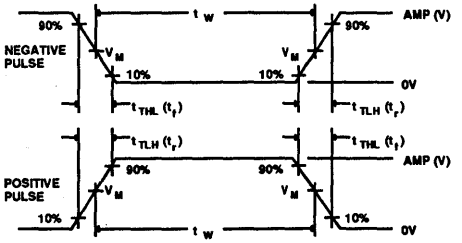
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F240, 74F241
Buffers

FAST Products

74F240 Octal Inverter Buffer (3-State)
74F241 Octal Buffer (3-State)
Product Specification

FEATURES
- **Octal bus interface**
- **3-State buffer outputs sink 64mA**
- **15mA source current**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F240	4.3ns	37mA
74F241	5.0ns	53mA

DESCRIPTION

The 74F240 and 74F241 are octal buffers that are ideal for driving bus lines of buffer memory address registers. The outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The devices feature two Output Enables each controlling four of the 3-state outputs.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F240N, N74F241N
20-Pin Plastic SOL	N74F240D, N74F241D

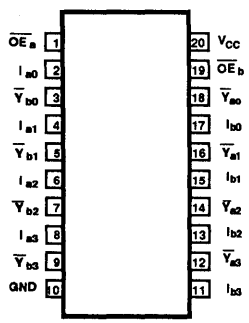
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{an}, I_{bn}	Data inputs ('F240)	1.0/1.67	20µA/1.0mA
I_{an}, I_{bn}	Data inputs ('F241)	1.0/2.67	20µA/1.6mA
$\overline{OE}_a$, $\overline{OE}_b$	Output enable input (active Low)	1.0/1.67	20µA/1.0mA
OE_b	Output enable input (active High, 'F241)	1.0/1.0	20µA/1.0mA
Y_{an}, Y_{bn}	Data outputs ('F241)	750/106.7	15mA/64mA
$\overline{Y}_{an}$, $\overline{Y}_{bn}$	Data outputs ('F240)	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

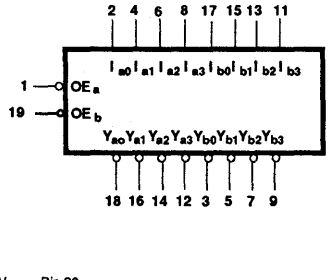
PIN CONFIGURATION

74F240



LOGIC SYMBOL

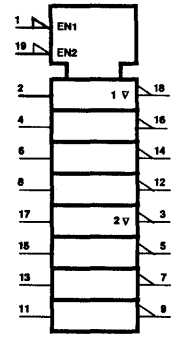
74F240



V_{CC} = Pin 20
GND = Pin 10

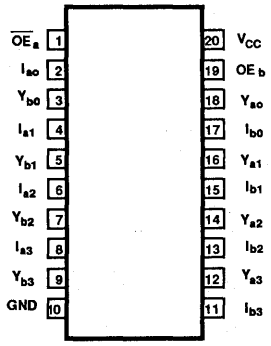
LOGIC SYMBOL(IEEE/IEC)

74F240



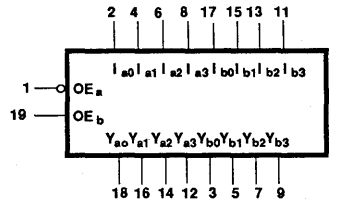
PIN CONFIGURATION

74F241



LOGIC SYMBOL

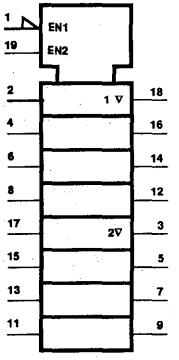
74F241



V_{CC} = Pin 20
GND = Pin 10

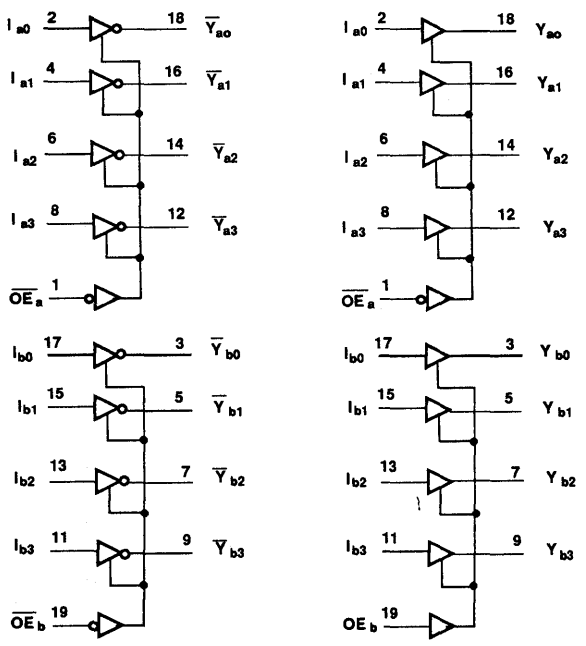
LOGIC SYMBOL(IEEE/IEC)

74F241



LOGIC DIAGRAM,

74F240 | 74F241



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE, 74F240

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_a$	$\overline{Y}_b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

FUNCTION TABLE, 74F241

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_a	Y_b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3mA	±10% V_{CC}	2.4			V
						±5% V_{CC}	2.7	3.4		V
					I_{OH} = -15mA	±10% V_{CC}	2.0			V
						±5% V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10% V_{CC}		0.38	0.55	V
					I_{OL} = 64mA	±5% V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7 V					20	µA
I_{IL}	Low-level input current	'F240 all inputs		V_{CC} = MAX, V_I = 0.5 V					-1.0	mA
		'F241 $\overline{OE}_a$, OE_b							-1.0	mA
		'F241 I_{an}, I_{bn}							-1.6	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	74F240	I_{CCH}	V_{CC} = MAX				12	18	mA
			I_{CCL}					50	70	mA
			I_{CCZ}					35	45	mA
		74F241	I_{CCH}	V_{CC} = MAX				40	60	mA
			I_{CCL}					60	90	mA
			I_{CCZ}					65	90	mA

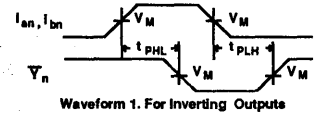
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

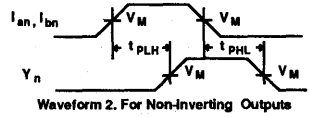
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to $\overline{Y}_n$	74F240	Waveform 1	3.0 2.0	4.5 3.0	6.5 4.5	3.0 2.0	7.5 5.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	3.0 4.5	5.0 6.5	7.5 8.5	3.0 4.0	9.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 3 Waveform 4	3.0 3.0	5.5 5.0	7.0 7.0	3.0 3.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to Y_n	74F241	Waveform 2	2.5 2.5	4.0 4.0	5.2 5.2	2.5 2.5	6.2 6.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.0 5.0	5.7 7.0	2.0 2.0	6.7 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 6.0	2.0 2.0	7.0 7.0	ns

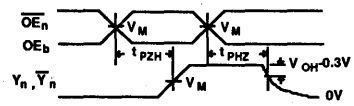
AC WAVEFORMS



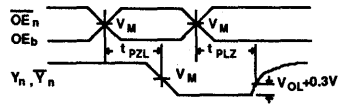
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



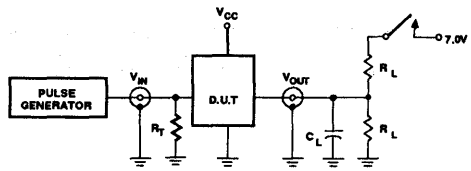
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

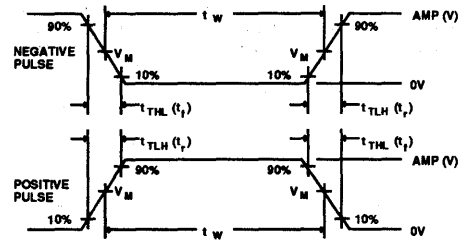
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F242, 74F243
Transceivers

FAST Products

74F242 Quad Transceiver, Inverting (3-State)
74F243 Quad Transceiver (3-State)

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F242	4.3ns	31.2mA
74F243	4.0ns	66mA

ORDERING INFORMATION

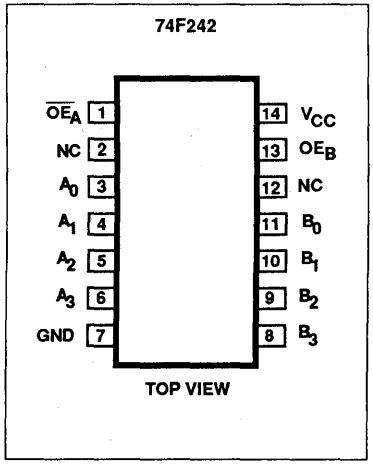
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F242N, N74F243N
14-Pin Plastic SO	N74F242D, N74F243D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

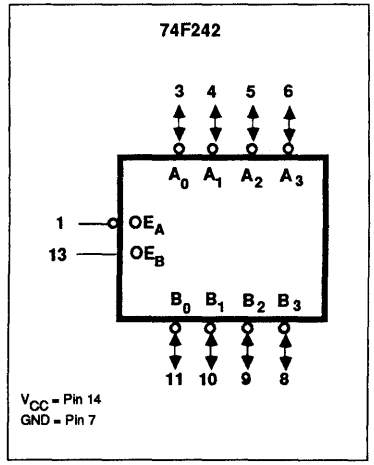
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_n, B_n	Data inputs ('F242)	3.5/1.67	70μA/1.0mA
A_n, B_n	Data inputs ('F243)	3.5/2.67	70μA/1.6mA
$\overline{OE}_A$	Output enable input (active Low)	1.0/1.67	20μA/1.0mA
OE_B	Output enable input	1.0/1.67	20μA/1.0mA
A_n, B_n	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

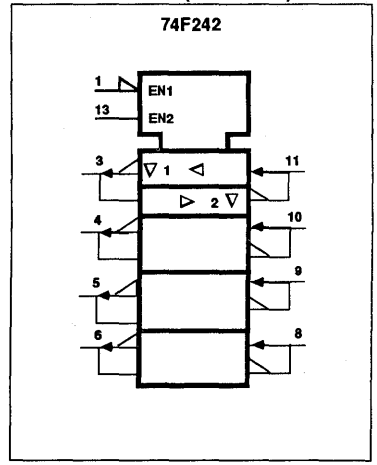
PIN CONFIGURATION



LOGIC SYMBOL

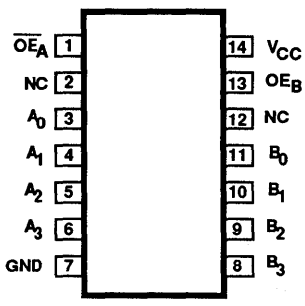


LOGIC SYMBOL(IEEE/IEC)



PIN CONFIGURATION

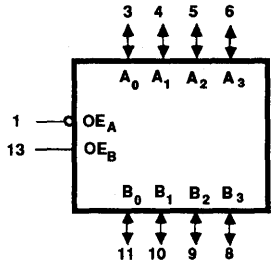
74F243



TOP VIEW

LOGIC SYMBOL

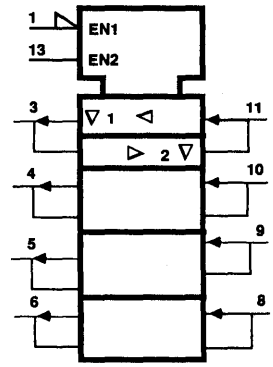
74F243



V_{CC} = Pin 14
GND = Pin 7

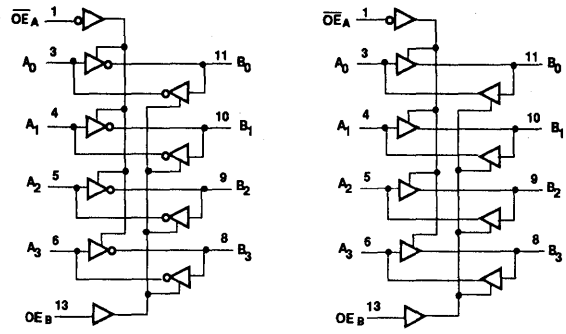
LOGIC SYMBOL(IEEE/IEC)

74F243



LOGIC DIAGRAM

74F242 74F243



V_{CC} = Pin 14
GND = Pin 7

FUNCTION TABLE, 74F242

INPUTS		OUTPUTS	
$\overline{OE}_A$	OE_B	A_n	B_n
L	L	INPUT	$B=\overline{A}$
H	L	Z	Z
L	H	a	a
H	H	$A=\overline{B}$	INPUT

FUNCTION TABLE, 74F243

INPUTS		OUTPUTS	
$\overline{OE}_A$	OE_B	A_n	B_n
L	L	INPUT	B=A
H	L	Z	Z
L	H	a	a
H	H	A=B	INPUT

H = High voltage level
L = Low voltage level
Z = High impedance "off" state
a = This condition is not allowed due to excessive currents

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=-15mA	±10%V_{CC}	2.0	3.2		V
					±5%V_{CC}	2.0	3.1		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	A_0-A_3, B_0-B_3	V_{CC} =MAX, V_I = 5.5V					100	µA
		$\overline{OE}_A$, OE_B	V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	$\overline{OE}_A$, OE_B only	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-1	mA
I_{IH}+I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O= 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current, Low-level voltage applied	'F242	V_{CC} = MAX, V_O= 0.5V					-1.0	mA
		'F243						-1.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F242	I_{CCH}	V_{CC} = MAX			22	35	mA
			I_{CCL}				40	55	mA
			I_{CCZ}				32	45	mA
		'F243	I_{CCH}	V_{CC} = MAX			64	80	mA
			I_{CCL}				64	90	mA
			I_{CCZ}				71	90	mA

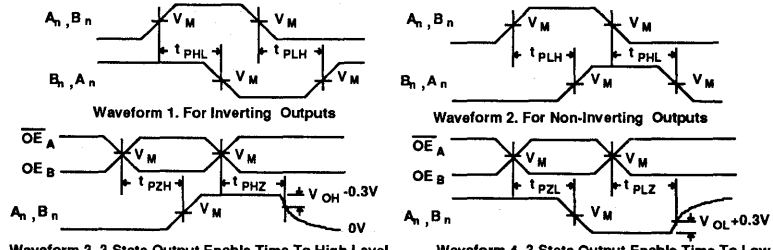
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

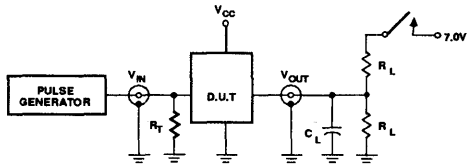
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to B_n, A_n	74F242	Waveform 1	3.0 2.0	4.5 3.0	6.5 4.5	3.0 2.0	7.5 4.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	3.5 3.5	6.0 6.5	7.5 9.0	3.5 3.5	8.5 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 3 Waveform 4	4.0 3.5	7.0 6.0	9.0 9.5	4.0 3.5	9.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to B_n, A_n	74F243	Waveform 2	2.5 2.5	4.0 4.0	5.2 5.2	2.0 2.0	6.2 6.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.5 5.0	5.7 7.5	2.0 2.0	6.7 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.0 4.5	6.0 6.0	2.0 2.0	7.0 7.0	ns

AC WAVEFORMS



NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

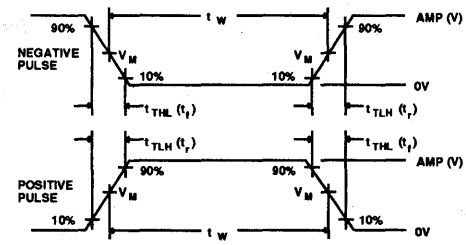
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F244
Buffer

FAST Products

74F244 Octal Buffer (3-State)
Product Specification

FEATURES
- **Octal bus interface**
- **3-State Output buffer output sink 64mA**
- **15mA source current**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F244	4.0ns	53mA

DESCRIPTION

The 74F244 is an octal buffer that is ideal for driving bus lines of buffer memory address registers. The outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}_a$ and $\overline{OE}_b$, each controlling four of the 3-state outputs.

ORDERING INFORMATION

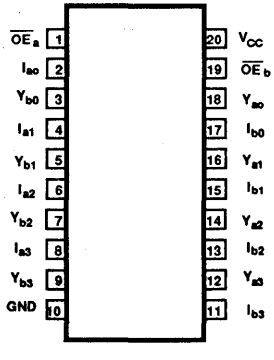
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F244N
20-Pin Plastic SOL	N74F244D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

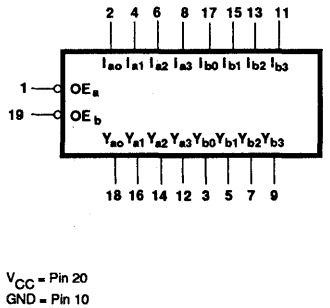
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{an}, I_{bn}	Data inputs	1.0/2.67	20µA/1.6mA
$\overline{OE}_a$ $\overline{OE}_b$	Output enable inputs (active Low)	1.0/1.67	20µA/1.0mA
Y_{an}, Y_{bn}	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

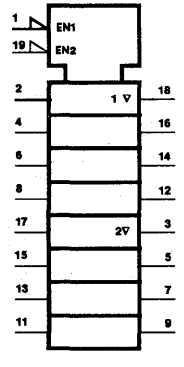
PIN CONFIGURATION



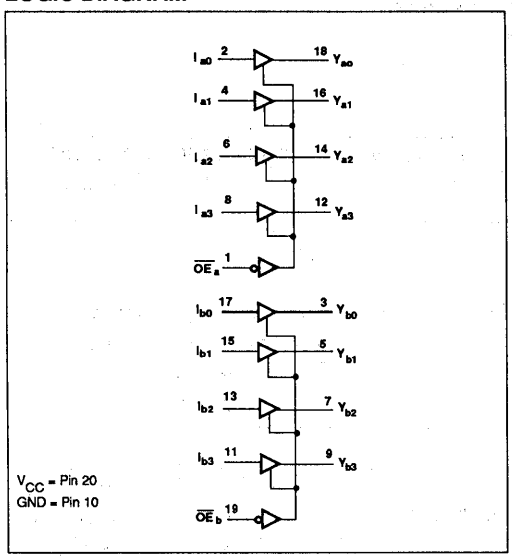
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH}=-15mA	±10%V_{CC}	2.0			V
				±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}			0.55	V
				±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	$\overline{OE}_a$, $\overline{OE}_b$	V_{CC} = MAX, V_I = 0.5V				-1.0	mA
		I_{an}, I_{bn}					-1.6	mA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			40	60	mA
		I_{CCL}				60	90	mA
		I_{CCZ}				60	90	mA

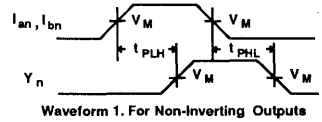
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

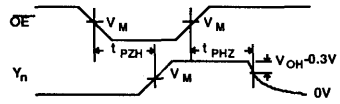
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to Y_n	Waveform 1	2.5 2.5	4.0 4.0	5.2 5.2	2.0 2.0	6.2 6.5	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	2.0 2.0	4.3 5.0	5.7 7.0	2.0 2.0	6.7 8.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 2 Waveform 3	1.5 1.5	2.5 2.5	5.5 5.5	1.0 1.0	6.0 5.5	ns ns

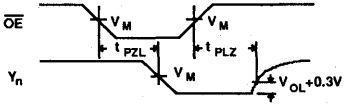
AC WAVEFORMS



Waveform 1. For Non-Inverting Outputs



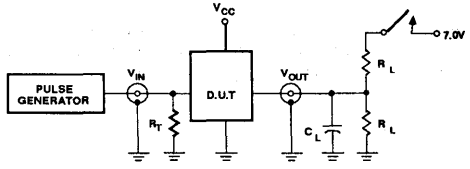
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

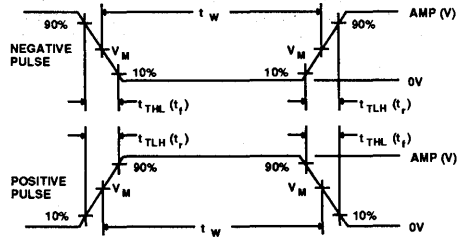
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F245
Transceiver

FAST Products

FEATURES

- **Octal bidirectional bus interface**
- **3-state buffer outputs sink 64mA**
- **15 mA source current**
- **Outputs are placed in high impedance state during power-off conditions**

Octal Transceiver (3-State)
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F245	4.0ns	70mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F245N
20-Pin Plastic SOL	N74F245D

DESCRIPTION

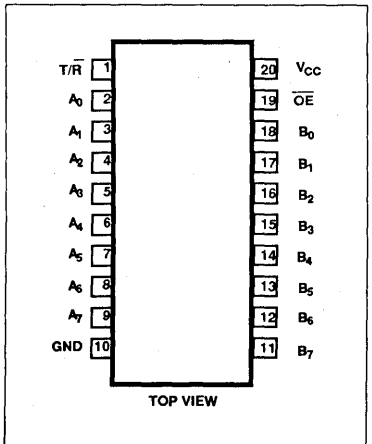
The 74F245 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both transmit and receive directions. The B port outputs are capable of sinking 64mA and sourcing 15mA, producing very good capacitive drive characteristics.The device features an Output Enable ($\overline{OE}$) input for easy cascading and Transmit/Receive($T/\overline{R}$) input for direction control. The 3-state outputs, B_0-B_7, have been designed to prevent output bus loading if the power is removed from the device.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

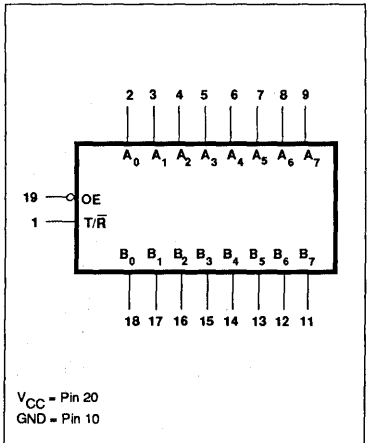
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7, B_0- B_7	Data inputs	3.5/1.0	70μA/0.6mA
$\overline{OE}$	Output enable input (active Low)	1.0/2.0	20μA/1.2mA
$T/\overline{R}$	Transmit/Receive input	1.0/2.0	20μA/1.2mA
A_0- A_7	A port outputs	150/40	3.0mA/24mA
B_0- B_7	B Port outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

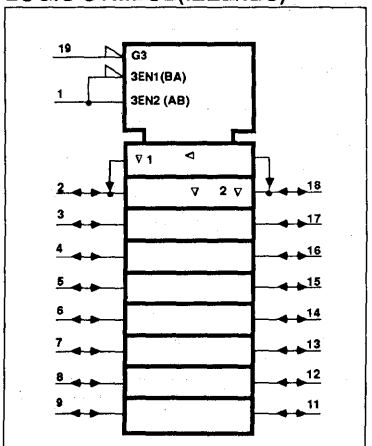
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

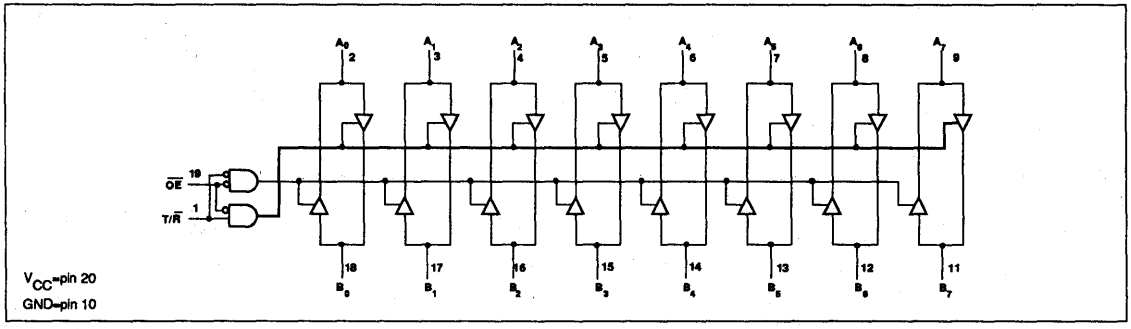


FUNCTION TABLE

INTPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B data to Bus A
L	H	Bus A data to Bus B
H	X	Z

H=High voltage level
L=Low voltage level
X=Don't care
Z=High impedance "off " state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0-B_7			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		B_0-B_7		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=20mA	±10%V_{CC}		0.30	0.50	V
				I_{OL}=24mA	±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$	V_{CC} = 5.5V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 0.5V					-1.2	mA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = MAX, V_O= 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-600	µA
I_{OS}	Short-circuit output current[3]	A_0-A_7	V_{CC} = MAX			-60		-150	mA
		B_0-B_7				-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				60	87	mA
		I_{CCL}					70	100	mA
		I_{CCZ}					75	110	mA

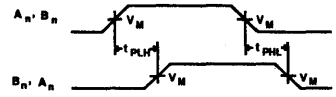
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

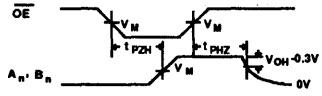
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	Waveform 1	2.5 2.5	3.5 4.0	6.0 6.0	2.5 2.5	7.0 7.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	2.0 3.5	4.5 5.5	7.0 8.0	2.0 3.5	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 2 Waveform 3	2.5 1.0	5.0 3.5	6.5 6.0	2.0 1.0	7.5 7.0	ns

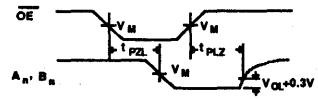
AC WAVEFORMS



Waveform 1. Propagation Delay For Non-Inverting Output



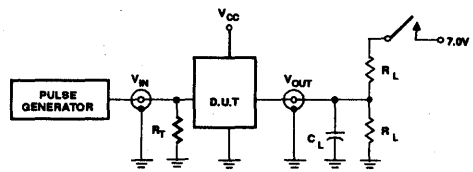
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

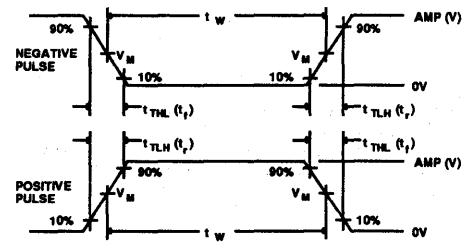
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F251, 74F251A
Multiplexers

FAST Products

74F251 8-input Multiplexer (3-State)
74F251A 8-input Multiplexer (3-State)
Product Specification

FEATURES
- **High speed 8-to-1 multiplexing**
- **On chip decoding**
- **Multifunction capability**
- **Inverting and Non-Inverting outputs**
- **Both outputs are 3-state for further multiplexer expansion**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F251	5.5ns	15mA
74F251A	4.5ns	19mA

DESCRIPTION

The 74F251 and 74F251A are logic implementation of a single 8-position switch with the switch position controlled by the state of three Select (S_0,S_1,S_2) inputs. True(Y) and complementary ($\overline{Y}$) outputs are both provided. The output Enable ($\overline{OE}$) is active Low. When $\overline{OE}$ is High, both outputs are in high impedance state, allowing multiple output connections to a common bus without driving nor loading the bus significantly. All but one device must be in high impedance state to avoid high currents that would exceed the maximum ratings when the outputs of the 3-state devices are tied together. When the output of more than one device is tied together the user must ensure that there is no overlap in the active Low portion of the output enable voltages.

74F251A is the faster version of 74F251.

ORDERING INFORMATION

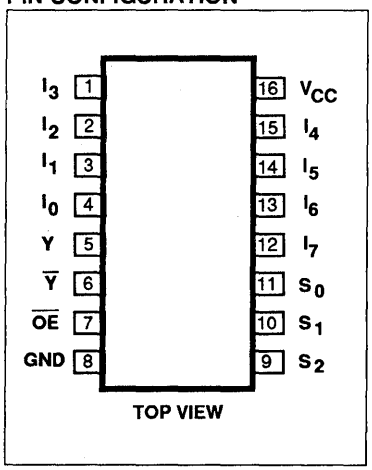
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F251N, N74F251AN
16-Pin Plastic SO	N74F251D, N74F251AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0- I_7	Data inputs	1.0/1.0	20µA/0.6mA
S_0- S_2	Select inputs	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
Y, $\overline{Y}$	Data outputs	150/40	3mA/24mA

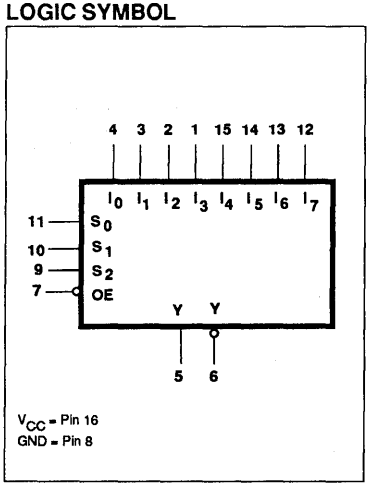
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



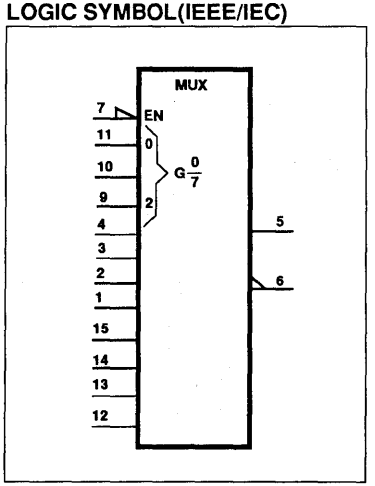
TOP VIEW

LOGIC SYMBOL

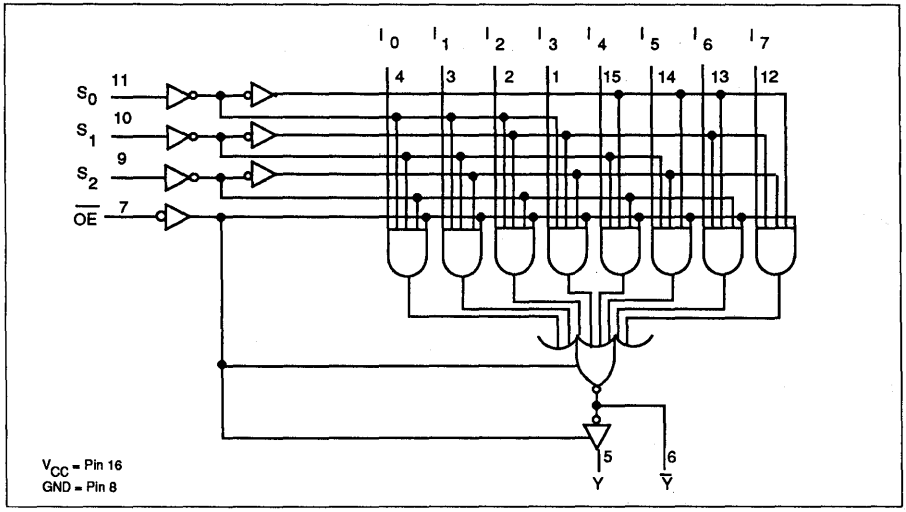


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
S_2	S_1	S_0	$\overline{OE}$	Y	$\overline{Y}$
X	X	X	H	Z	Z
L	L	L	L	I_0	$\overline{I}_0$
L	L	H	L	I_1	$\overline{I}_1$
L	H	L	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
H	L	L	L	I_4	$\overline{I}_4$
H	L	H	L	I_5	$\overline{I}_5$
H	H	L	L	I_6	$\overline{I}_6$
H	H	H	L	I_7	$\overline{I}_7$

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
				V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
				V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]			V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	74F251	V_{CC} = MAX			14	22	mA
		I_{CCL}					14	22	mA
		I_{CCZ}					16	24	mA
		I_{CCH}	74F251A	V_{CC} = MAX			20	27	mA
		I_{CCL}					17	24	mA
		I_{CCZ}					21	29	mA

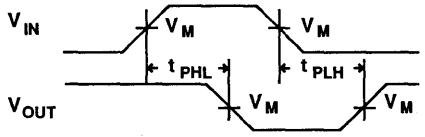
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

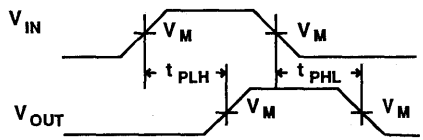
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	74F251	Waveform 2	3.0 3.0	4.0 4.5	6.0 6.5	2.5 3.0	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$		Waveform 1	2.5 1.0	4.0 2.0	6.0 4.0	2.0 1.0	7.0 5.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y		Waveform 1, 2	4.0 4.0	7.0 7.0	9.5 9.0	3.5 4.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$		Waveform 1, 2	3.5 1.5	6.0 5.0	9.0 7.5	3.5 1.5	10.0 8.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Y		Waveform 3 Waveform 4	4.0 4.0	6.5 5.5	10.0 8.0	4.0 3.5	11.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Y		Waveform 3 Waveform 4	4.0 4.0	5.5 5.5	8.0 8.0	3.5 3.5	9.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to $\overline{Y}$		Waveform 3 Waveform 4	2.5 3.0	4.0 4.0	6.5 6.5	2.0 2.5	7.5 7.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to $\overline{Y}$		Waveform 3 Waveform 4	2.5 2.0	4.0 4.0	6.0 6.5	2.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y	74F251A	Waveform 2	3.0 3.0	5.0 5.0	7.0 7.0	2.5 3.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$		Waveform 1	2.5 1.0	4.5 2.5	7.0 5.0	2.0 1.0	7.5 5.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y		Waveform 1, 2	4.5 4.0	6.5 5.5	10.0 9.0	4.0 3.5	11.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$		Waveform 1, 2	3.5 2.5	6.0 4.5	9.0 7.0	3.5 2.5	9.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Y		Waveform 3 Waveform 4	3.5 3.5	5.5 5.0	7.5 7.5	3.0 3.0	8.5 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Y		Waveform 3 Waveform 4	2.5 1.0	4.0 4.0	6.5 6.0	2.0 1.0	7.0 6.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to $\overline{Y}$		Waveform 3 Waveform 4	2.5 2.5	4.0 4.0	6.5 6.5	2.0 2.5	7.0 7.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to $\overline{Y}$		Waveform 3 Waveform 4	3.5 1.0	5.0 2.0	7.5 4.5	3.0 1.0	8.0 4.5	ns

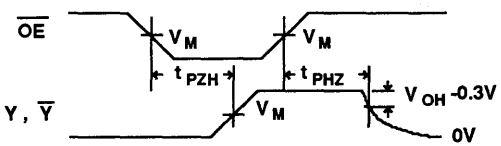
AC WAVEFORMS



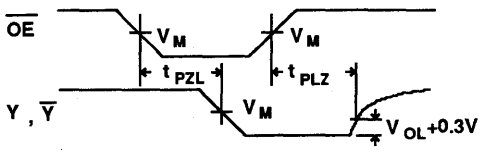
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs

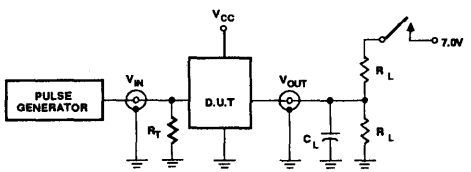


Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

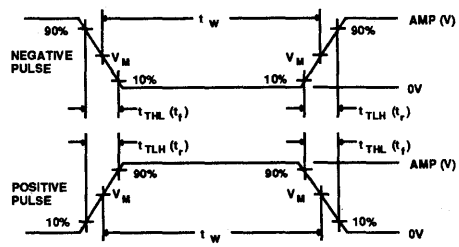
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F253
Multiplexer

FAST Products

Dual 4-Input Multiplexer (3-State)

Product Specification

FEATURES
- **3-state outputs for bus interface and multiplex expansion**
- **Common select inputs**
- **Separate Output Enable inputs**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F253	7.0ns	12mA

DESCRIPTION

The 74F253 has two identical 4-input multiplexers with 3-state outputs which select two bits from four sources selected by common Select inputs (S_0,S_1). When the individual Output Enable ($\overline{OE}_a$,$\overline{OE}_b$) inputs of the 4-input multiplexers are High, the outputs are forced to a high impedance (Hi-Z) state.

The 'F253 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two common Select inputs.

To avoid exceeding the maximum current ratings when the outputs of the 3-state devices are tied together, all but one device must be in the high-impedance state. Therefore, only one Output Enable must be active at a time.

ORDERING INFORMATION

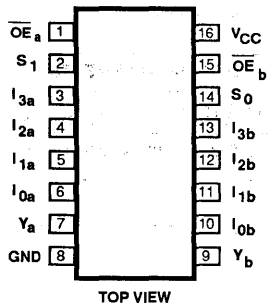
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F253N
16-Pin Plastic SO	N74F253D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0a}- I_{3a}	Port A data inputs	1.0/1.0	20µA/0.6mA
I_{0b}- I_{3b}	Port B data inputs	1.0/1.0	20µA/0.6mA
S_0, S_1	Common Select inputs	1.0/1.0	20µA/0.6mA
$\overline{OE}_a$	Port A Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}_b$	Port B Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
Y_a, Y_b	3-state outputs	150/40	3mA/24mA

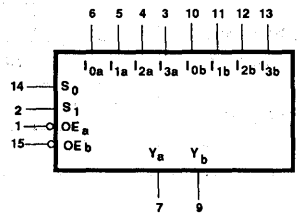
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



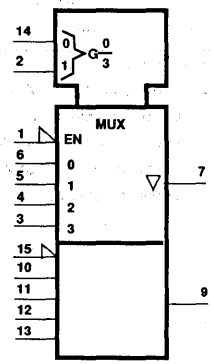
TOP VIEW

LOGIC SYMBOL

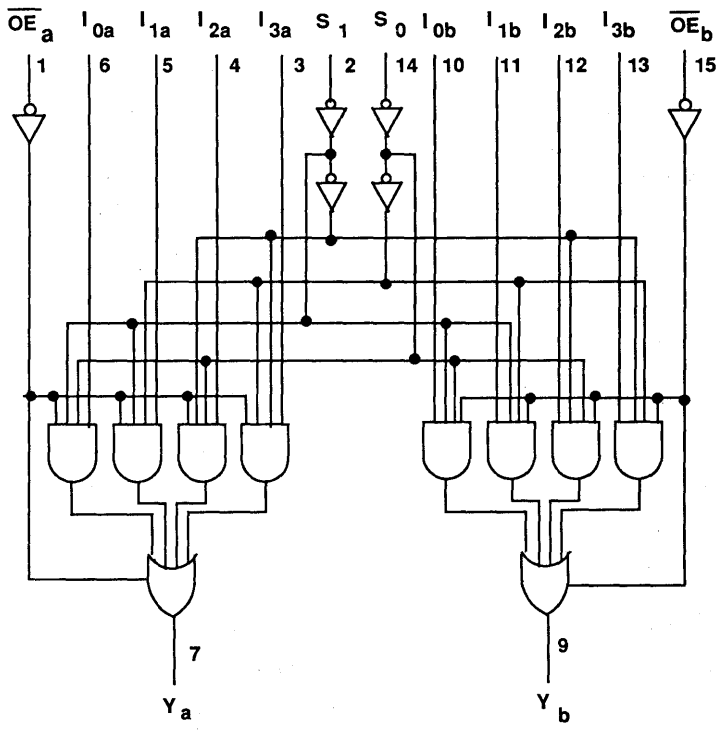


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{OE}_n$=GND, S_n=I_n=4.5V		10	16	mA
		I_{CCL}		$\overline{OE}_n$=S_n=I_n=GND		12	23	mA
		I_{CCZ}		$\overline{OE}_n$=4.5V, S_n=I_n=GND		14	23	mA

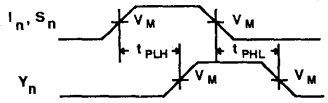
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

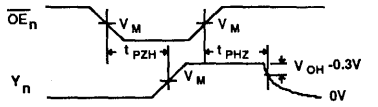
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	Waveform 1	3.0 3.0	4.5 5.0	7.0 7.0	3.0 3.0	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y_n	Waveform 1	4.5 5.0	7.5 8.5	10.5 11.0	4.5 4.5	11.0 12.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	3.0 3.0	6.5 6.5	8.0 8.0	3.0 3.0	9.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 2 Waveform 3	2.5 2.0	3.5 3.0	5.0 5.0	2.0 1.5	6.0 6.0	ns

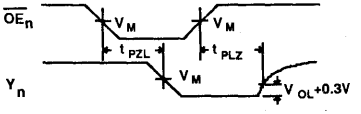
AC WAVEFORMS



Waveform 1. Propagation Delay, Data and Select to Output



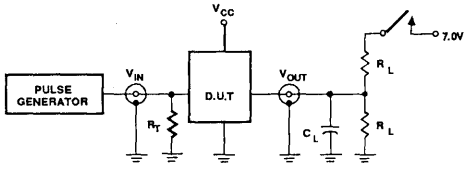
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

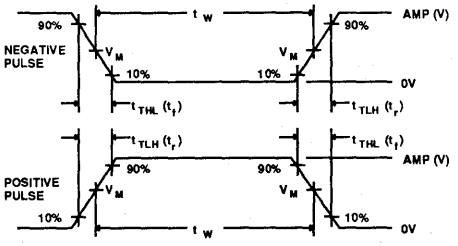
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F256
Latch

Dual Addressable Latch

FAST Products

FEATURES

- **Combines dual demultiplexer and 8-bit latch**
- **Serial-to-parallel capability**
- **Output from each storage bit available**
- **Random (addressable) data entry**
- **Easily expandable**
- **Common reset input**
- **Useful as dual 1-of-4 active-High decoder**

DESCRIPTION

The 74F256 dual addressable latch has four distinct modes of operation which are selectable by controlling the Master Reset ($\overline{MR}$) and Enable ($\overline{E}$) inputs (see Function Table). In the addressable latch mode, data at the Data inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states. and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held High (inactive) while the address lines are changing. In the dual 1-of-4 decoding or demultiplexing mode ($\overline{MR}$=$\overline{E}$=Low), addressed outputs will follow the level of the Data inputs, with all other outputs Low. In the Master Reset mode, all outputs are Low and unaffected by the Address and Data inputs.

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F256	7.0ns	28mA

ORDERING INFORMATION

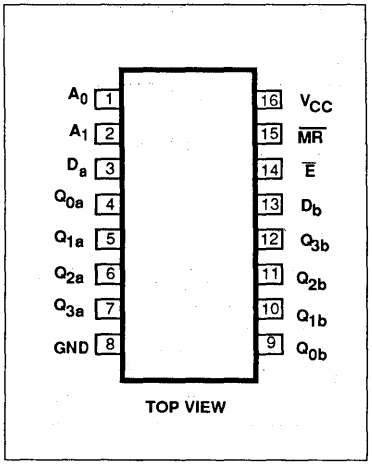
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F256N
16-Pin Plastic SO	N74F256D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_a, D_b	Port A, port B inputs	1.0/1.0	20µA/0.6mA
A_0, A_1	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}$	Enable (active Low)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset inputs (active Low)	1.0/1.0	20µA/0.6mA
Q_{0a} - Q_{3a}	Port A outputs	50/33	1.0mA/20mA
Q_{0b} - Q_{3b}	Port B outputs	50/33	1.0mA/20mA

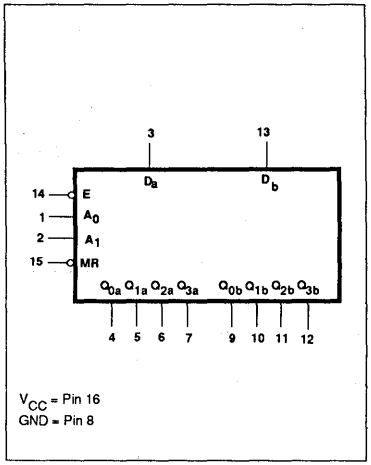
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



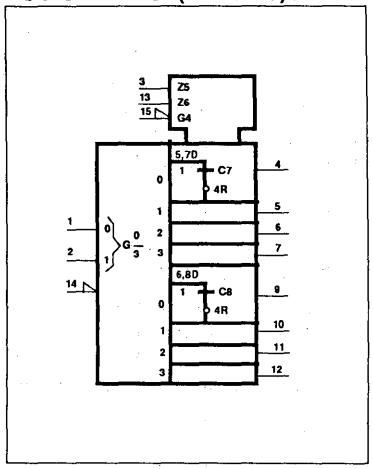
TOP VIEW

LOGIC SYMBOL

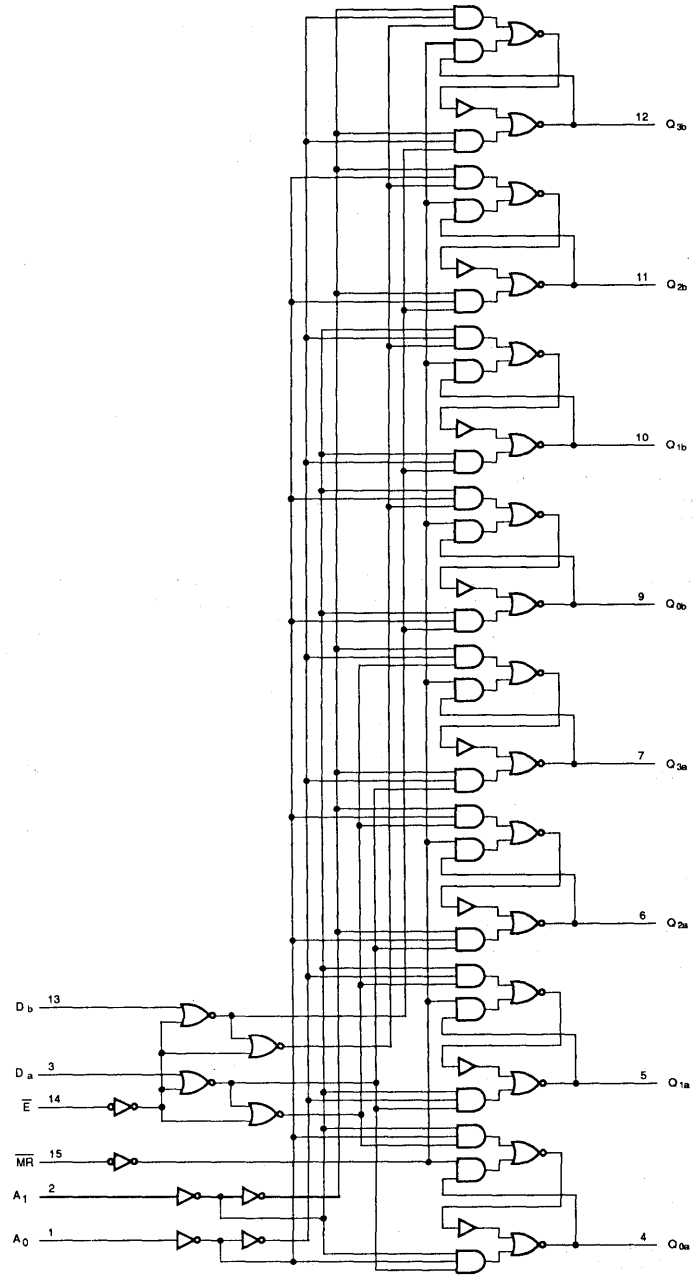


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

FUNCTION TABLE

INPUTS					OUTPUTS				OPERATING MODE
$\overline{MR}$	$\overline{E}$	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3	
L	H	X	X	X	L	L	L	L	Master Reset
L	L	d	L	L	Q=d	L	L	L	Demultiplex (active-High decoder when D=H)
L	L	d	H	L	L	Q=d	L	L	
L	L	d	L	H	L	L	Q=d	L	
L	L	d	H	H	L	L	L	Q=d	
H	H	X	X	X	q_0	q_1	q_2	q_3	Store (do nothing)
H	L	d	L	L	Q=d	q_1	q_2	q_3	Addressable Latch
H	L	d	H	L	q_0	Q=d	q_2	q_3	
H	L	d	L	H	q_0	q_1	Q=d	q_3	
H	L	d	H	H	q_0	q_1	q_2	Q=d	

H = High voltage level
L = Low voltage level
X = Don't care
d = High or Low data one setup time prior to the Low-to-High Enable transition
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			21	42	mA
		I_{CCL}				33	60	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. To reduce the effect of external noise during test.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

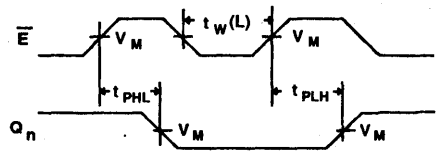
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 2	4.0 3.0	7.0 5.0	9.5 7.0	4.0 2.5	10.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n	Waveform 1	4.5 3.0	8.0 5.0	10.5 7.0	4.5 3.0	12.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 3	5.0 4.5	10.0 8.5	14.0 9.5	5.0 4.0	14.5 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 4	5.0	7.0	9.0	4.5	10.0	ns

AC SETUP REQUIREMENTS

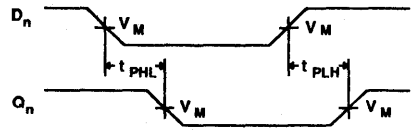
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{E}$	Waveform 5	3.0 6.5			3.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{E}$	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n to $\overline{E}$[1]	Waveform 6	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n to $\overline{E}$[2]	Waveform 6	0 0			0 0		ns
$t_w(L)$	$\overline{E}$ Pulse width, Low	Waveform 1	7.5			8.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 4	3.0			3.0		ns

NOTES:
1. The Address to Enable setup time is the time before the High-to -Low Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The Address to Enable hold time is the time before the Low-to -High Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

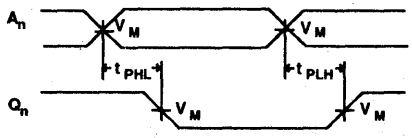
AC WAVEFORMS



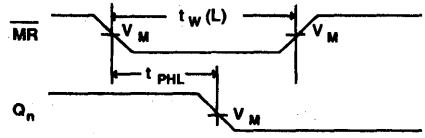
Waveform 1. Propagation Delay, Enable Input To Output, Enable Pulse Width



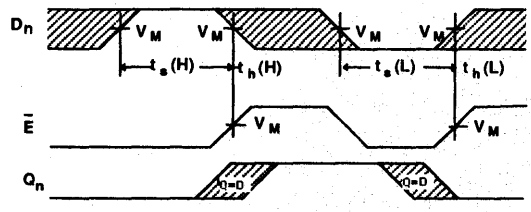
Waveform 2. Propagation Delay, Data To Output



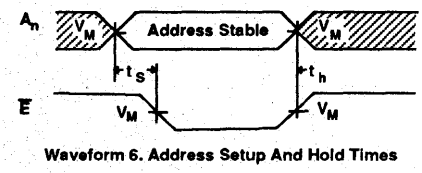
Waveform 3. Propagation Delay Address To Output



Waveform 4. Master Reset Pulse Width And Master Reset to Output Delay



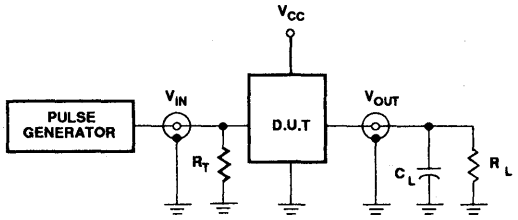
Waveform 5. Data Setup And Hold Times



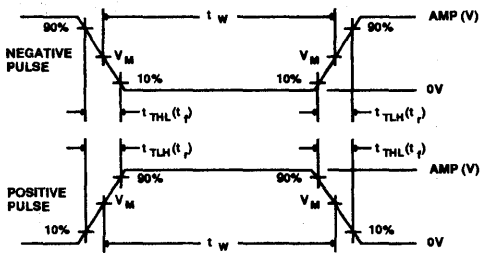
Waveform 6. Address Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAST 74F257, 74F257A
Data Selectors/Multiplexers

FAST Products

74F257 Quad 2-Line To 1-Line Selector/Multiplexer, Non-Inverting (3-State)
74F257A Quad 2-Line To 1-Line Selector/Multiplexer, Non-Inverting (3-State)

FEATURES

- **Multifunction capability**
- **Non-Inverting data path**
- **3-state outputs**
- **See 'F258A for inverting version**

DESCRIPTION

The 74F257/74F257A has four identical 2-input multiplexers with 3-state outputs which select 4 bits of data from two sources under control of a common Select (S) input. The I_{0n} inputs are selected when the common Select input is Low and the I_{1n} inputs are selected when the common Select input is High. Data appears at the outputs in true non-inverted form from the selected inputs. The 'F257/'F257A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the common Select input. Outputs are forced to a high impedance "off" state when the Output Enable ($\overline{OE}$) is High. All but one device must be in high impedance state to avoid currents that would exceed the maximum ratings if the outputs were tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of 3-state devices were tied together.

The 74F257A is the faster version of 74F257.

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F257	4.3ns	12mA
74F257A	4.3ns	12mA

ORDERING INFORMATION

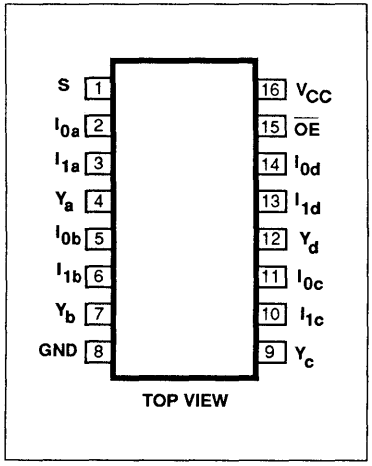
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F257N, N74F257AN
16-Pin Plastic SO	N74F257D, N74F257AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

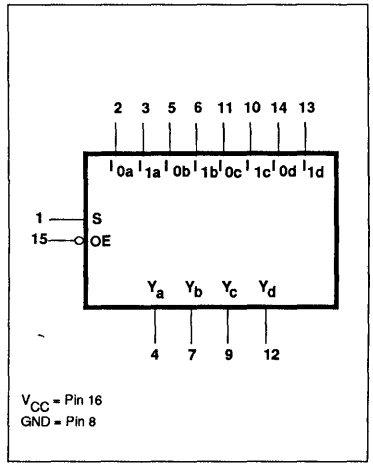
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0n}, I_{1n}	Data inputs	1.0/1.0	20µA/0.6mA
S	Common Select input	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{Y}_a$ - $\overline{Y}_d$	Data outputs	150/33	3.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

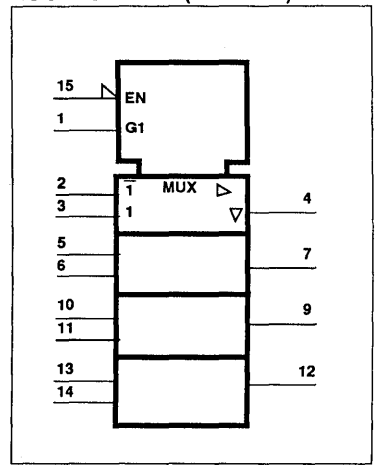
PIN CONFIGURATION



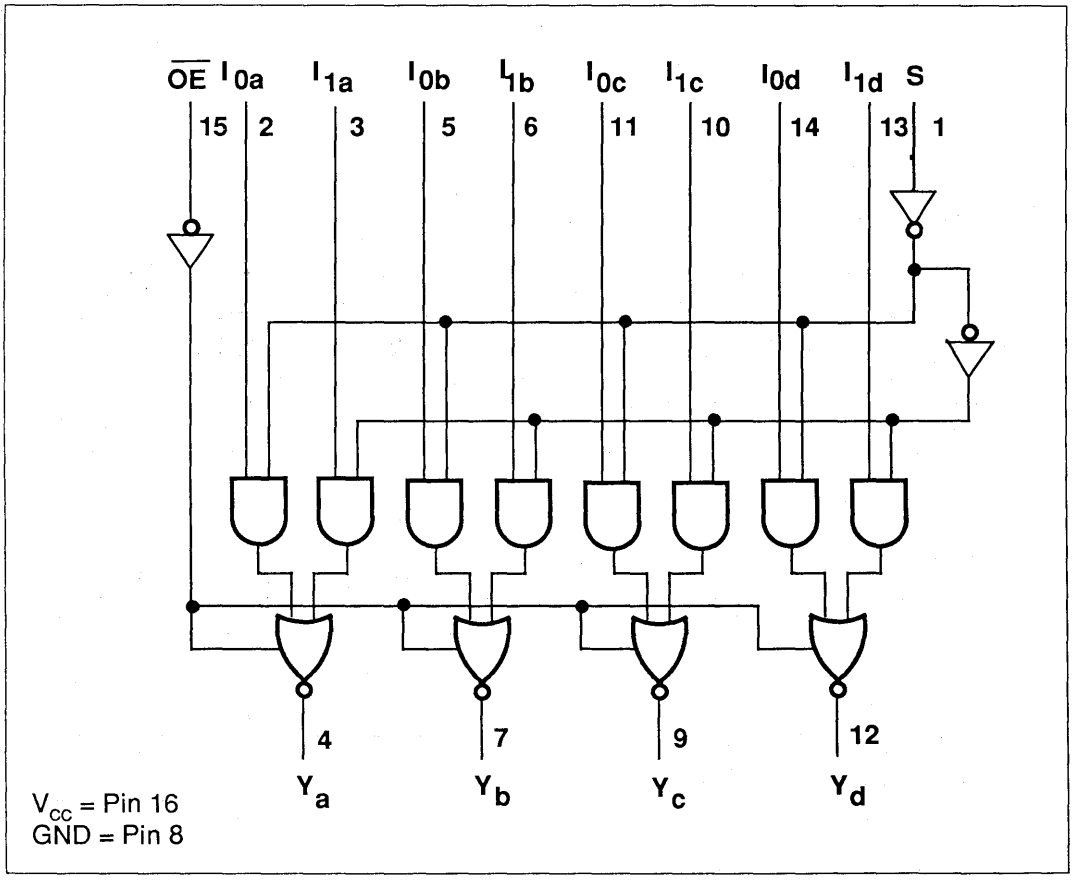
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM

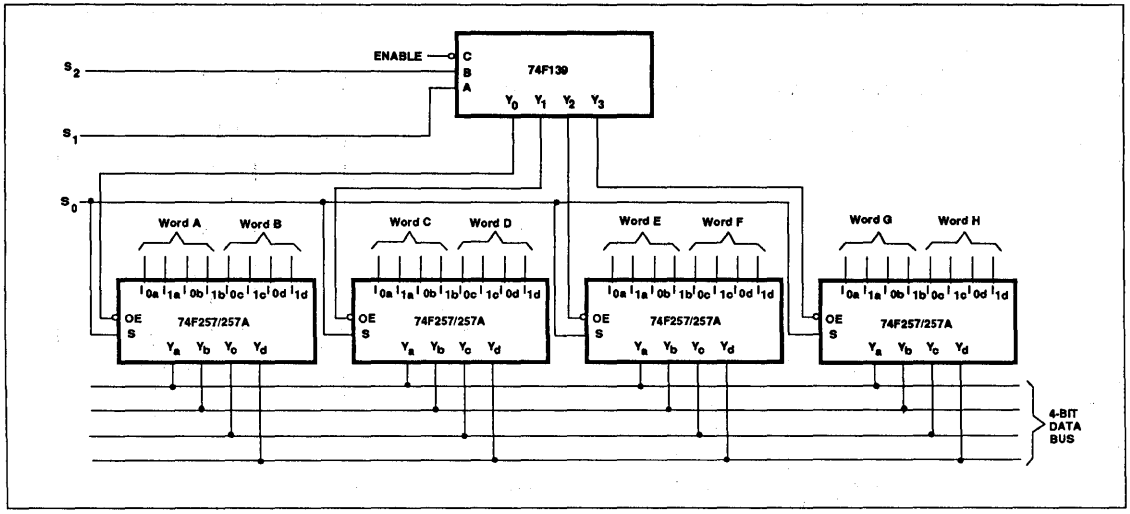


FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

APPLICATION



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
				V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
				V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]			V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[4] (total)	'F257	I_{CCH}	V_{CC} = MAX			9.0	16.0	mA
			I_{CCL}				14.5	22.0	mA
			I_{CCZ}				15.0	23.0	mA
		'F257A	I_{CCH}	V_{CC} = MAX			9.0	15.0	mA
			I_{CCL}				14.5	22.0	mA
			I_{CCZ}				15.0	23.0	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed lasty.
4. Measure I_{CC} with all outputs open and inputs grounded.

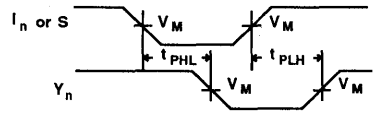
AC ELECTRICAL CHARACTERISTICS for 'F257

SYMBOL	PARAMETER	TEST CONDITION	LIMITS T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	LIMITS T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH}	Propagation delay	Waveform 1	3.0	4.5	6.0	3.0	7.0	ns
t_{PHL}	I_n to Y_n		2.0	3.5	5.5	2.0	6.5	
t_{PLH}	Propagation delay	Waveform 1	4.5	8.0	13.0	4.5	15.0	ns
t_{PHL}	S to Y_n		3.5	6.0	8.5	3.5	9.5	
t_{PZH}	Output Enable time to	Waveform 2	3.0	6.0	7.5	3.0	8.5	ns
t_{PZL}	High or Low level	Waveform 3	3.0	6.0	7.5	3.0	8.5	
t_{PHZ}	Output Disable time from	Waveform 2	2.0	4.0	6.0	2.0	7.0	ns
t_{PLZ}	High or Low level	Waveform 3	2.0	3.5	6.0	2.0	7.0	

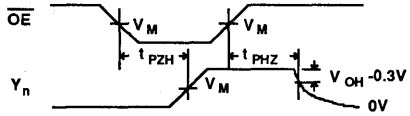
AC ELECTRICAL CHARACTERISTICS for 'F257A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	Waveform 1	3.0 2.0	4.5 3.5	6.0 5.0	3.0 2.0	7.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay S to Y_n	Waveform 1	5.5 4.0	7.5 5.5	9.5 7.0	5.0 4.0	10.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	4.5 4.5	6.5 6.0	7.5 7.5	4.5 4.5	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 2 Waveform 3	2.0 2.0	4.0 3.5	5.5 5.5	2.0 2.0	6.0 6.0	ns

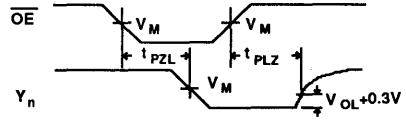
AC WAVEFORMS



Waveform 1. Propagation Delay, Data and Select to Output



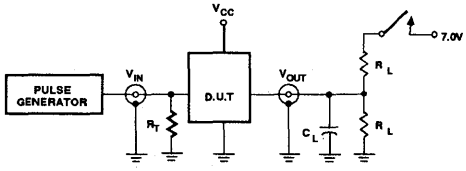
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

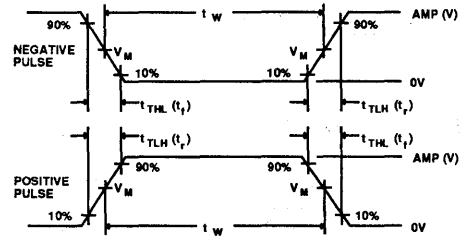
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F258, 74F258A
Data Selectors/Multiplexers

FAST Products

74F258 Quad 2-Line To 1-Line Selector/Multiplexer, Inverting (3-State)
74F258A Quad 2-Line To 1-Line Selector/Multiplexer, Inverting (3-State)

Product Specification

FEATURES

- **Multifunction capability**
- **Inverting data path**
- **3-state outputs**
- **See 'F257A for non-inverting version**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F258	3.8ns	10.7mA
74F258A	3.5ns	14mA

DESCRIPTION

The 74F258/74F258A has four identical 2-input multiplexers with 3-state outputs which select 4 bits of data from two sources under control of a common Select (S) input. The I_{0n} inputs are selected when the Select input is Low and the I_{1n} inputs are selected when the Select input is High. Data appears at the outputs in inverted form. The 'F258/'F258A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic level supplied to the Select input. Outputs are forced to a high impedance "off" state when the Output Enable input ($\overline{OE}$) is High. All but one device must be in high impedance state to avoid currents that would exceed the maximum ratings if the outputs are tied together. Design of the output signals must ensure that there is no overlap when outputs of 3-state devices are tied together.

The 'F258A is the faster version of 'F258.

ORDERING INFORMATION

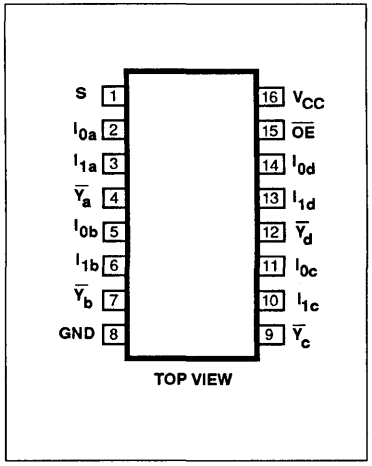
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F258N, N74F258AN
16-Pin Plastic SO	N74F258D, N74F258AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

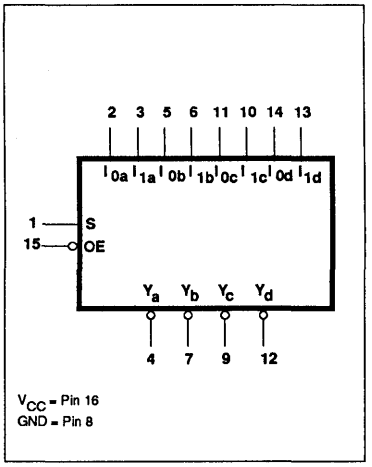
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0n}, I_{1n}	Data inputs	1.0/1.0	20µA/0.6mA
S	Common Select input	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{Y}_a$ - $\overline{Y}_d$	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

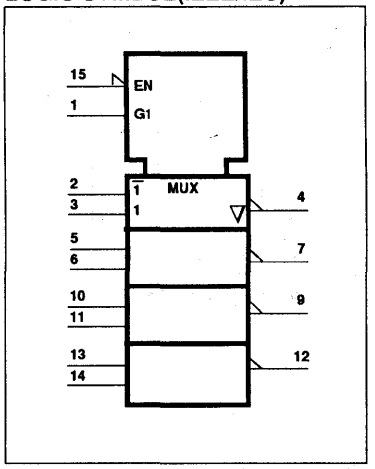
PIN CONFIGURATION



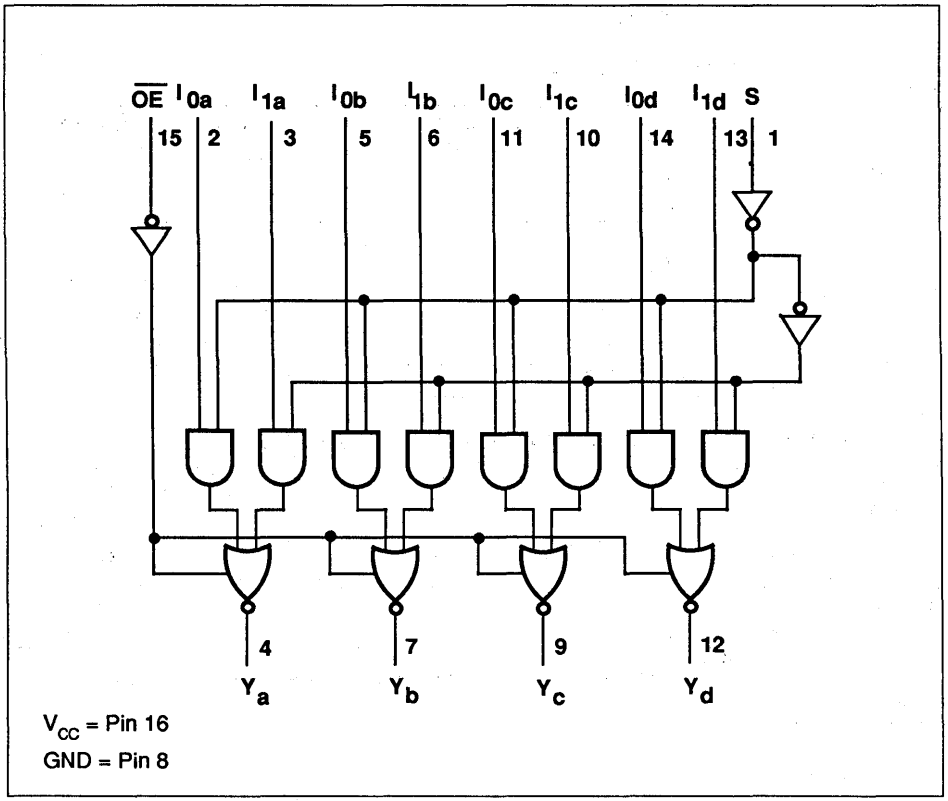
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	I_{1n}= 4.5V, $\overline{OE}$= I_{0n}= S= GND		8.5	11.5	mA
		I_{CCL}		I_{1n}= S= 4.5V, $\overline{OE}$= I_{0n}= GND		17	23	mA
		I_{CCZ}		I_{1n}= $\overline{OE}$= 4.5V, I_{0n}= S= GND		16	22	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

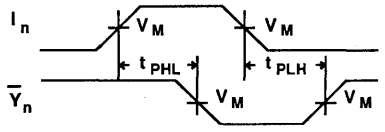
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F258					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	Waveform 1	2.5 1.0	4.0 2.5	6.0 4.7	2.5 1.0	7.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}_n$	Waveform 2	3.5 2.5	6.5 6.0	8.5 9.5	3.5 2.5	9.5 11.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 3 Waveform 4	3.0 3.0	5.9 5.5	7.5 7.5	3.0 3.0	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 3 Waveform 4	2.0 2.0	3.5 3.5	6.0 6.0	2.0 2.0	7.0 7.0	ns

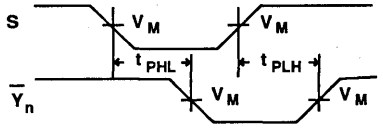
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F258A					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	Waveform 1	3.0 1.0	4.5 2.5	6.0 4.0	2.5 1.0	7.0 4.5	ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}_n$	Waveform 2	3.5 2.5	6.5 6.0	8.0 8.0	3.5 2.5	9.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 3 Waveform 4	4.0 4.0	6.0 5.5	7.5 7.5	3.5 3.5	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 3 Waveform 4	2.0 2.0	3.5 3.5	5.5 5.5	2.0 2.0	6.5 6.0	ns

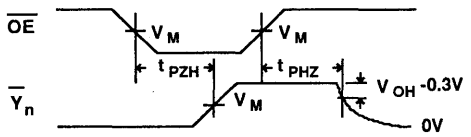
AC WAVEFORMS



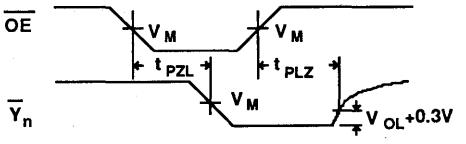
Waveform 1. Propagation Delay, Data to Output



Waveform 2. Propagation Delay, Select to Output



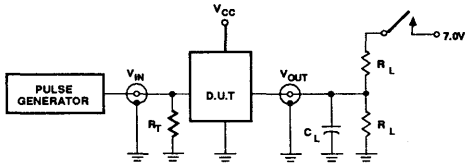
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

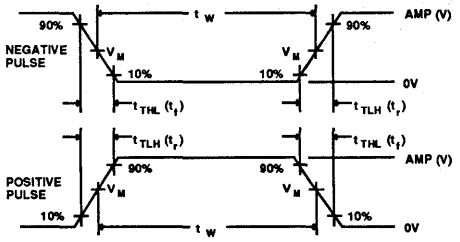
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F259
Latch

FAST Products

FEATURES

- **Combines demultiplexer and 8-bit latch**
- **Serial-to-parallel capability**
- **Output from each storage bit available**
- **Random (addressable) data entry**
- **Easily expandable**
- **Common reset input**
- **Useful as a 1-of-8 active-High decoder**

DESCRIPTION

The 74F259 addressable latch has four distinct modes of operation which are selectable by controlling the Master Reset ($\overline{MR}$) and Enable ($\overline{E}$) inputs (see Function Table). In the addressable latch mode, data at the Data inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the store mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the Enable should be held High (inactive) while the address lines are changing. In the 1-0f-8 decoding or demultiplexing mode ($\overline{MR}$=$\overline{E}$=Low), addressed outputs will follow the level of the Data input, with all other outputs Low. In the Master Reset mode, all outputs are Low and unaffected by the Address and Data inputs.

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F259	7.5ns	31mA

ORDERING INFORMATION

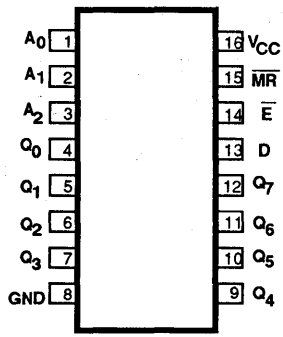
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F259N
16-Pin Plastic SO	N74F259D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D	Data input	1.0/1.0	20µA/0.6mA
A_0, A_1, A_2	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}$	Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset inputs (active Low)	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

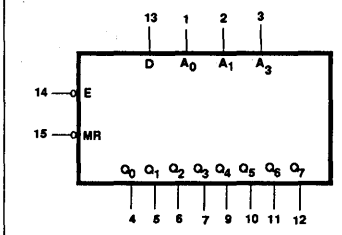
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



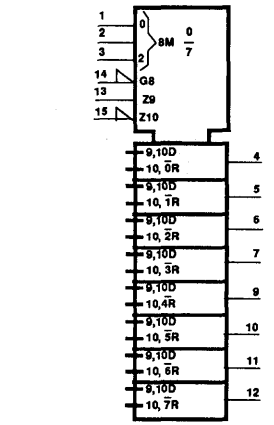
TOP VIEW

LOGIC SYMBOL

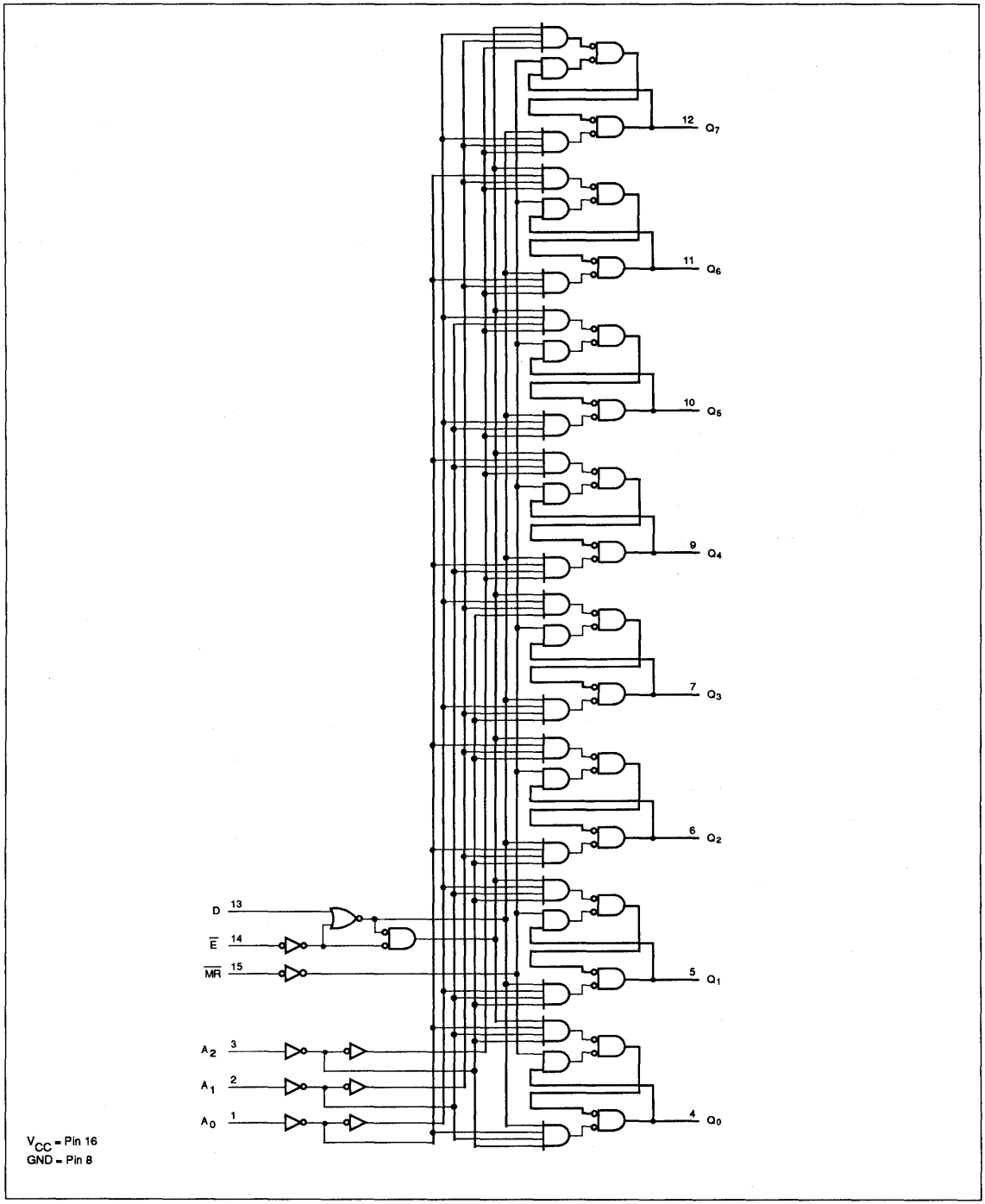


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS								OPERATING MODE
$\overline{MR}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	L	L	L	L	L	L	L	L	L	Master Reset
L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L	Demultiplex (active-High decoder when D=H)
L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L	
L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L	
.	.	.	.	.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	.	.	.	.	
L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d	
H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7	Store (do nothing)
H	L	d	L	L	L	Q=d	q_1	q_2	q_3	q_4	q_5	q_6	q_7	Addressable Latch
H	L	d	H	L	L	q_0	Q=d	q_2	q_3	q_4	q_5	q_6	q_7	
H	L	d	L	H	L	q_0	q_1	Q=d	q_3	q_4	q_5	q_6	q_7	
.	.	.	.	.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	.	.	.	.	
H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q=d	

H = High voltage level
L = Low voltage level
X = Don't care
d = High or Low data one setup time prior to the Low-to-High Enable transition
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			24	46	mA
		I_{CCL}				37	75	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. To reduce the effect of external noise during test.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

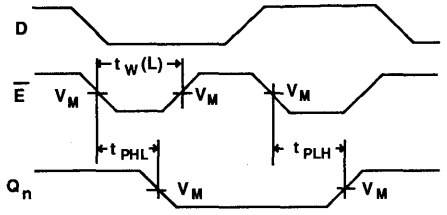
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D to Q_n	Waveform 1	4.0 3.0	7.0 5.0	9.0 7.0	4.0 2.5	10.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n	Waveform 1	4.5 3.0	8.0 5.0	10.5 7.0	4.5 3.0	12.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 2	5.0 4.0	10.0 8.5	14.0 9.5	5.0 4.0	14.5 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 3	5.0	7.0	9.0	4.5	10.0	ns

AC SETUP REQUIREMENTS

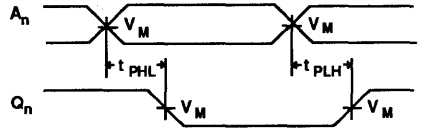
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D to $\overline{E}$	Waveform 4	3.0 6.5			3.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D to $\overline{E}$	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n to $\overline{E}$[1]	Waveform 5	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n to $\overline{E}$[2]	Waveform 5	0 0			0 0		ns
$t_w(L)$	$\overline{E}$ Pulse width, Low	Waveform 1	7.5			8.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 3	3.0			3.0		ns

NOTES:
1. The Address to Enable setup time is the time before the High-to-Low Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The Address to Enable hold time is the time before the Low-to-High Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

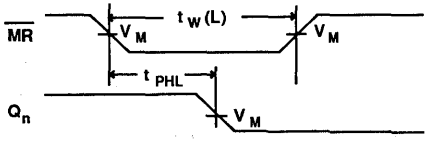
AC WAVEFORMS



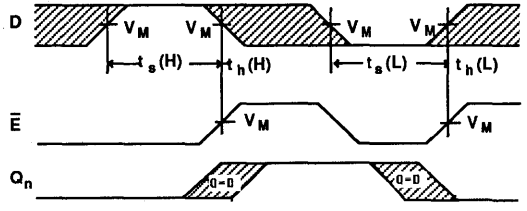
Waveform 1. Propagation Delay, Enable Input To Output, Enable Pulse Width



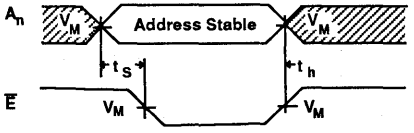
Waveform 2. Propagation Delay Address To Output



Waveform 3. Master Reset Pulse Width And Master Reset to Output Delay



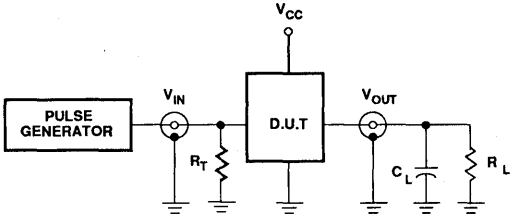
Waveform 4. Data Setup And Hold Times



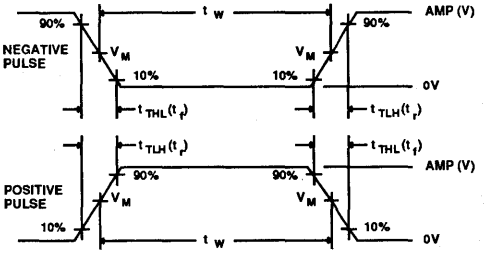
Waveform 5. Address Setup And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAST 74F260 Gate

Dual 5-Input NOR Gate

FAST Products

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F260	3.5 ns	6 mA

ORDERING INFORMATION

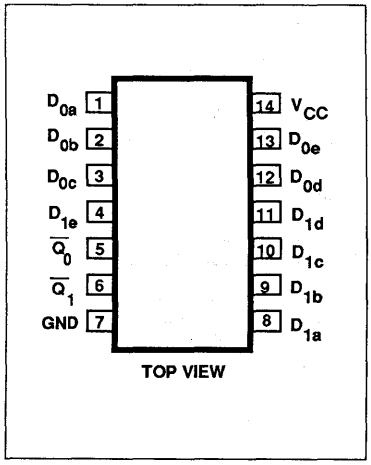
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F260N
14-Pin Plastic SO	N74F260D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

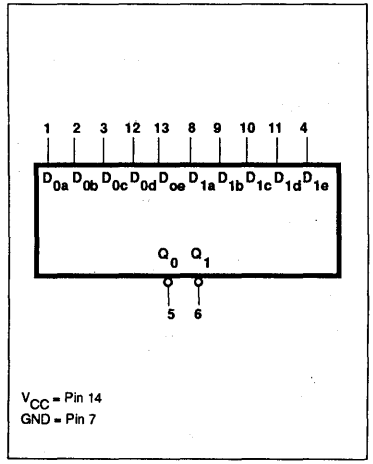
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}, D_{nc}, D_{nd}, D_{ne}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}_0$, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

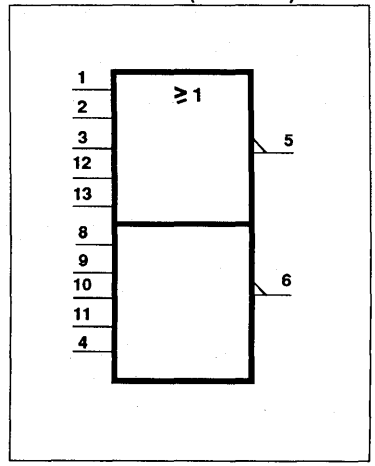
PIN CONFIGURATION



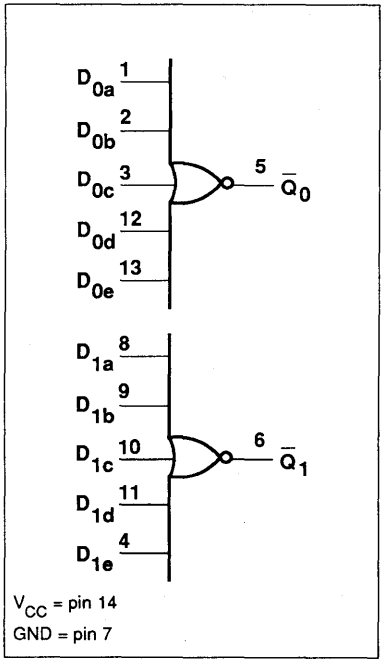
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = pin 14
GND = pin 7

FUNCTION TABLE

INPUTS					OUTPUT
D_{na}	D_{nb}	D_{nc}	D_{nd}	D_{ne}	$\overline{Q}_n$
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
L	L	L	L	L	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

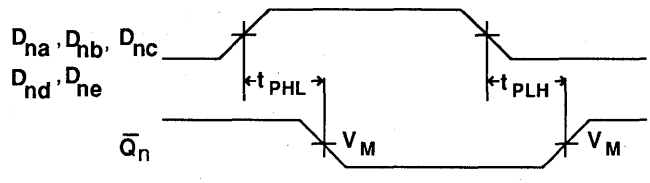
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN}=GND		4.6	6.5	mA
		I_{CCL}		V_{IN}=4.5V		7.3	9.5	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd}, D_{ne} to $\overline{Q}_n$	Waveform 1	2.5 1.5	4.0 2.5	5.5 4.0	2.0 1.0	6.5 4.5	ns

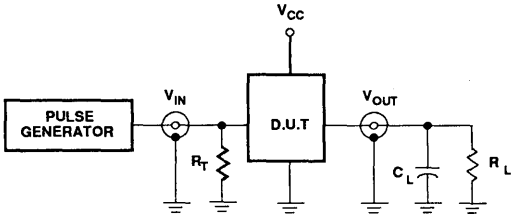
AC WAVEFORMS



Waveform 1. For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



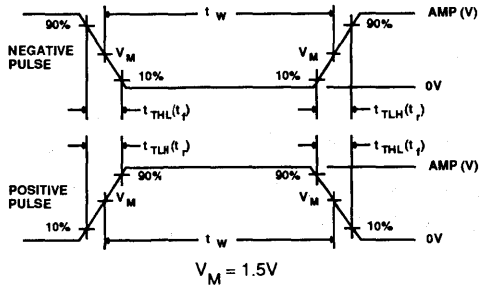
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F269 Counter

FAST Products

8-Bit Bidirectional Binary Counter
Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F269	115MHz	95mA

FEATURES

- **Synchronous counting and loading**
- **Built-in look-ahead carry capability**
- **Count frequency 115 MHz typ**
- **Supply current 95mA typ**

DESCRIPTION

The 74F269 is a fully synchronous 8-stage Up/Down Counter featuring a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

ORDERING INFORMATION

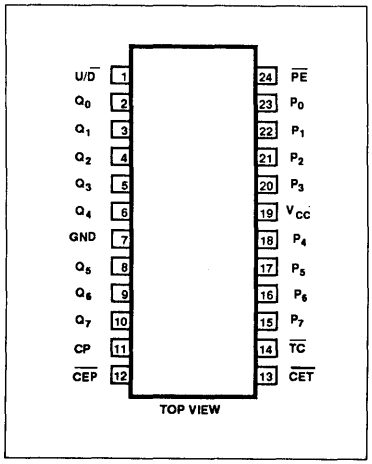
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim Dip (300 mil)	N74F269N
24-Pin Plastic SOL	N74F269D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

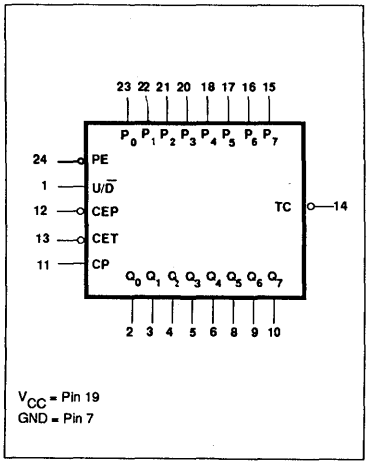
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
P_0 - P_7	Parallel Data inputs	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/1.0	20µA/0.6mA
U/$\overline{D}$	Up/Down count control input	1.0/1.0	20µA/0.6mA
$\overline{CEP}$	Count Enable Parallel input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20µA/0.6mA
$\overline{TC}$	Terminal Count output (active Low)	50/33	1.0mA/20mA
Q_0 - Q_7	Flip-flop outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

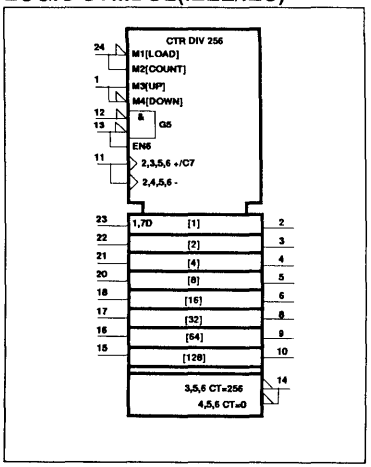
PIN CONFIGURATION



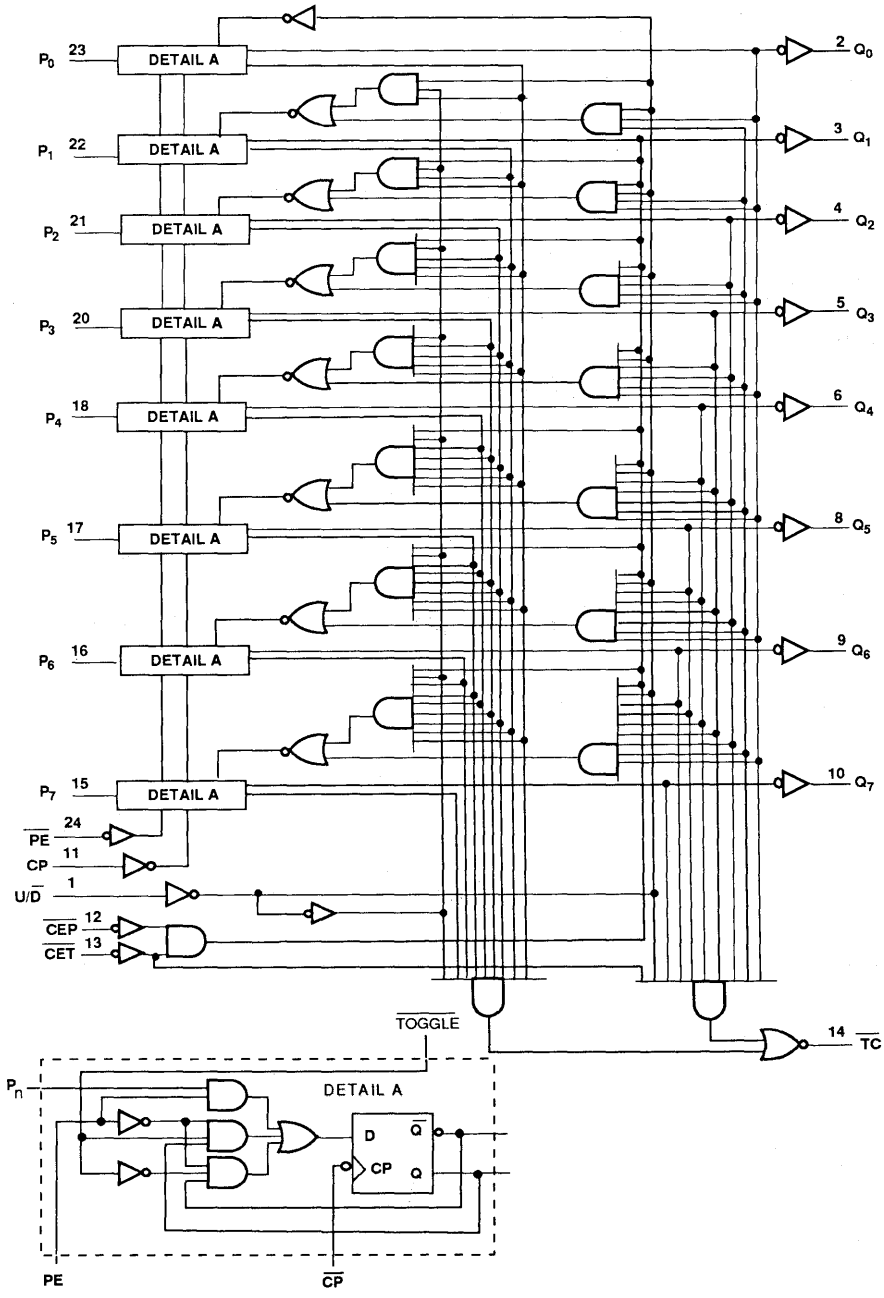
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} =pin19
GND=pin 7

MODE SELECT-FUNCTION TABLE

INPUTS						OUTPUTS		OPERATING MODE
CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	P_n	Q_n	$\overline{TC}$	
↑	X	X	X	l	l	L	(a)	Parallel load
↑	X	X	X	l	h	H	(a)	
↑	h	l	l	h	X	Count up	(a)	Count up
↑	l	l	l	h	X	Count down	(a)	Count down
↑	X	h	l	h	X	q_n	(a)	Hold (do nothing)
↑	X	X	h	h	X	q_n	H	

H = High voltage level
h = High voltage level one setup prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup prior to the Low-to-High clock transition
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
(a) = $\overline{TC}$ is Low when $\overline{CET}$ is Low and the counter is at Terminal Count. The Terminal Count up is with all Q_n outputs High andTerminal Count Down is with all Q_n outputs Low.

APPLICATION

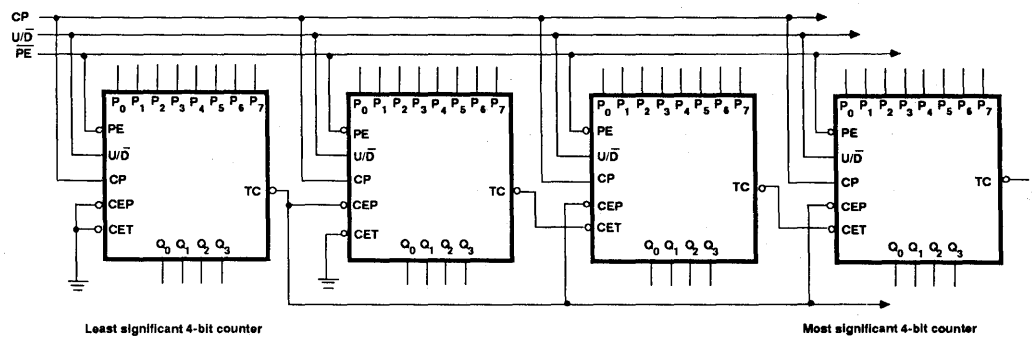


Figure 1
Synchronous multistage counting scheme

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{PE}$=$\overline{CET}$=$\overline{CEP}$=U/$\overline{D}$=GND, P_n=4.5V, CP=↑		93	120	mA
		I_{CCL}		$\overline{PE}$=$\overline{CET}$=$\overline{CEP}$=U/$\overline{D}$=GND, P_n=GND, CP=↑		98	125	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

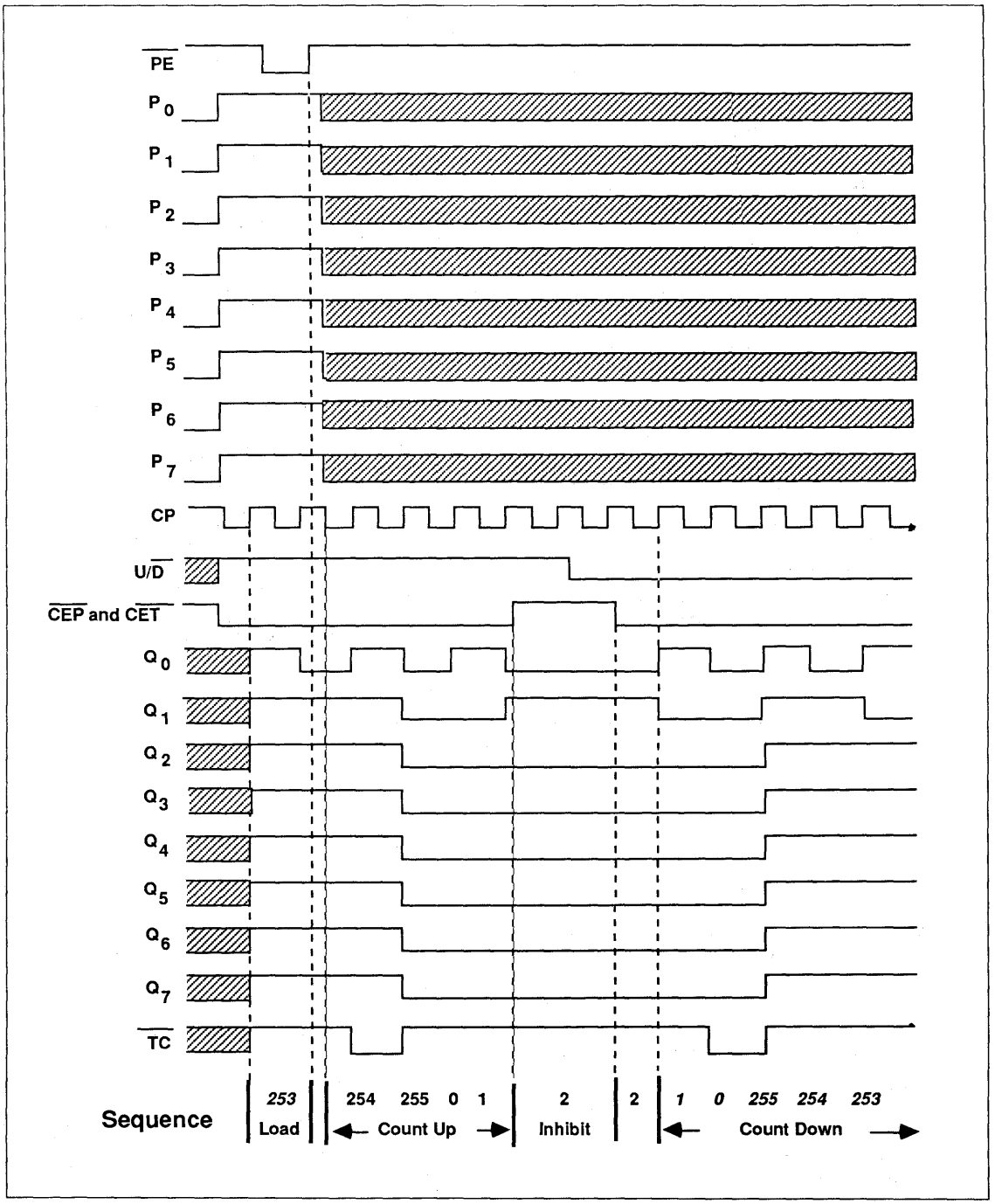
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		85		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n (Load, $\overline{PE}$=Low)	Waveform 1	3.0 4.0	6.0 6.5	8.5 8.5	3.0 4.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n (Count, $\overline{PE}$=High)	Waveform 1	3.0 4.5	6.0 7.0	9.0 10.0	3.0 4.0	10.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	4.5 5.0	6.5 6.5	9.5 9.5	4.0 5.0	10.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	3.5 3.5	6.0 6.5	9.0 9.0	3.0 3.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	Waveform 3	4.5 4.5	7.0 7.0	9.0 9.5	4.0 4.0	10.0 10.0	ns

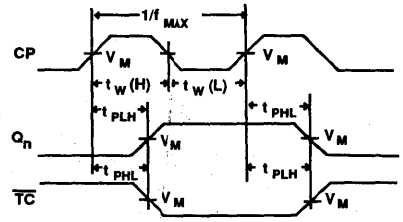
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low P_n to CP	Waveform 4	2.0 2.0			2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low P_n to CP	Waveform 4	0 1.0			0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP	Waveform 4	5.0 5.5			5.5 6.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	4.5 5.5			5.0 6.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/$\overline{D}$ to CP	Waveform 6	5.5 5.5			6.5 6.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low U/$\overline{D}$ to CP	Waveform 6	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 4.5			4.0 5.0		ns

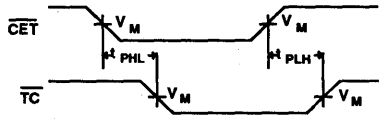
TIMING DIAGRAM (Typical Load, Count and Inhibit Sequence)



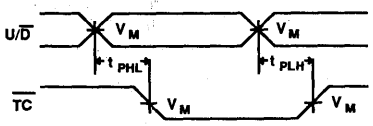
AC WAVEFORMS



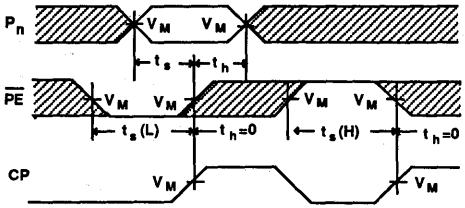
Waveform 1.
Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



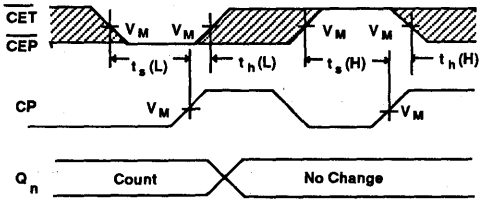
Waveform 2.
Propagation Delay, $\overline{CET}$ Input to Terminal Count Output



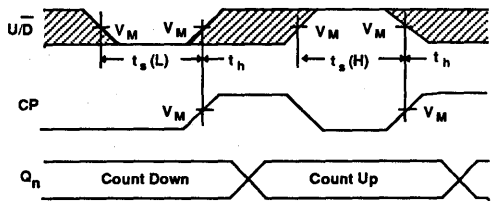
Waveform 3.
Propagation Delay, Up/Down Count Control Input to Terminal Count Output



Waveform 4.
Parallel Data and Parallel Enable Setup and Hold Times



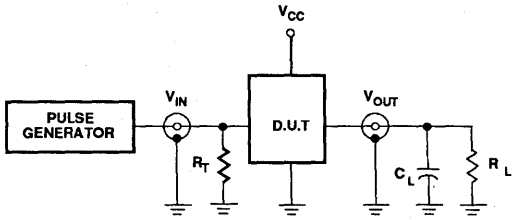
Waveform 5.
Count Enables Setup and Hold Times



Waveform 6.
Up/Down Count Control Setup and Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

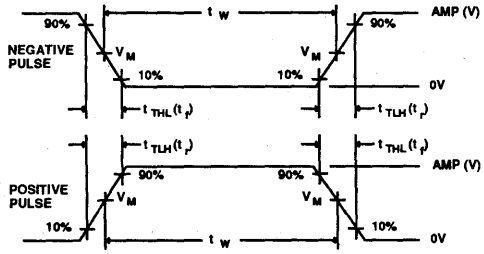
TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F273
Flip-Flop

FAST Products

Octal D Flip-Flop
Product Specification

FEATURES
- **High impedance NPN base inputs for reduced loading (20μA in Low and High states)**
- **Ideal buffer for MOS microprocessor or memory**
- **Eight edge-triggered D-type flip-flops**
- **Buffered common clock**
- **Buffered asynchronous Master Reset**
- **See 'F377 for clock enable version**
- **See 'F373 for transparent latch version**
- **See 'F374 for 3-state version**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F273	125MHz	66mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F273N
20-Pin Plastic SOL	N74F273D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/0.033	20μA/20μA
$\overline{MR}$	Master Reset input (active Low)	1.0/0.033	20μA/20μA
CP	Clock Pulse input (active rising edge)	1.0/0.033	20 A/20 A
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

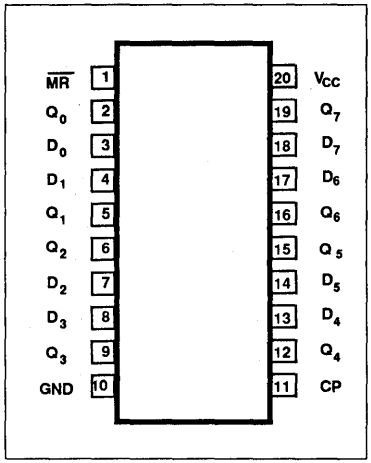
DESCRIPTION

The 74F273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

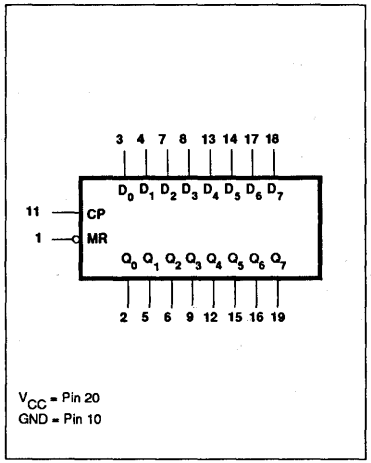
The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the CP and $\overline{MR}$ are common to all elements.

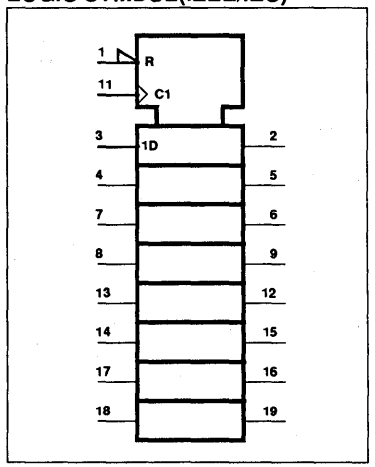
PIN CONFIGURATION



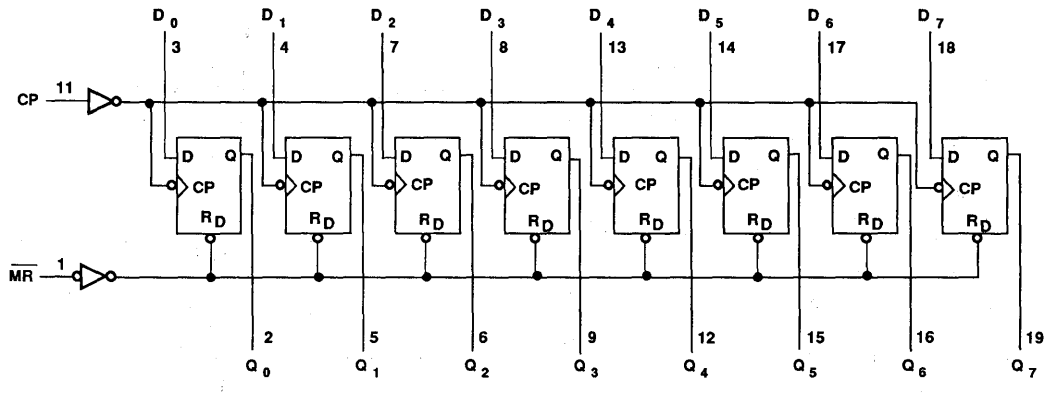
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{MR}$	CP	D_n	Q_0 - Q_7	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$\overline{MR}$ &CP inputs	V_{CC} = MIN, V_{IL} = 0.0V,[3]	±10%V_{CC}	2.5			V
			V_{IH} = 4.5V,[3] I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
		other inputs	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_{OS}	Short circuit output current[4]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			65	85	mA
		I_{CCL}				68	88	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. To reduce the effect of external noise during test.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

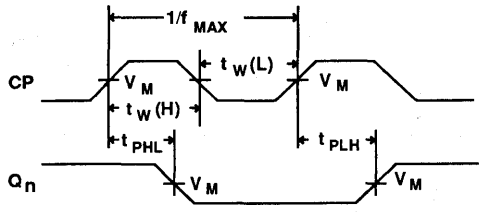
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	115	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n	Waveform 1	4.0 4.0	7.5 7.5	9.5 9.5	4.0 4.0	10.5 10.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	4.0	5.5	8.5	3.5	9.0	ns

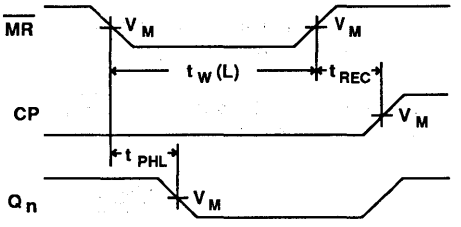
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 3	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.5		ns
$t_w(L)$	Master Reset Pulse width, Low	Waveform 2	3.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	8.5			9.0		ns

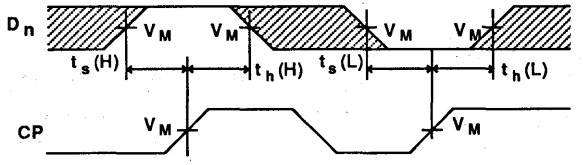
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

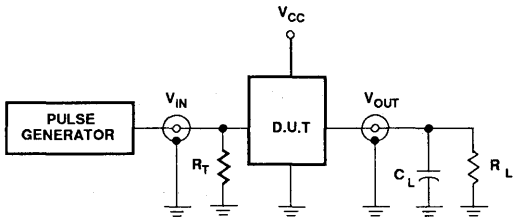


Waveform 3. Data Setup And Hold Times

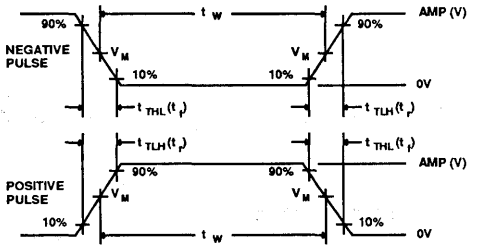
NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F280A, 74F280B
Parity Checker Generator

FAST Products

9-Bit Odd/Even Parity Generator/Checker

Product Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in Low and High states)**
- **Buffered inputs--one normalized load**
- **Word length easily expanded by cascading**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F280A	6.5ns	26mA
74F280B	5.5ns	26mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F280AN, N74F280BN
14-Pin Plastic SO	N74F280AD, N74F280BD

DESCRIPTION

The 74F280A is a 9-bit Parity Generator or Checker commonly used to detect errors in high speed data transmission or data retreival systems. Both Even (Σ_E) and Odd (Σ_O) parity outputs are available for generating and checking even or odd parity on up to 9 bits.

The Even (Σ_E) parity output is High when an even number of data inputs (I_0-I_8) are HIgh. The Odd (Σ_O) parity output is High when an odd number of data inputs are High.

Expansion to larger word sizes is accomplished by tying the Even (Σ_E) outputs of up to nine parallel devices to the data inputs of the final stage. This expansion scheme allows an 81-bit data word to be checked in less than 20ns.

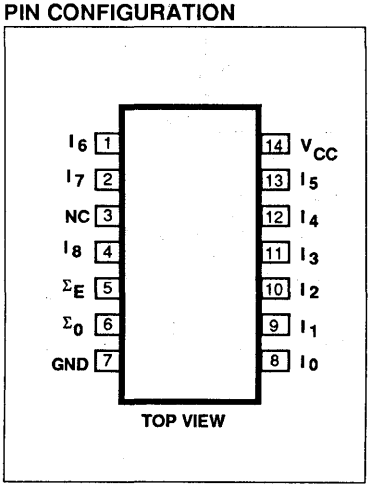
The 74F280B is a faster version of 74F280A.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0-I_8	Data inputs	1.0/0.033	20μA/20μA
Σ_E, Σ_O	Parity outputs	50/33	1.0mA/20mA

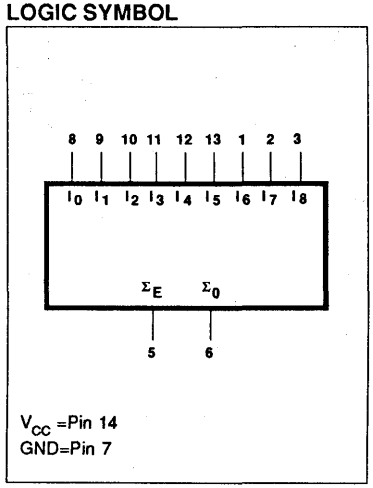
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



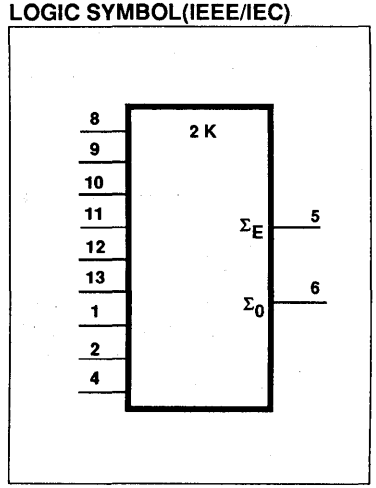
TOP VIEW

LOGIC SYMBOL

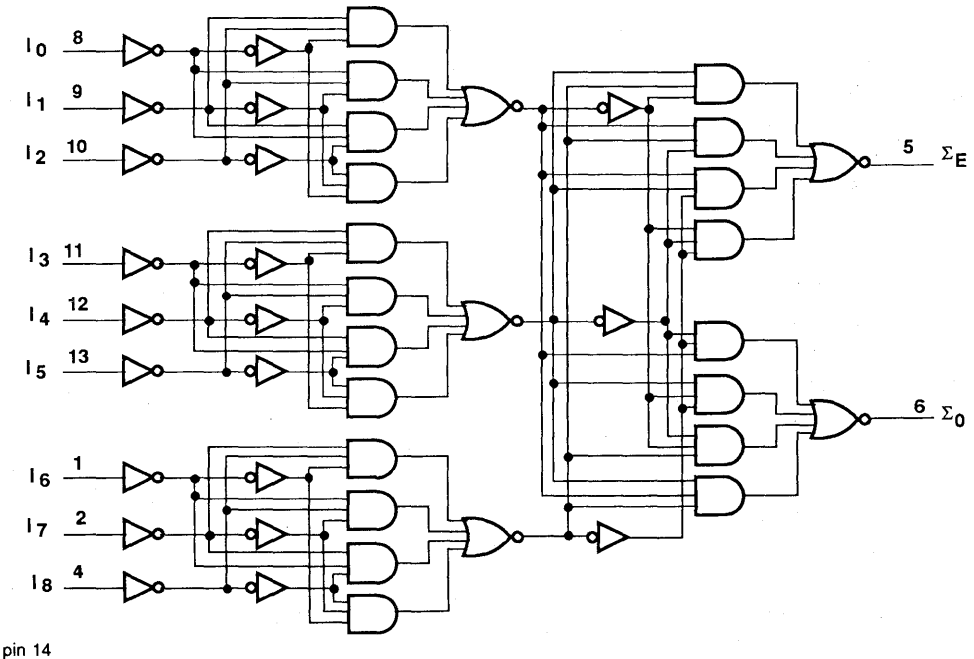


V_{CC} =Pin 14
GND=Pin 7

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = pin 14
GND = pin 7

FUNCTION TABLE

INPUTS	OUTPUTS	
Number of High data inputs (I_0-I_8)	Σ_E	Σ_O
Even ------ 0, 2, 4, 6, 8	H	L
Odd ------1, 3, 5, 7, 9	L	H

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-20	µA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			26	35	mA

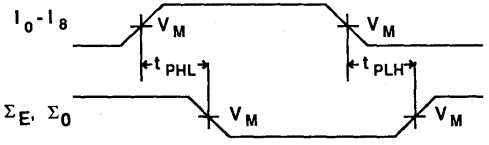
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

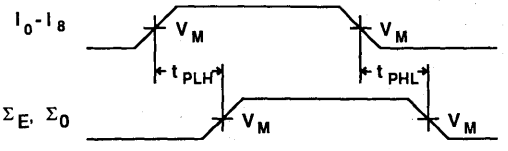
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_E	'F280A	Waveform 1,2	5.0 9.0	7.0 11.1	9.0 13.0	5.0 7.5	10.0 14.5	ns
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_O	'F280A	Waveform 1,2	6.5 7.0	8.6 9.1	10.5 12.0	6.5 6.0	11.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_E	'F280B	Waveform 1,2	4.0 4.0	6.5 7.0	9.0 10.0	3.5 3.5	10.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_O	'F280B	Waveform 1,2	4.0 4.0	6.5 7.0	9.0 10.0	3.5 3.5	10.0 11.0	ns

AC WAVEFORMS



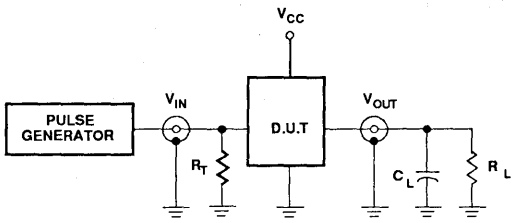
Waveform 1. Propagation Delay For Inverting Outputs



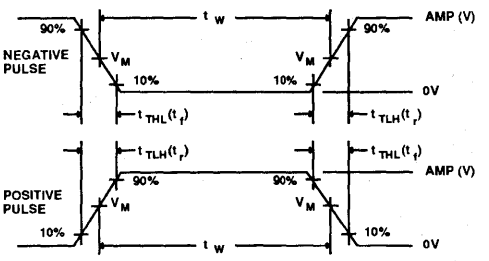
Waveform 2. Propagation Delay For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F283

4-Bit Binary Full Adder With Fast Carry

Product Specification

FEATURES

- **High speed 4-bit binary addition**
- **Cascadable in 4-bit increments**
- **Fast internal carry look-ahead**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F283	6.5ns	40mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F283N
16-Pin Plastic SO	N74F283D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	A operand inputs	1.0/2.0	20µA/1.2mA
B_0 - B_3	B operand inputs	1.0/2.0	20µA/1.2mA
C_{IN}	Carry input	1.0/1.0	20µA/0.6mA
C_{OUT}	Carry output	50/33	1.0mA/20mA
Σ_0 - Σ_3	Sum outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 74F283 adds two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the sum outputs (Σ_0-Σ_3) and the outgoing carry (C_{OUT}) according to the equation:

$C_{IN} + 2^0(A_0 + B_0) + 2^1(A_1 + B_1) + 2^2(A_2 + B_2) + 2^3(A_3 + B_3)$

$= \Sigma_0 + 2\Sigma_1 + 4\Sigma_2 + 8\Sigma_3 + 16C_{OUT}$

where (+) = plus

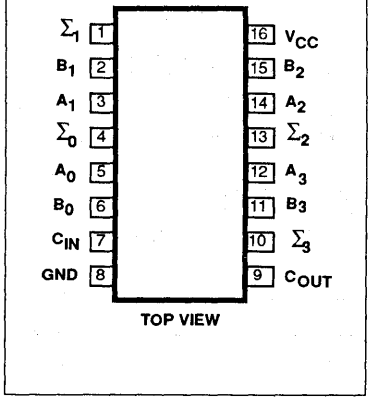
Due to the symmetry of the binary add function, the 'F283 can be used with either all active-High operands (positive logic) or with all active-Low operands (negative logic). See Function Table. In case of all active-Low operands (negative logic) the results Σ_1- Σ_4 and C_{OUT} should be interpreted also as active-Low. With active-High inputs, C_{IN} cannot be left open; it must be held Low when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus A_0, B_0, C_{IN} can arbitrarily be assigned to pins 5, 6, 7, etc.

Due to pin limitations, the intermediate carries of the 'F283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage.

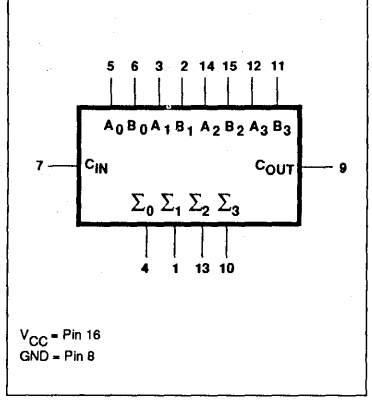
Figure a shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A_3, B_3) Low makes Σ_3 dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, Figure b shows a way of dividing the 'F283 into a 2-bit and a 1-bit adder. The third stage adder (A_2, B_2, Σ_2) is used as means of getting a carry (C_{10}) signal into the fourth stage adder (via A_2 and B_2) and bringing out the carry from the second stage on Σ_2. Note that as long as A_2 and B_2 are the same, whether High or Low, they do not influence Σ_2. Similarly, when A_2 and B_2 are the same, the carry into the third stage does not influence the carry out of the third stage.

Figure c shows a method of implementing a 5-input encoder where the inputs are equally weighted. The outputs Σ_0, Σ_1 and Σ_2 present a binary number equal to the number of inputs I_0 - I_4 that are true. Figure d shows one method of implementing a 5-input majority gate. When three or more of the inputs I_0 - I_4 are true, the output M_4 is true.

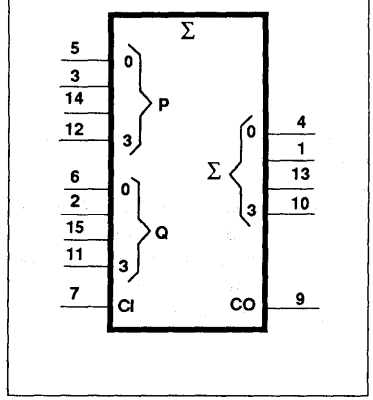
PIN CONFIGURATION



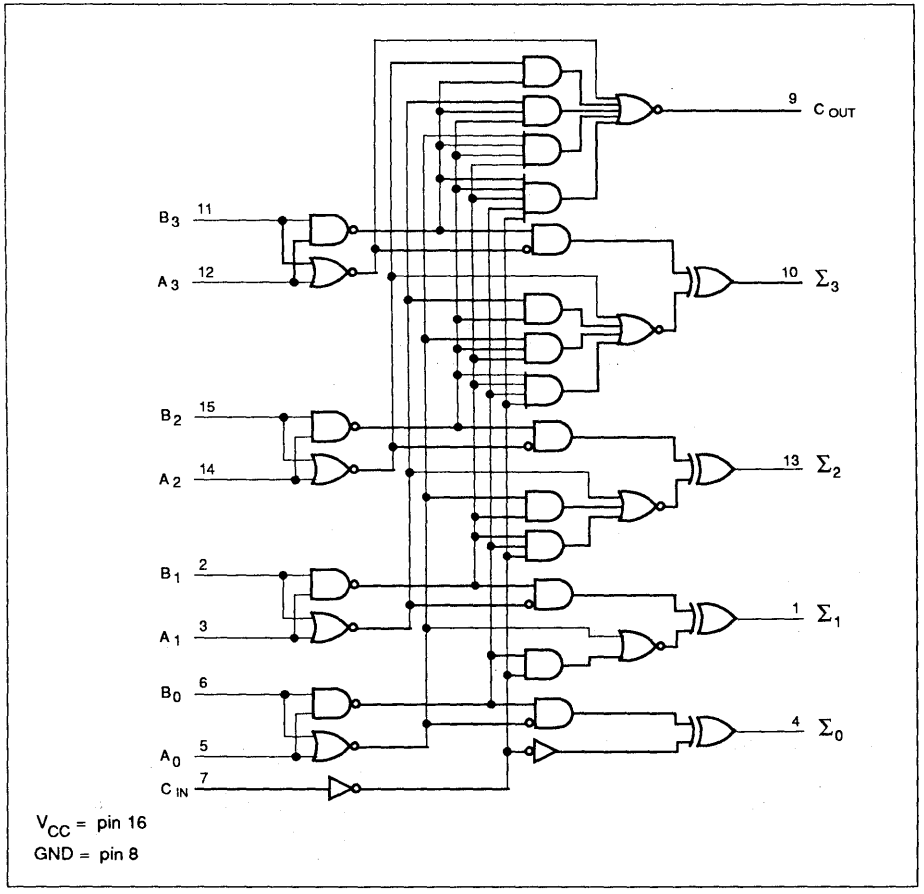
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

PINS	C_{IN}	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	Σ_0	Σ_1	Σ_2	Σ_3	C_{OUT}
Logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active High	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active Low	1	1	0	1	0	0	1	1	0	0	0	1	1	0

H = High voltage level
L = Low voltage level

Example:
1001
1010
10011
(10+9=19)
(carry+5+6=12)

APPLICATIONS

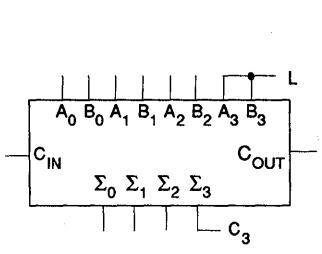


Figure a 3-bit adder

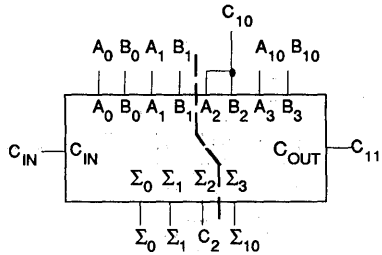


Figure b 2-bit and 1-bit adder

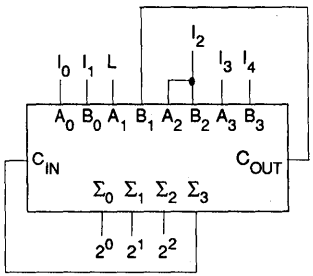


Figure c 5-input Encoder

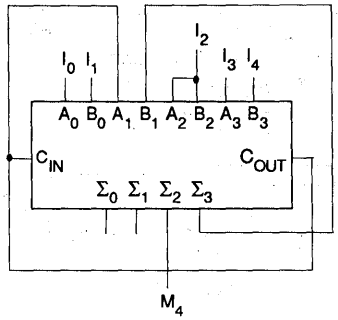


Figure d 5-input majority Gate

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	C_{IN} only	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		A_n, B_n					-1.2	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			40	55	mA

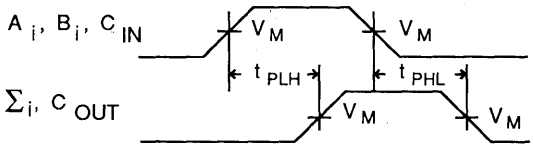
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} should be measured with all outputs open and the following conditions:
   Condition 1: all inputs grounded
   Condition 2: all B intputs Low, other inputs at 4.5V
   Condition 3: all inputs at 4.5V

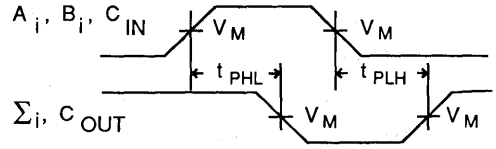
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_i	Waveform 1, 2	3.5 4.0	7.0 7.0	9.5 9.5	3.0 3.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to Σ_i	Waveform 1, 2	3.5 3.5	7.0 7.0	9.5 9.5	2.5 3.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to C_{OUT}	Waveform 2	3.5 3.0	5.7 5.4	7.5 7.0	3.5 2.5	8.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to C_{OUT}	Waveform 1, 2	3.5 2.5	5.7 5.3	7.5 7.0	3.0 2.5	8.5 8.0	ns

AC WAVEFORMS



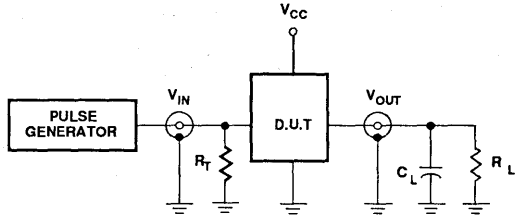
Waveform 1. Propagation Delay
Operands and Carry inputs to Outputs



Waveform 2. Propagation Delay
Operands and Carry inputs to Outputs

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



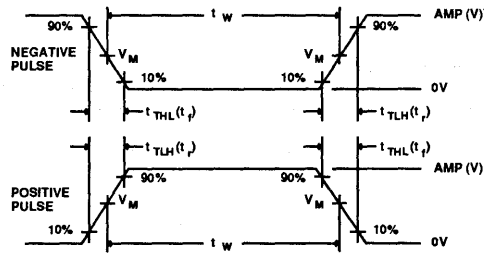
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F298
Multiplexer

Quad 2-Input Multiplexer With Storage

Product Specification

FAST Products

FEATURES

- **Fully synchronous operation**
- **Select from two data sources**
- **Buffered, negative edge triggered clock**
- **Provides the equivalent of function capabilities of two separate MSI functions (74F157 and 74F175)**

DESCRIPTION

The 74F298 is a high speed Quad 2-Input Multiplexer with storage.It selects 4 bits of data from two sources (ports) under the control of a common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the High-to-Low transition of the clock ($\overline{CP}$). The 4-bit register is fully edge triggered. The data inputs (I_0 and I_1) and Select input (S) must be stable only one setup time prior to the High-to-Low transition of the clock for predictable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F298	115MHz	30mA

ORDERING INFORMATION

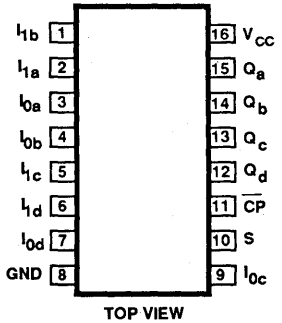
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-pin Plastic DIP	N74F298N
16-pin Plastic SO	N74F298D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0a}, I_{0b}, I_{0c}, I_{0d}	Data inputs	1.0/1.0	20µA/0.6mA
I_{1a}, I_{1b}, I_{1c}, I_{1d}	Data inputs	1.0/1.0	20µA/0.6mA
S	Select input	1.0/1.0	20µA/0.6mA
$\overline{CP}$	Clock input (active falling edge)	1.0/1.0	20µA/0.6mA
Q_a, Q_b, Q_c, Q_d	Data outputs	50/33	1.0mA/20mA

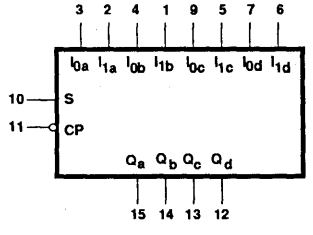
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



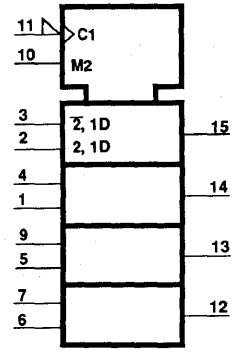
TOP VIEW

LOGIC SYMBOL

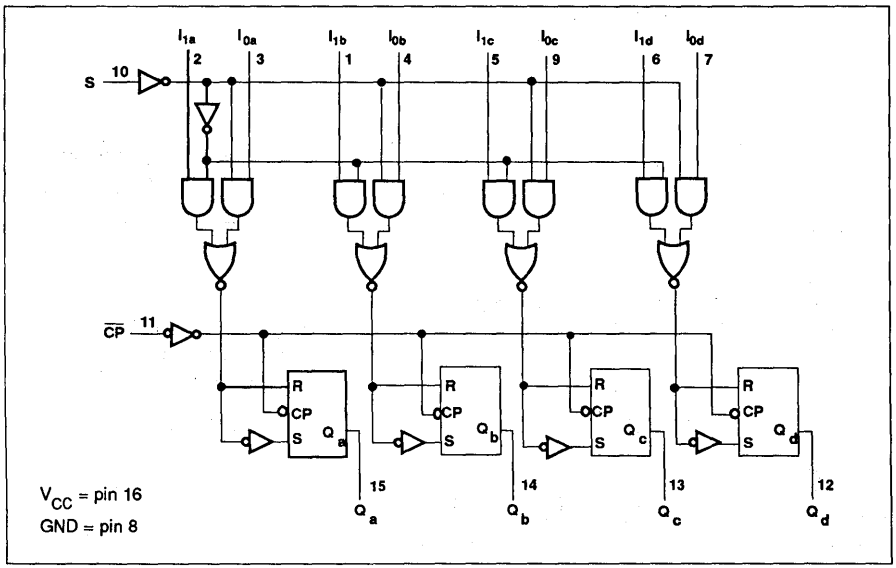


V_{CC} = pin 16
GND = pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT	OPERATING MODE
$\overline{CP}$	S	I_{0n}	I_{1n}	Q_n	
↓	l	l	X	L	Load source "0"
↓	l	h	X	H	
↓	h	X	l	L	Load source "1"
↓	h	X	h	H	

H = High voltage level
h = High voltage level one set-up time prior to the High-to Low clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low clock transition
X = Don't care
↓ = High-to-Low clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current(total)	I_{CCH}	V_{CC} = MAX			30	40	mA
		I_{CCL}				32	40	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

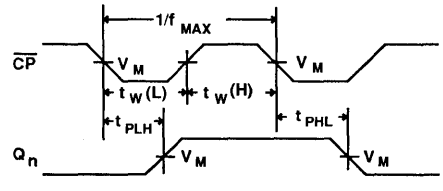
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	110	115		150		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_n	Waveform 1	4.0 4.5	5.5 6.5	7.5 8.5	4.0 4.5	9.0 9.5	ns

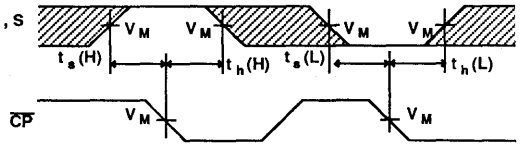
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I_{0n}, I_{1n} to $\overline{CP}$	Waveform 2	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I_{0n}, I_{1n} to $\overline{CP}$	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S to $\overline{CP}$	Waveform 2	6.0 5.0			7.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S to $\overline{CP}$	Waveform 2	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse width, High or Low	Waveform 1	5.0 5.0			5.0 7.0		ns

AC WAVEFORMS



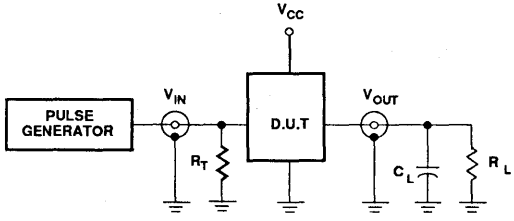
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



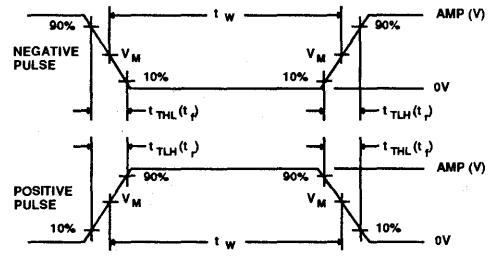
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F299
Register

8-Bit Universal Shift/Storage Register(3-State)
Product Specification

FAST Products

FEATURES

- **Common parallel I/O for reduced pin count**
- **Additional serial inputs and outputs for expansion**
- **Four operating modes: Shift left, shift right, load and store**
- **3-state outputs for bus oriented applications**

DESCRIPTION

The 74F299 is an 8-bit universal shift / storage register with 3-state outputs. Four modes of operation are possible: Hold (store), shift left, shift right and parallel load. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. A separate active-Low Master Reset is used to reset the register.

The 74F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Function Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting on longer words. A Low signal on $\overline{MR}$ overrides the Select and and CP input and resets the flip-flops.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F299	115 MHz	58mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F299N
20-Pin Plastic SOL	N74F299D

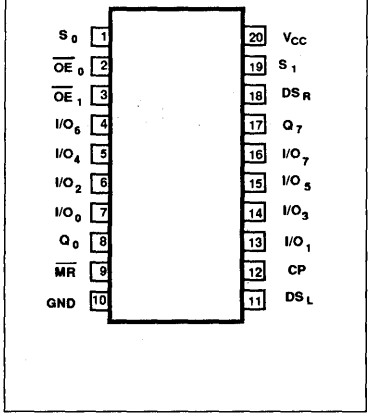
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
DS_R	Serial data input for right shift	1.0/1.0	20µA/0.6mA
DS_L	Serial data input for left shift	1.0/1.0	20µA/0.6mA
S_0, S_1	Mode Select inputs	1.0/2.0	20µA/1.2mA
CP	Clock Pulse input (Active rising edge)	1.0/1.0	20 A/0.6mA
$\overline{MR}$	Asynchronous Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
Q_0, Q_7	Serial outputs	50/33	1.0mA/20mA
I/O_n	Multiplexed parallel data inputs or	3.5/1.0	70µA/0.6mA
	3-state parallel outputs	150/40	3.0mA/24mA

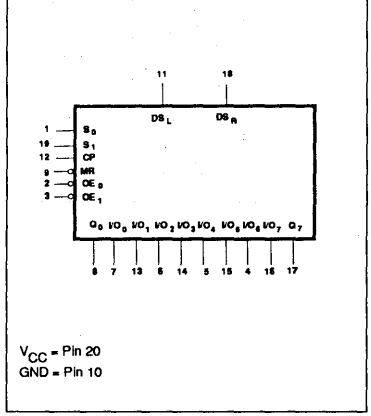
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended set up and hold times, relative to the rising edge of clock are observed. A High signal on either $\overline{OE}_0$ or $\overline{OE}_1$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by High signals on both S_0 and S_1 in preparation for a parallel load operation.

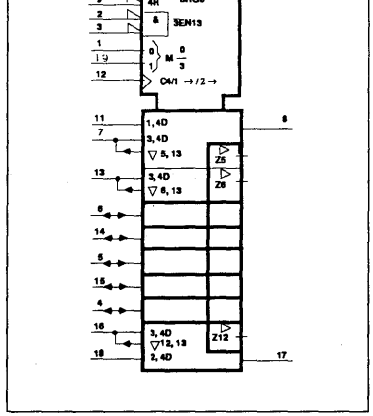
PIN CONFIGURATION



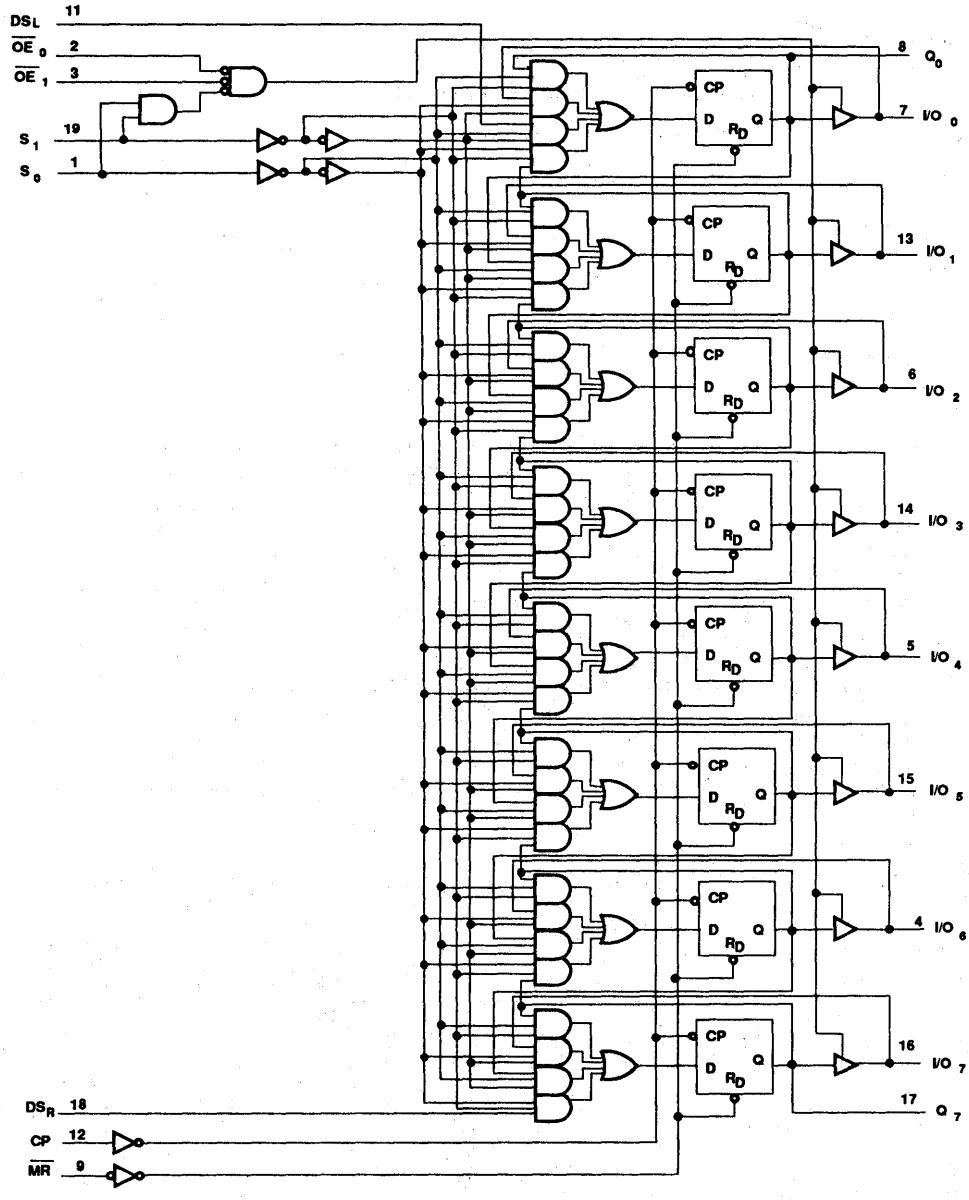
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE

INPUTS					OPERATING MODE
$\overline{OE}_n$	$\overline{MR}$	S_1	S_0	CP	
L	L	X	X	X	Asynchronous Reset; Q_0-Q_7=Low
L	H	H	H	↑	Parallel load ; $I/O_n \rightarrow Q_n$ (I/O_n outputs disabled)
L	H	L	H	↑	Shift right ; $DS_R \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
L	H	H	L	↑	Shift left ; $DS_L \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
L	H	L	L	X	Hold
H	X	X	X	X	Outputs in High Z

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	Q_0, Q_7	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_0, Q_7			-1	mA
		I/O_n			-3	mA
I_{OL}	Low-level output current	Q_0, Q_7			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	Q_0, Q_7	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = MAX, V_I = 7.0V					100	µA
		I/O_n	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	except I/O_n	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	S_0, S_1	V_{CC} = MAX, V_I = 0.5V					-1.2	mA
		others						-0.6	mA
I_{IH}+I_{OZH}	Off-state current High level voltage applied	I/O_n only	V_{CC} = MAX, V_I = 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state current Low-level voltage applied	I/O_n only	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				55	80	mA
		I_{CCL}					70	90	mA
		I_{CCZ}					65	85	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

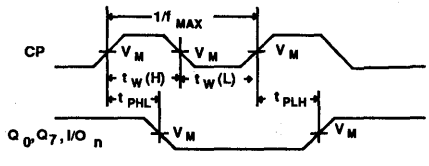
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	I/O	Waveform 1	70	100		70		MHz
		Q_n		85	115		85		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_0 or Q_7		Waveform 1	4.0 4.5	5.0 6.0	7.5 8.0	3.5 4.5	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n		Waveform 1	4.0 4.0	6.0 6.5	9.0 9.0	4.0 4.0	10.0 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_0 or Q_7		Waveform 2	5.5	7.5	9.5	5.5	10.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/O_n		Waveform 2	5.5	7.5	10.0	5.5	10.5	ns
t_{PZH} t_{PZL}	Output Enable time Sn, $\overline{OE}$ to I/O_n		Waveform 4 Waveform 5	3.5 4.0	6.0 7.5	8.0 10.0	3.5 4.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time Sn, $\overline{OE}$ to I/O_n		Waveform 4 Waveform 5	2.5 1.5	4.5 2.5	7.0 5.5	2.5 1.5	8.0 6.5	ns

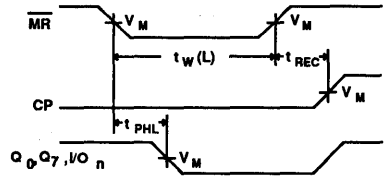
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_0 or S_1 to CP	Waveform 3	6.5 6.5			7.5 7.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_0 or S_1 to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n, DS_L or DS_R to CP	Waveform 3	3.5 3.5			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n, DS_L or DS_R to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	5.0 4.5			5.0 4.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	4.0			4.0		ns

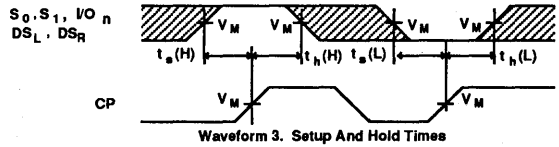
AC WAVEFORMS



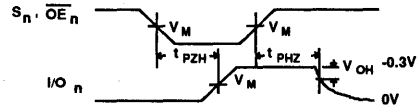
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



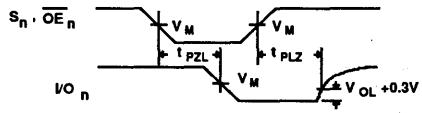
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 3. Setup And Hold Times



Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

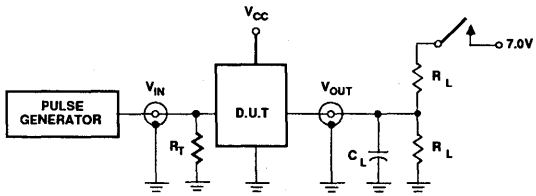


Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

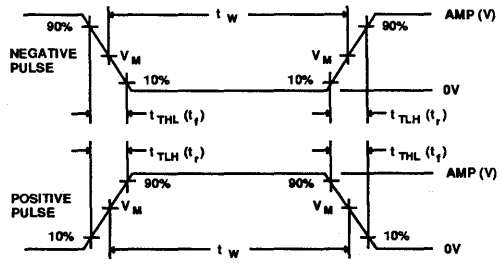
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F322
Register

8-Bit Serial/Parallel Register With Sign Extend (3-State)

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F322	125 MHz	60mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F322N
20-Pin Plastic SOL	N74F322D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0, D_1	Serial data inputs	1.0/1.0	20µA/0.6mA
S	Serial data select input	1.0/2.0	20µA/1.2mA
$\overline{SE}$	Sign Extend input	1.0/3.0	20µA/1.8mA
CP	Clock Pulse input (Active rising edge)	1.0/1.0	20µA/0.6mA
S/$\overline{P}$	Serial (High) or Parallel (Low) mode control input	1.0/1.0	20µA/0.6mA
$\overline{RE}$	Register Enable input (active-Low)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Asynchronous Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
Q_7	Bi-state serial output	50/33	1.0mA/20mA
I/O_n	Multiplexed parallel data inputs or	3.5/1.0	70µA/0.6mA
	3-state parallel outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

FAST Products

FEATURES

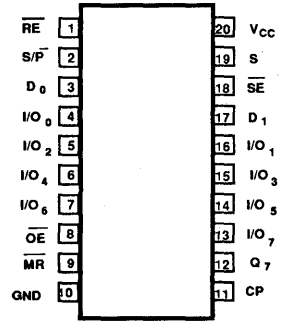
- **Multiplexed parallel I/O ports**
- **Separate serial input and output**
- **Sign extend function**
- **3-state outputs for bus applications**
- **Direct Overriding Clear**

DESCRIPTION

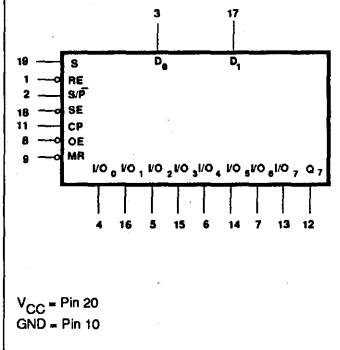
The 74F322 is an 8-bit shift register with provision for either serial or parallel loading and with 3-state parallel outputs plus a bi-state serial output. Parallel data inputs and outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store), shift right with serial entry, shift right with sign extend, and parallel load. An asynchronous Master Reset ($\overline{MR}$) input overrides clocked operation and clears the register.

The 'F322 contains eight D-type edge triggered flip-flops and the interstage gating required to perform right shift and the intrastage gating necessary for hold and synchronous parallel load operations. A Low signal on $\overline{RE}$ enables shifting or parallel loading, while a High signal enables the hold mode. A High signal on S/$\overline{P}$ enables shift right, while a Low signal disables the 3-state output buffers and enables parallel loading. In the shift right mode a High signal on $\overline{SE}$ enables serial entry from either D_0 or D_1, as determined by the S input. A Low signal on $\overline{SE}$ enables shift right but Q_7 reloads its contents thus performing the sign extend function. A High signal on $\overline{OE}$ disables the 3-state output buffers, regardless of the other control inputs. In this condition the shifting and loading operations can still be performed.

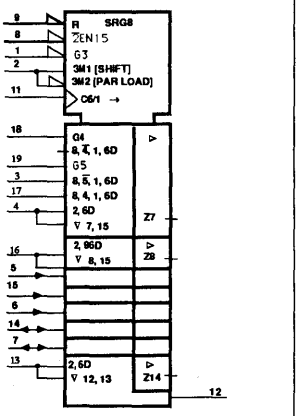
PIN CONFIGURATION



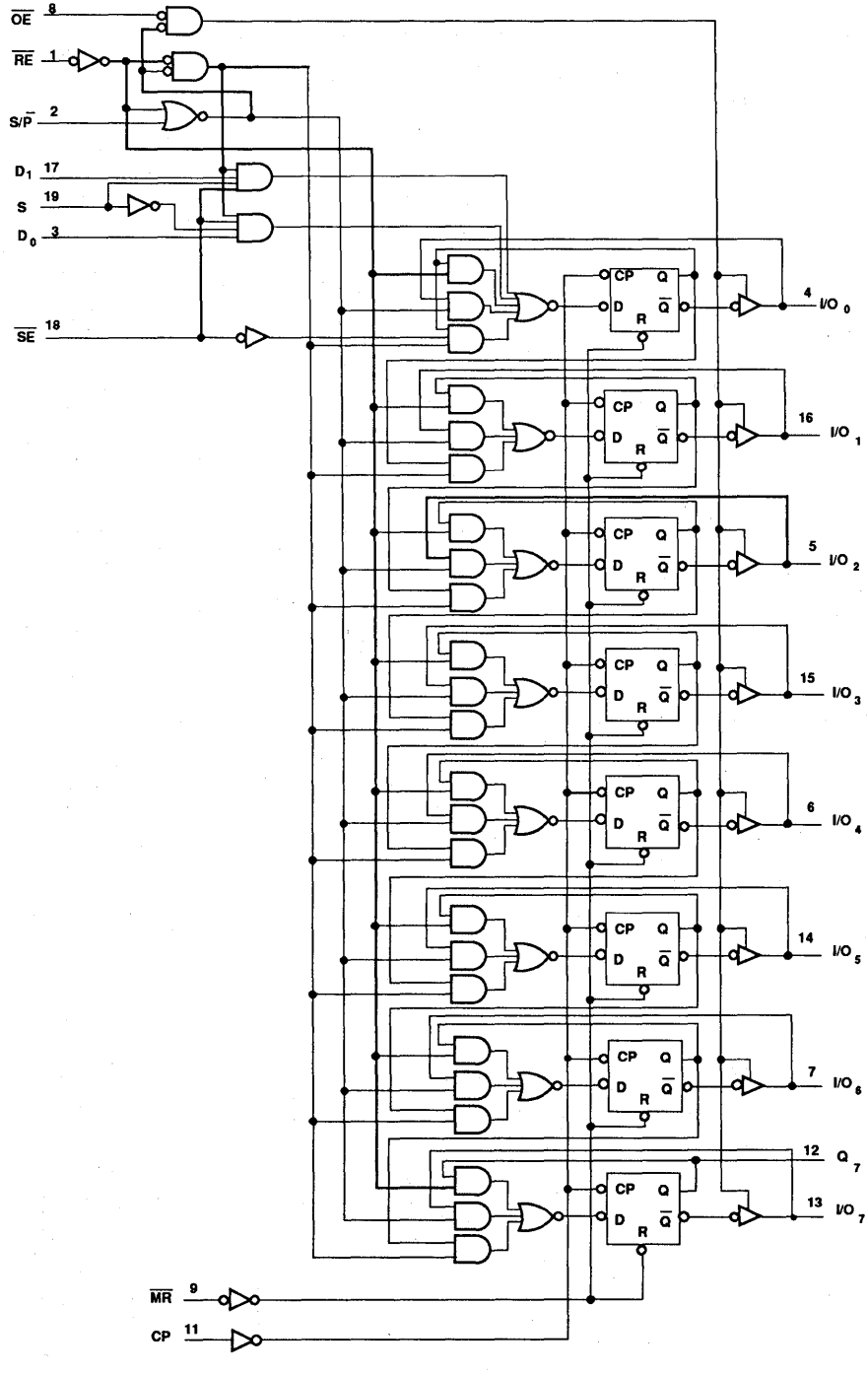
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE

INPUTS							OUTPUTS									OPERATING MODE
$\overline{MR}$	$\overline{RE}$	S/$\overline{P}$	$\overline{SE}$	S	$\overline{OE}$*	CP	I/O_0	I/O_1	I/O_2	I/O_3	I/O_4	I/O_5	I/O_6	I/O_7	Q_7	
L	H	X	X	X	L	X	L	L	L	L	L	L	L	L	L	Clear
L	X	H	X	X	L	X	L	L	L	L	L	L	L	L	L	
H	L	L	X	X	X	↑	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_7	Parallel load
H	L	H	H	L	L	↑	D_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_6	Shift right
H	L	H	H	H	L	↑	D_1	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_6	
H	L	H	L	X	L	↑	O_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_6	Sign extend
H	H	X	X	X	L	X	NC	NC	NC	NC	NC	NC	NC	NC	NC	Hold
X	L	L	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	NC	3-State
X	X	X	X	X	H	↕	Z	Z	Z	Z	Z	Z	Z	Z	NC	

H = High voltage level
L = Low voltage level
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
I_0-I_7 = The level of the steady state input at the respective I/O terminal is loaded into the flip-flop while the flip-flop outputs (except Q_7) are isolated from the I/O terminal.
D_0-D_7 = The level of the steady state inputs to the serial multiplexer input.
O_0-O_7 = The level of the respective Q_n flip-flop prior to the last clock Low-to-High transition.
* = When the input is High, all I/O terminals are at the high impedance state, sequential operation or clearing of the register is not affected.
↕ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	Q_7	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_7			-1	mA
		I/O_n			-3	mA
I_{OL}	Low-level output current	Q_7			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	Q_7	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}		0.38	0.55	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = MAX, V_I = 7.0V					100	µA
		I/O_n	V_{CC} = MAX, V_I = 5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	$\overline{SE}$	V_{CC} = MAX, V_I = 0.5V					-1.8	mA
		S						-1.2	mA
		others						-0.6	mA
$I_{IH}+I_{OZH}$	Off-state output current High-level voltage applied		V_{CC} = MAX, V_I = 2.7V					70	µA
$I_{IL}+I_{OZL}$	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				50	75	mA
		I_{CCL}					60	90	mA
		I_{CCZ}					65	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

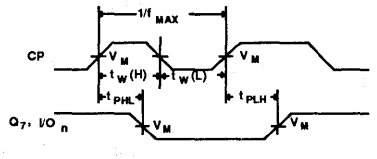
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	110	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	4.0 4.5	6.0 7.0	9.0 9.5	4.0 4.5	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_7	Waveform 1	4.5 5.0	6.5 6.5	9.0 9.0	4.5 5.0	10.0 9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/O_n	Waveform 2	5.0	6.5	9.5	4.5	10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_7	Waveform 2	5.0	6.5	9.5	4.5	10.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to I/O_n	Waveform 4 Waveform 5	3.0 5.5	5.0 7.5	8.0 10.5	3.0 5.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to I/O_n	Waveform 4 Waveform 5	2.0 1.0	4.0 2.5	6.5 5.5	2.0 1.0	7.5 6.0	ns
t_{PZH} t_{PZL}	Output Enable time $S/\overline{P}$ to I/O_n	Waveform 4 Waveform 5	4.0 6.0	6.0 8.0	9.0 11.0	3.5 5.5	10.0 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $S/\overline{P}$ to I/O_n	Waveform 4 Waveform 5	4.0 2.0	6.0 4.0	9.0 7.0	3.5 2.0	10.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{RE}$ to I/O_n	Waveform 4 Waveform 5	8.0 9.0	9.5 11.0	12.5 14.0	7.0 8.0	14.0 16.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{RE}$ to I/O_n	Waveform 4 Waveform 5	6.5 4.5	8.5 6.5	11.5 9.5	5.5 4.0	13.0 10.5	ns

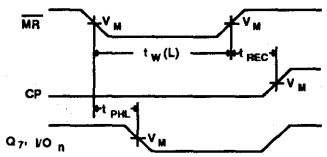
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{RE}$ to CP	Waveform 3	8.0 12.5			9.5 14.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{RE}$ to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_0, D_1 or I/O_n to CP	Waveform 3	4.0 4.5			6.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_0, D_1 or I/O_n to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{SE}$ to CP	Waveform 3	5.5 5.0			7.0 5.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{SE}$ to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S/$\overline{P}$ to CP	Waveform 3	10.5 9.5			11.0 10.5		ns
$t_s(H)$ t_sL)	Setup time, High or Low S to CP	Waveform 3	4.0 8.5			4.5 9.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S or S/$\overline{P}$ to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 3	5.0 5.0			5.0 5.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 3	5.0			5.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 2	4.0			4.5		ns

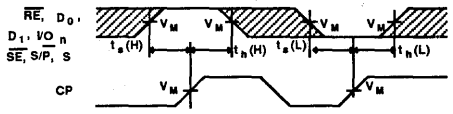
AC WAVEFORMS



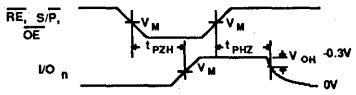
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



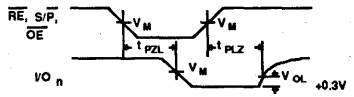
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 3. Data Setup And Hold Times



Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

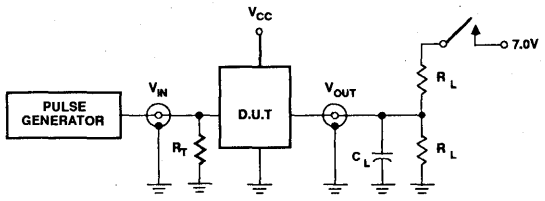


Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

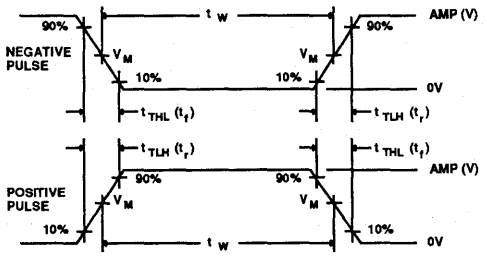
NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F323

Register

FAST Products

8-Bit Universal Shift/Storage Register With Synchronous Reset and Common I/O pins (3-State)

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F323	115 MHz	55mA

FEATURES

- **Common parallel I/O for reduced pin count**
- **Additional serial inputs and outputs for expansion**
- **Four operating modes: Shift left, shift right, load and store**
- **3-state outputs for bus oriented applications**

DESCRIPTION

The 74F323 is an 8-bit universal shift /storage register with 3-state outputs.Its function is similar to the 74F299 with the exception of synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin counts. Separate serial inputs and outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. Four modes of operation are possible: Hold (store), shift left, shift right and parallel load.

The 74F323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operations is determined by $S_0$and S_1, as shown in the Function Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words. A Low signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of clock. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended set up and hold times, relative to the rising edge of clock are observed. A high signal on either $\overline{OE}_0$ or $\overline{OE}_1$disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by High signals on both S_0 and S_1 in preparation for a parallel load operation.

ORDERING INFORMATION

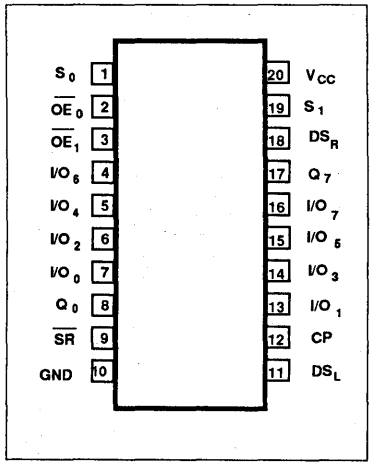
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F323N
20-Pin Plastic SOL	N74F323D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

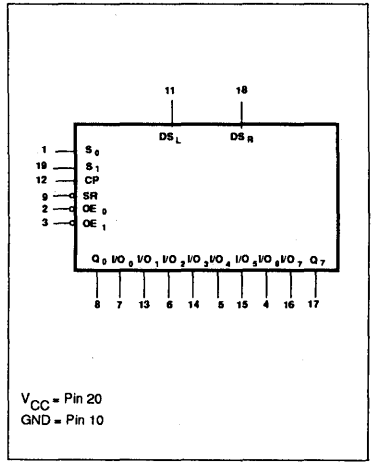
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
DS_R	Serial data input for right shift	1.0/1.0	20µA/0.6mA
DS_L	Serial data input for left shift	1.0/1.0	20µA/0.6mA
S_0 ,S_1	Mode select inputs	1.0/2.0	20µA/1.2mA
CP	Clock Pulse input (Active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{SR}$	Synchronous Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}_0$,$\overline{OE}_1$	Output enable input (active Low)	1.0/1.0	20µA/0.6mA
Q_0 ,Q_7	Serial outputs	50/33	20µA/20mA
I/O_n	Multiplexed parallel data inputs or	3.5/1.0	70µA/0.6mA
	3-state parallel outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

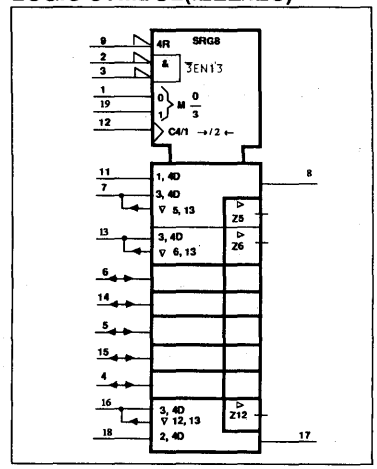
PIN CONFIGURATION



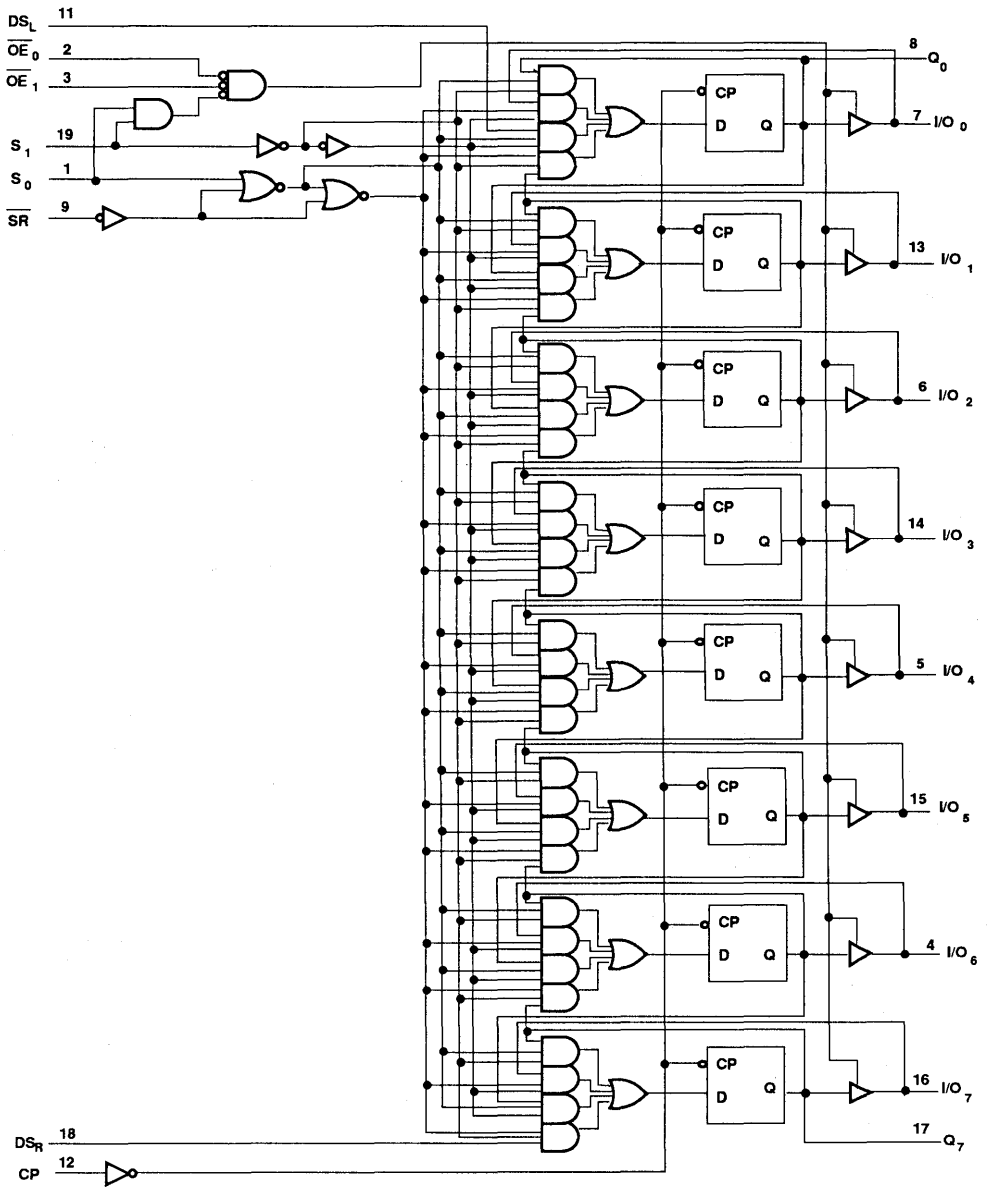
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE

INPUTS					OPERATING MODE
$\overline{OE}_n$	$\overline{SR}$	S_1	S_0	CP	
L	L	X	X	↑	Synchronous Reset; Q_0-Q_7=Low
L	H	H	H	↑	Parallel load ; $I/O_n \rightarrow Q_n$
L	H	L	H	↑	Shift right ; $DS_R \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc
L	H	H	L	↑	Shift left ; $DS_L \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
L	H	L	L	X	Hold
H	X	X	X	X	Outputs disabled (3-state)

H = High voltage level
L = Low voltage level
NC = No change
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	Q_0, Q_7	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_0, Q_7			-1	mA
		I/O_n			-3	mA
I_{OL}	Low-level output current	Q_0, Q_7			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	Q_0, Q_7	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OH}=-3mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = MAX, V_I = 7.0V					100	µA
		I/O_n	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	except I/O_n	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	S_0, S_1	V_{CC} = MAX, V_I = 0.5V					-1.2	mA
		others						-0.6	mA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied	I/O_n only	V_{CC} = MAX, V_O= 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied	I/O_n only	V_{CC} = MAX, V_O= 0.5V					-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				55	75	mA
		I_{CCL}					65	90	mA
		I_{CCZ}					55	85	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

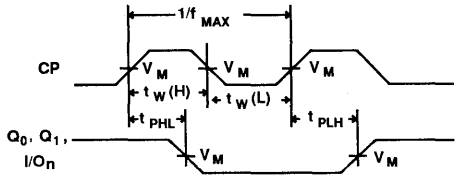
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	I/O_n	Waveform 1	70	100		70		MHz
		Q_n		85	115		85		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_0 or Q_7		Waveform 1	4.0 3.5	6.0 6.0	8.5 8.5	4.0 4.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n		Waveform 1	4.0 5.0	6.0 6.5	9.0 9.5	4.0 5.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable time S_n, $\overline{OE}$ to I/O_n		Waveform 3 Waveform 4	3.5 4.0	6.0 8.0	9.0 11.0	3.5 4.0	10.0 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time S_n, $\overline{OE}$ to I/O_n		Waveform 3 Waveform 4	2.5 1.5	5.0 3.0	7.5 5.5	2.5 1.0	8.0 6.5	ns

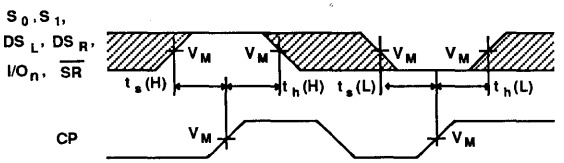
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_0 or S_1 to CP	Waveform 2	6.5 6.5			7.5 7.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_0 or S_1 to CP	Waveform 2	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n, DS_L or DS_R to CP	Waveform 2	3.5 3.5			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n, DS_L or DS_R to CP	Waveform 2	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{SR}$ to CP	Waveform 2	7.0 7.0			8.5 8.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{SR}$ to CP	Waveform 2	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	3.5 3.5			4.0 4.0		ns

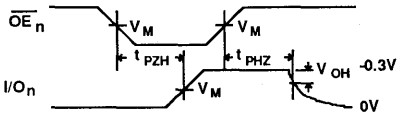
AC WAVEFORMS



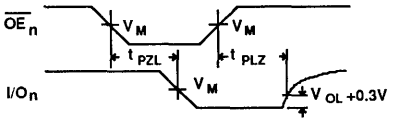
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data, Select and Reset Setup And Hold Times



Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level

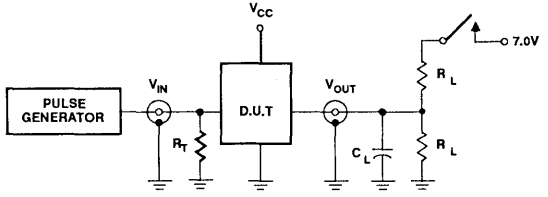


Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

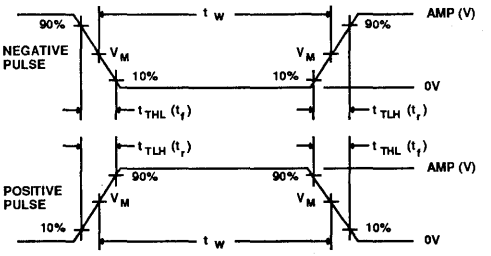
NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F350
Shifter

FAST Products

4-Bit Shifter
Product Specification

FEATURES

- **Shifts 4 bits of data to 0,1,2,3 places under control of two select lines**
- **3-state outputs for bus organized systems**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F350	5.2ns	24mA

DESCRIPTION

The 74F350 is a combination logic circuit that shifts a 4-bit word from 0 to 3 places. No clocking is required as with shift registers. The 'F350 can be used to shift any number of bits any number of places up or down by suitable interconnection. Shifting can be:

1. Logical-- with logic zeros filled in at either end of the shifting field.

2. Arithmetic-- where the sign bit is extended during a shift down.

3. End around-- where the data word forms a continuous loop.

The 3-state outputs are useful for bus interface applications or expansion to a larger number of shift positions in end around shifting. The active Low Output Enable ($\overline{OE}$) controls the state of the outputs. The outputs are in the high impedance "off" state when $\overline{OE}$ is High, and they are active when $\overline{OE}$ is Low.

ORDERING INFORMATION

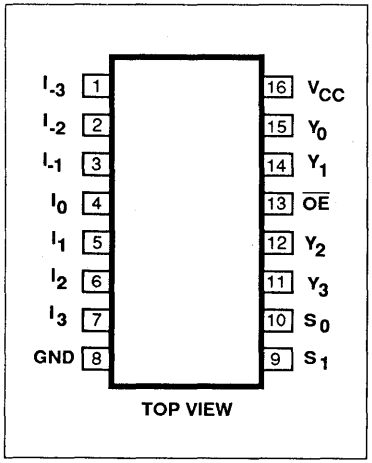
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F350N
16-Pin Plastic SO	N74F350D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{-n}, I_n	Data inputs	1.0/2.0	20µA/1.2mA
S_0, S_1	Select inputs (active Low)	1.0/2.0	20µA/1.2mA
$\overline{OE}$	Output Enable input (active Low)	1.0/2.0	20µA/1.2mA
Y_0 - Y_3	Data outputs	150/40	3.0mA/24mA

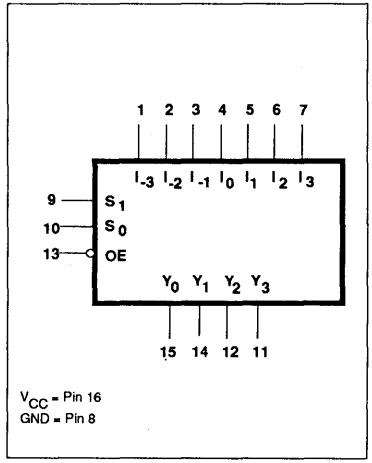
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



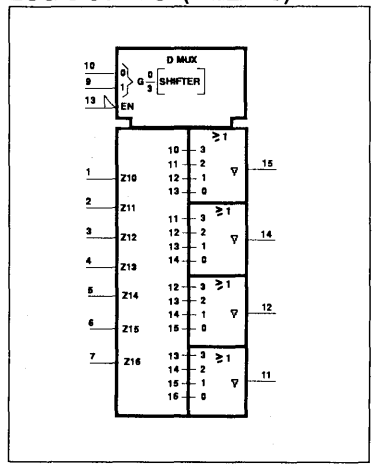
TOP VIEW

LOGIC SYMBOL

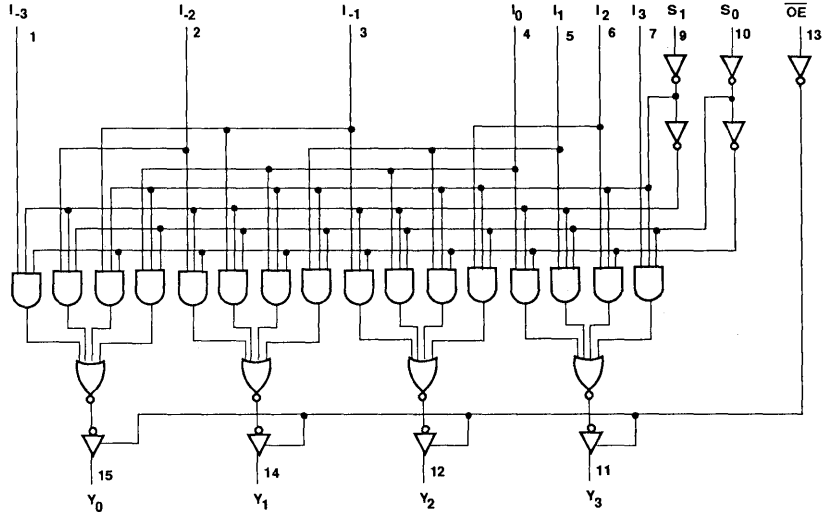


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



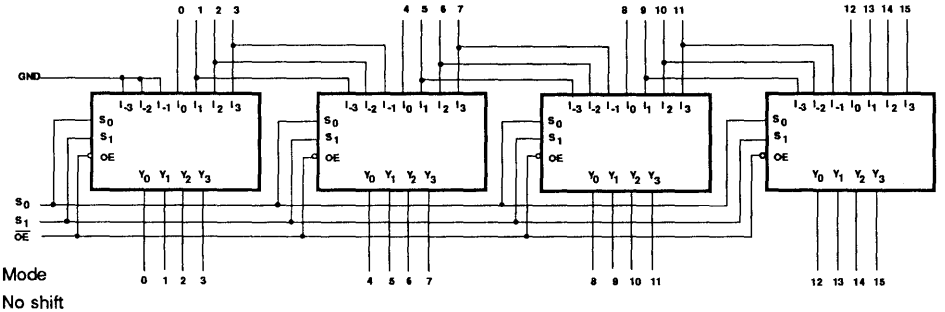
V_{CC}= pin 16
GND= Pin 8

FUNCTION TABLE

INPUTS										OUTPUTS			
$\overline{OE}$	S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D_3	D_2	D_1	D_0	X	X	X	D_3	D_2	D_1	D_0
L	L	H	X	D_2	D_1	D_0	D_{-1}	X	X	D_2	D_1	D_0	D_{-1}
L	H	L	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_1	D_0	D_{-1}	D_{-2}
L	H	H	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_0	D_{-1}	D_{-2}	D_{-3}

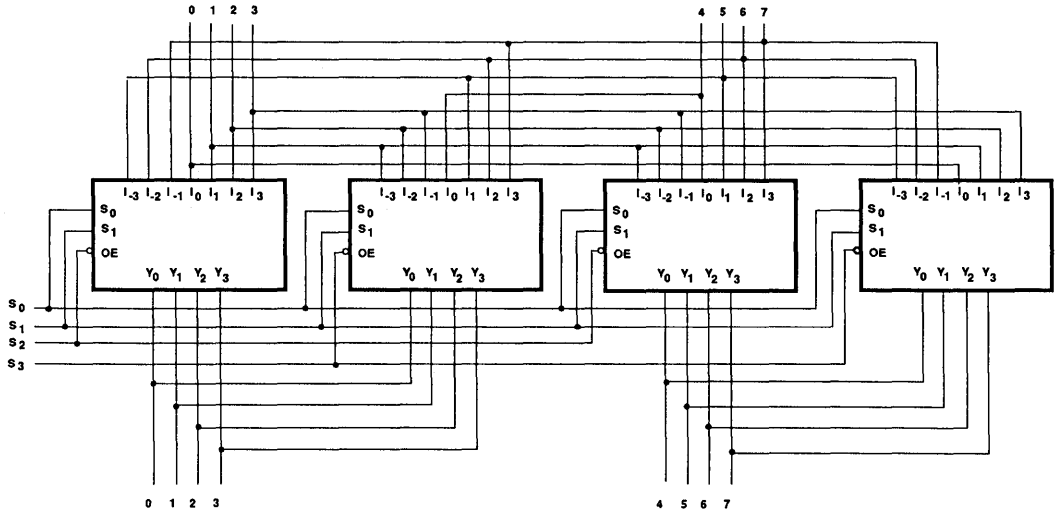
H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state
D_n = High or Low state of referenced I_n input

APPLICATION for 16-bit shift up 0,1,2, or 3 places



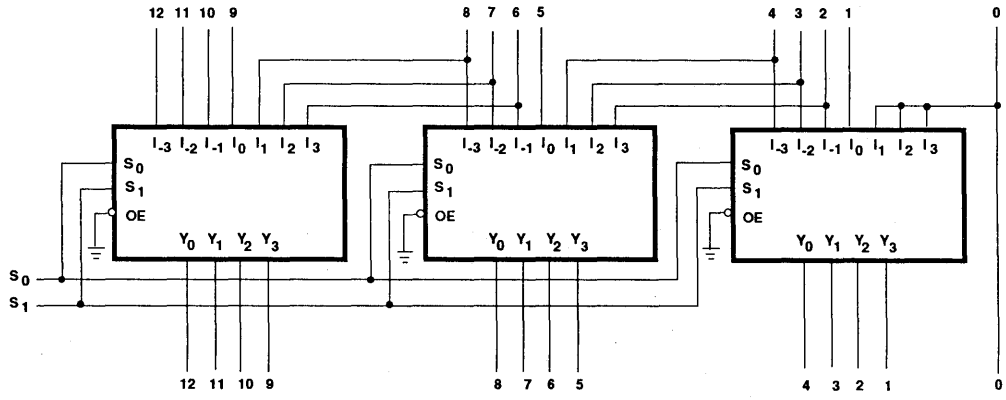
S_0	S_1	Mode
L	L	No shift
H	L	Shift 1 place
L	H	Shift 2 places
H	H	Shift 3 places

APPLICATION for 8-bit end around shift 0,1,2,3,4,5,6,7 places



S_2	S_1	S_0	Mode
L	L	L	No shift
L	L	H	Shift end around 1
L	H	L	Shift end around 2
L	H	H	Shift end around 3
H	L	L	Shift end around 4
H	L	H	Shift end around 5
H	H	L	Shift end around 6
H	H	H	Shift end around 7

APPLICATION for 13-bit two's complement scaler



S_1	S_0		Scale
L	L	+8	1/8
L	H	+4	1/4
H	L	+2	1/2
H	H	No change	1

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-1.2	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			22	35	mA
		I_{CCL}				26	41	mA
		I_{CCZ}				26	42	mA

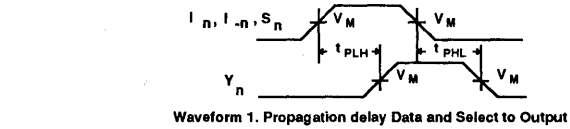
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

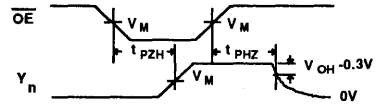
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	Waveform 1	3.0 2.5	4.5 4.0	6.0 5.5	3.0 2.5	7.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y_n	Waveform 1	4.0 3.0	7.8 6.5	10.0 8.5	4.0 3.0	11.0 9.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	2.5 4.0	5.0 7.0	7.0 9.0	2.5 4.0	8.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 2 Waveform 3	2.0 2.0	3.9 4.0	5.5 5.5	2.0 2.0	6.5 6.5	ns

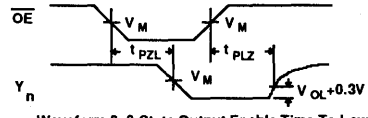
AC WAVEFORMS



Waveform 1. Propagation delay Data and Select to Output



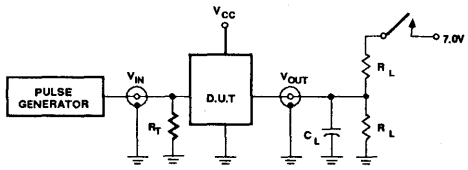
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

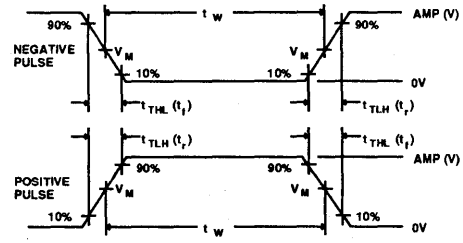
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F352
Multiplexer

FAST Products

Dual 4-Line to 1-Line Multiplexer

Product Specification

FEATURES
- **Inverting version of 'F153**
- **Separate enable for each multiplexer section**
- **Common select inputs**
- **See 'F353 for 3-state version**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F352	5.5ns	10mA

DESCRIPTION

The 74F352 is a dual 4-input multiplexer that can select 2 bits of data from up to four sources selected by common Select inputs (S_0,S_1). The two 4-input multiplexer circuits have individual active-Low Enables ($\overline{E}_a$,$\overline{E}_b$) which can be used to strobe the outputs independently. Outputs ($\overline{Y}_a$, $\overline{Y}_b$) are forced High when the corresponding Enables ($\overline{E}_a$,$\overline{E}_b$) are High.

The 'F352 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two common Select inputs.

ORDERING INFORMATION

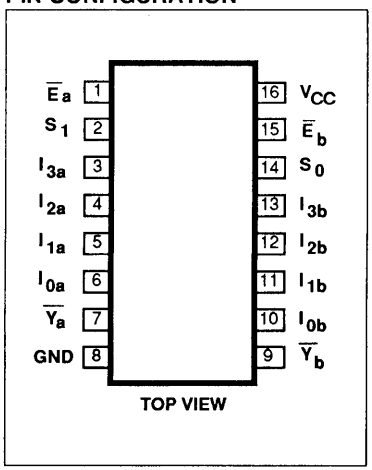
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F352N
16-Pin Plastic SO	N74F352D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

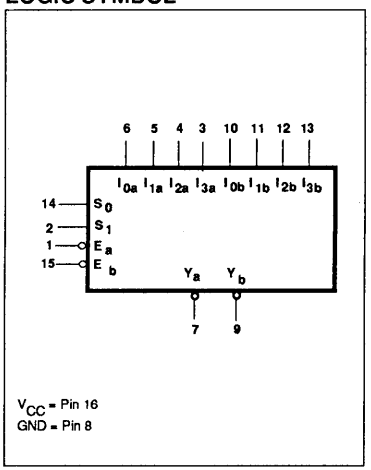
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0a}- I_{3a}	Port A data inputs	1.0/1.0	20µA/0.6mA
I_{0b}- I_{3b}	Port B data inputs	1.0/1.0	20µA/0.6mA
S_0, S_1	Common Select inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_a$	Port A Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{E}_b$	Port B Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{Y}_a$, $\overline{Y}_b$	Port A, B data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

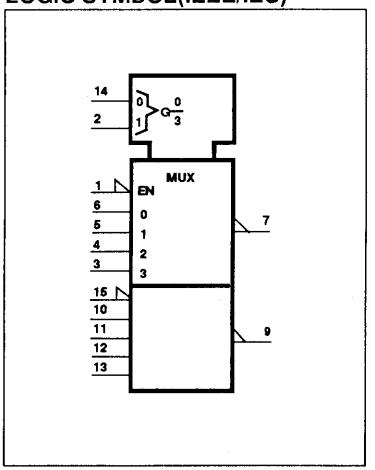
PIN CONFIGURATION



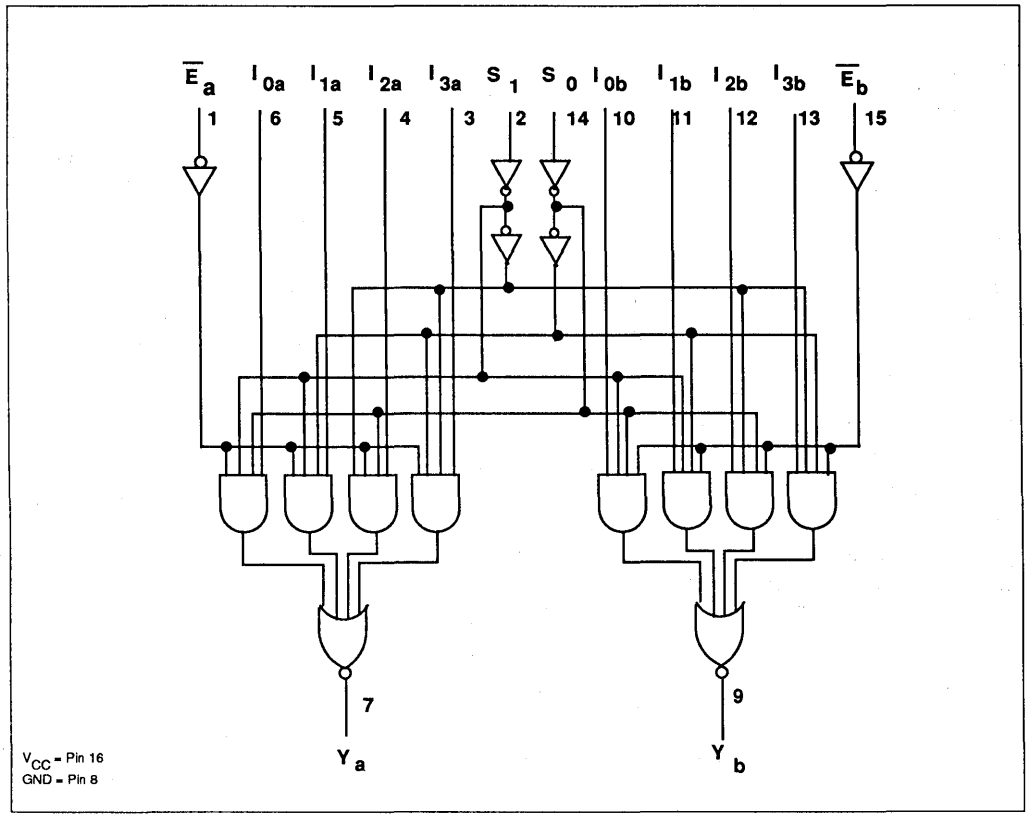
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUT
S_0	S_1	$\overline{E}_n$	I_{on}	I_{1n}	I_{2n}	I_{3n}	$\overline{Y}_n$
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{E}_n$=S_n=I_n=GND		8	14	mA
		I_{CCL}		$\overline{E}_n$=GND, S_n=I_n=4.5V		12	20	mA

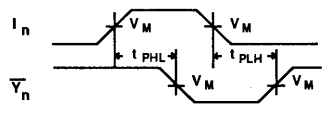
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

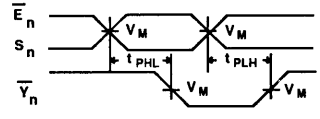
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	Waveform 1	2.5 1.5	5.0 3.0	7.0 4.5	2.0 1.0	8.0 5.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}_n$	Waveform 2	4.5 4.0	6.5 6.0	11.0 8.5	4.0 3.5	12.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to $\overline{Y}_n$	Waveform 2	2.5 3.5	5.0 6.0	6.5 8.0	2.0 3.0	7.0 8.5	ns

AC WAVEFORMS



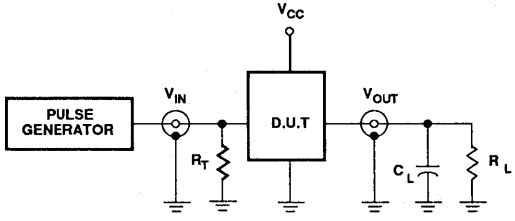
Waveform 1. Propagation Delay, Select to Output



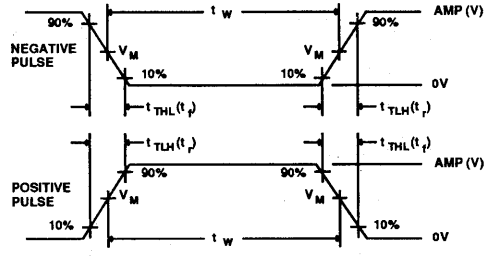
Waveform 2. Propagation Delay, Enable and Select to Output

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F353
Multiplexer

FAST Products

Dual 4-Input Multiplexer (3-State)

Product Specification

FEATURES
- **Inverting version of 'F253**
- **3-state outputs for bus interface and multiplex expansion**
- **Common select inputs**
- **Separate Output Enable inputs**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F353	6.0ns	11mA

DESCRIPTION

The 74F353 has two identical 4-input multiplexers with 3-state outputs which select two bits from four sources selected by common Select inputs (S_0,S_1). When the individual Output Enable ($\overline{OE}_a$,$\overline{OE}_b$) inputs of the 4-input multiplexers are High, the outputs are forced to a high impedance (Hi-Z) state.

The 'F353 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two common Select inputs.

To avoid exceeding the maximum current ratings when the outputs of the 3-state devices are tied together, all but one device must be in the high-impedance state. Therefore, only one Output Enable must be active at a time.

ORDERING INFORMATION

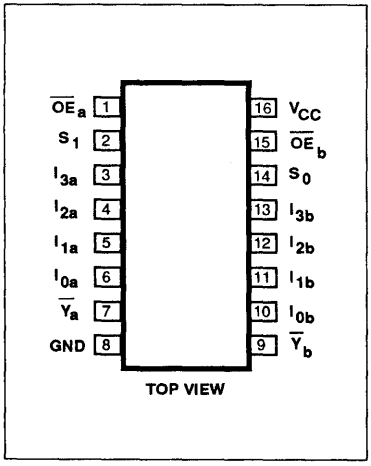
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F353N
16-Pin Plastic SO	N74F353D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0a}- I_{3a}	Port A data inputs	1.0/1.0	20µA/0.6mA
I_{0b}- I_{3b}	Port B data inputs	1.0/1.0	20µA/0.6mA
S_0, S_1	Common Select inputs	1.0/1.0	20µA/0.6mA
$\overline{OE}_a$	Port A Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}_b$	Port B Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{Y}_a$, $\overline{Y}_b$	3-state outputs	150/40	3mA/24mA

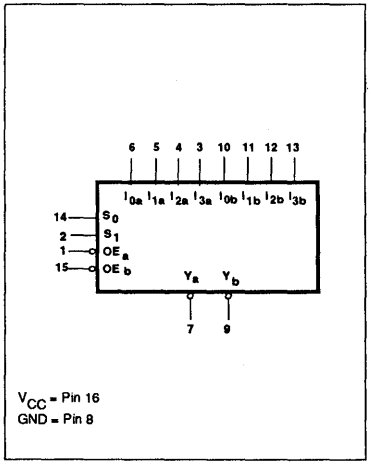
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



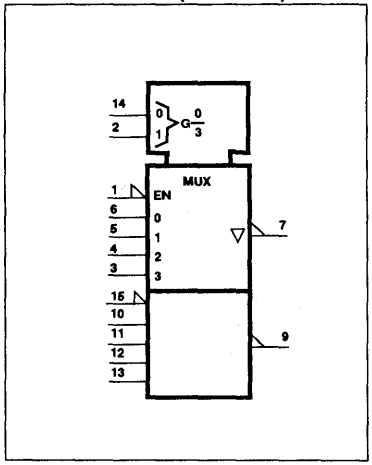
TOP VIEW

LOGIC SYMBOL



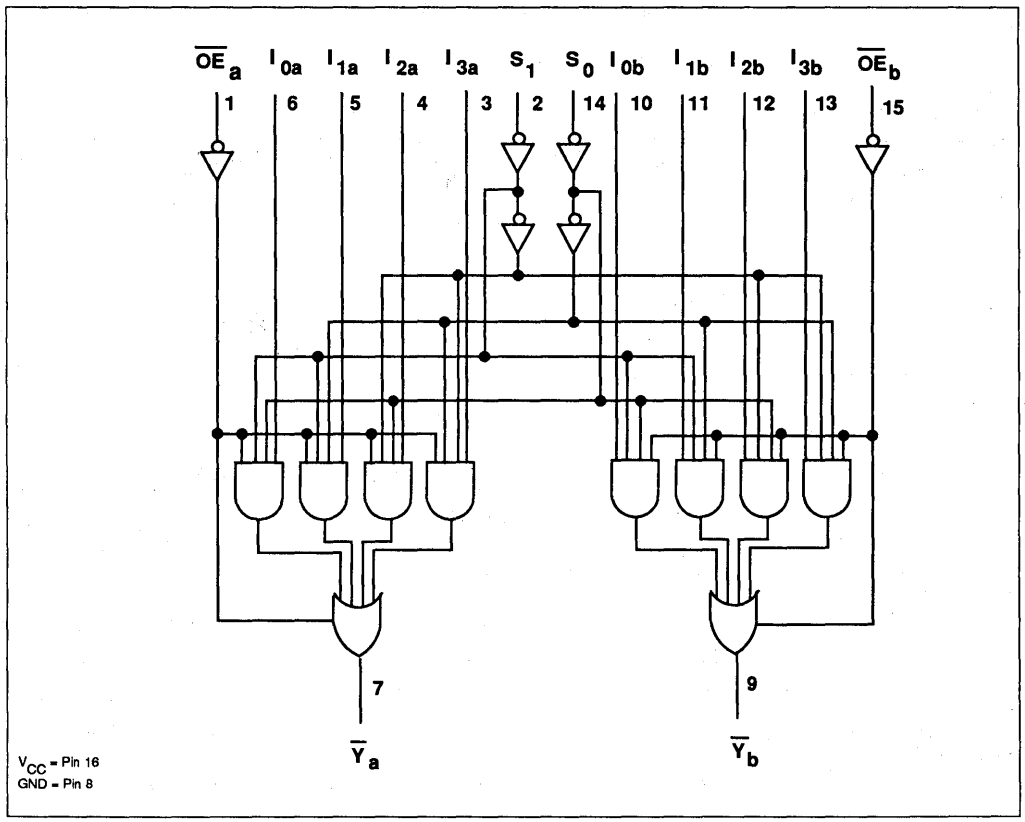
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



853-0103-95946

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	$\overline{Y}$
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX	$\overline{OE}_n$=S_n=I_n=GND		9	14	mA
	Supply current (total) I_{CCL}	V_{CC} = MAX	$\overline{OE}_n$=S_n=GND, I_n=4.5V		11	20	mA
	Supply current (total) I_{CCZ}	V_{CC} = MAX	$\overline{OE}_n$=4.5V, S_n=I_n=GND		13	23	mA

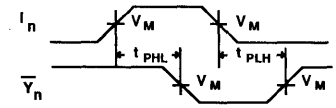
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

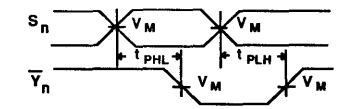
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	Waveform 1	3.0 1.5	5.0 3.0	7.0 5.0	3.0 1.0	8.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}_n$	Waveform 2	5.0 3.0	9.0 6.0	12.0 8.5	4.5 3.0	12.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 3 Waveform 4	4.0 4.0	6.0 6.5	8.0 8.0	3.5 3.5	9.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 3 Waveform 4	2.5 1.5	4.0 2.5	5.5 6.0	2.0 1.5	6.0 7.0	ns

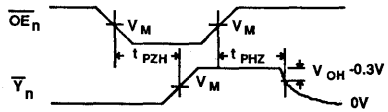
AC WAVEFORMS



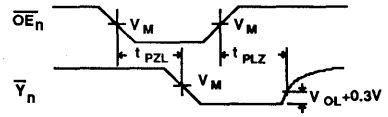
Waveform 1. Propagation Delay, Data to Output



Waveform 2. Propagation Delay, Select to Output



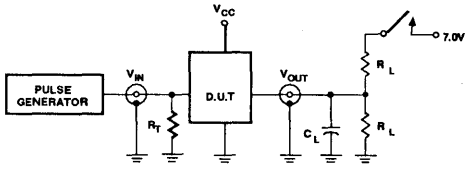
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

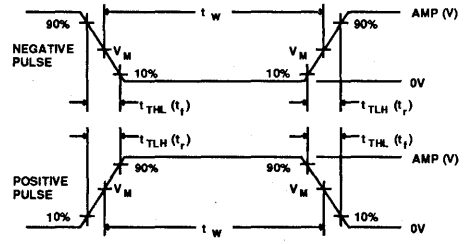
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F365, 74F366 74F367, 74F368 Buffers/Drivers

FAST Products

'F365, 'F367 Hex Buffer/Driver (3-State)
'F366, 'F368 Hex Inverter Buffer/Driver (3-State)
Product Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **High speed**
- **Bus oriented**
- **3-state buffer outputs sink 64mA**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F365, 74F367	5.0ns	36mA
74F366, 74F368	5.0ns	33mA

ORDERING INFORMATION

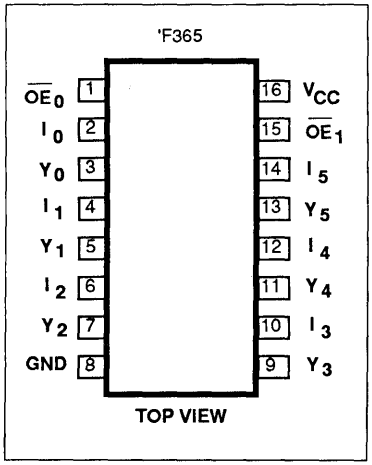
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F365N, N74F366N, N74F367N, N74F368N
16-Pin Plastic SO	N74F365D, N74F366D, N74F367D, N74F368D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

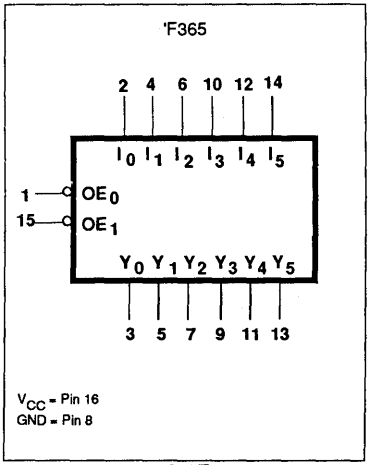
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0-I_5	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_0$, $\overline{OE}_1$	Output enable inputs (active Low)	1.0/0.033	20μA/20μA
Y_0- Y_5, $\overline{Y}_0$- $\overline{Y}_5$	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

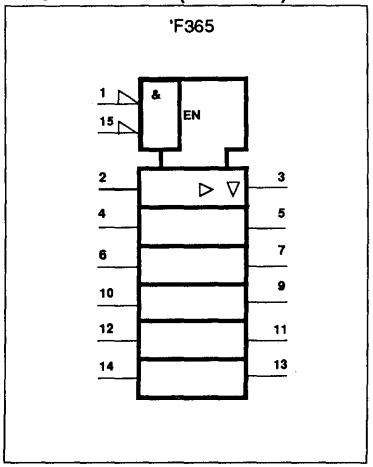
PIN CONFIGURATION



LOGIC SYMBOL

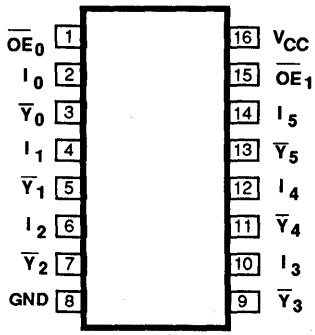


LOGIC SYMBOL(IEEE/IEC)



PIN CONFIGURATION

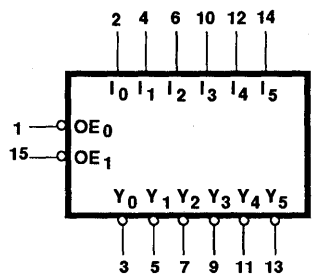
'F366



TOP VIEW

LOGIC SYMBOL

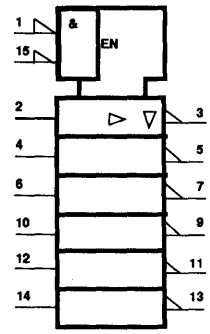
'F366



V_{CC} = Pin 16
GND = Pin 8

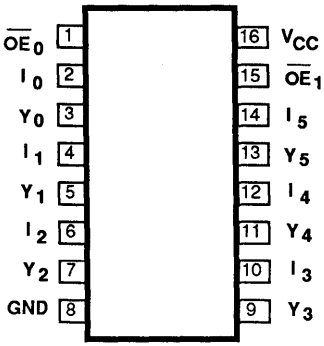
LOGIC SYMBOL(IEEE/IEC)

'F366



PIN CONFIGURATION

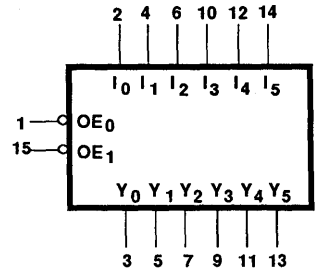
'F367



TOP VIEW

LOGIC SYMBOL

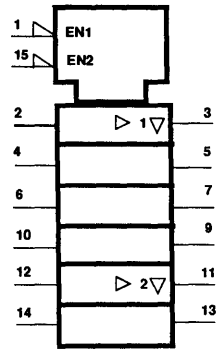
'F367



V_{CC} = Pin 16
GND = Pin 8

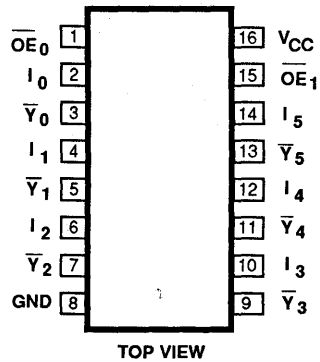
LOGIC SYMBOL(IEEE/IEC)

'F367



PIN CONFIGURATION

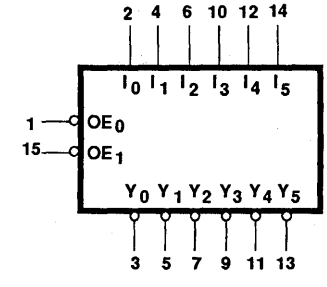
'F368



TOP VIEW

LOGIC SYMBOL

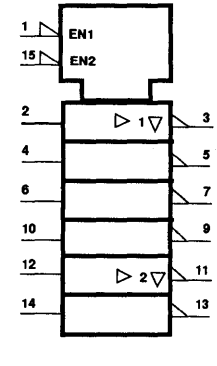
'F368



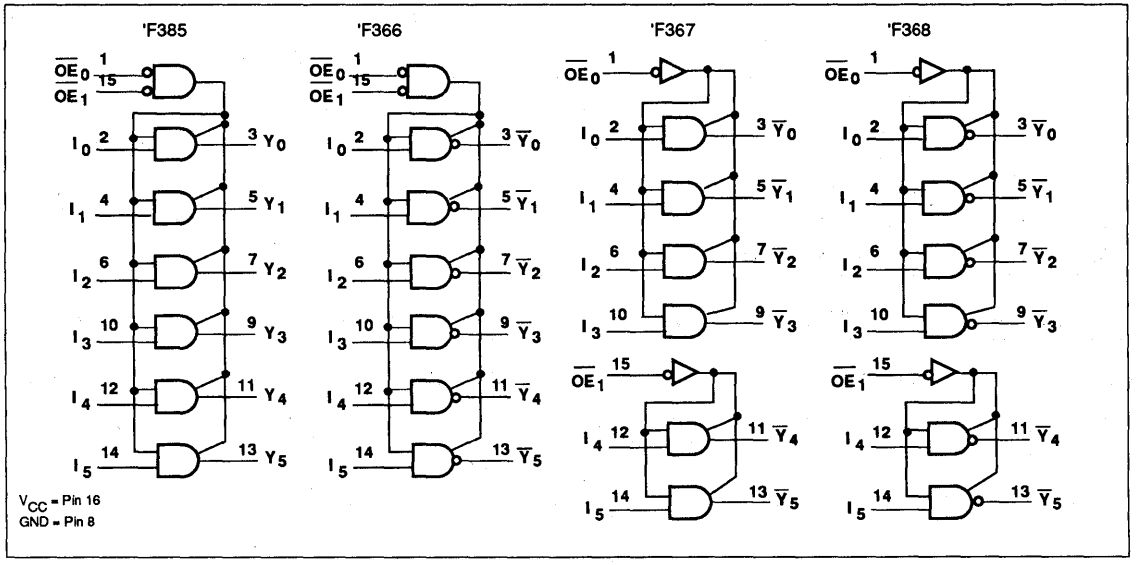
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)

'F368



LOGIC DIAGRAM



FUNCTION TABLE for 'F365 and 'F366

INPUTS			OUTPUTS	
$\overline{OE}_0$	$\overline{OE}_1$	I_n	Y_n	$\overline{Y}_n$
L	L	L	L	H
L	L	H	H	L
X	H	X	Z	Z
H	X	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

FUNCTION TABLE for 'F367 and 'F368

INPUTS		OUTPUTS	
$\overline{OE}_n$	I_n	Y_n	$\overline{Y}_n$
L	L	L	H
L	H	H	L
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

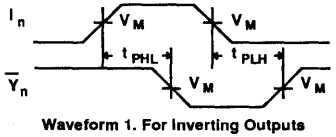
SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.7	3.3		V
				V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-15mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}			0.55	V
						±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F365 'F367	I_{CCH}	V_{CC} = MAX				25	35	mA
			I_{CCL}					47	62	mA
			I_{CCZ}					35	48	mA
		'F366 'F368	I_{CCH}	V_{CC} = MAX				18	25	mA
			I_{CCL}					47	62	mA
			I_{CCZ}					35	48	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

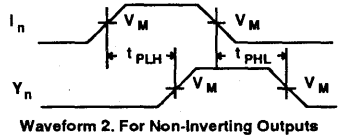
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	'F366, 'F368	Waveform 1	3.0 2.0	5.0 3.0	6.5 5.0	3.0 1.5	7.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	'F365, 'F367	Waveform 2	2.5 2.5	4.5 5.5	6.5 7.0	2.0 2.0	7.0 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	'F365, 'F366	Waveform 3 Waveform 4	2.5 2.5	6.5 6.0	9.5 9.0	2.5 2.5	10.0 9.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	'F367, 'F368	Waveform 3 Waveform 4	3.0 3.0	5.5 6.5	7.5 8.5	3.0 3.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.5 4.0	6.5 6.5	2.0 2.0	7.0 7.0	ns

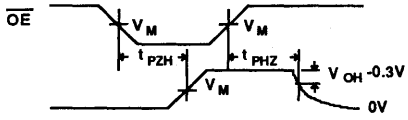
AC WAVEFORMS



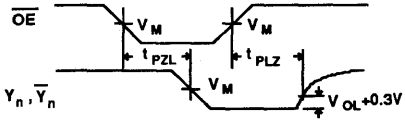
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



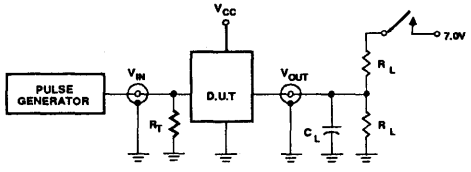
Waveform 3. 3-State Output Enable Time To High Level Y_n, $\overline{Y}_n$ And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

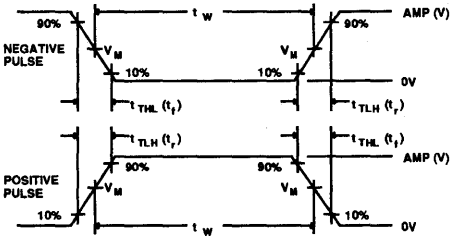
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F373, 74F374
Latch/Flip-Flop

FAST Products

74F373 Octal Transparent Latch (3-State)
74F374 Octal D Flip-Flop (3-State)
Product Specification

FEATURES

- **8-bit transparent latch-'F373**
- **8-bit positive edge triggered register-'F374**
- **3-State Outputs glitch free during power-up and power-down**
- **Common 3-state Output register**
- **Independent register and 3-state buffer operation**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F373	4.5ns	35mA
74F374	5.5ns	55mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F373N, N74F374N
20-Pin Plastic SOL	N74F373D, N74F374D

DESCRIPTION

The 74F373 is an octal transparent latch coupled to eight 3-State output devices. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High, and stores the data that is present one set-up time before the High-to-Low enable transition.

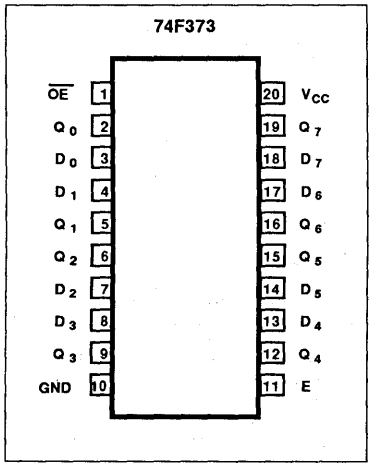
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

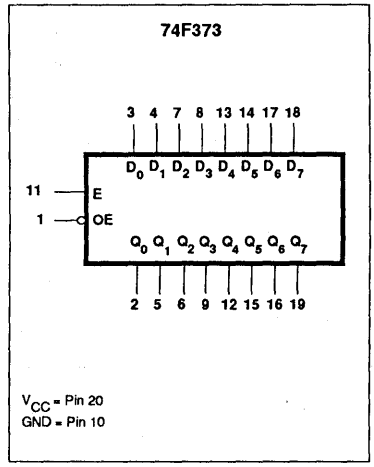
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20µA/0.6mA
E ('F373)	Enable input (active High)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
CP ('F374)	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	3-State outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

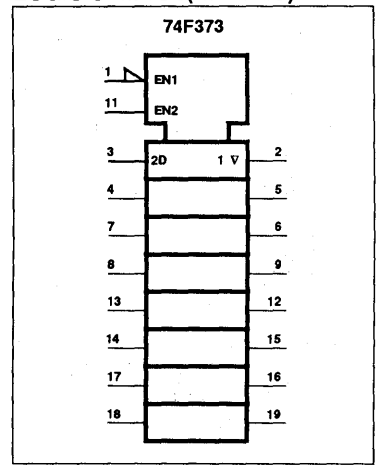
PIN CONFIGURATION



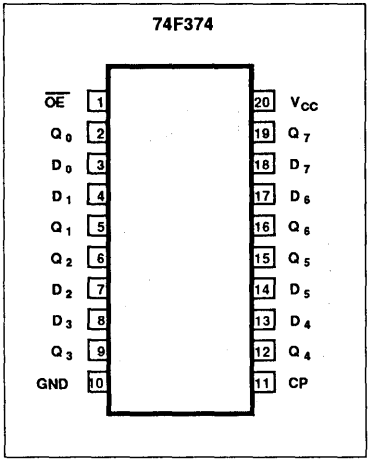
LOGIC SYMBOL



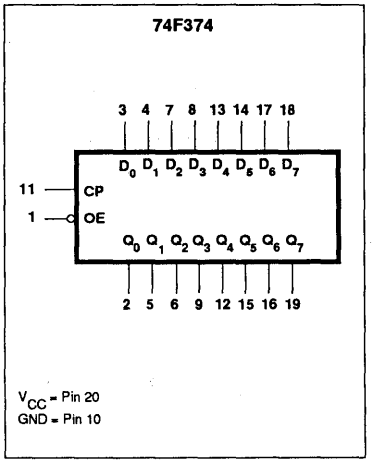
LOGIC SYMBOL(IEEE/IEC)



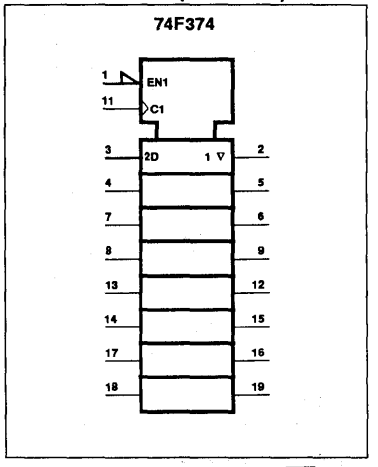
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

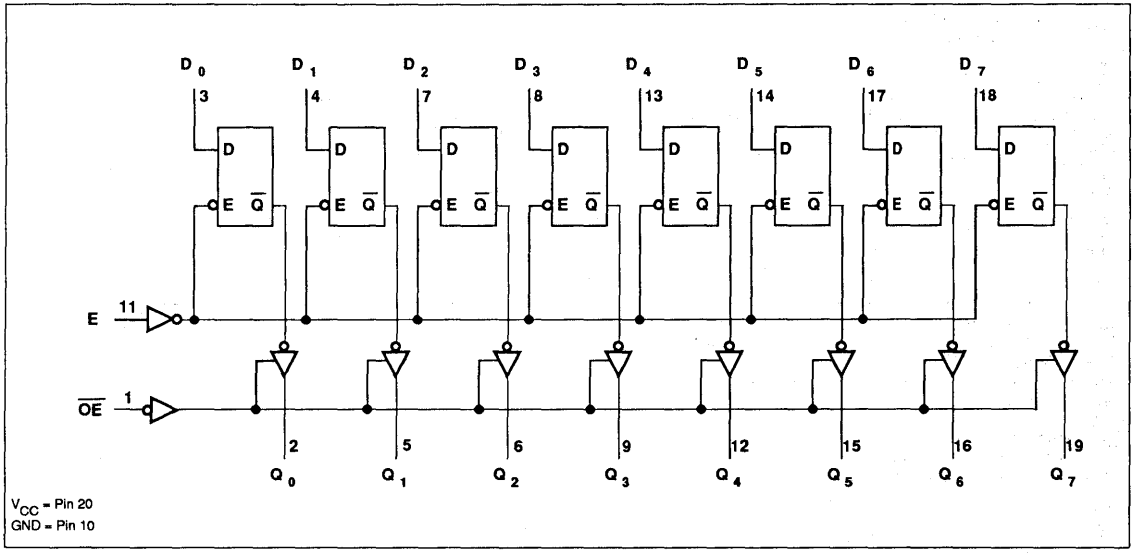
The 'F374 is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

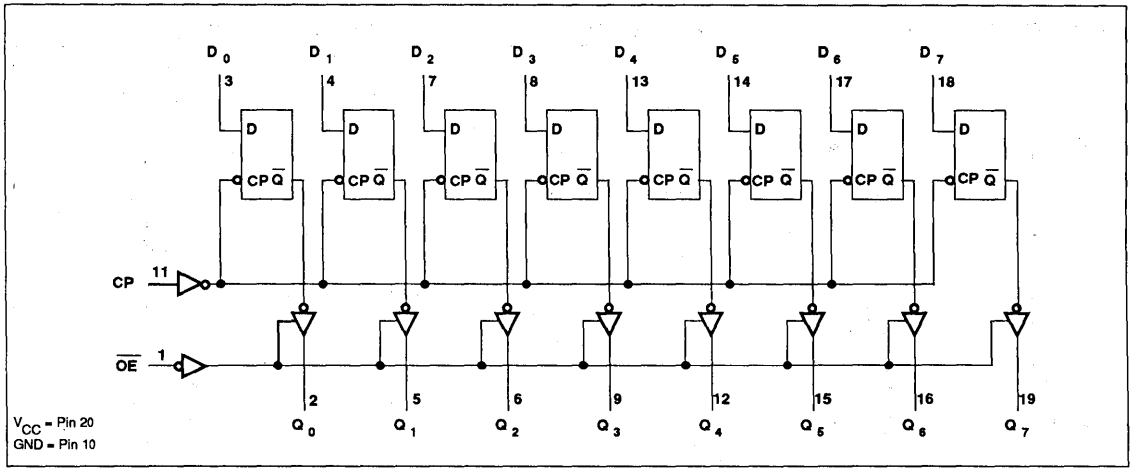
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is Low, the data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM 74F373



LOGIC DIAGRAM 74F374



FUNCTION TABLE 74F373

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	D_n	REGISTER	Q_0 - Q_7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X D_n	NC D_n	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

FUNCTION TABLE 74F374

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	D_n	REGISTER	Q_0 - Q_7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↕	X	NC	NC	Hold
H H	↕ ↑	X D_n	NC D_n	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	'F373	V_{CC} = MAX			35	60	mA
		'F374				57	86	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

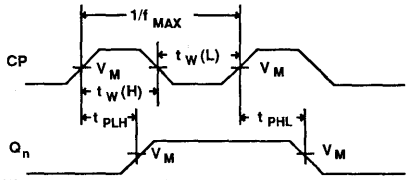
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F373	Waveform 3	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n		Waveform 2	5.0 3.0	9.0 4.0	11.5 7.0	5.0 3.0	12.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	5.0 5.6	11.0 7.5	2.0 2.0	11.5 8.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	4.5 3.8	6.5 5.0	2.0 2.0	7.0 6.0	ns ns
f_{MAX}	Maximum Clock frequency	74F374	Waveform 1	150	165		140		ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	3.5 3.5	5.0 5.0	7.5 7.5	3.0 3.0	8.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	9.0 5.3	11.0 7.5	2.0 2.0	12.0 8.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	5.3 4.3	6.0 5.5	2.0 2.0	7.0 6.5	ns ns

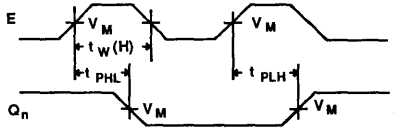
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Set-up time D_n to E	74F373	Waveform 4	0 1.0			0 1.0		ns
t_h(H) t_h(L)	Hold time D_n to E		Waveform 4	3.0 3.0			3.0 3.0		ns
t_w(H)	E Pulse width, High		Waveform 1	3.5			4.0		ns
t_s(H) t_s(L)	Set-up time D_n to CP	74F374	Waveform 5	2.0 2.0			2.0 2.0		ns
t_h(H) t_h(L)	Hold time D_n to CP		Waveform 5	0 0			0 0		ns
t_w(H) t_w(L)	CP Pulse width, High or Low		Waveform 1	3.5 4.0			3.5 4.0		ns

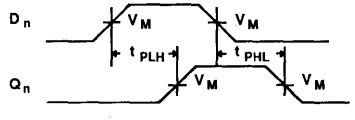
AC WAVEFORMS



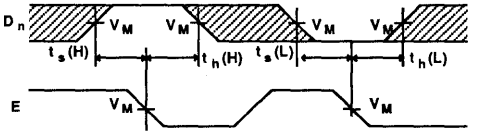
Waveform 1. Propagation Delay Clock To Output , Clock Pulse Widths, and Maximum Clock Frequency



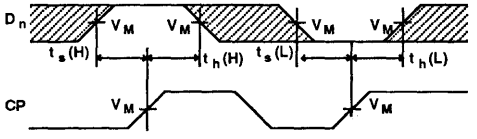
Waveform 2. Propagation Delay,Enable to Outputs And Enable Pulse Width



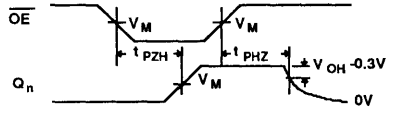
Waveform 3. Propagation Delay, Data To Outputs



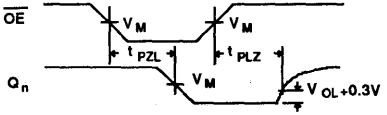
Waveform 4. Data Setup And Hold Times



Waveform 5. Data Setup And Hold Times



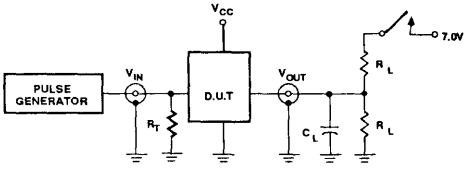
Waveform 6. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 7. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

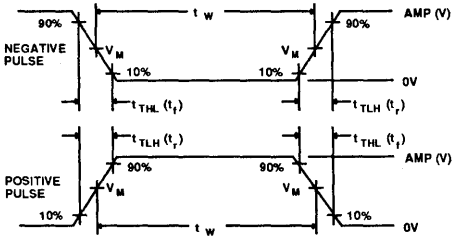
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F377
Flip-Flop

FAST Products

Octal D Flip-Flop With Enable
Product Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in Low and High states)**
- **Ideal for addressable register applications**
- **Enable for address and data synchronization applications**
- **Eight edge-triggered D-type flip-flops**
- **Buffered common clock**
- **See 'F273 for Master Reset version**
- **See 'F373 for transparent latch version**
- **See 'F374 for 3-State version**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F377	120MHz	65mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F377N
20-Pin Plastic SOL	N74F377D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/0.033	20μA/20μA
CP	Clock Pulse input (active rising edge)	1.0/0.033	20μA/20μA
$\overline{E}$	Enable input (active-Low)	1.0/0.033	20μA/20μA
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

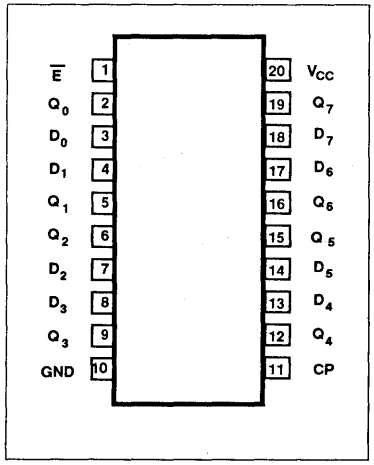
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

DESCRIPTION

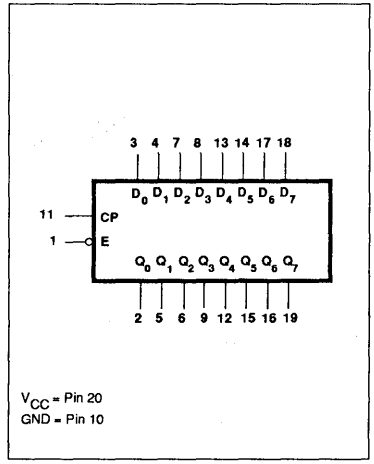
The 74F377 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Enable ($\overline{E}$) input is Low.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{E}$ input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

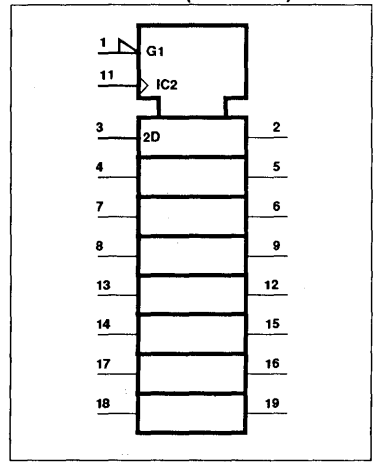
PIN CONFIGURATION



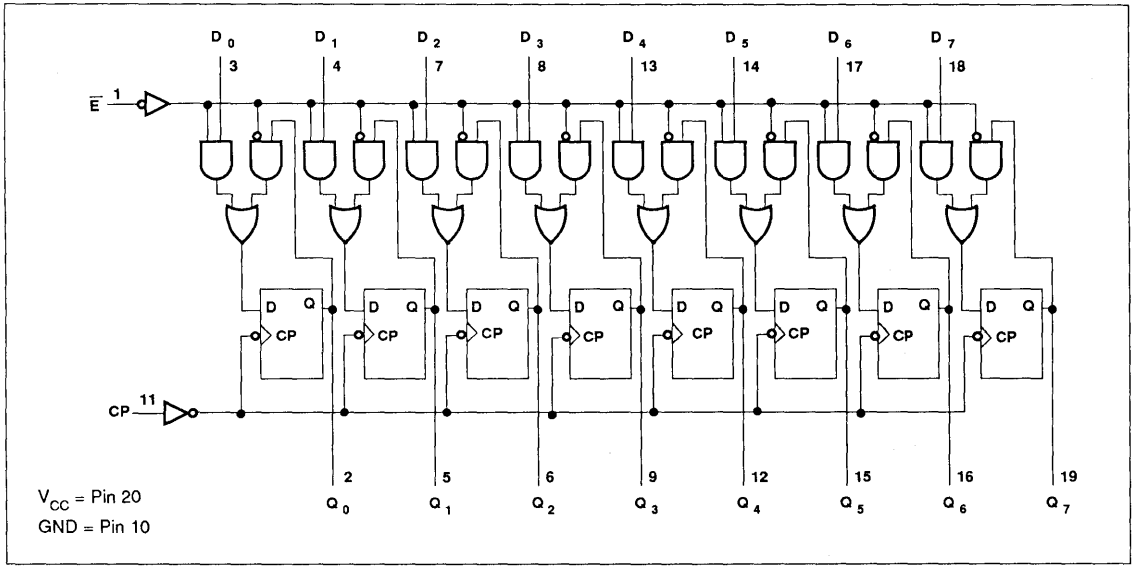
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{E}$	CP	D_n	Q_n	
l	↑	h	H	Load "1"
l	↑	l	L	Load "0"
h	↑	X	no change	Hold (do nothing)
H	X	X	no change	

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$\overline{E}$ &CP inputs	V_{CC} = MIN, V_{IL} = 0.0V,[3] V_{IH} = 4.5V,[3] I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
		other inputs	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_{OS}	Short circuit output current[4]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	D_n=4.5V, CP=↑, $\overline{E}$=GND		55	72	mA
		I_{CCL}		D_n=$\overline{E}$=GND, CP=↑		70	90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. To reduce the effect of external noise during test.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

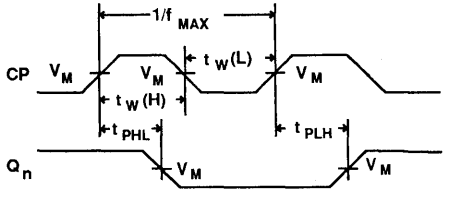
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	110	120		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	4.0 4.0	7.0 7.0	9.0 9.0	4.0 4.0	10.0 10.5	ns

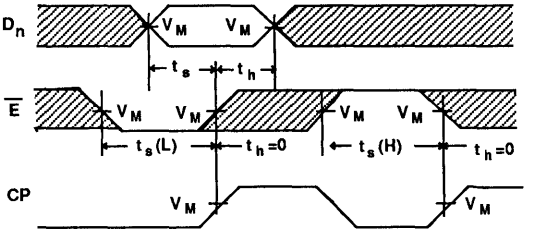
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2	2.0 2.0			2.5 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2	0.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{E}$ to CP	Waveform 2	3.0 4.0			3.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{E}$ to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	Clock Pulse width High or Low	Waveform 1	4.0 4.5			5.0 5.0		ns

AC WAVEFORMS



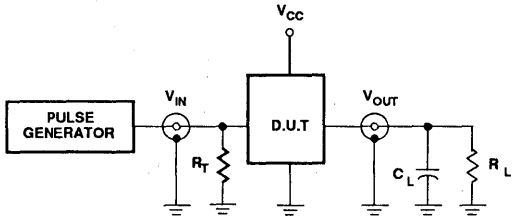
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



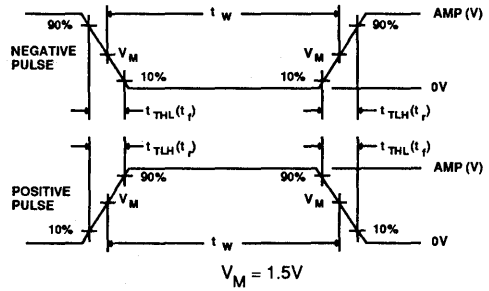
Waveform 2.
Data And Enable Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F378
Flip-Flop

FAST Products

Hex D Flip-Flop With Enable
Product Specification

FEATURES
- **8-bit high-speed parallel register**
- **Positive edge-triggered D-type inputs**
- **Fully buffered common Clock and Enable inputs**
- **Input clamp diodes limit high speed termination effects**
- **Fully TTL and CMOS compatible**

DESCRIPTION

The 74F378 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Enable ($\overline{E}$) input is Low.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output. The $\overline{E}$ input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F378	100MHz	35mA

ORDERING INFORMATION

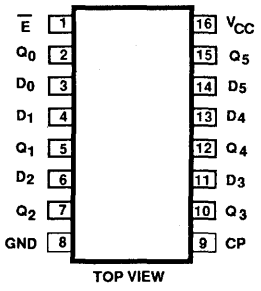
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F378N
16-Pin Plastic SO	N74F378D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_5	Data inputs	1.0/1,0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1,0	20µA/0.6mA
$\overline{E}$	Enable input (active Low)	1.0/1,0	20µA/0.6mA
Q_0 - Q_5	Data outputs	50/33	1.0mA/20mA

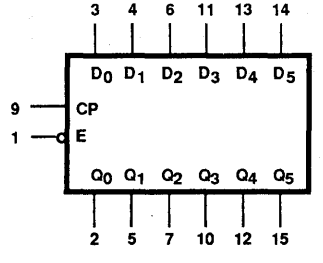
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



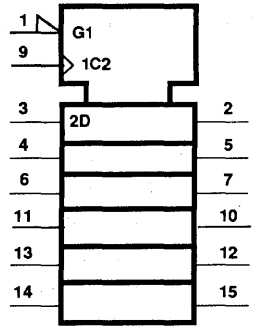
TOP VIEW

LOGIC SYMBOL

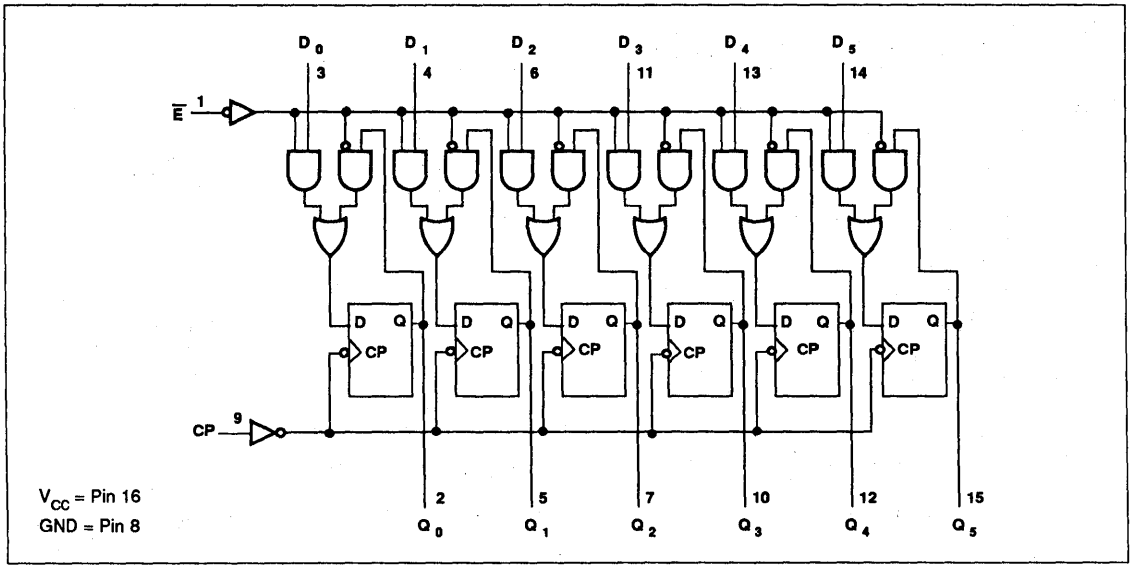


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{E}$	CP	D_n	Q_n	
l	↑	h	H	Load "1"
l	↑	l	L	Load "0"
h	↑	X	no change	Hold (do nothing)
H	X	X	no change	

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			32	45	mA
		I_{CCL}				35	45	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

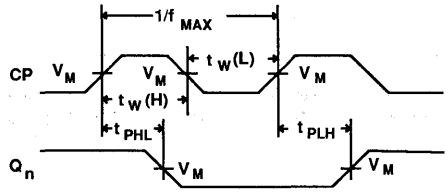
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	3.0 3.5	5.5 6.0	7.5 8.5	3.0 3.5	8.5 9.5	ns

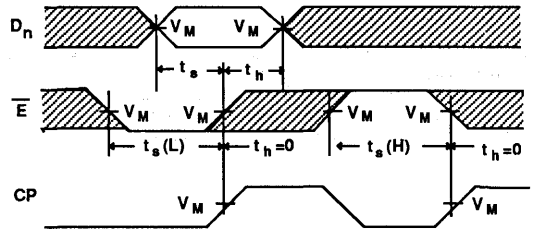
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2	4.0 4.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{E}$ to CP	Waveform 2	4.0 10.0			4.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{E}$ to CP	Waveform 2	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Clock Pulse width High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns

AC WAVEFORMS



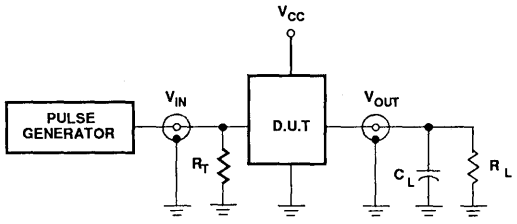
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



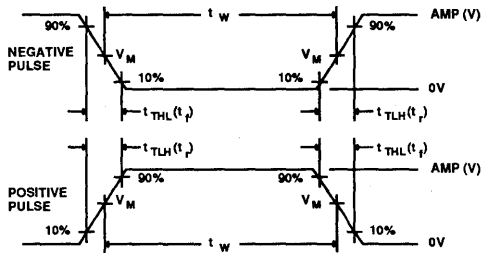
Waveform 2. Data And Enable Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F379
Register

Quad Parallel Register With Enable

FAST Products

Product Specification

FEATURES

- **Edge-triggered D-type inputs**
- **Buffered positive edge-triggered clock**
- **Buffered common Enable input**
- **True and complementary outputs**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F379	120MHz	28mA

DESCRIPTION

The 74F379 is a 4-bit register with buffered common Enable ($\overline{E}$). This device is similar to the 'F175 but features the common Enable rather common Master Reset.

ORDERING INFORMATION

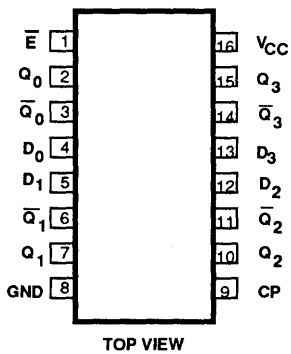
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F379N
16-Pin Plastic SO	N74F379D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{E}$	Enable input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
Q_0 - Q_3	True outputs	50/33	1.0mA/20mA
$\overline{Q}_0$ - $\overline{Q}_3$	Complementary outputs	50/33	1.0mA/20mA

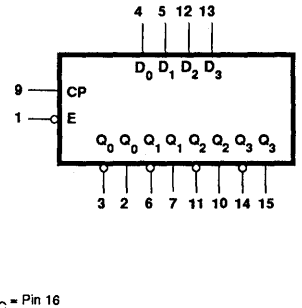
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



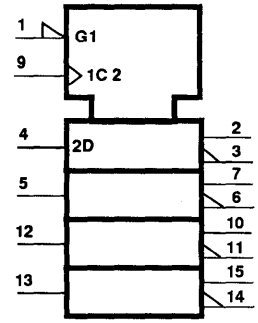
TOP VIEW

LOGIC SYMBOL

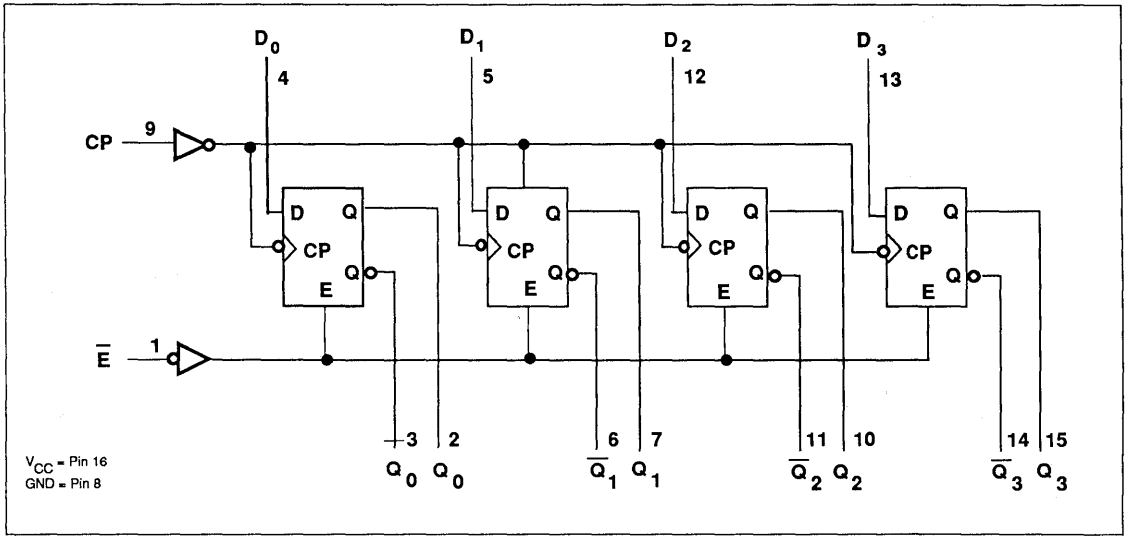


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
H	↑	X	NC	NC
L	↑	h	H	L
L	↑	l	L	H

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
NC = No change

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, D_n=$\overline{E}$=4.5V, CP=↑			28	40	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

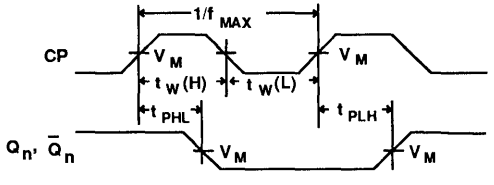
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	Waveform 1	3.5 4.5	5.0 6.5	7.0 8.5	3.5 4.5	8.0 9.5	ns

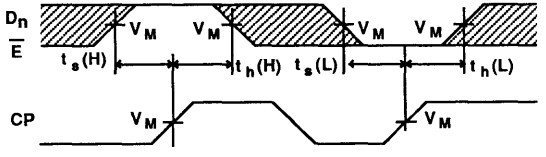
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{E}$ to CP	Waveform 2	6.0 6.0			6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{E}$ to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns

AC WAVEFORMS



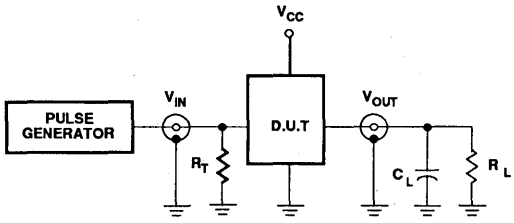
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



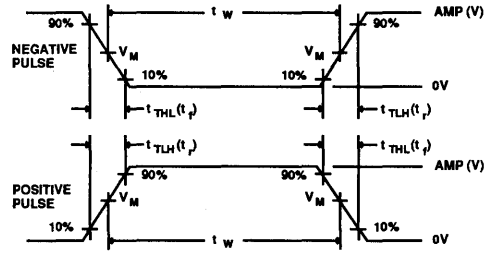
Waveform 2. Data And Enable Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAST 74F381
Arithmetic Logic Unit

FAST Products

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F381	6.5 ns	59mA

FEATURES

- **Low-input loading minimizes drive requirements**
- **Performs six arithmetic and logic functions**
- **Selectable Low (clear) and High (preset) functions**
- **Carry Generate and Propagate outputs for use with Carry look-ahead generator**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F381N
20-Pin Plastic SOL	N74F381D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_3	A operand inputs	1.0/4.0	20µA/2.4mA
B_0-B_3	B operand inputs	1.0/4.0	20µA/2.4mA
S_0-S_2	Function select inputs	1.0/1.0	20µA/0.6mA
C_n	Carry input	1.0/4.0	20µA/2.4mA
$\overline{P}$	Carry Propagate output (active-Low)	50/33	1.0mA/20mA
$\overline{G}$	Carry Generate output (active-Low)	50/33	1.0mA/20mA
F_0-F_3	Outputs	50/33	1.0mA/20mA

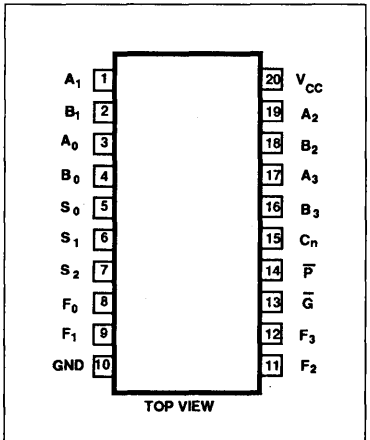
NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

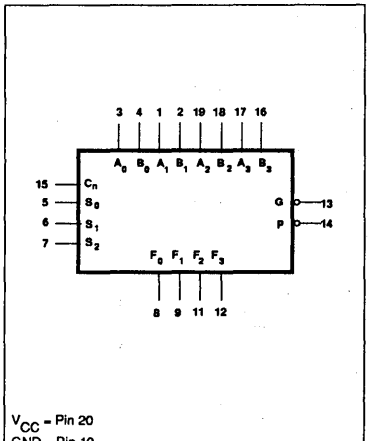
The 74F381 performs three arithmetic and three logic operations on two 4-bit words, A and B. Three additional Select (S_0-S_2) input codes force the Function outputs Low or High. Carry Propagate ($\overline{P}$) and Generate ($\overline{G}$) outputs are provided for use with the 'F182 Carry Look Ahead Generator for high-speed expansion to longer word lengths. For ripple expansion, refer to the 'F382 ALU data sheet.

Signals applied to the Select inputs (S_0-S_2) determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output function levels is shown in the Function Table. The circuit performs the arithmetic functions for either active-High or active-Low operands, with output levels in the same convention. In the subtract operating modes, it is necessary to force a Carry (High for active-High operands, Low for active-Low operands) into the C_n input of the least significant package. The Carry Generate ($\overline{G}$) and Carry Propagate ($\overline{P}$) outputs supply input signals to the 'F182 Carry look-ahead generator for expansion to longer word length, as shown in FIgure 1. Note that an 'F382 ALU is used for the most significant package. Typical delays for Figure 1 are given in Table 1.

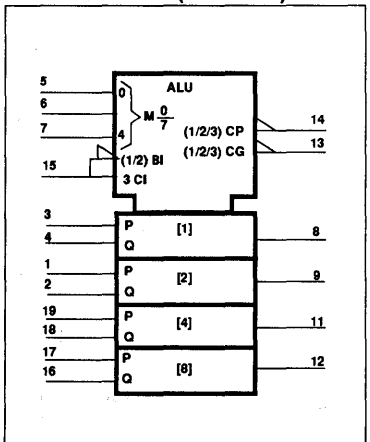
PIN CONFIGURATION



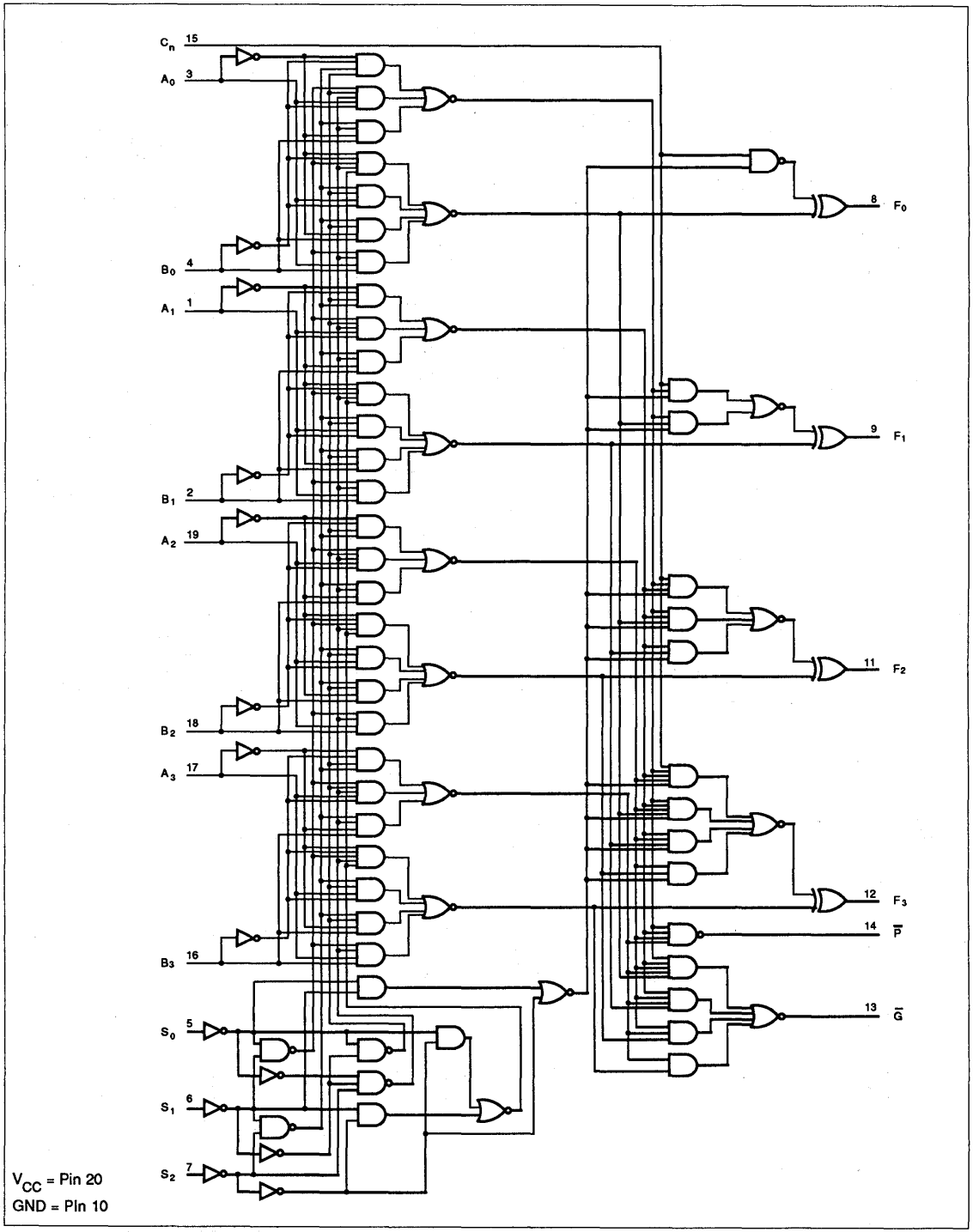
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS						OPERATING MODE
S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	$\overline{G}$	$\overline{P}$	
L	L	L	X	X	X	L	L	L	L	L	L	Clear
H	L	L	L	L	L	H	H	H	H	H	L	B minus A
H	L	L	L	L	H	L	H	H	H	L	L	
H	L	L	L	H	L	L	L	L	L	H	H	
H	L	L	L	H	H	H	H	H	H	H	L	
H	L	L	H	L	L	L	L	L	L	H	L	
H	L	L	H	L	H	H	H	H	H	L	L	
H	L	L	H	H	L	H	L	L	L	H	H	
H	L	L	H	H	H	L	L	L	L	H	L	
L	H	L	L	L	L	H	H	H	H	H	L	A minus B
L	H	L	L	L	H	L	L	L	L	H	H	
L	H	L	L	H	L	L	H	H	H	L	L	
L	H	L	L	H	H	H	H	H	H	H	L	
L	H	L	H	L	L	L	L	L	L	H	L	
L	H	L	H	L	H	H	L	L	L	H	H	
L	H	L	H	H	L	H	H	H	H	L	H	
L	H	L	H	H	H	L	L	L	L	H	L	
H	H	L	L	L	L	L	L	L	L	H	H	A Plus B
H	H	L	L	L	H	H	H	H	H	H	L	
H	H	L	L	H	L	H	H	H	H	H	L	
H	H	L	L	H	H	L	H	H	H	L	L	
H	H	L	H	L	L	H	L	L	L	H	H	
H	H	L	H	L	H	L	L	L	L	H	L	
H	H	L	H	H	L	L	L	L	L	H	L	
H	H	L	H	H	H	H	H	H	H	L	L	
L	L	H	X	L	L	L	L	L	L	H	H	A ⊕ B
L	L	H	X	L	H	H	H	H	H	H	H	
L	L	H	X	H	L	H	H	H	H	H	L	
L	L	H	X	H	H	L	L	L	L	L	L	
H	L	H	X	L	L	L	L	L	L	H	H	A + B
H	L	H	X	L	H	H	H	H	H	H	H	
H	L	H	X	H	L	H	H	H	H	H	H	
H	L	H	X	H	H	H	H	H	H	H	L	
L	H	H	X	L	L	L	L	L	L	L	L	AB
L	H	H	X	L	H	L	L	L	L	H	H	
L	H	H	X	H	L	L	L	L	L	L	L	
L	H	H	X	H	H	H	H	H	H	H	L	
H	H	H	X	L	L	H	H	H	H	H	H	Preset
H	H	H	X	L	H	H	H	H	H	H	H	
H	H	H	X	H	L	H	H	H	H	H	H	
H	H	H	X	H	H	H	H	H	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION SELECT TABLE

SELECT			OPERATING MODE
S_0	S_1	S_2	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	A⊕B
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = High voltage level
L = Low voltage level

Table 1. 16-Bit Delay Tabulation

PATH SEGMENT	TOWARD F	OUTPUT Cn+4, OVR
A_i or B_i to $\overline{P}$	7.2 ns	7.2ns
$\overline{P}_i$ to C_{n+i} ('F182)	6.2 ns	6.2ns
C_n to F	8.1 ns	-
C_n to C_{n+4}, OVR	-	8.0ns
Total Delay	21.5 ns	21.4 ns

APPLICATION

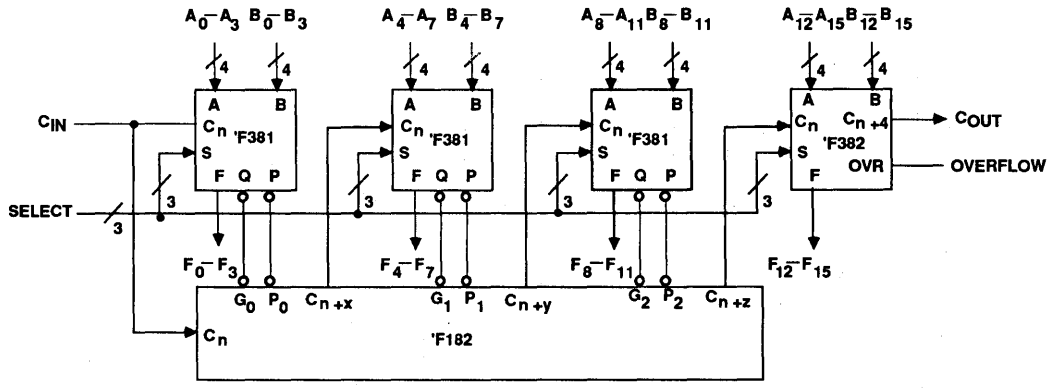


Figure 1. 16-Bit Look-Ahead Carry ALU Expansion

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	A_n, B_n, C_n	V_{CC} = MAX, V_I = 0.5V				-2.4	mA
		S_0, S_1, S_2					-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			59	89	mA

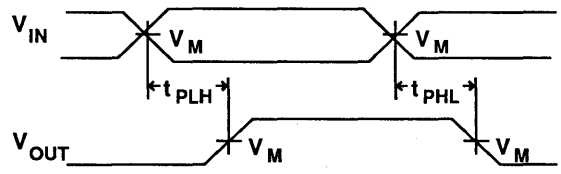
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to F_n	Waveform 1	2.5 2.5	6.0 4.5	11.0 6.5	2.5 2.5	12.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay Any A_n or B_n to any F_n	Waveform 1	3.5 3.0	7.0 6.0	13.0 9.0	3.5 3.0	16.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to F_n	Waveform 1	5.0 4.0	9.0 7.5	20.0 10.5	5.0 4.0	21.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to $\overline{G}$	Waveform 1	3.5 3.0	6.5 6.0	9.0 8.5	3.5 3.0	10.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to $\overline{P}$	Waveform 1	3.0 3.5	5.5 6.0	8.0 8.5	3.0 3.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{G}$ or $\overline{P}$	Waveform 1	5.0 5.5	7.5 8.5	11.0 12.5	5.0 5.0	12.5 14.0	ns

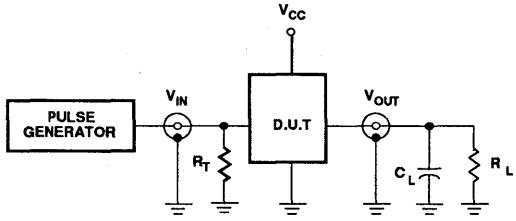
AC WAVEFORMS



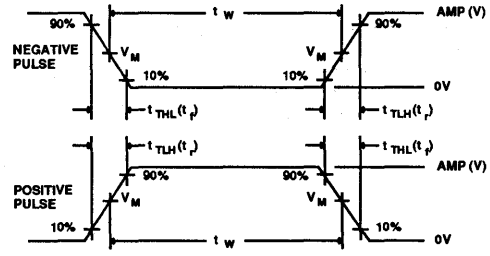
Waveform 1. Propagation Delay for Non-Inverting or Inverting paths

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F382
Arithmetic Logic Unit

FAST Products

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F382	7.0 ns	54mA

FEATURES

- **Performs six arithmetic logic functions**
- **Selectable Low (clear) and High (preset) functions**
- **Low-input loading minimizes drive requirements**
- **Carry output for ripple expansion**
- **Overflow output for Two's Complement arithmetic**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F382N
20-Pin Plastic SOL	N74F382D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_3	A operand inputs	1.0/4.0	20µA/2.4mA
B_0-B_3	B operand inputs	1.0/4.0	20µA/2.4mA
S_0-S_2	Function select inputs	1.0/1.0	20µA/0.6mA
C_n	Carry input	1.0/5.0	20µA/3.0mA
C_{n+4}	Carry output	50/33	1.0mA/20mA
OVR	Overflow output	50/33	1.0mA/20mA
F_0-F_3	Outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

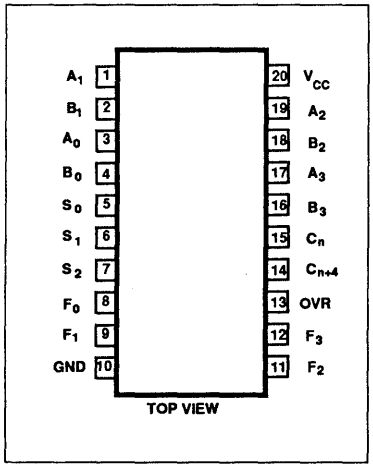
DESCRIPTION

The 74F382 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select (S_0-S_2) input codes force the Function outputs Low or High. An overflow output is provided for convenience in Two's Complement arithmetic.

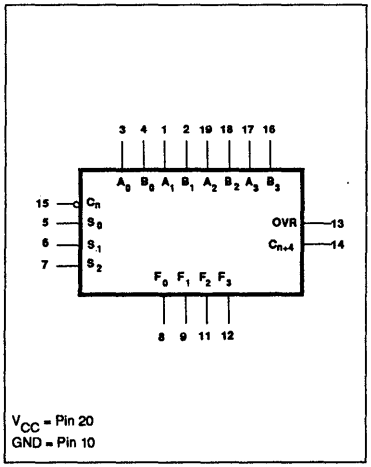
A carry output is provided for ripple expansion. For high-speed expansion using a carry look-ahead generator, refer to the 'F381 data sheet.

Signals applied to the Select inputs, S_0-S_2, determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Function Table. The circuit performs the arithmetic functions for either active-High or active-Low operands, with output levels in the same convention. In the subtract operating modes it is necessary to force a carry (High for active-High operands, Low for active-Low operands) into the C_n input of the least significant package. Ripple expansion is illustrated in Figure 1. The overflow output OVR is the Exclusive-OR of C_{n+3} and C_{n+4}; a High signal on OVR indicates overflow in Two's complement operation (See Table 2 for Two's complement arithmetic). Typical delays for Figure 1 are given in Table 1.

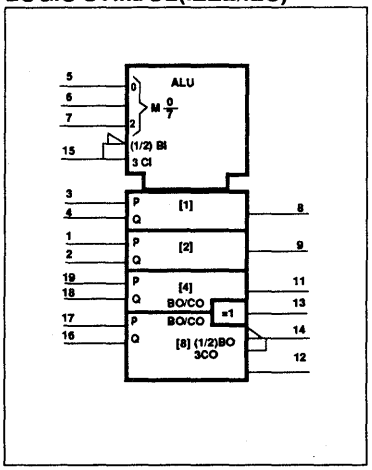
PIN CONFIGURATION



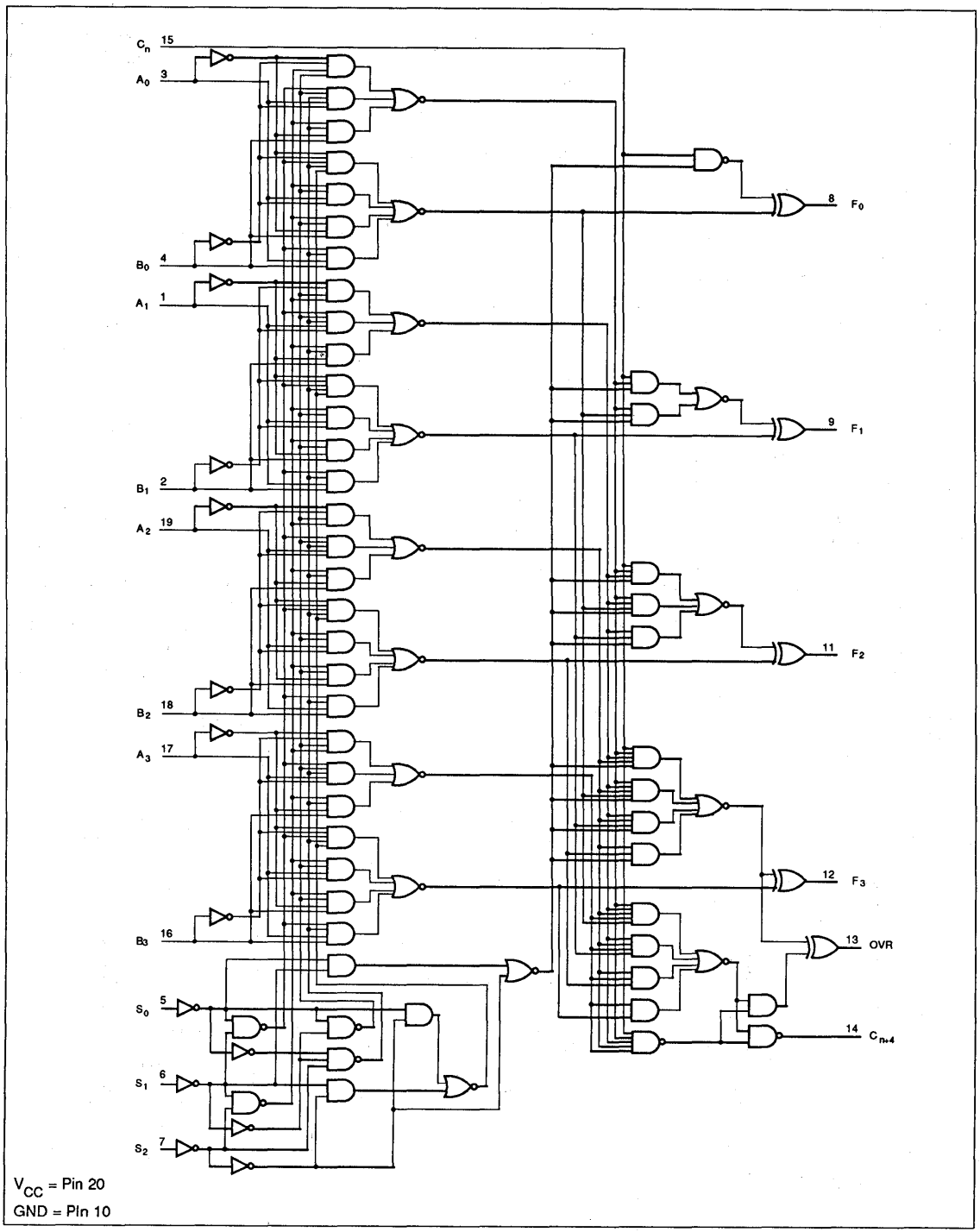
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS						OPERATING MODE
S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	OVR	C_{n+4}	
L	L	L	L	X	X	L	L	L	L	H	H	Clear
L	L	L	H	X	X	L	L	L	L	H	H	
H	L	L	L	L	L	H	H	H	H	L	L	B minus A
H	L	L	L	L	H	L	H	H	H	L	H	
H	L	L	L	H	L	L	L	L	L	L	L	
H	L	L	L	H	H	H	H	H	H	L	L	
H	L	L	H	L	L	L	L	L	L	L	H	
H	L	L	H	L	H	H	H	H	H	L	H	
H	L	L	H	H	L	H	L	L	L	L	L	
H	L	L	H	H	H	L	L	L	L	L	H	
L	H	L	L	L	L	H	H	H	H	L	L	A minus B
L	H	L	L	L	H	L	L	L	L	L	L	
L	H	L	L	H	L	L	H	H	H	L	H	
L	H	L	L	H	H	H	H	H	H	L	L	
L	H	L	H	L	L	L	L	L	L	L	H	
L	H	L	H	L	H	H	L	L	L	L	L	
L	H	L	H	H	L	H	H	H	H	L	H	
L	H	L	H	H	H	L	L	L	L	L	H	
H	H	L	L	L	L	L	L	L	L	L	L	A Plus B
H	H	L	L	L	H	H	H	H	H	L	L	
H	H	L	L	H	L	H	H	H	H	L	L	
H	H	L	L	H	H	L	H	H	H	L	H	
H	H	L	H	L	L	H	L	L	L	L	L	
H	H	L	H	L	H	L	L	L	L	L	H	
H	H	L	H	H	L	L	L	L	L	L	H	
H	H	L	H	H	H	H	H	H	H	L	H	
L	L	H	X	L	L	L	L	L	L	L	L	A ⊕ B
L	L	H	X	L	H	H	H	H	H	L	L	
L	L	H	L	H	L	H	H	H	H	L	L	
L	L	H	X	H	H	L	L	L	L	H	H	
L	L	H	H	H	L	H	H	H	H	H	H	
H	L	H	X	L	L	L	L	L	L	L	L	A + B
H	L	H	X	L	H	H	H	H	H	L	L	
H	L	H	X	H	L	H	H	H	H	L	L	
H	L	H	L	H	H	H	H	H	H	L	L	
H	L	H	H	H	H	H	H	H	H	H	H	
L	H	H	X	L	L	L	L	L	L	H	H	AB
L	H	H	X	L	H	L	L	L	L	L	L	
L	H	H	X	H	L	L	L	L	L	H	H	
L	H	H	L	H	H	H	H	H	H	L	L	
L	H	H	H	H	H	H	H	H	H	H	H	
H	H	H	X	L	L	H	H	H	H	L	L	Preset
H	H	H	X	L	H	H	H	H	H	L	L	
H	H	H	X	H	L	H	H	H	H	L	L	
H	H	H	L	H	H	H	H	H	H	L	L	
H	H	H	H	H	H	H	H	H	H	H	H	

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION SELECT TABLE

SELECT			OPERATING MODE
S_0	S_1	S_2	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	A⊕B
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = High voltage level
L = Low voltage level

Table 1. 16-Bit Delay Tabulation

PATH SEGMENT	TOWARD F	OUTPUT Cn+4, OVR
A_i or B_i to C_{n+4}	6.5 ns	6.5ns
C_n to C_{n+4}	6.3 ns	6.3ns
C_n to C_{n+4}	6.3 ns	6.3ns
C_n to F	8.1 ns	-
C_n to C_{n+4}, OVR	-	8.0ns
Total Delay	27.2 ns	27.1ns

Table 2. Two's Complement Arithmetic

MSB			LSB	Numerical Value
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	-8
H	L	L	H	-7
H	L	H	L	-6
H	L	H	H	-5
H	H	L	L	-4
H	H	L	H	-3
H	H	H	L	-2
H	H	H	H	-1

H = High voltage level
L = Low voltage level

APPLICATION

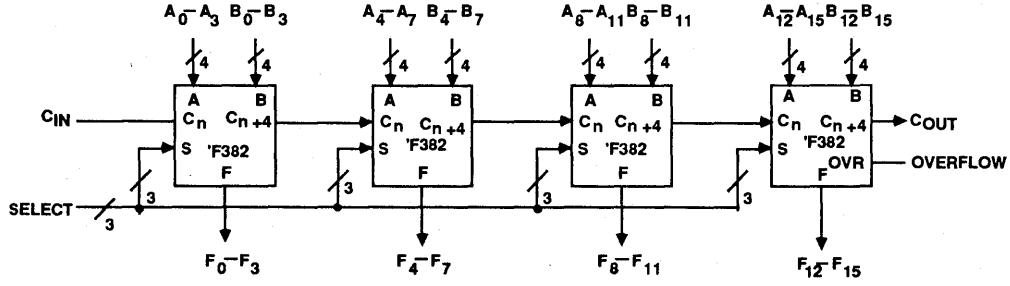


Figure 1. 16-Bit Ripple Carry ALU Expansion

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	C_n	V_{CC} = MAX, V_I = 0.5V				-3.0	mA
		A_0-A_3, B_0-B_3					-2.4	mA
		S_0, S_1, S_2					-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			54	81	mA

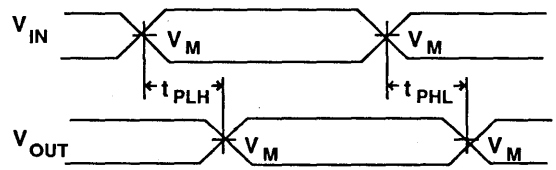
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to F_n	Waveform 1	3.0 2.5	7.0 4.5	12.0 6.5	2.5 2.5	13.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to F_n	Waveform 1	3.5 3.0	8.0 6.0	13.5 10.0	3.5 2.5	17.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay S_i to F_i	Waveform 1	5.5 5.5	9.0 7.5	15.0 10.5	5.5 5.5	16.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to C_{n+4}	Waveform 1	3.5 3.5	7.0 6.5	10.5 9.5	3.5 3.5	11.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay S_i to OVR or C_{n+4}	Waveform 1	7.0 5.0	10.5 8.0	14.5 11.0	6.5 5.0	17.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	Waveform 1	3.0 3.5	4.5 5.0	6.0 6.5	2.5 3.5	6.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay C_n to OVR	Waveform 1	4.5 3.0	9.0 5.0	13.5 6.5	4.0 3.0	15.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to OVR	Waveform 1	6.0 3.5	9.0 6.5	12.5 9.0	5.5 3.5	16.5 10.0	ns

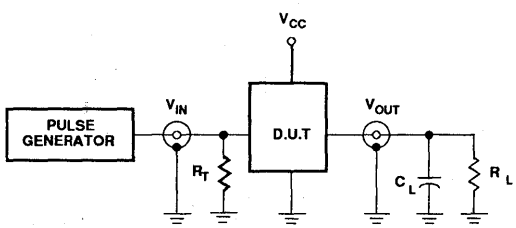
AC WAVEFORMS



Waveform 1. Propagation Delay for Non-Inverting or Inverting paths

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



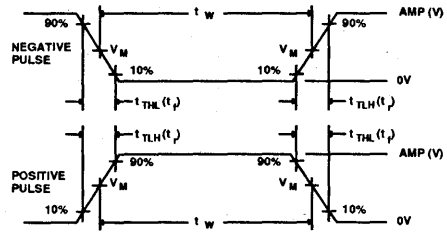
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F385
Adder/Subtractor

FAST Products

Quad Serial Adder/Subtractor
Product Specification

FEATURES

- **Four independent adder/subtractors**
- **Two's complement arithmetic**
- **Synchronous operation**
- **Common Clear and Clock**
- **One's complement or magnitude only capability**
- **'F385 is designed for use with serial multipliers in implementing digital filters and butterfly networks in fast Fourier transforms**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F385	140 MHz	55mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F385N
20-Pin Plastic SOL	N74F385D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

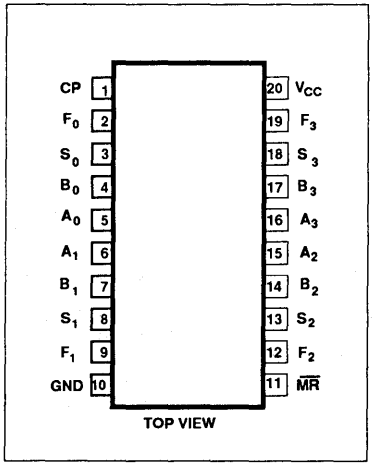
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	A operand inputs	1.0/1.0	20µA/0.6mA
B_0 - B_3	B operand inputs	1.0/1.0	20µA/0.6mA
S_0 - S_3	Function select inputs	1.0/1.0	20µA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Asynchronous Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
F_0 - F_3	Sum or difference outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

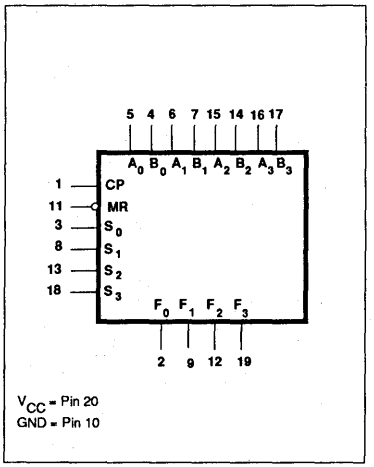
DESCRIPTION

The 74F385 contains four serial adder/subtractors with common Clock and Master Reset, but independent Operand and Select inputs. Each adder/subtractor contains two edge-triggered flip-flops to store sum and carry, as shown in the Logic Diagram. Flip-flop state changes occur on the rising edge of the Clock Pulse (CP) input signal. The Select (S) input should be Low for the Add (A plus B) mode and High for the Subtract (A minus B) mode. A Low signal on the asynchronous Master Reset ($\overline{MR}$) input clears the sum flip-flop and resets the Carry flip-flop to zero in the Add mode or presets it to one in the Subtract mode. In the Subtract mode, the B operand is internally complemented. Presetting the Carry flip-flop to one completes the Two's Complement transformation by adding one to "A plus B" during the first (LSB) operation after $\overline{MR}$ is released. For One's Complement subtraction, the Carry flip-flop can be set to zero by making S Low during reset, then making S High after the reset but before the next Clock.

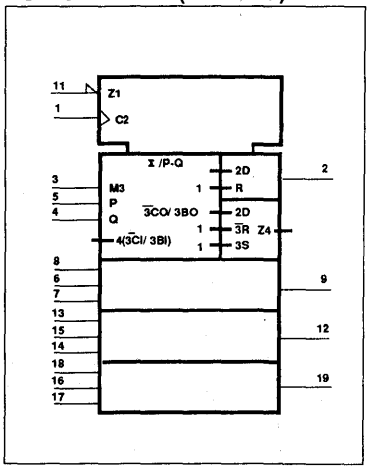
PIN CONFIGURATION



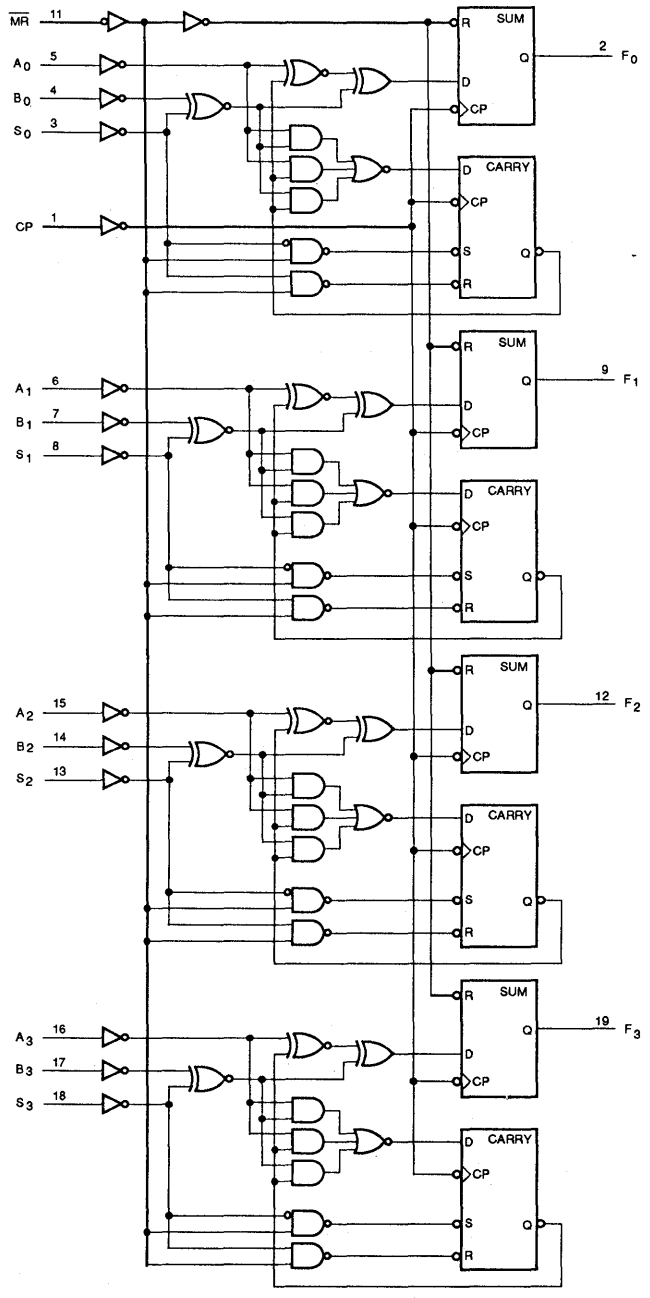
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC}=pin 20
GND=pin 10

FUNCTION TABLE

INPUTS*				INTERNAL CARRY**		OUTPUT*	OPERATING MODE
$\overline{MR}$	S	A	B	C	C_1	F	
L	L	X	X	L	L	L	Clear
L	H	X	X	H	H	L	
H	L	L	L	L	L	L	Add
H	L	L	L	H	L	H	
H	L	L	H	L	L	H	
H	L	L	H	H	H	L	
H	L	H	L	L	L	H	
H	L	H	L	H	H	L	
H	L	H	H	L	H	L	
H	L	H	H	H	H	H	
H	H	L	L	L	L	H	Subtract
H	H	L	L	H	H	L	
H	H	L	H	L	L	L	
H	H	L	H	H	L	H	
H	H	H	L	L	H	L	
H	H	H	L	H	H	H	
H	H	H	H	L	L	H	
H	H	H	H	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't care
* = Inputs before Clock transition, output after C
** = Carry flip-flop state before (C) and after (C_1) Clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			55	80	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

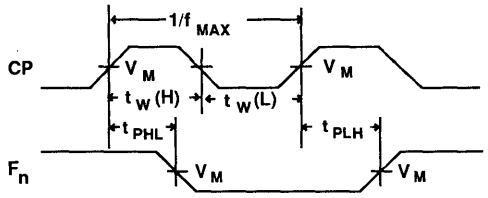
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frquency	Waveform 1	100	140		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to F_n	Waveform 1	3.0 3.5	5.0 5.5	8.0 9.0	2.5 3.5	9.0 10.0	ns
t_{PLH}	Propagation delay $\overline{MR}$ to F_n	Waveform 2	4.0	6.5	9.5	4.0	10.5	ns

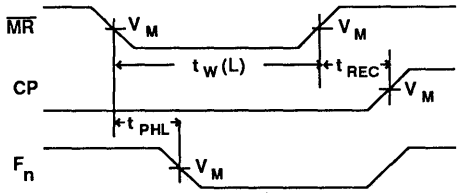
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n, B_n or S_n to CP	Waveform 3	12.0 12.0			12.0 12.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n, B_n or S_n to CP	Waveform 3	0 0			0 0		ns
t_w(H) t_w(L)	CP Pulse width, High or Low	Waveform 3	6.0 6.0			6.0 6.0		ns
t_w(L)	$\overline{MR}$ Pulse width, Low	Waveform 2	6.0			6.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 2	8.5			9.5		ns

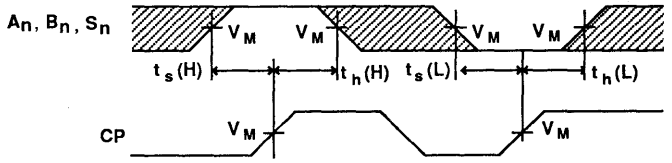
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



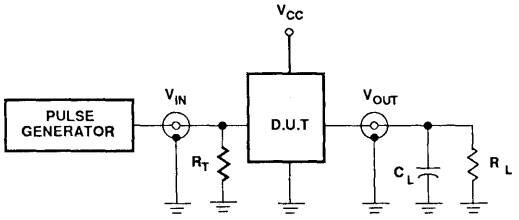
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



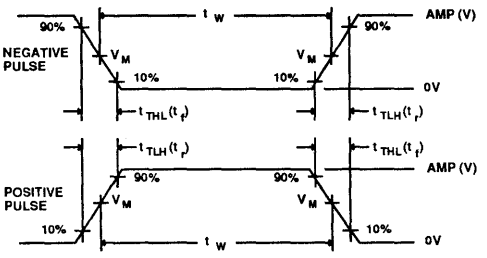
Waveform 3. Data And Select Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F393
Dual 4-Bit Binary Ripple Counter

FAST Products

Product Specification

FEATURES
- **Two 4-Bit binary counters**
- **Two Master Resets to clear each 4-bit counter individually**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F393	125MHz	40mA

DESCRIPTION

The 74F393 is a Dual Ripple Counter with separate Clock ($\overline{CP}_n$) and Master Reset Reset (MR) inputs to each counter. The two counters are identified by the "a" and "b" suffixes in the pin configuration. The operation of each half of the 'F393 is the same. The counters are triggered by a High-to-Low transition of the Clock ($\overline{CP}_a$ and $\overline{CP}_b$) inputs. The counter outputs are internally connected to provide Clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high speed address decoding. The Master Resets (MR_a and MR_b) are active High asynchronous inputs; one for each 4-bit counter. A High level in the MR input overrides the Clock and sets the outputs Low.

ORDERING INFORMATION

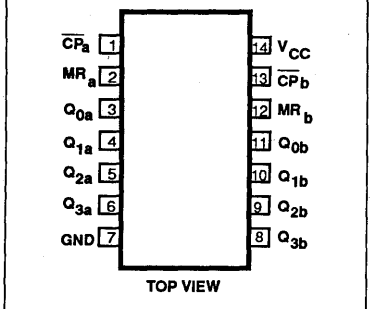
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F393N
14-Pin Plastic SO	N74F393D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{CP}_a$, $\overline{CP}_b$	Clock inputs	1.0/1.0	20µA/0.6mA
MR_a, MR_b	Master Reset inputs	1.0/1.0	20µA/0.6mA
Q_{na} - Q_{nb}	Data outputs	50/33.3	1.0mA/20mA

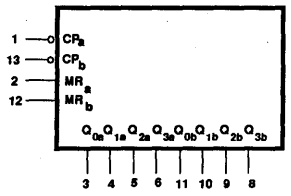
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



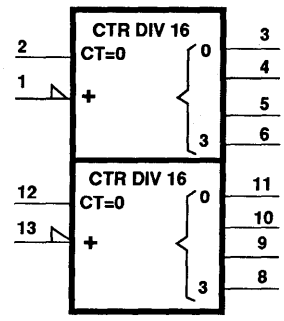
TOP VIEW

LOGIC SYMBOL

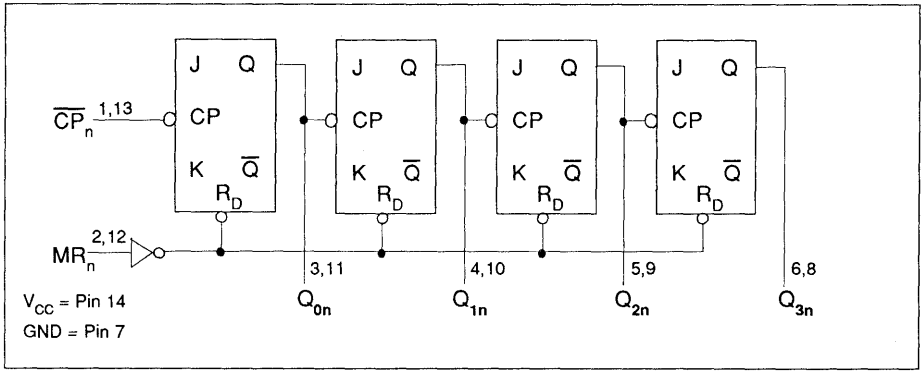


V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

COUNT	OUTPUTS			
	Q_{0n}	Q_{1n}	Q_{2n}	Q_{3n}
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			25	36	mA
		I_{CCL}				42	58	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

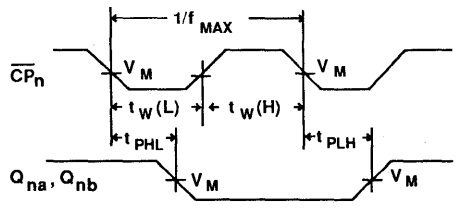
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_n$ to Q_{0a}, Q_{0b}	Waveform 1	3.5 5.0	5.5 7.0	8.0 10.0	3.5 5.0	9.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_n$ to Q_{1a}, Q_{1b}	Waveform 1	5.0 7.5	7.0 9.5	10.0 12.0	4.5 7.0	13.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_n$ to Q_{2a}, Q_{2b}	Waveform 1	8.0 9.5	10.0 11.5	13.0 14.5	7.0 9.0	15.0 15.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_n$ to Q_{3a}, Q_{3b}	Waveform 1	10.5 12.0	12.5 14.0	15.5 16.5	10.0 11.5	17.0 17.5	ns
t_{PHL}	Propagation delay MR to Q_{na}, Q_{nb}	Waveform 2	4.0	6.0	9.0	4.0	9.0	ns

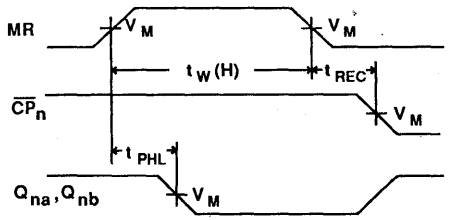
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_w(H)$ $t_w(L)$	$\overline{CP}_n$ Pulse width, High or Low	Waveform 1	4.5 3.5			5.0 4.0		ns
$t_w(H)$	MR Pulse width High	Waveform 2	3.5			4.5		ns
t_{REC}	Recovery time MR to $\overline{CP}_n$	Waveform 2	2.5			3.0		ns

AC WAVEFORMS



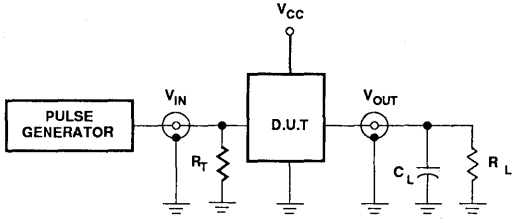
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



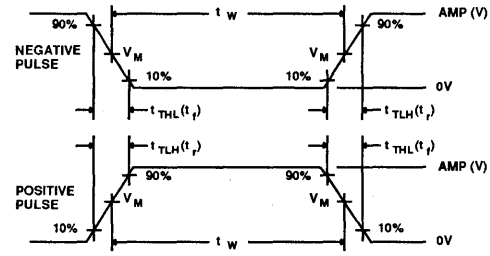
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F395
Shift Register

FAST Products

4-Bit Cascadable Shift Register (3-state)

Product Specification

FEATURES
- **4-bit parallel load shift register**
- **Independent 3-state buffer outputs, Q_0-Q_3**
- **Separate Q_s output for serial expansion**
- **Asynchronous Master Reset**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F395	120MHz	32mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F395N
16-Pin Plastic SO	N74F395D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
D_s	Serial data input	1.0/1.0	20µA/0.6mA
PE	Parallel Enable input	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CP}$	Clock Pulse input (active falling edge)	1.0/1.0	20µA/0.6mA
Q_s	Serial expansion output	50/33	1.0mA/20mA
Q_0 - Q_3	Data outputs (3-state)	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

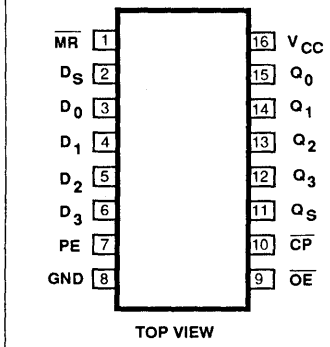
The 74F395 is a 4-bit Shift Register with serial and parallel synchronous operating modes and 3-state buffer outputs. The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is High, data is loaded from the Parallel Data inputs (D_0 - D_3) into the register synchronous with the High-to-Low transition of the Clock input ($\overline{CP}$). When PE is Low, the data at the Serial Data input (D_s) is loaded into the Q_0 flip-flop, and the data in the register is shifted one bit to the right in the direction ($Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$) synchronous with the negative clock transition. The PE and Data inputs are fully edge-triggered and must be stable one setup prior to the High-to-Low transition of the clock.

The Master Reset ($\overline{MR}$) is an asynchronous active-Low input. When Low, the $\overline{MR}$ overrides the clock and all other inputs and clears the register.

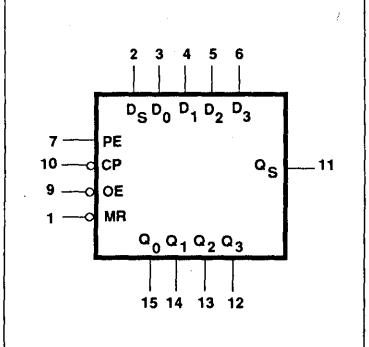
The 3-state output buffers are designed to drive heavily loaded 3-state buses, or large capacitive loads.

The active-Low Output Enable ($\overline{OE}$) controls all four 3-state buffers independent of the register operation. The data in the register appears at the outputs when $\overline{OE}$ is Low. The outputs are in High impedance "OFF" state, which means they will neither drive nor load the bus when $\overline{OE}$ is High. The output from the last stage is brought out separately. This output (Q_s) is tied to the Serial Data input (D_s) of the next register for serial expansion applications. The Q_s output is not affected by the 3-state buffer operation.

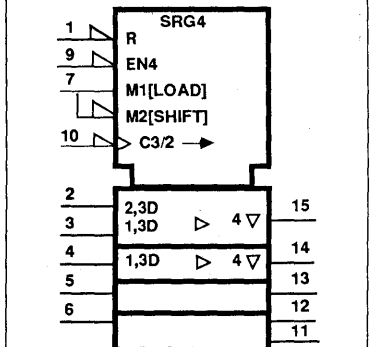
PIN CONFIGURATION



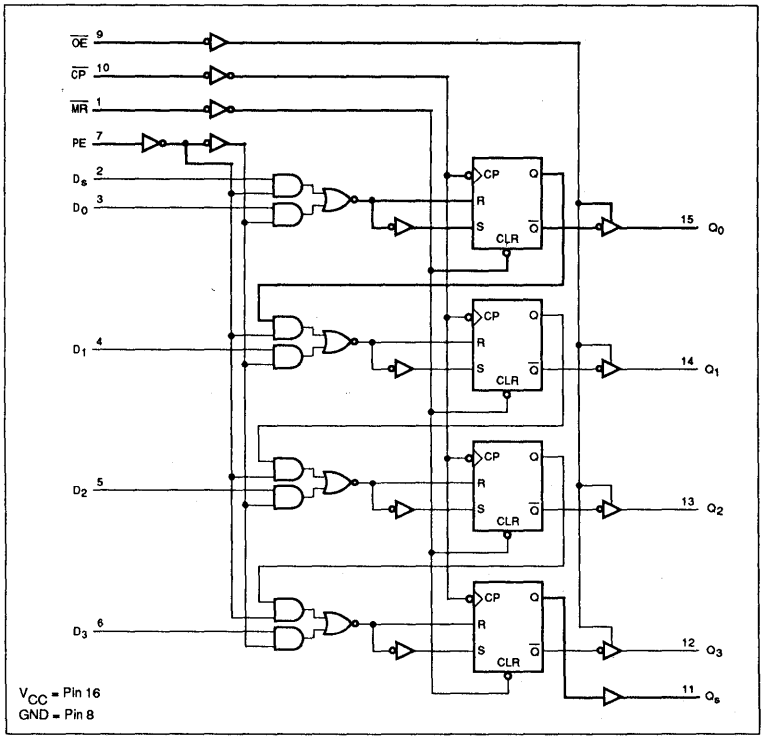
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT-FUNCTION TABLE

INPUTS					OUTPUTS				REGISTER OPERATING MODES
$\overline{MR}$	$\overline{CP}$	PE	D_S	D_n	Q_0	Q_1	Q_2	Q_3	
L	X	X	X	X	L	L	L	L	Reset (clear)
H	↓	l	l	X	L	q_0	q_1	q_2	Shift right
H	↓	l	h	X	H	q_0	q_1	q_2	
H	↓	h	X	l	L	L	L	L	Parallel load
H	↓	h	X	h	H	H	H	H	

INPUTS		OUTPUTS		3-STATE BUFFER OPERATING MODES
$\overline{OE}$	Q_n (Register)	Q_0, Q_1, Q_2, Q_3	Q_S	
L	L	L	L	Read
L	H	H	H	
H	L	Z	L	Disable buffers
H	H	Z	H	

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low clock transition
q_n = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the High-to-Low clock transition
X = Don't care
Z = High impedance "OFF" state
↓ = High-to-Low clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	Q_S	40	mA
		Q_0-Q_3	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_S			-1	mA
		Q_0-Q_3			-3	mA
I_{OL}	Low-level output current	Q_S			20	mA
		Q_0-Q_3			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	Q_S	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		Q_0- Q_3		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OZH}	Off-state output current High level voltage applied	Q_0- Q_3 only	V_{CC} = MAX, V_O= 2.7V					50	µA
I_{OZL}	Off-state output current Low level voltage applied	Q_0- Q_3 only	V_{CC} = MAX, V_O= 0.5V					-50	µA
I_{OS}	Short-circuitoutput current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{MR}$=PE=D_n=D_s=4.5V, $\overline{OE}$=GND, CP=↓			33	48	mA
		I_{CCL}		$\overline{MR}$=$\overline{OE}$=D_n=D_s=GND, PE=4.5V, CP=↓			35	50	mA
		I_{CCZ}		$\overline{MR}$=D_n=D_s=GND, $\overline{OE}$=4.5V			32	46	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

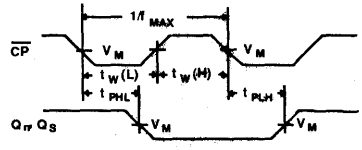
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	105	120		95		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_n	Waveform 1	3.5 5.0	6.0 8.0	8.5 11.0	3.5 5.0	9.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_S	Waveform 1	5.0 5.5	6.5 7.5	9.0 10.0	4.5 5.0	10.0 10.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	5.0	7.5	10.0	5.0	10.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_S	Waveform 2	4.5	7.0	9.0	4.5	9.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 4 Waveform 5	4.0 3.5	6.5 6.0	9.0 8.0	4.0 3.5	10.0 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 4 Waveform 5	1.0 1.0	2.5 3.5	4.5 5.5	1.0 1.0	5.5 6.5	ns

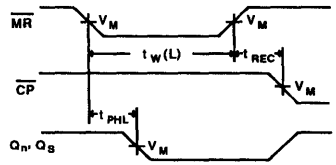
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to $\overline{CP}$	Waveform 3	2.5 1.5			3.0 2.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to $\overline{CP}$	Waveform 3	1.5 1.5			1.5 1.5		ns
t_s(H) t_s(L)	Setup time, High or Low PE to $\overline{CP}$	Waveform 3	6.5 6.0			7.0 6.5		ns
t_h(H) t_h(L)	Hold time, High or Low PE to $\overline{CP}$	Waveform 3	0 0			0 0		ns
t_w(H) t_w(L)	$\overline{CP}$ Pulse width High or Low	Waveform 1	5.0 4.0			5.5 4.5		ns
t_w(L)	$\overline{MR}$ Pulse width Low	Waveform 2	2.5			3.0		ns
t_{REC}	Recovery time $\overline{MR}$ to $\overline{CP}$	Waveform 2	6.0			7.0		ns

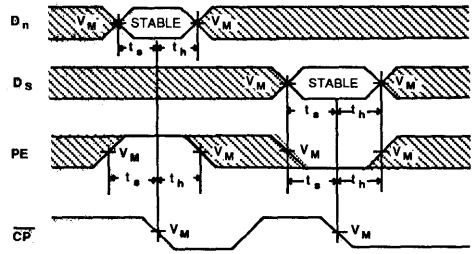
AC WAVEFORMS



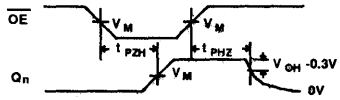
Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths, and Maximum Clock Frequency



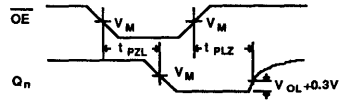
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 3. Parallel Enable and Data Setup Time and Hold Time



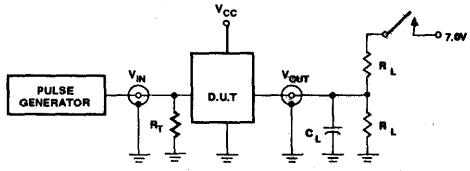
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs and Totem-Pole Output (Q_S)

SWITCH POSITION

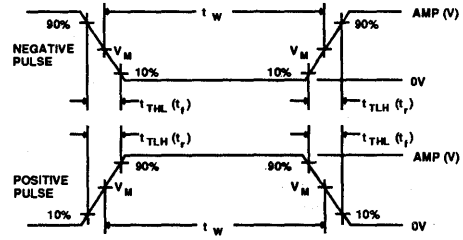
TEST	SWITCH
t_{PZL}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F398, 74F399 Registers

74F398 Quad 2-Port Register With True And Complementary Outputs
74F399 Quad 2-Port Register

Product Specification

FEATURES

- **Select inputs from two data sources**
- **Fully positive edge triggered**
- **Both True and Complementary outputs-'F398**

DESCRIPTION

The 74F398 and 74F399 are the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock.

The 'F399 is the 16-pin version of the 'F398, with only the true (Q_n) outputs of the flip-flops available.

The 'F398 and 'F399 are high speed quad 2-port registers. They select 4 bits of data from either of two sources (Ports) under control of a common select input (S). The selected data is transferred to a 4-bit output register synchronous with the Low-to-High transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0n}, I_{1n}) and Select input (S) must be stable only a setup time prior to and hold time after the Low-to-High transition of the Clock input for predictable operation. The 'F398 has both Q and $\overline{Q}$ outputs.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F398	120MHz	25mA
74F399	120MHz	22mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-pin Plastic DIP	N74F398N
20-pin Plastic SOL	N74F398D
16-pin Plastic DIP	N74F399N
16-pin Plastic SO	N74F399D

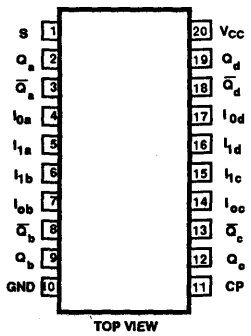
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0a}, I_{0b}, I_{0c}, I_{0d}	Data inputs from source 0	1.0/1.0	20µA/0.6mA
I_{1a}, I_{1b}, I_{1c}, I_{1d}	Data inputs from source 1	1.0/1.0	20µA/0.6mA
S	Common Select input	1.0/1.0	20µA/0.6mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
Q_a, Q_b, Q_c, Q_d	Register true outputs	50/33	1.0mA/20mA
$\overline{Q}_a$, $\overline{Q}_b$, Q_c, $\overline{Q}_d$	Register complementary outputs ('F398)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

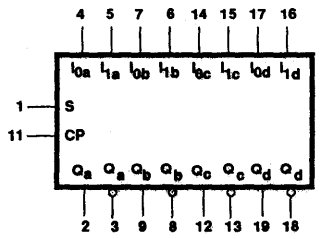
'F398



TOP VIEW

LOGIC SYMBOL

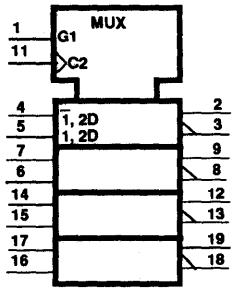
'F398



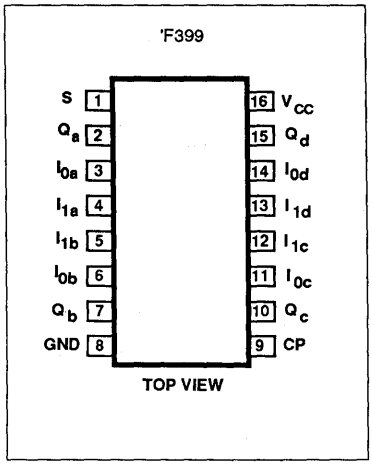
V_{CC} = pin 20
GND = pin 10

LOGIC SYMBOL(IEEE/IEC)

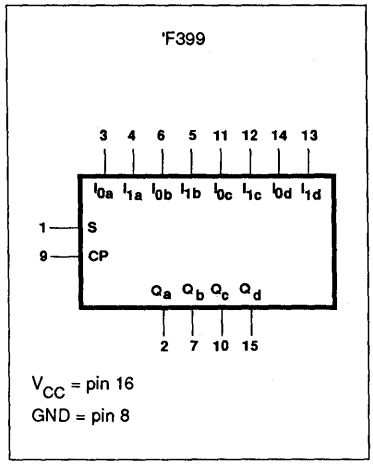
'F398



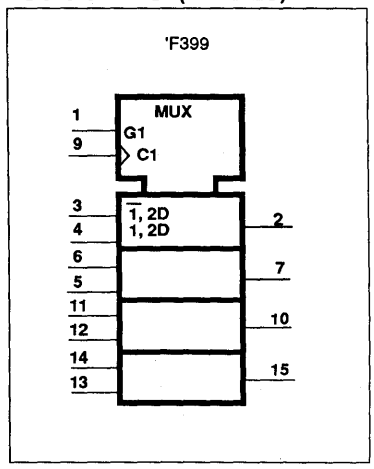
PIN CONFIGURATION



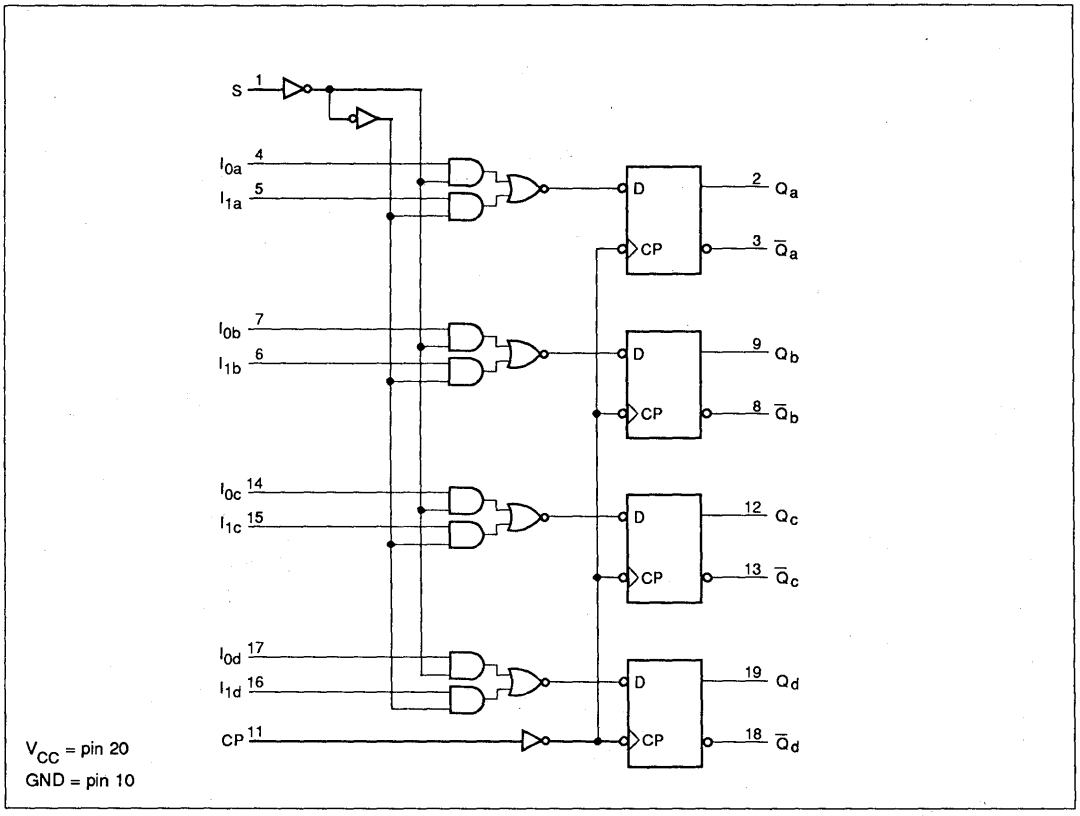
LOGIC SYMBOL



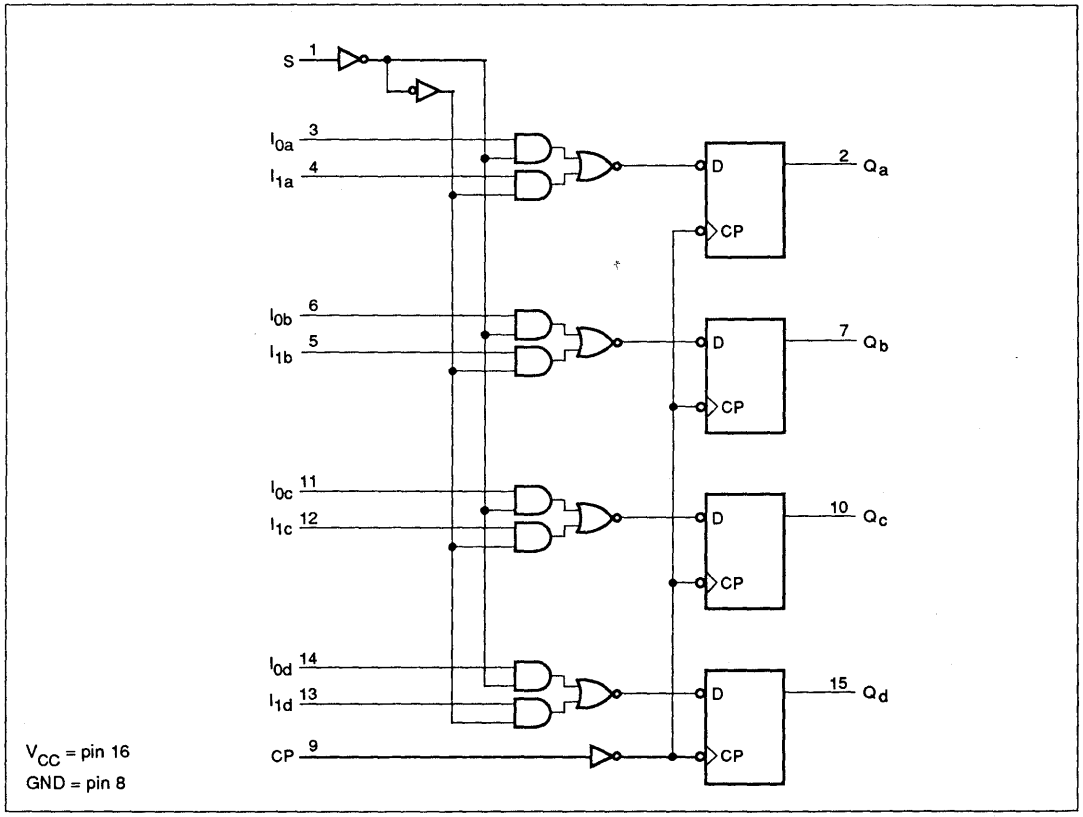
LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM for 'F398



LOGIC DIAGRAM for 'F399



FUNCTION TABLE

INPUTS				OUTPUTS	
CP	S	I_{0n}	I_{1n}	Q_n	$\overline{Q}_n$*
↑	l	l	X	L	H
↑	l	h	X	H	L
↑	h	X	l	L	H
↑	h	X	h	H	L

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
* = For 'F398 only

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	'F398	V_{CC} = MAX			25	38	mA
		'F399				22	34	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

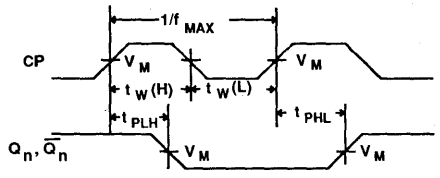
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	Waveform 1	3.0 3.0	5.7 6.5	7.5 8.5	3.0 3.0	8.5 9.0	ns

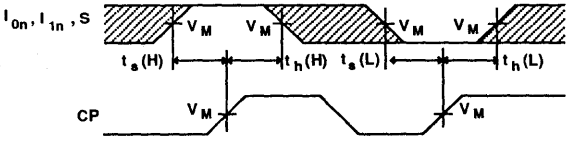
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I_{0n}, I_{1n} to CP	Waveform 2	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I_{0n}, I_{1n} to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S to CP	Waveform 2	7.5 7.5			8.5 8.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S to CP	Waveform 2	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns

AC WAVEFORMS



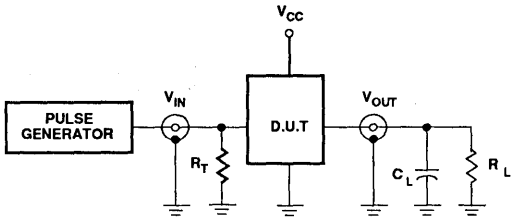
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



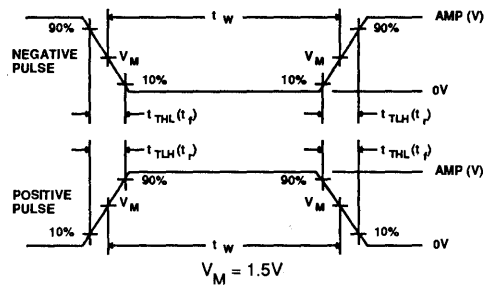
Waveform 2. Data And Select Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F410
Register Stack-16X4 RAM
3-State Output Register

FAST Products

Product Specification

TYPE	TYPICAL ACCESS TIME	TYPICAL SUPPLY CURRENT (TOTAL)
74F410	19.5ns	45mA

FEATURES
- **Edge-triggered output register**
- **Typical access time of 19.5ns**
- **Optimize for register stack operation**
- **3-state outputs**
- **18-pin package**

DESCRIPTION

The 74F410 is a register oriented high speed 64-bit Read/Write Memory organized as 16-words by 4-bits. An edge-triggered 4-bit output register allows new input data to be written while previous data is held. 3-state outputs are provided for maximum versatility. The 74F410 is fully compatible with all TTL families.

ORDERING INFORMATION

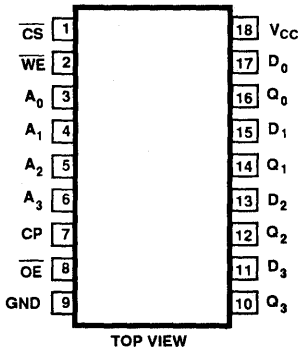
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
18-Pin Plastic DIP (300 mil wide)	N74F410N

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	Address inputs	1.0/1.0	20µA/0.6mA
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{CS}$	Chip Select input (active Low)	1.0/2.0	20µA/1.2mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{WE}$	Write Enable input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/2.0	20µA/1.2mA
Q_0 - Q_3	Data outputs	150/40	3.0mA/24mA

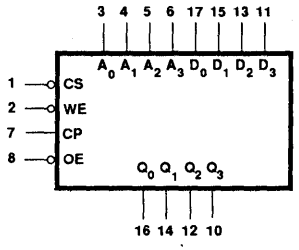
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



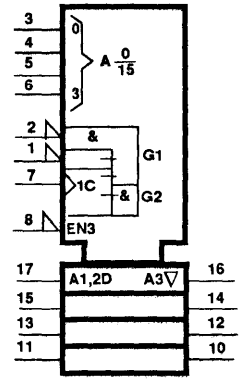
TOP VIEW

LOGIC SYMBOL



V_{CC} = Pin 18
GND = Pin 9

LOGIC SYMBOL(IEEE/IEC)



Register Stack-16 X 4 RAM 3-State Output Register

FAST 74F410

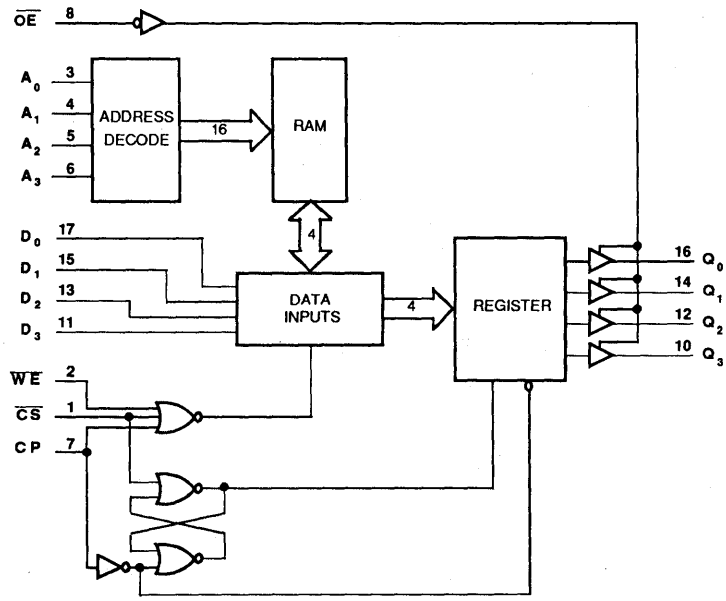
FUNCTIONAL DESCRIPTION

Write Operation--- When the three control inputs, Write Enable ($\overline{WE}$), Chip Select ($\overline{CS}$), and Clock (CP), are Low the information on the data inputs (D_0-D_3) is written into the memory location selected by the address inputs (A_0-A_3). If the input data changes while $\overline{WE}$, $\overline{CS}$, and CP are Low, the contents of the selected memory location follow these changes, provided setup and hold time criteria are met.

Read Operation--- When $\overline{CS}$ is Low, $\overline{WE}$ is High, and CP goes from Low-to-High, the contents of the memory location selected by the address inputs (A_0-A_3) are edge-triggered into the Output Register.

When $\overline{WE}$ is Low, $\overline{CE}$ is Low, and CP goes from Low-to-High, the data at the Data inputs is edge-triggered into the Output Register. The $\overline{OE}$ input controls the output buffers. When $\overline{OE}$ is High the four outputs (Q_0-Q_3) are in a high impedance or OFF-state; when $\overline{OE}$ is Low, the outputs are determined by the state of the Output Register.

LOGIC DIAGRAM



V_{CC} = Pin 18
GND = Pin 9

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	An, Dn, $\overline{WE}$, $\overline{OE}$	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		CP, $\overline{CS}$					-1.2	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC}=MAX			45	70	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Register Stack-16 X 4 RAM 3-State Output Register

FAST 74F410

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	4.0 4.5	6.5 6.5	8.5 9.0	3.5 4.0	9.5 10.0	MHz
t_{PZH} t_{PZL}	Enable time to High or Low level $\overline{OE}$ to Q_n	Waveform 3, 4	3.0 4.5	4.5 6.0	7.5 9.0	2.5 3.5	8.5 9.5	ns
t_{PHZ} t_{PLZ}	Disable time from High or Low level $\overline{OE}$ to Q_n	Waveform 3, 4	2.0 2.0	3.5 3.5	6.0 6.5	1.5 2.0	6.5 7.0	ns

AC SETUP REQUIREMENTS for READ MODE

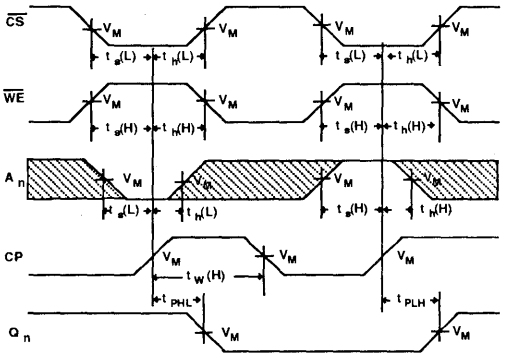
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(L)$	Setup time, Low $\overline{CS}$ to CP[1]	Waveform 1	4.0			4.5		ns
$t_h(L)$	Hold time, Low $\overline{CS}$ to CP[1]	Waveform 1	3.5			4.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n to CP[1]	Waveform 1	13.0 13.0			15.0 15.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n to CP[1]	Waveform 1	0 0			0 0		ns
$t_s(L)$	Setup time, High $\overline{WE}$ to CP[1]	Waveform 1	13.0			15.0		ns
$t_h(L)$	Hold time, High $\overline{WE}$ to CP[1]	Waveform 1	0			0		ns
$t_w(L)$	CP Pulse width, Low	Waveform 1	5.0			6.0		ns

NOTE: 1. Low-to-High clock transition

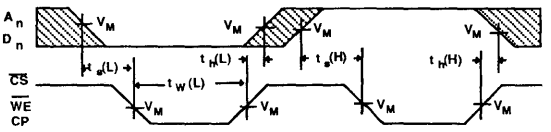
AC SETUP REQUIREMENTS for WRITE MODE

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n to $\overline{WE}$, $\overline{CS}$, CP	Waveform 2	0 0			0 0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n to $\overline{WE}$, $\overline{CS}$, CP	Waveform 2	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{WE}$, $\overline{CS}$, CP	Waveform 2	6.0 6.0			8.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{WE}$, $\overline{CS}$, CP	Waveform 2	0 0			0 0		ns
$t_w(L)$	$\overline{WE}$ Pulse width, Low	Waveform 2	7.0			8.0		ns
$t_w(L)$	$\overline{CS}$ Pulse width, Low	Waveform 2	6.0			7.0		ns
$t_w(L)$	CP Pulse width, Low	Waveform 2	7.0			8.0		ns

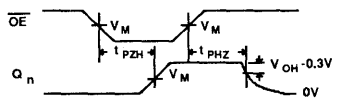
AC WAVEFORMS



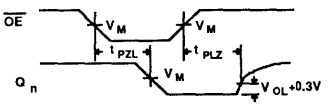
Waveform 1. Read Cycle Timing



Waveform 2. Write CycleTiming



Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level

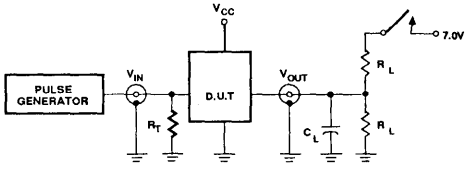


Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

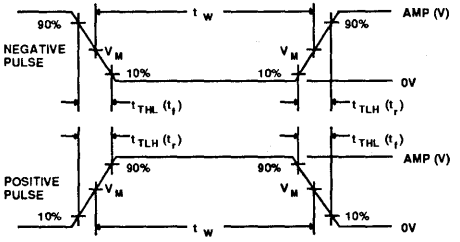
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F412/432
Multi-Mode Buffered Latches

74F412 Multi-Mode Buffered Latch, Non-Inverting (3-State)
74F432 Multi-Mode Buffered Latch, Inverting (3-State)

Product Specification

FEATURES

- **Status flip-flop for interrupt commands**
- **Asynchronous or latched receiver modes**
- * **'F412 Non-Inverting**
  'F432 Inverting
- **3-state outputs**
- **300 mil wide Slim Dip package**
- **Functional equivalent to Intel 8212 except that 'F432 has inverting outputs**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F412	8.0ns	45mA
74F432	9.0ns	50mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F412N, N74F432N
24-Pin Plastic SOL	N74F412D, N74F432D

DESCRIPTION

The 'F412/'F432 have 8-bit latches with 3-state output buffers. Also included is a status flip-flop for providing device-busy or request-interrupt commands.

Separate mode (M) and Select ($\overline{S}_0$, S_1) inputs allow data to be stored with the outputs enabled or disabled. The devices can also be operated in a fully transparent mode.

Both 'F412 and 'F432 are functional equivalent to the Intel 8212 except that 'F432 has the inverting outputs.

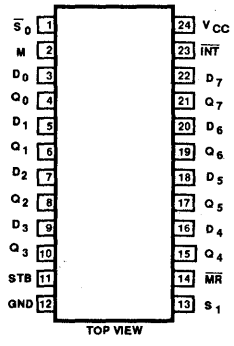
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0- D_7	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{S}_0$, S_1	Select inputs	1.0/1.0	20µA/0.6mA
STB	Strobe input	1.0/1.0	20µA/0.6mA
M	Mode Control input	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input	1.0/1.0	20µA/0.6mA
$\overline{INT}$	Interrupt Output	50/33	1mA/20mA
Q_0- Q_7	Data Latched Outputs	150/40	3mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

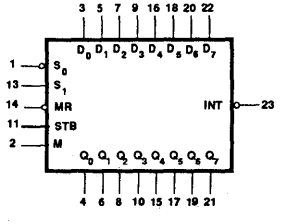
PIN CONFIGURATION

'F412



LOGIC SYMBOL

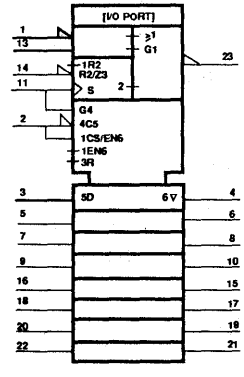
'F412



V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

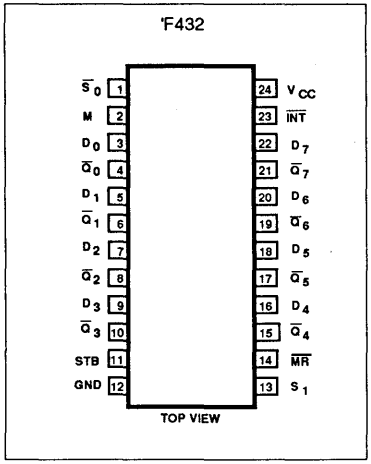
'F412



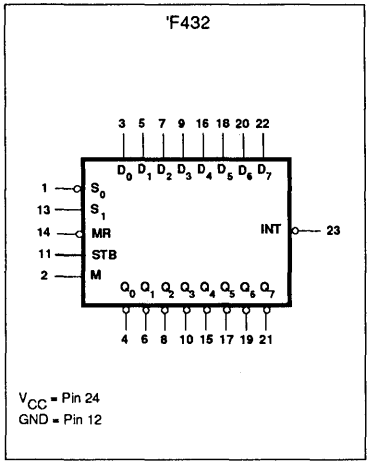
Multi-Mode Buffered Latches

FAST 74F412/432

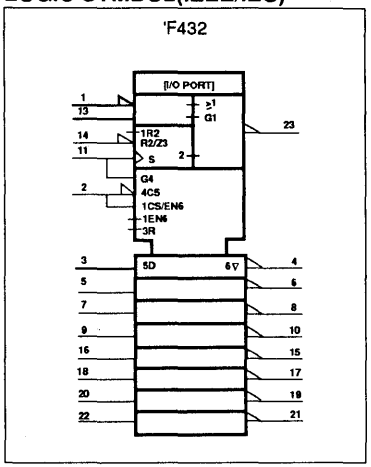
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



This high performance eight-bit parallel expandable buffer latch incorporates package and mode selection inputs and an edge-triggered status flip-flop designed specifically for implementing bus organized input/output ports. The 3-state data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides busy or request interrupt commands. The eight data latches are fully transparent when the internal gate enable, G, input is High and the outputs are enabled. Latch transparency is selected by the mode control (M), select ($\overline{S}_0$, S_1), and the strobe (STB) inputs and during transparency each data output (Q_n) follows its respective data input (D_n). This mode of operation can be terminated by clearing, de-selecting, or holding the data latches.

An input mode or an output mode is selectable from the M input. In the input mode, M=L, the eight data at the inputs are enabled when the strobe is High regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken Low, the latches will store the most recently setup data.

In the output mode, M=H, the output buffers are enabled regardless of any other control input. During the output mode the contents of the register is under control of the select ($\overline{S}_0$ and S_1) inputs.

FUNCTION TABLE for Data Latches

INPUTS					DATA IN	OUTPUTS		OPERATING MODE
$\overline{MR}$	M	$\overline{S}_0$	S_1	STB		'F412	'F432	
L	H	H	X	X	X	L	H	Clear
L	L	L	H	L	X	L	H	
X	L	X	L	X	X	Z	Z	De-select
X	L	H	X	X	X	Z	Z	
H	H	H	X	X	X	Q_0	$\overline{Q}_0$	Hold
H	L	L	H	L	X	Q_0	$\overline{Q}_0$	
H	H	L	H	X	L	L	H	Data Bus
H	H	L	H	X	H	H	L	
H	L	L	H	H	L	L	H	Data Bus
H	L	L	H	H	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

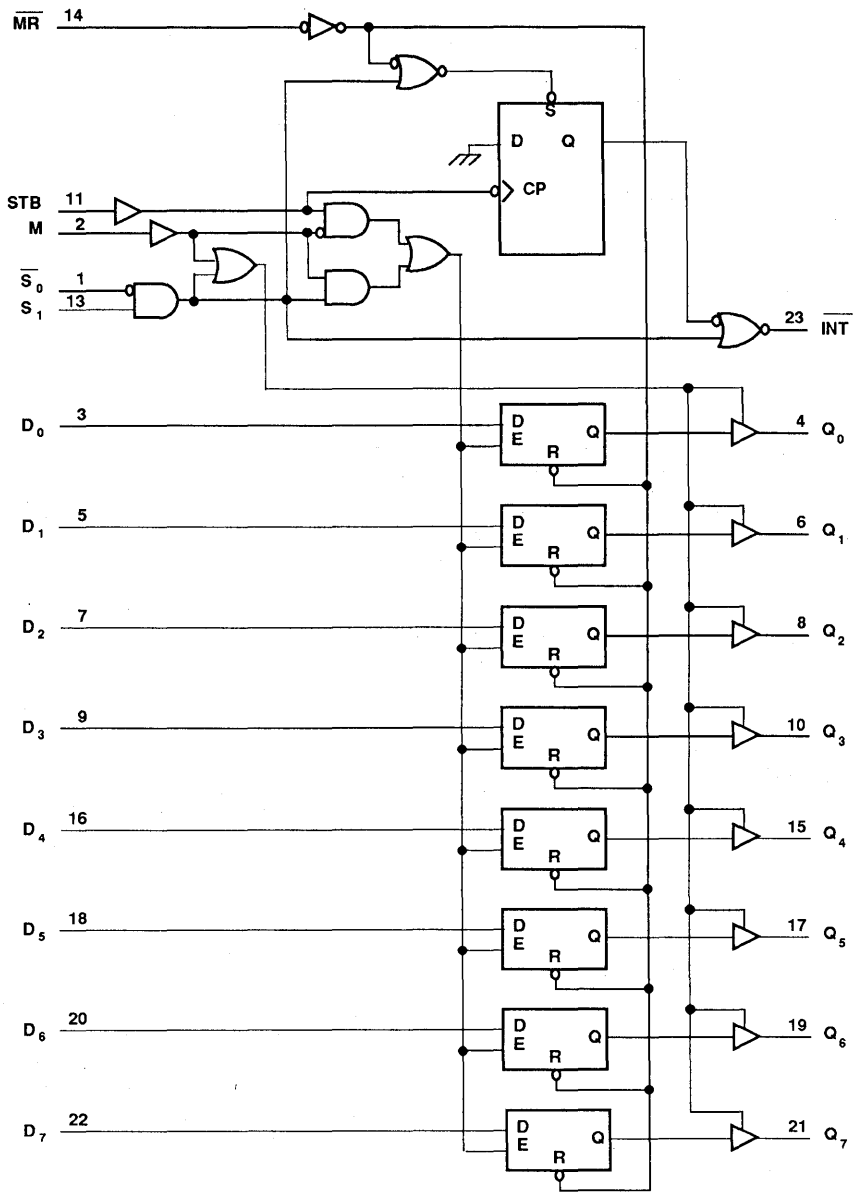
FUNCTION TABLE for Status Flip-Flop

INPUTS				$\overline{INT}$
$\overline{MR}$	$\overline{S}_0$	S_1	STB	
L	H	X	X	H
L	X	L	X	H
H	X	X	↓	L
H	L	H	X	L

H = High voltage level
L = Low voltage level
↓= High-to-Low transition

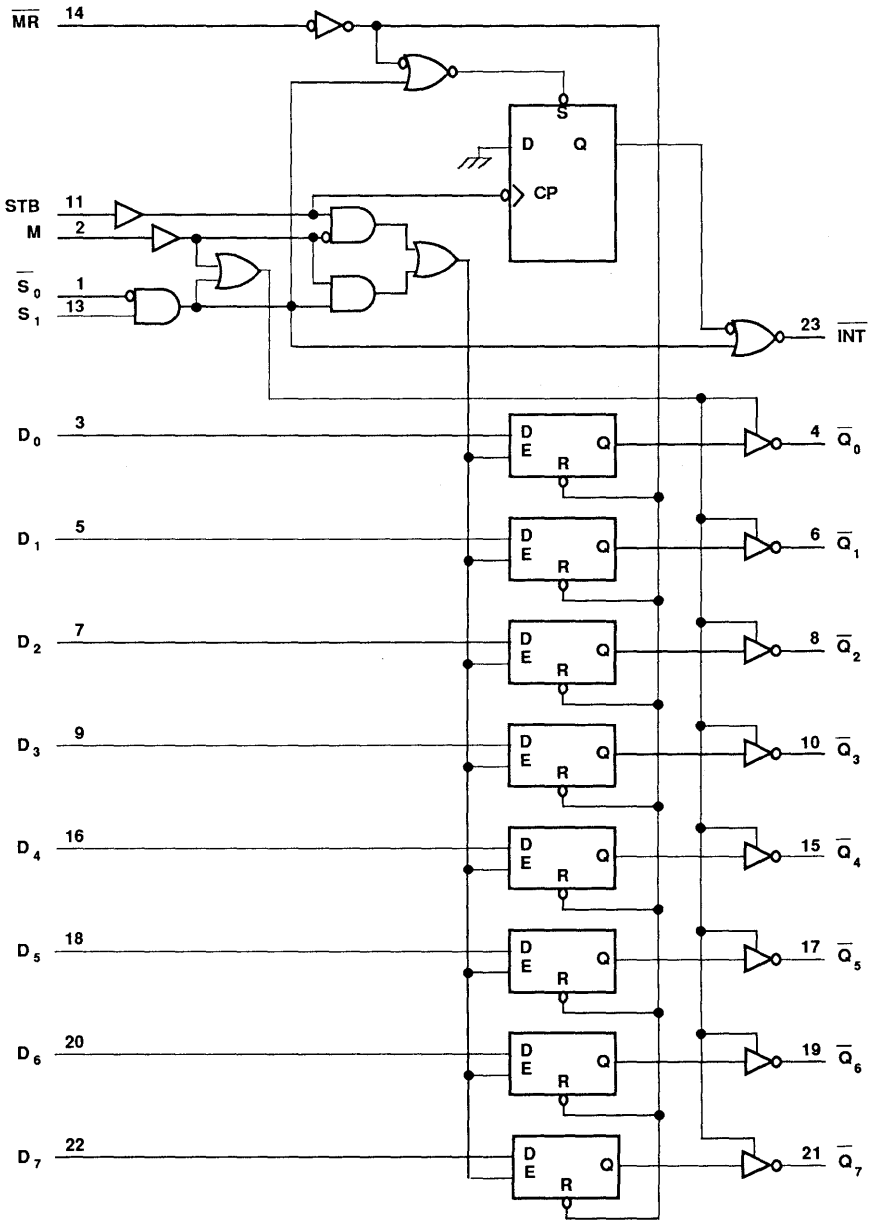
X = Don't care

LOGIC DIAGRAM for 'F412



V_{CC} =Pin 24
GND =Pin 12

.OGIC DIAGRAM for 'F432



V_{CC} =Pin 24
GND =Pin 12

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	$\overline{INT}$	40	mA
		Q_0- Q_7	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	$\overline{INT}$			-1	mA
		Q_0- Q_7			-3	mA
I_{OL}	Low-level output current	$\overline{INT}$			20	mA
		Q_0- Q_7			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -1mA	±10% V_{CC}	2.5			V
						±5% V_{CC}	2.7	3.4		V
					I_{OH} = -3mA	±10% V_{CC}	2.4			V
						±5% V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} =MAX	±10% V_{CC}		0.30	0.50	V
						±5% V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7 V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5 V					-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	'F412	I_{CCH}	V_{CC} = MAX				35	50	mA
			I_{CCL}					45	60	mA
			I_{CCZ}					45	60	mA
		'F432	I_{CCH}	V_{CC} = MAX				40	55	mA
			I_{CCL}					50	70	mA
			I_{CCZ}					50	65	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 74F412

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	3.5 2.0	6.0 3.5	8.5 6.5	3.0 2.0	9.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_0$, S_1 or STB to Q_n	Waveform 1, 2	7.5 7.0	13.0 9.0	17.0 14.0	7.0 6.5	18.5 15.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_0$ or S_1 to $\overline{INT}$	Waveform 1, 2	3.0 3.0	6.0 6.5	9.5 10.5	3.0 3.0	10.5 11.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 1	6.0	8.0	12.0	5.5	13.0	ns
t_{PHL}	Propagation delay STB to $\overline{INT}$	Waveform 2	6.5	10.0	13.0	5.5	15.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level $\overline{S}_0$ to Q_n	Waveform 5 Waveform 6	7.0 7.0	9.0 10.0	12.5 13.5	6.0 6.0	14.0 15.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level $\overline{S}_0$ to Q_n	Waveform 5 Waveform 6	4.5 6.5	7.5 12.0	10.5 15.0	4.0 6.0	12.0 16.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level S_1 to Q_n	Waveform 5 Waveform 6	6.0 6.0	10.0 9.0	13.0 12.0	5.0 5.5	14.0 13.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level S_1 to Q_n	Waveform 5 Waveform 6	4.0 6.5	6.0 10.0	9.5 13.5	3.5 6.0	10.5 15.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level M to Q_n	Waveform 5 Waveform 6	5.0 5.0	8.5 8.5	11.0 11.0	4.5 4.5	12.0 12.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level M to Q_n	Waveform 5 Waveform 6	4.0 6.0	6.5 9.5	9.0 12.5	3.5 5.5	10.0 14.0	ns

AC SETUP REQUIREMENTS for 74F412

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to $\overline{S}_0$, S_1, STB or M	Waveform 3	0 0			1.0 1.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to $\overline{S}_0$, S_1, STB or M	Waveform 3	8.0 8.0			9.0 9.0		ns
t_w(H) t_w(L)	$\overline{S}_0$, S_1, STB or M Pulse width, High or Low	Waveform 3	8.0 8.0			9.0 9.0		ns
t_w(L)	$\overline{MR}$ Pulse width, Low	Waveform 4	8.0			9.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to $\overline{S}_0$, S_1, M, STB	Waveform 4	0			0		ns

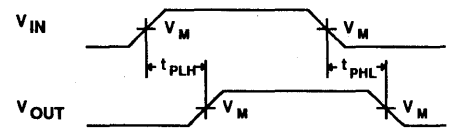
AC ELECTRICAL CHARACTERISTICS for 74F432

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	4.5 2.5	7.5 4.5	10.5 7.0	4.0 2.5	12.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_0$, S_1 or STB to Q_n	Waveform 1, 2	8.5 6.0	14.0 9.5	17.0 13.0	8.0 5.5	19.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_0$ or S_1 to $\overline{INT}$	Waveform 1, 2	3.0 3.5	6.0 6.5	9.5 10.5	2.5 3.0	10.5 10.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 1	8.0	12.0	16.0	7.5	17.0	ns
t_{PHL}	Propagation delay STB to $\overline{INT}$	Waveform 2	7.0	10.0	13.5	6.5	14.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level $\overline{S}_0$ or S_1 to Q_n	Waveform 5 Waveform 6	6.0 6.0	9.0 11.0	12.5 14.0	5.5 5.5	14.0 15.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level $\overline{S}_0$ or S_1 to Q_n	Waveform 5 Waveform 6	4.0 6.0	7.5 11.5	11.5 15.0	3.5 5.5	12.5 16.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level M to Q_n	Waveform 5 Waveform 6	5.0 6.0	7.5 8.0	11.0 11.5	4.5 5.5	12.0 13.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level M to Q_n	Waveform 5 Waveform 6	3.5 6.0	6.0 10.0	9.5 13.0	3.0 5.5	10.5 13.5	ns

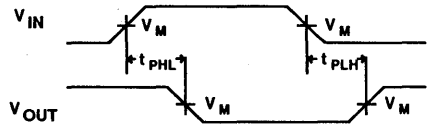
AC SETUP REQUIREMENTS for 74F432

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to $\overline{S}_0$, S_1, STB or M	Waveform 3	0 0			1.0 1.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to $\overline{S}_0$, S_1, STB or M	Waveform 3	9.0 8.0			9.5 8.5		ns
t_w(H) t_w(L)	$\overline{S}_0$, S_1, STB or M Pulse width, High or Low	Waveform 3	8.0 8.0			9.0 9.0		ns
t_w(L)	$\overline{MR}$ Pulse width, Low	Waveform 4	8.0			9.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to $\overline{S}_0$, S_1, M, STB	Waveform 4	0			0		ns

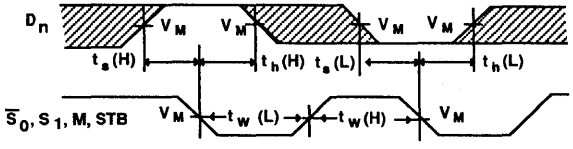
AC WAVEFORMS



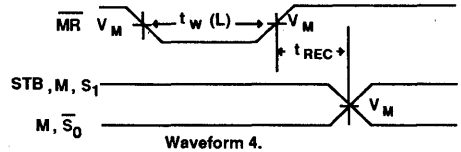
Waveform 1. Propagation Delay, Non-Inverting Outputs



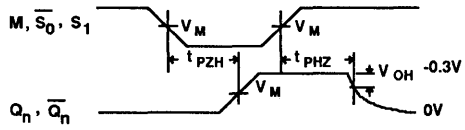
Waveform 2. Propagation Delay, Inverting Outputs



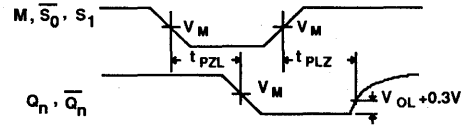
Waveform 3. Setup And Hold Times



Waveform 4.
Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Strobe Recovery Time



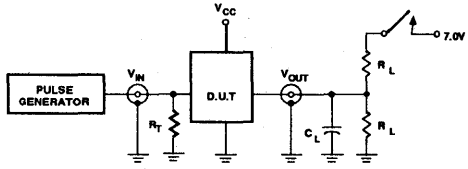
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

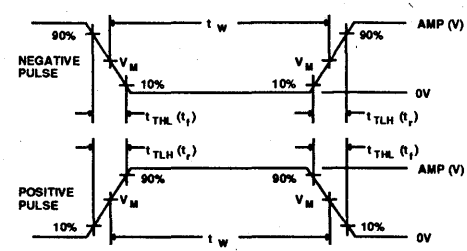
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F[3]	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F455, 74F456
Buffers/Drivers

74F455 Octal Buffer/Driver With Parity, Inverting (3-State)
74F456 Octal Buffer/Driver With Parity, Non-Inverting (3-State)

Product Specification

FAST Products

FEATURES

- **High impedance NPN base inputs for reduced loading (40μA in High and Low states)**
- **'F455 combines 'F240 and 'F280A functions in one package**
- **'F456 combines 'F244 and 'F280A functions in one package**
- **'F455 and 'F456 are center pin versions of the 'F655A and 'F656A respectively**
- **'F455 Inverting**
  'F456 Non-Inverting
- **3-state outputs sink 64mA and source 15mA**
- **24-pin plastic Slim DIP (300mil) package**
- **Broadside pinout simplifies PC board layout**

DESCRIPTION

The 'F455 and 74F456 are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F455	6.5ns	64mA
74F456	7.5ns	64mA

ORDERING INFORMATION

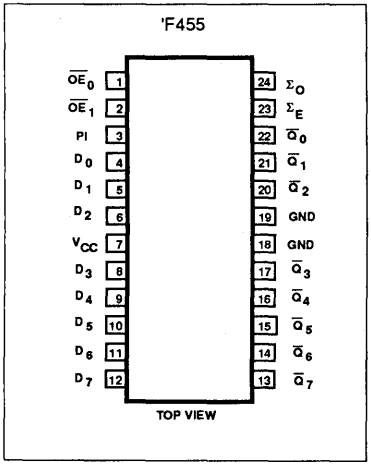
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F455N, N74F456N
24-Pin Plastic SOL	N74F455D, N74F456D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

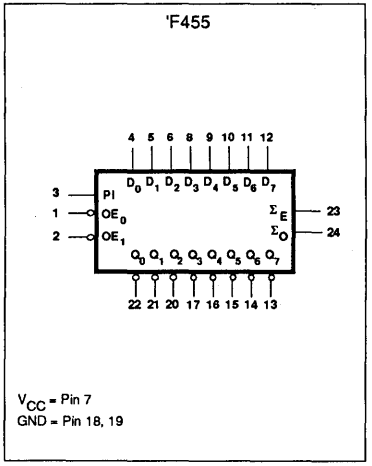
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0- D_7	Data inputs	2.0/0.066	40μA/40μA
PI	Parity input	1.0/0.033	20μA/20μA
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable inputs (active Low)	1.0/0.033	20μA/20μA
Σ_E, Σ_O	Parity outputs	750/106.7	15mA/64mA
$\overline{Q}_0$- $\overline{Q}_7$	Data outputs ('F455)	750/106.7	15mA/64mA
Q_0- Q_7	Data outputs ('F456)	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

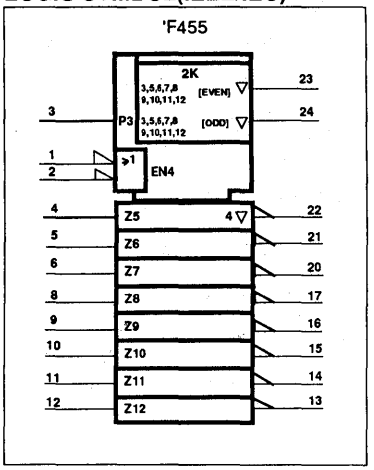
PIN CONFIGURATION



LOGIC SYMBOL

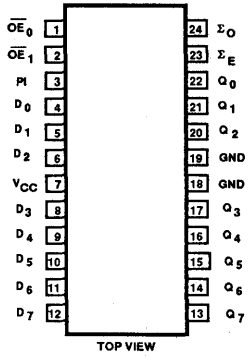


LOGIC SYMBOL(IEEE/IEC)



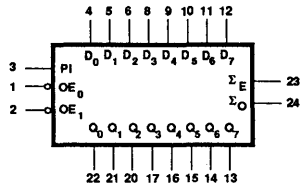
PIN CONFIGURATION

'F456



LOGIC SYMBOL

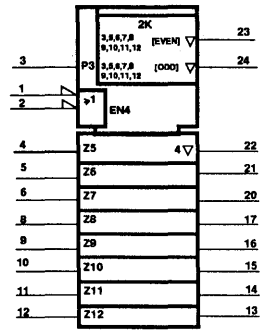
'F456



V_{CC} = Pin 7
GND = Pin 18, 19

LOGIC SYMBOL(IEEE/IEC)

'F456



FUNCTION TABLE

INPUTS			OUTPUTS	
			'F455	'F456
$\overline{OE}_0$	$\overline{OE}_1$	D_n	$\overline{Q}_n$	Q_n
L	L	L	H	L
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z

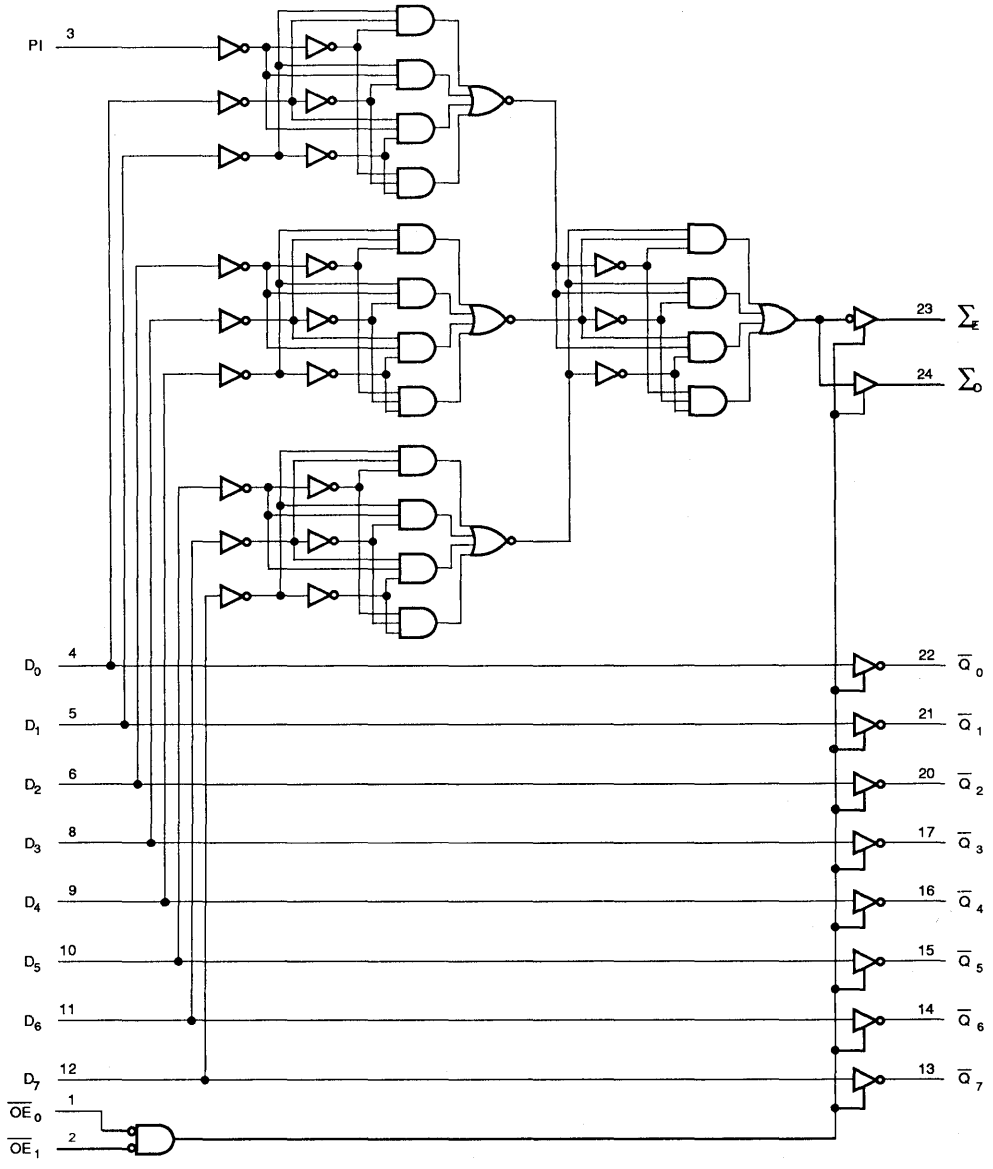
H= High voltage level
L= Low voltage level
X=Don't care
Z =High impedance "off" state

FUNCTION TABLE for PARITY OUTPUTS

INPUTS	OUTPUTS	
Number of inputs High (PI, D_0-D_7)	Σ_E	Σ_O
Even ------ 0, 2, 4, 6, 8	H	L
Odd ------1, 3, 5, 7, 9	L	H
Any $\overline{OE}_n$=High	Z	Z

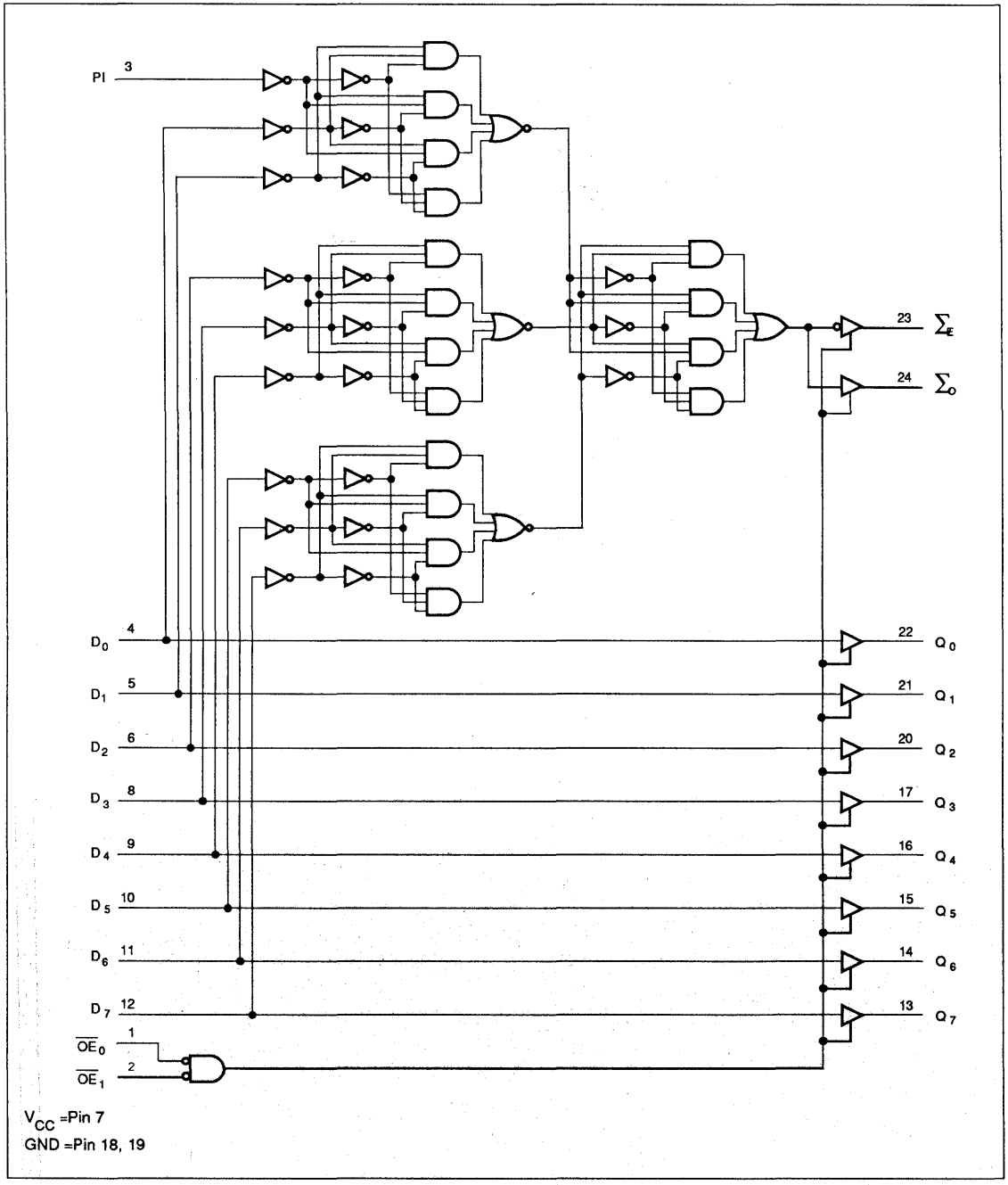
H= High voltage level
L= Low voltage level
X=Don't care
Z =High impedance "off" state

LOGIC DIAGRAM for 'F455



V_{CC} =Pin 7
GND =Pin 18, 19

LOGIC DIAGRAM for 'F456



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
				I_{OH}=-15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	D_n	V_{CC} = MAX, V_I = 2.7V					40	µA
		PI, $\overline{OE}_n$						20	µA
I_{IL}	Low-level input current	D_n	V_{CC} = MAX, V_I = 0.5V					-40	µA
		PI, $\overline{OE}_n$						-20	µA
I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				50	80	mA
		I_{CCL}					78	110	mA
		I_{CCZ}					63	90	mA

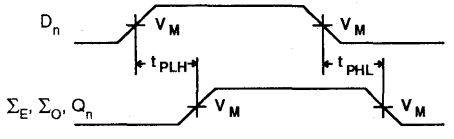
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

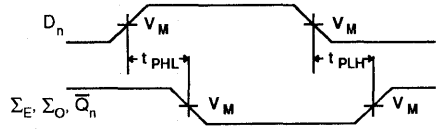
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	'F455	Waveform 2	2.0 1.0	4.5 2.0	6.5 4.0	2.0 1.0	7.5 4.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	'F456	Waveform 1	2.0 2.5	4.5 5.0	6.5 7.0	2.0 2.5	7.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Σ_E, Σ_O		Waveform 1, 2	5.5 5.5	10.0 11.0	13.0 14.5	5.5 5.5	14.0 16.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	4.0 4.0	7.0 8.0	9.5 10.5	4.0 4.0	10.5 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 3 Waveform 4	1.5 2.0	4.0 5.0	6.5 7.5	1.5 2.0	7.5 8.0	ns

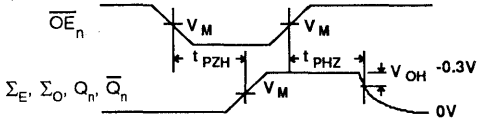
AC WAVEFORMS



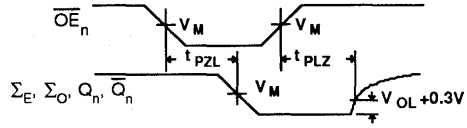
Waveform 1. Propagation Delay, Non-Inverting Outputs



Waveform 2. Propagation Delay, Inverting Outputs



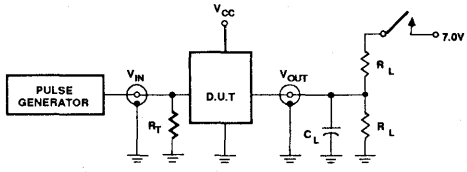
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

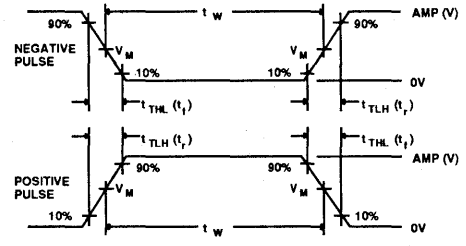
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F521
8-Bit Identity Comparator

FAST Products

Comparator

Product Specification

FEATURES
- **Compares two 8-bit words in 6.5ns typical**
- **Expandable to any word length**
- **High speed version of ALS688**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F521	7.0ns	24mA

DESCRIPTION

The 74F521 is an expandable 8-bit comparator. It compares two words of up to 8 bits each and provides a Low output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active-Low enable input.

ORDERING INFORMATION

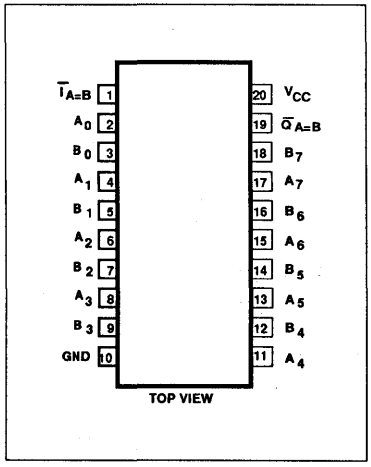
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F521N
20-Pin Plastic SO	N74F521D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

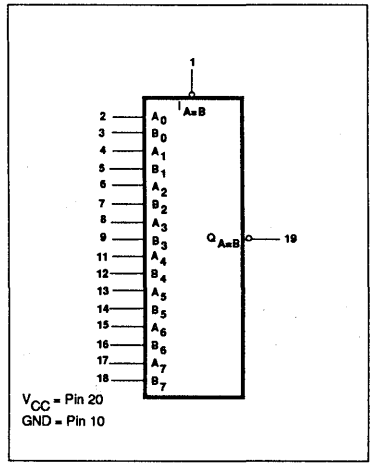
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7	Word A inputs	1.0/1.0	20µA/0.6mA
B_0- B_7	Word B inputs	1.0/1.0	20µA/0.6mA
$\overline{I}_{A=B}$	Expansion or Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{Q}_{A=B}$	Identity output (active Low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

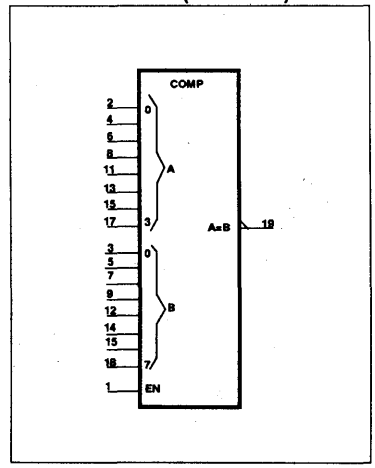
PIN CONFIGURATION



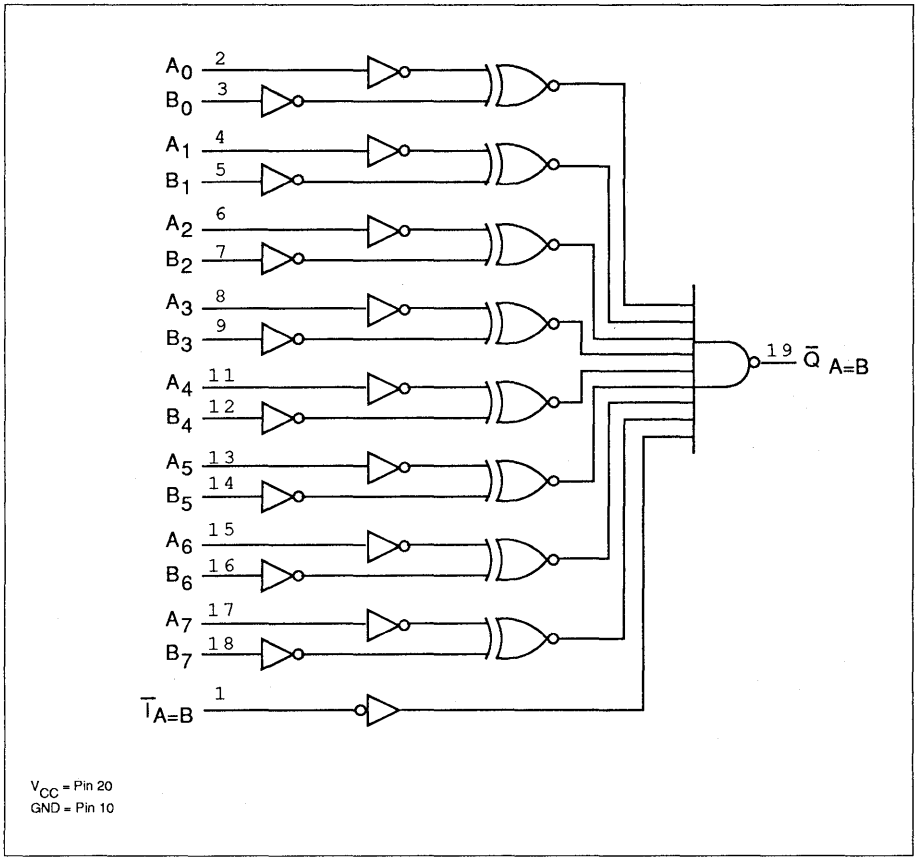
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM

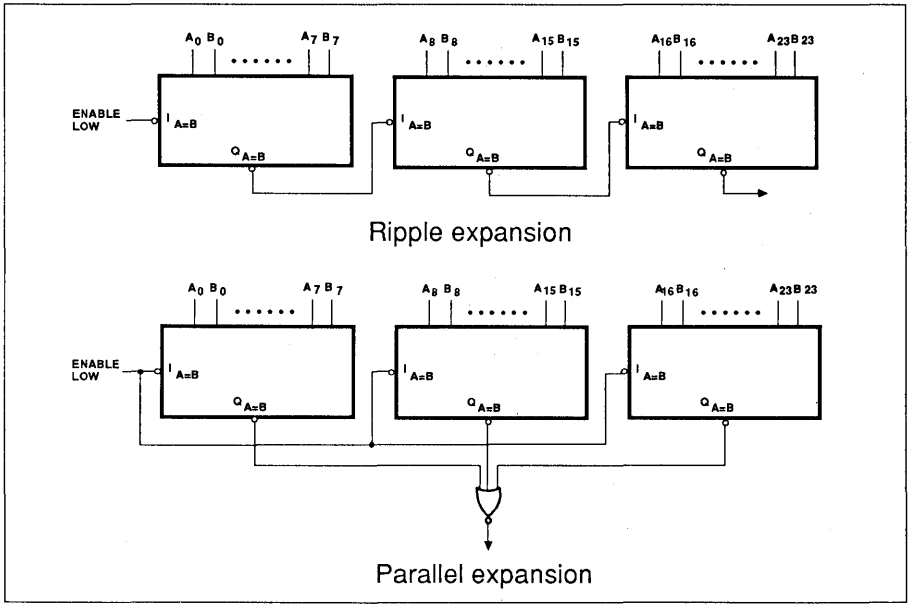


FUNCTION TABLE

INPUTS		OUTPUT
$\overline{I}_{A=B}$	A, B	$\overline{Q}_{A=B}$
L	A=B*	L
L	A≠B	H
H	A=B*	H
H	A≠B	H

H = High voltage level
L = Low voltage level
X = Don't care
*$A_0=B_0$, $A_1=B_1$, $A_2=B_2$, etc.

APPLICATIONS



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

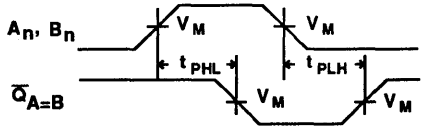
SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
			±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX			24	36	mA
	Supply current (total) I_{CCL}				24	36	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

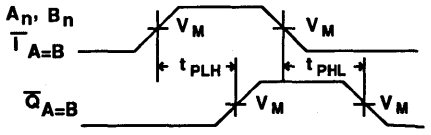
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to $\overline{Q}_{A=B}$	Waveform1,2	3.5 3.0	8.0 8.0	9.5 9.0	3.5 2.5	11.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{I}_{A=B}$ to $\overline{Q}_{A=B}$	Waveform 2	3.0 3.5	5.0 6.5	6.5 7.0	3.0 3.5	7.5 8.0	ns

AC WAVEFORMS



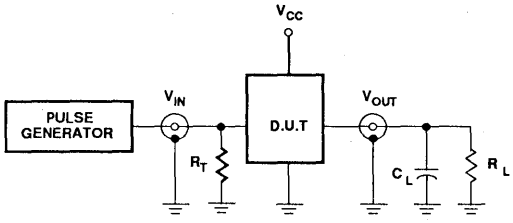
Waveform 1. For Inverting Outputs



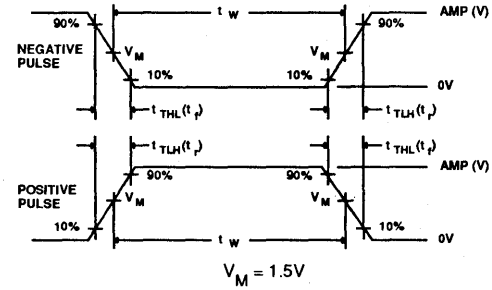
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F524
Comparator

FAST Products

8-Bit Register Comparator (Open Collector+3-State)
Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F524	65MHz	110mA

FEATURES

- **8-Bit bidirectional register with bus-oriented input-output**
- **Independent serial input-output to register**
- **Register bus comparator with 'equal to', 'greater than' and 'less than' outputs**
- **Cascadable in groups of 8-bits**
- **Open collector comparator outputs for AND-wired expansion**
- **Two's complement or magnitude compare**

DESCRIPTION

The 74F524 is an 8-bit bidirectional register with parallel input and output plus serial input and output progressing from LSB to MSB. All data inputs, serial and parallel, are loaded by the rising edge of the clock. The device functions are controlled by two control lines (S_0,S_1) to execute shift, load, hold and read out. An 8-bit comparator examines the data stored in the registers and on the data bus. Three true-High, open collector outputs representing 'register equal to bus', 'register greater than bus' and 'register less than bus' are provided. These outputs can be disabled to the OFF state by the use of Status Enable ($\overline{SE}$). A mode control has also been provided to allow Two's Complement as well as magnitude compare. Linking inputs are provided for expansion to longer words.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F524N
20-Pin Plastic SOL[1]	N74F524D

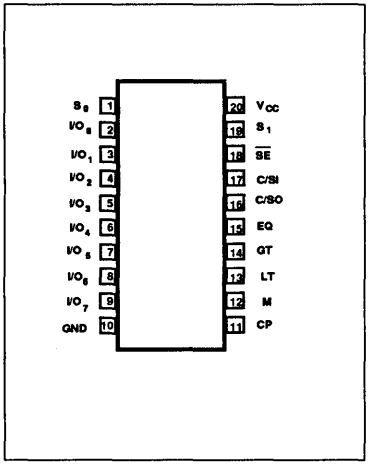
NOTE:
1.Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

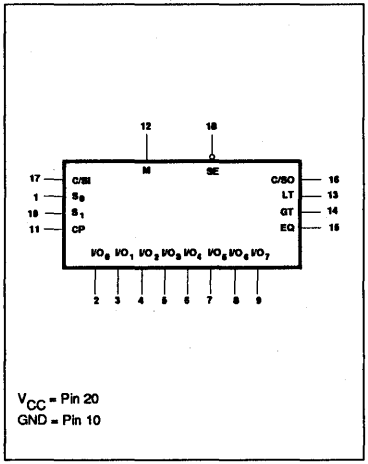
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/On	Parallel data inputs	3.5/1.0	70μA/0.6mA
S_0, S_1	Mode select inputs	1.0/1.0	20μA/0.6mA
C/SI	Status priority or serial data input	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{SE}$	Status enable input (active Low)	1.0/1.0	20μA/0.6mA
M	Compare mode select input	1.0/1.0	20μA/0.6mA
I/O_n	3-state parallel data outputs	150/40	3.0mA/24mA
C/SO	Status priority of serial data output	50/33	1.0mA/20mA
LT	Register less than bus output	OC/33	OC/20mA
EQ	Register equal to bus output	OC/33	OC/20mA
GT	Register greater than bus output	OC/33	OC/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC=Open Collector

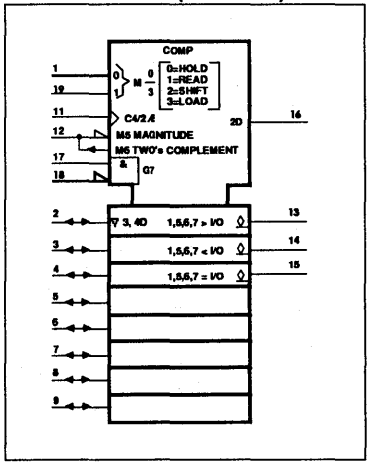
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



FUNCTIONAL DESCRIPTIONS

The 'F524 contains eight D-type flip-flops connected as a shift register with provision for either parallel or serial loading. Parallel data may be read from or loaded into the registers via the data bus I/O_0-I/O_7. Serial data is entered from the C/SI input and may be shifted into the register and out through the C/SO output. Both parallel and serial data entry occurs on the rising edge of the clock (CP). The operation of the shift register is controlled by two signals, S_0 and S_1, according to the Select Function Table. The 3-state parallel output buffers are enabled only in the READ mode.

SELECT FUNCTION TABLE

S_0	S_1	OPERATION
L	L	HOLD-Retains data in shift register
L	H	READ- Read contents in register onto data bus
H	L	SHIFT- Allows serial shifting on next rising clock edge
H	H	LOAD-Load data on bus into register

H=High voltage level
L=Low voltage level

One port of an 8-bit comparator is attached to the data bus while the other port is tied to the outputs of the internal register. Three active-OFF Open Collector outputs indicate whether the contents held in the shift register are 'greater than' (GT), 'less than' (LT), or 'equal to' (EQ) the data on the input bus. A High signal on the Status Enable ($\overline{SE}$) input disables these outputs to the OFF state. A mode control (M) input allows selection between a straightforward magnitude compare or a comparison between Two's complement numbers.

NUMBER REPRESENTAION SELECT TABLE

M	OPERATION
L	Magnitude compare
H	Two's Complement compare

H=High voltage level
L=Low voltage level

For 'greater than' or 'less than' detection, the C/SI input must be held High,as indicated in the Status Function Table. The internal logic is arranged such that a Low signal on the C/SI input places the 'greater than' and 'less than' outputs in their off state. (Note that this off state serves also as the active state when C/SI is High. It is intended for use in expansion to word lengths greater than 8 bits using multiple

STATUS FUNCTION TABLE (Hold mode)

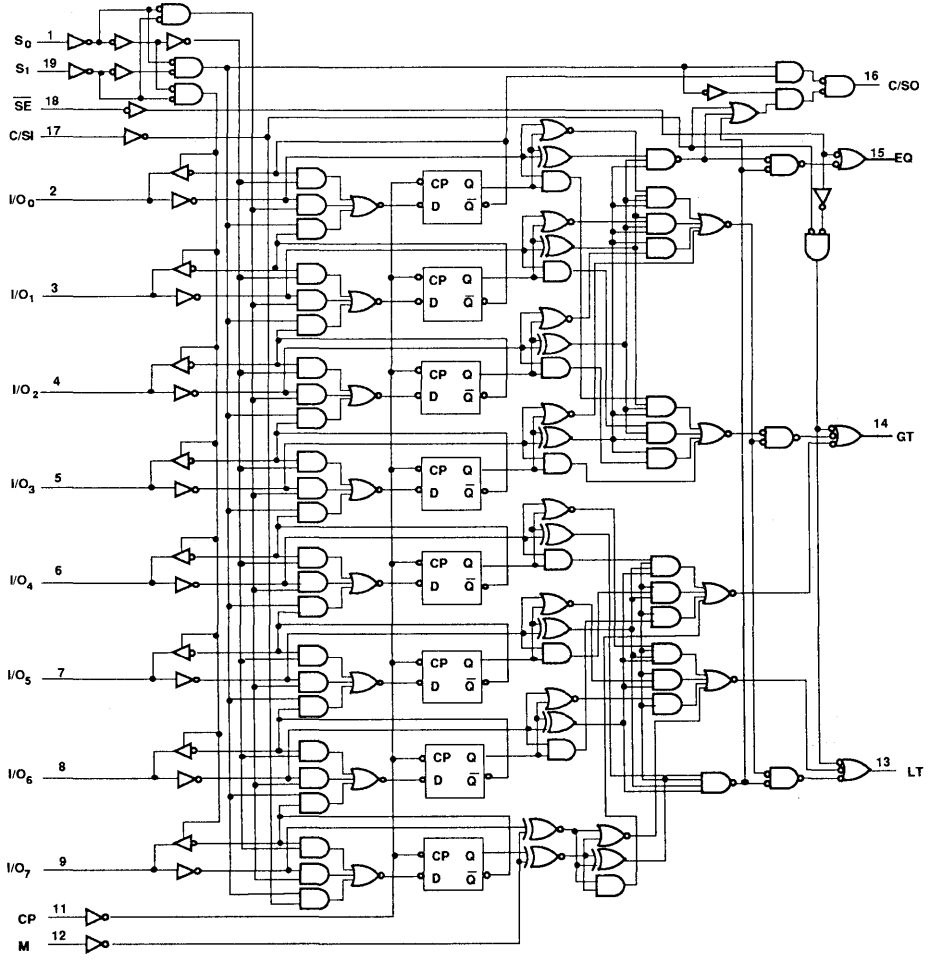
INPUTS			OUTPUTS			
$\overline{SE}$	C/SI	Data comparison	EQ	GT	LT	C/SO
H	H	X	H	H	H	①
H	L	X	H	H	H	L
L	L	O_A-O_H >I/O_0-I/O_7	L	H	H	L
L	L	O_A-O_H =I/O_0-I/O_7	H	H	H	L
L	L	O_A-O_H <I/O_0-I/O_7	L	H	H	L
L	H	O_A-O_H >I/O_0-I/O_7	L	H	L	L
L	H	O_A-O_H =I/O_0-I/O_7	H	L	L	H
L	H	O_A-O_H <I/O_0-I/O_7	L	L	H	L

①= Low if data are not equal, otherwise High
H = High voltage level
L = Low voltage level
X = Don't care

74F524's as explained in the next 3 paragraphs.) The C/SO output will be forced High if the 'equal to' status condition exists; otherwise, C/SO will be held Low.

Word length expansion (in groups of 8 bits) can be achieved by connecting the C/SO output of the more significant byte to the C/SI input of the next less significant byte and also to its own $\overline{SE}$ input (see Figure 1). The CS/I input of the most significant device is held High while the $\overline{SE}$ input of the least significant device is held Low. The corresponding status outputs are AND-wired together. In the case of two's complement number compare, only the Mode input to the most significant device should be High. The Mode inputs to all other cascaded devices are held Low.
Suppose that an inequality condition is detected in the most signicant device. Assuming that the byte stored in the register is greater than the byte on the data bus, then the EQ and LT outputs will be pulled Low, whereas the GT output will float High. Also, the CS/O output of the most significant device will be forced Low, disabling the subsequent devices but enabling its own status outputs. The correct status condition is thus indicated. The same applies if the registered byte is less than the data byte, only in this case the EQ and GT outputs go Low, whereas LT output floats High.
If an equality condition is detected in the most significant device, its C/SO output is forced High. This enables the next less significant device and disables its own status outputs. In this way, the status output priority is handed down to the next less significant device which now effectively becomes the most significant byte. The worst case propagation delay for a compare operation involving '**n**' cascaded 'F524s will be when an equality condition is detected in all but the least significant byte. In this case, the status priority has to ripple all the way down the chain before the correct status output is established. Typically, this will take 35+6(**n**-2) ns.

LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10

APPLICATION

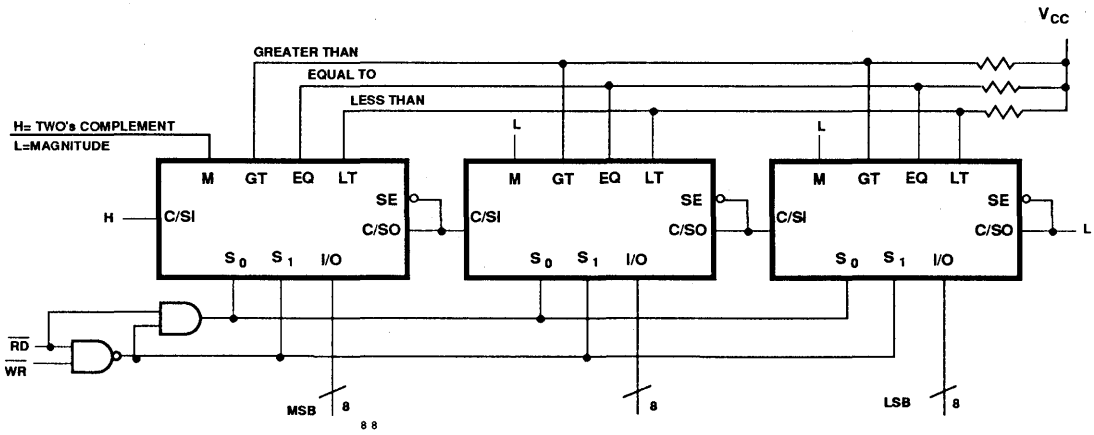


Figure 1. Cascading 'F524s for comparing longer words

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	All except I/O	40	mA
		I/O only	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_K	Input clamp current				-18	mA
V_{OH}	High level output voltage	LT, EQ, GT only			4.5	V
I_{OH}	High-level output current	Not LT, EQ, GT, C/SO			-3	mA
		C/SO only			-1	mA
I_{OL}	Low-level output current	All except I/O			20	mA
		I/O only			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current	LT, EQ, GT only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OH}	High-level output voltage	C/SO only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=MAX	±10%V_{CC}	2.5			V
		I/O_n only			±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	I/O_n	V_{CC} =5.5V, V_I =5.5V					1	mA
		Except I/O_n	V_{CC} = 5.5V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	Except I/O_n	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied	I/O_n only	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-0.6	mA
I_{OS}	Short-circuit output current[3]	Except LT, EQ, GT	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX				110	150	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

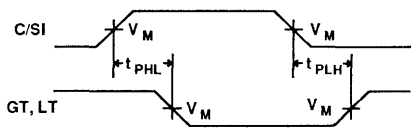
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 4	50	65		45		MHz
t_{PLH} t_{PHL}	Propagation delay I/O_n to EQ	Waveform 2	9.0 4.5	12.5 7.5	20.0 12.0	9.0 4.5	21.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay I/O_n to GT	Waveform 2	8.5 6.5	11.0 9.5	19.0 16.5	8.5 6.5	20.0 17.5	ns
t_{PLH} t_{PHL}	Propagation delay I/O_n to LT	Waveform 2	8.0 6.0	11.0 10.5	19.5 16.0	8.0 6.0	20.5 17.0	ns
t_{PLH} t_{PHL}	Propagation delay I/O_n to C/SO	Waveform 2	7.0 4.5	13.0 8.0	20.0 14.0	7.0 4.5	21.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to EQ	Waveform 4	10.0 4.0	16.0 10.0	25.0 16.5	10.0 4.0	26.0 17.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to GT	Waveform 4	10.0 8.5	14.0 14.5	21.0 22.0	10.0 8.5	22.0 23.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to LT	Waveform 4	9.0 5.5	16.0 14.0	25.0 18.0	9.0 5.5	26.0 19.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to C/SO (Compare)	Waveform 4	8.5 8.5	16.0 16.0	21.0 21.0	8.5 8.5	22.0 22.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to C/SO (Serial shift)	Waveform 4	5.0 4.5	10.0 9.0	13.0 11.5	5.0 4.5	14.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay C/SI to GT	Waveform 1	9.0 2.5	12.5 4.5	19.0 8.5	9.0 2.0	20.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay C/SI to LT	Waveform 1	8.0 2.5	12.0 6.0	20.0 8.5	8.0 2.5	21.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to C/SO	Waveform 2	6.5 5.5	8.0 10.0	14.5 18.0	6.5 5.5	15.5 19.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to EQ	Waveform 2	3.5 2.5	7.0 4.5	10.5 8.0	3.5 2.5	11.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to GT	Waveform 2	6.5 3.5	9.0 5.0	16.0 8.0	6.5 3.0	17.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SE}$ to LT	Waveform 2	5.0 3.5	9.0 5.5	13.5 8.0	5.0 3.0	14.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay C/SI to C/SO	Waveform 2	4.0 4.0	7.0 7.0	11.0 11.0	4.0 4.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay M to GT	Waveform 2	8.0 6.0	13.0 10.0	19.5 15.5	8.0 6.0	20.5 16.5	ns
t_{PLH} t_{PHL}	Propagation delay M to LT	Waveform 2	8.0 4.5	15.0 8.0	22.0 12.0	8.0 4.0	23.0 13.0	ns
t_{PZH} t_{PZL}	Output Enable time S_n to I/O_n	Waveform 5 Waveform 6	4.5 5.5	7.0 9.0	13.0 15.0	4.5 5.5	14.0 16.0	ns
t_{PHZ} t_{PLZ}	Output Disable time S_n to I/O_n	Waveform 5 Waveform 6	3.0 4.5	5.0 8.0	12.0 12.5	2.0 4.5	13.0 13.5	ns

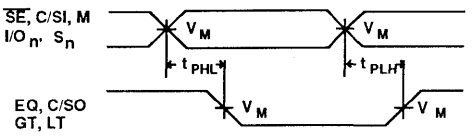
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 3	6.0 6.0			6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_0, S_1 to CP	Waveform 3	13.5 10.0			15.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_0, S_1 to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low C/SI to CP	Waveform 3	7.0 7.0			7.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low C/SI to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 4	5.0 10.0			5.0 10.0		ns

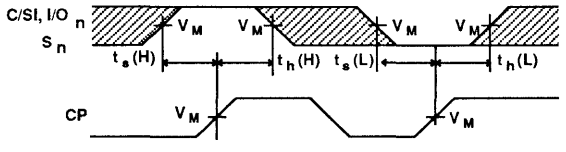
AC WAVEFORMS



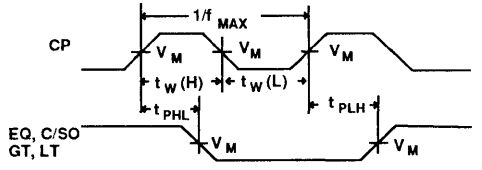
Waveform 1.
Propagation Delay for Inverting outputs



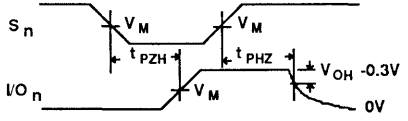
Waveform 2.
Propagation Delay for Non-Inverting outputs



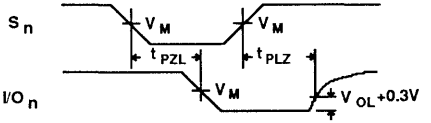
Waveform 3. Setup And Hold Times



Waveform 4. Propagation Delay, Clock To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level

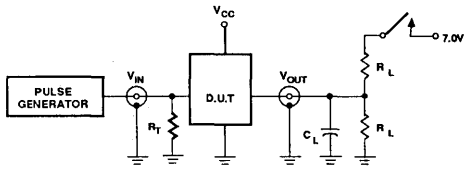


Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State and Open Collector Outputs

SWITCH POSITION

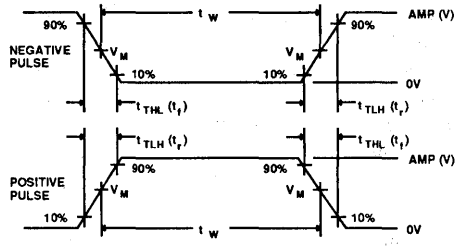
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
Open Collector	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F533, 74F534
Latch/Flip-Flop

FAST Products

74F533 Octal Transparent Latch, Inverting (3-State)
74F534 Octal D Flip-Flop, Inverting (3-State)

FEATURES

- **8-bit transparent latch-'F533**
- **8-bit positive edge triggered register-'F534**
- **3-State output buffers**
- **Common 3-state Output register**
- **Independent register and 3-state buffer operation**

DESCRIPTION

The 74F533 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the data that is present one set-up time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F533	5.5ns	41mA

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F534	165MHz	51mA

ORDERING INFORMATION

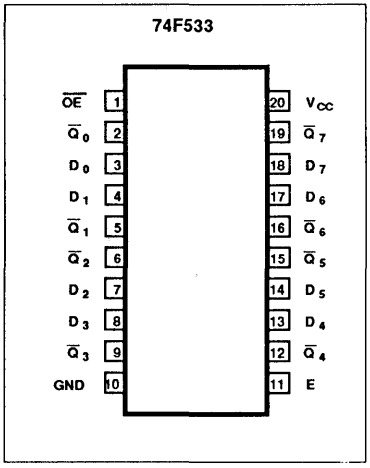
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F533N, N74F534N
20-Pin Plastic SOL	N74F533D, N74F534D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

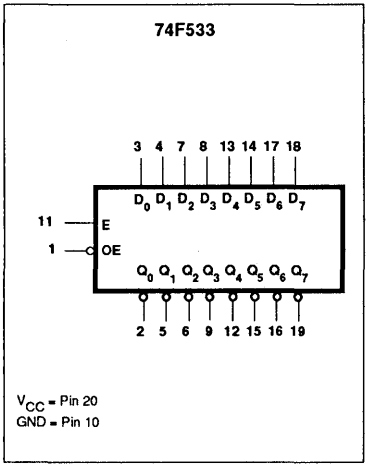
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20µA/0.6mA
E ('F533)	Enable input (active High)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
CP ('F534)	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{O}_0$ - $\overline{O}_7$	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

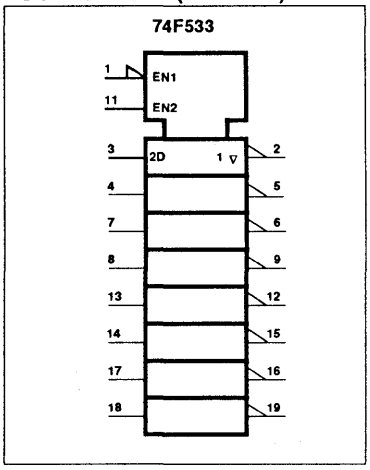
PIN CONFIGURATION



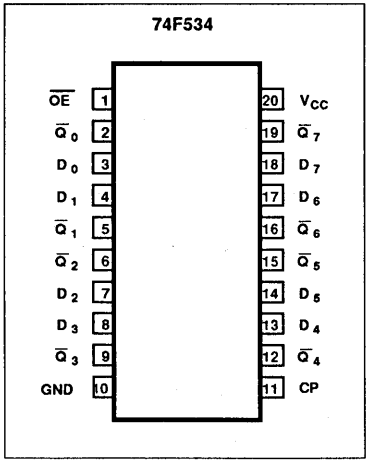
LOGIC SYMBOL



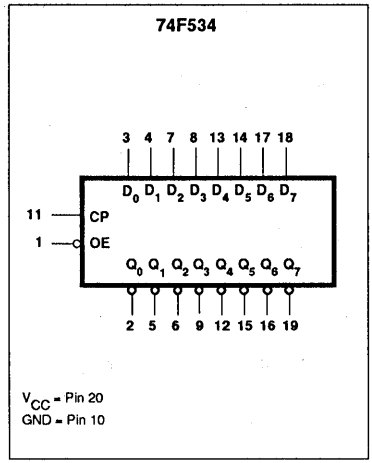
LOGIC SYMBOL(IEEE/IEC)



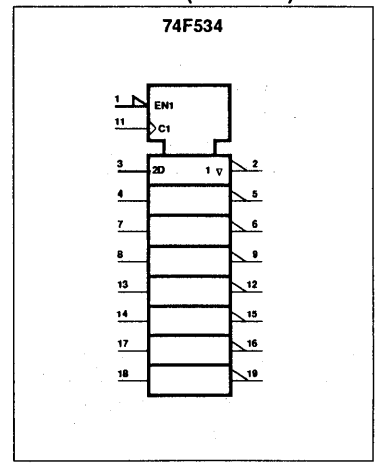
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



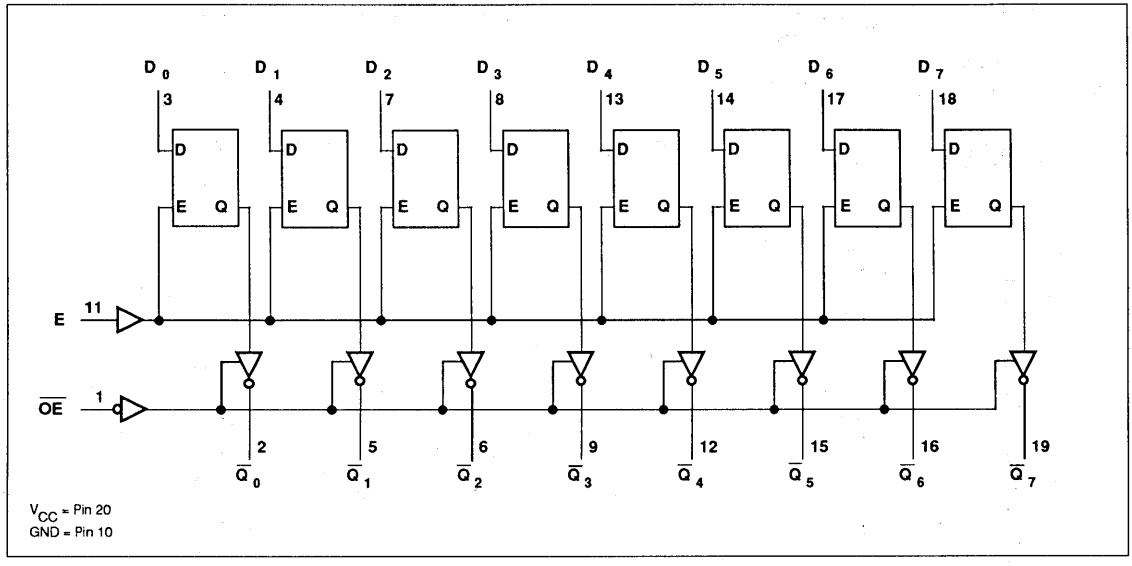
in high impedance "off" state, which means they will neither drive nor load the bus.

The 'F534 is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

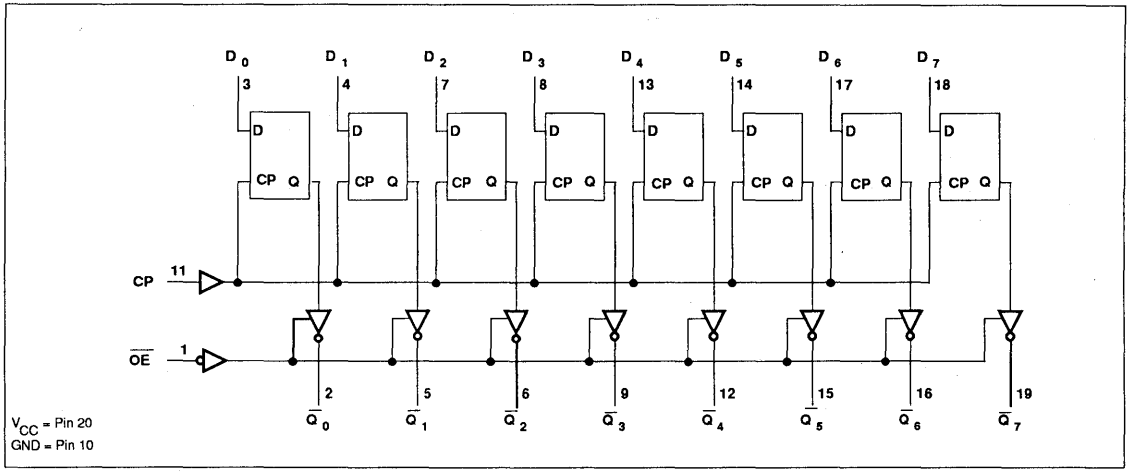
The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's $\overline{Q}$ output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 74F533



LOGIC DIAGRAM, 74F534



FUNCTION TABLE, 74F533

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	D_n	REGISTER	$\overline{Q}_0$ - $\overline{Q}_7$	
L L	H H	L H	L H	H L	Enable and read register
L L	↓ ↓	l h	L H	H L	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X D_n	NC D_n	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

FUNCTION TABLE, 74F534

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	D_n	REGISTER	$\overline{Q}_0$ - $\overline{Q}_7$	
L L	↑ ↑	l h	L H	H L	Load and read register
L	↟	X	NC	NC	Hold
H H	↡ ↑	X D_n	NC D_n	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↟ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	74F533	V_{CC} = MAX	$\overline{OE}$=4.5V, D_n=E=GND		41	61	mA
		74F534		$\overline{OE}$=4.5V, D_n=GND		51	86	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

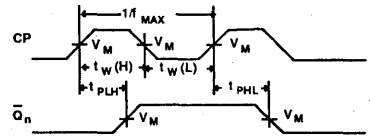
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	74F533	Waveform 2	4.0 3.0	6.0 4.5	8.5 7.0	4.0 3.0	9.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay E to $\overline{Q}_n$		Waveform 3	5.0 3.0	6.5 4.5	9.5 7.0	5.0 3.0	10.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	4.5 5.0	7.0 7.0	2.0 2.0	8.0 8.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	3.5 3.0	6.0 5.5	2.0 2.0	7.0 6.5	ns ns
f_{MAX}	Maximum Clock frequency	74F534	Waveform 1	150	165		135		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$		Waveform 1	3.0 3.0	4.5 4.5	7.0 7.0	2.5 2.5	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	4.5 5.0	7.5 7.5	2.0 2.0	8.5 8.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	3.5 3.5	6.5 5.5	2.0 2.0	7.5 6.5	ns ns

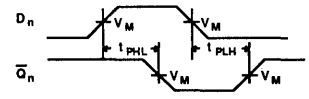
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time D_n to E	74F533	Waveform 4	1.5 0			1.5 0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to E		Waveform 4	2.5 2.5			2.5 2.5		ns
$t_w(H)$	E Pulse width, High		Waveform 3	3.0			3.0		ns
$t_s(H)$ $t_s(L)$	Set-up time D_n to CP	74F534	Waveform 5	2.0 2.0			2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP		Waveform 5	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1	3.0 3.5			3.5 4.0		ns

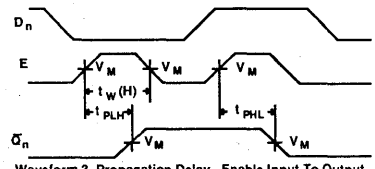
AC WAVEFORMS



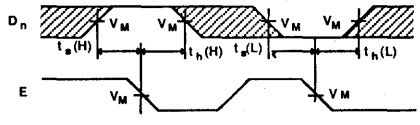
Waveform 1. Propagation Delay, Clock And Enable Inputs To Output, Enable, and Clock Pulse Widths, and Maximum Clock Frequency



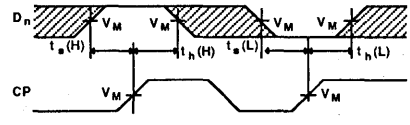
Waveform 2. Propagation Delay For Data To Output



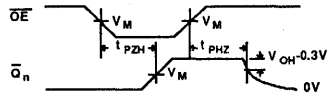
Waveform 3. Propagation Delay, Enable Input To Output, And Enable Pulse Width



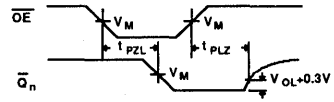
Waveform 4. Data Setup And Hold Times



Waveform 5. Data Setup And Hold Times



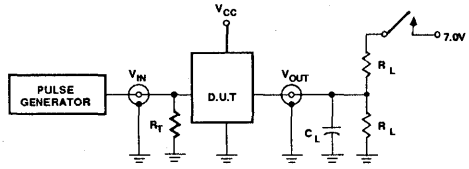
Waveform 6. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 7. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

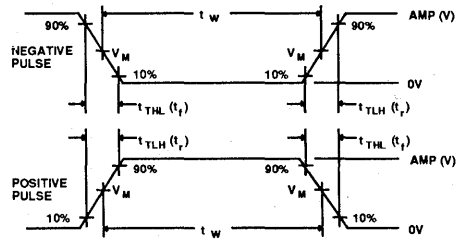
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F537
1-Of-10 Decoder (3-state)

Product Specification

FAST Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F537	9 ns	44mA

DESCRIPTION

The 74F537 is one of ten decoder/demultiplexer with four active High BCD inputs and ten mutually exclusive outputs. A Polarity control (P) input determines whether the outputs are active Low or active High. The 'F537 has 3-state outputs, and a High signal on the Output Enable ($\overline{OE}$) input forces all outputs to the high impedance state. Two input Enables, active High (E_1) and active Low ($\overline{E}_0$), are available for demultiplexing data to the selected output in either non-inverted or inverted form. Input codes greater than BCD nine causes all outputs to go to the inactive state (i.e., same polarity as the P input).

ORDERING INFORMATION

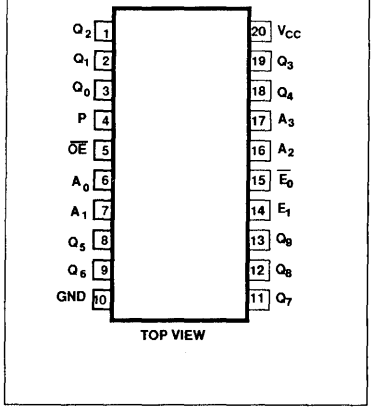
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F537N
20-Pin Plastic SOL	N74F537D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

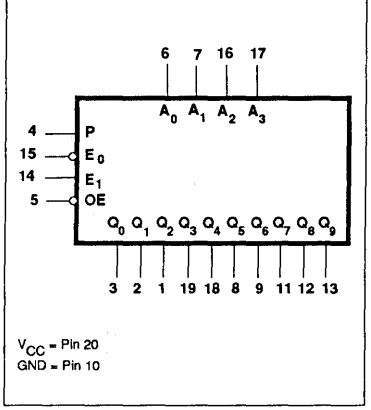
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_0$	Enable input (active Low)	1.0/1.0	20µA/0.6mA
E_1	Enable input (active High)	1.0/1.0	20µA/0.6mA
P	Polarity control input	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output enable input	1.0/1.0	20µA/0.6mA
Q_0 - Q_9	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

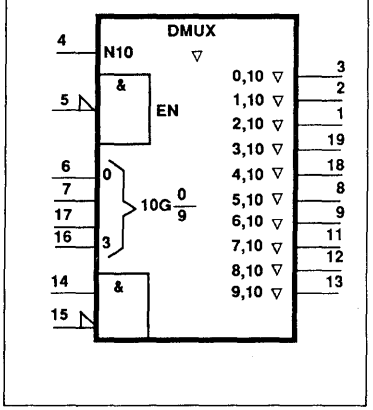
PIN CONFIGURATION



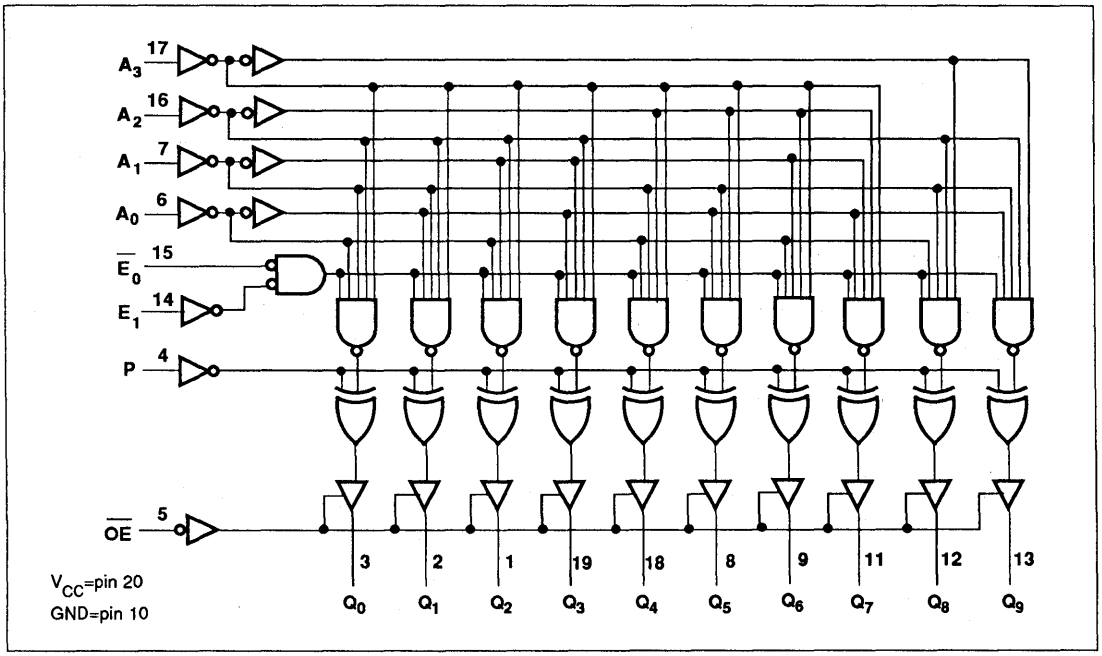
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS										OPERATING MODE
$\overline{OE}$	$\overline{E}_0$	E_1	A_3	A_2	A_1	A_0	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	
H	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	High impedance
L	H	X	X	X	X	X	Outputs equal P input										Disable
L	X	L	X	X	X	X											
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	Active High output (P=L)
L	L	H	L	L	L	H	L	H	L	L	L	L	L	L	L	L	
L	L	H	L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	H	L	L	H	H	L	L	L	H	L	L	L	L	L	L	
L	L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	
L	L	H	L	H	L	H	L	L	L	L	L	H	L	L	L	L	
L	L	H	L	H	H	L	L	L	L	L	L	L	H	L	L	L	
L	L	H	L	H	H	H	L	L	L	L	L	L	L	H	L	L	
L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L	
L	L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	
L	L	H	H	X	H	X	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	X	X	L	L	L	L	L	L	L	L	L	L	
L	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H	Active Low output (P=H)
L	L	H	L	L	L	H	H	L	H	H	H	H	H	H	H	H	
L	L	H	L	L	H	L	H	H	L	H	H	H	H	H	H	H	
L	L	H	L	L	H	H	H	H	H	L	H	H	H	H	H	H	
L	L	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H	
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	
L	L	H	L	H	H	L	H	H	H	H	H	H	L	H	H	H	
L	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	
L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	L	H	
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	L	
L	L	H	H	X	H	X	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	X	X	H	H	H	H	H	H	H	H	H	H	

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			44	66	mA

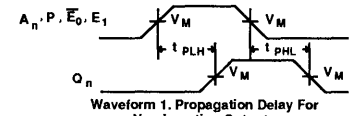
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

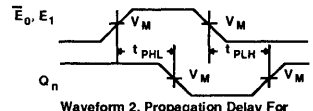
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 1	4.5 3.0	9.0 7.5	14.0 11.0	4.5 3.0	16.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$ to Q_n	Waveform 2	4.0 3.0	8.0 8.0	11.0 11.0	4.0 3.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay E_1 to Q_n	Waveform 2	6.0 4.0	8.5 8.5	11.5 11.5	6.0 4.0	13.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay P to Q_n	Waveform 1	5.0 3.5	12.5 6.5	16.0 10.0	5.0 3.5	17.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_n	Waveform 3 Waveform 4	2.5 4.0	4.5 5.5	7.0 8.0	2.5 4.0	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q_n	Waveform 3 Waveform 4	1.5 2.0	3.0 4.0	6.0 6.5	1.0 2.0	7.0 7.0	ns

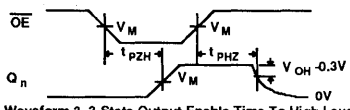
AC WAVEFORMS



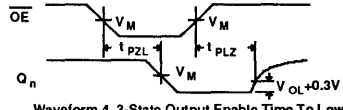
Waveform 1. Propagation Delay For Non-Inverting Outputs



Waveform 2. Propagation Delay For Inverting Outputs



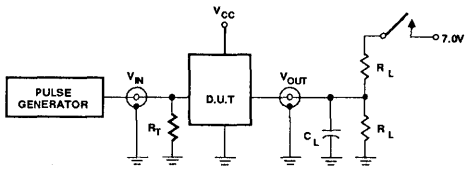
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



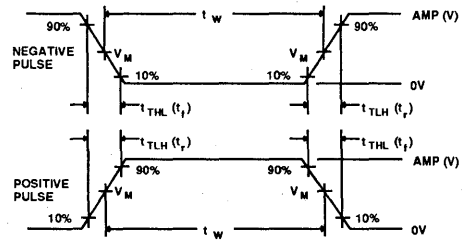
Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F538
1-Of-8 Decoder (3-state)

Product Specification

FAST Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F538	8.5 ns	35mA

DESCRIPTION

The 74F538 decoder/demultiplexer accepts three address (A_0 - A_2) input signals and decodes them to select one of eight mutually exclusive outputs. A Polarity control (P) input determines whether the outputs are active Low or active High. The 'F538 has 3-state outputs, and a High signal on the Output Enables ($\overline{OE}_n$) inputs will force all outputs to the high impedance state. Two active High (E_2, E_3) and active Low ($\overline{E}_0$, $\overline{E}_1$) inputs are available for easy expansion to 1-of-32 decoding with four packages, or for data demultiplexing to 1-of-8 or 1-of-16 destinations.

ORDERING INFORMATION

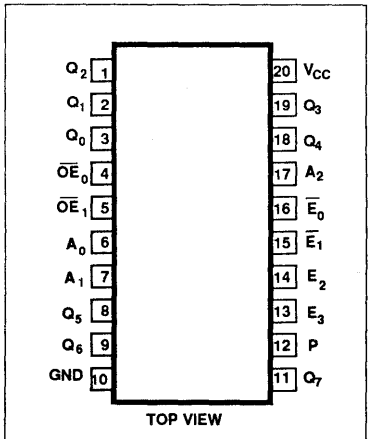
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F538N
20-Pin Plastic SOL	N74F538D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

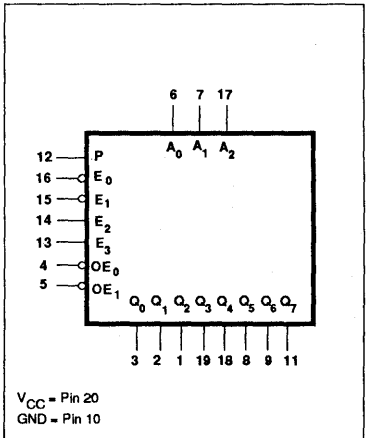
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_2	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_0$, $\overline{E}_1$	Enable inputs (active Low)	1.0/1.0	20µA/0.6mA
E_2, E_3	Enable inputs (active High)	1.0/1.0	20µA/0.6mA
P	Polarity control input	1.0/1.0	20µA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable inputs	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

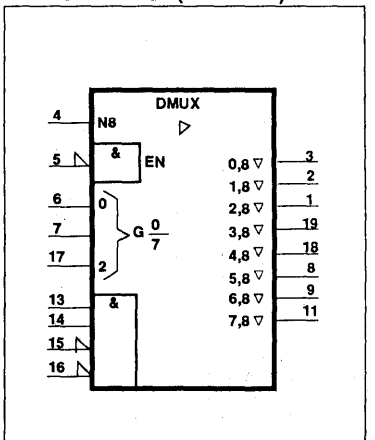
PIN CONFIGURATION



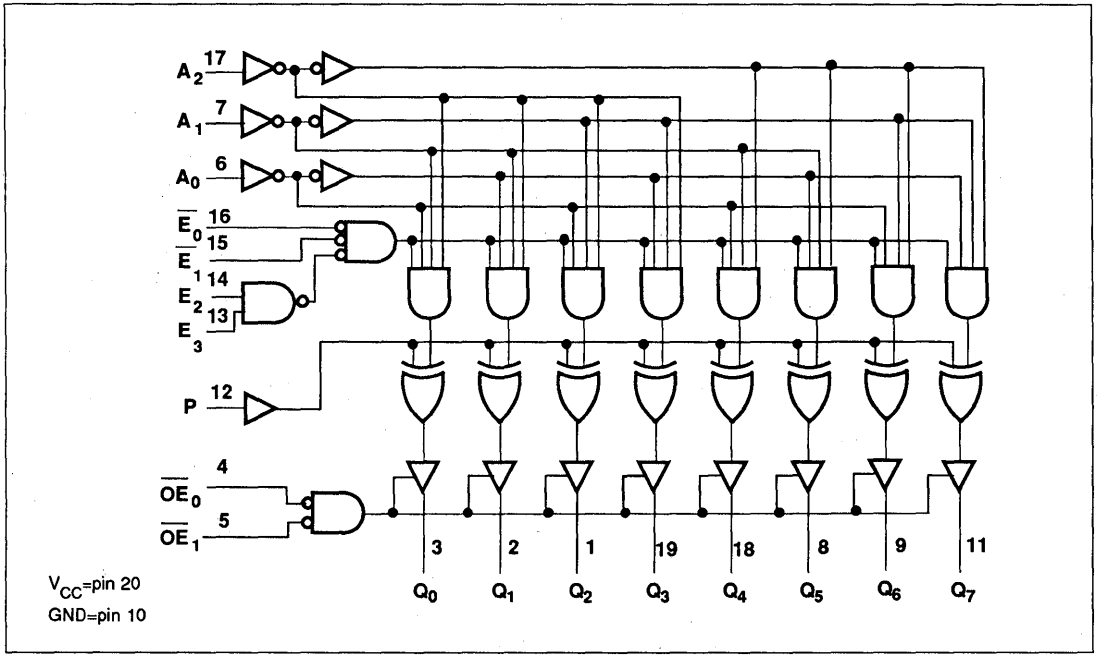
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS									OUTPUTS								OPERATING MODE
$\overline{OE}_0$	$\overline{OE}_1$	$\overline{E}_0$	$\overline{E}_1$	E_2	E_3	A_2	A_1	A_0	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	High impedance
X	H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	
L	L	H	X	X	X	X	X	X	Outputs equal P input								Disable
L	L	X	H	X	X	X	X	X									
L	L	X	X	L	X	X	X	X									
L	L	X	X	X	L	X	X	X									
L	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L	L	Active High output (P=L)
L	L	L	L	H	H	L	L	H	L	H	L	L	L	L	L	L	
L	L	L	L	H	H	L	H	L	L	L	H	L	L	L	L	L	
L	L	L	L	H	H	L	H	H	L	L	L	H	L	L	L	L	
L	L	L	L	H	H	H	L	L	L	L	L	L	H	L	L	L	
L	L	L	L	H	H	H	L	H	L	L	L	L	L	H	L	L	
L	L	L	L	H	H	H	H	L	L	L	L	L	L	L	H	L	
L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	H	
L	L	L	L	H	H	L	L	L	L	H	H	H	H	H	H	H	Active Low output (P=H)
L	L	L	L	H	H	L	L	H	H	L	H	H	H	H	H	H	
L	L	L	L	H	H	L	H	L	H	H	L	H	H	H	H	H	
L	L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H	
L	L	L	L	H	H	H	L	L	H	H	H	H	L	H	H	H	
L	L	L	L	H	H	H	L	H	H	H	H	H	L	H	H	H	
L	L	L	L	H	H	H	H	L	H	H	H	H	H	L	H	H	
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			30	40	mA
		I_{CCL}				35	50	mA
		I_{CCZ}				35	50	mA

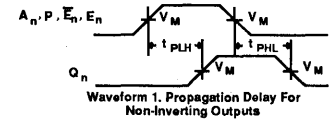
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

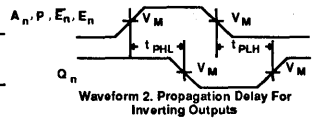
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 1, 2	5.5 3.0	8.5 7.5	13.0 12.5	5.0 3.0	14.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$ or $\overline{E}_1$ to Q_n	Waveform 1, 2	5.5 3.0	8.5 7.5	12.0 12.0	5.0 3.0	13.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay E_2 or E_3 to Q_n	Waveform 1, 2	6.5 4.0	9.0 7.0	12.5 12.5	5.5 3.5	13.5 13.0	ns
t_{PLH} t_{PHL}	Propagation delay P to Q_n	Waveform 1, 2	4.5 3.5	9.5 6.5	15.0 10.0	4.0 3.5	16.5 10.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_0$ or $\overline{OE}_1$ to Q_n	Waveform 3 Waveform 4	2.5 6.5	5.5 9.5	9.5 13.5	2.0 6.0	11.0 15.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_0$ or $\overline{OE}_1$ to Q_n	Waveform 3 Waveform 4	1.0 1.0	3.0 3.5	6.0 8.5	1.0 1.0	7.0 9.5	ns

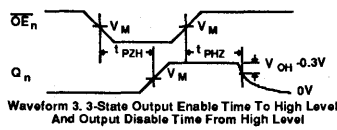
AC WAVEFORMS



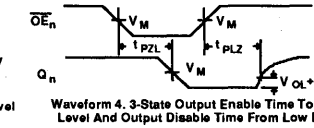
Waveform 1. Propagation Delay For Non-Inverting Outputs



Waveform 2. Propagation Delay For Inverting Outputs



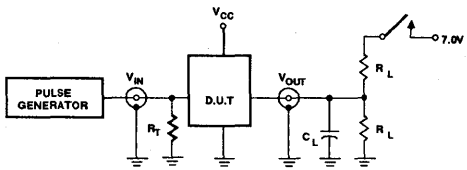
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

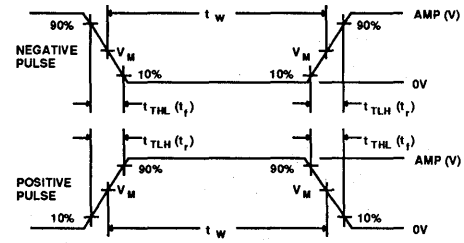
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F539
Dual 1-Of-4 Decoder (3-state)

Product Specification

FAST Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F539	7.5 ns	40mA

DESCRIPTION

The 74F539 contains two independent decoders. Each accepts two address (A_0 - A_1) input signals and decodes them to select one of four mutually exclusive outputs. A Polarity control (P) input determines whether the outputs are active Low (P=H) or active High (P=L). An active-Low Enable ($\overline{E}$) is available for data demultiplexing. Data is routed to the selected output in non-inverted or inverted form in the active-Low mode or inverted form in the active-High mode. A High signal on the Output Enable ($\overline{OE}_n$) input forces the 3-state outputs to the high impedance state.

ORDERING INFORMATION

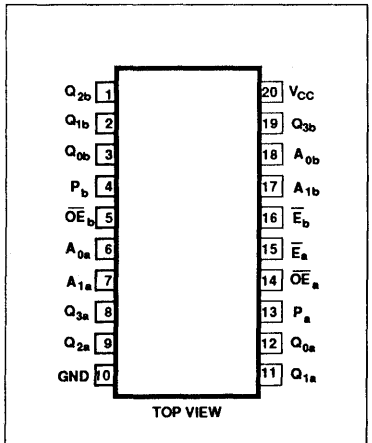
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F539N
20-Pin Plastic SOL	N74F539D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

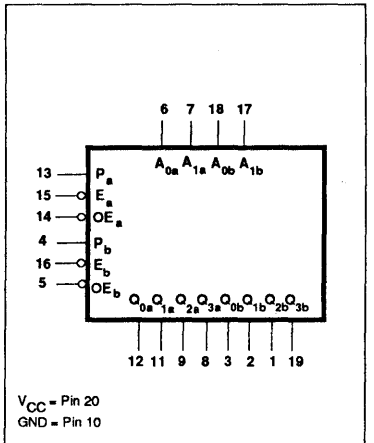
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_{0a}, A_{1a}	Decoder A Address inputs	1.0/1.0	20µA/0.6mA
A_{0b}, A_{1b}	Decoder B Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_a$, $\overline{E}_b$	Enable inputs (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}_a$, $\overline{OE}_b$	Output enable inputs (active Low)	1.0/1.0	20µA/0.6mA
P_a, P_b	Polarity control inputs	1.0/1.0	20µA/0.6mA
Q_{0a} - Q_{3a}	Decoder A Data outputs	150/40	3.0mA/24mA
Q_{0b} - Q_{3b}	Decoder B Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

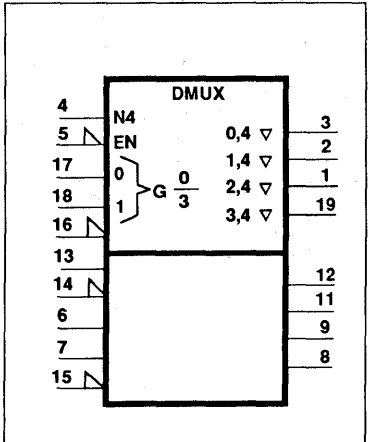
PIN CONFIGURATION



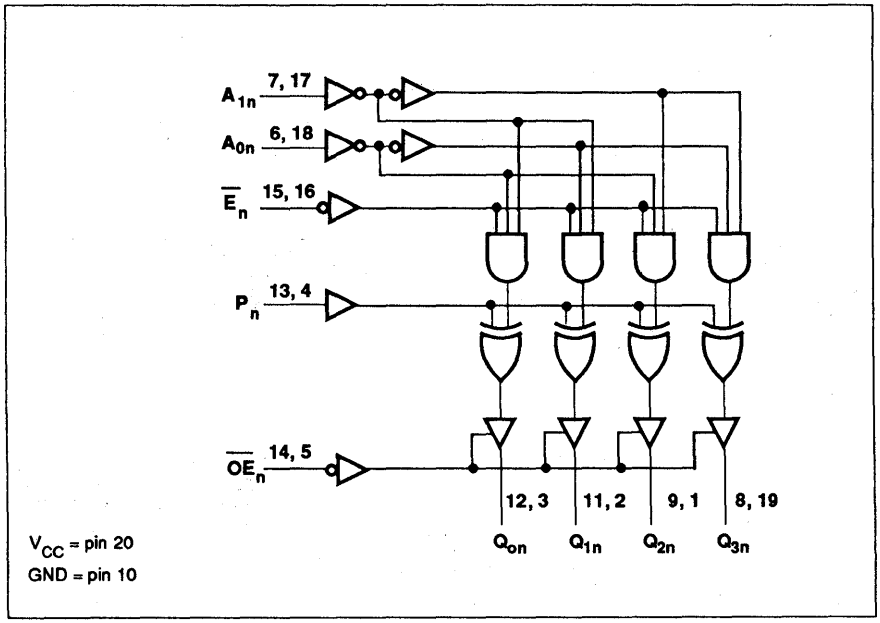
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS				OPERATING MODE
$\overline{OE}_n$	$\overline{E}_n$	A_{1n}	A_{0n}	Q_{0n}	Q_{1n}	Q_{2n}	Q_{3n}	
H	X	X	X	Z	Z	Z	Z	High impedance
L	H	X	X	$Q_n = P$				Disable
L	L	L	L	H	L	L	L	Active High output (P=L)
L	L	L	H	L	H	L	L	
L	L	H	L	L	L	H	L	
L	L	H	H	L	L	L	H	
L	L	L	L	L	H	H	H	Active Low output (P=H)
L	L	L	H	H	L	H	H	
L	L	H	L	H	H	L	H	
L	L	H	H	H	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off "state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			35	50	mA
		I_{CCL}				40	55	mA
		I_{CCZ}				40	60	mA

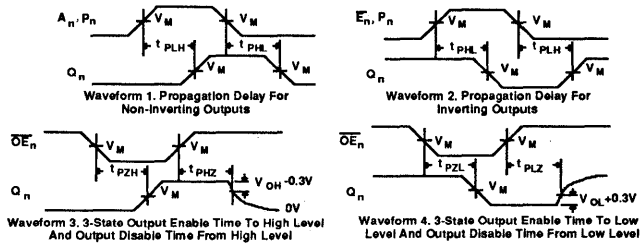
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

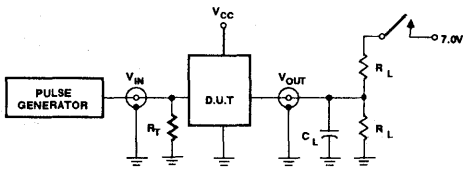
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 1	4.5 3.0	8.5 8.0	12.5 12.5	4.0 3.0	13.5 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to Q_n	Waveform 2	5.0 3.0	7.5 7.0	11.0 11.0	4.5 3.0	12.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay P_n to Q_n	Waveform 1	4.0 3.5	6.5 5.5	9.5 9.0	3.5 3.0	10.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay P_n to Q_n (INV)	Waveform 2	6.0 4.0	11.5 6.0	14.5 9.0	5.0 4.0	15.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_n$ to Q_n	Waveform 3 Waveform 4	2.5 5.5	4.0 7.0	7.5 10.5	2.0 5.0	8.5 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_n$ to Q_n	Waveform 3 Waveform 4	1.5 2.0	3.0 4.0	6.0 8.0	1.0 1.5	6.5 8.5	ns

AC WAVEFORMS



NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

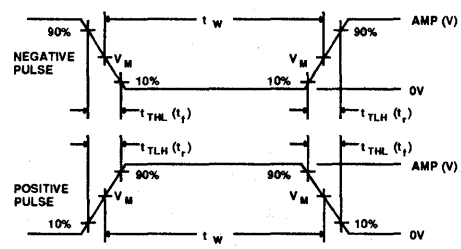
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F540, 74F541
Buffers

FAST Products

74F540 Octal Inverter Buffer (3-State)
74F541 Octal Buffer (3-State)
Product Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Low power, light bus loading**
- **Functional similar to the 'F240 and 'F241**
- **Provides ideal interface and increases fan-out of MOS Microprocessors**
- **Efficient pinout to facilitate PC board layout**
- **Octal bus interface**
- **3-State buffer outputs sink 64mA**
- **15mA source current**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F540	3.5ns	58mA
74F541	5.5ns	55mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F540N, N74F541N
20-Pin Plastic SOL	N74F540D, N74F541D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

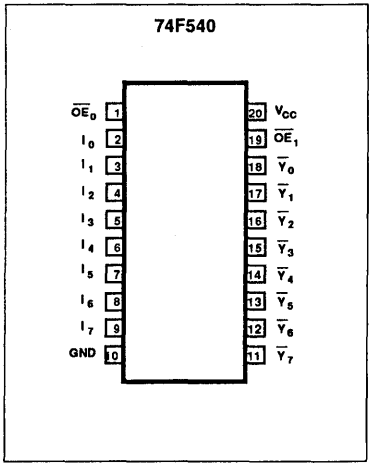
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0-I_7	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_0$, $\overline{OE}_1$	3-state output enable inputs (active Low)	1.0/0.033	20μA/20μA
Y_0-Y_7	Data outputs ('F541)	750/106.7	15mA/64mA
$\overline{Y}_0$-$\overline{Y}_7$	Data outputs ('F540)	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

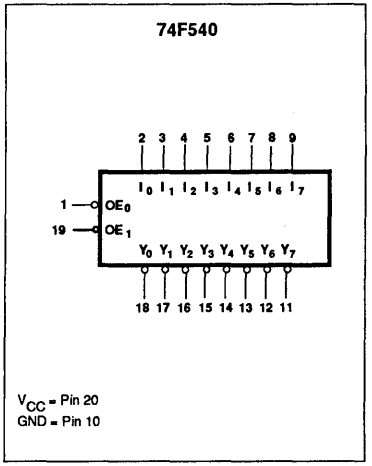
DESCRIPTION

The 74F540 and 74F541 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The devices feature input and outputs on opposite sides of the package to facilitate printed circuit board layout.

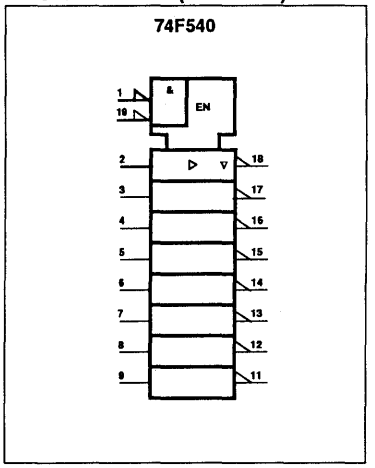
PIN CONFIGURATION



LOGIC SYMBOL

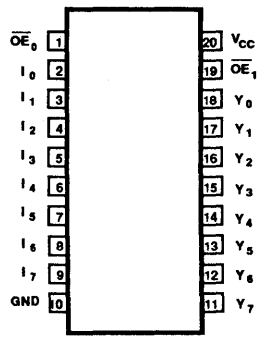


LOGIC SYMBOL(IEEE/IEC)



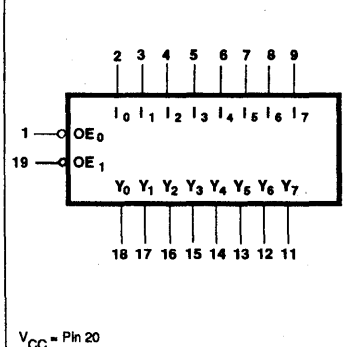
PIN CONFIGURATION

74F541



LOGIC SYMBOL

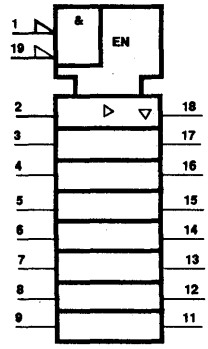
74F541



V_{CC} = Pin 20
GND = Pin 10

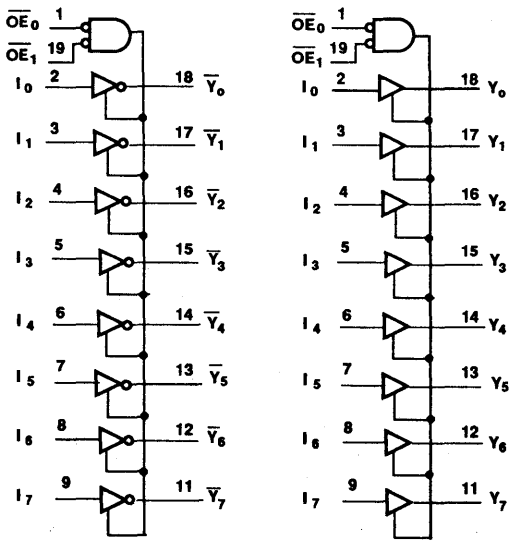
LOGIC SYMBOL(IEEE/IEC)

74F541



LOGIC DIAGRAM

74F540 74F541



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE

INPUTS			OUTPUTS	
			'F541	'F540
$\overline{OE}_0$	$\overline{OE}_1$	I_n	Y_n	$\overline{Y}_n$
L	L	L	L	H
L	L	H	H	L
X	H	X	Z	Z
H	X	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH}=-15mA	±10%V_{CC}	2.0			V
				±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}			0.55	V
				±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} =0.0V, V_i = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total) 'F540	V_{CC} = MAX	I_{CCH}	I_n=$\overline{OE}_n$=GND		22	30	mA
			I_{CCL}	I_n=4.5V, $\overline{OE}_n$=GND		58	75	mA
			I_{CCZ}	I_n=GND, $\overline{OE}_n$=4.5V		40	55	mA
	'F541		I_{CCH}	I_n=4.5V, $\overline{OE}_n$=GND		30	40	mA
			I_{CCL}	I_n=$\overline{OE}_n$=GND		55	72	mA
			I_{CCZ}	I_n=GND, $\overline{OE}_n$=4.5V		45	58	mA

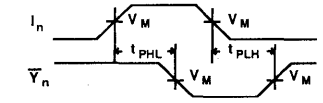
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

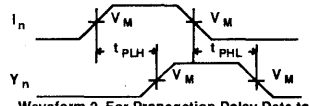
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	74F540	Waveform 1	3.0 1.5	4.5 2.5	6.5 4.5	2.5 1.5	7.5 5.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	74F540	Waveform 3 Waveform 4	3.0 4.0	5.5 7.5	7.5 9.5	3.0 4.0	8.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	74F540	Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 5.5	2.0 2.0	6.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	74F541	Waveform 2	2.5 3.5	5.0 6.0	6.5 7.0	2.5 3.0	7.0 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	74F541	Waveform 6 Waveform 7	3.0 3.0	5.5 6.5	7.0 8.5	3.0 3.0	7.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	74F541	Waveform 6 Waveform 7	2.0 2.0	4.0 4.0	7.0 7.0	2.0 2.0	7.5 7.5	ns

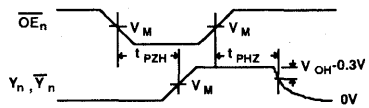
AC WAVEFORMS



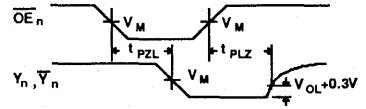
Waveform 1. For Propagation Delay Data to Output for 'F540



Waveform 2. For Propagation Delay Data to Output for 'F541



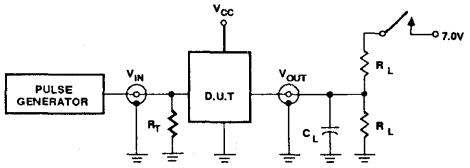
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

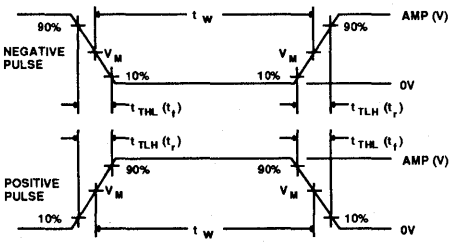
TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST Products

FAST 74F543, 74F544 Transceivers

'F543 Octal Registered Transceiver, Non-Inverting (3-State)
'F544 Octal Registered Transceiver, Inverting (3-State)
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F543	6.0ns	80mA
74F544	6.5ns	95mA

FEATURES

- **Combines 74F245 and 74F373 type functions in one chip**
- **8-bit octal transceiver with D-type latch**
- **'F543 Non-inverting**
  'F544 Inverting
- **Back-to-back registers for storage**
- **Separate controls for data flow in each direction**
- **A outputs sink 24mA and source 3mA**
- **B outputs sink 64mA and source 15mA**
- **300 mil wide 24-pin Slim DIP package**
- **3-state outputs for bus-orientated applications**

DESCRIPTION

The 74F543 and 74F544 Octal Registered Transceivers contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. While the 'F543 has non-inverting data path, the 'F544 inverts data in both directions. The A outputs are guaranteed to sink 24mA while the B outputs are rated for 64mA.

ORDERING INFORMATION

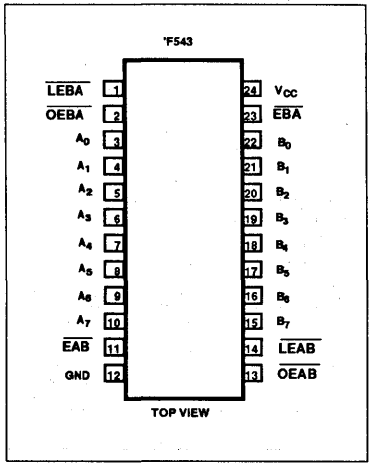
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F543N, N74F544N
24-Pin Plastic SOL	N74F543D, N74F544D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

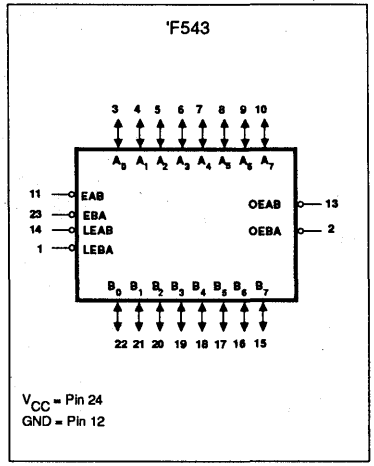
PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F543 'F54	A_0 - A_7	Port A, 3-state inputs	3.5/1.0	70µA/0.6mA
	B_0 - B_7	Port B, 3-state inputs	3.5/1.0	70µA/0.6mA
	$\overline{OEAB}$	A-to-B Output Enable input (Active Low)	1.0/1.0	20µA/0.6mA
	$\overline{OEBA}$	B-to-A Output Enable input (Active Low)	1.0/1.0	20µA/0.6mA
	$\overline{EAB}$	A-to-B Enable input (Active Low)	1.0/2.0	20µA/1.2mA
	$\overline{EBA}$	B-to-A Enable input (Active Low)	1.0/2.0	20µA/1.2mA
	$\overline{LEAB}$	A-to-B Latch Enable input (Active Low)	1.0/1.0	20µA/0.6mA
	$\overline{LEBA}$	B-to-A Latch Enable input (Active Low)	1.0/1.0	20µA/0.6mA
'F543	A_0 - A_7	Port A, 3-state outputs	150/40	3.0mA/24mA
	B_0 - B_7	Port B, 3-state outputs	750/106.7	15mA/64mA
'F544	$\overline{A}_0$ - $\overline{A}_7$	Port $\overline{A}$, 3-state outputs	150/40	3.0mA/24mA
	$\overline{B}_0$ - $\overline{B}_7$	Port $\overline{B}$, 3-state outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

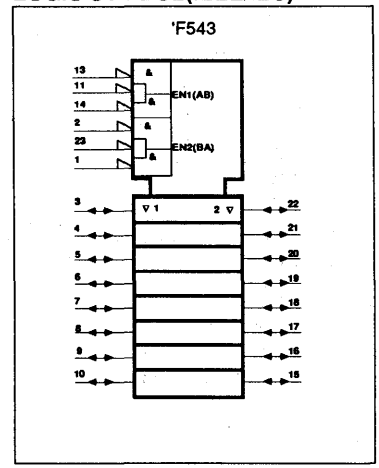
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

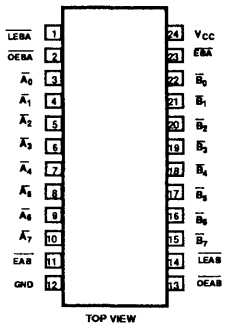


Bus Transceivers

FAST 74F543, 74F544

PIN CONFIGURATION

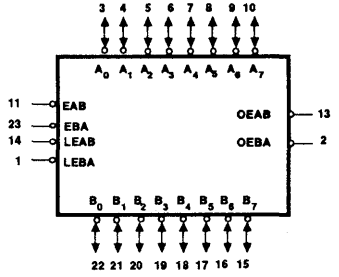
'F544



TOP VIEW

LOGIC SYMBOL

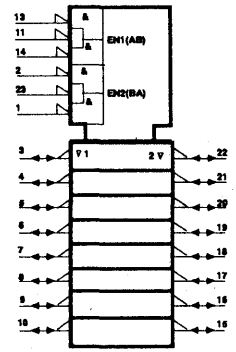
'F544



V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

'F544



FUNCTIONAL DESCRIPTION

The 'F543 and 'F544 contain two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{EAB}$) input must be Low in order to enter data from A_0-A_7 or take data from B_0-B_7, as indicated in the Function Table. With $\overline{EAB}$ Low, a Low signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent Low-to High transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both Low, the 3-state B output buffers are active and display the data present at the outputs of the A latches.

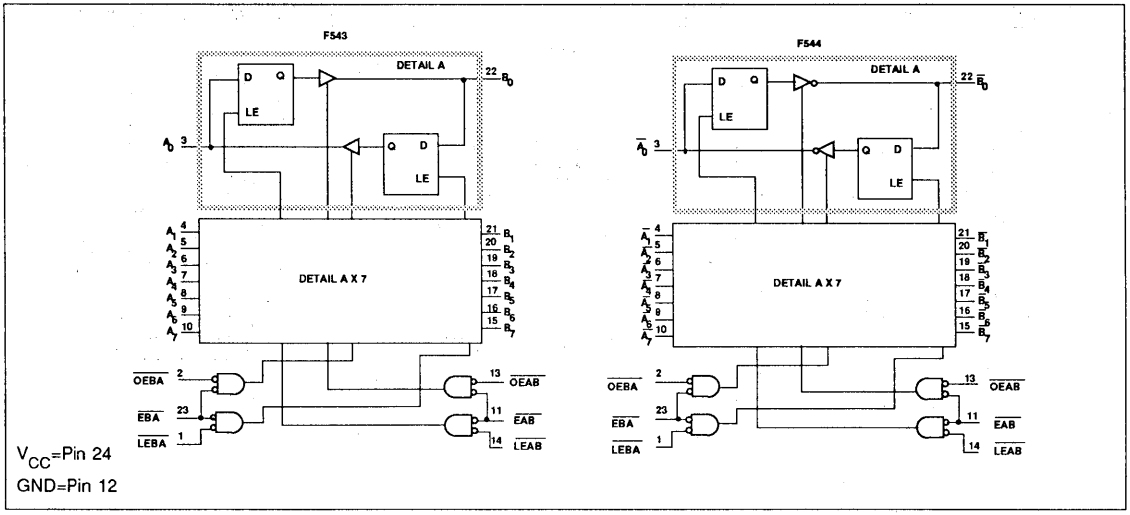
Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

FUNCTION TABLE for 'F543 and 'F544

INPUTS				OUTPUTS		STATUS
$\overline{OEXX}$	$\overline{EXX}$	$\overline{LEXX}$	DATA	'F543	'F544	
H	X	X	X	Z	Z	Disabled
X	H	X	X	Z	Z	Disabled
L	↑	L	h	Z	Z	Disabled + Latch
L	↑	L	l	Z	Z	
L	L	↑	h	H	L	Latch + Display
L	L	↑	l	L	H	
L	L	L	H	H	L	Transparent
L	L	L	L	L	H	
L	L	H	X	NC	NC	Hold

H= High voltage level
L= Low voltage level
h= High state must be present one setup time before the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
l = Low state must be present one setup time before the Low-to -High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
↑ =Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
X=Don't care
NC=No change
Z =High impedance "off" state

LOGIC DIAGRAM



V_{CC}=Pin 24
GND=Pin 12

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7, $\overline{A}_0$-$\overline{A}_7$	48	mA
		B_0-B_7, $\overline{B}_0$-$\overline{B}_7$	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7, $\overline{A}_0$-$\overline{A}_7$			-3	mA
		B_0-B_7, $\overline{B}_0$-$\overline{B}_7$			-15	mA
I_{OL}	Low-level output current	A_0-A_7, $\overline{A}_0$-$\overline{A}_7$			24	mA
		B_0-B_7, $\overline{B}_0$-$\overline{B}_7$			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$\overline{A_0}$-$\overline{A_7}$, A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		B_0-B_7, $\overline{B_0}$-$\overline{B_7}$		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	$\overline{A_0}$-$\overline{A_7}$, A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7, $\overline{B_0}$-$\overline{B_7}$		I_{OL}=64mA	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEAB}$, $\overline{OEBA}$, $\overline{EAB}$, $\overline{EBA}$, $\overline{LEAB}$, $\overline{LEBA}$	V_{CC} =MAX, V_I =7.0V					100	µA
		Others	V_{CC} =5.5, V_I =5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		$\overline{EAB}$, $\overline{EBA}$						-1.2	mA
I_{OZH} + I_{IH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZH} + I_{IL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-600	µA
I_{OS}	Short-circuit output current[3]	A_0-A_7, $\overline{A_0}$-$\overline{A_7}$	V_{CC} = MAX			-60		-150	mA
		B_0-B_7, $\overline{B_0}$-$\overline{B_7}$				-100		-225	mA
I_{CC}	Supply current (total)	'F543	I_{CCH}	V_{CC} = MAX			70	105	mA
			I_{CCL}				95	135	mA
			I_{CCZ}				95	135	mA
		'F544	I_{CCH}	V_{CC} = MAX			80	110	mA
			I_{CCL}				105	140	mA
			I_{CCZ}				100	135	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 74F543

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	3.5 3.0	5.5 5.0	8.5 8.0	3.0 2.5	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	2.5 2.5	4.0 4.5	7.0 7.5	2.5 2.5	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to A_n	Waveform 1, 2	5.0 4.0	7.0 6.0	10.0 9.0	4.5 4.0	11.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEAB}$ to B_n	Waveform 1, 2	6.0 4.5	8.5 6.5	11.5 9.5	5.5 4.0	12.5 10.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ to A_n or $\overline{OEAB}$ to B_n	Waveform 4 Waveform 5	2.0 3.5	4.0 5.0	7.5 8.5	1.5 3.0	8.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ to A_n or $\overline{OEAB}$ to B_n	Waveform 4 Waveform 5	1.0 1.5	3.0 4.0	6.5 7.5	1.0 1.0	7.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{EBA}$ to A_n or $\overline{EAB}$ to B_n	Waveform 4 Waveform 5	4.5 5.0	7.0 7.0	10.5 10.5	4.0 4.5	11.5 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{EBA}$ to A_n or $\overline{EAB}$ to B_n	Waveform 4 Waveform 5	2.5 4.5	5.0 7.0	8.5 10.5	2.0 3.0	9.5 12.0	ns

AC SETUP REQUIREMENTS for 74F543

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n to $\overline{LEAB}$ or B_n to $\overline{LEBA}$	Waveform 3	0.0 2.5			0.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n to $\overline{LEAB}$ or B_n to $\overline{LEBA}$	Waveform 3	0.0 1.5			0.0 2.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n to $\overline{EAB}$ or B_n to $\overline{EBA}$	Waveform 3	1.0 2.5			1.5 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n to $\overline{EAB}$ or B_n to $\overline{EBA}$	Waveform 3	0.0 1.5			0.0 2.0		ns
$t_w(L)$	Latch enable Pulse width, Low	Waveform 3	4.0			4.5		ns

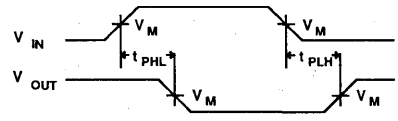
AC ELECTRICAL CHARACTERISTICS for 74F544

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{B}_n$ or B_n to $\overline{A}_n$	Waveform 1	3.0 3.0	6.5 5.0	9.5 8.0	3.0 3.0	10.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to $\overline{A}_n$	Waveform 1, 2	4.0 4.0	7.0 7.0	9.5 9.5	4.0 4.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEAB}$ to $\overline{B}_n$	Waveform 1, 2	5.0 4.0	8.0 7.5	11.5 9.5	4.0 4.0	12.5 10.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ to $\overline{A}_n$ or $\overline{OEAB}$ to $\overline{B}_n$	Waveform 4 Waveform 5	2.0 3.5	4.0 5.5	7.0 8.5	1.5 3.0	7.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ to $\overline{A}_n$ or $\overline{OEAB}$ to $\overline{B}_n$	Waveform 4 Waveform 5	1.0 1.5	4.0 4.0	6.5 6.5	1.0 1.5	7.0 7.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{EBA}$ to $\overline{A}_n$ or $\overline{EAB}$ to $\overline{B}_n$	Waveform 4 Waveform 5	4.0 4.5	7.0 8.0	9.5 11.0	3.5 4.5	10.0 12.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{EBA}$ to $\overline{A}_n$ or $\overline{EAB}$ to $\overline{B}_n$	Waveform 4 Waveform 5	2.5 4.5	5.0 8.5	8.0 11.5	2.5 4.0	9.0 11.5	ns

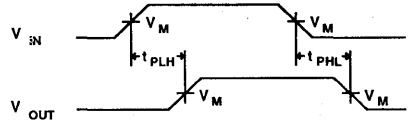
AC SETUP REQUIREMENTS for 74F544

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n to $\overline{LEAB}$ or B_n to $\overline{LEBA}$	Waveform 3	1.5 1.5			2.0 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n to $\overline{LEAB}$ or B_n to $\overline{LEBA}$	Waveform 3	1.5 2.0			2.5 2.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n to $\overline{EAB}$ or B_n to $\overline{EBA}$	Waveform 3	1.5 1.5			2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n to $\overline{EAB}$ or B_n to $\overline{EBA}$	Waveform 3	1.5 2.0			2.0 2.0		ns
$t_w(L)$	Latch enable Pulse width, Low	Waveform 3	4.0			4.5		ns

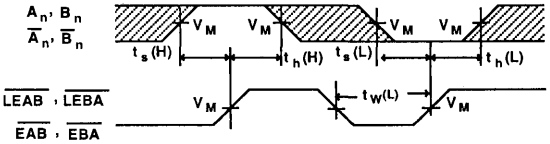
AC WAVEFORMS



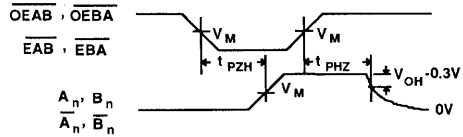
Waveform 1. Propagation Delay For Inverting Output



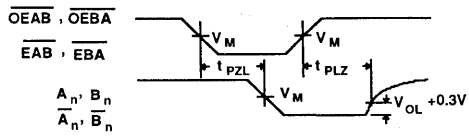
Waveform 2. Propagation Delay For Non-Inverting Output



Waveform 3. Data Setup And Hold Times And Latch Enable pulse width



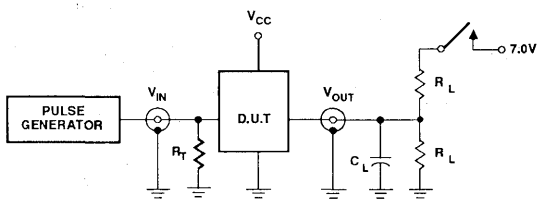
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



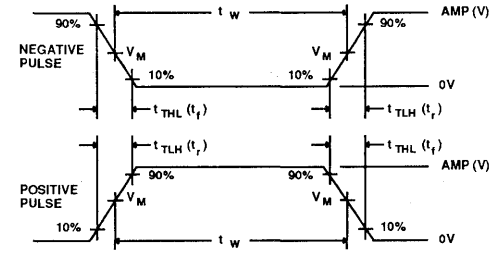
Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded area indicate when the input is permitted to change for predictable output

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F545
Transceiver

FAST Products

Octal Bidirectional Transceiver (With 3-State Inputs/Outputs)
Product Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (70μA in High and Low states) output**
- **Higher drive than 8304**
- **8-bit bidirectional data flow reduces system package count**
- **3-state inputs/outputs for interfacing with bus orientated systems**
- **24 mA and 64mA bus drive capability on A and B ports, respectively**
- **Transmit/Receive and Output Enable simplify control logic**
- **Pin for pin replacement for Intel 8286**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F545	4.0ns	87mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F545N
20-Pin Plastic SOL	N74F545D

DESCRIPTION

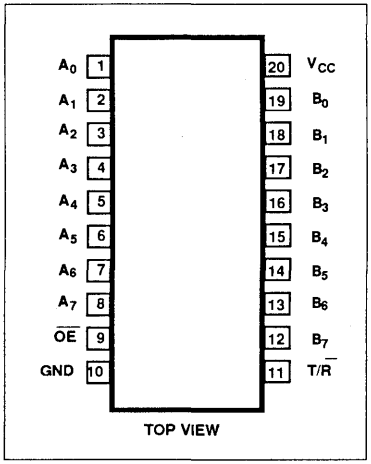
The 74F545 is an 8-bit, 3-state, high speed transceiver. It provides bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA bus drive capability on the A ports and 64mA bus drive capbility on the B ports. One input, Transmit/Receive ($T/\overline{R}$) determines the direction of logic signals through the bidirectional transceiver. Transmit enables data from A ports to B ports; Receive enables data from B ports to A ports. The Output Enable input disables both A and B ports by placing them in a 3-state condition. The 74F545 performs the same function as the 74F245, the only difference being package pin assignment.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

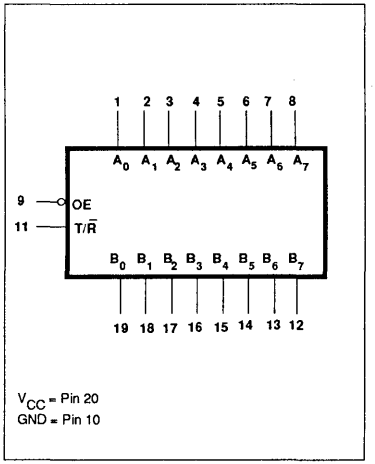
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7, B_0- B_7	Data inputs	3.5/0.117	70μA/70μA
$\overline{OE}$	Output Enable input (active Low)	2.0/0.067	40μA/40μA
$T/\overline{R}$	Transmit/Receive input	2.0/0.067	40μA/40μA
A_0- A_7	Port A 3-state outputs	150/40	3.0mA/24mA
B_0- B_7	Port B 3-state outputs	750/107	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

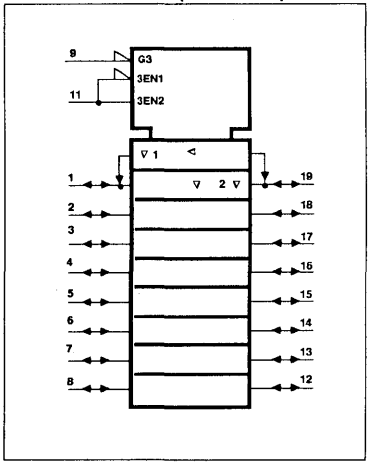
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

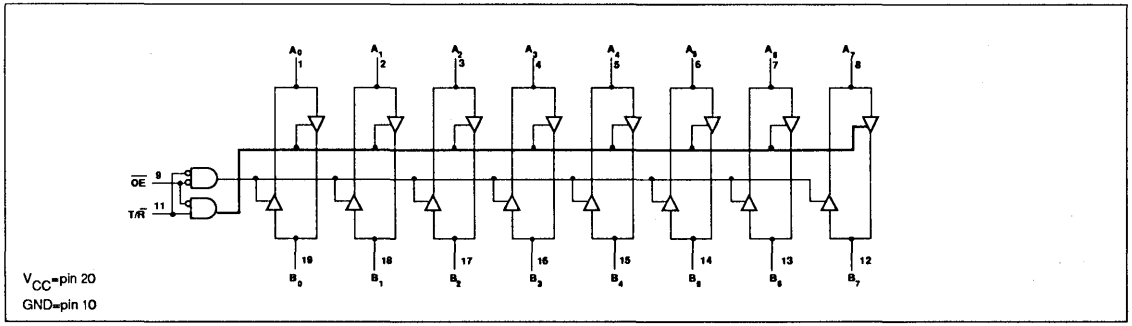


FUNCTION TABLE

INTPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B data to Bus A
L	H	Bus A data to Bus B
H	X	Z

H=High voltage level
L=Low voltage level
X=Don't care
Z=High impedance "off " state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0-B_7			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	A_0-A_7, B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
		B_0-B_7		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = 5.5V, V_I =5.5V					1.0	mA
I_{IH}	High-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 2.7V					40	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-40	µA
I_{OZH} +I_{IH}	Off state output current, High-level voltage applied		V_{CC} = MAX, V_I = 2.7V					70	µA
I_{OZL}+I_{IL}	Off state output current, Low-level voltage applied		V_{CC} = MAX, V_i = 0.5V					-70	µA
I_{OS}	Short circuit output current[3]	A_0-A_7	V_{CC} = MAX			-60		-150	mA
		B_0-B_7				-100		-225	µA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = MAX	T/$\overline{R}$=A_n=4.5V, $\overline{OE}$=GND			77	90	mA
		I_{CCL}		$\overline{OE}$=T/$\overline{R}$=B_n=GND			96	120	mA
		I_{CCZ}		T/$\overline{R}$=B_n=GND, $\overline{OE}$=4.5V			89	110	mA

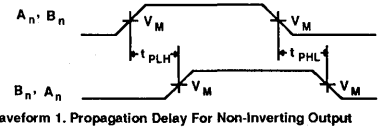
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with outputs open.

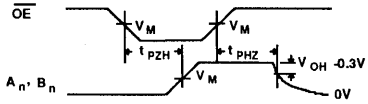
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	Waveform 1	1.5 2.5	3.5 4.5	5.5 6.5	1.5 2.5	6.5 7.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	6.0 5.5	8.5 8.0	10.5 9.5	6.0 5.5	11.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 2 Waveform 3	2.5 2.0	5.0 4.5	7.0 6.5	2.5 2.0	8.0 7.5	ns

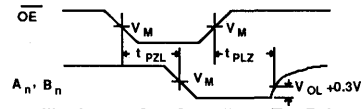
AC WAVEFORMS



Waveform 1. Propagation Delay For Non-Inverting Output



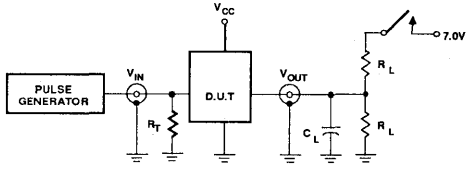
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

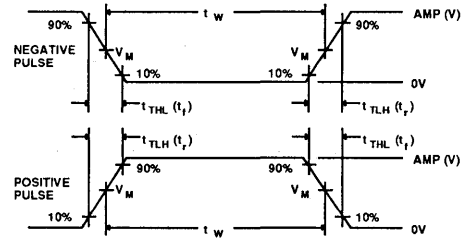
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F547
Decoder/Demultiplexer

FAST Products

Octal Decoder/Demultiplexer With Address Latches And Acknowledge (Open Collector)
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F547	8.0 ns	17mA

FEATURES

- **3-to-8 line address decoder**
- **Address storage latches**
- **Multiple enables for address extension**
- **Open Collector Acknowledge output**

DESCRIPTION

The 74F547 is a 3-to-8 line address decoder withn latches for address storage. Designed primarily to simplify multiple-chip selection in a microprocessor system, it contains one active Low and two active High Enables to conserve address space. Also included is an active Low Acknowledge output that responds to either a Read or Write input signal when the Enables are active.

For applications in which the separation of latch enable and chip enable functions is not required, LE and $\overline{E}_0$ can be tied together such that when High the outputs are OFF and the latches are transparent, and when Low the latches are storing and the selected output is enabled. The Open-Collector Acknowledge ($\overline{ACK}$) output is normally High (i.e.OFF) and goes Low when $\overline{E}_0$, E_1 and E_2 are all active and either the Read ($\overline{RD}$) or Write ($\overline{WR}$) input is Low, as indicated in the Acknowlege Function Table.

ORDERING INFORMATION

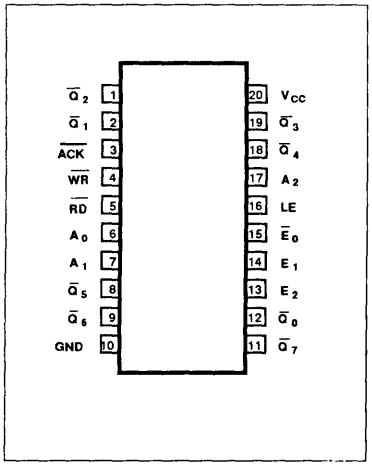
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F547N
20-Pin Plastic SOL	N74F547D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

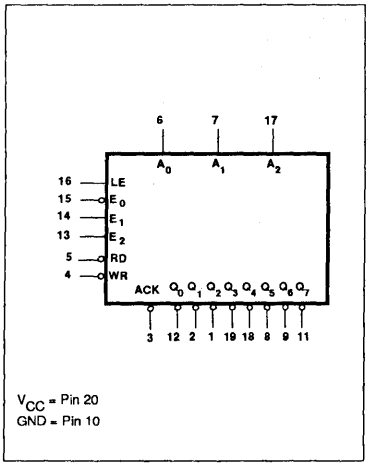
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	Output select address input	1.0/1.0	20µA/0.6mA
$\overline{E}_0$	Chip enable input (active Low)	1.0/1.0	20µA/0.6mA
E_1, E_2	Chip enable inputs	1.0/1.0	20µA/0.6mA
LE	Latch enable input	1.0/1.0	20µA/0.6mA
$\overline{RD}$	Read ackowledge input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{WR}$	Write ackowledge input (active Low)	1.0/1.0	20µA/0.6mA
Q_0 -Q_7	Decoder outputs (active Low)	50/33	1.0mA/20mA
$\overline{ACK}$	Open Collector Acknowledge output (active Low)	OC/33	OC/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC=Open collector

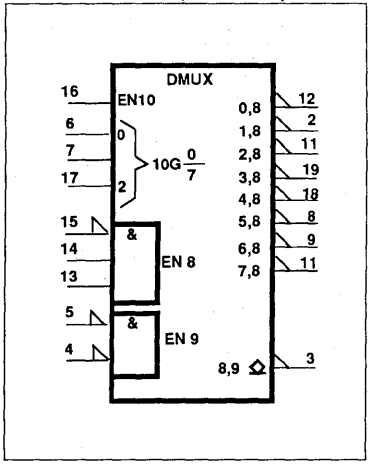
PIN CONFIGURATION



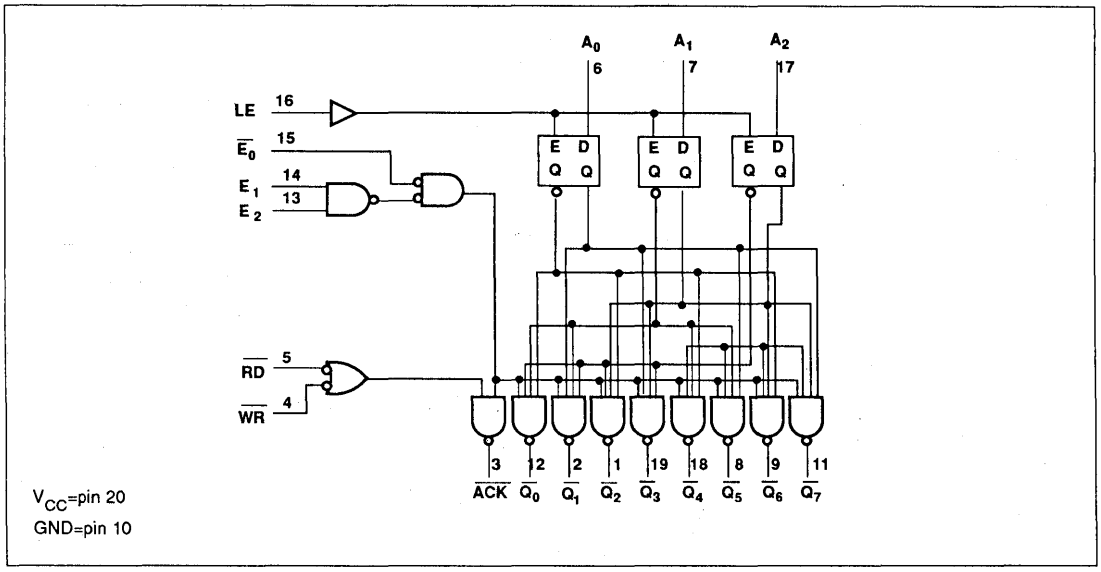
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



DECODER FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_0$	E_1	E_2	A_2	A_1	A_0	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$
L	H	H	L	L	L	L	H	H	H	H	H	H	H
L	H	H	L	L	H	H	L	H	H	H	H	H	H
L	H	H	L	H	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	H	L	L	H	H	H	H	L	H	H	H
L	H	H	H	L	H	H	H	H	H	H	L	H	H
L	H	H	H	H	L	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ACKNOWLEDGE FUNCTION TABLE

INPUTS					OUTPUT
$\overline{E}_0$	E_1	E_2	$\overline{RD}$	$\overline{WR}$	$\overline{ACK}$
H	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
L	H	H	H	H	H
L	H	H	L	X	L
L	H	H	X	L	L

H = High voltage level
L = Low voltage level
X = Don't care

LATCH and OUTPUT STATUS FUNCTION TABLE

INPUTS				LATCH STATUS	DECODER OUTPUTS
$\overline{E}_0$	E_1	E_2	LE		
L	H	H	H	Transparent	Address inputs decoded
L	H	H	L	Storing	Latched address decoded
H	X	X	H	Transparent	Outputs disabled (High)
H	X	X	L	Storing	
X	L	X	H	Transparent	
X	L	X	L	Storing	
X	X	L	H	Transaprent	
X	X	L	L	Storing	

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_K	Input clamp current				-18	mA
V_{OH}	High-level output voltage	$\overline{ACK}$ only			4.5	V
I_{OH}	High-level output current	Except $\overline{ACK}$			-1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current	$\overline{ACK}$ only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OH}	High-level output voltage	Except $\overline{ACK}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short-circuit output current[3]	Except $\overline{ACK}$	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX				17	25	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

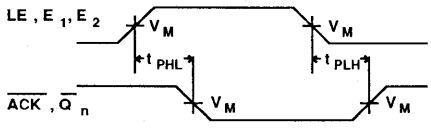
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Q}_n$	Waveform 3	2.0 4.5	4.5 7.0	9.0 12.0	1.5 4.0	10.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$ to $\overline{Q}_n$	Waveform 2	2.5 3.0	4.5 5.5	8.5 8.5	2.0 3.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to $\overline{Q}_n$	Waveform 1	3.5 5.0	6.0 10.5	10.0 14.0	3.0 5.0	11.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay E_1 or E_2 to $\overline{Q}_n$	Waveform 1	4.0 4.0	6.0 6.0	10.0 10.0	3.0 4.0	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$, $\overline{RD}$, or $\overline{WR}$ to $\overline{ACK}$	Waveform 2	6.5 3.5	9.0 5.5	13.0 9.5	6.5 3.0	14.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay E_1 or E_2 to $\overline{ACK}$	Waveform 1	7.5 4.5	11.0 6.5	14.0 10.0	7.0 4.0	15.0 11.0	ns

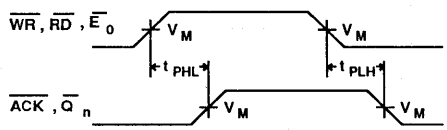
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n to LE	Waveform 4	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n to LE	Waveform 4	6.0 6.0			6.0 6.0		ns
$t_w(H)$	LE Pulse width, High	Waveform 4	6.0			6.0		ns

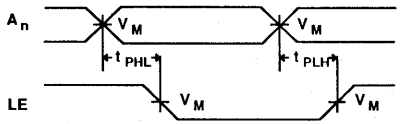
AC WAVEFORMS



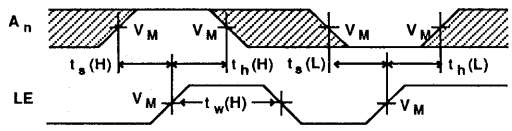
Waveform 1. Propagation Delay for Enable inputs and Latch Enable input to Acknowledge and decoder outputs



Waveform 2. Propagation Delay for Enable input to decoder outputs and Write and Read inputs to Acknowledge output



Waveform 3. Propagation Delay for output select Address input to decoder outputs

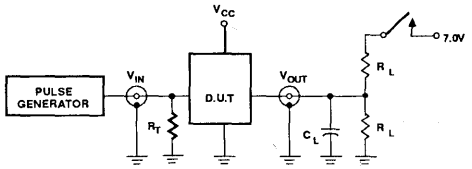


Waveform 4. Data Setup And Hold Times and Latch Enable pulse width

NOTE: For all waveforms, V_M = 1.5V.

The shaded area indicate when the input is permitted to change for predictable ouput.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs

SWITCH POSITION

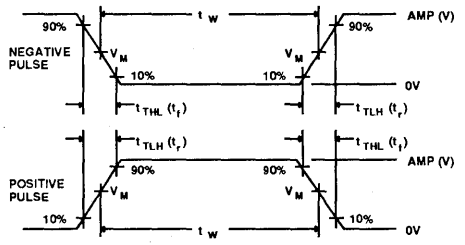
TEST	SWITCH
Open Collector	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F548
Decoder/Demultiplexer

FAST Products

Octal Decoder/Demultiplexer With Acknowledge (Open Collector)
Product Specification

FEATURES
- **3-to-8 line address decoder**
- **Multiple enables for address extension**
- **Open Collector Acknowledge output**
- **Active-Low Decoder outputs**

DESCRIPTION
The 74F548 is a 3-to-8 line address decoder with four Enable inputs. Two of the Enables are active-Low and two are active-High for maximum addressing versatility. Also provided is an active-Low Acknowledge output that responds to either a Read or Write input signal when the Enables are active.

When enabled, the 'F548 accepts the A_0-A_2 address inputs and decodes them to select one of eight active-Low mutually exclusive outputs, as shown in the Decoder FunctionTable. When one or more Enables is active, all decoder outputs are High. Thus, the 'F548 can be used as a demultiplexer by applying data to one of the Enables.

The Open Collector Acknowledge ($\overline{ACK}$) output is normally High (i.e.OFF) and goes Low when the Enables are all active and either the Read ($\overline{RD}$) or Write ($\overline{WR}$) input is Low, as indicated in the Acknowledge Function Table.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F548	6.5 ns	14mA

ORDERING INFORMATION

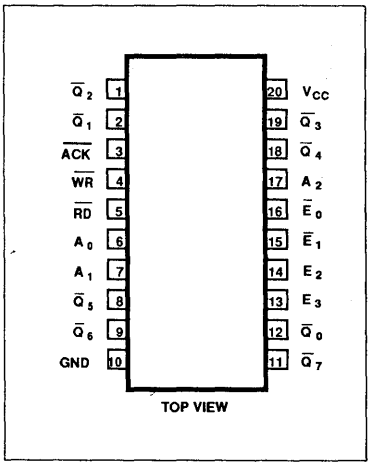
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F548N
20-Pin Plastic SOL	N74F548D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

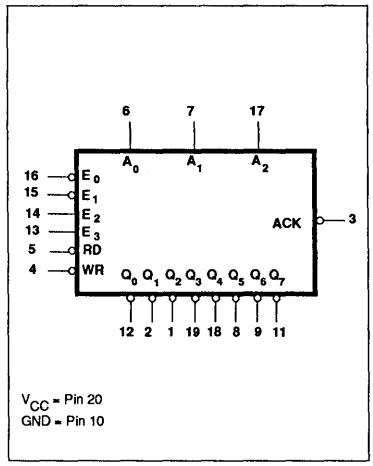
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_2	Output select address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_0$, $\overline{E}_1$	Chip enable inputs (active Low)	1.0/1.0	20µA/0.6mA
E_2, E_3	Chip enable inputs	1.0/1.0	20µA/0.6mA
$\overline{RD}$	Read ackowledge input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{WR}$	Write ackowledge input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{Q}_0$ - $\overline{Q}_7$	Decoder outputs (active Low)	50/33	1.0mA/20mA
$\overline{ACK}$	Open Collector Acknowledge output (active Low)	OC/33	OC/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC=Open collector

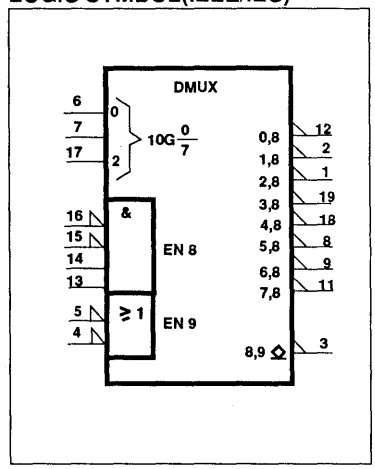
PIN CONFIGURATION



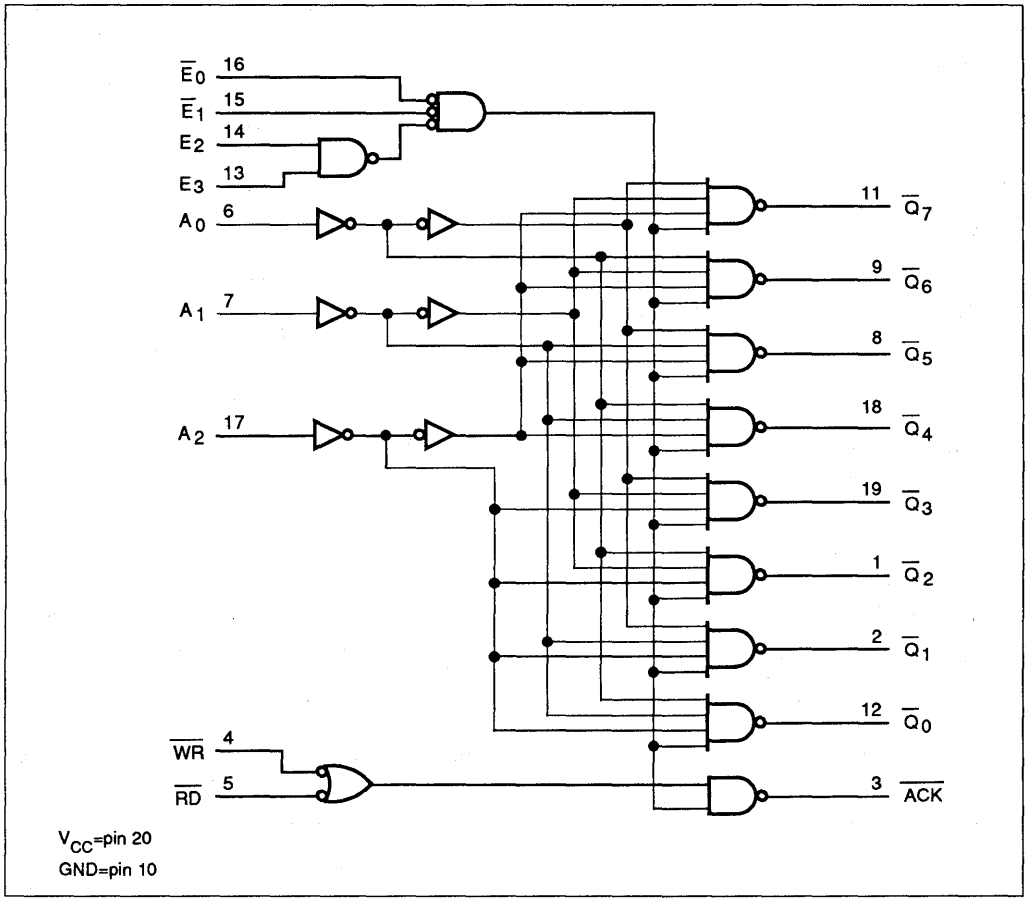
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



DECODER FUNCTION TABLE

INPUTS							OUTPUTS							
$\overline{E}_0$	$\overline{E}_1$	E_2	E_3	A_2	A_1	A_0	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$
H	X	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	X	H	H	H	H	H	H	H	H
X	X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ACKNOWLEDGE FUNCTION TABLE

INPUTS						OUTPUT
$\overline{E}_0$	E_1	E_2	E_3	$\overline{RD}$	$\overline{WR}$	$\overline{ACK}$
H	X	X	X	X	X	H
X	H	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
L	L	H	H	H	H	H
L	L	H	H	L	X	L
L	L	H	H	X	L	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_K	Input clamp current				-18	mA
V_{OH}	High-level output voltage	$\overline{ACK}$ only			4.5	V
I_{OH}	High-level output current	Except $\overline{ACK}$			-1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current	$\overline{ACK}$ only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OH}	High-level output voltage	Except $\overline{ACK}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximuminput voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short circuit output current[3]	Except $\overline{ACK}$	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX				14	21	mA

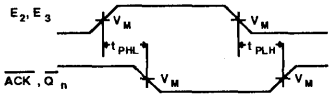
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

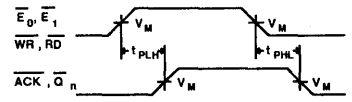
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Q}_n$	Waveform 3	2.0 4.0	4.5 6.5	8.0 9.5	1.5 4.0	9.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$ or $\overline{E}_1$ to $\overline{Q}_n$	Waveform 2	2.5 3.5	4.5 5.5	8.5 8.5	2.0 3.0	9.5 9.5	ns
t_{PHL} t_{PLH}	Propagation delay E_2 or E_3 to $\overline{Q}_n$	Waveform 1	4.0 4.0	6.0 6.0	9.5 9.5	3.0 3.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$ or $\overline{E}_1$ to $\overline{ACK}$	Waveform 1	6.5 3.0	9.5 6.0	12.5 9.5	6.5 3.0	13.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay E_2 or E_3 to $\overline{ACK}$	Waveform 1	8.0 4.0	11.0 7.0	14.0 10.0	8.0 4.0	15.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{RD}$ or $\overline{WR}$ to $\overline{ACK}$	Waveform 2	5.5 2.5	9.0 5.0	12.0 8.0	5.5 2.5	12.5 8.5	ns

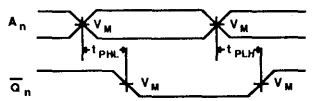
AC WAVEFORMS



Waveform 1. Propagation Delay for Chip Enable (E_2, E_3) Inputs to Write Acknowledge and Decoder Outputs



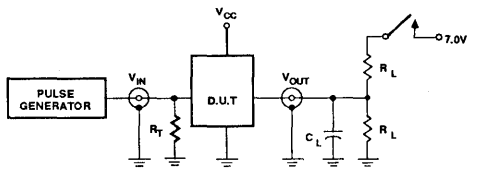
Waveform 2. Propagation Delay for Chip Enable ($\overline{E}_0$, $\overline{E}_1$), inputs to Decoder and Write Acknowlege Outputs and Read or Write Acknowledge Inputs to Write Acknowledge Outputs



Waveform 3. Propagation Delay for Output Select Address Input to Decoder Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs

SWITCH POSITION

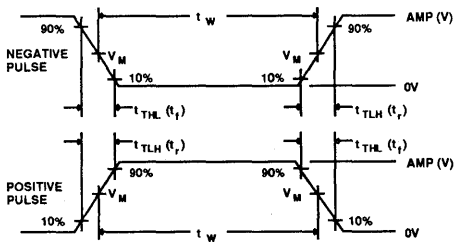
TEST	SWITCH
Open Collector	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F552 Transceiver

Octal Registered Transceiver With Parity and Flags (3-State)

FAST Products

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F552	85MHz	120mA

FEATURES

- **8-Bit bidirectional I/O port with handshake**
- **Register status flag flip-flops**
- **Separate clock enable and output enable**
- **Parity generation and parity check**
- **B outputs and parity output sink 64mA**

DESCRIPTION

The 74F552 Octal Registered Transceiver contains two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock (CPR, CPS) and Clock Enable ($\overline{CER}$, $\overline{CES}$) inputs, as well as a flag flip-flop that is set automatically as the register is loaded. The flag output will be reset when the Output Enable returns to High after reading the output port. Each register has a separate Output Enable ($\overline{OEAS}$, $\overline{OEBR}$) for its 3-state buffer. The separate Clocks, Flags and Enables provide considerable flexibility as I/O ports for demand-response data transfer. When data is transferred from the A port to the B port, a parity bit is generated. On the other hand, when data is transferred from the B port to the A port, the parity of input data on B_0-B_7 is checked.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP (600mil)	N74F552N
28-Pin Plastic SOL[1]	N74F552D

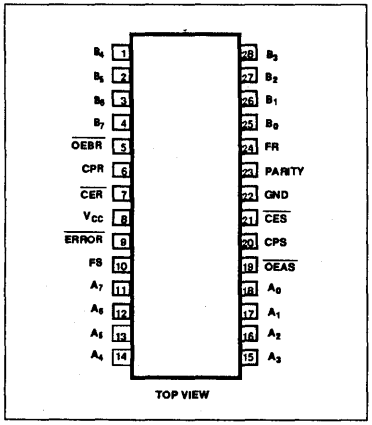
NOTE:
1. Thermal mounting technique are recommended. See AN SMD-100 Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

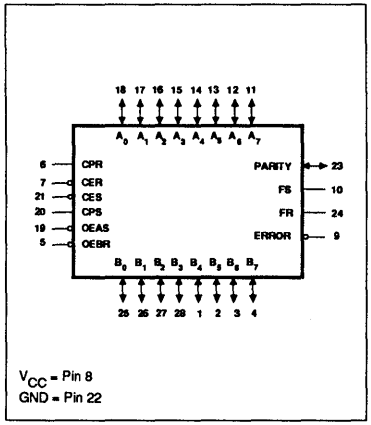
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A-to-B Data inputs	3.5/1.0	70µA/0.6mA
B_0 - B_7	B-to-A Data inputs	3.5/1.0	70µA/0.6mA
CPR	R registers clock input (active rising edge)	1.0/1.0	20µA/0.6mA
CPS	S registers clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{CER}$	R registers clock Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CES}$	S registers clock Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OEBR}$	A-to-B Output Enable input (active Low) and clear FS output (active Low)	1.0/2.0	20µA/1.2mA
$\overline{OEAS}$	B-to-A Output Enable input (active Low) and clear FR output (active Low)	1.0/2.0	20µA/1.2mA
PARITY	Parity bit transceiver input	3.5/1.0	70µA/0.6mA
	Parity bit transceiver output	750/106.7	15mA/64mA
$\overline{ERROR}$	Parity check output (active Low)	50/33.3	1.0mA/20mA
A_0 - A_7	A-to-B Data outputs	150/40	3.0mA/24mA
B_0 - B_7	B-to-A Data outputs	750/106.7	15mA/64mA
FR	A-to-B Status Flag output (active High)	50/33.3	1.0mA/20mA
FS	B-to-A Status Flag output (active High)	50/33.3	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

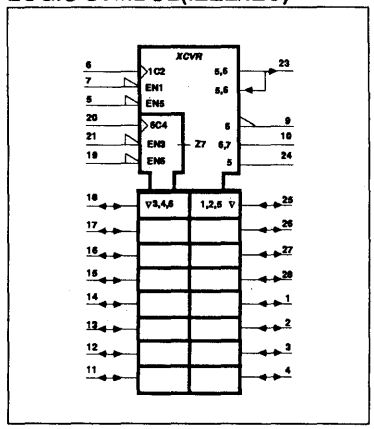
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



FUNCTIONAL DESCRIPTION

Data applied to the A inputs are entered and stored on the rising edge of the CPR clock pulse, provided that the $\overline{CER}$ is Low; simultaneously, the status flip-flop is set and the A-to-B flag (FR) output goes High. As the $\overline{CER}$ returns to High, the data will be held in R register. This data entered from the A inputs will appear at the B port I/O pins after the $\overline{OEBR}$ has gone Low. When $\overline{OEBR}$ is Low, a parity bit appears at the PARITY pin, which will be set High when there is an even number of 1s or all 0s at the Q outputs of the R register. After the data is assimilated, the receiving system clears the flag FR, by changing the signal at the $\overline{OEBR}$ pin from Low to High. Data flow from B-to-A proceeds in the same manner described for A-to-B flow. A Low at the $\overline{CES}$ pin and a Low-to-High transition at the CPS pin enters the B input data and the parity input data into the S register and the parity register respectively and set the flag output FS to HIgh. A Low signal at the $\overline{OEAS}$ pin enables the A port I/O pins and a Low-to-High transition of the $\overline{OEAS}$ signal clears the FS flag. When $\overline{OEAS}$ is Low, the parity check output $\overline{ERROR}$ will be High if there is an odd number of 1s at the Q outputs of the S registers and the parity register.

R or S REGISTER FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
A_n or B_n	CPX	$\overline{CEX}$	INTERNAL Q	
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	
X	↧	L	NC	Keep old data

H= High voltage level
L= Low voltage level
NC=No change
X=Don't care
X=R or S for CPX and $\overline{CEX}$
↑ =Low-to-High transition
↧ =Not Low-to-High transition

OUTPUT CONTROL TABLE

INPUT	OUTPUTS		OPERATING MODE
$\overline{OEXX}$	INTERNAL Q	A_n or B_n	
H	X	Z	Disable outputs
L	L	L	Enable outputs
L	H	H	

H= High voltage level
L= Low voltage level
X=Don't care
XX=AS or BR
Z =High impedance "off" state

R or S FLAG FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{CEX}$	CPX	$\overline{OEXX}$	FR or FS	
H	X	↧	NC	Hold flag
L	↑	↧	H	Set flag
X	X	↑	L	Clear flag

H= High voltage level
L= Low voltage level
NC=No change
X=Don't care
X=R or S for CPX and $\overline{CEX}$
XX=AS or BR
↑ =Low-to-High transition
↧ =Not Low-to-High transition

PARITY GENERATION FUNCTION TABLE

INPUTS		OUTPUTS		OPERATING MODE
$\overline{OEBR}$	CPR	Number of Highs in the Q outputs of the R register	PARITY	
H	↑	X	Z	Hold data
L	↑	0,2,4,6,8	H	Load data
L	↑	1,3,5,7	L	

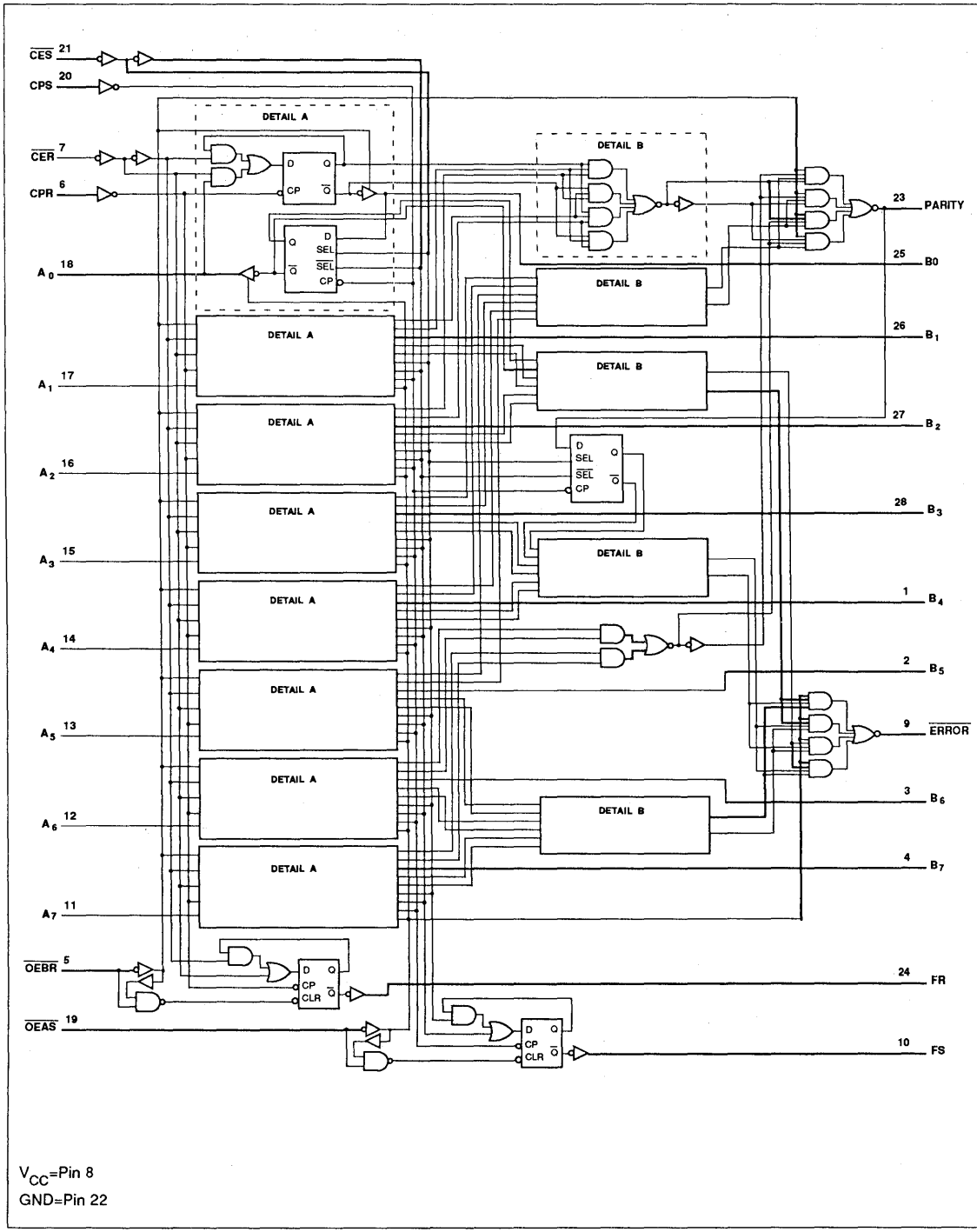
H= High voltage level
L= Low voltage level
X=Don't care
Z =High impedance "off" state
↑ =Low-to-High transition

PARITY CHECK FUNCTION TABLE

INPUTS			OUTPUTS		OPERATING MODE
$\overline{OEAS}$	CPS	PARITY	Number of Highs in the Q outputs of the R register	$\overline{ERROR}$	
H	↑	X	X	H	Parity check
L	↑	L	0,2,4,6,8	L	
L	↑	L	1,3,5,7	H	
L	↑	H	0,2,4,6,8	H	
L	↑	H	1,3,5,7	L	

H= High voltage level
L= Low voltage level
X=Don't care
↑ =Low-to-High transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to $+V_{CC}$	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	FR, FS, $\overline{ERROR}$	40	mA
		A_0- A_7	48	mA
		B_0- B_7, PARITY	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	FR, FS, $\overline{ERROR}$			-1	mA
		A_0- A_7			-3	mA
		B_0- B_7, PARITY			-15	mA
I_{OL}	Low-level output current	FR, FS, $\overline{ERROR}$			20	mA
		A_0- A_7			24	mA
		B_0- B_7, PARITY			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	FR, FS, $\overline{ERROR}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		A_0- A_7		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
		B_0- B_7, PARITY		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	FR, FS, $\overline{ERROR}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=20mA	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
		A_0- A_7		I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0- B_7, PARITY		I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = MAX, V_I = 7.0V					100	µA
		A_0- A_7, B_0- B_7, PARITY	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	others except A_0- A_7, B_0- B_7, PARITY	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	others	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		$\overline{OEAS}$, $\overline{OEBA}$						-1.2	mA
I_{OZH}+ I_{IH}	Off-state output current, High-level voltage applied	A_0- A_7, B_0- B_7, PARITY	V_{CC} = MAX, V_O= 2.7V					70	µA
I_{OZL}+ I_{IL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-600	µA
I_{OS}	Short-circuit Output current[3]	A_0-A_7, FS, FR, $\overline{ERROR}$	V_{CC} = MAX			-60		-150	mA
		B_0-B_7, PARITY				-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				115	170	mA
		I_{CCL}					125	185	mA
		I_{CCZ}					120	180	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

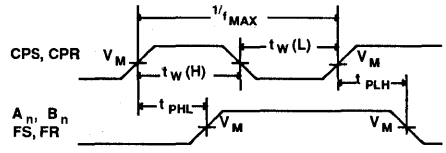
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	Waveform 1	70	85		60		MHz
t_{PLH} t_{PHL}	Propagation delay CPS to A_n or CPR to B_n	Waveform 1	3.5 4.0	5.0 6.0	8.0 9.0	3.0 3.5	8.5 9.0	ns
t_{PLH}	Propagation delay CPS to FS or CPR to FR	Waveform 1	3.0	5.0	7.5	2.5	8.5	ns
t_{PHL}	Propagation delay $\overline{OEAS}$ to FS or $\overline{OEBR}$ to FR	Waveform 2	4.0	6.0	8.5	3.5	9.0	ns
t_{PLH} t_{PHL}	Propagation delay CPS to $\overline{ERROR}$	Waveform 4	6.5 7.5	13.0 11.5	16.5 15.0	6.0 7.0	18.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay CPR to PARITY	Waveform 4	6.5 10.5	8.5 13.5	11.0 17.0	5.5 10.0	12.5 18.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OEAS}$ to $\overline{ERROR}$	Waveform 3	3.5 3.0	5.5 5.0	8.0 7.0	3.0 2.5	8.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEAS}$ to A_n or $\overline{OEBR}$ to B_n	Waveform 7 Waveform 8	2.5 4.0	4.0 6.5	7.0 9.5	2.0 4.0	8.0 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEAS}$ to An or $\overline{OEBR}$ to B_n	Waveform 7 Waveform 8	2.0 2.0	4.0 3.5	7.0 7.0	1.5 1.5	8.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBR}$ to PARITY	Waveform 7 Waveform 8	2.0 4.0	4.0 5.5	7.0 8.0	2.0 3.0	7.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBR}$ to PARITY	Waveform 7 Waveform 8	2.0 2.0	4.0 4.0	7.0 7.5	2.0 2.0	7.5 8.0	ns

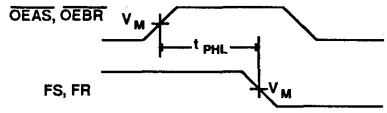
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n or B_n or PARITY to CPS or CPR	Waveform 5	7.5 4.5			8.5 5.5		ns
t_h(H) t_h(L)	Hold time, High or Low A_n or B_n or PARITY to CPS or CPR	Waveform 5	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low $\overline{CES}$ to CPS or $\overline{CER}$ to CPR	Waveform 5	7.0 7.0			7.5 7.5		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{CES}$ to CPS or $\overline{CER}$ to CPR	Waveform 5	0 0			0 0		ns
t_w(H) t_w(L)	CPS or CPR Pulse width, High or Low	Waveform 1	5.0 6.5			6.5 7.5		ns
t_{rec}	Recovery time $\overline{OEBR}$ to CPR or $\overline{OEAS}$ to CPS	Waveform 6	14.5			16.5		ns

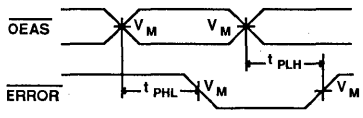
AC WAVEFORMS



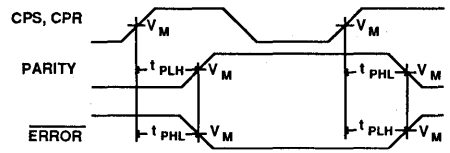
Waveform 1. Propagation Delay, Clock input to output and maximum clock frequency



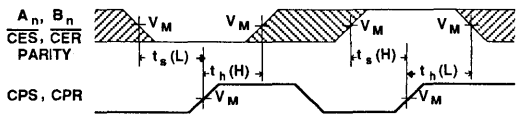
Waveform 2. Propagation Delay, Output Enable to Flag output



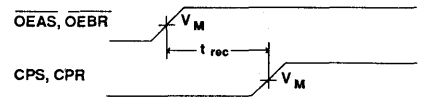
Waveform 3. Propagation Delay, Output Enable to ERROR



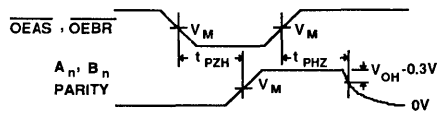
Waveform 4. Propagation Delay, Clock to PARITY and ERROR



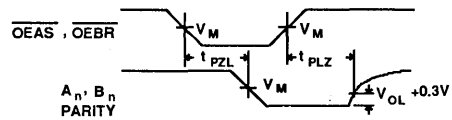
Waveform 5. Data Setup And Hold Times



Waveform 6. Recovery time from Output Enable to Clock



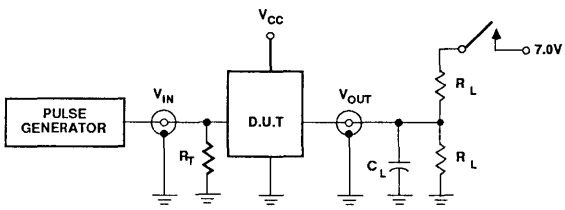
Waveform 7. 3-State Output Enable Time To High Level And Output Disable Time From High Level



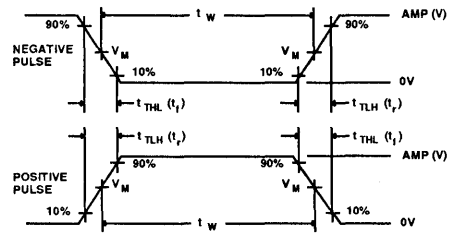
Waveform 8. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded area indicate when the input is permitted to change for predictable output

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F563, 74F564
Latch/Flip-Flop

74F563 Octal Transparent Latch (3-State)
74F564 Octal D Flip-Flop (3-State)
Product Specification

FAST Products

FEATURES

- **74F563 is broadside pinout version of 74F533**
- **74F564 is broadside pinout version of 74F534**
- **Inputs and Outputs on opposite side of package allow easy interface to Microprocessors**
- **Useful as an Input or Output port for Microprocessors**
- **3-State Outputs for Bus interfacing**
- **Common Output Enable**
- **74F573 and 74F574 are non-inverting versions of 74F563 and 74F564 respectively**
- **These are High-Speed replacements for N8TS807 and N8TS808**

DESCRIPTION

The 74F563 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F563	5.0ns	55mA
74F564	4.5ns	50mA

ORDERING INFORMATION

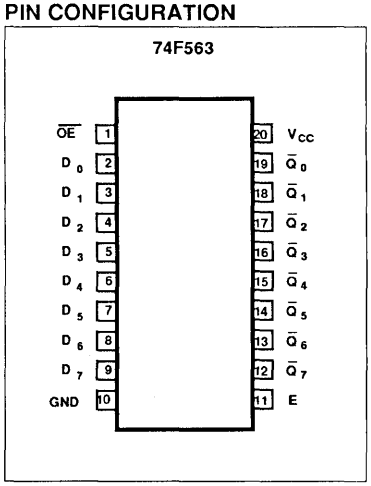
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F563N, N74F564N
20-Pin Plastic SOL	N74F563D, N74F564D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

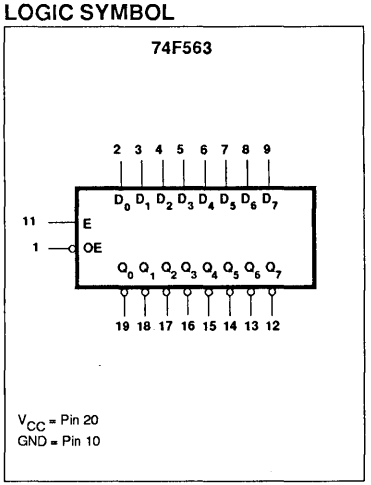
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20µA/0.6mA
E ('F563)	Latch Enable input (active High)	1.0/1.0	20 A /0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
CP ('F564)	Clock Pulse input (active rising edge)	1.0/1.0	20 A /0.6mA
$\overline{Q}_0$ - $\overline{Q}_7$	3-State outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

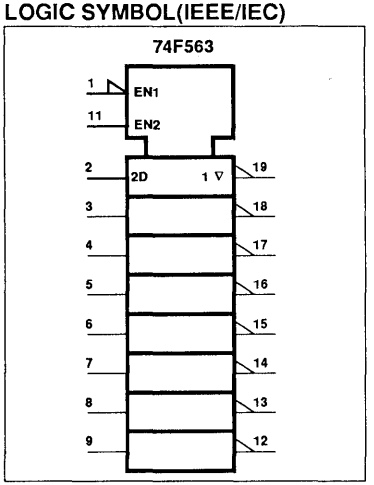
PIN CONFIGURATION



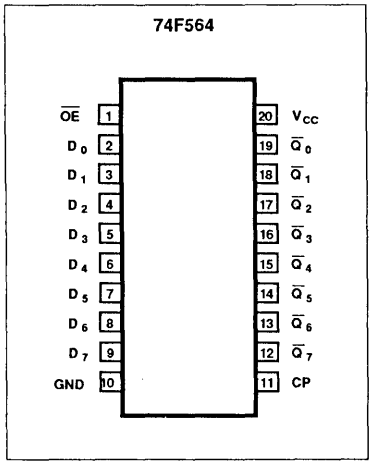
LOGIC SYMBOL



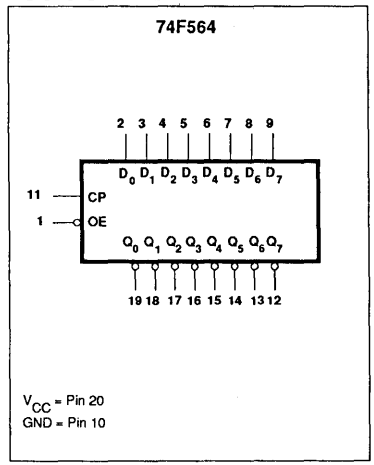
LOGIC SYMBOL(IEEE/IEC)



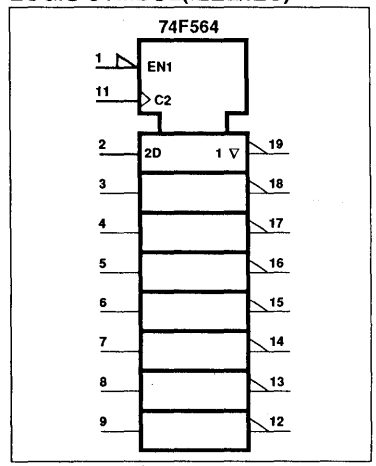
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



The 74F563 is functionally identical to the 74F533 but has a broadside pinout configuration to facilitate PC board layout and allows easy interface with microprocessors.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the data that is present one set-up time before the High-to-Low enable transition.

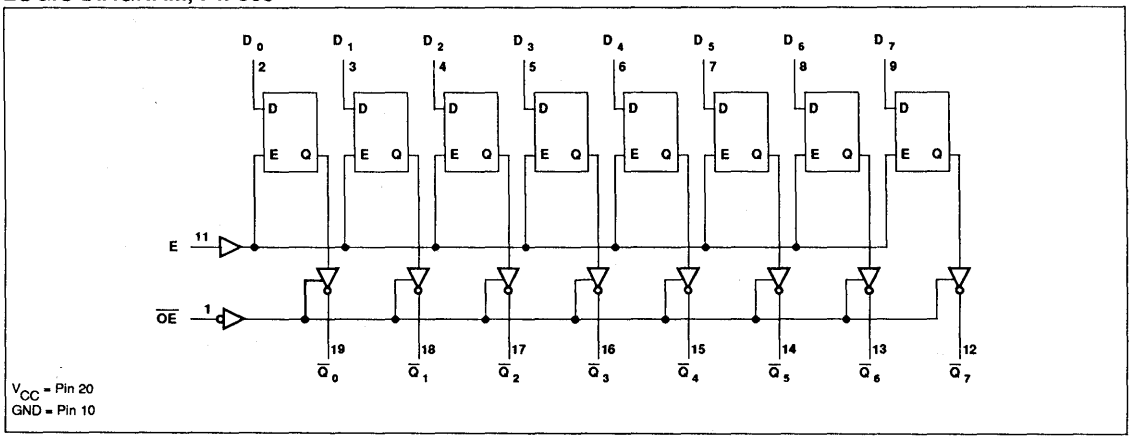
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independently of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74F564 is functionally identical to the 74F534 but has a broadside pinout configuration to facilitate PC board layout and allows easy interface with microprocessors.

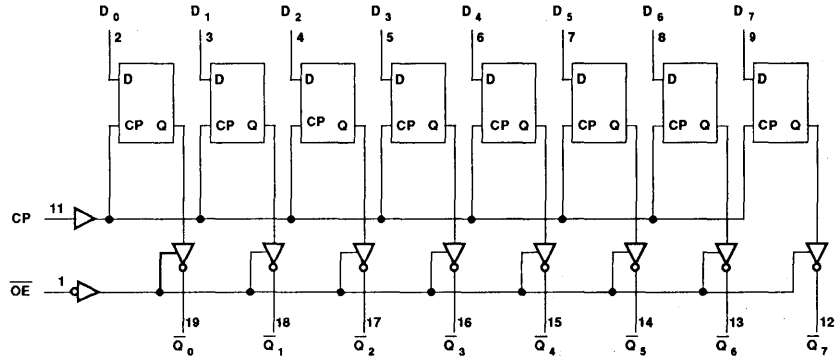
It is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates. The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's $\overline{Q}$ output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independently of the register operation. When $\overline{OE}$ is Low, data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 74F563



LOGIC DIAGRAM, 74F564



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE, 74F563

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	D_n	REGISTER	$\overline{Q}_0$ - $\overline{Q}_7$	
L	H	L	L	H	Enable and read register
L	H	H	H	L	
L	↓	l	L	H	Latch and read register
L	↓	h	H	L	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	D_n	D_n	Z	

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

FUNCTION TABLE, 74F564

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	D_n	REGISTER	$\overline{Q}_0$ - $\overline{Q}_7$	
L	↑	l	L	H	Load and read register
L	↑	h	H	L	
L	↟	X	NC	NC	Hold
H	↟	X	NC	Z	Disable outputs
H	↑	D_n	D_n	Z	

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↟ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	74F563		30	45	mA
		I_{CCL}			40	60	mA
		I_{CCZ}			45	65	mA
		I_{CCH}	74F564		45	65	mA
		I_{CCL}			50	75	mA
		I_{CCZ}			55	80	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

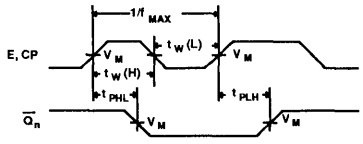
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	74F563	Waveform 2	4.0 2.5	6.5 4.5	9.0 7.0	3.5 2.0	10.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay E to $\overline{Q}_n$		Waveform 1	5.0 3.0	7.0 5.0	10.0 7.5	4.5 3.0	11.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	3.5 4.0	6.0 6.0	10.5 8.0	3.0 3.5	11.5 9.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	1.5 1.0	3.0 2.5	6.0 5.5	1.0 1.0	7.0 6.0	ns ns
f_{MAX}	Maximum Clock frequency	74F564	Waveform 1	110	125		100		ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$		Waveform 1	3.5 3.5	5.5 5.5	8.5 8.5	3.0 3.0	9.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 4 Waveform 5	2.5 4.0	4.5 6.0	7.5 8.5	1.5 3.5	8.5 9.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	1.0 1.0	3.0 2.5	6.0 5.5	1.0 1.0	7.0 6.0	ns ns

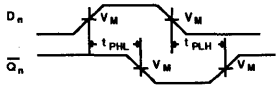
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time D_n to E	74F563	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to E		Waveform 3	3.0 2.5			3.0 2.5		ns
$t_w(H)$	E Pulse width, High		Waveform 1	3.5			3.5		ns
$t_s(H)$ $t_s(L)$	Set-up time D_n to CP	74F564	Waveform 3	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP		Waveform 3	2.0 2.0			2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1	4.5 4.5			4.5 4.5		ns

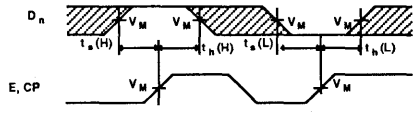
AC WAVEFORMS



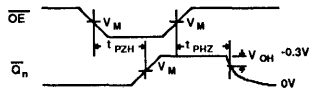
Waveform 1. Propagation Delay, Clock And Enable Inputs To Output, Enable, and Clock Pulse Widths, and Maximum Clock Frequency



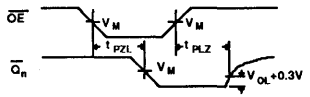
Waveform 2. Propagation Delay For Data To Outputs



Waveform 3. Data Setup And Hold Times



Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

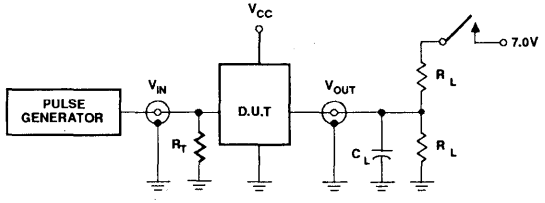


Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

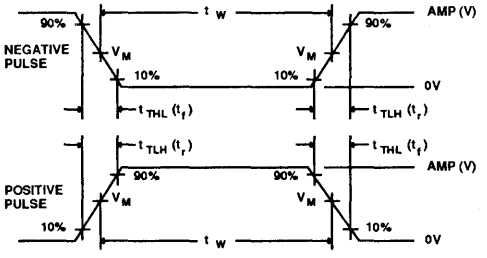
NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F568, 74F569 Counters

'F568 4-Bit Bidirectional Decade Synchronous Counter (3-state)
'F569 4-Bit Bidirectional Binary Synchronous Counter (3-state)
Product Specification

FAST Products

FEATURES

- **4-bit bidirectional counting**
  - **'F568 Decade counter**
  - **'F569 Binary counter**
- **Synchronous counting and loading**
- **Look ahead carry capability for easy cascading**
- **Preset capability for programmable operation**
- **Master Reset ($\overline{MR}$) overrides all other inputs**
- **Synchronous Reset ($\overline{SR}$) overrides counting and parallel loading**
- **Clock Carry ($\overline{CC}$) output to be used as a clock for flip-flops, register and counters**
- **3-state outputs for bus organized systems**

DESCRIPTION

The 74F568 and 74F569 are fully synchronous Up/Down Counters. The 74F568 is a BCD decade counter; the 74F569 is a binary counter. They feature preset capability for programmable operation, carry look ahead for easy cascading, and U/$\overline{D}$ input to control the direction of counting. For maximum flexibility there are both Synchronous and Master Reset inputs as well as both Clocked Carry ($\overline{CC}$) and Terminal Count ($\overline{TC}$) outputs. All state changes except Master Reset are initiated by rising edge of the clock. A High signal on the Output Enable ($\overline{OE}$) input forces the output buffers into the high impedance state but does not prevent counting, resetting or parallel loading.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F568	115MHz	40mA
74F569	115MHz	40mA

ORDERING INFORMATION

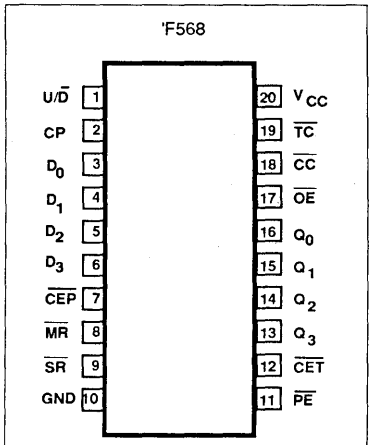
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic Dip	N74F568N, N74F569N
20-Pin Plastic Dip	N74F568D, N74F569D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

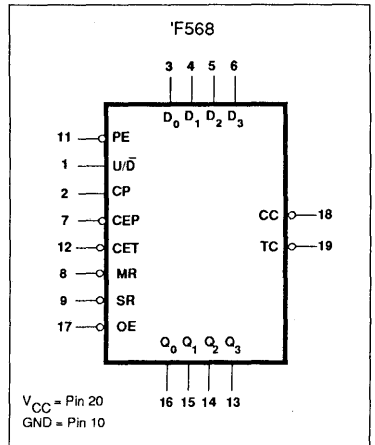
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Parallel data inputs	1.0/1.0	20µA/0.6mA
$\overline{CEP}$	Count Enable parallel input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/2.0	20µA/1.2mA
CP	Clock input (active rising edge)	1.0/1.0	20 A /0.6mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/2.0	20µA/1.2mA
U/$\overline{D}$	Up/Down count control input	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Resert input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{SR}$	Synchronous Reset (active Low)	1.0/1.0	20µA/0.6mA
$\overline{TC}$	Terminal Count output (active Low)	50/33	1.0mA/20mA
$\overline{CC}$	Clocked Carry output (active Low)	50/33	1.0mA/20mA
Q_0 -Q_3	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

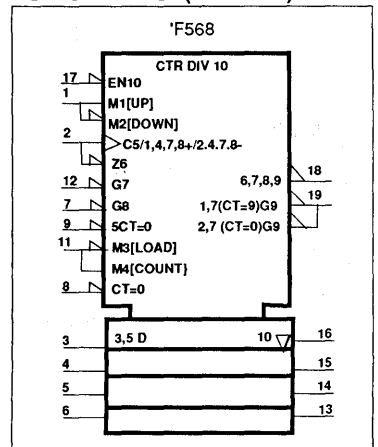
PIN CONFIGURATION



LOGIC SYMBOL

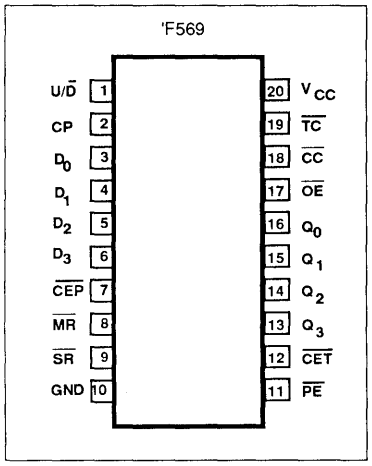


LOGIC SYMBOL(IEEE/IEC)

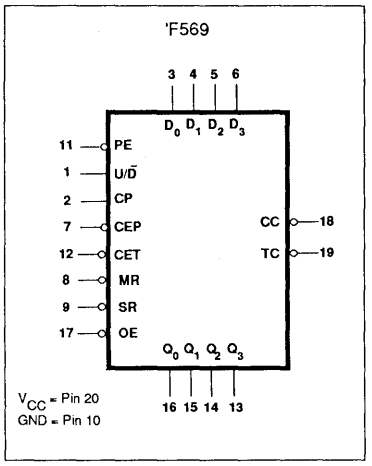


Counters | FAST 74F568, 74F569

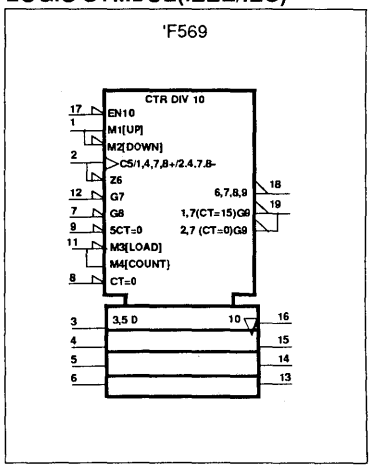
PIN CONFIGURATION



LOGIC SYMBOL



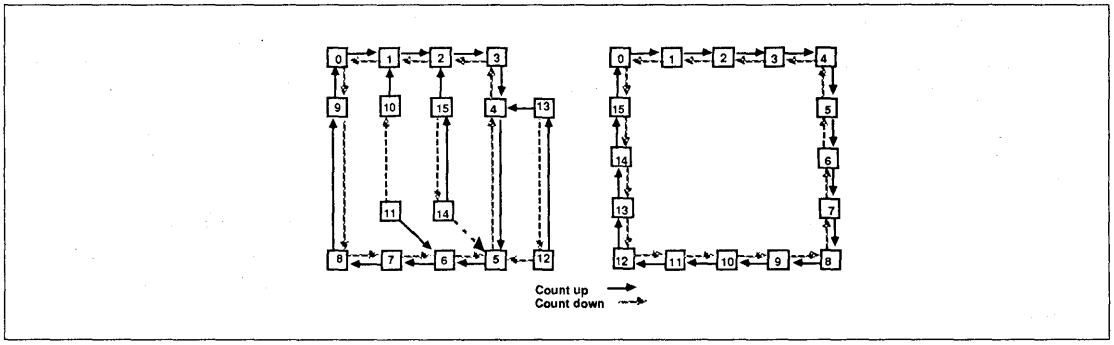
LOGIC SYMBOL(IEEE/IEC)



FUNCTIONAL DESCRIPTION

The 74F568 counts modulo-10 in the BCD(8421) sequence. From state 0 (LLLL) it increments to 9 (HLLH) in the up mode; in the down mode it will decrement 9 to 0. The 74F569 counts in the modulo-16 binary sequence. From state 0 (LLLL) it will increment to 15 in the up mode; in the down mode it will decrement from 15 to 0. The clock inupts of all flip-flops are driven in parallel through a clock buffer. All state changes (except due to Master Reset) occur synchronously with the Low-to-High transition of the Clock Pulse(CP) input signal.

STATE DIAGRAM



The circuits have five fundamental modes of operation, in order of precedence: asynchronous reset, synchronous reset, parallel load, count and hold. Six control inputs-Master Reset ($\overline{MR}$) Synchronous Reset ($\overline{SR}$), Count Enable Trickle ($\overline{CET}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel ($\overline{CEP}$), and the Up/Down(U/$\overline{D}$) input determine the mode of operation, as shown in the Function Table.

A Low signal on $\overline{MR}$ overrides all other inputs and asynchronously forces the flip-flop Q outputs Low. A Low signal on $\overline{SR}$ overrides counting and parallel loading and allows the Q output to go Low on the next rising edge of CP. A Low signal on $\overline{PE}$ overrides counting and allows information on the parallel data (D_n) inputs to be loaded into the flipflops on the next rising edge of CP. With $\overline{MR}$, $\overline{SR}$, and $\overline{PE}$ High, $\overline{CEP}$ and $\overline{CET}$ permit counting when both are Low. Conversely, a High signal on either $\overline{CEP}$ and $\overline{CET}$ inhibits counting. The 'F568 and 'F569 use edge triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, $\overline{CEP}$, $\overline{CET}$ or U/$\overline{D}$ inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed. Two types of outputs are provided as overflow/underflow indicators. The Terminal Count($\overline{TC}$) output is normally High and goes Low provided $\overline{CET}$ is Low, when the counter reaches zero in the down mode, or reaches maximum (9 for 'F568 and 15 for 'F569) in the up mode.

$\overline{TC}$ will then remain Low until a state change

FUNCTION TABLE

INPUTS							OPERATING MODE
$\overline{MR}$	$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	CP	
L	X	X	X	X	X	X	Asynchronous reset
h	I	X	X	X	X	↑	Synchronous reset
h	h	I	X	X	X	↑	Parallel load
h	h	h	I	I	h	↑	Count up (increment)
h	h	h	I	I	I	↑	Count down (decrement)
h	H	H	H	X	X	X	Hold (do nothing)
h	H	H	X	H	X	X	

H = High voltage level
h = High voltage level one setup prior to the Low-to-High clock transition
L = Low voltage level
I = Low voltage level one setup prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

occurs, whether by counting or presetting, or until U/$\overline{D}$ or $\overline{CET}$ is changed.

To implement synchronous multistage counters, the connections between the $\overline{TC}$ output and the $\overline{CEP}$ and $\overline{CET}$ inputs can provide either slow or fast carry propagation. Figure 1 shows the connections for a simple ripple carry, in which the clock period must be longer than the CP to $\overline{TC}$ delay of the first stage, plus the cumulative $\overline{CET}$ to $\overline{TC}$ delays of the intermediate stages, plus the $\overline{CET}$ to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry look ahead connections in Figure 2 are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the up mode, or min to max in the down mode, to start its final cycle. Since this takes 10 ('F568) or 16 ('F569) clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to $\overline{TC}$ delay of the first stage plus the $\overline{CEP}$ to CP setup time of the last stage. The $\overline{TC}$ output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, register or counters.

For such applications, the Clocked Carry ($\overline{CC}$) output is provided. The $\overline{CC}$ ouTput is normally High. When $\overline{CEP}$, $\overline{CET}$, and $\overline{TC}$ are Low, the $\overline{CC}$ output will go Low, when the clock next goes Low and will stay Low until the clock goes High again; as shown in the $\overline{CC}$ Function Table. When the Output Enable ($\overline{OE}$) is Low, the parallel data outputs Q_0 - Q_3 are active and follow the flip-flop Q outputs. A High signal on $\overline{OE}$ forces Q_0 - Q_3 to the High impedance state but does not prevent counting, loading or resetting.

LOGIC EQUATIONS:

Count Enable=$\overline{CEP}\cdot\overline{CET}\cdot\overline{PE}$

Up: $\overline{TC}= Q_0\cdot\overline{Q}_1\cdot\overline{Q}_2\cdot Q_3\cdot(Up)\cdot\overline{CET}$ for 'F568

Up: $\overline{TC}= Q_0\cdot Q_1\cdot Q_2\cdot Q_3\cdot(Up)\cdot\overline{CET}$ for 'F569

Down: $\overline{TC}= \overline{Q}_0\cdot\overline{Q}_1\cdot\overline{Q}_2\cdot\overline{Q}_3\cdot(Down)\cdot\overline{CET}$ for 'F568 and 'F569

APPLICATIONS

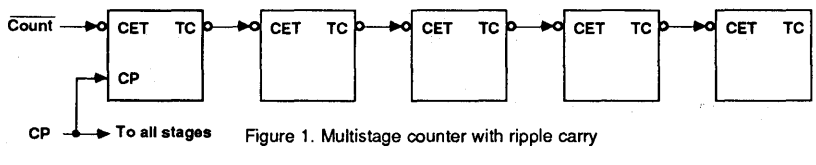


Figure 1. Multistage counter with ripple carry

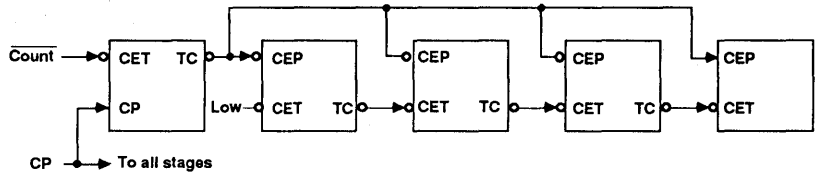


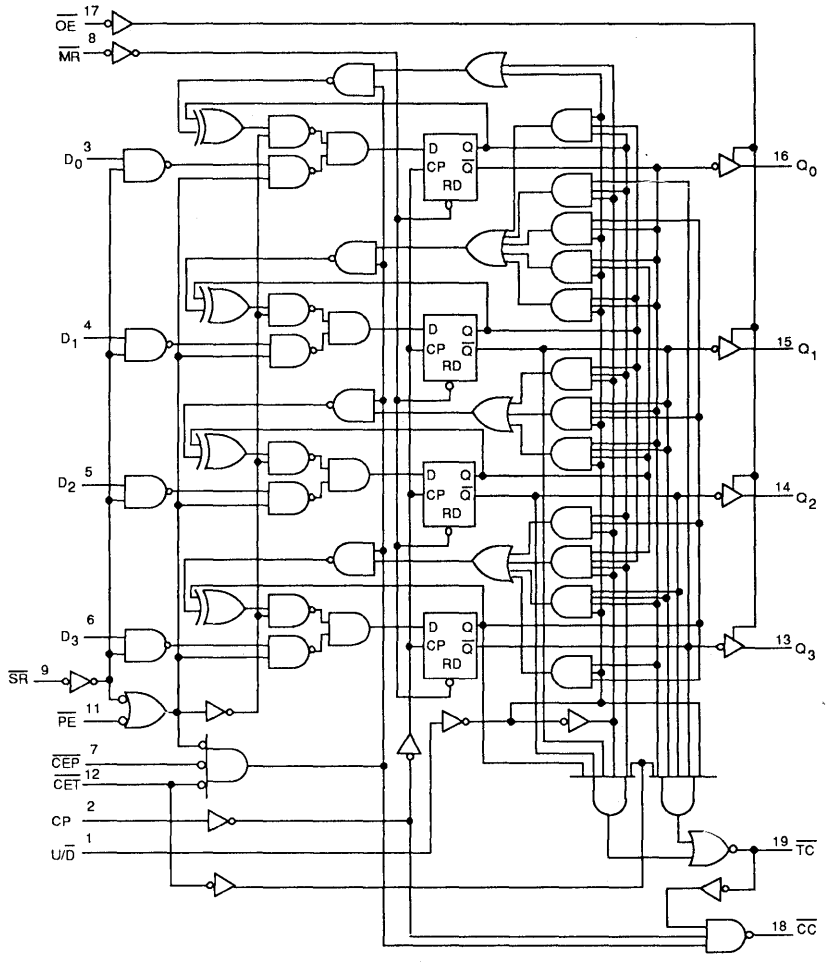
Figure 2. Multistage counter with look ahead carry

$\overline{CC}$ FUNCTION TABLE

INPUTS						OUTPUT
$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$\overline{TC}$*	CP	$\overline{CC}$
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	H	X	X	X	H
X	X	X	H	X	X	H
X	X	X	X	H	X	H
H	H	L	L	L	⊓	⊓

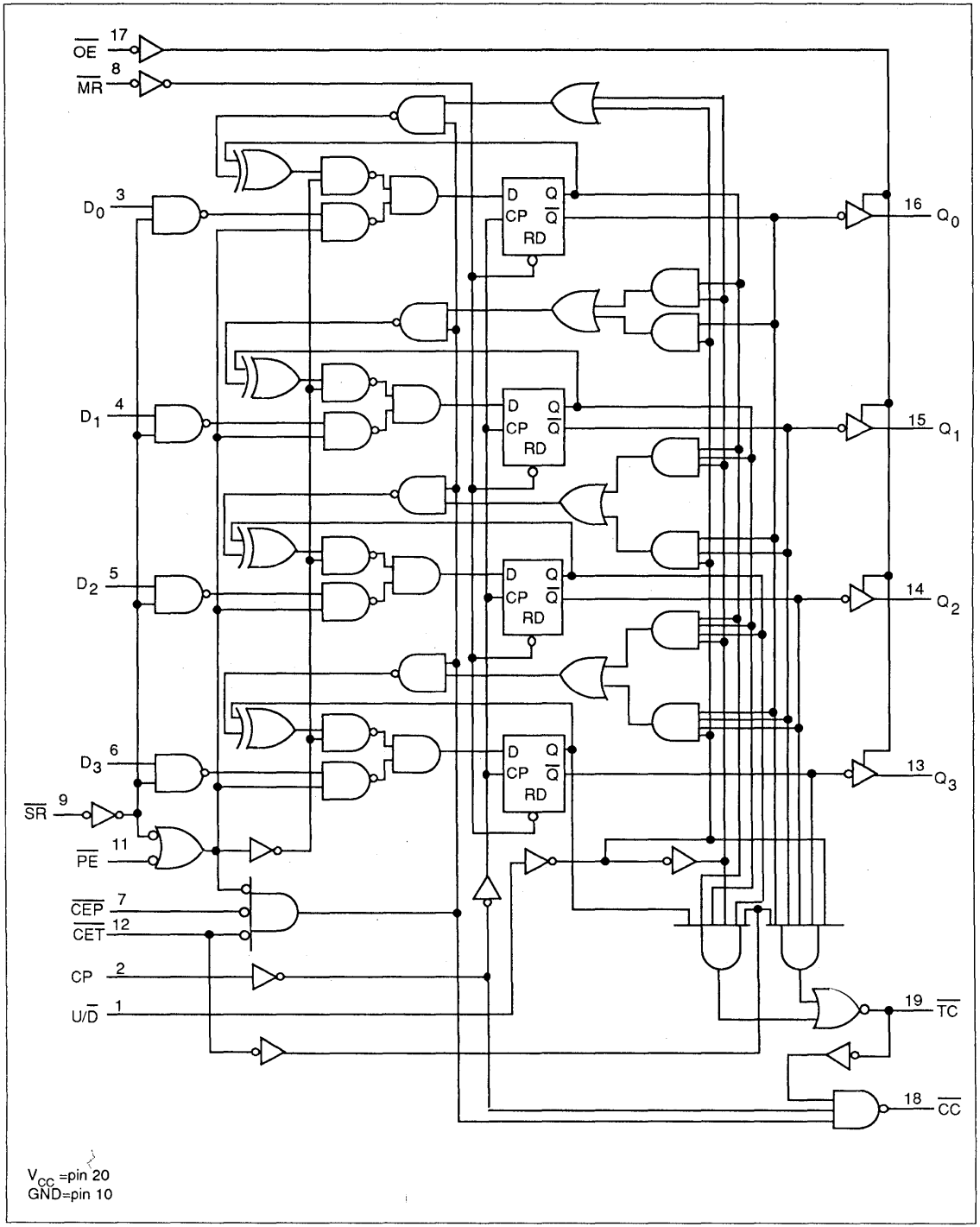
* = $\overline{TC}$ is generated internally
H = High voltage level
L = Low voltage level
X = Don't care
⊓ = Low pulse

LOGIC DIAGRAM for 'F568



V_{CC} = pin 20
GND= pin 10

LOGIC DIAGRAM for 'F569



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	$\overline{TC}$, $\overline{CC}$	40	mA
		Q_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	$\overline{TC}$, $\overline{CC}$			-1	mA
		Q_n			-3	mA
I_{OL}	Low-level output current	$\overline{TC}$, $\overline{CC}$			20	mA
		Q_n			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{CET}$, $\overline{PE}$					-1.2	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			38	60	mA
		I_{CCL}				43	62	mA
		I_{CCZ}				40	60	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

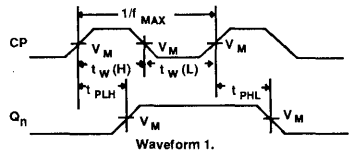
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Q_n	Waveorm 1	100	115		90		MHz
		$\overline{CC}$, $\overline{TC}$	Waveform 2	50	65		45		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$, High or Low)		Waveform 1	3.0 4.0	6.0 7.5	9.5 11.0	3.0 4.0	10.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$		Waveform 2	5.5 4.0	10.0 7.5	15.0 11.0	5.5 4.0	16.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$		Waveform 3	1.5 2.5	3.0 5.0	6.0 8.0	1.0 2.5	7.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	'F568	Waveform 4	2.5 5.0	5.0 10.0	9.0 15.0	2.0 5.0	10.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	'F569	Waveform 4	4.0 4.0	7.5 6.5	11.0 11.0	4.0 4.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{CC}$		Waveform 2	2.5 2.0	4.5 4.0	7.5 6.5	2.0 2.0	6.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CEP}$, $\overline{CET}$ to $\overline{CC}$		Waveform 2	2.0 3.5	4.0 5.5	7.0 9.0	1.5 3.0	7.5 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n		Waveform 5	6.0	8.0	11.0	5.5	12.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{CC}$		Waveform 4	4.5 5.0	9.0 11.0	12.0 16.0	4.0 5.0	13.5 17.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to $\overline{TC}$, $\overline{CC}$		Waveform 5	8.0	11.0	15.0	7.5	16.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SR}$ to $\overline{CC}$		Waveform 3	5.5 7.5	8.0 9.5	11.0 12.0	5.0 7.0	12.0 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PE}$ to $\overline{CC}$		Waveform 3	3.0 4.0	5.0 6.0	8.0 8.5	2.5 4.0	8.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level $\overline{OE}$ to Q_n		Waveform 10 Waveform 11	2.0 4.5	4.0 6.5	7.0 9.5	2.0 4.0	7.5 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level $\overline{OE}$ to Q_n		Waveform 10 Waveform 11	1.5 1.5	3.5 3.5	6.5 6.0	1.5 1.5	7.5 6.5	ns

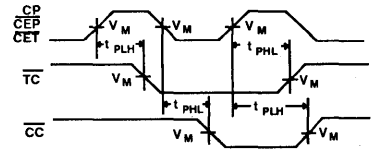
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP		Waveform 6	4.0 4.0			4.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP		Waveform 6	2.0 2.0			2.5 2.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP		Waveform 7	5.0 5.0			6.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP		Waveform 7	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP		Waveform 6	8.0 8.0			9.0 9.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP		Waveform 6	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/$\overline{D}$ to CP	'F568	Waveform 8	11.0 16.5			12.5 17.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/$\overline{D}$ to CP	'F569	Waveform 8	10.0 8.0			12.5 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low U/$\overline{D}$ to CP		Waveform 8	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{SR}$ to CP		Waveform 9	8.0 8.0			9.0 9.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{SR}$ to CP		Waveform 9	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1	7.0 5.0			8.0 6.0		ns
$t_w(H)$	$\overline{MR}$ Pulse width, Low		Waveform 5	4.5			5.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP		Waveform 5	6.0			7.0		ns

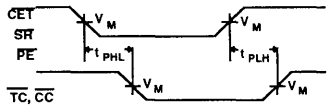
AC WAVEFORMS



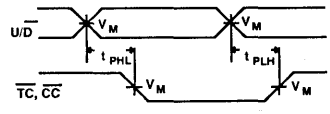
Waveform 1.
Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



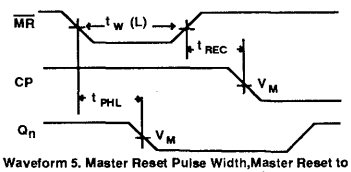
Waveform 2.
Propagation Delay, CP, CET, and CEP to CC and CP to TC



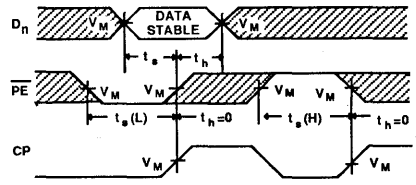
Waveform 3.
Propagation Delay, CET to TC and SR or PE to CC



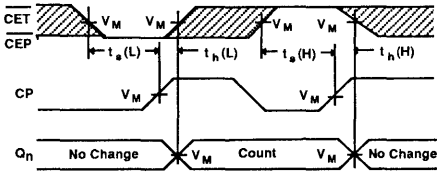
Waveform 4.
Propagation Delay, U/D to TC and CC



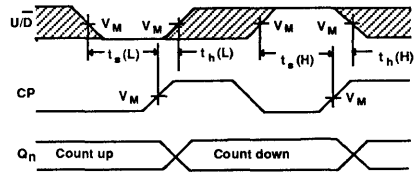
Waveform 5. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



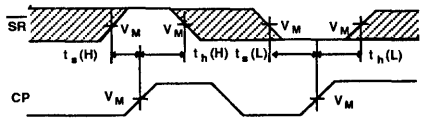
Waveform 6.
Data Parallel Data And Parallel Enable Setup And Hold Times



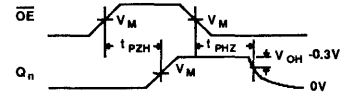
Waveform 7.
Count Enable Data Setup And Hold Times



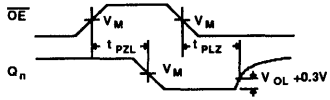
Waveform 8.
Up/Down Control Setup And Hold Times



Waveform 9. Synchronous Reset Setup And Hold Times



Waveform 10. 3-State Output Enable Time To High Level And Output Disable Time From High Level

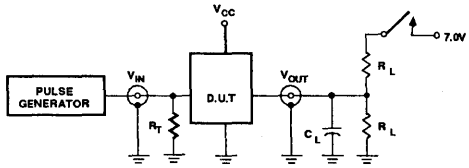


Waveform 11. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

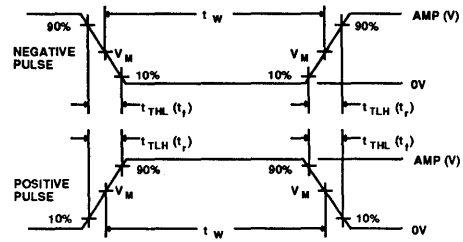
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F573, 74F574
Latch/Flip-Flop

FAST Products

74F573 Octal Transparent Latch (3-State)
74F574 Octal D Flip-Flop (3-State)

Product Specification

FEATURES

- **74F573 is broadside pinout version of 74F373**
- **74F574 is broadside pinout version of 74F374**
- **Inputs and Outputs on opposite side of package allow easy interface to Microprocessors**
- **Useful as an Input or Output port for Microprocessors**
- **3-State Outputs for Bus interfacing**
- **Common Output Enable**
- **74F563 and 74F564 are inverting version of 74F573 and 74F574 respectively**
- **3-State Outputs glitch free during power-up and power-down**
- **These are High-Speed replacements for N8TS805 and N8TS806**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F573	5.0ns	35mA
74F574	4.5ns	50mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F573N, N74F574N
20-Pin Plastic SOL	N74F573D, N74F574D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

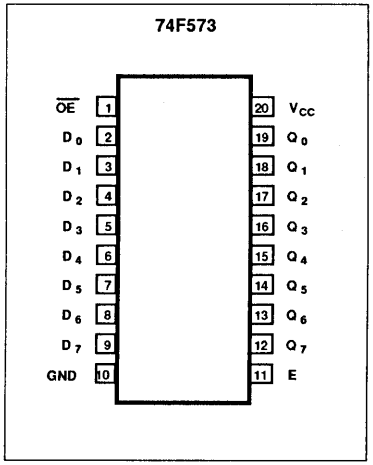
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20µA/0.6mA
E ('F573)	Latch enable input (active falling edge)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20µA/0.6mA
CP ('F574)	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
Q_0 - Q_7	3-State outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

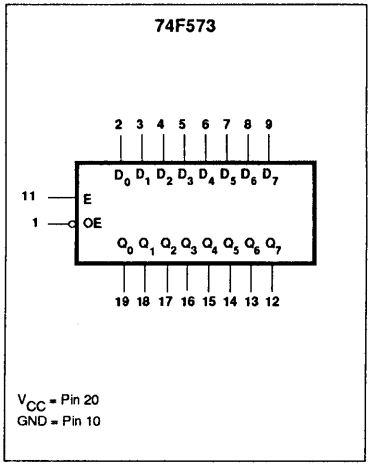
DESCRIPTION

The 74F573 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are con-

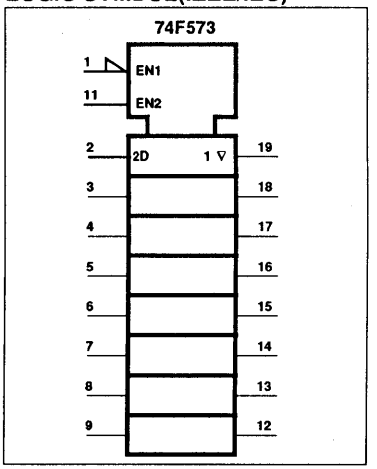
PIN CONFIGURATION



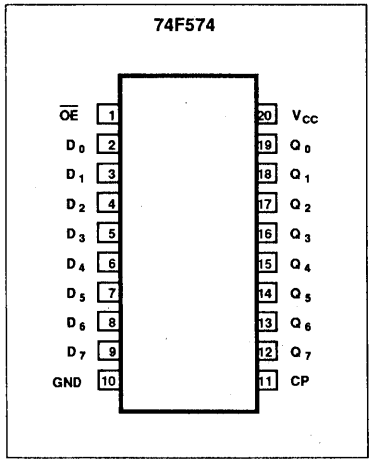
LOGIC SYMBOL



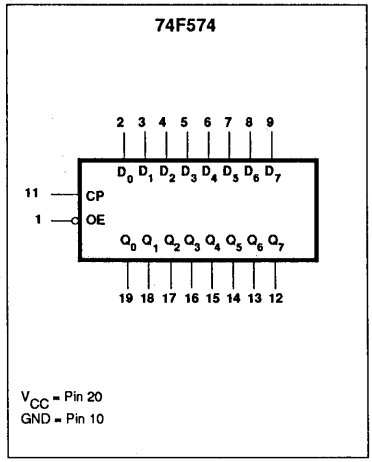
LOGIC SYMBOL(IEEE/IEC)



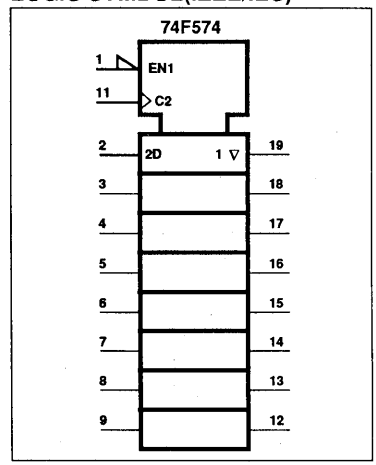
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



trolled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.
The 74F573 is functionally identical to the 74F373 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the data that is present one set-up time before the High-to-Low enable transition.

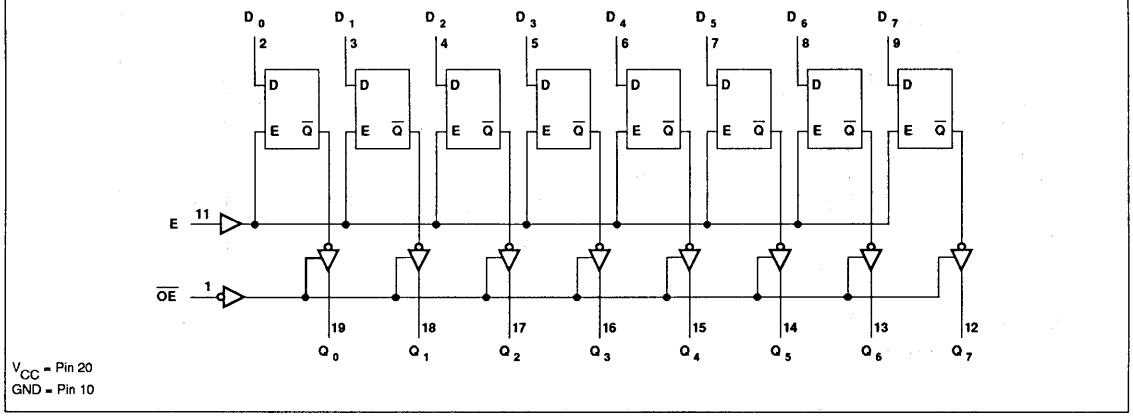
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74F574 is functionally identical to the 74F374 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

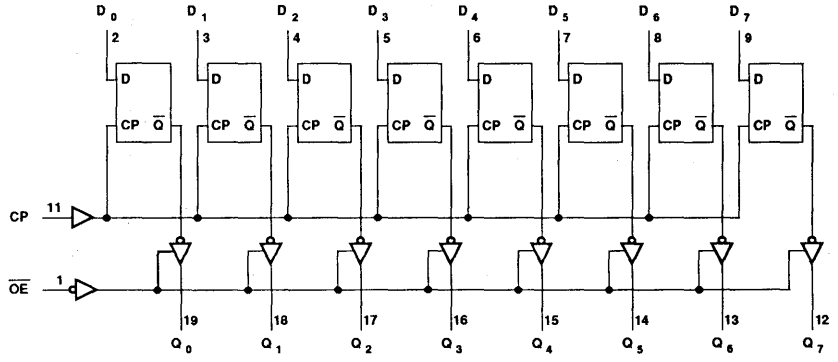
It is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates. The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 74F573



LOGIC DIAGRAM, 74F574



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE, 74F573

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	D_n	REGISTER	Q_0 - Q_7	
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L‾	X	NC	Z	Disable outputs
H	H	D_n	D_n	Z	

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

FUNCTION TABLE, 74F574

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	D_n	REGISTER	Q_0 - Q_7	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	↕	X	NC	NC	Hold
H	↑	D_n	D_n	Z	Disable outputs
H	X	X	X	Z	

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
				V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
				V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]			V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	74F573	V_{CC} = MAX			30	40	mA
		I_{CCL}					35	50	mA
		I_{CCZ}					40	60	mA
		I_{CCH}	74F574	V_{CC} = MAX			45	65	mA
		I_{CCL}					50	70	mA
		I_{CCZ}					55	90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

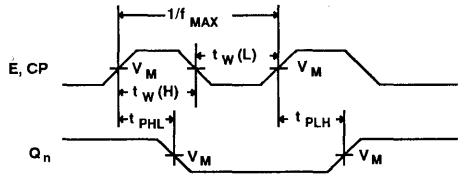
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F573	Waveform 2	3.0 1.0	5.5 3.5	8.0 6.0	2.5 1.0	9.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n		Waveform 1	4.5 3.0	8.5 5.0	11.5 7.0	4.0 2.5	12.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 5 Waveform 6	2.5 2.5	5.5 5.5	9.5 8.0	2.0 2.0	10.5 8.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 5 Waveform 6	1.0 1.0	3.0 2.5	6.0 5.5	1.0 1.0	6.5 5.5	ns ns
f_{MAX}	Maximum Clock frequency	74F574	Waveform 1	110	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	4.0 4.0	5.5 6.0	8.5 8.5	3.0 3.0	9.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 5 Waveform 6	2.5 3.0	4.5 6.0	8.0 8.5	2.0 3.0	8.0 9.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 5 Waveform 6	1.0 1.0	3.0 2.5	6.0 5.5	1.0 1.0	7.0 6.0	ns ns

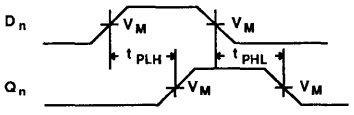
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Set-up time D_n to E	74F573	Waveform 4	0.0 1.5			0.0 2.0		ns
t_h(H) t_h(L)	Hold time D_n to E		Waveform 4	2.5 4.0			2.5 4.0		ns
t_w(H)	E Pulse width, High		Waveform 1	3.0			3.5		ns
t_s(H) t_s(L)	Set-up time D_n to CP	74F574	Waveform 3	2,0 2,0			2.0 2.0		ns
t_h(H) t_h(L)	Hold time D_n to CP		Waveform 3	1.5 1.5			1.5 1.5		ns
t_w(H) t_w(L)	CP Pulse width, High or Low		Waveform 1	3.0 4.5			3.0 4.5		ns

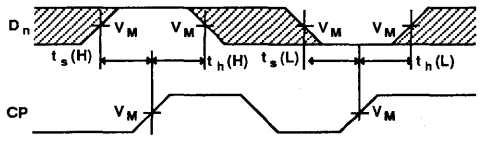
AC WAVEFORMS



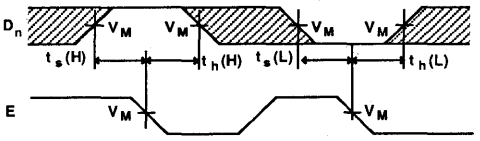
Waveform 1. Propagation Delay, Clock And Enable Inputs To Output, Enable, and Clock Pulse Widths, and Maximum Clock Frequency



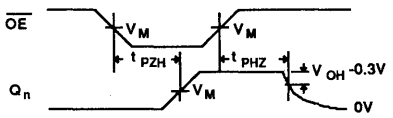
Waveform 2. Propagation Delay For Data To Outputs



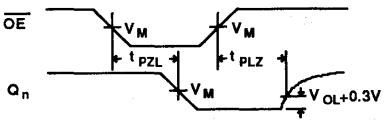
Waveform 3. Data Setup And Hold Times



Waveform 4. Data Setup And Hold Times



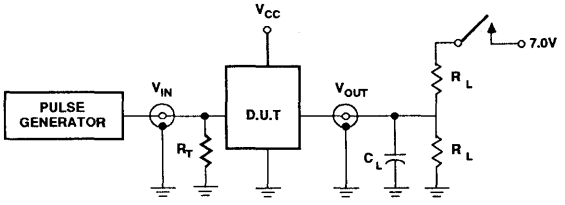
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



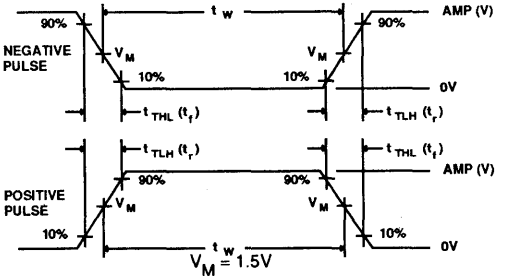
Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F579 Counter

FAST Products

8-Bit Bidirectional Binary Counter (3-state)
Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F579	115MHz	100mA

FEATURES

- Fully synchronous operation
- Multiplexed 3-state I/O ports for bus oriented applications
- Built in cascading carry capability
- U/$\overline{D}$ pin to control direction of counting
- Separate pins for Master Reset and Synchronous operation
- Center power pins to reduce effects of package inductance
- Count frequency 115MHz typ
- Supply current 100mA typ
- See 'F269 for 24 pin separate I/O port version
- See 'F779 for 16 pin version

DESCRIPTION

The 74F579 is a fully synchronous 8-stage Up/Down Counter with multiplexed 3-state I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, except for the case of asynchronous reset, are initiated by the rising edge of the clock. $\overline{TC}$ output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

ORDERING INFORMATION

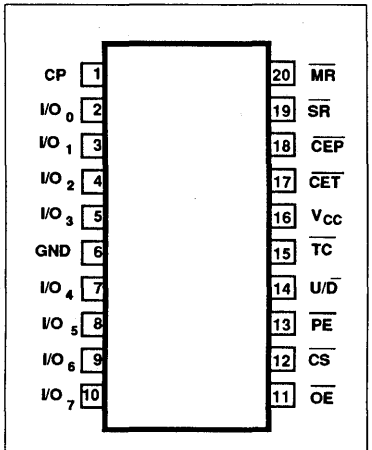
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic Dip	N74F579N
20-Pin Plastic SOL	N74F579D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

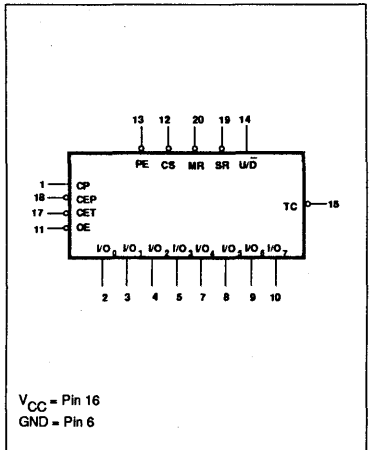
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/O_n	Data inputs	3.5/1.0	70µA/0.6mA
	Data outputs	150/40	3.0mA/24mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/1.0	20µA/0.6mA
U/$\overline{D}$	Up/Down count control input	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{SR}$	Synchronous Reset input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CEP}$	Count Enable Parallel input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CS}$	Chip Select input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20 A/0.6mA
$\overline{TC}$	Terminal count output (active Low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

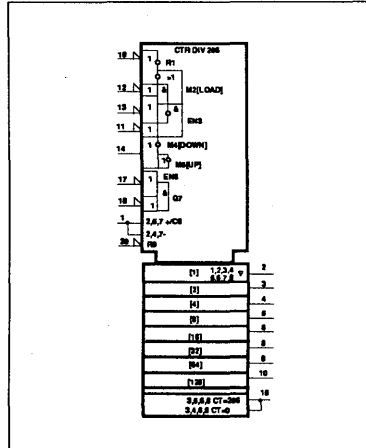
PIN CONFIGURATION



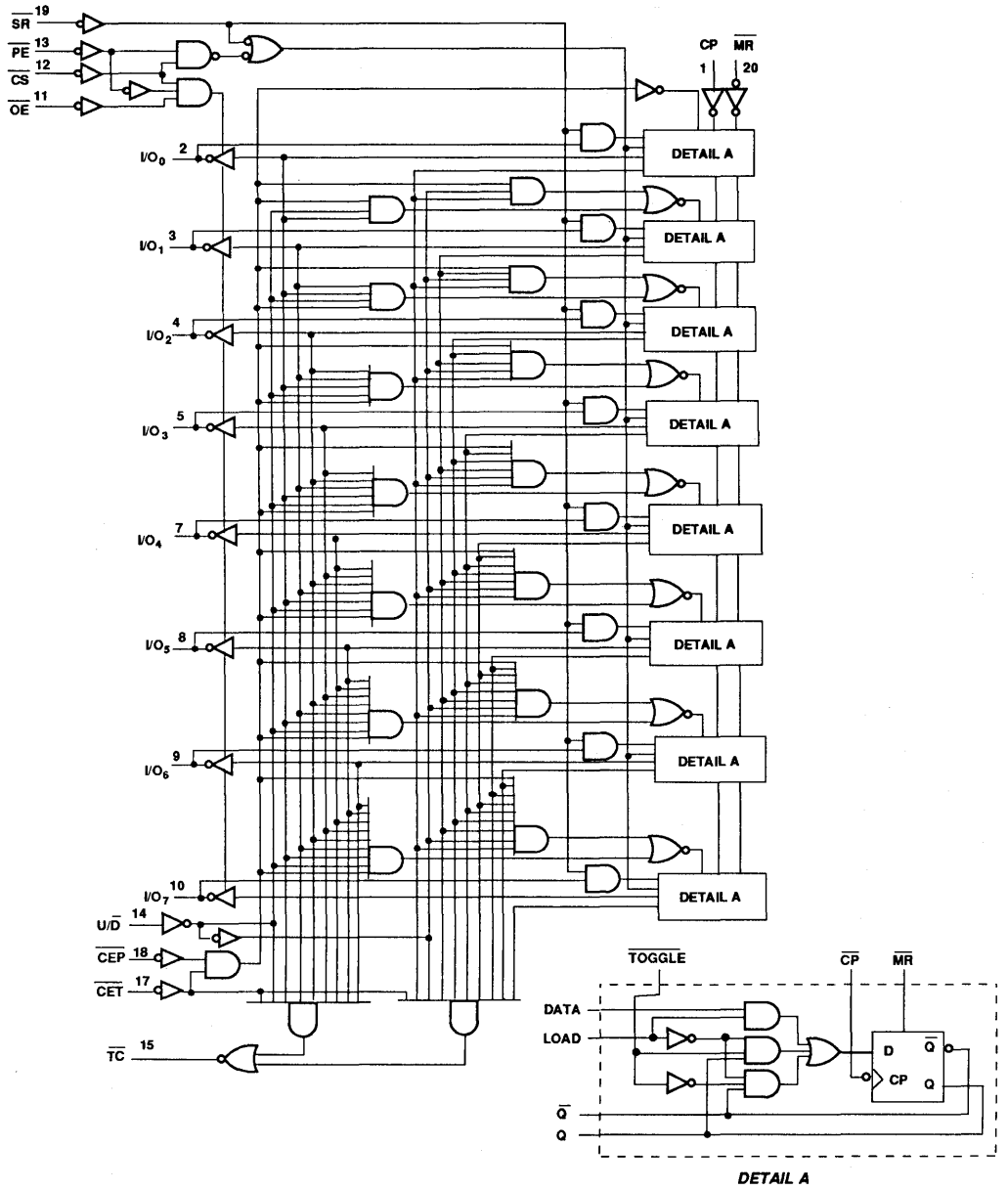
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} =pin16
GND=pin 6

FUNCTION TABLE

INPUTS									OPERATING MODE
$\overline{MR}$	$\overline{SR}$	$\overline{CS}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	$\overline{OE}$	CP	
X	X	H	X	X	X	X	X	X	I/O_0 to I/O_7 in high impedance ($\overline{PE}$ disabled)
X	X	L	H	X	X	X	H	X	I/O_0 to I/O_7 in high impedance
X	X	L	H	X	X	X	L	X	Flip-flop output appears on I/O_n lines
L	X	X	X	X	X	X	X	X	Asynchronous reset for all flip-flops
H	L	X	X	X	X	X	X	↑	Synchronous reset for all flip-flops
H	H	L	L	X	X	X	X	↑	Parallel load all flip-flops
H	H	(not LL)		H	X	X	X	↑	Hold
H	H	(not LL)		X	H	X	X	↑	Hold ($\overline{TC}$ held High)
H	H	(not LL)		L	L	H	X	↑	Count up
H	H	(not LL)		L	L	L	X	↑	Count down

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
(not LL) = $\overline{CS}$ and $\overline{PE}$ should never be Low voltage level at the same time..

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	$\overline{TC}$	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	$\overline{TC}$			-1	mA
		I/O_n			-3	mA
I_{OL}	Low-level output current	$\overline{TC}$			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	$\overline{TC}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN (V_{IL}=0.0V, V_{IH}=4.5V for $\overline{MR}$, CP inputs)	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OH}=-3mA	±10%V_{CC}	2.4	3.3		V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	I/O_n	V_{CC} = MAX, V_I = 5.5V					1	mA
		others	V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	except I/O_n	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
$I_{IH}+I_{OZH}$	Off-state current High-level voltage applied	I/O_n	V_{CC} = MAX, V_O= 2.7V					70	µA
$I_{IL}+I_{OZL}$	Off-state current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-800	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				95	135	mA
		I_{CCL}					105	145	mA
		I_{CCZ}					105	150	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

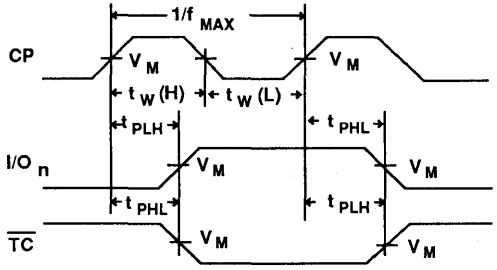
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	5.0 5.0	7.5 7.5	10.5 10.5	5.0 5.0	11.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	5.5 5.5	7.5 7.5	10.0 10.0	5.0 5.0	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	Waveform 4	3.5 4.5	5.5 6.5	8.0 8.0	3.5 4.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 3	3.5 3.5	5.5 6.0	7.0 8.0	3.5 3.5	8.5 8.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/O_n	Waveform 2	5.0	7.0	9.0	5.0	10.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{CS}$, $\overline{PE}$ to I/O_n	Waveform 6 Waveform 7	5.0 6.0	8.0 8.5	10.5 10.5	4.5 5.5	11.5 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{CS}$, $\overline{PE}$ to I/O_n	Waveform 6 Waveform 7	3.0 5.0	5.0 8.0	7.5 9.5	3.0 4.5	9.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to I/O_n	Waveform 6 Waveform 7	4.0 5.0	6.0 6.5	8.5 9.0	4.0 5.0	9.5 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to I/O_n	Waveform 6 Waveform 7	1.0 2.5	2.5 4.5	4.0 7.0	1.0 2.5	5.5 8.0	ns

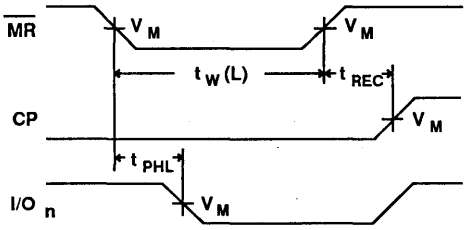
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 5	3.0 3.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/$\overline{D}$ to CP	Waveform 5	8.0 8.0			9.0 9.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low U/$\overline{D}$ to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	Waveform 5	9.5 9.5			10.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	5.0 9.0			5.5 10.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	0 0			0 0		ns
t_w(H $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.5 4.5			4.5 4.5		ns
$t_w(L)$	CP Pulse width, Low	Waveform 2	3.0			3.0		ns
t_{REC}	Recovery time, $\overline{MR}$ to CP	Waveform 2	4.0			4.5		ns

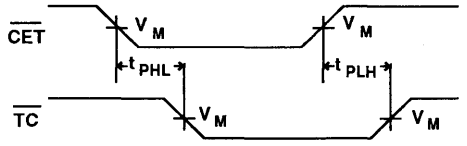
AC WAVEFORMS



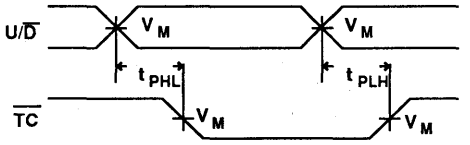
Waveform 1.
Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



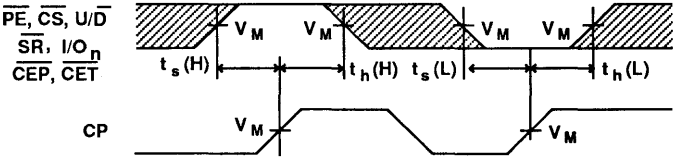
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



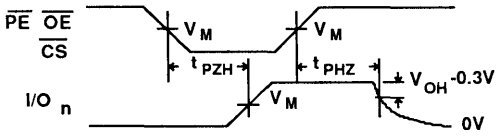
Waveform 3.
Propagation Delay, CET input to Terminal Count Output



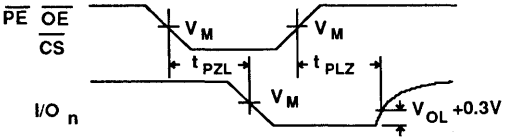
Waveform 4.
Propagation Delay, U/D input to Terminal Count Output



Waveform 5. Setup And Hold Times



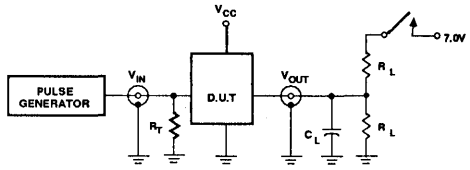
Waveform 6. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 7. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

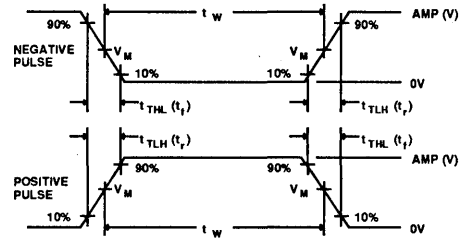
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F582
4-Bit BCD Arithmetic Logic Unit

FEATURES

- Performs four BCD functions
- P and G outputs for high speed expansion
- Add/Subtract delay 28ns max
  Look ahead delay 22.5ns max
- Supply current 85mA max
- 24 pin 300 mil Slim Dip package

DESCRIPTION

The 74F582 Binary Coded Decimal (BCD) Arithmetic Logic Unit (ALU) is a 24 pin expandable unit that performs addition, subtraction, comparison of two numbers and binary to BCD conversion.

The 'F582 input and output logic includes a Carry/$\overline{\text{Borrow}}$ which is generated internally in the look-ahead mode, allowing BCD to computed directly. For more than one BCD decade, the Carry/$\overline{\text{Borrow}}$ term may ripple between 'F582s.

When $\overline{A}$/S is Low, BCD addition is performed (A+B+C/$\overline{B}$=F). If an input is greater than 9 binary to BCD conversion results at the output.

When $\overline{A}$/S is High, subtraction is performed. If the C/$\overline{B}$ is Low, then the subtraction is accomplished by internally computing the nine's complement addition of the two BCD numbers(A-B-1=F). When C/$\overline{B}$ is High, the difference of the two numbers is figured as A-F=F. If A is greater than or equal to B, the BCD difference appears at the output F in its true form. If A is less than B and C/$\overline{B}$ is Low, the 9s complement of the true form appears at the output F. As long as A is less than B, an active Low borrow is also generated. The 'F582 also performs binary to BCD conversion. For inputs from 10 to 15, binary to BCD conversion occurs by grounding one set of inputs, A_n or B_n, and applying the binary number to the other set of inputs. This will generate a carry term to the next decade.

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F582	12.0 ns	55mA

ORDERING INFORMATION

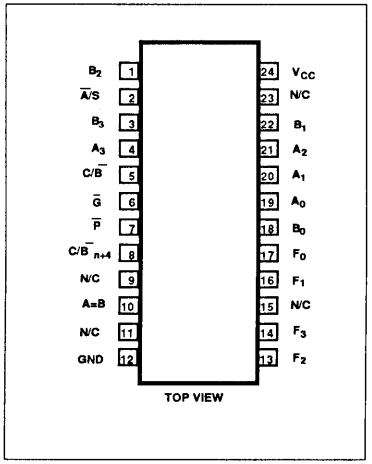
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300 mil)	N74F582N
24-Pin Plastic SOL	N74F582D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

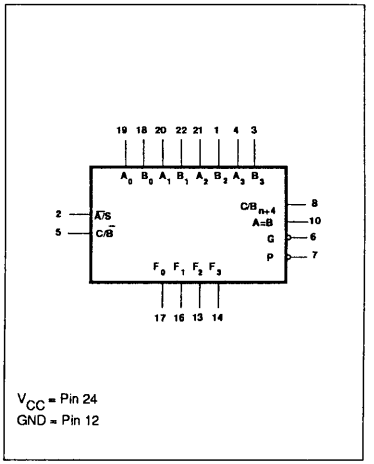
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_3	A operand inputs	1.0/2.0	20µA/1.2mA
B_0	B operand input	1.0/1.0	20µA/0.6mA
B_1	B operand input	1.0/4.0	20µA/2.4mA
B_2	B operand input	1.0/3.0	20µA/1.8mA
B_3	B operand input	1.0/2.0	20µA/1.2mA
$\overline{A}$/S	Add/Subtract input	1.0/3.0	20µA/1.8mA
C/$\overline{B}$	Carry/Borrow input	1.0/1.0	20µA/0.6mA
C/$\overline{B}_{n+4}$	Carry/Borrow output	50/33	1.0mA/20mA
$\overline{P}$	Carry Propagate output	50/33	1.0mA/20mA
$\overline{G}$	Carry Generator output	50/33	1.0mA/20mA
A=B	Comparator output	OC/33	OC/20mA
F_0-F_3	Outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC=Open Collector

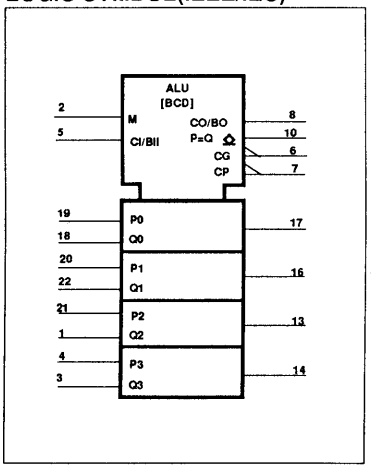
PIN CONFIGURATION



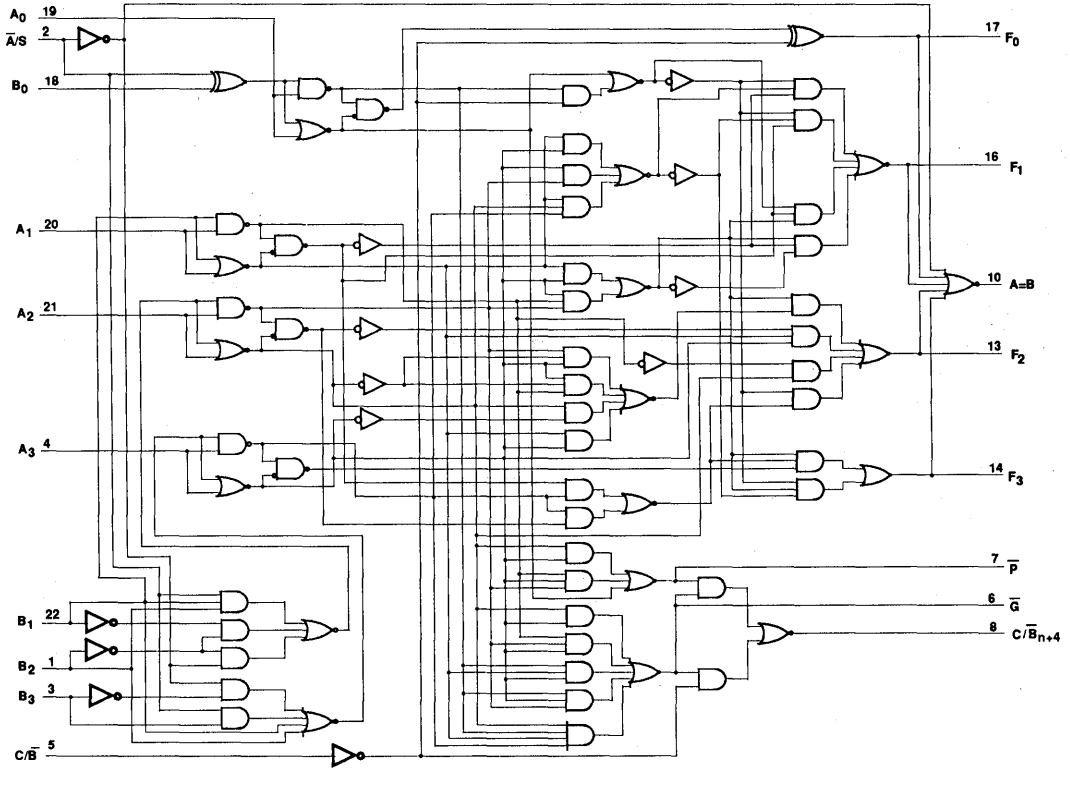
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12
NC = Pin 9, 15, 23

FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS		
	$\overline{A}$/S	A_n	B_n	C/$\overline{B}$	F_n	C/$\overline{B}_{n+4}$	A=B
Add	L	BCD Augend	BCD Addend	H=Carry L=No carry	IF C/$\overline{B}$=H F=A+B+1 IF C/$\overline{B}$=L F=A+B	F≤9 C/$\overline{B}_{n+4}$=L F>9 C/$\overline{B}_{n+4}$=H	X
Subtract	H	BCD Minuend	BCD Subtrahend	L=Borrow H=No Borrow	IF C/$\overline{B}$=L F=A-B-1 IF C/$\overline{B}$=H F=A-B	A>B C/$\overline{B}_{n+4}$=H A≤B C/$\overline{B}_{n+4}$=L A<B C/$\overline{B}_{n+4}$=L A≥B C/$\overline{B}_{n+4}$=H	X
Compare	H	BCD Word A	BCD Word B	H	A-B	A<B C/$\overline{B}_{n+4}$=L A>B C/$\overline{B}_{n+4}$=H	IF A=B Compare=H IF A≠B Compare=L
Binary to BCD Conversion	L	0≤A≤15	B=0	X	BCD	A≤9 C/$\overline{B}_{n+4}$=L A>9 C/$\overline{B}_{n+4}$=H	X

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_K	Input clamp current				-18	mA
V_{OH}	High-level output voltage	A=B only			4.5	V
I_{OH}	High-level output current	Except A=B			-1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current	A=B only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OH}	High-level output voltage	Except A=B	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7		3.4	V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.30	0.50	mA
					±5%V_{CC}		0.30	0.50	mA
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximuminput voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	B_0, C/$\overline{B}$	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		A_n, B_3						-1.2	mA
		B_2, $\overline{A}$/S						-1.8	mA
		B_1						-2.4	mA
I_{OS}	Short circuit output current[3]	Except A=B	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX				55	85	mA

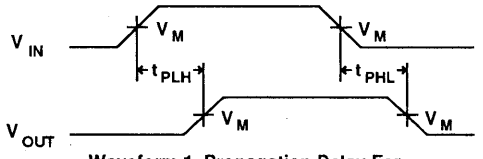
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

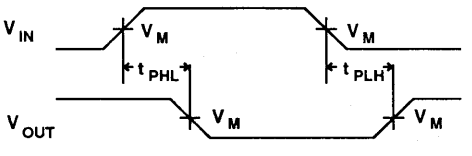
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to F_n	Waveform 1,2	5.0 4.0	17.5 14.0	23.0 19.0	5.0 4.0	25.0 20.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to $C/\overline{B}_{n+4}$	Waveform 1,2	7.0 4.0	16.0 10.0	20.0 14.0	6.0 4.0	22.5 16.0	ns
t_{PLH} t_{PHL}	Propagation delay $C/\overline{B}_n$ to $C/\overline{B}_{n+4}$	Waveform 1,2	3.5 2.5	5.5 5.0	8.0 7.0	3.0 2.5	8.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to A=B	Waveform 1,2	8.0 6.0	18.0 14.0	24.0 18.0	8.0 5.5	27.0 21.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to $\overline{G}$ or $\overline{P}$	Waveform 1,2	4.0 4.0	11.0 11.0	14.0 14.0	4.0 4.0	16.5 16.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}/S$ to F_n	Waveform 1,2	8.0 8.0	15.0 14.0	20.0 18.0	7.0 7.0	25.0 19.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}/S$ to A=B	Waveform 1,2	10.0 4.0	18.0 6.0	24.0 9.0	10.0 3.5	28.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}/S$ to $\overline{G}$ or $\overline{P}$	Waveform 1,2	6.0 6.0	11.0 11.0	14.5 14.5	6.0 6.0	16.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}/S$ to $C/\overline{B}_{n+4}$	Waveform 1,2	8.0 7.0	14.0 12.0	19.0 15.0	8.0 7.0	20.5 16.5	ns
t_{PLH} t_{PHL}	Propagation delay $C/\overline{B}_n$ to F_n	Waveform 1,2	4.0 3.0	13.0 9.0	17.5 13.0	4.0 3.0	18.5 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $C/\overline{B}_n$ to A=B	Waveform 1,2	8.0 4.0	15.0 8.0	20.0 12.0	8.0 3.5	22.5 13.0	ns

AC WAVEFORMS



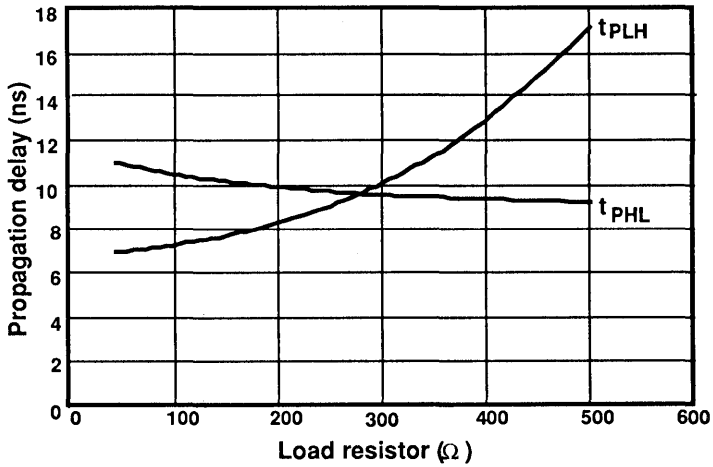
Waveform 1. Propagation Delay For Non-Inverting Output



Waveform 2. Propagation Delay For Inverting Output

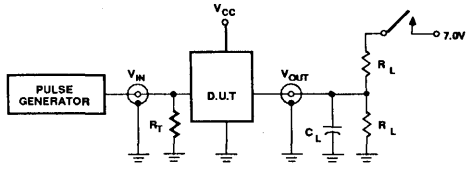
NOTE: For all waveforms, V_M = 1.5V

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



NOTE:
When using open-collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the pull-up resistor value from 500 Ω to 100Ω will improve the t_{PLH} up to 50% with only slight increase in the t_{PHL}. However, if the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers do not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open Collector Output and Totem-Pole Outputs

SWITCH POSITION

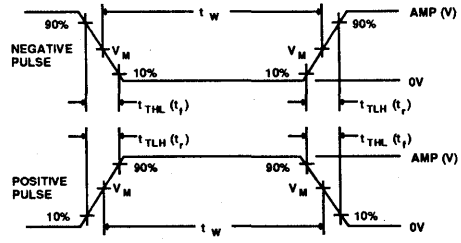
TEST	SWITCH
Open Collector	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F583
4-Bit BCD Adder

FAST Products

Product Specification

FEATURES

- **Adds two decimal numbers**
- **Full internal look-ahead**
- **Fast ripple carry for economical expansion**
- **Sum output delay 19.5ns max**
- **Ripple carry delay 8.5ns max**
- **Input to ripple delay 13.0ns max**
- **Supply current 60mA max**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F583	9.0ns	45mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F583N
16-Pin Plastic SO	N74F583D

DESCRIPTION

The 74F583 4-bit coded (BCD) full adder performs the addition of two decimal numbers (A_0 - A_3, B_0 - B_3). The look ahead generates BCD carry terms internally, allowing the 'F583 to then do BCD addition correctly. For BCD numbers 0 through 9 at A and B inputs, the BCD sum forms at the output.

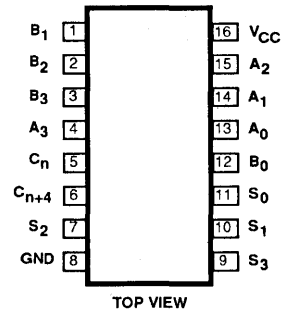
In addition of two BCD numbers totalling a number greater than 9, a valid BCD number and carry will result. For input values larger than 9, the number is converted from binary to BCD. Binary to BCD conversion occurs by grounding one set of inputs, A_n or B_n and applying a 4-bit binary number to the other set of inputs. If the input is between 0 and 9, a BCD number occurs at the output. If the binary input falls between 10 and 15, a carry term is generated. Both the carry term and the sum are the BCD equivalent of the binary input. Converting binary numbers greater than 16 may be achieved by cascading 'F583s.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

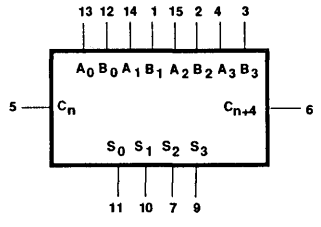
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	A operand inputs	1.0/2.0	20µA/1.2mA
B_0 - B_3	B operand inputs	1.0/2.0	20µA/1.2mA
C_n	Carry input	1.0/1.0	20µA/0.6mA
C_{n+4}	Carry output	50/33	1.0mA/20mA
S_0 - S_3	Sum outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

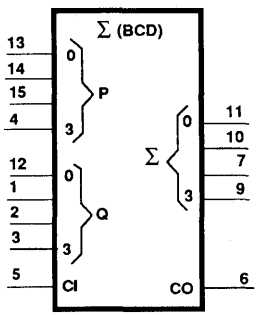
PIN CONFIGURATION



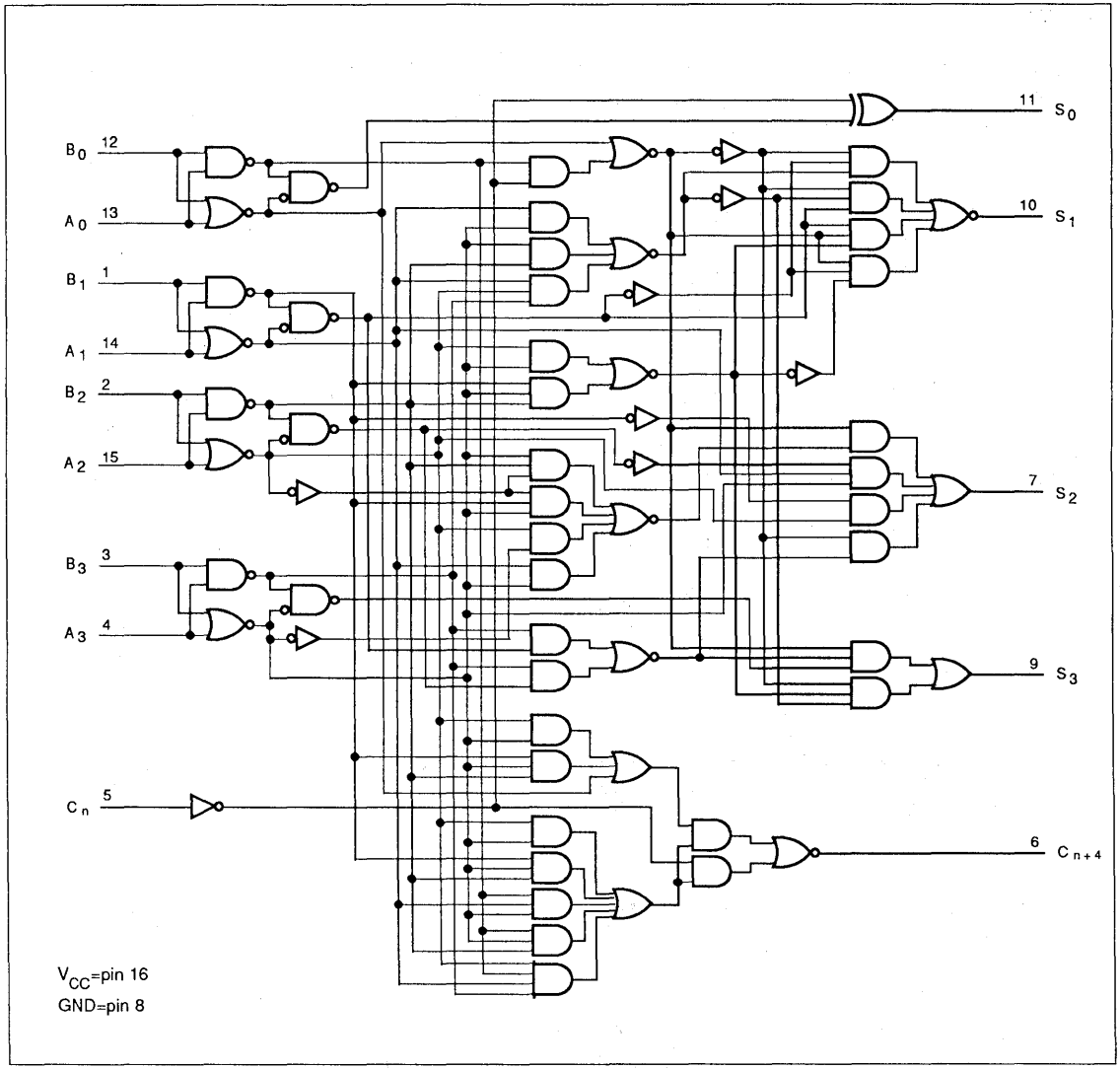
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	C_n only	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		A_n & B_n					-1.2	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			45	60	mA

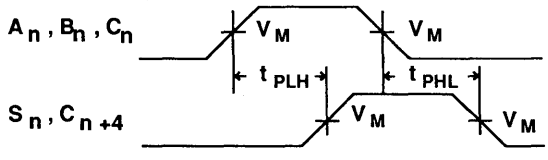
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

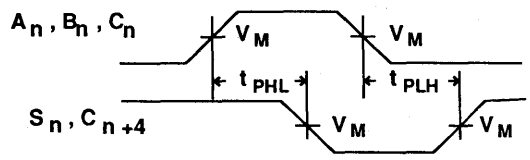
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to S_n	Waveform 1	5.0 5.0	13.0 10.5	17.0 14.0	5.0 5.0	18.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to S_n (INV)	Waveform 2	6.0 4.0	11.0 8.0	18.0 12.0	5.0 4.0	19.5 12.5	ns
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	Waveform 1,2	3.5 2.5	5.0 4.0	8.0 7.0	3.0 2.0	8.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to C_{n+4}	Waveform 1,2	5.0 5.0	8.0 7.5	11.5 10.5	4.5 4.5	13.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay C_n to S_n	Waveform 1	4.0 3.5	12.0 8.0	15.5 12.5	3.5 3.0	17.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay C_n to S_n (INV)	Waveform 2	6.0 3.5	9.5 8.0	13.0 11.5	5.0 3.0	14.5 12.0	ns

AC WAVEFORMS



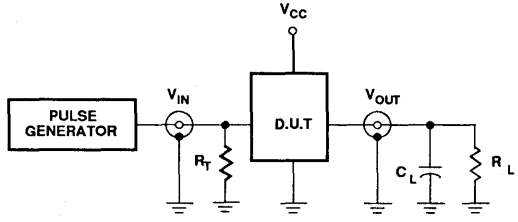
Waveform 1. Propagation Delay For Non-Inverting Outputs



Waveform 2. Propagation Delay For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



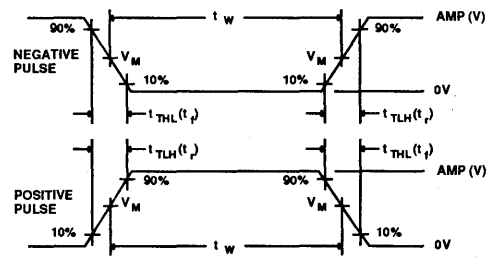
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F588
Transceiver

FAST Products

FEATURES
- **High-impedance NPN base inputs for reduced loading (70μA in High and Low states)**
- **Non-inverting buffers**
- **Bidirectional data path**
- **B outputs sink 64mA and source 15mA**

DESCRIPTION
The 74F588 contains eight non-inverting bidirectional buffers with 3-state outputs and is intended for bus-oriented applications. The B port have termination resistors as specified in the IEEE-488 specifications. Current sinking capability is 24mA at the A ports and 64 mA at the B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active High) enables data from A ports to B ports and Receive (active Low) enables data from B ports to A ports. The Output Enable input, when High, disables both A and B ports by placing them in a high-impedance condition.

Octal Bidirectional Transceiver With IEEE-488 Termination Resistors (3 state Inputs and Outputs)
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F588	4.0ns	96mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F588N
20-Pin Plastic SOL[1]	N74F588D

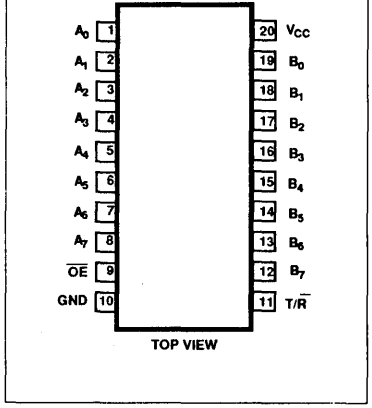
NOTE 1:
Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

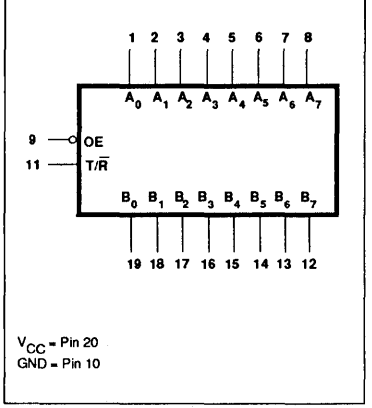
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7	Port A data inputs	3.5/0.117	70μA/70μA
B_0- B_7	Port B data inputs	T^2/5.33	T^2/3.2mA
$\overline{OE}$	Output Enable input (active Low)	2.0/0.067	40μA/40μA
$T/\overline{R}$	Transmit/Receive input	2.0/0.067	40μA/40μA
A_0- A_7	Port A outputs	150/40	3.0mA/24mA
B_0- B_7	Port B outputs	750/106.7	15mA/64mA

NOTE:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
2. T= Resistance Termination per IEEE-488 Standard

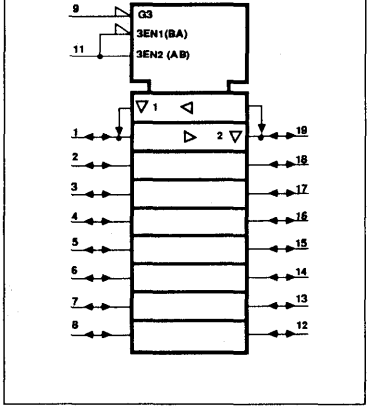
PIN CONFIGURATION



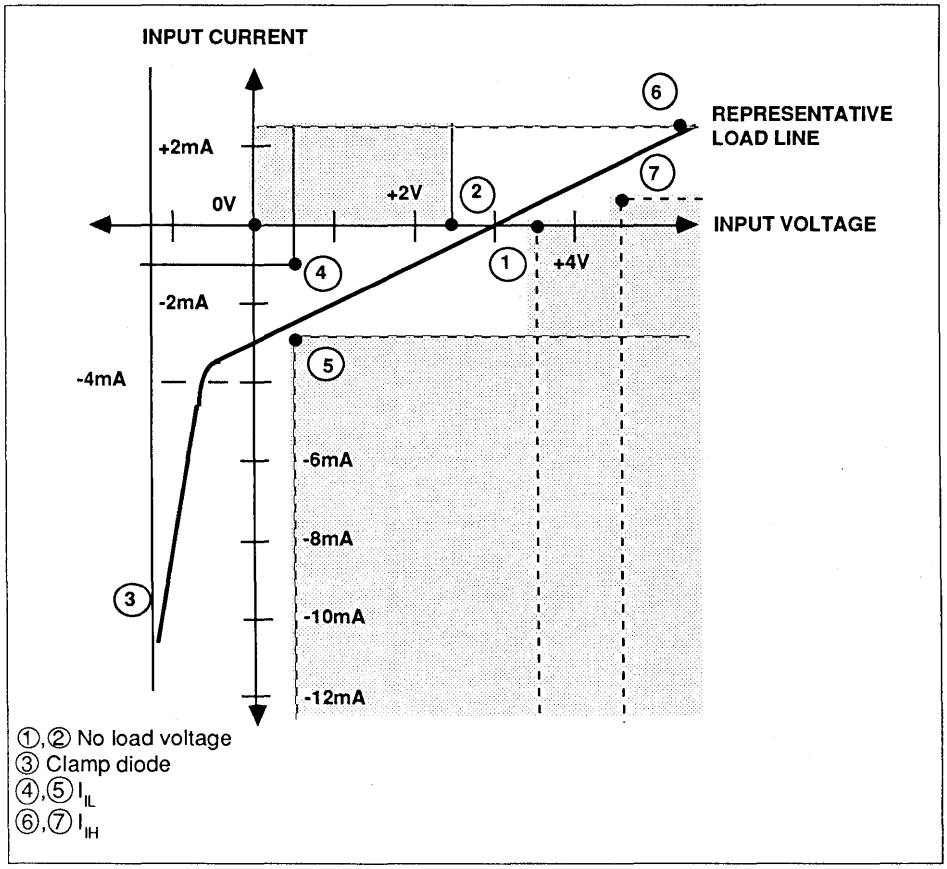
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



B port Input Characteristics with T/$\overline{R}$ Low

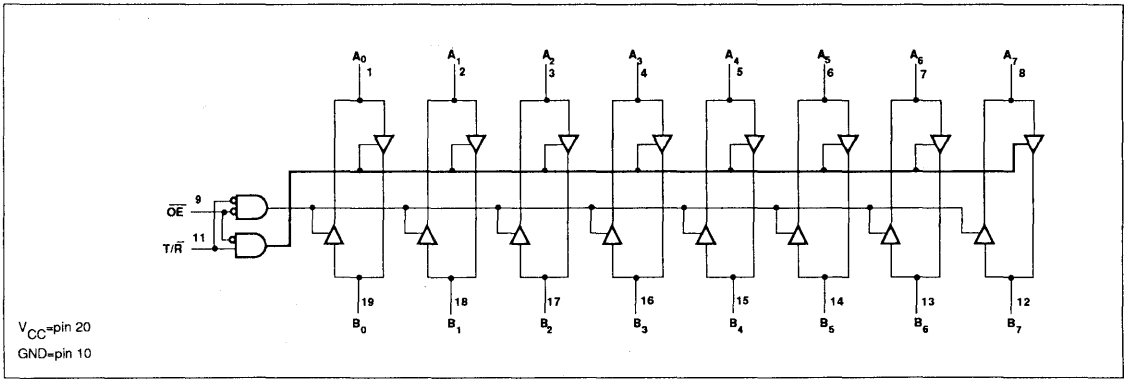


FUNCTION TABLE

INTPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B data to Bus A
L	H	Bus A data to Bus B
H	X	Z

H=High voltage level
L=Low voltage level
X=Don't care
Z=High impedance "off " state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Currebt applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0-B_7			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	A_0-A_7, B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, $\overline{OE}$ = 0.0V	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		B_0-B_7		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, $\overline{OE}$ = 0.0V	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{NL}	No load voltage	B_0-B_7	I_{OUT} = 0.0mA, T/$\overline{R}$ = 0.0V			2.5		3.7	mA
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	A_0-A_7	V_{CC} = MAX, V_I = 5.5V					1.0	mA
		$\overline{OE}$, T/$\overline{R}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	$\overline{OE}$, T/$\overline{R}$	V_{CC} = MAX, V_I = 2.7V					40	µA
I_{IL}	Low-level input current	$\overline{OE}$, T/$\overline{R}$	V_{CC} = MAX, V_I = 0.5V					-40	µA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied	A_0-A_7	V_{CC} = MAX, V_I =2.7V, T/$\overline{R}$ =4.5V					70	µA
		B_0-B_7	V_{CC} = MAX, V_I =5.0V, T/$\overline{R}$ =0.0V			0.7			mA
			V_{CC} = MAX, V_I =5.5V, T/$\overline{R}$ =0.0V					2.5	mA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied	A_0-A_7	V_{CC} = MAX, V_I =0.5V, T/$\overline{R}$ =4.5V					-70	mA
		B_0-B_7	V_{CC} = MAX, V_I =0.4V, T/$\overline{R}$ =0.0V			-1.3		-3.2	mA
I_{OS}	Short-circuit output current[3]	A_0-A_7	V_{CC} = MAX			-60		-150	mA
		B_0-B_7				-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	A_n=T/$\overline{R}$=4.5V, $\overline{OE}$=0.0V			82	100	mA
		I_{CCL}		A_n= $\overline{OE}$ =0.0V, T/$\overline{R}$= 4.5V			110	135	mA
		I_{CCZ}		$\overline{OE}$=4.5V			95	125	mA

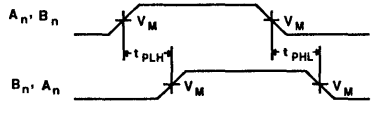
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

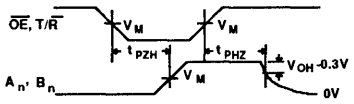
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	Waveform 1	2.0 2.5	3.5 4.5	6.0 7.0	2.0 2.0	7.0 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	5.5 5.0	7.5 7.5	10.0 9.5	5.5 5.0	11.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 2 Waveform 3	2.5 2.5	4.5 4.0	7.0 7.0	2.5 2.5	8.0 7.5	ns

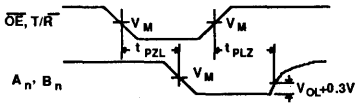
AC WAVEFORMS



Waveform 1. Propagation Delay For Non-Inverting Outputs



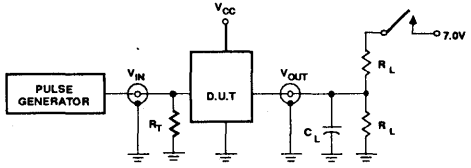
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

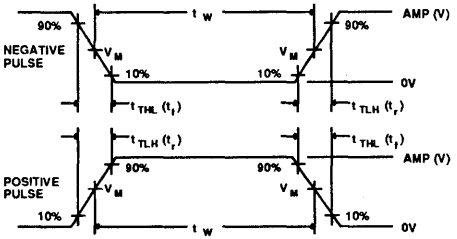
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F595
Shift Register

FAST Products

8-Bit Shift Register with Output Latches (3-state)
Product Specification

FEATURES

- **Low noise, no switching feedthru current**
- **Controlled output edge rates**
- **High impedance PNP base inputs for reduced loading (20μA in High and Low states)**
- **8-bit serial-in, parallel-out shift register with storage**
- **3-state outputs**
- **Shift register has direct clear**
- **Guaranteed shift frequency-DC to 100MHz**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F595	130MHz	65mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F595N
16-Pin Plastic SO	N74F595D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_S	Serial data input	1.0/0.033	20μA/20μA
SHCP	Shift register clock pulse input (active rising edge)	1.0/0.033	20μA/20μA
STCP	Storage register clock pulse input (active rising edge)	1.0/0.033	20μA/20μA
$\overline{SHR}$	Shift register reset input (active Low)	1.0/0.033	20μA/20μA
$\overline{OE}$	Output enable input (active Low)	1.0/0.033	20μA/20μA
Q_S	Serial expansion output	50/33	1.0mA/20mA
Q_0 - Q_7	Data outputs	150/40	3.0mA/24mA

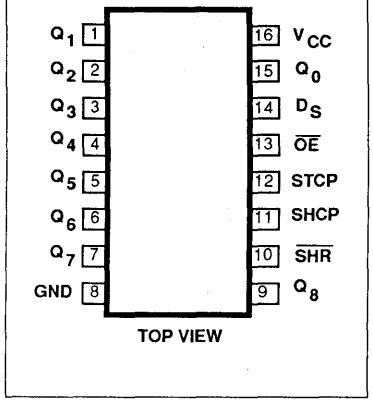
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 74F595 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct overriding clear, serial input and serial output pins for cascading. Both the shift register and storage register clocks are positive edge-triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

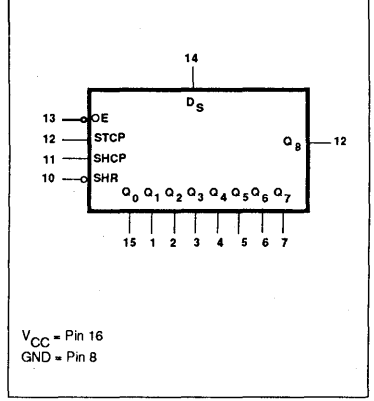
This device uses patented circuitry to control system noise and internal ground bounce. This is done by eliminating switching feedthru current and controlling both Low-to-High and High-to-Low slew rates.

PIN CONFIGURATION



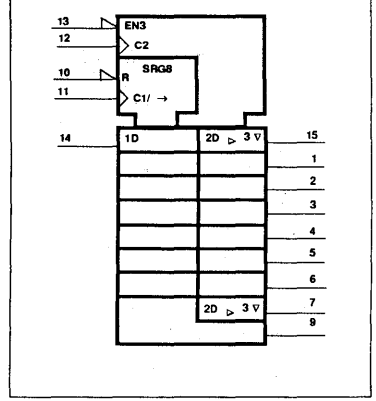
TOP VIEW

LOGIC SYMBOL

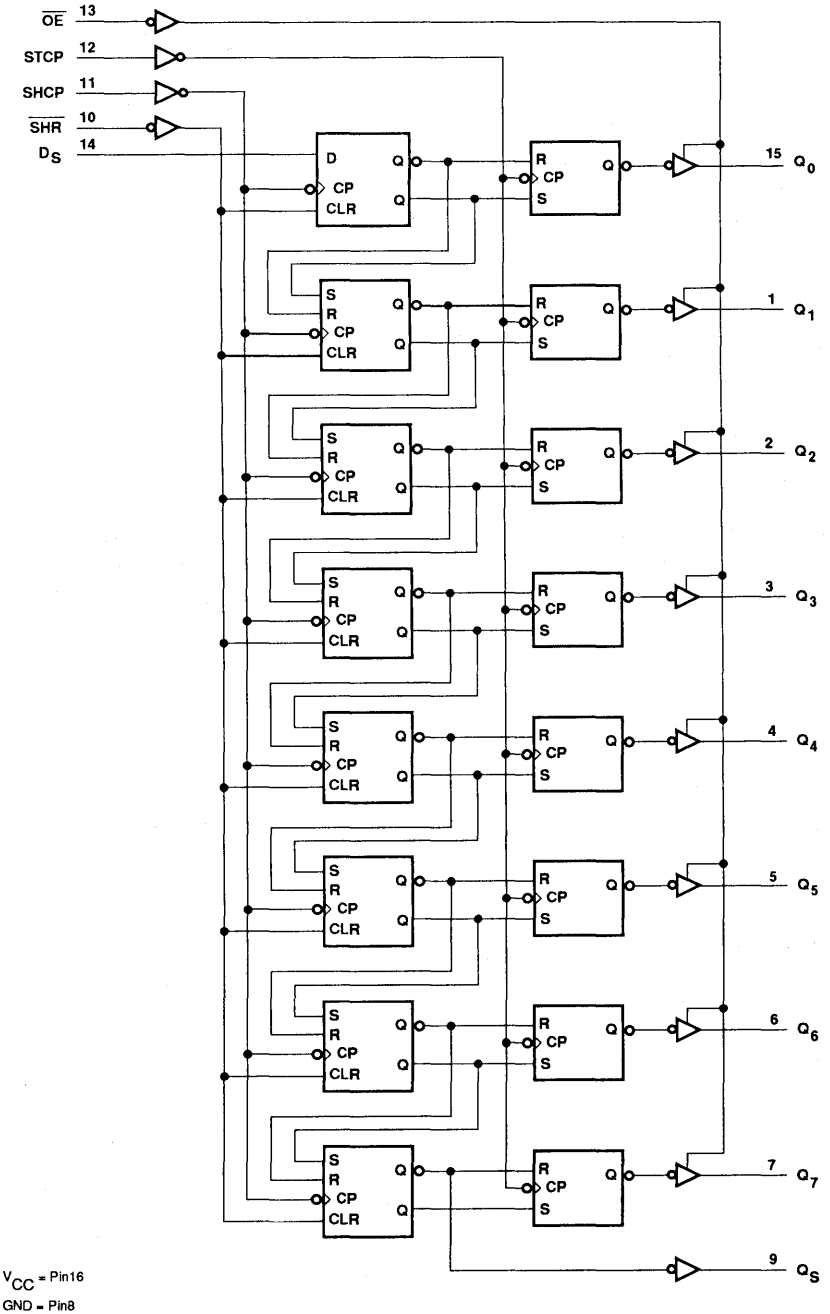


V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT - FUNCTION TABLE

INPUTS					INTERNAL SHIFT REGISTERS		INTERNAL STORAGE REGISTER	OUTPUTS		OPERATING MODE
$\overline{OE}$	$\overline{SHR}$	SHCP	STCP	D_S	O_0	O_1 - O_7	Q_0 - Q_7	Q_0 - Q_7	Q_S	
H	H	↕	↕	X	O_0	O_1 - O_7	Q_0 - Q_7	Z	Q_7	No change
H	L	X	↕	X	L_0	L	Q_0 - Q_7	Z	L	Clear shift register, hold latch
L	L	X	↕	X	L_0	L	Q_0 - Q_7	Q_0 - Q_7	L	
H	H	↑	↕	d_s	D_s	o_0 - o_6	Q_0 - Q_7	Z	o_6	Shift
L	H	↑	↕	d_s	D_s	o_0 - o_6	Q_0 - Q_7	Q_0 - Q_7	o_6	
H	H	↕	↑	X	O_0	O_1 - O_7	o_0 - o_7	Z	Q_7	Store
L	H	↕	↑	X	O_0	O_1 - O_7	o_0 - o_7	o_0 - o_7	Q_7	
H	H	↑	↑	d_s	D_s	o_0 - o_6	o_0 - o_7*	Z	o_6	Store, then shift
L	H	↑	↑	d_s	D_s	o_0 - o_6	o_0 - o_7*	o_0 - o*	o_6	

H = High voltage level.
L = Low voltage level.
X = Don't care.
Z = High impedance.
d_n(o_n) = Lower case letters indicate the state of the referenced input (or output) one set up time prior to the Low -to-High clock transition.
↑ = Low-to-High clock transition.
↕ = Not a Low-to-High clock transition.
*= When clocking both SHCP and STCP simultaneously the Shift Register state will always be one clock pulse ahead of the Storage Register.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	Q_S	40	mA
		Q_0- Q_7	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_S			-1	mA
		Q_0- Q_7			-3	mA
I_{OL}	Low-level output current	Q_S			20	mA
		Q_0- Q_7			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	Q_S	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		Q_0- Q_7		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	Q_S	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=20mA	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
		Q_0- Q_7		I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	mA
I_{OZH}	Off state output current, High-level voltage applied	Q_0- Q_7 only	V_{CC} =MAX, V_O=2.7V					50	µA
I_{OZL}	Off state output current, Low-level voltage applied	Q_0- Q_7 only	V_{CC} =MAX, V_O=0.5V					-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				55	85	mA
		I_{CCL}					70	105	mA
		I_{CCZ}					65	105	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

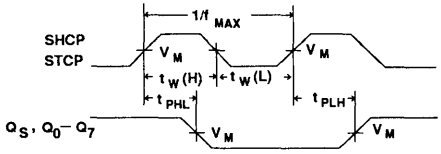
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	115	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay SHCP to Q_S	Waveform 1	6.0 2.5	8.0 4.5	10.5 7.5	5.0 2.5	12.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay STCP to Q_0- Q_7	Waveform 1	5.5 3.0	8.0 5.0	11.0 8.0	4.5 3.0	13.0 8.5	ns
t_{PHL}	Propagation delay $\overline{SHR}$ to Q_S	Waveform 2	3.5	5.5	8.0	3.0	8.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_0- Q_7	Waveform 5 Waveform 6	3.5 3.0	5.5 5.5	9.0 8.5	2.5 2.5	10.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q_0- Q_7	Waveform 5 Waveform 6	2.0 4.0	4.0 6.0	7.0 9.0	1.5 3.0	8.5 10.0	ns

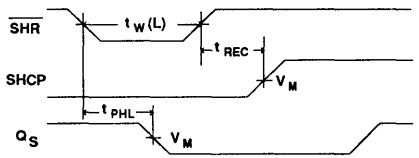
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_S to SHCP	Waveform 3	2.0 2.0			2.5 2.5		ns
t_h(H) t_h(L)	Hold time, High or Low D_S to SHCP	Waveform 3	0 0			0 0		ns
t_s(L)	Setup time, Low $\overline{SHR}$ to STCP	Waveform 3	4.5			5.0		ns
t_s(H)	Setup time, High SHCP to STCP	Waveform 4	4.5			5.0		ns
t_w(H) t_w(L)	SHCP Pulse width, High or Low	Waveform 1	3.5 4.0			4.0 4.0		ns
t_w(H) t_w(L)	STCP Pulse width, High or Low	Waveform 1	4.0 3.0			4.0 3.5		ns
t_w(L)	$\overline{SHR}$ Pulse width, Low	Waveform 2	3.0			3.0		ns
t_{REC}	Recovery time $\overline{SHR}$ to SHCP	Waveform 2	3.0			3.0		ns

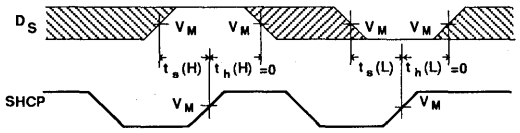
AC WAVEFORMS



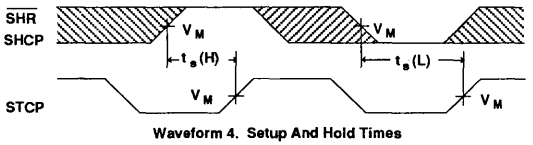
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



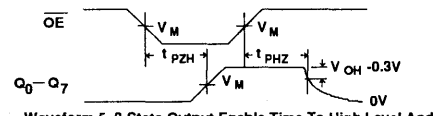
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



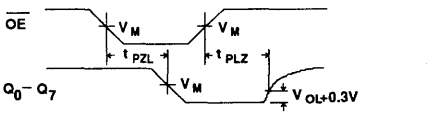
Waveform 3. Data Setup And Hold Times



Waveform 4. Setup And Hold Times



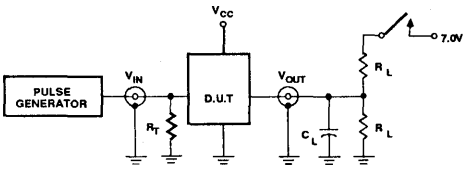
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

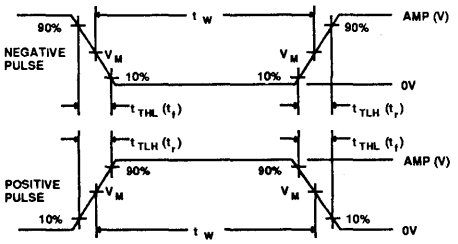
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F597, 74F598
Shift Registers

74F597 8-Bit Shift Register with Input Latches
74F598 8-Bit Shift Register with Input Latches (3-State)
Preliminary Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F597	120MHz	75mA
74F598	120MHz	75mA

FEATURES

- **High impedance NPN base input for reduced loading (20μA in High and Low states)**
- **8-bit Parallel storage register**
- **Shift register has asynchronous direct overriding load and reset**
- **Guaranteed shift frequency DC to 120MHz**
- **Parallel 3-State I/O, Storage register inputs**
- **Shift register outputs-'F598**

DESCRIPTION

The 74F597 consists of an 8-bit storage register feeding a parallel-in, serial out 8-bit shift register. The storage register and shift register have separate positive edge triggered clocks. The shift register also has asynchronous direct load (from storage) and reset inputs.

The 74F598 consists of an 8-bit storage register feeding a parallel/serial-in, parallel/serial out 8-bit shift register. Both the storage register and shift register have positive edge triggered clocks. The shift register also has asynchronous direct load (from storage) and reset inputs. The 'F598 has 3-state I/O ports that provide parallel shift register outputs and also has multiplexed serial data input.

ORDERING INFORMATION

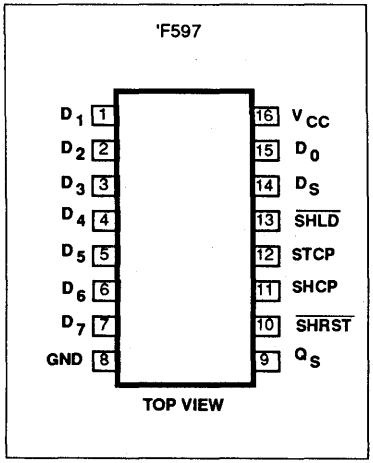
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F597N
20-Pin Plastic DIP	N74F598N
16-Pin Plastic SO	N74F597D
20-Pin Plastic SOL	N74F598D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

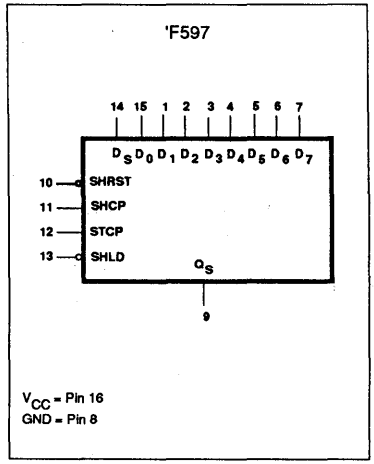
	PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F597	D_S	Serial data input	1.0/0.033	20μA/20μA
	D_0-D_7	Parallel data inputs	1.0/0.033	20μA/20μA
	SHCP	Shift register clock pulse input	1.0/0.033	20μA/20μA
	STCP	Storage register clock pulse input	1.0/0.033	20μA/20μA
	$\overline{SHLD}$	Shift register load input (active Low)	1.0/0.033	20μA/20μA
	$\overline{SHRST}$	Shift register reset input (active Low)	1.0/0.033	20μA/20μA
	Q_S	Serial data output	50/33	1.0mA/20mA
'F598	I/O_n	Parallel data inputs	1.0/0.033	20μA/20μA
	D_{S0}, D_{S1}	Serial data inputs	1.0/0.033	20μA/20μA
	SHCP	Shift register clock pulse input	1.0/0.033	20μA/20μA
	$\overline{STCP}$	Storage register clock pulse input	1.0/0.033	20μA/20μA
	$\overline{SHCPEN}$	Shift register clock pulse enable input	1.0/0.033	20μA/20μA
	$\overline{SHLD}$	Shift register load input (active Low)	1.0/0.033	20μA/20μA
	$\overline{SHRST}$	Shift register reset input (active Low)	1.0/0.033	20μA/20μA
	S	Serial data selector input	1.0/0.033	20μA/20μA
	$\overline{OE}$	Output Enable input	1.0/0.033	20μA/20μA
	Q_S	Serial data output	50/33	1.0mA/20mA
	I/O_n	Parallel data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

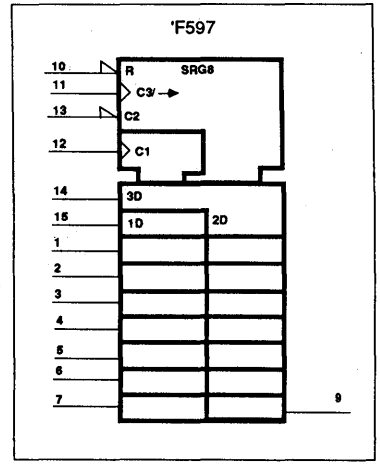
PIN CONFIGURATION



LOGIC SYMBOL

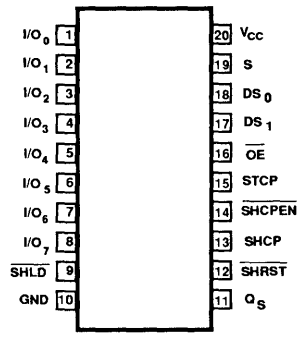


LOGIC SYMBOL(IEEE/IEC)



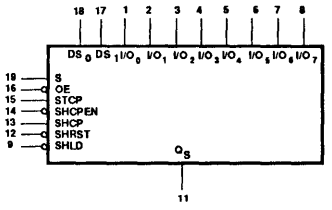
PIN CONFIGURATION

'F598



LOGIC SYMBOL

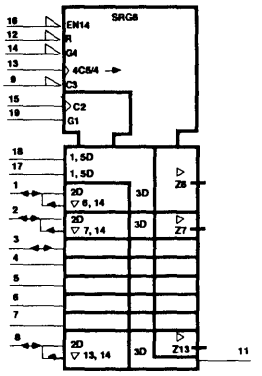
'F598



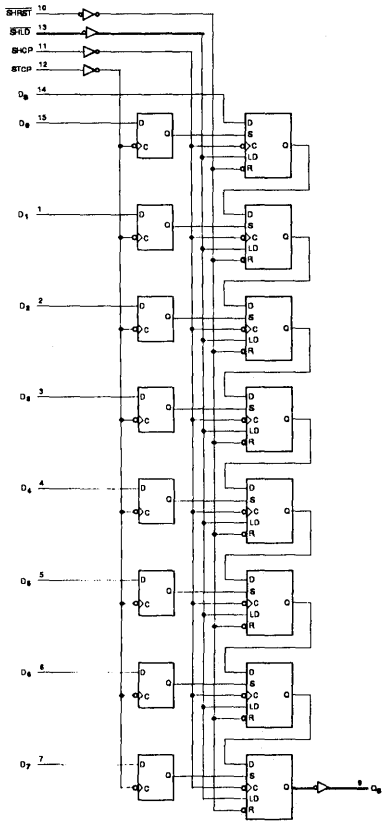
VCC = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)

'F598

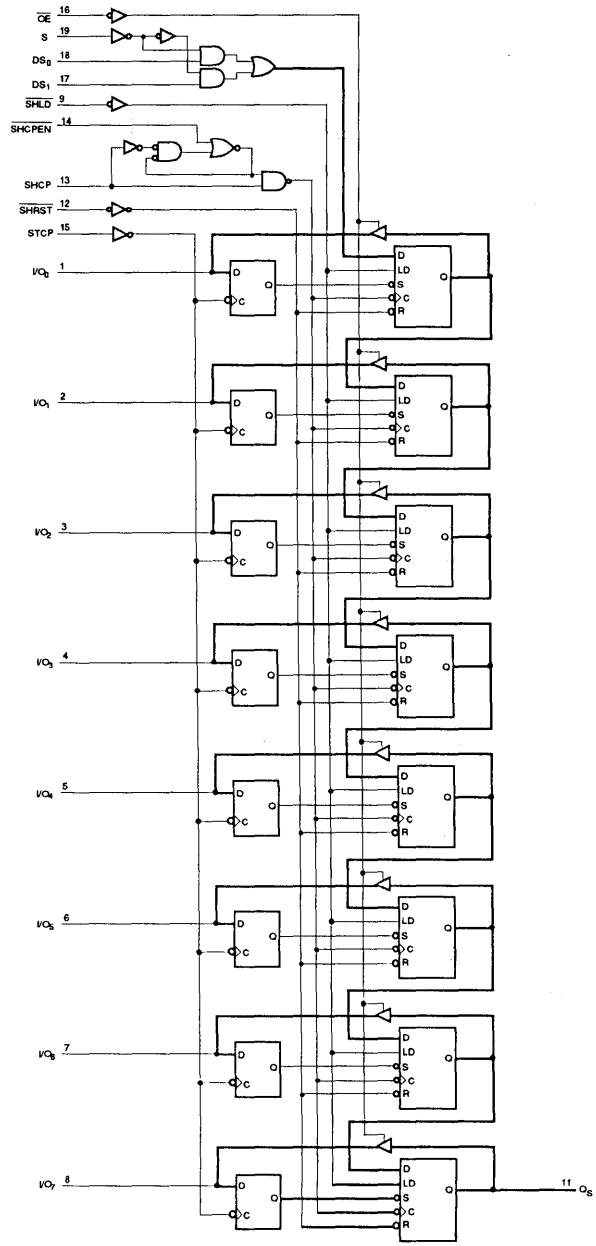


LOGIC DIAGRAM for 'F597



VCC = Pin16
GND = Pin8

LOGIC DIAGRAM FOR 'F598



V_{CC} = Pin 20

GND = Pin 10

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	Q_S	40	mA
		I/O_0- I/O_7	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_S			-1	mA
		I/O_0- I/O_7			-3	mA
I_{OL}	Low-level output current	Q_S			20	mA
		I/O_0- I/O_7			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	Q_S	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MI	I_{OL}=MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		I/O_n	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
$I_{OZH}+I_{IH}$	Off-state output current High-level voltage applied	I/O_n only	V_{CC} = MAX, V_O= 2.7V					70	µA
$I_{OZL}+I_{IL}$	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-70	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	'F597	I_{CCH}	V_{CC} = MAX			45	70	mA
			I_{CCL}				48	75	mA
		'F598	I_{CCH}				75	90	mA
			I_{CCL}				78	95	mA
			I_{CCZ}				85	100	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 'F597

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximun clock frequency	Waveform 1	100	120		80		MHz
t_{PLH} t_{PHL}	Propagation delay SHCP to Q_S	Waveform 1	4.0 4.0	6.5 7.0	8.5 9.0	4.0 4.0	9.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHLD}$ to Q_S	Waveform 1	4.0 4.0	7.5 8.0	9.5 10.0	4.0 4.0	10.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay STCP to Q_S	Waveform 1	4.0 4.0	7.5 8.0	9.5 10.0	4.0 4.0	10.0 11.0	ns
t_{PHL}	Propagation delay, $\overline{SHRST}$ to Q_S	Waveform 3	4.0	8.0	10.0	4.0	11.0	ns

AC SETUP REQUIREMENTS for 'F597

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_S to SHCP	Waveform 3	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_S to SHCP	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low STCP to $\overline{SHLD}$	Waveform 4	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low STCP to $\overline{SHLD}$	Waveform 4	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	SHCP pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(H)$ $t_w(L)$	STCP pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	$\overline{SHRST}$ pulse width, Low	Waveform 1	4.0			4.0		ns
$t_w(L)$	$\overline{SHLD}$ pulse width, Low	Waveform 1	4.0			4.0		ns
t_{REC}	Recovery time, $\overline{SHRST}$ to SHCP	Waveform 2	6.0			7.0		ns
t_{REC}	Recovery time, $\overline{SHLD}$ to SHCP	Waveform 2	6.0			7.0		ns

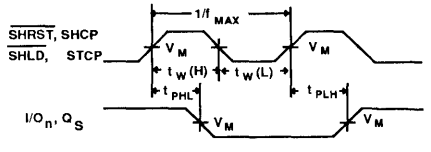
AC ELECTRICAL CHARACTERISTICS for 'F598

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximun clock frequency	Waveform 1	100	120		80		MHz
t_{PLH} t_{PHL}	Propagation delay SHCP to Q_S	Waveform 1	4.0 4.0	6.5 7.0	8.5 9.0	4.0 4.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay STCP to Q_S ($\overline{SHLD}$ =Low)	Waveform 1	4.0 4.0	7.5 8.0	9.5 10.0	4.0 4.0	10.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHLD}$ to Q_S	Waveform 1	4.0 4.0	7.5 8.0	9.0 9.0	4.0 4.0	10.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay SHCP to I/O_n	Waveform 1	4.0 4.0	7.0 7.0	9.0 9.0	4.0 4.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SHLD}$ to I/O_n	Waveform 1	4.0 4.0	7.0 7.0	9.0 9.0	4.0 4.0	10.0 10.0	ns
t_{PHL}	Propagation delay, $\overline{SHRST}$ to I/O_n	Waveform 2	4.0	8.0	10.0	4.0	11.0	ns
t_{PHL}	Propagation delay, $\overline{SHRST}$ to Q_S	Waveform 2	4.0	8.0	10.0	4.0	11.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 5 Waveform 6	4.0 4.0	7.5 7.5	9.0 9.0	4.0 4.0	10.5 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 5 Waveform 6	3.0 3.0	6.0 6.0	8.0 8.0	3.0 3.0	9.0 9.0	ns

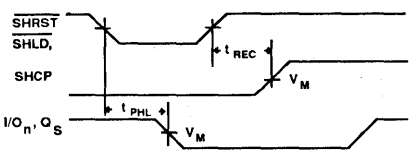
AC SETUP REQUIREMENTS for 'F598

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_{Sn} to SHCP	Waveform 3	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_{Sn} to SHCP	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low STCP to $\overline{SHLD}$	Waveform 4	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low STCP to $\overline{SHLD}$	Waveform 4	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{SHCPEN}$ to SHCP	Waveform 3	6.0 6.0			6.0 6.0		ns
$t_w(H)$ $t_w(L)$	SHCP pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(H)$ $t_w(L)$	STCP pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	$\overline{SHRST}$ pulse width, Low	Waveform 1	4.0			4.0		ns
$t_w(L)$	$\overline{SHLD}$ pulse width, Low	Waveform 1	4.0			4.0		ns
t_{REC}	Recovery time, $\overline{SHRST}$ to SHCP	Waveform 2	6.0			7.0		ns
t_{REC}	Recovery time, $\overline{SHLD}$ to SHCP	Waveform 2	6.0			6.0		ns

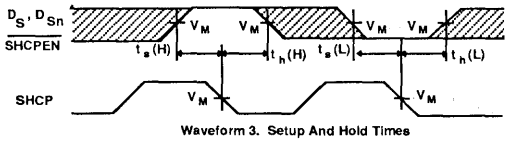
AC WAVEFORMS



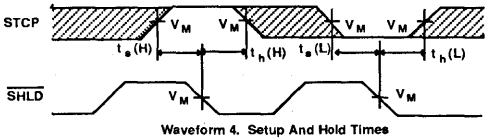
Waveform 1. Propagation Delay, Clock Inputs To Output, Clock Pulse Width, Maximum Clock Frequency, Shift Register Reset And Load Inputs To Serial Data Output



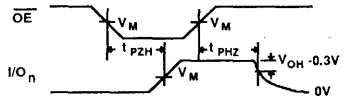
Waveform 2. Propagation Delay, Shift Register Reset And Load InputsTo Serial Data Output, Shift Register Reset And Load Inputs To Shift register Clock Pulse Input Recovery Time



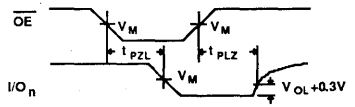
Waveform 3. Setup And Hold Times



Waveform 4. Setup And Hold Times



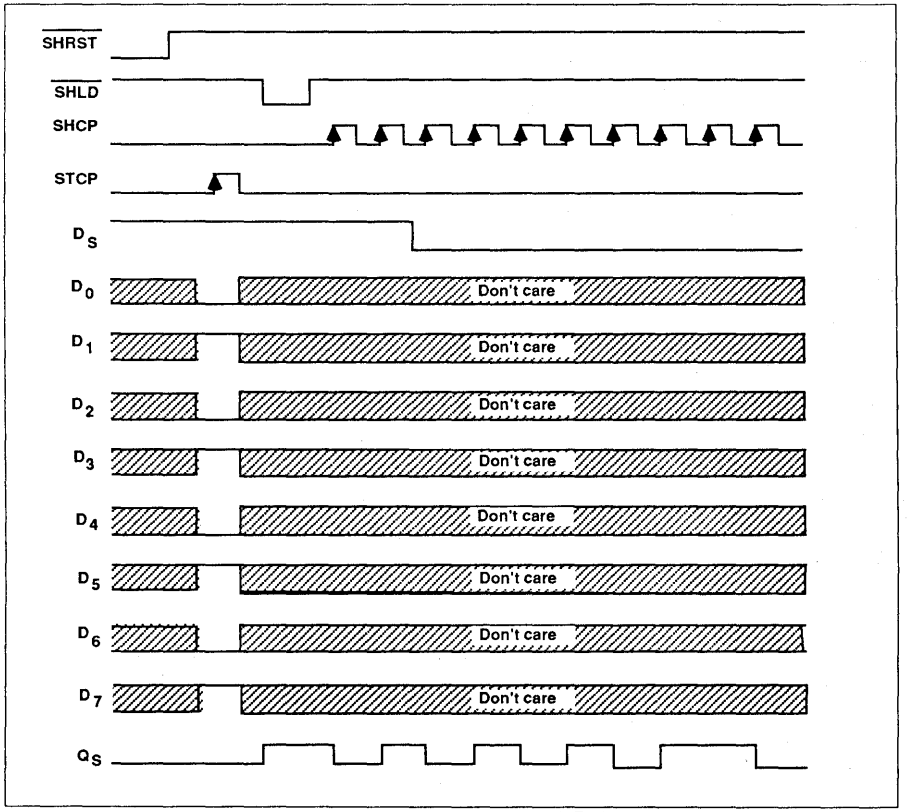
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



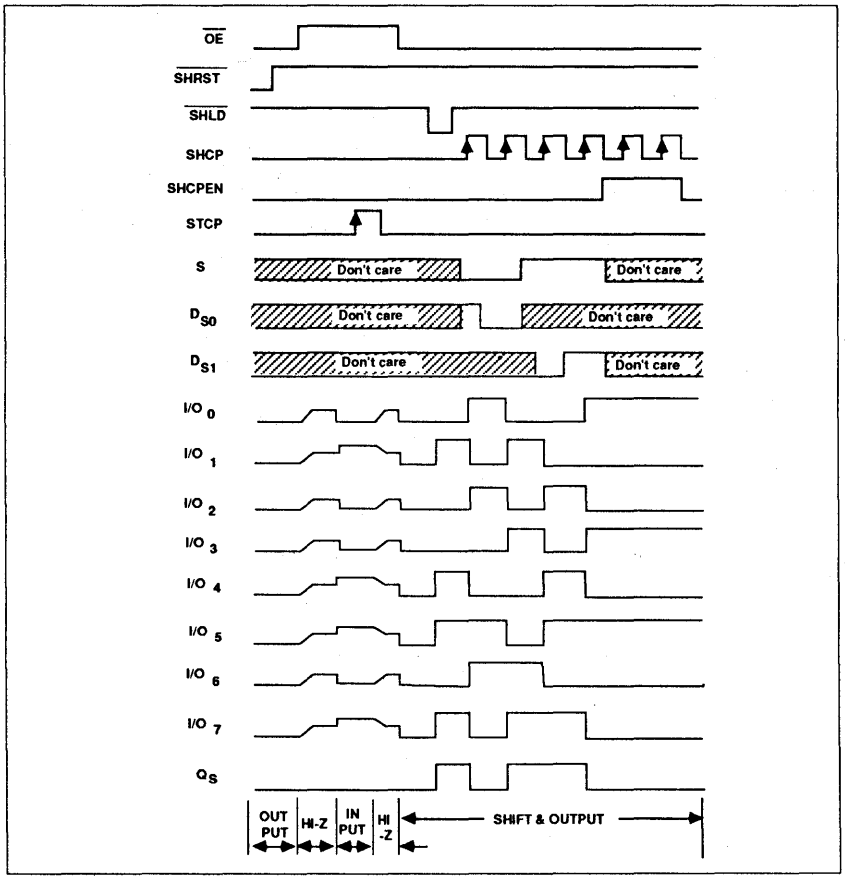
Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

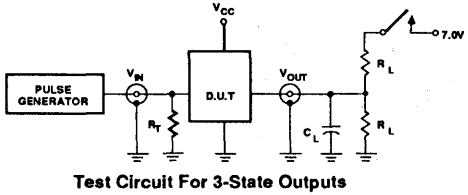
TYPICAL TIMING DIAGRAM for 74F597



TYPICAL TIMING DIAGRAM for 74F598



TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

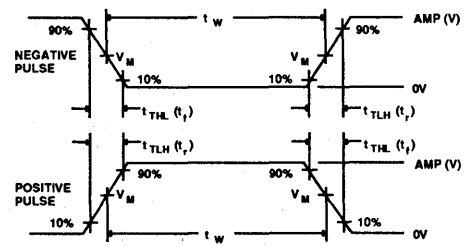
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F604
Register

FAST Products

Dual Octal Register (3-State)

Product Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Stores 16-bit-wide Data inputs, multiplexed 8-bit outputs**
- **3-state outputs**
- **Typical shift frequency of 105 MHz**
- **Power supply current 75mA typical**

DESCRIPTION

The 74F604 contains 16 D-type edge triggered flip-flops with common and individual data inputs. Organized as 8-bit A and B registers, the flip-flop outputs are connected by pairs to eight 2-input multiplexers. A Select (SELECT $A/\overline{B}$) input determines whether the A or B register contents are multiplexed to the eight 3-state outputs. Data entered from the B inputs are selected when SELECT $A/\overline{B}$ is Low: data from the A inputs are selected when SELECT $A/\overline{B}$ is High. Data enters the flip-flops on the rising edge of the clock (CP) input, which also controls the 3-state outputs. The outputs are enabled when CP is High and disabled when CP is Low.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F604	105MHz	75mA

ORDERING INFORMATION

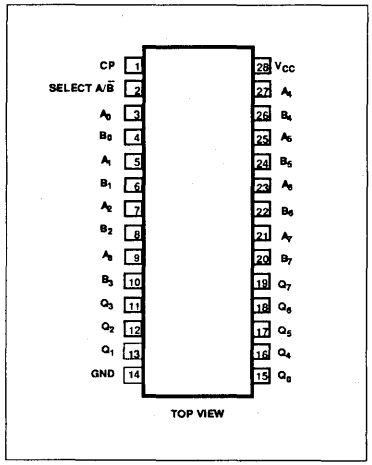
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP	N74F604N
28-Pin Plastic SOL	N74F604D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

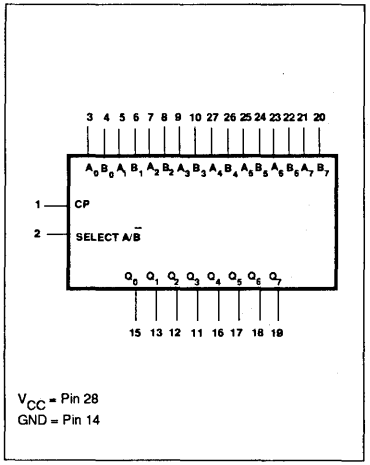
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_7, B_0-B_7	Data inputs	1.0/0.033	20μA/20μA
SELECT $A/\overline{B}$	Select input	1.0/0.033	20μA/20μA
CP	Clock Pulse Input (active rising edge)	1.0/0.033	20 A/20 A
Q_0-Q_7	Data outputs	150/40	3mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

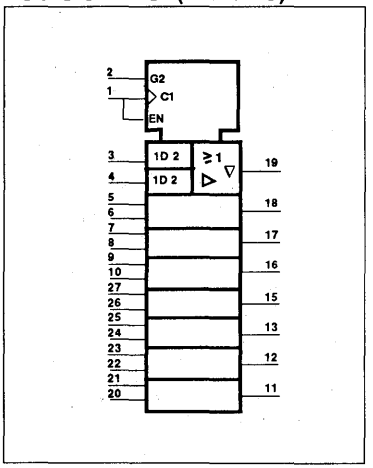
PIN CONFIGURATION



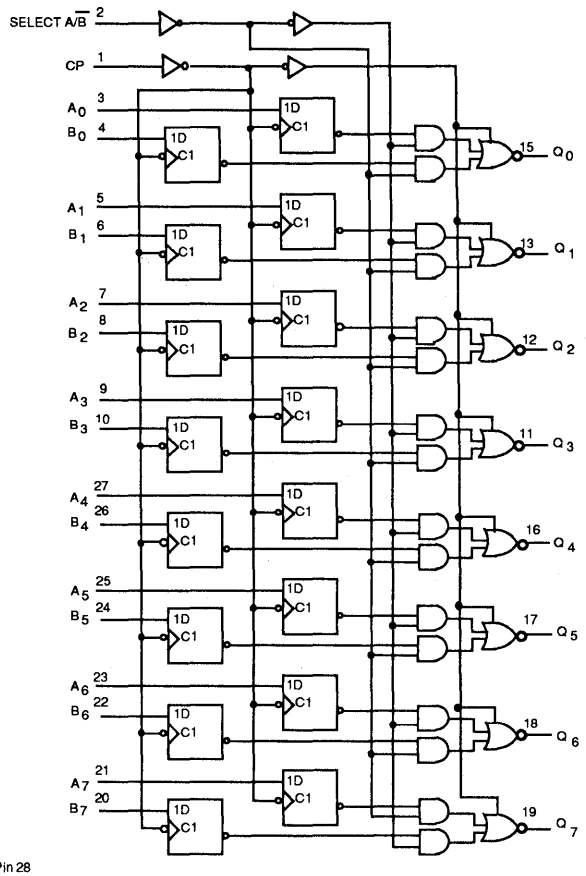
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS
A_0-A_7	B_0-B_7	SELECT A/$\overline{B}$	CP	Q_0-Q_7
A data	B data	L	↑	B data
A data	B data	H	↑	A data
X	X	X	L	Z
X	X	L	H	B register stored data
X	X	H	H	A register stored data

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	A_n, B_n, SELECT A/$\overline{B}$=4.5V, CP= ↑		60	82	mA
		I_{CCL}		A_n, B_n, SELECT A/$\overline{B}$=GND, CP= ↑		75	100	mA
		I_{CCZ}		A_n, B_n, SELECT A/$\overline{B}$=GND, CP= GND		75	100	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed lasty.

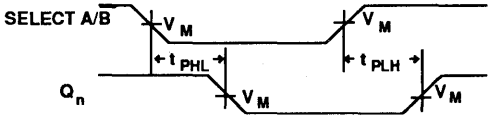
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 3	95	105		80		MHz
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Q_n (B register)	Waveform 1	5.0 6.0	7.0 8.5	9.0 10.5	4.5 5.5	10.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Q_n (A register)	Waveform 2	6.0 4.0	8.0 6.5	10.0 8.5	5.5 3.5	11.5 9.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 4 Waveform 5	5.0 6.5	7.5 9.0	9.5 11.0	4.5 6.0	10.5 12.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 4 Waveform 5	5.0 5.0	7.0 7.0	9.5 9.5	4.5 4.5	11.0 11.0	ns

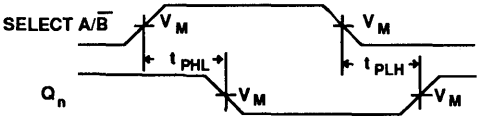
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n, B_n, SELECT A/$\overline{B}$ to CP	Waveform 3	1.0 2.0			2.0 3.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n, B_n, SELECT A/$\overline{B}$ to CP	Waveform 3	0 1.0			0 1.5		ns
t_w(H)	CP Pulse width, High	Waveform 3	5.0			6.0		ns

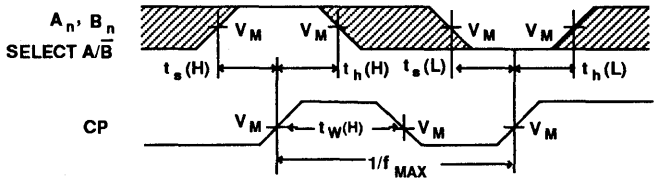
AC WAVEFORMS



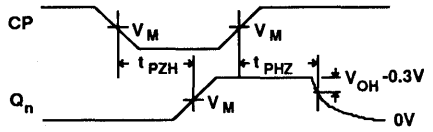
Waveform 1. Propagation Delay, SELECT A/B To Output (B register stored data=Low. CP=H)



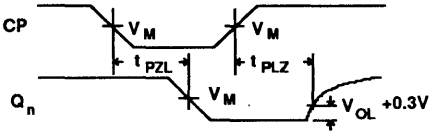
Waveform 2. Propagation Delay, SELECT A/B To Output (A register stored data=Low. CP=H)



Waveform 3. Data And Select Setup And Hold Times ,Clock pulse width , And Maximum Clock Frequency



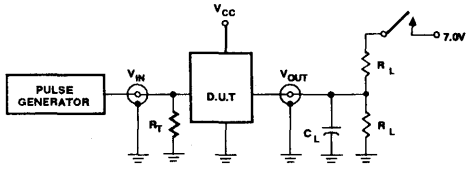
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

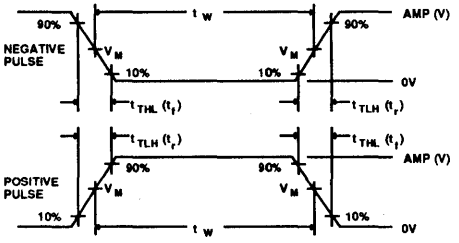
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F605
Register

FAST Products

Dual Octal Register (Open Collector)

Product Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Stores 16-bit-wide Data inputs, multiplexed 8-bit outputs**
- **Open Collector outputs**
- **Propagation delay 10ns typical**
- **Power supply current 85mA typical**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F605	105MHz	85mA

DESCRIPTION

The 74F605 contains 16 D-type edge triggered flip-flops with commom clock and individual data inputs. Organized as 8-bit A and B registers, the flip-flop outputs are connected by pairs to eight 2-input multiplexers. A Select (SELECT A/$\overline{B}$) input determines whether the A or B register contents are multiplexed to the eight Open Collector outputs. Data entered from the B inputs are selected when SELECT A/$\overline{B}$ is Low; data from the A inputs are selected when SELECT A/$\overline{B}$ is High. Data enters the flip-flops on the rising edge of the clock (CP) input, which also controls the Open Collector outputs. The outputs are enabled when CP is High and disabled when CP is Low.

These functions are well-suited for receiving 16-bit simultaneous data and transmitting it as two sequential 8-bit words.

ORDERING INFORMATION

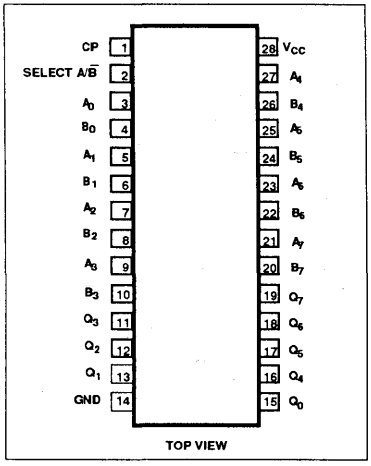
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP	N74F605N
28-Pin Plastic SOL	N74F605D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

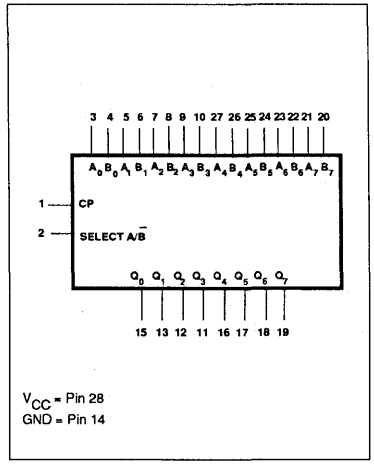
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_7, B_0-B_7	Data inputs	1.0/0.033	20μA/20μA
SELECT A/$\overline{B}$	Select input	1.0/0.033	20μA/20μA
CP	Clock Pulse Input (active rising edge)	1.0/0.033	20μA/20μA
Q_0-Q_7	Data outputs	OC/40	OC/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC = Open Collector

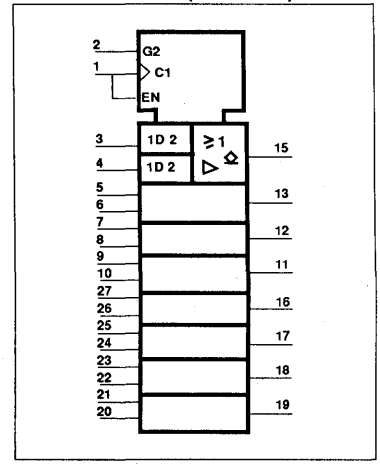
PIN CONFIGURATION



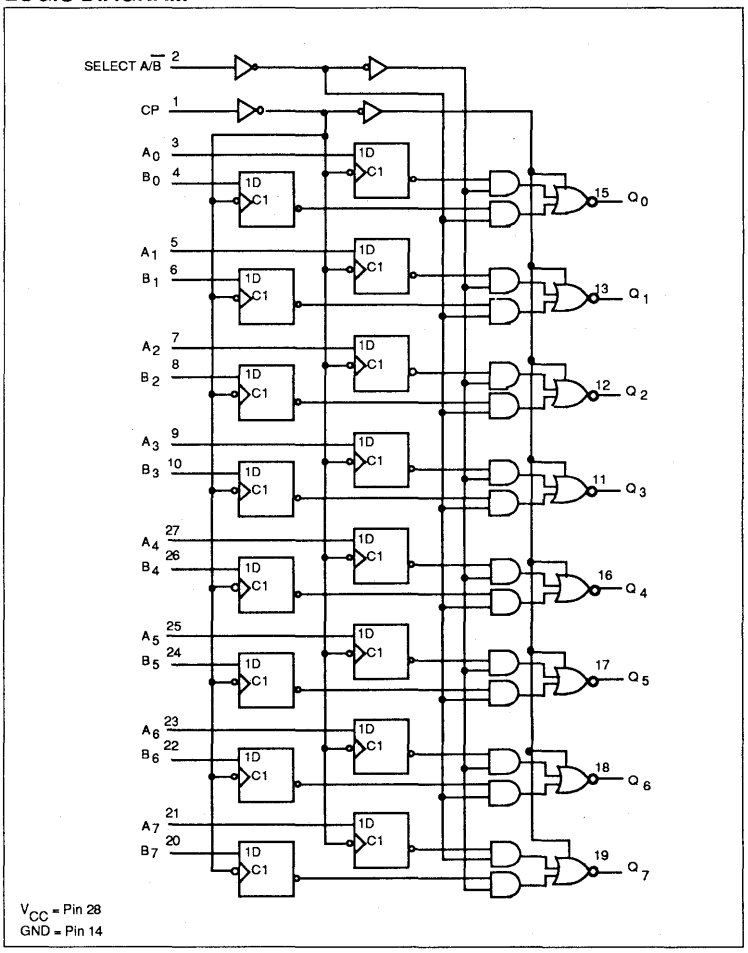
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS
A_0-A_7	B_0-B_7	SELECT A/$\overline{B}$	CP	Q_0-Q_7
A data	B data	L	↑	B data
A data	B data	H	↑	A data
X	X	X	L	OFF
X	X	L	H	B register stored data
X	X	H	H	A register stored data

H = High voltage level
L = Low voltage level
X = Don't care
OFF= Pulled up through resistor (open collector)
↑ =Low-to-High transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=4.5V					250	µA
V_{OL}	Low-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		.35	.50	V
					±5%V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{CC}	Supply current [total]	I_{CCH}	V_{CC} = MAX	A_n = B_n = SELECT $A/\overline{B}$ = 4.5V, CP =↕			80	100	mA
		I_{CCL}		A_n = B_n = SELECT $A/\overline{B}$ = GND, CP =↕			85	105	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

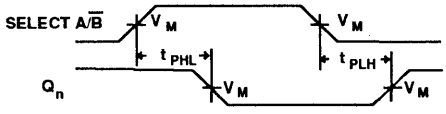
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 4	95	105		80		MHz
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Q_n (B register)	Waveform 2	7.5 7.5	9.5 10.0	11.5 12.0	7.0 7.0	12.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Q_n (A register)	Waveform 1	8.5 6.5	11.0 8.5	13.0 11.0	8.0 6.0	14.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 3	8.5 6.5	11.0 9.0	13.0 11.0	8.0 6.0	14.5 12.0	ns

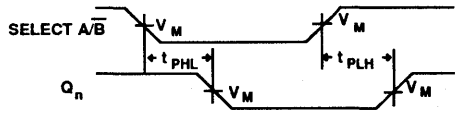
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n, B_n, SELECT A/$\overline{B}$ to CP	Waveform 4	1.0 3.0			2.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n, B_n, SELECT A/$\overline{B}$ to CP	Waveform 4	1.0 2.0			2.0 3.0		ns
$t_w(H)$	CP Pulse width, High	Waveform 4	5.0			6.0		ns

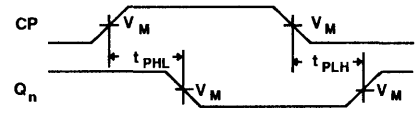
AC WAVEFORMS



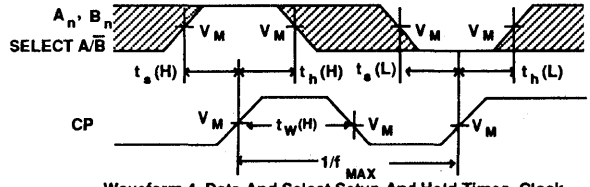
Waveform 1. Propagation Delay, SELECT A/$\overline{B}$ To Output (A register stored data=Low. CP=H)



Waveform 2. Propagation Delay, SELECT A/$\overline{B}$ To Output (B register stored data=Low. CP=H)



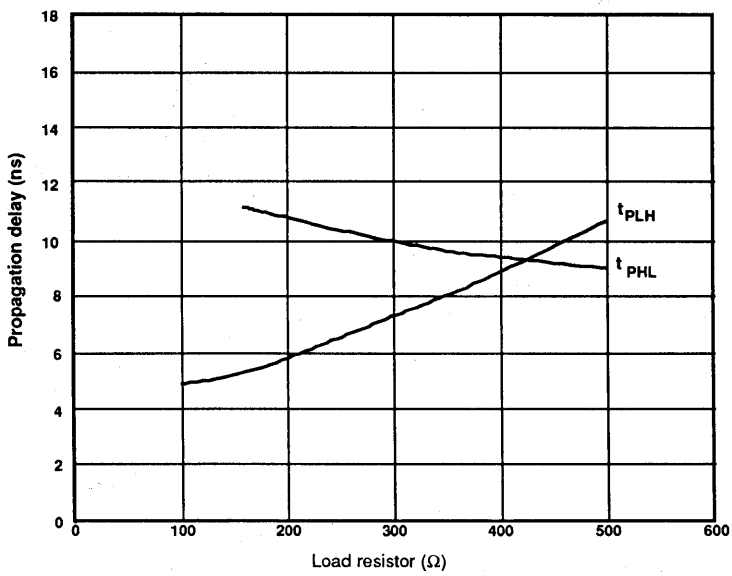
Waveform 3. Propagation Delay, Clock To Output (A register stored data=Low. SELECT A/$\overline{B}$=H,)



Waveform 4. Data And Select Setup And Hold Times ,Clock pulse width , And Maximum Clock Frequency

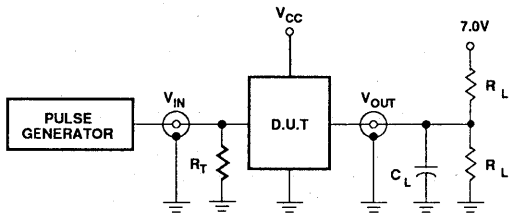
NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

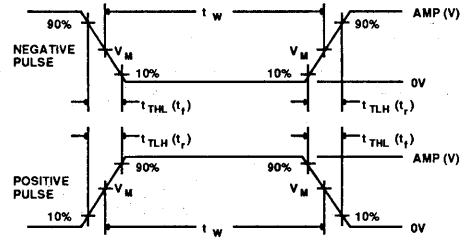


NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F620, 74F623 Transceivers

FAST Products

74F620 Octal Bus Transceiver, Inverting (3-State)
74F623 Octal Bus Transceiver, Non-Inverting (3-State)
Product Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (70μA in High and Low states)**
- **Ideal for applications which require high output drive and minimal bus loading**
- **Octal bidirectional bus interface**
- **3-state buffer outputs sink 64mA and source 15mA**
- **-'F620 Inverting**
  -'F623 Non-Inverting

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F620	3.5ns	80mA
74F623	4.5ns	105mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F620N, N74F623N
20-Pin Plastic SOL[1]	N74F620D, N74F623D

NOTE:
1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal considerations for suface mounted device.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

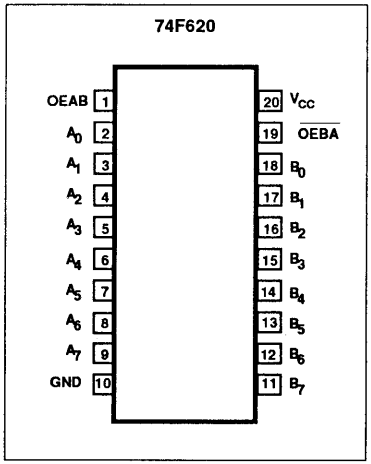
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0-A_7, B_0-B_7	Data inputs	3.5/1.16	70μA/70μA
$\overline{OEBA}$, OEAB	Output Enable inputs	1.0/0.033	20μA/20μA
A_0-A_7	Data outputs	150/40	3mA/24mA
B_0-B_7	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

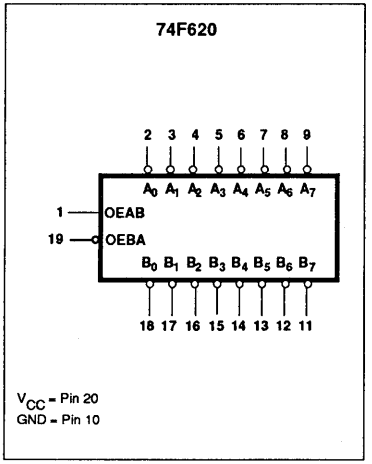
DESCRIPTION

The 74F620 is an octal bus transceiver featuring inverting 3-state bus-compatible outputs in both send and receive directions. The outputs are capable of sinking 64mA and sourcing up to 15mA, providing very good capacitive drive characteristics. The 74F623 is a non-inverting version of the 74F620.These octal bus transceivers are designed for asynchronous two-way communication between data busses. The control function implementation allows for maximum flexibilty in timing. These devices allow data transmission from the A bus to the B bus or from B bus to A bus, depending upon the logic levels at the Enable inputs ($\overline{OEBA}$ and OEAB). The Enable inputs can be used to disable the device so that the busses are effectively isolated. The dual-enable configuration gives the 'F620 and 'F623 the capability to store data by the simultaneous enabling of $\overline{OEBA}$ and OEAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance,both sets of bus lines (16 in all) will remain at their last states.

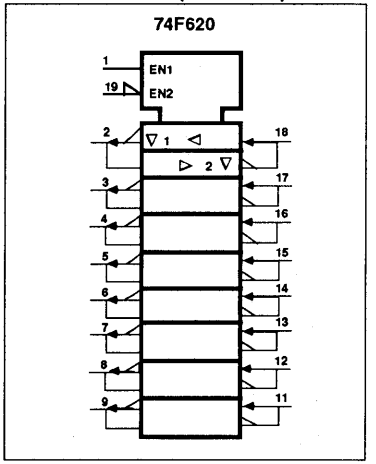
PIN CONFIGURATION



LOGIC SYMBOL

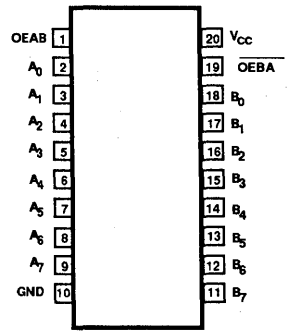


LOGIC SYMBOL(IEEE/IEC)



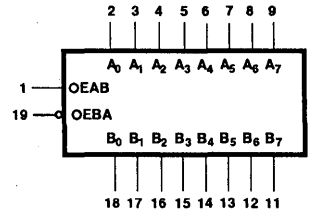
PIN CONFIGURATION

74F623



LOGIC SYMBOL

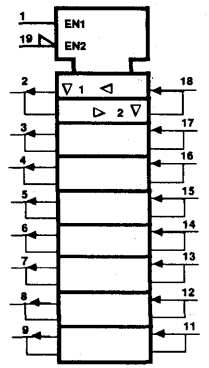
74F623



V_{CC} = Pin 20
GND = Pin 10

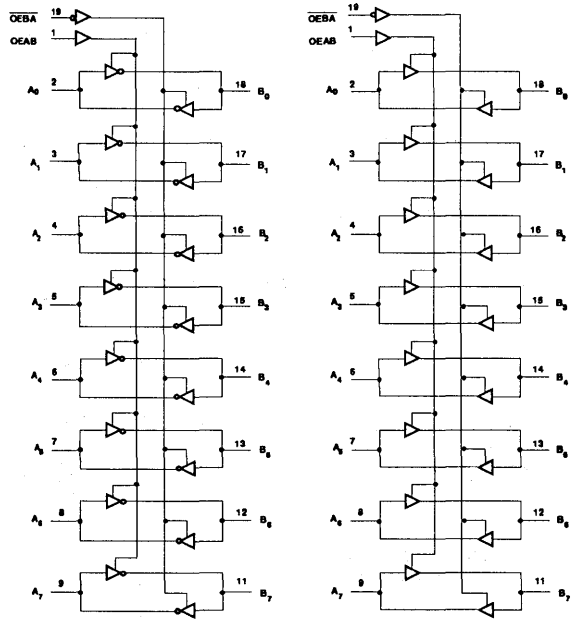
LOGIC SYMBOL(IEEE/IEC)

74F623



LOGIC DIAGRAM

74F620 74F623



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE

INPUTS		OPERATING MODES	
$\overline{OEBA}$	OEAB	'F620	'F623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Z	Z
L	H	$\overline{B}$ data to A bus $\overline{A}$ data to B bus	B data to A bus A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0-B_7			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	A_0-A_7, B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
		B_0-B_7		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEBA}$, OEAB	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		Others	V_{CC} = 5.5V, V_I =5.5V					1	mA
I_{IH}	High-level input current	$\overline{OEBA}$, OEAB only	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OZH} +I_{IH}	Off state output current, High-level voltage applied	A_0-A_7, B_0-B_7	V_{CC} = MAX, V_I = 2.7V					70	µA
I_{OZL}+I_{IL}	Off state output current, Low-level voltage applied		V_{CC} = MAX, V_I = 0.5V					-70	µA
I_{OS}	Short circuit output current[3]	A_0-A_7	V_{CC} = MAX			-60		-150	mA
		B_0-B_7				-100		-225	mA
I_{CC}	Supply current (total)	'F620 I_{CCH}	V_{CC} = MAX	$\overline{OEBA}$=OEAB=4.5V; A_0-A_7=GND			70	92	mA
		'F620 I_{CCL}		$\overline{OEBA}$=OEAB=4.5V; A_0-A_7=4.5V			84	110	mA
		'F620 I_{CCZ}		OEAB=GND; $\overline{OEBA}$= A_0-A_7=4.5V			84	110	mA
		'F623 I_{CCH}	V_{CC} = MAX	$\overline{OEBA}$=OEAB=4.5V; A_0-A_7=4.5V			110	140	mA
		'F623 I_{CCL}		$\overline{OEBA}$=OEAB=4.5V; A_0-A_7=GND			110	140	mA
		'F623 I_{CCZ}		OEAB=GND; $\overline{OEBA}$= A_0-A_7=4.5V			99	130	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

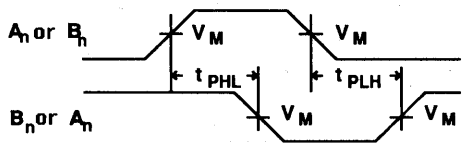
AC CHARACTERISTICS for 'F620

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	2.5 1.0	4.5 2.5	6.5 4.5	2.0 1.0	7.5 5.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	2.5 1.0	4.5 2.5	6.5 4.5	2.0 1.0	7.5 5.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, $\overline{OEBA}$ to A_n	Waveform 3 Waveform 4	3.0 4.0	7.5 7.5	10.5 10.5	2.5 3.5	11.5 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level, $\overline{OEBA}$ to A_n	Waveform 3 Waveform 4	2.5 2.0	4.5 4.5	7.5 7.0	2.0 1.5	8.0 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, OEAB to B_n	Waveform 3 Waveform 4	4.5 4.5	7.5 7.5	10.5 10.0	4.0 4.0	11.5 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level, OEAB to B_n	Waveform 3 Waveform 4	3.0 4.0	6.5 6.5	9.5 9.5	2.5 3.5	10.5 10.5	ns

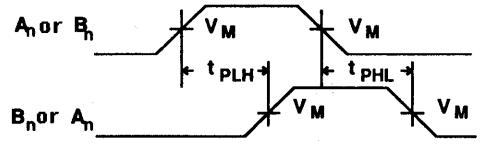
AC CHARACTERISTICS for 'F623

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	2.0 3.0	4.0 5.0	5.5 7.0	2.0 2.5	6.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	2.0 2.5	4.0 4.5	5.5 6.5	2.0 2.5	6.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, $\overline{OEBA}$ to A_n	Waveform 3 Waveform 4	5.0 5.0	8.5 7.5	10.5 9.5	5.0 5.0	12.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level, $\overline{OEBA}$ to A_n	Waveform 3 Waveform 4	2.5 2.5	4.5 4.5	6.5 6.5	2.5 2.5	7.5 7.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, OEAB to B_n	Waveform 3 Waveform 4	5.0 4.5	8.0 7.0	10.0 9.0	5.0 4.5	11.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level, OEAB to B_n	Waveform 3 Waveform 4	3.0 4.0	6.0 7.0	8.5 9.0	3.0 4.0	10.0 10.0	ns

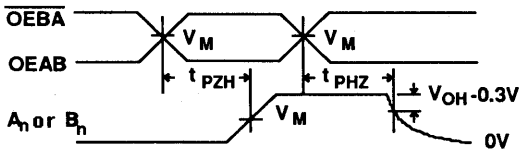
AC WAVEFORMS



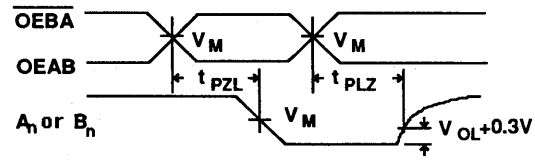
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



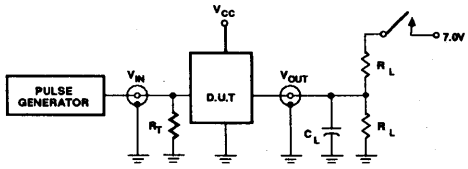
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

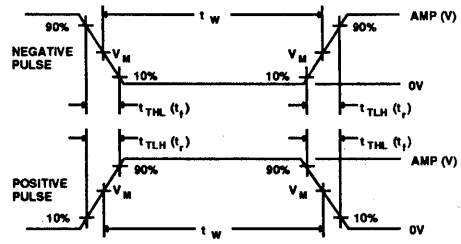
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F621, 74F622
Transceivers

FAST Products

74F621 Octal Bus Transceiver, Non-Inverting (Open Collector)
74F622 Octal Bus Transceiver, Inverting (Open Collector)
Product Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Octal bidirectional bus interface**
- **Open collector outputs sink 64mA and source 15mA**
- **-'F621 Non-Inverting**
  -'F622 Inverting

DESCRIPTION

The 74F621 is an octal bus transceiver featuring non-inverting open collector bus-compatible outputs in both send and receive directions. The outputs are capable of sinking 64mA and sourcing up to 15mA, providing very good capacitive drive characteristics. The 74F622 is a inverting version of the 74F621. These octal bus transceivers are designed for asynchronous two-way communication between data busses. The control function implementation allows for maximum flexibilty in timing. These devices allow data transmission from the A bus to the B bus or from B bus to A bus, depending upon the logic levels at the Enable inputs ($\overline{OEBA}$ and OEAB). The Enable inputs can be used to disable the device so that the busses are effectively isolated. The dual-enable configuration gives the 'F621 and 'F622 the capability to store data by the simultaneous enabling of $\overline{OEBA}$ and OEAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F621	8.0ns	105mA
74F622	8.5ns	53mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F621N, N74F622N
20-Pin Plastic SOL[1]	N74F621D, N74F622D

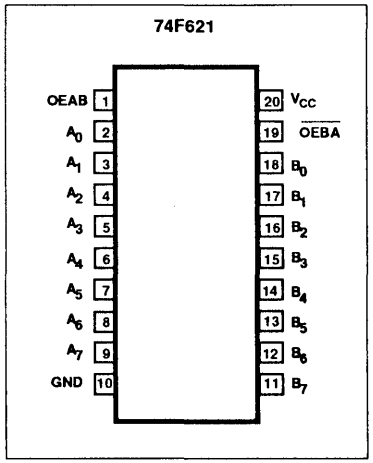
NOTE:
1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal considerations for suface mounted device.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

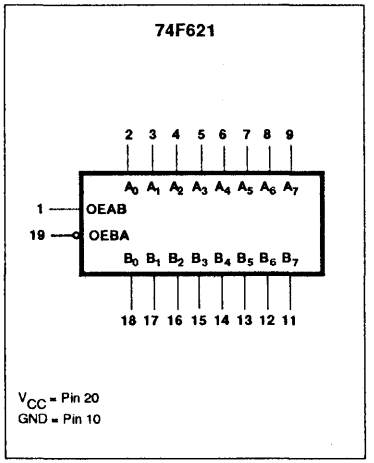
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7, B_0- B_7	Data inputs	1.0/0.033	20μA/20μA
$\overline{OEBA}$, OEAB	Output Enable inputs	1.0/0.033	20μA/20μA
A_0- A_7	Data outputs	OC/40	OC /24mA
B_0- B_7	Data outputs	OC/106.7	OC/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC=Open Collector

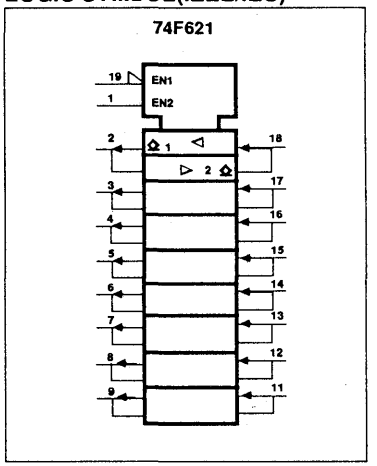
PIN CONFIGURATION



LOGIC SYMBOL

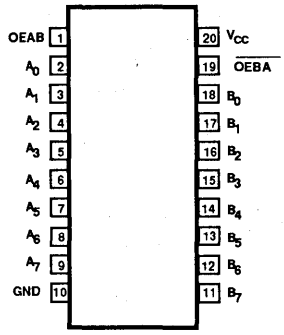


LOGIC SYMBOL(IEEE/IEC)



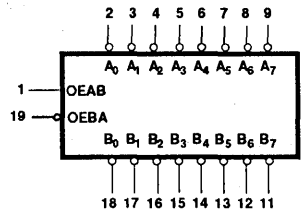
PIN CONFIGURATION

74F622



LOGIC SYMBOL

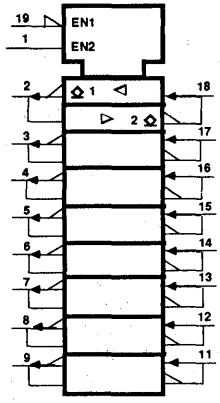
74F622



V_{CC} = Pin 20
GND = Pin 10

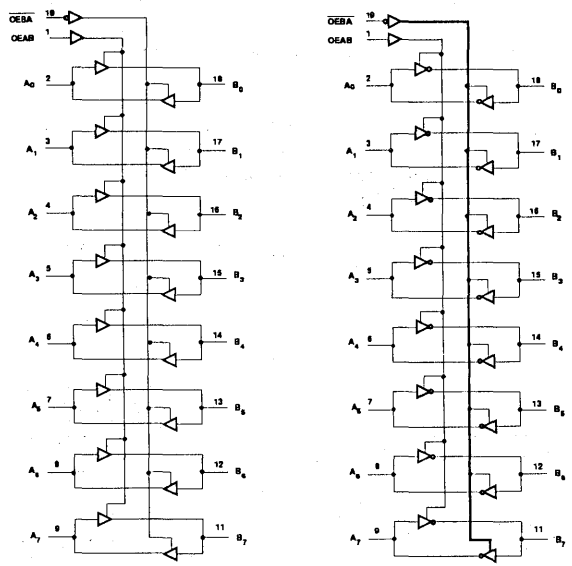
LOGIC SYMBOL(IEEE/IEC)

74F622



LOGIC DIAGRAM

74F621 74F622



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE

INPUTS		OPERATING MODES	
$\overline{OEBA}$	OEAB	74F621	74F622
L	L	B data to A bus	$\overline{B}$ data to A bus
H	H	A data to B bus	$\overline{A}$ data to B bus
H	L	OFF	OFF
L	H	B data to A bus	$\overline{B}$ data to A bus
		A data to B bus	$\overline{A}$ data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
OFF= High if pull-up resistor is connected to open collector output

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0 - A_7	48	mA
		B_0 - B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
V_{OH}	High-level output voltage				4.5	V
I_{OL}	Low-level output current	A_0 - A_7			24	mA
		B_0 - B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEAB}$, $\overline{OEBA}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		others	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{CC}	Supply current (total)	'F621	I_{CCH}	V_{CC} = MAX	$\overline{OEBA}$=OEAB=A_0-A_7=4.5V		105	140	mA
			I_{CCL}		$\overline{OEBA}$=OEAB=4.5V, A_0-A_7=GND		105	140	mA
		'F622	I_{CCH}		$\overline{OEBA}$=OEAB=4.5V, A_0-A_7=GND		37	48	mA
			I_{CCL}		$\overline{OEBA}$=OEAB=A_0-A_7=4.5V		68	90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

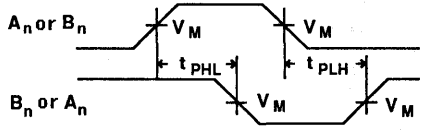
AC ELECTRICAL CHARACTERISTICS for 74F621

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	6.0 4.0	9.5 6.0	12.0 8.0	5.5 3.5	13.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	6.0 3.5	9.0 5.5	12.0 7.5	5.5 3.0	12.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OEBA}$ to A_n	Waveform 3	6.0 3.5	10.0 6.5	13.5 10.5	5.5 3.0	14.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay OEAB to B_n	Waveform 4	7.0 3.5	12.0 6.5	15.0 9.5	6.0 3.0	17.0 10.0	ns

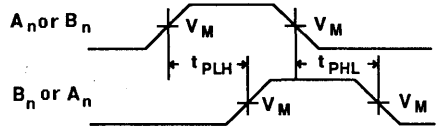
AC ELECTRICAL CHARACTERISTICS for 74F622

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	8.0 1.5	11.0 4.0	12.5 5.5	8.0 1.5	13.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	7.5 1.5	10.0 3.5	12.0 5.0	7.5 1.5	12.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OEBA}$ to A_n	Waveform 3	8.0 6.0	10.5 8.0	12.0 10.0	8.0 6.0	12.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay OEAB to B_n	Waveform 4	10.0 5.0	12.5 7.5	14.5 9.0	10.0 5.0	15.5 9.5	ns

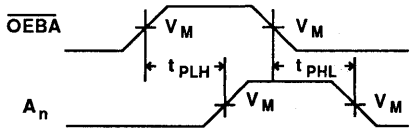
AC WAVEFORMS



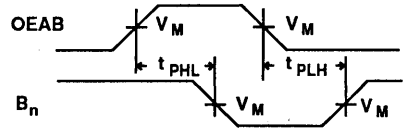
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



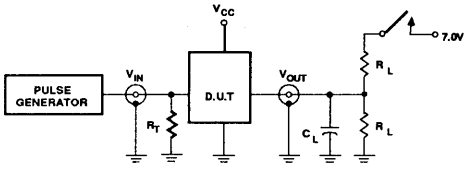
Waveform 3. Propagation delay, $\overline{OEBA}$ to An



Waveform 4. Propagation delay, OEAB to Bn

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

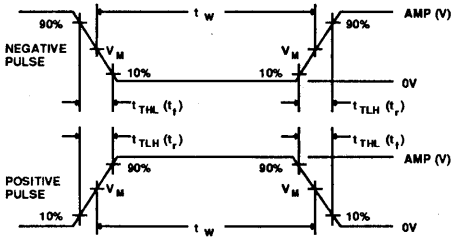
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F640
Transceiver

FAST Products

Octal Bus Transceiver , Inverting (3-State)
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F640	3.5ns	78mA

FEATURES

- **High-impedance NPN base inputs for reduced loading (70μA in High and Low states)**
- **Ideal for applications which require high-output drive and minimal bus loading**
- **Inverting version of 'F245**
- **Octal bidirectional bus interface**
- **3-state buffer outputs sink 64mA and source 15mA**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F640N
20-Pin Plastic SOL	N74F640D

DESCRIPTION

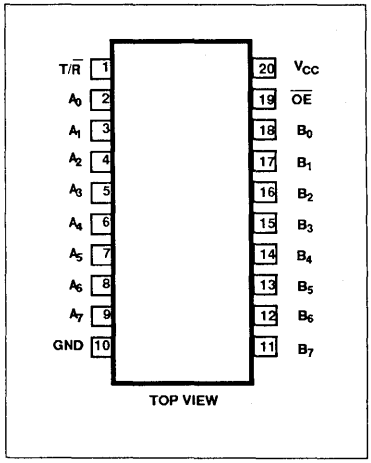
The 74F640 is an octal transceiver featuring inverting 3-state bus compatible outputs in both transmit and receive directions. The B port outputs are capable of sinking 64mA and sourcing 15mA, providing very good capacitive drive characteristics.The device features an Output Enable ($\overline{OE}$) input for easy cascading and Transmit/Receive($T/\overline{R}$) input for direction control. The 3-state outputs, B_0-B_7, have been designed to prevent output bus loading if the power is removed from the device.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

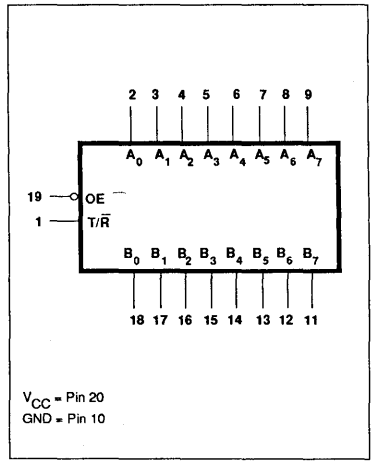
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7, B_0- B_7	Data inputs	3.5/0.115	70μA/70μA
$\overline{OE}$	Output enable input (active Low)	2.0/0.067	40μA/40μA
$T/\overline{R}$	Transmit/Receive input	2.0/0.067	40μA/40μA
A_0- A_7	A port outputs	150/40	3.0mA/24mA
B_0- B_7	B Port outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

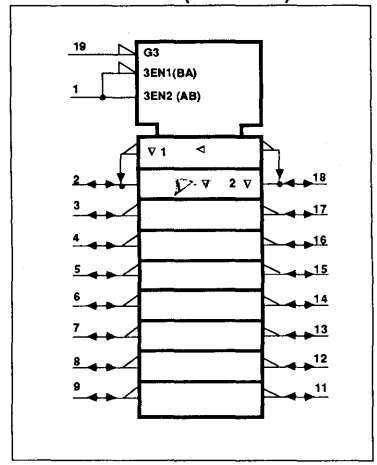
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

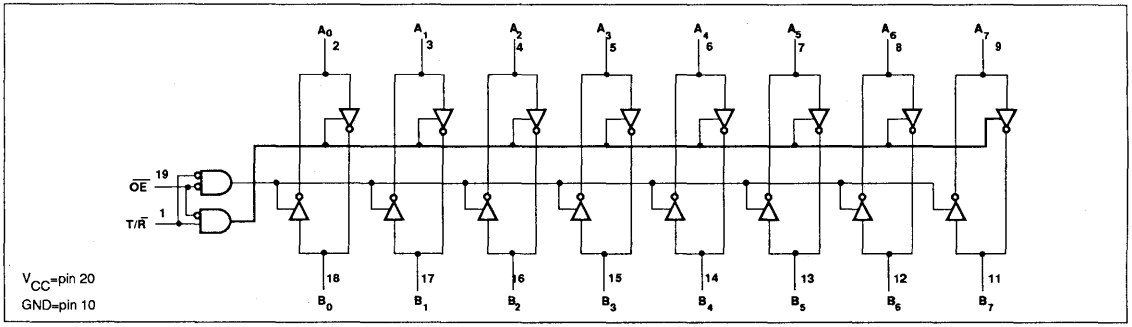


FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B data to Bus $\overline{A}$
L	H	Bus A data to Bus $\overline{B}$
H	X	Z

H=High voltage level
L=Low voltage level
X=Don't care
Z=High impedance "off " state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0-B_7			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	A_0-A_7, B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
		B_0-B_7		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = 5.5V, V_I =5.5V					1.0	mA
I_{IH}	High-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 2.7V					40	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-40	µA
I_{OZH} +I_{IH}	Off state output current, High-level voltage applied		V_{CC} = MAX, V_I = 2.7V					70	µA
I_{OZL}+I_{IL}	Off state output current, Low-level voltage applied		V_{CC} = MAX, V_I = 0.5V					-70	µA
I_{OS}	Short circuit output current[3]	A_0-A_7	V_{CC} = MAX			-60		-150	mA
		B_0-B_7				-100		-225	µA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	T/$\overline{R}$=A_n=4.5V, $\overline{OE}$=GND			66	85	mA
		I_{CCL}		T/$\overline{R}$=B_n=$\overline{OE}$=GND			91	120	mA
		I_{CCZ}		T/$\overline{R}$=B_n=GND, $\overline{OE}$=4.5V			78	102	mA

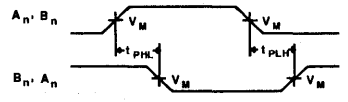
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

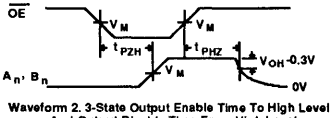
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	Waveform 1	2.0 1.0	4.5 2.5	7.0 5.0	2.0 1.0	8.0 5.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	6.0 6.0	9.0 9.0	11.0 11.0	6.0 6.0	13.0 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 2 Waveform 3	2.5 2.0	5.5 4.5	8.0 7.0	2.5 2.0	9.0 7.5	ns

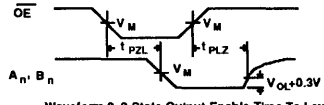
AC WAVEFORMS



Waveform 1. Propagation Delay For Inverting Outputs



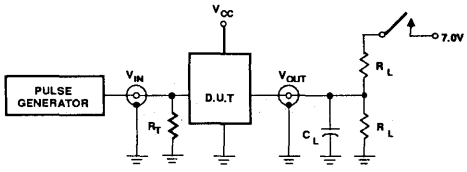
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

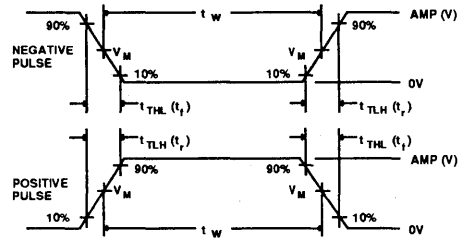
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F641, 74F642
Transceivers

FAST Products

74F641 Octal Bus Transceiver With Common Output Enable, Non-Inverting (Open Collector)
74F642 Octal Bus Transceiver With Common Output Enable, Inverting (Open Collector)
Product Specification

FEATURES

- High impedance NPN base inputs for reduced loading (20μA in High and Low states)
- Octal bidirectional bus interface
- Common Output Enable for both Transmit and Receive modes
- Open collector outputs sink 64mA
- -'F641 Non-Inverting
  -'F642 Inverting

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F641	8.0ns	69mA
74F642	8.5ns	52mA

ORDERING INFORMATION

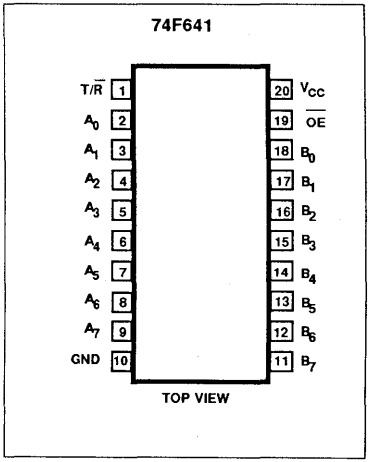
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F641N, N74F642N
20-Pin Plastic SOL	N74F641D, N74F642D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

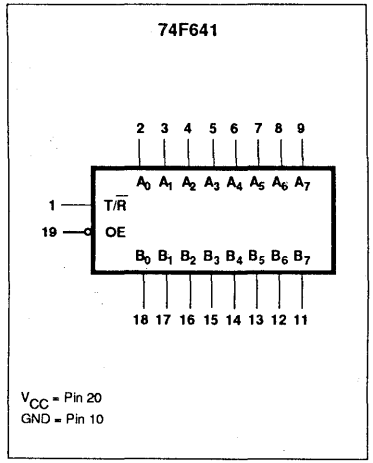
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7, B_0- B_7	Data inputs	1.0/0.033	20μA/20μA
T/$\overline{R}$	Transmit / Receive input	2.0/0.067	40μA/40μA
$\overline{OE}$	Output Enable inputs	2.0/0.067	40μA/40μA
A_0- A_7	Data outputs	OC/40	OC /24mA
B_0- B_7	Data outputs	OC/106.7	OC/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC=Open Collector

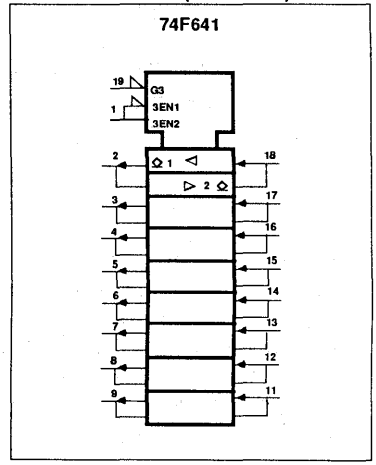
PIN CONFIGURATION



LOGIC SYMBOL

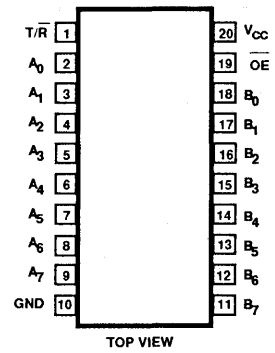


LOGIC SYMBOL(IEEE/IEC)



PIN CONFIGURATION

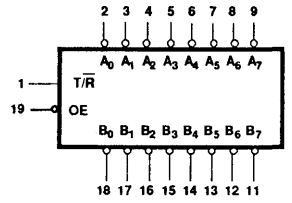
74F642



TOP VIEW

LOGIC SYMBOL

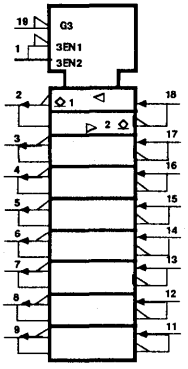
74F642



V_{CC} = Pin 20
GND = Pin 10

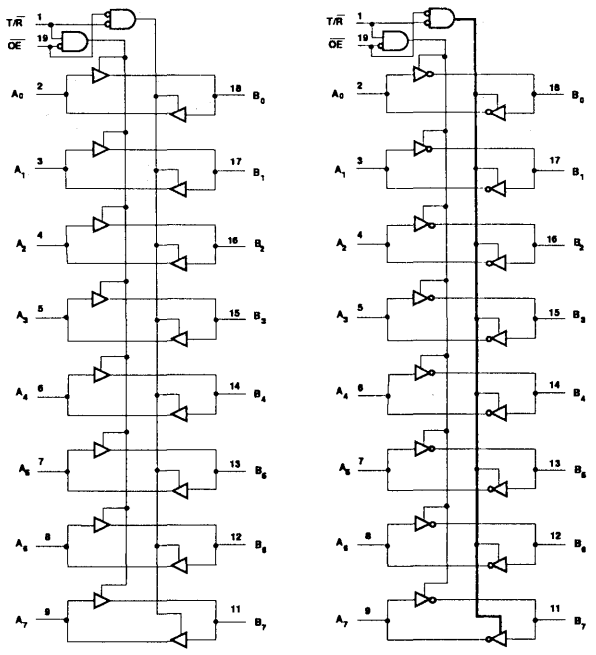
LOGIC SYMBOL(IEEE/IEC)

74F642



LOGIC DIAGRAM

74F641 | 74F642



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE 'F641

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	T/$\overline{R}$	A_n	B_n
L	L	A=B	INPUTS
L	H	INPUTS	B=A
H	X	OFF	OFF

H = High voltage level
L = Low voltage level
X = Don't care
OFF= High if pull-up resistor is connected to open collector output

FUNCTION TABLE 'F642

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	T/$\overline{R}$	A_n	B_n
L	L	A=$\overline{B}$	INPUTS
L	H	INPUTS	B=$\overline{A}$
H	X	OFF	OFF

H = High voltage level
L = Low voltage level
X = Don't care
OFF= High if pull-up resistor is connected to open collector output

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A_0 - A_7	48	mA
		B_0 - B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
V_{OH}	High-level output voltage				4.5	V
I_{OL}	Low-level output current	A_0 - A_7			24	mA
		B_0 - B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	T/$\overline{R}$, $\overline{OE}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_n, B_n	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	T/$\overline{R}$, $\overline{OE}$	V_{CC} = MAX, V_I = 2.7V					40	µA
		A_n, B_n						20	µA
I_{IL}	Low-level input current	T/$\overline{R}$, $\overline{OE}$	V_{CC} = MAX, V_I = 0.5V					-40	µA
		A_n, B_n						-20	µA
I_{CC}	Supply current (total)	'F641 I_{CCH}	V_{CC} = MAX	A_n=T/$\overline{R}$=4.5V, $\overline{OE}$=GND			60	90	mA
		'F641 I_{CCL}		T/$\overline{R}$=4.5V, A_n=$\overline{OE}$=GND			78	120	mA
		'F642 I_{CCH}		A_n=T/$\overline{R}$=$\overline{OE}$=4.5V			37	55	mA
		'F642 I_{CCL}		A_n=T/$\overline{R}$=4.5V, $\overline{OE}$=GND			67	98	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

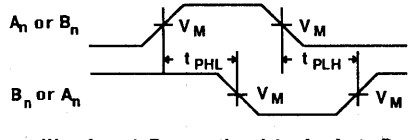
AC ELECTRICAL CHARACTERISTICS for 74F641

SYMBOL	PARAMETER	TEST CONDITION	LIMITS: T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			LIMITS: T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	7.5 4.0	10.0 6.0	12.5 9.5	7.5 4.0	13.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	6.0 3.5	9.5 5.5	12.0 7.5	6.0 3.5	12.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to A_n	Waveform 4	7.0 5.0	10.5 7.0	12.5 9.0	7.0 5.0	13.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to B_n	Waveform 4	9.0 5.5	10.5 7.5	12.5 9.5	9.0 5.5	13.5 10.5	ns

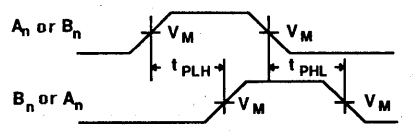
AC ELECTRICAL CHARACTERISTICS for 74F642

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	9.0 2.0	11.5 4.5	13.5 6.5	9.0 2.0	14.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	8.5 1.5	10.5 4.0	12.5 6.0	8.5 1.5	13.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to A_n	Waveform 3	8.5 6.0	10.5 8.0	12.5 10.5	8.5 6.0	13.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to B_n	Waveform 3	9.0 6.5	11.5 9.0	13.5 11.0	9.0 6.5	14.0 11.5	ns

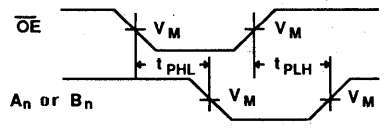
AC WAVEFORMS



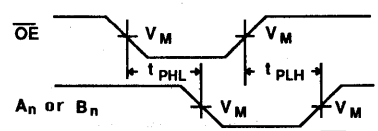
Waveform 1. Propagation delay for An to Bn or Bn to An ('F642)



Waveform 2. Propagation delay for An to Bn or Bn to An ('F641)



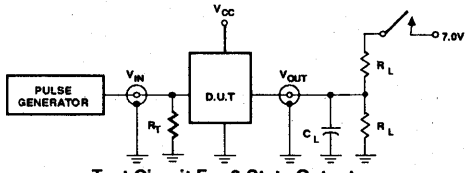
Waveform 3. Propagation delay for $\overline{OE}$ to An or Bn Outputs ('F642) (Bn or An inputs in High state)



Waveform 4. Propagation delay for $\overline{OE}$ to An or Bn Outputs ('F641) (Bn or An inputs in Low state)

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

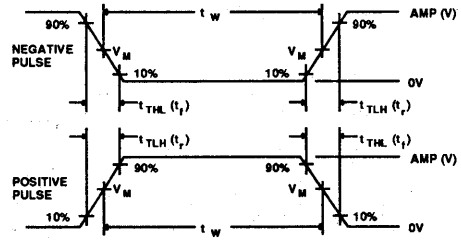
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F646, 74F646A 74F648, 74F648A Transceivers/Registers

74F646/646A Octal Transceiver/Register, Non-Inverting (3-State)
74F648/648A Octal Transceivers/Register, Inverting (3-State)
Preliminary Specification for 74F646A and 74F648A
Product Specification for 74F646 and 74F648

FEATURES

- **Combines 'F245 and 'F374 type functions in one chip**
- **High impedance base inputs for reduced loading (70µA in High and Low states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **Controlled ramp outputs for 'F646A/'F648A**
- **3-state outputs**
- **300 mil wide 24-pin Slim Dip package**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F646/648	115MHz	140mA
74F646A/648A	115MHz	120mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F646N, N74F646AN, N74F648N, N74F648AN
24-Pin Plastic SOL[1]	N74F646D, N74F646AD, N74F648D, N74F648AD

NOTE 1: Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

DESCRIPTION

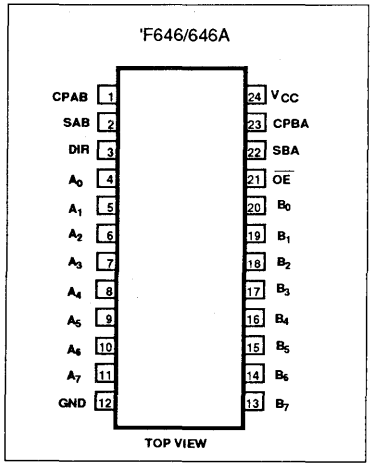
The 74F646/646A and 74F648/648A Transceivers/Registers consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will clocked into the registers as the appropriate clock pin goes High. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

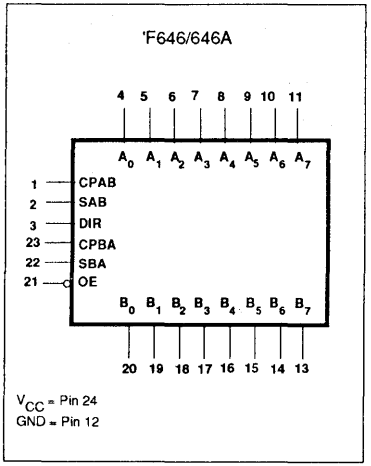
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7, B_0 - B_7	A and B inputs for 'F646/'F648	3.5/0.166	70µA/70µA
A_0 - A_7, B_0 - B_7	A and B inputs for 'F646A/'F648A	1.0/0.033	20µA/20µA
CPAB	A-to-B clock input	1.0/0.033	20µA/20µA
CPBA	B-to-A clock input	1.0/0.033	20µA/20µA
SAB	A-to-B select input	1.0/0.033	20µA/20µA
SBA	B-to-A select input	1.0/0.033	20µA/20µA
DIR	Data flow Directional control enable input	1.0/0.033	20µA/20µA
$\overline{OE}$	Output Enable input	1.0/0.033	20µA/20µA
A_0 - A_7	A outputs	750/106.7	15mA/64mA
B_0 - B_7	B outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

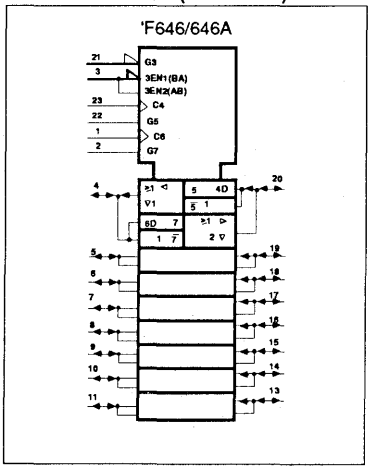
PIN CONFIGURATION



LOGIC SYMBOL

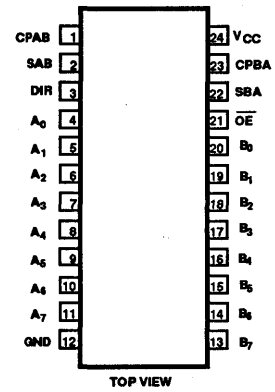


LOGIC SYMBOL(IEEE/IEC)



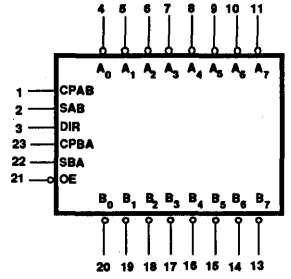
PIN CONFIGURATION

'F648/648A



LOGIC SYMBOL

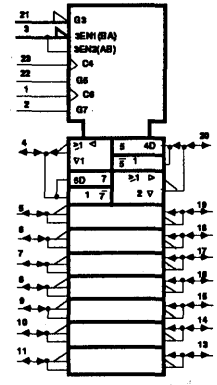
'F648/648A



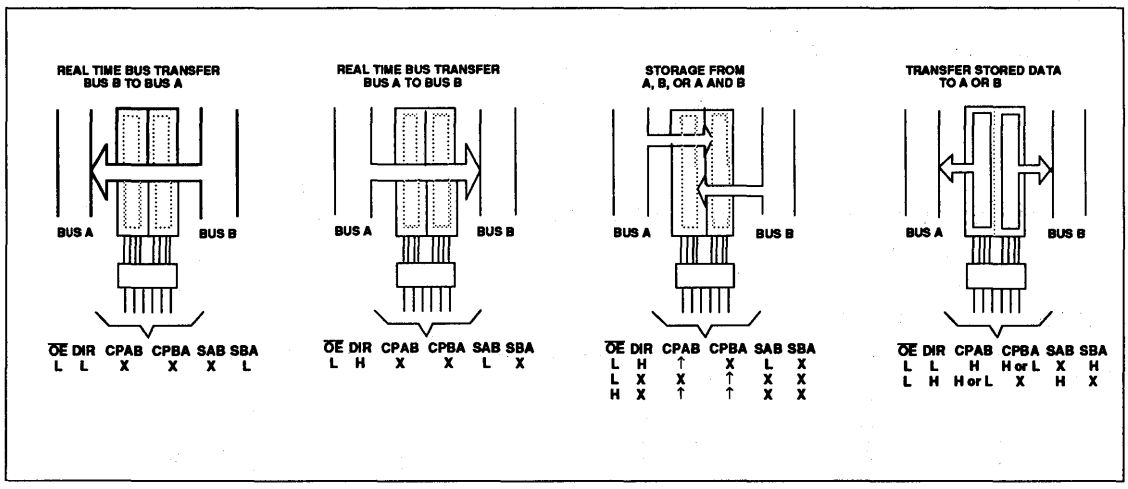
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

'F648/648A



The select (SAB, SBA) pins determine whether data is stored or transfered through the device in real-time. The DIR determines which bus will receive data when the $\overline{OE}$ is active Low. In the isolation mode ($\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two busses , A or B may be driven at a time. The following examples demonstrates the four fundamental bus-management functions that can be performed with the 'F646/646A and 'F648/648A.

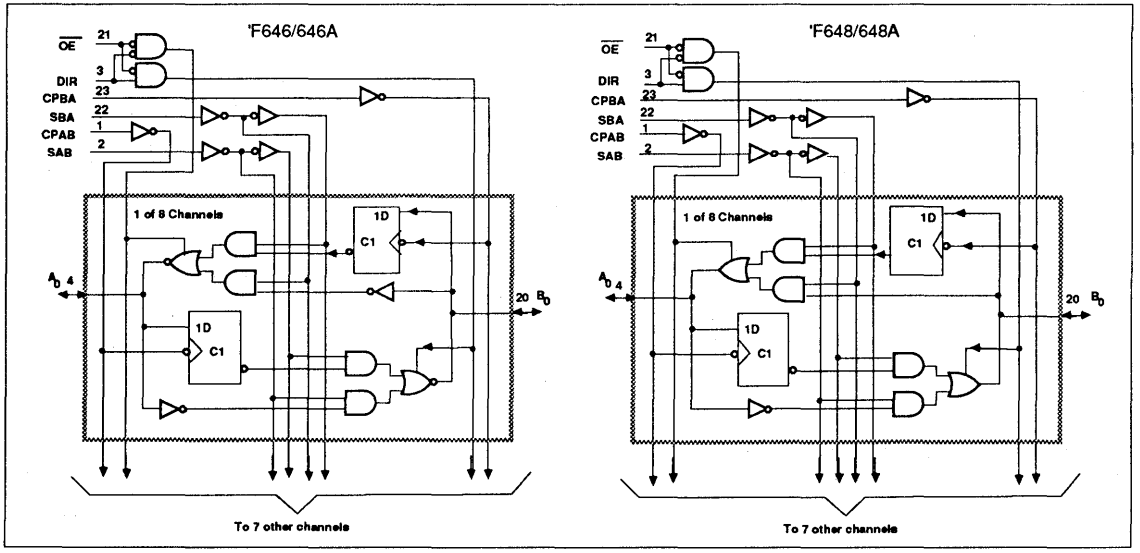


FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	A_0-A_7	B_0-B_7	'F646/646A	'F648/648A
X	X	↑	X	X	X	Input	Unspecified*	Store A, B unspecified*	Store A, B unspecified*
X	X	X	↑	X	X	Unspecified*	Input	Store B, A unspecified*	Store B, A unspecified*
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus	Real time $\overline{B}$ data to A bus Stored $\overline{B}$ data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus	Real time $\overline{A}$ data to B bus Stored $\overline{A}$ data to B bus

H= High voltage level
L= Low voltage level
X=Don't care
↑ =Low-to-High clock transition
*= The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enable, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH}=-15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = MAX, V_I = 5.5V					1	mA
I_{IH}	High-level input current	$\overline{OE}$, DIR CPAB, CPBA SAB, SBA	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OZH} + I_{IH}	Off-state output current, High-level voltage applied	A_0-A_7, B_0-B_7	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZH} + I_{IL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-70	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F646 'F648	I_{CCH}	V_{CC} = MAX			125	165	mA
			I_{CCL}				160	210	mA
			I_{CCZ}				135	160	mA
		'F646A 'F648A	I_{CCH}				110	145	mA
			I_{CCL}				120	155	mA
			I_{CCZ}				130	170	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 74F646

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.5 5.5	7.5 8.0	10.0 10.0	5.0 5.0	11.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2,3	4.0 4.0	6.0 6.5	9.0 9.0	4.0 4.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2,3	5.0 5.0	7.0 6.5	8.5 8.5	4.5 4.5	10.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	5.0 6.5	7.0 8.5	10.0 11.0	4.5 6.0	11.0 12.5	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	Waveform 5 Waveform 6	4.5 6.0	6.5 8.5	9.0 11.0	4.0 5.5	10.0 12.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	6.5 6.5	9.0 9.0	11.5 11.5	6.0 6.0	12.5 13.5	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to A_n or B_n	Waveform 5 Waveform 6	5.5 5.5	8.5 8.5	11.0 11.0	4.5 5.0	13.0 12.5	ns

AC SETUP REQUIREMENTS for 74F646

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.0 6.0			4.0 6.0		ns

AC ELECTRICAL CHARACTERISTICS for 74F648

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.0 5.0	7.0 7.5	9.5 9.5	4.5 4.5	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2,3	3.0 4.0	6.0 6.0	8.5 8.5	2.5 3.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2,3	4.5 4.5	7.0 6.5	8.5 8.5	4.5 4.5	10.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	4.5 6.0	7.0 8.5	10.0 11.0	4.5 5.5	11.0 12.5	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	Waveform 5 Waveform 6	4.5 6.0	7.0 8.5	10.0 11.0	4.0 5.5	11.0 12.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	6.0 6.0	9.0 8.5	11.5 12.0	6.0 6.0	12.5 13.5	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to A_n or B_n	Waveform 5 Waveform 6	5.0 6.0	9.0 9.0	12.5 12.5	4.5 5.0	14.0 14.0	ns

AC SETUP REQUIREMENTS for 74F648

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.0 4.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	3.5 6.5			4.0 7.0		ns

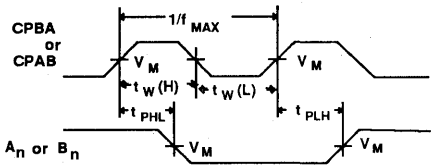
AC ELECTRICAL CHARACTERISTICS for 74F646A/74F648A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	3.0 3.0	4.0 4.5	8.0 8.0	4.5 4.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2,3	2.0 2.0	3.5 3.0	7.5 7.5	2.5 2.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2,3	2.0 2.0	3.5 3.0	7.5 7.5	4.5 4.5	9.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	2.0 2.0	3.0 3.0	7.0 7.0	4.5 4.5	8.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	Waveform 5 Waveform 6	2.0 2.0	3.0 3.0	7.0 7.0	4.0 4.0	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	2.0 2.0	3.0 3.0	7.0 7.0	5.0 5.0	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to A_n or B_n	Waveform 5 Waveform 6	2.0 2.0	3.0 3.0	7.0 7.0	4.0 4.0	8.5 8.5	ns

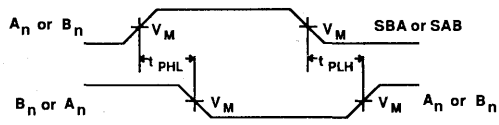
AC SETUP REQUIREMENTS for 74F646A/74F648A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.5 4.5			5.0 5.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.0 6.0			4.0 6.0		ns

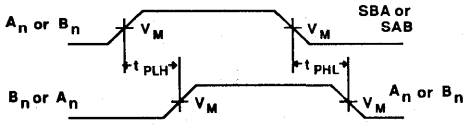
AC WAVEFORMS



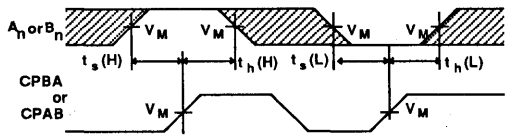
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



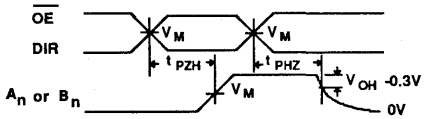
Waveform 2. Propagation Delay, An to Bn or Bn to An and SBA or SAB to An or Bn



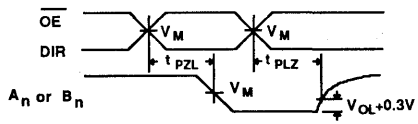
Waveform 3. Propagation Delay, An to Bn or Bn to An and SBA or SAB to An or Bn



Waveform 4. Data Setup And Hold Times



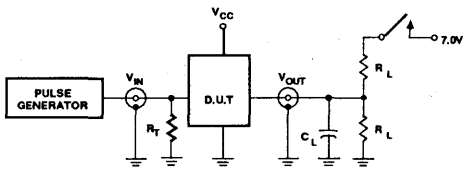
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

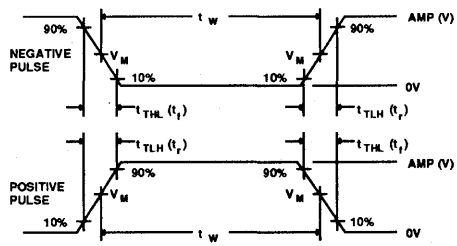
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F647, 74F649 Transceivers/Registers

74F647 Octal Transceiver/Register, Non-Inverting (Open Collector)
74F649 Octal Transceivers/Register, Inverting (Open Collector)
Product Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **Open Collector outputs**
- **300 mil wide 24-pin Slim Dip package**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F647	65MHz	125mA
74F649	65MHz	125mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F647N, N74F649N
24-Pin Plastic SOL[1]	N74F647D, N74F649D

NOTE : 1.Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

DESCRIPTION

The 74F647 and 74F649 Transceivers/Registers consist of bus transceiver circuits with open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a High logic level. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both. The select (SAB,SBA) controls can multiplex stored and real-time (transparent mode) data.The DIR determines which bus will receive data when the Output Enable, $\overline{OE}$ is active Low. In the isolation mode (Output Enable, $\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register.

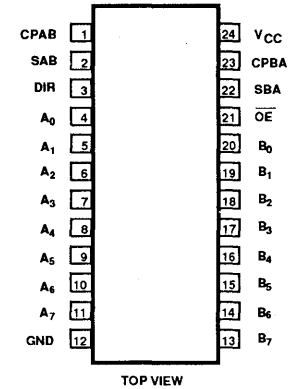
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A inputs	1.0/0.033	20μA/20μA
B_0 - B_7	B inputs	1.0/0.033	20μA/20μA
CPAB	A-to-B clock inputs	1.0/0.033	20μA/20μA
CPBA	B-to-A clock inputs	1.0/0.033	20μA/20μA
SAB	A-to-B select input	1.0/0.033	20μA/20μA
SBA	B-to-A select input	1.0/0.033	20μA/20μA
DIR	Data flow Directional control enable input	1.0/0.033	20μA/20μA
$\overline{OE}$	Output Enable input	1.0/0.033	20μA/20μA
A_0 - A_7	A outputs	OC/106.7	OC/64mA
B_0 - B_7	B outputs	OC/106.7	OC/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC=Open-Collector

PIN CONFIGURATION

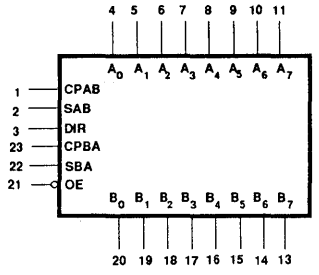
'F647



TOP VIEW

LOGIC SYMBOL

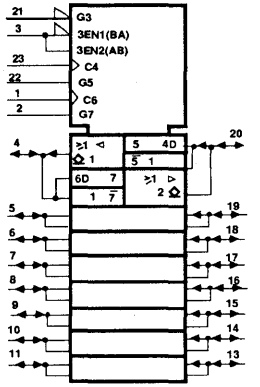
'F647



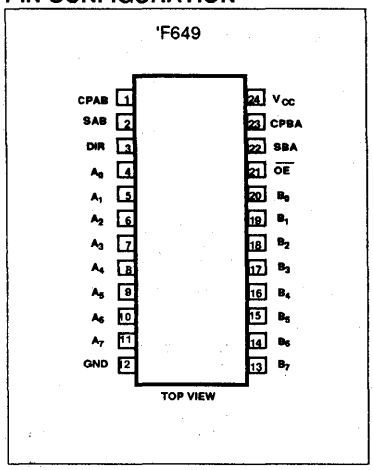
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

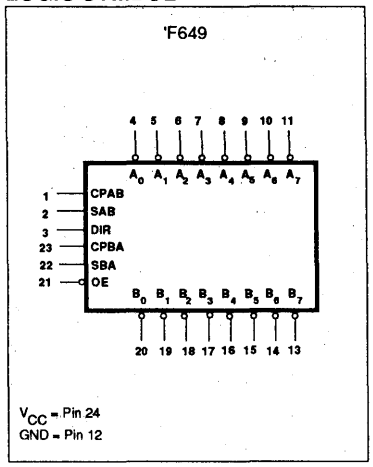
'F647



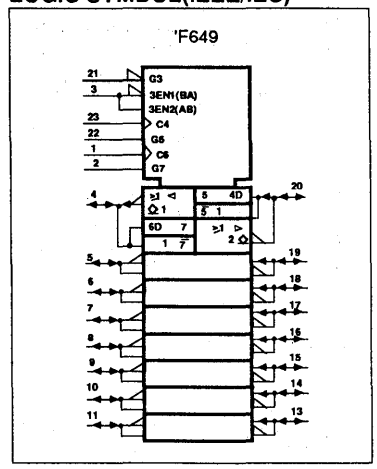
PIN CONFIGURATION



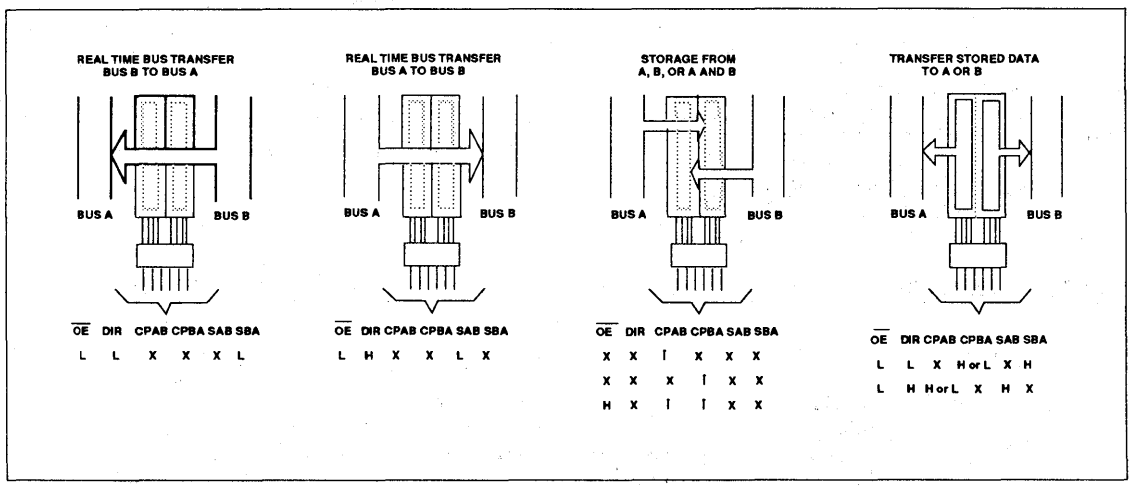
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two busses , A or B, may be driven at a time. The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'F647 and 'F649.

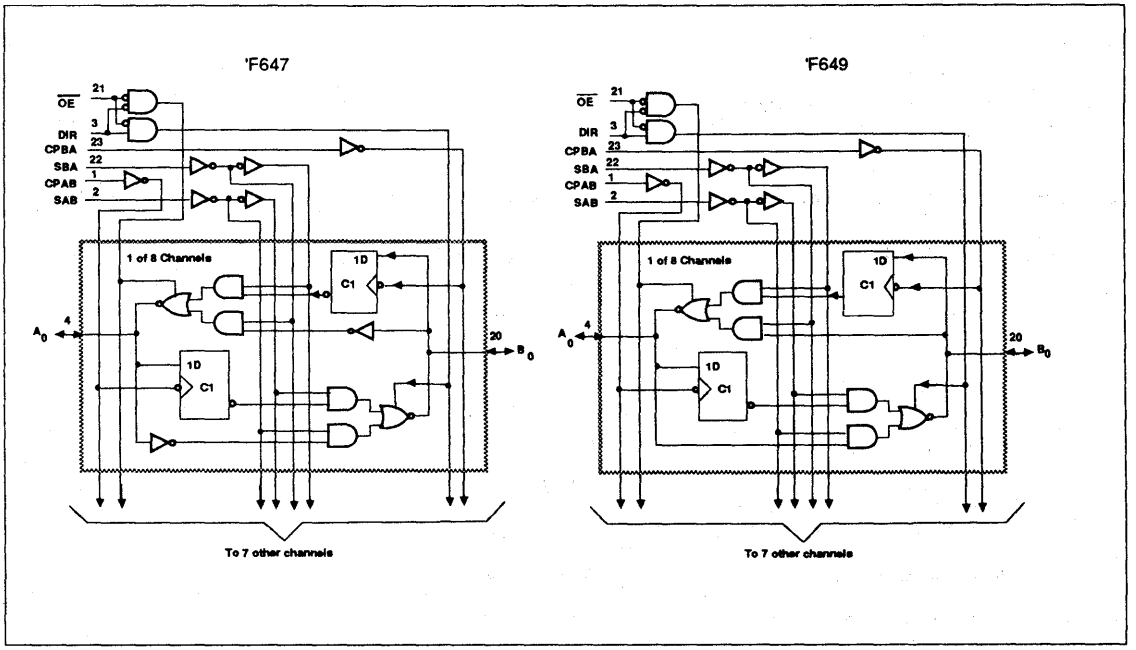


FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	A_0-A_7	B_0-B_7	'647	'649
X	X	↑	X	X	X	Input	Unspecified*	Store A, B unspecified*	Store A, B unspecified*
X	X	X	↑	X	X	Unspecified*	Input	Store A, B unspecified*	Store A, B unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B data	Store A and B data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real time B data to A bus	Real time B data to A bus
L	L	X	H or L	X	H			Stored B data to A bus	Stored B data to A bus
L	H	H or L	X	L	X	Input	Output	Real time A data to B bus	Real time A data to B bus
L	H	X	X	H	X			Stored A data to B bus	Stored A data to B bus

H= High voltage level
L= Low voltage level
X=Don't care
↑ =Low-to-High clock transition
*= The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enable, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} =0.0V, V_I = 7.0V					100	µA
		A_n, B_n	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				105	145	mA
		I_{CCL}					145	200	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

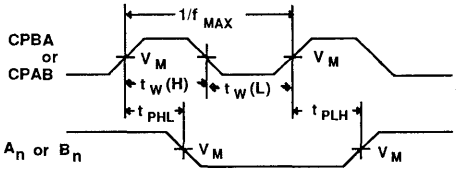
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	50	65		40		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to B_n or CPBA to A_n	Waveform 1	10.0 5.5	15.0 8.5	18.0 11.0	10.0 5.5	19.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 2 Waveform 3	10.5 4.0	13.5 7.0	16.5 9.5	10.5 4.0	19.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay SBA to A_n or SAB to B_n	Waveform 2 Waveform 3	10.5 4.0	14.5 7.0	17.5 9.5	10.5 4.0	20.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to A_n or B_n	Waveform 2 Waveform 3	13.0 6.5	17.0 10.0	20.0 12.5	13.0 6.5	22.5 13.5	ns
t_{PLH} t_{PHL}	Propagation delay DIR to A_n or B_n	Waveform 2 Waveform 3	13.0 7.0	17.0 15.0	20.0 18.0	13.0 7.0	22.5 20.0	ns

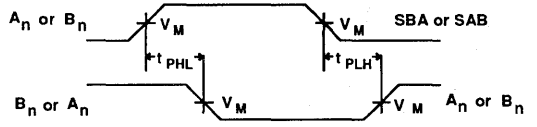
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n to CPBA or B_n to CPAB	Waveform 4	4.0 4.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n to CPBA or B_n to CPAB	Waveform 4	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.5 6.0			4.5 6.5		ns

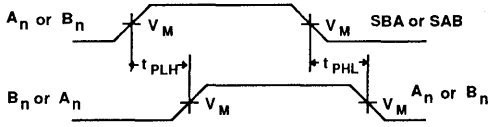
AC WAVEFORMS



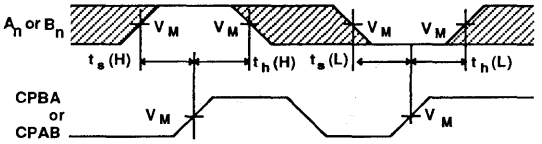
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Propagation Delay, An to Bn or Bn to An and SBA to An or SAB to Bn



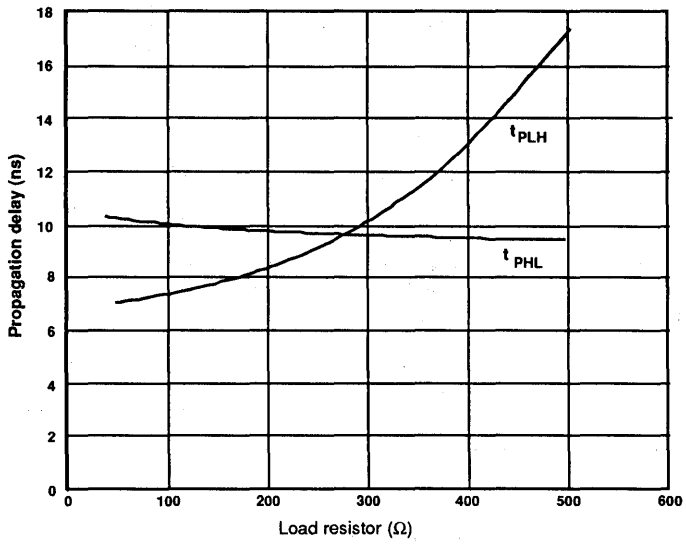
Waveform 3. Propagation Delay, An to Bn or Bn to An and SBA to An or SAB to Bn



Waveform 4. Data Setup And Hold Times

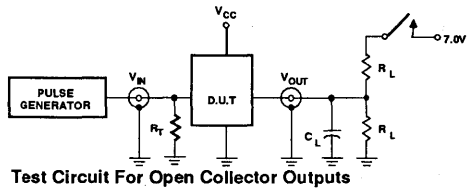
NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs

SWITCH POSITION

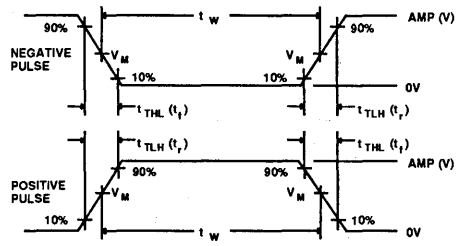
TEST	SWITCH
Open Collector	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F651, 74F651A 74F652, 74F652A Transceivers/Registers

FAST Products

74F651/74F651A Octal Transceiver/Register, Inverting (3-State)
74F652/74F652A Octal Transceiver/Register, Non-Inverting (3-State)
Preliminary Specification for 74F651A and 74F652A
Product Specification for 74F651 and 74F652

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F651/74F652	110MHz	140mA
74F651A/74F652A	110MHz	120mA

FEATURES

- **High impedance base inputs for reduced loading (70µA in High and Low states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **3-state outputs**

DESCRIPTION

The 74F651/74F651A and 74F652/74F652A Transceivers/ Registers consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{OEBA}$) and Select (SAB, SBA) pins are provided for bus management.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim Dip (300mil)	N74F651N, N74F651AN, N74F652N, N74F651AN
24-Pin Plastic SOL[1]	N74F651D, N74F651AD, N74F652D, N74F652AD

NOTE 1:
Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

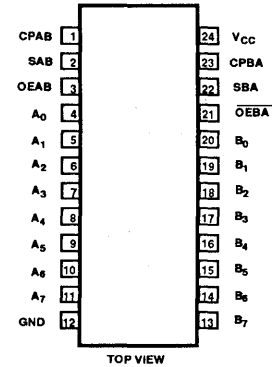
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A inputs	3.5/0.116	70µA/70µA
B_0 - B_7	B inputs	3.5/0.116	70µA/70µA
CPAB	A-to-B clock input	1.0/0.033	20µA/20µA
CPBA	B-to-A clock input	1.0/0.033	20µA/20µA
SAB	A-to-B select input	1.0/0.033	20µA/20µA
SBA	B-to-A select input	1.0/0.033	20µA/20µA
OEAB	A-to-B output enable input	1.0/0.033	20µA/20µA
$\overline{OEBA}$	B-to-A output enable input	1.0/0.033	20µA/20µA
A_0 - A_7	A outputs	750/106.7	15mA/64mA
B_0 - B_7	B outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

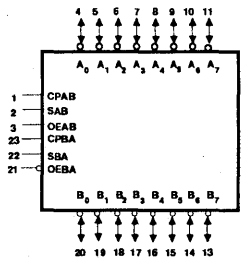
'F651/651A



TOP VIEW

LOGIC SYMBOL

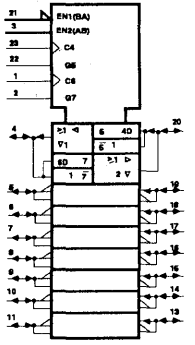
'F651/651A



V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

'F651/651A



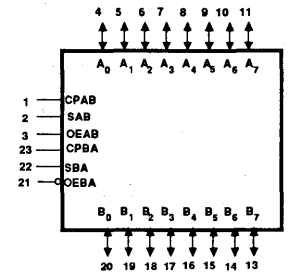
Transceivers/Registers

FAST 74F651, 74F652, 74F651A, 74F652A

The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'F651/651A and 'F652/652A.
The select pins determine whether data is stored or transferred through the device in real time.
The Output Enable pins determine the direction of the data flow.

LOGIC SYMBOL

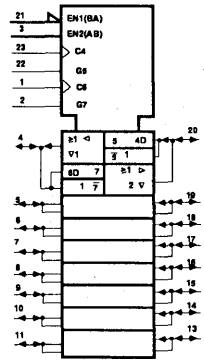
'F652/652A



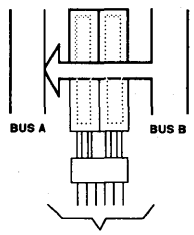
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

'F652/652A

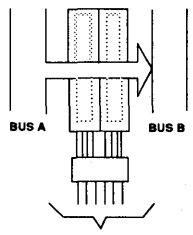


REAL TIME BUS TRANSFER BUS B TO BUS A



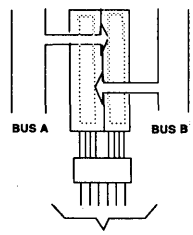
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



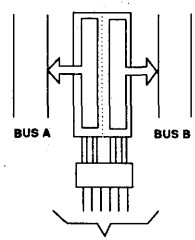
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

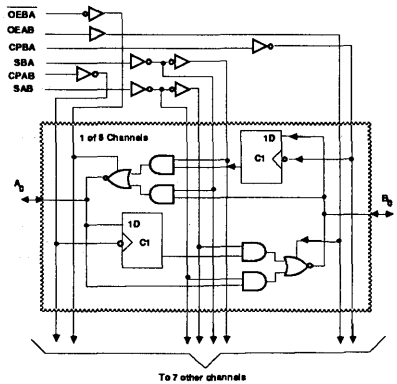
TRANSFER STORED DATA TO A AND/OR B



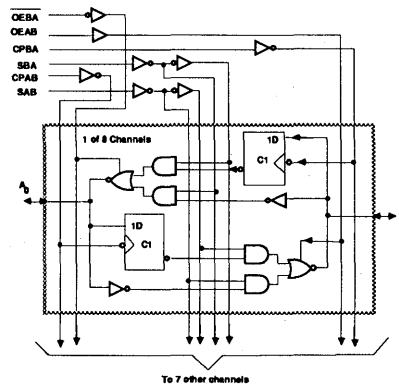
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

LOGIC DIAGRAM

'F651/651A



'F652/652A



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A_n	B_n	'F651/651A	'F652/652A
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B data	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified*	Store A, Hold B	Store A, Hold B
H	H	↑	↑	L	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified*	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	L	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real time $\overline{B}$ data to A bus	Real time B data to A bus
L	L	X	H or L	X	H			Stored $\overline{B}$ data to A bus	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real time $\overline{A}$ data to B bus	Real time A data to B bus
H	H	H or L	X	H	X			Stored $\overline{A}$ data to B bus	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ data to B bus	Stored A data to B bus
								Stored $\overline{B}$ data to A bus	Stored B data to A bus

NOTES:
H= High voltage level
L= Low voltage level
*= The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
↑ =Low-to-High clock transition
X=Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
				I_{OH}=-15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	OEAB, $\overline{OEBA}$, CPAB, CPBA SAB, SBA	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
$I_{IH}+I_{OZH}$	Off-state output current High-level voltage applied	A_0-A_7, B_0-B_7	V_{CC} = MAX, V_I = 2.7V					70	µA
$I_{IL}+I_{OZL}$	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_I = 0.5V					-70	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	74F651 74F652 I_{CCH}	V_{CC} = MAX				110 140[4]	155 185[4]	mA
		74F651 74F652 I_{CCL}					155 165[4]	200 240[4]	mA
		74F651 74F652 I_{CCZ}					130	175	mA
		74F651A 74F652A I_{CCH}					110	145	mA
		74F651A 74F652A I_{CCL}					120	155	mA
		74F651A 74F652A I_{CCZ}					130	170	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. These values are for worst case only. Worst case is defined as all (16) I/O pins selected as outputs. When using worst case conditions thermal mounting is required.

AC ELECTRICAL CHARACTERISTICS for 74F651/74F652

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	90	110		80		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.0 5.5	7.0 7.5	10.5 11.0	4.5 5.0	12.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2,3	3.0 3.0	6.0 6.0	10.0 9.0	2.5 3.0	12.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2,3	4.0 4.0	7.0 6.5	10.0 9.5	4.0 4.0	12.5 10.0	ns
t_{PZH} t_{PZL}	Output Enable time OEAB or $\overline{OEBA}$ to A_n or B_n	Waveform 7 Waveform 8	4.0 6.0	7.0 10.5	10.0 12.0	3.5 5.5	11.0 13.0	ns
t_{PHZ} t_{PLZ}	Output Disable time OEAB or $\overline{OEBA}$ to A_n or B_n	Waveform 7 Waveform 8	4.5 4.5	9.5 9.0	13.0 13.0	4.0 4.0	14.5 15.5	ns

AC SETUP REQUIREMENTS for 74F651/74F652

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.0 4.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low[1] $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	5.0 5.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	0 0			0 0		ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.5 6.5			4.5 6.5		ns

Note: 1.Setup time is to protect against current surge caused by enabling 16 outputs (64mA per output) simultaneously.

AC ELECTRICAL CHARACTERISTICS for 74F651A/74F652A

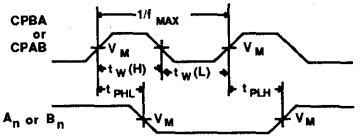
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	90	110		80		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.0 4.5	7.0 6.5	9.5 9.0	4.5 4.0	11.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	Waveform 2,3	2.0 2.0	5.0 4.5	8.0 8.0	2.0 2.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2,3	4.0 4.0	7.0 6.5	9.0 8.5	4.0 4.0	11.5 9.0	ns
t_{PZH} t_{PZL}	Output Enable time OEAB or $\overline{OEBA}$ to A_n or B_n	Waveform 7 Waveform 8	4.0 5.0	7.0 8.5	9.0 10.0	3.5 4.5	10.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time OEAB or $\overline{OEBA}$ to A_n or B_n	Waveform 7 Waveform 8	4.5 4.5	8.0 8.0	9.5 9.5	4.0 4.0	10.5 10.5	ns

AC SETUP REQUIREMENTS for 74F651A/74F652A

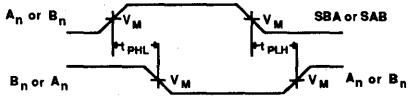
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.0 4.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low[1] $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	5.0 5.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 5, 6	0 0			0 0		ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.5 6.5			4.5 6.5		ns

Note: 1.Setup time is to protect against current surge caused by enabling 16 outputs (64mA per output) simultaneously.

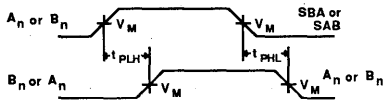
AC WAVEFORMS



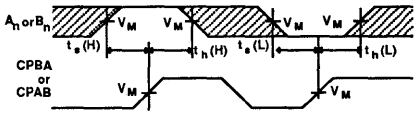
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



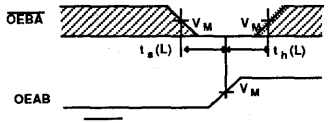
Waveform 2. Propagation Delay, An to Bn or Bn to An and SAB or SBA to An or Bn



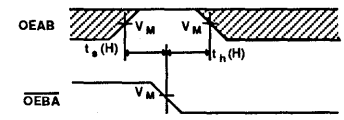
Waveform 3. Propagation Delay, An to Bn or Bn to An and SAB or SBA to An or Bn



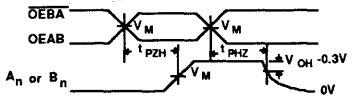
Waveform 4. Data Setup and Hold Times



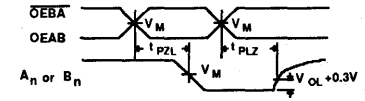
Waveform 5. OEBA to OEAB Setup and Hold Times



Waveform 6. OEAB to OEBA Setup and Hold Times



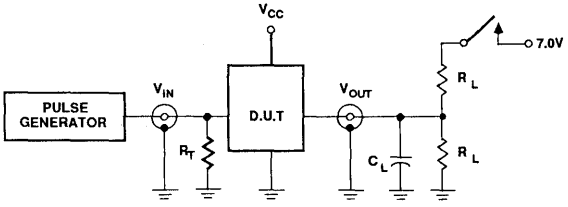
Waveform 7. 3-State Output Enable Time To High Level And Output Disable Time From High Level



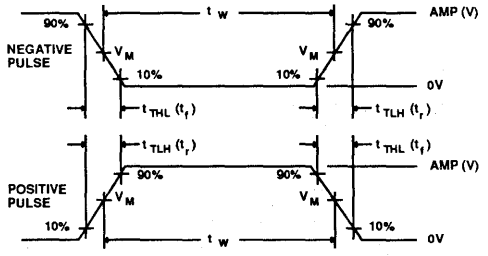
Waveform 8. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F653, 74F654 Transceivers/Registers

'F653 Octal Transceiver/Register, Inverting (3-state +Open Collector)
'F654 Octal Transceiver/Register, Non-Inverting (3-state +Open Collector)

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F653	90MHz	140mA
74F654	90MHz	140mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Cerdip (300mil)	N74F653F, N74F654F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A inputs	1.0/0.033	20µA/20µA
B_0 - B_7	B inputs	3.5/0.116	70µA/70µA
CPAB	A-to-B clock input	1.0/0.033	20µA/20µA
CPBA	B-to-A clock input	1.0/0.033	20µA/20µA
SAB	A-to-B select input	1.0/0.033	20µA/20µA
SBA	B-to-A select input	1.0/0.033	20µA/20µA
OEAB	A-to-B output enable input	1.0/0.033	20µA/20µA
$\overline{OEBA}$	B-to-A output enable input	1.0/0.033	20µA/20µA
A_0 - A_7	A outputs	OC /106.7	OC /64mA
B_0 - B_7	B outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC=Open Collector

FAST Products

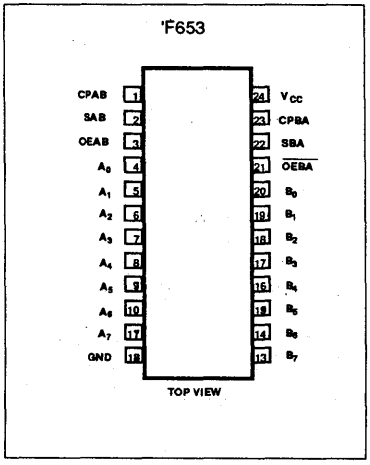
FEATURES

- **High impedance NPN base inputs for redued loading (70µA in High and Low states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **3-state outputs (B_0-B_7) or Open-Collector outputs (A_0-A_7)**

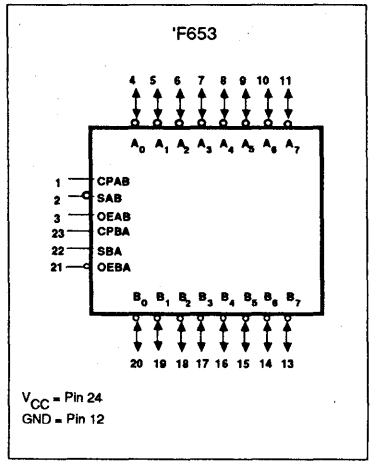
DESCRIPTION

The 74F653 and 74F654 Transceivers/Registers consist of bus transceiver circuits with 3-state (B_0-B_7) or open collector (A_0-A_7)outputs , D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{OEBA}$) and Select (SAB, SBA) pins are provided for bus management.

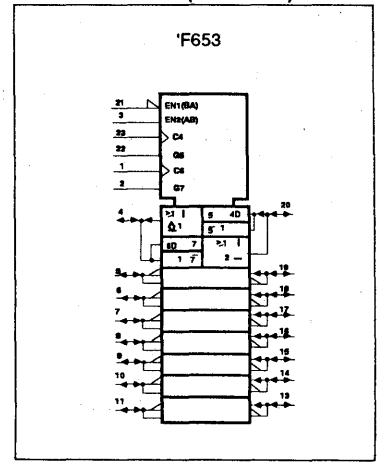
PIN CONFIGURATION



LOGIC SYMBOL

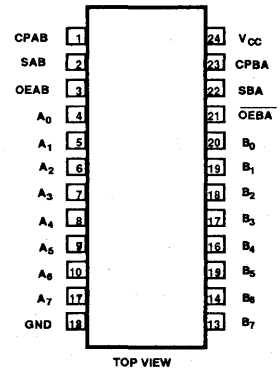


LOGIC SYMBOL(IEEE/IEC)



PIN CONFIGURATION

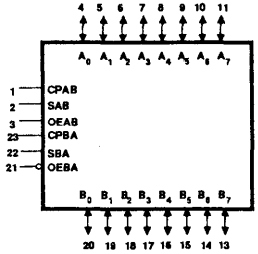
'F654



TOP VIEW

LOGIC SYMBOL

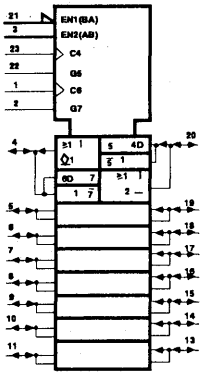
'F654



V_{CC} = Pin 24
GND = Pin 12

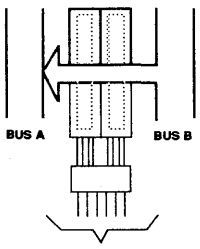
LOGIC SYMBOL(IEEE/IEC)

'F654



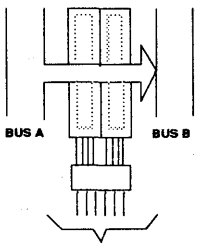
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'F653 and 'F654. The select pins determine whether data is stored or transferred through the device in real time. The output enable pins determine the direction of the data flow.

REAL TIME BUS TRANSFER BUS B TO BUS A



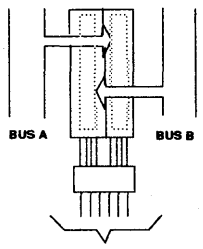
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



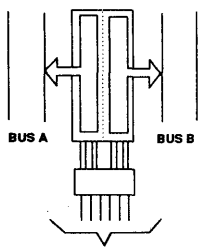
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

TRANSFER STORED DATA TO A AND/OR B



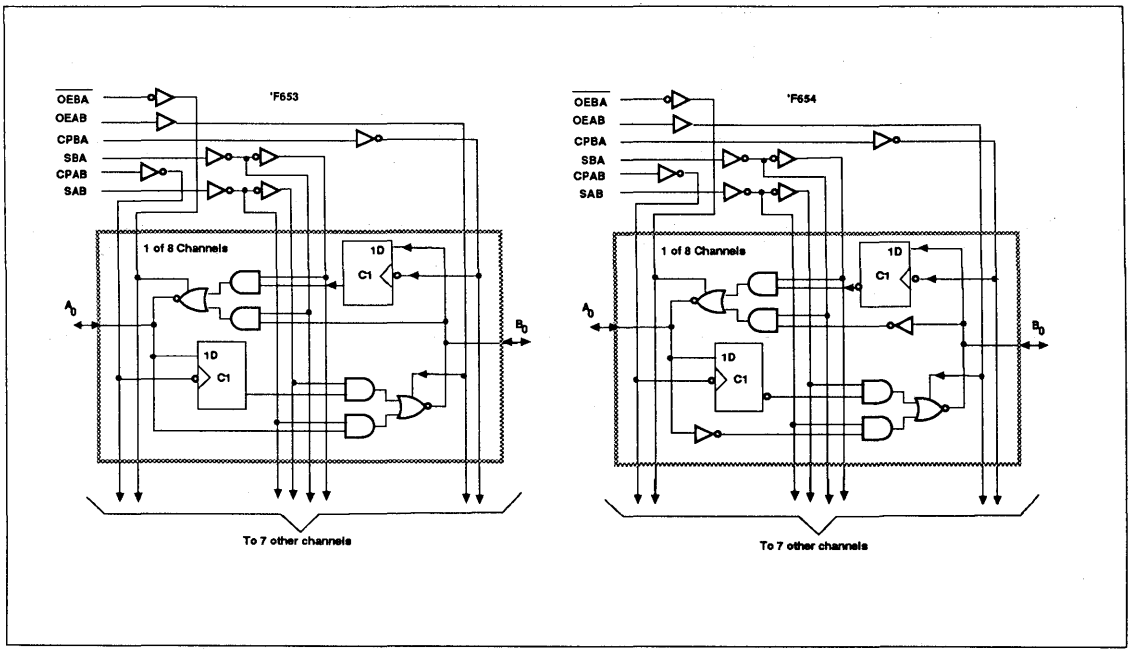
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA
H	L	H or L	H or L	H	H

FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
OEAB	$\overline{OEBA}$	CPAB	CPBA	SAB	SBA	A_n	B_n	'F653	'F654
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B data	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified*	Store A, Hold B	Store A, Hold B
H	H	↑	↑	L	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified*	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	L	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real time $\overline{B}$ data to A bus	Real time B data to A bus
L	L	X	H or L	X	H			Stored $\overline{B}$ data to A bus	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real time $\overline{A}$ data to B bus	Real time A data to B bus
H	H	H or L	X	H	X			Stored $\overline{A}$ data to B bus	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ data to B bus Stored $\overline{B}$ data to A bus	Stored A data to B bus Stored B data to A bus

H= High voltage level
L= Low voltage level
*= The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.
↑ =Low-to-High clock transition
X=Don't care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
V_{OH}	High-level output voltage	A_0 - A_7			4.5	V
I_{OH}	High-level output current	A_0 - A_7			-3	mA
		B_0 - B_7			-15	mA
I_{OL}	Low-level output current				64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
I_{OH}	High-level output current	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OH}	High-level output voltage	B_0-B_7	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
				I_{OH}=-15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	OEAB, $\overline{OEBA}$, CPAB, CPBA SAB, SBA A_0-A_7	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{IH}+I_{OZH}	Off-state current High-level voltage applied	B_0-B_7	V_{CC} = MAX, V_O= 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-70	µA
I_{OS}	Short-circuit output current[3]	B_0-B_7	V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				110 140[4]	160 185[4]	mA
		I_{CCL}					140 160[4]	210 240[4]	mA
		I_{CCZ}					130	175	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. These values are for worst case only. Worst case is defined as all (16) I/O pins selected as outputs. When using worst case conditions thermal mounting is required.

AC ELECTRICAL CHARACTERISTICS

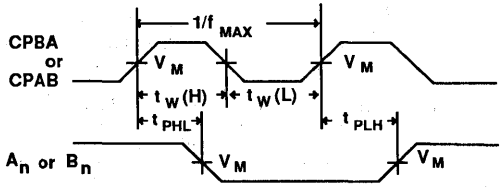
SYMBOL	PARAMETER		TEST CONDITION	74F653, 74F654					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	A_0-A_7	Waveform 1	55	70		45		MHz
		B_0-B_7		100	115		85		
t_{PLH} t_{PHL}	Propagation delay CPBA to A_n		Waveform 1	6.0 6.0	14.5 8.0	19.0 11.0	5.5 5.5	21.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CPAB to B_n		Waveform 1	5.5 5.5	7.5 8.0	10.5 10.5	5.0 5.5	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n		Waveform 3, 4	4.5 4.5	14.0 7.0	18.5 10.0	4.0 4.0	20.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n to B_n		Waveform 3, 4	4.0 4.0	6.0 6.5	9.5 9.5	3.5 4.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SBA to A_n		Waveform 3, 4	5.0 5.0	15.0 7.5	18.5 10.5	4.5 4.5	21.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB to B_n		Waveform 3, 4	5.0 5.0	7.0 7.0	10.0 10.0	4.5 4.5	12.0 10.5	ns
t_{PLH} t_{PHL}	Output Enable and Disable time $\overline{OEBA}$ to A_n		Waveform 2	6.5 6.5	16.0 10.0	20.0 12.5	6.0 6.0	23.0 14.0	ns
t_{PZH} t_{PZL}	Output Enable time OEAB to B_n		Waveform 8 Waveform 9	4.5 6.0	6.5 8.0	9.5 11.0	4.0 5.5	10.0 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time OEAB to B_n		Waveform 8 Waveform 9	6.5 6.0	9.5 9.0	13.0 12.0	6.0 5.5	14.5 14.5	ns

AC SETUP REQUIREMENTS

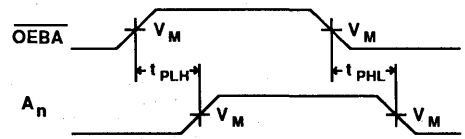
SYMBOL	PARAMETER	TEST CONDITION	74F653, 74F654					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 5	4.5 4.5			5.5 5.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 5	0 0			0 0		ns
t_s(H) t_s(L)	Setup time, High or Low [1] $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 6, 7	5.0 5.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{OEBA}$ to OEAB or OEAB to $\overline{OEBA}$	Waveform 6, 7	0 0			0 0		ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	W aveform 1	4.5 6.5			4.5 6.5		ns

Note : 1. Setup time is to protect against current surge caused by enabling 16 outputs (64mA per output) simultaneously.

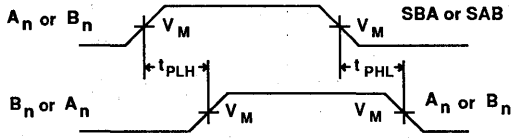
AC WAVEFORMS



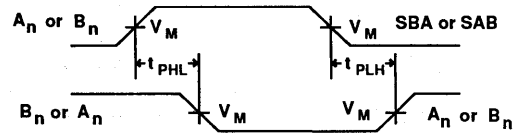
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



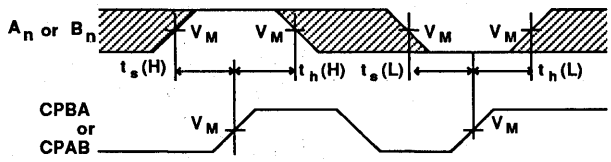
Waveform 2. Enable and Disable Times for Open Collector Outputs



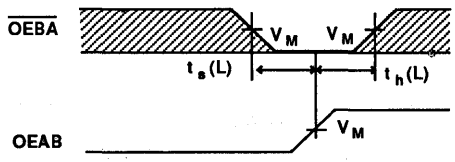
Waveform 3. Propagation Delay, An to Bn or Bn to An and SBA to An or SAB to Bn



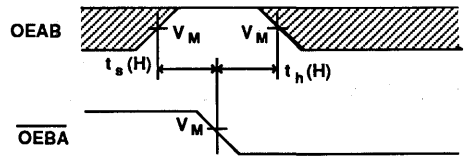
Waveform 4. Propagation Delay, An to Bn or Bn to An and SBA to An or SAB to Bn



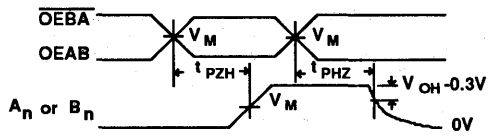
Waveform 5. Data Setup And Hold Times



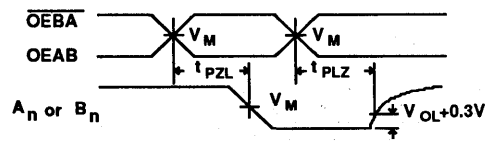
Waveform 6. $\overline{OEBA}$ to OEAB Setup And Hold Times



Waveform 7. OEAB to $\overline{OEBA}$ Setup And Hold Times



Waveform 8. 3-State Output Enable Time To High Level And Output Disable Time From High Level

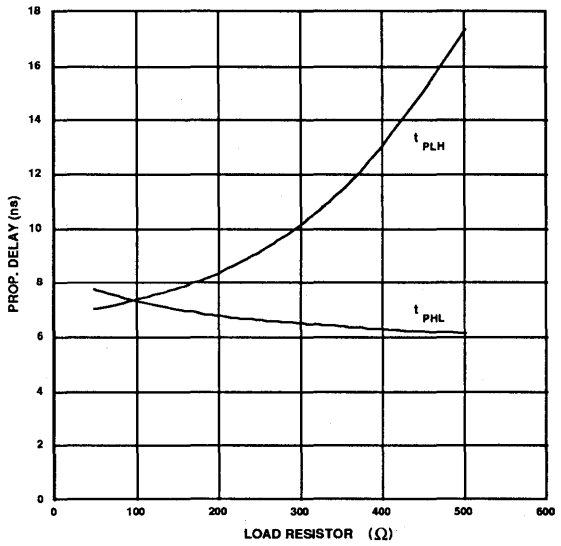


Waveform 9. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

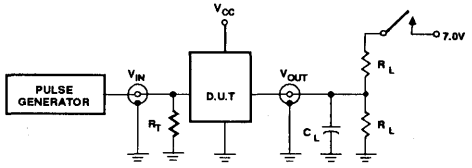
The shaded areas indicate when the input is permitted to change for predictable output performance.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers do not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State and Open Collector Outputs

SWITCH POSITION

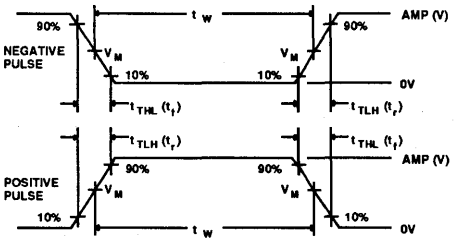
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
Open Collector	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F655A, 74F656A
Buffers/Drivers

74F655A Octal Buffer/Driver With Parity, Inverting (3-State)
74F656A Octal Buffer/Driver With Parity, Non-Inverting (3-State)

Product Specification

FAST Products

FEATURES

- **Significantly improved AC performance over 'F655 and 'F656**
- **High impedance NPN base inputs for reduced loading (40μA in High and Low states)**
- **Ideal in applications where high output drive and light bus loading are required (I_{IL} is 40μA vs FAST std of 600 A)**
- **'F655A combines 'F240 and 'F280A functions in one package**
- **'F656A combines 'F244 and 'F280A functions in one package**
- **'F655A Inverting**
  'F656A Non-Inverting
- **3-state outputs sink 64mA and source 15mA**
- **24-pin plastic Slim DIP (300mil) package**
- **Inputs on one side and outputs on the other side simplifies PC board layout**
- **Combined functions reduce part count and enhance system performance**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F655A	6.5ns	64mA
74F656A	6.5ns	64mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F655AN, N74F656AN
24-Pin Plastic SOL	N74F655AD, N74F656AD

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0- D_7	Data inputs	2.0/0.066	40μA/40μA
PI	Parity input	1.0/0.033	20μA/20μA
$\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$	Output Enable inputs (active Low)	1.0/0.033	20μA/20μA
Σ_E, Σ_O	Parity outputs	750/106.7	15mA/64mA
$\overline{Q}_0$- $\overline{Q}_7$	Data outputs ('F655A)	750/106.7	15mA/64mA
Q_0- Q_7	Data outputs ('F656A)	750/106.7	15mA/64mA

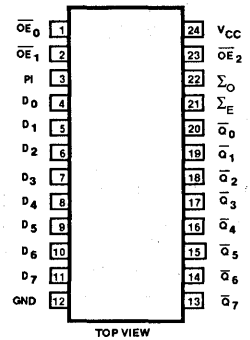
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 74F655A and 74F656A are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

PIN CONFIGURATION

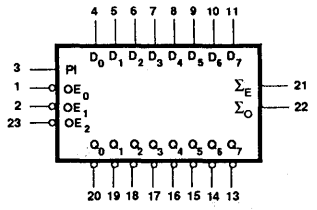
'F655A



TOP VIEW

LOGIC SYMBOL

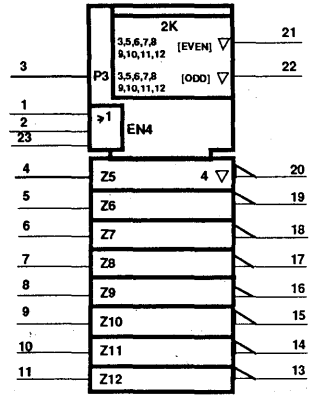
'F655A



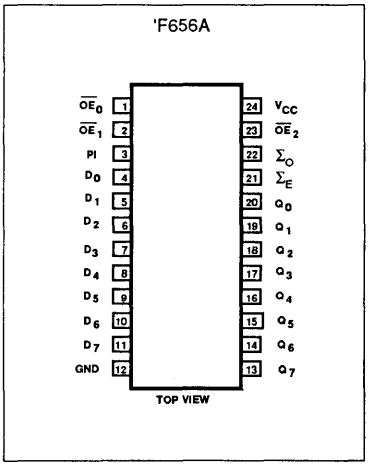
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

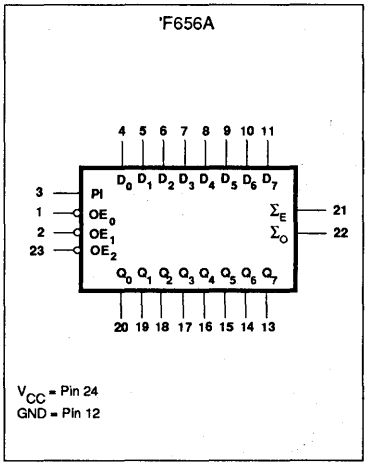
'F655A



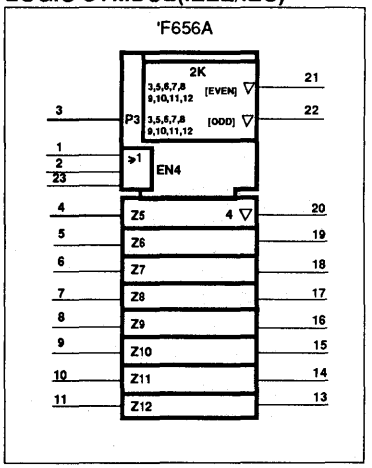
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



FUNCTION TABLE

INPUTS				OUTPUTS	
				'F655A	'F656A
$\overline{OE}_0$	$\overline{OE}_1$	$\overline{OE}_2$	D_n	$\overline{Q}_n$	Q_n
L	L	L	L	H	L
L	L	L	H	L	H
H	X	X	X	Z	Z
X	H	X	X	Z	Z
X	X	H	X	Z	Z

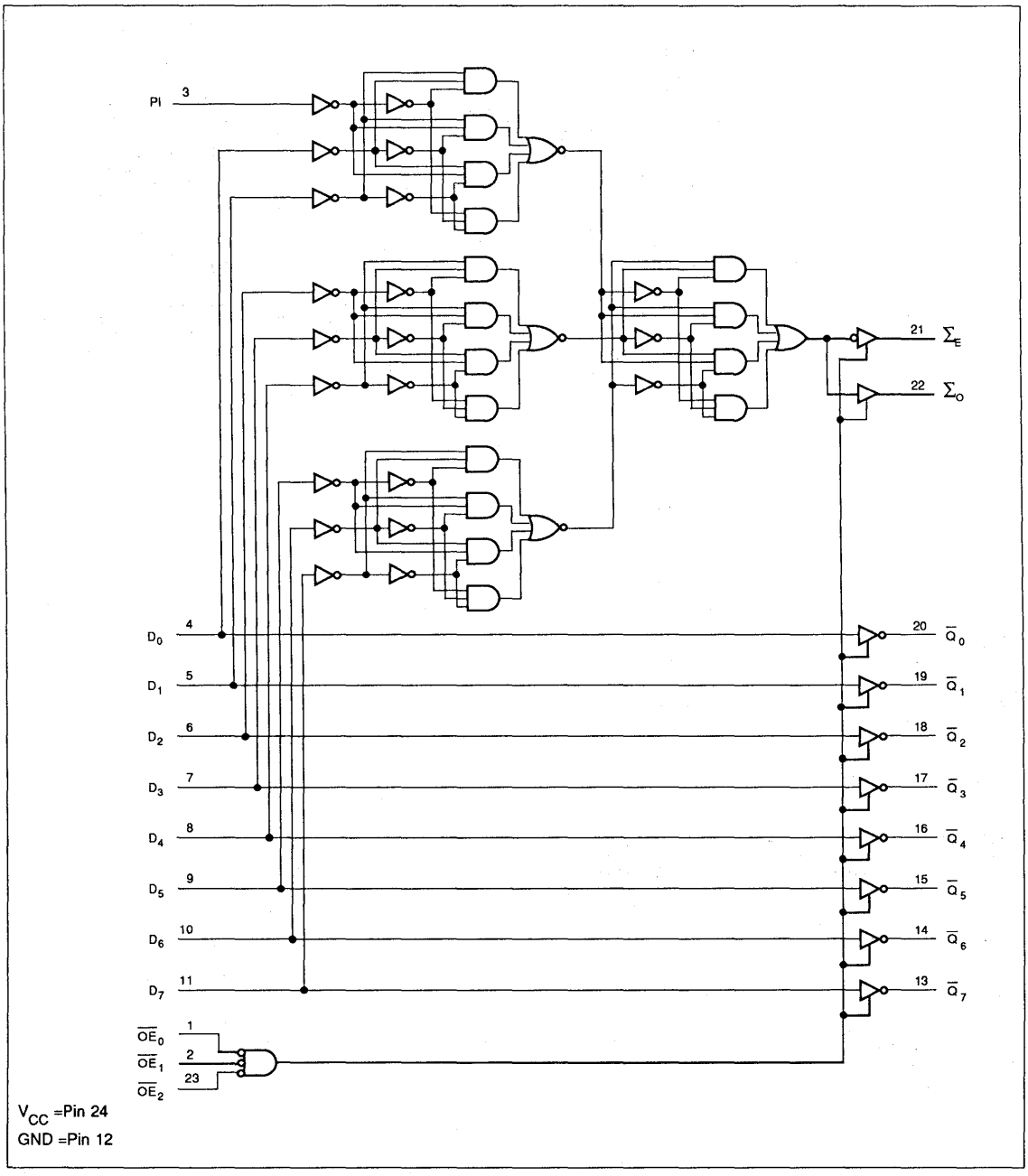
H= High voltage level
L= Low voltage level
X=Don't care
Z =High impedance "off" state

FUNCTION TABLE for PARITY OUTPUTS

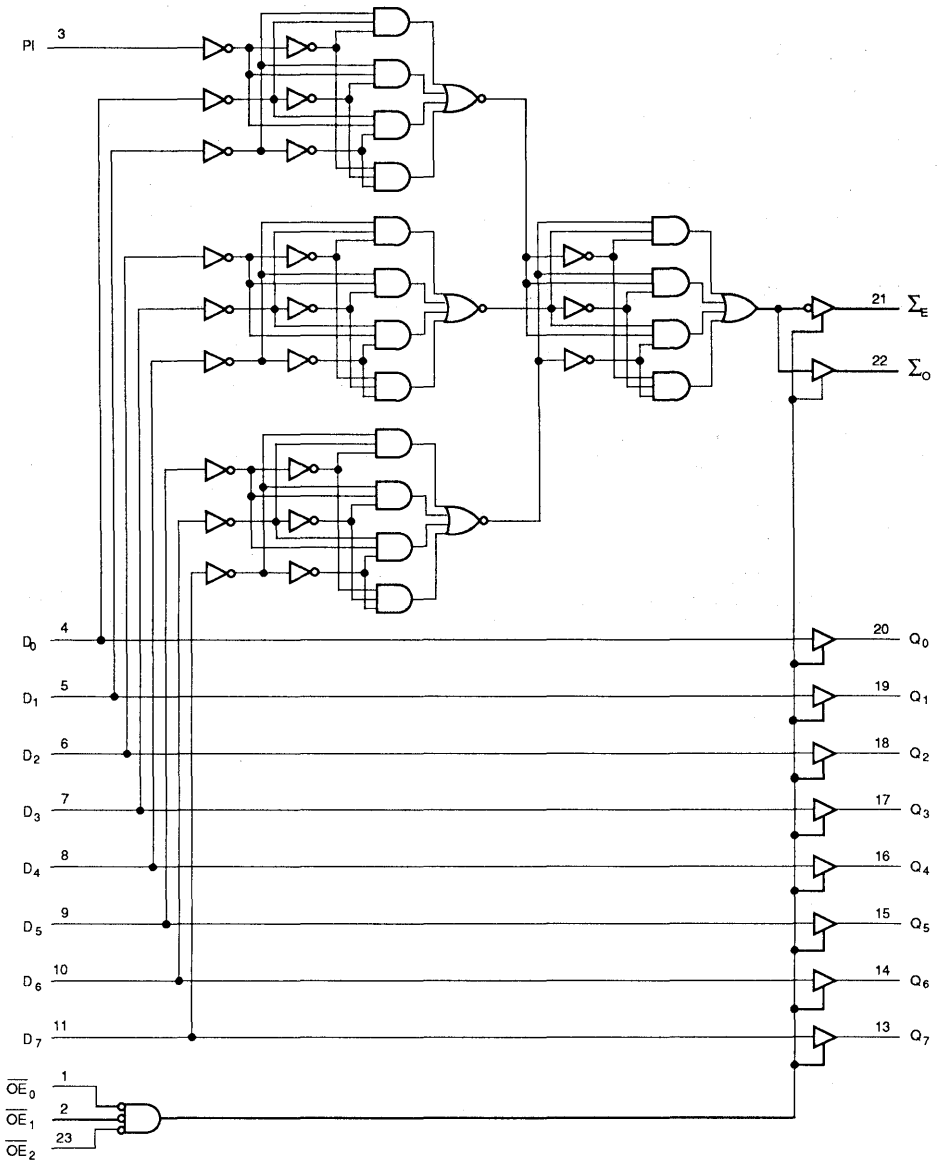
INPUTS	OUTPUTS	
Number of inputs High (PI, D_0-D_7)	Σ_E	Σ_O
Even ------ 0, 2, 4, 6, 8	H	L
Odd ------1, 3, 5, 7, 9	L	H
Any $\overline{OE}_n$=High	Z	Z

H= High voltage level
L= Low voltage level
Z =High impedance "off" state

LOGIC DIAGRAM for 'F655A



LOGIC DIAGRAM for 'F656A



V_{CC} =Pin 24
GND =Pin 12

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

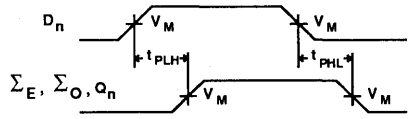
SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
				I_{OH}=-15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=MAX	±10%V_{CC}			0.55	V
					±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	D_n	V_{CC} = MAX, V_I = 2.7V					40	µA
		PI, $\overline{OE}_n$						20	µA
I_{IL}	Low-level input current	D_n	V_{CC} = MAX, V_I = 0.5V					-40	µA
		PI, $\overline{OE}_n$						-20	µA
I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				50	80	mA
		I_{CCL}					78	110	mA
		I_{CCZ}					83	90	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

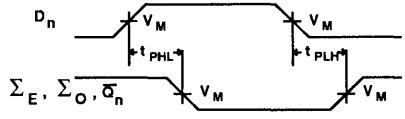
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	'F655A	Waveform 2	2.0 1.0	4.5 2.5	6.5 4.0	2.0 1.0	7.5 4.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	'F656A	Waveform 1	2.0 2.5	4.0 5.5	6.5 7.0	2.0 2.5	7.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Σ_E, Σ_O		Waveform 1, 2	5.5 5.5	10.0 11.0	13.0 14.5	5.5 5.5	14.0 16.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	4.0 4.0	7.0 8.0	10.5 11.0	4.0 4.0	11.5 12.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level		Waveform 3 Waveform 4	1.5 2.0	4.5 5.0	8.0 8.0	1.5 2.0	9.0 9.0	ns

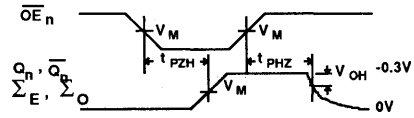
AC WAVEFORMS



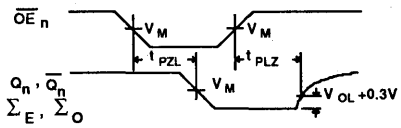
Waveform 1. Propagation Delay, Non-Inverting Outputs



Waveform 2. Propagation Delay, Inverting Outputs



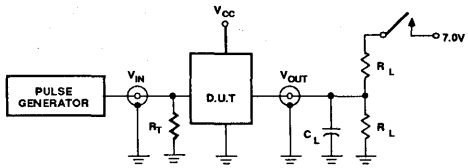
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

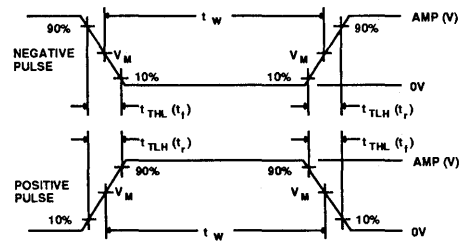
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F657, 74F657A Transceivers

FAST Products

FEATURES

- **Combines 74F245 and 74F280A functions in one package**
- **High impedance base input for reduced loading (70μA in High and Low states)**
- **Ideal in applications where High output drive and light bus loading are required (I_{IL} is 70μA vs FAST std of 600μA)**
- **3-state buffer outputs sink 64mA and source 15 mA**
- **Input diodes for termination effects**
- **24-pin plastic Slim Dip (300mil) package**

DESCRIPTION

The 74F657 is an octal transceiver featuring non-inverting buffers with 3-state outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 24mA at the A ports and 64mA at the B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active-High) enables data from A ports to B ports; Receive (active-Low) enables data from B ports to A ports.

The 74F657A is the faster version of 74F657.

74F657/657A Octal Transceivers With 8-Bit Parity Generator/Checker (3-State)

Product Specification for 74F657

Preliminary Specification for 74F657A

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F657	8.0ns	100mA
74F657A	7.0ns	100mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300 mil)	N74F657N, N74F657AN
24-Pin Plastic SOL[1]	N74F657D, N74F657AD

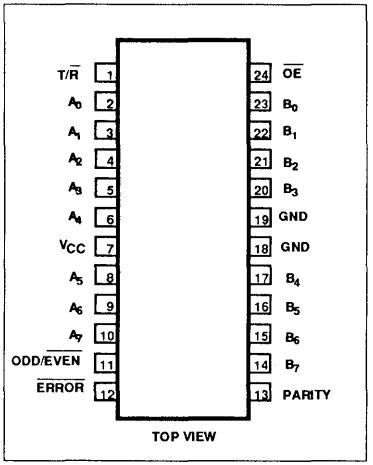
NOTE:
1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

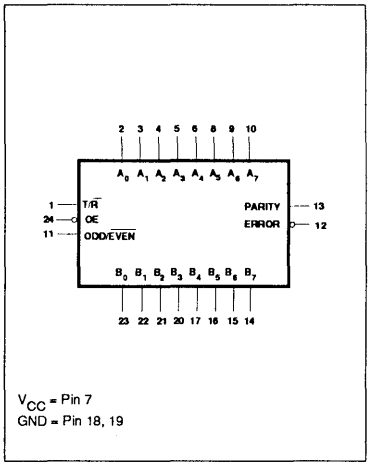
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A ports 3-state inputs	3.5/0.117	70μA/70μA
B_0 - B_7	B ports 3-state inputs	3.5/0.117	70μA/70μA
PARITY	Parity input	3.5/0.117	70μA/70μA
$T/\overline{R}$	Transmit/Receive input	2.0/0.066	40μA/40μA
ODD/$\overline{EVEN}$	Parity select input	1.0/0.033	20μA/20μA
$\overline{OE}$	Output Enable input (active Low)	2.0/0.066	40μA/40μA
A_0 - A_7	A port 3-state outputs	150/40	3.0mA/24mA
B_0 - B_7	B port 3-state outputs	750/106.7	15mA/64mA
PARITY	Parity output	750/106.7	15mA/64mA
$\overline{ERROR}$	Error output	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

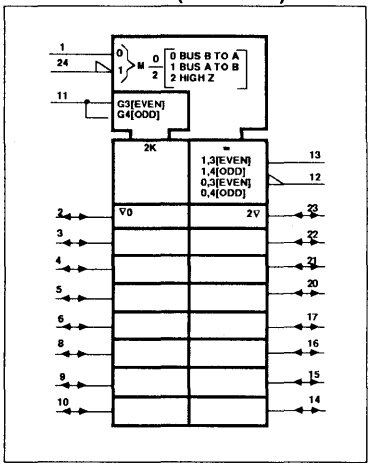
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



The Output Enable ($\overline{OE}$)input disables both the A and B ports by placing them in a high impedance condition when the $\overline{OE}$ input is High. The parity select (ODD/$\overline{EVEN}$) input gives the user the option of odd or even parity systems. The parity (PARITY) pin is an output from the generator/checker when transmitting from the port A to B (T/$\overline{R}$=High) and an input when receiving from port B to A port (T/$\overline{R}$=Low). When transmitting (T/$\overline{R}$=High) the parity select (ODD/$\overline{EVEN}$) input is set, then the A port data is polled to determine the number of High bits. The parity (PARITY) output then goes to the logic state determined by the parity select (ODD/$\overline{EVEN}$) setting and by the number of High bits on port A. For example, if the parity select (ODD/$\overline{EVEN}$) is set Low (even parity), and the number of High bits on port A is odd, then the parity (PARITY) output will be High, transmitting even parity. If the number of High bits on port A is even, then the parity (PARITY) output will be Low, keeping even parity. When in receive mode (T/$\overline{R}$=Low) the B port is polled to determine the number of High bits. If parity select (ODD/$\overline{EVEN}$) is Low (even parity) and the number of Highs on port B is:

(1) odd and the parity (PARITY) input is High, then $\overline{ERROR}$ will be High, signifying no error.

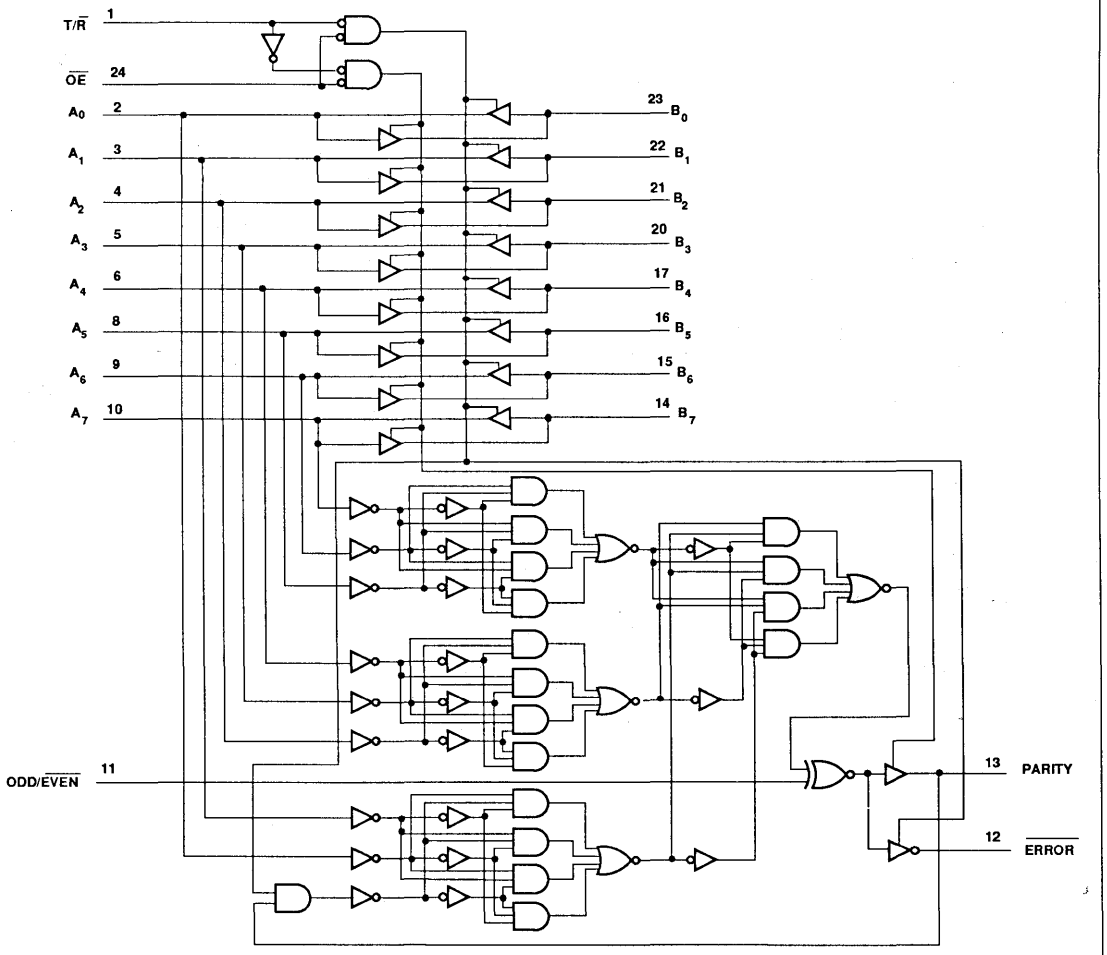
(2) even and the parity (PARITY) input is High, then $\overline{ERROR}$ will be asserted Low, indicating an error.

FUNCTION TABLE

NUMBER OF INPUTS THAT ARE HIGH	INPUTS			INPUT/ OUPUT	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$	PARITY	$\overline{ERROR}$	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	3-state

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



V_{CC}=Pin 7
GND=Pin 18, 19

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7, PARITY, $\overline{ERROR}$	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0B_7, PARITY, $\overline{ERROR}$			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7, PARITY, $\overline{ERROR}$			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	All outputs	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		B_0-B_7, PARITY, $\overline{ERROR}$		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7, PARITY, $\overline{ERROR}$		I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$, ODD/$\overline{EVEN}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_0-A_7	V_{CC} = MAX, V_I = 5.5V					2	mA
		B_0-B_7						1	mA
I_{IH}	High-level input current	ODD/$\overline{EVEN}$	V_{CC} = MAX, V_I = 2.7V					20	µA
		$\overline{OE}$, T/$\overline{R}$						40	µA
I_{IL}	Low-level input current	ODD/$\overline{EVEN}$	V_{CC} = MAX, V_I = 0.5V					-20	µA
		$\overline{OE}$, T/$\overline{R}$						-40	µA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied	A_0-A_7, B_0-B_7, PARITY	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-70	µA
I_{OZH}	Off-state output current High-level voltage applied	$\overline{ERROR}$	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]	A_0-A_7	V_{CC} = MAX			-60		-150	mA
		B_0-B_7				-100		-225	µA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				90	125	mA
		I_{CCL}					106	150	mA
		I_{CCZ}					98	145	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 74F657

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 2	2.5 3.0	5.5 6.0	7.5 7.5	2.5 3.0	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to PARITY	Waveform 1,2	7.0 7.0	10.0 10.0	14.0 15.0	7.0 7.0	16.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{EVEN}$ to PARITY, $\overline{ERROR}$	Waveform 1,2	4.5 4.5	7.5 8.0	11.0 11.5	4.5 4.5	12.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to $\overline{ERROR}$	Waveform 1,2	8.0 8.0	14.0 14.0	20.5 20.5	7.5 7.5	22.5 22.5	ns
t_{PLH} t_{PHL}	Propagation delay PARITY to $\overline{ERROR}$	Waveform 1,2	8.0 8.0	11.5 12.0	15.5 15.5	7.5 8.0	16.5 17.0	ns
t_{PZH} t_{PZL}	Output Enable time[1] to High or Low level	Waveform 3 Waveform 4	3.0 4.0	5.5 7.0	8.0 9.5	3.0 4.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 3 Waveform 4	2.0 2.0	4.5 4.0	7.5 6.0	2.0 2.0	8.0 6.5	ns

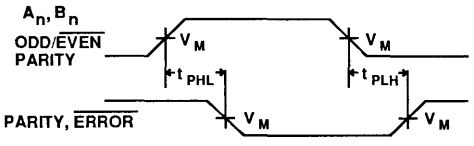
NOTE:
1. These delay times reflect the 3-state recovery time only and not the signal through the buffers or the parity check circuitry. To assure VALID information at the $\overline{ERROR}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{ERROR}$ output . VALID data at the $\overline{ERROR}$ pin ≥ (B to A) + (A to PARITY) .

AC ELECTRICAL CHARACTERISTICS for 74F657A

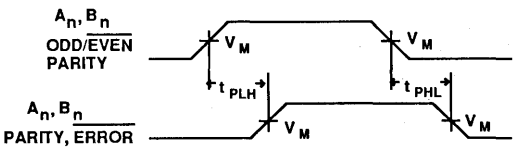
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 2	2.0 2.0	4.5 4.5	7.0 7.0	2.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n to PARITY	Waveform 1,2	6.5 6.5	9.5 9.5	13.0 13.0	6.5 6.5	14.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{EVEN}$ to PARITY, $\overline{ERROR}$	Waveform 1,2	4.5 4.5	7.0 7.0	10.5 10.5	4.5 4.5	11.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to $\overline{ERROR}$	Waveform 1,2	7.0 7.0	12.0 12.0	18.0 18.0	6.5 6.5	19.0 19.0	ns
t_{PLH} t_{PHL}	Propagation delay PARITY to $\overline{ERROR}$	Waveform 1,2	8.0 8.0	10.5 10.5	14.0 14.0	7.0 7.0	15.0 15.0	ns
t_{PZH} t_{PZL}	Output Enable time[1] to High or Low level	Waveform 3 Waveform 4	3.0 4.0	5.5 6.5	8.0 9.0	3.0 4.0	9.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 3 Waveform 4	2.0 2.0	4.5 4.0	7.5 6.0	2.0 2.0	8.0 6.5	ns

NOTE:
1. These delay times reflect the 3-state recovery time only and not the signal through the buffers or the parity check circuitry. To assure VALID information at the $\overline{ERROR}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{ERROR}$ output . VALID data at the $\overline{ERROR}$ pin ≥ (B to A) + (A to PARITY) .

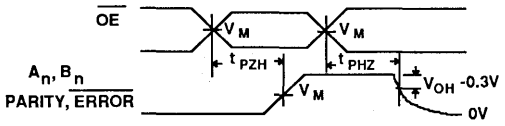
AC WAVEFORMS



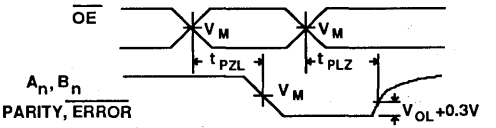
Waveform 1. Propagation Delay for Inverting Outputs



Waveform 2. Propagation Delay for Non-Inverting Outputs



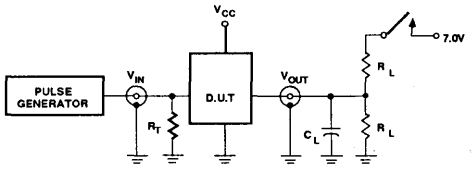
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

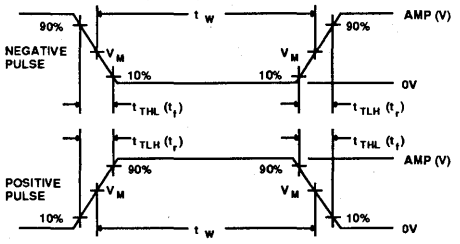
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F670
Register File

4X4 Register File (3-State)
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N74F670	6.5 ns	50mA

FEATURES

- **Simultaneous and independent Read and Write operations**
- **Expandable to almost any word size and bit length**
- **3-state outputs**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F670N
16-Pin Plastic SOL	N74F670D

DESCRIPTION

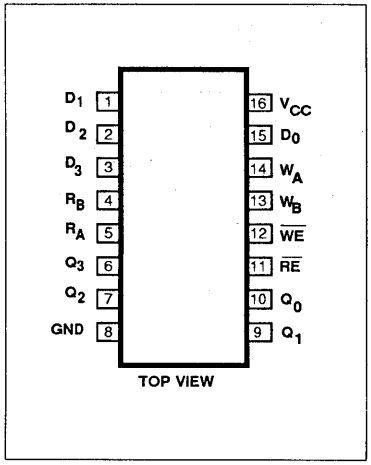
The 74F670 is a 16 bit 3-state Register File organized as 4 words of 4 bits each. Separate Read and Write Address and Enable inputs are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four data inputs. The Write Address inputs (W_A and W_B) determine the location of the stored word. The Write Address inputs should only be changed when the $\overline{WE}$ input is High for conventional operation. When the Write Enable ($\overline{WE}$) input is Low, the data is entered into the addressed location. The addressed location remains transparent to the data while the $\overline{WE}$ is Low.Data supplied at the inputs will be read out in true (non-inverting) form from the 3-state outputs. Data and address inputs are inhibited when $\overline{WE}$ is High. Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (R_A, R_B). The addressed word appears at the four outputs when the Read Enable ($\overline{RE}$) is Low. Data outputs are in the High impedance "off " state when the $\overline{RE}$ is High. This permits outputs to be tied together to increase the word capacity to very large numbers. Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-state outputs together. Since the limiting factor for expansion is the output High current, further stacking is possible by tying pullup resistors to the outputs to increase the I_{OH} current available. Design of the Read Enable signals for the stacked devices must ensure that there is no overlap in the Low levels which cause more than one output tobe active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the Enable and address inputs of each device in parallel.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

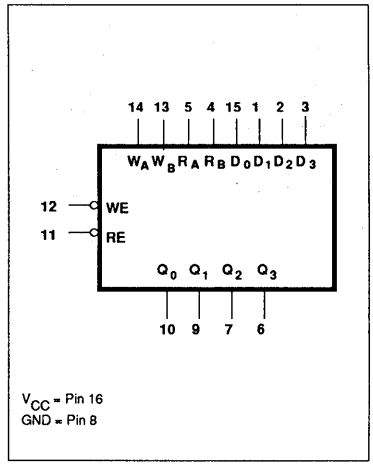
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
W_A, W_B	Write address inputs	1.0/1.0	20µA/0.6mA
R_A, R_B	Read address inputs	1.0/1.0	20µA/0.6mA
$\overline{WE}$	Write Enable input	1.0/1.0	20µA/0.6mA
$\overline{RE}$	Read Enable input	1.0/1.0	20µA/0.6mA
Q_0 - Q_3	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

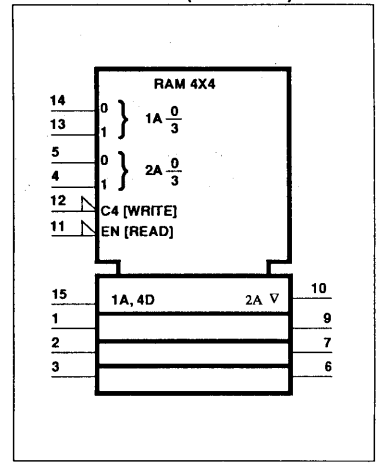
PIN CONFIGURATION



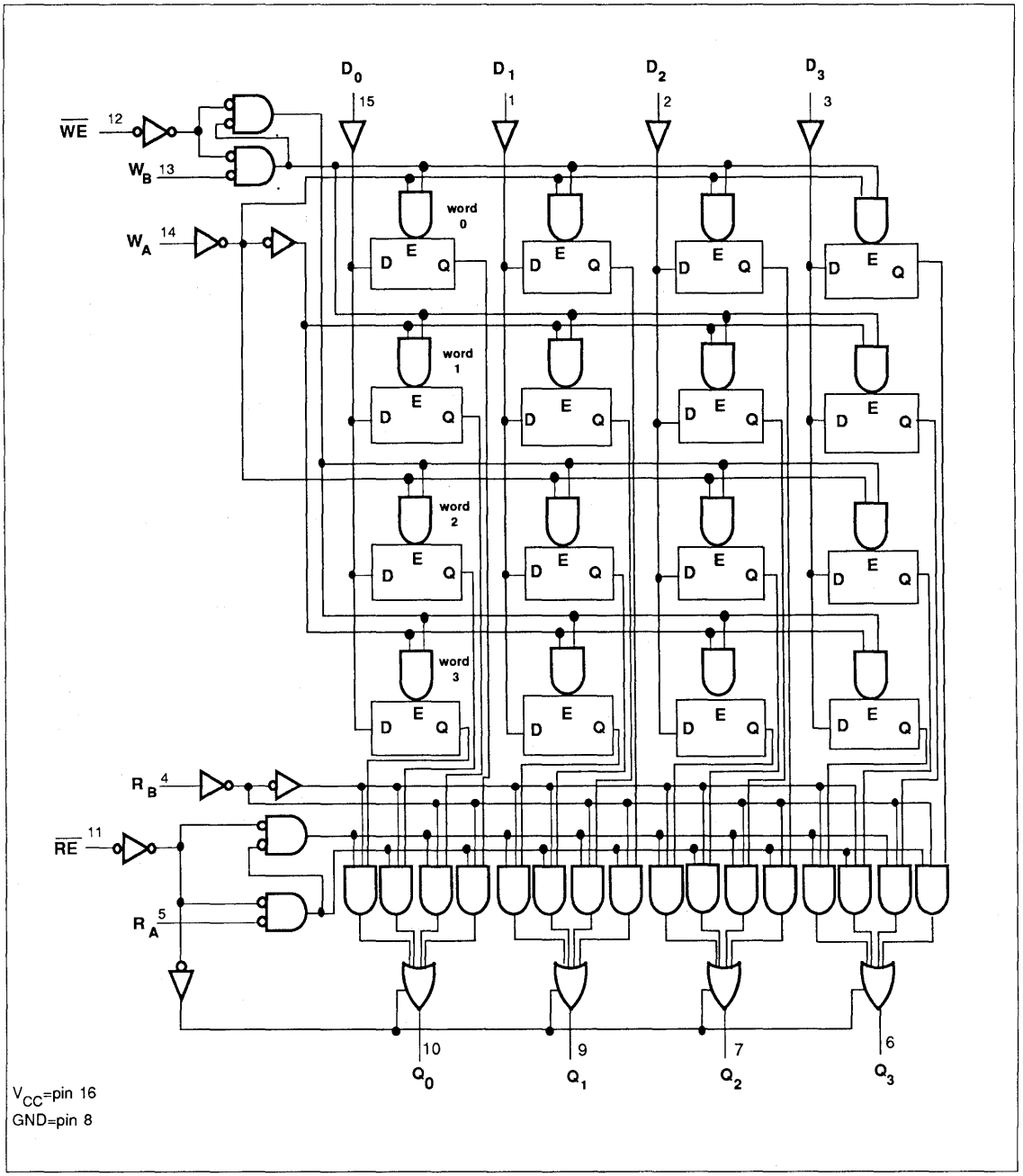
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



WORD SELECT FUNCTION TABLE

WRITE MODE		READ MODE		OPERATING MODE
W_B	W_A	R_B	R_A	Word selected
L	L	L	L	Word 0
L	H	L	H	Word 1
H	L	H	L	Word 2
H	H	H	H	Word 3

H = High voltage level
L = Low voltage level

WRITE MODE FUNCTION TABLE

INPUTS		INTERNAL LATCHES*	OPERATING MODE
$\overline{WE}$	D_n		
L	L	L	Write data
L	H	H	
H	X	NC	Data latched

H = High voltage level
L = Low voltage level
NC=No change
X = Don't care
*=The write address (W_A and W_B) to the "Internal latches" must be stable while $\overline{WE}$ is Low for conventional operation.

READ MODE FUNCTION TABLE

INPUT	INTERNAL LATCHES*	OUTPUT	OPERATING MODE
$\overline{RE}$		Q_n	
L	L	L	Read
L	H	H	
H	X	Z	Disabled

H = High voltage level
L = Low voltage level
X=Don't care
Z=High impedance"off" state
*=The selection of the "internal latches" by Read Address (R_A and R_B) are not constrained by $\overline{WE}$ or $\overline{RE}$ operation.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH}	Off state output current, High-level voltage applied		V_{CC} =MAX, V_O=2.7V				50	µA
I_{OZL}	Off state output current, Low-level voltage applied		V_{CC} =MAX, V_O=0.5V				-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			50	70	mA
		I_{CCL}				50	70	mA
		I_{CCZ}				55	80	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

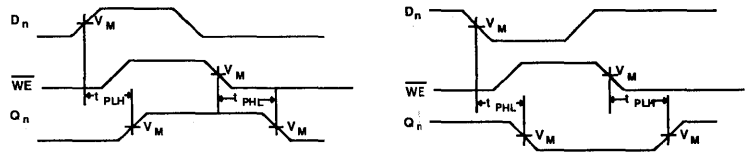
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay R_A, R_B to Q_n	Waveform 2	3.5 4.0	5.5 5.5	9.0 8.5	3.0 3.5	10.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{WE}$ to Q_n	Waveform 1	5.0 6.5	7.0 8.5	10.0 11.5	4.5 6.0	11.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	3.5 6.0	6.0 8.0	8.5 11.0	3.0 5.5	9.5 12.5	ns
t_{PZH} t_{PZL}	$\overline{RE}$ Enable time Q_n High or Low level	Waveform 3 Waveform 4	3.0 4.5	7.0 6.5	12.0 9.0	2.5 4.0	13.0 10.0	ns
t_{PHZ} t_{PLZ}	$\overline{RE}$ Disable time Q_n High or Low level	Waveform 3 Waveform 4	2.0 3.0	3.0 5.0	6.5 8.5	1.5 3.0	7.5 8.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to positive going $\overline{WE}$	Waveform 2	1.5 6.0			1.5 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to positive going $\overline{WE}$	Waveform 2	0 1.0			0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low W_A, W_B to negative going $\overline{WE}$[1]	Waveform 2	0 0			0 0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low W_A, W_B to negative going $\overline{WE}$[1]	Waveform 2	0 0			0 0		ns
$t_w(L)$	$\overline{RE}$ Pulse width, Low	Waveform 3	6.5			8.5		ns

NOTE 1: Write Address (W_A,W_B) setup time will protect the data written into the previous address. If protection of data in the previous address is not required, setup time for Write Address to $\overline{WE}$ can be ignored.. Any address selection sustained for the final 7ns of the $\overline{WE}$ pulse and during hold time for Write Address to $\overline{WE}$ will result in data being written into that location.

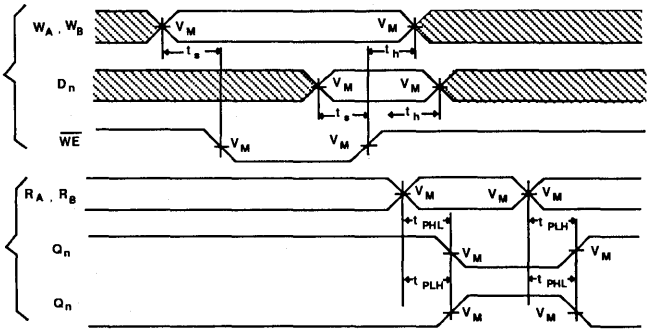
AC WAVEFORMS



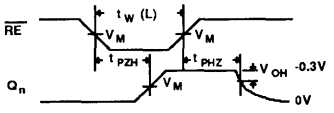
Waveform1. Propagation delay, Write Enable And Data To Outputs

Setup and Hold times for Write Address to Write Enable and data to Write Enable

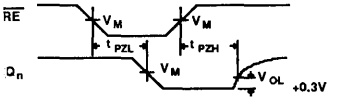
Propagation delays for Read Address to output



Waveform 2. Setup and Hold Times, Write Address To Write Enable and Data To Write Enable And Propagation Delay Read Address To Output



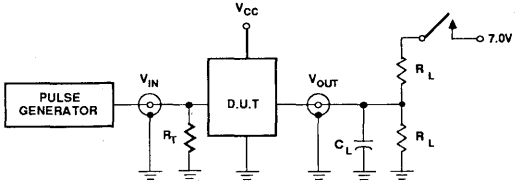
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

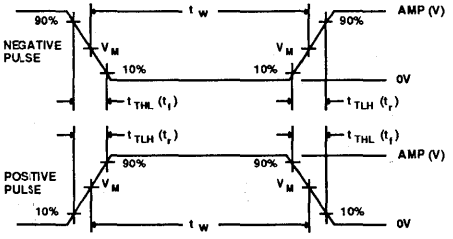
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F674
Shift Register

FAST Products

16-Bit Serial/Parallel-In, Serial-Out Shift Register (3-State)
Product Specification

FEATURES
- **16-bit serial I/O shift register**
- **16-bit parallel-in/serial-out converter**
- **Recirculating serial shifting**
- **Common serial data I/O pin (3-state)**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F674	95MHz	55mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F674N
24-Pin Plastic SOL	N74F674D

DESCRIPTION

The 74F674 is a 16 bit shift register with serial and parallel load capability and serial output. A single pin serves alternately as an input for serial entry or as 3-state serial output. In the serial out mode the data recirculates in the register. Chip Select, Read/Write and Mode inputs provide control flexibility. The 'F674 operates in one of four modes, as indicated in the Function Table.

Hold : a High signal on the Chip Select ($\overline{CS}$) input prevents clocking and forces the Serial Input/Output (SI/O) 3-state buffer into the high impedance state.

Serial load : data present on the SI/O pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks.

Serial output : the SI/O 3-state buffer is active and the register contents are shifted out from Q_{15} and simultaneously shifted back into Q_0.

Parallel load : data present on D_0- D_{15} is entered into the register on the falling edge of $\overline{CP}$. The SI/O 3-state buffer is active and represents the Q_{15} output.

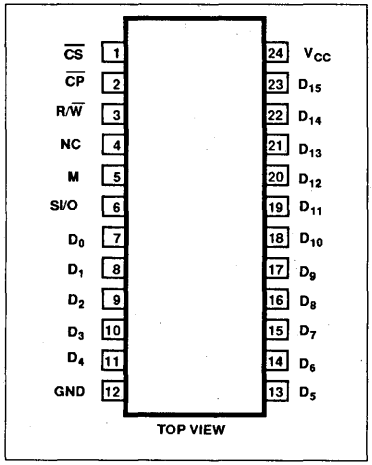
To prevent false clocking, $\overline{CP}$ must be Low during a Low-to-High transition of $\overline{CS}$.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

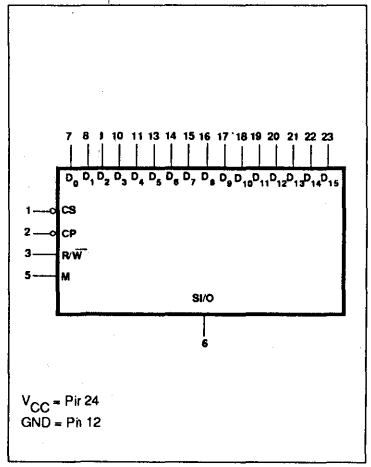
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 -D_{15}	Parallel data inputs	1.0/1.0	20µA/0.6mA
$\overline{CS}$	Chip Select input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CP}$	Clock Pulse input (active falling edge)	1.0/1.0	20µA/0.6mA
M	Mode select input	1.0/1.0	20µA/0.6mA
R/$\overline{W}$	Read/Write input	1.0/1.0	20µA/0.6mA
SI/O	Serial data input or	3.5/1.0	70µA/0.6mA
	Serial 3-state output	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

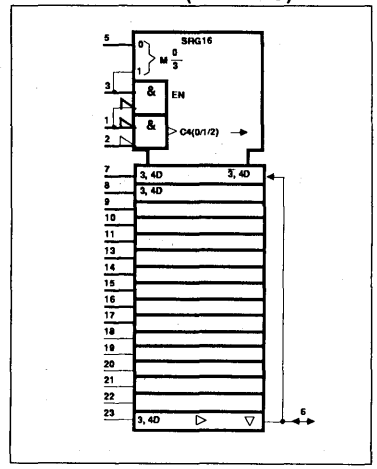
PIN CONFIGURATION



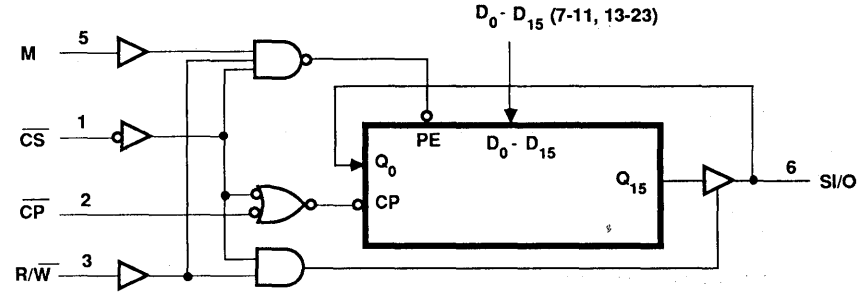
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} =pin 24
GND=pin 12

FUNCTION TABLE

CONTROL INPUTS				SI/O STATUS	OPERATING MODE
$\overline{CS}$	R/$\overline{W}$	M	$\overline{CP}$		
H	X	X	X	High Z	Hold
L	L	X	↓	Data in	Serial load
L	H	L	↓	Data out	Serial output with recirculation
L	H	H	↓	Active	Parallel load ; no shifting

H = High voltage level
L = Low voltage level
X = Don't care
↓ = High-to-Low transition of designated input

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	SI/O only	V_{CC} = MAX, V_I = 5.5V				100	µA
		others	V_{CC} = MAX, V_I = 7.0V					
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OZH} + I_{IH}	Off state output current, High-level voltage applied	SI/O only	V_{CC} =MAX, V_O=2.7V				70	µA
I_{OZL}+I_{IL}	Off state output current, Low-level voltage applied		V_{CC} =MAX, V_O=0.5V				-600	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			55	80	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

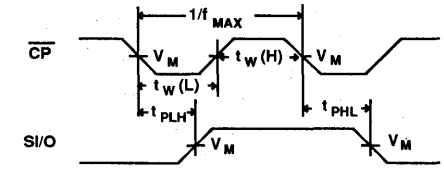
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frquency	Waveform 1	80	95		70		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to SI/O	Waveform 1	7.0 6.0	9.5 8.5	12.5 11.5	6.5 5.5	14.0 12.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{CS}$ to SI/O	Waveform 3 Waveform 4	5.5 7.0	8.5 9.5	11.0 12.5	5.0 6.5	12.5 14.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{CS}$ to SI/O	Waveform 3 Waveform 4	3.0 4.5	6.0 7.5	8.5 10.0	3.0 4.5	10.0 11.5	ns
t_{PZH} t_{PZL}	Output Enable time R/$\overline{W}$ to SI/O	Waveform 3 Waveform 4	6.0 7.5	8.5 10.0	11.5 13.0	5.5 7.0	13.0 14.0	ns
t_{PHZ} t_{PLZ}	Output Disable time R/$\overline{W}$ to SI/O	Waveform 3 Waveform 4	5.0 5.5	7.5 8.0	10.5 11.0	4.5 5.0	12.0 13.5	ns

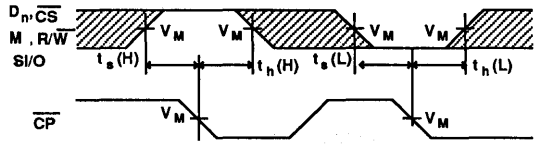
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low SI/O to $\overline{CP}$	Waveform 2	2.0 2.0			2.5 2.5		ns
t_h(H) t_h(L)	Hold time, High or Low SI/O to $\overline{CP}$	Waveform 2	1.5 1.5			2.0 2.0		ns
t_s(H) t_s(L)	Setup time, High or Low D_n to $\overline{CP}$	Waveform 2	1.5 1.0			2.0 1.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to $\overline{CP}$	Waveform 2	3.0 4.0			3.0 4.0		ns
t_s(H) t_s(L)	Setup time, High or Low M to $\overline{CP}$	Waveform 2	2.0 5.5			2.5 6.0		ns
t_h(H) t_h(L)	Hold time, High or Low M to $\overline{CP}$	Waveform 2	0.0 0.0			1.0 1.0		ns
t_s(L)	Setup time, Low $\overline{CS}$ to $\overline{CP}$	Waveform 2	8.0			9.0		ns
t_h(H)	Hold time, High $\overline{CS}$ to $\overline{CP}$	Waveform 2	0.0			0.0		ns
t_w(H) t_w(L)	$\overline{CP}$ Pulse width, High or Low	Waveform 1	3.5 4.5			4.0 5.0		ns

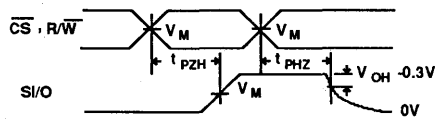
AC WAVEFORMS



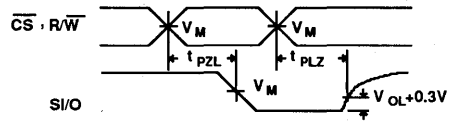
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Setup And Hold Times



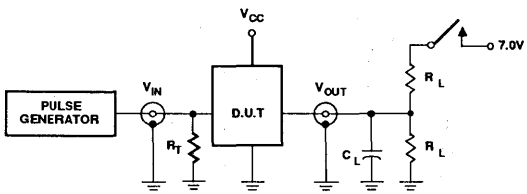
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

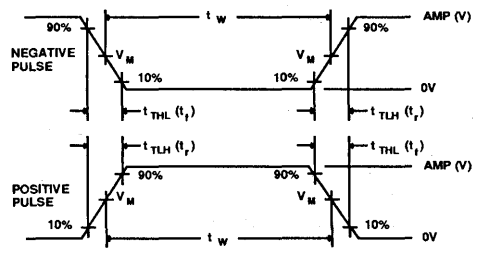
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F676
Shift Register

FAST Products

16-Bit Serial/Parallel-In, Serial-Out Shift Register (3-State)
Product Specification

FEATURES
- **16-bit parallel-to-serial conversion**
- **16-bit serial-in, serial-out**
- **Chip select control**
- **Power supply current 48mA typical**
- **Shift frequency 110 MHz typical**
- **Available in 300mil-wide 24-pin Slim DIP package**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F676	110MHz	48mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F676N
24-Pin Plastic SOL	N74F676D

DESCRIPTION

The 74F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the mode (M) input is High, information present on the parallel data (D_0 - D_{15}) inputs is entered on the falling edge of the clock pulse ($\overline{CP}$) input signal. When M is Low, data is shifted out of the most significant bit position while information present on the serial (SI) input shifts into the least significant bit position. A High signal on the chip select ($\overline{CS}$) input prevents both parallel and serial operations. The 16 bit shift register operates in one of three modes, as indicated in the shift register Function Table.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_{15}	Parallel data inputs	1.0/1.0	20µA/0.6mA
SI	Serial data input	1.0/1.0	20µA/0.6mA
$\overline{CS}$	Chip Select input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CP}$	Clock Pulse input (active falling edge)	1.0/1.0	20µA/0.6mA
M	Mode select input	1.0/1.0	20µA/0.6mA
SO	Serial data output	50/33	1mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

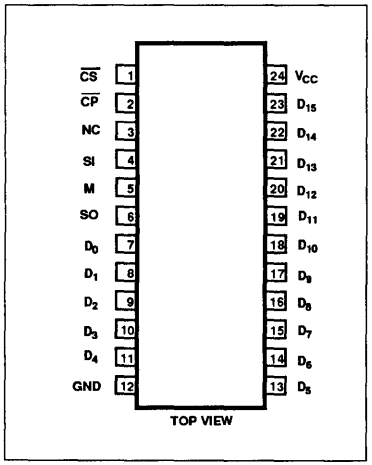
Hold : a High signal on the Chip Select ($\overline{CS}$) input prevents clocking, and data is stored in the 16 registers.

Shift/Serial load : data present on the SI pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks finally appearing on the SO pin.

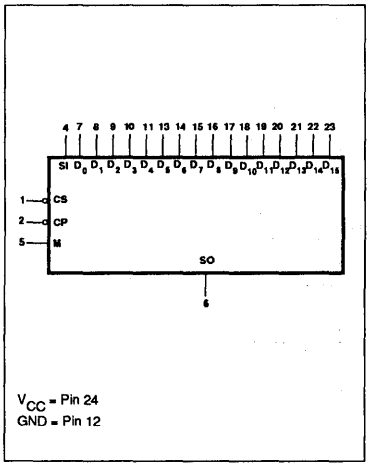
Parallel load : data present on D_0 - D_{15} are entered into the register on the falling edge of $\overline{CP}$. The SO output represents the Q_{15} register output.

To prevent false clocking, $\overline{CP}$ must be Low during a Low-to-High transition of $\overline{CS}$.

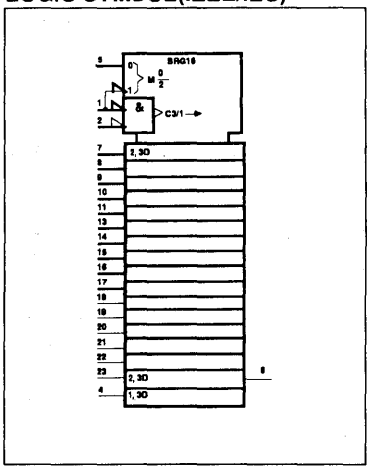
PIN CONFIGURATION



LOGIC SYMBOL

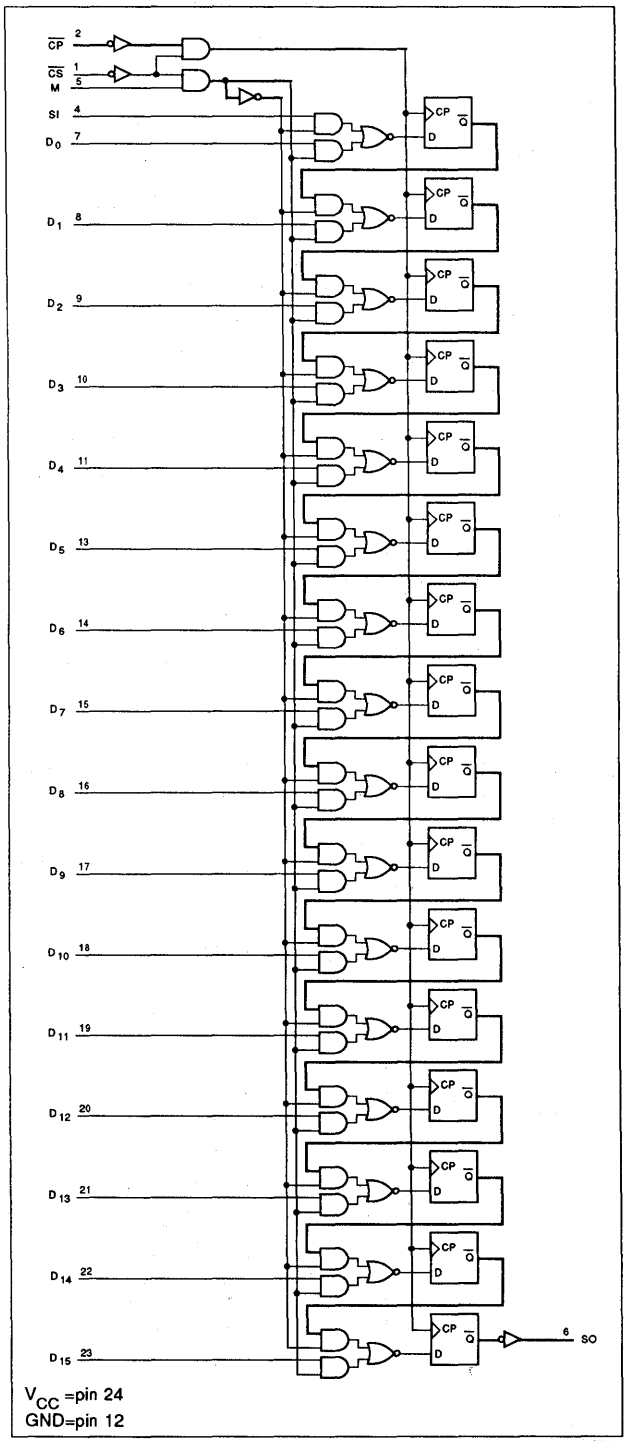


LOGIC SYMBOL(IEEE/IEC)



Shift Register | FAST 74F676

LOGIC DIAGRAM



FUNCTION TABLE

CONTROL INPUTS			OPERATING MODE
$\overline{CS}$	M	$\overline{CP}$	
H	X	X	Hold
L	L	↓	Shift/Serial load
L	H	↓	Parallel load

H = High voltage level
L = Low voltage level
X = Don't care
↓ = High-to-Low transition of clock input

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			48	72	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

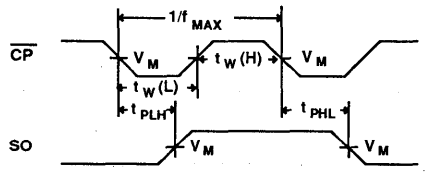
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	110		90		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to SO	Waveform 1	4.5 5.0	8.0 7.0	11.0 12.5	4.5 5.0	12.0 13.5	ns

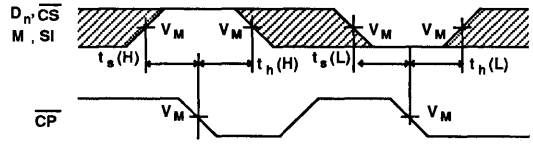
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low SI to $\overline{CP}$	Waveform 2	4.0 4.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low SI to $\overline{CP}$	Waveform 2	4.0 4.0			4.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{CP}$	Waveform 2	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{CP}$	Waveform 2	4.0 4.0			4.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low M to $\overline{CP}$	Waveform 2	8.0 8.0			8.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low M to $\overline{CP}$	Waveform 2	2.0 2.0			2.0 2.0		ns
$t_s(L)$	Setup time, Low $\overline{CS}$ to $\overline{CP}$	Waveform 2	10.0			10.0		ns
$t_h(H)$	Hold time, High $\overline{CS}$ to $\overline{CP}$	Waveform 2	10.0			10.0		ns
$t_w(H)$ $t_w(L)$	$\overline{CP}$ Pulse width, High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns

AC WAVEFORMS



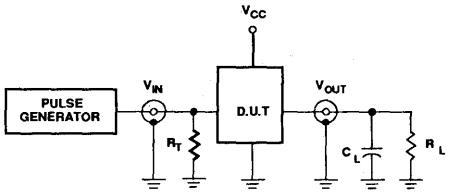
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



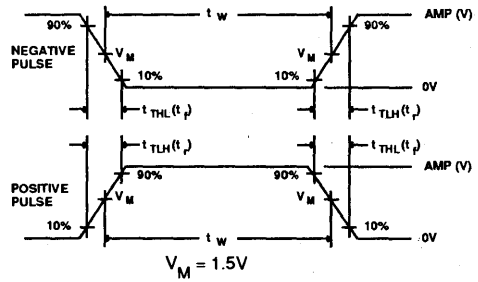
Waveform 2. Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F711/711-1, 74F712/712-1 Multiplexers

74F711 Quint 2-to-1 Data Selector Multiplexer (3-State)
74F711-1 Quint 2-to-1 Data Selector Multiplexer With 30 ohm Series Termination Resistors (3-State)
74F712 Quint 3-to-1 Data Selector Multiplexer
74F712-1 Quint 3-to-1 Data Selector Multiplexer With 30 ohm Series Termination Resistors

Preliminary Specification for 74F711 and 74F712
Product Specification for 74F711-1 and 74F12-1

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F711	5.5ns	26mA
74F711-1	7.0ns	32mA
74F712	6.0ns	19mA
74F712-1	7.0ns	31mA

FEATURES for 74F711/711-1

- **Consists of five 2-to-1 Multiplexers**
- **High impedance PNP base inputs for reduced loading (20μA in High and Low states)**
- **Designed for address multiplexing of dynamic RAM and other applications**
- **Output inverting/non-inverting option**
- **A 30 ohm series termination resistor on each output-'F711-1**
- **Outputs sink 64mA ('F711 only)**

FEATURES for 74F712/712-1

- **Consists of five 3-to-1 Multiplexers**
- **High impedance PNP base inputs for reduced loading (20μA in High and Low states)**
- **Designed for address multiplexing of dynamic RAM and other applications**
- **A 30 ohm series termination resistor on each output-'F712-1**
- **Outputs sink 64mA ('F712 only)**

DESCRIPTION

The 74F711/711-1 consists of five 2-to-1 multiplexers designed for address multiplexing for dynamic RAMs and other multiplexing applications. The 'F711 has a common select (S) input, an Output Enable ($\overline{OE}$) input and an Output Inverting ($\overline{INV}$) input to control the 3-state outputs. The outputs source 15mA and sink 64mA. The 'F711-1 is same as the 'F711 except that it has a 30 ohm series termination

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F711N, N74F711-1N
24-Pin Plastic Slim DIP (300 mil)	N74F712N, N74F712-1N
20-Pin Plastic SOL	N74F711D, N74F711-1D
24-Pin Plastic SOL	N74F712D, N74F712-1D

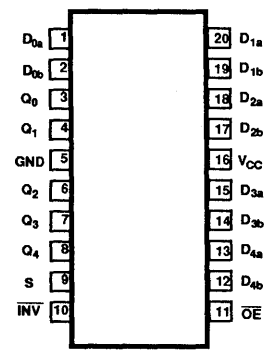
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

TYPE	PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F711/ 'F711-1	D_{na}, D_{nb}	Data inputs	1.0/0.033	20μA/20μA
	S	Select input	1.0/0.033	20μA/20μA
	$\overline{OE}$	Output Enable input (active Low)	1.0/0.033	20μA/20μA
	$\overline{INV}$	Output Inverting input (active Low)	1.0/0.033	20μA/20μA
	Q_0 - Q_4	Data outputs for 'F711	750/106.7	15mA/64mA
	Q_0 - Q_4	Data outputs for 'F711-1	600/8.33	12mA/5mA
'F712/ 'F712-1	D_{na}, D_{nb}, D_{nc}	Data inputs	1.0/0.033	20μA/20μA
	S_0, S_1	Select inputs	1.0/0.033	20μA/20μA
	Q_0 - Q_4	Data outputs for 'F712	750/106.7	15mA/64mA
	Q_0 - Q_4	Data outputs for 'F712-1	600/8.33	12mA/5mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

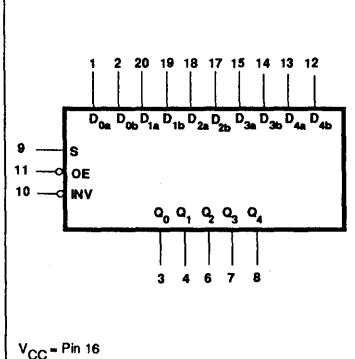
'F711/'F711-1



TOP VIEW

LOGIC SYMBOL

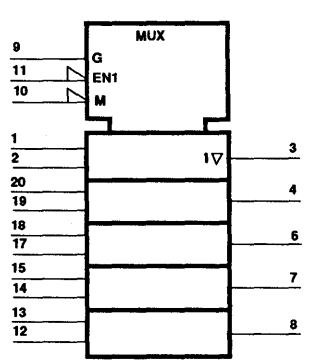
'F711/'F711-1



V_{CC} = Pin 16
GND = Pin 5

LOGIC SYMBOL(IEEE/IEC)

'F711/'F711-1

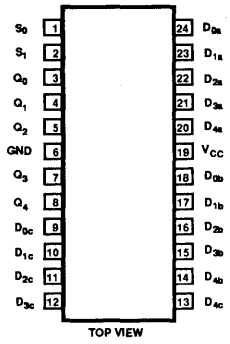


Multiplexers

FAST 74F711/711-1, 74F712/712-1

PIN CONFIGURATION

'F712/712-1



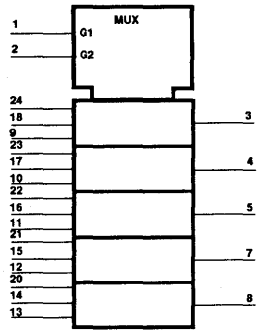
LOGIC SYMBOL

'F712/712-1

V_{CC} = Pin 19
GND = Pin 6

LOGIC SYMBOL(IEEE/IEC)

'F712/712-1



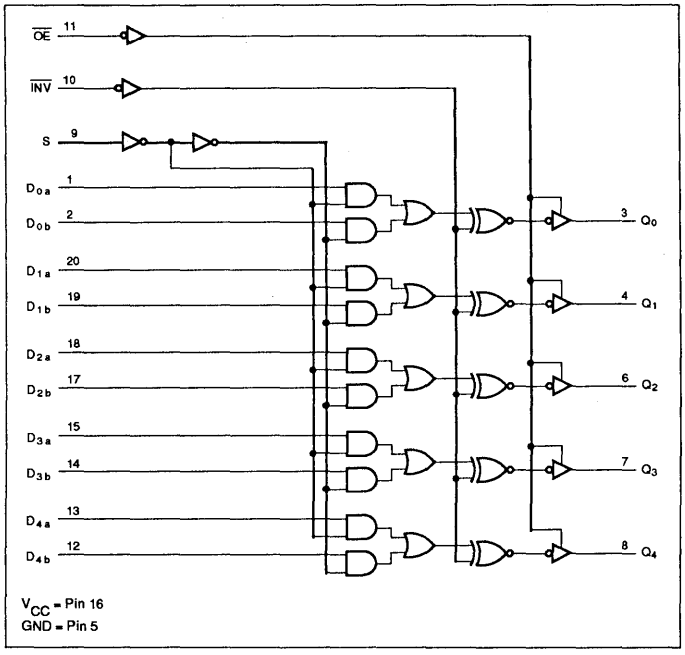
resistor on each output to reduce line noise and the 3-state outputs source 12mA and sink 5mA.

The inverting ($\overline{INV}$) input, when Low, changes data path to inverting in.

To improve speed and noise immunity, V_{CC} and GND side pins are used.

The 74F712/712-1 consists of five 3-to-1 multiplexers designed for address multiplexing for dynamic RAMs and other multiplexing applications. The 'F712 has two select (S_0,S_1) inputs to determine which set of five inputs will be propagated to the five outputs. The outputs source 15mA and sink 64mA. The 'F712-1 is same as the 'F712 except that it has a 30 ohm series termination resistor on each output to reduce line noise and the outputs source 12mA and sink 5mA.

LOGIC DIAGRAM for 'F711/711-1



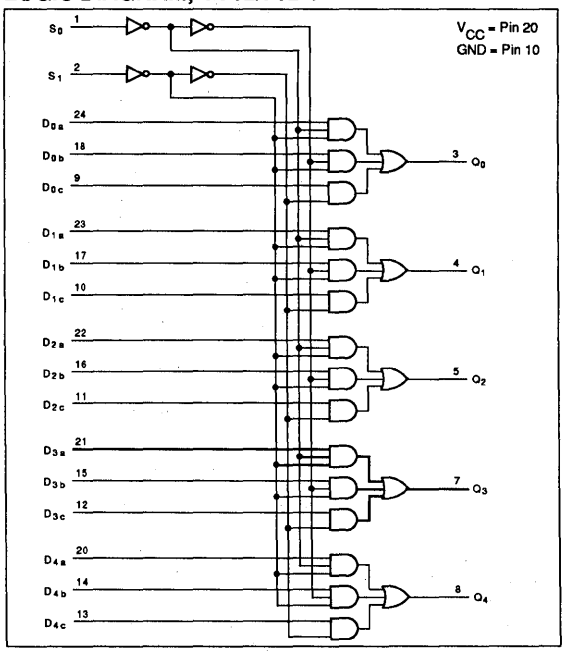
V_{CC} = Pin 16
GND = Pin 5

FUNCTION TABLE for 'F711/711-1

INPUTS					OUTPUT
S	$\overline{INV}$	$\overline{OE}$	D_{na}	D_{nb}	Q_n
L	L	L	data a	data b	$\overline{\text{data a}}$
H	L	L	data a	data b	$\overline{\text{data b}}$
L	H	L	data a	data b	data a
H	H	L	data a	data b	data b
X	X	H	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM, 'F712/712-1



FUNCTION TABLE for 'F712/712-1

INPUTS					OUTPUT
S_0	S_1	D_{na}	D_{nb}	D_{nc}	Q_n
L	L	data a	data b	data c	data a
H	L	data a	data b	data c	data b
X	H	data a	data b	data c	data c

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	'F711, 'F712	128	mA
		'F711-1, 'F712-1	10	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	'F711, 'F712			-15	mA
		'F711-1, 'F712-1			-12	mA
I_{OL}	Low-level output current	'F711, 'F712			64	mA
		'F711-1, 'F712-1			5	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	'F711/ 'F711-1 'F712/ 'F712-1	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		'F711-1/ 'F712-1 only		I_{OH}=-12mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
		'F711/ 'F712 only		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	'F711/ 'F712 only	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
		'F711-1/ 'F712-1		I_{OL}=5mA	±10%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximun input voltage		V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} =MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} =MAX, V_I = 0.5V					-20	µA
I_{OZH}	Off-state output current High-level voltage applied	'F711/ 'F711-1 only	V_{CC} =MAX, V_O= 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} =MAX, V_O= 0.5V					-50	µA
I_{OS}	Short circuit output current[3]	'F711/'F712	V_{CC} =MAX			-100		-225	mA
		'F711-1/ 'F712-1				-60		-150	mA
I_{CC}	Supply current (total)	'F711	I_{CCH}	V_{CC} =MAX			23	35	mA
			I_{CCL}				28	40	mA
			I_{CCZ}				29	40	mA
		'F711-1	I_{CCH}	V_{CC} =MAX			30	40	mA
			I_{CCL}				33	45	mA
			I_{CCZ}				34	45	mA
		'F712	I_{CCH}	V_{CC} =MAX			16	25	mA
			I_{CCL}				22	33	mA
		'F712-1	I_{CCH}	V_{CC} =MAX			29	40	mA
			I_{CCL}				32	45	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

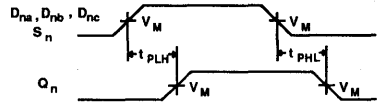
AC ELECTRICAL CHARACTERISTICS for 74F711/74F711-1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to Q_n	Waveform 1, 2	3.5 2.0	6.5 5.5	9.5 8.5	3.0 1.5	10.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay S, $\overline{INV}$ to Q_n	Waveform 1,3	8.0 5.0	11.0 9.0	14.5 12.5	6.5 5.0	17.0 13.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_n	Waveform 4 Waveform 5	3.5 3.5	5.5 6.5	8.0 9.0	2.5 2.5	9.0 10.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q_n	Waveform 4 Waveform 5	1.0 3.0	3.5 5.5	6.5 8.0	1.0 2.5	7.5 9.5	ns

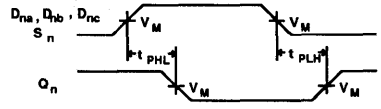
AC ELECTRICAL CHARACTERISTICS for 74F712/74F712-1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to Q_n	Waveform 1, 2	2.5 2.5	5.0 5.0	8.0 8.0	2.0 2.0	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q_n	Waveform 1	8.0 6.0	10.5 9.0	13.5 12.0	7.0 6.0	16.0 12.0	ns

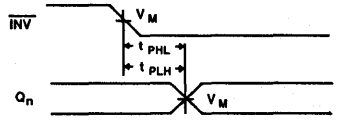
AC WAVEFORMS



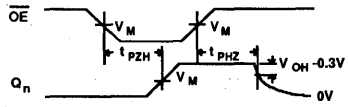
Waveform 1. Propagation Delay For Non-Inverting Output



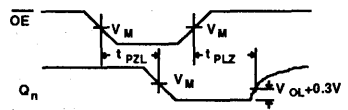
Waveform 2. Propagation Delay For Inverting Output



Waveform 3. Propagation Delay For $\overline{INV}$ To Output



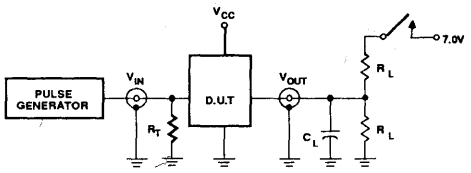
Waveform4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

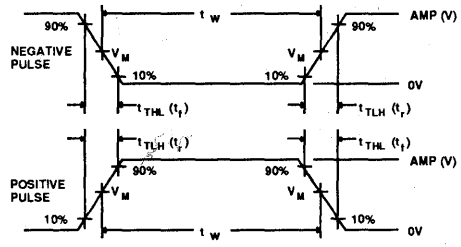
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F723/723-1, 74F725/725-1

FAST Products

Multiplexers

74F723 Quad 3-to-1 Data Selector Multiplexer (3-State)
74F723-1 Quad 3-to-1 Data Selector Multiplexer With 30 ohm Series Termination Resistors (3-State)
74F725 Quad 4-to-1 Data Selector Multiplexer
74F725-1 Quad 4-to-1 Data Selector Multiplexer With 30 ohm Series Termination Resistors

Preliminary Specification for 74F723 and 74F725
Product Specification for 74F723-1 and 74F251-1

FEATURES for 74F723/723-1

- Consists of four 3-to-1 Multiplexers
- High impedance PNP base inputs for reduced loading (20μA in High and Low states)
- Inverting or non-inverting data path capability by an Inverting ($\overline{INV}$) input
- Designed for address multiplexing of dynamic RAM and other applications
- Multiple side pins for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)
- 3-State outputs sink 64mA ('F723 only)
- 30 ohm output series termination resistor option-74F723-1

FEATURES for 74F725/725-1

- Consists of four 4-to-1 Multiplexers
- High impedance PNP base inputs for reduced loading (20μA in High and Low states)
- Equivalent to two 'F253s without 3-state
- Outputs sink 64mA ('F725 only)
- 30 ohm output series termination resistor option-74F725-1

DESCRIPTION

The 74F723/723-1 consists of four 3-to-1 multiplexers designed for address multiplexing for dynamic RAMs and other multiplexing applications. Select (S_0,S_1)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F723	5.5ns	23mA
74F723-1	7.5ns	33mA
74F725	6.0ns	16mA
74F725-1	7.0ns	20mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300 mil)	N74F723N, N74F723-1N, N74F725N, N74F725-1N
24-Pin Plastic SOL	N74F723D, N74F723-1D, N74F725D, N74F725-1D

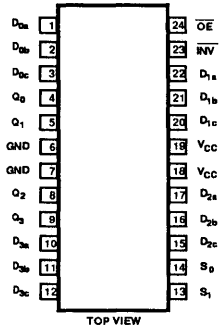
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

TYPE	PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F723/ 'F723-1	D_{na}, D_{nb}, D_{nc}	Data inputs	1.0/0.033	20μA/20μA
	S_0, S_1	Select inputs	1.0/0.033	20μA/20μA
	$\overline{INV}$	Output Inverting input	1.0/0.033	20μA/20μA
	$\overline{OE}$	Output Enable input	1.0/0.033	20μA/20μA
'F723	Q_0 - Q_3	Data outputs	750/106.7	15mA/64mA
'F723-1	Q_0 - Q_3	Data outputs	600/8.33	12mA/5mA
'F725/ 'F725-1	D_{na}, D_{nb}, D_{nc}, D_{nc}	Data inputs	1.0/0.033	20μA/20μA
	S_0, S_1	Select inputs	1.0/0.033	20μA/20μA
'F725	Q_0 - Q_3	Data outputs	750/106.7	15mA/64mA
'F725-1	Q_0 - Q_3	Data outputs	600/8.33	12mA/5mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

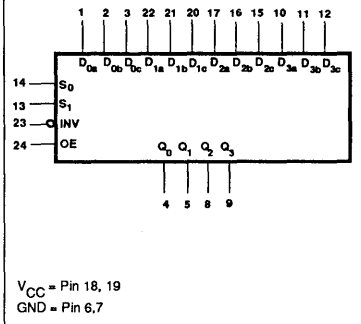
'F723/'F723-1



TOP VIEW

LOGIC SYMBOL

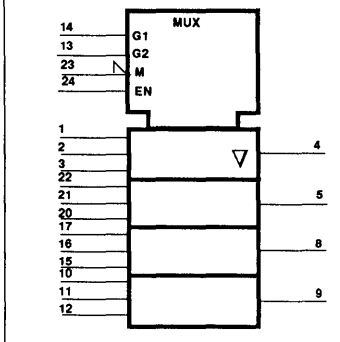
'F723/'F723-1



V_{CC} = Pin 18, 19
GND = Pin 6,7

LOGIC SYMBOL(IEEE/IEC)

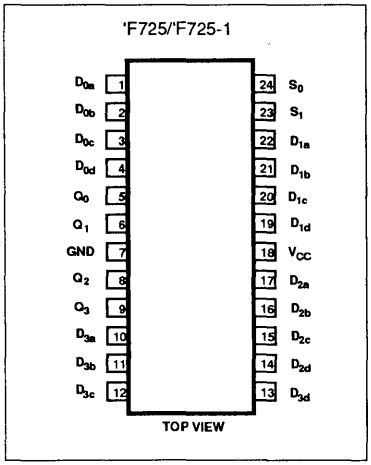
'F723/'F723-1



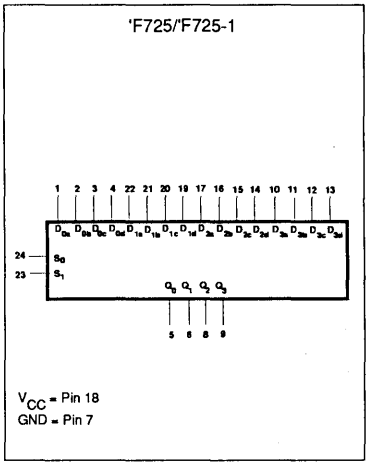
Multiplexers

FAST 74F723/723-1, 74F725/725-1

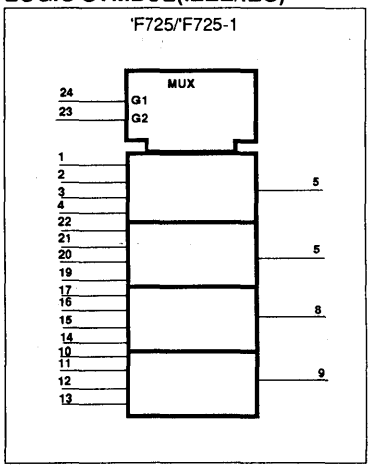
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

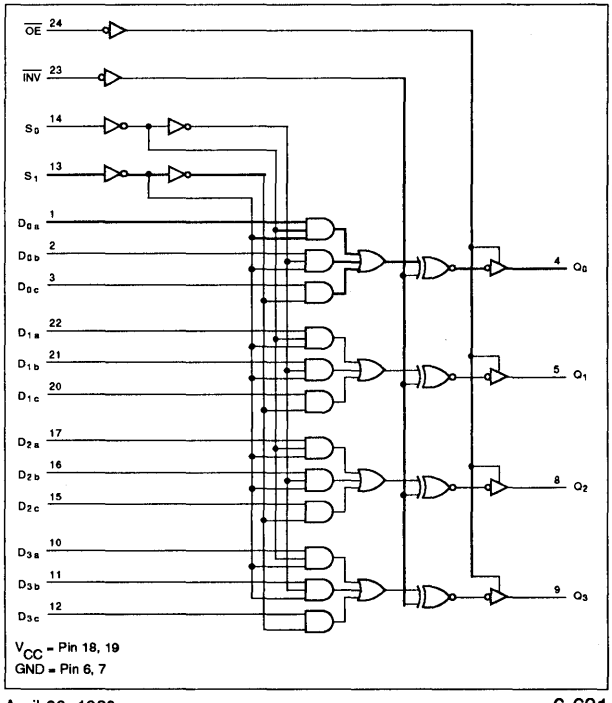


inputs control which line is to be selected, as defined in the Function Table for 'F723/723-1. The inverting ($\overline{INV}$) input, when Low, changes data path to inverting.

To improve speed and noise immunity, V_{CC} and GND side pins are used. The 3-state outputs sorrce 15mA and sink 64mA. The 74F723-1 is same as 74F723 except that it has a 30 ohm series termination resistor on each output to reduce line noise and the 3-state outputs source 12mA and sink 5mA.

The 74F725/725-1 consists of four 4-to-1 multiplexers designed for general multiplexing purpose. The select (S_0,S_1) inputs control which line is to be selected, as defined in the Function Table for 'F725/725-1. The outputs source 15mA and sink 64mA. The 74F725-1 is same as the 74F725 except that it has a 30 ohm series termination resistor on each output to reduce line noise and the outputs source 12mA and sink 5mA.

LOGIC DIAGRAM for 'F723/'F723-1

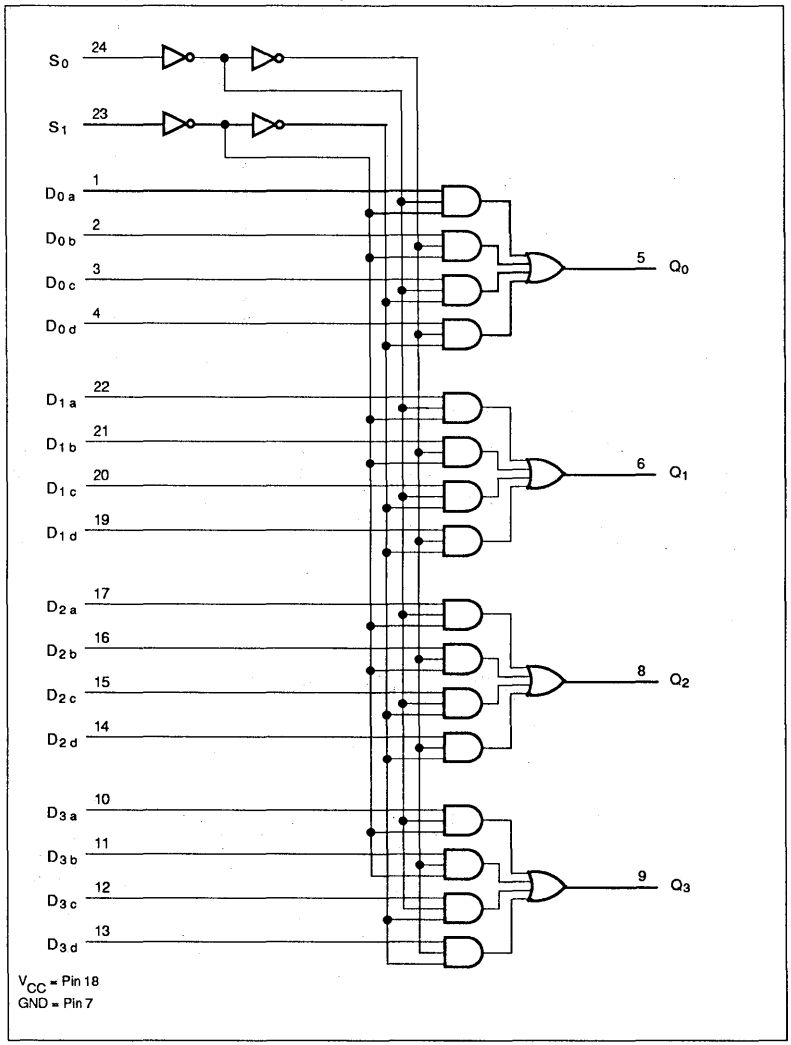


FUNCTION TABLE for 'F723/'F723-1

INPUTS							OUTPUT
S_0	S_1	$\overline{INV}$	$\overline{OE}$	D_{na}	D_{nb}	D_{nc}	Q_n
L	L	L	L	data a	data b	data c	$\overline{\text{data a}}$
L	L	H	L	data a	data b	data c	data a
H	L	L	L	data a	data b	data c	$\overline{\text{data b}}$
H	L	H	L	data a	data b	data c	data b
X	H	L	L	data a	data b	data c	$\overline{\text{data c}}$
X	H	H	L	data a	data b	data c	data c
X	X	X	H	X	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM for 'F725/'F725-1



FUNCTION TABLE for 'F725/'F725-1

INPUTS						OUTPUT
S_0	S_1	D_{na}	D_{nb}	D_{nc}	D_{nd}	Q_n
L	L	data a	data b	data c	data d	data a
H	L	data a	data b	data c	data d	data b
L	H	data a	data b	data c	data d	data c
H	H	data a	data b	data c	data d	data d

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	'F723-1, 'F725=1	10	mA
		'F723, 'F725	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	'F723-1, 'F725-1			-12	mA
		'F723, 'F725			-15	mA
I_{OL}	Low-level output current	'F723-1, 'F725-1			5	mA
		'F723, 'F725			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	'F723/ 'F723-1 'F725/ 'F725-1	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		'F723-1/ 'F725-1		I_{OH}=-12mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
		'F723/ 'F725		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	'F723-1/ 'F725-1	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=5mA	±10%V_{CC}		0.38	0.55	V
					±5%V_{CC}		0.38	0.55	V
		'F723/ 'F725		I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximun input voltage		V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} =MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} =MAX, V_I = 0.5V					-20	µA
I_{OZH}	Off-state output current High-level voltage applied	'F723/ 'F723-1 only	V_{CC} =MAX, V_O= 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} =MAX, V_O= 0.5V					-50	µA
I_{OS}	Short circuit output current[3]	'F723/'F725	V_{CC} =MAX			-100		-225	mA
		'F723-1/ 'F725-1				-60		-150	mA
I_{CC}	Supply current (total)	'F723 I_{CCH}	V_{CC} =MAX				19	30	mA
		'F723 I_{CCL}					24	35	mA
		'F723 I_{CCZ}					29	35	mA
		'F723-1 I_{CCH}					33	45	mA
		'F723-1 I_{CCL}					33	45	mA
		'F723-1 I_{CCZ}					35	50	mA
		'F725 I_{CCH}					17	35	mA
		'F725 I_{CCL}					20	40	mA
		'F725-1 I_{CCH}					17	35	mA
		'F725-1 I_{CCL}					20	40	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

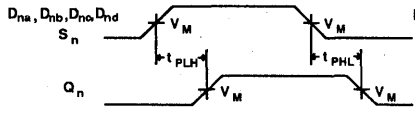
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to Q_n	'F723	Waveform 1, 2	1.5 1.5	3.5 3.5	6.0 6.0	1.5 1.5	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1, $\overline{INV}$ to Q_n		Waveform 1, 2	2.0 2.0	6.5 6.5	9.5 9.5	2.0 2.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_n		Waveform 4 Waveform 5	2.0 2.0	4.0 4.0	7.0 7.0	2.0 2.0	8.0 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q_n		Waveform 4 Waveform 5	1.5 1.5	3.0 4.0	6.0 6.0	1.5 1.5	6.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc} to Q_n	'F723-1	Waveform 1, 2	3.0 3.0	6.5 5.5	9.0 8.5	3.0 2.5	10.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1, $\overline{INV}$ to Q_n		Waveform 1, 2	7.0 5.0	10.5 9.5	14.0 12.5	6.0 5.0	16.0 13.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Q_n		Waveform 4 Waveform 5	3.0 4.0	5.0 6.0	8.0 9.0	2.5 3.5	8.5 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Q_n		Waveform 4 Waveform 5	2.0 3.5	3.5 5.0	6.5 8.0	1.0 3.0	7.5 8.5	ns

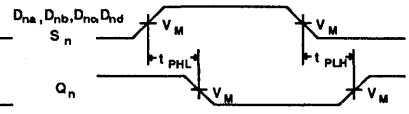
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd} to Q_n	'F725	Waveform 1, 2	3.0 3.0	5.5 5.0	8.0 8.0	2.5 2.5	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q_n		Waveform 1	8.0 6.5	10.5 8.5	13.5 11.5	7.0 6.0	15.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd} to Q_n	'F725-1	Waveform 1, 2	3.0 3.0	5.5 5.0	8.0 8.0	2.5 2.5	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to Q_n		Waveform 1	8.0 6.5	10.5 8.5	13.5 11.5	7.0 6.0	15.5 12.0	ns

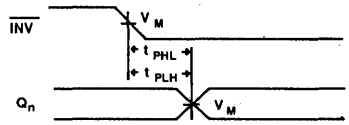
AC WAVEFORMS



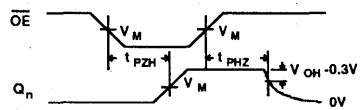
Waveform 1. Propagation Delay For Non-Inverting Output



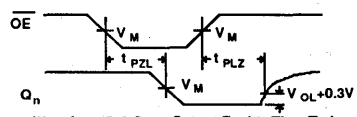
Waveform 2. Propagation Delay For Inverting Output



Waveform 3. Propagation Delay For $\overline{INV}$ To Output



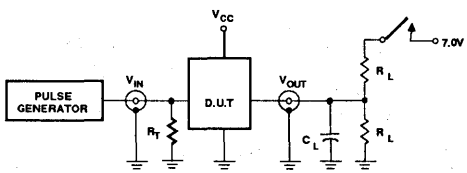
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

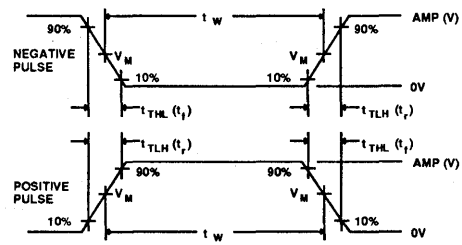
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F732, 74F733
Multiplexers

74F732 Quad Data Multiplexer, Inverting (3-State)
74F733 Quad Data Multiplexer, Non-Inverting (3-State)
Product Specification

FAST Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F732	6.0ns	65mA
74F733	6.0ns	75mA

FEATURES

- **Quad 2-to-1 Multiplexer (two busses to one bus)**
- **Data can flow in either direction between busses (A → B, A → C, B → C, B → A, C → A, C → B)**
- **A built-in "break-before-make" feature eliminates current glitches and simplifies PC board design**
- **Output Enable for each bus to allow flexible contention control**
- **3-State outputs sink 64mA**

DESCRIPTION

The 74F732/74F733 are Quad Data Multiplexers designed to provide a simple means to control the flow of bidirectional data between three data busses.

The 74F732/74F733 consist of four multiplexers. Each multiplexer has three I/O (A_n, B_n, C_n) pins and uses one Output Enable pin ($\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$). There are two Select (S_0, S_1) pins and a Direction (DIR) pin to control data flow paths for all four multiplexers.

With the Select control, data can flow in the following directions between busses: A to B, A to C, B to A, B to C, C to B, A to B and C. A built-in "break-before-make" feature eliminates current glitches common to systems using 3-State transceivers to accomplish the same function.

ORDERING INFORMATION

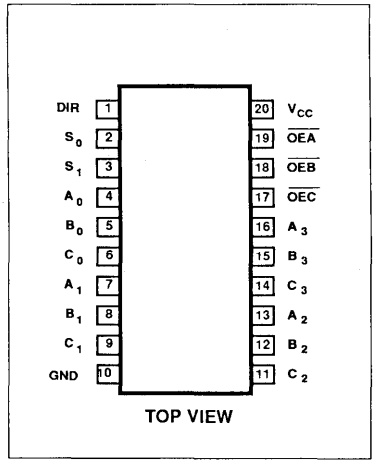
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F732N, N74F733N
20-Pin Plastic SOL	N74F732D, N74F733D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	Data inputs for Bus A	3.5/1.0	70μA/0.6mA
B_0 - B_3	Data inputs for Bus B	3.5/1.0	70μA/0.6mA
C_0 - C_3	Data inputs for Bus C	3.5/1.0	70μA/0.6mA
DIR	Direction control input	1.0/1.0	20μA/0.6mA
S_0 - S_1	Select inputs	1.0/1.0	20μA/0.6mA
$\overline{OEA}$, $\overline{OEB}$ $\overline{OEC}$	Output Enable inputs (Active Low)	1.0/1.0	20μA/0.6mA
A_0 - A_3	Data output for Bus A	750/106.7	15mA/64mA
B_0 - B_3	Data output for Bus B	750/106.7	15mA/64mA
C_0 - C_3	Data output for Bus C	750/106.7	15mA/64mA

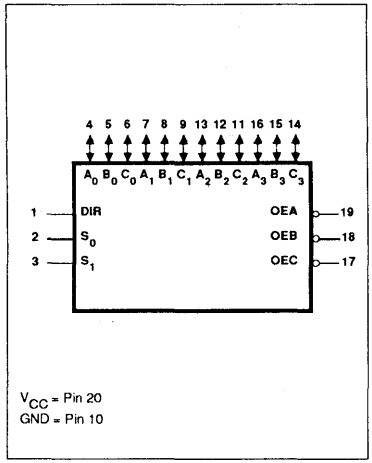
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

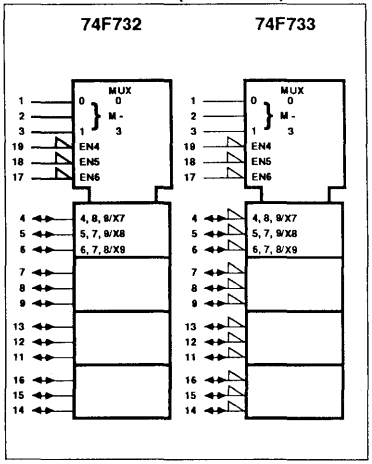


TOP VIEW

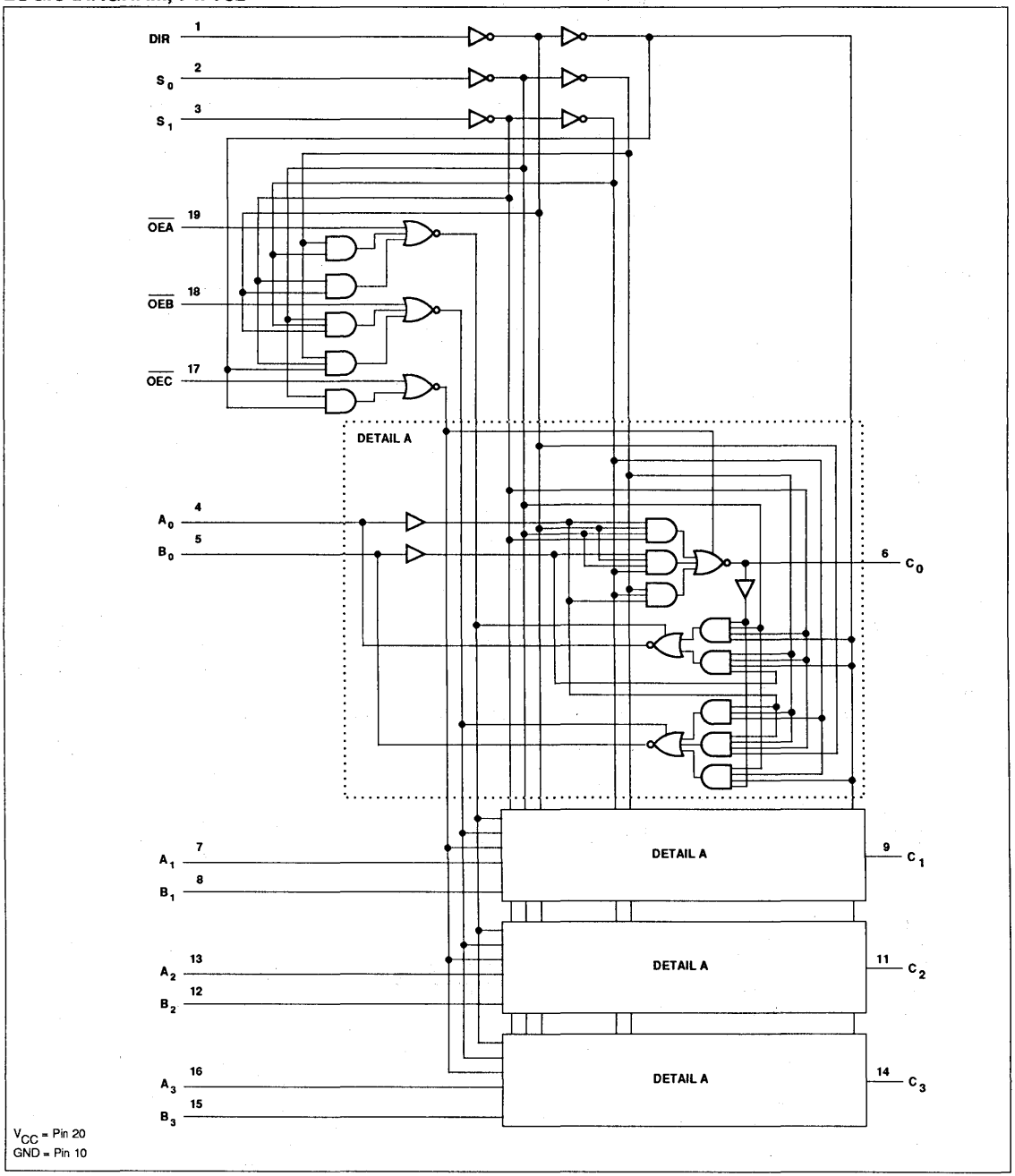
LOGIC SYMBOL



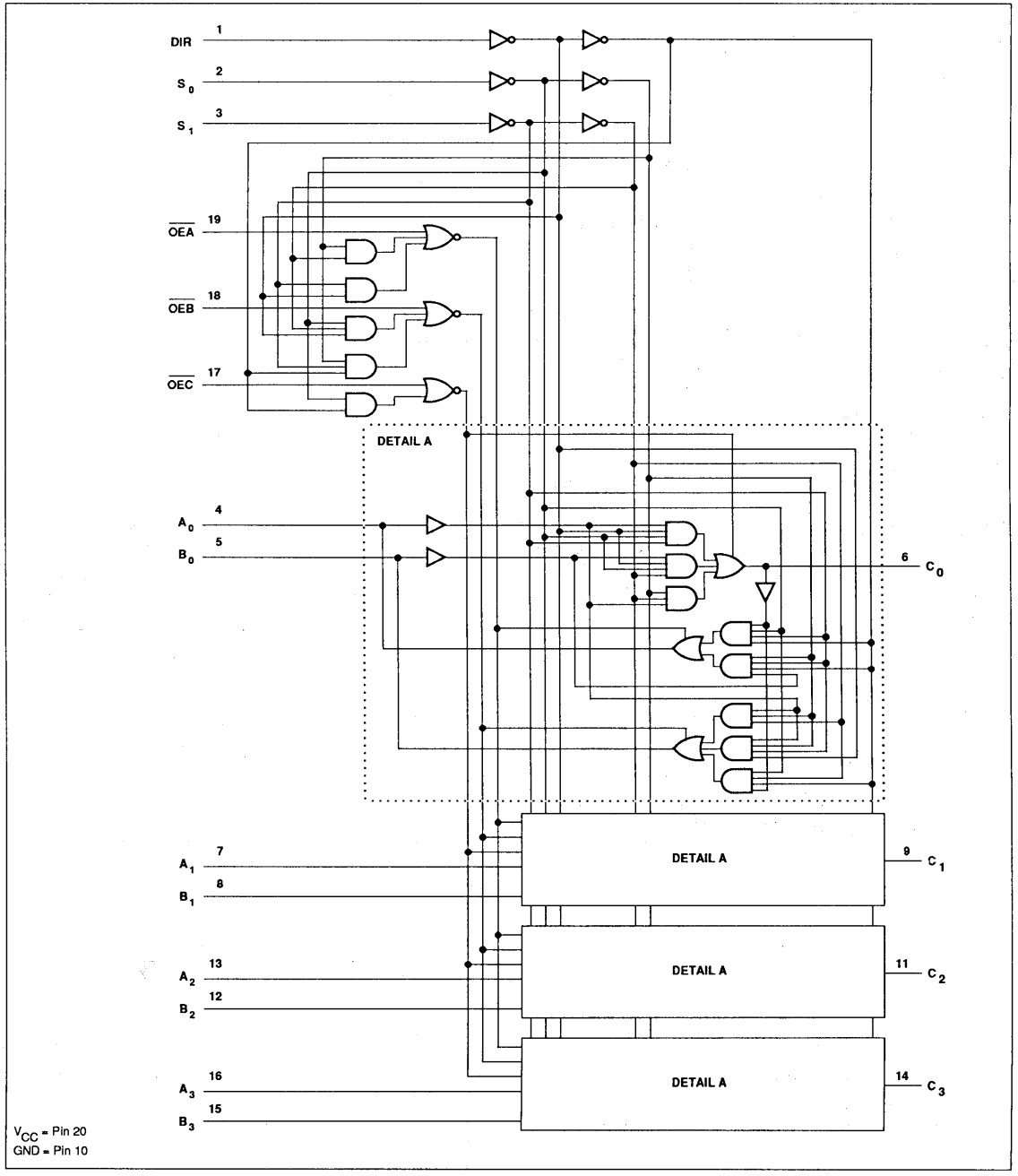
LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM, 74F732



LOGIC DIAGRAM, 74F733



FUNCTION TABLE

INPUTS						OPERATING MODE
DIR	S_0	S_1	$\overline{OEA}$	$\overline{OEB}$	$\overline{OEC}$	
X	X	X	H	X	X	Bus A disabled except for input
X	X	X	X	H	X	Bus B disabled except for input
X	X	X	X	X	H	Bus C disabled except for input
L	L	L	X	H*	L	Data flow from Bus A to Bus C
H	L	L	L	H*	X	Data flow from Bus C to Bus A
L	L	H	H*	X	L	Data flow from Bus B to Bus C
H	L	H	H*	L	X	Data flow from Bus C to Bus B
L	H	L	X	L	H*	Data flow from Bus A to Bus B
H	H	L	L	X	H*	Data flow from Bus B to Bus A
X	H	H	X	L	L	Data flow from Bus A to Bus B and Bus C
X	H	H	X	H	L	Data flow from Bus A to Bus C
X	H	H	X	L	H	Data flow from Bus A to Bus B

H = High voltage level
L = Low voltage level
X = Don't care
* = If this is not High then the corresponding outputs will be High (74F732) or Low (74F733)

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3mA	±10% V_{CC}	2.4			V
					±5% V_{CC}	2.7	3.4		V
				I_{OH} = -15mA	±10% V_{CC}	2.0			V
					±5% V_{CC}	2.0	3.1		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10% V_{CC}		0.38	0.55	V
				I_{OL} = 64mA	±5% V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	$\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ DIR, S_0, S_1	V_{CC} = MAX, V_I = 2.7 V					20	µA
I_{IL}	Low-level input current	$\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ DIR, S_0, S_1	V_{CC} = MAX, V_I = 0.5 V					-0.6	mA
I_{OZH} + I_{IH}	Off-state output current, High-level voltage applied	A_0 - A_3 B_0 - B_3 C_0 - C_3	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL} + I_{IL}	Off-state output current, Low-level voltage applied	A_0 - A_3 B_0 - B_3 C_0 - C_3	V_{CC} = MAX, V_O = 0.5V					-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	74F732	I_{CCH}	V_{CC} = MAX			55	80	mA
			I_{CCL}				75	105	mA
			I_{CCZ}				65	100	mA
		74F733	I_{CCH}	V_{CC} = MAX			70	100	mA
			I_{CCL}				80	115	mA
			I_{CCZ}				80	110	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 74F732

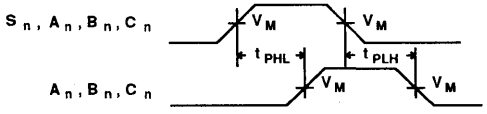
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n, C_n to A_n, B_n, C_n	Waveform 1, 2	2.0 1.0	4.5 3.0	8.0 6.0	2.0 1.0	8.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to A_n, B_n, C_n (NINV)	Waveform 1	4.5 4.5	7.0 7.0	10.0 10.0	4.0 4.0	11.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to A_n, B_n, C_n (INV)	Waveform 2	5.0 2.5	7.0 4.5	10.0 7.5	4.5 2.5	10.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time from $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3 Waveform 4	2.0 4.0	4.5 6.5	7.5 9.5	1.5 3.5	8.5 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	7.0 7.0	1.5 2.0	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time from DIR, S_0, S_1 to A_n, B_n, C_n	Waveform 3 Waveform 4	4.0 5.5	7.5 8.5	11.0 11.5	3.0 5.0	13.5 13.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from DIR, S_0, S_1 to A_n, B_n, C_n	Waveform 3 Waveform 4	1.0 1.0	6.0 4.5	9.0 7.5	1.0 1.0	10.0 8.0	ns

AC ELECTRICAL CHARACTERISTICS for 74F733

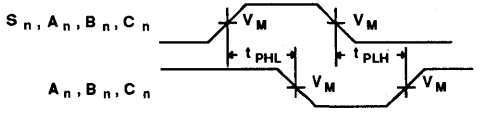
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n, C_n to A_n, B_n, C_n	Waveform 1, 2	1.5 1.5	4.0 4.0	7.0 7.0	1.0 1.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to A_n, B_n, C_n (NINV)	Waveform 1	3.0 4.0	5.0 6.0	7.5 9.0	2.5 3.5	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S_0, S_1 to A_n, B_n, C_n (INV)	Waveform 2	5.0 3.0	7.5 5.0	10.5 8.0	4.5 3.0	13.5 8.5	ns
t_{PZH} t_{PZL}	Output Enable time from $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3 Waveform 4	2.5 3.5	5.0 5.5	7.5 8.5	2.0 3.0	8.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from $\overline{OEA}$, $\overline{OEB}$, $\overline{OEC}$ to A_n, B_n, C_n	Waveform 3 Waveform 4	2.0 2.0	4.0 4.5	7.0 7.0	1.5 2.0	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time from DIR, S_0, S_1 to A_n, B_n, C_n	Waveform 3 Waveform 4	4.5 5.5	7.5 8.5	11.0 12.0	4.0 5.0	13.0 13.5	ns
t_{PHZ}* t_{PLZ}*	Output Disable time from DIR, S_0, S_1 to A_n, B_n, C_n	Waveform 3 Waveform 4	1.5 7.0	4.5 11.5	7.5 14.5	1.0 7.0	8.0 16.0	ns

* Because of the 3-state output characteristics, the pick-off point is V_{OL} +0.8V.

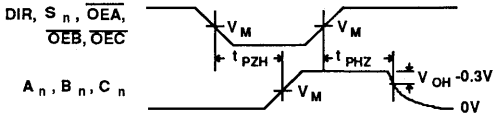
AC WAVEFORMS



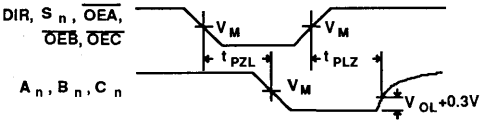
Waveform 1. Propagation Delay, Select And Data Busses



Waveform 2. Propagation Delay, Select And Data Busses



Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level

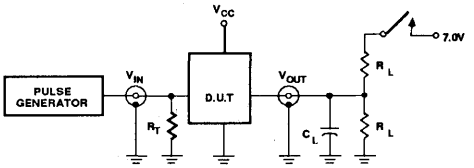


Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

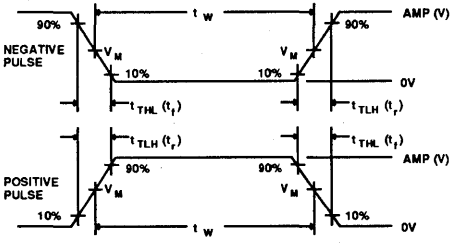
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F755
Register

FAST Products

Octal MailBox Register With Ready Flag (3-State)

Product Specification

FEATURES

- **Flag set on Write signal (if desired)**
- **Automatic flag set upon Read signal**
- **Pen collector flag status output**
- **Flag status can be read via data bus**
- **300 mil 24 pin Slim DIP plastic package option**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
N74F755	180MHz	60mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F755N
24-Pin Plastic SOL	N74F755D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

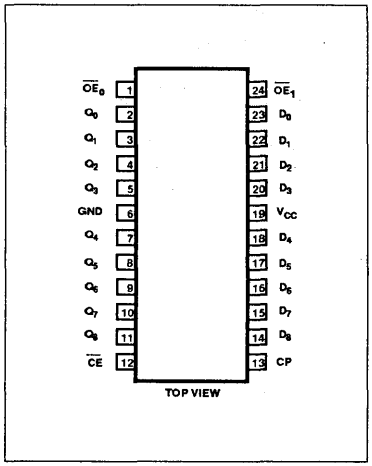
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_8	Data inputs	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/3.0	20µA/1.8mA
$\overline{CE}$	Chip Enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable inputs (active Low)	1.0/1.0	20µA/0.6mA
Q_8	Open Collector output	OC/ 40	OC/24mA
Q_0 - Q_7	Data outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC=Open Collector

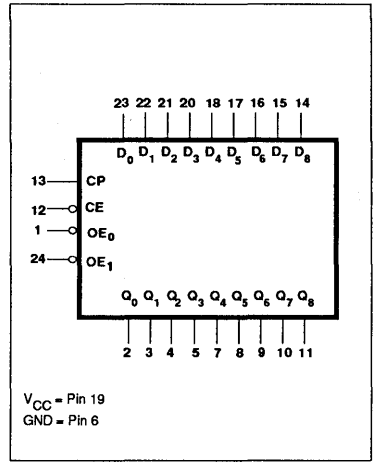
DESCRIPTION

The 74F755 is an octal three state register with simple handshaking logic. Data is latched into and read from the part in the same manner as the 'F374 or other octal registers with the exception that the 'F755 has a Clock Enable pin. Handshaking can be performed in either a polled or interrupt environment by using the D_8 input and the Q_7 or Q_8 output. D_8 is latched along with the other data bits on the rising edge of the clock, but is handled differently on the output. The status of this bit can be sampled on the Q_8 open collector output and used as an interrupt or other control function. The status of D_8 can also be sampled on the Q_7 output with the appropriate combination of $\overline{OE}_0$ and $\overline{OE}_1$ for polled operation. The D_8 register is automatically reset when Q_0-Q_7 are sampled, resetting the handshaking for the next cycle. The 'F755 is equipped with a true Clock Enable ($\overline{CE}$) pin. There are no functional restrictions on the use of the $\overline{CE}$ pin. $\overline{CE}$ may be cycled with the clock input either Low or High with no false clocks generated. The 'F755 can serve as a single chip communications channel with simple handshaking, or two can be used for a bidirectional channel.

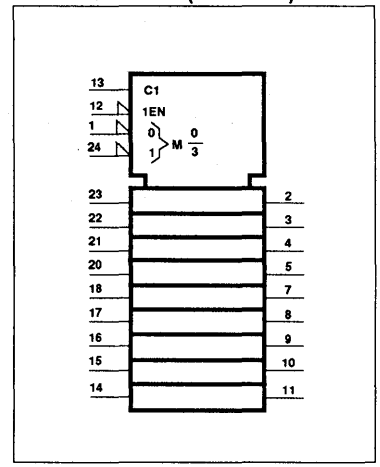
PIN CONFIGURATION



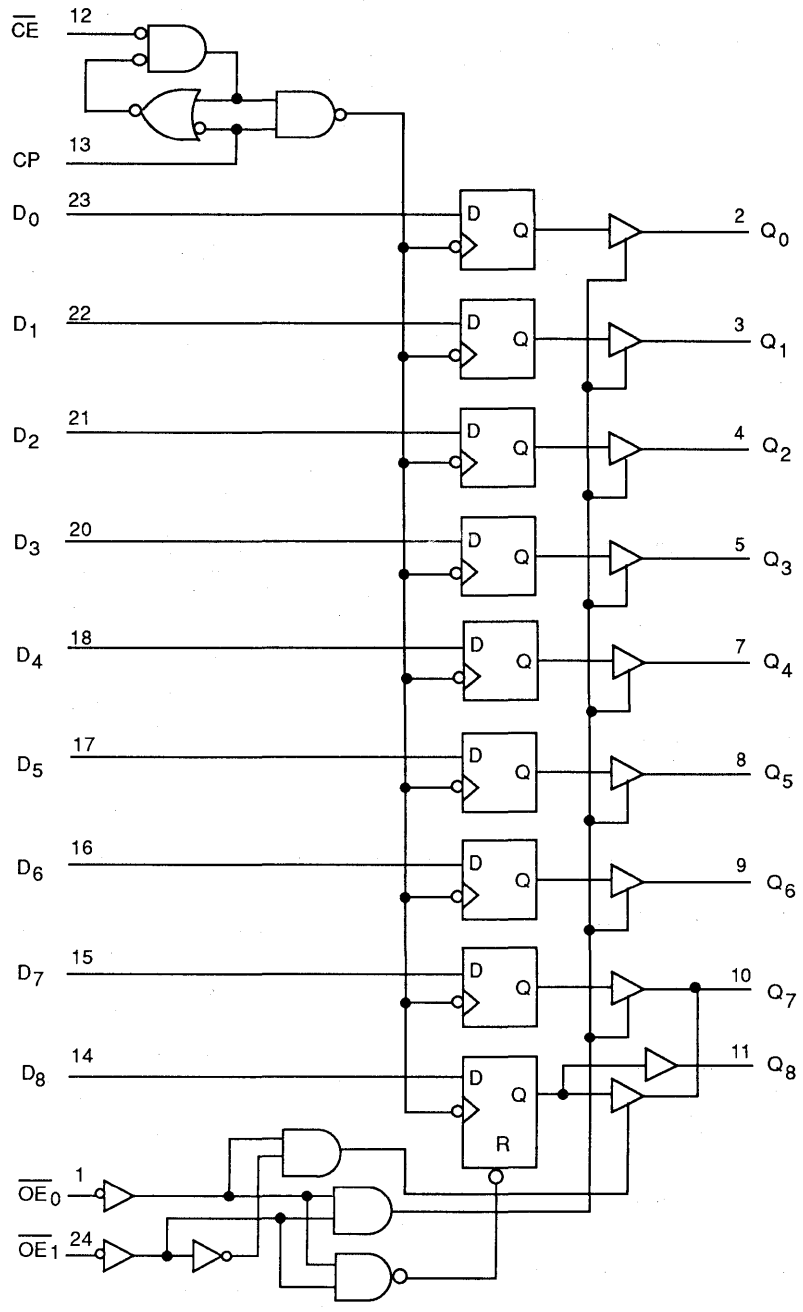
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC}=Pin 19
GND=Pin 6

FUNCTION TABLE

INPUTS						INTERNAL REGISTERS		OUTPUTS			OPERATING MODE
$\overline{OE}_0$	$\overline{OE}_1$	$\overline{CE}$	CP	D_0-D_7	D_8	Q_0-Q_7	Q_8	Q_0-Q_6	Q_7	Q_8	
H	X	L	↕	X	X	Q_0-Q_7	Q_8	Z	Z	Q_8	Hold and Read Q_8
H	X	H	X	X	X	Q_0-Q_7	Q_8	Z	Z	Q_8	
L	H	L	↕	X	X	Q_0-Q_7	Q_8	Z	Q_8	Q_8	
L	H	H	X	X	X	Q_0-Q_7	Q_8	Z	Q_8	Q_8	
L	L	L	↕	X	X	Q_0-Q_7	L	Q_0-Q_6	Q_7	L	Hold and Read (Q_0-Q_7) and reset Q_8
L	L	H	X	X	X	Q_0-Q_7	L	Q_0-Q_6	Q_7	L	
H	X	L	↑	D_0-D_7	D_8	D_0-D_7	D_8	Z	Z	D_8	Load (D_0-D_8)
L	H	L	↑	D_0-D_7	D_8	D_0-D_7	D_8	Z	D_8	D_8	
L	L	L	↑	D_0-D_7	X	D_0-D_7	L	D_0-D_6	D_7	L	Load (D_0-D_7) and reset Q_8

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
V_{OH}	High level output voltage	Q_8 only			4.5	V
I_{OH}	High-level output current	Q_0-Q_7			-3	mA
I_{OL}	Low-level output current				24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
I_{OH}	High-level output current	Q_8 only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OH}	High-level output voltage	Q_0-Q_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=MAX	±10%VCC	2.4			V
					±5%VCC	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=MAX	±10%VCC		0.35	0.50	V
					±5%VCC		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 5.5V, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V					-600	µA
		CP						-1.8	mA
I_{OZH}	Off-state output current High-level voltage applied	Q_0-Q_7	V_{CC} = MAX, V_O= 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				50	70	mA
		I_{CCL}					65	90	mA
		I_{CCZ}					60	90	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

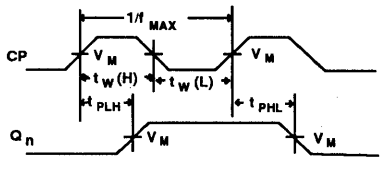
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	165	180		160		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_0-Q_7	Waveform 1	3.0 4.5	5.0 6.5	8.0 9.5	2.5 4.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_8	Waveform 1	7.5 5.0	9.5 6.5	12.0 9.5	7.5 4.5	12.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_1$ to Q_7	Waveform 2	6.0 6.5	7.5 8.5	10.5 11.0	5.0 6.5	11.5 11.5	ns
t_{PHL}	Propagation delay OE_n to Q_8 (reset)	Waveform 2	9.0	11.5	15.0	8.0	17.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_0$ to Q_0-Q_7	Waveform 4 Waveform 5	7.0 7.5	9.0 10.0	12.0 13.0	6.0 6.5	13.0 13.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_0$ to Q_0-Q_7	Waveform 4 Waveform 5	3.5 4.0	5.5 6.0	8.0 9.0	2.5 3.5	9.0 9.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_1$ to Q_0-Q_7	Waveform 4 Waveform 5	5.5 6.0	7.5 8.0	10.5 11.0	4.5 5.5	11.5 12.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_1$ to Q_0-Q_7	Waveform 4 Waveform 5	3.0 3.5	5.0 5.5	7.5 8.5	2.5 3.0	8.5 9.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_0$ to Q_7	Waveform 4 Waveform 5	9.5 10.5	11.0 12.5	14.0 15.0	8.5 9.5	16.0 17.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_0$ to Q_7	Waveform 4 Waveform 5	3.5 3.5	5.0 5.5	8.0 8.0	2.5 3.5	8.5 8.5	ns

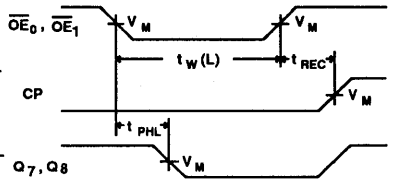
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 3	3.5 3.0			4.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CE}$ to CP	Waveform 3	0.0 0.0			0.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP	Waveform 3	2.0 3.0			2.5 3.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	3.0 3.5			3.0 4.0		ns
$t_w(L)$	$\overline{OE}_0$ Pulse width,Low	Waveform 2	6.5			8.5		ns
$t_w(L)$	$\overline{OE}_1$ Pulse width, Low	Waveform 2	5.5			6.5		ns
t_{REC}	Recovery time, $\overline{OE}_n$ to CP	Waveform 2	5.0			5.5		ns

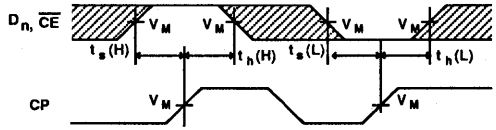
AC WAVEFORMS



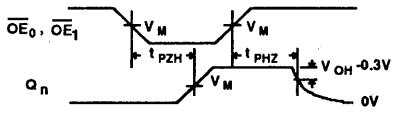
Waveform 1.
Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



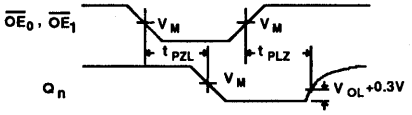
Waveform 2. Output Enables Pulse Width, Output Enables to Q8 Output Delay and Output Enables to Clock ad Chip Enable Recovery Time



Waveform 3. Data Setup And Hold Times



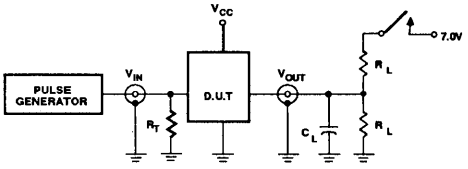
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

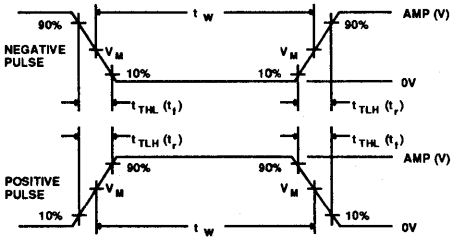
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F756, 74F757, 74F760 Buffers

FAST Products

74F756 Octal Inverter Buffer (Open Collector)
74F757 Octal Buffer (Open Collector)
74F760 Octal Buffer (Open Collector)

Product Specification

FEATURES

- **Octal bus interface**
- **Open collector versions of 74F240, 74F241 and 74F244**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F756	9.0ns	40mA
74F757	9.0ns	45mA
74F760	9.0ns	45mA

DESCRIPTION

The 74F756, 74F757 and 74F760 are octal buffers that are ideal for driving bus lines of buffer memory address registers. The 74F756 is the open collector version of 74F240, 74F757 is the open collector version of 74F241 and 74F760 is the open collector version of 74F244. These devices feature two Output Enables, $\overline{OE}_a$ and $\overline{OE}_b$ (or OE_b for the 'F757), each controlling four of the outputs.

ORDERING INFORMATION

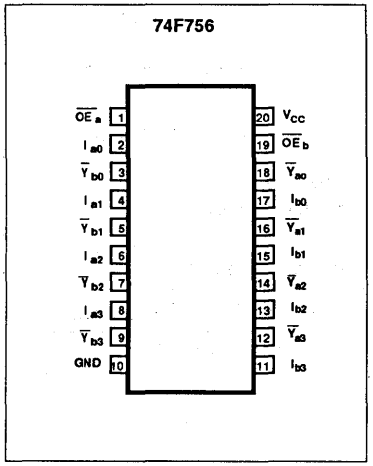
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F756N, N74F757N, N74F760N
20-Pin Plastic SOL	N74F756D, N74F757D, N74F760D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

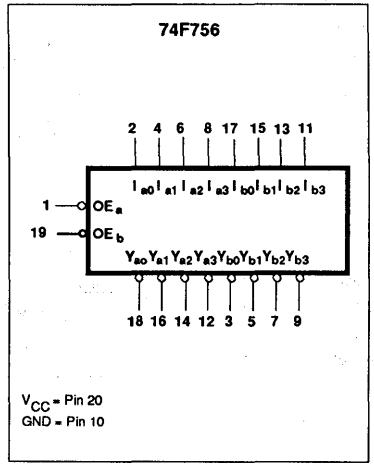
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{an}, I_{bn}	Data inputs	1.0/1.67	20µA/1.0mA
$\overline{OE}_a$ $\overline{OE}_b$	Output enable input (active Low)	1.0/1.67	20µA/1.0mA
OE_b	Output enable input (active High 'F757)	1.0/1.67	20µA/1.0mA
Y_{an}, Y_{bn}	Data outputs ('F757, 'F760)	OC/106.7	OC/64mA
$\overline{Y}_{an}$, $\overline{Y}_{bn}$	Data outputs ('F756)	OC/106.7	OC/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC= Open Collector

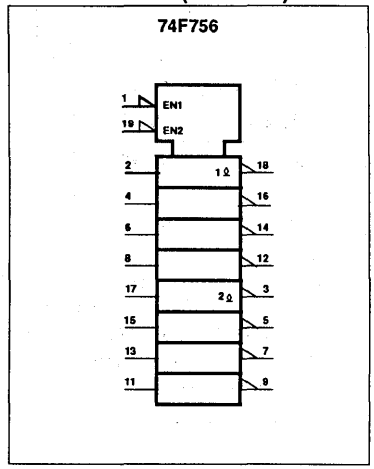
PIN CONFIGURATION



LOGIC SYMBOL

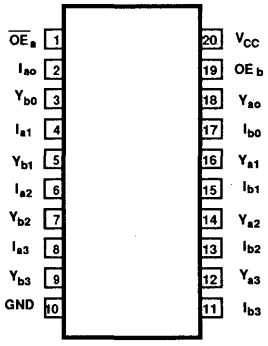


LOGIC SYMBOL(IEEE/IEC)



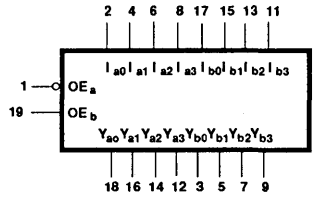
PIN CONFIGURATION

74F757



LOGIC SYMBOL

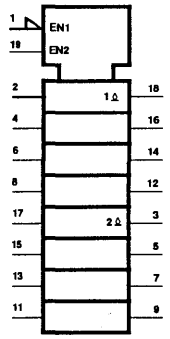
74F757



V_{CC} = Pin 20
GND = Pin 10

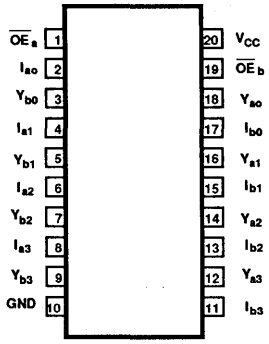
LOGIC SYMBOL(IEEE/IEC)

74F757



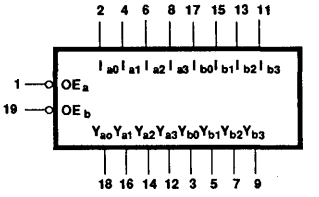
PIN CONFIGURATION

74F760



LOGIC SYMBOL

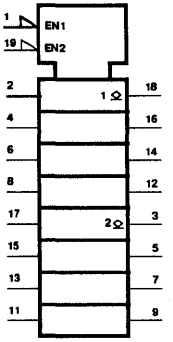
74F760



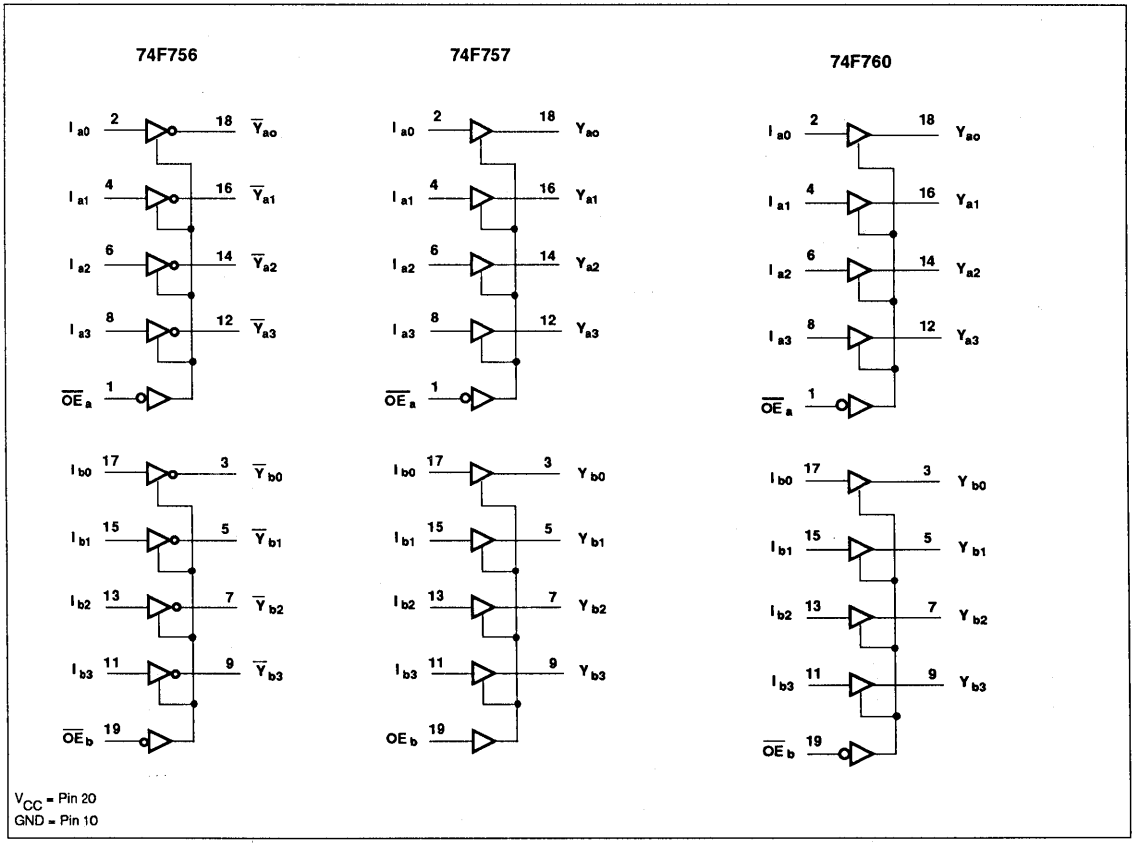
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)

74F760



LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE, 74F756

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_a$	$\overline{Y}_b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	H(off)	H(off)

FUNCTION TABLE, 74F757

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_a	Y_b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	H(off)	H(off)

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE, 74F760

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	H(off)	H(off)

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER				UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_K	Input clamp current			-18	mA
V_{OH}	High level output voltage			4.5	V
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
I_{OH}	High-level output current			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
					I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-1.0	mA
I_{CC}	Supply current (total)	74F756	I_{CCH}	V_{CC} = MAX				20	30	mA
			I_{CCL}					50	70	mA
		74F757	I_{CCH}					30	40	mA
			I_{CCL}					55	80	mA
		74F760	I_{CCH}					25	37	mA
			I_{CCL}					55	80	mA

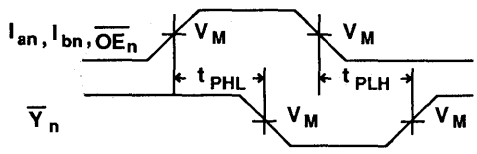
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

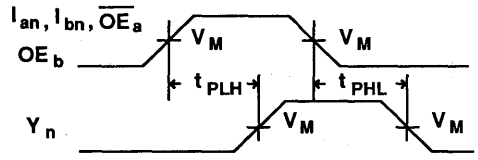
AC ELECTRICAL CHARACTERISITICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to $\overline{Y}_n$	74F756	Waveform 1, 2	8.5 1.0	11.0 3.0	14.0 6.0	8.5 1.0	15.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_n$ to $\overline{Y}_n$		Waveform 1, 2	9.0 5.0	11.5 7.0	14.5 10.0	9.0 4.5	15.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to Y_n	74F757	Waveform 1, 2	7.5 3.0	10.5 5.5	13.5 8.5	7.5 3.0	14.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_a$ or OE_b to Y_n		Waveform 1, 2	9.5 4.5	12.5 7.0	16.5 10.0	9.0 4.0	17.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to Y_n	74F760	Waveform 1, 2	7.5 3.5	10.0 5.5	13.5 8.5	7.5 3.0	14.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_n$ to Y_n		Waveform 1, 2	9.5 5.0	11.5 7.0	14.5 10.0	9.0 4.5	15.0 10.5	ns

AC WAVEFORMS



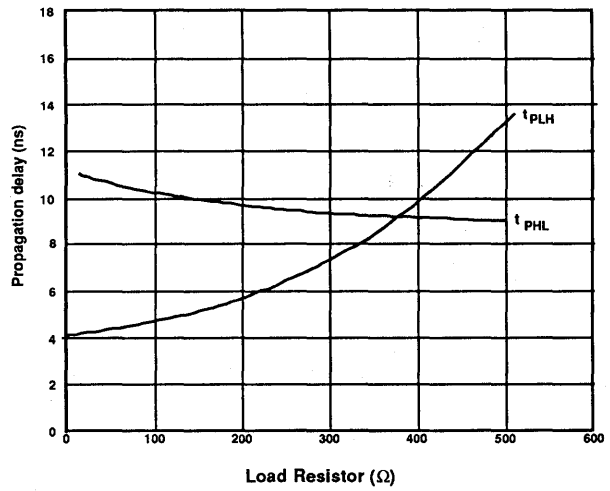
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs

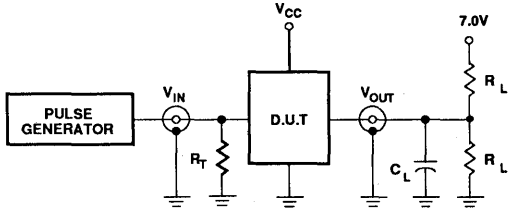
NOTE: For all waveforms, V_M = 1.5V.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

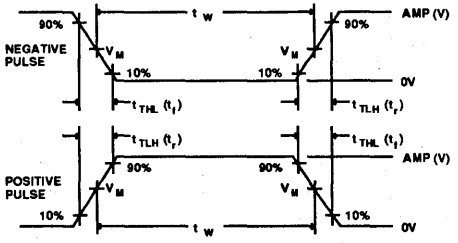


NOTE:
When using open-collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the pull-up resistor value from 500 Ω to 100Ω will improve the t_{PLH} up to 50% with only slight increase in the t_{PHL}. However, if the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers do not exceed the I_{oL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F764/765, 74F764A/765A, 74F764-1/765-1
DRAM Dual-Ported Controllers

This document contains Product specifications for the 74F764/765 and 74F764-1/765-1, and Preliminary specification for the 74F764A/765A

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F764/765	150MHz	150mA
74F764A/765A	175MHz	150mA
74F764-1/765-1	150MHz	125mA

FEATURES

- **Allows two microprocessors to access the same bank of dynamic RAM**
- **Performs arbitration, signal timing, address multiplexing, and refresh**
- **9 address output pins allow direct control of up to 256K dynamic RAMS**
- **External address multiplexing enables control of 1Mbit (or greater) dynamic RAMs**
- **Separate refresh clock allows adjustable refresh timing**
- **F764/F764A/F764-1 have on-chip 18-bit address input latch**
- **F764/765, F764-1/765-1 allow control of dynamic RAMs with row access times down to 40ns**
- **F764A/765A allow control of dynamic RAMs with row access times down to 30ns**
- **F764/765, F764A/765A output drivers designed for incident wave switching**
- **F764-1/765-1 output drivers designed for first reflected wave switching**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%, T_A = 0°C to +70°C
Plastic DIP	74F764N, 74F765N, 74F764AN, 74F765AN, 74F764-1N, 74F765-1N
PLCC-44	74F764A, 74F765A, 74F764AA, 74F765AA, 74F764-1A, 74F765-1A

DESCRIPTION

The 74F764/765 DRAM Dual-ported Controller is a High-speed synchronous dual-port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing device to share the same block of DRAM. The device performs arbitration, signal timing, address multiplexing, and refresh address generation, replacing up to 25 discrete devices.

74F764 vs 74F765

The F764, though functionally and pin-to-pin compatible with the F765, differs from the later in that it has an on-chip address input latch. This is useful in systems that have unlatched or multiplexed address and data bus.

74F764/765 vs 74F764A/765A

The 74F764A/765A is a faster version of the F764/765. The F764/765, rated at a maximum clock frequency of 100MHz, can control dynamic RAMs with row access times down to 40ns. The F764A/765A devices on the other hand are rated at 150MHz which translates to control of 30ns dynamic RAMs.

74F764/765, 74F764A/765A vs 74F764-1/765-1

The 74F764-1/765-1, though as fast as the 74F764/765, differs from the 74F764/765 and 74F764A/765A in the following respects:

a) they reduce the row address hold time by half-a-clock cycle, and
b) their outputs are optimized for first reflected wave switching as opposed to incident wave switching.

The specialized outputs eliminate the need for signal terminations inessentially all applications.

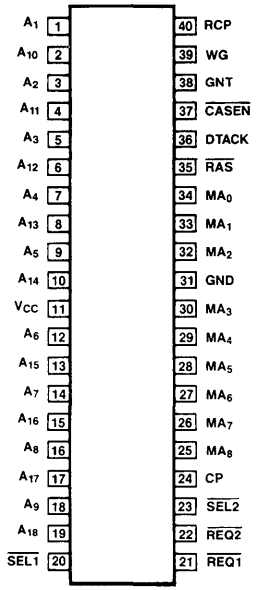
All devices are available in 40-pin plastic DIP or 44-pin PLCC with pinouts designed to allow convenient placement of microprocessors, DRAMs, and other support chips.

DRAM Dual-Ported Controllers

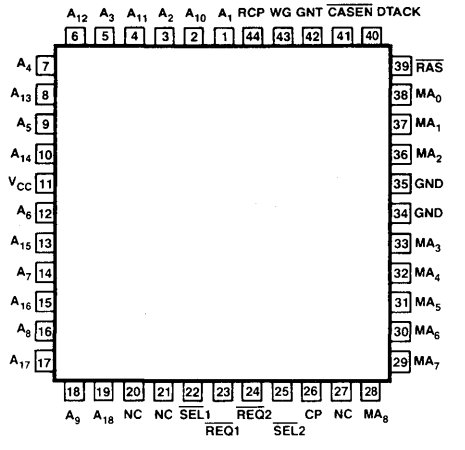
FAST 74F764/765, 74F764A/765A, 74F764-1/765-1

PIN CONFIGURATION

N Package

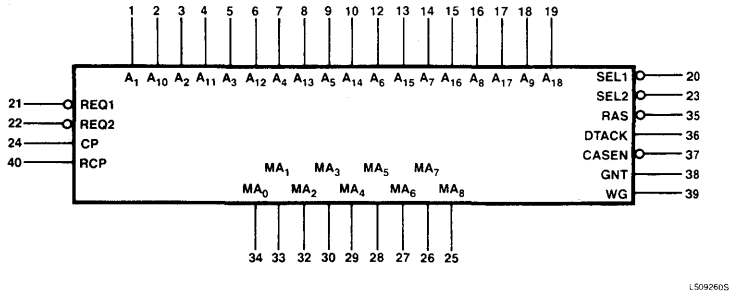


A Package



LOGIC SYMBOL

N Package



V_{CC} = Pin 11
GND = Pin 31

PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A_1	1	1	I	Address inputs used to generate memory row address
A_2	3	3	I	
A_3	5	5	I	
A_4	7	7	I	
A_5	9	9	I	
A_6	12	12	I	
A_7	14	14	I	
A_8	16	16	I	
A_9	18	18	I	
A_{10}	2	2	I	Address inputs used to generate memory column address
A_{11}	4	4	I	
A_{12}	6	6	I	
A_{13}	8	8	I	
A_{14}	10	10	I	
A_{15}	13	13	I	
A_{16}	15	15	I	
A_{17}	17	17	I	
A_{18}	19	19	I	
$\overline{REQ}_1$	21	23	I	Memory access request from Microprocessor 1
$\overline{REQ}_2$	22	24	I	Memory access request from Microprocessor 2
CP	24	26	I	Clock input which determines the master timing
RCP	40	44	I	Refresh clock determines the period of refresh for each row after it is internally divided by 64
$\overline{SEL}_1$	20	22	O	Select signal is activated in response to active $\overline{REQ}_1$ input, indicating selection of Microprocessor 1
V_{CC}	11	11		Power supply +5V ±10%
GND	31	34 35		Ground
$\overline{SEL}_2$	23	25	O	Select signal is activated in response to active $\overline{REQ}_2$ input, indicating selection of Microprocessor 2
MA_0	34	38	O	Memory address output pins, designed to drive address lines of the DRAM
MA_1	33	37	O	
MA_2	32	36	O	
MA_3	30	33	O	
MA_4	29	32	O	
MA_5	28	31	O	
MA_6	27	30	O	
MA_7	26	29	O	
MA_8	25	28	O	
GNT	38	42	O	Grant output, activated upon start of a memory access cycle
$\overline{RAS}$	35	39	O	Row address strobe, used to latch the row address into the bank of DRAM (to be connected directly to the $\overline{RAS}$ inputs of the DRAMs)
WG	39	43	O	Write Gate may be gated with the microprocessor's write strobe to perform an early write cycle
$\overline{CASEN}$	37	41	O	Column Address Strobe Enable is used to latch the column address into the bank of DRAMs
DTACK	36	40	O	Data Transfer Acknowledge indicates that data on the DRAM output lines is valid or the proper access time has been met

DRAM Dual-Ported Controllers

FAST 74F764/765, 74F764A/765A, 74F764-1/765-1

ARCHITECTURE

The 74F764/765 DRAM dual-ported controller is a synchronous device, with all signal generation being a function of the input clock (CP).

The 'F764/765 arbitration logic is divided into two stages. The first stage controls which one of the two $\overline{REQ}$ inputs will be serviced by activating the corresponding $\overline{SEL}$ output. This arbitration takes place irrespective of whether or not a refresh cycle is in progress. The arbitration is accomplished by sampling the $\overline{REQ}_1$ and $\overline{REQ}_2$ inputs on different edges of the CP clock. $\overline{REQ}_1$ is sampled on the rising edge and $\overline{REQ}_2$ on the falling edge (refer to Figures 1 – 4).

Therefore, if access to the DRAM is requested by both processors at the same time, the contention is automatically resolved. The internal flip-flops of the device used in the arbitration process have been chosen for their immunity to metastable conditions.

The second stage of arbitration selects between the selected processor and any internal refresh request. Refresh always has priority and is serviced immediately after the current cycle is completed (if needed). This arbitration stage also indicates the start of an access cycle by asserting the GNT output.

The Refresh Clock (RCP) input determines the period for each row. This clock may be held in the High state for external or no refresh applications. When used, a refresh request is internally generated every 64 RCP cycles. The refresh counter is incremented at the end of every refresh cycle, and provides the refresh address.

Since $\overline{SEL}$ outputs indicate which one of the two memory accessing devices has been selected to be serviced, these provide an indication of which processor's address bus should be asserted at the controller address inputs. A Data Transfer Acknowledge (DTACK) signal is generated by the timing logic and either this signal or GNT may be used with the $\overline{SEL}$ outputs to indicate the end or beginning of an access cycle for each processor.

FUNCTIONAL DESCRIPTION

As described earlier, the timing, arbitration, refresh and multiplexing functions provided by the controller are all derived from the CP input. The period of this clock for the F764/765 and F764A/765A should be set equal to: (Tras(of the DRAM) + 16 – 5)/4ns plus any system guard-band required.

For the F764-1/765-1 the CP clock input period should be equal to:
(Tras(of the DRAM) + 22 – 10)/4ns plus any system guard-band required.

A microprocessor requests access to the DRAM by activating the appropriate $\overline{REQ}$ input. If a refresh cycle is not in process and the other request input is not active, the $\overline{SEL}$ output corresponding to the active $\overline{REQ}$ input will be asserted to indicate the selected processor. The GNT output then goes High to indicate the start of a memory access cycle. If however, a refresh cycle is in process, and there is only one active $\overline{REQ}$ input, the $\overline{SEL}$ output corresponding to the active input $\overline{REQ}$ will be asserted but the GNT output will not go High until after the completion of the refresh cycle (see Figures 10, 11, 14 and 15).

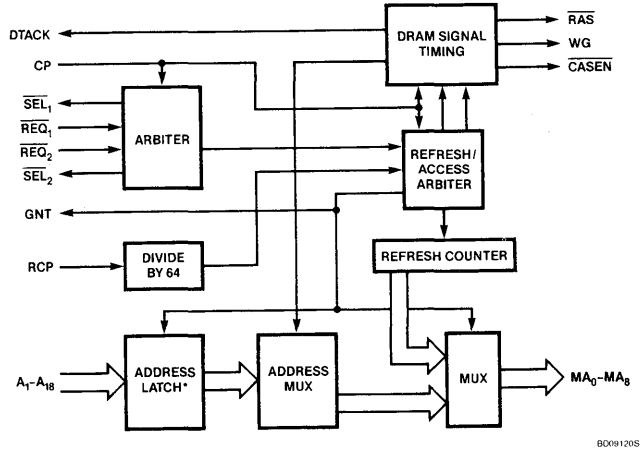
When the device is servicing a memory access cycle and a memory access is also requested by the other processor before the current cycle is completed, the $\overline{SEL}$ output for the other processor will not be issued, though GNT is asserted at that time, because the other processor is performing an access cycle. This will ensure that there is no contention on the address bus, i.e., the address bus is not driven by both processors at the same time.

Following the completion of the current memory access cycle, the $\overline{SEL}$ output corresponding to the awaiting $\overline{REQ}$ input will be asserted, followed by the GNT output. If however, there were any pending refresh requests, assertion of the GNT output will be held OFF until the refresh request has been serviced.

When GNT goes High, the $A_1 - A_{18}$ address inputs to the 'F764/F764A/F764-1 are latched internally and the $A_1 - A_9$ signals are propagated to the $MA_0 - MA_8$ outputs. The address inputs are not latched by the 'F765/F765A/F765-1 and therefore, $A_1 - A_9$ inputs propagate directly to the $MA_0 - MA_8$ outputs.

A half-clock cycle is allowed for the address signals to propagate through to the outputs, after which the $\overline{RAS}$ output is asserted.

BLOCK DIAGRAM



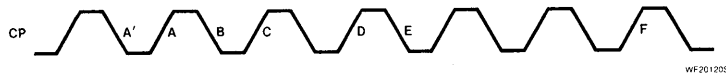
NOTE:
* The address input latch is available only on the 74F764, 74F764A, and 74F764-1.

One clock cycle later, the $A_{10} - A_{18}$ latch outputs on the 'F764/F764A or $A_{10} - A_{18}$ inputs to the 'F765/F765A are selected and propagated to the $MA_0 - MA_8$ outputs. This occurs half a clock cycle earlier on the F764-1/765-1 (refer to Figures 3 and 4). The Write Gate (WG) output becomes valid at this time to indicate the proper time to gate the Write signal from the selected processor to the DRAM to perform an Early Write cycle.

A half-clock cycle is again allowed for the $A_{10} - A_{18}$ signals to propagate and stabilize. $\overline{CASEN}$ then becomes valid. $\overline{CASEN}$ can be used as $\overline{CAS}$ output or decoded with Higher-order address signals to produce multiple $\overline{CAS}$ signals. After $\overline{CASEN}$ is valid, the controller will wait for 2½ clock cycles before negating $\overline{RAS}$, making a total $\overline{RAS}$ pulse width of approximately 4 clock cycles. Since this width matches the standard DRAM access time, the controller next asserts DTACK output, indicating that valid data is on the DRAM data lines or that a memory access cycle is complete. DTACK may be used to assert valid data transfer acknowledge for processors requiring this signal (i.e., the 68000 family of processors).

All controller output signals are held in this final state until the selected processor withdraws its request by driving its $\overline{REQ}$ input High. When the request is withdrawn, internal synchronization takes place, the controller output signals become inactive, and any pending memory access or refresh cycles are serviced.

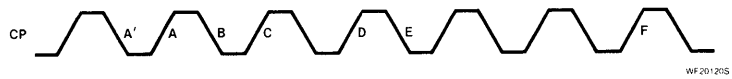
A refresh cycle is serviced by propagating the 9 refresh counter address signals to the $MA_0 - MA_8$ outputs. After a half-clock cycle the $\overline{RAS}$ output is asserted for four cycles and then negated for three clock cycles to meet the $\overline{RAS}$ precharge requirements of the DRAMs (see Figures 5 and 6).



A' $\overline{REQ}_2$ sampled
A $\overline{REQ}_1$ sampled
$\overline{SEL}_1$ triggered ($\overline{SEL}_1$ triggered by $\overline{REQ}_1$ sample circuitry) ($\overline{REQ}_2$ disabled by $\overline{SEL}_1$ circuitry)
B GNT triggered
$A_1 - A_{18}$ latched (Input address latch triggered by GNT circuitry)*
$A_1 - A_9$ propagate to $MA_0 - MA_8$ outputs
C $\overline{RAS}$ triggered
D WG triggered
$A_{10} - A_{18}$ selected and propagated to $MA_0 - MA_8$ outputs
E $\overline{CASEN}$ triggered
F $\overline{RAS}$ negated
DTACK triggered

* Only on the 'F764/F764A.

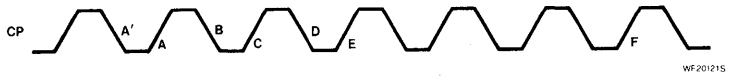
Figure 1. Sequence of Events for $\overline{REQ}_1$ Memory Access Cycle for F764/765 and F764A/765A



A' $\overline{REQ}_2$ sampled
$\overline{SEL}_2$ triggered ($\overline{SEL}_2$ triggered by $\overline{REQ}_2$ sampling circuitry)
A $\overline{REQ}_1$ is not sampled (disabled by $\overline{SEL}_2$ circuitry)
B GNT triggered
$A_1 - A_{18}$ latched (Input address latch triggered by GNT circuitry)*
$A_1 - A_9$ propagate to $MA_0 - MA_8$ outputs
C $\overline{RAS}$ triggered
D WG triggered
$A_{10} - A_{18}$ selected and propagated to $MA_0 - MA_8$ outputs
E $\overline{CASEN}$ triggered
F $\overline{RAS}$ negated
DTACK triggered

* Only on the 'F764/F764A.

Figure 2. Sequence of Events for $\overline{REQ}_2$ Memory Access Cycle for F764/765 and F764A/765A



A' $\overline{REQ}_2$ sampled

A $\overline{REQ}_1$ sampled ($\overline{REQ}_2$ disabled by $\overline{SEL}_1$ circuitry)
$\overline{SEL}_1$ triggered ($\overline{SEL}_1$ triggered by $\overline{REQ}_1$ sample circuitry)

B GNT triggered
$A_1 - A_{18}$ latched (Input address latch triggered by GNT circuitry)*
$A_1 - A_9$ propagate to $MA_0 - MA_8$ outputs

C $\overline{RAS}$ triggered

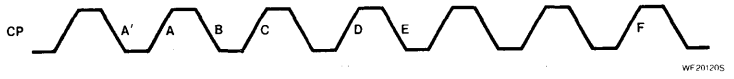
D WG triggered
$A_{10} - A_{18}$ selected and propagated to $MA_0 - MA_8$ outputs

E $\overline{CASEN}$ triggered

F $\overline{RAS}$ negated
DTACK triggered

* Only on the F764-1.

Figure 3. Sequence of Events for $\overline{REQ}_1$ Memory Access Cycle for F764-1/765-1



A' $\overline{REQ}_2$ sampled
$\overline{SEL}_2$ triggered ($\overline{SEL}_2$ triggered by $\overline{REQ}_2$ sampling circuitry)

A $\overline{REQ}_1$ is not sampled (disabled by $\overline{SEL}_2$ circuitry)

B GNT triggered
$A_1 - A_{18}$ latched (Input address latch triggered by GNT circuitry)*
$A_1 - A_9$ propagate to $MA_0 - MA_8$ outputs

C $\overline{RAS}$ triggered

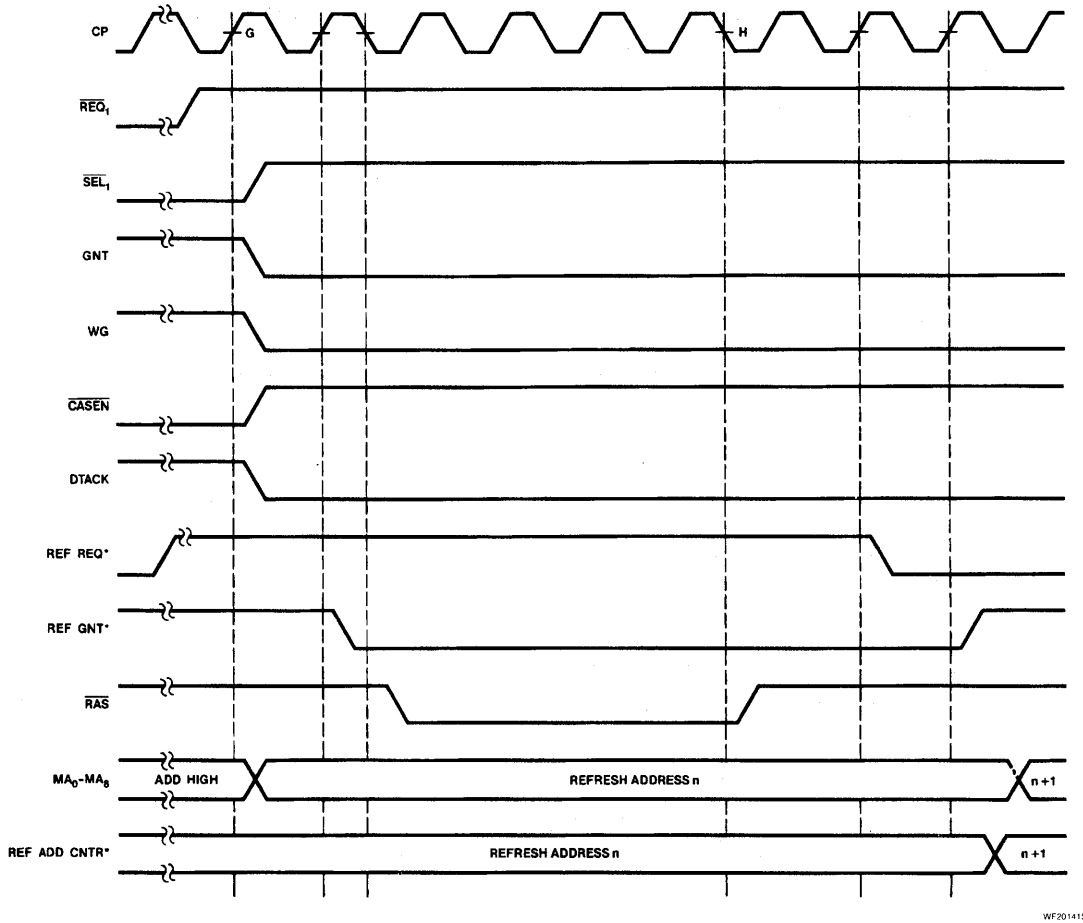
D WG triggered
$A_{10} - A_{18}$ selected and propagated to $MA_0 - MA_8$ outputs

E $\overline{CASEN}$ triggered

F $\overline{RAS}$ negated
DTACK triggered

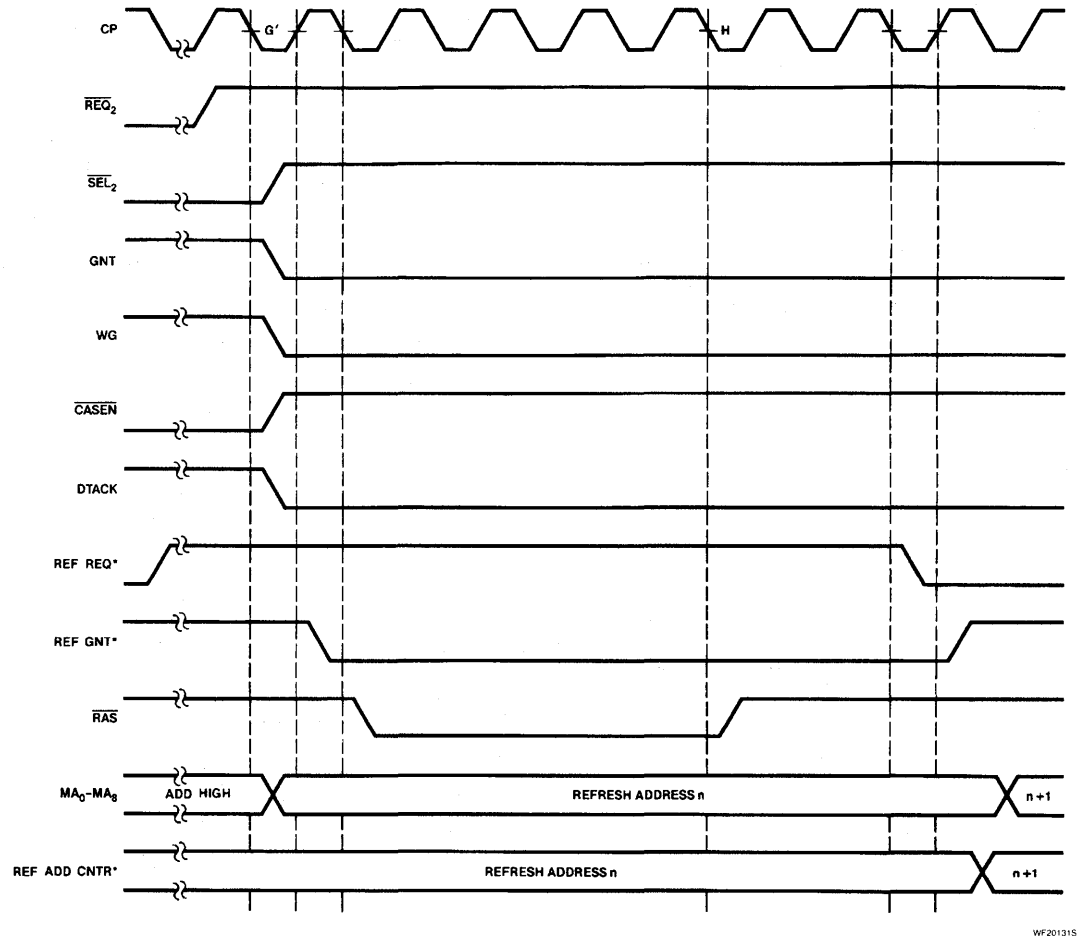
* Only on the 'F764-1.

Figure 4. Sequence of Events for $\overline{REQ}_2$ Memory Access Cycle for F764-1/765-1



NOTE:
* These are internal signals only.

Figure 5. Refresh Cycle Timing Following a $\overline{REQ_1}$ Memory Access Cycle for All Devices



NOTE:
* These are internal signals only.

Figure 6. Refresh Cycle Timing Following a $\overline{REQ}_2$ Memory Access Cycle for All Devices

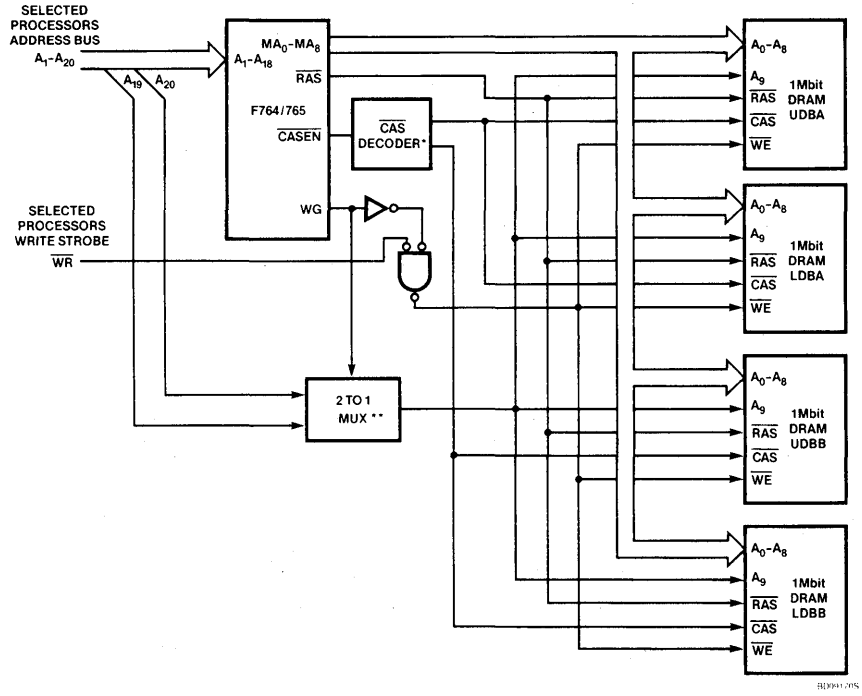
USING 74F764/765, 74F764A/765A, AND 74F764-1/765-1 TO ADDRESS 1MBIT DRAMS

The addressing capabilities of the DRAM dual-ported controllers can be extended to address 1Mbit (or greater) DRAMs by using an external multiplexer to multiplex additional address bits.

Figure 7 shows an application, using an external 2-to-1 multiplexer to address 1Mbit dynamic RAMs. The 9-bit internal refresh counter of the controller provides 512 row addresses which more than meet the refreshing needs for most industry standard 1Mbit DRAMs. Therefore, it is unnecessary to provide for any additional refresh address bits for DRAMs with up to 512 rows.

Additional address bits (for larger DRAMs) may also be multiplexed externally as long as the DRAM refreshing requirements do not exceed 512 row addresses.

The WG output of the controller should be used to multiplex between the external row and column address bits. However it is important that the propagation delay through the external multiplexer does not cause column address setup violations on the dynamic RAM.



* The $\overline{CAS}$ decode logic is not necessary if multiple $\overline{CAS}$ signals are not required. The application also does not show further decoding of multiple $\overline{CAS}$ signals to distinguish between Upper and Lower data bytes. If required, multiple $\overline{CAS}$ signal generation and Upper and Lower byte decoding can be accomplished as shown in Figures 16 – 18.

** Propagation delay through the multiplexer should be considered when using the controller for 1Mbit addressing.

Figure 7. Using the Controller to Address 1Mbit DRAMs

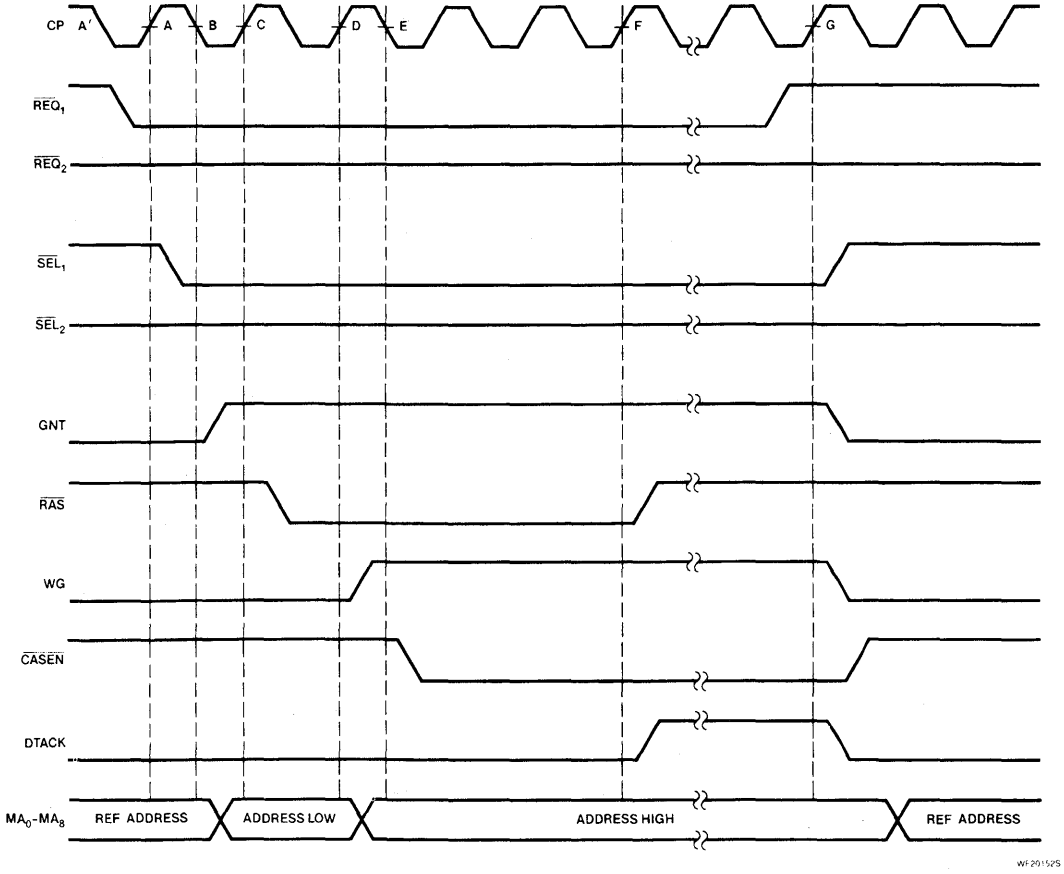


Figure 8. Request 1 ($\overline{REQ}_1$) Memory Access Cycle Timing for F764/765 and F764A/765A

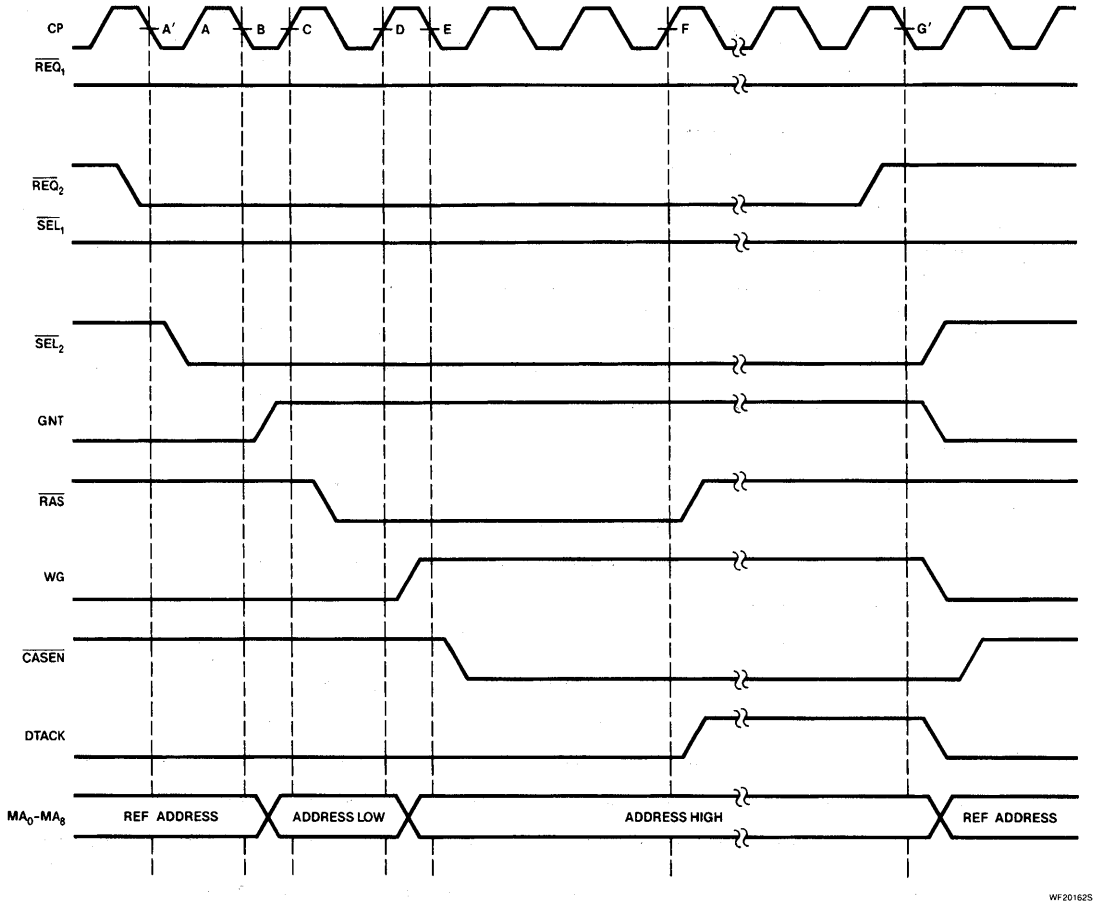


Figure 9. Request 2 ($\overline{REQ_2}$) Memory Access Cycle Timing for F764/765 and F764A/765A

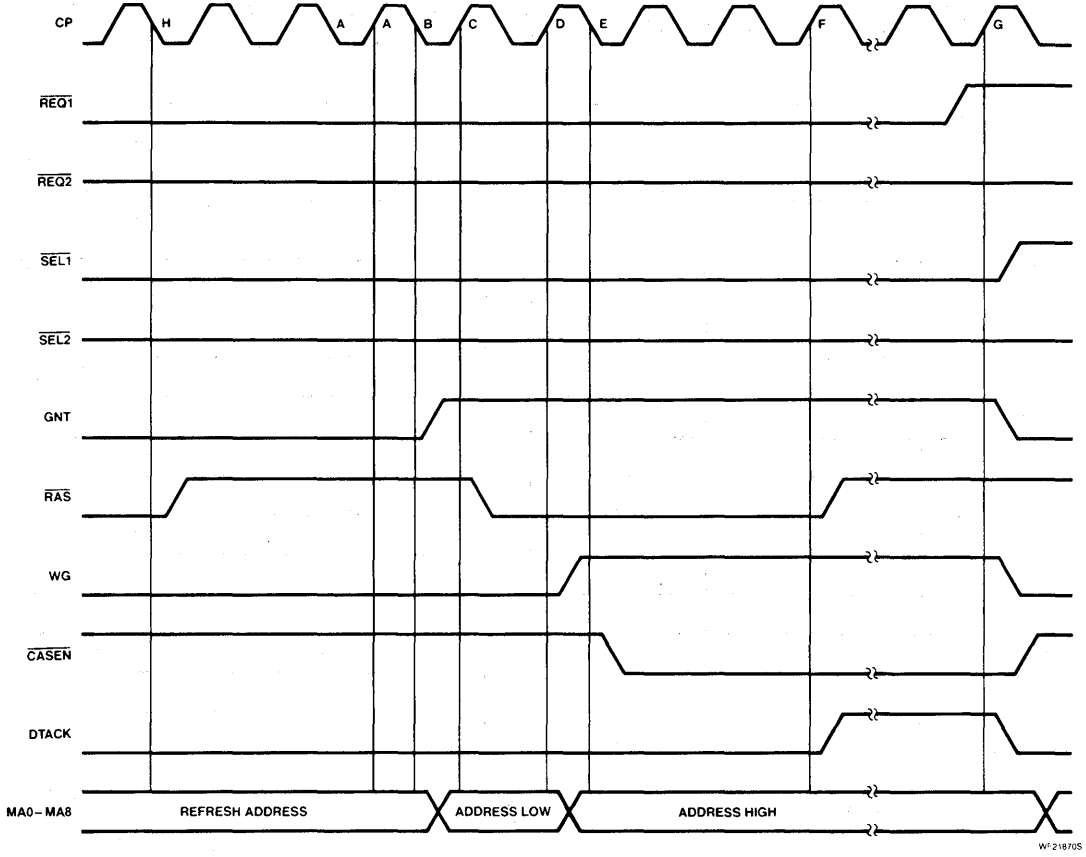


Figure 10. Request 1 ($\overline{REQ}_1$) Memory Access Cycle Timing Following a Refresh Cycle for F764/765 and F764A/765A

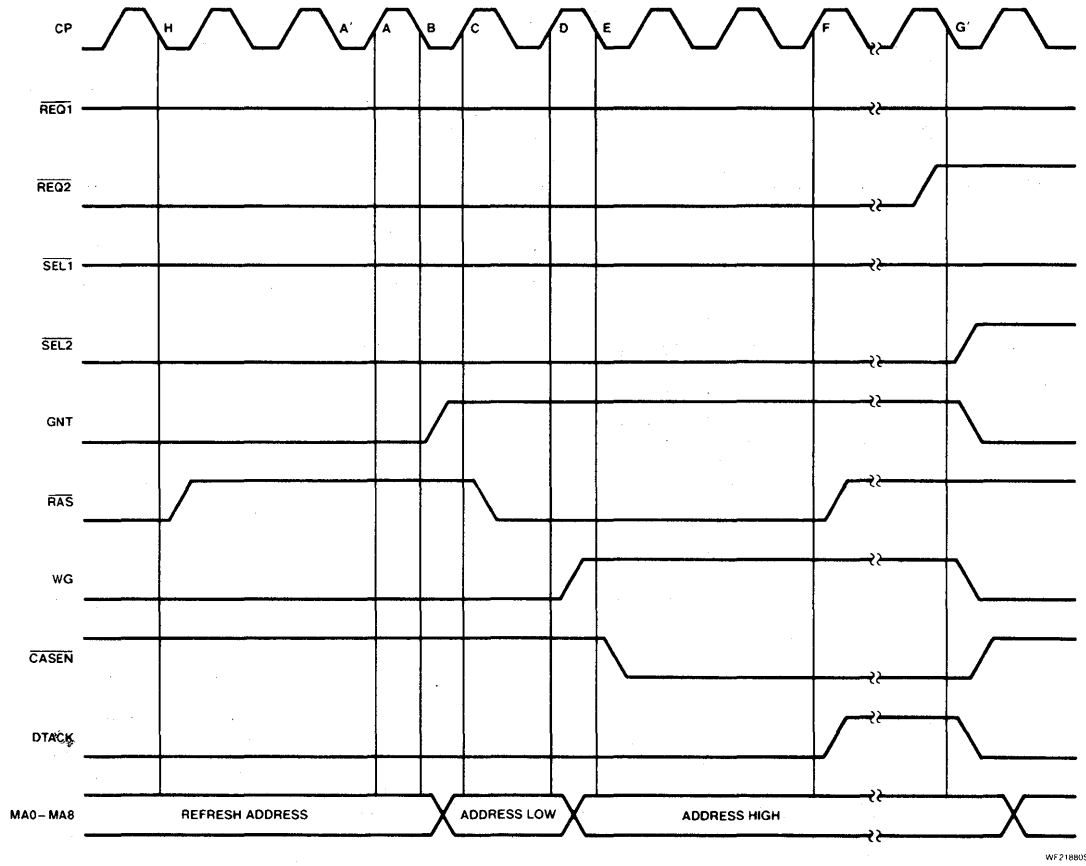


Figure 11. Request 2 ($\overline{REQ}_2$) Memory Access Cycle Timing Following a Refresh Cycle for F764/765 and F764A/765A

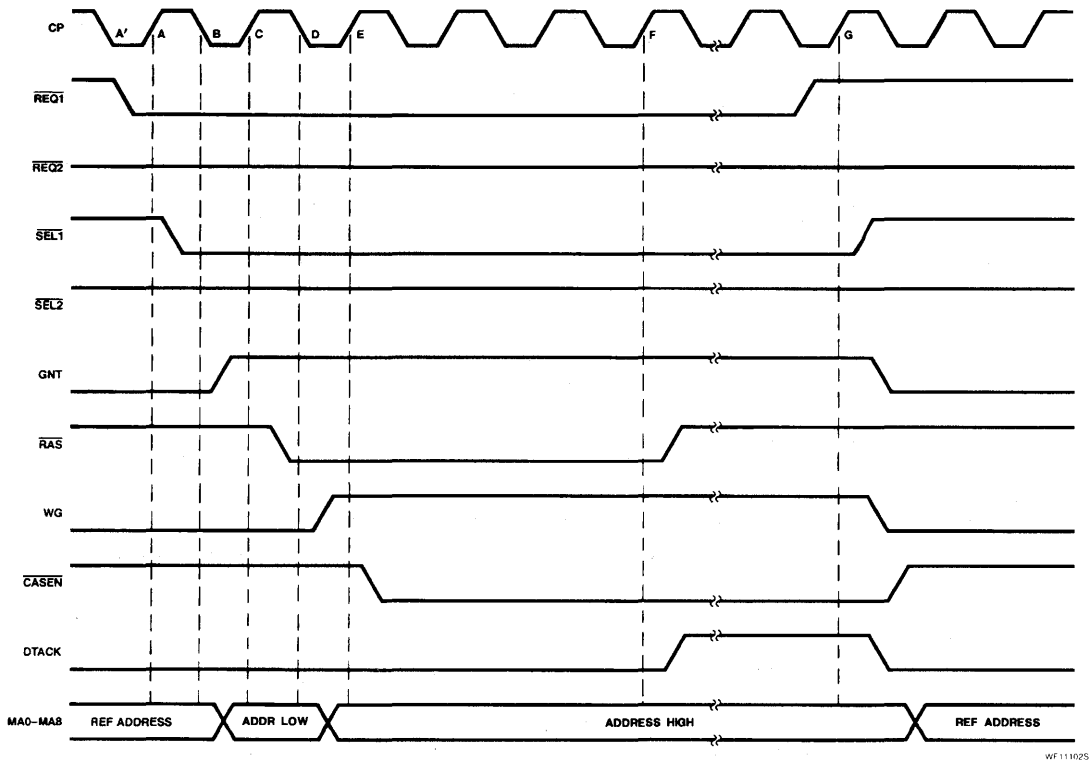


Figure 12. Request 1 ($\overline{REQ}_1$) Memory Access Cycle Timing for F764-1/765-1

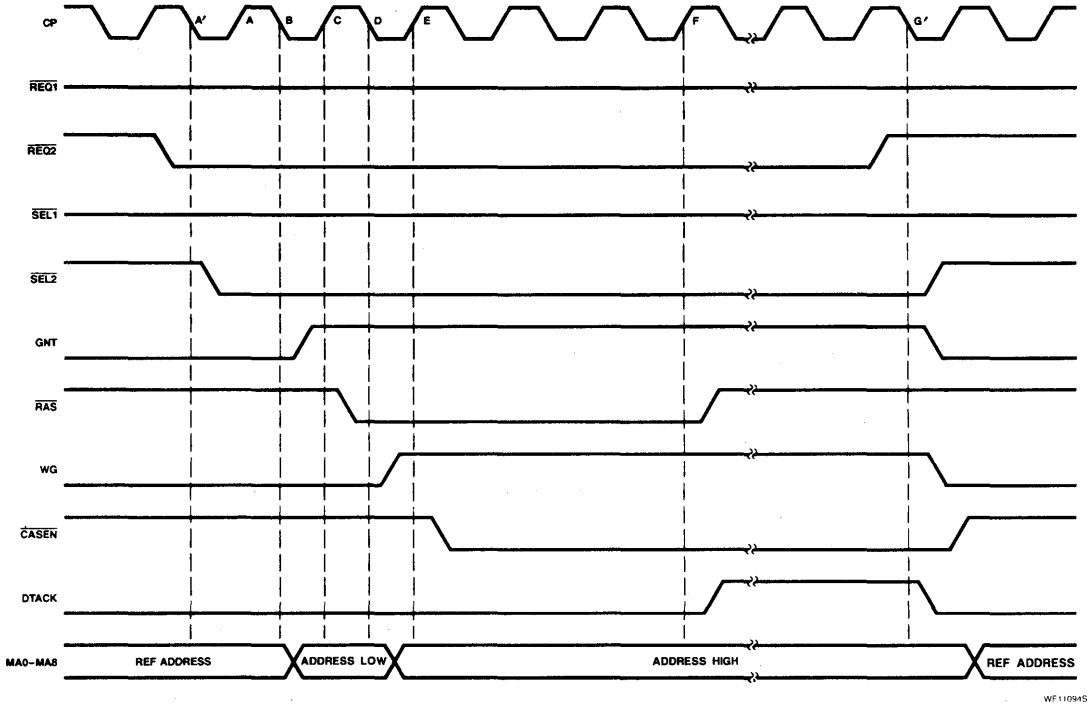


Figure 13. Request 2 ($\overline{REQ}_2$) Memory Access Cycle Timing for F764-1/765-1

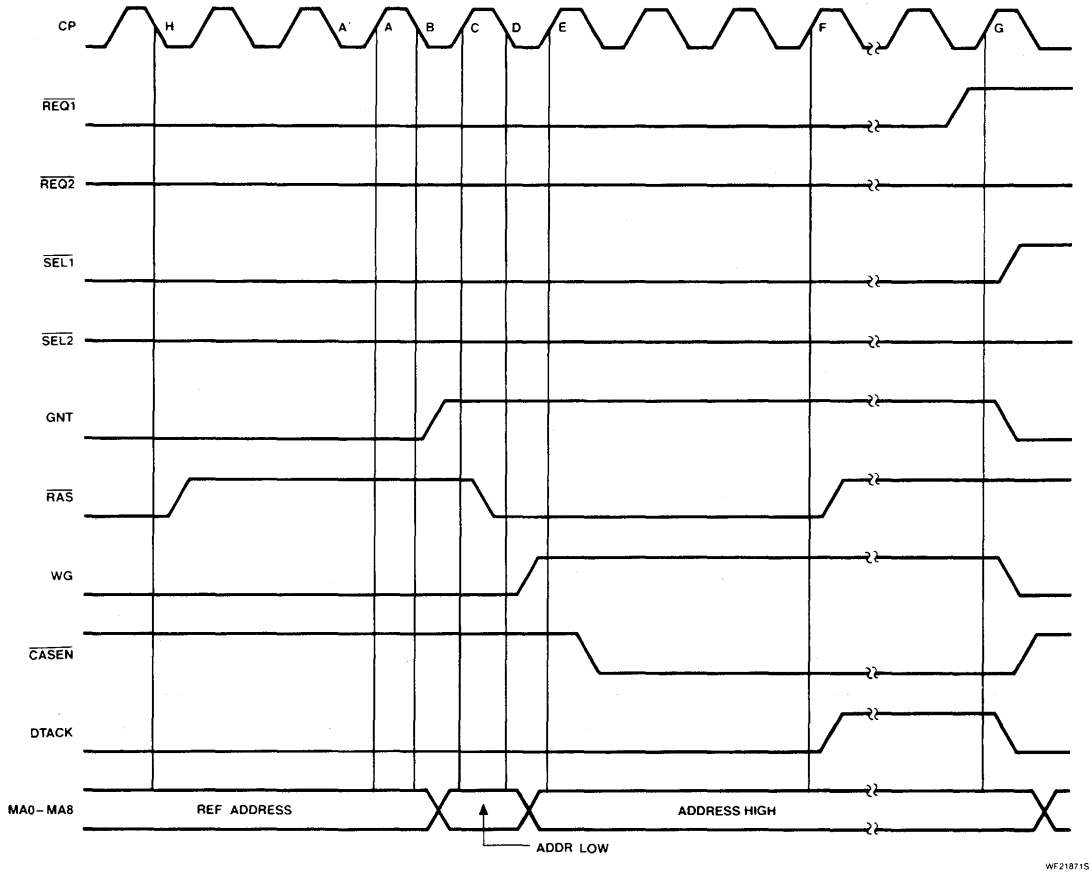


Figure 14. Request 1 ($\overline{REQ}_1$) Memory Access Cycle Timing Following a Refresh Cycle for F764-1/765-1

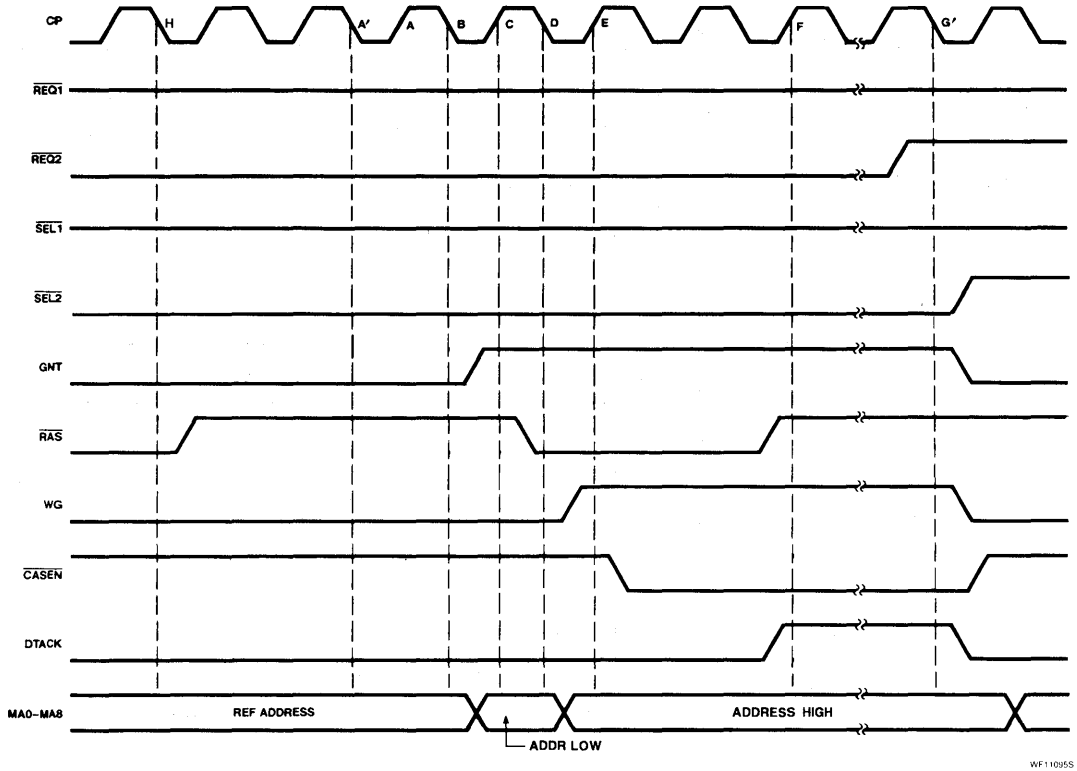


Figure 15. Request 2 ($\overline{REQ}_2$) Memory Access Cycle Timing Following a Refresh Cycle for F764-1/765-1

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range).

SYMBOL	PARAMETER	74F764/765, 74F764A/765A	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	500	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74F764/765, 74F764A/765A			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current[1]			24	mA
T_A	Operating free-air temperature[1]	0		70	°C

NOTE:
1. Transient currents will exceed these values in actual operation. Please refer to Appendix A for detailed discussion.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F764/765, 74F764A/765A			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −15mA	±10%V_{CC}	2.5	3.2		V
					±5%V_{CC}	2.7	3.4		V
V_{OH2}[3]	High-level output voltage			I_{OH2}[3] = −35mA	±5%V_{CC}	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{OL2}[4]	Low-level output voltage			I_{OL2}[4] = 60mA	±5%V_{CC}		0.45	0.80	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					−0.6	mA
I_{OS}	Short-circuit output current[5]		V_{CC} = MAX			−100		−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				150	200	mA
		I_{CCL}					165	210	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Refer to Appendix A.
4. Refer to Appendix A.
5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well over the normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER[1]	74F764/765, 74F764A/765A					UNIT
		$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 300pF$, $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 300pF$, $R_L = 70\Omega$		
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay CP(G) to $\overline{SEL_1}$	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(A) to $\overline{SEL_1}$	5	10	14	5	16	ns
t_{PLH}	Propagation delay CP(G') to $\overline{SEL_2}$	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(A') to $\overline{SEL_2}$	5	10	14	5	16	ns
t_{PLH}	Propagation delay CP(B) to GNT	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(G or G') to GNT	5	10	15	5	16	ns
t_{PLH} t_{PHL}	Propagation delay CP(B) to MA(row address)	5 5	12 11	17 15	5 5	18 16	ns
t_{PLH}	Propagation delay CP(F or H) to $\overline{RAS}$	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(C) to $\overline{RAS}$	5	10	14	5	16	ns
t_{PLH}	Propagation delay CP(D) to WG	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(G or G') to WG	8	13	17	8	18	ns
t_{PLH} t_{PHL}	Propagation delay CP(D) to MA(column address)	5 5	12 10	17 15	5 5	18 16	ns
t_{PLH}	Propagation delay CP(G or G') to $\overline{CASEN}$	7	17	23	7	25	ns
t_{PHL}	Propagation delay CP(E) to $\overline{CASEN}$	5	10	14	5	16	ns
t_{PLH}	Propagation delay CP(F) to DTACK	5	10	14	5	16	ns
t_{PHL}	Propagation delay CP(G or G') to DTACK	6	13	17	5	18	ns
74F765, 74F765A Only							
t_{PLH} t_{PHL}	Propagation delay $A_1 - A_{18}$ to $MA_0 - MA_8$	4 2	7 5	12 8	4 4	13 19	ns

NOTE:
1. For test conditions, see the AC waveforms.

AC SETUP AND HOLD REQUIREMENTS

SYMBOL	PARAMETER[2]	74F764/765, 74F764A/765A					UNIT
		$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 300pF$, $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 300pF$, $R_L = 70\Omega$		
		Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{REQ}_1$, $\overline{REQ}_2$ to CP	2 2			2 2		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CP to $\overline{REQ}_1$, $\overline{REQ}_2$	2 2			3 3		ns
$t_w(H)$ $t_w(L)$	CP pulse width High or Low	5 5			5 5		ns
$t_w(H)$ $t_w(L)$	RCP pulse width High or Low	10 10			10 10		ns
74F764, 74F764A Only							
$t_s(H)$ $t_s(L)$	Setup time, High or Low $A_1 - A_{18}$ to CP(↓)	-4^1 -4			-5 -5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CP(↓) to $A_1 - A_{18}$	5 5			5 5		ns
74F764/765 Only							
f_{MAX}	Input clock frequency	100	150		100		MHz
74F764A/765A Only							
f_{MAX}	Input clock frequency	150	175		150		MHz

NOTES:

1. These numbers indicate that the address inputs have a negative setup time and could be valid 4ns after the falling edge of the CP clock. It is suggested that $\overline{SEL}_2$ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of $\overline{SEL}_1$ to enable Address Bus 1. This will insure that setup time for Address Bus 1 is not violated.
2. For the Test Conditions, see the AC Waveforms.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range).

SYMBOL	PARAMETER	74F764-1/765-1	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	500	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74F764-1/765-1			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current[1]			−20	mA
I_{OL}	Low-level output current[1]			8	mA
T_A	Operating free-air temperature	0		70	°C

NOTE:
1. Transient currents will exceed these values in actual operation. Please refer to Appendix A for detailed discussion.

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			74F764-1, 74F765-1			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = −20mA	±10%V_{CC}	2.4	2.70		V
					±5%V_{CC}	2.6	3.0		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 8mA	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{OL2}[3]	Low-level output voltage			I_{OL2}[3] = 75mA	±5%V_{CC}		2.1	2.5	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				−0.7	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.2	−0.6	mA
I_{OS}	Short-circuit output current[4]		V_{CC} = MAX			−80	−150	−225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				120	165	mA
		I_{CCL}					125	170	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Refer to Appendix A.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well over the normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	74F764-1/765-1					UNIT
		$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 300pF$, $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 300pF$, $R_L = 70\Omega$		
		Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	100	150		100		MHz
t_{PLH}	Propagation delay CP(G) to $\overline{SEL_1}$	9	12	15	8	17	ns
t_{PHL}	Propagation delay CP(A) to $\overline{SEL_1}$	13	16	20	12	22	ns
t_{PLH}	Propagation delay CP(G') to $\overline{SEL_2}$	9	12	15	8	17	ns
t_{PHL}	Propagation delay CP(A') to $\overline{SEL_2}$	13	16	20	12	22	ns
t_{PLH}	Propagation delay CP(B) to GNT	9	12	14	8	16	ns
t_{PHL}	Propagation delay CP(G or G') to GNT	20	23	26	17	28	ns
t_{PLH} t_{PHL}	Propagation delay CP(B) to MA(row address)	11 14	14 18	17 22	10 13	19 24	ns
t_{PLH}	Propagation delay CP(F or H) to $\overline{RAS}$	11	14	16	10	18	ns
t_{PHL}	Propagation delay CP(C) to $\overline{RAS}$	13	17	20	12	22	ns
t_{PLH}	Propagation delay CP(D) to WG	9	11	14	8	16	ns
t_{PHL}	Propagation delay CP(G or G') to WG	20	23	26	19	26	ns
t_{PLH} t_{PHL}	Propagation delay CP(D) to MA(column address)	12 14	14 18	17 21	11 13	19 23	ns
t_{PLH}	Propagation delay CP(G or G') to $\overline{CASEN}$	14	17	20	12	22	ns
t_{PHL}	Propagation delay CP(E) to $\overline{CASEN}$	14	16	19	13	21	ns
t_{PLH}	Propagation delay CP(F) to DTACK	10	12	15	9	17	ns
t_{PHL}	Propagation delay CP(G or G') to DTACK	20	23	26	19	28	ns
	74F765-1 Only						
t_{PLH} t_{PHL}	Propagation delay $A_1 - A_{18}$ to $MA_0 - MA_8$	9 9	11 12	14 15	8 8	16 17	ns

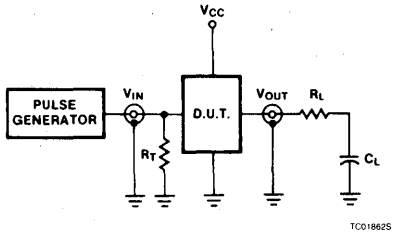
AC SETUP AND HOLD REQUIREMENTS

SYMBOL	PARAMETER	74F764-1/765-1					UNIT
		$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 300pF$, $R_L = 70\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 300pF$, $R_L = 70\Omega$		
		Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{REQ_1}$, $\overline{REQ_2}$ to CP	3	1		4		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CP to $\overline{REQ_1}$, $\overline{REQ_2}$	2	0		3		ns
$t_w(H)$ $t_w(L)$	CP pulse width High or Low	5	3		5		ns
$t_w(H)$ $t_w(L)$	RCP pulse width High or Low	5			5		ns
	74F764-1 Only						
$t_s(H)$ $t_s(L)$	Setup time, High or Low $A_1 - A_{18}$ to CP($\downarrow$)	0	-1^1		1		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CP($\downarrow$) to $A_1 - A_{18}$	5	3		6		ns

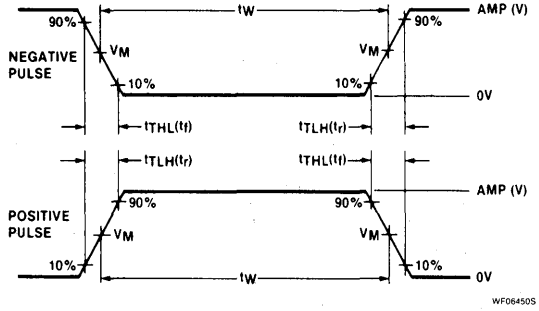
NOTE:

1. These numbers indicate that the address inputs have a negative setup time and could be valid 1ns after the falling edge of the CP clock. It is suggested that $\overline{SEL_2}$ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of $\overline{SEL_1}$ to enable Address Bus 1. This will insure that setup time for Address Bus 1 is not violated.

TEST CIRCUIT AND WAVEFORMS FOR ALL DEVICES



Test Circuit Simulating RAM Boards



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to GND; see AC Characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

APPLICATIONS

The DRAM dual-ported controller can be designed into a wide range of single and dual-port interface configurations. The processors could be general or special-purpose (micro-controllers) and the data bus may differ in size.

Figure 16 shows a 68000 processor sharing a 64K × 8 (two banks each consisting of sixteen 16K × 1 devices) memory with a Z-80 processor. Since neither Z-80 nor 68000 have multiplexed address and data bus, the 'F765/F765A/F765-1 is appropriate.

Since the Z-80 has an 8-bit wide data bus, data buffers are used to convert the 16-bit memory data bus to an 8-bit wide processor bus. Address bit (A_0) from the Z-80 serves as an enable to one of the two data buffers at a given time. Address bit (A_{15}) from either the Z-80 or the 68000 distinguishes between Memory Banks A and B. Where Bank A consists of Upper Data Byte A (UDBA) and Lower Data Byte A (LDBA) and Bank B consists of Upper Data Byte B (UDBB) and Lower Data Byte B (LDBB).

When the Z-80 is selected and A_{15} is a zero, all even bytes will be accessed from UDBA and all odd bytes from LDBA. Similarly, when A_{15} is a one, UDBB will contain all even bytes and LDBB all odd bytes.

For 68000, Upper and Lower Data Strobes ($\overline{UDS}$ and $\overline{LDS}$) determine whether a byte or word transfer will take place. The $\overline{WAIT}$ input on the Z-80 is asserted when $\overline{REQ}_1$ is generated, and is negated when the GNT output is asserted by the controller. The additional gating circuitry is to ensure that $\overline{DTACK}$ to the 68000 is asserted only when it is selected.

Figure 17 shows two 8086 processors sharing 1MByte (two banks each consisting of sixteen 256K × 1 devices) of dynamic RAM. Using 74F764 in this application may eliminate the need for an external address latch.

Similarly, Figure 18 shows two 68020 processors sharing the same amount of memory.

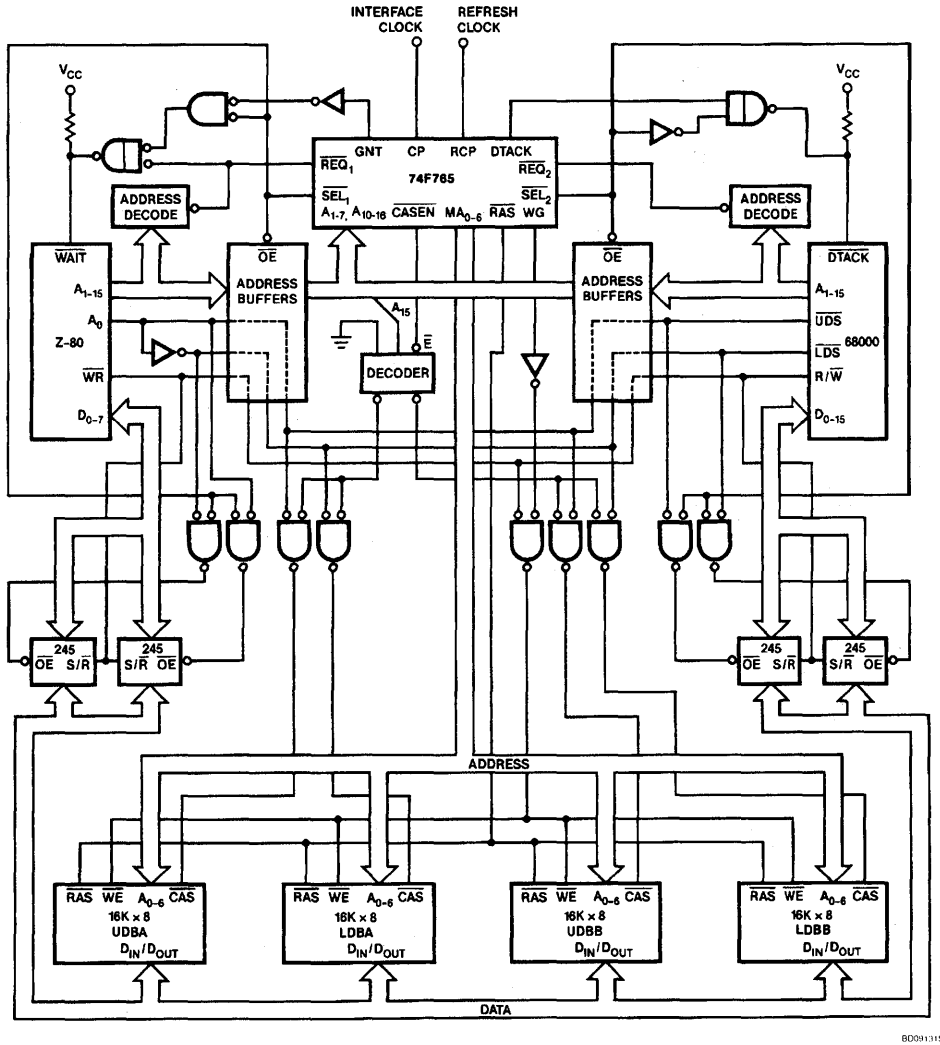
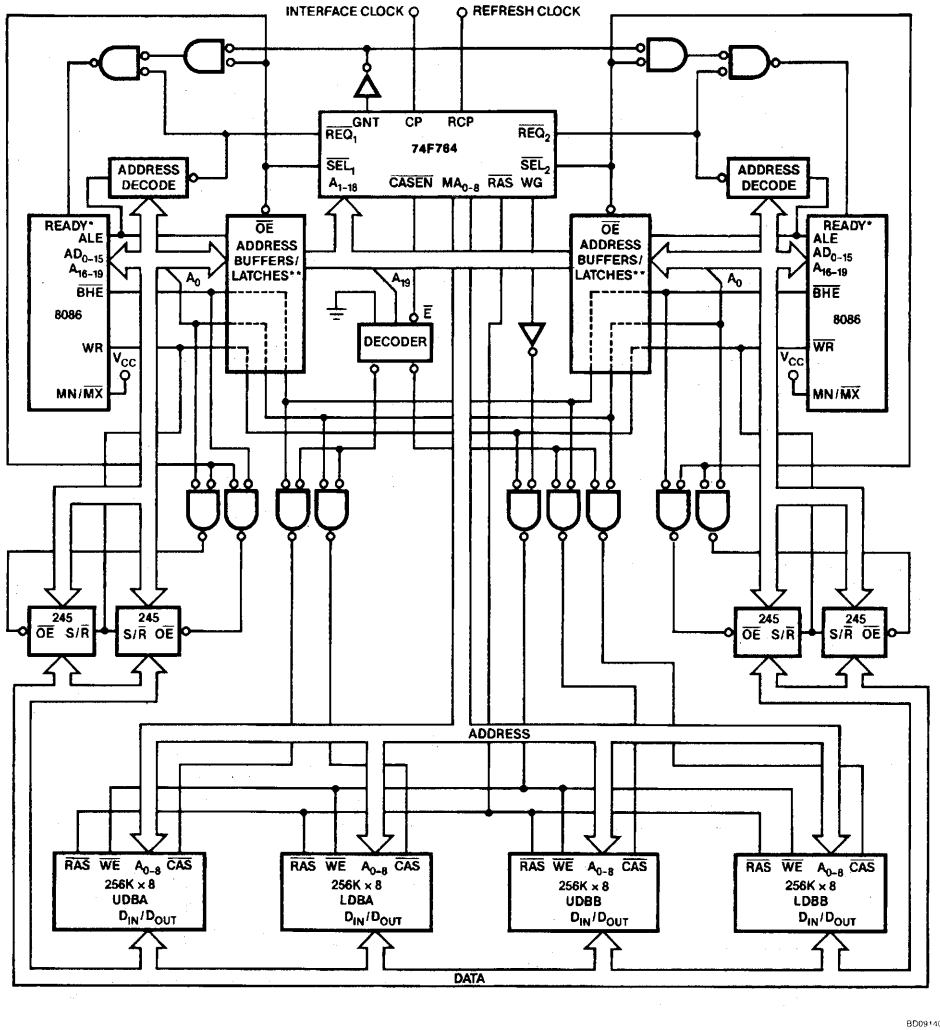


Figure 16. A 68000 Processor Sharing 64K × 8 DRAM With a Z-80



* It might be necessary to synchronize READY by the 8284A. Please refer to the 8086 data sheet.
** Whether or not the 8086 address bus needs to be latched externally, should be determined by the relative speeds of the 8086 and the controller.

Figure 17. Two 8086 Processors Sharing 1MBYTE of DRAM

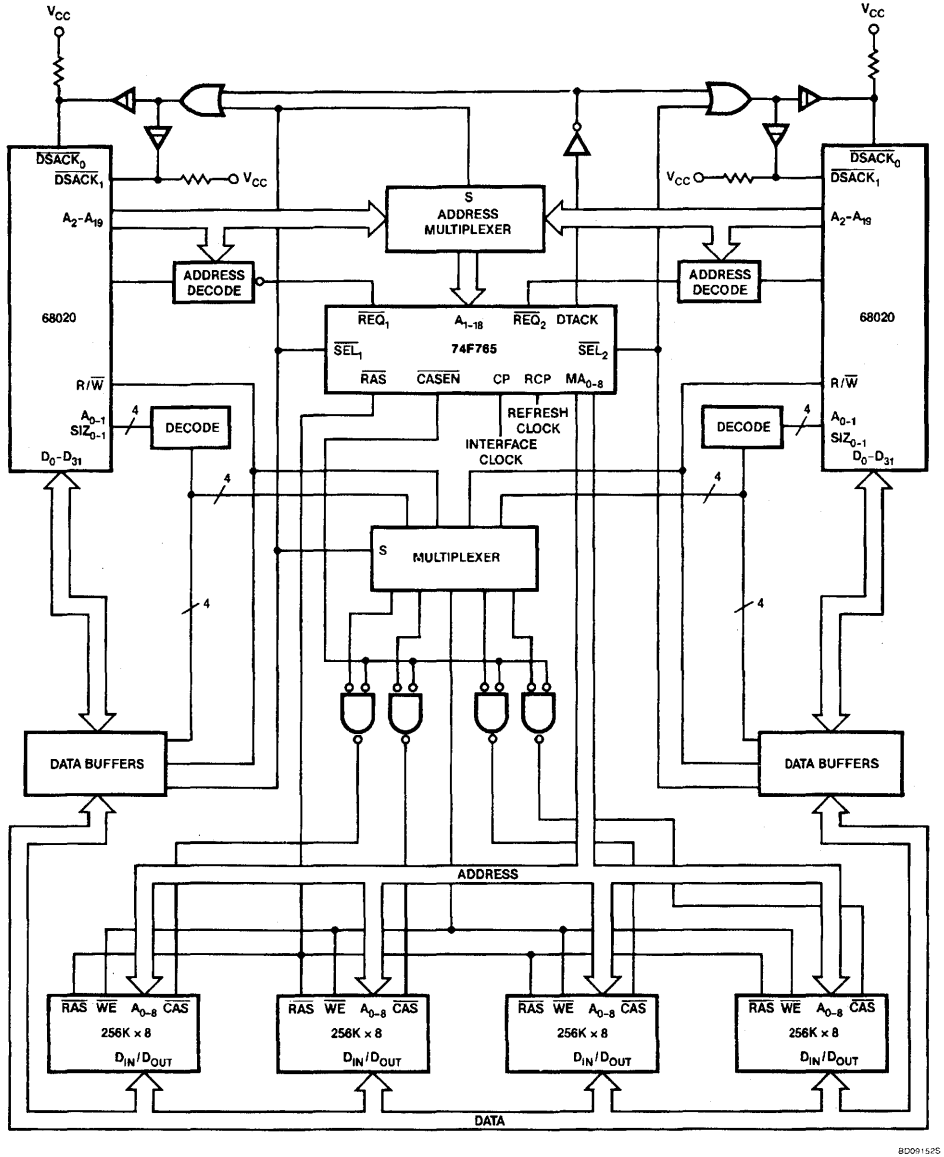


Figure 18. Two 68020 Processors Sharing 1MBYTE of DRAM

74F764 FAMILY LINE DRIVING CHARACTERISTICS

The 74F764/765 and 74F764A/765A are designed to provide incident wave switching in Dual-Inline-Package (DIP) or Zig-zag-Inline-Package (ZIP) housed memory arrays and first reflected wave switching in Single-Inline-Package (SIP) or Single-Inline-Module (SIM) housed arrays. The 74F764-1/765-1, on the other hand, are designed to provide first reflected wave switching with as wide a range of characteristic impedances as possible.

The I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} parameters are included in the product specifications to assist engineers in designing systems which will switch memory array signal lines in the above mentioned manner. For example, the characteristic impedance of signal lines in DIP housed memory arrays is usually around 70Ω. If a signal line has settled out in a High state at 4 volts and must be pulled down to 0.8 volts or less on the incident wave, the DRAM Controller output must sink (4-0.8)/70A or 46mA at 0.8 volts. The I_{OL2}/V_{OL2} parameter indicates that the signal line in question will always be switched on the incident wave over the full commercial operating range.

It should be noted here that I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} are intended for transient use only and that steady state operation at I_{OH2} or I_{OL2} is not recommended (long term, steady state operation at these currents may result in electromigration).

Figures 1 – 4 show the output I/V characteristics of the DRAM Controller family of devices. These figures also demonstrate a graphical method for determining the incident wave (and first reflected wave) characteristics of the devices.

The suggested line termination for the 74F764/765 or 74F764A/765A driving dual-inline packaged or zig-zag packaged DRAMs is shown in Figure 8a. When driving single-inline modules using the 74F764/765 or 74F764A/765A, or when driving any type of memory arrays with the 74F764-1/765-1, the schottky diode termination shown in Figure 8b can be used (most of these will need no termination at all).

Figures 5 – 7 are double exposures showing the High to Low and Low to High transitions while driving four banks of eight Dual-Inline-Packaged DRAMs. The signal line is unterminated in Figures 5 and 6, allowing the 74F764/765/764A/765A to ring two volts below ground while the 74F764-1/765-1 make nice clean transitions. In Figure 7 the 74F764/765/764A/765A is driving the same signal line but with one of its four branches terminated with its characteristic impedance in series with 300pF to ground (the worst of the four branches is shown).

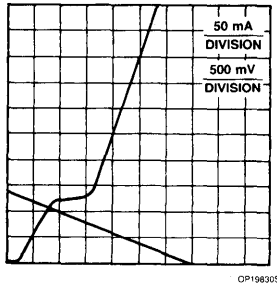


Figure 1. I-V Output Characteristics of the 74F764 and 765 in the Low State. Light Line is the I-V Curve of a 25Ω Transmission Line Settled to 3.5V (Typical for Recommended Termination). The High to Low Incident Wave on This Line Would Typically be to .8V

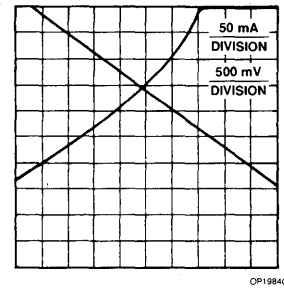


Figure 2. I-V Output Characteristics of the 74F764 and 765 in the High State. Light Line is the I-V Curve of a 35Ω Transmission Line Settled to .25V. The Incident Wave on the Low to High Transition Will Typically be to 2.4V on This Line. Any Line Over 35Ω Will Typically be Switched on the Incident Wave

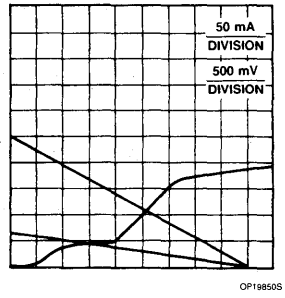


Figure 3. I-V Output Characteristics of the 74F764-1 and 765-1 in the Low State. Any Unterminated Line Impedance Between 18Ω and 70Ω (Both Shown) Will Typically Switch on the First Reflected Wave Without Violating the-1V Minimum Input Voltage Specification Typical of DRAMs

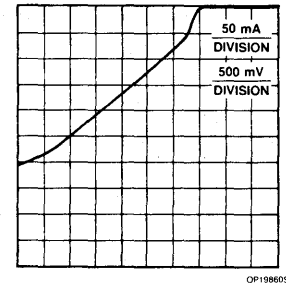


Figure 4. I-V Output Characteristics of the 74F764-1 and 765-1 While in the High State

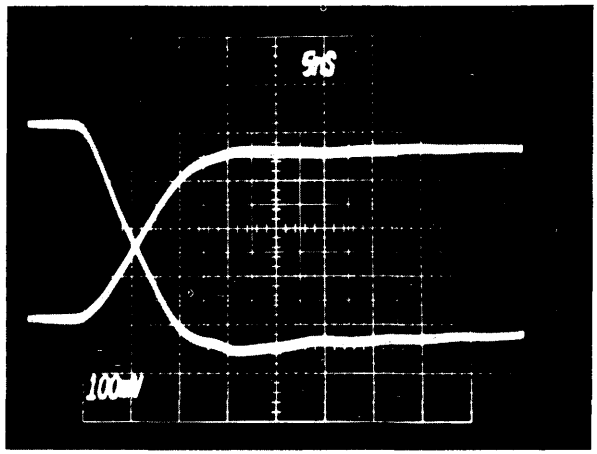


Figure 5. 74F764-1/765-1 Driving 32 DRAMs (Unterminated)

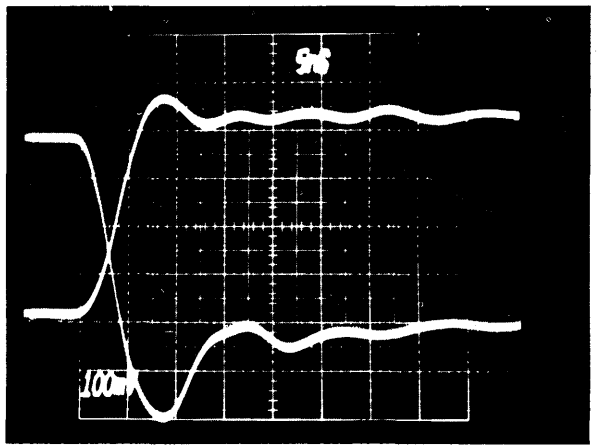


Figure 6. 74F764/765/764A/765A Driving 32 DRAMs (Unterminated)

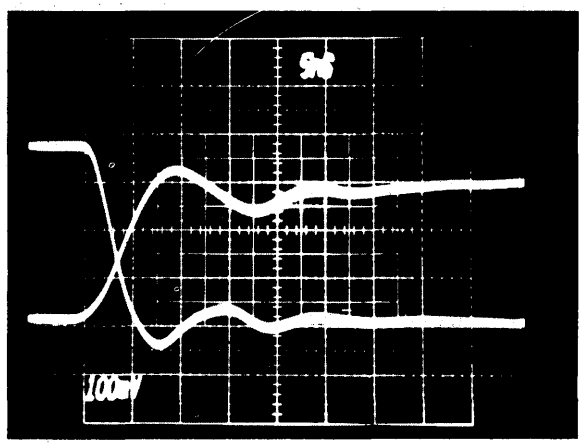


Figure 7. 74F764/765/764A/765A Driving 32 DRAMs (Terminated as in Figure 8a)

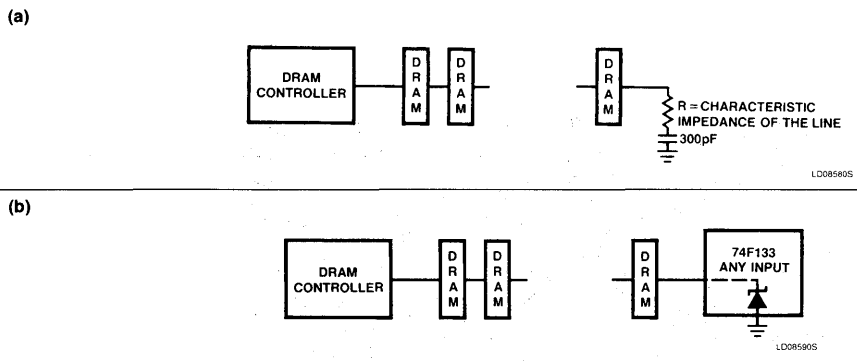


Figure 8

Signetics

FAST 74F776
Pi-Bus Transceiver

FAST Products

Octal Bidirectional Latched Transceiver (Open Collector)
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	MAX SUPPLY CURRENT (TOTAL)
74F776	7.5ns	85mA

FEATURES

- Octal Latched Transceiver
- Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms
- High drive (100mA) open collector drivers on B-port
- Reduced voltage swing (1 volt) produces less noise and reduces power consumption
- High speed operation enhances performance of backplane buses and facilitates incident wave switching
- Compatible with Pi-bus and IEEE 896 Futurebus Standards
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch-free power up / power down operation
- Multiple package options

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP (600mil)[1]	N74F776N
28-Pin PLCC[1]	N74F776A

NOTE:
1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	PNP latched inputs	3.5/0.117	70µA/70µA
B_0 - B_7	Data inputs with threshold circuitry	5.0/0.167	100µA/100µA
OEA	A Output Enable input (active High)	1.0/0.033	20µA/20µA
$\overline{OEB}_0$, $\overline{OEB}_1$	B Output Enable inputs (active Low)	1.0/0.033	20µA/20µA
$\overline{LE}$	Latch Enable input (active Low)	1.0/0.033	20µA/20µA
A_0 - A_7	3-State outputs	150/40	3mA/24mA
B_0 - B_7	Open Collector outputs	OC*/166.7	OC*/100mA

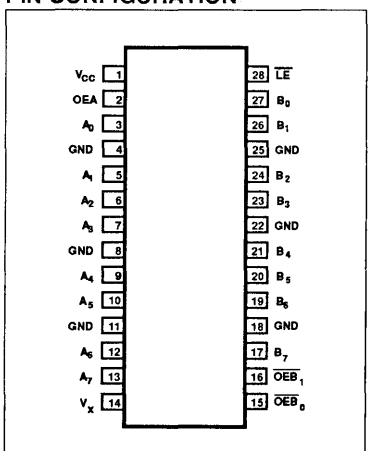
NOTES:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
* OC = Open Collector

DESCRIPTION

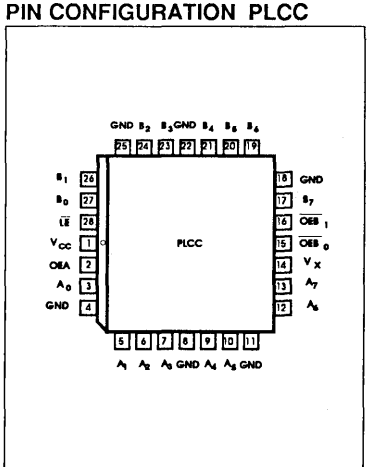
The 74F776 is an octal bidirectional latched transceiver and is intended to provide the electrical interface to a high performance wired-or bus. The B port inverting drivers are low-capacitance open collector with controlled ramp and are designed to sink 100 mA from 2 volts. The B port inverting receivers have a 100 mV threshold region and a 4ns glitch filter.

The 74F776 B port interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive

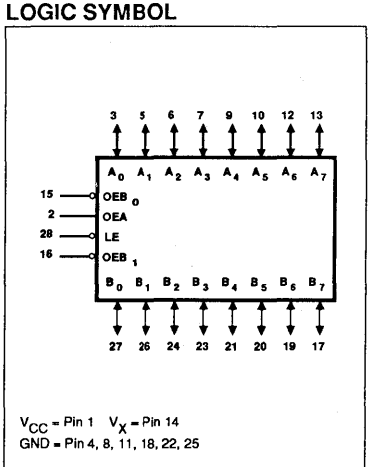
PIN CONFIGURATION



PIN CONFIGURATION PLCC



LOGIC SYMBOL



DESCRIPTION (Continued)

loading (<5 pF). Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.

The 74F776 A port has TTL 3-State drivers and TTL receivers with a latch function. A separate High-level control voltage input (V_x) is provided to limit the A side output level to a given voltage level (such as 3.3V). For 5.0V systems, V_x is simply tied to V_{CC}.

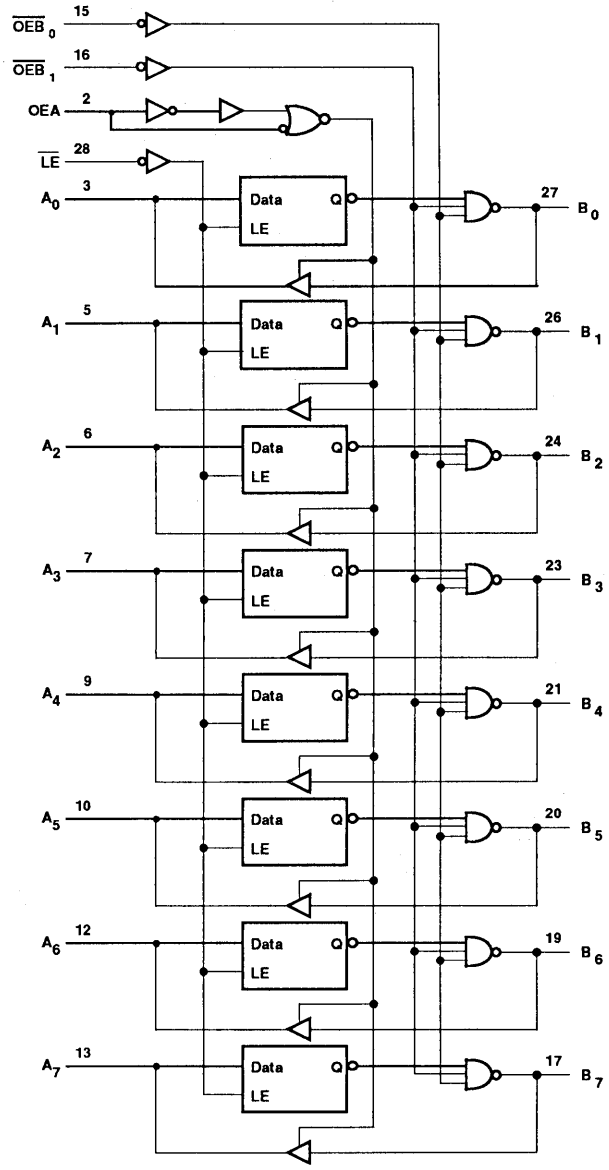
The 'F776 has a designed feature to control the B output transitions during power sequencing. There are two possible sequences, They are as follows:

1. When $\overline{LE}$=Low and $\overline{OEB}_n$= Low then the B outputs are disabled until the $\overline{LE}$ circuitry takes control. Then the B outputs will follow the A inputs, making a maximum of one transition during power-up (or down).
2. If $\overline{LE}$=High or $\overline{OEB}_n$= High then the B outputs will be disabled durng power-up (or down).

PIN DESCRIPTION

SYMBOL	PINS	TYPE	NAME AND FUNCTION
A_0	3	I/O	PNP latched input / 3-State output (with V_X control option)
A_1	5	I/O	
A_2	6	I/O	
A_3	7	I/O	
A_4	9	I/O	
A_5	10	I/O	
A_6	12	I/O	
A_7	13	I/O	
B_0	27	I/O	Data input with special threshold circuitry to reject noise / Open Collector output, High current drive
B_1	26	I/O	
B_2	24	I/O	
B_3	23	I/O	
B_4	21	I/O	
B_5	20	I/O	
B_6	19	I/O	
B_7	17	I/O	
$\overline{OEB}_0$	15	I	Enables the B outputs when both pins are Low
$\overline{OEB}_1$	16	I	
OEA	2	I	Enables the A outputs when High
$\overline{LE}$	28	I	Latched when High (a special delay feature is built in for proper enabling times)
V_X	14	I	Clamping voltage keeping V_{OH} from rising above V_X (V_X = V_{CC} for normal use)

LOGIC DIAGRAM



V_{CC} = Pin 1 V_X = Pin 14
GND = Pin 4, 8, 11, 18, 22, 25

FUNCTION TABLE

INPUTS						LATCH	OUTPUTS		MODE
A_n	B_n*	$\overline{LE}$	OEA	$\overline{OEB_0}$	$\overline{OEB_1}$	STATE	A_n	B_n	
H	X	L	L	L	L	H	Z	Z	A 3-state, Data from A to B
L	X	L	L	L	L	L	Z	L	
X	X	H	L	L	L	Q_n	Z	Q_n	A 3-state, Latched data to B
–	–	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	L	H(2)	H	Z(2)	Preconditioned Latch enabling data transfer from B to A
–	L	H	H	L	L	H(2)	L	Z(2)	
–	–	H	H	L	L	Q_n	Q_n	Q_n	Latch state to A and B
H	X	L	L	H	X	H	Z	Z	B and A 3-state
L	X	L	L	H	X	L	Z	Z	
X	X	H	L	H	X	Q_n	Z	Z	
–	H	L	H	H	X	H	H	Z	B 3-state, Data from B to A
–	L	L	H	H	X	L	L	Z	
–	H	H	H	H	X	Q_n	H	Z	
–	L	H	H	H	X	Q_n	L	Z	
H	X	L	L	X	H	H	Z	Z	B and A 3-state
L	X	L	L	X	H	L	Z	Z	
X	X	H	L	X	H	Q_n	Z	Z	
–	H	L	H	X	H	H	H	Z	B 3-state, Data from B to A
–	L	L	H	X	H	L	L	Z	
–	H	H	H	X	H	Q_n	H	Z	
–	L	H	H	X	H	Q_n	L	Z	

H = High voltage level
L = Low voltage level
X = Don't care
– = Input not externally driven
Z = High Impedance (off) state
Q_n = High or Low voltage level one setup time prior to the Low-to-High $\overline{LE}$ transition
(1) = Condition will cause a feedback loop path; A to B and B to A
(2) = The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB_0}$ and $\overline{OEB_1}$ are Low and $\overline{LE}$ is High.
B* = Precaution should be taken to insure the B inputs do not float. If they do they are equal to Low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_X	Threshold control		-0.5 to +7.0	V
V_{IN}	Input voltage	$\overline{OEB}_n$, OEA, $\overline{LE}$	-0.5 to +7.0	V
		A_0 - A_7, B_0 - B_7	-0.5 to 5.5	
I_{IN}	Input current		-40 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A_0 -A_7	48	mA
		B_0 - B_7	200	
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except B_0 - B_7	2.0			V
		B_0 - B_7	1.6			
V_{IL}	Low-level input voltage	Except B_0 - B_7			0.8	V
		B_0 - B_7			1.45	
I_{IK}	Input clamp current	Except A_0 - A_7			-18	mA
		A_0 - A_7			-40	
I_{OH}	High-level output current	A_0 - A_7			-3	mA
I_{OL}	Low-level output current	A_0 -A_7			24	mA
		B_0 - B_7			100	
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
I_{OH}	High level output current	$B_0 - B_7$	V_{CC} = MAX, V_{IL} =MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
I_{OFF}	Power-off output current	$B_0 - B_7$	V_{CC} = 0.0V, V_{IL} =MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
V_{OH}	High-level output voltage	$A_0 - A_7$[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3mA, $V_X = V_{CC}$	2.5		V_{CC}	V
				I_{OH} = -0.4mA, V_X = 3.13V & 3.47V	2.5		V_X	V
V_{OL}	Low-level output voltage	$A_0 - A_7$[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20mA, $V_X = V_{CC}$			0.5	V
		$B_0 - B_7$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA			1.15	V
				I_{OL} = 4mA	0.40			V
V_{IK}	Input clamp voltage	$A_0 - A_7$	V_{CC} = MIN, $I_I = I_{IK}$				-0.5	V
		Except $A_0 - A_7$	V_{CC} = MIN, $I_I = I_{IK}$				-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = 0.0V, V_I = 7.0V				100	µA
		$A_0 - A_7, B_0 - B_7$	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High-level input current	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 2.7V, $B_n - A_n$ = 0V				20	µA
		$B_0 - B_7$	V_{CC} = MAX, V_I = 2.1V				100	µA
I_{IL}	Low-level input current	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 0.5V				-20	µA
		$B_0 - B_7$	V_{CC} = MAX, V_I = 0.3V				-100	µA
$I_{OZH} + I_{IH}$	Off-state output current, High-level voltage applied	$A_0 - A_7$	V_{CC} = MAX, V_O =2.7V				70	µA
$I_{OZL} + I_{IL}$	Off-state output current, Low-level voltage applied	$A_0 - A_7$	V_{CC} = MAX, V_O =0.5V				-70	µA
I_X	High-level control current		V_{CC} = MAX, $V_X = V_{CC}$, $\overline{LE}$ = OEA = $\overline{OEB}_n$ = 2.7V, $A_0 - A_7$ = 2.7V, $B_0 - B_7$ = 2.0V		-100		100	µA
			V_{CC} = MAX, V_X = 3.13V & 3.47 V, $\overline{LE}$ = OEA = 2.7V, $\overline{OEB}_n = A_0 - A_7$ = 2.7V, $B_0 - B_7$ = 2.0V		-10		10	mA
I_{OS}	Short-circuit output current[3]	$A_0 - A_7$ only	V_{CC} = MAX, B_n = 1.6V, OEA = 2.0V, $\overline{OEB}_n$ = 2.7V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			70	100	mA
		I_{CCL}	V_{CC} = MAX, V_{IL} = 0.5V			100	145	mA
		I_{CCZ}	V_{CC} = MAX, V_{IL} = 0.5V			80	100	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, $V_X = V_{CC}$ for all test conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH}=1.6V and V_{IL}=1.3V.

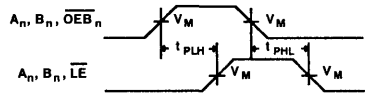
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay B to A	Waveform 1, 2	5.5 6.0	7.5 7.5	12.0 10.5	5.0 6.0	12.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time from High or Low OEA to A	Waveform 4.5	8.0 8.5	10.5 12.0	14.5 14.5	7.5 8.5	15.5 17.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low OEA to A	Waveform 4.5	2.0 2.0	4.5 4.5	7.0 7.5	2.0 2.0	7.5 8.0	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 9Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_D = 30pF, R_U = 9Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A to B	Waveform 1, 2	2.0 3.5	4.0 6.0	7.0 8.0	2.0 3.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to B	Waveform 1, 2	3.0 4.0	5.0 6.0	8.5 9.0	2.5 3.0	10.0 9.5	ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OEB_n}$ to B	Waveform 1, 2	2.5 4.5	4.5 7.5	7.5 10.5	1.5 3.5	8.5 10.5	ns
t_{TLH} t_{THL}	Transition time, B Port 1.3V to 1.7 V, 1.7V to 1.3V	Test Circuit and Waveform	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	4.5 4.5	ns

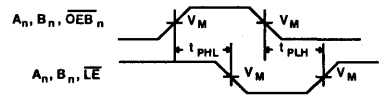
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Set-up time A to $\overline{LE}$	Waveform 3	5.0 5.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time A to $\overline{LE}$	Waveform 3	0.0 0.0			0.0 0.0		ns
t_w(L)	$\overline{LE}$ Pulse width, Low	Waveform 3	6.0			6.0		ns

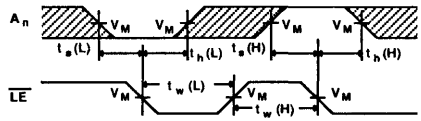
AC WAVEFORMS



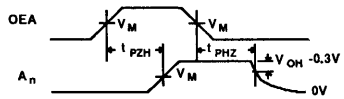
Waveform 1. Propagation Delay For Data To Output



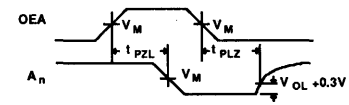
Waveform 2. Propagation Delay For Data To Output



Waveform 3. Data Setup And Hold Times And $\overline{LE}$ Pulse Widths



Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

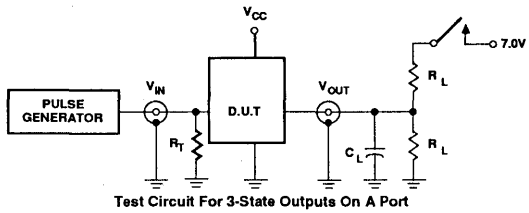


Waveform 5 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

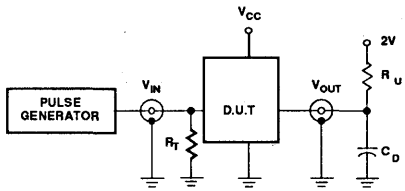
TEST CIRCUIT AND WAVEFORMS



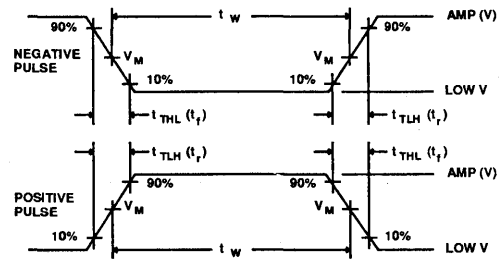
Test Circuit For 3-State Outputs On A Port

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test Circuit For Outputs On B Port



$V_M = 1.5V$

Input Pulse Definition

FAMILY 74F	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_U = Pull up resistor; see AC CHARACTERISTICS for value.

Signetics

FAST 74F777

Triple Bidirectional Latched Bus Transceiver

FAST Products

Triple Bidirectional Latched Bus Transceiver
(3-State + Open Collector)
Objective Specification

TYPE	TYPICAL PROPAGATION DELAY	MAX SUPPLY CURRENT (TOTAL)
74F777	ns	mA

FEATURES

- **Latching Transceiver**
- **High drive open collector output current with minimum output swing**
- **Compatible with Test Mode (TM) Bus specification**
- **Controlled output ramp**
- **Multiple package options**

DESCRIPTION

The 74F777 is a triple bidirectional latched Bus transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. This bus has a loaded characteristics impedance range of 20 to 50 ohms and is terminated on each end with a 30 to 40 ohm resistor.

The 74F777 is a triple bidirectional transceiver with open collector B and 3-state A port output drivers. A latch function is provided for the A port signals. The B port output driver is designed to sink 100 mA from 2 volts to minimize crosstalk and ringing on the bus.

A separate output threshold clamp voltage (V_X) is provided to prevent the A port output High level from exceeding future high density processor supply voltage levels. For 5 volt systems, V_X is simply tied to V_{CC}.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Ceramic DIP (300mil)[1]	N74F777F
20-Pin PLCC[1]	N74F777A

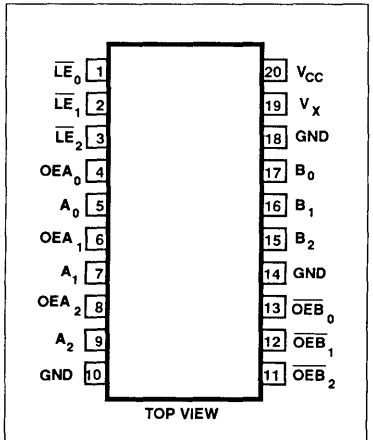
NOTE:
1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

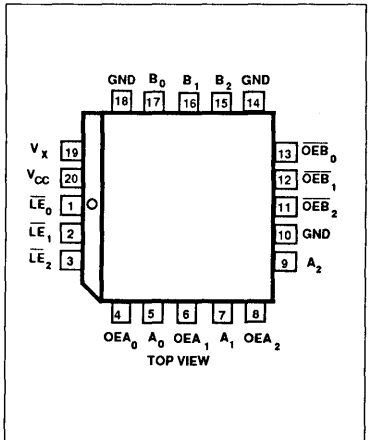
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_2	PNP latched inputs	3.5/0.117	70µA/70µA
B_0 - B_2	Data inputs with threshold circuitry	5.0/0.167	100µA/100µA
OEA_0 - OEA_2	A Output Enable inputs (active High)	1.0/0.033	20µA/20µA
$\overline{OEB}_0$ - $\overline{OEB}_2$	B Output Enable inputs (active Low)	1.0/0.033	20µA/20µA
$\overline{LE}_0$ - $\overline{LE}_2$	Latch Enable inputs (active Low)	1.0/0.033	20µA/20µA
A_0 - A_2	3-State outputs	150/40	3mA/24mA
B_0 - B_2	Open Collector outputs	OC*/166.7	OC*/100mA

NOTES:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
* OC = Open Collector

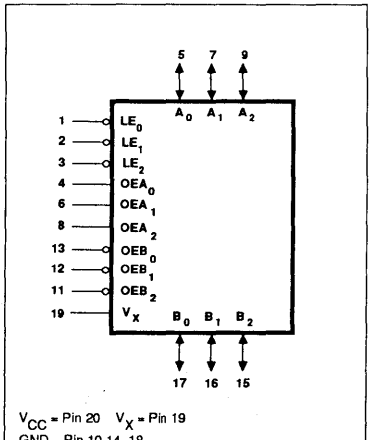
PIN CONFIGURATION



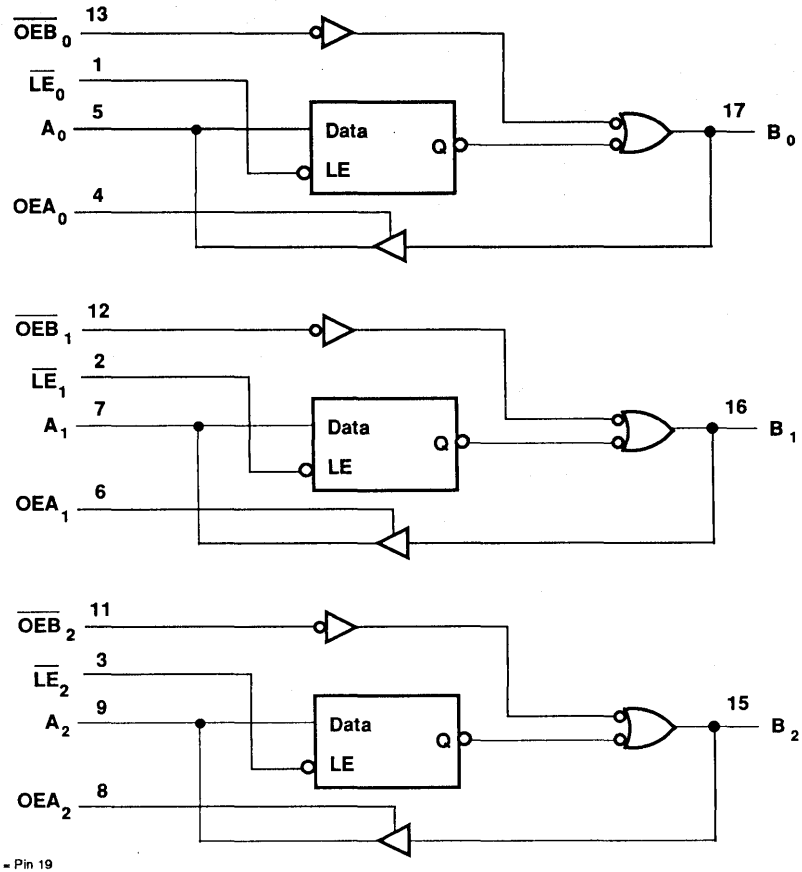
PIN CONFIGURATION PLCC



LOGIC SYMBOL



LOGIC DIAGRAM



V_{CC} = Pin 20 V_X = Pin 19
GND = Pin 10, 14, 18

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_X	Threshold control		-0.5 to +7.0	V
V_{IN}	Input voltage	$\overline{OEB_n}$, OEA_n, $\overline{LE_n}$	-0.5 to +7.0	V
		A_0 - A_2, B_0 - B_2	-0.5 to 5.5	
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A_0 - A_2	48	mA
		B_0 - B_2	200	
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except B_0 - B_2	2.0			V
		B_0 - B_2	1.6			
V_{IL}	Low-level input voltage	Except B_0 - B_2			0.8	V
		B_0 - B_2			1.45	
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0 - A_2			-3	mA
I_{OL}	Low-level output current	A_0 - A_2			24	mA
		B_0 - B_2			100	
V_{OH}	High-level output voltage	B_0 - B_2		2.0	4.0	V
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
I_{OH}	High level output current	B_0 - B_2	V_{CC} = MAX, V_{IL} =MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
I_{OFF}	Power-off output current	B_0 - B_2	V_{CC} = 0.0V, V_{IL} =MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
V_{OH}	High-level output voltage	A_0 - A_2[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3mA, V_X = V_{CC}	2.5		V_{CC}	V
				I_{OH} = -0.4mA, V_X = 3.13V & 3.47V	2.5		V_X	V
V_{OL}	Low-level output voltage	A_0 - A_2[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20mA, V_X = V_{CC}			0.5	V
		B_0 - B_2	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA			1.15	V
				I_{OL} = 4mA	0.40			V
V_{IK}	Input clamp voltage	A_0 - A_2	V_{CC} = MIN, I_I = I_{IK}				-0.5	V
		Except A_0 - A_2	V_{CC} = MIN, I_I = I_{IK}				-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEB}_n$, OEA_n, $\overline{LE}_n$	V_{CC} = 0.0V, V_I = 7.0V				100	µA
		A_0 - A_2, B_0 - B_2	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High-level input current	$\overline{OEB}_n$, OEA_n, $\overline{LE}_n$	V_{CC} = MAX, V_I = 2.7V, B_n - A_n = 0V				20	µA
		B_0 - B_2	V_{CC} = MAX, V_I = 2.1V				100	µA
I_{IL}	Low-level input current	$\overline{OEB}_n$, OEA_n, $\overline{LE}_n$	V_{CC} = MAX, V_I = 0.5V				-20	µA
		B_0 - B_2	V_{CC} = MAX, V_I = 0.3V				-100	µA
I_{OZH} + I_{IH}	Off-state output current, High-level voltage applied	A_0 - A_2	V_{CC} = MAX, V_O =2.7V				70	µA
I_{OZL} + I_{IL}	Off-state output current, Low-level voltage applied	A_0 - A_2	V_{CC} = MAX, V_O =0.5V				-70	µA
I_X	High-level control current		V_{CC} = MAX, V_X = V_{CC}, $\overline{LE}$ = OEA_n = $\overline{OEB}_n$ = 2.7V, A_0 - A_2 = 2.7V, B_0 - B_2 = 2.0V		-100		100	µA
			V_{CC} = MAX, V_X = 3.13V & 3.47 V, $\overline{LE}$ = OEA_n = 2.7V, $\overline{OEB}_n$ = A_0 - A_7 = 2.7V, B_0 - B_2 = 2.0V		-10		10	mA
I_{OS}	Short-circuit output current[3]	A_0 - A_2 only	V_{CC} = MAX, B_n = 1.6V, OEA_n = 2.0V, $\overline{OEB}_n$ = 2.7V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			70	100	mA
		I_{CCL}	V_{CC} = MAX, V_{IL} = 0.5V			100	145	mA
		I_{CCZ}	V_{CC} = MAX, V_{IL} = 0.5V			80	100	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, V_X = V_{CC} for all test conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH}=1.6V and V_{IL}=1.3V.

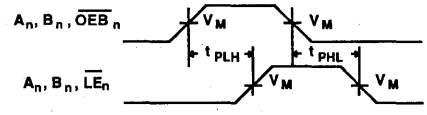
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay B to A	Waveform 1, 2	5.5 6.0	8.5 8.5	12.0 11.5	4.5 6.0	13.5 12.0	ns
t_{PZH} t_{PZL}	Output Enable time from High or Low OEA_n to A	Waveform 4.5	8.0 8.5	10.5 12.5	13.5 16.0	7.0 8.5	16.5 19.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low OEA_n to A	Waveform 4.5	2.0 2.0	3.0 3.0	8.0 8.0	2.0 2.0	8.5 8.5	ns
t_{TLH} t_{THL}	Transition time, B Port 0.8V to 1.8 V, 1.8V to 0.8V	Test Circuit and Waveform	0.5 0.5	2.5 2.0	5.0 5.0	0.5 0.5	6.0 6.0	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 9Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_D = 30pF, R_U = 9Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A to B	Waveform 1, 2	1.5 3.5	4.0 6.0	7.0 9.0	1.0 2.5	9.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}_n$ to B	Waveform 1, 2	3.0 4.0	5.0 6.0	8.0 9.0	2.0 3.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OEB}_n$ to B	Waveform 1, 2	2.5 3.0	4.5 7.5	7.5 10.5	1.5 3.0	8.5 11.0	ns
t_{TLH} t_{THL}	Transition time, B Port 1.3V to 1.7 V, 1.7V to 1.3V	Test Circuit and Waveform	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	4.5 4.5	ns

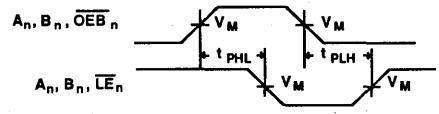
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 30pF, R_U = 9Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 30pF, R_U = 9Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time A to $\overline{LE}$	Waveform 3	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time A to $\overline{LE}$	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	$\overline{LE}$ Pulse width, High or Low	Waveform 3	15.0 15.0			15.0 15.0		ns

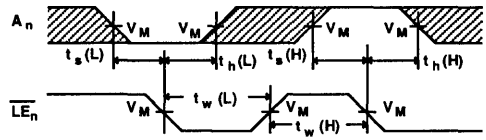
AC WAVEFORMS



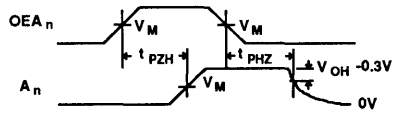
Waveform 1. Propagation Delay For Data To Output



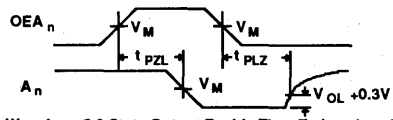
Waveform 2. Propagation Delay For Data To Output



Waveform 3. Data Setup And Hold Times And $\overline{LE}$ Pulse Widths



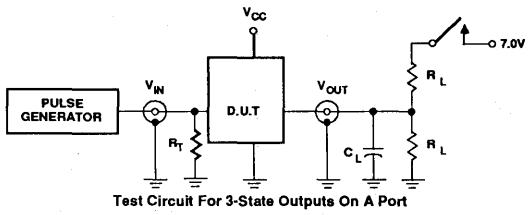
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

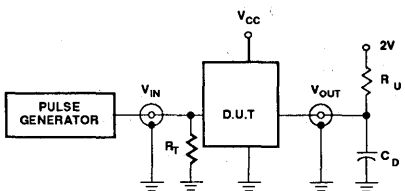
TEST CIRCUIT AND WAVEFORMS



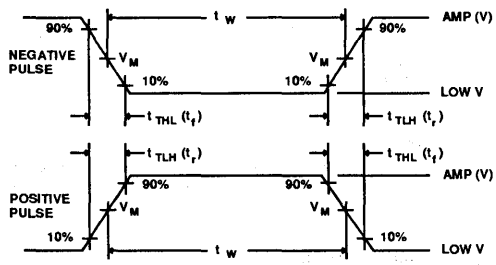
Test Circuit For 3-State Outputs On A Port

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test Circuit For Outputs On B Port



$V_M = 1.5V$

Input Pulse Definition

FAMILY 74F	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_U = Pull up resistor; see AC CHARACTERISTICS for value.

Signetics

FAST 74F779 Counter

8-Bit Bidirectional Binary Counter (3-state)

FAST Products

FEATURES

- **Multiplexed 3-state I/O ports for bus oriented applications**
- **Built-in look-ahead carry capability**
- **Center power pins to reduce effects of package inductance**
- **Count frequency 145MHz typical**
- **Supply current 90mA typical**
- **See 'F269 for 24 pin separate I/O port version**
- **See 'F579 for 20 pin version**
- **See 'F579 for 20 pin version**
- **See 'F1179 for extended function version of the 'F799**

DESCRIPTION

The 74F779 is fully synchronous 8-stage Up/Down Counter with multiplexed 3-state I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pins (S_0,S_1). The device also features carry look-ahead for easy cascading. All state changes are initiated by the rising edge of the clock. When $\overline{CET}$ is HIgh the data outputs are held in their current state and $\overline{TC}$ is held High. The $\overline{TC}$ output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F779	145MHz	90mA

ORDERING INFORMATION

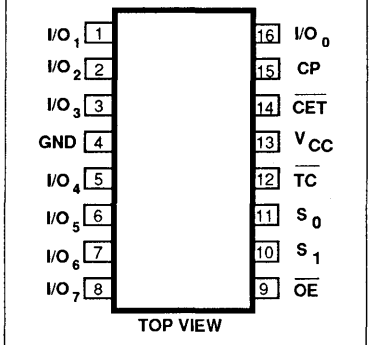
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F779N
16-Pin Plastic SOL	N74F779D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/O_n	Data inputs	3.5/1.0	70µA/0.6mA
	Data outputs	150/40	3.0mA/24mA
S_0,S_1	Select inputs	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{TC}$	Terminal count output (active Low)	50/33	1.0mA/20mA

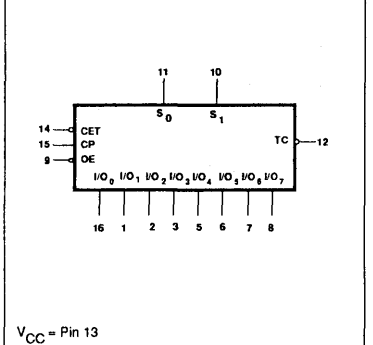
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



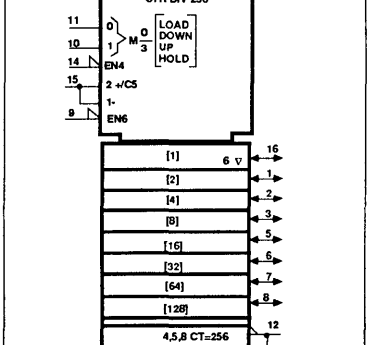
TOP VIEW

LOGIC SYMBOL

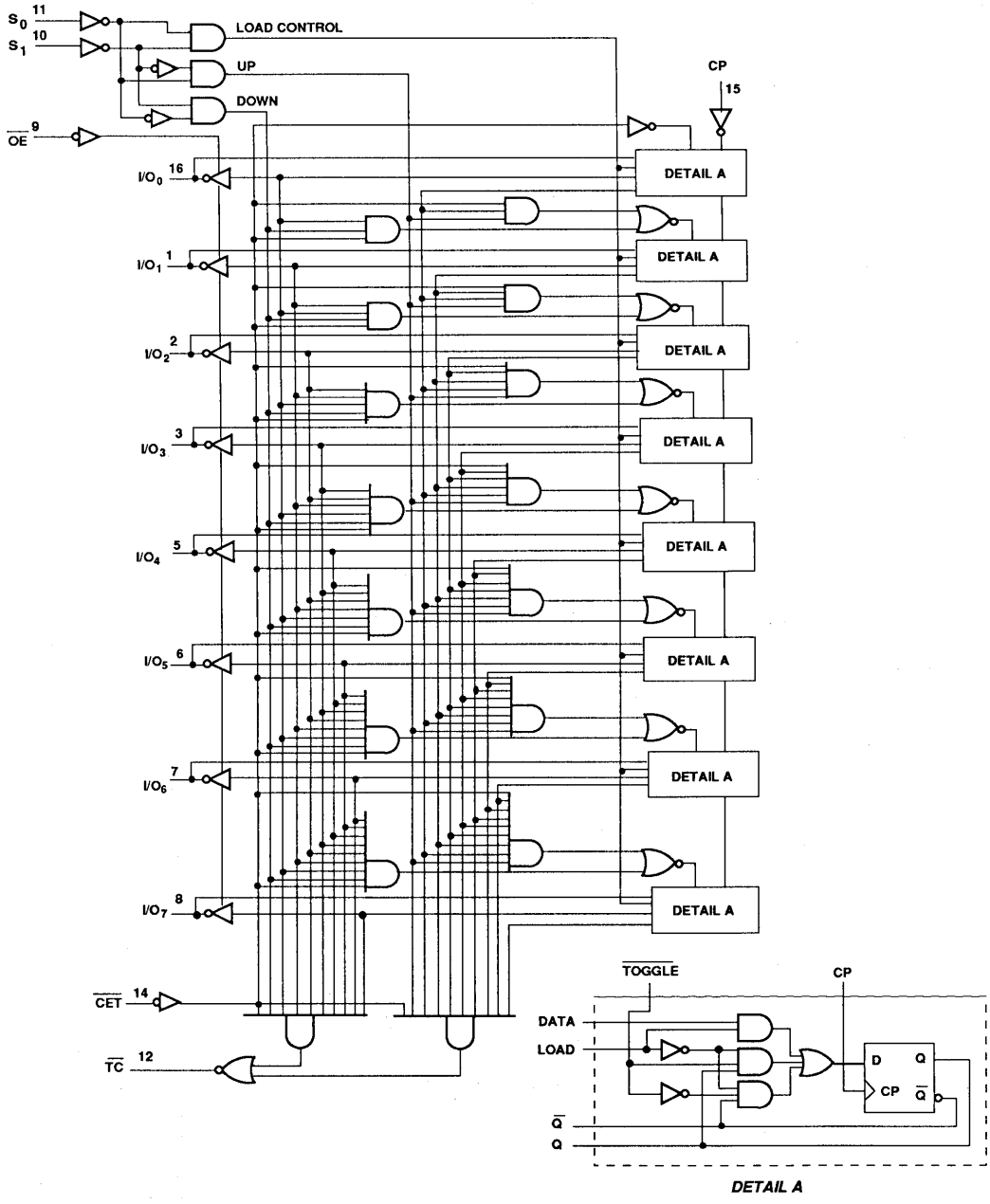


V_{CC} = Pin 13
GND = Pin 4

LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = pin 13
GND= pin 4

FUNCTION TABLE

INPUTS					OPERATING MODE
S_1	S_0	$\overline{CET}$	$\overline{OE}$	CP	
X	X	X	H	X	I/O_0 to I/O_7 in high impedance
X	X	X	L	X	Flip-flop outputs appears on I/O lines
L	L	X	H	↑	Parallel load all flip-flops
(not LL)		H	X	↑	Hold ($\overline{TC}$ held High)
H	L	L	X	↑	Count up
L	H	L	X	↑	Count down

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
(not LL) = S_0 and S_1 should never be Low voltage level at the same time in the hold mode only.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	$\overline{TC}$	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	$\overline{TC}$			-1	mA
		I/O_n			-3	mA
I_{OL}	Low-level output current	$\overline{TC}$			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$\overline{TC}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	I/O_n	V_{CC} = 5.5V, V_I = 5.5V					1	mA
		others	V_{CC} = 5.5V, V_I =7.0V					100	µA
I_{IH}	High-level input current	except I/O_n	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied	I/O_n	V_{CC} = MAX, V_O= 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-600	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				82	116	mA
		I_{CCL}					91	128	mA
		I_{CCZ}					97	136	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

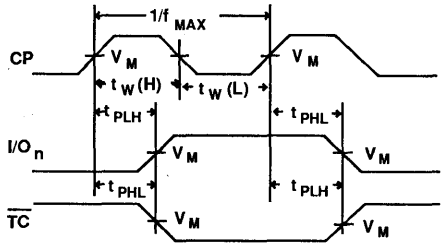
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	125	145		115		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	4.5 5.5	7.0 8.0	10.5 10.5	4.5 5.5	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	4.5 4.5	7.0 7.0	9.0 9.0	4.5 4.5	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	3.0 3.0	4.5 5.5	6.5 7.5	2.5 2.5	7.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time from High or Low level	Waveform 4 Waveform 5	2.5 4.5	4.5 6.5	7.0 9.0	2.5 4.5	8.0 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 4 Waveform 5	1.0 1.0	3.0 4.0	6.5 7.0	1.0 1.0	8.0 8.0	ns

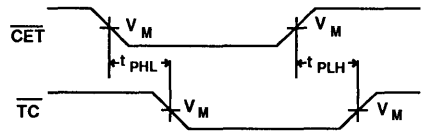
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 3	5.0 5.0			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CET}$ to CP	Waveform 3	5.0 5.5			5.0 6.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CET}$ to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_n to CP	Waveform 3	8.0 8.0			8.5 8.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_n to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 4.0			4.0 4.0		ns

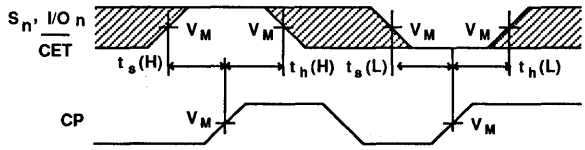
AC WAVEFORMS



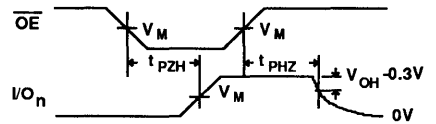
Waveform 1.
Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



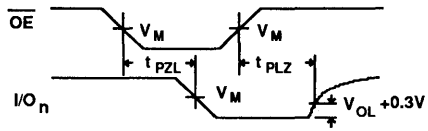
Waveform 2.
Propagation Delay, $\overline{CET}$ input to Terminal Count Output



Waveform 3. Data Setup And Hold Times



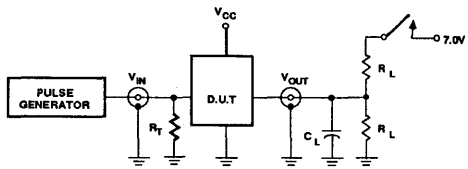
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

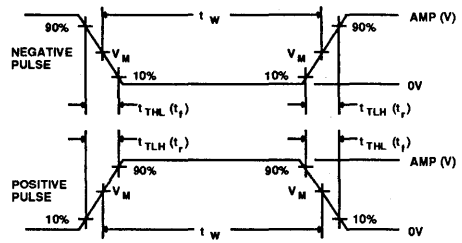
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F786
Asynchronous Bus Arbiter

4-Bit Asynchronous Bus Arbiter
Product Specification

FAST Products

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N74F786	6.6ns	55mA

FEATURES
- **Arbitrates between 4 asynchronous inputs**
- **Separate grant output for each input**
- **Common output enable**
- **On-board 4 input AND gate**
- **Metastable-free outputs**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F786N
16-Pin Plastic SO	N74F786D

DESCRIPTION

The 74F786 is an asynchronous 4-bit arbiter designed for high speed real-time applications. The priority of arbitration is determined on a first-come first-served basis. Separate Bus Grant ($\overline{BG}_n$) outputs are available to indicate which one of the request inputs is served by the arbitration logic. All $\overline{BG}$ outputs are enabled by a common enable ($\overline{EN}$) pin. In order to generate a bus request signal a separate 4 input AND gate is provided which may also be used as an independent AND gate. Unused Bus Request ($\overline{BR}_n$) inputs may be disabled by tying them High.

The 'F786 is designed so that contention between two or more request signals will not glitch or display a metastable condition. In this situation an increase in the $\overline{BR}_n$ to $\overline{BG}_n$ t_{PHL} may be observed. A typical 'F786 has an h = 6.6ns, τ = .41ns and and T_0 = 5µsec.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{BR}_0$ - $\overline{BR}_3$	Bus Request inputs (active Low)	1.0/3.0	20µA/1.8mA
A, B, C, D	AND gate inputs	1.0/1.0	20µA/0.6mA
$\overline{EN}$	Common Bus Grant output enable input (active Low)	1.0/1.0	20µA/0.6mA
Y_{OUT}	AND gate output	150/40	3.0mA/24mA
$\overline{BG}_0$ - $\overline{BG}_3$	Bus Grant outputs (active Low)	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

Where:

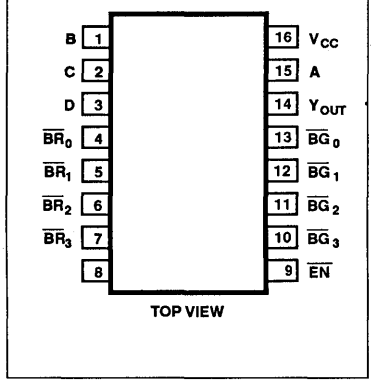
h= Typical propagation delay through the device and τ and T_0 are device parameters derived from test results and can most nearly be defined as:

τ= A function of the rate at which a latch in a metastable state resolves that condition.

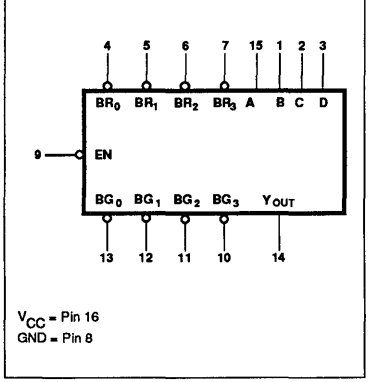
T_0= A function of the measurement of the propensity of a latch to enter a metastable state. T_0 is also a very strong function of the normal propagation delay of the device.

For further information, please refer to the 'F786 application notes.

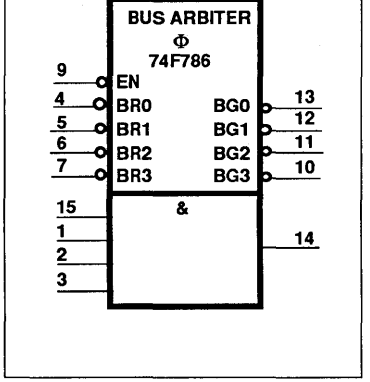
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



FUNCTIONAL DESCRIPTION

The $\overline{BR}_n$ inputs have no inherent priority. The arbiter assigns priority to the incoming requests as they are received, therefore, the first $\overline{BR}$ asserted will have the highest priority. When a bus request is received its corresponding bus grant becomes active, provided that $\overline{EN}$ is Low. If additional bus requests are made during this time they are queued. When the first request is removed, the arbiter services the bus request with the next highest priority. Removing a request while a previous request is being serviced can cause a grant to be changed when arbitrating between three or four requests. For that reason, the user should not remove ungranted requests when arbitrating between three or four requests. This does not apply to arbitration between two requests.

If two or more $\overline{BR}_n$ inputs are asserted at precisely the same time, one of them will be selected at random, and all $\overline{BG}_n$ outputs will be held in the High state until the selection is made. This guarantees that an erroneous $\overline{BG}_n$ will not be generated even though a metastable condition may occur internal to the device.

When the $\overline{EN}$ is in the High state the $\overline{BG}_n$ outputs are forced High.

PIN DESCRIPTION

SYMBOL	PINS	TYPE	NAME	FUNCTION
$\overline{BR}_0$ - $\overline{BR}_3$	4 - 7	I	Bus Request inputs (Active Low)	The logic of this device arbitrates between these four inputs. Unused inputs should be tied high.
$\overline{BG}_0$ - $\overline{BG}_3$	13 - 10	O	Bus Grant outputs (Active Low)	These outputs indicate the selected bus request. $\overline{BG}_0$ corresponds to $\overline{BR}_0$, $\overline{BG}_1$ to $\overline{BR}_1$, etc.
A, B, C, D	15, 1 - 3	I	Inputs of the 4-input AND gate.	
Y_{OUT}	14	O	Output of the 4-input AND gate.	
$\overline{EN}$	9	I	Enable input	When Low it enables the $\overline{BR}_0$ - $\overline{BR}_3$ outputs.

ARBITER FUNCTION TABLE

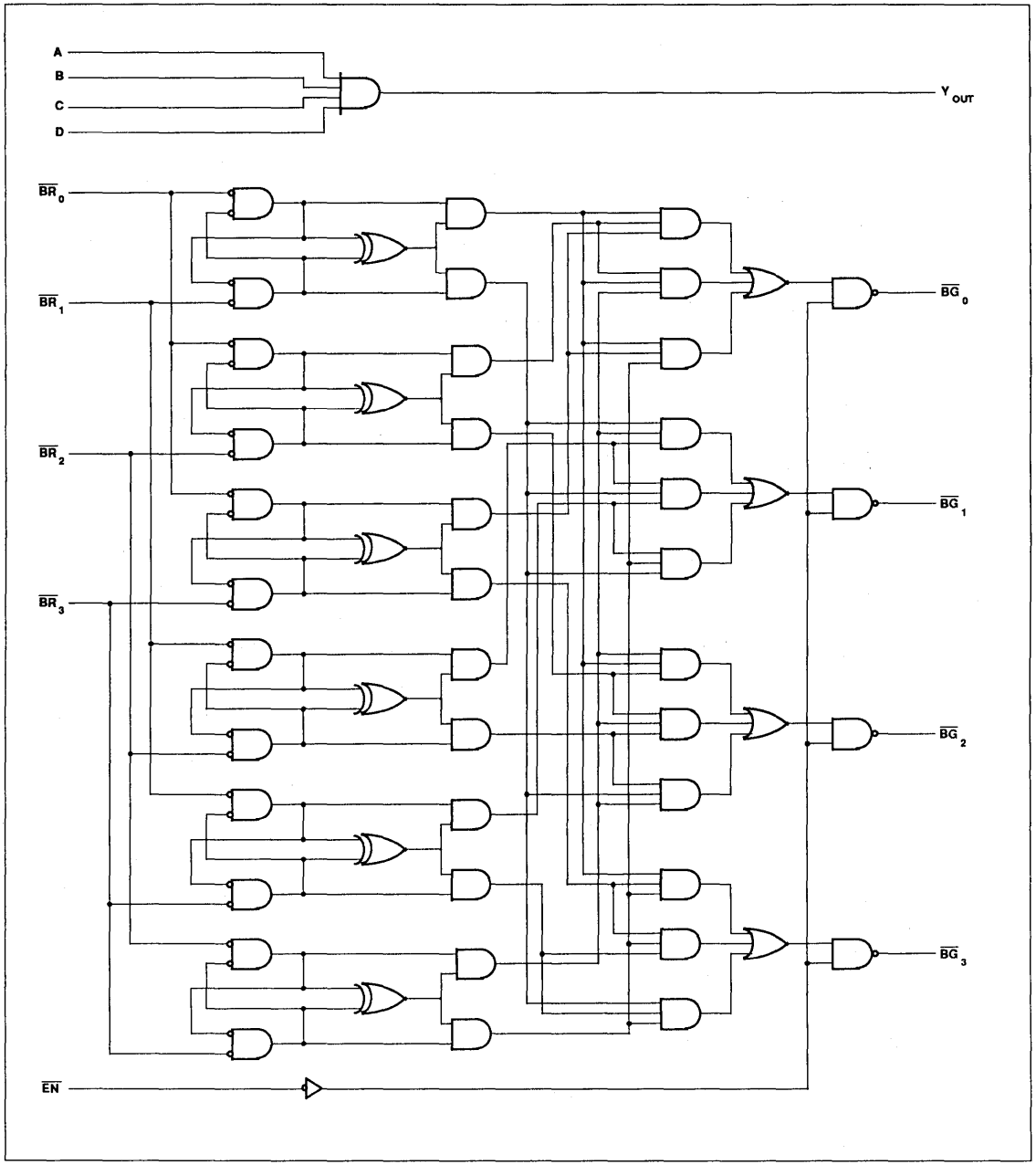
INPUTS					OUTPUTS			
$\overline{EN}$	$\overline{BR}_0$	$\overline{BR}_1$	$\overline{BR}_2$	$\overline{BR}_3$	$\overline{BG}_0$	$\overline{BG}_1$	$\overline{BG}_2$	$\overline{BG}_3$
L	1	X	X	X	L	H	H	H
L	X	1	X	X	H	L	H	H
L	X	X	1	X	H	H	L	H
L	X	X	X	1	H	H	H	L
H	X	X	X	X	H	H	H	H

L = Low voltage level
H = High voltage level
X = Don't care
1 = First of inputs to go Low

AND FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y_{OUT}
L	L	L	L	L
L	L	L	H	L
L	L	H	L	L
L	L	H	H	L
L	H	L	L	L
L	H	L	H	L
L	H	H	L	L
L	H	H	H	L
H	L	L	L	L
H	L	L	H	L
H	L	H	L	L
H	L	H	H	L
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	H

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	A-D, $\overline{EN}$	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		$\overline{BR}_n$					-1.8	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			55	80	mA

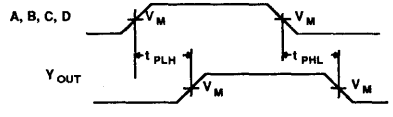
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

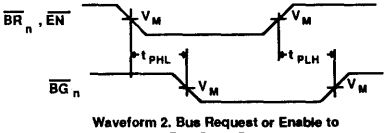
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B, C, D to Y_{OUT}	Waveform 1	2.5 2.5	4.5 4.5	7.5 7.5	2.0 2.5	8.5 7.5	MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{BR}_n$ to $\overline{BG}_n$	Waveform 2	5.0 4.5	7.0 6.5	10.0 9.5	4.5 4.0	10.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EN}$ to $\overline{BG}_n$	Waveform 2	3.0 2.5	5.0 4.5	8.0 7.5	2.5 2.5	8.5 8.0	ns
t_{PHL}	Propagation delay, $\overline{BR}_a$ to $\overline{BG}_b$	Waveform 3	5.0	7.0	10.0	4.5	10.5	ns

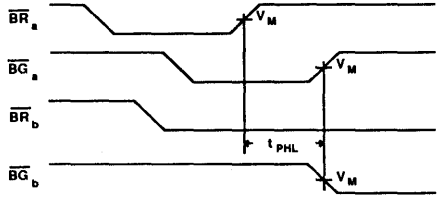
AC WAVEFORMS



Waveform 1. AND Gate Input to Output Delays



Waveform 2. Bus Request or Enable to Bus Grant Delays

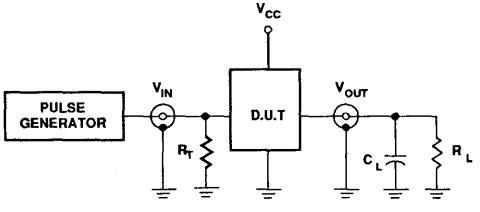


Waveform 3. Bus Request to Bus Grant Delay

NOTE: a and b represent any of the Bus Requests or Grants. $\overline{BG}_a$ Low-to-High transition and the $\overline{BG}_b$ High-to-Low transition occur simultaneously.

For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



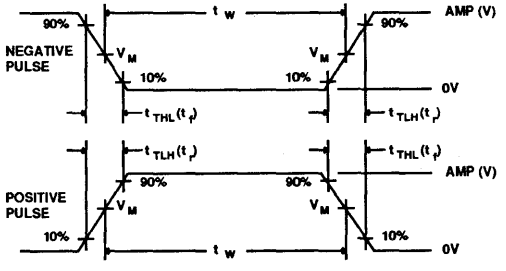
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F804, 74F1804
NAND DRIVERS

FAST Products

74F804-Hex Two-Input NAND Driver
74F1804-Hex Two-Input NAND Driver
Product Specification

FEATURES
- **High capacitive drive capability**
- **Choice of configuration**
  Corner V_{CC} and GND-- 'F804
  Center V_{CC} and GND-- 'F1804
- **Typical propagation delay of 2.5ns**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F804	2.5ns	9mA
74F1804	2.5ns	9mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F804N, N74F1804N
20-Pin Plastic SOL	N74F804D, N74F1804D

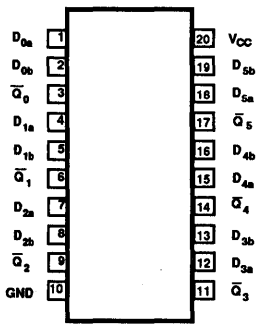
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na} - D_{nb}	Data inputs	1.0/0.033	20µA/20µA
$\overline{Q}_0$ - $\overline{Q}_5$	Data outputs	2400/80	48mA/48mA

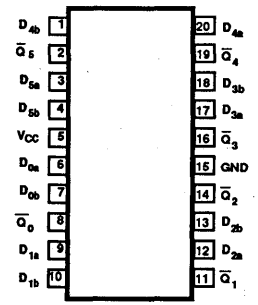
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

'F804

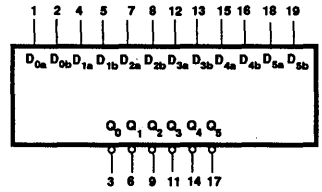


'F1804



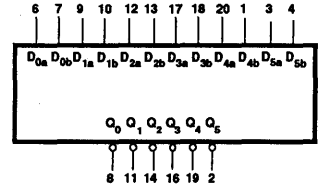
LOGIC SYMBOL

'F804



V_{CC} = Pin 20
GND = Pin 10

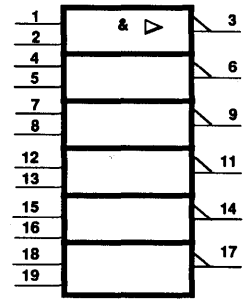
'F1804



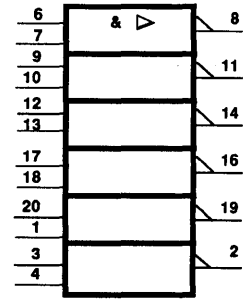
V_{CC} = Pin 5
GND = Pin 15

LOGIC SYMBOL(IEEE/IEC)

'F804



'F1804



FUNCTION TABLE

INPUTS		OUTPUT
D_a	D_b	$\overline{Q}$
L	X	H
X	L	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	96	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-48	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

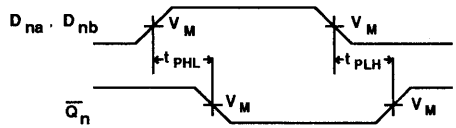
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.0			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.38	0.55	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_O	Output current[3]		V_{CC} = MAX, V_O=2.25V		-60		-160	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} =GND		2.0	3.0	mA
		I_{CCL}		V_{IN} =4.5V		15	20	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to $\overline{Q}_n$	Waveform 1	1.0 1.0	2.0 3.0	4.0 4.5	1.0 1.0	4.0 5.0	ns

AC WAVEFORMS

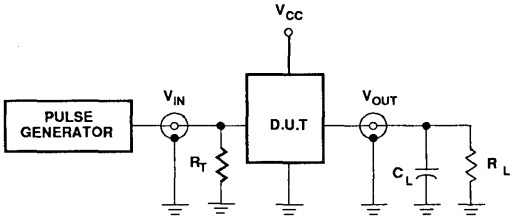


Waveform 1.

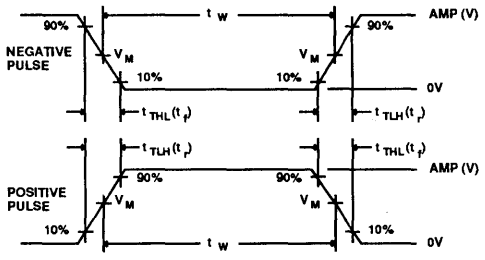
Propagation Delay for Input to Output

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F805, 74F1805
NOR Drivers

FAST Products

74F805-Hex Two-Input NOR Driver
74F1805-Hex Two-Input NOR Driver
Product Specification

FEATURES
- **High capacitive drive capability**
- **Choice of configuration**
  Corner V_{CC} and GND-- 'F805
  Center V_{CC} and GND-- 'F1805
- **Typical propagation delay of 2.3ns**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F805	2.3ns	10mA
74F1805	2.3ns	10mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F805N, N74F1805N
20-Pin Plastic SOL	N74F805D, N74F1805D

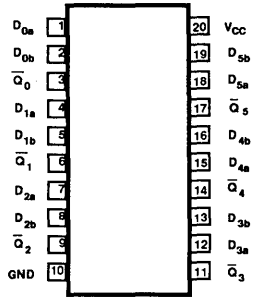
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na} - D_{nb}	Data inputs	1.0/0.033	20µA/20µA
$\overline{Q}_0$ - $\overline{Q}_5$	Data outputs	2400/80	48mA/48mA

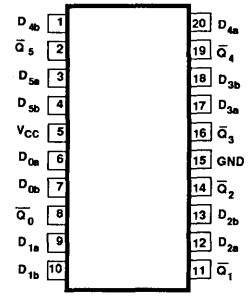
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

'F805

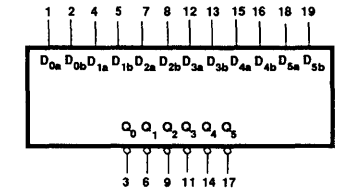


'F1805



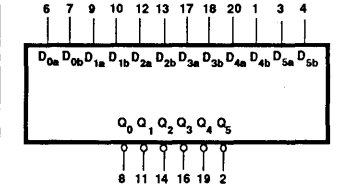
LOGIC SYMBOL

'F805



VCC = Pin 20
GND = Pin 10

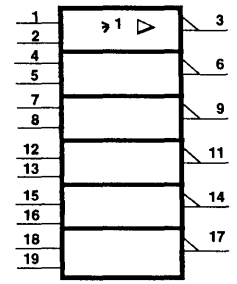
'F1805



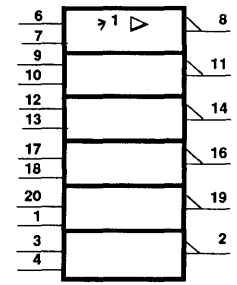
VCC = Pin 5
GND = Pin 15

LOGIC SYMBOL(IEEE/IEC)

'F805



'F1805



FUNCTION TABLE

INPUTS		OUTPUT
D_{na}	D_{nb}	$\overline{Q}_n$
H	X	L
X	H	L
L	L	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	96	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-48	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

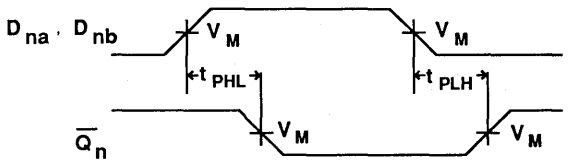
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.0			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.38	0.55	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_O	Output current[3]		V_{CC} = MAX, V_O=2.25V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	V_{IN} =GND		3	5	mA
		I_{CCL}		V_{IN} =4.5V		17	25	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to $\overline{Q}_n$	Waveform 1	1.0 1.0	2.0 2.5	4.0 4.5	1.0 1.0	4.0 4.5	ns

AC WAVEFORMS

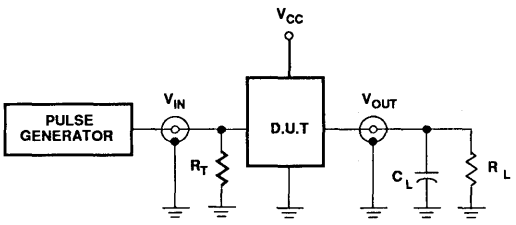


Waveform 1.

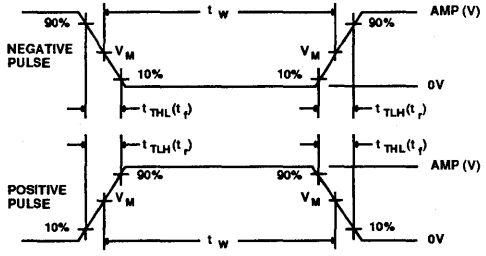
Propagation Delay for Input to Output

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F807

Octal Shift/Count Registered Transceiver with Adder and Parity (3-State)

Preliminary Specification

FEATURES

- **High speed parallel registers with positive edge-triggered D-type flip-flops**
- **High speed full adder**
- **8-bit parity generator**
- **High impedance PNP inputs for light bus loading**
- **Center V_{CC} and GND pins and controlled output buffers minimize ground-bounce problems**
- **3-state outputs glitch free during power-up and power-down**
- **Broadside pinout**

DESCRIPTION

The 74F807 Octal Bus, Shift/Count Transceiver is designed to input data from either the A or B ports to an internal storage register. This data can then be shifted left with serial or parallel outputs, added to additional data that appears on the A-input with Carry In and Carry Out bits, incremented by the Clock Input or incremented by the Clock enabled with Carry In. An 8-bit odd parity generator is attached to the register Q Outputs.

The data in the storage register can be presented on either the A or B ports for output.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F807	100MHz	210mA

ORDERING INFORMATION

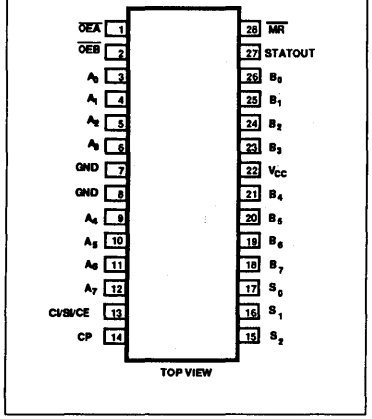
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP (600 mils)	N74F807N
28-Pin SOL	N74F807D
28-Pin PLCC	N74F807A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

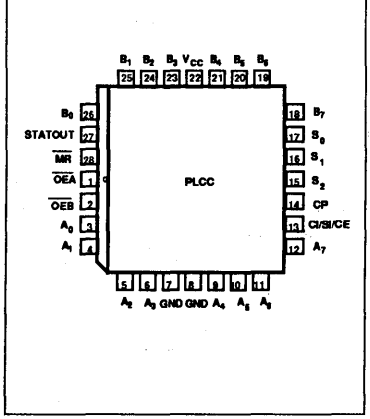
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_n, B_n	Data I/O inputs	3.5/0.166	70µA/70µA
$\overline{OEA}$, $\overline{OEB}$	Output Enable inputs	1.0/0.033	20µA/20µA
CI/SI/CE	Carry/Serial/Clock Enable input	1.0/0.033	20µA/20µA
CP	Clock input	1.0/0.033	20µA/20µA
$\overline{MR}$	Master Reset input	1.0/0.033	20µA/20µA
S_n	Select inputs	1.0/0.033	20µA/20µA
STATOUT	Status Out output	150/40	3.0mA/24mA
A_n, B_n	Data I/O outputs	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

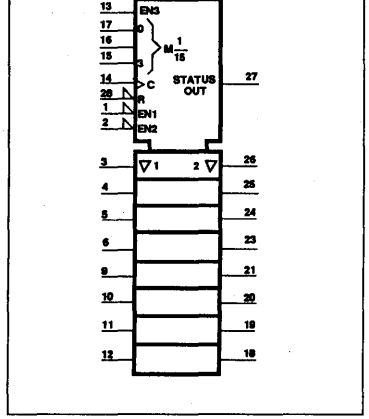
DIP PIN CONFIGURATION



PLCC PIN CONFIGURATION

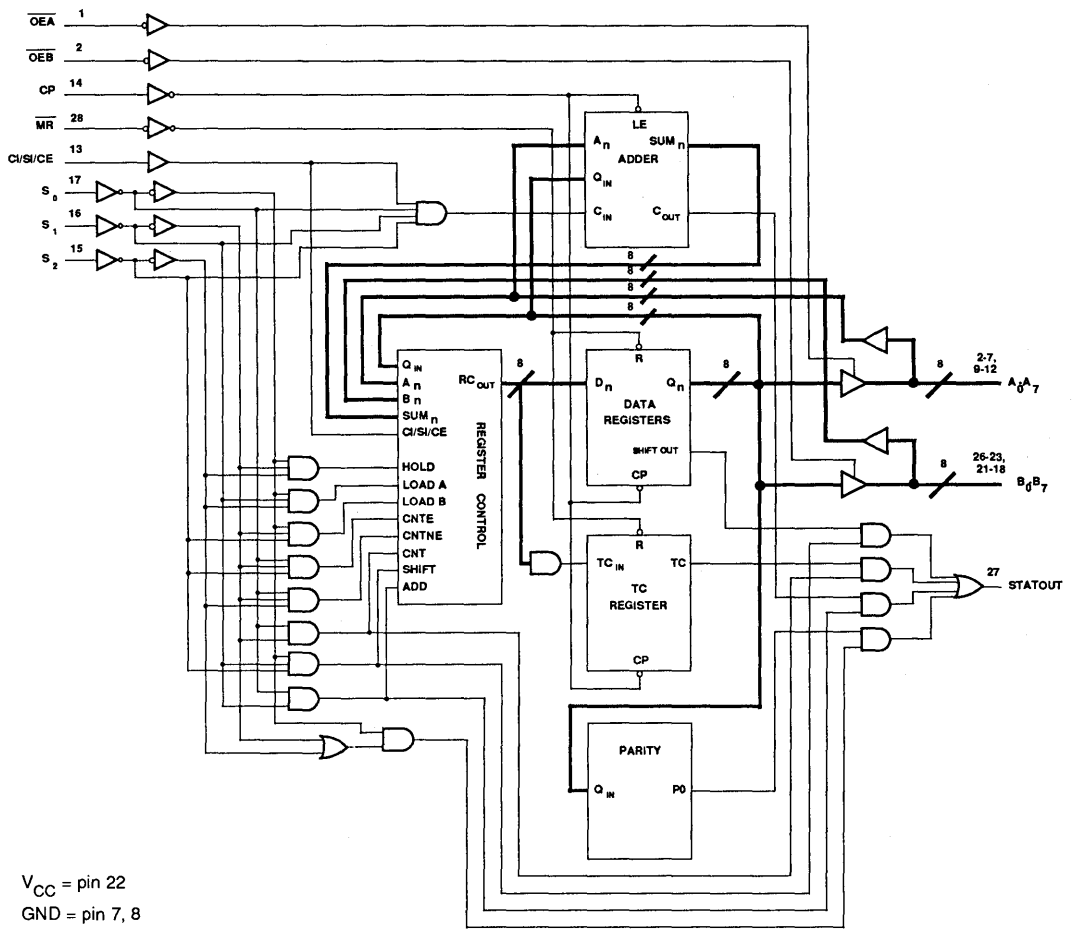


LOGIC SYMBOL(IEEE/IEC)



Octal Shift/Count Transceiver | FAST 74F807

LOGIC DIAGRAM



Octal Shift/Count Transceiver — FAST 74F807

FUNCTION TABLE

INPUTS								INTERNAL REGISTER	DATA I/O		OUTPUT	OPERATING MODE
$\overline{MR}$	CP	$\overline{OE}_a$	$\overline{OE}_b$	S_0	S_1	S_2	CI/SI/CE	Q_n	A_n	B_n	STATOUT	
L	X	L	L	X	X	X	X	L	L	L	(1)	Clear
L	X	L	H	X	X	X	X	L	L	Z	(1)	
L	X	H	L	X	X	X	X	L	Z	L	(1)	
X	X	H	H	X	X	X	X	X	Z	Z	X	3-State
H	↑	X	L	L	L	L	CI/SI/CE	CI/SI/CE + a_{n0} + q_{n0}	a_{n1}	CI/SI/CE + a_{n0} + q_{n0}	C_{OUT}	Add Mode w/Carry In
H	↑	X	L	L	L	H	X	a_{n0} + q_{n0}	a_{n1}	a_{n0} + q_{n0}	C_{OUT}	Add Mode wo/Carry In
H	↑	H	L	L	H	L	H	q_{n0} + 1	Z	q_{n0} + 1	TC(2)	Count w/Count Enable (count)
H	↑	L	H	L	H	L	H	q_{n0} + 1	q_{n0} + 1	Z	TC(2)	
H	↑	L	L	L	H	L	H	q_{n0} + 1	q_{n0} + 1	q_{n0} + 1	TC(2)	
H	X	H	L	L	H	L	L	q_{n0}	Z	q_{n0}	TC(2)	Count w/Count Enable (hold)
H	X	L	H	L	H	L	L	q_{n0}	q_{n0}	Z	TC(2)	
H	X	L	L	L	H	L	L	q_{n0}	q_{n0}	q_{n0}	TC(2)	
H	↑	H	L	L	H	H	X	q_{n0} + 1	Z	q_{n0} + 1	TC(2)	Count wo/Count Enable
H	↑	L	H	L	H	H	X	q_{n0} + 1	q_{n0} + 1	Z	TC(2)	
H	↑	L	L	L	H	H	X	q_{n0} + 1	q_{n0} + 1	q_{n0} + 1	TC(2)	
H	↑	H	L	H	L	L	CI/SI/CE	(4)	Z	(4)	Q_7	Shift
H	↑	L	H	H	L	L	CI/SI/CE	(4)	(4)	Z	Q_7	
H	↑	L	L	H	L	L	CI/SI/CE	(4)	(4)	(4)	Q_7	
H	↑	H	H	H	L	H	X	A_{n0}	a_{n0}	Z	Parity(3)	Load A Inputs
H	↑	H	L	H	L	H	X	A_{n0}	a_{n0}	A_{n0}	Parity(3)	
H	↑	L	X	H	L	H	X	Q_{n0}	q_{n0}	X	Parity(3)	
H	↑	H	H	H	H	L	X	B_{n0}	Z	b_{n0}	Parity(3)	Load B Inputs
H	↑	L	H	H	H	L	X	B_{n0}	B_{n0}	b_{n0}	Parity(3)	
H	↑	X	L	H	H	L	X	Q_{n0}	X	q_{n0}	Parity(3)	
H	X	L	H	H	H	H	X	Q_{n0}	Q_{n0}	Z	Parity(3)	Hold
H	X	H	L	H	H	H	X	Q_{n0}	Z	Q_{n0}	Parity(3)	
H	X	L	L	H	H	H	X	Q_{n0}	Q_{n0}	Q_{n0}	Parity(3)	

H = High voltage level.
L = Low voltage level.
a, b, q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition.
X = Don't care.
Z = High impedance.
↑ = Low-to-High clock transition.
(1) = If in count mode STATOUT=Low, STATOUT is not affected by $\overline{MR}$ in other modes.
(2) =Terminal count is High when the output is at terminal count (HHHHHHHH).
(3) = Parity is High for odd number of register outputs High, Low for even number of register outputs High.
(4) = CI/SI/CE→ Q_0→ Q_1, etc.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-20	µA
I_{OZH}+I_{IH}	Off-state output current High-level voltage applied	A_n, B_n	V_{CC} = MAX, V_O= 2.7V				70	µA
I_{OZL}+I_{IL}	Off-state output current Low-level voltage applied	A_n, B_n	V_{CC} = MAX, V_O= 0.5V				-70	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			190	220	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

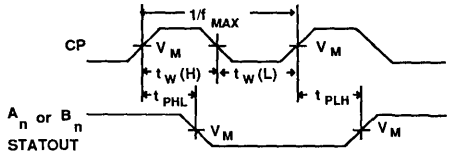
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	85	100		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to A_n or B_n	Waveform 1	7.0 7.0	9.0 9.0	12.0 12.5	2.5 2.0	14.0 13.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to A_n or B_n	Waveform 3	8.0	10.0	13.5	7.0	14.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to STATOUT	Waveform 1	8.0 5.5	9.5 7.0	12.5 10.0	6.5 5.0	15.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n to STATOUT	Waveform 4	9.0 6.0	15.0 13.0	20.0 21.5	8.0 5.5	22.5 24.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to STATOUT	Waveform 3	10.0	21.0	23.5	10.0	25.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to STATOUT	Waveform 4	3.5 3.5	11.5 8.0	14.0 10.5	3.5 3.0	16.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CI/SI/CE to STATOUT	Waveform 4	10.0 10.0	19.0 21.0	21.5 23.5	9.5 9.5	24.0 28.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEB}$ to B_n or $\overline{OEA}$ to A_n	Waveform 6 Waveform 7	2.0 2.0	6.0 6.0	8.5 8.5	1.5 1.5	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEB}$ to B_n or $\overline{OEA}$ to A_n	Waveform 6 Waveform 7	1.5 2.0	4.0 6.0	7.5 8.5	1.0 1.0	8.5 9.5	ns

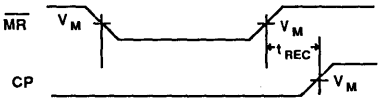
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n, B_n to CP	Waveform 5	6.0 8.0			7.0 9.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n, B_n to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_n to CP	Waveform 5	8.0 8.0			10.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_n to CP	Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low CI/SI/CE to CP	Waveform 5	8.0 8.0			10.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CI/SI/CE to CP	Waveform 5	0 0			0 0		ns
$t_w(H)$	CP Pulse width, High or Low	Waveform 1	4.0 3.5			5.0 4.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 3	4.0			4.5		ns
t_{REC}	Recovery Time, $\overline{MR}$ to CP	Waveform 2	4.0			5.0		ns

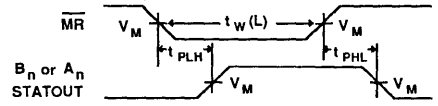
AC WAVEFORMS



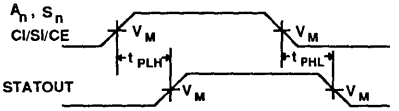
Waveform 1. Propagation Delay, Clock Input To Outputs, Clock Pulse Width, and Maximum Clock Frequency



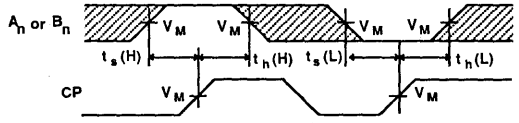
Waveform 2. Master Reset to Clock Recovery Time



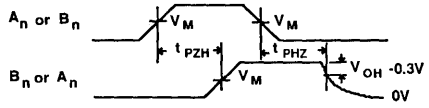
Waveform 3. Propagation Delay, Master Reset to Data or Master Reset to STATOUT



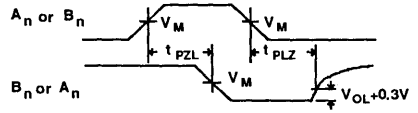
Waveform 4. Propagation Delay, Select to STATOUT, CI/SI/CE to STATOUT or Data to STATOUT



Waveform 5. Data Setup And Hold Times



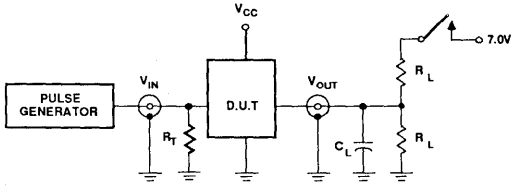
Waveform 6. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 7. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

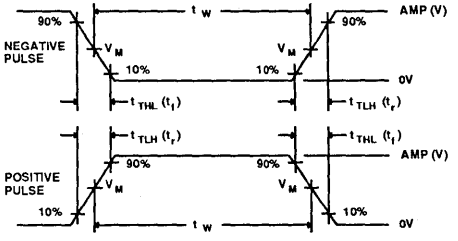
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F808, 74F1808 AND DRIVERS

FAST Products

74F808-Hex 2-Input AND Driver
74F1808-Hex 2-Input AND Driver
Preliminary Specification

FEATURES

- High capacitive drive capability
- Choice of configuration
  Corner V_{CC} and GND-- 'F808
  Center V_{CC} and GND-- 'F1808
- Typical propagation delay of 2.6ns

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F808	2.6ns	11mA
74F1808	2.6ns	11mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F808N, N74F1808N
20-Pin Plastic SOL	N74F808D, N74F1808D

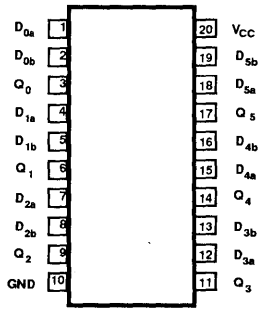
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na} - D_{nb}	Data inputs	1.0/0.033	20µA/20µA
Q_0 - Q_5	Data outputs	2400/80	48mA/48mA

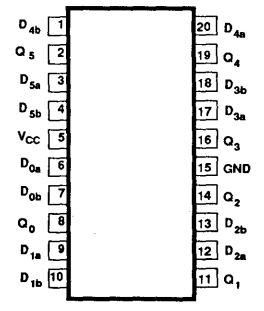
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

'F808

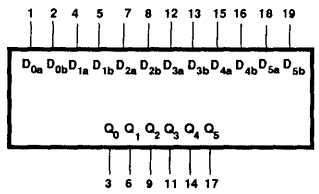


'F1808



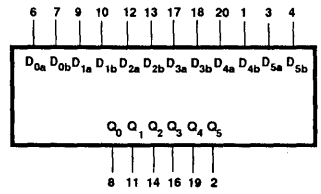
LOGIC SYMBOL

'F808



V_{CC} = Pin 20
GND = Pin 10

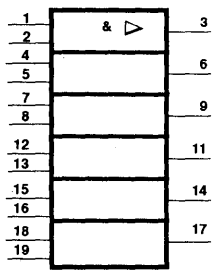
'F1808



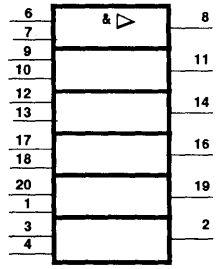
V_{CC} = Pin 5
GND = Pin 15

LOGIC SYMBOL(IEEE/IEC)

'F808



'F1808



FUNCTION TABLE

INPUTS		OUTPUT
D_{na}	D_{nb}	Q_n
L	X	L
X	L	L
H	H	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	96	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-48	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

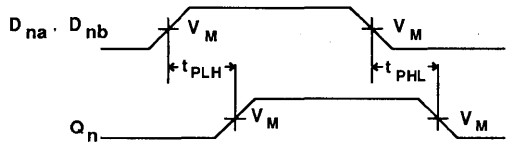
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.0			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.38	0.55	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximun input voltage		V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} =MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} =MAX, V_I = 0.5V				-20	µA
I_{OS}	Short circuit output current[3]		V_{CC} =MAX, V_O= 2.25V		-60		-160	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} =MAX	V_{IN} =GND		6.5	11	mA
		I_{CCL}		V_{IN} =4.5V		19	32	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to Q_n	Waveform 1	1.0 1.0	2.5 2.4	4.5 4.5	1.0 1.0	5.0 5.0	ns

AC WAVEFORMS

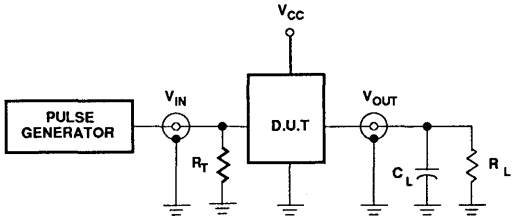


Waveform 1.

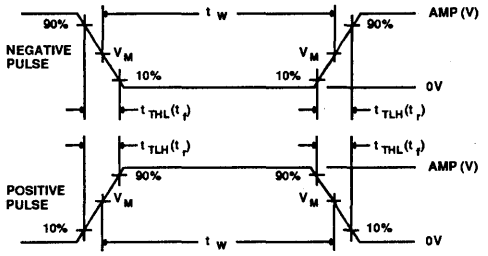
Propagation Delay for Input to Output

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F821/822/823/824/825/826

Bus Interface Registers

'F821/'F822 10-Bit Bus Interface Registers, NINV/INV (3-State)
'F823/'F824 9-Bit Bus Interface Registers, NINV/INV (3-State)
'F825/'F826 8-Bit Bus Interface Registers, NINV/INV (3-State)
Product Specification

FAST Products

FEATURES

- **High speed parallel registers with positive edge-triggered D-type flip-flops**
- **High performance bus interface buffering for wide data/address paths or busses carrying parity**
- **High impedance PNP base inputs for reduced loading (20μA in High and Low states)**
- **I_{IL} is 20μA vs 1000μA for AM29821 series**
- **Buffered control inputs to reduce AC effects**
- **Ideal where high speed, light loading, or increased fan-in as required with MOS microprocessors**
- **Positive and negative over-shoots are clamped to ground**
- **3-state outputs glitch free during power-up and power-down**
- **Slim Dip 300 mil package**
- **Broadside pinout compatible with AMD AM 29821-29826 series**
- **Outputs sink 64mA and source 24mA**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F821, 74F822	180MHz	75mA
74F823, 74F824	180MHz	70mA
74F825, 74F826	180MHz	65mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic SLIM DIP (300mil)	N74F821N, N74F822N, N74F823N, N74F824N, N74F825N, N74F826N
24-Pin Plastic SOL	N74F821D, N74F822D, N74F823D, N74F824D, N74F825D, N74F826D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F821 'F822	D_n	Data inputs	1.0/0.033	20μA/20μA
	CP	Clock input	1.0/0.033	20μA/20μA
	$\overline{OE}$	Output enable input (activeLow)	1.0/0.033	20μA/20μA
	Q_n, $\overline{Q}_n$	Data output	1200/106.7	24mA/64mA
'F823 'F824	D_n	Data inputs	1.0/0.033	20μA/20μA
	CP	Clock input	1.0/0.033	20μA/20μA
	$\overline{CE}$	Clock enable input (active Low)	1.0/0.033	20μA/20μA
	$\overline{MR}$	Master reset input (active Low)	1.0/0.033	20μA/20μA
	$\overline{OE}$	Output enable input (active Low)	1.0/0.033	20μA/20μA
	Q_n, Q_n	Data outputs	1200/106.7	24mA/64mA
'F825 'F826	D_n	Data inputs	1.0/0.033	20μA/20μA
	CP	Clock input	1.0/0.033	20μA/20μA
	$\overline{CE}$	Clock enable input (active Low)	1.0/0.033	20μA/20μA
	$\overline{MR}$	Master reset input (active Low)	1.0/0.033	20μA/20μA
	$\overline{OE}_n$	Output enable inputs (active Low)	1.0/0.033	20μA/20μA
	Q_n, $\overline{Q}_n$	Data outputs	1200/106.7	24mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 74F821 series Bus Interface Registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of busses carrying parity.

The 'F821/'F822 are buffered 10-bit wide versions of the popular 'F374/'F534 functions.
The 'F822 is the inverted output version of 'F821.

The74F823 and 74F824 are 9-bit wide buffered registers with Clock Enable($\overline{CE}$) and Master Reset ($\overline{MR}$) which are ideal for parity bus interfacing in high microprogrammed systems.
The 'F 824 is the inverted output version of 'F823.

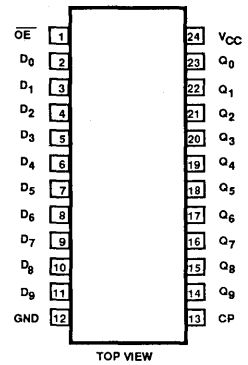
The74F825 and 74F826 are 8-bit buffered registers with all the 'F823/'F824 controls plus Output Enable ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring High I_{OL}/I_{OH}.
The 'F826 is the inverted output version of 'F825.

Bus Interface Registers

FAST 74F821/822/823/824/825/826

PIN CONFIGURATION

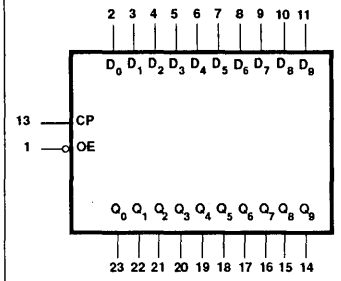
'F821



TOP VIEW

LOGIC SYMBOL

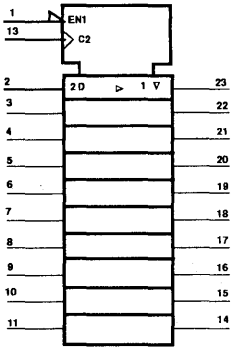
'F821



V_{CC} = Pin 24
GND = Pin 12

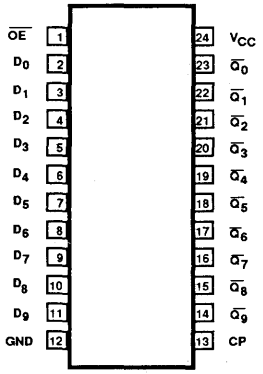
LOGIC SYMBOL(IEEE/IEC)

'F821



PIN CONFIGURATION

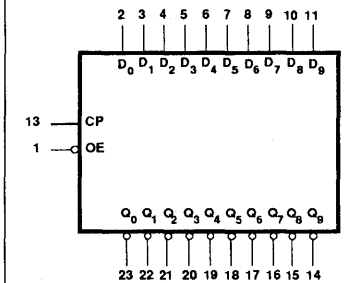
'F822



TOP VIEW

LOGIC SYMBOL

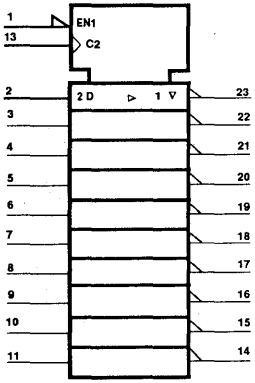
'F822



V_{CC} = Pin 24
GND = Pin 12

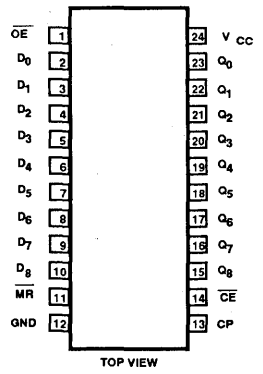
LOGIC SYMBOL(IEEE/IEC)

'F822



PIN CONFIGURATION

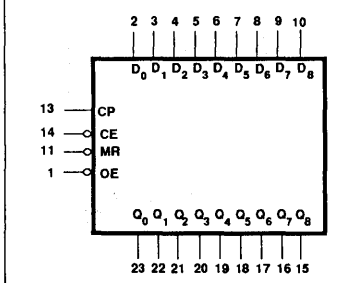
'F823



TOP VIEW

LOGIC SYMBOL

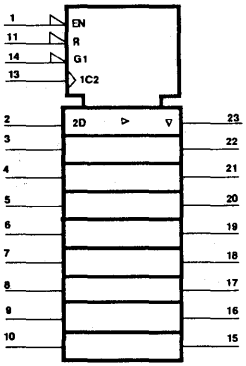
'F823



V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

'F823

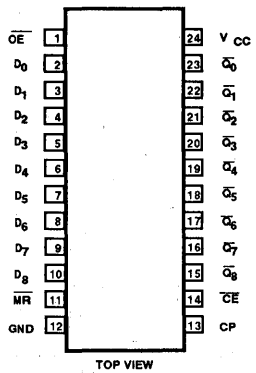


Bus Interface Registers

FAST 74F821/822/823/824/825/826

PIN CONFIGURATION

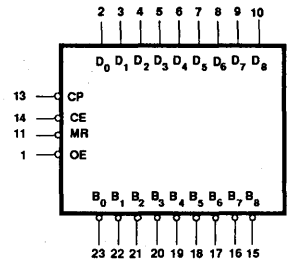
'F824



TOP VIEW

LOGIC SYMBOL

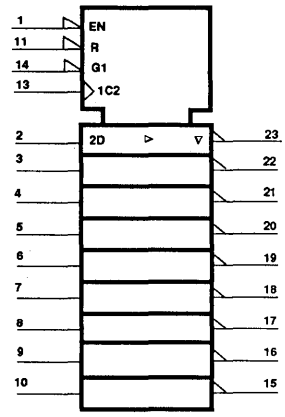
'F824



V_{CC} = Pin 24
GND = Pin 12

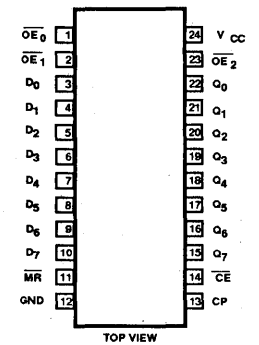
LOGIC SYMBOL(IEEE/IEC)

'F824



PIN CONFIGURATION

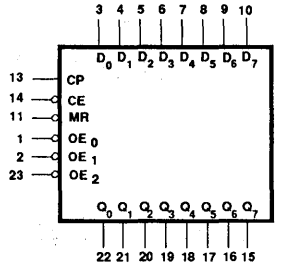
'F825



TOP VIEW

LOGIC SYMBOL

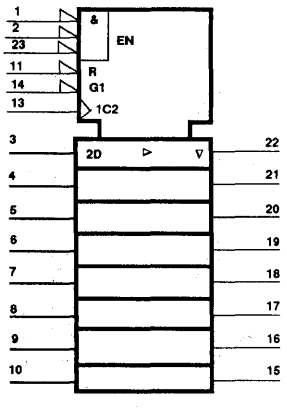
'F825



V_{CC} = Pin 24
GND = Pin 12

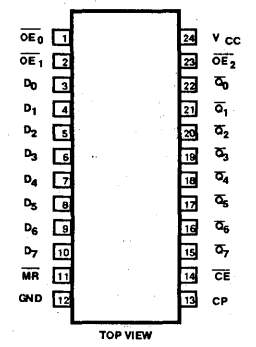
LOGIC SYMBOL(IEEE/IEC)

'F825



PIN CONFIGURATION

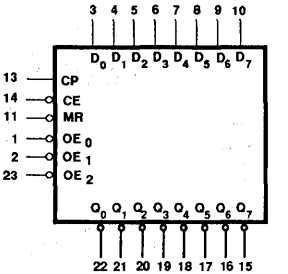
'F826



TOP VIEW

LOGIC SYMBOL

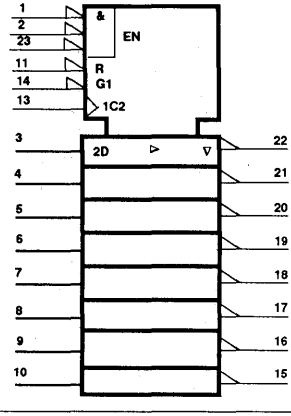
'F826



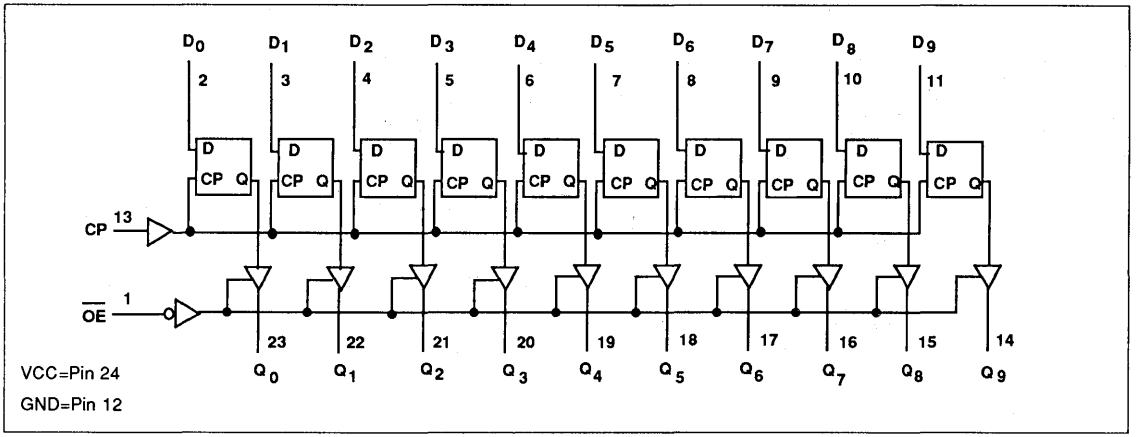
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

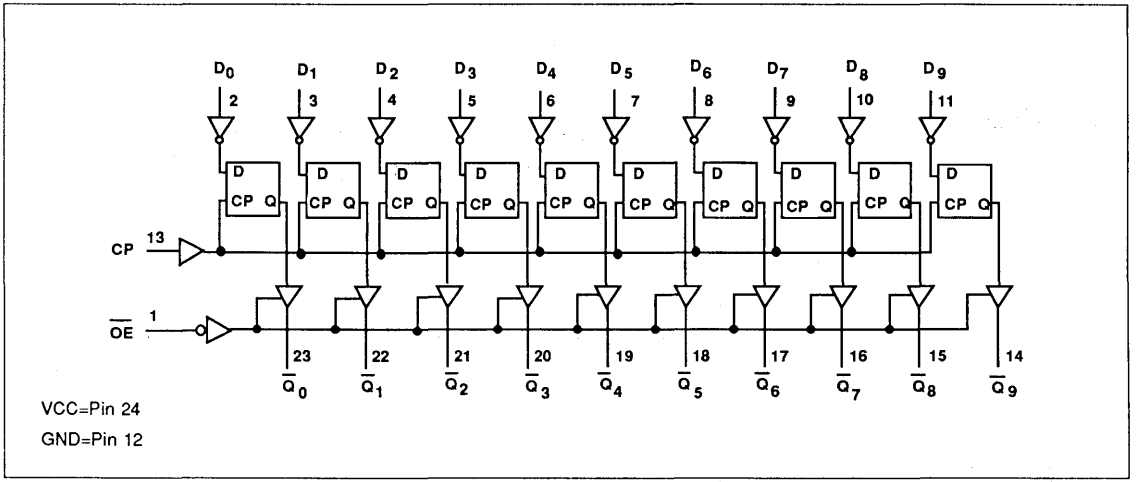
'F826



LOGIC DIAGRAM for 'F821



LOGIC DIAGRAM for 'F822

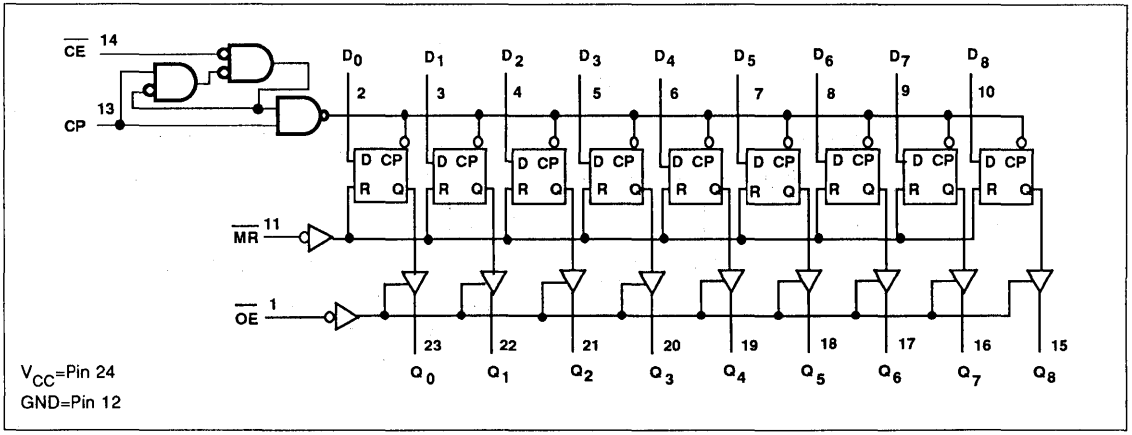


FUNCTION TABLE for 'F821 and 'F822

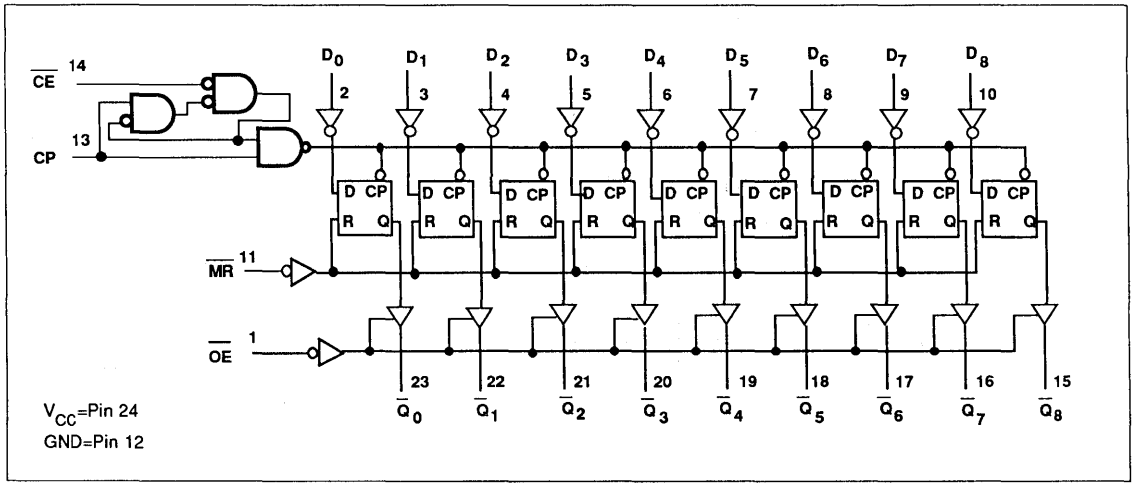
INPUTS			OUTPUTS		OPERATING MODE
			'F821	'F822	
$\overline{OE}$	CP	D_n	Q	$\overline{Q}$	
L	↑	l	L	H	Load and read data
L	↑	h	H	L	
L	↕	X	NC	NC	Hold
H	X	X	Z	Z	High impedance

H = High voltage level
L = Low voltage level
h = High state must be present one setup time before the Low-to-High clock transition
l =Low state must be present one setup time before the Low-to -High clock transition
↑ =Low-to-High clock transition
↕ = Not a Low-to-High clock transition
X =Don't care
NC =No change
Z =High impedance "off" state

LOGIC DIAGRAM for 'F823



LOGIC DIAGRAM for 'F824

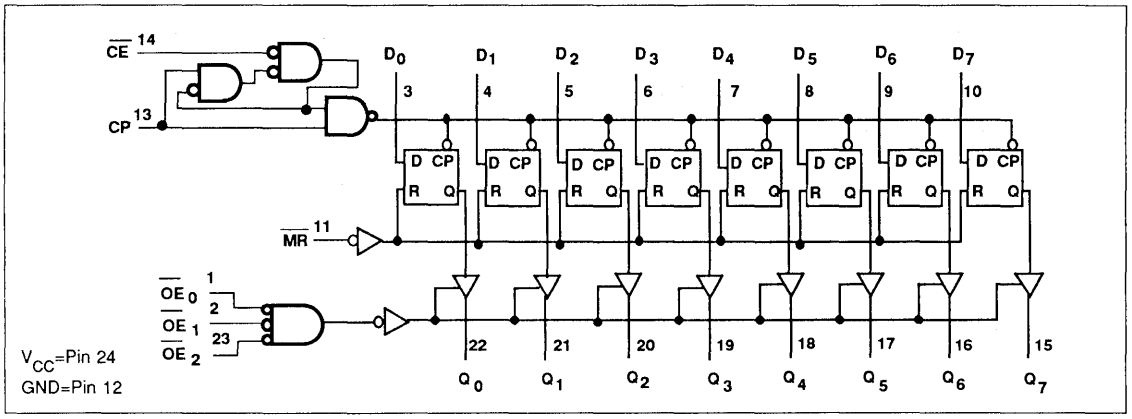


FUNCTION TABLE for 'F823 and 'F824

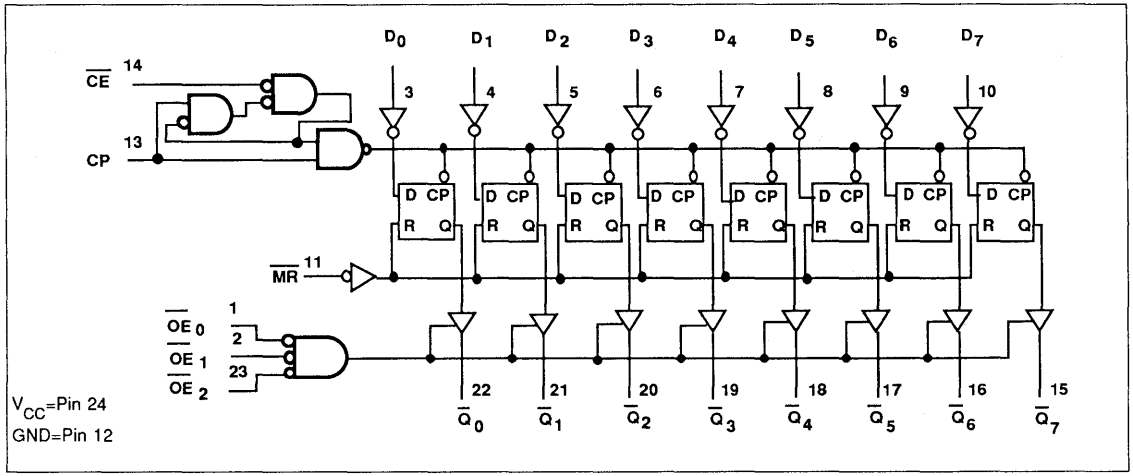
INPUTS					OUTPUTS		OPERATING MODE
					'F823	'F824	
$\overline{OE}$	$\overline{MR}$	$\overline{CE}$	CP	D_n	Q	$\overline{Q}$	
L	L	X	X	X	L	L	Clear
L	H	L	↑	h	H	L	Load and read data
L	H	L	↑	l	L	H	
L	H	H	↕	X	NC	NC	Hold
H	X	X	X	X	Z	Z	High impedance

H = High voltage level
L = Low voltage level
h = High state must be present one setup time before the Low-to-High clock transition
l =Low state must be present one setup time before the Low-to -High clock transition
↑ =Low-to-High clock transition
↕ =Not a Low-to-High clock transition
X =Don't care
NC =No change
Z =High impedance "off" state

LOGIC DIAGRAM for 'F825



LOGIC DIAGRAM for 'F826



FUNCTION TABLE for 'F825 and 'F826

INPUTS					OUTPUTS		OPERATING MODE
					'F825	'F826	
$\overline{OE}_n$	$\overline{MR}$	$\overline{CE}$	CP	D_n	Q	$\overline{Q}$	
L	L	X	X	X	L	L	Clear
L	H	L	↑	h	H	L	Load and read data
L	H	L	↑	l	L	H	
L	H	H	↕	X	NC	NC	Hold
H	X	X	X	X	Z	Z	High impedance

H = High voltage level
L = Low voltage level
h = High state must be present one setup time before the Low-to-High clock transition
l = Low state must be present one setup time before the Low-to -High clock transition
↑ = Low-to-High clock transition
↕ = Not a Low-to-High clock transition
X = Don't care
NC = No change
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-24	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} =-15mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.4			V
					I_{OH} =-24mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=64mA	±10%V_{CC}			0.55	V
						±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OZH}	Off-state output current, HIgh voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low voltage applied			V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F821 'F822	I_{CCH}	V_{CC} = MAX				75	105	mA
			I_{CCL}					75	105	mA
			I_{CCZ}					75	115	mA
		'F823 'F824	I_{CCH}	V_{CC} = MAX				65	100	mA
			I_{CCL}					70	105	mA
			I_{CCZ}					75	110	mA
		'F825 'F826	I_{CCH}	V_{CC} = MAX				60	85	mA
			I_{CCL}					60	90	mA
			I_{CCZ}					65	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

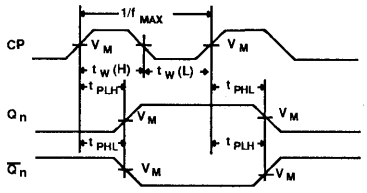
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	150	180		140		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	'F821 'F823 'F825 'F826	Waveform 1	4.0 4.0	6.5 6.0	8.5 8.5	4.0 3.5	9.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$	'F822 'F824	Waveform 1	4.5 4.5	6.5 6.5	9.0 9.0	4.5 4.5	10.0 9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n or $\overline{Q}_n$	'F823 'F824 'F825 'F826	Waveform 2	3.0	5.0	8.0	3.0	8.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_n$ to Q_n or $\overline{Q}_n$		Waveform 4 Waveform 5	5.0 3.0	7.0 5.0	10.0 8.0	4.0 2.5	11.5 9.0	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}_n$ to Q_n or $\overline{Q}_n$		Waveform 4 Waveform 5	1.5 1.5	3.5 3.5	6.5 6.5	1.5 1.5	7.5 7.5	ns

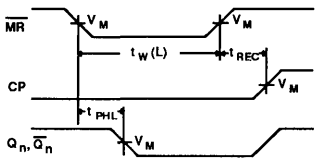
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	'F821 'F822	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	'F823 'F824 'F825 'F826	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP		Waveform 3	2.0 2.0			2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1	3.5 3.5			4.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CE}$ to CP	'F823 'F824 'F825 'F826	Waveform 3	0.0 2.0			0.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP		Waveform 3	0.0 2.5			0.0 3.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low		Waveform 2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP		Waveform 2	2.5			2.5		ns

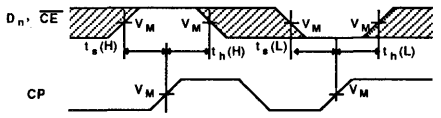
AC WAVEFORMS



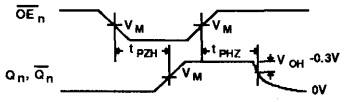
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



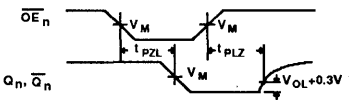
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 3. Data Setup And Hold Times



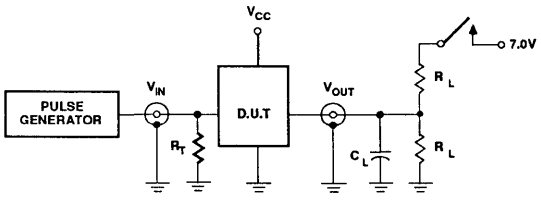
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



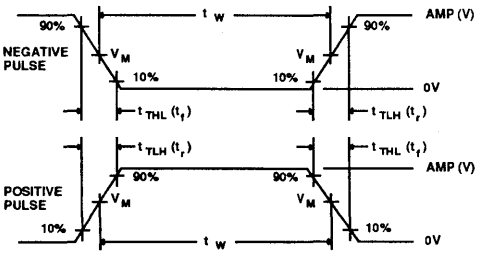
Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F827, 74F828
Buffers

74F827 10-Bit Buffer/Line Driver, Non-Inverting (3-State)
74F828 10-Bit Buffer/Line Driver, Inverting (3-State)
Product Specification

FAST Products

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **I_{IL} is 20μA vs FAST family spec of 600 A and 1000 A for AMD 29827/29828 series**
- **Ideal where high speed, light bus loading and increased fan-in are required**
- **Controlled rise and fall times to minimize ground bounce**
- **Glitch free power up in 3-state**
- **Flow through pinout architecture for microprocessor oriented applications**
- **Outputs sink 64mA**
- **Slim 300 mil-wide plastic 24-pin package**
- **Pinout and function compatible with AMD 29827/29828 series**

DESCRIPTION

The 74F827 and 74F828 10-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($\overline{OE}_0$, $\overline{OE}_1$) for maximum control flexibility.

The 'F827 and 'F828 are functionally and pin compatible to AMD AM29827 and AM 29828.

The 'F828 is an inverting version of 'F827.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F827	6.0ns	60mA
74F828	6.0ns	55mA

ORDERING INFORMATION

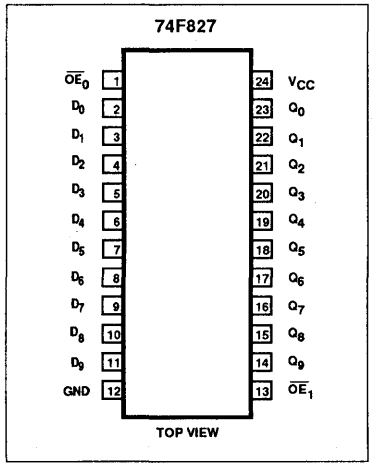
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic DIP (300 mil)	N74F827N, N74F828N
24-Pin Plastic SOL	N74F827D, N74F828D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

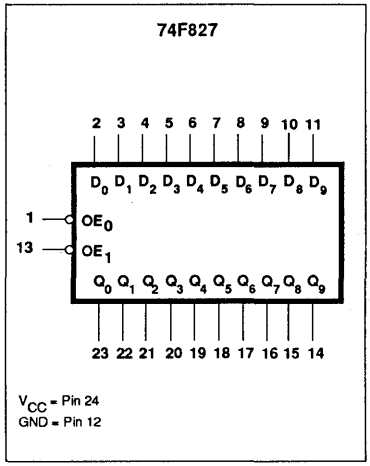
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0- D_9	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_0$ $\overline{OE}_1$	Output enable inputs (active Low)	1.0/0.033	20μA/20μA
Q_0- Q_9	Data outputs ('F827)	1200/106.7	24mA/64mA
$\overline{Q}_0$- $\overline{Q}_9$	Data outputs ('F828)	1200/106.7	24mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

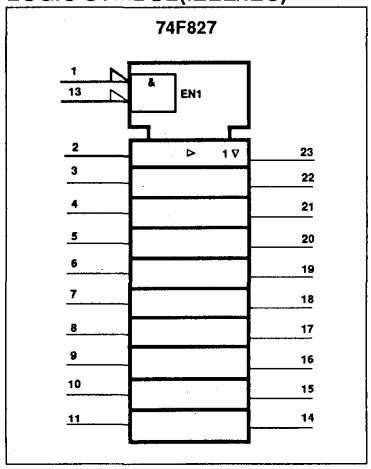
PIN CONFIGURATION



LOGIC SYMBOL

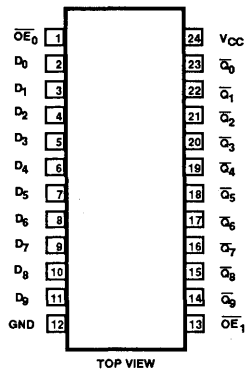


LOGIC SYMBOL(IEEE/IEC)



PIN CONFIGURATION

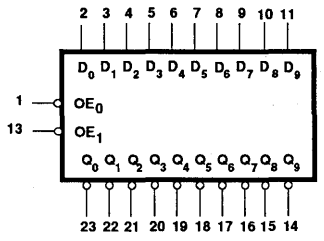
74F828



TOP VIEW

LOGIC SYMBOL

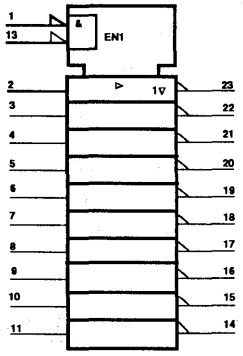
74F828



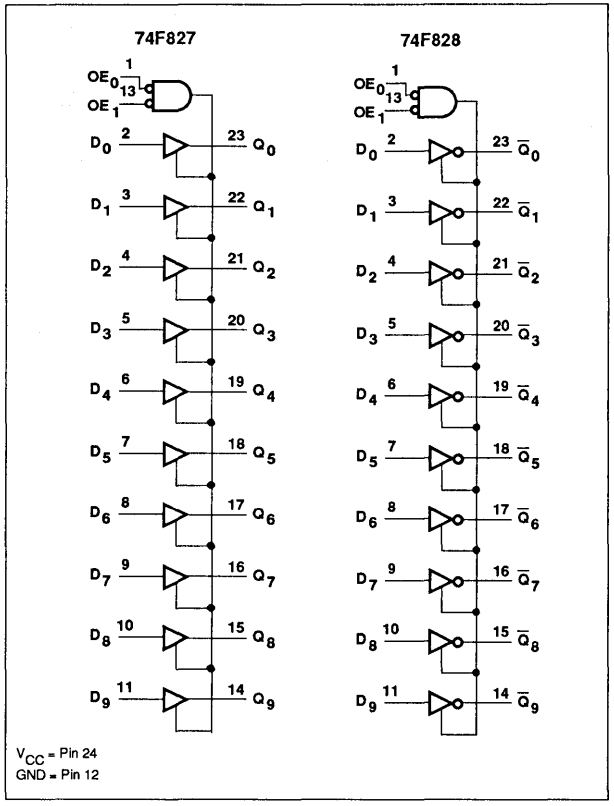
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

74F828



LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12

FUNCTION TABLE

INPUTS		OUTPUTS		OPERATING MODE
		'F827	'F828	
$\overline{OE}_n$	D_n	Q_n	$\overline{Q}_n$	
L	L	L	H	Transparent
L	H	H	L	Transparent
H	X	Z	Z	High impedance

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-24	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -15mA	±10%V_{CC}	2.4			V
						±5%V_{CC}	2.4	3.3		V
					I_{OH} = -24mA	±10%V_{CC}	2.0			V
						±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}			0.55	V
						±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OZH}	Off-state output current, HIgh voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low voltage applied			V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F827	I_{CCH}	V_{CC} = MAX				50	70	mA
			I_{CCL}					70	100	mA
			I_{CCZ}					60	90	mA
		'F828	I_{CCH}	V_{CC} = MAX				30	45	mA
			I_{CCL}					65	85	mA
			I_{CCZ}					55	70	mA

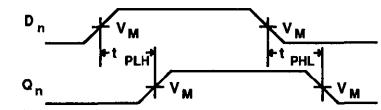
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

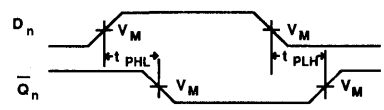
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	74F827	Waveform 1	2.0 2.0	5.5 4.5	8.5 8.5	2.0 2.0	9.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4	5.0 4.0	10.0 7.0	13.5 12.0	4.5 4.0	15.5 13.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_n$ to Q_n		Waveform 3 Waveform 4	2.5 2.5	5.0 5.0	8.0 8.0	2.0 2.0	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	74F828	Waveform 2	2.0 1.0	6.0 3.0	8.5 7.0	2.0 1.0	9.5 8.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4	7.5 6.5	10.0 8.5	13.0 12.0	7.0 6.0	15.0 13.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_n$ to $\overline{Q}_n$		Waveform 3 Waveform 4	2.5 1.5	5.0 4.0	8.5 7.0	2.0 1.5	9.0 8.0	ns

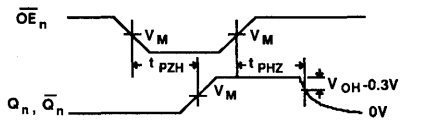
AC WAVEFORMS



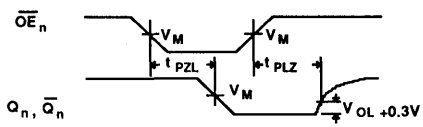
Waveform 1. Propagation Delay For Non-Inverting Output



Waveform 2. Propagation Delay For Inverting Output



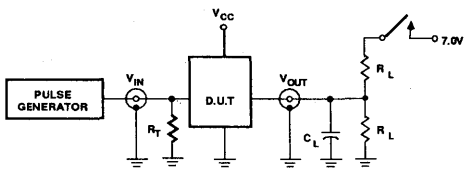
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

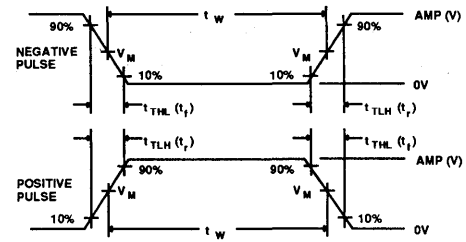
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F832, 74F1832
OR Drivers

FAST Products

74F832-Hex Two-Input OR Driver
74F1832-Hex Two-Input OR Driver
Preliminary Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F832	2.5ns	11mA
74F1832	2.5ns	11mA

FEATURES
- High capacitive drive capability
- Choice of configuration
  Corner V_{CC} and GND-- 'F832
  Center V_{CC} and GND-- 'F1832
- Typical propagation delay of 2.5ns

ORDERING INFORMATION

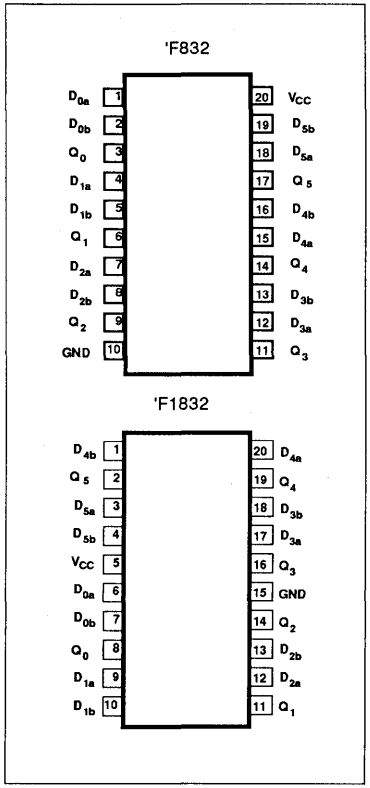
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F832N, N74F1832N
20-Pin Plastic SOL	N74F832D, N74F1832D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

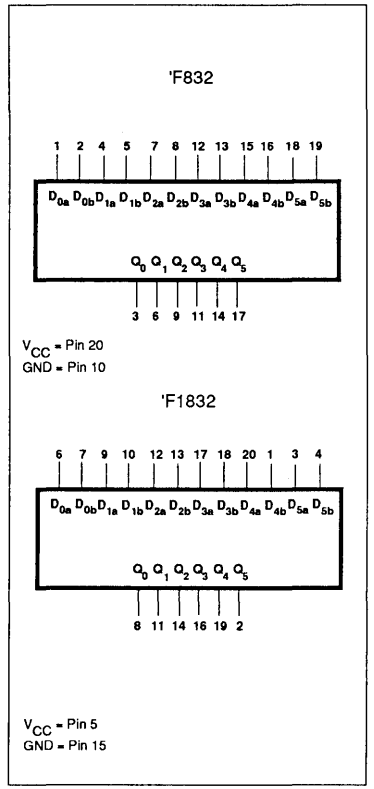
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na} - D_{nb}	Data inputs	1.0/0.033	20µA/20µA
Q_0 - Q_5	Data outputs	2400/80	48mA/48mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

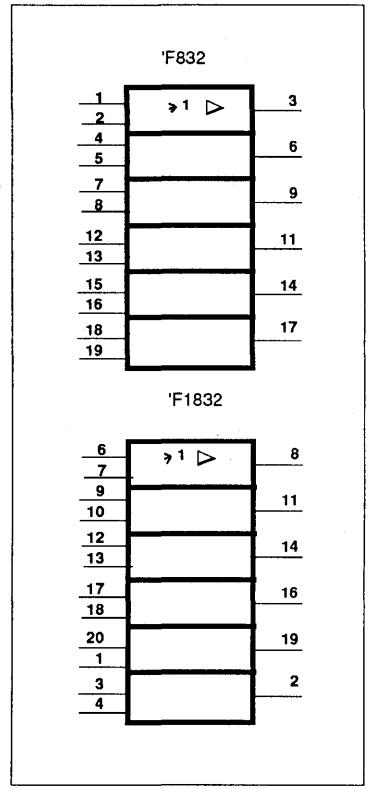
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



FUNCTION TABLE

INPUTS		OUTPUT
D_{na}	D_{nb}	Q_n
H	X	H
X	H	H
L	L	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	96	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-48	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

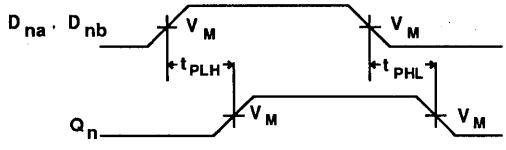
SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.0			V
			±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.38	0.55	V
			±5%V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input clamp current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-20	µA
I_O	Output current[3]	V_{CC} = MAX, V_O=2.25V		-60		-160	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX	V_{IN} =GND		9	15	mA
	Supply current (total) I_{CCL}	V_{CC} = MAX	V_{IN} =4.5V		22	36	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to Q_n	Waveform 1	1.0 1.0	2.5 2.4	4.5 4.5	1.0 1.0	5.5 5.5	ns

AC WAVEFORMS

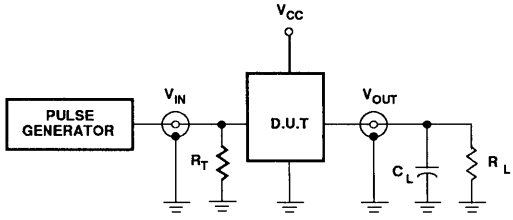


Waveform 1.

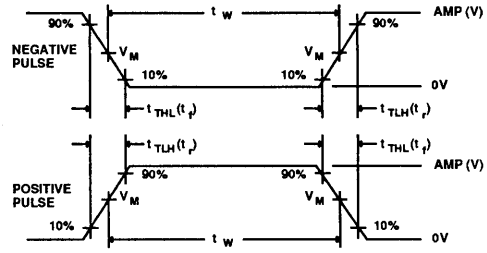
Propagation Delay for Input to Output

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F835
Shift Register

8-Bit Shift Register with 2:1 Mux-in, Latched "B" inputs, and Serial Out

FAST Products

Product Specification

FEATURES
- **Combines the 'F373, two 'F157s, and the 'F166 functions in one package**
- **Interleaved loading with 2:1 mux**
- **Dual 8-bit Parallel inputs**
- **Transparent Latch on all "B" inputs**
- **Guaranteed Serial Shift Frequency to 60MHz**
- **Expandable to 16-bits or more with serial input**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F835	85MHz	45mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300 mil)	N74F835N
24-Pin Plastic SOL	N74F835D

DESCRIPTION

The 74F835 is a high speed 8-bit parallel/serial-in, serial-out shift register whose parallel inputs have been connected to an internal octal two-to-one multiplexer with all the 'B' inputs connected to an octal latch.

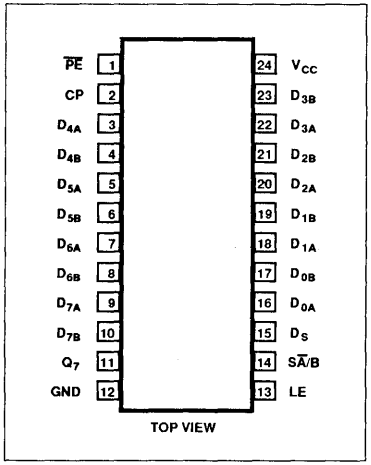
It is useful in any design where a 2:1 mux input with a transparent latch is needed.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

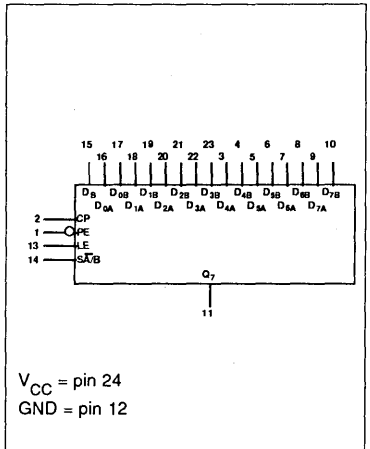
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{0A} - D_{7A}	Parallel data inputs	1.0/1.0	20µA/0.6mA
D_{0B} - D_{7B}	Latched Parallel data inputs	1.0/1.0	20µA/0.6mA
D_S	Serial data input	1.0/1.0	20µA/0.6mA
CP	Shift Register Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{SA}$/B	Mux Select	1.0/1.0	20µA/0.6mA
LE	Latch Enable input (for B inputs)	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input	1.0/1.0	20µA/0.6mA
Q_7	Output	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

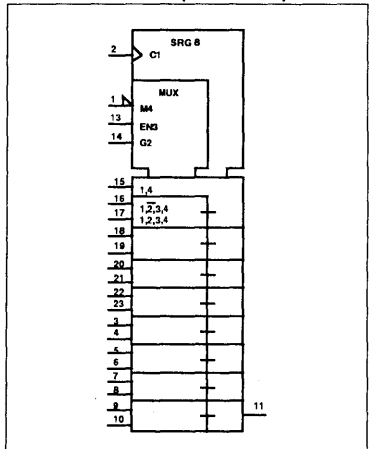
PIN CONFIGURATION



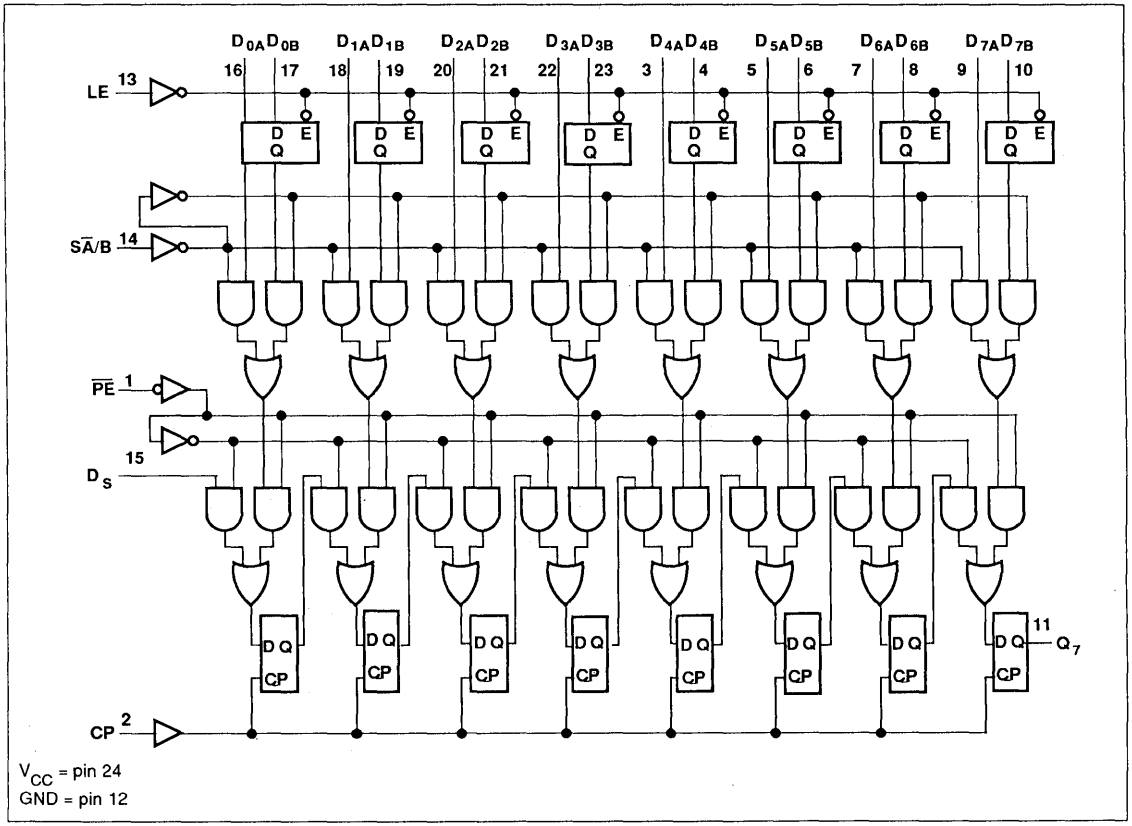
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM

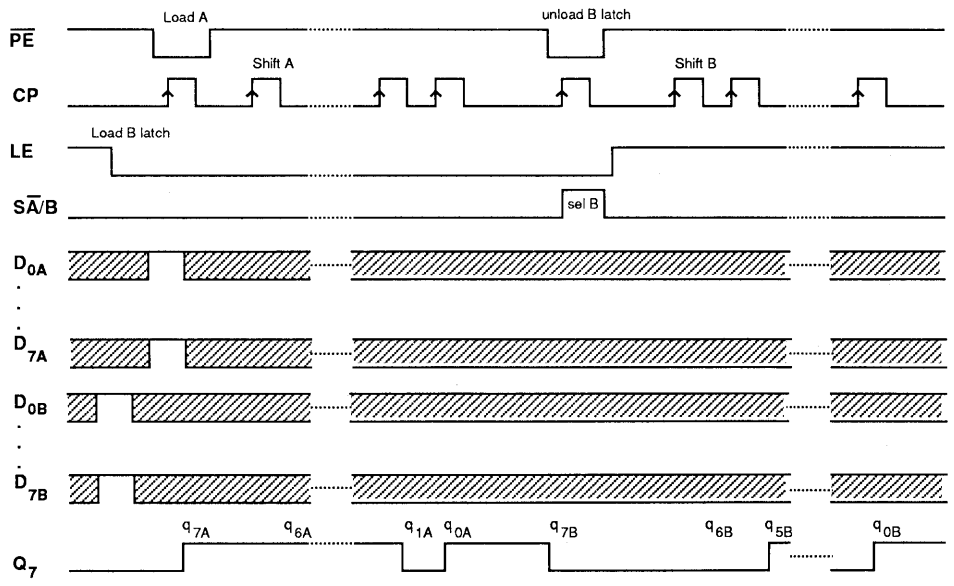


FUNCTION TABLE

OPERATING MODE	INPUTS							INTERNAL			OUTPUT
								B Latch	Serial Reg		
	$\overline{PE}$	CP	LE	$S\overline{A}/B$	D_{nA}	D_{nB}	D_S		Q_8	Q_{1-6}	Q_7
Parallel load A data	L	↑	X	L	h	X	X	X	H	H	H
					l	X	X	X	L	L	L
Latch B data	X	X	L	X	X	h	X	H	X	X	X
					X	l	X	L	X	X	X
Parallel load B data (from Latch)	L	↑	L	H	X	X	X	h	H	H	H
					X	X	X	l	L	L	L
Parallel load B data (Transparent Mode)	L	↑	H	H	X	h	X	h	H	H	H
					X	l	X	l	L	L	L
Serial Shift	H	↑	X	X	X	X	h	X	H	q_{n-1}	q_6
					X	X	l	X	L	q_{n-1}	q_6

H = High voltage level
L = Low voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
q_n = Lower case letters indicate the state of the referenced flop cell one cycle prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

TYPICAL TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		.30	.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		.30	.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			45	65	mA
		I_{CCL}				45	65	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

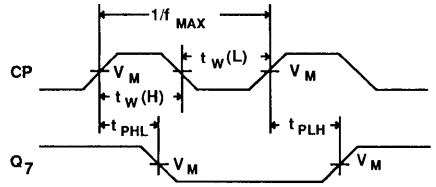
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS: T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			LIMITS: T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		UNIT
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	70	85		60		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_7 (Load)	Waveform 1	7.0 7.0	9.0 9.0	11.5 11.5	6.5 6.5	12.5 12.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_7 (Shift)	Waveform 1	7.0 7.0	9.0 9.0	11.5 11.5	6.5 6.5	12.5 12.5	ns

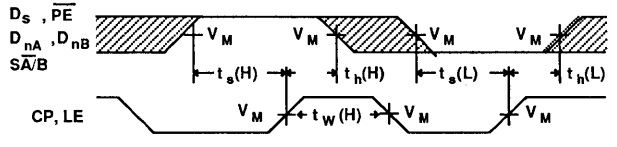
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time D_{nA} or D_{nB} to CP	Waveform 2	2.0 2.0			2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold time D_{nA} or D_{nB} to CP	Waveform 2	2.5 2.5			3.0 3.0		ns
$t_s(H)$ $t_s(L)$	Setup time D_S to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_S to CP	Waveform 2	3.5 3.5			4.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{PE}$ to CP	Waveform 2	4.5 4.5			5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time $\overline{PE}$ to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_s(H)$ $t_s(L)$	Setup time D_{nB} to LE	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_h(H)$ $t_h(L)$	Hold time D_{nB} to LE	Waveform 2	3.0 3.0			3.5 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time $S\overline{A}/B$ to CP	Waveform 2	3.5 3.5			4.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold time $S\overline{A}/B$ to CP	Waveform 2	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	Clock pulse width, High or Low	Waveform 1	6.0 5.0			6.5 5.0		ns
$t_w(H)$	Latch Enable pulse width, High	Waveform 2	4.5			5.0		ns

AC WAVEFORMS



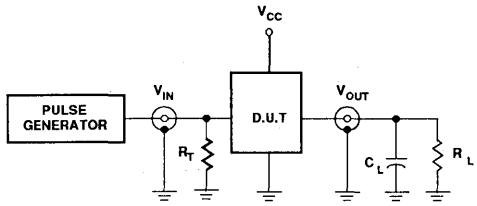
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



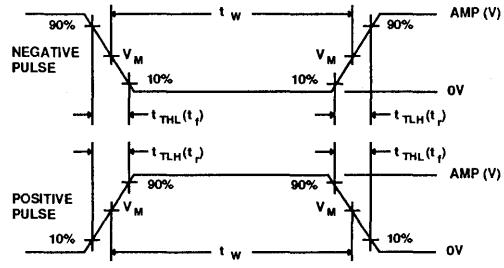
Waveform 2. Data and Select Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST Products

FAST 74F838

Microprogram Sequence Controller

Preliminary Specification

FEATURES

- **5-bit address generator (32 micro-instruction addressability)**
- **Two subroutine branching capability**
- **Interrupt branching**
- **Cascadable for increased addressing**
- **Direct branching over full address range**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F838	90MHz	mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F838N
20-Pin SOL	N74F838D

DESCRIPTION

The 74F838 Microprogram Sequence Controller generates addresses to access instructions from a microprogram memory.

This high speed device provides an efficient means of controlling the flow through a microprgram by providing a powerful set of sequencing functions.

In addition to providing branching facility over the entire address range, the device also supports two subroutines and an interrupt level.

The 74F838 can directly address up to 32 micro-instructions: two or more of these devices may be cascaded for increased addressing. For example, two devices can address 1K and three devices can address up to 32K of program storage.

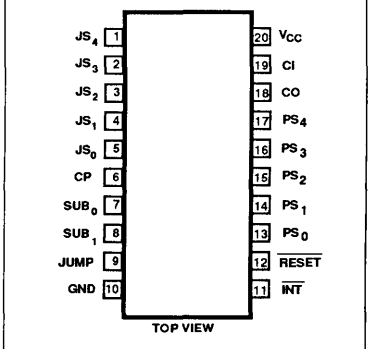
Combined with memory, the 74F838 form a powerful control section for CPUs and I/O controllers.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

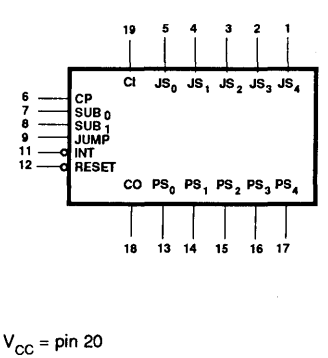
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
JS_0 - JS_4	Jump state inputs	1.0/1.0	20µA/0.6mA
JMP	Jump input	1.0/1.0	20µA/0.6mA
SUB_0, SUB_1	Subroutine inputs	1.0/1.0	20µA/0.6mA
$\overline{INT}$	Interrupt input	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20µA/0.6mA
CI	Cascade In input	1.0/1.0	20µA/0.6mA
$\overline{RESET}$	Reset input	1.0/1.0	20µA/0.6mA
PS_0 - PS_4	Present state outputs	150/40	3.0mA/24mA
CO	Cascade Out output	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

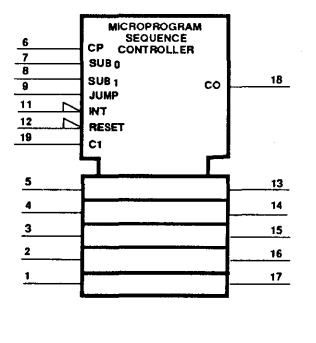
PIN CONFIGURATION



LOGIC SYMBOL



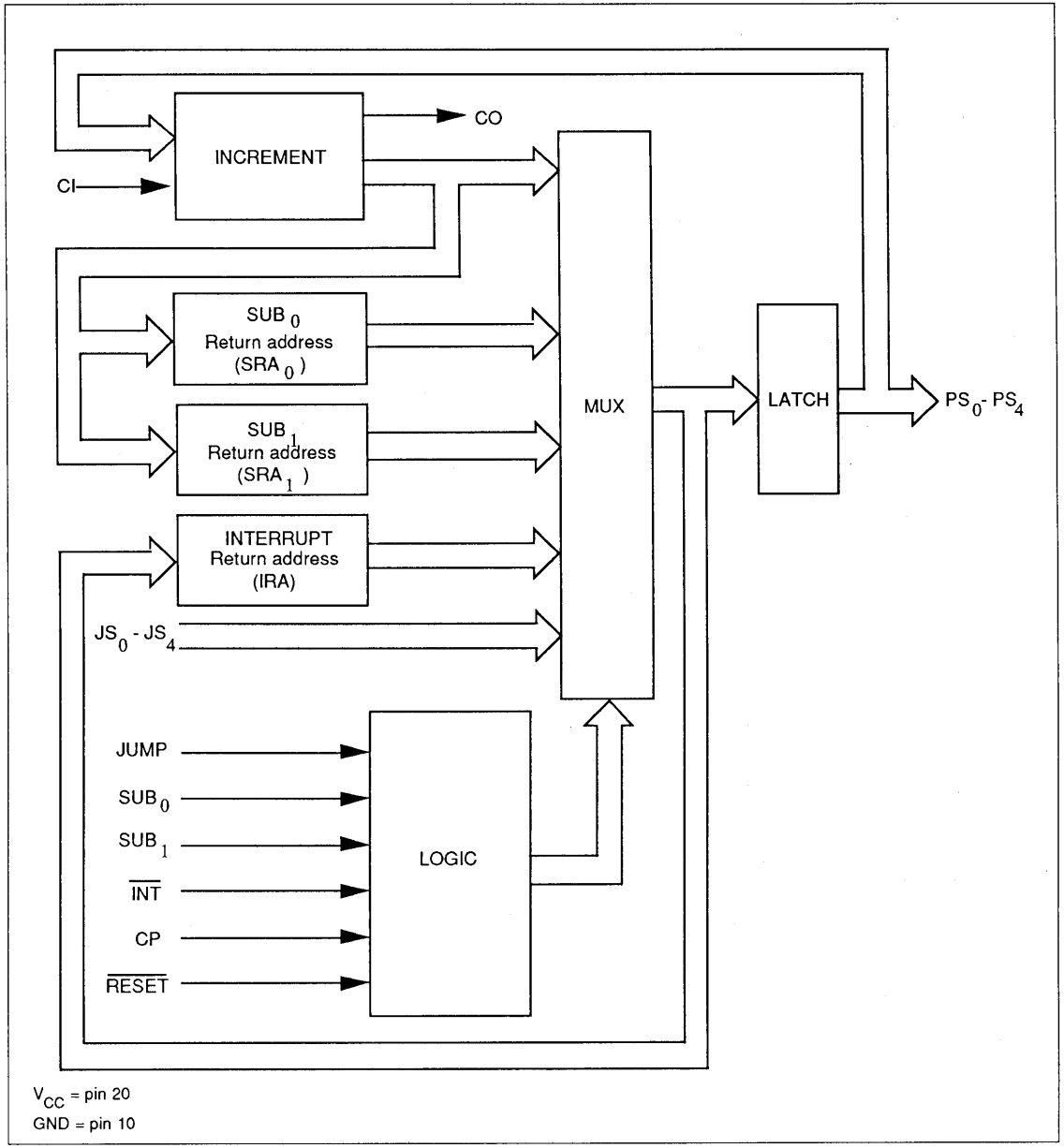
LOGIC SYMBOL(IEEE/IEC)



PIN DESCRIPTION

PIN NO.	SYMBOL	TYPE	FUNCTION	DESCRIPTION
5 4 3 2 1	JS_0 JS_1 JS_2 JS_3 JS_4	Input	Jump State	Address on these inputs is transferred to the PS_0-PS_4 outputs if the JMP input is High or the SUB_0 or SUB_1 inputs change from Low-to-High. These inputs are ignored if neither of the above conditions is true.
7 8	SUB_0 SUB_1	Input	Subroutine	On a Low-to-High transition, the Present State address (PS_0-PS_4) plus one is saved internally as a return address, and address on pins JS_0-JS_4 will be transferred to the PS_0-PS_4 outputs. On a High-to-Low transition, the saved return address state will be enabled onto the PS_0-PS_4 outputs.
9	JMP	Input	Jump	When JMP is High, the next state address will be JS_0-JS_4.
11	$\overline{INT}$	Input	Interrupt	On a High-to-Low transition, the next address to appear on the PS_0-PS_4 output is saved internally as a return address and PS_0-PS_4 are forced to all ones. If this feature is used, a micromode jump would normally be stored at state address 11111. SUB_0 or SUB_1 inputs are ignored when $\overline{INT}$ is Low. On a Low-to-High transition, the saved return address state is enabled onto the PS_0-PS_4 outputs.
6	CP	Input	Clock	This clock determines the sequence rate of the controller.
12	$\overline{RESET}$	Input	Reset	When Low, all internal registers and PS_0-PS_4 are set to zeros.
19	CI	Input	Cascade In	This input should be tied to V_{CC} for the least significant device. For all other devices, CI is connected to CO of the previous device.
18	CO	Output	Cascade Out	This signal is connected to CI of the next device. One device permits 32 states: two devices allow 1024 states; three devices allow 32,768 states.
13 14 15 16 17	PS_0 PS_1 PS_2 PS_3 PS_4	Output	Present state	The address of the present state.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS				OPERATING MODE
								INTERNAL REGISTERS			
$\overline{RESET}$	$\overline{INT}$	JUMP	SUB_0	SUB_1	CP	JS_n	PS_0-PS_4	SRA_0	SRA_1	IRA	
L	X	X	X	X	X	X	00000	0	0	0	Reset
H	H	L	H or L	H or L	↑	X	PS_{n+1}				Increment
H	L	L	X	X	↑	X	PS_{n+1}				
H	L	H	X	X	↑	JS_n	JS_n				Jump
H	H	H	↓	↓	↑	JS_n	JS_n				
H	H	X	↑	H or L	↑	JS_n	JS_n	PS_{n+1}			Subroutine Call
H	H	X	H or L	↑	↑	JS_n	JS_n		PS_{n+1}		
H	H	X	↑	↑	↑	JS_n	JS_n	PS_{n+1}	PS_{n+1}		
H	H	L	↓	H or L	↑	X	SRA_0				Return from Subroutine
H	H	L	H or L	↓	↑	X	SRA_1				
H	↓	L	H or L	H or L	↑	X	11111			PS_{n+1}	Interrupt Call
H	↓	H	H or L	H or L	↑	JS_n	11111			JS_n	
H	↓	X	↑	H or L	↑	JS_n	11111	PS_{n+1}		JS_n	
H	↓	X	H or L	↑	↑	JS_n	11111		PS_{n+1}	JS_n	
H	↓	X	↑	↑	↑	JS_n	11111	PS_{n+1}	PS_{n+1}	JS_n	
H	↓	L	↓	H or L	↑	X	11111			SRA_0	
H	↓	L	H or L	↓	↑	X	11111			SRA_1	Return from Interrupt
H	↑	X	X	X	↑	X	IRA				Illegal
H	H	H	↓	H or L	↑	JS_n	$JS_n + SRA_0$				
H	H	H	H or L	↓	↑	JS_n	$JS_n + SRA_1$				
H	H	L	↓	↓	↑	X	$SRA_0 + SRA_1$				
H	H	H	↓	↓	↑	JS_n	$JS_n + SRA_0 + SRA_1$				
H	↓	H	↓	H or L	↑	JS_n	11111			$JS_n + SRA_0$	
H	↓	H	H or L	↓	↑	JS_n	11111			$JS_n + SRA_1$	
H	↓	L	↓	↓	↑	X	11111			$SRA_0 + SRA_1$	
H	↓	H	↓	↓	↑	JS_n	11111			$JS_n + SRA_0 + SRA_1$	

H = High voltage level.
L = Low voltage level.
X = Don't care.

↓ = High-to-Low clock transition.

⇣ = Antything except a High-to-Low clock transition.

↑ = Low-to-High clock transition.

H or L = Either High or Low

0 =Low output

1 = High output

To avoid timing problems $\overline{INT}$ is sampled on the falling edge of the clock and serviced on the next rising edge.

APPLICATION

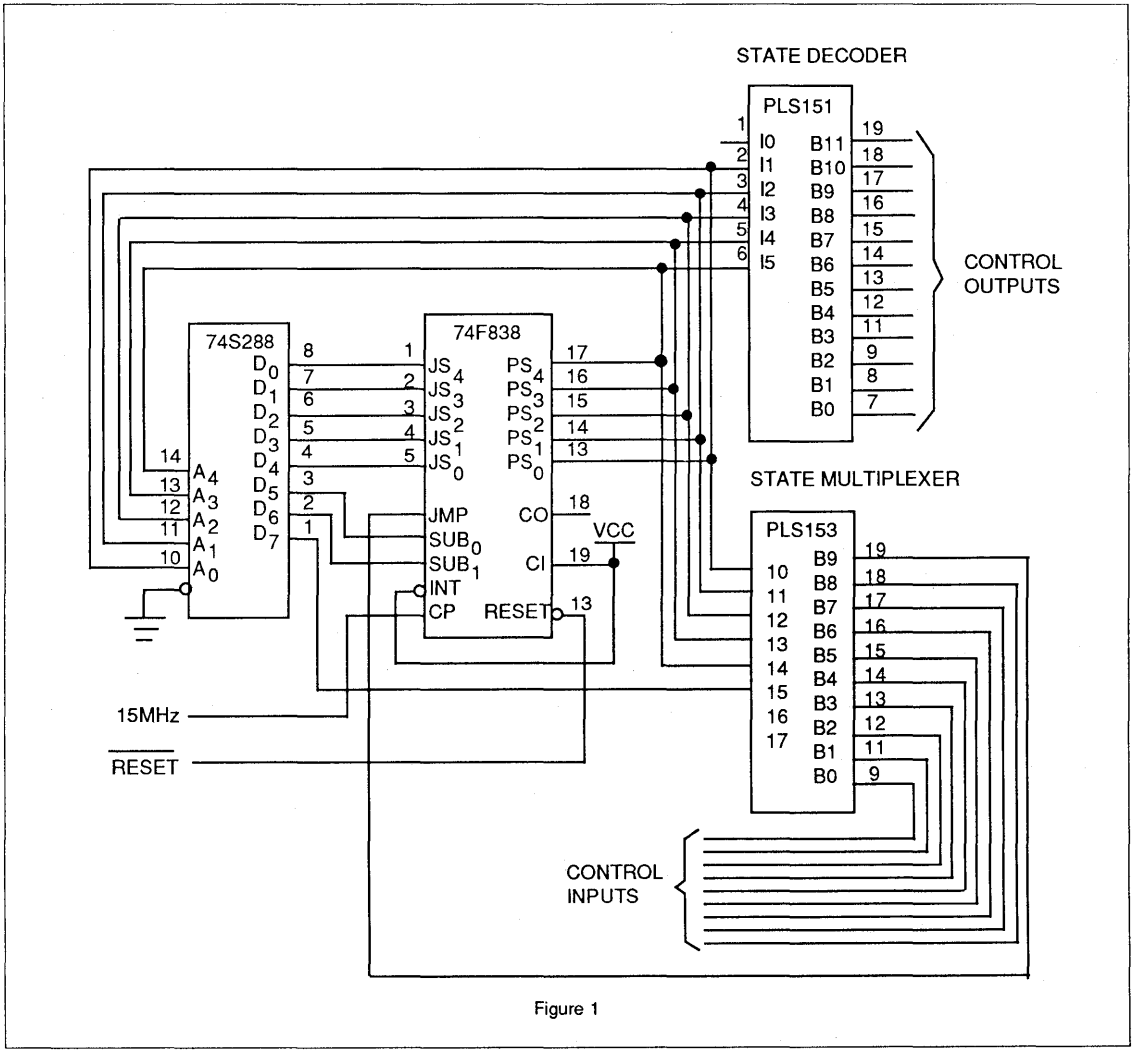


Figure 1

As shown in Figure 1, a PROM paired with a 74F838 creates a state machine. When reset, the PS_0-PS_4 outputs are zero. The present state is decoded to generate control inputs. In this application, a PLS151 acts as the state decoder. When a state has a branch option based on the state of a control signal, the Present is used as the address input to a multiplexer. The output of the multiplexer connects to the JUMP input of the 74F838. When the proper state is decoded, the associated control input is passed on to the JUMP input. In this application, to allow a forced jump, D_0 is also a control input. All state changes occur on the rising edge of the Clock input. However, since the interrupt input ($\overline{INT}$) is normally asynchronous in many applications, to avoid timing problems, $\overline{INT}$ is sampled on the falling edge of the Clock.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximun input voltage		V_{CC} =MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} =MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} =MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} =MAX, V_O= 2.25V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} =MAX				90	mA
		I_{CCL}					90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

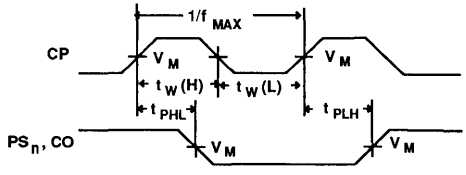
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	70	90				MHz
t_{PLH} t_{PHL}	Propagation delay CP to PS_n or CO	Waveform 1						ns
t_{PHL}	Propagation delay $\overline{RESET}$ to PS_n or CO.	Waveform 2						ns

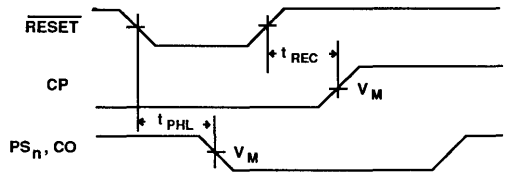
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low JS_n to CP	Waveform 3						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low JS_n to CP	Waveform 3						ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low JMP to CP	Waveform 3						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low JMP to CP	Waveform 3						ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{INT}$ to CP	Waveform 3						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{INT}$ to CP	Waveform 3						ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low SUB_n to CP	Waveform 3						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low SUB_n to CP	Waveform 3						ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low CI to CP	Waveform 3						ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CI to CP	Waveform 3						ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1						ns
$t_w(L)$	$\overline{RESET}$ Pulse width, Low	Waveform 2						ns
t_{REC}	Recovery Time, $\overline{RESET}$ to CP	Waveform 2						ns

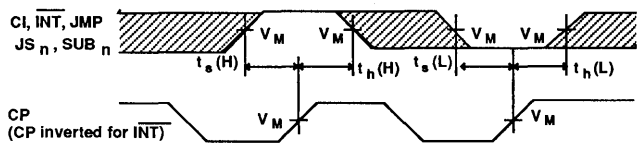
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock To Output, Clock Pulse Width, Maximum Clock Frequency



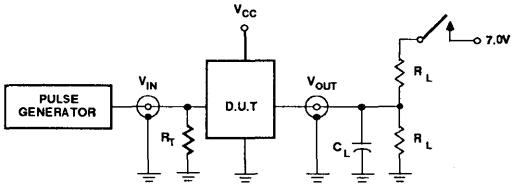
Waveform 2. Propagation Delay, Reset To Output, Reset To Clock Pulse Recovery Time



Waveform 3. Setup And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

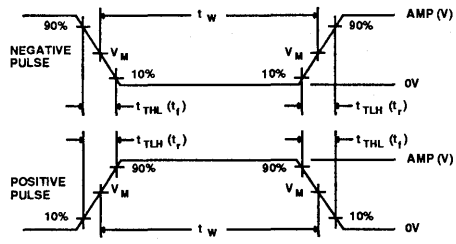
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F841/842/843/844/845/846
Bus Interface Latches

'F841/'F842 10-Bit Bus Interface Latches, NINV/INV (3-State)
'F843/'F844 9-Bit Bus Interface Latches, NINV/INV (3-State)
'F845/'F846 8-Bit Bus Interface Latches, NINV/INV (3-State)
Product Specification

FEATURES

- **High speed parallel latches**
- **Extra data width for wide address/ data paths or busses carrying parity**
- * **High impedance NPN base input structure minimizes bus loading**
- * **I_{IL} is 20μA vs 1000μA for AM29841 series**
- **Buffered control inputs to reduce AC effects**
- **Ideal where high speed, light loading, or increased fan-in are required as with MOS micro-processors**
- **Positive and negative over-shoots are clamped to ground**
- **3-state outputs glitch free during power-up and power-down**
- **48mA sink current**
- **Slim Dip 300 mil package**
- **Broadside pinout**
- **Pin-for-pin and function compat-ible with AMD AM29841-846 series**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F841, 74F842	5.5ns	60mA
74F843, 74F845	5.5ns	75mA
74F844, 74F846	6.2ns	60mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F841N, N74F842N, N74F843N, N74F844N, N74F845N, N74F846N
24-Pin Plastic SOL	N74F841D, N74F842D, N74F843D, N74F844D, N74F845D, N74F846D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_n	Data inputs	1.0/0.033	20μA/20μA
LE	Latch Enable input	1.0/0.033	20μA/20μA
$\overline{OE}$, $\overline{OE}_n$	Output Enable input (active-Low)	1.0/0.033	20μA/20μA
$\overline{MR}$	Master Reset input (active-Low)	1.0/0.033	20μA/20μA
$\overline{PRE}$	Preset input (active-Low)	1.0/0.033	20μA/20μA
Q_n	Data outputs	1200/80	24mA/48mA
$\overline{Q}_n$	Data outputs	1200/80	24mA/48mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 'F841-'846 bus interface latch series are designed to provide extra data width for wider address/data paths of busses carrying parity.

The 'F841-'F846 series are functionally and pin compatible to the AMD AM29841-AM29846 series.

The 'F841 consists of ten D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the LE High-to-Low transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is Low. When $\overline{OE}$ is High the output is in the High-impedance state

The 'F842 is the inverted output version of 'F841.

The 'F843 consists of nine D-type latches with 3-state outputs. In addition to the LE and $\overline{OE}$ pins, the 'F843 has a Master Reset ($\overline{MR}$) pin and Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{MR}$ is Low, the outputs are Low if $\overline{OE}$ is Low. When $\overline{MR}$ is High, data can be entered into the latch. When $\overline{PRE}$ is Low, the outputs are High, if $\overline{OE}$ is Low. $\overline{PRE}$ overrides $\overline{MR}$.

The 'F844 is the inverted output version of 'F843.

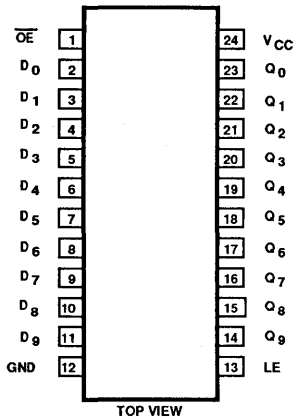
The 'F845 consists of eight D-type latches with 3-state outputs. In addition to the LE, $\overline{OE}$, $\overline{MR}$ and $\overline{PRE}$ pins, the 'F845 has two additional $\overline{OE}$ pins making a total of three Output Enables ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) pins. The multiple Output Enables ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$,

The 'F846 is the inverted output version of 'F845.

Bus Interface Latches FAST 74F841/842/843/844/845/846

PIN CONFIGURATION

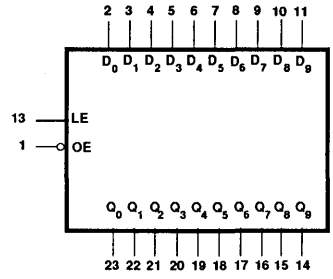
'F841



TOP VIEW

LOGIC SYMBOL

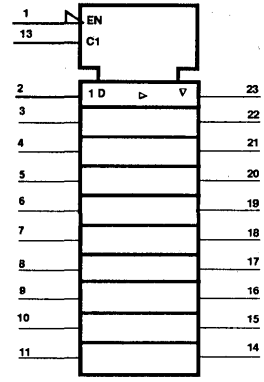
'F841



V_{CC} = Pin 24
GND = Pin 12

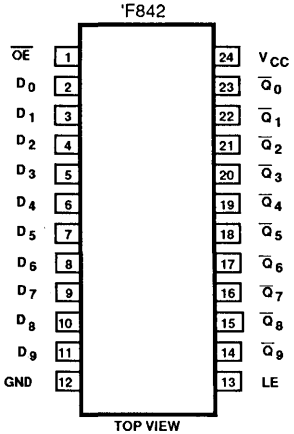
LOGIC SYMBOL(IEEE/IEC)

'F841



PIN CONFIGURATION

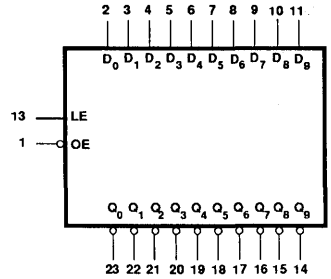
'F842



TOP VIEW

LOGIC SYMBOL

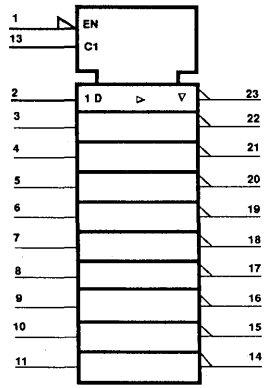
'F842



V_{CC} = Pin 24
GND = Pin 12

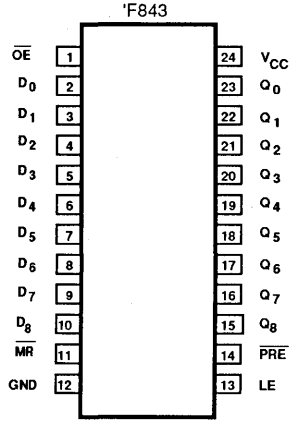
LOGIC SYMBOL(IEEE/IEC)

'F842



PIN CONFIGURATION

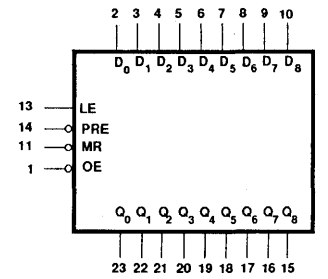
'F843



TOP VIEW

LOGIC SYMBOL

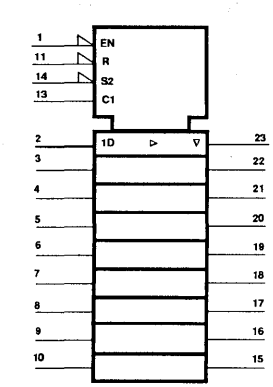
'F843



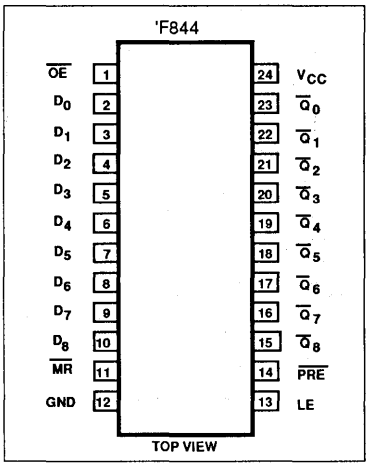
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

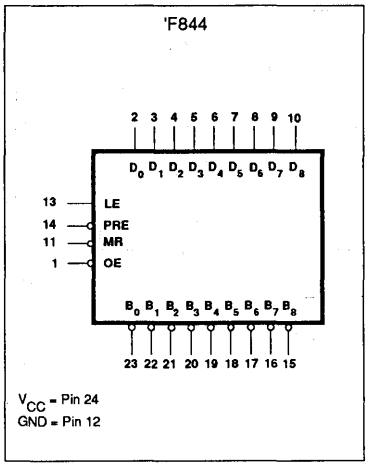
'F843



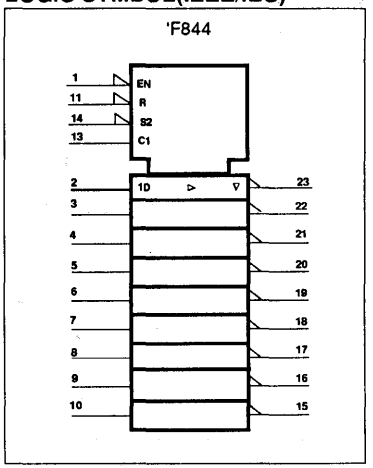
PIN CONFIGURATION



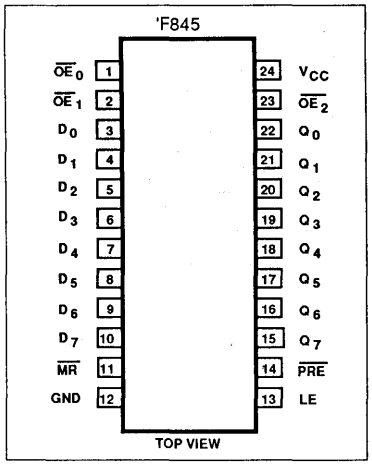
LOGIC SYMBOL



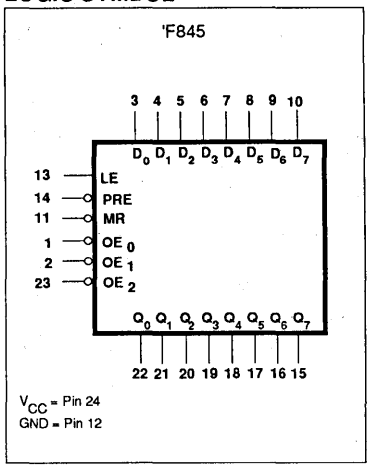
LOGIC SYMBOL(IEEE/IEC)



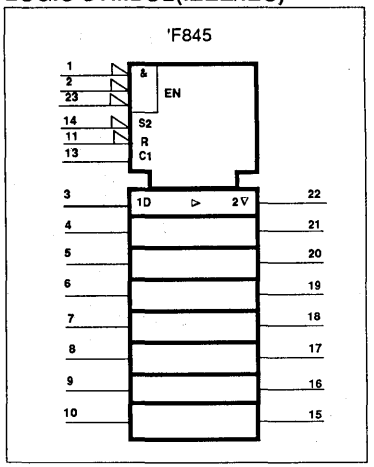
PIN CONFIGURATION



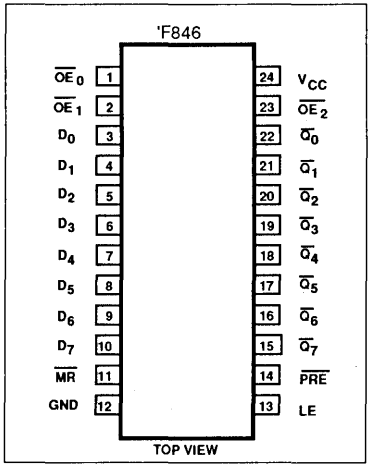
LOGIC SYMBOL



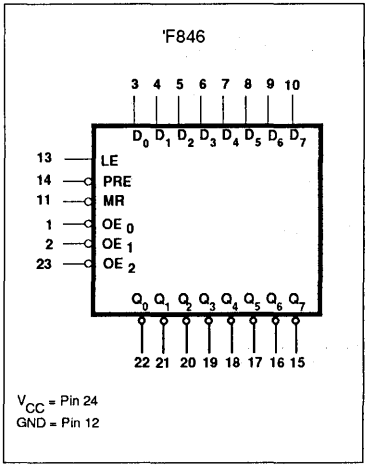
LOGIC SYMBOL(IEEE/IEC)



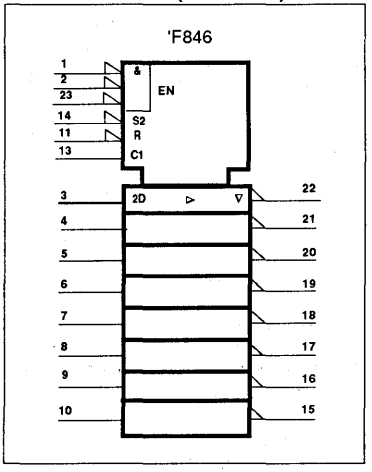
PIN CONFIGURATION



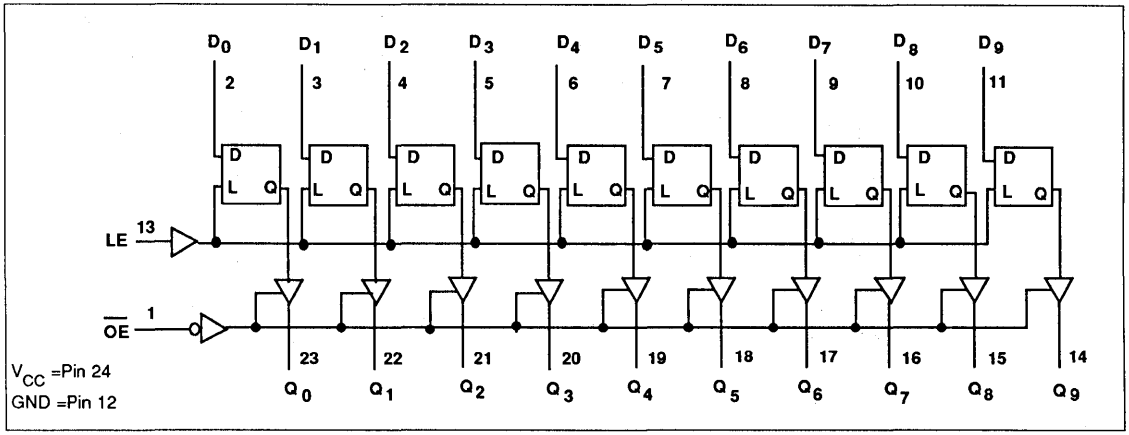
LOGIC SYMBOL



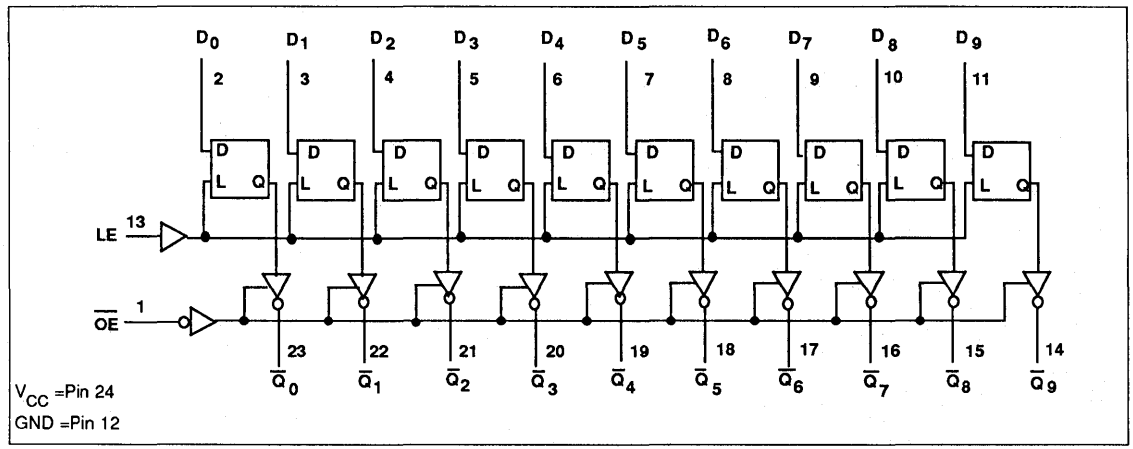
LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM for 'F841



LOGIC DIAGRAM for 'F842

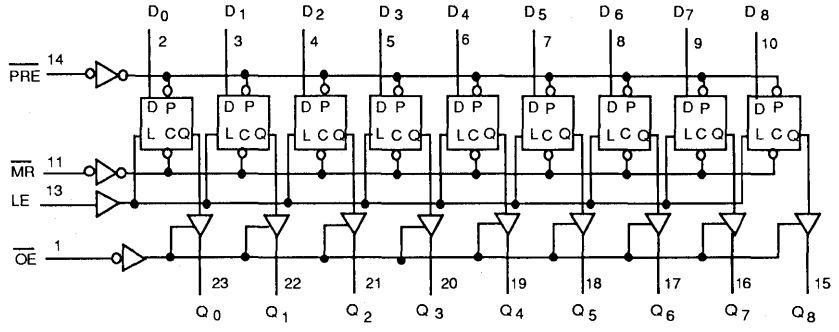


FUNCTION TABLE for 'F841 and 'F842

INPUTS			OUTPUTS		OPERATING MODE
			'F841	'F842	
$\overline{OE}$	LE	D_n	Q	$\overline{Q}$	
L	H	L	L	H	Transparent
L	H	H	H	L	
L	↓	l	L	H	Latched
L	↓	h	H	L	
H	X	X	Z	Z	High impedance
L	L	X	NC	NC	Hold

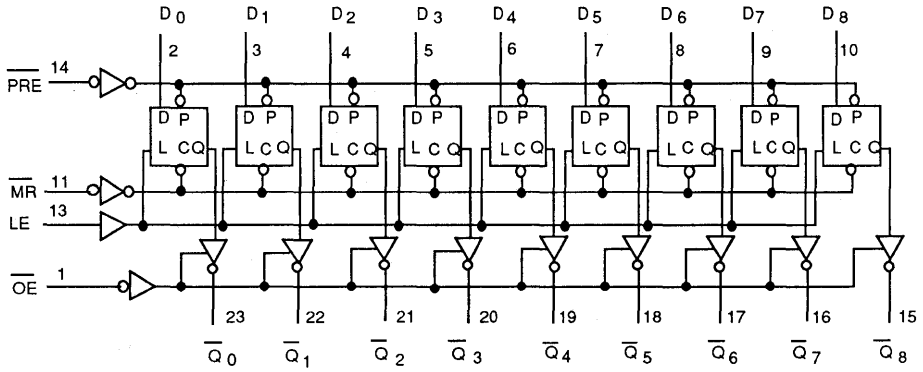
H= High voltage level
L= Low voltage level
h= High state one setup time before the High-to-Low LE transition
l = Low state one setup time before the High-to-Low LE transition
↓= High-to-Low transition
X=Don't care
NC=No change
Z =High impedance "off" state

LOGIC DIAGRAM for 'F843



V_{CC} =Pin 24
GND =Pin 12

LOGIC DIAGRAM for 'F844



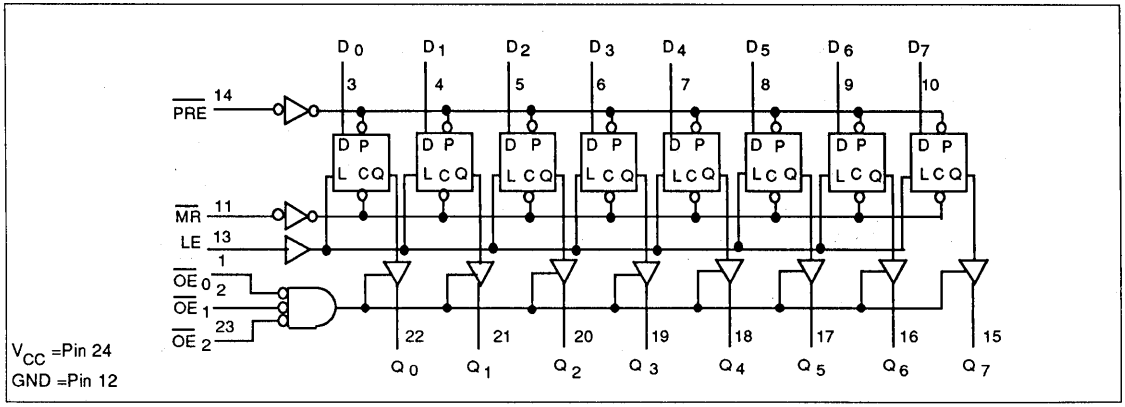
V_{CC} =Pin 24
GND =Pin 12

FUNCTION TABLE for 'F843 and 'F844

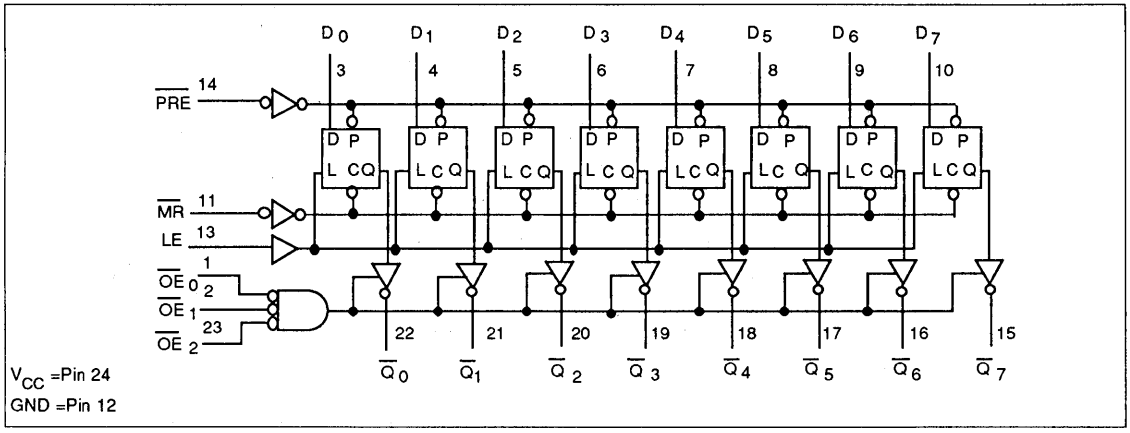
INPUTS					OUTPUTS		OPERATING MODE
					'F843	'F844	
$\overline{OE}$	$\overline{PRE}$	$\overline{MR}$	LE	D_n	Q	$\overline{Q}$	
L	L	X	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	H	H	H	L	L	H	Transparent
L	H	H	H	H	H	L	
L	H	H	↓	l	L	H	Latched
L	H	H	↓	h	H	L	
H	X	X	X	X	Z	Z	High impedance
L	H	H	L	X	NC	NC	Hold

H= High voltage level
L= Low voltage level
h= High state one setup time before the High-to-Low LE transition
l =Low state one setup time before the High-to-Low LE transition
↓=High-to-Low transition
X=Don't care
NC=No change
Z =High impedance "off " state

LOGIC DIAGRAM for 'F845



LOGIC DIAGRAM for 'F846



FUNCTION TABLE for 'F845 and 'F846

INPUTS					OUTPUTS		OPERATING MODE
					'F845	'F846	
$\overline{OE}_n$	$\overline{PRE}$	$\overline{MR}$	LE	D_n	Q	$\overline{Q}$	
L	L	X	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	H	H	H	L	L	H	Transparent
L	H	H	H	H	H	L	
L	H	H	↓	l	L	H	Latched
L	H	H	↓	h	H	L	
H	X	X	X	X	Z	Z	High impedance
L	H	H	L	X	NC	NC	Hold

H= High voltage level
L= Low voltage level
h= High state one setup time before the High-to-Low LE transition
l =Low state one setup time before the High-to-Low LE transition
↓=High-to-Low transition
X=Don't care
NC=No change
Z =High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	84	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			74F841, 74F842, 74F843, 74F844, 74F845, 74F846			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -15mA	±10% V_{CC}	2.4			V
						±5% V_{CC}	2.4	3.3		V
					I_{OH} = -24mA	±10% V_{CC}	2.0			V
						±5% V_{CC}	2.0			V
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 32mA	±10% V_{CC}		0.38	0.55	V
					I_{OL} = 48mA	±5% V_{CC}		0.38	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7 V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5 V					-20	µA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied			V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F841	I_{CCH}	V_{CC} = MAX				50	65	mA
			I_{CCL}					60	80	mA
			I_{CCZ}					70	92	mA
I_{CC}	Supply current (total)	'F842	I_{CCH}	V_{CC} = MAX				40	60	mA
			I_{CCL}					65	90	mA
			I_{CCZ}					60	90	mA
I_{CC}	Supply current (total)	'F843 'F845	I_{CCH}	V_{CC} = MAX				65	90	mA
			I_{CCL}					75	100	mA
			I_{CCZ}					85	115	mA
I_{CC}	Supply current (total)	'F844 'F846	I_{CCH}	V_{CC} = MAX				50	70	mA
			I_{CCL}					70	95	mA
			I_{CCZ}					70	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	74F841, 74F842					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	'F841	Waveform 1, 2	2.0 2.5	4.0 4.5	7.5 7.5	2.0 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay LE to Q_n or $\overline{Q}_n$	'F841	Waveform 1, 2	4.5 4.0	6.5 6.0	9.5 9.0	4.0 3.5	10.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	'F842	Waveform 1, 2	3.5 3.0	5.5 5.0	8.5 8.0	4.5 4.0	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to Q_n or $\overline{Q}_n$	'F842	Waveform 1, 2	5.0 4.5	7.0 6.5	10.0 9.0	3.0 3.0	10.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, $\overline{OE}_n$ to Q_n or $\overline{Q}_n$		Waveform 5 Waveform 6	2.5 6.5	4.5 8.5	8.0 12.0	2.0 5.5	8.5 13.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level, $\overline{OE}_n$ to Q_n or $\overline{Q}_n$		Waveform 5 Waveform 6	1.0 1.0	4.5 5.0	8.0 8.0	1.0 1.0	8.5 8.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	74F841, 74F842					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, High or Low D_n to LE		Waveform 4	0.0 0.0			1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to LE	'F841	Waveform 4	2.5 3.0			3.0 4.0		ns
$t_w(H)$	LE Pulse width, High	'F841	Waveform 4	3.5			4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to LE	'F842	Waveform 4	3.0 3.5			3.5 4.5		ns
$t_w(H)$	LE Pulse width, High	'F842	Waveform 4	3.0			3.0		ns

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F843, 74F845					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	Waveform 1, 2	2.0 2.5	4.5 4.5	7.5 8.0	2.0 2.5	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to Q_n or $\overline{Q}_n$	Waveform 1, 2	4.5 4.0	6.5 6.0	9.5 8.5	4.0 4.0	10.0 8.5	ns
t_{PLH}	Propagation delay $\overline{PRE}$ to Q_n or $\overline{Q}_n$	Waveform 3	3.5	5.5	8.5	3.0	9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n or $\overline{Q}_n$	Waveform 3	2.0	4.5	7.5	2.0	8.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, $\overline{OE}_n$ to Q_n or $\overline{Q}_n$	Waveform 5 Waveform 6	2.5 5.5	4.5 7.5	7.5 10.5	2.0 5.0	8.0 11.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level, $\overline{OE}_n$ to Q_n or $\overline{Q}_n$	Waveform 5 Waveform 6	1.0 1.0	4.5 5.0	8.0 8.0	1.0 1.0	8.5 8.5	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	74F843, 74F845					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Set-up time, High or Low D_n to LE	Waveform 4	1.0 1.0			1.0 1.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to LE	Waveform 4	3.0 2.5			3.0 3.0		ns
t_w(H)	LE Pulse width, High	Waveform 4	3.5			3.5		ns
t_w(L)	$\overline{PRE}$ Pulse width, Low	Waveform 3	7.0			7.5		ns
t_w(L)	$\overline{MR}$ Pulse width, Low	Waveform 3	4.5			4.5		ns
t_{rec}	$\overline{PRE}$ Recovery time	Waveform 3	0.0			0.0		ns
t_{rec}	$\overline{MR}$ Recovery time	Waveform 3	2.0			2.0		ns

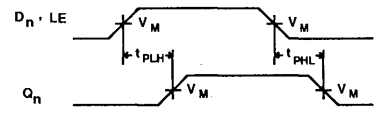
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F844, 74F846					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n or $\overline{Q}_n$	Waveform 1, 2	3.5 3.0	5.5 5.0	8.5 8.0	3.0 3.0	9.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to Q_n or $\overline{Q}_n$	Waveform 1, 2	5.0 4.5	7.0 6.5	10.0 9.0	5.0 4.5	10.5 9.5	ns
t_{PLH}	Propagation delay $\overline{PRE}$ to Q_n or $\overline{Q}_n$	Waveform 3	3.5	5.5	8.5	3.0	9.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n or $\overline{Q}_n$	Waveform 3	5.0	7.0	10.0	4.5	10.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level, $\overline{OE}_n$ to Q_n or $\overline{Q}_n$	Waveform 5 Waveform 6	2.5 6.5	5.0 8.5	7.5 11.5	2.0 5.5	8.0 12.5	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level, $\overline{OE}_n$ to Q_n or $\overline{Q}_n$	Waveform 5 Waveform 6	1.0 1.0	4.5 5.0	8.0 8.0	1.0 1.0	8.5 8.5	ns

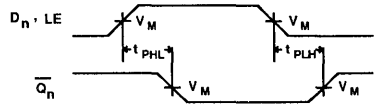
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	74F844, 74F846					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Set-up time, High or Low D_n to LE	Waveform 4	0.0 0.0			0.0 0.0		ns
t_h(H) t_h(L)	Hold time, High or Low D_n to LE	Waveform 4	3.0 4.0			3.0 4.0		ns
t_w(H)	LE Pulse width, High	Waveform 4	3.0			3.0		ns
t_w(L)	$\overline{PRE}$ Pulse width, Low	Waveform 3	4.0			5.0		ns
t_w(L)	$\overline{MR}$ Pulse width, Low	Waveform 3	4.0			5.0		ns
t_{rec}	$\overline{PRE}$ Recovery time	Waveform 3	0.0			0.0		ns
t_{rec}	$\overline{MR}$ Recovery time	Waveform 3	3.5			4.5		ns

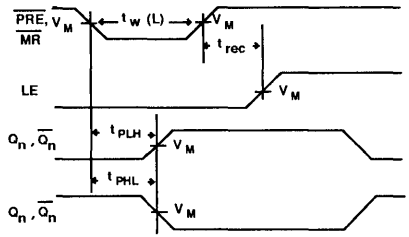
AC WAVEFORMS



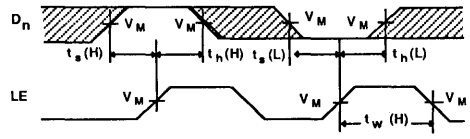
Waveform 1. Propagation Delay, Non-Inverting Path



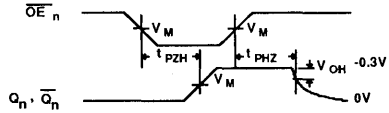
Waveform 2. Propagation Delay, Inverting Path



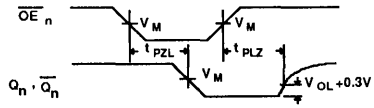
Waveform 3.
Master Reset and Preset Pulse Width, Master Reset and Preset to Output Delay and Master Reset and Preset to Latch Enable Recovery Time



Waveform 4. Data Setup And Hold Times



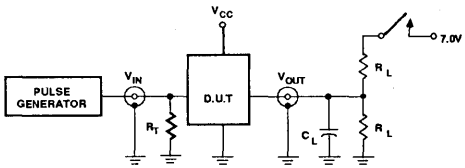
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

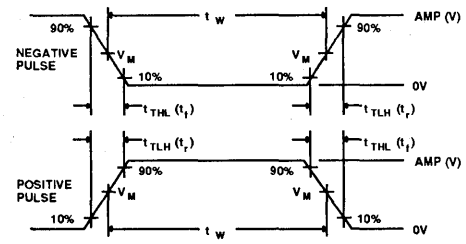
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F861, 74F862, 74F863, 74F864 Bus Transceivers

'F861/'F862 10-Bit Bus Transceivers, NINV/INV (3-State)
'F863/'F864 9-Bit Bus Transceivers, NINV/INV (3-State)
Product Specification

FAST Products

FEATURES

- **Provide high performance bus interface buffering for wide data/address paths or busses carrying parity**
- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **I_{IL} is 20μA vs 1000μA for AM29861 series**
- **Buffered control inputs for light loading, or increased fan-in as required with MOS microprocessors**
- **Positive and negative over-shoots are clamped to ground**
- **3-state outputs glitch free during power-up and power-down**
- **Slim Dip 300 mil package**
- **Broadside pinout compatible with AMD AM 29861-29864 series**
- **Outputs sink 64mA**

DESCRIPTION

The 74F861 series Bus Transceivers provide high performance bus interface buffering for wide data/address paths of busses carrying parity. The 'F863/'F864 9-bit Bus Transceivers have NOR-ed transmit and receive output enables for maximum control flexibility.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F861, 74F862	6.0ns	150mA
74F863, 74F864	6.0ns	115mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F861N, N74862N, 74F863N, N74F864N
24-Pin Plastic SOL[1]	N74F861D, N74F862D, 74F863D, N74F864D

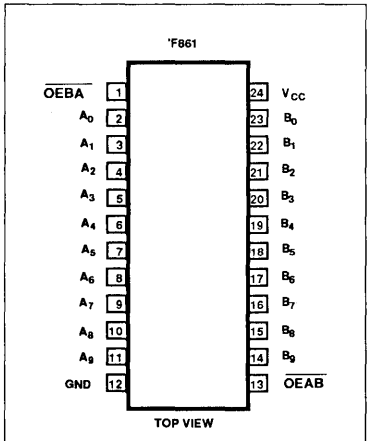
NOTE:
1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal considerations for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

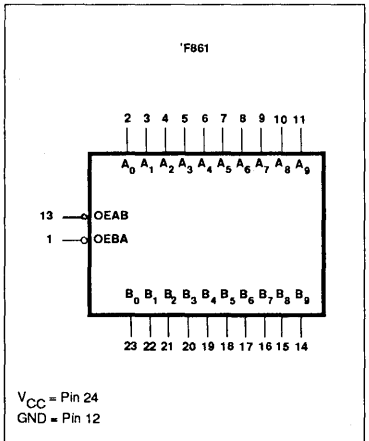
PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
'F861 'F862	A_0 - A_9	Data transmit inputs	3.5/0.117	70μA/70μA
	B_0 - B_9	Data receive inputs	3.5/0.117	70μA/70μA
	$\overline{OEBA}$	Transmit output enable input	1.0/0.033	20μA/20μA
	$\overline{OEAB}$	Receive output enable input	1.0/0.033	20μA/20μA
	A_0 - A_9	Data transmit outputs	1200/106.7	24mA/64mA
	B_0 - B_9	Data receive outputs	1200/106.7	24mA/64mA
'F863 'F864	A_0 - A_9	Data transmit inputs	3.5/0.117	70μA/70μA
	B_0 - B_9	Data receive inputs	3.5/0.117	70μA/70μA
	$\overline{OEBA}_n$	Transmit output enable inputs	1.0/0.033	20μA/20μA
	$\overline{OEAB}_n$	Receive output enable inputs	1.0/0.033	20μA/20μA
	A_0 - A_8	Data transmit outputs	1200/106.7	24mA/64mA
	B_0 - B_8	Data receive outputs	1200/106.7	24mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

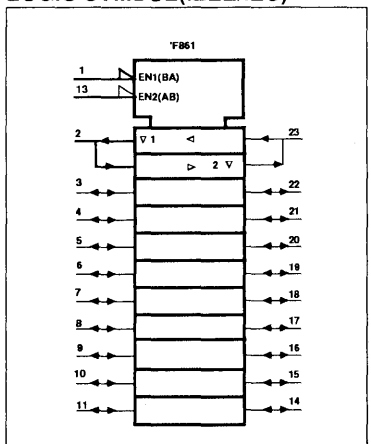
PIN CONFIGURATION



LOGIC SYMBOL

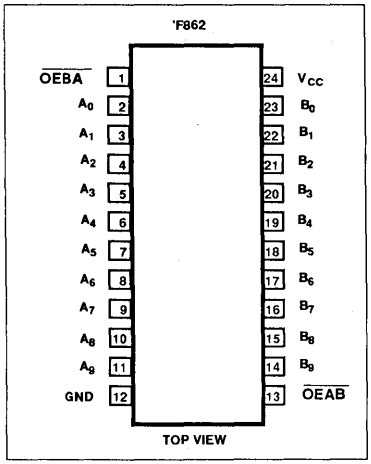


LOGIC SYMBOL(IEEE/IEC)

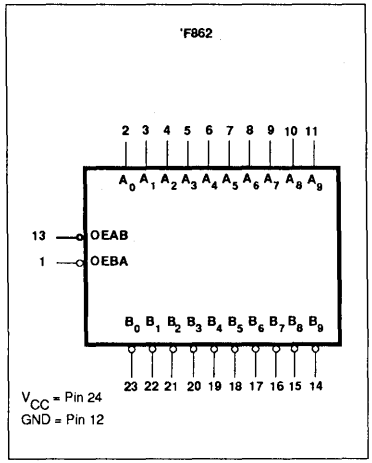


Bus Transceivers — FAST 74F861, 74F862, 74F863,74F864

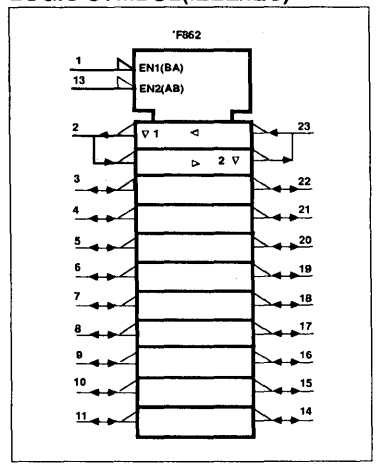
PIN CONFIGURATION



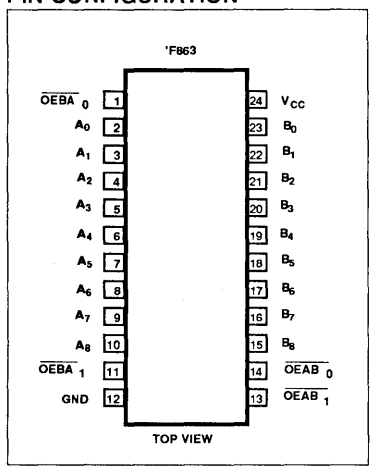
LOGIC SYMBOL



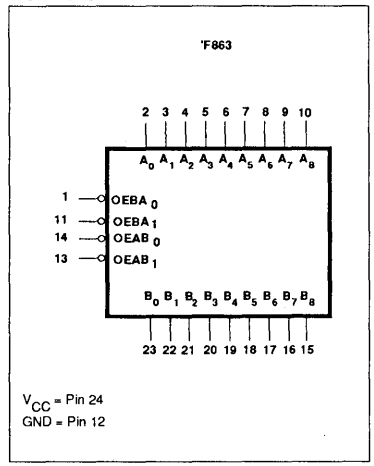
LOGIC SYMBOL(IEEE/IEC)



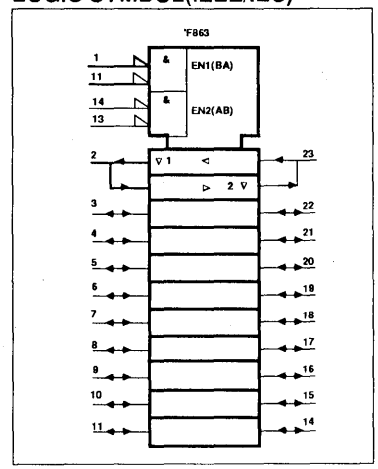
PIN CONFIGURATION



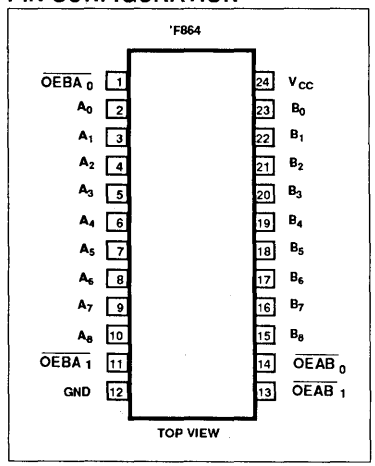
LOGIC SYMBOL



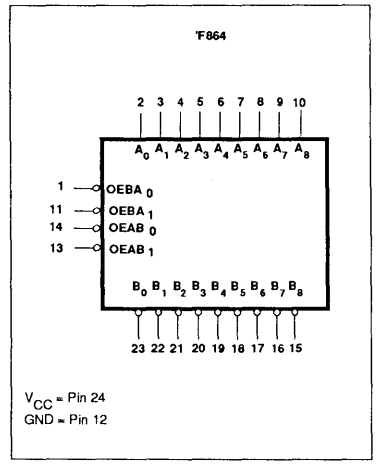
LOGIC SYMBOL(IEEE/IEC)



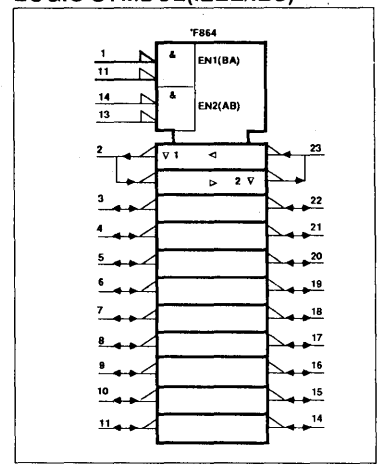
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

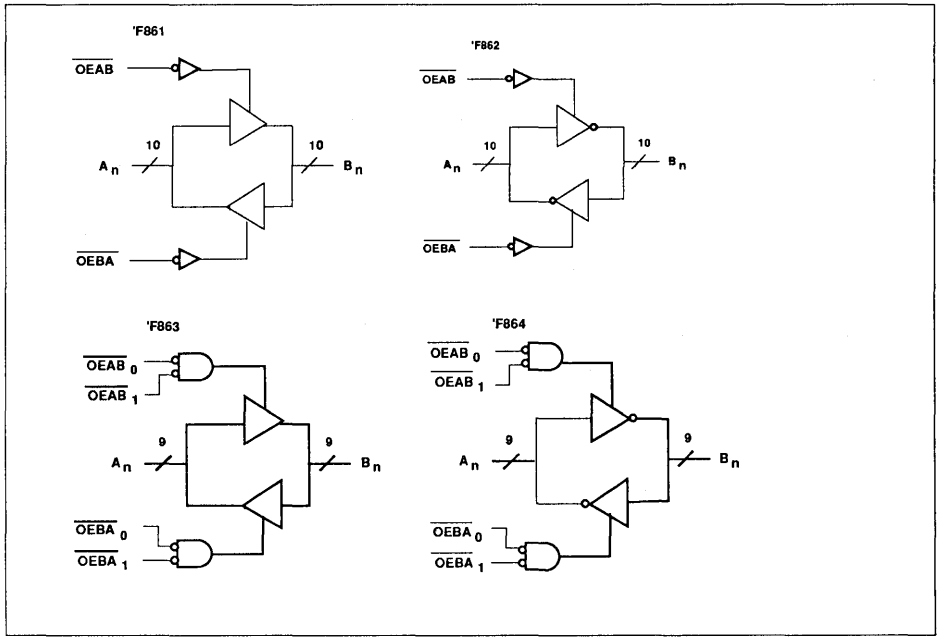


FUNCTION TABLE for 'F861 and 'F862

INPUTS		OPERATING MODES	
$\overline{OEAB}$	$\overline{OEBA}$	'F861	'F862
L	H	A data to B bus	A data to B bus
H	L	B bus to A data	B bus to A data
H	H	Z	Z

H = High voltage level
L = Low voltage level
Z = High impedance "off" state

LOGIC DIAGRAM



FUNCTION TABLE for 'F863 and 'F864

INPUTS				OPERATING MODES	
$\overline{OEAB}_0$	$\overline{OEAB}_1$	$\overline{OEBA}_0$	$\overline{OEBA}_1$	'F863	'F864
L	L	H	X	A data to B bus	A data to B bus
L	L	X	H		
H	X	L	L	B bus to A data	B bus to A data
X	H	L	L		
H	H	H	H	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-24	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-15mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.4	3.3		V
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-24mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEAB}$, $\overline{OEBA}$ $\overline{OEAB}_n$, $\overline{OEBA}_n$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_n, B_n	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
$I_{IH}+I_{OZH}$	High-level input current	A_n, B_n	V_{CC} = MAX, V_O= 2.7V					70	µA
$I_{IL}+I_{OZL}$	Low-level input current		V_{CC} = MAX, V_O= 0.5V					-70	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F861 'F863	I_{CCH}	V_{CC} = MAX			145	195	mA
			I_{CCL}				140	195	mA
			I_{CCZ}				165	220	mA
		'F862 'F864	I_{CCH}	V_{CC} = MAX			90	130	mA
			I_{CCL}				120	170	mA
			I_{CCZ}				130	160	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

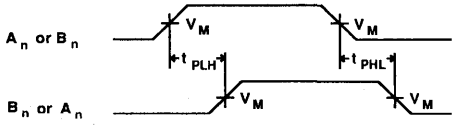
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F861, 74F863					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	4.0 3.0	6.0 5.0	9.0 8.0	3.5 2.5	10.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	4.0 2.5	6.0 5.0	9.0 8.0	3.5 2.5	10.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	6.0 4.5	8.0 7.0	11.5 10.5	5.0 4.5	13.0 12.0	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	6.0 5.5	8.0 7.5	11.0 11.0	5.0 4.5	13.0 12.0	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	3.5 2.5	5.5 5.0	9.0 8.5	3.0 2.0	9.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	3.5 2.5	5.5 4.5	8.5 8.5	3.0 2.0	9.5 9.5	ns

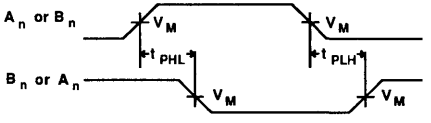
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F862, 74F864					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	4.0 1.5	6.0 3.5	9.0 6.5	3.0 1.5	10.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	4.0 1.5	6.0 3.5	9.0 6.5	3.0 1.5	10.5 7.0	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	6.5 7.0	8.5 9.5	12.0 13.5	5.5 6.0	13.5 15.5	ns
t_{PZH} t_{PZL}	Output Enable time High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	6.5 7.5	8.0 9.5	11.5 13.5	5.5 6.5	13.5 15.5	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level $\overline{OEBA}_n$ to A_n	Waveform 3 Waveform 4	3.0 2.5	5.0 4.0	8.5 8.5	2.5 2.0	9.5 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable time High or Low level $\overline{OEAB}_n$ to B_n	Waveform 3 Waveform 4	3.0 2.5	5.0 4.0	8.5 8.5	2.5 2.0	9.5 9.0	ns

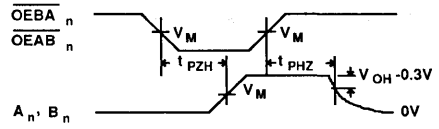
AC WAVEFORMS



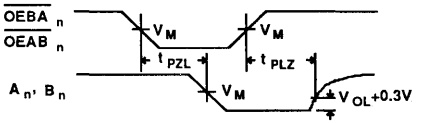
Waveform 1. Propagation Delay For Non-Inverting Output



Waveform 2. Propagation Delay For Inverting Output



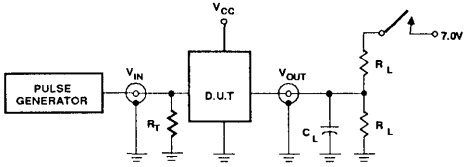
Waveform 3 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

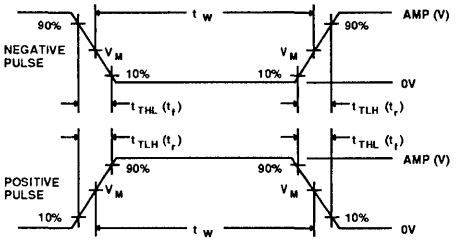
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F881
Arithmetic Logic Unit

FAST Products

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F881	7.3 ns	48mA

FEATURES

- Full look-ahead carry for high speed arithmetic operation on long words
- Arithmetic Operating Modes:
  - -Addition
  - -Subtraction
  - -Shift operand A one position
  - -magnitude comparison
  - -plus twelve other arithmetic operations
- Logic Function Modes:
  - -Exclusive-OR
  - -Comparator
  - -AND, NAND, OR, NOR
  - -provides status register check
  - -plus ten other logic operations
- Replaces 'AS881
- Same pinout and functions as 'F181 except for $\overline{P}$, $\overline{G}$, and C_{n+4} outputs when the device is in Logic Mode (M=H)
- Available in 300 mil-wide Slim 24 pin Dip package

ORDERING INFORMATION

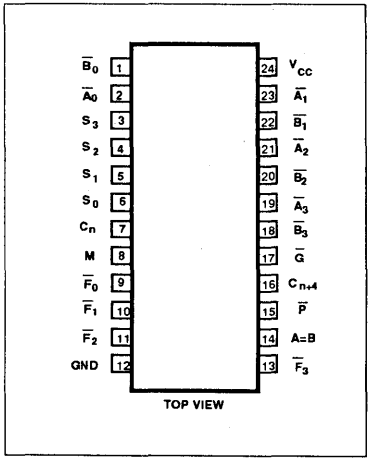
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300 mil)	N74F881N
24-Pin Plastic SOL	N74F881D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

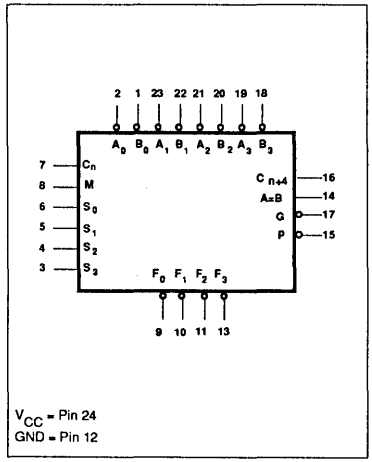
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{A}_0$-$\overline{A}_3$	A operand inputs	3.0/3.0	60µA/1.8mA
$\overline{B}_0$-$\overline{B}_3$	B operand inputs	3.0/3.0	60µA/1.8mA
M	Mode control input	1.0/1.0	20µA/0.6mA
S_0-S_3	Function select inputs	4.0/4.0	80µA/2.4mA
C_n	Carry input	6.0/6.0	120µA/3.6mA
C_{n+4}	Carry output	50/33	1.0mA/20mA
$\overline{P}$	Carry Propagate output	50/33	1.0mA/20mA
$\overline{G}$	Carry Generate output	50/33	1.0mA/20mA
A=B	Compare output	OC/33	OC/20mA
$\overline{F}_0$-$\overline{F}_3$	Outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC=Open Collector

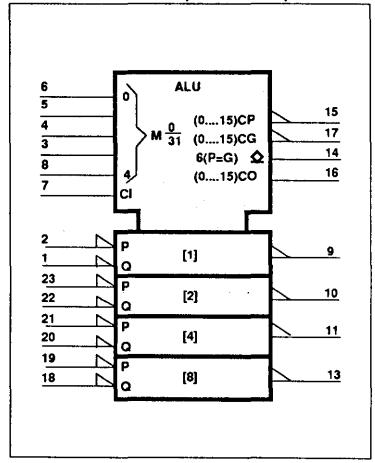
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Arithmetic Logic Unit | FAST 74F881

PIN DESIGNATION TABLE

Pin number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
I (active-Low data)	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	$\overline{F}_0$	$\overline{F}_1$	$\overline{F}_2$	$\overline{F}_3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
II (active-High data)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

DESCRIPTION

The 74F881 is an Arithmetic Logic Unit (ALU)/ function generator that has a complexity of 77 equivalent gates on a monolithic chip. This circuit performs 16 binary arithmetic operation on two 4-bits word as shown in Tables 1 and 2. These operations are selected by the four function select lines (S_0, S_1, S_2, S_3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a Low level voltage to the Mode control input (M). A full carry look- ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the 'F882 full carry look-ahead circuit, high speed arithmetic operations can be performed.

The method of cascading 'F882 circuits with these ALUs to provide multi-level full carry look-ahead is illustrated under signal designation.

If high speed is not important, a ripple carry input (C_n) and a ripple carry output (C_{n+4}) are available. However, the ripple carry delay has also been minimized so that arithmetic manupilations for small word lengths can be performed without external circuitry.

The 'F881 will accomodate active-High or active-Low data if the pin designations are interpreted as indicated in the Pin Designation Table.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

The 'F881 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F_0, F_1, F_2, F_3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a High level to indicate equality (A=B). The ALU must be in the subtract mode with C_n=H when performing the comparison. The A=B output is open collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select lines (S_3, S_2,S_1, S_0) at L, H, H, L respectively.

This circuit has been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select lines (S_0, S_1, S_2, S_3) with the mode-control input (M) at a High level to disable the internal carry. The 16 logic functions are detailed in the Logic Function Table and include Exclusive-OR, NAND, AND, NOR, and OR functions.

The 'F881 has the same pinout and same fuctionality as the 'F181 exccept for the $\overline{P}$, $\overline{G}$, and C_{n+4} outputs when the device is in the logic mode (M=H).

In the logic mode the 'F881 provides the user with a status check on the input word A and B, and the output word F. While in the logic mode the $\overline{P}$, $\overline{G}$, and C_{n+4} outputs supply status information based upon the following logical combinations:

$$\overline{P} = F_0 + F_1 + F_2 + F_3$$
$$\overline{G} = H$$
$$C_{n+4} = PC_n$$

The combination of signals on the S_3 through S_0 function select lines determine the operation performed on the data words to generate the output $\overline{F}_i$. By monitoring the $\overline{P}$ and C_{n+4} outputs, the user can determine if all pairs of input bits are equal of if any pair of inputs are both High (see Function Table). The 'F881 has the unique feature of providing A=B status while the Exclusive-OR function is being utilized. When the function select lines (S_3, S_2,S_1, S_0) equal H, L, L, H ; a status check is generated to determine whether all pairs ($\overline{A}_i$, $\overline{B}_i$) are equal in the following manner: $\overline{P} = (A_0 \oplus B_0) + (A_1 \oplus B_1) + (A_2 \oplus B_2) + (A_3 \oplus B_3)$. This unique bit-by-bit comparison of the data words which is available on the totem pole $\overline{P}$ output is particularly useful when cascading 'F881s. As the A=B condition is sensed in the first stage the signal is propagated through the same ports used for carry generation in the arithmetic mode ($\overline{P}$ and $\overline{G}$). Thus the A=B status is transmitted to the second stage more quickly without the need for external multiplexing logic. The A=B open collector output allows the user to check the validity of the bit-by-bit result by comparing the two signals for parity.

If the user wishes to check for any pair of data inputs ($\overline{A}_i$, $\overline{B}_i$) being High, it is necessary to set the function select lines (S_3, S_2,S_1, S_0) to L, H, L, L. The data pairs will then be ANDed together and the results ORed in the following manner: $\overline{P} = \overline{A}_0\overline{B}_0 + \overline{A}_1\overline{B}_1 + \overline{A}_2\overline{B}_2 + \overline{A}_3\overline{B}_3$.

SIGNAL DESIGNATIONS

In both Figures 1 and 2, the polarity indicators (▷) indicate that the associated input or output is active-Low with respect to the function shown inside the symbol. The symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-Low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accomodate the logic functions and arithmetic operations for the active-High data given in Table 2. The 'F181 and 'F881 together with the 'F882 and 'F182 can be used with the signal designation of either FIgure 1 or Figure 2.

COMPARATOR TABLE

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA	ACTIVE-HIGH DATA
H	H	A≥B	A≤B
H	L	A<B	A>B
L	H	A>B	A<B
L	L	A≤B	A≥B

H = High voltage level
L = Low voltage level

FUNCTION TABLE FOR INPUT BITS EQUAL/NOT EQUAL
$S_0=S_3=H$, $S_1=S_2=L$, and M=H

C_n	DATA INPUTS				OUTPUTS		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	$A_0=B_0$	$A_1=B_1$	$A_2=B_2$	$A_3=B_3$	H	L	H
L	$A_0=B_0$	$A_1=B_1$	$A_2=B_2$	$A_3=B_3$	H	L	L
X	$A_0\neq B_0$	X	X	X	H	H	L
X	X	$A_1\neq B_1$	X	X	H	H	L
X	X	X	$A_2\neq B_2$	X	H	H	L
X	X	X	X	$A_3\neq B_3$	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE FOR INPUT PAIRS HIGH/NOT HIGH
$S_0=S_1=S_3=L$, $S_2=H$, and M=H

C_n	DATA INPUTS				OUTPUTS		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	$\overline{A}_0$ or $\overline{B}_0$=L	$\overline{A}_1$ or $\overline{B}_1$=L	$\overline{A}_2$ or $\overline{B}_2$=L	$\overline{A}_3$ or $\overline{B}_3$=L	H	L	H
L	$\overline{A}_0$ or $\overline{B}_0$=L	$\overline{A}_1$ or $\overline{B}_1$=L	$\overline{A}_2$ or $\overline{B}_2$=L	$\overline{A}_3$ or $\overline{B}_3$=L	H	L	L
X	$\overline{A}_0=\overline{B}_0$=H	X	X	X	H	H	L
X	X	$\overline{A}_1=\overline{B}_1$=H	X	X	H	H	L
X	X	X	$\overline{A}_2=\overline{B}_2$=H	X	H	H	L
X	X	X	X	$\overline{A}_3=\overline{B}_3$=H	H	H	L

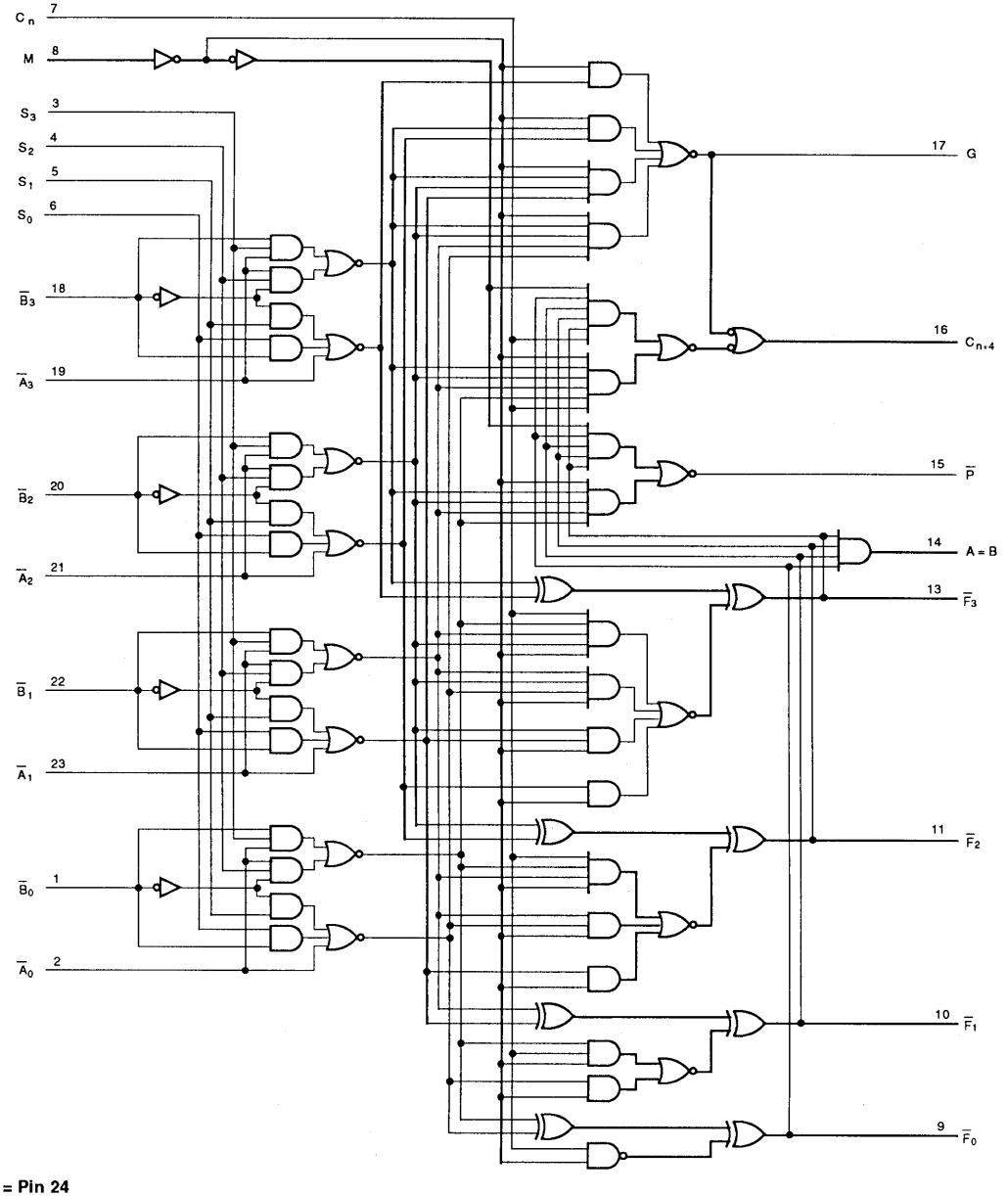
H = High voltage level
L = Low voltage level
X = Don't care

SELECT TABLE FOR DATA INPUT PAIRS

S_3	S_2	S_1	S_0	M	$\overline{P}=F_0+F_1+F_2+F_3$
L	H	L	L	H	$\overline{A}_0\overline{B}_0+\overline{A}_1\overline{B}_1+\overline{A}_2\overline{B}_2+\overline{A}_3\overline{B}_3$
H	L	L	H	H	$(A_0 \oplus B_0)+(A_1 \oplus B_1)+(A_2 \oplus B_2)+(A_3 \oplus B_3)$

H = High voltage level
L = Low voltage level

LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12

APPLICATION

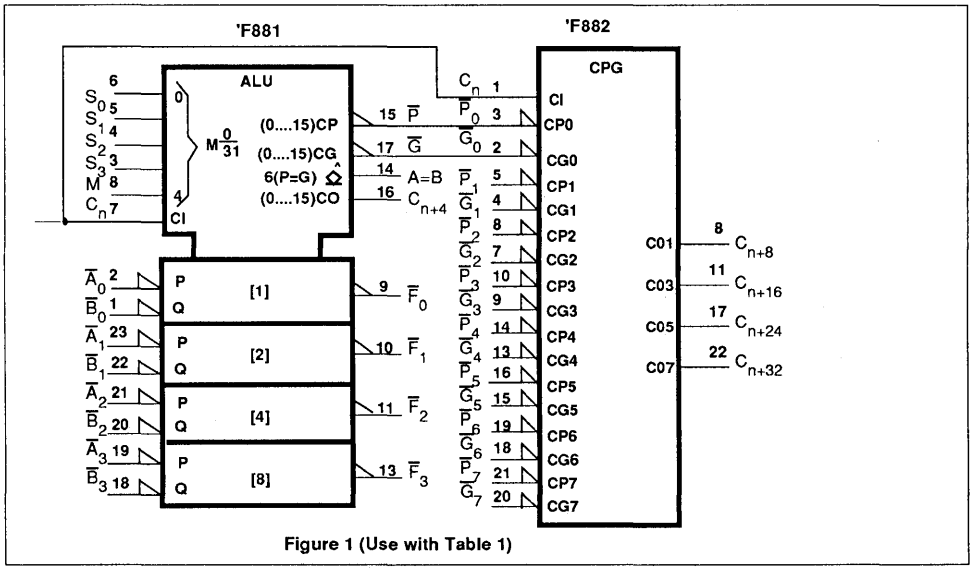


Figure 1 (Use with Table 1)

TABLE 1

SELECTION				ACTIVE LOW DATA		
S_3	S_2	S_1	S_0	(M=H) Logic Functions	M=L; Arithmetic Operations	
					C_n=L (no carry)	C_n=H (with carry)
L	L	L	L	F=$\overline{A}$	F=A minus 1	F=A
L	L	L	H	F=$\overline{AB}$	F=AB minus 1	F=AB
L	L	H	L	F=$\overline{A}$+B	F=A$\overline{B}$ minus 1	F=A$\overline{B}$
L	L	H	H	F=1	F=minus 1 (2's complement)	F=zero
L	H	L	L	F=$\overline{A + B}$	F=A plus (A+$\overline{B}$)	F=A plus (A+$\overline{B}$) plus 1
L	H	L	H	F=$\overline{B}$	F=AB plus (A+$\overline{B}$)	F=AB plus (A+$\overline{B}$) plus 1
L	H	H	L	F=$\overline{A \oplus B}$	F=A minus B minus 1	F=A minus B
L	H	H	H	F=A + $\overline{B}$	F=A+$\overline{B}$	F=(A + $\overline{B}$) plus 1
H	L	L	L	F=$\overline{A}$B	F=A plus (A+B)	F=A plus (A+B) plus 1
H	L	L	H	F=A$\oplus$B	F=A plus B	F=A plus B plus 1
H	L	H	L	F=B	F=A$\overline{B}$ plus (A+B)	F=A$\overline{B}$ plus (A+B) plus 1
H	L	H	H	F=A+B	F=(A+B)	F=A+B plus 1
H	H	L	L	F=0	F=A plus A*	F=A plus A plus 1
H	H	L	H	F=A$\overline{B}$	F=AB plus A	F=AB plus A plus 1
H	H	H	L	F=AB	F=A$\overline{B}$ plus A	F=A$\overline{B}$ plus A plus 1
H	H	H	H	F=A	F=A	F=A plus 1

H = High voltage level
L = Low voltage level
* = Each bit is shifted to the next more significant position.

APPLICATION

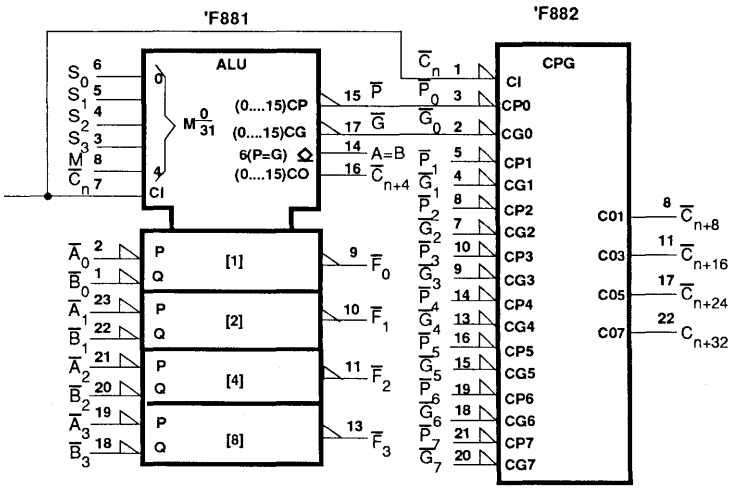


Figure 2 (Use with Table 2)

TABLE 1

SELECTION				ACTIVE HIGH DATA		
S_3	S_2	S_1	S_0	(M=H) Logic Functions	M=L; Arithmetic Operations	
					$\overline{C}_n$=H (no carry)	$\overline{C}_n$=L (with carry)
L	L	L	L	F=$\overline{A}$	F=A	F=A plus 1
L	L	L	H	F=$\overline{A+B}$	F=A+B	F=(A+B) plus 1
L	L	H	L	F=$\overline{A}$B	F=A+$\overline{B}$	F=(A+$\overline{B}$) plus 1
L	L	H	H	F=0	F=minus 1 (2's complement)	F=zero
L	H	L	L	F=$\overline{AB}$	F=A plus A$\overline{B}$	F=A plus A$\overline{B}$ plus 1
L	H	L	H	F=$\overline{B}$	F=(A+B) plus A$\overline{B}$	F=(A+B) plus A$\overline{B}$ plus 1
L	H	H	L	F=A $\oplus$ B	F=A minus B minus 1	F=A minus B
L	H	H	H	F=A$\overline{B}$	F=A$\overline{B}$ minus 1	F=A$\overline{B}$
H	L	L	L	F=$\overline{A}$+B	F=A plus AB	F=A plus AB plus 1
H	L	L	H	F=$\overline{A \oplus B}$	F=A plus B	F=A plus B plus 1
H	L	H	L	F=B	F=(A+$\overline{B}$) plus AB	F=(A+$\overline{B}$) plus AB plus 1
H	L	H	H	F=AB	F=AB minus 1	F=AB
H	H	L	L	F=1	F=A plus A*	F=A plus A plus 1
H	H	L	H	F=A+$\overline{B}$	F=(A+B) plus A	F=(A+B) plus A plus 1
H	H	H	L	F=A+B	F=(A+$\overline{B}$) plus A	F=(A+$\overline{B}$) plus A plus 1
H	H	H	H	F=A	F=A minus 1	F=A

H = High voltage level
L = Low voltage level
* = Each bit is shifted to the next more significant position.

Table 3. SUM MODE TEST TABLE **Function Inputs:** $S_0=S_3=4.5V$, $S_1=S_2=M=0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$,C_n	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$,C_n	$\overline{G}$
t_{PLH}, t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$,C_n	$\overline{G}$
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$,C_n	C_{n+4}
t_{PLH}, t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$,C_n	C_{n+4}
t_{PLH}, t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

Table 4. DIFF MODE TEST TABLE **Function Inputs:** $S_1=S_2=4.5V$, $S_0=S_3=M=0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$,C_n	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$,C_n	$\overline{F}_i$
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$, $\overline{B}$,C_n	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	$\overline{G}$
t_{PLH}, t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	$\overline{G}$
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$,C_n	A=B
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$,C_n	A=B
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$,C_n	C_{n+4}
t_{PLH}, t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$, $\overline{B}$,C_n	C_{n+4}
t_{PLH}, t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	Any $\overline{F}$ or C_{n+4}

Table 5. DIFF MODE TEST TABLE

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$,C_n	$\overline{F}_i$	$S_1=S_2=M=4.5V$,$S_0=S_3=0V$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$,C_n	$\overline{F}_i$	$S_1=S_2=M=4.5V$,$S_0=S_3=0V$

Table 6. INPUT BITS EQUAL/NOT EQUAL TEST TABLE **Function Inputs:** $S_0=S_3=M=4.5V$, $S_1=S_2=0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	None	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	None	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$, $\overline{B}$, C_n	None	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{A}$, $\overline{B}$, C_n	None	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	None	C_{n+4}
t_{PLH}, t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	None	C_{n+4}
t_{PLH}, t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$, $\overline{B}$, C_n	None	C_{n+4}
t_{PLH}, t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{A}$, $\overline{B}$, C_n	None	C_{n+4}

Table 7. INPUT PAIRS HIGH/NOT HIGH TEST TABLE **Function Inputs:** S_2=M=4.5V, S_0=S_1=S_3=0V

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}, t_{PHL}	$\overline{A}_j$	$\overline{B}_j$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{B}_j$	$\overline{A}_j$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{P}$
t_{PLH}, t_{PHL}	$\overline{A}_j$	$\overline{B}_j$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	C_{n+4}
t_{PLH}, t_{PHL}	$\overline{B}_j$	$\overline{A}_j$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	C_{n+4}

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_K	Input clamp current				-18	mA
V_{OH}	High level output voltage	A=B only			4.5	V
I_{OH}	High-level output current	Any output except A=B			-1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
I_{OH}	High-level output current	A=B only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OH}	High-level output voltage	Any output except A=B	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	M	V_{CC} = MAX, V_I = 2.7V					20	µA
		$\overline{A}_0$-$\overline{A}_3$, $\overline{B}_0$-$\overline{B}_3$						60	µA
		S_0-S_3						80	µA
		C_n						120	µA
I_{IL}	Low-level input current	M	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		$\overline{A}_0$-$\overline{A}_3$, $\overline{B}_0$-$\overline{B}_3$						-1.8	mA
		S_0-S_3						-2.4	mA
		C_n						-3.6	mA
I_{OS}	Short circuit output current[3]	Any output except A=B	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current [total]	I_{CCH}	V_{CC} = MAX	S_0-S_3=M=$\overline{A}_0$-$\overline{A}_3$=4.5V, $\overline{B}_0$-$\overline{B}_3$=C_n=GND			48	65	mA
		I_{CCL}		S_0-S_3=M=4.5V, $\overline{B}_0$-$\overline{B}_3$=C_n=$\overline{A}_0$-$\overline{A}_3$=GND			48	65	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

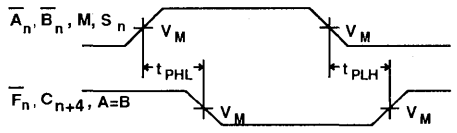
SYMBOL	PARAMETER	TEST CONDITIONS				LIMITS					UNIT
						T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
		Mode	Table	Wave form	Condition	Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}					2.0 2.0	5.0 6.5	7.5 8.5	2.0 2.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4}	Sum	3	1	$M=S_1=S_2=0V$, $S_0=S_3=4.5V$	5.5 5.5	10.0 8.5	13.0 13.0	5.0 5.0	14.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4}	Diff	4	4	$M=S_0=S_3=0V$, $S_1=S_2=4.5V$	5.5 5.5	10.5 9.0	14.0 13.0	5.0 5.0	15.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4} (status check)	Equality $\overline{A}_i=\overline{B}_i$ or $\overline{A}_i\neq\overline{B}_i$	6	1	$M=C_n=4.5V$ $S_0=S_3=4.5V$ $S_1=S_2=0V$	5.0 5.0	9.0 10.0	13.0 13.0	4.5 4.5	14.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4} (status check)	$\overline{A}_i=\overline{B}_i=H$ or $\overline{A}_i=\overline{B}_i=L$		1	$M=C_n=4.5V$, $S_2=4.5V$ $S_0=S_1=S_3=0V$	5.0 5.0	9.0 10.5	13.0 14.0	4.5 4.5	14.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}_n$		4	2		3.0 3.0	5.5 5.5	8.0 8.5	2.5 2.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	Sum	3	2	$M=S_1=S_2=0V$, $S_0=S_3=4.5V$	3.0 3.0	5.0 5.0	8.0 8.5	2.5 2.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	Diff	4	3	$M=S_0=S_3=0V$, $S_1=S_2=4.5V$	3.0 3.0	5.0 5.5	8.5 9.0	2.5 2.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	Sum	3	2	$M=S_1=S_2=0V$, $S_0=S_3=4.5V$	2.0 2.0	4.5 5.0	7.5 8.0	2.0 2.0	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	Diff	4	3	$M=S_0=S_3=0V$, $S_1=S_2=4.5V$	2.5 2.5	5.0 5.5	8.5 8.5	2.0 2.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$ (status check)	Equality $\overline{A}_i=\overline{B}_i$ or $\overline{A}_i\neq\overline{B}_i$	6	3	$M=C_n=0V$ $S_2=S_3=4.5V$	6.0 4.0	9.5 7.0	13.0 11.0	6.0 4.0	14.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$ (status check)	$\overline{A}_i=\overline{B}_i=H$ or $\overline{A}_i=\overline{B}_i=L$	7	3	$M=C_n=4.5V$, $S_2=4.5V$ $S_0=S_1=S_3=0V$	6.0 4.0	10.0 7.5	13.0 11.0	6.0 4.0	14.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Sum	3	2	$M=S_1=S_2=0V$ $S_0=S_3=4.5V$	2.0 3.0	4.5 5.5	7.5 8.5	2.0 3.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Diff	4	3	$M=S_0=S_3=0V$, $S_1=S_2=4.5V$	2.5 3.5	5.0 6.0	8.0 9.0	2.0 3.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Logic	5	3	M=4.5V	3.5 3.0	6.0 5.5	9.0 9.0	3.0 2.5	10.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to A=B	Diff	4	3	$M=S_0=S_3=0V$, $S_1=S_2=4.5V$	8.0 6.0	14.5 9.0	20.0 12.5	8.0 6.0	22.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}_n$	Sum		1 + 2		3.5 3.5	6.5 7.0	10.0 10.5	3.0 3.5	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}_n$	Diff		1 + 2		3.5 3.5	7.0 7.5	10.5 11.0	3.0 3.5	11.5 11.5	ns

NOTE: "$\overline{A}_n$ or $\overline{B}_n$ to F_n" means any $\overline{A}$ or any $\overline{B}$ to any $\overline{F}$ and "$\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$" means $\overline{A}_1$, $\overline{B}_1$ to $\overline{F}_1$; $\overline{A}_2$, $\overline{B}_2$ to $\overline{F}_2$ (the subscripts must be the same).

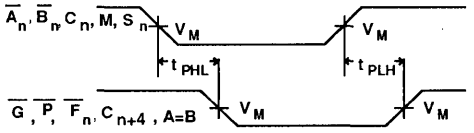
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
		Mode	Waveform	Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{F}_n$		1 + 2	2.5 3.0	6.0 6.5	10.0 10.5	2.0 3.0	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to A=B		1 + 2	12.0 5.5	16.5 9.0	22.0 13.0	11.0 5.0	24.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to C_{n+4}		1	4.0 4.0	10.0 7.5	12.5 10.0	4.0 4.0	14.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{G}$		2	3.0 3.0	5.0 5.0	8.0 8.0	2.5 2.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$		2	2.5 3.5	7.5 7.0	13.0 11.0	2.0 3.5	14.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_n$	Sum	1 + 2	3.0 3.0	7.0 6.5	9.5 9.5	3.0 3.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_n$	DIff	1 + 2	3.0 3.0	6.5 6.0	9.5 9.5	3.0 3.0	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay M to A=B	Sum	1 + 2	13.0 5.5	16.5 9.5	22.0 12.0	12.0 5.0	24.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay M to A=B	Diff	1 + 2	13.5 5.5	16.5 9.5	22.0 12.0	12.0 5.0	24.0 13.5	ns

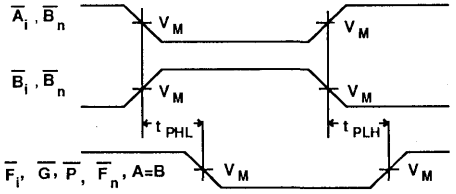
AC WAVEFORMS



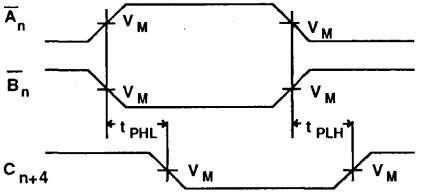
Waveform 1. Propagation Delay for Operands to Carry Output and Ouptuts



Waveform 2. Propagation Delay for Carry input to Carry output, Carry Input to Outputs, and Operands to Carry Generate and Carry Propagate Outputs



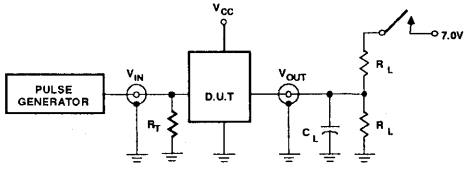
Waveform 3. Propagation Delay for Operands to Carry Generate and Propagate Outputs, Operands to A=B Output and Outputs



Waveform 4. Propagation Delay for Operands to Carry Output

NOTE: For all waveforms, $V_M = 1.5V$

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs

SWITCH POSITION

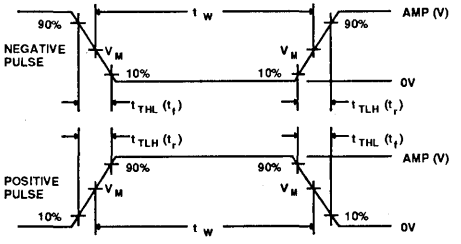
TEST	SWITCH
Open Collector	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F882
Look-Ahead Carry Generator

FAST Products

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F882	4.0ns	20mA

FEATURES

- **Capable of anticipating the carry across a group of eight 4-bit binary adders**
- **Cascadable to perform look-ahead across n-bit adders**
- **Typical carry time, C_n to any C_{n+l} is less than 6ns**
- **Replaces AS882**
- **Available in 300 mil-wide Slim 24 pin Dip package**

DESCRIPTION

The 74F882 is a high speed carry look-ahead generator capable of anticipating the carry across a group of eight 4-bit adders, thereby permitting the designer to implement look-ahead for a 32-bit ALU with a single package. In addition, full look-ahead is possible across n-bit adders cascading 'F882's.

ORDERING INFORMATION

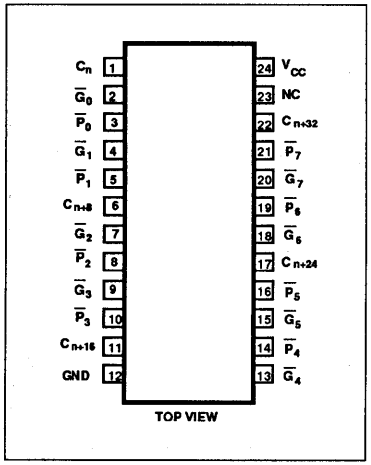
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300 mil)	N74F882N
24-Pin Plastic SOL	N74F882D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

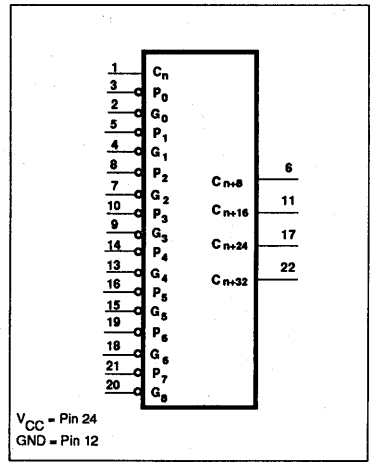
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
C_n	Carry input	1.0/1.0	20µA/0.6mA
$\overline{G}_0$, $\overline{G}_4$	Carry generate inputs	1.0/7.0	20µA/4.2mA
$\overline{G}_1$, $\overline{G}_2$	Carry generate inputs	1.0/9.0	20µA/5.4mA
$\overline{G}_3$	Carry generate input	1.0/10.0	20µA/6.0mA
$\overline{G}_5$	Carry generate input	1.0/8.0	20µA/4.8mA
$\overline{G}_6$	Carry generate input	1.0/2.0	20µA/1.2mA
$\overline{G}_7$	Carry generate input	1.0/3.0	20µA/1.8mA
$\overline{P}_0$, $\overline{P}_1$	Carry generate inputs	1.0/4.0	20µA/2.4mA
$\overline{P}_2$, $\overline{P}_3$	Carry propagate inputs	1.0/2.0	20µA/1.2mA
$\overline{P}_4$, $\overline{P}_5$, $\overline{P}_6$, $\overline{P}_7$	Carry propagate inputs	1.0/1.0	20µA/0.6mA
C_{n+8}	Carry output	50/33	1.0mA/20mA
C_{n+16}	Carry output	50/33	1.0mA/20mA
C_{n+24}	Carry output	50/33	1.0mA/20mA
C_{n+32}	Carry output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

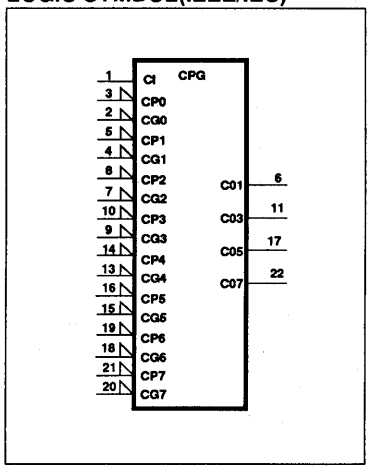
PIN CONFIGURATION



LOGIC SYMBOL

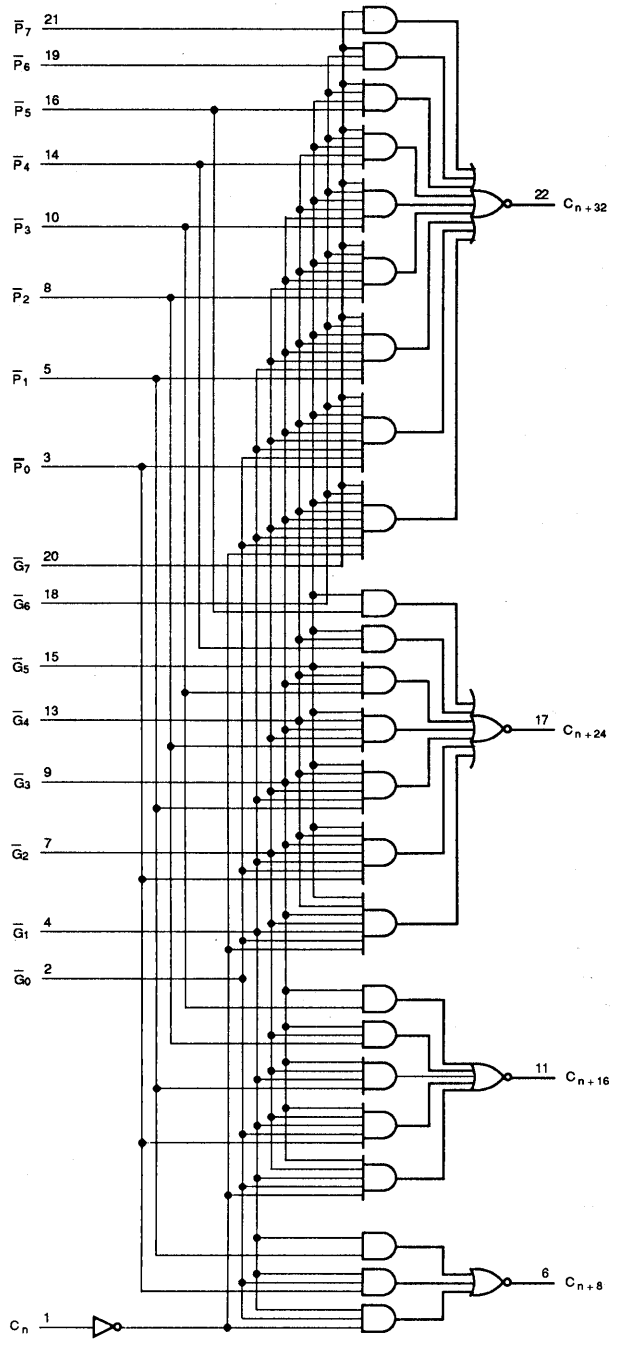


LOGIC SYMBOL(IEEE/IEC)



Look-Ahead Carry Generator | FAST 74F882

LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12

FUNCTION TABLE for C_{n+32} OUTPUT

INPUTS																	OUTPUT
$\overline{G}_7$	$\overline{G}_6$	$\overline{G}_5$	$\overline{G}_4$	$\overline{G}_3$	$\overline{G}_2$	$\overline{G}_1$	$\overline{G}_0$	$\overline{P}_7$	$\overline{P}_6$	$\overline{P}_5$	$\overline{P}$	$\overline{P}_3$	$\overline{P}_2$	$\overline{P}_1$	$\overline{P}_0$	C_n	C_{n+32}
L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	L	L	X	X	X	X	X	X	X	H
X	X	X	L	X	X	X	X	L	L	L	X	X	X	X	X	X	H
X	X	X	X	L	X	X	X	L	L	L	L	X	X	X	X	X	H
X	X	X	X	X	L	X	X	L	L	L	L	L	X	X	X	X	H
X	X	X	X	X	X	L	X	L	L	L	L	L	L	X	X	X	H
X	X	X	X	X	X	X	L	L	L	L	L	L	L	L	X	X	H
X	X	X	X	X	X	X	X	L	L	L	L	L	L	L	L	H	H
All other combinations																	L

FUNCTION TABLE for C_{n+24} OUTPUT

INPUTS													OUTPUT
$\overline{G}_5$	$\overline{G}_4$	$\overline{G}_3$	$\overline{G}_2$	$\overline{G}_1$	$\overline{G}_0$	$\overline{P}_5$	$\overline{P}_4$	$\overline{P}_3$	$\overline{P}_2$	$\overline{P}_1$	$\overline{P}_0$	C_n	C_{n+24}
L	X	X	X	X	X	X	X	X	X	X	X	X	H
X	L	X	X	X	X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	L	L	X	X	X	X	X	H
X	X	X	L	X	X	L	L	L	X	X	X	X	H
X	X	X	X	L	X	L	L	L	L	X	X	X	H
X	X	X	X	X	L	L	L	L	L	L	X	X	H
X	X	X	X	X	X	L	L	L	L	L	L	H	H
All other combinations													L

FUNCTION TABLE for C_{n+16} OUTPUT

INPUTS									OUTPUT
$\overline{G}_3$	$\overline{G}_2$	$\overline{G}_1$	$\overline{G}_0$	$\overline{P}_3$	$\overline{P}_2$	$\overline{P}_1$	$\overline{P}_0$	C_n	C_{n+16}
L	X	X	X	X	X	X	X	X	H
X	L	X	X	L	X	X	X	X	H
X	X	L	X	L	L	X	X	X	H
X	X	X	L	L	L	L	X	X	H
X	X	X	X	L	L	L	L	H	H
All other combinations									L

FUNCTION TABLE for C_{n+8} OUTPUT

INPUTS					OUTPUT
$\overline{G}_1$	$\overline{G}_0$	$\overline{P}_1$	$\overline{P}_0$	C_n	C_{n+8}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

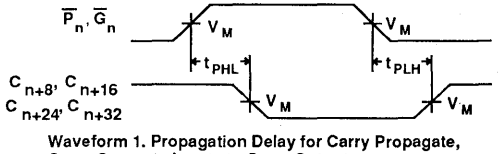
SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	C_n, $\overline{P}_4$, $\overline{P}_5$, $\overline{P}_6$, $\overline{P}_7$	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
		$\overline{G}_0$, $\overline{G}_4$						-4.2	mA
		$\overline{G}_1$, $\overline{G}_2$						-5.4	mA
		$\overline{G}_3$						-6.0	mA
		$\overline{G}_5$						-4.8	mA
		$\overline{G}_6$, $\overline{P}_2$, $\overline{P}_3$						-1.2	mA
		$\overline{G}_7$						-1.8	mA
		$\overline{P}_0$, $\overline{P}_1$						-2.4	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				15	25	mA
		I_{CCL}					23	35	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

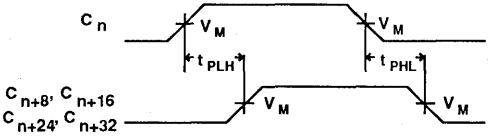
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to Any output	Waveform 2	2.5 3.0	5.0 5.5	8.5 9.5	2.0 3.0	9.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{P}_n$ or $\overline{G}_n$ to C_{n+8}	Waveform 1	1.0 1.0	3.5 2.5	6.0 5.5	1.0 1.0	7.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{P}_n$ or $\overline{G}_n$ to C_{n+16}	Waveform 1	2.0 1.0	4.0 2.5	7.0 6.0	2.0 1.0	8.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{P}_n$ or $\overline{G}_n$ to C_{n+24}	Waveform 1	2.0 2.0	4.0 4.0	7.5 7.5	1.5 1.5	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{P}_n$ or $\overline{G}_n$ to C_{n+32}	Waveform 1	1.5 1.0	4.5 4.5	8.0 8.0	1.0 1.0	8.5 8.5	ns

AC WAVEFORMS



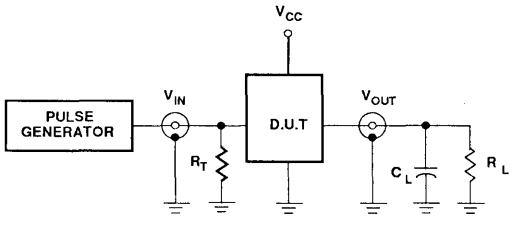
Waveform 1. Propagation Delay for Carry Propagate, Carry Generate Inputs to Carry Outputs



Waveform 2. Propagation Delay for Carry input to Carry outputs

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



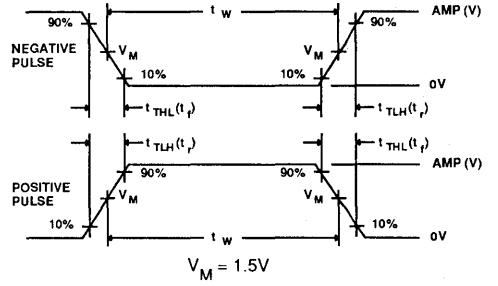
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F899

Dual Latch Transceiver with Parity

FAST Products

9-Bit Dual Latch Transceiver With 8-bit Parity Generator/Checker (3-State Outputs)
Preliminary Specification

FEATURES

- **Combines 'F543 and 'F280 functions into one package**
- **Combines 'F657 and 'F373 functions into one package (No need to change T/$\overline{R}$ to check parity)**
- **Output sink of 24 mA for the A-Bus and 64 mA for the B-bus**
- **Symmetrical (A and B bus functions are identical)**
- **Selectable generate parity or "feed-through" parity for A-to-B and B-to-A directions**
- **Independant transparent latches for A-to-B and B-to-A directions**
- **Selectable ODD/$\overline{EVEN}$ parity**
- **Continously checks parity of both A bus and B bus latches as $\overline{ERRA}$ and $\overline{ERRB}$**
- **Ability to simultaneously generate and check parity**
- **Can simultaneously read/latch A and B bus data**

TYPE	TYPICAL PROPAGATION DELAY	MAX SUPPLY CURRENT (TOTAL)
74F899	8.0ns	150mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP (600mil)	N74F899N
28-Pin PLCC	N74F899A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

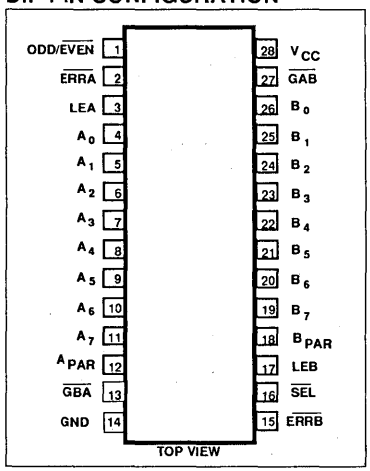
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	Latched A bus 3-State inputs	3.5/0.117	70µA/70µA
B_0 - B_7	Latched B bus 3-State inputs	3.5/0.117	70µA/70µA
A_{PAR}	A bus parity 3-State input	1.0/0.033	20µA/20µA
B_{PAR}	B bus parity 3-State input	1.0/0.033	20µA/20µA
ODD/$\overline{EVEN}$	Parity Select Input (Low for EVEN parity)	1.0/0.033	20µA/20µA
$\overline{GBA}$,$\overline{GAB}$	Output Enable Inputs (Gate A to B, B to A)	2.0/0.066	40µA/40µA
$\overline{SEL}$	Mode Select Input (Low for generate)	1.0/0.033	20µA/20µA
LEA,LEB	Latch Enable Inputs (Low for latch)	1.0/0.033	20µA/20µA
$\overline{ERRA}$, $\overline{ERRB}$	Error Signal Outputs (active Low)	150/40	3mA/24mA
A_0 - A_7	A bus 3-State outputs	150/40	3mA/24mA
B_0 - B_7	B bus 3-State outputs	750/106.7	15mA/64mA
A_{PAR}	A bus parity 3-State output	150/40	3mA/24mA
B_{PAR}	B bus parity 3-State output	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

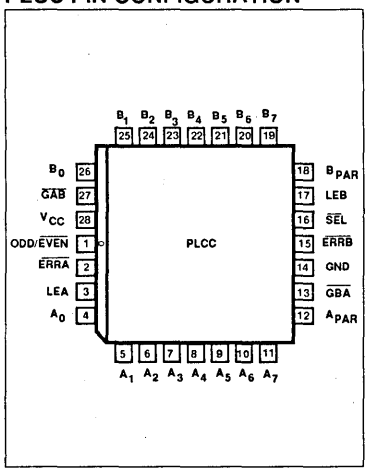
DESCRIPTION

The 'F899 is a 9-bit to 9-bit parity transceiver with separate transparent latches for the A bus and B bus. Either bus can generate or check parity. The parity bit can be fed-through with no change or the generated parity can be substituted with the $\overline{SEL}$ input. Parity error checking of the

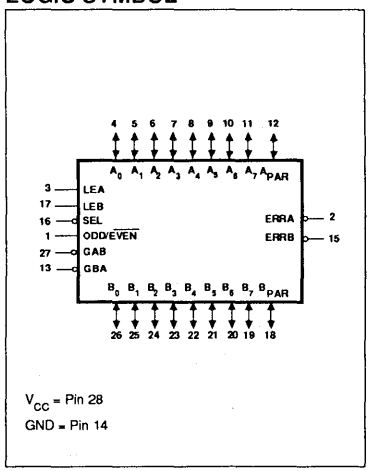
DIP PIN CONFIGURATION



PLCC PIN CONFIGURATION



LOGIC SYMBOL



V_{CC} = Pin 28
GND = Pin 14

A and B bus latches is continuously provided with $\overline{ERRA}$ and $\overline{ERRB}$, even with both buses in 3-State.
The device has a guaranteed current sinking capability of 24 mA for the A-bus and 64 mA for the B-bus. Otherwise, the part is symmetrical (A and B bus functions are identical).

The 'F899 features independent latch enables for the A and B bus latches, a select pin for ODD/$\overline{EVEN}$ parity, and separate error signal output pins for checking parity.

FUNCTIONAL DESCRIPTION:

The 'F899 has three principal modes of operation which are outlined below. All modes apply to both the A-to-B and B-to-A directions.

Transparent latch, Generate parity, Check A and B bus parity:

Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as B_{PAR} (A_{PAR}). If LEA and LEB are High and the Mode Select ($\overline{SEL}$) is Low, the parity generated from A_0-A_7 and B_0-B_7 can be checked and monitored by $\overline{ERRA}$ and $\overline{ERRB}$. (Fault detection on both input and output buses.)

Transparent latch, Feed-through parity, Check A and B bus parity:

Bus A (B) communicates to Bus B (A) in a feed-through mode if $\overline{SEL}$ is High. Parity is still generated and checked as $\overline{ERRA}$ and $\overline{ERRB}$ and can be used as an interrupt to signal a data/parity bit error to the CPU.

Latched input, Generate/Feed-through parity, Check A (and B) bus parity:

Independent latch enables (LEA and LEB) allow other permutations of:

Transparent latch / 1bus latched / both busses latched
Feed-through parity / generate parity
Check in bus parity / check out bus parity / check in and out bus parity

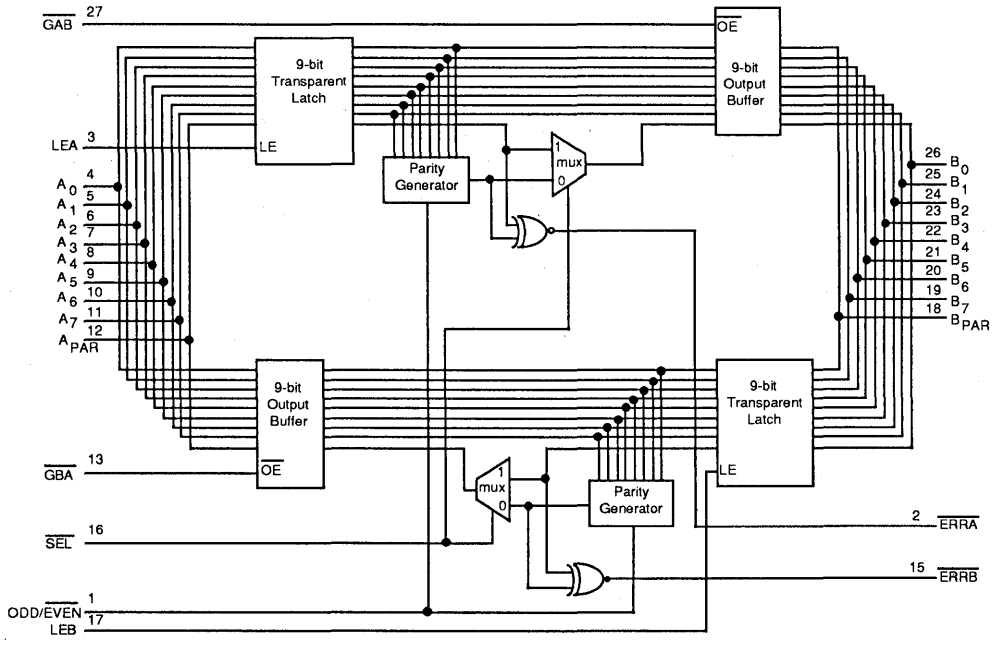
See function table below.

FUNCTION TABLE

INPUTS					OPERATING MODE
$\overline{GAB}$	$\overline{GBA}$	$\overline{SEL}$	LEA	LEB	
H	H	X	X	X	3-state A bus and B bus (Input A & B simultaneously)
H	L	L	L	H	B → A, Transparent B latch, Generate parity from B_0-B_7, Check B bus parity
H	L	L	H	H	B → A, Transparent A & B latch, Generate parity from B_0-B_7, Check A & B bus parity
H	L	L	X	L	B → A, B bus latched, Generate parity from latched B_0-B_7 data, Check B bus parity
H	L	H	X	H	B → A, Transparent B latch, Parity feed-through, Check B bus parity
H	L	H	H	H	B → A, Transparent A & B latch, Parity feed-through, Check A & B bus parity
L	H	L	H	X	A → B, Transparent A latch, Generate parity from A_0-A_7, Check A bus parity
L	H	L	H	H	A → B, Transparent A & B latch, Generate parity from A_0-A_7, Check A & B bus parity
L	H	L	L	X	A → B, A bus latched, Generate parity from latched A_0-A_7 data, Check A bus parity
L	H	H	H	L	A → B, Transparent A latch, Parity feed-through, Check A bus parity
L	H	H	H	H	A → B, Transparent A & B latch, Parity feed-through, Check A & B bus parity
L	L	X	X	X	Output to A bus and B bus (NOT ALLOWED)

H = High voltage level
L = Low voltage level
X = Don't care

BLOCK DIAGRAM



V_{CC} = Pin 28
GND = Pin 14

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A_0 - A_7, A_{PAR}, $\overline{ERRA}$, $\overline{ERRB}$	48	mA
		B_0 - B_7, B_{PAR}	128	
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0 - A_7			-3	mA
		B_0 - B_7			-15	
I_{OL}	Low-level output current	A_0 - A_7			24	mA
		B_0 - B_7			64	
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	All outputs	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		B_0-B_7, B_{PAR}		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7, A_{PAR}, $\overline{ERRA}$, $\overline{ERRB}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7, B_{PAR}		I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	Other Inputs	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_0-A_7, A_{PAR}	V_{CC} = MAX, V_I = 5.5V					2.0	mA
		B_0-B_7, B_{PAR}						1.0	mA
I_{IH}	High-level input current	ODD/$\overline{EVEN}$, $\overline{SEL}$, LEA, LEB	V_{CC} = MAX, V_I = 2.7V					20	µA
		$\overline{GAB}$, $\overline{GBA}$						40	µA
I_{IL}	Low-level input current	ODD/$\overline{EVEN}$, $\overline{SEL}$, LEA, LEB	V_{CC} = MAX, V_I = 0.5V					-20	µA
		$\overline{GAB}$, $\overline{GBA}$						-40	µA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied	A_0-A_7, A_{PAR} B_0-B_7, B_{PAR}	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-70	µA
I_{OZH}	Off-state output current High-level voltage applied	ODD/$\overline{EVEN}$, $\overline{SEL}$, LEA, LEB, $\overline{GAB}$, $\overline{GBA}$	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]	A_0-A_7, A_{PAR}	V_{CC} = MAX			-60		-150	mA
		B_0-B_7, B_{PAR}				-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				90	125	mA
		I_{CCL}					106	150	mA
		I_{CCZ}					98	145	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

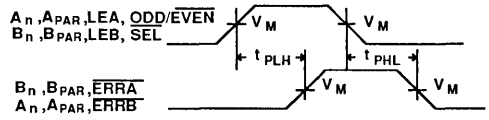
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay (Transparent latch) A_n to B_n or B_n to A_n	Waveform 1		8.0 8.0		5.0 5.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay (Feed-through Parity) A_{PAR} to B_{PAR} or B_{PAR} to A_{PAR}	Waveform 1		8.0 8.0		5.0 5.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay (Generate Parity) A_n, A_{PAR} to B_{PAR} or B_n, B_{PAR} to A_{PAR}	Waveform 1		10.0 10.0		8.0 8.0	15.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay (Check Parity) A_n, A_{PAR} to $\overline{ERRA}$ or B_n, B_{PAR} to $\overline{ERRB}$	Waveform 1		10.0 10.0		8.0 8.0	15.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{EVEN}$ to $\overline{ERRA}$, $\overline{ERRB}$, A_{PAR}, or B_{PAR}	Waveform 1		10.0 10.0		8.0 8.0	15.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay SEL to A_{PAR}, B_{PAR}	Waveform 1		8.0 8.0		5.0 5.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay LEA to B_n, B_{PAR} or LEB to A_n, A_{PAR}	Waveform 1		8.0 8.0		5.0 5.0	12.0 12.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{GBA}$ to A_n, A_{PAR} or $\overline{GAB}$ to B_n, B_{PAR}	Waveform 3, 4		10.0 10.0		8.0 8.0	15.0 15.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{GBA}$ to A_n, A_{PAR} or $\overline{GAB}$ to B_n, B_{PAR}	Waveform 3, 4		10.0 10.0		8.0 8.0	15.0 15.0	ns

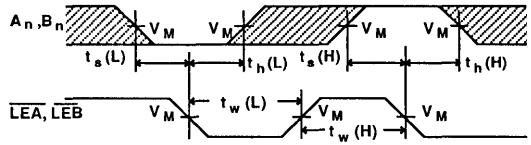
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Set-up time A_n to LEA or B_n to LEB	Waveform 2	3.0 3.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time A_n to LEA or B_n to LEB	Waveform 2	0.0 0.0			0.0 0.0		ns
t_w(H) t_w(L)	Pulse width LEA or LEB	Waveform 2	5.0 5.0			5.0 5.0		ns

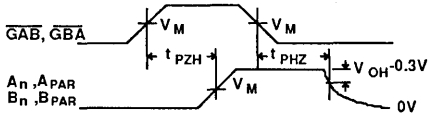
AC WAVEFORMS



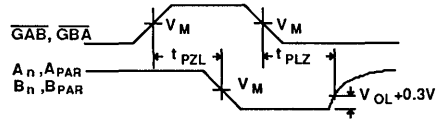
Waveform 1. Propagation Delay For Input To Output



Waveform 2. Data Setup And Hold Times And LEA, LEB Pulse Widths



Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level

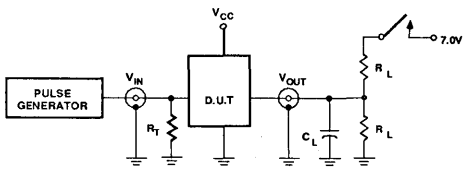


Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

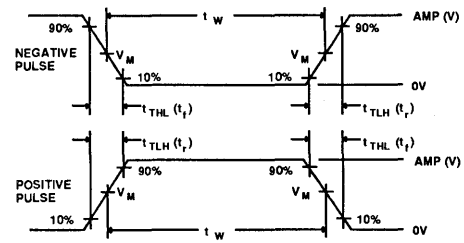
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F1240, 74F1241 Buffers

FAST Products

74F1240 Octal Inverter Buffer (3-State)
74F1241 Octal Buffer (3-State)
Product Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Low power, light loading**
- **Functional pin for pin equivalent of 'F240 and 'F241**
- **1/30th the bus loading of 'F240 and 'F241**
- **Provides ideal interface and increase fan-out of MOS Microprocessors**
- **Octal bus interface**
- **3-State buffer outputs sink 64mA**
- **15mA source current**

DESCRIPTION

The 74F1240 and 74F1241 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}_n$, each controlling four of the 3-state outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1240	3.5ns	40mA
74F1241	4.5ns	46mA

ORDERING INFORMATION

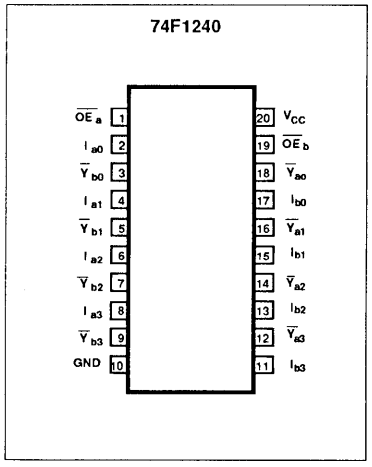
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F1240N, N74F1241N
20-Pin Plastic SOL	N74F1240D, N74F1241D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

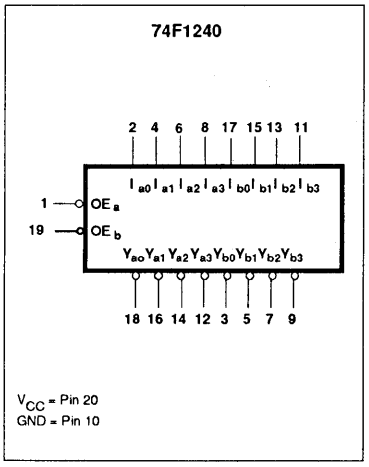
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{an}, I_{bn}	Data inputs	1.0/0.033	20μA/20μA
I_{an}, I_{bn}	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_a$, $\overline{OE}_b$	Output enable input (active Low)	1.0/0.033	20μA/20μA
OE_b	Output enable input (active High, 'F1241)	1.0/0.033	20μA/20μA
Y_{an}, Y_{bn}	Data outputs ('F1241)	750/106.7	15mA/64mA
$\overline{Y}_{an}$, $\overline{Y}_{bn}$	Data outputs ('F1240)	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

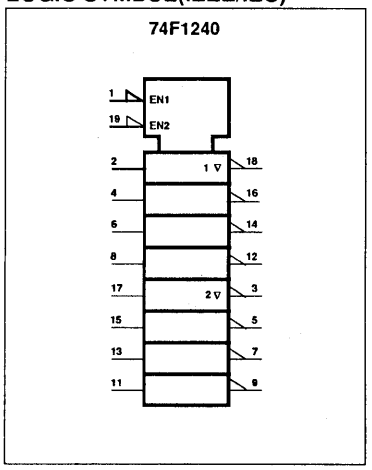
PIN CONFIGURATION



LOGIC SYMBOL

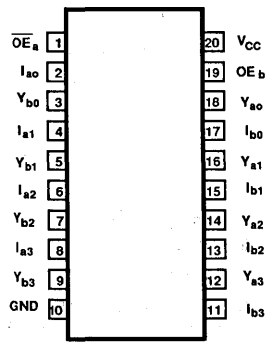


LOGIC SYMBOL(IEEE/IEC)



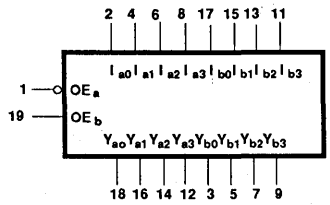
PIN CONFIGURATION

74F1241



LOGIC SYMBOL

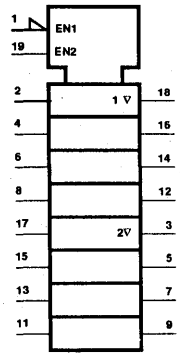
74F1241



V_{CC} = Pin 20
GND = Pin 10

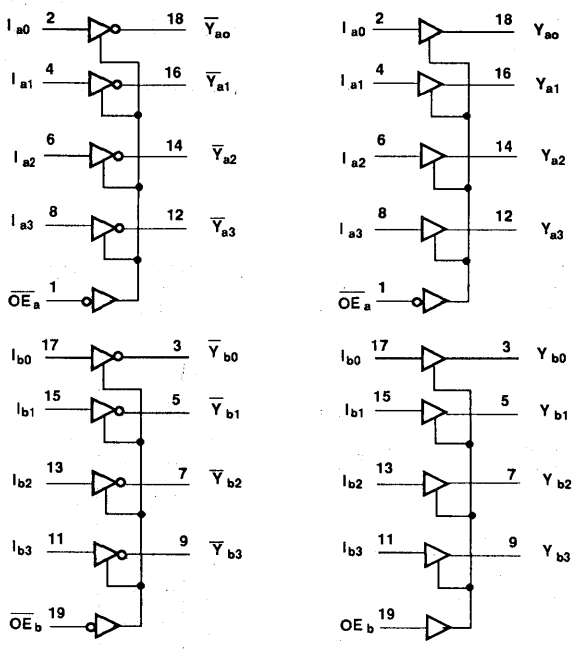
LOGIC SYMBOL(IEEE/IEC)

74F1241



LOGIC DIAGRAM

74F1240 | 74F1241



V_{CC} = Pin 20
GND = Pin 10

FUNCTION TABLE, 74F1240

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_a$	$\overline{Y}_b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

FUNCTION TABLE, 74F1241

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_a	Y_b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

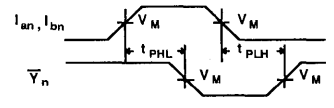
SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3mA	±10% V_{CC}	2.4			V
				±5% V_{CC}	2.7	3.3		V
			I_{OH} = -15mA	±10% V_{CC}	2.0			V
				±5% V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48mA	±10% V_{CC}		0.38	0.55	V
			I_{OL} = 64mA	±5% V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V					-20	µA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	74F1240	I_{CCH}	V_{CC} = MAX		22	30	mA
			I_{CCL}			58	75	mA
			I_{CCZ}			44	58	mA
		74F1241	I_{CCH}	V_{CC} = MAX		33	44	mA
			I_{CCL}			62	80	mA
			I_{CCZ}			45	60	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

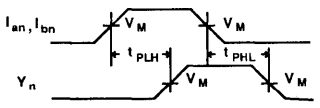
AC CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to $\overline{Y}_n$	74F1240	Waveform 1	3.0 1.5	4.5 2.5	6.5 4.5	2.5 1.5	7.5 5.0	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	74F1240	Waveform 3 Waveform 4	3.0 4.0	5.5 7.0	7.5 9.0	3.0 4.0	8.0 9.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	74F1240	Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 5.5	2.0 2.0	6.5 6.0	ns ns
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to Y_n	74F1241	Waveform 2	2.5 2.5	4.0 5.0	5.5 6.5	2.5 2.5	6.0 7.0	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	74F1241	Waveform 3 Waveform 4	3.0 3.0	5.5 6.5	7.0 8.0	3.0 3.0	7.5 8.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	74F1241	Waveform 3 Waveform 4	3.0 3.0	5.5 6.0	7.5 8.0	3.0 3.0	8.5 8.5	ns ns

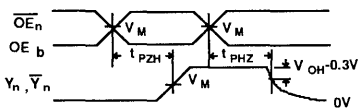
AC WAVEFORMS



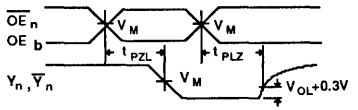
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



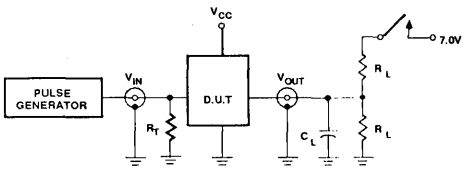
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

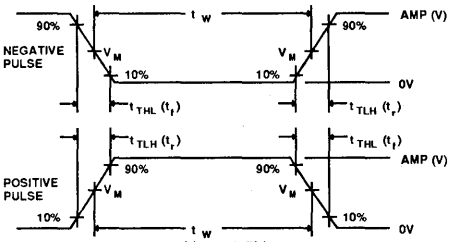
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F1242, 74F1243 Transceivers

FAST Products

74F1242 Quad Transceiver, Inverting (3-State)
74F1243 Quad Transceiver (3-State)

Product Specification

FEATURES

- High impedance NPN base inputs for reduced loading (70µA in High and Low states)
- Low power, light-bus loading
- Functional pin for pin equivalent of 'F242 and 'F243
- 1/30th the bus loading of 'F242 and 'F243
- Provides ideal interface and increases fan-out of MOS Microprocessors
- 3-State buffer outputs sink 64mA and source 15mA

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1242	3.5ns	43mA
74F1243	4.5ns	44mA

ORDERING INFORMATION

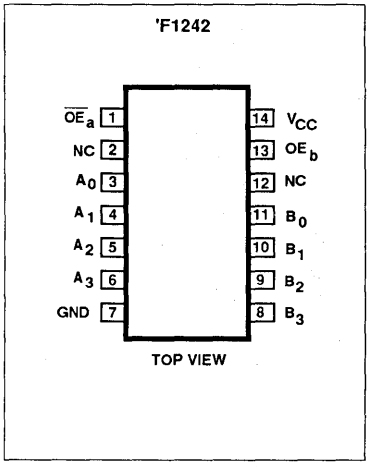
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F1242N, N74F1243N
14-Pin Plastic SO	N74F1242D, N74F1243D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

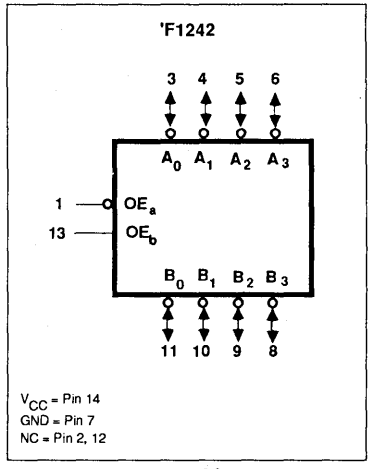
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_n, B_n	Data inputs	3.5/0.117	70µA/70µA
$\overline{OE}_a$	Output Enable input (active Low)	1.0/0.033	20µA/20µA
OE_b	Output Enable input	1.0/0.033	20µA/20µA
A_n, B_n	Data outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

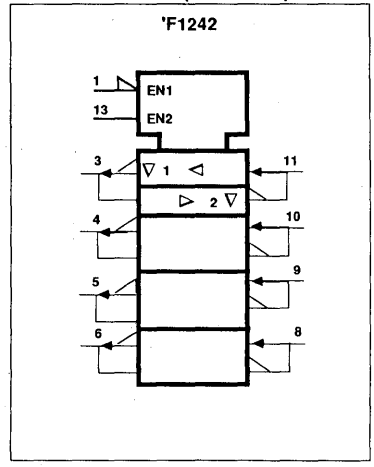
PIN CONFIGURATION



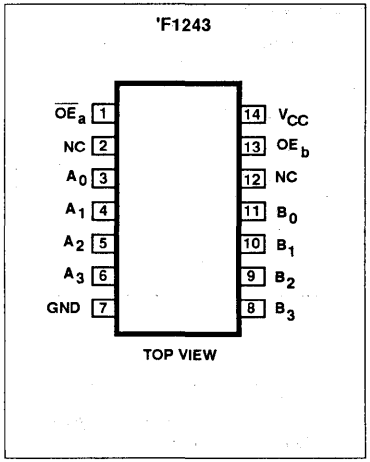
LOGIC SYMBOL



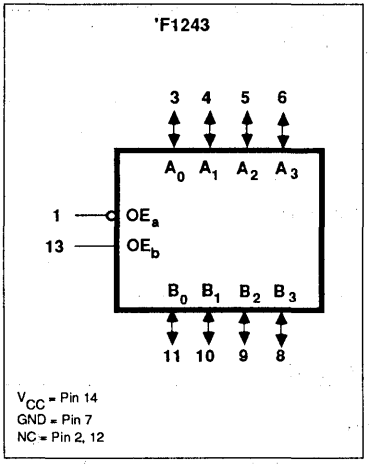
LOGIC SYMBOL(IEEE/IEC)



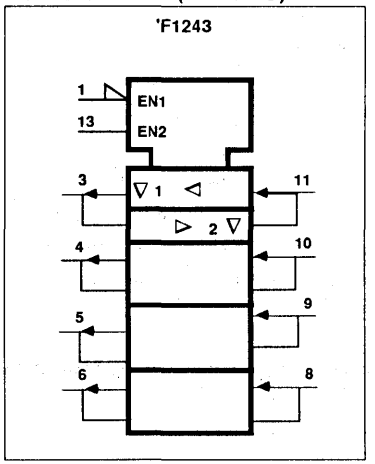
PIN CONFIGURATION



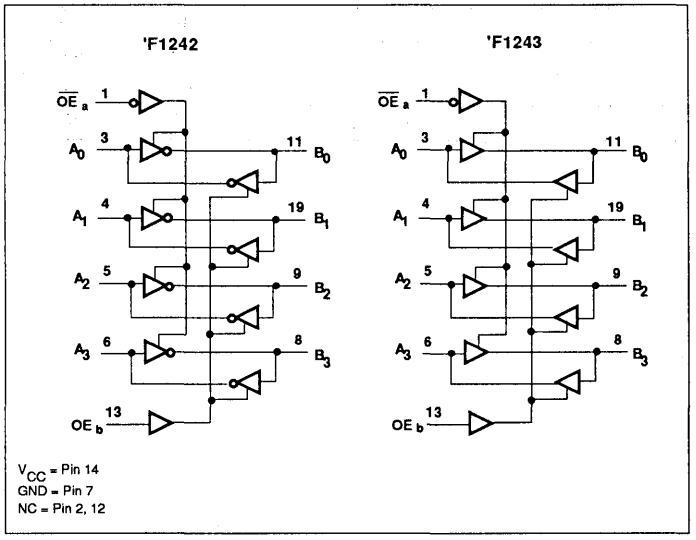
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE, 'F1242

INPUTS		OUTPUTS	
$\overline{OE}_a$	OE_b	A_n	B_n
L	L	INPUT	$B=\overline{A}$
H	L	Z	Z
L	H	a	a
H	H	$A=\overline{B}$	INPUT

FUNCTION TABLE, 'F1243

INPUTS		OUTPUTS	
$\overline{OE}_a$	OE_b	A_n	B_n
L	L	INPUT	B=A
H	L	Z	Z
L	H	a	a
H	H	A=B	INPUT

H = High voltage level
L = Low voltage level
Z = High impedance "off" state
a = This condition is not allowed due to excessive currents

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

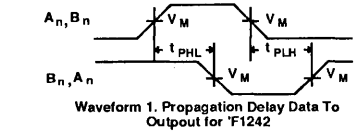
SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	A_0-A_3, B_0-B_3	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
		$\overline{OE}_a$, OE_b	V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	$\overline{OE}_a$, OE_b only	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{IH}+I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-70	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total)	'F1242 I_{CCH}	V_{CC} = MAX				35	46	mA
		'F1242 I_{CCL}					50	72	mA
		'F1242 I_{CCZ}					45	60	mA
		'F1243 I_{CCH}	V_{CC} = MAX				40	50	mA
		'F1243 I_{CCL}					52	65	mA
		'F1243 I_{CCZ}					44	60	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

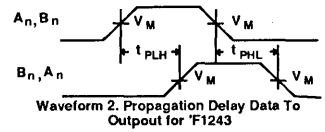
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to B_n, A_n	'F1242	Waveform 1	3.0 1.5	4.5 2.5	6.0 4.0	3.0 1.5	6.5 4.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	3.5 3.0	5.5 5.5	7.5 7.5	3.0 3.0	8.0 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 3 Waveform 4	3.5 3.0	6.0 5.0	8.0 7.5	3.5 3.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to B_n, A_n	'F1243	Waveform 2	2.0 3.0	4.0 5.0	5.5 6.5	2.0 3.0	6.0 7.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level		Waveform 3 Waveform 4	2.5 2.5	5.5 5.0	8.0 7.5	2.5 2.5	8.5 8.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 3 Waveform 4	3.5 2.0	6.5 5.0	8.5 7.5	3.0 2.0	9.0 8.0	ns

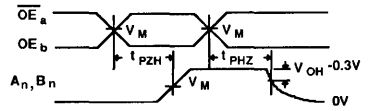
AC WAVEFORMS



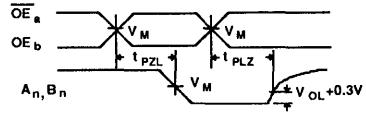
Waveform 1. Propagation Delay Data To Outpout for 'F1242



Waveform 2. Propagation Delay Data To Outpout for 'F1243



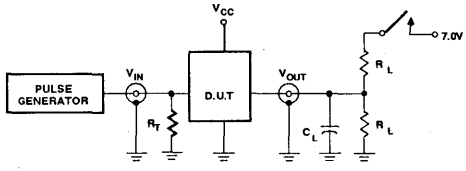
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

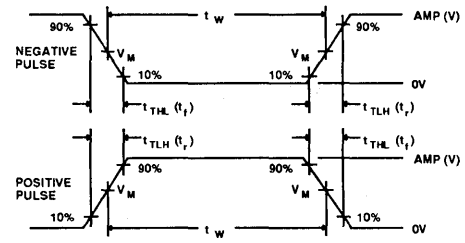
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F1244
Buffer

FAST Products

74F1244 Octal Buffer (3-State)

Product Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Low power, light loading**
- **Functional pin for pin equivalent of 'F244**
- **1/30th the bus loading of 'F244**
- **Provides ideal interface and increase fan-out of MOS Microprocessors**
- **Octal bus interface**
- **3-State buffer outputs sink 64mA and source 15mA**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1244	4.5ns	43mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F1244N
20-Pin Plastic SOL	N74F1244D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{an}, I_{bn}	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_a$, $\overline{OE}_b$	Output Enable inputs (active Low)	1.0/0.033	20μA/20μA
Y_{an}, Y_{bn}	Data outputs	750/106.7	15mA/64mA

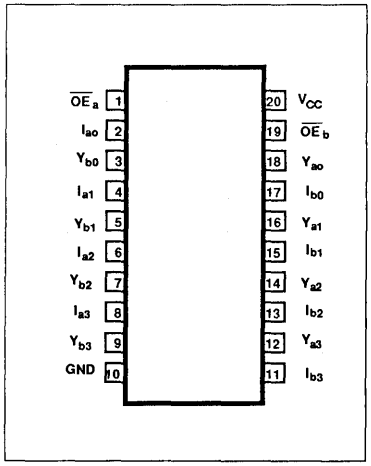
NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

DESCRIPTION

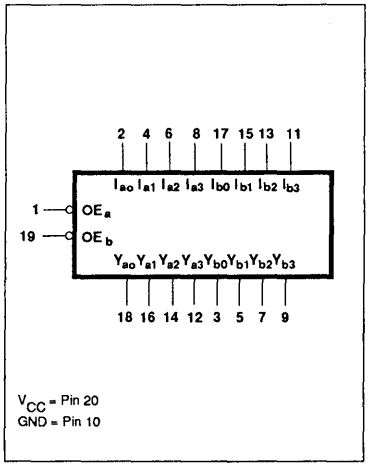
The 74F1244 is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}_a$ and $\overline{OE}_b$, each controlling four of the 3-state outputs.

The 'F1244 is pin and functional compatible with the 'F244. The lower power and light bus loading features make it an ideal part to interface directly with MOS Microprocessors.

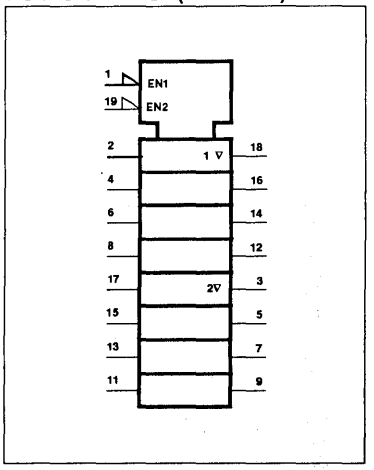
PIN CONFIGURATION



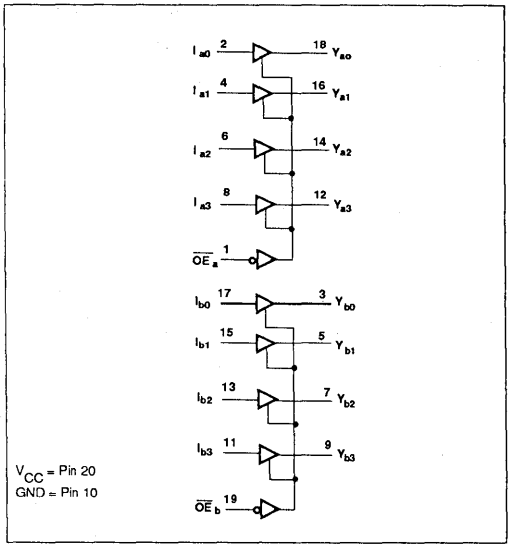
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

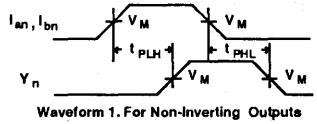
SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH}=-15mA	±10%V_{CC}	2.0			V
				±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX V_{IH} = MIN,	I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
			I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = MAX, V_O = 0.5V					-50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-100		-225	mA
I_{CC}	Supply current (total) I_{CCH}	V_{CC} = MAX				30	40	mA
	I_{CCL}					57	75	mA
	I_{CCZ}					43	58	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

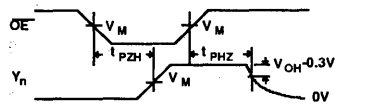
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_{an}, I_{bn} to Y_n	Waveform 1	2.5 2.0	4.0 5.0	5.5 7.0	2.5 2.0	6.0 7.5	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2 Waveform 3	3.0 3.0	6.0 6.5	7.5 8.0	3.0 3.0	8.5 8.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 2 Waveform 3	2.0 2.0	4.0 4.0	5.5 5.5	2.0 2.0	6.0 6.0	ns ns

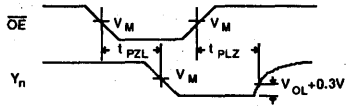
AC WAVEFORMS



Waveform 1. For Non-Inverting Outputs



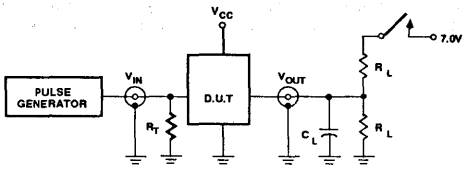
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

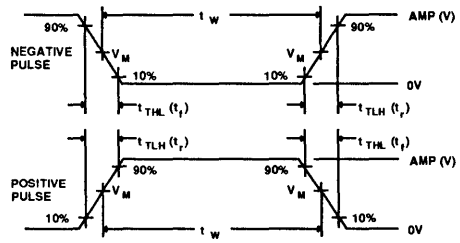
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

FAST 74F1245
Transceiver

FAST Products

FEATURES

- **Same function and pinout as 74F245**
- **High impedance NPN base inputs for reduced loading (70μA in Low and High states)**
- **Useful in applications where light loading bus loading or direct interface with output of a MOS microprocessor is desired**
- **Octal bidirectional bus interface**
- **Glitch free during 3-state power up and power down**
- **3-state buffer outputs sink 64mA and source 15mA**

DESCRIPTION

The 74F1245 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both transmit and receive directions. The B port outputs are capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features an Output Enable ($\overline{OE}$) input for easy cascading and Transmit/Receive($T/\overline{R}$) input for direction control. The 3-state outputs, B_0-B_7, have been designed to prevent output bus loading if the power is removed from the device.

Octal Transceiver (3-State)
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1245	5.0ns	115mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F1245N
20-Pin Plastic SOL[1]	N74F1245D

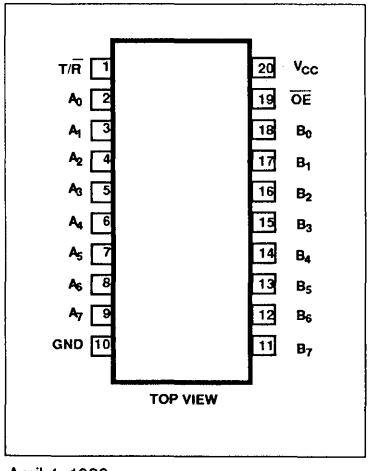
NOTE:
1. Thermal mounting technique are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

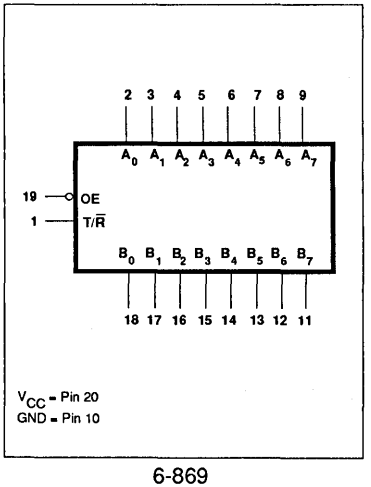
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7, B_0- B_7	A and B port inputs	3.5/0.117	70μA/70μA
$\overline{OE}$	Output Enable input (active Low)	2.0/0.033	40μA/20μA
$T/\overline{R}$	Transmit/Receive input	2.0/0.033	40μA/20μA
A_0- A_7	A port outputs	150/40	3.0mA/24mA
B_0- B_7	B Port outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

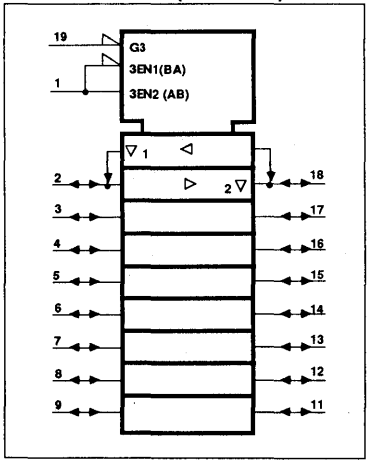
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)

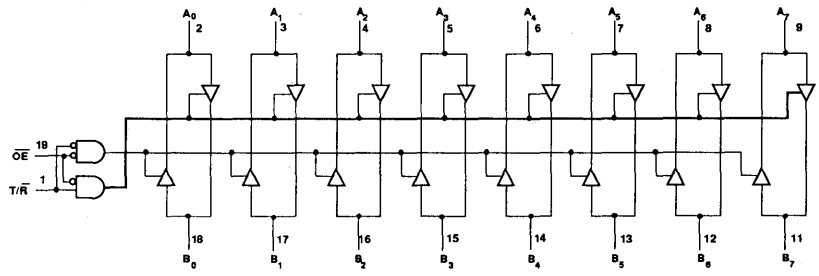


FUNCTION TABLE

INTPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	T/$\overline{R}$	A_n	B_n
L	L	A=B	INPUTS
L	H	INPUTS	B=A
H	X	Z	Z

H=High voltage level
L=Low voltage level
X=Don't care
Z=High impedance "off " state

LOGIC DIAGRAM



V_{CC}=pin 20
GND=pin 10

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0-B_7			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

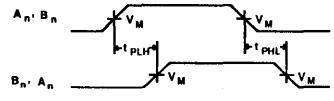
SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	A_0-A_7, B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
		B_0-B_7		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=48mA	±10%V_{CC}		0.30	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$	V_{CC} = 5.5V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
I_{IH}	High-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 2.7V					40	µA
I_{IL}	Low-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = MAX, V_O= 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-70	µA
I_{OS}	Short-circuit output current[3]	A_0-A_7	V_{CC} = MAX			-60		-150	mA
		B_0-B_7				-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				120	155	mA
		I_{CCL}					116	150	mA
		I_{CCZ}					110	165	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

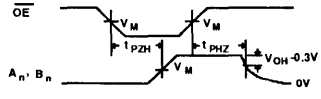
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, B_n to A_n	Waveform 1	2.0 2.5	4.0 5.0	6.5 7.5	1.5 2.0	7.0 8.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 2 Waveform 3	3.0 4.0	6.0 7.5	8.0 10.0	2.5 3.5	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 2 Waveform 3	2.0 4.0	5.0 7.0	8.0 10.0	1.5 4.0	9.0 11.0	ns

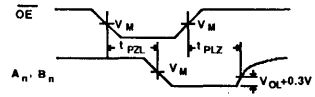
AC WAVEFORMS



Waveform 1. Propagation Delay For Non-Inverting Output



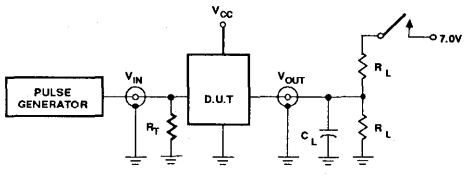
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

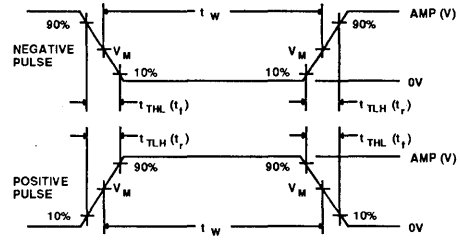
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F1604
LATCH

FAST Products

Dual Octal Latch

Product Specification

FEATURES

- **High impedance NPN base inputs for reduced loadling (20μA in High and Low state)**
- **Stores 16-Bit-Wide data inputs, multiplexed 8-Bit outputs**
- **Propagation delay 7.0ns typical**
- **Power supply current 70mA typical**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1604	7.0 ns	70mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP	N74F1604N
28-Pin Plastic SOL	N74F1604D

DESCRIPTION

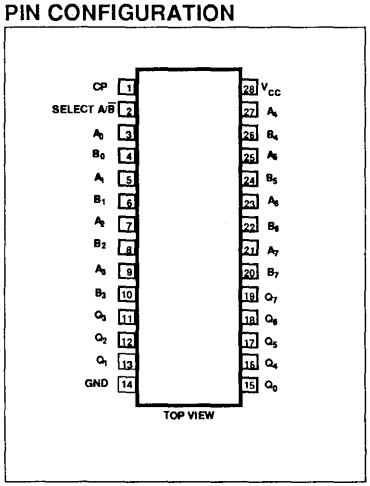
The 74F1604 is a Dual Octal Transparent Latch. Organized as 8-bit A and B latches, the latch outputs are connected by pairs to eight 2-input multiplexers. A Select (SELECT A/$\overline{B}$) input determines whether the A or B latch contents are multiplexed to the eight outputs. Data from the B inputs are selected when SELECT A/$\overline{B}$ is Low: data from the A inputs are selected when SELECT A/$\overline{B}$ is High. Data enters the latch on the falling edge of the Latch Enable ($\overline{LE}$) input. The Latch remains transparent to the data inputs while $\overline{LE}$ is Low, and stores the data that is present one setup time before the Low-to-High Latch Enable transition.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

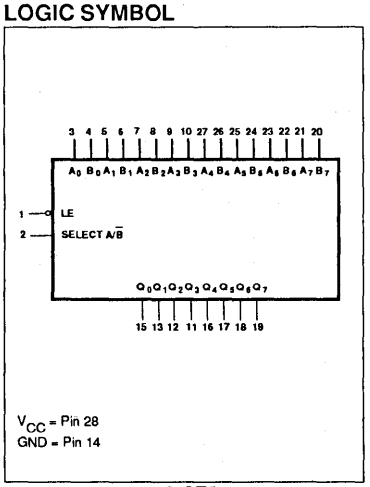
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_n, B_n	Data inputs	1.0/.033	20μA/20μA
SELECT A/$\overline{B}$	Select input	1.0/.033	20μA/20μA
$\overline{LE}$	Latch Enable input (Active Low)	1.0/.033	20μA/20μA
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

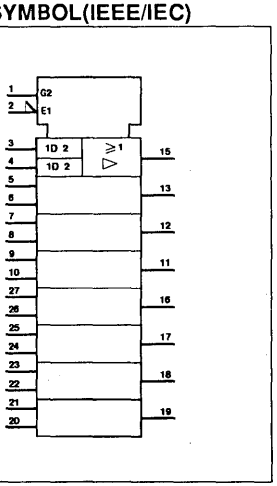
PIN CONFIGURATION



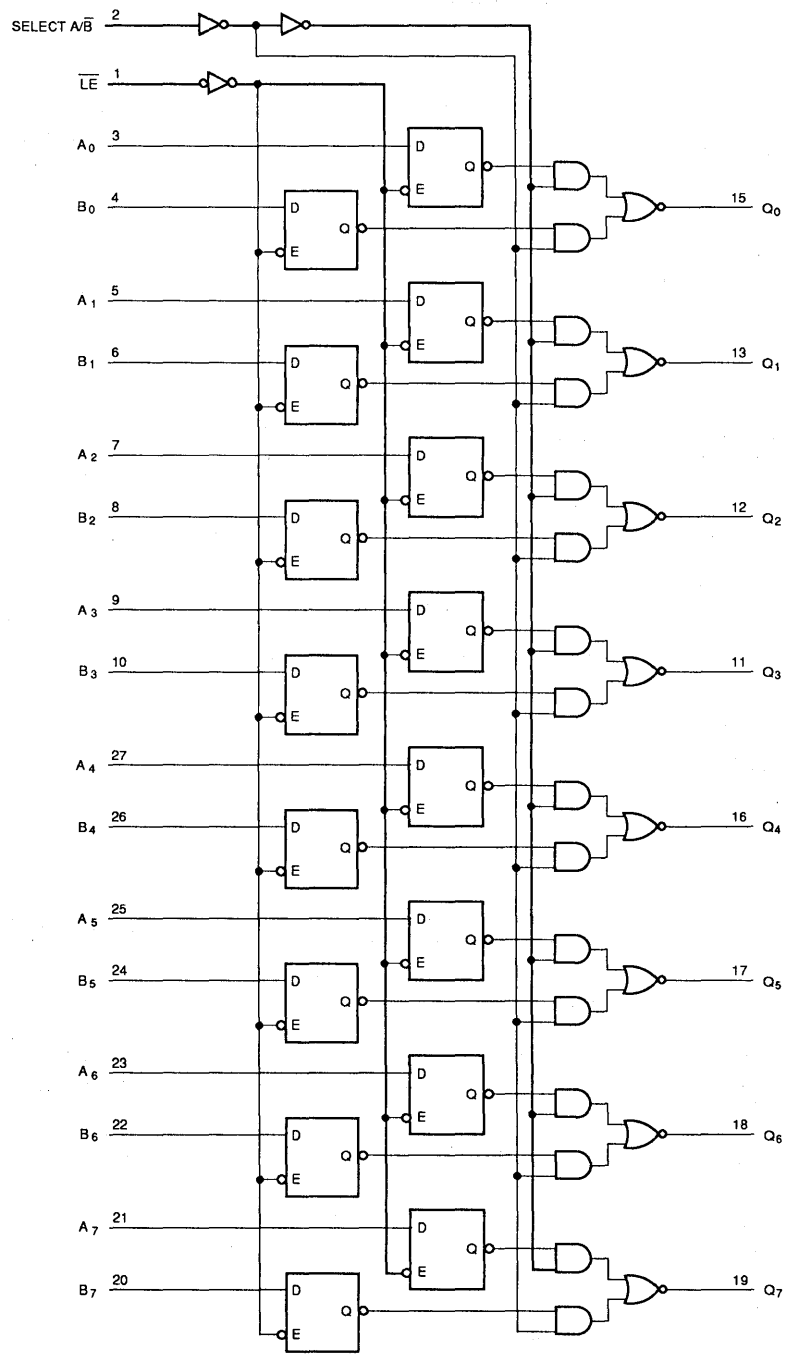
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS	OPERATING MODE
A_0 - A_7	B_0 - B_7	SELECT A/$\overline{B}$	$\overline{LE}$	Q_0 - Q_7	
A data	B data	L	L	B data	Enable and Read Register
A data	B data	H	L	A data	
X	X	X	H	NC	Hold
A data	B data	l	↑	B data	Latch and Read Register
A data	B data	h	↑	A data	

H = High voltage level
h = High voltage level one setup time to the Low-to-High $\overline{LE}$ transition
L = Low voltage level
l = Low voltage level one setup time to the Low-to-High $\overline{LE}$ transition
NC = No change
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=-1mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH}=-3mA	±10%V_{CC}	2.4			V
				±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC}=MAX,V=0.5V					-20	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			60	80	mA
		I_{CCL}				75	100	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

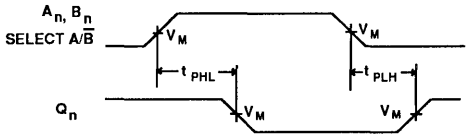
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Q_n (NINV)	Waveform 2	3.0 3.5	5.5 6.5	8.5 10.0	2.5 3.0	9.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay SELECT A/$\overline{B}$ to Q_n (INV)	Waveform 1	4.0 2.5	7.0 4.5	10.5 7.5	3.5 2.0	12.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to Q_n	Waveform 3	6.5 6.0	9.5 9.0	13.0 12.5	5.5 5.0	15.0 14.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to Q_n	Waveform 1,2	4.0 4.0	6.5 7.0	9.5 10.5	3.5 3.5	10.5 12.5	ns

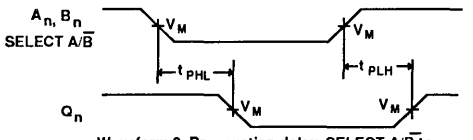
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n, B_n to $\overline{LE}$	Waveform 4	0.0 1.0			0.0 3.5		ns
t_h(H) t_h(L)	Hold time, High or Low A_n, B_n to $\overline{LE}$	Waveform 4	1.5 3.0			2.0 3.5		ns
t_w(L)	Pulse width, Low $\overline{LE}$	Waveform 4	6.5			7.5		ns

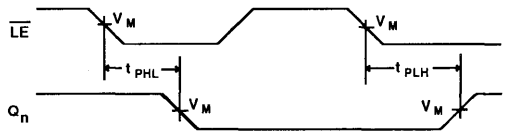
AC WAVEFORMS



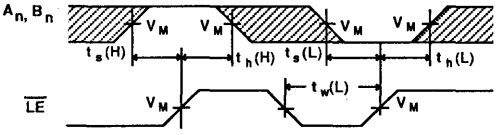
Waveform 1. Propagation delay, SELECT A/$\overline{B}$ to Output (A register stored data = Low) or Propagation delay, A n, Bn to Output



Waveform 2. Propagation delay, SELECT A/$\overline{B}$ to Output (B register stored data = Low) or Propagation delay, A n, Bn to Output



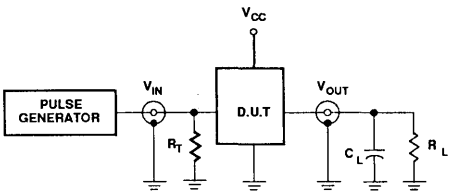
Waveform 3. Propagation delay, Latch Enable to Outputs



Waveform 4. Setup and Hold Times and $\overline{LE}$ pulse width

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

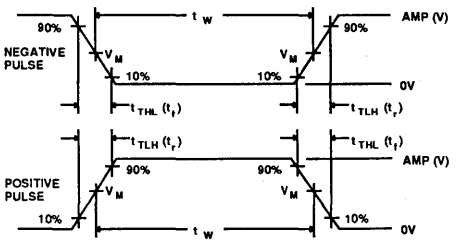
TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F1760

4-Way Latched Address Multiplexer

FAST Products

Preliminary Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1760	ns	150mA

FEATURES

- **Consists of 10 bit wide 4-1 multiplexer**
- **Separate address latch input for each channel**
- **3-state address outputs**
- **Designed for address multiplexing of dynamic RAMs and other applications**

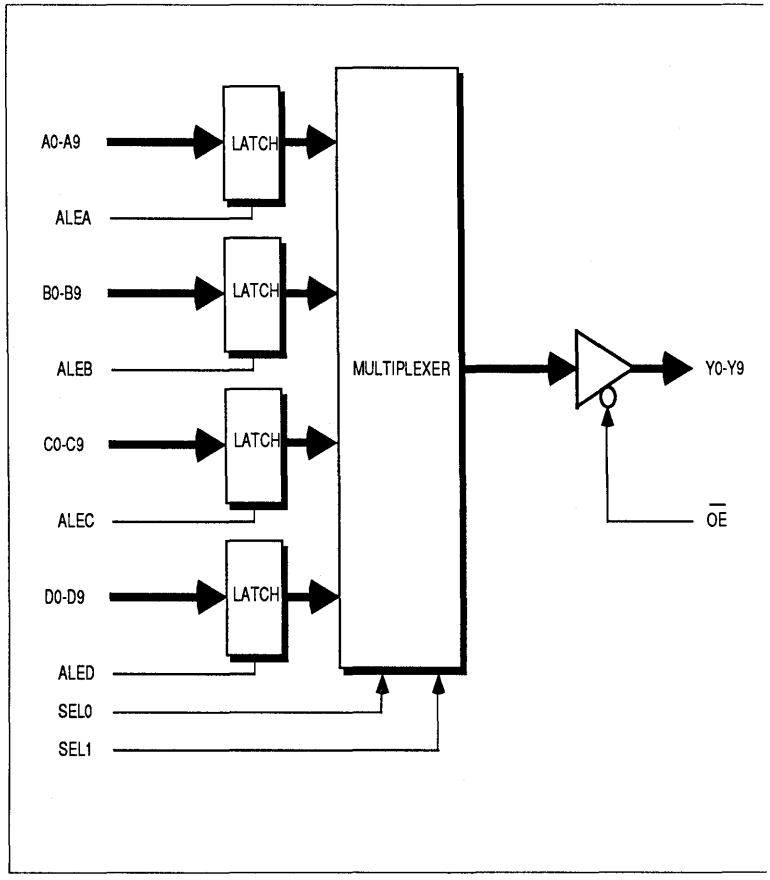
DESCRIPTION

The 'F1760 is a 10 bit wide 4-1 multiplexer. Each 10-bit channel has a separate address latch enable pin thus eliminating the need for external address latches. The 'F1760 has a common pair of Select (SEL0, SEL1) inputs to select between channels and a common Output Enable ($\overline{OE}$) pin to control the 3-State outputs.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
64-Pin Plastic DIP	N74F1760N
68-Pin Plastic PLCC	N74F1760A

BLOCK DIAGRAM



Signetics

FAST 74F1761

DRAM And Interrupt Vector Controller

FAST Products

Preliminary Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1761	100MHz	200mA

FEATURES

- **Programmable DRAM signal timing generator**
- **Automatic refresh circuitry**
- **Provides byte selection for 16 and 32 bit buses**
- **Interrupt Priority Encoder included**
- **Interrupt Acknowledge vector generator on-chip**

DESCRIPTION

The Signetics DRAM and Interrupt Vector Controller (DIVC) is a high performance bipolar device designed to reduce board space and improve performance in micro-processor-based systems. The DIVC's functions include a DRAM signal interface with user programmable timing to match the performance of specific DRAMs used in a system. With a maximum clock frequency of 100 MHz, this means a timing resolution of 10 nsec. The DRAM Controller section also includes automatic refresh arbitration, with the duration and frequency of refresh totally programmable by the user. When used with the 74F1762 Memory Address Controller, the DIVC provides a complete system solution for DRAM and Interrupt Control. For Interrupt Control, the DIVC contains an Interrupt Priority Decoder with latched inputs controlled by the Interrupt Latch Enable (ILE) input. In addition, the DIVC contains an Interrupt Acknowledge Controller which passes a program-mable 8-bit vector on the system data bus upon receipt of an interrupt acknowledge. There are 7 interrupt acknowledge vectors, each accessable by placing the priority number of the interrupt acknowledge on the A_1-A_3 signal inputs while acknowledging an interrupt.

ORDERING INFORMATION

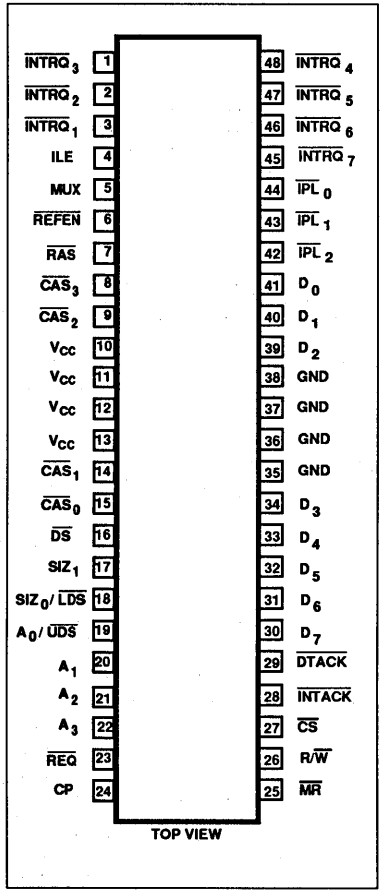
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
48-Pin Plastic DIP	N74F1761N
44-Pin PLCC	N74F1761A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

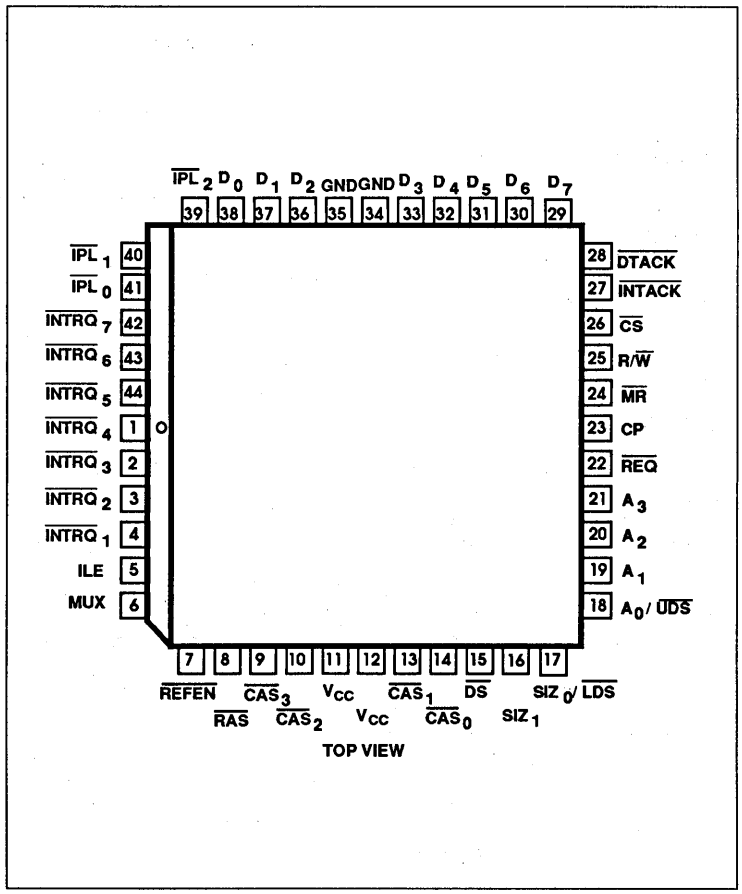
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{REQ}$	DRAM Request input	1.0/1.0	20µA/0.6mA
$SIZ_0/\overline{LDS}$, SIZ_1, $A_0/\overline{UDS}$, A_1	Byte Select inputs	1.0/1.0	20µA/0.6mA
A_2, A_3	Register Select inputs	1.0/1.0	20µA/0.6mA
$\overline{CS}$, $\overline{DS}$	Chip Select, Data Strobe inputs	1.0/1.0	20µA/0.6mA
R/$\overline{W}$	Read/Write input	1.0/1.0	20µA/0.6mA
$\overline{INTACK}$	Interrupt Acknowledge input	1.0/1.0	20µA/0.6mA
ILE	Interrupt Latch Enable intput	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input	1.0/1.0	20µA/0.6mA
$\overline{INTRQ}_{1-7}$	Interrupt Request inputs	1.0/1.0	20µA/0.6mA
$\overline{DTACK}$	Data Transfer Acknowledge output	OC/40	OC/24mA
D_0-D_7	Data Bus outputs	50/40	1.0mA/24mA
IPL_{0-2}	Interrupt Priority outputs	50/40	1.0mA/24mA
$\overline{RAS}$, MUX, $\overline{REFEN}$, $\overline{CAS}_{0-7}$	DRAM Control outputs	N/A	35mA/60mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
FAST Unit Loads do not correspond to DRAM input Loads.
OC=Open Collector

DIP PIN CONFIGURATION



PLCC PIN CONFIGURATION



NOTE: Pinout assignments are strictly preliminary and are subject to change

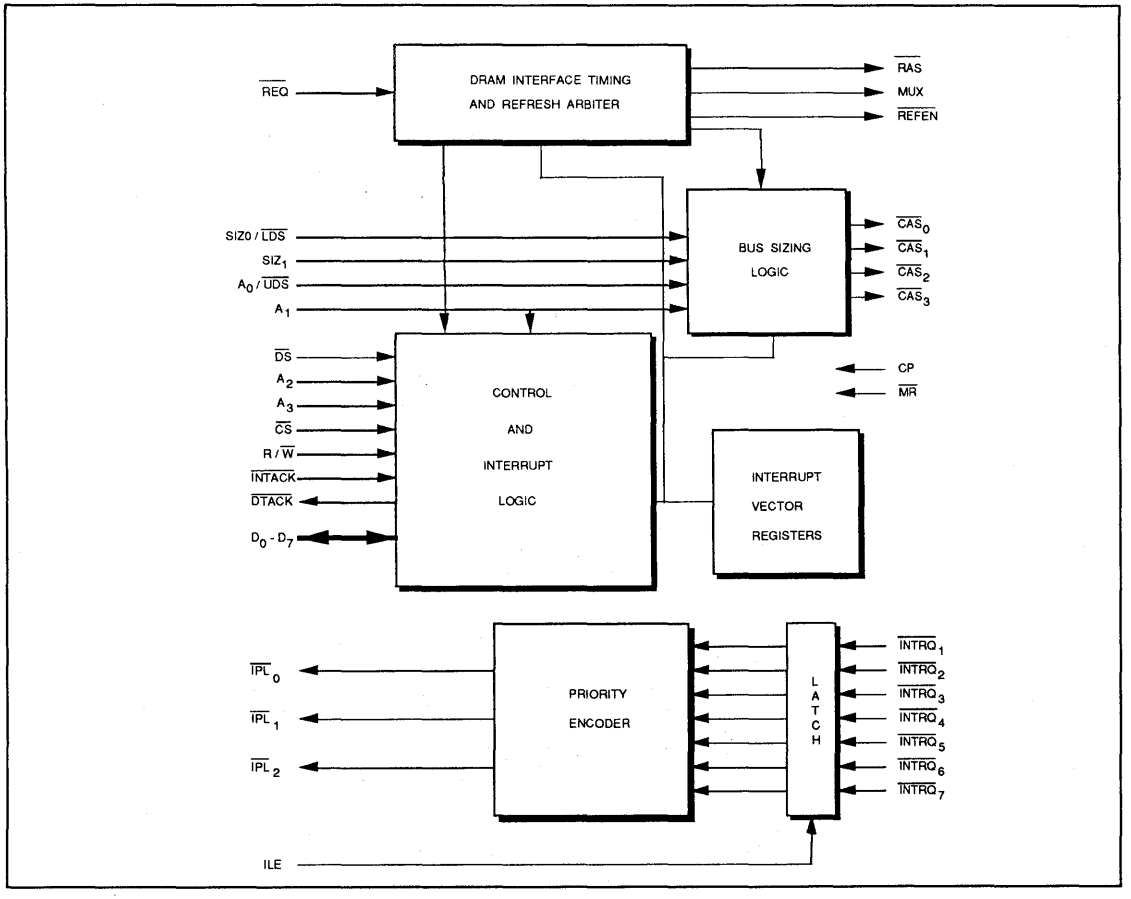
FUNCTIONAL DESCRIPTION

Figure 1 shows the overall architecture of the 74F1761. The DRAM Interface Timing section produces the $\overline{RAS}$, MUX, $\overline{CAS}$, $\overline{DTACK}$ and Refresh Enable ($\overline{REFEN}$) signals in response to the Request ($\overline{REQ}$) input. The timing of these signals is configurable by programming a register set within the F1761 (see **REGISTER DESCRIPTION**). The timing section also includes a refresh arbiter that allows for refreshing the DRAM at a frequency programmable by the user. While a refresh cycle is being executed, the $\overline{REFEN}$ output is asserted, allowing a companion memory address generator (such as the 74F1762 Memory Address Controller) to assert a refresh row address on the DRAM address inputs.

The Bus Sizing Logic section is a configurable decoder that allows for multiple $\overline{CAS}$ outputs depending on the state of the $\overline{DS}$, $SIZ_0/\overline{LDS}$, SIZ_1, $A_0/\overline{UDS}$, and A_1 signal inputs, and the selected bus size scheme (See **Table 4. CAS DECODING SUMMARY**). By programming the Configuration Register, the F1761 can respond to a variety of 8, 16, and 32 Bit Processor signal outputs. In the 8-bit mode, the F1761 will assert one of four $\overline{CAS}$ outputs depending on the state of the A_0 and A_1 inputs during the $\overline{CAS}$ signal assertion time determined by the timing logic. In the 16-bit mode, the F1761 will assert $\overline{CAS_0}$ and/or $\overline{CAS_1}$ depending on the state of the $\overline{UDS}$ and LDS inputs, respectively. In the 32 Bit mode, the A_1, A_0, SIZ_1 and SIZ_0 determine the $\overline{CAS}$ outputs to be asserted according to the 68020 byte-selection scheme.

The Control and Interrupt Logic section determines the response of the F1761 in one of two modes. The internal registers of the device can be accessed by asserting the $\overline{CS}$ and $\overline{DS}$ inputs while placing the address of the register to be accessed on

BLOCK DIAGRAM



the A_1, A_2, and A_3 inputs. The R/$\overline{W}$ input indicates to the F1761 the direction of data transfer when accessing a particular register. In addition, the configuration register contains one bit of register addressing that is initialized to 0. The lower order registers contain the timing information for the DRAM interface, while the upper order registers contain the Interrupt Vectors to be passed during an interrupt acknowledge. All internal registers are read/write, with unused bits being read as zeros and ignored during write cycles. In the Interrupt Acknowledge mode, the $\overline{INTACK}$ input signals the F1761 that an interrupt acknowledge is occuring. The F1761 responds by placing the contents of one of seven vector registers on the data outputs, according to the value of the A_1, A_2, and A_3 signal inputs. For both Register Access and Interrupt Acknowledge modes, the device will assert $\overline{DTACK}$ to indicate the completion of the cycle. This $\overline{DTACK}$ signal is also asserted by the DRAM timing logic in response to a Request from the processor, with its timing programmed by the user.

The F1761 also includes an 8 to 3 bit Interrupt Priority Encoder which can be used to interface with the 68000 family of processors, with the Interrupt inputs ($\overline{INTRQ_1}$ - $\overline{INTRQ_7}$) latched on the falling edge of the Interrupt Latch Enable (ILE) input. The ILE input can be connected to the processor clock for glitch-free interrupting.

All of the DRAM interface timing is based upon the Master Clock (CP) input. Numerical values programmed into the Timing Registers indicate the number of clock cycles between events. When a 0 value is programmed into a timing skew, the two events indicated will happen simultaneously. The AC specifications indicate the amount of timing variation due to propogation delays within the device. The Master Reset input ($\overline{MR}$) initializes all timing registers to their maximum delay (All ones) and clears the Configuration Register.

PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
$\overline{DS}$	2	2	Input	Active Low Data Strobe used to enable the Data Bus during register access cycles and the $\overline{CAS}$ outputs during DRAM access cycles.
$SIZ_0/\overline{LDS}$	3	3	Input	In 16-bit Mode, an active Low Lower Data Strobe signal used to enable the $\overline{CAS}_1$ output during a DRAM access cycle. In 32-bit Mode, an active High SIZE 0 signal used with SIZ_1 to indicate to the DIVC the size of the DRAM access transaction.
SIZ_1	4	4	Input	In 32-bit Mode, an active High SIZE 1 signal used with SIZ_0 to indicate to the DIVC the size of the DRAM access transaction.
$A_0/\overline{UDS}$	5	5	Input	In 16-bit Mode, an active Low Upper Data Strobe used to enable the $\overline{CAS}_0$ output during a DRAM access cycle. In 32-bit Mode, used with A1 to indicate to the DIVC the byte boundary of the DRAM access transaction.
A_1	6	6	Input	During DIVC register access, forms the least significant address bit of the register address. During DRAM access and in 32-bit Mode, used with A_0 to indicate to the DIVC the byte boundary of the DRAM access transaction.
A_2, A_3	7,8	7,8	Inputs	During DIVC register access, forms the most significant two address bits of the register address.
$\overline{REQ}$	1	1	Input	Active Low DRAM Access Request indicating to the DIVC that the processor wishes to access the DRAM controlled by the DIVC.
$\overline{CS}$	9	9	Input	Active Low Chip Select used for Register Access with the DIVC.
$R/\overline{W}$	10	10	Input	Read/Write signal used to indicate the direction of register access with the DIVC.
V_{CC}	11-14	11-14		Power Supply +5V ± 10%
$\overline{INTACK}$	15	13	Input	Active Low Interrupt Acknowledge signal used with the A_1, A_2, and A_3 inputs to assert the contents of one of seven internal Interrupt Vector Registers on the data bus (D_0-D_7).
$\overline{DTACK}$	16	14	Output	Active Low Data Transfer Acknowledge indicates to the processor the completion of a DIVC register or DRAM access cycle. For DRAM access, this signal's timing is programmable internally. Open Collector Output.
D_0-D_7	17-24	15-22	Input/ Output	Active High 3-State Data Bus over which data is transferred between the processor and internal registers of the DIVC.
$\overline{IPL}_0$ $\overline{IPL}_1$ $\overline{IPL}_2$	34 33 32	32 31 30	Output Output Output	Active Low Interrupt Priority Level signals indicating to the processor the priority level of the highest latched interrupt request on the $\overline{INTRQ}_{1-7}$ inputs. A level of all ONES indicates no interrupt rrequest pending
ILE	39	35	Input	Active High Interrupt Latch Enable which causes the internal latches connected to the $\overline{INTRQ}_{1-7}$ inputs to become transparent. A High-to-Low transition causes the $\overline{INTRQ}_{1-7}$ signals to be internally latched.
$\overline{INTRQ}_{1-7}$	31-25	41-38	Input	Active Low Interrupt Request inputs.
CP	40	36	Input	DIVC Clock input.
$\overline{MR}$	41	37	Input	Active Low Master Reset input.
$\overline{CAS}_{0-3}$	45-42	41-38	Output	Active Low Column Address Strobe inputs.
$\overline{REFEN}$	46	42	Output	Active Low Refresh Enable output. Indicates that the refresh address should be asserted.
MUX	47	43	Output	Active High Multiplexer output. Indicates that the column address should be asserted to the DRAMS.
$\overline{RAS}$	48	44	Output	Active Low Row Address Strobe inputs.
GND	35-38	33-34		Ground Reference.

TABLE 2. DIVC Register Selection Map

RSS[1]	A_3	A_2	A_1	ACRONYM	REGISTER NAME	MODE	AFFECTED BY RESET
X	0	0	0	CR	Configuration Register	R/W	Yes
0	0	0	1	RTR	Refresh Timing Register	R/W	Yes
0	0	1	0	TR2	Timing Register 2	R/W	Yes
0	0	1	1	TR3	Timing Register 3	R/W	Yes
0	1	0	0	TR4	Timing Register 4	R/W	Yes
0	1	0	1	TR5	Timing Register 5	R/W	Yes
0	1	1	0	-----	Reserved	-----	-----
0	1	1	1	-----	Reserved	-----	-----
1	0	0	1	VR1	Vector Register 1	R/W	No
1	0	1	0	VR2	Vector Register 2	R/W	No
1	0	1	1	VR3	Vector Register 3	R/W	No
1	1	0	0	VR4	Vector Register 4	R/W	No
1	1	0	1	VR5	Vector Register 5	R/W	No
1	1	1	0	VR6	Vector Register 6	R/W	No
1	1	1	1	VR7	Vector Register 7	R/W	No

NOTE:
1. RSS=Register Set Select Bit in the Configuration Register

REGISTER DESCRIPTION

Register Map

The DIVC contains a set of registers which can be programmed by a controlling processor to configure the DIVC for different bus sizes, DRAM timing, and Interrupt Vectors. Table 2 shows the Register Map of the DIVC. Note that the higher-order bit of the register address (RSS) is contained in the Configuration Register. Access to the Configuration Register is independent of the value of the RSS bit. By toggling the RSS bit, two sets of registers can be accessed. Those registers accessed with RSS = 0 are the DRAM timing registers for programming events during DRAM access. With RSS = 1, the seven Interrupt Vector registers can be accessed.

Configuration Register (CR)

This register configures the mode of access and register set select for the DIVC. **Bits 7 and 6** are used to specify the size of the bus to be used with the DRAM controlled by the DIVC. In the 8-bit mode, the Column Address Strobe outputs will respond to $\overline{CAS}$ signal assertion from the Timing Block by asserting one of the $\overline{CAS}$ outputs depending on the state of the A_0 and A_1 inputs, in binary fashion (i.e. If A_0=A_1=0 then $\overline{CAS}_0$=0; if A_0=0 and A_1=1 then $\overline{CAS}_2$=0). In 16-bit mode, the DIVC responds to a $\overline{CAS}$ assertion from the Timing Block by asserting $\overline{CAS}_0$ and $\overline{CAS}_1$ depending on the state of the $\overline{UDS}$ and $\overline{LDS}$ inputs, respectively. In 32-bit mode, the SIZ_0, SIZ_1, A_0, and A_1 inputs determine the state of the $\overline{CAS}$ outputs according to the decoding used with the 68020 Microprocessor, with $\overline{CAS}_0$ corresponding to the most significant byte and $\overline{CAS}_3$ corresponding to the least significant byte of the 32-bit bus. **Bit 5** is used as a register set select (RSS) for accessing the other registers in the DIVC. When RSS is low, registers 1 through 5 correspond to the Refresh Timing Register and Timing Registers 2 through 5. With RSS high, registers 1 through 7 correspond to Vector Registers 1 through 7. **Bit 4** is used to disable the refreshing operation of the DRAM Controller section of the DIVC. When set, no refreshes will be performed and internally generated Refresh Requests will be ignored, regardless of the state of the refresh timing parameters. Other bits in the Configuration Register are ignored on write cycles and are read as zeros on read cycles. All implemented bits of this register are reset to zeros when the DIVC is reset.

Refresh Timing Register (RTR)

The value in this register is used with a reloadable counter within the DIVC to generate refresh requests. Each time the counter counts down (using the CP clock divided by sixteen), a refresh request will be generated inside the DIVC. If no DRAM access is taking place, the DIVC immediately performs a refresh cycle, using the REFRESH RASON to RASOFF delay programmed into Timing Register 2, and the RASOFF to REFRESHOFF delay programmed into Timing Register 3. If a DRAM access cycle has already begun, the DIVC will wait until the completion of the DRAM access cycle, after which it will perform the refresh cycle as explained. A value of all zeros will program the DIVC with the shortest possible delay between refresh requests: 16 CP clock cycles. At 100 MHz., this register gives a refresh period resolution of 160 nsec. Resetting the DIVC changes all bits to ones.

Timing Register 2 (TR2)

Bits 0 to 4 of this register program the $\overline{RAS}$ pulse width of a refresh cycle in CP clock cycles. Although a value of zero would normally result in no $\overline{RAS}$ pulse during a refresh cycle, internal propagation delays cause a small $\overline{RAS}$ pulse to be output. Resetting the DIVC will result in all these bits being set to ones. **Bits 5 to 7** are ignored during write cycles and read as zeros during read cycles.

Timing Register 3 (TR3)

Bits 0 to 3 of this register program the

Table 3. REGISTER BIT FORMATS

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	BUS SIZING		RSS	RD	UNIMPLEMENTED			
CR	00 = 8 Bit Mode 01 = 16 Bit Mode 10 = 32 Bit Mode 11 = Invalid		See Text	Refresh Disable				

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	REFRESH TIMING COUNTER VALUE							
RTR	Refresh Period in CP/16 Cycles							

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	UNIMPLEMENTED			REFRESH RAS PULSE WIDTH				
TR2				CP Cycles				

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	UNIMPLEMENTED			REFRESH RAS OFF TO REFRESH OFF				
TR3				CP Cycles - 1				

delay between $\overline{RAS}$ negated and the end of a refresh cycle. Because an access cycle could begin immediately after the refresh, some delay may be desired between RASOFF and the end of the refresh cycle to accomodate $\overline{RAS}$ precharge requirements of the DRAMs. The value programmed into these bits should be one less than the number of clock cycle delays desired. Resetting the DIVC will result in these bits being set to ones. **Bits 4 to 7** are ignored during write cycles and read as zeros during read cycles.

Timing Register 4 (TR4)

Bits 5-7 of this register program the DIVC with the ACCESS GRANT TO $\overline{RAS}$ delay of a DRAM access cycle in CP clock cycles. Since the $\overline{REFEN}$ output is asserted during a refresh cycle, it is commonly used as a select signal for address multiplexers that select between a processor address and the refresh row address. If, on the completion of a refresh cycle, the DIVC immediately performs an access cycle, there may be a need to wait until the processor's row address has become stable at the DRAMs, before asserting $\overline{RAS}$. (Since the $\overline{REFEN}$ output is negated at the same time as the refresh $\overline{RAS}$ output, and there is a programmable delay between RASOFF and REFRESHOFF, the problem is associated with the application. See explanation of bits 3-7 in Timing Register 3) These bits can be programmed with the number of clock cycles to wait from the time that an access is granted until $\overline{RAS}$ is asserted. A value of zero will result in no delay between events. **Bits 3 and 4** configure the timing between $\overline{RAS}$ and the MUX output asserted in CP clock cycles. A value of zero in these bits will cause no delay between $\overline{RAS}$ and MUX. **Bits 0 to 2** configure the timing between MUX asserted and $\overline{CAS}$ asserted in CP clock cycles. A value of zero in these bits will cause no delay between MUX and $\overline{CAS}$. Resetting the DIVC sets all bits of this register to ones.

Timing Register 5 (TR5)

Bits 5 to 7 of this register program the delay between the assertion of CAS and the negation of $\overline{RAS}$, in CP clock cycles. A value of zero in these bits results in no delay between these events. **Bits 0 to 4** program the delay beween the assertion of $\overline{RAS}$ and the assertion of $\overline{DTACK}$ back to the processor over the chip's DTACK signal pin. A value of zero in these bits results in no delay between these events. Resetting the DIVC will result in all bits of this register being set to ones.

Interrupt Vector Registers 1 to 7 (VR1-7)

Each of these registers can be programmed to contain the 8-bit vector to be placed on the DIVC's data bus during an Interrupt Acknowledge cycle. When the processor asserts the $\overline{INTACK}$ and $\overline{DS}$ inputs and places the Interrupt Priority on the A_1, A_2, and A_3 inputs, the DIVC will respond by placing the contents of the Interrupt Vector Register addressed by these address inputs on the data bus and asserting $\overline{DTACK}$. In this way, peripheral devices which do not contain the interrupt acknowledging circuitry can be used with a processor which expects these kinds of acknowledge cycles to occur. Resetting the DIVC does not affect the contents of these registers.

TABLE 3. REGISTER BIT FORMATS (Continued)

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
TR4	GRANT TO RAS DELAY			RAS TO MUX DELAY		MUX TO CAS DELAY		
	CP Cycles			CP Cycles		CP Cycles		

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
TR5	CAS TO RAS OFF DELAY			RAS TO DTACK DELAY				
	CP Cycles			CP Cycles				

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VR1-VR7	INTERRUPT VECTOR VALUE							

TABLE 4. CAS DECODING SUMMARY

MODE	$SIZ_0/\overline{LDS}$	SIZ_1	$A_0/\overline{UDS}$	A_1	$\overline{CAS}_0$	$\overline{CAS}_1$	$\overline{CAS}_2$	$\overline{CAS}_3$
8	X	X	0	0	0	1	1	1
8	X	X	1	0	1	0	1	1
8	X	X	0	1	1	1	0	1
8	X	X	1	1	1	1	1	0
16	1	X	1	X	1	1	1	1
16	1	X	0	X	0	1	1	1
16	0	X	1	X	1	0	1	1
16	0	X	0	X	0	0	1	1
32	1	0	0	0	0	1	1	1
32	1	0	1	0	1	0	1	1
32	1	0	0	1	1	1	0	1
32	1	0	1	1	1	1	1	0
32	0	1	0	0	0	0	1	1
32	0	1	1	0	1	0	0	1
32	0	1	0	1	1	1	0	0
32	0	1	1	1	1	1	1	0
32	1	1	0	0	0	0	0	1
32	1	1	1	0	1	0	0	0
32	1	1	0	1	1	1	0	0
32	1	1	1	1	1	1	1	0
32	0	0	0	0	0	0	0	0
32	0	0	1	0	1	0	0	0
32	0	0	0	1	1	1	0	0
32	0	0	1	1	1	1	1	0

NOTE: This table gives the functional decoding of the $\overline{CAS}$ output signals of the DIVC when $\overline{DS}$ is valid and the DRAM timing circuitry asserts $\overline{CAS}$.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	120	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-35	mA
I_{OL}	Low-level output current			60	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -15mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH2}[3] = -35mA	±10%V_{CC}	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
			I_{OL2}[4] = 60mA	±10%V_{CC}		0.45	0.80	V
V_{IK}	Input clamp voltage	V_{CC}= MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_O	Output current[5]	V_{CC} = MAX, V_O = 2.25V			-100		-225	mA
I_{CC}	Supply current (total)	V_{CC}= MAX				200	220	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH2} is the current necessary to guarantee a Low to High transition in a 70Ω transmission line and is specified for the $\overline{RAS}$, $\overline{CAS}_{0-3}$, MUX, and $\overline{REFEN}$ signals.
4. I_{OL2} is the current necessary to guarantee a High to Low transition in a 70Ω transmission line and is specified for the $\overline{RAS}$, $\overline{CAS}_{0-3}$, MUX, and $\overline{REFEN}$ signals.
5. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L =300pF, R_L = 70Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1 (1)	100	110		100		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CS}$ or $\overline{DS}$ to D_n (Read)	Waveform 3 (10) Test Circuit 2		5.0 5.0	8.0 8.0		10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CS}$ or $\overline{DS}$ negated to D_n invalid (Read)	Waveform 3 (11) Test Circuit 2		8.0 8.0	10.0 10.0		12.0 12.0	ns
t_{PHL}	Propagation delay $\overline{CS}$ to $\overline{DTACK}$ asserted	Waveform 3,4 (12) Test Circuit 3		4.0	5.0		6.0	ns
t_{PLH}	Propagation delay $\overline{CS}$ negated to $\overline{DTACK}$ negated	Waveform 3,4 (13) Test Circuit 3		4.0	5.0		6.0	ns
t_{PLH} t_{PHL}	Propagation delay D_n (data in) invalid to $\overline{DS}$ negated (Write)	Waveform 4 (15)		0 0	0 0	0 0		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{DS}$ negated to D_n (data in) invalid (Write)	Waveform 4 (16)		5.0 5.0	3.0 3.0	5.0 5.0		ns
t_{PLH} t_{PHL}	Propagation delay $\overline{INTACK}$ or $\overline{DS}$ to D_n (data out)	Waveform 8 (20) Test Circuit 2		5.0 5.0	8.0 8.0		10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{INTACK}$ or $\overline{DS}$ negated to D_n (data out) invalid	Waveform 8 (21) Test Circuit 2		8.0 8.0	10.0 10.0		10.0 10.0	ns
t_{PHH}	Propagation delay $\overline{INTACK}$ asserted to $\overline{DTACK}$ asserted	Waveform 8 (22) Test Circuit 3		4.0	6.0		7.0	ns
t_{PLL}	Propagation delay $\overline{INTACK}$ negated to $\overline{DTACK}$ negated	Waveform 8 (23) Test Circuit 3		4.0	5.0		6.0	ns
t_{PLL}	Propagation delay, Worst case $\overline{REQ}$ negated to $\overline{RAS}$ with 000 IN TR4	Waveform 6 (25)			8.0 +Tcp		11 +Tcp	ns
t_{PHL}	Propagation delay, CP to $\overline{RAS}$ asserted	Waveform 6 (26)		6.0	9.0 [7.0]		11.0 [9.0]	ns
t_{PHH}	Propagation delay, CP to $\overline{RAS}$ negated	Waveform 6 (27)		10.0	14.0 [7.0]		16.0 [9.0]	ns
t_{PHH}	Propagation delay, CP to MUX asserted	Waveform 6 (28) Test Circuit 2		7.0	8.0 [7.0)		10.0 [12.0]	ns
t_{PHL}	Propagation delay $\overline{REQ}$ negated to MUX negated	Waveform 6 (29) Test Circuit 2		5.0	6.0		8.0	ns
t_{PHL}	Propagation delay, CP to $\overline{CAS}$ asserted	Waveform 6 (30)		9.0	12.0 [14.0]		14.0 [16.0]	ns
t_{PHH}	Propagation delay $\overline{REQ}$ negated to $\overline{CAS}$ negated	Waveform 6 (31)		8.0	10.0		12.0	ns
t_{PHL}	Propagation delay CP to $\overline{DTACK}$ asserted	Waveform 6 (34) Test Circuit 3		7.0	9.0 [11.0]		110 [13.0]	ns
t_{PHH}	Propagation delay $\overline{REQ}$ negated to $\overline{DTACK}$ negated	Waveform 6 (35) Test Circuit 3		5.0	7.0		9.0	ns
t_{PHL}	Propagation delay, CP to $\overline{REFEN}$ asserted	Waveform 5 (36) Test Circuit 3		4.0	5.0		6.0	ns
t_{PHH}	Propagation delay, CP to $\overline{REFEN}$ negated	Waveform 5 (38) Test Circuit 3		5.0	10.0		12.0	ns
t_{PHL}	Propagation delay CP to Refresh $\overline{RAS}$ asserted	Waveform 5 (37)		5.0	6.0		7.0	ns
t_{PHH}	Propagation delay CP to Refresh $\overline{RAS}$ negated	Waveform 5 (39)		5.0	11.0		13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{INTRQ}$ asserted to $\overline{IPL}$ asserted	Waveform 7 (43) Test Circuit 2		5.0	10.0		12.0	ns

NOTES: 1. Worst case REQ to RAS assumes that REQ did not meet setup time requirements on the last rising edge of CP, that 000 was programmed into the GRANT to $\overline{RAS}$ delay in TR4, and that no refresh request is pending of being executed. Tcp is AC parameter number 1.

2. Numbers in square brackets indicarte propagation delay with 0 programmed into the appropriate delay field.

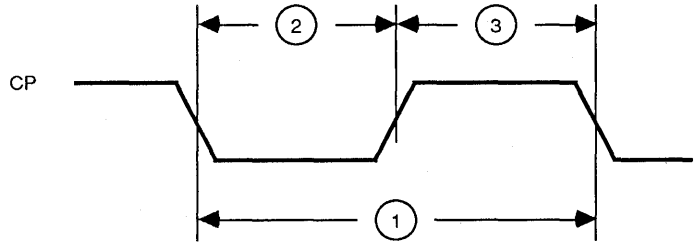
3. Numbers in round brackets in the TEST CONDITION column correspond to numbers (in circles) in AC WAVEFORMS .

AC SETUP REQUIREMENTS

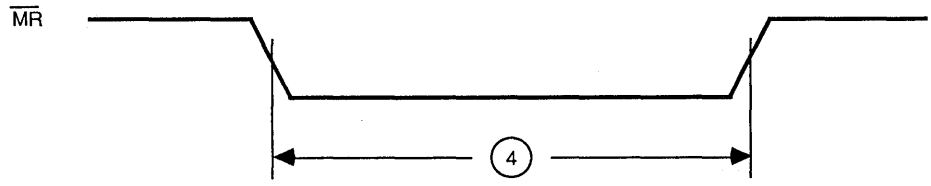
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 300pF, R_L = 70Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_1 - A_3 to $\overline{CS}$	Waveform 3,4 (6)	5.0 5.0	3.0 3.0		5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_1 - A_3 to $\overline{CS}$	Waveform 3,4 (7)	3.0 3.0	2.0 2.0		3.0 3.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low R/$\overline{W}$ to $\overline{CS}$	Waveform 3,4,8 (8)	5.0 5.0	3.0 3.0		5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low R/$\overline{W}$ to $\overline{CS}$	Waveform 3,4,8 (9)	3.0 3.0	2.0 2.0		3.0 3.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_1 - A_3 to $\overline{INTACK}$	Waveform 8 (17)	5.0 5.0	3.0 3.0		5.0 5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_1 - A_3 to $\overline{INTACK}$	Waveform 8 (19)	3.0 3.0	2.0 2.0		3.0 3.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{INTRQ}$ to ILE	Waveform 7 (40)	8.0 8.0	6.0 6.0		10.0 10.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{INTRQ}$ to ILE	Waveform 7 (41)	6.0 6.0	8.0 8.0		10.0 10.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low SIZ_0, SIZ_1, A_0, A_1 to $\overline{CAS}$	Waveform 6 (32)	4.0 4.0	3.0 3.0		4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low SIZ_0, SIZ_1, A_0, A_1 to $\overline{CAS}$	Waveform 6 (33)	0 0	0 0		0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{REQ}$ to CP	Waveform 6 (24)	2.0 2.0	1.2 1.2		2.0 2.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1 (3,2)	5.0 5.0	4.0 4.0		5.0 5.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2 (4)	20	15		20		ns
$t_w(L)$	$\overline{CS}$ Pulse width, Low	Waveform 3,4 (5)	50	40		50		ns
$t_w(L)$	$\overline{DS}$ Pulse width, Low	Waveform 4 (14)	30	25		30		ns
$t_w(L)$	$\overline{INTACK}$ Pulse width, Low	Waveform 8 (17)	30	25		30		ns
$t_w(L)$	ILE Pulse width, Low	Waveform 7 (42)	17	15		12		ns

NOTES:
1. These numbers indicate that the address inputs have a negative setup time and could not be valid 4ns after the falling edge of the CP clock. It is suggested that $\overline{SEL_2}$ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of $\overline{SEL_1}$ to enable Address Bus 1. This will insure that setup time for Address Bus 1 is not violated.
2. Numbers in round brackets in the TEST CONDITIONS column correspond to numbers (in circles) in AC WAVEFORMS

AC WAVEFORMS



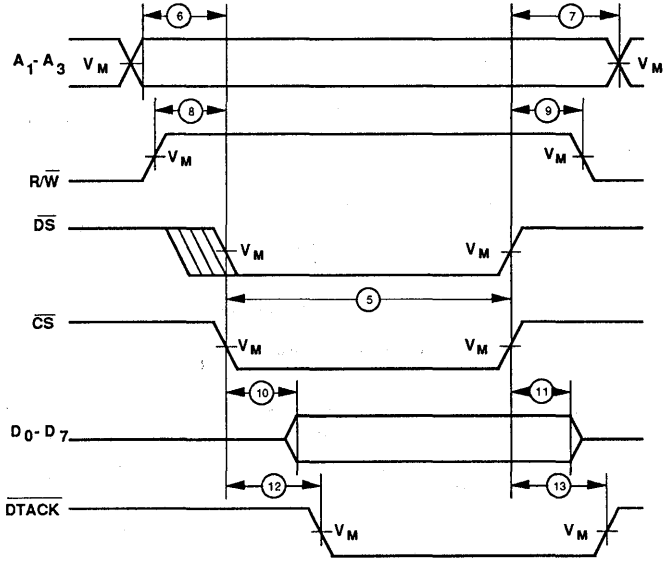
Waveform 1. CP Timing



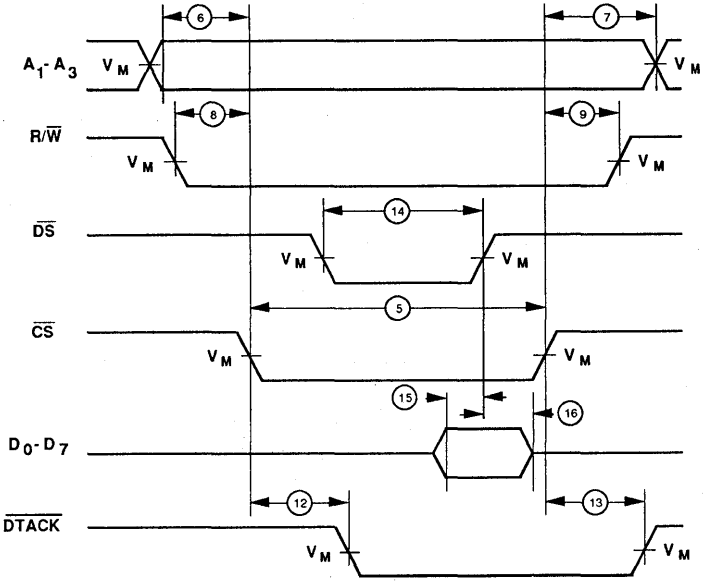
Waveform 2. MR Timing

NOTE: For all waveforms, $V_M = 1.5V$.

AC WAVEFORMS



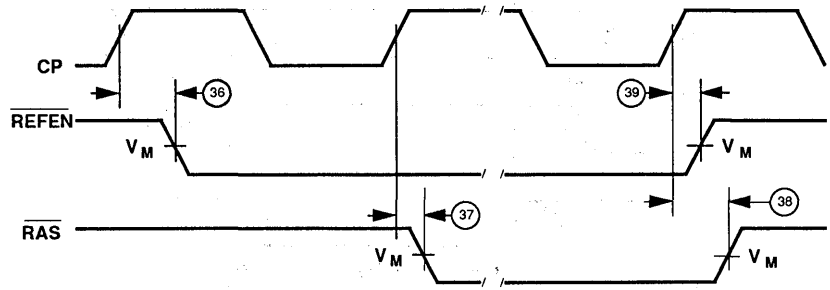
Waveform 3. Bus Timing (Read Cycle)



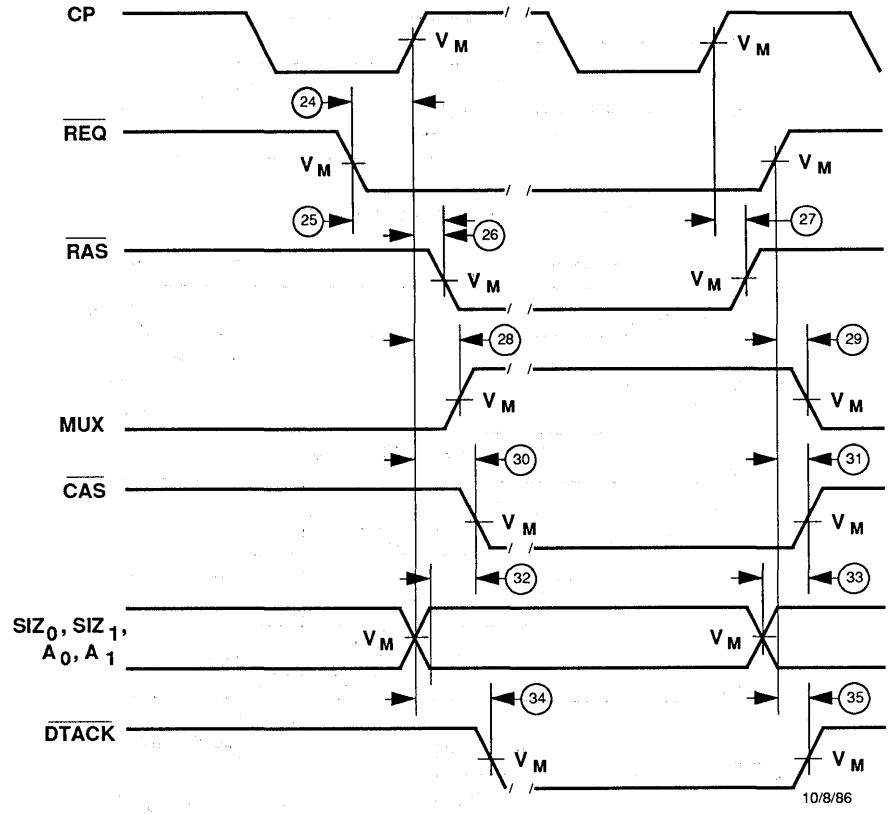
Waveform 4. Bus Timing (Write Cycle)

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

AC WAVEFORMS



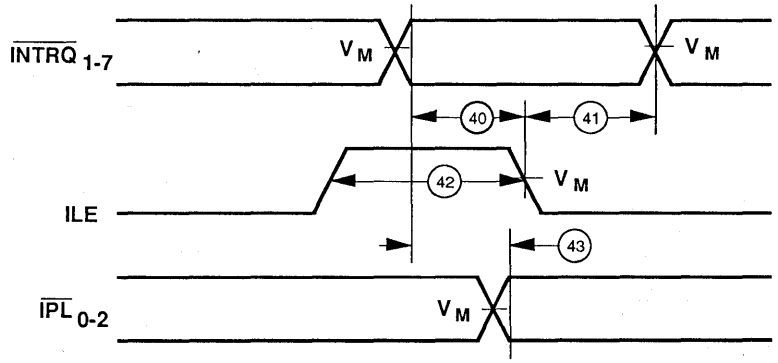
Waveform 5. Refresh Timing



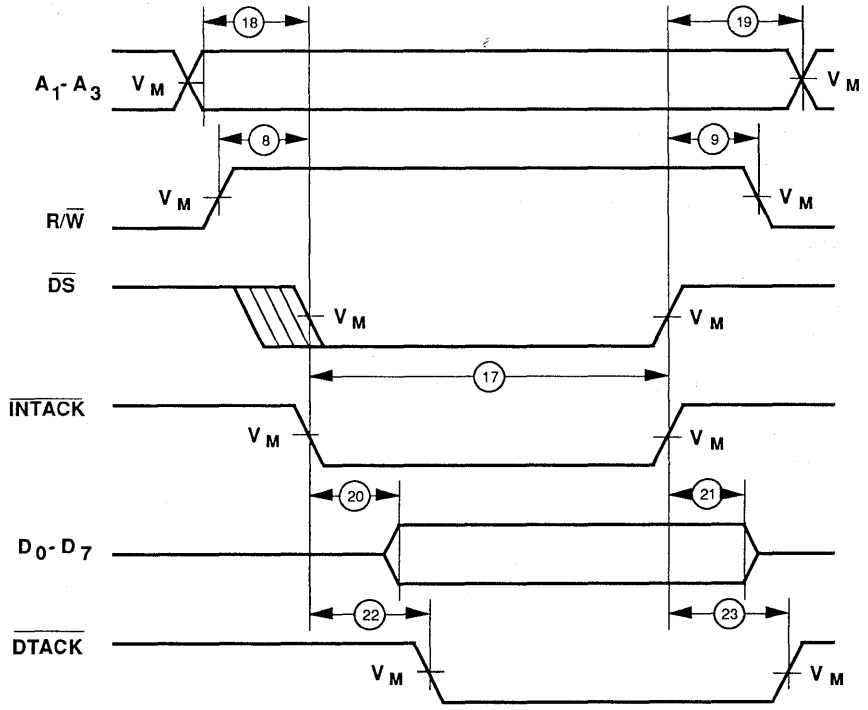
Waveform 6. DRAM Access Timing

NOTE: For all waveforms, $V_M = 1.5V$.

AC WAVEFORMS



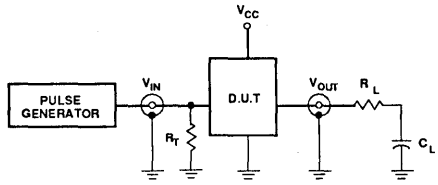
Waveform 7. Interrupt Request Timing



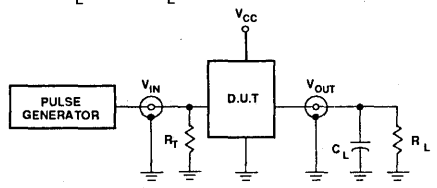
Waveform 8. Interrupt Acknowledge Timing

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

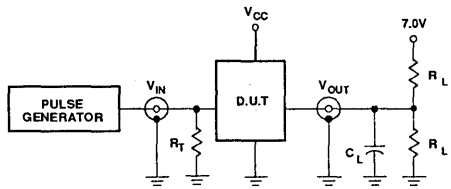
TEST CIRCUITS AND WAVEFORMS



Test Circuit 1 for $\overline{RAS}$ and $\overline{CAS}$ signals
R_L = 70 Ω, C_L = 300 pF



Test Circuit 2 for microprocessor interface signal
R_L = 500 Ω, C_L = 50 pF



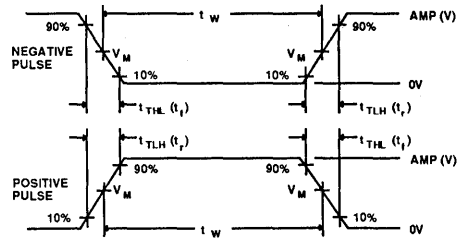
Test Circuit 3 for $\overline{DTACK}$ signal
R_L = 500 Ω, C_L = 50 pF

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F1762

Memory Address Multiplexer

Product Specification

FAST Products

FEATURES

- **Provides refresh and multiplexed row and column addresses for DRAMs**
- **Addressing up to 4MBit DRAMs**
- **Compatible with 74F1761 DIVC and other DRAM controllers**
- **High-performance outputs**
- **High-speed address multiplexing**
- **On-chip 11-bit refresh counter**

TYPE	TYPICAL DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
N74F1762	5.3ns	90mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
Plastic DIP	N74F1762N
PLCC 44	N74F1762A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
RA_0 - RA_{10}	Row address inputs	1.0/1.0	20µA/0.6mA
CA_0 - CA_{10}	Column address inputs	1.0/1.0	20µA/0.6mA
$\overline{MA}_0$ - $\overline{MA}_{10}$	DRAM address outputs	N/A	15mA/20mA
$\overline{REFEN}$	Refresh enable input	1.0/1.0	20µA/0.6mA
MUX	Row/column select input	1.0/1.0	20µA/0.6mA
COUNT	Refresh address count input	1.0/1.0	20µA/0.6mA
MR	Refresh counter reset input	1.0/1.0	20µA/0.6mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state. FAST Unit Loads do not correspond to DRAM Input Loads. See Functional Description for details.

PRODUCT DESCRIPTION

The Signetics Memory Address Multiplexer is designed for use in very high performance dynamic RAM applications. In addition to multiplexing row and column addresses, the device also generates and multiplexes refresh addresses. Though specifically designed to be used with the 74F1761, DRAM and Interrupt Vector Controller, it may be used with any other custom or standard DRAM timing controller chip.

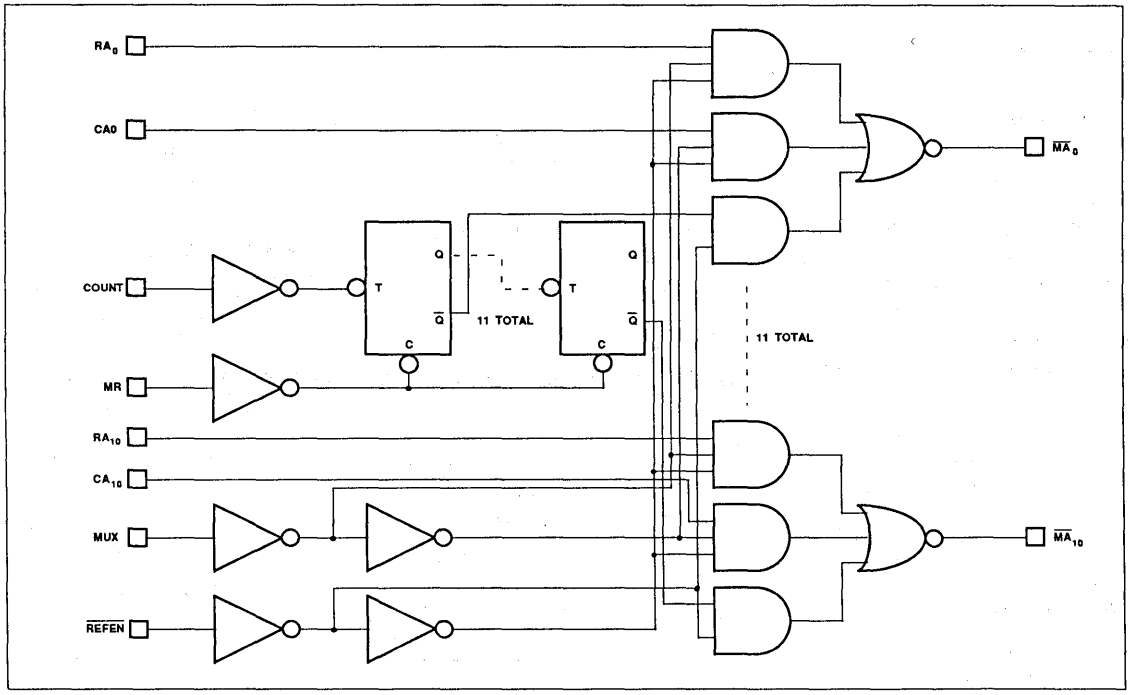
The 'F1762 contains 22 address inputs (RA_0 - RA_{10}) and (CA_0 - CA_{10}), an 11-bit refresh counter, and eleven 3-to-1 multiplexers. The multiplexed row, column or refresh address is output on the eleven high-performance outputs ($\overline{MA}_0$ - $\overline{MA}_{10}$). This enables direct addressing of up to 4MBit dynamic RAMs. Combined with the 'F1761, the 'F1762 provides a complete 4MBit DRAM and interrupt control solution. This solution can control dynamic RAMs with access times down to 40ns.

FUNCTIONAL DESCRIPTION

Functionally, the 'F1762 Memory Address Multiplexer is quite simple. Referring to the logic diagram, the 11-bit Refresh Counter is controlled by the COUNT input, which increments the value stored in the refresh counter on every Low to High transition. When the 'F1762 is used with the 'F1761, this pin is usually connected to the $\overline{REFEN}$ input, so that at the end of every refresh cycle, the refresh counter will be incremented. The Master Reset (MR) input clears the contents of the refresh counter, and may be used for diagnostic testing or initializing after power-up. The eleven 3-to-1 multiplexers are controlled by the MUX and $\overline{REFEN}$ inputs. When $\overline{REFEN}$ is asserted, regardless of the state of the MUX signal, the contents of the internal refresh counter are inverted and asserted at the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs. When $\overline{REFEN}$ is negated, the MUX signal controls which set of address inputs will be propagated to the outputs. With MUX Low, the Row Address inputs (RA_0 - RA_{10}) will be inverted and asserted at the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs. When MUX is High, the Column Addresses (CA_0 - CA_{10}) will be correspondingly asserted.

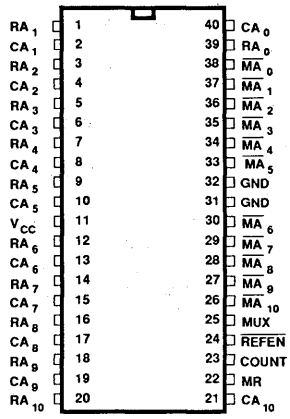
The $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs have specialized drivers to switch 70 ohm transmission lines (typical of DRAM arrays) on the incident edge, thus improving overall system performance. For more information on the driving characteristics, please refer to the DC electrical characteristics and also Signetics application note number AN218.

LOGIC DIAGRAM

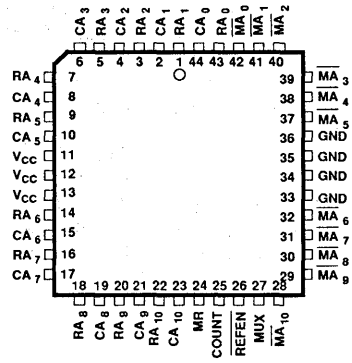


PIN CONFIGURATION

N Package



A Package



PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
RA_0 - RA_{10}	39, 1, 3, 5, 7, 9, 12, 14, 16, 18, 20	43, 1, 3, 5, 7, 9, 14, 16, 18, 20, 22	I	Row Address Inputs. When $\overline{REFEN}$ is negated and MUX is Low, these inputs are inverted and propogated to the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs.
CA_0 - CA_{10}	40, 2, 4, 6, 8, 10, 13, 15, 17, 19, 21	44, 2, 4, 6, 8, 10, 15, 17, 19, 21, 23	I	Column Address Inputs. When $\overline{REFEN}$ is negated and MUX is High, these inputs are inverted and propogated to the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs.
$\overline{MA}_0$ - $\overline{MA}_{10}$	38, 37, 36, 35, 34, 33, 30, 29, 28, 27, 26	42, 41, 40, 39, 38, 37, 32, 31, 30, 29, 28	O	Active Low Memory Address Outputs. These outputs contain the address from either the internal refresh counter, the Row Address inputs, or the Column Address inputs depending on the state of the $\overline{REFEN}$ and MUX signal inputs.
$\overline{REFEN}$	24	26	I	Active Low Refresh Enable Input. When asserted, the address contained in the internal refresh counter is asserted on the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs.
MUX	25	27	I	Row / Column Address Multiplex Input. If $\overline{REFEN}$ is High, this signal will multiplex the inverted Row or Column address inputs on the $\overline{MA}_0$ - $\overline{MA}_{10}$ outputs when it is asserted Low or High respectively.
COUNT	23	25	I	Refresh Counter Count Clock Input. A Low to High transition on this input will increment the internal refresh counter by one regardless of the state of $\overline{REFEN}$ input.
MR	22	24	I	Active High Refresh Counter Master Reset Input. A High level on this input will reset the internal refresh counter to all zeros.
V_{CC}	11	11, 12, 13		+5V ± 10% Supply input.
GND	31, 32	33, 34, 35, 36		Ground.

FUNCTION TABLE

INPUTS						OUTPUTS	COUNTER
MR	COUNT	MUX	$\overline{REFEN}$	RA_n	CA_n	$\overline{MA}_n$	COUNTER CONTENTS
H	X	X	X	X	X	UN*	Reset to 0
L	↑	X	X	X	X	UN*	Increment by 1
H	X	X	L	X	X	L	Reset to 0
L	X	X	L	X	X	COUNTER CONTENTS	Unchanged
L	X	L	H	L	X	H	Unchanged
L	X	L	H	H	X	L	Unchanged
L	X	H	H	X	L	H	Unchanged
L	X	H	H	X	H	L	Unchanged

*The state of the outputs is dependant on the state of the MUX and $\overline{REFEN}$ inputs. The Counter is reset any time MR is High, and if MR is Low, it is incremented on every low to high transistion of COUNT.

UN = Unspecified
H = High level voltage
L = Low level voltage
X = Don't care
↑ = Low-to-High transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	120	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage[3]		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -15mA	±10%V_{CC}	2.5	3.2		V
					±5%V_{CC}	2.7	3.4		V
				I_{OH2} = -35mA	±5%V_{CC}	2.4			V
V_{OL}	Low-level output voltage[4]		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.5	V
					±5%V_{CC}		0.35	0.5	V
				I_{OL2} = 60mA	±5%V_{CC}		0.45	0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Low-level output voltage		V_{CC} = 0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_O[5]	Output current		V_{CC} = MAX, V_{OUT} = 2.25V			-30		-120	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				55	80	mA
		I_{CCL}					90	120	mA

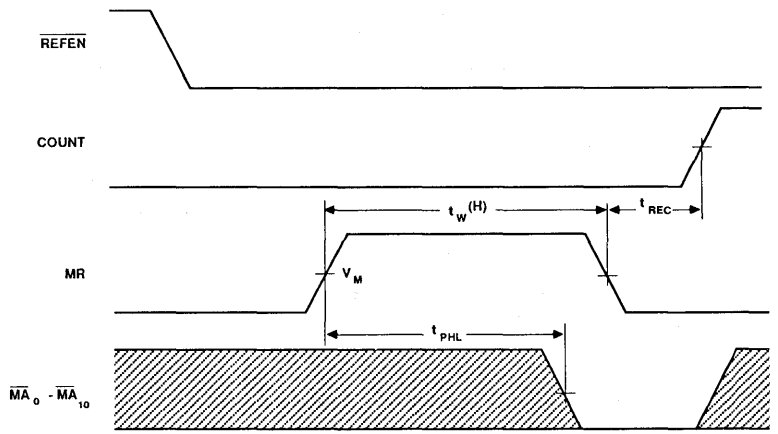
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH2} is the current necessary to guarantee a Low-to-High transition in a 70Ω transmission line.
4. I_{OL2} is the current necessary to guarantee a High-to-Low transition in a 70Ω transmission line.
5. The output conditions have been chosen to produce a current that closely approximates one-half of the short circuit current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 300pF, R_L = 70Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay, MUX(↑) to $\overline{MA}_0$ - $\overline{MA}_{10}$, (column address) valid	Waveform 3	2.0 2.5	4.5 5.0	7.5 8.0	2.0 2.5	8.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay, MUX(↓) to $\overline{MA}_0$ - $\overline{MA}_{10}$, (row address) valid	Waveform 3	4.0 2.0	6.5 4.5	9.5 7.5	3.0 2.0	10.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{REFEN}$ (↑) to $\overline{MA}_0$ - $\overline{MA}_{10}$	Waveform 2	2.0 2.0	4.3 4.5	7.5 8.0	2.0 2.0	8.5 11.0	ns
t_{PLH} t_{PHL}	$\overline{REFEN}$ (↓) to $\overline{MA}_0$ - $\overline{MA}_{10}$ (refresh address) valid	Waveform 2	4.0 2.0	6.9 4.7	10.5 7.5	3.5 2.0	11.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay, RA_0 - RA_{10} to $\overline{MA}_0$ - $\overline{MA}_{10}$	Waveform 4	1.0 0.5	3.0 2.2	6.0 5.0	1.0 0.5	6.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay, CA_0 - CA_{10} to $\overline{MA}_0$ - $\overline{MA}_{10}$	Waveform 5	1.0 0.5	3.0 2.2	6.0 5.0	1.0 0.5	6.5 5.5	ns
t_{PLH} t_{PHL}	COUNT (↑) to $\overline{MA}_0$ - $\overline{MA}_{10}$ (refresh address) valid	Waveform 2	2.0	15.0	35.0	2.0	40.0	ns
t_{PHL}	Propagation delay, MR(↑) to $\overline{MA}_0$ - $\overline{MA}_{10}$	Waveform 1	3.0	5.8	10.5	2.5	11.0	ns
t_w(H)	COUNT pulse width, High	Waveform 2	5.0			5.0		ns
t_w(L)	COUNT pulse width, Low	Waveform 2	5.0			5.0		ns
t_w(H)	MR Pulse width	Waveform 1	5.0			5.0		ns
t_{rec}	Recovery time, MR (↓) to COUNT (↑)	Waveform 1	5.0			5.0		ns

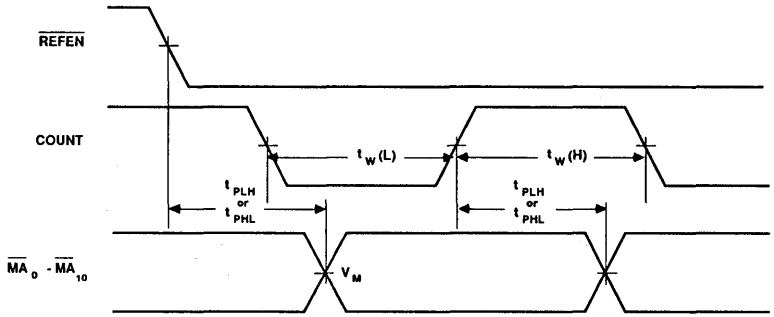
AC WAVEFORMS



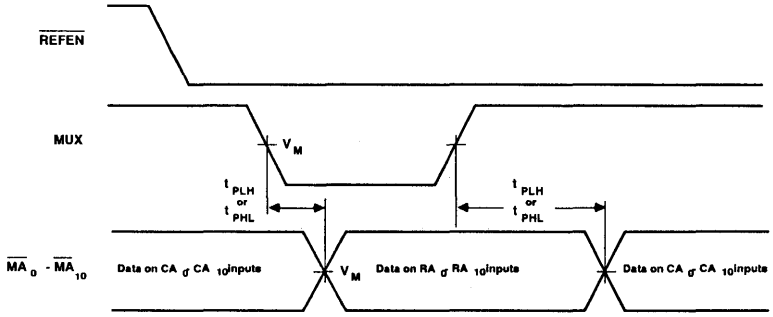
Waveform 1. Waveforms Showing Master Reset Timing

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

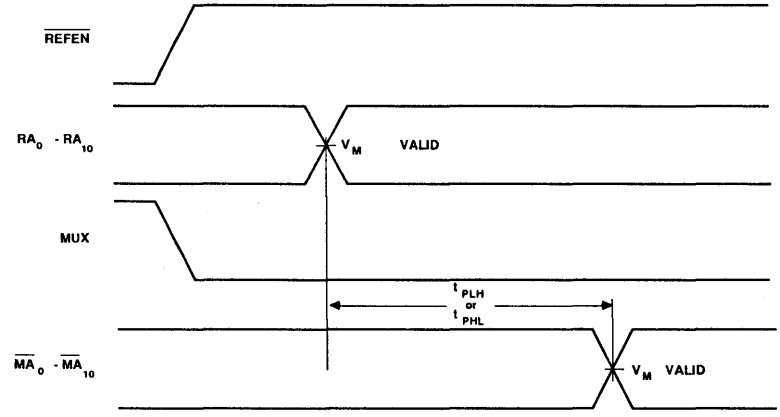
AC WAVEFORMS



Waveform 2. Waveforms Showing Refresh Timing



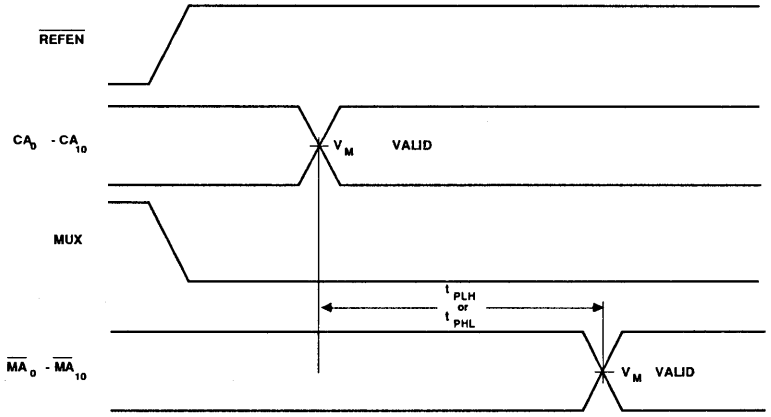
Waveform 3. Waveforms Showing Address Multiplexing Timing



Waveform 4. Waveforms Showing RA_0 - RA_{10} to $\overline{MA}_0$ - to $\overline{MA}_{10}$ Propagation Delay

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

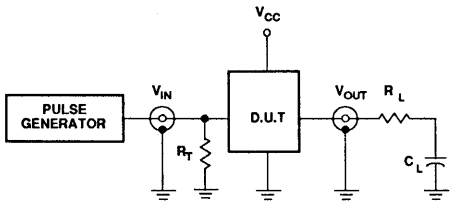
AC WAVEFORMS



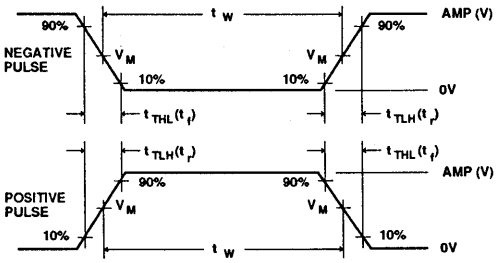
Waveform 4. Waveforms Showing CA_0 - CA_{10} to $\overline{MA}_0$ - to $\overline{MA}_{10}$ Propagation Delay

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F1763 Intelligent DRAM Controller (IDC)

FAST Products

Preliminary Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1763	100 MHz	150 mA

FEATURES

- **DRAM signal timing generator**
- **Automatic refresh circuitry**
- **Selectable row address hold and $\overline{RAS}$ precharge times**
- **Supports page mode accesses**
- **Controls 1 MBit DRAMs**
- **Intelligent burst-mode refresh after page-mode access cycles**

PRODUCT DESCRIPTION

The Signetics Intelligent Dynamic RAM Controller is a 1 MBit, single-port version of the popular 74F764 Dual Port Dynamic RAM Controller. It contains automatic signal timing, address multiplexing and refresh control required for interfacing with dynamic RAMs. Additional features have been added to this device to take advantage of technological advances in Dynamic RAMs. A Page-Mode access pin allows the user to assert $\overline{RAS}$ for the entire access cycle rather than the predefined four-clock-cycle pulse width used for normal random access cycles. In addition, the user has the ability to select the $\overline{RAS}$ precharge time and Row-Address Hold time to fit the particular DRAMs being used. $\overline{DTACK}$ has been modified from previous family parts to become a negative true, tri-stated output. The options for latched or unlatched address are contained on a single device by the addition of an Address Latch Enable ($\overline{ALE}$) input. Finally, a burst refresh monitor has been added to ensure complete refreshing after lengthy page-mode access cycles. With a maximum clock frequency of 100 MHz, the F1763 is capable of driving DRAM arrays with access times down to 40 nsec.

ORDERING INFORMATION

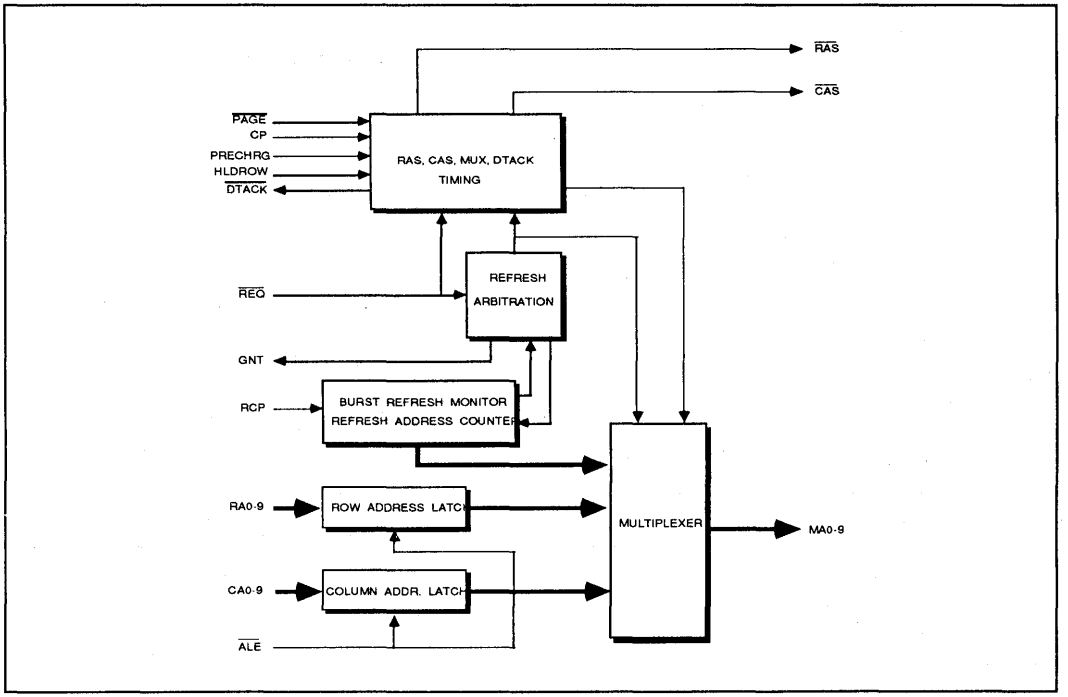
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A=0°C to 70°C
48-Pin Plastic DIP	N74F1763N
44-Pin PLCC	N74F1763A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

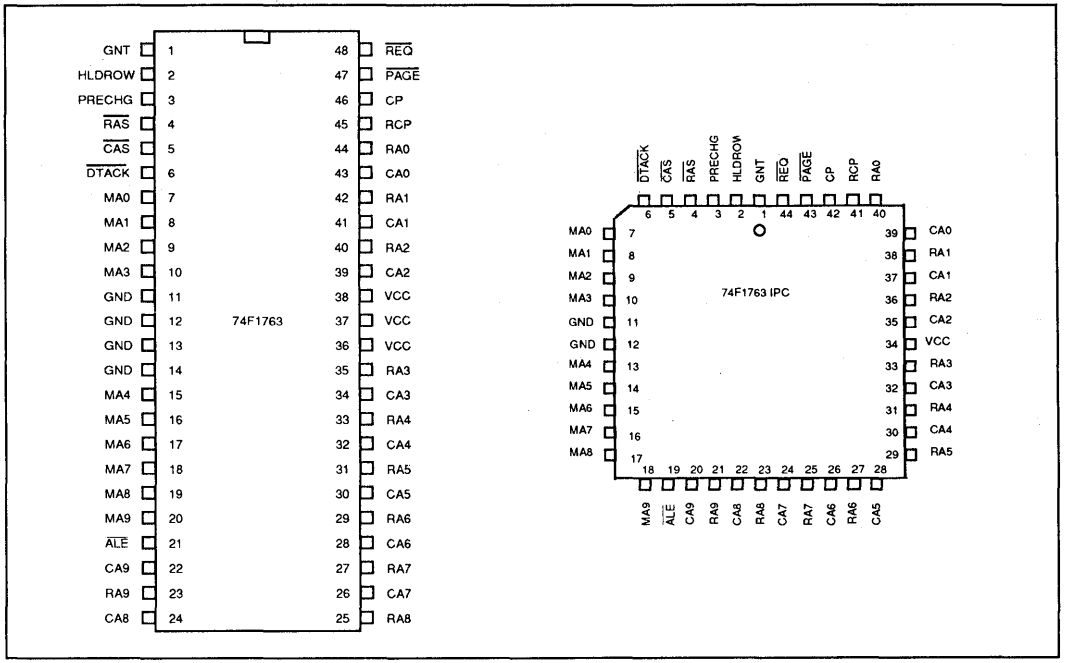
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{REQ}$	DRAM Request Input	1.0/1.0	20 µA/0.6 mA
CP	Clock Input	1.0/1.0	20 µA/0.6 mA
$\overline{PAGE}$	Page Mode Select Input	1.0/1.0	20 µA/0.6 mA
PRECHRG	$\overline{RAS}$ Precharge Select Input	1.0/1.0	20 µA/0.6 mA
HLDROW	Row Hold Select Input	1.0/1.0	20 µA/0.6 mA
$\overline{DTACK}$	Data Transfer Ack. Output	50/80	35 mA/60 mA
GNT	Access Grant Output	50/80	35 mA/60 mA
RCP	Refresh Clock Input	1.0/1.0	20 µA/0.6 mA
RA_0-RA_9	Row Address Inputs	1.0/1.0	20 µA/0.6 mA
CA_0-CA_9	Column Address Inputs	1.0/1.0	20 µA/0.6 mA
$\overline{ALE}$	Address Latch Enable Input	1.0/1.0	20 µA/0.6 mA
$\overline{RAS}$	Row Address Strobe Output	N/A	35 mA/60 mA
$\overline{CAS}$	Column Address Strobe Output	N/A	35 mA/60 mA
MA_0-MA_9	DRAM Address Outputs	N/A	35 mA/60 mA

NOTE:
One (1.0) FAST Unit Load is defined as 20 uA in the HIGH state and 0.6 mA in the LOW state.
FAST Unit Loads do not correspond to DRAM Input Loads. See Functional Description for details.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	PINS		TYPE	NAME AND FUNCTION
	DIP	PLCC		
$\overline{REQ}$	48	44	Input	Active Low Memory Access Request input, must be asserted for the entire DRAM access cycle. $\overline{REQ}$ is sampled on the rising edge of the CP clock.
GNT	1	1	Input	Active High Grant output. When High indicates that a DRAM access cycle has begun. Asserted from the rising edge of the CP clock.
$\overline{PAGE}$	47	43	Input	Active Low Page-Mode Access input. Forces the IDC to keep $\overline{RAS}$ asserted for as long as the $\overline{PAGE}$ input is Low.
HLDROW	2	2	Input	Row Address Hold input. If Low will configure the IDC to maintain the row addresses for a full CP clock cycle after $\overline{RAS}$ is asserted. If High will program the IDC to maintain row addresses for a 1/2 CP clock cycle.
PRECHRG	3	3	Input	$\overline{RAS}$ Precharge input. A Low will program the IDC to guarantee a minimum of 4 CP clock cycles of precharge. A High will guarantee 3 clock cycles of precharge.
CP	46	42	Input	Clock input. Used by the Controller for all timing and arbitration functions.
RCP	45	41	Input	Refresh Clock input. Divided internally by 64 to produce an internal Refresh Request.
$\overline{DTACK}$	2	2	Output	Active Low, 3-state Data Transfer Acknowledge output. Enabled by the $\overline{REQ}$ input and asserted four clock cycles after the assertion of $\overline{RAS}$.
RA_0-RA_9	44,42, 40,35, 33,31, 29,27, 25,23	40, 38, 36, 33, 31, 29, 27, 25, 23, 21	Inputs	Row Address inputs. Propagated to the MA_{0-9} outputs when GNT is asserted.
CA_0-CA_9	43,41, 39,34, 32,30, 28,26, 24,22	39, 37, 35, 32, 30, 28, 26, 24, 22, 20	Inputs	Column Address inputs. Propagated to the MA_{0-9}outputs 1 CP clock cycle after $\overline{RAS}$ is asserted, if HLDROW=0 or 1/2 clock cycle later if HLDROW is 1.
$\overline{RAS}$	4	4	Output	Active Low Row Address Strobe. Asserted for four clock cycles during each refresh cycle. Also asserted for four clock cycles during processor access if the $\overline{PAGE}$ input is false. If PAGE is true, $\overline{RAS}$ is negated upon negation of $\overline{PAGE}$ or $\overline{REQ}$, whichever occurs first.
$\overline{CAS}$	5	5	Output	Active Low Column Address Strobe. Asserted 1 CP clock cycle after $\overline{RAS}$ if HLDROW=1, or 11/2 clock cycle later if HLDROW=0. Negated upon negation of $\overline{REQ}$.
MA_0-MA_9	7-9, 14-19	7-10, 13-18	Output	DRAM multiplexed address outputs. Row and column addresses asserted on these pins during an access cycle. Refresh counter addresses presented on these outputs during refresh cycles.
$\overline{ALE}$	21	19	Input	Active Low Address Latch Enable input. A Low on this pin will cause the address latches to be transparent. A Low to High transition will latch the RA_{0-9} & CA_{0-9} inputs.
V_{CC}	36-38	34		+5 V ± 10% Supply Input.
GND	11-14	11, 12		Ground

FUNCTIONAL DESCRIPTION

The 74F1763 1 Megabit Intelligent DRAM Controller (IDC) is a synchronous device with all signal timing being a function of the CP input clock.

Arbitration:

When a memory access request ($\overline{REQ}$) is asserted and sampled by the IDC, internal arbitration takes place between this request and any pending refresh requests. Refresh always has priority over a memory access cycle and is serviced either immediately or following the current memory access cycle (if any). The IDC will perform a refresh cycle immediately when it becomes due if it is not performing a memory access cycle. If a memory refresh becomes due during a memory access cycle the controller will wait until after its completion before starting a refresh cycle. Similarly, if a memory access request is made when a refresh cycle is in process, the DRAM controller will wait until the cycle is completed before granting access to the requesting processor. If no refresh cycle is in process, and the $\overline{RAS}$ precharge requirement of the DRAM has been satisfied, the access will be granted within one clock cycle of the CP clock . The Grant (GNT) output goes high at this time to indicate the start of a memory access cycle.

Address multiplexing:

The row (RA_{0-9}) and column (CA_{0-9}) address inputs may be latched at any time using the $\overline{ALE}$ input pin. Otherwise the $\overline{ALE}$ input should remain Low to allow the addresses to propagate to the MA0-9 address outputs. When GNT becomes valid, the RA0-9 address inputs will have already propagated to the MA_{0-9} outputs for the row address. At this time, the $\overline{RAS}$ output becomes valid. One or one-half CP clock cycles later (depending on the state of the HLDROW input) the CA0-9 address inputs are propagated to the MA0-9 outputs for a column address. $\overline{CAS}$ is always asserted one and one-half CP clock cycles after $\overline{RAS}$ is asserted. If the $\overline{PAGE}$ input is High, $\overline{RAS}$ will be negated approximately four CP clock cycles after its initial assertion. At this time the $\overline{DTACK}$ output becomes valid indicating the completion of a memory access cycle. The IDC will maintain the state of all its outputs untill the $\overline{REQ}$ input is negated (see AC electrical characteristics).

Row address hold times:

If the HLDROW input of the IDC is High the row address outputs will remain valid 1/2 CP clock cycle after $\overline{RAS}$ is asserted. If the HLDROW input is Low the row address outputs will remain valid one CP clock cycle after $\overline{RAS}$ is asserted.

$\overline{RAS}$ precharge timing:

In order to meet the $\overline{RAS}$ precharge requirement of dynamic RAMs, the controller will hold-off a subsequent $\overline{RAS}$ signal assertion due to a processor access request or a refresh cycle for four or three full CP clock cycles from the previous negation of $\overline{RAS}$, depending on the state of the PRECHG input. If the PRECHG input is Low, $\overline{RAS}$ remains High for at least 4 CP clock cycles. If the PRECHG input is High $\overline{RAS}$ remains High for at least 3 CP clock cycles.

Refresh timing:

The refreshing block of the controller functions by accepting a refresh clock (RCP) and dividing it down internally by 64 to produce an internal refresh request. This refresh request is recognized either immediately or at the end of a running memory access cycle. Due to the possibility that page mode access cycles may be lengthy, the controller keeps track of how many refresh requests have been missed by logging them internally (up to 128) and services any pending refresh requests at the end of the memory access cycle. The controller performs $\overline{RAS}$-only refresh cycles until all pending refresh requests are depleted.

Page-mode access:

Fast accesses to consecutive locations of DRAM can be realized by asserting the $\overline{PAGE}$ input while requesting access to the memory. In this mode, the controller does not automatically negate $\overline{RAS}$ after four CP clock cycles, but keeps it asserted throughout the access cycle. By using external gates, the $\overline{CAS}$ output can be gated on and off while changing the column address inputs to the controller, which will propogate to the MA_{0-9} address outputs and provide a new column address. This is only useful if the $\overline{ALE}$ input is Low, enabling the user to change addresses. This mode can be used with DRAMs that support page or nibble mode addressing.

Output driving characteristics:

Considering the transmission line characteristic of the DRAM arrays, the outputs of the IDC have been designed to provide incident-edge switching, needed in high performance systems. For more information on the driving characteristics, please refer to Signetics application note number AN218.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	120	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATION CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-35	mA
I_{OL}	Low-level output current			60	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -15mA	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
			I_{OH2}[3] = -35mA	±10%V_{CC}	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
			I_{OL2}[4] = 60mA	±10%V_{CC}		0.45	0.80	V
V_{IK}	Input clamp voltage	V_{CC}= MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	A
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_O	Output current[5]	V_{CC} = MAX, V_O= 2.25V			-100		-225	mA
I_{CC}	Supply current (total)	V_{CC}= MAX					220	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH2} is the current necessary to guarantee a Low to High transition in a 70Ω transmission line.
4. I_{OL2} is the current necessary to guarantee a High to Low transition in a 70Ω transmission line.
5. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS

NO	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A=0°C to +70°C V_{cc}=+5.0V ±10% C_L=300pF RL=70Ω			T_A=0°C to +70°C V_{cc}=+5.0V ±10% C_L=300pF RL=70Ω		
			Min	Typ	Max	Min	Max	
1	CP clock period (tcp)		10			10		ns
2	CP clock low time		5			5		ns
3	CP clock high time		5			5		ns
4	RCP clock period		100			100		ns
5	RCP clock low time		10			10		ns
6	RCP clock high time		10			10		ns
7	Setup time $\overline{REQ}$ to CP(↑)		2			2		ns
8	Propagation delay CP(↑) to GNT High		5	10	14	5	16	ns
9	Propagation delay $\overline{REQ}$(↑) to GNT Low		7	12	16	7	18	ns
10	RA0-9, CA0-9 High or Low set-up to $\overline{ALE}$(↑)		2			2		ns
11	$\overline{ALE}$(↑) to RA0-9,CA0-9 High or Low hold		2			2		ns
12	Propagation delay RA0-9,CA0-9 High or Low to MA0-9		4	7	12	4	13	ns
13	Propagation delay $\overline{REQ}$(↑) to MA0-9		7	12	25	7	25	ns
14	Propagation delay CP(↑) to valid MA0-9 (column address)		5	12	17	5	18	ns
15	MA0-9 (row address) hold after $\overline{RAS}$(↓)	HLDROW = 1	1/2tcp			1/2tcp		ns
16	Propagation delay CP(↑) to $\overline{RAS}$(↓)		5	10	14	5	16	ns
17	MA0-9 (row address) hold after $\overline{RAS}$(↓)	HLDROW = 0	1tcp			1tcp		ns
18	$\overline{RAS}$ Low pulse width	PAGE = 1	4tcp			4tcp		ns
19	Propagation delay CP(↑) to $\overline{RAS}$(↑)		6	11	15	6	17	ns
20	Propagation delay $\overline{REQ}$(↑) to $\overline{RAS}$(↑)		8	13	17	8	19	ns
21	Propagation delay CP(↓) to $\overline{CAS}$(↓)		5	10	14	5	16	ns
22	Propagation delay $\overline{PAGE}$(↑) to $\overline{RAS}$(↑)		4	7	12	4	13	ns
23	Propagation delay $\overline{RAS}$(↓) to $\overline{CAS}$(↓)		1.5tcp -5	1.5tcp -2	1.5tcp	1.5tcp -5	1.5tcp	ns
24	Propagation delay $\overline{REQ}$(↑) to $\overline{CAS}$(↑)		6	11	15	6	17	ns

AC ELECTRICAL CHARACTERISTICS

NO	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A=0°C to +70°C V_{cc}=+5.0V ±10% C_L=300pF RL=70Ω			T_A=0°C to +70°C V_{cc}=+5.0V ±10% C_L=300pF RL=70Ω		
			Min	Typ	Max	Min	Max	
25	Set-up time $\overline{PAGE}$(↓) to CP(↑)		2			2		ns
26	Propagation delay CP(↑) to $\overline{DTACK}$(↓)		5	10	14	5	16	ns
27	Propagation delay $\overline{REQ}$(↓) to $\overline{DTACK}$(↑)				12		14	ns
28	Propagation delay $\overline{RAS}$(↓) to $\overline{DTACK}$(↓)			4tcp				ns
29	Propagation delay $\overline{REQ}$(↑) to $\overline{DTACK}$(3-state)				12		14	ns
30	MA0-9 (refresh address) set-up to $\overline{RAS}$(↓)	PRECHRG =1		1/2tcp				ns
31	MA0-9 (refresh address) set-up to $\overline{RAS}$(↓)	PRECHRG = 0		1/2tcp				ns
32	MA0-9 (refresh address) hold after $\overline{RAS}$(↓)	PRECHRG = 1	1tcp	1tcp +20	1tcp +30	1tcp	1tcp +35	ns
33	MA0-9 (refresh address) hold after $\overline{RAS}$(↓)	PRECHRG = 0	1tcp	1tcp +20	1tcp +30	1tcp	1tcp +35	ns
34	$\overline{RAS}$ high (precharge) time	PRECHRG = 0	4tcp			4tcp		ns
35	$\overline{RAS}$ low time	PRECHRG = 0	4tcp			4tcp		ns
36	$\overline{RAS}$ high (precharge) time	PRECHRG = 1	3tcp			3tcp		ns
37	$\overline{RAS}$ low time	PRECHRG = 1	4tcp			4tcp		ns

TIMING DIAGRAM

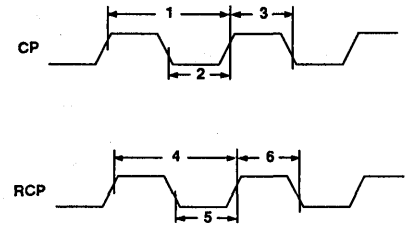


Figure 1: Clock cycle Timing

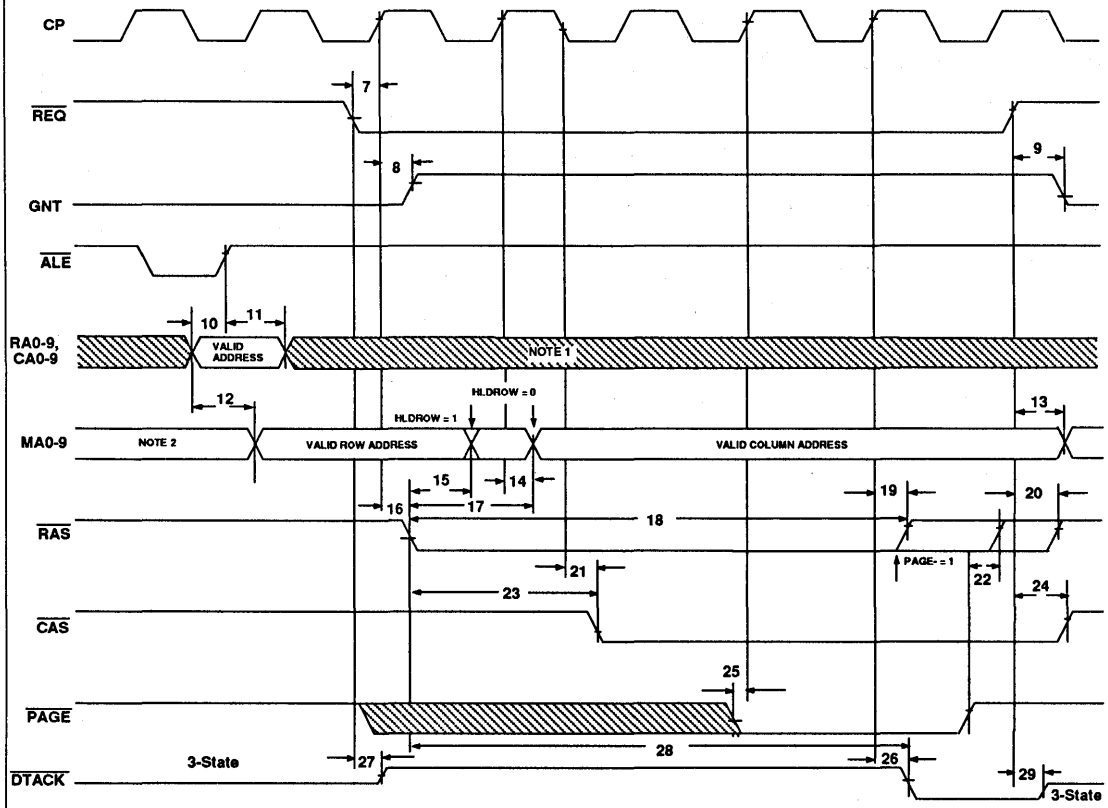


Figure 2: Memory access cycle timing

Note 1: If the RA0-9 & CA0-9 address inputs are not latched, they should remain valid until the corresponding $\overline{REQ}$ is negated.
Note 2: MA0-9 outputs will contain the present row address on the RA0-9 inputs or the last row address latched into the device.

TIMING DIAGRAM

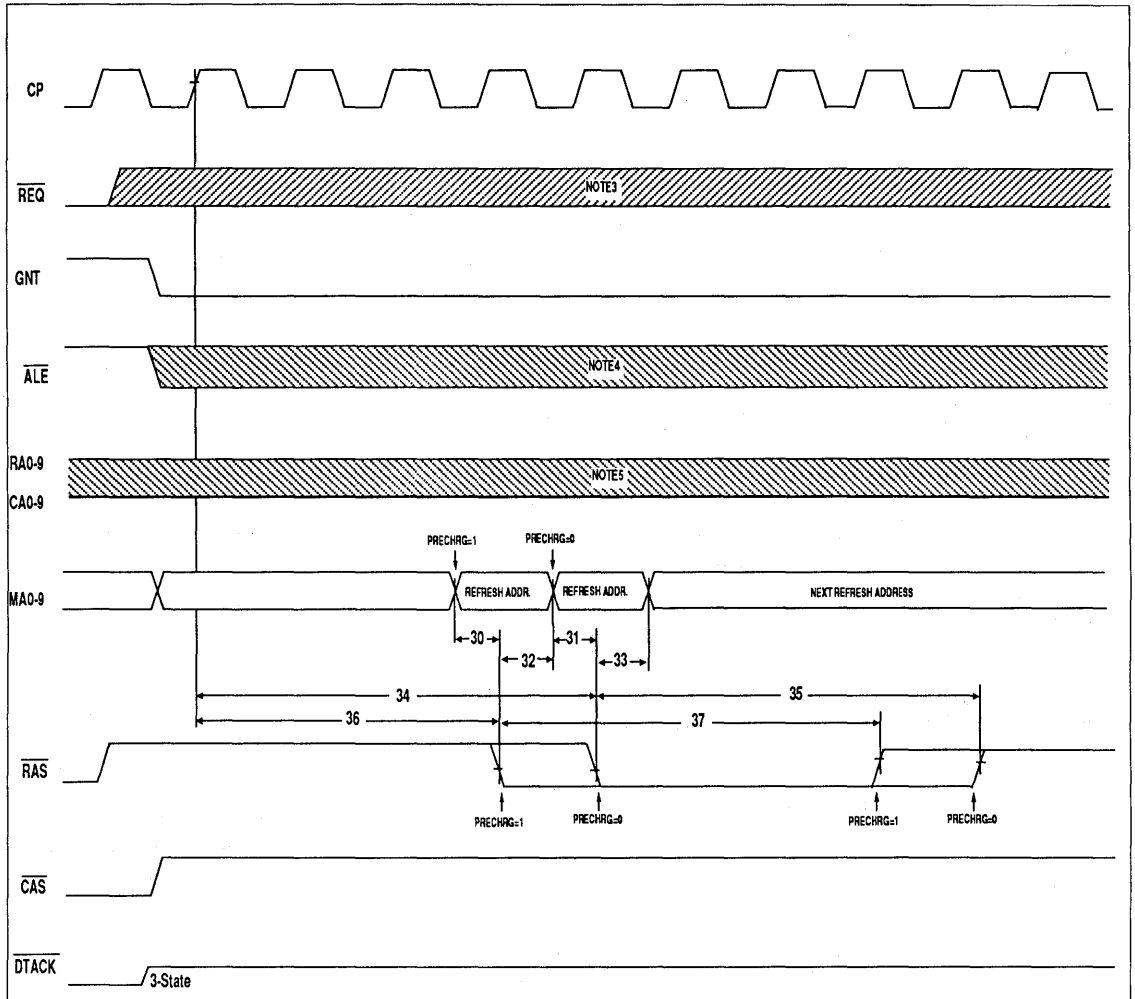


Figure 3: Refresh cycle timing following a memory access cycle

Note 3: $\overline{REQ}$ input is a don't care during a memory refresh cycle. If $\overline{REQ}$ is asserted during a refresh cycle, it will be recognized at the first rising CP clock edge, but GNT will not be asserted until after the completion of the refresh cycle (see Figure 4).

Note 4: RA0-9 & CA0-9 address inputs may be latched at anytime during a memory refresh cycle. However, a memory access cycle will not begin until after the completion of the refresh cycle.

Note 5: RA0-9 & CA0-9 are don't care during a memory refresh cycle.

TIMING DIAGRAM

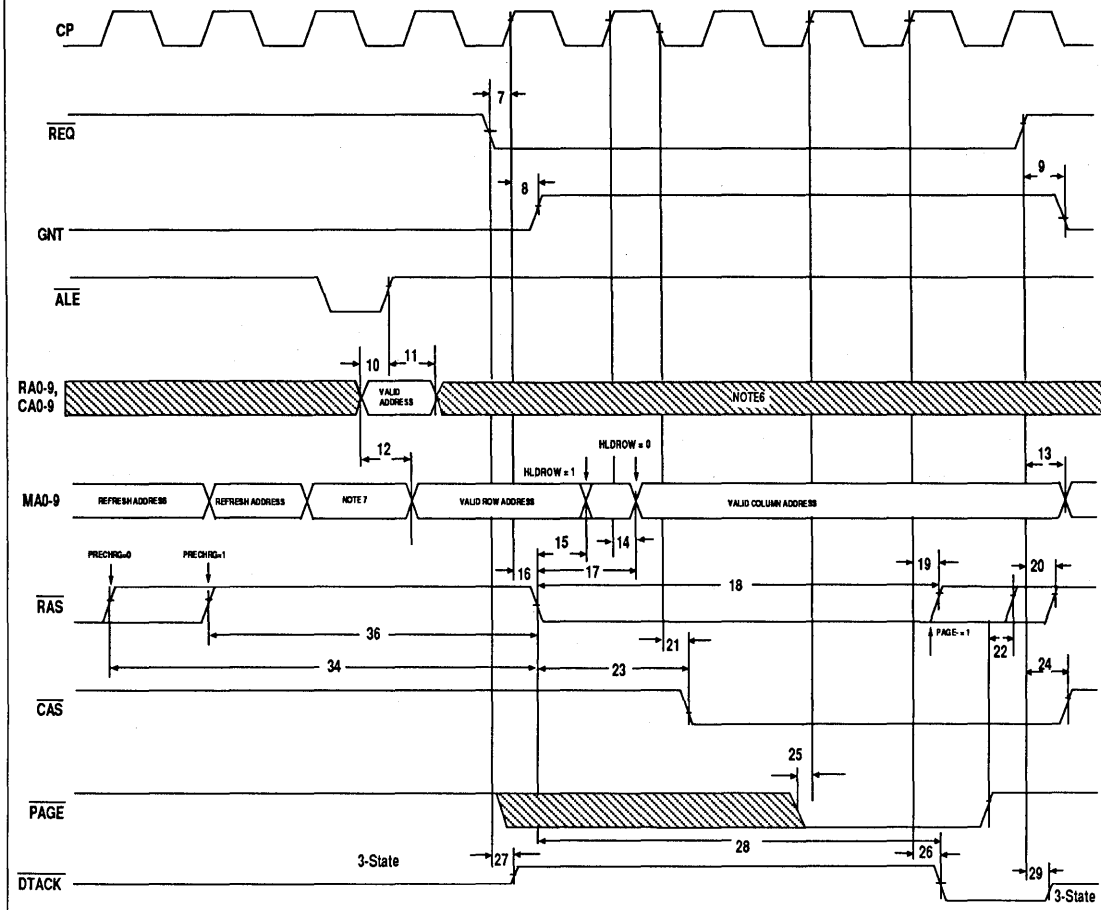


Figure 4: Memory access cycle timing following a refresh cycle

Note 6: If RA0-9 & CA0-9 address inputs are not latched, they should remain valid until the corresponding $\overline{REQ}$ is negated.
Note 7: MA0-9 outputs will contain the present row address on the RA0-9 inputs or the last row address latched into the device.

Signetics

FAST Products

FAST 74F1764/1765 74F1764-1/1765-1 1 Megabit DRAM Dual-Ported Controller

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1764/1765	150MHz	150mA
74F1764-1/1765-1	150MHz	125mA

FEATURES

- **Allows two microprocessors to access the same bank of dynamic RAM**
- **Performs arbitration, signal timing, address multiplexing and refresh**
- **10 address output pins allow direct control of up to 1Mbit dynamic RAMs**
- **External address multiplexing enables control of 4Mbit (or greater) dynamic RAMs**
- **Separate refresh clock allows adjustable refresh timing**
- **74F1764/F1764-1 have on-chip 20-bit address input latch**
- **Allows control of dynamic RAMS with row access times down to 40ns**
- **74F1764/F1765 output drivers designed for incident wave switching**
- **74F1764-1/F1765-1 output drivers designed for first reflected wave switching**

DESCRIPTION

The 74F1764/1765 DRAM Dual-ported Controller is a high speed synchronous dual-port arbiter and timing generator that allows two microprocessors, microcontrollers, or any other memory accessing device to share the same block of DRAM. The device performs arbitration, signal timing, address multiplexing, and refresh address generation, replacing up to 25 discrete devices.

74F1764 vs 74F1765

The 74F1764 though functionally and pin to pin compatible with the 74F1765 differs from the later in that it has an on-chip address input latch. This is useful in systems that have unlatched or multiplexed address and data bus.

ORDERING INFORMATION

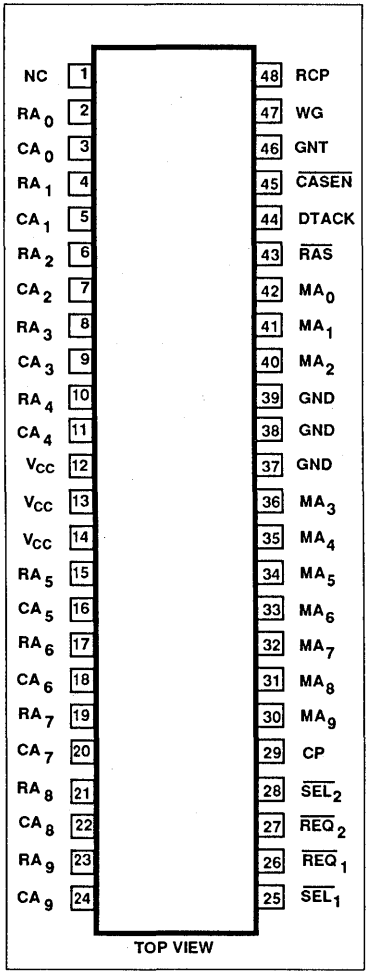
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
48-Pin Plastic DIP	N74F1764N, N74F1765N, N74F1764-1N, N74F1765-1N
44-Pin PLCC	N74F1764A, N74F1765A, N74F1764-1A, N74F1765-1A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

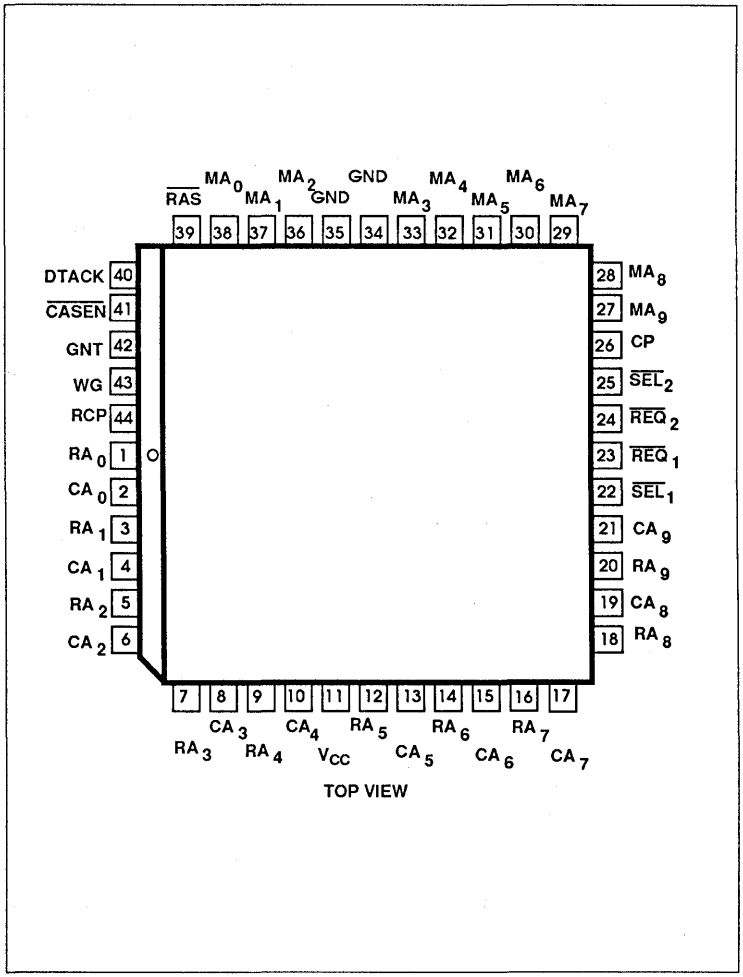
PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
RA_0 - RA_9		Row address inputs	1.0/1.0	20µA/0.6mA
CA_0 - CA_9		Column address inputs	1.0/1.0	20µA/0.6mA
$\overline{REQ_1}$, $\overline{REQ_2}$		Memory access request inputs	1.0/1.0	20µA/0.6mA
CP		Clock input	1.0/1.0	20µA/0.6mA
RCP		Refresh clock input	1.0/1.0	20µA/0.6mA
$\overline{SEL_1}$, $\overline{SEL_2}$	'F1764/1765	Select outputs	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
MA_0 - MA_9	'F1764/1765	Memory address outputs	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
GNT	'F1764/1765	Grant output	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
$\overline{RAS}$	'F1764/1765	Row address strobe output	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
WG	'F1764/1765	Write gate output	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
$\overline{CASEN}$	'F1764/1765	Column address strobe enable output	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA
DTACK	'F1764/1765	Data transfer acknowledge output	750/40	15.0mA/24mA
	'F1764-1/1765-1		1000/13.3	20.0mA/8mA

NOTE:
1.One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state

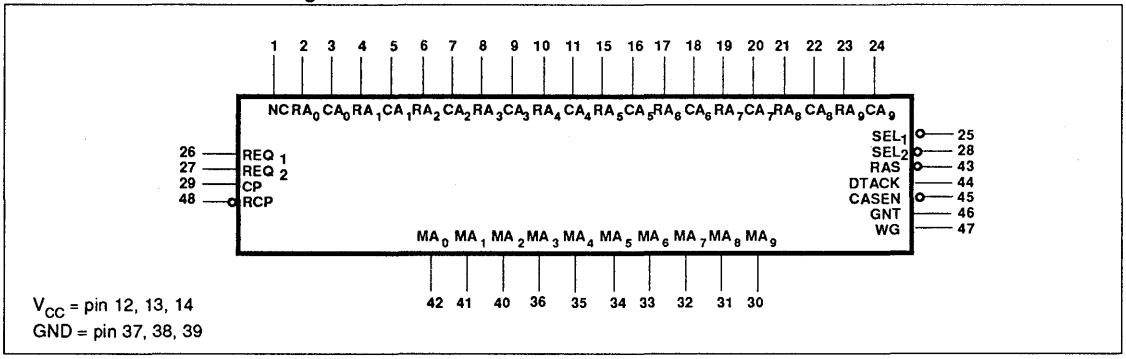
DIP PIN CONFIGURATION



PLCC PIN CONFIGURATION



LOGIC SYMBOL for N Package



PIN DESCRIPTION

SYMBOL	PINS DIP	PINS PLCC	TYPE	NAME AND FUNCTION
RA_0	2	1	Inputs	Address inputs used to generate memory row address
RA_1	4	3		
RA_2	6	5		
RA_3	8	7		
RA_4	10	9		
RA_5	15	12		
RA_6	17	14		
RA_7	19	16		
RA_8	21	18		
RA_9	23	20		
CA_0	3	2	Inputs	Address inputs used to generate memory column address
CA_1	5	4		
CA_2	7	6		
CA_3	9	8		
CA_4	11	10		
CA_5	16	13		
CA_6	18	15		
CA_7	20	17		
CA_8	22	19		
CA_9	24	21		
$\overline{REQ}_1$	26	23	Input	Memory acess request from Microprocessor 1
$\overline{REQ}_2$	27	24	Input	Memory acess request from Microprocessor 2
CP	29	26	Input	Clock input which determines the master timing
RCP	48	44	Input	Refresh clock determines the period of refresh for each row after it is internally divided by 64
$\overline{SEL}_1$	25	22	output	Select signal is activated in response to active REQ_1 input indicating selection of Microprocessor 1
$\overline{SEL}_2$	28	25	output	Select signal is activated in response to active REQ_2 input indicating selection of Microprocessor 2
MA_0	42	38	Outputs	Memory address outputs designed to drive address lines of the DRAM
MA_1	41	37		
MA_2	40	36		
MA_3	36	33		
MA_4	35	32		
MA_5	34	31		
MA_6	33	30		
MA_7	32	29		
MA_8	31	28		
MA_9	30	27		
GNT	46	42	Output	Grant output, activated upon start of a memory access cycle
$\overline{RAS}$	43	39	Output	Row address strobe, used to latch the row address into the bank of DRAM (to be connected directly to the RAS inputs of the DRAMs)
WG	47	43	Output	Write Gate may be gated with the microprocessor's write strobe to perform an early write cycle
$\overline{CASEN}$	45	41	Output	Column address Strobe Address Enable is used to latch the column address into the bank of DRAMs
DTACK	44	40	Output	Data Transfer Acknowledge indicates that the data on the DRAM output lines is valid or the proper access time has been met

ARCHITECTURE

The 74F1764/1765 1 Megabit DRAM dual-ported controller is a synchronous device, with all signal generation being a function of the input clock (CP).

The 'F1764/1765 arbitration logic is divided into two stages. The first stage controls which one of the two $\overline{REQ}$ inputs will be serviced by activating the corresponding $\overline{SEL}$ output. This arbitration takes place irrespective of whether or not a refresh cycle is in progress The arbitration is accomplished by sampling the $\overline{REQ}_1$ and $\overline{REQ}_2$ inputs on differenrt edges of the CP clock. $\overline{REQ}_1$ is sampled on the rising edge and $\overline{REQ}_2$ on the falling edge (refer to Figure 1 and 2).

Therefore, if access to the DRAM is requested by both processors at the same time, the contention is automatically resolved. The internal flip-flops of the device used in the arbitration process have been chosen for their immunity to metastable conditions.

The second stage of arbitration selects between the selected processor and any internal refresh request. Refresh always has priority and is serviced immediately after the current cycle is completed (if needed). This arbitration stage also indicates the start of an access cycle by asserting the GNT output.

The Refresh Clock (RCP) input determines the period for each row. This clock may be held in the High state for external or no refresh applications. When used, a refresh request is internally generated every 64 RCP cycles. The refresh counter is incremented at the end of every refresh cycle, and provides the refresh address.

Since $\overline{SEL}$ outputs indicate which one of the two memory accessing devices has been selected to be serviced, these provide an indication of which processor's address bus should be asserted at the controller address inputs. A Data Transfer Acknowledge (DTACK) signal is generated by the timing logic and either this signal or GNT may be used with the $\overline{SEL}$ outputs to indicate the end or beginning of an access cycle for each processor.

FUNCTIONAL DESCRIPTION

As described earlier, the timing, arbitration, refresh and multiplexing functions provided by the controller are all derived from the CP input. The period of this clock should be set equal to:
(tras (of the DRAM) + 16-5)/4 plus any system guard-band required.

For the 74F1764-1/1765-1 the CP clock input period should be equal to:
(Tras (of the DRAM) + 22-10)/4 plus any system guard-band required.

A microprocessor requests access to the DRAM by activating the appropriate $\overline{REQ}$ input. If a refresh cycle is not in process and the other request input is not active, the $\overline{SEL}$ output corresponding to the active $\overline{REQ}$ input will be asserted to indicate the selected processor. The GNT output then goes High to indicate the start of a memory access cycle. If however, a refresh cycle is in process, and there is only one active $\overline{REQ}$ input, the $\overline{SEL}$ output corresponding to the active input $\overline{REQ}$ will be asserted but the GNT output will not go High until the completion of the refresh cycle (see Figures 8 and 9).

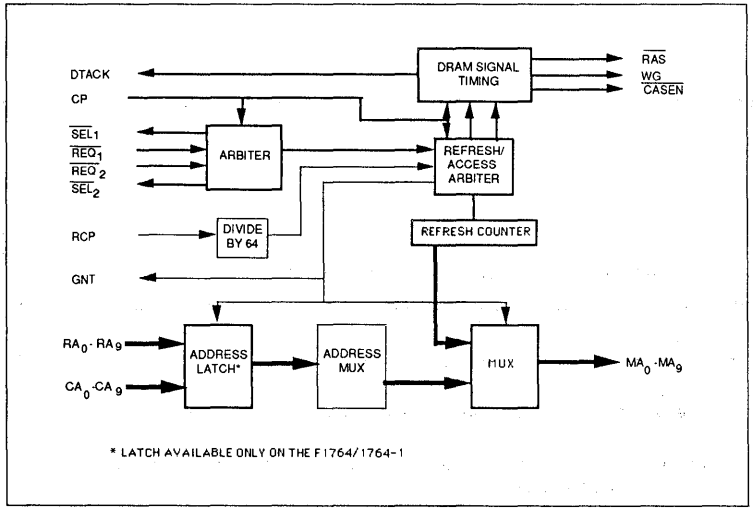
When the device is servicing a memory access cycle and a memory access is also requested by the other processor before the current cycle is completed, the $\overline{SEL}$ output for the other processor will not be issued, though GNT is asserted at that time, because the other processor is performing an access cycle. This will insure that there is no contention on the address bus, i.e., the address bus is not driven by both processors at the same time.

Following the completion of the current memory access cycle, the $\overline{SEL}$ output corresponding to the awaiting $\overline{REQ}$ input will be asserted, followed by the GNT output. If ,however, there are any pending refresh requests, assertion of the GNT output will be held OFF until the refresh has been serviced.

When GNT goes High, the RA_0-RA_9 and CA_0-CA_9 address input to the 'F1764/ 'F1764-1 are latched internally and the RA_0-RA_9 signals are propagated to the MA_0-MA_9 outputs. The address inputs are not latched by the 74F1765/F1765-1 and therefore, RA_0-RA_9 inputs propagate directly to the MA_0-MA_9 outputs.

A half-clock cycle is allowed for the address signals to propagate through to the outputs, after which the $\overline{RAS}$ output is asserted.

BLOCK DIAGRAM



One clock cycle later, the CA_0-CA_9 latch outputs on the 'F1764 and 'F1764-1 or CA_0-CA_9 inputs to the 'F1765 and 'F1765-1 are selected and propagated to the MA_0-MA_9 outputs. The Write Gate (WG) output becomes valid at this time to indicate the proper time to gate the Write signal from the selected processor to the DRAM to perform an Early Write cycle.

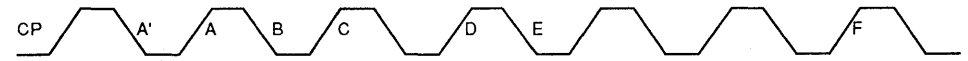
A half-clock cycle is again allowed for the CA_0-CA_9 signals to propagate and stabilize. $\overline{CASEN}$ then becomes valid. $\overline{CASEN}$ can be used as $\overline{CAS}$ output or decoded with higher order address signals to produce multiple $\overline{CAS}$ signals. After $\overline{CASEN}$ is valid, the controller will wait for 2 and one-half clock cycles before negating $\overline{RAS}$, making a total $\overline{RAS}$ pulse width of approximately 4 clock cycles. Since this width matches the standard DRAM access time, the controller next asserts DTACK output, indicating that valid data is on the DRAM data lines or that a memory access cycle is complete. DTACK may be used to assert valid data transfer acknowledge for processors requiring this signal (i.e., the 68000 family of processors).

All controller output signals are held in this final state until the selected processor withdraws its request by driving its $\overline{REQ}$ input High.

When the request is withdrawn, internal synchronization takes place, the controller output signals become inactive, and any pending memory access or refresh cycles are serviced.

A refresh cycle is serviced by propagating the 10 refresh counter address signals to the MA_0-MA_9 outputs. After a half-clock cycle the $\overline{RAS}$ output is asserted for four cycles and then negated for three clock cycles to meet the $\overline{RAS}$ precharge requirements of the DRAMS (see Figures 3 and 4).

TIMING SEQUENCE

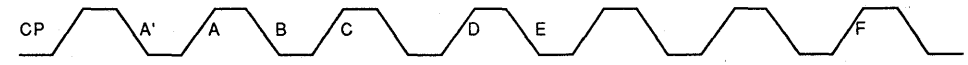


A' $\overline{REQ_2}$ sampled
A $\overline{REQ_1}$ sampled
SEL_1 triggered (SEL_1 triggered by $\overline{REQ_1}$ sample circuitry) ($\overline{REQ_2}$ disabled by SEL_1 circuitry)
B $\overline{GNT}$ triggered
RA_0-RA_9 and CA_0-CA_9 latched (input address latch triggered by GNT circuitry)*
RA_0-RA_9 propagate to MA_0-MA_9 outputs
C $\overline{RAS}$ triggered
D WG triggered
CA_0-CA_9 selected and propagated to MA_0-MA_9 outputs
E $\overline{CASEN}$ triggered
F $\overline{RAS}$ negated
DTACK triggered

* Only on 'F1764 and 'F1764-1

Figure 1. Sequence of Events for $\overline{REQ_1}$ Memory Access Cycle

TIMING SEQUENCE

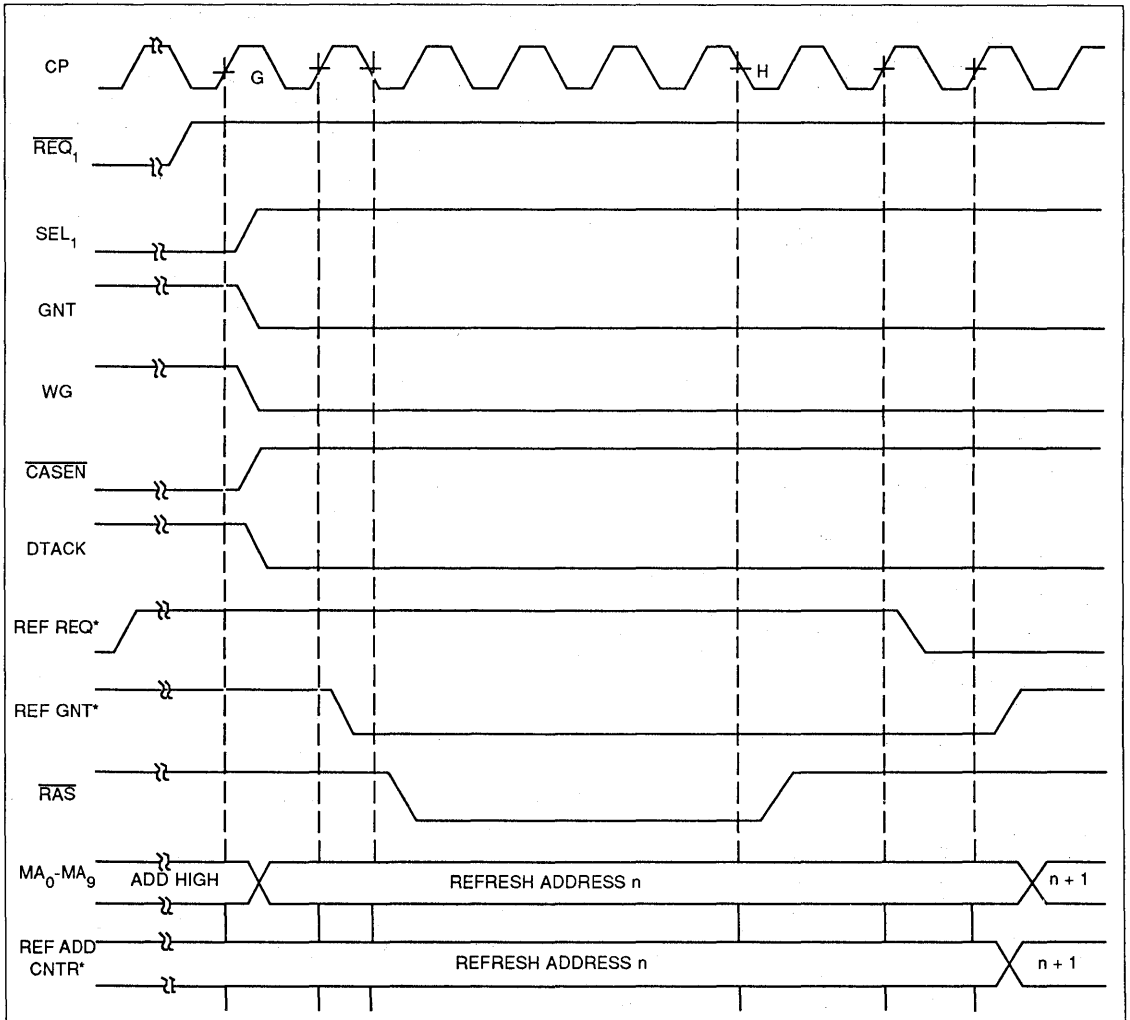


A' $\overline{REQ_2}$ sampled
SEL_1 triggered (SEL_2 triggered by $\overline{REQ_2}$ sampling circuitry)
A $\overline{REQ_1}$ is not sampled(disabled by SEL_2 circuitry)
B $\overline{GNT}$ triggered
RA_0-RA_9 and CA_0-CA_9 latched (input address latch triggered by GNT circuitry)*
RA_0-RA_9 propagate to MA_0-MA_9 outputs
C $\overline{RAS}$ triggered
D WG triggered
CA_0-CA_9 selected and propagated to MA_0-MA_9 outputs
E $\overline{CASEN}$ triggered
F $\overline{RAS}$ negated
DTACK triggered

* Only on 'F1764 and 'F1764-1

Figure 2. Sequence of Events for $\overline{REQ_2}$ Memory Access Cycle

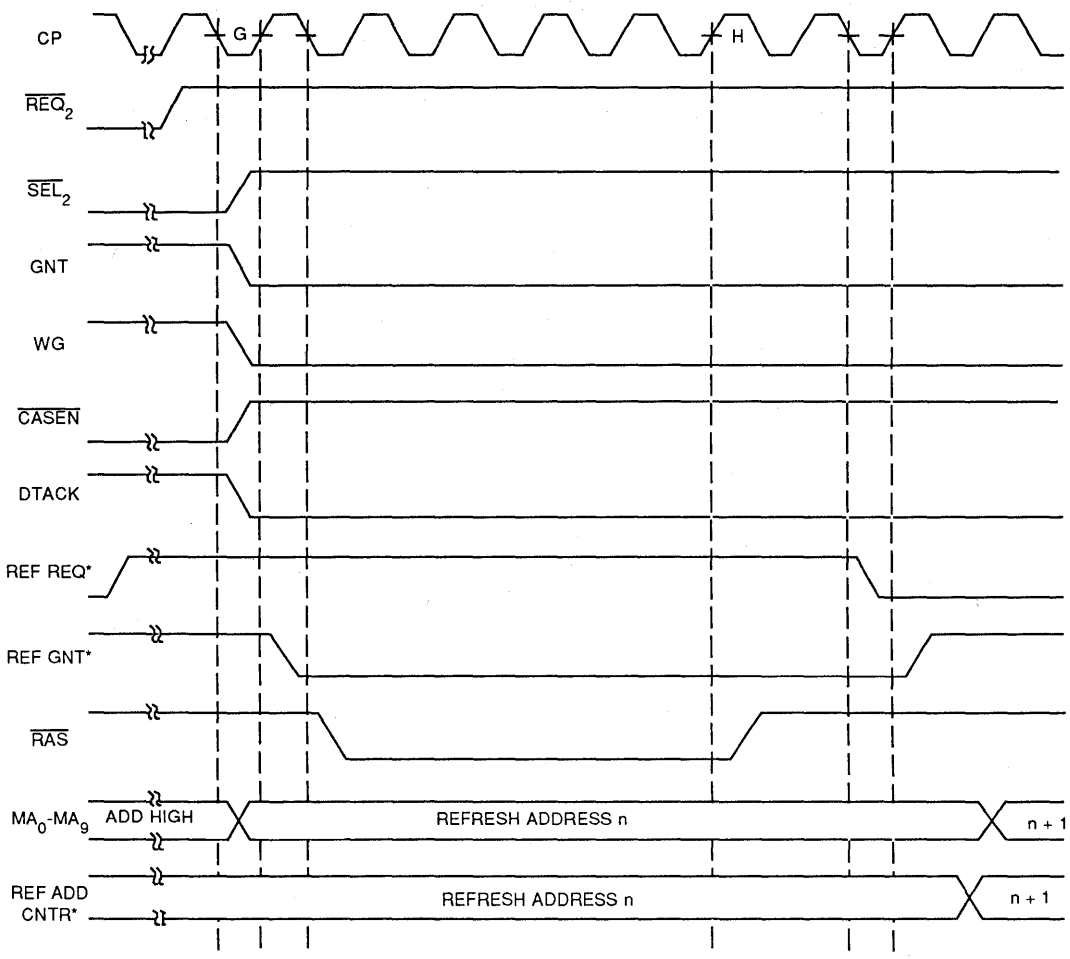
TIMING DIAGRAM



Note: *= These are internal signlas only

Figure 3. Refresh Cycle Timing Following a $\overline{REQ}_1$ Memory Access Cycle

TIMING DIAGRAM



Note: *= These are internal signlas only

Figure 4. Refresh Cycle Timing Following a $\overline{REQ}_2$ Memory Access Cycle

Using 74F1764/1765 AND 74F1764-1/ 1765-1 TO ADDRESS 4MBIT DRAMS

The addressing capabilities of the 1 Megabit DRAM dual-ported controllers can be extended to address 4Mbit (or greater) DRAMs by using an external multiplexer to multiplex additional address bits.

Figure 5 shows an application, using an external 2-to-1 multiplexer to address 4Mbit dynamic RAMs. The 10-bit internal refresh counter of the controller provides 1024 row addresses which more than meet the refreshing needs for most industry standard 4Mbit DRAMs. Therefore, it is unnecessary to provide for any additional refresh address bits for DRAMs with up to 1024 rows.

Additional address bits (for larger DRAMs) may also be multiplexed externally as long as the DRAM refreshing requirements do not exceed 1024 row addresses.

The WG output of the controller should be used to multiplex between the external row and column addresses. However, it is important that the propagation delay through the external multiplexer does not cause column address setup violations on the dynamic RAM.

APPLICATION

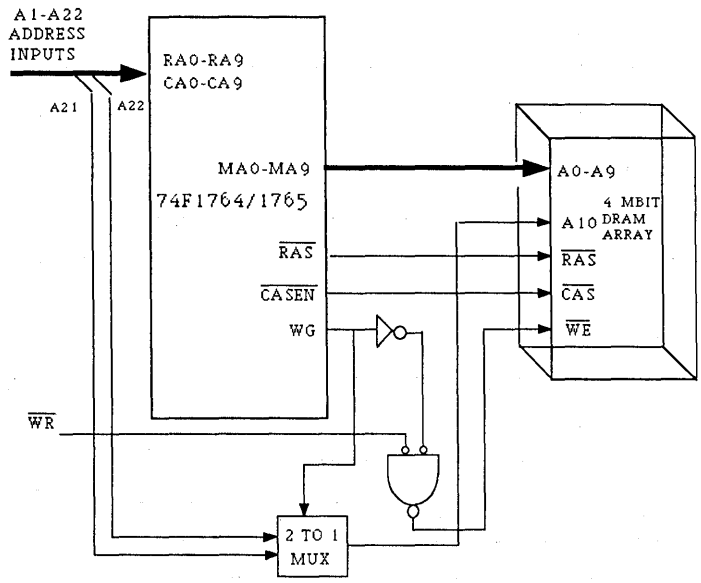


Figure 5. Using the Controller to Address 4Mbit DRAMS

TIMING DIAGRAM

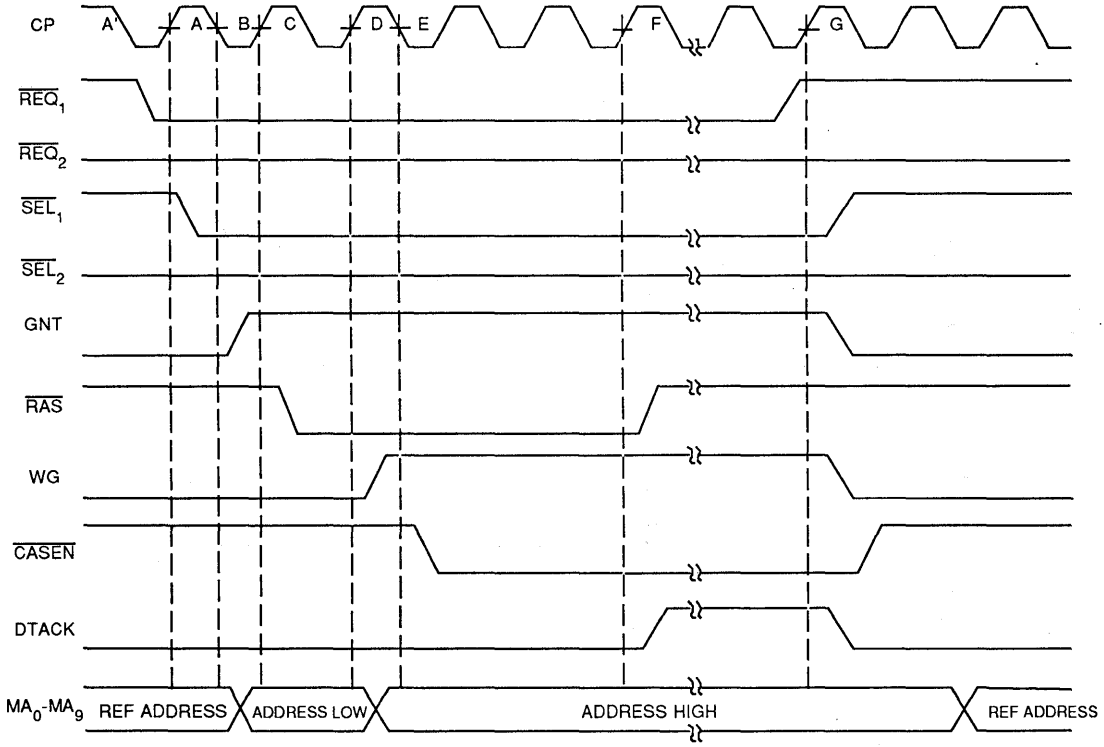


Figure 6. Request 1 ($\overline{REQ_1}$) Memory Access Cycle Timing

TIMING DIAGRAM

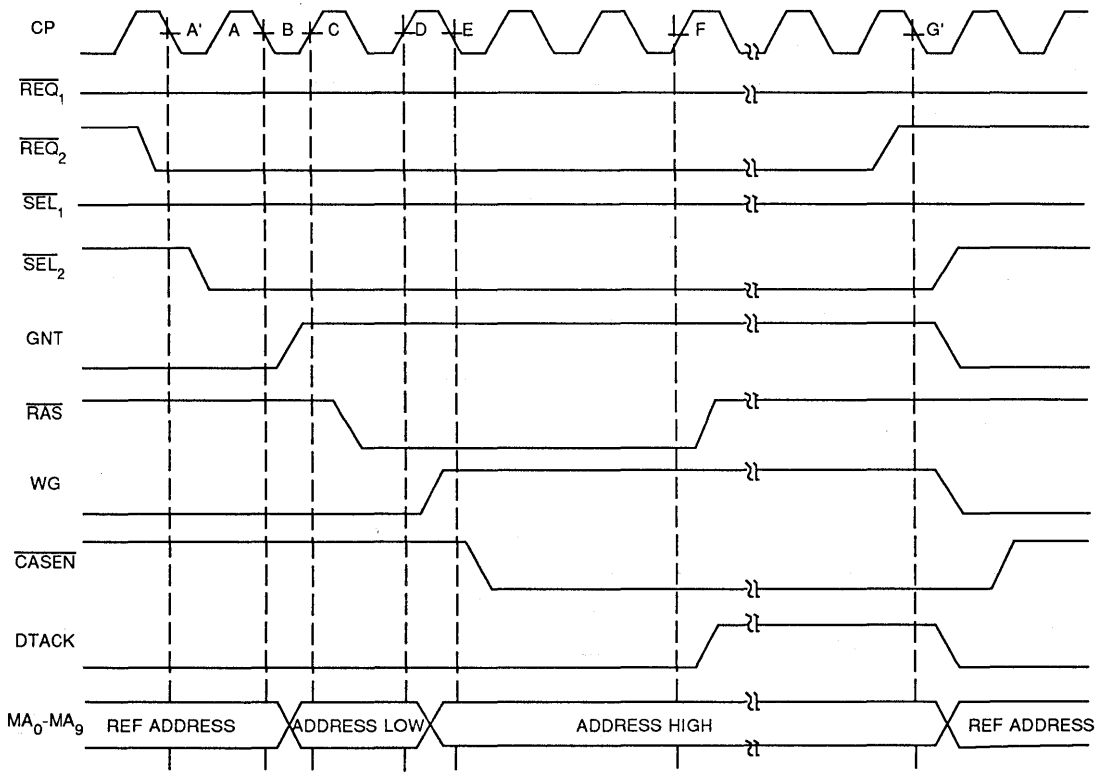


Figure 7. Request 2 ($\overline{REQ_2}$) Memory Access Cycle Timing

TIMING DIAGRAM

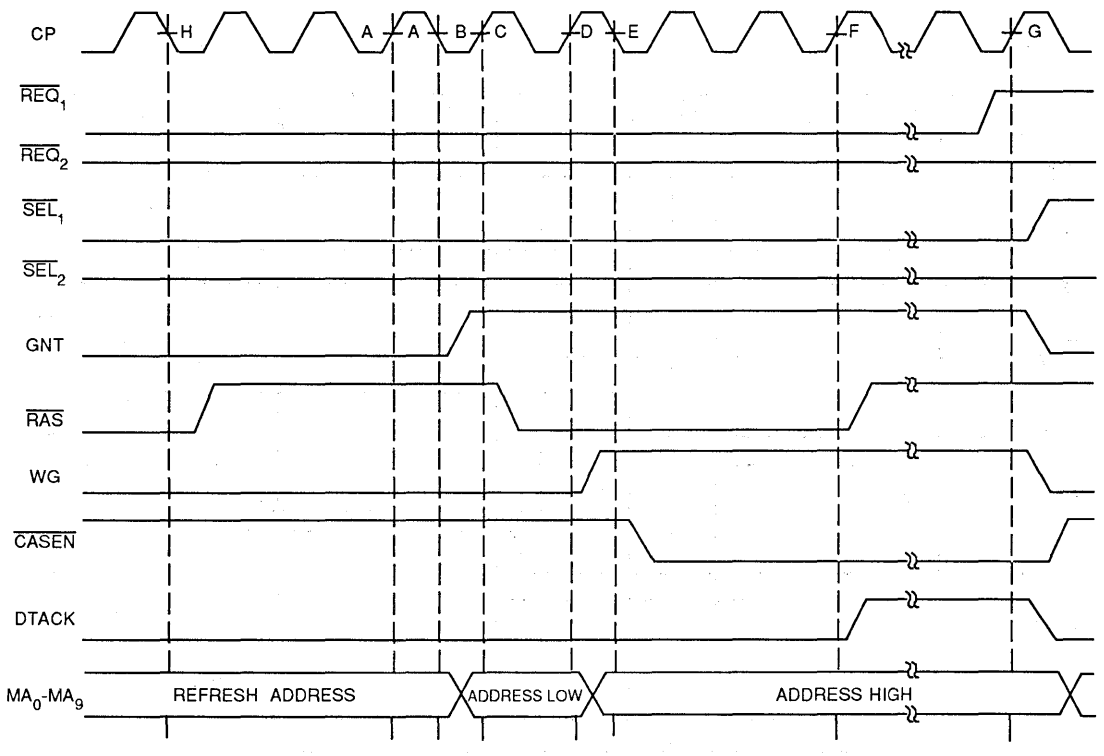


Figure 8. Request 1 ($\overline{REQ_1}$) Memory Access Cycle Timing Following a refresh Cycle

TIMING DIAGRAM

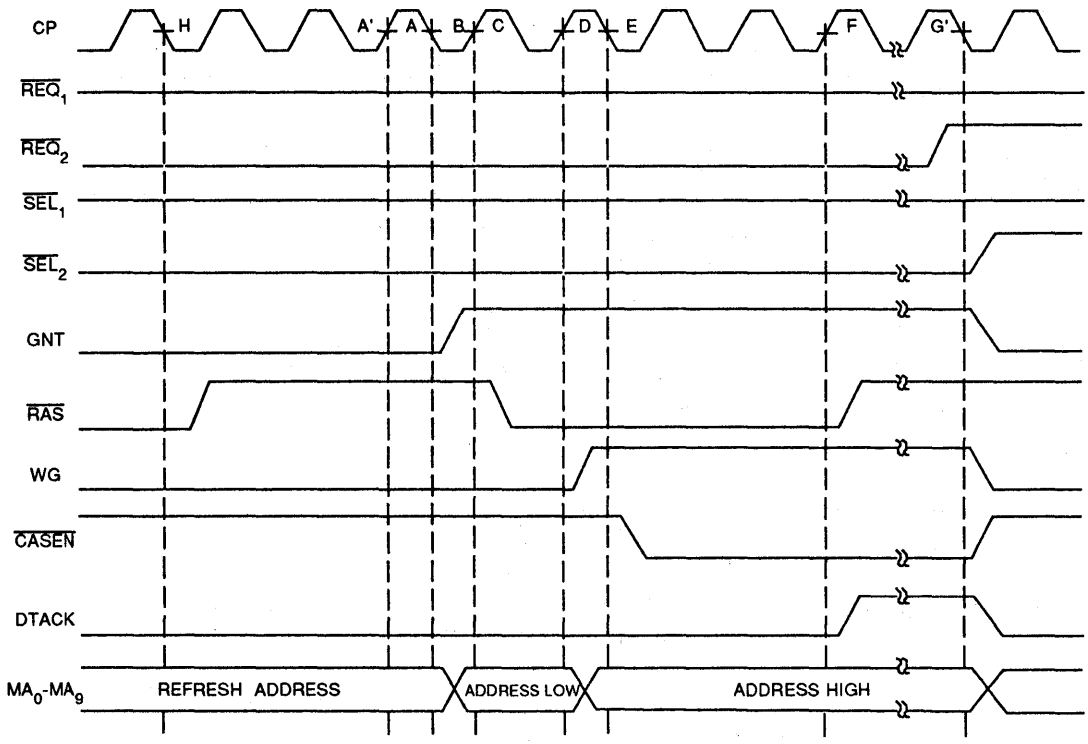


Figure 9. Request 2 ($\overline{REQ}_2$) Memory Access Cycle Timing Following a refresh Cycle

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	500	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current[1]	74F1764/74F1765			-15	mA
		74F1764-1/74F1765-1			-20	mA
I_{OL}	Low-level output current[1]	74F1764/74F1765			24	mA
		74F1764-1/74F1765-1			8	mA
T_A	Operating free-air temperature range		0		70	°C

NOTES:
1. Transient currents will exceed these values in actual operation. Please refer to Appendix A for a detailed discussion.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS			UNIT
							Min	Typ[2]	Max	
V_{OH}	High-level output voltage		74F1764 74F1765	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-15mA	±10%V_{CC}	2.5			V
						±5%V_{CC}	2.7			V
V_{OH2}[3]					I_{OH2}[3]=-35mA	±5%V_{CC}	2.4			V
V_{OH}			74F1764-1 74F1765-1	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-20mA	±10%V_{CC}	2.4	2.7		V
						±5%V_{CC}	2.6	3.0		V
V_{OL}	Low-level output voltage		74F1764 74F1765	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
						±5%V_{CC}		0.35	0.50	V
					I_{OL2}[4]=60mA	±5%V_{CC}		0.45	0.80	V
			74F1764-1 74F1765-1	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=8mA	±10%V_{CC}		0.30	0.50	V
						±5%V_{CC}		0.30	0.50	V
V_{OH2}[3]					I_{OL2}[3]=75mA	±5%V_{CC}		2.1	2.5	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} =MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} =MAX, V_I = 0.5V					-0.6	mA
I_{OS}	Short-circuit output current[5]		74F1764 74F1765	V_{CC} =MAX			-100		-225	mA
			74F1764-1 74F1765-1	V_{CC} =MAX			-60	100	-150	mA
I_{CC}	Supply current (total)	I_{CCH}	74F1764 74F1765	V_{CC} =MAX				150	200	mA
		I_{CCL}						165	210	mA
		I_{CCH}	74F1764-1 74F1765-1					120	165	mA
		I_{CCL}						125	170	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Refer to Appendix A.
4. Refer to Appendix A.
5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 74F1764/74F1765

SYMBOL	PARAMETER	TEST CONDITION (Refer to Timing Diagrams)	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 300pF, R_L = 70Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		100	150		100		MHz
t_{PLH}	Propagation delay, CP(G) to $\overline{SEL}_1$		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(A) to $\overline{SEL}_1$		5.0	10.0	14.0	5.0	16.0	ns
t_{PLH}	Propagation delay, CP(G') to $\overline{SEL}_2$		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(A') to $\overline{SEL}_2$		5.0	10.0	14.0	5.0	16.0	ns
t_{PLH}	Propagation delay, CP(B) to GNT		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(G or G') to GNT		5.0	10.0	15.0	5.0	16.0	ns
t_{PLH} t_{PHL}	Propagation delay CP(B) to MA (row address)		5.0 5.0	12.0 11.0	17.0 15.0	5.0 5.0	18.0 16.0	ns
t_{PLH}	Propagation delay, CP(F or H) to $\overline{RAS}$		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(C) to $\overline{RAS}$		5.0	10.0	14.0	5.0	16.0	ns
t_{PLH}	Propagation delay, CP(D) to WG		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(G or G') to WG		8.0	13.0	17.0	8.0	18.0	ns
t_{PLH} t_{PHL}	Propagation delay CP(D) to MA (column address)		5.0 5.0	12.0 10.0	17.0 15.0	5.0 5.0	18.0 16.0	ns
t_{PLH}	Propagation delay, CP(G or G') to $\overline{CASEN}$		7.0	17.0	23.0	7.0	25.0	ns
t_{PHL}	Propagation delay, CP(E) to $\overline{CASEN}$		5.0	10.0	14.0	5.0	16.0	ns
t_{PLH}	Propagation delay, CP(F) to DTACK		5.0	10.0	14.0	5.0	16.0	ns
t_{PHL}	Propagation delay, CP(G or G') to DTACK		6.0	13.0	17.0	5.0	18.0	ns
t_{PLH} t_{PHL}	Propagation delay RA_0-RA_9, CA_0-CA_9 to MA_0-MA_9	74F1765 only	4.0 2.0	7.0 5.0	12.0 8.0	4.0 4.0	13.0 9.0	ns

AC SETUP REQUIREMENTS for 74F1764/74F1765

SYMBOL	PARAMETER		TEST CONDITION (Refer to Timing Diagrams)	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 300pF, R_L = 70Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{REQ}_1$, $\overline{REQ}_2$ to CP			2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{REQ}_1$, $\overline{REQ}_2$ to CP			2.0 2.0			3.0 3.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low RA_0-RA_9, CA_0-CA_9 to CP	74F1764 only		-4.0[1] -4.0			-5.0 -5.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low RA_0-RA_9, CA_0-CA_9 to CP	74F1764 only		5.0 5.0			5.0 5.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low			5.0 5.0			5.0 5.0		ns
$t_w(H)$ $t_w(L)$	RCP Pulse width, High or Low			10.0 10.0			10.0 10.0		ns

NOTES:

1. These numbers indicate that the address inputs have a negative setup time and could not be valid 4ns after the falling edge of the CP clock. It is suggested that $\overline{SEL}_2$ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of $\overline{SEL}_1$ to enable Address Bus 1. This will insure that setup time for Address Bus 1 is not violated.

AC ELECTRICAL CHARACTERISTICS for 74F1764-1/74F1765-1

SYMBOL	PARAMETER	TEST CONDITION (Refer to Timing Diagrams)	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 300pF, R_L = 70Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		150	175		100		MHz
t_{PLH}	Propagation delay, CP(G) to $\overline{SEL_1}$		9.0	12.0	15.0	8.0	17.0	ns
t_{PHL}	Propagation delay, CP(A) to $\overline{SEL_1}$		13.0	16.0	20.0	12.0	22.0	ns
t_{PLH}	Propagation delay, CP(G') to $\overline{SEL_2}$		9.0	12.0	15.0	8.0	17.0	ns
t_{PHL}	Propagation delay, CP(A') to $\overline{SEL_2}$		13.0	16.0	20.0	12.0	22.0	ns
t_{PLH}	Propagation delay, CP(B) to GNT		9.0	12.0	14.0	8.0	16.0	ns
t_{PHL}	Propagation delay, CP(G or G') to GNT		20.0	23.0	26.0	17.0	28.0	ns
t_{PLH} t_{PHL}	Propagation delay CP(B) to MA (row address)		11.0 14.0	14.0 18.0	17.0 22.0	10.0 13.0	19.0 24.0	ns
t_{PLH}	Propagation delay, CP(F or H) to $\overline{RAS}$		11.0	14.0	16.0	10.0	18.0	ns
t_{PHL}	Propagation delay, CP(C) to $\overline{RAS}$		13.0	17.0	20.0	12.0	22.0	ns
t_{PLH}	Propagation delay, CP(D) to WG		9.0	11.0	14.0	8.0	16.0	ns
t_{PHL}	Propagation delay, CP(G or G') to WG		20.0	23.0	26.0	19.0	26.0	ns
t_{PLH} t_{PHL}	Propagation delay CP(D) to MA (column address)		12.0 14.0	14.0 18.0	17.0 21.0	11.0 13.0	19.0 23.0	ns
t_{PLH}	Propagation delay, CP(G or G') to $\overline{CASEN}$		14.0	17.0	20.0	12.0	22.0	ns
t_{PHL}	Propagation delay, CP(E) to $\overline{CASEN}$		14.0	16.0	19.0	13.0	21.0	ns
t_{PLH}	Propagation delay, CP(F) to DTACK		10.0	12.0	15.0	9.0	17.0	ns
t_{PHL}	Propagation delay, CP(G or G') to DTACK		20.0	23.0	26.0	19.0	28.0	ns
t_{PLH} t_{PHL}	Propagation delay RA_0-RA_9, CA_0-CA_9 to MA_0-MA_9 ('F1765-1 only)		9.0 9.0	11.0 12.0	14.0 15.0	8.0 8.0	16.0 17.0	ns

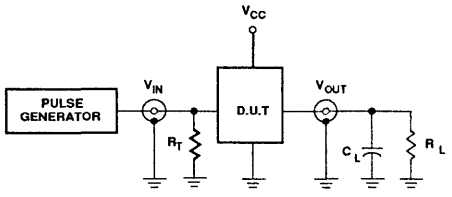
AC SETUP REQUIREMENTS for 74F1784-1/74F1765-1

SYMBOL	PARAMETER	TEST CONDITION (Refer to Timing Diagrams)	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 300pF, R_L = 70Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 300pF, R_L = 70Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low $\overline{REQ_1}$, $\overline{REQ_2}$ to CP		3.0 3.0	1.0 1.0		4.0 4.0		ns
t_h(H) t_h(L)	Hold time, High or Low $\overline{REQ_1}$, $\overline{REQ_2}$ to CP		2.0 2.0	0 0		3.0 3.0		ns
t_s(H) t_s(L)	Setup time, High or Low RA_0-RA_9, CA_0-CA_9 to CP (74F1764-1 only)		0 0	-1.0[1] -1.0[1]		1.0 1.0		ns
t_h(H) t_h(L)	Hold time, High or Low RA_0-RA_9, CA_0-CA_9 to CP (74F1764-1 only)		5.0 5.0	3.0 3.0		6.0 6.0		ns
t_w(H) t_w(L)	CP Pulse width, High or Low		5.0 5.0	3.0 3.0		5.0 5.0		ns
t_w(H) t_w(L)	RCP Pulse width, High or Low		5.0 5.0			5.0 5.0		ns

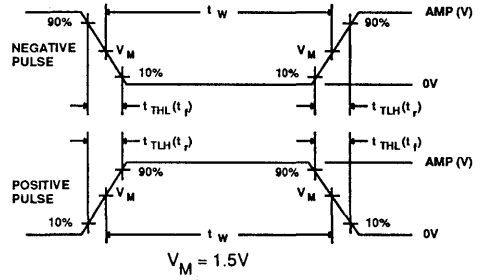
NOTES:

1. These numbers indicate that the address inputs have a negative setup time and could not be valid 4ns after the falling edge of the CP clock. It is suggested that $\overline{SEL_2}$ be used to enable Address Bus 2 and the opposite polarity of the same be used, instead of $\overline{SEL_1}$ to enable Address Bus 1. This will insure that setup time for Address Bus 1 is not violated.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

APPLICATIONS

The 1 Megabit DRAM dual-ported controller can be deigned into a wide range of single and dual-port interface configurations. The processors could be general or special-purpose (microcontrollers) and the data bus may differ in size.

Figure 10 shows two 68000 processors sharing a 4Meg X 8 (two banks each consisting of sixteen 1 Meg devices) memory. Since the 68000 does not have a multiplexed address and data bus, the 'F 1765/'F1765-1 is appropriate.

Address bit (A21) from either the two 68000 processors distinguishes between Memory Banks A and B. Where Bank A consists of Upper Data Byte A (UDBA) and Lower Data Byte A (LDBA) and Bank B consists of Upper Data Byte B (UDBB) and Lower Data Byte B (LDBB).

Upper and Lower Data Strobes (UDS and LDS) from either of the two 68000 determine whether a byte or word transfer will take place. The additional circuitry is to ensure that DTACK to the 68000 is asserted only when it is selected.

Figure 11 shows two 8086 processors sharing 1 Mbyte (two banks each consisting of sixteen 256K X 1 devices) of dynamic RAM. Using 'F1764/1764-1 in this application may eliminate the need for an external address latch.

Similarly Figure 12 shows two 6020 processors sharing 4Mbyte of memory.

APPLICATION

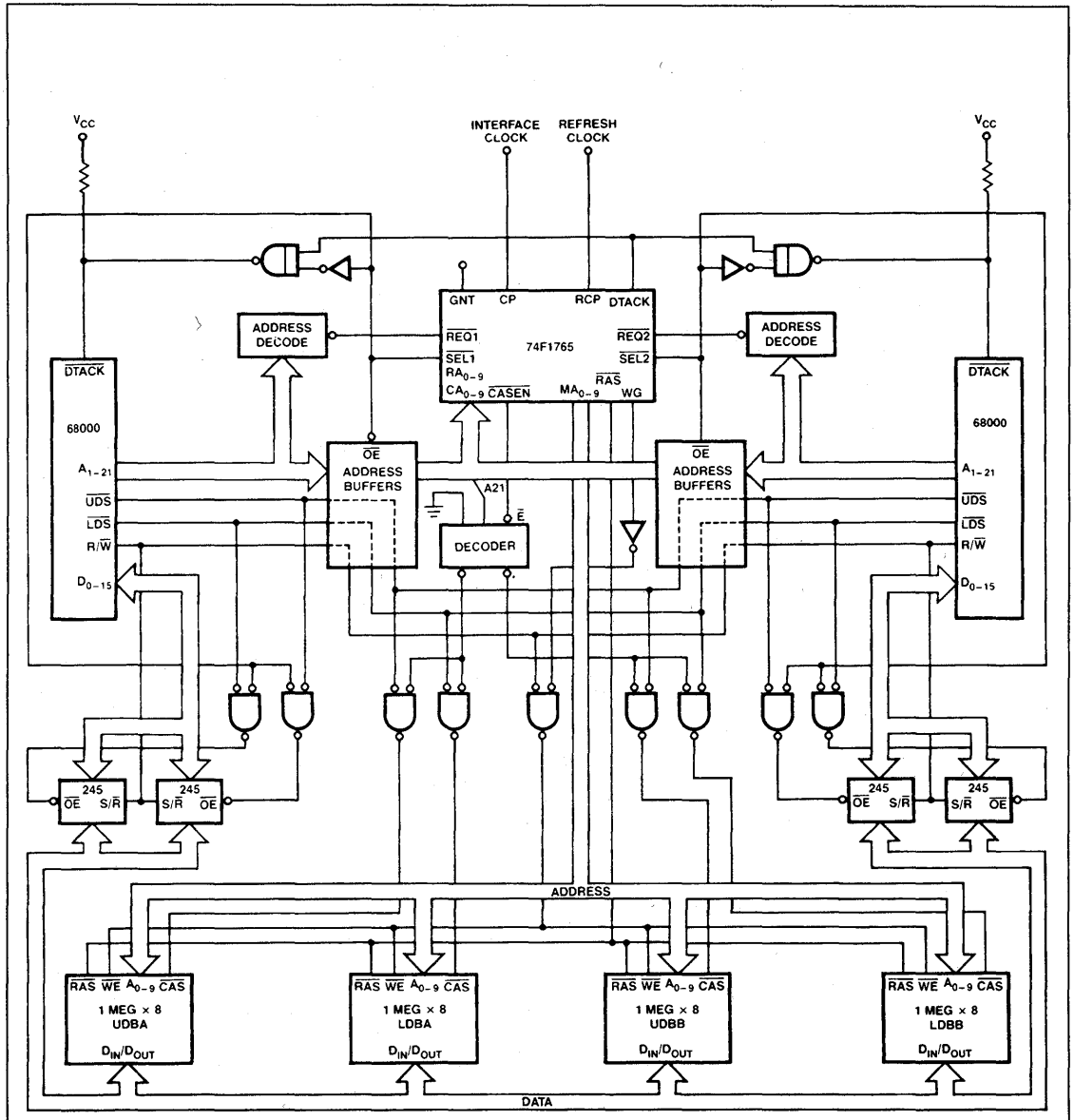
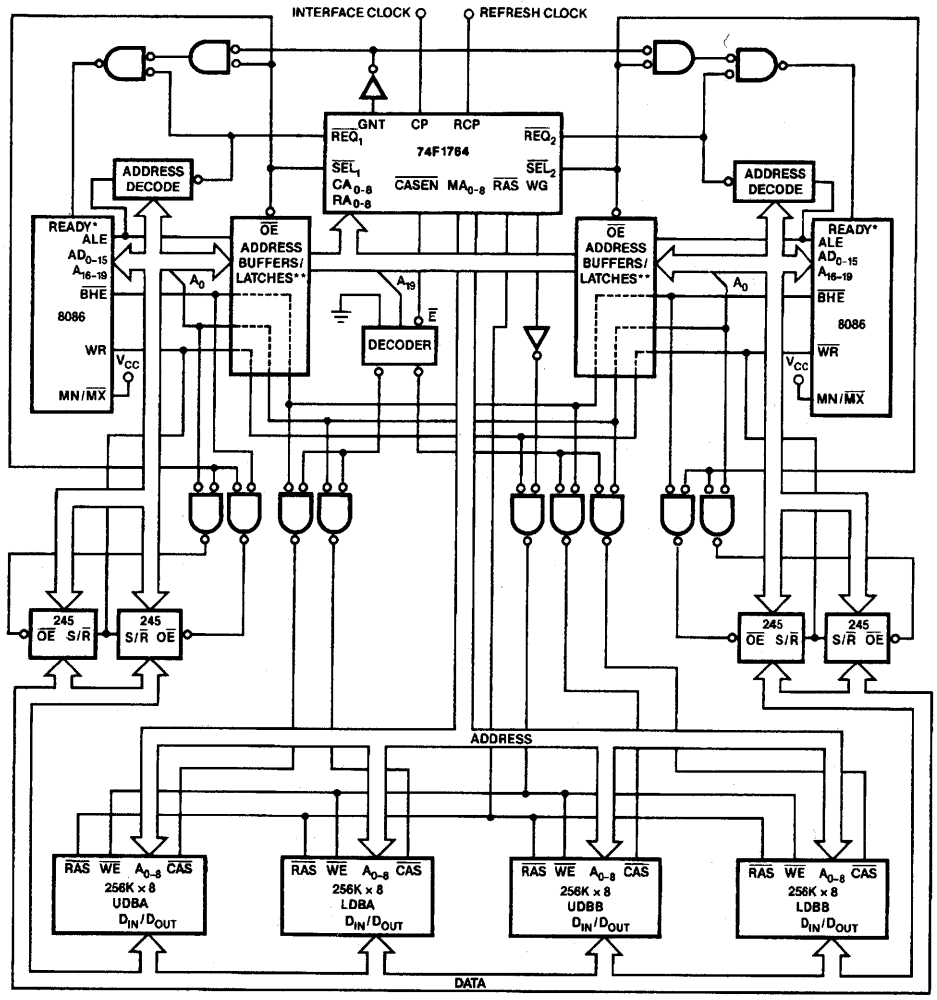


Figure 12. Two 68000 Processors Sharing 4Mbyte of DRAM

APPLICATION



Notes:
*= It might be necessary ti synchronize READY by the 8284A. Please refer to the 8086 data sheet.
**= Whether or not the 8086 address needs to be latched externally, should be determined by the relative speeds of the 8086 and the controller

Figure 11. Two 8086 Processors Sharing 1Mbyte of DRAM

APPLICATION

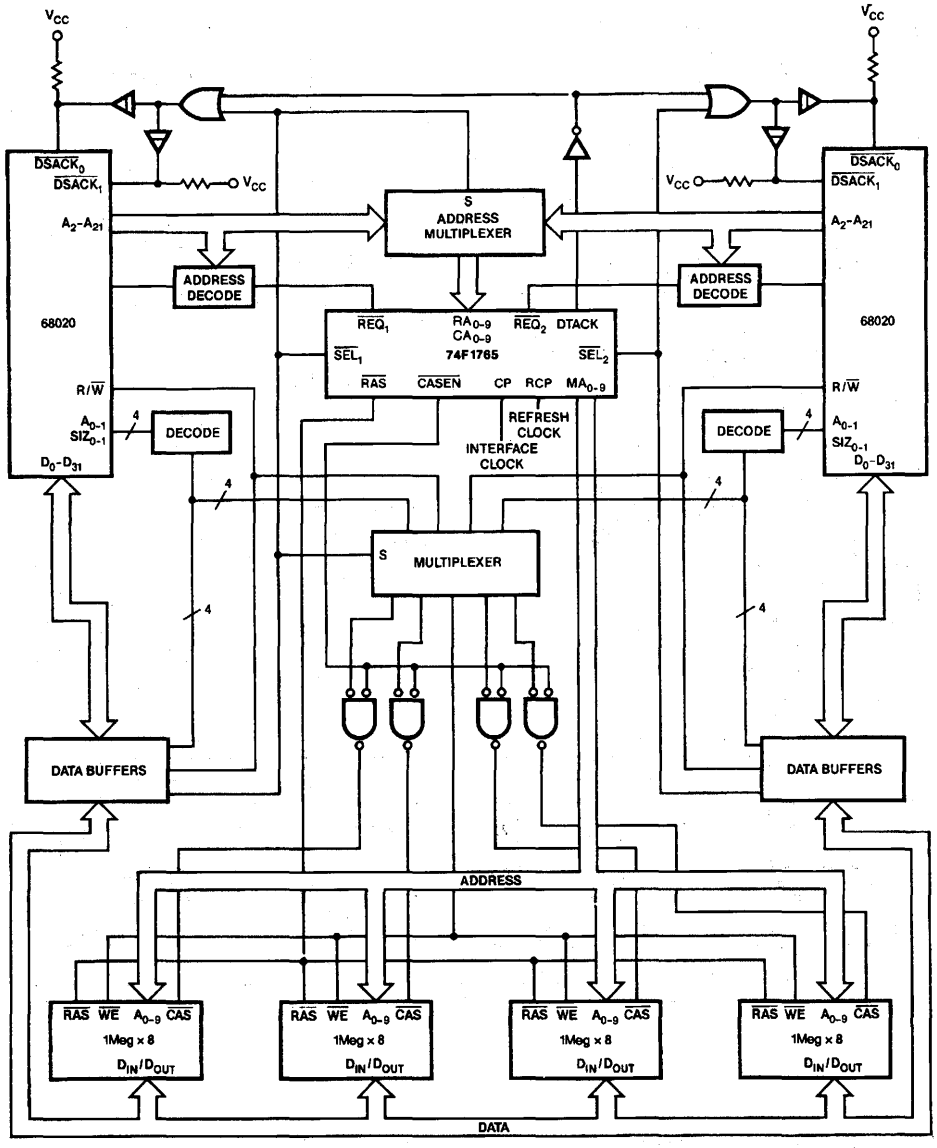


Figure 12. Two 68020 Processors Sharing 4Mbyte of DRAM

APPENDIX A

74F1764 FAMILY LINE DRIVING CHARACTERISTICS

The 74F1764/1765 are designed to provide wave switching in dual-in package (DIP) or zig-zag in-line package (ZIP) housed memory arrays and first reflected wave switching in single in-line package (SIP) or single in-line module(SIM) housed arrays. The 74F1764-1/1765-1, on the other hand, are designed to provide first reflected wave switching with as wide a range of characteristics impedances as possible.

The I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} parameters are included in the product specifications to assist engineers in designing systems which will switch memory array signal lines in the above mentioned manner. For example, the characteristic impedance of signal lines in DIP housed memory arrays is usually around 70Ω. If a signal line has settled out in a High state at 4V and must be pulled down to 0.8V or less on the incident wave, the DRAM controller output must sink (4-0.8)/70A or 46mA at 0.8V. The I_{OL2}/V_{OL2} parameter indicates that the signal line in question will always be swithced on the incidient wave over the full commercial operating range.

It should be noted here that I_{OL2}/V_{OL2} and I_{OH2}/V_{OH2} are intended for transient use only and that steady state operation at I_{OH2} or I_{OL2} is not recommended (long term, steady-state operation at these currents may result in electromigration).

Figures 1-4 show the output I/V characteristics of the DRAM Controller family of devices. These figures also demonstrate graphical method for determining the incident wave (and first reflected wave) characteristics of the devices.

The suggested line termination for the 74F1764/1765 driving a dual in-line packaged or zig-zag packaged DRAMs is shown in Figure 8a. When driving single in-line modules using the 74F1764/1765 or when driving any type of memory arrays with the 74F1764-1/1765-1, The Schottky diode termination shown in Figure 8b can be used (most of these will need no termination at all).

Figures 5-7 are double exposures showing the High to Low to High transitions while driving four banks of eight dual in-line packaged DRAMs. The signal line is unterminated in Figures 5 and 6, allowing the 74F1764/1765 to ring two volts below ground while the 74F1764-1/1765-1 make nice clean transitions. In Figure 7 the 74F1764/1765 is driving the same signal line but with one of its four branches terminated with its characteristic impedance in series with 300 pF to ground (the worst of the four branches is shown).

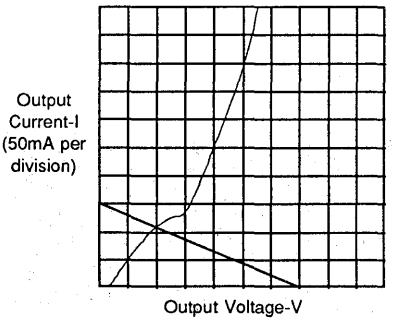


Figure 1.
I-V Output Characteristics of the 74F1764/1765 in the Low state. Light line is the I-V Curve of a 25Ω transmission line settled to 3.5V (typical for recommended termination). The High to Low incident wave on this line will typically be to 0.8V.

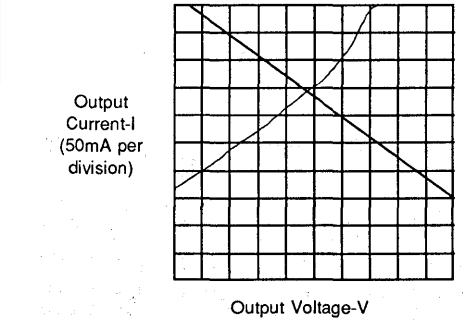


Figure 2.
I-V Output Characteristics of the 74F1764/1765 in the High state. Light line is the I-V Curve of a 35Ω transmission line settled to 0.25V . The incident wave on the Low to High transition will typically be to 2.4V on this line. Any line over 35Ω will typically be switched on the incident wave.

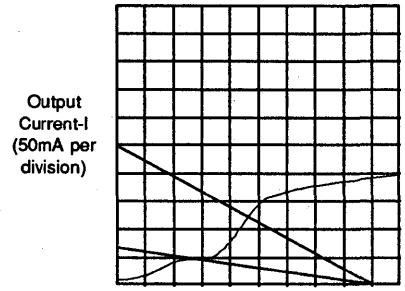


Figure 3.
I-V Output Characteristics of the 74F1764-1/1765-1 in the Low state. Any unterminated line impedance between 18Ω and 70Ω (both shown) will typically switch on the first reflected wave without violating the -1V minimum input voltage specification typical of DRAMs

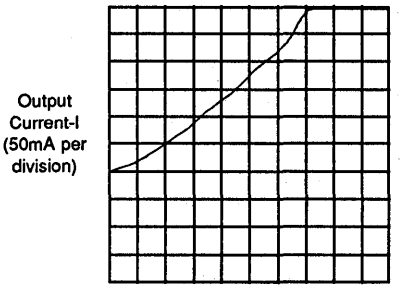


Figure 4.
I-V Output Characteristics of the 74F1764-1/1765-1 in the High state.

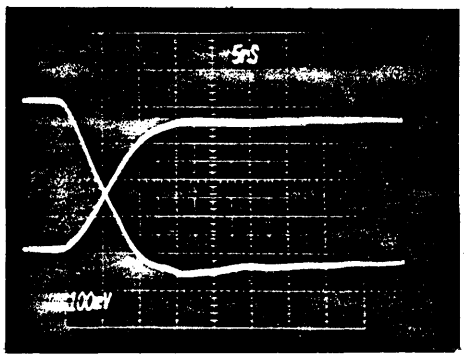


Figure 5.
74F1764-1/1765-1 Driving 32 DRAMS (Unterminated)

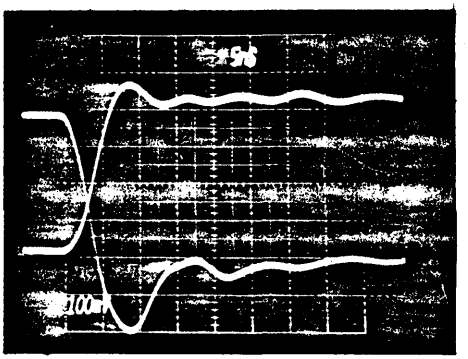


Figure 6.
74F1764/1765 Driving 32 DRAMS (Unterminated)

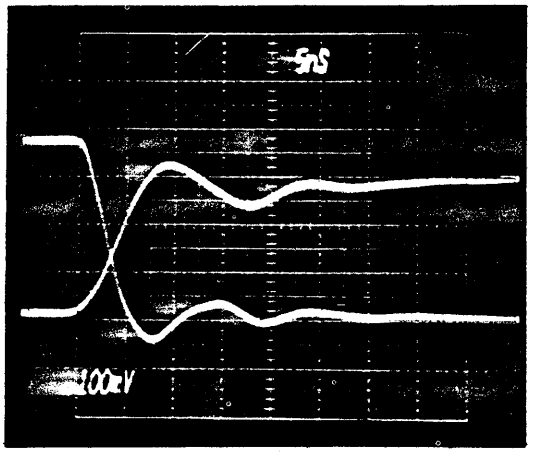


Figure 7.
74F1764/1765 Driving 32 DRAMS (Terminated as in Figure 8a)

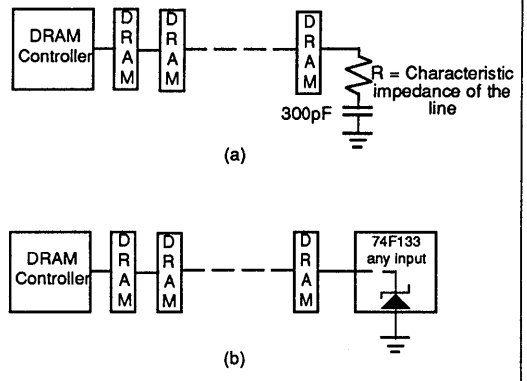


Figure 8.
74F1764/1765 Driving 32 DRAMS (Unterminated)

Signetics

FAST Products

FAST 74F1766

Burst Mode DRAM Controller

Preliminary Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1766	150MHz	200mA

FEATURES

- **Allows Burst-Mode Access for systems using Nibble/Page/Static Column DRAM access mode**
- **Complete control of DRAM access, acknowledge, refresh, and address multiplexing timing functions**
- **True RAS interleaving for minimum refresh and RAS precharge overhead**
- **Asynchronous Arbitration logic to speed up access time**
- **Selectable Precharge, acknowledge, and Row address hold times**
- **FAST logic allows control of 30 nsec DRAMs**
- **48 pin DIP and 44 pin PLCC package option**

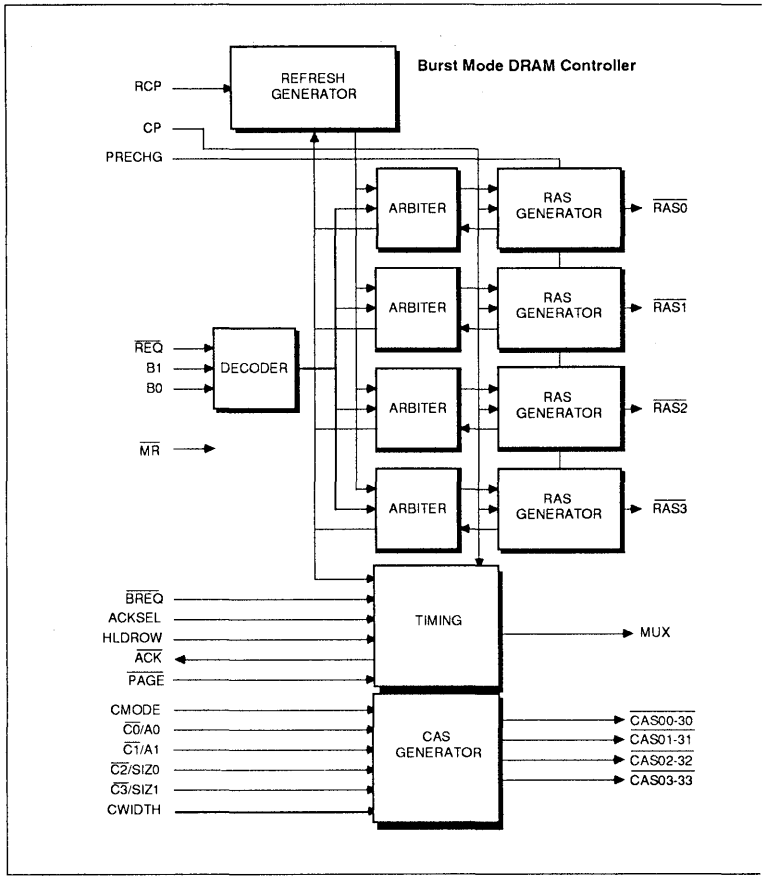
DESCRIPTION

The Signetics Burst-Mode DRAM Controller is a high-performance arbiter and timing generator that supports Nibble, and Static column modes of a dynamic RAM. The controller performs access/refresh arbitration, generates and performs memory refresh, provides RAS interleaving, CAS byte decoding and works with the 74F1762 Memory Address Multiplexer to control up to 4 MBit DRAMs.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
48-Pin Plastic DIP	N74F1766N
44-Pin Plastic PLCC	N74F1766A

BLOCK DIAGRAM



Signetics

FAST 74F1779 Counter

8-Bit Bidirectional Binary Counter (3-state)

FAST Products

FEATURES

- **Multiplexed 3-state I/O ports for bus oriented applications**
- **Built-in look-ahead carry capability**
- **Center power pins to reduce effects of package inductance**
- **Count frequency 145MHz typical**
- **Supply current 90mA typical**
- **See 'F269 for 24 pin separate I/O port version**
- **See 'F579 for 20 pin version**
- **See 'F779 for 16 pin version with abbreviated function table**

DESCRIPTION

The 74F1779 is a fully synchronous 8-stage Up/Down Counter with multiplexed 3-state I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pins (S_0,S_1). The device also features carry look-ahead for easy cascading. All state changes are initiated by the rising edge of the clock. When $\overline{CET}$ is HIgh the data outputs are held in their current state and $\overline{TC}$ is held High. The $\overline{TC}$ output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

The 74F1779 differs from 74F779 in that it has an additional hold mode as described in the Function Table.

Product Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F1779	130MHz	100mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F1779N
16-Pin Plastic SOL[1]	N74F1779D

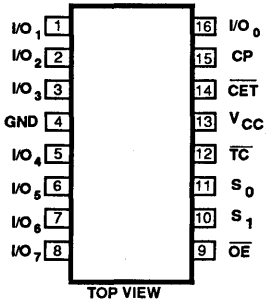
NOTE 1: Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

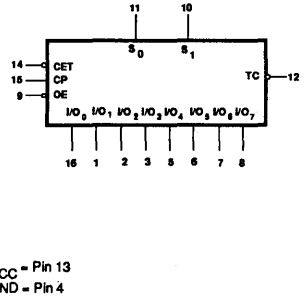
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/O_n	Data inputs	3.5/1.0	70µA/0.6mA
	Data outputs	150/40	3.0mA/24mA
S_0,S_1	Select inputs	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{TC}$	Terminal count output (active Low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

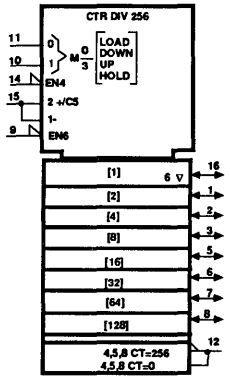
PIN CONFIGURATION



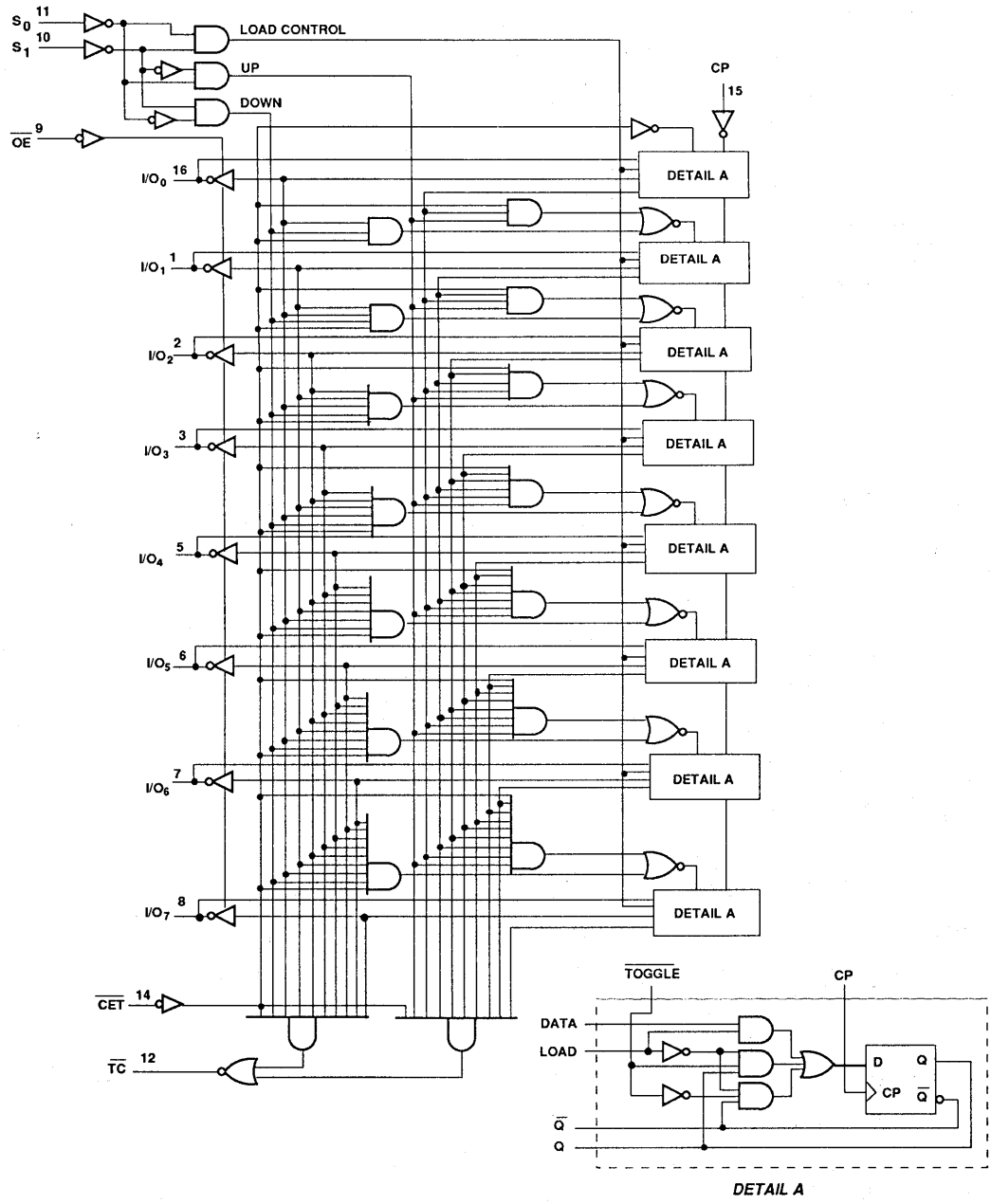
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = pin 13
GND= pin 4

FUNCTION TABLE

INPUTS					OPERATING MODE
S_1	S_0	$\overline{CET}$	$\overline{OE}$	CP	
X	X	X	H	X	I/O_0 to I/O_7 in high impedance
X	X	X	L	X	Flip-flop outputs appears on I/O lines
L	L	X	H	↑	Parallel load all flip-flops
(not LL)		H	X	↑	Hold ($\overline{TC}$ held High)
H	H	X	X	↑	Hold
H	L	L	X	↑	Count up
L	H	L	X	↑	Count down

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
(not LL) = S_0 and S_1 should never be Low voltage level at the same time in the hold mode only.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	$\overline{TC}$	40	mA
		I/O_n	48	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	$\overline{TC}$			-1	mA
		I/O_n			-3	mA
I_{OL}	Low-level output current	$\overline{TC}$			20	mA
		I/O_n			24	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$\overline{TC}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-1mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/O_n		I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	I/O_n	V_{CC} = 5.5V, V_I = 5.5V					1	mA
		others	V_{CC} = 5.5V, V_I =7.0V					100	µA
I_{IH}	High-level input current	except I/O_n	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
$I_{IH}+I_{OZH}$	Off-state output current High-level voltage applied	I/O_n	V_{CC} = MAX, V_O= 2.7V					70	µA
$I_{IL}+I_{OZL}$	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O= 0.5V					-600	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				100	145	mA
		I_{CCL}					100	145	mA
		I_{CCZ}					110	155	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

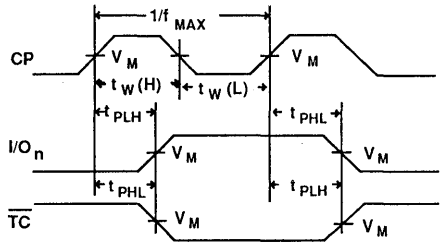
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	115	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	4.0 5.0	6.5 7.0	10.0 10.5	4.0 5.0	10.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	4.0 4.5	6.5 6.5	9.0 9.0	3.5 4.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	2.0 2.5	4.0 4.5	6.5 7.0	2.0 2.5	7.5 7.5	ns
t_{PZH} t_{PZL}	Output Enable time from High or Low level	Waveform 4 Waveform 5	2.0 4.5	4.0 6.5	6.5 9.0	2.0 4.0	7.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 4 Waveform 5	1.0 1.0	3.0 4.0	6.0 7.0	1.0 1.0	6.5 7.5	ns

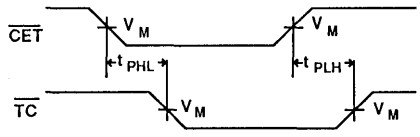
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 3	4.0 3.5			4.5 3.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CET}$ to CP	Waveform 3	4.5 7.0			5.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CET}$ to CP	Waveform 3	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_n to CP	Waveform 3	7.5 8.5			8.0 9.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_n to CP	Waveform 3	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	3.0 4.5			3.0 5.5		ns

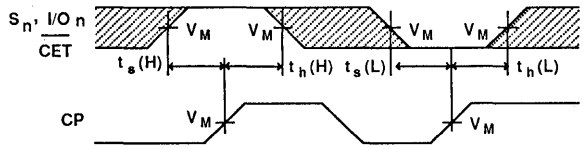
AC WAVEFORMS



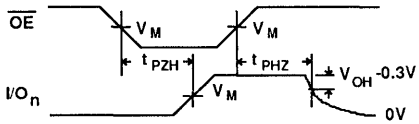
Waveform 1.
Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



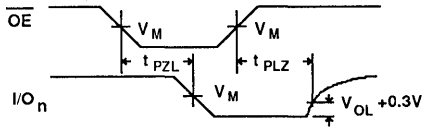
Waveform 2.
Propagation Delay, $\overline{CET}$ input to Terminal Count Output



Waveform 3. Data Setup And Hold Times



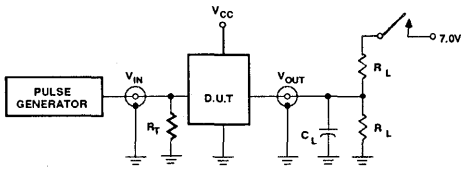
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



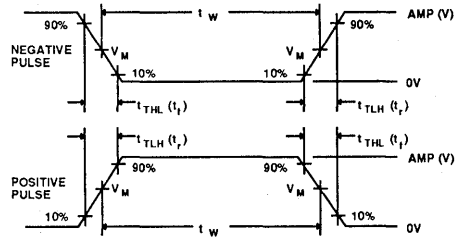
Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F1894,1895,1896,1897
Transceiver with Parity Error

FAST Products

F1894 - 9-Bit Transceiver With Latched 8-Bit Parity Error (OC)
F1895 - 9-Bit Transceiver With Latched 8-Bit Parity Error (3-State)
F1896 - 9-Bit Transceiver With Registered 8-Bit Parity Error (OC)
F1897 - 9-Bit Transceiver With Registered 8-Bit Parity Error (3-State)
Preliminary Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F1894,95,96,97	8.0ns	100mA

FEATURES

- **Similar to 74F657 functions except:**
  - **continuously checks A port Parity**
  - **has internal parity error latch/reg**
  - **has parity bit carry through**
- **Error output continuously checks A port Parity**
- **High impedance NPN base input for reduced loading (70μA in High and Low states)**
- **Ideal in applications where High output drive and light bus loading are required (I_{IL} is 70μA vs FAST std of 600μA)**
- **3-state B Port outputs sink 64mA**
- **Input diodes for termination effects**
- **28 pin plastic Slim Dip (300mil) package**

DESCRIPTION

The 74F1894-97 are 9-bit transceivers featuring non-inverting buffers with 3-state outputs [F1894, F1896] or open collector outputs [F1895, F1897] and a latched [F1894, F1895] or registered [F1896, F1897] 8-bit even parity error generator, and are intended for bus-oriented applications. The B port outputs are all capable of sinking 64mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The A port outputs have a guaranteed current sinking capability of 24mA and source 3mA. The Direc-

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic Slim DIP (300 mil)	N74F1894N,95N,96N,97N
28-Pin Plastic SOL[1]	N74F1894D,95D,96D,97D

NOTE 1: Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

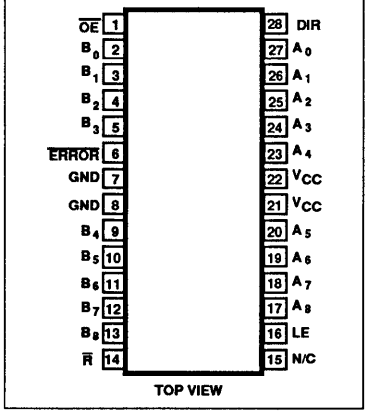
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A port 3-state inputs	3.5/0.117	70μA/70μA
B_0 - B_7	B port 3-state inputs	3.5/0.117	70μA/70μA
$\overline{R}$	$\overline{ERROR}$ Latch/Register Reset input	1.0/0.033	20μA/20μA
LE	Latch Enable input (F1894, 95 only)	1.0/0.033	20μA/20μA
CP	Register Clock input (F1896, 97 only)	1.0/0.033	20μA/20μA
DIR	$\overline{A\text{-to-}B}$, B-to-A Direction input	2.0/0.066	40μA/40μA
$\overline{OE}$	A/B Output Enable input (active Low)	2.0/0.066	40μA/40μA
$\overline{EOE}$	Error Output Enable input ('F1895, 97 only)	1.0/0.033	20μA/20μA
A_0 - A_7	A port 3-state outputs	150/40	3.0mA/24mA
B_0 - B_7	B port 3-state outputs	750/106.7	15mA/64mA
$\overline{ERROR}$	Even Parity Error output (3-state*or OC)	750*/106.7	15mA*/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

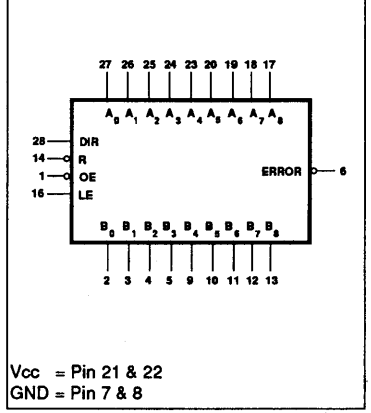
PIN CONFIGURATION

'F1894



LOGIC SYMBOL

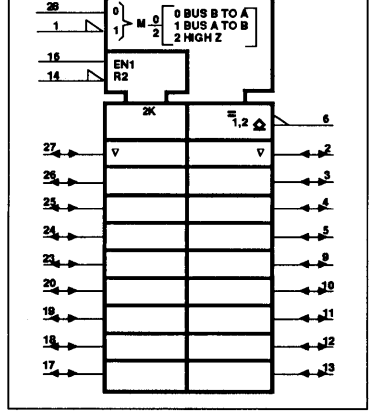
'F1894



Vcc = Pin 21 & 22
GND = Pin 7 & 8

LOGIC SYMBOL(IEEE/IEC)

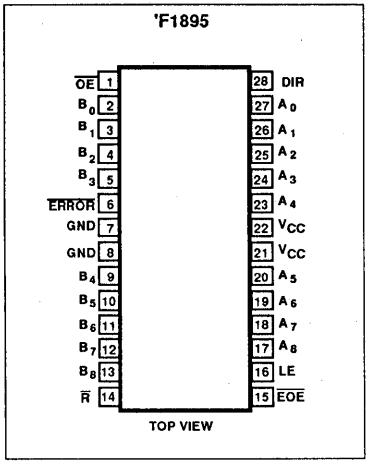
'F1894



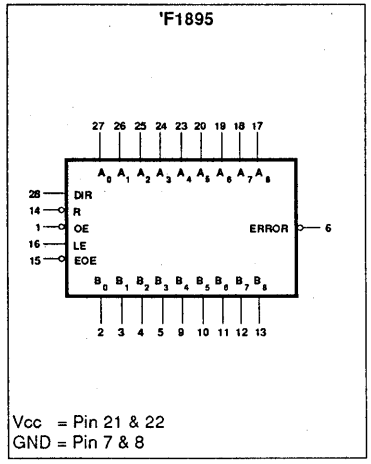
Transceiver with Parity Error

FAST 74F1894, F1895, F1896, F1897

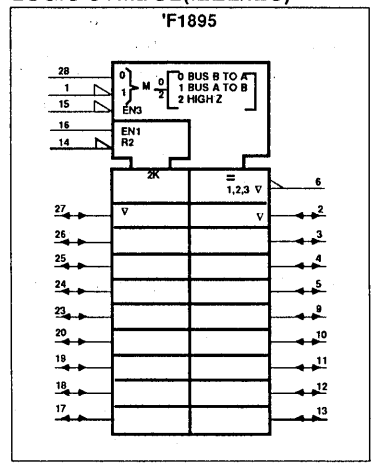
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



tion [DIR] input determines the direction of data flow through the bidirectional transceivers. Active-Low enables data from A ports to B ports; Active-High enables data from B ports to A ports.

The error ($\overline{ERROR}$) pin is an output from the even parity checker connected to port A. If the number of High bits on port A is odd, then the error ($\overline{ERROR}$) output will be Low, indicating bad (or odd) parity. If the number of High bits on port A is even, then the error ($\overline{ERROR}$) output will be High, indicating even parity.

The F1894 & F1895 have a transparent latch on the error ($\overline{ERROR}$) output. The latch is transparent (data passes through) when the latch enable (LE) pin is High. The data is latched on the error ($\overline{ERROR}$) output when the latch enable (LE) pin is Low. If an error has occurred and is latched, the error ($\overline{ERROR}$) output will remain Low until the latch becomes transparent or is cleared with a Low on the reset input ($\overline{R}$) pin.

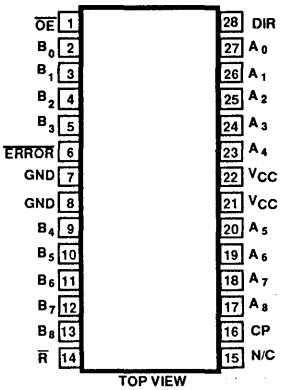
The F1896 & F1897 have a D flip-flop register on the error ($\overline{ERROR}$) output. The data is entered into the register on the rising edge of the register clock input (CP) pin. If an error has occurred, the error ($\overline{ERROR}$) output will remain Low until the register is cleared with a Low on the reset ($\overline{R}$) input.

The F1895 & F1987 also have an error output enable ($\overline{EOE}$) pin. When error output enable ($\overline{EOE}$) is Low , the error ($\overline{ERROR}$) output is enabled. When error output enable ($\overline{EOE}$) is High, the error ($\overline{ERROR}$) output is in 3-State.

Transceiver with Parity Error — FAST 74F1894, F1895, F1896, F1897

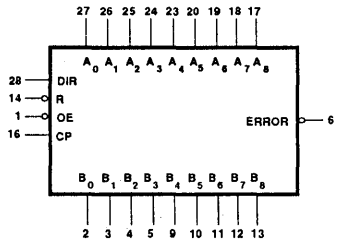
PIN CONFIGURATION

'F1896



LOGIC SYMBOL

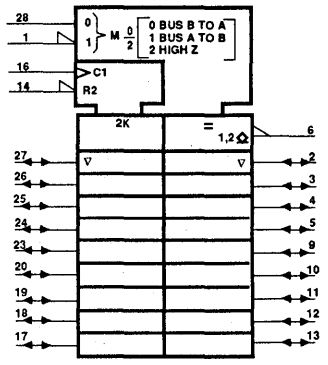
'F1896



Vcc = Pin 21 & 22
GND = Pin 7 & 8

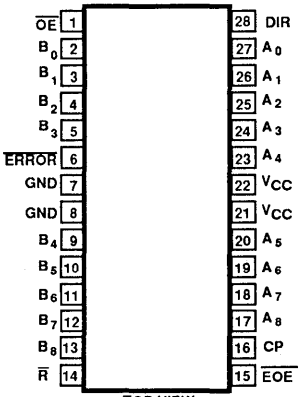
LOGIC SYMBOL(IEEE/IEC)

'F1896



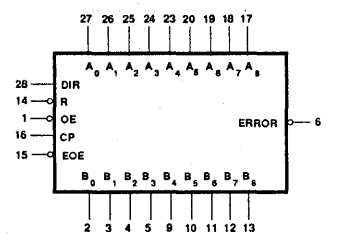
PIN CONFIGURATION

'F1897



LOGIC SYMBOL

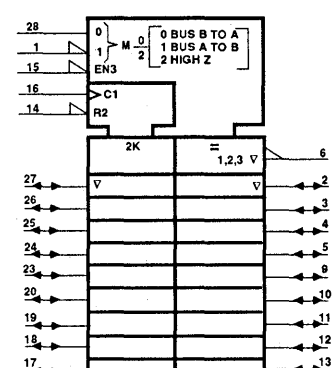
'F1897



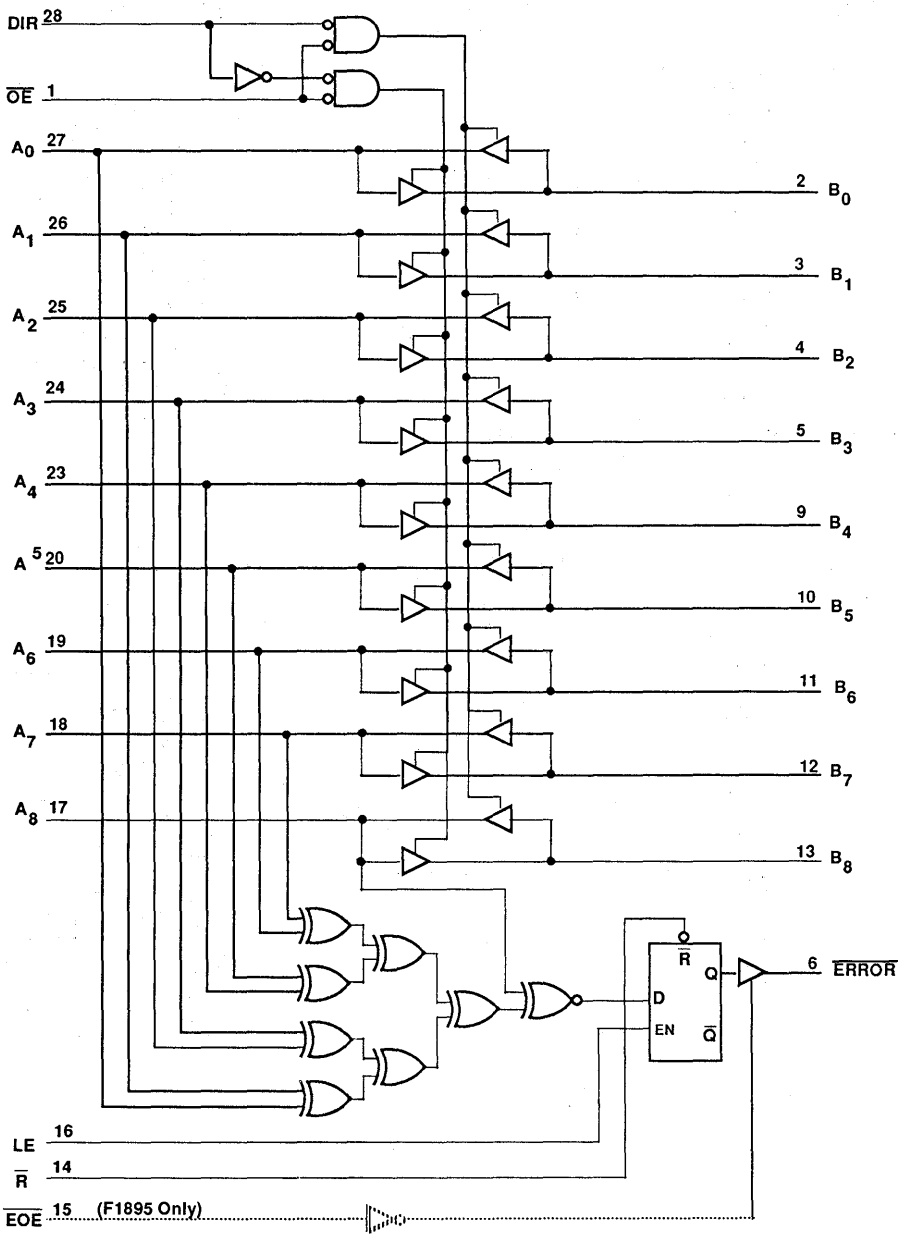
Vcc = Pin 21 & 22
GND = Pin 7 & 8

LOGIC SYMBOL(IEEE/IEC)

'F1897

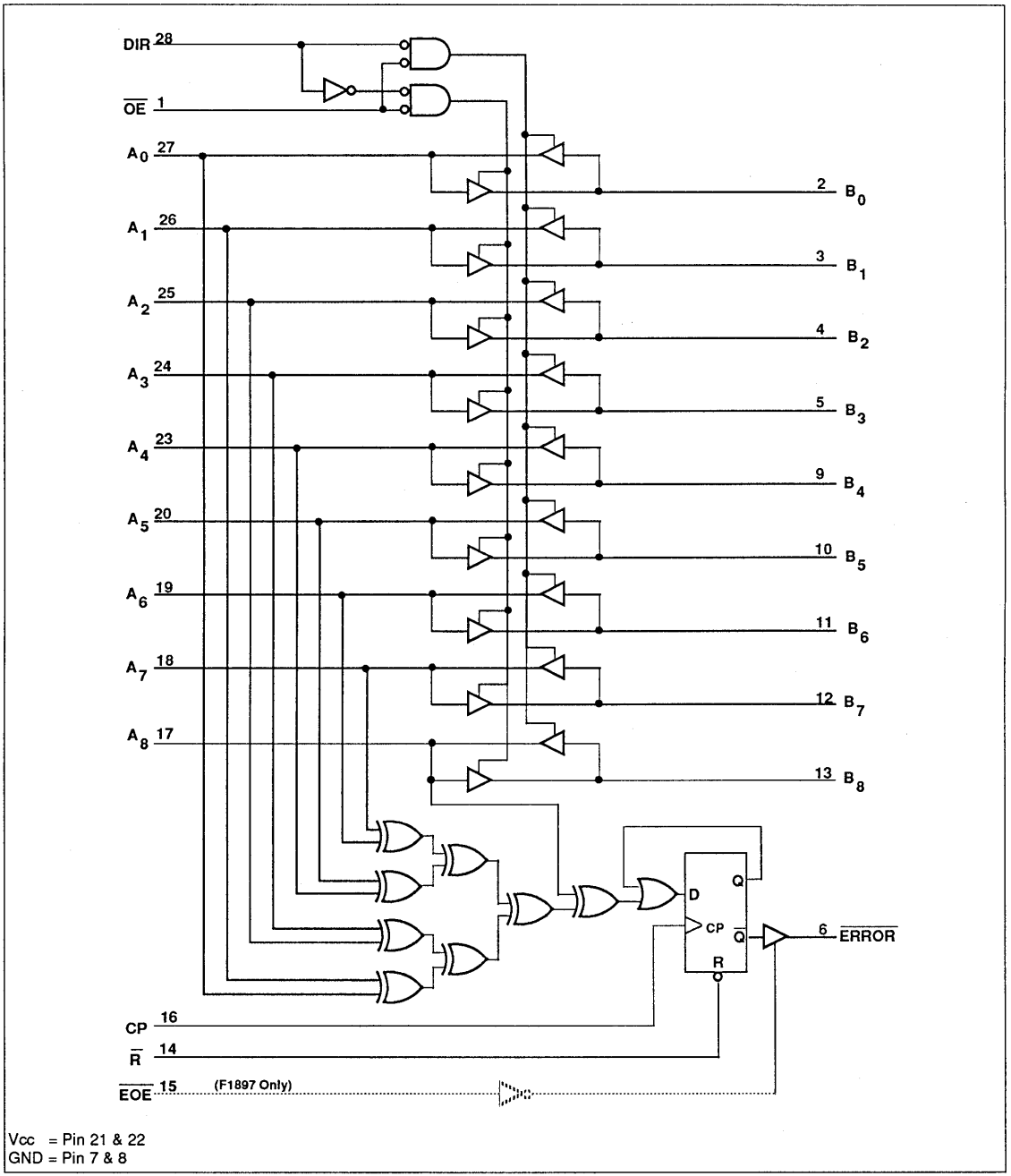


LOGIC DIAGRAM FOR 'F1894, 'F1895



Vcc = Pin 21 & 22
GND = Pin 7 & 8

LOGIC DIAGRAM FOR 'F1896, 'F1897



Vcc = Pin 21 & 22
GND = Pin 7 & 8

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7, $\overline{ERROR}$	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0-B_7, $\overline{ERROR}$			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7, $\overline{ERROR}$			64	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		B_0-B_7, $\overline{ERROR}$		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7, $\overline{ERROR}$		I_{OL}=48mA	±10%V_{CC}		0.30	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{R}$, LE, CP, DIR, $\overline{OE}$, $\overline{EOE}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_0-A_7	V_{CC} = MAX, V_I = 5.5V					2	mA
		B_0-B_7						1	mA
I_{IH}	High-level input current	$\overline{R}$, LE, CP, $\overline{EOE}$	V_{CC} = MAX, V_I = 2.7V					20	µA
		DIR, $\overline{OE}$						40	µA
I_{IL}	Low-level input current	$\overline{R}$, LE, CP, $\overline{EOE}$	V_{CC} = MAX, V_I = 0.5V					-20	µA
		DIR, $\overline{OE}$						-40	µA
I_{OZH} + I_{IH}	Off-state output current, High-level voltage applied	A_0-A_7, B_0-B_7, $\overline{ERROR}$(3S)	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZH} + I_{IL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-70	µA
I_{OZH}	Off-state output current, High-level voltage applied	$\overline{ERROR}$(OC)	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 2.7V					-50	µA
I_{OS}	Short-circuit output current[3]	A_0-A_7	V_{CC} = MAX			-60		-150	mA
		B_0-B_7				-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				90	125	mA
		I_{CCL}					106	150	mA
		I_{CCZ}					99	145	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 2	2.5 2.5	5.5 5.5	7.5 7.5	2.5 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{ERROR}$	Waveform 1, 2	7.0 7.0	10.0 10.0	14.0 14.0	7.0 7.0	16.0 16.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{R}$ to $\overline{ERROR}$	Waveform 1, 2	4.5 4.5	7.5 7.5	11.0 11.0	4.5 4.5	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay LE to $\overline{ERROR}$ (F1894,95 ONLY)	Waveform 1, 2	4.5 4.5	7.5 7.5	11.0 11.0	4.5 4.5	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{ERROR}$ (F1896,97 ONLY)	Waveform 1, 2	4.5 4.5	7.5 7.5	11.0 11.0	4.5 4.5	12.0 12.0	ns
t_{PZH} t_{PZL}	Output Enable time[1] to High or Low level	Waveform 4 Waveform 5	3.0 4.0	5.5 7.0	8.0 9.5	3.0 4.0	9.0 11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 4 Waveform 5	2.0 2.0	4.5 4.0	7.5 6.0	2.0 2.0	8.0 6.5	ns

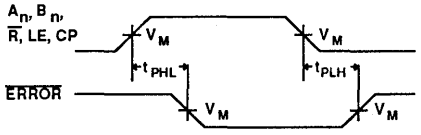
NOTE:

1. These delay times reflect the 3-state recovery time only and not the signal through the buffers or the parity check circuitry. To assure VALID information at the $\overline{ERROR}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry to the $\overline{ERROR}$ output (same as A to $\overline{ERROR}$) after the $\overline{ERROR}$ pin has been enabled (Output Enable time). VALID data at the $\overline{ERROR}$ pin ≤ (B to A) + (A to $\overline{ERROR}$) + (Output Enable time).

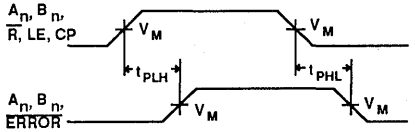
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n to CP	Waveform 3	7.0 7.0			14.0 14.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n to LE	Waveform 3	7.0 7.0			14.0 14.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n to CP	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n to LE	Waveform 3	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CP	Waveform 3	7.0 7.0			8.0 8.0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low LE	Waveform 3	7.0 7.0			8.0 8.0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low $\overline{R}$	Waveform 3	7.0 7.0			8.0 8.0		ns

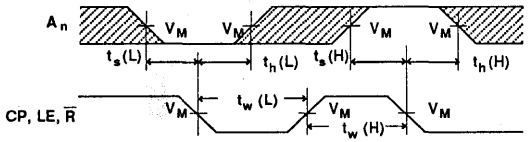
AC WAVEFORMS



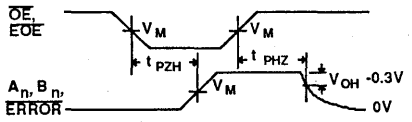
Waveform 1. Propagation Delay for Inverting Outputs



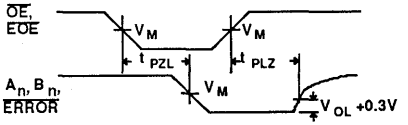
Waveform 2. Propagation Delay for Non-Inverting Outputs



Waveform 3. Data Setup And Hold Times And CP, LE, and R Pulse Widths



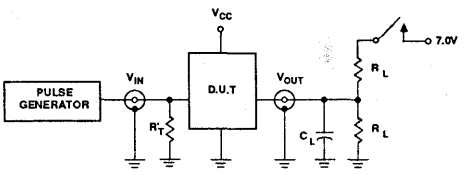
Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 5. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded area indicate when the input is permitted to change for predictable output

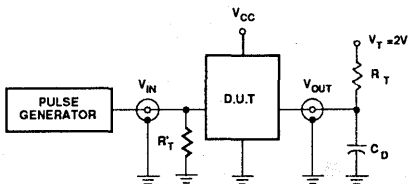
TEST CIRCUIT AND WAVEFORMS



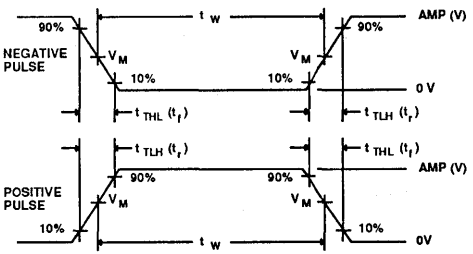
Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test Circuit For Open Collector Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R'_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistor; see AC CHARACTERISTICS for value.

Signetics

FAST Products

FAST 74F2952, 74F2953 Transceivers

'F2952 Registered Transceiver, Non-Inverting (3-State)
'F2953 Registered Transceiver, Inverting (3-State)
Product Specification

FEATURES

- **8-bit Registered Transceivers**
- **Two 8-bit , back-to-back registers store data moving in both directions between two bidirectional busses**
- **Separate Clock, Clock Enable and 3-state Enable provided for each register**
- **'F2952 Non-inverting 'F2953 Inverting**
- **AM2952/2953 functional equivalent**
- **A outputs sink 24mA and source 3mA**
- **B outputs sink 64mA and source 15mA**
- **300 mil wide 24-pin Slim DIP package**

DESCRIPTION

The 74F2952 and 74F2953 are 8-bit Registered Transceivers. Two 8-bit back to back registers store data flowing in both directions between two bi-directional busses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-state output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F2952	160MHz	105mA
74F2953	160MHz	105mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F2952N, N74F2953N
24-Pin Plastic SOL[1]	N74F2952D, N74F2953D

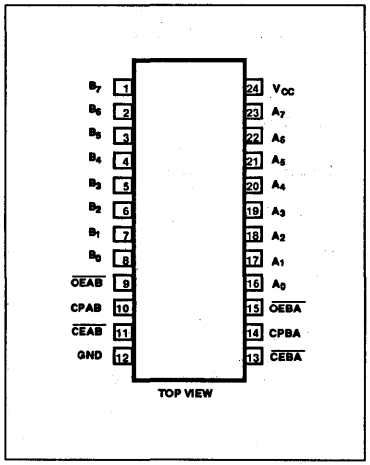
NOTE:
1.Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

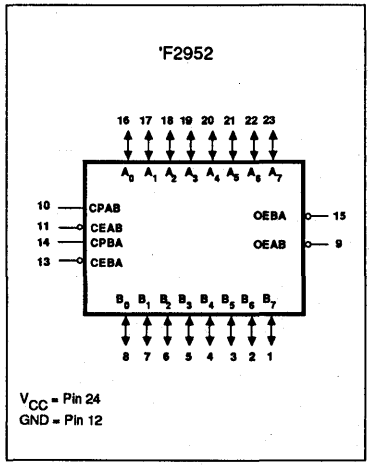
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	Port A, 3-state inputs	3.5/1.0	70µA/0.6mA
B_0 - B_7	Port B, 3-state inputs	3.5/1.0	70µA/0.6mA
CPAB,CPBA	Clock inputs	1.0/1.0	20µA/0.6mA
$\overline{CEAB}$,$\overline{CEBA}$	Clock Enable inputs	1.0/1.0	20µA/0.6mA
$\overline{OEAB}$,$\overline{OEBA}$	Output Enable inputs	1.0/1.0	20µA/0.6mA
A_0 - A_7	Port A, 3-state outputs	150/40	3.0mA/24mA
B_0 - B_7	Port B, 3-state outputs	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

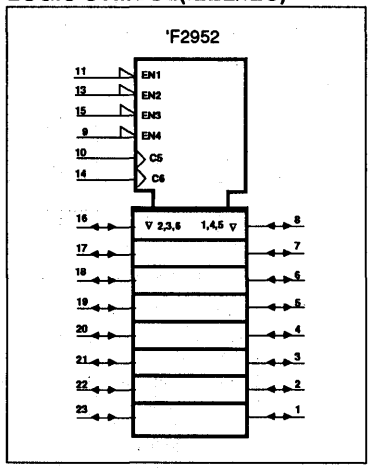
PIN CONFIGURATION



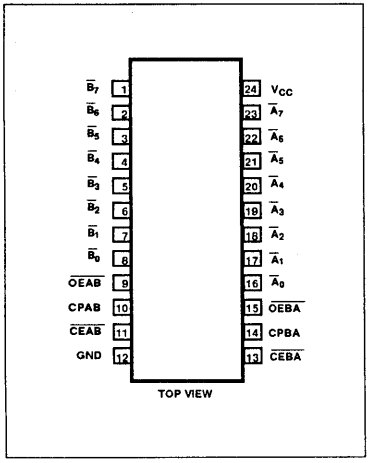
LOGIC SYMBOL



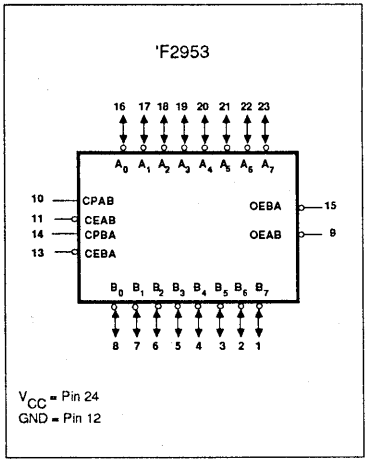
LOGIC SYMBOL(IEEE/IEC)



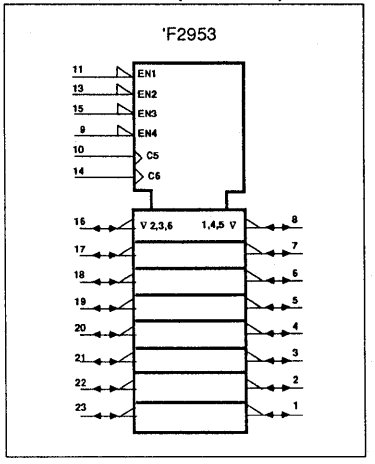
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



FUNCTION TABLE for Register A_n or B_n

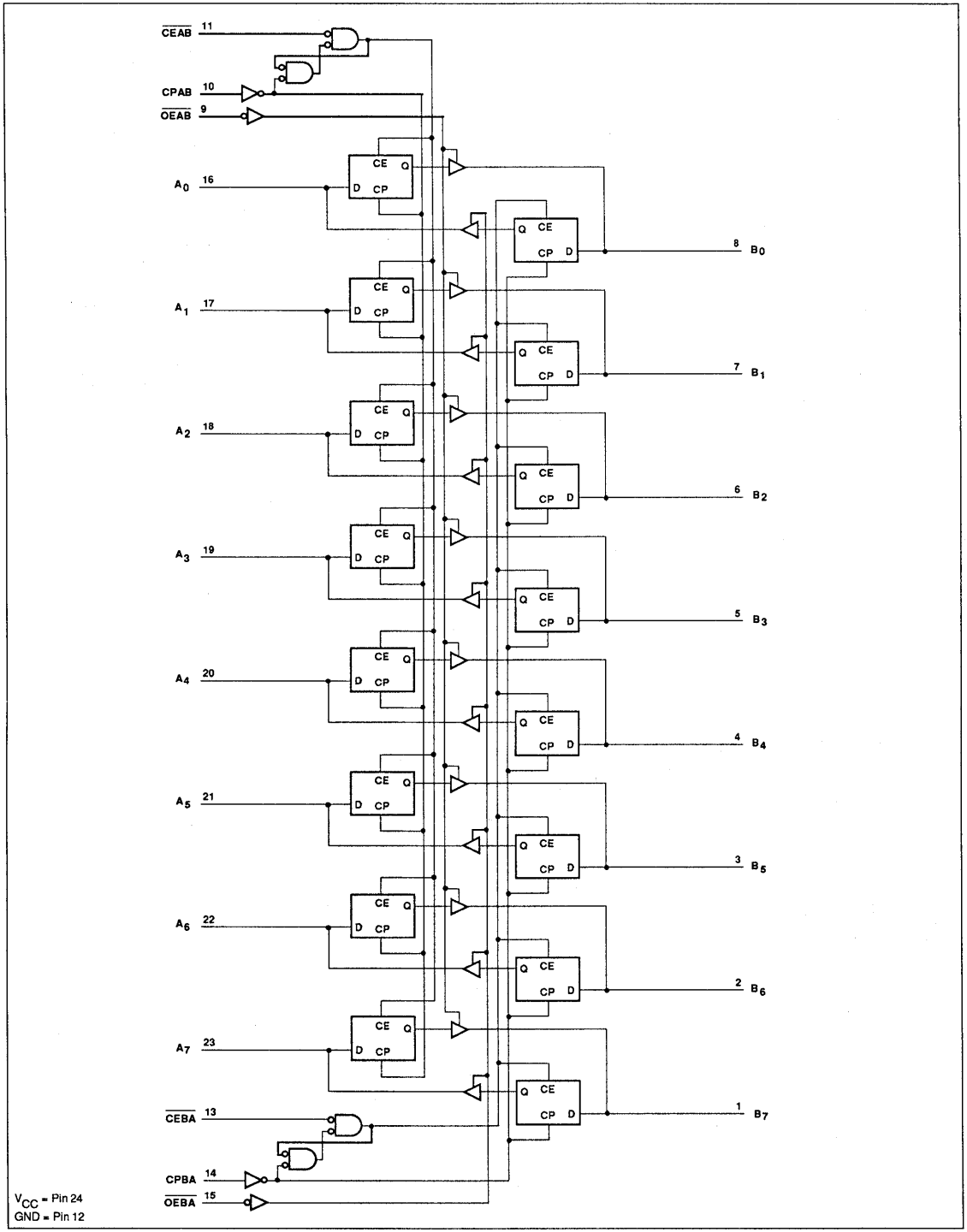
INPUTS			INTERNAL	OPERATING MODE
A_n or B_n	CPXX	$\overline{CEXX}$	Q	
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	

FUNCTION TABLE for Output Enable

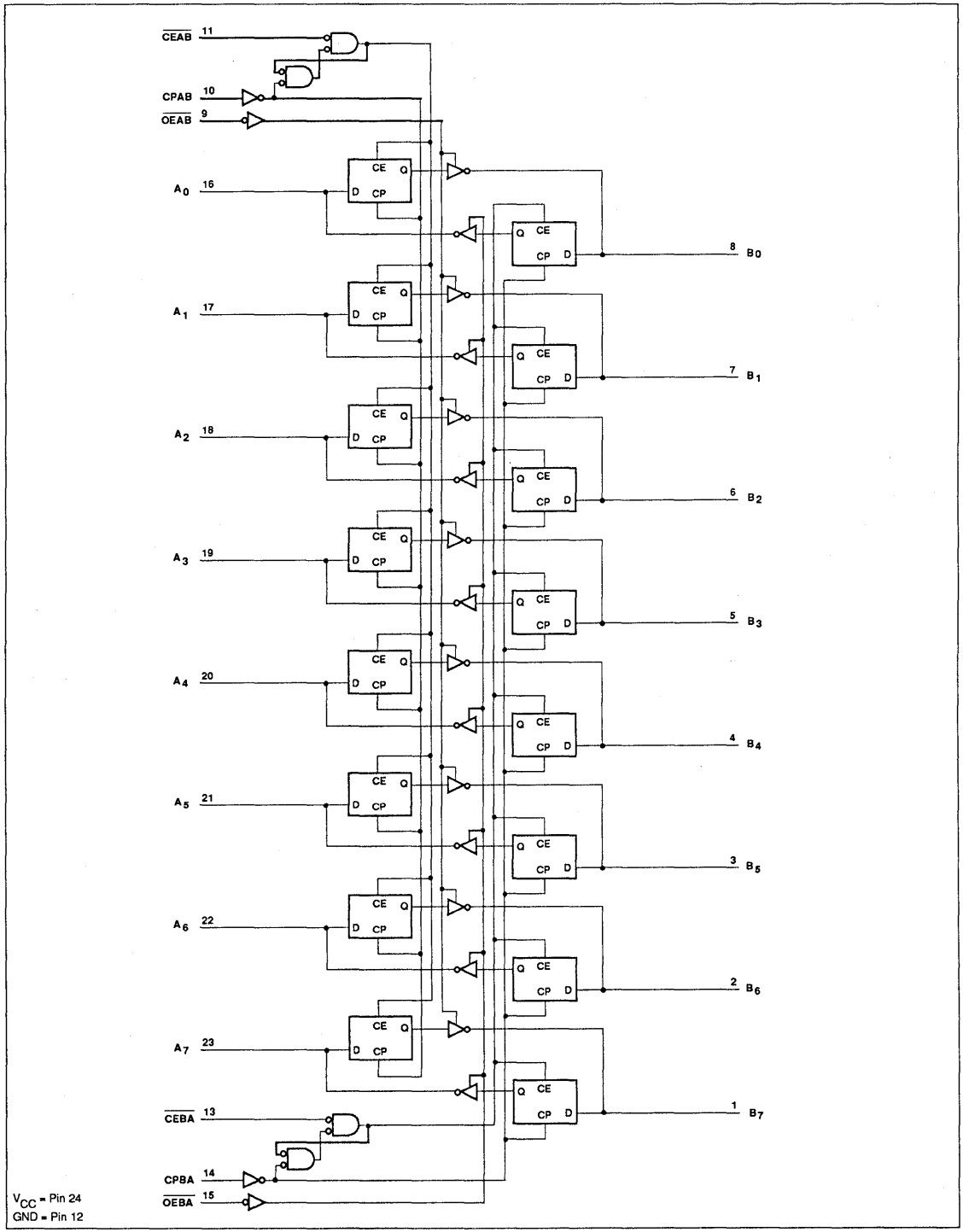
INPUTS	INTERNAL	A_n or B_n OUTPUTS		OPERATING MODE
$\overline{OEXX}$	Q	'F2952	'F2953	
H	X	Z	Z	Disable outputs
L	L	L	H	Enable outputs
L	H	H	L	

H= High voltage level
L= Low voltage level
↑ =Low-to-High transition
X=Don't care
XX=AB or BA
NC=No change
Z =High impedance "off" state

LOGIC DIAGRAM for 'F2952



LOGIC DIAGRAM for 'F2953



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0-B_7			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
		B_0-B_7		I_{OH}=-15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=48mA	±10%V_{CC}		0.38	0.55	V
				I_{OL}=64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{CPAB}$, $\overline{CPBA}$, $\overline{OEAB}$ $\overline{OEBA}$,$\overline{CEAB}$, $\overline{CEBA}$	V_{CC} = 5.5V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = 5.5V, V_I = 5.5V					1	mA
I_{IH}	High-level input current	$\overline{CPAB}$, $\overline{CPBA}$, $\overline{OEAB}$, $\overline{OEBA}$, $\overline{CEAB}$, $\overline{CEBA}$	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied	A_0-A_7, B_0-B_7	V_{CC} = MAX, V_O= 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied	A_0-A_7, B_0-B_7	V_{CC} = MAX, V_O = 0.5V					-60	µA
I_{OS}	Short-circuit output current[3]	A_0-A_7	V_{CC} = MAX, V_O=0.00V			-60		-150	mA
		B_0-B_7				-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				90	140	mA
		I_{CCL}					120	175	mA
		I_{CCZ}					105	155	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

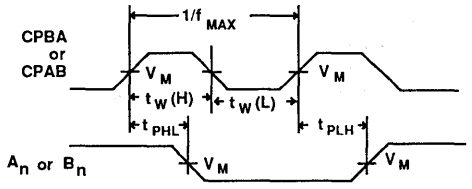
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	74F2952, 74F2953					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	145	160		135		MHz
t_{PLH} t_{PHL}	Propagation delay CPBA or CPAB to A_n or B_n	Waveform 1	3.0 3.5	5.0 6.0	7.5 8.5	2.5 3.5	8.0 9.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	Waveform 3 Waveform 4	2.0 3.5	4.5 6.0	7.0 9.5	2.0 3.0	8.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	Waveform 3 Waveform 4	2.0 1.5	4.0 3.5	8.0 6.5	1.5 1.0	9.0 7.0	ns

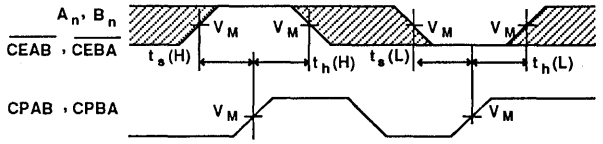
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	74F2952, 74F2953					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	'F2952	Waveform 2	4.5 3.5			5.0 4.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	'F2953	Waveform 2	4.0 3.5			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA		Waveform 2	0.0 0.0			0.0 0.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEAB}$,$\overline{CEBA}$ to CPAB , CPBA		Waveform 2	0.0 4.0			0.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEAB}$,$\overline{CEBA}$ to CPAB , CPBA		Waveform 2	2.5 2.5			2.5 3.0		ns
$t_w(H)$ $t_w(L)$	CPAB or CPBA Pulse width, High or Low		Waveform 1	3.0 3.5			3.0 3.5		ns

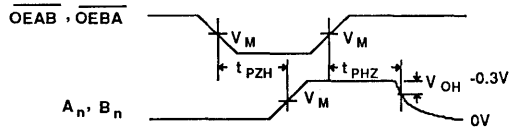
AC WAVEFORMS



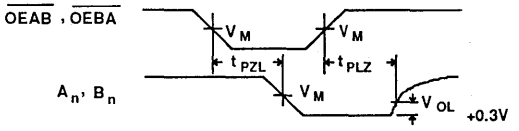
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup And Hold Times



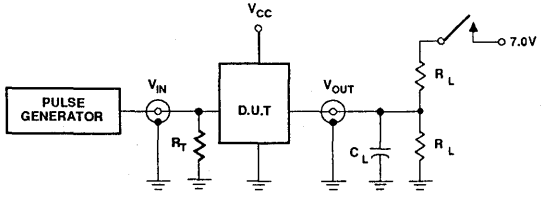
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



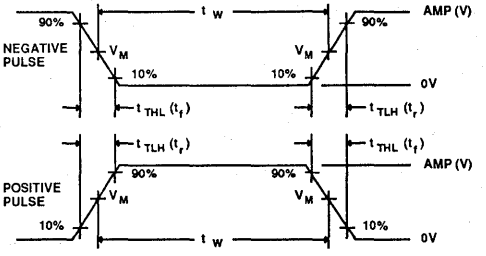
Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded area indicate when the input is permitted to change for predictable output

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F3037
30Ω Line Driver

Quad Two-Input NAND 30Ω Line Driver

FAST Products

FEATURES

- **30Ω line driver**
- **160mA output drive capability in the Low state**
- **67mA output drive capability in the High state**
- **High speed**
- **Facilitates incident wave switching**
- **3nh lead inductance each on V_{CC} and GND when both side pins are used**

DESCRIPTION

The 74F3037 is a high current Line Driver composed of four 2-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The drive capability of the 'F3037 is 67mA source and 160mA sink with a V_{CC} as low as 4.5V. This guarantees incident wave switching with V_{OH} not less than 2.0V and V_{OL} not more than 0.8V while driving impedances as low as 30 ohms. This is applicable with any combination of outputs using continuous duty.
The propagation delay of the part is minimally affected by reflections when terminated only by the TTL inputs of other devices. Performance may be improved by full or partial line termination.

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3037	3.8 ns	13 mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F3037N
16-Pin Plastic SOL[1]	N74F3037D

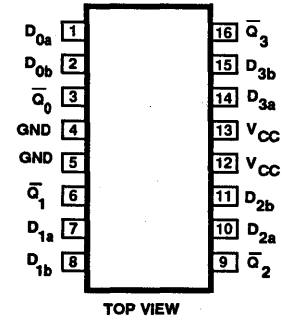
NOTE:
1. Thermal mounting techniques are recommended. See SMD Process Apllications (page 17) for a discussion of thermal consideration for surface mounted devices. If driving impedances 42 ohms or greater then thermal mounting is not necessary.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

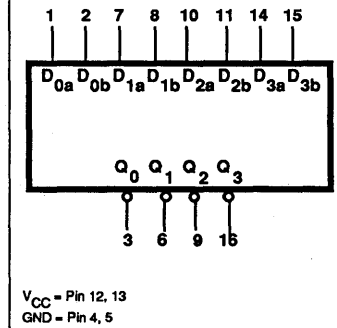
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}_n$	Data outputs	3350/266	67mA/160mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

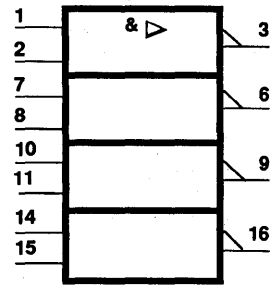
PIN CONFIGURATION



LOGIC SYMBOL

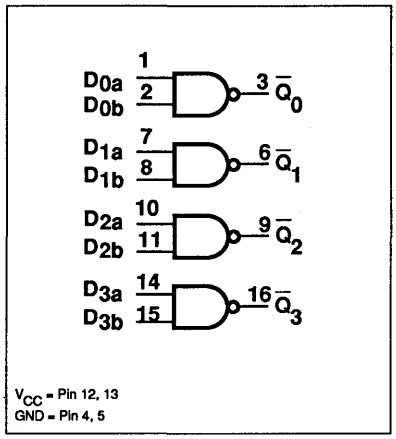


LOGIC SYMBOL (IEEE/IEC)



30Ω Line Driver | FAST 74F3037

LOGIC DIAGRAM



V_{CC} = Pin 12, 13
GND = Pin 4, 5

FUNCTION TABLE

INPUTS		OUTPUT
D_{na}	D_{nb}	$\overline{Q}_n$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	320	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-67	mA
I_{OL}	Low-level output current			160	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

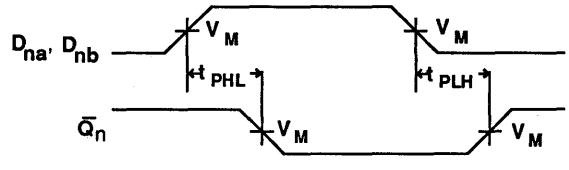
SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -45mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH1} = -67mA[3]	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		0.42	0.55	V
				I_{OL1} = 160mA[4]	±5%V_{CC}			0.80	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_O	Output current[5]		V_{CC} = MAX, V_O = 2.25V			-80		-180	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				3.5	6.0	mA
		I_{CCL}					27	40	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH1} is the current necessary to guarantee the Low to High transition in a 30 ohm transmission line on the incident wave.
4. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30 ohm transmission line on the incident wave.
5. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to $\overline{Q}_n$	Waveform 1	3.0 1.5	4.5 3.0	6.0 5.0	2.5 1.5	6.5 5.5	ns

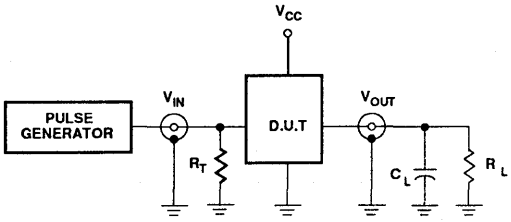
AC WAVEFORMS



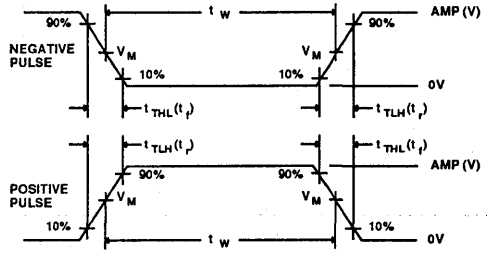
Waveform 1. Propagation Delay for Inputs to Output

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST 74F3038
30Ω Line Driver

Quad Two-Input NAND 30Ω Line Driver (Open Collector)

FAST Products

Product Specification

FEATURES

- **30Ω line driver**
- **160mA output drive capability**
- **High speed**
- **Facilitates incident wave switching**
- **3nh lead inductance each on V_{CC} and GND when both side pins are used**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3038	9.0 ns	17 mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	74F3038N
16-Pin Plastic SO	74F3038D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}_n$	Data outputs	OC/266	OC/160mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC = Open Collector

DESCRIPTION

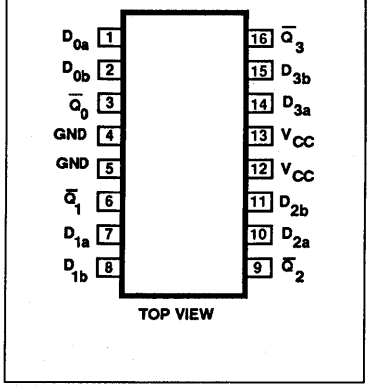
The 74F3038 is a high current Open-Collector Line Driver composed of four 2-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The 74F3038 can sink 160mA with a V_{CC} as low as 4.5V. This guarantees incident wave switching with V_{OL} not more than 0.8V while driving impedances as low as 30 ohm. This is applicable with any combination of outputs using continuous duty.

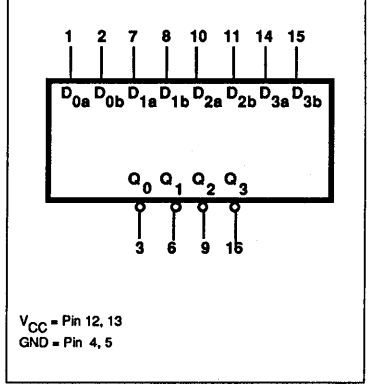
The AC specifications for the 74F3038 were determined using the standard FAST load for open-collector parts of 50 pf capacitance, a 500 ohm pull-up resistor and a 500 ohm pull-down resistor. (See Test Circuit).

Reducing the load resistors to 100 ohm will decrease the t_{PLH} propagation delay by approximately 50 % while increasing t_{PHL} only slightly. The graph of typical propagation delay vs load resistor (See AC Characteristics section for Graph) shows a spline fit curve from four measured data points. R_L=30 ohm, R_L=100 ohm, R_L=300 ohm, and R_L=500 ohm.

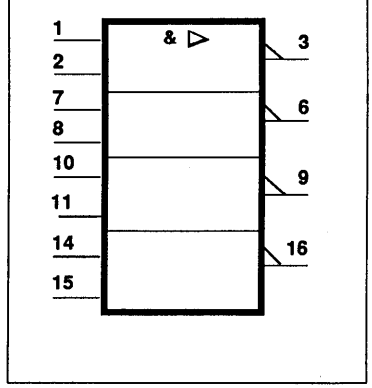
PIN CONFIGURATION



LOGIC SYMBOL

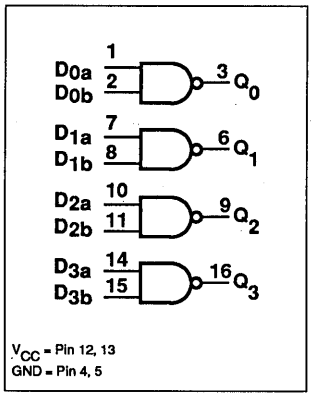


LOGIC SYMBOL (IEEE/IEC)



30Ω Line Driver | FAST 74F3038

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
D_{na}	D_{nb}	$\overline{Q}_n$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	320	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			160	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

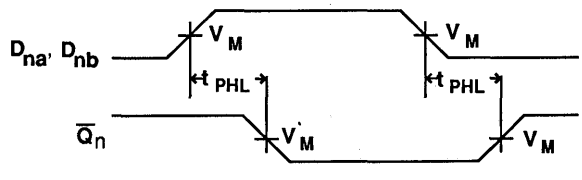
SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OL}	Low-level output current		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		.42	.55	V
				I_{OL} = 160mA[3]	±5%V_{CC}			.80	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} =MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{CC}	Supply current [total]	I_{CCH}	V_{CC} = MAX		V_{IN} =GND		3.5	6.0	mA
		I_{CCL}			V_{IN} = 4.5V		30	40	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30Ω transmission line on the incident wave.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb} to $\overline{Q}_n$	Waveform 1	6.0 1.5	9.5 3.0	12.0 5.0	5.5 1.5	12.5 5.5	ns

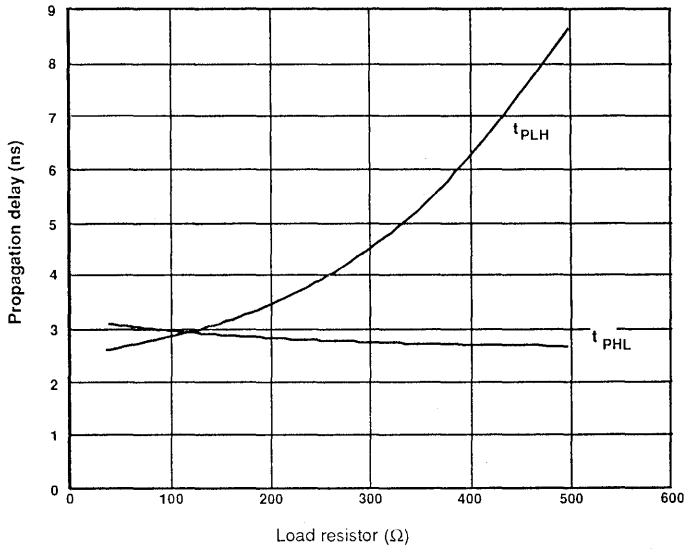
AC WAVEFORMS



Waveform 1.Propagation Delay for Inputs to Output

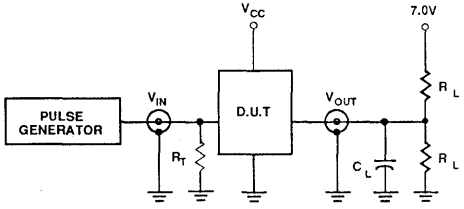
NOTE: For all waveforms, V_M = 1.5V.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



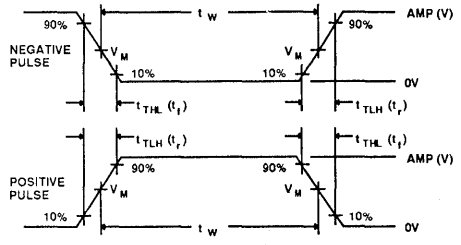
Test Circuit For Open Collector Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FEATURES

- **30Ω line driver**
- **160mA output drive capability in the Low state**
- **67mA output drive capability in the High state**
- **High speed**
- **Facilitates incident wave switching**
- **3nh lead inductance each on V_{CC} and GND when both side pins are used**

DESCRIPTION

The 74F3040 is a high current Line Driver composed of two 4-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The drive capability of the 'F3040 is 67mA source and 160mA sink with a V_{CC} as low as 4.5V. This guarantees incident wave switching with V_{OH} not less than 2.0V and V_{OL} not more than 0.8V while driving impedances as low as 30 ohms. This is applicable with any combination of outputs using continuous duty.
The propagation delay of the part is minimally affected by reflections when terminated only by the TTL inputs of other devices, Performance may be improved by full or partial line termination.

FAST 74F3040
30Ω Line Driver

Dual 4-Input NAND 30Ω Line Driver

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3040	3.7 ns	7.5 mA

ORDERING INFORMATION

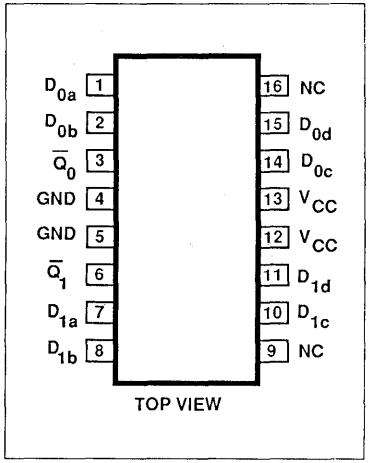
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F3040N
16-Pin Plastic SO	N74F3040D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

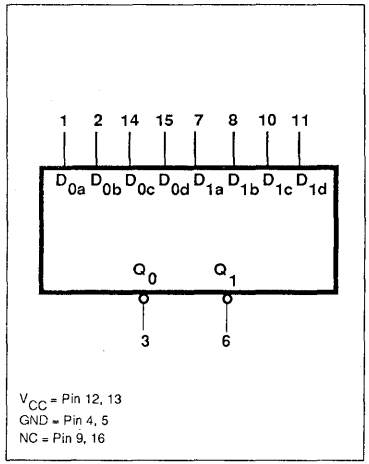
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}, D_{nc}, D_{nd}	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Q}_n$	Data output	3350/266	67mA/160mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

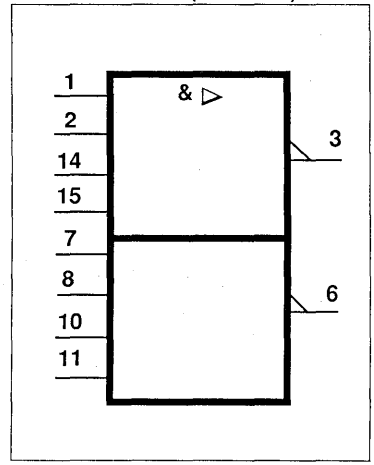
PIN CONFIGURATION



LOGIC SYMBOL

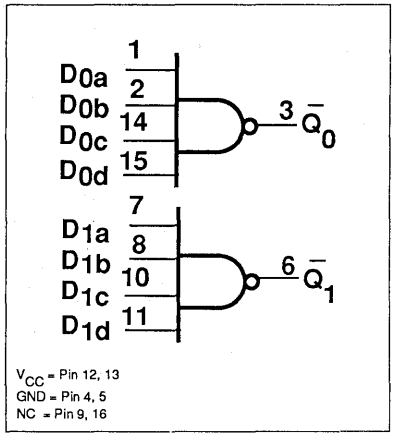


LOGIC SYMBOL (IEEE/IEC)



30Ω Line Driver | FAST 74F3040

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT
D_{na}	D_{nb}	D_{nc}	D_{nd}	$\overline{Q}_n$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't carre

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	320	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-67	mA
I_{OL}	Low-level output current			160	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

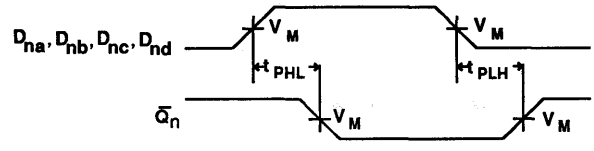
SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -45mA	±10%V_{CC}	2.5			V
				I_{OH1} = -67mA[3]	±5%V_{CC}	2.7			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		0.42	0.55	V
				I_{OL1} = 160mA[4]	±5%V_{CC}			0.80	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_O	Output current[5]		V_{CC} = MAX, V_O = 2.25V			-80		-180	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				2.0	4.0	mA
		I_{CCL}					14	20	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH1} is the current necessary to guarantee the Low to High transition in a 30 ohm transmission line on the incident wave.
4. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30 ohm transmission line on the incident wave.
5. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd} to $\overline{Q}_n$	Waveform 1	2.5 1.0	4.5 2.5	6.5 4.5	2.5 1.0	7.0 5.0	ns

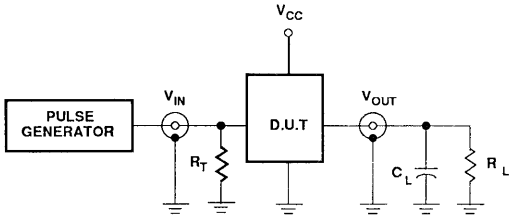
AC WAVEFORMS



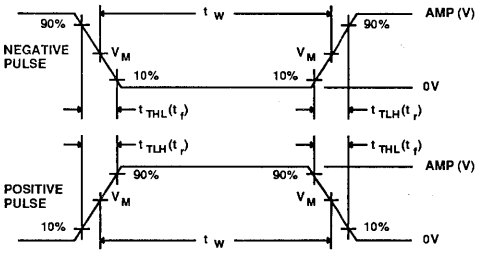
Waveform 1. Propagation Delay for Inputs to Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F3893

Quad FutureBus Backplane Transceiver (3 State +Open Collector)

FAST Products

Preliminary Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3893	3.5ns	70mA

FEATURES

- **Quad Backplane Transceiver**
- **Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms**
- **Reduced voltage swing (1 volt) produces less noise and reduces power consumption**
- **High speed operation enhances performance of backplane buses and facilitates incident wave switching**
- **Compatible with IEEE 896 Futurebus Standards**
- **Built-in precision band-gap (BG) reference provides accurate receiver threshold and improved noise immunity**
- **Controlled output ramp and multiple GND pins minimize ground bounce**
- **Glitch-free power up / power down operation**
- **Pin and function compatible with NSC DS3893**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
20-Pin PLCC	N74F3893A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/0.167	20µA/100µA
DE	Data Enable input	1.0/0.667	20µA/400µA
$\overline{RE}$	Receiver Enable input	1.0/0.167	20µA/100µA
I/O_0- I/O_3	Receiver inputs	1.0/0.083	20µA/50µA
I/O_0- I/O_3	Driver outputs	OC/33	OC/24mA
R_0 - R_3	Receiver outputs	150/40	3mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
OC = Open Collector

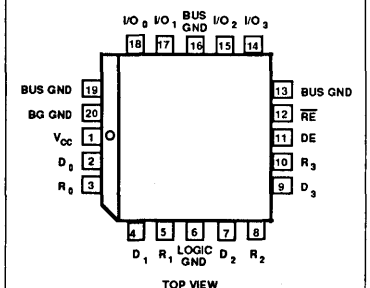
DESCRIPTION

The 74F3893 is a quad backplane transceiver and is intended to be used in very high speed bus systems.

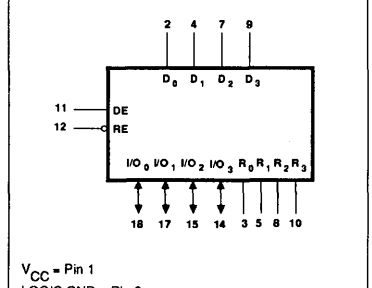
The 74F3893 interfaces to 'Backplane Transceiver Logic' (BTL) . BTL features a reduced (1V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading (< 7 pF). Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.

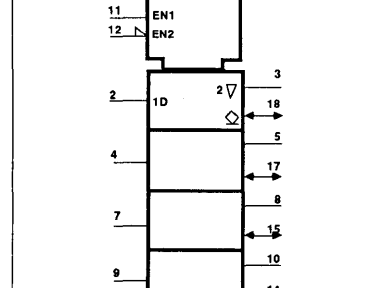
PIN CONFIGURATION



LOGIC SYMBOL

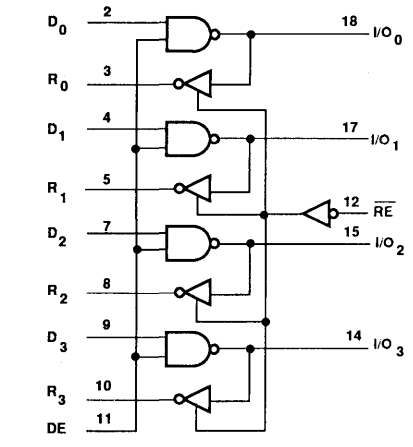


LOGIC SYMBOL(IEEE/IEC)



Quad Backplane Transceiver | FAST 74F3893

LOGIC DIAGRAM



V_{CC} = Pin 1

LOGIC GND = Pin 6

BUS GND = Pin 13, 16, 19

BG GND = Pin 20

FUNCTION TABLE

INPUTS			INPUT/OUTPUT	OUTPUT	OPERATING MODE
DE	$\overline{RE}$	D_n	I/O_n	R_n	
H	X	L	H	L	Transmit
H	X	H	L	H	
H	H	D_n	$\overline{D}_n$	Z	Receiver 3-state
L	H	X	H	Z	Transmit to bus
L	L	X	H	L	Receive
L	L	X	L	H	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-1.5 to +6.5	V
V_{IN}	Input voltage	-1.5 to +6.5	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
V_{TH}	Receiver input threshold		1.475	1.55	1.625	V
I_{OH}	High-level output current	R_n only			-3	mA
I_{OL}	Low-level output current				24	mA
C_{IN}	Bus-port capacitance at I/O_n=V_T=2V				7	pF
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
I_{OHB}	High-level output current	I/O_n(Power on)	V_{CC}=MIN, V_{IL} = MAX, V_{IH} =MIN, V_{OH} = 1.5V		10	100	µA
		I/O_n(Power off)	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} =MIN, V_{OH} = 1.5V			100	µA
V_{OH}	High-level output voltage	R_n	V_{CC} = MIN, V_{IL}= MAX, I_{OH} = MAX	2.5			V
V_{OHB}	High-level output Bus voltage	I/O_n	V_{CC} = MAX , D_n =0.8V, V_T= 2.0V, R_T= 10Ω	1.9			V
V_{OL}	Low-level output voltage	R_n	V_{CC} = MIN, V_{IN} = 2.0V, I_{OL} = 6mA, I/O_n =2V $\overline{RE}$=0.8V		0.35	0.5	V
V_{OLB}	Low-level output Bus voltage	I/O_n	D_n = DE = V_{IH}, V_T= 2.2V, R_T= 10Ω	0.75	1.0	1.2	V
			D_n = DE = V_{IH}, V_T= 2.14V, R_T= 18.5Ω	0.75	1.0	1.1	V
V_{OCB}	Driver output positive clamp voltage	I/O_n	V_{CC} = MAX or 0V, I/O_n =1mA	1.9		2.9	V
			V_{CC} = MAX or 0V, I/O_n =10mA	2.3		3.2	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}		-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V, DE = $\overline{RE}$ = D_n = V_{CC}			1	mA
I_{IH}	High-level input current	D_n, $\overline{RE}$, DE	V_{CC} = MAX, V_I = 2.7V, DE = $\overline{RE}$ = D_n = 2.4V			40	µA
I_{IHB}	High level output bus current (power off)	I/O_n	V_{CC} = 0V, D_n = DE = 0.8V, I/O_n = 1.2V			100	µA
I_{IL}	Low-level input current	D_n, $\overline{RE}$	V_{CC} = MAX, V_I = 0.5V, DE = V_{CC} = MAX			-100	µA
		DE	V_{CC} = MAX, V_I = 0.5V, D_n = V_{CC} = MAX			-700	µA
I_{ILB}	Low-level output bus current (power on)		V_{CC} = MAX, D_n = DE = 0.8V, I/O_n = 0.75V	-250		100	µA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = MAX, V_O =2.5V, $\overline{RE}$=2V			20	µA
I_{CZL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O =0.5V, $\overline{RE}$=2V			-20	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX, I/O_n = 1.2V, V_O =0V, $\overline{RE}$=0.8V	-80		-200	mA
I_{CC}	Supply current (total)		V_{CC} = MAX, D_n = DE =$\overline{RE}$ =V_{IH}		70	100	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for Driver and Driver Enable

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V, V_T=2V C_L = 30pF R_T = 10Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10%, V_T=2V C_L = 30pF R_T = 10Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to I/O_n	Waveform 1	2.0 2.0	3.5 3.5	6.0 6.0	2.6 1.5	6.75 6.0	ns
t_{PLH} t_{PHL}	Propagation delay DE to I/O_n	Waveform 1		3.5 3.5		2.6 1.5	6.75 6.0	ns
t_{TLH} t_{THL}	D_n to I/O_n Transition time 10% to 90%, 90% to 10%	Waveform 1				1.0 1.0	5.0 5.0	ns
t_{Dskew}	Skew between Drivers in same package			1.0				ns

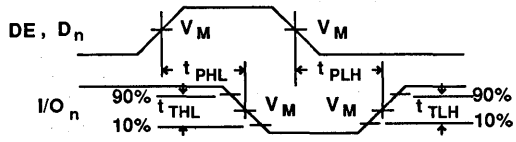
AC ELECTRICAL CHARACTERISTICS for Receiver

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 30pF R_L = 1kΩ			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 30pF R_L = 1kΩ		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I/O_n to R_n	Waveform 1		3.5 3.5		3.1 3.6	8.0 7.25	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 2		1.0				ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 3						ns
t_{Rskew}	Skew between Receivers in same package							ns

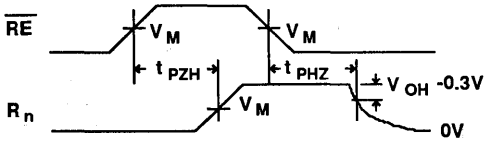
AC ELECTRICAL CHARACTERISTICS for Receiver Enable

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Output Enable to High or Low level $\overline{RE}$ to R_n	Waveform 2 Waveform 3		9.0 10.0		2.0 2.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Output Disable from High or Low level $\overline{RE}$ to R_n	Waveform 2 Waveform 3		4.0 4.0		1.0 1.0	8.0 8.0	ns

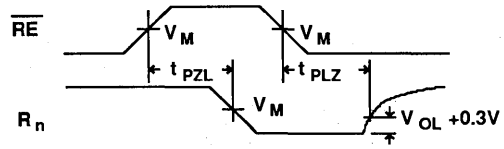
AC WAVEFORMS



Waveform 1. Propagation Delay For Driver



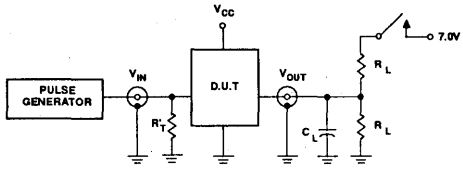
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

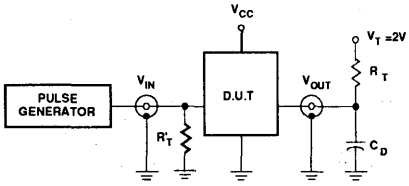
TEST CIRCUIT AND WAVEFORMS



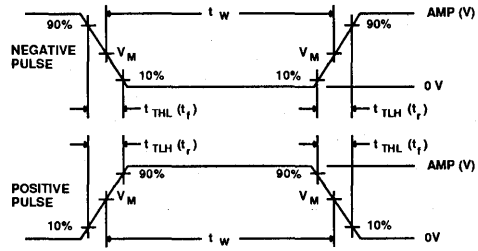
Test Circuit For 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test Circuit For Open Collector Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R'_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistor; see AC CHARACTERISTICS for value.

FAST 74F4763

4-MBit Intelligent DRAM Controller

FAST Products

Preliminary Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F4763	150MHz	175mA

FEATURES

- **DRAM signal timing generator**
- **Automatic refresh circuitry**
- **Dual Ported arbitration**
- **Selectable row address hold and RAS precharge times**
- **Supports Page and Nibble Mode accesses**
- **On-chip column address counter**
- **Multiple CAS outputs with CAS enables for byte addressing**
- **Controls 4-MBit DRAMs**
- **Intelligent burst-mode refresh after page mode access cycles**

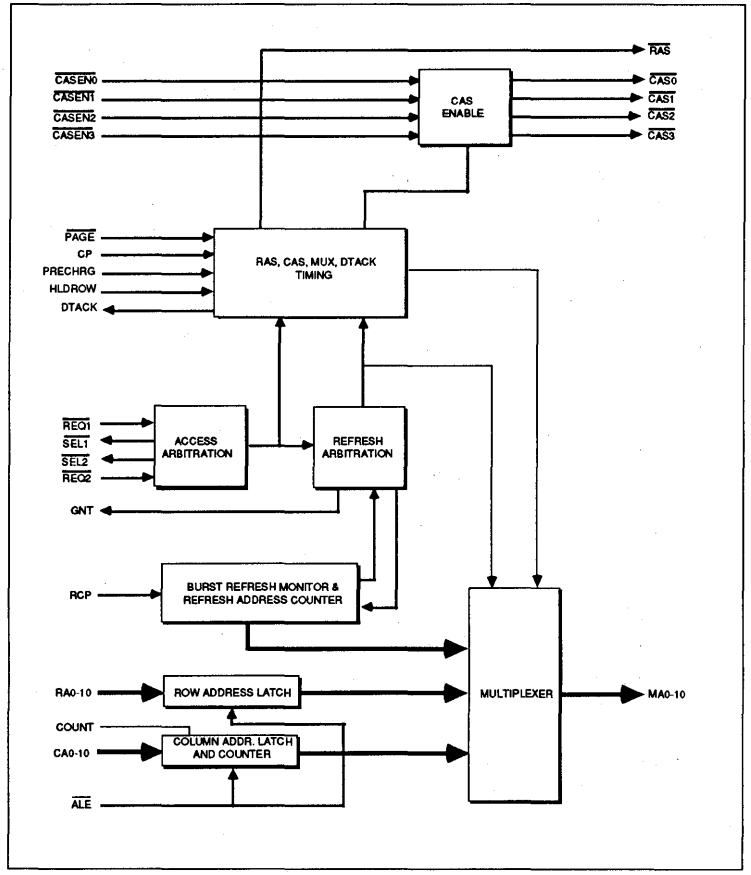
ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
64-Pin Plastic DIP	N74F4763N
68-Pin Plastic PLCC	N74F4763A

PRODUCT DESCRIPTION

The Signetics 4-MBit Intelligent DRAM Controller is a 4-MBit dual-ported version of the 'F1763 Intelligent DRAM Controller. It contains automatic signal timing, address multiplexing, refresh control, and access and refresh arbitration. Additional features include multiple CAS outputs, selectable row address hold and $\overline{RAS}$ precharge times, page mode support and on-chip column address counter for all major modes of burst access to the DRAMs.

BLOCK DIAGRAM



Signetics

FAST Products

FAST 74F5074 FLIP-FLOP

Synchronizing Dual D-Type Flip-Flop With Metastable Immune Charateristics

Preliminary Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F5074	200 MHz	18mA

FEATURES

- **Metastable Immune Characteristics**
- **Propagation delay skew and output to output skew less than 1.5ns**
- **Same pinout and function as 74F74**
- **See 74F50728 for Synchronizing Cascaded D-Type Flip-Flop**
- **See 74F50729 for Synchronizing Cascaded Dual D-Type Flip-Flop with Edge-Triggered Set and Reset**
- **See 74F50109 for Synchronizing Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flops**

DESCRIPTION

The 74F5074 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also true and complementary outputs.

Set ($\overline{S}_n$) and Reset ($\overline{R}_n$) are asynchronous active-Low inputs and operate independently of the Clock (CP) input. Data must be stable just one setup time prior to the Low-to-High transition of the clock for guaranteed propagation delays.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D input may be changed without affecting the levels of the output.

The 74F5074 is designed so that the outputs can never display a metastable state due to setup and hold times violations. If setup and hold times are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F5074 are: τ < .200ns, T_o=10 µs, and h=3.8ns.

ORDERING INFORMATION

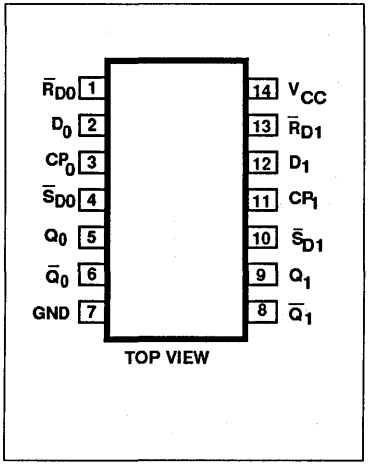
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F5074N
14-Pin Plastic SO	N74F5074D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

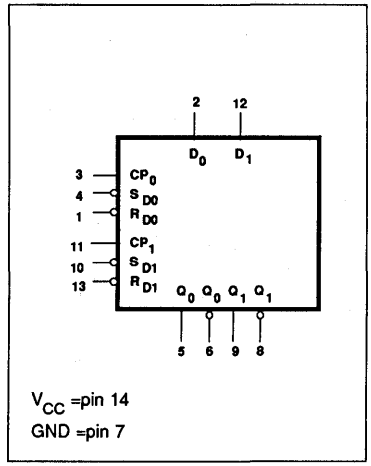
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0, D_1	Data inputs	1.0/0.166	20µA/100µA
CP_0, CP_1	Clock inputs (active rising edge)	1.0/0.083	20µA/50µA
$\overline{S}_{D0}$, $\overline{S}_{D1}$	Set inputs (active Low)	1.0/0.083	20µA/50µA
$\overline{R}_{D0}$, $\overline{R}_{D1}$	Reset inputs (active Low)	1.0/0.083	20µA/50µA
Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

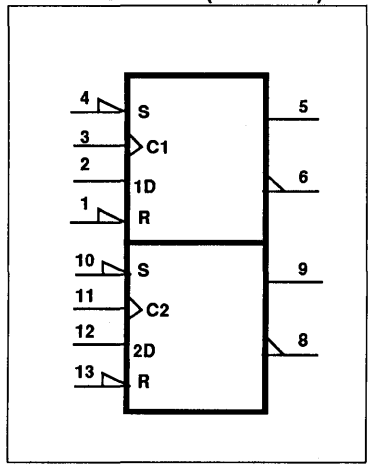
PIN CONFIGURATION



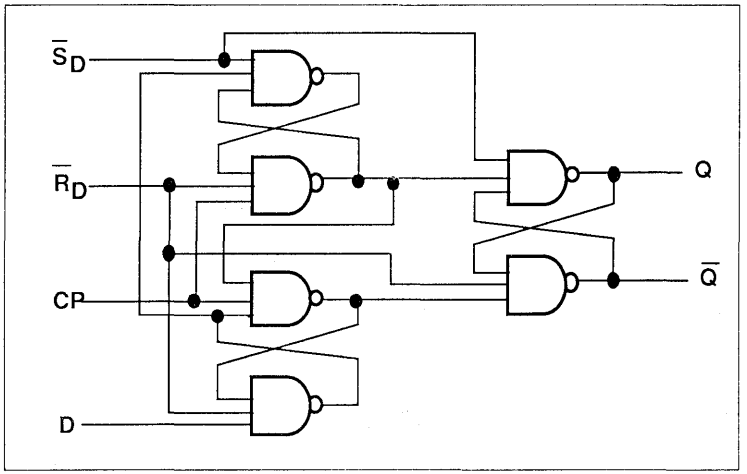
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$	
L	H	X	X	H	L	Asynchronous Set
H	L	X	X	L	H	Asynchronous Reset
L	L	X	X	H	H	Undetermined*
H	H	↑	h	H	L	Load "1"
H	H	↑	l	L	H	Load "0"
H	H	↥	X	NC	NC	Hold

H = High voltage level
h = High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
X = Don't care

↑ = Low-to-High clock transition
↥ = Low-to-High clock transition
NC =No change from the previous setup
* = This setup is unstable and will change when either Set or Reset return to the High level.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} =MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} =MAX	±10%V_{CC}		0.30	0.50	V
			±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current $\frac{D_n}{CP_n, \overline{S}_{Dn}, \overline{R}_{Dn}}$	V_{CC} = MAX, V_I = 0.5V				-100	µA
						-50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			18	24	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs High in turn.

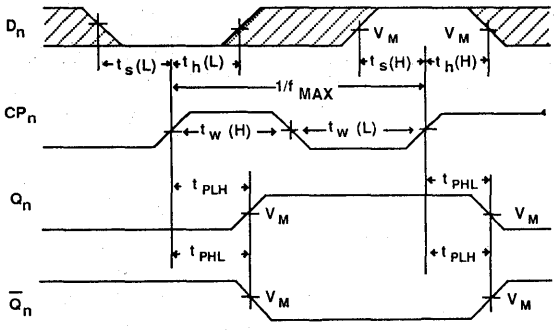
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1		200		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	3.8 3.8	4.5 5.0	2.0 2.0	5.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_{Dn}$ to Q_n or $\overline{Q}_n$	Waveform 2	2.0 2.0	3.8 3.8	4.5 5.0	2.0 2.0	5.5 6.0	ns

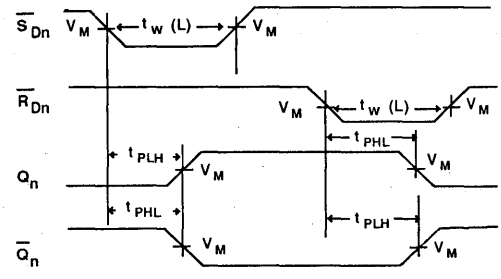
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP_n	Waveform 1	1.0 1.0			1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP_n	Waveform 1	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	$\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ Pulse width, Low	Waveform 2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to CP_n	Waveform 3	2.0			2.0		ns

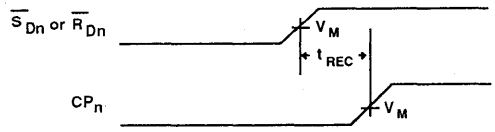
AC WAVEFORMS



Waveform 1. Propagation Delay For data to output, data setup time and hold times, and clock width



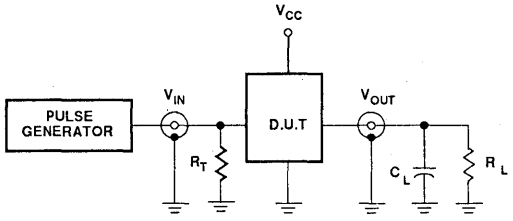
Waveform 2.
Propagation Delay for set and reset to output, set and reset pulse width



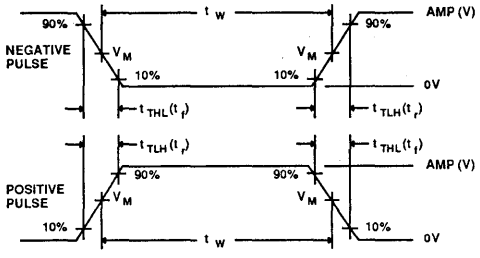
Waveform 3.
Recovery time for set or reset to clock

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F5300 LED Driver

FAST Products

Objective Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F5300	3.8 ns	5.0mA

FEATURES

- TTL inputs
- Output enable control
- Single supply
- High current source and sink capability

APPLICATIONS

- High speed serial data communication
- Fiber optic data links
- Local area and metropolitan area networks
- Digital Television
- PBX systems

ASSOCIATED PRODUCTS

- NE 5210/11/12 transimpedance amplifiers
- NE5214/5217 postamplifier with data quantizer

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
8-Pin Plastic SO	74F5300D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D	Data input	1.0/1.0	20µA/0.6mA
E	Enable input	1.0/1.0	20µA/0.6mA
Q	Data output	3350/200	67mA/120mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

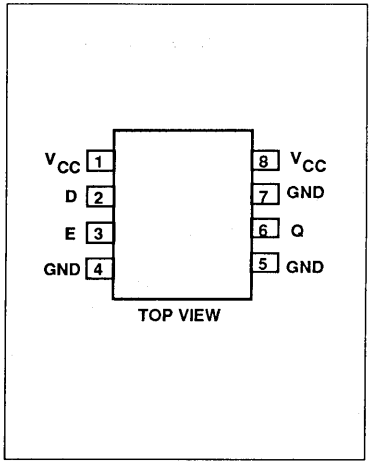
The 74F5300 is an LED driver designed for use in fiber optics links.

The TTL input buffer accepts TTL data. A logic High on the Enable pin enables the buffer to drive the output driver amplifier.

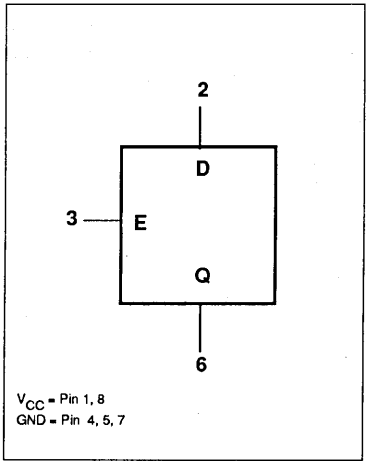
The output driver amplifier is capable of sourcing more than 60 mA and sinking more than 120 mA from low impedances.

The high current output driver has been designed to deal with transmission line effects of high speed switching systems with fast rising and falling edges. The performance of the system can be enhanced by matching impedance at the output for proper termination.

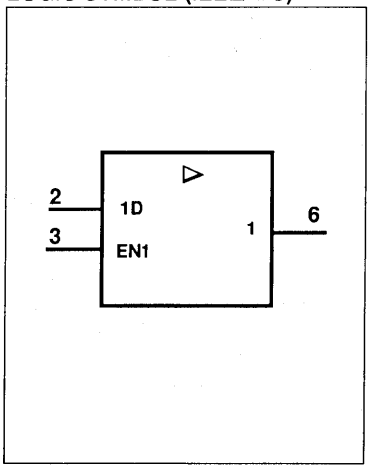
PIN CONFIGURATION



LOGIC SYMBOL

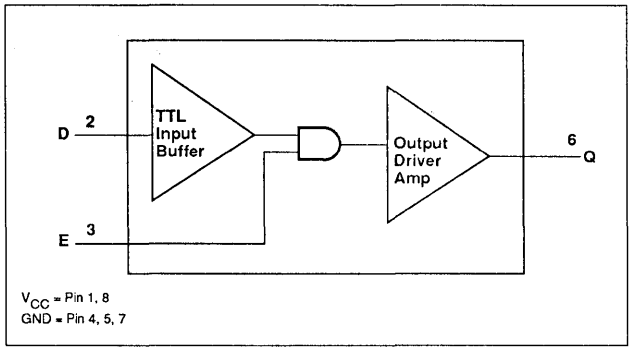


LOGIC SYMBOL (IEEE/IEC)

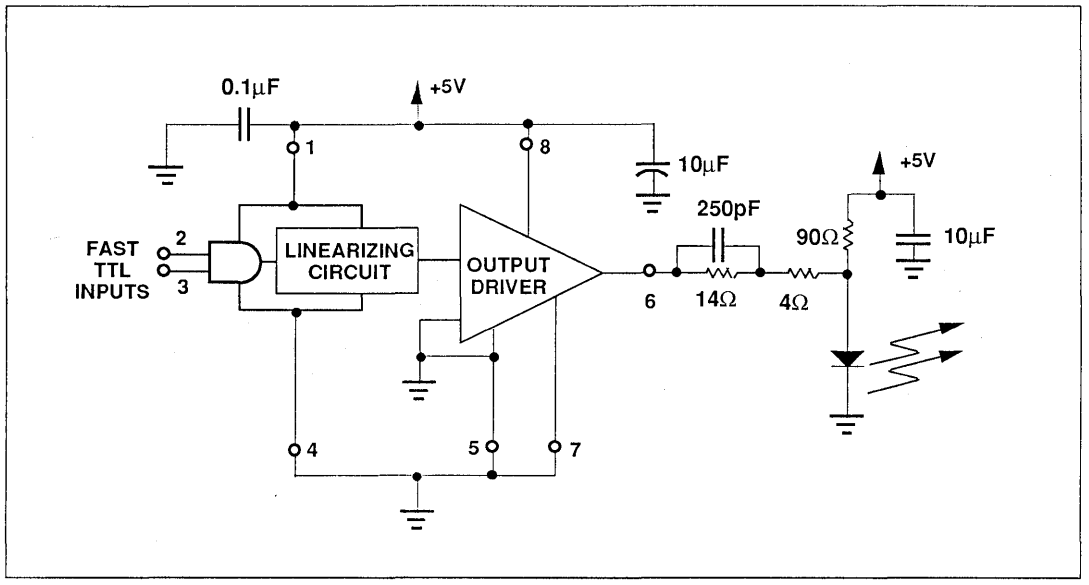


LED Driver | FAST 74F5300

LOGIC DIAGRAM



APPLICATION



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	240	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-67	mA
I_{OL}	Low-level output current			120	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

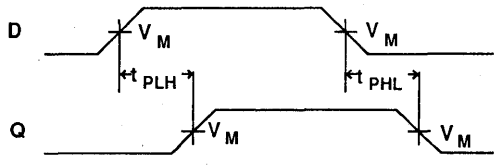
SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -45mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = -67mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		0.42	0.55	V
				I_{OL} = 120mA	±5%V_{CC}		0.45	0.60	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				2.0	4.0	mA
		I_{CCL}					8.0	12	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. The device is not short circuit protected.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 100Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 100Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D to Q	Waveform 1	2.5 2.5	3.8 3.8	6.0 6.0			ns
D_{tpw}	Pulse width distortion			0.4				ns
t_{THL} t_{TLH}	Rise time 10% to 90% Fall time 90% to 10%	Test circuits and Waveforms		1.2 1.2				ns

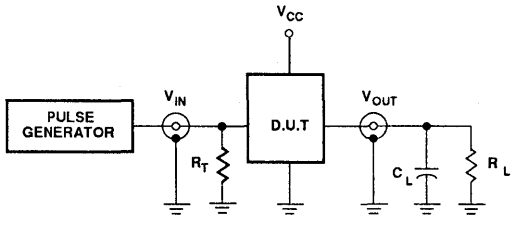
AC WAVEFORMS



Waveform 1. Propagation Delay for Input to Output

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



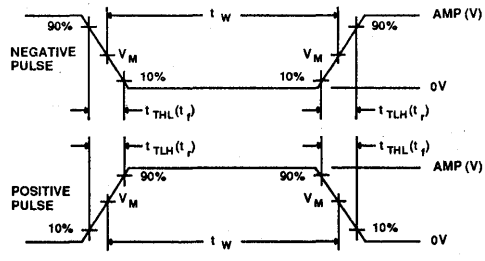
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F8960, 74F8961
Futurebus Transceivers

FAST Products

Preliminary Specification for
74F8960-Octal Latched Bidirectional Futurebus Transceiver, INV (OC)
Product Specification for
74F8961-Octal Latched Bidirectional Futurebus Transceiver, NINV (OC)

TYPE	TYPICAL PROPAGATION DELAY	MAX SUPPLY CURRENT (TOTAL)
74F8960	7.5ns	85mA
74F8961	7.5ns	85mA

FEATURES

- Octal Latched Transceiver
- Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms
- High drive (100mA) open collector drivers on B-port
- Reduced voltage swing (1 volt) produces less noise and reduces power consumption
- High speed operation enhances performance of backplane buses and facilitates incident wave switching
- Compatible with IEEE 896 Futurebus Standard
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch-free power up / power down operation

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
28-Pin Plastic DIP (600 mil)[1]	N74F8960N, N74F8961N
28-Pin PLCC[1]	N74F8960A, N74F8961A

NOTE:
1. Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	PNP latched inputs	3.5/0.0117	70µA/70µA
B_0 - B_7	Data inputs with threshold circuitry	5.0/0.167	100µA/100µA
OEA	A Output Enable input (active High)	1.0/0.033	20µA/20µA
$\overline{OEB}_0$, $\overline{OEB}_1$	B Output Enable inputs (active Low)	1.0//0.033	20µA/20µA
$\overline{LE}$	Latch Enable input (active Low)	1.0//0.033	20µA/20µA
A_0 - A_7	3-State outputs	150/40	3mA/24mA
B_0 - B_7	Open Collector outputs	OC*/166.7	OC*/100mA

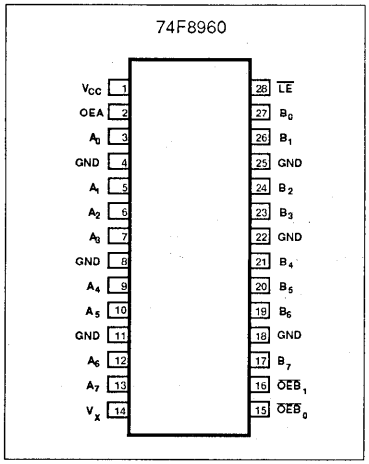
NOTES:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.
* OC = Open Collector

DESCRIPTION

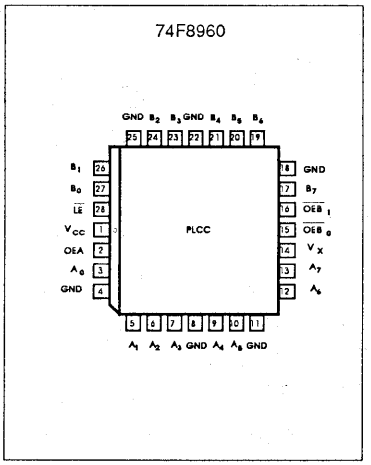
The 74F8960 and 74F8961 are octal bidirectional latched transceivers and are intended to provide the electrical interface to a high performance wired-OR bus. The B port inverting drivers are low-capacitance open collector with controlled ramp and are designed to sink 100 mA from 2 volts. The B port receivers have a 100 mV threshold region and a 4 ns glitch filter.

The B port interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading (<5 pF).

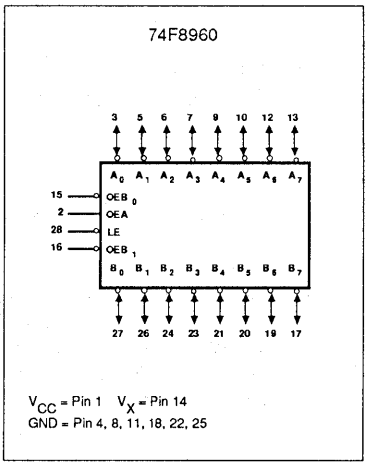
PIN CONFIGURATION DIP



PIN CONFIGURATION PLCC



LOGIC SYMBOL



DESCRIPTION (Continued)

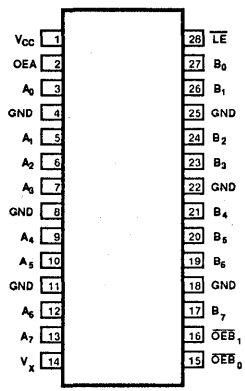
Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane. The 74F8960 and 74F8961 A ports have TTL 3-State drivers and TTL receivers with a latch function. A separate High level control input (V_X) is provided to limit the A port output level to a given voltage level (such as 3.3V). For 5.0V systems, V_x is simply tied to V_{CC}.

74F8961 is the non-inverting version of 74F8960.

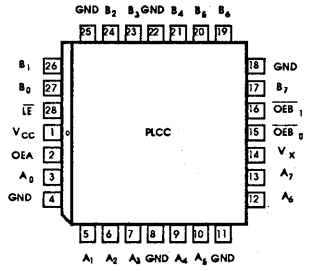
PIN CONFIGURATION

74F8961



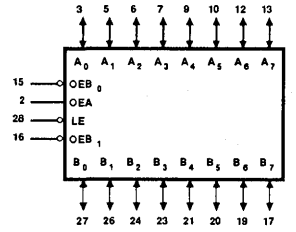
PIN CONFIGURATION PLCC

74F8961



LOGIC SYMBOL

74F8961

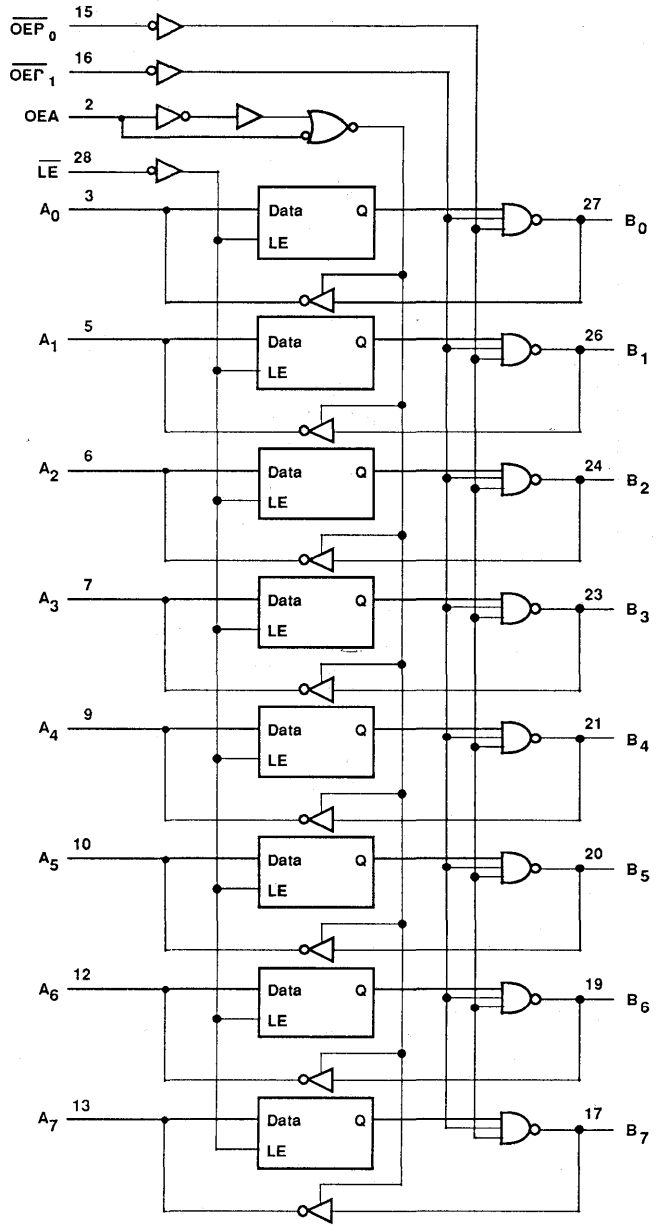


V_{CC} = Pin 1 V_X = Pin 14
GND = Pin 4, 8, 11, 18, 22, 25

PIN DESCRIPTION

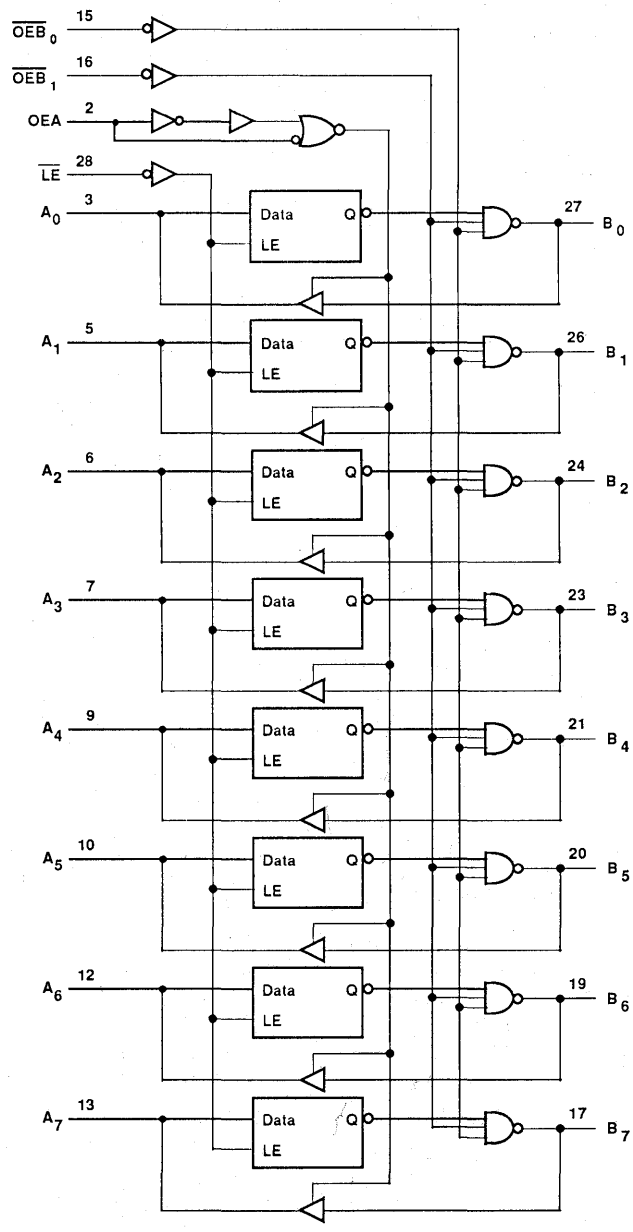
SYMBOL	PINS	TYPE	NAME AND FUNCTION
A_0	3	I/O	PNP latched input / 3-state output (with V_X control option)
A_1	5	I/O	
A_2	6	I/O	
A_3	7	I/O	
A_4	9	I/O	
A_5	10	I/O	
A_6	12	I/O	
A_7	13	I/O	
B_0	27	I/O	Data input with special threshold circuitry to reject noise / Open Collector output, High current drive
B_1	26	I/O	
B_2	24	I/O	
B_3	23	I/O	
B_4	21	I/O	
B_5	20	I/O	
B_6	19	I/O	
B_7	17	I/O	
$\overline{OEB}_0$	15	I	Enables the B outputs when both pins are Low
$\overline{OEB}_1$	16	I	
OEA	2	I	Enables the A outputs when High
$\overline{LE}$	28	I	Latched when High (a special delay feature is built in for proper enabling times)
V_X	14	I	Clamping voltage keeping V_{OH} from rising above V_X ($V_X = V_{CC}$ for normal use)

LOGIC DIAGRAM 74F8960



V_{CC} = Pin 1 V_X = Pin 14
GND = Pin 4, 8, 11, 18, 22, 25

LOGIC DIAGRAM 74F8961



V_{CC} = Pin 1 V_X = Pir
GND = Pin 4, 8, 11, 18, 22, 25

FUNCTION TABLE 74F8960

INPUTS						LATCH	OUTPUTS		MODE
A_n	B_n*	$\overline{LE}$	OEA	$\overline{OEB}_0$	$\overline{OEB}_1$	STATE	A_n	B_n	
H	X	L	L	L	L	H	Z	L	A 3-state, Data from A to B
L	X	L	L	L	L	L	Z	H**	
X	X	H	L	L	L	Q_n	Z	$\overline{Q}_n$	A 3-state, Latched data to B
–	–	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	L	L(2)	L	Z(2)	Preconditioned Latch enabling data transfer from B to A
–	L	H	H	L	L	L(2)	H	Z(2)	
–	–	H	H	L	L	Q_n	$\overline{Q}_n$	$\overline{Q}_n$	Latch state to A and B
H	X	L	L	H	X	H	Z	Z	B and A 3-state
L	X	L	L	H	X	L	Z	Z	
X	X	H	L	H	X	Q_n	Z	Z	
–	H	L	H	H	X	H	L	Z	B 3-state, Data from B to A
–	L	L	H	H	X	L	H	Z	
–	H	H	H	H	X	Q_n	L	Z	
–	L	H	H	H	X	Q_n	H	Z	
H	X	L	L	X	H	H	Z	Z	B and A 3-state
L	X	L	L	X	H	L	Z	Z	
X	X	H	L	X	H	Q_n	Z	Z	
–	H	L	H	X	H	H	L	Z	B 3-state, Data from B to A
–	L	L	H	X	H	L	H	Z	
–	H	H	H	X	H	Q_n	L	Z	
–	L	H	H	X	H	Q_n	H	Z	

H = High voltage level
L = Low voltage level
X = Don't care
– = Input not externally driven
Z = High Impedance (off) state
Q_n = High or Low voltage level one setup time prior to the Low-to-High $\overline{LE}$ transition
(1) = Condition will cause a feedback loop path; A to B and B to A
(2) = The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB}_0$ and $\overline{OEB}_1$ are Low and $\overline{LE}$ is High.
H** = Goes to level of pullup voltage.
B* = Precaution should be taken to insure B inputs do not float. If they do they are equal to Low state.

FUNCTION TABLE. 74F8961

INPUTS						LATCH	OUTPUTS		MODE
A_n	B_n*	$\overline{LE}$	OEA	$\overline{OEB_0}$	$\overline{OEB_1}$	STATE	A_n	B_n	
H	X	L	L	L	L	H	Z	H**	A 3-state, Data from A to B
L	X	L	L	L	L	L	Z	L	
X	X	H	L	L	L	Q_n	Z	Q_n	A 3-state, Latched data to B
–	–	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
–	H	H	H	L	L	H(2)	H	Z(2)	Preconditioned Latch enabling data transfer from B to A
–	L	H	H	L	L	H(2)	L	Z(2)	
–	–	H	H	L	L	Q_n	Q_n	Q_n	Latch state to A and B
H	X	L	L	H	X	H	Z	Z	B and A 3-state
L	X	L	L	H	X	L	Z	Z	
X	X	H	L	H	X	Q_n	Z	Z	
–	H	L	H	H	X	H	H	Z	B 3-state, Data from B to A
–	L	L	H	H	X	L	L	Z	
–	H	H	H	H	X	Q_n	H	Z	
–	L	H	H	H	X	Q_n	L	Z	
H	X	L	L	X	H	H	Z	Z	B and A 3-state
L	X	L	L	X	H	L	Z	Z	
X	X	H	L	X	H	Q_n	Z	Z	
–	H	L	H	X	H	H	H	Z	B 3-state, Data from B to A
–	L	L	H	X	H	L	L	Z	
–	H	H	H	X	H	Q_n	H	Z	
–	L	H	H	X	H	Q_n	L	Z	

H = High voltage level
L = Low voltage level
X = Don't care
– = Input not externally driven
Z = High Impedance (off) state
Q_n = High or Low voltage level one setup time prior to the Low-to-High $\overline{LE}$ transition
(1) = Condition will cause a feedback loop path; A to B and B to A
(2) = The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB}_0$ and $\overline{OEB}_1$ are Low and $\overline{LE}$ is High.
H** = Goes to level of pullup voltage.
B* = Precaution should be taken to insure B inputs do not float. If they do they are equal to Low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_X	Threshold control		-0.5 to +7.0	V
V_{IN}	Input voltage	$\overline{OEB}_n$, OEA, $\overline{LE}$	-0.5 to +7.0	V
		A_0 - A_7, B_0 - B_7	-0.5 to 5.5	
I_{IN}	Input current		-40 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A_0 - A_7	48	mA
		B_0 - B_7	200	
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except B_0 - B_7	2.0			V
		B_0 - B_7	1.625			
V_{IL}	Low-level input voltage	Except B_0 - B_7			0.8	V
		B_0 - B_7			1.475	
I_{IK}	Input clamp current	Except A_0 - A_7			-18	mA
		A_0 - A_7			-40	
I_{OH}	High-level output current	A_0 - A_7			-3	mA
I_{OL}	Low-level output current	A_0 -A_7			24	mA
		B_0 - B_7			100	
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
I_{OH}	High level output current	B_0 - B_7	V_{CC} = MAX, V_{IL} =MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
I_{OFF}	Power-off output current	B_0 - B_7	V_{CC} = 0.0V, V_{IL} =MAX, V_{IH} = MIN, V_{OH} = 2.1V				100	µA
V_{OH}	High-level output voltage	A_0 - A_7[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = -3mA, V_X = V_{CC}	2.5		V_{CC}	V
				I_{OH} = -0.4mA, V_X = 3.13V & 3.47V	2.5		V_X	V
V_{OL}	Low-level output voltage	A_0 - A_7[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 20mA, V_X = V_{CC}			0.5	V
		B_0 - B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA			1.15	V
				I_{OL} = 4mA	0.40			V
V_{IK}	Input clamp voltage	A_0 - A_7	V_{CC} = MIN, I_I = I_{IK}				-0.5	V
		Except A_0 - A_7	V_{CC} = MIN, I_I = I_{IK}				-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = 0.0V, V_I = 7.0V				100	µA
		A_0 - A_7, B_0 - B_7	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High-level input current	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 2.7V, B_n - A_n = 0V				20	µA
		B_0 - B_7	V_{CC} = MAX, V_I = 2.1V				100	µA
I_{IL}	Low-level input current	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = MAX, V_I = 0.5V				-20	µA
		B_0 - B_7	V_{CC} = MAX, V_I = 0.3V				-100	µA
I_{OZH} + I_{IH}	Off-state output current, High-level voltage applied	A_0 - A_7	V_{CC} = MAX, V_O =2.7V				70	µA
I_{OZL} + I_{IL}	Off-state output current, Low-level voltage applied	A_0 - A_7	V_{CC} = MAX, V_O =0.5V				-70	µA
I_X	High-level control current		V_{CC} = MAX, V_X = V_{CC}, $\overline{LE}$ = OEA = $\overline{OEB}_n$ = 2.7V, A_0 - A_7 = 2.7V, B_0 - B_7 = 2.0V		-100		100	µA
			V_{CC} = MAX, V_X = 3.13V & 3.47 V, $\overline{LE}$ = OEA = 2.7V, $\overline{OEB}_n$ = A_0 - A_7 = 2.7V, B_0 - B_7 = 2.0V		-10		10	mA
I_{OS}	Short-circuit output current[3]	A_0 - A_7 only	V_{CC} = MAX, B_n = 1.6V, OEA = 2.0V, $\overline{OEB}_n$ = 2.7V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			70	100	mA
		I_{CCL}	V_{CC} = MAX, V_{IL} = 0.5V			100	145	mA
		I_{CCZ}	V_{CC} = MAX, V_{IL} = 0.5V			80	100	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, V_X = V_{CC} for all test conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH}=1.6V and V_{IL}=1.3V.

AC ELECTRICAL CHARACTERISTICS for 74F8960

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay B to A	Waveform 1, 2	5.5 6.0	7.5 7.5	12.0 10.5	5.0 6.0	12.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time from High or Low OEA to A	Waveform 4.5	8.0 8.5	10.5 12.0	14.5 14.5	7.5 8.5	15.5 17.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low OEA to A	Waveform 4.5	2.0 2.0	4.5 4.5	7.0 7.5	2.0 2.0	7.5 8.0	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_D = 30pF R_U = 9Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_D = 30pF R_U = 9Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A to B	Waveform 1, 2	2.0 3.5	4.0 6.0	7.0 8.0	2.0 3.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to B	Waveform 1, 2	3.0 4.0	5.0 6.0	8.5 9.0	2.5 3.0	10.0 9.5	ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OEB}_n$ to B	Waveform 1, 2	2.5 4.5	4.5 7.5	7.5 10.5	1.5 3.5	8.5 10.5	ns
t_{TLH} t_{THL}	Transition time, B Port 1.3V to 1.7 V, 1.7V to 1.3V	Test Circuit and Waveforms	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	4.5 4.5	ns

AC SETUP REQUIREMENTS for 74F8960

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Set-up time A to $\overline{LE}$	Waveform 3	5.0 5.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time A to $\overline{LE}$	Waveform 3	0.0 0.0			0.0 0.0		ns
t_w(L)	$\overline{LE}$ Pulse width, Low	Waveform 3	6.0			6.0		ns

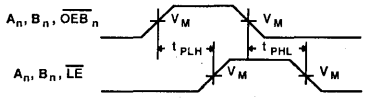
AC ELECTRICAL CHARACTERISTICS for 74F8961

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay B to A	Waveform 1, 2	5.5 6.0	7.5 7.5	12.0 10.5	5.0 6.0	12.0 11.0	ns
t_{PZH} t_{PZL}	Output Enable time from High or Low OEA to A	Waveform 4.5	8.0 8.5	10.5 12.0	14.5 14.5	7.5 8.5	15.5 17.0	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low OEA to A	Waveform 4.5	2.0 2.0	4.5 4.5	7.0 7.5	2.0 2.0	7.5 8.0	ns
SYMBOL	**PARAMETER**	**TEST CONDITION**	**B PORT LIMITS**					**UNIT**
			T_A = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 9Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_D = 30pF, R_U = 9Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A to B	Waveform 1, 2	2.0 3.5	4.0 6.0	7.0 8.0	2.0 3.0	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to B	Waveform 1, 2	3.0 4.0	5.0 6.0	8.5 9.0	2.5 3.0	10.0 9.5	ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OEB_n}$ to B	Waveform 1, 2	2.5 4.5	4.5 7.5	7.5 10.5	1.5 3.5	8.5 10.5	ns
t_{TLH} t_{THL}	Transition time, B Port 1.3V to 1.7 V, 1.7V to 1.3V	Test Circuit and Waveforms	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	4.5 4.5	ns

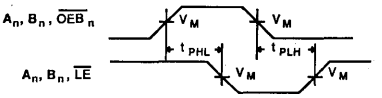
AC SETUP REQUIREMENTS for 74F8961

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Set-up time A to $\overline{LE}$	Waveform 3	5.0 5.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time A to $\overline{LE}$	Waveform 3	0.0 0.0			0.0 0.0		ns
t_w(L)	$\overline{LE}$ Pulse width, Low	Waveform 3	6.0			6.0		ns

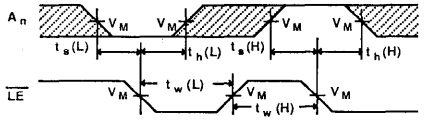
AC WAVEFORMS



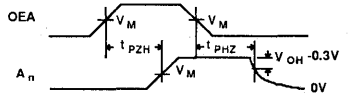
Waveform 1. Propagation Delay For Data To Output



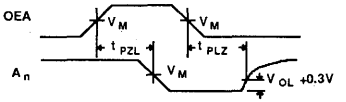
Waveform 2. Propagation Delay For Data To Output



Waveform 3. Data Setup And Hold Times And $\overline{LE}$ Pulse Widths



Waveform 4. 3-State Output Enable Time To High Level And Output Disable Time From High Level

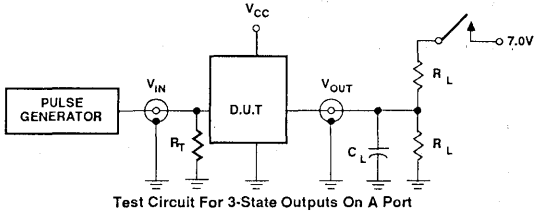


Waveform 5 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

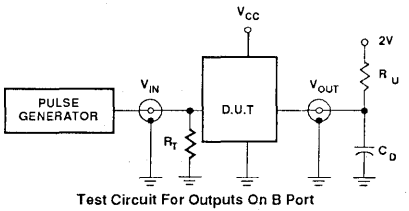
TEST CIRCUIT AND WAVEFORMS



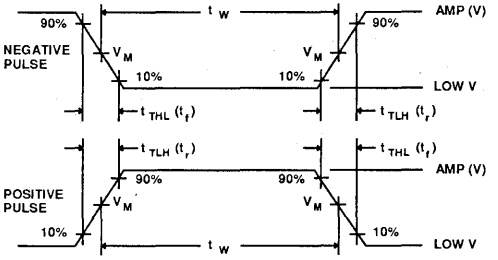
Test Circuit For 3-State Outputs On A Port

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test Circuit For Outputs On B Port



$V_M = 1.5V$

Input Pulse Definition

FAMILY 74F	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_U = Pull up resistor; see AC CHARACTERISTICS for value.

Signetics

FAST 74F30240,74F30244
30Ω Line Drivers

FAST Products

'F30240 Octal 30Ω Line Driver With Enable, Inverting (Open Collector)
'F30244 Octal 30Ω Line Driver With Enable, Non-Inverting (Open Collector)
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F30240	9.5ns	62.5mA
74F30244	10.5ns	69mA

FEATURES

- Ideal for driving transmission lines or backplanes. 160mA I_{OL} ideal for applications with impedance as low as 30Ω
- Guaranteed threshold voltages on the incident wave while driving line as low as 30Ω.
- High impedance NPN base inputs for reduced loading (20μA in High and Low states)
- Ideal for applications which require high output drive and minimal bus loading
- Octal interface
- 'F30240 Inverting
- 'F30244 Non-Inverting
- Open-Collector outputs sink 160mA
- Multiple side pins are used for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)
- Available in 24-pin standard slim DIP (300mil) plastic or CERDIP packages

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Cerdip (300 mil)	N74F30240F, N74F30244F
24-Pin Plastic Slim DIP(300 mil)[1]	N74F30240N, N74F30244N

NOTE:
1.Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

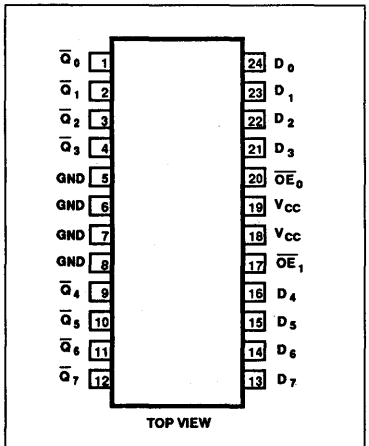
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0- D_7	Data inputs	1.0/0.033	20μA/20μA
$\overline{OE}_0$- $\overline{OE}_1$	Output Enable inputs (active Low)	1.0/0.033	20μA/20μA
$\overline{Q}_0$- $\overline{Q}_7$	Data outputs (OC) for 'F30240	OC/266.7	OC/160mA
Q_0- Q_7	Data outputs (OC) for 'F30244	OC/266.7	OC/160mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC = Open Collector

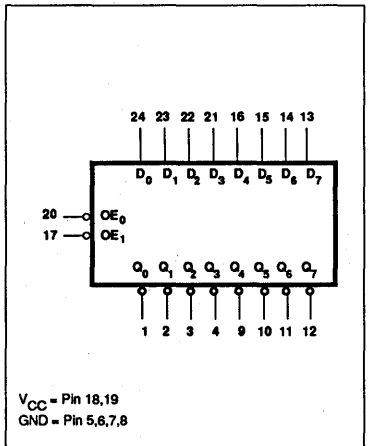
DESCRIPTION

The 74F30240/F30244 are high current open collectors octal buffers composed of eight inverters. The 'F30240 has inverting data paths and the 'F30244 has non-inverting paths. Each device has eight inverters with two Output Enables($\overline{OE}_0$, $\overline{OE}_1$) each controlling four outputs. Both drivers are designed to deal with the low-impedance transmission line effects found on printed circuit boards when fast edge rates are used. The 160 mA I_{OL} provides ample power to achieve TTL switching voltages on the incident wave.

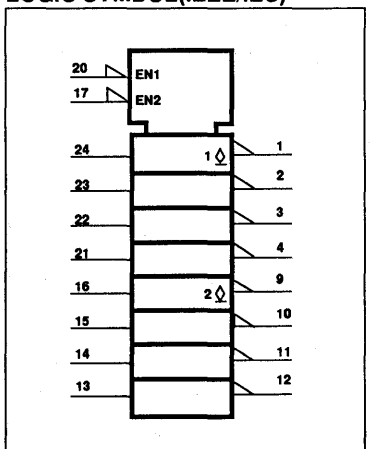
PIN CONFIGURATION



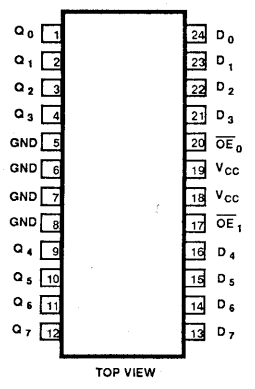
LOGIC SYMBOL



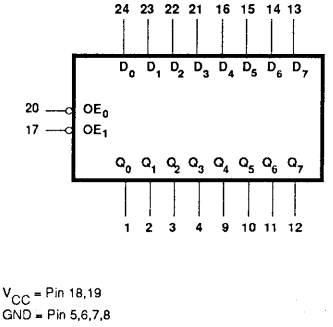
LOGIC SYMBOL(IEEE/IEC)



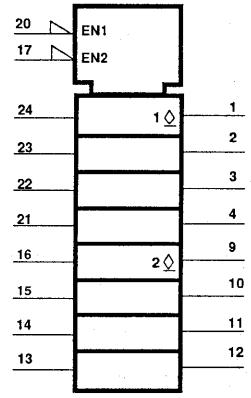
PIN CONFIGURATION



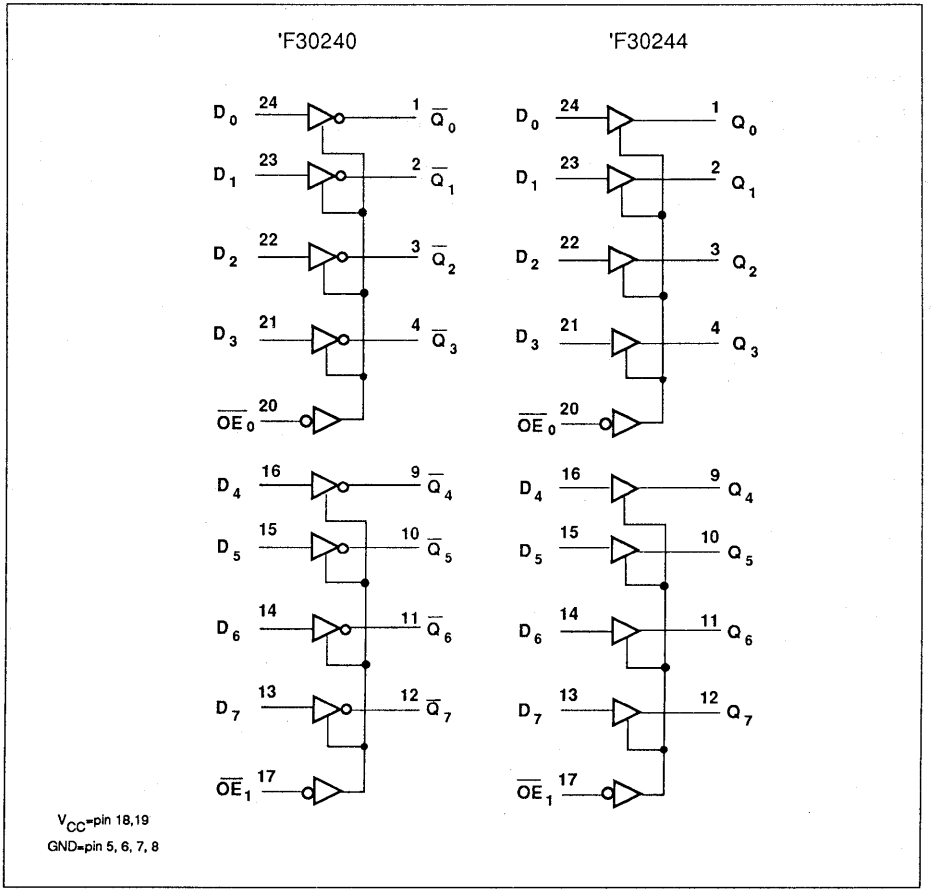
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS	
		'F30240	'F30244
$\overline{OE}_n$	D_n	$\overline{Q}_n$	Q_n
L	L	H	L
L	H	L	H
H	X	OFF	OFF

H=High voltage level
L=Low voltage level
X=Don't care
OFF=Pulled up through resistor (open collector)

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	320	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			160	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

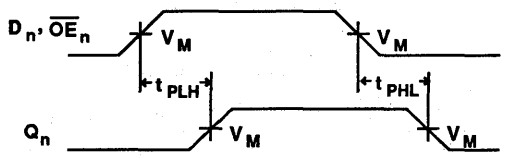
SYMBOL	PARAMETER			TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
I_{OH}	High-level output current			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH}=MAX					250	µA
V_{OL}	Low-level output current			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		.42	.55	V
					I_{OL} = 160mA[3]	±5%V_{CC}			.80	V
V_{IK}	Input clamp voltage			V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage			V_{CC} =0.0V, V_I = 7.0V					100	µA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{CC}	Supply current [total]	'F30240	I_{CCH}	V_{CC} = MAX				13	23	mA
			I_{CCL}					70	95	mA
		'F30244	I_{CCH}					19	27	mA
			I_{CCL}					70	100	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30Ω transmission line on the incident wave.

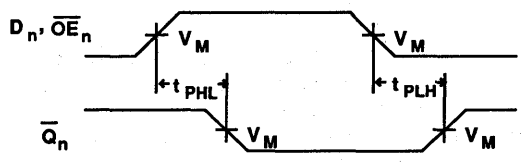
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω Min	Typ	Max	LIMITS T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω Min	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	'F30240	Waveform 2	4.0 1.0	10.0 2.0	14.5 5.0	4.0 1.0	15.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_n$ to $\overline{Q}_n$	'F30240	Waveform 1,2	4.0 3.5	10.0 6.0	14.0 9.0	4.0 3.5	14.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{Q}_n$	'F30244	Waveform 1	4.0 3.0	10.5 5.5	14.5 9.0	4.0 3.0	15.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}_n$ to $\overline{Q}_n$	'F30244	Waveform 1,2	4.0 3.5	9.5 6.0	14.0 9.0	4.0 3.5	14.5 10.5	ns

AC WAVEFORMS



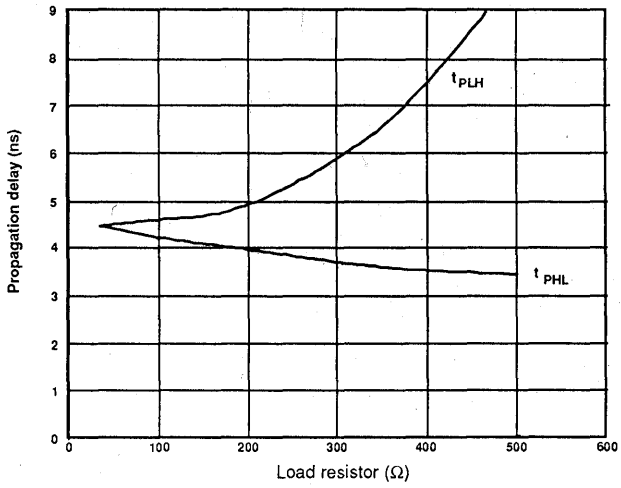
Waveform 1. Propagation Delay For Data To Output



Waveform 2. Propagation Delay For Data To Output

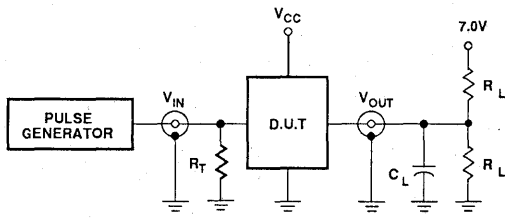
NOTE: For all waveforms, V_M = 1.5V.

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

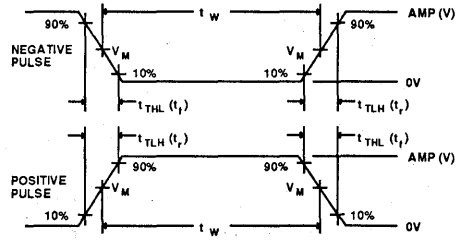


NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Open Collector Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F30245,74F30640 Transceivers

'F30245 Octal 30Ω Transceiver Non-Inverting
(Open Collector With Enable + 3-State)
'F30640 Octal 30Ω Transceiver Inverting
(Open Collector With Enable + 3-State)
Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F30245	5.5ns	90mA
74F30640	5.0ns	85mA

FAST Products

FEATURES

- High impedance NPN base inputs for reduced loading
- Ideal for applications which require high output drive and minimal bus loading
- Octal bidirectional bus interface
- 'F30245 Non-Inverting
- 'F30640 Inverting
- Choice of outputs:
  Open collectors (B_0-B_7) and 3-states(A_0-A_7)
- Open-Collector outputs sink 160mA
- 160mA I_{OL} ideal for low-impedance applications and transmission line effects with impedance as low as 30Ω
- 3-state buffer outputs sink 24mA
- Multiple side pins are used for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)
- Available in 24-pin standard slim DIP (300mil) plastic or CERDIP packages
- Flow through pinout structure facilitates PC board layout

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Cerdip (300 mil)	N74F30245F, N74F30640F
24-Pin Plastic Slim DIP[1]	N74F30245N, N74F30640N

NOTE:
1.Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

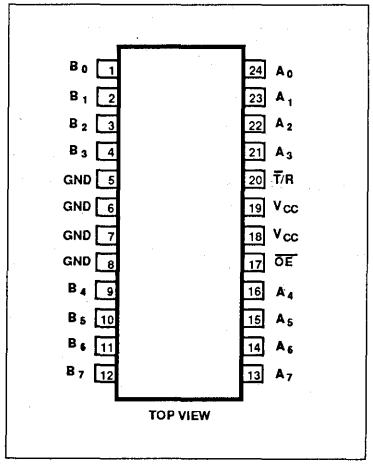
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0- A_7	Data inputs	3.5/0.1167	70μA/70μA
B_0- B_7	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active Low)	2.0/0.0667	40μA/40μA
$\overline{T}$/R	Transmit/Receive input	2.0/0.0667	40μA/40μA
A_0- A_7	Data outputs (3-state)	150/40	3.0mA/24mA
B_0- B_7	Data outputs (OC)	OC/266.7	OC/160mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC = Open Collector

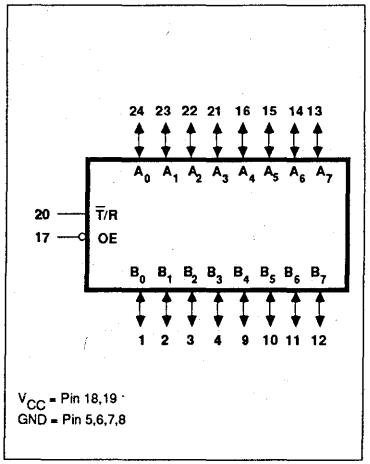
DESCRIPTION

The 74F30245/F30640 are high current octal transceivers. The 'F30245 has non-inverting data paths and the 'F30640 has inverting paths. The B outputs are open collector with 160mA I_{OL} while the A outputs are 3-state with 24mA I_{OL}.Both transceivers are designed to deal with the low-impedance transmission line effects found on printed circuit boards when fast edge rates are used. The 160 mA I_{OL} provides ample power to achieve TTL switching voltages on the incident wave.

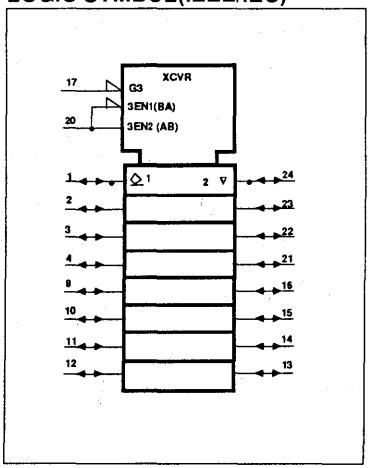
PIN CONFIGURATION



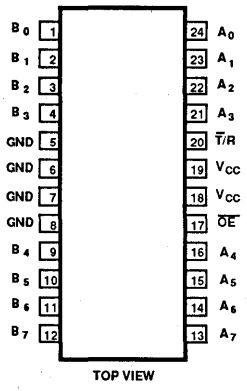
LOGIC SYMBOL



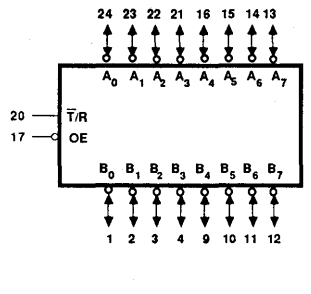
LOGIC SYMBOL(IEEE/IEC)



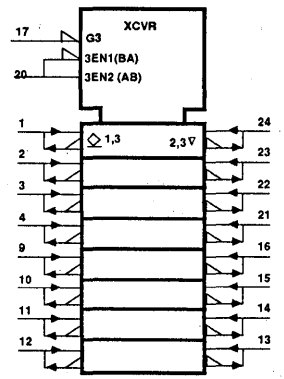
PIN CONFIGURATION



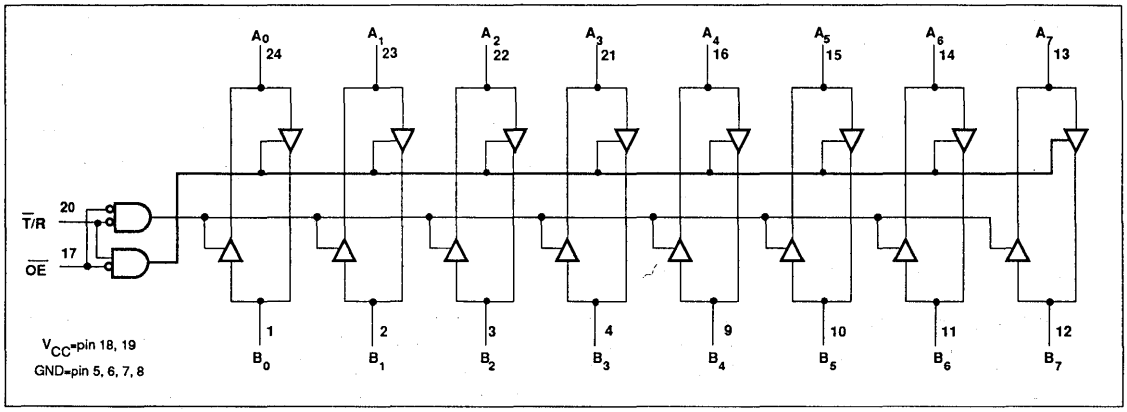
LOGIC SYMBOL



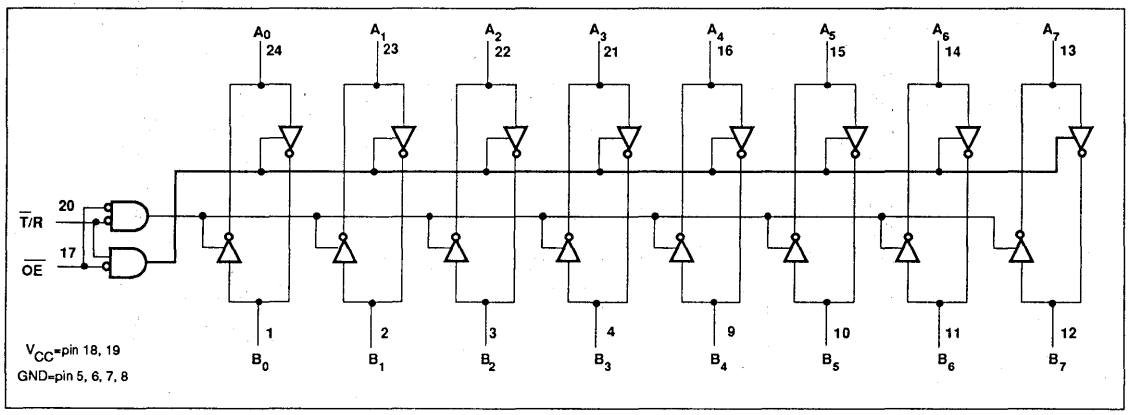
LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM 'F30245



LOGIC DIAGRAM 'F30640



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS			
		'F30245		'F30640	
$\overline{OE}$	$\overline{T}/R$	A_n	B_n	A_n	B_n
L	H	A=B	Inputs	A=$\overline{B}$	Inputs
L	L	Inputs	B=A	Inputs	B=$\overline{A}$
H	X	Z	Z	Z	Z

H=High voltage level
L=Low voltage level
X=Don't care
Z=High impedance "off " state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7	320	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
V_{OH}	High-level output voltage	B_0-B_7			4.5	V
I_{OH}	High-level output current	A_0-A_7			-3	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7			160	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
I_{OH}	High-level output current	B_0-B_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX					250	µA
V_{OH}	High-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN,	I_{OL}=24mA	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7		I_{OL}=100mA	±10%V_{CC}		0.42	0.55	V
				I_{OL1}=160mA[4]	±5%V_{CC}			0.80	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	$\overline{T}$/R, $\overline{OE}$	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = 5.5V, V_I = 5.5V					1.0	mA
I_{IH}	High-level input current	$\overline{T}$/R, $\overline{OE}$	V_{CC} = MAX, V_I = 2.7V					40	µA
		B_0-B_7						20	µA
I_{IL}	Low-level input current	$\overline{T}$/R, $\overline{OE}$	V_{CC} = MAX, V_I = 0.5V					-40	µA
		B_0-B_7						-600	µA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied	A_0-A_7	V_{CC} = MAX, V_O= 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied	A_0-A_7	V_{CC} = MAX, V_O= 0.5V					-70	µA
I_{OS}	Short-circuit output current[3]	A_0-A_7	V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	'F30245	V_{CC} = MAX			50	80	mA
		I_{CCL}					100	145	mA
		I_{CCZ}					60	85	mA
		I_{CCH}	'F30640	V_{CC} = MAX			40	60	mA
		I_{CCL}					75	130	mA
		I_{CCZ}					45	65	mA

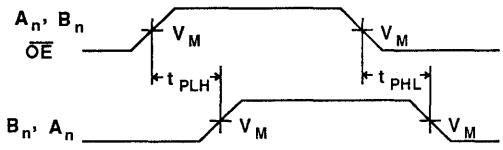
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30 ohm transmission line on the incident wave.

AC ELECTRICAL CHARACTERISTICS

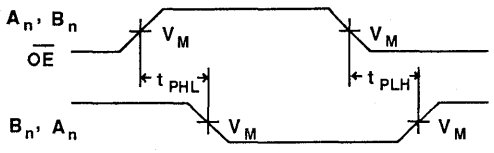
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH}* t_{PHL}	Propagation delay A_n to B_n	'F30245	Waveform 1,2	7.5 3.0	10.0 4.5	13.0 7.5	7.0 2.5	13.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n		Waveform 1,2	2.0 2.0	3.5 3.5	6.5 6.0	1.5 1.5	7.0 6.5	ns
t_{PLH}* t_{PHL}	Propagation delay A_n to B_n	'F30640	Waveform 1,2	7.5 1.0	10.0 2.0	13.0 5.0	7.5 1.0	13.5 5.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n		Waveform 1,2	1.0 1.0	2.5 2.0	5.5 5.0	1.0 1.0	6.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to B_n	B_n ouputs	Waveform 1,2	7.5 3.5	9.5 5.5	13.0 8.5	7.5 3.0	13.5 9.0	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	A_n ouputs	Waveform 3 Waveform 4	2.5 1.5	4.5 4.0	7.5 8.0	2.0 1.5	8.0 8.5	ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	A_n ouputs	Waveform 3 Waveform 4	1.5 1.0	3.5 3.5	6.5 6.5	1.0 1.0	7.5 7.0	ns

* = See Figure A for Open Collector Output information

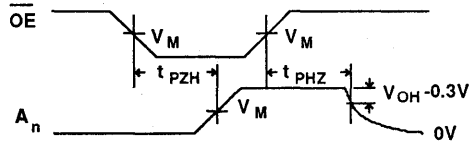
AC WAVEFORMS



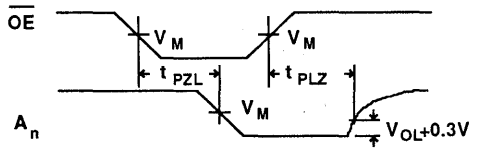
Waveform 1. Propagation Delay For Non-Inverting Output



Waveform 2. Propagation Delay For Inverting Output



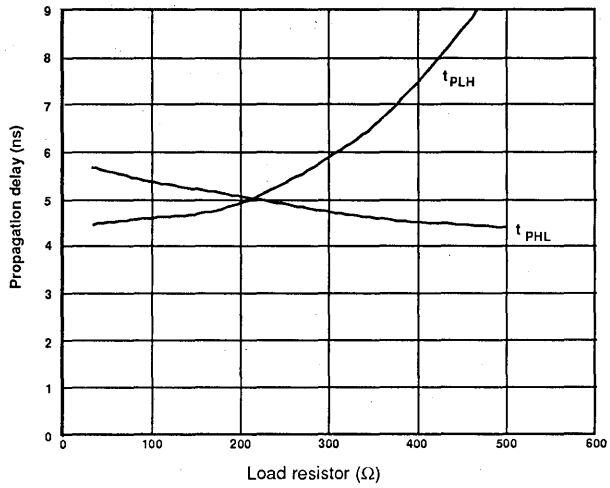
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

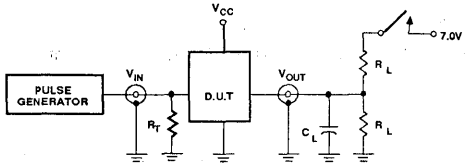
TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



NOTE:
When using Open-Collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only a slight increase in the t_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers does not exceed the I_{OL} maximum specification.

Figure A

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs and Open Collector (OC) outputs

SWITCH POSITION

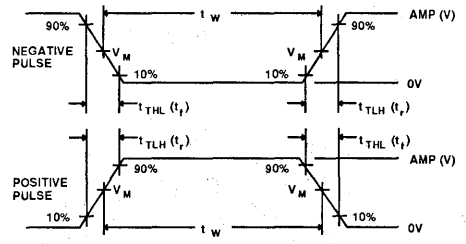
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
OC	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F50109
FLIP-FLOP

FAST Products

Synchronizing Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flops With Metastable Immune Characteristics

Preliminary Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F50109	200 MHz	18mA

FEATURES

- **Metastable Immune Characteristics**
- **Propagation delay skew and output to output skew less than 1.5ns**
- **Same pinout and function as 74F109**
- **See 74F5074 for Synchronizing Dual D-Type Flip-Flop**
- **See 74F50728 for Synchronizing Cascaded D-Type Flip-Flop**
- **See 74F50729 for Synchronizing Cascaded Dual D-Type Flip-Flop with Edge-Triggered Set and Reset**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F50109N
16-Pin Plastic SO	N74F50109D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_0, J_1	J inputs	1.0/0.166	20µA/100µA
$\overline{K}_0$, $\overline{K}_1$	K inputs	1.0/0.166	20µA/100µA
CP_0, CP_1	Clock inputs (active rising edge)	1.0/0.083	20µA/50µA
$\overline{S}_{D0}$, $\overline{S}_{D1}$	Set inputs (active Low)	1.0/0.083	20µA/50µA
$\overline{R}_{D0}$, $\overline{R}_{D1}$	Reset inputs (active Low)	1.0/0.083	20µA/50µA
Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

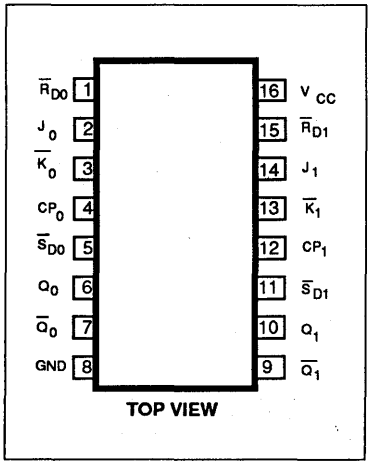
NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 74F50109 is a dual positive edge-triggered JK-type flip-flop featuring individual J, $\overline{K}$, Clock, Set and Reset inputs; also true and complementary outputs.
Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-Low inputs and operate independently of the Clock (CP) inputs.
The J and $\overline{K}$ are edge-triggered inputs which control the state changes of the flip-flops as described in the Function Table. The J and $\overline{K}$ inputs must be stable just one setup time prior to the Low-to-High transition of the clock for guaranteed propagation delays. The J$\overline{K}$ design allows operation as a D flip-flop by tying J and $\overline{K}$ inputs together.

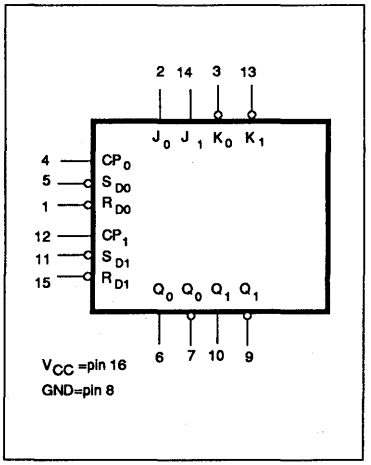
The 74F50109 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup and hold times are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F50109 are: τ < .200ns, T_o=10µs, and h=3.8ns.

PIN CONFIGURATION

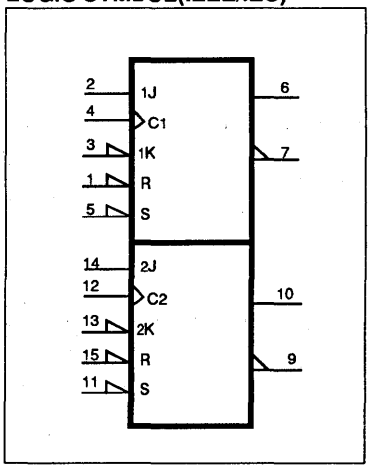


TOP VIEW

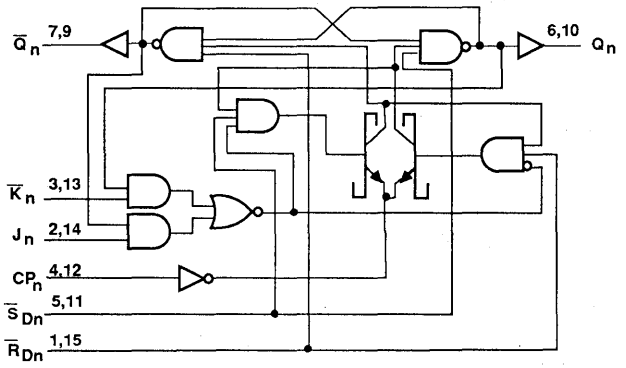
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



V_{CC} =pin 16
GND =pin 8

FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
$\overline{S}_{Dn}$	$\overline{R}_{Dn}$	CP_n	J_n	$\overline{K}_n$	Q_n	$\overline{Q}_n$	
L	H	X	X	X	H	L	Asynchronous Set
H	L	X	X	X	L	H	Asynchronous Reset
L	L	X	X	X	H	H	Undetermined (Note)
H	H	↑	h	l	$\overline{q}$	q	Toggle
H	H	↑	l	l	L	H	Load "0"(Reset)
H	H	↑	h	h	H	L	Load "1" (Set)
H	H	↑	l	h	q	$\overline{q}$	Hold "no change"

H = High voltage level
h = High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
q = Lower case indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
Note = Both outputs will be High if both $\overline{S}_{Dn}$ and $\overline{R}_{Dn}$ go Low simultaneously.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the devicUnles otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} =MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} =MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	J_n, $\overline{K}_n$, CP_n	V_{CC} =MAX, V_I = 7.0V					0.1	mA
		$\overline{S}_{Dn}$, $\overline{R}_{Dn}$						0.2	mA
I_{IH}	High-level input current		V_{CC} =MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	J_n, $\overline{K}_n$	V_{CC} =MAX, V_I = 0.5V					-100	µA
		CP_n, $\overline{S}_{Dn}$, $\overline{R}_{Dn}$						-50	µA
I_{OS}	Short circuit output current[3]		V_{CC} =MAX			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} =MAX				18	24	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs High in turn.

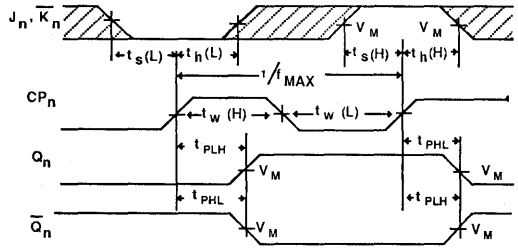
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1		200		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	3.8 3.8	4.5 5.0	2.0 2.0	5.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_{Dn}$ to Q_n or $\overline{Q}_n$	Waveform 2	2.0 2.0	3.8 3.8	4.5 5.0	2.0 2.0	5.5 6.0	ns

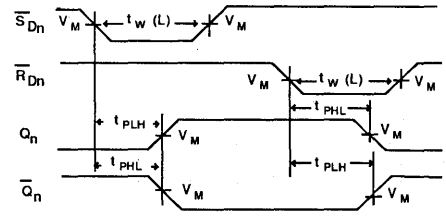
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J_n, $\overline{K}_n$ to CP_n	Waveform 1	1.0 1.0			1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J_n, $\overline{K}_n$ to CP_n	Waveform 1	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP_n Pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	$\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ Pulse width, Low	Waveform 2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to CP_n	Waveform 3	2.0			2.0		ns

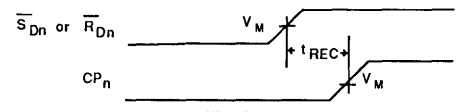
AC WAVEFORMS



Waveform 1.
Propagation Delay for Data to Output, Data Setup Time and Hold Times, Clock Width, and Maximum Clock Frequency



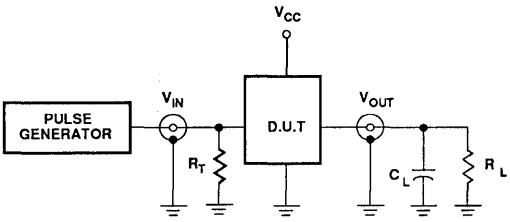
Waveform 2.
Propagation Delay for Set and Reset to Output, Set and Reset Pulse Width



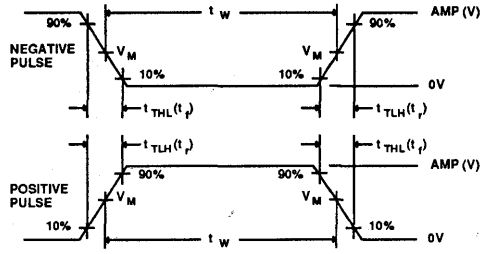
Waveform 3.
Recovery Tme for Set or Reset to Clock

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST Products

74F50728
FLIP-FLOP

Synchronizing Cascaded Dual D-Type Flip-Flop With Metastable Immune Characteristics

Preliminary Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F50728	200 MHz	20mA

FEATURES

- **Metastable Immune Characteristics**
- **Propagation delay skew and output to output skew less than 1.5ns**
- **See 74F5074 for Synchronizing Dual D-Type Flip-Flop**
- **See 74F50109 for Synchronizing Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop**
- **See 74F50729 for Synchronizing Cascaded Dual D-Type Flip-Flop with Edge-Triggered Set and Reset**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F50728N
14-Pin Plastic SO	N74F50728D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0, D_1	Data inputs	1.0/0.166	20µA/100µA
CP_0, CP_1	Clock inputs (active rising edge)	1.0/0.083	20µA/50µA
$\overline{S}_{D0}$, $\overline{S}_{D1}$	Set inputs (active Low)	1.0/0.083	20µA/50µA
$\overline{R}_{D0}$, $\overline{R}_{D1}$	Reset inputs (active Low)	1.0/0.083	20µA/50µA
Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

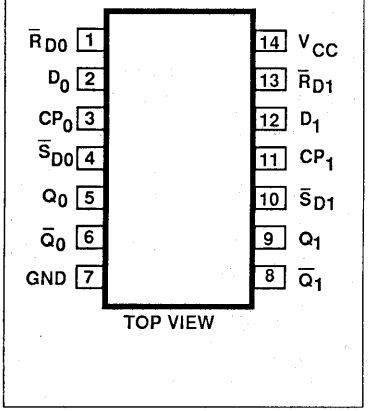
DESCRIPTION

The 74F50728 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also true and complementary outputs.

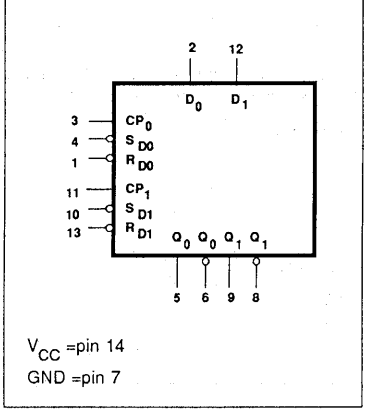
Set ($\overline{S}_n$) and Reset ($\overline{R}_n$) are asynchronous active-Low inputs and operate independently of the Clock (CP) input. They set and reset both flip-flops of a cascaded pair simultaneously. Data must be stable just one setup time prior to the Low-to-High transition of the clock for guaranteed propagation delays.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D input may be changed without affecting the levels of the output. Data entering the 'F50728 requires two clock cycles to arrive at the outputs. The 'F50728 is designed so that the outputs can never display a metastable state due to setup and hold times violations. If setup and hold times are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F50728 are: τ < .200ns, T_o=10µs, and h=3.8ns.

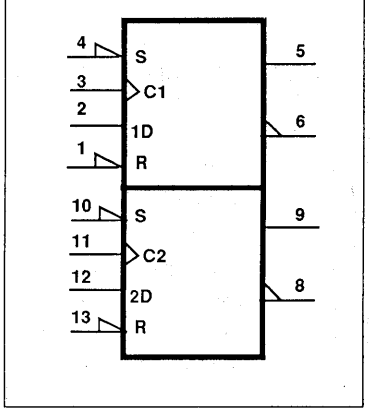
PIN CONFIGURATION



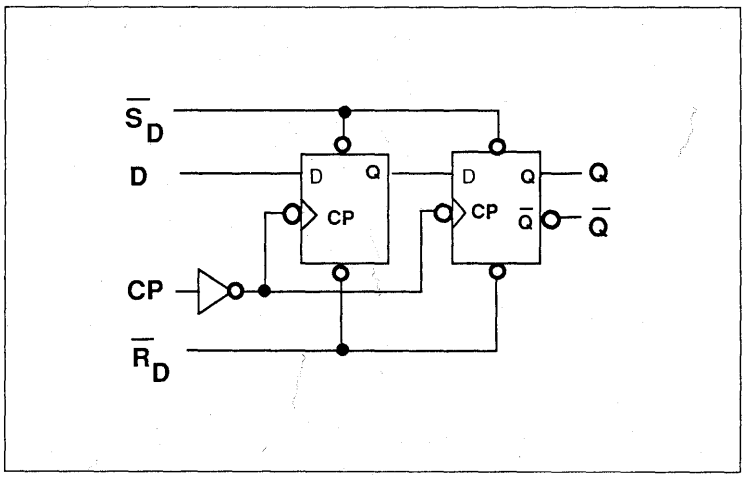
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				INTERNAL REGISTER	OUTPUTS		OPERATING MODE
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	Q	$\overline{Q}$	
L	H	X	X	H	H	L	Asynchronous Set
H	L	X	X	L	L	H	Asynchronous Reset
L	L	X	X	X	H	H	Undetermined*
H	H	↑	h	h	H	L	Load "1"
H	H	↑	l	l	L	H	Load "0"
H	H	L	X	NC	NC	NC	Hold

H = High voltage level
h = High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
X = Don't care

↑ = Low-to-High clock transition
NC =No change from the previous setup
* = This setup is unstable and will change when either Set or Reset return to the High level.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} =MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} =MAX	±10%V_{CC}		0.30	0.50	V
			±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current $\frac{D_n}{CP_n, \overline{S}_{Dn}, \overline{R}_{Dn}}$	V_{CC} = MAX, V_I = 0.5V				-100	µA
						-50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			20	26	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs High in turn.

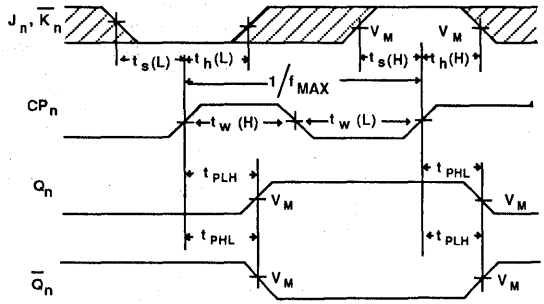
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1		200		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	3.8 3.8	4.5 5.0	2.0 2.0	5.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_{Dn}$ to Q_n or $\overline{Q}_n$	Waveform 2	2.0 2.0	3.8 3.8	4.5 5.0	2.0 2.0	5.5 6.0	ns

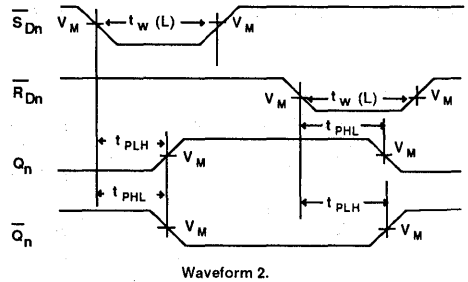
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 1	1.0 1.0			1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 1	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(L)$	$\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ Pulse width, Low	Waveform 2	4.0			4.0		ns
t_{rec}	Recovery time $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to CP	Waveform 3	2.0			2.0		ns

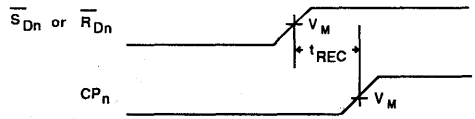
AC WAVEFORMS



Waveform 1. Propagation Delay For data to output, data setup time and hold times, and clock width



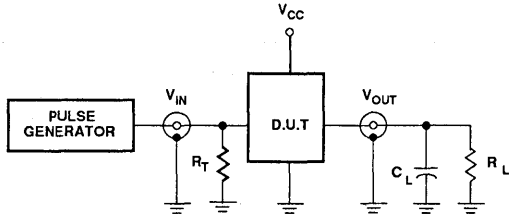
Waveform 2.
Propagation Delay for set and reset to output, set and reset pulse width



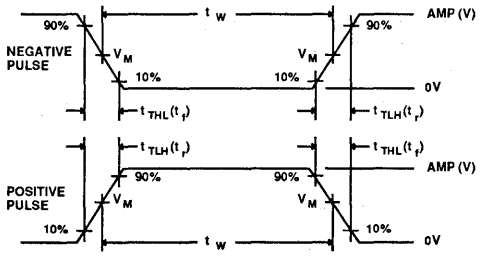
Waveform 3.
Recovery time for set or reset to clock

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST Products

FAST 74F50729 FLIP-FLOP

Synchronizing Dual D-Type Flip-Flop With Edge triggered Set and Reset And Metastable Immune Characteristics

Preliminary Specification

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F50729	200 MHz	18mA

FEATURES

- **Metastable Immune Characteristics**
- **Propagation delay skew and output to output skew less than 1.5ns**
- **See 74F5074 for Synchronizing Dual D-Type Flip-Flop**
- **See 74F50109 for Synchronizing Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop**
- **See 74F50728 for Synchronizing Cascaded Dual D-Type Flip-Flop**

DESCRIPTION

The 74F50729 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also true and complementary outputs.

Set ($\overline{S}_n$) and Reset ($\overline{R}_n$) are asynchronous positive-edge triggered inputs and operate independently of the Clock (CP) input. Data must be stable just one setup time prior to the Low-to-High transition of the clock for guaranteed propagation delays.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D input may be changed without affecting the levels of the output.

The 74F50729 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup and hold times are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F50729 are: τ<.200ns, T_o=10µs, and h=3.8ns.

ORDERING INFORMATION

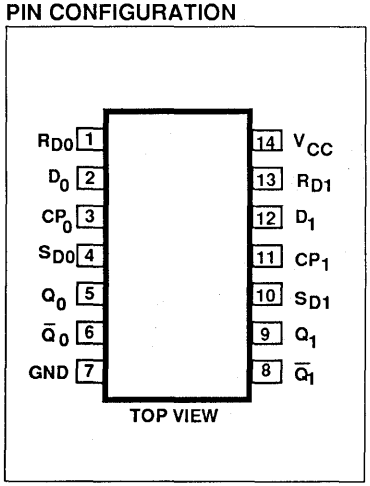
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
14-Pin Plastic DIP	N74F50729N
14-Pin Plastic SO	N74F50729D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

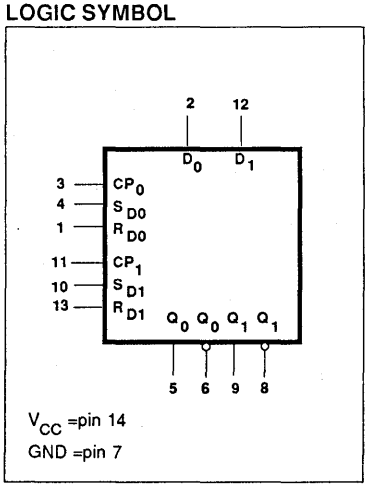
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0, D_1	Data inputs	1.0/0.166	20µA/100µA
CP_0, CP_1	Clock inputs (active rising edge)	1.0/0.083	20µA/50µA
S_{D0}, S_{D1}	Set inputs (active rising edge)	1.0/0.083	20µA/50µA
R_{D0}, R_{D1}	Reset inputs (active rising edge)	1.0/0.083	20µA/50µA
Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$	Data outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

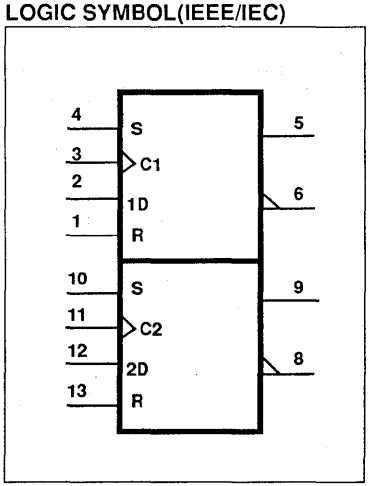
PIN CONFIGURATION



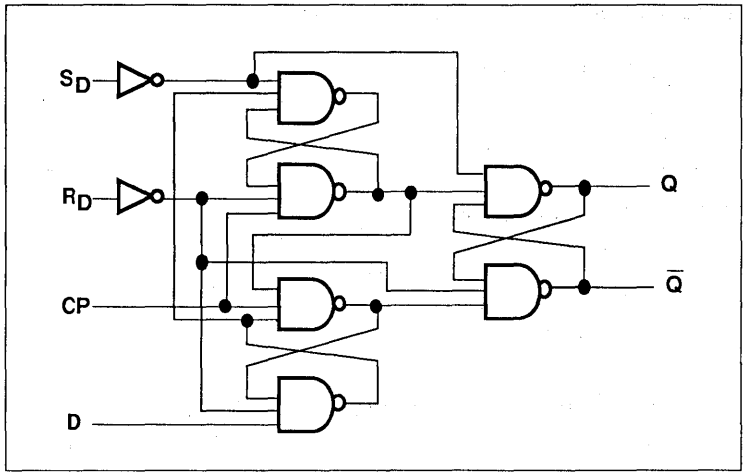
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
S_D	R_D	CP	D	Q	$\overline{Q}$	
↑	↥	X	X	H	L	Asynchronous Set
↥	↑	X	X	L	H	Asynchronous Reset
↥	↥	↑	h	H	L	Load "1"
↥	↥	↑	l	L	H	Load "0"
↥	↥	↥	X	NC	NC	Hold

H = High voltage level
h = High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
X = Don't care
↑ = Low-to-High transition
NC =No change from the previous setup
↥ = Not Low-to-High transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} =MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = MAX ±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} =MAX ±10%V_{CC}		0.30	0.50	V
				±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	D_n	V_{CC} = MAX, V_I = 0.5V				-100	µA
		CP_n, S_{Dn}, R_{Dn}					-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX			18	24	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs High in turn.

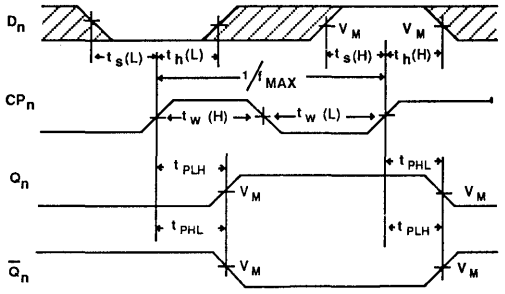
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1		200				MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	3.8 3.8	4.5 5.0	2.0 2.0	5.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay S_{Dn} to R_{Dn} to Q_n or $\overline{Q}_n$	Waveform 2	2.0 2.0	3.8 3.8	4.5 5.0	2.0 2.0	5.5 6.0	ns

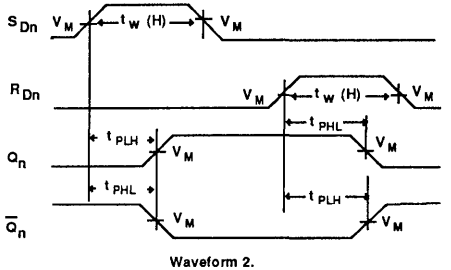
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 1	1.0 1.0			1.0 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 1	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns
$t_w(H)$	S_{Dn} or R_{Dn} Pulse width, High	Waveform 2	4.0			4.0		ns
t_{REC}	Recovery time S_{Dn} or R_{Dn} to CP	Waveform 3	2.0			2.0		ns
t_{REC}	Recovery time S_{Dn} to R_{Dn} or R_{Dn} to S_{Dn}	Waveform 3	2.0			2.0		ns

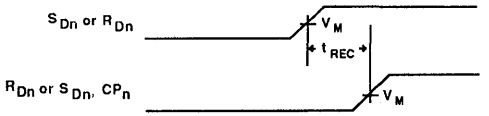
AC WAVEFORMS



Waveform 1. Propagation Delay For data to output, data setup time and hold times, and clock width



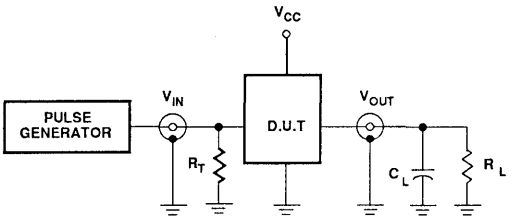
Waveform 2.
Propagation Delay for set and reset to output, set and reset pulse width



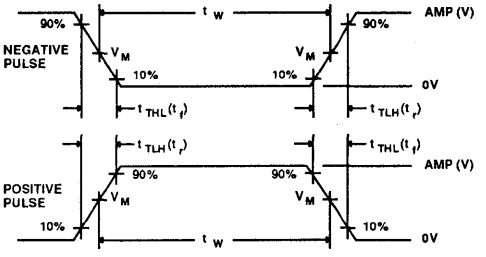
Waveform 3.
Recovery time for set or reset to clock and set to reset or reset to set

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Signetics

FAST Application Notes

Signetics

Section 7
FAST Application Notes

FAST Products

INDEX

Signetics

AN202
Testing And Specifying FAST Logic

Application Note

FAST Products

INTRODUCTION

FAST™ is a second generation Schottky logic family that utilizes advanced oxide-isolation techniques to increase the speed and decrease the power dissipation beyond the levels achievable with conventional junction-isolated families. The improved performance of the family is exhibited in two ways — first, the speed and power characteristics of the devices are improved, and second, the conditions under which speed and power are specified are much tighter. For instance, LS and S TTL families offer AC limits only at a nominal +5.00V V_{CC} supply voltage and at room temperature, 25°C. By contrast, FAST guarantees improved AC performance and specifies that performance over a supply variation of +5.00V ±10% and at temperatures from 0°C to 70°C. Thus the designer no longer needs to derate his propagation delays from the data sheet limits to compensate for speed degradation over the temperature range.

With every advance of this magnitude, there arise new considerations that must be kept in mind both by the system designer and the user setting up test procedures. FAST is no exception, and it is these considerations that will be addressed in this application note. This paper represents an attempt to describe the way the FAST logic parts are specified, why they are spec'd in the way they are, and how the parts may be tested in the qualification lab and at incoming inspection to verify their performance.

THE FAST DATA SHEET PHILOSOPHY

Signetics FAST data sheets have been configured with an eye to quick useability . . . they are self contained and should require no reference to other sections for information. The typical propagation delays listed at the top of the page are the average between t_{PLH} and t_{PHL} for the most significant data path through the part. In the case of clocked products, this is sometimes the max frequency of operation, but in any event this number is a 5.00V – 25°C typical specification. The I_{CC} typical current shown in that same specification block is the average current (in the case of a gate, this will be the average of the I_{CCH} and I_{CCL} currents) at room temperature and V_{CC} = 5.00V. It represents the total current through the package, not the *current through individual functions.*

Other considerations are the Fanout And Loading tables. Some manufacturers relate these numbers in terms of 7400 gate loads . . . Signetics feels that FAST is unlikely to be mixed with other logic families and so gives the loading factors in terms of FAST unit loads. A FAST unit load is defined to be 0.6mA in the Low state and 20μA in the High state. Thus in the case of the 74F00 gate, the inputs are specified as 1 Ful (FAST unit load) each . . . the outputs need a little explanation. The standard FAST output is specified with an I_{OL} sink current of 20mA and an I_{OH} of +1.0mA. Thus the fanout of this gate in the Low state is 20mA/0.6mA or 33 FAST unit loads. In the High state the fanout is 1mA/20μA or 50 FAST unit loads. In each case, the Fanout and Loading Table on the Signetics data sheets states the High/Low fanout numbers . . . thus the 74F00 output fanout is specified as 50/33 Ful.

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings table carries the maximum limits to which the part can be subjected without damaging it . . . there is no implication that the part will function at these extreme conditions. Thus, specifications such as the most negative voltage that may be applied to the outputs only guarantees that if less than –0.5V is applied to the output pin, after that voltage is removed the part will still be functional and its useful life will not have been shortened — it is difficult to imagine the meaning of the term "functionality" WHILE that voltage is applied to the output.

Input voltage and output voltage specification in this table reflect the device breakdown voltages in the positive direction (+7.0V) and the effect of the clamping diodes in the negative direction (–0.5V).

RECOMMENDED OPERATING CONDITIONS

The Recommended Operating Conditions table has a dual- purpose. In one sense, it sets some environmental conditions (operating free-air temperature), and in another, it sets the conditions under which the limits set forth in the DC Electrical Characteristics table and AC Electrical Characteristics table will be met. Another way of looking at this table is to think of it, not as a set of limits guaranteed by Signetics, but as the conditions Signetics uses to test the parts and guarantee that they will then meet the limits set forth in the DC and AC Electrical Characteristics tables.

Some care must be used in interpreting the numbers in this table. Signetics feels strongly that the specifications set forth in a data sheet should reflect as accurately as possible the operation of the part in an actual system. In particular, the input threshold values of V_{IH} and V_{IL} can be tested by the user with parametric test equipment . . . if V_{IH} and V_{IL} are applied to the inputs, the outputs will be at the voltages guaranteed by the DC Electrical Characteristics table providing that there is adequate grounding and the input voltages are free from noise, otherwise a guardbanded V_{IH} and V_{IL} should be used, ie., 2.5V instead of 2.0V and .5V instead of .8V. There is a tendency on the part of some users to use V_{IH} and V_{IL} as conditions applied to the inputs to test the part for functionality in a "truth-table exerciser" mode. This frequently causes problems because of the noise present at the test head of automated test equipment. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, on the order of milliseconds, and any noise present at the inputs has settled out before the outputs are measured. (This is not the case with clocked or enabled parts and poor or moderate fixturing may induce oscillations or severe ground bounce if noise is present.) But in functionality testing, the outputs are examined much faster, before the noise on the inputs are settled out and the part has assumed its final and correct output state. Since these are unloaded outputs, having faster edge rates, this causes more noise. If the outputs are loaded, the 50pF per output pin can cause substantial ground bounce. Thus V_{IH} and V_{IL} should never be used in testing the functionality of any TTL part including FAST. For these types of tests input voltages of +4.5V and 0.0V should be used for the High and Low states respectively.

In no way does this imply that the devices are noise sensitive in the final system. The use of "hard" Highs and Lows during functional testing is done primarily to (1) reduce the effects of the large amounts of noise typically present at the test heads of automated test

7

™FAST is a trademark of Fairchild Camera and Instrument Corporation.

Testing And Specifying FAST Logic AN202

equipment with cables that may at times reach several feet and (2) deal with testing parts exhibiting fast edge rates and 50pF per output pin. The situation in a system on a PC board is less severe than in a noisy production environment.

DC ELECTRICAL CHARACTERISTICS

This table reflects the DC limits used by Signetics during its testing operations and conducted under the conditions set forth under the Recommended Operating Conditions table. V_{OH}, for example, is guaranteed to be no less than 2.7V when tested with $V_{CC} = +4.75V$, $V_{IH} = 2.0V$, $V_{IL} = 0.8V$, across the temperature range from 0° to 70°C, and with an output current of $I_{OH} = -1.0mA$. In this table, one sees the heritage of the original junction isolated Schottky family . . . $V_{OL} = 0.5V$ at $I_{OL} = 20mA$. This gives the user a guaranteed worst-case Low state noise immunity of 0.3V. In the High state the noise immunity is 0.7V worst case. Although at first glance it would seem one-sided to have greater noise immunity in the High state than in the Low, this is a useful state of affairs. Because the impedance of an output in the High state is generally much higher than in the Low state, more noise immunity in the High state is needed. This is because the noise source couples noise onto the output connection of the device — that output tries to pull the noise source down by sinking the energy to ground or to V_{CC} depending on the state. The ability of the output to do that is determined by its output impedance. The lower half of the output stage is a very low-impedance transistor which can effectively pull the noise source down. Because of the higher impedance of the upper stage of the output, it is not as effective in shunting the noise energy to V_{CC}, so that an extra 0.4V of noise immunity in the High state compensates for the higher impedance. The result is a nice balance of sink and drive current capabilities with the optimum amount of noise immunity in both states.

I_I, the maximum input current at maximum input voltage, is a measure of the input leakage current at the guaranteed minimum input breakdown voltage of 7.0V. Although some users consider this to be a test of the input breakdown itself, that voltage is typically over 15V. At room temperature, this leakage current should be less than 10μA. (This is not the case with NPN input designed parts.)

Short-Circuit Output Current is a parameter that has appeared on digital data sheets since the inception of integrated circuit logic devices, but the meaning and implications of that *specification* have totally changed. Originally I_{OS} was an attempt to reassure the user that if a stray oscilloscope probe accidentally shorted an output to ground the device would not be damaged. In this manner, an extremely long time was associated with the I_{OS} test. However, thermally induced malfunctions could occur after several seconds of sustained test. Over a period of time, I_{OS} became a measure of the ability of an output to charge line capacitance. Assume a device is driving a long line and is in the Low state. When the output is switched High, the rise time of the output waveform is limited by the rate at which the line capacitance can be charged to its new state of V_{OH}. At the instant that the output switches, the line capacitance looks like a short to ground. I_{OS} is the current demanded by the capacitive load as the voltage begins to rise and the demand decreases. The full value of I_{OS} need only be supplied for a few hundred microseconds at most, even with 1.0μFd of line capacitance tied to the output, a load that is unrealistically high by several orders of magnitude.

The effective of a large I_{OS} surge through the relatively small transistors that make up the upper part of the output stage is not serious, AS LONG AS THAT CURRENT IS LIMITED TO A SHORT DURATION. If the hard short is allowed to remain, the full I_{OS} current will flow through that output state and may cause functional failure or damage to the structure. A test induced failure may occur if the I_{OS} test time is excessive. As long as the I_{OS} condition is very brief, typically 50ms or less with ATE equipment, the local heating does not reach the point where damage or functional failures might occur. As we have already seen, this is considerably longer than the time of the effective current surge that must be supplied by the device in the case of charging line capacitance. The Signetics data sheet limits for I_{OS} reflect the conditions that the part will see in the system — full I_{OS} spikes for extremely short periods of time. Problems could occur if slow test equipment or test methods ground an output for too long a time causing functional failure or damage.

AC TESTING

FAST data sheets carry several types of AC information. The AC Characteristics table contains the guaranteed limits when tested under the conditions set forth under the AC Test Circuits And Waveforms. In some cases, the test conditions are further defined by the AC Setup Conditions — this is generally the case with counters and flip-flops where setup and hold times are involved. All of the AC Characteristics are guaranteed with 50pF load capacitances and with the fewest number possible of outputs switching, depending upon the functionality of the device. One of the sets of limits is spec'd at 25°C and +5.00V V_{CC} — these relate closely to the standard Schottky specifications which are under similar conditions but use only 15pF load capacitances. While these numbers are convenient for comparing the two families, keep in mind that using full 50pF loads with the Schottky devices would add several nanoseconds to their propagation delays. These numbers are ideal for checking out test jigs and correlating data since they do not involve temperature or supply voltage spreads. For system design, full specifications are included that include temperature and supply voltage variations — in one case the military ranges and in the other, the commercial ranges.

AC TEST JIGS AND SETUPS

Each FAST data sheet spells out the test circuit used to check AC performance, the waveforms, measurement points, rep rate, test loads, etc. But there are only the quantifiable variables involved in this testing. There is another more complex side to the issue — test jigs and equipment setups.

To get an appreciation for the problems involved in testing FAST, consider these facts. The output rise and fall times on FAST outputs are very sharp. Translating these edge rates into the effective sine wave equivalents generates frequencies on the order of several hundred MHz. At these frequencies, attention to RF phenomena is required.

Because of these RF frequencies, it is necessary to have an AC test jig that has minimal modifying effect on the input and output waveforms. To do this the jig must be constructed properly. The following items are key in dealing with AC jig construction.

BYPASSING CAPACITORS

Signetics uses high quality capacitors that have good RF qualities to decouple the power supply lines on the test jig, right at the V_{CC} pin to the ground plane. Four capacitors with absolute minimum lead length are used. Microwave chip capacitors are recommended. (Note: In some sensitive test environments it is advisable to decouple the V_{CC}, as well as bypass. This is done by passing the V_{CC} through a wire wrapped around a ferrite core 6 – 8 times. The inductor created helps decouple the noise from V_{CC} and reduces dramatically, the tendency for feedback oscillations through the V_{CC} and ground current loop. This is a key problem on clocked parts since the ground bounce created by the fast edge rates and high currents will effect V_{CC} and ground substantially and thereby effect internal thresholds.) These are one each, 10μFd dipped tantalum, 0.1μFd dipped tantalum or chip, .001μFd chip and 100pF chip.

Testing And Specifying FAST Logic AN202

GROUNDING

One of the biggest contributors to waveform degradation is improper grounding. In reference up to the test jig, the grounding is best done with one or more large ground planes that are directly connected to the ground pin of the test socket. The Signetics AC Test Jigs, both DIP and SO styles, are constructed as a four layer PC board with the 2 internal layers as ground planes. Ground planes are also interdigitated between all signal lines to decrease crosstalk. There are holes drilled in these and they are plated through to connect with the internal 2 layers and the top and bottom layers. See Figure 3 to see the interdigitated ground planes on the PCB layout of the SO jig. This grounding scheme has been used with great success in 10k and 100k ECL fixturing. The board is laid out so that the characteristic impedance of the signal lines is 50Ω. This is done by using industry standard stripline techniques. The ground plane also passes down through the center of the part on the bottom side of the board and ground pin is soldered to it using copper wire to connect the pin and the ground plane. On the top side of the board, the V_{CC} plane goes through the center of the part too, and connects to the V_{CC} pin in like manner as the ground pin. See Figure 1. The bypass capacitors are attached on the bottom side to the V_{CC} pin from the ground plane, see Figure 1. As the V_{CC} is brought on board, the V_{CC} wire is wrapped around a ½ inch ferrite core, 6-8 times, then makes connection with the V_{CC} plane on the top side.

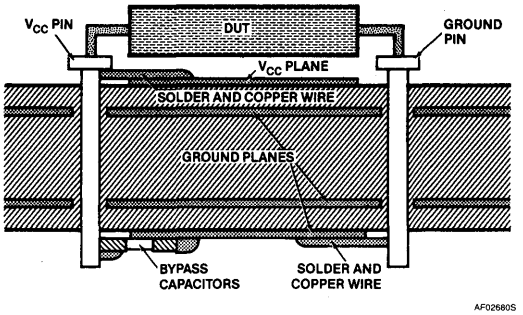


Figure 1

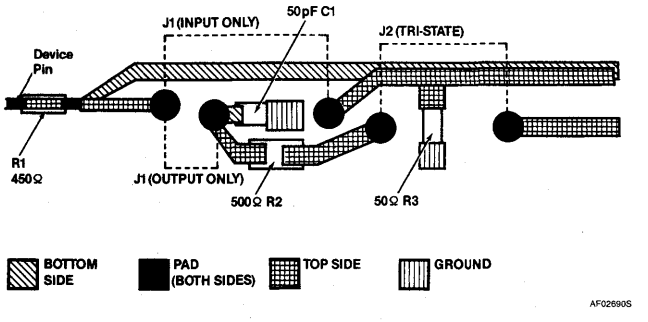


Figure 2a. FAST AC Test Fixture — Board Layout

INTERCONNECTS

The next concern is getting the input signal to the part and the output signal to the measurement system. As stated before, the Signetics jig is laid out for a 50Ω characteristic impedance. We recommend that the user maintain a 50Ω environment for the input signal as close as possible to the input pin and then terminate in 50Ω. On our jig, we terminate with a 50Ω chip resistor. The signal is brought on board through an SMB connector to the 50Ω trace on the top side of the board. The signal is terminated by the chip resistor, R3, see Figure 2a and 2b. The signal proceeds to the DUT pin, a distance of about .5 inches, through Jumper 1 (in the Input Only position), and the rest of the trace. The same pin on the opposite side of the board has a 450Ω chip resistor soldered to it. The other side of this resistor, R1, is soldered to a 50Ω trace on the bottom side of the board that runs to an SMB connector on the edge of the jig. This connects to the 50Ω input of the Sampling Oscilloscope. This 450Ω resistor in series with the 50Ω input of the scope creates a 10X divided 500Ω probe for the scope and provides impedance matching for the scope. See Figure 2b. This circuit also doubles as the resistive portion of the FAST AC Output Load and thereby allows the output to be sensed in the same fashion. When the input is not used for a signal or generator input, the line may be switched to one of three voltage sources. V_S 1 – V_S 3, by the use of a DIP switch on each pin. It may also be left open and then the 50Ω pull-down resistor that is used for an input terminator, pulls the line to ground and can be used as a hard low level. See Figure 2b. This scheme eliminates excessive cabling to each input to provide static input levels and thereby reduces parasitic inductances and cross-talk. It also eliminates the need for bulky and sometimes unreliable high impedance probes by using the 50Ω input of the Sampling Scope. With the designed-in flexibility of Jumper 1 and Jumper 2, and the selectable nature of V_{CC} and Ground pin designations, one can configure this board for any V_{CC} and Ground pin designations, select which pins are outputs or inputs and even provide the proper pull-up for 3-state outputs. This makes the board entirely universal for designated V_{CC}/Ground configurations. To explain this, the output of the device is connected to its capacitive load by Jumper 1 in the Output Only position. This means that no pin can be both output and input at the same time, but can be either. Jumper 2 allows an output to be connected to the 3-state pull-up resistor, R2, and have that connected to the needed 7V. See Figure 2a and 2b. The scope is connected in the same way as the input, with the 450Ω resistor and the 50Ω of the scope comprising the 500Ω needed for the FAST load. One other consideration exists. In small part quantity testing, the elimination of a socket is very desirable, using inserted pins that are flush with the jig. In larger quantity testing, sockets may be needed, however. If this is the case, some degradation in the performance will occur due to the increased lead inductance for each pin, which is observable, and the addition of group delay through the socket may alter or affect the readings obtained.

7

Testing And Specifying FAST Logic AN202

HIGH-FREQUENCY DESIGN

The exact jig delay time is determined by the size of the universal jig that is being used. It is important to know that the frequency response of the jig must be High to prevent any delay factor from varying with the edge rates. The frequency response of the jig indicates how constant the impedance remains over frequency. The characteristic impedance of a transmission line is expressed as . . .

$$Z_o = \frac{V}{I} = \sqrt{\frac{L_o}{C_o}}$$

Where L_o is the inductance per unit length, C_o is the capacitance per unit length, Z_o is in Ohms, L_o in Henrys, and C_o in Farads. Propagation velocity and its inverse, delay per unit length d, are also expressed in L_o and C_o. . .

$$V = \frac{1}{\sqrt{L_o\ C_o}} \qquad \delta = \sqrt{L_o\ C_o}$$

where δ is expressed in nanoseconds, L_o is in microhenrys per unit length, and C_o in microfarads per unit length. From this, it is clear that if the Z_o changes over frequency, then the delay per unit length will vary as well. Therefore, it is imperative to know how the jig responds over frequency and that all measurement line lengths are identical.

Frequency response also depends on the phase as well as the magnitude of the impedance. If the phase changes so does the delay, since delay is the derivative of phase change with frequency. An S-parameter analysis is needed in evaluating jig performance.

UNIVERSAL JIG CONSTRUCTION

Jig universality is with respect to chip pin count and V_{CC} and ground pin placements and as such, separate universal test jigs are built for 14, 16, 20, 24, and 28 pin parts.

An S-parameter analysis was performed in a network analyzer to optimize the jig layout. This assured that the jig had a flat frequency response over the spectrum of interest for FAST products. Figure 2b shows the schematic of the fixture and Figure 2a shows a drawing of the board layout, component placement and signal paths. The equipment used to analyze the jigs and loads was: HP8505A Network Analyzer, HP8503A S-Parameter Test Set, HP8501A Storage Normalizer. In some measurements the equipment was driven by an HP9845B desk-top computer.

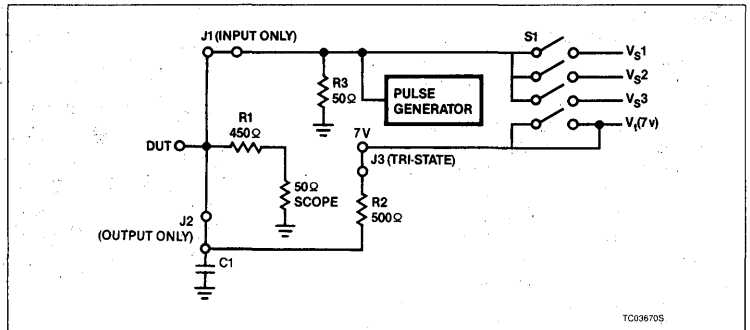


Figure 2b. FAST AC Test Fixture — Schematic

Jigs produced in this way should have minimal lead length to reduce the characteristic inductance. This in turn minimizes reflections with their accompanying waveform distortions and measurement inaccuracies.

AC TEST LOADS FOR THE SIGNETICS UNIVERSAL JIG

As stated previously, the Network Analyzer was also used to design and optimize AC test loads to be used with the universal jig. FAST product loads require 50pF load capacitance and 500Ω resistance to ground.

Signetics meets the 50pF requirement through the use of a 45pF load, 4pF jig capacitance, and 3pF probe capacitance. The result, 52pF, is slightly more stringent than required.

A few words about load capacitors are in order. All capacitors have an associated inductance. Due to this inductance, a capacitor will form a series resonant circuit at some frequency. For single 50pF capacitors, this typically occurs between 200 and 600MHz depending on the type of capacitor. Above this resonant frequency, the capacitor has inductive characteristics and does not present a capacitive load. This is very important with FAST because harmonics due to the sharp edge transition rates occur at 600MHz and above.

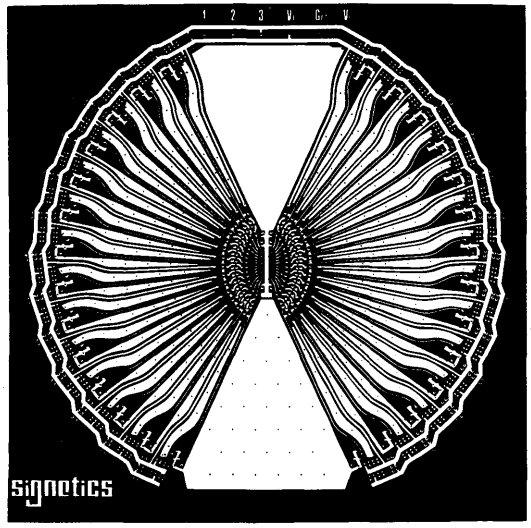
The Signetics FAST loads solve this problem by reducing the load capacitor lead inductance by paralleling three 15pF chip capacitors. The resulting load is 45pF. At the same time, since smaller value caps are used to build up the capacitive load, the associated series resonant point is above 1.2GHz.

The load resistors are 1/8W selected 510Ω ± 10Ω chip resistors.

The entire load assembly is constructed on the jig PCB along with the input termination, and the jumpers with select an input or output path. The load circuit is detailed on the FAST data sheets for 3-state parts.

CORRELATION

While numerous ATE systems are available and are very efficient, it is imperative that the ATE correlate to a user's bench setup. Since the Signetics FAST parts are all characterized on the setup described in this note, it is just as important that the user bench jigs meet the same performance criteria. Without similar jigs, it will be very difficult to correlate AC data.



CD07580S

Figure 3

Signetics

AN203
Test Fixtures for High-Speed Logic

Application Note

ALS Products

INTRODUCTION

The Signetics Standard Products Division (SPD) operates a Characterization Laboratory in Orem, Utah. This Lab maintains the capability of testing the 11 logic product families the Division supports. These include: AuTTL-74XXX, Schottky-74SXXX, Low-Power Schottky-74LSXXX, FAST-74FXXX, ALS-74ALSXXX, High-Speed CMOS-74HCXXX, High-Speed CMOS/TTL-74HCTXXX, Advanced CMOS/TTL (ACL)-74ACT11XXX, Advanced CMOS (ACL)-74AC11XXX, and both 10K and 100K ECL.

Due to the great diversity of product families and the different testing requirements and complexity of the product types of each family, Signetics SPD Characterization has designed and built a bench test AC fixture that is specifically designed to address to only the High-speed logic families. It has the advantages of being very versatile, has high bandwidth capability ($\geqslant$ 750MHz), is 50Ω system compatible, and is manually programmable for the input static voltages. This provides the ability to have one fixture that addresses many product types across families. The extent of this versatility is explained in the following Application Note. The families that this fixture is intended to support are: FAST, ALS, ACL, 10K ECL, and 100K ECL (Note: This fixture is compatible with any 500Ω pulldown load.)

THEORY OF OPERATION

There are several key points in testing the faster edge-rate logic families. They are:

- Very good bypassing and decoupling (they are different).
- Large ground and V_{CC} planes
- Low-impedance signal lines (i.e., 50Ω)
- Signal lines that are uniform in impedance over frequency
- Signal lines must have high bandwidth (> 500MHz)
- Low-inductance paths for the DUT leads, including V_{CC} and GND
- Output AC load close to the DUT

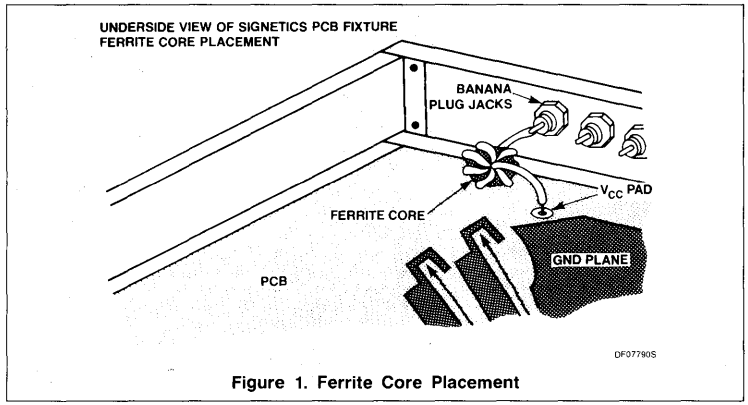


Figure 1. Ferrite Core Placement

- Measurement point close to the DUT
- Avoidance of ground loops (especially on inputs at DC levels)

Additional items of concern to the test engineer and the manager are:

- Versatility and/or ease of use (there are trade-offs)
- Cost
- The number of fixtures needed to support products

Each of these concerns have merit and must be understood by the user of these logic families if valid and correlatable results are to be found.

V_{CC} and GND

The secret in V_{CC} and GND use in fixturing is to do the things that reduce the noise that can: 1) get to your part, and 2) come from your part. This is done by reducing the noise of the V_{CC} as it arrives to the fixture, by judicious application of frequency dependant bypassing at the DUT V_{CC} pin to GND and reducing inductance from the V_{CC} and GND pins of the DUT to the point where good contact of the bypassing and V_{CC} and GND planes occur. All of these are techniques used in good RF and microwave board design. By reducing parasitic inductances and cleaning up any sources of noise, good signal integrity is better maintained.

These points are evident in the fixture Signetics has designed. Part of the noise reduction of the power supply as it arrives is done by bypassing the power supply at its terminals. The power is then brought to the fixture via banana cables, (as short as possible), to jacks on the chassis of the fixture. An 18 gauge wire, attached to the jack, is wrapped through a $^{3}/_{4}$ inch ferrite core 8 to 12 times for decoupling of any spikes. (Details of the cores used are included in the parts list.) This acts as a Low-pass filter. The wire is then soldered to the bottom of the PC board onto the large V_{CC} plane that narrows to the V_{CC} bus running between the pins of the DUT. See Figures 1 and 2 for detail.

Triangle-shaped, the V_{CC} plane provides a Low inductive path for the V_{CC} to the DUT pin. See Figure 2 for the board layouts. The V_{CC} bus from this plane travels down between the DUT pins to that connection. This is so connection to the V_{CC} bus is easy and very short. The DUT may have V_{CC} located on any pin with this configuration. The pin is connected to the V_{CC} bus by soldering small copper braid or similar Low-inductance wire capable of carrying the current for the device, see Figure 3.

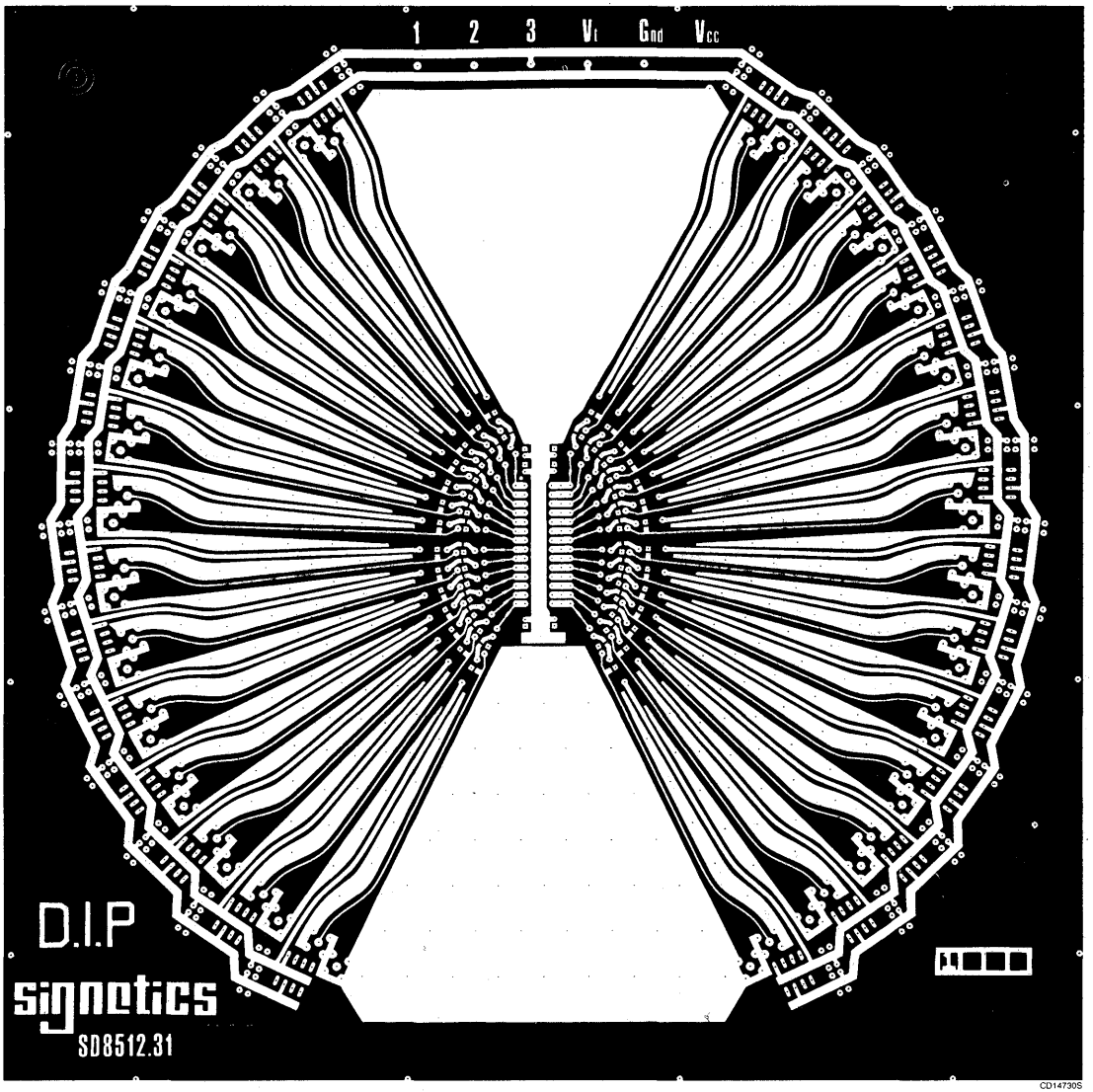


Figure 2a. Board Layout - Top Side

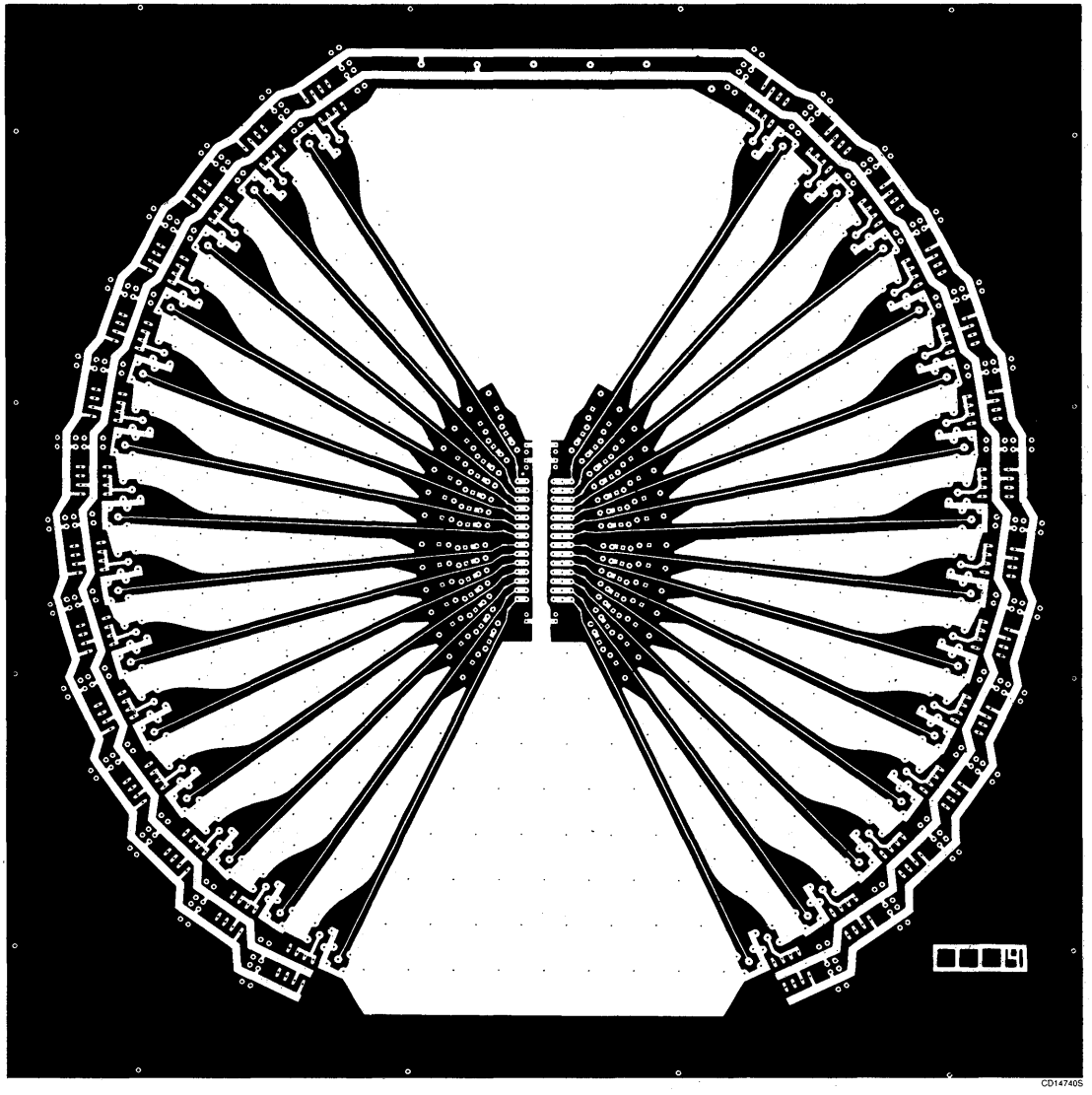


Figure 2b. Board Layout - Bottom Side

Test Fixtures for High-Speed Logic AN203

On the opposite side of the top layer of the board is a triangle-shaped ground plane. Ground planes are also located on the bottom layer of the board in the same places as the V_{CC} and ground planes of the top layer. Since this fixture is laid out for 50Ω stripline, layers 2 and 3 are almost total ground plane, with holes in them for feed-throughs and components. Also found between the signal lines, on the top and bottom layers, are ground plane "fingers" that are connected to all 4 layers by plated-through holes. This provides good separation of the signal lines resulting in lower crosstalk.

The bottom layer ground plane consists of two triangle-shaped planes connected by a bus strip that runs between the DUT pins. This was done for 3 reasons: First, this allows connection of any ground pin of the DUT to the ground, regardless of location; like the V_{CC} connection on the top layer. Second, it allows the connection of the bypass capacitors from the V_{CC} pin to the ground with the shortest possible lead length. Characterization uses typically 2 or 3 ceramic chip capacitors and 1 or 2 dipped tantalum capacitors (35V) to bypass the V_{CC} pin. It is important to keep the dipped tantalum capacitor's leads as short as possible to reduce series inductance. The recommended values of capacitors are: 100pf, .01μf, .1μf. and 10μf. We have found at times, the need to adjust these values depending upon the product type and its performance. Some noise sensitive circuits need more bypassing in the lower and extreme higher values of capacitance. And third, the connection of the two planes eliminates possible ground loops and the feed-throughs create a ground mesh and give an excellent ground plane for the circuit. Figure 3 illustrates the bypass connections.

BYPASS AND DECOUPLING

It is important to understand the difference between decoupling, as with the ferrite core, and bypassing, as with capacitors. Decoupling occurs as or high-frequency signals are removed by saturation of the ferrite core. This prevents "noise" that may be on the V_{CC} power supply from getting on the V_{CC} plane. The action of the bypassing capacitors is to: 1) "pass" any non-DC signals that occur on the V_{CC} (due to the part's operation) to ground, and 2) be able to provide the "instantaneous" current demands of the part as it switches.

The various values of capacitors are intended to provide a Low-impedance path at all operating frequencies. Since real-world capacitors have resonance points at a given frequency, depending upon their value and type of capacitor (and actually turn inductive above the resonance point), using different values that have different resonance points allows an across-frequency Low-impedance path for V_{CC} noise.

An important point in the use of bypass capacitors is the minimization of lead length. Lead length represents inductance; inductance in series with the capacitance. If it is too much, it can cause resonance and oscillation problems with the part and/or power supplies and nullify the benefit of the capacitors. It also plays a major part in inhibiting the effect of the "instantaneous" current response needed by the part from the bypass capacitors. It actually can cause the ground of the device to track the change in current to the degree of the lead inductance. The lower the inductance, the lower the "ground bounce" effect. Hence, short or no lead lengths on capacitors are needed to help prevent the effects of ground bounce.

SIGNAL LINES

A signal line is defined as a line that carries the input stimulus, either DC or AC, or output response, to or from the device. Since these signals are measured and determine the data which characterizes the part, it is critical that they are of the highest integrity and represent, as far as physically possible, the action of the part; not the nuances of the fixture. To achieve this, the line must not be able to change the signal over the measureable frequencies of the device, nor affect the delay of the part.

The fixture as designed, has 50Ω signal lines determined by a stripline layout method. The 50Ω value was selected for several reasons: 1) the 50Ω value matches impedance with the pulse generators that are used as input stimulus. 2) The output loads specified for this fixture are either a 500Ω pulldown or a 50Ω pulldown (ECL), in parallel with a capacitive load. This allows the 50Ω signal line to be terminated into this load for either a 10:1 or a 1:1 match. 3) A Low-impedance line will have better characteristics with regards to crosstalk and resisting external noise.

There are two types of signal lines on this fixture: input and output; both of which are 50Ω transmission lines. The input line is on the top side of the board and is always terminated in 50Ω. It is connected to the DUT via a .3" jumper, Jumper #1 for input. When this jumper is installed, the DUT pin is available only as an input. To allow this line to be used as an output, a .1" jumper, Jumper #1 for output, is used instead of the .3" jumper. This connects the DUT pin to the AC load when the DUP pin is an output. See Figure 5.

The output signal line can be dedicated two different ways. The first method, used for ECL, is to leave shorted the 50Ω trace and have it run directly into the SMB connector into the 50Ω sampling system. The second method is to cut the trace at the DUT pin and solder the 450Ω chip resistor, R1, across the cut. This, combined with the 50Ω scope, then appears to the part as either a 500Ω probe for the input signal or the 500Ω output AC load for the output signal.

The signal lines are equal length and therefore do not introduce any extraneous delay from pin to pin. We also characterized the impedance of the lines over frequency to ensure minimal distortion over the frequency range and any effective change in propagation delay caused by the relationship of inductance and group delay. Figure 4 illustrates the frequency response of the signal lines in impedance.

This is considered to be high bandwith and encompasses the frequency range exhibited by ALS, ACL, ELC, and FAST logic families.

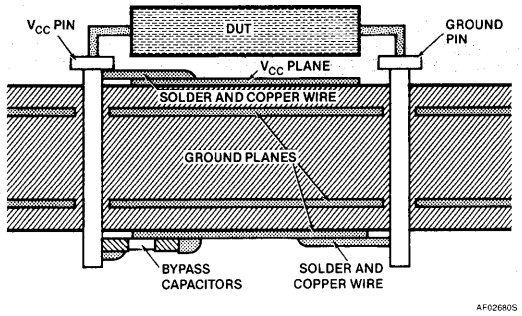


Figure 3. Decoupling Connections

Test Fixtures for High-Speed Logic

AN203

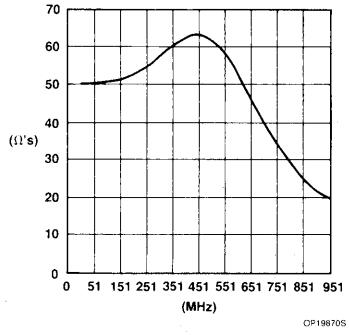


Figure 4. Signal Line Frequency Response

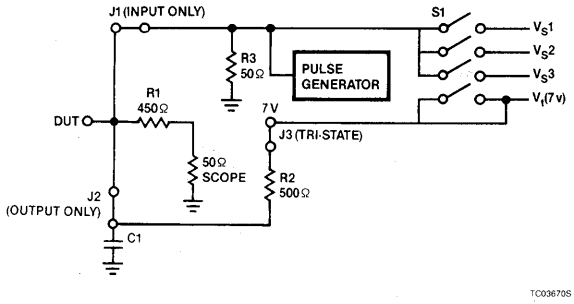


Figure 5. Signetics PCB Fixture Schemetic

LOADING

The explanation of the two types of AC loads that may be used will be covered in two parts. First the ALS, ACL, and FAST implementation will be discussed, then the ECL implementation.

ALS. ACL, and FAST Implementation

The FAST, ALS, and ACL product families AC load is specified as a 50pF capacitor and a 500Ω resistor in parallel. This load has the advantage of being adaptable to both a High-impedance (A.T.E.) or a Low-impedance (bench) measurement environment. The Signetics fixture uses a Low-impedance environment primarily for two reasons. The first reason is that experience of the last 5 years has told us that High-impedance probes represent a reliability concern and can introduce hard to detect errors into the waveform. The second reason being that most suppliers of these technologies provide data based upon the Low-impedance approach and most large users of these products do so as well. This also allows the fixture to be used for ECL testing since that product uses a totally 50Ω environment. Figure 5 illustrates how this test fixture implements the 50pF/500Ω load schematically.

The fixture was laid out to present the load as close as possible to the device, and yet allow for flexibility in deciding if a certain pin is an output or an input. This distance is critical due to its inductive effect upon ground bounce phenomena. *It is acknowledged here that a fixture dedicated to a single device type without jumpers, and therefore placing the load virtually on the pin of the device, would show the ground bounce phenomena for simultaneous switching to be less than that of this fixture. However, this fixture can be so dedicated by not using the pads as provided, but rather by using the ground bus, like the bypass capacitors used. The flexibility of this fixture substantially reduces the cost of fixturing for these families. Studies on simultaneous switching with this fixture have shown dramatically favorable results to previous fixtures. Those studies continue. For work other than that of simultaneous switching, there will be no appreciable difference with a dedicated fixture.*

As illustrated in Figure 5, the load is shared with the 50Ω input of the measurement system; a 50Ω sampling oscilloscope. The 450Ω resistor: R1, is soldered to the socket pin of the device and is in series with the 50Ω input of the scope. Figure 6 illustrates this on the board layout of one input/output pin. This allows virtually a probe tip on the device pin. The load capacitor: C1, is a 33pF ceramic chip capacitor. This is added to the measured value of 17pF of board capacitance, achieving the 50pF value specified for the load. The distance from the pin to the capacitor is .5 inches and is adequate for the testing of these product families.

For testing 3-State parameters, the 500Ω resistor: R2, is connected to it's pullup supply. V_t via a .3" jumper: Jumper #2. The V_t supply is bussed to each pin and may or may not be connected with that jumper. See Figures 5 and 6.

ECL Implementation

When testing ECL product, the 450Ω resistor: R1, is not used, Rather, this point is left shorted together in the construction process. Also for ECL, the load chip capacitor: C1, the tri-state pull-up resistor: R2, the 50Ω terminator: R3, and the "output only" jumper: Jumper #1, are not used. The input signal travels down the input path, is jumpered using the "input only" (Jumper #1), goes to the device, travels out the output path (left shorted, no R1), and proceeds to the scope. When the signal is an output, the "input only" jumper: Jumper #1, is removed and a 50Ω terminator is connected to the SMB connector as the load or the 50Ω input of the scope. See Figure 7.

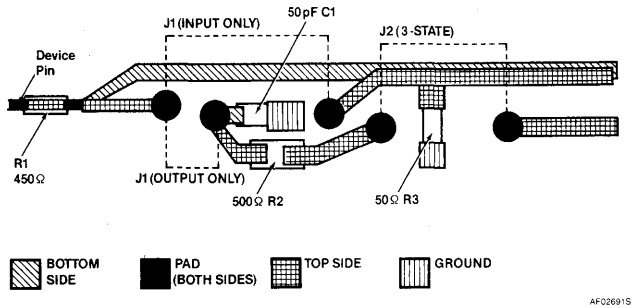


Figure 6. Signetics Fixture - Board

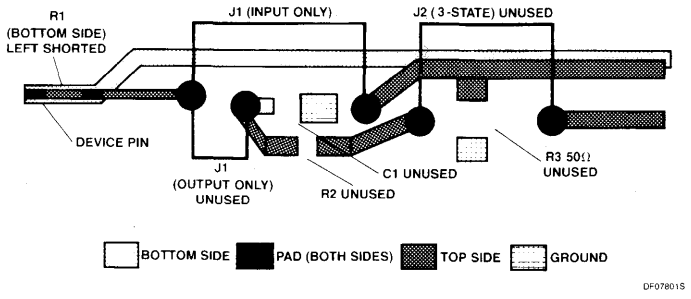


Figure 7. ECL Configuration

Test Fixtures for High-Speed Logic AN203

INPUT STIMULUS AND MEASUREMENT

When the input is not used for a signal input, the line may be switched to one of three voltage sources: V_S 1 through V_S 3, by the use of a DIP switch on each pin. It may also be left open and then the 50Ω pulldown resistor: R1, pulls the line to ground and can be used as a hard low level. See Figure 5. These voltage levels are brought in from external supplies through banana connectors like V_{CC}. This scheme eliminates excessive cabling to each input to provide the static input levels and thereby reduces parasitic inductances and cross-talk. Each of the 3 busses and the V_t bus all have places for bypass capacitors in the event of noise on the static levels. Figure 8 illustrates the DIP switch and SMB connectors and how they control the input stimulus and output measurement.

As stated previously, the measurements are made with 50Ω sampling systems. The connections to these systems are made via SMB connectors. This was chosen since it is compatible with SMC; it is push-on, it is small for easy configuration, and it is capable of high bandwidth operation. Figure 8 illustrates where the connections are made, where the pulse generators connect to the input and an SMB connector. Since the 450Ω resistor: R1, is soldered directly to the pin of the device, the actual probe tip is at that point. See Figure 6. This has the advantage of eliminating any distance from the device to the probe tip, thus guaranteeing accurate results.

VERSATILITY AND COST

At some point, there is a choice between the most technically attractive options and the cost of options. This fixture has been primarily designed to optimize the cost effectiveness of test fixturing yet yielding a technically sound tool. To do this, a compromise has been made between the ease of use and the versatility.

In the construction of the fixture, a choice is made as to where the V_{CC} and GND pins are to be located. This then dedicates this particular fixture to part types with this V_{CC} and GND configurations. This is alos done with a dedicated fixture. However, on a dedicated fixture, the pins are individually constructed to be either an input or an output, and in so doing, the fixture is usable for 1-to-4 devices. The Signetics fixture, once dedicated to a particular V_{CC} and GND configuration, is built up to have both input and output components on all signal pins. The selection of which pin is an output or an input is made by inserting the appropriate jumper, See Figures 5 and 6. The same applies in doing tri-state testing. The tradeoff here is that it would probably take less time to setup the dedicated fixture than the Signetics fixture. To help compensate for that tradeoff, we have the three Vs supplies that may be switched into any pin to provide input static levels and eliminate the need to bus input High or Low levels by external cabling. For the user that means the only connections being made to the fixture are:

- the V_{CC} (banana jack)
- the GND (banana jack): this is the common ground of all input supplies.
- the V_S 1, V_S 2, and V_S 3 supplies (banana jack): these may be any voltage and are switchable. Signetics connects programmable supplies to these connectors.
- the V_t supply (banana jack): this is the 3-State pullup voltage and is permanently connected to the bus to each pin. It is selectable by Jumper #2, see Figures 5 and 6. For FAST and ALS products this is 7V. For ACL products this is $V_{CC} \times 2$ and it is not used for ECL applications.
- Input Stimulus (inside SMB connector: this is found on every input/output pin. More than one pin may be used in this manner. **CAUTION:** When using this connector as an input stimulus, make sure V_{S-1}, V_{S-2}, V_{S-3} are disconnected. This will short the power supplies to the generator if they are not disconnected.
- Output Measurement or Scope Connection (outside SMB connector: this is also found on every input/output pin. More than one pin may be used in this manner. Remember, if this pin is not connected to a scope and is an output, a 50Ω resistor must be connected here to ground to complete the 50Ω resistive load. Signetics has constructed 50Ω load by soldering a high-quality (High-frequency) 50Ω resistor inside a female SMB cable connector. See Figure 9.

CAUTION: V_{S-1}, V_{S-2}, and V_{S-3} are all on the same DIP switch. Since they connect to the same bus per pin, **ONLY ONE SUPPLY MAY BE CONNECTED AT ONE TIME**, Otherwise, this will result in a short between power supplies connected.

With these 6 connections, the fixture is capable of testing the product lines as mentioned.

The cost of this fixture ranges from 550 per fixture, dedicated to a 20-pin device in quantities of 1 – 10, to as low as 385 per fixture of the same type in quantities over 100. This is not substantially higher than the cost of a dedicated fixture; which is estimated at 200 – 500. The factor to consider would be the quantity of fixtures for the number of products to be tested. To have a dedicated fixture for every 2 – 3 product types versus a "universal" test fixture for 20 – 30 product types is worth considering from a cost standpoint.

Included in Appendix 1 is the parts list for this fixture and the supplies used by Signetics. This in no way constitutes Signetics endorsements of these suppliers and the customer may select their own supplier if they so desire. This fixture is offerd to the public to duplicate and use within their own environments. Signetics will not provide any materials but will allow the manufacturers of the board and materials to build and/or supply for any requesting party. Pricing and availability are left to the vendors and Signetics has no control over those issues. The intent is to provide something for users of high-speed logic that has been proven and tested in a true high-speed use, and provide a characterization of these products prior to their introduction to the market place.

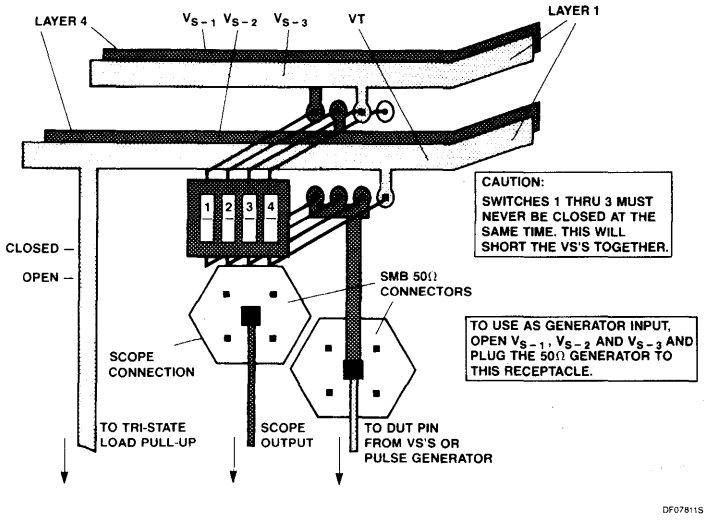


Figure 8. DIP Switch Connections for V_{S-1}, V_{S-2}, V_{S-3}, and V_T and the SMB Connectors for Input Signals and Output Measurement

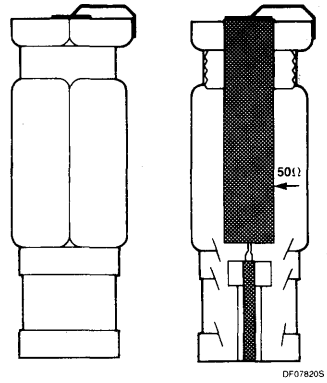


Figure 9. 50Ω Load Resistors Using Output Pin SMB Cable Connectors

5. APPENDIX I - Component and Vendor List

The following prices are quoted for a 30 piece build of a 24 pin test fixture and are not binding in any way.

1. Printed circuit mother board.
   SO and SOL -#SD8512.28
   DIP -#SD8512.31
   Requirement: 1 per part configuration

   Supplier: Prototype and Production Circuits
   8040 S. 1444 W.
   West Jordan, UT 84084
   (801) 566-5431

2. SO and SOL sockets.

#_PINS	PART_#
14	001-014
16	001-016
16L	001-116
20	001-120
24	001-124
28	001-128

   SOIC through hole socket
   Requirement: 1 per board

   Supplier: Surface Mount Devices, Inc.
   PO Box 16818
   Stamford, CT. 06903
   (203) 322-8290

3. L$G-1AG14-1 Socket Terminal Pins.
   For DIP boards - number of pins equal to the part pin count times by (7) seven.
   $24 \times 7 = 160 \times .20 =$
   For SO and SOL boards - number of pins equal to the part pins count times by (5) five.
   $24 \times 5 = 120 \times .20 =$

4. Shorting Blocks (Jumpers).
   .3 inch 8136-475G1 Requirement: 1 per pin
   cost per part $\times$ 24 =
   .1 inch 8136-651P2 Requirement: 1 per pin
   cost per part $\times$ 24 =

   Supplier: Augat

5. Chip Resistors.
   50Ω 1% CRCW 1210 Requirement: 1 per pin
   cost per part $\times$ 24 =
   450Ω 1% CRCW 1206 Requirement: 1 per pin
   cost per part $\times$ 24 =
   500Ω 1% CRCW 1206 Requirement: 1 per pin
   cost per part $\times$ 24 =

   Supplier: Dale Electronics, Inc.
   2300 Riverside Blvd.
   Norfolk, Nebraska 68701
   (402) 371-0080

6. Chip Capacitors.

Ceramic Part_#		Requirement
33pf	500R15N330JP	1 per bin
	cost per part × 24 =	
15pf	500R15N150JP4	1 per board
	cost per part × 1 =	
.015μf	500$41W103KP4	1 per board
	cost per part × 1 =	
.1μf	500$41W104KP4	1 per board
	cost per part × 1 =	

Supplier: Johanson Dielectrics

7. Dipped Tantalum.

Ceramic		Requirement
10μf	106k025NLF	1 per board
	cost per part × 1 =	
47μf	476K020WLG	1 per board
	cost per part × 1 =	

Supplier: Mallory

8. Ferrite Core.

T80-1 Requirement: 1 per board

cost per part × 1 =

Supplier: Amidon Associates
12033 Otsego Street
North Hollywood, CA 91607
(818) 760-4429

9. Mounting Screw.

4-40 × 1/4 Phillips pan head machine screw Requirement: 16 per board.

cost per part × 16 =

Supplier: Bonneville Industry Supply Co.
45 So. 1500 W.
Orem, Utah
(801) 225-7770

10. Bannana Plug Jack.

H.H._Smith_Type	Order_#	Requirement
White 1509-101	28F1178	6/board-color your choice
Red 1509-102	35F870	6/board-color your choice
Black 1509-103	35F869	6/board-color your choice
Green 1509-104	28F1179	6/board-color your choice
Blue 1509-105	28F1180	6/board-color your choice
Yellow 1509-107	28F1182	6/board-color your choice

cost per part × 6 =

Supplier: Newark Electronics

11. Switch.

76P$B04 4-bit side actuated piano-dip Requirement: 1 per pin

cost per part × 24 =

Supplier: Grayhill Co.

12. Connectors - Snap-on SMB.

51-051-0000-220 - Straight jack receptacle Requirement: 2 per pin

cost per part × 48 =

Supplier: Sealectro

13. Mounting frame.
    Signetic's number CB-1.0 Requirement: 1 per test fixture

    Supplier: Electronic Chassis Corp.
    468 North 1200 West
    Lindon, Utah 84062
    (801) 785-9113

14. Hookup wire.
    No. 18/20 gauge Teflon coated — about 24 inches per test fixture.

The following components may be needed in use of the test fixtures but are not part of the test fixtures.

61-001-0000-89	50Ω terminator plug	As required or hand built with 50Ω resistor and 51-007-0000
51-007-0000	Straight Cable Clamp Type	As required
51-083-0000-222	"T" adaptor J-J-J	As required
51-085-0000	"T" adaptor J-P-J	As required
51-072-0000	Adaptor J-J	As required
51-073-0000	Adaptor P-P	As required
51-001-0020	Shorting plug	As required
61-002-0000-89	50Ω terminator jack	As required
Supplier:	Sealectro Corp (415) 965-1212	

6. APPENDIX II-Construction Hints

A suggested order of assembly is as follows:

1. Cut traces for 450Ω resistor. (Not needed for ECL)
2. Install SMB Connectors. Elevate base from board .05".
3. Install DIP Switches. Note: Numbers on switches may not correlate to Vs supply numbers.
4. Install Augat socket pin.
5. Install load/termination resistors and capacitors.
6. Strap V_{CC} and GND pins to appropriate bus strips.
7. Install bypass capacitors.
8. Clean flux off of board and components.
9. Check for lead to frame shorts on PLCC board. (Not discussed in App Note.)
10. Install banana jacks on frame.
11. Attach board to frame with 1/4 Phillips pan head machine screws.
12. Wrap wire 8-12 times around ferrite core. Leave enough wire to connect to frame and board. See Figure 1.
13. Connect V_{CC}, GND, and voltage supplies from banana jacks to board.
14. Remove all remaining flux. Keep "flux-off" from banana jacks.

Hints on construction:

— A .05" shim that fits under the SMB connector base helps elevate it during construction.

— Mount the SMB connector with flat side out rather that point side out. See Figure 8.

— Solder Augat socket pins in with a part inserted to hold the pins steady.

— "Piano DIP" switches have the numbers reversed from the Board notation. Taping a new number on the board designations will help match the switches.

— Hint for solder chip components: apply a small amount of solder on one side of the pads on the board.

— Keep DIP switches and SMB connectors spaced as far away from each other as the holes will permit, ie., push the SMBs in and the DIP switches out.

Signetics

AN205
Using FAST ICs For μP-To-Memory Interfaces

Application Note

FAST Products

INTRODUCTION

Most microprocessor-based systems use some form of bipolar interface between the processor and memory; only a very primitive system does not require such interface support. TTL devices in quad, hex, or octal configurations are used to meet functional and circuit-interface requirements of the system. For complex systems, the interface support may be extensive while, for simple systems, only a few devices may be required to ensure operational integrity. In a majority of system designs, one or more of the following interface requirements must be addressed.

- Buffering and Demultiplexing of Data/ Address Buses
- Signal Timing and Signal Isolation
- Address Decoding
- Bank Switching
- Handling of Wait States
- Adjusting Read/ Write Data Rates
- Refreshing Dynamic RAM
- Unique Interface Requirements such as Multi-Processor Networks, Data Communication Links, etc.

Interface support is an important part of the overall design job; when implemented with the proper parts, system efficiency can be dramatically improved, higher reliability can be obtained and the design can be executed with minimum parts. This Application Note shows how common interface problems can be solved by using a minimum of high-performance bipolar devices from Signetics.

BUFFERING AND DEMULTIPLEXING

Microprocessor outputs are inherently fanout-limited; thus, some form of buffering is required to drive multiple loads such as those found on address and data buses. Extended bus configurations coupled with MOS loads tend to produce large capacitive sinks which degrade waveforms and also increase propagation delays. The use of TTL buffers provides an easy and economical way of overcoming or, at least, minimizing these harmful effects. In those systems that use shared memories and direct memory access (DMA), buffers are frequently used for isolation and as a method for switching between multiple buses. Buffers are also commonly used to optimize signal-to-noise ratios and to drive multicard bus interfaces. For the most part, buffer and latch-control functions can be summarized as follows:

- Latch the address information in systems that use multiplexed buses.
- During read operations, avoid bus contention by preventing the system from driving the multiplexed address/ data bus until the address information is removed.
- Control the direction of data transceivers according to processor operation while preserving write-data and read-data hold times and avoiding bus contention when switching direction.
- Isolate the microprocessor from the system bus during DMA and multiprocessor operations.

With the use of 16-bit microprocessors, systems have become more sophisticated; likewise, buffer control and interface circuits have become somewhat more complex. Many of the 16-bit machines use multiplexed address/data buses to reduce I/O pin count; as a result, latches are required to demultiplex, hold, and buffer the address bus. Not only must the address information be latched at the correct time but the date bus must usually be buffered with bidirectional transceivers to provide the necessary drive. As previously indicated, the interface circuits must be able to avoid bus contention and, when required, to isolate the processor from the system bus.

Buffers and latch-control signals for three popular 16-bit microprocessors — the 8086, the Z8001, and the 68000 — are shown in Figure 1. For each processor, the buffer and interface functions are summarized at the bottom of the figure. Although the timing-and-control functions of the interface support circuits are fairly complex, these internal complexities are transparent to the user; only the bus connections and a few control lines are required to achieve the management goals of the system.

INTERFACE FUNCTIONS (8086 SYSTEM)

- Multiplexed address/data bus ($AD_0 - AD_{15}$)
- 3-State latches (74F373) used for demultiplexing; latches are continuously enabled by ALE until data is stable on the bus and a timing pulse is delivered by the microprocessor.
- HLDA is used to float address bus during DMA operation.
- Data bus buffered by 74F1245 or 74F245 Transceivers; data direction controlled by DT/$\overline{R}$ in minimum mode.
- Bus control and DMA isolation controlled by $\overline{DEN}$ is minimum mode.

INTERFACE FUNCTIONS (Z8001 SYSTEM)

- Address bus ($AD_0 - AD_{15}$) latched with 74F373s using $\overline{AS}$ for latch enable and $\overline{BUSAK}$ for isolation. (Note: The segmented outputs are designed to drive a Memory Management Unit with internal latches; however, in this application, the address outputs are prelatched since they are not stable for the entire cycle.)
- Data bus buffered with 74F1245s or 74F245s; $\overline{DS}$ and R/$\overline{W}$, respectively, control data direction and bus contention.
- BUSAK controls DMA isolation.

Using FAST ICs For μP-To-Memory Interfaces AN205

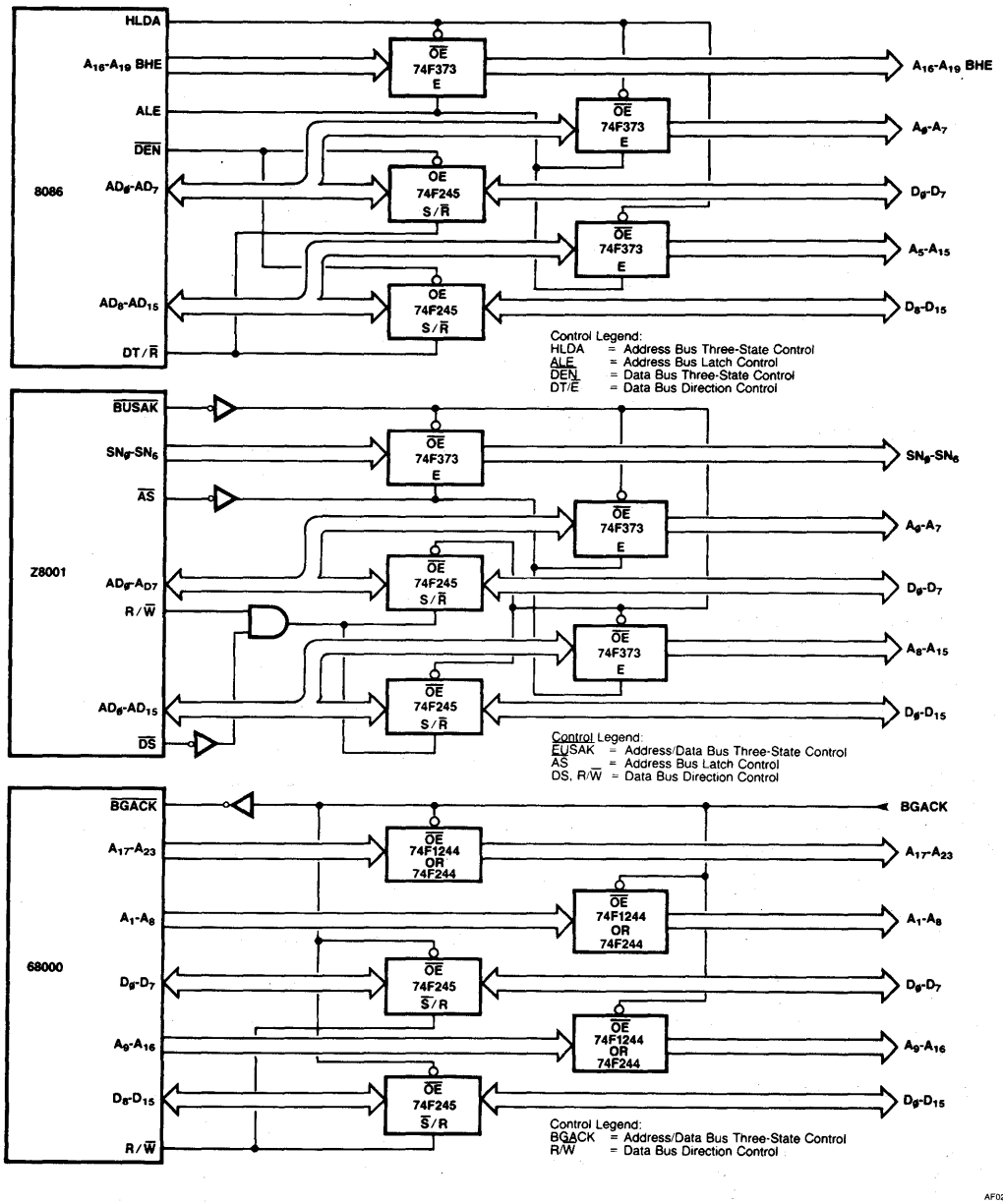


Figure 1. Examples of Processor-to-Bus Interfaces

7

Using FAST ICs For μP-To-Memory Interfaces AN205

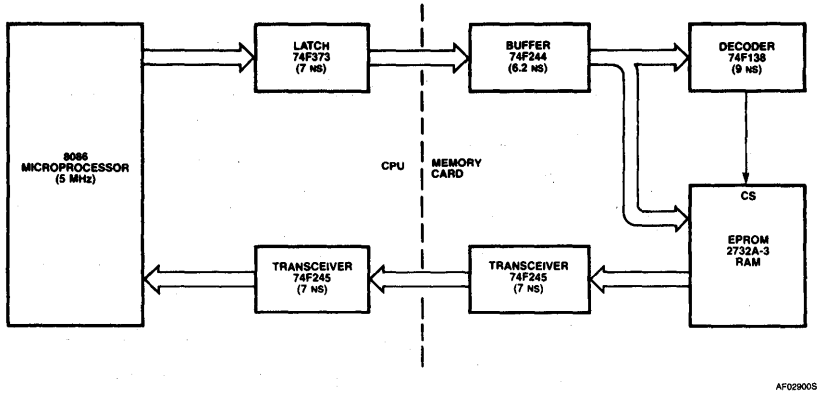


Figure 2. System Showing Typical Interface Delays

INTERFACE FUNCTIONS (68000 SYSTEM)

- Address bus buffered by 74F1244s or 74F244s and DMA isolation controlled by BGACK.
- Data bus buffered by 74F1245 or 74F245 Transceivers with R/W and BGACK, respectively, controlling data direction and bus isolation. (Note: In this configuration, a larger processor package is required since the address and data buses are separate; some advantage in speed and simplified timing are to be gained.)

Figure 2 shows the effects of buffers and an address decoder on the memory access time in a system configuration. The access time of the 8086 microprocessor is defined as the time from which a valid address appears at the output of the processor assuming that there are no wait states. Observe that each buffer and the decoding function adds a specific delay to the data-processing chain. In addition to these propagation delays, the system designer must consider capacitive loading, buffer access delays, (that is, are buffers enabled when valid data appears at input) and any other delay parameters that would extend the memory access time. (Note: The normal 8086 buffer control does not affect access time.) The delay should be calculated using maximum propagation delays over the operating temperature range of the system. Based on these considerations, the memory access time for the system shown in Figure 2 can be approximated as follows:

8086 READ CYCLE — Address Valid Output to Data Valid Input 460ns

2732 MEMORY ACCESS TIME (T_{CE})-T_{CE} = 460ns-3 (7ns) — 6.2ns-9ns = 423.8ns

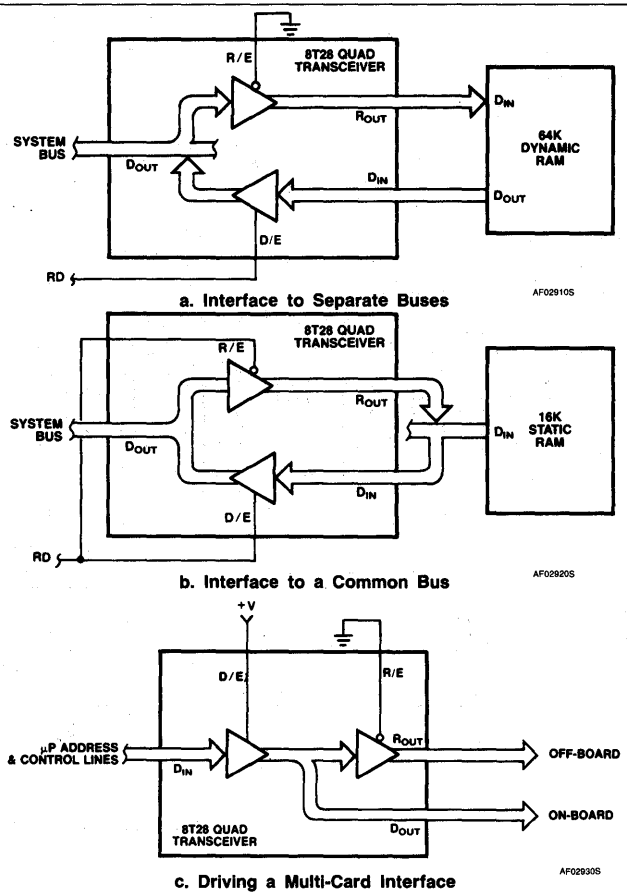


Figure 3. Using 8T28 Transceive to Obtain Optimum Interface Flexibility

Using FAST ICs For μP-To-Memory Interfaces AN205

BIDIRECTIONAL BUS INTERFACES

Virtually all microprocessor-based systems use a bidirectional bus interface between the processor and I/O peripherals; the memory interface may require separate-or-common bus connections. In either case, the 8T28 Quad Transceiver is well suited to this type of application. The 8T28 is able to drive a capacitive load of 300-picofarads without waveform degradation and the three-state outputs provide the switching speeds of TTL while offering the drive capabilities of open-collector gates. Typical bus interfaces are shown in Figure 3.

In Figure 3a, the transceiver provides a bidirectional interface between the system bus and separate input/output buses of the dynamic RAM. The D_{IN} bus is continuously driven while the D_{OUT} bus is gated onto the system bus via D/E.

Figure 3b shows a static RAM interface implemented by tying R_{OUT} and D_{IN} together. Here, the 8T28 functions as a normal bidirectional transceiver, providing buffered drive between the system bus on one hand and the memory I/O bus on the other. The bottom panel shows how the 8T28 can be used in the dual capacity of an on-board/off-board buffer/driver. To prevent signal degradation in such multi-board systems, the address/data/control buses must be buffered if off-board extensions are to be driven. Furthermore, the on-board/off-board buses should be buffer-isolated to prevent down-stream noise and/or failures from feeding back to the mother board. In Figure 3, observe that driver gates of the 8T28 are used to drive the on-board bus and receiver gates are used for the off-board bus. Low cost and minimum component count make the 8T28 ideally suited for such double-buffered applications.

MEMORY ADDRESS DECODING

In any computer system, information on the address bus must be decoded to generate select signals for memory and any I/O peripherals. There are numerous decoding schemes and a variety of implementation techniques. Generally, the methods used depend on system complexity which, in turn, depends on memory size, mapping parameters, access time, the particular technology, etc. Although simple decoders are frequently used in uncomplicated systems, the more sophisticated applications use PROMs to provide the required flexibility and to satisfy the mapping complexities that are usually encountered.

To develop trouble-free decoding circuits, the designer must be aware of those areas that can degrade system performance. For instance, caution is advised when using decoder outputs to terminate date write cycles. When read/write strobes (such as "E" on the 6801) are used to enable the address decoder, the data hold time is reduced because the trailing edge of the address decoder output now follows the trailing edge of the strobe signal to which the "hold time" is referenced. In systems that are sensitive to hold time, read and write strobes should not be used to enable address decoding circuits. Instead, the strobes should be gated with the decoder outputs to reduce the hold time.

Signetics makes a wide range of decoders, demultiplexers, and PROMs that are suitable for both simple and complex decoding functions. Some of the more common decoding applications are summarized in Figures 4 through 7.

Using FAST ICs For μP-To-Memory Interfaces AN205

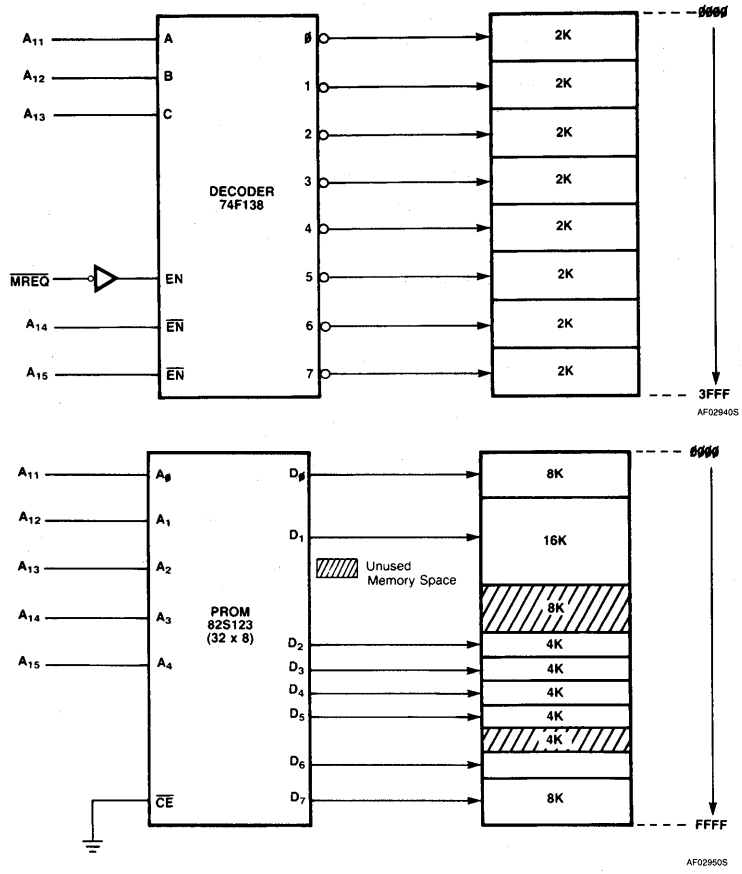


Figure 4. Two Simple Decoding Methods

OPERATION & APPLICATIONS SUMMARY

For small uncomplicated systems, the 74F138 decoder provides a cost-effective interface between the system address bus and memory. The configuration shown above is not only economical, it is fast, uses very little power, and requires no programming.

Such systems are commonly used to generate contiguous memory addresses and to decode memory segments of equal size. With additional decoding circuits, the memory mapping capabilities of the system can be expanded.

Where speed is not a critical factor, the PROM decoder shown below adds considerable flexibility with no increase in chip count. The 82S123 can generate contiguous or non-contiguous address space and can be memory-mapped to satisfy the requirements of most applications. Although the PROM decoder is a bit more expensive and uses slightly more power, it has the advantage of being field programmable.

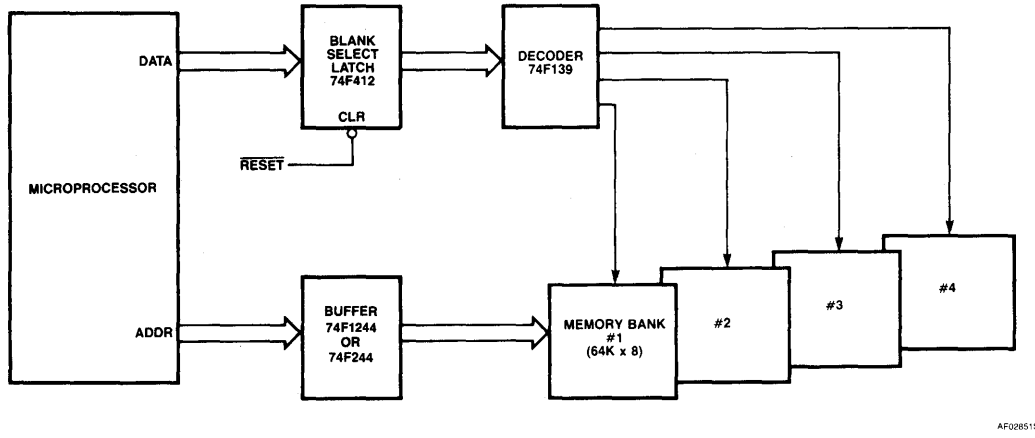


Figure 6. Extending the Logical Address Space Via Bank Switching

OPERATION & APPLICATIONS SUMMARY

In some applications, it is desirable for the system memory to extend beyond the logical address space of the processor. As shown, such a system can be easily implemented with a few interface parts and a bit of software. The four memory banks are wired in parallel; each bank can be as large as the logical memory space of the microprocessor — 512 bytes for 8-bits of address and 64K for a 16-bit address bus. An output port under software control selects the active bank; the bank address is decoded to ensure that only the appropriate memory bank is enabled. In this way, the possibility of bank contention is eliminated.

Memory allocation schemes such as these are frequently used in multiprocessor environments and, in this type of application, a copy of the operating system kernel must reside in each memory bank. The system can be enhanced by providing direct switching between the memory banks; however, additional hardware is required for such operations.

7

Using FAST ICs For μP-To-Memory Interfaces AN205

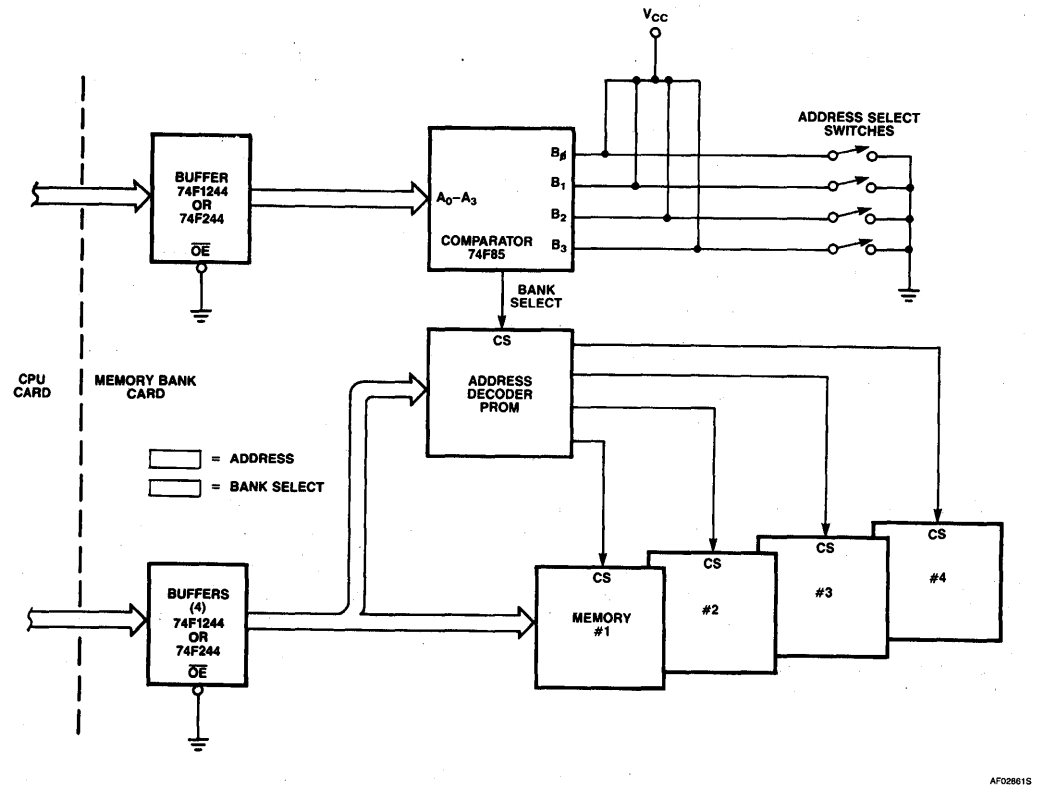


Figure 7. Multi-Board Decoding System With Extended Address Space

OPERATION & APPLICATIONS SUMMARY

In a multi-board system, the address decoding and memory-bank select functions can be implemented as shown here. The bank address on the memory card is identified by setting the address select switches of the comparator to a predetermined configuration. When the bank select signals from the CPU card match the present bank address, the PROM is enabled and the appropriate memory bank is placed on-line. Data bus control for the system is not shown.

The system show in Figure 6 and the one shown here are similar in that the four memory banks are wired in parallel and each bank can be as large as the logical address space of the microprocessor.

Using FAST ICs For μP-To-Memory Interfaces AN205

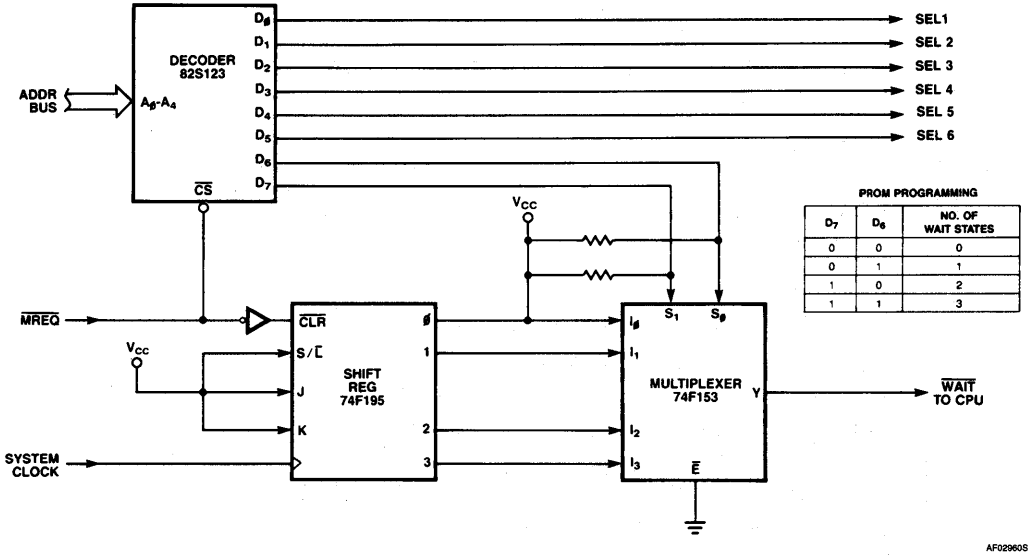


Figure 8. Programming Wait States to Optimize Data Throughput

SPECIAL MEMORY-INTERFACE CIRCUITS

In some applications, the memory interface circuits must be adapted to the unique requirements of the system. For instance, a system may use devices whose response time and wait-state requirements are vastly different, necessitating programmed wait states for optimum throughput.

Other examples include capturing a high-speed bit stream without the use of high-speed (high cost) memories, refreshing dynamic RAM via interleaving, and minimizing leakage problems when driving open-collector buses. Figures 8 through 11 show how Signetics ICs can be used to solve interface problems of this type.

OPERATION & APPLICATIONS SUMMARY

Using the "slowest" device in the system as a reference for data through-put is a gross waste of processor time. ROM is usually slower than RAM, and I/O devices are generally slowest of all. One way of reducing the harmful effects of these diverse characteristics is to program wait states for each device such that inactive periods for the CPU will be minimized. With the PROM decoder in the system shown above programmed in this manner, the multiplexer selects the appropriate tap of the shift register to initiate the required number of wait states. The wait cycle is terminated when a "1" is shifted to the selected tap; the shift register is cleared at the end of each wait state cycle.

7

Using FAST ICs For μP-To-Memory Interfaces AN205

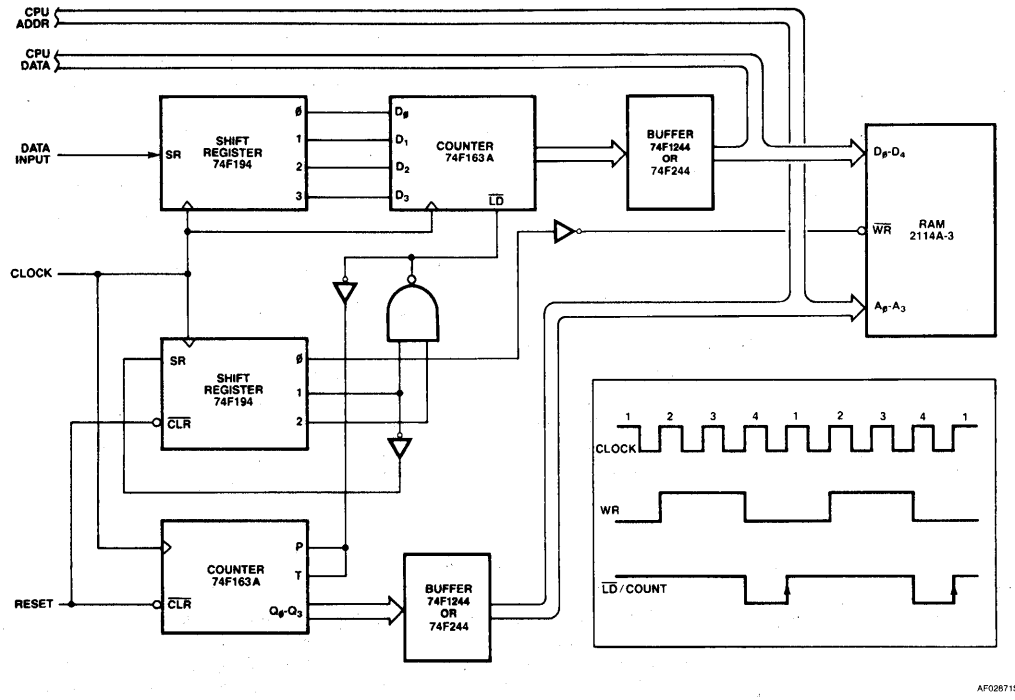


Figure 9. Storing High-Speed Serial Bit Stream With Low-Speed RAM

OPERATION & APPLICATIONS SUMMARY

In the design and use of logic analyzers, disk media, modems, and other similar equipment, a high-speed serial bit stream must be stored in memory. The above system shows how a 20MHz serial data stream can be captured and stored in a relatively low-speed RAM that has a 5MHz (200ns) cycle rate. The system uses a simple parallel to serial converter, thus, saving the cost of high-speed memory devices. Other than the synchronizing clock being supplied by the serial-input system and the setup/hold times of the shift registers being met, operation is simple and straightforward.

- Incoming serial data is clocked into shift register.
- After each fourth bit, data is transferred in parallel to a 4-bit counter (74F163) used as a latch.
- Data is written into RAM while four new bits enter shift register.
- Memory addressing is performed by incrementing the 74F163s and timing is controlled by a simple ring counter.

Using FAST ICs For μP-To-Memory Interfaces AN205

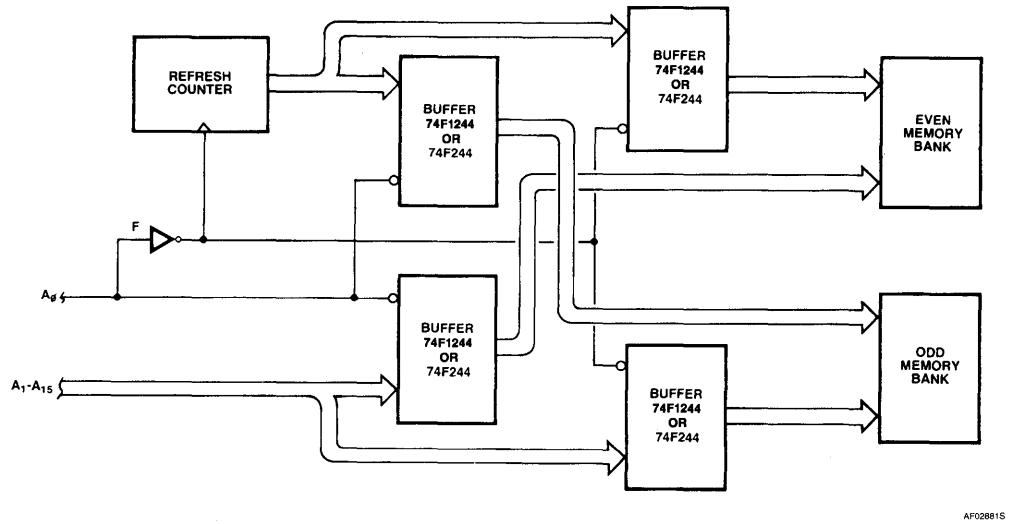


Figure 10. Using Interleaving Technique to Refresh Dynamic RAM Memories

OPERATION & APPLICATIONS SUMMARY

Most dynamic RAMs must be refreshed at least every 2-milliseconds to ensure retention of valid data. One method of memory refresh is shown in the above example. This system uses interleaving and relies on the premise that, during normal program execution, A_0 toggles frequently enough to refresh the RAM without slowing the microprocessor with wait-states or DMA cycles to refresh the counter. If the system program uses wait-states, halt instructions, or address incrementing is otherwise limited, A_0 may not toggle at a rate sufficient to accomplish refresh. For such situations, additional circuits or special programming may be required to prevent loss of data. Operation of the system can be summarized as follows:

- When even bank is addressed by CPU, odd bank is refreshed by address counter.
- Even bank is refreshed when CPU addresses the odd bank.
- A_0 increments the refresh counter before each odd-bank refresh.

7

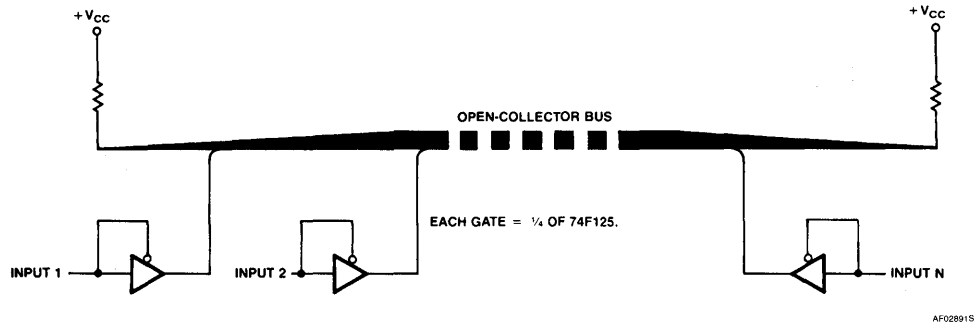


Figure 11. Reducing Leakage Current When Driving Open-Collector Buses

OPERATION & APPLICATIONS SUMMARY

The number of buffers (7406 type) that can share an open-collector bus is often limited by device leakage or by the increased power consumption caused by lowering the values of the pullup resistors. A method of reducing the leakage current is shown in the above example. Here, the logic input and output enable of each gate are tied together; thus, the gate output is floated High to drive the open-collector bus. Floating the gate outputs provides a significant reduction in leakage current which allows the use of more gates and/or reduced power consumption by the pullups.

SUMMARY

Many of the applications and concepts provided in this document were direct contributions or heavily influenced by entries in the Signetics' Interface Circuit Design contest. Our special thanks to those individuals whose entries are referenced in whole or in part.

As integrated circuits become more and more complex, fewer and fewer parts are required to implement a functional system; thus, interface support is a major consideration in the overall design process. To produce a competitive and cost effective product, the user must choose interface components that are efficient, reliable, and those that reflect the best features of current technologies. Signetics has met these challenges in the past and will continue to meet them in the future, providing silicon solutions that are truly state of the art — be it logic, memories, gate arrays, or other. For further documentation and/or applications assistance, call or write to your nearest Signetics Sales and Service Office — there is one near you.

AN206
Using μP I/O Ports With FAST Logic

Application Note

FAST Products

INTRODUCTION

Signetics interface ICs are most often used to implement input and output ports in microprocessor based systems. This application note illustrates the effective use of Signetics FAST devices to interface microprocessor data and address buses to general purpose I/O ports. Topics illustrated include handshaking, multiplexing, arbitration, and bit manipulating. More complex circuits involving memory interfacing, shared memory, and multiple processors are covered in other application notes.

Simple I/O Ports

The simple Input/Output ports shown in Figure 1 use 74F374 octal flip-flops and 74F244 octal 3-State buffers to interface to a microprocessor's data bus. The input port is enabled by $\overline{RD}$ AND $\overline{PORTSEL}$. The output is enabled by $\overline{WR}$ and $\overline{PORTSEL}$.

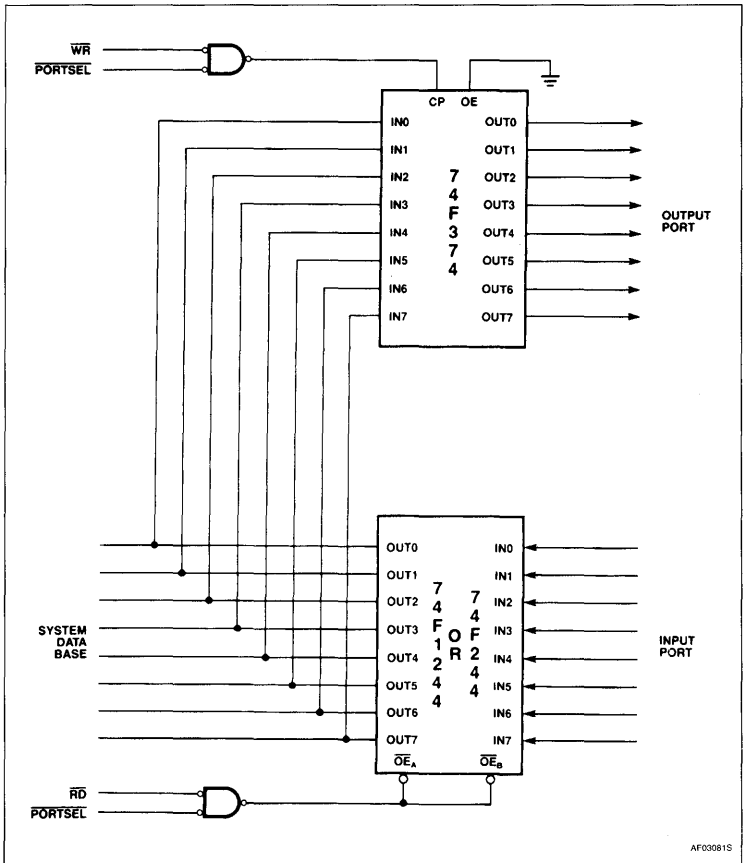


Figure 1. Simple Input/Output Ports Interface With Microprocessor Data Bus

When 16 pin packages are preferable to 20 pin packages for physical design considerations, 3-State multiplexers may be used as input ports. In Figure 2, 74F257 quad two-input multiplexers are used. A_0 selects between port A and port B.

In Figure 3, a 74F373 octal transparent latch is used to drive a light emitting diode annunciator array. The output follows the data bus while E is High, and the display freezes when E goes Low. The 20mA sink current of the 74F373 permits interface to most LED devices.

A potential hazard exists when using transparent latches as output ports. The timing diagram of Figure 4 shows that data may not be valid when E is brought High, causing invalid data to be present on the output for a brief period. This will not cause a problem when driving LEDs because the duration of the invalid data is too short to be seen. But, problems will occur if the outputs are used to trigger other circuits that cannot tolerate glitches. Flip-flops should be used instead of transparent latches when these conditions exist.

Interfacing microprocessors to slow peripherals, such as printers, usually requires handshaking logic. In Figure 5, the 74F374, 3-State octal flip-flop acts as an output port for the microprocessor and as an input port for peripheral. The microprocessor writes data to the output port which sets /data available Low. The peripheral then reads input port which sets /data accepted Low and /data available back to High. The Low /data accepted line interrupts microprocessor indicating that peripheral is ready for another data transfer.

Bit Manipulation

In Figure 6, the 74F251, 3-State 8 to 1 multiplexer provides a bit-oriented input port. This technique permits processors which do not have built-in bit manipulating capability to examine single bits at input ports efficiently. In addition, parallel inputs may be read bit-serially over a single data line. Address lines A_0, A_1, and A_2 select the bit to be read, and data bus line D_7 is selected to permit a simple software decision based on JUMP-ON-SIGN or SHIFT-LEFT & JUMP-ON-CARRY.

Using μP I/O Ports AN206

A versatile bit-oriented output port may be implemented with a 74F259, eight-bit addressable latch as shown in Figure 7. With this technique single output bits may be manipulated without maintaining a copy of the output port contents in memory. This is useful in bit-oriented control applications. The addressable latch effectively performs serial to parallel conversion on data supplied from the system bus. Data is written to 1 of 8 output bit locations specified by address lines A_0, A_1, and A_2.

Caution: Address inputs must be stable before latch is enabled or data can be entered into incorrect locations. If output glitches cannot be tolerated, data input must also be stable before the latch is enabled.

A similar technique is used in Figure 8, to accomplish bit manipulation without using the data bus. Each bit is associated with two addresses. If A_0 is High, the bit is set High; if A_0 is Low, the bit is set Low. With this approach bit-manipulation is faster and requires less program memory because data does not have to be loaded and output from the accumulator. Also PCB layout complexity is reduced by removing the data bus from the output port.

I/O Timing

In many applications it is necessary to adjust timing to match microprocessor specifications to bus specifications. For example, the MC6809 microprocessor has data write hold time of 30ns, making it difficult to interface to peripheral chips such as floppy disk controllers that have longer hold time requirements.

Figure 9 extends this hold time for interface to slow peripheral devices. A 74F373 3-State octal transparent latch is used to freeze data on I/O bus during write operations. During read operations, the 74F373 outputs are floated and data is read through the 74F244 3-State octal buffer.

Figure 10 shows the timing diagram for an I/O bus with extended hold time. During the write cycle, data is latched by 74F373 on the falling edge of E. Data remains on the outputs of the 74F373 until the rising edge of Q at the beginning of the next cycle, when the outputs are floated. The read cycle is unaffected. Data hold time is extended to ¼ cycle – from 30ns to 250ns for a 1MHz cycle rate. Note that a latch is used instead of a flip-flop to preserve the data setup time of the 6809.

A dedicated hardware solution is faster in systems requiring High throughput rates where the required function is performed frequently. In Figure 11, a 74F374 3-State octal flip-flop is used as both input and output port. By jumpering the output data lines of the 74F374 to different system data bus lines, various dedicated functions can be realized – examples are nibble swapping, bit transposing, and data encryption. The software to perform data manipulation is simple – data is written to the octal flip-flop, and manipulated data is read back into the processor using the following instructions: OUT (DATA MANIPULATOR), A IN A, (DATA MANIPULATOR)

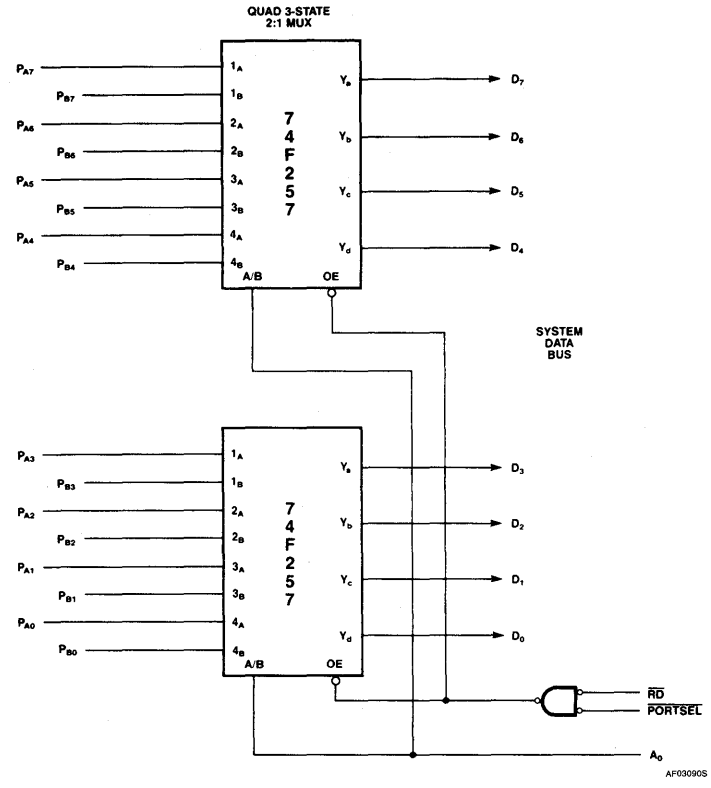


Figure 2. Use of 3-State Multiplexers As Input Ports

Using μP I/O Ports AN206

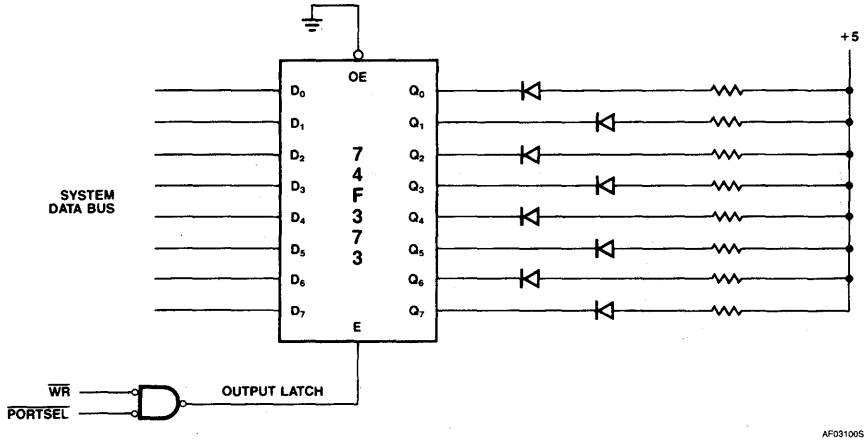


Figure 3. Output Port Driving LEDs Using 74F373 Octal Transparent Latch

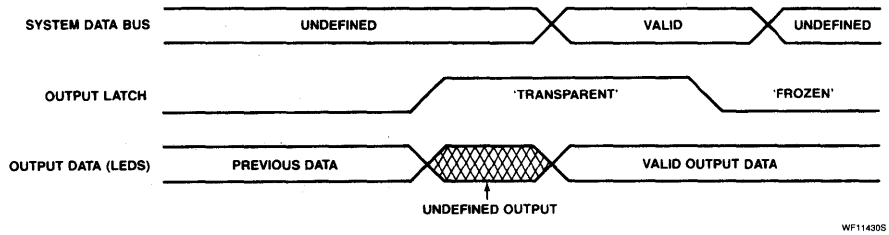


Figure 4. Potential Hazard Exists When Using Transparent Latch as Output Port

Using μP I/O Ports AN206

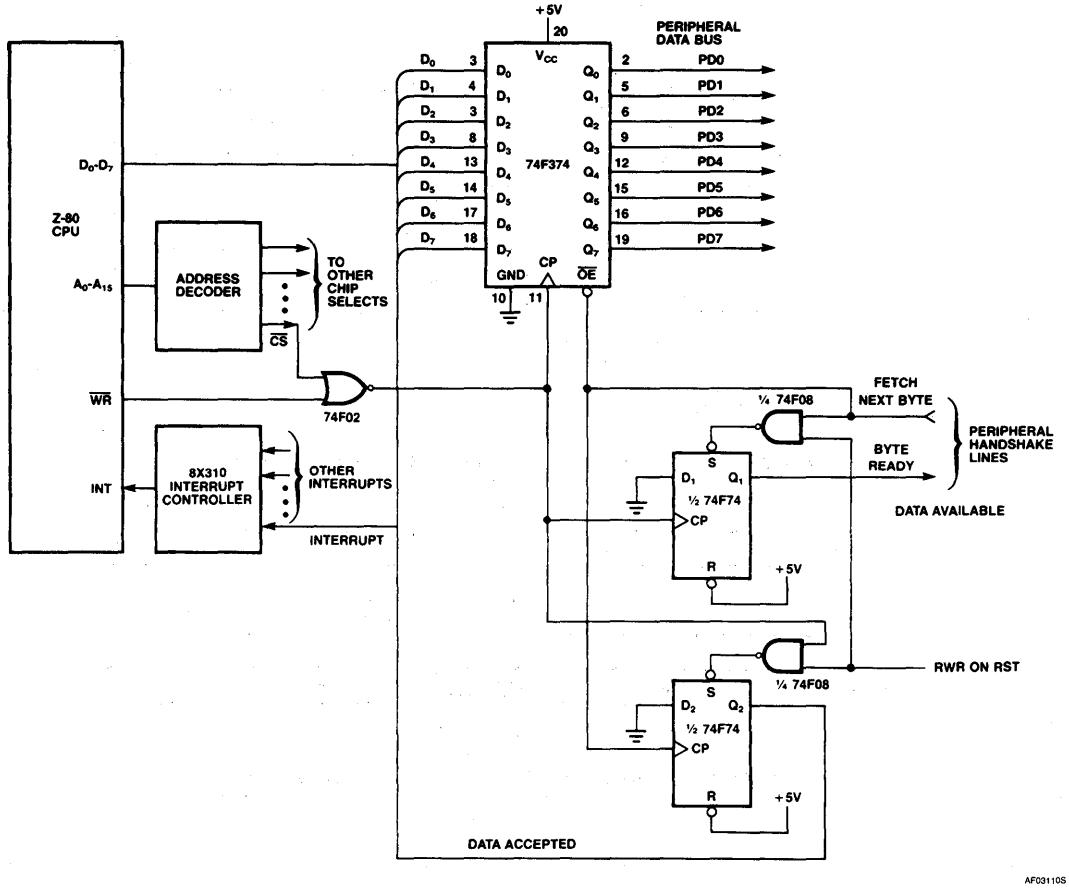


Figure 5. Interfacing Microprocessors to Slow Peripherals, Such as Printers, Using Handshaking Logic

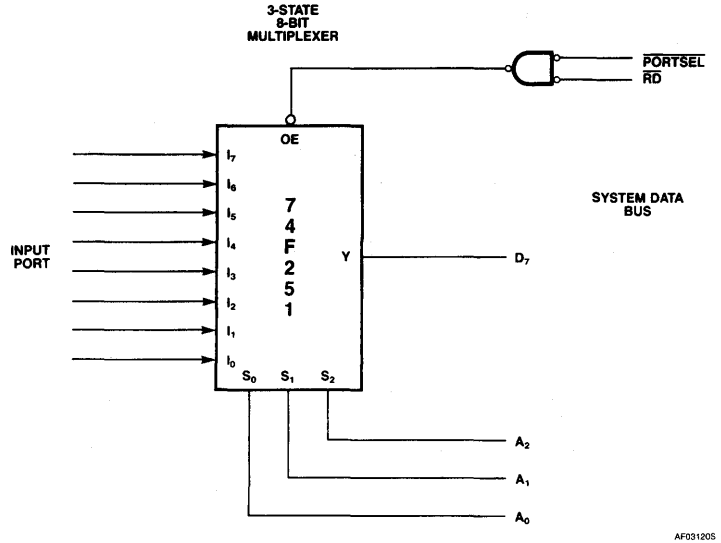


Figure 6. 3-State 8 to 1 Multiplexer Provides Versatile Bit-Oriented Input Port

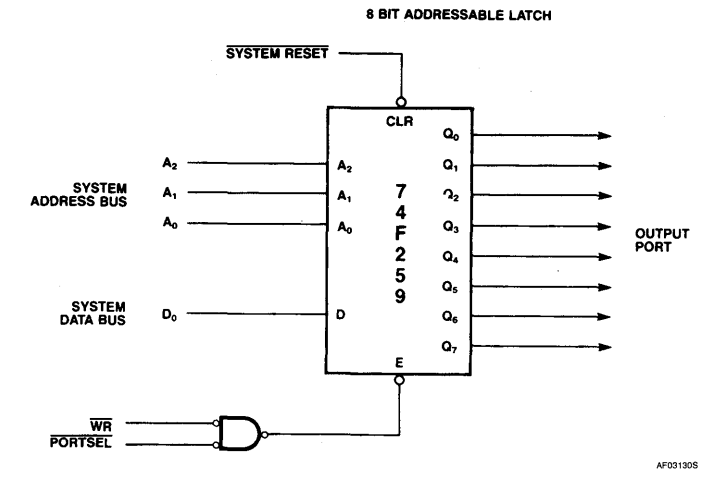


Figure 7. 8-Bit Addressable Latch Provides Versatile Bit-Oriented Output Port

7

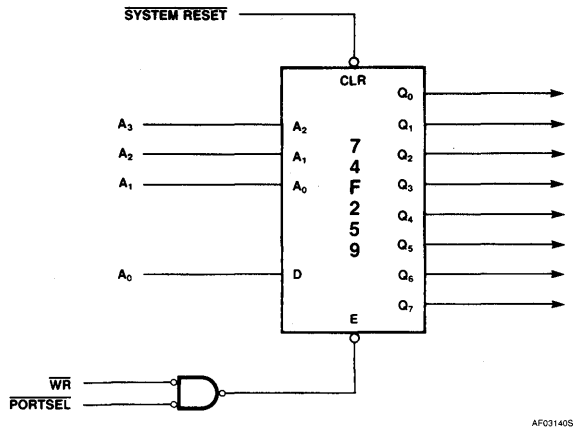


Figure 8. Bit Addressable Output Port Does Not Require Data Bus

Using μP I/O Ports AN206

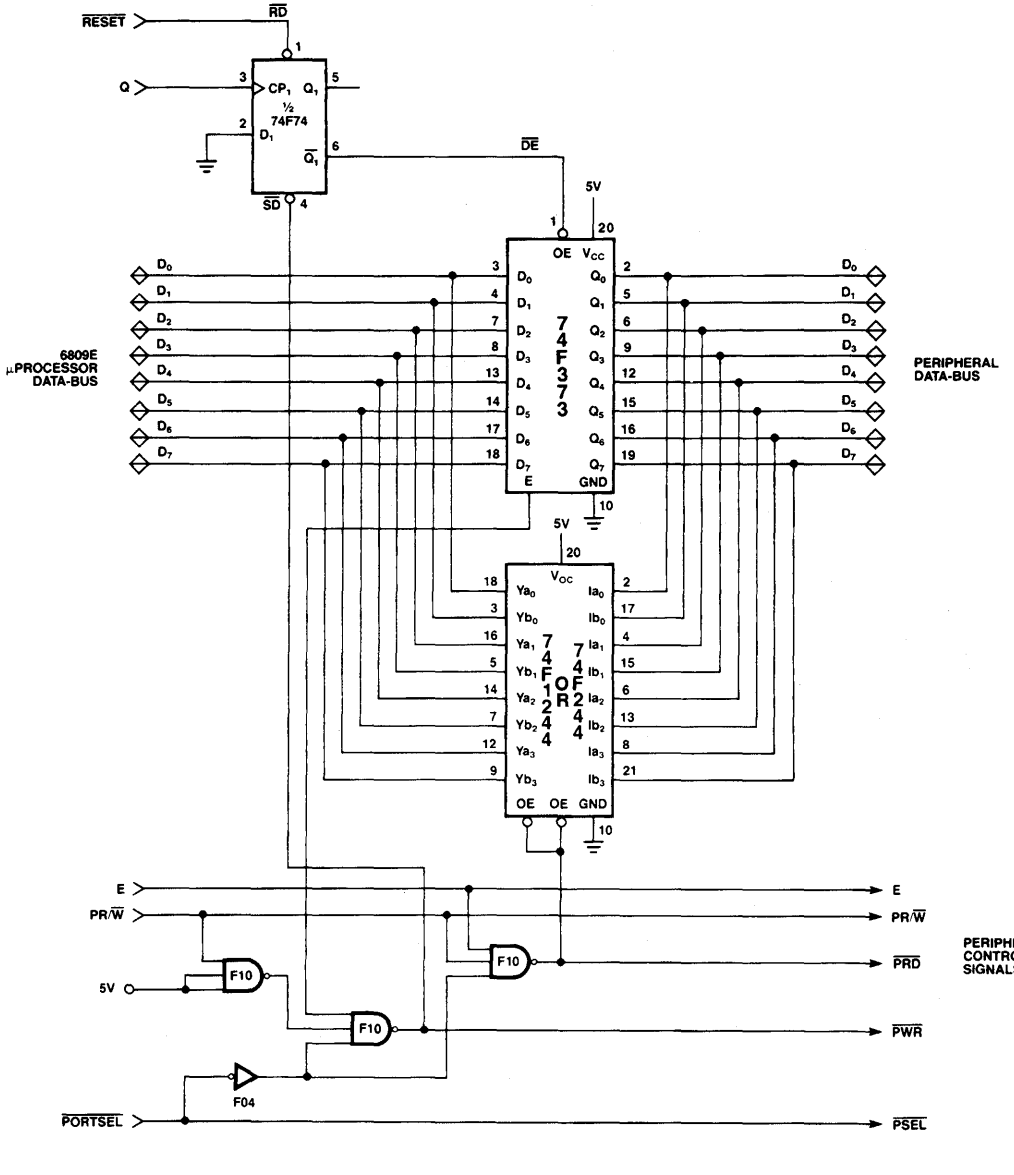
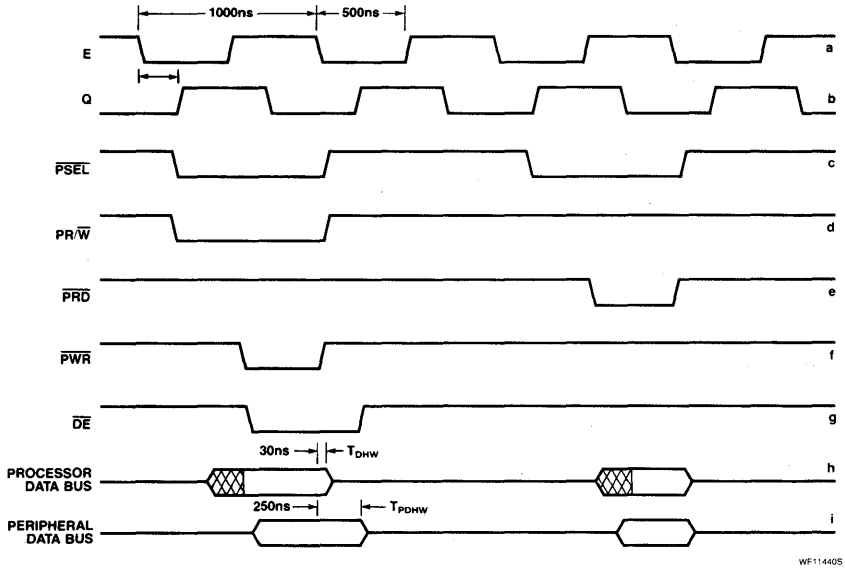


Figure 9. Hold Time Extended for Interface to Slow Peripheral With MC6809 Microprocessor



NOTES:
1. RESET -Power on reset
2. Q -6809E processor clock (1MHz shown)
3. O -Quadrature clock for 5809?
4. DE -Peripheral bus driver enable
5. PR/$\overline{W}$ -Peripheral READ/$\overline{WRITE}$
6. PSEL -Peripheral select
7. PRD -Peripheral read
8. PWR -Peripheral write
9. T_{DHW} -6809E output data hold time
10. T_{PDHW} -Peripheral write data hold time

Figure 10. Timing Diagram for I/O Bus With Extended Hold Time

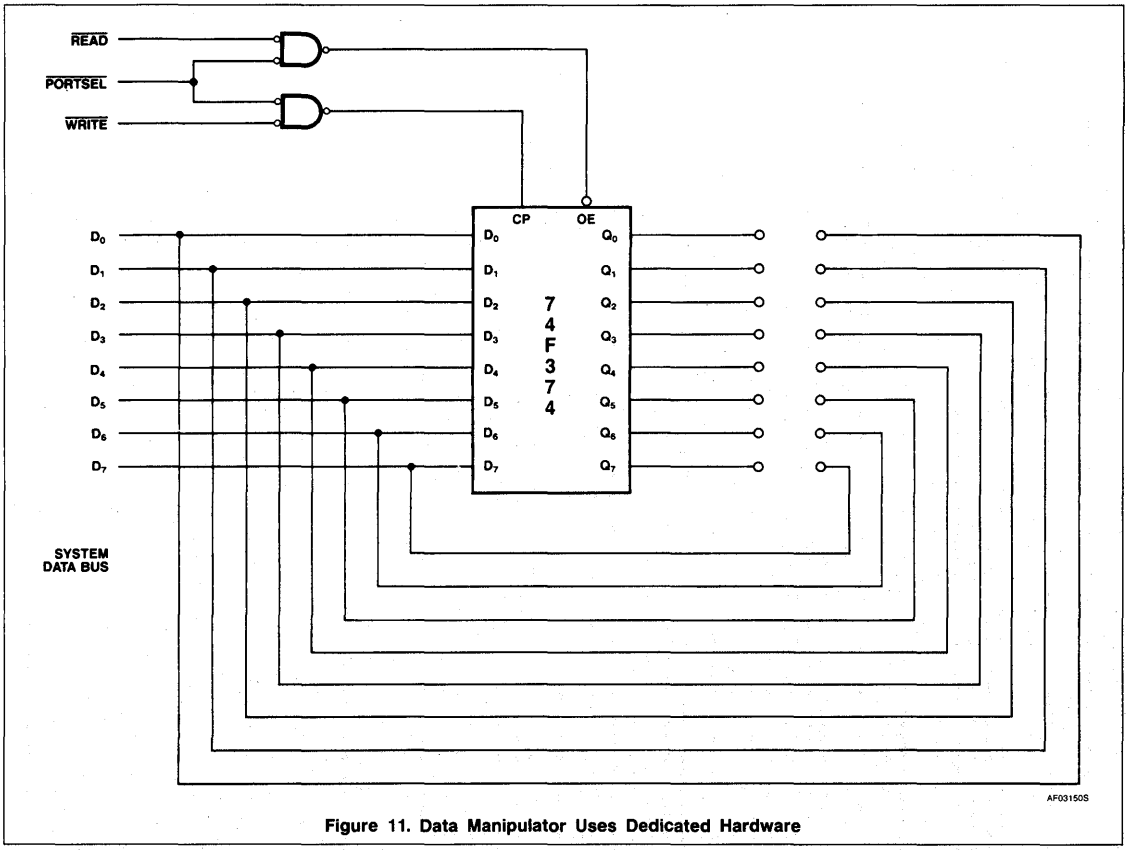


Figure 11. Data Manipulator Uses Dedicated Hardware

BIBLIOGRAPHY

Many of the applications illustrated in this note were contributed or influenced by entries in Signetics' Interface Circuit design contest. Special thanks are due to the following individuals whose entries were referenced in whole or in part in this note:
V.K. Agrawal
Timothy Anderson
Wiley M. Bird
James A. Ciarpella
Mark Forbes
Loren H. Johnson
Prakash R. Kollaram
G.B. Livingston
Joseph Mastroieni
Jonathan A. Titus
Eugene M. Zumchak

Signetics

AN207
Multiple μP Interfacing With FAST ICs

Application Note

Logic Products

INTRODUCTION

As microprocessor costs continue to decrease and the demands on product performance continue to increase, designers are increasingly turning to multiple microprocessor systems to meet the performance challenge. The introduction of many "peripheral controller" type processors has made this choice even more attractive. This application note addresses typical problems associated with interfacing multiple microprocessors, and illustrates the use of Signetics Interface Circuits in solving these problems.

A multi-processor system contains two or more processors communicating through parallel ports, multi-port memories, serial data links, and/or shared buses. The most popular multi-processor architectures are "loosely coupled" systems. In loosely coupled systems each processor operates asynchronously with the other processors, usually performing a separate function. Communication is not continuous, and occurs only when necessary.

A special application for multiple microprocessor systems is in redundant systems. As the price of microprocessors dropped, it became economically feasible to achieve greatly increased reliability by employing several processors operating in parallel, performing identical functions. After each operation a vote is taken on the result. If there is disagreement, a fault has been detected, and appropriate corrective action can be taken. Appropriate action might be switching in a third processor, repeating the process, or activating an error sequence and/or an alarm.

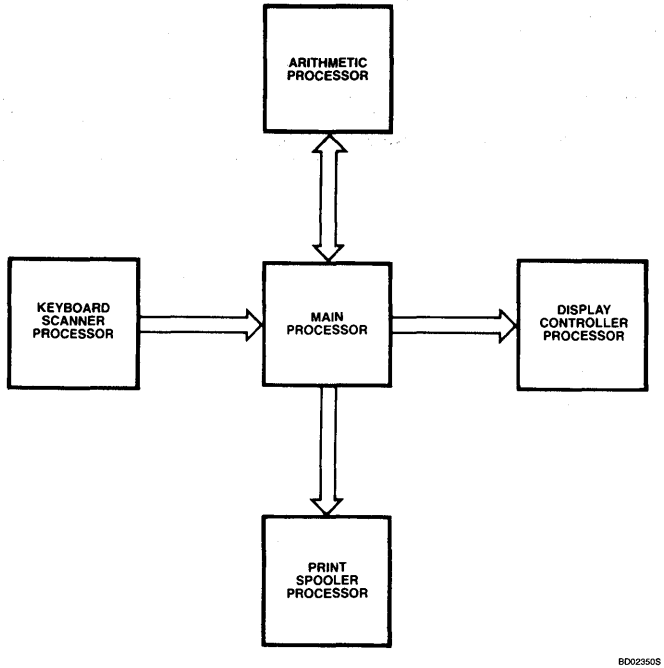


Figure 1. Typical Multi-processor System

In the typical loosely coupled multiple processor system of Figure 1, a main processor "delegates" processing work to four other processors. A keyboard scanner microprocessor scans the keyboard continuously, debounces key closures, performs code conversions, and transmits key codes to the main processor in a format that it can easily assimilate. A separate arithmetic processor accepts parameters from the main processor, performs arithmetic calculations, and provides the results for the main processor to read when it is not busy with other tasks. The display controller accepts data and commands from the main processor, then displays and manipulates data on CRT or other displays. The display controller refreshes the display and supports graphic displays without tying up the main processor. The print spooler is a separate processor that accepts files to be printed from the main processor using high-speed data transfers. Then the print spooler stores and feeds data to the printer at the printer's lower data rate, freeing the main processor for other chores. Each processor module contains its own "local" ROM, RAM, or I/O, so that it performs its task independently, and communicates with other processors only when necessary. As a result, the system as a whole operates closer to its maximum speed.

Some of the advantages of multiple microprocessor systems are:

- Each processor performs a relatively independent task.
  - Design is easily split among team members.
  - Testing is easily performed on a modular level.
  - Modules can be added or modified without affecting other modules.
- Multi-processing allows distributed processing where modules may be physically separated from the main system.

Multiple μP Interfacing With FAST ICs AN207

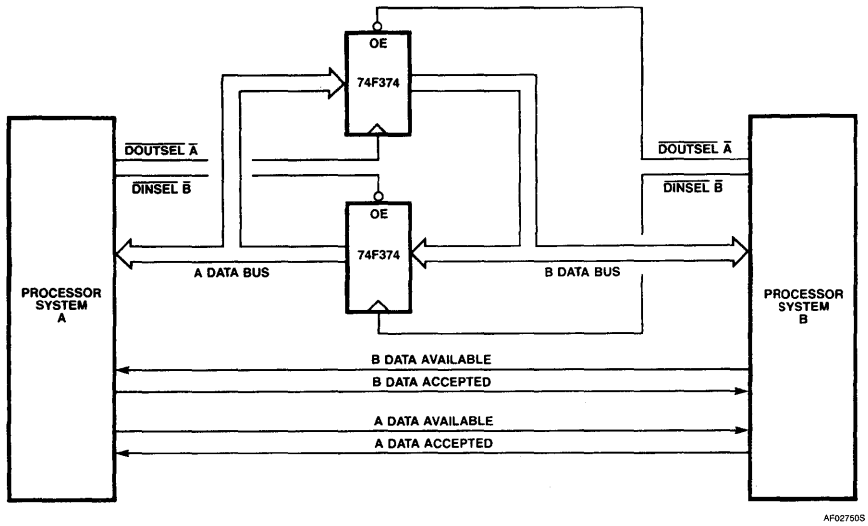


Figure 2. Basic Inter-processor Communication Using Parallel I/O Ports

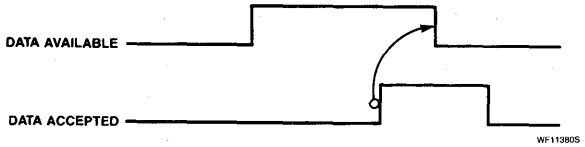


Figure 3. Handshake For Parallel Port Communication

- Parallel processing greatly increases system performance and throughput.
- Hardware cost is less than single-processor systems with similar performance.
- Reliability can be increased easily by redundant processing.

The following application examples illustrate the use of Signetics FAST Interface Circuits in multiple processor systems.

PARALLEL I/O PORT COMMUNICATIONS

Figure 2 shows how parallel I/O ports using Signetics FAST Interface devices are used to accomplish simple 2-processor communications. Two 74F374 octal 3-State registers are used to implement bi-directional parallel data communication. Each 74F374 acts as output port to one processor and input port to the other. The handshake lines are needed when the processors operate asynchronously to ensure that data has been received before new data is transmitted. A handshake timing protocol (Figure 3) implemented in software acts as a traffic cop to assure valid data communications. The transmitting processor starts the handshake by setting Data Available to indicate that data is valid. The receiving processor sets Data Accepted to indicate data has been read. The transmitter then resets Data Available allowing the receiver to reset Data Accepted. The transmitter will not send new data until Data Accepted is reset.

COMMUNICATIONS VIA MULTI-PORT MEMORY

Figure 4 shows the logic required for two processors to communicate through a multi-port memory. The RAM is accessible from both processor A and processor B via 74F157 multiplexers used to select one processor's bus at a time. Multi-byte messages and data blocks may be written into the memory by one processor and read out by the other at a later time. No byte-by-byte handshake is required. The multi-port memory provides increased system performance at somewhat higher cost compared to a parallel port technique. Because of the use of multi-port memories in microprocessor systems, these systems can become quite complex. Another application note in this series covers interfacing to multi-port memories in greater depth.

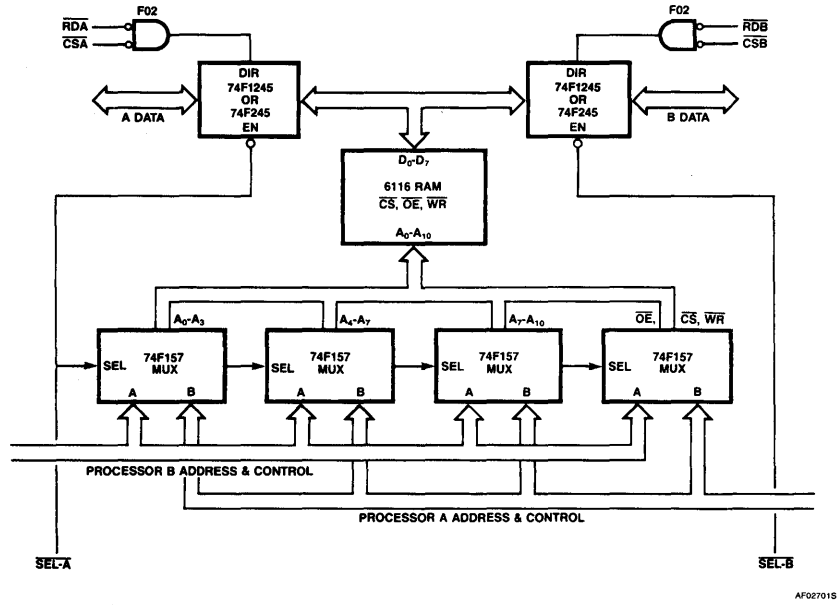


Figure 4. Multiport Memory Provides High-performance Multi-processor Communications

SERIAL COMMUNICATIONS

Although serial communications between multiple processors is slower than the parallel methods examined above, it is usually less expensive and very useful for communicating with remote units. Serial communications via RS-232 or RS-422 links can provide reliable communications over great distances. Implementation of serial communications is simplified by the availability of Universal Asynchronous Receiver Transmitter (UART) devices and well established standards for circuit interfaces and protocols. Figure 5 shows local/remote processor communication using Signetics SC2681 UART devices. In many cases additional interface lines are required for handshaking.

SHARED BUS ARCHITECTURE

One of the most powerful multiple processor architectures uses the popular shared bus concept. In Figure 6, each processor has its own local bus with some combination of RAM, ROM, and I/O available locally. The shared bus permits use of "global resources" such as global memory and global I/O which are accessible to all processors on the shared bus. Common interfaces such as printer ports do not have to be implemented for each processor, and may be connected to the shared bus. Multiple processors communicate indirectly with one another through the global RAM. This technique provides highest throughput when interconnecting more than two processors. It also reduces cost through sharing of global resources.

Any processor permitted to drive the system address, data, and control buses is known as a "master." Processors not having this capability are "slaves." A useful attribute of shared bus systems is the ability to add whole new functions by connecting a new master to the bus. Figure 7 shows a typical shared system bus interface using Signetics Interface circuits. Three 74F244 octal 3-State buffers are used to drive the 24 bit system address bus (16 bits in some cases). Two 74F245 octal bidirectional 3-State buffers are used to drive the 16 bit data bus (8 bits in some cases). In addition, half a 74F244 is used to drive the system command bus, composed of the signals $\overline{IORD}$, $\overline{IOWR}$, $\overline{MEMRD}$, and $\overline{MEMWR}$.

Multiple local processors may request use of the shared bus by setting $\overline{BUS\ REQUEST}$ active and waiting for the arbitration logic to assert $\overline{BUS\ GRANT}$. The arbitration logic indicates to the local processor when it may access the shared bus after a request has been made. This is necessary to prevent more than one local processor from accessing the system bus at the same time, resulting in bus contention and possible system failure.

ARBITRATION

Contention by several processors for use of shared resources can create sticky timing problems unless care is exercised in the design of appropriate arbitration logic to resolve timing conflicts. Schemes for bus arbitration vary in speed, cost, and flexibility and involve parallel, serial, transparent, pseudo-transparent, polled, and flag operations.

Parallel Priority Resolution

Parallel priority resolution is most useful in systems with 4 or more masters, where its speed outweighs the disadvantage of the additional hardware. A scheme for system bus arbitration using parallel priority resolution is shown in Figure 8.

A master's priority is determined by using a 74F148 priority encoder. Each master's arbitration logic generates a $\overline{REQ}$ to the priority encoder. When there is contention, the master whose $\overline{REQ}$ is connected to the highest priority input will be granted access.

A 74F138 is used to decode the encoder outputs to generate the $\overline{EI}$ (enable input) to the arbitration logic of the master which has been granted access. $\overline{CLEAR}$ is used to remove all masters from the bus during reset or when an error condition is present. $\overline{ARB\ CLOCK}$ is used to synchronize all bus arbitration inputs and outputs to prevent race conditions and to facilitate a standard interface

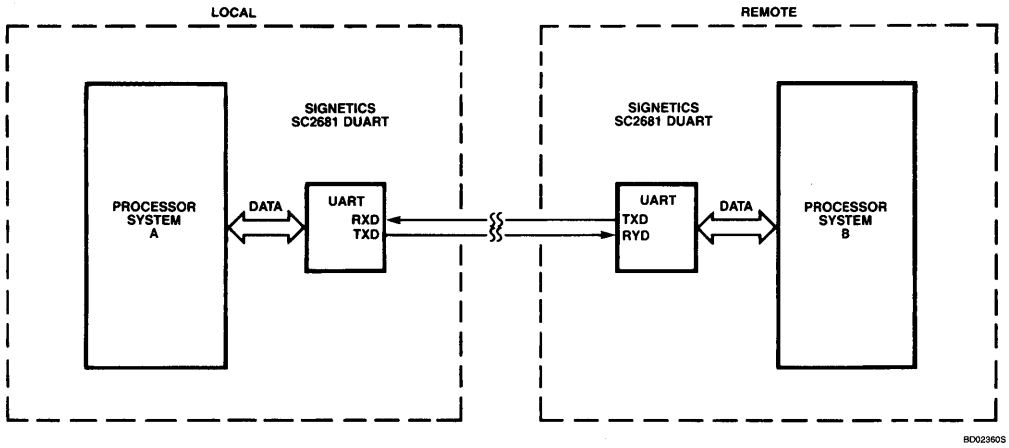


Figure 5. Serial Communications Link Provides Economical Inter-processor Communications

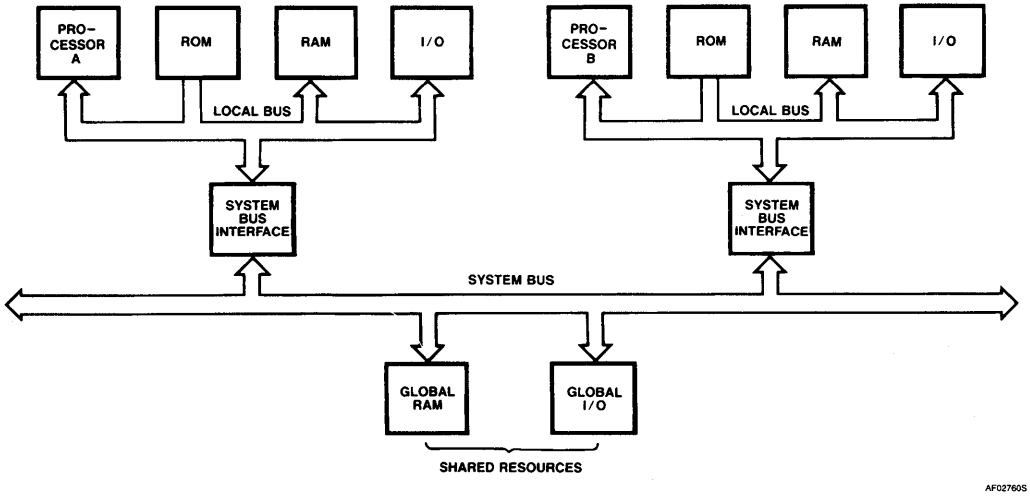


Figure 6. Shared Bus Provides Most Powerful Multiple Processor Architecture

7

Multiple μP Interfacing With FAST ICs AN207

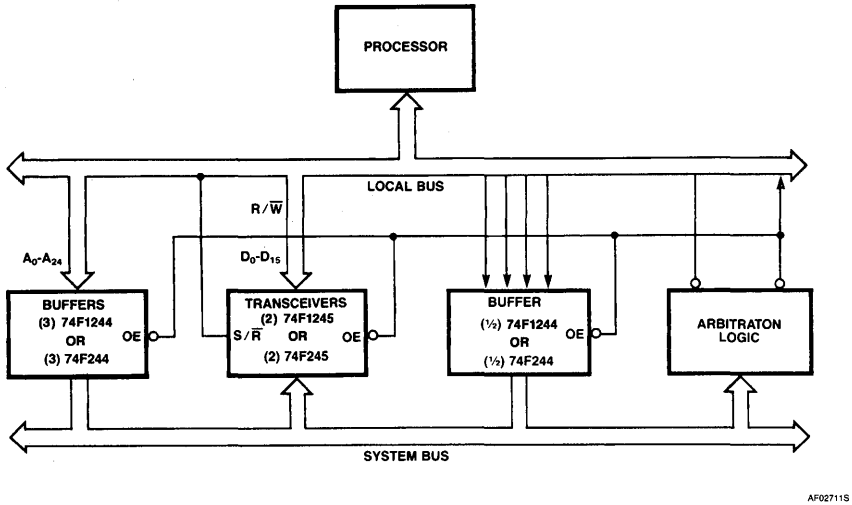


Figure 7. Typical System Bus Interface

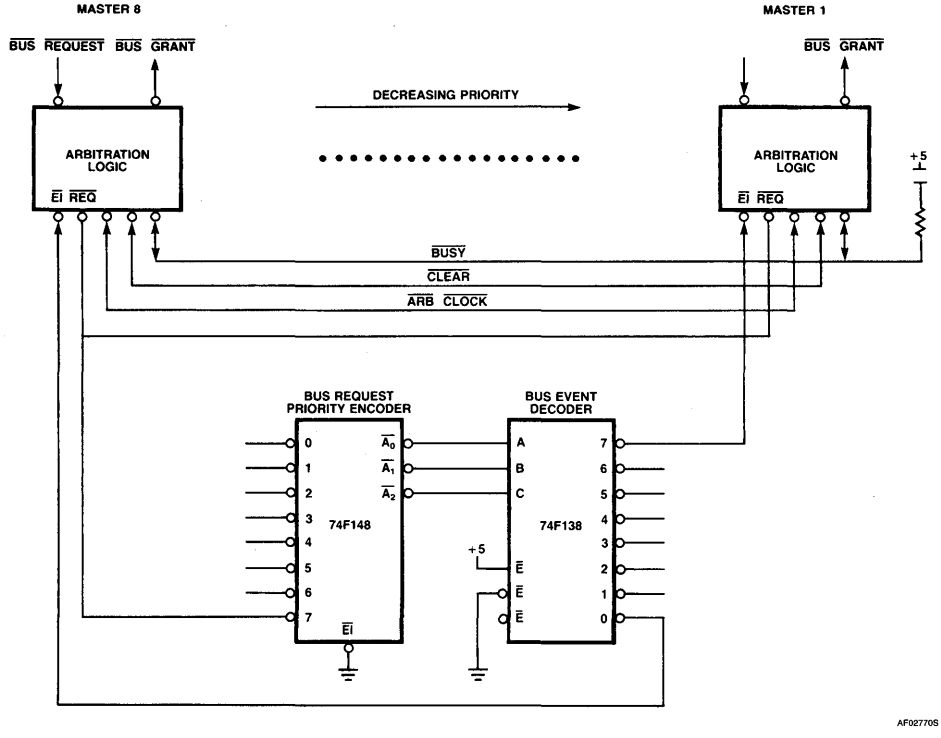


Figure 8. System Bus Arbitration Using Parallel Priority Resolution

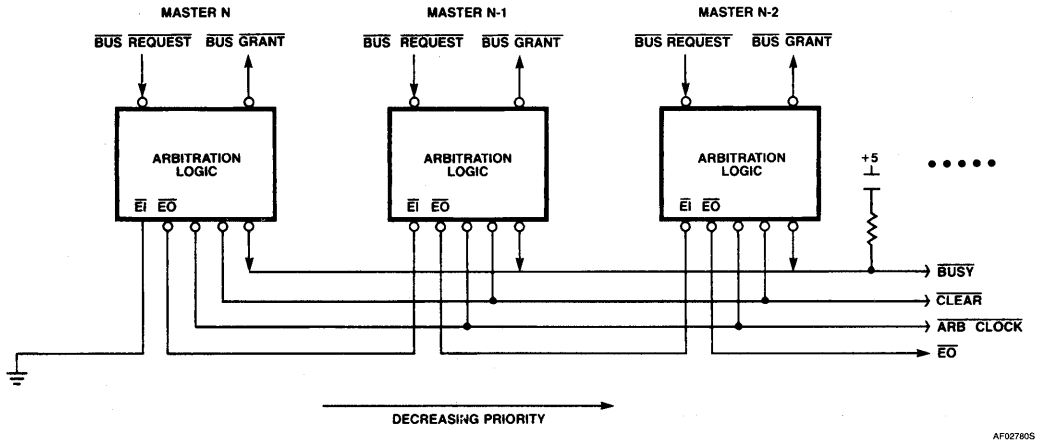


Figure 9. System Bus Arbitration Using Serial Priority Resolution

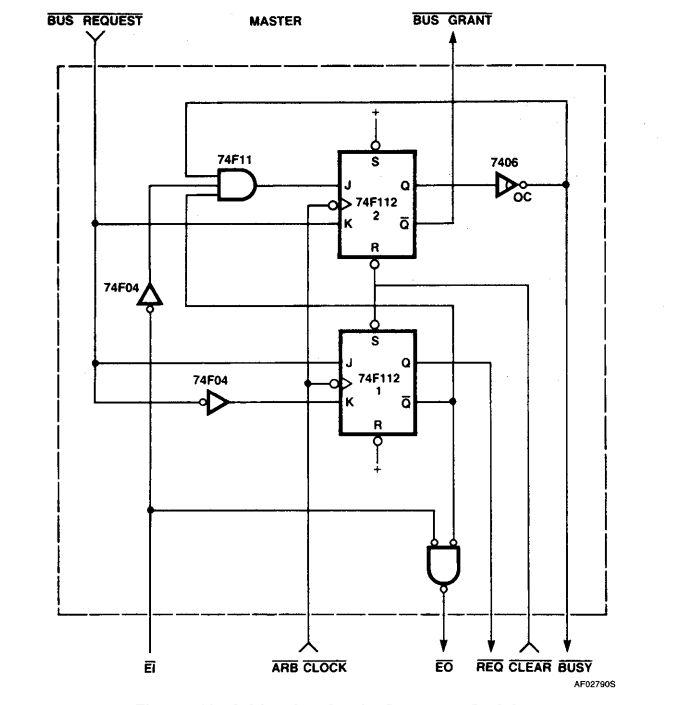


Figure 10. Arbitration Logic Supports Serial Or Parallel Priority Resolution Techniques

design. $\overline{BUSY}$ is generated by the master currently accessing the bus to indicate that the bus is in use. Even after a master has been granted access by the priority resolution, it must still wait for the current master to vacate the bus, i.e., $\overline{BUSY}$ going inactive. The arbitration logic generates a $\overline{BUS\ GRANT}$ to a master when $\overline{EI}$ is asserted and $\overline{BUSY}$ is not.

Serial Priority Resolution

Serial priority resolution eliminates the need for encoder/decoder hardware at the expense of speed. In Figure 9 a master's priority is determined by its physical location in a daisy chain configuration. A master negates its $\overline{EO}$ (enable output) when its $\overline{EI}$ (enable input) is negated or when it wants to access the bus. This negates $\overline{EO}$ for all masters further down the line *to go inactive*. If a master requests the bus, and no higher priority master is requesting the bus, as indicated by $\overline{EI}$ being asserted, the master may access the bus when the current master is finished. The ARB clock rate is limited to the speed at which the daisy chain signals can propagate through all masters.

Arbitration Logic

Arbitration logic suitable for either parallel or serial priority resolution is shown in Figure 10. The logic shown synchronizes a master's $\overline{BUS\ REQUEST}$ input to $\overline{ARB\ CLOCK}$ using flip-flop 1, asserting $\overline{REQ}$ and negating $\overline{EO}$. If $\overline{EI}$ is asserted and $\overline{BUSY}$ is not, the master may access the bus on the next falling edge of $\overline{ARB\ CLOCK}$. This arbitration is provided by flip-flop 2. $\overline{BUS\ GRANT}$ and $\overline{BUSY}$ are asserted. When the access is complete, the master negates $\overline{BUS\ REQUEST}$ inactive. On the falling edge of $\overline{ARB\ CLOCK}$, $\overline{REQ}$ negated and, if $\overline{EI}$ is asserted $\overline{EO}$ is asserted. On the next falling edge $\overline{BUSY}$ and $\overline{BUS\ GRANT}$ are negated. The timing diagram for this sequence is shown in Figure 11. Note that a master must wait for the current master to complete a transfer and negate $\overline{BUSY}$ before it may access the bus.

7

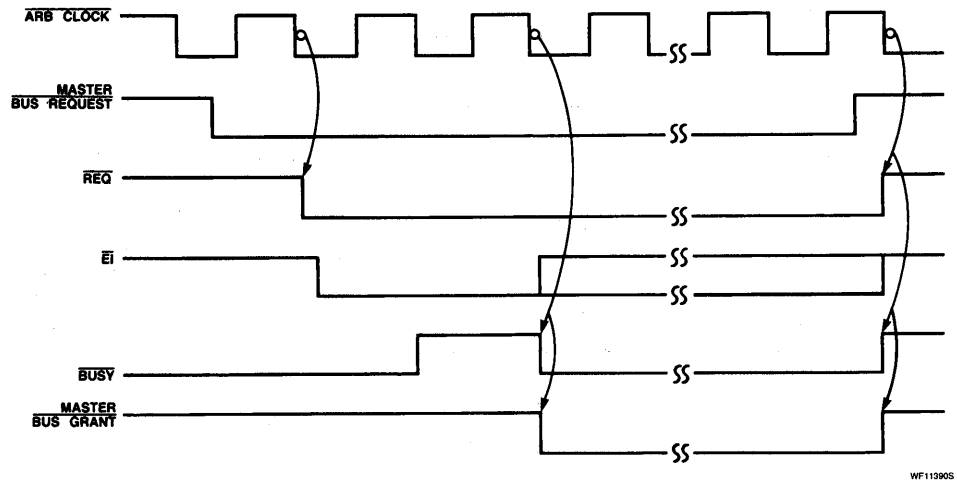


Figure 11. Timing Diagram For Arbitration Logic

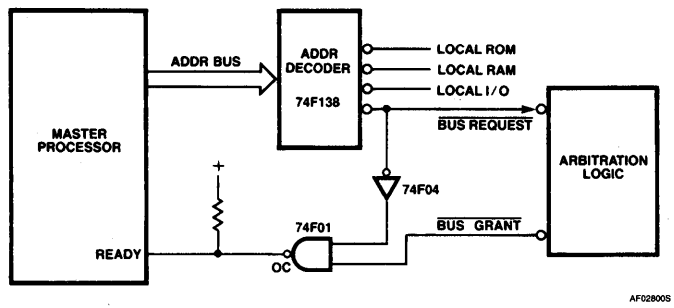


Figure 12. Pseudo-transparent Access To Shared Bus

Multiple μP Interfacing With FAST ICs AN207

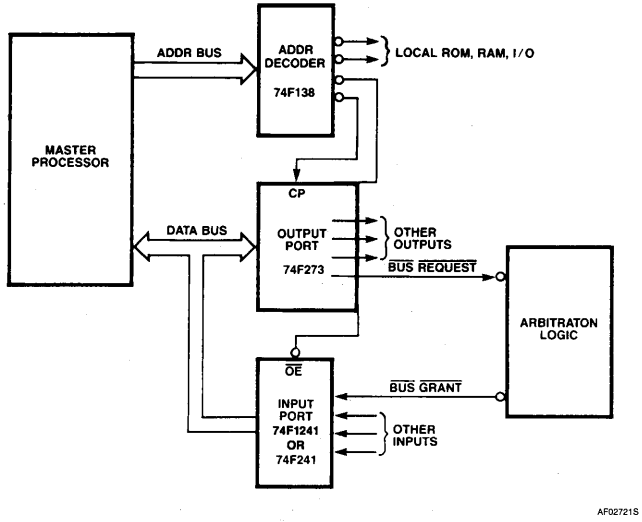


Figure 13. Polled Access To Shared Bus

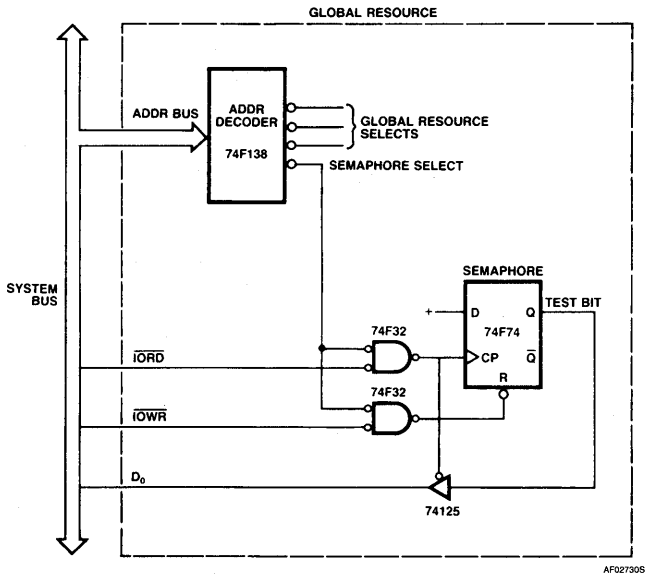


Figure 14. Semaphore (Flag) Register Permits Access To Shared Resource Without Monopolizing Shared Bus

Pseudo-Transparent Priority Resolution

The logic of Figure 12 uses "cycle stealing" to permit single byte transfers with pseudo-transparent arbitration. When the address decoder determines that a master requires access to shared bus, it asserts $\overline{\text{BUS REQUEST}}$. The processor's READY line is held negated, "freezing" the processor until the arbitration logic asserts $\overline{\text{BUS GRANT}}$. Then READY is asserted and the shared bus cycle occurs. The processor is unaware of arbitration and unaware that the bus is shared. With this technique, a watchdog timer should be used to ensure that the processor doesn't "hang up" if faulty bus operation prevents access. Access occurs one cycle at a time, preventing any one master from "hogging" the bus.

Polled Access to Shared Bus

The logic in Figure 13 uses an output port to request access to the bus, and polls an input port to determine when access has been granted. Once access is granted, the master retains the bus until it negates the $\overline{\text{BUS REQUEST}}$ output port bit. Large block moves may occur without fear of another master changing the data as with cycle-by-cycle arbitration. However, this approach greatly slows down the response time of the system, because of the waiting while each master performs. All other masters must wait, even if they do not require the use of the same shared resource.

Semaphore (Flag) Arbitration

The logic of Figure 14 improves on the polled access technique by permitting access to a shared resource when that resource is available. A master first reads the semaphore register associated with the resource it wishes to access. The master may not access the resource unless the semaphore bit is false. When the semaphore bit is false, reading the register automatically sets the bit true. When the master reads a false semaphore, it may then access the resource. All other masters reading the semaphore will see it set and will not access the resource. The master may access the resource until it is no longer needed. By writing to the semaphore register, it is automatically reset, allowing other masters to access the resource. Only the one resource, not the entire shared bus, is monopolized by one master at a time. The hardware performs a function similar to a software read-modify-write operation.

The timing for the semaphore operation is shown in Figure 15. If the semaphore bit is false and the register is read, the bit is set true at the end of the read cycle (rising edge of $\overline{\text{IORD}}$). The semaphore bit is reset by doing a "dummy" write to the semaphore register. The bit is set false at the beginning of the cycle ($\overline{\text{IOWR}}$ going low).

INTERFACING THE MC68000 TO THE MULTIBUS™*

One of the best examples of a multi-processor shared bus is the MULTIBUS. One of the

*MULTIBUS is a trademark of Intel Corporation.

Multiple μP Interfacing With FAST ICs AN207

most popular 16 bit processors in new designs today is the MC68000. Yet, to our knowledge, there are currently (mid-83) no LSI MULTIBUS arbiter ICs available to allow a designer to easily interface the two. There are arbiter ICs available, but they were designed for other processors and are cumbersome and limited in performance when interfaced to the 68000.

The following is the design for a 68000 MULTIBUS interface. The design supports serial or parallel arbitration and performs with a 10MHz bus clock. Operation is similar to the example described previously. Tables 1 and 2 define the MC68000 bus control signals and the MULTIBUS arbitration signals. The timing diagram for MC68000 read and write cycles is shown in Figure 16.

Figure 17 shows the control circuitry for the MC68000 to MULTIBUS interface. The master initiates a MULTIBUS transfer by asserting $\overline{\text{MULTIREQ}}$ active. This is usually the output of address decode circuitry. $\overline{\text{AS}}$ clears the request at the end of the transfer. Flip-flops 1, 2, and 3 sample and synchronize the bus request to the falling edge of $\overline{\text{BCLK}}$. Since $\overline{\text{MULTIREQ}}$ is asynchronous to $\overline{\text{BCLK}}$, flip-flop 2 serves as a synchronizer and is clocked on the rising edge of $\overline{\text{BCLK}}$. All inputs to the arbiter are thus synchronous so that race conditions at flip-flop inputs are avoided.

If the bus is not in use ($\overline{\text{BUSY}}$ is not asserted), and no higher priority master requests the bus ($\overline{\text{BRPN}}$ is asserted), the master is granted access on the next falling edge of $\overline{\text{BCLK}}$. Flip-flop 4 provides this function. If these conditions are not satisfied, $\overline{\text{DTACK}}$ is used to force the CPU to wait. Once the master is granted access, it sets $\overline{\text{BUSY}}$ active to indicate that the bus is in use. $\overline{\text{BUSEN}}$ (bus enable) also becomes active and gates the master's address, data, and control buses onto the MULTIBUS. One half cycle later, on the rising edge of $\overline{\text{BCLK}}$, flip-flop 5 sets CMDEN (Command Enable) active. This allows RD or WR strobes to be asserted on the MULTIBUS. This delay is necessary because the MULTIBUS requires data and address valid 50ns before read or write commands. DS is used to generate the read or write strobes.

The MULTIBUS transfer is completed when $\overline{\text{XACK}}$ is asserted terminating the 68000 cycle by asserting $\overline{\text{DTACK}}$. The master maintains control of the MULTIBUS until another master requests access, as indicated by asserted $\overline{\text{CBRQ}}$. If the current master is not performing a MULTIBUS transfer, it loses the bus on the next falling edge of $\overline{\text{BCLK}}$. CMDEN, $\overline{\text{BUSEN}}$, and $\overline{\text{BUSY}}$ are negated. Flip-flop 4 provides this function.

Table 1. MC68000 Bus Control Signals. (Refer To The Signetics 68000 Microprocessor Data Sheet For More Information.)

CLK	Clock. Time reference for 68000 microprocessor bus control.
$\overline{\text{AS}}$	Address Strobe. Indicates that address on address bus is valid.
$\overline{\text{UDS}}$, $\overline{\text{LDS}}$	Upper and Lower Data Strobe. Indicates that the processor is reading from or writing to the upper data byte ($D_7 - D_{15}$) and/or the lower data byte ($D_0 - D_7$).
R/$\overline{\text{W}}$	Read/Write. Indicates whether the current bus cycle is a read or a write cycle.
$\overline{\text{DTAK}}$	Data Transfer Acknowledge. Input to the 68000 indicating that the data transfer can be completed, on the high to low transition.
$\overline{\text{BCLK}}$	Bus Clock. All arbitration signals listed below must be synchronized to the negative edge of this clock. It is independent of any processor clock.
$\overline{\text{BPRN}}$	Bus Priority In. Indicates that no higher priority master is requesting the bus. Similar to $\overline{\text{EI}}$ in previous examples.
$\overline{\text{BPRO}}$	Bus Priority Out. Used in serial priority resolution circuits. Similar to $\overline{\text{EO}}$ in previous examples.
$\overline{\text{BUSY}}$	Bus Busy. Driven by current bus master to indicate that the bus is in use.
$\overline{\text{BREQ}}$	Bus Request. Used in parallel priority resolution circuits. Similar to $\overline{\text{REQ}}$ in previous examples.
$\overline{\text{CBRQ}}$	Common Bus Request. Driven by all potential bus masters requesting bus. Used to save time by allowing the present bus master to avoid arbitration after each cycle if no other requests are active.
$\overline{\text{XACK}}$	Transfer Acknowledge. Indicates that the MULTIBUS data transfer is completed on high to low transition.

The logic that interfaces the MC68000 to the MULTIBUS is shown in Figure 18. 74F533 inverting octal 3-State latches are used to gate the 20 bit address and 16 bits of data onto the MULTIBUS. Note that the data and address bus is negative true. 74F240 octal 3-State inverting buffers are used to gate 16 bits of data onto and off of the MULTIBUS. Data direction is determined by the MC68000's R/W line. A 74F139, 2 to 4 decoder is used to decode I/O and RD/WR to generate the 4 MULTIBUS commands. I/O is the output of address decode circuitry which decodes I/O addresses. A 74F244 is used to gate the commands onto the MULTIBUS.

Signetics FAST logic family is used in this design to increase speed and bus drive capability while minimizing MULTIBUS loading.

REDUNDANT MICROPROCESSORS ENHANCE RELIABILITY

Figure 19 shows how two 6809E microprocessors are used in a parallel redundancy scheme to prevent faulty operation from damaging external systems. Two systems with identical processors, RAM, ROM, and I/O are first synchronized. After synchronization, their data buses are compared every cycle. If the data on the two buses is different, an error has occurred and the system shuts down.

A common clock is used to drive the 6809E processor in each system so that a timing reference is established. Upon reset, both processors execute a sync instruction and the critical output circuits are turned off. When both processors have executed the sync instruction, as indicated by BA = 0 and BS = 1, the START button is used to interrupt the processors and they begin program execution in synchronism. The critical outputs are also turned on. On the falling edge of E, the data buses of the two systems are compared using the 74F521 octal comparator. If the data does not match, at least one system is operating incorrectly. The 74F74 flip-flop latches the error condition and turns off the critical outputs.

A similar technique should be used on outputs to ensure that an output goes active only when the output of both systems goes active.

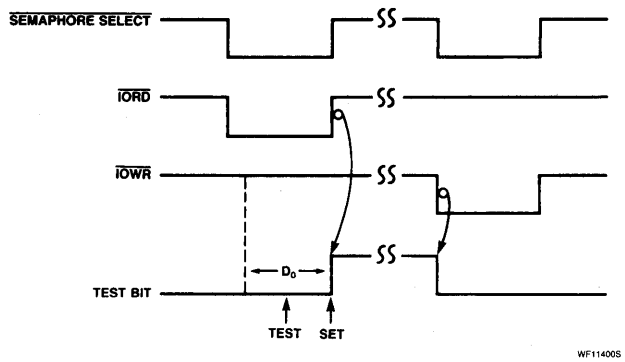


Figure 15. Timing Diagram For Semaphore Operation

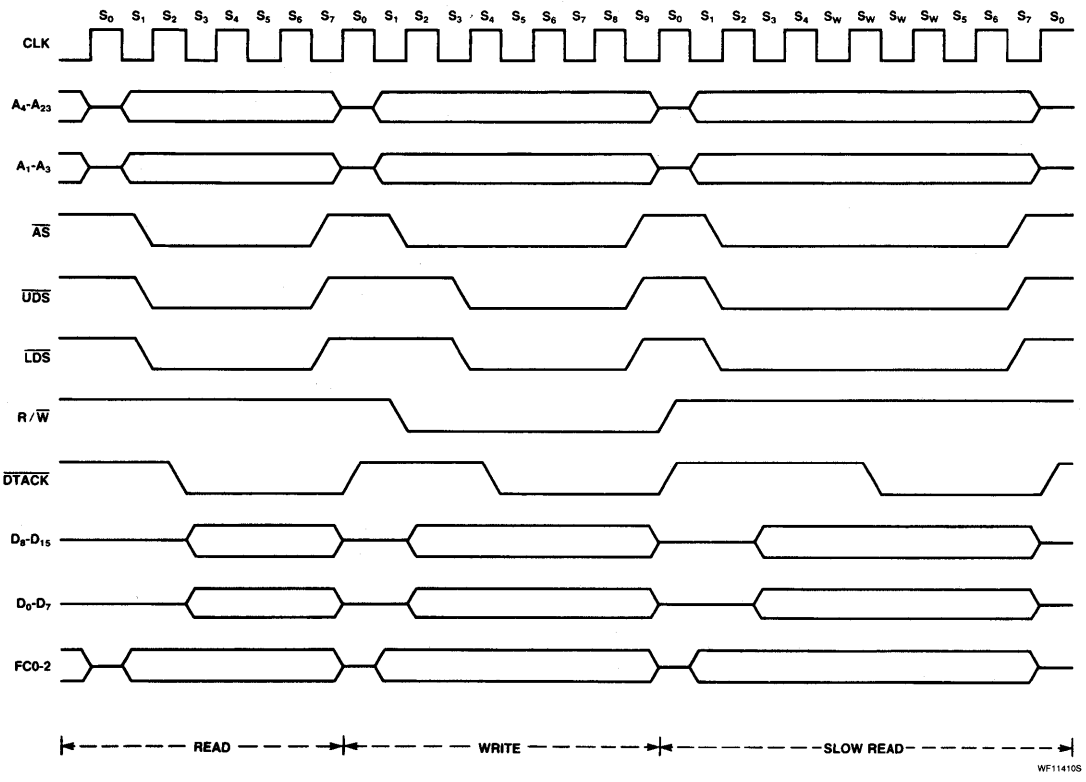


Figure 16. MC68000 Read And Write Cycle Timing Diagram

7

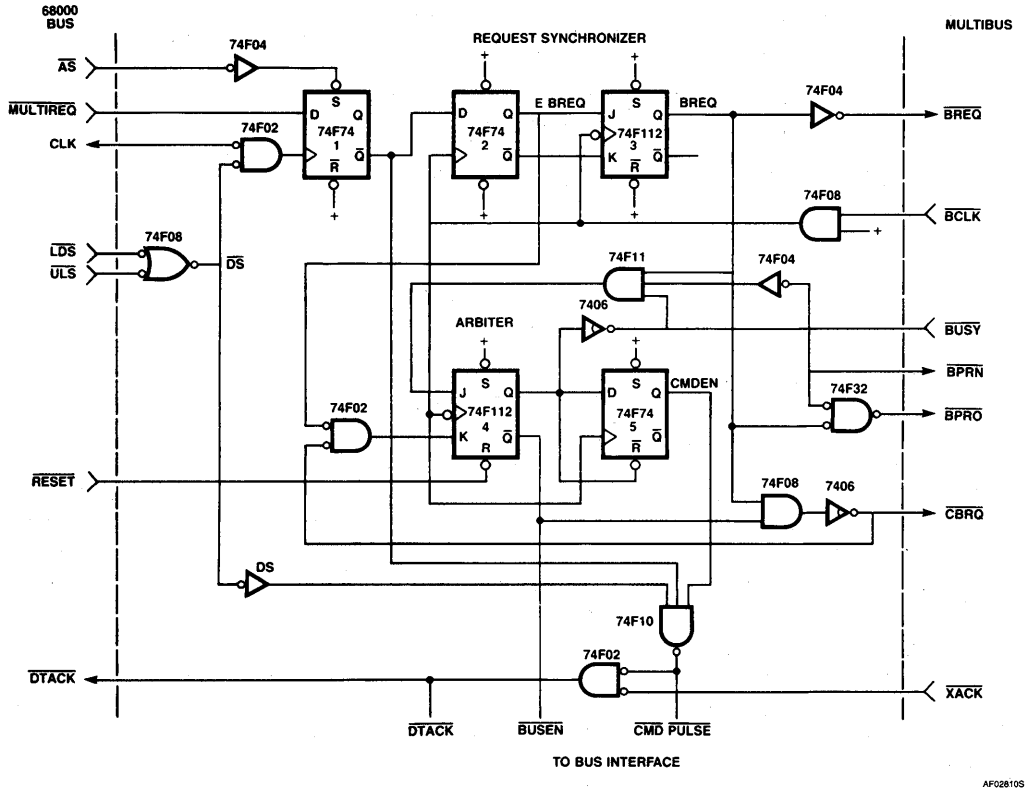


Figure 17. MC68000 MULTIBUS Interface Control Circuitry

Multiple μP Interfacing With FAST ICs AN207

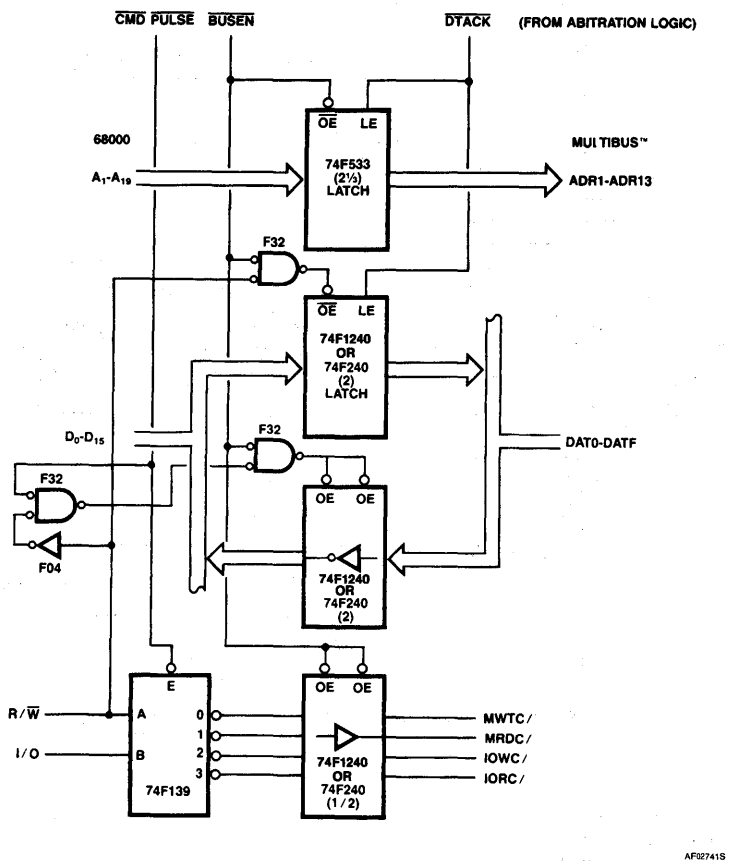


Figure 18. MC68000 To MULTIBUS Interface Logic

7

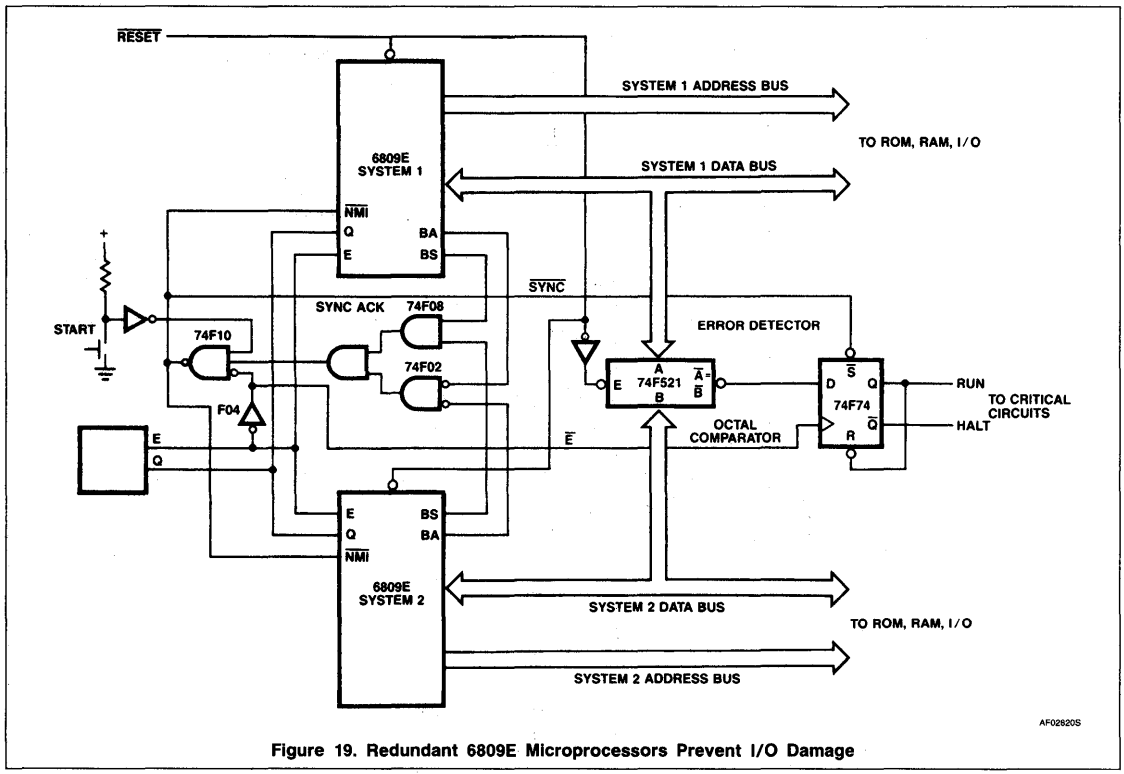


Figure 19. Redundant 6809E Microprocessors Prevent I/O Damage

BIBLIOGRAPHY

Many of the applications illustrated in this note were contributed or influenced by entries in Signetics' Interface Circuit design contest. Special thanks are due to the individuals whose entries were referenced in whole or in part in this note.

AN208
Interrupt Control Logic Using FAST ICs

Application Note

FAST Products

INTRODUCTION

This application note shows how Signetics FAST circuits can be used to implement interrupt control logic for a variety of microprocessors. The circuits presented serve a variety of functions, which include:

- Masking: How to selectively enable interrupt inputs
- Prioritizing: Which interrupt is serviced when more than one interrupt occurs
- Vector Generation: How the interrupt service routine is selected

An interrupt is an asynchronous input to a microprocessor that suspends current program execution and causes a jump to an interrupt service routine. Interrupts are especially useful in real-time systems and have become a standard feature in microprocessor designs.

REASONS FOR USING INTERRUPTS

The use of interrupts generally increases the efficiency of the system. Without interrupts, the microprocessor must poll each peripheral to determine when it is ready for service. The time spent polling cuts down available processing time, and polling is unnecessary when the peripheral devices are not ready for service. With interrupts, the peripheral device informs the processor when it is ready; thus no time is wasted.

Interrupts also provide faster response to service requests from a peripheral. The high data rate of many devices, (e.g. disk drives) requires immediate response to prevent loss of data. As another example, a power-fail interrupt can be used to initiate an orderly shutdown in the remaining moments.

Interrupts can also be used for error handling. If a parity error is detected in the memory, for example, an interrupt can be generated to suspend the operation of the program or invoke an error-handling routine.

INTERRUPT LATCHING

Figure 1 shows a circuit that captures asynchronous events and generates an interrupt to the microprocessor. The 74F533 inverting octal latch is used to "freeze" the state of the interrupt inputs. This is necessary to catch short interrupt request pulses. When all interrupt requests are inactive, the latch enable (LE) input of the 74F533 is asserted. When any request is asserted, the interrupt signal to the microprocessor ($\overline{INT}$) is asserted and the latch is disabled. Thus, the state of the interrupt inputs is latched.

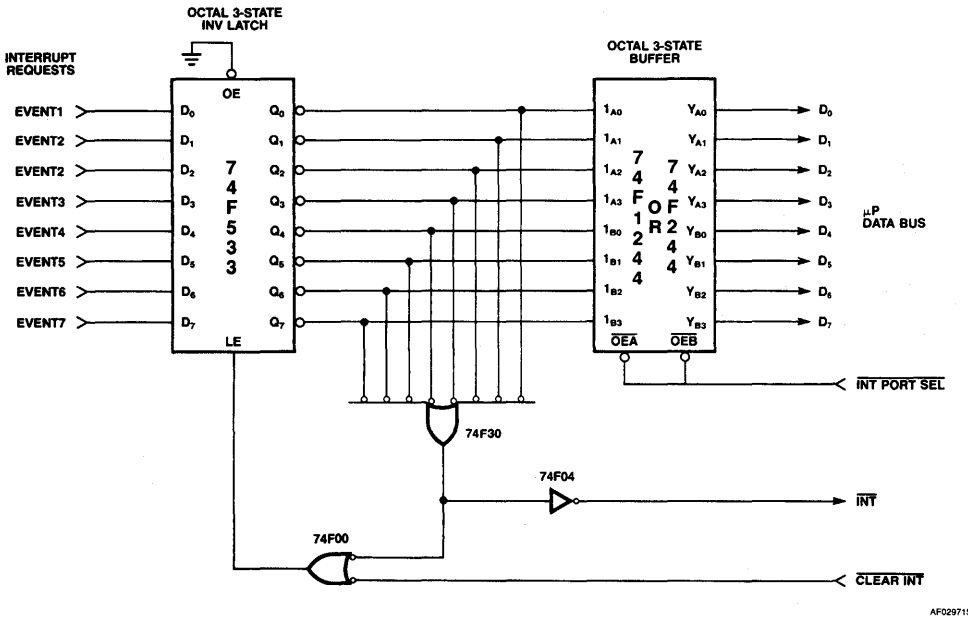


Figure 1. Interrupt Latching

Interrupt Control Logic Using FAST ICs AN208

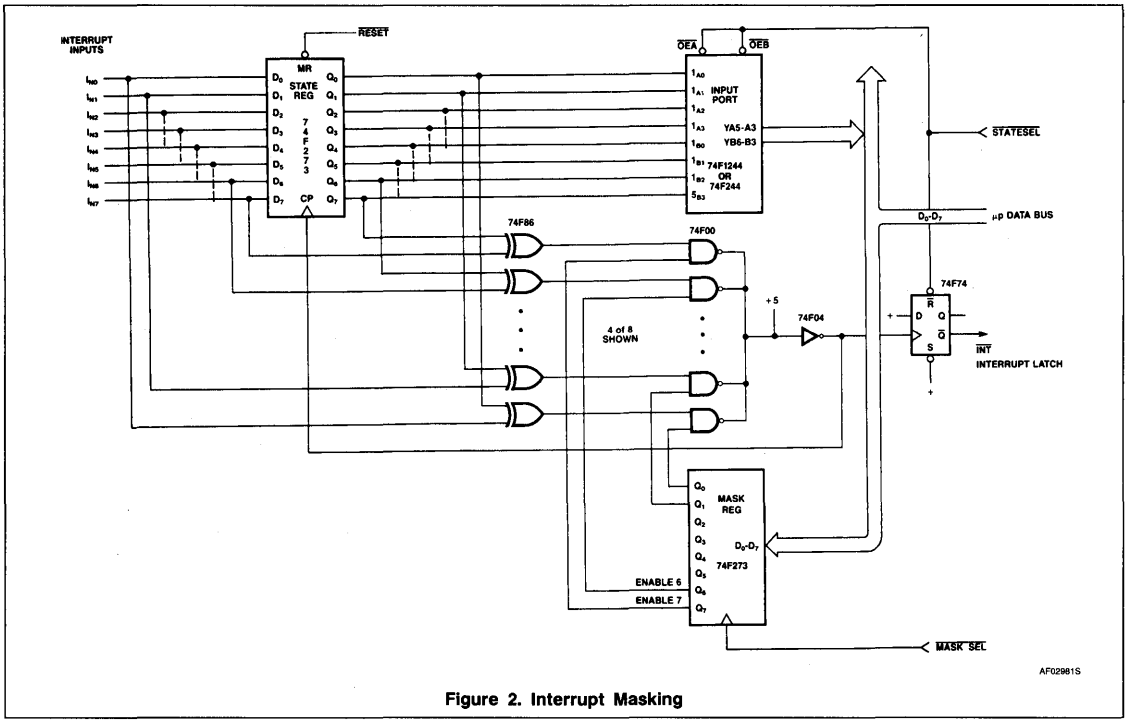


Figure 2. Interrupt Masking

During its interrupt service routine, the microprocessor reads the interrupt latch outputs via the74F1244 or 74F244 octal 3-State buffer to determine which event caused the interrupt. This scheme is most useful with microprocessors such as the 68000 family that do not have vectored interrupts.

At the end of the interrupt service routine, the microprocessor resets the latch by pulsing the /CLEARINT output line. This would typically be generated by decoding a write to a particular address.

INTERRUPT MASKING

Figure 2 shows an interrupt controller that allows each interrupt input to be individually enabled or disabled (masked). A 74F273 octal D flip-flop stores the state of the interrupt inputs whenever any input changes.

Exclusive-OR gates 74F86 compare the inputs of the state register to its outputs; whenever an input changes, the corresponding exclusive-OR gate output goes High.

Another 74F273, connected as an output port, serves as the mask register. The microprocessor writes a bit pattern to this port to determine which interrupts are enabled. The outputs of the exclusive-OR gates are then ANDed with the mask register outputs, so that interrupt inputs with a zero in their mask bit are ignored.

Whenever any unmasked input changes state, the state register is clocked, and the interrupt latch is set. The microprocessor reads the state register via the 74F1244 or 74F244 3-State buffer acting as an input port, and the interrupt latch is cleared.

Caution: This circuit can be fooled if an interrupt input changes twice before the microprocessor reads the state register. Therefore, this design should be used only for relatively slow-changing interrupt inputs.

INTERRUPT PRIORITIZING

In the previous circuits, the hardware does not select which interrupt has highest priority. If two or more interrupts are simultaneously asserted, the microprocessor software must decide which to process first.

Figure 3 shows a circuit with prioritization logic to select the highest priority interrupt. Interrupt inputs are sampled by the 74F377 octal flip-flop. This register is also used to freeze the state of the interrupt inputs when the output of the priority encoder is being read by the microprocessor. If one (or more) interrupt input is asserted, the output of the 74F148 priority encoder will indicate the number of the highest priority active interrupt.

The $\overline{GS}$ output of the encoder is effectively the OR of all the inputs, and produces the interrupt signal to the microprocessor. The microprocessor then reads the interrupt number via the 74F1244 or 74F244 3-State buffer connected as an input port. The microprocessor can use the interrupt number as an index pointer into a branch table, to access the appropriate service routine.

A 74F138 3-to-8 decoder decodes the interrupt number to generate individual reset signals for each interrupt source. The decoder is enabled when the microprocessor reads the interrupt number, so the interrupt output of the device being serviced is automatically reset.

RESTART VECTOR GENERATION FOR 8080 – FAMILY PROCESSORS

The 8080, 8085, NSC800, and Z80 all have interrupt modes in which a vector is automatically read from the interrupting device. (For the 8080, this is the only mode; the other processors also have additional modes.) This vector is treated as an instruction; the single-byte CALL instructions called RESTARTs are

Interrupt Control Logic Using FAST ICs AN208

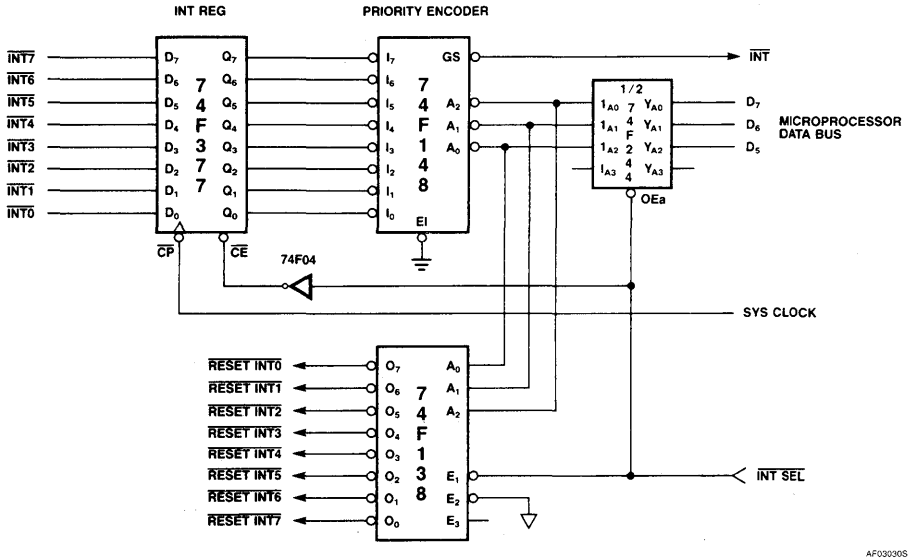


Figure 3. Interrupt Prioritizing

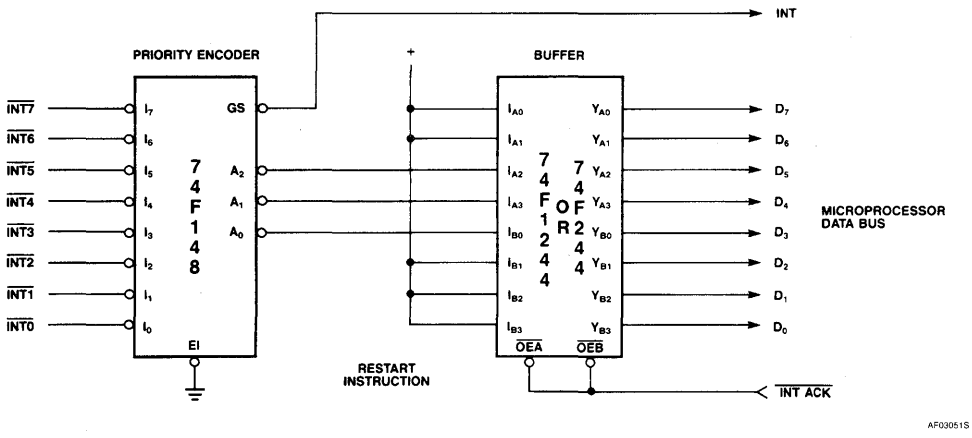


Figure 4. Restart Vector Generation Circuit

generally used for the vectors. The format of the restart instructions is 11CBA111 (binary), where CBA represents the three-bit identifier. Figure 4 illustrates a restart vector generation circuit.

The 74F148 priority encoder generates the interrupt request to the microprocessor when any interrupt input is asserted. It also provides the three-bit identifier to the appropriate inputs of the 74F1244 or 74F244. When the microprocessor performs an interrupt acknowledge cycle, the restart instruction is read via the 74F244 octal buffer. Table 1 shows the vectors generated for each input. Interrupt input 7 produces an identification code of 000, since the priority encoder outputs are active-Low.

Note that the interrupt inputs are not latched by this circuit, and thus must remain asserted until the interrupt acknowledge cycle is completed.

The Z80 microprocessor has several modes of interrupt operation. The mode described above is called mode 1. Mode 2 is a table-driven mode in which the vector supplied by the peripheral is used as a pointer to a table. The service routine address is then read from the table.

Figure 5 shows a circuit for generating the vectors for Z80 mode 2 interrupts. The 74F148 priority encoder generates a three-bit binary number corresponding to the highest priority active interrupt. This number is read by the microprocessor during the interrupt

Table 1. 8080-Family Interrupt Vector Generation

HIGHEST PRIORITY ACTIVE INPUT	VECTOR GENERATED	INSTRUCTION NAME 8080	Z80
INT7	11000111	RST0	RST 0
INT6	11001111	RST1	RST 8
INT5	11010111	RST2	RST 16
INT4	11011111	RST3	RST 24
INT3	11100111	RST4	RST 32
INT2	11101111	RST5	RST 40
INT1	11110111	RST6	RST 48
INT0	11111111	RST7	RST 56

acknowledge cycle via the 74F244 octal 3-State driver.

Table 2 shows the vectors generated by the circuit. The least significant data input of the 74F1244 or 74F244 is grounded, and the code from the priority encoder provides the next three bits. This is necessary because each interrupt vector must point to a two-byte entry in the service routine address table. The four most significant bits are set by the switches. This allows the same circuit to be used in several places in a system by setting the switches differently on each.

VECTORED INTERRUPTS FOR 68000 - FAMILY MICROPROCESSORS

The 68000 microprocessor and its derivatives (68002 and 65002) do not have a built-in mechanism for handling vectored interrupts. When an interrupt occurs, the microprocessor fetches the address of the service routine from memory locations FFF8 and FFF9 (for the 65002, locations FFFE and FFFF). Normally these are ROM locations, and the interrupt service routine address is therefore fixed.

Figure 6 shows a circuit that provides vectored, prioritized interrupts for these microprocessors. When the microprocessor reads from address FFF8 or FFF9, this circuit disables the normal address buffers and substitutes a different address via a second set of 74F1244 or 74F244 octal 3-State drivers. Bits 1, 2 and 3 of the substituted address are determined by the highest priority active interrupt input. Thus, the service routine address is fetched from a different memory location for each interrupt input. The high-order address bits are set by the switches.

Table 2. Interrupt Vectors Generated By Circuit In Figure 5

HIGHEST PRIORITY ACTIVE INPUT	VECTOR GENERATED (HEX)
INT7	X 0
INT6	X 2
INT5	X 4
INT4	X 6
INT3	X 8
INT2	X A
INT1	X C
INT0	X E

NOTE:
1. X = Switch settings

DAISY CHAIN INTERRUPT PRIORITY SYSTEM

In the previous examples, a priority encoder was used to set the priority of each interrupt source. Another way to set priority is with an interrupt priority daisy chain, as shown in Figure 7. The priority of each device is determined by its physical location in the chain. Support for an interrupt daisy chain is built into the peripheral chips for some microprocessor families, such as the Z80. This example shows how a similar daisy chain can be implemented for other microprocessors such as the 8085 or 68000.

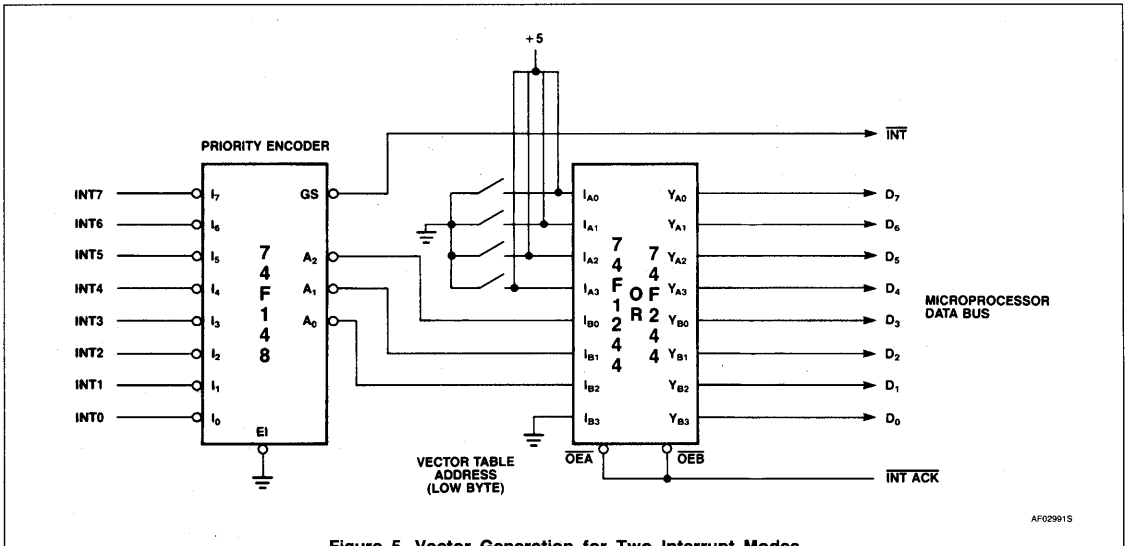


Figure 5. Vector Generation for Two Interrupt Modes

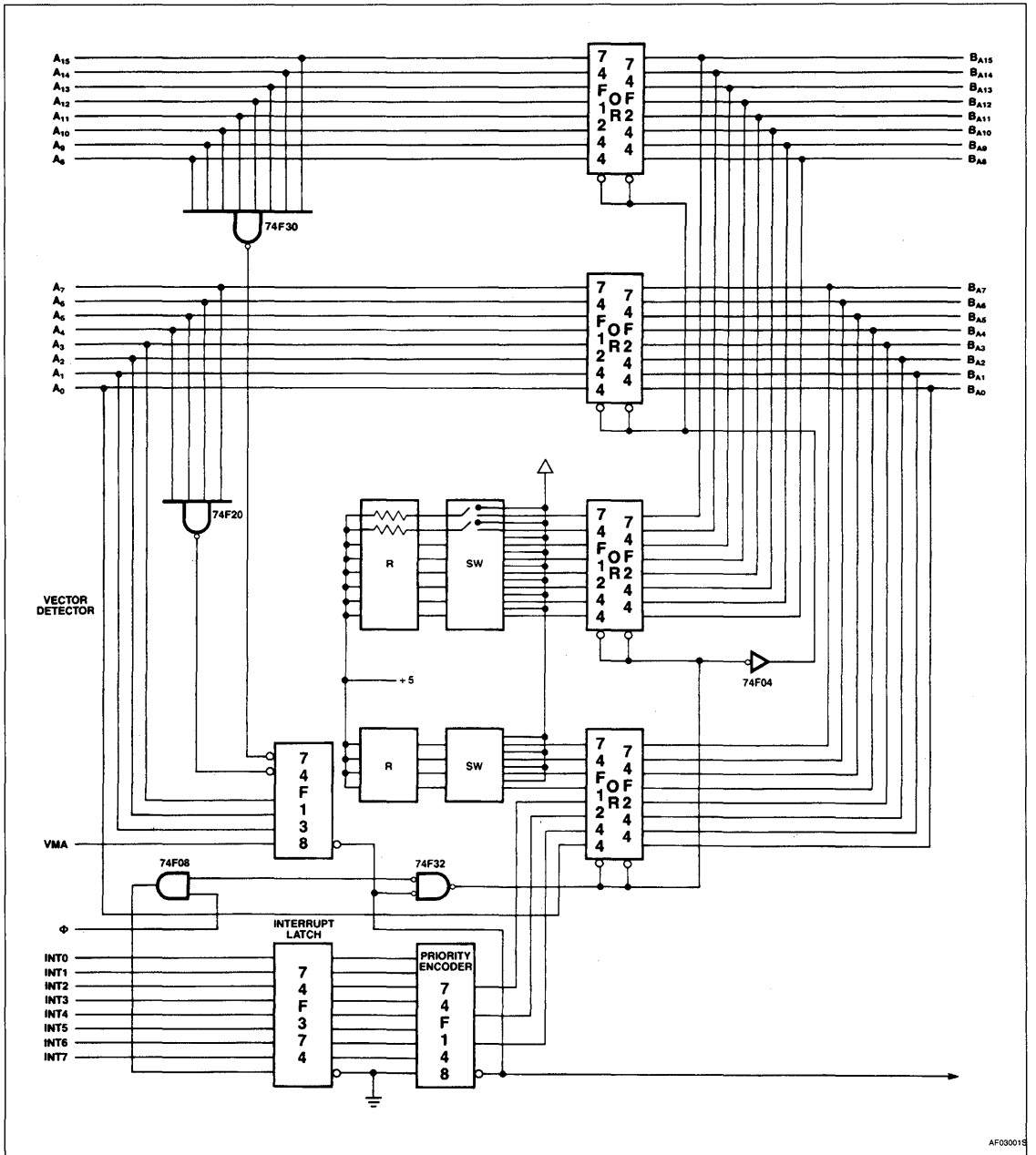


Figure 6. Prioritized Interrupt Vector Generator

Interrupt Control Logic Using FAST ICs AN208

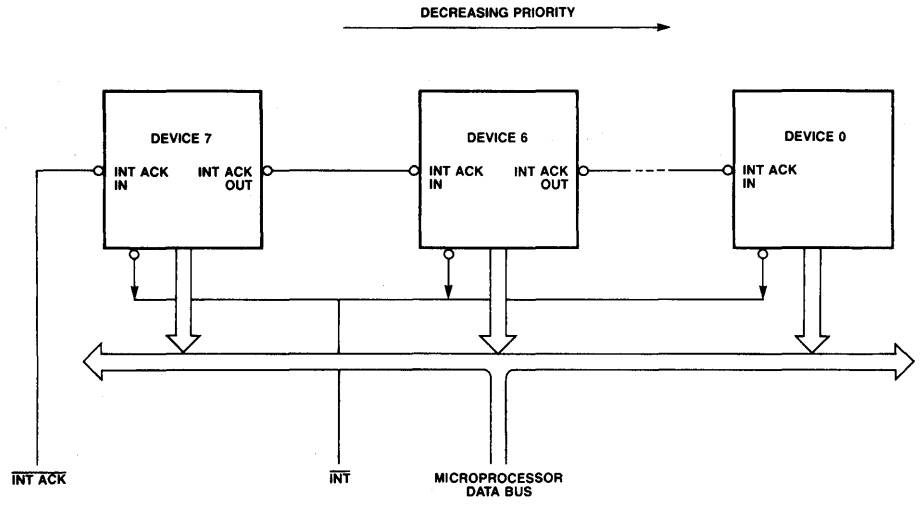


Figure 7. Daisy Chain Interrupt

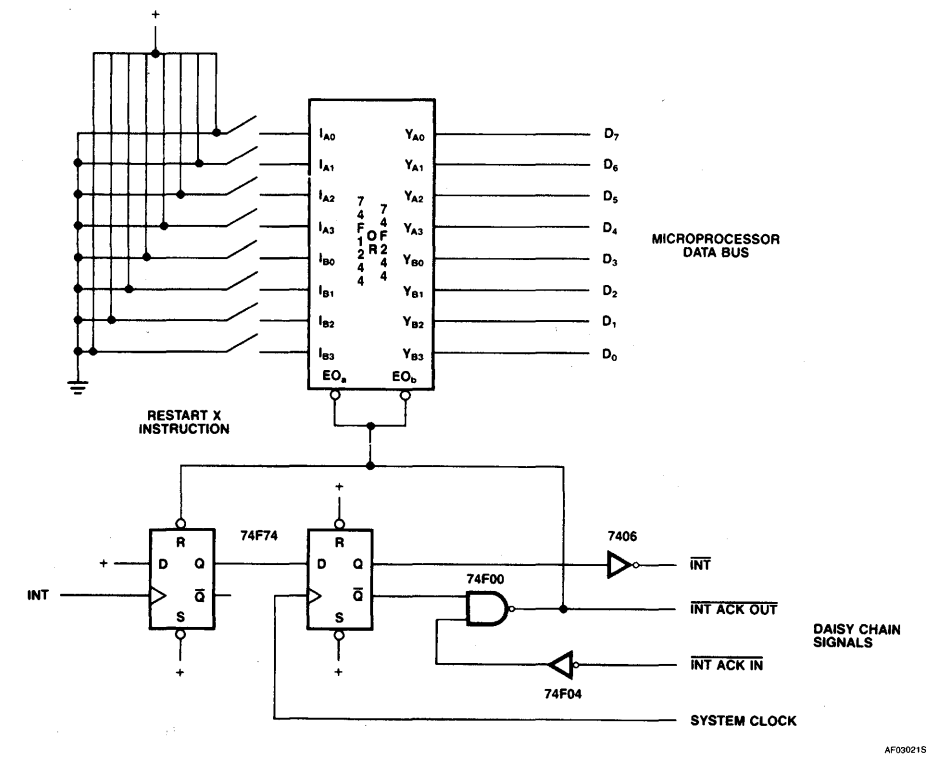


Figure 8. Logic Circuit for Implementation of Daisy Chain Interrupt

Interrupt Control Logic Using FAST ICs AN208

When one or more device asserts an interrupt, the microprocessor responds by asserting $\overline{\text{INTACK}}$ active. This signal connects directly to the highest priority device's $\overline{\text{INTACK IN}}$ input. If that device had not asserted an interrupt, then it passes the interrupt acknowledge signal to the next device via its $\overline{\text{INTACK OUT}}$ signal. Thus, the interrupt acknowledge is passed along from one device to the next until it reaches the highest priority device that generated an interrupt. That device then places its interrupt vector on the data bus.

Figure 8 shows an implementation of this system. The two 74F74 flip-flops latch the interrupt request and synchronize it with the system clock. The signal at $\overline{\text{INTACK IN}}$ is passed to $\overline{\text{INTACK OUT}}$ unless the interrupt latch is set. The 74F244 drives the interrupt vector (restart instruction) to the data bus when $\overline{\text{INTACK IN}}$ is active and the interrupt latch is set. Switches allow the interrupt instruction to be selected for each device.

68000 INTERRUPT STRUCTURE

The 68000 16-bit microprocessor provides an extremely versatile interrupt structure. There are seven interrupt priority levels with up to 256 different vectors per level. The 68000 has a three-bit interrupt input which specifies the interrupt level. A code of 000 means no interrupt; any other code produces an interrupt, and the level corresponds to the code.

Figure 9 shows the timing diagram for the interrupt acknowledge cycle. When the 68000 recognizes the interrupt, it places the interrupt acknowledge code on the function code outputs $/FC_0 - /FC_2$, and outputs the interrupt level being serviced on address lines A_0, A_1 and A_2. The interrupting device then places the interrupt vector on the data bus from which it is read by the 68000.

Figure 10 shows a circuit that allows the user, under program control, to generate an interrupt of any priority level and to supply any interrupt vector. The program uses a MOVE instruction to output the desired interrupt level and vector. The circuit then generates the interrupt. This allows subroutines to be implemented as interrupt service routines. It is also useful for testing interrupt service routines.

All signals are VERSABUS™ signals, with the exception of INT ADDR* which is the output of the address decoder, and RD/$\overline{\text{WR}}$* which must be derived from the VERSABUS™ control signals. Note that the address and data buses are active low; VERSABUS™ notation is used (active low signal names are followed by an asterisk "*"). DS0* and DS1* are basically the same as the 68000's $\overline{\text{UDS}}$ and $\overline{\text{LDS}}$. IACKIN* and IACKOUT* are priority daisy chain signals as described previously. IPL1* through IPL7* are the seven interrupt signals which are fed through a priority encoder on the CPU board (not shown) to generate the binary-encoded interrupt signals to the 68000.

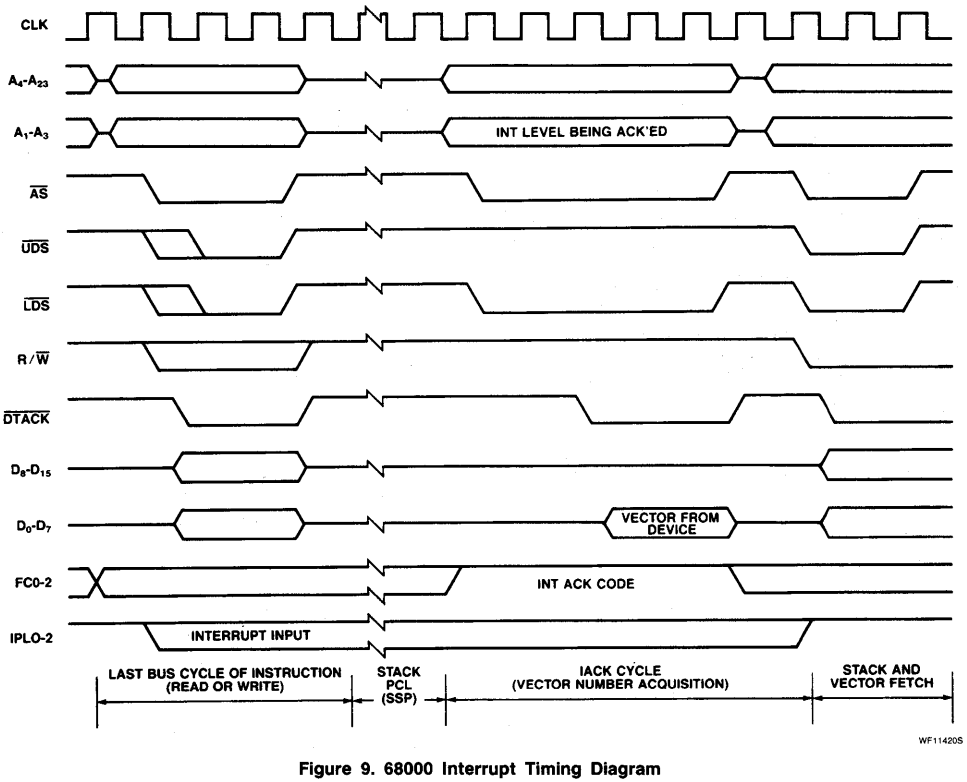


Figure 9. 68000 Interrupt Timing Diagram

Interrupt Control Logic Using FAST ICs AN208

The operation of the circuit is as follows:

- The software performs a move instruction to the address decoded as INTADDR*, with the interrupt vector in $D_0 - D_7$ and the interrupt level in D_8, D_9 and D_A.
- Flip-flop I is set, releasing the clear from the 74F175 priority register C. The new interrupt level is clocked into the register and an interrupt of that level is generated by the 74F138 decoder D.
- At the same time, the interrupt vector is loaded into the 74F373 latch L.
- After an appropriate delay 74F73A flip-flops P and Q generate XACK*, and the cycle completes.

When the 68000 recognizes the interrupt, the following sequence occurs:

- The priority level being serviced, as indicated by the state of A_0, A_1 and A_2, is compared to the contents of the interrupt priority latch C by the 74F85 comparator B. (Note that the $\overline{Q}$ outputs of the 74F175 are used to invert the active low address signals.)
- If the levels match, the interrupt vector is placed on the data bus, XACK* is generated, and the cycle terminates. Flip-flop I is reset, which removes the interrupt by clearing the interrupt request register.

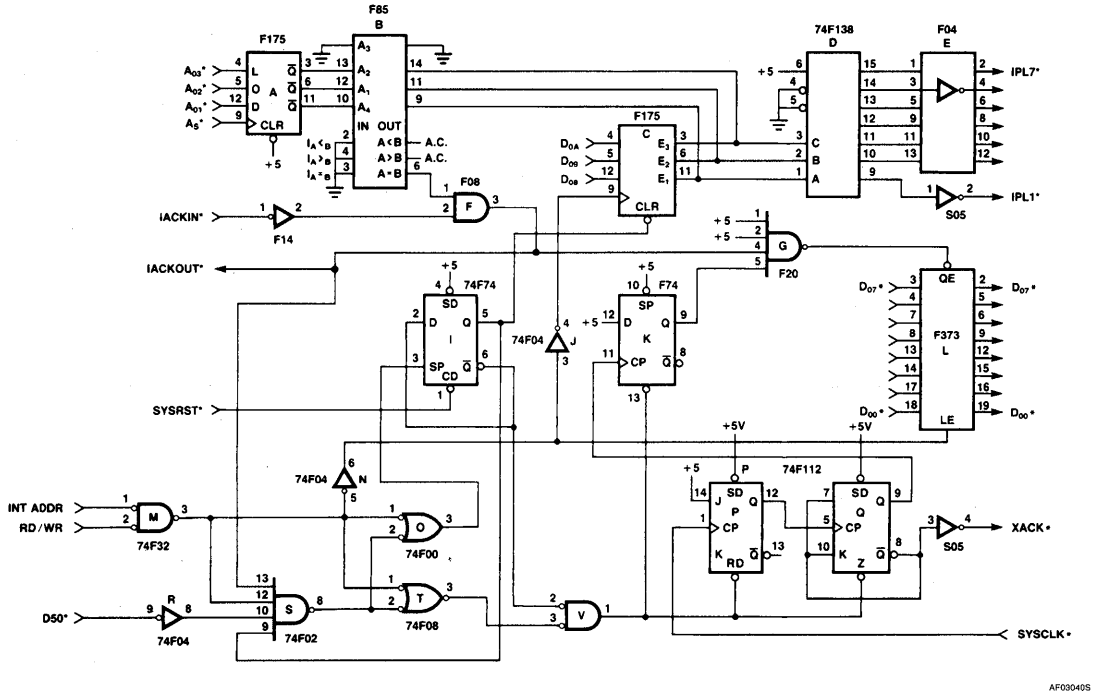


Figure 10. Complete Interrupt Circuit for 68000

BIBLIOGRAPHY

Many of the applications illustrated in this note were contributed or influenced by entries in Signetics' Interface Circuit design contest. Special thanks are due to the individuals whose entries were referenced in whole or in part in this note.

Signetics

AN212
Package Lead Inductance Considerations In High-Speed Applications

FAST Products

Application Note

Authors: Stephen C. Hinkle,
Jeffrey A. West

INTRODUCTION

As circuits become faster, more concern needs to be focused on packaging and interconnects in order to fully utilize device performance. One area of concern is with the package leads between the chip and the board environment. The current flowing into or out of an integrated circuit is conducted through a lead frame trace and bonding wire connecting the integrated circuit to outside circuitry. These leads are circuit elements, inductors, and have a definite effect on the circuit performance because they generate noise in High-speed applications.

Inductance is the measure of change in the magnetic field surrounding a conductor resulting from the variation of the current flowing through the conductor. The change in current through the inductor induces a counter electromotive force, EMF, which opposes that change in current.

An example is a buffer driver discharging a 50pF load. At a switching rate of about 3V in 2ns, the current generated by discharging that capacitor at that rate is:

$$I = C\frac{dV}{dt} \simeq 50pF * \frac{3v}{2ns} = 75mA.$$

All this current flows through the ground lead of the package. Changing the current through this lead generates a ground lead voltage or ground bounce. A typical lead inductance has been measured to be about 10nH. Switching 75mA through a ground lead with an inductive value of 10nH causes a ground bounce of about:

$$V = L\frac{dI}{dt} \simeq 10nH * \frac{75mA}{1ns} = 750mV.$$

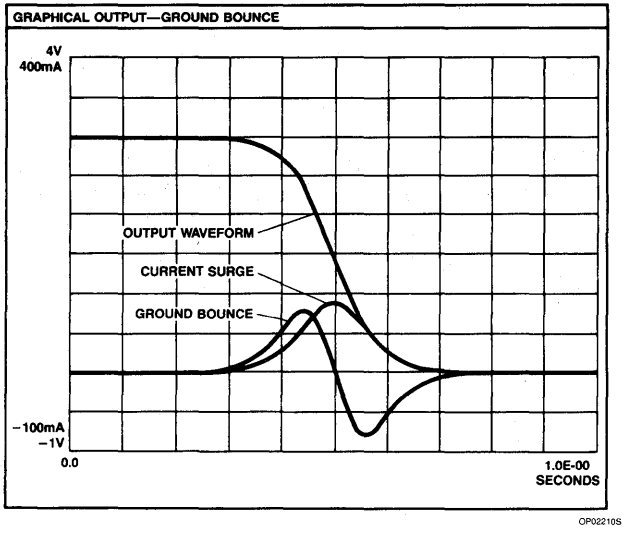


Figure 1

Figure 1 illustrates the current surge and ground bounce during switching. This was modeled using the equations:

$$V(t) = \frac{3V}{1 + e^{(t\text{-}to)/K}}$$

$$I_C(t) = C\frac{dV(t)}{dt}$$

$$V_L(t) = L\frac{dI_C(t)}{dt} = LC\frac{d^2V(t)}{dt^2}$$

If more than one output is switched at a time this ground bounce can get very large. Changing the ground reference on the chip can have significant effects on circuit performance. A V_{CC} bounce can also be calculated when the 50pF load capacitors are being charged and can also have serious effects on circuit performance.

Some of the problems caused by package lead inductance are:

1. Adding delay through buffer parts
2. Changing the state of flip-flop parts
3. Output glitching on unswitched outputs
4. Circuit oscillations

GENERAL PROBLEMS ASSOCIATED WITH GROUND BOUNCE IN High-SPEED CIRCUITS

Adding Delay Through Buffer Parts

Delay through a buffer part is not only a function of the gate itself but is also a function of how many gates in the package are switching at once. Switching more than one output at a time adds to the current being forced through the ground lead of the package. The ground potential seen by the chip rises because of the lead inductance. This rise in ground potential raises the threshold of the gate and tends to turn the gate back OFF slowing the discharge rate of the load capacitor. The gate doesn't finish switching until the ground bounce settles out.

7

Package Lead Inductance Considerations In High-Speed Applications

AN212

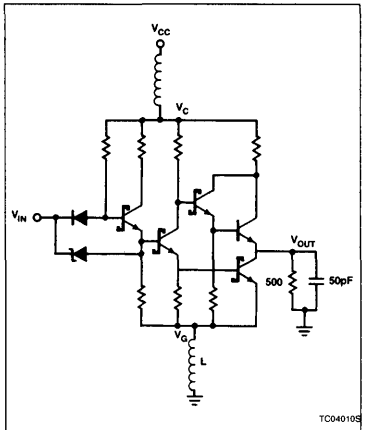


Figure 2

Figure 2 shows an example of a buffer connected to a test load. Probing on the ground pad, V_G, shows the effect ground lead inductance has on the ground pad potential.

Figures 3 and 4 show the ground and V_{CC} bounce during switching on an 'F240 Buffer. The effect of ground bounce on this part is to slow the propagation delays from 3ns with only one output switching to 5ns with all 8 outputs switching at once. AC specifications are usually generated with only one gate switching at a time. For example the 'F240 T_{PHL} limits are 2.0ns minimum, 3.5ns typical and 4.7ns maximum. Therefore when using AC specifications based on single gate switching, a derating factor for multiple switching should be used. A derating factor of 250 to 300ps per output switching has been suggested as a reasonable number and some customers are using this in their internal specifications.

Integrated Circuits Containing Flip-Flops

Integrated circuits containing flip-flops might be seriously affected by inductive ground bounce because of the possibility of the flip-flops changing states. To explore this effect, the 'F374, an Octal D-type flip-flop, was analyzed by comparing test results from the conventional corner mount V_{CC} and ground package to that of a side mount V_{CC} and ground version. A test setup was used where alternate 1's and 0's were clocked into seven of the eight flip-flops to obtain simultaneous output switching and worst case ground bounce. The eighth flip-flop input was held at a DC bias of 2.0V. This should result in its output being held at a constant 1 level.

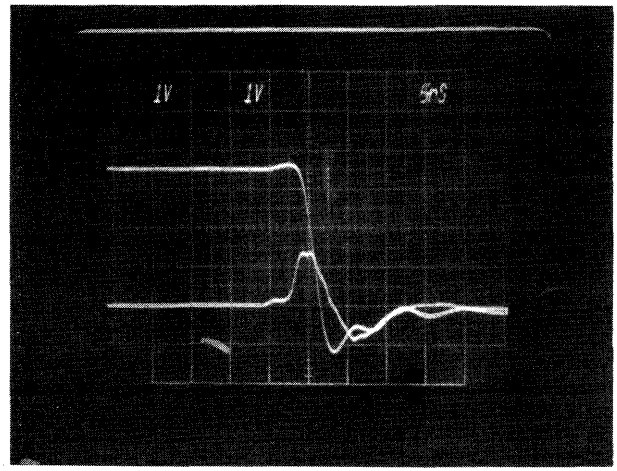


Figure 3

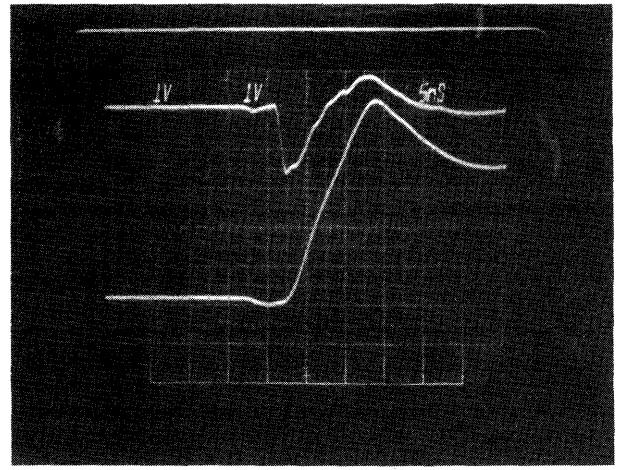
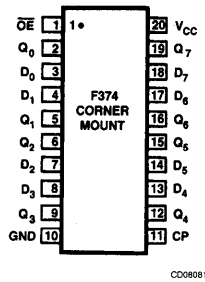


Figure 4

Package Lead Inductance Considerations In High-Speed Applications

AN212



74F374 Failure Analysis

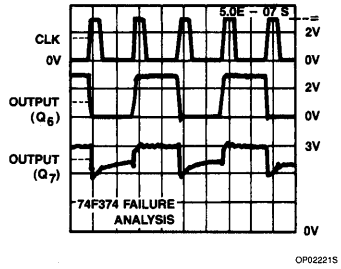
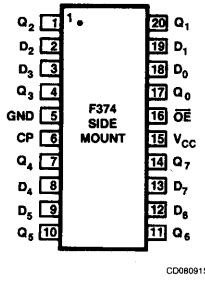


Figure 5



74F374XL

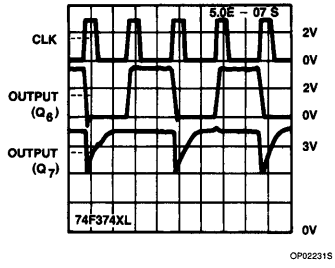


Figure 6

Figure 5 shows the corner mount results. The ground bounce is sufficient to couple the output of the eighth flip-flop (Q_7) to less than 2.0V during the transition of the other seven outputs represented by Q_6. The output then charges to a marginal V_{OH} level.

Figure 6 shows the results from the side mount version. Output glitching during the transition of the other seven outputs is still present, but due to the approximately 50% reduction in lead inductance over the corner mount version, the output is allowed to charge back to its original V_{OH} level.

Output Glitching During Multiple Switching

In some cases the effects of ground bounce can be minimized if properly taken into consideration during the design and layout of the integrated circuit. Note in Figure 7, the glitch that was present on the output of the 'F11, a triple 3-input AND gate, during an early transition of the other two outputs. A newer version of the 'F11 is shown in Figure 8. Note that the glitch has been greatly minimized.

Circuit Oscillations

A fourth area of concern is the possibility of circuit oscillations during slow input transitions through threshold. This would be of importance if the delay through the part is on the order of the natural period of oscillations of the ground inductance and the load capacitance.

During testing, a particular problem has been seen when the inputs are driven by a power supply by way of a cable. Because there is a delay through the cable, it takes time for the power supply to sense a change in the impedance at the input near threshold. This delay sets up oscillations between the power supply and the input of the part when the input is held near threshold.

Inductance Measurements And Verification

To verify that lead inductance caused these problems, the lead inductance was measured and circuit simulations done to show circuit behavior. Measurement of lead inductance was accomplished using an HP S-parameter test set. These measured values of lead inductance were used in a circuit simulation program. The results of the simulation show voltage and current wave forms similar to the measured waveforms.

7

Package Lead Inductance Considerations In High-Speed Applications

AN212

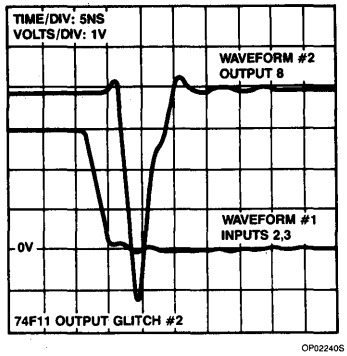


Figure 7

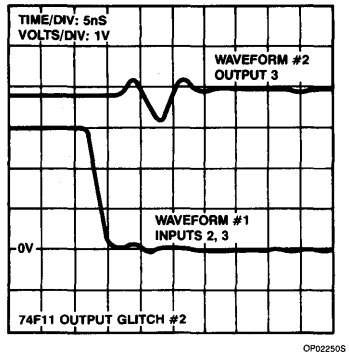


Figure 8

Derivation of the S-parameter Method

The general form for voltage and current along a transmission line is:

$$\bar{V}(z) = V^+ e^{-\gamma z} + V^- e^{\gamma z}$$
$$\bar{I}(z) = I^+ e^{-\gamma z} - I^- e!s$$

Where V^+, V^-, I^+, I^- are constants, usually complex, determined by the boundary conditions, z is the distance from the load and gamma (γ) is a complex term involving a real or loss term and an imaginary or phase shift term.

$$\gamma = \alpha + j\beta$$
$$\gamma \simeq 1/2(R\sqrt{C/L} + G\sqrt{L/C}) + j\omega\sqrt{LC}.$$

Considering the lossless case where R = 0 and G = 0, $\gamma = j\beta$ and only results in a phase shift. The equations for voltage and current then become:

$$\bar{V}(z) = V^+ e^{-j\beta z} + V^- e^{j\beta z}$$
$$\bar{I}(z) = I^+ e^{-j\beta z} - I^- e^{j\beta z}$$

To find Z_1 set z = O. (See Figure 9).

$$\bar{Z}_1 = \bar{V}_1/\bar{I}_1 = (V^+ + V^-)/(I^+ - I^-)$$

since, $I^+ = V^+/Z_0$ and,

$$I^- = V^-/Z_0,$$

$$\bar{Z}_1 = (V^+ + V^-)/(V^-/Z_0 - V^+/Z_0), \text{ or,}$$

$$\bar{Z}_1 = Z_0 \frac{1 + V^-/V^+}{1 - V^-/V^+}$$

V^-/V^+ is called the reflection coefficient and is usually complex,

$$\Gamma = V^-/V^+.$$

The impedance at the load then becomes:

$$\bar{Z}_1 = Z_0 \frac{1 + \Gamma}{1 - \Gamma}$$

On the S-parameter test set, the magnitude of the reflection coefficient, $|\Gamma|$, is measured in dB at a particular angle,

$$\Gamma_{real} = 10^{(|\Gamma dB|/20)} \angle \theta.$$

For an inductor,

$$\bar{Z}_1 = Z_0 \frac{1 + \Gamma}{1 - \Gamma} = R + j\omega L ,$$

usually $R \simeq 0$ and L can be solved for directly.

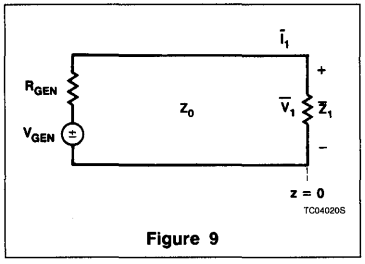


Figure 9

Package Lead Inductance Considerations In High-Speed Applications

AN212

Table 1

PACKAGE	REFLECTION COEFFICIENT	INDUCTANCE
16-pin (300mil-wide)		
8 to 16	−0.50 ∠ 162°C	25.62nH
4 to 12	−0.32 ∠ 172°C	11.51nH
24-pin (600mil-wide)		
12 to 24	−0.56 ∠ 157°C	32.78nH
6 to 18	−0.29 ∠ 157°C	18.33nH
24-pin (300mil-wide)		
12 to 24	−0.47 ∠ 160°C	28.39nH
6 to 18	−0.34 ∠ 170°C	14.27nH

Example

A 16-pin package measuring from pin 8 to 16 has a reflection coefficient $\Gamma_{dB} = -0.5 \angle 162°$, Z_0 of the system is 50Ω and the measurement frequency is 50MHz.

$$\Gamma_{dB} = -0.5 \angle 162°$$

$$\Gamma_{real} = 0.944 \angle 162° = -0.898 + j0.292$$

$$\bar{Z}_1 = Z_0 \frac{1+\Gamma}{1-\Gamma} = 50^* \frac{0.102+j0.292}{1.898-j0.292}$$

$$= 50^* \frac{0.309 \angle 70.7°}{1.920 \angle -8.74°}$$

$$= 8.05 \angle 79°$$

$$\bar{Z}_1 = 1.475+j7.914$$

$L = 7.914/(2\pi^*50MHz) = \underline{25.19nH}$.

Alternately, using the approximation R = 0, so $|Z_1| = \omega L$:

$$L = \frac{8.05}{2\pi^*50MHz} = \underline{25.62nH}$$

Three packages were used to measure lead inductance, a 16-pin CERDIP, a 24-pin CERDIP and a 24-pin skinny CERDIP. V_{CC} and ground were double bonded to an 80 × 80 mil blank die. Table 1 shows the results of the measurements.

These values are the total inductance V_{CC} to ground. Each lead inductance would be about one half these members.

Simulation of Measured Values

Both ground and V_{CC} bounce for the 'F240 were simulated using the inductive values measured. The results were similar to the measured data of the 'F240, Figures 3 and 4. The simulation of the 'F240 is shown in Figure 10. This shows the pad V_{CC}, the pad ground (V_G) and the inputs (V_{IN}) and outputs (V_{OUT}) when all 8 buffers are switched simultaneously.

SUMMARY

A major contributor to noise in High-speed circuits is package lead inductance. Integrated circuits are packaged with lead frame traces and bonding wire. These leads act as inductors. Voltage generated across these leads follow the law:

$$V = L \frac{di}{dt}$$

This represents noise to an integrated circuit chip and can cause performance degradation. The faster the switching rates become, the more lead inductance can affect circuit performance.

As circuits become faster, more care should be taken in packaging and chip layout. In some cases like the 'F11, a better layout can help remove potential problems but in most cases like the 'F240, the noise is strictly a function of the package. Care should be taken in integrated circuit packages to minimize lead lengths. Side mount V_{CC} and ground pins, smaller packages such as the surface mounted SO, and High levels of board integration are a few possibilities which would help minimize lead lengths.

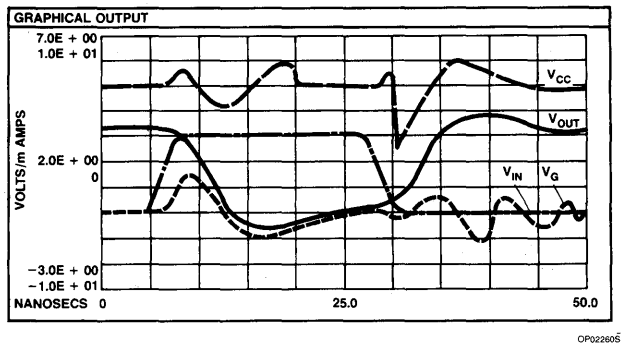


Figure 10

Signetics

AN213

74F30XXX FAMILY APPLICATIONS

High Current Buffers/Transceivers

Application Note

Standard Products

The 74F30XXX Family

- 74F3037 Quad 2-Input NAND, Totem-Pole Buffer
- 74F3038 Quad 2-Input NAND, Open Collector Buffer
- 74F3040 Dual 4-Input NAND Totem-Pole Buffer
- 74F30240 Octal, Inverting, Open Collector Buffer
- 74F30244 Octal, Non-Inverting Open Collector Buffer
- 74F30245 Octal, Non-Inverting, Transceiver
- 74F30640 Octal, Inverting, Transceiver

Major Family Features

- Incident-Wave, 30Ω Transmission Line Drivers
- High Output Currents - I_{OL}/I_{OH} = +160mA/−67mA
- 74FXXX Speeds - Gate Speeds <6.5 ns
- "Flow-Through" Signal Design
- Multiple, Center-Package Supply Pins
- Low V_{CC} Shut-Off Circuit
- Low Impedance Voltage Reference
- Active (Dynamic) Pull-Off Circuit
- "Light-Load" ±20μA NPN Inputs
- Applications Described on Page 6

KEY DESIGN PARAMETERS V_{CC} = 5.0 V ±10% & T_A = 0°C to 70°C

SYM	PARAMETER	MIN.	TYP.	MAX.	UNIT
I_{IL}	F3037/38/40, V_{IL} = 0.5V, V_{CCmax}			-20	μA
I_{IH}	F3037/38/40, V_{IL} = 2.7V, V_{CCmax}			20	μA
I_I	F30240/244 Input Leakage, Hi/Low	-20		+20	μA
I_I	F30245/640 A_N Port I/O Leakage, Hi/Low	-70		+70	μA
I_{OL}	V_{OL} = 0.55V, V_{CCmin} (All Devices)	100			mA
I_{OL1}	V_{OL1} = 0.8V, V_{CCmin} (All Devices)	160			mA
I_{OH}	F3037/40, V_{OH} = 2.5V, V_{CCmin}	-45			mA
I_{OH1}	F3037/40, V_{OH1} = 2.0V, V_{CCmin}	-67			mA
I_{OZ}	F30245/640, B_N Hi-Z Leakage, Hi/Low	-70		+70	μA
I_{OL}	F30245/640, A_N, V_{OL} = 0.50V, V_{CCmin}	24			mA
I_{OH}	F30245/640, A_N, V_{OH} = 2.4V, V_{CCmin}			-3.0	mA
I_O	F3037/40, V_{OH} = 2.25, V_{CCmax}	-60		-160	mA
I_{OS}	F3037/40, V_{OH} = 0.0V, V_{CCmax}		-300		mA
I_{OS}	F30245/640, A_N, V_{OH} = 0.0V, V_{CCmax}			-150	mA
t_P	F3037 Prop. Delays (PD), HL or LH	1.5		6.5	ns
t_P	F30245/640, A_N to B_N PD, HL or LH	1.0		13.5	ns
t_P	F30245/640, B_N to A_N PD, HL or LH	1.0		7.0	ns
t_{PZ}	F30245/640 A_N & B_N Hi-Z PD, HL or LH	1.0		8.0	ns
I_{CC}	F30XXX Per Gate, V_{CCmin}		8		mA
V_{CCZ}	F30XXX Octals, Low V_{CC} Hi-Z Outputs	2.0			Volts
P_{Dmax}	24-Pin Plastic DIP, T_A = 70°C, T_J = 130°C		1		Watt
θ_{JA}	24-Pin Plastic DIP Thermal Resistance		60		°C/W
θ_{JA}	16-Pin Plastic DIP Thermal Resistance		83		°C/W

Introduction

The Signetics 74F30XXX Family is a new series of very high output current, high performance drivers designed to handle low impedance environments of printed circuit board transmission lines and signal busses. This Family can drive lines with characteristic impedances as low as 30Ω at standard 74F speed.

This Application Note explains how the 74F30XXX's design innovations (2 patents) will give you several major advantages over other high current TTL gate, buffer and transceiver designs. It also illustrates how to use the 74F30XXX's superior characteristics in many applications that currently cannot be handled by standard TTL buffer products.

The totem-pole structure of the 74F3037/40 can easily sink 100mA @ 0.55V (160mA @ 0.8V) and source −45 mA @ 2.5V (−67mA @ 2.0V). The open collector (OC) 74F3038 Quad and 74F30240/244 Octal Buffers use only the 74F3037/40's high current pull-down output structure. The 74F30245/640 Octal Transceivers use high current OC outputs for the B_N port with the A_N port's 3-State outputs able to handle +24/−3mA at TTL (0.5V/2.4V) logic output voltage levels.

Speed is not sacrificed for high output current drive. The 74F30XXX's propagation delays are similar to standard 74F

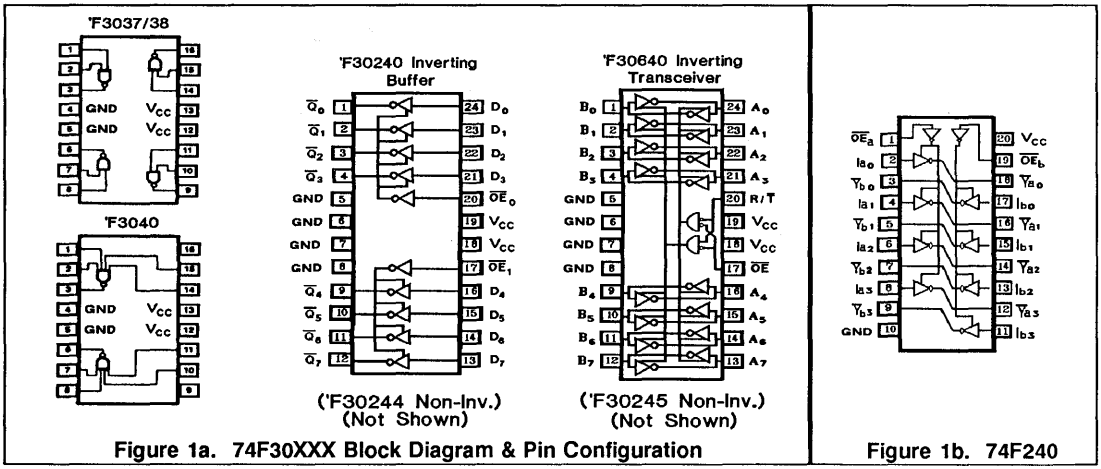


Figure 1a. 74F30XXX Block Diagram & Pin Configuration

Figure 1b. 74F240

devices. As an example, the 74F3037 and the 74F37 both have guaranteed propagation delays between 1.5 and 6.5ns (min/max).

Flow-Through Design

Figure 1a shows the Block Diagrams and Pin Configuration of 5 of the 7 parts of the 74F30XXX Family (74F30244/245 not shown). Notice that each device has at least one ground pin for every two outputs and one V_{CC} pin for every four outputs. Also, the 74F30XXX Octals use a "broadside" design to allow signals to "flow-through" the package. I/O control pins are placed on both sides of the V_{CC} pins.

Comparing the standard 74F240 Pin-Configuration (Figure 1b) with that of the 74F30240, you can see that the 74F30XXX's Flow-through design simplifies the design and layout of large, bus-oriented PC boards.

Input Structures

As shown in Figure 2a (74F3037/40 Circuit Diagram), the input structure is a simple diode AND gate driving the base of Q1. D1 is the input Schottky clamp diode. D2 is the AND input terminal with an input threshold of 2 V_{BE} voltage drops and an I_{IL} (V_I = 0.5V) of 600μA. When all of the inputs are HIGH and one input goes LOW, the input speed-up Schottky diode, D3, discharges the base stored-charge of Q3A & Q3B to ground allowing them to be quickly turned OFF.

A patented "Light-Load" NPN input is used on the inputs of the 74F30240/244 Octal Buffers and the A_N port inputs of the 74F30245/640 Octal Transceivers (Figure 4a). Its input bias current is less than ±20μA for V_I between 0.0V and 5.5V. This NPN input also has a patented NPN transistor turn OFF speed-up circuit (D2/Q2/D4). These patents are discussed in the "Light-Load Input Drivers and Transceivers" Applications Note AN215.

74F3037/40 Output Drive

Figure 3 shows a simplified version of the 74F3037/40's typical output LOW (I_{OL}) and HIGH (I_{OH}) currents versus the output voltage. Note the symmetry of the HIGH and LOW output resistance. As V_{OL} is swept from 0.16V to 5V, R_{OL} (output LOW resistance) changes from ~2.4Ω to ~23Ω. For the same output voltage sweep, R_{OH} (output HIGH resistance) goes from ~23Ω to ~3.6Ω to Hi-Z.

At V_O = 1.5V, the 74F3037's HI and LOW output resistances are approximately 23Ω. If the slope of these sourcing and sinking 23Ω resistances are extended to zero output current, they appear to be switched between equivalent supply busses of +4.75V and -7.75V. This symmetrical output resistance characteristics and the 12.5V apparent output swing are the major reasons that the 74F3037/40 show such excellent 30Ω unterminated transmission line, incident wave switching performance.

Referring to Figure 2a, both Q6 and R8 of the 74F3037/40 are very large area devices producing a relatively large, parasitic capacitance to ground at the collector of Q6. During LOW-to-HIGH output transitions. This 7-10pF capacitance produces a small amount of additional transient I_{OH} drive which helps produce a smooth output transition.

74F3037/40 Output Feed-Through Current

The 74F3037/40's totem-pole output has been designed with virtually no output current spiking or feed-through current. Feed-through current can occur during any output transition when both the pull-up and pull-down output transistors are ON simultaneously. In standard TTL circuits, feed-through current is one of the prime contributors to power supply noise and increased power dissipation with increasing frequency of operation.

To minimize feed-through current, internal circuit delays are used to prevent the upper and lower structures of the 74F3037/40's totem pole output from being ON at the same time. Without this feed-through current, supply plane noise is significantly reduced.

Many standard TTL gate output structures have feed-through currents which are limited only by their pull-up I_{OS} resistors. This condition significantly reduces the amount of output current available during switching transitions. Under heavy load conditions, feed-through can cause non-linearities or flattening in the output switching waveforms. The innovative 74F3037/40 design virtually eliminates feed-through current, allowing the outputs to have significantly more available output transition current and producing very linear output switching transitions.

Figure 2a. 74F3037/40 Circuit Diagram

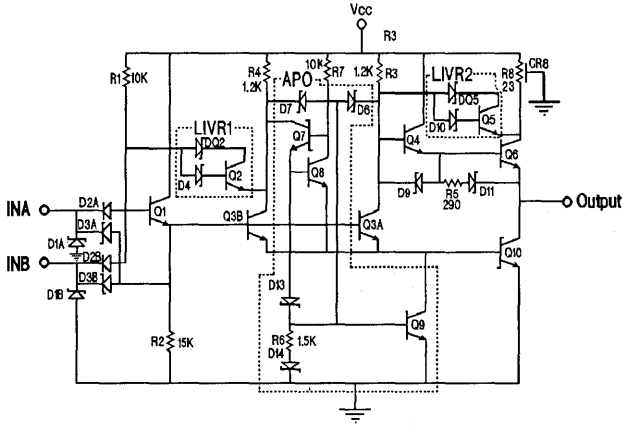


Figure 2b. Non-LIVR Buffer Output

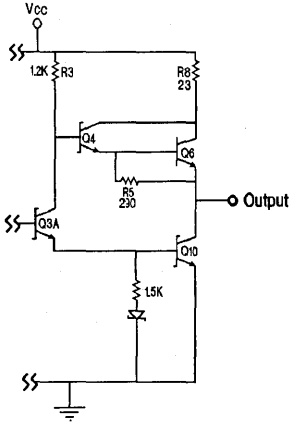


Figure 2. 74F3037/40 Circuit Diagram & Non-LIVR Buffer

Figure 3a. Output LOW Current
For the 74F3037/40

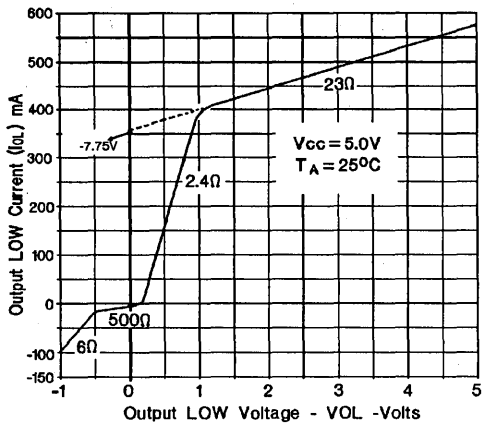


Figure 3b. Output HIGH Current
For the 74F3037/40 w/ & w/o LIVR

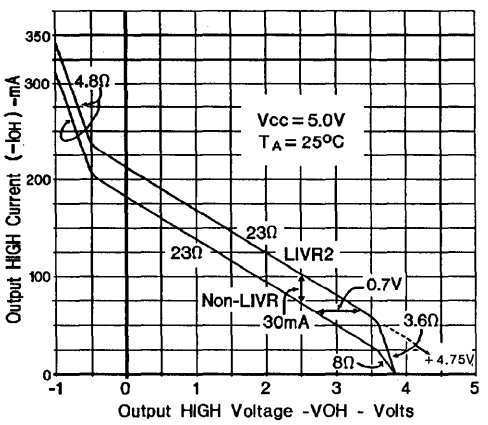


Figure 3. 74F3037/40 Sinking & Sourcing Output Driver Capabilities

Low Impedance Voltage Reference

The patented Low Impedance Voltage Reference is a temperature compensating voltage reference used throughtout the 74F30XXX Family for input speed up (LIVR1) and output noise immunity improvement (LIVR2). The 74F3037 (Figure 2a) is used in the following analyses of the LIVR1 and LIVR2 circuits.

LIVR1 Operation

Refering to Figure 2a, the combination Q1, Q3B and LIVR1 (D4, DQ2 and Q2) is a "kicker circuit" which reduces input propagation delay. LIVR1 is connected between the base of the input transistor, Q1, and the collector of Q3B. When all inputs switch HIGH, current from R1 flows into the base of Q1. Q1's collector-emitter current rapidly turns ON the phase-splitter transistor, Q3A, which turns OFF the output pull-up structure.

When the collector voltage of Q3B has dropped sufficiently to forward bias LIVR1, it begins to regulate Q1's base drive, and a low quiescent Q3A/B base drive current is established. With Q1's collector tied directly to V_{CC}, it cannot saturate and, therefore, can be turned OFF quickly.

LIVR2 Operation

This section compares a standard Schottky Darlington pull-up (non-LIVR Figure 2b) with that of the 74F3037/40's LIVR2 pull-up (Figure 2b). For simplicity, the same circuit resistor values will be used.

Assumptions:

- The Q6 $V_{CE(SAT)}$ of the Darlington output pull-up structure will be aproximatley 0.9V.
- The LIVR2 allows the Q6 $V_{CE(SAT)}$ to drop to 0.2V
- R8, the Ios resistor, for both output HIGH driver circuits is 23Ω.

Figure 4a. Output Enable Cell

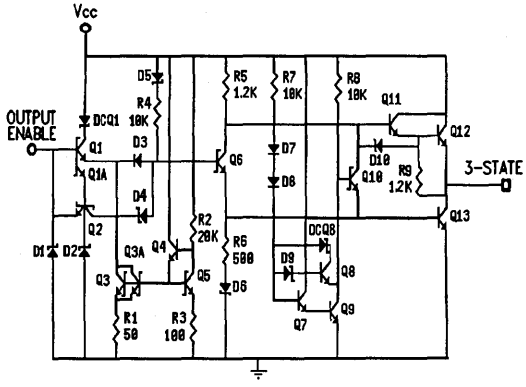


Figure 4b. Data Cell

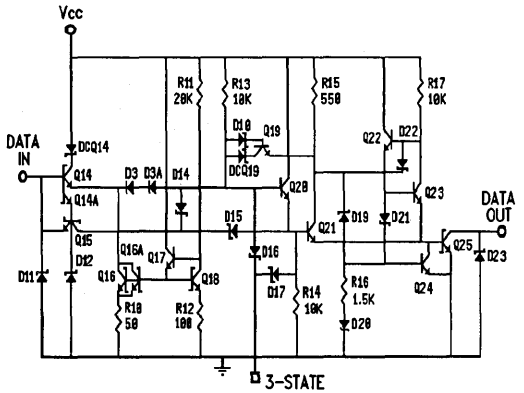


Figure 4. 74F30240 Circuit Diagrams

Under these conditions, the LIVR2 output can supply an additional 30mA (23Ω x 0.7V) output HIGH current (I_{OH}) at any specified output HIGH voltage. Also, at the same I_{OH}, the LIVR2 increases V_{OH} by ~0.7V over that of the standard non-LIVR, Darlington pull-up. Refer to Figure 3b.

Active Pull-Off Circuitry

The patented Active Pull-Off (APO) circuit (Figure 2a) consists of a dynamic base discharge and a quiescent pull-off network for the output pull-down transistor (Q10). The APO reduces I_{CCL} (I_{CC} with outputs LOW) requirements by about 30% in comparison to passive pull-off circuits by eliminating the standby pull-off current. This circuit is also part of the timing network for eliminating any totem pole feed-through current.

Low VCC Shut-Down Circuit

In a multi-card bus system where power to one card could be disrupted for any reason, the powerless card must not effect access to the system by the other cards. Systems with common signal busses and power supply planes must continue to operate regardless of any subsystem failure. Many bus driver products in common use today do not provide an output disable circuitry that disables or Hi-Zs all shared system interconnections when V_{CC} drops below its nominal operating range.

The Signetics 74F30XXX octals have solved this problem with a very effective Low V_{CC} Shut-Down circuit. This circuit is shown in the 74F30240's Output Enable Cell (Figure 4a). It detects when V_{CC} falls below 4 V_{BE} voltage drops (R7 biasing D7, D8, Q7 & Q9) then turns Q9 OFF and Q10/Q13 ON by allowing the current through R8 to drive Q10's base instead of being shunted to ground by Q9. This V_{CCZ} value will be >2.0V for T_A = 0° to 70°C.

When Q13 is ON, D16 and D17 (in the 74F30240's Data Cell Figure 4b) shunt the base drive of both Q20 and Q21 to ground. With these transistors OFF, the Data Cell's open collector output (Q25) cannot be turned ON.

The 74F30245/640 Octal Transceivers also have blocking-diodes in the output pull-ups of the A_N port which effectively block any output leakage current through the pull-up path when power is off.

Power Dissipation

The Active Pull-Off and the Low Impedance Voltage Reference circuits used throughout the 74F30XXX Family significantly reduce the I_{CC} over standard advanced Schottky design techniques. In fact, without these innovations, the 74F30XXX Family would not be practical due to lower performance and excessive transient and quiescent power dissipation.

Because the 74F3037/40's totem-pole output has virtually no output feed-through current, I_{CC} does not increase significantly due to increasing frequency. This is not true for most other TTL logic families.

For the 74F30240, the I_{CCH} is about 1/3 of the I_{CCL}. The guaranteed values of I_{CCH} and I_{CCL} are <23mA and <95mA. For reference, the standard 74F240's I_{CCH}/I_{CCL} guarantees are 18/70mA, which is 75% of the 74F30240 version.

The 74F30240 in a 24-pin, 0.3 inch lead centers, plastic dual in-line package is an example of the chip/package power dissipation handling capabilities of the Family:

- With I_{CCL} = 95mA @ V_{CC} = 5.5V, 8 fully loaded outputs @ I_{OL} = 160mA and V_{OL} = 0.5V @ 70°C, the total package power dissipation will be equal to 1.16W.
- Using T_A = 70°C, T_J = 130°C and θJA = 50°C/W (with an air flow of 200 LFPM) yields a package power dissipation capability of 1.2W.

However, assuming that not all conditions will be worst case simultaneously, the total chip power dissipation should never exceed 1.0W. In designs utilizing 74F30XXX parts near their maximum specified drive capabilities, conservative design precautions dictate that the thermal resistance of the packages be reduced by increasing the air-flow across and/or heat sinking the packages.

Ground & VCC Bounce

A major problem with sourcing and sinking large amounts of current at a dV/dt of >1V/ns is inductance in the ground leads of a package (Figure 5a) which causes "ground bounce" during output transitions due to the load currents being switched ON and OFF. Another component of "ground bounce" in standard TTL circuits is feed-through current which has been eliminated in the 74F3037/40 totem-pole output devices. Changes in output current must overcome the inductances of the package power supply and output leads before being able to drive any load. In doing so, voltages are developed across these inductances which can effect the internal logic thresholds of high-speed logic devices.

V_{CC} bounce is not nearly as critical as ground bounce since a TTL gate's input threshold is referenced only to package ground lead. Also, the V_{CC}-to-output current (I_{OH}) (zero for open collector devices) is usually much smaller than output-to-ground current (I_{OL}).

Figure 5b illustrates the measured lead inductance for both 16- and 24-pin plastic DIPs. Note that the center pins of any PDIP package, being the closest to the chip, have the lowest inductance. Lead length and cross-sectional area equate to inductance. The longer the ground lead, the greater the lead inductance and the larger the ground bounce.

$$dV_{GND} = L(dI/dt)$$

A comparison of the actual measured lead inductance for 16- and 24-pin plastic DIPs with both corner and center (with and without multiple) supply pins devices is shown below:

#/PINS	PWR PINS	# V_{CC}/GND PINS	EQUIV. IND.
16-Pins	Corner	16/8	10.5nH
16-Pins	Center	12/4	3.3nH
16-Pins	Center	12,13/4,5	1.7nH
24-Pins	Corner	24/12	18.1nH
24-Pins	Center	18/6	3.7nH
24-Pins	Center	18,19/5,6,7,8	1.9/1.2nH

On the 24-pin PDIP the ratio between the lead inductance of a single, corner ground lead (18.1nH) and 4 center grounds (1.2nH) is 15:1.

Using the example of a 74F30240 with all eight outputs switching simultaneously from a HIGH-to-LOW state into 30Ω loads, I_{CC} changes plus the total output current into the ground lead will be:

$$dI_{CC} = 95mA(LOW) - 23mA(HIGH) = 72mA$$
$$dI_{OUT} = 8 \times (5.0V-0.5V)/30\Omega = 8 \times (0.15A) = 1.2A$$
$$dI_{GND} = dI_{CC} + dI_{OUT} = 72mA + 1.2A = 1.27A$$

For 1 Corner Ground Pin - L_{GND} = 18.1nH

$$dV_{GND} = L(dI/dt) = 18.1nH \times (1.27A/2ns) = 11.5V$$

For 4 Center Ground Pins L_{GND} = 1.2nH

$$dV_{GND} = L(dI/dt) = 1.2nH \times (1.27A/2ns) = 763mV$$

In use, the internal ground bounce will not actually reach these calculated voltage levels. The ground bounce is divided between the equivalent inductance in series with the 8 outputs (paralleled 1.6nH) and the 4 ground supply pins' equivalent inductance (1.2nH).

Also, because the length of the PC board trace to any load increases the effective output lead inductance and, because the supply pins are tied to large, low inductance supply planes, the ground bounce voltage is significantly reduced by dividing the potential ground voltage rise between the output and supply inductances.

Minimizing the effects of supply bounce on the internal logic threshold levels of TTL logic chips allows faster systems to be built. If corner supply pins parts are used, the logic LOW level threshold can be jeopardized by ground bounce, whereas, the ground bounce on the 74F30240/244/245/640 chips, with their multiple, center supply pin design, only effects the chip's thresholds by <0.7V during HIGH-to-LOW transitions.

Living with Ground Bounce

If non-inverting buffers and transceivers (74F30244/ 245) are used, the ground bounce actually enhances the noise immunity of the chip. Changes in the current through the ground lead inductance reinforce the input thresholds by creating a very effective dynamic input hysteresis.

Care should be taken to minimize supply bounce during output switching transitions. These include minimizing supply lead inductance by keeping their PC board traces as short and as wide as possible. Inductance in the output lead actually reduces supply bounce as mentioned earlier.

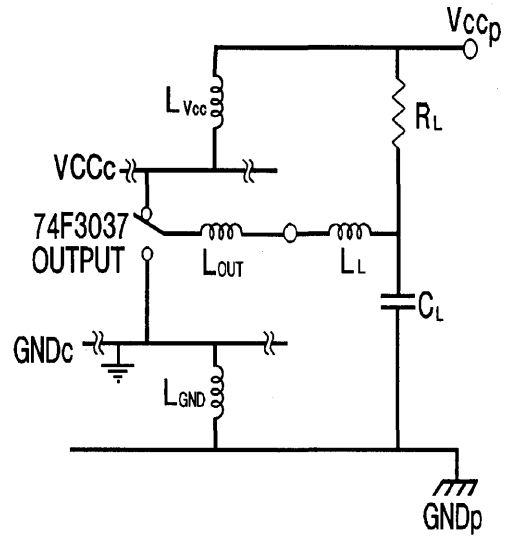


Figure 5a. Plastic DIP Lead Inductance

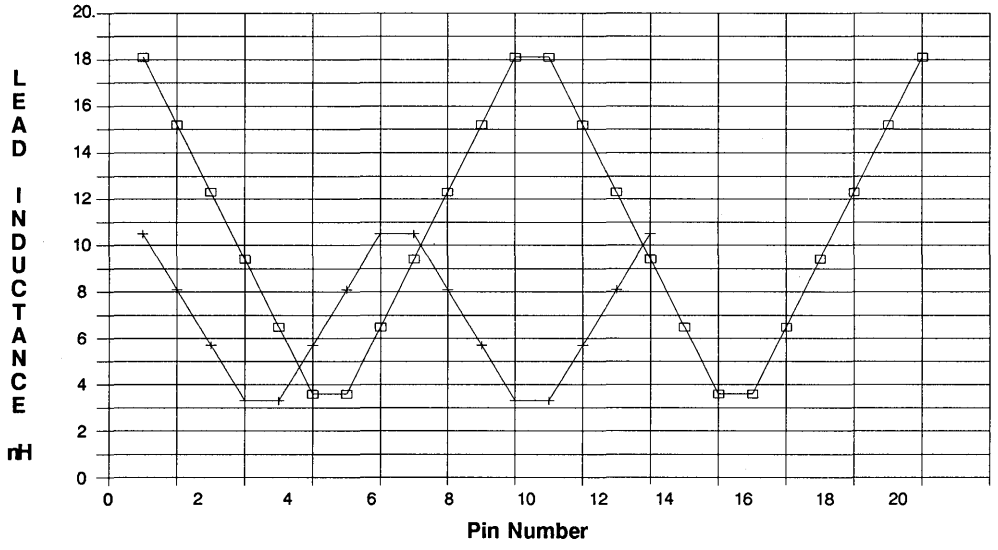


Figure 5b. Lead Inductance Per Lead for 16- & 24-Pin Plastic DIPs

High Performance Transmission Line Drivers

Introduction

The use of the 74F30XXX Family devices in high performance printed circuit board applications requires an understanding of some fundamental transmission line principles. It is assumed that you have some background in transmission line theory. Because of the unique requirements of every system, specific PC board design techniques will not be covered. The Signetics ECL Manual has some good background information on high performance PC board design.

This Application Note is intended to provide enough practical information to utilize the significant high performance advantages of the 74F30XXX Family in driving low impedance, high performance PC board transmission lines.

Incident wave signal switching of a transmission line requires the driver be able to achieve and maintain initial TTL input logic levels without having to wait for a signal reflection. The driver must also be able to continue to supply enough sinking and sourcing current to guarantee good noise margin during line reflections or crosstalk.

With standard TTL buffers unable to support incident wave switching, waiting for a reflection before a driver can achieve solid TTL input logic levels would be a major source of system timing error and noise. The reflected signal will take several nanoseconds to return to the driver source. During this time, the incident signal level could be in the input threshold region of a receiving gate creating the potential for that gate to oscillate or detect incorrect logic states.

PC board busses and backplanes usually have low, irregular characteristic impedances, Z_0, and are difficult to terminate properly (See Figure 6). To obtain incident wave switching of TTL voltage levels in this environment requires very high current drivers. Where proper termination is impractical, the 74F3037/40 Totem-Pole Output Gates could be the only solution. They can drive unterminated transmission lines of $Z_0 \geq 30\Omega$.

All 74F30XXX devices can drive properly terminated, low impedance transmission lines. When the line is correctly terminated, during the LOW-to-HIGH output transition, the driver output (whether open collector or totem-pole) will switch to V_{EQ} (the equivalent termination voltage) in <2ns, as if it were driving a resistor network tied directly to the output. If the V_{EQ} is less than 5V, the Family can also drive line impedances lower than 30Ω (See Figure 6b):

$$Z_0 = dV/I_{OL} = [V_{EQ} - V_{OL}]/I_{OL}$$

where:

V_{OL} = 0.5V @ I_{OL} = 160mA
Z_0 (V_{EQ} = 5.0V) = [5.0V - 0.5V]/160mA ≅ 30Ω
Z_0 (V_{EQ} = 3.0V) = [3.0V - 0.5V]/160mA ≅ 16Ω

When a buffer or transceiver is placed in the middle of a 70Ω PC board (typical) bus transmission line, its output sees two paralleled 70Ω impedances or 35Ω. With this heavy loading, standard TTL buffer outputs cannot generate TTL input logic level. However, the 74F30XXX Family was developed specifically for these types of difficult bus driver applications.

Characteristic Impedance

A driver switching the voltage onto a transmission line will see neither capacitance nor inductance but primarily resistance. This resistance, Z_0, is the characteristic impedance of the transmission line. The characteristic line impedance is calculted by:

$$Z_0 = \sqrt{[L_D/(C_D + C_i)]}$$

where: (See Figure 6)

C_D = Distributed Capacitance Per Unit Length
C_i = Total Input Capacitance Per Unit Length
L_D = Distributed Inductance Per Unit Length

In large device arrays such as memory PC boards, C_D, C_i and L_D (and therefore Z_0) are determined primarily by both the pitch of the package pins and the pitch the package placement rather than the number of devices attached to a bus. Example, SIP (single in-line packages) memory chips can be placed much closer together than

Figure 6a

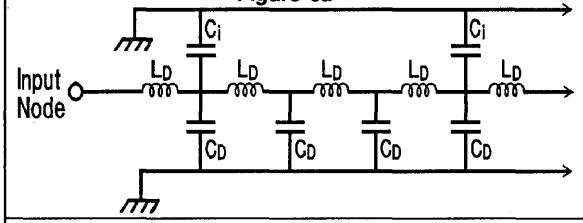
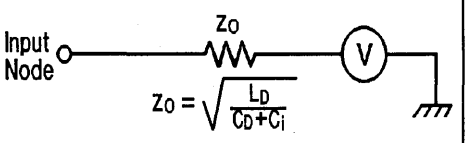


Figure 6b



a.... A simplified signal bus or transmission line model showing the first 2 DRAM inputs on the line. C_i is a DRAM's input capacitance. C_D is the distributed PC trace capacitance. L_D is the distributed PC trace inductance.

b.... Equivalent circuit for the Input Node. If Z_0 is given by the equation shown. The current to drive the Input Node is: $I_{OL} = V_{EQ}/Z_0$, where V is the difference between the Input Node voltage and the quiescent voltage on the line.

Figure 6. Transmission Line Model

can DIPs. Therefore, the input capacitance per unit length of the PC trace, C_i, can be much larger for SIPs than for DIPs, which reduces Z_o. Also, the newer surface mount packaging technologies tend to produce transmission lines with lower characteristic impedance than through-hole (DIP/SIP) technologies.

Line Propagation Delays & Reflections

The basic resistive characteristic of Z_o and the signal propagation speed of transmission lines, regardless of their termination, is a function of its cross section area and distributed/mutual L & C. The line termination determines only the magnitude and polarity of the reflected signal, not the initial impedance seen by a bus driver.

Three rules of thumb:

- Modern PC board designs can easily produce transmission lines with Z_o of 70Ω or lower.
- Signal propagation speeds will be in the 1.5ns per foot range. Although, with very large distributed input capacitance per unit length (C_i), 4.5-5.0ns/ft is possible.
- An abrupt change in Z_o causes a signal to be partially reflected. $V_{(reflected)}/V_{(incident)}$ is determined by the impedance immediately before and after the change. The magnitude of the propagated and reflected signal voltages will be::

$$V_{(ref)} = V_{(inc)}[(Z_1 - Z_0)/(Z_1 + Z_0)]$$
$$V_{OUT} = V_{(inc)} + V_{(ref)}$$
$$= 2V_{(inc)}[(Z_1)/(Z_1 + Z_0)]$$

where:

$V_{(ref)}$	=	Reflected Signal Voltage
$V_{(inc)}$	=	Incident Signal Voltage
V_{OUT}	=	Total Propagated & Reflected Signal
Z_o	=	Incident Line Z_o
Z_1	=	Next Section Line Z_o

Also, because of the real-world limitation of PC board design, the characteristic impedance of a line will change at different points along the line. These impedance variations will cause reflections. However, since the driver only has one shot at incident wave switching of a line (at the driving point), the signal wave traveling away from the source should initially encounter the lowest line impedance followed by incrementally increasing or the same characteristic impedances, if possible.

When the transmission line's Z_o decreases, the propagating signal voltage will be reduced and a negative reflection generated. Also, if the propagating signal sees an increase in Z_o, the signal voltage will be increased and a positive reflection voltage will be generated.

Incident Wave Switching Line Drivers

When comparing logic families, you will find that the 74F30XXX drivers are the only products available which are able to handle incident wave switching into a 30Ω transmission line. Under very heavy loading, the 74F3037/40 outputs produce significantly greater HIGH logic level noise margin than any competing standard device.

The 74F3037/40 has been designed specifically for the higher current and speed requirements of high performance PC board busses and transmission lines where the Z_o may have significant variations. Their totem-pole output structure provides enough current drive capability to force TTL input logic levels into a 30Ω load tied to either V_{CC} or GND.

Figure 7 illustrates the excellent noise immunity provided by the totem pole output structure of a 74F3037 output (P_0) driving a 40", 30Ω transmission line terminated with only the input of another 74F3037 (P_1). The 40" line's propagation delay is about 5ns or t_{TPD} = 1.5ns/ft. The waveforms are simplified to illustrate the concept. In an actual system, you could expect to see many small reflections traveling along the transmission line.

Since the line is nearly an open circuit at P_1, the 4.0V HIGH-to-LOW output transition tries to double when it arrives at P_1 (+5ns), driving P_1 negative until the input clamp is forward biased. This signal is reflected back to the P_0 source (+10ns), pulling it below ground momentarily.

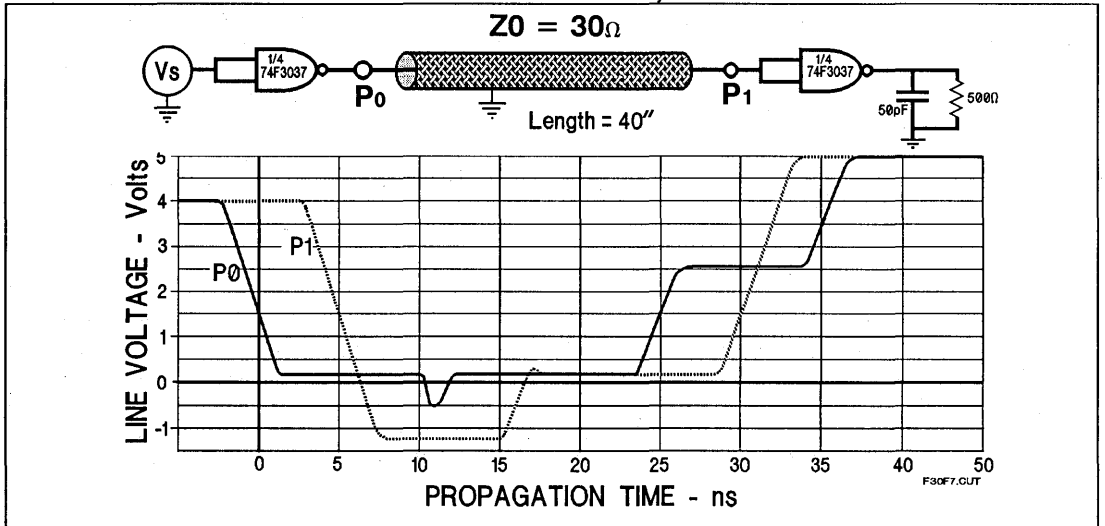


Figure 7. 74F3037/40 Driving Unterminated 30Ω Transmission Line (Simplifed

At the LOW-to-HIGH output transition, the 74F3037 initially achieves a full 2.5V level before running out of steam. The 2.5V signal travels down the line to P_1 (+5ns) where it is doubled and reflected. The reflected signal arrives back at P0 (+10ns), reenforcing the HIGH level to nearly 5.0V and completely turning off the 74F3037 pull-up structure. With the pull-up structure OFF, no additional charge can be pumped into the line, and the line voltage stops rising.

Open Collector Buffers & Transceivers

Figure 8 is an illustration of a typical multi-tap 70Ω transmission line with each end terminated by a resistive voltage divider producing a V_{EQ} = 3.0V and R_{EQ} = Z_0 = 70Ω. As shown, one of the B_N port outputs of a 74F30245 Open Collector Octal Transceiver (with no output pull-up resistor) can be placed anywhere along the middle of a transmission line (PC board trace). This output has to drive the equivalent of two paralleled 70Ω ($Z_0/2$ = 35Ω) transmission lines tied to 3.0V.

During the LOW-to-HIGH driver output transition, the OC driver output turns OFF, and the signal snaps up to 3.0V in less than 2ns. The output reacts as if it were tied to a 3.0V, 35Ω resistive termination. No reflections of the incident signal voltage occur from either end of the transmission line because both are terminated with Z_0. These terminations also absorb the HIGH-to-LOW output transition signal voltage without reflection.

Crosstalk

Crosstalk signals or injected noise can be inductively and/or capacitively coupled between two parallel signal lines. Crosstalk between adjacent transmission lines can be significant with large mutual inductance and capacitance even when the ends of the transmission lines are correctly terminated or tied to a line driver. Crosstalk noise travels down a transmission line (similar to actual data) and is absorbed or reflected at the terminations at each end of the line.

Crosstalk noise is a basic characteristic of the physical layout of adjacent transmission lines, not a failure of the driver. Long parallel signal lines can have a fairly high mutual inductance and capacitance if care is not taken in their design. The increased crosstalk due to narrower spacing between lines could pose system problems as denser memory and surface mount technology (SMT) packaging become more popular.

Shielding should be used to reduce the electromagnetic and electrostatic field strengths between adjacent lines. Multilayer PC boards significantly reduce mutual inductance and capacitance by isolating signal planes from each other through the use of alternating signal and ground planes. Further isolation can be achieved by inserting narrow, grounded filaments between each signal line on the same wiring plane.

Concerns that the 74F30XXX Family can produce more crosstalk is valid. However, the Family was specifically designed to drive large amounts of output current at very high speeds. Therefore, PC board design must take into consideration the high output current and fast edge rates generated by 74F30XXX devices.

Negative Reflections Cause MOS Failures

If the minimum input voltage specification of -1.0V is exceeded, the reliability of MOS devices can be seriously degraded. Transmission lines using end termination techniques should be incorporated into high performance PC board designs to minimize the negative excursion of reflected signals. Correct line termination is essential to prevent blowing up MOS device I/O ports connected to PC board bus lines!

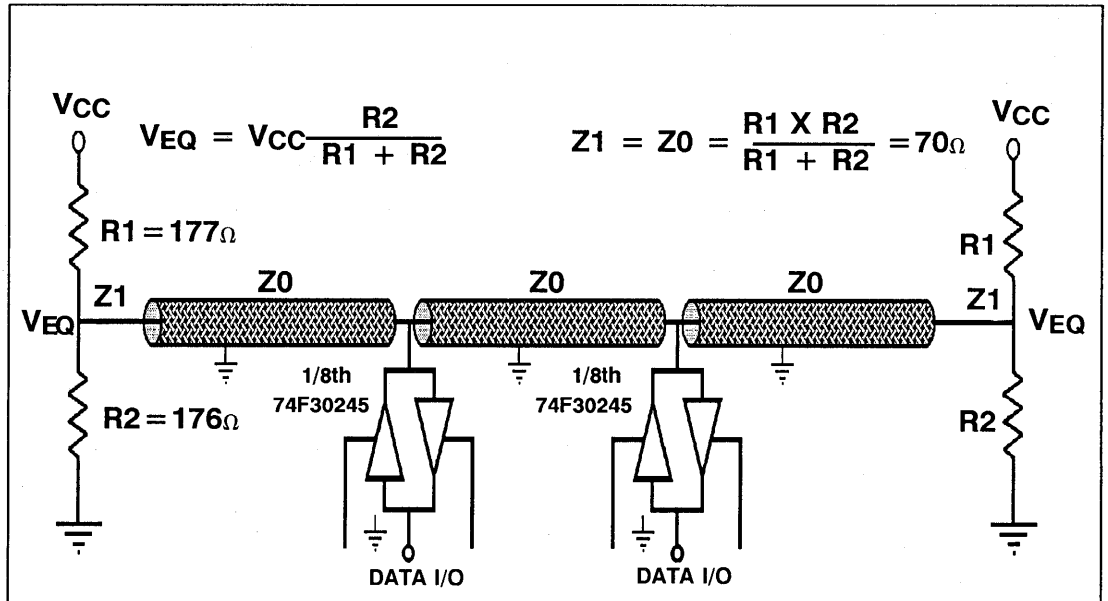


Figure 8. 74F30245 Multiple-Tap, Correctly Terminated 70Ω Transmission Line Transceiver

Applications of the 74F30XXX Family AN213

Summary of Recommendations

Significant factors influencing PC board designs are easily overlooked. Here are a few recommendations that must be taken into consideration:

- Keep signal line lengths as short as possible to reduce crosstalk, reflections and signal timing skews. Break long lines into shorter parallel lengths.
- In applications where there can be significant variations in Z_o, use 74F3037/40 Totem-Pole output drivers. If possible, terminate a transmission line with an impedance that is equal to or slightly higher than the Z_o at the terminal end of the line. If variations in Z_o must occur, Z_o should increase as the distance from the driver increases. Try to keep the incremental Z_o changes per unit length of transmission line to a minimum.
- To keep the negative reflected voltage at the I/Os of MOS devices less than 1.0V, correctly terminate the end(s) of the signal transmission line. For additional protection, you can also use the Schottky clamp diodes available across all I/O pins of Signetics' 74FXXX and 74F30XXX devices.
- The most elegant solution to driving low Z_o transmission lines is to use the Signetics 74F30XXX Octal Open Collector Output Buffers and Transceivers. If both ends of the line are terminated with its characteristic impedance (Z_o), these drivers can be tapped into any point along the line. Direct and injected crosstalk signals are absorbed at the end terminations minimizing system noise. The line driver will see heavy, predominantly resistive loads.
- Since you now need the speed and drive capabilities of the 74F30XXX Family, you are automatically in the high performance end of the speed spectrum. In these high-speed applications, multi-layer PC boards are virtually mandatory. Keep the ground paths as wide and as short as possible to minimize induced ground noise.
- Capacitively bypass the supply pins of all devices with a 0.1 - 0.33μF ceramic and/or tantalum capacitor as close to the supply pins as possible.

High Current Driver Applications

Figure 9 illustrates that under controlled conditions, the open collector 74F30240 and 74F30244 Octal Buffers can be used to drive eight power MOSFETs, lamps (incandescent and LED), solenoids and relays.

Octal Power MOSFET Driver

Power MOSFETs are well known for their extraordinary switching speeds -- much faster than the best power bipolar transistors of equivalent current/voltage handling capabilities. When comparing MOSFETs to equivalent power bipolar transistors, MOSFETs exhibit many advantages:

- Turn ON & OFF in 2ns vs. Bipolar's 200ns
- Negative vs. Positive Gain Tempco --- No Thermal Run-Away Characteristic
- Gate Turn-ON Thresholds Between 2V and 6V
- Low R_{ON} with 0V V_{DS} offset vs. $V_{CE(OFFSET)}$ > 0.15V
- R_{ON} < 0.15 Ohm @ I_{DS} > 10A
- Voltage-to-R_{ON} vs. Current-to-Current Amplification
- Capacitive AC Input vs. Current Base Drive Equivalent Gate Capacitance < 2000pF
- Low Cost 50V to 250V Power Transistors @ > 12A

The rise/fall switching speeds of MOSFETs are of primary consideration in high efficiency switching applications such as switched mode power supplies. The 74F30244 Buffer can easily switch an equivalent power MOSFET gate capacitance of 1000pF in <50ns.

An excellent example of today's leading edge power MOSFETs is the Siliconix BUZ71. At 25°C, the BUZ71's specifications are:

- V_{GSON} = ON Gate-Source Threshold < 5.0V
- I_{DSON} = Drain-Source ON Current > 12A
- V_{DSO} = Drain-Source Breakdown Voltage > 50V
- R_{DSON} = Drain-Source ON Resistance < 0.150Ω
- C_{GS} = Gate-Source Capacitance < 650pF
- C_{DG} = Drain-Gate Capacitance < 160pF
- P_{DSON} = Chip ON Power Dissipation < 22W
- P_L = Power to Load = 500W

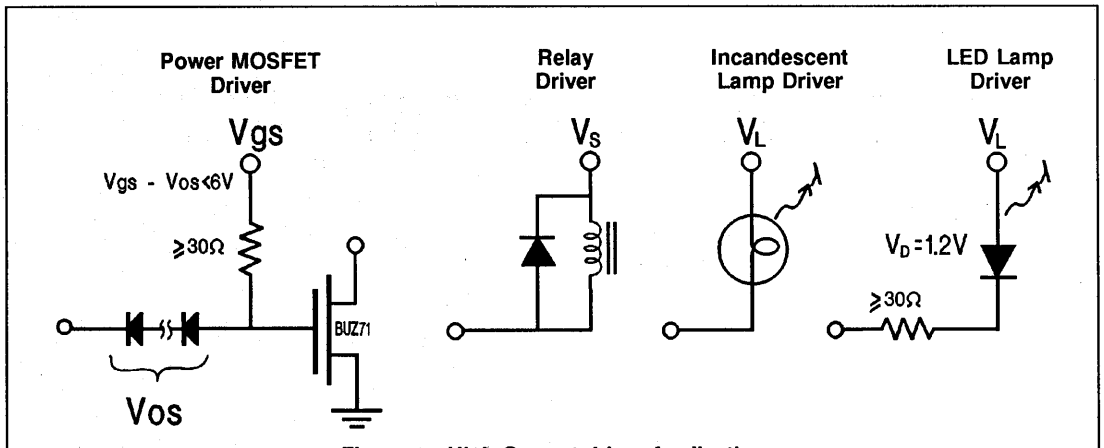


Figure 9. High Current driver Applications

The high current capabilities of the 74F30244 can easily drive the AC loading of the 650pF gate-source capacitance and 160pF drain-gate Miller capacitance. However, an offset voltage (V_{OS} = 3 Schottky diodes or more) should be provided to speed the LOW-to-High transition and increase the gate supply voltage. Since power MOSFETs are very fast and an oscillating driver could cause load switching problems, a non-inverting driver (such as the 74F30244) should be used to take advantage of the dynamic input threshold hysteresis generated by ground bounce.

Octal Solenoid or Relay Drivers

Since solenoids and relays are inductive circuit elements, the ON load current exponentially increases from zero to quiescent value of current. When the driver tries to turn OFF the load current, a quenching diode, placed across the coil, prevents the output of the driver from being damaged by the coil's back-EMF inductive kick.

A 74F30240 can easily handle eight 160mA, 5V solenoid or relays with the back-EMF diodes in place.

Octal Incandescent Lamp Drivers

All incandescent lamps have positive filament resistance temperature coefficients. At room temperature, a lamp's filament resistance can easily be less than 10% of its ON resistance. Therefore, a 100mW (5V at 20mA) lamp could have a cold or inrush current of 200mA. The absolute maximum output LOW current specified for the 74F30XXX Family is 320mA. For this reason, we suggest that the inrush not exceed 320mA in incandescent lamp applications. Therefore, assuming a 10:1 ON:OFF resistance ratio, the ON current should be in the 32mA range. Outputs may be paralleled for additional output drive current.

When the lamp is turned ON, the initial filament current exponentially decays to the quiescent ON current within 10 to 100ms depending upon its size. When the lamp is turned OFF, the thermal decay time constant is very long compared to the turn-ON time constant, greater than 100 times, since the filament, being in a vacuum, has a very high thermal resistance. Therefore, the only time the inrush or cold filament current must be taken into consideration is in applications in which the lamp is OFF for seconds.

Octal LED Lamp Drivers

LEDs (Light Emitting Diodes) have none of the inrush current problems of incandescent lamps. Low cost LEDs are available with spectral emissions from infrared (IR) to green. The intrinsic forward-biased diode voltage drop ranges from 1.2V to 1.6V, depending on the technology -- GaAs, GaAsP, as well as other mixtures. Visible LEDs, red-yellow-green, are used as indicators and don't require fast switching times. If the design requires low cost, high current octal LED drivers, the 74F30240/244 Buffers are excellent solutions.

IR LEDs are used in communications applications where the receiver is a photo-sensitive semiconductor material. Silicon PIN diodes make excellent, very high- speed receivers for emmissions of IR LEDs. Both the emitter's spectral energy output and the receiver's maximum spectral sensitivity are in the 900Å range. The 74F3037 is an ideal Fiber Optic Communications (FOC) IR LED transmitter driver.

Fiber Optic Communications (FOC)

74F3037 FOC LED Driver

High performance, low cost FOC LED transmitter drivers using the 74F3037 can achieve data rates greater than 170MBaud depending upon the length of the fiber optic cable. Using 5% tolerance components, 1/2 of a 74F3037 and a Hewlett-Packard HFBR-1402.4 FOC LED, a one kilometer, 170MBaud FOC link can be produced with an optical output pulse width distortion of less than 15% (See Figure 10). Since the FOC LED is much harder to turn ON than OFF, the 74F3037's fast, HIGH level turn ON and large pull-up output current is nearly an ideal combination for high-speed fiber optic communication. The peaking capacitor, C, compensates for the LED's slow turn-ON time and peaks the LED's light output during both the ON and OFF transitions. Contact Hewlett-Packard's Optical Communication Div., San Jose, CA, for more information on FOC LED transmitters, PIN photo diode receivers and fiber optic cable.

FOC Photo PIN Diode Receiver

The receiver consists of an HP HFBR-2208 Photo Pin Diode driving a Signetics NE5212 Transimpedance Current, Differential Amplifier followed by a Signetics 10116 Triple ECL Line Receiver. The Trans-Z Amp's ~7KΩ (single-ended) internal feedback resistance converts the PIN diode's photon generated currents into 100mV differential output swings. The NE5212's outputs are capacitively-coupled into the input of the 3-stage ECL amplifier where it is quantized into solid ECL logic levels in the last stage.

The NE5212 Trans-Z Amp has a nearly flat DC-to-120MHz bandwidth. Contact Signetics Linear Division for more information on this and many other FOC products.

One more important point ---- the cost of this FOC transmitter/receiver pair is less than $50 using off-the-shelf standard parts.

Figure 10a. FOC Transmitter

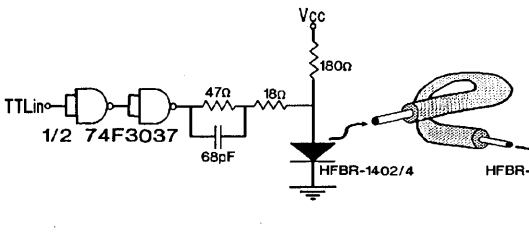


Figure 10b. FOC Receiver

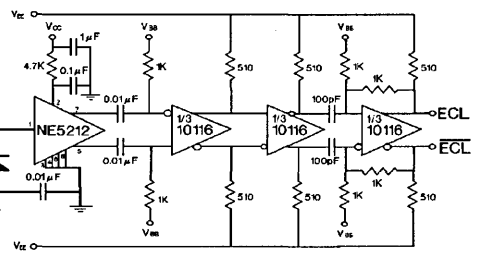


Figure 10. 74F3037 Fiber Optic Communications Applications

Signetics

AN214
74F Extended Octal–Plus Family Applications

Application Note

Standard Products

74F Extended Octal-Plus Family Features

- 8-, 9- & 10-Bit "Light–Load" Bus Products
  - Buffers/Drivers
    - With & Without Latches or Registers
    - With & Without 8–Bit Parity Checker/Generator
  - Tranceivers
    - With & Without Dual Registers
    - With & Without 8–Bit Parity Checker/Generator
- Patented "Light–Load" Inputs:
  - Input Current = ±20μA per Input
  - Transceiver I/O Pins = ±70μA
- High Performance Output Drive Currents:
  - I_{OL} = 64mA/48mA @ ±5%/10% V_{CC}
  - I_{OH} = –15mA/–3mA @ ±5%/10% V_{CC}
- "Flow–Through" or "Broadside" I/O Pin-Configuration
- Ideal for MOS CPU, Peripherals and Semi-custom Bus Interface
- 24-Pin, 300mil, Plastic Slim-DIPs
- High Performance Buffers – – – – – $t_{P(max)}$ = 7.5ns
- High Performance Latches/Registers – f_T = 100MHz

Introduction

The 74F Extended Octal–Plus© Family incorporates all of the latest Signetics' octal, 9–bit and 10–bit buffer, transceiver, latch and register functions. All devices in this Family utilize the Signetics patented "Light–Load" NPN, ±20μA input current structure and have "Flow–Through" or "Broadside" input/output pin configurations where the inputs and outputs are lined–up on opposite sides of a standard 24–pin Slim–DIP package. The "Light–Load" inputs, "Broadside" design and high functional density/performance of the Family make this product line ideal for buffering the limited drive capabilities of standard, custom and semicustom MOS VLSI devices to the rigorous environments of today's leading edge high performance logic designs. The Family also is an excellent choice for all general interface applications.

"Flow–Through" Design

The "Flow–Through" or "Broadside" chip layout/package design is illustrated in Figure 214–1 showing the Block Diagrams and Pin Configurations of the 74F828 10–Bit Inverting Buffer. Note that all of these "Broadside" designs allow logic signals to flow into one side and out of the other without crossing or folding back on signal paths such as the 74F240 Octal Buffers (Figure 214–2). If you compare the physical layout requirements of the path of PC board bus lines for the 74F828 to that of the 74F240's "Zig-Zag" path, you will see the significant advantages of the 74F Extended Octal–Plus© Family's "Flow–Through" design in simplifying the design and layout of large, high density, bus–oriented PC boards.

The 24–Pin, 300mil Slim–DIP Solution

With the advent of advanced Schottky TTL technology came the ability to significantly increase the functional density of standard logic building blocks. However, not until the development of the 24–pin, 300mil Slim–DIP package was it possible to take full advantage of these new chip densities. The entire Family provides significant advantages in package count, pin count and packing density when compared to older technologies. Further density enhancements can be achieved by using Signetics' surface mounted packages.

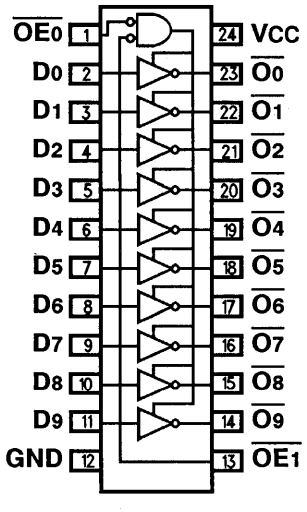


Figure 214-1. 74F828 Broadside Pin Configuration

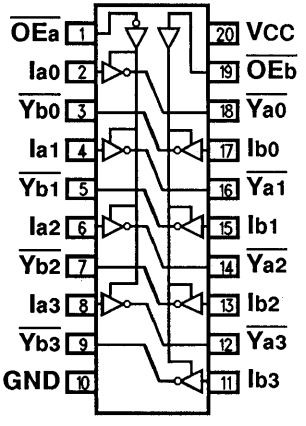


Figure 214-2. 74F240 "Zig-Zag" Pin Configuration

74F Extended Octal-Plus Family Applications AN214

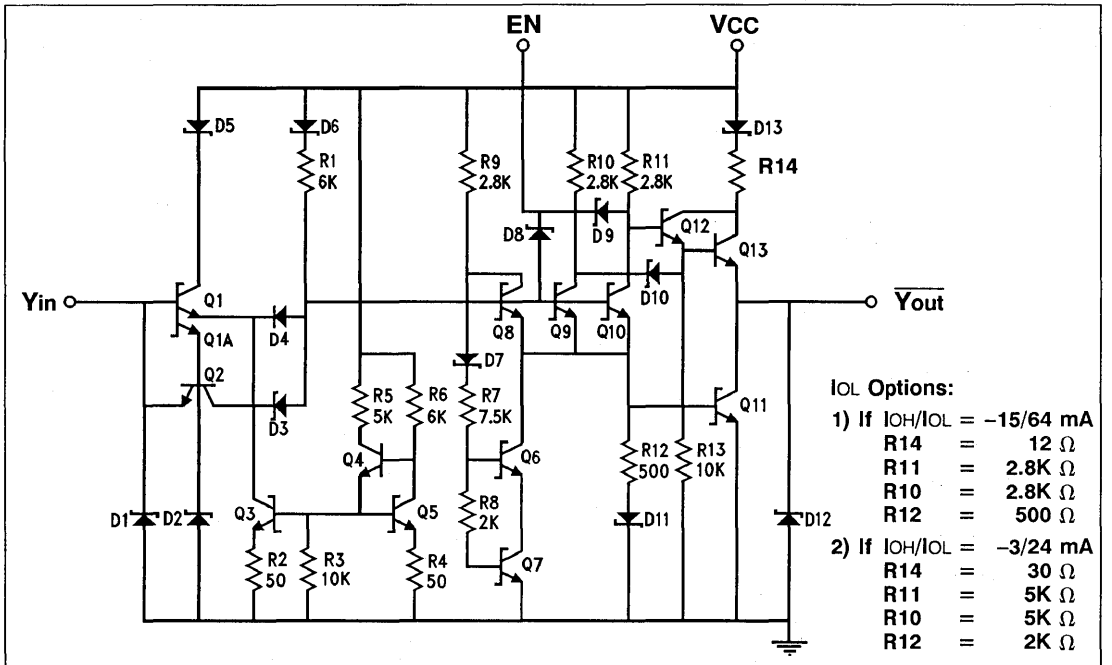


Figure 214–3. 74F455 Buffer/Drive Cell Circuit Diagram

By combining high functional density into a 24–pin, 300mil Slim–DIP package, the Signetics 74F Extended Octal–Plus© Family allows the reduction of PC board parts count and cost while optimizing layout with "Broadside" chip designs, reducing total system power dissipation and increasing system reliability.

The 8-, 9- & 10-Bit Series 24–Pin Solution

Whether your system requires an 8-, 9- or 10-bit bus interface, the Extended Octal–Plus© Family has standardized solutions in 24–pin/Slim–DIP/Broadside input/output packages with corner power supply pins (12 & 24) and standard designations for common control functions located at or near the package corners. Octals offer more mode control inputs than do the 9- or 10–bit products. Virtually all Family devices with 3–State outputs are guaranteed to source/sink –15/64mA @ V_{OH}/V_{OL} = 2.0/0.55V (Except for the 74F841–846 Latched Drivers which are spec'ed at –15mA/48mA). The A_N port outputs of several of the Family's transceivers are guaranteed to supply –3mA/48mA).

The Octal Parity Bus Series offers several notable exceptions to the above standard pinouts. This Series has three parts with two center–package ground pins to minimize ground–bounce noise. All outputs (except the A_N port of the 74F657 Parity Bus Transceiver spec'ed at –3mA/24mA) are guaranteed to source/sink more than –15mA/64mA.

Table 214–1. Family Output Drive Capabilities using the 74F657 Parity Bus Transceiver

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions, V_{IL} = MAX and V_{IH} = MIN)

PARAMETER			TEST CONDITIONS		Min	Typ	Max	UNITS
V_{OH}	HIGH–level Output Voltage	All Outputs	I_{OH} = –3mA	±10%V_{CC}	2.4			V
V_{OH}	HIGH–level Output Voltage	All Outputs	I_{OH} = –3mA	±5%V_{CC}	2.7	3.4		V
V_{OH}	HIGH–level Output Voltage	B_N Port, PARITY $\overline{ERROR}$	I_{OH} = –15mA	±10%V_{CC}	2.0			V
V_{OH}	HIGH–level Output Voltage	B_N, PARITY $\overline{ERROR}$	I_{OH} = –15mA	±5%V_{CC}	2.0			V
V_{OL}	LOW–Level Output Voltage	A_N Port	I_{OL} = 24mA	±10%V_{CC}		0.35	0.50	V
V_{OL}	LOW–Level Output Voltage	A_N Port	I_{OL} = 24mA	±5%V_{CC}		0.35	0.50	V
V_{OL}	LOW–Level Output Voltage	B_N Port, PARITY, $\overline{ERROR}$	I_{OL} = 48mA	±10%V_{CC}		0.40	0.55	V
V_{OL}	LOW–Level Output Voltage	B_N Port, PARITY, $\overline{ERROR}$	I_{OL} = 64mA	±5%V_{CC}		0.40	0.55	V
I_{OS}	A_N Output HIGH Level Short Circuit Current (R14 = 30Ω)			V_{CC} = MAX.			–150	mA
I_{OS}	B_N Output HIGH Level Short Circuit Current (R14 = 12Ω)			V_{CC} = MAX.			–225	mA

74F Extended Octal-Plus Family Applications AN214

Current PC board, multi-layer technology make it possible to take into consideration the physical location of input/output pins, transmission line characteristics and supply power distribution. Lining up all inputs and output on opposite sides of the package allows the address, data and control bus signal to flow in a direct physical path from the μP CPU through the bus interface chips and onto the appropriate bus. This "Broadside" bus design approach produces very clean PC board layouts and may, in fact eliminate an entire PC board interconnection layer. Standardization of power supply, mode control and input/output pins whether 8-, 9- or 10-bit bus functions permits simplified, structured PC board layout.

Input Structures

Referring to Figure 214-3, the 74F455 Inverting Buffer/Driver Cell Circuit Diagram is an example of the Family's input and output circuitry. The patented Signetics "Light-Load" NPN input structure (Q1/3/4/5, R1/2/3/4/5/6 & D4) and turn-OFF speed-up circuit (Q2 & D2/3) are used throughout the 74F Extended Octal-Plus© Family. The "Light-Load" NPN input is actually a high speed, differential amplifier with the reference side, the anode of D4, clamped at two diode voltage drops above ground (BE junctions of Q8/9/10 and Q11 of ~1.4V at 25°C). When the V_{IH} rises above this clamp voltage, the BE junction of Q1 is forward based allowing beta amplified, CE current to flow into the <1.0mA constant current source, Q3 (driven by Q4/5 & R2/3/4/5/6) . The beta of Q1 is guaranteed, by design, to be >50, thereby, guaranteeing that the input base bias current will be <20μA. The emitter of Q1 rises to $1V_{BE}$ (~300mV) below the V_{IH}, reverse biasing D4 and permitting Q8/9/10 base bias current to flow through R1.

The patented turn-OFF circuit consisting of Q2 and D2/3 produces a dynamic speed to help turn Q8/9/10 OFF quickly. During the time that the Q1 is turned-ON (input = V_{IH} >2.0V), the reverse-biased Schottky diode, D2, acting as a capacitor, will be charged to the voltage at the emitter of Q1A or $1V_{BE}$ voltage drop below the input (>2.0 – $1V_{BE}$). When the input in switched to <V_{IL} (or <0.8V), the D2 stored charge discharges through the BE of Q2. Q2 CE current through D3 rapidly turns Q8/9/10 OFF.

These circuit innovations produce high performance, very low input bias current (±20μA) gate inputs. This input leakage represents a 30X reduction over the standard 74F Family's 600uA input current with virtually no loss in speed. The 74F Extended Octal-Plus© Transceivers have an input loading current of ±70μA which is the combination of the "Light-Load" NPN input structure's ±20μA and the 3-State Hi-Z output's ±50μA leakage current.

The low "Light-Load" input current and high speed performance make this Family ideal for interfacing to low drive capability, slower MOS CPU, peripherals and semi-custom chips used in most of today's state-of-the-art logic designs. Besides very low input current requirements, this "Light-Load" input has another significant advantage over "traditional" input structures: Very lower input capacitance (smaller stored charge) due to very small devices geometries. Therefore, when Extended Octal-Plus devices are connected to a bus, they present less AC bus loading and do not significantly lower the characteristic impedance of the bus to the extend "traditional" input structures do. Thus, the amount of the AC current a bus driver has to produce to change the state of the bus is lowered and in many cases can make a difference between incident wave switching of the bus vs. losing time waiting for a reflected wave.

The Signetics 74F "Light-Load" Input Structure is discussed in more detail in Application Note AN215.

Output Drive Capabilities

Virtually all devices in the Extended Octal-Plus© Family are guaranteed to source/sink more than -15mA/64mA @ V_{OH}/V_{OL} = 2.0/0.55V. One exception is the 74F841-thru-846 Series of Bus Interface Latches which are specified at -15/48mA. Several of the Family's transceiver products have lower A_N output drive

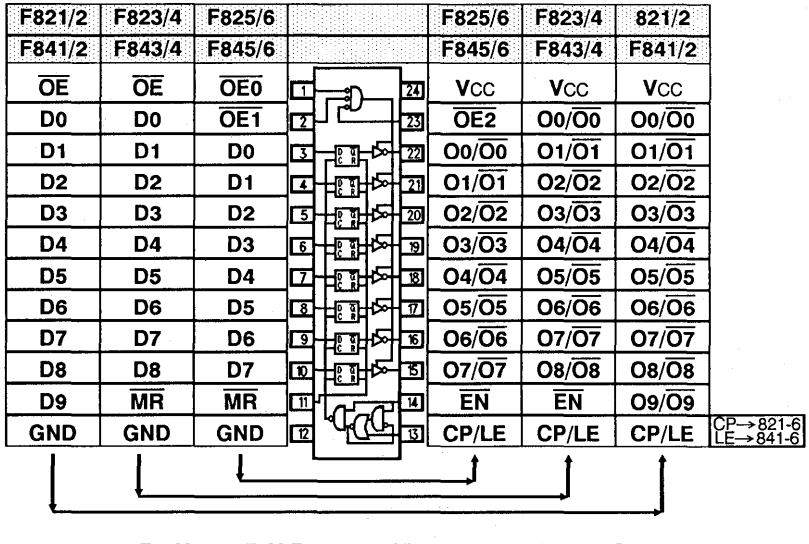


Figure 215-4a. 74F82X & 74F8X Registered/Latched Buffer Pin Configurations

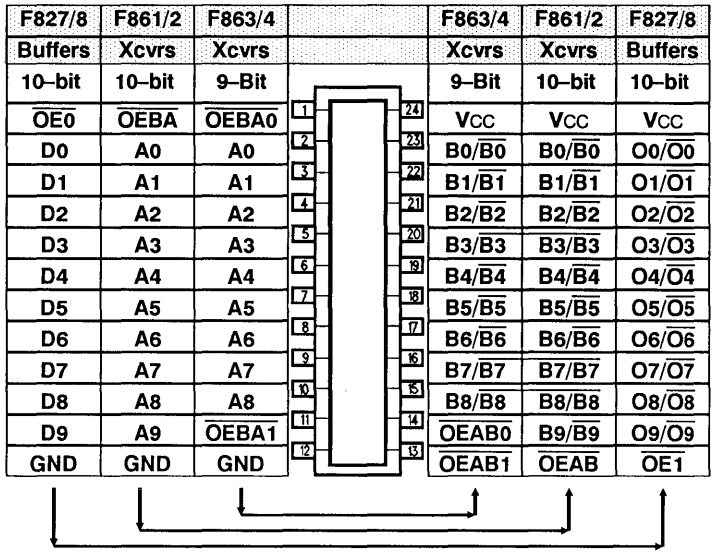


Figure 214-4b. 74F827/8 & 74F861–4 Buffers & Transceivers Pin Configurations

capabilities to reduce package power dissipation. Refer to Tables 214–1 and 3.

For example, the 74F657 Parity Bus Transceiver has two output ports with different capacities: The A_N port is guaranteed to source/sink –3mA/24mA (I_{OH}/I_{OL} = 2.4/0.50V), and the B_N port has an output drive capability of –15mA/64mA at 2.0V/0.55V. The 74F657's A_N port is designed to interface the chip side of the PC board to the backplane bus, while the B_N Port is capable of driving a transmission line or bus backplane line.

Referring to Figure 214–3, all of the Family's 3-State, totem–pole output structures have a Schottky blocking diode, D13, in their pull–up output structures. These diodes block leakage current from flowing into the outputs when V_{CC} is either open or shorted to ground.

This gives a very important advantage of being able to power down a PCB (or several PCBs) without disabling the bus and even without producing any glitching on the bus due to an undesired

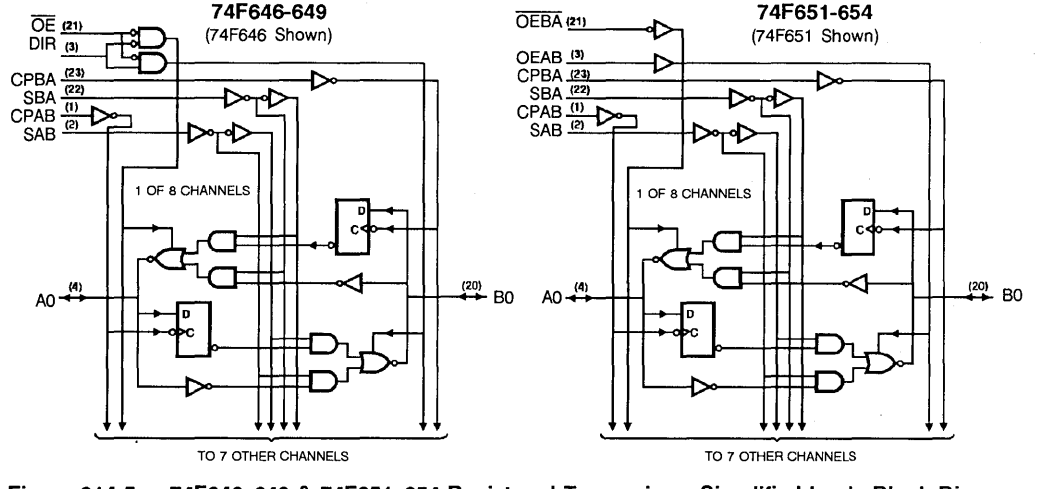


Figure 214-5a. 74F646–649 & 74F651–654 Registered Transceivers Simplified Logic Block Diagram

74F Extended Octal-Plus Family Applications AN214

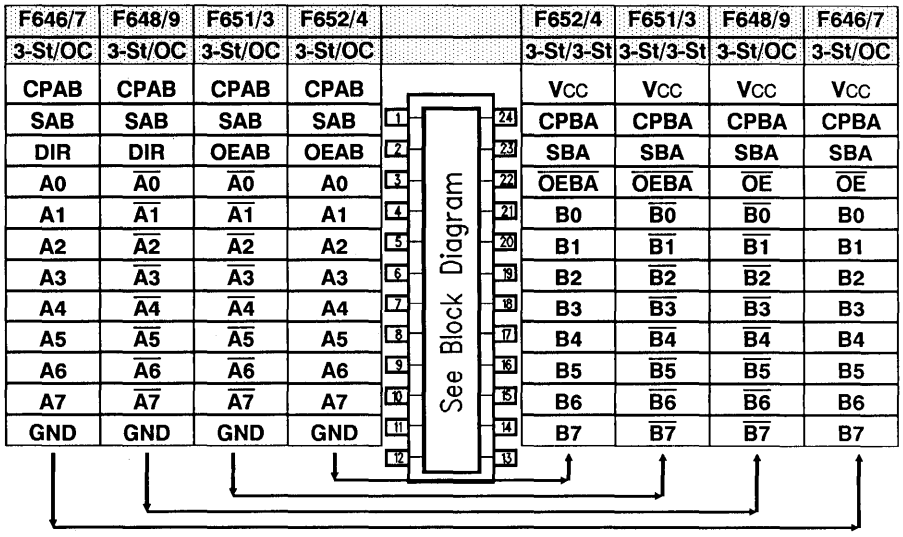


Figure 214-5b. 74F646–649 & 74F651–653 Dual Registered Transceivers Pin Configurations

change in the output state of the device being powered down.

The output short-circuit (Ios) limiting resistor (R14), the anode-to-cathode resistance/voltage drop of D13 and the collector-to-emitter/base-to-emitter resistance/voltage drop of Q13 limit the amount of current that can be sourced from a HIGH level output at a specified V_{OH}. For most of the parts in the Family, R14 is equal to 12Ω. The An port of several of the transceivers utilize an R14 of 30Ω producing I_{OH} (@ V_{OH} = 2.0V) of -6mA versus -15mA from the BN ports 12Ω R14.

The output HIGH level sourcing current, I_{OH}, at a specified output voltage, V_{OH}, can be calculated by subtracting the voltage drops of D13, the pull-up darlington transistor, Q12/13, and the desired V_{OH} level from V_{CC} and dividing by the value of R14 plus the anode-to-cathode resistance of D13 and the collector-to-emitter/base-to-emitter resistance.

Assumptions:
$V_{D13} \cong 0.5V$ @ $R_{ON} = 3\Omega$ @ 25°C),
$V_{Q12/13} \cong 1.2V$ @ $R_{ON} = 8\Omega$ @ 25°C)
$I_{OH} = -[V_{CC}-(V_{D13}+V_{Q12/Q13}+V_{OH})]/(R14+R_{D13}+R_{Q13})$.
$I_{OH}(R14 = 12\Omega) = -[4.5V-(0.5V+1.2V+2.0V)]/23\Omega = -35mA$
$I_{OH}(R14 = 30\Omega) = -[4.5V-(0.5V+1.2V+2.0V)]/41\Omega = -20mA$
$I_{OS} = I_{OH}$ @ V_{OH} = 0.0V and V_{CC} = 5.5V
$I_{OS}(R14 = 12\Omega) = -[5.5V-(0.5V+1.2V)]/23\Omega = -165mA$
$I_{OS}(R14 = 30\Omega) = -[5.5V-(0.5V+1.2V)]/41\Omega = -93mA$

Obviously, we have been very conservative in the I_{OH} specification to guardband against all conditions of temperature and input/output/supply voltage levels. The R_{ON} resistances of the output pullup transistors and blocking diode are large enough to prevent Ios from exceeding -225mA for R14 = 12Ω and -150mA for R14 = 30Ω. (Refer to Table 214-1)

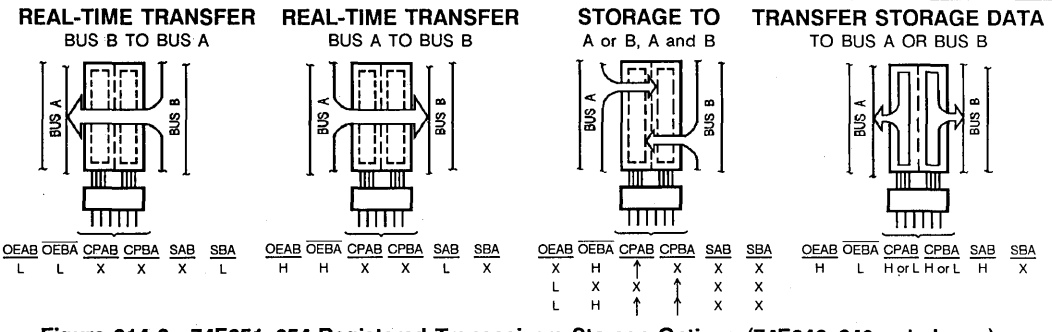


Figure 214-6. 74F651–654 Registered Transceivers Storage Options (74F646–649 not shown)

74F Extended Octal-Plus Family Applications AN214

Table 214–2. Parity Bus Family vs. The Competition

PART NUMBER	DESCRIPTION	TOTAL # of PINS	t_{PDmax}* IN to OUT	t_{PDmax}* IN to PARITY	I_{CCmax}**	POWER PINS	BROADSIDE DESIGN
74F455/F456 vs. 74F240/F244 + 74F280	Octal Parity Buffer	24	7.5ns	16.0ns	110mA	Center	Yes
		38	7.5ns	14.5ns	125mA	Corner	No
74F655A/F656A vs. 74F240/F244 + 74F280	Octal Parity Buffer	24	7.5ns	16.0ns	110mA	Corner	Yes
		38	7.5ns	14.5ns	125mA	Corner	No
74F657 vs. 74F240/F245 + 74F280 + 1 AND Gate	Octal Parity Transceiver	24	7.5ns	16.0ns	110mA	Center	Yes
		38	8.0ns	14.5ns	125mA	Corner	No

NOTES:
* = Propagation Delays of DATA IN-to-DATA OUT and IN-to-PARITY OUT, T_A = 0° to 70°C, V_{CC} = +5.0V±10%, Output Load = C_L = 50pF & R_L = 500Ω
** = Worst Case Power, T_A = 0° to 70°C, V_{CC} = +5.0V±10%, Output Load = C_L = 50pF & R_L = 500Ω

74F821 – 74F863 Series

The 74F821 through 74F863 Series of Octal, 9-bit and 10-bit Buffers, Latch Buffers, Register Buffers and Transceivers are standardized around the AMD 298XX series with one significant difference – the Signetics' "Light-Load" NPN input offers a 50:1 reduction in input loading (1000uA vs. 20μA). This Series illustrates the standardized on 24-pin/300mil Slim-DIP packages, "Broadside" input/output pinouts and control function pins. All 74F8XX 3-state outputs are guaranteed to source/sink –15mA/64mA, except for the 74F84X Latched Buffers which are specified at –15/48mA.

The logic diagram and pin configurations of the 74F828 Non-Inverting 10-Bit Buffer (Figure 214–1) and the 74F821–826 and 74F841–6 Registered/Latched Buffers (Figure 214–4a) are excellent illustrations of the standardized pin configuration illustrating "Broadside" chip design.

Figure 214–4b shows the pin-outs of the 74F827/8 Buffers and 74F861–4 Transceivers. There currently are no 9-bit buffer offerings in this Series.

Registered Transceivers Series

The 74F646–9 and 74F651–4 Octal Dual-Registered Transceivers offer a "Light-Load" combination of a 74F245 type transceiver with two 74F373/374 type octal registers within a 24-pin, Slim-DIP, Broadside input/output package. This Series offers a significant 6:1 package count reduction advantage over older technologies.

Figure 214–5a shows the 74F646 and 74F651 Transceivers Simplified Block Diagrams, and this Series' Pin Configurations are depicted in Figure 214–5b. Figure 214–6 graphically illustrates four optional storage and transfer modes of the 74F651 Octal, Non-Inverting, 3-State, Dual-Registered Transceiver. The 74F651 will be used to explain the operation of the entire Series. The 74F646/8 (3-State, INV/NINV) and the 74F647/9 (O.C., INV/NINV) Octal Dual-Registered Transceivers offer optional signal direction control logic and output enable to the 74F651–4 series.

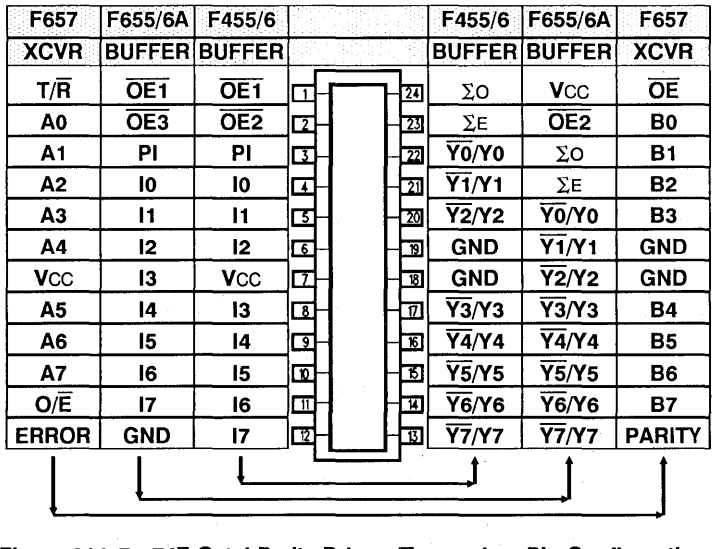


Figure 214–7. 74F Octal Parity Drivers/Transceiver Pin Configurations

74F Extended Octal-Plus Family Applications AN214

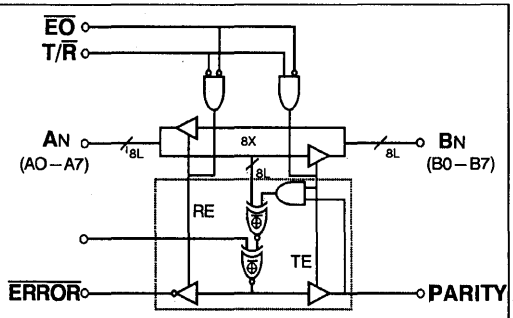


Figure 214–8a. 74F657 Simplified Block Diagram

This Series allows you to store or real-time transfer data in either direction through the transceiver function. Data at the A_N port can be stored in either the A_N port register or the B_N port register and, then, can be transferred either from the A_N port register to the B_N port outputs or from the B_N port register to the A_N port outputs.

The same capabilities are available to data presented to the B-port. When a port's output buffers are enabled ($\overline{OE}$ = LOW and DIR = LOW for A_N outputs enabled or HIGH for B_N outputs enabled), the SXX select inputs (SAB and SBA) control the two EX-OR gates allowing the output port data to come either directly from the other port (real-time transfer) or from the other port's input storage register.

The CPAB and CPBA inputs are the LOW-to-HIGH edge-triggered clock inputs for the A_N port register and B_N port register. Data presented to either port's inputs can be clocked into its input register on a LOW-to-HIGH CPXX input regardless of the logic levels on any of the other mode control inputs.

The 74F651-4's OEAB and $\overline{OEBA}$ output enable inputs may be tied together to enable the B_N outputs when HIGH or A_N outputs when held LOW or can be used separately to independently control the two output ports. Tying the 74F651-4's OEAB and $\overline{OEBA}$ together is logically equivalent to the DIR input of the 74F646-9.

Parity Bus Series Advantages

The increased functional density of the Parity Bus Series produces a 2:1 package reduction (plus 1 AND gate) and, therefore, 38:24 pin reduction. Power dissipation savings of 82.5mW for the 74F455/456/655A/656A Drivers and 137.5mW for the 74F657 are also achieved through shared internal logic. Table 214-2 shows the package/pin advantage as well as the worst case propagation delays and I_{CC} of the Family versus their competition.

Figure 214-7 is a summary of the pin configurations of entire Parity Bus Drivers and Transceiver Series.

The 74F455/456/655A/655A Octal Parity Bus Drivers and the 74F657 Octal Parity Bus Transceiver Series combines the popular Signetics 75F24X buffer/transceiver functions with the 74F280 9-bit Parity Generator/Checker, "Broadside" input/output pin configurations, "Light-Load" inputs and an increased guaranteed sink/source capabilities of −15mA/64mA for low impedance bus environments. The 74F445/446 Drivers with their multiple center-package ground supply pins are logically identical to the 74F655A/656A Drivers except for the latters' single corner-package supply pins and an additional $\overline{Output\ Enable}$ input. The 74F657 Parity Bus Transceiver allows the parity to be generated and checked in both directions in a single package replacing one 74F245 Transceiver, 20-pin DIP and two 74F280, 16-pin DIPs plus a couple of gates.

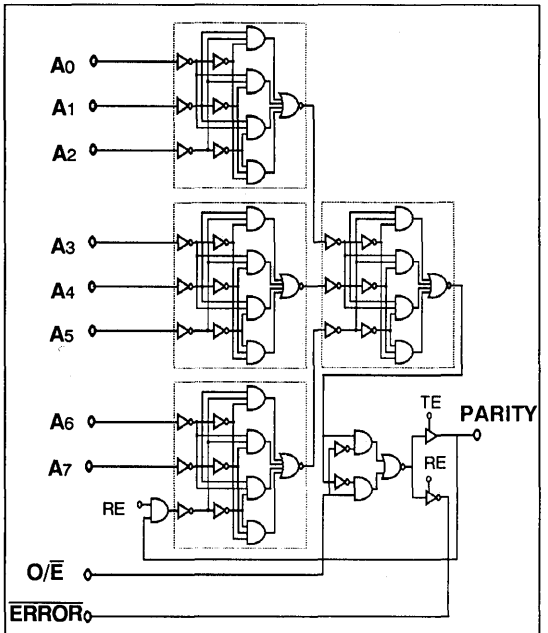


Figure 214–8b. 74F657 Parity Tree Logic Diagram

74F657 Operation

The 74F657 Parity Bus Transceiver, as shown in its simplified logic diagram Figure 214-8a, is a combination of a 74F245 Octal Transceiver and a 74F280A 9-Bit Parity Generator/Checker plus one AND gate. Figures 214-8b expands the logic block diagram of the Family's Parity Tree Logic (inside the dashed line of Figure 214-8a).

During TRANSMIT mode (A_N = Hi-Z), the PARITY and $\overline{ERROR}$ outputs are generated from the A_N input/output port. In the RECEIVE mode, the B_N port is the input from the system or mother board bus (B-port outputs = Hi-Z).

For best speed performance, PARITY should always be generated from the A_N port for the B_N port (TRANSMIT mode), and parity $\overline{ERROR}$ should always be checked for data coming in on the B-port (RECEIVE mode). EVEN or ODD parity generation and checking is determined by the EVEN/$\overline{ODD}$ input (EVEN = HIGH & ODD = LOW).

In the TRANSMIT mode (T/$\overline{R}$ = HIGH), transmitted data travels from the A-port to the B-port in less than 8.0ns generating a PARITY bit output in less than 16.0ns. Whereas, in the RECEIVE mode (T/$\overline{R}$ = LOW), received data traverses from the B-port to the A-port path in, again, less than 8.0ns, but then, the $\overline{ERROR}$ checking output, being generated from the output data presented to the A-port and the PARITY input, takes an additional 16.5ns or less to

74F Extended Octal-Plus Family Applications AN214

stabilize. Therefore, the total RECEIVEd-data-to-$\overline{\text{ERROR}}$ checking output propagation time is the sum of the B_N-to-A_N delay (8ns) and the A_N/PARITY-to-$\overline{\text{ERROR}}$ output delay (16.5ns) or 22.5ns.

However, in many cases, the propagation delay that has to be taken into consideration does not have to include parity calculation time and could be equal to that of just the transceiver part (8ns). This is due to the fact that it may not be too late to interrupt whatever needs to be interrupted in case of a parity error after the data has already gone by (i.e. via late bus error).

Parity Tree Analysis

The basic 3-Input Comparator Cell, inside the dashed line in Figure 214-8b, is used throughout the Parity Bus Series. If there are an even number of HIGH inputs (0 or 2) the output of the 3-input Comparitor Cell will be HIGH, while an odd number (1 or 3) will produce an output LOW. The 74F657's Parity Tree Logic, combines four of the 3-Input Comparators with a 2-input comparator, a 2-input AND gate and output buffers for PARITY and $\overline{\text{ERROR}}$ to produce the complete parity generator/checker logic.

The 74F588 IEEE-488 Octal Transceiver

The 74F588 is a non-inverting IEEE-488 standard transceiver contains eight bidirectional 3-state buffers. The B_N port outputs can source/sink -15mA/64mA (guaranteed) and have series termination resistors as specified in the IEEE-488 specification. The A_N port, which interfaces to the PC board or system logic bus, is guaranteed to source/sink -3mA/24mA. The 74F588 pinout in identical to that of the 74F545 Octal Transceiver with the IEEE-488 termination resistors in series with the B_N port.

Metastability in Latches and Registers

Interfacing a basically asynchronous real-world with synchronous logic systems can and does cause many circuit designer headaches. The problem: latches and registers which are normally considered to have only two stable states (High and Low) actually have a third – The METASTABLE State. This third operating point occurs when the cross-coupled latch is exactly balanced. This state is only stable when there is no noise on the chip which would tend to destablize the perfect energy balance between the bistable states of the latch. Refer to Figure 214-9.

Metastability can occur when input data violate the setup time or hold time specifications at the clocking or strobing edge of the synchronizing clock input. With no system noise the latch can't decide "yes or no" so it is possible for the latch to "go metastable" or "maybe." With noise on the chip, random energy will "nudge" the latch toward one of its "bistable" states – HIGH or LOW. This metastable state time can range from nanoseconds to milliseconds. With today's very high performance logic families, the metastable condition can last for perhaps 1000 times the latch's normal propagation delay time. A metastable latch has an unpredictable delay time during which the output is between logic levels. This metastable state can easily last more than 50ns with today's high performance logic families and WILL cause systems to "crash" if great care isn't taken with asynchronous, real-world interfacing.

The D-type latch shown in Figure 214-9 has DATA applied to NAND gate 1 and $\overline{\text{DATA}}$ applied to NAND gate 2. When the LE (Latch Enable) input is LOW, gates 1 & 2 outputs are HIGH and the G3/4 R-S latch is latched and stable. When LE is HIGH, the latch appears to be transparent to the DATA input – Q equals DATA. On the HIGH-to-LOW transition of LE, the DATA logic level that meets the latch's setup and hold time is stored in the latch.

If DATA changes during the setup time to hold time period, it is possible for both outputs of gates 1 & 2 to be in the input tresholds region of gates 3 & 4, respectively. Under these conditions, the latch (gates 3 & 4) could be perfectly balanced in the METASTABLE state. Eventually, chip and system noise will cause the latch to be force into a HIGH/LOW stable state.

The Extended Octal-Plus© Family, while not entirely immune, has been made metastable resistant by using design techniques which force the latch toward a stable state much more quickly than older bus interface families.

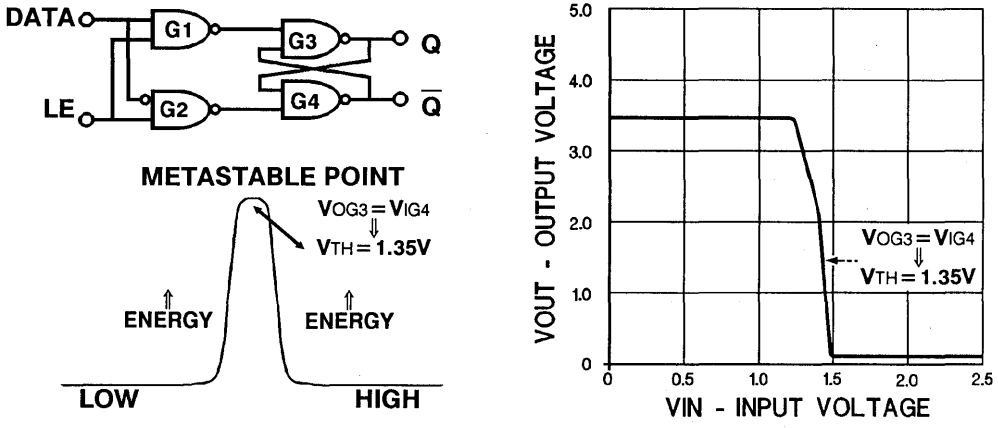


Figure 214-9. Metastability in Latches and Registers

Dual–Registered Transceiver Applications

Figure 214–10 illustrates how the 74F646–9 and 74F651–4 can be used to either synchronize data transfer between two systems or pipeline data. Data is stored in a register, then, while retreiving more data, the first data is read. When the second is available it can either be stored or read directly. Two slower systems can be multiplexed into a high speed system in the same way.

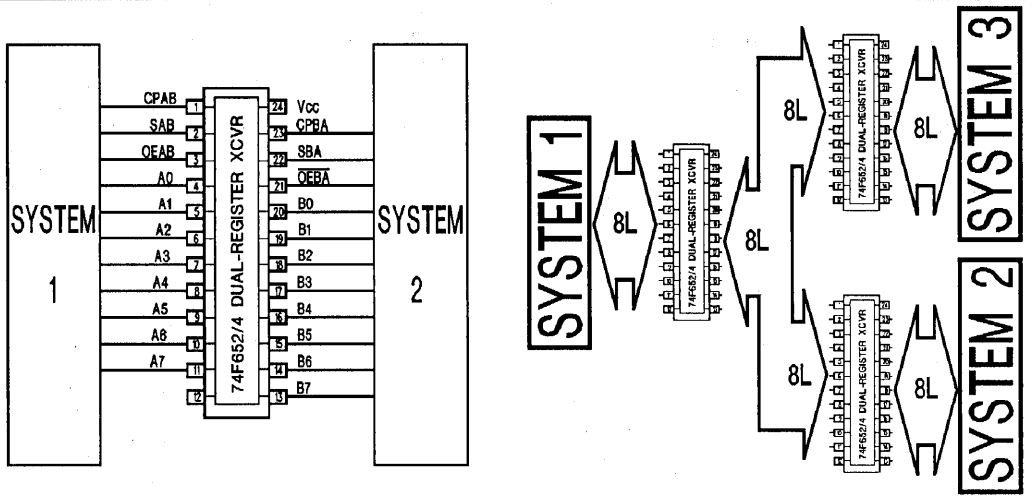


Figure 214-10. 74F Extended Octal–Plus© Dual–Registered Transceiver Applications

Parity Bus Transceiver Applications

Figure 214–11 illustrates the functional density advantages of the Parity Bus Series using the 74F657 in a typical microprocessor/data bus transceiver application. Note the 74F245 + 74F280A version would still require a 2–input AND gate and 3–state buffers for the PARITY and $\overline{\text{ERROR}}$ outputs. And, of course, it would require an order of magnitude higher input current than a single 74F657 would and would also introduce much higher capacitive loading (for both the bus and the microcontroller).

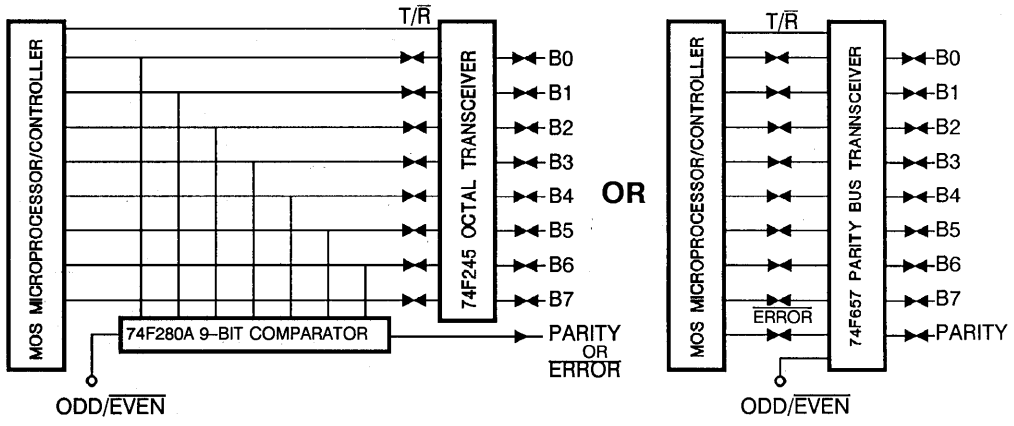


Figure 214-11 74F657 Parity Bus Transceiver Applications

74F Extended Octal-Plus Family Applications — AN214

Table 214-3 The Extended Octal-Plus© Family Capabilities Summary

Part Number	#-Bits	Polarity	Output	Brd-Side	I_{OH}/I_{OL} min	Storage	Speed	Parity	Comments
"Light-Load" Buffer and Line Driver Functions									
74F455/456	8-Bit	INV/NINV	3-St	Yes	−15/64mA	None	7.5ns	Yes	Multiple/Ctr Package GND Pins, Σ_E, Σ_O = −15/64mA
4F540/541	8-Bit	INV/NINV	3-St	Yes	−15/64mA	None	7.5ns	No	Broadside Pinout of F240
4F655A/656A	8-Bit	INV/NINV	3-St	Yes	−15/64mA	None	7.5ns	Yes	Σ_E, Σ_O = −15/64mA
74F827/828	10-Bit	NINV/INV	3-St	Yes	−15/64mA	None	9.0ns	No	
"Light-Load" Register and Latch Functions									
74F821/822	10-Bit	NINV/INV	3-St	Yes	−15/64mA	Reg	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enable}}$ & Clock EN Inputs
74F823/824	9-Bit	NINV/INV	3-St	Yes	−15/64mA	Reg	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enable}}$ & Clock EN Inputs
74F825/826	8-Bit	NINV/INV	3-St	Yes	−15/64mA	Reg	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enable}}$ & Clock EN Inputs
74F841/842	10-Bit	NINV/INV	3-St	Yes	−15/48mA	Latch	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enable}}$ & LE Enable Inputs
74F843/844	9-Bit	NINV/INV	3-St	Yes	−15/48mA	Latch	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enable}}$ & LE Enable Inputs
74F845/846	8-Bit	NINV/INV	3-St	Yes	−15/48mA	Latch	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enable}}$ & LE Enable Inputs
"Light-Load" Transceiver Functions									
74F545	8-Bit	NINV	A_N 3-St	Yes	−3/24mA	None	7.0ns	No	
			B_N 3-St	Yes	−15/64mA	None	7.0ns	No	
74F550/551	8-Bit	NINV/INV	B_N 3-St	Yes	−15/64mA	B_N-Reg	10.5ns	No	$A_N \rightarrow B_N$, ERROR , Status Registers, 50MHz
			A_N 3-St	Yes	−3/24mA	A_N-Reg	10.5-ns	No	$B_N \rightarrow A_N$, Multiple/Center Package GND Pins **
74F552	8-Bit	NINV	B_N 3-St	Yes	−15/64mA	B_N-Reg	10.5ns	Yes	$A_N \rightarrow B_N$, PARITY, $\overline{\text{ERROR}}$, Status Registers
			A_N 3-St	Yes	−3/24mA	A_N-Reg	10.5-ns	Yes	$B_N \rightarrow A_N$, Multiple/Center Package GND Pins **
74F588	8-Bit	NINV	A_N=3-St	Yes	−3/24mA	None	7.5ns	No	
			B_N 3-St	Yes	−15/64mA	None	7.5ns	No	IEEE-488/GPIB w/ Line Termination Resistors
74F620/623	8-Bit	INV/NINV	B_N 3-St	Yes	−15/64mA	None	7.5ns	No	$A_N \rightarrow B_N$
			A_N 3-St	Yes	−3/24mA	None	7.5ns	No	$B_N \rightarrow A_N$
74F621/622	8-Bit	NINV/INV	B_N OC	Yes	OC/64mA	None	13.0ns	No	$A_N \rightarrow B_N$
			A_N OC	Yes	OC/24mA	None	12.5ns	No	$B_N \rightarrow A_N$
74F640	8-Bit	INV	A/B 3-St	Yes	−15/64mA	None	7.5ns	No	$A_N \leftrightarrow B_N$
74F641/642	8-Bit	NINV/INV	B_N OC	Yes	OC/64mA	None	13.0ns	No	$A_N \rightarrow B_N$
			A_N OC	Yes	OC/20mA	None	12.0ns	No	$B_N \rightarrow A_N$
74F646/648	8-Bit	NINV/INV	A/B 3-St	Yes	−15/64mA	2 Reg	11.5ns	No	$A_N \leftrightarrow B_N$, Registers for A_N & B_N Ports, 80MHz (min.)
74F647/649	8-Bit	NINV/INV	A/B OC	Yes	OC/64mA	2 Reg	19.5ns	No	$A_N \leftrightarrow B_N$, Registers for A_N & B_N Ports, 40MHz (min.)
74F651/652	8-Bit	INV/NINV	A/B 3-St	Yes	−15/64mA	2 Reg	12.5ns	No	$A_N \leftrightarrow B_N$, Registers for A_N & B_N Ports, 80MHz (min.)
74F653/654	8-Bit	NINV/INV	B_N 3-St	Yes	−15/64mA	B_N-Reg	11.0ns	No	$A_N \rightarrow B_N$, B_N Port = 85MHz (min.)
			A_N OC	Yes	OC/64mA	A_N-Reg	20.0ns	No	$B_N \rightarrow A_N$, A_N Port = 45MHz (min.)
74F657	8-Bit	NINV	B_N 3-St	Yes	−15/64mA	None	8.0ns	Yes	$A_N \rightarrow B_N$, PARITY, $\overline{\text{ERROR}}$ = −15/64mA
			A_N 3-St	Yes	−3/24mA	None	8.0-ns	No	$B_N \rightarrow A_N$, Multiple/Center Package GND Pins
74F861/862	10-Bit	NINV/INV	A/B 3-St	Yes	−15/64mA	None	10.0ns	No	$A_N \leftrightarrow B_N$
74F863/864	9-Bit	NINV/INV	A/B 3-St	Yes	−15/64mA	None	10.0ns	No	$A_N \leftrightarrow B_N$
74F1245	8-Bit	NINV	B_N 3-St	Yes	−15/64mA	None	8.0ns	No	$A_N \rightarrow B_N$, "Light-Load" Pin-for-Pin F245 Replacement
			A_N 3-St	Yes	−3/24mA	None	8.0ns	No	$B_N \rightarrow A_N$
74F2951/2952	8-Bit	INV/NINV	A/B 3-St	Yes	−15/64mA	2 Reg	12.5ns	No	$A_N \leftrightarrow B_N$, Registers for A_N & B_N Ports, 80MHz (min.) **

NOTES: All parameters are worse-case, unless otherwise speified
- 3-St ⇒ 3-State
- OC ⇒ Open Collector
- Reg ⇒ LOW-to-HIGH Edge Clocked D-Type Register
- Latch ⇒ HIGH Logic Level on the Latch Enable Logic, Data Passes Directly Through D-Type Latch,
- ⇒ HIGH-to-LOW Logic Level Transition of the Latch Enable, Data is Stored in the D-Type Latch
- ** ⇒ These device utilize standard FAST input structures producing input currents of +20μA & −0.6mA.

Signetics

AN215

74FXXXX "Light Load" Input Products

Application Note

Standard Products

Major "Light-Load" Input Features

- Patented "Light-Load" NPN Input Structure
  - Normal Input Pins = ±20μA per input
  - Transceiver I/O Pins = ±70μA per I/O pin
  - Primarily Capacitive Loading = <10pF
- Ideal for MOS CPU, Peripherals & Semi-custom Bus Interfaces
- Patented Turn-OFF Speed-up Circuit
- No Significant Speed Disadvantage -- Standard 74F Speeds
- PC Board Transmission Line Drive Capability: -15/64mA I_{OH}/I_{OL}
- "Broadside" Design in 20-, 24- and 28-Pin Slim-DIP Packages
- "Light-Load" Family Includes:
  - 19 Buffers and Line Driver Parts
  - 19 Shift Register, Register & Latch Parts
  - 19 Transceivers (No Storage)
  - 8 Dual Registered Transceivers
  - 7 Arithmetic Functions

Introduction

The Signetics 74F "Light Load" product line is a high performance, TTL bus compatible series of very low input bias current (±20μA), buffer/driver, transceiver, register, multiplexer and arithmetic MSI functions. The patented "Light Load", ±20μA NPN input structure, shown in Figure 215-1, combined with a unique input speed-up circuit (also patented) makes this product line ideal for interfacing with all MOS devices, without any speed degradation. When compared to the I_{IL} of standard FAST inputs of 600μA (larger for some other logic families) this "Light Load" input shows a 30:1 reduction in I_{IL} loading (600μA/20μA).

These devices were specifically designed to meet the requirements of buffering low output drive MOS VLSI/LSI devices from the rigorous loading environment PC board/mother-board busses and system back planes. The "Light Load" inputs and improved speed performance make this product line ideal for interfacing to low output drive capability, slower MOS CPU, peripherals and semi-custom chips used in most state-of-the-art logic designs today's. Using these "Light Load" input bus products, MOS chip outputs will only have to drive the small amount of distributed PC trace capacitance and inductance loading. The MOS device output drive capability isn't wasted on drivers/transceivers with large DC input current drive requirements.

See Table 215-1 for a complete listing of the part numbers and functions of the "Light Load" product line.

"Flow-Through" Design

Figure 215-2 illustrates the pin configurations of the 74F84X Latched Buffer Series. Notice that all of the "Light Load" Input data bus products use a "Flow-Through" design which allows logic signals to flow into one side and out of the other without crossing or folding back on signal paths such as the 74F24X octal series. Comparing the physical PC board signal bus path layout required for the 74F845 Octal Registered Buffer to that of the zig-zag signal

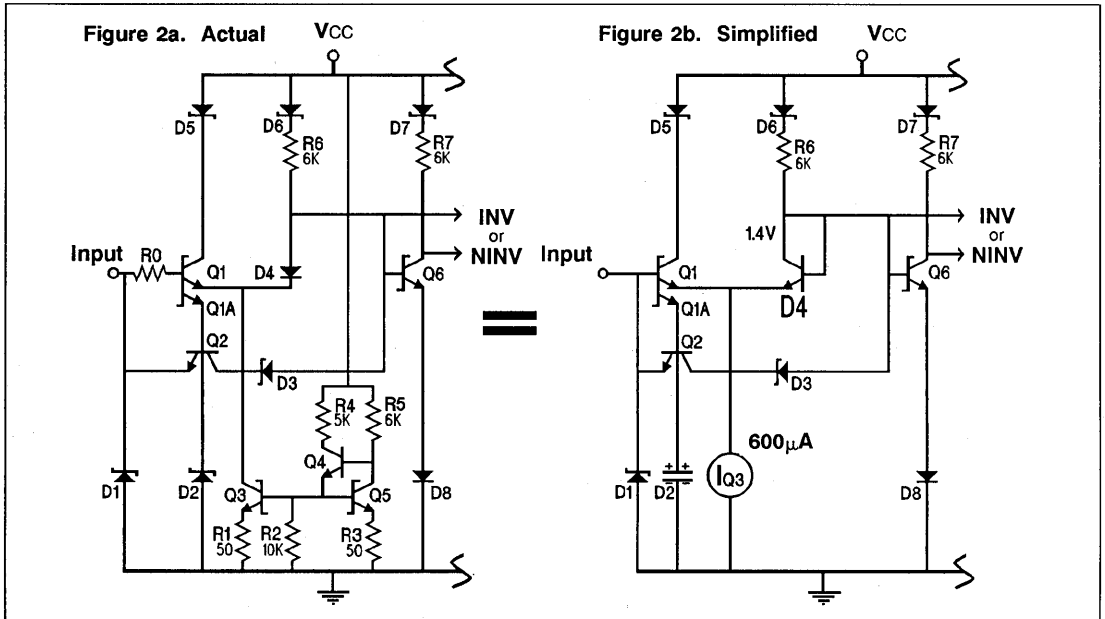


Figure 215-1. The "Light-Load" and Speed-Up Circuit Input Structure (Actual & Simplified)

The 74F "Light Load" Input Products AN215

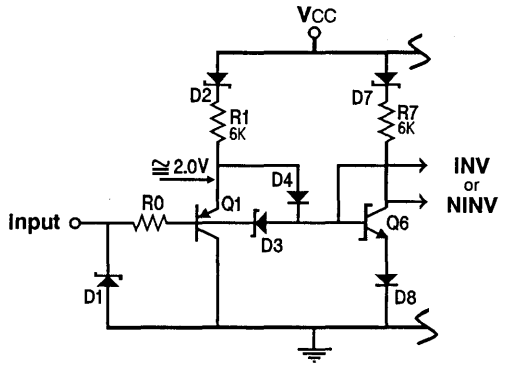


Figure 215-1c. Future "Light Load" PNP Input

path of the 74F240 Octal Inverting Buffer, you will see the significant advantages of the this product line's "Flow-Through" design in simplifying the design and layout of large, bus-oriented PC boards.

The "Light Load" Input product line combines "Flow-Through" design, high speed performance and high functional density into 20-, 24-and 28-pin, 300-mil Slim-DIP packages significantly reducing system propagation delays, parts count, power dissipation, PC board area/complexity and, therefore, total cost while enhancing total system reliability.

Input Structure - Differential Amplifier

Figure 215–1 shows the circuit diagram of the patented "Light Load" NPN Input (Q1/3, R6 & D4) and the Turn-OFF Speed-Up Circuit (Q2, D2 & D3). This input structure is actually a linear differential amplifier consisting of Q1, D4 and a constant current sink made up of Q3/4/5 and R1/2/3. The input bias current of this amplifier is less than $\pm 20\mu A$ for V_I between 0.0V and 5.5V. The Turn-OFF Speed-Up circuit (D2/Q2/D3) quickly discharges Q6's base-collector stored-charge to ground. The following analysis assumes room temperature and 5.0V_{CC} operation.

The Q1's base is the input side of the differential amplifier and D4's anode is the reference side. When the input is HIGH (2.0V), Q1 is turned-ON and I_{CE} plus I_{BE} current flows into Q3's constant current sink network of ~600μA. Since D4's anode is clamped at 1.3V to 1.4V by the V_{BE} of Q6 plus D8's voltage drop, and since Q1's emitter voltage is pulling the cathode of D4 up to greater than ~1.4V (the 2.0V_{IH} minus Q1's 0.6V_{BE}), R6's (6K) current can not flow through D4 and forward biases Q6's base-emitter.

Since Q6 is a Schottky clamped transistor, it has a V_{CEsat} ~0.5V. When Q6 is turned-ON by R6, the voltage at its collector drops to ~0.9V from ground (adding in D8 voltage drop) which turns-OFF the output totem-poll pull-down driver transistors and turns-ON the pull-up. This topic will be discussed in more detail in the next section (Refer to Figure 215-3).

Input Structure - Constant Current Sink

The constant current sink produced by Q3/4/5 and R1/2/3/4/5 sinks a relatively constant 600μA to ground. This "current mirror" circuit drives the base-to-ground voltage of Q3 and Q5 to Q5 V_{BE} plus the voltage drop across R3. Since Q3 and Q5 are identical, the voltage drops across R1 will equal that of R3. Therefore, the current

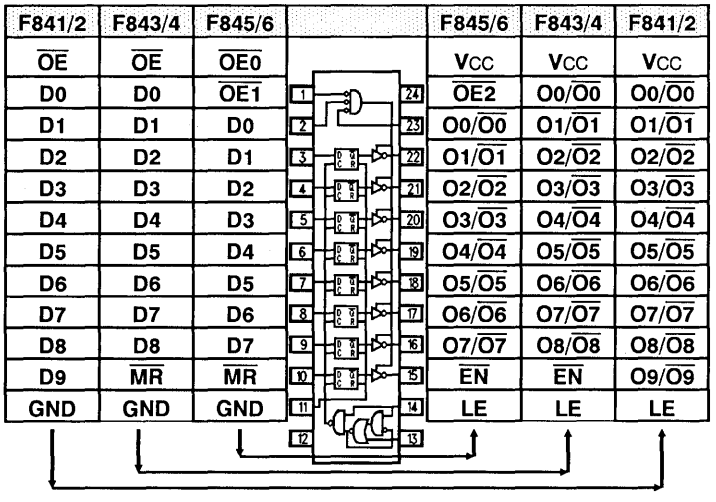


Figure 215-2. 74F84X Latched Buffer Pin Configurations

The 74F "Light Load" Input Products AN215

through R1 equal the current through R3 times the ratio of R3:R1.

The base bias currents for Q3 and Q5 is supplied by Q4. Because of the relatively high βs of Q3 and Q5 (>50), their base currents of ~10μA do not significantly effect the currents through R3 and R1 (β or BETA = transistor current gain). At 25°C and V_{CC} = 5.0V, R3's current is approximately equal to:

$I_{R3} = [V_{CC} - (V_{BE\text{-}Q4} + V_{BE\text{-}Q5})]/(R3 + R5)$

$I_{R3} = (5.0V - 1.2V)/(50\Omega + 6000\Omega) \cong 600\mu A$

Therefore:

$I_{CE\text{-}Q3} \cong I_{R1} = I_{R5} * (R3/R1) \cong 600\mu A$

With Q1's β also greater than 50, the HIGH logic level input bias current is less than 20μA:

$I_{OH} = I_{CE\text{-}Q3}/BETA_{Q1} \cong 600\mu A/>50) < 12\mu A$

The "Light Load" PNP Input

We will soon be introducing a new product line of "Light Load" PNP devices. One of the first products will be the 74F821 through 74F826 Registered Buffers which will have the same pin configurations and options as the 74F841 through 74F846 Latched Buffers (See Figure 215–2). The 74F82X series will provide a positive-going edge triggered clock input to its 8-, 9- and 10-bit register storage parts versus the 74F84X series' HIGH level Latch Enabled latches.

With Signetics' latest oxide-isolated process, a new, high performance "Light Load" PNP input structure will soon be available. This new PNP input, shown in Figure 215–1c, provides a high impedance AND input structure versus the NPN input OR input and reduces the chip power dissipation by eliminating the requirement for a constant current source for each input.

The PNP input is still a differential amplifier with the cathode of D3 referenced to 2 V_{BE} voltage drops from ground. When the input is HIGH ($V_{IH} \geq 2V$), no Q1 emitter–base current can flow because the anode of D3 is clamped to the 2 V_{BE}. As D4 forward biased with the current from R1, the output driver transistor (Q6) turns ON. When the input is LOW ($V_{IL} \leq 0.8V$), Q1's emitter–base junction is forward biased which turns ON the β amplified emitter–collector current of Q1. When Q1 is ON, the anode of D4 is clamped OFF by the input V_{IL} voltage plus Q1's emitter–base drop (V_{IL} + Q1V_{BE} $\leq 0.8V + 0.6V = 1.4V$). Therefore, the input threshold at the base of Q1 is ≅ 1.4V (2 V_{BE}) at 25°C.

With the β of Q1 typically greater than 100, the V_{IL} input bias current is guaranteed to be less than 20μA. With the input HIGH, the input leakage is also guaranteed to be less than 20μA. The β amplification of Q1 is basically the only difference between this PNP input's 20μA I_{IL} and the standard diode input's I_{IL} of 600μA.

When the base of Q1 is switched LOW, the Schottky diode D3 provides a turn-OFF speed-up path to ground which quickly discharges the base of the driver transistor (Q6).

Output Structures

A characteristic example of the output structures found throughout the 74FXXXX Light Load Product Line is the 74F657 Parity Bus Transceiver which has two basic output designs. Figure 215-3 illustrates the 74F657's output structure designs of these output structures: A_N Port's output (Figure 3b) is guaranteed to handle –3/+24mA (2.4/0.5V V_{OH}/V_{OL}), and the B_N Port (Figure 3a) can drive greater than –15/+64mA (2.0/0.55V V_{OH}/V_{OL}). The A_N port is

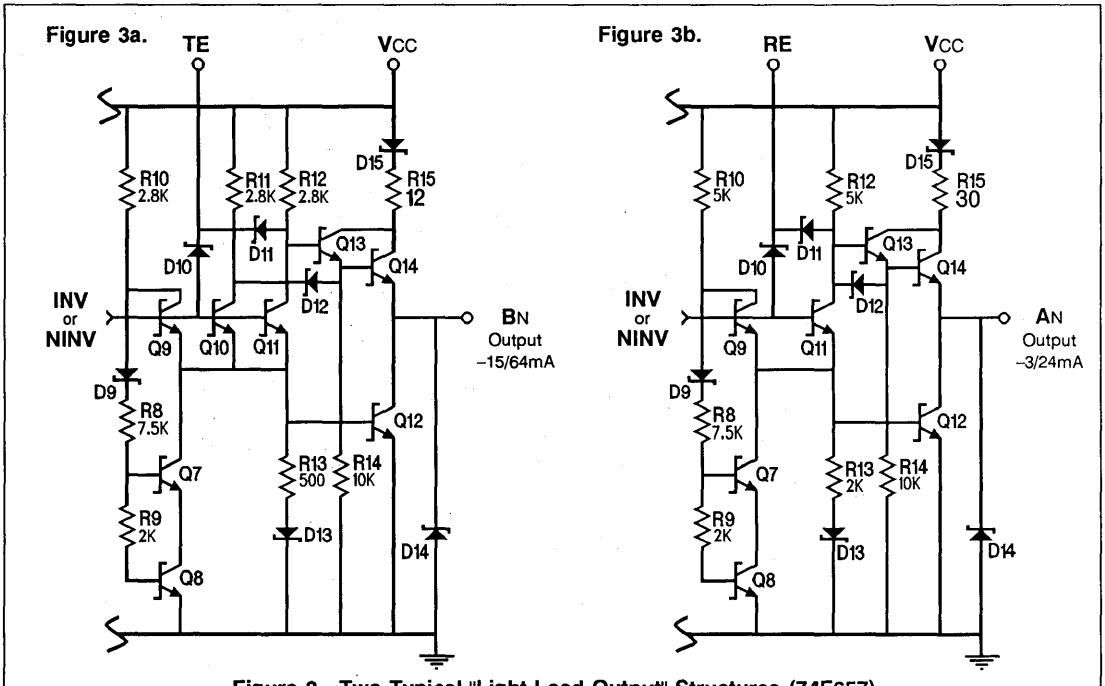


Figure 3. Two Typical "Light-Load Output" Structures (74F657)

The 74F "Light Load" Input Products — AN215

Table 215-1. 74FXXXX Light Load Input Products

Part Number	#-Bits	Polarity	Output	Broad-Side	I_{OH}/I_{OL} min	Storage	Speed	Parity	Comments
"Light-Load" Buffers and Line Drivers									
74F125/6	4-Bit	NINV	3-St	No	−15/64mA	None	6.5ns	No	Separate output enables (F125 = $\overline{EN}$ & F126 = EN)
74F365/6	6-Bit	NINV	3-St	No	−15/64mA	None	7.5ns	No	Common output enable
74F367/8	6-Bit	INV	3-St	No	−15/64mA	None	7.5ns	No	Two output enables controlling 3 outputs each
74F455/6	8-Bit	INV/NINV	3-St	Yes	−15/64mA	None	7.5ns	Yes	Multiple/Ctr Package GND Pins, Σ_E, Σ_O = −15/64mA
74F540/1	8-Bit	INV/NINV	3-St	Yes	−15/64mA	None	7.5ns	No	Broadside Pinout of F240
74F655A/6A	8-Bit	INV/NINV	3-St	Yes	−15/64mA	None	7.5ns	Yes	Σ_E, Σ_O = −15/64mA
74F804/1804	6-Bit	2I-NAND	3-St	No	−48/48mA	None	4.0ns	No	PNP Hex 2-InNAND Gate, F1804 has Ctr Supply Pins
74F805/1805	6-Bit	2I-NOR	3-St	No	−48/48mA	None	4.0ns	No	PNP Hex 2-Input NOR Gate, F1805 has Ctr Supply Pins
74F808/1808	6-Bit	2I-AND	3-St	No	−48/48mA	None	5.0ns	No	PNP Hex 2-Input AND Gate, F1808 has Ctr Supply Pins
74F827/8	10-Bit	NINV/INV	3-St	Yes	−15/64mA	None	9.0ns	No	
74F832/1832	6-Bit	2I-OR	3-St	No	−48/48mA	None	5.5ns	No	PNP Hex 2-Input OR Gate, F1832 has Ctr Supply Pins
74F1240/1	8-Bit	INV/NINV	3-St	No	−15/64mA	None	6.5ns	No	Light Load pin replacements for F240/1
74F1244	8-Bit	INV/NINV	3-St	No	−15/64mA	None	7.0ns	No	Light Load pin replacements for F244
74F30240/4	8-Bit	INV/NINV	OC	Yes	OC/160mA	None	15.0ns	No	Octal, 30Ω PC Board Data Transmission Line Driver
"Light-Load" Registers and Latches									
74F166	8-Bit	NINV	3-St	Yes	−1/20mA	S/R	110MHz	No	Serial/Parallel −In, Serial−Out
74F195	4-Bit	NINV	3-St	Yes	−1/20mA	S/R	110MHz	No	Serial/Parallel −In, Serial−Out
74F273	8-Bit	NINV	3-St	No	−1/20mA	S/R	120MHz	No	D-Type Flip−Flops
74F377	8-Bit	NINV	3-St	No	−1/20mA	S/R	100MHz	No	D-Type Flip−Flops
74F595	8-Bit	NINV	3-St	Yes	−3/20mA	S/R	80MHz	No	S or P−In, Serial-Out w/D-Register Output Storage
74F597	8-Bit	NINV	3-St	Yes	−3/20mA	S/R	80MHz	No	S or P−In, Serial−Out w/D-Register Input Storage
74F598	8-Bit	NINV	3-St	Yes	−3/20mA	S/R	80MHz	No	F597 w/Multiplexed Inputs and Outputs
74F821/2	10-Bit	NINV/INV	3-St	Yes	−15/64mA	Reg	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enables}}$ & Clock EN Inputs
74F823/4	9-Bit	NINV/INV	3-St	Yes	−15/64mA	Reg	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enables}}$ & Clock EN Inputs
74F825/6	8-Bit	NINV/INV	3-St	Yes	−15/64mA	Reg	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enables}}$ & Clock EN Inputs
74F841/2	10-Bit	NINV/INV	3-St	Yes	−15/48mA	Latch	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enables}}$ & LE Enable Inputs
74F843/4	9-Bit	NINV/INV	3-St	Yes	−15/48mA	Latch	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enables}}$ & LE Enable Inputs
74F845/6	8-Bit	NINV/INV	3-St	Yes	−15/48mA	Latch	100MHz	No	Data, $\overline{\text{Master Reset}}$, $\overline{\text{Output Enables}}$ & LE Enable Inputs
"Light-Load" Transceivers/Latched or Registered Transceivers									
74F545	8-Bit	NINV	A_N=3-St	Yes	−3/24mA	None	7.0ns	No	Pin−for−Pin Replacement for the Intel 8286
			B_N=3-St	Yes	−15/64mA	None	7.0ns	No	
74F588	8-Bit	NINV	A_N=3-St	Yes	−3/24mA	None	7.5ns	No	
			B_N=3-St	Yes	−15/64mA	None	7.5ns	No	IEEE-488/GPIB w/ Output Line Termination Resistors
74F620/23	8-Bit	INV/NINV	B_N=3-St	Yes	−15/64mA	None	7.5ns	No	$A_N \leftrightarrow B_N$, A_N=−3/24mA
74F621/22	8-Bit	NINV/INV	B_N=OC	Yes	OC/64mA	None	13.0ns	No	$A_N \leftrightarrow B_N$, A_N=OC/24mA
74F640	8-Bit	INV	A/B=3-St	Yes	−15/64mA	None	7.5ns	No	$A_N \leftrightarrow B_N$
74F641/42	8-Bit	NINV/INV	A/B=OC	Yes	OC/64mA	None	13.0ns	No	$A_N \leftrightarrow B_N$
74F646/48	8-Bit	NINV/INV	A/B=3-St	Yes	−15/64mA	2-Reg	11.5ns	No	$A_N \leftrightarrow B_N$, Registers for A_N & B_N Ports, 80MHz (min.)
74F647/49	8-Bit	NINV/INV	A/B=OC	Yes	OC/64mA	2-Reg	19.5ns	No	$A_N \leftrightarrow B_N$, Registers for A_N & B_N Ports, 40MHz (min.)
74F651/2	8-Bit	INV/NINV	A/B=3-St	Yes	−15/64mA	2-Reg	12.5ns	No	$A_N \leftrightarrow B_N$, Registers for A_N & B_N Ports, 80MHz (min.)
74F653/4	8-Bit	NINV/INV	B_N=3-St	Yes	−15/64mA	B_N-Reg	11.0ns	No	$A_N \rightarrow B_N$, B_N Port = 85MHz (min.)
			A_N=OC	Yes	OC/64mA	A_N-Reg	20.0ns	No	$B_N \rightarrow A_N$, A_N Port = 45MHz (min.)
74F657	8-Bit	NINV	B_N=3-St	Yes	−15/64mA	None	8.0ns	Yes	$A_N \leftrightarrow B_N$, PARITY I/O, ODD/$\overline{\text{EVEN}}$ In & $\overline{\text{ERROR}}$ Out
74F861/2	10-Bit	NINV/INV	A/B=3-St	Yes	−15/64mA	None	10.0ns	No	$A_N \leftrightarrow B_N$
74F863/4	9-Bit	NINV/INV	A/B=3-St	Yes	−15/64mA	None	10.0ns	No	$A_N \leftrightarrow B_N$
74F1242/3	8-Bit	INV	A/B=3-St	No	−15/64mA	None	7.5ns	No	$A_N \leftrightarrow B_N$, Light Load pin replacements for F240/1
74F1245	8-Bit	INV	A/B=3-St	Yes	−15/64mA	None	6.5ns	No	$A_N \leftrightarrow B_N$, Light Load pin replacements for F245
74F30245	8-Bit	NINV	B_N=OC	Yes	OC/160mA	None	15.0ns	No	Octal, 30Ω Transmission Line Drive, B_N = 0.6mA I_{IL}
			A_N=3-St	Yes	−3/24mA	None	7.0ns	No	A_N "Light-Load" Inputs
74F30640	8-Bit	INV	B_N=OC	Yes	OC/160mA	None	15.0ns	No	Octal, 30Ω Transmission Line Drive, B_N = 0.6mA I_{IL}
			A_N=3-St	Yes	−3/24mA	None	7.0ns	No	A_N "Light-Load" Inputs
"Light Load" Arithmetic Functions									
74F85	4-Bit	INV/NINV	3-St	No	−1/20mA	None	14.5ns	No	4-Bit Magnitude Comparator
74F280A/B	9-Bit	NINV	3-St	Yes	−1/20mA	None	14.5ns	Yes	Parity Generator/Checker, "B" is faster than "A" version
74F604/5	16-Bit	NINV	3-St/OC	Yes	−3/24mA	D-Reg	80MHz	No	Dual 8−Bit Registered Octal Multiplexer

NOTES: All parameters are worse−case, unless otherwise speified
- 3−St ⇒ 3−State
- OC ⇒ Open Collector
- Reg ⇒ LOW−to−HIGH Edge Clocked D−Type Register
- Latch ⇒ HIGH Logic Level on the Latch Enable Logic, Data Passes Directly Through D−Type Latch, ⇒ HIGH−to−LOW Logic Level Transition of the Latch Enable, Data is Stored in the D−Type Latch
- S/R ⇒ Shift Register

designed to drive the chip side of the PC board to backplane interface, while the B_N Port is capable of driving PC board data transmission lines and back plane signal line with a characteristic impedance as low as 70Ω.

Referring back to Figure 215–1a, the base drive current for Q9/10/11 comes from either R6 for an inverting output or R7, if the output is non-inverting. For the inverting case, D4 is back-biased when the base voltage applied to Q1 ($\geq 2.0V_{OH}$) and Q9 base drive is supplied from R6. Q9's base is clamped at the sum of base-emitter forward biased voltage drops of Q9/10/11 and Q12. Q12's base drive primarily comes from R10/11/12 when Q9/10/11 are ON.

When Q9/10/11 begin to turn–ON, the base drive for Q12 must first overcome the R13/D13 base clamp before current can flow into Q12's base. During the output voltage HIGH to LOW transition, this delay minimizes totem–pole feed–through current into the ground lead by allowing the collector of Q11 (Phase Splitter Transistor – Q_{PS}) to pull down toward 1 V_{BE} + 1 V_{CEsat} and, thereby, turning–OFF the Q13/14 darlington totem–pole output pull–up driver before Q12 completely turns–ON.

When the gate input switches from V_{IH} to V_{IL} ($\leq 0.8V$), the charge stored in D2 discharges through the base–emitter of Q2. Q2 (through D3) quickly pulls the bases of Q9/10/11 toward ground. When the collector of Q9 rises high enough (~1.3V) to forward bias the Q12 base clamping network of D9/R8/R9/Q7/Q8, Q12 is quickly turned–OFF before the Q13/14 totem pole pull–up can turn–ON. This design minimizes feed–through ground during the output voltage LOW to HIGH transition.

The 3-state, totem-pole output structures of both the A_N and B_N ports have Schottky blocking diodes, D15, in their pull-ups. Their purpose is to block leakage current from flowing into the outputs when V_{CC} is either open or shorted to ground. These diodes will not let current flow until the output voltage reaches 5.5V.

The I_{OS} limiting resistors, R15, limit the amount of current that can be sourced from the HIGH to ground. Note that R15 is 12Ω for the B_N outputs and 30Ω for the A_N outputs. Therefore, under the same conditions, the B_N output pull-up structure will be able to source 2.5 time more current than the A_N outputs.

Minimizing Ground Bounce

Refer to Application Note AN213 – 74F30XXX Family Applications for a detailed discussion of "ground-bounce" and internal noise generation due to reduced ground lead inductance. When a TTL output switches from LOW to HIGH or HIGH to LOW some feed-through or crossover current will be injected into the ground lead of the IC while both the pull-up and pull-down output drive structures are ON simultaneously. The larger the number of switched outputs the larger the feed-through current and "ground bounce."

"Ground bounce" directly effects the input threshold of a gate and, therefore, its noise sensitivity. The newer output structure design used in the "Light Load" NPN Input Product Line allow all outputs to switch simultaneously with minimal "ground bounce."

Signetics

FAST Products

AN216
Arbitration In Shared Resource Systems

Application Note

INTRODUCTION

The need for more powerful and faster systems gave birth to multiprocessing and multitasking systems. But to achieve this, cost and reliability were not to be sacrificed. To reduce cost it is vital to share resources, but to do so requires reliable means of arbitration. In a multiprocessing system, a single bus may be shared between various processors or intelligent peripherals. The resources shared by processors (Figure 1) are generally termed as global resources and those shared between the local processor and the peripherals (Figure 2) are typically known as local resources. Whether local or global, there always exists a protocol that will connect and disconnect various devices to and from the shared resources. Various bus architectures in existence today have different ways of doing this.

No matter what the protocol of a specific bus, there is always a method which dictates how arbitration shall be performed between two or more devices. Some systems employ synchronous arbitration and some use an asynchronous approach. The third option is not to use arbitration at all, but instead to employ time-multiplexing. This is used mainly in data communications by dividing the common media into various time slots. Each processor (station) is assigned a predetermined time for using the media. If the station does not need to use the media during its assigned time-slot, it may pass control to the next station. This obviously results in an inefficient use of the bus bandwidth.

Synchronous and asynchronous arbitration have their advantages and disadvantages, and are both used in system designs. Some applications may even use a combination of the two. Generally, synchronous arbitration is used in systems where the designer can take the time to synchronize signals with the master clock. In synchronous arbitration the request is sampled on a clock edge, and therefore if it is asserted close to, but after the sampling clock edge, it will not be recognized

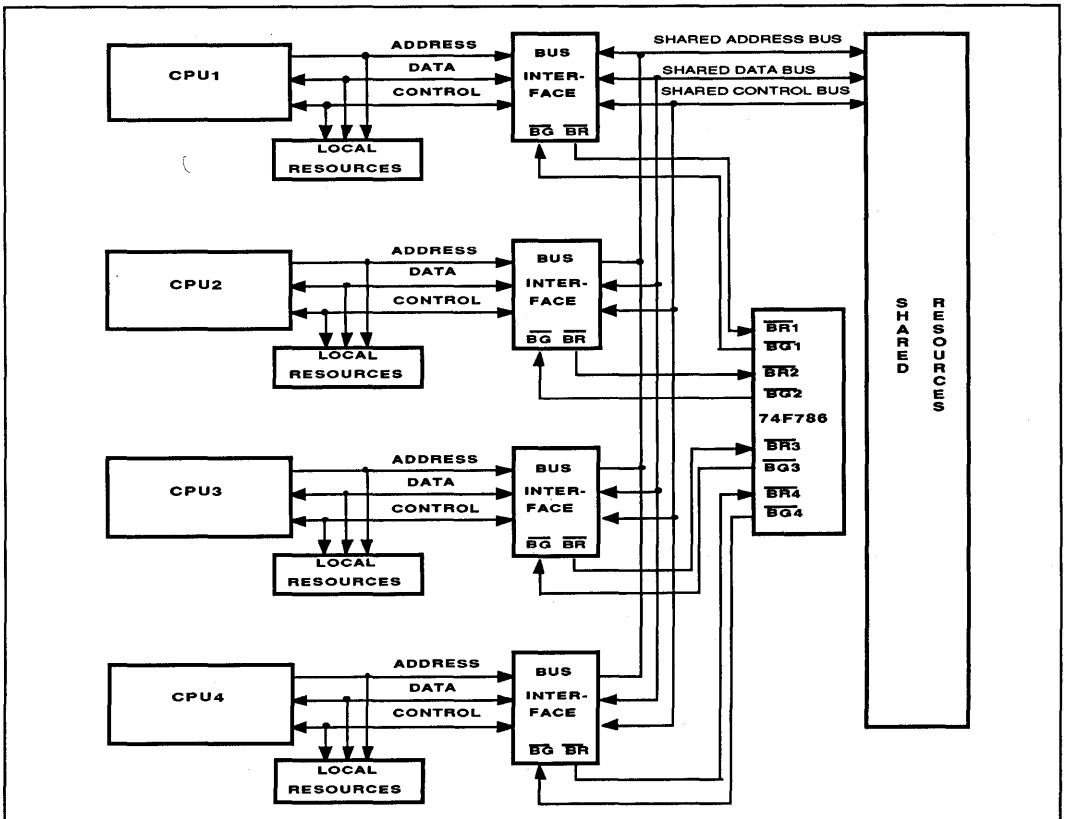


Figure 1: Sharing global resources

July 18, 1988

until after a whole clock cycle. Todays applications, where speeds are being pushed to their limits may not find that an optimal solution. Therefore more and more designers tend towards asynchronous arbitration because it is much faster on the average. Since applications vary drastically from one to another, some may be better served by first-come-first-serve arbitration, some with fixed priority and some with dynamic priority.

In a first-come-first-served scheme as the name implies, the request to be asserted first is selected first. All other requests made after the first are queued in their respective order of assertion. After the current request is serviced, the request asserted second will be selected and so on. If the request just serviced is asserted again, before all other active requests are serviced, it will be placed at the end of the queue. In a fixed priority method all inputs have a hard-wired priority and cannot be changed. In a dynamic priority assignment the user can change the priority depending upon the system needs. For example, processors performing vital tasks may be placed at a higher priority as compared to processors doing background tasks.

Arbitration, whether synchronous or asynchronous, always brings up the question of "metastability". A hard fact that relates itself all the way back to the beginning of the history of electronics. In its simplest definition it is the state of a flip- flop that is neither a logic"1" or a logic"0", and is a result of violations of its set-up and hold times. This condition must be allowed and dealt with in arbitration and synchronization designs.

Metastability

Various publications have talked about this subject and given recommendations for reducing but not completely eliminating this potential problem. Briefly the suggestions consist of using very fast flip-flops (with very small set-up and hold times), using multiple flip-flops and delay lines and designing of metastable-hardened flip-flops. Please note that a metastable-hardened flip-flop does not necessarily mean that it will never enter a metastable state, but rather it is a flip-flop that is highly optimized to be used in applications where the system designer can not guarantee the minimum set-up and hold times specified by the manufacturer. Since, as of today, the design of a metastable free flip-flop is not practically possible, the next best thing that could be done is design of a flip-flop with significantly reduced set-up and hold times and reduced propagation delays. This will ensure reduced probability of being in a metastable state. Since we still will have some probability of not meeting the minimum set-up and hold times and potentially being in a metastable state, another requirement to be im-

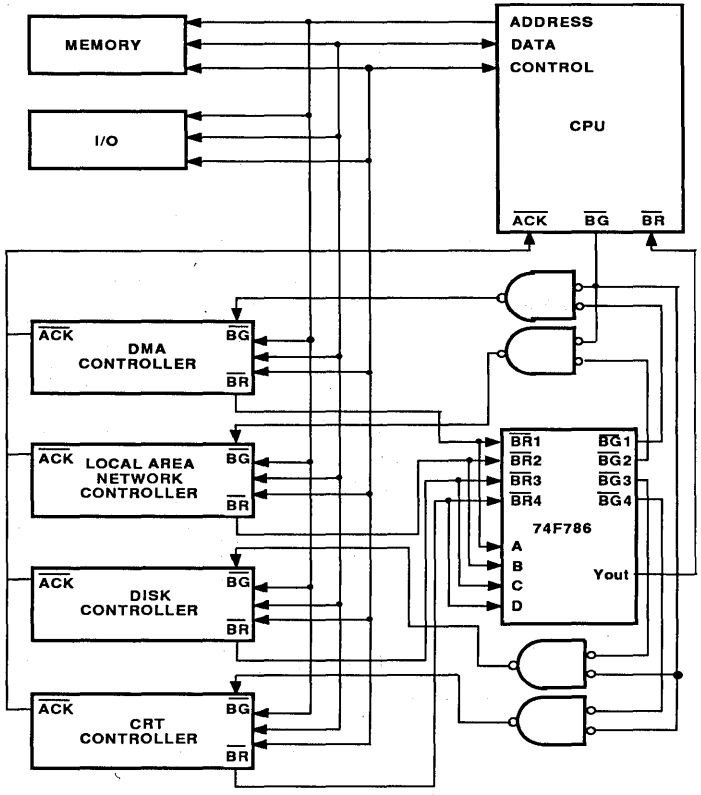


Figure 2: Sharing local resources

posed on this flip-flop would be to hold its previous state and not to propagate this invalid state to its outputs until it has decided to settle in a "0" or a "1" state. By doing so it could be guaranteed that the outputs of a flip-flop will never be in an undetermined state even though the flip-flop may internally be in a metastable state. The penalty that the user would expect to pay in such a design will be a propagation delay that can extend beyond the maximum specified in the data sheet.

74F786- 4-Input Asynchronous Arbiter

The key consideration when arbitrating for shared resources is that access may not be granted to more than one device at a given time. If this could be guaranteed, it would improve reliability. This application note describes a product from Signetics, which guarantees against simultaneous grants and does so at very high speeds. The Signetics 74F786 (Figure 3) is a general purpose asynchronous bus arbiter designed to address the needs for real-time applications, where arbitration is desired between multiple devices sharing common resources. The design goal was to provide for a device, the outputs of which could be guaranteed against logic hazards (glitches), metastability and that no more than one output could be active at a given time. The arbiter has four Bus Request ($\overline{BR}_n$) inputs which allow arbitration between two to four asynchronous inputs. The priority

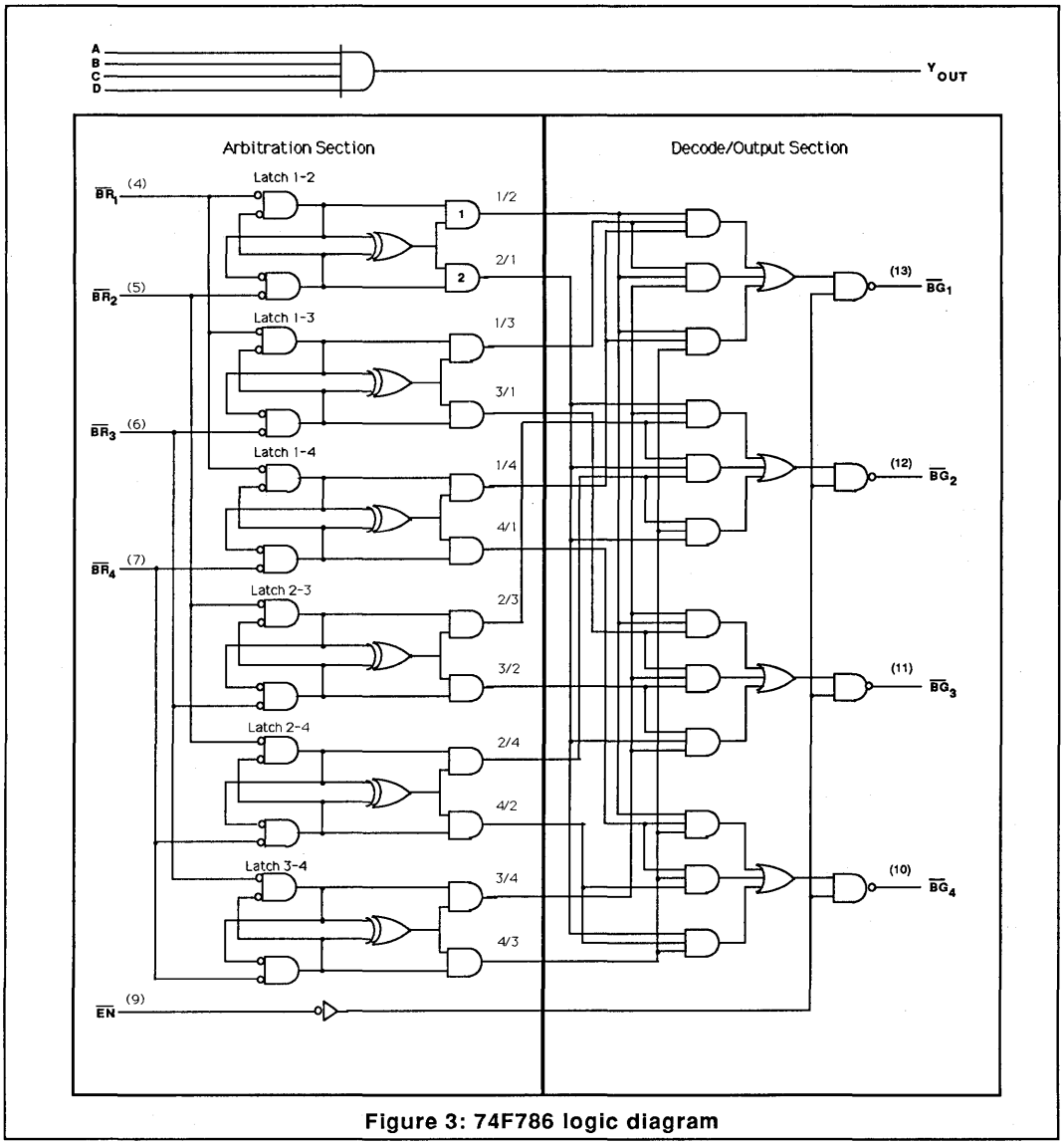


Figure 3: 74F786 logic diagram

is determined on a first-come-first-served basis. Corresponding to each input is a separate Bus Grant ($\overline{BG}_n$) output which indicates which one of the request inputs is served by the arbiter at a given time. All these outputs are enabled by a common enable ($\overline{EN}$) input. Also included on-chip, is a general purpose four-input AND gate which may be used to generate a bus request signal (Figures 2) or as an independent AND gate.

Since the Bus Request inputs have no inherent priority, the arbiter assigns priority to the incoming requests as they are received. Therefore, the first request asserted will have the highest priority. When a Bus Request is received, its corresponding Bus Grant becomes active, provided $\overline{EN}$ is LOW, and no other Bus Grant is active. Typically, a Bus Grant is selected in 6.6 nsec from the time of assertion of a request input. If additional Bus Requests are made after the first request goes LOW, they are queued in their respective order. When the first request is removed, the arbiter services the request with the next highest priority, based upon a first-come-first-served algorithm.

Metastable-Free Outputs

The 74F786 logic diagram (Figure 3) consists of two sections: the arbitration section and the decoding/output section. Within the arbitration section lie six independent 2-input arbiters each of which arbitrates between the two Bus Request ($\overline{BR}_n$) inputs connected to that specific arbiter. Each 2-input arbiter is comprised of two cross-coupled NOR gates, an EX-OR gate and two AND gates. The cross-coupled NOR gates are designed so that they are securely latched when a schottky diode voltage difference appears between the outputs of these NOR gates. The EX-OR gate is designed so that its output will remain LOW until there is at least 1Vbe difference between its inputs. This creates a noise-margin of 1Vbe (base to emitter voltage)-1Vsky (schottky voltage) ≈ 0.3 Volts and assures that the output of the EX-OR will not go HIGH until after the two NOR gates have resolved any contention problems. This guarantees that neither of the outputs of a 2-input arbiter can be in a metastable state, and also that both outputs cannot be high simultaneously. As is clear from Figure 3, the first 2-input arbiter is responsible for deciding between the $\overline{BR}_1$ and $\overline{BR}_2$ inputs. Since both AND gate outputs cannot be high at the same time, the other three possible configurations are; First, AND gate1 is HIGH indicating that $\overline{BR}_1$ arrived at the latch before $\overline{BR}_2$ (designated 1/2); second, AND gate2 is HIGH indicating $\overline{BR}_2$ arrived before $\overline{BR}_1$ (designated 2/1) and third both AND gates are LOW indicating that neither $\overline{BR}_1$ nor $\overline{BR}_2$ has been latched.

Glitch-Free Outputs

The decode section of the 'F786 is responsible for insuring that the outputs do not glitch or produce a logic hazard. While there are three possible Karnaugh mappings, to produce an optimum decode section with a minimum number of transistors and balanced propagation times, the mapping in Table 1 was chosen. Solving Table 1 for $\overline{BG}_1$-$\overline{BG}_4$ yields the following equations:

$\overline{BG}_1$=1/2.1/3.1/4+1/2.1/3.3/4+1/2.1/4.4/3
$\overline{BG}_2$=2/1.2/3.2/4+2/1.2/3.3/4+2/1.2/4.4/3
$\overline{BG}_3$=3/1.3/2.3/4+1/2.3/1.3/4+2/1.3/2.3/4
$\overline{BG}_4$=4/1.4/2.4/3+1/2.4/1.4/3+2/1.4/2.4/3

To see if a glitch can occur let's take the worst possible case, that is, let $\overline{BR}_1$ beat $\overline{BR}_2$, 2 beat 3, 3 beat 4 and 4 beat 1 (a possible situation when all inputs are asserted simultaneously). Also, let's have the outputs of the arbitration section switch sequentially. Initially, all the variables in the equations are false (remember, the outputs of the arbitration section have three possible states). First, when 1/2 goes true 2/1 must remain false. This eliminates several terms from playing a role in deciding which output becomes active. In fact, $\overline{BG}_2$ has been removed from the list and is no longer a contender. At this point, while all the outputs are high (inactive) we have decided that $\overline{BG}_2$ will remain inactive. This leaves us with the following equations.

$\overline{BG}_1$=1/2.1/3.1/4+1/2.1/3.3/4+1/2.1/4.4/3
$\overline{BG}_3$=3/1.3/2.3/4+1/2.3/1.3/4+~~2/1.3/2.3/4~~
$\overline{BG}_4$=4/1.4/2.4/3+1/2.4/1.4/3+~~2/1.4/2.4/3~~

Similarly when 2/3 goes true 3/2 must remain false, which further eliminates a term from thus set of 3 equations.

$\overline{BG}_1$=1/2.1/3.1/4+1/2.1/3.3/4+1/2.1/4.4/3
$\overline{BG}_3$=~~3/1.3/2.3/4~~+1/2.3/1.3/4+~~2/1.3/2.3/4~~
$\overline{BG}_4$=4/1.4/2.4/3+1/2.4/1.4/3+~~2/1.4/2.4/3~~

Now when 3/4 goes true 4/3 must remain false. This eliminates $\overline{BG}_4$ from the contending list and the contest now is between $\overline{BG}_1$ and $\overline{BG}_3$ as indicated from the following equations.

$\overline{BG}_1$=1/2.1/3.1/4+1/2.1/3.3/4+~~1/2.1/4.4/3~~
$\overline{BG}_3$=~~3/1.3/2.3/4~~+1/2.3/1.3/4+~~2/1.3/2.3/4~~

When 4/1 goes true 1/4 must remain false.

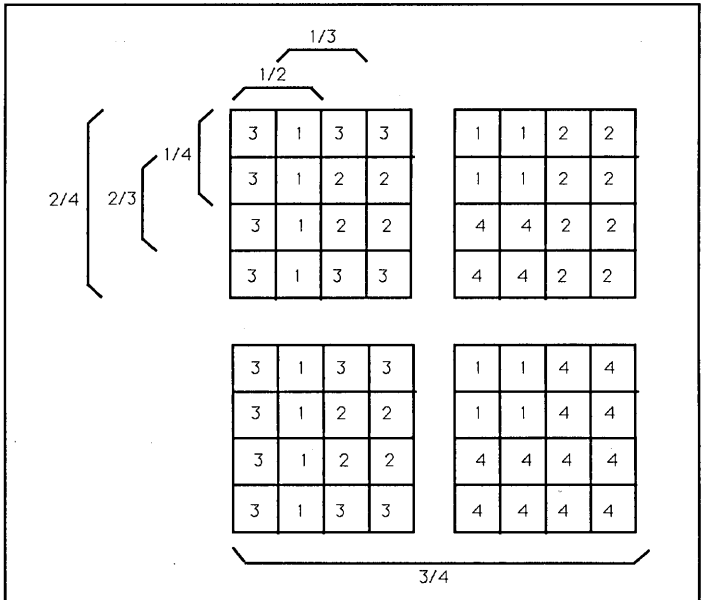


Table 1: 74F786 Karnaugh mappings

Still no decision has been made and is dependent on the two 2-4 and 1-3 latches not taken into account yet. In this case the 2-4 latch status is a don't care, so the outcome of the 1-3 latch dictates the Bus Request granted.

$\overline{BG}_1$=1/2. 1/3. 3/4
$\overline{BG}_3$=1/2. 3/1. 3/4
If the 1-3 latch settles in the 1/3 state $\overline{BR}_1$ gets the grant, and with 3/1 remaining false, $\overline{BG}_3$ will remain inactive. Similarly if the 1-3 latch goes to the 3/1 state $\overline{BR}_3$ gets the grant, and with 1/3 remaining false $\overline{BG}_1$ will remain inactive.

Notice that the Bus Grant was given in this case without regard to the 2-4 latch. In fact, a quick review shows that neither the 2-3 latch nor the 1-4 latch played a role in making the decision. Each grant is dependent on the state of three latches. By the nature of the encoding logic, as the three activating latches are switched, three outputs are forced to remain in an inactive state. This insures a glitch-free output.

Let's assume that in the example above, the 1-3 latch goes to the 1/3 state and hence $\overline{BG}_1$ is asserted. At this time the other five latches in the circuit will be in 1/2, 4/1, 2/3, 2/4 and 3/4 states. If at this point $\overline{BR}_3$ is removed, then latch 3-4 changes from 3/4 to 4/3 and hence $\overline{BR}_4$ steals the grant (with 1/2. 4/1. 4/3). This concludes that if three or more requests are asserted precisely at the same time, and one of them is removed prior to being serviced, it may cause premature termination of the present grant and assertion of another grant. Therefore, when using three or more Bus Requests it is not advised to remove a request before being serviced. On the other hand, arbitration between two requests does not have this restriction. The user if necessary, may decide to remove an ungranted request at his discretion.

Extended Propagation Delays

Since the outputs of the six 2-input arbiters can not display a metastable condition, the Bus Grant outputs can not display a metastable condition because the decoding/output section does not have any storage element to go metastable. Even though the Bus Grant outputs can't go metastable, the cross-coupled NOR gates can. To determine the metastability characteristics of these NOR gates, the 'F786 was evaluated by Mr. Thomas J. Chaney of Washington University in St. Louis, Missouri, who is considered to be a leading expert in this field. Table 2 gives of the 19 devices supplied to him, the test results from the fastest, the slowest and a typical package. In order to determine the Mean Time Between Package Unresolved (MTBPU) with the relative arrival times of the two input signal transitions uniformly distributed, the following formula is used:

MTBPU= $[\exp(t'/\tau)]/[T_0(\text{Input 1 rate})(\text{Input 2 rate})]$.

Where:

t'= Time given to resolve contention between inputs after they are asserted and τ and T_0 are device parameters derived from tests and can most nearly be defined as:

τ= A function of the rate at which a latch in a metastable state resolves that condition.

& T_0= A function of the measurement of the propensity of a latch to enter a metastable state. T_0 is also a very strong function of the normal propagation delay of the device.

Solving for t', the resolving time measured from the arrival of the first input, and setting up the equation so the value of T_0 in Table 2 (given in nsec.) can be substituted directly is:

$t'=(\tau)\ln[(T_0)(3E14)]$.

The implication of the above equation is that, even though typical propagation delay through the arbiter is about 6.6nsec, contention between inputs may extend this time significantly and can be calculated from Table 2.

Package	Latch	Output Measured	τ (nsec)	T_0 (nsec)	h (nsec)	t' for 1 failure/century (inputs at 10E6hz)
FASTEST	1-2	13	.38	175E2	6.6	16.6
	1-3	13	.39	79E2	6.6	16.4
	1-4	13	.39	69E2	6.6	16.4
	2-3	12	.38	109E2	6.6	16.1
	2-4	12	.39	68E2	6.6	16.5
	3-4	11	.38	181E2	6.6	16.3
SLOWEST	1-2	13	.44	34E2	6.6	18.1
	1-3	13	.44	17E2	6.6	18.0
	1-4	13	.43	26E2	6.6	17.8
	2-3	12	.44	16E2	6.6	17.9
	2-4	12	.46	8E2	6.6	18.5
	3-4	11	.44	29E2	6.6	18.2
TYPICAL	1-2	13	.41	56E2	6.6	17.3
	1-3	13	.42	24E2	6.6	17.2
	1-4	13	.43	17E2	6.6	17.5
	2-3	12	.43	18E2	6.6	17.4
	2-4	12	.39	72E2	6.6	16.6
	3-4	11	.41	49E2	6.6	17.2

Where h= typical propagation delay through the device.

Table 2: 74F786 test results for all latches for three packages.
All tests with V_{cc}=5.0vdc and at room temperature

Signetics

FAST Products

AN217

Metastability Tests For The 74F786- A 4-Input Asynchronous Bus Arbiter

Application Note

INTRODUCTION

Under contract with Signetics, Mr. Thomas J. Chaney of Washington University, St. Louis tested a set of nineteen 74F786 samples (packages) to determine the metastable state recovery statistics for the circuits. The tests were conducted using a procedure described in a paper entitled "Characterization and Scaling of MOS Flip-Flop Performance", (section IV), by T. Chaney and F. Rosenberger, presented at the CalTech Conference on VLSI, Jan. 1979. The general test procedure was to test all 19 packages under one condition, then test the best, worst, and an average package in more detail. According to Mr. Chaney, the test results from the 19 packages formed one of the tightest groupings that he had ever seen. As the parts were numbered, package No. 7 had the fastest resolving times, No.11 produced some of the slowest resolving times, and No.1 had resolving times near the middle of the test results. This ranking of the test results from 3 packages remained the same through out the balance of the test program, which supports the complete testing of only 3 packages. In general, the poorest performance resulted when the packages were heated to near 75 °C with Vcc = 4.5vdc and the best performance resulted when the packages were cooled to near 0 °C with Vcc = 5.5vdc. The variation within one package caused by the temperature and Vcc changes was greater than the variation from package to package. It must be noted that none of the packages tested even approached the data sheet input to output worst case propagation delay of 10.5ns. All the packages tested for a single active output, had propagation delays of about 6ns. Typically, the parts with longer propagation delays also have slower resolving times. Thus one would expect that the delay time needed to have only one failure in 32 years using a 10nsec. propagation delay part would be much longer than a value derived from just adding 10-6=4 ns to the above calculations. Thus it appears that the poorest performance measured in this study should be considered a measurement at the edge of the typical range for 74F786 parts.

It must also be noted that the tight grouping of this set of packages means that, when comparing differences between these test results, the measured error, as outlined in "Measured Flip-Flop Responses to Marginal Triggering", IEEETC, Dec. 1983, is significant. This is illustrated in association with Table 5.

Test Program And Data

Through out the test period, the connections to some of the package pins was as shown in Figure 1. The 4 input pins (1, 2, 3 and 15) to the AND gate were all grounded. The output of the AND, pin 14, was left open. The output enable $\overline{EN}$ pin (9) was grounded. The power ground pin (8) was grounded and the Vcc power pin (16) was connected to Vcc. The 4 input pins to the arbiter (4, 5, 6 and 7) were treated as a group with two of the pins always receiving an input from the tester and the other two inputs always connected to Vcc through 1KΩ resistors. For any arbiter input pair configuration, there are two outputs (of the set: Pins 10, 11,12 and 13) active. These two active output pins are each connected to a grounded 510Ω resistor, a grounded 30pF silvered mica capacitor, and a grounded scope probe (13pF). Thus each active output pin has a load of approximately 500Ωs to ground and 50pF to ground (43pF plus 5 to 10pF wiring capacitor). In addition, the active output pin being tested was connected to the input of a comparator (3pF max.). The other input to this comparator was referenced to 1.5vdc. The 1.5vdc reference voltage was not varied with Vcc. The two arbiter input signals generated by the tester were negative going pulses, each of the same width (approximately 100ns), which were time shifted relative to each other to produce metastable behavior in the arbiter circuit. This form of input causes only one of the two possibly active outputs to switch low.

First Pass Through Packages

The test conditions used for the selection process from the 19 packages is shown in Figure 1 with the results shown in Table 1. The values reported in Table 1 were calculated with t' (defined later) at 7.60 and 9.93ns. Note that the active inputs are pins 6 and 7 and the output tested is pin 11. The last column of this table is the period, after two requests, required to assure that the pack-

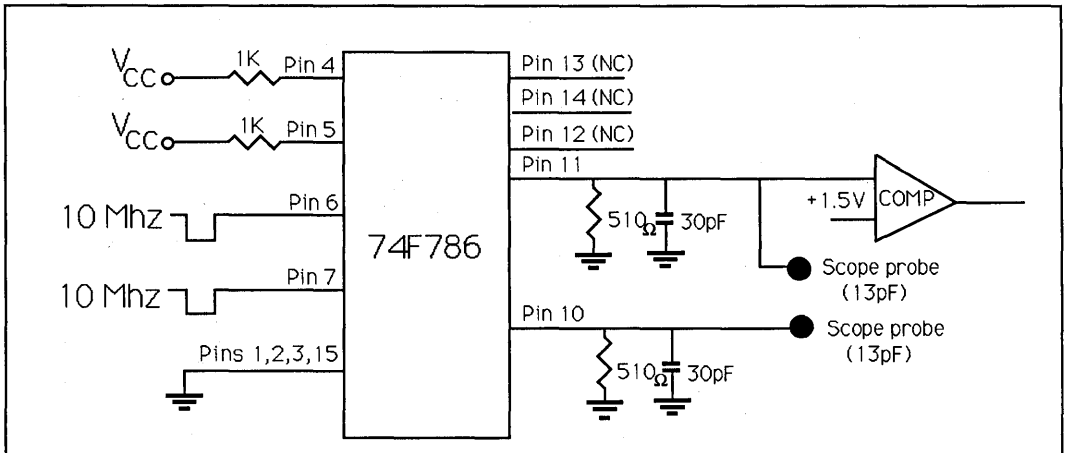


Figure 1: Test set-up for the 74F786

July 18, 1988

Metastability Tests For The 74F786-A 4-Input Asynchronous Bus Arbiter

AN217

age would fail to resolve less than once per century. These numbers are based on the assumption that the 2 inputs are not synchronized and both are running at 10mhz (a 100ns clock period). It is assumed that the relative arrival times of the two input signal transitions are uniformly distributed over the clock period. The Mean Time Between Package Unresolved (MTBPU) is then:

MTBPU = [exp(t'/τ)/[(T_0)(Input1 rate)(Input2 rate)]

Where:

t'= Time given to resolve contention between inputs after they are asserted and τ and T_0 are device parameters derived from tests and can most nearly be defined as:

τ = A function of the rate at which a latch in a metastable state resolves that condition and

T_0= A function of the measurement of the propensity of a latch to enter a metastable state. T_0 is also a very strong function of the normal propagation delay of the device. Also one century = 3E9 seconds.

Solving for t', the resolving time measured from the arrival of the first request, and setting up the equation so the value of T_0 in Table 1 (given in ns) can be substituted directly gives:

$$t' = (\tau)1n[(T0)(3E14)]$$

As a result of the first round of tests, three packages were selected for further testing. Package 7 was selected as the fastest, package 11 as the slowest, and package 1 as a typical package.

Package Number	τ (ns)	T_0(ns)	h (ns)	t' for 1 failure/century (inputs at 10E6hz)
1	0.44	17E2	6.6	17.8
2	0.44	15E2	6.6	18.0
3	0.39	12E2	6.6	16.6
4	0.46	9E2	6.6	18.5
5	0.44	9E2	6.6	17.7
6	0.40	63E2	6.6	16.9
7	0.39	103E2	6.6	16.6
8	0.46	8E2	6.6	18.6
9	0.44	22E2	6.6	18.1
10	0.46	9E2	6.6	18.4
11	0.45	18E2	6.6	18.5
12	0.45	14E2	6.6	18.3
13	0.45	11E2	6.6	18.3
14	0.45	15E2	6.6	18.2
15	0.45	11E2	6.6	18.2
16	0.43	30E2	6.6	17.6
17	0.44	16E2	6.6	18.0
18	0.39	126E2	6.6	16.9
19	0.43	31E2	6.6	17.8

Table 1: Test results for inputs on pins 6 & 7 and ouput measured at pin 11. V_{cc} = 5.0vdc at room temperature. t' = 7.60 and 9.93ns

Input Pins	Latch Under Test	Output Pins Active
4,5	Latch 1-2	13,12 - test pin 13
4,6	Latch 1-3	13,11 - test pin 13
4,7	Latch 1-4	13,10 - test pin 13
5,6	Latch 2-3	12,11 - test pin 12
5,7	Latch 2-4	12,10 - test pin 12
6,7	Latch 3-4	11,10 - test pin 11

Table 2: Arbiter inputs and corresponding latches and output mapping

Second Set Of Tests

Using the logic diagram of the 74F786 (Figure 2), it is possible to construct Table 2. Note from Table 2 that thus far, all testing has been conducted on latch 3-4 (pins 6 &7). The second set of tests, conducted only on the 3 packages selected from the first set of tests, involved testing each of the 6 latches in the package to select the poorest performing latch in each package. This step also included testing each of the two active output pins for each input condition to select the path with the longest propogation delay.

Package Number	Latch	Output Measured	τ (ns)	T_0(ns)	h (ns)	t' for 1 failure/century (inputs at 10E6hz)
7	1-2	13	.38	175E2	6.6	16.6
7	1-3	13	.39	79E2	6.6	16.4
7	1-4	13	.39	69E2	6.6	16.4
7	2-3	12	.38	109E2	6.6	16.1
7	2-4	12	.39	68E2	6.6	16.5
7	3-4	11	.38	181E2	6.6	16.3
11	1-2	13	.44	34E2	6.6	18.1
11	1-3	13	.44	17E2	6.6	18.0
11	1-4	13	.43	26E2	6.6	17.8
11	2-3	12	.44	16E2	6.6	17.9
11	2-4	12	.46	8E2	6.6	18.5
11	3-4	11	.44	29E2	6.6	18.2
1	1-2	13	.41	56E2	6.6	17.3
1	1-3	13	.42	24E2	6.6	17.2
1	1-4	13	.43	17E2	6.6	17.5
1	2-3	12	.43	18E2	6.6	17.4
1	2-4	12	.39	72E2	6.6	16.6
1	3-4	11	.41	49E2	6.6	17.2

Table 3: Test results for all 6 latches from packages 7, 11 and 1. All tests with V_{cc} = 5.0vdc and at room temperature

The results of this comparison testing is shown in Table 3. The results from this Table indicate that latches 1-2 and 3-4 have longer propogation delays than the middle four latches. This propagation delay difference is less than 0.4ns. For each of the conditions tested and reported in Table 3, there is a second active pin that could have been used to measure the performance of the latch under test. For package 1 only, the other active pin was tested for each of the latchs. The results of this test are shown in Table 4. In theory, the results should be the same except for possible differences in propogation delay. The value of τ should be the same, but the value of T_0 could be different. In all 6 cases, the active pin previously not tested had a shorter propagation delay (function of T_0) than the active pin that was tested.

Table 4 also indicates something else. That

Metastability Tests For The 74F786- A 4-Input Asynchronous Bus Arbiter

AN217

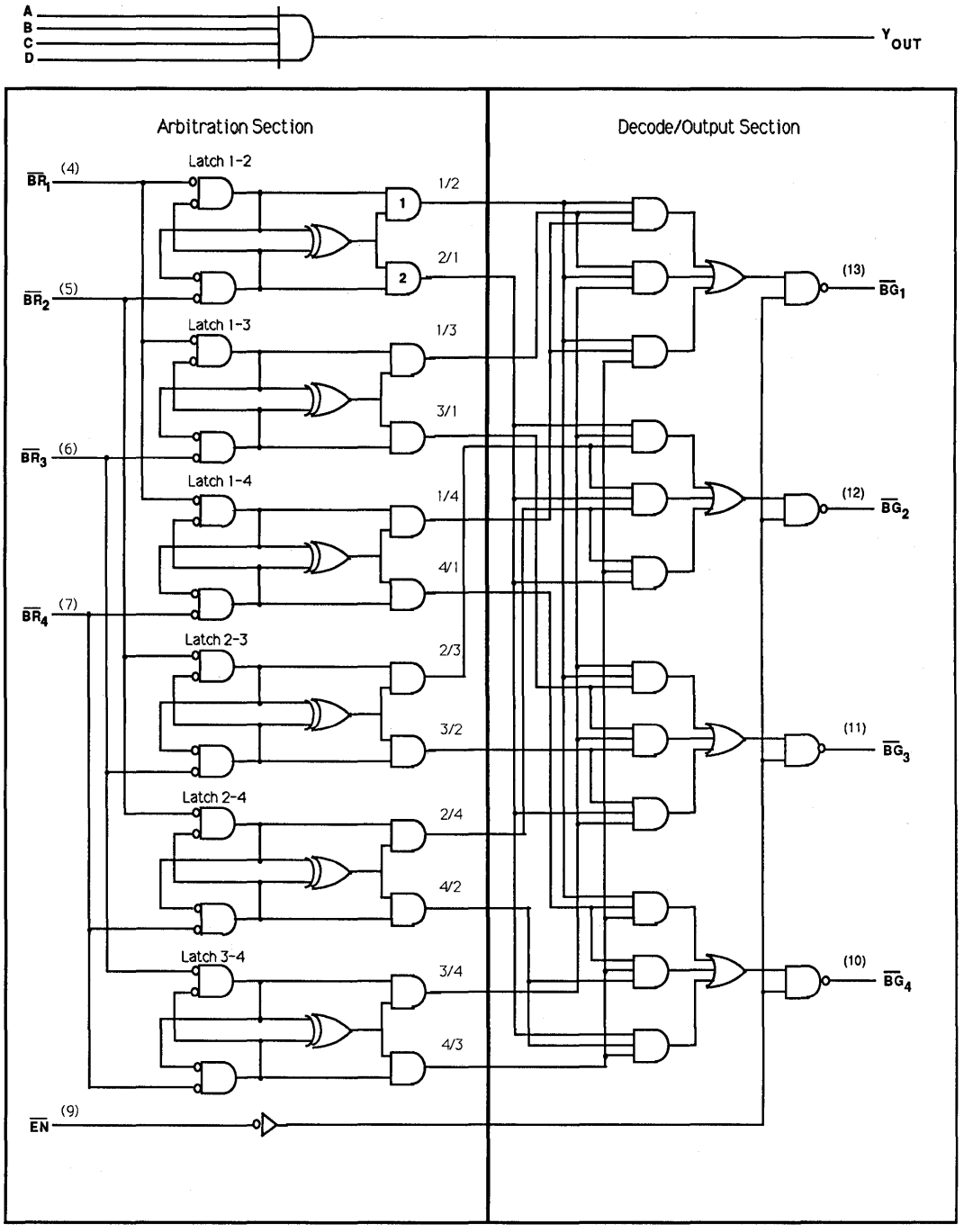


Figure 2: 74F786 logic diagram

July 18, 1988

Metastability Tests For The 74F786-A 4-Input Asynchronous Bus Arbiter

is the accuracy with which the data in this report can be interpreted. Note that τ varies as much as 0.05ns, which is within the 0.06ns measurement error range of the test equipment used.

The results of the second set of tests are:
(1) The 6 latches in each of the 3 selected packages behaved the same, relative to each other.
(2) In all 3 packages, the latch selected is of little importance, therefore, Latch1-2 was selected at random for further testing.
(3) It was reasonable to continue with the 3 selected packages and to restrict further testing to latch1-2 and to only record data from pin 13.

Temperature And Power Supply Variation Testing

The temperature and power supply variation testing was conducted on packages 1, 7 and 11. These tests were conducted on latch1-2 only of each package (inputs 4 and 5, results measured at pin 13). The results are shown in Table 5. The poorest performance was measured again from package 11. The worst case condition was measured at Vcc = 4.5vdc and the case temperature at 75°C and is shown in Table 5 as a bold entry. This line gives what could be considered the worst case measured performance from the 19 packages tested.

Package Number	Latch	Output Measured	τ (ns)	T_0(ns)	h (ns)	t' for 1 failure/century (inputs at 10E6hz)
1	Latch 1-2	13	0.41	156E2	6.6	17.3
1	Latch 1-2	*13	0.39	160E2	6.6	16.8
1	Latch 1-2	12	0.36	390E2	6.6	15.8
1	Latch 1-3	13	0.42	24E2	6.6	17.2
1	Latch 1-3	*13	0.39	101E2	6.6	16.5
1	Latch 1-3	11	0.36	137E2	6.6	15.6
1	Latch 1-4	13	0.43	17E2	6.6	17.5
1	Latch 1-4	*13	0.40	77E2	6.6	16.7
1	Latch 1-4	10	0.35	201E2	6.6	15.3
1	Latch 2-3	12	0.43	18E2	6.6	17.4
1	Latch 2-3	*12	0.40	63E2	6.6	16.7
1	Latch 2-3	11	0.37	88E2	6.6	15.5
1	Latch 2-4	12	0.39	72E2	6.6	16.6
1	Latch 2-4	*12	0.39	79E2	6.6	16.6
1	Latch 2-4	10	0.36	96E2	6.6	15.5
1	Latch 3-4	11	0.41	49E2	6.6	17.2
1	Latch 3-4	*11	0.40	99E2	6.6	16.9
1	Latch 3-4	10	0.36	246E2	6.6	15.7

*These values were computed using the subset of sample times used to measure the response from the other active pin in each case.

Table 4: Test results for all 6 latches from package 1, measured and/or computed different ways. All tests with V_{cc} = 5.0vdc and at room temperature

Package Number	V_{cc}	Temperature	τ (ns)	T_0(ns)	h (ns)	t' for 1 failure/century (inputs at 10E6hz)
7	4.5	3°C	0.37	260E2	6.6	16.3
7	5.5	3°C	0.38	67E2	6.6	15.8
7	4.5	75°C	0.44	70E2	6.6	18.4
7	5.5	75°C	0.43	37E2	6.6	17.7
11	4.5	3°C	0.41	88E2	6.6	17.4
11	5.5	3°C	0.39	64E2	6.6	16.6
11	4.5	Room Temp.	0.42	76E2	6.6	17.9
11	5.5	Room Temp.	0.42	30E2	6.6	17.5
11	4.5	75°C	0.50	15E2	6.6	20.3
11	**4.5**	**75°C**	**0.51**	**8E2**	**6.6**	**20.6**
11	5.5	75°C	0.47	19E2	6.6	19.3
1	4.5	Room Temp.	0.42	93E2	6.6	17.7
1	5.5	Room Temp.	0.42	48E2	6.6	17.1
1	4.5	75°C	0.44	69E2	6.6	18.7
1	5.5	75°C	0.44	37E2	6.6	18.3

Table 5: Test results for latch1-2 from packages 7,11 and 1.All tests with V_{cc} = 4.5vdc-5.0vdc and temperatures from 0°C to 75°C

Signetics

AN218
DESIGN HIGH PERFORMANCE MEMORY BOARDS USING FAST LOGIC AND SIMPLE TRANSMISSION LINE TECHNIQUES

Application Note

Author: Edward Allyn Burton

INTRODUCTION AND OVERVIEW

With ever increasing memory speeds and correspondingly higher speed drivers, transmission line effects in memory boards are becoming more and more of a problem. An engineer can easily control, manipulate or work around the transmission line effects if he has all the information he needs and he understands how to use it. This article will supply that information and understanding as well as a fairly detailed look at some of the most common problems encountered in memory board design.

The article has three main parts. The first part lists and briefly explains the transmission line equations which will be used in the rest of the paper. The second part provides capacitance, inductance, and driver current/voltage information which is useful when applying the transmission line equations to memory boards. The third part is a detailed look at problems which often arise in memory board design and an evaluation of the solutions in common use.

PART 1: TRANSMISSION LINE EQUATIONS

A signal line in the memory array of a bare printed circuit board has both capacitance and inductance (L) distributed along its length. When the memory chips are inserted, the input capacitance of each input the signal line must drive is added to the line's distributed capacitance to give the total capacitance (C). The characteristic impedance (Z_0) of the signal line is given by Equation 1. Note that since (L) and (C) are both directly proportional to the length of the line, characteristic impedance is not a function of line length.

Eq. 1 $Z_0=(L/C)^{1/2}$

Equation 2 gives the current (I) a driver needs to source in order to change the voltage on a signal line by an amount (V). Notice that I-V relationship of the line at its input is that of a resistance (Z_0) to the voltage existing on the line before the driver tried to change it.

Eq. 2 $I=V/Z_0$

When the voltage is changed at the driven end of a signal line, the voltage wave travels down the line at a finite speed. Equation 3 gives the time (T) it takes for a transition to propagate from one end of the signal line to the other.

Eq. 3 $T=(LC)^{1/2}$

When a voltage wave ($V_{incident}$)travels down a signal line and encounters an impedance change from Z_0 to some new impedance (Z_1), $V_{incident}$ will split into a reflected part ($V_{reflected}$) and transmitted part ($V_{transmitted}$). $V_{reflected}$ will (as the name implies) travel back up the line toward the driver, and $V_{transmitted}$ will travel on down the line in the original direction of propagation. $V_{reflected}$ and $V_{transmitted}$ are given by Equations 4 and 5.

Eq. 4 $V_{reflected}=V_{incident}(Z_1-Z_0)/(Z_1+Z_0)$

Eq. 5 $V_{transmitted}=V_{incident}+V_{reflected}$

PART 2: TRANSMISSION LINE PARAMETERS IN MEMORY BOARDS

In order to use the preceding equations, an engineer will need to know the inductance and the capacitance of the signal lines in his memory board, and the output I-V relationship of the drivers on that board. This section provides the information needed for a quantitative understanding of all the examples which will be shown later. However, there are simply too many memory drivers and memory parts to fully document here. The information will still provide a very broad qualitative understanding of transmission line behavior in memory boards, and this qualitative understanding is a very powerful design and debug tool.

INDUCTANCE AND CAPACITANCE

Figures 1 and 2 show how the distributed inductance and capacitance of a signal line vary with width and dielectric thickness on a fiberglass memory board with a ground plane. These figures are not exact, but they don't have to be exact. A 15 percent error in the calculated characteristic impedance or propagation delay of a memory board signal line is unlikely to cause any problems, and this means that a 30 to 35 percent error in the inductance or the capacitance of a signal line will likely be allowable (because of the square root relationship between L and C and Z_0). By the same reasoning, a typical input capacitance of 3pF is suggested for calculations, although from some memory suppliers it will be closer to 2pF, while from others it will be closer to 4pF.

Note that on a two layer memory board there is no ground plane, so Figures 1 and 2 can't be applied. The distributed capacitance for 15 mil line on a typical 60 mil thick two layer memory board is about 1pF/inch, and the distributed inductance is around 20nH/inch.

BALLPARK CALCULATIONS

Ballpark estimates for the characteristic impedance and propagation speed can be calculated using the preceding information and typical packing densities for various memory packaging modes. The dual-in-line package (DIP), for instance, is typically packed on a board at around a 0.5 inch pitch so that there are two inputs for a one inch length of line. This means that the input capacitance on a one inch length of line will be 6pF. Figures 1 and 2 show that for a typical four layer memory board, with a line width of 10 mils and a dielectric thickness of 15 mils, the distributed capacitance for a one inch length of line will be about 3pF, and the distributed inductance for the line will be about 12nH. The values for L and C (required for use in Equations 1 and 3) for this one inch DIP

DESIGN HIGH PERFORMANCE MEMORY BOARDS USING SIMPLE TRANSMISSION LINE TECHNIQUES

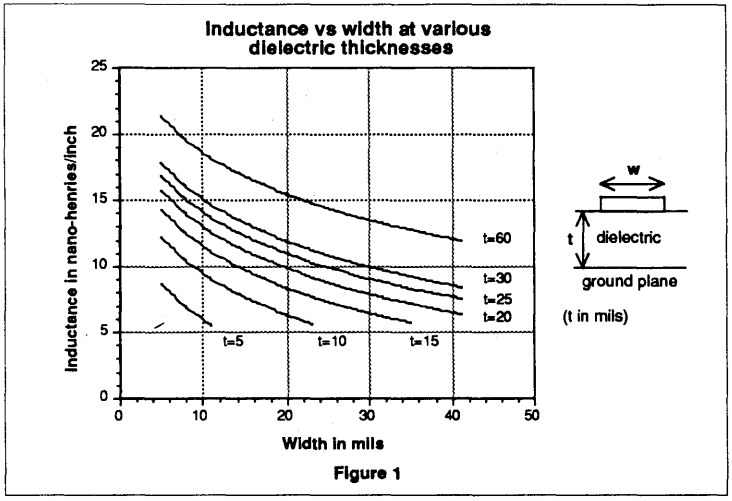


Figure 1

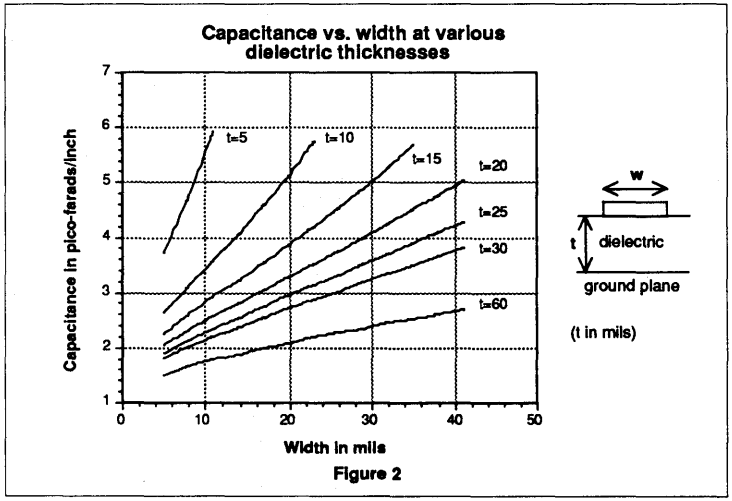


Figure 2

Package	Pitch	L	C	Z0	T
DIP	0.5 inch	12 nH	9 pF	37 ohms	0.3ns
ZIP	0.2 inch	12 nH	18 pF	26 ohms	0.5ns
SIP	0.3 inch	12 nH	103 pF*	11 ohms	1.1ns

* SIP capacitance includes on-module wiring capacitance of 6 pF per module.

Table 1

memory line will be 12nH and 9pF. The ballpark characteristic impedance and propagation delay for one inch lengths of DIP, ZIP, and SIP memory lines are shown in Table 1.

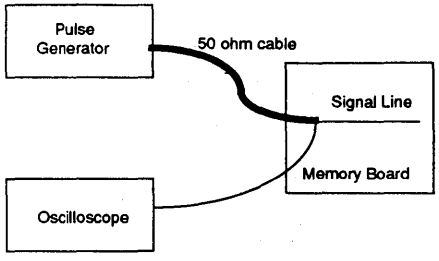
MEASURING IMPEDANCE AND PROPAGATION DELAY

Often an engineer will want to analyze a board which has already been built. In this case, it is easy to directly measure the characteristic impedance and the propagation delay of the signal lines using an oscilloscope and a pulse generator rather than calculating it from its inductance and capacitance. To do this, connect the pulse generator, unterminated signal line, and oscilloscope as shown in Figure 3a. The oscilloscope waveform will have the same basic shape as the one in Figure 3c. The initial voltage drop (V1) is the transmitted signal from the 50 ohm cable to the signal line, and the second voltage drop (V2) is its reflection from the unterminated (infinite impedance terminated) end of the signal line. Notice that for a change in impedance from some finite impedance (Z_0) to an infinite impedance, Equation 4 predicts that the reflected signal will be of the same magnitude and sign as the incident signal, i.e., the initial voltage drop will travel to the end of the line and then reflect as a voltage drop of the same magnitude as the first, and then it will propagate back up the signal line to the oscilloscope input. The time difference (2T) between the midpoints of these two voltage drops is twice the propagation delay of the signal line. Measure V1 and record it as $V_{transmitted}$. Then replace the signal line with a length of 50 ohm cable about a meter long as shown in Figure 3b. The oscilloscope waveform will still have the same basic shape, but the initial voltage drop will probably be different. Since this time the initial voltage drop (V1) is the transmitted signal from 50 ohms to 50 ohms, it will be equal to the incident signal. Measure V1 and this time record it as $V_{incident}$. Application of Equations 4 and 5 followed by a little algebraic manipulation yields the characteristic impedance of the signal line:

$$Z_0 = (V_{transmitted}/(2V_{incident}-V_{transmitted})) 50\Omega$$

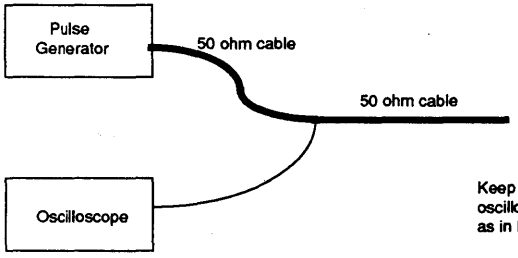
DESIGN HIGH PERFORMANCE MEMORY BOARDS USING SIMPLE TRANSMISSION LINE TECHNIQUES

AN218



Notes: The pulse generator must be set with a low enough amplitude and a high enough DC offset that reflections don't go below ground or above Vcc. The signal's edge rate must be less than twice the line delay. The oscilloscope probe must have a high impedance. The memory board should have power applied and the memory chips installed.

Figure 3a



Keep the pulse generator and oscilloscope settings the same as in Figure 3a.

Figure 3b

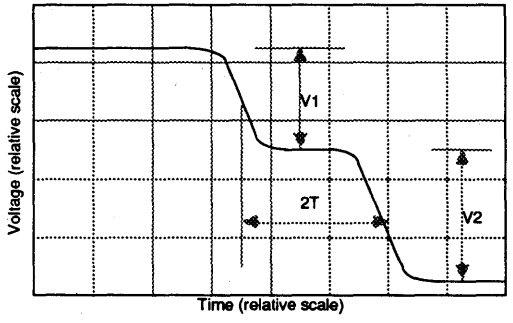


Figure 3c

DRIVER I-V CHARACTERISTICS

In order to anticipate the behavior of a particular driver in a memory board, an engineer will need to know the driver's I-V output characteristics. This information is given in Figures 4 and 5 for the parts which are used later as examples. Figure 4 shows the current each part will sink as a function of output voltage when it is in the low state, and Figure 5 shows the current each part will source as a function of output voltage when it is in the high state.

It should be noted that the curves for the 74F765 are representative of the standard 24ma FAST™ output, the curves for the 74F3037 are representative of the standard FAST™ 30 ohm line driver output, and the curves for the 74F765-1 are representative of all Signetics DRAM controllers which have a "dash one" designation.

PART 3: COMMON PROBLEMS AND THEIR SOLUTIONS

Transmission line problems in memory boards generally become significant when signal line propagation delays approach or exceed 1ns. The reasons for this will become apparent in the analysis of the following problems. A look at the "ballpark" estimates made earlier shows that a 1ns long transmission line translates to about 3 inches of DIP, 2 inches of ZIP, or 1 inch of SIP based memory line. Since these lengths are exceeded in most memory boards, transmission line problems are very common.

UNDERSHOOT

One of the most common problems noticed in memory design is a violation of the specified minimum input voltage of the memory chips (-1v). An example of this is shown in Figure 6 where a 24ma FAST™ part drives a 60 ohm line hard enough that the reflection at the opposite end of the line goes 3.5 volts below ground. This violation (usually referred to as "undershoot") would almost certainly cause the memory chips to malfunction.

The analysis of Figure 6 starts with a load-line method which proves to be very important for determining the incident wave. The 60 ohm transmission line of Figure 6 is initially settled to a high voltage of about 5 volts. When the line's driver then goes into the low state, its output voltage and current is given by the intersection of the driver's output I-V curve (Figure 4) with the input I-V curve of the transmission line. This input I-V curve is a line through the points (5v,0ma) and (0v,83ma) (from Equation 2), and the point of intersection of the two curves is about (.75v, 75ma). The incident voltage wave ($V_{incident}$) is a -4.25 volt change from 5 volts to .75 volts. This voltage wave propagates to the end of the line opposite the driver where it encounters an impedance change from 60 ohms to an infinite impedance. The reflected wave (from Equation 4) at this impedance change will be $V_{reflected} = V_{incident} = -4.25$ volts, i.e., a change from .75 volts to -3.5 volts, and subsequent reflections of this wave account for the continued peaks and valleys.

DESIGN HIGH PERFORMANCE MEMORY BOARDS USING SIMPLE TRANSMISSION LINE TECHNIQUES

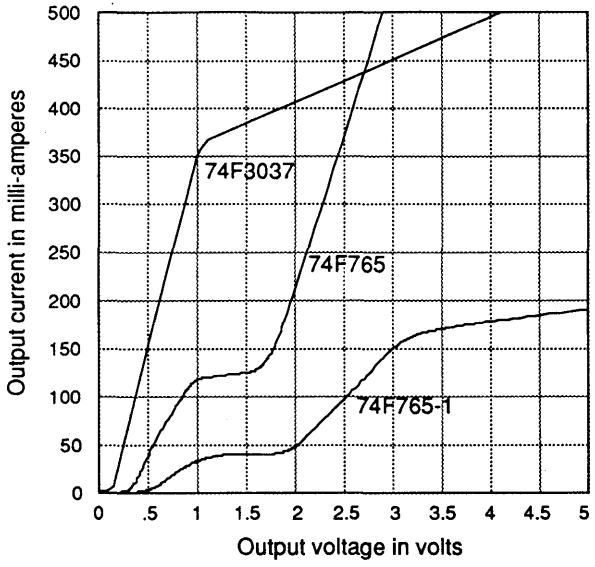


Figure 4 Voltage vs Current of Low State Outputs

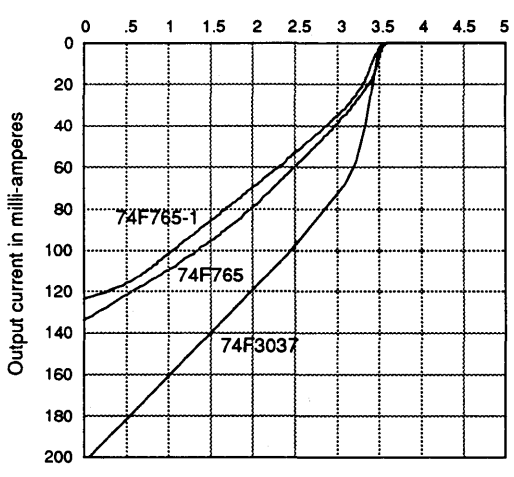


Figure 5 Voltage vs Current of High State Outputs

There are three basic methods an engineer can use to work around this problem.

Method 1. Use a slower driver and/or drive pieces of the line in parallel to effectively speed up the line.

Method 2. Increase the impedance of the driver or decrease that of the line.

Method 3. Put some finite impedance on the end of the line opposite the driver.

Method 1 (Slow Driver, Fast Line)

The idea behind the first method is to allow only one volt of the transition to fit onto the line at a time. By limiting the slew rate of the driver to less than 1 volt in twice the propagation delay of the line, one can guarantee that the undershoot will also be less than a volt. To apply this method to the example in Figure 6, we would break the 5ns long transmission line into four 1.25ns long sections and use a driver which made the 5 volt transition in a minimum of eight nanoseconds. The drawbacks of this method make it impractical for most designs. These drawbacks include:

- the requirement for a controlled slew rate driver with a very specific slew rate;
- the impact on timing due to the required slow transition time;
- the layout inconvenience of short memory lines in systems having more than an eight bit word.

Method 2 (Reflected Wave Switching, or "series termination")

The idea behind the second method is to reduce $V_{incident}$ to 50% of the total desired transition and then rely on the reflection from the unterminated end of the line to complete the transition. The usual way of doing this is by putting a resistor in series with the output of the driver (see Figure 7a) so that the impedance of the driver is roughly matched to that of the line. It is easy to show (from Equation 2) that this will result in an incident wave equal to half the desired transition and (from Equation 4) that the reflection from the unterminated end of the line will complete the transition. Since the driver's impedance is equal to that of the line, the reflected wave will not produce a second reflection when it returns to the driver (see Equation 4).

The two ends of a line driven with the series termination method are monitored by an oscilloscope in Figure 7b. Notice that the voltage at the driven end of the line is in the input threshold region for a time equal to twice the propagation delay of the line. This time spent in the threshold region often skews the address lines enough with respect to the row and column address strobes in dynamic memory boards that the row and column address setup times fail or become marginal. This problem can be avoided by allowing for an extra 2T worth of setup time in the design, but the increased delay quickly becomes

DESIGN HIGH PERFORMANCE MEMORY BOARDS USING SIMPLE TRANSMISSION LINE TECHNIQUES

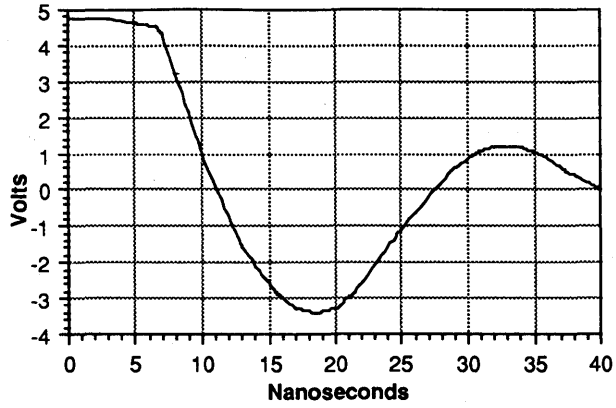


Figure 6 Oscilloscope view of the un-terminated end of an address line. The line has 32 DIPs, a line delay of 5ns, and it is driven by a 74F153.

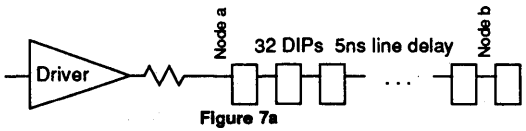


Figure 7a

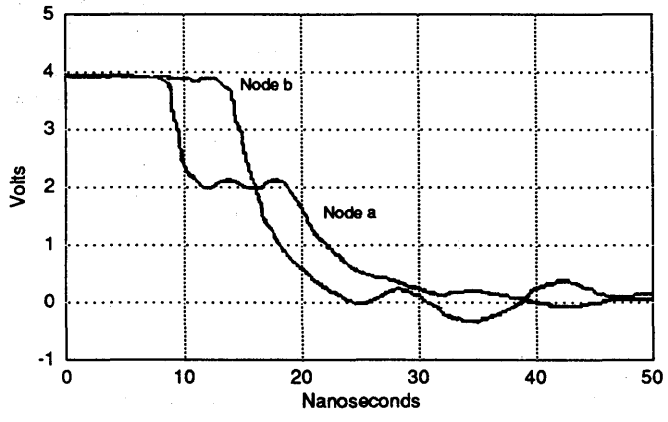


Figure 7b

a problem in large memory boards. Since any ground noise can easily cause multiple transitions to be made on signals which are left in the threshold region, this method should be used with caution on the strobe lines.

Series termination is probably the most widely used method for driving signal lines on memory boards. One reason for its popularity is that a very rough match between the driver's impedance and the impedance of the line will still make a memory line behave properly. It can be shown from Equations 2 and 4 that if the driver's impedance is within +50% and –40% of the line's characteristic impedance, the reflected wave will not violate the –1 volt minimum input voltage specification or the .8 volt maximum low input voltage specification. Thus a 30 ohm output impedance will work reasonably well with the ballpark estimates made previously for DIP and ZIP packages even if a large variation in input capacitance occurs from one memory chip vendor to the next.

The series termination method is offered by Signetics and several other companies in integrated circuits (the 74F721 and 74F723 for example). Signetics also offers an extension of this idea in some of its dynamic RAM controllers (see Figure 8). The output stage for these controllers will reflected wave switch lines in the 17 to 67 ohm range rather than the 18 to 45 ohm range one gets with the more conventional 30 ohm output impedance.

Method 3 (Terminations)

The basic idea behind this method is to place some terminating impedance at the end of the line opposite the driver. The simplest form of this would be a resistor ($R=Z_0$) to a constant voltage. In this case the reflection (undershoot) would be eliminated (see Equation 4). This termination can be generalized to the two resistor network in Figure 9c in which two resistors in parallel equal Z_0 and the terminating voltage is usually set to around three volts by a 2 to 3 ratio in the resistors. This termination offers very high performance, and it is particularly suited to high speed, high drive, open collector drivers like the 74F3038.

The high D.C. power dissipation of termination 9c can be avoided by using a capacitor to provide the constant voltage (see Figure 9e). This termination offers adequate undershoot suppression, and at the same time the lack of D.C. current flow often provides higher noise margins. This termination and the previous one should only be used in cases where the driver has adequate drive to fully switch the line with the incident wave, because there will be no reflection to make up for partial transitions.

Finally, Figure 9d shows a diode termination which can be used with any driver whether it is switching lines on the incident wave or not, and this termination has a lower power dissipation than either of the previous two terminations. This termination will also tend to speed up the transition time at the terminated end of the transmission line (notice that this transition time is always slow due to losses in

DESIGN HIGH PERFORMANCE MEMORY BOARDS USING SIMPLE TRANSMISSION LINE TECHNIQUES

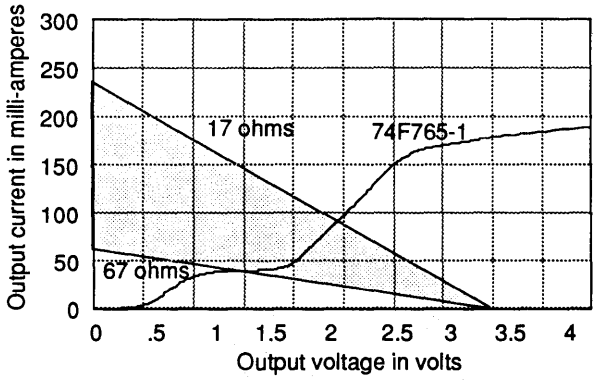


Figure 8 Current vs voltage for 74F765-1 output and 17 to 67 ohm transmission lines settled to 4 volts. Since the intersection of the output curve with each of the transmission line curves is between 1.5 and 2.4 volts, these impedances are all suited to first reflected wave switching by the 74F765-1 (the incident wave to 2.4 v will reflect to .8 v and the incident wave to 1.5 v will reflect to -1 v).

the line). The 74F133 has a high speed Schottky diode from ground to each of its 13 inputs, so it can be used as a low cost termination pack for this method. The method typically limits undershoot to just short of a volt which is not as good as can be achieved with the previous terminations, and the method is somewhat worse in relation to noise, but it can be used very effectively.

NOISE

Often, when one signal line is switched, voltage spikes (noise) will appear on adjacent lines. These voltage spikes can generally be traced to the lead frame inductance of the driver, the inductance of the ground plane, or the mutual inductance between adjacent signal lines. This noise is generally increased as transition times and line spacings are decreased and as line lengths are increased. Lines with terminations 9a, 9b and 9d will typically exhibit more noise than those terminated with 9c and 9e.

Noise can easily become a very serious problem in memory design, but Figure 10 shows that adherence to a few simple guidelines will keep noise down to an acceptable level even under the most adverse conditions. First, use a ground plane or minimize the length of the ground trace from the driver to the memory chips. Second, use lots of decoupling capacitors (especially on two layer boards). Finally, if noise does become a problem, change to a different termination and/or driver.

BRANCH INDUCED WAVEFORM DISTORTION

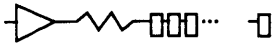
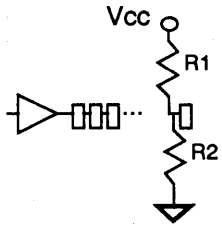
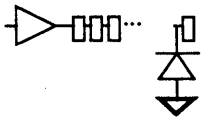
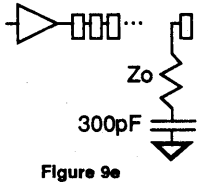
Infrequently, memory lines travel a considerable distance as a single line (several nanoseconds) and then branch into two or more directions. This can result in severe waveform distortion like that shown in Figure 11. In this example, a series terminated line travels 3ns as a single line and then splits into two parallel branches which are each 3ns long. The 2 volt incident wave travels down the line to the branch where the impedance of the line is effectively halved. At this point a reflection of $2\ V \times (.5\ Z_0 - Z_0)/(.5\ Z_0 + Z_0) = -.67$ volts travels back towards the driver, which drops the voltage of this first section of line back down from 2 volts to 1.3 volts. This section of the line stays at 1.3 volts for 6ns, at which point the reflections return from the unterminated ends of the two branches and bring the voltage back up above the input threshold again. The glitch seen at the driven end of this line would clearly be undesirable on any memory signal line.

Avoid long branches.

SUMMARY

The steadily increasing speed of memories, memory drivers and the systems these devices are being used in has created a need for engineers to understand, manipulate, subdue, or work around transmission line effects. This paper has presented the basic tools needed to accomplish this task, and it has given insight into where they are useful. Although several line driving and terminating techniques have been discussed, their individual advantages and disadvantages make it difficult to make general recommendations which are not tied to specific applications. The basic equations which govern transmission line behavior should augment the discussions on line driving and terminating techniques and their impact on undershoot and crosstalk, allowing the reader to adapt the ideas to his specific application.

DESIGN HIGH PERFORMANCE MEMORY BOARDS USING SIMPLE TRANSMISSION LINE TECHNIQUES

 Figure 9a	Reflections	- Large, edge rate dependent
	Noise	- Poor
	Power	+ Low power
	Noise Margins	+ Large noise margins
	Hints	Often equivalent to 9b when driving SIPs or parallel banks of DIPs or Zips
 Figure 9b	Reflections	+ Limits or eliminates undershoot
	Noise	Poor on very low impedances, but good on higher impedances.
	Power	+ Low power
	Noise Margins	+ Good DC noise margins
		- Leaves signals in the threshold for 2T during transitions
	Hints	Increases setup times by 2T
 Figure 9c	Reflections	+ Limits or eliminates undershoot
	Noise	+ Low noise
	Power	- High power
	Noise Margins	- Usually has poor noise margins unless high current drivers are used
	Hints	Works well with high speed, high drive, open collector parts like the 74F3038 Only good for incident wave switched lines $Z_0 = R1R2/(R1+R2)$
 Figure 9d	Reflections	+ Typically limits undershoot to just less than a volt
	Noise	- Poor
	Power	+ Low power
	Noise Margins	+ Large noise margins once reflections have settled out -1 volt undershoot tends to reflect for several times the line delay which leaves the line somewhat susceptable to noise
	Hints	74F133 can be used as a diode pack. Avoid extremely fast edge rates.
 Figure 9e	Reflections	+ Limits or eliminates undershoot
	Noise	+ Good
	Power	+ Low DC power dissipation
	Noise Margins	+ Large noise margins
	Hints	Primarily for incident wave switched lines

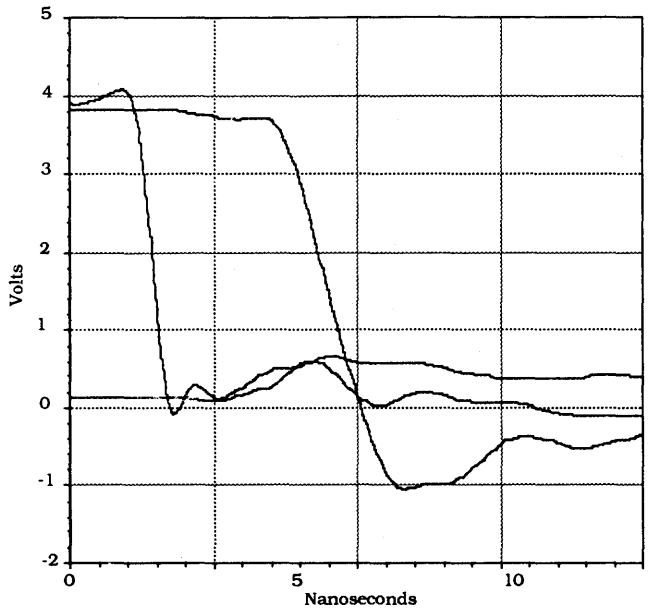


Figure 10 Two adjacent diode terminated lines driven by a 74F3037 on a dual layer Board. The sub-nanosecond edge rate of the driver does not induce excessive noise on the adjacent line even in this poor environment.

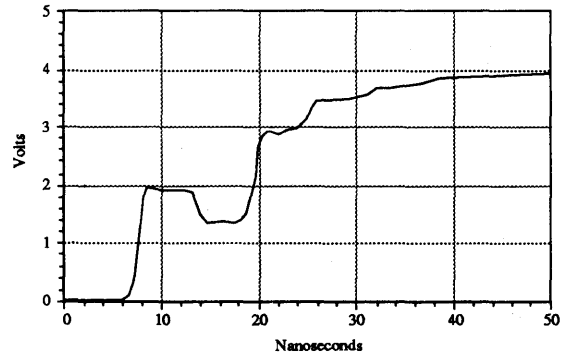


Figure 11 Branch induced waveform distortion

Signetics

AN SMD-100
Thermal Considerations For Surface Mounted Devices

INTRODUCTION

Thermal characteristics of integrated circuit (IC) packages have always been a major consideration to both producers and users of electronics products. This is because an increase in junction temperature (T_J) can have an adverse effect on the long term operating life of an IC. As will be shown in this paper, the advantages realized by miniaturization can often have trade-offs in terms of increased junction temperatures. Some of the **VARIABLES affecting T_J are controlled by the PRODUCER of the IC, while others are controlled by the USER and the ENVIRONMENT in which the device is used.**

With the increased use of Surface Mount Device (SMD) technology, management of thermal characteristics remains a valid concern because not only are the SMD packages much smaller, but the thermal energy is concentrated more densely on the printed wiring board (PWB). For these reasons, the designer and manufacturer of surface mount assemblies (SMAs) must be more aware of all the variables affecting T_J.

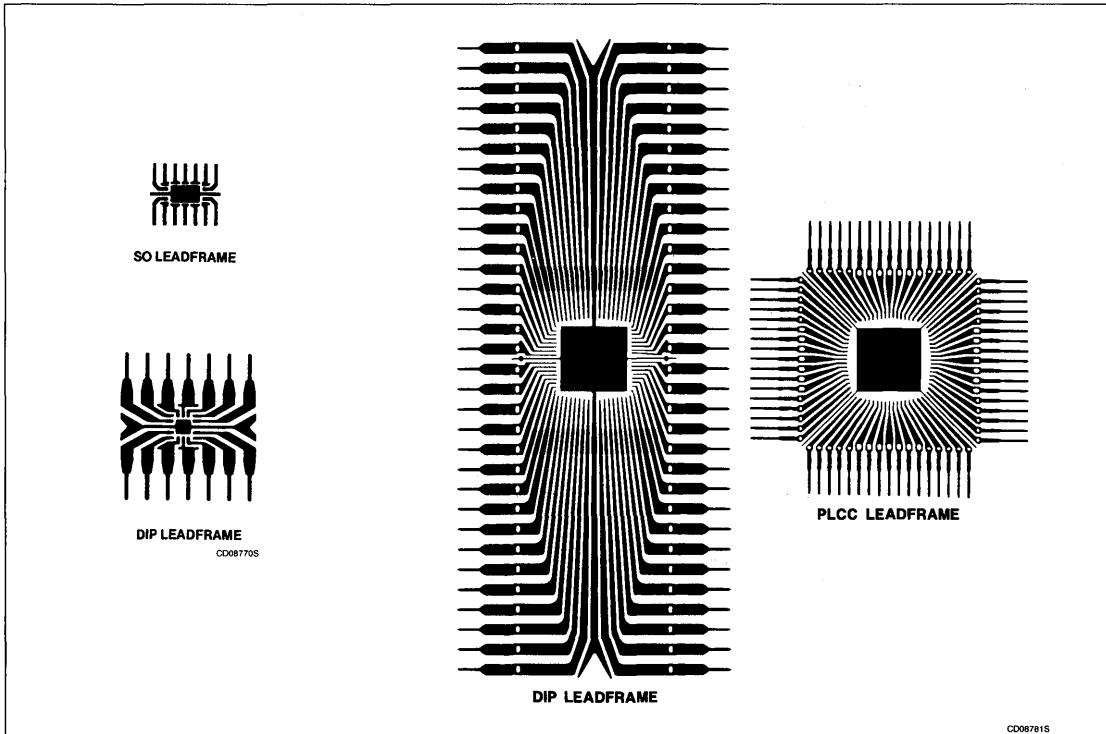
POWER DISSIPATION

Power dissipation (P_D), varies from one device to another and can be obtained by multiplying V_{CC} Max by typical I_{CC}. Since I_{CC} decreases with an increase in temperature, maximum I_{CC} values are not used.

THERMAL RESISTANCE

The ability of the package to conduct this heat from the chip to the environment is expressed in terms of thermal resistance. The term normally used is Theta JA (θ_{JA}). θ_{JA} is often separated into two components: thermal resistance from the junction to case, and the thermal resistance from the case to ambient. θ_{JA} represents the total resistance to heat flow from the chip to ambient and is expressed as follows:

$$\theta_{JC} + \theta_{CA} = \theta_{JA}$$



a. SO-14 Leadframe Compared to a 14-Pin DIP Leadframe

b. PLCC-68 Leadframe Compared to a 64-Pin DIP Leadframe

Figure 1

Thermal Considerations For Surface Mounted Devices

JUNCTION TEMPERATURE (T_J)

Junction temperature (T_J) is the temperature of a powered IC measured by Signetics at the substrate diode. When the chip is powered, the heat generated causes the T_J to rise above the ambient temperature (T_A). T_J is calculated by multiplying the power dissipation of the device by the thermal resistance of the package and adding the ambient temperature to the result.

$$T_J = (P_D \times \theta_{JA}) + T_A$$

FACTORS AFFECTING θ_{JA}

There are several factors which affect the thermal resistance of any IC package. Effective thermal management demands a sound understanding of all these variables. Package variables include the leadframe design and materials, the plastic used to encapsulate the device, and to a lesser extent other variables such as the die size and die attach methods. Other factors that have a significant impact on the θ_{JA} include the substrate upon which the IC is mounted, the density of the layout, the air-gap between the package and the substrate, the number and length of traces on the board, the use of thermally conductive epoxies, and external cooling methods.

PACKAGE CONSIDERATIONS

Studies with dual-in-line plastic (DIP) packages over the years have shown the value of proper leadframe design in achieving minimum thermal resistance. SMD leadframes are smaller than their DIP counterparts (see Figures 1a and 1b). Because the same die is used in each of the packages, the die-pad, or flag, must be at least as large in the SO as in the DIP.

While the size and shape of the leads have a measurable effect on θ_{JA}, the design factors that have the most significant effect are the die-pad size and the tie-bar size. With design constraints caused by both miniaturization and the need to assemble packages in an automated environment, the internal design of an SMD is much different than in a DIP. However, the design is one that strikes a balance between the need to miniaturize, the need to automate the assembly of the package, and the need to obtain optimum thermal characteristics.

LEAD FRAME MATERIAL is one of the more important factors in thermal management. For years the DIP leadframes were constructed out of Alloy-42. These leadframes met the producers' and users' specifications in quality and reliability. However three to five years ago, the leadframe material of DIPs was changed from Alloy-42 to Copper (CLF) in order to provide reduced θ_{JA} and extend the reliable temperature-operating range. While this change has already taken place for the DIP, it is still taking place for the SO package. Signetics began making 14-pin SO packages with CLF in April 1984 and completed conversion to CLF for all SO packages by 1985. As is shown in Figures 10 through 14, the change to CLF is producing dramatic results in the θ_{JA} of SO packages. All PLCCs are assembled with copper leadframes.

The MOLDING COMPOUND is another factor in thermal management. The compound used by Signetics and Philips is the same high purity epoxy used in DIP packages (at present, HC-10, Type II). This reduces corrosion caused by impurities and moisture.

OTHER FACTORS often considered are the die size, die attach methods, and wire bonding. Tests have shown that die size has a minor effect on θ_{JA} (see Figures 10 through 14).

While there is a difference between the thermal resistance of the silver-filled adhesive used for die attach and a gold silicon eutectic die attach, the thickness of this layer (1 – 2 mils) is so small as to make the difference insignificant.

Gold wire bonding in the range of 1.0 to 1.3 mils does not provide a significant thermal path in any package.

In summary, the SMD leadframe is much smaller then in a DIP and, out of necessity, is designed differently; however, the SMD package offers an adequate θ_{JA} for all moderate power devices. Further, the change to CLF will reduce the θ_{JA} even more, lowering the T_J and providing an even greater margin of reliability.

SIGNETICS' THERMAL RESISTANCE MEASUREMENTS — SMD PACKAGES

The graphs illustrated in this application note show the thermal resistance of Signetics' SMD devices. These graphs give the relationship between θ_{JA} (junction-to-ambient) or θ_{JC} (junction-to-case) and the device die size. Data is also provided showing the difference between still air (natural convection cooling) and air flow (forced cooling) ambients. All θ_{JA} tests were run with the SMD device soldered to test boards (See the Test Ambient section for details). It is important to recognize that the test board is an essential part of the test environment and that boards of different sizes, trace layouts or compositions may give different results from this data. Each SMD user should compare their system to the Signetics test system and determine if the data is appropriate or needs adjustment for their application.

Test Method

Signetics uses what is commonly called the TSP (temperature sensitive parameter) method. This method meets MIL-STD 883C, Method 1012.1. The basic idea of this method is to use the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power dissipation. The thermal resistance can be calculated using the following equation:

$$\theta_{JA} = \frac{\Delta T_J}{P_D} = \frac{T_J - T_A}{P_D}$$

Test Procedure

TSP Calibration

The TSP diode is calibrated using a constant temperature oil bath and constant current power supply. The calibration temperatures used are typically 25°C and 75°C and are measured to an accuracy of ±0.1°C. The calibration current must be kept low to avoid significant junction heating, data given in this report used constant currents of either 1.0mA or 3.0mA. The temperature coefficient (K-Factor) is calculated using the following equation:

$$K = \frac{T_2 - T_1}{V_{F2} - V_{F1}} \quad \Big| \quad I_F = \text{Constant}$$

Where: K = Temperature Coefficient (°C/mV)
T_2 = Higher Test Temperature (°C)
T_1 = Lower Test Temperature (°C)
V_{F2} = Forward Voltage at I_F and T_2
V_{F1} = Forward Voltage at I_F and T_1
I_F = Constant Forward Measurement Current
(See Figure 2)

Thermal Resistance Measurement

The thermal resistance is measured by applying a sequence of constant current and constant voltage pulses to the device under test. The constant current pulse (same current at which the TSP was calibrated) is used to measure the forward voltage of the TSP. The constant voltage pulse is used to heat the part. The measurement pulse is very short

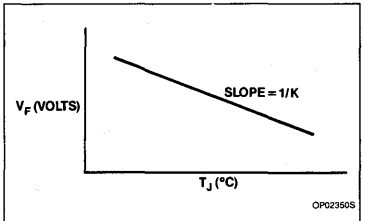


Figure 2. Forward Voltage — Junction Temperature Characteristics of a Semiconductor Junction Operating at a Constant Current. The K Factor is the Reciprocal of the Slope

Thermal Considerations For Surface Mounted Devices

(less than 1% of cycle) compared to the heating pulse (greater than 99% of cycle) to minimize junction cooling during measurement. This cycle starts at ambient temperature and continues until steady-state conditions are reached. The thermal resistance can then be calculated using the following equation:

$$\theta_{JA} = \frac{\Delta T_J}{P_D} = \frac{K\ (V_{FA} - V_{FS})}{V_H \times I_H}$$

Where: V_{FA} = Forward Voltage of TSP at Ambient Temperature (mV)
V_{FS} = Forward Voltage of TSP at Steady-State Temperature (mV)
V_H = Heating Voltage (V)
I_H = Heating Current (A)

Test Ambient

θ_{JA} Tests

All θ_{JA} test data collected in this application note was obtained with the SMD devices soldered to either Philips SO Thermal Resistance Test Boards or Signetics PLCC Thermal Resistance Test Boards with the following parameters:

Board size - SO Small: 1.12″ × 0.75″ × 0.059″
- SO Large: 1.58″ × 0.75″ × 0.059″
- PLCC: 2.24″ × 2.24″ × 0.062″

Board Material - Glass epoxy, FR-4 type with 1 oz. sq.ft. copper solder coated

Board Trace Configuration - See Figure 3.

SO devices are set at 8 – 9 mil stand-off and SO boards use one connection pin per device lead. PLCC boards generally use 2 – 4 connection pins regardless of device lead count. Figure 5 shows a cross-section of an SO part soldered to test board and Figure 4 shows typical board/device assemblies ready for θ_{JA} Test.

The still air tests were run in a box having a volume of 1 cubic foot of air at room temperature. The air flow tests were run in a 4″ × 4″ cross-section by 26″ long wind tunnel with air at room temperature. All devices were soldered on test boards and held in a horizontal test position. The test boards were held in a Textool ZIF socket with 0.16″ stand-off. Figure 6 shows the air flow test setup.

θ_{JC} Tests

The θ_{JC} test is run by holding the test device against an "infinite" heat sink (water cooled block approximately 4″ × 7″ × 0.75″) to give a θ_{CA} (case-to-ambient) approaching zero. The copper heat sink is held at a constant temperature (≈20°C) and monitored with a thermocouple (0.040″ diameter sheath, grounded junction type K) mounted flush with heat sink surface and centered below die in the test device. Figure 7 shows the θ_{JC} test mounting for a PLCC device.

SO devices are mounted with the bottom of the package held against the heat sink. This is achieved by bending the device leads straight out from the package body. Two small wires are soldered to the appropriate leads for tester connection. Thermal grease is used between the test device and heat sink to assure good thermal coupling.

PLCC devices are mounted with the top of the package held against the heat sink. A small spacer is used between the hold-down mechanism and PLCC bottom pedestal. Small hook up wires and thermal grease are used as with the SO setup. Figure 7 shows the PLCC mounting.

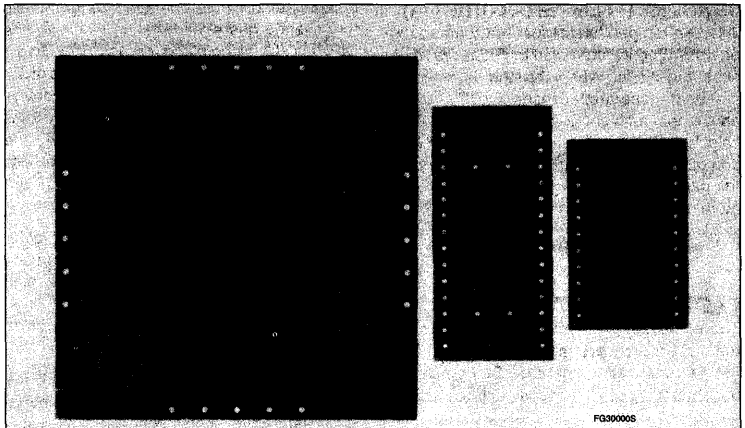


Figure 3. Board Trace Configuration for Thermal Resistance Test Boards

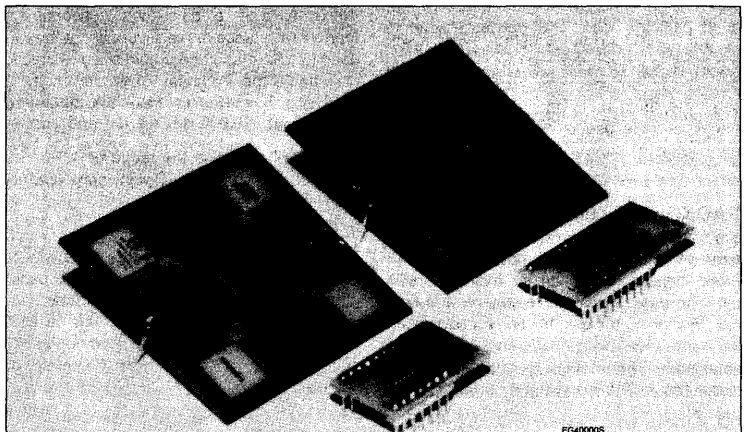


Figure 4. Device/Board Assemblies

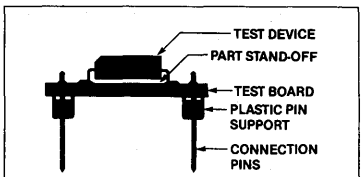


Figure 5. Cross-Section of Test Device Soldered to Test Board

Thermal Considerations For Surface Mounted Devices

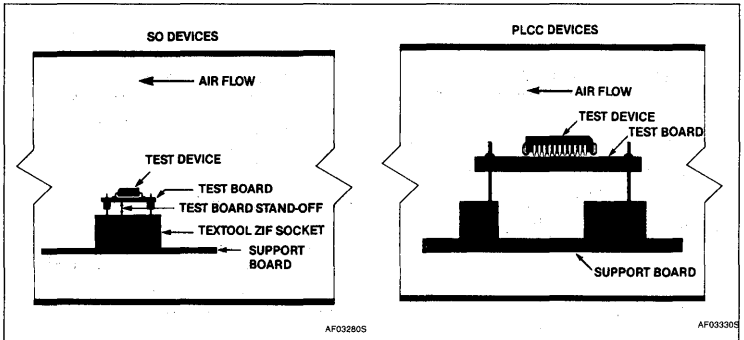


Figure 6. Air Flow Test Setup

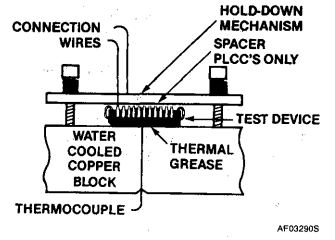


Figure 7. θ_{JC} Test Setup With PLCC Device

DATA PRESENTATION

The data presented in this application note was run at constant power dissipation for each package type. The power dissipation used is given under Test Conditions for each graph. Higher or lower power dissipation will have a slight effect on thermal resistance. The general trend of thermal resistance decreasing with increasing power is common to all packages. Figure 8 shows the average effect of power dissipation on SMD θ_{JA}.

Thermal resistance can also be affected by slight variations in internal leadframe design such as pad size. Larger pads give slightly lower thermal resistance for the same size die. The data presented represents the typical Signetics leadframe/die combinations with large die on large pads and small die on small pads. The effect of leadframe design is within the ±15% accuracy of these graphs.

SO devices are currently available in both copper or alloy 42 leadframes; however, Signetics is converting to copper only. PLCC devices are only available using copper leadframes.

The average lowering effect of air flow on SMD θ_{JA} is shown in Figure 9.

Thermal Calculations

The approximate junction temperature can be calculated using the following equation:

$$T_J = (\theta_{JA} \times P_D) + T_A$$

Where: T_J = Junction Temperature (°C)
θ_{JA} = Thermal Resistance Junction-to-Ambient (°C/W)
P_D = Power Dissipation at a T_J ($V_{CC} \times I_{CC}$) (W)
T_A = Temperature of Ambient (°C)

Example: Determine approximate junction temperature of SOL-20 at 0.5W dissipation using 10,000 sq. mil die and copper leadframe in still air and 200 LFPM air flow ambients. Given T_A = 30°C,

1. Find θ_{JA} for SOL-20 using 10,000 sq. mil die and copper leadframe from typical θ_{JA} data —SOL-20 graph.
   Answer: 88°C/W @ 0.7W
2. Determine θ_{JA} @ 0.5W using Average Effect of Power Dissipation on AMD θ_{JA}, Figure 8.

   Percent change in Power =

   $$\frac{0.5W - 0.7W}{0.7W} \times 100 = -28.6\%$$

   From Figure 8:
   28.6% change in power gives 3.5% increase in θ_{JA}
   Answer:
   88°C/W + (88 × 0.035) = 91°C/W @ 0.5W
3. Determine θ_{JA} @ 0.5W in 200 LFPM air flow from Average Effect of Air Flow on SMD θ_{JA}, Figure 9.
   From Figure 9:
   200 LFPM air flow gives 14% decrease in θ_{JA}
   Answer:
   91°C/W – (91 × 0.14) = 78°C/W
4. Calculate approximate junction temperature
   Answer:
   T_J (still air) = (91°C/W × 0.5W) + 30 = 76°C
   T_J (200 LFPM) = (78°C/W × 0.5W) + 30 = 69°C

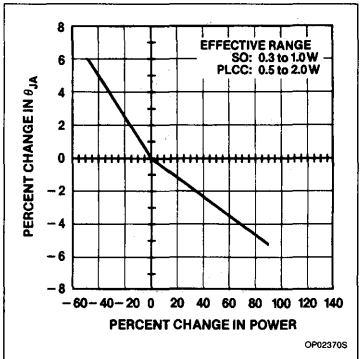


Figure 8. Average Effect of Power Dissipation on SMD θ_{JA}

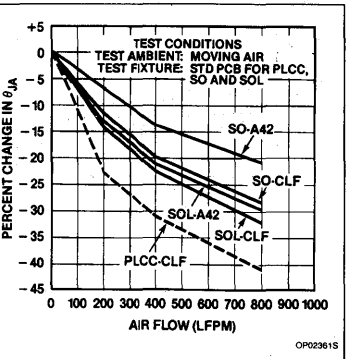
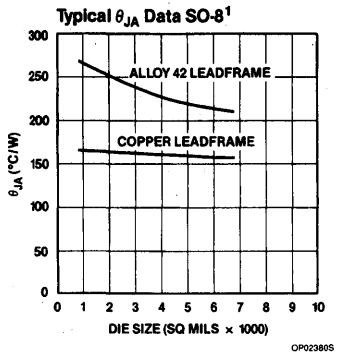
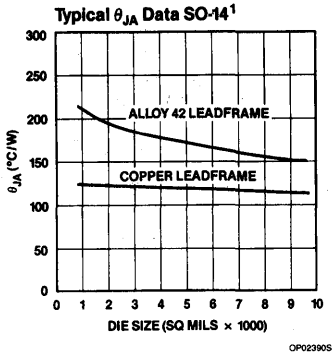
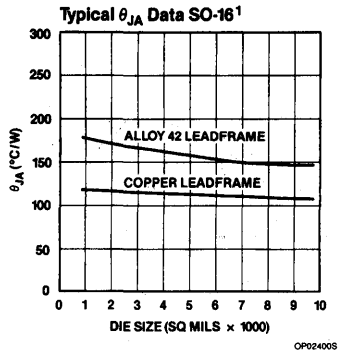


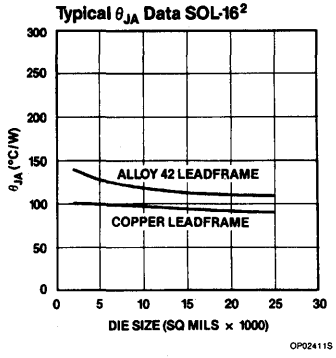
Figure 9. Average Effect of Air Flow on SMD θ_{JA}

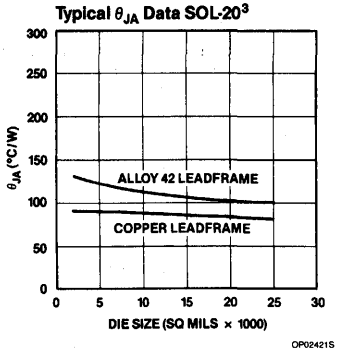
TYPICAL SMD THERMAL (θ_{JA})

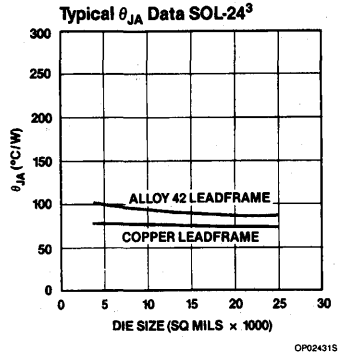


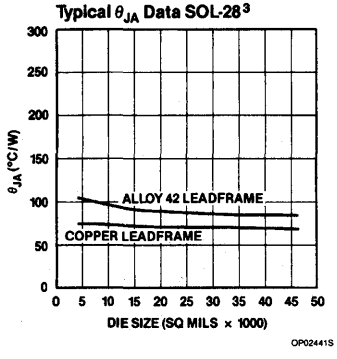












NOTES:

1. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	0.5W
Test fixture:	Philips PCB (1.12" × 0.75" × 0.059")
Accuracy:	±15%

2. TEST CONDITIONS:

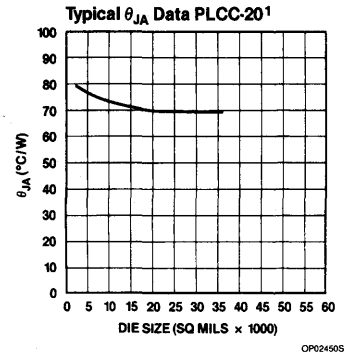
Test ambient:	Still air
Power dissipation:	0.5W
Test fixture:	Philips PCB (1.58" × 0.75" × 0.059")
Accuracy:	±15%

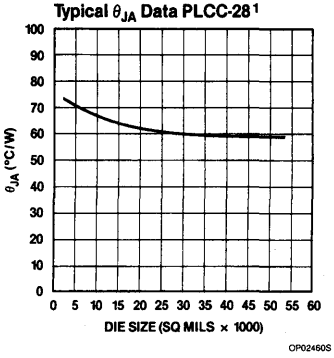
3. TEST CONDITIONS:

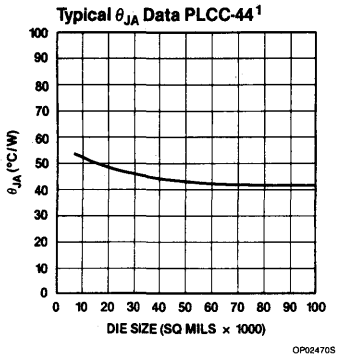
Test ambient:	Still air
Power dissipation:	0.7W
Test fixture:	Philips PCB (1.58" × 0.75" × 0.059")
Accuracy:	±15%

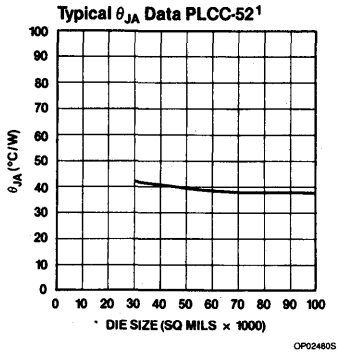
Figure 10

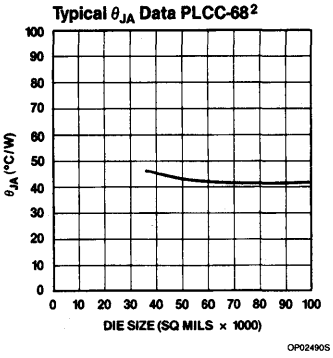
TYPICAL SMD THERMAL (θ_{JA})

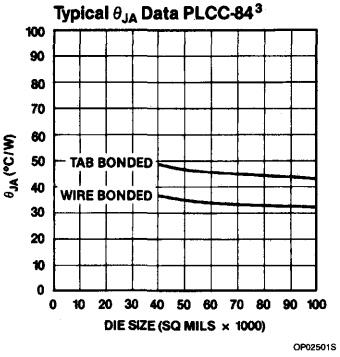












NOTES:

1. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	0.75W
Test fixture:	Signetics PCB (2.24" × 2.24" × 0.062")
Accuracy:	±15%

2. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	1.0W
Test fixture:	Signetics PCB (2.24" × 2.24" × 0.062")
Accuracy:	±15%

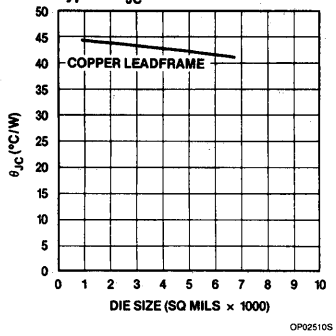
3. TEST CONDITIONS:

Test ambient:	Still air
Power dissipation:	1.5W
Test fixture:	Signetics PCB (2.24" × 2.24" × 0.062")
Accuracy:	±15%

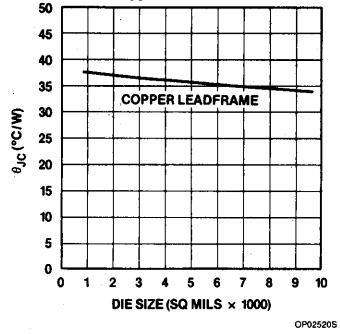
Figure 11

TYPICAL SMD THERMAL (θ_{JC})

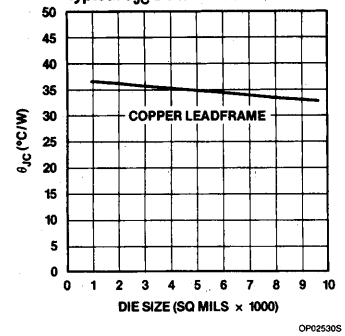
Typical θ_{JC} Data SO-8 [1]



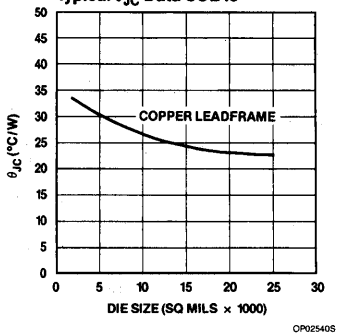
Typical θ_{JC} Data SO-14 [1]



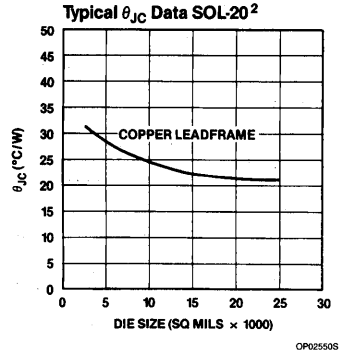
Typical θ_{JC} Data SO-16 [1]



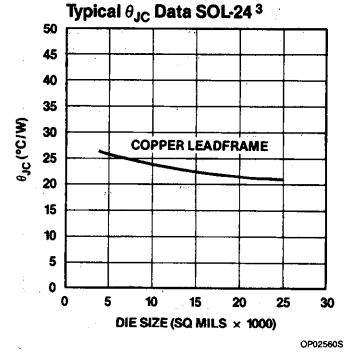
Typical θ_{JC} Data SOL-16 [1]



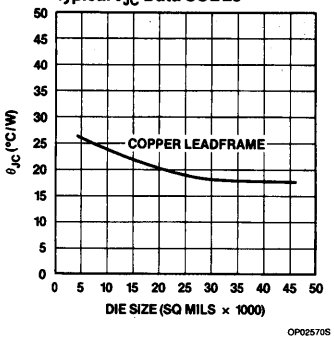
Typical θ_{JC} Data SOL-20 [2]



Typical θ_{JC} Data SOL-24 [3]



Typical θ_{JC} Data SOL-28 [3]



NOTES:

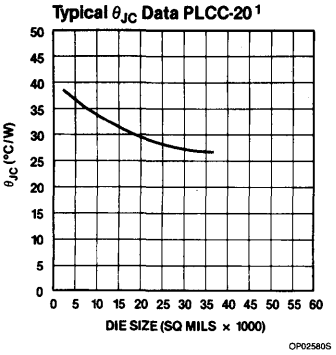
1. TEST CONDITIONS:
Power dissipation: 0.5W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

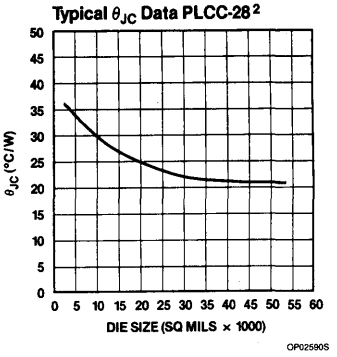
2. TEST CONDITIONS:
Power dissipation: 0.7W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

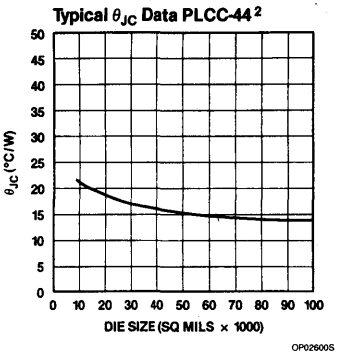
3. TEST CONDITIONS:
Power dissipation: 1.0W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

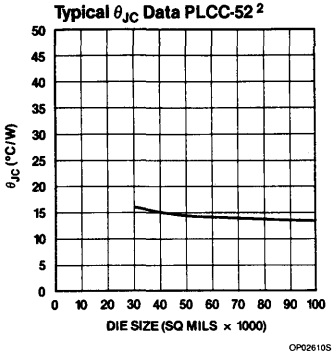
Figure 12

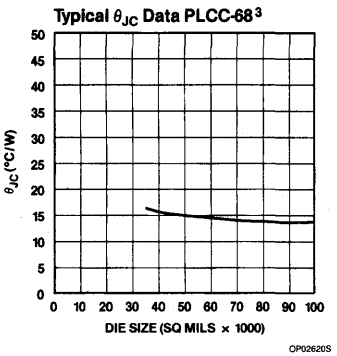
TYPICAL SMD THERMAL (θ_{JC})

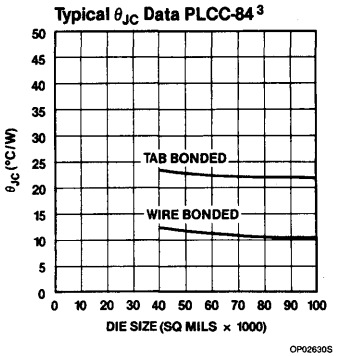












NOTES:

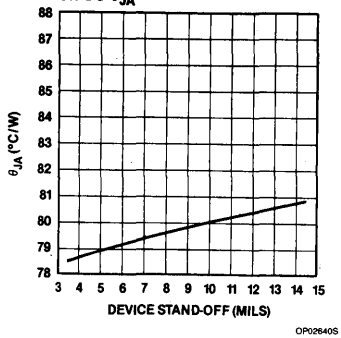
1. TEST CONDITIONS:
Power dissipation: 0.75W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

2. TEST CONDITIONS:
Power dissipation: 1.0W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

3. TEST CONDITIONS:
Power dissipation: 2.0W
Test fixture: "Infinite" heat sink
Accuracy: ±15%

Figure 13

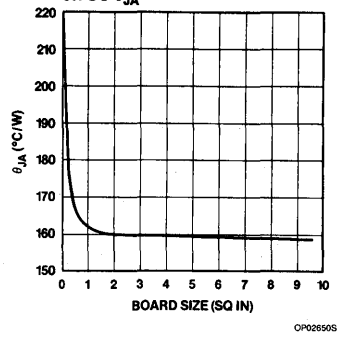
Effect of Device Stand-Off on SO θ_{JA}[1]



NOTES:
1. TEST CONDITIONS:

Package type:	SOL-20 CLF
Die size:	11,322 sq mils
Test ambient:	Still air
Power dissipation:	0.75W
Test fixture:	Philips PCB (1.58" × 0.75" × 0.059")

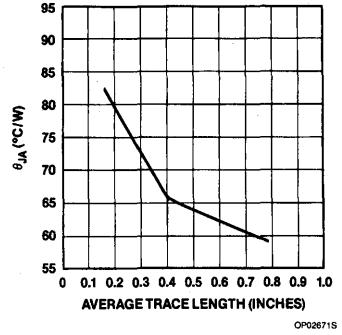
Effect of Board Size on SO θ_{JA}[2]



2. TEST CONDITIONS:

Package type:	SO-14 CLF
Die size:	5,040 sq mils
Test ambient:	Still air
Power dissipation:	0.6W
Test fixture:	0.062" thick PCB with "No Traces" 8-9 MIL stand-off

Effect of Trace Length on 28-Lead PLCC θ_{JA}[3]



3. TEST CONDITIONS:

Package type:	PLCC-28 CLF
Die size:	10,445 sq mils
Test ambient:	Still air
Power dissipation:	1.0W
Test fixture:	Signetics PCB (2.24" × 2.24" × 0.062") trace 27 MIL wide 1 oz SQ ft copper

Figure 14

Thermal Considerations For Surface Mounted Devices

SYSTEM CONSIDERATIONS

With the increases in layout density resulting from surface mounting with much smaller packages, other factors become even more important. THE USER IS IN CONTROL OF THESE FACTORS.

One of the most obvious factors is the substrate material on which the parts are mounted. Environmental constraints, cost considerations and other factors come into play when choosing a substrate. The choice is expanding rapidly, from the standard glass epoxy PWB materials and ceramic substrates to flexible circuits, injection molded plastics, and coated metals. Each of these has its own thermal characteristics which must be considered when choosing a substrate material.

Studies have shown that the air gap between the bottom of the package and the substrate has an effect on θ_{JA}. The larger the gap, the higher the θ_{JA}. Using thermally conductive epoxies in this gap can slightly reduce the θ_{JA}.

It has long been recognized that external cooling can reduce the junction temperatures of devices by carrying heat away from both the devices and the board itself. Signetics has done several studies on the effects of external cooling on boards with SO packages. The results are shown in Figures 15 through 18.

The designer should avoid close spacing of high power devices so that the heat load is spread over as large an area as possible. Locate components with a higher junction temperature in the cooler locations on the PCBs.

The number and size of traces on a PWB can affect θ_{JA} since these metal lines can act as radiators, carrying heat away from the package and radiating it to the ambient. Although the chips themselves use the same amount of energy in either a DIP or an SO package, the increased density of a Surface Mounted Assembly concentrates the thermal energy into a smaller area.

It is evident that nothing is free in PWB layout. More heat concentrated into a smaller area makes it incumbent on the system designer to provide for the removal of thermal energy from his system.

Large conductor traces on the PCB conduct heat away from the package faster than small traces. Thermal vias from the mounting surface of the PCB to a large area ground plane in the PCB reduces the heat buildup at the package.

In addition to the package's thermal considerations, thermal management requires one to at least be aware of potential problems caused by mismatch in thermal expansion.

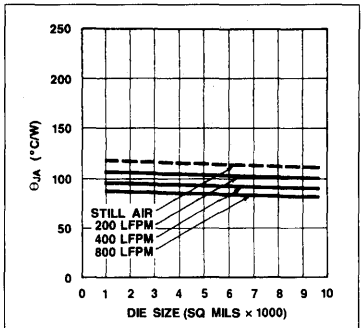


Figure 15. Results of Air Flow on θ_{JA} on SO-14 With Copper Leadframe

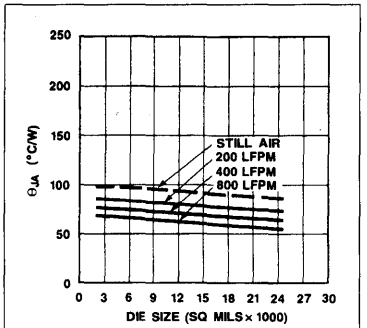


Figure 16. Results of Air Flow on θ_{JA} on SOL-16 With Copper Leadframe

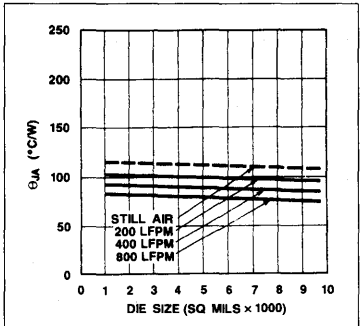


Figure 17. Results of Air Flow on θ_{JA} on SO-16 With Copper Leadframe

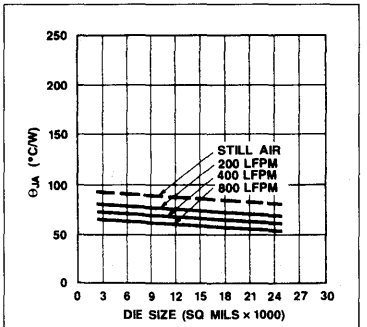


Figure 18. Results of Air Flow on θ_{JA} on SOL-20 With Copper Leadframe

The very nature of the SMD assembly, where the devices are soldered directly onto the surface, not through it, results in a very rigid structure. If the substrate material exhibits a different thermal coefficient of expansion (TCE) than the IC package, stresses can be setup in the solder joints when they are subjected to temperature cycling (and during the soldering process itself) that may ultimately result in failure.

Because some of the boards assembled will require the use of Leadless Ceramic Chip Carriers (LCCCs), TCE must be understood. As will be seen below, TCE is less of a problem with the commercial SMD packages with leads.

Take the example of a leadless ceramic chip carrier with a TCE of about 6×10^{-6}/K soldered to a conventional glass-epoxy laminate with a TCE in the region of 16×10^{-6}/K. This thermal expansion mismatch has been shown to fracture the solder joints during thermal cycling. Substrate materials with matched TCEs should be evaluated for these SMD assemblies to avoid problems caused by thermal expansion mismatch.

The stress level associated with thermal expansion and contraction of small SMDs such as capacitors and resistors, where the actual change in length is small, are normally rather low. However, as component sizes increase, stresses can increase substantially.

Thermal expansion mismatch is unlikely to cause too many problems in systems operating in benign environments; but, in harsher conditions, such as thermal cycling in military or avionic applications, the mechanical stresses setup in solder joints due to the different TCEs of the substrate and the component are likely to cause failure.

The basic problem is outlined in Figure 19. The leadless SMD is soldered to the substrate as shown, resulting in a very rigid structure. If the substrate material exhibits a different TCE from that of the SMD material, the amount of expansion for each will differ for any given increase in temperature. The soldered joint will have to accommodate this difference, and failure can ultimately result. The larger the component size, the higher the stress levels so that this phenomenon is at its most critical in applications requiring large LCCCs with high pin-counts.

Thermal Considerations For Surface Mounted Devices

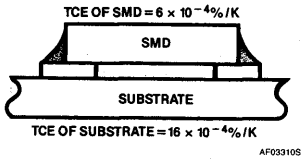


Figure 19. The Basic Problem of Thermal Expansion Mismatch Is That the Substrate and Component May Each Have Different Thermal Coefficients of Expansion.

NOTE: Data provided by N.V. Philips

To address this problem, three basic solutions are emerging. First, the use of leadless ceramic chip carriers can sometimes be avoided by using leaded devices; the leads can flex and absorb the stress. Second, when this solution is not feasible, the stresses can be taken up by inserting a compliant elastomeric layer between the ceramic package and the epoxy glass substrate. Third, TCE values of component and substrate can be matched.

USING LEADED DEVICES (SO, SOL & PLCC)

The current evolution in commercial electronics includes the adoption of the commercial SMD packages, i.e. SO with gull-wing leads or the PLCC with rolled-under J-leads, rely on the compliance of the leads themselves to avoid any serious problems of thermal expansion mismatch. At elevated temperatures, the leads flex slightly and absorb most of the mechanical stress resulting from the thermal expansion differentials.

Similarly, leaded holders can be used with LCCCs to attach them to the substrate and thus absorb the stress.

Unfortunately, using a lead does not always ensure sufficient compliancy. The material from which the lead is made, and the way it is formed and soldered can adversely affect it. For example, improper soldering techniques, which cause excess solder to over-fill the bend of the gull-wing lead of an SO can significantly reduce the lead's compliancy.

COMPLIANT LAYER

This approach introduces a compliant layer onto the interface surface of the substrate to absorb some of the stresses. A 50μm thick elastomeric layer is bonded to the laminate. To make contacts, carbon or metalic powders are introduced to form conductive stripes in the nonconductive elastomer material. Unfortunately, substrates using this technique are substantially more expensive than standard uncoated boards.

Another solution is to increase the compliancy of the solder joint. This is done by increasing the stand-off height between the underside of the component and the substrate. To do this, a solder paste containing lead or ceramic spheres which do not melt when the surrounding solder reflows, thus keeping the component above the substrate can be used.

MATCHING TCE

There are two ways to approach this solution. The TCE of the substrate laminate material can be matched to that of the LCCC either by replacing the glass fibers with fibers exhibiting a lower TCE (composites such as epoxy-Kevlar® or polyimide-Kevlar and polyimide-quartz), or by using low TCE metals (such as Invar®, Kovar, or molybdenum).

This latter approach involves bonding a glass-polyimide or a glass-epoxy multilayer to the low TCE restraining core material. Typical of such materials are copper-Invar-copper, Alloy-42, copper-molybdenum-copper, and copper-graphite. These restraining-core constructions usually require that the laminate be bonded to both sides to form a balanced structure so that they will not warp or twist.

This inevitably means an increase in weight, which has always been a negative factor in this approach. However, the SMD substrate can be smaller and the components more densely packed in many cases overcoming the weight disadvantages. On the positive side, the material's high thermal conductivity helps to keep the components cool. Moreover, copper-clad-Invar lends itself readily to moisture-proof multilayering for the creation of ground and power planes and for providing good inherent EMI/RFI shielding.

Kevlar is lighter and widely used for substrates in military applications; but, it suffers from a serious drawback which, although overcome to a certain extent by careful attention to detail, can cause problems. The material, when laminated, can absorb moisture and chemical processing fluids around the edges. Thermal conductivity, machinability and cost are not as attractive as for copper-clad Invar.

For the majority of commercial substrates however, where the use of ceramic chip carriers in any quantity is the exception rather than the rule, and when adequate cooling is available, the mismatch of TCEs poses little or no problem. For these substrates traditional FR-4 glass-epoxy and phenolic-paper will no doubt remain the most widely used materials.

Although FR-4 epoxy-glass has been the traditional material for plated-through professional substrates, it is phenolic-paper laminate (FR-2) which finds the widest use in consumer electronics. While it is the cheapest material, it unfortunately has the lowest dimensional stability, rendering it unsuitable for the mounting of LCCCs.

SUBSTRATE TYPES

FR-4 glass-epoxy substrates are the most commonly used for commercial electronic circuits. They have the advantage of being cheap, machinable, and lightweight. Substrate size is not limited. On the negative side, they have poor thermal conductivity and a high TCE, between 13 and 17 $\times$ 10^{-6}/K. This means they are a poor match to ceramic.

Glass polyimide substrates have a similar TCE range to glass-epoxy boards, but better thermal conductivity. They are, however, three to four times more expensive.

Polyimide Kevlar substrates have the advantage of being lightweight and not restricted in size. Conventional substrate processing methods can be used and its TCE (between 4 and 8), matches that of ceramic. Its disadvantages are that it is expensive, difficult to drill and is prone to resin microcracking and water absorption.

Polyimide quartz substrates have a TCE between 6 and 12 making them a good match for LCCCs. They can be processed using conventional techniques, although drilling vias can be difficult. They have good dielectric properties and compare favorably with FR-4 for substrate size and weight.

Alumina (ceramic) substrates are used extensively for high-reliability military applications and thick-film hybrids. The weight, cost, limited substrate size and inherent brittleness of alumina means that its use as a substrate material is limited to applications where these disadvantages are outweighed by the advantage of good thermal conductivity and a TCE that exactly matches that of LCCCs. A further limitation is that they require Thick-film screening processing.

Copper-clad Invar substrates are the leading contenders for TCE control at present. It can be tailored to provide a selected TCE by varying the copper-to-Invar ratio. Figure 20 shows the construction of a typical multilayer substrate employing two cores providing the power and ground planes. Plated-through holes provide an integral board-to-board interconnection. The low TCE of the core dominates the TCE of the overall substrate, making it possible to mount LCCCs with confidence.

Because the TCE of copper is high, and that of Invar is low, the overall TCE of the substrate can be adjusted by varying the thickness of the copper layers. Figure 21 plots the TCE range of the copper-clad Invar as a function of copper thickness, and shows the TCE range of each of several other materials to which the clad material can be matched. For example, if the TCE of Alumina is to be matched, then the core should have about 46% thickness of copper. When this material is used as a thermal mounting plane, it also acts as a heatsink.

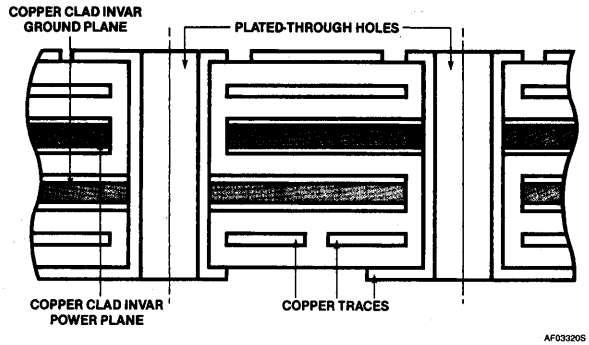


Figure 20. Section Through a Typical Multilayer Substrate Incorporating Copper-clad Invar Ground and Power Planes, Interconnected Via Plated-though Holes.

NOTE: Data provided by N.V. Philips

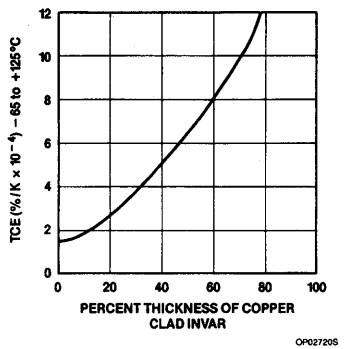


Figure 21. The TCE Range of Copper-clad Invar as a Function of Copper Thickness.

NOTE: Data provided by N.V. Philips

Thermal Considerations For Surface Mounted Devices

Table 1. Substrate Material Properties

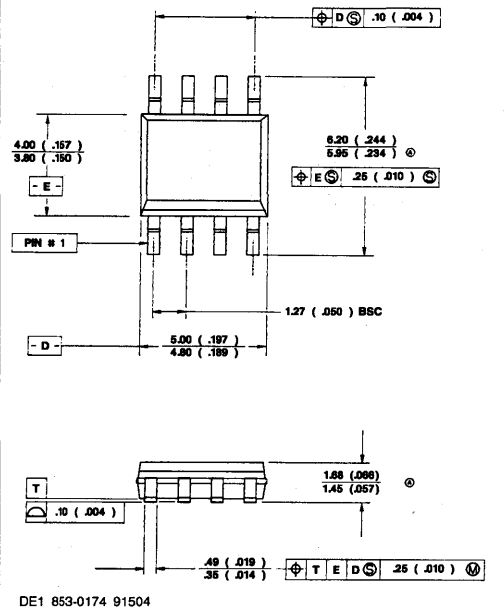
SUBSTRATE MATERIAL	TCE (10^{-6}/K)	THERMAL CONDUCTIVITY (W/M^{3}K)
Glass–epoxy (FR–4)	13 – 17	0.15
Glass polyimide	12 – 16	0.35
Polyimide Kevlar	4 – 8	0.12
Polyimide quartz	6 – 12	TBD
Copper–clad Invar	6.4 (typical	165 (lateral) 16 (transverse)
Alumina	5 – 7	21
Compliant layer Substrate	See Notes	0.15 – 0.3

NOTES:
Compliant layer conforms to TCE of the LCCC and to base substrate material
Data provided by N.V. Philips
KEVLAR® is a registered trademark of DU PONT.
INVAR® is a registered trademark of TEXAS INSTRUMENTS.

CONCLUSION

Thermal management remains a major concern of producers and users of ICs. The advent of SMD technology has made a thorough understanding of the thermal characteristics of both the devices and the systems they are used in mandatory. The SMD package, being smaller, does have a higher θ_{JA} than its standard DIP counterpart — even with Copper Lead Frames. That is the major trade–off one accepts for package miniaturization. However, consideration of all the variables affecting IC junction temperatures will allow the user to take maximum advantage of the benefits derived from use of this technology.

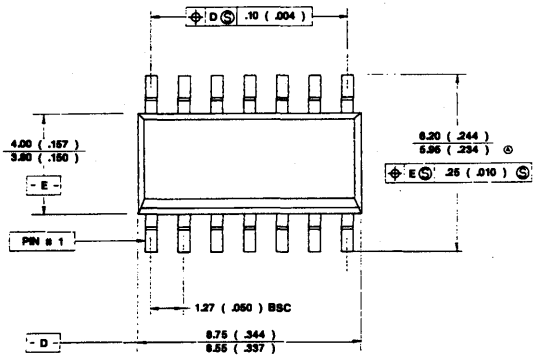
8–PIN PLASTIC SMALL OUTLINE (SO)

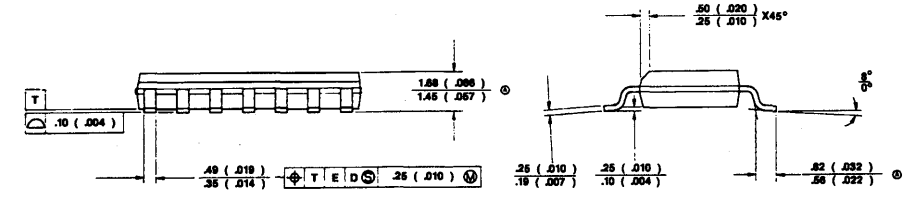


NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

Thermal Considerations for Surface Mounted Devices

14–PIN PLASTIC SMALL OUTLINE (SO)



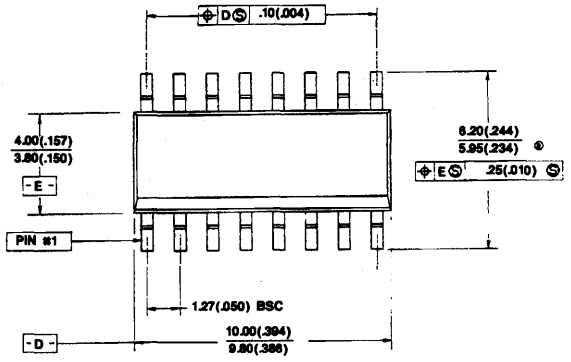


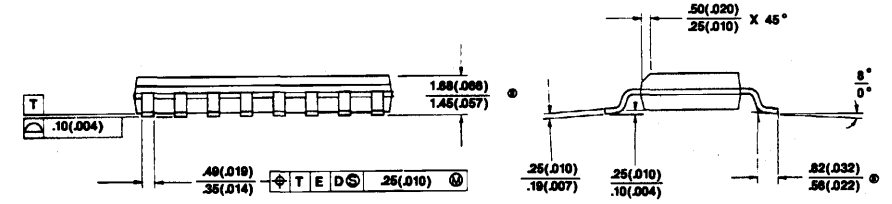
DH1 853-0175 91504

PO02270S

NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

16–PIN PLASTIC SMALL OUTLINE (SO)





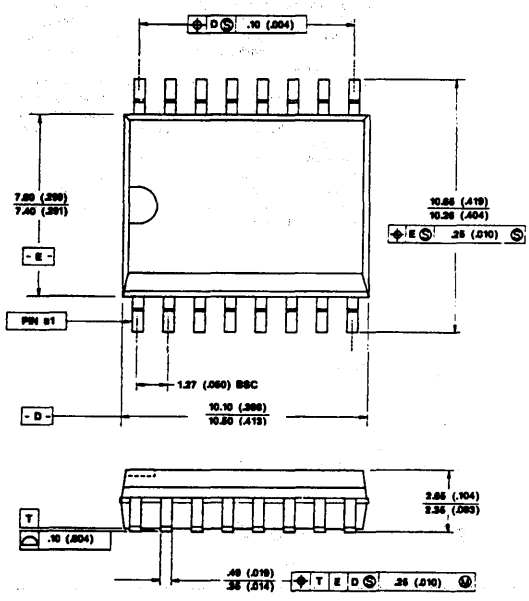
DJ1 853-0005 91504

PO01830S

NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AC for standard small outline (SO) package, 16 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "T", "D" and "E" are reference Datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15 mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix "D" after the product number.

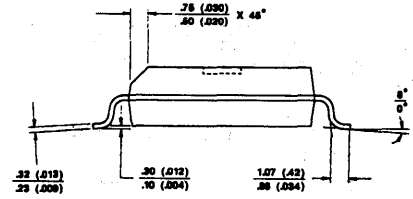
Thermal Considerations For Surface Mounted Devices

16–PIN PLASTIC SMALL OUTLINE (SOL)



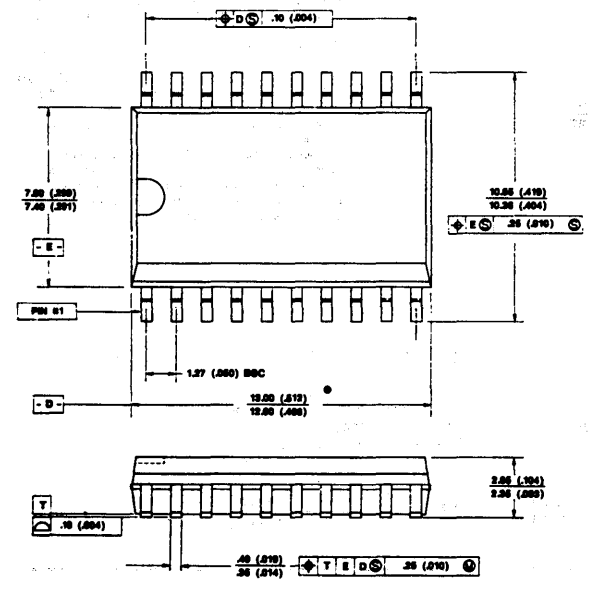
DJ2 853-0171 81218

NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.



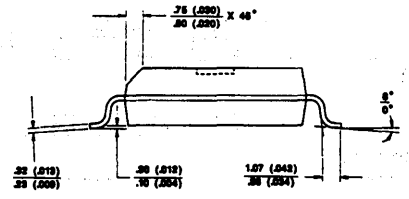
PO02290S

20–PIN PLASTIC SMALL OUTLINE (SOL)



DL2 853-0172 82948

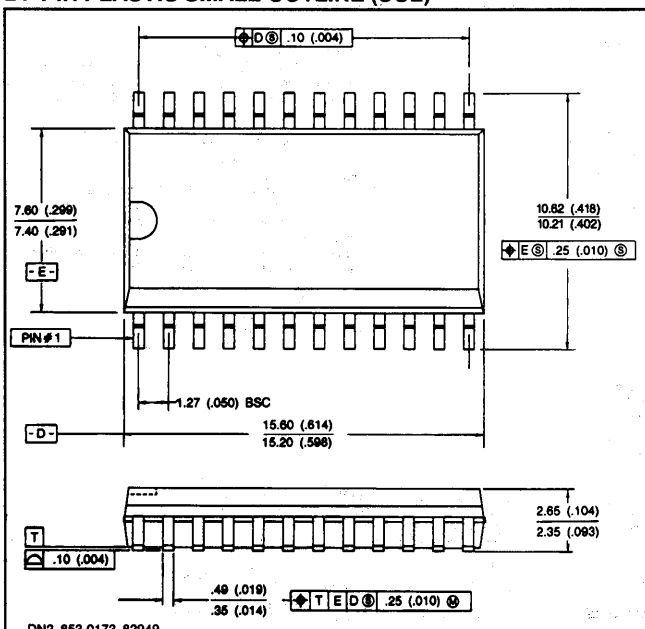
NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

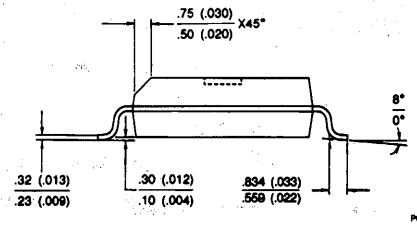


PO02360S

Thermal Considerations For Surface Mounted Devices

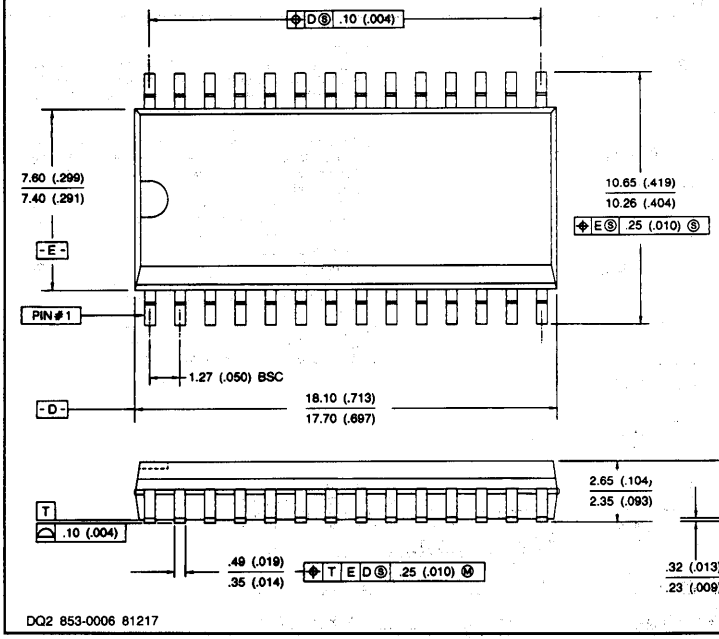
24–PIN PLASTIC SMALL OUTLINE (SOL)

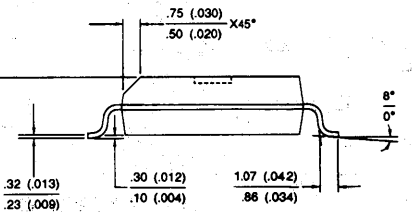




NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

28–PIN PLASTIC SMALL OUTLINE (SOL)

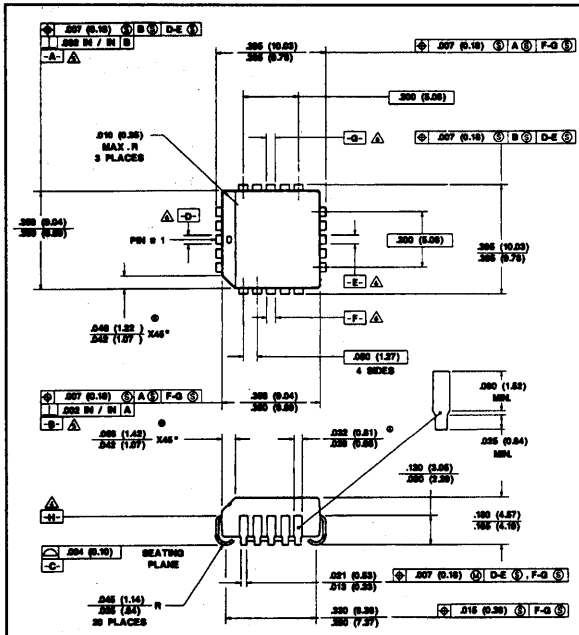




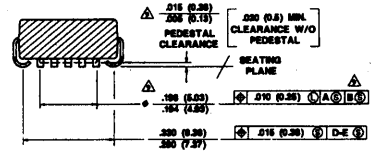
NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AE for standard small outline (SO) package, 28 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

Thermal Considerations For Surface Mounted Devices

20–PIN PLASTIC LEADED CHIP CARRIER



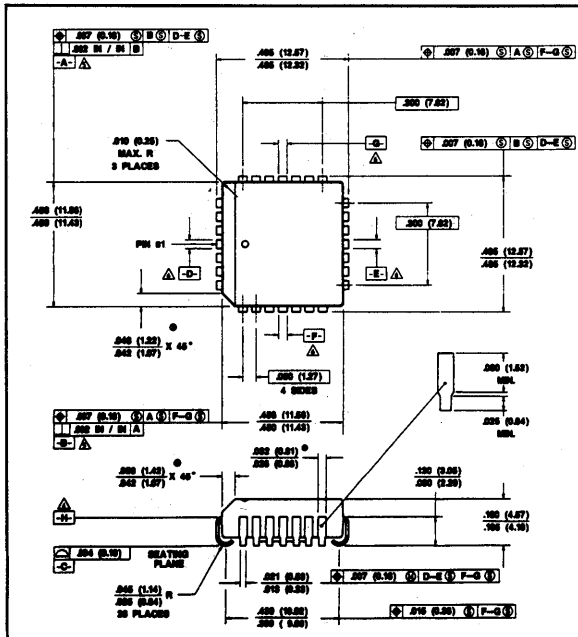
AL1 853-0400 93885



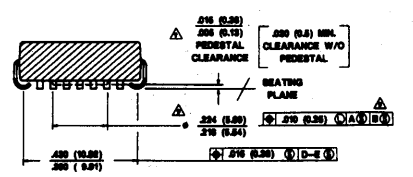
PO02330S

NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AA for plastic leaded chip carrier 20 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead. Where lead exists plastic body.
5. Location to datum "A" and "B" to be determined at plane "H".These datums do not include mold flash. Mold flash protrusion shall not exceed .006" (0.15mm) on any side.
6. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
7. Pin numbers continue counterclockwise to pin #20 (top view).
8. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.
9. Applicable to packages with pedestal only.

28–PIN PLASTIC LEADED CHIP CARRIER



AQ1 853-0401 93885

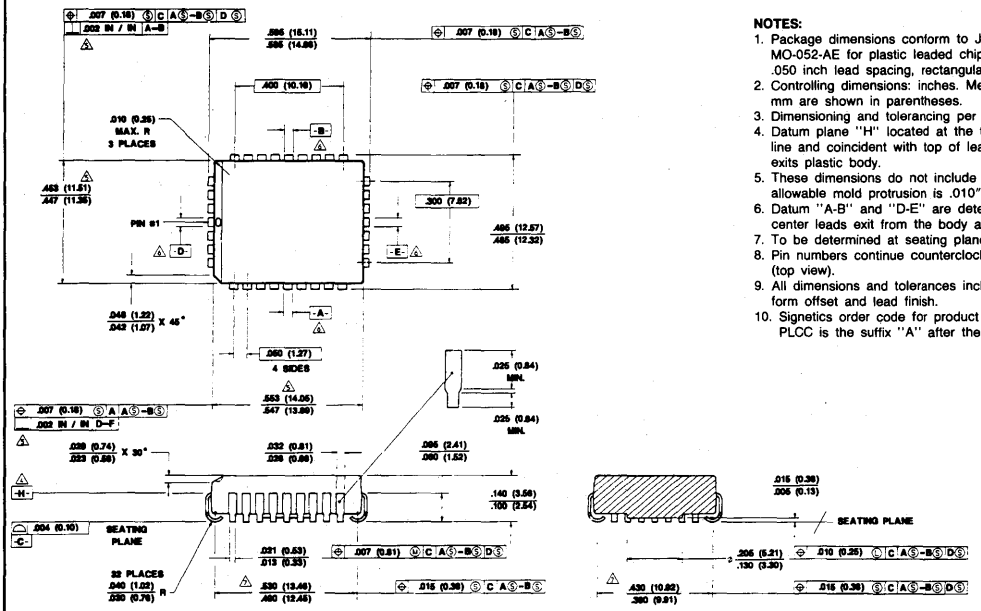


PO02200S

NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AB for plastic leaded chip carrier 28 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead. Where lead exits plastic body.
5. Location to datum "A" and "B" to be determined at plane "H". These Datums do not include mold flash. Mold flash protrusion shall not exceed .006" (0.15 mm) on any side.
6. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
7. Pin numbers continue counterclockwise to pin #28 (top view).
8. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.
9. Applicable to packages with pedestal only.

Thermal Considerations For Surface Mounted Devices

32–PIN PLASTIC LEADED CHIP CARRIER



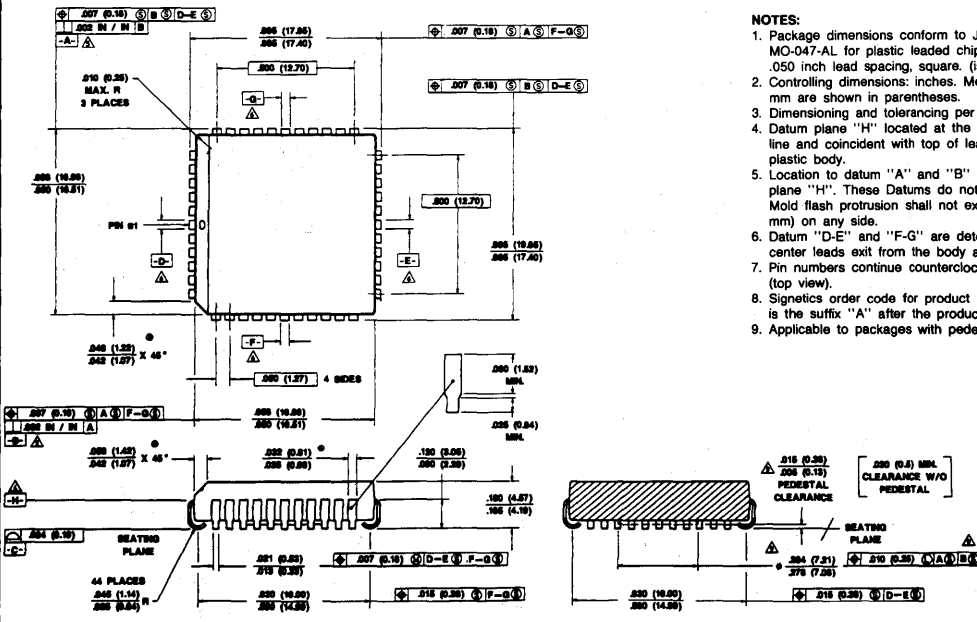
AR2 853-0402 94665

PO02210S

NOTES:

1. Package dimensions conform to JEDEC specification MO-052-AE for plastic leaded chip carrier 32 leads, .050 inch lead spacing, rectangular. (issue A, 8/1/85).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead, where leads exits plastic body.
5. These dimensions do not include mold protrusion. allowable mold protrusion is .010" (.254 mm).
6. Datum "A-B" and "D-E" are determined where these center leads exit from the body at plane "H".
7. To be determined at seating plane "C".
8. Pin numbers continue counterclockwise to pin #32 (top view).
9. All dimensions and tolerances include lead trim and form offset and lead finish.
10. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.

44–PIN PLASTIC LEADED CHIP CARRIER



AX1 853-0403 93885

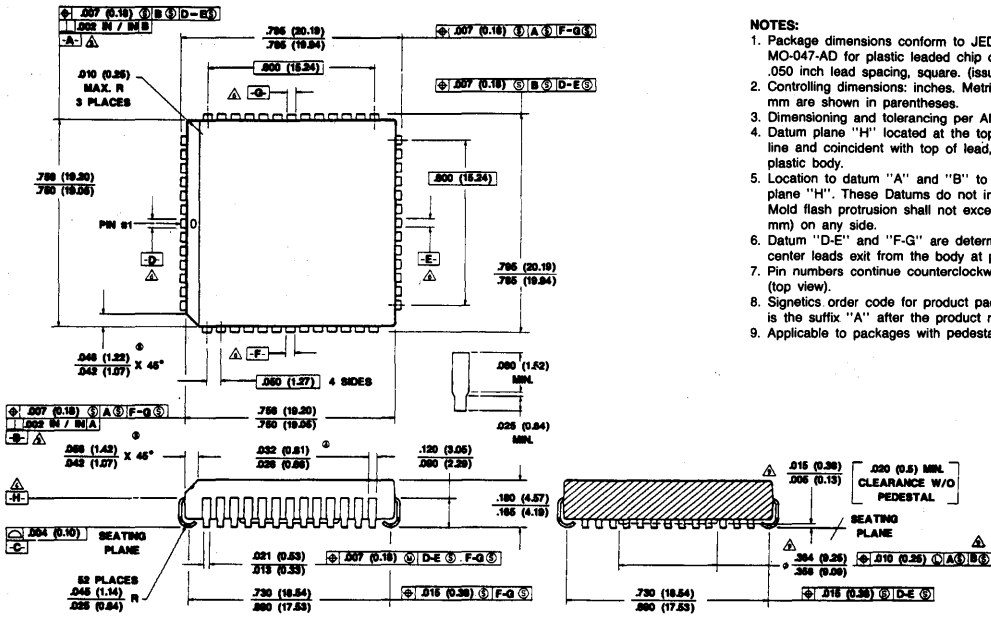
PO02220S

NOTES:

1. Package dimensions conform to JEDEC specification MO-047-AL for plastic leaded chip carrier 44 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead, where lead exits plastic body.
5. Location to datum "A" and "B" to be determined at plane "H". These Datums do not include mold flash. Mold flash protrusion shall not exceed .006" (0.15 mm) on any side.
6. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
7. Pin numbers continue counterclockwise to pin #44 (top view).
8. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.
9. Applicable to packages with pedestal only.

Thermal Considerations For Surface Mounted Devices

52–PIN PLASTIC LEADED CHIP CARRIER

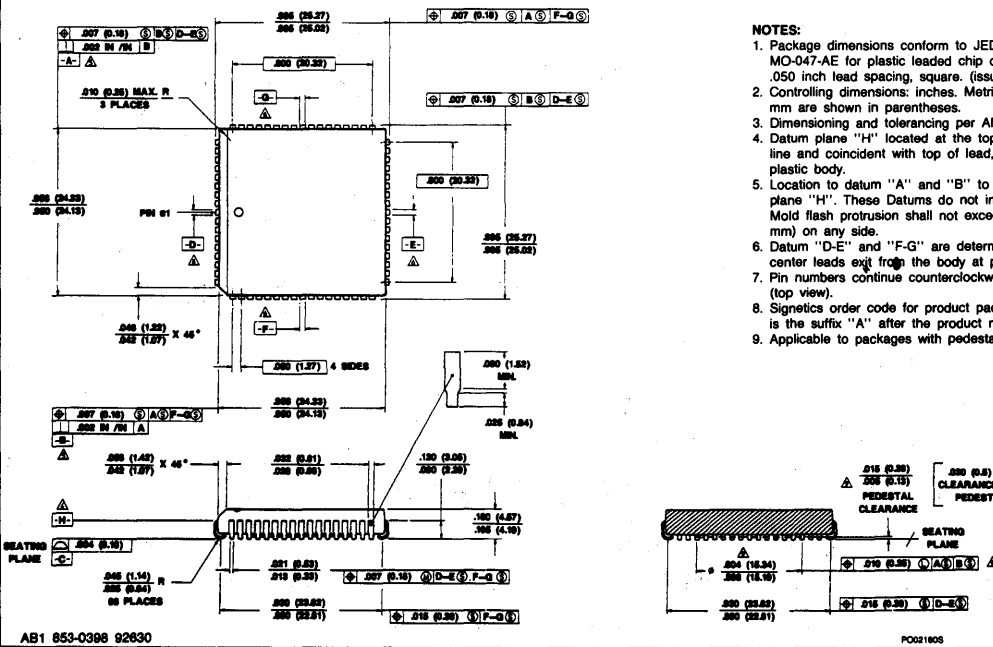


AA1 853-0397 93885

PO02230S

NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AD for plastic leaded chip carrier 52 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead, where lead exits plastic body.
5. Location to datum "A" and "B" to be determined at plane "H". These Datums do not include mold flash. Mold flash protrusion shall not exceed .006" (0.15 mm) on any side.
6. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
7. Pin numbers continue counterclockwise to pin #52 (top view).
8. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.
9. Applicable to packages with pedestal only.

68–PIN PLASTIC LEADED CHIP CARRIER



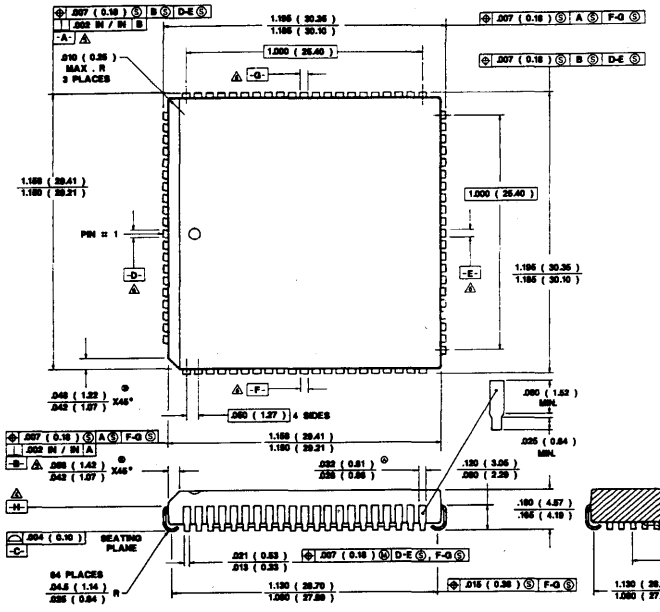
AB1 853-0398 92630

PO02180S

NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AE for plastic leaded chip carrier 68 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead, where lead exits plastic body.
5. Location to datum "A" and "B" to be determined at plane "H". These Datums do not include mold flash. Mold flash protrusion shall not exceed .006" (0.15 mm) on any side.
6. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
7. Pin numbers continue counterclockwise to pin #68 (top view).
8. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.
9. Applicable to packages with pedestal only.

Thermal Considerations For Surface Mounted Devices

84–PIN PLASTIC LEADED CHIP CARRIER (PLCC)



AC1 853-0399 93885

P002310S

NOTES:

1. Package dimensions conform to JEDEC specification MO-047-AF for plastic leaded chip carrier 84 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead, where lead exits plastic body.
5. Location to datum "A" and "B" to be determined at plane "H". These Datums do not include mold flash. Mold flash protrusion shall not exceed .006" (0.15 mm) on any side.
6. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
7. Pin numbers continue counterclockwise to pin #84 (top view).
8. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.
9. Applicable to packages with pedestal only.

Signetics

Section 8
Surface Mounted ICs

FAST Products

Signetics

Surface Mounted ICs

FAST Products

INTRODUCTION

Economic survival is driving the electronics industry to use cheaper, faster, more reliable and more dense systems and components. Assembly technologies, such as SMD (Surface Mounted Device) technology, developed and used in hybrids and for military electronics for over two decades, is being adapted to commercial electronics as part of this evolution. With SMD technology, components are soldered directly to a metalized footprint on the surface of the board or substrate rather than being inserted through holes drilled in the board and then soldered. Because of this evolution, package styles specially designed to facilitate surface mounting are now in high demand.

The reasons for the change to SMD technology vary from one customer to another; but the primary motivator is higher profits through lower manufacturing and material costs, or an improved product, or both.

Improved Electrical Performance

Because SMD packages are much smaller than their DIP counterparts, they have much less capacitance and inductance, and provide improved AC performance, especially in high-speed environments. They help to minimize problems associated with ground bounce and multiple output switching found with standard DIP packages. The SO package is especially suitable for high-speed families such as FAST and High-Speed CMOS where package inductance can induce or compound problems not normally found in slower technologies.

Ease Of Automation

SMD pick-and-place machines offer higher yields, faster cycle rates (3 – 10x faster), and much higher throughput volumes than automatic insertion machines for DIP packages.

Greatly Increased Densities

Greatly increased densities can be achieved through surface mounting. The packages themselves are much smaller (as much as 70%) and can be placed much closer together. Furthermore, both sides of the board can be used with SMDs.

Reduced Board Costs

The number of layers, total size of the board, and the number of plated through holes can be reduced, thus lowering the total cost of the board (many companies claim savings of 30 to 50%).

Easier Board Rework

In those instances where rework is necessary, it is much faster and cheaper with SMDs.

Improved Reliability

Not only are the components proving to be at least as reliable as their DIP counterparts but, surface mounted assemblies show fewer failures in stress tests than equivalent through hole assemblies.

Lower Shipping, Storage And Handling Costs

SMD components are up to 70% smaller and weigh up to 90% less than DIPs (up to 95% savings in storage area for Tape & Reel SMD components vs DIPs and up to 90% savings in component weight). Surface mount assemblies offer additional savings in both weight and space, both of which can be linked to increased profits.

SMD packages for integrated circuits fall into two categories: Swiss Outline, also known as Small Outline (SO), and the Plastic Leaded Chip Carrier (PLCC).

SO PACKAGE

The SO package was developed by N.V. Philips Corp, originally for the Swiss watch industry. In the mid 1970s Signetics introduced linear ICs in SO packages to the US market (hybrid and telecommunications). As demand grew, other technologies such as FAST, Low Power Schottky, Schottky, TTL, CMOS, High-Speed CMOS (HC and HCT), ECL, ROMs, RAMs, PROMs, were made available in SO packages.

The SO is a dual-in-line plastic package with leads spaced 0.050″ apart and bent down and out in a Gull-Wing format. It comes in two widths: 0.150″ SO, and 0.300″ SOL (SO-Large) depending on the pin count.

As ICs became more complex and the number of pins grew, the standard dual-in-line packages grew longer and wider, presenting new electrical and mechanical problems. Some of these were resolved with the introduction of the ceramic leadless chip carrier (LCC). These were square, ceramic packages without leads which can be socketed or soldered directly to a substrate if the thermal coefficient of expansion of the chip carrier and the substrate are to be matched.

In 1980, the Plastic Leaded Chip Carrier (PLCC) was introduced as a cheaper alternative to the LCC. However, this was at the same time that SMD was winning acceptance in commercial electronics and the PLCC was seen as an ideal SMD package for the higher pin count devices (those with more than 28 leads). The PLCC is a square, plastic package with leads on four sides, spaced down and under in a J-Bend configuration. It is available in the higher pin counts: 20, 28, 44, 52, 68, 84 with even higher pin counts under development.

The smallest square PLCC is the 20 pin package. There are many reasons for this; the primary one is that below 20 pins, the package would be as thick as it is square,

Table 1

PIN COUNT	SO	SOL	PLCC
8	x		
14	x		
16	x	x	
18		x	x (rectangular)
20		x	x
24		x	
28		x	x
44			x
52			x
68			x
84			x

Surface Mounted ICs

resulting in a cube-like package which would be very difficult to handle in an automated environment.

Logic and linear devices are available in SO while the more complex parts such as microprocessors, microcontrollers, complex peripherals, large memory devices, and other higher pin count integrated circuits will be found in the PLCC.

ASSEMBLY

The assembly of these SMD packages is virtually the same as for the older DIP packages using the same materials and most of the same equipment and assembly technologies.

The only differences in the process are the smaller lead frames, different lead bends (gull-wing for SO and J-Bend for the PLCC), and closer spacing resulting in a much smaller package for the same basic die.

RELIABILITY

Reliability studies of SMD components, conducted not only by Signetics and Philips, but by many of our competitors and customers, have revealed that these packages are at least as reliable as the standard plastic DIP packages that have been used over the past 20 years. In several cases, test results of the SMD packages have been better than their DIP counterparts.

STANDARDIZATION

The SO package is an industry standard format. In June 1985, the JEDEC (Joint Electronics Engineering Council) of the EIA (Electronics Industries Association) issued a Solid State Product Outlines Standard for each of the SO formats: MS-012 AA-AC for the 0.150″ body width SO and Ms-013 AA-AE for the 0.300″ body width SOL. In addition to the JEDEC Standard, de facto standardization has been achieved in the industry in that most of the major US and European IC manufacturers (more than 15 companies currently) use this standard.

The PLCC is also a standardized format, with a JEDEC Registered Outline #MO-047 AA-AH. It also is multiple sourced with over 10 US IC manufacturers using this standard.

Points worth noting: All SO And SOL packages have 0.050″ lead spacing and a Gull-Wing lead bend, while all PLCC packages have the same lead spacing and a J-Bend lead bend.

TAPE AND REEL

One revolutionary phenomenon in SMD is the development of Tape and Reel for the IC packages. Philips and several other companies making automatic placement equipment recognized the need for a feed system which allows for positive indexing large volumes of components at high-speed in order to get maximum efficiency out of the new pick-and-place machines. Tubes are limited to a relatively small number of parts (dictated by tube length) and depend on gravity to feed components to the placement head. After several proposed tape formats, Philips, Signetics, many of the component and placement equipment manufacturers, and board manufacturers convened under the auspices of EIA (Electronic Industries Association) and agreed on an industry standard specification for Tape and Reel for both SO and PLCC packages. The proposed EIA specification RS 481A is being used by Signetics and Philips, both of whom have shipped components on Tape and Reel since late 1984.

Surface Mounted ICs

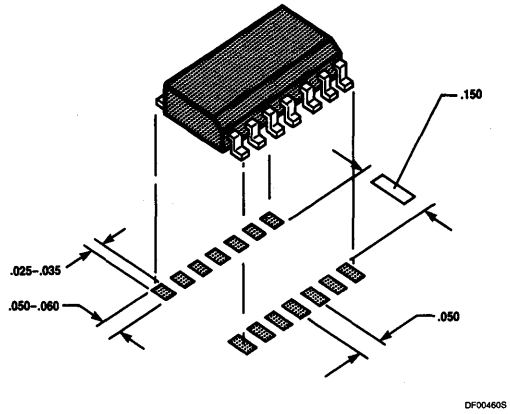
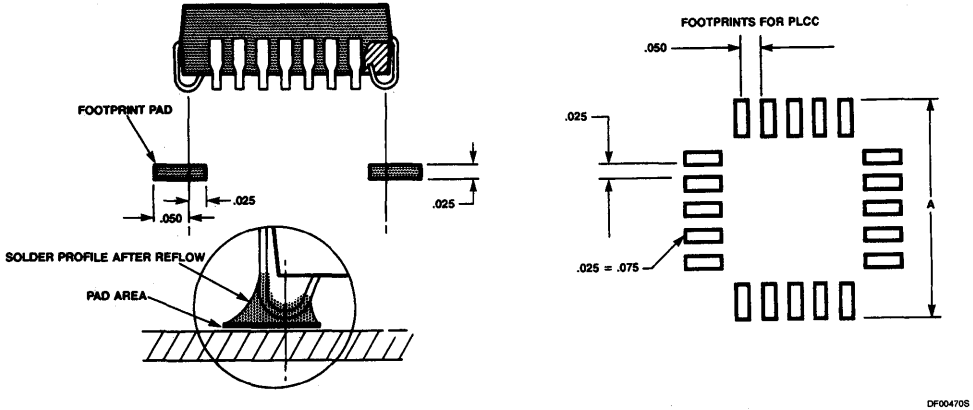


Figure 1. Manufacturers' Recommended Footprint



PINS	A
20	.425
28	.525
44	.725
52	.825
68	1.025

Figure 2. Footprint Design for The PLCC-IC

8

Signetics

Section 9
Package Outlines

FAST Products

INDEX

Package Outlines

Logic Products

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

1. Dimensions are shown in Metric units (Millimeters) and English units (Inches).
2. Lead material: Copper Alloy, solder (63%Sn/37%Pb) dipped.
3. Body material: Plastic (Epoxy)
4. Thermal resistance values are determined by temperature sensitive parameter (TSP) method. This method uses the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power application. The substrate diode of a Bipolar technology device is generally the diode used in these tests. Die size and test environment have significant effects on thermal resistance values.

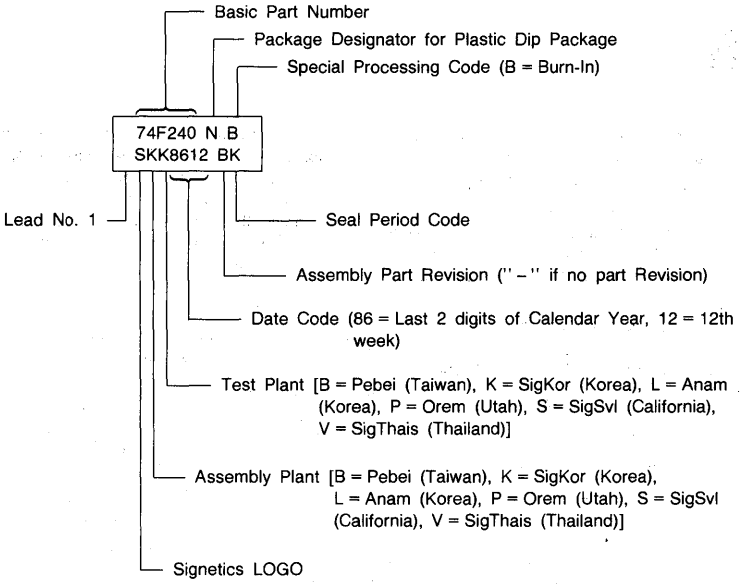
PLASTIC PACKAGES OUTLINES

Package Type	Number of Leads	Package Feature	Package Ordering Code	Package Outline Code	Thermal Resistance θ_{JA}/θ_{JC} (°C/W)	Die Size (square mils)	Test Conditions	
							Test Ambient	Test Fixture
SO[1] (Copper Leadframe)	14 pin (SO-14)	3.9mm (0.15″) Body width	D	DH1	124/37	2,500	Still air at room temperature	Device soldered to Philips glass epoxy test board (1.12″ × 0.75″ × 0.059″) with 0.008 – 0.009″ stand-off. Accuracy: ± 15%
	16 pin (SO-16)		D	DJ1	113/36			
	16 pin (SOL-16)	7.5mm (0.30″) Body width	D	DJ2	98/30	5,000		Device soldered to Philips glass epoxy test board (1.58″ × 0.75″ × 0.059″) with 0.008 – 0.009″ stand-off. Accuracy: ± 15%
	20 pin (SOL-20)		D	DL2	90/28			
	24 pin (SOL-24)		D	DN2	76/26			
	28 pin (SOL-28)		D	DQ2	70/24	10,000		
PLCC[2] (Copper Leadframe)	44 pin (PLCC-44)	0.650″ Square body	A	AX1	50/20	15,000	Still air at room temperature	Device soldered to Philips glass epoxy test board (2.24″ × 2.24″ × 0.062″) with 0.008 – 0.009″ stand-off. Accuracy: ± 15%
DIP[3] (Copper Leadframe)	14 pin (DIP-14)	0.300″ Lead row centers	N	NH1	89/44	2,500	Still air at room temperature	Device in Textool ZIF socket with 0.040″, stand-off. Accuracy: ± 15%
	16 pin (DIP-16)		N	NJ1	86/43			
	20 pin (DIP-20)		N	NL1	74/32	5,000		Device in Textool ZIF socket with 0.040″, stand-off. Accuracy: ± 15%
	24 pin SLIM DIP (DIP-24)		N	NN1	65/36			
	24 pin (DIP-24)	0.600″ Lead row centers	N	NN3	59/30			
	28 pin (DIP-28)		N	NQ3	52/27	10,000		
	40 pin (DIP-40)		N	NW3	45/19	15,000		

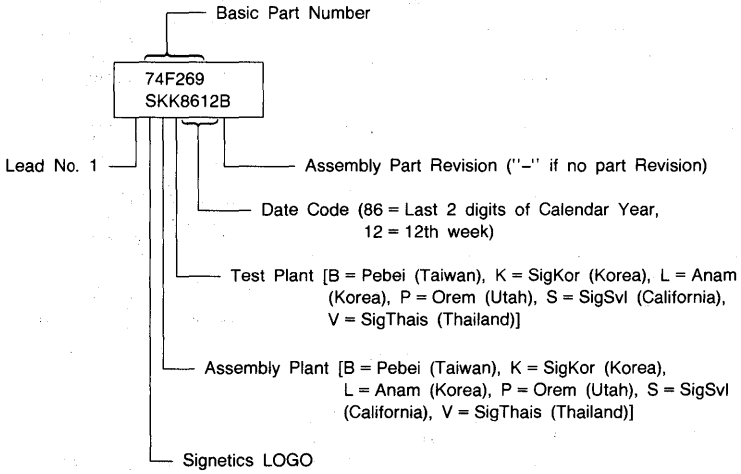
NOTES:
1. SO = **S**mall **O**utline
2. PLCC = **P**lastic **L**eaded **C**hip **C**arrier
3. DIP = **D**ual-**I**n-Line **P**ackage

Package Outlines

4. Package Symbolization for Plastic Dual-In-Line Package (DIP) Top Side

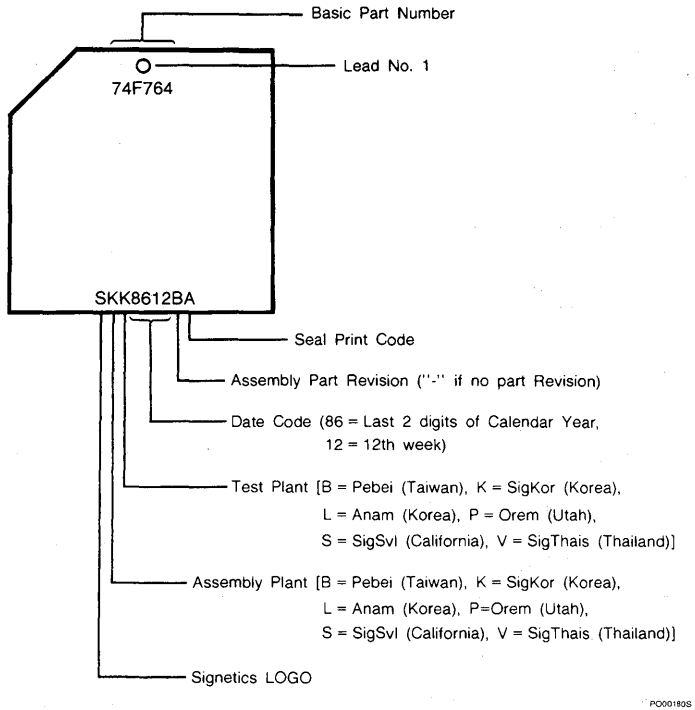


5. Package Symbolization for Plastic Small Outline Package (SO) Top Side



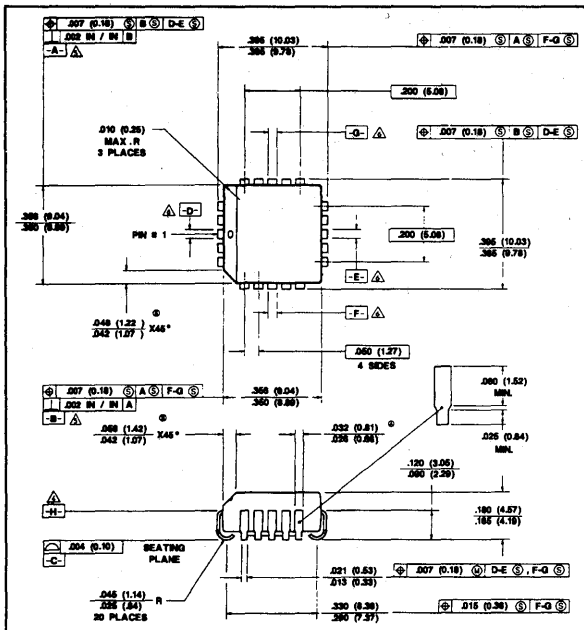
Package Outlines

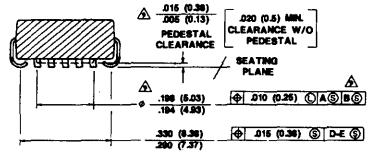
6. Package Symbolization for Plastic Leaded Chip Carrier (PLCC)



Package Outlines

20–PIN PLASTIC LEADED CHIP CARRIER



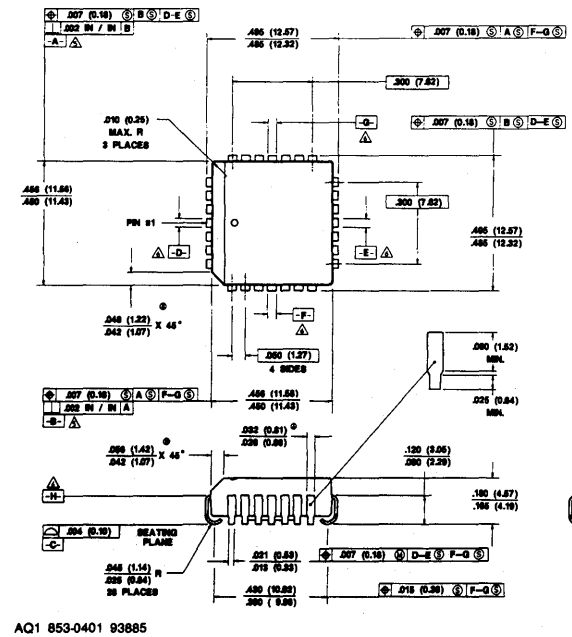


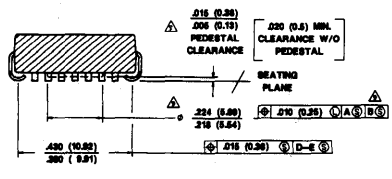
AL1 853-0400 93885

PO02330S

NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AA for plastic leaded chip carrier 20 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead. Where lead exists plastic body.
5. Location to datum "A" and "B" to be determined at plane "H".These datums do not include mold flash. Mold flash protrusion shall not exceed .006" (0.15mm) on any side.
6. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
7. Pin numbers continue counterclockwise to pin #20 (top view).
8. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.
9. Applicable to packages with pedestal only.

28–PIN PLASTIC LEADED CHIP CARRIER





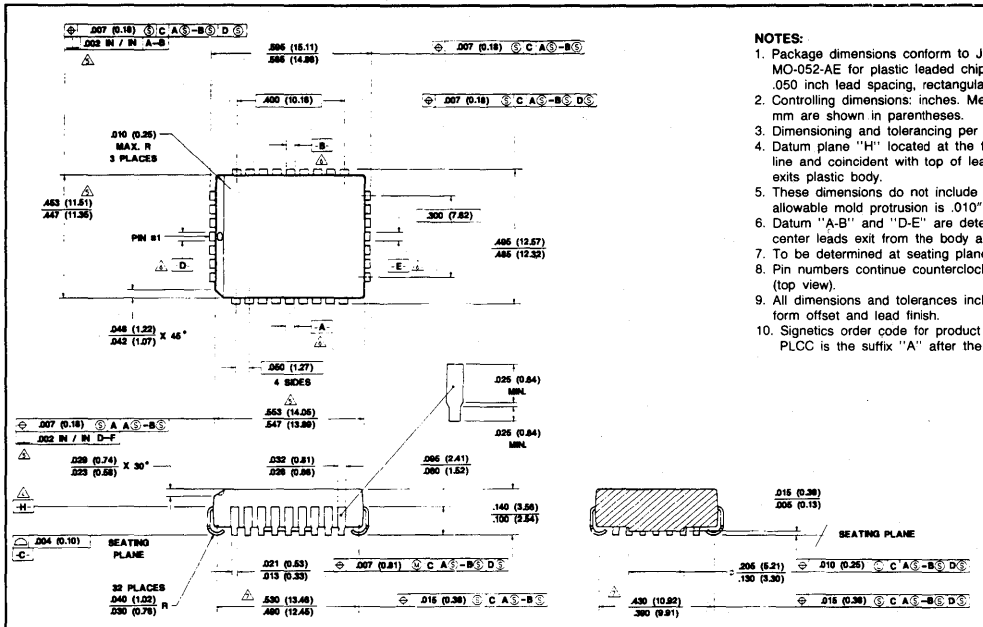
AQ1 853-0401 93885

PO02200S

NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AB for plastic leaded chip carrier 28 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead. Where lead exits plastic body.
5. Location to datum "A" and "B" to be determined at plane "H". These Datums do not include mold flash. Mold flash protrusion shall not exceed .006" (0.15 mm) on any side.
6. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
7. Pin numbers continue counterclockwise to pin #28 (top view).
8. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.
9. Applicable to packages with pedestal only.

Package Outlines

32–PIN PLASTIC LEADED CHIP CARRIER

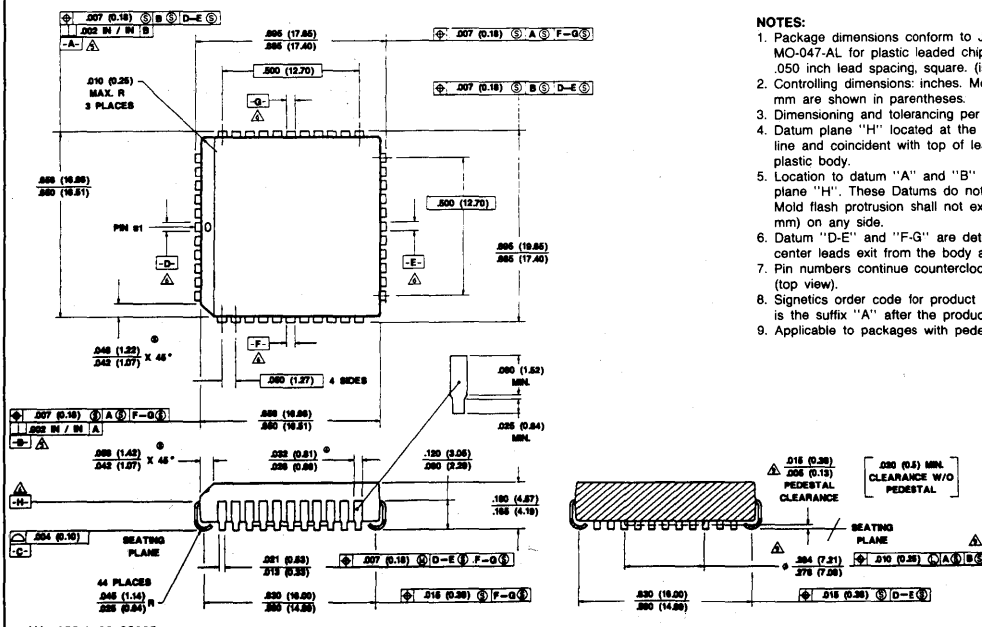


AR2 853-0402 94665

PO02210S

NOTES:
1. Package dimensions conform to JEDEC specification MO-052-AE for plastic leaded chip carrier 32 leads, .050 inch lead spacing, rectangular. (issue A, 8/1/85).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead, where leads exits plastic body.
5. These dimensions do not include mold protrusion. allowable mold protrusion is .010" (.254 mm).
6. Datum "A-B" and "D-E" are determined where these center leads exit from the body at plane "H".
7. To be determined at seating plane "C".
8. Pin numbers continue counterclockwise to pin #32 (top view).
9. All dimensions and tolerances include lead trim and form offset and finish.
10. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.

44–PIN PLASTIC LEADED CHIP CARRIER



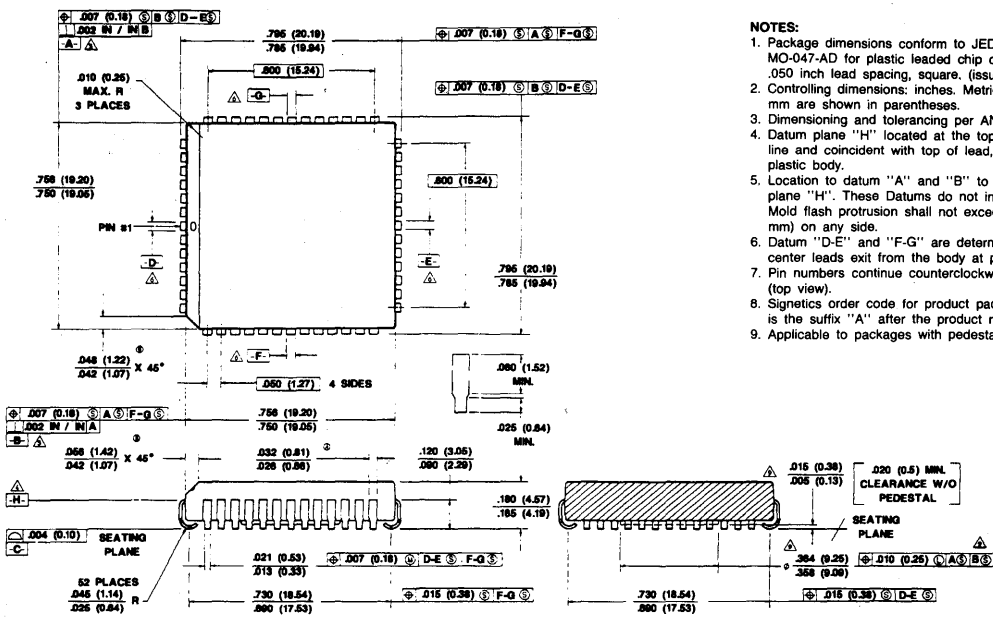
AX1 853-0403 93685

PO02220S

NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AL for plastic leaded chip carrier 44 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead, where lead exits plastic body.
5. Location to datum "A" and "B" to be determined at plane "H". These Datums do not include mold flash. Mold flash protrusion shall not exceed .006" (0.15 mm) on any side.
6. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
7. Pin numbers continue counterclockwise to pin #44 (top view).
8. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.
9. Applicable to packages with pedestal only.

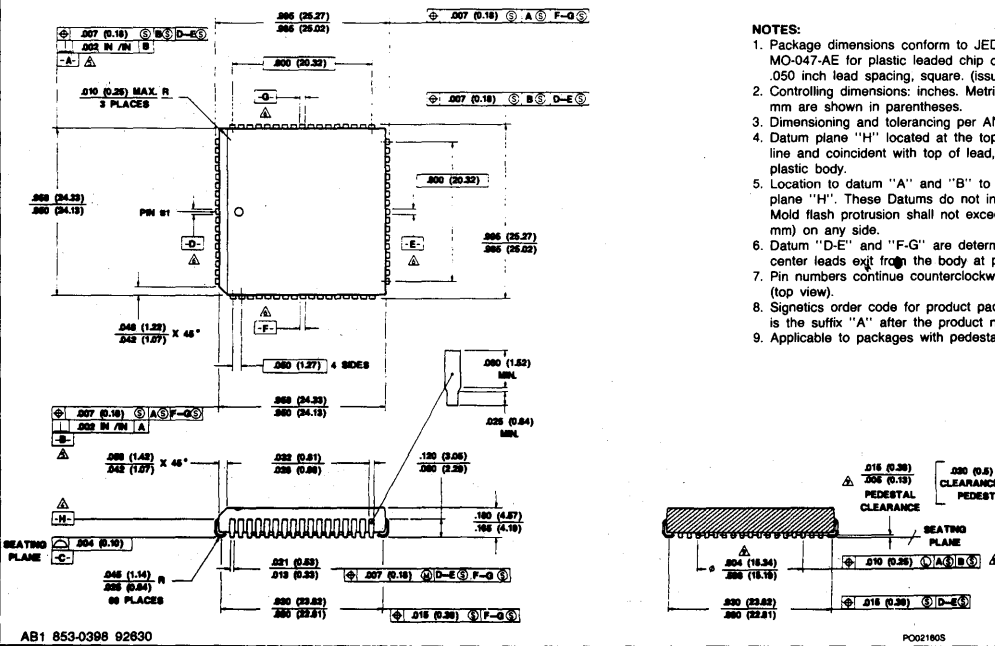
Package Outlines

52–PIN PLASTIC LEADED CHIP CARRIER



NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AD for plastic leaded chip carrier 52 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead, where lead exits plastic body.
5. Location to datum "A" and "B" to be determined at plane "H". These Datums do not include mold flash. Mold flash protrusion shall not exceed .006" (0.15 mm) on any side.
6. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
7. Pin numbers continue counterclockwise to pin #52 (top view).
8. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.
9. Applicable to packages with pedestal only.

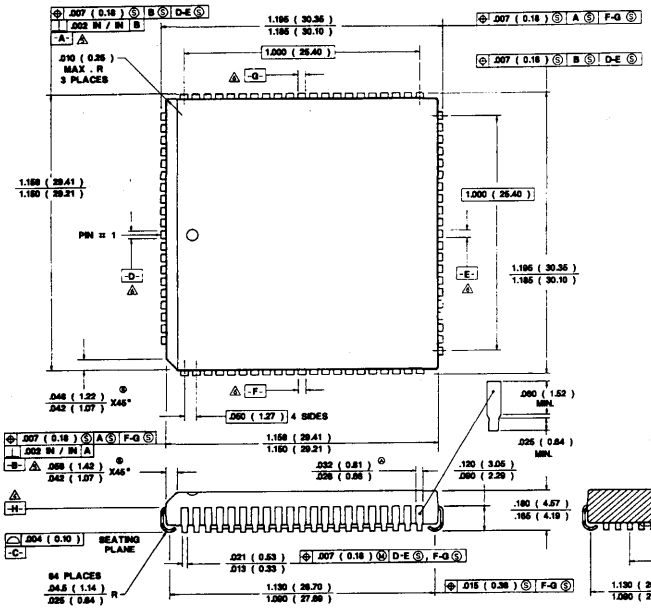
68–PIN PLASTIC LEADED CHIP CARRIER



NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AE for plastic leaded chip carrier 68 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead, where lead exits plastic body.
5. Location to datum "A" and "B" to be determined at plane "H". These Datums do not include mold flash. Mold flash protrusion shall not exceed .006" (0.15 mm) on any side.
6. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
7. Pin numbers continue counterclockwise to pin #68 (top view).
8. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.
9. Applicable to packages with pedestal only.

Package Outlines

84–PIN PLASTIC LEADED CHIP CARRIER (PLCC)



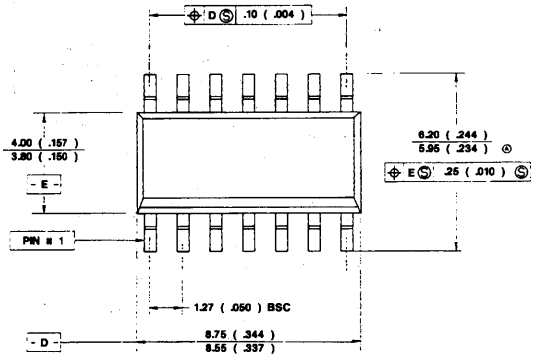
NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AF for plastic leaded chip carrier 84 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead, where lead exits plastic body.
5. Location to datum "A" and "B" to be determined at plane "H". These Datums do not include mold flash. Mold flash protrusion shall not exceed .006" (0.15 mm) on any side.
6. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
7. Pin numbers continue counterclockwise to pin #84 (top view).
8. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.
9. Applicable to packages with pedestal only.

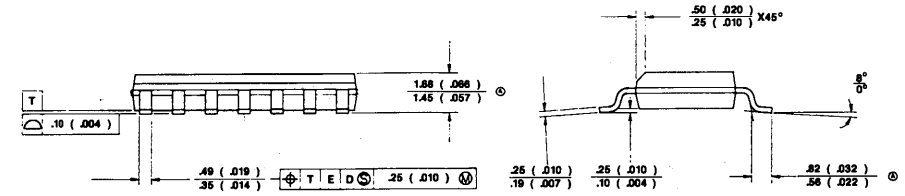
AC1 853-0399 93885

POO2310S

Package Outlines

14–PIN PLASTIC SMALL OUTLINE (SO)



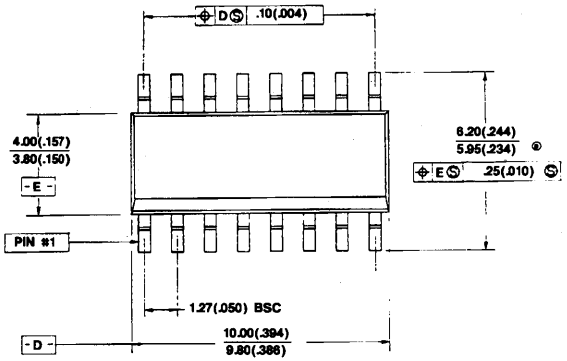


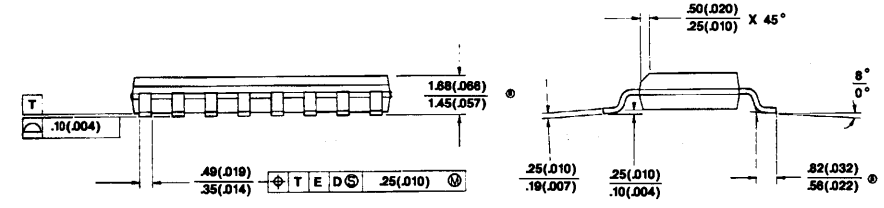
DH1 853-0175 91504

PO02270S

NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AB for standard small outline (SO) package, 14 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

16–PIN PLASTIC SMALL OUTLINE (SO)





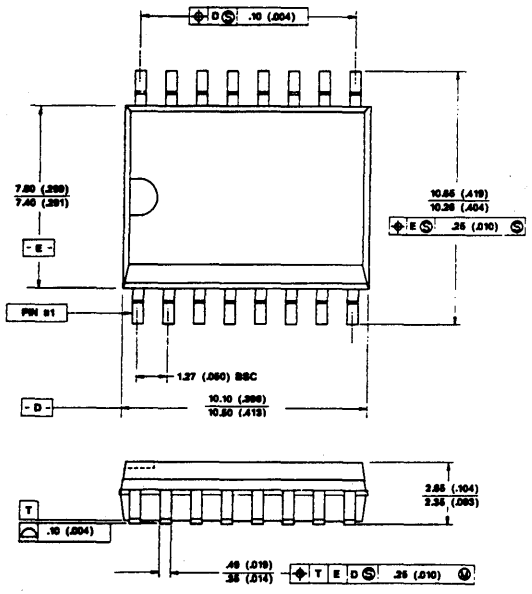
DJ1 853-0005 91504

PO01830S

NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AC for standard small outline (SO) package, 16 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "T", "D" and "E" are reference Datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15 mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix "D" after the product number.

Package Outlines

16–PIN PLASTIC SMALL OUTLINE (SOL)

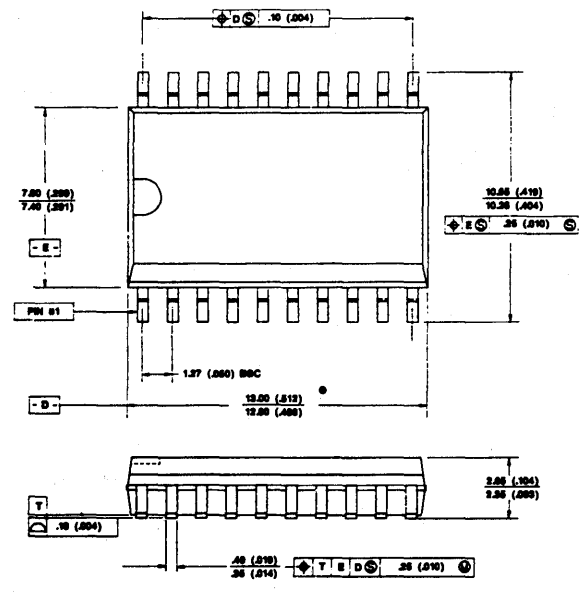


NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

DJ2 853-0171 81218

PO02290S

20–PIN PLASTIC SMALL OUTLINE (SOL)



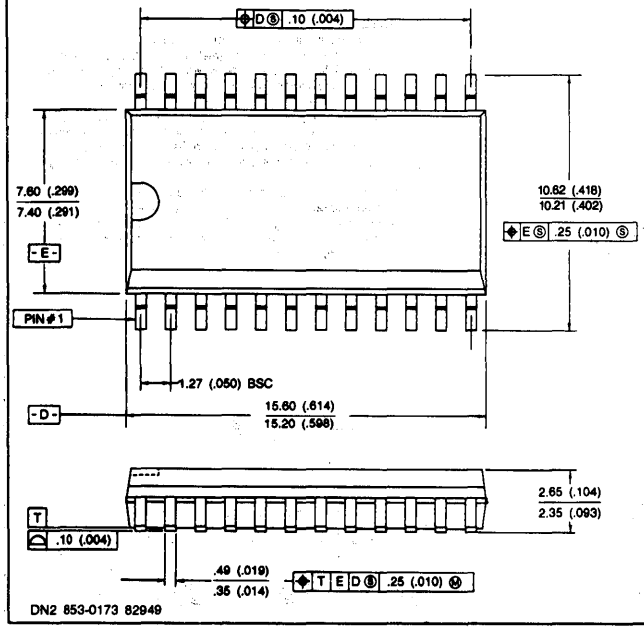
NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

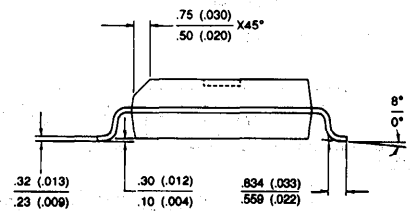
DL2 853-0172 82948

PO02350S

Package Outlines

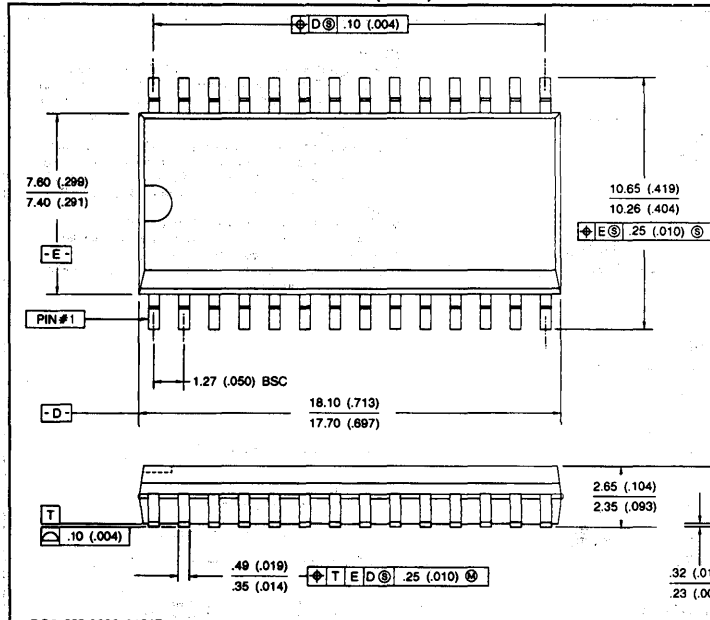
24–PIN PLASTIC SMALL OUTLINE (SOL)

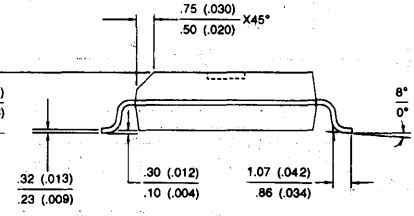




NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

28–PIN PLASTIC SMALL OUTLINE (SOL)

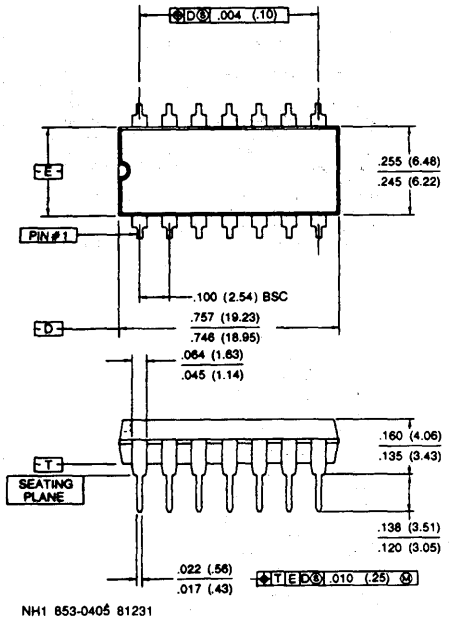


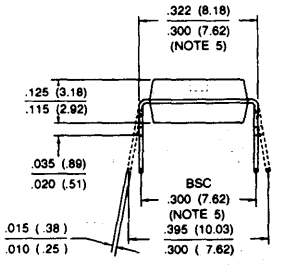


NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AE for standard small outline (SO) package, 28 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

Package Outlines

14–PIN PLASTIC DUAL IN–LINE (PDIP)



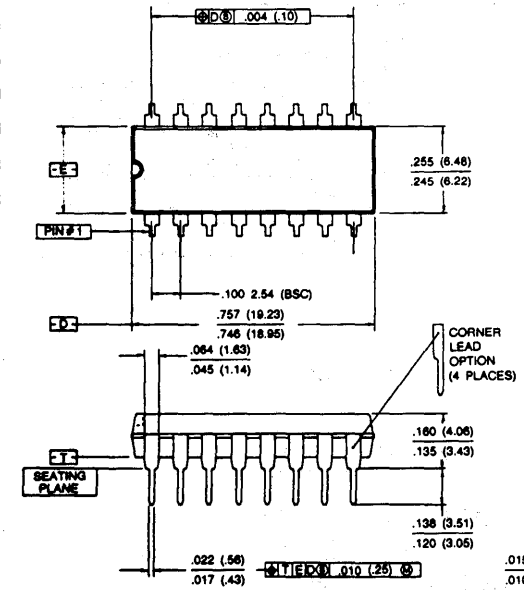


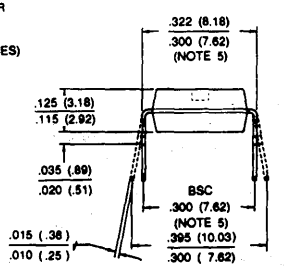
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AC for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 14 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

NH1 853-0405 81231

PO00330S

16–PIN PLASTIC DUAL IN–LINE (PDIP)





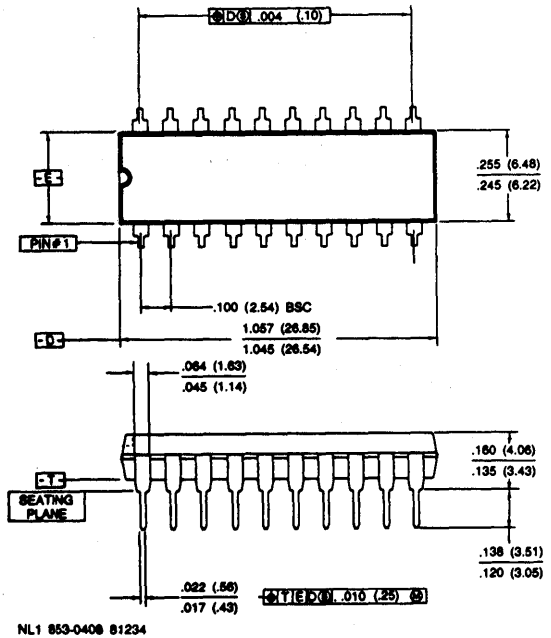
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

NJ1 853-0406 81232

PO00260S

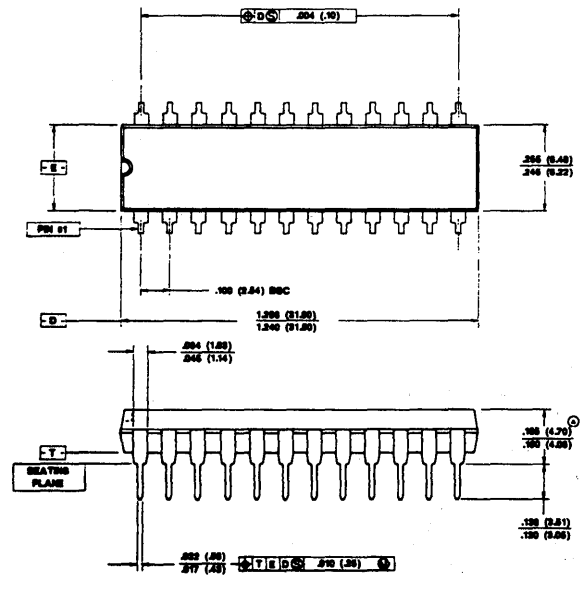
Package Outlines

20–PIN PLASTIC DUAL IN–LINE (PDIP)



NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AE for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 20 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

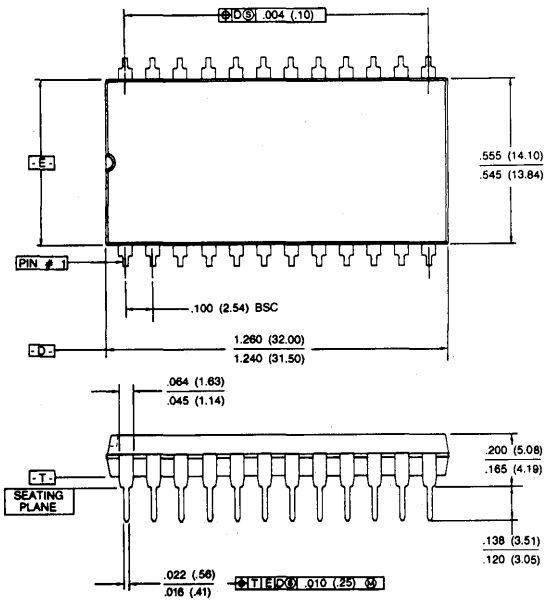
24–PIN PLASTIC DUAL IN–LINE (PDIP)



NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AF for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 24 leads (issue B. 7/85)
3. Dimension and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.

Package Outlines

24–PIN PLASTIC DUAL IN–LINE (PDIP) (600mil–wide)

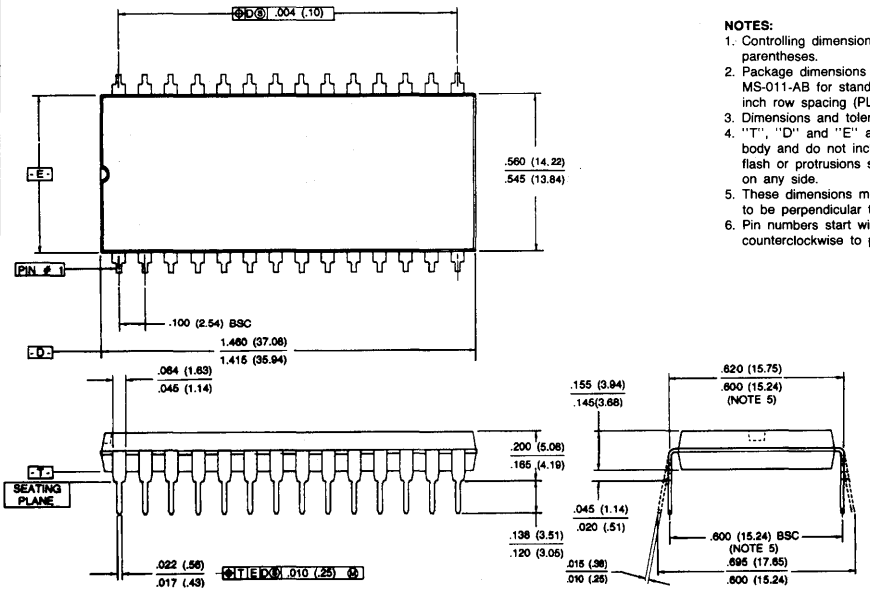


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AA for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 24 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from the top.
7. This package is not processed through standard Signetics process.
   Lead finish: solder plated.
   Lead angle: 90 degree bend.

NN3 853-1202 86270

PO00362S

28–PIN PLASTIC DUAL IN–LINE (600mil–wide)



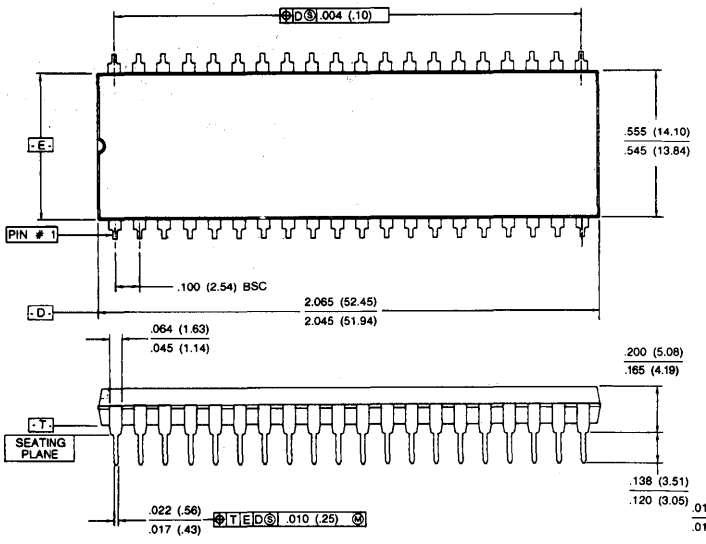
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AB for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 28 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from the top.

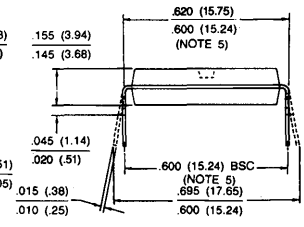
NQ3 853-0413 84099

PO00372S

Package Outlines

40–PIN PLASTIC DUAL IN–LINE (PDIP)





NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-011-AC for standard dual in-line (DIP) package .600 inch row spacing (PLASTIC) 40 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #40 when viewed from the top.

NW3 853-0415 84971

PO00382S

Signetics

FAST Products

Section 10
Sales Offices, Representatives & Distributors

Signetics

a division of North American Philips Corporation

Signetics Company
811 E. Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 408/991-2000

98-2915-400

Signetics
Philips Components

PHILIPS

PHILIPS