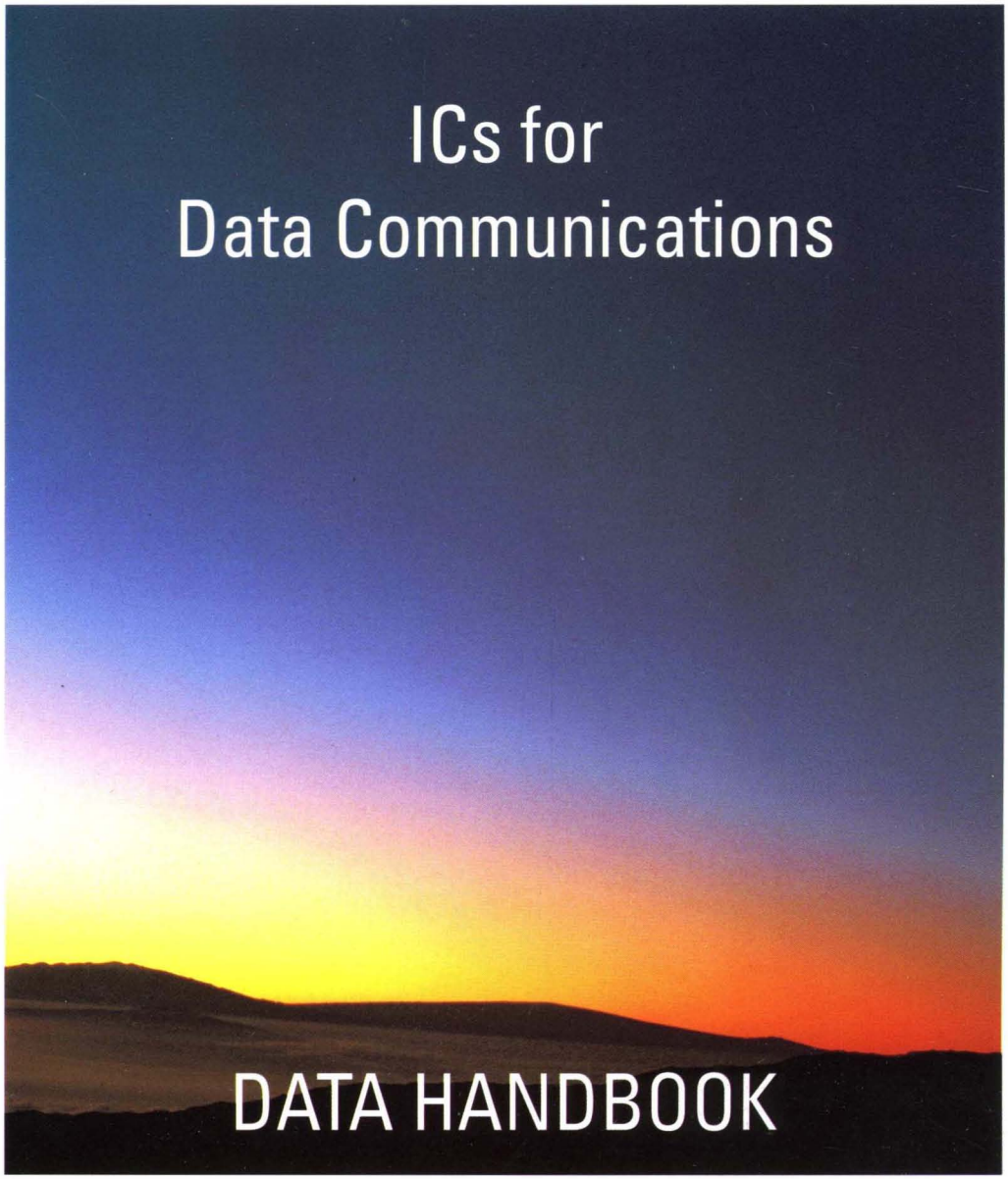
ICs for Data Communications



DATA HANDBOOK

BOOK IC19 1994

Philips Semiconductors

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ICs for Data Communications

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Preface

Data Communications is one of the fastest growing markets in electronics and one in which Philips Semiconductors has had a leadership position for many years. Our industry standard UARTs are complemented with the advanced architecture of the Dual Universal Serial Communications Controller (DUSCC) products and, more recently, by the innovative I/O Processor family. Taking advantage of an advanced CMOS technology, this entire product line represents the most comprehensive in the industry and it continues to grow.

In addition to the product focus, Philips Semiconductors continues its committment to the highest levels of quality to insure our customers of cost effective ownership and world class reliability. In addition to the Digital Data Communication product family, Philips Semiconductors offers a very extensive portfolio of semiconductor products, the details of which can be obtained from your local sales office.

Section 1
General information

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Functional Index

ICs for Data Communications

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Alphanumeric Product List

Product Status

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

Ordering information

DATA COMMUNICATIONS CONTROLLERS

Example: S C N X X X X X C 6 N 4 8

SC – Philips Designator

Process/Power Variation
N = N – Channel
C = C – MOS
B = Bipolar

Basic Part Number
See individual data sheets

Temperature
C = 0°C to 70°C (Commercial)
A = –40°C to +80°C (Automotive)
M = –55°C to +125°C (Military)
P = –20°C to +70°C (Philips)

Timing Variation

Spd	Sym	Spd	Sym	Spd	Sym
01	1	21	1	41	1
02	2	22	2	42	2
03	3	23	3	43	3
04	4	24	4	44	4
05	5	25	5	45	5
06	6	26	6	46	6
07	7	27	7	47	7
08	8	28	8	48	8
09	9	29	9	49	9
10	A	30	0	50	0
11	B	31	1	51	1
12	C	32	2	52	2
13	D	33	3	53	3
14	E	34	4	54	4
15	F	35	5	55	5
16	6	36	6	56	6
17	7	37	7	57	7
18	8	38	8	58	8
19	9	39	9		.
20	0	40	0		.

Unless otherwise noted.

Pin count
14, 16, 20, 24, 28, 40, 48, etc.

Package Code
A = Plastic Leaded Chip Carrier (PLCC)
N = Plastic Dual In-Line
F = Ceramic Dual In-Line

FUTUREBUS+ PRODUCTS

Example: FB XXXX BB

Package Code:
A = Plastic Leaded Chip Carrier (PLCC)
BB = Quad Flat Pack (QFP)

Device Number

Designates Futurebus+ Product.
Temperature Range: 0°C to +70°C

LINEAR AND RF PRODUCTS

Example: NE XXXX N

Package Code:
A = Plastic Leaded Chip Carriers (PLCC)
D = Plastic SO
DK = Shrink Small Outline Package (SSOP)
F = Ceramic Dual In-Line
FE = Hermetic Cerdip (8 Lead)
N = Plastic Dual In-Line

Device Number

Device Family and Temperature Range Prefix
AU = -40°C to +125°C
NE = 0 to +70°C
SE = –55°C to +125°C
SA = –40°C to +80°C

Network terms

A

Access method: A software/hardware method of transferring data between host–resident application programs and remote devices. This term is usually used to describe communications software residing in a mainframe computer.

ACK or acknowledge: A character or sequence of characters sent by a receiver to notify a sender that the last message was received correctly. ACK is also sent by a remote device as a "go–ahead" response to a selection sequence.

Acoustic coupler: A type of modem that permits use of a telephone handset as a connection to the public telephone network for data transmission by means of sound transducers.

Adaptive differential pulse code modulation: One of the methods of pulse code modulation utilized in digitizing an analog signal (32 Kbps is typical).

Adaptive equalization: A modem feature allowing it to automatically compensate for distortions on the line.

Adaptive predictive coding: A methodology used in compressing digitized voice signals.

Algorithm: A prescribed set of well–defined rules or processes for arriving at a solution to a problem. A mathematical process.

Alphanumeric: Made up of letters (alphabetic) and numbers (numeric).

Alternative route: A secondary communications path used to reach a destination if the primary path is unavailable.

Amplitude modulation: Transmission of information on a communications line by varying the voltage level or amplitude.

Ambient noise: Signal interference that is present on a communications line at all times (background noise).

Amplifier: A device that increases the power or amplitude of a signal.

Amplitude variation (ripple): Unwanted variation of signal voltage at different frequencies on a communications line.

Analog signal: A signal that changes in a non-discrete manner (smooth transitioning to different levels).

Answer back: A transmission from a receiving data processing device in response to a request from a transmitting data processing device that it is ready to accept or has received data.

ARQ, Automatic re-transmission request: A generic description of a protocol mechanism that involves re-transmission of message blocks received in error. There are several types of ARQ operation.

Asynchronous: A data transmission which does not require a separate clock signal for the reception of data. In code sets, character codes containing start and stop bits.

Asynchronous transmission (start–stop transmission): Provides transmission of one character at a time with a start bit and one or more stop bits appended on each one. Any amount of time can elapse before the next character can be sent.

Attenuation: Loss of communication signal energy.

Audio frequencies: Frequencies that can be heard by the average human ear, usually between 15 and 20,000 Hz.

Automatic dialer: A device that will automatically dial telephone numbers on the network. Operation of the dialer may be manual or automatic.

B

Backward channel (also called reverse channel): A channel used for sending data in the opposite direction of the primary (forward) channel. The backward channel is usually used for sending data at low speeds for either control purposes or keyboard data.

Balanced circuit: A circuit terminated by a network whose impedance balances the impedance of the line so that the return losses are negligible.

Bandwidth: The information carrying capability of a communications channel or line.

Baseband: The frequency band occupied by individual information bearing signals before they are combined with a carrier in the modulation process. In LANs, one transmitting device at a time on the circuit.

Base group: Twelve communications paths capable of carrying the human voice on a telephone set. A unit of frequency-division multiplexing systems bandwidth allocation.

Baud: Data communication rate unit taken from the name Baudot. Defined as the number of signal level changes per second regardless of the information content of those signals.

Baudot: A five-level code set named for the early French telegrapher who invented it. International Telegraph Alphabet (ITA) Number 2 is the formal name.

Bias: Communications signal distortion with respect to bit timing.

Bit: Binary digit contraction. The smallest unit of data communications information, used to develop code representations of characters.

Bit–oriented protocol: Refers to those data communications protocols that move bits across a data link without regard to the meaning of those bits. Nearly all bit-oriented protocols follow the international HDLC recommendations.

Bit rate: The rate at which bits (binary digits) are transmitted over a communications path. Normally expressed in bits per second (BPS). The bit rate is not to be confused with the data signaling rate (baud), which measures the rate of signal changes being transmitted.

Bit stream: Refers to a continuous series of bits being transmitted on a transmission line.

Blank: A condition of "no information" in a data recording medium or storage location, which can be represented by all spaces or all zeros, depending on the medium.

Block error rate testing: Testing a data line with groups of information arranged into transmission blocks for error checking.

Block: Some set of contiguous bits, bytes, or both that make up a definable quantity of information.

Block check character: A single character appended to the end of a data block for error-checking purposes. The BCC is usually LRC but could also be checksum results.

Blocked Asynchronous/Synchronous Transmission: A proprietary software package for sending asynchronous and synchronous information used primarily by personal computer interfaces.

Blocking: A condition in a switching system or PBX in which no paths or circuits are available to complete a call and no dial tone is

Network terms

returned to the calling party. In this situation there is no alternative but to hang up and try the call again. Also referred to as denial or busy condition.

Block multiplexer channel: A computer peripheral multiplexer channel that interleaves blocks of data. See also Byte multiplexer channel. Contrast with selector channel.

Break: A signal used to "break in" when the opposite party or unit is sending. A feature of dial point-to-point teletypewriter systems operating in half duplex.

Breakout box: A test device utilized for monitoring and inserting signals at the RS-232 interface. Bridge Equipment and techniques used to connect circuits and equipment to each other ensuring minimum transmission impairment. Bridging is normally required on multipoint data channels where the drop for the local loop is separated from the circuit that continues on to the next drop.

Broadband: Refers to transmission facilities whose bandwidth (range of frequencies they will handle) is greater than that available on voice-grade facilities; sometimes called wideband. Also used to describe a particular kind of local area network configuration where multiple different users can share the same cable facility in different channels.

Broadcast: The ability to send messages or communicate with many or all points on a circuit simultaneously.

Burst: A series of events occurring as a group.

Burst error: A series of consecutive errors in data transmission. Refers to the phenomenon on communication lines where errors are highly prone to occurring in groups or clusters.

Bus: A single connective link between multiple processing sites (co-located only) where any of the processing sites can transmit to any other but only one way at a time.

Byte: Some set of contiguous bits that make up a discrete item of information. Bytes are 8 bits long.

Byte multiplexer channel: Multiplexer channel that interleaves bytes of data from different sources. Contrasts with selector channel.

C

Call forwarding: Calls to one station can be automatically switched to another specified station.

Call setup time: The overall length of time required to establish a switched call between pieces of data terminal equipment.

Camp-on: A feature of a switching station or device that notifies a calling station that a called station is busy and allows the calling station to wait and be automatically connected when the line is free.

Carrier: An analog signal at some frequency modified by information (changes to frequency or amplitude or phase or combinations of amplitude and phase) to represent that data in a communication system.

Carrier system: A method of obtaining or deriving several channels from one communication path by combining them at the originating end, transmitting a wideband or high-speed signal, and then separating the original information at the receiving end.

Centrex: A type of private branch exchange service where the equipment is physically located in the local telephone exchange.

Chain: A series of processing locations that information must pass through each location on a store-and-forward basis in order to get to a final location.

Channel: A data communication path.

Channel bank: Communication equipment performing multiplexing. Typically used for multiplexing voice-grade channels.

Character: A language unit composed of bits.

Character parity: A technique of adding an overhead bit to a character code to provide error-checking capability.

Character synchronization: The process through which a receiving device can determine which bits, sent over a data link, should be grouped together into characters.

Checksum: A BCC or BCS that is computed using simple binary addition.

Circuit: The electrical path that provides communication between two or more locations.

Circuit switching: A method of communication in which an electrical connection between calling and called stations is established on demand for exclusive use of the caller until the connection is released.

Clocking: Time synchronizing of communication information.

Cluster: A group of user terminals co-located and connected to a single controller through which each terminal is afforded the opportunity to access a single communication line.

Cluster controller: An intelligent device, usually located at a remote site, that allows several "dumb" terminals or similar devices to connect to a single modem on a data link.

Coaxial cable: Cable with a shield against noise around a signal–carrying conductor.

CODEC, Coder/Decoder: A device for digitizing a voice signal or converting the digitized signal back to voice. Performs the opposite function of a modem.

Communication line controller: A hardware unit that performs line control functions with the modem.

Compandor: A device used on some telephone channels to improve transmission performance. The equipment compresses the outgoing speech volume range and expands the incoming speech volume range on a long–distance telephone circuit.

Concentrator: An electronic device that interfaces in a store and forward mode with multiple communication lines at a message level and then re-transmits those messages via one or more high-speed communications lines to a processing site.

Conditioning: A technique of modifying electrical circuit parameters on a communication line to improve the capability of that line to support higher data transmission rates. (See Equalization.)

Contention: User competition for use of the same communications facilities; a method of line control in which terminals request or bid to transmit. If the channel is not free, the terminals must wait until it is.

Control character: A character that is normally non-printable and used for control purposes rather than for the exchange of information.

Controlled carrier: A feature of a modem that allows the modem carrier signal to be turned on or off under command of the DTE. A controlled carrier is necessary at remote locations on multipoint lines.

Network terms

CRC, cyclic redundancy check: An error-checking control technique utilizing a specifically binary prime divisor that results in a unique remainder.

CSMA/CD, carrier sensed multiple access/collision detection: A method of transmitting information in the local area network environment (LAN) where only one transmitter may be on the line at any one time. If two devices transmit simultaneously, the signals "collide" and both must cease transmission. Each will try again at a later time determined by a different internal delay.

CTS, clear to send: A control line between a modem and a controller used to operate over a communication line.

Current loop: An interface in which the absence or presence of current now (as opposed to voltage levels) is used to provide signaling between devices.

Cursor: A lit area on an electronic display screen used to indicate the next character location to be accessed.

D

Data compression: The technique that provides for the transmission of fewer data bits without the loss of information. The receiving location expands the received data bits into the original bit sequence.

Data set (modem): An electronic terminating unit for analog lines used for data signal modulation and demodulation.

dBm: Power level measurement unit in the telephone industry. 0 dBm is 1mW at 1004 Hz terminated by 600Ω impedance.

Decibel (dB): Power level measurement unit.

Dedicated line: A communication line that is not dialed. Also called a leased line or private line.

Delay: A period of time that elapses between the end of one event and the start of another.

Delay distortion: A distortion that occurs on communication lines due to the different propagation speeds of signals at different frequencies. Some frequencies travel more slowly than others in a given transmission medium and therefore arrive at the destination at slightly different times. Delay distortion is measured in microseconds of delay relative to the delay at 1200 Hz. Delay distortion does not affect voice, but it can have a serious effect on data transmissions.

Demodulator: A functional section of a modem that converts the received analog line signals back to digital form.

Dial line: A communication line that is dialed.

Digital: A two-discrete-state signal.

Distortion: The unwanted modification or change of signals from their true form by some characteristic of the communication line or equipment being used for transmission (such as delay distortion, amplitude distortion).

DPCM, differential pulse code modulation: A method of digitizing an analog signal.

Drop outs: On a communication line, the signal can temporarily disappear, causing loss of data. Drop outs are often caused by environmental influences such as lightning.

E

Echo distortion: A telephone line impairment caused by electrical reflections at distant points where line impedances are dissimilar.

Echoplex: An error-detection method in which characters sent by a terminal to a host are sent back to the terminal and displayed.

Echo suppressor: A device installed in long-distance telephone lines for eliminating echo back to the speaker. Echo suppressors can cause difficulties with simultaneous two-way communications unless they are disabled by the modems.

Emulation: The act of imitating or performing as if a device or program were something else.

Encryption: The technique of modifying a known bit stream on a transmission line so that it appears to be a random sequence of bits to an unauthorized observer.

End office: The first telephone office that a data line is connected to over the local loop or access line. The end switching office for a dialed connection.

Envelope delay: An analog line impairment where a variation of signal delay with frequency occurs across the data channel bandwidth (see Delay distortion).

Equalization: A technique used to compensate for distortions present on a communication channel.

Error rate: The number of errors per unit of information in the test to establish the error rate.

F

FDM, frequency-division multiplexing: A multiplexing technique with which a data line bandwidth is divided into different frequency sub-channels used to share a data line between several user terminals.

Fiber-optics: Glass fibers that carry visible light containing information in cables.

Filter: Electronic circuitry that blocks some components of a signal while allowing other components to pass through uniformly. For example, a high-pass filter blocks all frequencies in a signal that are below a specified frequency called the "cut off."

Firmware: A set of software instructions set permanently or semi-permanently into a read-only memory.

Fixed equalization: A simple equalization technique for modems by which the amount of compensation is preset internally or externally to the modem.

Flag: A bit field or character of data used to set apart the data on either side of the flag. A delimiter.

Flow control: A procedure by which a sending station can be "throttled" so that it does not send more data into the data link or network than can be handled by the link or network.

FM, frequency modulation: A method of transmitting digital information on an analog line by changing the carrier frequency between two different values.

Format: A structure of a message or data such that specific controls or data can be identified by their position during processing.

Forward error correction: The technique that provides for the transmittal of additional information with the original bit stream so that if an error is detected the correct information can be recreated at the receive end without a re-transmission.

Network terms

Four-wire circuit: A circuit that consists of two twisted pair cables. A four-wire circuit provides two separate circuits between stations.

Frame: Bit–oriented protocols refer to data blocks as frames. Also, in T-1 transmissions, 8 bits from each of 24 channels plus 1 frame bit for a total of 193 bits.

Frequency: The number of cycles of an alternating current signal per unit time.

Frequency shift keying, FSK: A form of frequency modulation in which the carrier frequency is made to vary or change in frequency at the instant there is a change in the state of the signal being transmitted (the carrier frequency on the line during a one or marking condition would be shifted to another predetermined frequency during a zero or spacing condition).

Frequency stacking: Another name for FDM, which indicates how the multiplexing is performed.

Front end: An auxiliary computer system that performs network control operations, freeing the host computer system to do data processing.

Full duplex: A four-wire circuit, or a protocol that provides for transmission in both directions at the same time between the same two points.

Full–duplex modem: Provides a channel for sending data in each direction. Full-duplex modems are required for two stations to send data to each other at the same time.

G

Gain: The degree to which the amplitude of a signal is increased. The amount of amplification realized when a signal passes through an amplifier or repeater. Normally measured in decibels.

Gaussian noise: A noise whose amplitude is characterized by the Gaussian distribution, a well known statistical distribution (white noise, ambient noise, hiss).

Geosynchronous: A communication satellite orbit at the correct distance from earth and at the correct speed to appear fixed in space as the earth rotates.

Gigahertz (GHz): An analog frequency unit equal to 1 billion Hz.

Go-back-N: A form of continuous ARQ in which all blocks or frames following a block received in error are discarded and need to be resent.

Group address: Used to address two or more stations in a predesignated group.

Guardband: The unused frequency band between two channels that provides separation of the channels to prevent mutual interference.

H

Half duplex: A communication line consisting of two wires or a protocol capable of transmitting only one direction at a time.

Handshaking: Line termination interplay to establish a data communication path.

Harmonic: Frequencies that are multiples of some fundamental frequency.

Harmonic distortion: A data communications line impairment caused by erroneous frequency generations along the line.

High-level data link control: An ISO standard data communications line protocol.

Hertz: Internationally recognized unit of measure for electrical frequency. The number of cycles per second. Abbreviated Hz.

House cables: Conductors within a building used to connect communications equipment to termination blocks.

Hybrid: An inductive device that converts a two-wire circuit into a four-wire circuit or a four-wire circuit into a two-wire circuit.

I

Impedance: The total opposition offered by a component or circuit to the flow of an alternating or varying current; a combination of resistance, capacitance, and inductance.

Impulse noise: A type of interference on communication lines characterized by high amplitude and short duration. This type of interference may be caused by lightning, electrical sparking action, or by the make-break action of switching devices.

Insertion loss: Signal power loss due to connecting communication equipment units with dissimilar impedance values.

Integrity of data: The status of information after being processed by software or transmitted over a communication link.

Interference: Refers to unwanted occurrences on communications channels that are a result of natural or man-made noises and signals, not properly a part of the signals being transmitted.

Intermodulation distortion: An analog line impairment where two frequencies create an erroneous frequency, which in turn distorts the original data signal representation.

Isochronous: The term given to the movement of start-stop data (asynchronous transmission) over a synchronous data link with each intervening time interval being an integral number of character times.

J

Jitter: Type of analog communication line distortion caused by the variation of a signal from its reference timing positions, which can cause data transmission errors, particularly at high speeds.

K

L

Leased line, private line, dedicated line: A communications line, usually a four-wire circuit, for voice, data, or both leased from a communications carrier on a monthly basis.

Line driver: An inexpensive amplifying device that allows two or more devices to communicate over inexpensive twisted-pair cable up to 2000 feet and up to 19,200 BPS.

Loading coils: Inductive devices that improve the quality of voice transmissions (distorts data signals and must therefore be compensated for by standard modems).

Local loop: The access line from either a user terminal or a computer port to the first telephone office along the line path (also called station loop, end loop, or subscriber loop).

Logging: The act of recording something for future reference, such as error events or transactions.

Loopback: Directing signals back toward the source at some point along a communications path.

Network terms

Loop current: A teletypewriter-to-line interface and operating technique that involves switching an electrical current on and off to represent data bits.

M

Mark: Interface standards define a mark to be the condition of the data line when sending a logic one.

Megahertz, MHz: A unit of analog frequency equal to 1 million Hz.

Message switching: Routing messages among three or more locations by store-and-forward techniques in a computer.

Metallic circuits: Refers to circuits that use metal wire (copper) from end to end. Implies that no loading coils or any other devices are interposed between the ends of the circuit. Metallic circuits have electrical (DC) continuity from end to end.

Microcode: A set of software instructions that executes a macro instruction.

Microwave: A radio carrier system using frequencies whose wavelengths are very short.

Milliampere, mA: Electric current measurement unit equal to 0.001 Ampere.

Milliwatt, mW: A power unit of measurement equal to 0.001 watt.

Modem (data set): An acronym taken from functions the unit performs by modulating and demodulating the digital information from a terminal or computer port into an analog carrier signal to be sent over an analog line.

Modem eliminator: A device that allows two DTE devices to be connected without using modems.

Modem sharing unit: A device that allows several terminals or other devices to share a single modem.

Multiplexer: A device that accepts many data lines and combines them into a single high-speed, composite data stream.

Multipoint line: Also called a multidrop line. A communications line having several subsidiary controllers that share time on the line under control of a central site.

Multistation controller: A terminal controller having more than one terminal device connected to it for subsequent access to the communication line.

N

Narrowband: Refers to a LAN configuration in which only one user can transmit at any one time (sometimes called baseband).

Noise: A communications line impairment that is inherent in the line design or induced by transient bursts of energy.

O

Octet: A group of eight bits that usually, though not necessarily, represents a byte, or word, and so on.

P

Packet switching: The transfer of data by means of addressed packets whereby a channel is only occupied for the duration of transmission of the packet. The channel is then available for the transfer of other packets.

PAD, packet assembler/disassembler: Equipment providing packet assembly and disassembly facilities.

Parity error: An error that occurs in a particular entity of data in which an extra or redundant bit is sent with the data. Detects only odd numbers of bit errors. Even numbers of bit errors are not detected.

Pass–band filters: Filters used in modem design to allow only the frequencies within the communication channel to pass, while rejecting all frequencies outside the pass band.

Patching jacks: Series–access devices used to patch around faulty equipment using spare units.

Private branch exchange: A telephone switchboard.

PCM, pulse code modulation: A generic method of converting an analog signal to a digital form.

Phase hits: A sudden electrical disturbance on a communication line which causes the phase of the carrier signal to change, causing bit errors on the data link.

Phase jitter: An analog line impairment caused by power and communication equipment along the line, shifting the signal phase relationship back and forth.

PM, phase modulation: A method of combining digital information onto a line-carrying signal by variation of the phase relationship of the signal. May also indicate preventive maintenance in the form of service functions provided during periods of normal operation to reduce the probability of failure later on.

Point to point: A communications line connected directly from one point to another, as opposed to multipoint lines.

Polling: A control message sent from a master site to a slave site as an invitation for the slave site to transmit data to the master site.

Propagation delay: The time necessary for a signal to travel from one point on the circuit to another.

Protocol: A formal set of conventions governing the format and control of inputs and outputs between two communicating processes. Includes handshaking and line discipline.

PSK, phase shift keying: A method of analog modulation utilizing differences in phase only as representing data bit one of several ways to represent an analog signal. Typical methods involve modifying the amplitude (PAM), width or duration (PDM), or position (PPM). The most common pulse modulation technique in telephone work is pulse code modulation (PCM). In PCM, the analog signals are sampled at regular intervals and a series of binary bits representing the amplitude of each pulse is transmitted, representing the amplitude of the information signal at that time. The standard sampling in today's environment is 8000 times per second with 8 binary bits representing each sample pulse giving a required transmission rate of 64,000 BPS.

Q

QAM, quadrature amplitude modulation: A method of modulation in which two carriers in quadrature are used for modulation. One carrier is used for modulating the X axis and the other carrier is used for modulating the Y axis.

Quadrature distortion: Analog signal distortion frequently found in phase modulation modems.

R

Regenerative repeaters: A device interposed between the ends of a data link or between nodes of a network to regenerate distorted signals. Used in digital transmission.

Network terms

Response time: The time measured from the depression of the enter key at a terminal to the display of the first character of the response at that terminal site.

Reverse channel: An optional feature provided on some modems that provides simultaneous communication from the receiver to the transmitter on a two-wire channel. It may be used for circuit assurance, circuit breaking, and facilitating certain forms of error control and network diagnostics. Also called backward channel.

RTS, request to send: An RS-232 control signal that requests a data transmission on a communication line.

S

SDLC, synchronous data link control: An IBM data communications message protocol. A subset of HDLC.

Slicing level: A voltage or current level of a digital signal that determines whether a one or zero bit will be recognized.

Slot: A unit of time in a TDM frame in which a sub-channel bit or character is carried to the other end of the circuit and extracted by the receiving TDM unit.

S/N, signal–to–noise ratio: The relative power levels of a communication signal and noise on a data line, expressed in decibels.

Space-division multiplexing: Refers to using a separate circuit or channel for each device. Essentially this means no multiplexing at all. If, for example, a new terminal needs to be added to a system, a separate wire is run to accommodate it.

Start bit: In asynchronous transmission, the start bit is appended to the beginning of a character so that the bit sync and character sync can occur at the receiver. The start bit is always a "0" or "space" condition.

Start–stop: Also known as asynchronous transmission. A transmission technique in which each character is preceded by a start bit and followed by a stop bit.

Stop-and-wait ARQ: A form of ARQ in which the sender sends one block of data and stops sending until an acknowledgment for that block is received from the receiver. An example is bisync.

Stop bit: In asynchronous transmission, the stop bit is appended to th end of each character. The stop bit is always a "1" or "mark" condition. It sets the receiving hardware to a condition where it looks for the start bit of a new character. May be 1 or 2 bits.

Store and forward: A data communication technique that accepts messages or transactions, stores them until they are completely in the memory system, and then forwards them to the next location as addressed in the message or transaction header.

Streaming: A condition of a remote modem when it is sending a carrier signal on a multi-drop communication line and will not turn off.

String coding: A technique for combining multiple sequential occurrences of the same character or bits.

Switched service: A common carrier communications service that requires that call establishment take place before a data link can be established. For example, DDD is a switched service.

Sync (syn): A bit or character used to synchronize a time frame in a TDM. Also a synchronizing sequence used by synchronous modems to perform bit synchronization and by the line controller for character synchronization.

Synchronous modem: A DCE that utilizes a clocking signal to perform bit synchronization with the incoming data.

Synchronous transmission: Messages sent in blocks where all characters or bits are sent contiguously. No start or stop bits are appended to characters. Each block begins with a sync sequence and a start of message sequence so that character framing can occur at the receiver and ends with an end of message sequence to prepare the receiver to look for a new message.

T

Tariff: The rates, rules, and regulations concerning specific equipment and services provided by a communications carrier.

T-Carrier: The AT&T name for their digital carrier system used for carrying data or digitized voice signals.

TDMA, time division multiple access: A method utilized primarily in satellite transmission in which various users share their time on the same satellite link (portions of separate users are multiplexed onto the same link through a satellite).

Telemetry: Collection and transmission of data obtained from remote locations by sensing conditions in a real-time environment.

Telex: A teletypewriter service that allows subscribers to send messages to other subscribers on an international level over the public telephone network.

Terrestrial circuits: Non-satellite channels.

Text: That part of a message or transaction between the control information of the header and the control information of the trace section or tail that constitutes the information to be processed or delivered to the addressed location.

Thermal noise: A type of electromagnetic noise produced in conductors or in electronic circuitry that is proportional to temperature. See also Gaussian noise.

Time-division multiplexing, TDM: A technique for combining several information channels into one facility or transmission path in which each channel is allotted a specific position in the signal stream based on time. At the receiving end, the signals are separated to reconstruct the individual input channels.

Time-out: A protocol procedure that requires a device to make some response to a command or message block within a certain period of time. If the response does not occur within that period of time, a time-out condition occurs, which is considered an error condition.

Time sharing: A processing technique by which multiple users at their own remote terminals have the ability to share common computer resources at the same time.

Trailer or trace block: Control information transmitted after the body or text of a message or transaction used for tracing error events, timing the communications through the network, and recovering misplaced blocks or transactions after system failures.

Transparency: A transmission mode achieved when both the sending and receiving devices do not react to the content of the data they are sending.

Trunk: A multiple line circuit that connects two switching or distribution stations or centers. Also a circuit from a PBX to a Class 5 telephone office.

Network terms

Turnaround time: The time required for a modem to reverse direction of transmission on a two-wire circuit.

U

V

Validity checking: The techniques used to check the accuracy of data after transmission on data lines.

VF, voice frequency or voice-grade line: A 4.2kHz bandwidth telephone channel designed to carry the human voice from one telephone set to another. The usable portion of the band is 300 Hz to 3300 Hz.

VHF, very high frequency: A radio carrier frequency band used in radio transmissions.

VRC, vertical redundancy checking: A method of character parity checking.

W

WATS, Wide Area Telephone Service: A flat rate or measured bulk rate long–distance telephone service provided on an incoming or outgoing basis. By use of an access line, WATS permits a customer to make telephone calls to any dialable telephone number in a specific zone for an hourly rate. INWATS permits reception of calls from specific zones over an access line in like manner but the called party is charged with the call. The United States has been divided into five zones of increasingly greater coverage depending on the location of the customer.

White noise: See Gaussian noise; Thermal noise.

Wideband: In LAN systems, the ability for multiple users to communicate simultaneously in different channels. Same as broadband.

Word: One or more contiguous bytes, which may also be used to identify a class of computer.

NETWORK STANDARDS

Three types of Network Standards are described here. The first will be the Electronic Industries Association (EIA) specifications, which are always preceded by the letters RS (Recommended Standard) or EIA. The second set will be the CCITT standard interface specifications, which are always preceded by the letter V, and the third series of specifications, also established by the CCITT, are always preceded by the letter X. A V specification deals primarily with telephone circuits, while the X specifications deal primarily with data interfaces and public data networks. The most common specifications in use today are identified below.

EIA–232–D. Interface between data terminal equipment and data communication equipment employing serial binary data interchange (January 1987).

EIA–269–B. Synchronous signaling rates for data transmission (January 1976; identical to ANSI X3.1–1976).

EIA–334–A. Signal quality at interface between data processing terminal equipment and synchronous data communication equipment for serial data transmission (August 1981) (also adopted as ANSI X3.24–1967).

EM–334–A–1. Addendum No. 1 to EIA–334–A and EIA–404. Application of signal quality requirements to EIA449.

EIA–357. Interface between facsimile terminal equipment and voice–frequency data communication terminal equipment (June 1968).

EIA–363. Standard for specifying signal quality for transmitting and receiving data processing terminal equipment using serial data transmission at the interface with non-synchronous data communication equipment (May 1969).

EU–366–A. Interface between data terminal equipment and automatic calling equipment for data communication (March 1979).

EIA–404–A. Standard for start/stop signal quality between data terminal equipment and non-synchronous data communication equipment ANSI approved (January 1986).

EIA–404–1. Addendum No. 1 to EIA–404 and EIA–334–A. Application of signal requirements to EIA449.

EIA–410. Standard for electrical characteristics of class A closure interchange circuits (April 1974).

EIA–422–A. Electrical characteristics of balanced voltage digital interface circuits (December 1978).

EIA–423–A. Electrical characteristics of unbalanced voltage digital interface circuits (December 1978).

EIA–449–1. General–purpose 37–position interface for Data Terminal Equipment and Data Circuit terminating Equipment employing serial–binary data interchange. (The electrical signal characteristics for EIA–449 are defined by either EIA–422 or EIA–423, since EIA–449 is only a mechanical and functional definition standard) (February 1980).

EIA–470–A. Telephone instruments with loop signaling. Performance and technical criteria for connecting and interfacing various elements of the public telephone network.

EIA–491. Interface between a numerical control unit and peripheral equipment employing asynchronous binary data interchange over circuits having EIA–423–A electrical characteristics (October 1982).

EIA–496. Interface between data communication equipment (DCE) and the public switched telephone network (PSTN). ANSI approved (May 1984).

EIA–S30. High–speed 25–position interface for Data Terminal Equipment and Data Circuit Terminating Equipment. ANSI approved (March 1987).

V. CCITT. Code designation.

V.1. Equivalence between binary notation symbols and the significant conditions of a two–condition code.

V.2. Power levels for data transmission over telephone lines.

V.3. International Telegraph Alphabet No. 5.

V.4. General structure of signals of International Telegraph Alphabet No. 5 code for data transmission over public telephone network.

V.5. Standardization of data–signaling rates for synchronous data transmission in the general switched telephone network.

V.6. Standardization of data–signaling rates for synchronous data transmission on leased telephone–type circuits.

V.7. Definition of terms concerning data communication over the telephone network.

V.10(X.26). Electrical characteristics for unbalanced double–current interchange circuits for general use with integrated circuit equipment in the field of data communications (and provisional amendments, May 1977).

Network terms

V.11(X.27). Electrical characteristics for balanced double–current interchange circuits for general use with integrated circuit equipment in the field of data communications (and provisional amendments, May 1977).

V.15. Use of acoustic coupling for data transmission.

V.19. Modems for parallel data transmission using telephone signaling frequencies.

V.20. Parallel data transmission modems standardized for universal use in the general switched telephone network.

V.21. 300–bit/s full–duplex modem standardized for use in the general switched telephone network.

V.22. 1200 BPS full–duplex modem standardized for use in the general switched telephone network and on point–to–point two–wire leased telephone–type circuits.

V.22bis. 2400 BPS full–duplex modem using the frequency division technique standardized for use on the general switched telephone network and on point–to–point two–wire leased telephone–type circuits.

V.23. 600/1.2K BPS modem standardized for use in the general switched telephone network.

V.24. List of definitions for interchange circuits between data terminal equipment and data circuit terminating equipment (and provisional amendments, May 1977).

V.25. Automatic calling and/or answering equipment on the general switched telephone network, including disabling of echo suppressors on manually established calls.

V.25bis. Automatic calling and/or answering equipment on the general switched telephone network using the 100 series interchange circuits.

V.26. 2.4/1.2 KBPS modem standardized for use on four–wire leased telephone–type circuits.

V.26bis. 2.4/1.2 KBPS modem standardized for use in the general switched telephone network.

V.26ter. 2.4 KBPS full–duplex modem using the echo cancellation technique standardized for use on the general switched telephone network and on point–to–point two–wire leased telephone–type circuits.

V.27. 4.8 KBPS modem with manual equalizer standardized for use on leased telephone–type circuits.

V.27bis. 4.8 KBPS modem with automatic equalizer standardized for use on leased telephone–type circuits.

V.27ter. 4.8/2.4 KBPS modem standardized for use in the general switched telephone network.

V.28. Electrical characteristics for unbalanced double–current interchange circuits.

V.29. 9.6 KBPS modem standardized for use on point–to–point four–wire leased telephone–type circuits.

V.31. Electrical characteristics for single–current interchange circuits controlled by contact closure.

V.32. A family of two–wire, full–duplex modems operating at data signaling rates of up to 9600 BPS for use on the general switched telephone network and on leased telephone–type circuits.

V.35. Data transmission at 48 KBPS using 60– to 108–kHz group band circuits. V.36. Modems for synchronous data transmission using 60– to 108–kHz group band circuits.

V.37. Synchronous data transmission at a data signaling rate higher than 72 KBPS using 60–108 kHz group band circuits.

V.40. Error indication with electromechanical equipment.

V.41. Code independent error control system.

V.50. Standard limits for transmission quality of data transmission.

V.51. Organization of the maintenance of international telephone–type circuits used for data transmission.

V.52. Characteristics of distortion and error–rate measuring apparatus for data transmission.

V.53. Limits for the maintenance of telephone–type circuits used for data transmission.

V.54. Loop test devices for modems.

V.55. Specification for an impulsive noise measuring instrument for telephone–type circuits.

V.56. Comparative tests of modems for use over telephone–type circuits.

V.57. Comprehensive data test set for high data signaling rates.

V.100. Interconnection between public data networks (PDNs) and the public switched telephone network (PSTN).

V.110. Support of data terminal equipment (DTEs) with V–series type interfaces by an integrated services digital network (ISDN).

X

X. CCITT Recommendation designation.

X.1. International user classes of service in public data networks.

X.2. International user facilities in public data networks.

X.3. Packet assembly/disassembly facility (PAD) in a public data network.

X.4. General structure of signals of international alphabet no. 5 code for data transmission over public data networks.

X.20. Interface between data terminal equipment and data circuit–terminating equipment for start/stop transmission services on public data networks.

X.20bis(V.21). Compatible interface between data terminal equipment and data circuit–terminating equipment for start/stop transmission services on public data networks.

X.21. General–purpose interface between data terminal equipment and data circuit–terminating equipment for synchronous operation on public data networks.

X.21bis. Use on public data networks of data terminal equipment that is designed for interfacing to synchronous V–series modems.

X.24. List of definitions of interchange circuits between data terminal equipment and data circuit–terminating equipment on public data networks.

X.25. Interface between data terminal equipment and data circuit–terminating equipment for terminals operating in the packet mode on public data networks (and provisional amendment, April 1977).

Network terms

X.26. Electrical characteristics for unbalanced double–current interchange circuits for general use with integrated circuit equipment in the field of data communications (identical to V.10).

X.27. Electrical characteristics for balanced double–current interchange circuits for general use with integrated circuit equipment in the field of data communications (identical to V.11).

X.28. DTE/DCE interface for start/stop mode data terminal equipment accessing the packet assembly/disassembly facility (PAD) on a public network situated in the same country.

X.29. Procedures for exchange of control information and user data between a packet–mode DTE and a packet assembly/disassembly facility (PAD).

X.30. Standardization of basic model page–printing machine in accordance with International Telegraph Alphabet No. 5.

X.31. Characteristics, from the transmission point of view, at the interchange point between data terminal equipment and data circuit–terminating equipment in a 200 BPS start/stop data terminal.

X.32. Answer–back units for 200 BPS start/stop machines in accordance with International Telegraph Alphabet No. 5.

X.33. Standardization of an international text for the measurement of the margin of start/stop machines in accordance with International Telegraph Alphabet No. 5.

X.92. Hypothetical reference connections for public synchronous data net– works.

X.95. Network parameters in public data networks.

X.96. Call progress signals in public data networks.

X.500. A specification defining the universal interconnectivity of public electronic mail networks. X.500 implies a global directory for all of the different services, not just electronic mail; services include telephone, Telex, and other networks. X.500 is in its early stages of development.

X3.1. Synchronous signaling rates for data transmission.

X3.4. Code of information interchange.

X3.15. Bit sequencing of the American National Standard Code for Information Interchange in serial–by–bit transmission.

X3.16. Character structure and character parity sense for serial–by–bit data communication in the American National Standard Code for Information Interchange.

X3.24. Signal quality at interface between data processing technical equipment for synchronous data transmission.

X3.25. Character structure and character parity sense for parallel–by–bit communication in the American National Standard Code for Information Interchange.

X3.2. Procedures for the use of communication control characters of American National Standard Code for Information Interchange in specified data communications links.

X3.36. Synchronous high–speed data signaling rates between data terminal equipment and data communication equipment.

X3.41. Code extension techniques for use with seven–bit coded character set of American National Standard Code for Information Interchange.

X3.44. Determination of the performance of data communication systems.

X3.57. Message heading formats for information interchange using ASCII for data communication system control.

Networking acronyms

A

AAL ATM Adaptation Layer, two sublayers concerned with segmenting large PDUs into ATM cells; type 1 = CBR, 2 = VBR. See also SAR.

ABM Asynchronous Balanced Mode (layer 2).

ACD Automatic Call Distributor, PBX function or machine to spread calls among phones.

ACF Access Control Field, first byte in ATM header (802.6).

ACK Positive Acknowledgment, message or control bytes in a protocol (DtE + 1/0).

A/D Analog-to-Digital, usually a conversion of voice to digital formt.

ADCCP Advanced Data Communications Control Procedure, ANSI counterpart to HDtC.

ADCU Association of Data Communications Users.

ADM Add/Drop Multiplexer, node with 2 aggregates that supports data pass–through.

ADM Asynchronous Disconnected Mode (layer 2).

ADNS ARINC Data Network Service, a packet network.

ADPCM Adaptive Differential Pulse Code Modulation, a form of voice compression that typically uses 32 kbit/s.

ALS Active Line State, possible status of FDDI optical fiber.

AMI Alternate Mark Inversion, line coding for T–1 spans where 0 (space) is no voltage and successive 1s (marks) are pulses of opposite polarity. See also DMC, NRZ, 4B/5B.

AN Access Node.

ANSI American National Standards Institute, the US member of the ISO.

APDU Application PDU (OSI).

APS Automalic Protection Switch.

ARP Address Resolution Protocol, a way for routers to adjust addresses between different protocols or domains.

ARPA Advanced Research Projects Agency, created Arpanet packet network, folded into NSFnet in 1990.

ARQ Automatic Repeal reQuest, for retransmission; an error correction scheme for data links, used with a CRC.

ASCII American Standard Code for Information Interchange, based on 7 bits plus parity.

ASE Applications Service Element, protocol at upper layer 7 (SS7, OSI).

ASR Automatic Send/Receive, a printer with keyboard or a Teletype machine.

ATD Asynchronous Time Division, ETSI proposal for pure cell relay, without SONET or other framing.

ATM Asynchronous Transfer Mode, a type of framing used in BISDN and SONET.

AU Administrative Unit, payload plus pointers (SDH).

AUG AU Group, one or more AUs to fill an STM (SDH).

AWG American Wire Gauge, conventional designator of wire size.

B

B Bearer channel, a DS–0 for user trafrlc.

BCC Block Check Code, a CRC or similarly calculated number to find transmission errors.

BCD Binary Coded Decimal, 4–bit expression for 0 (0000) to 9 (1001).

BCM Bit Compression Mux, same as M44 for ADPCM.

BCN Beacon, frames sent downstream by station on ring when upstream input is lost (802.5).

B-DCS Broadband Digital Cross–connect System, DACS OC–1, STS–1, DS–3 and higher rates only (see W–DCS).

BER Bit Error Ratio, errored bits over total bits; should be < 1^{-7} for transmission lines.

BERT Bit Error Ralc Test(er).

BIP Bit Interleaved Parity, error checking method (BIP8 in SONET).

BISDN Broadband ISDN, generally access at more than 100 Mbit/s.

BISYNC Binary Synchronous communications, a protocol.

BITS Building Integrated Timing Supply, stratum 1 clock in CO.

BNS Broadband Network Switch, usually ATM or packet based, DS–3 and faster.

BOC Bell Operating Company, a telephone company.

bps Bits per second, serial digital stream data rate, now bit/s.

BPV Bipolar Violation, two pulses of the same polarity in a row.

BRA Basic Rate Access, ISDN 2B+D loop.

BRI Basic Rate Interface, 2B+D on one local loop.

BSC Binary Synchronous Communications, a half-duplex protocol.

BSS Broadband Switching System, cell-based CO switch for B-ISDN.

BWB Bandwidth Balancing, method to reduce a station's access to a transmission bus, to improve fairness (802.6).

C

C Capacitance, the property of a device that holds an electrical charge.

CASE Common Application Service Elements, application protocol (MAP).

CBR Constant (Continuous) Bit Rate, channel or service in ATM network for voice or sync data in a steady flow.

CBX Computerized Branch eXchange, PABX.

CCITT Comite Consultatif Internationale de Telegraphique et Telephonique, The International Telegraph and Telephone Consultative Committee, part of ITU.

CCIR International Radio Consultative Committee, sister group to CCITT.

CCR Commitment, Concurrency and Recovery (OSI).

CCS Common Channel Signaling.

CCSA Common Control Switching Arrangement.

Networking acronyms

CCS6 CCS system 6, first out of band signaling system in N.A. (CCIS).

CD Carrier Detect, digital output from modem when it receives analog modem signal.

CD Count Down, a counter that holds the number of cells queued ahead of the local message segment (802.6).

CDMA Code Division Multiple Access, spread spectrum; broadcast frequency changes rapidly in pattern known to receiver.

CELP Code-Excited Linear Predictive coding, a voice compression algorithm used at 8 kbit/s.

CEPT Conference on European Posts & Telecommunications (Conference of European Postal and Telecommunications administrations), a body that sets policy for services and interfaces in 26 countries.

CFA Carrier Failure Alarm, detection of red (local) or yellow (remote) alarm on T-1.

CGA Carrier Group Alarm, trunk conditioning applied during CFA.

CIT Computer Integrated Telephony, DEC's PHI.

CL Common Language, Bellcore codes to identify equipment, locations, etc.

CL ConnectionLess.

CLLM Consolidated Link Layer Management (802).

CLN Connectionless Network, packet address is unique and network routes all traffic.

CLNP Connectionless mode Network (layer) Protocol (SONET).

CLTS Connectionless Transport Service, OSI datagram protocol.

CMA Communications Managers Association.

CMDR Command Reject, similar to FRMR (HDLC).

CMI Coded Mark Inversion, line signal for STS–3.

CMIP Constanl Mark, Inverted; line coding for T–1 local loop in Japan.

CMIP Common (network) Management Information Protocol, part of the OSI network management scheme, connection oriented .

CMIS Common (network) Management Information Service, runs on CMIP (OSI).

CMISE CMIS Element.

CMOS Complementary Metal Oxide Semiconductor, low power method (lower than NMOS) to make ICs.

CMOT CMIP over TCP/IP.

CMT Connection Management, part of SMT that establishes physical link between adjacent stations (FDDI).

CO Central Office, of a phone company, where the switch is located; the other end of the local loop opposite CP.

COC Central Office Connection, separately tariffed part of T–1 circuit within a CO.

COCF Connection Oriented Convergence Function, MAC–layer entity.

CODEC COder–DECoder, converts analog voice to digital, and back.

COFA Change of Frame Alignment, movement of SPE within STS frame.

CO-LAN Central Office Local Area Network, a data switching service based on a data PBX in a carrier's CO.

CONP Connection mode Network layer Protocol.

COS Class Of Service.

Interconnection Networking in Europe.

COT Central office Terminal, equipment at CO end of digital loop or line.

CP Central Processor, CPU that runs network under center–weighted control.

CP Customer Premises, as opposed to CO.

CPE Customer Premises Equipment, hardware in user's office.

CPI Computer–PBX Interface, a data interface between NTI and DEC.

CPN Customer Premises Node, CPE.

CPU Central Processor Unit, the computer.

CR Carriage Return, often combined with a line feed when sending to a printer.

CRC Cyclic Redundancy Check, an error detection scheme, used with ARQ.

CRV Coding Rule Violation, unique bit signal for F bit in frame 1 of CMI.

CS Convergence Sublayer, where header and trailer are added before segmentation.

CSC Circuit–Switched Channel (Connection).

CSMA Carrier Sense Multiple Access, a LAN transport method, usually with "/CD" for collision detection or "/CA" collision avoidance.

CSPDN Circuit Switched Public Data Network.

CS–PDU Convergence layer PDU, info plus new hcader and trailer to make packet that is segmented into cells or SUs.

CSU Channel Service Unit, the interface to the T–1 line that terminates the local loop.

CTS Clear To Send, lead on interface indicating DCE is ready to receive data.

CV Coding Violation, transmission error in SONET section.

CVSD Continuously Variable Slope Delta modulation, a voice encoding technique offering variable compression.

D

D Delta (or Data) channel, 16 kbit/s in BRI, 64 kbit/s in PRI, used for signaling (and perhaps some packet data).

D3 Third generation channel bank, 24 channels on one T–1.

D4 Fourth generation digital channel bank, up to 48 voice channels on two T–1's or one T–1C.

D5 Fifth generation channel bank with ESF.

DA Destination Address, field in frame header (802).

D/A Digital-to-Analog, decoding of voice signal.

D/A Drop and Add, similar to drop and insert.

DACS Digital Access and Cross–connect System, a digital switching device for routing T–1 lines, and DS–O portions or lines, among multiple T–1 ports.

Networking acronyms

DARPA Defense ARPA, formerly just ARPA.

DAS Dual–Attached (Access) Station, device on main dual FO rings, 4 fibers (FDDI).

DASS Digital Access Signaling System, protocol for ISDN D channel in U.K.

dB Decibel, 1/10th of a bel; 10 log (x/y) where x/y is a ratio or like quantities (power).

dBm Decibel level referenced to 1 mW at 1004 Hz into 600 ohms impedance.

dBm0 Power that would be at zero TLP reference level, = measurement – (TLP at that point).

dBrn Power level relalivc to noise, dBm + 90.

dBrnC dBrn through a C–weighted audio filter (matches ear's response).

DB25 Code for 25–pin connector specified for RS–232 I/F.

D.C. Direct Current, used for some signaling forms; type of power in CO.

DCC Data Communications Channel, overhead connection in D bytes for SONET management.

DCE Data Circuit–terminating Equipment, see next DCE.

DCE Data Communications Equipment, 'gender' of interface on modem; see DTE.

DCS Digital Cross–connect System, DACS.

DDCMP Digital Data Communications Message Protocol.

DDD Direct Distance Dialing, refers to PSTN.

DDS Digital Data System, network that supports DATAPHONE Digital Service.

DDSD Delay Dial Start Dial, a start–stop protocol for dialing into a CO switch.

DES Data Encryption Standard, moderately difficult to break.

D/I Drop and Insert a mux function or type.

DIP Dual In–line Package, for chips and switches.

DIS Draft International Standard, preliminary form of OSI standard.

DISC Disconnect, command frame sent between LLC entities (layer 2).

DLC Data Link Connection, one logical bit stream in LAPD (layer 2).

DLC Digital Loop Carricr, mux system to gather analog loops and carry thcm to CO.

DLCI Data Link Connection Identifier, address in a frame (I.122).

DLE Data Link Escape, ESC.

DLL Data Link Layer, layer 2 (OSI).

DM Disconnected Mode, LLC frame to reject a connection request (layer 2).

DMC Differential Manchester Code, pulse pattern that puts transition at center of each bit time for clocking, transition [none] at start of period for 0 [1] (802.5).

DMI Digitally Multiplexed Interface, AT&T interface for 23 64 kbit/s channels and a 24th for signaling.

DMPDU Derived MAC Protocol Data Unit, a 44–octet segment of upper layer packet plus cell header/trailer (802.6); see L2PDU.

DMS Digital Multiplex System.

DNA Digital Network Architecture, DEC's networking scheme.

DNIC Data network Identification Code, assigned like an area code to public data networks.

DNIC Data Network Interface Circuit, 2B+D ISDN U interface.

DNIS Dialed Number Identification Service, where carrier delivers number of called extension after PBX acknowledges call.

DNR DCE Not Ready, signaling bit in CMI.

DoV Data over Voice, modems combine voice and data on one twisted pair.

DP Dial Pulse, rotary dialing rather than DTMF.

DPBX Data PBX, a switch under control of end users at terminals.

DPCM Differential Pulse Code Modulation, voice compression algorithm used in ADPCM.

DPNSS Digital Private network Signaling System, PBX interface for common channel signaling.

DPO Dial Pulse Originate, a form of channel bank plug–in that accepts dial pulses.

DPT Dial Pulse Terminate, a channel bank plug that outputs pulses.

DQDB Distributed Queue Dual Bus, an IEEE 802.6 protocol to access MAN's, typically at T–1, T–3, or faster.

DS–0 Digital Signal level 0, 64,000 bit/s, the worldwide standard speed for PCM digitized voice channels.

DS–OA Digital Signal level 0 with a single rate adapted channel.

DS–0B Digital Signal level 0 with multiple channels sub–rate multiplexed in DDS format.

DS–1 Digital Signal level 1, 1.544 Mbit/s in North America, 2.048 Mbit/s in CCITT countries.

DS–1A Proposed designation for 2.048 Mbit/s in North America.

DS–1C Two T–1's, used mostly by Telcos internally.

DS–2 Four T–1's, little used in US, common in Japan.

DS–3 Digital Signal level 3, 44.736 Mbit/s, carrying 28 T–1's.

DSAP Destination Service Access Point, address field in header of LLC frame to identify a user within a station address (layer 2).

DSI Digital Speech Interpolation, a voice compression technique that relies on the stalistics of voice traffic over many channels.

DSP Digital Signal Processor, specialized chip optimized for fast computations.

DSP Display System Protocol, protocol for faster bisync traffic over packet nets.

DSR Data Set Ready, signal indicating DCE and line ready to receive data.

DSSI D–channel Signaling System 1, access protocol for switched connection signaling (Q.931 & ANSI T1S1/90–214).

Networking acronyms

DSU Digital (Data) Service Unit, converts RS–232 or other terminal interface to line coding for local loop transmission.

DTAU Digital Test Access Unit, CO equipmcnt on T–1 line.

DTE Data Terminal Equipment, 'gender' of interface on terminal or PC; scc DCE.

DTMF Dual Tone Multi–Frequency, TOUCHTONE dialing, as opposed to DP.

DTR Data Terminal Ready, signal that terminal is ready to receive data from DCE.

DVI Digital Video Interactive, applications with large, bursty bandwidth.

DX Duplex, a 2–way audio channel bank plug without signaling.

E

E–1 European digital signal level 1, 2.048 Mbit/s.

E&M Signaling leads on a voice tie line, known as Ear and Mouth.

EBCDIC Extended Binary Coded Decimal Interchange Code, extended character SCI on IBM hosts.

EC Error Correction, process to check packets for errors and send again if needed.

ECC Error Checking Code, 2 bytes (usually) in frame or packet derived from data to let receiver test for transmission errors.

ECL Emilter Coupled logic, transislor clrcuit type optimized for high speed.

ECN Explicit Congestion Notification, network warns terminals of congestion by setting bits in frame header (I.122).

ECO Engineering Change Order, document from designer ordering change in product.

ED Ending Delimiter, unique symbol to mark end of LAN frame (TT in FDDI, HDLC flag, etc.).

EDI Electronic Document (Data) Interchange, transfer of business information (P. 0., invoice, etc.) in defined formats.

EGP Exterior Gateway Protocol, on the Internet (TCP/IP).

EIA Electronic Industries Association, publisher of standards (e.g. RS–232).

EMI Electro Magnetic Interference.

EMS Element Management System, usually a vendor–specific NMS for a hardware domain (OSI).

ENQ Enquiry, control byte that requests a repeat transmission or control of line.

EOC Embedded Operation Channel, D bytes devoted to alarms, supervision, and provisioning (SONET).

EOM End of Message.

EOT End Of Transmission, control byte; preceded by DLE indicates switched station going on hook.

ERL Echo Return Loss.

ERS Errored Second, a 1 sec. interval containing 1 or more transmission errors.

ESB Errored Second type B, new name for bursty ES.

ESC Escape, an ASCII character.

ESD ElectroStatic Discharge, electrical "shock" from person or other source that can destroy semiconduclors.

ESS Electronic Switching System, a CO switch.

ETC End of Transmission Block, control byte in BSC.

ETN Electronic Tandem network.

ETO Equalized Transmit Only, voice interface with compensation to correct for frequency response of the line.

ETX End of Text, control byte.

F

F Final, control bit in frame header (layer 2).

F Framing, bit position in TDM frame where known pattern repeats.

FACS Facility Assignment Control System, for telco to manage outside plant (local loops).

FAD Frame Assembler/Disassembler, functlons like a PAD, but for frames.

FADU File Access Data Unit (OSI).

FAS Frame Alignment Signal, bit or byte used by receiver to locate TDM channels.

FAX Facsimile.

FB Framing Bit.

FC Frame Control, field to define type or frame (FDDI).

FCC Federal Communication Commission, regulates communications in US.

FCOT Fiber oplic Central Office Terminal.

FCS Frame Check Sequence, error checking code (layer 2).

FDDI Fiber Distributed Data Interface, 100 Mbit/s FO standard for a LAN or MAN.

FDL Facility Data Link, part of the ESF framing bits available for user data, in some cases.

FDM Frequency Division Multiplexer.

FDX Full Duplex.

F_C Extended framing ("F sub c"), old name for ESF.

FEC Forward Error Correction, using redundancy in a signal to allow the receiver to correct transmission errors.

FEP Front End Processor, peripheral computer to mainframe CPU, handles communications.

FEXT Far End Cross Talk.

FIB Forward Indicator Bit, field in SUs (SS7).

FID Format Identification, bit C–1 in DS–3 format shows if M13, M28, or Syntran signal.

FIFO First In First Out, buffer type that delays bit stream.

FISU Fill–In Signaling Unit, 'idle' packet that carries ACKs as sequence numbers (SS7).

FITL Fiber In The Loop, optical technology from CO to customer premises.

Networking acronyms

FIX Fcdcral Interncl Exchangc, point or interconnection for U.S. agency research networks.

FO Fibcr Optic, bascd on optical cable.

FOTP Fiber Optic Test Procedure.

FOTS Fiber Optic Terminal System, mux or CO switch interface.

FPDU FTAM PDU.

FPDU Frame relay protocol Data Unit (I.122).

FR Frame Relay, interface to simplified packetized switching network (I.122).

FRS Frame Relay Switch.

FRMR Frame Reject, LLC response to error that cannot be corrected by ARQ, may cause reset or disconnect (layer 2).

FS Failed Second, now called UAS.

FSN Forward Sequence Number, sent sequence number of this SU/packet (SS7).

FT–1 Fractional T–1, digital capacity of N x 64 kbit/s but usually less than 1/2 a T–1.

FTAM File Transfer, Access, and Management; an OSI layer–7 protocol for LAN interworking (802).

FTP File Transfer Protocol (TCP/IP)

FLLC Fiber To The Curb, local loop is fibcr from CO to just outside CP, wire into CP.

G

G3 Group 3, analog facsimile standard at up to 9.6 kbit/s.

G4 Group 4, digital facsimile standard at 56/64 kbit/s.

Gbit/s Giga bit/s per second, billions (10^9) per second.

GOSIP Government OSI Profile, suite of protocols mandated for US Federal and U.K. contractors; –T = Transport model; –A = Application model.

GPS Global Positioning System, satellites that report exact time

GS Ground start, analog phone interface.

GSM Group Special Mobile, part of CEPT working on cellular.

GSTM General Switched Telephone Network, CCITT term to replace PSTN after 1990's privatizations.

H

H Halt, line State symbol (FDDI).

H_X High–speed bearer channel (ISDN).

H_0 384 kbit/s.

H_1 1.536 Mbit/s (N. Amer.) or 1.920 Mbit/s (CEPT areas).

H_{11} 1.536 Mbit/s (N. Amer.).

H_{12} 1.920 Mbit/s (CEPT areas).

H_2 DS–3 (N. Amer.) or 32.768 Mbit/s.

H_{21} 32.768 Mbit/s (CEPT).

H_{22} DS–3 (N. Amer.) (or 43 to 45 Mbit/s).

H_3 Would have been 60–70 Mbit/s but left undefined for lack of interest.

H_4 132.032 to 138.240 Mbit/s.

HCM High Capacity Multiplexing, 6 channels of 9600 in a DS–0.

HCS Header Check Sequence, CRC on header fields only, not on info; HEC (ATM).

HCV High Capacity Voice, 8 or 16 kbit/s scheme.

HDB3 High Density Bipolar 3–zeros, line coding for 2 Mbit/s lines replaces 4 zeros with BPV (CEPT).

HDLC High–level Data Link Control, layer–2 full–duplex protocol.

HDSL High bit–rate Digital Subscriber Line, proposal to T1E1 for way to duty T–1 over local loops without repeaters.

HDTV High Definition Television, double resolution TV image and candidate application for broadband networks.

HEC Header Error Control, ECC in ATM cell for header, not data. (See HCS)

HEL Header Extension Length, the number of 32–bit words in HE (802.6).

HIPPI High–speed Peripheral Parallel Interface, computer channel simplex interface clocked at 25 MHz; 800 Mbit/s when 32 bils wide, 1.6 Gbit/s when 64 bits.

HLM Heterogeneous LAN Management, OSI NMS protocol specification without layers 3–6, developed by IBM and 3Com to save memory in workstations.

HOB Head Of Bus, station and function that generates cells or slots on a bus (DQDB).

HOPS Horizontally Oriented protocol Structure, proposal for high performance interfaces at broadband rates.

HPR High Peformance Routing, a form of dynamic call routing in the PSTN.

HRC Hybrid Ring Control, TDM sublayer at bottom of data link (2) that splits FDDI into packet– and circuit switched parts.

HSSI High Speed Serial Interface, of 600 or 1200 Mbit/s.

HSPS High Speed Peripheral Shelf.

Hz Herz, cycles/second.

I

I I class central office switch is not in HPR network.

I Idle, line state symbol (FDDI).

I Information, type of layer 2 frame that carries user data.

IAB Internet Activities Board, defines LAN standards like SNMP.

IBR Intermediate bit Rate, between 64 and 1536 kbit/s; fractional T–1 rates.

IC Integrated Circuit.

ICCF Industry Carriers Compatibility Forum.

ICMP Internal Control Message protocol, reports to a host errors detected in a router by IP.

IDF Intermediate Distribution Frame.

Networking acronyms

idle Integrated Digital Loop Carrier, combination or RDT (remote MUX), transmission facility, and IDT to feed voice and data into a CO switch.

IDT Integrated Digital Terminal, M24 function in a CO switch to terminate a T–1 line from RDT.

IEC International Electrotechnical Commission, standards body.

IEEE Institute or Electrical and Electronics Engineers, Inc.: engineering society that sets standards.

I/F Interface.

IG ISDN Gateway (AT&T).

IGRP Interior Gateway Routing Protocol, learns best routes through LAN (TCP/IP).

ILS Idle Line State, presence of idle codes on optical fiber line (FDDI).

IMD InterModulation Distortion.

IMPDU Initial MAC PDU, the SDU received from LLC with additional header/trailer to aid in segmentation and reassembly (802.6).

IN Intelligent Network.

IND Indication (OSI).

INE Intelligent Network Element.

I/O Input/Output.

IR InfraRed, light with wave length longer than red like 1300 nm used over fiber.

ISDN Integrated Services Digital Network.

ISDN–UP ISDN User Part, protocol from layer 3 and up for signaling services for users Q.761–Q.766 (SS7).

ISDU Isochronous Service Data Unit, upper layer packet from TDM or circuit–switched service (802.6).

ISI Inter–Symbol Interference, source of errors where pulses (symbols) spread and overlap due to dispersion.

ISO International Standards Organization (International Organization for Standardization). ANSI is US member.

ISSI Inter–Switching System Interface, between nodes in a public network, not available to CPE (e.g. SMDS to B–ISDN).

ISSIP ISSI Protccol.

ISUP ISDN User Part.

ITB End of Intermediate Transmission Block, control byte in BSC.

IWF InterWorking Function, the conversation process between FR and X.25, etc.

IWWU InterWorking Unit, adapter between circuit– and packet–based switches; e.g., SMDS and SONET.

J

J Non–data character for starting delimiter (11000) in 4B/5B coding (802.6).

JB7 Jam Bit 7, force bits in position 7 within a DS–0 to 1 for 1's density.

K

K Non–data character for starting delimiter (10001) in 4B/5B coding (802.6).

kbit/s Thousands of bits per second

KG Key Generator (Krypto Gear), encryption equipment from NSA.

kHz Kilohertz, thousands of cycles per second.

L

L2–PDU Layer 2 Protocol Data Unit, fixed length cell (SMDS).

L3–PDU Layer 3 Protocol Data Unit, a variable length packet at OSI level 3.

LADT Local Area Data Transport, telco circuit on copper pair.

LAN Local Area Network.

LAP Link Access Procedure, layer 2 protocol for error correcting.

LAPB LAP Balanced, HDLC protocol for data sent into X.25 network, etc.

LAPD Varian~ or tAPB lor ISDN D channels.

LAPD+ LAPD protocol for other than D channels, e.g. B channels.

LAPM LAP Modem, part of V.42 modem standard.

LAT Local Area Transport, DECnet protocol for terminals.

LATA Local Access and Transport Area, a geographic region. The LEC can carry all traffic within a LATA, but nothing between LATA's.

LC Local Channel, the local loop.

LCI Logical Connection Identifier, short address in connection–oriented frame.

LCN Logical Channel Number, form of address in a packet.

LDM Limited Distance Modem.

LED Light Emitting Diode, semiconductor used as light source in FO transmitters.

LLB Local Loop Back.

LLC Logical Link Control, the upper sublayer of the OSI data link layer (layer 2).

LLC1 Connection oriented LLC. LLC2 Connectionless LLC.

LME Layer Management Entity, the process that controls configuration, etc. (802.6).

LMI Local Management Interface, transport specification for frame relay that sets way to assign DLCIs, etc.

LOF Loss Of Frame, condition where mux cannot find framing, OOF, for 2.5 sec.

LOFC Loss of Frame Count, number of LOFs.

LOP Loss of Pointer, SONET error condition.

LOS Loss Of Signal, incoming signal not present (no rceivcd data).

LPC Linear Predictive Coding, voice encoding technique.

LSAP Link layer Service Access Point, logical address of boundary between layer 3 and LLC sublayer in 2 (802).

LSB Least Significant Bit, position in byte with smallest value.

Networking acronyms

LSSU Link Status Signaling Unit, control packet at layer 3 (SS7).

LSU Line State Unknown, possible report from FDDI line state monitor.

LTE Line Terminating Equipment, SONET nodes that switch, CLC, and so create or take apart an SPE (SONET).

LU Logical Unit, upper level protocol in SNA.

LU6.2 Set of services that support program-to-program communications at levels 4–6.

M

M Million when used as prefix to abbreviation: Mbit/s.

m Milli (1/1000) when used as prefix: mm = millimeter

m Meter (39.37 inches)

M13 Multiplexer between DS–1 and DS–3 levels.

M24 Multiplexer function between 24 DS–O channels and a T–1, a channel bank.

M28 Same as M 13, but different format, not compatible.

M41 Multiplexer function to put 44 ADPCM channels into one T–1; four bundles, each of one common signaling channel with 11 voice channels; transcoder or BCM.

M48 Multiplexer function to put 48 ADPCM channels into one T–1; signaling in each voice channel.

M55 ADPCM multiplexer that puts SS voice channels in five bundles on an E–1.

MAC Medium (Media) Access Control, the lower sublayer of the OSI data link layer.

MAN Metropolitan Area Network, typically 100 M bi t/s.

MAP Manufacturing Automation Protocol, for LANs; closely related to TOP, and written MAP/TOP (802.4).

MAU Media Access Unit, device attached physically to cable (802.3 layer 1).

MAU Multiple (Multistation) Access Unit, hub device in a LAN (802.5).

Mbit/s Megabit (1,00,00 bits) per second.

MCF MAC Convergence Function, how an SDU is framed into a packet (PDU), segmented, and loaded into cells (802.6).

MCP MAC Convergence Protocol, segmentation and reassembly procedure to put MSDUs into cells (802.6).

MDDB Multi–Drop Data Bridging, digital bridging of PCM encoded modem signals, equivalent to analog bridging.

MDF Main Distribution Frame, large CO wire rack for low speed data and voice cross connects.

MDI Medium Dependent Interface, link between MAU and cable (802 layer 1).

MF Multi–Frequency, tone signaling on analog circuits.

MFA MultiFrame Alignment, code in time slot 16 of E–1 to mark start of superframe.

MHS Message Handling System, OSI store and forward protocol.

MHz Megahertz, million cycles per second.

MIB Management Information Base, OSI defined description of a network for management purposes (SNMP, IP).

MIC Media Interface Connector, dual–fiber equipment socket and cable plug FDDI).

MIS Management Information Systems, dept. that runs the big computers.

MNP Microcom Networking Protocol, error correction in modems.

modem MOdulate/DEModulate, modulate analog signal from digital data and reverse.

MPDU MAC PDU (802.6).

MPL Maximum Packet Lifetime, number of hops allowed before packet is discarded.

ms Millisecond, l/l000 second.

M/S Master/Slave, relationship in a protocol where master always issues commands and slave only responds.

MSAP MAC Service Access Point, logical address (up to 60 bits) of boundary between MAC and LLC sublayers (802).

MSDU MAC Service Data Unit, data packet in LAN format; may be long and variable length before segmentation into cells.

MSS MAN Switching System.

MTBF Mean Time Between Failures, average for one device.

MTS Message Toll Service, normal dial up phone service.

MUX Multiplexer.

N

n Nano, prefix meaning 10^{-9} of the unit as nln = 10^{-9} meter.

NAK Negative Acknowledgment, protocol control byte indicating error.

NAS Network Applications Solutions, set of DEC APIs for communication.

NAU Network Addressable Unit, device or process running an SNA protocol stack.

NCB Network Control Block, command packet in SNMP.

NCB Network Control Block, transport protocol in LAN Manager (level 4).

NCC Network Control Center.

NCI Network Control Interface.

NCP Network Control Point, for SDN and AT&T switched network.

NCTE Network Channel Terminating Equipment; first device at CP end of local loop; e.g., CSU.

NDF New Data Flag, inversion of some pointer bits to indicate change in SPE position in STS frame (SONET).

NE Network Element

NEBS Network Equipment–Building Standards, Bellcore generic spec for CO equipment (TR63).

NEXT Near End Cross Talk, interference on 2–wire interfaces from sent signals leaking back into the receiver.

Networking acronyms

NFS Network File System, protocol for file transfers on a LAN.

NFS Network File Server, computer with shared storage, on a LAN.

NI Network Interface; demarcation point between PSTN and CPE.

NIC Network Interface Card, add–in card for PC, etc. to connect to LAN.

NID Network IDentification, field in network level header (MAP).

NISDN Narrowband ISDN, access at T-1 or less.

NM Network Management.

NME NM Element.

NMOS N–channel Metal Oxide Semiconductor, common IC type uses more power than CMOS.

NMP Network Management Protocol.

NMS Network Management System.

NNI Network–Node Interface, point-to-point interface between two switches for SDH, SONET, or B–ISDN network.

NPDU Network PDU, Layer 3 packet (OSI).

NR Number Received, control field sequence, tells sender the N_S that receiver expects in next frame (Layer 2).

NRZ Non–Return to Zero, signal transitions from positive to negative without assuming 0 value. See also DMC, AMI.

NRZI NRZ Invert on ones, coding changes polarity to indicate 'I' and remains unchanged for '0.'

ns Nanosecond, 10^{-9} second.

NS Number Sent, sequence number of frame in its control field; determined by sender.

NSA Non–Service Affecting, fault that does not interrupt transmission.

NSAP Network Service Access Point,

NSC Network Service Center, for SDN.

NT–1 Network Termination 1, the first device on the CP end of the local loop (like the CSU).

NT–2 Network Termination 2, the second CP device, like the DSU (TSDN).

NTN Network Terminal Number, address of terminal on data network, part of global address with DMC (X.121).

NTSC National Television Standards Committee, group and format they defined for U.S. TV broadcasting.

NUI Network/User Interface.

O

OA&M Operations, Administration, and Maintenance.

OAM&P Operations, Administration, Maintenance, & Provisioning, telco housekeeping.

OC–1 Optical Carrier level I, SONET rate of 51.84 Mbit/s, matches STS–1.

OC–3 Optical Carrier level 3, SONET rate of 155.52 Mbit/s, matches STS–3.

OC–N Higher SONET levels, N times 51.84 Mbit/s.

OCU Office Channel Unit, "CSU" in the CO; also called OCR.

OCU–DP OCu–Data Port, channel bank plug I/0 to 4– wire local loop and CSU on CP.

OF Optical Fiber.

OLTP On Line Transaction Processing.

ONA Open Network Architecture, FCC plan for equal access to public networks.

ONI Operator Number Identification.

OOF Out Of Frame, mux is searching for framing bit pattern.

OOS Out Of Synchronization; multiplexers can't transmit data when OOS.

OPR Optical power received, by a FO termination.

ORL Optical Return Loss.

OS Operating System, main software to run a CPU.

OSI Open Systems Interconnection, a 7–layer model for protocols defined by the ISO.

OSI/NMF OSI Network Management Forum, standards group for NM protocols.

OSIone Global organization to promote OSI standards.

OSI TP OSI Transaction Processing, a protocol.

OTDR Optical Time Domain Reflectometry (Reflectometer), method (tester) to locate breaks in OF.

OW Order Wire, DS–0 in overhead intended for voice path to support maintenance.

P

PA Preamble, a period of usually steady signal ahead of a LAN frame, to set timing, reserve the cable, etc.

PA Pre–Arbitrated, portion of traffic on DQDB MAN with assigned bandwidth, usually isochronous connections (802.6).

PABX Private Automated Branch eXchange, electronic PBX.

PAD Packet Assembler/Disassembler, device to convert between packets (X.25, etc.) and sync or async data.

PAL Programmable Array Logic, large semi–custom chip.

PAM Pulse Amplitude Modulation; used within older channel banks.

PARIS Packetized Automated Routing Integrated System, fast switch developed by IBM.

PBX Private Branch eXchange, small phone switch inside a company, manual or automatic.

PC Path Control, level 3 in SNA for network routing.

PCM Pulse Code Modulation, the standard digital voice format at 64kbit/s.

PCN Personal Communications Network, second generation cellular system.

PCR Preventive Cyclic Retransmission, error correction procedure that repeats packets whenever link bandwidth is available (SS7).

PDG Packet Data Group, 12 octets in FDDI frame (outside of WBCs) not assignable to circuit–switched connections.

PDH Pleisiochronous Digital Hierarchy, present multiplexing scheme from T-1 to T–3 and higher, contrast with SDH.

Networking acronyms

PDN Public Data Network; usually packetized.

PDS Premises Distribution System, the voice and data wiring inside a customer office.

PDU Protocol Data Unit, information packet (ADDR, CTRL, INFO) passed at one level between protocol stacks (OSI).

pel Picture Element, the smallest portion of a graphic image encoded digitally.

P/F Poll/Final, bit in control field of LLC frames to indicate receiver must acknowledge (P) or this is last frame (F) (Layer 2).

PHY PHYsical, layer 1 of the OSI model.

PI Primary In, FO port that receives light from main fiber ring (FDDI).

PIN Positive–Intrinsic–Negative, type of semiconductor photo detector.

PL Pad Length, number (0–3) of octets of 0s added to make Info field a multiple of 4 octets (802.6)

PL Physical Layer, level 1 in OSI model.

PL Private Line, a dedicated leased line, not switched.

PL Performance Loop Back, LB done at point of ESF performance function in CPE.

PLCP Physical Layer Convergence Protocol (Procedure), part of PHY that adapts transmission medium to handle a given protocol sublayer (DQDB).

PLL Phase Locked Loop, electronic circuit that recovers clock timing from data.

PLP Packet Layer Protocol, at Layer 3 like X.25.

PLS Physical Link Signaling, part of layer 1 that encodes and decodes transmissions, e.g. Manchester coding (IEEE 802).

PMA Physical Medium Attachment, electrical driver for specific LAN cable in MAU, separated from PLS by AUI (802.3).

PMD Physical Layer, Medium Dependent, a sublayer in layer 1 (below PLS) of LAN protocols; also PMA (802).

PO Primary Out, FO port that sends light into the main fiber ring (FDDI).

POF Plastic Optical Fiber, for short distances rather than glass for long haul.

POH Path OverHead, bytes in SDH for channels carried between switches over multiple lines and through DCCs.

POP Point Of Presence; end of IXC portion of long–distance line at central office (Tel).

POS Point of Sale.

POTS Plain Old Telephone Service, residential type service.

PPDU Presentation (Layer) PDU (OSI).

ppm Parts Per Million.

PPP Point-to-Point Protocol, non–proprietary interface on routers for WAN links.

pps Pulses Per Second, speed of rotary dialing dial pulses.

PRC Primary Reference Clock, GPS–controlled rubidium oscillator used as stratum 1 source.

PRA Primary Rate Access, via PRI for ISDN.

PRBS PseudoRandom Bit Sequence, fixed bit pattern, for testing, that looks random.

PRI Primary Rate Interface; 23B+D (T–1) or 30B+D (CEPT).

PRS Primary Rate Source, stratum 1 clock.

PSI Primary Subnet Identifier, part of address in network level header (MAP).

PSN Packet Switched Network.

PSPDN Packet Switched Public Data Network.

PSTN Public Switched Telephone Network, the telco–owned dial–up network.

PTE Path Terminating Equipment, SONET nodes on ends of logical connections.

PTAT Private Trans–Atlantic Telephone, cable from US to U.K., Ireland, and Bermuda.

PUB AT&T Technical PUBlication, Bell System de facto standard.

PUC Public Utilities Commission, state body that regulates telephones, also PSC.

PVC Permanent Virtual Circuit, assigned connection over a packet/frame network, not switchable by user.

Q

Q Quiet, line state symbol (FDDI).

QA Queued Arbitrated, portion of packet traffic that contends for bandwidth (DQDB).

QOS Quality of Service.

QPSX Queued packet Synchronous eXchange, old name for DQDB; QPSX Systems Inc. originated it in Australia.

Q.921 CCITT recommendation for level 2 protocol in signaling system 7.

Q.931 CCITT recommendation for level 3 protocol in signaling system 7.

R

R Interface reference point in the ISDN model to pre–ISDN phones and terminals.

R Ring, one of the conductors in a standard twisted pair, 2–wire local loop (the one connected to the 'ring', the second part of a phone plug) or the DTE–to–DCE side of a 4–wire interface.

R1 Ring, or R lead of the DCE–to–DTE pair in a 4–wire interface.

RACE Research for Advanced Communications in Europe, program to develop broadband.

RAI Remote Alarm Indication.

RARP Reverse ARP, Internet protocol to let diskless workstation learn its IP address from a server (TCP/IP).

RBOC Regional Bell Operating Company, one of about 22 local telephone companies formerly part of Bell System.

RBS Robbed Bit Signaling, in PCM.

RD Receive Data, lead on electrical interface.

Networking acronyms

RD Request Disconnect, secondary station unnumbered frame asking primary station for DISC (Layer 2).

RDA Remote Database Access, service element (OSI).

REJ Reject, S-format LLC frame acknowledges received data units while requesting retransmission from specific errored frame (Layer 2).

RELP Residually-Excited Linear Predictive Coding, voice encoding scheme (8–16kBit/s).

REQ Request (OSI).

RF Radio Frequency.

RFI Radio Frequency Interference.

RFT Remote Fiber Terminal, equivalent to SLC96.

RI Ring Indicator, digital lead on modem tells DTE when call comes in.

RI Routing Indicator, bit in LAN packet header to distinguish transparent- from source-routed packets.

RIM Request Initialization Mode, Layer 2 supervisory frame.

RIP Routing Information Protocol, method for LANs to learn topology (TCP/IP).

RISC Reduced Instruction Set Computer.

RJ Registered Jack, connector for UNI; RJ1 1 is standard phone, RJ48 for T–1.

RJE Remote Job Entry, one form of BSC.

RL Ring Latency, time for empty token to traverse full ring with no load (FDDI).

RMN Remote Multiplexing Node.

RO Receive Only.

ROSE Remote Operation Service Element (OSI).

RNR Receiver Not Ready, S–format LLC frame acknowledges received data units but stops sender temporarily (Layer 2).

RR Receive Ready, S–format LLC frame acknowledges received data units and shows ability to receive more (Layer 2).

RSET Reset, Layer 2 supervisory frame to zero counters.

RSL Request and Status Link, same as PHI or SCAI.

RSP Response (OSI).

RTS Request To Send; lead on terminal interface.

RVI Reverse Interrupt, positive ACK that lets station take control of a BSC line.

RZ Return to Zero; signal pauses at zero voltage between each pulse, when making zero crossings.

S

S Status, signaling bit in CMI.

S ISDN interface point between TA and NT–2.

S Supervisory frame, commands at LLC level: RR, RNR, REJ, SREJ (Layer 2).

SA Source Address, field in frame header (802).

SA Synchronous Allocation, time allocated to FDDI station for sending sync frames (802.6).

SAA Systems Application Architecture, compatibility scheme for communications among IBM computers.

SABM Sel Asynchronous Balanced Mode, connection request between HDLC controllers or LLC entities (Layer 2).

SABME SABM Extended, uses optional 16–bit control fields.

SAFER Split Access Flexible Egress Routing, service at one site from two toll offices over separate T–1 loops (AT&T).

SAP Service Access Point, logical address of a session within a physical station, part of a header address at an interface between sublayers (802).

SAPI SAP Identifier, address between layers in protocol stack; e.g., subfield in first octet of LAP–D address.

SAR Segmentation And Reassembly, protocol layer that divides packets into cells.

SAR–PDU SAR Protocol Data Unit, segment of CS–PDU with additional header and possibly a trailer (e.g., a cell in ATM).

SARM Sel Asynchronous Response Mode, unnumbered frame connection request (Layer 2).

SARME SARM Extended, uses optional 16–bit control field.

SAS Single–Attached Station, FDDI node linked to network by 2 optical fibers (vs. DAS).

SB Signal Battery, second lead to balance M lead in E&M Circuit.

SCAI Switch–to–Computer Applications Interface, link between host CPU and voice switch to integrate applications; also PHI and RSL.

SCP Service Control Point, CPU linked to SS7 that supports carrier services (800, ANI).

SD Staging Delimiter, unique symbol to mark start of LAN frame (JK in FDDI, HDLC flag, etc.).

S/D Signal-to-Distortion ratio.

SDDN Software Defined Data network, virtual private network built on public data net.

SDH Synchronous Digital Hierarchy, digital multiplexing plan where all levels are synched to same master clock.

SDLC Synchronous Data Link Control; a half–duplex IBM protocol based on HDLC.

SDM Subrate Digital Multiplexing, a DDS service to put multiple low–speed channels in a DS–0.

SDN Software Defined Network.

SDS Switched Digital Service, generic term for carrier function.

SDU Service Data Unit, information packet or segment passed vertically between adjacent layers in a protocol stack.

SFND Clear to Send, signaling bit in CMI.

SES Severely Errored Second, interval when BER exceeds 10^{-3}, >319 CRC errors in ESF, frame slip, or alarm is present.

SF Single Frequency; form of on/off–hook signaling within telcos.

SF Super frame, 12 T-1 frames.

SFET Synchronous Frequency Encoding Technique, a way to send precise isoc clocking rate as a delta from system clock.

Networking acronyms

SG Signal Ground, second lead to balance E lead in E&M signal circuit.

SHR Self–Healing Ring, topology can survive one failure in line or node (802.6, etc.).

SI Sequenced Information, LAP–D frame type.

SI Secondary In, FO port that receives light from secondary fiber ring (FDDI).

SIM Set Initialization Mode, Layer 2 supervisory frame.

SIR Sustained Information Rate, average throughput; basis for SMDS access class.

SIT Special Information Tone, audible signal (often three rising notes) preceding an announcement by the network to a caller.

SIP SMDS Interface Protocol.

SIVR Speaker Independent Voice Recognition.

SLC Subscriber Loop Carrier, usually digital loop system.

SLIC Subscriber Line Interface Card (circuit), on a switch.

SMB Server Message Block, a LAN client–server protocol.

SMDR Station Message Detail Recording, keeping list of all calls from each phone, usually by PBX or computer.

SMDS Switched Multi–megabit Digital Service, offered on a MAN by a carrier; service mark of Bellcore.

SMF Single Mode Fiber, thin strand that supports only one transmission mode for low dispersion of optical waves.

SMT Station ManagemenT, NMS for FDDI.

SMTP Simple Mail Transfer Protocol (TCP/IP).

S/MUX Workstation software to allow UNIX daemons to talk to SNMP manager station.

SNA SDH Network Aspects, evolving standards for VC payloads and network management (SDH).

SNA Systems Network Architecture, IBM's data communication scheme.

SNADS SNA Distribution Services, communication architecture for electronic mail and other applications.

SNAP Sub–Network Access Protocol (802.1).

SNI Subscriber–Network Interface, the demark point.

SNMP Simple Network Management protocol, started in TCP/IP, but extending to many LAN devices (Layer 4–5).

SNR Signal-to-Noise Ratio, in dB.

SNRM Set Normal Response Mode, unnumbered command frame (Layer 2).

SNRME SNRM Extended, uses optional 16–bit control field.

SO Secondary Out, FO port that sends light into the secondary fiber ring (FDDI).

SO Serving Office, central office where IXC has POP.

SOH Section OverHead, bytes in SDH for channels carried through repeaters between line terminations like DCC or switch.

SOH Start of Header, control byte in BSC.

SONET Synchronous Optical Network.

SPAC Standards Promotion and Applications Group, has same function as COS.

SPCS Stored Program Controlled switch, CO switch (analog or digital) controlled by a computer.

SPDU Session (Layer) PDU (OSI).

SPF Synchronous Payload Envelope, data area in SONET/STS/SDH format, with POH.

SPF Shortest Path First, LAN router protocol that minimizes some measure (delay) and not just "hops" between nodes.

SREJ Selective REJ, Layer 2 frame that requests retransmission of one specific I frame.

SRL Singing Return Loss.

SRT Source Routing Transparent, variation of source routing combined with spanning tree algorithm for bridging (802).

SS7 Signaling System 7, to replace CCIS in ISDN.

SSA Systems Applications Architecture, SNA plan to allow programs on different computers to communicate.

SSAP Source Service Access Point, field in LLC frame header to identify the sending session within a physical station (802).

SSCP System Services Control Point, host software that controls SNA network.

SSM Single Segment Message, frame short enough to be carried in one cell.

ST Stream, network layer protocol for very high speed connections.

STDM Statistical Time Division Multiplexer.

STE Section Terminating Equipment, SONET repealer.

STM Synchronous Transfer Mode, one of several possible formats for SONET and BISDN.

STM–1 Synchronous Transport Module–1, smallest SDH bandwidth; = 155.52 Mbit/s, STM–n = n x 155.52 Mbit/s.

STP Shielded Twisted Pair, telephone cable with additional shielding for high speed data and LANs.

STP Signal Transfer Point, packet switch for SS7.

STS–1 Synchronous Transport Signal, level I; electrical equivalent of OC– 1, 51.84 Mbit/s.

STS–N Signal in STS format at N x 51.84 Mbit/s.

STSX–n Interface for cross–connect of STS–n signal that defines STS–n.

STX Start of Text, control byte in BSC.

SV Subvector, part of NMVT (SNA).

SVC Switched Virtual Circuit, temporary logical connection in a packet/frame network.

SWIFT Switched Fractional T–1, telco service defined by Bellcore, includes full T–1.

SW56 Switched 56 kilobit/s, digital dial up service.

SYN Synchronization character, 16h ASCII.

sync Synchronous.

SYNTRAN Synchronous Transmission, byte aligned format for an electrical DS–3 interface.

T

T Interface between NT–1 and NT–2 (ISDN).

Networking acronyms

T Non–data character in 4B/5B coding, ending delimiter (802.6).

T Tip, one of the conductors in a standard twisted pair, 2–wire local loop (the wire connected to the 'tip' of a phone plug) or one of the DTE–to–DCE pair or a 4–wire interface.

T–1 Transmission at DS–1, 1.544 Mbit/s.

T1 Tip or T lead of the DCE–to–DTE pair in a 4–wire interface.

T1DM T–1 Data Multiplexer, brings DS–OBs together on a DS–1 (Tel).

T1D1 TSC of T1 for BRI U interface.

T1E1 TSC or T1 for SNI.

T1M1 TSC or T1 for NMS and OSS.

T1Q1 TSC of T1 for ADPCM, voice compression, etc.

T1S1 TSC of T1 for ISDN bearer services.

T1X1 TSC of T1 for SONET and SS7.

TA Terminal Adapter, matches ISDN formats to existing interfaces like V.35, RS–232.

TABS Telemetry Asynchronous Block Serial, M/S packet protocol used to control network elements and get ESF stats.

TAPS Test and Acceptance Procedures, telco document for equipment instalation and set up.

TASI Time Assigned Speech Interpolation; analog voice compression comparable to DSI and statistical multiplexing of data.

TAT Trans–Atlantic Telephone, applied to cables, as TAT–8.

TBD To Be Determined, appears often in unfinished technical standards.

TC Terminating Channel; local loop.

TC Transport Connection.

TC Transmission Control, Level 4 in SNA.

TC Trunk Conditioning, insertion of various signaling bits in A and B positions of DS–0 during carrier failure alarm condition.

TCA TeleCommunications Association.

TCA Threshold Crossing Alert, alarm that a monitored statistic has exceeded preset value.

TCP/IP Transmission Control Protocol (connection oriented with error correction) of ten runs on Internet Protocol (a connectionless datagram service).

TD Transmit Data.

TDD Telecom Device for the Deaf, Teletype machine or terminal with modem for dial–up access.

TDM Time Division Multiplexing (or multiplexer).

TDMA Time Division Multiple Access, stations take turns sending in bursts, via satellite or LAN.

TDS Terrestrial Digital Service, MCI's T–1 and DS–3 service.

TE Terminal Equipment, supports native ISDN or B–ISDN formats without a TA.

TEI Terminal Endpoint Identifier, subfield in second octet of LAP–D address field.

TEST Test command, LLC UI frame to create loopback (Layer 2).

TH Transmission Header, 2 bytes in framing format for layer 4 protocol (SNA).

TLI Transport Level Interface, for UNIX.

TL1 Transaction Language 1, to control network elements (TR482); CCITT's form of MML.

TLP Transmission Level Point related to gain (or loss) in voice channel; measured power – TLP at that point = power at 0 TLP site.

TMN Telecommunications Management Network, a support network to run a SONET network.

TMS Timing Monitoring System.

TO Transmit Only; audio plug for a channel bank without signaling.

TOP Technical and Office Protocol; for LAN's.

TOPS Task Oriented Procedures, telco document for equipment operation and maintenance.

TOS Type Of Service, connection attribute used to select route in LAN (SPF).

TP Transaction Processing, work of a terminal on–line with a host computer.

TPEX Twisted Pair Ethernet Transceiver.

TP–N Transport Protocol of Class N (N = 0 to 4), OSI layer 4.

TP–0 Connectionless TP (ISO 8602).

TP–4 Connection oriented TP (ISO 8073).

TPDU Transport Protocol Data Unit (OSI).

TPF Transaction Processing Facility, IBM host software for OLTP.

TPSE Transport Processing Service Element (OSI).

TR Technical Reference, a final Bellcore standard.

TR Token Ring, a form of LAN.

TS Transport Service (OSI).

TSDU Transport Service Data Unit (OSI).

TSI Time Slot Interchange; method of temporarily storing data bytes so they can be sent in a different order than received; a way to switch voice or data.

TTC Telecommunications Technology Committee, Japanese standards body.

TTR Timed Token Rotation, type of token passing protocol (FDDI).

TTRT Target Token–Rotation Time, expected or allowed period for token to circulate once around ring (802.4, 802.6).

TTY Teletypewriter.

TU Tributary Unit, virtual container plus path overhead (SDH).

TUG TU Group, one or more TUs multiplexed into a larger VC (SDH).

TWX TeletypeWriter Exchange, switched service (originally Western Union) separate from Telex.

Networking acronyms

U

u English transliteration of Greek mu ( ), for micro or millionth; prefix in appreviation of units like us, um.

U Interface between CO and CP for ISDN.

U Unnumbered format, command frames, same as UI (Layer 2).

UA Unnumbered Acknowledgement, LLC frame to accept connection request (Layer 2).

UART Universal Async Receiver Transmitter, interface chip for serial async port.

UAS Unavailable Second, when BER of line has exceeded 10^{-3} for 10 consecutive seconds until next AVS start.

UDLC Universal Data Link Control, Sperry Univac's HDLC.

UDP/IP Universal Data Protocol or User Datagram Protocol, Internal protocol.

uF Microfarad, one millionth of the unit of capacitance.

UI Unnumbered Information, frame at LLC level whose control field begins with 11: XID, TEST, SABME, UA, DM, DISC, FRMR (802).

ULP Upper Layer Protocol.

UNI User–Network Interface, demark point or SDH and B–ISDN at customer premises.

UNR Uncontrolled Not Ready, signaling bit in CMI.

UP Unnumbered Poll, command frame (Layer 2).

U–Plane User Plane, bearer circuit for customer information, controlled by C–Plane.

UPS Uninterruptable Power Supply.

us Microsecond; 10^{-6} second.

USART Universal Sync/Async Receiver Transmitter, interface chip for sync and async data I/O.

USAT Ultra–Small Aperture SATellite; uses ground station antenna less than 1m diameter.

USOC Universal Service Order Code.

V

VAN Value Added Network; generally a packet switched network with access to data bases, protocol conversion, CIC.

VBR Variable Bit Rate, packetized bandwidth on demand, not dedicated (ATM).

VC Virtual Container, a cell of bytes carrying a slower channel to define a path in SDH; VC–n corresponds to DS–n, n = 1 to 4.

VC Virtual Circuit, logical connection in packet network so net can transfer data between two ports.

VCC Virtual Channel Connection (SMDS).

VCI Virtual Circuit (or Channel) Identifier, part of a packet/frame address header (X02.6, ATM).

VCX Virtual Channel Cross–connect, device to switch ATM cells on logical connections.

VDT Video Display Terminal, often applied to any type of "tube" or PC.

VF Voice Frequency, 300–3300 Hz.

VG Voice Grade; related to the common analog phone line.

VGPL Voice Grade Private Line, an analog line.

VHF Very High Frequency, radio band from 30 to 300 MHz.

VMTP Versatile Message Transport Protocol, designed at Stanford to replace TCP and TP4 in high–speed networks.

VNL Via Net Loss, related to TLP.

VPI Virtual Path Identifier, VCI in ETSI version or ATM.

VQC Vector Quantizing Code; a voice compression technique that runs at 32 and 16 kbit/s.

VQL Variable Quantizing Level; voice encoding method.

VR Receive state Variable, value in register at receiver indicating next NS expected (Layer 2).

VS Send state Variable, value in register or sender of Ns in last frame sent (Layer 2).

VSAT Very Small Aperture Terminal, satellite dish under 1m.

VT Virtual Tributary, logical channel made up of a sequence of cells within SONET or similar facility.

VTAM Virtual Telecommunications Access Method, SNA protocol and host program.

VTE Virtual Tributary Envelope, the real payload plus path overhead within a VT (SONET).

VTNS Virtual Telecommunications Network Service.

V35 Former CCITT recommendation for a modem with a 48 kbit/s interface, being replaced by TIA–530A.

W

WACK Wait before transmit positive Acknowledgment, control sequence or DLE plus second character (30 ASCII, 6B EBCDIC).

WAN Wide Area Network, the T–1, T–3, or broadband backbone that covers a large geographical area.

WATS Wide Area Telephone Service.

WBC WideBand Channel, one or 16 FDDI subframes of 6.144 Mbit/s assignable to packet or circuit connections.

W–DCS Wideband Digital Cross–connect System, 3/1 DACS for OC–1, STS–1, DS–3, and below, including T–1 (see B–DCS).

WDM Wavelength Division Multiplexing, 2 or more colors of light on 1 fiber.

X

X X class central office switch is in HPR net but not linked to NP.

X.25 CCITT recommendation defining Level 3 protocol to access a packet switched network.

XID Exchange Identification, type of UI command to set up exchange parameters between LLC entities (Layer 2).

XNS Xerox Network Services, a LAN protocol slack.

Networking acronyms

X–off Transmit Off, ASCII character from receiver to stop sender.

X–on Transmit On, ok to resume sending.

XTP eXpress Transfer Protocol, a simplified low–processing protocol proposed for broadband network.

Y

Y Yellow alarm control bit in sync byte (TS 24) of T1DM, Y=O indicates alarm.

Z

Z Impedance, nominal 600 ohm analog interface may be closer to complex value of 900 R + 2 uF C.

ZBTSI Zero Byte Time Slot Interchange, process to maintain 1's density.

Understand datacom protocols by examining their structures

Authors: Alex Goldberger and Stephen Y. Lau

Although you'll probably never design a datacom protocol, you'll often need to interface to a particular protocol environment. And you can better select among the many silicon implementations becoming available if you know protocol basics.

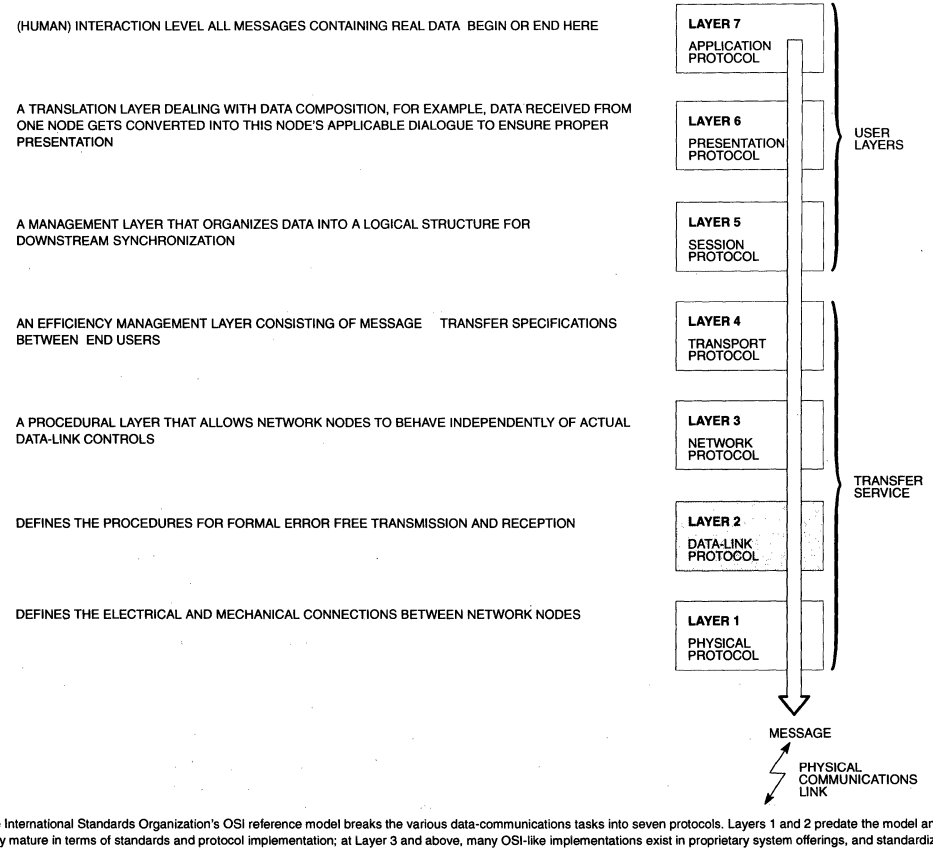
INTRODUCTION

As technical and market factors make your product's data communications capability more important, meeting the requirements of the datacom protocol dictated by the application environment becomes vital. Unfortunately, the wide variety of protocols and their subtle differences complicate the design task. But by understanding the tradeoffs involved in working with various protocols, you can design a product for many years of service in a variety of network environments. And the key to that flexibility lies in implementing a protocol that's now in wide use and likely to remain widely used, or at least compatible with future protocols. Further, becoming familiar with these protocols is the first step in intelligently selecting among the many IC-level implementations becoming available.

What is a protocol?

In the most general terms, a protocol is a formal set of conventions governing the format and relative timing of message exchange between two communications terminals. When dealing with protocols, though, most datacom engineers tend to think in terms of the 7-layer Open System Interconnection (OSI) reference model developed by the International Standards Organization (Figure 1). This widely (if academically) accepted architecture provides a framework in which you can define every aspect of data communications.

The model's first protocol, Layer 1, underwrites electrical and mechanical conventions such as connector format and signal/pin assignments. Familiar standards such as EIA's RS-232C, RS-442 and RS-449 as well as CCITT's V.24 and X.21 are Level 1 protocols. Layer 2 — the area in which datacom engineers get most involved and the focus of this article — defines procedures for error-free transmission and reception.



The International Standards Organization's OSI reference model breaks the various data-communications tasks into seven protocols. Layers 1 and 2 predate the model and are fairly mature in terms of standards and protocol implementation; at Layer 3 and above, many OSI-like implementations exist in proprietary system offerings, and standardization efforts are underway. Layer 2 protocols, the focus of this article precisely define the format of message transmissions and provide error-detection/recovery mechanisms.

Figure 1. Theoretically Describing Any Datacom Link

Understand datacom protocols by examining their structures

Layers 3 and 4 add standards for message transport, and the three highest layers define the procedures for human interaction with overall network services.

DLCs define transmission methods and detect and correct errors

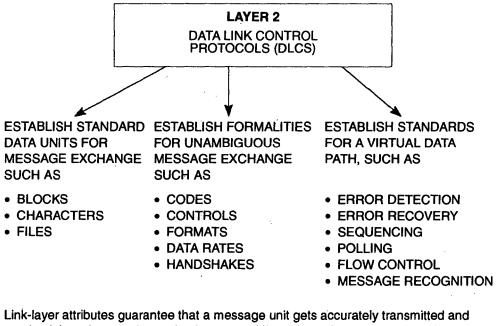
Layers 1 through 4 are designated the transfer service because they move
messages from one point to another; layers 5 through 7 are known as the user layers because they provide user access to messages on the network.

From a design standpoint, the vast majority of work in both hardware and software implementations focuses on Layers 1 and 2. Above the link layer (Layer 2), implementations abound in the form of proprietary offerings from competing firms; the electronics industry is seeking a consensus on exactly what the corresponding standards and protocols should be.

Specifics of link-layer protocols

Although still undergoing development, Layer 2 protocols, also known as link-layer
protocols or data-link controls (DLCs) are relatively well defined by function and type. In terms of function, several aspects define a DLC. First, a DLC is a formal ritual for communications; it is the precise definition of message transmission and acknowledgement between computers and their peripherals for every message transfer. Although not the communicated data itself, every link-layer protocol facilitates communications by embodying a structure for transport of information from one point to another.

In addition, a clearly defined method for data transfer among computers and peripherals must accommodate coding and transmission errors even under the best circumstances. Besides the error sources that a busy



Link-layer attributes guarantee that a message unit gets accurately transmitted and received; how these tasks are implemented differentiates the various data-link controls.

Figure 2. Link Layer Attributes

datacom link might suffer because of a low signal-to-noise ratio, receiving stations might be engaged in other tasks when a message gets sent. Thus, the second major characteristic of a DLC is the ability to detect and recover from mistakes and complete the communication process.

Figure 2 details other important link-layer-protocol attributes. All DLCs embody all or some of these features, whether implemented in hardware or software. In fact, variations of these features define the various link-layer protocols.

Thus, as a family of protocols, DLCs share many common features but also accommodate a wide variety of performance characteristics that require full understanding for correct DLC selection. For instance, it is not unusual for networks to use both synchronous and asynchronous transmission and wide variations in data rates. Datacom-equipment designers must carefully evaluate the choices to ensure correct positioning of their products in the marketplace.

To see how link-layer protocols fit into a typical datacom scheme, examine Figure 3. In this system, a terminal user wants access to an applications program that is physically located some distance away. Between the terminal and host computer that stores the desired program is a complex network of modems, transmission facilities and protocol-conversion devices. Each communications layer at the terminal end has an equivalent layer at the host-computer end. Thus, the modems "talk" only to each other, ignoring the actual meaning of the data they handle. Likewise, the data-link controls interact as peers to assure the successful transmission and reception of data without regard for the modems' modulation scheme.

This peer-to-peer communication, when combined with the structure of the OSI model, leads to the concept of enveloping. As the user data generated in Layer 7 moves down the model, the protocol associated with each layer adds control information. By the time the user data reaches the physical link layer (Layer 1), it has been successively enveloped several times. Following transmission across the data link, the enveloped data moves up the model. At each layer, the peer-level envelope of control information gets stripped off for evaluation and action by its peer protocol.

Datacom messages don't necessarily contain user data, though. Messages such as polling or acknowledgement — where a computer grants permission for a terminal to send a message, or where any receiver sends a short message ACKing or NAKing another message — can originate and terminate at Layer 2 with higher layers none the wiser.

For the system designer, an end-to-end view builds a virtual communications path through a network. Because you cannot always predict the various network environments in which a product will see use, you should concentrate your design effort on the data-link interface, thereby allowing for the use of any higher level protocols. Your goal, of course, is to control data transmission and reception by synchronizing sender and receiver and to detect errors and provide successful recovery techniques. A subordinate but no less important objective is to minimize overhead so that datacom efficiency remains high and costs remain low.

The DLCs at your disposal for this job can be classified according to several criteria, such as error-handling capability, message format, method of communication-line control and flow-control procedure. The implementation of any DLC requires knowledge of all these criteria because enough variation exists to mandate complete specification by the engineer. In other words, every data-link-control protocol is itself a procedure that offers several modes of operation depending on the aforementioned options.

Sync vs async transmission

Before selecting a DLC, you should first determine if your application requires synchronous or asynchronous operation because this aspect can limit DLC options. Furthermore, other technical issues are involved in the sync/async decision.

The prime distinction between sync and async operation lies in the time domain In async, the time interval between transmissions is variable. Control bits, which designate message start and stop, frame each character; asynchronous characters vary in length

Understand datacom protocols by examining their structures

depending on the information code (e.g., ASCII, EBC-DIC or IBM's 6-bit Transcode) and are usually 5- to 8-bits long. On the other hand, sync transmission proceeds without character-by-character framing once synchronization is achieved; there are no intervening control bits for start/stop.

Because of its inherent simplicity and historical momentum (async transmission methods were introduced years before sync methods), async transmission is now used in perhaps millions of terminals, primarily where low-speed communication (less than 1800bps) is sufficient. Async's prime disadvantage is its control overhead, which can reach three control bits for five data bits or 37%. In contrast, fully synchronous transmissions typically have less than 2% overhead and suit multiplexing. This high efficiency also allows synchronous data rates over voice-grade lines as high as 9.6kbps.

By comparing transmission data structures, you can see why async (with its inherent idle times) suits man/machine interfaces while continuously flowing sync offers the high speed needed in machine-to-machine interfaces. Thus, character-mode CRT terminals generally employ async transmissions to keep costs low. On the other hand, the trend in intelligent terminals, which pre-process data and then transmit it to a host in blocks, is toward sync transmissions.

Some equipment might provide both means. For example, a cluster controller, which interfaces a CPU to a group of terminals, can use async mode for the terminal ports while communicating with the host over a synchronous link.

By themselves, synchronous and asynchronous formats are not protocols. Rather, they are transmission methods that place performance restrictions on a communications channel to ensure data integrity. DLCs that use sync or async transmission mirror these performance restrictions and act as policemen to assure that messages are correctly transferred independently of the transmission methods employed.

Sync and async transmissions are closely related to the two main classifications of link-layer protocols: character-oriented protocols (COPs) and bit-oriented protocols (BOPs). Async mode, with its character-by-character framing, does not lend itself to BOPs, which inherently lack character framing in their information fields and thus required COP; sync transmission, in contrast, can use either a COP or BOP.

Despite this fact, BOPs and COPs are not direct competitors for datacom applications. One well-established rule of modern datacom engineering is that bit orientation is synonymous with high-speed operation. However, a great deal of installed datacom equipment requires relatively slow speeds; thus, the DLC decision in the applications environment rests with other factors contained in the definitions of BOPs and COPs.

For most applications, you will likely deal with one of the several widely used BOPs or COPs. Examining the BOPs first, note that they are all variations of the International Standards Organization's High Level Data Link Control (HDLC). The US version, sponsored by the American National Standards Institute (ANSI), is designated the Advanced Data Communications Control Procedure (ADCCP). Perhaps the most popular version of HDLC is IBM's Synchronous Data Link Control (SDLC), but a variation becoming more widely used is the Link Access Procedure B (LAPB), a host-to-node datacom protocol contained in the CCITT's X.25 multilevel protocol (which covers Layers 1, 2 and 3).

Turning to the COPs, note that the two dominant versions are IBM's Binary Synchronous Communications (BSC or Bisync) and Digital Equipment Corp's Digital Data Communications Message Protocol (DDCMP). Between these two exist hundreds of proprietary variations (such as ones for passenger-reservation systems) that emulate the IBM or DEC technique in thousands of compatible products.

To gain a better understanding of the differences among these DLC types, first examine the structures of two very popular BOPs (HDLC, and SDLC) and the two top COP contenders, Bisync and DDCMP (Figure [4]).

BOPs all have similar frame structures

HDLC-subset distinctions become visible with a field-by-field description of a typical BOP frame. Beginning with an 8-bit flag sequence, a frame is sequentially built by adding Address, Control, Information (data) and Frame Check fields and finally another flag. All fields except the Information field consist of single or multiple 8-bit patterns designated octets. The Information field can be of any length (not necessarily a multiple of characters or bytes), although some specific implementations such as SDLC require that it be an integer multiple of eight bits.

The entire transmitted frame, also called a block, gets examined by each station attached to the data link. The BOP hardware resident in each receiver continuously examines the Address field and enables that receiver immediately upon detection of its own address. The address is usually a single octet, but provisions are available for transmitting a multiple-octet address.

In all HDLC implementations, the DLC behaves differently for primary and secondary stations, or masters and slaves. In any network, only one master can exist, and slaves can transmit only when the master explicitly gives them permission to do so. When a secondary station transmits, the Address field is its own rather than the destination address. A primary station accepts this message only if it has given that secondary station permission to transmit. As one measure of flow control, the primary station periodically enables each secondary by transmitting an explicit permission message. Mandating the inclusion of the Address field in every message permits a primary station to interleave receptions from two or more secondary stations without garbled results.

Next in sequence, the control field contains one or two octets depending on which HDLC subset and mode — extended (two octets) or non-extended (one octet) — are used. Control determines (informs the receiver of) the message type, the sequencing of send and receive flames, the explicit poll command (permission to transmit) and/or the final response from secondary to primary station. A primary station uses the Control field to command specific actions by a secondary, while a secondary station encodes the Control field with appropriate response data. Together, the Address and Control fields make up a Header.

The Information field can contain virtually any number of bits, but practical considerations limit the field according to flow-control regulation in complex networks. (For instance, you might not want to repeat a 20-min block because one error shows up; you would use smaller blocks.) However, long Information fields are easily accommodated with sequential frames that collectively constitute a complete transmission. Data in the field can employ any code structure: BCD, standard binary, packed decimal or others. It is important to use a code defined by the terminal address. Note in addition that the special control characters exclusive to a particular secondary station get included in the Information field.

Understand datacom protocols by examining their structures

Finally, the Frame Check field provides a code that can serve at the receiving end to verify error-free message reception. It is generally the remainder of a CRC calculation based on a standardized polynomial.

BOPs use few control characters

BOPs do not use control characters to delineate message blocks. Only two distinct bit patterns, which need not occur on character boundaries, carry special meaning within a BOP message: Flag (01111110) and Abort (1111111). Thus, to achieve data transparency, you need only ensure that a sequence of six or more ONEs never gets transmitted unless you want to send a Flag or an Abort. (Transparency is important because every datacom message consists of bit patterns representing both data and control information that flow along one communications link; you therefore need techniques that distinguish data from control. Transparency allows characters (bit patterns) to get transmitted as data without regard for their inherent control definitions).

To ensure data transparency, BOPs use a bit-stuffing technique termed Zero Insertion and Deletion (Figure [5]a). The transmitting end examines the outgoing bit stream, and if it detects a sequence of five ONEs, it unconditionally inserts a ZERO into the bit stream (the Flag- and Abort-generation circuits bypass this step). The receiving end then deletes any ZERO that follows exactly five ONEs.

What are the major differences among the major BOPs? As seen in Figure [6], they differ primarily in the length of the Address and Control fields and method of re-transmitting rejected (erroneous) frames. When designing a data-link protocol into a piece of equipment, you will generally choose the one that your device must interface with. But if no such restrictions apply — for example, when you are interconnecting a closed system — the HDLC/ADCCP protocol provides the most flexibility because the Address-field extension allows you to address a large number of stations and the 2-octet Control-field option allows as many as 127 frames to remain unacknowledged before a response from the secondary station is required.

COPs: a more complex control structure

Turning to the structure of COP frames, note that although the exact nature and sequence of fields varies with the DLC, all COP blocks contain Header, Information (data) and Block Check fields. The detailed structure of a COP (Figure [4]) illustrates the options for each field, and the differences between the two most widely used COPs — Bisync and DDCMP — are discernible.

The first major field, the Header, although here an independent field, performs the same basic role as in BOPs — it can incorporate the address of either the message source or destination, a job number, message type (control or data) and required control action, as well as positive or negative acknowledgement related to error-free reception of a prior message. The control sub-field can serve to initialize a receiver, ask why an acknowledgement has not yet occurred, abort a message transfer or acknowledge correct or incorrect reception of prior blocks. Encoding of the control messages is accomplished with predetermined characters.

Next, a typical Information field can contain characters of an information code set in BCD, binary, floating point or other pure data codes. Because of its great flexibility, the field can also contain a special code or even a machine-language computer program.

Completing a message unit, the Block Check field provides a code that, when used at the receiving end, can verify error-free reception of a message. This field can be based on a parity check or, as is the case in all major DLCs, the remainder of a CRC calculation. Some DLCs provide a Block Check field at the end of both the Header and Information fields.

As previously noted, COPs have a common characteristic in that they all use a fully defined set of control characters (Figure [4]b). Remember that BOPs use only two control-character sequences; thus, the use of this character set makes code transparency in COPs a complex task because of a relatively long list of bit sequences that cannot appear in the Information field.

In their approach to handling data transparency, COPs fall into two sub-classes: The Character Controlled class (such as Bisync) uses special 2-character sequences to enter and exit the Transparent mode (Figure [5]b); the Character Count class (such as DDCMP) uses a standardized Header format that explicitly provides a character count for the Information field. This latter approach allows a receiver to determine the end of a message without including control characters in the Information field, thus automatically making this field transparent.

Some significant differences between BOPs and COPs should now be apparent (Figures 4, 5 and 6). Both types of DLC provide for data transparency, but the overhead for BOPs is lower than for COPs, resulting in higher data rates for BOPs. Furthermore, BOP message frames share many common characteristics regardless of the specific DLC used, including a standard frame format, code independence due to bit stuffing, positional significance rather than control characters or character counts, and either half- or full-duplex operation (only some COPs work in full-duplex mode). In addition, BOPs offer a wider range of modes and user programmability as well as the widest acceptance among vendors and standards organizations. Thus, despite the fact that COPs have been in use for more than 20 years and currently control more network nodes than any other type of link-layer protocol, you can safely assume that more datacom-engineering time will be devoted to designing-in HDLC-like BOPs during the next decade than to any other DLC.

The second major DLC function

Recall from the initial definition of a DLC that a key function is error detection and correction. This task varies in importance depending on the DLC application. It ranges from completely ignoring errors in applications such as hulk-text transfers of lengthy word-processing files to absolute zero-defect assurance in applications such as transferring financial records or stock quotes.

Statistical error rates for various applications give insight into the error-control/recovery task that you must consider in DLC selection. In transfers between a computer and disk at rates to 10^9 bps, the error rate typically equals one in 10^3 bits. In a typical datacom setting using a dial-up public telephone network, though, the data rate is a comparatively modest 10^3 to 10^4 bps while the error rate escalates to one in 10^5 bits. These two applications are thus more than 10 orders of magnitude apart in expected errors.

DLC error-control methods include Hamming codes, vertical (parity) and longitudinal redundancy checks (VRCs and LRCs) and cyclic redundancy checks (CRCs). Link-layer protocol structures always provide Error Control fields, and detected errors result in a request for re-transmission across the data link.

In general, DLCs offer two types of re-transmission requests (ARQs): Stop/Wait and Continuous. In the Stop/Wait procedure, the transmitting station literally stops sending after the transmission of a block or frame. It then waits until the receiving station performs the predetermined error check, sending an ACK to confirm correct reception. If the receiver finds the message erroneous, it sends a

Understand datacom protocols by examining their structures

NAK and the previous block gets re-transmitted. The overhead in terms of line idle time and turnaround for this type of ARQ is obviously very high, and DLCs that use it don't fully exploit line capacity. The Stop/Wait procedure is most often found in simplex and half-duplex communication links.

In continuous ARQ, blocks move continuously and the transmitter provides buffer storage while both the transmitter and receiver monitor block counts. When it detects an erroneous block, the receiver transmits a NAK control message that contains the defective block's number. Two implementations of this type of ARQ are widely used: Go-Back-N and selective repeat (Figure [7]). The former results in the re-transmission of both the defective block and all subsequent in-transit blocks; the latter improves link efficiency by re-transmitting only the defective blocks. Both implementations require a full-duplex link and typically can improve line utilization by a factor of two because line turnaround and idle time are virtually eliminated.

LANs vs datacom links

Although datacom links have seen wide use for many years, the great attention now given to local-area networks (LANs) raises the question of what differentiates the two.

To understand the distinctions, look first at the general description of a LAN: a datacom system that allows several independent devices to intercommunicate and that confines communication to a moderate-sized area such as an office building, a warehouse or a campus. It accomplishes communication over a physical channel with a moderate to high data rate (1M to 10M bps) and a consistently low error rate (because of LANs' well-defined cable links, you can better predict and control such speed-degrading factors as cable and unit delays). Finally, LANs allow any network user or device to have direct access to any other point.

A standard datacom link, on the other hand, generally uses a long-distance network consisting of interconnect facilities in different parts of a country or the world often a part of the public switched telephone network. A more important distinction, though, is that standard datacom links implicitly rely on a master that controls bus activity. Although the polling method used in standard datacom networks to allocate link usage functions adequately, it does have several disadvantages:

1. It is difficult to adapt the system to changing conditions. For instance, if some unit's activity peaks at certain times, you must write an elaborate software algorithm so that the master can account for this fact. Further, if system characteristics change over time, you must continually update this algorithm.

2. Modularity is difficult to implement. Because a central unit controls all system activity, adding or deleting modules from the bus dictates a change in the control software. This requirement holds even if you add or delete units that talk only to each other and not to the primary.

3. Total system reliability depends on the primary station's reliability; if that unit goes down for any reason, the entire system stops functioning.

4. Protocol overhead for data collection or control applications can be high. Because standard serial buses do not have interrupt capability, the primary must continually poll the data-gathering and status-monitoring units. Often, however, the polling action indicates no change in status and returns little meaningful data. Thus, protocol overhead is high compared with the volume of data gathered.

As noted earlier, most LANs do not employ the central-controller concept; each network unit can take control of the system bus when needed and transmit data directly to appropriate units. Because several units can vie for bus control simultaneously, two prevalent methods of resolving such conflicts have arisen: carrier sense multiple access with collision detection (CSMA CD) and token passing.

This networking concept leads to the following advantages over classical datacom structures:

1. The bus can self adapt to changing conditions because modules request the bus only when they need it. If necessary, some modules can be assigned higher priority than others.

2. Modularity is easy to implement. You can add units to the bus without disturbing existing units provided that the total at any time does not exceed the bus's effective bandwidth.

3. System reliability is high because system communications capability does not depend on any particular unit being connected.

4. Control and monitoring systems are efficiently implemented (when bus bandwidth is close to the data bandwidth) because any unit can directly address any other, effectively allowing interrupt capability.

Because LANs achieve high transmission speeds and typically interconnect intelligent equipment, they universally use synchronous transmission mode, generally implemented with BOPs. The LAN unit of information transfer, usually designated a packet, is structurally similar to an HDLC frame. It consists of a source address, destination address, control code, information and a frame-check sequence. The two addresses identify the transmitter and receiver, the control code tells the receiver what kind of data is being sent and the frame-check sequence allows detection of transmission errors. Unlike conventional BOP frames, however, LAN frames do not need bit stuffing to achieve data transparency. Rather, the start- and end-of-packet delimiters get implemented with special code-violation patterns in the modulation scheme (typically Manchester) that encodes the clock and data on one signal, instead of using a special character such as a flag.

Thus, although classical datacom networks could be designated LANs if they meet the general definition previously presented, there is nonetheless a clear distinction between them — although the functional differences between the most advanced datacom links and the least advanced LANs are small.

PREAMBLE	START FRAME DELIMITER	ADDRESS (DESTINATION)	ADDRESS (SOURCE)	MESSAGE LENGTH	MEDIA-ACCESS CONTROL DATA	PAD	FRAME CHECK	**CSMA** (TYPICAL)

START FRAME DELIMITER (2 OCTETS)	ACCESS CONTROL (1 OCTET)	ADDRESS (DESTINATION) (2/6 OCTETS)	ADDRESS (SOURCE) (2/6/ OCTETS)	INFORMATION (≤ 4099 OCTETS)	FRAME CHECK (4 OCTETS)	END FRAME DELIMITER (2 OCTETS)	**TOKEN RING**

PREAMBLE/ IDLE (1 OR MORE OCTETS)	START-FRAME DELIMITER (1 OCTET)	ACCESS CONTROL (1 OCTET)	ADDRESS (DESTINATION) (2/6 OCTETS)	ADDRESS (SOURCE) (2/6/ OCTETS)	INFORMATION (≤ 4099 OCTETS)	FRAME CHECK (4 OCTETS)	END FRAME DELIMITER (1 OCTET)	**TOKEN BUS**

Framing diagrams for popular LAN types show that these message packets require both source and destination addresses, in contrast to DLC protocol's single-master multiple-slave architectures, which require polling at the expense of speed.

A designer's review of data communications

Author: Alex Goldberger *Reprinted by permission of Computer Design, from May 1981 issue*

Efficient communication systems depend on knowledge of design concepts and principles for encoding and transmitting digital data

Recent developments in information systems and computer and microcomputer hardware have highlighted the need for efficient data communications. Industrialists, educators, financial institutions, and government organizations are finding computer services essential to their operation, and the data communications link is an integral part of these services.

Data communication refers to the electronic transmission of encoded information or data from one point to another. As used here, the term encompasses all the physical elements, systems, devices, and procedures that are required for the transmission and reception of data between two or more points. Elements of a data communication system are communication channels, transmission modes, line conditioning, modems, serial communication interfaces, data link configurations, information codes, and protocols.

The data communication process generally requires at least five elements: a transmitter or source of information, a message, a binary serial interface, a communication channel or link, and a receiver of transmitted information (Figure 1) . A data communications interface is often needed to make the binary serial data compatible with the communication channel.

Communication Channels and Facilities

A communications link or channel is a path for electrical transmission between two or more stations or terminals. It may be a single wire, a group of wires, a co-axial cable, or a special part of the radio frequency spectrum. The purpose of a channel is to carry information from one location to another. All channels have limitations on their information handling abilities, depending upon their electrical and physical characteristics.

There are three basic types of channels: simplex, half-duplex, and full-duplex. As an example of each, consider transmission between points A and B in Figure 1.

Transmission from A to B only (and not from B to A) requires a simplex channel. Simplex channels are used in loop mode configurations such as supermarket checkout terminals. Transmission from A to B and then from B to A, but not simultaneously, requires a half-duplex channel. If a 2-wire circuit is used, the line must be turned around to reverse the direction of transmission. A 4-wire circuit eliminates line turnaround. Transmission from A to B and from B to A simultaneously describes a full-duplex channel. Although four wires are most often used, a 2-wire circuit can support full-duplex communications if the frequency spectrum is subdivided into receive and transmit channels.

In addition to the direction of transmission, a channel is characterized by its bandwidth. In general, the greater the bandwidth of the assigned channel, the higher the possible transmission speed. This speed is usually measured in terms of the number of line signal elements per second, the baud rate. If a signal element represents one of two binary states, the baud rate is equal to the bit rate. When more than two states are represented, as in multilevel modulation, the bit rate exceeds the baud rate. The range of channels includes private wire, wideband, Digital Data Service, limited distance, voice grade, subvoice grade, and telegraph (Table 1).

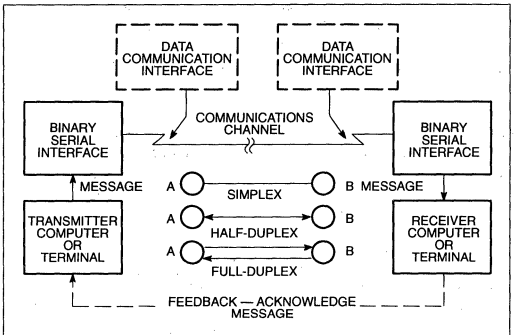


Figure 1. Elements of Data Communications Process. Five major elements are source, message, interface channel, and receiver. Channel can be any of three basic types.

Digital vs Analog Transmission

Digital transmission can be applied to digital data or analog voice signals. In either case, information is sent over the communications channel as a stream of pulses. Pulses transmitted over a communication line are distorted by line capacitance, inductance, and leakage.

The longer the line or the faster the pulse rate, the more difficult it is to interpret the received signal. This signal degradation is the reason for the closely spaced regenerative repeaters used in digital data transmission facilities. When noise and distortion threaten to destroy the integrity of the pulse stream, the pulses are detected and regenerated. If the regeneration process is repeated properly, the received signal will be an exact replica of the transmitted signal. It is possible to transmit pulses over short distances using privately owned cable or common carrier wire pairs. This is baseband transmission and usually requires line drivers and receivers on each end of the line. Longer distance communication must use the digital transmission facilities of the common carriers.

In analog transmission, a continuous range of signal amplitudes or frequencies is sent over the communications line. Linear amplifiers maintain signal quality. The voice telephone network supplied by the common carriers uses analog transmission facilities to service most data communications users. To interface the analog voice channels to digital terminals and computers, a modulator-demodulator (modem) is used. In a modem, digital information modulates a carrier signal, which passes through the telephone network just as does a voice signal. At the receiving end, the signal is demodulated back into digital form.

Voice Grade Lines

Voice grade telephone lines are available through the public switched network (Direct Distance Dialed or DDD); as private leased lines without conditioning; and as private, conditioned, leased lines. Although the bandwidth is the same for all three, the effective data rates vary because of different specifications for signal noise, amplitude attenuation, and envelope delay distortion.

Dial-up lines are the 2-wire pairs supplied by the common carriers on the public switched telephone network. Most often these lines are used for half-duplex operation, although frequency band splitting modems can facilitate full-duplex at 1200 bits/s. A major advantage of dial-up lines is that any point on a worldwide telephone network can be reached. Furthermore, communication costs are limited to the time the lines are actually in use.

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Table 1. Communication Channel Characteristics

Channel Type	Channel Interface	Data Rates (bits/s)	Applications
Fiber optics	Fiber optic connector	Up to 2G	Computer-computer, WAN, Computer-high speed peripheral
Private wire or cable	Line drivers and receivers Modem eliminators Limited distance modems	1M to 155M	In-plant data communications Local Area Network
Wideband analog	Wideband Bell 300-series modems, CCITT V-series wideband modems	19.2k to 230.4k	Telephone channel multiplexing
Dataphone Digital Service	Data Service Unit Digital Station Terminal	2.4k, 4.8k, 9.6k, 56k, 1.544M	Private terminal-computer geographically dispersed links
Switched telephone network (DDD)	2-wire modems Acoustic couplers	0 to 2k (async), 2k to 4.8k (sync) 300, 450, 600, 1.2k (async)	Terminals, data collection stations, other interactive communications
Leased voice grade lines (with or without conditioning)	2/4 wire modems	0 to 2.4k (async) 2k to 9.6k (sync)	Remote batch, private communications networks
Subvoice grade	Narrowband modems	150 to 200	Teletypes, A-D converters, telemetry
Telegraph	DC signaling	45 to 75	TWX, TELEX

Four major problems are associated with the switched telephone network. First, the lines may be noisy. The human brain can interpret what is being said despite the interference that plagues many calls, but computers and terminals can easily lose or misinterpret data because of noise. Second, delay distortion is caused by the various frequency components of a signal being transmitted at a nonuniform speed through the transmission medium. This may result in received data that are erroneous. Third, the switched network requires relatively long connect, disconnect, and turnaround times, which limit the system data throughput. Fourth, the reliability of telephone switching equipment is relatively low.

Although more costly than dial-up lines, private leased lines largely circumvent the problems that afflict the switched network. Their basic advantages are ready availability and freedom from busy signals, fixed monthly charges, and conditioning for better data quality, as well as higher transmission rates and throughput. Leased lines are generally 4-wire circuits usable for half- or full-duplex operation. Simultaneous transmission and reception is possible, and line turn-around is eliminated. The basic disadvantages of leased lines are higher cost and the line's connection to only one location. However, if telecommunication demands entail high volume, high quality, high speed traffic between two points, a leased line is the best choice.

Digital Data Services

The Bell System developed a digital transmission network that provides higher data rates with fewer errors at a lower cost than conventional analog transmission facilities. Known as Dataphone Digital Service (DDS), the network is available in 32 U.S. cities and recently has been granted Federal Communications Commission (FCC) approval for 64 other cities. Two point, full-duplex, private line service is provided at synchronous data rates of up to I.544M bits/s. In June 1977, the FCC approved construction of American Telephone & Telegraph (AT&T)'s Dataphone Switched Digital Service (DSDS).

Specialized common carriers offer a variety of services in addition to those of the Bell System. These include shared private line services such as EXECUNET by MCI Communications and SPRINT by Southern Pacific; satellite services by the Radio Corporation of America, Western Union, and others; packet-switching carriers including Telenet by General Telephone and Electronics and Tymnet by Tymshare; and facsimile and electronic mail services such as Graphnet, TWX, TELENET, and SPEEDFAX.

Modems

Modems are devices that convert digital data from a computer or terminal to a modulated carrier waveform required by the communication channel. One modem is needed at each end of the channel, as shown in Figure 2. Modems are also known as data sets and are designed for specific kinds of service and for specific bandwidths or data rates. Those discussed here accept a binary serial input from the transmitter and provide a binary serial output to the receiver. Parallel input modems (used mostly for paper tape transmission) and analog input machines (used primarily for facsimile transmission) are not considered. The three types that are considered are short haul, wideband, and voice grade (Table 2).

Voice grade telephone lines with a bandwidth of 2700 Hz (300 to 3000 Hz) are by far the most common medium used for data communications. A voice grade modem, designed for use on these lines, should be selected on the basis of the type of service (dial-up or leased), the required data rate, and an acceptable level of error performance. The two broad categories of voice grade modems are asynchronous units and synchronous units. Asynchronous units operate at a maximum data rate of 1800 bits/s over dial-up facilities and 2000 bits/s on conditioned leased lines. Acoustic couplers are asynchronous modems designed for dial-up use that are generally limited to speeds of 600 bits/s or less. Synchronous units operate at a maximum data rate of 4800 bits/s over dial-up and 9600 bits/s on conditioned leased lines.

Wideband modems operate over telephone transmission facilities at speeds of 19.2k bits/s to 230.4k bits/s. This class of data set is supplied almost exclusively by the common carrier and requires the bandwidth of 6 to 60 dedicated voice grade channels. Examples are the Bell 303B, -C, and -D for 19.2k-, 50k- and 230.4k-bit/s full-duplex operation.

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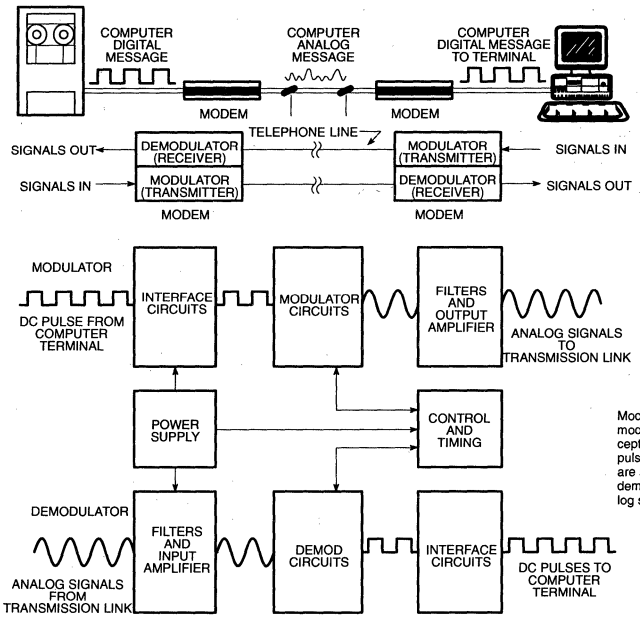

Figure 2. Analog Transmission Using Modems

Short haul modems operate over relatively short distances — generally less than 10 mi (16 km) — on solid conductor, non-band limited, non-loaded lines. In some cases, they are not true modems but are line drivers and line receivers that transmit and receive digital data. Although the communication line must be carefully chosen, the cost can often be one-tenth that of a voice grade modem rated at the speed. Other advantages are higher speed and reliability and easier maintenance.

Asynchronous and Synchronous Transmission

Asynchronous data are typically produced by low speed terminals with rates of less than 1200 bits/s. In asynchronous systems [Figure 3(a)], the transmission line is in a mark (binary I) condition in its idle state . As each character is transmitted, it is preceded by a start bit, or transition from mark to space (binary 0), which indicates to the receiving terminal that a character is being transmitted. The receiving device detects the start bit and the data bits that make up the character. At the end of the character transmission, the line is returned to a mark condition by one or more stop bits, and is ready for the beginning of the next character. (An asynchronous character varies in length depending on the information code employed.) This process is repeated character by character until the entire message has been sent. The start and stop bits permit the receiving terminal to synchronize itself to the transmitter on a character by character basis.

Synchronous transmission (Figure 3(b)) uses an internal clocking source within the modem to synchronize the transmitter and receiver. Once a synchronization character (SYN) has been sensed by the receiving terminal, data transmission proceeds character by character without the intervening start and stop bits. The incoming stream of data bits is interpreted on the basis of the receive clock supplied by the modem. This clock is usually derived from the received data through a phase locked loop. The receiving device accepts data from the modem until it detects a special ending character or a character terminal count at which time it knows that the message is over. The message block usually consists of one or two synchronization characters, a number of data and control characters (typically 100 to 10,000), a terminating character, and one or two error control characters. Between messages, the communication line may idle in SYN characters or be held to mark. Note that synchronous modems can be used to transmit asynchronous data, and, conversely, asynchronous modems can be used for synchronous data if the receiving terminal can derive the clock from the data.

Asynchronous transmission is advantageous when transmission is irregular (e.g., when it is initiated by a keyboard operator's typing speed). It is also inexpensive because of the simple interface logic and circuitry required. Synchronous transmission, on the other hand, makes far better use of the transmission facility by eliminating the start and stop bits on each character. Furthermore, synchronous data are suitable for multilevel modulation, which combines two or four bits in one signal element (baud). This can facilitate data rates of 4.8k- or 9.6k bits/s over a bandwidth of 2.4 kHz. Synchronous modems offer higher transmission speeds, but are more expensive because they require precisely synchronized clock and data.

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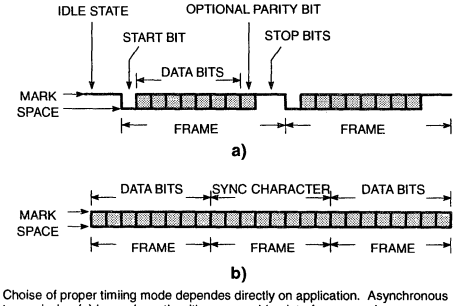
Table 2. Communication Channel Characteristics

Modem Type	Communications Channel	Data Rates (bits/s)	Use
1. Voice grade (vg)			
a. High speed synchronous	Leased line (3002 Dial-up	4.8k, 7.2k, 9.6k 4.8k	High volume machine to machine communications. 600 to 1200 bits/s.
b. Medium speed synchronous Medium speed asynchronous Medium speed asynchronous	Leased line/dial-up Leased line Dial-up	2.4k, 3.6k 1.8k, 2k 1.2k	Interactive or low speed remote batch operations. 150 to 300 bits/s
c. Low speed asynchronous	Dial-up	300, 600	Interactive teleprinters and glass teletypewriters, data acquisition and collection. 30 to 60 bits/s
2. Wideband			
a. Super group (60vg) b. Group (12vg) c. Half group (6vg) d. Lineplexer (2vg)	5700, 5800 (TELEPAK) 8801 8803 2 leased lines	230.4k 40.8k, 50k, 56k 19.2k 19.2k	Large volume telephone line multiplexing, dedicated computer to computer links
3. Short haul			
a. Limited distance [<10 mi (<16km)]	Private wire/cable Non-loaded, non-conditioned, non-carrier line	2k to 1M 2k to 19.2k	Data communications in plant (private wire) or off premises where distance is <10 mi (<16 km) [(leased line)]
b. Medium distance [<50 mi (<80km)]	Leased line	2k to 9.6k	Intermediate distance [10 to 50 mi (16 to 80 km)]
4. Modem eliminators and line drivers/receivers	Private wire/cable	2k to 1.544M	On-premises data communications. Typical distances are 500 ft (152 m) to 2 mi (3.2 km)



Choise of proper timiing mode dependes directly on application. Asynchronous transmission (a) is used mostly with man-machine interfaces; synchronous transmission (b) offers high speed necessary for machine-machine communication.

Figure 3. Asynchronous and Synchronous Transmission

Modulation Techniques

Whether to use the dial-up network or leased lines depends on how the modem modulates data prior to sending them over the phone line. Certain modulation techniques permit higher transmission rates than others, and all modulation techniques directly affect the maximum data rate and the error performance. The three basic modulation techniques are frequency shift keying (FSK), amplitude modulation (AM), and phase modulation (PM) (Figure 4).

The most popular form of frequency modulation is FSK, in which the carrier frequency (operating at, say, 1700 Hz) is modulated ±500 Hz to present binary 1 or binary 0. Thus, a frequency of 1200 Hz represents a zero, while a frequency of 2200 Hz represents a binary 1. FSK techniques are generally quite suitable for low speed devices like teleprinters and allow operation at speeds as high as 1800 bits/s.

AM enables a modem to transmit and receive the analog equivalents of binary 1s and 0s. This technique involves varying the amplitude of the line's carrier frequency. Several levels of amplitude modulation are possible, allowing twice as much data to be sent in the same time frame. Both AM and FSK are quite suitable for data transmission; however, FSK has a noise advantage over AM, and AM allows more efficient use of the available bandwidth.

PM modems are generally described in terms of the number of phase shifts generated, and operate at speeds of 2000 bits/s and above. In this technique, the transmitted signal is shifted a certain number of degrees in response to the pattern of bits coming from the terminal or computer. For example, in a 2-phase PM modem, if the analog signal generated by the transmitting modem is shifted 180°, a binary 1 (or 0 if desired) is indicated. If there is no shift, then the signal will be interpreted as a series of zeros (or ones) until such a shift is sensed. Generally, PM modems operate in four and eight phases, permitting up to two or three times the data to be sent over the line in the same bandwidth. Most 4800- and 9600-bits/s modems use PM.

Conditioning and Equalization

As data in the form of analog signals are sent down the line between modems, they suffer from the effects of envelope delay and amplitude distortion. Signals of different frequencies are delayed or attenuated by varying amounts as they are transmitted. To compensate for these effects, two techniques are employed: line conditioning and modem equalization.

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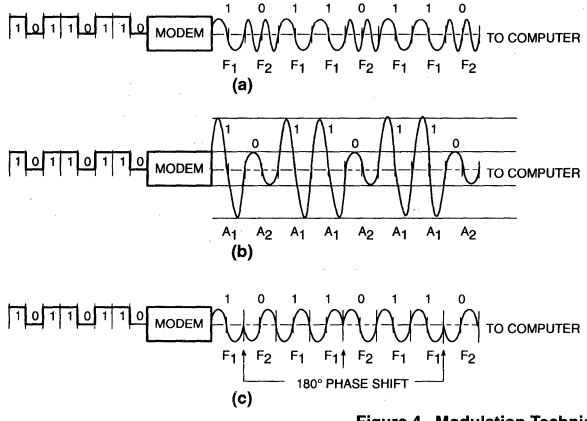


In frequency shift keying (a), digital signal (left) received by modem is shifted in frequency to represent binary 1 and binary 0. Because of the time needed to shift from one frequency to another, two is generally the maximum number used. In amplitude modulation (b), digital signals are amplitude modulated by modems using this technique. Here, one carrier signal amplitude (A1) represents binary 1, and another (A2), binary 0. In phase modulation (c), whenever 180° phase shift is encountered, receiving mode assigns value of binary 0; at all other times, value of binary 1 is assumed.

Figure 4. Modulation Techniques

Conditioning is the process by which the telephone company maintains the quality of a specific, privately leased line to a certain standard of permissible delay distortion and signal attenuation. AT&T has two types of conditioning referred to as C and D, There are five categories of C conditioning (C1 through C5) and two categories of D conditioning (D1 and D2). C conditioning attempts to equalize the drop in signal voltage and envelope delay for all frequencies transmitted; D conditioning controls the signal to noise ratio and harmonic distortion. Both may be used on the same communication channel.

Equalization refers to modem compensation for amplitude and envelope delay distortion of the line. Equalization is seldom required in lower-speed modems attached to a leased line, since minimum line conditioning is sufficient. However, conditioning and equalization are required when higher speed modems (4.8k- and 9.6k bits/s) are attached. Modems used for high speed transmission over the dial-up network must have equalization, since it is never certain exactly which unconditioned telephone line will be used.

Communication Line Sharing and Modem Sharing

When several input/output devices are required at one end of a communication link, a multiplexer or modem sharing unit, which enables these devices to share one communication line, can be used to reduce costs. Multiplexers take low speed inputs from a number of terminals and combine them into one high speed data stream for simultaneous transmission on a single channel. At the other end of the link, a second multiplexer (actually a de-multiplexer) reconverts the high speed data stream into a series of low speed inputs to the host computer. The channel is split into time slots (time division multiplexing) or frequency bands (frequency division multiplexing). Intelligent or statistical multiplexers increase line utilization by allocating time slots on the basis of a line activity algorithm.

Modem sharing units enable multiple terminals to share one modem. They are particularly valuable in networks that require clusters of terminals at remote sites because the number of modems and transmission lines are reduced. Operation is polled half-duplex. Multiport modems can split a high speed channel (e.g., 9600 bits/s) into various medium speed channels (e.g., four 2400 bits/s and two 4800 bits/s), thus permitting several medium speed terminals to share a 9600 bit/s line. A miniplexer is a device that performs channel splitting for DDS as well as for a single 3002 leased line. A lineplexer or biplexer splits 19.2 kbit/s data into two 9600 bit/s paths that can be transmitted over two conditioned full-duplex channels. This eliminates the need for a wideband channel to send and receive data at 19.2 kbits/s. A port sharing unit connects to a communication controller or central processing unit port and transmits or receives data from two to six terminals or modems. Less costly than a multiplexer, it reduces the number of controller ports in a polled terminal data communications configuration and makes more efficient use of connected ports.

Standards and Protection

The electrical, functional, and physical interface to data terminal equipment provided by modems is compatible with Electronics Industries Association (EIA) or International Consultative Committee for Telephone and Telegraph (CCITT) standards. Most commercial models conform to EIA RS-232, and plug to plug compatibility via a 25-pin connector is ensured between modems and data terminal equipment that subscribe to this standard. CCITT V.26 is the electrical equivalent of RS-232-C, while V.24 is the U.S. standard's functional pin equivalent. CCITT V.35, a current-mode, 34-pin connector interface standard for serial data transmission up to 56k bits/s, is used by wideband European modems and in the Bell System DDS Data Service Unit at 56k bits/s. Military standard (MIL-STD) 188 is a U.S. government standard for military communications equipment. An improved EIA functional standard, RS-449, was approved in November 1977.

Common carrier equipment on the switched telephone network must be protected. A device called a data access arrangement (DAA) limits the attached modem's signaling power to prevent it from exceeding the power level restrictions of the communication channel. In 1977, the FCC ruled that modem manufacturers can incorporate equivalent protective circuitry in their products, register them with the FCC, and connect them directly to the telephone network. DAAs are available from FCC-certified independent suppliers and can be leased from the Bell System. Modems rented from the Bell System or those used on leased lines do not require a DAA.

A designer's review of data communications

Protocols

Protocols provide the necessary ground rules to ensure the orderly and accurate transfer of data between digital devices. Data communications protocols are growing in importance as the terminal population increases, distributed processing becomes widespread, and new communications technologies, such as packet switching and satellite links, become commonplace.

Protocols associated with data communications have several major levels, or layers, that define various functions and operations. Each level is designed to be functionally independent of the others, but the function of each depends on the correct operation of the previous level. The protocols embodied in these levels range from those that define the physical and electrical links, e.g., RS-232-C and CCITT V.35, to those that are responsible for functions such as message buffering, code conversion, recognition and reporting of faulty conditions in terminals or lines, communication with the host mainframe, and management of the communication network. They are implemented by software packages like International Business Machines (IBM)'s Systems Network Architecture (SNA), CCITT's X.25, and Digital Equipment Corporation (DEC)'s DECnet.

The remainder of this article concerns data link control protocols (DLCs), the sets of rules necessary for effective communication between terminals and computers over conventional communications channels. DLCs are involved in handling the communications link itself and moving information across it efficiently and accurately. Their basic functions are to establish and terminate a connection between two stations; to ensure message integrity through error detection, requests for re-transmission, and positive or negative acknowledgments; to identify sender and receiver through polling or selection; and to handle special control functions such as requests for status, station reset, reset acknowledge, start, start acknowledge, and disconnect.

Structure of Data Link Controls

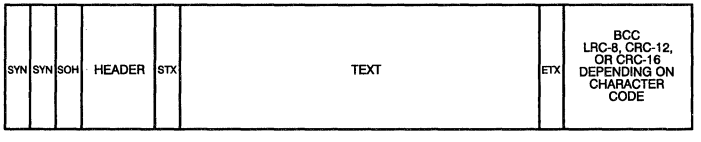
Data link controls can be classified into Character Oriented Protocols (COPs) and bit oriented protocols (BOPs). In COPs, a defined set of communication control characters effects the orderly operation of the data link. These control characters are part of a character code set. COP messages are transmitted in blocks composed of a header or control field, a body or text field, and a trailer or error checking field with characters used as field or block delimiters. Examples of COPs are IBM's Binary Synchronous Communications Protocol (BISYNC) and DEC's Digital Data Communications Message Protocol (DDCMP). Block formats for these are illustrated in Figure 5.

BOPs use only two or three specific control characters for operation of the data link. These characters are used to delimit the beginning (FLAG) and end (FLAG, ABORT, GA) of a message frame. Upon receipt of the opening FLAG, positional significance is used to delineate the bit sequence that follows into prescribed fields (Figure 5).

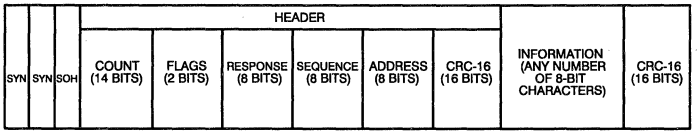
These fields are address, control, information, and frame check sequence. The address, control, and frame check fields are of fixed length; the information field length is variable and may be zero.

COP Messages

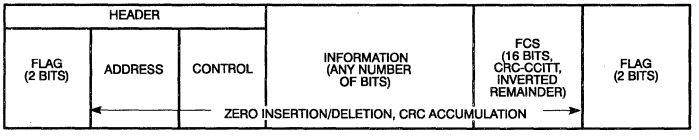
As already stated, COP messages are transmitted in units called blocks. The header field contains auxiliary information that identifies the address of the message destination or source, the job number (if any), the type of message (data or control), the control action, and a positive or negative acknowledgment to ensure error-free reception of a previous message (or messages). Control actions are used to reset or initialize a secondary station, to acknowledge good or bad reception of blocks, to inquire why a response or acknowledgment has not occurred within a specific time period, or to abort a transfer sequence. The control information is conveyed via special characters or character sequences.



a. Binary Synchronous Communications (BISYNC)



b. Digital Data Communications Message (DDCMP)



c. Bit Oriented Protocol (BOP) Block Format

SYN : SYNCHRONOUS IDLE
SOH : START OF HEADING
STX : START OF TEXT
ETX : END OF TEXT

BCC : BLOCK CHECK CHARACTER
LRC : LONGITUDINAL REDUNDANCY CHECK
CRC : CYCLIC REDUNDANCY CHECK
FCS : FRAME CHECK SEQUENCE

Byte control protocols (a) and (b) use special control characters to enforce orderly data transmission of blocks containing header, body text, and trailing data. Bit oriented protocol (c) requires only two or three special control characters; however, information must be distinguished from final FLAG.

Figure 5. Typical Data Link Control Structures

A designer's review of data communications

The text field contains any data being transmitted. The text may be characters of the information code set or may be transparent to that code set. In the latter case, pure data (binary, packed decimal, floating point), specialized codes, or machine language computer programs must be distinguished from characters in the code set being used. This is done by employing a transparent mode whose implementation depends on the specific DLC.

To ensure correct reception of information over communication facilities, a sequence of check bits, often called block check characters or BCC, are generated and transmitted as an error check field. Each block of data transmitted is checked for errors at the receiving station in one of several ways, depending on the code and functions employed. These checking methods include vertical redundancy check (VRC), a parity check on each character, in conjunction with a longitudinal redundancy check (LRC), a horizontal parity; and cyclic redundancy check (CRC), which involves a polynomial division of the bit stream by a CRC polynomial.

BOP Messages

BOPs are more straightforward and universal than the COP just discussed. BOP messages are also transmitted in frames, and all messages adhere to one standard frame format. Common characteristics of BOPs are the independence of codes, line configurations, and peripherals; the use of positional significance instead of control characters or character counts; one standard frame format for all messages; the possibility of half- or full- duplex operation; the achievement of information transparency through zero insertion and deletion; and error checking on a complete frame.

A frame starts with the 8-bit FLAG sequence, followed in order by the sequences ADDRESS, CONTROL, INFORMATION (if present), and FRAME CHECK, and ends with another FLAG sequence. Each station attached to the data link continuously searches for the FLAG sequence and an ADDRESS sequence. In multipoint operation, for example, a secondary station must detect a FLAG immediately followed by its own ADDRESS to enable the receiver.

When the primary station transmits, the station ADDRESS sequence, which is usually one 8-bit field, designates which secondary station is to receive the balance of the transmitted frame. When a secondary station transmits, the ADDRESS tells the primary station which secondary station originated the frame. A secondary station must recognize its valid address before it can accept a frame and take any action on the contents of that frame. Also, the primary station will accept a frame only when it contains the address of a secondary station that has been given permission to transmit. To ensure the integrity of the data being transmitted, the ADDRESS sequence appears within each frame. This enhances flexibility in that the primary station can interleave receptions from several secondary stations without intermixing individual station information transfers.

The CONTROL field follows the ADDRESS sequence and is composed of one or two 8-bit bytes, depending on the protocol implementation. It is the heart of the BOP message, for it determines the type of message, the send and receive frame sequence counts, and a poll command from the primary station or final response from the secondary station. The primary station uses CONTROL to tell (command) the addressed secondary station what operation to perform. The secondary station uses CONTROL to react (respond) to the primary station.

The INFORMATION field may vary in length; this includes different lengths in the sequential frames making up a complete transmission. The data may be configured in any code structure: straight binary, binary coded decimal, and packed decimal, among others. However, the content of the field must be self-defining by actual or implied means. For example, peripheral device control characters, such as carriage return, will actually be part of the INFORMATION field, while the code being used may be implied in the address of a

Table 3. Common Protocol Characteristics

Feature	BiSYNC	DDCMP	SDLC	ADCCP
Full duplex	No	Yes	Yes	Yes
Half duplex	Yes	Yes	Yes	Yes
Message format	Variable	Fixed	Fixed	Fixed
Link control	Control character, character sequences, option header	Header (fixed)	Control field (8 bits)	Control field (8/16 bits)
Station addressing	Header	Header	Address field (8 bits)	Address field (8 bits to 00)
Error checking	Information field only	Header, information field	Entire frame	Entire frame
Error detection	VRC/LRC-8 VRC/LRC-16	CRC-16	CRC-CCITT	CRC—CCITT
Request for retransmission	Stop and wait	Go back N	Go back N	Go back N, selected reject
Maximum frames outstanding	1	255	7	127
Framing —start	2 SYNs	2 SYNs	Flag	Flag
—end	Terminating characters	Count	Flag	Flag
Gaps between characters allowed	Yes	No	No	No
Information transparency	Transparent mode	Inherent (count)	Inherent (zero/insertion/deletion)	Inherent (zero/insertion/deletion)
Control characters	Numerous	SOH, DLE, ENQ	None	None
Character codes	ASCII EBCDIC Transcode	ASCII (control character only)	Any	Any

A designer's review of data communications

specific terminal designed for a specific code. Furthermore, whether a frame contains an INFORMATION field at all depends on the particular CONTROL format transmitted. Table 3 presents a comparison of common DLCs.

Synchronization Techniques

Four kinds of synchronization — bit, character, block and message — must be distinguished when using synchronous transmission. Bit synchronization is achieved through a received clock signal which is coincident with the received serial data stream. Most modems or "business machines" (i.e., terminals) derive this clock by means of phased lock loops from the 0 to I and I to 0 transitions occurring in the received data. This technique, called self-clocking, overcomes the effect of propagation delay between distant stations and the tendency of electronic circuits within the modem to drift.

Character synchronization is accomplished by recognizing one or two "phasing" characters, often called SYN or sync characters. The receiver senses these SYN characters and phases its receive logic to recognize, by bit count, the beginning and end of each subsequent character. To ensure character synchronization throughout a message, SYN sequences are sometimes inserted in the transmitted data stream at 1- or 2-second intervals. This permits receiving stations to verify that they are in sync.

Request for Re-transmission

As previously mentioned, DLCs include an error checking field to allow the receiving station to validate the message. When errors are detected, the receiving station issues a request for re-transmission (ARQ). The two types of ARQs are stop and wait and continuous Each provides defined methods for acknowledging correct (error free) reception of transmitted blocks of information.

When a connection is established in the stop and wait ARQ, the transmitter sends one block and then stops. Eventually, the receiver acquires that block, subjects the block to an error check, and then sends an ACK control character to the transmitter to indicate that the block is correct, or a NAK control character to indicate an error. If an ACK is returned, the transmitter sends the next block in sequence. If a NAK is returned, that block is re-transmitted. Thus, the stop and wait mode involves periods of idleness, including propagation delays between each block, so that the line is not communicating nearly at its rated capacity.

In continuous ARQ, the transmitter keeps sending one block after another without stopping. The receiver and transmitter retain individual counts of the blocks outstanding and provide buffer storage to retain those blocks. Only when an erroneous block is detected does the receiver tell the transmitter to re-send that block and all subsequent in-transit, but unacknowledged, blocks.

Summary

As the installed base of computers and the speed and volume of their output have increased, so has the need to transmit that output to more places over longer distances. Inherent in the data communications process — the electronic transmission of encoded information from one point to another — are various physical elements, devices, and systems, as well as standards and procedures. An understanding of these basic elements and concepts can help users of computer services to take advantage of the communication systems that are now available.

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Complex datacom peripheral ICs interface to many processors

Revised by: A. Kazmi

Single-chip datacom peripherals have become so powerful they now implement a variety of software-selectable protocols. A large family of such devices is designed to interface to the 68000 and 80x processor families.

With computing power and memory dropping in price, you can now cost effectively put computational capability closer to where information is gathered or displayed. To capitalize on this distributed-processing trend, you must be aware of how to make various system elements communicate. Thus, you must be familiar with communication protocols and the ways to implement them with the variety of datacom peripherals now available.

First select the protocol

Protocols are the standard procedures and conventions that govern the transfer of data among communicating data-processing machines (see reference). They're classified by the manner in which they allow data to be transmitted, and for the purposes of this article (which addresses device-to-device links rather than bus-architecture interconnects such as local-area networks), you must be familiar with the terms asynchronous, synchronous, bit oriented and byte oriented protocols.

In asynchronous systems, transmission begins with a Zero/One transition that, when held long enough, becomes the start bit. Thus, the receiving node doesn't have to anticipate a transmission, and the structure of unique start and stop bits allows the receiver to synchronize itself to the transmitter on a character-by-character basis. In practical applications, you'll typically find asynchronous data in low-speed terminals with bit rates less than 1200 bps.

For higher speed synchronous transmission, the protocol coordinates the sending and receiving stations. There are two broad categories of protocols used in synchronous communication known as character-oriented protocols (COPs) and bit-oriented protocols (BOPs). COPs, dominated by IBM's Bisync and DEC's DDCMP, use units called blocks; in addition to data, these blocks contain error-checking and -correcting information. BOPs, although relatively new, have proliferated quickly; they're more straightforward in structure and application than COPs. BOP messages are transmitted in frames, and all messages adhere to a common format. Two of the most common BOPs are HDLC (ISO's high-level data-link control) and SDLC (IBM's synchronous data-link control). And while COPs can work in asynchronous as well as synchronous mode, BOPs can't. datacom peripheral chips now exist to help you implement all these protocols.

Look over this family tree

If your design goal is a system with minimum cost and maximum reliability, you'll likely investigate single-chip implementations for the central controller and protocol peripheral. One large family of datacom peripherals revolves around the 68000 and 80x processor families.

These parts often have dual numbers such as the 2681 and 68681. The former is the processor-independent version; the latter offers direct 68000 interface with minimum glue circuitry. If the last three digits of the part numbers are the same, their internal control sections are virtually indistinguishable. Understanding this fact gives you a head start in selecting the correct device for a particular processor and protocol. Following is a list of some of the more popular devices that you can now obtain; they appear in numerical order:

- 2652/68652 multiprotocol communications controller (MPCC) — dedicated to synchronous protocols and formats. It transmits and receives bit- and character-oriented protocols and also includes extra support for Bisync operation. Because the device can recognize and create special characters such as message delimiters (flags), sync characters and other link-control operators, it further enhances synchronous-communications transparency for bit-oriented protocols.
- 2661/68661 enhanced programmable communication interface (EPCI) — an upgraded version of the popular 2651 PCI. It functions as a universal synchronous/asynchronous receiver/transmitter (USART) that provides special support for Bi-sync. The EPCI also provides features that free the host from preprocessing data. For instance, if the µP can't feed data to it fast enough, it inserts control characters that serve as controlled datacom Wait states so the controller doesn't lose synchronization with the other node or otherwise lose data.

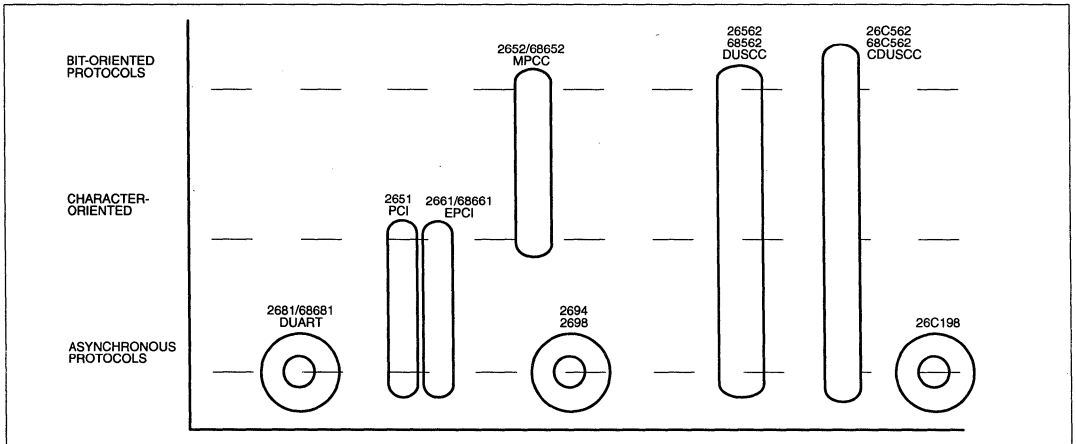
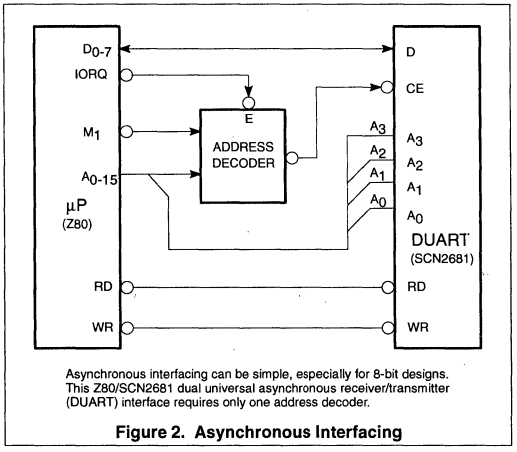


Figure 1. Philips Data Communication Products

Complex datacom peripheral ICs interface to many processors

- 2681/68681 dual universal asynchronous receiver/transmitter (DUART) — this dual-channel device performs well with 8- and 16-bit processors. The 2681 provides enhancements compared with single- and dual-channel UARTs: In addition to its two asynchronous data channels, it offers independent bit-rate generators (BRGs), self testing and interrupt handling. Moreover, you can use it in either polled or interrupt-driven systems. The 2681 comes in configurations of 24, 28 or 40 pins, each with different levels of I/O. For interfacing to the 68000, the 40-pin 68681 supplies the asynchronous handshake signals that the 68000 requires as well as an interrupt vector in response to receipt of an interrupt-acknowledge signal.
- The SC26C92 is a CMOS dual full duplex UART that is pin and software compatible with the previous SCN2681 and SCC2692. It features 8 byte FIFOs for each transmitter and receiver with four interrupt levels for each FIFO. Internal baud rates are provided to 230.4Kb; to 1Mb with an external clock.
- The SC26C94 is configured as four independent CMOS UARTs. It features 8 byte FIFOs for each receiver and transmitter with internal baud rates from 50b to 460.8Kb; to 1Mb with external clock. Its principle difference from the traditional Philips family UARTs resides in arbitrating interrupt system which drives a context sensitive configurable interrupt vector. Two 16 bit programmable counter/timers are provided with four I/O pins for each UART.
- The SCC2698B is a CMOS octal UART based upon the previous design of Philips UARTs and is software compatible with previous SCC and SCN type devices. It features 8 full duplex and independent UARTs with internal baud rates from 50b to 115.2Kb, four open-drain interrupt pins, four 16 bit programmable counter/timers and a multiplicity of general purpose output pins. Automatic RTS/CTS hand-shake is supported for all channels.
- The SC26/68C198 is a CMOS octal UART based upon the SC26C94. It features 16 byte FIFOs for each receiver transmitter, internal baud rates from 50 to 460.8Kb; to 1Mb with an external clock. It has an arbitrating interrupt system which drives a context sensitive and configurable interrupt vector. Its new features include programmable control of a fully automatic Xon/Xoff function, Multidrop character recognition, a general three character recognition system and a synchronous or asynchronous bus interface operating at a nominal 33MHz.
- The 26562 and 68562 Dual Universal Serial Communications Controller (DUSCC). This dual channel communication controller offers synchronous and asynchronous modes. In synchronous mode it offers Bit Oriented Protocols (BOP) such as HDLC, SDLC, etc. and Character Oriented Protocols (COP) such as BiSYNC, DDCMP, etc. It offers a wide range of Tx/Rx clock selection, one counter/timer per channel and an easy to use DMA interface. DUSCC has an on-board DPLL to reconstruct clock from receive data and various data encoding schemes such as NRZ, NRZI, FM and Manchester. DUSCC offers various methods of error detection ranging from parity generation/detection to CRC–16 generation detection (it also includes LRC and VRC methods). The 68562 provides bus interface signals for Mot 68000 family and 26562 provides bus interface with Intel 80x family. DUSCC can be used in interrupt or vector driven environments for control purposes and in DMA, interrupt and vectored mode for data I/O purpose.
- The 26C562/68C562 CMOS Dual Universal Communication Controller (CDUSCC) is an enhancement of its predecessor NDUSCC. It offers faster bus interface and higher serial data rate. It also offers deeper FIFOs, more standard baud rates, better interrupt control/enabling scheme and reduced power consumption.

These devices allow datacom designers to easily address protocol requirements in either synchronous or asynchronous mode because the controllers take over much of the datacom requirements for interpreting protocol rules.



Asynchronous interfacing can be simple, especially for 8-bit designs. This Z80/SCN2681 dual universal asynchronous receiver/transmitter (DUART) interface requires only one address decoder.

Figure 2. Asynchronous Interfacing

Design examples use similar software

Whether used individually or in combination, the Philips Semiconductors datacom interface chips support most standard protocols for device-to-device communications. To help you select the proper device for your system, consider the following design examples. Note that these examples don't provide software listings because they all operate on the same basic principles, and the routines would vary little.

Prior to initiating data communications, you must instruct the controller to program in the peripheral's operational mode by performing write operations to the Mode and Command registers; likewise, you can re-configure the devices any time during program execution. But if you do, be sure to disable the transmitter and receiver pair prior to loading the new command and mode information, or else you run a high risk of truncating a character during transmission or losing it during reception.

Once initialization is complete, software can control the transfer of information by either polling or interrupt subroutines or DMA operation. In all cases, the software must determine the request, whether for transmit- or receive-data requests. In addition, the routines should check for any errors that might have occurred and resolve those problems. In all cases, the routine must reset the condition that indicated the request. In most cases, it does so by reading or writing data to appropriate buffers on the communication chip.

Hardware design should be just as straightforward, if not easier. Take for example the asynchronous interface circuit in Figure 2, which serves simple datacom tasks such as connecting dissimilar communication devices like printers and modems. It uses the 2681/68681 DUART, which interfaces to either an 8- or 16-bit system with relatively few parts; this I/O-mapped Z80 interface requires only an address decoder. The processor's MI signal inhibits

Complex datacom peripheral ICs interface to many processors

the Chip Enable signal during interrupt-acknowledge cycles. A Wait state ensures that the data lines settle before the peripheral reads the data. And as simple as this circuit seems, the Z80/2641 UART interface is even simpler. It also requires only a decoder, but reduces the number of connections to eight data lines, the Chip Enable signal and three address lines for device selection and read/write control.

Compare the simplicity of Figure 2's 8-bit interface to the 16-bit interface in Figure 3. Part of the latter's complexity, however, arises because the DUART takes advantage of the DMA capability provided by the 68430 DMA interface (DMAI). The DMAI provides all the signals necessary to interface to the 68000 as both a peripheral and system master. The control signals drive the bus directly, while five other ICs demultiplex the address/data bus from the DMAI. During a register read/write cycle, U_4 and U_5 function as bi-directional data buffers and U_1 serves as an input buffer for the register address. U_1 to U_3 are active during the DMA operation and drive the memory address onto the bus.

The rest of the circuitry interfaces the DUART as a 68000 peripheral or a DMAI device. The address lines to the DUART come from multiplexer U_6, and the DMAI selects U_6's output with its $\overline{Own}$ signal (Own is an output-control signal asserted during DMA transfers). The controller thus selects between two sets of multiplexer inputs: the address bus and $\overline{Uds}$ (upper data strobe) or a hardwired address.

Because of its two channels, the DUART is normally addressed at even or odd memory locations. To address contiguous memory locations, however, try ANDing the DUART select with Lds or Uds (U_8 and U_9) to generate the DUART Cs signal, and then use Uds for the DUART least significant address. The hardwired address, selected during DMA operations, addresses the transmitter/receiver registers. The most significant bit of this address comes from flip flop U_7, which determines the channel that is accessed. The system sets the flip-flop during the initialization process.

To control the data path to the DUART during system and direct memory access, multiplexer U_{10} gates the DUART's $\overline{Cs}$ and $R/\overline{W}$ signals. The ANDed signals from U_8 and U_9 also enable the proper transceiver buffer for the data to or from the DUART through multiplexer U_{10}. During DMAI operation, RI_W is inverted to the DUART because a memory read is a write to the DUART.

During host access, the system requires a Dtack (data transfer acknowledge) signal at the proper time. For that purpose, U_8 and U_{13} gate the DUART's Dtack signal onto the system bus during host access. Finally, the interrupt request (Intr) asks for a DMA operation by being routed to the DMAI's Req input. When a DMA transfer is in process, the Dtack from the DUART serves as $\overline{Rdy}$ for the DMAI.

Complex datacom peripheral ICs interface to many processors

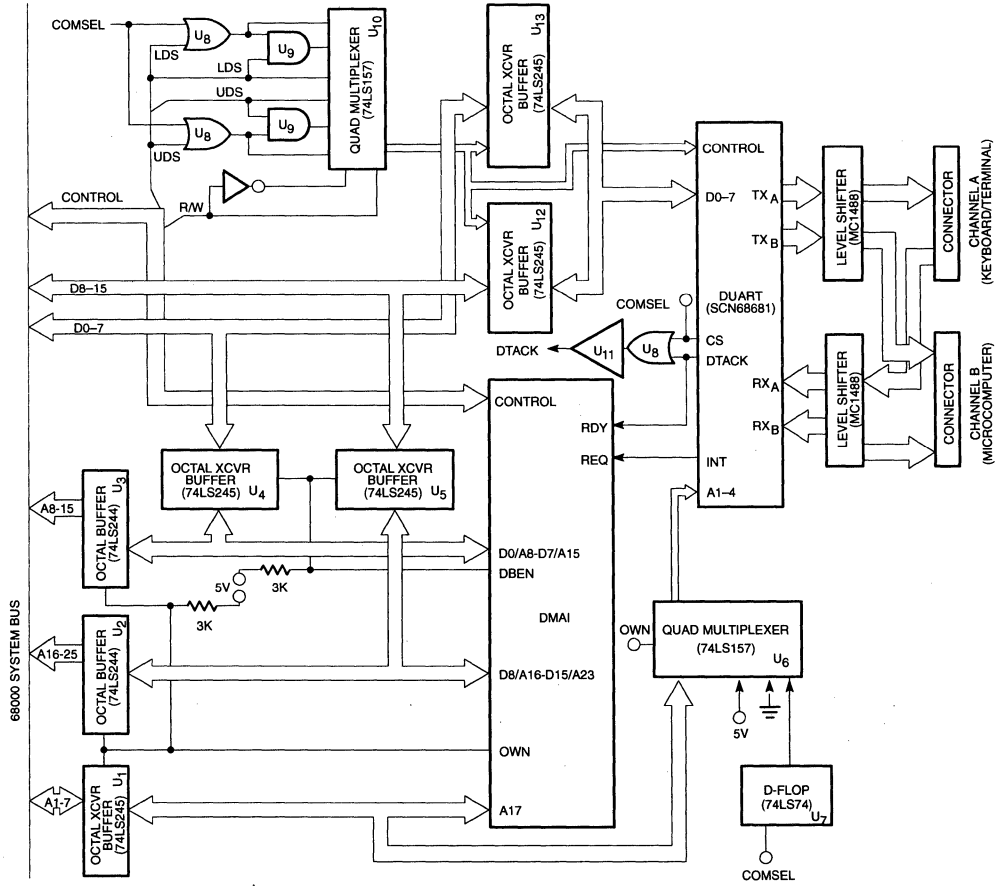


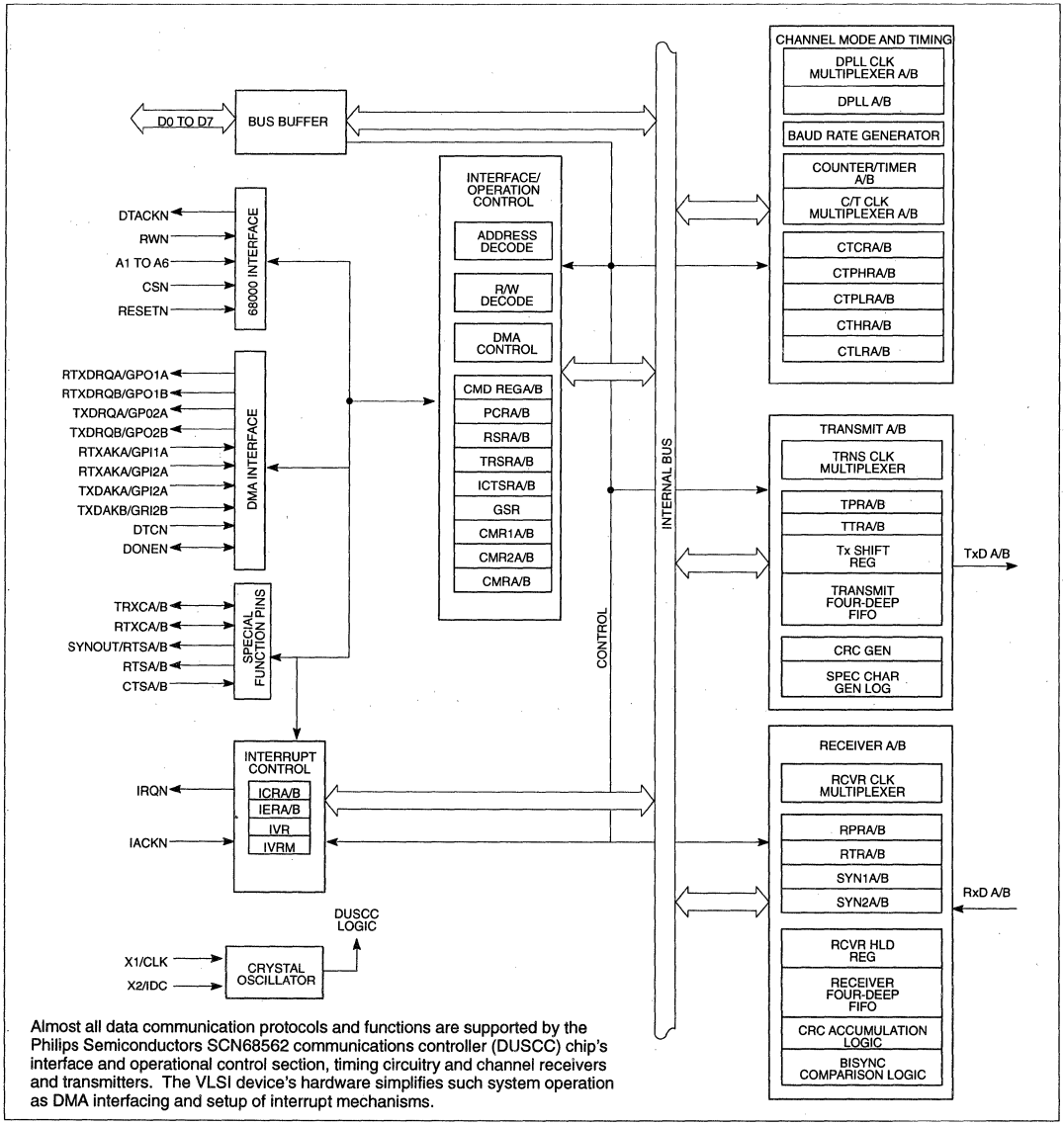
Figure 3 – To add DMA to asynchronous capability with the 2681, add the direct memory access interface (DMAI) to the design. The DMAI provides the control signals necessary to interface to the 68000 as both a peripheral and system master.

Controller contends with multiple protocols

The most widely used data communication protocols are now supported by a single-chip controller that requires minimum external hardware.

The need to transfer large amounts of data at high speed between several different local workstations and large computer systems has generated a variety of message transaction schemes or protocols. While several protocols have evolved, development of dedicated controller ICs to handle them has not kept pace.

A single-chip VLSI device from Philips Semiconductors, the SCN68562 Dual-Channel Universal Synchronous Communications Controller (DUSCC), incorporates circuitry for virtually all subsystems and functions required in advanced data communication systems. The chip provides interfacing to advanced DMA controllers and supports such interrupt structures as vectored, daisy chained, priority, and masked using minimum external logic. In many applications, the DMA and interrupt interfaces are implemented easily through direct connections from the DUSCC's request and acknowledge lines to the control bus.



Almost all data communication protocols and functions are supported by the Philips Semiconductors SCN68562 communications controller (DUSCC) chip's interface and operational control section, timing circuitry and channel receivers and transmitters. The VLSI device's hardware simplifies such system operation as DMA interfacing and setup of interrupt mechanisms.

Controller contends with multiple protocols

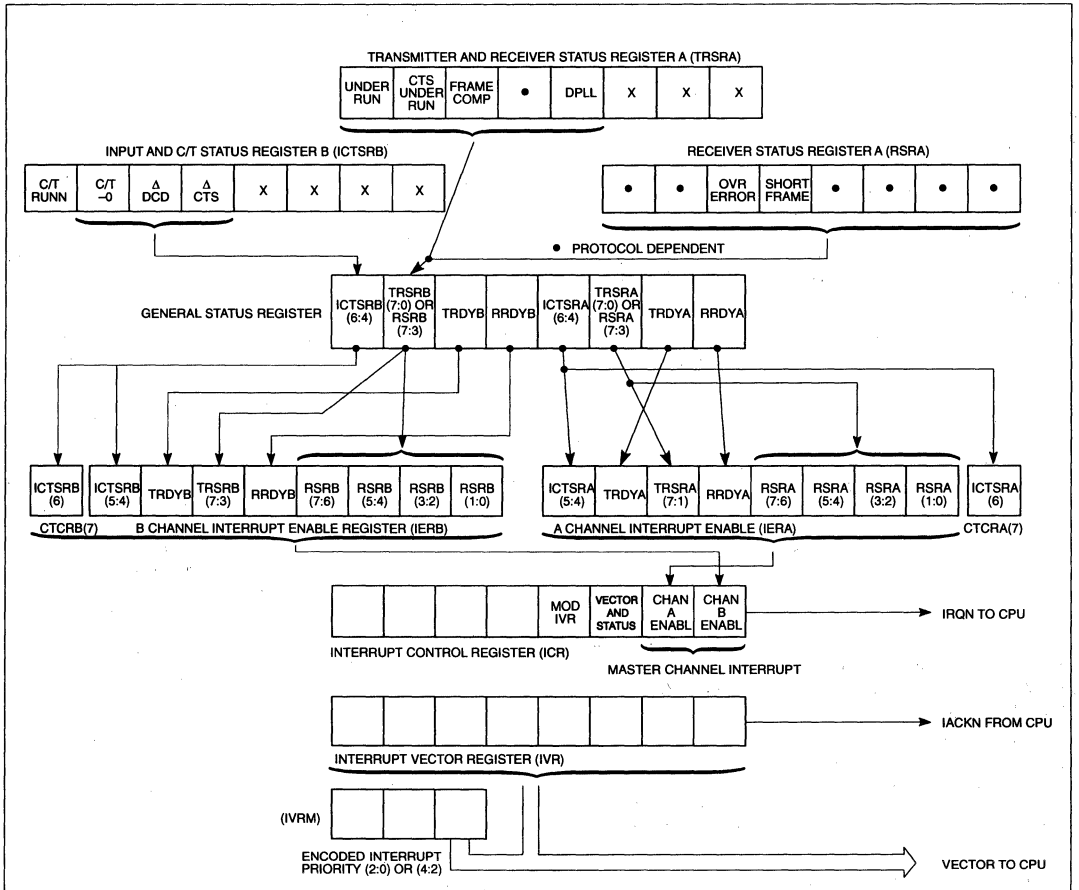
The DUSCC's two independent data communications channels permit substantial programming flexibility for handling multiple protocols. Because of variations in bit- and character-oriented protocols, a controller must provide a more encompassing solution for high performance data communication systems. For example, when the transmitter/receivers can be operated either as full-duplex synchronous or asynchronous channels, the chip can embrace a broad range of advanced bit- and character-oriented protocols, including HDLC/ADCCP, SDLC, X.25, X.75 link level, IBM Bisync, DDCMP, and X.21.

An architectural overview

Architecturally, the DUSCC has four major sub-sections: interface and operational controls, timing circuitry, channel receivers, and channel transmitters. The interface and operational control section handles transactions between the device and its various interfaces, coordinates activities between the other sections, and executes commands. Interface circuitry extends to a host processor, an interrupt structure, the DMA, and multifunction pins.

The host processor interface is dedicated to the complete set of control, data, and bus signals for the 68x and 80x processor families. Eight DMA interface pins can be configured to provide individual DMA request and acknowledge signals for the individual transmitters and receivers. An additional control signal, DONE, provides flow control. For example, it can signify the completion of a message sequence and the termination of DMA operation.

A triple set of registers configures each channel. The channel-mode configuration pair (CMR1 and CMR2) selects the channel protocol/transmission mode, message format, and error-check sequence. The system interface and pin configuration register (PCR) selects the function of the multifunction pins.



A variety of interrupt schemes including vectoring, daisy chaining, and masking can be set up through the DUSCC's interrupt control register (ICR) and interrupt enable register (IER). The ICR determines the relative interrupt priorities of one data communication channel with respect to the other. Channel interrupt conditions are enabled in the IER.

Controller contends with multiple protocols

Interrupt masking can be performed either on individual groups or channel interrupt conditions using the IER, or on an entire channel under control of the ICR. In addition to handling interrupt request and acknowledge signals, the DUSCC provides a mechanism to create interrupt daisy chains using its X2/IDC pin to propagate the interrupt acknowledge signal. Most application timing functions can be derived from the DUSCC's internal timing circuitry. This section consists of independent 16-bit timer/counters and digital phase locked loop (DPLL) circuits for each channel, and a common crystal clock and baud rate generator. Clock signals for the transmitters and receivers can be selected from an external source or from one of the internal sources mentioned above.

The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2/IDC pins or from an external clock connected to the X1/CLK pin. The oscillator's output provides the clock signal for the DUSCC's logic and other internal timing circuits.

The baud rate generator runs off the oscillator signal or on the external signal, generating 16 baud rates simultaneously. These signals are made available to the receiver, transmitter, DPLL, and counter/timer. Since the 16 baud rates are available simultaneously, each receiver and transmitter can select its baud rate independently.

Each channel includes a DPLL that is used in synchronous modes to recover clock information from the received data stream. The DPLL contains a 6-bit counter that is incremented by sampling a clock signal at 32 times the nominal data rate. The clock source can be from an external input, the receiver baud rate, the counter/timer, or the crystal oscillator. The DPLL uses the sampling clock signal together with the received data to construct a data clock that can be used as the DUSCC receiver data clock, transmitter clock or both. This results in a DPLL square wave output clock at a data rate that can be programmed to be sent out on a special pin. Users can select NRZ/NRZI, FM0, FM 1, or Manchester as the encoding format of the received data.

Transmitter/receiver flexibility

Dedicated hardware is integrated within the transmitter and receiver circuits to generate and detect special character sequences, to generate various error sequences and to handle many of the overhead tasks associated with advanced message formats. The large number of operational registers for each channel and the concise set of control commands allow easy setup and operation of the DUSCC.

Each transmitter channel consists of three major sections: clock multiplexer and control registers; TxFIFO and shift register; and special character generation logic. After a channel is configured for a protocol/transmission mode, transmitter operation is refined by the contents of the transmitter parameter register (TPR) and the transmitter timing register (TTR).

The transmitter's clock source is selected from inputs to the transmitter-clock multiplexer. Inputs are the channel counter/timer, the other channel's counter/timer, baud rate generator, DPLL, or an external clock signal. The TPR selects the clock source and baud rate if the baud rate generator is chosen as the transmitter clock signal.

The transmitter accepts parallel character data from the data bus and loads the data into the transmitter FIFO register (TxFIFO), which consists of four 8-bit holding registers. Data is then moved to the transmitter shift register (TxSR), which serializes it according to the transmission format. The TxSR can also be loaded from special character logic or from the cyclic redundancy check/longitudinal redundancy check.

The transmitter-ready signal, TxRDY, indicates the status of the TxFIFO and is set either when an empty position exists in the FIFO or if the entire FIFO is empty. The user can choose the frequency of service requests because the DMA and interrupt service request follow the state of TxRDY.

The receiver architecture is basically similar to that of the transmitter. The receiver consists of a clock multiplexer and control registers, FIFO and shift register, receiver data path, and error accumulation logic. After a channel is configured for the receive mode, receiver operation is refined by the contents of the receiver parameter register (RPR) and receiver timing register (RTR). The RPR selects the number of bits per character and controls operation of an external enable control line for all receiver transmission modes. The interpretation of the remaining bits in the RPR depends on the receive mode selected.

Timing signals are selected from the receiver timing multiplexer. Its inputs are an external timing source, the baud rate generator, channel counter/ timers, and the DPLL output clock. The clock source and data rate selections of the baud rate generator are made through the RTR. This register also selects the DPLL clock source from among counter/timers, external source, baud rate generator, and crystal oscillator inputs.

No single data path can support the diverse requirements of the various transmission modes efficiently. Thus, the DUSCC data path can be viewed as four separate paths — an asynchronous path and three paths to support the requirements of different protocols. Each data path is responsible for assembling characters into the receiver shift receiver (RxSR). After assembly, characters are sent to the receiver FIFO along with appropriate status information.

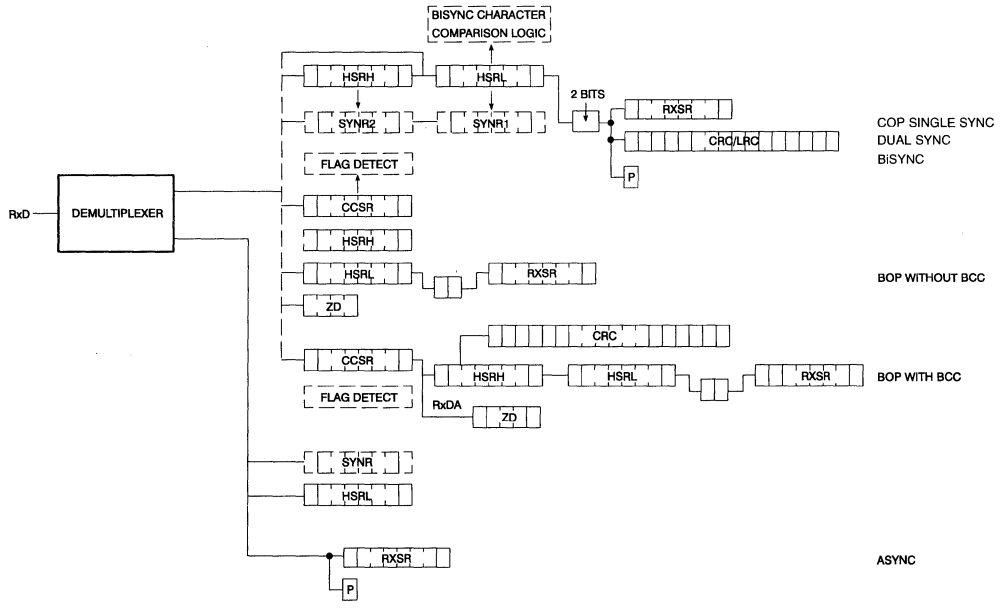
The receiver FIFO consists of four 8-bit holding registers with appended status bits. Data is loaded into the FIFO after a character is assembled; data is removed when a character is read. The state of the receiver FIFO (RxFIFO) is indicated by the receiver ready status signal (RxRDY). As in the operation of the transmitter, a user can choose when the RxRDY bit is set.

Down the data paths

The asynchronous path of the DUSCC is comprised of the holding register (HSRL) and the RxSR in parallel. The HSRL path is active only if a character comparison option is selected. In this case, all incoming data is matched against the contents of the SYN1 register on a bit-by-bit basis to determine a character match. If a match is obtained, a flag in the receiver-status register is set. This feature can be used to generate an interrupt. If the character comparison option is not selected, character data is shifted only to the RxSR. After a character is assembled in the RxSR, it is loaded into the RxFIFO.

Synchronous data paths can be pictured as one of three parallel paths that become active in the following channel conditions: a character-oriented protocol (COP) with or without a block-check character (BCC); a bit-oriented protocol (BOP) without BCC and BOP with BCC. The COP path contains the two 8-bit holding registers (HSRH and HSRL) in series with the shift register, CRC accumulation logic, two synchronizing flip-flops, and special Bisync comparison logic. Data entering this path is held first in either or both of the holding registers. During each bit time, data in the register (or registers) is compared against the contents of either the SYN1 register or the SYN1 and SYN2 registers. Comparison depends on the synchronizing pattern chosen — whether the pattern uses single or dual SYN characters. A match is indicated by the setting of a status bit in the receiver status register (RSR).

Controller contends with multiple protocols



To support the requirements of various protocols, the DUSCC provides a number of internal data paths. One path is asynchronous — the holding register (HSRL) in parallel with receiver shift register (RxSR) configuration at the bottom of the figure — while the other three paths are synchronous. Synchronous paths are used for the bit-oriented protocol (BOP) without CRC, BOP with CRC, and the character-oriented protocol (COP) including BiSYNC data communication protocols.

The BOP without a BCC path uses three parallel inputs to the character comparison (CCSR), HSRH, and HSRL registers, in series with the receiver register. In this arrangement, data is shifted into the three registers simultaneously. The holding pair of shift registers compares their contents with the SYN1 and SYN2 registers to determine if the correct station address has been received. All data entering this path is compared in the CCSR for the flag sequence. When a match occurs, the status bit in the RSR is set. Data entering the HSRL is assembled in character form in the RxSR and then transferred to the FIFO. Zero deletion occurs on all data received unless a flag or abort is detected.

In the case of the BOP with BCC data path, the CCSR, the holding registers, and the RxSR, are arranged in series. The CCSR remains active throughout a message frame and compares the incoming bit stream to determine the flag sequence. The address is compared using the 16-bit holding registers. As character data bits are shifted from the CCSR to the holding register pair, they generate the received BCC character according to the selected accumulation format of the CRC/LRC logic.

In Bisync mode, special comparison logic checks for control sequences and is active for both normal and transparent operation. Comparisons can be made either with EBCDIC or ASCII text messages as selected in the channel mode register. When detected, these sequences cause either a status bit in the RSR to be set or initiate special processing. This comparison logic makes the DUSCC a powerful tool for processing Bisync text. It frees the processor from searching for these special sequences and eliminates the need for additional processing associated with such sequences.

Minimum of hardware

An advanced two-channel data communication system can be implemented with the DUSCC. (The Table depicts the specifications for a typical data communication system supporting the different protocols.) Because so much of the hardware is already in the device, few additional parts are required.

Since the DUSCC provides separate DMA request and acknowledge signals for the transmitter and receiver, the full-duplex requirement for channel A is satisfied with a minimum of hardware between the DMA controllers and the DUSCC.

The complex vectored interrupt scheme for channel B is established by programming the interrupt control register for vectored interrupts and their formats. Separate interrupt vectors can be generated for the transmitter, receiver, and counter/timer by selecting bits in the interrupt control register. An interrupt masking can be performed through the interrupt-enable register. The interrupt interface involves simply connecting the interrupt request and acknowledge signals to the appropriate control bus signals. No additional hardware is necessary to complete this portion of the design.

A minimum of design is required to select the various interfaces for both channels. For channel A, five registers are used to select the channel interfaces and to set up the protocol requirements. Channel-configuration registers CMR1 and CMR2 establish the DMA structure and define operation of the data channel. External

Controller contends with multiple protocols

inputs are defined by the pin-control register and the address of the secondary station is stored in the SYN1 and SYN2 registers. Channel B is set up just as easily. But it requires additional programming of the interrupt control and enable registers to establish the interrupt structure.

Operating refinements for each channel are made through the transmitter and receiver parameter registers (TPR and RTR). These define the message format and select automatic features that are invoked under various transmitter and receiver conditions. The channel A transmitter, for example, is set up to terminate the BOP message automatically by sending an end of message sequence and then mark the data line when an underrun occurs. In similar fashion, channel B is set up to linefill with a sync pattern until another character is loaded into the transmitter when an underrun occurs. These actions do not require the intervention of the host processor.

Once the interfaces are established, transmitter and receiver operations are controlled and monitored through the command and the transmitter/receiver status registers. The DUSCC provides a set of commands that directly supports transmission of Bisync and BOP messages. Each command performs an action necessary to generate a message in the specific protocol. In Bisync, the first character of a message after the SYN pattern is an SOH, STX, or DLE-STX pattern. The send-DLE command not only sends the DLE-STX sequence, but the command can be appended to any character to transmit special control sequences as the protocol requires.

In BOP mode, the message frame after the flag character consists of 0 to n address bytes, followed by 1 or 2 control bytes. The sequence is transmitted by loading the data into the transmitter FIFO. After the last control byte, the transmitter switches automatically to the programmed character length. A feature of the transmitter is its ability to send the last character for a bit count less than the programmed character length by specifying a shorter character length in the output/miscellaneous register.

Section 2
Digital Data Communications Data Sheets

CONTENTS

Asynchronous Communication Product Line (UARTs)

Device	Technology Description	Package Type(s)	Icc mA @ Vcc = 5V	Temp Range deg C	Speed	Buffer Rx/Tx FIFO	Interrupt	Misc Pins I,O,I/O	16 Bit Counter Timer	Key Features
SCN2681	NMOS DUART	PDIP24,28 PDIP40 PLCC44	150	0 to +70 −40 to +85	Std. 50 to 38.4kHz 16x Ext. 880 to 125kHz 16x 0 to 1MHz 1x	4/2	Normal	7,8,0	1	• Basic feature set
SCN2681T	NMOS DUART	PDIP40 PLCC44	150	0 to +70	Std. 50 to 38.4kHz 16x Ext. 880 to 500kHz 16x 0 to 1MHz 1x	4/2	Normal	7,8,0	1	• Basic feature set • High speed version of SCN2681
SCN68681	NMOS DUART	PDIP40 PLCC44	150	0 to +70 −40 to +85	Std. 50 to 38.4kHz 16x Ext. 880 to 125kHz 16x 0 to 1MHz 1x	4/2	Normal Vectored IACK/DACK	6,8,0	1	• Basic feature set • Motorola interface compatible, version of SCN2681
SCC2691	CMOS UART	PDIP24 PDIP28 PSOL24	2	0 to +70 −40 to +85	Std. 50 to 38.4kHz 16x Ext. 880 to 125kHz 16x 0 to 1MHz 1x	4/2	Normal	1,1,0	1	• Basic feature set • SOL package has very small footprint • Single channel version of SCC2692
SCC2692	CMOS DUART	PDIP28 PDIP40 PLCC44	10	0 to +70 −40 to +85	Std. 50 to 38.4kHz 16x Ext. 880 to 125kHz 16x 0 to 1MHz 1x	4/2	Normal	7,8,0	1	• Basic feature set • CMOS version of SCN2681 • Counter timer can be used as receiver watch dog
SCC68692	CMOS DUART	PDIP28 PDIP40 PLCC44	10	0 to +70 −40 to +85	Std. 50 to 38.4kHz 16x Ext. 880 to 125kHz 16x 0 to 1MHz 1x	4/2	Normal Vectored IACK/DACK	6,8,0	1	• Basic feature set • Motorola interface compatible, CMOS version of SCN68681 • Counter timer can be used as receiver watch dog
SC26C92	CMOS DUART	PDIP40 PLCC44	25	0 to +70	Std. 50 to 38.4kHz 16x Ext. 880 to 1MHz 16x 0 to 1MHz 1x	9/9	Normal Multi level	7,8,0	1	• Enhanced faster version of SCC2692 • Watchdog timers for each receiver • Deeper FIFOs with interrupts on 4 levels
SC26C94 SC68C94	CMOS QUART	PDIP48 PLCC52	50	0 to +70 −40 to +85	Std. 50 to 38.4kHz 16x Ext. 880 to 1MHz 16x 0 to 1MHz 1x	9/9	Normal Vectored IACK/DACK	0,0,16	2	• Enhanced quad version of SC2692 • Versatile, programmable high speed interrupt controller • Watch dog timers for each receiver • 8 level FIFO interrupt
SCC2698B	CMOS OCTART	PDIP48 PLCC52	30	0 to +70 −40 to +85	Std. 50 to 38.4kHz 16x Ext. 880 to 1MHz 16x 0 to 1MHz 1x	4/2	Normal	16,8,16	4	• Basic feature set • 8 independent channels arranged as 4x SCC2692 on a single chip
SC26C198 SC68C198 SC26L198 SC68L198	CMOS OCTART	PLCC84	120	0 to +70 −40 to +85	Std. 50 to 500kHz 16x Ext. 880 to 1MHz 16x 0 to 1MHz 1x	16/16	Normal Vectored IACK/DACK	0,0,32	0	• New design with Basic feature set and many enhancements • Available as C198 for 5V: CMOS/TTL (33MHz) or 3.3V: CMOS (20MHz) and as L198 for 3.3V: CMOS/TTL (25MHz) • Xon/Xoff in band flow control, 3 byte character recognition • Asynchronous, Synchroncus bus operation up to 33MHz @ 5V • Bus cycle 120ns, data release time 30ns @ 5 Volt • Two 16 bit odd baud rate generators

Basic Feature Set			
	• All Philips Semiconductors UARTs are full duplex on all channels • All receivers and transmitters are fully independent with respect to clock speed, clock source and operation mode	• All UARTs have individual interrupt status • Counter timers have independent programmable clock source and dual mode • Each UART has its own modem or flow control	• All UARTs have wake-up mode for multi drop support • All CMOS devices have power-down mode • All UARTs have Programmable data formats, channel modes

Synchronous Communication Product Line

Device	Technology Description	Package Type(s)	Icc mA @ Vcc = 5V	Temp Range deg C	Speed	Key Features
SCN2651	NMOS Programmable Communication Interface (PCI)	PDIP28 PLCC28	150	0 to +70 –40 to +85	0–1Mbps data rate 16 internal baud rates (50 to 19.2K) external BRG	• Synchronous/asynchronous operation (full/half duplex) • 5–8 bit character (1, 1.5, 2 stop bits in asynchronous mode) • Odd, even, no parity in asynchronous mode • Single or dual SYN, transparent and non-transparent auto SYN/DLE insertion/deletion in synchronous operations • Double buffer transmit and receive operation
SCN2661 **SCN68661**	NMOS Enhanced Programmable Communication Interface (PCI)	PDIP28 PLCC28	150	0 to +70 –40 to +85	19 internal baud rates (50 to 38.4K)	• Functionally it is an enhanced version of SCN2651 • Available in three different baud rate versions • Enhanced for BREAK detect and external jam sync, DLE detect, SYN1 stripping, drop RTS, stop bit search and data bus timing/drivers
SCN2652 **SCN68652**	NMOS Enhanced Programmable Communication Interface (PCI)	PDIP40 PLCC44	150	0 to +70 –40 to +85	0–2Mbps data rate	• Supports synchronous Bit Oriented (SDLC, ADCCP, HDLC) and Character Oriented (DDCMP, DISYNC) Protocols • SYNC Generation, detection in BCP and Auto Zero insertion/deletion in BOP modes • Programmable 8 or 16 bit data bus • Full/half duplex transmit and receive operation
SCC26562 **SCN68562**	NMOS DUAL Universal Serial Communication Controller (DUSCC)	PDIP48 PLCC52	275	0 to +70	0–4Mbps data rate 16 internal baud rates (50 to 38.4K) Internal DPLL and counters	• Dual channel synchronous and asynchronous operation • Bit Oriented (HDLC, SDLC, X.25/75) and Character Oriented (BISYNC, DDCMP) Protocols • Parity and Frame Check Sequence (FCS) generation/checking • Poll, Interrupt, Vectored Interrupt, Modified Vector Interrupt, DMA and Wait Data Transfer modes • Data coding/encoding modes: NRZ, NRZI, FM0, FM1, Manchester • On-chip oscillator (16MHz), 16 bit counter/timer, DPLL • Modern control inputs/outputs and external synchronous pin • 4 byte receiver and transmitter FIFOs and Rx/Tx shift registers for each channel • Rx overrun and Tx underrun controls • Full/half duplex transmit and receive operation
SC26C562 **SC68C562**	CMOS DUAL Universal Serial Communication Controller (CDUSCC)	PDIP48 PLCC52	80	PDIP48 0 to +70 PLCC52 0 to +70 –40 to +85	0–1Mbps data rate 19 internal baud rates (50 to 64K) Internal DPLL and counters	• Functionally it is an enhancement of SCN26562/68562 • Faster transmit/receive data rate (10MHz) • 16 byte deep Tx/Rx FIFOs • 170ns bus cycle • More and higher internal BRG selections • Better control over individual interrupt conditions • Supports X.21 pattern recognition • Provides more Tx/Rx status information

Programmable communications interface (PCI) SCN2651

DESCRIPTION

The Philips Semiconductors SCN2651 PCI is a universal synchronous/asynchronous data communications controller chip designed for microcomputer systems. It interfaces directly to the Philips Semiconductors SCN2650 microprocessor and may be used in a polled or interrupt driven system environment. The SCN2651 accepts programmed instructions from the microprocessor and supports many serial data communication disciplines, synchronous and asynchronous, in the full or half-duplex mode.

The PCI serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

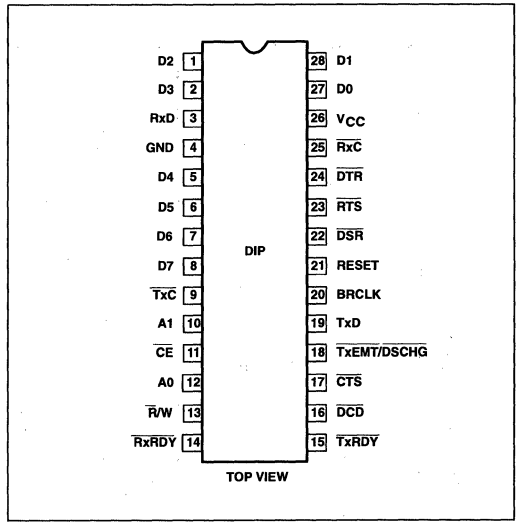
The SCN2651 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode.

The PCI is constructed using Philips Semiconductors n-channel silicon gate depletion load technology and is packaged in a 28-pin DIP.

FEATURES

- Synchronous operation
  - 5- to 8-bit characters
  - Single or double SYN operation
  - Internal character synchronization
  - Transparent or non-transparent mode
  - Automatic SYN or DLE-SYN insertion
  - SYN or DLE stripping
  - Odd, even, or no parity
  - Local or remote maintenance loopback mode
  - Baud rate: DC to 1Mbps (1X clock)
- Asynchronous operation
  - 5- to 8-bit characters
  - 1, 1-1/2 or 2 stop bits
  - Odd, even, or no parity
  - Parity, overrun and framing error detection
  - Line break detection and generation
  - False start bit detection
  - Automatic serial echo mode
  - Local or remote maintenance loopback mode
  - Baud rate: DC to 1Mbps
    (1X clock)
    DC to 62.5kbps (16X clock)
    DC to 15.625kbps
    (64X clock)

PIN CONFIGURATIONS



OTHER FEATURES

- Internal or external baud rate clock
- 16 internal rates – 50 to 19,200 baud
- Double buffered transmitter and receiver
- Full or half duplex operation
- TTL compatible inputs and outputs
- Single 5V power supply
- No system clock required
- 28-pin dual in-line package

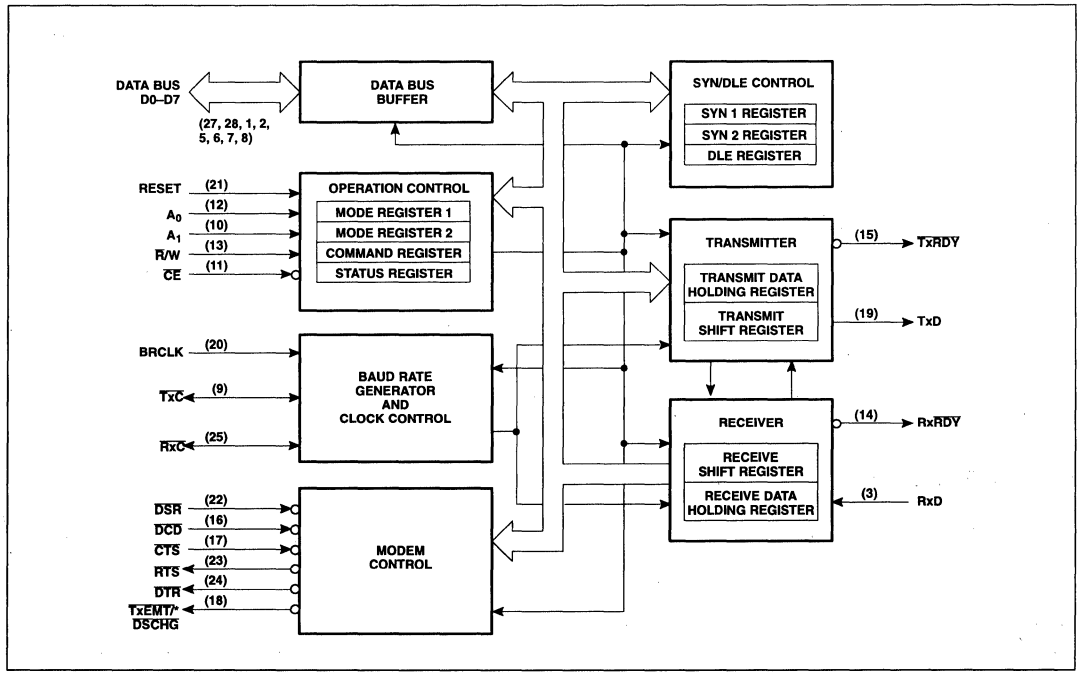
APPLICATIONS

- Intelligent terminals
- Network processors
- Front-end processors
- Remote data concentrators
- Computer to computer links
- Serial peripherals

ORDERING CODE

PACKAGES	V_{CC} = 5V ±5%		DWG #
	Commercial 0°C to +70°C	Automotive -40°C to +85°C	
28-Pin Plastic Dual In-Line Package (DIP)	SCN2651CC1N28	Not available	0413B

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature[2]	Note 4	°C
T_{STG}	Storage temperature	-65 to +150	°C
	All voltages with respect to ground[3]	-0.5 to +6.0	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effect of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over operating temperature range unless otherwise specified. See ordering code table for applicable temperature range and operating supply range.

CAPACITANCE

T_A = 25°C, V_{CC} = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Capacitance						
C_{IN} C_{OUT} $C_{I/O}$	Input Output Input/Output	f_C = 1MHz Unmeasured pins tied to ground			20 20 20	pF pF pF

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
Output voltage						
V_{OL}	Low	I_{OL} = 1.6mA			0.4	V
V_{OH}	High	I_{OH} = -100µA	2.4			V
I_{IL}	Input leakage current	V_{IN} = 0 to 5.25V	-10		10	µA
3-State output leakage current						
I_{LH}	Data bus high	V_O = 4.0V	-10		10	µA
I_{LL}	Data bus low	V_O = 0.45V	-10		10	µA
I_{CC}	Power supply current				150	mA

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified. See ordering code table for applicable temperature range and operating supply range.
2. All voltage measurements are referenced to ground. All time measurements are at the 50% level for inputs (except t_{BRH} and t_{BRL}) and at 0.8V and 2.0V for outputs. Input levels for testing are 0.45V and 2.4V.
3. Typical values are at +25°C, typical supply voltages and typical processing parameters.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Pulse width						
t_{RES}	Reset		1000			ns
t_{CE}	Chip enable		300			ns
Set-up and hold time						
t_{AS}	Address setup		20			ns
t_{AH}	Address hold		20			ns
t_{CS}	R/$\overline{W}$ control setup		20			ns
t_{CH}	R/$\overline{W}$ control hold		20			ns
t_{DS}	Data setup for write		225			ns
t_{DH}	Data hold for write		0			ns
t_{RXS}	RX data setup		300			ns
t_{RXH}	RX data hold		350			ns
t_{DD}	Data delay time for read	C_L = 100pF			250	ns
t_{DF}	Data bus floating time for read	C_L = 100pF			150	ns
t_{CED}	$\overline{CE}$ to $\overline{CE}$ delay		700			ns
Input clock frequency						
f_{BRG}	Baud rate generator		1.0	5.0688	5.0738	MHz
$f_{R/T}$[6]	$\overline{TxC}$ or $\overline{RxC}$		dc		1.0	MHz
Clock width						
t_{BRH}[5]	Baud rate high		70			ns
t_{BRL}[5]	Baud rate low		70			ns
$t_{R/TH}$	$\overline{TxC}$ or $\overline{RxC}$ high		500			ns
$t_{R/TL}$[6]	$\overline{TxC}$ or $\overline{RxC}$ low		500			ns
t_{TXD}	TxD delay from falling edge of $\overline{TxC}$	C_L = 100pF			650	ns
t_{TCS}	Skew between TxD changing and falling edge of $\overline{TxC}$ output[4]	C_L = 100pF		0		ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified. See ordering code table for applicable temperature range and operating supply range.
2. All voltage measurements are referenced to ground. All time measurements are at the 50% level for inputs (except t_{BRH} and t_{BRL}) and at 0.8V and 2.0V for outputs. Input levels for testing are 0.45V and 2.4V.
3. Typical values are at +25°C, typical supply voltages and typical processing parameters.
4. Parameter applies when internal transmitter clock is used.
5. Under test conditions of 5.0688MHz, f_{BRG}, t_{BRH}, and t_{BRL} measured at V_{IH} and V_{IL} respectively.
6. $t_{R/T}$ and $t_{R/TL}$ shown for all modes except local loopback. For local loopback mode $f_{R/T}$ = 0.7MHz and $t_{R/TL}$ = 700ns min.

PIN DESCRIPTION

Pin No.	Symbol	Name and Function	Type
27, 28, 1, 2, 5-8	$D0 - D_7$	8-Bit data bus	I/O
21	RESET	Reset	I
12, 10	A_0–A_1	Internal register select lines	I
13	$\overline{R/W}$	Read or write command	I
11	$\overline{CE}$	Chip enable input	I
22	$\overline{DSR}$	Data set ready	I
24	$\overline{DTR}$	Data terminal ready	O
23	$\overline{RTS}$	Request to send	O
17	$\overline{CTS}$	Clear to send	I
16	$\overline{DCD}$	Data carrier detected	I
18	$\overline{TxEMT/DSCHG}$	Transmitter empty or data set change	O
9	$\overline{TxC}$	Transmitter clock	I/O
25	$\overline{RxC}$	Receiver clock	I/O
19	TxD	Transmitter data	O
3	RxD	Receiver data	I
15	$\overline{TxRDY}$	Transmitter ready	O
14	$\overline{RxRDY}$	Receiver ready	O
20	BRCLK	Baud rate generator clock	I
26	V_{CC}	+5V supply	I
4	GND	Ground	I

Table 1. Baud Rate Generator Characteristics Crystal Frequency = 5.0688MHz

Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Divisor
50	0.8kHz	0.8kHz	–	6336
75	1.2	1.2	–	4224
110	1.76	1.76	–	2880
134.5	2.152	2.1523	0.016	2355
150	2.4	2.4	–	2112
300	4.8	4.8	–	1056
600	9.6	9.6	–	528
1200	19.2	19.2	–	264
1800	28.8	28.8	–	176
2000	32.0	32.081	0.253	158
2400	38.4	38.4	–	132

NOTE: *Error at 19200 can be reduced to zero by using crystal frequency 4.9152MHz. 16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X.

BLOCK DIAGRAM

The PCI consists of six major sections. These are the transmitter, receiver, timing, operation control, modem control and SYN/DLE control. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

Operation Control

This functional block stores configuration and operation commands from the CPU and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus and contains mode registers 1 and 2, the command register, and the status register. Details of register addressing and protocol are presented in the PCI programming section of this data sheet.

Timing

The PCI contains a baud rate generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full-duplex operation. See Table 1.

Receiver

The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU.

Transmitter

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Modem Control

The modem control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modem.

SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the CPU. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

INTERFACE SIGNALS

The PCI interface signals can be grouped into two types: the CPU-related signals (shown in Table 2), which interface the SCN2651 to the microprocessor system, and the device-related signals (shown in Table 3), which are used to interface to the communications device or system.

OPERATION

The functional operation of the SCN2651 is programmed by a set of control words supplied by the CPU. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the PCI programming section of the data sheet.

After programming, the PCI is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the CPU to a serial bit stream. These actions are accomplished within the framework specified by the control words.

Receiver

The SCN2651 is conditioned to receive data when the $\overline{DCD}$ input is low and the RxEN bit in the command register is true. In the asynchronous mode, the receiver looks for a high to low transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit-time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and one stop bit(s) have been assembled. The data is then transferred to the receive data holding register, the RxRDY bit in the status register is set, and the $\overline{RxRDY}$ output is asserted. If the character length is less than 8 bits, the high order unused bits in the holding register are set to zero. The parity error, framing error, and overrun error status bits are strobed into the status register on the positive going edge of $\overline{RxC}$ corresponding to the received character boundary. If a break condition is detected (RxD is low for the entire character as well as the stop bit[s]), only one character consisting of all zeros (with the FE status bit set) will be transferred to the holding register. The RxD input must return to a high condition before a search for the next start bit begins.

When the PCI is initialized into the synchronous mode, the receiver first enters the hunt mode on a 0 to 1 transition of RxEN (CR2). In this mode, as data is shifted into the receiver shift register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly mode begins. If single SYN operation is programmed, the SYN detect status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN detect bit to be set. Otherwise, the PCI returns to the hunt mode. (Note that the sequence SYN1–SYN1–SYN2 will not achieve synchronization.) When synchronization has been achieved, the PCI continues to assemble characters and transfer them to the holding register, setting the RxRDY status bit and asserting the $\overline{RxRDY}$ output each time a character is transferred. The PE and OE status bits are set as appropriate. Further receipt of the appropriate SYN sequence sets the SYN detect status bit. If the SYN stripping mode is

Table 2. CPU-Related Signals

PIN NAME	PIN NO.	INPUT/ OUTPUT	FUNCTION
V_{CC}	26	I	+5V supply input
GND	4	I	Ground
RESET	21	I	A high on this input performs a master reset on the SCN2651. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.
$A_1 - A_0$	10, 12	I	Address lines used to select internal PCI registers.
$\overline{R/W}$	13	I	Read command when low, write command when high.
$\overline{CE}$	11	I	Chip enable command. When low, indicates that control and data lines to the PCI are valid and that the operation specified by the $\overline{RW}$, A_1 and A_0 inputs should be performed. When high, places the D_0–D_7 lines in the 3-State condition.
$D_7 - D_0$	8, 7, 6, 5, 2, 1, 28, 27	I/O	8-bit, three-state data bus used to transfer commands, data and status between PCI and the CPU. D_0 is the least significant bit, D_7 the most significant bit.
$\overline{TxRDY}$	15	O	This output is the complement of status register bit SR0. When low, it indicates that the transmit data holding register (THR) is ready to accept a data character from the CPU. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{RxRDY}$	14	O	This output is the complement of status register bit SR1. When low, it indicates that the receive data holding register (RHR) has a character ready for input to the CPU. It goes high when the RHR is read by the CPU, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{TxEMT/DSCHG}$	18	O	This output is the complement of status register bit SR2. When low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This output goes high when the status register is read by the CPU, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the CPU for this line to go high. It is an open drain output which can be used as an interrupt to the CPU.

Table 3. Device-Related Signals

PIN NAME	PIN NO.	INPUT/O UTPUT	FUNCTION
BRCLK	20	I	5.0688MHz clock input to the internal baud rate generator. Not required if external receiver and transmitter clocks are used.
$\overline{RxC}$	25	I/O	Receiver clock. If external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin becomes an output at 1X the programmed baud rate.*
$\overline{TxC}$	9	I/O	Transmitter clock. If external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. The transmitted data changes on the falling edge of the clock. If internal transmitter clock is programmed, the pin becomes an output at 1X the programmed baud rate.*
RxD	3	I	Serial data input to the receiver. "Mark" is high, "Space" is low.
TxD	19	O	Serial data output from the transmitter. "Mark" is high, "space" is low. Held in mark condition when the transmitter is disabled.
$\overline{DSR}$	22	I	General purpose input which can be used for data set ready or ring indicator condition. Its complement appears as status register bit SR7. Causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes.
$\overline{DCD}$	16	I	Data carrier detect input. Must be low in order for the receiver to operate. Its complement appears as status register bit SR6. Causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes.
$\overline{CTS}$	17	I	Clear to send input. Must be low in order for the transmitter to operate. If it goes high during transmission, the character in the transmit shift register will be transmitted before termination.
$\overline{DTR}$	24	O	General purpose output which is the complement of command register bit CR1. Normally used to indicate data terminal ready.
$\overline{RTS}$	23	O	General purpose output which is the complement of command register bit CR5. Normally used to indicate request to send.

NOTE: *$\overline{RxC}$ and $\overline{TxC}$ outputs have short circuit protection max. C_L = 100pF

commanded, SYN characters are not transferred to the Holding Register. Note that the SYN characters used to establish initial synchronization are not transferred to the holding register in any case.

Transmitter

The PCI is conditioned to transmit data when the $\overline{CTS}$ input is Low and the TxEN command register bit is set. The SCN2651 indicates to the CPU that it can accept a character for transmission by setting the TxRDY status bit and asserting the $\overline{TxRDY}$ output. When the CPU writes a character into the transmit data holding register, these conditions are negated. Data is transferred from the holding register to the transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the transmit holding register, the TxD output remains in the marking (high) condition and the $\overline{TxEMT/DSCHG}$ output and its corresponding status bit are asserted. Transmission resumes when the CPU loads a new character into the holding register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the send break command bit high.

In the synchronous mode, when the SCN2651 is initially conditioned to transmit, the TxD output remains high and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the CPU. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity, if commanded) are generated by the PCI unless the CPU fails to send a new character to the PCI by the time the transmitter has completed sending the previous character.

Since synchronous communication does not allow gaps between characters, the PCI asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, SYN1–SYN2 doublets, or DLE–SYN1 doublets, depending on the state of MR16 and MR17. Normal transmission of the message resumes when a new character is available in the transmit data holding register. If the send DLE bit in the command register is true, the DLE character is automatically transmitted prior to transmission of the message character in the THR.

PCI PROGRAMMING

Prior to initiating data communications, the SCN2651 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The PCI can be reconfigured at any time during program execution. However, if the change has an effect on the reception of a character the receiver should be disabled. Alternatively if the change is made 1 1/2 RxC periods after RxRDY goes active it will affect the next character assembly. A flowchart of the initialization process appears in Figure 1.

The internal registers of the PCI are accessed by applying specific signals to the $\overline{CE}$, $\overline{R}/W$, A_1 and A_0 inputs. The conditions necessary to address each register are shown in Table 4.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions $A_1 = 0$, $A_0 = 1$, and $\overline{R}/W = 1$. The first operation loads the SYN1 register. The next loads the SYN2 register, and the third loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses mode register 1, and a subsequent operation addresses mode register 2. If more than the

required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 register and mode register 1 by a RESET input or by performing a "read command register" operation, but are unaffected by any other read or write operation.

The SCN2651 register formats are summarized in Tables 5, 6, 7 and 8. Mode registers 1 and 2 define the general operational characteristics of the PCI, while the command register controls the operation within this basic framework. The PCI indicates its status in the status register. These registers are cleared when a RESET input is applied.

Mode Register 1 (MR1)

Table 5 illustrates mode register 1. Bits MR11 and MR10 select the communication format and baud rate multiplier. 00 specifies synchronous mode and 1X multiplier. 1X, 16X, and 64X multipliers are programmable for asynchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7, or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14.

In asynchronous mode, MR17 and MR16 select character framing of 1, 1.5, or 2 stop bits. (If 1X baud rate is programmed, 1.5 stop bits default to 1 stop bit on transmit.) In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17 = 1, and SYN1–SYN2 is used when MR17 = 0. If the transparent mode is specified by MR16, DLE–SYN1 is used for character fill and SYN detect, but he normal synchronization sequence is used. Also DLE stripping and DLE detect (with MR14 = 0) are enabled.

Mode Register 2 (MR2)

Table 6 illustrates mode register 2. MR23, MR22, MR21, and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable. When driven by a 5.0688MHz input at the BRCLK input (Pin 20), the BRG output has zero error except at 134.5 2000, and 19,200 baud, which have errors of +0.016%, +0.235%, and +3.125% respectively.

MR25 and MR24 select either the BRG or the external inputs $\overline{TxC}$ and $\overline{RxC}$ as the clock source for the transmitter and receiver, respectively. If the BRG clock is selected, the baud rate factor in asynchronous mode is 16X regardless of the factor selected by MR11 and MR10. In addition, the corresponding clock pin provides an output at 1X the baud rate.

Table 4. SCN2651 Register Addressing

$\overline{CE}$	A_1	A_0	$\overline{R/W}$	FUNCTION
1	X	X	X	3-State data bus
0	0	0	0	Read receive holding register
0	0	0	1	Write transmit holding register
0	0	1	0	Read status register
0	0	1	1	Write SYN1/SYN2/DLE registers
0	1	0	0	Read mode registers 1/2
0	1	0	1	Write mode registers 1/2
0	1	1	0	Read command register
0	1	1	1	Write command register

NOTE: See AC Characteristics section for timing requirements.

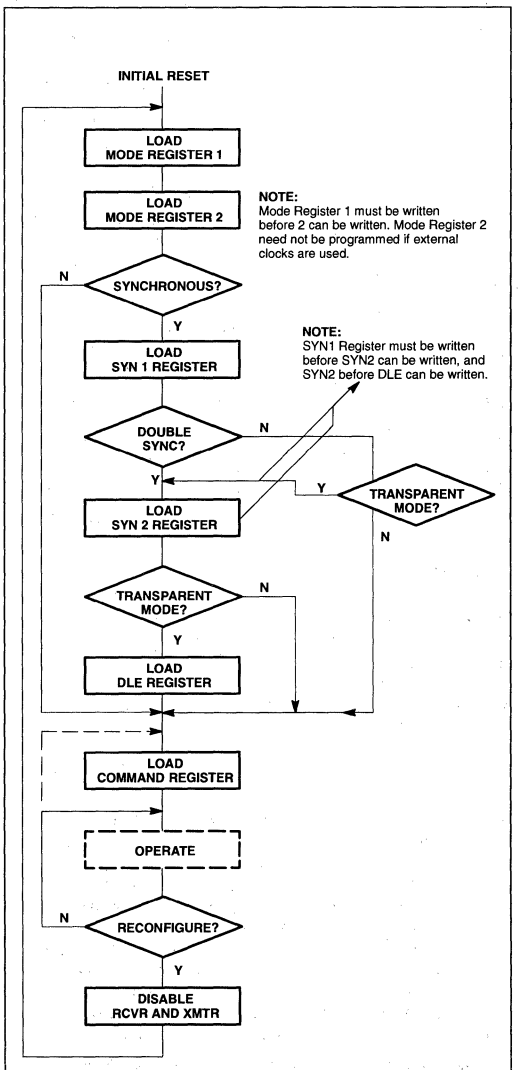


Figure 1. SCN2651 Initialization Flowchart

Table 5. Mode Register 1 (MR1)

MR17	MR16	MR15	MR14	MR13	MR12	MR11	MR10
		Parity Type	**Parity Control**	**Character Length**		**Mode and Baud Rate Factor**	
Async: Stop bit length 00 = Invalid 01 = 1 Stop bit 10 = 1 1/2 Stop bits 11 = 2 Stop bits		0 = Odd 1 = Even	0 = Disabled 1 = Enabled	00 = 5 Bits 01 = 6 Bits 10 = 7 Bits 11 = 8 Bits		00 = Synchronous 1X rate 01 = Asynchronous 1X rate 10 = Asynchronous 16X rate 11 = Asynchronous 64X rate	
Sync: Number of SYN char 0 = Double SYN 1 = Single SYN	**Sync: Transparency control** 0 = Normal 1 = Transparent						

NOTE:
Baud rate factor in asynchronous applies only if external clock is selected. Factor is 16X if internal clock is selected. Mode must be selected (MR11, MR10) in any case.

Table 6. Mode Register 2 (MR2)

MR27	MR26	MR25	MR24	MR23	MR22	MR21	MR20
		Transmitter Clock	**Receiver Clock**	**Baud Rate Selection**			
Not used		0 = External 1 = Internal	0= External 1 = Internal	0000 = 50 Baud 0001 = 75 0010 = 110 0011 = 134.5 0100 = 150 0101 = 300 0110 = 600 0111 = 1200		1000 = 1800 Baud 1001 = 2000 1010 = 2400 1011 = 3600 1100 = 4800 1101 = 7200 1110 = 9600 1111 = 19,200	

Table 7. Command Register (CR)

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode		**Request to Send**	**Reset Error**		**Receive Control (RxEN)**	**Data Terminal Ready**	**Transmit Control (TxEN)**
00 = Normal operation 01 = Async: automatic echo mode Sync: SYN and/or DLE stripping mode 10 = Local Loopback 11 = Remote Loopback		0 = Force $\overline{RTS}$ output high 1 = Force $\overline{RTS}$ output low	0 = Normal 1 = Reset error flag in status reg (FE, OE, PE/DLE DETECT)	**Async: Force Break** 0 = Normal 1 = Force break **Sync Send DLE** 0 = Normal 1 = Send DLE	0 = Disable 1 = Enable	0 = Force $\overline{DTR}$ output high 1 = Force $\overline{DTR}$ output low	0 = Disable 1 = Enable

Command Register (CR)

Table 7 illustrates the command register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. A 0 to 1 transition of CR2 forces start bit search (async mode) or hunt mode (sync mode) on the second $\overline{RxC}$ rising edge. Disabling the receiver causes $\overline{RxRDY}$ to go high (inactive). If the transmitter is disabled, it will complete the transmission of the character in the transmit shift register (if any) prior to terminating operation. The TxD output will then remain in the marking state (high) while $\overline{TxRDY}$ and $\overline{TxEMT}$ will go high (inactive). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected.

Bits CR1 (DTR) and CR5 (RTS) control the $\overline{DTR}$ and $\overline{RTS}$ outputs. Data at the outputs is the logical complement of the register data.

In asynchronous mode, setting CR3 will force and hold the TxD output low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go high for at least one bit time before beginning transmission of the next character in the transmit data holding register. In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the transmit data holding register. CR3 should be reset in response to the next TxRDY.

Table 8. Status Register (SR)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
Data Set Ready	**Data Carrier Detect**	**FE/SYN Detect**	**Overrun**	**PE/DLE Detect**	**TxEMT/ DSCHG**	**RxRDY**	**TxRDY**
0 = $\overline{DSR}$ input is high 1 = $\overline{DSR}$ input is low	0 = $\overline{DCD}$ input is high 1 = $\overline{DCD}$ input is low	**Async:** 0 = Normal 1 = Framing ERROR **Sync:** 0 = Normal 1 = SYN char detected	0 = Normal 1 = Overrun error	**Async:** 0 = Normal 1 = Parity error **Sync:** 0 = Normal 1 = Parity error or DLE char received	0 = Normal 1 = Change in $\overline{DSR}$ or $\overline{DCD}$, or transmit shift register is empty	0 = Receive holding register empty 1 = Receive holding register has data	0 = Transmit holding register busy 1 = Transmit holding register empty

Setting CR4 causes the error flags in the status register (SR3, SR4, and SR5) to be cleared. This is a one time command. There is no internal latch for this bit.

The PCI can operate in one of four submodes within each major mode (synchronous or asynchronous). The operational submode is determined by CR7 and CR6. CR7 – CR6 = 00 is the normal mode, with the transmitter and receiver operating independently in accordance with the mode and status register instructions.

In asynchronous mode, CR7 – CR6 = 01 places the PCI in the automatic echo mode. Clocked,

regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2 = 1), but the transmitter need not be enabled. CPU to receiver communications continues normally, but the CPU to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected.

The following conditions are true while in automatic echo mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. $\overline{TxRDY}$ output = **1.**
4. The $\overline{TxEMT/DSCHG}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In synchronous mode, CR7 – CR6 = 01 places the PCI in the automatic SYN/DLE stripping mode. The exact action taken depends on the setting of bits MR17 and MR16:

1. In the non-transparent, single SYN mode (MR17 – MR16 = 10), characters in the data stream matching SYN1 are not transferred to the receive data holding register (RHR).
2. In the non-transparent, double SYN mode (MR17 – MR16 = 00), characters in the data stream matching SYN1, or SYN2 if immediately preceded by SYN1, are not transferred the RHR. However, only the first SYN1 of an SYN1 – SYN1 pair is stripped.
3. In transparent mode (MR16 = 1), character in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However, only the first DLE of a DLE–DLE pair is stripped.

Note that automatic stripping mode does not affect the setting of the DLE detect and SYN detect status bits (SR3 and SR5).

Two diagnostic submodes can also be configured. In local loopback mode (CR7 – CR6 = 10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.
2. $\overline{DTR}$ is connected to $\overline{DCD}$ and $\overline{RTS}$ is connected to $\overline{CTS}$.
3. The receiver is clocked by the transmit clock.
4. The $\overline{DTR}$, $\overline{RTS}$ and $\overline{TxD}$ outputs are held high.
5. The $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ and RxD inputs are ignored.

Additional requirements to operate in the local loopback mode are that CR0 (TxEN), CR1 (DTR), and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the PCI.

The second diagnostic mode is the remote loopback mode (CR7 – CR6 = 11). In this mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. No data is sent to the local CPU, but he error status conditions (PE, OE, FE) are set.
4. The $\overline{RxRDY}$, $\overline{TxRDY}$, and $\overline{TxEMT/DSCHG}$ outputs are held high.
5. CR0 (TxEN) is ignored.
6. All other signals operate normally.

Status Register

The data contained in the status register (as shown in Table 8) indicate receiver and transmitter conditions and modem/data set status.

SR0 is the transmitter ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to 0, it indicates that the transmit data holding register has been loaded by the CPU and the data has not been transferred to the transmit shift register. If set equal to 1, it indicates that the Holding Register is ready to accept data from the CPU. This bit is initially set when the transmitter is enabled by CR0, unless a character has previously been loaded into the holding register. It is not set when the automatic echo or remote loopback modes are programmed. When this bit is set, the $\overline{TxRDY}$ output pin is low. In

the automatic echo and remote loopback modes, the output is held high.

SR1, the receiver ready (RxRDY) status bit, indicates the condition of the receive data holding register. If set, it indicates that a character has been loaded into the holding register from the receive shift register and is ready to be read by the CPU. If equal to zero, there is no new character in the holding register. This bit is cleared when the CPU reads the receive data holding register or when the receiver is disabled by CR2. When set, the $\overline{\text{RxRDY}}$ output is low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{\text{DSR}}$ or $\overline{\text{DCD}}$ inputs or that the transmit shift register has completed transmission of a character and no new character has been loaded into the transmit data holding register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. TxEMT will not go active until at least one character has been transmitted. It is cleared by loading the transmit data holding register. The DSCHG condition is enabled when TxEN = 1 or RxEN = 1. If the status register is read twice and SR2 = 1 while SR6 and SR7 remain unchanged, then a TxEMT condition exists. It is cleared when the status register is read by the CPU. When SR2 is set, the $\overline{\text{TxEMT/DSCHG}}$ output is low.

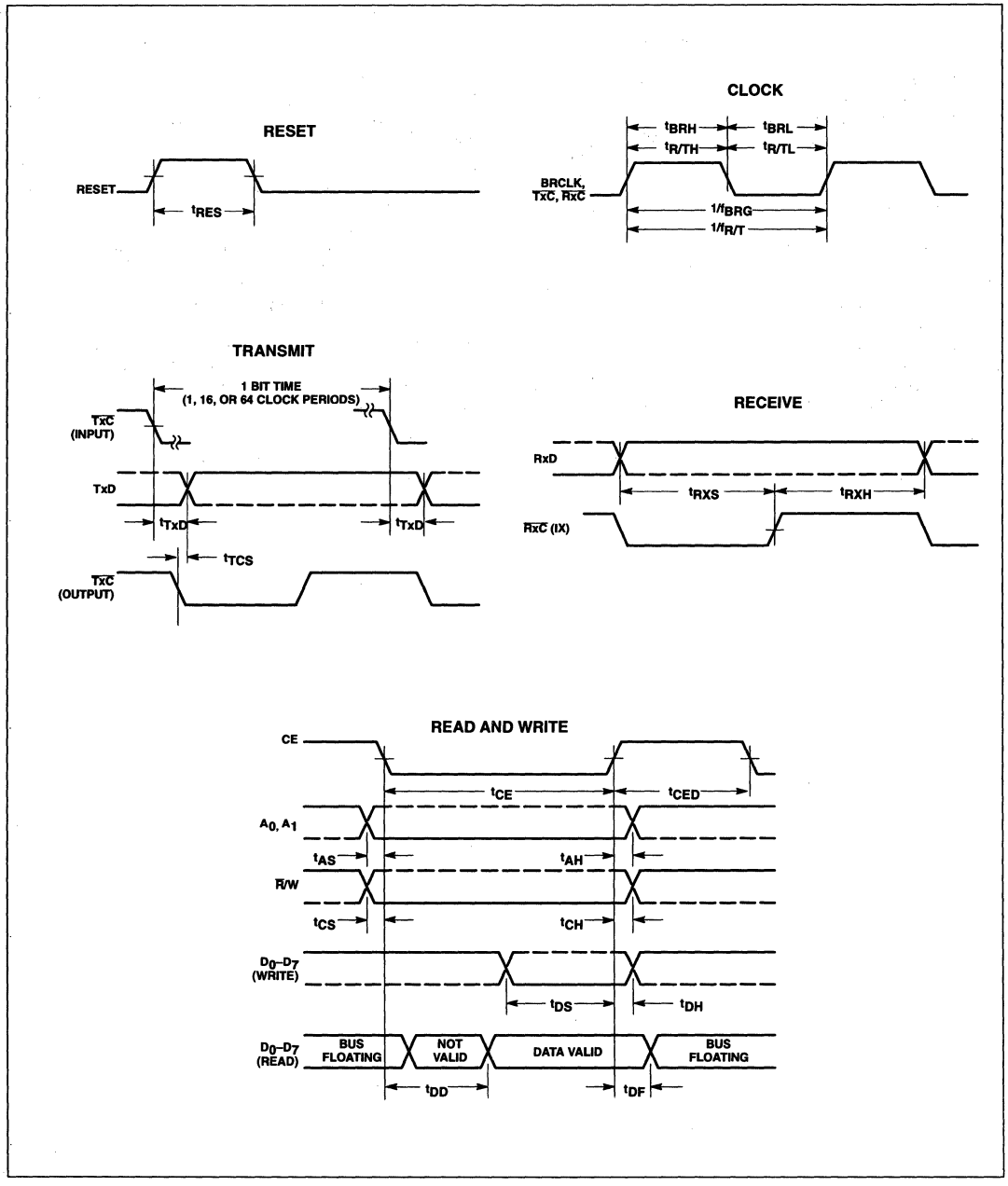
SR3, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16 = 1), with parity disabled, it indicates that a character matching the DLE register has been received. However, only the first DLE of two successive DLEs will set SR3. This bit is cleared when the receiver is disabled and by the reset error command, CR4.

The overrun error status bit, SR4, indicates that the previous character loaded into the receive holding register was not read by the CPU at the time a new received character was transferred into it. This bit is cleared when the receiver is disabled and by the reset error command, CR4.

In asynchronous mode, bit SR5 signifies that the received character was not framed by the programmed number of stop bits. (If 1.5 stop bits are programmed, only the first stop bit is checked.) If RHR = 0 when SR5 = 1, a break condition is present. In synchronous non-transparent mode (MR16 = 0), it indicates receipt of the SYN1 character in single SYN mode or the SYN1 – SYN2 pair in double SYN mode. In synchronous transparent mode (MR16 = 1), this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1 – SYN2) and, after synchronization has been achieved, when a DLE–SYN1 pair is received. The bit is reset when the receiver is disabled, when the reset error command is given in asynchronous mode, and when the status register is read by the CPU in the synchronous mode.

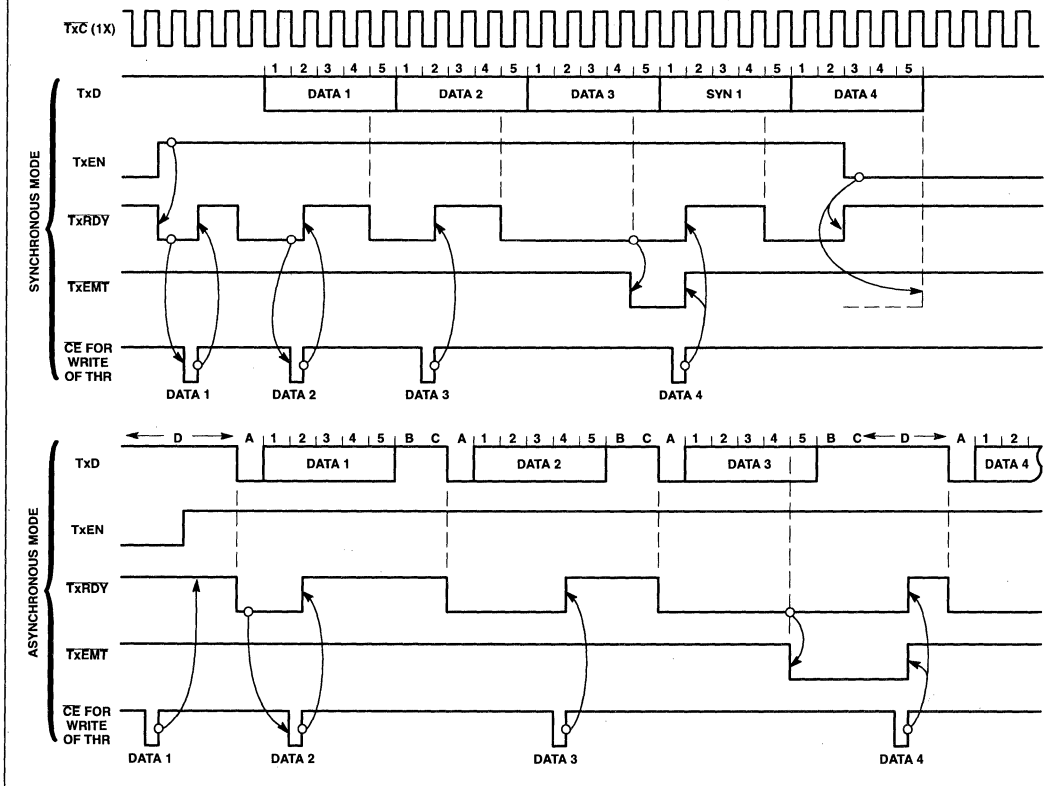
SR6 and SR7 reflect the conditions of the $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ inputs respectively. A low input sets its corresponding status bit and a high input clears it.

TIMING DIAGRAMS



TIMING DIAGRAMS (Continued)

TxRDY, TxEMT (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])

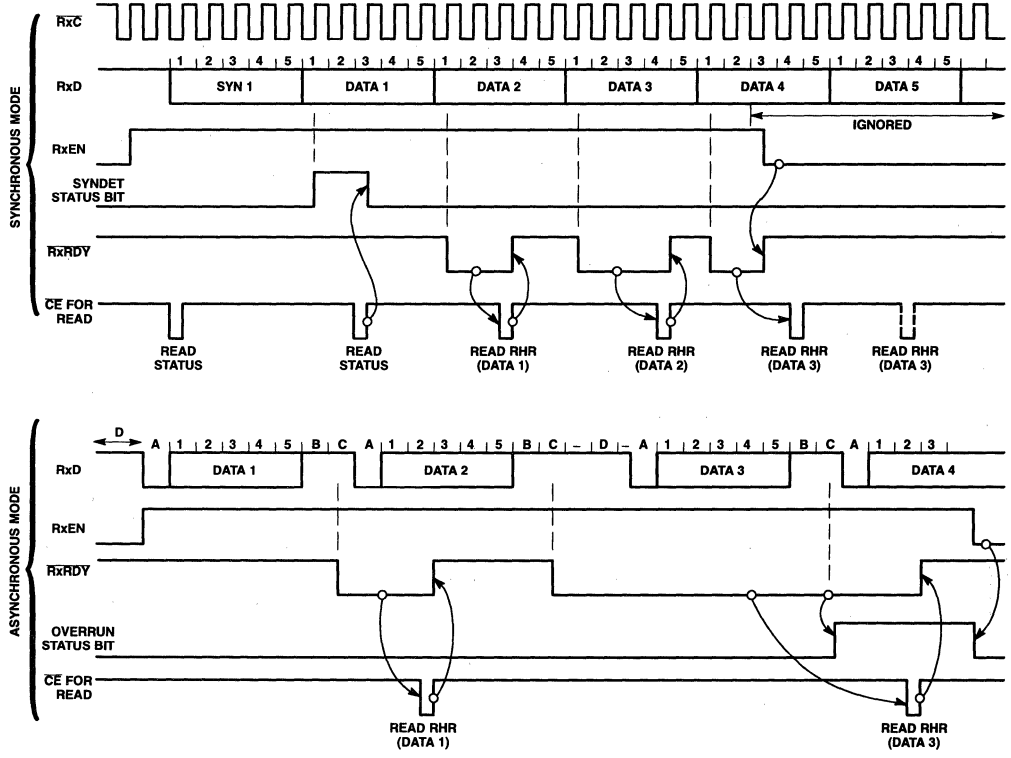


NOTES:

A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
TxEMT goes low at the beginning of the last data bit, or, if parity is enabled, at the beginning of the parity bit.

TIMING DIAGRAMS (Continued)

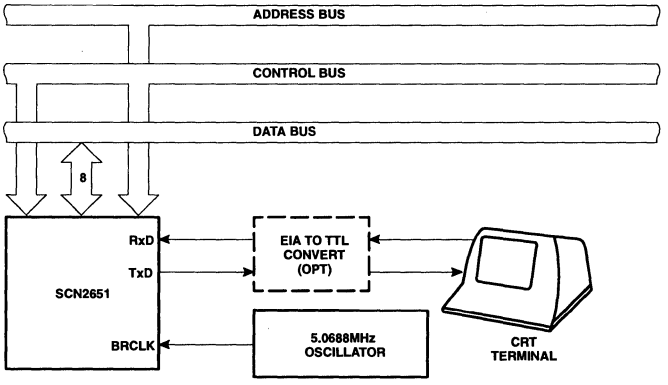
RxRDY (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



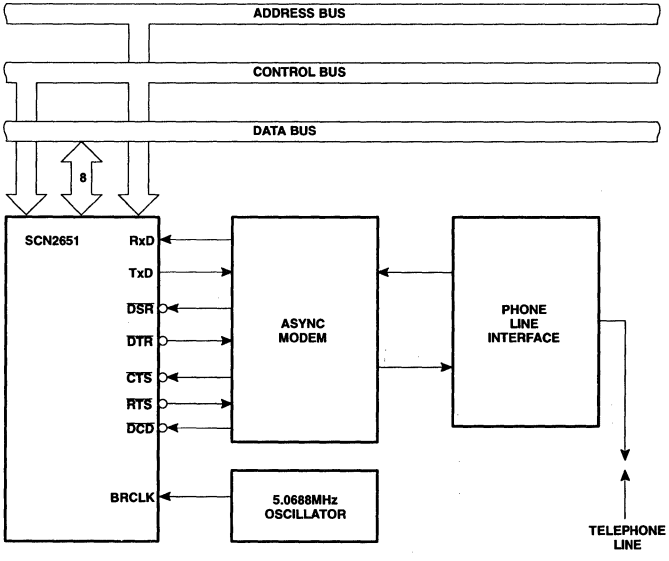
NOTES:
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition

TYPICAL APPLICATIONS

ASYNCHRONOUS INTERFACE TO CRT TERMINAL

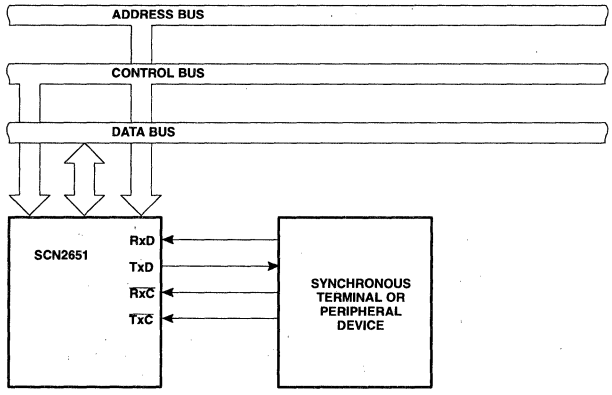


ASYNCHRONOUS INTERFACE TO TELEPHONE LINES

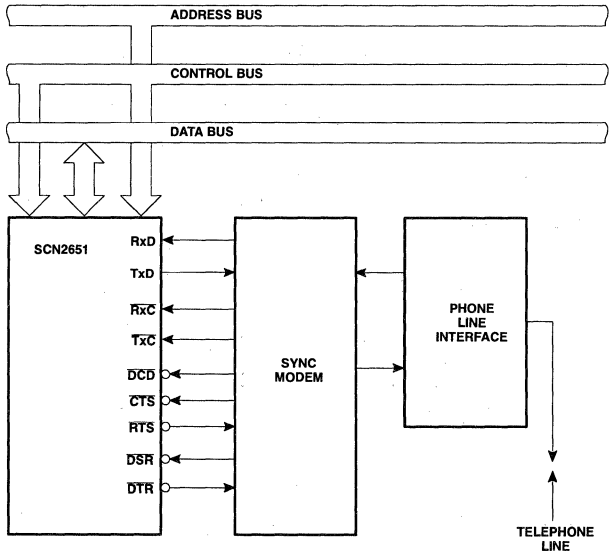


TYPICAL APPLICATIONS (Continued)

SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES



Multi-protocol communications controller (MPCC) SCN2652/SCN68652

DESCRIPTION

The SCN2652/68652 Multi-Protocol Communications Controller (MPCC) is a monolithic n-channel MOS LSI circuit that formats, transmits and receives synchronous serial data while supporting bit-oriented or byte control protocols. The chip is TTL compatible, operates from a single +5V supply, and can interface to a processor with an 8 or 16-bit bidirectional data bus.

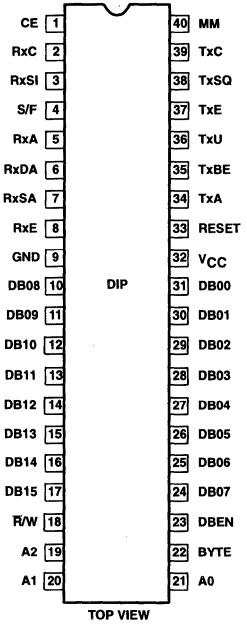
APPLICATIONS

- Intelligent terminals
- Line controllers
- Network processors
- Front end communications
- Remote data concentrators
- Communication test equipment
- Computer to computer links

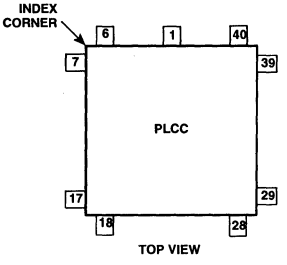
FEATURES

- DC to 2Mbps data rate
- Bit-oriented protocols (BOP): SDLC, ADCCP, HDLC
- Byte-control protocols (BCP): DDCMP, BISYNC (external CRC)
- Programmable operation
  - 8 or 16-bit tri-state data bus
  - Error control – CRC or VRC or none
  - Character length – 1 to 8 bits for BOP or 5 to 8 bits for BCP
  - SYNC or secondary station address comparison for BCP-BOP
  - Idle transmission of SYNC/FLAG or MARK for BCP-BOP
- Automatic detection and generation of special BOP control sequences, i.e., FLAG, ABORT, GA
- Zero insertion and deletion for BOP
- Short character detection for last BOP data character
- SYNC generation, detection, and stripping for BCP
- Maintenance mode for self-testing
- TTL compatible
- Single +5V supply

PIN CONFIGURATION



TOP VIEW



TOP VIEW

Pin	Function	Pin	Function
1	NC	23	NC
2	CE	24	A0
3	RxC	25	BYTE
4	RxSI	26	DBEN
5	S/F	27	DB07
6	RxA	28	DB06
7	RxDA	29	DB05
8	RxSA	30	DB04
9	RxE	31	DB03
10	GND	32	DB02
11	DB08	33	DB01
12	NC	34	NC
13	DB09	35	DB00
14	DB10	36	VCC
15	DB11	37	RESET
16	DB12	38	TxA
17	DB13	39	TxBE
18	DB14	40	TxU
19	DB15	41	TxE
20	R/W	42	TxSQ
21	A2	43	TxC
22	A1	44	MM

NOTE: DB00 is least significant bit, highest number (that is, DB15, A2) is most significant bit.

ORDERING CODE

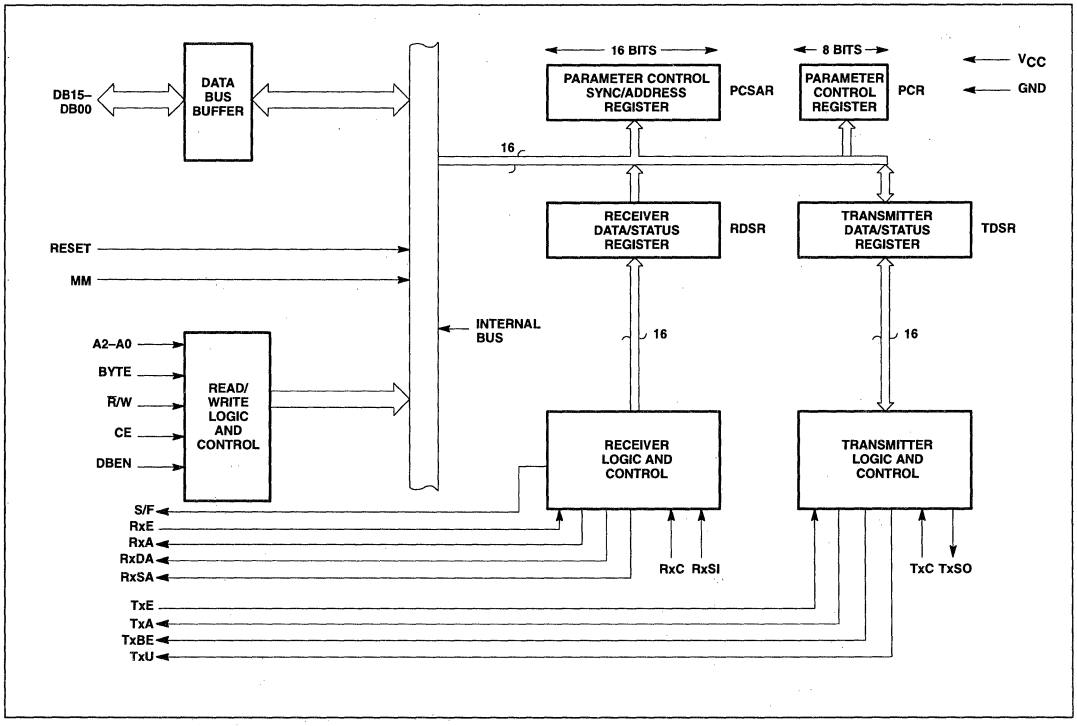
PACKAGES	V_{CC} = 5V ±5%		DWG #
	Commercial 0°C to +70°C	Automotive –40°C to +85°C	
40-Pin Ceramic Dual In-Line Package (DIP)	SCN2652AC2F40 / SCN68652AC2F40		0590B
40-Pin Plastic Dual In-Line Package (DIP)	SCN2652AC2N40 / SCN68652AC2N40	Contact Factory	0415C
44-Pin Square Plastic Lead Chip Carrier (PLCC)	SCN2652AC2A44 / SCN68652AC2A44	Contact Factory	0403G

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature[2]	Note 4	°C
T_{STG}	Storage temperature	–65 to +150	°C
V_{CC}	All inputs with respect to GND[3]	–0.3 to +7	V

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over operating temperature range unless otherwise specified. See ordering code table for applicable temperature range and operating supply range.

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
DB15–DB00	17–10 24–31	I/O	**Data Bus:** DB07–DB00 contain bidirectional data while DB15–DB08 contain control and status information to or from the processor. Corresponding bits of the high and low order bytes can be wire OR'ed onto an 8-bit bus. The data bus is floating if either CE or DBEN are low.
A2–A0	19–21	I	**Address Bus:** A2–A0 select internal registers. The four 16-bit registers can be addressed on a word or byte basis. See Register Address section.
BYTE	22	I	**Byte:** Single byte (8-bit) data bus transfers are specified when this input is high. A low level specifies 16-bit data bus transfers.
CE	1	I	**Chip Enable:** A high input permits a data bus operation when DBEN is activated.
$\overline{R}$/W	18	I	**Read/Write:** $\overline{R}$/W controls the direction of data bus transfer. When high, the data is to be loaded into the addressed register. A low input causes the contents of the addressed register to be presented on the data bus.
DBEN	23	I	**Data Bus Enable:** After A2–A0, CE, BYTE and $\overline{R}$/W are set up, DBEN may be strobed. During a read, the 3-state data bus (DB) is enabled with information for the processor. During a write, the stable data is loaded into the addressed register and TxBE will be reset if TDSR was addressed.
RESET	33	I	**Reset:** A high level initializes all internal registers (to zero) and timing.
MM	40	I	**Maintenance Mode:** MM internally gates TxSO back to RxSI and TxC to RxC for off line diagnostic purposes. The RxC and RxSI inputs are disabled and TxSO is high when MM is asserted.
RxE	8	I	**Receiver Enable:** A high level input permits the processing of RxSI data. A low level disables the receiver logic and initializes all receiver registers and timing.
RxA	5	O	**Receiver Active:** RxA is asserted when the first data character of a message is ready for the processor. In the BOP mode this character is the address. The received address must match the secondary station address if the MPCC is a secondary station. In BCP mode, if strip-SYNC ($PCSAR_{13}$) is set, the first non-SYNC character is the first data character; if strip-SYNC is zero, the character following the second SYNC is the first data character. In the BOP mode, the closing FLAG resets RxA. In the BCP mode, RxA is reset by a low level at RxE.
RxDA*	6	O	**Receiver Data Available:** RxDA is asserted when an assembled character is in $RDSR_L$ and is ready to be presented to the processor. This output is reset when $RDSR_L$ is read.
RxC	2	I	**Receiver Clock:** RxC (1X) provides timing for the receiver logic. The positive going edge shifts serial data into the RxSR from RxSI.
S/F	4	O	**SYNC/FLAG:** S/F is asserted for one RxC clock time when a SYNC or FLAG character is detected.
RxSA*	7	O	**Receiver Status Available:** RxSA is asserted when there is a zero to one transition of any bit in $RDSR_H$ except for RSOM. It is cleared when $RDSR_H$ is read.
RxSI	3	I	**Receiver Serial Input:** RxSI is the received serial data. Mark = '1', space = '0'.
TxE	37	I	**Transmitter Enable:** A high level input enables the transmitter data path between $TDSR_L$ and TxSO. At the end of a message, a low level input causes TxSO = 1(mark) and TxA = 0 after the closing FLAG (BOP) or last character (BCP) is output on TxSO.
TxA	34	O	**Transmitter Active:** TxA is asserted after TSOM ($TDSR_8$) is set and TxE is raised. This output will reset when TxE is low and the closing FLAG (BOP) or last character (BCP) has been output on TxSO.
TxBE*	35	O	**Transmitter Buffer Empty:** TxBE is asserted when theTDSR is ready to be loaded with new control information or data. The processor should respond by loading theTDSR which resets TxBE.
TxU*	36	O	**Transmitter Underrun:** TxU is asserted during a transmit sequence when the service of TxBE has been delayed for one character time. This indicates the processor is not keeping up with the transmitter. Line fill depends on $PCSAR_{11}$. TxU is reset by RESET or setting of TSOM ($TDSR_8$), synchronized by the falling edge of TxC.
TxC	39	I	**Transmitter Clock:** TxC (1X) provides timing for the transmitter logic. The positive going edge shifts data out of the TxSR to TxSO.
TxSO	38	O	**Transmitter Serial Output:** TxSO is the transmitted serial data. Mark = '1', space = '0'.
V_{CC}	32	I	**+5V:** Power supply.
GND	9	I	**Ground:** 0V reference ground.

*Indicates possible interrupt signal

Table 1. Register Access

REGISTERS		NO. OF BITS	DESCRIPTION*
Addressable			
PCSAR	Parameter control sync/ address register	16	$PCSAR_H$ and PCR contain parameters common to the receiver and transmitter. $PCSAR_L$ contains a programmable SYNC character (BCP) or secondary station address (BOP).
PCR	Parameter control register	8	$RDSR_H$ contains receiver status information.
RDSR	Receive data/status register	16	$RDSR_L$ = RxDB contains the received assembled character.
TDSR	Transmit data/status register	16	$TDSR_H$ contains transmitter command and status information. TDSRL = TxDB contains the character to be transmitted
Non-Addressable			
CCSR	Control character shift register	8	These registers are used for character assembly (CSSR, HSR, RxSR), disassembly (TxSR), and CRC accumulation/generation (RxCRC, TxCRC).
HSR	Holding shift register	16	
RxSR	Receiver shift register	8	
TxSR	Transmitter shift register	8	
RxCRC	Receiver CRC accumulation register	16	
TxCRC	Transmitter CRC generation register	16	

NOTES:
*H = High byte – bits 15–8
L = Low byte – bits 7–0

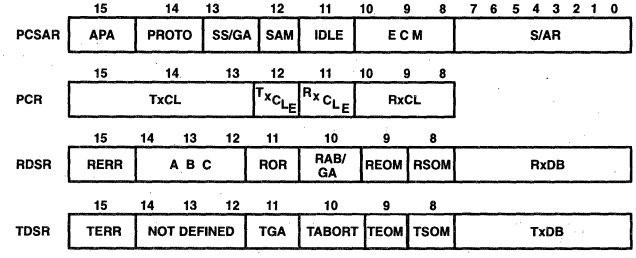
Table 2. Error Control

CHARACTER	DESCRIPTION
FCS	Frame check sequence is transmitted/received as 16 bits following the last data character of a BOP message. The divisor is usually CRC–CCITT ($X^{16} + X^{12} + X^5 + 1$) with dividend preset to 1's but can be other wise determined by ECM. The inverted remainder is transmitter as the FCS.
BCC	Block check character is transmitted/received as two successive characters following the last data character of a BCP message. The polynomial is CRC–16 ($X^{16} + X^{15} + X^2 + 1$) or CRC–CCITT with dividend preset to 0's (as specified by ECM). The true remainder is transmitted as the BCC.

Table 3. Special Characters

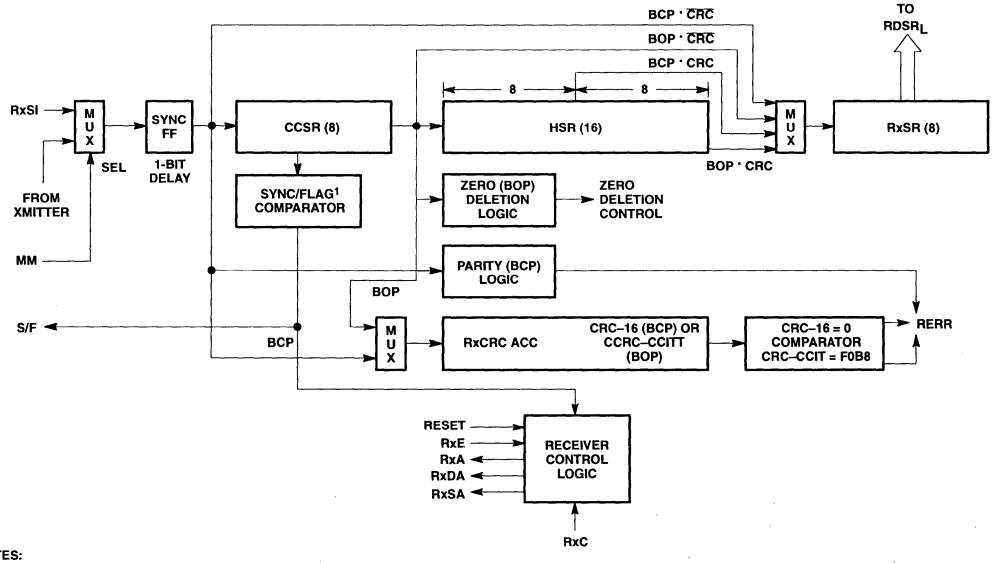
OPERATION	BIT PATTERN	FUNCTION
BOP		
FLAG	01111110	Frame message
ABORT	11111111 generation	Terminate communication
	01111111 detection	
GA	01111111	Terminate loop mode repeater function
Address	$(PCSAR_L)^1$	Secondary station address
BCP		
SYNC	$(PCSAR_L)$ or $(TxDB)^2$ generation	Character synchronization

NOTES:
1. ( ) = contents of.
2. For IDLE = 0 or 1 respectively.



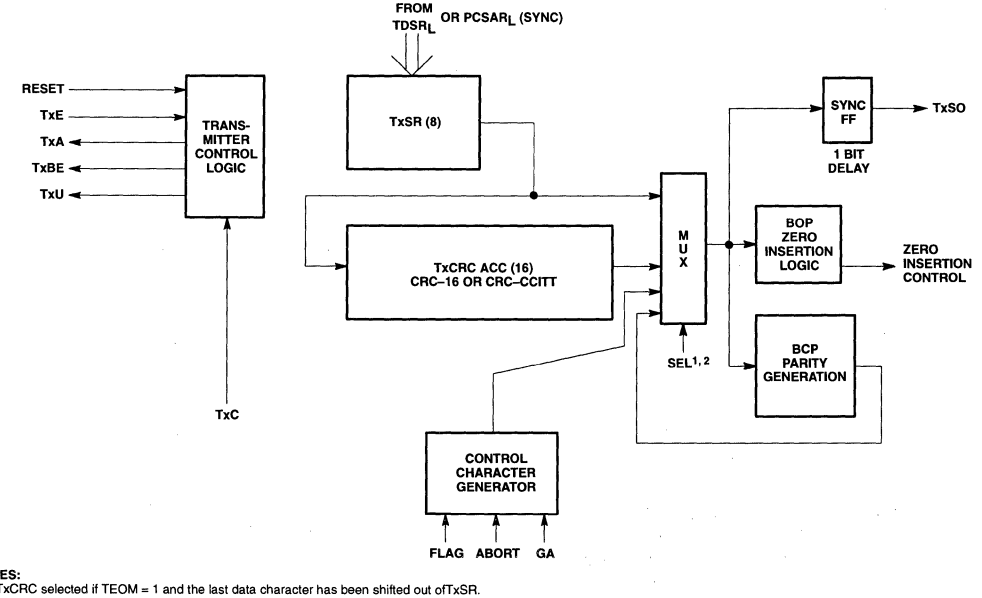
NOTE:
Refer to Register Formats for mnemonics and description.

Figure 1. Short Form Register Bit Formats



NOTES:
1. Detected in SYNC FF and 7 MS bits of CCSR.
2. In BOP mode, a minimum of two data characters must be received to turn the receiver active.

Figure 2. MPCC Receiver Data Path



NOTES:
1. TxCRC selected if TEOM = 1 and the last data character has been shifted out ofTxSR.
2. In BCP parity selected will be generated after each character is shifted out of TxSR.

Figure 3. MPCC Transmitter Data Path

FUNCTIONAL DESCRIPTION

The MPCC can be functionally partitioned into receiver logic, transmitter logic, registers that can be read or loaded by the processor, and data bus control circuitry. The register bit formats are shown in Figure 1 while the receiver and transmitter data paths are depicted in Figures 2 and 3.

RECEIVER OPERATION

General

After initializing the parameter control registers (PCSAR and PCR), the RxE input must be set high to enable the receiver data path. The serial data on the RxSI is synchronized and shifted into an 8-bit Control Character Shift Register (CCSR) on the rising edge of RxC. A comparison between CCSR contents and the FLAG (BOP) or SYNC (BCP) character is made until a match is found. At that time, the S/F output is asserted for one RxC time and the 16-bit Holding Shift Register (HSR) is enabled. The receiver then operates as described below.

BOP Operation

A flowchart of receiver operation in BOP mode appears in Figure 4. Zero deletion (after five ones are received) is implemented on the received serial data so that a data character will not be interpreted as a FLAG, ABORT, or GA. Bits following the FLAG are shifted through the CCSR, HSR, and into the Receiver Shift Register (RxSR). A character will be assembled in the RxSR and transferred to the $RDSR_L$ for presentation to the processor. At that time the RxDA output will be asserted and the processor must take the character no later than one RxC time after the next character is assembled in the RxSR. If not, an overrun ($RDSR_{11} = 1$) will occur and succeeding characters will be lost.

The first character following the FLAG is the secondary station address. If the MPCC is a secondary station ($PCSAR_{12} = 1$), the contents of RxSR are compared with the address stored in $PCSAR_L$. A match indicates the forthcoming message is intended for the station; the RxA output is asserted, the character is loaded into $RDSR_L$, RxDA is asserted and the Receive Start of Message bit (RSOM) is set. No match indicates that another station is being addressed and the receiver searches for the next FLAG.

If the MPCC is a primary station, ($PCSAR_{12} = 0$), no secondary address check is made; RxA is asserted and RSOM is set once the first non-FLAG character has been loaded into $RDSR_L$ and RxDA has been asserted. Extended address field can be supported by software if $PCSAR_{12} = 0$.

When the 8 bits following the address character have been loaded into $RDSR_L$ and RxDA has been asserted, RSOM will be cleared. The processor should read this 8-bit character and interpret it as the Control field.

Received serial data that follows is read and interpreted as the information field by the processor. It will be assembled into character lengths as specified by PCR_{8-10}. As before, RxDA is asserted each time a character has been transferred into $RDSR_L$ and is cleared when $RDSR_L$ is read by the processor. $RDSR_H$ should only be read when RxSA is asserted. This occurs on a zero to one transition of any bit in $RDSR_H$ except for RSOM. RxSA and all bits in $RDSR_H$ except RSOM are cleared when $RDSR_H$ is read. The processor should check $RDSR_{9-15}$ each time RxSA is asserted. If $RDSR_9$ is set, then $RDSR_{12-15}$ should be examined.

Receiver character length may be changed dynamically in response to RxDA: read the character in RxDB and write the new character length into RxCL. The character length will be changed on the next receiver character boundary. A received residual (short) character will be transferred into RxDB after the previous character in RxDB has been read, i.e. there will not be an overrun. In general the last two characters are protected from overrun.

The CRC–CCITT, if specified by $PCSAR_{8-10}$, is accumulated in RxCRC on each character following the FLAG. When the closing FLAG is detected in the CCSR, the received CRC is in the 16-bit HSR. At that time, the Receive End of Message bit (REOM) will be set; RxSA and RxDA will be asserted. The processor should read the last data character in $RDSR_L$ and the receiver status in $RDSR_{9-15}$. If $RDSR_{15} = 1$, there has been a transmission error; the accumulated CRC–CCITT is incorrect. If $RDSR_{12-14} \neq 0$, last data character is not of prescribed length. Neither the received CRC nor closing FLAG are presented to the processor. The processor may drop RxE or leave it active at the end of the received message.

RxBCP Operation

The operation of the receiver in BCP mode is shown in Figure 5. The receiver initially searches for two successive SYNC characters, of length specified by PCR_{8-10}, that match the contents of $PCSAR_L$. The next non-SYNC character or next SYNC character, if stripping is not specified ($PCSAR_{13} = 0$), causes RxA to be asserted and enables the receiver data path. Once enabled, all characters are assembled in RxSR and loaded into $RDSR_L$. RxDA is active when a character is available in $RDSR_L$. RxSA is active on a 0 to 1 transition of any bit in $RDSR_H$. The signals are cleared when RDSRl or $RDSR_H$ are read respectively.

If CRC–16 error control is specified by $PCSAR_{8-10}$, the processor must determine the last character received prior to the CRC field. When that character is loaded into $RDSR_L$ and RxDA is asserted, the received CRC will be in CCSR and HSR_L. To check for a transmission error, the processor must read the receiver status ($RDSR_H$) and examine $RDSR_{15}$. This bit will be set for one character time if an error free message has been received. If $RDSR_{15} = 0$, the CRC–16 is in error. The state of $RDSR_{15}$ in BCP CRC mode does not set RxSA. Note that this bit should be examined only at the end of a message. The accumulated CRC will include all characters starting with the first non-SYNC character if $PCSAR_{13} = 1$, or the character after the opening two SYNCs if $PCSAR_{13} = 0$. This necessitates external CRC generation/checking when supporting IBM's

BISYNC. This can be accomplished using the Philips Semiconductors SCN2653 Polynomial Generator/Checker. See Typical Applications.

If VRC has been selected for error control, parity (odd or even) is regenerated on each character and checked when the parity bit is received. A discrepancy causes $RDSR_{15}$ to be set and RxSA to be asserted. This must be sensed by the processor. The received parity bit is stripped before the character is presented to the processor.

When the processor has read the last character of the message, it should drop RxE which disables the receiver logic and initializes all receiver registers and timing.

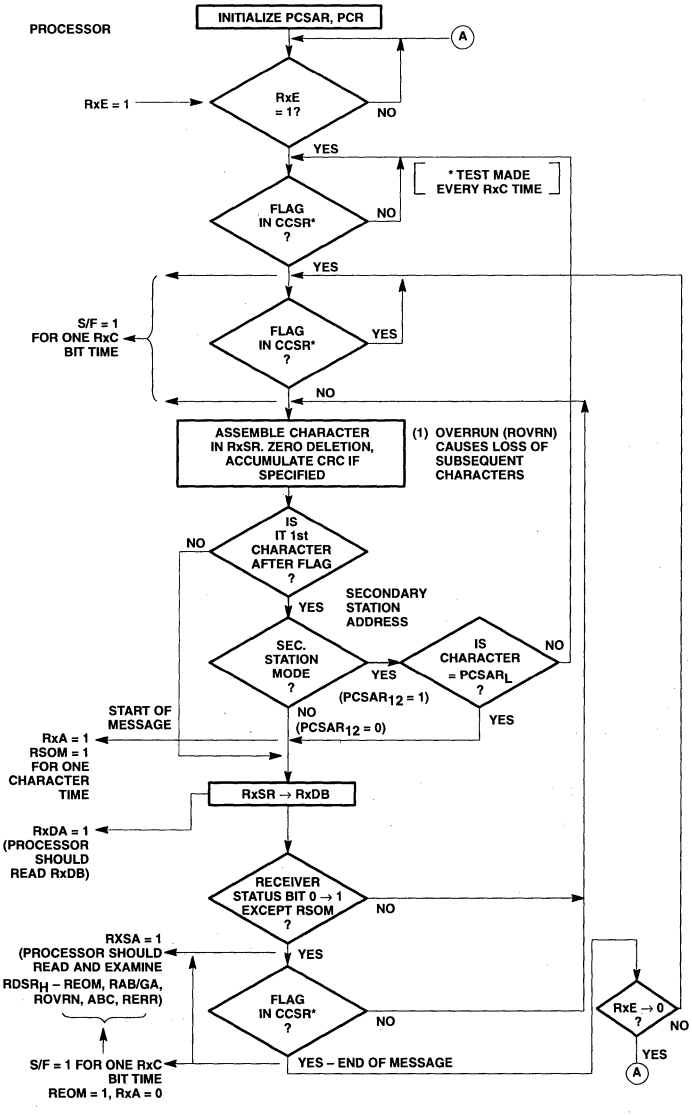


Figure 4. BOP Receive

TRANSMITTER OPERATION

General

After the parameter control registers (PCSAR and PCR) have been initialized, TxSO is held at mark until TSOM ($TDSR_8$) is set and TxE is raised. Then, transmitter operation depends on protocol mode.

TxBOP Operation

Transmitter operation for BOP is shown in Figure 6. A FLAG is sent after the processor sets the Transmit Start of Message bit (TSOM) and raises TxE. The FLAG is used to synchronize the message that follows. TxA will also be asserted. When TxBE is asserted by the MPCC, the processor should load $TDSR_L$ with the first character of the message. TSOM should be cleared at the same time $TDSR_L$ is loaded (16-bit data bus) or immediately thereafter (8-bit data bus). FLAGS are sent as long as TSOM = 1. For counting the number of FLAGs, the processor should reassert TSOM in response to the assertion of TxBE.All succeeding characters are loaded into $TDSR_L$ by the processor when TxBE = 1. Each

character is serialized in TxSR and transmitted on TxSO. Internal zero insertion logic stuffs a "0" into the serial bit stream after five successive "1s" are sent. This insures a data character will not match a FLAG, ABORT, or GA reserved control character. As each character is transmitted, the Frame Check Sequence (FCS) is generated as specified by Error Control Mode ($PCSAR_{8-10}$). The FCS should be the CRC–CCITT polynomial ($X^{16} + X^{12} + X^5 + 1$) preset to 1s. If an underrun occurs (processor is not keeping up with the transmitter), TxU and TERR ($TDSR_{15}$) will be asserted with ABORT or FLAG used as the TxSO line fill depending on the state of IDLE ($PCSAR_{11}$). The processor must set TSOM to reset the underrun condition. To retransmit the message, the processor should proceed with the normal start of message sequence.

A residual character of 1 to 7 bits may be transmitted at the end of the information field. In response to TxBE, write the residual character length into TxCL and load TxDB with the residual character. Dynamic alteration of character length should be done in exactly the same sequence. The character length will be changed on the next transmit character boundary.

After the last data character has been loaded into $TDSR_L$ and sent to TxSR (TxBE = 1), the processor should set TEOM ($TDSR_9$). The MPCC will finish transmitting the last character followed by the FCS and the closing FLAG. The processor should clear TEOM and drop TxE when the next TxBE is asserted. This corresponds to the start of closing FLAG transmission. When TxE has been dropped. TxA will be low 1 1/2 bit times after the last bit of the closing FLAG has been transmitted. TxSO will be marked after the closing FLAG has been transmitted.

If TxE and TEOM are high, the transmitter continues to send FLAGs. The processor may initiate the next message by resetting TEOM and setting TSOM, or by loading $TDSR_L$ with a data character and then simply resetting TSOM (without setting TSOM).

TxBCP Operation

Transmitter operation for BCP mode is shown in Figure 7. TxA will be asserted after TSOM = 1 and TxE is raised. At that time SYNC characters are sent from $PCSAR_L$ or $TDSR_L$ (IDLE = 0 or 1) as long as TSOM = 1. TxBE is asserted at the start of transmission of the first SYNC character. For counting the number of SYNCs, the processor should reassert TSOM in response to the assertion of TxBE. When TSOM = 0 transmission is from $TDSR_L$, which must be loaded with characters from the processor each time TxBE is asserted. If this loading is delayed for more than one character time, an underrun results: TxU and TERR are asserted and the

TxSO line fill depend on IDLE ($PCSAR_{11}$). The processor must set TSOM and retransmit the message to recover. This is not compatible with IBM's BISYNC, so that the user must not underrun when supporting that protocol.

CRC–16, if specified by $PCSAR_{8-10}$, is generated on each character transmitted from $TDSR_L$ when TSOM =0. The processor must set TEOM = 1 after the last data character has been sent to TxSR (TxBE = 1). The MPCC will finish transmitting the last data character and the CRC–16 field before sending SYNC characters which are transmitted as long as TEOM = 1. If SYNCs are not desired after CRC–16 transmission, the processor should clear TEOM and lower TxE when the TxBE corresponding to the start of CRC–16 transmission is asserted. When TEOM = 0, the line is marked and a new message may be initiated by setting TSOM and raising TxE.

If VRC is specified, it is generated on each data character and the data character length must not exceed 7 bits. For software LRC or CRC, TEOM should be set only if SYNC's are required at the end of the message block.

SPECIAL CASE: The capability to transmit 16 spaces is provided for line turnaround in half duplex mode or for a control recovery situation. This is achieved by setting TSOM and TEOM, clearing TEOM when TxBE = 1, and proceeding as required.

PROGRAMMING

Prior to initiating data transmission or reception, PCSAR and PCR must be loaded with control information from the processor. The contents of these registers (see Register Format section) will configure the MPCC for the user's specific data communication environment. These registers should be loaded during power-on initialization and after a reset operation. They can be changed at any time that the respective transmitter or receiver is disabled.

The default value for all registers is zero. This corresponds to BOP, primary station mode, 8-bit character length, FCS = CRC–CCITT preset to 1s.

For BOP mode the character length register (PCR) may be set to the desired values during system initialization. The address and control fields will automatically be 8-bits. If a residual character is to be transmitted, TxCL should be changed to the residual character length prior to transmission of that character.

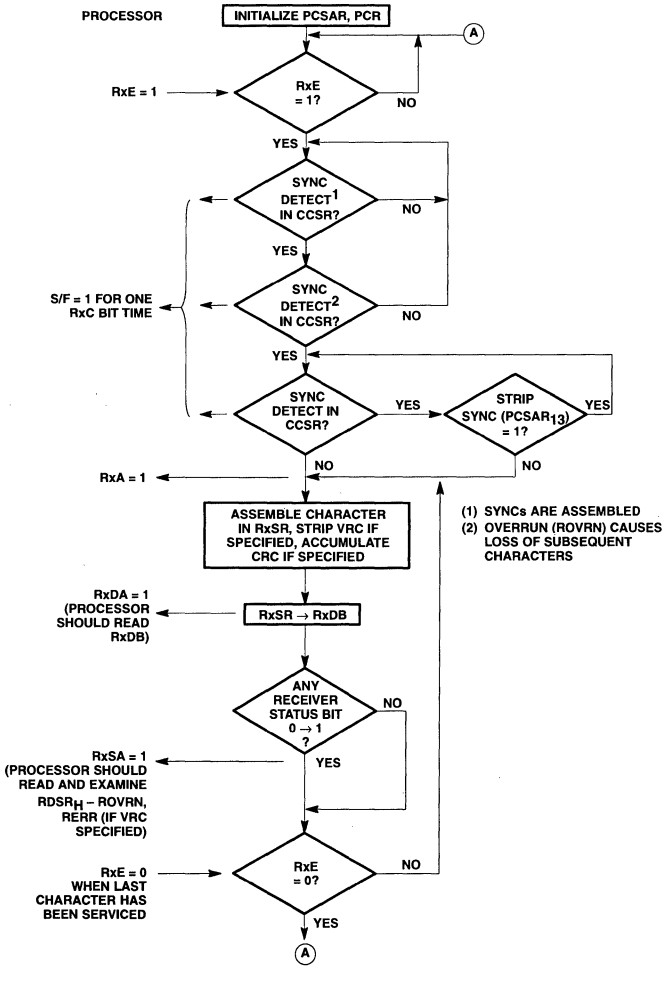
DATA BUS CONTROL

The processor must set up the MPCC register address (A2–A0), chip enable (CE), byte select (BYTE), and read/write ($\overline{R}/W$) inputs before each data bus transfer operation.

During a read operation ($\overline{R}/W$ = 0), the leading edge of DBEN will initiate an MPCC read cycle. The addressed register will place its contents on the data bus. If BYTE = 1, the 8-bit byte is placed on DB15–08 or DB07–00 depending on the H/L status of the register addressed. Unused bits in $RDSR_L$ are zero. If BYTE = 0, all 16 bits (DB15–00) contain MPCC information. The trailing edge of DBEN will reset RxDA and/or RxSA if $RDSR_L$ or $RDSR_H$ is addressed respectively.

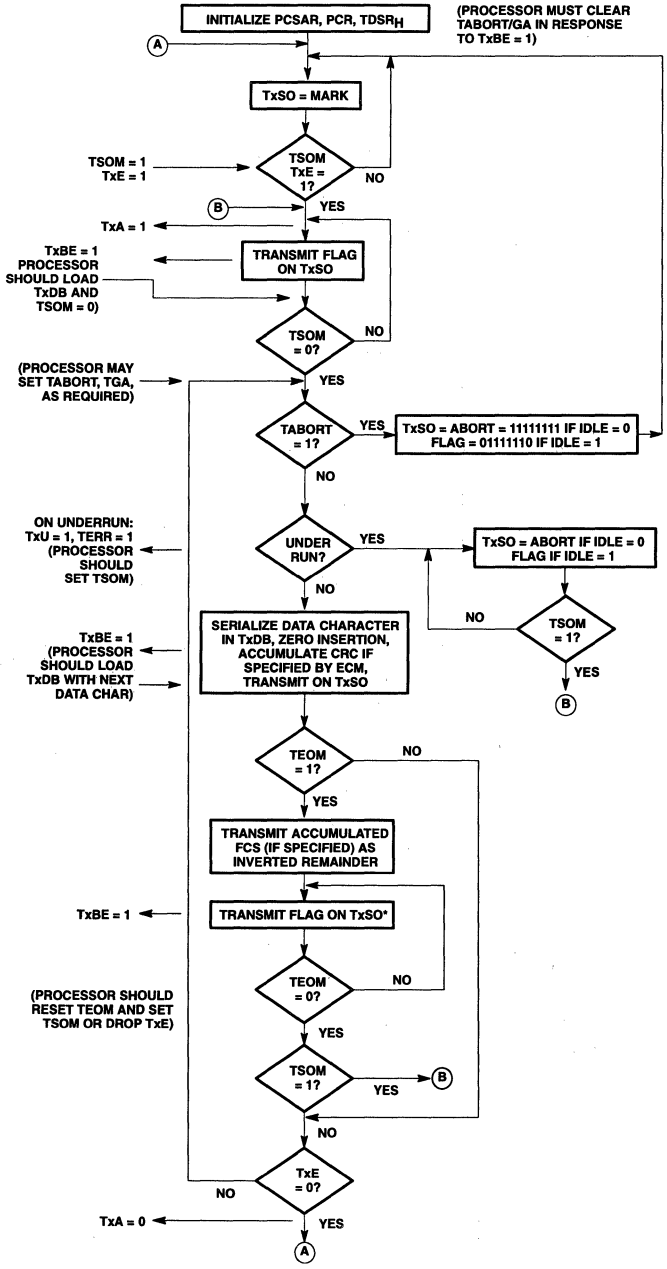
DBEN acts as the enable and strobe so that the MPCC will not begin its internal read cycle until DBEN is asserted.

During a write operation ($\overline{R}/W$ = 1), data must be stable on DB_{15-08} and/or DB_{07-00} prior to the leading edge of DBEN. The stable data is strobed into the addressed register by DBEN. TxBE will be cleared if the addressed register was $TDSR_H$ or $TDSR_L$.



NOTES:
1. Test made every RxC time.
2. Test made on Rx character boundary.

Figure 5. BCP Receive



*GA will be transmitted if TGA is set together with TEOM.

Figure 6. BOP Transmit

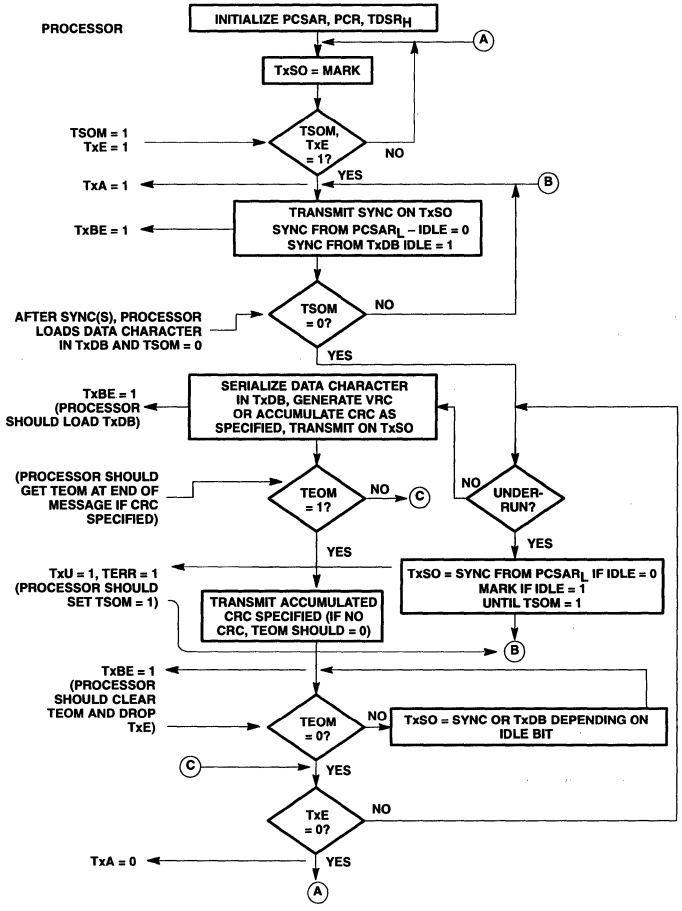


Figure 7. BCP Transmit

Table 4. MPCC Register Addressing

	A2	A1	A0	REGISTER
Byte = 0	**(16-Bit Data Bus = DB_{15} – DB_{00})**			
	0	0	X	RDSR
	0	1	X	TDSR
	1	0	X	PCSAR
	1	1	X	PCR*
Byte = 1	**(8-Bit Data Bus = DB_{7-0} or DB_{15-8}**)**			
	0	0	0	$RDSR_L$
	0	0	1	$RDSR_H$
	0	1	0	$TDSR_L$
	0	1	1	$TDSR_H$
	1	0	0	$PCSAR_L$
	1	0	1	$PCSAR_H$
	1	1	0	PCR_L*
	1	1	1	PCR_H

NOTES:
* PCR lower byte does not exist. It will be all "0"s when read.
** Corresponding high and low order pins must be tied together.

Table 5. Parameter Control Register (PCR)–(R/W)

BIT	NAME	MODE	FUNCTION
00–07	Not Defined		
08–10	RxCL	BOP/BCP	Receiver character length is loaded by the processor when RxCLE = 0. The character length is valid after transmission of single byte address and control fields have been received. 10 9 8 — Char length (bits) 0 0 0 — 8 0 0 1 — 1 0 1 0 — 2 0 1 1 — 3 1 0 0 — 4 1 0 1 — 5 1 1 0 — 6 1 1 1 — 7
11	RxCLE	BOP/BCP	Receiver character length enable should be zero when the processor loads RxCL. The remaining bits of PCR are not affected during loading. Always 0 when read.
12	TxCLE	BOP/BCP	Transmitter character length enable should be zero when the processor loads TxCL. The remaining bits of PCR are not affected during loading. Always 0 when read.
13–15	TxCL	BOP/BCP	Transmitter character length is loaded by the processor when TxCLe = 0. Character bit length specification format is identical to RxCL. It is valid after transmission of single byte address and control fields.

Table 6. Parameter Control SYNC/Address Register (PCSAR)–(R/W)

BIT	NAME	MODE	FUNCTION
00–07	S/AR	BOP	SYNC/address register. Contains the secondary station address if the MPCC is a secondary station. The contents of this register is compared with the first received non-FLAG character to determine if the message is meant for this station.
		BCP	SYNC character is loaded into this register by the processor. It is used for receive and transmit bit synchronization with bit length specified by RxCL and TxCL.
08–10	ECM	BOP/BCP	**Error Control Mode** / **10** / **9** / **8** / **Suggested Mode** / **Char. length** CRC–CCITT preset to 1's 0 0 0 BOP 1–8 CRC–CCITT preset to 0's 0 0 1 BCP 8 Not used 0 1 0 — CRC–16 preset to 0's 0 1 1 BCP 8 VRC odd 1 0 0 BCP 5–7 VRC even 1 0 1 BCP 5–7 Not used 1 1 0 — No error control 1 1 1 BCP/BOP 5–8 ECM should be loaded by the processor during initialization or when both data paths are idle.
11	IDLE		Determines line fill character to be used if transmitter underrun occurs (TxU asserted and TERR set) and transmission of special characters for BOP/BCP.
		BOP	IDLE = 0, transmit ABORT characters during underrun and when TABORT = 1. IDLE = 1, transmit FLAG characters during underrun and when TABORT = 1.
		BCP	IDLE = 0 transmit initial SYNC characters and underrun line fill characters from theS/AR. IDLE = 1 transmit initial SYNC characters from TxDB and marks TxSO during underrun.
12	SAM	BOP	Secondary Address Mode = 1 if the MPCC is a secondary station. This facilitates automatic recognition of the received secondary station address. When transmitting, the processor must load the secondary address into TxDB. SAM = 0 inhibits the received secondary address comparison which serves to activate the receiver after the first non-FLAG character has been received.
13	SS/GA		Strip SYNC/Go Ahead. Operation depends on mode.
		BOP	SS/GA = 1 is used for loop mode only and enables GA detection. When a GA is detected as a closing character, REOM and RAB/GA will be set and the processor should terminate the repeater function. SS/GA = 0 is the normal mode which enables ABORT detection. It causes the receiver to terminate the frame upon detection of an ABORT or FLAG.
		BCP	SS/GA = 1, causes the receiver to strip SYNC's immediately following the first two SYNC's detected. SYNC's in the middle of a message will not be stripped. SS/GA = 0, presents any SYNC's after the initial two SYNC's to the processor.
14	PROTO		Determines MPCC Protocol mode
		BOP BCP	PROTO = 0 PROTO = 1
15	APA	BOP	All parties address. If this bit is set, the receiver data path is enabled by an address field of '11111111' as well as the normal secondary station address.

Table 7. Transmit Data/Status Register (TDSR) (R/W except TDSR15)

BIT	NAME	MODE	FUNCTION
00–07	TxDB	BOP/BCP	Transmit data buffer. Contains processor loaded characters to be serialized in TxSR and transmitted on TxSO.
08	TSOM		Transmitter start of message. Set by the processor to initiate message transmission provided TxE = 1.
		BOP	TSOM = 1 generates FLAGs. When TSOM = 0 transmission is from TxDB and FCS generation (if specified) begins. FCS, as specified by $PCSAR_{8-10}$, should be CRC–CCITT preset to 1's.
		BCP	TSOM = 1 generates SYNCs from $PCSAR_L$ or transmits from TxDB for IDLE = 0 or 1 respectively. When TSOM = 0 transmission is from TxDB and CRC generation (if specified) begins.
09	TEOM		Transmit end of message. Used to terminate a transmitted message.
		BOP	TEOM = 1 causes the FCS and the closing FLAG to be transmitted following the transmission of the data character in TxSR. FLAGs are transmitted until TEOM = 0. ABORT or GA are transmitted if TABORT or TGA are set when TEOM = 1.
		BCP	TEOM = 1 causes CRC–16 to be transmitted (if selected) followed by SYNCs from $PCSAR_L$ or TxDB (IDLE = 0 or 1). Clearing TEOM prior to the end of CRC–16 transmission (when TxBE = 1) causes TxSO to be marked following the CRC–16. TxE must be dropped before a new message can be initiated. If CRC is not selected, TEOM should not be set.
10	TABORT	BOP	Transmitter abort = 1 will cause ABORT or FLAG to be sent (IDLE = 1 or 1) after the current character is transmitted. (ABORT = 11111111)
11	TGA	BOP	Transmit go ahead (GA) instead of FLAG when TEOM = 1. This facilitates repeater termination in loop mode. (GA = 01111111)
12–14	Not Defined		
15	TERR	Read only	Transmitter error = 1 indicates the TxDB has not been loaded in time (one character time–1/2 TxC period after TxBE is asserted) to maintain continuous transmission. TxU will be asserted to inform the processor of this condition. TERR is cleared by setting TSOM. See timing diagram.
		BOP	ABORT's or FLAG's are sent as fill characters (IDLE = 0 or 1)
		BCP	SYNC's or MARK's are sent as fill characters (IDLE = 0 or 1). For IDLE = 1 the last character before underrun is not valid.

Table 8. Receiver Data/Status Register (RDSR)–(Read Only)

BIT	NAME	MODE	FUNCTION
00–07	RxDB	BOP/BCP	Receiver data buffer. Contains assembled characters from the RxSR. If VRC is specified, the parity bit is stripped.
08	RSOM	BOP	Receiver start of message = 1 when a FLAG followed by a non-FLAG has been received and the latter character matches the secondary station if SAM = 1. RxA will be asserted when RSOM = 1. RSOM resets itself after one character time and has no affect on RxSA.
09	REOM	BOP	Receiver end of message = 1 when the closing FLAG is detected and the last data character is loaded into RxDB or when an ABORT/GA character is received. REOM is cleared on reading $RDSR_H$, reset operation, or dropping of RxE.
10	RAB/GA	BOP	Received ABORT or GA character = 1 when the receiver senses an ABORT character if SS/GA = 0 or a GA character if SS/GA = 1. RAB/GA is cleared on reading $RDSR_H$, reset operation, or dropping of RxE. A received abort does not set RxDA.
11	ROR	BOP/BCP	Receiver overrun = 1 indicates the processor has not read last character in the RxDB within one character time + 1/2 RxC period after RxDA is asserted. Subsequent characters will be lost. ROR is cleared on reading $RDSR_H$, reset operation, or dropping of RxE.
12–14	ABC	BOP	Assembled bit count. Specifies the number of bits in the last received data character of a message and should be examined by the processor when REOM = 1(RxDA and RxSA asserted). ABC = 0 indicates the message was terminated (by a flag or GA) on a character boundary as specified by PCR_{8-10}. Otherwise, ABC = number of bits in the last data character. ABC is cleared when $RDSR_H$ is read, reset operation, or dropping RxE. The residual character is right justified in$RDSR_L$.
15	RERR	BOP/BCP	Receiver error indicator should be examined by the processor when REOm = 1 in BOP, or when the processor determines the last data character of the message in BCP with CRC or when RxSA is set in BCP with VRC. CRC–CCITT preset to 1's/0's as specified by $PCSAR_{8-10}$: RERR = 1 indicates FCS error (CRC ≠ F0B8 or ≠ 0) RERR = 0 indicates FCS received correctly (CRC = F0B8 or = 0) CRC–16 preset to 0's on 8-bit characters specified by $PSCAR_{8-10}$: RERR = 1 indicates CRC–16 received correctly (CRC = 0). RERR = 0 indicates CRC–16 error (CRC≠0) VRC specified by $PCSAR_{8-10}$: RERR = 1 indicates VRC error RERR = 0 indicates VRC is correct.

DC ELECTRICAL CHARACTERISTICS[1, 2]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			
Output voltage						
V_{OL}	Low	I_{OL} = 1.6mA			0.4	V
V_{OH}	High	I_{OH} = –100µA	2.4			
I_{CC}	Power supply current	V_{CC} = 5.25V, T_A = 0°C			150	mA
Leakage current						
I_{IL}	Input	V_{IN} = 0 to 5.25V			10	µA
I_{OL}	Output	V_{OUT} = 0 to 5.25V			10	
Capacitance						
C_{IN}	Input	V_{IN} = 0V, f = 1MHz			20	pF
C_{OUT}	Output	V_{OUT} = 0V, f = 1MHz			20	

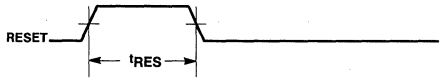
AC ELECTRICAL CHARACTERISTICS[1, 2, 3]

PARAMETER		2MHz CLOCK			UNIT
		Min	Typ	Max	
Set-up and hold time					
t_{ACS}	Address/control set-up	50			
t_{ACH}	Address/control hold	0			
t_{DS}	Data bus set-up (write)	50			ns
t_{DH}	Data bus hold (write)	0			
t_{RXS}	Receiver serial data set-up	150			
t_{RxH}	Receiver serial data hold	150			
Pulse width					
t_{RES}	RESET	250			ns
t_{DBEN}	DBEN	250		m[4]	
Delay Time					
t_{DD}	Data bus (read)			170	ns
t_{TxD}	Transmit serial data			250	
t_{DBEND}	DBEN to DBEN delay	200			
t_{DF}	Data bus float time (read)			150	ns
f	Clock (RxC, TxC) frequency			2.0	MHz
t_{CLK1}	Clock high (MM = 0)	165			
t_{CLK2}	Clock high (MM = 1)	240			ns
t_{CLK0}	Clock low	240			

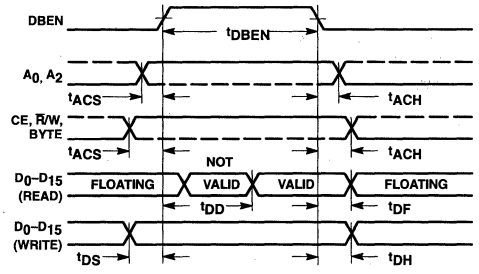
NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified. See ordering code table for applicable temperature range and operating supply range.
2. All voltage measurements are referenced to ground. All time measurements are at 0.8V or 2.0V. Input voltage levels for testing are 0.4V and 2.4V.
3. Output load C_L = 100pF.
4. m = TxC low and applies to writing to $TDSR_H$ only.

TIMING DIAGRAMS

RESET

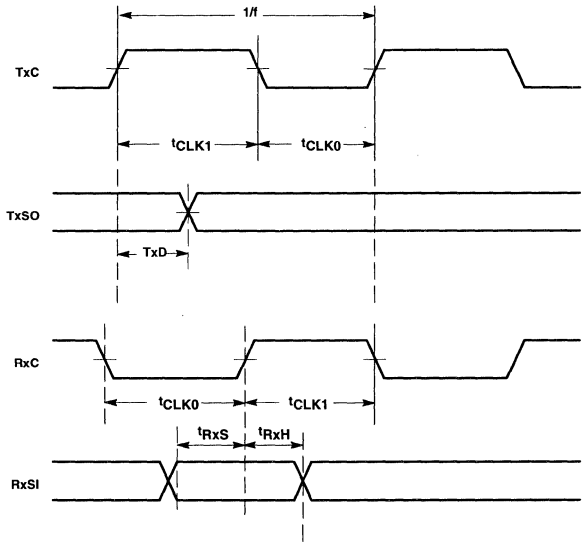


RESET AND WRITE DATA BUS

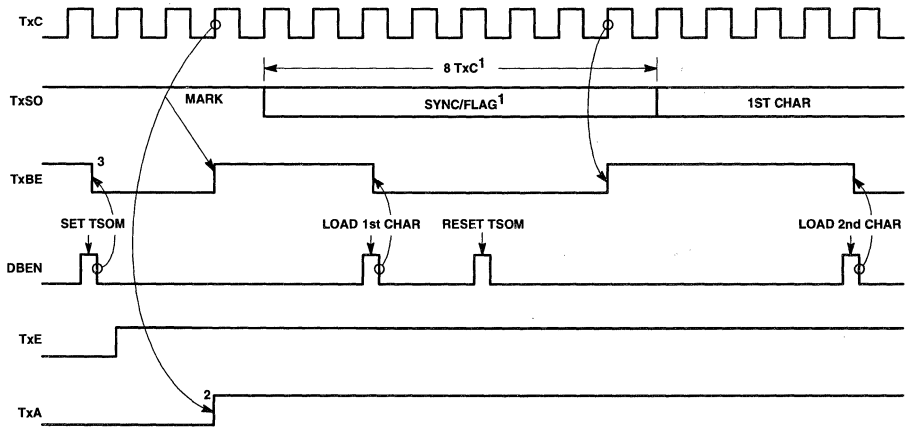


TIMING DIAGRAMS (Continued)

CLOCK



TRANSMIT – START OF MESSAGE

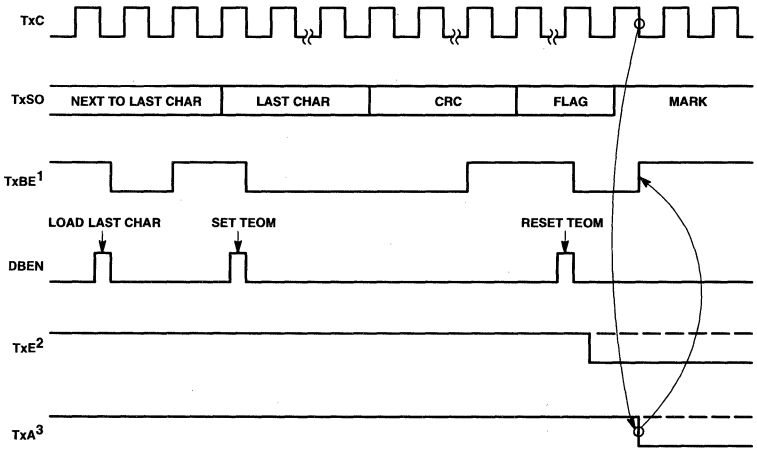


NOTES:

1. SYNC may be 5 to 8 bits and will contain parity bit as specified.
2. TxA goes high relative to TxC rising edge after TSOM has been set and TxE has been raised.
3. TxBE goes low relative to DBEN falling edge on the first write transfer into TDSR. It is reasserted 1 TxC time before the first bit of the transmitted SYNC/FLAG. TxBE then goes low relative to DBEN falling edge when writing into $TDSR_H$ and/or $TDSR_L$. It is reasserted on the rising edge of the TxC that corresponds to the transmission of the last bit of each character, except in BOP mode when the CRC is to be sent as the next character (see Transmit Timing–End of Message).

TIMING DIAGRAMS (Continued)

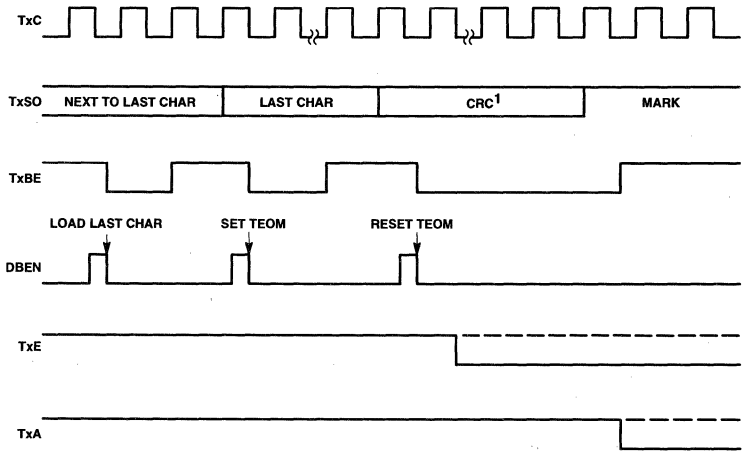
TRANSMIT – END OF BOP MESSAGE



NOTES:

1. TxBE goes low relative to the falling edge of DBEN corresponding to loading $TDSR_{H/L}$. It goes high one TxC before character transmission begins and also when TxA has been dropped.
2. TxE can be dropped before resetting TEOM if TxBE (corresponding to the closing FLAG) is high. Alternatively TxE can remain high and a new message initiated.
3. TxA goes low after TxE has been dropped and 1 1/2 TxC's after the last bit of the closing FLAG has been transmitted.

TRANSMIT TIMING – END OF BCP MESSAGE

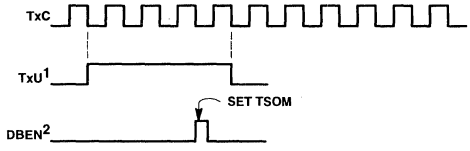


NOTE:

1. When SCN2652 generated CRC is not required. TEOM should only be set if SYNCs are to follow the message block. In that case, TxE should be dropped in response to TxBE (which corresponds to the start of transmission of the last character). When CRC is required, TxE must be dropped before CRC transmission is complete. Otherwise, the contents of TxDB will be shifted out on TxSO. This facilitates transmission of contiguous messages.

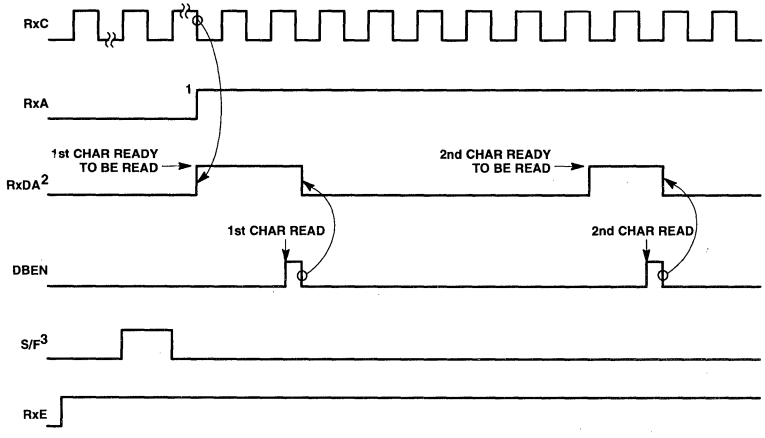
TIMING DIAGRAMS (Continued)

TRANSMIT UNDERRUN



NOTES:
1. TxU goes active relative to TxC falling edge if TxBE has not been serviced after n-1/2 TxC times (where n = transmit character length). TxU is reset on the TxC falling edge following assertion of the TSOM command.
2. An underrun will occur at the next character boundary if TEOM is reset and the transmitter remains enabled, unless the TSOM command is asserted or a character is loaded into the TxDB.

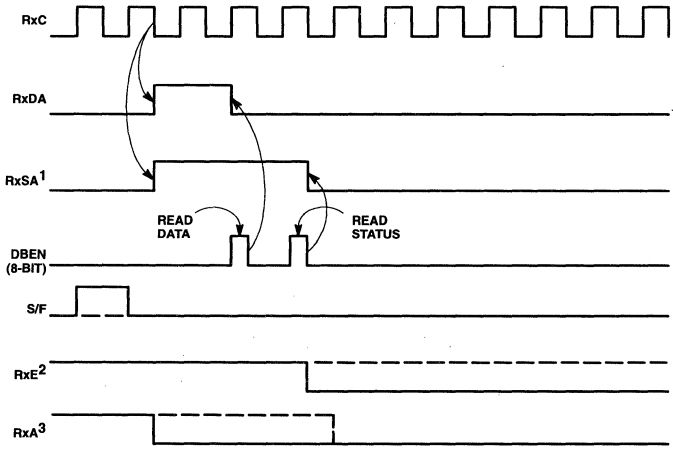
RECEIVE – START OF MESSAGE



NOTES:
1. RxA goes high relative to falling edge of RxC when RxE is high and: a. A data character following two SYNC's is in RxDB (BCP mode). b. Character following FLAG is in RxDB (BOP primary station mode). c. Character following FLAG is in RxDB and character matches the secondary station address or all parties address (BOP secondary station mode).
2. RxDA goes high on RxC falling edge when a character in RxDB is ready to be read. It comes up before RxSA and goes low on the falling edge of DBEN when RxDB is read.
3. S/F goes high relative to rising edge of RxC anytime a SYNC (BCP) or FLAG (BOP) is detected.

TIMING DIAGRAMS (Continued)

RECEIVE END OF MESSAGE

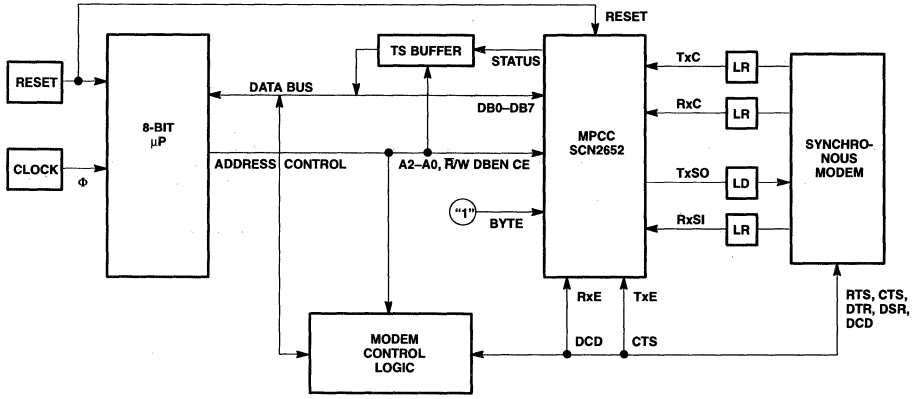


NOTES:

1. At the end of a BOP message, RxSA goes high when FLAG detection (S/F 1) forces REOm to be set. Processor should read the last data character ($RDSR_L$) and status ($RDSR_H$) which resets RxDA and RxSA respectively. For BCP end of message, RxSA may not be set and S/F = 0. The processor should read the last data character and status.
2. RxE must be dropped for BCP with non-contiguous messages. It may be left on at the end of a BOP message (see BOP Receive Operation).
3. RxA is reset relative to the falling edge of RxC after the closing FLAG of a BOP message (REOM = 1 and RxSA active.) or when RxE is dropped.

TYPICAL APPLICATIONS

SCN2652 MPCC MICROPROCESSOR INTERFACE

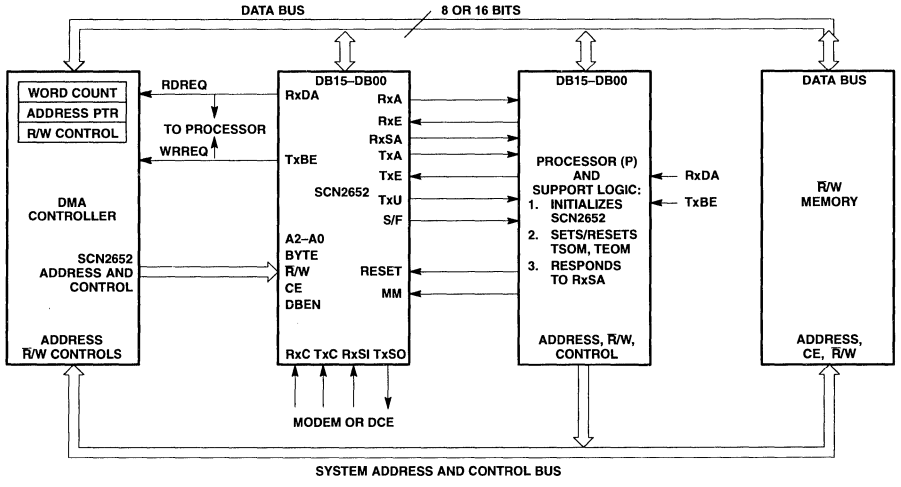


NOTES:

1. Possible µP interrupt requests are: RxDA RxSA TxBE TxU
2. Other SCN2652 status signals and possible uses are S F line idle indicator, frame delimiter. RxA handshake on RxE, line turn around control. TxA handshake on TxE, line turn around control.
3. Line drivers/receivers (LD/LR) convert EIA to TTL voltages and vice-versa.
4. RTS should be dropped after the CRC (BCP) or FLAG (BOP) has been transmitted. This forces CTS low and TxE low.
5. Corresponding high and low order bits of DB must be OR tied.

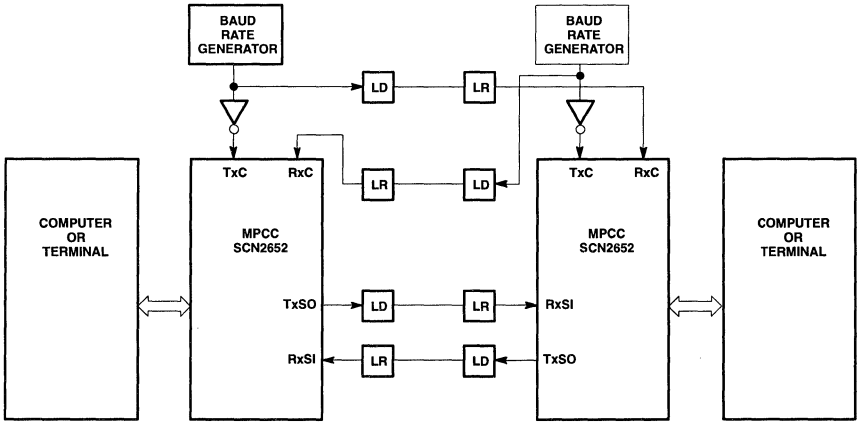
TYPICAL APPLICATIONS (Continued)

DMA/PROCESSOR INTERFACE



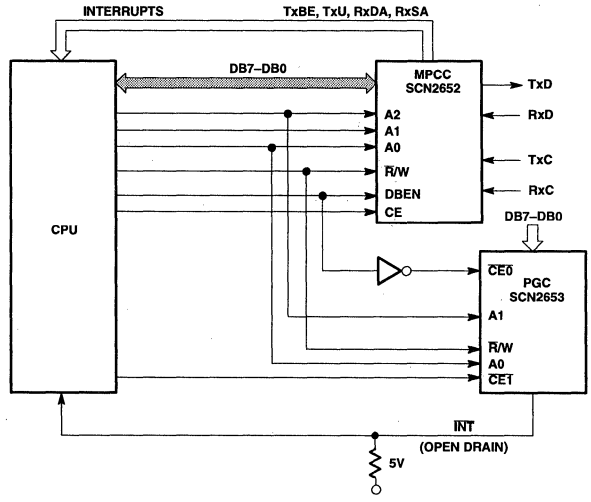
For non-DMA operation TxBE and RxDA are set to the processor which then loads or reads data characters as required.

CHANNEL INTERFACE



No Modem – DC Baseband Transmission

SCN2652/SCN2653 INTERFACE TYPICAL PROTOCOLS: BISYNC, DDCMP, SDLC, HDLC



Enhanced programmable communications interface (EPCI)

SCN2661/SCN68661

DESCRIPTION

The Philips Semiconductors SCN2661 EPCI is a universal synchronous/asynchronous data communications controller chip that is an enhanced version of the SCN2651. It interfaces easily to all 8-bit and 16-bit microprocessors and may be used in a polled or interrupt driven system environment. The SCN2661 accepts programmed instructions from the microprocessor while supporting many serial data communications disciplines —synchronous and asynchronous — in the full- or half-duplex mode. Special support for BISYNC is provided.

The EPCI serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

The SCN2661 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. Each version of the EPCI (A, B, C) has a different set of baud rates.

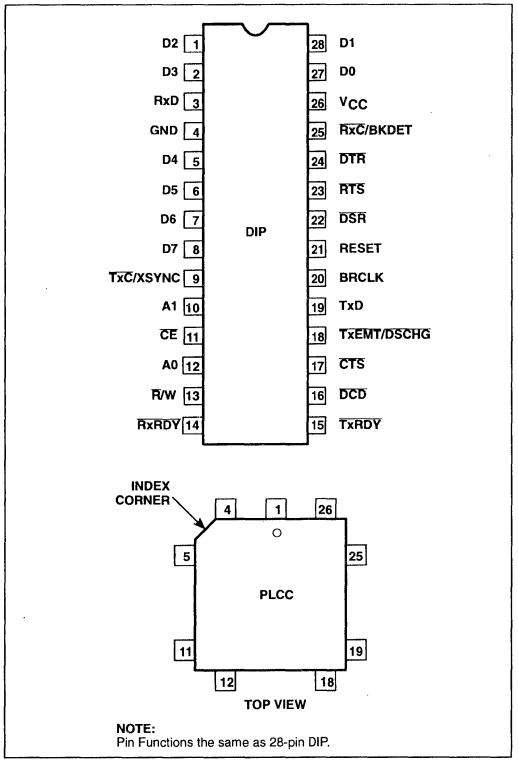
FEATURES

- Synchronous operation
  - 5- to 8-bit characters plus parity
  - Single or double SYN operation
  - Internal or external character synchronization
  - Transparent or non-transparent mode
  - Transparent mode DLE stuffing (Tx) and detection (Rx)
  - Automatic SYN or DLE-SYN insertion SYN, DLE and DLESYN stripping
  - Odd, even, or no parity
  - Local or remote maintenance loopback mode
  - Baud rate: DC to 1Mbps (1X clock)
- Asynchronous operation
  - 5- to 8-bit characters plus parity
  - 1, 1-1/2 or 2 stop bits transmitted
  - Odd, even, or no parity
  - Parity, overrun and framing error detection
  - Line break detection and generation
  - False start bit detection
  - Automatic serial echo mode (echoplex)
  - Local or remote maintenance loopback mode
  - Baud rate: DC to 1Mbps
    (1X clock)
    DC to 62.5kbps (16X clock)
    DC to 15.625kbps
    (64X clock)

OTHER FEATURES

- Internal or external baud rate clock
- 3 baud rate sets
- 16 internal rates for each set
- Double-buffered transmitter and receiver

PIN CONFIGURATIONS



NOTE:
Pin Functions the same as 28-pin DIP.

- Dynamic character length switching
- Full- or half-duplex operation
- TTL compatible inputs and outputs
- RxC and TxC pins are short-circuit protected
- Single +5V power supply
- No system clock required

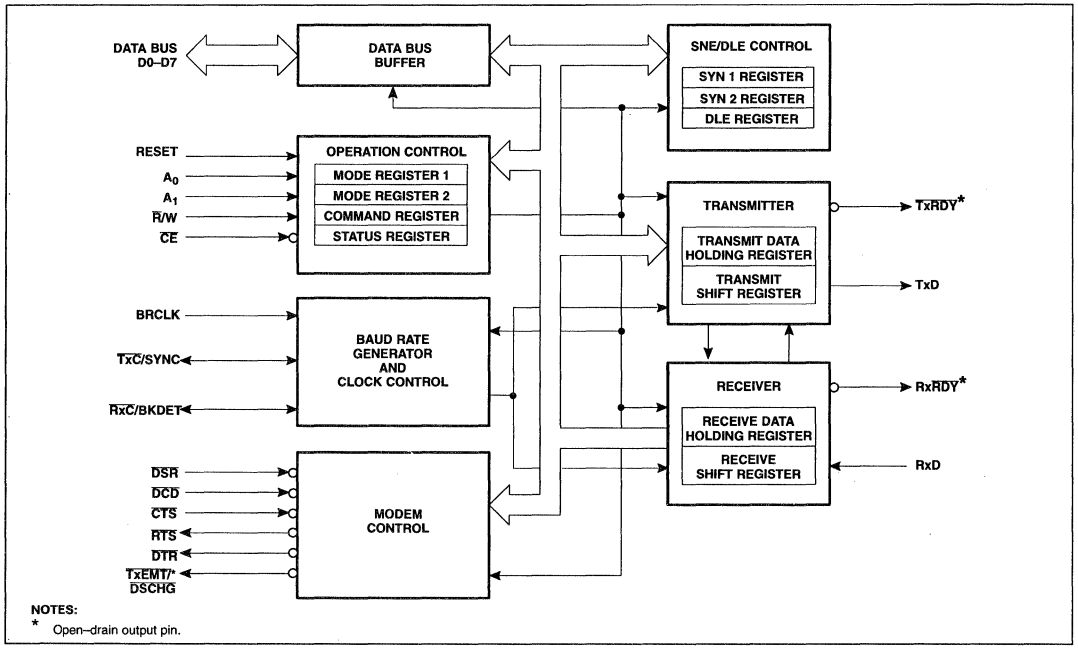
APPLICATIONS

- Intelligent terminals
- Network processors
- Front-end processors
- Remote data concentrators
- Computer-to-computer links
- Serial peripherals
- BISYNC adaptors

ORDERING CODE

PACKAGES	V_{CC} = +5V ±5%		DWG #
	Commercial 0°C to +70°C	Automotive -40°C to +85°C	
28-Pin Ceramic Dual In-Line Package (cerdip) 0.6" Wide	SCN2661BC1F28 SCN2661CC1F28	SCN2661BA1F28 SCN2661CA1F28	0589B
28-Pin Plastic Dual In-Line Package (DIP) 0.6" Wide	SCN2661AC1N28 SCN2661BC1N28 SCN2661CC1N28	Contact Factory	0413B
28-Pin Plastic Lead Chip Carrier (PLCC)	SCN2661AC1A28 SCN2661BC1A28 SCN2661CC1A28	Contact Factory	0401F

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature[2]	Note 4	°C
T_{STG}	Storage temperature	-65 to +150	°C
	All voltages with respect to ground[3]	-0.5 to +6.0	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum function temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effect of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Over recommended free-air operating temperature range and supply voltage range unless otherwise specified. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						
V_{IL} V_{IH}	Low High		2.0		0.8	V V
Output voltage						
V_{OL} V_{OH}[4]	Low High	I_{OL} = 2.2mA I_{OH} = -400µA	2.4		0.4	V V
I_{IL}	Input leakage current	V_{IN} = 0 to 5.5V			10	µA
3-State output leakage current						
I_{LH} I_{LL}	Data bus high Data bus low	V_O = 4.0V V_O = 0.45V			10 10	µA µA
I_{CC}	Power supply current				150	mA

NOTES:
1. Over recommended free-air operating temperature range and supply voltage range unless otherwise specified. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2. All voltages measurements are referenced to ground. All time measurements are at the 50% level for inputs (except t_{BRH} and t_{BRL}) and at 0.8V and 2.0V for outputs. Input levels swing between 0.4V and 2.4V, with a transition time of ≤ 20ns maximum.
3. Typical values are at +25°C, typical supply voltages and typical processing parameters.
4. $\overline{INTR}$, $\overline{TxRDY}$, $\overline{RxRDY}$ and $\overline{TxEMT/DSCHG}$ outputs are open-drain.

CAPACITANCE T_A = 25°C, V_{CC} = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Capacitance						
C_{IN} C_{OUT} $C_{I/O}$	Input Output Input/Output	f_C = 1MHz Unmeasured pins tied to ground			20 20 20	pF pF pF

AC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Pulse width						
t_{RES}	Reset		1000			ns
t_{CE}	Chip enable		250			ns
Setup and hold time						
t_{AS}	Address setup		10			ns
t_{AH}	Address hold		10			ns
t_{CS}	R/$\overline{W}$ control setup		10			ns
t_{CH}	R/$\overline{W}$ control hold		10			ns
t_{DS}	Data setup for write		150			ns
t_{DH}	Data hold for write		10			ns
t_{RXS}	RX data setup		300			ns
t_{RXH}	RX data hold		350			ns
t_{DD}	Data delay time for read	C_L = 150pF			200	ns
t_{DF}[7]	Data bus floating time for read	C_L = 150pF			100	ns
t_{CED}	CE to CE delay		600			ns
Input clock frequency						
f_{BRG}	Baud rate generator (2661A, B)		1.0	4.9152	4.9202	MHz
f_{BRG}	Baud rate generator (2661C)		1.0	5.0688	5.0738	MHz
$f_{R/T}$[6]	$\overline{TxC}$ or $\overline{RxC}$		dc		1.0	MHz
Clock width						
t_{BRH}[5]	Baud rate High (2661A, B)		75			ns
t_{BRH}[5]	Baud rate High (2661C)		70			ns
t_{BRL}[5]	Baud rate Low (2661A, B)		75			ns
t_{BRL}[5]	Baud rate Low (2661C)		70			ns
$t_{R/TH}$	$\overline{TxC}$ or $\overline{RxC}$ High		480			ns
$t_{R/TL}$[6]	$\overline{TxC}$ or $\overline{RxC}$ Low		480			ns
t_{TXD}	TxD delay from falling edge of $\overline{TxC}$	C_L = 150pF			650	ns
t_{TCS}	Skew between TxD changing and falling edge of $\overline{TxC}$ output[4]	C_L = 150pF		0		ns

NOTES:
1. Over recommended free-air operating temperature range and supply voltage range unless otherwise specified. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2. All voltages measurements are referenced to ground. All time measurements are at the 50% level for inputs (except t_{BRH} and t_{BRL}) and at 0.8V and 2.0V for outputs. Input levels swing between 0.4V and 2.4V, with a transition time of ≤ 20ns maximum.
3. Typical values are at +25°C, typical supply voltages and typical processing parameters.
4. Parameter applies when internal transmitter clock is used.
5. Under test conditions of 5.0688MHz f_{BRG} (68661) and 4.9152MHz f_{BRG} (68661A, B), t_{BRH} and t_{BRL} measured at V_{IH} and V_{IL}, respectively.
6. In asynchronous local loopback mode, using 1X clock, the following parameters apply: $f_{R/T}$ = 0.83MHz max and $t_{R/TL}$ = 700ns min.
7. See AC load conditions.

BLOCK DIAGRAM

The EPCI consists of six major sections. These are the transmitter, receiver, timing, operation control, modem control and SYN/DLE control. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

Operation Control

This functional block stores configuration and operation commands from the CPU and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus and contains mode registers 1 and 2, the command register, and the status register. Details of register addressing and protocol are presented in the EPCI programming section of this data sheet.

Timing

The EPCI contains a Baud Rate Generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full-duplex operation. See Table 1.

Receiver

The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU.

Transmitter

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate characters or bits (based on

the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Modem Control

The modern control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modem.

SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the CPU. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

Table 1. Baud Rate Generator Characteristics

68661A (BRCLK = 4.9152MHz)

MR23–20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	—	6144
0001	75	1.2	—	4096
0010	110	1.7598	–0.01	2793
0011	134.5	2.152	—	2284
0100	150	2.4	—	2048
0101	200	3.2	—	1536
0110	300	4.8	—	1024
0111	600	9.6	—	512
1000	1050	16.8329	0.196	292
1001	1200	19.2	—	256
1010	1800	28.7438	–0.19	171
1011	2000	31.9168	–0.26	154
1100	2400	38.4	—	128
1101	4800	76.8	—	64
1110	9600	153.6	—	32
1111	19200	307.2	—	16

68661B (BRCLK = 4.9152MHz)

MR23–20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	45.5	0.7279kHz	0.005	6752
0001	50	0.8	—	6144
0010	75	1.2	—	4096
0011	110	1.7598	–0.01	2793
0100	134.5	2.152	—	2284
0101	150	2.4	—	2048
0110	300	4.8	—	1024
0111	600	9.6	—	512
1000	1200	19.2	—	256
1001	1800	28.7438	–0.19	171
1010	2000	31.9168	–0.26	154
1011	2400	38.4	—	128
1100	4800	76.8	—	64
1101	9600	153.6	—	32
1110	19200	307.2	—	16
1111	38400	614.4	—	8

68661C (BRCLK = 5.0688MHz)

MR23–20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	—	6336
0001	75	1.2	—	4224
0010	110	1.76	—	2880
0011	134.5	2.1523	0.016	2355
0100	150	2.4	—	2112
0101	300	4.8	—	1056
0110	600	9.6	—	528
0111	1200	19.2	—	264
1000	1800	28.8	—	176
1001	2000	32.081	0.253	158
1010	2400	38.4	—	132
1011	3600	57.6	—	88
1100	4800	76.8	—	66
1101	7200	115.2	—	44
1110	9600	153.6	—	33
1111	19200	316.8	3.125	16

NOTE: 16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X and BRG can be used only for TxC.

OPERATION

The functional operation of the 68661 is programmed by a set of control words supplied by the CPU. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the EPCI programming section of the data sheet.

After programming, the EPCI is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the CPU to a serial bit stream. These actions are accomplished within the framework specified by the control words.

Receiver

The 68661 is conditioned to receiver data when the $\overline{DCD}$ input is Low and the RxEN bit in the commands register is true. In the asynchronous mode, the receiver looks for High-to-Low (mark to space) transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit-time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and one stop bit have been assembled. The data are then transferred to the receive data holding register, the RxRDY bit in the status register is set, and the $\overline{RxRDY}$ output is asserted. If the character length is less than 8 bits, the High order unused bits in the holding register are set to zero. The parity error, framing error, and overrun error status bits are strobed into the status register on the positive going edge of $\overline{RxC}$ corresponding to the received character boundary. If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space as a start bit if it persists into the next bit timer interval. If a break condition is detected (RxD is Low for the entire character as well as the stop bit), only one character consisting of all zeros (with the FE status bit SR5 set) will be transferred to the holding register. The RxD input must return to a High condition before a search for the next start bit begins.

Pin 25 can be programmed to be a break detect output by appropriate setting of MR27-MR24. If so, a detected break will cause that pin to go High. When RxD returns to mark for one RxC time, pin 25 will go low. Refer to the Break Detection Timing Diagram.

When the EPCI is initialized into the synchronous mode, the receiver first enters the hunt mode on a 0 to 1 transition of RxEN (CR2). In this mode, as data are shifted into the receiver shift register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly mode begins. If single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the EPCI returns to the hunt mode. (Note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization.) When synchronization has been achieved, the EPCI continues to assemble characters and transfer then to the holding register, setting the RxRDY status bit and asserting the $\overline{RxRDY}$ output each time a character is transferred. The PE and OE status bits are set as appropriate. Further receipt of the appropriate SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the holding register. Note that the SYN characters used to establish initial synchronization are not transferred to the holding register in any case.

External jam synchronization can be achieved via pin 9 by appropriate setting of MR27-MR24. When pin 9 is an XSYNC input, the internal SYN1, SYN1–SYN2, and DLE–SYN1 detection is disabled. Each positive going signal on XSYNC will cause the receiver to establish synchronization on the rising edge of the next RxC pulse. Character assembly will start with the RxD input at this edge. XSYNC may be lowered on the next rising edge of RxD. This external synchronization will cause the SYN DETECT status bit to be set until the status register is read. Refer to XSYNC timing diagram.

Table 2. CPU-Related Signals

PIN NAME	PIN NO.	INPUT/ OUTPUT	FUNCTION
RESET	21	I	A High on this input performs a master reset on the 68661. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.
A0, A1	12,10	I	Address lines used to select internal EPCI registers.
$\overline{R}$/W	13	I	Read command when Low, write command when High.
$\overline{CE}$	11	I	Chip enable command. When Low, indicates that control and data lines to the EPCI are valid and that the operation specified by the $\overline{RW}$, A1 and A0 inputs should be performed. When High, places the D0–D7 lines in the 3-State condition.
D0–D7	27,28,1,2,5–8	I/O	8-bit, 3-State data bus used to transfer commands, data and status between EPCI and the CPU. D0 is the least significant bit, D7 the most significant bit.
$\overline{TxRDY}$	15	O	This output is the complement of status register bit SR0. When Low, it indicates that the transmit data holding register (THR) is ready to accept a data character from the CPU. It goes High when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open-drain output which can be used as an interrupt to the CPU.
$\overline{RxRDY}$	14	O	This output is the complement of status register bit SR1. When Low, it indicates that the receive data holding register (RHR) has a character ready for input to the CPU. It goes High when the RHR is read by the CPU, and also when the receiver is disabled. It is an open-drain output which can be used as an interrupt to the CPU.
$\overline{TxEMT/DSCHG}$	18	O	This output is the complement of status register bit SR2. When Low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This output goes High when the status register is ready by the CPU, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the CPU for this line to go high. It is an open-drain output which can be used as an interrupt to the CPU. See Status Register (SR2) for details.

Table 3. Device-Related Signals

PIN NAME	PIN NO.	INPUT/ OUTPUT	FUNCTION
BRCLK	20	I	Clock input to the internal baud rate generator (see Table 1). Not required if external receiver and transmitter clocks are used.
$\overline{RxC}$/BKDET	25	I/O	Receiver clock. If external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin can be a 1X/16X clock or a break detect output pin.
$\overline{TxC}$/XSYNC	9	I/O	Transmitter clock. If external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. The transmitted data changes on the falling edge of the clock. If internal transmitter clock is programmed, this pin can be a 1X/16X clock output or an external jam synchronization input.
RxD	3	I	Serial data input to the receiver. "Mark" is High, "space" is Low.
TxD	19	O	Serial data output from the transmitter. "Mark" is High, "Space" is Low. Held in mark condition when the transmitter is disabled.
$\overline{DSR}$	22	I	General purpose input which can be used for data set ready or ring indicator condition. Its complement appears as status register bit SR7. Causes a Low output on $\overline{TxEMT/DSCHG}$ when its state changes if CR2 or CR0 = 1.
$\overline{DCD}$	16	I	Data carrier detect input. Must be Low in order for the receiver to operate. Its complement appears as status register bit SR6. Causes a Low output on $\overline{TxEMT/DSCHG}$ when its state changes if CR2 or CR0 = 1. If $\overline{DCD}$ goes High while receiving, the RxC is internally inhibited.
$\overline{CTS}$	17	I	Clear to send input. Must be Low in order for the transmitter to operate. If it goes High during transmission, the character in the transmit shift register will be transmitted before termination.
$\overline{DTR}$	24	O	General purpose output which is the complement of command register bit CR1. Normally used to indicate data terminal ready.
$\overline{RTS}$	23	O	General purpose output which is the complement of command register bit CR5. Normally used to indicate request to send. See Command Register (CR5) for details.

Transmitter

The EPCI is conditioned to transmit data when the $\overline{CTS}$ input is Low and the TxEN command register bit is set. The 68661 indicates to the CPU that it can accept a character for transmission by setting the TxRDY status bit and asserting the $\overline{TxRDY}$ output. When the CPU writes a character into the transmit data holding register, these conditions are negated. Data are transferred from the holding register to the transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the transmit holding register, the TxD output remains in the marking (High) condition and the $\overline{TxEMT/DSCHG}$ output and its corresponding status bit are asserted. Transmission resumes when the CPU loads a new character into the holding register. The transmitter can be forced to output a continuous Low (BREAK) condition by setting the send break command bit (CR3) High.

In the synchronous mode, when the 68661 is initially conditioned to transmit, the TxD output remains High and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the CPU. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity, if commanded) are generated by the EPCI unless the CPU fails to send a new character to the EPCI by the time the transmitter has completed sending the previous character. Since synchronous communication does not allow gaps between characters, the EPCI asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, SYN1–SYN2 doublets, or DLE–SYN1 doubles, depending on the state of MR16 and MR17. Normal transmission of the message resumes when a new character is available in the transmit data holding register. If the send DLE bit in the commands register is true, the DLE character is automatically transmitted prior to transmission of the message character in the THR.

EPCI PROGRAMMING

Prior to initiating data communications, the 68661 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The EPCI can be reconfigured at any time during program execution. A flowchart of the initialization process appears in Figure 1.

The internal registers of the EPCI are accessed by applying specific signals to the $\overline{CE}$, $\overline{R}/W$, A1 and A0 inputs. The conditions necessary to address each register are shown in Table 4.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions A1 = 0, A0 = 1, and $\overline{R}/W$ = 1. The first operation loads the SYN1 register. The next loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses mode register 1, and a subsequent operation addresses mode register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 register and mode register 1 by a RESET input or by performing a read command register operation, but are unaffected by any other read or write operation.

The 68661 register formats are summarized in Tables 5, 6, 7 and 8. Mode registers 1 and 2 define the general operational characteristics of the EPCI, while the command register controls the operation within this basic framework. The EPCI indicates its status in the status register. These registers are cleared when a RESET input is applied.

Mode Register 1 (MR1)

Table 5 illustrates mode register 1. Bits MR11 and MR10 select the communication format and baud rate multiplier. 00 specifies synchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7 or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14. In asynchronous mode, MR17 and MR16 select character framing of 1, 1.5, or 2 stop bits. (If 2X baud rate is programmed, 1.5 stop bits defaults to 1 stop bits on transmit.) In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17 = 1, and SYN1–SYN2 is used when MR17 = 0. If the transparent mode is specified by MR16, DLE–SYN1 is used for character fill and SYN detect, but the normal synchronization sequence is used to establish character sync. When transmitting, a DLE character in the transmit holding register will cause a second DLE character to be transmitted. This DLE stuffing eliminates the software DLE compare and stuff on each transparent mode data character. If the send DLE command (CR3) is active when a DLE is loaded into THR, only one additional DLE will be transmitted. Also, DLE stripping and DLE detect (with MR14 = 0) are enabled.

The bits in the mode register affecting character assembly and disassembly (MR12–MR16) can be changed dynamically (during active receive/transmit operation). The character mode register affects both the transmitter and receiver; therefore in synchronous mode, changes should be made only in half-duplex mode (RxEN = 1 or TxEN = 1, but not both simultaneously = 1). In asynchronous mode, character changes should be made when RxEN and TxEN = 0 or when TxEN = 1 and the transmitter is marking in half-duplex mode (RxEN = 0).

To effect assembly/disassembly of the next received/transmitted character, MR12 – 15 must be changed within n bit times of the active going state of $\overline{RxRDY/TxRDY}$. Transparent and non-transparent mode changes (MR16) must occur within n-1 bit times of the character to be affected when the receiver or transmitter is active. (n – smaller of the new and old character lengths.)

Table 4. 68661 Register Addressing

$\overline{CE}$	A_1	A_0	R/$\overline{W}$	FUNCTION
1	X	X	X	3-State data bus
0	0	0	0	Read receive holding register
0	0	0	1	Write transmit holding register
0	0	1	0	Read status register
0	0	1	1	Write SYN1/SYN2/DLE registers
0	1	0	0	Read mode register 1/2
0	1	0	1	Write mode register 1/2
0	1	1	0	Read command register
0	1	1	1	Write command register

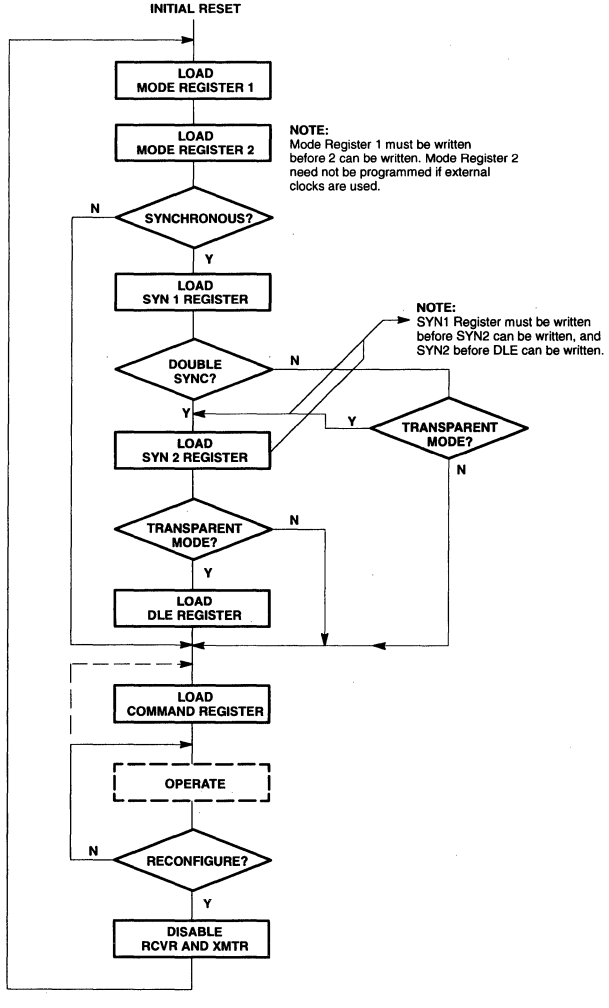


Figure 1. 68661 Initialization Flowchart

Table 5. Mode Register 1 (MR1)

MR17	MR16	MR15	MR14	MR13	MR12	MR11	MR10
Sync/Async		Parity Type	Parity Control	Character Length		Mode and Baud Rate Factor	
Async: Stop bit length 00 = invalid 01 = 1 stop bit 10 = 1 1/2 stop bits 11 = 2 stop bits		0 = Odd 1 = Even	0 = Disabled 1 = Enabled	00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits		00 = Synchronous 1X rate 01 = Asynchronous 1X rate 10 = Asynchronous 16X rate 11 = Asynchronous 64X rate	
Sync: Number of SYN char 0 = Double SYN 1 = Single SYN	**Sync: Transparency control** 0 = Normal 1 = Transparent						

NOTE: Baud rate factor in asynchronous applies only if external clock is selected. Factor is 16X if internal clock is selected. Mode must be selected (MR11, MR10) in any case.

Table 6. Mode Register 2 (MR2)

MR27 – MR24											MR23 – MR20
	TxC	RxC	Pin 9	Pin 25		TxC	RxC	Pin 9	Pin 25	Mode	Baud Rate Selection
0000	E	E	TxC	RxC	1000	E	E	XSYNC*	RXC/TxC	sync	
0001	E	I	TxC	1X	1001	E	I	TxC	BKDET	async	
0010	I	E	1X	RxC	1010	I	E	XSYNC*	RxC	sync	
0011	I	I	1X	1X	1011	I	I	1X	BKDET	async	See baud rates in Table 1.
0100	E	E	TxC	RxC	1100	E	E	XSYNC*	RxC/TxC	sync	
0101	E	I	TxC	16X	1101	E	I	TXC	BKDET	async	
0110	I	E	16X	RxC	1110	I	E	XSYNC*	RxC	sync	
0111	I	I	16X	16X	1111	I	I	16X	BKDET	async	

NOTES:
* When pin 9 is programmed as XSYNC input, SYN1, SYN1–SYN2, and DLE–SYN1 detection is disabled.
E = External clock
I = Internal clock (BRG)
1X and 16X are clock outputs.

Table 7. Command Register (CR)

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode		Request to Send	Reset Error	Sync/Async	Receive Control (RxEN)	Data Terminal Ready	Transmit Control (TxEN)
00 = Normal operation 01 = Async: Automatic Echo mode Sync: SYN and/or DLE stripping mode 10 = Local loopback 11 = Remote loopback		0 = Force $\overline{RTS}$ Output High one clock time after TxSR serialization 1 = Force $\overline{RTS}$ output Low	0 = Normal 1 = Reset error flags in status reg. (FE,OE,PE/ DLE detect.)	**Async:** Force Break 0 = Normal 1 = Force break **Sync** **Send DLE** 0 = Normal 1 = Send DLE	0 = Disable 1 = Enable Not applicable in	0 = Force $\overline{DTR}$ output High 1 = Force $\overline{DTR}$ output Low	0 = Disable 1 = Enable

Table 8. Status Register (SR)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
Data Set Ready	**Data Carrier Detect**	**FE/SYN Detect**	**Overrun**	**PE/DLE Detect**	**TxEMT DSCHG**	**RxRDY**	**TxRDY**
0 = $\overline{DSR}$ input is High 1 = $\overline{DSR}$ input is Low	0 = $\overline{DCD}$ input is High 1 = $\overline{DCD}$ input is Low	**Async:** 0 = Normal 1 = Framing error **Sync:** 0 = Normal 1 = SYN detected	0 = Normal 1 = Overrun error	**Async:** 0 = Normal 1 = Parity error **Sync:** 0 = Normal 1 = Parity error or DLE received	0 = Normal 1 = Change in $\overline{DSR}$ or $\overline{DCD}$, or transmit shift register is empty	0 = Receive holding register empty 1 = Receive holding register has data	0 = Transmit holding register busy 1 = Transmit holding register empty

Mode Register 2 (MR2)

Table 6 illustrates mode register 2. MR23, MR22, MR21 and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable for each EPCI version (–1,–2,–3). Versions 1 and 2 specify a 4.9152MHz TTL input at BRCLK (pin 20); version 3 specifies a 5.0688MHz input which is identical to the Philips Semiconductors 2651. MR23 – 20 are don't cares if external clocks are selected (MR25 – MR24 = 0). The individual rates are given in Table 1.

MR24 – MR27 select the receive and transmit clock source (either the BRG or an external input) and the function at pins 9 and 25. Refer to Table 6.

Command Register (CR)

Table 7 illustrates the command register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. A 0– to–1 transition of CR2 forces start bit search (async mode) or hunt mode (sync mode) on the second $\overline{RxC}$ rising edge. Disabling the receiver causes $\overline{RxRDY}$ to go High (inactive). If the transmitter is disabled, it will complete the transmission of the character in the transmit shift register (if any) prior to terminating operation. The TxD output will then remain in the marking state (High) while $\overline{TxRDY}$ and $\overline{TxEMT}$ will go High (inactive). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected. A 0–to–1 transition of CR2 will initiate start bit search (async) or hunt mode (sync).

Bits CR1 (DTR) and CR5 (RTS) control the $\overline{DTR}$ and $\overline{RTS}$ outputs. Data at the outputs are the logical complement of the register data.

In asynchronous mode, setting CR3 will force and hold the TxD output Low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go High for at least one bit time before beginning transmission of the next character in the transmit data holding register. In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the transmit data holding register. Since this is a one time command, CR3 does not have to be reset by software. CR3 should be set when entering and exiting transparent mode and for all DLE-non-DLE character sequences.

Setting CR4 causes the error flags in the status register (SR3, SR4, and SR5) to be cleared; this is a one time command. There is no internal latch for this bit.

When CR5 (RTS) is set, the $\overline{RTS}$ pin is forced Low. A 1–to–0 transition of CR5 will cause $\overline{RTS}$ to go High (inactive) one TxC time after the last serial bit has been transmitted. If a 1–to–0 transition of CR5 occurs while data is being transmitted, $\overline{RTS}$ will remain Low (active) until both the THR and the transmit shift register are empty and then go High (inactive) one TxC time later.

The EPCI can operate in one of four submodes within each major mode (synchronous or asynchronous). The operational sub-mode is determined by CR7 and CR6. CR7 – CR6 = 00 is the normal mode, with the transmitter and receive operating independently in accordance with the mode and status register instructions.

In asynchronous mode, CR7 – CR6 = 01 places the EPCI in the automatic echo mode. Clocked, regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2 = 1), but the transmitter need not be enabled. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled. Only the first character of a break condition is echoed.

The TxD output will go High until the next valid start is detected. The following conditions are true while in automatic echo mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. $\overline{TxRDY}$ **output = 1.**
4. The $\overline{TxEMT/DSCHG}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In synchronous mode, CR7 – CR6 = 01 places the EPCI in the automatic SYN/DLE stripping mode. The exact action taken depends on the setting of bits MR17 and MR16:

1. In the non-transparent, single SYN mode (MR17 – MR16 = 10), characters in the data stream matching SYN1 are not transferred to the Receive Data Holding register (RHR).
2. In the non-transparent, double SYN mode (MR17 – MR16 = 00), character in the data stream matching SYN1, or SYN2 if immediately preceded by SYN1, are not transferred the RHR.
3. In transparent mode (MR16 = 1), character in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However, only the first DLE of a DLE–DLE pair is stripped.

Note that automatic stripping mode does not affect the setting of the DLE detect and SYN detect status bits (SR3 and SR5).

Two diagnostic sub-modes can also be configured. In local loopback mode (CR7 – CR6 = 10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.
2. $\overline{DTR}$ is connected to $\overline{DCD}$ and $\overline{RTS}$ is connected to $\overline{CTS}$.
3. The receiver is clocked by the transmit clock.
4. The $\overline{DTR}$, $\overline{RTS}$ and $\overline{TxD}$ outputs are held High.
5. The $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ and RxD inputs are ignored.

Additional requirements to operate in the local loopback mode are that CR0 (TxEN), CR1 (DTR) and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the EPCI.

The second diagnostic mode is the remote loopback mode (CR7 – CR6 = 11). In this mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receiver clock.
3. No data are sent to the local CPU, but he error status conditions (PE, FE) are set.
4. The $\overline{RxRDY}$, $\overline{TxRDY}$, and $\overline{TxEMT/DSCHG}$ outputs are held High.
5. CR0 (TxEN) is ignored.
6. All other signals operate normally.

Status Register

The data contained in the status register (as shown in Table 8) indicates receiver and transmitter conditions and modem/data set status.

SR0 is the transmitter ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to 0–, it indicates that the transmit data holding register has been loaded by the CPU and the data has not been transferred to the transmit register. If set equal to 1, it indicates that the holding register is ready to accept data from the CPU. This bit is initially set when the transmitter is enabled by CR0, unless a character has previously been loaded into the holding register. It is not set when the automatic echo or remote loopback modes are programmed. When this bit is set, the $\overline{TxRDY}$ output pin is Low. In the automatic echo and remote loopback modes, the output is held High.

SR1, the receiver ready (RxRDY) status bit, indicates the condition of the receive data holding register. If set, it indicates that a character has been loaded into the holding register from the receive shift register and is ready to be read by the CPU. If equal to zero, there is no new character in the holding register. This bit is cleared when the CPU reads the receive data holding register or when the receiver is disabled by CR2. When set, the $\overline{RxRDY}$ output is Low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs (when CR2 or CR0 = 1) or that the transmit shift register has completed transmission of a character and no new character has been loaded into the transmit data holding register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. TxEMT will not go active until at least one character has been transmitted. It is cleared by loading the transmit data holding register. The DSCHG conditions is enabled when TxEN = 1 or RxEN = 1. It is cleared when the status register is read by the CPU. If the status register is read twice and SR2 – 1 while SR6 and SR7 remain unchanged, then a TxEMT condition exists. When SR2 is set, the $\overline{TxEMT/DSCHG}$ output is Low.

SR3, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16 = 1), with parity disabled, it indicates that a character matching DLE register was received and the present character is neither SYN2 or DLE. This bit is cleared when the next character following the above sequence is loaded into RHR, when the receiver is disabled, or by a reset error command, CR4.

The overrun error status bit, SR4, indicates that the previous character loaded into the receive holding register was not ready the CPU at the time of new received character was transferred into it. This bit is cleared when the receiver is disabled or by the reset error command, CR4.

In asynchronous mode, bit SR5 signifies that the received character was not framed by a stop bit; i.e., only the first stop bit is checked. If RHR = 0 when SR5 = 1, a break condition is present. In synchronous non-transparent mode (MR16 = 0), it indicates receipt of the SYN1 character in single SYN mode or the SYN1 – SYN2 pair in double SYN mode. In synchronous transparent mode (MR16 = 1), this bit is set upon detection of the initial synchronizing characters (SYN or SYN1 – SYN2) and, after synchronization has been achieved, when a DLE–SYN1 pair is received. The bit is reset when the receiver is disabled, when the reset error command is given in asynchronous mode, or when the status register is read by the CPU in the synchronous mode.

SR6 and SR7 reflect the conditions of the $\overline{DCD}$ and $\overline{DSR}$ inputs, respectively. A Low input sets its corresponding status bit, and a High input clears it.

Table 9. 68661 EPCI vs 2651 PCI

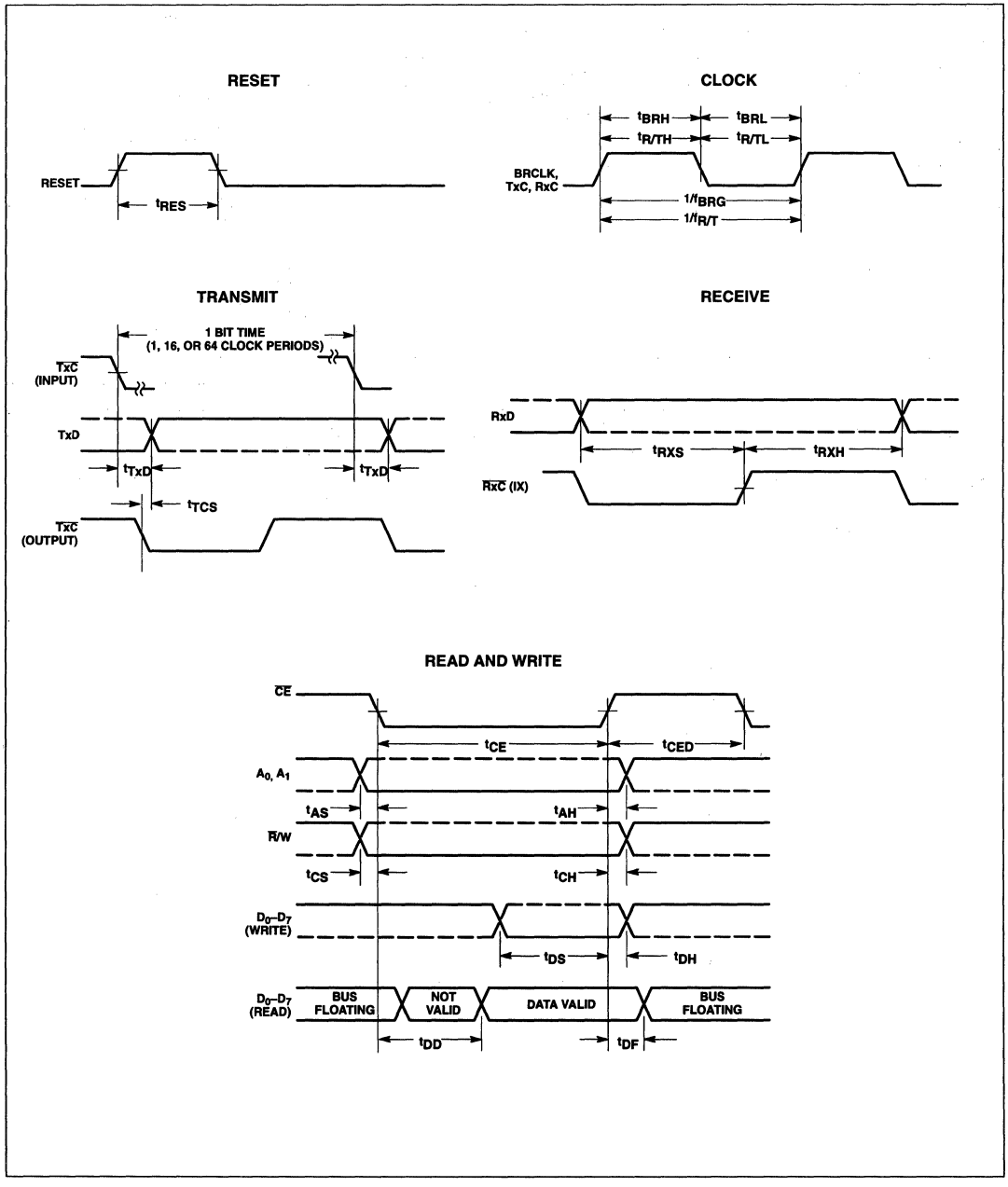
FEATURE	EPCI	PCI
1. MR2 BIT 6, 7	Control pins 9, 25	Not used
2. DLE detect – SR3	SR3 = 0 for DLE–DLE, DLE – SYN1	SR3 = 1 for DLE–DLE, DLE – SYN1
3. Reset of SR3, DLE detect	Second character after DLE, or receiver disable, or CR4 = 1	Receiver disable, or CR4 = 1
4. Send DLE – CR3	One time command	Reset via CR3 on next $\overline{\text{TxRDY}}$
5. DLE stuffing in transparent mode	Automatic DLE stuffing when DLE is loaded except if CR3 = 1	None
6. SYN1 stripping in double sync non-transparent mode	All SYN1	First SYN1 of pair
7. Baud rate versions	Three	One
8. Terminate ASYNC transmission (drop RTS)	Reset CR5 in response to $\overline{\text{TxEMT}}$ changing from 1 to 0	Reset CR0 when $\overline{\text{TxEMT}}$ goes from 1 to 0. Then reset CR5 when $\overline{\text{TxEMT}}$ goes from 1 to 0
9. Break detect	Pin 25*	FE and null character
10. Stop bit searched	One	Two
11. External jam sync	Pin 9**	No
12. Data bus timing	Improved over 2651	—
13. Data bus drivers	Sink 2.2mA Source 400µA	Sink 1.6mA Source 100µA

NOTES:
* Internal BRG used for RxC.
** Internal BRG used for TxC.

AC LOAD CONDITIONS

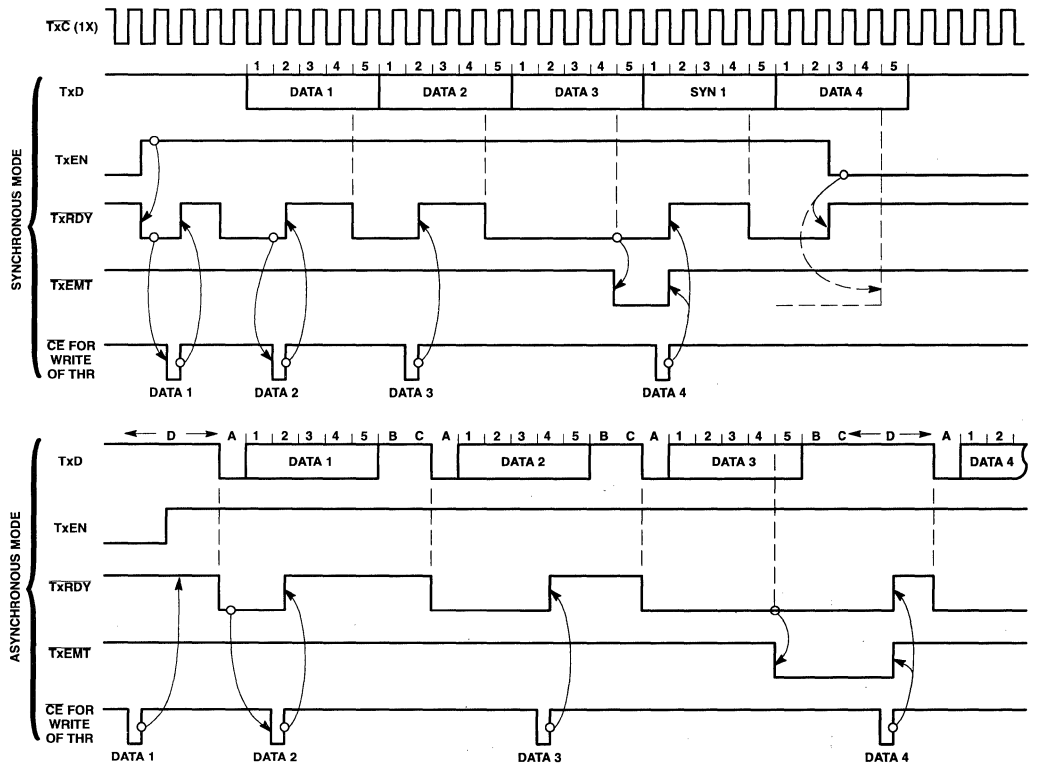
NOTES:
Open-drain outputs.
C_L = Load capacitance includes JIG and probe capacitance.

TIMING DIAGRAMS



TIMING DIAGRAMS (Continued)

TxRDY, TxEMT (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])

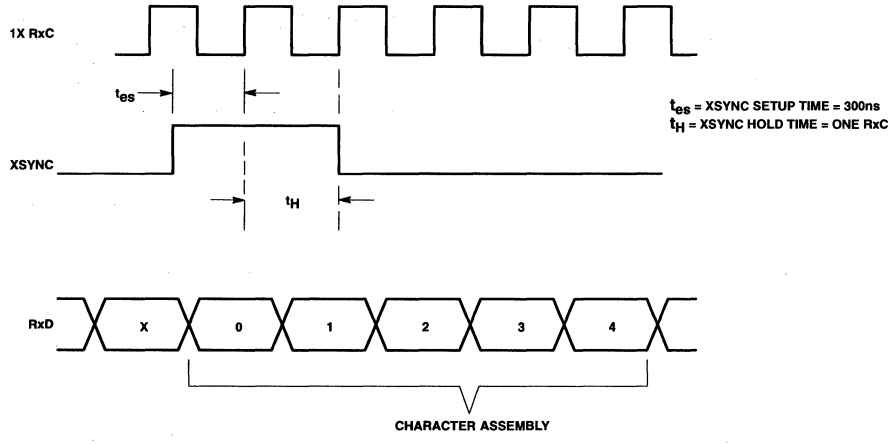


NOTES:

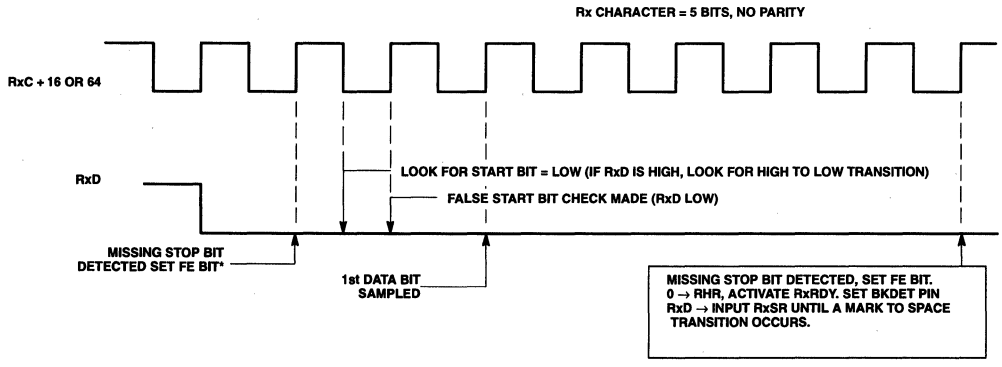
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
TxEMT goes low at the beginning of the last data bit, or, if parity is enabled, at the beginning of the parity bit.

TIMING DIAGRAMS (Continued)

EXTERNAL SYNCHRONIZATION WITH XSYNC



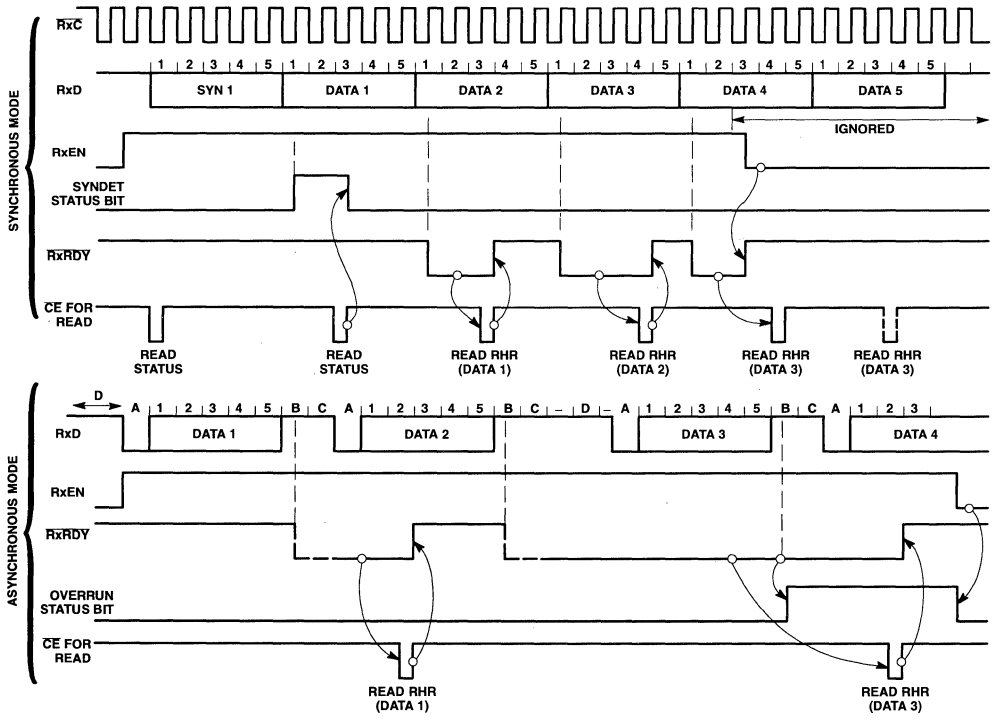
BREAK DETECTION TIMING



NOTE:
* If the stop bit is present, the start bit search will commence immediately.

TIMING DIAGRAMS (Continued)

RxRDY (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])

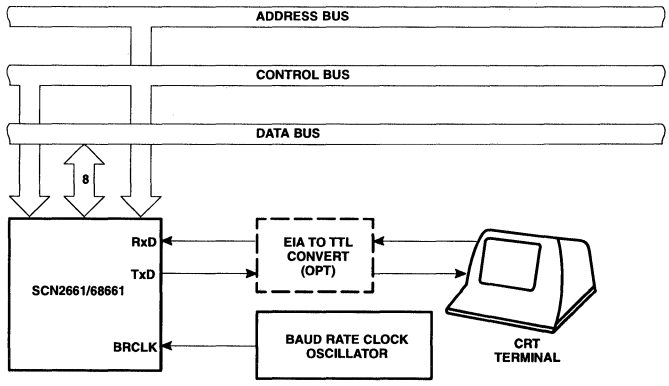


NOTES:

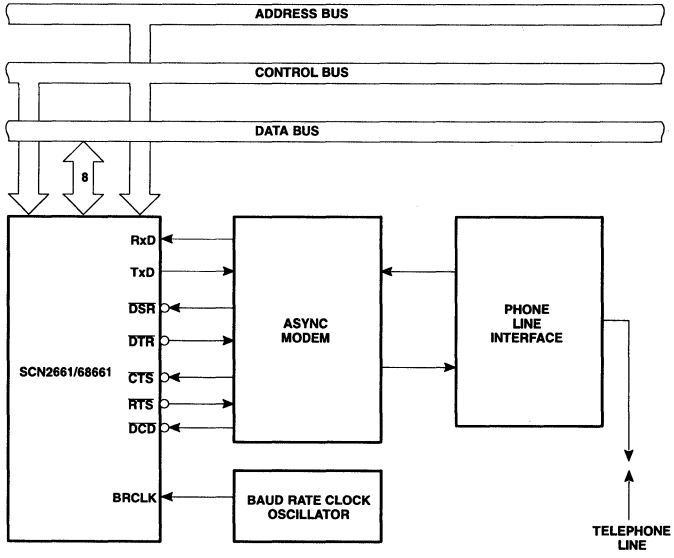
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
Only one stop bit is detected

TYPICAL APPLICATIONS

ASYNCHRONOUS INTERFACE TO CRT TERMINAL

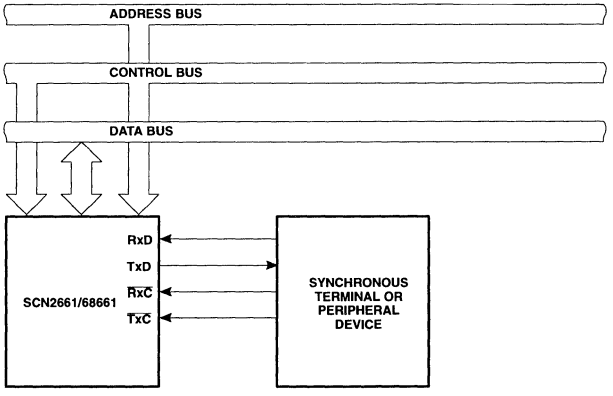


ASYNCHRONOUS INTERFACE TO TELEPHONE LINES

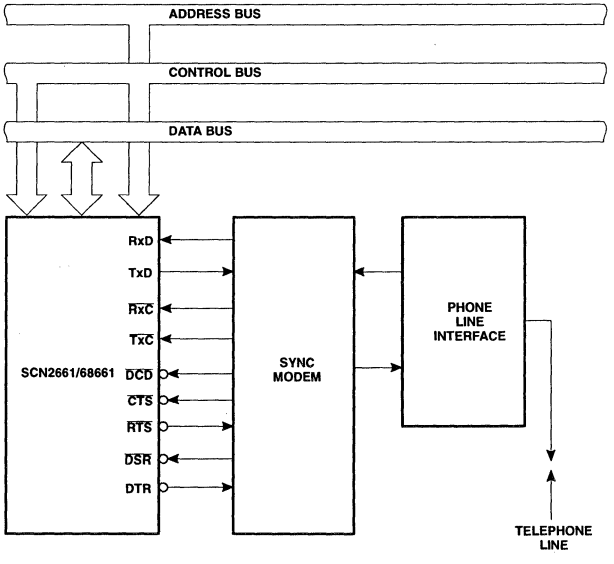


TYPICAL APPLICATIONS (Continued)

SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES



Dual asynchronous receiver/transmitter (DUART) SCN2681

DESCRIPTION

The Philips Semiconductors SCN2681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruply buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the buffer of the receiving device is full.

Also provided on the SCN2681 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The SCN2681 is available in three package versions: 40-pin and 28–pin, both 0.6" wide DIPs; a compact 24-pin 0.4" wide DIP; and a 44-pin PLCC.

FEATURES

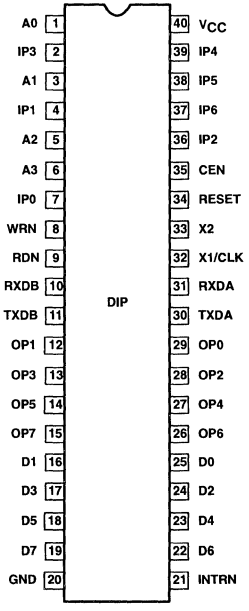
- Dual full-duplex asynchronous receiver/transmitter
- Quadruple buffered receiver data registers
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - Non-standard rates to 115.2Kb
  - One user-defined rate derived from programmable timer/counter
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function programmable 16-bit counter/timer
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
  - 100kΩ typical pull-up resistor
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer: 1X – 1MB/sec, 16X – 125kB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Single +5V power supply
- Commercial and industrial temperature ranges available
- DIP and PLCC packages

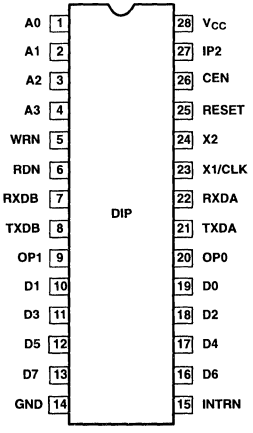
ORDERING INFORMATION

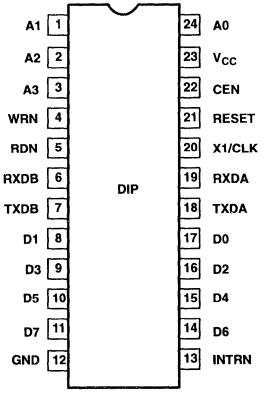
DESCRIPTION	ORDER CODE					
	Commercial			Automotive		
	V_{CC} = +5V ±5%, T_A = 0°C to +70°C			V_{CC} = +5V ±10%, T_A = -40°C to +85°C		
	Ceramic DIP	Plastic DIP	Plastic LCC	Ceramic DIP	Plastic DIP	Plastic LCC
24-Pin[1]	Not available	SCN2681AC1N24	Not available	Not available	SCN2681AE1N24	Not available
28-Pin[2]	SCN2681AC1F28	SCN2681AC1N28	Not available	SCN2681AE1F28	SCN2681AE1N28	Not available
40-Pin[2]	Not available	SCN2681AC1N40	Not available	SCN2681AE1F40	SCN2681AE1N40	Not available
44-Pin	Not available	Not available	SCN2681AC1A44	Not available	Not available	SCN2681AE1A44

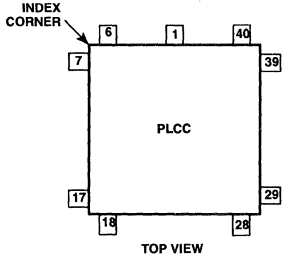
NOTES:
1. 400mil-wide Dual In-Line Package
2. 600mil-wide Dual In-Line Package

PIN CONFIGURATIONS









PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A0	24	INTRN
3	IP3	25	D6
4	A1	26	D4
5	IP1	27	D2
6	A2	28	D0
7	A3	29	OP6
8	IP0	30	OP4
9	WRN	31	OP2
10	RDN	32	OP0
11	RXDB	33	TXDA
12	NC	34	NC
13	TXDB	35	RXDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CEN
18	D1	40	IP2
19	D3	41	IP6
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	VCC

PIN DESCRIPTION

SYMBOL	APPLICABLE			TYPE	NAME AND FUNCTION
	40/44	28	24		
D0–D7	X	X	X	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	X	X	X	I	**Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A3 inputs. When High, places the D0-D7 lines in the 3-State condition.
WRN	X	X	X	I	**Write Strobe:** When Low and CEN is also Low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	X	X	X	I	**Read Strobe:** When Low and CEN is also Low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0–A3	X	X	X	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	X	X	X	I	**Reset:** A High level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Clears Test modes, sets MR pointer to MR1.
INTRN	X	X	X	O	**Interrupt Request:** Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	X	X	X	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5).
X2	X	X		I	**Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5).
RxDA	X	X	X	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	X	X	X	I	**Channel B Receive Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	X	X	X	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	X	X	X	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
OP0	X	X		O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	X	X		O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	X			O	**Output 2:** General purpose output or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	X			O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	X			O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYA/FFULLA output.
OP5	X			O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYB/FFULLB output.
OP6	X			O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYA output.
OP7	X			O	**Output 7:** General purpose output or Channel B open-drain, active-Low, TxRDYB output.
IP0	X			I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	X			I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	X	X		I	**Input 2:** General purpose input or counter/timer external clock input.
IP3	X			I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	X			I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.

PIN DESCRIPTION (Continued)

SYMBOL	APPLICABLE			TYPE	NAME AND FUNCTION
	40/44	28	24		
IP5	X			I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	X			I	**Input 6:** General purpose input or Channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	X	X		I	**Power Supply:** +5V supply input.
GND	X	X		I	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	See Note 4	°C
T_{STG}	Storage temperature range	-65 to +150	°C
	All voltages with respect to ground[3]	-0.5 to +6.0	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)[5]		2			V
V_{IH}	Input high voltage (except X1/CLK)[4]		2.5			V
V_{IH}	Input high voltage (X1/CLK)		4			V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}	Output high voltage (except o.d. outputs)[5]	I_{OH} = -400µA	2.4			V
V_{OH}	Output high voltage (except o.d. outputs)[4]	I_{OH} = -400µA	2.9			V
I_{IL}	Input leakage current	V_{IN} = 0 to V_{CC}	-10		10	µA
I_{LL}	Data bus 3-stage leakage current	V_O = 0.4 to V_{CC}	-10		10	µA
I_{X1L}	X1/CLK low input current	V_{IN} = 0, X2 grounded	-4	-2	0	mA
		V_{IN} = 0, X2 floated	-3	-1.5	0	mA
I_{X1H}	X1/CLK high input current	V_{IN} = V_{CC}, X2 grounded	-1	0.2	1	mA
		V_{IN} = V_{CC}, X2 floated	0	3.5	10	mA
I_{X2L}	X2 low input current	V_{IN} = 0, X1/CLK floated	-100	-30	0	µA
I_{X2H}	X2 high input current	V_{IN} = V_{CC}, X1/CLK floated	0	+30	100	µA
I_{OC}	Open-collector output leakage current	V_O = 0.4 to V_{CC}	-10		10	µA
I_{OCC}	Power supply current					
	0°C to +70°C version				150	mA
	-40°C to +85°C version				175	mA

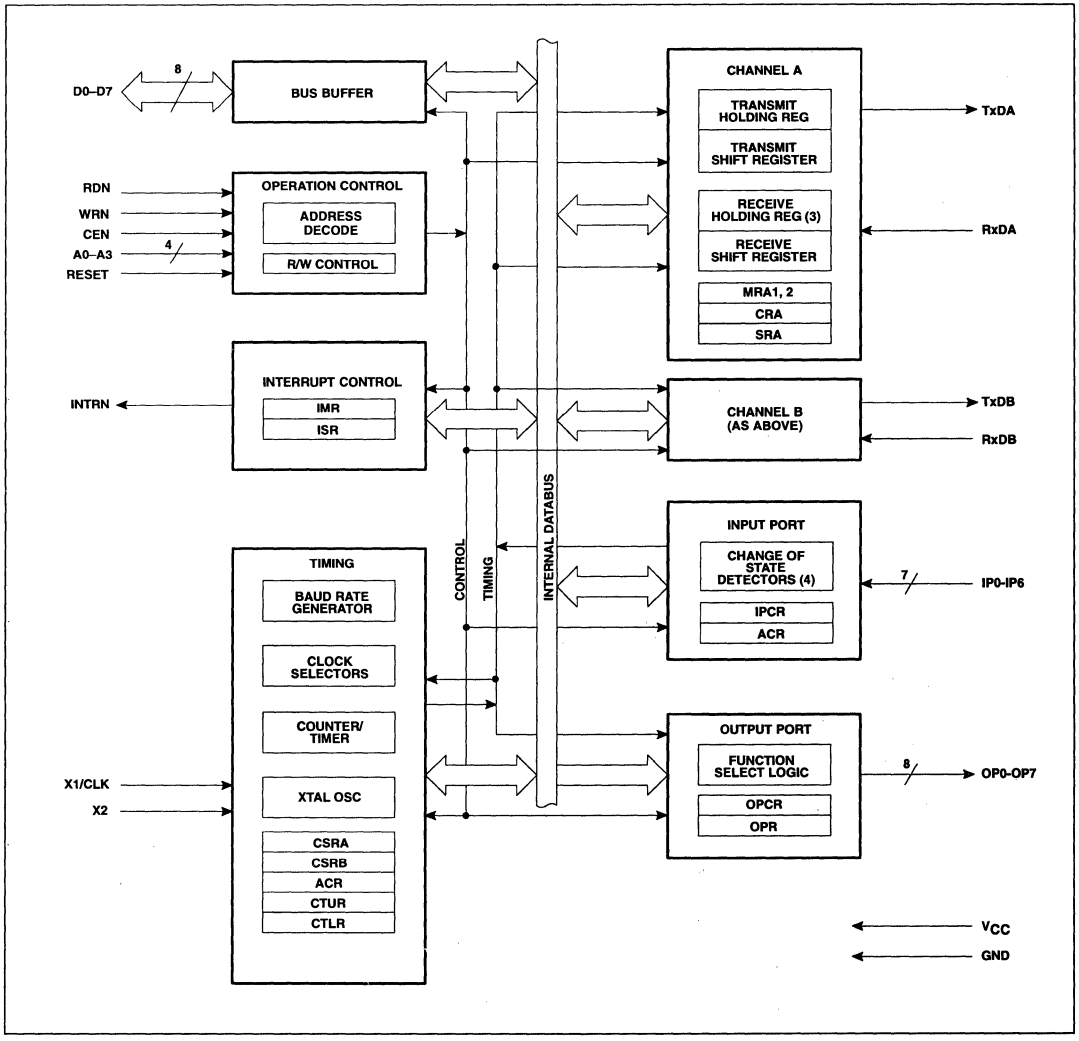
NOTES:
1. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. T_A < 0°C
5. $T_A \geq$ 0°C

AC CHARACTERISTICS T_A = -55°C to +125°C[1], V_{CC} = +5.0V ± 10%[2, 3, 4, 5]

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Reset Timing (Figure 1)					
t_{RES}	RESET pulse width	200			ns
Bus Timing (Figure 2)[6]					
t_{AS}	A0-A3 setup time to RDN, WRN Low	10			ns
t_{AH}	A0-A3 hold time from RDN, WRN Low	100			ns
t_{CS}	CEN setup time to RDN, WRN Low	0			ns
t_{CH}	CEN hold time from RDN, WRN High	0			ns
t_{RW}	WRN, RDN pulse width	225			ns
t_{DD}	Data valid after RDN Low			175	ns
t_{DF}	Data bus floating after RDN High			100	ns
t_{DS}	Data setup time before WRN High	100			ns
t_{DH}	Data hold time after WRN High	20			ns
t_{RWD}	High time between READs and/or WRITE[7, 8]	200			ns
Port Timing (Figure 3)[6]					
t_{PS}	Port input setup time before RDN Low	0			ns
t_{PH}	Port input hold time after RDN High	0			ns
t_{PD}	Port output valid after WRN High			400	ns
Interrupt Timing (Figure 4)					
t_{IR}	INTRN (or OP3-OP7 when used as interrupts) negated from:				
	Read RHR (RxRDY/FFULL interrupt)			300	ns
	Write THR (TxRDY interrupt)			300	ns
	Reset command (delta break interrupt)			300	ns
	Stop C/T command (counter interrupt)			300	ns
	Read IPCR (input port change interrupt)			300	ns
	Write IMR (clear of interrupt mask bit)			300	ns
Clock Timing (Figure 5)[10]					
t_{CLK}	X1/CLK High or Low time	100			ns
f_{CLK}	X1/CLK frequency	2.0	3.6864	4.0	MHz
t_{CTC}	CTCLK (IP2) High or Low time	100			ns
f_{CTC}	CTCLK (IP2) frequency	0		4.0	MHz
t_{RX}[9]	RxC High or Low time	220			ns
f_{RX}[9]	RxC frequency (16X)	0		2.0	MHz
	(1X)	0		1.0	MHz
t_{TX}[9]	TxC High or Low time	220			ns
f_{TX}[9]	TxC frequency (16X)	0		2.0	MHz
	(1X)	0		1.0	MHz
Transmitter Timing (Figure 6)					
t_{TXD}[9]	TxD output delay from TxC Low			350	ns
t_{TCS}[9]	Output delay from TxC Low to TxD data output	0		150	ns
Receiver Timing (Figure 7)					
t_{RXS}[9]	RxD data setup time to RxC High	240			ns
t_{RXH}[9]	RxD data hold time from RxC High	200			ns

NOTES:
1. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
2. Parameters are valid over specified temperature range.
3. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of ≤ 20ns. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate.
4. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
5. Test condition for outputs: C_L = 150pF, except interrupt outputs. Test condition for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
6. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. In this case, all timing specifications apply referenced to the falling and rising edges of CEN, CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
7. If CEN is used as the 'strobing' input, the parameter defines the minimum High times between one CEN and the next. The RDN signal must be negated for t_{RWD} to guarantee that any status register changes are valid.
8. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.
9. This parameter is not applicable to the 28-pin device.
10. Operation to 0MHz is assured by design. However, operation at low frequencies is not tested and has not been characterized.

BLOCK DIAGRAM



BLOCK DIAGRAM

The SCN2681 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the block diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer.

Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register

(IMR) and the Interrupt Status Register (ISR). The IMR may be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions.

Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

If an external clock is used instead of a crystal, both X1 and X2 should use a configuration similar to the one in Figure 5.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4k baud. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the SCN2681 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

The input port pulse detection circuitry uses a 38.4kHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (this assumes that the clock input is 3.6864MHz). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs "coincident with the first sample pulse". The 50µs time refers to the situation in which the change-of-state is "just missed" and the first change-of-state is not detected until 25µs later.

Input Port

The inputs to this unlatched 7-bit port can be read by the CPU by performing a read operation at address D16. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always read as a logic 1. The pins of this port can also serve as auxiliary inputs to certain portions fo the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs lasting longer than 25 – 50µs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

Output Port

The output port pins may be controlled by the OPR, OPCR, MR and CR registers. Via appropriate programming they may be just another parallel port to external circuits, or they may represent many internal conditions of the UART. When this 8-bit port is used as a general purpose output port, the output port pins drive a state which is the complement of the Output Port Register (OPR). OPR(n) = 1 results in OP(n) = Low and vice versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address E16 with the accompanying data specifying the bits to be set (1 = set, 0 = no change).

Likewise, a bit is reset by a write at address F16 with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also individually assigned specific functions by appropriate programming of the Channel A mode registers (MR1A, MR2A), the Channel B mode registers (MR1B, MR2B), and the Output Port Configuration Register (OPCR).

TRANSMITTER OPERATION

The SCN2681 is conditioned to transmit data when the transmitter is enabled through the command register. The SCN2681 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When a character is loaded into the Transmit Holding Register (THR), the above conditions are negated. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again which means one full character time of buffering is provided. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR.

If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enable, the CTSN input must be Low in order for the character to be transmitted. If it goes High in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes Low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

Receiver

The SCN2681 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7 1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive Holding Register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than eight bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, overrun error and received break state (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one-half bit time before a search for the next start bit begins.

Receiver FIFO

The RHR consists of a First-In-First-Out (FIFO) stack with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4] will be set-upon receipt of the start bit of the new (overrunning) character).

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

Receiver Reset and Disable

Receiver disable stops the receiver immediately – data being assembled if the receiver shift register is lost. Data and status in the FIFO is preserved and may be read. A re-enable of the receiver after a disable will cause the receiver to begin assembling characters at the next start bit detected. A receiver reset will discard the present shift register date, reset the receiver ready bit (RxRDY), clear the status of the byte at the top of the FIFO and re-align the FIFO read/write pointers. This has the appearance of "clearing or flushing" the receiver FIFO. In fact, the FIFO is NEVER cleared! The data in the FIFO remains valid until overwritten by another received character. Because of this erroneous reading, the FIFO will miss-align the FIFO pointers and result in the reading of previously read data. A receiver reset will re-align the pointers.

Multidrop Mode

The DUART is equipped with a wake up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wake up' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the

Table 1. SCN2681 Register Addressing

A3	A2	A1	A0	READ (RDN = 0)	WRITE (WRN = 0)
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	BRG Test *	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
0	1	0	0	Input Port Change Register (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Register (CRUR)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	1X/16X Test	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
1	1	0	0	*Reserved*	*Reserved*
1	1	0	1	Input Port	Output Port Conf. Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

* See Table 5 for BRG Test frequencies.

received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems.

For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1x by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1x, switches the pointer to MR2x. The pointer then remains at MR2x, so that subsequent accesses are always to MR2x unless the pointer is reset to MR1x as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'OA' should never be read during normal operation since they are reserved for internal diagnostics.

MR1A – Channel A Mode Register 1

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7] – Channel A Receiver Request-to-Send Control
This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the Channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1A[6] – Channel A Receiver Interrupt Select
This bit selects either the Channel A receiver ready status (RxRDY) or the Channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

MR1A[5] – Channel A Error Mode Select
This bit select the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block" mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

MR1A[4:3l – Channel A Parity Mode Select
If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] + 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] – Channel A Parity Type Select
This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] – Channel A Bits Per Character Select
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

Table 2. Register Bit Formats

	BIT 7	BIT 6	BIT 5	BIT 4 BIT 3	BIT 2	BIT 1 BIT 0
	RxRTS CONTROL	**RxINT SELECT**	**ERROR MODE**	**PARITY MODE**	**PARITY TYPE**	**BITS PER CHARACTER**
MR1A MR1B	0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multidrop Mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

	BIT 7 BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	CHANNEL MODE	**TxRTS CONTROL**	**CTS ENABLE Tx**	**STOP BIT LENGTH***			
MR2A MR2B	00 = Normal 01 = Auto-Echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

NOTE:
*Add 0.5 to values shown for 0 – 7 if channel is programmed for 5 bits/char.

	BIT 7 BIT 6 BIT 5 BIT 4	BIT 3 BIT 2 BIT 1 BIT 0
CSRA CSRB	**RECEIVER CLOCK SELECT**	**TRANSMITTER CLOCK SELECT**
	See Text	See Text

	BIT 7	BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		MISCELLANEOUS COMMANDS	**DISABLE Tx**	**ENABLE Tx**	**DISABLE Rx**	**ENABLE Rx**
CRA CRB	Not used – should be 0	See Text	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
*Access to the upper four bits of the command register should be separated by three (3) edges of the X1 clock. A disabled transmitter cannot be loaded.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	RECEIVED BREAK*	**FRAMING ERROR***	**PARITY ERROR***	**OVERRUN ERROR**	**TxEMT**	**TxRDY**	**FFULL**	**RxRDY**
SRA SRB	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
* These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3 BIT 2	BIT 1 BIT 0
	OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**
OPCR	0 = OPR[7] 1 = TxRDYB	0 = OPR[6] 1 = TxRDYA	0 = OPR[5] 1 = RxRDY/ FFULLB	0 = OPR[4] 1 = RxRDY/ FFULLA	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1x) 11 = RxCB(1x)	00 = OPR[2] 01 = TxCA(16x) 10 = TxCA(1x) 11 = RxCA(1x)

	BIT 7	BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	BRG SET SELECT	**COUNTER/TIMER MODE AND SOURCE**	**DELTA IP 3 INT**	**DELTA IP 2 INT**	**DELTA IP 1 INT**	**DELTA IP 0 INT**
ACR	0 = set 1 1 = set 2	See Table 4	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IPCR	DELTA IP 3	DELTA IP 2	DELTA IP 1	DELTA IP 0	IP 3	IP 2	IP 1	IP 0
	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ISR	INPUT PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	COUNTER READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA
	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IMR	IN. PORT CHANGE INT	DELTA BREAK B INT	RxRDY/ FFULLB INT	TxRDYB INT	COUNTER READY INT	DELTA BREAK A INT	RxRDY/ FFULLA INT	TxRDYA INT
	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CTUR	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CTLR	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]

MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] – Channel A Mode Select

Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically re-transmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is re-clocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is re-clocked and re-transmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the

device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the deselection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been retransmitted.

MR2A[5] – Channel A Transmitter Request-to-Send Control
CAUTION: When the transmitter controls the OP pin (usually used for the RTSN signal) the meaning of the pin is not RTSN at all! Rather, it signals that the transmitter has finished the transmission (i.e., end of block).

This bit allows deactivation of the RTSN output by the transmitter. This output is manually asserted and negated by the appropriate commands issued via the command register. MR2[5] set to 1 caused the RTSN to be reset automatically one bit time after the character(s) in the transmit shift register and in the THR (if any) are completely transmitted (including the programmed number of stop bits) if a previously issued transmitter disable is pending. This feature can be used to automatically terminate the transmission as follows:

1. Program the auto-reset mode: MR2[5]=1
2. Enable transmitter, if not already enabled
3. Assert RTSN via command
4. Send message
5. After the last character of the message is loaded to the THR, disable the transmitter. (If the transmitter is underrun, a special case exists. See note below.)
6. The last character will be transmitted and the RTSN will be reset one bit time after the last stop bit is sent.

NOTE: The transmitter is in an underrun condition when both the TxRDY and the TxEMT bits are set. This condition also exists immediately after the transmitter is enabled from the disabled or reset state. When using the above procedure with the transmitter in the underrun condition, the issuing of the transmitter disable must be delayed from the loading of a single, or last, character until the TxRDY becomes active again after the character is loaded.

MR2A[4] – Channel A Clear-to-Send Control
If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IPO) each time it is ready to send a character. If IPO is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes Low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character..

MR2A[3:0] – Channel A Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of .563 TO 1 AND .563 to 2 bits. In increments of 0.625 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1.0625 to 2 stop bits can be programmed in increments of .0625 bit.

The receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit is enabled) in all cases.

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode registers 1 and 2 are identical to the bit definitions for MRA and MR2A except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

CSRA – Channel A Clock Select Register

CSRA[7:4] – Channel A Receiver Clock Select
This field selects the baud rate clock for the Channel A receiver as follows:

CSRA[7:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
0000	50	75
0001	110	110
0010	134.5	134.5
0011	200	150
0100	300	300
0101	600	600
0110	1,200	1,200
0111	1,050	2,000
1000	2,400	2,400
1001	4,800	4,800
1010	7,200	1,800
1011	9,600	9,600
1100	38.4k	19.2k
1101	Timer	Timer
1110	IP4–16X	IP4–16X
1111	IP4–1X	IP4–1X

(See also Table 5)

The receiver clock is always a 16X clock except for CSRA[7] = 1111.

CSRA[3:0] – Channel A Transmitter Clock Select
This field selects the baud rate clock for the Channel A transmitter. The field definition is as per CSR[7:4] except as follows:

CSRA[3:0]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP3–16X	IP3–16X
1111	IP3–1X	IP3–1X

The transmitter clock is always a 16X clock except for CSR[3:0] = 1111.

CSRB – Channel B Clock Select Register

CSRB[7:4] – Channel B Receiver Clock Select
This field selects the baud rate clock for the Channel B receiver. The field definition is as per CSRA[7:4] except as follows:

CSRB[7:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP6–16X	IP6–16X
1111	IP6–1X	IP6–1X

The receiver clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0] – Channel B Transmitter Clock Select
This field selects the baud rate clock for the Channel B transmitter. The field definition is as per CSRA[7:4] except as follows:

CSRB[3:0]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP5–16X	IP5–16X
1111	IP5–1X	IP5–1X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

CRA[7] – Not Used
Should be set to zero for upward compatibility with newer parts.

CRA[6:4] – Channel A Miscellaneous Command
The encoded value of this field may be used to specify a single command as follows:

CRA[6:4] – COMMAND

000 No command.

001 Reset MR pointer. Causes the Channel A MR pointer to point to MR1.

010 Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.

011 Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.

100 Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.

101 Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.

110 Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.

111 Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.

CRA[3] – Disable Channel A Transmitter
This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state. A disable transmitter cannot be loaded.

CRA[2] – Enable Channel A Transmitter
Enables operation of the Channel A transmitter. The TxRDY status bit will be asserted.

CRA[1] – Disable Channel A Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] – Enable Channel A Receiver
Enables operation of the Channel A receiver. If not in the special wake up mode, this also forces the receiver into the search for start-bit state.

CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

SRA – Channel A Status Register

SRA[7] – Channel A Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line to the marking state for at least one-half a bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

SRA[6] – Channel A Framing Error
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first bit position.

SRA[5] – Channel A Parity Error
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multidrop mode the parity error bit stores the receive A/D bit.

SRA[4] – Channel A Overrun Error
This bit, when set indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a 'reset error status' command.

SRA[3] – Channel A Transmitter Empty (TxEMTA)
This bit will be set when the transmitter underruns, i.e., both the TxEMT and TxRDY bits are set. This bit and TxRDY are set when the transmitter is first enabled and at any time it is re-enabled after either (a) reset, or (b) the transmitter has assumed the disabled state. It is always set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission.

It is reset when the THR is loaded by the CPU, a pending transmitter disable is executed, the transmitter is reset, or the transmitter is disabled while in the underrun condition.

SRA[2] – Channel A Transmitter Ready (TxRDYA)
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled or reset, and is set when the transmitter is first enabled, viz., characters loaded into the THR while the transmitter is disabled will not be transmitted.

SRA[1] – Channel A FIFO Full (FFULLA)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SRA[0] – Channel A Receiver Ready (RxRDYA)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift to the FIFO and reset when the CPU reads the RHR, if after this read there are not more characters still in the FIFO.

SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR – Output Port Configuration Register

OPCR[7] – OP7 Output Select
This bit programs the OP7 output to provide one of the following:
- The complement of OPR[7].
- The Channel B transmitter interrupt output which is the complement of TxRDYB. When in this mode OP7 acts as an Open- Collector output. Note that this output is not masked by the contents of the IMR.

OPCR[6] – OP6 Output Select
This bit programs the OP6 output to provide one of the following:
- The complement of OPR[6].
- The Channel A transmitter interrupt output which is the complement of TxRDYA. When in this mode OP6 acts as an Open-Collector output. Note that this output is not masked by the contents of the IMR.

OPCR[5] – OP5 Output Select
This bit programs the OP5 output to provide one of the following:
- The complement of OPR[5].
- The Channel B transmitter interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an Open-Collector output. Note that this output is not masked by the contents of the IMR.

OPCR[4] – OP4 Output Select
This field programs the OP4 output to provide one of the following:
- The complement of OPR[4].
- The Channel B transmitter interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an Open-Collector output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] – OP3 Output Select
This bit programs the OP3 output to provide one of the following:
- The complement of OPR[3].
- The counter/timer output, in which case OP3 acts as an Open-Collector output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
- The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] – OP2 Output Select
This field programs the OP2 output to provide one of the following:
- The complement of OPR[2].
- The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
- The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates to be generated by the BRG:

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.
Set 2: 75, 110, 134.5, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, and 19.2k baud.

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 3.

ACR[6:4] – Counter/Timer Mode And Clock Source Select
This field selects the operating mode of the counter/timer and its clock source as shown in Table 4.

ACR[3:0] – IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – IP3, IP2, IP1, IP0 Change-of-State
These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – IP3, IP2, IP1, IP0 Current State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to 00_{16} when the DUART is reset.

ISR[7] – Input Port Change Status
This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] – Channel B Change In Break
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

ISR[5] – Channel B Receiver Ready or FIFO Full
The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in Channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel B FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[4] – Channel B Transmitter Ready
This bit is a duplicate of TxRDYB (SRB[2]).

ISR[3] – Counter Ready.
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] – Channel A Change in Break
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

ISR[1] – Channel A Receiver Ready Or FIFO Full
The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in Channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU read the RHR. IF after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel A FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the ISR[0] and IMR waiting character is loaded into the FIFO.

ISR[0] – Channel A Transmitter Ready
This bit is a duplicate of TxRDYA (SRA[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3–OP7 or the reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is 0002_{16}. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the CT generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR.

If the value in CTUR and CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. In this

mode the C/T runs continuously. Receipt of a start counter command (read with A3-A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR. The waveform so generated is often used for a data clock. The formula for calculating the divisor n to load to the CTUR and CTLR for a particular 1X data clock is shown below:

$$n = \frac{C/T\ Clock\ Frequency}{2 \cdot 16 \cdot Baud\ rate\ desired}$$

Often this division will result in a non-integer number; 26.3, for example. One can only program integer numbers in a digital divider. Therefore, 26 would be chosen. This gives a baud rate error of 0.3/26.3 which is 1.14%; well within the ability asynchronous mode of operation.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3-A0 = 1111). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

On power up and after reset, the timer/counter runs in timer mode and can only be restarted. Because it cannot be shut off or stopped, and runs continuously in timer mode, it is recommended that at initialization, the output port (OP3) should be masked off through the OPCR[3:2] = 00 until the T/C is programmed to the desired operational state.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a counter command. Upon reaching terminal count (0000_{16}), the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU.

It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

Table 3. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz

NORMAL RATE (BAUD)	ACTUAL 16x CLOCK (kHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2k	307.2	0
38.4k	614.4	0

NOTE: Duty cycle of 16x clock is 50% ± 1%.

Table 4. ACR 6:4 Field Definition

ACR 6:4	MODE	CLOCK SOURCE
000	Counter	External (IP2)
001	Counter	TxCA – 1x clock of Channel A transmitter
010	Counter	TxCB – 1x clock of Channel B transmitter
011	Counter	Crystal or external clock (x1/CLK) divided by 16
100	Timer	External (IP2)
101	Timer	External (IP2) divided by 16
110	Timer	Crystal or external clock (x1/CLK)
111	Timer	Crystal or external clock (x1/CLK) divided by 16

NOTE: Timer mode generates a squarewave.

TIMING DIAGRAMS

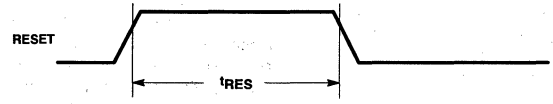


Figure 1. Reset Timing

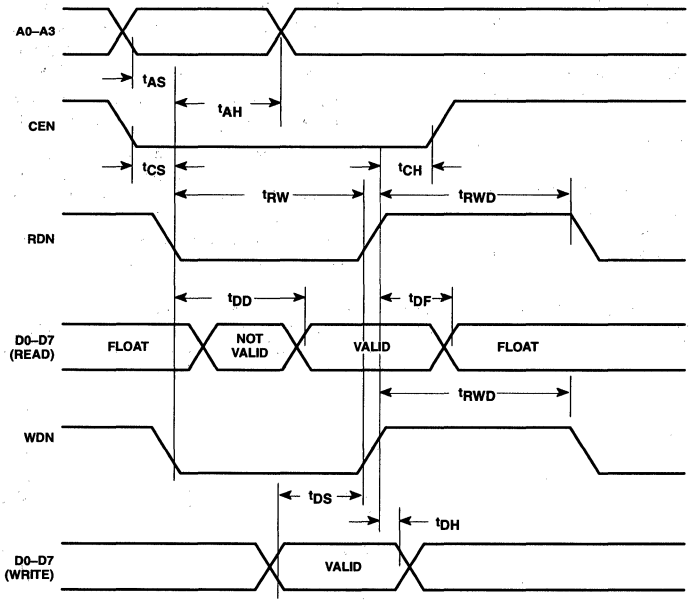


Figure 2. Bus Timing

TIMING DIAGRAMS (Continued)

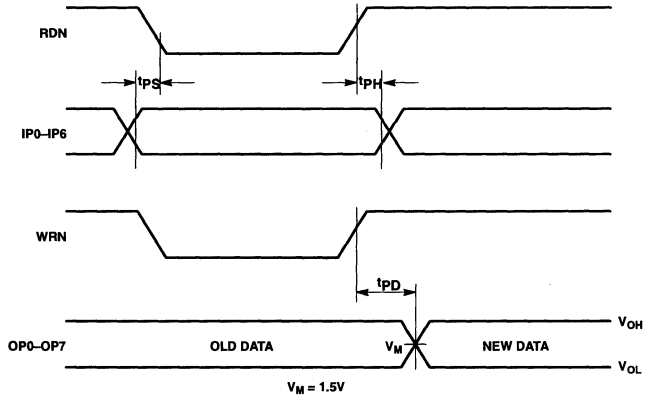
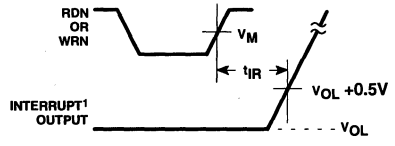


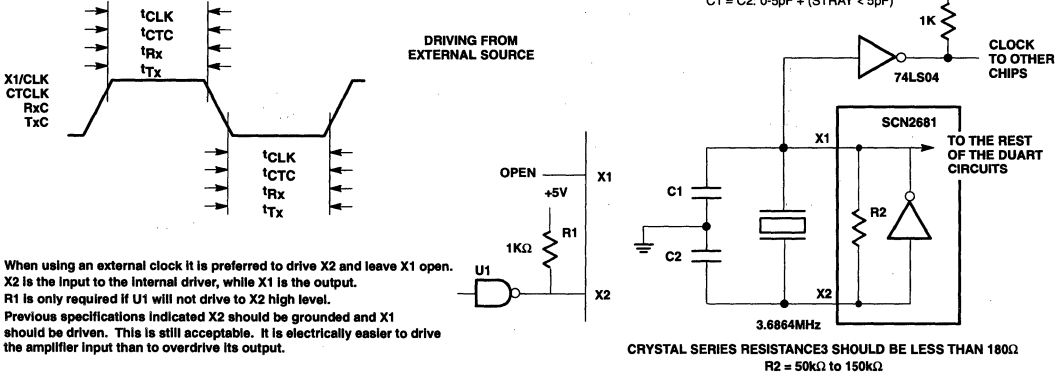
Figure 3. Port Timing



NOTES:

1. INTRN or OP3 – OP7 when used as interrupt outputs.
2. The test for open-drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from themidpoint of the switching signal, V_M, to a point 0.5V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 4. Interrupt Timing



When using an external clock it is preferred to drive X2 and leave X1 open. X2 is the input to the internal driver, while X1 is the output. R1 is only required if U1 will not drive to X2 high level. Previous specifications indicated X2 should be grounded and X1 should be driven. This is still acceptable. It is electrically easier to drive the amplifier input than to overdrive its output.

CRYSTAL SERIES RESISTANCE3 SHOULD BE LESS THAN 180Ω
R2 = 50kΩ to 150kΩ

Figure 5. Clock Timing

TIMING DIAGRAMS (Continued)

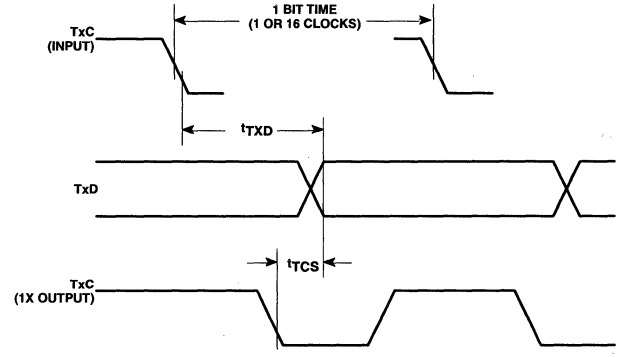


Figure 6. Transmit

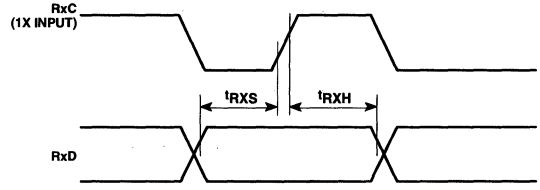
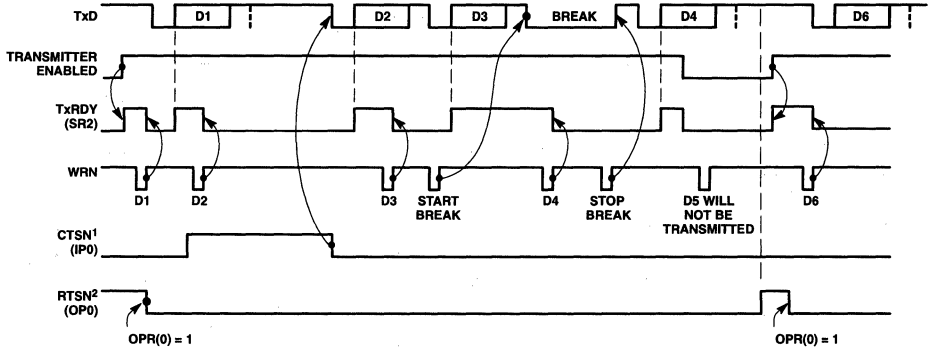


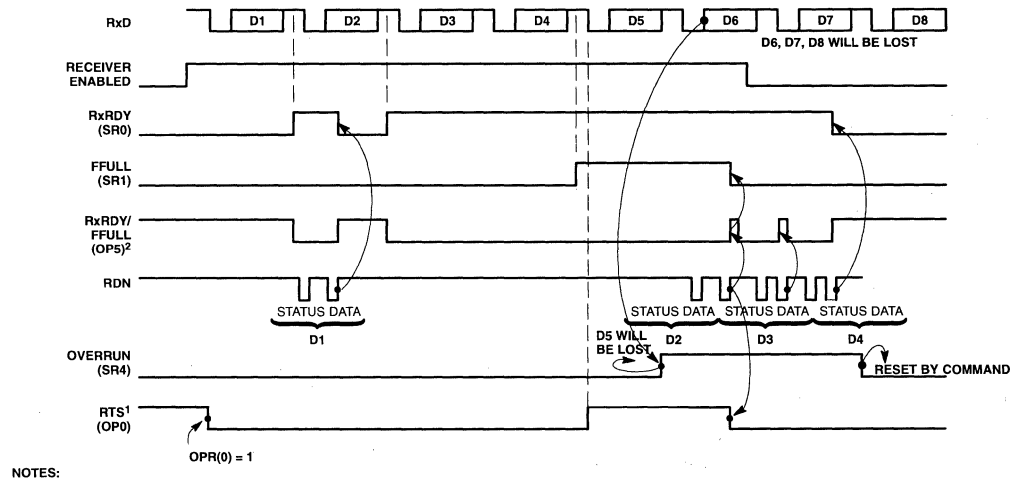
Figure 7. Receive



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 8. Transmitter Timing

TIMING DIAGRAMS (Continued)



NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) = 1 and MR(6) = 0.

Figure 9. Receiver Timing

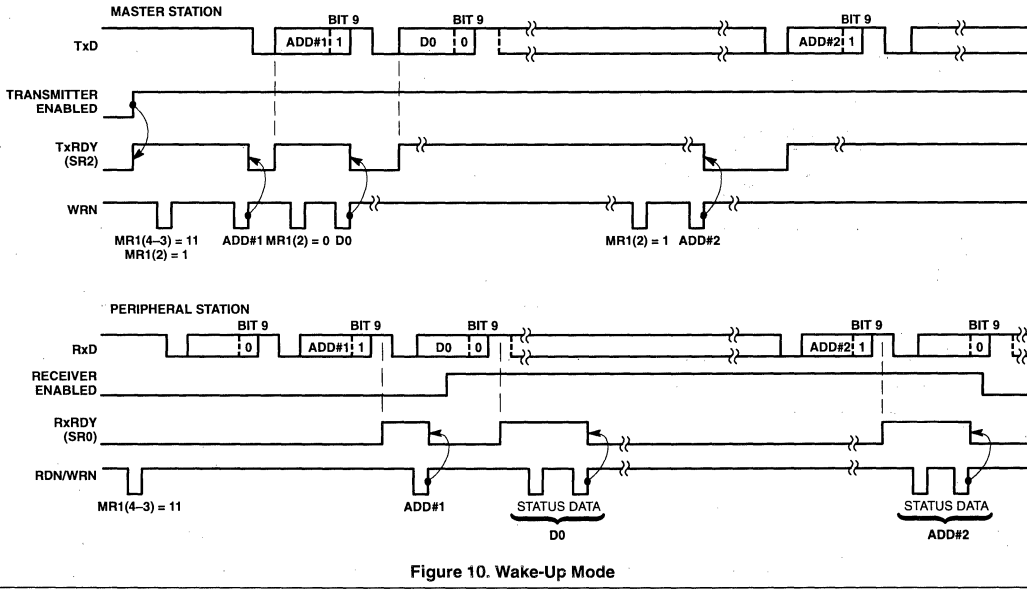


Figure 10. Wake-Up Mode

Output Port Notes

The output ports are controlled from three places: the OPCR register, the OPR register, and the MR registers. The OPCR register controls the source of the data for the output ports OP2 through OP7. The data source for output ports OP0 and OP1 is controlled by the MR and CR registers. When the OPR is the source of the data for the output ports, the data at the ports is inverted from that in the OPR register. The content of the OPR register is controlled by the "Set Output Port Bits Command" and the "Reset Output Bits Command". These commands are at E and F,

respectively. When these commands are used, action takes place only at the bit locations where ones exist. For example, a one in bit location 5 of the data word used with the "Set Output Port Bits" command will result in OPR5 being set to one. The OP5 would then be set to zero (V_{SS}). Similarly, a one in bit position 5 of the data word associated with the "Reset Output Ports Bits" command would set OPR5 to zero and, hence, the pin OP5 to a one (V_{DD}).

The CTS, RTS, CTS Enable Tx signals

CTS (Clear To Send) is usually meant to be a signal to the transmitter meaning that it may transmit data to the receiver. The CTS input is on pin IP0 for TxA and on IP1 for TxB. The CTS signal is active low; thus, it is called CTSAN for TxA and CTSBN for TxB.

RTS is usually meant to be a signal from the receiver indicating that the receiver is ready to receive data. It is also active low and is, thus, called RTSAN for RxA and RTSBN for RxB. RTSAN is on pin op0 and RTSBN is on OP1. A receiver's RTS output will usually be connected to the CTS input of the associated transmitter. Therefore, one could say that RTS and CTS are different ends of the same wire!

MR2(4) is the bit that allows the transmitter to be controlled by the CTS pin (IP0 or IP1). When this bit is set to one AND the CTS input is driven high, the transmitter will stop sending data at the end of the present character being serialized. It is usually the RTS output of the receiver that will be connected to the transmitter's CTS input. The receiver will set RTS high when the receiver FIFO is full AND the start bit of the fourth character is sensed. Transmission then stops with four valid characters in the receiver. When MR2(4) is set to one, CTSN must be at zero for the transmitter to operate. If MR2(4) is set to zero, the IP pin will have no effect on the operation of the transmitter.

MR1(7) is the bit that allows the receiver to control OP0. When OP0 (or OP1) is controlled by the receiver, the meaning of that pin will be RTS. However, a point of confusion arises in that OP0 (or OP1) may also be controlled by the transmitter. When the transmitter is controlling this pin, its meaning is not RTS at all. It is, rather, that the transmitter has finished sending its last data byte. Programming the OP0 or OP1 pin to be controlled by the receiver and the transmitter at the same time is allowed, but would usually be incompatible.

RTS is expressed at the OP0 or OP1 pin which is still an output port. Therefore, the state of OP0 or OP1 should be set low for the receiver to generate the proper RTS signal. The logic at the output is basically a NAND of the OPR register and the RTS signal as generated by the receiver. When the RTS flow control is selected via the MR(7) bit state of the OPR register is not changed. Terminating the use of "Flow Control" (via the MR registers) will return the OP0 or OP1 pins to the control of the OPR register.

Transmitter Disable Note

The sequence of instructions enable transmitter — load transmit holding register — disable transmitter will result in nothing being sent if the time between the end of loading the transmit holding register and the disable command is less that 3/16 bit time in the 16x mode or one bit time in the 1x mode. Also, if the transmitter, while in the enabled state and underrun condition, is immediately disabled after a single character is loaded to the transmit holding register, that character will not be sent.

In general, when it is desired to disable the transmitter before the last character is sent AND the TxEMT bit is set in the status register (TxEMT is always set if the transmitter has underrun or has just been enabled), be sure the TxRDY bit is active immediately before issuing the transmitter disable instruction. TxRDY sets at the end of the "start bit" time. It is during the start bit that the data in the transmit holding register is transferred to the transmit shift register.

Non-standard baud rates are available as shown in Table [5] below, via the BRG Test function.

Table 5. Baud Rates Extended

	Normal BRG		BRG Test	
CSR[7:4]	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0000	50	75	4,800	7,200
0001	110	110	880	880
0010	134.5	134.5	1,076	1,076
0011	200	150	19.2K	14.4K
0100	300	300	28.8K	28.8K
0101	600	600	57.6K	57.6K
0110	1,200	1,200	115.2K	115.2K
0111	1,050	2,000	1,050	2,000
1000	2,400	2,400	57.6K	57.6K
1001	4,800	4,800	4,800	4,800
1010	7,200	1,800	57.6K	14.4K
1011	9,600	9,600	9,600	9,600
1100	38.4K	19.2K	38.4K	19.2K
1101	Timer	Timer	Timer	Timer
1110	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X
1111	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X

NOTE: Each read on address H'2' will toggle the baud rate test mode. When in the BRG test mode, the baud rates change as shown to the left. This change affects all receivers and transmitters on the DUART. Also, the RTSN outputs (OP[0] and OP[1]) become the transmitter 1x clock.

The test mode at address H'A' changes all transmitters and receivers to the 1x mode and connects the output ports to some internal nodes.

A condition that occurs infrequently has been observed where the receiver will ignore all data. It is caused by a corruption of the start bit generally due to noise. When this occurs the receiver will appear to be asleep or locked up. The receiver must be reset for the UART to continue to function properly.

Reset in the Normal Mode (Receiver Enabled)

Recovery can be accomplished easily by issuing a receiver software reset followed by a receiver enable. All receiver data, status and programming will be preserved and available before reset. The reset will NOT affect the programming.

Reset in the Wake-Up Mode (MR1[4:3] = 11)

Recovery can also be accomplished easily by first exiting the wake-up mode (MR1[4:3] = 00 or 01 or 10), then issuing a receiver software reset followed by a wake-up re-entry (MR1[4:3] = 11). All receiver data, status and programming will be preserved and available before reset. The reset will NOT affect the programming.

The receiver has a digital filter designed to reject "noisy" data and the receiver state machine was designed to reject noisy start bits or noise that might be considered a start bit. In spite of these precautions, corruption of the start bit can occur in 15ns window approximately 100ns prior to the rising edge of the data clock. The probability of this occurring is less than 10^{-5} at 9600 baud.

A corrupted start bit may have some deleterious effects in ASYNC operation if it occurs within a normal data block. The receiver will tend to align its data clock to the next '0' bit in the data stream, thus potentially corrupting the remainder of the data block. A good design practice, in environments where start bit corruption is possible, is to monitor data quality (framing error, parity error, break change and received break) and "data stopped" time out periods. Time out periods can be enabled using the counter/timer in the SCC2691, SCC2692, SCC2698B and SC68692 products. This monitoring can indicate a potential start bit corruption problem.

SCN2681/SCN68681 and SCC2691 data communications AN405

INTRODUCTION

This SCN2681/SCN68681 and SCC2691 data communications applications note contains answers to some of the most frequently discussed user inquiries. There are three main sections: functions that are common to all three; functions that are unique to the SCN2681/SCN68681; and a typical SCC2691 application using the musical instrument digital interface (MIDI).

DUART/UART COMMON FUNCTIONS

Reading Reserved Register

Performing a bus read operation at location 02H or 0AH will force these devices into a diagnostic operation. This diagnostic mode is used to test the baud rate generator circuitry. When a read operation occurs on either address, the device will output clock pulses on the general purpose outputs that are a multiple of the frequencies in the baud rate table.

This mode may be entered accidentally, in some cases, by a monitor program that uses a write followed by an automatic read/verify cycle. For example, a write to CRA or CRB with this type of monitor will invoke the reserved test mode. Care must be taken when a development system is used in the manual mode, since most development systems use a write followed by a read/verify cycle. Mostly, this anomaly can occur in the SC68681. If the rising edge of the write pulse occurs before the rising edge of CEN, the reserved mode is invoked (even if R/WN rising is only 10 to 20ns early). Users of the SCN68681 must be sure that the rising edge of R/WN rises with or after the rising edge of CEN.

Receiver FIFO

All three devices have a three-deep receive FIFO. The FIFO acts more like a circular queue than a FIFO. The FIFO acts more like a circular queue than a FIFO. The receiver has both a head and tail pointer. The head pointer is controlled by a bus read operation and is bumped to the next location whenever a read of the receiver takes place. The tail pointer is bumped whenever a character is assembled in the receive shift register and transferred to the receive holding register.

After an external reset is applied or a reset receiver command is issued, the head and tail pointers are at the same location in the FIFO. Although the data sheet specifies the receiver is flushed when a reset receiver command is issued, nothing is done to the contents of the receiver. Therefore, three consecutive reads of the the receiver will move the head pointer around in a circle until it comes back to the starting point. If no new data has been received in the receive shift register, the old data will still be in the FIFO.

Care must be taken when using a monitor in the manual mode, since the receiver head pointer can be bumped by a write to the transmit holding register (THR). (Write followed by a read/verify operation at the same address has already been discussed. See Reading Reserved Registers.)

The best way to determine if the receiver should be read is to poll the RxRDY bit in either the ISR or the SR registers. If RxRDY = 1, read the receiver again. Continue this loop until RxRDY = 0. Once this state is reached, stop reading the receiver, or the pointers will be bumped beyond the current valid data.

Detecting the End of Break

Detecting a break is a simple function built into all three devices. The receiver continuously samples RxD. If a low is sensed for the start bit and the full number of programmed bit times, a zero character is accumulated in the receive FIFO. If no stop bit is sensed (a mark condition, then the receiver samples beyond the character frame for one more bit time. If a low is sensed, a framing error has been detected. Once the framing error bit is set in the status register and a zero is accumulated in the receive FIFO, the resulting condition forces the received break bit to set in the ISR and in the SRA or SRB. In this manner, a start of break is detected.

In order to detect an end of break, the delta break bits in the ISR register must be tested. Whether the CPU is polling the ISR or if the CPU is interrupt driven, the zero character in the receive FIFO should not be read nor should the receive break be cleared in SRA or SRB until the break is completely over. To detect an end of break, the CPU should issue a reset delta break command (50H to CRA or CRB), which will reset the delta break bit in the ISR. If the CPU is using interrupts, the next step is to mask on the delta break interrupt. If the CPU is polling, it should continue polling until the delta break sets. Delta break will be set and interrupt only when a change of state occurs on RxD. When the rising edge of RxD occurs and the break is over, the delta break bit can be cleared (50H to CRA or CRB), the received break and framing error can be cleared (40H to CRA or CRB), and the zero character can be read from the receiver and discarded.

Disabling the Transmitter After a Short Frame

The data sheet states that the transmitter may be disabled after the last character is loaded in the transmit shift register. This is used to end a block transmission or to negate RTS, after the last character is shifted out of the transmit shift register. This method of disabling the transmitter is essential if the RTS handshake lines are to be used. It is not a good method to use when short, one or two byte frames are to be transmitted as a response to a primary or secondary station. The problem occurs when the transmitter is re-enabled to send another short frame response. If the last character of a message is still being serialized when an enable transmitter command is executed, the serialized character will either be garbled or lost.

For example, assume that the last character of a two byte frame was loaded into the THR. If the transmitter is running at 9600 baud, it will take from 1 to 2ms before the last character is completely shifted out on TxD (the 2ms time occurs when the first character in the two byte frame is currently in the TSR). If the CPU needs to send another response, it will start by enabling the transmitter and loading the first byte of the next frame. Even if the second byte of the last frame is now in the TSR, the transmitter must go to mark due to the re-enable command and the last character is either lost or garbled.

The best way to avoid this problem is to wait until the last character is completely shifted out of the TSR before disabling the transmitter. This can be verified by polling the TxEMPT bit until it is set in SRA or SRB. As pointed out earlier, this will not work when using RTS, since the RTS output will only toggle if the transmitter is disabled while the last data character is in the THR. In that case, the user can time out a delay before re-enabling the transmitter.

Disabling the Transmitter and/or Receiver on the Fly

Problems have been encountered when trying to write to the mode registers (MR2, MR1), or the clock select registers (CSRA/B), or to ACR[7] without first disabling the transmitter and receiver. If the mode register changes while character serialization is still active, the transmission may start over under the new mode configurations. If the mode register changes after serialization is complete and the transmitter is empty, two potential problems can appear: TxD may

go to the space condition for a short period of time, or TxRDY in the ISR will set and then reset. These results are obtained independent of the data written to the mode registers. Programming the registers to the current values can still product the above results.

The problem is more serious when writing to CSRA/B or ACR[7], when the clock is still running. If the transmit and/or receive clocks are changed without disabling the transmitter and receiver, a clipped or shortened clock may appear during the change from one frequency to another. These short clock pulses can lock up the transmitter and/or receiver, until they are re-enabled by command to CRA or CRB.

The best way to avoid these problems is to disable the transmitter and receiver, before changing either the mode or CSR registers or ACR[7]. Disabling the transmitter and receiver will stop the TXC and RXC while the changes are made. When the changes are complete, the transmitter and receiver should be reset and then re-enabled by software command. A reset command insures that everything is in a known state before the changes are initiated.

Setting Up the Counter/Timer as a Timer

The maximum frequency that can be generated by the C/T (counter/timer) is dependent on whether the 1X or 16X clock source mode is used. If the C/T is to be used to drive the receiver directly, a 16X clock must be generated that will sample the incoming data stream.

As an example, let the X1/CLK input = 4MHz and set the C/T to its minimum value (CTUR/CTLR = 0002H). Since the C/T will count down to zero before its output changes state, two full counts must pass before the C/T output changes back to its original state. Therefore, the maximum frequency output will be 4MHz divided by 4 (minimum count) divided by 16 (for sampling clock). This results in a 62.5kHz baud rate.

If a higher C/T clock rate is required, the 1X mode must be programmed. The highest C/T output is 1MHz (4MHz divided by 4). The C/T can be programmed to output 1MHz on OP3, which can be tied by wire to IP3/4 or IP5/6. These inputs can be selected to be transmit and receive 1X clock inputs. To program this type of function, write OPCR = 04H, ACR = 60H, CTUR/CTLR = 0002H, and CSRA/B =FFH. Start the C/T by performing a read at address 0EH (start counter command). When in the timer mode, the C/T will not stop oscillating until ACR[6:4] is written to the counter mode followed by a stop time command (read at address 0FH).

The counter can be used to count external events, or used as a system delay timer. As an example, the C/T can be set up to time out a 2ms delay and interrupt the CPU (used to refresh dynamic RAM). Using the X1/CLK at 4MHz as the C/T clock, the total time in counts is (2ms) / (250ns times 16) = 500 or 01F4H (times 16 is used since X1/CLK divided by 16 is the only internal clock source available in the counter mode). This function would be implemented by writing ACR = 30H, CTUR/CTLR = 01F4H, and IMR = 04H. The counter must be stopped and started by command from the CPU for each count down (stop = read at address 0FH, start = read at address 0EH).

Multidrop/Wake-Up Mode

If MR1[4:3], the devices are in the multidrop or wake-up (SCC2691) mode. This will cause the transmitter to send data with the last bit of each character identified as the address/data (A/D) bit. If MR1[2] = 0, the A/D bit will be '1' and the assembled character will be interpreted by the secondary receiver as an address. Both primary and secondary stations must be in the multidrop mode. In order to transmit an address character followed by data characters, a write must be performed to MR1. Writing of the mode registers may cause garbled data, if the transmitter and receiver are not disabled. The following sequence should be used when writing to the mode registers:

1. To insure that the transmitter is in a quiescent state, do not write to MR1 until TxEMT = 1.
2. Reset the MR pointers. Disable the transmitter and the receiver.
3. Write MR1 using the previously written data, with MR1[2] = 1 (Tx address). Reset and enable the transmitter and receiver.
4. Load the address character in the transmit holding register (THR). The A/D bit will be appended to the character during transmission according to the polarity of MR1[2].
5. Wait until TxEMT = 1. (Wait for transmitter empty).
6. Reset the MR pointers. Disable the transmitter, and the receiver.
7. Write MR1 using previous data with MR1[2] = 0 (Tx data). Reset and enable the transmitter and receiver.
8. Load the first data character into the THR. Continue sending data until the message is done. To send a message to a different address, repeat steps 1 through 8.

When the secondary station sets RxRDY = 1, the CPU must immediately read the receiver to determine if the address is correct. If the received address compares, the CPU must set RxEN = 1 in CRA or CRB so the message can be received. At higher baud rates (19.2k and 38.4k), some users have lost the first character of the message. This is due to the amount of time required for the CPU to read the address out of the receiver and finish a compare operation before enabling the receiver. If this is a problem, the CPU can enable the receiver (RxEN = 1) as soon as the address is received and the CPU is initially interrupted. Later, after the compare operation is finished, the CPU can either read the data from the receiver or reset the receiver depending on the received address (see Figure 1 for a software example).

Handling Interrupts

When the transmitter is enabled and TxRDY is masked on in the IMR, and interrupt will occur immediately. If no messages are to be sent, the user should mask TxRDY off (IMR[4:0] = 0), or no other interrupts will be generated. Only the interrupting section of the device can reset the current interrupt.

For example, loading the transmitter resets TxRDY, reading the receiver resets RxRDY, stopping the counter resets counter ready, etc. If the function is not fully serviced, all other pending interrupts are held up. To avoid this problem only enable the IMR bits that will be immediately in use. Enable and disable TxRDY in the IMR just prior to and at the end of a block transmission.

Driving X1 Externally or Using a Crystal

If a user wants to use an external clock instead of a crystal, the best way is to drive X1 and ground X2 (SCN2681/68681 only). The data sheets show two inverters used to drive X1 out of phase with X2. While this is acceptable, it sacrifices the use of one gate. The only drawback to driving the clock inputs from an external source is that a minimum high voltage of 4.0 volts is required. A V_{OH} greater than 4.0 volts can be insured by use of an open collector buffer (with resistor), or by adding a pull-up resistor to an ordinary TTL buffer (be sure V_{OL} is less than 0.8 volts). Another requirement is the minimum high and low clock pulse width must be 100ns. This parameter can best be met with an external oscillator that has 50% duty cycle.

Another more subtle problem has been seen using a crystal on the X1/X2 inputs. If capacitors C1 and C2 with values of 15pF or greater are used, power-on problems may be experienced

intermittently. The crystal may not oscillate due to an insufficient charge on the capacitors. It is recommended that C1 and C2 be around 5pF to insure proper charging during the power on cycle. Many DUARTs show a 60/40 duty cycle when the crystal is installed between X1 and X2. When viewed with an oscilloscope on X1, the typical high time is 90ns, while the low time is approximately 130ns. To force the crystal to operate at a 50% duty cycle (with clock high and low time approximately 110ns), a 100kΩ or greater resistor should be added from the X1 input to the X2 input. This addition will raise the oscillator's trip point and force the crystal high and low times to be equal.

In the case of the SCC2691, none of the above problems have been experienced with the crystal. The SCC2691 is different when driven from an external source. Any time X1 is driven, X2 must be left open. If X2 is grounded, the clock will not oscillate. Note that the X1 output can only drive one CMOS external buffer. Care must be taken not to overload the X1/CLK input.

X1/X2 Crystal

When ordering the 3.6864MHz crystal, either a series or a parallel crystal can be used as long as the frequency tolerance is close to +.005%. Because of the nature of the X1/X2 circuit, a parallel crystal should be used. Testing has shown that if the tolerance value is low, the error in frequency is divided down to the point where it is negligible. A series crystal can be used if the tolerance is +.005% or less. For crystal samples call: Saronix, located in Palo Alto, CA. Request part no. NMP037: 3.6864MHz HC-18/U. A second crystal source is U.S. Crystal, located in Fort Worth, Texas. Request part number SIG36864-HC18.

General Initialization

Figure 2 describes the typical flow of software initialization. Usually the mode registers are first. If a reset was issued prior to the initialization, there is no need to reset the MR pointers. Note that the transmitter and receiver should be disabled and reset when either the mode registers (MR1A/B and MR2A/B) are loaded.

Asynchronous Diagnostics

Figure 3 is a software function program that can be used to test the integrity of the data bus as well as TxDA, RxDA, TxDB and RxDB. The program starts by initializing channel 'A' and 'B'. Next the MR pointers are reset and MR1A is read back and compared to the value written. If the compare passes, a relay is turned on that shorts TxDA with RxDA and TxDB with RxDB. Since the channels are in the normal mode, this will result in an external loop back. Transmitter 'A' is loaded with 256 characters as the transmitter comes ready. When the receiver interrupts the CPU, the receive FIFO is read and the contents compared with what had been transmitted. If all 256 characters are received correctly, channel 'B' is tested in the same manner. Since the SCC2691 does not have A3 to select channel 'B', the second half of this test is a simple retest of the SCC2691 using different initialization values.

SCN2681/68681 UNIQUE FUNCTIONS

Delta Break Anomaly

When the 'Rev E' parts are powered-on, some have the delta break bits set (ISR[6:2]). This can cause two possible problems: (1) if these bits are masked on in the IMR, they will immediately get a break interrupt; (2) the first characters received into the RHR will be flagged with errors (framing, break or parity) in SRA/B even though the characters were received correctly.

The way to clear these errors is to issue an external hardware reset a second time after the power-up reset, or to issue a clear delta break command to CRA or CRB before enabling the transmitter and receiver. The best method is to first, disable the transmitter and receiver; second, initialize all registers (Mr1, MR2, CSRA/B, ACR, etc.), and then clear all errors through the command registers. To be effective, this must take place at the end of the initialization routine. The ending string of commands to CRA or CRB might look like:

CRX = 50H (clear delta break bit)
CRX = 20H (reset receiver)
CRX = 30H (reset transmitter)
CRX = 45H (clear errors, enable Tx/Rx)

RTS/CTS Functions

When using the RTS/CTS functions, care must be taken to follow the flow chart in the data sheet on how to set up RTS. Although the RTS output will negate automatically, the output must first be asserted by writing a '1' to the appropriate output pin after the transmitter has been enabled, and before the first byte of the message is loaded into the THR. When the receiver controls negation of RTS, a '1' must be written to the appropriate output pin immediately after enabling the receiver.

When the receiver is controlling the negation of RTS, the sending transmitter will be stopped when the FIFO is full and the start bit of a fourth character is detected in the RSR. If the sending transmitter is a Philips Semiconductors part, the transmission will be ended when the character currently in the TSR is finished being shifted out on TxD.

When CTS goes high, the transmitter clock is stopped after the current character is shifted out on TxD. The only problem this causes is that the TxEMPT bit will not set in the SRA or SRB (even if the transmitter is empty), until the clock starts running again (when CTS goes back low).

The receivers are designed to hold three characters in the RHR and one character in the RSR. If the sending transmitter is not a Philips Semiconductors part, the character in the RSR may be overrun by a fifth character. For example, if the sending transmitter is made by Intel, the transmitter will continue to empty both the THR and the TSR when its CTS input is high. Although it will not allow any other characters to be transmitted, the receiver shift register (RSR) is still overrun.

Input Port

The 40-pin version of the SCN2681 and SCN68681 have a 7-bit input port that can be read through two different means. The port can be read in parallel by doing a read at address 'OD' hex. The lower four bits of the input port can also be read through the input port change register (IPCR). The bits in the IPCR will change as IP0–IP3 change. IPCR[0:3] show the current state of IP0–IP3. IPCR[4:7] will be set if a change of state has occurred since the IPCR was read last. Users will note that there can be differences between the data in the lower four data bits when a read is executed at address 'OD' hex. The reason for the difference is that the IPCR is updated by the internal state machine which is run on a 38.4k clock. It will take at least one clock time (25μs) to update the IPCR. Since a read of the input port is done immediately, there can be a difference in the two values.

In order to demonstrate how IP0–IP3 can interrupt the CPU, assume that the IP0 input is connected to some critical element. The interrupt is enabled by writing a one to the delta IP0 interrupt (ACR[0]) and also to the input port change mask (IMR[7]). The delta

change bits (IPCR[4:7]) should be reset by performing a read of the IPCR. When IP0 changes, IPCR[4] will be set and with it ISR[7] will set, causing an interrupt. The interrupt is reset by a read of the IPCR.

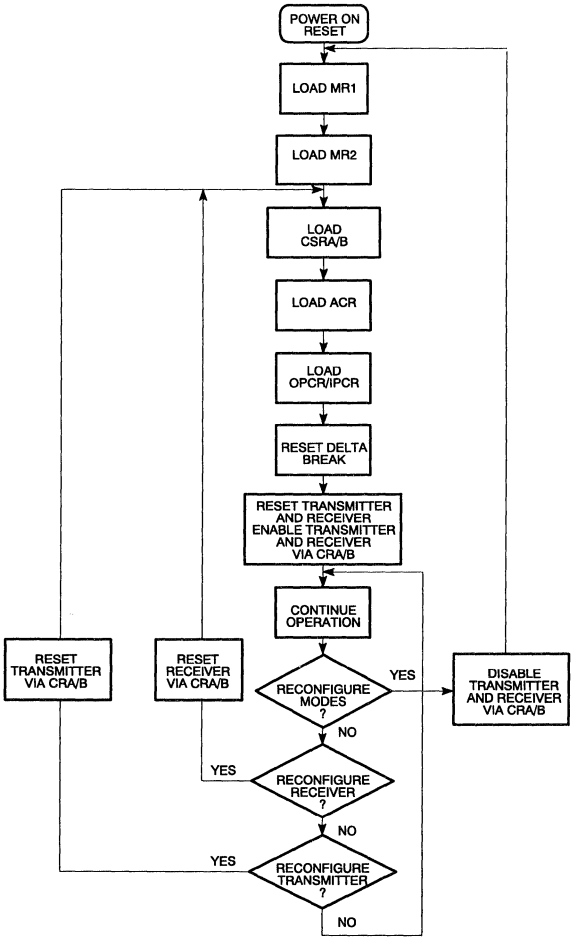


Figure 1. Asynchronous Initialization

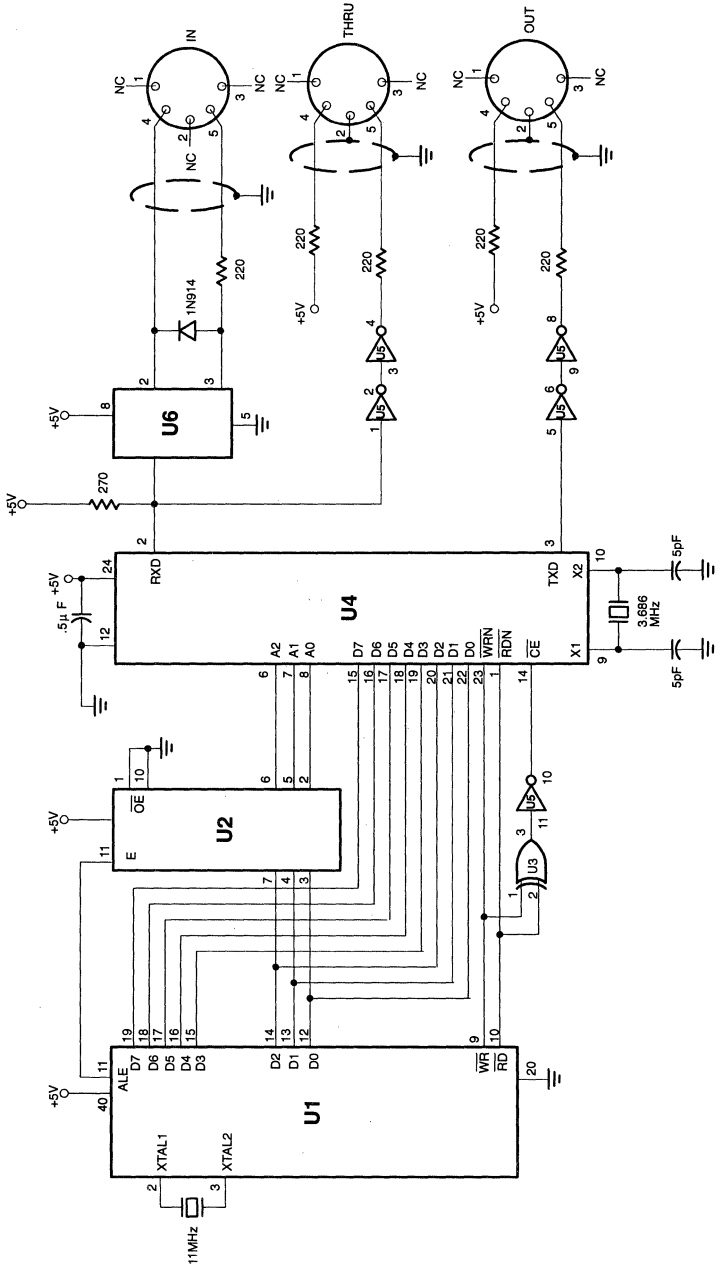


Figure 2. MIDI Interface Using SCC2691

Dual asynchronous receiver/transmitter (DUART) SCN2681T

DESCRIPTION

The Philips Semiconductors SCN2681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. The SCN2681T features a faster bus cycle time than the standard SCN2681. The quick bus cycle eliminates or reduces the need for wait states with fast CPUs and permits high throughput in I/O intensive systems. Higher external clock rates may be used with the transmitter, receiver and counter timer which in turn provide greater versatility in baud rate generation. The SCN2681T interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruple buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the receiver buffer is full.

Also provided on the SCN2681T are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

For a complete functional description and programming information for the SCN2681T, refer to the SCN2681 product specification.

FEATURES

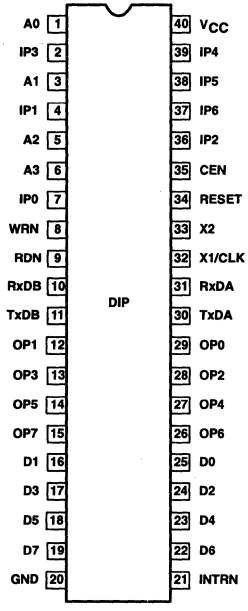
- Fast bus cycle times reduce or eliminate CPU wait states
- Dual full-duplex asynchronous receiver/transmitters
- Quadruple buffered receiver data registers
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - Non-standard rates to 115.2
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function programmable 16-bit counter/timer
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
  - 100kΩ typical pull-up resistors
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer rates:
  1X – 1MB/sec transmitter and receiver; 16X – 500kB/sec receiver and 250kB/sec transmitter
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Single +5V power supply
- Commercial and industrial temperature ranges available

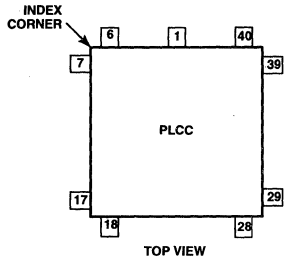
ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±10%, T_A = 0°C to +70°C	DWG #
40-Pin Plastic Dual In-Line Package (600mil-wide DIP)	SCN2681TC1N40	0415C
44-Pin Plastic Lead Chip Carrier (PLCC)	SCN2681TC1A44	0403G

NOTE: For a full register description and programming information see the SCN2681.

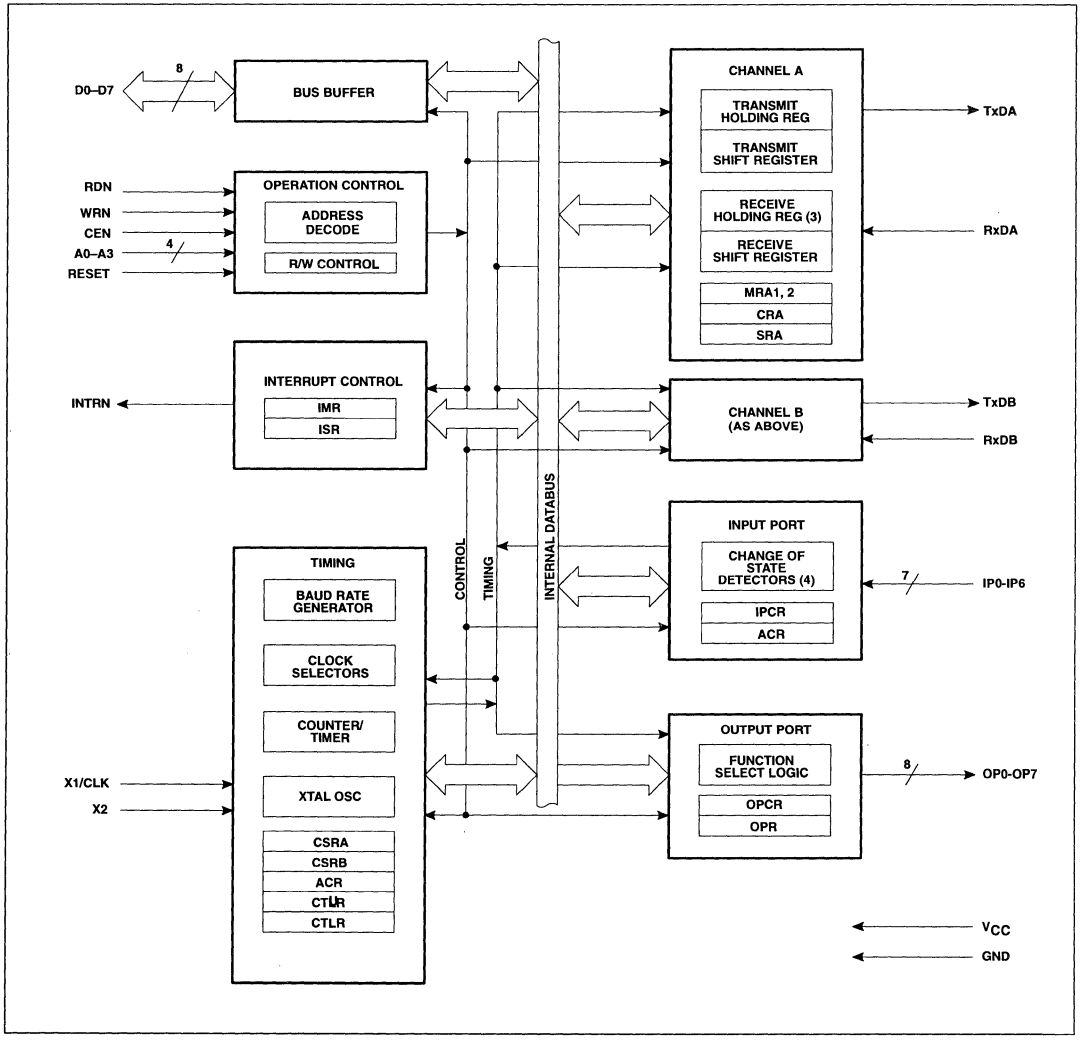
PIN CONFIGURATIONS





PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A0	24	INTRN
3	IP3	25	D6
4	A1	26	D4
5	IP1	27	D2
6	A2	28	D0
7	A3	29	OP6
8	IP0	30	OP4
9	WRN	31	OP2
10	RDN	32	OP0
11	RxDB	33	TxDA
12	NC	34	NC
13	TxDB	35	RxDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CEN
18	D1	40	IP2
19	D3	41	IP6
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	V_{CC}

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	TYPE	NAME AND FUNCTION
D0–D7	I/O	**Data Bus:** Bidirectional three-state data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	I	**Chip Enable:** Active low input signal. When low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the WRN, RDN, and A0–A3 inputs. When CEN is high, the DUART places the D0–D7 lines in the three-state condition.
WRN	I	**Write Strobe:** When low and CEN is also low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	I	**Read Strobe:** When low and CEN is also low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0–A3	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	I	**Reset:** A high level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0–OP7 in the high state, stops the counter/timer, and puts channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (high) state. Clears Test modes, sets MR pointer to MR1.
INTRN	O	**Interrupt Request:** Active-low, open-drain output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5).
X2	I	**Crystal 2:** Connection for other side of crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5). If X1/CLK is driven from an external source, this pin should be grounded.
RxDA	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. 'Mark' is high, 'space' is low.
RxDB	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. 'Mark' is high, 'space' is low.
TxDA	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is high, 'space' is low.
TxDB	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is high, 'space' is low.
OP0	O	**Output 0:** General purpose output, or channel A request to send (RTSAN, active-low). Can be deactivated automatically on receive or transmit.
OP1	O	**Output 1:** General purpose output, or channel B request to send (RTSBN, active-low). Can be deactivated automatically on receive or transmit.
OP2	O	**Output 2:** General purpose output, or channel A transmitter 1X or 16X clock output, or channel A receiver 1X clock output.
OP3	O	**Output 3:** General purpose output, or open-drain, active-low counter/timer output, or channel B transmitter 1X clock output, or channel B receiver 1X clock output.
OP4	O	**Output 4:** General purpose output, or channel A open-drain, active-low, RxRDYA/FFULLA output.
OP5	O	**Output 5:** General purpose output, or channel B open-drain, active-low, RxRDYB/FFULLB output.
OP6	O	**Output 6:** General purpose output, or channel A open-drain, active-low, TxRDYA output.
OP7	O	**Output 7:** General purpose output, or channel B open-drain, active-low TxRDYB output.
IP0	I	**Input 0:** General purpose input, or channel A clear to send active-low input (CTSAN).
IP1	I	**Input 1:** General purpose input, or channel B clear to send active-low input (CTSBN).
IP2	I	**Input 2:** General purpose input, or counter/timer external clock input.
IP3	I	**Input 3:** General purpose input, or channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	I	**Input 4:** General purpose input, or channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	I	**Input 5:** General purpose input, or channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	I	**Input 6:** General purpose input, or channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	I	**Power Supply:** +5V supply input.
GND	I	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
	All voltages with respect to GND[3]	-0.5 to +6.0	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL} V_{IH} V_{IH}	Input low voltage Input high voltage (except X1/CLK) Input high voltage (X1/CLK)		 2.0 3.5		0.8	V
V_{OL} V_{OH}	Output low voltage Output high voltage (except o.c. outputs)[4]	I_{OL} = 2.4mA I_{OH} = -400µA	 2.4		0.4	V
I_{IL} I_{LL}	Input leakage current Data bus 3-state leakage current	V_{IN} = 0 to V_{CC} V_O = 0.4 to V_{CC}	-10 -10		10 10	µA
I_{X1L}	X1/CLK low input current	V_{IN} = 0, X2 grounded V_{IN} = 0, X2 floated	-4 -3	-2 -1.5	0 0	mA mA
I_{X1H}	X1/CLK high input current	V_{IN} = V_{CC}, X2 = grounded V_{IN} = V_{CC}, X2 floated	-1 0	0.2 3.5	1 10	mA mA
I_{X2L} I_{X2H}	X2 low input current X2 high input current	V_{IN} = 0, X1/CLK floated V_{IN} = V_{CC}, X1/CLK floated	-100 0	-30 +30	0 100	µA µA
I_{OC}	Open-collector output leakage current	V_O = 0.4 to V_{CC}	-10		10	µA
I_{CC}	Power supply current[5] 0°C to +70°C version				150	mA

NOTES:
1. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.0V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. For bus operations, CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3, 4]

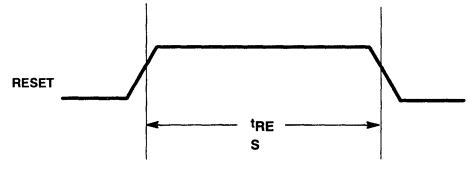


Figure 1. Reset Timing

NOTES:
1. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.0V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{RES}	Reset pulse width	1.0		µs

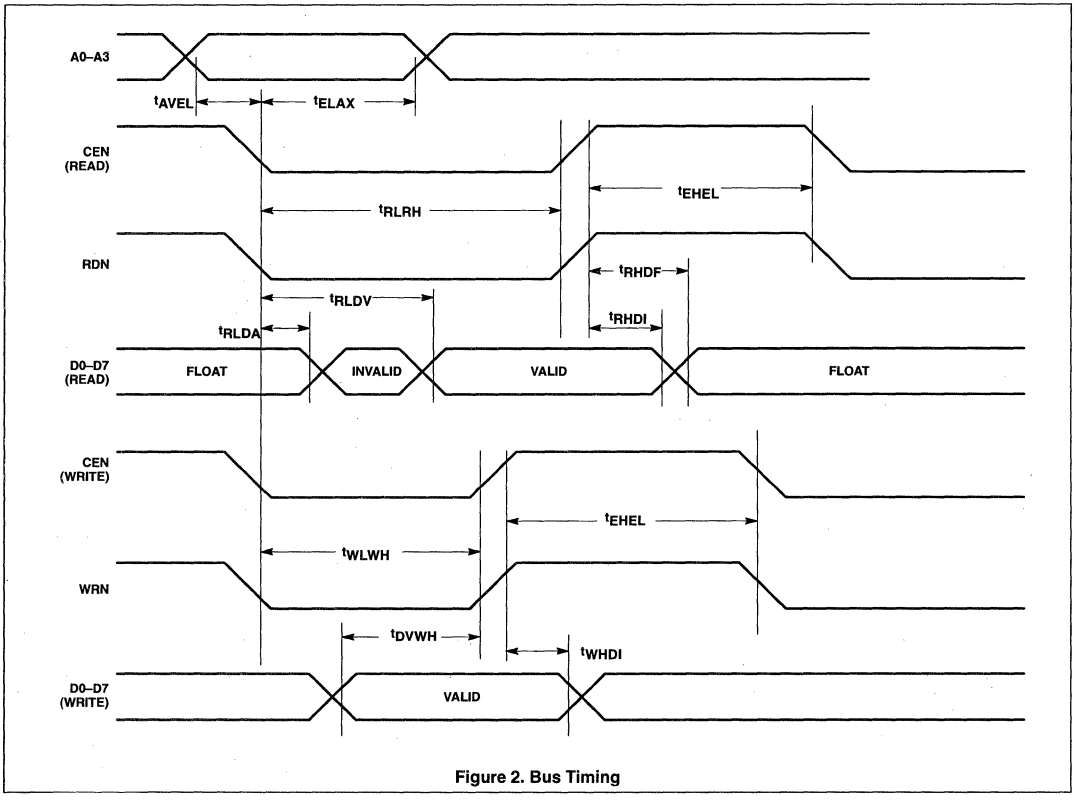


Figure 2. Bus Timing

SYMBOL	PARAMETER[1]	LIMITS		UNIT
		Min	Max	
t_{AVEL}	A0–A3 setup to RDN and CEN, or WRN and CEN low	0		ns
t_{ELAX}	RDN and CEN, or WRN and CEN low to A0–A3 invalid	100		ns
t_{RLRH}	RDN and CEN low to RDN or CEN high	120		ns
t_{EHEL}	CEN high to CEN low[2, 3]	110		ns
t_{RLDA}	CEN and RDN low to data outputs active	15		ns
t_{RLDV}	CEN and RDN low to data valid			ns
t_{RHDI}	CEN or RDN high to data invalid	10		ns
t_{RHDF}	CEN or RDN high to data outputs floating		100	ns
t_{WLWH}	WRN and CEN low to WRN or CEN high	75		ns
t_{DVWH}	Data input valid to WRN or CEN high	35	65	ns
t_{WHDI}	WRN or CEN high to data invalid	15		ns

NOTES:
1. For bus operations, CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
2. If CEN is used as the 'strobing' input, the parameter defines the minimum high times between one CEN and the next. The RDN signal must be negated for t_{EHEL} to guarantee that any status register changes are valid. As a consequence, this minimum time must be met for the RDN input even if the CEN is used as the strobing signal for bus operations.
3. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.

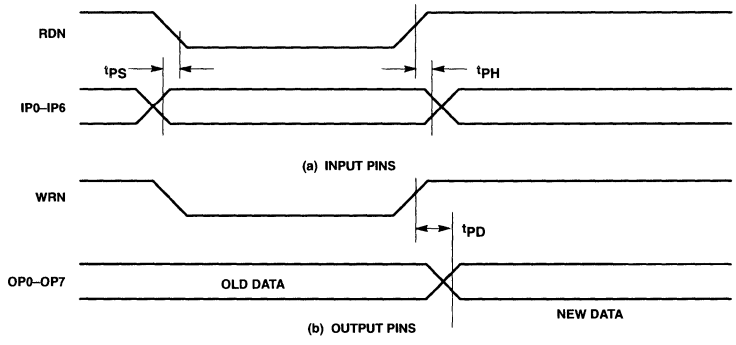
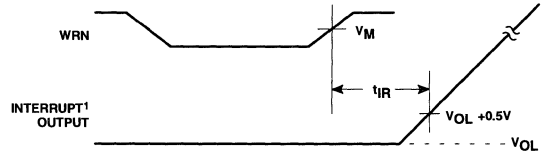


Figure 3. Port Timing

SYMBOL	PARAMETER[1]	LIMITS		UNIT
		Min	Max	
t_{PS}	Port input setup time before RDN low	0		ns
t_{PH}	Port input hold time after RDN high	0		ns
t_{PD}	Port output valid after WRN high		200	ns

NOTE:
1. For bus operations, CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.



NOTES:
1. INTRN or OP3-OP7 when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, V_M, to a point 0.5V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 4. Interrupt Timing

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{IR}	INTRN (or OP3–OP7 when used as interrupts) negated from:			
	Read RHR (RxRDY/FFULL interrupt)		200	ns
	Write THR (TxRDY interrupt)		200	ns
	Reset command (delta break interrupt)		200	ns
	Stop C/T command (counter interrupt)		200	ns
	Read IPCR (input port change interrupt)		200	ns
	Write IMR (clear of interrupt mask bit)		200	ns

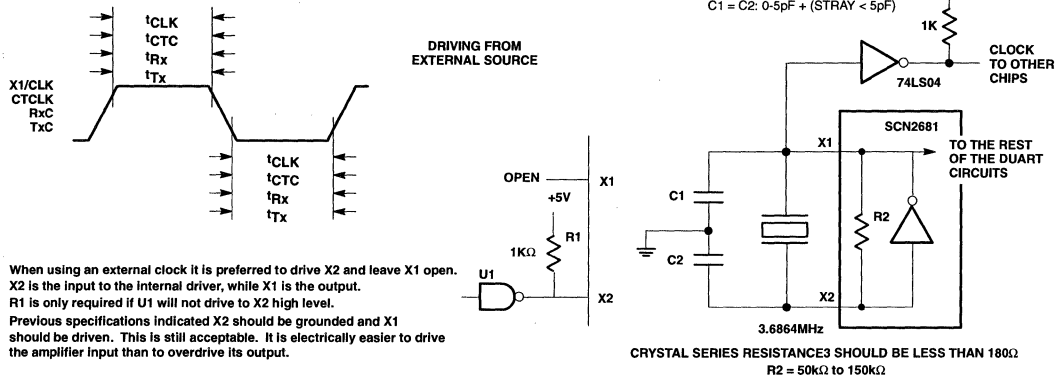


Figure 5. Clock Timing

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
	X1/CLK high or low time	90			ns
t_{CLK}	X1/CLK frequency	2		4	MHz
f_{CLK}	CTCLK (IP2) high or low time	55			ns
t_{CTC}	CTCLK (IP2) frequency[1]	0		8	MHz
f_{CTC}	RxC high or low time	55			ns
t_{RX}	RxC frequency (16X)[1]	0	3.6864	8	MHz
f_{RX}	(1X)[1]	0		1	MHz
t_{TX}	TxC high or low time	110			ns
f_{TX}	TxC frequency (16X)[1]	0		4	MHz
	(1X)[1]	0		1	MHz

NOTE:
1. Minimum frequencies are not tested but are guaranteed by design.

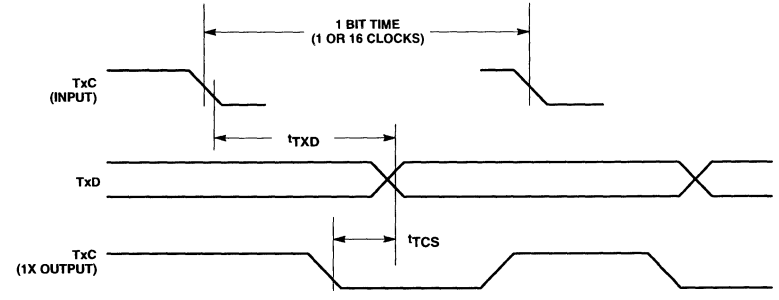


Figure 6. Transmit

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{TXD}	TxD output delay from TxC low		300	ns
t_{TCS}	Output delay from TxC low to TxD data output	0	100	ns

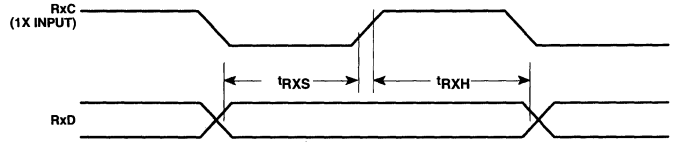
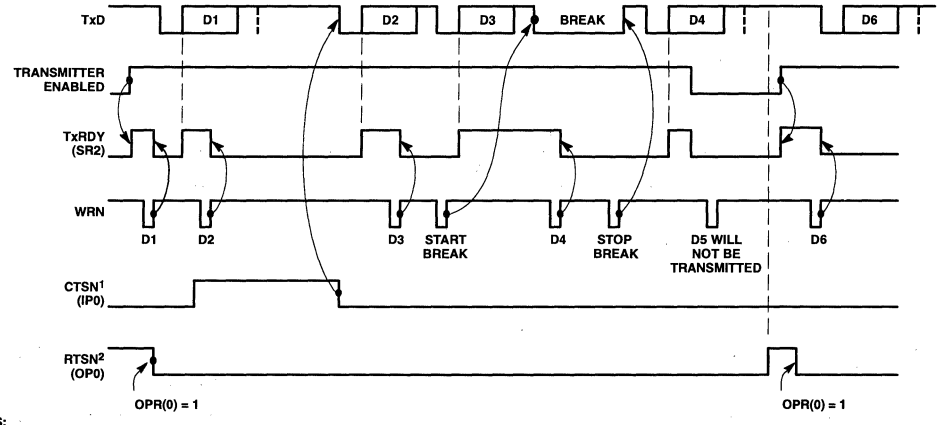


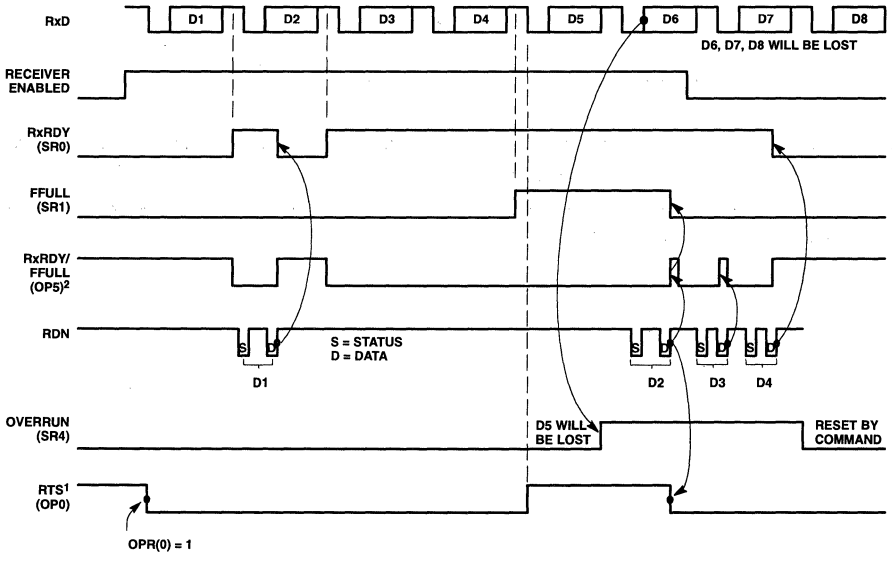
Figure 7. Receive

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_{RXS}	RxD data setup time to RxC high	200		ns
t_{RXH}	RxD data hold time from RxC high	25		ns



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 8. Transmitter Timing



NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) = 1 and MR1(6) = 0.

Figure 9. Receiver Timing

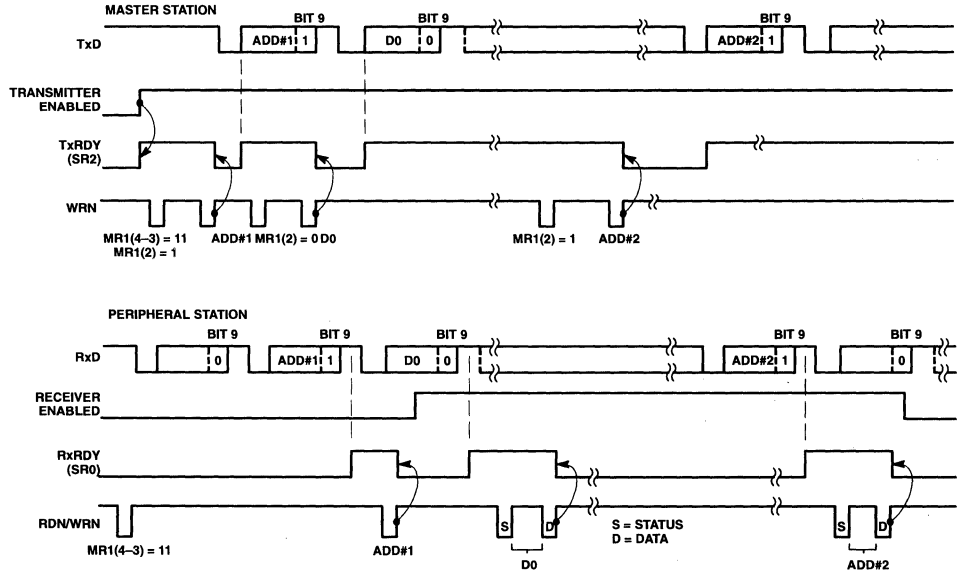


Figure 10. Wake-Up Mode

Dual asynchronous receiver/transmitter (DUART) SCN68681

DESCRIPTION

The Philips Semiconductors SCN68681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. It is compatible with other S68000 family devices, and can also interface easily with other microprocessors. The DUART can be used in polled or interrupt driven systems.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruply buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the buffer of the receiving device is full.

Also provided on the SCN68681 are a multipurpose 6-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

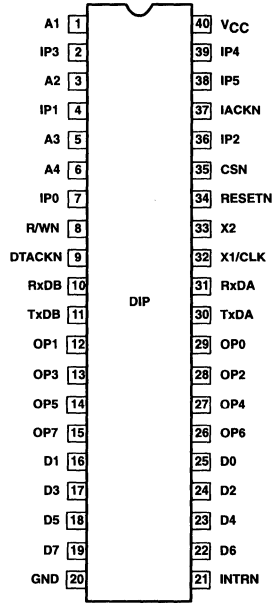
FEATURES

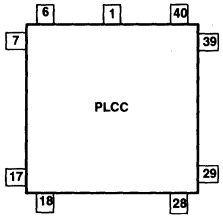
- S68000 bus compatible
- Dual full-duplex asynchronous receiver/transmitter
- Quadruple buffered receiver data registers
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - Non-standard rates to 115.2kb
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
- Multi-function programmable 16-bit counter/timer
- Multi-function 6-bit input port
  - Can serve as clock or control inputs
  - Change-of-state detection on four inputs
  - 100kΩ typical pull-up resistors
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Interrupt vector output on interrupt acknowledge
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer rates:
  1X - 1MB/sec, 16X - 125kB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Single +5V power supply
- Commercial and industrial temperature ranges available
- DIP and PLCC packages

ORDERING INFORMATION

DESCRIPTION	ORDER CODE		DWG #
	V_{CC} = +5V +5%, T_A = 0°C to +70°C	V_{CC} = +5V +10%, T_A = 40°C to +85°C	
40-Pin Ceramic Dual In-Line Package (cerdip)	Not available	SCN68681E1F40	0590B
40-Pin Plastic Dual In-Line Package (DIP)	SCN68681C1N40	SCN68681E1N40	0415C
44-Pin Plastic Leaded Chip Carrier (PLCC)	SCN68681C1A44	SCN68681E1A44	0403G

PIN CONFIGURATIONS





PIN/FUNCTION

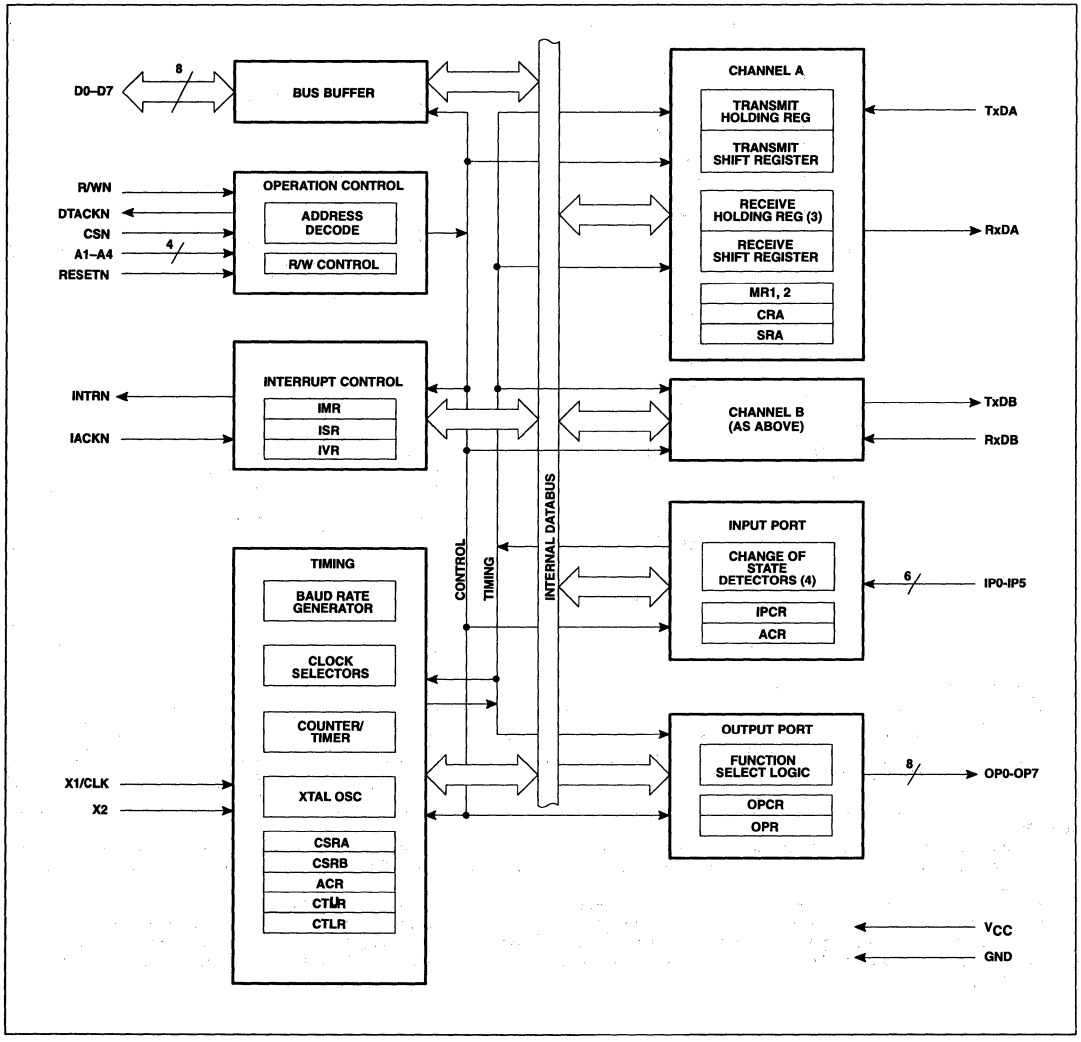
1	NC	16	OP5	31	OP2
2	A1	17	OP7	32	OP0
3	IP3	18	D1	33	TxDA
4	A2	19	D3	34	NC
5	IP1	20	D5	35	RxDA
6	A3	21	D7	36	X1/CLK
7	A4	22	GND	37	X2
8	IP0	23	NC	38	RESETN
9	R/WN	24	INTRN	39	CSN
10	DTACKN	25	D6	40	IP2
11	RxDB	26	D4	41	IACKN
12	NC	27	D2	42	IP5
13	TxDB	28	D0	43	IP4
14	OP1	29	OP6	44	V_{CC}
15	OP3	30	OP4		

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	See Note 4	°C
T_{STG}	Storage temperature range	-65 to +150	°C
	All voltages with respect to ground[3]	-0.5 to +6.0	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	TYPE	NAME AND FUNCTION
D0-D7	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CSN	I	**Chip Select:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the R/WN, RDN and A1-A4 inputs. When High, places the D0-D7 lines in the 3-State condition.
R/WN	I	**Read/Write:** A High input indicates a read cycle and a Low input indicates a write cycle, when a cycle is initiated by assertion of the CSN input.
A1-A4	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESETN	I	**Reset:** A Low level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), initializes the IVR to hex 0F, puts OP0-OP7 in the High state, stops the counter/timer, and puts Channel A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Clears Test modes, sets MR pointer to MR1.
DTACKN	O	**Data Transfer Acknowledge:** Three-state active Low output asserted in write, read, or interrupt cycles to indicate proper transfer of data between the CPU and the DUART.
INTRN	O	**Interrupt Request:** Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
IACKN	I	**Interrupt Acknowledge:** Active-Low input indicating an interrupt acknowledge cycle. In response, the DUART will place the interrupt vector on the data bus and will assert DTACKN if it has an interrupt pending.
X1/CLK	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. If a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7).
X2	I	**Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7). If an external clock is used, this pin should be grounded.
RxDA	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low.
OP0	O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	O	**Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYA/FFULLA output.
OP5	O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYB/FFULLB output.
OP6	O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYA output.
OP7	O	**Output 7:** General purpose output, or Channel B open-drain, active-Low, TxRDYB output.
IP0	I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	I	**Input 2:** General purpose input, or Channel B receiver external clock input (RxCB), or counter/timer external clock input. When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP3	I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
V_{CC}	I	**Power Supply:** +5V supply input.
GND	I	**Ground:**

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage					
V_{IH}	Input high voltage (except X1/CLK)[5]		2		0.8	V
V_{IH}	Input high voltage (except X1/CLK)[4]		2.5			
V_{IH}	Input high voltage (X1/CLK)		4			
V_{OL}	Output low voltage	I_{OL} = 2.4mA				
V_{OH}	Output high voltage (except o.d. outputs)[5]	I_{OH} = -400µA	2.4		0.4	V
V_{OH}	Output high voltage (except o.d. outputs)[4]	I_{OH} = -400µA	2.9			
I_{IL}	Input leakage current	V_{IN} = 0 to V_{CC}	–10		10	µA
I_{LL}	Data bus 3-State leakage current	V_O = 0.4 to V_{CC}	–10		10	
I_{X1L}	X1/CLK low input current	V_{IN} = 0, X2 grounded	-4	-2	0	mA
		V_{IN} = 0, X2 floated	-3	-1.5	0	mA
I_{X1H}	X1/CLK high input current	V_{IN} = V_{CC}, X2 grounded	-1	0.2	1	mA
		V_{IN} = V_{CC}, X2 floated	0	3.5	10	mA
I_{X2L}	X2 low input current	V_{IN} = 0, X1/CLK floated	-100	-30	0	µA
I_{X2H}	X2 high input current	V_{IN} = V_{CC}, X1/CLK floated	0	+30	100	µA
I_{OC}	Open-collector output leakage current				10	µA
I_{CC}	Power supply current	V_O = 0.4 to V_{CC}	–10			
	0°C to +70°C version				150	mA
	-40°C to +85°C version				175	mA

NOTES:
1. Parameters are valid over specified temperature range. See Ordering information table for applicable operating temperature range and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. T_A < 0°C
5. $T_A \geq$ 0°C

AC CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10% [1, 2, 3, 4]

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ[3]	Max	
Reset Timing (See Figure 1)					
t_{RES}	RESETN pulse width	200			ns
Bus Timing (See Figures 2, 3, 4)					
t_{AS}	A1-A4 setup time to CSN Low	10			ns
t_{AH}	A1-A4 hold time from CSN Low	100			ns
t_{RWS}	RWN setup time to CSN High	0			ns
t_{RWH}	RWN holdup time to CSN High	0			ns
t_{CSW}	CSN High pulse width	90			ns
t_{CSD}[5]	CSN or IACKN High from DTACKN Low	20			ns
t_{DD}	Data valid from CSN or IACKN Low			175	ns
t_{DF}	Data bus floating from CSN or IACKN High[7]			100	ns
t_{DS}	Data setup time to CLK High	100			ns
t_{DH}	Data hold time from CSN High	20			ns
t_{DAL}	DTACKN Low from read data valid	0			ns
t_{DCR}	DTACKN Low (read cycle) from CLK High			125	ns
t_{DCW}	DTACKN Low (write cycle) from CLK High			125	ns
t_{DAH}	DTACKN High from CSN or IACKN High			100	ns
t_{DAT}	DTACKN High impedance from CSN or IACKN High			125	ns
t_{CSC}[6]	CSN or IACKN setup time to clock High	90			ns
Port Timing (See Figure 5)					
t_{PS}	Port input setup time to CSN Low	0			ns
t_{PH}	Port input hold time from CSN High	0			ns
t_{PD}	Port output valid from CSN High			400	ns
Interrupt Reset Timing (See Figure 6)					
t_{IR}	INTRN or OP3-OP7 when used as interrupts negated from:				
	Read RHR (RxRDY/FFULL interrupt)			300	ns
	Write THR (TxRDY interrupt)			300	ns
	Reset command (delta break interrupt)			300	ns
	Stop C/T command (counter interrupt)			300	ns
	Read IPCR (input port change interrupt)			300	ns
	Write IMR (clear of interrupt mask bit)			300	ns
Clock Timing (See Figure 7)					
t_{CLK}	X1/CLK High or Low time	100			ns
f_{CLK}	X1/CLK frequency	0[8]	3.6864	4.0	MHz
t_{CTC}	CTCLK High or Low time	100			ns
f_{CTC}	CTCLK frequency	0		4.0	MHz
t_{RX}	RxC High or Low time	220			ns
f_{RX}	RxC frequency (16X)	0		2.0	MHz
	(1X)	0		1.0	MHz
t_{TX}	TxC High or Low time	220			ns
f_{TX}	TxC frequency (16X)	0		2.0	MHz
	(1X)	0		1.0	MHz
Transmitter Timing (See Figure 8)					
t_{TXD}	TxD output delay from TxC Low			350	ns
t_{TCS}	Output delay from TxC Low to TxD data output			150	ns
Receiver Timing (See Figure 9)					
t_{RXS}	RxD data setup time to RxC High	240			ns
t_{RXH}	RxD data hold time from RxC High	200			ns

NOTES:

1. Parameters are valid over specified temp. range. See Ordering information table for applicable operating temp. and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test condition for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. This specification will impose maximum 68000 CPU CLK to 6MHz. Higher CPU CLK can be used if repeating bus reads are not performed. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.
6. This specification imposes a lower bound on CSN and IACKN Low, guaranteeing that it will be Low for at least 1 CLK period. This requirement is made on CSN only to insure assertion of DTACKN and not to guarantee operation of the part.
7. This spec is made only to insure that DTACKN is asserted with respect to the rising edge of the X1/CLK pin as shown in the timing diagram, not to guarantee operation of the part. If setup time is violated, DTACKN may be asserted as shown, or may be asserted 1 clock cycle later.
8. Operation to 0MHz is assured by design. Minimum test frequency is 2.0MHz.

BLOCK DIAGRAM

The SCN68681 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the Block Diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The DTACKN output is asserted during write and read cycles to indicate to the CPU that data has been latched on a write cycle, or that valid data is present on the bus on a read cycle.

Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR), the Auditory Control Register(ACR) and the Interrupt Vector Register (IVR). The IMR may be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. When IACKN is asserted, and the DUART has an interrupt pending, the DUART responds by placing the contents of the IVR register on the data bus and asserting DTACKN.

Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART. If an external is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 7.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4k baud. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the SCN68681 comprises a full-duplex asynchronous receiver/transmitter (DUART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

The input port pulse detection circuitry uses a 38.4kHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (assuming that the clock input is 3.6864MHz). The detection circuitry, in order to guarantee a true change in level has occurred, requires that two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs coincident with the first sample pulse. The 50µs time refers to the situation in which the change of state is just missed and the first change of state is not detected until 25µs later.

Input Port

The inputs to this unlatched 6-bit port can be read by the CPU by performing a read operation at address H'D'. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always read as a logic 1 and D6 will reflect the level of IACKN. The pins of this port can also serve as auxiliary inputs to certain portions of the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs, lasting longer than 25 - 50µs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

Output Port

The 8-bit multipurpose output port can be used as a general purpose output port, in which case the outputs are the complements of the Output Port Register (OPR). OPR[n] = 1 results in OP[n] = Low and vice versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address H'E' with the accompanying data specifying the bits to be reset (1 = set, 0 = no change). Likewise, a bit is reset by a write at address H'F' with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also individually assigned specific functions by appropriate programming of the Channel A mode registers (MR1A, MR2A), the Channel B mode registers (MR1B, MR2B), and the Output Port Configuration Register (OPCR).

OPERATION

Transmitter

The SCN68681 is conditioned to transmit data when the transmitter is enabled through the command register. The SCN68681 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When a character is loaded into the Transmit Holding Register (THR), the above conditions are negated. Data is transferred from the holding

register to transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again which means one full character time of buffering is provided. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR. If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enable, the CTSN input must be Low in order for the character to be transmitted. If it goes High in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes Low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

Receiver

The SCN68681 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive Holding Register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one-half bit time before a search for the next start bit begins.

Receiver FIFO

The RHR consists of a First-In-First-Out (FIFO) stack with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4]) will be set-upon receipt of the start bit of the new (overrunning) character).

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

Receiver Reset and Disable

Receiver disable stops the receiver immediately – data being assembled if the receiver shift register is lost. Data and status in the FIFO is preserved and may be read. A re-enable of the receiver after a disable will cause the receiver to begin assembling characters at the next start bit detected. A receiver reset will discard the present shift register date, reset the receiver ready bit (RxRDY), clear the status of the byte at the top of the FIFO and re-align the FIFO read/write pointers. This has the appearance of "clearing or flushing" the receiver FIFO. In fact, the FIFO is NEVER cleared! The data in the FIFO remains valid until overwritten by another received character. Because of this erroneous reading, the FIFO will miss-align the FIFO pointers and result in the reading of previously read data. A receiver reset will re-align the pointers.

Multidrop Mode

The DUART is equipped with a wake up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wake up' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it

wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems.

For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1x by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1x, switches the pointer to MR2x. The pointer then remains at MR2x, so that subsequent accesses are always to MR2x unless the pointer is reset to MR1x as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'OA' should never be read during normal operation since they are reserved for internal diagnostics.

MR1A – Channel A Mode Register 1

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7] – Channel A Receiver Request-to-Send Control
This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the Channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1A[6] – Channel A Receiver Interrupt Select
This bit selects either the Channel A receiver ready status (RxRDY) or the Channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

MR1A[5] – Channel A Error Mode Select
This bit select the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block" mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

Table 1. SCN68681 Register Addressing

A4	A3	A2	A1	READ (R/WN = 1)	WRITE (R/WN = 0)
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	BRG Test	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
0	1	0	0	Input Port Change Register (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Register (CRUR)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	1X/16X Test	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
1	1	0	0	Interrupt Vector Register (IVR)	Interrupt Vector Register (IVR)
1	1	0	1	Input Port	Output Port Conf. Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

MR1A[4:3l – Channel A Parity Mode Select
If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] = 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] – Channel A Parity Type Select
This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] – Channel A Bits Per Character Select
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] – Channel A Mode Select
Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically re-transmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is re-clocked and re-transmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is re-clocked and re-transmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been re-transmitted.

MR2A[5] – Channel A Transmitter Request-to-Send Control
CAUTION: When the transmitter controls the OP pin (usually used for the RTSN signal) the meaning of the pin is not RTSN at all! Rather, it signals that the transmitter has finished the transmission (i.e., end of block).

This bit allows deactivation of the RTSN output by the transmitter. This output is manually asserted and negated by the appropriate commands issued via the command register. MR2[5] set to 1 caused the RTSN to be reset automatically one bit time after the character(s) in the transmit shift register and in the THR (if any) are completely transmitted (including the programmed number of stop bits) if a previously issued transmitter disable is pending. This feature can be used to automatically terminate the transmission as follows:

1. Program the auto-reset mode: MR2[5]=1
2. Enable transmitter, if not already enabled
3. Assert RTSN via command
4. Send message
5. After the last character of the message is loaded to the THR, disable the transmitter. (If the transmitter is underrun, a special case exists. See note below.)
6. The last character will be transmitted and the RTSN will be reset one bit time after the last stop bit is sent.

NOTE: The transmitter is in an underrun condition when both the TxRDY and the TxEMT bits are set. This condition also exists immediately after the transmitter is enabled from the disabled or reset state. When using the above procedure with the transmitter in the underrun condition, the issuing of the transmitter disable must be delayed from the loading of a single, or last, character until the TxRDY becomes active again after the character is loaded.

MR2A[4] – Channel A Clear-to-Send Control
If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IP0) each time it is ready to send a character. If IP0 is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character.

MR2A[3:0] – Channel A Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16 bit. The receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit is enabled), in all cases.

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

Table 2. Register Bit Formats

	BIT 7	BIT 6	BIT 5	BIT 4 BIT 3	BIT 2	BIT 1 BIT 0
MR1A MR1B	RxRTS CONTROL	RxINT SELECT	ERROR MODE	PARITY MODE	PARITY TYPE	BITS PER CHARACTER
	0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multidrop Mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

	BIT 7 BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MR2A MR2B	CHANNEL MODE	TxRTS CONTROL	CTS ENABLE Tx	STOP BIT LENGTH*			
	00 = Normal 01 = Auto-Echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

NOTE:
*Add 0.5 to values shown for 0 - 7 if channel is programmed for 5 bits/char.

	BIT 7 BIT 6 BIT 5 BIT 4	BIT 3 BIT 2 BIT 1 BIT 0
CSRA CSRB	RECEIVER CLOCK SELECT	TRANSMITTER CLOCK SELECT
	See Text	See Text

	BIT 7	BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CRA CRB		MISCELLANEOUS COMMANDS	DISABLE Tx	ENABLE Tx	DISABLE Rx	ENABLE Rx
	Not used – should be 0	See Text	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
*Access to the upper four bits of the command register should be separated by three (3) edges of the X1 clock. A disabled transmitter cannot be loaded.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SRA SRB	RECEIVED BREAK*	FRAMING ERROR*	PARITY ERROR*	OVERRUN ERROR	TxEMT	TxRDY	FFULL	RxRDY
	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE:
* These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3 BIT 2	BIT 1 BIT 0
OPCR	**OP7**	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**
	0 = OPR[7] 1 = TxRDYB	0 = OPR[6] 1 = TxRDYA	0 = OPR[5] 1 = RxRDY/ FFULLB	0 = OPR[4] 1 = RxRDY/ FFULLA	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1x) 11 = RxCB(1x)	00 = OPR[2] 01 = TxCA(16x) 10 = TxCA(1x) 11 = RxCA(1x)

	BIT 7	BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ACR	**BRG SET SELECT**	**COUNTER/TIMER MODE AND SOURCE**	**DELTA IP3 INT**	**DELTA IP2 INT**	**DELTA IP1 INT**	**DELTA IP0 INT**
	0 = set 1 1 = set 2	See Table 4	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IPCR	**DELTA IP3**	**DELTA IP2**	**DELTA IP1**	**DELTA IP0**	**IP3**	**IP2**	**IP1**	**IP0**
	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ISR	**INPUT PORT CHANGE**	**DELTA BREAK B**	**RxRDY/ FFULLB**	**TxRDYB**	**COUNTER READY**	**DELTA BREAK A**	**RxRDY/ FFULLA**	**TxRDYA**
	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IMR	**IN. PORT CHANGE INT**	**DELTA BREAK B INT**	**RxRDY/ FFULLB INT**	**TxRDYB INT**	**COUNTER READY INT**	**DELTA BREAK A INT**	**RxRDY/ FFULLA INT**	**TxRDYA INT**
	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CTUR	**C/T[15]**	**C/T[14]**	**C/T[13]**	**C/T[12]**	**C/T[11]**	**C/T[10]**	**C/T[9]**	**C/T[8]**

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CTLR	**C/T[7]**	**C/T[6]**	**C/T[5]**	**C/T[4]**	**C/T[3]**	**C/T[2]**	**C/T[1]**	**C/T[0]**

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IVR	**IVR[7]**	**IVR[6]**	**IVR[5]**	**IVR[4]**	**IVR[3]**	**IVR[2]**	**IVR[1]**	**IVR[0]**

CSRA – Channel A Clock Select Register

CSRA[7:4] – Channel A Receiver Clock Select
This field selects the baud rate clock for the Channel A receiver. The field definition is shown in Table 3.

CSRA[3:0] – Channel A Transmitter Clock Select
This field selects the baud rate clock for the Channel A transmitter. The field definition is as shown in Table 3, except as follows:

CSRA[3:0]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP3-16X	IP3-16X
1111	IP3-1X	IP3-1X

The transmitter and receiver clock is always a 16X clock except for 1111 selection.

Table 3. Baud Rate Clock = 3.6864 MHz

CSRA[7:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
0000	50	75
0001	110	110
0010	134.5	134.5
0011	200	150
0100	300	300
0101	600	600
0110	1,200	1,200
0111	1,050	2,000
1000	2,400	2,400
1001	4,800	4,800
1010	7,200	1,800
1011	9,600	9,600
1100	38.4k	19.2k
1101	Timer	Timer
1110	IP4-16X	IP4-16X
1111	IP4-1X	IP4-1X

See Table 6. also.

CSRB – Channel B Clock Select Register

CSRB[7:4] – Channel B Receiver Clock Select
This field selects the baud rate clock for the Channel B receiver. The field definition is as shown in Table 3, except as follows:

CSRB[7:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP2-16X	IP2-16X
1111	IP2-1X	IP2-1X

The receiver clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0] – Channel B Transmitter Clock Select
This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

CSRB[3:0]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP5-16X	IP5-16X
1111	IP5-1X	IP5-1X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

CRA[7] – Not Used
Should be set to zero for upward compatibility with newer parts.

CRA[6:4] – Miscellaneous Commands
The encoded value of this field may be used to specify a single command as follows:

CRA[6:4] – COMMAND
NOTE: Access to the upper four bits of the command register should be separated by three (3) edges of the X1 clock.

000 No command.
001 Reset MR pointer. Causes the Channel A MR pointer to point to MR1.
010 Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.
011 Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.
100 Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.
101 Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.
110 Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.
111 Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.

CRA[3] – Disable Channel A Transmitter
This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2] – Enable Channel A Transmitter
Enables operation of the Channel A transmitter. The TxRDY status bit will be asserted.

CRA[1] – Disable Channel A Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] – Enable Channel A Receiver
Enables operation of the Channel A receiver. If not in the special wake up mode, this also forces the receiver into the search for start-bit state.

CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.,

SRA – Channel A Status Register

SRA[7] – Channel A Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received further entries to the FIFO are inhibited until the RxDA line to the marking state for at least one-half a bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

SRA[6] – Channel A Framing Error
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SRA[5] – Channel A Parity Error
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multidrop mode the parity error bit stores the receive A/D bit.

SRA[4] – Channel A Overrun Error
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a 'reset error status' command.

SRA[3] – Channel A Transmitter Empty (TxEMTA)
This bit will be set when the transmitter underruns, i.e., both the TxEMT and TxRDY bits are set. This bit and TxRDY are set when the transmitter is first enabled and at any time it is re-enabled after either (a) reset, or (b) the transmitter has assumed the disabled state. It is always set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission.

It is reset when the THR is loaded by the CPU, a pending transmitter disable is executed, the transmitter is reset, or the transmitter is disabled while in the underrun condition.

SRA[2] – Channel A Transmitter Ready (TxRDYA)
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, viz., characters loaded into the THR while the transmitter is disabled will not be transmitted.

SRA[1] – Channel A FIFO Full (FFULLA)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SRA[0] – Channel A Receiver Ready (RxRDYA)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift to the FIFO and reset when the CPU reads the RHR, if after this read there are not more characters still in the FIFO.

SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR – Output Port Configuration Register

OPCR[7] – OP7 Output Select
This bit programs the OP7 output to provide one of the following:
0: The complement of OPR[7].
1: The Channel B transmitter interrupt output which is the complement of TxRDYB. When in this mode OP7 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[6] – OP6 Output Select
This bit programs the OP6 output to provide one of the following:
0: The complement of OPR[6].
1: The Channel A transmitter interrupt output which is the complement of TxRDYA. When in this mode OP6 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[5] – OP5 Output Select
This bit programs the OP5 output to provide one of the following:
0: The complement of OPR[5].
1: The Channel B transmitter interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[4] – OP4 Output Select
This field programs the OP4 output to provide one of the following:
0: The complement of OPR[4].
1: The Channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] – OP3 Output Select
This bit programs the OP3 output to provide one of the following:
00: The complement of OPR[3].
01: The counter/timer output, in which case OP3 acts as an open-drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
10: The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
11: The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] – OP2 Output Select
This field programs the OP2 output to provide one of the following:
00: The complement of OPR[2].
01: The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
10: The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
11: The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select

This bit selects one of two sets of baud rates to be generated by the BRG:

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.

Set 2: 75, 110, 134.5, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, and 19.2k baud.

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 4.

Table 4. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz

NORMAL RATE (BAUD)	ACTUAL 16x CLOCK (kHz)	ERROR (%)
50	0 .8	0
75	1 .2	0
110	1 .759	-0 .069
134 .5	2 .153	0 .059
150	2 .4	0
200	3 .2	0
300	4 .8	0
600	9 .6	0
1050	16 .756	-0 .260
1200	19 .2	0
1800	28 .8	0
2000	32 .056	0 .175
2400	38 .4	0
4800	76 .8	0
7200	115.2	0
9600	153.6	0
19 .2k	307.2	0
38 .4k	614.4	0

NOTE:
Duty cycle of 16x clock is 50% ± 1%.

ACR[6:4] – Counter/Timer Mode And Clock Source Select

This field selects the operating mode of the counter/timer and its clock source as shown in Table 5.

Table 5. ACR 6:4 Field Definition

ACR [6:4]	MODE	CLOCK SOURCE
000	Counter	External (IP2)*
001	Counter	TxCA – 1x clock of Channel A transmitter
010	Counter	TxCB – 1x clock of Channel B transmitter
011	Counter	Crystal or external clock (x1/CLK) divided by 16
100	Timer	External (IP2)*
101	Timer	External (IP2) divided by 16*
110	Timer	Crystal or external clock (X1/CLK)
111	Timer	Crystal or external clock (X1/CLK) divided by 16

NOTE:
* In these modes, the Channel B receiver clock should normally be generated from the baud rate generator. Timer mode generates squarewave.

ACR[3:0] – IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable

This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7] – IP3, IP2, IP1, IP0 Change-of-State

These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – IP3, IP2, IP1, IP0 Current State

These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to 00_{16} when the DUART is reset.

ISR[7] – Input Port Change Status

This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] – Channel B Change In Break

This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

ISR[5] – Channel B Receiver Ready or FIFO Full

The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in Channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel B FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[4] – Channel B Transmitter Ready

This bit is a duplicate of TxRDYB (SRB[2]).

ISR[3] – Counter Ready.
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] – Channel A Change in Break
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

ISR[1] – Channel A Receiver Ready Or FIFO Full
The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in Channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU read the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel A FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the ISR[0] and IMR waiting character is loaded into the FIFO.

ISR[0] – Channel A Transmitter Ready
This bit is a duplicate of TxRDYA (SRA[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3-OP7 or the reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is 0002_{16}. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR and CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. In this mode the C/T runs continuously. Receipt of a start counter command (read with A4-A1) = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR. The waveform so generated is often used for a data clock. The formula for calculating the divisor n to load to the CTUR and CTLR for a particular 1X data clock is shown below:

$$n = \frac{C/T\ Clock\ Frequency}{2 \cdot 16 \cdot Baud\ rate\ desired}$$

Often this division will result in a non-integer number; 26.3, for example. One can only program integer numbers in a digital divider. Therefore, 26 would be chosen. This gives a baud rate error of 0.3/26.3 which is 1.14%; well within the ability asynchronous mode of operation.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A4-A1 = 1111). The command, however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

On power-up and after reset, the counter/timer runs in timer mode and can only be restarted. Because it cannot be shut off or stopped, and runs continuously in timer mode, it is recommended that at initialization, the output port, OP3, should be masked off through the OPCR[3:2] = 00 until the C/T is programmed to the desired operational state.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching terminal count 0000_{16}, the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

IVR – Interrupt Vector Register

This register contains the interrupt vector. The register is initialized to H'0F' by RESET. The contents of the register are placed on the data bus when the DUART responds to a valid interrupt acknowledge cycle.

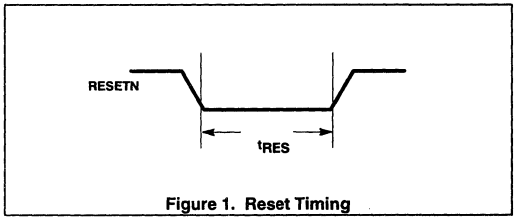


Figure 1. Reset Timing

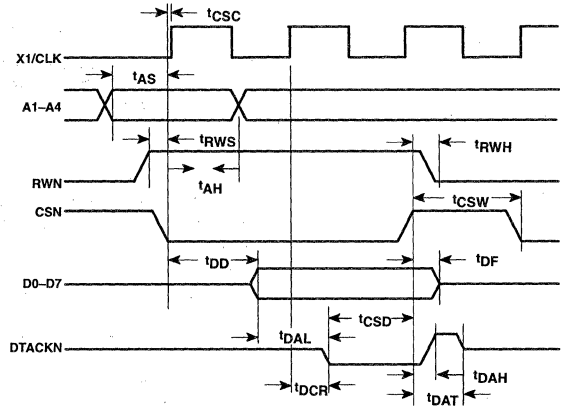
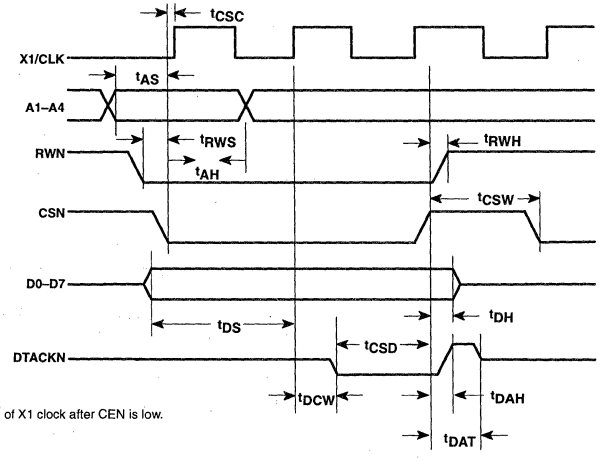


Figure 2. Bus Timing (Read Cycle)



NOTE:
DACKN requires two rising edges of X1 clock after CEN is low.

Figure 3. Bus Timing (Write Cycle)

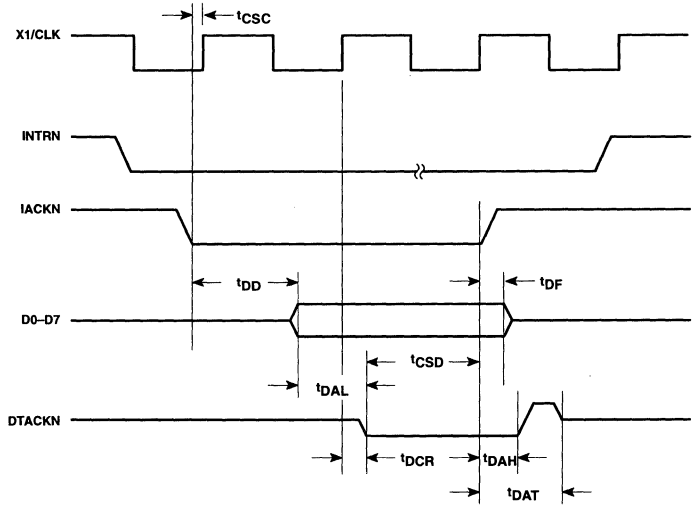


Figure 4. Interrupt Cycle Timing

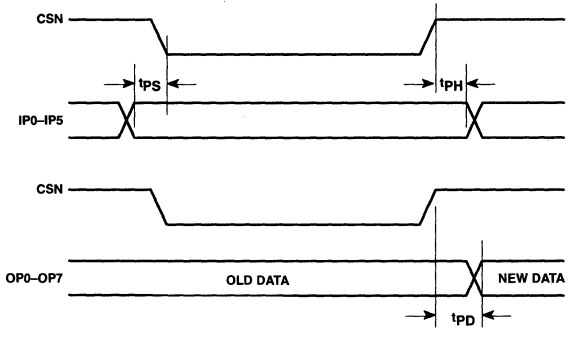


Figure 5. Port Timing

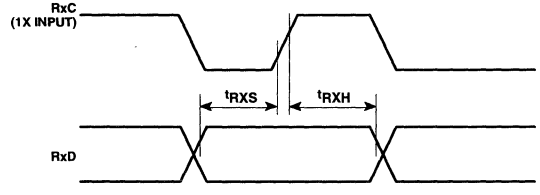


Figure 6. Receive Timing

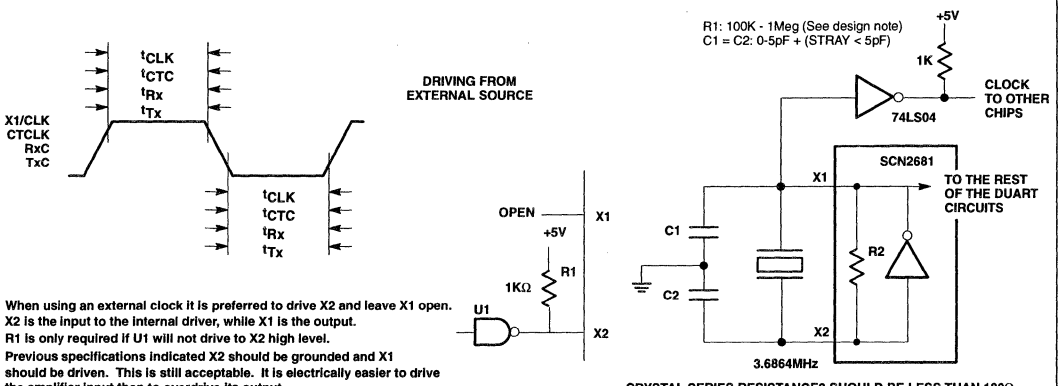
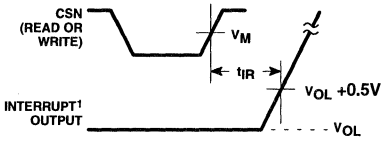


Figure 7. Clock Timing



NOTES:

1. INTRN or OP3 – OP7 when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the mid point of the switching signal, V_M, to a point 0.5 volts above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 8. Interrupt Timing

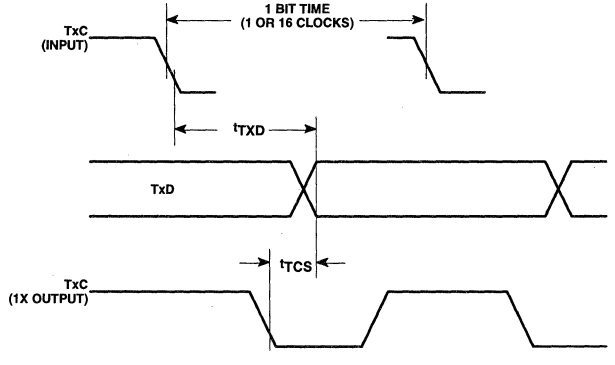


Figure 9. Transmit Timing

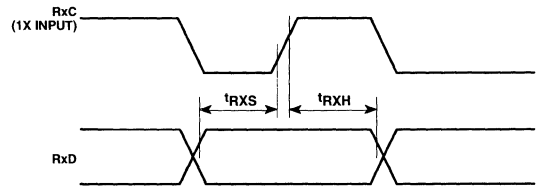
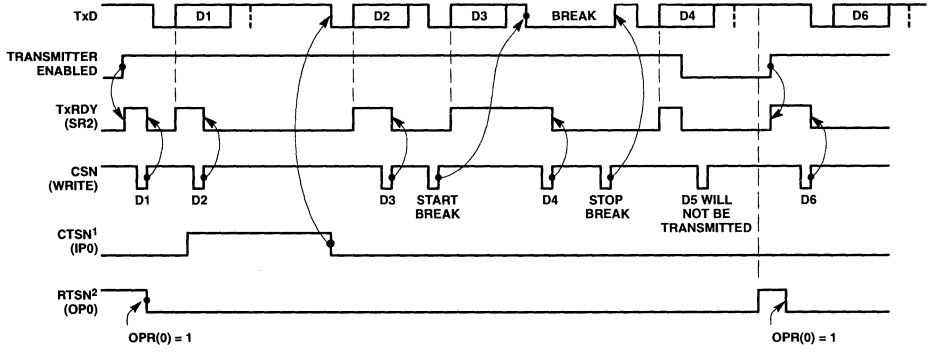
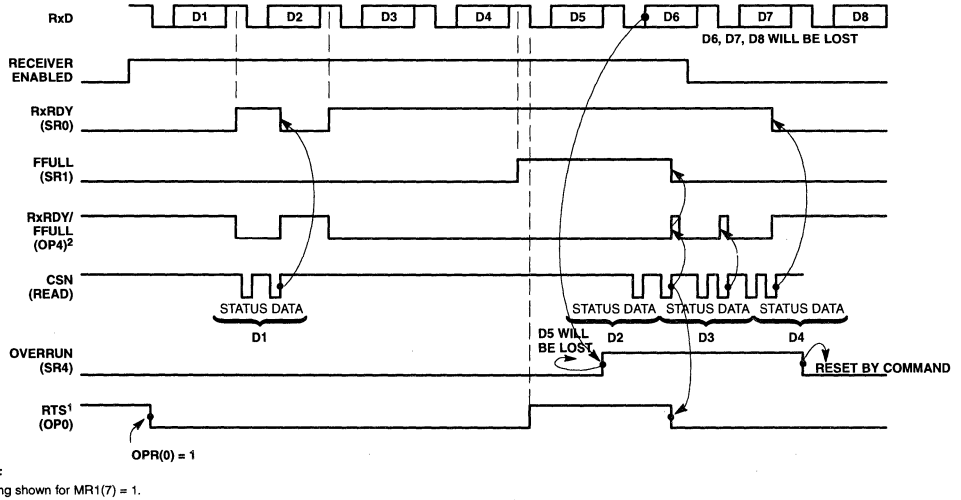


Figure 10. Receive Timing



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 11. Transmitter Timing



NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) and MR1(6) = 0.

Figure 12. Receiver Timing

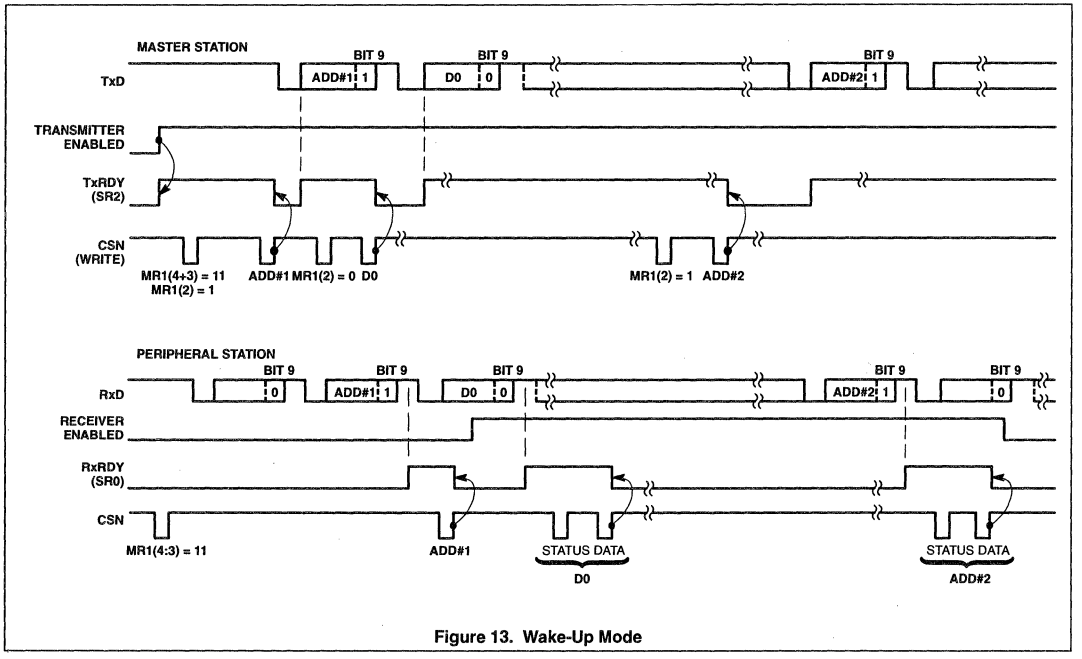


Figure 13. Wake-Up Mode

Output Port Notes

The output ports are controlled from three places: the OPCR register, the OPR register, and the MR registers. The OPCR register controls the source of the data for the output ports OP2 through OP7. The data source for output ports OP0 and OP1 is controlled by the MR and CR registers. When the OPR is the source of the data for the output ports, the data at the ports is inverted from that in the OPR register. The content of the OPR register is controlled by the "Set Output Port Bits Command". These commands are at E and F, respectively. When these commands are used, action takes place only at the bit locations where ones exist. For example, a one in bit location 5 of the data word used with the "Set Output Port Bits" command will result in OPR5 being set to one. The OP5 would then be set to zero (V_{SS}). Similarly, a one in bit position 5 of the data word associated with the "Reset Output Ports Bits" command would set OPR5 to zero, and hence, the pin OP5 to a one (V_{DD}).

The CTS, RTS, CTS Enable Tx signals

CTS (Clear To Send) is usually meant to be a signal to the transmitter meaning that it may transmit data to the receiver. The CTS input is on pin MPI. The CTS signal is active low; thus, it is called CTS.

RTS is usually meant to be a signal from the receiver indicating that the receiver is ready to receive data. It is also active low and is, thus, called RTSN. RTSN is on pin MP0. A receiver's RTS output will usually be connected to the CTS input of the associated transmitter. Therefore, one could say that RTS and CTS are different ends of the same wire!

MR2(4) is the bit that allows the transmitter to be controlled by the CTS pin (MPI). When this bit is set to one AND the CTS input is driven high, the transmitter will stop sending data at the end of the present character being serialized. It is usually the RTS output of the receiver that will be connected to the transmitter's CTS input. The receiver will set RTS high when the receiver FIFO is full AND the start bit of the fourth character is sensed. Transmission then stops with four valid characters in the receiver. When MR2(4) is set to one, CTSN must be at zero for the transmitter to operate. If MR2(4) is set to zero, the MP pin will have no effect on the operation of the transmitter.

MR1(7) is the bit that allows the receiver to control MP0. When MP0 is controlled by the receiver, the meaning of that pin will be RTS. However, a point of confusion arises in that MP0 may also be controlled by the transmitter. When the transmitter is controlling this pin, its meaning is not RTS at all. It is, rather, that the transmitter has finished sending its last data byte. Programming the MP0 pin to be controlled by the receiver and the transmitter at the same time is allowed, but would usually be incompatible.

RTS is expressed at the MP0 pin which is still an output port. Therefore, the state of MP0 should be set low for the receiver to generate the proper RTS signal. The logic at the output is basically a NAND of the MP0 bit register and the RTS signal as generated by the receiver. When the RTS flow control is selected via the MR(7) bit the state of the MP0 register is not changed. Terminating the use of "Flow Control" (via the MR registers) will return the MP0 pin to the control of the MP0 register.

Transmitter Disable Note

The sequence of instructions enable transmitter — load transmit holding register — disable transmitter will result in nothing being sent if the time between the end of loading the transmit holding register and the disable command is less that 3/16 bit time in the 16x mode or one bit time in the 1x mode. Also, if the transmitter,

while in the enabled state and underrun condition, is immediately disabled after a single character is loaded to the transmit holding register, that character will not be sent.

In general, when it is desired to disable the transmitter before the last character is sent AND the TxEMT bit is set in the status register (TxEMT is always set if the transmitter has underrun or has just been enabled), be sure the TxRDY bit is active immediately before issuing the transmitter disable instruction. TxRDY sets at the end of the "start bit" time. It is during the start bit that the data in the transmit holding register is transferred to the transmit shift register.

Non-standard baud rates are available as shown in Table 6 below, via the BRG Test function.

Table 6. Baud Rates Extended

	Normal BRG		BRG Test	
CSR[7:4]	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0000	50	75	4,800	7,200
0001	110	110	880	880
0010	134.5	134.5	1,076	1,076
0011	200	150	19.2K	14.4K
0100	300	300	28.8K	28.8K
0101	600	600	57.6K	57.6K
0110	1,200	1,200	115.2K	115.2K
0111	1,050	2,000	1,050	2,000
1000	2,400	2,400	57.6K	57.6K
1001	4,800	4,800	4,800	4,800
1010	7,200	1,800	57.6K	14.4K
1011	9,600	9,600	9,600	9,600
1100	38.4K	19.2K	38.4K	19.2K
1101	Timer	Timer	Timer	Timer
1110	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X
1111	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X

NOTE:
Each read on address H'2' will toggle the baud rate test mode. When in the BRG test mode, the baud rates change as shown to the left. This change affects all receivers and transmitters on the DUART. Also, the RTSN outputs (OP[0] and OP[1]) become the transmitter 1x clock.

The test mode at address H'A' changes all transmitters and receivers to the 1x mode and connects the output ports to some internal nodes.

A condition that occurs infrequently has been observed where the receiver will ignore all data. It is caused by a corruption of the start bit generally due to noise. When this occurs the receiver will appear to be asleep or locked up. The receiver must be reset for the UART to continue to function properly.

Reset in the Normal Mode (Receiver Enabled)

Recovery can be accomplished easily by issuing a receiver software reset followed by a receiver enable. All receiver data, status and programming will be preserved and available before reset. The reset will NOT affect the programming.

Reset in the Wake-Up Mode (MR1[4:3] = 11)

Recovery can also be accomplished easily by first exiting the wake-up mode (MR1[4:3] = 00 or 01 or 10), then issuing a receiver software reset followed by a wake-up re-entry (MR1[4:3] = 11). All receiver data, status and programming will be preserved and available before reset. The reset will NOT affect the programming.

The receiver has a digital filter designed to reject "noisy" data and the receiver state machine was designed to reject noisy start bits or noise that might be considered a start bit. In spite of these precautions, corruption of the start bit can occur in 15ns window approximately 100ns prior to the rising edge of the data clock. The probability of this occurring is less than 10^{-5} at 9600 baud.

A corrupted start bit may have some deleterious effects in ASYNC operation if it occurs within a normal data block. The receiver will tend to align its data clock to the next '0' bit in the data stream, thus potentially corrupting the remainder of the data block. A good design practice, in environments where start bit corruption is possible, is to monitor data quality (framing error, parity error, break change and received break) and "data stopped" time out periods. Time out periods can be enabled using the counter/timer in the SCC2691, SCC2692, SCC2698B and SC68692 products. This monitoring can indicate a potential start bit corruption problem.

Universal asynchronous receiver/transmitter (UART) SCC2691

DESCRIPTION

The Philips Semiconductors SCC2691 Universal Asynchronous Receiver/Transmitter (UART) is a single-chip CMOS-LSI communications device that provides a full-duplex asynchronous receiver/transmitter. It is fabricated with Philips Semiconductors CMOS technology which combines the benefits of high density and low power consumption.

The operating speed of the receiver and transmitter can be selected independently as one of 18 fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the UART particularly attractive for dual-speed channel applications such as clustered terminal systems.

The receiver is quadruple buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full.

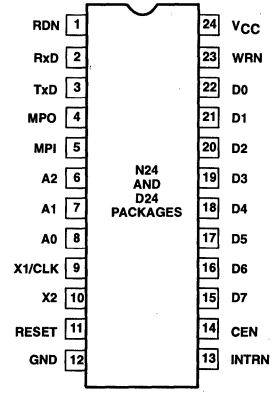
The UART provides a power-down mode in which the oscillator is frozen but the register contents are stored. This results in reduced power consumption on the order of several magnitudes.

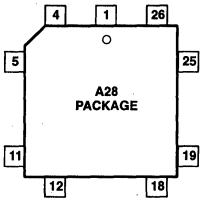
The UART is fully TTL compatible and operates from a single +5V power supply.

FEATURES

- Full-duplex asynchronous receiver/transmitter
- Quadruple buffered receiver data register
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Baud rate for the receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4K baud
  - Non-standard rates to 115.2kb
  - One user-defined rate derived from programmable timer/counter
  - External 1X or 16X clock
- Parity, framing, and overrun detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote Loopback
- Multi-function programmable 16-bit counter/timer

PIN CONFIGURATIONS





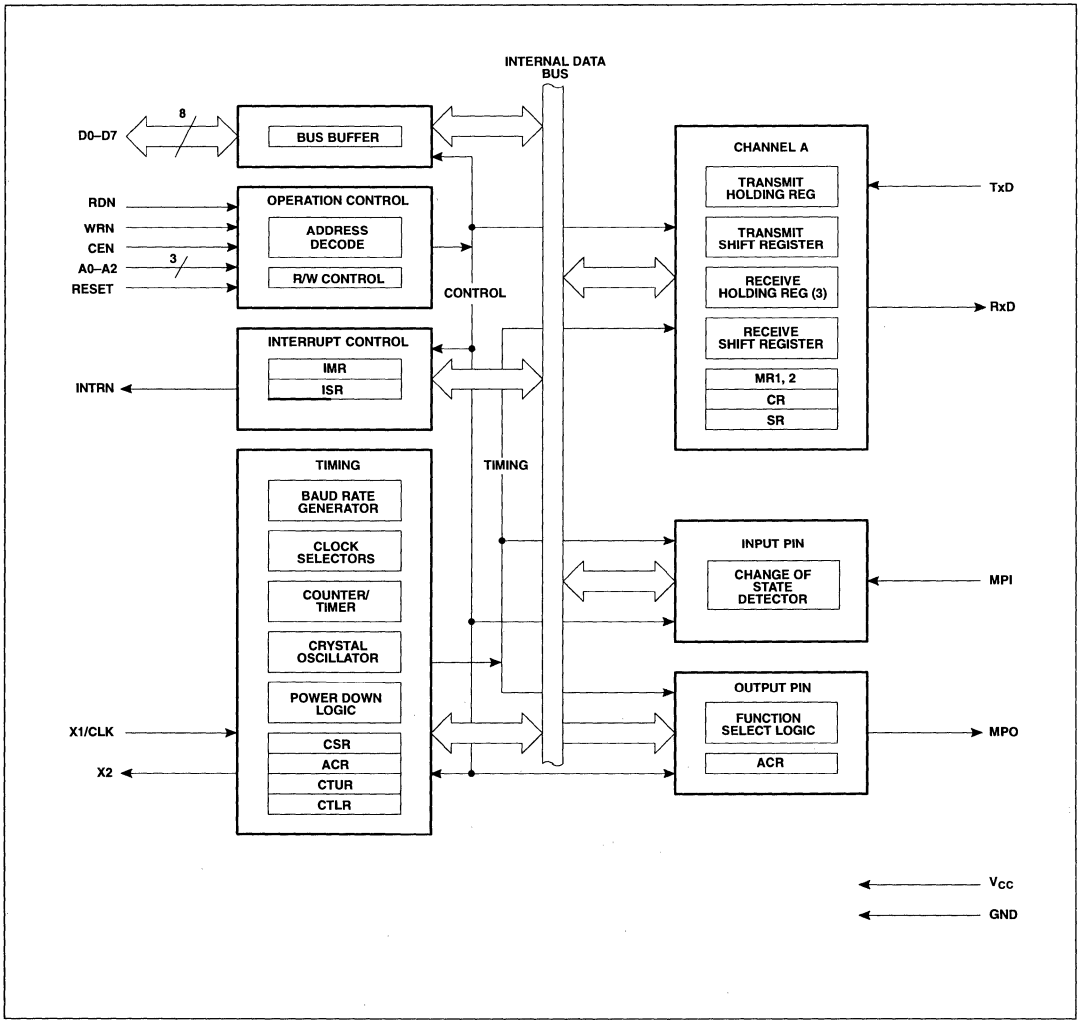
Pin	Symbol	Pin	Symbol
1	V_{CC}	15	GND
2	RDN	16	INTRN
3	RxD	17	CEN
4	TxD	18	D7
5	MPO	19	D6
6	MPI	20	D5
7	NC	21	D4
8	NC	22	D3
9	A2	23	NC
10	A1	24	D2
11	A0	25	D1
12	X1/CLK	26	NC
13	X2	27	D0
14	RESET	28	WRN

- Single interrupt output with seven maskable interrupting conditions
- On-chip crystal oscillator
- Low power mode
- TTL compatible
- Single +5V power supply
- Commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature versions available
- SOL, PLCC and 300 mil wide DIP packages available

ORDERING INFORMATION

PACKAGES	V_{CC} = +5V ±10%, T_A = 0°C to +70°C	V_{CC} = +5V ±10%, T_A = –40°C to +85°C	DWG #
24-Pin Plastic Dual In-Line Package (DIP)	SCC2691AC1N24	SCC2691AE1N24	0410D
28-Pin Plastic Leaded Chip Carrier (PLCC) Package	SCC2691AC1A28	SCC2691AE1A28	0401F
24-Pin Plastic Small Outline Large (SOL) Package	SCC2691AC1D24		0173D

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
D0–D7	22–15	27, 25, 24, 22–18	I	**Data Bus:** Active-high 8-bit bidirectional 3-State data bus. Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the UART take place over this bus. The direction of the transfer is controlled by the WRN and RDN inputs when the CEN input is low. When the CEN input is high, the data bus is in the 3-State condition.
CEN	14	17	I	**Chip Enable:** Active-low input. When low, data transfers between the CPU and the UART are enabled on D0–D7 as controlled by the WRN, RDN and A0–A2 inputs. When CEN is high, the UART is effectively isolated from the data bus and D0–D7 are placed in the 3-State condition.
WRN	23	28	I	**Write Strobe:** Active-low input. A low on this pin while CEN is low causes the contents of the data bus to be transferred to the register selected by A0–A2. The transfer occurs on the trailing (rising) edge of the signal.
RDN	1	2	I	**Read Strobe:** Active-low input. A low on this pin while CEN is low causes the contents of the register selected by A0–A2 to be placed on the data bus. The read cycle begins on the leading (falling) edge of RDN.
A0–A2	8–6	11–9	I	**Address Inputs:** Active-high address inputs to select the UART registers for read/write operations.
RESET	11	14	I	**Reset:** Master reset. A high on this pin clears the status register (SR), the interrupt mask register (IMR), and the interrupt status register (ISR), sets the mode register pointer to MR1, and places the receiver and transmitter in the inactive state causing the TxD output to go to the marking (high) state. Clears Test modes.
INTRN	13	16	O	**Interrupt Request:** This active-low output is asserted upon occurrence of one or more of seven maskable interrupting conditions. The CPU can read the interrupt status register to determine the interrupting condition(s). This open-drain output requires a pull-up resistor.
X1/CLK	9	12	I	**Crystal 1:** Crystal or external clock input. When using the crystal oscillator, this pin serves as the connection for one side of the crystal. If a crystal is not used, an external clock is supplied at this input. An external clock (or crystal) is required even if the internal baud rate generator is not utilized. This clock is used to drive the internal baud rate generator, as an optional input to the timer/counter, and to provide other clocking signals required by the chip.
X2	10	13	I	**Crystal 2:** Connection for other side of crystal. If an external source is used instead of a crystal, this connection should be open.
RxD	2	3	I	**Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified, this input is sampled on the rising edge of the clock.
TxD	3	4	O	**Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the marking (high) condition when the transmitter is idle or disabled and when the UART is operating in local loopback mode. If external transmitter is specified, the data is shifted on the falling edge of the transmitter clock.
MPO	4	5	O	**Multi-Purpose Output:** One of the following functions can be selected for this output pin by programming the auxiliary control register: **RTSN** – Request to send active-low output. This output is asserted and negated via the command register. By appropriate programming of the mode registers, RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted or when the receiver FIFO and shift register are full. **C/TO** – The counter/timer output. **TxC1X** – The 1X clock for the transmitter. **TxC16X** – The 16X clock for the transmitter. **RxC1X** – The 1X clock for the receiver. **RxC16X** – The 16X clock for the receiver. **TxRDY** – The transmitter holding register empty signal. Active-low output. **RxRDY/FFULL** – The receiver FIFO not empty/full signal. Active-low output.
MPI	5	6	I	**Multi-Purpose Input:** This pin can serve as an input for one of the following functions: **GPI** – General purpose input. The current state of the pin can be determined by reading the ISR. **CTSN** – Clear-to-send active-low input. **CTCLK** – Counter/timer external clock input. **RTCLK** – Receiver and/or transmitter external clock input. This may be a 1X or 16X clock as programmed by CSR[3:0] or CSR[7:4].
V_{CC}	24	1	I	**Power Supply:** +5V supply input.
GND	12	15	I	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	Note 4	°C
T_{STG}	Storage temperature range	−65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	−0.5 to + 7.0	V
V_S	Voltage from any pin to ground[3]	−0.5 to V_{CC} ±10%	V
P_D	Power Dissipation	300	mW

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperature, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range. See Ordering Information table for applicable operating temperature and V_{CC} supply range.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL} V_{IH}	Input low voltage Input high voltage				0.8	V
	All except X1/CLK X1/CLK		2 0.8V_{CC}		 V_{CC}	V V
V_{OL} V_{OH}[4]	Output low voltage Output high voltage (except open drain outputs)	I_{OL} = 2.4mA I_{OH} = −400µA	 2.4		0.4	V V
I_{IL}	Input leakage current	V_{IN} = 0 to V_{CC}	−10		10	µA
I_{LL}	Data bus 3-State leakage current	V_O = 0.4 to V_{CC}	−10		10	µA
I_{OD}	Open-drain output leakage current	V_O = 0.4 to V_{CC}	−10		10	µA
I_{XIL}	X1/CLK low input current	V_{IN} = 0, X2 floated	−100	−30	0	µA
I_{XIH}	X1/CLK high input current	V_{IN} = V_{CC}, X2 floated	0	30	100	µA
I_{X2L}	X2 low output current	V_{OUT} = 0, X1/CLK = V_{CC}	−100			µA
I_{X2H}	X2 high output current	V_{OUT} = V_{CC}, X1/CLK = 0V			100	µA
I_{CCA}	Power supply current, active 0°C to +70°C −40°C to +85°C			0.8 1.0	2.0 2.5	mA mA
I_{CCD}	Power down current[5]				500	µA

NOTES:
1. Parameters are valid over specified temperature range. See Ordering Information table for applicable operating temperature and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all input signals swing between 0V and 3.0V with a transition time of 20ns max. For X1/CLK, this swing is between 0.4V and 4.0V. All time measurements are referenced at input voltages of 0.8V and 2V and output voltages of 0.8V and 2V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test condition for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. For power down current levels in the 1µA region see the UART application note.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3, 4]

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Reset timing (Figure 1)					
t_{RES}	Reset pulse width	100			ns
Bus timing (Figure 2)[5]					
t_{AS}	A0–A2 setup time to RDN, WRN low	10			ns
t_{AH}	A0–A2 hold time from RDN, WRN low	100			ns
t_{CS}	CEN setup time to RDN, WRN low	0			ns
t_{CH}	CEN hold time from RDN, WRN high	0			ns
t_{RW}	WRN, RDN pulse width	150			ns
t_{DD}	Data valid after RDN low				ns
t_{DF}	Data bus floating after RDN high			125	ns
t_{DS}	Data setup time before WRN high	50		110	ns
t_{DH}	Data hold time after WRN high	30			ns
t_{RWD}	Time between reads and/or writes[6, 7]	150			ns
MPI and MPO timing (Figure 3)[5]					
t_{PS}	MPI input setup time before RDN low	30			ns
t_{PH}	MI input hold time after RDN low	30			ns
t_{PD}	MPO output valid after WRN high			370	ns
Interrupt timing (Figure 4)					
t_{IR}	INTRN negated				
	Read RHR (RxRDY/FFULL interrupt)			370	ns
	Write THR (TxRDY, TxEMT interrupt)			370	ns
	Reset command (break change interrupt)			370	ns
	Reset command (MPI change interrupt)			370	ns
	Stop C/T command (counter interrupt)			370	ns
	Write IMR (clear of interrupt mask bit)			270	ns
Clock timing (Figure 5)					
t_{CLK}	X1/CLK high or low time	100			ns
f_{CLK}	X1/CLK frequency[9]	0		4.0	MHz
t_{CTC}	Counter/timer clock high or low time	100			ns
f_{CTC}	Counter/timer clock frequency	0[8]		4.0M	Hz
t_{RX}	RxC high or low time	220			ns
f_{RX}	RxC frequency (16X)	0[8]	3.6864	2.0M	Hz
	RxC frequency (1X)	0[8]		1.0M	Hz
t_{TX}	TxC high or low time	220			ns
f_{TX}	TxC frequency (16X)	0[8]		2.0M	Hz
	TxC frequency (1X)	0[8]		1.0M	Hz
Transmitter timing (Figure 6)					
t_{TXD}	TxD output delay from TxC low			350	ns
t_{TCS}	TxC output delay from TxD output data	0		150	ns
Receiver timing (Figure 7)					
t_{RXS}	RxD data setup time to RxC high	100			ns
t_{RXH}	RxD data hold time from RxC high	100			ns

NOTES:

1. Parameters are valid over specified temp. range. See Ordering Information table for applicable operating temp. and V_{CC} supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all input signals swing between 0V and 3.0V with a transition time of 20ns max. For X1/CLK, this swing is between 0.4V and 4.0V. All time measurements are referenced at input voltages of 0.8V and 2V and output voltages of 0.8V and 2V as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test condition for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. In this case, all timing specifications apply referenced to the falling and rising edges of CEN. CEN and RDN (also CEN and WRN) are ORed internally. As a consequence, this signal asserted last initiates the cycle and the signal negated first terminates the cycle.
6. If CEN is used as the 'strobing' input, this parameter defines the minimum high time between one CEN and the next. The RDN signal must be negated for t_{RWD} guarantee that any status register changes are valid.
7. Consecutive write operations to the command register require at least three rising edges of the X1 clock between writes.
8. These parameters are guaranteed by design, but are not 100% tested in production.
9. Operation to 0MHz is assured by design. Minimum test frequency is 2MHz.

BLOCK DIAGRAM

As shown in the block diagram, the UART consists of: data bus buffer, interrupt control, operation control, timing, receiver and transmitter.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data busses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and UART.

Interrupt Control

A single interrupt output (INTRN) is provided which may be asserted upon occurrence of any of the following internal events:

- Transmit holding register ready
- Transmit shift register empty
- Receive holding register ready or FIFO full
- Change in break received status
- Counter reached terminal count
- Change in MPI input
- Assertion of MPI input

Associated with the interrupt system are the interrupt mask register (IMR) and the interrupt status register (ISR). The IMR can be programmed to select only certain of the above conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. However, the bits of the ISR are not masked by the IMR.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The functions performed by the CPU read and write operations are shown in Table 1.

Table 1. Register Addressing

A2	A1	A0	READ (RDN = 0)	WRITE (WRN = 0)
0	0	0	MR1, MR2	MR1, MR2
0	0	1	SR	CSR
0	1	0	BRG Test	CR
0	1	1	RHR	THR
1	0	0	1X/16X Test	ACR
1	0	1	ISR	IMR
1	1	0	CTU	CTUR
1	1	1	CTL	CTLR

NOTE;
*Reserved registers should never be read during operation since they are reserved for internal diagnostics.
ACR = Auxiliary control register
CR = Command register
CSR = Clock select register
CTL = Counter/timer lower
CTLR = Counter/timer lower register
CTU = Counter/timer upper
CTUR = Counter/timer upper register
MR = Mode register A
SR = Status register
THR = Tx holding register

Mode registers 1 and 2 are accessed via an auxiliary pointer. The pointer is set to MR1 by RESET or by issuing a reset pointer command via the command register. Any read or write of the mode register while the pointer is at MR1 switches the pointer to MR2. the pointer then remains at MR2 so that subsequent accesses are to MR2, unless the pointer is reset to MR1 as described above.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and two clock selectors.

The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/ CLK and X2 inputs with a minimum of external components. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. If an external clock is used instead of a crystal, X1/CLK is driven using a configuration similar to the one in Figure 5. In this case, the input high-voltage must be capable of attaining the voltage specified in the DC Electrical Characteristics. The clock serves as the basic timing reference for the baud rate generator (BRG), the counter/timer, and other internal circuits. A clock frequency, within the limits specified in the electrical specifications, must be supplied if the internal BRG is not used.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. Thirteen of these are available simultaneously for use by the receiver and transmitter. Eight are fixed, and one of two sets of five can be selected by programming ACR[7]. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The clock selectors allow the independent selection by the receiver and transmitter of any of these baud rates or an external timing signal.

The C/T operation is programmed by ACR[6:4]. One of eight timing sources can be used as the input to the C/T. The output of the C/T is available to the clock selectors and can be programmed by ACR[2:0} to be output on the MPO pin.

In the timer mode, the C/T generates a square wave whose period is twice the number of clock periods loaded into the C/T upper and lower registers. The counter ready bit in the ISR is set once each cycle of the square wave. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be affected. In this mode the C/T runs continuously and does not recognize the stop counter command (the command only resets the counter ready bit in the ISR). Receipt of a start C/T command causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR. Counting begins upon receipt of a start C/T command. Upon reaching terminal count, the counter ready bit in the ISR is set. The counter continues counting past the terminal count until stopped by the CPU. If MPO is programmed to be the output of the C/T, the output remains high until terminal count is reached, at which time it goes low. The output returns to the high state and the counter ready bit is cleared when the counter is stopped by a stop counter command. the CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command following a stop counter command. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower eight bits of the counter may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems

which may occur if a carry from the lower eight bits to the upper eight bits occurs between the times that both halves of the counter are read. However, a subsequent start counter command causes the counter to begin a new count cycle using the values in CTUR and CTLR.

Receiver and Transmitter

The UART is a full-duplex asynchronous receiver/transmitter. The operating frequency for the receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input. Registers associated with the communications channel are: the mode registers (MR1 and MR2), the clock select register (CSR), the command register (CR), the status register (SR), the transmit holding register (THR), and the receive holding register (RHR).

Transmitter

The transmitter accepts parallel data from the CPU and converts it to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains high and the TxEMT bit in the SR will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character in the THR. In the 16X clock mode, this also resynchronizes the internal 1X transmitter clock so that transmission of the new character begins with minimum delay.

The transmitter can be forced to send a break (continuous low condition) by issuing a start break command via the CR. The break is terminated by a stop break command.

If the transmitter is disabled, it continues operating until the character currently being transmitted and the character in the THR, if any, are completely sent out. Characters cannot be loaded in the THR while the transmitter is disabled.

Receiver

The receiver accepts serial data on the RxD pin, converts the serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition, and presents the assembled character to the CPU. The receiver looks for a high-to-low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled again each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled high, the start bit is invalid and the search for a valid start bit begins again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and the parity bit (if any) have been assembled, and one sop bit has been detected. The data is then transferred to the RHR and the RxRDY bit in the SR is set to a 1. If the character length is less than eight bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (i.e. framing error) and RxD remains low for one-half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point(one-half bit time after the stop bit was sampled).

The parity error, framing error and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set.

If a break condition is detected (RxD is low for the entire character including the stop bit), only one character consisting of all zeros will be loaded in the FIFO and the received break bit in the SR is set to 1. The RxD input must return to a high condition for two successive clock edges of the 1X clock (internal or external) before a search for the next start bit begins.

RECEIVER FIFO

The RHR consists of a first-in-first-out (FIFO) queue with a capacity of three characters. Data is loaded from the receive shift register into the top-most empty position of the FIFO. The RxRDY bit in the status register (SR) is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three queue positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are appended to each data character in the FIFO. Status can be provided in two ways, as programmed by the error mode control bit in mode register 1. In the character mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the block mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last reset error command was issued. In either mode, reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore, the SR should be read prior to reading the corresponding data character.

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

Receiver Reset and Disable

Receiver disable stops the receiver immediately – data being assembled if the receiver shift register is lost. Data and status in the FIFO is preserved and may be read. A re-enable of the receiver after a disable will cause the receiver to begin assembling characters at the next start bit detected. A receiver reset will discard the present shift register date, reset the receiver ready bit (RxRDY), clear the status of the byte at the top of the FIFO and re-align the FIFO read/write pointers. This has the appearance of "clearing or flushing" the receiver FIFO. In fact, the FIFO is NEVER cleared! The data in the FIFO remains valid until overwritten by another received character. Because of this erroneous reading, the FIFO will miss-align the FIFO pointers and result in the reading of previously read data. A receiver reset will re-align the pointers.

WAKE-UP MODE

In addition to the normal transmitter and receiver operation described above, the UART incorporates a special mode which provides automatic wake-up of the receiver through address frame recognition for multi-processor communications. This mode is selected by programming bits MR1[4:3] to '11'.

In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, whose receivers are normally disabled, examine the received data stream and 'wake-up' the CPU [by setting RxRDY) only upon receipt of an address character. The CPU

compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, an address/data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1[2]. MR1[2] = 0 transmits a zero in the A/D bit position which identifies the corresponding data bits as data, while MR1[2] = 1 transmits a one in the A/D bit position which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits in the THR.

While in this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character in the RHR FIFO if the received A/D bit is a one, but discards the received character if the received A/D bit is a zero. If enabled, all received characters are then transferred to the CPU via the RHR. In either case, the data bits are loaded in the data FIFO while the A/D bit is loaded in the status FIFO position normally used for parity error (SR[5]). Framing error, overrun error, and break detect operate normally whether or not the receiver is enabled.

MULTI-PURPOSE INPUT PIN

The MPI pin can be programmed as an input to one of several UART circuits. The function of the pin is selected by programming the appropriate control register (MR2[4]), ACR[6:4], CSR [7:4, 3:0]}. Only one of the functions may be selected at any given time. If CTS or GPI is selected, a change of state detector provided with the pin is activated. A high-to-low or low-to-high transition of the inputs lasting longer than 25–50µs sets the MPI change-of-state bit in the interrupt status register. The bit is cleared via a command. The change-of-state can be programmed to generate an interrupt to the CPU by setting the corresponding bit in the interrupt mask register.

The input port pulse detection circuitry uses a 38.4kHz sampling clock derived from one of the baud rate generator taps. This produces a sampling period of slightly more than 25µs (assuming a 3.6864MHz oscillator input). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs coincident with the first sample pulse. The 50µs time refers to the condition where the change of state is just missed and the first change of state is not detected until after an additional 25µs.

MULT-PURPOSE OUTPUT PIN

This pin can be programmed to serve as a request-to-send output, the counter/timer output, the output for the 1X or 16X transmitter or receiver clocks, the TxRDY output or the RxRDY/FFULL output (see ACR[2:0] – MPO Output Select).

REGISTERS

The operation of the UART is programmed by writing control words in the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. Addressing of the registers is as described in Table 1.

The contents of certain control registers are initialized to zero on reset (see RESET pin description). Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems. For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. The contents of the MR, the CSR, and the ACR should only be changed while the receiver and transmitter are disabled, and certain changes to the ACR should only be made while the C/T is stopped. The bit formats of the UART are shown in Table 3.

MR1 – Mode Register 1

MR1 is accessed when the MR pointer points to MR1. The pointer is set to MR1 by RESET or by a set pointer command applied via the CR. After reading or writing MR1, the pointers are set at MR2.

MR1[7] – Receiver Request-to-Send Control
The bit controls the deactivation of the RTSN output (MPO) by the receiver. This output is normally asserted and negated by commands applied via the command register. MR1[7] = 1 causes RTSN to be automatically negated upon receipt of a valid start bit if the receiver FIFO is full. RTSN is reasserted when an empty FIFO position is available. This feature can be used to prevent overrun in the receiver by using the RTSN output signal to control the CTS input of the transmitting device.

MR1[6] – Receiver Interrupt Select
This bit selects either the receiver ready status (RxRDY) or the FIFO full status (FFULL) to be used for CPU interrupts.

MR1[5] – Error Mode Select
This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break). In the character mode, status is provided on a character-by-character basis. The status applies only to the character at the top of the FIFO. In the block mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last reset error command was issued.

MR1[4:3] – Parity Mode Select
If with parity or force parity is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR![4:3] = 11 selects the channel to operate in the special wake-up mode.

MR1[2] – Parity Type Select
This bit selects the parity type (odd or even) if the with parity mode is programmed by MR1[4:3], and the polarity of the forced parity bit if the force parity mode is programmed. It has no effect if the no parity mode is programmed. In the special wake-up mode, it selects the polarity of the transmitted A/D bit.

MR1[1:0] – Bits Per Character Select
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2 – Mode Register 2

MR2 is accessed when the channel MR pointer points to MR2, which occurs after any access to MR1. Accesses to MR2 do not change the pointer.

MR2[7:6] – Mode Select
The UART can operate in one of four modes. MR2[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2[7:6] = 01 places the channel in the automatic echo mode, which automatically re-transmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is re-clocked and retransmitted on the TxD output.
2. The receive clock is used for the transmitter.

3. The receiver must be enabled, but the transmitter need not be enabled.
4. The TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU-to-receiver communication continues normally, but the CPU-to-transmitter link is disabled.

Two diagnostic modes can also be selected. MR2[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxD output is held high.
4. The RxD input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2[7:6] = 11. In this mode:

1. Received data is re-clocked and retransmitted on the TxD output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., the transmitted parity bit is as received.
5. The receiver must be enabled, but the transmitter need not be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

When switching in and out of the various modes, the selected mode is activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected, the device will switch out of the mode immediately. An exception to this is switching out of auto-echo or remote loopback modes; if the deselection occurs just after the receiver has sampled the stop bit (indicated in auto-echo by assertion o fRxRDY), and the transmitter is enabled, the transmitter is enabled, the transmitter will remain in auto-echo mode until one full stop bit has been retransmitted.

MR2[5] – Transmitter Request-to–Send Control

CAUTION: When the transmitter controls the OP pin (usually used for the RTSN signal) the meaning of the pin is not RTSN at all! Rather, it signals that the transmitter has finished the transmission (i.e., end of block).

This bit allows deactivation of the RTSN output by the transmitter. This output is manually asserted and negated by the appropriate commands issued via the command register. MR2[5] set to 1 caused the RTSN to be reset automatically one bit time after the character(s) in the transmit shift register and in the THR (if any) are completely transmitted (including the programmed number of stop bits) if a previously issued transmitter disable is pending. This feature can be used to automatically terminate the transmission as follows:

1. Program the auto-reset mode: MR2[5]=1
2. Enable transmitter, if not already enabled
3. Assert RTSN via command
4. Send message
5. After the last character of the message is loaded to the THR, disable the transmitter. (If the transmitter is underrun, a special case exists. See note below.)
6. The last character will be transmitted and the RTSN will be reset one bit time after the last stop bit is sent.

NOTE: The transmitter is in an underrun condition when both the TxRDY and the TxEMT bits are set. This condition also exists immediately after the transmitter is enabled from the disabled or reset state. When using the above procedure with the transmitter in the underrun condition, the issuing of the transmitter disable must be delayed from the loading of a single, or last, character until the TxRDY becomes active again after the character is loaded.

MR2[4] – Clear-to-Send Control

The sate of this bit determines if the CTSN input (MPI) controls the operation of the transmitter. If this bit is 0, CTSN has no effect on the transmitter. If this bit is a 1, the transmitter checks the sate of CTSN each time it is ready to send a character. If it is asserted (low), the character is transmitted. If it is negated (high), the TxD output remains in the marking state and the transmission is delayed until CTSN goes low. Changes in CTSN while a character is being transmitted do not affect the transmission of that character. This feature can be used to prevent overrun of a remote receiver.

MR2[3:0] – Stop Bit Length Select

This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1–9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1–1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a mark condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit if parity is enabled). If an external 1X clock is used for the transmitter, MR2[3] = 0 selects one stop bit and MR2[3] = 1 selects two stop bits to be transmitted.

CSR – Clock Select Register (see Table 5. also)

Table 2. Baud Rate Selection

CSR[3:0]/ [7:4]	ACR[7] = 0	ACR[7] = 1
0 0 0 0	50	75
0 0 0 1	110	110
0 0 1 0	134.5	134.5
0 0 1 1	200	150
0 1 0 0	300	300
0 1 0 1	600	600
0 1 1 0	1,200	1,200
0 1 1 1	1,050	2,000
1 0 0 0	2,400	2,400
1 0 0 1	4,800	4,800
1 0 1 0	7,200	1,800
1 0 1 1	9,600	9,600
1 1 0 0	38.4k	19.2k
1 1 0 1	Timer	Timer
1 1 1 0	MPI – 16X	MPI – 16X
1 1 1 1	MPI–1X	MPI–1X
The receiver clock is always a 16X clock, except for CSR[7:4] = 1111.		

CSR[7:4] – Receiver Clock Select

This field selects the baud rate clock for the receiver as shown in Table 2. The baud rates listed are for a 3.6864MHz crystal or external clock.

Table 3. Register Bit Formats

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MR1 (Mode Register 1)							
RxRTS Control	**RxINT Select**	**Error Mode**	**Parity Mode**		**Parity Type**	**Bits per Character**	
0 = no 1 = yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With parity 01 = Force parity 10 = No parity 11 = Special mode		0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8	
MR2 (Mode Register 2)							
Channel Mode		**TxRTS Control**	**CTS Enable Tx**	**Stop Bit Length***			
00 = Normal 01 = Auto echo 10 = Local loop 11 = Remote loop		0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 =1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000
NOTE: *Add 0.5 to values shown for 0–7 if channel is programmed for 5 bits/character.							
CSR (Clock Select Register)							
Receiver Clock Select				**Transmitter Clock Select**			
See Text				See Text			
CR (Command Register)							
Miscellaneous Commands				**Disable Tx**	**Enable Tx**	**Disable Rx**	**Enable Rx**
See Text				0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes
NOTE: Access to the miscellaneous commands should be separated by 3 X1 clock edges. A disabled transmitter cannot be loaded.							
SR (Channel Status Register)							
Received Break	**Framing Error**	**Parity Error**	**Overrun Error**	**TxEMT**	**TxRDY**	**FFULL**	**RxRDY**
0 = No 1 = Yes *	0 = No 1 = Yes *	0 = No 1 = Yes *	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes
NOTE: *These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits [7:5] from the top of the FIFO together with bits [4;0]. These bits are cleared by a reset error status command. In character mode they are reset when the corresponding data character is read from the FIFO.							
ACR (Auxiliary Control Register)							
BRG Set Select	**Counter/Timer Mode and Source**			**Power-Down Mode**	**MPO Pin Function Select**		
0 = Set 1 1 = Set 2	See Text			0 = On PWRDN Active 1 = Off Normal	000 = RTSN 001 = C/TO 010 = TxC (1X) 011 = TxC (16X)	100 = RxC (1X) 101 = RxC (16X) 110 = TxRDY 111 = RxRDY/FFULL	
ISR (Interrupt Status Register)							
MPI Pin Change	**MPI Pin Current State**	**Not used**	**Counter Ready**	**Delta Break**	**RxRDY/ FFULL**	**TxEMT**	**TxRDY**
0 = No 1 = Yes	0 = Low 1 = High		0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes
IMR (Interrupt Mask Resister)							
MPI Change Interrupt	**MPI Level Interrupt**	**Not used**	**Counter Ready Int**	**Delta Break Interrupt**	**RxRDY/FFULL Interrupt**	**TxEMT Interrupt**	**TxRDY Interrupt**
0 = Off 1 = On	0 = Off 1 = On		0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On
CTUR (Counter/Timer Upper Register)							
C/T[15]	**C/T[14]**	**C/T[13]**	**C/T[12]**	**C/T[11]**	**C/T[10]**	**C/T[9]**	**C/T[8]**

Table 3. Register Bit Formats (Continued)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CTLR (Counter/Timer Lower Register)							
C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]

CSR[3:0] – Transmitter Clock Select
This field selects the baud rate clock for the transmitter. The field definition is as shown in Table 2.

CR – Command Register

CR is used to write commands to the UART. Multiple commands can be specified in a single write to CR as long as the commands are non-conflicting, e.g., the enable transmitter and reset transmitter commands cannot be specified in a single command word.

CR[7:4] – Miscellaneous Commands
The encoded value of this field may be used to specify a single command as follows:

NOTE: Access to the upper four bits of the command register should be separated by three (3) edges of the X1 clock.

0000 No command.
0001 Reset MR pointer. Causes the MR pointer to point to MR1.
0010 Reset receiver. Resets the receiver as if a hardware reset had been applied. The receiver is disable and the FIFO is flushed.
0011 Reset transmitter. Resets the transmitter as if a hardware reset had been applied
0011 Reset error status. Clears the received break, parity error, framing error, and overrun error bits in the status register (SR[7:4]). Used in character mode to clear OE status (although RB, PE, and FE bits will also be cleared), and in block mode to clear all error status after a block of data has been received.
0101 Reset break change interrupt. Causes the break detect change bit in the interrupt status register (ISR[3]) to be cleared to zero.
0110 Start break. Forces the TxD output low (spacing). If the transmitter is empty, the start of the break condition will be delayed up to two bit times. If the transmitter is active, the break begins when transmission of the character is completed. If a character is in the THR, the start of break is delayed until that character or any others loaded after it have been transmitted (TxEMT must be true before break begins). The transmitter must be enabled to start a break
0111 Stop break. The TxD line will go high (marking) within two bit times. TxD will remain high for one bit time before the next character, if any, is transmitted.
1000 Start C/T. In counter or timer modes, causes the contents of CTUR/CTLR to be preset into the counter/timer and starts the counting cycle. In timer mode, any counting cycle in progress when the command is issued is terminated. In counter mode, has no effect unless a stop C/T command was issued previously.
1001 Stop counter. In counter mode, stops operation of the counter/timer, resets the counter ready bit in the ISR, and forces the MPO output high if it is programmed to be the output of the C/T. In timer mode, resets the counter ready bit in the ISR but has no effect on the counter/timer itself or on the MPO output.
1010 Assert RTSN. Causes the RTSN output (MPO) to be asserted (low).
1011 Negate RTSN.Causes the RTSN output (MPO) to be negated (high).
1100 Reset MPI change interrupt. Causes the MPI change bit in the interrupt status register (ISR[7]) to be cleared to zero.
1100 Reserved.
111x Reserved.

CR[3] – Disable Transmitter
This command terminates operation and resets the TxRDY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state. A disabled transmitter cannot be loaded.

CR[2] – Enable Transmitter
Enables operation of the channel A transmitter. The TxRDY status bit will be asserted.

CR[1] – Disable Receiver
This command terminates operation of the receiver immediately; a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special wake-up mode is programmed, the receiver operates even if it is disabled (see Wake-up Mode).

CR[0] – Enable Receiver
Enables operation of the receiver. If not in the special wake-up mode, this also forces the receiver into the search for start bit state.

SR – Channel Status Register

The status register is updated while RDN is negated. Therefore, the bus interface used with this device must not use a static RDN line. The RDN line must be pulsed to allow status register updates.

SR[7] – Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received; further entries to the FIFO are inhibited until the RxD line returns to the marking state for at least one half bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the change in break bit in the ISR (ISR[3]) is set. ISR[3] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry is capable of detecting breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must last until the end of the next character time in order for it to be detected.

SR[6] – Framing Error (FE)
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SR[5]– Parity Error (PE)
This bit is set when the with parity or force parity mode is programmed and the corresponding character in the FIFO was

received with incorrect parity. In special wake-up mode, the parity error bit stores the received A/D bit.

SR[4] – Overrun Error (OE)
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a reset error status command.

SR[3] – Transmitter Empty (TxEMT)
This bit will be set when the transmitter underruns, i.e., both the TxEMT and TxRDY bits are set. This bit and TxRDY are set when the transmitter is first enabled and at any time it is re-enabled after either (a) reset, or (b) the transmitter has assumed the disabled state. It is always set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission.

It is reset when the THR is loaded by the CPU, a pending transmitter disable is executed, the transmitter is reset, or the transmitter is disabled while in the underrun condition.

SR[2] – Transmitter Ready (TxRDY)
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, e.g., characters loaded in the THR while the transmitter is disabled will not be transmitted.

SR[1] – FIFO Full (FFULL)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the FIFO and there is no character in the receive shift register. If a character is waiting in the receive shift register because the FIFO is full, FFULL will be reset by the CPU read and then set by the transfer of the character to the FIFO, which causes all three FIFO positions to be occupied.

SR[0] – Receiver Ready (RxRDY)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR, and no more characters are in the FIFO.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates generated by the BRG.

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.

Set 2: 75, 110, 134.5, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, and 19.2k baud.

The selected set of rates is available for use by the receiver and transmitter. See Table 2 for characteristics of the BRG.

ACR[6:4] – Counter/Timer Mode and Clock Source Select
This field selects the operating mode of the counter/timer and its clock source as follows:

ACR [6:4]	Mode	Clock Source
0 0 0	Counter	MPI pin
0 0 1	Counter	MPI pin divided by 16 TxC–1X clock of the transmitter
0 1 0	Counter	Crystal or external clock (X1/CLK) divided by 16
0 1 1	Counter	MPI pin
1 0 0	Timer	MPI pin divided by 16
1 0 1	Timer	
1 1 0	Timer	Crystal or external clock (X1/CLK)
1 1 1	Timer	Crystal or external clock (X1/CLK) divided by 16

The timer mode generates a squarewave.

ACR[3] – Power-Down Mode Select
This bit, when set to zero, selects the power-down mode. In this mode, the SCC2691 oscillator is stopped and all functions requiring this clock are suspended. The contents of all registers are saved. It is recommended that the transmitter and receiver be disabled prior to placing the SCC2691 in this mode. Note that this bit must be set to a logic 1 after reset.

When the power-down mode is enabled, internal circuitry forces the X1/CLK pin to the low state and the X2 pin to the high state. If an external clock is being used to drive the device, it is recommended that the clock source be three-stated or forced low while the UART is in power-down mode in order to prevent the clock driver from being short circuited.

Table 4. BRG Characteristics

Crystal or Clock = 3.6864MHz

Nom Rate (Baud)	Actual 16X* Clock (kHz)	Error (%)
50	0.8	0
75	1.2	0
110	1.759	–0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	–0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2k	307.2	0
38.4k	614.4	0

*Duty cycle of 16X clock is 50% ±1%

ACR[2:0] – MPO Output Select
This field programs the MPO output pin to provide one of the following:

000 Request-to-send active-low output (RTSN). This output is asserted and negated via the command register. RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted out or when the receiver FIFO and receiver shift register are full using MR2[5] and MR1[7], respectively.

001 The counter/timer output. In the timer mode, this output is a square wave with a period of twice the value (in clock periods) of the contents of the CTUR and CTLR. In the counter mode, the output remains high until the terminal count is reached, at which time it goes low. The output returns to the high state when the counter is stopped by a stop counter command.

010 The 1X clock for the transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a non-synchronized 1X clock is output.

011 The 16X clock for the transmitter. This is the clock selected by CSR[3:0] = 1111.

100 The 1X clock for the receiver, which is the clock that samples the received data. If data is not being received, a non-synchronized 1X clock is output.

101 The 16X clock for the receiver. This is the clock selected by CSR[7:4], and is a 1X clock if CSR[7:4] = 1111.

110 The transmitter register empty signal, which is the complement of SR[2]. Active low output.

111 The receiver ready or FIFO full signal (complement of ISR[2]). Active-low output.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the interrupt mask register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output is asserted (low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR; the true status is provided regardless of the contents of the IMR. This register is cleared when the device is reset.

ISR[7] – MPI Change-of-State
This bit is set when a change-of-state occurs at the MPI input pin. It is reset by a reset change interrupt command.

ISR[6] – MPI Current State
This bit provides the current state of the MPI pin. This information is latched and reflects the state of the pin at the leading edge of the ISR ready cycle.

ISR[4] – Counter Ready
In the counter mode of operation, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.
In the timer mode, this bit is set once each cycle of the generated square wave (every other time the C/T reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the C/T.

ISR[3] – Change in Break
This bit, when set, indicates that the receiver has detected the beginning or end of a received break. It is reset when the CPU issues a reset break change interrupt command.

ISR[2] – Receiver Ready or FIFO Full
The function of this bit is programmed by MR1[6]. If programmed as receiver ready, it indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receiver FIFO. If the FIFO contains more characters, the bit will be set again after the FIFO is read. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the FIFO is read and there is no character in the receive shift register. If there is a character waiting in the receive shift register because the FIFO is full, the bit is set again when the waiting character is transferred into the FIFO.

ISR[1] – Transmitter Empty
This bit is a duplicate of TxEMT (SR[3]).

ISR[0] – Transmitter Ready
This bit is a duplicate of TxRDY (SR[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR cause an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is a '1', the INTRN output is asserted (low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask reading of the ISR. NOTE: When IMR[6] is a 1, a 1 on the MPI pin causes and interrupt.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded is H'0002'.

In the timer (programmable divider) mode, the C/T generates a square wave whose period is twice the value (in clock periods) of the CTUR and CTLR. The waveform so generated is often used for a data clock. The formula for calculating the divisor n to load to the CTUR and CTLR for a particular 1X data clock is shown below:

$$n = \frac{C/T\ Clock\ Frequency}{2\ x\ 16\ Baud\ rate\ desired}$$

Often this division will result in a non-integer number; 26.3, for example. One can only program integer numbers in a digital divider. Therefore, 26 would be chosen. This gives a baud rate error of 0.3/26.3 which is 1.14%; well within the ability asynchronous mode of operation.

If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be.

The counter ready status bit (ISR[4]) is set once each cycle of the square wave. The bit is reset by a stop counter command. The command, however, does not stop the C/T. The generated square wave is output on MPO if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded in CTUR and CTLR. Counting begins upon receipt of a start C/T command. Upon reaching the terminal count, the counter ready interrupt bit (ISR[4]) is set. the counter continues counting past the terminal count until stopped by the CPU. If MPO is programmed to be the output of the C/T, the output remains high until the terminal count is reached, at which time it goes low.

The output returns to the high state and ISR[4] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous values are preserved and used for the next count cycle.

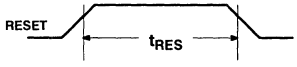


Figure 1. Reset Timing

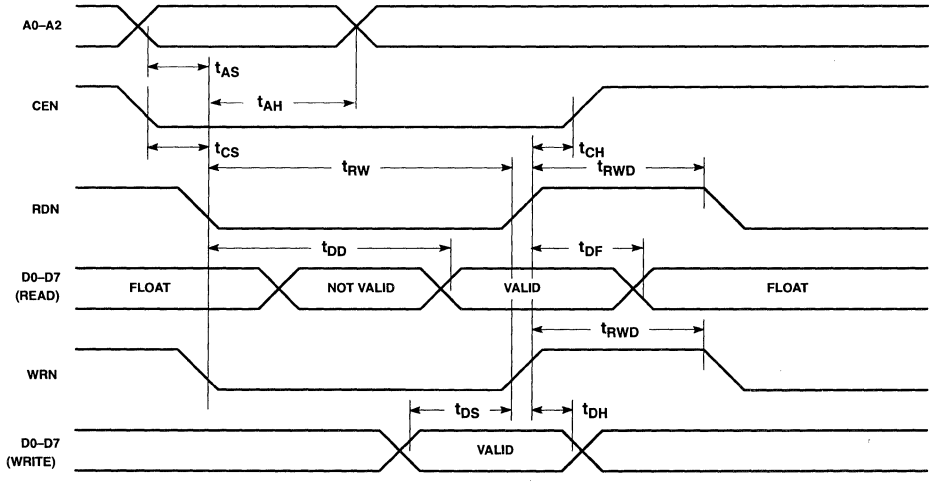


Figure 2. Bus Timing

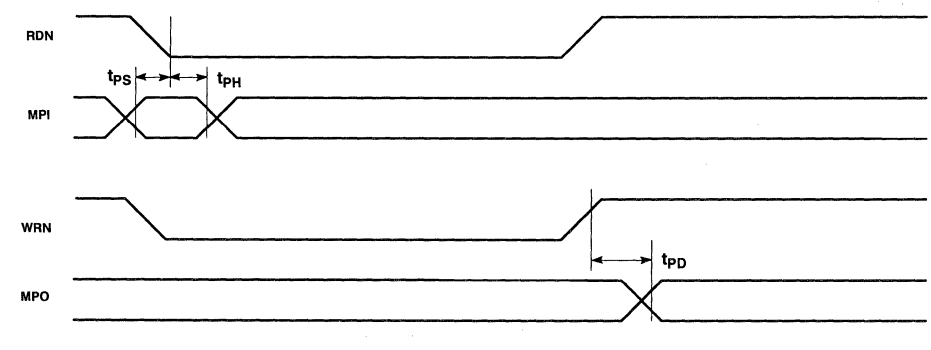
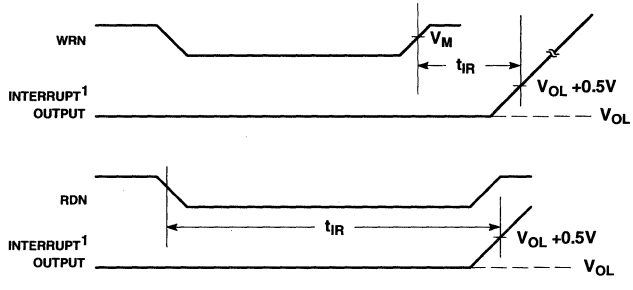


Figure 3. I/O Timing



NOTES:
1. INTRN or MPO when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, V_M, to a point 0.5V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 4. Interrupt Timing

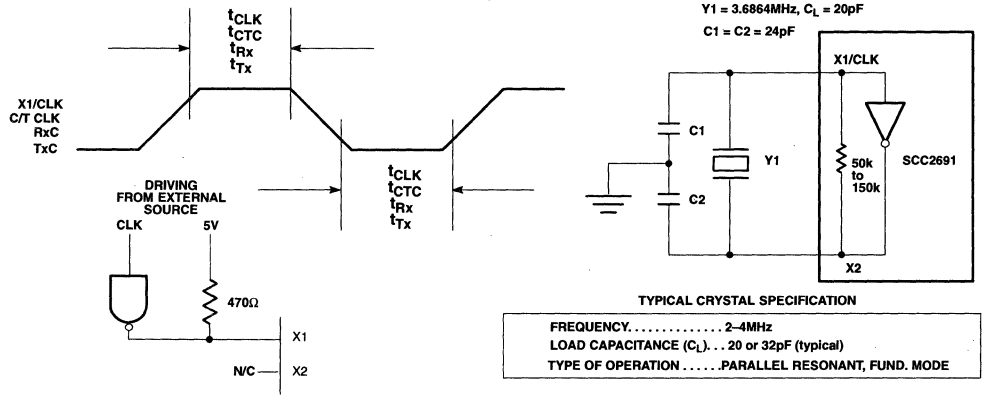


Figure 5. Clock Timing

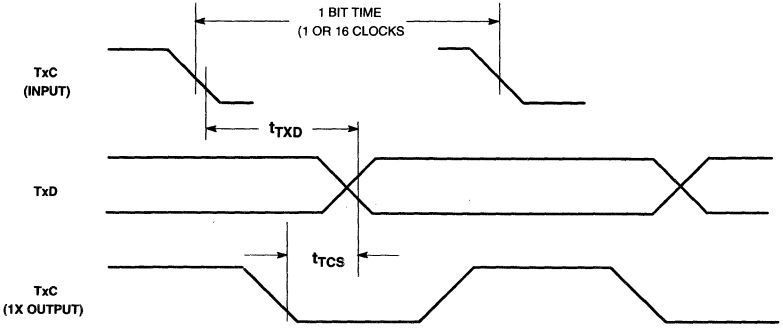


Figure 6. Transmit Timing

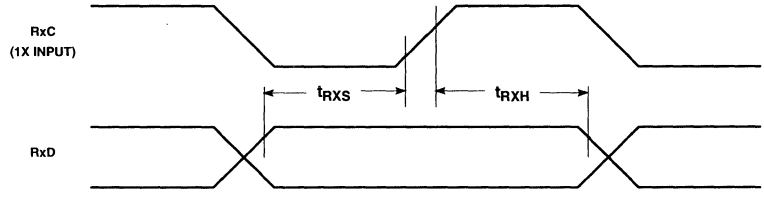
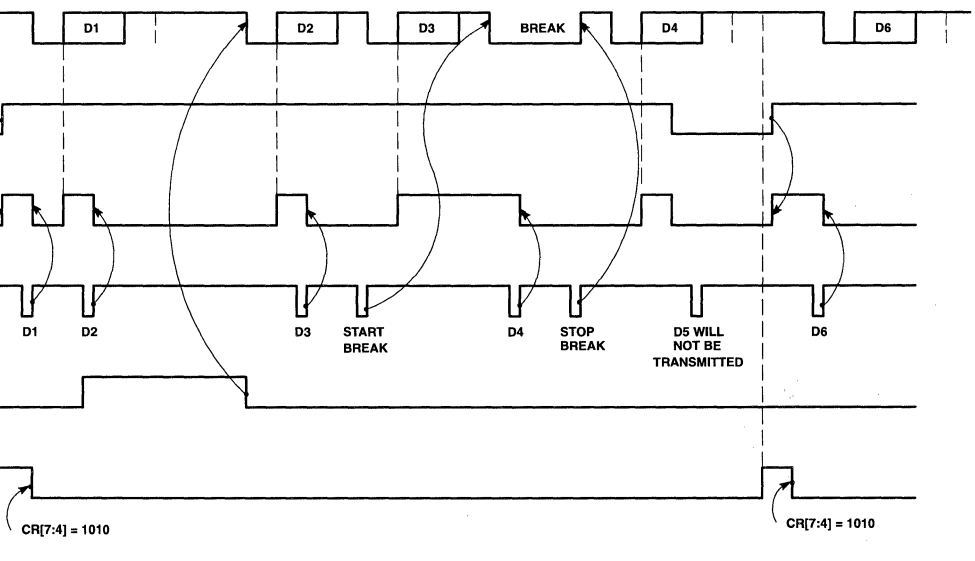


Figure 7. Receive Timing



NOTES:
1. TIMING SHOWN FOR MR2[4] = 1.
2. TIMING SHOWN FOR MR2[5] = 1.

Figure 8. Transmitter Timing

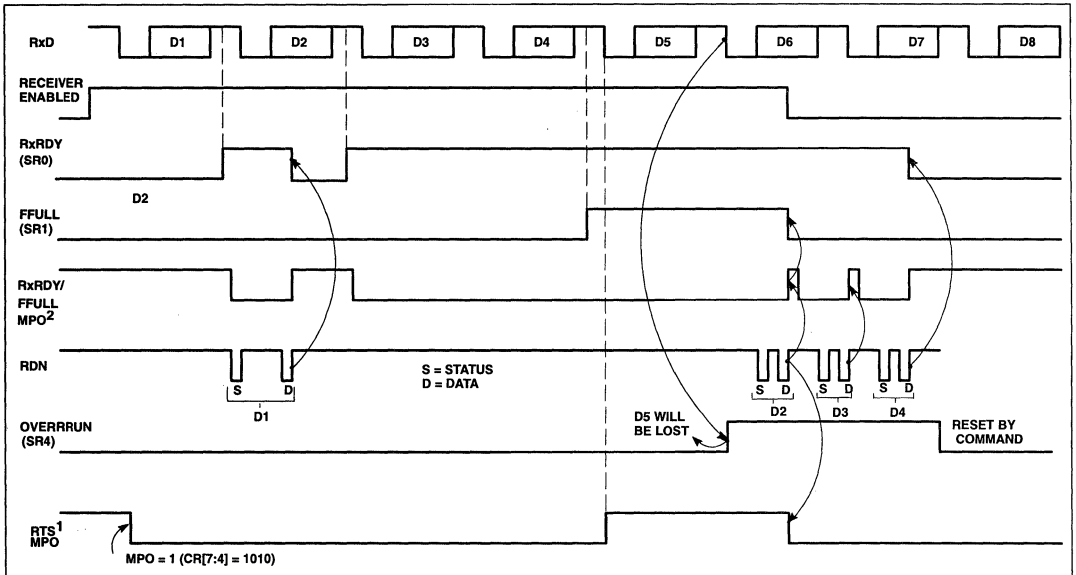


Figure 9. Receiver Timing

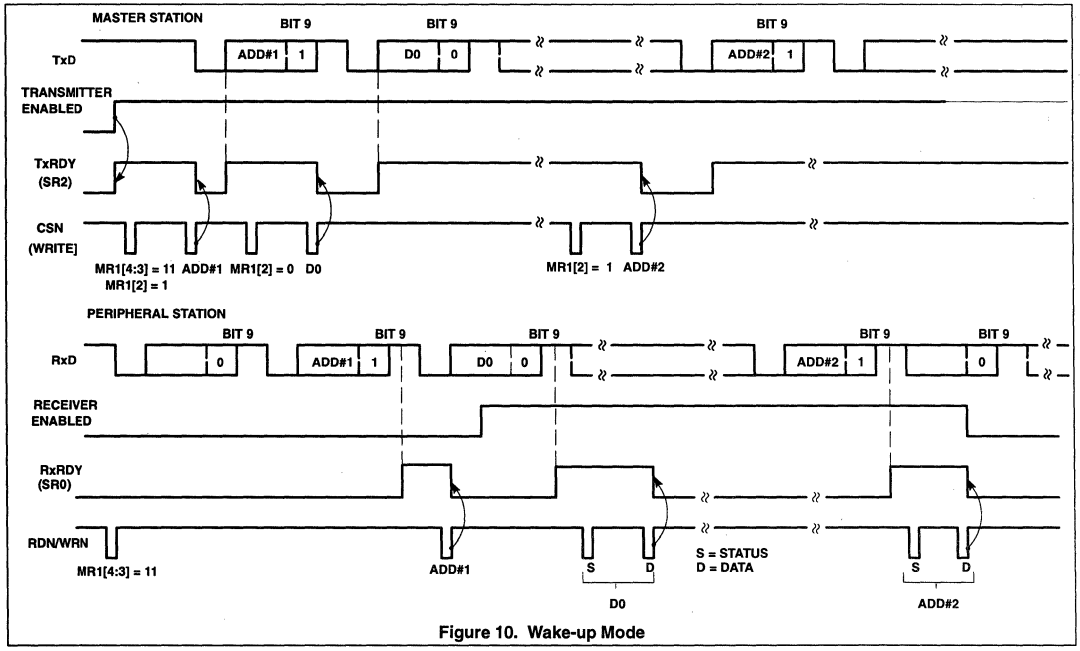


Figure 10. Wake-up Mode

The CTS, RTS, CTS Enable Tx signals

CTS (Clear To Send) is usually meant to be a signal to the transmitter meaning that it may transmit data to the receiver. The CTS input is on pin MPI. The CTS signal is active low; thus, it is called CTSN.

RTS is usually meant to be a signal from the receiver indicating that the receiver is ready to receive data. It is also active low and is, thus, called RTSN. RTSN is on pin MP0. A receiver's RTS output will usually be connected to the CTS input of the associated transmitter. Therefore, one could say that RTS and CTS are different ends of the same wire!

MR2(4) is the bit that allows the transmitter to be controlled by the CTS pin (MPI). When this bit is set to one AND the CTS input is driven high, the transmitter will stop sending data at the end of the present character being serialized. It is usually the RTS output of the receiver that will be connected to the transmitter's CTS input. The receiver will set RTS high when the receiver FIFO is full AND the start bit of the fourth character is sensed. Transmission then stops with four valid characters in the receiver. When MR2(4) is set to one, CTSN must be at zero for the transmitter to operate. If MR2(4) is set to zero, the MP pin will have no effect on the operation of the transmitter.

MR1(7) is the bit that allows the receiver to control MP0. When MP0 is controlled by the receiver, the meaning of that pin will be RTS. However, a point of confusion arises in that MP0 may also be controlled by the transmitter. When the transmitter is controlling this pin, its meaning is not RTS at all. It is, rather, that the transmitter has finished sending its last data byte. Programming the MP0 pin to be controlled by the receiver and the transmitter at the same time is allowed, but would usually be incompatible.

RTS can also be controlled by the commands 1010 and 1011 in the command register. RTS is expressed at the MP0 pin which is still an output port. Therefore, the state of MP0 should be set low (by commands to the CR register) for the receiver to generate the proper RTS signal. The logic at the output is basically a NAND of the MP0 bit register and the RTS signal as generated by the receiver. When the RTS flow control is selected via the MR(7) bit the state of the MP0 register is not changed. Terminating the use of "Flow Control" (via the MR registers) will return the MP0 pin to the control of the MP0 register.

Transmitter Disable Note

The sequence of instructions enable transmitter — load transmit holding register — disable transmitter will result in nothing being sent if the time between the end of loading the transmit holding register and the disable command is less that 3/16 bit time in the 16x mode or one bit time in the 1x mode. Also, if the transmitter, while in the enabled state and underrun condition, is immediately disabled after a single character is loaded to the transmit holding register, that character will not be sent.

In general, when it is desired to disable the transmitter before the last character is sent AND the TxEMT bit is set in the status register (TxEMT is always set if the transmitter has underrun or has just been enabled), be sure the TxRDY bit is active immediately before issuing the transmitter disable instruction. TxRDY sets at the end of the "start bit" time. It is during the start bit that the data in the transmit holding register is transferred to the transmit shift register.

Non-standard baud rates are available as shown in Table 5 below, via the BRG Test function.

Table 5. Baud Rates Extended

	Normal BRG		BRG Test	
CSR[7:4]	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0000	50	75	4,800	7,200
0001	110	110	880	880
0010	134.5	134.5	1,076	1,076
0011	200	150	19.2K	14.4K
0100	300	300	28.8K	28.8K
0101	600	600	57.6K	57.6K
0110	1,200	1,200	115.2K	115.2K
0111	1,050	2,000	1,050	2,000
1000	2,400	2,400	57.6K	57.6K
1001	4,800	4,800	4,800	4,800
1010	7,200	1,800	57.6K	14.4K
1011	9,600	9,600	9,600	9,600
1100	38.4K	19.2K	38.4K	19.2K
1101	Timer	Timer	Timer	Timer
1110	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X
1111	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X

NOTE:
Each read on address H'2' will toggle the baud rate test mode. When in the BRG test mode, the baud rates change as shown to the left. This change affects all receivers and transmitters on the DUART. Also, the RTSN output (MP0) become the transmitter 1x clock.

The test mode at address H'A' changes all transmitters and receivers to the 1x mode and connects the output ports to some internal nodes.

A condition that occurs infrequently has been observed where the receiver will ignore all data. It is caused by a corruption of the start bit generally due to noise. When this occurs the receiver will appear to be asleep or locked up. The receiver must be reset for the UART to continue to function properly.

Reset in the Normal Mode (Receiver Enabled)

Recovery can be accomplished easily by issuing a receiver software reset followed by a receiver enable. All receiver data, status and programming will be preserved and available before reset. The reset will NOT affect the programming.

Reset in the Wake-Up Mode (MR1[4:3] = 11)

Recovery can also be accomplished easily by first exiting the wake-up mode (MR1[4:3] = 00 or 01 or 10), then issuing a receiver software reset followed by a wake-up re-entry (MR1[4:3] = 11). All receiver data, status and programming will be preserved and available before reset. The reset will NOT affect the programming.

The receiver has a digital filter designed to reject "noisy" data and the receiver state machine was designed to reject noisy start bits or noise that might be considered a start bit. In spite of these precautions, corruption of the start bit can occur in 15ns window approximately 100ns prior to the rising edge of the data clock. The probability of this occurring is less than 10^{-5} at 9600 baud.

A corrupted start bit may have some deleterious effects in ASYNC operation if it occurs within a normal data block. The receiver will tend to align its data clock to the next '0' bit in the data stream, thus potentially corrupting the remainder of the data block. A good design practice, in environments where start bit corruption is possible, is to monitor data quality (framing error, parity error, break change and received break) and "data stopped" time out periods. Time out periods can be enabled using the counter/timer in the SCC2691, SCC2692, SCC2698B and SC68692 products. This monitoring can indicate a potential start bit corruption problem.

Dual asynchronous receiver/transmitter (DUART) SCC2692

DESCRIPTION

The Philips Semiconductors SCC2692 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruply buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the receiver buffer is full.

Also provided on the SCC2692 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The SCC2692 is available in three package versions: 40-pin and 28-pin, 0.6" wide, DIPs and a 44-pin PLCC.

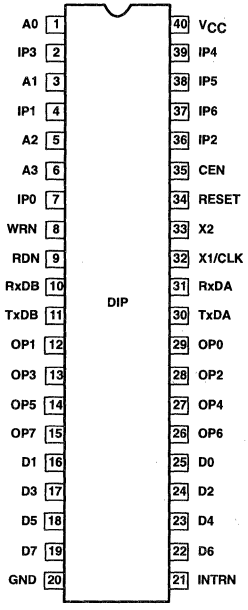
FEATURES

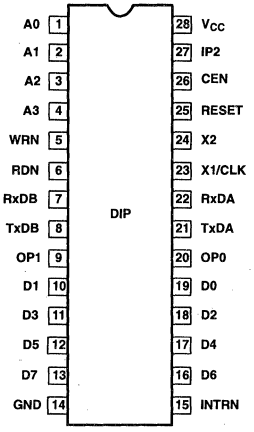
- Dual full-duplex asynchronous receiver/transmitters
- Quadruple buffered receiver data register
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - Non-standard rates to 115.2Kb
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
  - Multidrop mode (also called 'wake-up' or '9-bit')
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
  - Inputs have typically >100k pull-up resistors
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer rates: 1X – 1MB/sec, 16X – 125kB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Power down mode
- Receiver timeout mode
- Commercial and industrial temperature range versions
- TTL compatible
- Single +5V power supply

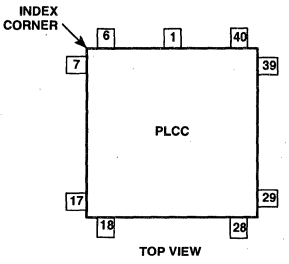
ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±10%, T_A = 0 to +70°C	V_{CC} = +5V ±10%, T_A = -40 to +85°C	DWG #
40-Pin Ceramic Dual In-Line Package (Cerdip)	SCC2692AC1F40	SCC2692AE1F40	0590B
28-Pin Ceramic Dual In-Line Package (Cerdip)	SCC2692AC1F28	SCC2692AE1F28	0589B
40-Pin Plastic Dual In-Line Package (DIP)	SCC2692AC1N40	SCC2692AE1N40	0415C
28-Pin Plastic Dual In-Line Package (DIP)	SCC2692AC1N28	SCC2692AE1N28	0413B
44-Pin Plastic Leaded Chip Carrier (PLCC) Package	SCC2692AC1A44	SCC2692AE1A44	0403G

PIN CONFIGURATIONS







PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A0	24	INTRN
3	IP3	25	D6
4	A1	26	D4
5	IP1	27	D2
6	A2	28	D0
7	A3	29	OP6
8	IP0	30	OP4
9	WRN	31	OP2
10	RDN	32	OP0
11	RXDB	33	TXDA
12	NC	34	NC
13	TXDB	35	RXDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CEN
18	D1	40	IP2
19	D3	41	IP6
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	V_{CC}

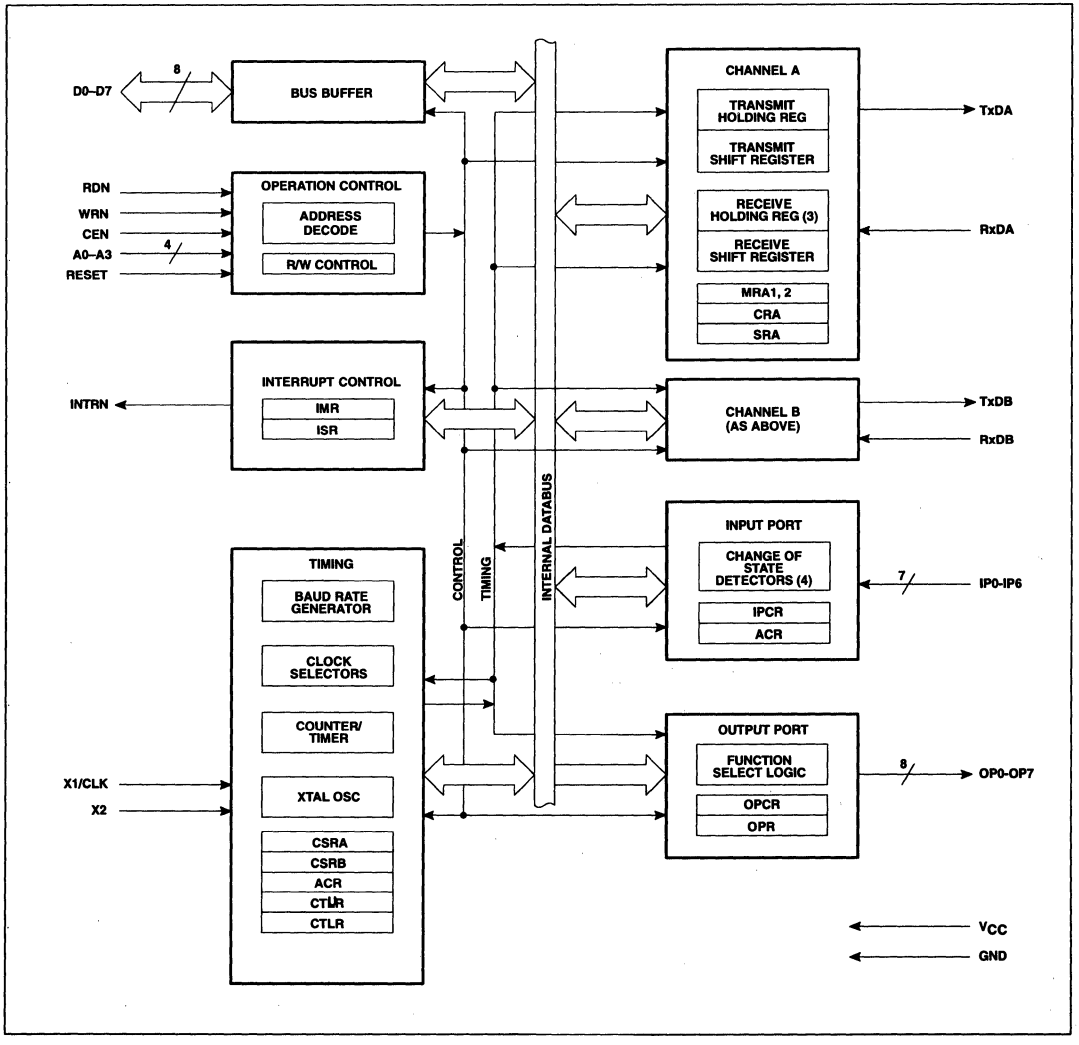
ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	Note 4	°C
T_{STG}	Storage temperature range	-65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	-0.5 to +7.0	V
V_S	Voltage from any pin to GND[3]	-0.5 to V_{CC} +0.5	V
P_D	Power dissipation	750	mW

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	APPLICABLE		TYPE	NAME AND FUNCTION
	40,44	28		
D0-D7	X	X	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	X	X	I	**Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A3 inputs. When High, places the D0-D7 lines in the 3-State condition.
WRN	X	X	I	**Write Strobe:** When Low and CEN is also Low, the contents of the data bus are loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	X	X	I	**Read Strobe:** When Low and CEN is also Low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0-A3	X	X	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	X	X	I	**Reset:** A High level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0-OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Resets Test modes, MR pointer set to MR1.
INTRN	X	X	O	**Interrupt Request:** Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	X	X	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5).
X2	X	X	I	**Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5). If X1/CLK is driven from an external source, this pin can be left open or connected to ground.
RxDA	X	X	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	X	X	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	X	X	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	X	X	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low.
OP0	X	X	O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	X	X	O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	X		O	**Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	X		O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	X		O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYAN/FFULLAN output.
OP5	X		O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYBN/FFULLBN output.
OP6	X		O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYAN output.
OP7	X		O	**Output 7:** General purpose output, or Channel B open-drain, active-Low, TxRDYBN output.
IP0	X		I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	X		I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	X	X	I	**Input 2:** General purpose input or counter/timer external clock input.
IP3	X		I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	X		I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	X		I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	X		I	**Input 6:** General purpose input or Channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	X	X	I	**Power Supply:** +5V supply input.
GND	X	X	I	**Ground**

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage					V
V_{IH}	Input high voltage (except X1/CLK)[6]		2.0		0.8	V
V_{IH}	Input high voltage (except X1/CLK)[7]		2.5			V
V_{IH}	Input high voltage (X1/CLK)		0.8 V_{CC}			V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}	Output high voltage (except OD outputs)[4]	I_{OH} = -400µA	V_{CC} -0.5			V
I_{IX1PD}	X1/CLK input current - power down	V_{IN} = 0 to V_{CC}	-10		+10	µA
I_{ILX1}	X1/CLK input low current - operating	V_{IN} = 0	-75		0	µA
I_{IHX1}	X1/CLK input high current - operating	V_{IN} = V_{CC}	0		75	µA
I_{OHX2}	X2 output high current - operating	V_{OUT} = V_{CC}, X1 = 0	0		+75	µA
I_{OHX2S}	X2 output high short circuit current - operating	V_{OUT} = 0, X1 = 0	-10		-1	mA
I_{OLX2}	X2 output low current - operating	V_{OUT} = 0, X1 = V_{CC}	-75		0	µA
I_{OLX2S}	X2 output low short circuit current - operating and power down	V_{OUT} = V_{CC}, X1 = V_{CC}	1		10	mA
I_I	Input leakage current:					
	All except input port pins	V_{IN} = 0 to V_{CC}	-10		+10	µA
	Input port pins	V_{IN} = 0 to V_{CC}	-20		+10	µA
I_{OZH}	Output off current high, 3-state data bus	V_{IN} = V_{CC}			10	µA
I_{OZL}	Output off current low, 3-state data bus	V_{IN} = 0V	-10			µA
I_{ODL}	Open-drain output low current in off-state	V_{IN} = 0	-10			µA
I_{ODH}	Open-drain output high current in off-state	V_{IN} = V_{CC}			10	µA
	Power supply current[5]					
	Operating mode	TTL input levels			10	mA
I_{CC}		CMOS input levels			10	mA
	Power down mode[8]	TTL input levels			3.0	mA
		CMOS input levels			2.0	mA

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7KΩ to V_{CC}.
5. All outputs are disconnected. Inputs are switching between TTL levels of 2.4V and 0.4V or CMOS levels of V_{CC} -0.2V and V_{SS} + 0.2V.
6. $T_A \geq 0°C$
7. $T_A < 0°C$
8. See UART application note for 5µA.

AC CHARACTERISTICS[1, 2, 4]

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ[3]	Max	
Reset Timing (See Figure 1)					
t_{RES}	RESET pulse width	200			ns
Bus Timing[5] (See Figure 2)					
t_{AS}	A0-A3 setup time to RDN, WRN Low	10			ns
t_{AH}	A0-A3 hold time from RDN, WRN Low	100			ns
t_{CS}	CEN setup time to RDN, WRN Low	0			ns
t_{CH}	CEN hold time from RDN, WRN High	0			ns
t_{RW}	WRN, RDN pulse width	225			ns
t_{DD}	Data valid after RDN Low			175	ns
t_{DA}	RDN Low to data bus active[7]	15			ns
t_{DF}	Data bus floating after RDN High			125	ns
t_{DI}	RDN High to data bus invalid[7]	20			ns
t_{DS}	Data setup time before WRN High	100			ns
t_{DH}	Data hold time after WRN High	20			ns
t_{RWD}	High time between reads and/or writes[5, 6]	200			ns

AC CHARACTERISTICS (Continued)[1, 2, 4]

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ[3]	Max	
Port Timing[5] (See Figure 3)					
t_{PS}	Port input setup time before RDN Low	0			ns
t_{PH}	Port input hold time after RDN High	0			ns
t_{PD}	OP_n output valid from WRN High			400	ns
Interrupt Timing (See Figure 4)					
t_{IR}	INTRN (or OP3-OP7 when used as interrupts) negated from:				
	Read RHR (RxRDY/FFULL interrupt)			300[9]	ns
	Write THR (TxRDY interrupt)			300[9]	ns
	Reset command (break change interrupt)			300[9]	ns
	Stop C/T command (counter interrupt)			300[9]	ns
	Read IPCR (input port change interrupt)			300[9]	ns
	Write IMR (clear of interrupt mask bit)			300[9]	ns
Clock Timing (See Figure 5)					
t_{CLK}	X1/CLK High or Low time	100			ns
f_{CLK}	X1/CLK frequency[10]	0	3.6864	4	MHz
t_{CTC}	CTCLK (IP2) High or Low time	100			ns
f_{CTC}	CTCLK (IP2) frequency[8]	0		4	MHz
t_{RX}	RxC High or Low time	220			ns
f_{RX}	RxC frequency (16X)[8]	0		2	MHz
	(1X)[8]	0		1	MHz
t_{TX}	TxC High or Low time	220			ns
f_{TX}	TxC frequency (16X)[8]	0		2	MHz
	(1X)[8]	0		1	MHz
Transmitter Timing (See Figure 6)					
t_{TXD}	TxD output delay from TxC Low (TxC input pin)			350	ns
t_{TCS}	Output delay from TxC Low to TxD data output (TxC 1x output pin)	0		150	ns
Receiver Timing (See Figure 7)					
t_{RXS}	RxD data setup time to RxC High	240			ns
t_{RXH}	RxD data hold time from RxC High	200			ns

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7KΩ to V_{CC}.
5. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ORed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
6. If CEN is used as the 'strobing' input, the parameter defines the minimum High times between one CEN and the next. The RDN signal must be negated for t_{RWD} to guarantee that any status register changes are valid.
7. Guaranteed by characterization of sample units.
8. Minimum frequencies are not tested but are guaranteed by design.
9. 325ns maximum for T_A > 70°C.
10. Operation to 0MHz is assured by design. Minimum test frequency is 2.0MHz.

BLOCK DIAGRAM

The SCC2692 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the Block Diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer.

Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register

(IMR) and the Interrupt Status Register (ISR). The IMR can be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions.

Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

If an external clock is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 5.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. A 3.6864MHz crystal or external clock must be used to get the standard baud rate. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the SCC2692 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

Input Port

The inputs to this unlatched 7-bit port can be read by the CPU by performing a read operation at address H'D'. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always read as a logic 1. The pins of this port can also serve as auxiliary inputs to certain portions of the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs, lasting longer than 25 - 50µs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

The input port pulse detection circuitry uses a 38.4KHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (this assumes that the clock input is 3.6864MHz). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs "coincident with the first sample pulse". The 50µs time refers to the situation in which the change-of-state is "just missed" and the first change-of-state is not detected until 25µs later.

Output Port

The output port pins may be controlled by the OPR, OPCR, MR and CR registers. Via appropriate programming they may be just another parallel port to external circuits, or they may represent many internal conditions of the UART. When this 8-bit port is used as a general purpose output, the pins so defined will assume the compliment of the associated bit in the Output Port Register (OPR). OPR(n) = 1 results in OP(n) = Low and vice versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address H'E' with the accompanying data specifying the bits to be reset (1 = set, 0 = no change). Likewise, a bit is reset by a write at address H'F' with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also individually assigned specific functions by appropriate programming of the Channel A mode registers (MR1A, MR2A), the Channel B mode registers (MR1B, MR2B), and the Output Port Configuration Register (OPCR).

Output ports are driven high on hardware reset.

OPERATION

Transmitter

The SCC2692 is conditioned to transmit data when the transmitter is enabled through the command register. The SCC2692 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When a character is loaded into the Transmit Holding Register (THR), the above conditions are negated. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again which means one full character time of buffering is provided. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR.

If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enable, the CTSN input must be Low in order for the character to be transmitted. If it goes High in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes Low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

Receiver

The SCC2692 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive Holding Register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one-half bit time before a search for the next start bit begins.

Receiver FIFO

The RHR consists of a First-In-First-Out (FIFO) stack with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4] will be set-upon receipt of the start bit of the new (overrunning) character.

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

Receiver Reset and Disable

Receiver disable stops the receiver immediately – data being assembled if the receiver shift register is lost. Data and status in the FIFO is preserved and may be read. A re-enable of the receiver after a disable will cause the receiver to begin assembling characters at the next start bit detected. A receiver reset will discard the present shift register date, reset the receiver ready bit (RxRDY), clear the status of the byte at the top of the FIFO and re-align the FIFO read/write pointers. This has the appearance of "clearing or flushing" the receiver FIFO. In fact, the FIFO is NEVER cleared! The data in the FIFO remains valid until overwritten by another received character. Because of this erroneous reading, the FIFO will miss-align the FIFO pointers and result in the reading of previously read data. A receiver reset will re-align the pointers.

Receiver Timeout Mode

The timeout mode uses the received data stream to control the counter/timer. Each time a received character is transferred from the shift register to the RHR, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know there is data left in the FIFO. The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

The timeout mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. The timeout mode should only be used by one channel at once, since it uses the C/T. CTU and CTL must be loaded with a value greater than the normal receive character period. The timeout mode disables the regular START/STOP

Table 1. SCC2692 Register Addressing

A3	A2	A1	A0	READ (RDN = 0)	WRITE (WRN = 0)
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	BRG Test	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
0	1	0	0	Input Port Change Register (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Register (CRUR)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	1X/16X Test	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
1	1	0	0	Reserved	Reserved
1	1	0	1	Input Port (IPR)	Output Port Conf. Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

Counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RHR, the C/T is stopped after 1 C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Since receiving a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx = 'Ax', will also clear the counter ready bit and stop the counter until the next character is received.

Multidrop Mode

The DUART is equipped with a receiver wake-up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wake-up' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems.

For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1X by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1X, switches the pointer to MR2X. The pointer then remains at MR2X, so that subsequent accesses are always to MR2X unless the pointer is reset to MR1X as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'OA' should never be read during normal operation since they are reserved for internal diagnostics.

MR1A – Channel A Mode Register 1

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7] – Channel A Receiver Request-to-Send Control

This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the Channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the

RTSAN output signal to control the CTSN input of the transmitting device.

MR1A[6] – Channel A Receiver Interrupt Select
This bit selects either the Channel A receiver ready status (RxRDY) or the Channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

MR1A[5] – Channel A Error Mode Select
This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

MR1A[4:3] – Channel A Parity Mode Select
If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] = 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] – Channel A Parity Type Select
This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] – Channel A Bits Per Character Select
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] – Channel A Mode Select
Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically re-transmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is re-clocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is re-clocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been re-transmitted.

MR2A[5] – Channel A Transmitter Request-to-Send Control
CAUTION: When the transmitter controls the OP pin (usually used for the RTSN signal) the meaning of the pin is not RTSN at all! Rather, it signals that the transmitter has finished the transmission (i.e., end of block).

This bit allows deactivation of the RTSN output by the transmitter. This output is manually asserted and negated by the appropriate commands issued via the command register. MR2[5] set to 1 caused the RTSN to be reset automatically one bit time after the character(s) in the transmit shift register and in the THR (if any) are completely transmitted (including the programmed number of stop bits) if a previously issued transmitter disable is pending. This feature can be used to automatically terminate the transmission as follows:

1. Program the auto-reset mode: MR2[5]=1

2. Enable transmitter, if not already enabled
3. Assert RTSN via command
4. Send message
5. After the last character of the message is loaded to the THR, disable the transmitter. (If the transmitter is underrun, a special case exists. See note below.)
6. The last character will be transmitted and the RTSN will be reset one bit time after the last stop bit is sent.

NOTE: The transmitter is in an underrun condition when both the TxRDY and the TxEMT bits are set. This condition also exists immediately after the transmitter is enabled from the disabled or reset state. When using the above procedure with the transmitter in the underrun condition, the issuing of the transmitter disable must be delayed from the loading of a single, or last, character until the TxRDY becomes active again after the character is loaded.

MR2A[4] – Channel A Clear-to-Send Control
If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IPO) each time it is ready to send a character. If IPO is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character..

MR2A[3:0] – Channel A Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit is enabled).

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

Table 2. Register Bit Formats

	BIT 7	BIT 6	BIT 5	BIT 4 BIT 3	BIT 2	BIT 1 BIT 0
MR1A MR1B	RxRTS CONTROL	RxINT SELECT	ERROR MODE	PARITY MODE	PARITY TYPE	BITS PER CHARACTER
	0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multidrop Mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

	BIT 7 BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MR2A MR2B	CHANNEL MODE	TxRTS CONTROL	CTS ENABLE Tx	STOP BIT LENGTH*			
	00 = Normal 01 = Auto-Echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000
NOTE: *Add 0.5 to values shown for 0 – 7 if channel is programmed for 5 bits/char.							

	BIT 7 BIT 6 BIT 5 BIT 4	BIT 3 BIT 2 BIT 1 BIT 0
CSRA CSRB	RECEIVER CLOCK SELECT	TRANSMITTER CLOCK SELECT
	See Text	See Text

	BIT 7 BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CRA CRB	MISCELLANEOUS COMMANDS	DISABLE Tx	ENABLE Tx	DISABLE Rx	ENABLE Rx
	See Text and Timing Requirement	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes
NOTE: Access to the miscellaneous commands should be separated by 3 X1 clock edges. A disabled transmitter cannot be loaded.					

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SRA SRB	RECEIVED BREAK*	FRAMING ERROR*	PARITY ERROR*	OVERRUN ERROR	TxEMT	TxRDY	FFULL	RxRDY
	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes
NOTE: *These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.								

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3 BIT 2	BIT 1 BIT 0
	OP7	OP6	OP5	OP4	OP3	OP2
OPCR	0 = OPR[7] 1 = TxRDYB	0 = OPR[6] 1 = TxRDYA	0 = OPR[5] 1 = RxRDY/ FFULLB	0 = OPR[4] 1 = RxRDY/ FFULLA	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1X) 11 = RxCB(1X)	00 = OPR[2] 01 = TxCA(16X) 10 = TxCA(1X) 11 = RxCA(1X)

	BIT 7	BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ACR	BRG SET SELECT	COUNTER/TIMER MODE AND SOURCE	DELTA IP 3 INT	DELTA IP 2 INT	DELTA IP 1 INT	DELTA IP 0 INT
	0 = set 1 1 = set 2	See Table 4	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IPCR	DELTA IP 3	DELTA IP 2	DELTA IP 1	DELTA IP 0	IP 3	IP 2	IP 1	IP 0
	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ISR	INPUT PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	COUNTER READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA
	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IMR	IN. PORT CHANGE INT	DELTA BREAK B INT	RxRDY/ FFULLB INT	TxRDYB INT	COUNTER READY INT	DELTA BREAK A INT	RxRDY/ FFULLA INT	TxRDYA INT
	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CTUR	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CTLR	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]

MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

CSRA – Channel A Clock Select Register

CSRA[7:4] – Channel A Receiver Clock Select

This field selects the baud rate clock for the Channel A transmitter. The field definition is shown in Table 3.

CSRA[3:0] – Channel A Transmitter Clock Select

This field selects the baud rate clock for the Channel A transmitter. The field definition is as shown in Table 3, except as follows:

CSRA[3:0]	ACR[7] = 0	ACR[7] = 1
1110	IP3-16X	IP3-16X
1111	IP3-1X	IP3-1X

The transmitter clock is always a 16X clock except for CSRA[3:0] = 1111.

Table 3. Baud Rate

CSRA[7:4]	ACR[7] = 0	ACR[7] = 1
0000	50	75
0001	110	110
0010	134.5	134.5
0011	200	150
0100	300	300
0101	600	600
0110	1,200	1,200
0111	1,050	2,000
1000	2,400	2,400
1001	4,800	4,800
1010	7,200	1,800
1011	9,600	9,600
1100	38.4K	19.2K
1101	Timer	Timer
1110	IP4-16X	IP4-16X
1111	IP4-1X	IP4-1X

NOTE: The receiver clock is always a 16X clock except for CSRA[7:4] = 1111. Also, see Table 6 for baud rates available in BRG Test.

CSRB – Channel B Clock Select Register

CSRB[7:4] – Channel B Receiver Clock Select
This field selects the baud rate clock for the Channel B receiver. The field definition is as shown in Table 3, except as follows:

CSRB[7:4]	ACR[7] = 0	ACR[7] = 1
1110	IP6-16X	IP6-16X
1111	IP6-1X	IP6-1X

The receiver clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0] – Channel B Transmitter Clock Select
This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

CSRB[3:0]	ACR[7] = 0	ACR[7] = 1
1110	IP5-16X	IP5-16X
1111	IP5-1X	IP5-1X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

CRA[7:4] – Miscellaneous Commands
Sequential writes to CR(7:4) should be separated by three edges of the X1 clock.

The encoded value of this field may be used to specify a single command as follows:

0000 No command.
0001 Reset MR pointer. Causes the Channel A MR pointer to point to MR1.
0010 Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.
0011 Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.
0100 Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.
0101 Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.
0110 Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.
0111 Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.
1000 Assert RTSN. Causes the RTSN output to be asserted (Low).
1001 Negate RTSN. Causes the RTSN output to be negated (High).
1010 Set Timeout Mode On. The receiver in this channel will restart the C/T as each receive character is transferred from the shift register to the RHR. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset. The counter will not start until the first character is received after the command is issued.
1011 Not used.
1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued to reset the ISR(3) bit.
1101 Not used.
1110 Power Down Mode On. In this mode, the DUART oscillator is stopped and all functions requiring this clock are suspended. The execution of commands other than disable power down mode (1111) requires a X1/CLK. While in the power down mode, do not issue any commands to the CR except the disable power down mode command. The contents of all registers will be saved while in this mode. It is recommended that the transmitter and receiver be disabled prior to placing the DUART into power down mode. This command is in CRA only.
1111 Disable Power Down Mode. This command restarts the oscillator. After invoking this command, wait for the oscillator to start up before writing further commands to the CR. This command is in CRA only.

CRA[3] – Disable Channel A Transmitter
This command terminates transmitter operation and resets the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2] – Enable Channel A Transmitter
Enables operation of the Channel A transmitter. The TxRDY status bit will be asserted.

CRA[1] – Disable Channel A Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the

special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] – Enable Channel A Receiver
Enables operation of the Channel A receiver. If not in the special wake-up mode, this also forces the receiver into the search for start bit state.

CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, with the exception of commands "Ex" and "Fx" which are used for power downmode. These two commands are not used in CRB. All other control actions that apply to CRA also apply to CRB.

SRA – Channel A Status Register

SRA[7] – Channel A Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line to the marking state for at least one-half a bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

SRA[6] – Channel A Framing Error
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SRA[5] – Channel A Parity Error
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multidrop mode the parity error bit stores the receive A/D bit.

SRA[4] – Channel A Overrun Error
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a 'reset error status' command.

SRA[3] – Channel A Transmitter Empty (TxEMTA)
This bit will be set when the transmitter underruns, i.e., both the TxEMT and TxRDY bits are set. This bit and TxRDY are set when the transmitter is first enabled and at any time it is re-enabled after either (a) reset, or (b) the transmitter has assumed the disabled state. It is always set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission.

It is reset when the THR is loaded by the CPU, a pending transmitter disable is executed, the transmitter is reset, or the transmitter is disabled while in the underrun condition.

SRA[2] – Channel A Transmitter Ready (TxRDYA)
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, e.g., characters loaded into the THR while the transmitter is disabled will not be transmitted.

SRA[1] – Channel A FIFO Full (FFULLA)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SRA[0] – Channel A Receiver Ready (RxRDYA)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift to the FIFO and reset when the CPU reads the RHR, if after this read there are not more characters still in the FIFO.

SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR – Output Port Configuration Register

OPCR[7] – OP7 Output Select
This bit programs the OP7 output to provide one of the following:
0 The complement of OPR[7].
1 The Channel B transmitter interrupt output which is the complement of TxRDYB. When in this mode OP7 acts as an open- drain output. Note that this output is not masked by the contents of the IMR.

OPCR[6] – OP6 Output Select
This bit programs the OP6 output to provide one of the following:
0 The complement of OPR[6].
1 The Channel A transmitter interrupt output which is the complement of TxRDYA. When in this mode OP6 acts as an open- drain output. Note that this output is not masked by the contents of the IMR.

OPCR[5] – OP5 Output Select
This bit programs the OP5 output to provide one of the following:
0 The complement of OPR[5].
1 The Channel B transmitter interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[4] – OP4 Output Select
This field programs the OP4 output to provide one of the following:
0 The complement of OPR[4].

1 The Channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] – OP3 Output Select
This bit programs the OP3 output to provide one of the following:
00 The complement of OPR[3].
01 The counter/timer output, in which case OP3 acts as an open-drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
10 The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
11 The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] – OP2 Output Select
This field programs the OP2 output to provide one of the following:
00 The complement of OPR[2].
01 The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
10 The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
11 The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates to be generated by the BRG:

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05K, 1.2K, 2.4K, 4.8K, 7.2K, 9.6K, and 38.4K baud.
Set 2: 75, 110, 134.5, 150, 300, 600, 1.2K, 1.8K, 2.0K, 2.4K, 4.8K, 9.6K, and 19.2K baud.

Table 4. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz

BAUD RATE	ACTUAL 16X CLOCK (kHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2K	307.2	0
38.4K	614.4	0

NOTE: Duty cycle of 16X clock is 50% ±1%.

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 4.

ACR[6:4] – Counter/Timer Mode And Clock Source Select
This field selects the operating mode of the counter/timer and its clock source as shown in Table 5.

ACR[3:0] – IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

Table 5. ACR 6:4 Field Definition

ACR 6:4	MODE	CLOCK SOURCE
000	Counter	External (IP2)
001	Counter	TxCA – 1X clock of Channel A transmitter
010	Counter	TxCB – 1X clock of Channel B transmitter
011	Counter	Crystal or IP2 clock (X1/CLK) divided by 16
100	Timer	External (IP2) divided by 16
101	Timer	Crystal or external clock (X1/CLK)
110	Timer	Crystal or IP2 clock (X1/CLK) divided by 16
111	Timer	

NOTE: Timer mode generates a squarewave.

IPCR – Input Port Change Register

IPCR[7:4] – IP3, IP2, IP1, IP0 Change-of-State
These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – IP3, IP2, IP1, IP0 Change-of-State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to 00_{16} when the DUART is reset.

ISR[7] – Input Port Change Status
This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] – Channel B Change In Break
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset

when the CPU issues a Channel B 'reset break change interrupt' command.

ISR[5] – Channel B Receiver Ready or FIFO Full
The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in Channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel B FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[4] – Channel B Transmitter Ready
This bit is a duplicate of TxRDYB (SRB[2]).

ISR[3] – Counter Ready.
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] – Channel A Change in Break
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

ISR[1] – Channel A Receiver Ready Or FIFO Full
The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in Channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel A FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the ISR[0] and IMR waiting character is loaded into the FIFO.

ISR[0] – Channel A Transmitter Ready
This bit is a duplicate of TxRDYA (SRA[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3-OP7 or the reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. The waveform so generated is often used for a data clock. The formula for calculating the divisor n to load to the CTUR and CTLR for a particular 1X data clock is shown below:

$$n = \frac{C/T\ clock\ Frequency}{2 \cdot 16 \cdot Baud\ rate\ desired}$$

Often this division will result in a non-integer number; 26.3, for example. One can only program integer numbers in a digital divider. Therefore, 26 would be chosen. This gives a baud rate error of 0.3/26.3 which is 1.14%; well within the ability asynchronous mode of operation.

If the value in CTUR and CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read at address A3-A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a start counter command (read with A3-A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3-A0 = H'F'). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

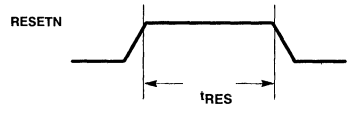


Figure 1. Reset Timing

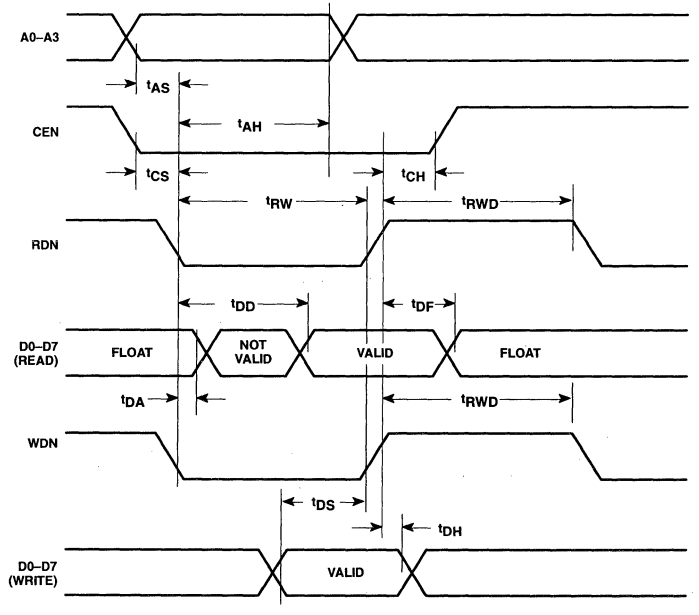


Figure 2. Bus Timing

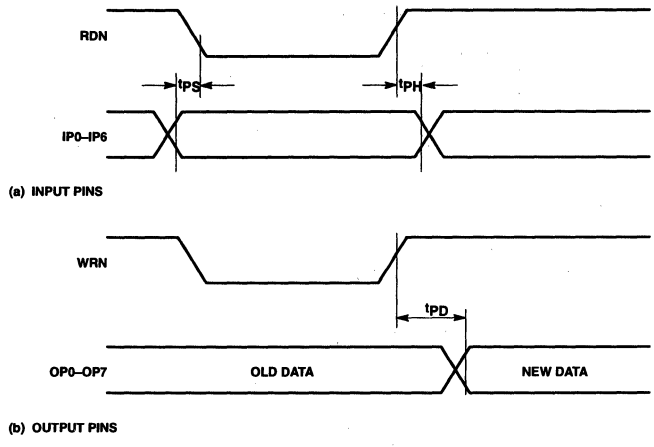
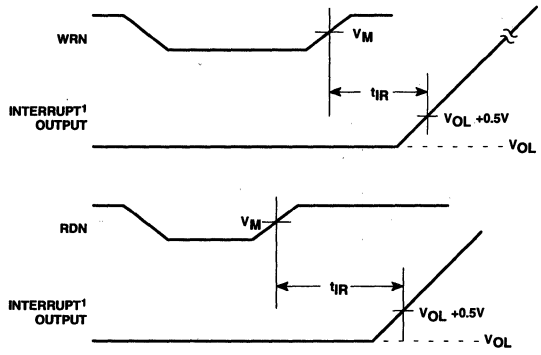
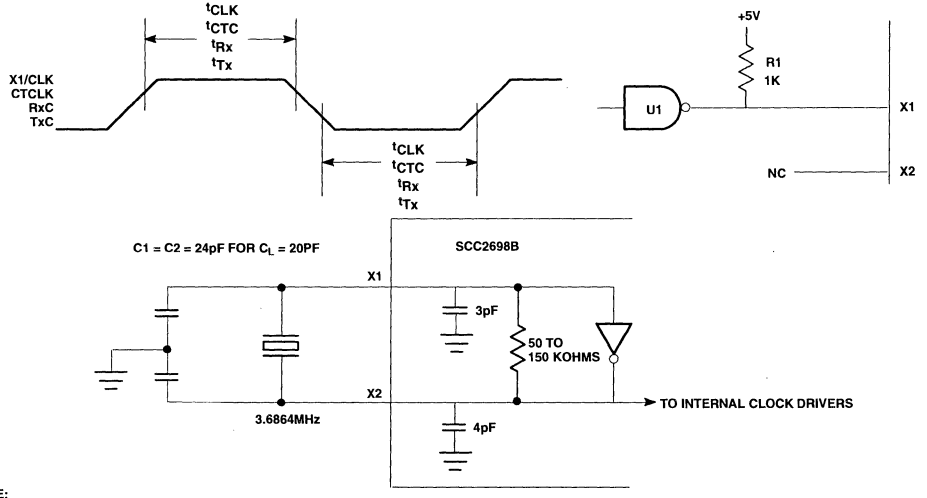


Figure 3. Port Timing



NOTES:
1. INTRN or OP3-OP7 when used as interrupt outputs.
2. The test for open-drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, V_M, to a point 0.5V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 4. Interrupt Timing



NOTE:
C1 AND C2 SHOULD BE BASED ON MANUFACTURER'S SPECIFICATION. PARASITIC CAPACITANCE SHOULD BE INCLUDED WITH C1 AND C2. R1 IS ONLY REQUIRED IF U1 WILL NOT DRIVE TO X1 INPUT LEVELS

TYPICAL CRYSTAL SPECIFICATION

FREQUENCY:	2 – 4MHZ
LOAD CAPACITANCE (C_L):	12 – 32pF
TYPE OF OPERATION:	PARALLEL RESONANT, FUNDAMENTAL MODE

Figure 5. Clock Timing

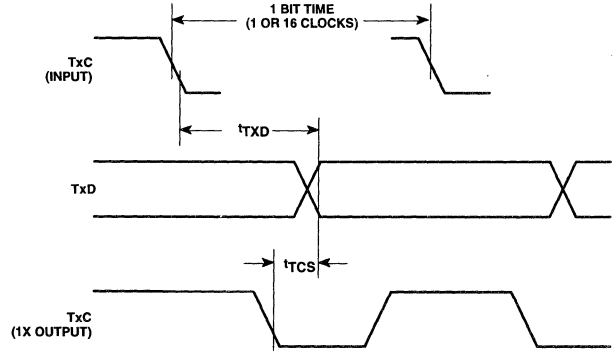


Figure 6. Transmitter External Clocks

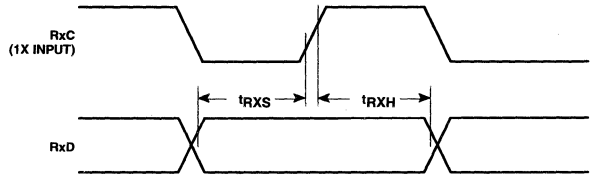
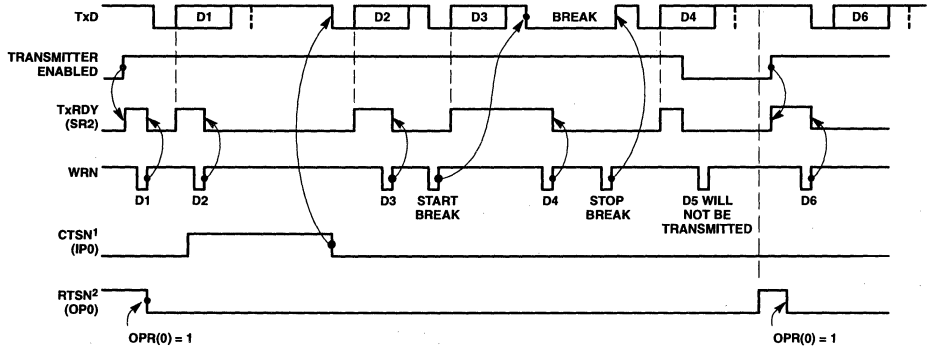
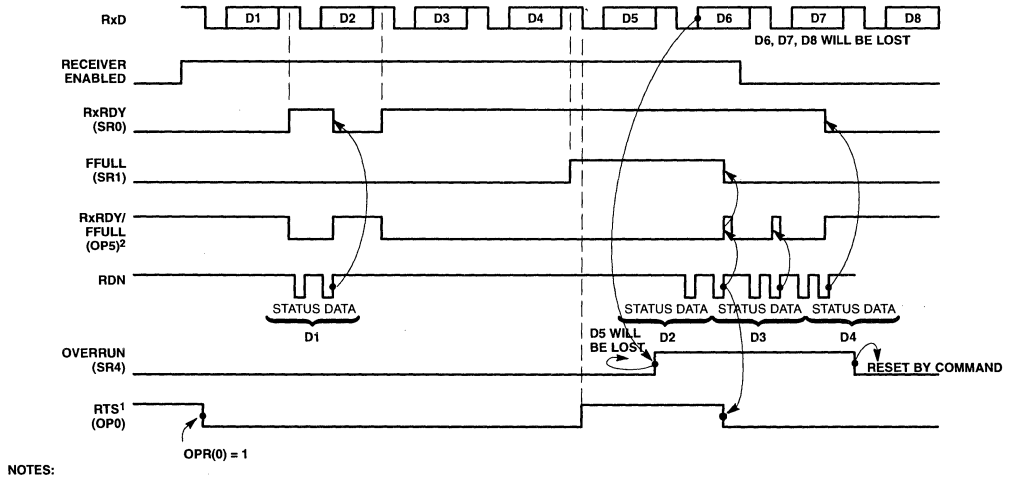


Figure 7. Receiver External Clock



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 8. Transmitter Timing



NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) = 1 and MR(6) = 0.

Figure 9. Receiver Timing

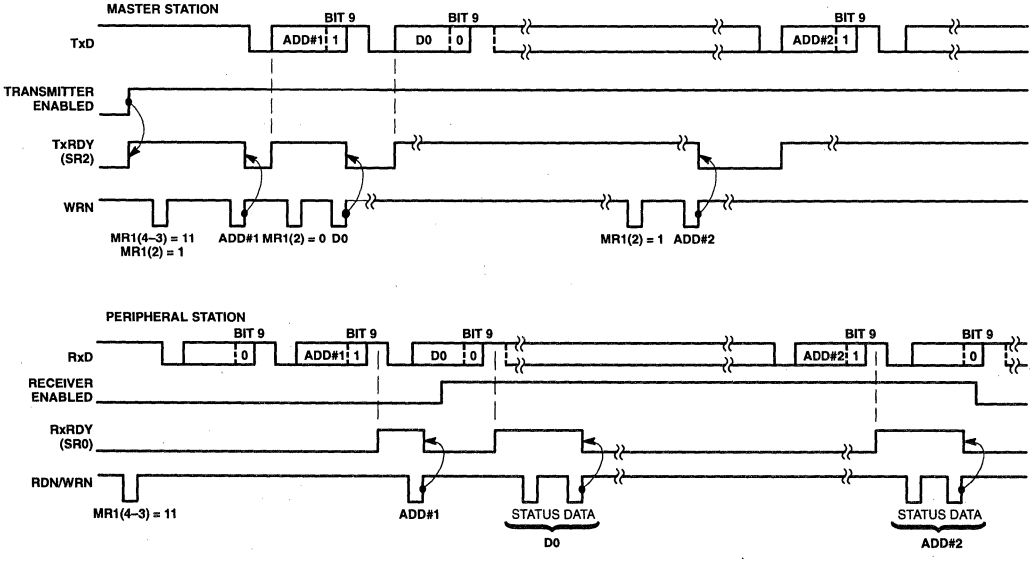


Figure 10. Wake-Up Mode

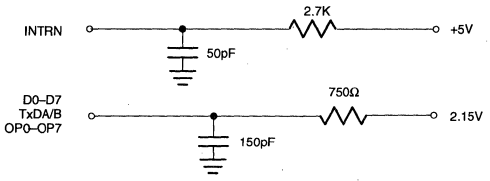


Figure 11. Test Conditions on Outputs

Output Port Notes

The output ports are controlled from four places: the OPCR register, the OPR register, the MR registers and the command register. The OPCR register controls the source of the data for the output ports OP2 through OP7. The data source for output ports OP0 and OP1 is controlled by the MR and CR registers. When the OPR is the source of the data for the output ports, the data at the ports is inverted from that in the OPR register. The content of the OPR register is controlled by the "Set Output Port Bits Command" and the "Reset Output Bits Command". These commands are at E and F, respectively. When these commands are used, action takes place only at the bit locations where ones exist. For example, a one in bit location 5 of the data word used with the "Set Output Port Bits" command will result in OPR5 being set to one. The OP5 would then be set to zero (V_{SS}). Similarly, a one in bit position 5 of the data word associated with the "Reset Output Ports Bits" command would set OPR5 to zero and, hence, the pin OP5 to a one (V_{DD}).

The CTS, RTS, CTS Enable Tx signals

CTS (Clear To Send) is usually meant to be a signal to the transmitter meaning that it may transmit data to the receiver. The CTS input is on pin IP0 for TxA and on IP1 for TxB. The CTS signal is active low; thus, it is called CTSAN for TxA and CTSBN for TxB.

RTS is usually meant to be a signal from the receiver indicating that the receiver is ready to receive data. It is also active low and is, thus, called RTSAN for RxA and RTSBN for RxB. RTSAN is on pin OP0 and RTSBN is on OP1. A receiver's RTS output will usually be connected to the CTS input of the associated transmitter. Therefore, one could say that RTS and CTS are different ends of the same wire!

MR2(4) is the bit that allows the transmitter to be controlled by the CTS pin (IP0 or IP1). When this bit is set to one AND the CTS input is driven high, the transmitter will stop sending data at the end of the present character being serialized. It is usually the RTS output of the receiver that will be connected to the transmitter's CTS input. The receiver will set RTS high when the receiver FIFO is full AND the start bit of the fourth character is sensed. Transmission then stops with four valid characters in the receiver. When MR2(4) is set to one, CTSN must be at zero for the transmitter to operate. If MR2(4) is set to zero, the IP pin will have no effect on the operation of the transmitter.

MR1(7) is the bit that allows the receiver to control OP0. When OP0 (or OP1) is controlled by the receiver, the meaning of that pin will be RTS. However, a point of confusion arises in that OP0 (or OP1) may also be controlled by the transmitter. When the transmitter is controlling this pin, its meaning is not RTS at all. It is, rather, that the transmitter has finished sending its last data byte. Programming the OP0 or OP1 pin to be controlled by the receiver and the transmitter at the same time is allowed, but would usually be incompatible.

RTS can also be controlled by the commands 1000 and 1001 in the command register. RTS is expressed at the OP0 or OP1 pin which is still an output port. Therefore, the state of OP0 or OP1 should be set low (either by commands of the CR register or by writing to the Set Output Ports Register) for the receiver to generate the proper RTS signal. The logic at the output is basically a NAND of the OPR register and the RTS signal as generated by the receiver. When the RTS flow control is selected via the MR(7) bit state of the OPR register is not changed. Terminating the use of "Flow Control" (via the MR registers) will return the OP0 or OP1 pins to the control of the OPR register.

Transmitter Disable Note

The sequence of instructions enable transmitter — load transmit holding register — disable transmitter will result in nothing being sent if the time between the end of loading the transmit holding register and the disable command is less that 3/16 bit time in the 16x mode or one bit time in the 1x mode. Also, if the transmitter, while in the enabled state and underrun condition, is immediately disabled after a single character is loaded to the transmit holding register, that character will not be sent.

In general, when it is desired to disable the transmitter before the last character is sent AND the TxEMT bit is set in the status register (TxEMT is always set if the transmitter has underrun or has just been enabled), be sure the TxRDY bit is active immediately before issuing the transmitter disable instruction. TxRDY sets at the end of the "start bit" time. It is during the start bit that the data in the transmit holding register is transferred to the transmit shift register.

Table 6. Baud Rates Extended

	Normal BRG		BRG Test	
CSR[7:4]	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0000	50	75	4,800	7,200
0001	110	110	880	880
0010	134.5	134.5	1,076	1,076
0011	200	150	19.2K	14.4K
0100	300	300	28.8K	28.8K
0101	600	600	57.6K	57.6K
0110	1,200	1,200	115.2K	115.2K
0111	1,050	2,000	1,050	2,000
1000	2,400	2,400	57.6K	57.6K
1001	4,800	4,800	4,800	4,800
1010	7,200	1,800	57.6K	14.4K
1011	9,600	9,600	9,600	9,600
1100	38.4K	19.2K	38.4K	19.2K
1101	Timer	Timer	Timer	Timer
1110	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X
1111	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X

NOTE:
Each read on address H'2' will toggle the baud rate test mode. When in the BRG test mode, the baud rates change as shown to the left. This change affects all receivers and transmitters on the DUART. Also, the RTSN outputs (OP[0] and OP[1]) become the transmitter 1x clock.

The test mode at address H'A' changes all transmitters and receivers to the 1x mode and connects the output ports to some internal nodes.

A condition that occurs infrequently has been observed where the receiver will ignore all data. It is caused by a corruption of the start bit generally due to noise. When this occurs the receiver will appear to be asleep or locked up. The receiver must be reset for the UART to continue to function properly.

Reset in the Normal Mode (Receiver Enabled)

Recovery can be accomplished easily by issuing a receiver software reset followed by a receiver enable. All receiver data, status and programming will be preserved and available before reset. The reset will NOT affect the programming.

Reset in the Wake-Up Mode (MR1[4:3] = 11)

Recovery can also be accomplished easily by first exiting the wake-up mode (MR1[4:3] = 00 or 01 or 10), then issuing a receiver software reset followed by a wake-up re-entry (MR1[4:3] = 11). All receiver data, status and programming will be preserved and available before reset. The reset will NOT affect the programming.

The receiver has a digital filter designed to reject "noisy" data and the receiver state machine was designed to reject noisy start bits or noise that might be considered a start bit. In spite of these precautions, corruption of the start bit can occur in 15ns window approximately 100ns prior to the rising edge of the data clock. The probability of this occurring is less than 10^{-5} at 9600 baud.

A corrupted start bit may have some deleterious effects in ASYNC operation if it occurs within a normal data block. The receiver will tend to align its data clock to the next '0' bit in the data stream, thus potentially corrupting the remainder of the data block. A good design practice, in environments where start bit corruption is possible, is to monitor data quality (framing error, parity error, break change and received break) and "data stopped" time out periods. Time out periods can be enabled using the counter/timer in the SCC2691, SCC2692, SCC2698B and SC68692 products. This monitoring can indicate a potential start bit corruption problem.

SCC2692 differences from the SCN2681 AN414

Author: D. Ibarra

DESCRIPTION

The SCC2692 is a CMOS version of the SCN2681 DUART. The SCC2692 is functionally and pin-to-pin compatible with the SCN2681 and can be substituted into existing SCN2681 designs. There are a few additional features and differences in the SCC2692 which are discussed below.

The major difference between the two parts is that the SCC2692 is CMOS, while the SCN2681 is NMOS. This means the SCC2692 draws significantly less power than the SCN2681.

Another difference between the two parts is that the SCC2692 has used edge triggered latches for the configuration registers: MR1 MR2 CSR. OPCR and ACR. The SCN2681 uses transparent latches, gated by WRN AND CEN. So, because of the undefined state of the data bus prior to the data being valid, both the receiver and transmitter must be disabled before writing to any register which could affect them, even if the same data is being rewritten. The SCC2692 will not be affected by the undefined data and will allow, for example the transmitter configuration to be changed without affecting the receiver operation. Only the transmitter would have to be disabled for the following: changing the transmitted stop bit length; changing the value of the transmitted ninth bit during wake-up mode; and changing the clock source or value for the transmitter only. It is still recommended to disable the transmitter or receiver before changing their respective configurations.

SOFTWARE

The SCN2681 counter/timer will be in timer mode with the timer running after power up and and after a hardware reset. The SCC2692 counter/timer will also be in timer mode after power up and after a hardware reset, but the timer will not be running until it receives a start counter/timer command (read at address H'E'). After this initial start the SCC2692 timer will run continuously. Subsequent start C/T commands will cause either the SCC2692 or the SCN2681 to immediately load the values in the CTUR and CTLR and start a new cycle. The stop counter command will reset the counter ready status bit (ISR[3]), but will have no effect on the timer mode operation for either part.

Utilizing command register (CR) bit 7 which is an unused bit in the SCN2681 makes six additional commands available to the user. SCN2681 programs which set this bit to zero will not be affected by this change and will run with the SCC2692.

Timeout Mode

This mode is useful for when the user programs RxRDY to interrupt the CPU when the receive FIFO is full. When less than three characters are received, the FIFO won't become full and the CPU won't get an RxRDY interrupt. The timeout mode provides the user with a time out interrupt via the counter/timer. If characters are received and the FIFO does not become full, a preselected period of delay can be timed out by the counter/timer (C/T) and the CPU interrupted.

The counter/timer is used in this mode by programming CTUR/CTLR with a value greater than the normal receive character period. Each time a received character is transferred from the shift register to the receive holding register (RHR), the C/T is reloaded with the value in CTLR/CTUR and then restarted. If a continuous data stream is not received and the C/T is allowed to end the count, the counter ready bit ISR[3], will be set. If the interrupt mask, IMR[3], has been set, an interrupt will be generated. This mode is enabled by writing CR = H'A0', and is turned off by writing CR = H'C0'.

Power Down Mode

Power down mode can be used for energy conservation during idle periods. This mode saves the contents of all the internal registers, stops the oscillator and suspends the operation of any function that uses the oscillator. In addition, the current used by the part is reduced. The part can be put into power down mode at any time and restored to normal operation when needed. Since all register values are saved, re-initialization is not necessary.

To put the part into power down mode:

- CRA = H'30' — Reset Tx A
- CRA = H'20' — Reset Rx A
- CRB = H'30' — Reset Tx B
- CRB = H'20' — Reset Rx B
- CRA = H'E0' — power down mode on

To get out of power down mode:

- CRA – H'F0' — Power down mode off
- Wait for oscillator to start up
- CRA = H'05' — Enable Rx A and Tx A
- CRB = H'05' — Enable Rx B and Tx B

Set/Reset RTSN Output

The RTSN output (OP0 and OP1) can be programmed to be asserted or negated automatically by either the receiver or the transmitter and it can be manually asserted and negated. Both the SCN2681 and the SCC2692 provide the ability to manually set and reset the output port bits by writing the appropriate bit mask to the Set output port bits command address or to the Reset output port bits command address (see data sheets for details). The SCC2692 as an additional feature provides commands in the CR to easily assert and negate just the RTSN output. CR H'80' will assert RTSN, cause the output to go low while CR = H'90' will negate RTSN, cause the output to go high.

HARDWARE

The on board oscillator circuitry in the SCC2692 is different from the SCN2681. This was required because of the addition of the power down mode logic. SCN2681 boards which use a crystal between the X1 and X2 pins with an equal value capacitor from X1 to ground as from X2 to ground can be used unmodified with the SCC2692. The SCC2692 does not require an external resistor but will operate with one there. SCN2681 boards which use an external oscillator to drive a signal into X1 and have X2 grounded can be used with the SCC2692.

The oscillators on both parts are the same basic type, consisting of an inverter and feedback resistor between the X1 and X2 pins, which, with the addition of an external crystal and capacitors, are used to implement a Pierce oscillator. The SCN2681 has the output of the inverter connected to X1, the input of the inverter connected to X2, and the inverter is a Schmitt trigger. The SCC2692 has the input of the inverter connected to X1 and the output of the inverter connected to X2.

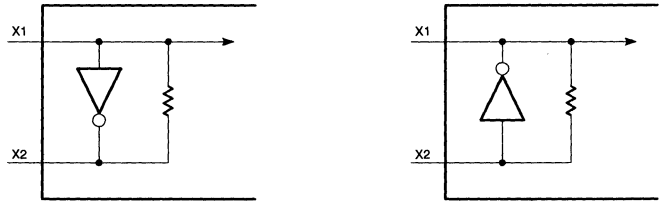
Because of the Schmitt trigger inverter, the SCN2681 is limited to using small value external capacitors. If capacitors of 15pF or greater are used, intermittent power–on problems may be experienced. The oscillator may stay in relaxation mode oscillating at a frequency much lower than the one the crystal is specified for. For this reason we recommend using external capacitors of around

SCC2692 differences from the SCN2681 AN414

5pF and board supplied stray capacitance of no more than 5pF. It has also been found that adding an external resistor of 100k–1 MΩ across X1 and X2 will solve other start up problems for some designs. While we recommend using balanced capacitors (C1=C2) of 5pF, unbalanced values may be used. Since the X2 pin (input to the internal inverter) has the most sensitivity to capacitance, many designs use a larger value capacitor (10–15pF) on the X1 pin while leaving 5pF on the X2 pin.

The SCC2692 oscillator is not limited to the recommendations required for the SCN2681. It does not need an external resistor and will operate with a much wider range of external capacitor values. New designs using the SCC2692 oscillator should use a parallel calibrated crystal and the external capacitor values should be adjusted until the total circuit capacitance matches the capacitance specified for the crystal. The capacitor values are not limited to any specific value but the two capacitors should be approximately equal in value. Using two 24pF capacitors and a 3.6864MHz crystal with CL = 20pF will give accurate reliable results. A source for this crystal is: Saronix, Palo Alto, CA, part number NYP037–20. From California call (800) 422-3355; outside California call (800) 227-8974.

Some designs will not use the on board oscillator circuitry but will drive the part with an external clock source. The SCN2681 and the SCC2692 both require that the external clock be driven into the X1 pin. The SCN2681 requires that the X2 pin be grounded while the SCC2692 X2 pin can be grounded or left open. Alternately, the X2 input can be driven with the complement of the clock signal going to X1 for both parts.



Oscillator Configuration

Extended baud rates for SCN2681, SCN68681, SCC2691, SCC2692, SCC68681 and SCC2698B

Author: Peter Narvaez

AFFECT OF 'RESERVED REGISTERS' ON BAUD RATES

The Philips Semiconductors UART chips (EXCEPTING the SC26C94) all have two test modes which are accessed via a READ of the reserved registers at hex address 2 and A. Each time a read of either address is performed, a flip-flop at that address will toggle. Software must keep track of the state of these flop-flops since there is no internal indication of the sate of these flop-flops. They are reset to the non-test condition by a hardware reset of the chip. Other methods for resetting are described below.

The test mode at address 2 is useful for the user requiring higher speed baud rates. It gives rates up to 115.2Kb in the 16x mode. In test mode 2 the dividers in the baud rate generator are changed. Test mode 2 will, therefore, effect all UARTs on the chip. Please note in the table below that some of the more common baud rates do not change when in test mode 2. Test 2 also changes the RTSN outputs to the transmitter 1x clock.

Table 1. Baud Rates

Test 2 = 0 Test A = 0	Test 2 = 1 Test A = 0	Test 2 = 1 Test A = 1	Test 2 = 0 Test A = 1
1x Baud Rate	1x Baud Rate	1x Baud Rate	1x Baud Rate
38,400	38,400	614,400	614,400
19,200	19,200	307,200	307,200
9,600	9,600	153,600	153,600
7,200	57,600	921,600	115,200
4,800	4,800	76,800	76,800
2,400	57,600	921,600	38,400
2,000	2,000	32,000	32,000
1,800	14,400	230,400	28,800
1,200	115,200	1,843,200	19,200
1,050	1,050	16,800	16,800
600	57,600	921,600	9,600
300	28,800	460,800	4,800
200	19,200	307,200	3,200
150	14,400	230,400	2,400
134.5	1,076	17,216	2,152
110	880	14,080	1,760
75	7,200	115,200	1,200
50	4,800	76,800	800

The baud rate of 115,200 would be selected by first reading address 2 and then setting the CSR (Clock Select Register) for the 1200 baud rate.

The test mode at address A changes all receivers and transmitters to the 1x mode of operation. It also connects some of the output pins to to various internal signals (mostly baud rate clocks). This mode is not very useful unless the 1x mode is desired for all channels and the output port pins are not used. Use of the test mode will not violate any of the specified speed parameters. Its use as a normal mode of operation is not, however, specifically verified in productions testing.

As mentioned previously, returning from the test mode to normal operation only requires another read of address 2 or A as appropriate. If for some reason the software is not aware of which test mode is in use, it can be painful to properly reset the test modes since there are four choices of action and only one of them will be correct. Of course a hardware reset will always reset both test modes. Since a hardware reset often is equivalent to a system restart, the following methods are presented to regain control of the test mode.

At the risk of belaboring the subject it should be mentioned that several approaches and several versions of each could be applied – the practicality of each being dependent on the hardware in use. These may be characterized or typed as follows:

1. Internal transmit loop of: send – test – set condition – send ...
2. Use Counter/Timer (C/T) to generate a time period in which a byte or start bit may be sent.
3. Set the C/T to stop upon the completion of transmission. The value in the C/T then directly represents the speed of the unknown data clock. The inverse of 2)
4. Sending data to or receiving data from a known good device and evaluating the error status of that data.

For the discussion below it will be convenient to represent the state of the test flip-flops as two binary bits (00 being normal) thus:

We choose a baud rate which is different for all four conditions of the test bits. The 7200 baud rate is one of these. Any configuration of the test bits except 00 will increase the baud rate by a factor of eight or more. (Specifically 00 = 1x; 01 = 8x; 10 = 1 6x. 11 = 128x). A bit time at 7200 baud is about 138µs and half of that 69µs.

Table 2. Baud Rates

Flip-Flop	Test A	Test 2	7200 Baud Rate
00	inactive	inactive	7200 (normal)
01	inactive	active	57,600
10	active	inactive	115,200
11	active	active	921,000

Type 1.

This method will use features internal to the UART to determine and reset to the normal mode. It will use the counter/timer to set up a known time reference and then read the value of the TxEMT and TxRDY bits in the status register at the end of this time. In normal operation at 7200 baud the A bit time will require 512 clocks of the X1 input. We know that a test mode will increase the 7200 baud rate by at least 8. A bit time then requires 64 'X1' clocks.

Reset receiver and transmitter then set up transmitter for local loop back and 7200 baud. Set counter timer for counter mode, its preset value to 48 (0030 hex), its clock to the X1 input. This C/T setting will cause it to time out at approximately three-fourths bit time. (The precise time is not important nor is the X1 frequency). Interrupt on C/T ready or poll the ISR (Interrupt Status Register) C/T ready bit. The control register setup follows. (Hex values)

13 → MR1 AA → CSR 00 → OPCR 00 → IPCR 00 → CTUR

07 → MR2 4A → CR 60 → ACR 08 → IMR 30 → CTLR

The test loop will look for the TxRDY TxMT status bits to be in the 00 condition when the C/T times out. This will mean that the start bit of a transmitted character has not completed. Since the test modes will, in general, make the data clocks faster by at least a factor of eight, any data clock slower than 2x will cause the above bits to be in the 00 state at C/T time out. The flow would then be:

Extended baud rates for SCN2681, SCN68681, SCC2691, SCC2692, SCC68681 and SCC2698B

BEGIN
Toggle Test 2
TEST ROUTINE:
Enable Transmitter
Load Transmit holding register
Start Counter/timer
Wait for C/T time out
Stop C/T
END TEST
Read status register, if TxEMT and TxRDY = 00 then quit
Reset Transmitter
Toggle Test A
Call Test Routine
Read status register, if TxEMT and TxRDY = 00 then quit
Toggle Test 2

END

Assuming the test flop-flops were not in state 00 to begin with, the above will always return the test flip-flops to 00 on or before the second toggle of Test 2. The above is predicated upon knowing the system is in a test condition but not which one. It is therefore valid to guess Test 2 and just blindly toggle that flip-flop as a first step.

Type 2.

Similar to above without TEST ROUTINE and TEST. In this method the value of the C/T will be used to determine an approximate bit rate and from that determine which flip-flops need to be toggled in order to return to normal operation. Since we are dealing with large the baud rate changes that test modes bring about it is not necessary to make exact measurements.

Set up the UART as above
Enable Transmitter
Load Transmit holding register
Start Counter/timer
Wait for C/T time out
Stop C/T
Read status register.

Depending on the test mode active we would expect the TxEMT TxRDY bits to be as follows:

Table 3.

Test Mode	TxEMT TxRDY
01	00
10	01
11	11

Toggle the test mode bits according to the indication of the transmitter status bits.

Type 3.

Here the value in the C/T is used to determine the active test mode. Preset the C/T to 48 (0030 hex). Set the interrupt for TxRDY. The UART control register settings follow.

13 → MR1 AA → CSR 00 → OPCR 00 → IPCR 00 → CTUR

07 → MR2 4A → CR 60 → ACR 01 → IMR 30 → CTLR
Enable Transmitter
Load Transmit holding register
Start Counter/timer
Wait for TxRDY C/T time out
Stop C/T
Read C/T upper and lower registers

Table 4.

Counter Value	Indicates Test State
> 512	01 (CTU > 0)
< 16, > 24	10
< 0, > 4	11

The above numbers are based on the time required for a start bit to be sent. Other time intervals of course may be used. The exact values also depend on how fast the control processor can service the interrupts or how long a pooling loop is. One could just as well use a full character time instead of a start bit time.

Type 4.

This test will send a character to a known good receiver. It is suggested to send an eight bit '00' character with even parity at 1800 baud. The test mode will increase the 1800 baud rate to 14400, 230400, or 28800. The UART control register settings follow.

03 → MR1 AA → CSR 00 → OPCR 00 → IPCR 00 → CTUR

07 → MR2 4A → CR EO → ACR 01 → IMR 30 → CTLR

Set the receiver to 9600 baud. Depending on the active test mode and a bit of asynchronous timing the receiver will 'see' the 00 character as follows:

Table 5.

Test Mode	Character Received
01	E0 or C0
11	No data received. Byte time shorter than a start bit.
10	FE or FC

The above, of course, may not be very practical when the status of the receiver is not available to the local processor. These have not verified the above in hardware. However, the idea of what is desired is shown. Actual applications will no doubt vary from the above as hardware and system timing dictate

Dual asynchronous receiver/transmitter (DUART) SCC68692

DESCRIPTION

The Philips Semiconductors SCC68692 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It is compatible with other S68000 family devices and can also interface easily with other microprocessors. The DUART can be used in a polled or interrupt driven systems.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruple buffered to minimize the potential of receiver over-run or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the receiver buffer is full.

Also provided on the SCC68692 are a multipurpose 6-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

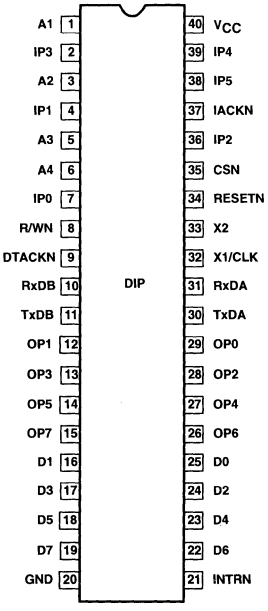
FEATURES

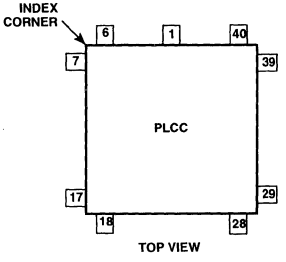
- S68000 bus compatible
- Dual full-duplex asynchronous receiver/transmitters
- Quadruple buffered receiver data register
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - Non-standard rates to 115.2kb
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
  - Multidrop mode (also called 'wake-up' or '9-bit')
- Multi-function 6-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
  - Inputs have typically >100k pull-up resistors
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Interrupt vector output on interrupt acknowledge
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
- Maximum data transfer rates: 1X – 1MB/sec, 16X – 125kB/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Power down mode
- Receiver timeout mode
- Commercial and Industrial temperature range versions
- TTL compatible
- Single +5V power supply

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±10%, T_A = 0 to +70°C	V_{CC} = +5V ±10%, T_A = -40 to +85°C	DWG #
40-Pin (600 mils wide) Ceramic Dual In-Line Package (Cerdip)	SCC68692C1F40	SCC68692E1F40	0590B
40-Pin (600 mils wide) Plastic Dual In-Line Package (DIP)	SCC68692C1N40	SCC68692E1N40	0415C
44-Pin Plastic Leaded Chip Carrier (PLCC)	SCC68692C1A44	SCC68692E1A44	0403G

PIN CONFIGURATIONS





TOP VIEW

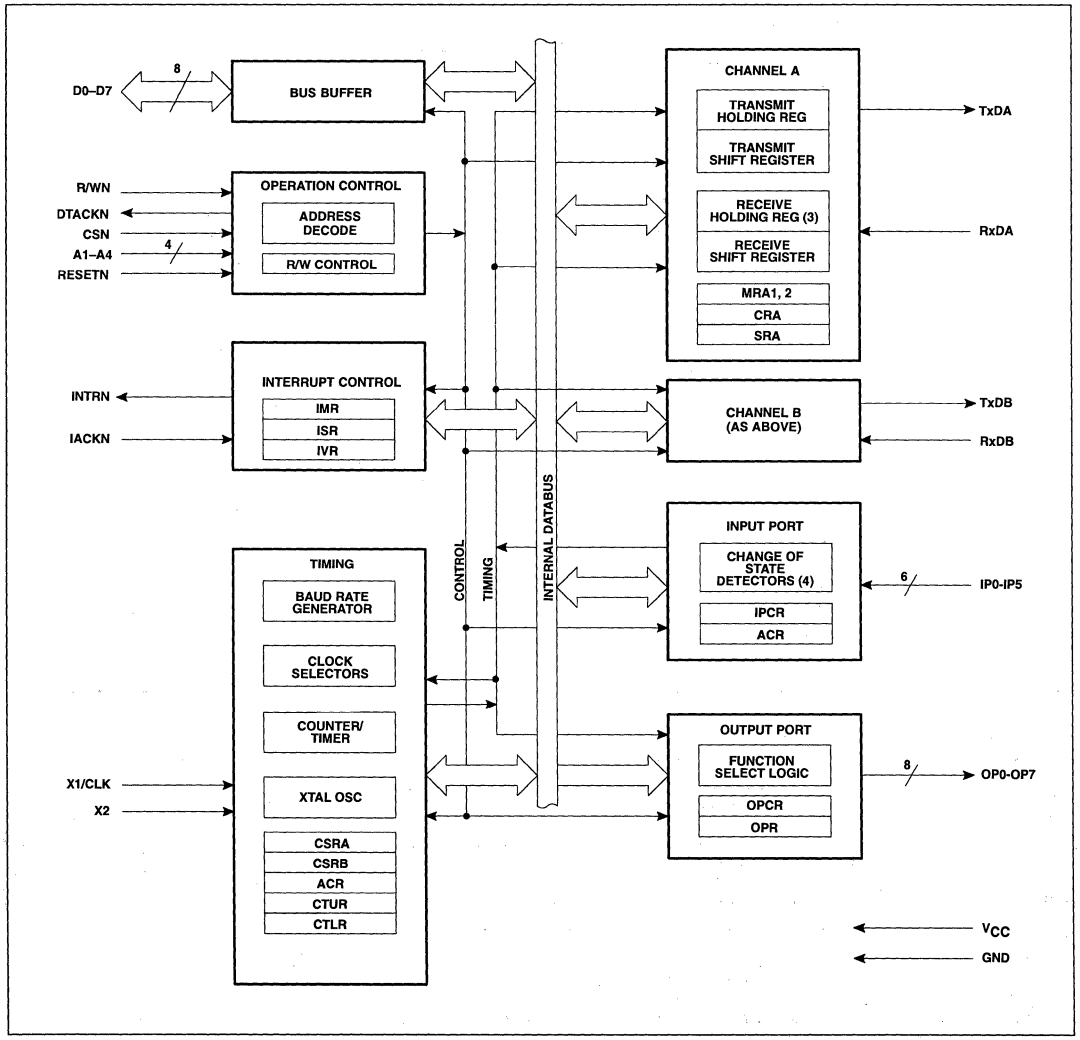
PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A1	24	INTRN
3	IP3	25	D6
4	A2	26	D4
5	IP1	27	D2
6	A3	28	D0
7	A4	29	OP6
8	IP0	30	OP4
9	R/WN	31	OP2
10	DTACKN	32	OP0
11	RxDB	33	TxDA
12	NC	34	NC
13	TxDB	35	RxDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CSN
18	D1	40	IP2
19	D3	41	IACKN
20	D5	42	IP5
21	D7	43	IP4
22	GND	44	V_{CC}

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	Note 4	°C
T_{STG}	Storage temperature range	–65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	–0.5 to +7.0	V
V_S	Voltage from any pin to GND[3]	–0.5 to V_{CC} +0.5	V
P_D	Power dissipation	750	mW

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NO.	TYPE	NAME AND FUNCTION
D0–D7	25,16,24,17 23,18,22,19	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CSN	35	I	**Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0–D7 as controlled by the R/WN and A1–A4 inputs. When CEN is High, the DUART places the D0–D7 lines in the 3-State condition.
R/WN	8	I	**Read/Write:** A High input indicates a read cycle and a low input indicates a write cycle, when a cycle is initiated by assertion of the CSN input.
A1–A4	1,2,5,6	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESETN	34	I	**Reset:** A Low level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), initializes the IVR to hex 0F, puts OP0–OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Resets Test Mode, sets MR pointer to MR1.
DTACKN	9	O	**Data Transfer Acknowledge:** 3-State active-Low output asserted in write, read, or interrupt cycles to indicate proper transfer of data between the CPU and the DUART.
INTRN	21	O	**Interrupt Request:** Active-Low, open-drain output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
IACKN	37	I	**Interrupt Acknowledge:** Active-Low input indicating an interrupt acknowledge cycle. In response, the DUART will place the interrupt vector on the data bus and will assert DTACKN if it has an interrupt pending.
X1/CLK	32	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7).
X2	33	I	**Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 7). If X1/CLK is driven from an external source, this pin can be left open.
RxDA	31	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	10	I	**Channel B Receive Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	30	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	11	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low.
OP0	29	O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	12	O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	28	O	**Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	13	O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	27	O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxRDYAN/FFULLAN output.
OP5	14	O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxRDYBN/FFULLBN output.
OP6	26	O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxRDYAN output.
OP7	15	O	**Output 7:** General purpose output or Channel B open-drain, active-Low, TxRDYBN output.
IP0	7	I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	4	I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	36	I	**Input 2:** General purpose input or Channel B receiver external clock input (RxCB), or counter/timer external clock input. When external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP3	2	I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	39	I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	38	I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
V_{CC}	40	I	**Power Supply:** +5V supply input.
GND	20	I	**Ground**

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)[6]		2.0			V
V_{IH}	Input high voltage (except X1/CLK)[7]		2.5			V
V_{IH}	Input high voltage (X1/CLK)		$0.8V_{CC}$			V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}	Output high voltage (except OD outputs)[4]	I_{OH} = –400µA	V_{CC} –0.5			V
I_{IX1PD}	X1/CLK input current – power down	V_{IN} = 0 to V_{CC}	–10		+10	µA
I_{ILX1}	X1/CLK input low current – operating	V_{IN} = 0	–75		0	µA
I_{IHX1}	X1/CLK input high current – operating	V_{IN} = V_{CC}	0		75	µA
I_{OHX2}	X2 output high current – operating	V_{OUT} = V_{CC}, X1 = 0	0		+75	µA
I_{OHX2S}	X2 output high short circuit current – operating	V_{OUT} = 0, X1 = 0	–10		–1	mA
I_{OLX2}	X2 output low current – operating	V_{OUT} = 0, X1 = V_{CC}	–75		0	µA
I_{OLX2S}	X2 output low short circuit current – operating and power down	V_{OUT} = V_{CC}, X1 = V_{CC}	1		10	mA
I_I	Input leakage current:					
	All except input port pins	V_{IN} = 0 to V_{CC}	–10		+10	µA
	Input port pins	V_{IN} = 0 to V_{CC}	–20		+10	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			10	µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0V	–10			µA
I_{ODL}	Open-drain output low current in off State	V_{IN} = 0	–10			µA
I_{ODH}	Open-drain output high current in off State	V_{IN} = V_{CC}			10	µA
I_{CC}	Power supply current[5]					
	Operating mode	TTL input levels			10	mA
		CMOS input levels			10	mA
	Power down mode[12]	TTL input levels			3.0	mA
		CMOS input levels			2.0	mA

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test condition for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. All outputs are disconnected. Inputs are switching between TTL levels of 2.4V and 0.4V or CMOS levels of V_{CC} –0.2V and V_{SS} + 0.2V.
6. $T_A \geq 0°C$
7. $T_A < 0°C$

AC CHARACTERISTICS[1, 2, 4]

SYMBOL	FIGURE	PARAMETER	LIMITS			UNIT
			Min	Typ[3]	Max	
Reset Timing						
t_{RES}	1	RESET pulse width	200			ns
Bus Timing[5]						
t_{AS}	2,3,4	A1–A4 setup time to CSN Low	10			ns
t_{AH}	2,3,4	A1–A4 hold time from CSN Low	100			ns
t_{RWS}	2,3,4	RWN setup time to CSN High	0			ns
t_{RWH}	2,3,4	RWN holdup time to CSN High	0			ns
t_{CSW}[8]	2,3,4	CSN High pulse width	160			ns
t_{CSD}[9]	2,3,4	CSN or IACKN High from DTACKN Low	20			ns
t_{DD}	2,3,4	Data valid from CSN or IACKN Low			175	ns
t_{DA}	2	RDN Low to data bus active[8]	15			ns
t_{DF}	2,3,4	Data bus floating from CSN or IACKN High[8]			125	ns
t_{DI}	2	RDN High to data bus invalid[8]	20			ns
t_{DS}	2,3,4	Data setup time to CLK High	100			ns
t_{DH}	2,3,4	Data hold time from CSN High	0			ns
t_{DAL}	2,3,4	DTACKN Low from read data valid	0			ns
t_{DCR}	2,3,4	DTACKN Low (read cycle) from CLK High			125	ns
t_{DCW}	2,3,4	DTACKN Low (write cycle) form CLK High			125	ns
t_{DAH}	2,3,4	DTACKN High from CSN or IACKN High			100	ns
t_{DAT}	2,3,4	DTACKN High impedance from CSN or IACKN High			125	ns
t_{CSC}[7]	2,3,4	CSN or IACKN setup time to clock High	90			ns
Port Timing[5]						
t_{PS}	5	Port input setup time to CSN Low	0			ns
t_{PH}	5	Port input hold time from CSN High	0			ns
t_{PD}	5	Port output valid from CSN High			400	ns
Interrupt Timing						
t_{IR}	6	INTRN (or OP3–OP7 when used as interrupts) negated from:				
		Read RHR (RxRDY/FFULL interrupt)			300[10]	ns
		Write THR (TxRDY interrupt)			300[10]	ns
		Reset command (break interrupt)			300[10]	ns
		Stop C/T command (counter interrupt)			300[10]	ns
		Read IPCR (input port change interrupt)			300[10]	ns
		Write IMR (clear of interrupt mask bit)			300[10]	ns
Clock Timing						
t_{CLK}	7	X1/CLK High or Low time	100			ns
f_{CLK}	7	X1/CLK frequency	0[11]	3.6864	4	MHz
t_{CTC}	7	CTCLK (IP2) High or Low time	100			ns
f_{CTC}	7	CTCLK (IP2) frequency[9]	100		4	MHz
t_{RX}	7	RxC High or Low time	220			ns
f_{RX}	7	RxC frequency (16X)[9]	100		2	MHz
		(1X)[9]	100		1	MHz
t_{TX}	7	TxC High or Low time	220			ns
f_{TX}	7	TxC frequency (16X)[9]	0		2	MHz
		(1X)[9]	0		1	MHz
Transmitter Timing						
t_{TXD}	8	TxD output delay from TxC Low			350	ns
t_{TCS}	8	Output delay from TxC Low to TxD data output			150	ns
Receiver Timing						
t_{RXS}	9	RxD data setup time to RxC High	240			ns
t_{RXH}	9	RxD data hold time from RxC High	200			ns

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test condition for interrupt outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}.
5. This specification will impose maximum 68000 CPU CLK to 6MHz. Higher CPU CLK can be used if repeating bus reads are not performed. Consecutive write operations to the same command register require at least three edges of the X1 clock between writes.

6. This specification imposes a lower bound on CSN and IACKN Low, guaranteeing that it will be Low for at least 1 CLK period. This requirement is made on CSN only to insure assertion of DTACKN and not to guarantee operation of the part.
7. This specification is made only to insure that DTACKN is asserted with respect to the rising edge of the X1/CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the setup time is violated, DTACKN may be asserted as shown, or may be asserted one clock cycle later.
8. Guaranteed by characterization of sample units.
9. Minimum frequencies are not tested but are guaranteed by design.
10. 325ns maximum for $T_A > 70°C$.
11. Operation to 0MHz is assured by design. Minimum test frequency is 2.0MHz.
12. See UART application note for power down currents less than 5µA.

BLOCK DIAGRAM

The SCC68692 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the Block Diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The DTACKN output is asserted during write and read cycles to indicate to the CPU that data has been latched on a write cycle, or that valid data is present on the bus on a read cycle.

Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR), the Auxiliary Control Register (ACR), and the Interrupt Vector Register (IVR). The IMR may be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. When IACKN is asserted, and the DUART has an interrupt pending, the DUART responds by placing the contents of the IVR register on the data bus and asserting DTACKN.

Outputs OP3–OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

If an external is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 7.

If an external clock is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 5.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. A 3.6864MHz crystal or external clock must be used to get the standard baud rate. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the SCC68692 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

Input Port

The inputs to this unlatched 6-bit port can be read by the CPU by performing a read operation at address H'D'. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always be read as a logic 1 and D6 will reflect the level of IP2. The pins of this port can also serve as auxiliary inputs to certain portions of the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs, lasting longer than 25 – 50µs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

The input port pulse detection circuitry uses a 38.4kHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (this assumes that the clock input is 3.6864MHz). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if

the transition occurs "coincident with the first sample pulse". The 50µs time refers to the situation in which the change-of-state is "just missed" and the first change-of-state is not detected until 25µs later.

Output Port

The output port pins may be controlled by the OPR, OPCR, MR and the CR registers. Via appropriate programming they may be just another parallel port to external circuits, or they may represent many internal conditions of the UART. When this 8-bit port is used as a general purpose output port, the output port pins assume a state which is the complement of the Output Port Register (OPR). OPR(n) = 1 results in OP(n) = Low and vice versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address H'E' with the accompanying data specifying the bits to be reset (1 = set, 0 = no change). Likewise, a bit is reset by a write at address H'F' with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also be individually assigned specific functions by appropriate programming of the Channel A mode registers (MR1A, MR2A), the Channel B mode registers (MR1B, MR2B), and the Output Port Configuration Register (OPCR).

Output ports are driven high on hardware reset.

OPERATION

Transmitter

The SCC68692 is conditioned to transmit data when the transmitter is enabled through the command register. The SCC68692 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When a character is loaded into the Transmit Holding Register (THR), the above conditions are negated. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again which means one full character time of buffering is provided. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR. If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enable, the CTSN input must be Low in order for the character to be transmitted. If it goes High in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes Low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

Receiver

The SCC68692 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7–1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive Holding Register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one-half bit time before a search for the next start bit begins.

Receiver FIFO

The RHR consists of a First-In-First-Out (FIFO) stack with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4] will be set-upon receipt of the start bit of the new (overrunning) character.

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

Receiver Reset and Disable

Receiver disable stops the receiver immediately – data being assembled if the receiver shift register is lost. Data and status in the FIFO is preserved and may be read. A re-enable of the receiver after a disable will cause the receiver to begin assembling characters at the next start bit detected. A receiver reset will discard the present shift register date, reset the receiver ready bit (RxRDY), clear the status of the byte at the top of the FIFO and re-align the FIFO read/write pointers. This has the appearance of "clearing or flushing" the receiver FIFO. In fact, the FIFO is NEVER cleared! The data in the FIFO remains valid until overwritten by another received character. Because of this erroneous reading, the FIFO will miss-align the FIFO pointers and result in the reading of previously read data. A receiver reset will re-align the pointers.

Timeout Mode

The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RHR, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know there is data left in the FIFO. The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. The timeout mode should only be used by one channel at once, since it uses the C/T. CTU and CTL must be loaded with a value greater than the normal receive character period. The timeout mode disables the regular START/STOP Counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RHR, the C/T is stopped after 1 C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Since receiving a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx = 'Ax', will also clear the counter ready bit and stop the counter until the next character is received.

Multidrop Mode

The DUART is equipped with a wake up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wake up' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems. For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1x by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1x, switches the pointer to MR2x. The pointer then remains at MR2x, so that subsequent accesses are always to MR2x unless the pointer is reset to MR1x as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'0A' should never be read during normal operation since they are reserved for internal diagnostics.

Table 1. Register Addressing

A3	A2	A1	A0	READ (RDN = 0)	WRITE (WRN = 0)
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	BRG Test	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
0	1	0	0	Input Port Change Register (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Register (CRUR)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	1X/16X Test	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
1	1	0	0	Interrupt Vector Register (IVR)	Interrupt Vector Register (IVR)
1	1	0	1	Input Port	Output Port Conf. Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

MR1A – Channel A Mode Register 1

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7] – Channel A Receiver Request-to-Send Control
This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the Channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1A[6] – Channel A Receiver Interrupt Select
This bit selects either the Channel A receiver ready status (RxRDY) or the Channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

MR1A[5] – Channel A Error Mode Select
This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block" mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

MR1A[4:3] – Channel A Parity Mode Select
If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] = 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] – Channel A Parity Type Select
This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] – Channel A Bits Per Character Select
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] – Channel A Mode Select
Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically re-transmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is re-clocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.

6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is re-clocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been retransmitted.

MR2A[5] – Channel A Transmitter Request-to-Send Control

CAUTION: When the transmitter controls the OP pin (usually used for the RTSN signal) the meaning of the pin is not RTSN at all! Rather, it signals that the transmitter has finished the transmission (i.e., end of block).

This bit allows deactivation of the RTSN output by the transmitter. This output is manually asserted and negated by the appropriate commands issued via the command register. MR2[5] set to 1 caused the RTSN to be reset automatically one bit time after the character(s) in the transmit shift register and in the THR (if any) are completely transmitted (including the programmed number of stop bits) if a previously issued transmitter disable is pending. This feature can be used to automatically terminate the transmission as follows:

1. Program the auto-reset mode: MR2[5]=1
2. Enable transmitter, if not already enabled
3. Assert RTSN via command
4. Send message
5. After the last character of the message is loaded to the THR, disable the transmitter. (If the transmitter is underrun, a special case exists. See note below.)
6. The last character will be transmitted and the RTSN will be reset one bit time after the last stop bit is sent.

NOTE: The transmitter is in an underrun condition when both the TxRDY and the TxEMT bits are set. This condition also exists immediately after the transmitter is enabled from the disabled or reset state. When using the above procedure with the transmitter in the underrun condition, the issuing of the transmitter disable must be delayed from the loading of a single, or last, character until the TxRDY becomes active again after the character is loaded.

Table 2. Register Bit Formats

	BIT 7	BIT 6	BIT 5	BIT 4 BIT 3	BIT 2	BIT 1 BIT 0
MR1A MR1B	RxRTS CONTROL	RxINT SELECT	ERROR MODE	PARITY MODE	PARITY TYPE	BITS PER CHARACTER
	0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multidrop Mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

	BIT 7 BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MR2A MR2B	CHANNEL MODE	TxRTS CONTROL	CTS ENABLE Tx	STOP BIT LENGTH*			
	00 = Normal 01 = Auto-Echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

NOTE: *Add 0.5 to values shown for 0 – 7 if channel is programmed for 5 bits/char.

	BIT 7 BIT 6 BIT 5 BIT 4	BIT 3 BIT 2 BIT 1 BIT 0
CSRA CSRB	RECEIVER CLOCK SELECT	TRANSMITTER CLOCK SELECT
	See Text	See Text

	BIT 7 BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CRA CRB	MISCELLANEOUS COMMANDS	DISABLE Tx	ENABLE Tx	DISABLE Rx	ENABLE Rx
	See Text	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE: Access to the miscellaneous commands should be separated by 3 X1 clock edges. A disabled transmitter cannot be loaded.

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SRA SRB	RECEIVED BREAK*	FRAMING ERROR*	PARITY ERROR*	OVERRUN ERROR	TxEMT	TxRDY	FFULL	RxRDY
	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE: *These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3 BIT 2	BIT 1 BIT 0
	OP7	OP6	OP5	OP4	OP3	OP2
OPCR	0 = OPR[7] 1 = TxRDYB	0 = OPR[6] 1 = TxRDYA	0 = OPR[5] 1 = RxRDY/ FFULLB	0 = OPR[4] 1 = RxRDY/ FFULLA	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1x) 11 = RxCB(1x)	00 = OPR[2] 01 = TxCA(16x) 10 = TxCA(1x) 11 = RxCA(1x)

	BIT 7	BIT 6 BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	BRG SET SELECT	COUNTER/TIMER MODE AND SOURCE	DELTA IP3 INT	DELTA IP2 INT	DELTA IP1 INT	DELTA IP0 INT
ACR	0 = set 1 1 = set 2	See Table 4	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	DELTA IP3	DELTA IP2	DELTA IP1	DELTA IP0	IP3	IP2	IP1	IP0
IPCR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IN PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	COUNTER READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA
ISR	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IN PORT CHANGE INT	DELTA BREAK B INT	RxRDY/ FFULLB INT	TxRDYB INT	COUNTER READY INT	DELTA BREAK A INT	RxRDY/ FFULLA INT	TxRDYA INT
IMR	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]
CTUR								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]
CTLR								

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IVR[7]	IVR[6]	IVR[5]	IVR[4]	IVR[3]	IVR[2]	IVR[1]	IVR[0]
IVR								

MR2A[4] – Channel A Clear-to-Send Control
If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IPO) each time it is ready to send a character. If IPO is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character.

MR2A[3:0] – Channel A Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1–9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1–1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit is enabled).

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

Table 3. Baud Rate

CSRA[7:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
0000	50	75
0001	110	110
0010	134.5	134.5
0011	200	150
0100	300	300
0101	600	600
0110	1,200	1,200
0111	1,050	2,000
1000	2,400	2,400
1001	4,800	4,800
1010	7,200	1,800
1011	9,600	9,600
1100	38.4k	19.2k
1101	Timer	Timer
1110	IP4–16X	IP4–16X
1111	IP4–1X	IP4–1X

NOTE: The receiver clock is always a 16X clock except for CSRA[7:4] = 1111.

CSRA – Channel A Clock Select Register

CSRA[7:4] – Channel A Receiver Clock Select
This field selects the baud rate clock for the Channel A transmitter. The field definition is shown in Table 3.

CSRA[3:0] – Channel A Transmitter Clock Select
This field selects the baud rate clock for the Channel A transmitter. The field definition is as shown in Table 3, except as follows:

CSRA[3:0]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP3–16X	IP3–16X
1111	IP3–1X	IP3–1X

The transmitter clock is always a 16X clock except for CSRA[3:0] = 1111.

CSRB – Channel B Clock Select Register

CSRB[7:4] – Channel B Receiver Clock Select
This field selects the baud rate clock for the Channel B receiver. The field definition is as shown in Table 3, except as follows:

CSRB[7:4]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP2–16X	IP2–16X
1111	IP2–1X	IP2–1X

The receiver clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0] – Channel B Transmitter Clock Select
This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

CSRB[3:0]	ACR[7] = 0	Baud Rate ACR[7] = 1
1110	IP5–16X	IP5–16X
1111	IP5–1X	IP5–1X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.
NOTE: Access to the upper four bits of the command register should be separated by three (3) edges of the X1 clock.

CRA[7:4] – Miscellaneous Commands
The encoded value of this field may be used to specify a single command as follows:

0000 No command.
0001 Reset MR pointer. Causes the Channel A MR pointer to point to MR1.
0010 Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.
0011 Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.
0100 Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block

block mode to clear all error status after a block of data has been received.

0101 Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.

0110 Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.

0111 Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.

1000 Assert RTSN. Causes the RTSN output to be asserted (Low).

1001 Negate RTSN. Causes the RTSN output to be negated (High).

1010 Set Timeout Mode On. The receiver in this channel will restart the C/T as each receive character is transferred from the shift register to the RHR. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset.

1011 Not used.

1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued

1101 Not used.

1110 Power Down Mode On. In this mode, the DUART oscillator is stopped and all functions requiring this clock are suspended. The execution of commands other than disable power down mode (1111) requires a X1/CLK. While in the power down mode, do not issue any commands to the CR except the disable power down mode command. It is recommended that the transmitter and receiver be disabled prior to placing the DUART into power down mode. This command is in CRA only. Design Note: The part will not output DTACKN while in power down mode. Use automatic DTACKN generation.

1111 Disable Power Down Mode. This command restarts the oscillator. After invoking this command, wait for the oscillator to start up before writing further commands to the CR. This command is in CRA only.

CRA[3] – Disable Channel A Transmitter
This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2] – Enable Channel A Transmitter
Enables operation of the Channel A transmitter. The TxRDY status bit will be asserted.

CRA[1] – Disable Channel A Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] – Enable Channel A Receiver
Enables operation of the Channel A receiver. If not in the special wake up mode, this also forces the receiver into the search for start bit state.

CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, with the exception of commands "Ex" and "Fx" which are used for power downmode. These two commands are not used in CRB. All other control actions that apply to CRA also apply to CRB.

SRA – Channel A Status Register

SRA[7] – Channel A Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line to the marking state for at least one-half a bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

SRA[6] – Channel A Framing Error
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SRA[5] – Channel A Parity Error
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity. In the special multidrop mode, the parity error bit stores the received A/D bit.

SRA[4] – Channel A Overrun Error
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a 'reset error status' command.

SRA[3] – Channel A Transmitter Empty (TxEMTA)
This bit will be set when the transmitter underruns, i.e., both the TxEMT and TxRDY bits are set. This bit and TxRDY are set when the transmitter is first enabled and at any time it is re-enabled after either (a) reset, or (b) the transmitter has assumed the disabled state. It is always set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission.

It is reset when the THR is loaded by the CPU, a pending transmitter disable is executed, the transmitter is reset, or the transmitter is disabled while in the underrun condition.

SRA[2] – Channel A Transmitter Ready (TxRDYA)
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, e.g., characters loaded into the THR while the transmitter is disabled will not be transmitted.

SRA[1] – Channel A FIFO Full (FFULLA)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SRA[0] – Channel A Receiver Ready (RxRDYA)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift to the FIFO and reset when the CPU reads the RHR, if after this read there are not more characters still in the FIFO.

SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR – Output Port Configuration Register

OPCR[7] – OP7 Output Select
This bit programs the OP7 output to provide one of the following:
0 The complement of OPR[7].
1 The Channel B transmitter interrupt output which is the complement of TxRDYB. When in this mode OP7 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[6] – OP6 Output Select
This bit programs the OP6 output to provide one of the following:
0 The complement of OPR[6].
1 The Channel A transmitter interrupt output which is the complement of TxRDYA. When in this mode OP6 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[5] – OP5 Output Select
This bit programs the OP5 output to provide one of the following:
0 The complement of OPR[5].
1 The Channel B transmitter interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[4] – OP4 Output Select
This field programs the OP4 output to provide one of the following:
0 The complement of OPR[4].
1 The Channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] – OP3 Output Select
This bit programs the OP3 output to provide one of the following:
00 The complement of OPR[3].
01 The counter/timer output, in which case OP3 acts as an open-drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
10 The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
11 The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] – OP2 Output Select
This field programs the OP2 output to provide one of the following:
00 The complement of OPR[2].
01 The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
10 The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
11 The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates to be generated by the BRG.

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.
Set 2: 75, 110, 134.5, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, and 19.2k baud.

Table 4. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz

BAUD RATE	ACTUAL 16x CLOCK (kHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	–0069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16756	–0260
1200	192	0
1800	288	0
2000	32056	0.175
2400	384	0
4800	768	0
7200	1152	0
9600	1536	0
19.2k	3072	0
38.4k	614	0

NOTE: Duty cycle of 16x clock is 50% ± 1%.

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 4.

ACR[6:4] – Counter/Timer Mode And Clock Source Select
This field selects the operating mode of the counter/timer and its clock source as shown in Table 5.

Table 5. ACR [6:4] Field Definition

[6:4]	MODE	CLOCK SOURCE
000	Counter	External (IP2)
001	Counter	TxCA – 1x clock of Channel A transmitter
010	Counter	TxCB – 1x clock of Channel B transmitter
011	Counter	Crystal or IP2 clock (x1/CLK) divided by 16
100	Timer	External (IP2)
101	Timer	External (IP2) divided by 16
110	Timer	Crystal or external clock (X1/CLK)
111	Timer	Crystal or IP2 clock (X1/CLK) divided by 16
NOTE: Timer mode generates a squarewave.		

ACR[3:0] – IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – IP3, IP2, IP1, IP0 Change-of-State
These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – IP3, IP2, IP1, IP0 Change-of-State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to H'00' when the DUART is reset.

ISR[7] – Input Port Change Status
This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] – Channel B Change In Break
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

ISR[5] – Channel B Receiver Ready or FIFO Full
The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in Channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel B FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[4] – Channel B Transmitter Ready
This bit is a duplicate of TxRDYB (SRB[2]).

ISR[3] – Counter Ready.
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] – Channel A Change in Break
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

ISR[1] – Channel A Receiver Ready Or FIFO Full
The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in Channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer caused the Channel A FIFO to become full; i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the ISR[0] and IMR waiting character is loaded into the FIFO.

ISR[0] – Channel A Transmitter Ready
This bit is a duplicate of TxRDYA (SRA[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be

asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3–OP7 or the reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. The waveform so generated is often used for a data clock. The formula for calculating the divisor n to load to the CTUR and CTLR for a particular 1X data clock is shown below:

$$n = \frac{C/T\ Clock\ Frequency}{2 \times 16\ Baud\ rate\ desired}$$

Often this division will result in a non-integer number; 26.3, for example. One can only program integer numbers in a digital divider. Therefore, 26 would be chosen. This gives a baud rate error of 0.3/26.3 which is 1.14%; well within the ability asynchronous mode of operation.

If the value in CTUR and CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read at address A3–A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a start counter command (read with A3–A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3–A0 = H'F'). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

IVR – Interrupt Vector Register

This register contains the interrupt vector. The register is initialized to H'0F' by RESET. The contents of the register are placed on the data bus when the DUART responds to a valid interrupt acknowledge cycle.

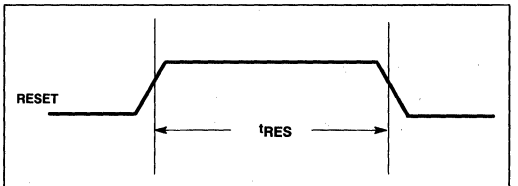
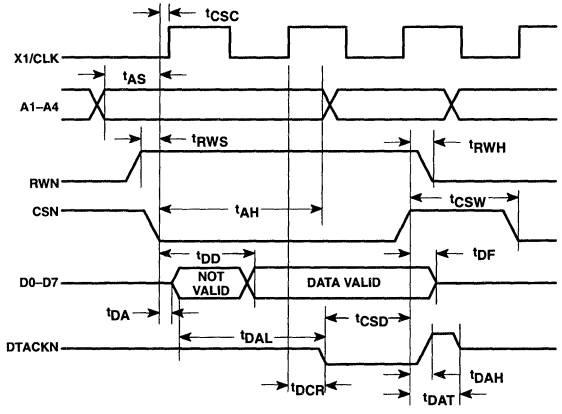
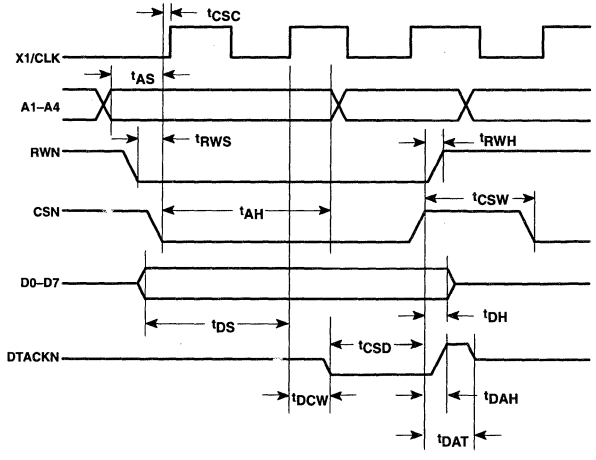


Figure 1. Reset Timing



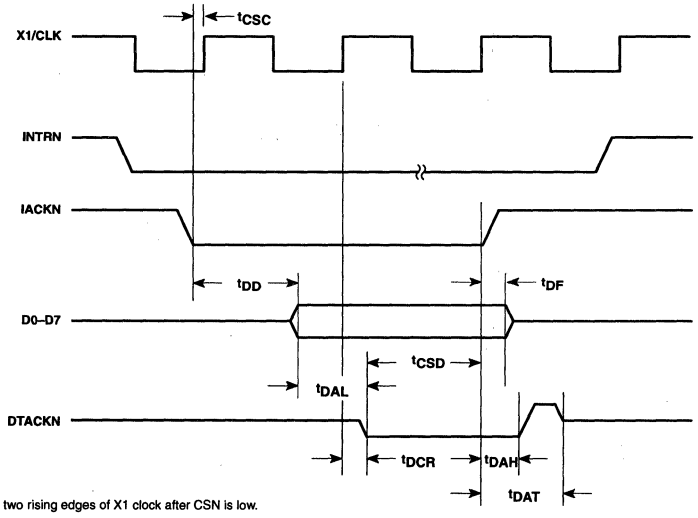
NOTE: DACKN low requires two rising edges of X1 clock after CSN is low.

Figure 2. Bus Timing (Read Cycle)



NOTE: DACKN low requires two rising edges of X1 clock after CSN is low.

Figure 3. Bus Timing (Write Cycle)



NOTE: DACKN low requires two rising edges of X1 clock after CSN is low.

Figure 4. Interrupt Cycle Timing

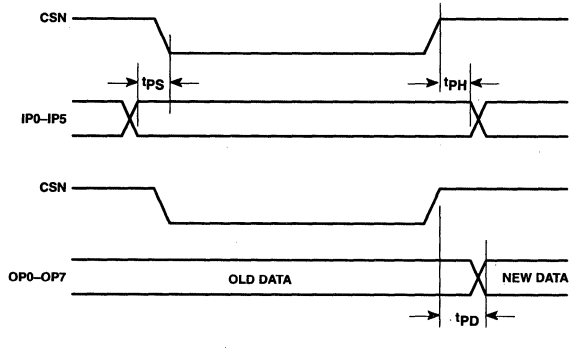
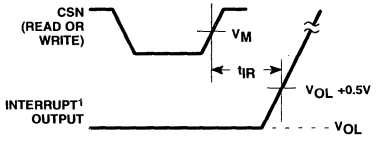


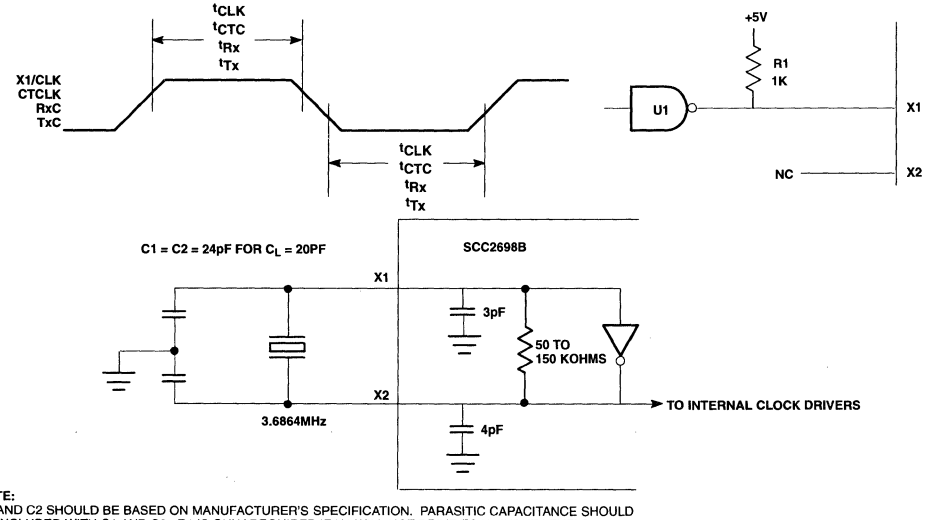
Figure 5. Port Timing



NOTES:

1. INTRN or OP3 – OP7 when used as interrupt outputs.
2. The test for open drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the mid point of the switching signal, V_M, to a point 0.5 volts above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 6. Interrupt Timing



NOTE:
C1 AND C2 SHOULD BE BASED ON MANUFACTURER'S SPECIFICATION. PARASITIC CAPACITANCE SHOULD BE INCLUDED WITH C1 AND C2. R1 IS ONLY REQUIRED IF U1 WILL NOT DRIVE TO X1 INPUT LEVELS

TYPICAL CRYSTAL SPECIFICATION

FREQUENCY:	**2 – 4MHZ**
LOAD CAPACITANCE (C_L):	**12 – 32pF**
TYPE OF OPERATION:	**PARALLEL RESONANT, FUNDAMENTAL MODE**

Figure 7. Clock Timing

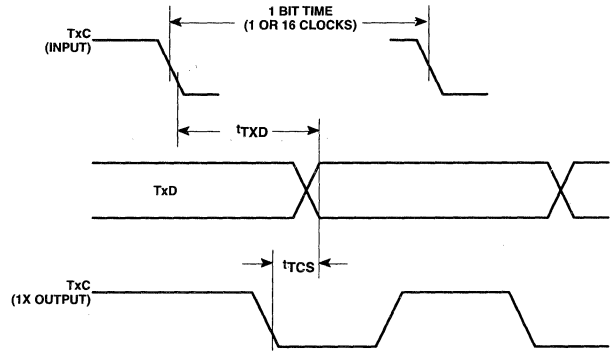


Figure 8. Transmit Timing

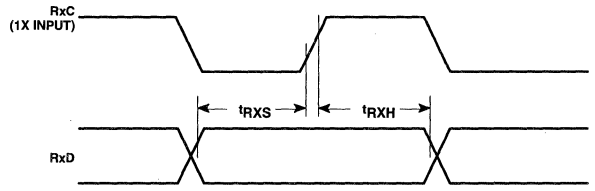
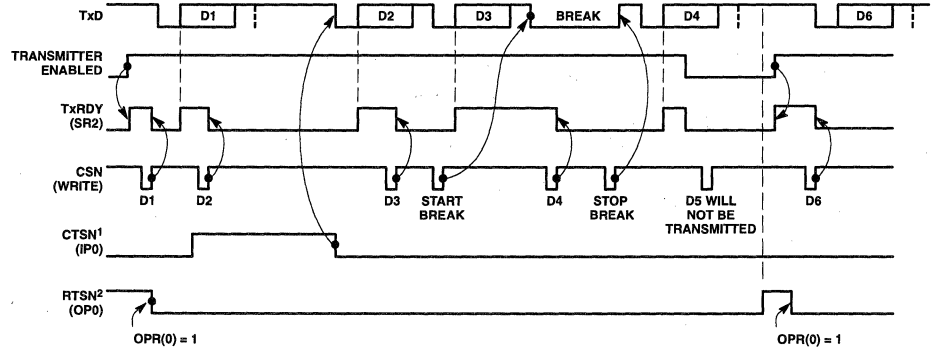
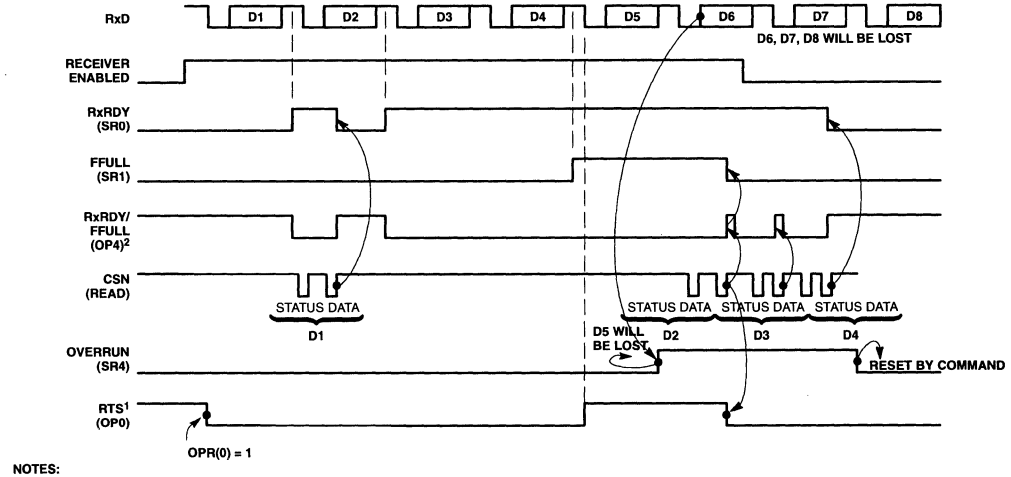


Figure 9. Receive Timing



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 10. Transmitter Timing



NOTES:
1. Timing shown for MR1(7) = 1.
2. Shown for OPCR(4) and MR1(6) = 0.

Figure 11. Receiver Timing

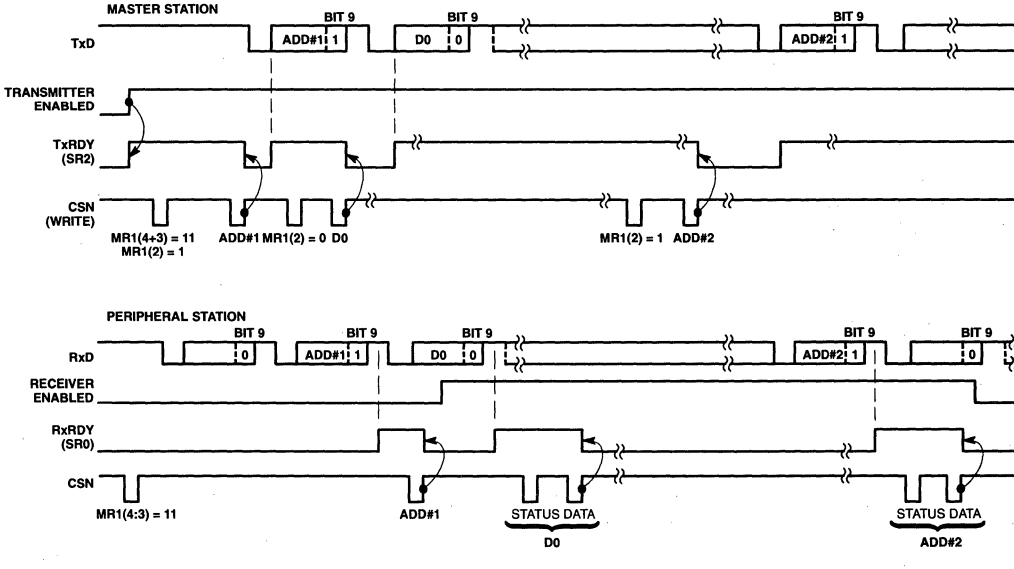


Figure 12. Wake-up Mode

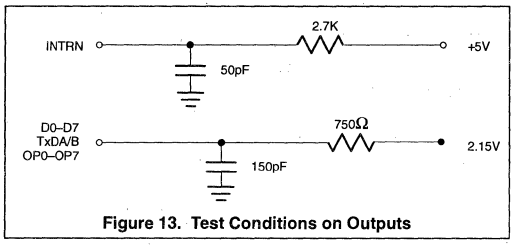


Figure 13. Test Conditions on Outputs

Output Port Notes

The output ports are controlled from four places: the OPCR register, the OPR register, the MR registers and the command register. The OPCR register controls the source of the data for the output ports OP2 through OP7. The data source for output ports OP0 and OP1 is controlled by the MR and CR registers. When the OPR is the source of the data for the output ports, the data at the ports is inverted from that in the OPR register. The content of the OPR register is controlled by the "Set Output Port Bits Command" and the "Reset Output Bits Command". These commands are at E and F, respectively. When these commands are used, action takes place only at the bit locations where ones exist. For example, a one in bit location 5 of the data word used with the "Set Output Port Bits" command will result in OPR5 being set to one. The OP5 would then be set to zero (V_{SS}). Similarly, a one in bit position 5 of the data word associated with the "Reset Output Ports Bits" command would set OPR5 to zero and, hence, the pin OP5 to a one (V_{DD}).

The CTS, RTS, CTS Enable Tx signals

CTS (Clear To Send) is usually meant to be a signal to the transmitter meaning that it may transmit data to the receiver. The CTS input is on pin MPI. The CTS signal is active low; thus, it is called CTS.

RTS is usually meant to be a signal from the receiver indicating that the receiver is ready to receive data. It is also active low and is, thus, called RTSN. RTSN is on pin MP0. A receiver's RTS output will usually be connected to the CTS input of the associated transmitter. Therefore, one could say that RTS and CTS are different ends of the same wire!

MR2(4) is the bit that allows the transmitter to be controlled by the CTS pin (MPI). When this bit is set to one AND the CTS input is driven high, the transmitter will stop sending data at the end of the present character being serialized. It is usually the RTS output of the receiver that will be connected to the transmitter's CTS input. The receiver will set RTS high when the receiver FIFO is full AND the start bit of the fourth character is sensed. Transmission then stops with four valid characters in the receiver. When MR2(4) is set to one, CTSN must be at zero for the transmitter to operate. If MR2(4) is set to zero, the MP pin will have no effect on the operation of the transmitter.

MR1(7) is the bit that allows the receiver to control MP0. When MP0 is controlled by the receiver, the meaning of that pin will be RTS. However, a point of confusion arises in that MP0 may also be controlled by the transmitter. When the transmitter is controlling this pin, its meaning is not RTS at all. It is, rather, that the transmitter has finished sending its last data byte. Programming the MP0 pin to be controlled by the receiver and the transmitter at the same time is allowed, but would usually be incompatible.

RTS can also be controlled by the commands 1000 and 1001 in the command register. RTS is expressed at the MP0 pin which is still an output port. Therefore, the state of MP0 should be set low (either by commands of the CR register or by writing to the Set Output Ports Register) for the receiver to generate the proper RTS signal. The logic at the output is basically a NAND of the MP0 bit register and the RTS signal as generated by the receiver. When the RTS flow control is selected via the MR(7) bit the state of the MP0 register is not changed. Terminating the use of "Flow Control" (via the MR registers) will return the MP0 pin to the control of the MP0 register.

Transmitter Disable Note

The sequence of instructions enable transmitter — load transmit holding register — disable transmitter will result in nothing being sent if the time between the end of loading the transmit holding register and the disable command is less that 3/16 bit time in the 16x mode or one bit time in the 1x mode. Also, if the transmitter, while in the enabled state and underrun condition, is immediately disabled after a single character is loaded to the transmit holding register, that character will not be sent.

In general, when it is desired to disable the transmitter before the last character is sent AND the TxEMT bit is set in the status register (TxEMT is always set if the transmitter has underrun or has just been enabled), be sure the TxRDY bit is active immediately before issuing the transmitter disable instruction. TxRDY sets at the end of the "start bit" time. It is during the start bit that the data in the transmit holding register is transferred to the transmit shift register.

Non-standard baud rates are available as shown in Table 5 below, via the BRG Test function.

Table 6. Baud Rate

	Normal BRG		BRG Test	
CSR[7:4]	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0000	50	75	4,800	7,200
0001	110	110	880	880
0010	134.5	134.5	1,076	1,076
0011	200	150	19.2K	14.4K
0100	300	300	28.8K	28.8K
0101	600	600	57.6K	57.6K
0110	1,200	1,200	115.2K	115.2K
0111	1,050	2,000	1,050	2,000
1000	2,400	2,400	57.6K	57.6K
1001	4,800	4,800	4,800	4,800
1010	7,200	1,800	57.6K	14.4K
1011	9,600	9,600	9,600	9,600
1100	38.4K	19.2K	38.4K	19.2K
1101	Timer	Timer	Timer	Timer
1110	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X
1111	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X

NOTE:
Each read on address H'A' will toggle the baud rate test mode. When in the BRG test mode, the baud rates change as shown to the left. This change affects all receivers and transmitters on the DUART. Also, the RTSN output (MP0) become the transmitter 1x clock.

The test mode at address H'2' changes all transmitters and receivers to the 1x mode and connects the output ports to some internal nodes.

A condition that occurs infrequently has been observed where the receiver will ignore all data. It is caused by a corruption of the start bit generally due to noise. When this occurs the receiver will appear to be asleep or locked up. The receiver must be reset for the UART to continue to function properly.

Reset in the Normal Mode (Receiver Enabled)

Recovery can be accomplished easily by issuing a receiver software reset followed by a receiver enable. All receiver data, status and programming will be preserved and available before reset. The reset will NOT affect the programming.

Reset in the Wake-Up Mode (MR1[4:3] = 11)

Recovery can also be accomplished easily by first exiting the wake-up mode (MR1[4:3] = 00 or 01 or 10), then issuing a receiver software reset followed by a wake-up re-entry (MR1[4:3] = 11). All receiver data, status and programming will be preserved and available before reset. The reset will NOT affect the programming.

The receiver has a digital filter designed to reject "noisy" data and the receiver state machine was designed to reject noisy start bits or noise that might be considered a start bit. In spite of these precautions, corruption of the start bit can occur in 15ns window approximately 100ns prior to the rising edge of the data clock. The probability of this occurring is less than 10^{-5} at 9600 baud.

A corrupted start bit may have some deleterious effects in ASYNC operation if it occurs within a normal data block. The receiver will tend to align its data clock to the next '0' bit in the data stream, thus potentially corrupting the remainder of the data block. A good design practice, in environments where start bit corruption is possible, is to monitor data quality (framing error, parity error, break change and received break) and "data stopped" time out periods. Time out periods can be enabled using the counter/timer in the SCC2691, SCC2692, SCC2698B and SC68692 products. This monitoring can indicate a potential start bit corruption problem.

SCC68692 differences from the SCN68681 AN415

Author: D. Ibarra

DESCRIPTION

The SCC68692 is a CMOS version of the SCN68681 DUART. The SCC68692 is functionally and pin-to-pin compatible with the SCN68681 and can be substituted into existing SCN68681 designs. There are a few additional features and differences in the SCC68692 which are discussed below.

The major difference between the two parts is that the SCC68692 is CMOS, while the SCN68681 is NMOS. This means the SCC68692 draws significantly less power than the SCN68681.

Another difference between the two parts is that the SCC68692 has used edge triggered latches for the configuration registers: MR1 MR2 CSR. OPCR and ACR. The SCN68681 uses transparent latches, gated by WRN AND CEN. So, because of the undefined state of the data bus prior to the data being valid, both the receiver and transmitter must be disabled before writing to any register which could affect them, even if the same data is being rewritten. The SCC68692 will not be affected by the undefined data and will allow, for example the transmitter configuration to be changed without affecting the receiver operation. Only the transmitter would have to be disabled for the following: changing the transmitted stop bit length; changing the value of the transmitted ninth bit during wake-up mode; and changing the clock source or value for the transmitter only. It is still recommended to disable the transmitter or receiver before changing their respective configurations.

SOFTWARE

The SCN68681 counter/timer will be in timer mode with the timer running after power up and and after a hardware reset. The SCC68692 counter/timer will also be in timer mode after power up and after a hardware reset, but the timer will not be running until it receives a start counter/timer command (read at address H'E'). After this initial start the SCC68692 timer will run continuously. Subsequent start C/T commands will cause either the SCC68692 or the SCN68681 to immediately load the values in the CTUR and CTLR and start a new cycle. The stop counter command will reset the counter ready status bit (ISR[3]), but will have no effect on the timer mode operation for either part.

Utilizing command register (CR) bit 7 which is an unused bit in the SCN68681 makes six additional commands available to the user. SCN68681 programs which set this bit to zero will not be affected by this change and will run with the SCC68692.

Timeout Mode

This mode is useful for when the user programs RxRDY to interrupt the CPU when the receive FIFO is full. When less than three characters are received, the FIFO won't become full and the CPU won't get an RxRDY interrupt. The timeout mode provides the user with a time out interrupt via the counter/timer. If characters are received and the FIFO does not become full, a preselected period of delay can be timed out by the counter/timer (C/T) and the CPU interrupted.

The counter/timer is used in this mode by programming CTUR/CTLR with a value greater than the normal receive character period. Each time a received character is transferred from the shift register to the receive holding register (RHR), the C/T is reloaded with the value in CTLR/CTUR and then restarted. If a continuous data stream is not received and the C/T is allowed to end the count, the counter ready bit ISR[3], will be set. If the interrupt mask, IMR[3], has been set, an interrupt will be generated. This mode is enabled by writing CR = H'A0', and is turned off by writing CR = H'C0'.

Power Down Mode

Power down mode can be used for energy conservation during idle periods. This mode saves the contents of all the internal registers, stops the oscillator and suspends the operation of any function that uses the oscillator. In addition, the current used by the part is reduced. The part can be put into power down mode at any time and restored to normal operation when needed. Since all register values are saved, re-initialization is not necessary.

To put the part into power down mode:

- CRA = H'30' — Reset Tx A
- CRA = H'20' — Reset Rx A
- CRB = H'30' — Reset Tx B
- CRB = H'20' — Reset Rx B
- CRA = H'E0' — power down mode on

To get out of power down mode:

- CRA – H'F0' -— Power down mode off
- Wait for oscillator to start up
- CRA = H'05' — Enable Rx A and Tx A
- CRB = H'05' — Enable Rx B and Tx B

Set/Reset RTSN Output

The RTSN output (OP0 and OP1) can be programmed to be asserted or negated automatically by either the receiver or the transmitter and it can be manually asserted and negated. Both the SCN68681 and the SCC68692 provide the ability to manually set and reset the output port bits by writing the appropriate bit mask to the Set output port bits command address or to the Reset output port bits command address (see data sheets for details). The SCC68692 as an additional feature provides commands in the CR to easily assert and negate just the RTSN output. CR H'80' will assert RTSN, cause the output to go low while CR = H'90' will negate RTSN, cause the output to go high.

HARDWARE

The on board oscillator circuitry in the SCC68692 is different from the SCN68681. This was required because of the addition of the power down mode logic. SCN68681 boards which use a crystal between the X1 and X2 pins with an equal value capacitor from X1 to ground as from X2 to ground can be used unmodified with the SCC68692. The SCC68692 does not require an external resistor but will operate with one there. SCN68681 boards which use an external oscillator to drive a signal into X1 and have X2 grounded can be used with the SCC68692.

The oscillators on both parts are the same basic type, consisting of an inverter and feedback resistor between the X1 and X2 pins, which, with the addition of an external crystal and capacitors, are used to implement a Pierce oscillator. The SCN68681 has the output of the inverter connected to X1, the input of the inverter connected to X2, and the inverter is a Schmitt trigger. The SCC68692 has the input of the inverter connected to X1 and the output of the inverter connected to X2.

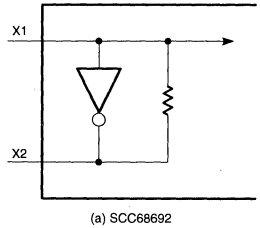
Because of the Schmitt trigger inverter, the SCN68681 is limited to using small value external capacitors. If capacitors of 15pF or greater are used, intermittent power–on problems may be experienced. The oscillator may stay in relaxation mode oscillating at a frequency much lower than the one the crystal is specified for. For this reason we recommend using external capacitors of around

SCC68692 differences from the SCN68681 AN415

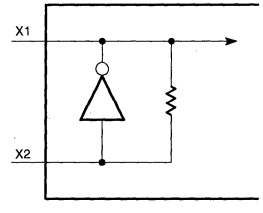
5pF and board supplied stray capacitance of no more than 5pF. It has also been found that adding an external resistor of 100k–1 MΩ across X1 and X2 will solve other start up problems for some designs. While we recommend using balanced capacitors (C1=C2) of 5pF, unbalanced values may be used. Since the X2 pin (input to the internal inverter) has the most sensitivity to capacitance, many designs use a larger value capacitor (10–15pF) on the X1 pin while leaving 5pF on the X2 pin.

The SCC68692 oscillator is not limited to the recommendations required for the SCN68681. It does not need an external resistor and will operate with a much wider range of external capacitor values. New designs using the SCC68692 oscillator should use a parallel calibrated crystal and the external capacitor values should be adjusted until the total circuit capacitance matches the capacitance specified for the crystal. The capacitor values are not limited to any specific value but the two capacitors should be approximately equal in value. Using two 24pF capacitors and a 3.6864MHz crystal with CL = 20pF will give accurate reliable results. A source for this crystal is: Saronix, Palo Alto, CA, part number NYP037–20. From California call (800) 422-3355; outside California call (800) 227-8974.

Some designs will not use the on board oscillator circuitry but will drive the part with an external clock source. The SCN68681 and the SCC68692 both require that the external clock be driven into the X1 pin. The SCN68681 requires that the X2 pin be grounded while the SCC68692 X2 pin can be grounded or left open. Alternately, the X2 input can be driven with the complement of the clock signal going to X1 for both parts.



(a) SCC68692



(b) SCN68681

Oscillator Configuration

Dual universal asynchronous receiver/transmitter (DUART) SC26C92

DESCRIPTION

The SC26C92 is a pin and function replacement for the SCC2692 with added features and deeper FIFOs. Its configuration on power up is that of the 2692. Its differences from the 2692 are: 8 character receiver, 8 character transmit FIFOs, watch dog timer for each receiver, mode register 0 is added, extended baud rate and overall faster speeds, programmable receiver and transmitter interrupts. (The SCC2692 is not being discontinued.)

The Philips Semiconductors SC26C92 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single-chip CMOS-LSI communications device that provides two full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver and transmitter is buffered by eight character FIFOs to minimize the potential of receiver overrun, transmitter underrun and to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote transmitter when the receiver buffer is full.

Also provided on the SC26C92 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The SC26C92 is available in two package versions: 40-pin 0.6" wide DIP and a 44-pin PLCC.

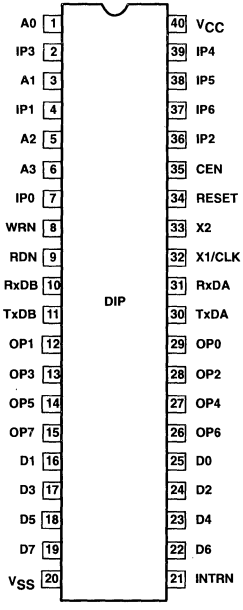
FEATURES

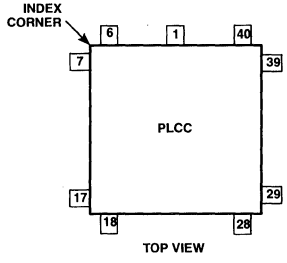
- Dual full-duplex independent asynchronous receiver/transmitters
- 8 character FIFOs for each receiver and transmitter
- Programmable data format
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Programmable baud rate for each receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4k baud
  - Other baud rates to 230.4k baud at 16X
  - Programmable user-defined rates derived from a programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex)
  - Automatic echo
  - Local loopback
  - Remote loopback
  - Multidrop mode (also called 'wake-up' or '9-bit')
- Multi-function 7-bit input port
  - Can serve as clock or control inputs
  - Change of state detection on four inputs
  - Inputs have typically >100k pull-up resistors
- Multi-function 8-bit output port
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
- Versatile interrupt system
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
  - Each FIFO can be programmed for four different interrupt levels
  - Watch dog timer for each receiver
- Maximum data transfer rates:
  1X – 1Mb/sec, 16X – 1Mb/sec
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- On-chip crystal oscillator
- Power down mode
- Receiver timeout mode
- Single +5V power supply
- Powers up to emulate SCC2692

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±10%, T_A = 0 to +70°C	DWG #
40-Pin Plastic Dual In-Line Package (DIP)	SC26C92C1N	0415C
44-Pin Plastic Leaded Chip Carrier (PLCC)	SC26C92C1A	0403G

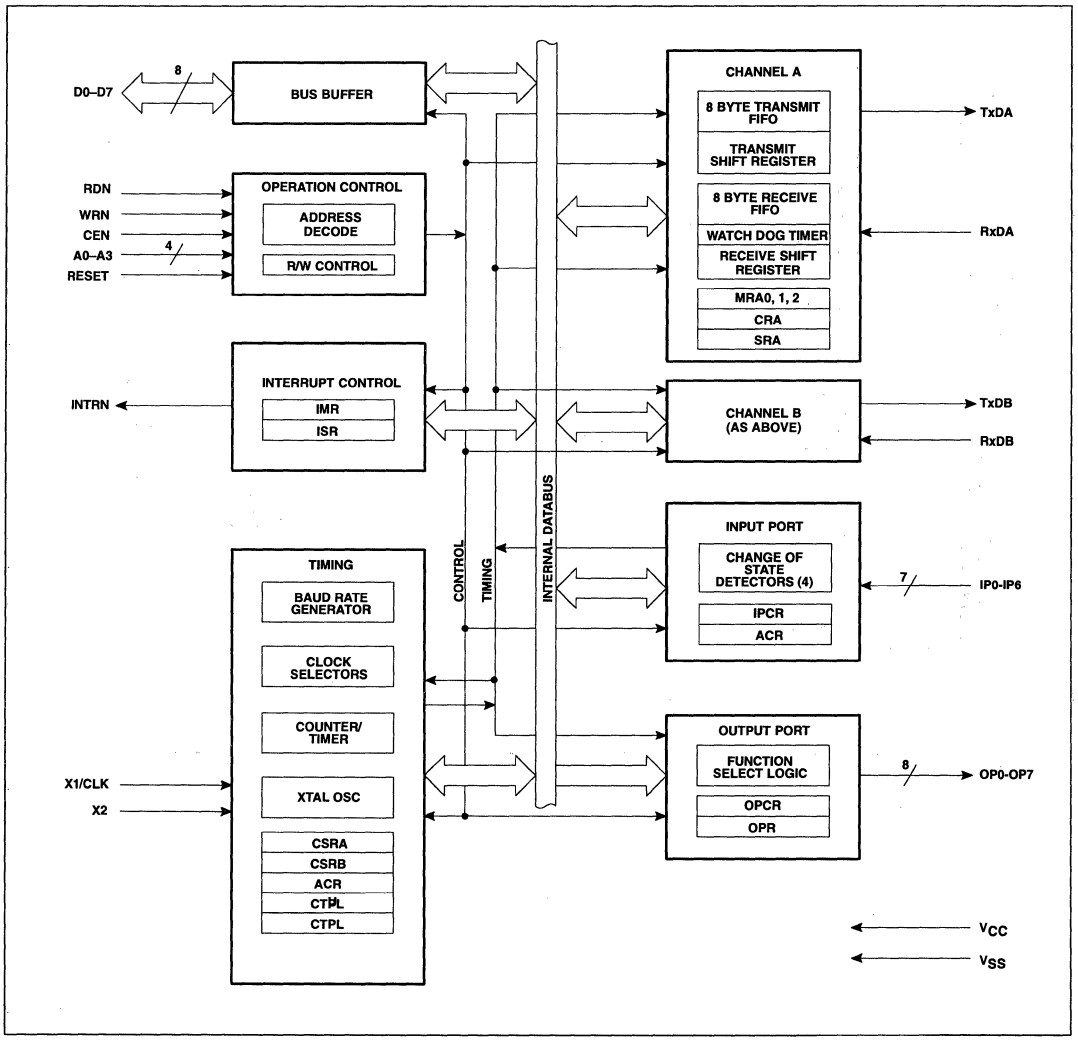
PIN CONFIGURATIONS





PIN/FUNCTION		PIN/FUNCTION	
1	NC	23	NC
2	A0	24	INTRN
3	IP3	25	D6
4	A1	26	D4
5	IP1	27	D2
6	A2	28	D0
7	A3	29	OP6
8	IP0	30	OP4
9	WRN	31	OP2
10	RDN	32	OP0
11	RXDB	33	TXDA
12	NC	34	NC
13	TXDB	35	RXDA
14	OP1	36	X1/CLK
15	OP3	37	X2
16	OP5	38	RESET
17	OP7	39	CEN
18	D1	40	IP2
19	D3	41	IP6
20	D5	42	IP5
21	D7	43	IP4
22	V_{SS}	44	V_{CC}

BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PKG 40,44	PIN TYPE	NAME AND FUNCTION
D0-D7	X	I/O	**Data Bus:** Bidirectional 3-State data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	X	I	**Chip Enable:** Active-Low input signal. When Low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A3 inputs. When High, places the D0-D7 lines in the 3-State condition.
WRN	X	I	**Write Strobe:** When Low and CEN is also Low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	X	I	**Read Strobe:** When Low and CEN is also Low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0-A3	X	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	X	I	**Reset:** A High level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0-OP7 in the High state, stops the counter/timer, and puts Channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (High) state. Sets MR pointer to MR1.
INTRN	X	O	**Interrupt Request:** Active-Low, open-drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	X	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5).
X2	X	I	**Crystal 2:** Connection for other side of the crystal. When a crystal is used, a capacitor must be connected from this pin to ground (see Figure 5). If X1/CLK is driven from an external source, this pin must be left open.
RxDA	X	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
RxDB	X	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. "Mark" is High, "space" is Low.
TxDA	X	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the "mark" condition when the transmitter is disabled, idle or when operating in local loopback mode. "Mark" is High, "space" is Low.
TxDB	X	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is High, 'space' is Low.
OP0	X	O	**Output 0:** General purpose output or Channel A request to send (RTSAN, active-Low). Can be deactivated automatically on receive or transmit.
OP1	X	O	**Output 1:** General purpose output or Channel B request to send (RTSBN, active-Low). Can be deactivated automatically on receive or transmit.
OP2	X	O	**Output 2:** General purpose output, or Channel A transmitter 1X or 16X clock output, or Channel A receiver 1X clock output.
OP3	X	O	**Output 3:** General purpose output or open-drain, active-Low counter/timer output or Channel B transmitter 1X clock output, or Channel B receiver 1X clock output.
OP4	X	O	**Output 4:** General purpose output or Channel A open-drain, active-Low, RxA interrupt ISR[1] output.
OP5	X	O	**Output 5:** General purpose output or Channel B open-drain, active-Low, RxB interrupt ISR[5] output.
OP6	X	O	**Output 6:** General purpose output or Channel A open-drain, active-Low, TxA interrupt ISR[0] output.
OP7	X	O	**Output 7:** General purpose output, or Channel B open-drain, active-Low, TxB interrupt ISR[4] output.
IP0	X	I	**Input 0:** General purpose input or Channel A clear to send active-Low input (CTSAN).
IP1	X	I	**Input 1:** General purpose input or Channel B clear to send active-Low input (CTSBN).
IP2	X	I	**Input 2:** General purpose input or counter/timer external clock input.
IP3	X	I	**Input 3:** General purpose input or Channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	X	I	**Input 4:** General purpose input or Channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	X	I	**Input 5:** General purpose input or Channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	X	I	**Input 6:** General purpose input or Channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	X	I	**Power Supply:** +5V supply input.
GND	X	I	**Ground**

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	Note 4	°C
T_{STG}	Storage temperature range	-65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	-0.5 to +7.0	V
V_S	Voltage from any pin to GND[3]	-0.5 to V_{CC} +0.5	V
P_D	Power dissipation[5]	750	mW

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. Maximum power dissipation of the chip when outputs are loaded externally. For operating current, see DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)[6]		2.4			V
V_{IH}	Input high voltage (X1/CLK)		0.8 V_{CC}			V
V_{OL}	Output low voltage	I_{OL} = 2.4mA			0.4	V
V_{OH}	Output high voltage (except OD outputs)[4]	I_{OH} = -400µA	V_{CC} -0.5			V
I_{IX1PD}	X1/CLK input current - power down	V_{IN} = 0 to V_{CC}	-1		+1	µA
I_{ILX1}	X1/CLK input low current - operating	V_{IN} = 0	-100		0	µA
I_{IHX1}	X1/CLK input high current - operating	V_{IN} = V_{CC}	0		100	µA
I_I	Input leakage current:					
	All except input port pins	V_{IN} = 0 to V_{CC}	-1		+1	µA
	Input port pins	V_{IN} = 0 to V_{CC}	-10		+10	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			1	µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0V	–1			µA
I_{ODL}	Open-drain output low current in off-state	V_{IN} = 0	–1			µA
I_{ODH}	Open-drain output high current in off-state	V_{IN} = V_{CC}			1	µA
I_{CC}	Power supply current[5]					
	Operating mode	CMOS input levels			25	mA
	Power down mode[7]	CMOS input levels			5.0	mA

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 3.0V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7KΩ to V_{CC}.
5. All outputs are disconnected. Inputs are switching between CMOS levels of V_{CC} -0.2V and V_{SS} + 0.2V.
6. WRN may reach 2.58V in most environments.
7. See UART application note for power down currents of 5µA or less.

AC CHARACTERISTICS[1, 2, 4]

SYMBOL	PARAMETER	LIMITS Min	LIMITS Typ[3]	LIMITS Max	UNIT
Reset Timing (See Figure 1)					
t_{RES}	RESET pulse width	200			ns
Bus Timing[5] (See Figure 2)					
t_{AS}	A0-A3 setup time to RDN, WRN Low	10			ns
t_{AH}	A0-A3 hold time from RDN, WRN Low	45			ns
t_{CS}	CEN setup time to RDN, WRN Low	0			ns
t_{CH}	CEN hold time from RDN, WRN High	0			ns
t_{RW}	WRN, RDN pulse width	110			ns
t_{DD}	Data valid after RDN Low			90	ns
t_{DA}	RDN Low to data bus active[7]	0			ns
t_{DF}	Data bus floating after RDN High			30	ns
t_{DI}	RDN High to data bus invalid[7]	0			ns
t_{DS}	Data setup time before WRN High	75			ns
t_{DH}	Data hold time after WRN High	8			ns
t_{RWD}	High time between reads and/or writes[5, 6]	55			ns
Port Timing[5] (See Figure 3)					
t_{PS}	Port input setup time before RDN Low	0			ns
t_{PH}	Port input hold time after RDN High	0			ns
t_{PD}	OP_n output valid from WRN High			110	ns
Interrupt Timing (See Figure 4)					
t_{IR}	INTRN (or OP3-OP7 when used as interrupts) negated from:				
	Read RxFIFO (RxRDY/FFULL interrupt)			100	ns
	Write TxFIFO (TxRDY interrupt)			100	ns
	Reset command (break change interrupt)			100	ns
	Stop C/T command (counter interrupt)			100	ns
	Read IPCR (input port change interrupt)			100	ns
	Write IMR (clear of interrupt mask bit)			100	ns
Clock Timing (See Figure 5)					
t_{CLK}	X1/CLK High or Low time	80			ns
f_{CLK}	X1/CLK frequency	2	3.6864	4	MHz
t_{CTC}	CTCLK (IP2) High or Low time	55			ns
f_{CTC}	CTCLK (IP2) frequency[8]	0		8	MHz
t_{RX}	RxC High or Low time (16X)	30			ns
f_{RX}	RxC frequency (16X)[8]	0		16	MHz
	(1X)[8, 9]	0		1	MHz
t_{TX}	TxC High or Low time (16X)	30			ns
f_{TX}	TxC frequency (16X)[8]	0		16	MHz
	(1X)[8, 9]	0		1	MHz
Transmitter Timing (See Figure 6)					
t_{TXD}	TxD output delay from TxC Low (TxC input pin)			120	ns
t_{TCS}	Output delay from TxC Low to TxD data output (TxC 1x output pin)	–30		30	ns
Receiver Timing (See Figure 7)					
t_{RXS}	RxD data setup time to RxC High	100			ns
t_{RXH}	RxD data hold time from RxC High	100			ns

NOTES:

1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 3.0V with a transition time of 5ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of 0.8V and 2.0V and output voltages of 0.8V and 2.0V, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test conditions for outputs: C_L = 150pF, except interrupt outputs. Test conditions for interrupt outputs: C_L = 50pF, R_L = 2.7KΩ to V_{CC}.
5. Timing is illustrated and referenced to the WRN and RDN inputs. Also, CEN may be the 'strobing' input. CEN and RDN (also CEN and WRN) are ORed internally. The signal asserted last initiates the cycle and the signal negated first terminates the cycle.
6. If CEN is used as the 'strobing' input, the parameter defines the minimum High times between one CEN and the next. The RDN signal must be negated for t_{RWD} to guarantee that any status register changes are valid.
7. Guaranteed by characterization of sample units.
8. Minimum frequencies are not tested but are guaranteed by design.
9. Clocks for 1X mode should be symmetrical.

Block Diagram

The SC26C92 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications Channels A and B, input port and output port. Refer to the Block Diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer.

Interrupt Control

A single active-Low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR). The IMR can be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions.

Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer.

When OP3 to OP7 are programmed as interrupts, their output buffers are changed to the open drain active low configuration.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the Baud Rate Generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

If an external is used instead of a crystal, X1 should be driven using a configuration similar to the one in Figure 5.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. Programming bit 0 of MR0 to a "1" gives additional baud rates of 57.6kB, 115.2kB and 230.4kB. These will be in the 16X mode. A 3.6864MHz crystal or external clock must be used to get the standard baud rate. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal.

The Counter/Timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the SC26C92 comprises a full-duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU via the receive FIFO. Three status bits (Break, Framing and Parity Errors) are also FIFOed with each data character.

Input Port

The inputs to this unlatched 7-bit port can be read by the CPU by performing a read operation at address H'D'. A High input results in a logic 1 while a Low input results in a logic 0. D7 will always read as a logic 1. The pins of this port can also serve as auxiliary inputs to certain portions of the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs, lasting longer than 25 - 50µs, will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU.

The input port pulse detection circuitry uses a 38.4KHz sampling clock derived from one of the baud rate generator taps. This results in a sampling period of slightly more than 25µs (this assumes that the clock input is 3.6864MHz). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples at the new logic level be observed. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs "coincident with the first sample pulse". The 50µs time refers to the situation in which the change-of-state is "just missed" and the first change-of-state is not detected until 25µs later.

Output Port

The output port pins may be controlled by the OPR, OPCR, MR and CR registers. Via appropriate programming they may be just another parallel port to external circuits, or they may represent many internal conditions of the UART. When this 8-bit port is used as a general purpose output port, the output port pins drive a state which is the complement of the Output Port Register (OPR). The OPR register is set and reset by writing to the SOPR and ROPR addresses. (See the description of the SOPR and ROPR registers). The output pins will drive the inverse data polarity of the OPR registers. The OPCR register conditions these output pins to be controlled by the OPR or by other signals in the chip. Output ports are driven high on hardware reset.

OPERATION

Transmitter

The SC26C92 is conditioned to transmit data when the transmitter is enabled through the command register. The SC26C92 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When the transmitter is initially enabled the TxRDY and TxEMPTY bits will be set in the status register. When a character is loaded to the transmit FIFO the TxEMPTY bit will be reset. The TxEMPTY will not set until:

1) the transmit FIFO is empty and the transmit shift register has finished transmitting the stop bit of the last character written to the transmit FIFO, or 2) the transmitter is disabled and then re-enabled. The TxRDY bit is set whenever the transmitter is enabled and the TxFIFO is not full. Data is transferred from the holding register to transmit shift register when it is idle or has completed transmission of the previous character. Characters cannot be loaded into the TxFIFO while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the TxFIFO, the TxD output remains High and the TxEMT bit in the Status Register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the TxFIFO.

If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous Low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS option is enabled (MR2[4] = 1), the CTS input at IP0 or IP1 must be Low in order for the character to be transmitted. The transmitter will check the state of the CTS input at the beginning of each character transmitted. If it is found to be High, the transmitter will delay the transmission of any following characters until the CTS has returned to the low state. CTS going high during the serialization of a character will not affect that character.

The transmitter can also control the RTSN outputs, OP0 or OP1 via MR2[5]. When this mode of operation is set, the meaning of the OP0 or OP1 signals will usually be 'end of message'. See description of the MR2[5] bit for more detail.

Receiver

The SC26C92 is conditioned to receive data when enabled through the command register. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive FIFO and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than 8 bits, the most significant unused bits in the RxFIFO are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains Low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is Low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RxFIFO and the received break bit in the SR is set to 1. The RxD input must return to a High condition for at least one-half bit time before a search for the next start bit begins.

Receiver FIFO

The RxFIFO consists of a First-In-First-Out (FIFO) stack with a capacity of eight characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all eight stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RxFIFO outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical-OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RxFIFO is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected; the character previously in the shift register is lost and the overrun error status bit (SR[4] will be set-upon receipt of the start bit of the new (overrunning) character).

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

Receiver Reset and Disable

Receiver disable stops the receiver immediately – data being assembled in the receiver shift register is lost. Data and status in the FIFO is preserved and may be read. A re-enable of the receiver after a disable will cause the receiver to begin assembling characters at the next start bit detected. A receiver reset will discard the present shift register date, reset the receiver ready bit (RxRDY), clear the status of the byte at the top of the FIFO and re-align the FIFO read/write pointers.

A 'watchdog timer' is associated with each receiver. Its interrupt is enabled by MR0[7]. The purpose of this timer is to alert the control processor that characters are in the RxFIFO which have not been read and/or the data stream has stopped. This situation may occur

at the end of a transmission when the last few characters received are not sufficient to cause an interrupt.

This counter times out after 64 bit times. It is reset each time a character is transferred from the receiver shift register to the RxFIFO or a read of the RxFIFO is executed.

Receiver Timeout Mode

In addition to the watch dog timer described in the receiver section, the counter/timer may be used for a similar function. Its programmability, of course, allows much greater precision of time out intervals.

The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RxFIFO, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the RxFIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know there is data left in the FIFO. The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

The timeout mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. The timeout mode should only be used by one channel at once, since it uses the C/T. If, however, the timeout mode is enabled from both receivers, the timeout will occur only when **both** receivers have stopped receiving data for the timeout period. CTU and CTL must be loaded with a value greater than the normal receive character period. The timeout mode disables the regular START/STOP Counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RxFIFO, the C/T is stopped after 1 C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Receiving a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx = 'Ax', will also clear the counter ready bit and stop the counter until the next character is received.

Pauses in data longer than the timeout period but shorter than the longest interrupt latency time may cause the ISR[3] bit to be reset before the interrupt is serviced. This will appear to be an "interrupt without a cause" which is indicated by a '0' in the ISR after the interrupt has been generated.

Multidrop Mode (9-bit or Wake-Up)

The DUART is equipped with a wake up mode for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for Channels A and B, respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wakeup' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, and Address/Data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the TxFIFO.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RxFIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RxFIFO. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receive is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems.

For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Each channel has 3 mode registers (MR0, 1, 2) which control the basic configuration of the channel. Access to these registers is controlled by independent MR address pointers. These pointers are set to 0 or 1 by MR control commands in the command register "Miscellaneous Commands". Each time the MR registers are accessed the MR pointer increments, stopping at MR2. It remains pointing to MR2 until set to 0 or 1 via the miscellaneous commands of the command register. The pointer is set to 1 on reset for compatibility with previous Philips Semiconductors UART software.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H'02' and H'0A' should never be read during normal operation since they are reserved for internal diagnostics.

Table 1. SC26C92 Register Addressing

A3	A2	A1	A0	READ (RDN = 0)	WRITE (WRN = 0)
0	0	0	0	Mode Register A (MR0A, MR1A, MR2A)	Mode Register A (MR0A, MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Register A (CSRA)
0	0	1	0	Reserved	Command Register A (CRA)
0	0	1	1	Rx Holding Register A (RxFIFOA)	Tx Holding Register A (TxFIFOA)
0	1	0	0	Input Port Change Register (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Preset Register (CTPU)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Preset Register (CTPL)
1	0	0	0	Mode Register B (MR0B, MR1B, MR2B)	Mode Register B (MR0B, MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Register B (CSRB)
1	0	1	0	Reserved	Command Register B (CRB)
1	0	1	1	Rx Holding Register B (RxFIFOB)	Tx Holding Register B (TxFIFOB)
1	1	0	0	Reserved	Reserved
1	1	0	1	Input Port (IPR)	Output Port Conf. Register (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command (SOP12)
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command (ROP12)

NOTE:
The three MR Registers are accessed via the MR Pointer and Commands 1xh and Bxh. (Where "x" represents receiver and transmitter enable/disable control)

The following named registers are the same for Channels A and B			
Mode Register	MRnA	MRnB	R/W
Status Register	SRA	SRB	R only
Clock Select	CSRA	CSRB	W only
Command Register	CRA	CRB	W only
Receiver FIFO	RxFIFOA	RxFIFOB	R only
Transmitter FIFO	TxFIFOA	TxFIFOB	W only

These registers control the functions which service both Channels		
Input Port Change Register	IPCR	R
Auxiliary Control Register	ACR	W
Interrupt Status Register	ISR	R
Interrupt Mask Register	IMR	W
Counter Timer Upper Value	CTU	R
Counter Timer Lower Value	CTL	R
Counter Timer Preset Upper	CTPU	W
Counter Timer Preset Lower	CTPL	W
Input Port Register	IPR	R
Output Configuration Register	OPCR	W
Set Output Port Bits	SOPR	W
Reset Output Port Bits	ROPR	W

Table 2. Register Bit Formats

	BIT 7	BIT 6	BIT 5 BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MR0A MR0B	Rx WATCH DOG	RxINT BIT 2	TxINT (1:0)	DON'T CARE	BAUD RATE EXTENDED II	TEST 2	BAUD RATE EXTENDED 1
MR0B[3:0] are reserved	0 = Disable 1 = Enable			Set to 0	0 = Normal 1 = Extend II	Set to 0	0 = Normal 1 = Extend

	BIT 7	BIT 6	BIT 5	BIT 4 BIT 3	BIT 2	BIT 1 BIT 0
MR1A MR1B	Rx CONTROLS RTS	Rx INT BIT 1	ERROR MODE	PARITY MODE	PARITY TYPE	BITS PER CHARACTER
	0 = No 1 = Yes	0 = RxRDY 1 = FFULL	0 = Char 1 = Block	00 = With Parity 01 = Force Parity 10 = No Parity 11 = Multidrop Mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

	BIT 7 BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MR2A MR2B	CHANNEL MODE	Tx CONTROLS RTS	CTS ENABLE Tx	STOP BIT LENGTH*			
	00 = Normal 01 = Auto-Echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

NOTE: *Add 0.5 to values shown for 0 – 7 if channel is programmed for 5 bits/char.

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CSRA CSRB	RECEIVER CLOCK SELECT				TRANSMITTER CLOCK SELECT			
	See Text				See Text			

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CRA CRB	MISCELLANEOUS COMMANDS*				DISABLE Tx	ENABLE Tx	DISABLE Rx	ENABLE Rx
	See Text				0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE: Access to the miscellaneous commands should be separated by 3 X1 clock edges. A disabled transmitter cannot be loaded.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SRA SRB	RECEIVED BREAK*	FRAMING ERROR*	PARITY ERROR*	OVERRUN ERROR	TxEMT	TxRDY	FFULL	RxRDY
	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE: *These status bits are appended to the corresponding data character in the receive FIFO. A read of the status provides these bits (7:5) from the top of the FIFO together with bits (4:0). These bits are cleared by a "reset error status" command. In character mode they are discarded when the corresponding data character is read from the FIFO.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3 BIT 2	BIT 1 BIT 0
OPCR	OP7	OP6	OP5	OP4	OP3	OP2
	0 = OPR[7] 1 = TxRDYB	0 = OPR[6] 1 = TxRDYA	0 = OPR[5] 1 = RxRDY/ FFULLB	0 = OPR[4] 1 = RxRDY/ FFULLA	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB(1X) 11 = RxCB(1X)	00 = OPR[2] 01 = TxCA(16X) 10 = TxCA(1X) 11 = RxCA(1X)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SOPR	See Note	See Note	See Note	See Note	See Note	See Note	See Note	See Note

NOTE: 0 = No Change; 1 = Set

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ROPR	See Note	See Note	See Note	See Note	See Note	See Note	See Note	See Note

NOTE: 0 = No Change; 1 = Reset

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OPR	OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0
	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low	0 = Pin High 1 = Pin Low

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ACR	BRG SET SELECT	COUNTER/TIMER MODE AND SOURCE			DELTA IP 3 INT	DELTA IP 2 INT	DELTA IP 1 INT	DELTA IP 0 INT
	0 = set 1 1 = set 2	See Table 4			0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IPCR	DELTA IP 3	DELTA IP 2	DELTA IP 1	DELTA IP 0	IP 3	IP 2	IP 1	IP 0
	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ISR	INPUT PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	COUNTER READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA
	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

Table 2. Register Bit Formats (Continued)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IMR	IN. PORT CHANGE INT	DELTA BREAK B INT	RxRDY/ FFULLB INT	TxRDYB INT	COUNTER READY INT	DELTA BREAK A INT	RxRDY/ FFULLA INT	TxRDYA INT
	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On	0 = Off 1 = On

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CTPU	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CTPL	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]

REGISTER DESCRIPTIONS Mode Registers

MR0 is accessed by setting the MR pointer to 0 via the command register command B.

MR0A

MR0[7] – This bit controls the receiver watch dog timer. 0 = disable, 1 = enable. When enabled, the watch dog timer will generate a receiver interrupt if the receiver FIFO has not been accessed within 64 bit times of the receiver 1X clock. This is used to alert the control processor that data is in the RxFIFO that has not been read. This situation may occur when the byte count of the last part of a message is not large enough to generate an interrupt.

MR0[6] – Bit 2 of receiver FIFO interrupt level. This bit along with Bit 6 of MR1 sets the fill level of the 8 byte FIFO that generates the receiver interrupt.

MR0[6]	MR1[6]	Interrupt Condition
0	0	1 or more bytes in FIFO (Rx RDY)
0	1	3 or more bytes in FIFO
1	0	6 or more bytes in FIFO
1	1	8 bytes in FIFO (Rx FULL)

MR0[5:4] – Tx interrupt fill level.

MR0[5]	MR0[4]	Interrupt Condition
0	0	8 bytes empty (Tx EMPTY)
0	1	4 or more bytes empty
1	0	6 or more bytes empty
1	1	1 or more bytes empty (Tx RDY)

MR0[3] – Not used. Should be set to 0.

MR0[2:0] – These bits are used to select one of the six baud rates (see Table 3).

000 Normal mode
001 Extended mode I
100 Extended mode II

Other combinations should not be used

Note: MR0[3:0] are not used in channel B and should be set to 0.

MR1A

MR1A is accessed when the Channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CR command 1. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7] – Channel A Receiver Request-to-Send Control (Flow Control)

This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0].

MR1A[7] = 1 causes RTSAN to be negated (OP0 is driven to a '1' [V_{CC}]) upon receipt of a valid start bit if the Channel A FIFO is full. This is the beginning of the reception of the ninth byte. If the FIFO is not read before the start of the tenth byte, an overrun condition will occur and the tenth byte will be lost. However, the bit in OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1[6] – Bit 1 of the receiver interrupt control. See description under MR0[6].

MR1A[5] – Channel A Error Mode Select

This bit select the operating mode of the three FIFOed status bits (FE, PE, received break) for Channel A. In the 'character' mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for Channel A was issued.

MR1A[4:3l – Channel A Parity Mode Select

If 'with parity' or 'force parity' is selected a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data MR1A[4:3] = 11 selects Channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] – Channel A Parity Type Select

This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no

parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] – Channel A Bits Per Character Select
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2A – Channel A Mode Register 2

MR2A is accessed when the Channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] – Channel A Mode Select
Each channel of the DUART can operate in one of four modes.
MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently.
MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The Channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e. transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held High.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop has been re-transmitted.

MR2A[5] – Channel A Transmitter Request-to-Send Control
This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0].
MR2A[5] = 1 caused OPR[0] to be reset automatically one bit time after the characters in the Channel A transmit shift register and in the TxFIFO, if any, are completely transmitted including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Asset RTSAN: OPR[0] = 1.
4. Send message.
5. Disable transmitter after the last character is loaded into the Channel A TxFIFO.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

MR2A[4] – Channel A Clear-to-Send Control
If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IPO) each time it is ready to send a character. If IPO is asserted (Low), the character is transmitted. If it is negated (High), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character..

MR2A[3:0] – Channel A Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character lengths of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a 'mark' condition at the center of the stop bit position (one bit time after the last data bit, or after the parity bit if enabled is sampled).

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

MR0B – Channel B Mode Register 0

MR0B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR0 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR0B, the pointer will point to MR1B.

The bit definitions for this register are identical to MR0A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs. MR0B[3:0] are reserved.

MR1B – Channel B Mode Register 1

MR1B is accessed when the Channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to MR1A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

MR2B – Channel B Mode Register 2

MR2B is accessed when the Channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for mode register are identical to the bit definitions for MR2A, except that all control actions apply to the Channel B receiver and transmitter and the corresponding inputs and outputs.

CSRA – Channel A Clock Select Register

CSRA[7:4] – Channel A Receiver Clock Select

This field selects the baud rate clock for the Channel A transmitter. The field definition is shown in Table 3.

CSRA[3:0] – Channel A Transmitter Clock Select

This field selects the baud rate clock for the Channel A transmitter. The field definition is as shown in Table 3, except as follows:

CSRA[3:0]	ACR[7] = 0	ACR[7] = 1
1110	IP3-16X	IP3-16X
1111	IP3-1X	IP3-1X

The transmitter clock is always a 16X clock except for CSR[3:0] = 1111.

CSRB – Channel B Clock Select Register

CSRB[7:4] – Channel B Receiver Clock Select

This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

CSRB[7:4]	ACR[7] = 0	ACR[7] = 1
1110	IP6-16X	IP6-16X
1111	IP6-1X	IP6-1X

The transmitter clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0] – Channel B Transmitter Clock Select

This field selects the baud rate clock for the Channel B transmitter. The field definition is as shown in Table 3, except as follows:

CSRB[3:0]	ACR[7] = 0	ACR[7] = 1
1110	IP5-16X	IP5-16X
1111	IP5-1X	IP5-1X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

CRA – Channel A Command Register

CRA is a register used to supply commands to Channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

CRA[7:4] – Miscellaneous Commands

Execution of the commands in the upper four bits of this register must be separated by 3 X1 clock edges. Other reads or writes (including writes tot he lower four bits) may be inserted to achieve this separation.

CRA[7:4] – Command

0000 No command.

0001 Reset MR pointer. Causes the Channel A MR pointer to point to MR1.

Table 3. Baud Rate

CSRA[7:4]	MR0[0] = 0 (Normal Mode)		MR0[0] = 1 (Extended Mode I)		MR0[2] = 1 (Extended Mode II)	
	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0000	50	75	50	450	4,800	7,200
0001	110	110	110	110	880	880
0010	134.5	134.5	134.5	134.5	1,076	1,076
0011	200	150	200	900	19.2K	14.4K
0100	300	300	1800	1800	28.8K	38.4K
0101	600	600	3600	3600	57.6K	57.6K
0110	1,200	1,200	7200	7,200	115.2K	115.2
0111	1,050	2,000	1,050	2,000	1,050	2,000
1000	2,400	2,400	14.4K	14.4K	57.6K	57.6K
1001	4,800	4,800	28.8K	28.8K	4,800	4,800
1010	7,200	1,800	7,200	1,800	57.6K	14.4K
1011	9,600	9,600	57.6K	57.6K	9,600	9,600
1100	38.4K	19.2K	230.4K	115.2K	38.4K	19.2K
1101	Timer	Timer	Timer	Timer	Timer	Timer
1110	IP4-16X	IP4-16X	IP4-16X	IP4-16X	IP4-16X	IP4-16X
1111	IP4-1X	IP4-1X	IP4-1X	IP4-1X	IP4-1X	IP4-1X

NOTE: The receiver clock is always a 16X clock except for CSRA[7:4] = 1111.

0010 Reset receiver. Resets the Channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.
0011 Reset transmitter. Resets the Channel A transmitter as if a hardware reset had been applied.
0100 Reset error status. Clears the Channel A Received Break, Parity Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.
0101 Reset Channel A break change interrupt. Causes the Channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.
0110 Start break. Forces the TxDA output Low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the TxFIFO, the start of the break will be delayed until that character, or any other loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.
0111 Stop break. The TxDA line will go High (marking) within two bit times. TxDA will remain High for one bit time before the next character, if any, is transmitted.
1000 Assert RTSN. Causes the RTSN output to be asserted (Low).
1001 Negate RTSN. Causes the RTSN output to be negated (High).
1010 Set Timeout Mode On. The receiver in this channel will restart the C/T as each receive character is transferred from the shift register to the RxFIFO. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset. (See also Watchdog timer description in the receiver section.)
1011 Set MR pointer to '0'
1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued to force a reset of the ISR(3) bit.
1101 Not used.
1110 Power Down Mode On. In this mode, the DUART oscillator is stopped and all functions requiring this clock are suspended. The execution of commands other than disable power down mode (1111) requires a X1/CLK. While in the power down mode, do not issue any commands to the CR except the disable power down mode command. The contents of all registers will be saved while in this mode. . It is recommended that the transmitter and receiver be disabled prior to placing the DUART into power down mode. This command is in CRA only. For maximum power reduction input pins should be at V_{SS} or V_{DD}.
1111 Disable Power Down Mode. This command restarts the oscillator. After invoking this command, wait for the oscillator to start up before writing further commands to the CR. This command is in CRA only.

CRA[3] – Disable Channel A Transmitter
This command terminates transmitter operation and reset the TxDRY and TxEMT status bits. However, if a character is being transmitted or if a character is in the TxFIFO when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2] – Enable Channel A Transmitter
Enables operation of the Channel A transmitter. The TxRDY and TxEMT status bits will be asserted if the transmitter is idle.

CRA[1] – Disable Channel A Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] – Enable Channel A Receiver
Enables operation of the Channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start-bit state.

CRB – Channel B Command Register

CRB is a register used to supply commands to Channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, with the exception of commands "Ex" and "Fx" which are used for power downmode. These two commands are not used in CRB. All other control actions that apply to CRA also apply to CRB.

SRA – Channel A Status Register

SRA[7] – Channel A Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line returns to the marking state for at least one-half a bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the Channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

This bit is reset by command 4 (0100) written to the command register or by receiver reset.

SRA[6] – Channel A Framing Error
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SRA[5] – Channel A Parity Error
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multidrop mode the parity error bit stores the receive A/D (Address/Data) bit.

SRA[4] – Channel A Overrun Error
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a 'reset error status' command.

SRA[3] – Channel A Transmitter Empty (TxEMTA)
This bit will be set when the transmitter underruns, i.e., both the TxEMT and TxRDY bits are set. This bit and TxRDY are set when the transmitter is first enabled and at any time it is re-enabled after either (a) reset, or (b) the transmitter has assumed the disabled state. It is always set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission.

It is reset when the THR is loaded by the CPU, a pending transmitter disable is executed, the transmitter is reset, or the transmitter is disabled while in the underrun condition.

SRA[2] – Channel A Transmitter Ready (TxRDYA)
This bit, when set, indicates that the transmit FIFO is not full and ready to be loaded with another character. This bit is cleared when the transmit FIFO is loaded by the CPU and there are (after this load) no more empty locations in the FIFO. It is set when a character is transferred to the transmit shift register. TxRDYA is reset when the transmitter is disabled and is set when the transmitter is first enabled. Characters loaded to the TxFIFO while this bit is 0 will be lost. This bit has different meaning from ISR[0].

SRA[1] – Channel A FIFO Full (FFULLA)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all eight FIFO positions are occupied. It is reset when the CPU reads the receive FIFO. If a character is waiting in the receive shift register because the FIFO is full, FFULLA will not be reset when the CPU reads the receive FIFO. This bit has different meaning from ISR1 when MR1 6 is programmed to a '1'.

SRA[0] – Channel A Receiver Ready (RxRDYA)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receive FIFO, only if (after this read) there are no more characters in the FIFO.

SRB – Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the Channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR – Output Port Configuration Register

OPCR[7] – OP7 Output Select
This bit programs the OP7 output to provide one of the following:
0 The complement of OPR[7].
1 The Channel B transmitter interrupt output which is the complement of ISR[4]. When in this mode OP7 acts as an open- drain output. Note that this output is not masked by the contents of the IMR.

OPCR[6] – OP6 Output Select
This bit programs the OP6 output to provide one of the following:
0 The complement of OPR[6].
1 The Channel A transmitter interrupt output which is the complement of ISR[0]. When in this mode OP6 acts as an open- drain output. Note that this output is not masked by the contents of the IMR.

OPCR[5] – OP5 Output Select
This bit programs the OP5 output to provide one of the following:
0 The complement of OPR[5].
1 The Channel B receiver interrupt output which is the complement of ISR[5]. When in this mode OP5 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[4] – OP4 Output Select
This field programs the OP4 output to provide one of the following:
0 The complement of OPR[4].
1 The Channel A receiver interrupt output which is the complement of ISR[1]. When in this mode OP4 acts as an open-drain output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] – OP3 Output Select
This bit programs the OP3 output to provide one of the following:
00 The complement of OPR[3].
01 The counter/timer output, in which case OP3 acts as an open-drain output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
10 The 1X clock for the Channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
11 The 1X clock for the Channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] – OP2 Output Select
This field programs the OP2 output to provide one of the following:
00 The complement of OPR[2].
01 The 16X clock for the Channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
10 The 1X clock for the Channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
11 The 1X clock for the Channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

SOPR – Set the Output Port Bits (OPR)

SOPR[7:0] – Ones in the byte written to this register will cause the corresponding bit positions in the OPR to set to 1. Zeros have no effect.

ROPR – Reset Output Port Bits (OPR)

ROPR[7:0] – Ones in the byte written to the ROPR will cause the corresponding bit positions in the OPR to set to 0. Zeros have no effect.

Table 4. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz

NORMAL RATE (BAUD)	ACTUAL 16X CLOCK (kHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2K	307.2	0
38.4K	614.4	0

NOTE: Duty cycle of 16X clock is 50% ± 1%.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates to be generated by the BRG (see Table 3).

The selected set of rates is available for use by the Channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table 4.

Table 5. ACR 6:4 Field Definition

ACR 6:4	MODE	CLOCK SOURCE
000	Counter	External (IP2)
001	Counter	TxCA – 1X clock of Channel A transmitter
010	Counter	TxCB – 1X clock of Channel B transmitter
011	Counter	Crystal or external clock (X1/CLK) divided by 16
100	Timer	External (IP2)
101	Timer	External (IP2) divided by 16
110	Timer	Crystal or external clock (X1/CLK)
111	Timer	Crystal or external clock (X1/CLK) divided by 16

NOTE: The timer mode generates a squarewave.

ACR[6:4] – Counter/Timer Mode And Clock Source Select
This field selects the operating mode of the counter/timer and its clock source as shown in Table 5.

ACR[3:0] – IP3, IP2, IP1, IP0 Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – IP3, IP2, IP1, IP0 Change-of-State
These bits are set when a change-of-state, as defined in the input port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – IP3, IP2, IP1, IP0 Change-of-State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the Interrupt Mask Register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR – the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to H'00' when the DUART is reset.

ISR[7] – Input Port Change Status
This bit is a '1' when a change-of-state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] – Channel B Change In Break
This bit, when set, indicates that the Channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel B 'reset break change interrupt' command.

ISR[5] – RxB Interrupt
This bit indicates that the channel B receiver is interrupting according to the fill level programmed by the MR0 and MR1 registers. This bit has a different meaning than the receiver ready/full bit in the status register.

ISR[4] – TxB Interrupt
This bit indicates that the channel B transmitter is interrupting according to the interrupt level programmed in the MR0[5:4] bits. This bit has a different meaning than the Tx RDY bit in the status register.

ISR[3] – Counter Ready.
In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] – Channel A Change in Break
This bit, when set, indicates that the Channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a Channel A 'reset break change interrupt' command.

ISR[1] – RxA Interrupt
This bit indicates that the channel A receiver is interrupting according to the fill level programmed by the MR0 and MR1 registers. This bit has a different meaning than the receiver ready/full bit in the status register.

ISR[0] – TxA Interrupt
This bit indicates that the channel A transmitter is interrupting according to the interrupt level programmed in the MR0[5:4] bits. This bit has a different meaning than the Tx RDY bit in the status register.

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR causes an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1' the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3-OP7 or the reading of the ISR.

CTPU and CTPL – Counter/Timer Registers

The CTPU and CTPL hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTPU/CTPL registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer mode, the C/T generates a square wave whose period is twice the value (in C/T clock periods) of the CTPU and CTPL. The waveform so generated is often used for a data clock. The formula for calculating the divisor n to load to the CTPU and CTPL for a particular 1X data clock is shown below.

$$n = \frac{C/T\ Clock\ Frequency}{2 \times 16 \times Baud\ rate\ desired}$$

Often this division will result in a non-integer number; 26.3, for example. One can only program integer numbers in a digital divider. Therefore, 26 would be chosen. This gives a baud rate error of 0.3/26.3 which is 1.14%; well within the ability asynchronous mode of operation.

If the value in CTPU and CTPL is changed, the current half-period will not be affected, but subsequent half periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read at address A3-A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a start counter command (read with A3-A0 = 1110) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTPU and CTPL.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3-A0 = H'F'). The command however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

In the counter mode, the value C/T loaded into CTPU and CTPL by the CPU is counted down to 0.. Counting begins upon receipt of a start counter command. Upon reaching terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTPU and CTPL at any time, but the new count becomes effective only on the next start counter commands. If new values have not been loaded, the previous count values are preserved and used for the next count cycle

In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8 bits to the upper 8 bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTPU and CTPL.

When the C/T clock divided by 16 is selected, the maximum divisor becomes 1,048,575.

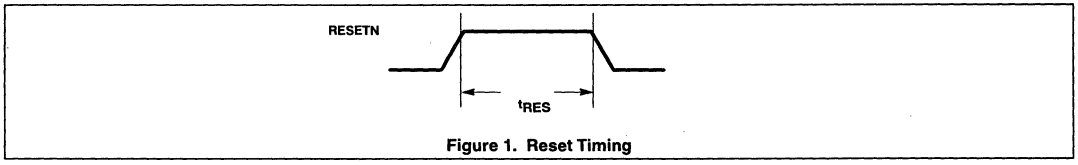


Figure 1. Reset Timing

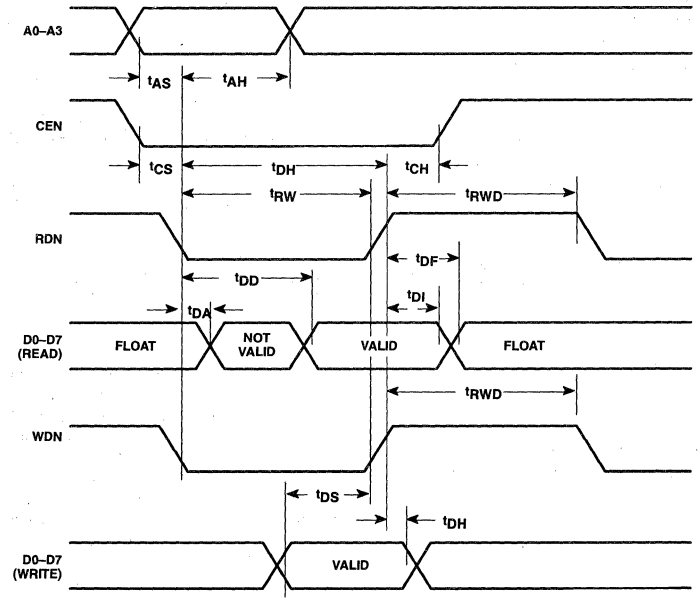


Figure 2. Bus Timing

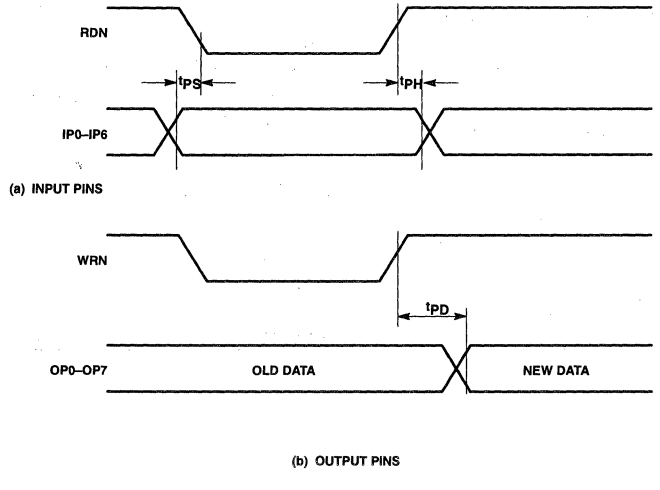
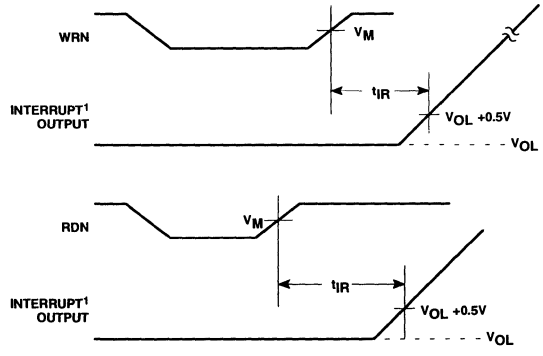
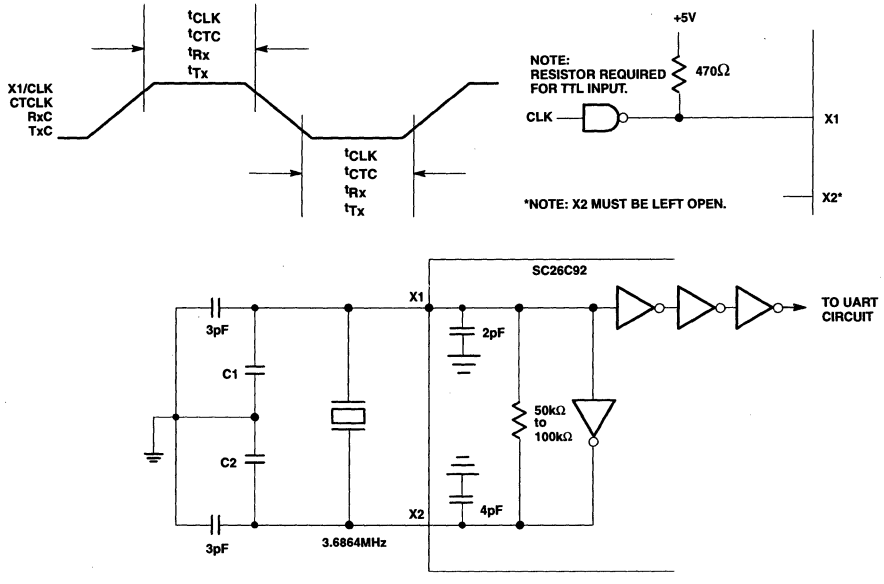


Figure 3. Port Timing



NOTES:
1. INTRN or OP3-OP7 when used as interrupt outputs.
2. The test for open-drain outputs is intended to guarantee switching of the output transistor. Measurement of this response is referenced from the midpoint of the switching signal, V_M, to a point 0.5V above V_{OL}. This point represents noise margin that assures true switching has occurred. Beyond this level, the effects of external circuitry and test environment are pronounced and can greatly affect the resultant measurement.

Figure 4. Interrupt Timing



C1 = C2 – 24pF FOR C_L = 20pF
C1 and C2 should be chosen according to the crystal manufacturer's specification.
C1 and C2 values will include any parasitic capacitance of the wiring and X1 X2 pins.
Gain at 3.6864MHz: 9 to 13 dB
Phase at 3.6864MHz: 272 to 276 degrees.
Package capacitance approximately 4pF.

Figure 5. Clock Timing

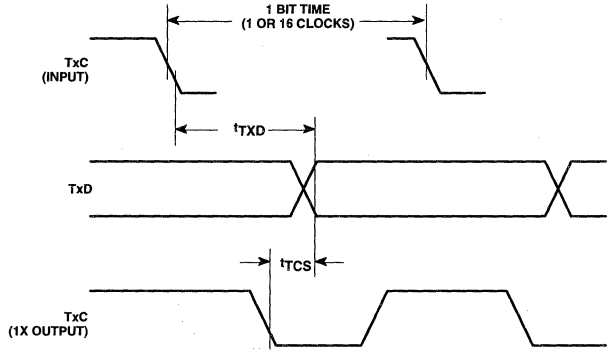


Figure 6. Transmitter External Clocks

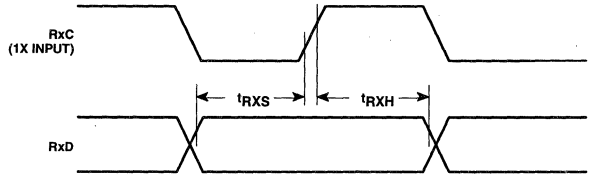
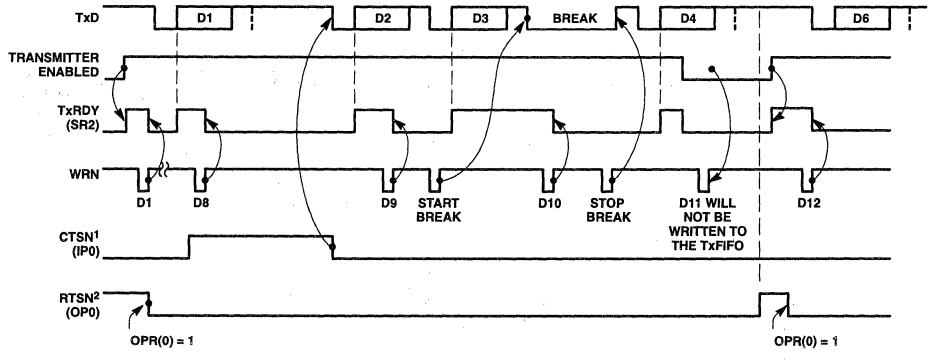


Figure 7. Receiver External Clock



NOTES:
1. Timing shown for MR2(4) = 1.
2. Timing shown for MR2(5) = 1.

Figure 8. Transmitter Timing

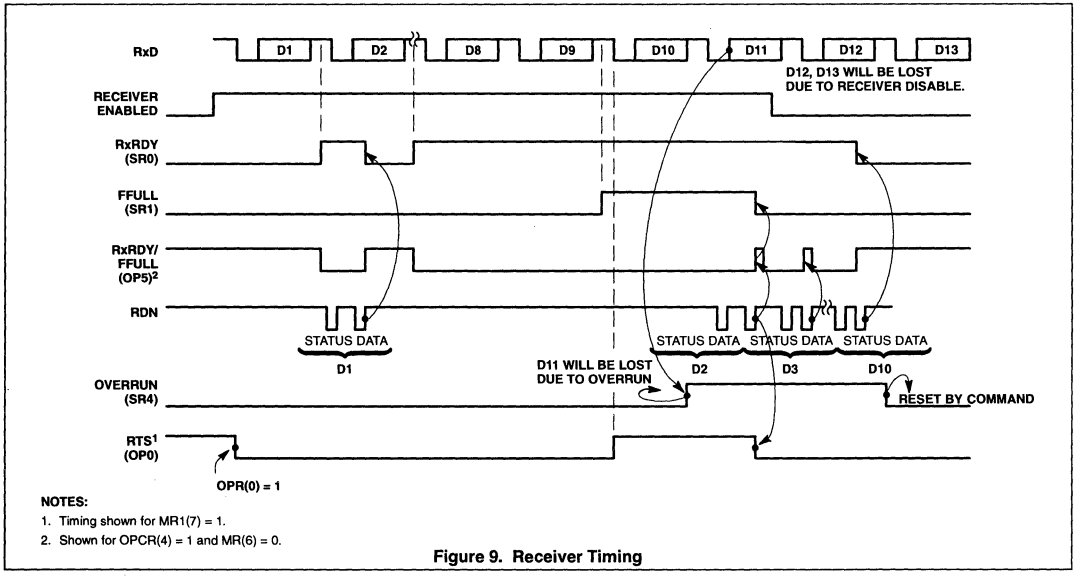


Figure 9. Receiver Timing

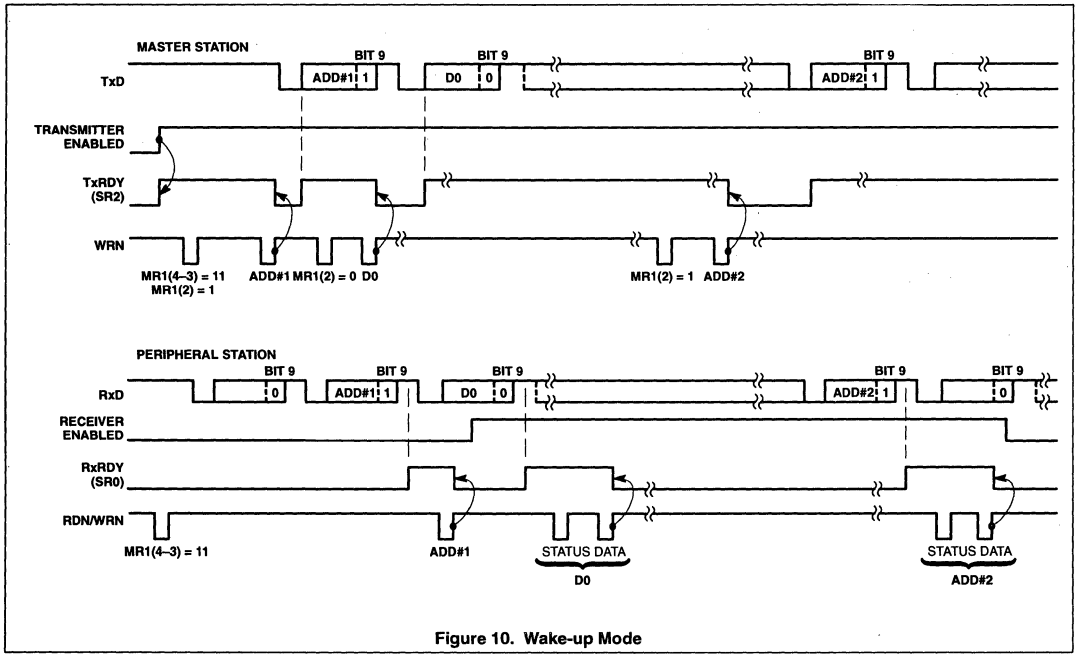


Figure 10. Wake-up Mode

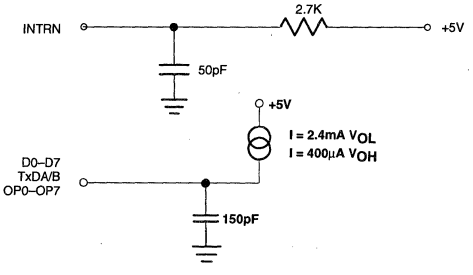


Figure 11. Test Conditions on Outputs

Output Port Notes

The output ports are controlled from four places: the OPCR register, the OPR register, the MR registers and the command register (except the 2681 and 68681) The OPCR register controls the source of the data for the output ports OP2 through OP7. The data source for output ports OP0 and OP1 is controlled by the MR and CR registers. When the OPR is the source of the data for the output ports, the data at the ports is inverted from that in the OPR register. The content of the OPR register is controlled by the "Set Output Port Bits Command" and the "Reset Output Bits Command". These commands are at E and F, respectively. When these commands are used, action takes place only at the bit locations where ones exist. For example, a one in bit location 5 of the data word used with the "Set Output Port Bits" command will result in OPR5 being set to one. The OP5 would then be set to zero (V_{SS}). Similarly, a one in bit position 5 of the data word associated with the "Reset Output Ports Bits" command would set OPR5 to zero and, hence, the pin OP5 to a one (V_{DD}).

The CTS, RTS, CTS Enable Tx signals

CTS (Clear To Send) is usually meant to be a signal to the transmitter meaning that it may transmit data to the receiver. The CTS input is on pin IP0 for TxA and on IP1 for TxB. The CTS signal is active low; thus, it is called CTSAN for TxA and CTSBN for TxB.

RTS is usually meant to be a signal from the receiver indicating that the receiver is ready to receive data. It is also active low and is, thus, called RTSAN for RxA and RTSBN for RxB. RTSAN is on pin OP0 and RTSBN is on OP1. A receiver's RTS output will usually be connected to the CTS input of the associated transmitter. Therefore, one could say that RTS and CTS are different ends of the same wire!

MR2(4) is the bit that allows the transmitter to be controlled by the CTS pin (IP0 or IP1). When this bit is set to one AND the CTS input is driven high, the transmitter will stop sending data at the end of the present character being serialized. It is usually the RTS output of the receiver that will be connected to the transmitter's CTS input. The receiver will set RTS high when the receiver FIFO is full AND the start bit of the ninth character is sensed. Transmission then stops with nine valid characters in the receiver. When MR2(4) is set to one, CTSN must be at zero for the transmitter to operate. If MR2(4) is set to zero, the IP pin will have no effect on the operation of the transmitter.

MR1(7) is the bit that allows the receiver to control OP0. When OP0 (or OP1) is controlled by the receiver, the meaning of that pin will be RTS. However, a point of confusion arises in that OP0 (or OP1) may also be controlled by the transmitter. When the transmitter is controlling this pin, its meaning is not RTS at all. It is, rather, that the transmitter has finished sending its last data byte.

Programming the OP0 or OP1 pin to be controlled by the receiver and the transmitter at the same time is allowed, but would usually be incompatible.

RTS can also be controlled by the commands 1000 and 1001 in the command register. These commands set and reset the bits OPR[0] and OPR[1]. RTS is expressed at the OP0 or OP1 pin which is still an output port. Therefore, the state of OP0 or OP1 should be set low (either by commands of the CR register or by writing to the Set Output Ports Register) for the receiver to generate the proper RTS signal. The logic at the output is basically a NAND of the OPR register and the RTS signal as generated by the receiver. When the RTS flow control is selected via the MR(7) bit state of the OPR register is not changed. Terminating the use of "Flow Control" (via the MR registers) will return the OP0 or OP1 pins to the control of the OPR register.

Quad universal asynchronous receiver/transmitter (QUART) SC26C94

DESCRIPTION

The 26C94 quad universal asynchronous receiver/transmitter (QUART) combines four enhanced Philips Semiconductors industry-standard UARTs with an innovative interrupt scheme that can vastly minimize host processor overhead. It is implemented using Philips Semiconductors' high-speed CMOS process that combines small die size and cost with low power consumption.

The operating speed of each receiver and transmitter can be selected independently at one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the QUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

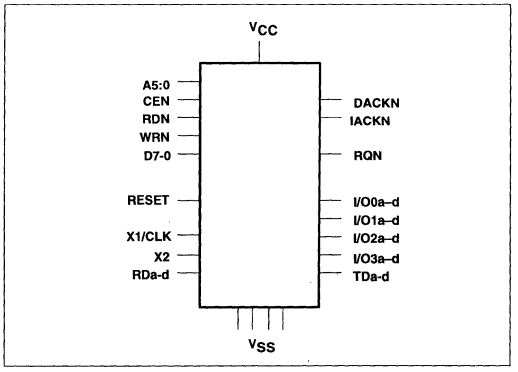
Each receiver is buffered with eight character FIFOs (first-in-first-out memories) and one shift register to minimize the potential for receiver overrun and to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full. (RTS control)

The 2694 provides a power-down mode in which the oscillator is stopped and the register contents are stored. This results in reduced power consumption on the order of several magnitudes. The QUART is fully TTL compatible and operates from a single +5V power supply.

FEATURES

- New low overhead interrupt control
- Four Philips Semiconductors industry-standard UARTs
- Eight byte receive FIFO and eight byte transmit FIFO for each UART
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Baud rate for the receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4K baud Non-standard rates to 1.0M baud
  - User-defined rates from the programmable counter/timer associated with each of two blocks
  - External 1x or 16x clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation

PIN CONFIGURATIONS

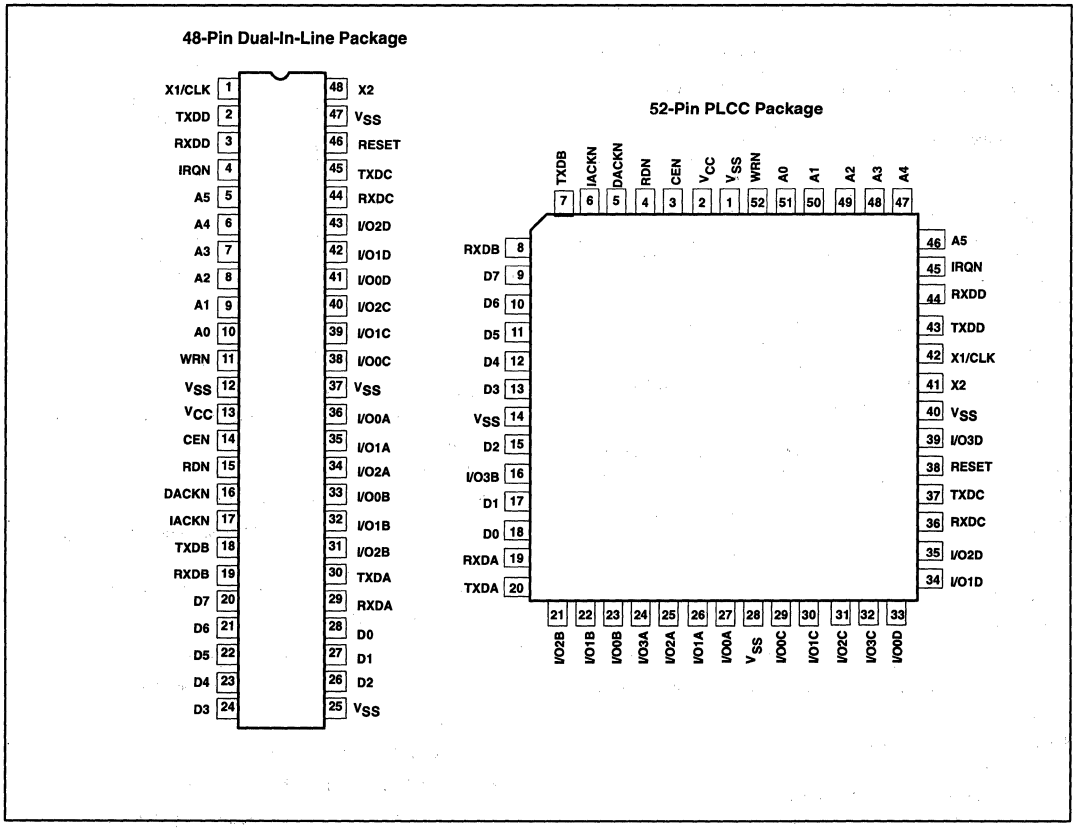


- Programmable channel mode
  - Normal (full-duplex), automatic echo, local loop back, remote loopback
- Programmable interrupt priorities
- Identification of highest priority interrupt
- Global interrupt register set provides data from interrupting channel
- Vectored interrupts with programmable vector format
- IACKN and DTACKN signals
- Built-in baud rate generator with choice of 18 rates
- Four I/O pins per UART for modem controls, clocks, etc.
- Power down mode
- High-speed CMOS technology
- 52-pin PLCC and 48-pin DIP
- Commercial and industrial temperature ranges available
- On-chip crystal oscillator
- TTL compatible
- Single +5V power supply with low power mode
- Two multifunction programmable 16-bit counter/timers
- 1MHz 16x mode operation
- 30ns data bus release time
- "Watch Dog" timer for each receiver

ORDERING INFORMATION

PACKAGES	V_{CC} = +5V ±10%, T_A = 0°C to +70°C	V_{CC} = +5V ±10%, T_A = –40°C to +85°C	DWG #
48-Pin Plastic Dual In-Line Package (DIP)	SC26C94C1N	SC26C94A1N	0416C
52-Pin Plastic Leaded Chip Carrier (PLCC) Package	SC26C94C1A	SC26C94A1A	0397E

PIN CONFIGURATIONS



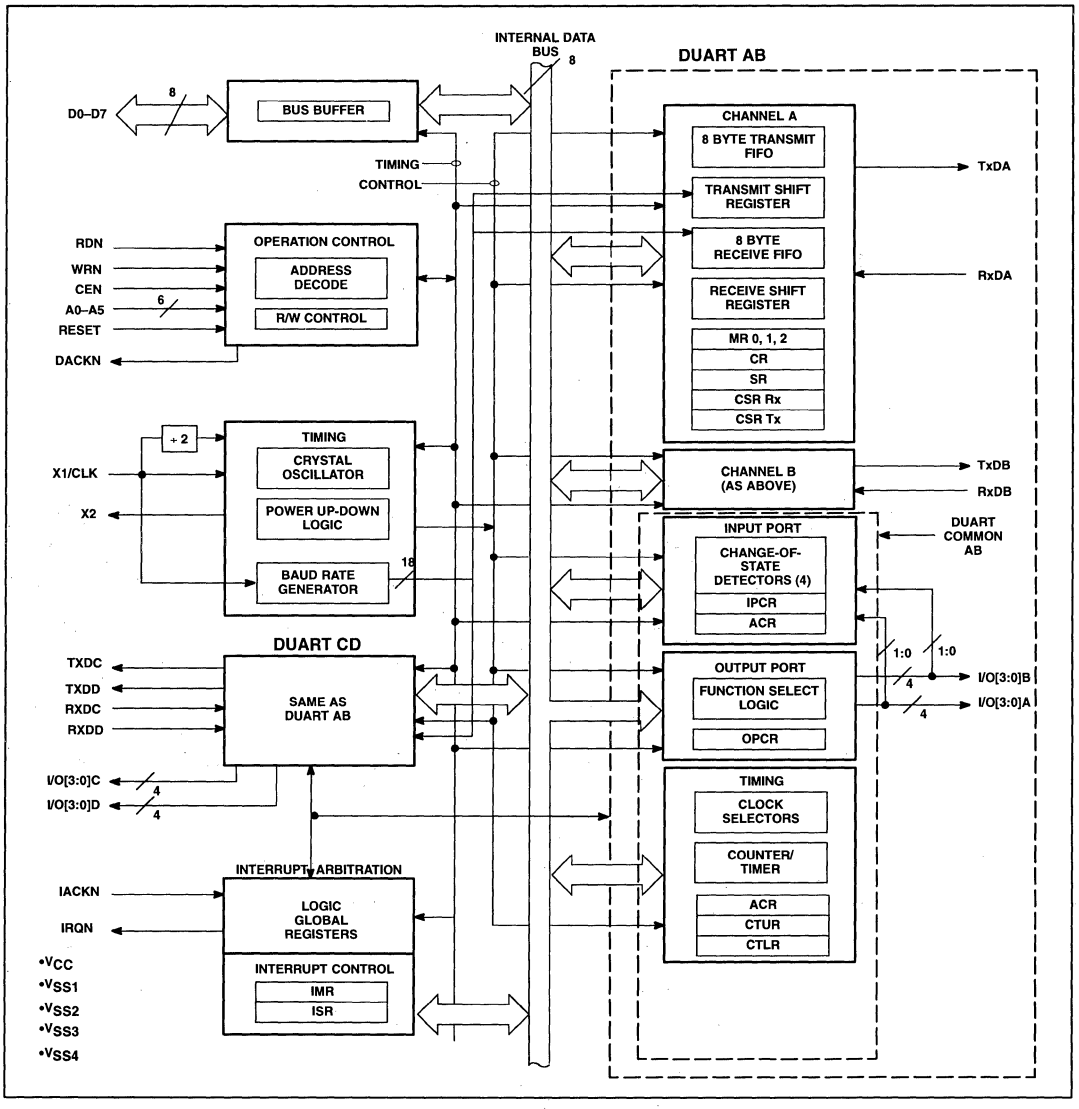
ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[3]	Note 4	°C
T_{STG}	Storage temperature range	–65 to +150	°C
V_{CC}	Voltage from V_{DD} to GND[4]	–0.5 to +7.0	V
V_S	Voltage from any pin to ground[4]	–0.5 to V_{CC} +0.5	V
P_D	Power dissipation	1	W

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range. See ordering information table for applicable temperature range and operating supply range.

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	TYPE	NAME AND FUNCTION
CEN	I	**Chip Select:** Active low input that, in conjunction with RDN or WRN, indicates that the host MPU is trying to access a QUART register. CEN must be inactive when IACKN is asserted.
A5:0	I	**Address Lines:** These inputs select a 26C94 register to be read or written by the host MPU.
D7:0	I/O	**8-bit Bidirectional Data Bus:** Used by the host MPU to read and write 26C94 registers.
RDN	I	**Read Strobe:** Active low input. When this line is asserted simultaneously with CEN, the 26C94 places the contents of the register selected by A5:0 on the D7:0 lines.
WRN	I	**Write Strobe:** Active low input. When this line is asserted simultaneously with CEN, the c2694 writes the data on D7:0 into the register selected by A5:0.
DACKN	O	**Data ACKnowledge:** Active low, open-drain output to the host MPU, which is asserted subsequent to a read or write operation. For a read operation, assertion of DACKN indicates that register data is valid on D7:0. For a write operation, it indicates that the data on D7:0 has been captured into the indicated register. This signal corresponds to READYN on 80x86 processors and DTACKN on 680x0 processors.
IRQN	O	**Interrupt Request:** This active low open-drain output to the host MPU indicating that one or more of the enabled UART interrupt sources has reached an interrupt value which exceeds that pre-programmed by host software. The IRQN can be used directly as a 680x0 processor input; it must be inverted for use as an 80x86 interrupt input. This signal requires an external pull-up resistor.
IACKN	I	**Interrupt ACKnowledge:** Active low input indicating that the host MPU is acknowledging an interrupt requested by this device. The 26C94 responds to the assertion of this signal by placing an interrupt vector on D7-D0 and asserting DACKN. This signal updates the CIR register in the interrupt logic.
TDa-d	O	**Transmit Data:** Serial outputs from the four UARTs.
RDa-d	I	**Receive Data:** Serial inputs to the four UARTs/
I/O0a-d	I/O	**Input/Output 0:** A multi-use input or output signal for each UART. These pins can be used as general purpose inputs, Clear to Send inputs, 1X or 16X Transmit Clock outputs or general purpose outputs. Change-of-state detection is provided for these pins.
I/O1a-d	I/O	**Input/Output 1:** A multi-use input or output signal for each UART. These pins can be used as general purpose or 1X or 16X transmit clock inputs, or general purpose 1X or 16X receive clock outputs. Change-of-state detection is provided for these pins. In addition, I/O1a and I/O1c can be used as Counter/Timer inputs and I/O1b and I/O1d can be used as Counter/Timer outputs.
I/O2a-d	I/O	**Input/Output 2:** A multi-use input or output signal for each UART. These pins can be used as general purpose inputs, 1X or 16X receive clock inputs, general purpose outputs, RTS output or 1X or 16X receive clock outputs.
I/O3a-d	I/O	**Input/Output 3:** A multi-use input or output signal for each UART. These pins can be used as general purpose inputs, 1X or 16X transmit clock inputs, general purpose outputs, or 1X or 16X transmit clock outputs.
RESET	I	**Master Reset:** Active high reset for the 26C94 logic. Must be asserted at power-up, may be asserted at other times that the system is to be reset and restarted. OSC set to divide by 1, MR pointer set to 1, DACKN enabled, I/O pins to input. Registers reset: OPR, CIR. IRQN, DTACKN, IVR Interrupt Vector, Power Down, Test registers, FIFO pointers, Baud rate generator, Error Status, Watch Dog Timers, Change of State detectors, counter/timer to timer, Transmitter and Receiver controllers and all interrupt bits.
X1/CLK	I	**Crystal 1 or Communication Clock:** This pin is normally connected to one side of a 3.6864MHz or a 7.3728MHz crystal, or can be connected to an external clock up to 8MHz.
X2	O	**Crystal 2:** If a crystal is used, this pin should be connected to its other terminal. If an external clock is applied to X1, this pin should be left unconnected.
V_{CC}, V_{SS1}, V_{SS2}, V_{SS3}, V_{SS4}		**Power and grounds:** respectively.

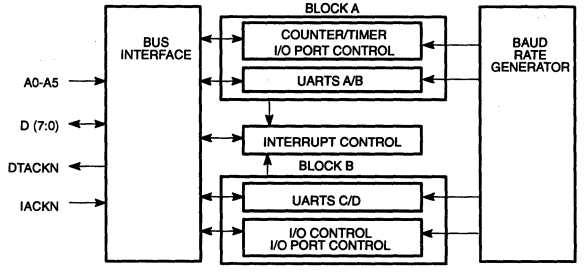


Figure 1. Channel Architecture

Table 1. QUART Registers[1]

A5:0	READ (RDN = Low)	WRITE (WRN = Low)
000000	Mode Register a (MR0a, MR1a, MR2a)	Mode Register a (MR0a, MR1a, MR2a)
000001	Status Register a (SRa)	Clock Select Register a (CSRa)
000010	Reserved	Command Register a (CRa)
000011	Receive Holding Register a (RxFIFOa)	Transmit Holding Register a (TxFIFOa)
000100	Input Port Change Reg ab (IPCRab)	Auxiliary Control Reg ab (ACRab)
000101	Interrupt Status Reg ab (ISRab)	Interrupt Mask Reg ab (IMRab)
000110	Counter/Timer Upper ab (CTUab)	Counter/Timer Upper Reg ab (CTURab)
000111	Counter/Timer Lower ab (CTLab)	Counter/Timer Lower Reg ab (CTLRab)
001000	Mode Register b (MR0b, MR1b, MR2b)	Mode Register b (MR0b, MR1b, MR2b)
001001	Status Register b (SRb)	Clock Select Register b (CSRb)
001010	Reserved	Command Register b (CRb)
001011	Receive Holding Register b (RxFIFOb)	Transmit Holding Register b (TxFIFOb)
001100	Output Port Register ab (OPRab)	Output Port Register ab (OPRab)
001101	Input Port Register ab (IPRab)	I/OPCRa (I/O Port Control Reg a)
001110	Start Counter ab	I/OPCRb (I/O Port Control Reg b)
001111	Stop Counter ab	Reserved
010000	Mode Register c (MR0c, MR1c, MR2c)	Mode Register c (MR0c, MR1c, MR2c)
010001	Status Register c (SRc)	Clock Select Register c (CSRc)
010010	Reserved	Command Register c (CRc)
010011	Receive Holding Register c (RxFIFOc)	Transmit Holding Register c (TxFIFOc)
010100	Input Port Change Reg cd (IPCRcd)	Auxiliary Control Reg cd (ACRcd)
010101	Interrupt Status Reg cd (ISRcd)	Interrupt Mask Reg cd (IMRcd)
010110	Counter/Timer Upper cd (CTUcd)	Counter/Timer Upper Reg cd (CTURcd)
010111	Counter/Timer Lower cd (CTLcd)	Counter/Timer Lower Reg cd (CTLRcd)
011000	Mode Register d (MR0d, MR1d, MR2d)	Mode Register d (MR0d, MR1d, MR2d)
011001	Status Register d (SRd)	Clock Select Register d (CSRd)
011010	Reserved	Command Register d (CRd)
011011	Receive Holding Register d (RxFIFOd)	Transmit Holding Register d (TxFIFOd)
011100	Output Port Register cd (OPRcd)	Output Port Register cd (OPRcd)
011101	Input Port Register cd (IPRcd)	I/OPCRc (I/O Port Control Reg c)
011110	Start Counter cd	I/OPCRd (I/O Port Control Reg d)
011111	Stop Counter cd	Reserved
100000	Bidding Control Register a (BCRa)	Bidding Control Register a (BCRa)
100001	Bidding Control Register b (BCRb)	Bidding Control Register b (BCRb)
100010	Bidding Control Register c (BCRc)	Bidding Control Register c (BCRc)
100011	Bidding Control Register d (BCRd)	Bidding Control Register d (BCRd)
100100	Reserved	Power Down
100101	Reserved	Power Up
100110	Reserved	Disable DACKN
100111	Reserved	Enable DACKN
101000	Current Interrupt Register (CIR)	Reserved
101001	Global Interrupting Channel Reg (GICR)	Interrupt Vector Register (IVR)
101010	Global Int Byte Count Reg (GIBCR)	Update CIR
101011	Global Receive Holding Reg (GRxFIFO)	Global Transmit Holding Reg (GTxFIFO)
101100	Interrupt Control Register (ICR)	Interrupt Control Register (ICR)
101101	Reserved	BRG Rate. 00 = low; 01 = high
101110	Reserved	Set X1/CLK divide by two[2]
101111	Reserved	Set X1/CLK Normal[2]
110000–111000	Reserved	Reserved
111001	Test Mode	Test Mode
111010–111111	Reserved	Reserved

NOTES:
1. Registers not explicitly reset by hardware reset power up randomly.
2. In X1/CLK divide by 2 all circuits receive the divided clock except the BRG and change-of-state detectors.

FUNCTIONAL BLOCKS

The QUART is composed of four Philips Semiconductors industry–standard UARTs, each having a separate transmit and receive channel.

The Basic UART cells in the QUART are configured with 8-byte Receive FIFOs and 8-byte Transmit FIFOs. Hardware supports interrupt priority arbitration based on the number of bytes available in the transmit and receive FIFOs, counter/timers, change of state detectors, break detect or receiver error. Attempts to push a full FIFO or pop an empty FIFO do not affect the count.

Baud Rate Generator

The baud rate generator used in the QUART is the same as that used in other Philips Semiconductors industry standard UARTs. It provides 18 basic Baud rates from 50 baud to 38,400 baud. It has been enhanced to provide to provide other baud rates up to 230,400 baud based on a 3.6364MHz clock; with an 8.0MHz clock rates to 500K baud. Other rates are available by setting the BRG rate to high at address 2D hex or setting Test 1 on at address 39 hex. See Table 3. These two modes are controlled by writing 00 or 01 to the addresses above. They are both set to 00 on reset. External Rx and Tx clocks yield rates to 1MHz in the 16X mode.

BLOCK DIAGRAM

As shown in the block diagram, the QUART consists of: data bus buffer, interrupt control, operation control, timing, and four receiver and transmitter channels. The four channels are divided into two different blocks, each block independent of the other.

Channel Blocks

There are two blocks (Block Diagram), each containing two sets of receiver/transmitters. In the following discussion, the description applies to Block A which contains channels a and b. However, the same information applies to all channel blocks.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the QUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The functions performed by the CPU read and write operations are shown in Table 1.

Mode registers (MR) 0, 1 and 2 are accessed via an address counter. This counter is set to one (1) by reset or a command 1x to the Command Register for compatibility with other Philips Semiconductors software. It is set to 0 via a command Bx to the Command Register (CR). The address counter is incremented with each access to the MR until it reaches 2 at which time it remains at 2. All subsequent accesses to the MR will be to MR2 until the MR counter is changed by a reset or an MR counter command.

The Mode Registers control the basic configuration of the UART channels. There is one for each UART. (Transmitter/receiver pair)

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, power up/down logic and a divide by 2 selector. Closely associated with the timing block are two 16-bit counter/timers; one for each DUART.

Oscillator

The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/CLK and X2 inputs with a minimum of external components. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. If an external clock is used instead of a crystal, X1 must be driven and X2 left floating as shown in Figure 10. The clock serves as the basic timing reference for the baud rate generator (BRG), the counter/timer, and other internal circuits. A clock frequency, within the limits specified in the electrical specifications, must be supplied even if the internal BRG is not used.

The X1 pin always supplies the clock for the baud rate generator. The X1 pin also has a feature such that it may be divided by 2. The divide by two mode must always be used whenever the X1 pin is above 4MHz. The baud rate generator supplies the standard rates when X1 is at 3.6864MHz. In the divide by 2 mode, all circuits receive the divide by two clock except baud rate generator and I/O pin change-of-state detectors. 7.3738MHz clock doubles standard baud rates.

Baud Rate Generator

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. The eighteen BRG rates are grouped in two groups. Eight of the 18 are common to each group. The group selection is controlled by ACR[7]. See the Baud Rate Table 3. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The clock selectors allow the independent selection, by the receiver and transmitter, of any of these baud rates or an external timing signal.

Counter/Timer

The counter timer is a 16-bit programmable divider that operates in one of three modes: counter, timer, time out. In the timer mode it generates a square wave. In the counter mode it generates a time delay. In the time out mode it monitors the time between received characters. The C/T uses the numbers loaded into the Counter/Timer Lower Register (CTLR) and the Counter/Timer Upper Register (CTUR) as its divisor.

There are two counter/timers in the QUART; one for each block. The counter/timer clock source and mode of operation (counter or timer) is selected by the Auxiliary Control Register bits 6 to 4 (ACR[6:4]). The output of the counter/timer may be used for a baud rate and/or may be output to the I/O pins for some external function that may be totally unrelated to data transmission. The counter/timer also sets the counter/timer ready bit in the Interrupt Status Register (ISR) when its output transitions from 1 to 0.

A register read address (see Table 1) is reserved to issue a start counter/timer command and a second register read address is reserved to issue a stop command. The value of D(7:0) is ignored. The START command always loads the contents of CTUR, CTLR to the counting registers. The STOP command always resets the ISR(3) bit in the interrupt status register.

Timer Mode
In the timer mode a symmetrical square wave is generated whose half period is equal in time to division of the selected counter/timer clock frequency by the 16-bit number loaded in the CTLR CTUR. Thus, the frequency of the counter/timer output will be equal to the counter/timer clock frequency divided by twice the value of the CTUR CTLR. While in the timer mode the ISR bit 3 (ISR[3]) will be set each time the counter/timer transitions from 1 to 0. (High to low) This continues regardless of issuance of the stop counter command. ISR[3] is reset by the stop counter command. NOTE: Reading of the CTU and CTL registers in the timer mode is not meaningful.

When the C/T is used to generate a baud rate *and* the C/T is selected through the CSR then the receivers and/or transmitter will be operating in the 16x mode. Calculation for the number 'n' to program the counter timer upper and lower registers is shown below.

$$n = \frac{\text{C/T Clock Frequency}}{2 * 16 * \text{Baud rate desired}}$$

Often this division will result in a non-integer number; 26.3 for example. One can only program integer numbers to a digital divider. Therefore 26 would be chosen. This gives a baud rate error of 0.3/26.3 which is 1.14%; well within the ability of the asynchronous mode of operation.

Counter Mode
In the counter mode the counter/timer counts the value of the CTLR CTUR down to zero and then sets the ISR[3] bit and sets the counter/timer output from 1 to 0. It then rolls over to 65,365 and continues counting with no further observable effect.

Reading the C/T in the counter mode outputs the present state of the C/T. If the C/T is not stopped, a read of the C/T may result in changing data on the data bus.

Timeout Mode
The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RxFIFO, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. If the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU will not be interrupted for the remaining characters in the RxFIFO.

By programming the C/T such that it would time out in just over one character time, the above situation could be avoided. The processor would be interrupted any time the data stream had stopped for more than one character time. NOTE: This is very similar to the watch dog time of MR0. The difference is in the programmability of the delay time and that the watchdog timer is restarted by either a receiver load to the RxFIFO or a system read from it.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. Only one receiver should use this mode at a time. However, if both are on, the timeout occurs after both receivers have been inactive for the timeout period. The start of the C/T will be on the logical or of the two receivers.

The timeout mode disables the regular START/STOP counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RxFIFO, the C/T is stopped after one C/T clock, reloaded with the value in CTUR and CTLR and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Since receiving a character restarts the C/T, the receipt of a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx='Ax', will also clear the counter ready bit and stop the counter until the next character is received.

The counter timer is controlled with six commands: Start/Stop C/T, Read/Write Counter/Timer lower register and Read/Write Counter/Timer upper register. These commands have slight differences depending on the mode of operation. Please see the detail of the commands under the CTLR CTUR Register descriptions.

Receiver and Transmitter

The QUART has four full-duplex asynchronous receiver/transmitters. The operating frequency for the receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input.

Registers associated with the communications channel are the mode registers (MR0, MR1 and MR2) Clock Select Register (CSR), Command Register (CR), Status Register (SR), Transmit FIFO (TxFIFO), and the Receive FIFO (RxFIFO). The transmit and receive FIFOs are each eight characters deep. The receive FIFO also stores three status bits with each character.

Transmitter
The transmitter accepts parallel data from the CPU and converts it to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the TxFIFO, the TxD output remains high and the TxEMT bit in the SR will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character in the TxFIFO. In the 16X clock mode, this also re-synchronizes the internal 1X transmitter clock so that transmission of the new character begins with minimum delay.

If the transmitter is disabled it continues operating until the character currently being transmitted and any characters in the TxFIFO, including parity and stop bits, have been transmitted. New data cannot be loaded to the TxFIFO when the transmitter is disabled.

The transmitter can be forced to send a break (a continuous low condition) by issuing a START BREAK command via the CR register. The break is terminated by a STOP BREAK command or a transmitter reset..

TxFIFO
The TxFIFO empty positions are encoded as a three bit number for presentation to the bidding logic. The coding will equal the number of bytes that remain to be filled. That is, a binary number of 101 will mean five bytes may be loaded; 111 means 7, etc. Eight positions will be indicated by a binary 111 *and* the FIFO empty bit will be set.

Receiver
The receiver accepts serial data on the RxD pin, converts the serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition, and presents the assembled character to the CPU via the receiver FIFO.

The receiver operates in two modes: the 1X and 16X. The 16X mode is the more robust of the two. It allows the receiver to establish a phase relation to the remote transmitter clock within 1/16 of a bit time and also allows validation of the start bit. The 1X mode does not validate the start bit and assumes that the receiver clock

rising edge is centered in the data bit cell. The use of the 1X mode implies that the transmitter clock is available to the receiver.

When operating in the 16X mode and after the receiver has been enabled the receiver state machine will look for a high to low transition on the RxD input. The detection of this transition will cause the divider being driven by the 16X clock to be reset to zero and continue counting. When the counter reaches 7 the RxD input is sampled again and if still low a valid START BIT will be detected. If the RxD input is high at count 7 then an invalid start bit will have been sensed and the receiver will then look for another high to low transition and begin validating again.

When a valid start bit is detected the receiver state machine allows the 16X divider circuit to continue counting 0 to 15. Each time the receiver passes count 7 (the theoretical center of the bit time) another data bit is clocked into the receiver shift register until the proper number of bits have been received including the parity bit, if used, and 1/2 stop bit. After the STOP BIT is detected the receiver state machine will wait until the next falling edge of the 1X clock and then clock the assembled character and its status bits into the receiver FIFO on the next rising edge of the 1X clock. The delay from the detection of the STOP BIT to the loading of the character to the RxFIFO will be from one half to one and one half X1 crystal clock periods, or twice that if X1/2 is used. Receiver Status Register bits for FIFO READY, FIFO FULL, parity error, framing error, break detect will also set at this time. The most significant bits for data characters less than eight bits will be set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (i.e. framing error) and RxD remains low for one-half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled). The parity error, framing error and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set.

If a break condition is detected (RxD is low for the entire character including the stop bit), only one character consisting of all zeros will be loaded in the FIFO and the received break bit in the SR is set to 1. The "Change of Break" bit in the ISR at position 2 or 6 is also set at this time. Note that the "Change of Break" bit will set again when the break condition terminates. The RxD input must return to a high condition for two successive clock edges of the 1X clock (internal or external) before a search for the next start bit begins.

NOTE: If the RxD input is low when the receiver is enabled and remains low for at least 9/16 of a bit time a valid start bit will be seen and data (probably random) will be clocked into the receiver FIFO. If the line remains low for a full character time plus a stop bit then a break will be detected.

Each receiver is equipped with a watchdog timer. This timer is enabled by MR0[7] and counts 64 RxC1X clocks. Its purpose is to alert the controlling CPU that data is in the FIFO which has not been read. This situation may occur at the end of a message when the last group of characters was not long enough to cause an interrupt.

RECEIVER FIFO

The RxFIFO consists of a first-in-first-out (FIFO) with a capacity of eight characters. Data is loaded from the receive shift register into the top-most empty position of the FIFO. The RxRDY bit in the status register (SR) is set whenever one or more characters are available to be read; a FFULL status bit is set if all eight stack positions are filled with data. The number of filled positions is encoded into a 3-bit value. This value is sent to the interrupt bidding logic where it is used to generate an interrupt. A read of the RxFIFO, outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits are 'popped' thus emptying a FIFO position for new data.

NOTE: The number of filled positions in the RxFIFO is coded as actual number filled positions. Seven filled will be coded as 7. Eight filled positions will be coded as 7 *and* the RxFIFO full status bit will be set.

In addition to the data word, three status bits (parity error, framing error, and received break) are appended to each data character in the FIFO. Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical OR of the status for all characters coming to the top of the FIFO since the last reset error command was issued. In either mode, reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RxFIFO is read. Therefore, the SR should be read prior to reading the corresponding data character.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exists, the contents of the FIFO are not affected: the character previously in the shift register is lost and the overrun error status bit, SR[4], will be set upon receipt of the start bit of the new (overrunning) character.

A "watchdog" timer is associated with each receiver. Its interrupt is enabled by MR0[7]. The purpose of this timer is alerting the control processor that characters are in the RxFIFO which have not been read and/or the datastream has stopped. This situation may occur at the end of a transmission when the last few characters received are not sufficient to cause an interrupt.

This counter times out after 64 bit times. It is reset each time a character is transferred from the Receive shift register to the RxFIFO or a read of the RxFIFO is executed.

WAKE-UP MODE (MULTI-DROP OR 9-BIT)

In addition to the normal transmitter and receiver operation described above, the QUART incorporates a special mode which provides automatic "wake up" of a receiver through address frame (or character) recognition for multi-processor or multi-station communications. This mode is selected by programming MR1[4:3] to '11'.

In this mode of operation a 'master' station transmits an address character to the several 'slave' stations on the line. The address character is identified by setting its parity bit to 1. The slave stations will usually have their receivers partially enabled as a result of setting MR1[4:3] to 11. When the receiver sees a one in the parity position, it considers it an address bit and loads that character to the RxFIFO and set the RxRDY bit in the status register. The user would usually set the receiver interrupt to occur on RxRDY as well. (All characters whose parity bits are set to 0 will be ignored). The local processor at the slave station will read the 'address' character just received. The local processor will test for an address match for this station and if match occurs it will enable the local receiver and receive the following data characters. The master will normally follow an address character(s) with data characters. Since the data characters transmitted by the master will have their parity bits set to zero, stations other than the addressed one(s) will ignore the data.

NOTE: The time between address and data fields must be enough for the local processor to test the address character and enable the receiver. At bit times approaching 10μs this may begin to be a point of concern.

The parity (Address/Data) bit should not be changed until the last stop bit of an address has been sent. Similarly the A/D bit should

not be changed to address until the last stop bit has been sent. Either of these conditions will be indicated by an active TxEMT bit in the SR.

The parity bit is not part of the TxFIFO. It is in the transmitter state machine. However, it could be controlled in the FIFO if 5, 6 or 7 bit data was transmitted by using a 6, 7 or 8 bit character. The most significant bit would then be in the 'parity' position and represent the A/D bit. The design of the UART is based, however, on the A/D bit being controlled from the MR register.

Parity should be changed immediately before the data bytes will be loaded to the transmitter.

A transmitted character consists of a start bit, the programmed number of data and stop bits and an "address/data" bit. The parity bit is used as the address or data indicator. The polarity of the A/D bit is selected by setting MR1[2] to zero or one; zero indicates that the current byte is data, while one indicates that the current byte is addressed. The desired polarity of the A/D bit (parity) should be programmed before the TxFIFO is loaded.

The receiver should be enabled before the beginning of the first data bit. The time required is dependent on the interrupt latency of the slave receivers. The transmitter is able to start data immediately after the address byte has been sent.

While in this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character in the RxFIFO if the received A/D bit is a one, but discards the received character if the received A/D bit is a zero. If enabled, all received characters are then transferred to the CPU via the RxFIFO. In either case, the data bits are loaded in the data FIFO while the A/D bit is loaded in the status FIFO position normally used for parity error (SR[5]). Framing error, overrun error, and break detect operate normally whether or not the receiver is enabled.

INPUT OUTPUT (I/O) PINS

There are 16 multi-use pins; four for each UART. These pins are accessed and controlled via the Input Port Register (IPR), I/O Port Control Register (I/OPCR), Input Port Change Register (IPCR), and Output Port Register (OPR). They may be individually programmed to be inputs or outputs. See Table 5.

I/O0x and I/O1x pins have change of state detectors. The change of state detectors sample the input ports every 26.04µs (with the X1 clock at 3.686400MHz) and set the change bit in the IPCR if the pin has changed since it was last read. Whether the pins are programmed as inputs or outputs the change detectors still operate and report changes accordingly. See the register descriptions of the I/O ports for the detailed use of these features.

Interrupt Priority System

The interrupt control for the QUART has been designed to provide very low interrupt service overhead for the controlling processor while maintaining a high degree of flexibility in setting the importance of interrupts generated in different functional blocks of the device.

This is accomplished by allowing each function of the QUART (18 total) which may cause an interrupt to generate a variable numeric code which contains the identity of the source, channel number and severity level. This code is compared (at the X1 clock rate or the X1 clock rate divided by 2) to an interrupt threshold. When the interrupting source generates a code that is numerically greater than the interrupt threshold the IRQN is asserted

This is referred to as the bidding process. The winning bid contains, in different fields, all the characteristics of the winning bidder. This data may be used in several ways to steer the controlling processor to the proper type and amount of service required (usually the amount of service refers to the number of bytes written to the transmitter or read from the receiver). Access to the winning bidder is provided via the CIR (Current Interrupt Register), interrupt vectors, modified interrupt vectors and Global registers.

NOTE: IRQN is essentially a level output. It will go active on an interrupt condition and stays active until all interrupting sources are serviced.

IRQN is designed to be an open drain active low level output. It will go low under the control of the arbitration system and remain low until the arbitration has determined that no more sources require service.

When only one Rx or Tx is interrupting, it is possible to see the IRQN assert more than once if, during an access to the FIFO, the CEN input is inactive for more than two cycles of the X1 clock or X1 divide by 2 if that feature is enabled.

IACKN may be thought of as a special read input. Driving IACKN low will update the CIR and then read the Interrupt Vector Register or the Interrupt Vector Register modified by the CIR.

Functional Description of the Interrupt Arbitration

For the purpose of this description, a 'source' is any one of the 18 QUART circuits that may generate an interrupt. The QUART contains eighteen sources which may cause an interrupt:

1. Four receiver data FIFO filled functions.
2. Four receiver BREAK detect functions.
3. Four transmitter FIFO space available functions.
4. Four "Change of State" detectors.
5. Two counter/timers.

The interrupt logic at each source produces a numeric code that identifies its interrupt priority condition currently pending. This code is compared to a programmable Interrupt Threshold via the arbitration logic which determines if the IRQN should be asserted. The arbitration logic only judges those possible interrupt sources which have been allowed to bid via the IMR (Interrupt Mask Register).

The arbitration logic produces a value which is the concatenation of the channel number, interrupt type, FIFO fill level and user-defined fields. The channel number and interrupt type fields are hardwired. During the "bid arbitration" process all bids from enabled sources are presented, simultaneously, to an internal interrupt bus. The bidding system and formats are discussed in more detail in following sections.

The interrupt arbitration logic insures that the interrupt with the numerically largest bid value will be the only source driving the interrupt bus at the end of the arbitration period. The arbitration period follows the period of the X1 clock. The maximum speed is 4.0MHz. If a higher speed X1 clock is used then the X1 clock "divide by 2" feature must be used.

The value of the winning bid determined during the arbitration cycle is compared to the "Interrupt Threshold" contained in the ICR (Interrupt Control Register). If the winning bid exceeds the value of the ICR the IRQN is asserted.

Priority Arbitration and Bidding

Each of the five "types" of interrupts has slightly different "bid" value, as follows:

Receivers

# rcv'd	rEr	1	1	Chan #
3	1	1	1	2

Transmitters

0	# avail	1	0	Chan #
1	3	1	1	2

Break Detect

Programmable	1	0	0	Chan #
3	1	1	1	2

Change of State

Programmable	0	0	1	Chan #
3	1	1	1	2

Counter/Timer

Programmable	0	1	0	1	Chan #
2	1	1	1	1	2

Bits shown above as '0' or '1' are hard-wired inputs to the arbitration logic. Their presence allows determination of the interrupt type and they insure that no bid will have a value of all zeros (a condition that is indistinguishable from not bidding at all). They also serve to set a default priority among the non-receive/transmit types when the programmable fields are all zeros.

The channel number always occupies the two LSBs. Inclusion of the channel number insures that a bid value generated will be unique and that a single "winner" will drive the Interrupt Bus at the end of the arbitration interval. The channel number portion of each UARTs bid is hard-wired with UARTa being channel number 0 and so forth.

As can be seen above, bits 4:2 of the winning bid value can be used to identify the type of interrupt, including whether data was received correctly or not. Like the Channel number field, these bits are hard-wired for each interrupt source.

The "# rcv'd" and "# avail" fields indicate the number of bytes present in the receiver FIFO and the number of empty bytes in the transmitter FIFO, respectively.

NOTE: When there are zero bytes in the receiver's FIFO, it does NOT bid. Similarly, a full transmitter FIFO makes NO bid. In the case where all bids have been disabled by the Interrupt Mask Register or as a result of their byte counts, the active-low Interrupt Bus will return FFh. This value always indicates no interrupt source is active and IRQN will be negated.

The high order bit of the transmitter "bid" is always zero. An empty transmit FIFO is, therefore, fixed at a lower interrupt priority than a 1/2 full receive FIFO. Bit 4 of a receiver bid is the Receiver Error Bit (RER). The RER is the OR of the parity, framing and overrun error conditions. The RER does little to modify the priority of receiver interrupts vs. transmitter interrupts. It is output to the Interrupt Bus to allow inclusion of good data vs. problem data information in the Current Interrupt Register.

The high order bits of bids for received break, CoS (Change of State) and Counter/Timer events are all programmable. By programming ones in these fields, the associated interrupt source can be made more significant than most receiver and all transmitter interrupts. Values near zero in these fields makes them lower priority classes of interrupt.

The channel address for C/T ab will be encoded as channel B (01)

The channel address for C/T cd will be encoded as channel D (11)

As shown in Figure 4, the bid arbitration process is controlled by the EVAL/HOLDN signal derived from the oscillator clock.

Receipt of an IACKN signal from the host MPU latches the latest "winning bid" from the latched Interrupt Bus into the Current Interrupt Register (CIR). This logic is diagrammed in Figure 5.

If the IACKN falling edge of Figure 4 occurs during EVAL time, the result from the last arbitration (captured by the Interrupt Bus latches) is stored in CIR. Otherwise, the next EVAL pulse is inhibited and the value in the Interrupt Bus Latches is stored in CIR.

Clearing the Interrupt

Activities which change the state of the ISR will cause the IRQN to assert or negate. In addition, the accessing of a global or local RxFIFO or TxFIFO reduces the associated byte count for transmitter and receiver data interrupts. If the byte count falls below the threshold value, the interrupt request is withdrawn. Other interrupt conditions are cleared when the interrupting source is cleared.

Once the interrupt is cleared, the programmable value lowered or its byte count value reduced by one of the methods listed above, a different bidder (or no bidder at all) will win the on-going arbitration. When the winning bid drops below the Interrupt Threshold Register's value, the IRQN pin will negate.

Arbitration - Aftermath

At the end of the arbitration, i.e., the falling edge of EVAL, the winning interrupt source is driving its Channel number, number of bytes (if applicable) and interrupt type onto the Interrupt Bus. These values are captured into a latch by the trailing edge of EVAL. The output of this latch is used by the Interrupt Threshold comparator; the winning value is captured into another set of latches called the Current Interrupt Register (CIR) at the time of an Interrupt Acknowledge cycle or execution of the "Update CIR" command.

The Current Interrupt Register and associated read logic is shown in Figure 5. Interrupting channel number and the three bit interrupt type code and FIFO fill level are readable via the Internal Data Bus.

The contents of the appropriate receiver or transmitter byte "counter", as captured at the time of IACKN assertion, make up bits 7:5 of the CIR. If the interrupt type stored in the Current Interrupt Register is not a receiver or transmitter data transfer type, the CIR7:5 field will read as the programmable fields of their respective bid formats.

The buffers driving the CIR to the DBUS also provide the means of implementing the Global Interrupting Channel and Global Byte Count Registers, described in a later section.

The winning bid channel number and interrupt type fields can also be used to generate part of the Interrupt Vector, as defined by the Interrupt Control Register.

Interrupt Context

The channel number of the winning "bid" is used by the address decoders to provide data from the interrupting UART channel via a set of Global pseudo-registers. The interrupt Global pseudo-registers are:

1. Global Interrupting Byte Count
2. Global Interrupting Channel
3. Global Receive Holding Register
4. Global Transmit Holding Register

The first two Global "registers" are provided by Current Interrupt Register fields as shown in Figure 5. The interrupting channel number latched in CIR modifies address decoding so that the Receive or Transmit Holding Register for the interrupting channel is accessed during I/O involving the Global Receive and Transmit Holding Registers. Similarly, for data interrupts from the transmitter and receiver, the number of characters available for transfer to the CPU or the number of transmit FIFO positions open is available by reading the Global Interrupt Byte Count Register. For non-data interrupts, a read of the Global Interrupt Byte Count Register yields a value equal to the highest programmable filed.

In effect, once latched by an IACK or the Update CIR command, the winning interrupt channel number determines the contents of the global registers. All Global registers will provide data from the interrupting UART channel.

Interrupt Threshold Calculation

The state of IRQN is determined by comparison of the winning "bid" value to the Interrupt Threshold field of the Interrupt Control Register.

The logic of the bidding circuit is such that when no interrupt source has a value greater than the interrupt threshold then the interrupt is not asserted and the CIR (Current Interrupt Register) is set to all ones. When one or more of the 18 interrupt sources which are enabled via the IMR (Interrupt Mask Register) exceed the threshold then the interrupt threshold is effectively disconnected from the bidding operation while the 18 sources now bid against each other. The final result is that the highest bidding source will disable all others and its value will be loaded to the CIR and the IRQN pin asserted low. This all occurs during each cycle of the X1, X2 crystal clock.

RECEIVER INPUT FILL LEVEL

MR0[6]	MR1[6]	Interrupt Condition
0	0	1 or more bytes in FIFO (Rx RDY) default*
0	1	6 or more bytes in FIFO
1	0	4 or more bytes in FIFO
1	1	8 or more bytes in FIFO (Rx FULL)
MR0[5:4] – Tx Interrupt fill level		
MR0[5]	**MR0[4]**	**Interrupt Condition**
0	0	8 bytes empty (Tx EMPTY) default*
0	1	4 or more bytes empty
1	0	6 or more bytes empty
1	1	1 or more bytes empty (Tx RDY)

*These conditions, for interrupt purposes, make the RxFIFO look like a 3 byte FIFO; the TxFIFO a 1 byte FIFO. This is to allow software compatibility with previous Philips UART devices. Both FIFOs accept 8 bytes of data regardless of this bit setting. Only the interrupt is affected.

INTERRUPT NOTE ON 26C94:

For the receivers and transmitters, the bidding of any particular unit may be held off unless one of four FIFO fill levels is attained. This is done by setting the RxINT and TxINT bits in MR0 and MR1 to non-zero values. This may be used to prevent a receiver or transmitter from generating an interrupt even though it is filed above the bid threshold. Although this is not in agreement with the idea that each enabled interrupt source bid with equal authority, it does allow the flexibility of giving particular receiver or transmitters more interrupt importance than others.

This may be used when the Interrupt Threshold is set at or above 100000. Note than in this case the transmitter cannot generate an interrupt. If the interrupt threshold MSBs were set to 011 *and* the 'Receiver Interrupt Bits' on the MR registers set to a value other than 00 then the RxFIFO could not generate and interrupt until it had 4, 6 or 8 bytes. This in effect partially defeats the hardwired characteristic that the receiver interrupts should have more importance than the transmitter. This characteristic has been implemented by setting the MSB of the transmitter bid to zero.

Vectored Interrupts

The QUART responds to an Interrupt Acknowledge (IACK) initiated by the host by providing an Interrupt Acknowledge Vector on D7:0. The interrupt acknowledge cycle is terminated with a DACKN pulse. The vector provided by the QUART can have one of the three forms under control of the IVC control field (bits 1:0 of the Interrupt Control Register):

With IVC = 00 (IVR only)

IVR7:0
8

With IVC = 01 (channel number)

IVR7:2	Chan #
6	2

With IVC = 10 (type & channel number)

IVR7:5	Type	Chan #
3	3	2

A code of 11 in the Interrupt Vector Control Field of the ICR results in NO interrupt vector being generated. The external data bus is driven to a high impedance throughout the IACK cycle. A DACKN will be generated normally for the IACK cycle, however.

NOTE: If IACKN is not being used then the command "UPDATE CIR" must be issued for the global and interrupt registers to be updated.

PROGRAMMING UART CONTROL REGISTERS

The operation of the QUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. Addressing of the registers is described in Table 1.

The bit formats of the QUART registers are depicted in Table 2.

Table 2. Register Bit Formats, Duart ab. [duplicated for Duart cd]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

MR0 (Mode Register 0)

Rx Watchdog Timer	RxINT2 bit	TxINT Control	These bits not implemented. They should be considered Reserved.			
0 = off 1 = on	These bits should normally be set to 0		x	x	x	x

MR1 (Mode Register 1)

RxRTS Control	RxINT1 Select	Error Mode	Parity Mode	Parity Type	Bits per Character
0 = No 1 = Yes	Normally set to 0	0 = Char 1 = Block	00 = With parity 01 = Force parity 10 = No parity 11 = Wake-up mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

MR2 (Mode Register 2)

Channel Mode	TxRTS Control	CTS Enable Tx	Stop Bit Length*
00 = Normal 01 = Auto-echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 4 = 0.813 8 = 1.563 C = 1.813 1 = 0.625 5 = 0.875 9 = 1.625 C = 1.875 2 = 0.688 6 = 0.938 A = 1.688 E = 1.938 3 = 0.750 7 = 1.000 B = 1.750 F = 2.000

NOTE: Add 0.5 to values shown above for 0–7, if channel is programmed for 5 bits/char.

CSR (Clock Select Register)

Receiver Clock Select	Transmitter Clock Select
See text	See text

CR (Command Register)

Miscellaneous Commands	Disable Tx	Enable Tx	Disable Rx	Enable Rx
See text	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE: Issuing commands contained in the upper four bits of the "Command Register" should be separated in time by at least three (3) X1 clock edges. Allow four (4) edges if the "X1 clock divide by 2" mode is used. A disabled transmitter cannot be loaded.

SR (Status Register)

Rec'd. Break	Framing Error	Parity Error	Overrun Error	TxEMT	TxRDY	RxFULL	RxRDY
0 = No 1 = Yes *	0 = No 1 = Yes *	0 = No 1 = Yes *	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE: These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits [7:5] from the top of the FIFO together with bits [4:0]. These bits are cleared by a reset error status command. Unless reset with the 'Error Reset' (CR command 40) or receiver reset, these bits will remain active in the Status Register after the RxFIFO is empty.

ACR (Auxiliary Control Register)

BRG Set Select	Counter/Timer Mode and Source	Delta I/O1b	Delta I/O0b	Delta I/O1a	Delta I/O0a
0 = set 1 1 = set 2	See text	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

IPCR (Input Port Change Register)

Delta I/O1b	Delta I/O0b	Delta I/O1a	Delta I/O0a	I/O1b	I/O0b	I/O1a	I/O0a
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

Table 2. Register Bit Formats, Duart ab. [duplicated for Duart cd] (continued)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

ISR (Interrupt Status Register)

I/O Port Change	Delta BREAKb	RxRDY/ FFULLb	TxRDYb	Counter Ready	Delta BREAKa	RxRDY/ FFULLa	TxRDYa
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

IMR (Interrupt Mask Register)

I/O Port Change INT	Delta BREAKb INT	RxRDY/ FFULLb INT	TxRDYb INT	Counter Ready INT	Delta BREAKa INT	RxRDY/ FFULLa INT	TxRDYa INT
0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

CTUR (Counter/Timer Upper Register)

C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]

CTUR (Counter/Timer Lower Register)

C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]

IPR (Input Port Register)

I/O3b	I/O2b	I/O3a	I/O2a	I/O1b	I/O0b	I/O1a	I/O0a
0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

Mode Registers 0, 1 and 2

The addressing of the Mode Registers is controlled by the MR Register pointer. On any access to the Mode Registers this pointer is always incremented. Upon reaching a value of 2 it remains at 2 until changed by a CR command or a hardware reset.

MR0 – Mode Register 0

Mode Register 0 (MR0) is part of the UART configuration registers. It controls the watch dog timer and the encoding of the number of characters received in the RxFIFO. The lower four bits of this register are not implemented in the hardware of the chip. MR0 is normally set to either 80h or 00h. A read of this register will return 1111 (Fh) in the lower four bits.

The MR0 register is accessed by setting the MR Pointer to zero (0) via the command register command 1011 (Bh).

MR0[7]: This bit enables or disables the RxFIFO watch dog timer.

MR0[7] = 1 enable timer

MR0[7] = 0 disable timer

MR0[6:4]: These bits are normally set to 0 except as noted in the "Interrupt Threshold Calculation" description

MR0[3:0]: These bits are not implemented in the chip. These bits should be be considered "reserved."

MR1 – Mode Register 1

MR1 is accessed when the MR pointer points to MR1. The pointer is set to MR1 by RESET, a set pointer command applied via the CR or after an access to MR0. After reading or writing MR1, the pointers are set at MR2.

MR1[7] – Receiver Request-to-Send Flow Control

This bit controls the deactivation of the RTSN output (I/O2x) by the receiver. This output is manually asserted and negated by commands applied via the command register. MR1[7] = 1 causes RTSN to be automatically negated upon receipt of a valid start bit if the receiver FIFO is full. RTSN is re-asserted when an empty FIFO position is available. This feature can be used to prevent overrun in the receiver by using the RTSN output signal to control the CTS input (the QUART I/O0 pin) of the transmitting device.

Use of this feature requires the I/O2 pin to be programmed as output via the I/OPCR and to be driving a 0 via the OPR. When the RxFIFO is full and the start bit of the ninth character is sensed the receiver logic will drive the I/O2 pin high. This pin will return low when another RxFIFO position is vacant.

MR1[6] – Receiver Interrupt Select 1

This bit is normally set to 0 except as noted in the "Interrupt Threshold Calculation" description. MR1[6] operates with MR0[6] to prevent the receiver from bidding until a particular fill level is attained. For software compatibility this bit is designed to emulate the RxFIFO interrupt function of previous Philips Semiconductors UARTs.

MR1[5] – Error Mode Select

This bit selects the operating mode of the three FIFOed status bits (received break, FE, PE). In the character mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO.

In the block mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last reset error command was issued.

In the "Block Error" mode the ORing of the error status bits and the presentation of them to the status register takes place as the bytes enter the RxFIFO. This allows an indication of problem data when the error occurs after the leading bytes have been received. In the character mode the error bits are presented to the status register when the corresponding byte is at the top of the FIFO.

MR1[4:3] – Parity Mode Select
If "with parity" or "force parity" is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR1[4:3] = 11 selects the channel to operate in the special wake-up mode (see 'Wake-Up Mode').

MR1[2] – Parity Type Select
This bit selects the parity type (odd or even) if the "with parity" mode is programmed by MR1[4:3], and the polarity of the forced parity bit if the "force parity" mode is programmed. It has no effect if the "no parity" mode is programmed. In the special "wake-up" mode, it selects the polarity of the transmitted A/D bit.

MR1[1:0] – Bits per Character Select
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2 – Mode Register 2

MR2 is accessed when the channel MR pointer points to MR2, which occurs after any access to MR1. Accesses to MR2 do not change the pointer.

MR2[7:6] – Mode Select
The QUART can operate in one of four modes. MR2[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2[7:6] = 01 places the channel in the automatic echo mode, which automatically re-transmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is re-clocked and retransmitted on the TxD output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.

Two diagnostic modes can also be selected. MR2[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxD output is held high.
4. The RxD input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2[7:6] = 11. In this mode:

1. Received data is re-clocked and retransmitted on the TxD output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., the transmitted parity bit is as received.
5. The receiver must be enabled, but the transmitter need not be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected, the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes; if the deselection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop bit has been retransmitted.

MR2[5] – Transmitter Request-to-Send Control

NOTE: When the transmitter controls the I/O2 pin (usually used for the RTSN signal) the meaning of the pin is not RTSN at all! Rather it signals that the transmitter has finished transmission. (i.e., end of block).

This bit controls the deactivation of the RTSN output (I/O2) by the transmitter. This output is manually asserted and negated by appropriate commands issued via the command register. MR2[5] = 1 causes RTSN to be reset automatically one bit time after the characters in the transmit shift register and in the TxFIFO (if any) are completely transmitted (includes the programmed number of stop bits if the transmitter is not enabled). This feature can be used to automatically terminate the transmission as follows:

1. Program auto-reset mode: MR2[5] = 1.
2. Enable transmitter.
3. Assert RTSN via command.
4. Send message.
5. Verify the next to last character of the message is being sent by waiting until transmitter ready is asserted. Disable transmitter after the last character of the message is loaded in the TxFIFO.
6. The last character will be transmitted and RTSN will be reset one bit time after the last stop bit.

MR2[4] – Transmitter Clear-to-Send Flow Control
The sate of this bit determines if the CTSN input (I/O0) controls the operation of the transmitter. If this bit is 0, CTSN has no effect on the transmitter. If this bit is a 1, the transmitter checks the sate of CTSN each time it is ready to send a character. If it is asserted (Low), the character is transmitted. If it is negated (High), the TxD output remains in the marking state and the transmission is delayed until CTSN goes Low. Changes in CTSN, while a character is being transmitted do not affect the transmission of that character. This feature can be used to prevent overrun of a remote receiver.

MR2[3:0] – Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1–9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1–1/16 to 2 stop bits can be programmed in increments of 1/16 bit. If an external 1X clock is used for the transmitter, MR2[3] = 0 selects one stop bit and MR2[3] = 1 selects two stop bits to be transmitted.

RECEIVER NOTE: In all cases, the receiver only checks for a "mark" condition at the center of the stop bit (1/2 to 9/16 bit time into the stop bit position). At this time the receiver has

finished processing the present character and is ready to search for the start bit of the next character.

Table 3. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz

NORMAL RATE (BAUD)	ACTUAL 16X CLOCK (kHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2K	307.2	0
38.4K	614.4	0

NOTE: Duty cycle of 16X clock is 50% ± 1%.

CR – Command Register

CR is used to write commands to the QUART.

CR[7:4] – Miscellaneous Commands

Issuing commands contained in the upper four bits of the "Command Register" should be separated in time by at least three (3) X1 clock edges. Allow four (4) edges if the "X1 clock divide by 2" mode is used. The encoded value of this field can be used to specify a single command as follows:

0000 No command.

0001 Reset MR pointer. Causes the MR pointer to point to MR1.

0010 Reset receiver. Resets the receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO pointer is reset to the first location.

0011 Reset transmitter. Resets the transmitter as if a hardware reset had been applied.

0100 Reset error status. Clears the received break, parity error, framing error, and overrun error bits in the status register (SR[7:4]). Used in character mode to clear OE status (although RB, PE, and FE bits will also be cleared), and in block mode to clear all error status after a block of data has been received.

0101 Reset break change interrupt. Causes the break detect change bit in the interrupt status register (ISR[2 or 6]) to be cleared to zero.

0110 Start break. Forces the TxD output low (spacing). If the transmitter is empty, the start of the break condition will be delayed up to two bit times. If the transmitter is active, the break begins when transmission of the character is completed. If a character is in the TxFIFO, the start of break is delayed until that character or any others loaded after it have been transmitted (TxEMT must be true before break begins). The transmitter must be enabled to start a break

0111 Stop break. The TxD line will go high (marking) within two bit times. TxD will remain high for one bit time before the next character, if any, is transmitted.

1000 Assert RTSN. Causes the RTSN output to be asserted (Low).

1001 Negate RTSN. Causes the RTSN output to be negated (High).

1010 Set Timeout Mode On. The register in this channel will restart the C/T as each receive character is transferred from the shift register to the RxFIFO. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset.
Only one receiver should use this mode at a time. However, if both are on, the timeout occurs after both receivers have been inactive for the timeout. The start of the C/T will be on the logical 'OR' of the two receivers.

1011 Set MR Pointer to 0.

1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued.

1101 Reserved.

111x Reserved for testing.

CSR – Clock Select Register

CSR[7:4] – Receiver Clock Select

When using a 3.6864MHz crystal or external clock input, this field selects the baud rate clock for the receiver as shown in Table 3.

The receiver clock is always a 16X clock, except for CSR[7:4] = 1111. I/O2x is external input.

CSR[3:0] – Transmitter Clock Select

This field selects the baud rate clock for the transmitter. The field definition is as shown in Table 3, except as follows:

CSR[3:0]	ACR[7] = 0	ACR[7] = 1
1 1 1 0	I/O3x – 16X	I/O3x – 16X
1 1 1 1	I/O3x – 1X	I/O3x – 1X

Table 4. Baud Rate

	BRG RATE = LOW		BRG RATE = HIGH		TEST 1 = 1	
CSR[7:4]	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0 0 0 0	50	75	50	450	4,800	7,200
0 0 0 1	110	110	110	110	880	880
0 0 1 0	134.5	38.4k	134.5	230.4K	1,076	38.4K
0 0 1 1	200	150	200	900	19.2K	14.4K
0 1 0 0	300	300	1800	1,800	28.8K	28.8K
0 1 0 1	600	600	3,600	3,600	57.6K	57.6K
0 1 1 0	1,200	1,200	7,200	7,200	115.2K	115.2K
0 1 1 1	1,050	2,000	1,050	2,000	1,050	2,000
1 0 0 0	2,400	2,400	14.4K	14.4K	57.6K	57.6K
1 0 0 1	4,800	4,800	28.8K	28.8K	4,800	4,800
1 0 1 0	7,200	1,800	7,200	1,800	57.6K	14.4K
1 0 1 1	9,600	9,600	57.6K	57.6K	9,600	9,600
1 1 0 0	38.4k	19.2k	230.4K	115.2K	38.4K	19.2K
1 1 0 1	Timer	Timer	Timer	Timer	Timer	Timer
1 1 1 0	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X
1 1 1 1	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X

CR[3] – Disable Transmitter
This command terminates transmitter operation and resets the TxRDY and TxEMT status bits. However, if a character is being transmitted or if a character is in the TxFIFO when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

While the transmitter is disabled (or a disable is pending), the TxFIFO may not be loaded.

CR[2] – Enable Transmitter
Enables operation of the transmitter. The TxRDY and TxEMT status bits will be asserted.

CR[1] – Disable Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. However any unread characters in the RxFIFO area are still available. Disable is not the same as a "receiver reset". With a receiver reset any characters not read are lost. The command has no effect on the receiver status bits or any other control registers. If the special wake–up mode is programmed, the receiver operates even if it is disabled (see Wake-up Mode).

CR[0] – Enable Receiver
Enables operation of the receiver. If not in the special wake-up mode, this also forces the receiver into the search for start bit state.

SR – Channel Status Register

SR[7] – Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received; further entries to the FIFO are inhibited until the RxDA line returns to the marking state for at least one-half bit time (two successive edges of the internal or external 1X clock).

When this bit is set, the change in break bit in the ISR (ISR[6 or 2]) is set. ISR[6 or 2] is also set when the end of the break condition, as defined above, is detected. The break detect circuitry is capable of detecting breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must last until the end of the next character in order for it to be detected.

SR[6] – Framing Error (FE)
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SR[5]– Parity Error (PE)
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity. In 'wake-up mode', the parity error bit stores the received A/D (Address/Data) bit.

In the wake-up mode this bit follows the polarity of the A/D parity bit as it is received. A parity of 1 would normally mean address and therefore, the end of a data block.

SR[4] – Overrun Error (OE)
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a reset error status command.

SRA[3] – Channel A Transmitter Empty (TxEMTA)
This bit will be set when the transmitter underruns, i.e., both the TxEMT and TxRDY bits are set. This bit and TxRDY are set when the transmitter is first enabled and at any time it is re-enabled after either (a) reset, or (b) the transmitter has assumed the disabled state. It is always set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission.

It is reset when the THR is loaded by the CPU, a pending transmitter disable is executed; the transmitter is reset, or the transmitter is disabled while in the underrun condition.

SR[2] – Transmitter Ready (TxRDY)
This bit, when set, indicates that the TxFIFO has at least one empty location that may be loaded by the CPU. It sets when the transmitter is first enabled. It is cleared when the TxFIFO is full (eight bytes); the transmitter is reset; a pending transmitter disable is executed; the transmitter is disabled when it is in the underrun condition. When this bit is **not** set characters written to the TxFIFO will not be loaded or transmitted; they are lost.

SR[1] – RxFIFO Full (FFULL)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all eight FIFO positions are occupied. It is reset when the CPU reads the FIFO and there is no character in the receive shift register. If a character is waiting in the receive shift

register because the FIFO is full, FFULL is not reset after reading the FIFO once.

SR[0] – RxFIFO Ready (RxRDY)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RxFIFO, and no more characters are in the FIFO.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects between two sets of baud rates that are available within each baud rate group generated by the BRG. See Table 3.

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.

Set 2: 75, 110, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, 19.2k, and 38.4k baud.

The selected set of rates is available for use by the receiver and transmitter.

ACR[6:4] – Counter/Timer Mode and Clock Source Select
This field selects the operating mode of the counter/timer and its clock source (see Table 4).

The I/O pins available for counter/timer clock source is I/O1a and I/O1c. The counter/timer clock selection is connected to the I/O1 pin and will accept the signal on this pin regardless of how it is programmed by the I/OPCR.

Table 5. ACR[6:4] C/T Clock and Mode Select

[6:4]	Mode	Clock Source
0 0 0	Counter	I/O1 pin
0 0 1	Counter	I/O1 pin divided by 16
0 1 0	Counter	TxC1XA clock of the transmitter
0 1 1	Counter	TxC1XB clock of the transmitter
1 0 0	Timer	I/O1 pin
1 0 1	Timer	I/O1 pin divided by 16
1 1 0	Timer	Crystal or external clock (X1/CLK)
1 1 1	Timer	Crystal or external clock (X1/CLK) divided by 16
The timer mode generates a squarewave		

ACR[3:0] – I/O1b, I/O0b, I/O1a, I/O0a Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register, ISR[7], to be set and thus allow the Change of State Detectors to enter the bidding process. If a bit is in the 'on' state, the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which may result in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – I/O1b, I/O0b, I/O1a, I/O0a Change-of-State Detectors
These bits are set when a change of state, as defined in the Input Port section of this data sheet, occurs at the respective pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – I/O1b, I/O0b, I/O1a, I/O0a State of I/O Pins
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins during the time the IPCR is read. The IPR is an unlatched register. Data can change during a read.

ISR – Interrupt Status Register

Important: The setting of these bits and those of the IMR are essential to the interrupt bidding process.

This register provides the status of all potential interrupt sources. The contents of this register are masked by the interrupt mask register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', then the interrupt source represented by this bit is allowed to enter the interrupt arbitration process. It will generate an interrupt (the assertion of INTRN low) only if its bid exceeds the interrupt threshold value. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR; the complete status is provided regardless of the contents of the IMR.

ISR[7] – I/O Change-of-State
This bit is set when a change-of-state occurs at the I/O1b, I/O0b, I/O1a, I/O0a input pins. It is reset when the CPU reads the IPCR.

ISR[6] – Channel b Change in Break
This bit, when set, indicates that the receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a reset break change interrupt command.

ISR[5] – Receiver Ready or FIFO Full Channel b
Normally the ISR[5] bit being set to one indicates the RxFIFO is filled with one or more bytes and/or the receiver watch dog timer (when enabled) has timed out.

The meaning of ISR[5] is controlled by the MR0[6] and MR1[6] bits which are normally set to 00. The ISR[5] bit setting to one allows the receiver to present its bid to the arbitration logic. This function is explained in the "Interrupt Note On 26C94" and under the "Receiver Interrupt Fill Level".

ISR[5], if set, will reset when the RxFIFO is read. If the reading of the FIFO does not reduce the fill level below that determined by the MR bits, then ISR[5] sets again within two X1 clock times. Further, if the MR fill level is set at 8 bytes AND there is a byte in the receiver shift register waiting for an empty FIFO location, then a read of the RxFIFO will cause ISR[5] to reset. It will immediately set again upon the transfer of the character in the shift register to the FIFO.

NOTE: The setting of ISR[5] means that the receiver has entered the bidding process. It is necessary for this bit to set for the receiver to generate an interrupt. It does **not** mean it **is** generating an interrupt.

ISR[4] – Transmitter Ready Channel b
The function of this bit is programmed by MR0[5:4] (normally set to 00). This bit is set when ever the number of empty TxFIFO positions exceeds or equals the level programmed in the MR0 register. This condition will almost always exist when the transmitter is first enabled. It will reset when the empty TxFIFO positions are reduced to a level less than that programmed in MR0[5:4] or the transmitter is disabled or reset.

The ISR[4] bit will reset with each write to the TxFIFO. If the write to the FIFO does not bring the FIFO above the fill level determined by the MR bits, the ISR[4] bit will set again within two X1 clock times.

NOTE: The setting of ISR[4] means that the transmitter has entered the bidding process. It is necessary for this bit to set for the transmitter to generate an interrupt. It does **not** mean it **is** generating an interrupt.

ISR[3] – Counter Ready
In the counter mode of operation, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command. It is initialized to '0' when the chip is reset.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time the C/T reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the C/T.

ISR[2] – Channel a Change in Break
This bit, when set, indicates that the receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a reset break change interrupt command.

ISR[1] – Receiver Ready or FIFO Full Channel a
See the description of ISR[5]. The channel 'a' receiver operation is the same as channel 'b'.

ISR[0] – Transmitter Ready Channel a
See the description of ISR[4]. Channel "a" transmitter operates in the same manner as channel "b."

IMR – Interrupt Mask Register

The programming of this register selects which interrupt sources will be allowed to enter the interrupt arbitration process. This register is logically ANDED with the interrupt status register. Its function is to allow the interrupt source it represents to join the bidding process if the corresponding IMR and ISR bits are both 1. It has no effect on the value in the ISR. It does not mask the reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read address at A5–A0 0Eh for C/T ab or read address 1Eh for C/T cd). After this, while in timer mode, the C/T will run continuously. Receipt of a subsequent start counter command causes the C/T to terminate the current timing cycle and to begin a new cycle using the values in the CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a "Stop Counter" command (read address at A5–A0 0Fh for C/T ab or read address 1Fh for C/T cd). The command, however, does not stop the C/T. It only resets the ISR[3] bit; the C/T continues to run. The ISR[3] bit will set again as the counter passes through 0. The generated square wave is output on an I/O pin if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded in CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching the terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter rolls over to 65535 and continues counting until stopped by the CPU. If I/O is programmed to be the output of the C/T, the output remains High until the terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower eight bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower eight bits to the upper eight bits occurs between the times that both halves of the counter is read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

I/O LOGIC

The QUART has four I/O pins for each channel. These pins may be individually programmed as an input or output under control of the I/OPCR (I/O Port Control Register). Functions which may use the I/O pins as inputs (Rx or Tx external clock, for example) are always sensitive to the signal on the I/O pin regardless of it being programmed as an input or an output. For example if I/O1a was programmed to output the RxC1X clock and the Counter/Timer was programmed to use I/O pin as its clock input the result would be the Counter/Timer being clocked by the RxC1X clock.

The 16 I/O ports are accessed and/or controlled by five (5) registers: IPR, ACR, I/OPCR, IPCR, OPR. They are shown in Table 6 of this document. Each UART has four pins. Two of these pins have "Change of State Detectors" (COS). These detectors set whenever the pin to which they are attached changes state. (1 to 0 or 0 to 1) The "Change of State Detectors" are enabled via the ACR. When enabled the COS devices may generate interrupts via the IMR and IPCR registers. Note that when the COS interrupt is enabled that any one or more of the four COS bits in the IPCR will enable the COS bidding. Each of the channel's four I/O lines are configured as inputs on reset.

The Change of State detectors sample the I/O pins at the rate of the 38.4KHz clock. A change on the pin will be required to be stable for at least 26.04µs and as much as 52.08µs for the COS detectors to confirm a change. Note that changes in the X1/clock frequency will effect this stability requirement.

Table 6.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

IPCR (Input Port Change Register ab) The lower four bits replicate the lower four bits of the IPR. The upper four bits reads state of Change detectors. Change detectors are enabled in ACR[3:0]. (DUART ab)

Delta I/O1b	Delta I/O0b	Delta I/O1a	Delta I/O0a	I/O1b	I/O0b	I/O1a	I/O0a
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

IPCR (Input Port Change Register cd) The lower four bits replicate the lower four bits of the IPR. The upper four bits reads state of Change detectors. Change detectors are enabled in ACR[3:0]. (DUART cd)

Delta I/O1d	Delta I/O0d	Delta I/O1c	Delta I/O0c	I/O1d	I/O0d	I/O1c	I/O0c
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

I/OPCR (I/O Port Configuration Register) One register for each UART.

I/O3x CONTROL	I/O2x CONTROL	I/O1x CONTROL	I/O0x CONTROL
Two bits for each I/O pin.			

This register controls the configuration of the I/O ports. It defines them as inputs or outputs and controls what sources will drive them in the case of outputs or which functions they will drive when used as an input. Each pin has four functions and hence two bits to control it. Each UART has one eight bit register to control its four I/O ports.

OPR (Output Port Register cd) for DUART cd

I/O3d	I/O2d	I/O3c	I/O2c	I/O1d	I/O0d	I/O1c	I/O0c
One bit for each pin. When I/O pins are configured as "General Purpose Outputs" the pins will be driven to the complement value of its associated OPR bit.							

OPR (Output Port Register ab) for DUART ab

I/O3b	I/O2b	I/O3a	I/O2a	I/O1b	I/O0b	I/O1a	I/O0a
One bit for each pin. When I/O pins are configured as "General Purpose Outputs" the pins will be driven to the complement value of its associated OPR bit.							

This register contains the data for the I/O ports when they are used as 'General Purpose Outputs' . The bits of the register are controlled by writing to the hex addresses at 0C and 1C. Ones written to the OPR drive the pins to 0; zeros drive the pins to 1. (The pins drive the value of the complement data written to the OPR)

IPR (Input Port Register cd) Reads I/O pins for DUART cd

I/O3d	I/O2d	I/O3c	I/O2c	I/O1d	I/O0d	I/O1c	I/O0c
0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

IPR (Input Port Register ab) Reads I/O pins for DUART ab

I/O3b	I/O2b	I/O3a	I/O2a	I/O1b	I/O0b	I/O1a	I/O0a
0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

This register reads the state of the 'I/O Ports'. The state of the I/O ports is read regardless of being programmed as inputs or outputs. The IPR can be thought of a just another 8 bit parallel port to the system data bus. The lower four bits of this register are replicated in the lower four bits of the IPCR register.

I/O Port Control Channel A (Channel C is similar)

IOPCR	IOPCRa[7:6]	IOPCRa[5:4]	IOPCRa[3:2]	IOPCRa[1:0]
	I/O3A	I/O2A	I/O1A	I/O0A
IOPCR = 00	IPR(5), TxCA in	IPR(4), RxCA in	IPR(1), C/Tab Clk in[1] TxCA in	IPR(0), CTSAN
IOPCR = 01	OPRab(5)	OPRab(4) RTSAN[1]	OPRab(1) RTSAN[2]	OPRab(0)
IOPCR = 10	TxC16A	RxC1A	RxC16A	TxC1A
IOPCR = 11	TxC1A	RxC16A	RxC1A	TxC16A

I/O Port Control Channel B (Channel D is similar)

IOPCR	IOPCRb[7:6]	IOPCRb[5:4]	IOPCRb[3:2]	IOPCRb[1:0]
	I/O3B	I/O2B	I/O1B	I/O0B
IOPCR = 00	IPR(7), TxCB in	IPR(6), RxCB in	IPR(3), TxCB in[1]	IPR(2), CTSBN
IOPCR = 01	OPRab(7)	OPRab(6) RTSBN[1]	OPRab(3) RTSBN[2]	OPRab(2)
IOPCR = 10	TxC16B	RxC1B	RxC16B	TxC1B
IOPCR = 11	TxC1B	RxC16B	RxC1B	TxC16B
The input part of the I/O pins is always active. The programming of the IOPCR bits to 00 merely turns off the out drivers and places the pin at high impedance.				

A read of the IPR register returns the value of the IPR bits as shown above. IPR(5) is at bit position 5 of the data bus. Note that the IPR bit positions do not follow the 0, 1, 2, 3 order of the I/O ports. During a read of the IPR the I/O ports are not latched. Therefore, it is possible to see changing data during the read. Port pins that have clocks on them may not yield valid data during the read.

Since the input circuits of the I/O ports are always active it is possible to direct the port signal back into the port. For example: I/O1 will output the RTS signal. Setting the Counter/Timer (C/T) to be clocked by the I/O1 port will result in the counter counting the number of times RTS goes active. The change of state detectors on I/O0 and I/O1 will, when programmed, always be sensitive to the signal on the port regardless of the source of that port's signal.

NOTES:

1. Normal configurations place RTSN output on I/O1 and place Tx external clock input on I/O3. For the 48 pin Dual In-Line package, I/O3 is not available. The following options allow flexible I/O programming with the 48 pin package:
   When IOPCR(7:6), the I/O3 control, ≠ 00, then I/O1 becomes available to the transmitter as an external clock.
   When IOPCR(5:4), the I/O2 control, = 01, then I/O2 may be the RTSN signal if MR1(7) = 1 and OPR(4) = 1.
2. I/O1 becomes RTSN when IOPCR(3:2) = 01 and MR1(7) = 1 and OPR(1) = 1. (OPR(3) for channel B)

Registers of the Interrupt System

The CIR, and "Global" registers are updated with the IACKN signal or from the "Update CIR" command at hex address 2A. These registers are not updated when IRQN is asserted since there could be a long time between the assertion of IRQN and the start of the interrupt service routine. (See notes following this section).

Current Interrupt Register (CIR)

# Bytes	Type	Chan #
3	3	2

The Channel # field indicates which of the four UARTs has the highest priority interrupt currently outstanding, while the Type field indicates its source within the UART. The Type field is encoded as follows:

000 No Interrupt
001 Change of State
x10 Transmit available
011 Receive available, no error
100 Receiver break change
101 Counter/Timer
111 Receive available, w/errors

With Type = x11, the # Bytes field indicates the count of received bytes available for reading, while with Type = x10 it indicates the number of bytes that can be written to the transmit FIFO.

The CIR is Read only at address 28H.

Global Interrupt Byte Count (GIBC)

00000	# Bytes
5	3

The GIBC is not an actual register but simply outputs the interrupting UART's transmit or receive byte counter value. The count, accurate at the time IACKN asserts, is captured in the CIR. The high order 5 bits are read as '0'. The GIBC is read only at address 2AH.

Global RxFIFO (GRxFIFO)

Received Data
8

Like the GIBC, no physical register implementation exists. The correct receiver's FIFO is popped based on the value of the interrupting channel field of the Current Interrupt Register.

If a receiver is not the cause of the current interrupt, a read of the Global RxFIFO will yield a byte containing all ones and NONE of the UART channels' receive FIFOs will be popped. (IMPORTANT)

The GRxFIFO is Read only at address 2BH.

Global TxFIFO (GTxFIFO)

Data to be Sent
8

Similar to the GRxFIFO, no physical register implementation exists. The byte is pushed into the correct transmitter's FIFO based on the interrupting channel field of the Current Interrupt Register.

If a transmitter is not the cause of the current interrupt, a write to the Global TxFIFO has no effect.

The GTxFIFO is Write only at address 2BH.

Global Interrupting Channel (GICR)

000000	Chan #
6	2

Like the other Global pseudo-registers no hardware register exists. The Channel number field of the Current Interrupt Register padded with leading zeros is output as the GICR. The GICR is Read only at address 29H.

C/Tab indicated by Channel code B 01
C/Tcd indicated by Channel code D 11

Interrupt Control (ICR)

Threshold	IVC
6	2

The Threshold Field is used by the interrupt comparator to determine if a winning interrupt "bid" should result in interrupting the host MPU. The threshold field resets to 00.

The IVC field controls what kind of vector the QUART returns to the host MPU during an Interrupt Acknowledge cycle:

00 Output contents of Interrupt Vector Register
01 Output 6 MSBs of IVR and Channel number as 2 LSBs
10 Output 3 MSBs of IVR, Interrupt Type and Channel number
11 Disable generation of vector during IACK cycle

The IVC field reset to 00. The ICR is read/write at address 2CH.

Bidding Control Registers (BCRs)

Rcv'd Break	State Change	C/T
3	3	2

This register is a transparent latch. It must be set to ensure the expected operation of the arbitration system. The 3 MSBs determine the priority of Received Break Interrupts; they are reset to 000.

Bits 4:2 determine the priority of Change of Input State interrupts, and are reset to 00.
BCR Counter/Timer bits reset to 00.
There is one BCR per UART channel; they can be read or written at addresses 20-23H.

Interrupt Vector (IVR)

Always Used	with IVC = 0x	w/IVC = 01 or 10
3	3	2

Holds the constant bits of the interrupt acknowledge vector. As shown, the three MSBs are always used, while the less significant bits can be replaced by the interrupt type code and/or Channel code bits contained in the CIR. The IVR is write only at address 29H.

DC ELECTRICAL CHARACTERISTICS[5, 6, 7]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL} V_{IH} V_{IH}	Input low voltage Input high voltage (except X1/CLK) Input high voltage (X1/CLK)		 2.0 $0.8V_{CC}$		 0.8	V V V
V_{OL} V_{OH}	Output Low voltage Output High voltage (except OD outputs)	I_{OL} = 4.0mA I_{OH} = −400µA I_{OH} = −100µA	 $0.8V_{CC}$ $0.9V_{CC}$		0.4	V V V
I_{IL} I_{IH}	Input current Low, I/O ports Input current High, I/O ports	V_{IN} = 0 V_{IN} = V_{CC}	−10		 10	µA µA
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	−1		1	µA
I_{ILX1} I_{IHX1}	X1/CLK input Low current X1/CLK input High current	V_{IN} = GND, X2 = open V_{IN} = V_{CC}, X2 = open	−100		 100	µA µA
I_{OZH} I_{OZL}	Output off current High, 3–state data bus Output off current Low, 3–state data bus	V_{IN} = V_{CC} V_{IN} = 0	−1		10 1	µA
I_{ODL} I_{ODH}	Open–drain output Low current in off state: IRQN Open–drain output Low current in off state: IRQN	V_{IN} = 0 V_{IN} = V_{CC}	−1		1	µA
I_{CC}	Power supply current Operating mode	TTL input levels 25°C with X1 = 4MHz			50	mA
	Power down mode				5	

* See UART application note for power down currents less than 5µA.

AC ELECTRICAL CHARACTERISTICS[5, 6, 7, 8]

SYMBOL	FIGURE	PARAMETER	LIMITS			UNIT
			Min	Typ	Max	
Reset timing						
t_{RES}	7	Reset pulse width	200			ns
I/O Port timing						
t_{PS}	8	I/O input setup time before RDN Low	0			ns
t_{PH}	8	I/O input hold time after RDN High	0			ns
t_{PD}	8	I/O output valid from WRN High RDN Low			 110 110	 ns ns
Interrupt timing						
t_{IR}	9	INTRN negated or I/O output High from: Read RHR (RxRDY/FFULL interrupt) Write THR (TxRDY interrupt) Reset command (break change interrupt) Reset command (I/O change interrupt) Stop C/T command (counter interrupt) Write IMR (clear of interrupt mask bit) With respect to a 3.6864MHz clock on pin X1/CLK			 100 100 100 100 100 100	 ns ns ns ns ns ns
Clock timing						
t_{CLK}	10	X1/CLK low/high time	125/100			ns
t_{CLK}	10	X1/CLK low/high time (above 4MHz; X1/CLK ÷ 2 active)	56/56			ns
t_{CLK}	10	X1/CLK frequency	0[9]	3.6864	8.0	MHz
t_{CTC}	10	Counter/timer clock high or low time	60			ns
f_{CTC}	10	Counter/timer clock frequency	0[9]		8	MHz
t_{RX}	10	RxC high or low time	30			ns
f_{RX}	10	RxC frequency (16X) RxC frequency (1X)	0[9] 0[9]		16 1.0	MHz MHz
t_{TX}	10	TxC high or low time	30			ns
f_{TX}	10	TxC frequency (16X) TxC frequency (1X)	0[9] 0[9]		16 1.0	MHz MHz
Transmitter timing						
t_{TXD}	11	TxD output delay from TxC low			120	ns
t_{TCS}	11	TxC output delay from TxD output data	–20		+20	ns
Receiver timing						
t_{RXS}	12	RxD data setup time to RxC high	100			ns
t_{RXH}	12	RxD data hold time from RxC high	100			ns

NOTES:

1. Stress above these listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other condition above those indicated in the operation section of the specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range. See ordering information table for applicable temperature range and operating supply range.
5. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of V_{IL} and V_{IH}, as appropriate.
6. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
7. Test condition for interrupt and I/O outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}. Test conditions for rest of outputs: C_L = 150pF.
8. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
9. This value is not tested, but is guaranteed by design. For t_{CLK} minimum test rate is 2.0MHz.

AC ELECTRICAL CHARACTERISTICS[1]

T_A = 25°C; V_{CC} = 5V ± 10%, unless otherwise specified. Limits shown as nn/nn refer to Commercial/Industrial temperature range. Single numbers apply to both ranges.

NO.	FIGURE	CHARACTERISTIC	LIMITS			UNIT
			Min	Typ	Max	
1	2	A[5:0] Setup time to RDN WRN Low	10			ns
2	2	A[5:0] Hold time from RDN WRN Low	45			ns
3	2	CEN Setup time to RDN WRN Low[2]	0			ns
4	2	CEN Hold time from RDN WRN High[2]	0			ns
5	2	RDN WRN Pulse Width Low	110/115			ns
6	2	D[7:0] Data Valid after CEN and RDN Low			110/115	ns
7	2	D[7:0] Data Bus floating after RDN or CEN High			30	ns
8	2	D[7:0] Data Bus Setup time before WRN or CEN High	40			ns
9	2	D[7:0] Hold time after WRN or CEN High	8			ns
10	2	Time between Reads and/or Writes[3]	50			ns

NOTES:
1. Parameters are valid over specified temperature range. See ordering information table for applicable temperature range and operating supply range.
2. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as a 'strobing' input. CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence the signal asserted last initiates the cycle; the signal negated first terminates the cycle.
3. The RDN signal must be negated for this time to guarantee that internal registers update before the next read.

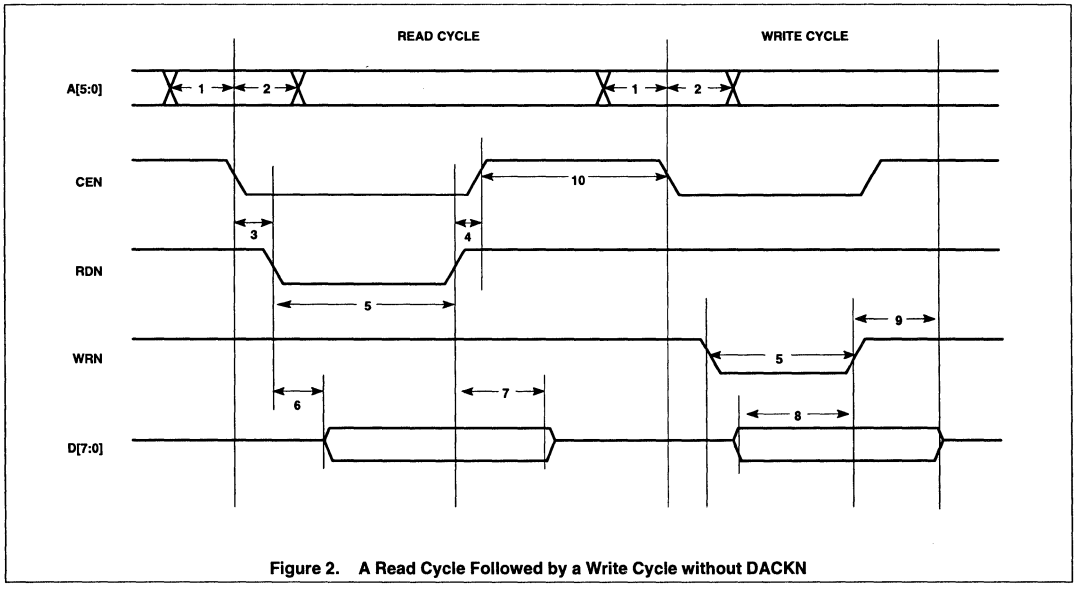


Figure 2. A Read Cycle Followed by a Write Cycle without DACKN

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$; $V_{CC} = 5V \pm 10\%$, unless otherwise specified. Limits shown as nn/nn refer to Commercial/Industrial temperature range. Single numbers apply to both ranges.

NO.	FIGURE	CHARACTERISTIC	LIMITS			UNIT
			Min	Typ	Max	
1	3	D[7:0] Valid after IACKN Low			110/115	ns
2	3	DACKN Low after IACKN Low	10 + 2 X1 edges[1]		90/122 + 3 X1 edges[1]	ns
3	3	D[7:0] floating after IACKN High	0		30	ns
4	3	DACKN High after IACKN High	0		30	ns
5	3	IACKN High after IACKN Low	110/115			ns

NOTE:
1. Consecutive write operations to the upper four bits of the Command Register (CR) require at least three X1/CLK edges; four X1/CLK edges in the 'X1/CLK divide by 2 edges' according to register 2E or 2F setting.

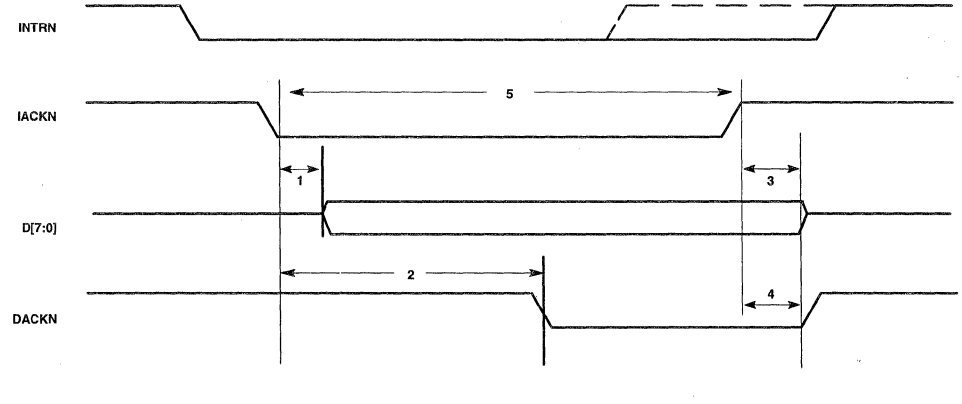


Figure 3. Interrupt Knowledge (IACKN) Timing

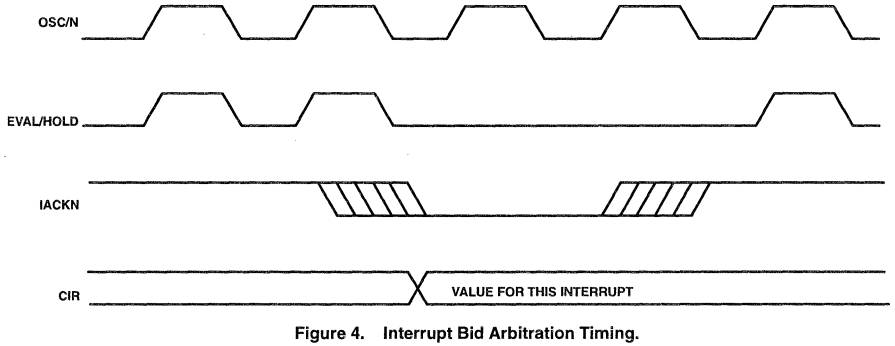


Figure 4. Interrupt Bid Arbitration Timing.

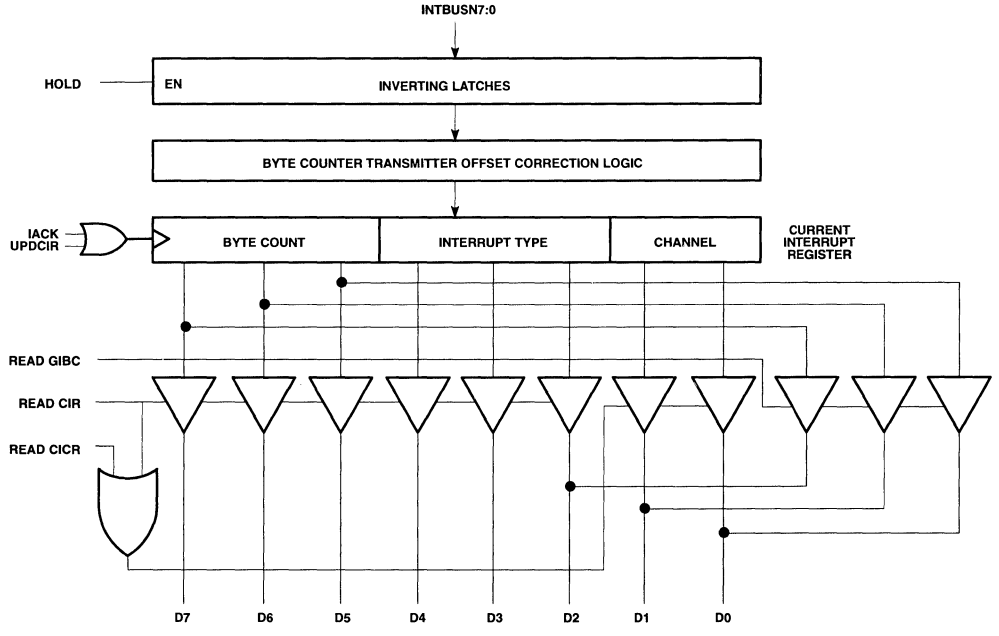


Figure 5. Current Interrupt Register Logic

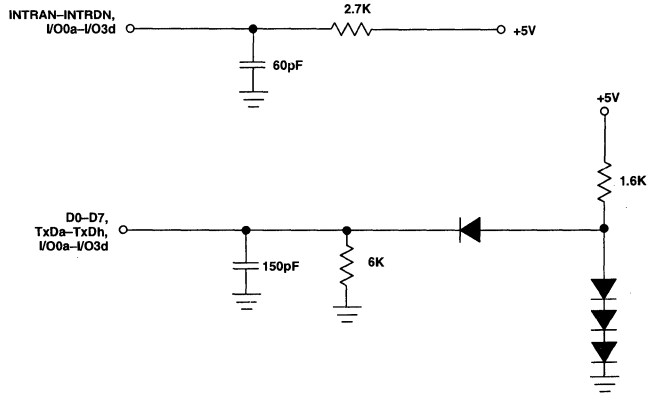


Figure 6. Test Conditions on Outputs

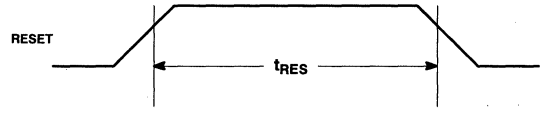
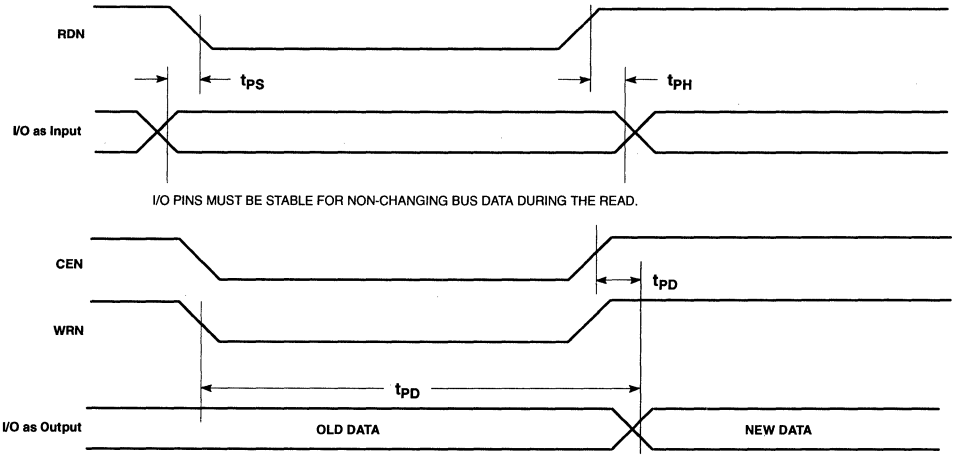
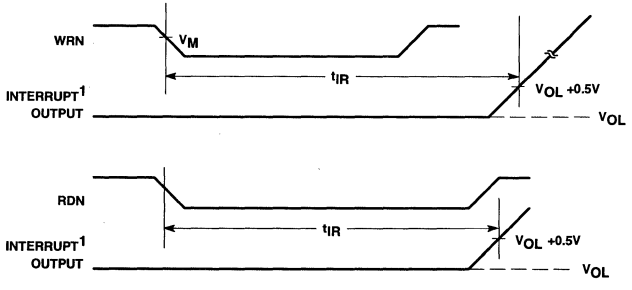


Figure 7. Reset Timing



NOTE: I/O PIN DATA IS NOT LATCHED

Figure 8. I/O Port Timing



NOTES:
1. INCLUDES I/O WHEN USED AS TxRDY or RxDY/FFULL OUTPUTS AS WELL AS INTRN.
2. THE TEST FOR OPEN DRAIN OUTPUTS IS INTENDED TO GUARANTEE SWITCHING OF THE OUTPUT TRANSISTOR. MEASUREMENT OF THIS RESPONSE IS REFERENCED FROM THE MIDPOINT OF THE SWITCHING SIGNAL, V_M, TO A POINT 0.5V ABOVE V_{OL}. THIS POINT REPRESENTS NOISE MARGIN THAT ASSURES TRUE SWITCHING HAS OCCURRED. BEYOND THIS LEVEL, THE EFFECTS OF EXTERNAL CIRCUITRY AND TEST ENVIRONMENT ARE PRONOUNCED AND CAN GREATLY AFFECT THE RESULTANT MEASUREMENT.

Figure 9. Interrupt Timing

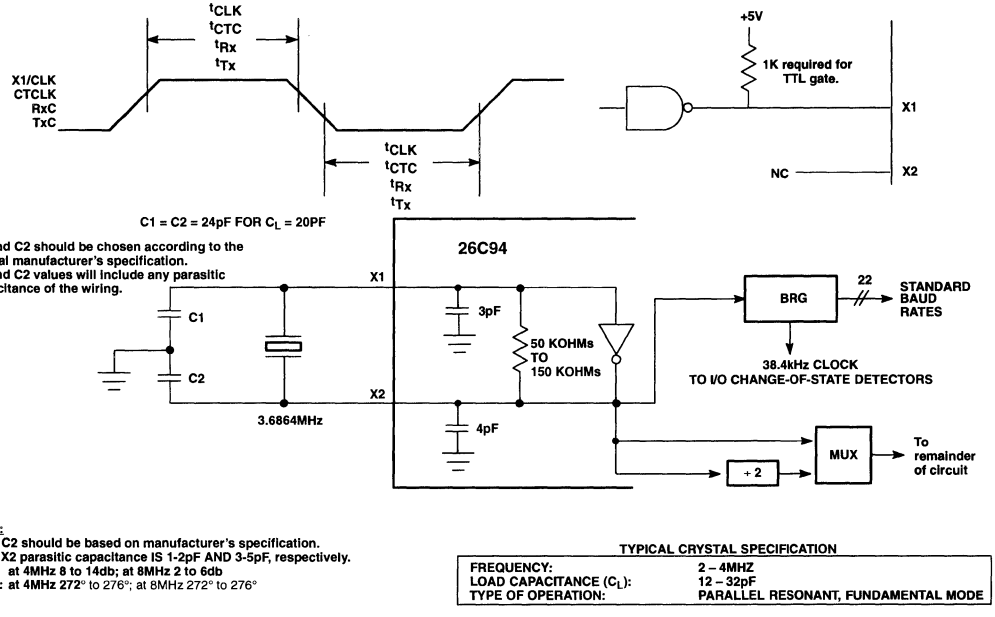


Figure 10. Clock Timing

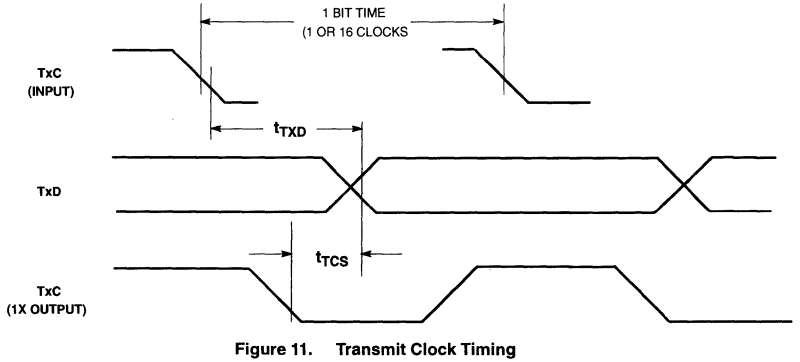


Figure 11. Transmit Clock Timing

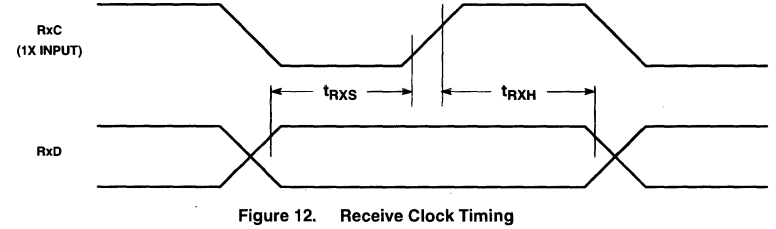


Figure 12. Receive Clock Timing

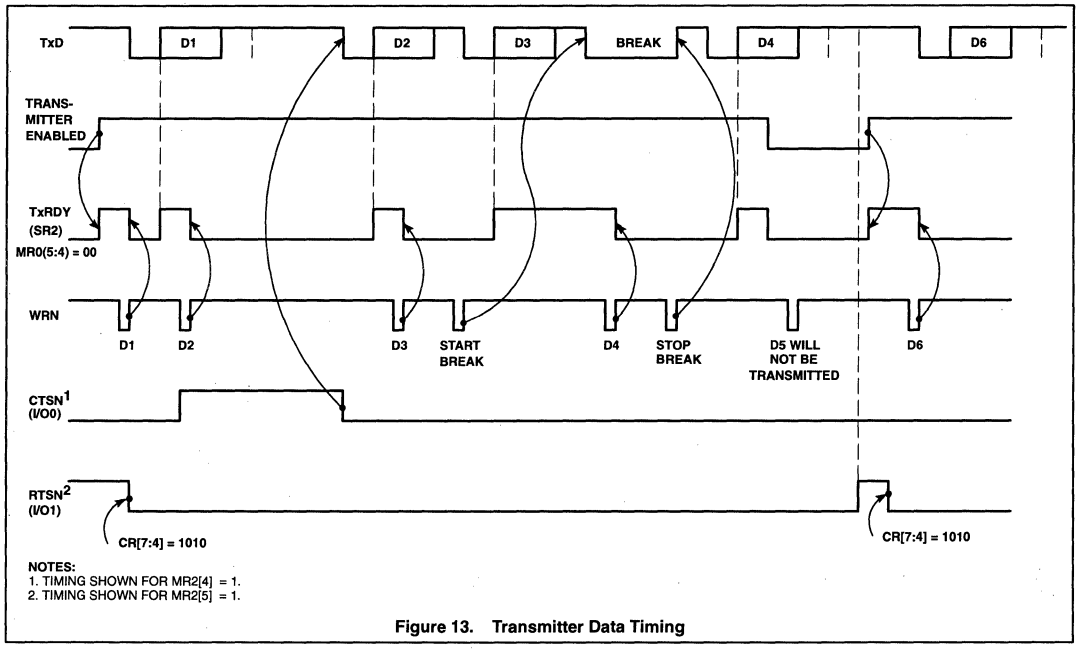


Figure 13. Transmitter Data Timing

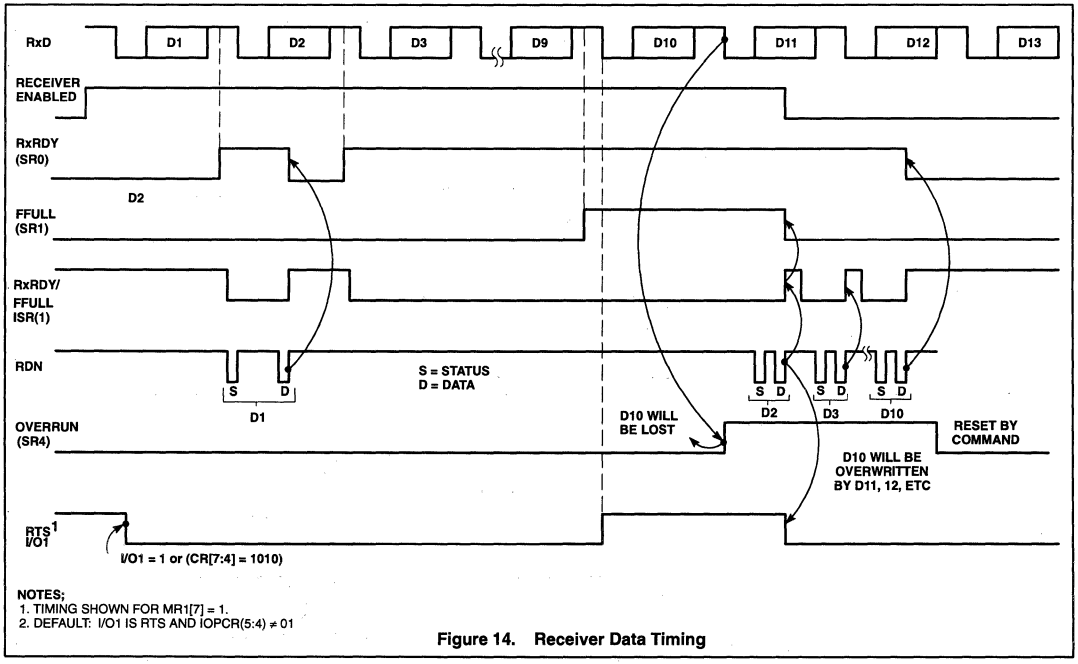


Figure 14. Receiver Data Timing

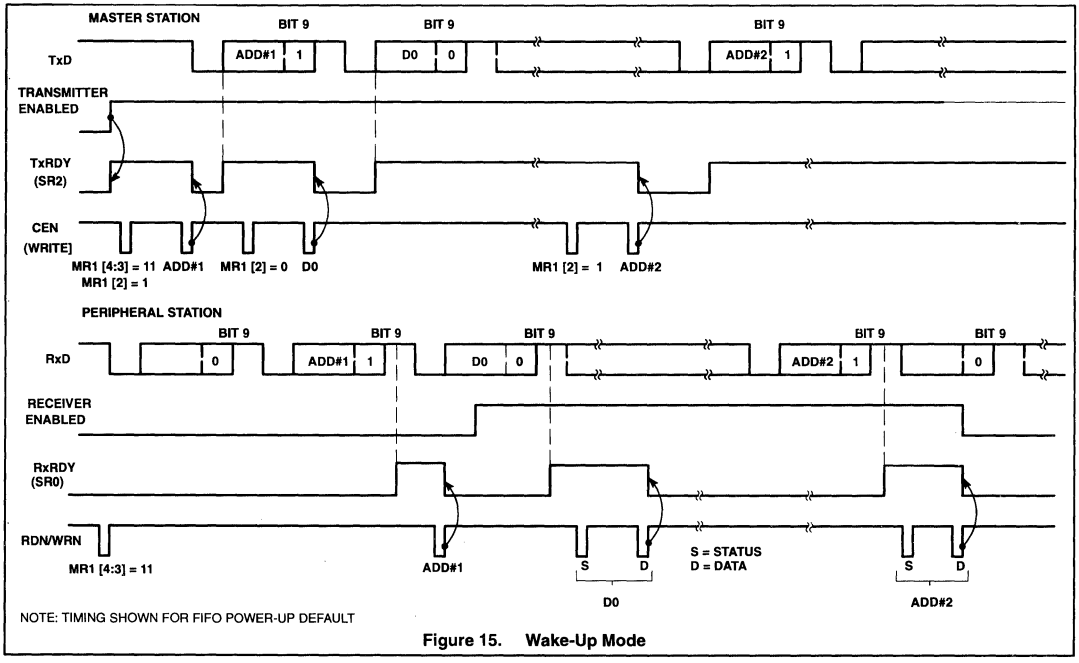


Figure 15. Wake-Up Mode

INTERRUPT NOTES

The following is a brief description of the new QUART "Bidding" interrupt system, interrupt vector and the use of the Global registers.

The new features of the QUARTs have been developed to greatly reduce the microprocessor time required to service uart interrupts. Bus cycle times have also been enhanced. By use of the new Current Interrupt Register (CIR) the speed of a polled system is also improved. For example programming the SCC2692 to interrupt on TxRDY and RxFUL would generate four interrupts for every six characters processed along with at least two additional accesses to the chip for each interrupt. This amounts to two non–data chip accesses per character. In the 26C94 this has been reduced to 0.25 non data accesses per character; an eight fold improvement. In certain conditions use of the global registers will yield a greater improvement.

The QUART has 18 possible sources which can be programmed to generate an interrupt:

- 4 Receiver channels
- 4 Transmitter Channels
- 4 Received "Break" conditions
- 4 Change of State Detectors (a total of 8 ports)
- 2 Counter/Timers

These sources are encoded in such a way that they generate a unique value. This value is defined by chip hardwire programming, user programming, and the source's present condition. The values the sources generate are compared (at the X1 clock rate) to a user defined Interrupt Threshold value contained in the ICR (Interrupt Control Register). When the source's value exceeds the threshold the interrupt is generated. It is the source's value which is captured in the CIR.

The heart of the interrupt speed enhancement is attained by allowing the interrupting source to encode its channel, interrupt type and, if appropriate, the number of FIFO bytes requiring service. This information is coded and transferred the CIR (Current Interrupt Register) at the time IACKN is asserted or the command 'Update CIR' is executed. Upon an interrupt the processor may read this register and in one access determine the "who, what and how much". This CIR value is used to drive the interrupt vector modification (when used) and the new "Global" registers.

"Global" Registers

The "Global Registers" are effectively pointers which use the contents of the CIR to direct a read or write operation to Rx or Tx or other source which is currently interrupting. There are four global registers defined in the register map:

1. Global Interrupting Byte Count
2. Global Interrupting Channel
3. Global Receive FIFO Register
4. Global Transmit FIFO Register

The global receive and transmit registers operate as an indirect address. The data read from the global receive register will be that of the currently interrupting receiver; the data written to the global transmit register will go to the currently interrupting transmitter. The interesting point here is that under certain circumstances an interrupt can be serviced without an interrogation of the chip.

For completeness it should be noted that the global registers are not physical devices. Reads of the Global Byte and Channel registers give the Byte count or Channel number, respectively, (right justified) of the interrupting channel. The CIR data is mapped to these "registers".

Table 7. Bidding Format

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION
Rx Byte count			Error 1	1	1	Channel No.		Receiver bid With error
Rx Byte count			no Error 0	1	1	Channel No.		Receiver bid No error
0	Tx Byte Count			1	0	Channel No.		Transmit bid
Programmable			1	0	0	Channel No.		Receive Break
Programmable			0	0	1	Channel No.		Change of State
Programmable		0	1	0	1	Channel No.		Counter/Timer

NOTES:
1. The ones and zeros above represent the hardwired positions.
2. Note the format of bits 4:2. They represent the identity of the interrupting source.
3. Bids with the highest number of contiguous MSBs win the bid.

1 1 1	Receiver with error
0 1 1	Receiver without error
x 1 0	Transmitter
1 0 0	Receiver Break detect
0 0 1	Change of State
1 0 1	Counter/Timer
0 0 0	No interrupt

In these identifiers the receivers are biased to have highest priority. The identifier bits and the channel number bits are hardwired on the chip. Normally the non–data interrupts would be programmed to a low value. The programmable fields can, in some cases, make these sources higher than a full receiver.

It would seem that a 11 programmed in the upper counter/timer bits, for example, would cause it to interrupt nearly all the time. This is not true . A counter/timer that has not timed out will not bid. In a similar fashion a receiver FIFO that is empty or a transmitter FIFO that is full will not bid

In general terms the threshold value programmed in the ICR (Interrupt Control Register) will reflect some fill level of the eight character transmit and receive FIFOs that allow processor service without underrun or overrun occurring.

Note that interrupt threshold value in the ICR is 6 bits long. This value is aligned with the bid arbitration logic such that it bids only through the most significant 6 bits. The result of this is that the channel value does not 'bid'. However the logic is such that other parts of the bid being equal the condition of the highest channel will be captured in CIR. The increasing order of the channels is A, B, C, D. Thus channel D is the "strongest" of the four.

It could be that the giving the highest strength to channel D may, from time to time, not be what would be most desired. Further it may be desired to alter the authority of a channel's bid. This may be done by setting the Rx and/or Tx interrupt bits in MR0 and MR1 to values different than zero. This will have the effect of not allowing the associated receiver or transmitter to bid until its FIFO reaches a particular fill level. Although this compromises the idea of the bidding interrupt scheme, it is entirely safe to use. In fact it is setting of MR0 and MR1 interrupt bits to zero that causes the receiver to stop bidding when it is empty and causes the transmitter to stop bidding when it is full. Altering the MR0 and MR1 interrupt bits only changes the level at which the Rx & Tx bidding is stopped.

See the "Interrupt Note on 26C94" which refers to the use of the MR registers in controlling the Rx and Tx bidding.

In normal operation the character of an interrupt will be controlled by the above registers in conjunction with the IMR (Interrupt Mask Register (one for each DUART)) . The function of the IMR will be to enable bidding of any particular source. Recall that the QUART has 18 functions which may generate an interrupt.

The format of the interrupt vector is controlled by the ICR[1:0] bits. The formats are shown in Table 7. The purpose of the vector modification is to allow the interrupting source (either channel or type and channel) to direct the processor to appropriate service routine. We have found that some users wish to use extremely tight loops for the service routines and find the addition of several tests of status bytes to be very 'expensive' in processor time.

NOTE ON QUART INTERFACE TO ITS CONTROLLING PROCESSOR

The QUART, has been designed to interface in either the synchronous interrupt environment (without DACKN) or the asynchronous interrupt environment (with DACKN). The 80xxx devices of Intel design are usually operated in a synchronous interrupt mode while those of Motorola design, 68xxx devices, operate in an asynchronous interrupt mode.

Note: Synchronous and asynchronous interrupt modes are not in any way associated with synchronous or asynchronous data transmission.

The QUART has been designed with the pins required to service either interface. In general then it is probable that in any application some of the interface pins will not be used. This note discusses what is required for the "text book" connections of the two methods. It should be noted that features of either method are not mutually exclusive.

The interface pins are all active low. (at V_{SS} or ground) The pins used for normal reading and writing to the QUART (the generation of a bus cycle) are CEN (Chip Enable), RDN (Read Enable), WRN (Write Enable). The pins used in the interrupt service are IRQN (Interrupt Request), IACKN (Interrupt Acknowledge). The pin used for data transfer is DACKN (Data Acknowledge). IRQN and DACKN are open drain outputs.

DACKN signaling can be enabled or disabled via writing to address 27h or 26h respectively. Note that if DACKN is enabled that writing to the QUART will occur on the falling edge of DACKN. The use of hardware reset (required at power up) enables DACKN.

Table 8. Configuration of Interrupt Vector for the QUART

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Interrupt vector for → ICR[1:0]=00	INTERRUPT VECTOR FORMATS (Controlled by ICR[1:0])							
	IVR[7:0]							
	Full interrupt vector							
Interrupt vector for → ICR[1:0]=01								
	IVR[7:2]						ICR[1:0]	
	Interrupt vector 6 MSBs						Channel number	
Interrupt vector for → ICR[1:0]=10								
	IVR[7:5]			ICR[4:2]			ICR[1:0]	
	Interrupt vector 3 MSBs			Interrupt type			Channel number	
Interrupt vector for → ICR[1:0]=11 (Inhibit)								
	Inhibit vector output. (Set bus to FFh)							
	CURRENT INTERRUPT REGISTER FORMAT CIR[7:0]							
	Rx or Tx byte count			Interrupt type: R/Tx CT COS BRK			Channel number	
	INTERRUPT CONTROL REGISTER FORMAT ICR[0:7]							
	Interrupt threshold ICR[7:2]						Interrupt vector format ICR[1:0]	

The Asynchronous Interface

Those familiar with 68xxx I/O will note the use of the two pins RDN and WRN to be in conflict with 68xxx devices use of the one R/WN pin. The R/WN must be inverted such that the R/WN may drive the WRN input while the inversion of R/WN drives the RDN input. It is good practice to condition the inversion of R/WN such that RDN will not become active on the termination of a write to the QUART while CEN is still asserted. These short periods of read could upset FIFO pointers in the chip.

During a read of the QUART DACKN signals that valid data is on the data bus. During a write to the QUART DACKN signals that data placed on the bus by the control processor has been written to the addressed register. The generation of DACKN begins with the start of a bus cycle (Read, Write or Interrupt Acknowledge) and then requires two edges of the X1 clock plus typically 70ns for its assertion.

In this mode the writing of data to the QUART registers occurs on the falling edge of DACKN or the rising edge of the combination of CEN and WRN which ever occurs first. This requires that the data to be written to the QUART registers be valid with respect to the leading edge of the combination of CEN and WRN. (In the synchronous mode it is the trailing edge)

IACKN updates the CIR (Current Interrupt Register) and places the Interrupt Vector or Modified Interrupt Vector on the bus if the Interrupt Vector is used.

The Synchronous Interface

In this mode the DACKN and IACKN are usually not used. Here data is written to the QUART on the trailing edge of the combination of CEN and WRN. The placing of data on the bus during a read cycle begins with the leading edge of the combination of CEN and RDN.

The read cycle will terminate with the rise of CEN or RDN which ever one occurs first. In this mode bus cycles are usually setup to be the minimum time required by the QUART and hence will be faster than bus cycles that are defined by the DACKN signal. DACKN should be turned off in this mode.

When IACKN is not used or is not available the command at 2Ah should be used to update the CIR (Current Interrupt Register). This register is normally updated by IACKN in response to the IRQN. Note that the CIR is not updated by IRQN since there could be a long time between the assertion of IRQN and the start of the interrupt service routine. During this time it is quite possible that another interrupt with a higher priority occurs. It is the CIR that contains the information that describes the interrupt source and its priority. It is therefor recommended that the first operation upon entering the interrupt service routine is the updating of the CIR. (Recall that the contents of the GLOBAL registers reflect the content of the CIR)

Summary

In the asynchronous mode all of the interface pins are usually used. The synchronous mode usually will not use the IACKN and DACKN. However there is no conflict in the quart if both modes are used in the same application. (i.e. More than one device may control the QUART) The principles to keep in mind are:

1. When IACKN is not used the CIR should be updated via command.
2. If DACKN is not used it should be disabled.
3. When in the asynchronous mode be sure DACKN is enabled.
4. With 68xxx type controllers the RDN signal must be generated.

Quad universal asynchronous receiver/transmitter (QUART) SC68C94

DESCRIPTION

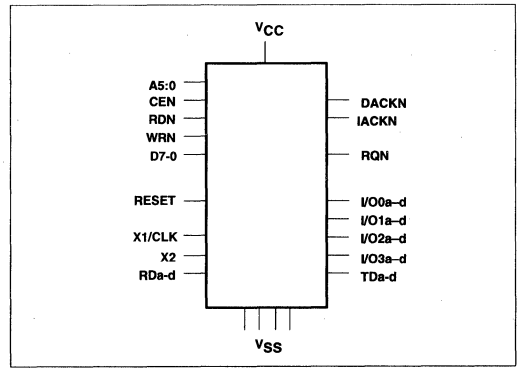
The 68C94 quad universal asynchronous receiver/transmitter (QUART) combines four enhanced Philips Semiconductors industry-standard UARTs with an innovative interrupt scheme that can vastly minimize host processor overhead. It is implemented using Philips Semiconductors' high-speed CMOS process that combines small die size and cost with low power consumption.

The operating speed of each receiver and transmitter can be selected independently at one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the QUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is buffered with eight character FIFOs (first-in-first-out memories) and one shift register to minimize the potential for receiver overrun and to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full. (RTS control)

The 68C94 provides a power-down mode in which the oscillator is stopped and the register contents are stored. This results in reduced power consumption on the order of several magnitudes. The QUART is fully TTL compatible and operates from a single +5V power supply.

PIN CONFIGURATIONS



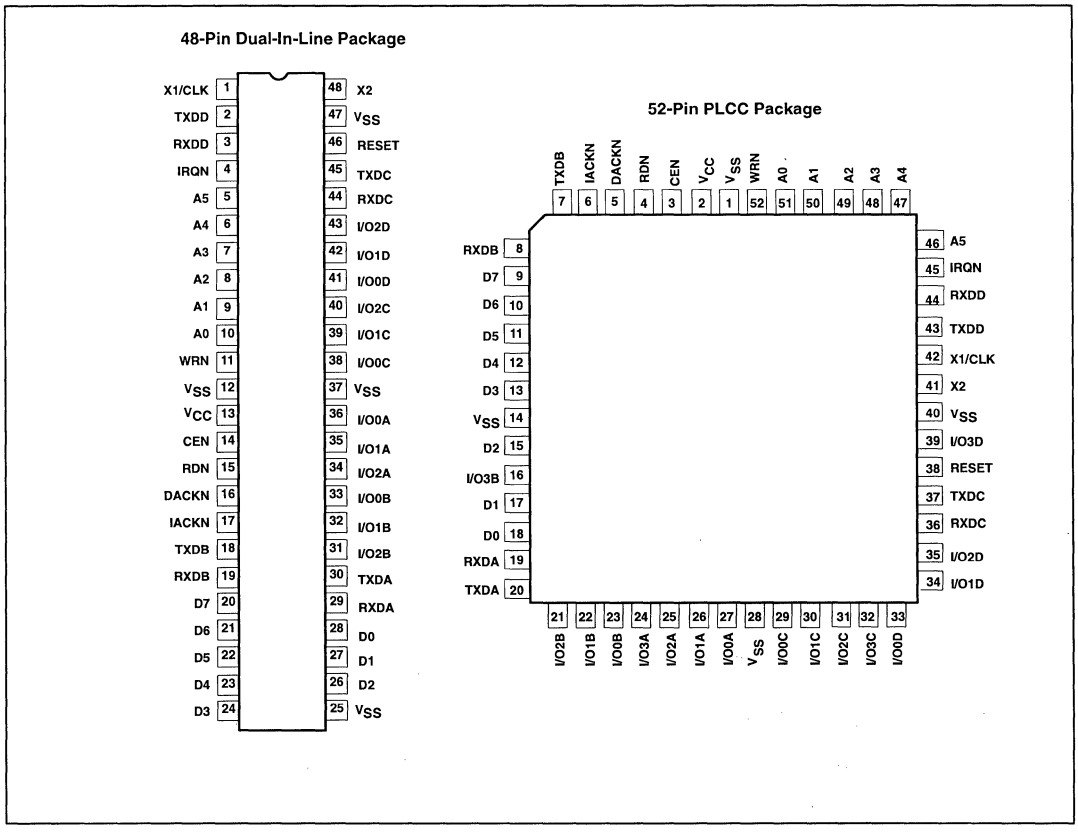
FEATURES

- New low overhead interrupt control
- Four Philips Semiconductors industry-standard UARTs
- Eight byte receive FIFO and eight byte transmit FIFO for each UART
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Baud rate for the receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4K baud Non-standard rates to 1.0M baud
  - User-defined rates from the programmable counter/timer associated with each of two blocks
  - External 1x or 16x clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex), automatic echo, local loop back, remote loopback
- Programmable interrupt priorities
- Identification of highest priority interrupt
- Global interrupt register set provides data from interrupting channel
- Vectored interrupts with programmable vector format
- IACKN and DTACKN signals
- Built-in baud rate generator with choice of 18 rates
- Four I/O pins per UART for modem controls, clocks, etc.
- Power down mode
- High-speed CMOS technology
- 52-pin PLCC and 48-pin DIP
- Commercial and industrial temperature ranges available
- On-chip crystal oscillator
- TTL compatible
- Single +5V power supply with low power mode
- Two multifunction programmable 16-bit counter/timers
- 1MHz 16x mode operation
- 30ns data bus release time
- "Watch Dog" timer for each receiver

ORDERING INFORMATION

PACKAGES	V_{CC} = +5V ±10%, T_A = 0°C to +70°C	V_{CC} = +5V ±10%, T_A = –40°C to +85°C	DWG #
48-Pin Plastic Dual In-Line Package (DIP)	SC68C94C1N	SC68C94A1N	0416C
52-Pin Plastic Leaded Chip Carrier (PLCC)	SC68C94C1A	SC68C94A1A	0397E

PIN CONFIGURATIONS



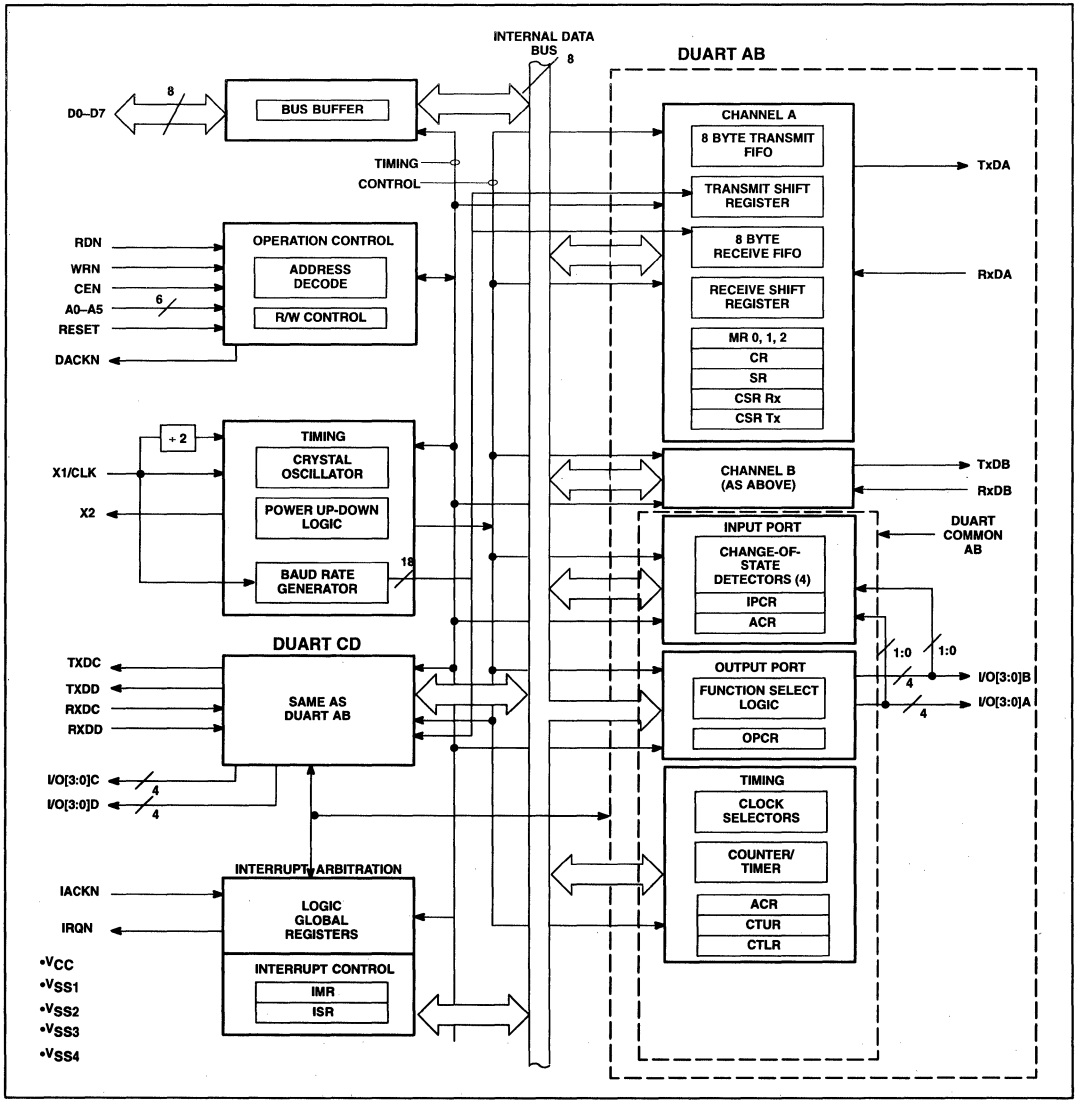
ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[3]	Note 4	°C
T_{STG}	Storage temperature range	–65 to +150	°C
V_{CC}	Voltage from V_{DD} to GND[4]	–0.5 to +7.0	V
V_S	Voltage from any pin to ground[4]	–0.5 to V_{CC} +0.5	V
P_D	Power dissipation	1	W

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range. See ordering information table for applicable temperature range and operating supply range.

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	TYPE	NAME AND FUNCTION
CEN	I	**Chip Select:** Active low input that, in conjunction with RDN or WRN, indicates that the host MPU is trying to access a QUART register. CEN must be inactive when IACKN is asserted.
A5:0	I	**Address Lines:** These inputs select a 68C94 register to be read or written by the host MPU.
D7:0	I/O	**8-bit Bidirectional Data Bus:** Used by the host MPU to read and write 68C94 registers.
RDN	I	**Read Strobe:** Active low input. When this line is asserted simultaneously with CEN, the 68C94 places the contents of the register selected by A5:0 on the D7:0 lines.
WRN	I	**Write Strobe:** Active low input. When this line is asserted simultaneously with CEN, the 68C94 writes the data on D7:0 into the register selected by A5:0.
DACKN	O	**Data ACKnowledge:** Active low, open-drain output to the host MPU, which is asserted subsequent to a read or write operation. For a read operation, assertion of DACKN indicates that register data is valid on D7:0. For a write operation, it indicates that the data on D7:0 has been captured into the indicated register. This signal corresponds to READYN on 80x86 processors and DTACKN on 680x0 processors.
IRQN	O	**Interrupt Request:** This active low open-drain output to the host MPU indicating that one or more of the enabled UART interrupt sources has reached an interrupt value which exceeds that pre-programmed by host software. The IRQN can be used directly as a 680x0 processor input; it must be inverted for use as an 80x86 interrupt input. This signal requires an external pull-up resistor.
IACKN	I	**Interrupt ACKnowledge:** Active low input indicating that the host MPU is acknowledging an interrupt requested by this device. The 68C94 responds to the assertion of this signal by placing an interrupt vector on D7-D0 and asserting DACKN. This signal updates the CIR register in the interrupt logic.
TDa-d	O	**Transmit Data:** Serial outputs from the four UARTs.
RDa-d	I	**Receive Data:** Serial inputs to the four UARTs/
I/O0a-d	I/O	**Input/Output 0:** A multi-use input or output signal for each UART. These pins can be used as general purpose inputs, Clear to Send inputs, 1X or 16X Transmit Clock outputs or general purpose outputs. Change-of-state detection is provided for these pins.
I/O1a-d	I/O	**Input/Output 1:** A multi-use input or output signal for each UART. These pins can be used as general purpose or 1X or 16X transmit clock inputs, or general purpose 1X or 16X receive clock outputs. Change-of-state detection is provided for these pins. In addition, I/O1a and I/O1c can be used as Counter/Timer inputs and I/O1b and I/O1d can be used as Counter/Timer outputs.
I/O2a-d	I/O	**Input/Output 2:** A multi-use input or output signal for each UART. These pins can be used as general purpose inputs, 1X or 16X receive clock inputs, general purpose outputs, RTS output or 1X or 16X receive clock outputs.
I/O3a-d	I/O	**Input/Output 3:** A multi-use input or output signal for each UART. These pins can be used as general purpose inputs, 1X or 16X transmit clock inputs, general purpose outputs, or 1X or 16X transmit clock outputs.
RESET	I	**Master Reset:** Active high reset for the 68C94 logic. Must be asserted at power-up, may be asserted at other times that the system is to be reset and restarted. OSC set to divide by 1, MR pointer set to 1, DACKN enabled, I/O pins to input. Registers reset: OPR, CIR. IRQN, DTACKN, IVR Interrupt Vector, Power Down, Test registers, FIFO pointers, Baud rate generator, Error Status, Watch Dog Timers, Change of State detectors, counter/timer to timer, Transmitter and Receiver controllers and all interrupt bits.
X1/CLK	I	**Crystal 1 or Communication Clock:** This pin is normally connected to one side of a 3.6864MHz or a 7.3728MHz crystal, or can be connected to an external clock up to 8MHz.
X2	O	**Crystal 2:** If a crystal is used, this pin should be connected to its other terminal. If an external clock is applied to X1, this pin should be left unconnected.
V_{CC}, V_{SS1}, V_{SS2}, V_{SS3}, V_{SS4}		**Power and grounds:** respectively.

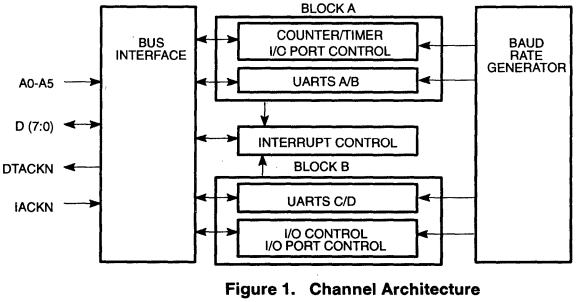


Figure 1. Channel Architecture

Table 1. QUART Registers[1]

A5:0	READ (RDN = Low)	WRITE (WRN = Low)
000000	Mode Register a (MR0a, MR1a, MR2a)	Mode Register a (MR0a, MR1a, MR2a)
000001	Status Register a (SRa)	Clock Select Register a (CSRa)
000010	Reserved	Command Register a (CRa)
000011	Receive Holding Register a (RxFIFOa)	Transmit Holding Register a (TxFIFOa)
000100	Input Port Change Reg ab (IPCRab)	Auxiliary Control Reg ab (ACRab)
000101	Interrupt Status Reg ab (ISRab)	Interrupt Mask Reg ab (IMRab)
000110	Counter/Timer Upper ab (CTUab)	Counter/Timer Upper Reg ab (CTURab)
000111	Counter/Timer Lower ab (CTLab)	Counter/Timer Lower Reg ab (CTLRab)
001000	Mode Register b (MR0b, MR1b, MR2b)	Mode Register b (MR0b, MR1b, MR2b)
001001	Status Register b (SRb)	Clock Select Register b (CSRb)
001010	Reserved	Command Register b (CRb)
001011	Receive Holding Register b (RxFIFOb)	Transmit Holding Register b (TxFIFOb)
001100	Output Port Register ab (OPRab)	Output Port Register ab (OPRab)
001101	Input Port Register ab (IPRab)	I/OPCRa (I/O Port Control Reg a)
001110	Start Counter ab	I/OPCRb (I/O Port Control Reg b)
001111	Stop Counter ab	Reserved
010000	Mode Register c (MR0c, MR1c, MR2c)	Mode Register c (MR0c, MR1c, MR2c)
010001	Status Register c (SRc)	Clock Select Register c (CSRc)
010010	Reserved	Command Register c (CRc)
010011	Receive Holding Register c (RxFIFOc)	Transmit Holding Register c (TxFIFOc)
010100	Input Port Change Reg cd (IPCRcd)	Auxiliary Control Reg cd (ACRcd)
010101	Interrupt Status Reg cd (ISRcd)	Interrupt Mask Reg cd (IMRcd)
010110	Counter/Timer Upper cd (CTUcd)	Counter/Timer Upper Reg cd (CTURcd)
010111	Counter/Timer Lower cd (CTLcd)	Counter/Timer Lower Reg cd (CTLRcd)
011000	Mode Register d (MR0d, MR1d, MR2d)	Mode Register d (MR0d, MR1d, MR2d)
011001	Status Register d (SRd)	Clock Select Register d (CSRd)
011010	Reserved	Command Register d (CRd)
011011	Receive Holding Register d (RxFIFOd)	Transmit Holding Register d (TxFIFOd)
011100	Output Port Register cd (OPRcd)	Output Port Register cd (OPRcd)
011101	Input Port Register cd (IPRcd)	I/OPCRc (I/O Port Control Reg c)
011110	Start Counter cd	I/OPCRd (I/O Port Control Reg d)
011111	Stop Counter cd	Reserved
100000	Bidding Control Register a (BCRa)	Bidding Control Register a (BCRa)
100001	Bidding Control Register b (BCRb)	Bidding Control Register b (BCRb)
100010	Bidding Control Register c (BCRc)	Bidding Control Register c (BCRc)
100011	Bidding Control Register d (BCRd)	Bidding Control Register d (BCRd)
100100	Reserved	Power Down
100101	Reserved	Power Up
100110	Reserved	Disable DACKN
100111	Reserved	Enable DACKN
101000	Current Interrupt Register (CIR)	Reserved
101001	Global Interrupting Channel Reg (GICR)	Interrupt Vector Register (IVR)
101010	Global Int Byte Count Reg (GIBCR)	Update CIR
101011	Global Receive Holding Reg (GRxFIFO)	Global Transmit Holding Reg (GTxFIFO)
101100	Interrupt Control Register (ICR)	Interrupt Control Register (ICR)
101101	Reserved	BRG Rate. 00 = low; 01 = high
101110	Reserved	Set X1/CLK divide by two[2]
101111	Reserved	Set X1/CLK Normal[2]
110000–111000	Reserved	Reserved
111001	Test Mode	Test Mode
111010–111111	Reserved	Reserved

NOTES:
1. Registers not explicitly reset by hardware reset power up randomly.
2. In X1/CLK divide by 2 all circuits receive the divided clock except the BRG and change-of-state detectors.

FUNCTIONAL BLOCKS

The QUART is composed of four Philips Semiconductors industry–standard UARTs, each having a separate transmit and receive channel.

The Basic UART cells in the QUART are configured with 8-byte Receive FIFOs and 8-byte Transmit FIFOs. Hardware supports interrupt priority arbitration based on the number of bytes available in the transmit and receive FIFOs, counter/timers, change of state detectors, break detect or receiver error. Attempts to push a full FIFO or pop an empty FIFO do not affect the count.

Baud Rate Generator

The baud rate generator used in the QUART is the same as that used in other Philips Semiconductors industry standard UARTs. It provides 18 basic Baud rates from 50 baud to 38,400 baud. It has been enhanced to provide to provide other baud rates up to 230,400 baud based on a 3.6364MHz clock; with an 8.0MHz clock rates to 500K baud. Other rates are available by setting the BRG rate to high at address 2D hex or setting Test 1 on at address 39 hex. See Table 3. These two modes are controlled by writing 00 or 01 to the addresses above. They are both set to 00 on reset. External Rx and Tx clocks yield rates to 1MHz in the 16X mode.

BLOCK DIAGRAM

As shown in the block diagram, the QUART consists of: data bus buffer, interrupt control, operation control, timing, and four receiver and transmitter channels. The four channels are divided into two different blocks, each block independent of the other.

Channel Blocks

There are two blocks (Block Diagram), each containing two sets of receiver/transmitters. In the following discussion, the description applies to Block A which contains channels a and b. However, the same information applies to all channel blocks.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the QUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The functions performed by the CPU read and write operations are shown in Table 1.

Mode registers (MR) 0, 1 and 2 are accessed via an address counter. This counter is set to one (1) by reset or a command 1x to the Command Register for compatibility with other Philips Semiconductors software. It is set to 0 via a command Bx to the Command Register (CR). The address counter is incremented with each access to the MR until it reaches 2 at which time it remains at 2. All subsequent accesses to the MR will be to MR2 until the MR counter is changed by a reset or an MR counter command.

The Mode Registers control the basic configuration of the UART channels. There is one for each UART. (Transmitter/receiver pair)

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, power up/down logic and a divide by 2 selector. Closely associated with the timing block are two 16-bit counter/timers; one for each DUART.

Oscillator

The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/ CLK and X2 inputs with a minimum of external components. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. If an external clock is used instead of a crystal, X1 must be driven and X2 left floating as shown in Figure 10. The clock serves as the basic timing reference for the baud rate generator (BRG), the counter/timer, and other internal circuits. A clock frequency, within the limits specified in the electrical specifications, must be supplied even if the internal BRG is not used.

The X1 pin always supplies the clock for the baud rate generator. The X1 pin also has a feature such that it may be divided by 2. The divide by two mode must always be used whenever the X1 pin is above 4MHz. The baud rate generator supplies the standard rates when X1 is at 3.6864MHz. In the divide by 2 mode, all circuits receive the divide by two clock except baud rate generator and I/O pin change-of-state detectors. 7.3738MHz clock doubles standard baud rates.

Baud Rate Generator

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. The eighteen BRG rates are grouped in two groups. Eight of the 18 are common to each group. The group selection is controlled by ACR[7]. See the Baud Rate Table 3. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The clock selectors allow the independent selection, by the receiver and transmitter, of any of these baud rates or an external timing signal.

Counter/Timer

The counter timer is a 16-bit programmable divider that operates in one of three modes: counter, timer, time out. In the timer mode it generates a square wave. In the counter mode it generates a time delay. In the time out mode it monitors the time between received characters. The C/T uses the numbers loaded into the Counter/Timer Lower Register (CTLR) and the Counter/Timer Upper Register (CTUR) as its divisor.

There are two counter/timers in the QUART; one for each block. The counter/timer clock source and mode of operation (counter or timer) is selected by the Auxiliary Control Register bits 6 to 4 (ACR[6:4]). The output of the counter/timer may be used for a baud rate and/or may be output to the I/O pins for some external function that may be totally unrelated to data transmission. The counter/timer also sets the counter/timer ready bit in the Interrupt Status Register (ISR) when its output transitions from 1 to 0.

A register read address (see Table 1) is reserved to issue a start counter/timer command and a second register read address is reserved to issue a stop command. The value of D(7:0) is ignored. The START command always loads the contents of CTUR, CTLR to the counting registers. The STOP command always resets the ISR(3) bit in the interrupt status register.

Timer Mode

In the timer mode a symmetrical square wave is generated whose half period is equal in time to division of the selected counter/timer clock frequency by the 16-bit number loaded in the CTLR CTUR. Thus, the frequency of the counter/timer output will be equal to the counter/timer clock frequency divided by twice the value of the CTUR CTLR. While in the timer mode the ISR bit 3 (ISR[3]) will be

set each time the counter/timer transitions from 1 to 0. (High to low) This continues regardless of issuance of the stop counter command. ISR[3] is reset by the stop counter command. NOTE: Reading of the CTU and CTL registers in the timer mode is not meaningful.

When the C/T is used to generate a baud rate *and* the C/T is selected through the CSR then the receivers and/or transmitter will be operating in the 16x mode. Calculation for the number 'n' to program the counter timer upper and lower registers is shown below.

$$n = \frac{\text{C/T Clock Frequency}}{2 * 16 * \text{Baud rate desired}}$$

Often this division will result in a non-integer number; 26.3 for example. One can only program integer numbers to a digital divider. Therefore 26 would be chosen. This gives a baud rate error of 0.3/26.3 which is 1.14%; well within the ability of the asynchronous mode of operation.

Counter Mode

In the counter mode the counter/timer counts the value of the CTLR CTUR down to zero and then sets the ISR[3] bit and sets the counter/timer output from 1 to 0. It then rolls over to 65,365 and continues counting with no further observable effect.

Reading the C/T in the counter mode outputs the present state of the C/T. If the C/T is not stopped, a read of the C/T may result in changing data on the data bus.

Timeout Mode

The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RxFIFO, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. If the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU will not be interrupted for the remaining characters in the RxFIFO.

By programming the C/T such that it would time out in just over one character time, the above situation could be avoided. The processor would be interrupted any time the data stream had stopped for more than one character time. NOTE: This is very similar to the watch dog time of MR0. The difference is in the programmability of the delay time and that the watchdog timer is restarted by either a receiver load to the RxFIFO or a system read from it.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. Only one receiver should use this mode at a time. However, if both are on, the timeout occurs after both receivers have been inactive for the timeout period. The start of the C/T will be on the logical or of the two receivers.

The timeout mode disables the regular START/STOP counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RxFIFO, the C/T is stopped after one C/T clock, reloaded with the value in CTUR and CTLR and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Since receiving a character restarts the C/T, the receipt of a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx='Ax', will also clear the counter ready bit and stop the counter until the next character is received.

The counter timer is controlled with six commands: Start/Stop C/T, Read/Write Counter/Timer lower register and Read/Write Counter/Timer upper register. These commands have slight differences depending on the mode of operation. Please see the detail of the commands under the CTLR CTUR Register descriptions.

Receiver and Transmitter

The QUART has four full-duplex asynchronous receiver/transmitters. The operating frequency for the receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input.

Registers associated with the communications channel are the mode registers (MR0, MR1 and MR2) Clock Select Register (CSR), Command Register (CR), Status Register (SR), Transmit FIFO (TxFIFO), and the Receive FIFO (RxFIFO). The transmit and receive FIFOs are each eight characters deep. The receive FIFO also stores three status bits with each character.

Transmitter

The transmitter accepts parallel data from the CPU and converts it to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the TxFIFO, the TxD output remains high and the TxEMT bit in the SR will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character in the TxFIFO. In the 16X clock mode, this also re-synchronizes the internal 1X transmitter clock so that transmission of the new character begins with minimum delay.

If the transmitter is disabled it continues operating until the character currently being transmitted and any characters in the TxFIFO, including parity and stop bits, have been transmitted. New data cannot be loaded to the TxFIFO when the transmitter is disabled.

The transmitter can be forced to send a break (a continuous low condition) by issuing a START BREAK command via the CR register. The break is terminated by a STOP BREAK command or a transmitter reset..

TxFIFO

The TxFIFO empty positions are encoded as a three bit number for presentation to the bidding logic. The coding will equal the number of bytes that remain to be filled. That is, a binary number of 101 will mean five bytes may be loaded; 111 means 7, etc. Eight positions will be indicated by a binary 111 *and* the FIFO empty bit will be set.

Receiver

The receiver accepts serial data on the RxD pin, converts the serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition, and presents the assembled character to the CPU via the receiver FIFO.

The receiver operates in two modes: the 1X and 16X. The 16X mode is the more robust of the two. It allows the receiver to establish a phase relation to the remote transmitter clock within 1/16 of a bit time and also allows validation of the start bit. The 1X mode does not validate the start bit and assumes that the receiver clock rising edge is centered in the data bit cell. The use of the 1X mode implies that the transmitter clock is available to the receiver.

When operating in the 16X mode and after the receiver has been enabled the receiver state machine will look for a high to low transition on the RxD input. The detection of this transition will cause the divider being driven by the 16X clock to be reset to zero and continue counting. When the counter reaches 7 the RxD input is sampled again and if still low a valid START BIT will be detected. If

the RxD input is high at count 7 then an invalid start bit will have been sensed and the receiver will then look for another high to low transition and begin validating again.

When a valid start bit is detected the receiver state machine allows the 16X divider circuit to continue counting 0 to 15. Each time the receiver passes count 7 (the theoretical center of the bit time) another data bit is clocked into the receiver shift register until the proper number of bits have been received including the parity bit, if used, and 1/2 stop bit. After the STOP BIT is detected the receiver state machine will wait until the next falling edge of the 1X clock and then clock the assembled character and its status bits into the receiver FIFO on the next rising edge of the 1X clock. The delay from the detection of the STOP BIT to the loading of the character to the RxFIFO will be from one half to one and one half X1 clock periods, or twice that if X1/2 is used. Receiver Status Register bits for FIFO READY, FIFO FULL, parity error, framing error, break detect will also set at this time. The most significant bits for data characters less than eight bits will be set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (i.e. framing error) and RxD remains low for one-half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled). The parity error, framing error and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set.

If a break condition is detected (RxD is low for the entire character including the stop bit), only one character consisting of all zeros will be loaded in the FIFO and the received break bit in the SR is set to 1. The "Change of Break" bit in the ISR at position 2 or 6 is also set at this time. Note that the "Change of Break" bit will set again when the break condition terminates. The RxD input must return to a high condition for two successive clock edges of the 1X clock (internal or external) before a search for the next start bit begins.

NOTE: If the RxD input is low when the receiver is enabled and remains low for at least 9/16 of a bit time a valid start bit will be seen and data (probably random) will be clocked into the receiver FIFO. If the line remains low for a full character time plus a stop bit then a break will be detected.

Each receiver is equipped with a watchdog timer. This timer is enabled by MR0[7] and counts 64 RxC1X clocks. Its purpose is to alert the controlling CPU that data is in the FIFO which has not been read. This situation may occur at the end of a message when the last group of characters was not long enough to cause an interrupt.

RECEIVER FIFO

The RxFIFO consists of a first-in-first-out (FIFO) with a capacity of eight characters. Data is loaded from the receive shift register into the top-most empty position of the FIFO. The RxRDY bit in the status register (SR) is set whenever one or more characters are available to be read; a FFULL status bit is set if all eight stack positions are filled with data. The number of filled positions is encoded into a 3-bit value. This value is sent to the interrupt bidding logic where it is used to generate an interrupt. A read of the RxFIFO, outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits are 'popped' thus emptying a FIFO position for new data.

NOTE: The number of filled positions in the RxFIFO is coded as actual number filled positions. Seven filled will be coded as 7. Eight filled positions will be coded as 7 *and* the RxFIFO full status bit will be set.

In addition to the data word, three status bits (parity error, framing error, and received break) are appended to each data character in the FIFO. Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical OR of the status for all characters coming to the top of the FIFO since the last reset error command was issued. In either mode, reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RxFIFO is read. Therefore, the SR should be read prior to reading the corresponding data character.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exists, the contents of the FIFO are not affected: the character previously in the shift register is lost and the overrun error status bit, SR[4], will be set upon receipt of the start bit of the new (overrunning) character.

A "watchdog" timer is associated with each receiver. Its interrupt is enabled by MR0[7]. The purpose of this timer is alerting the control processor that characters are in the RxFIFO which have not been read and/or the datastream has stopped. This situation may occur at the end of a transmission when the last few characters received are not sufficient to cause an interrupt.

This counter times out after 64 bit times. It is reset each time a character is transferred from the Receive shift register to the RxFIFO or a read of the RxFIFO is executed.

WAKE-UP MODE (MULTI-DROP OR 9-BIT)

In addition to the normal transmitter and receiver operation described above, the QUART incorporates a special mode which provides automatic "wakeup" of a receiver through address frame (or character) recognition for multi-processor or multi-station communications. This mode is selected by programming MR1[4:3] to '11'.

In this mode of operation a 'master' station transmits an address character to the several 'slave' stations on the line. The address character is identified by setting its parity bit to 1. The slave stations will usually have their receivers partially enabled as a result of setting MR1[4:3] to 11. When the receiver sees a one in the parity position, it considers it an address bit and loads that character to the RxFIFO and set the RxRDY bit in the status register. The user would usually set the receiver interrupt to occur on RxRDY as well. (All characters whose parity bits are set to 0 will be ignored). The local processor at the slave station will read the 'address' character just received. The local processor will test for an address match for this station and if match occurs it will enable the local receiver and receive the following data characters. The master will normally follow an address character(s) with data characters. Since the data characters transmitted by the master will have their parity bits set to zero, stations other than the addressed one(s) will ignore the data.

NOTE: The time between address and data fields must be enough for the local processor to test the address character and enable the receiver. At bit times approaching 10μs this may begin to be a point of concern.

The parity (Address/Data) bit should not be changed until the last stop bit of an address has been sent. Similarly the A/D bit should not be changed to address until the last stop bit has been sent. Either of these conditions will be indicated by an active TxEMT bit in the SR.

The parity bit is not part of the TxFIFO. It is in the transmitter state machine. However, it could be controlled in the FIFO if 5, 6 or 7 bit data was transmitted by using a 6, 7 or 8 bit character. The most significant bit would then be in the 'parity' position and represent the A/D bit. The design of the UART is based, however, on the A/D bit being controlled from the MR register.

Parity should be changed immediately before the data bytes will be loaded to the transmitter.

A transmitted character consists of a start bit, the programmed number of data and stop bits and an "address/data" bit. The parity bit is used as the address or data indicator. The polarity of the A/D bit is selected by setting MR1[2] to zero or one; zero indicates that the current byte is data, while one indicates that the current byte is addressed. The desired polarity of the A/D bit (parity) should be programmed before the TxFIFO is loaded.

The receiver should be enabled before the beginning of the first data bit. The time required is dependent on the interrupt latency of the slave receivers. The transmitter is able to start data immediately after the address byte has been sent.

While in this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character in the RxFIFO if the received A/D bit is a one, but discards the received character if the received A/D bit is a zero. If enabled, all received characters are then transferred to the CPU via the RxFIFO. In either case, the data bits are loaded in the data FIFO while the A/D bit is loaded in the status FIFO position normally used for parity error (SR[5]). Framing error, overrun error, and break detect operate normally whether or not the receiver is enabled.

INPUT OUTPUT (I/O) PINS

There are 16 multi-use pins; four for each UART. These pins are accessed and controlled via the Input Port Register (IPR), I/O Port Control Register (I/OPCR), Input Port Change Register (IPCR), and Output Port Register (OPR). They may be individually programmed to be inputs or outputs. See Table 5.

I/O0x and I/O1x pins have change of state detectors. The change of state detectors sample the input ports every 26.04μs (with the X1 clock at 3.686400MHz) and set the change bit in the IPCR if the pin has changed since it was last read. Whether the pins are programmed as inputs or outputs the change detectors still operate and report changes accordingly. See the register descriptions of the I/O ports for the detailed use of these features.

Interrupt Priority System

The interrupt control for the QUART has been designed to provide very low interrupt service overhead for the controlling processor while maintaining a high degree of flexibility in setting the importance of interrupts generated in different functional blocks of the device.

This is accomplished by allowing each function of the QUART (18 total) which may cause an interrupt to generate a variable numeric code which contains the identity of the source, channel number and severity level. This code is compared (at the X1 clock rate or the X1 clock rate divided by 2) to an interrupt threshold. When the interrupting source generates a code that is numerically greater than the interrupt threshold the IRQN is asserted

This is referred to as the bidding process. The winning bid contains, in different fields, all the characteristics of the winning bidder. This data may be used in several ways to steer the controlling processor to the proper type and amount of service required (usually the amount of service refers to the number of bytes written to the transmitter or read from the receiver). Access to the winning bidder is provided via the CIR (Current Interrupt Register), interrupt vectors, modified interrupt vectors and Global registers.

NOTE: IRQN is essentially a level output. It will go active on an interrupt condition and stays active until all interrupting sources are serviced.

IRQN is designed to be an open drain active low level output. It will go low under the control of the arbitration system and remain low until the arbitration has determined that no more sources require service.

When only one Rx or Tx is interrupting, it is possible to see the IRQN assert more than once if, during an access to the FIFO, the CEN input is inactive for more than two cycles of the X1 clock or X1 divide by 2 if that feature is enabled.

IACKN may be thought of as a special read input. Driving IACKN low will update the CIR and then read the Interrupt Vector Register or the Interrupt Vector Register modified by the CIR.

Functional Description of the Interrupt Arbitration

For the purpose of this description, a 'source' is any one of the 18 QUART circuits that may generate an interrupt. The QUART contains eighteen sources which may cause an interrupt:

1. Four receiver data FIFO filled functions.
2. Four receiver BREAK detect functions.
3. Four transmitter FIFO space available functions.
4. Four "Change of State" detectors.
5. Two counter/timers.

The interrupt logic at each source produces a numeric code that identifies its interrupt priority condition currently pending. This code is compared to a programmable Interrupt Threshold via the arbitration logic which determines if the IRQN should be asserted. The arbitration logic only judges those possible interrupt sources which have been allowed to bid via the IMR (Interrupt Mask Register).

The arbitration logic produces a value which is the concatenation of the channel number, interrupt type, FIFO fill level and user-defined fields. The channel number and interrupt type fields are hardwired. During the "bid arbitration" process all bids from enabled sources are presented, simultaneously, to an internal interrupt bus. The bidding system and formats are discussed in more detail in following sections.

The interrupt arbitration logic insures that the interrupt with the numerically largest bid value will be the only source driving the interrupt bus at the end of the arbitration period. The arbitration period follows the period of the X1 clock. The maximum speed is 4.0MHz. If a higher speed X1 clock is used then the X1 clock "divide by 2" feature must be used.

The value of the winning bid determined during the arbitration cycle is compared to the "Interrupt Threshold" contained in the ICR (Interrupt Control Register). If the winning bid exceeds the value of the ICR the IRQN is asserted.

Priority Arbitration and Bidding

Each of the five "types" of interrupts has slightly different "bid" value, as follows:

Receivers

# rcv'd	rEr	1	1	Chan #
3	1	1	1	2

Transmitters

0	# avail	1	0	Chan #
1	3	1	1	2

Break Detect

Programmable	1	0	0	Chan #
3	1	1	1	2

Change of State

Programmable	0	0	1	Chan #
3	1	1	1	2

Counter/Timer

Programmable	0	1	0	1	Chan #
2	1	1	1	1	2

Bits shown above as '0' or '1' are hard-wired inputs to the arbitration logic. Their presence allows determination of the interrupt type and they insure that no bid will have a value of all zeros (a condition that is indistinguishable from not bidding at all). They also serve to set a default priority among the non-receive/transmit types when the programmable fields are all zeros.

The channel number always occupies the two LSBs. Inclusion of the channel number insures that a bid value generated will be unique and that a single "winner" will drive the Interrupt Bus at the end of the arbitration interval. The channel number portion of each UARTs bid is hard-wired with UARTa being channel number 0 and so forth.

As can be seen above, bits 4:2 of the winning bid value can be used to identify the type of interrupt, including whether data was received correctly or not. Like the Channel number field, these bits are hard-wired for each interrupt source.

The "# rcv'd" and "# avail" fields indicate the number of bytes present in the receiver FIFO and the number of empty bytes in the transmitter FIFO, respectively.

NOTE: When there are zero bytes in the receiver's FIFO, it does NOT bid. Similarly, a full transmitter FIFO makes NO bid. In the case where all bids have been disabled by the Interrupt Mask Register or as a result of their byte counts, the active-low Interrupt Bus will return FFh. This value always indicates no interrupt source is active and IRQN will be negated.

The high order bit of the transmitter "bid" is always zero. An empty transmit FIFO is, therefore, fixed at a lower interrupt priority than a 1/2 full receive FIFO. Bit 4 of a receiver bid is the Receiver Error Bit (RER). The RER is the OR of the parity, framing and overrun error conditions. The RER does little to modify the priority of receiver interrupts vs. transmitter interrupts. It is output to the Interrupt Bus to allow inclusion of good data vs. problem data information in the Current Interrupt Register.

The high order bits of bids for received break, CoS (Change of State) and Counter/Timer events are all programmable. By programming ones in these fields, the associated interrupt source can be made more significant than most receiver and all transmitter interrupts. Values near zero in these fields makes them lower priority classes of interrupt.

The channel address for C/T ab will be encoded as channel B (01)

The channel address for C/T cd will be encoded as channel D (11)

As shown in Figure 4, the bid arbitration process is controlled by the EVAL/HOLDN signal derived from the oscillator clock.

Receipt of an IACKN signal from the host MPU latches the latest "winning bid" from the latched Interrupt Bus into the Current Interrupt Register (CIR). This logic is diagrammed in Figure 5.

If the IACKN falling edge of Figure 4 occurs during EVAL time, the result from the last arbitration (captured by the Interrupt Bus latches) is stored in CIR. Otherwise, the next EVAL pulse is inhibited and the value in the Interrupt Bus Latches is stored in CIR.

Clearing the Interrupt

Activities which change the state of the ISR will cause the IRQN to assert or negate. In addition, the accessing of a global or local RxFIFO or TxFIFO reduces the associated byte count for transmitter and receiver data interrupts. If the byte count falls below the threshold value, the interrupt request is withdrawn. Other interrupt conditions are cleared when the interrupting source is cleared.

Once the interrupt is cleared, the programmable value lowered or its byte count value reduced by one of the methods listed above, a different bidder (or no bidder at all) will win the on-going arbitration. When the winning bid drops below the Interrupt Threshold Register's value, the IRQN pin will negate.

Arbitration - Aftermath

At the end of the arbitration, i.e., the falling edge of EVAL, the winning interrupt source is driving its Channel number, number of bytes (if applicable) and interrupt type onto the Interrupt Bus. These values are captured into a latch by the trailing edge of EVAL. The output of this latch is used by the Interrupt Threshold comparator; the winning value is captured into another set of latches called the Current Interrupt Register (CIR) at the time of an Interrupt Acknowledge cycle or execution of the "Update CIR" command.

The Current Interrupt Register and associated read logic is shown in Figure 5. Interrupting channel number and the three bit interrupt type code and FIFO fill level are readable via the Internal Data Bus.

The contents of the appropriate receiver or transmitter byte "counter", as captured at the time of IACKN assertion, make up bits 7:5 of the CIR. If the interrupt type stored in the Current Interrupt Register is not a receiver or transmitter data transfer type, the CIR7:5 field will read as the programmable fields of their respective bid formats.

The buffers driving the CIR to the DBUS also provide the means of implementing the Global Interrupting Channel and Global Byte Count Registers, described in a later section.

The winning bid channel number and interrupt type fields can also be used to generate part of the Interrupt Vector, as defined by the Interrupt Control Register.

Interrupt Context

The channel number of the winning "bid" is used by the address decoders to provide data from the interrupting UART channel via a set of Global pseudo-registers. The interrupt Global pseudo-registers are:

1. Global Interrupting Byte Count
2. Global Interrupting Channel
3. Global Receive Holding Register
4. Global Transmit Holding Register

The first two Global "registers" are provided by Current Interrupt Register fields as shown in Figure 5. The interrupting channel number latched in CIR modifies address decoding so that the Receive or Transmit Holding Register for the interrupting channel is accessed during I/O involving the Global Receive and Transmit Holding Registers. Similarly, for data interrupts from the transmitter and receiver, the number of characters available for transfer to the CPU or the number of transmit FIFO positions open is available by reading the Global Interrupt Byte Count Register. For non-data interrupts, a read of the Global Interrupt Byte Count Register yields a value equal to the highest programmable filed.

In effect, once latched by an IACK or the Update CIR command, the winning interrupt channel number determines the contents of the global registers. All Global registers will provide data from the interrupting UART channel.

Interrupt Threshold Calculation

The state of IRQN is determined by comparison of the winning "bid" value to the Interrupt Threshold field of the Interrupt Control Register.

The logic of the bidding circuit is such that when no interrupt source has a value greater than the interrupt threshold then the interrupt is not asserted and the CIR (Current Interrupt Register) is set to all ones. When one or more of the 18 interrupt sources which are enabled via the IMR (Interrupt Mask Register) exceed the threshold then the interrupt threshold is effectively disconnected from the bidding operation while the 18 sources now bid against each other. The final result is that the highest bidding source will disable all others and its value will be loaded to the CIR and the IRQN pin asserted low. This all occurs during each cycle of the X1, X2 crystal clock.

RECEIVER INPUT FILL LEVEL

MR0[6]	MR1[6]	Interrupt Condition
0	0	1 or more bytes in FIFO (Rx RDY) default*
0	1	6 or more bytes in FIFO
1	0	4 or more bytes in FIFO
1	1	8 or more bytes in FIFO (Rx FULL)
MR0[5:4] – Tx Interrupt fill level		
MR0[5]	**MR0[4]**	**Interrupt Condition**
0	0	8 bytes empty (Tx EMPTY) default*
0	1	4 or more bytes empty
1	0	6 or more bytes empty
1	1	1 or more bytes empty (Tx RDY)

*These conditions, for interrupt purposes, make the RxFIFO look like a 3 byte FIFO; the TxFIFO a 1 byte FIFO. This is to allow software compatibility with previous Philips UART devices. Both FIFOs accept 8 bytes of data regardless of this bit setting. Only the interrupt is affected.

INTERRUPT NOTE ON 68C94:

For the receivers and transmitters, the bidding of any particular unit may be held off unless one of four FIFO fill levels is attained. This is done by setting the RxINT and TxINT bits in MR0 and MR1 to non-zero values. This may be used to prevent a receiver or transmitter from generating an interrupt even though it is filed above the bid threshold. Although this is not in agreement with the idea that each enabled interrupt source bid with equal authority, it does allow the flexibility of giving particular receiver or transmitters more interrupt importance than others.

This may be used when the Interrupt Threshold is set at or above 100000. Note than in this case the transmitter cannot generate an interrupt. If the interrupt threshold MSBs were set to 011 *and* the 'Receiver Interrupt Bits' on the MR registers set to a value other than 00 then the RxFIFO could not generate and interrupt until it had 4, 6 or 8 bytes. This in effect partially defeats the hardwired characteristic that the receiver interrupts should have more importance than the transmitter. This characteristic has been implemented by setting the MSB of the transmitter bid to zero.

Vectored Interrupts

The QUART responds to an Interrupt Acknowledge (IACK) initiated by the host by providing an Interrupt Acknowledge Vector on D7:0. The interrupt acknowledge cycle is terminated with a DACKN pulse. The vector provided by the QUART can have one of the three forms under control of the IVC control field (bits 1:0 of the Interrupt Control Register):

With IVC = 00 (IVR only)

IVR7:0
8

With IVC = 01 (channel number)

IVR7:2	Chan #
6	2

With IVC = 10 (type & channel number)

IVR7:5	Type	Chan #
3	3	2

A code of 11 in the Interrupt Vector Control Field of the ICR results in NO interrupt vector being generated. The external data bus is driven to a high impedance throughout the IACK cycle. A DACKN will be generated normally for the IACK cycle, however.

NOTE: If IACKN is not being used then the command "UPDATE CIR" must be issued for the global and interrupt registers to be updated.

PROGRAMMING UART CONTROL REGISTERS

The operation of the QUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. Addressing of the registers is described in Table 1.

The bit formats of the QUART registers are depicted in Table 2.

Table 2. Register Bit Formats, DUART AB. [duplicated for DUART CD]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

MR0 (Mode Register 0)

Rx Watchdog Timer	RxINT2 bit	TxINT Control	These bits not implemented. They should be considered Reserved.			
0 = off 1 = on	These bits should normally be set to 0		x	x	x	x

MR1 (Mode Register 1)

RxRTS Control	RxINT1 Select	Error Mode	Parity Mode	Parity Type	Bits per Character
0 = No 1 = Yes	Normally set to 0	0 = Char 1 = Block	00 = With parity 01 = Force parity 10 = No parity 11 = Wake-up mode	0 = Even 1 = Odd	00 = 5 01 = 6 10 = 7 11 = 8

MR2 (Mode Register 2)

Channel Mode	TxRTS Control	CTS Enable Tx	Stop Bit Length*
00 = Normal 01 = Auto-echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	0 = 0.563 4 = 0.813 8 = 1.563 C = 1.813 1 = 0.625 5 = 0.875 9 = 1.625 C = 1.875 2 = 0.688 6 = 0.938 A = 1.688 E = 1.938 3 = 0.750 7 = 1.000 B = 1.750 F = 2.000

NOTE:
Add 0.5 to values shown above for 0–7, if channel is programmed for 5 bits/char.

CSR (Clock Select Register)

Receiver Clock Select	Transmitter Clock Select
See text	See text

CR (Command Register)

Miscellaneous Commands	Disable Tx	Enable Tx	Disable Rx	Enable Rx
See text	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE: Issuing commands contained in the upper four bits of the "Command Register" should be separated in time by at least three (3) X1 clock edges. Allow four (4) edges if the "X1 clock divide by 2" mode is used. A disabled transmitter cannot be loaded.

SR (Status Register)

Rec'd. Break	Framing Error	Parity Error	Overrun Error	TxEMT	TxRDY	RxFULL	RxRDY
0 = No 1 = Yes *	0 = No 1 = Yes *	0 = No 1 = Yes *	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

NOTE: These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits [7:5] from the top of the FIFO together with bits [4:0]. These bits are cleared by a reset error status command. Unless reset with the 'Error Reset' (CR command 40) or receiver reset, these bits will remain active in the Status Register after the RxFIFO is empty.

ACR (Auxiliary Control Register)

BRG Set Select	Counter/Timer Mode and Source	Delta I/O1b	Delta I/O0b	Delta I/O1a	Delta I/O0a
0 = set 1 1 = set 2	See text	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

IPCR (Input Port Change Register)

Delta I/O1b	Delta I/O0b	Delta I/O1a	Delta I/O0a	I/O1b	I/O0b	I/O1a	I/O0a
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

Table 2. Register Bit Formats, Duart ab. [duplicated for Duart cd] (continued)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

ISR (Interrupt Status Register)

I/O Port Change	Delta BREAKb	RxRDY/ FFULLb	TxRDYb	Counter Ready	Delta BREAKa	RxRDY/ FFULLa	TxRDYa
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

IMR (Interrupt Mask Register)

I/O Port Change INT	Delta BREAKb INT	RxRDY/ FFULLb INT	TxRDYb INT	Counter Ready INT	Delta BREAKa INT	RxRDY/ FFULLa INT	TxRDYa INT
0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

CTUR (Counter/Timer Upper Register)

C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]

CTUR (Counter/Timer Lower Register)

C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]

IPR (Input Port Register)

I/O3b	I/O2b	I/O3a	I/O2a	I/O1b	I/O0b	I/O1a	I/O0a
0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

Mode Registers 0, 1 and 2

The addressing of the Mode Registers is controlled by the MR Register pointer. On any access to the Mode Registers this pointer is always incremented. Upon reaching a value of 2 it remains at 2 until changed by a CR command or a hardware reset.

MR0 – Mode Register 0

Mode Register 0 (MR0) is part of the UART configuration registers. It controls the watch dog timer and the encoding of the number of characters received in the RxFIFO. The lower four bits of this register are not implemented in the hardware of the chip. MR0 is normally set to either 80h or 00h. A read of this register will return 1111 (Fh) in the lower four bits.

The MR0 register is accessed by setting the MR Pointer to zero (0) via the command register command 1011 (Bh).

MR0[7]: This bit enables or disables the RxFIFO watch dog timer.

MR0[7] = 1 enable timer

MR0[7] = 0 disable timer

MR0[6:4]: These bits are normally set to 0 except as noted in the "Interrupt Threshold Calculation" description

MR0[3:0]: These bits are not implemented in the chip. These bits should be be considered "reserved."

MR1 – Mode Register 1

MR1 is accessed when the MR pointer points to MR1. The pointer is set to MR1 by RESET, a set pointer command applied via the CR or after an access to MR0. After reading or writing MR1, the pointers are set at MR2.

MR1[7] – Receiver Request-to-Send Flow Control

This bit controls the deactivation of the RTSN output (I/O2x) by the receiver. This output is manually asserted and negated by commands applied via the command register. MR1[7] = 1 causes RTSN to be automatically negated upon receipt of a valid start bit if the receiver FIFO is full. RTSN is re-asserted when an empty FIFO position is available. This feature can be used to prevent overrun in the receiver by using the RTSN output signal to control the CTS input (the QUART I/O0 pin) of the transmitting device.

Use of this feature requires the I/O2 pin to be programmed as output via the I/OPCR and to be driving a 0 via the OPR. When the RxFIFO is full and the start bit of the ninth character is sensed the receiver logic will drive the I/O2 pin high. This pin will return low when another RxFIFO position is vacant.

MR1[6] – Receiver Interrupt Select 1

This bit is normally set to 0 except as noted in the "Interrupt Threshold Calculation" description. MR1[6] operates with MR0[6] to prevent the receiver from bidding until a particular fill level is attained. For software compatibility this bit is designed to emulate the RxFIFO interrupt function of previous Philips Semiconductors UARTs.

MR1[5] – Error Mode Select

This bit selects the operating mode of the three FIFOed status bits (received break, FE, PE). In the character mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO.

In the block mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last reset error command was issued.

In the "Block Error" mode the ORing of the error status bits and the presentation of them to the status register takes place as the bytes enter the RxFIFO. This allows an indication of problem data when the error occurs after the leading bytes have been received. In the character mode the error bits are presented to the status register when the corresponding byte is at the top of the FIFO.

MR1[4:3] – Parity Mode Select
If "with parity" or "force parity" is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR1[4:3] = 11 selects the channel to operate in the special wake-up mode (see 'Wake-Up Mode').

MR1[2] – Parity Type Select
This bit selects the parity type (odd or even) if the "with parity" mode is programmed by MR1[4:3], and the polarity of the forced parity bit if the "force parity" mode is programmed. It has no effect if the "no parity" mode is programmed. In the special "wake-up" mode, it selects the polarity of the transmitted A/D bit.

MR1[1:0] – Bits per Character Select
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2 – Mode Register 2

MR2 is accessed when the channel MR pointer points to MR2, which occurs after any access to MR1. Accesses to MR2 do not change the pointer.

MR2[7:6] – Mode Select
The QUART can operate in one of four modes. MR2[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is re-clocked and retransmitted on the TxD output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.

Two diagnostic modes can also be selected. MR2[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxD output is held high.
4. The RxD input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2[7:6] = 11. In this mode:

1. Received data is re-clocked and retransmitted on the TxD output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., the transmitted parity bit is as received.
5. The receiver must be enabled, but the transmitter need not be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected, the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes; if the deselection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop bit has been retransmitted.

MR2[5] – Transmitter Request-to-Send Control

NOTE: When the transmitter controls the I/O2 pin (usually used for the RTSN signal) the meaning of the pin is not RTSN at all! Rather it signals that the transmitter has finished transmission. (i.e., end of block).

This bit controls the deactivation of the RTSN output (I/O2) by the transmitter. This output is manually asserted and negated by appropriate commands issued via the command register. MR2[5] = 1 causes RTSN to be reset automatically one bit time after the characters in the transmit shift register and in the TxFIFO (if any) are completely transmitted (includes the programmed number of stop bits if the transmitter is not enabled). This feature can be used to automatically terminate the transmission as follows:

1. Program auto-reset mode: MR2[5] = 1.
2. Enable transmitter.
3. Assert RTSN via command.
4. Send message.
5. Verify the next to last character of the message is being sent by waiting until transmitter ready is asserted. Disable transmitter after the last character of the message is loaded in the TxFIFO.
6. The last character will be transmitted and RTSN will be reset one bit time after the last stop bit.

MR2[4] – Transmitter Clear-to-Send Flow Control
The sate of this bit determines if the CTSN input (I/O0) controls the operation of the transmitter. If this bit is 0, CTSN has no effect on the transmitter. If this bit is a 1, the transmitter checks the sate of CTSN each time it is ready to send a character. If it is asserted (Low), the character is transmitted. If it is negated (High), the TxD output remains in the marking state and the transmission is delayed until CTSN goes Low. Changes in CTSN, while a character is being transmitted do not affect the transmission of that character. This feature can be used to prevent overrun of a remote receiver.

MR2[3:0] – Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1–9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1–1/16 to 2 stop bits can be programmed in increments of 1/16 bit. If an external 1X clock is used for the transmitter, MR2[3] = 0 selects one stop bit and MR2[3] = 1 selects two stop bits to be transmitted.

RECEIVER NOTE: In all cases, the receiver only checks for a "mark" condition at the center of the stop bit (1/2 to 9/16 bit time into the stop bit position). At this time the receiver has

finished processing the present character and is ready to search for the start bit of the next character.

Table 3. Bit Rate Generator Characteristics Crystal or Clock = 3.6864MHz

NORMAL RATE (BAUD)	ACTUAL 16X CLOCK (kHz)	ERROR (%)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2K	307.2	0
38.4K	614.4	0

NOTE: Duty cycle of 16X clock is 50% ± 1%.

CR – Command Register

CR is used to write commands to the QUART.

CR[7:4] – Miscellaneous Commands

Issuing commands contained in the upper four bits of the "Command Register" should be separated in time by at least three (3) X1 clock edges. Allow four (4) edges if the "X1 clock divide by 2" mode is used. The encoded value of this field can be used to specify a single command as follows:

0000 No command.

0001 Reset MR pointer. Causes the MR pointer to point to MR1.

0010 Reset receiver. Resets the receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO pointer is reset to the first location.

0011 Reset transmitter. Resets the transmitter as if a hardware reset had been applied.

0100 Reset error status. Clears the received break, parity error, framing error, and overrun error bits in the status register (SR[7:4]). Used in character mode to clear OE status (although RB, PE, and FE bits will also be cleared), and in block mode to clear all error status after a block of data has been received.

0101 Reset break change interrupt. Causes the break detect change bit in the interrupt status register (ISR[2 or 6]) to be cleared to zero.

0110 Start break. Forces the TxD output low (spacing). If the transmitter is empty, the start of the break condition will be delayed up to two bit times. If the transmitter is active, the break begins when transmission of the character is completed. If a character is in the TxFIFO, the start of break is delayed until that character or any others loaded after it have been transmitted (TxEMT must be true before break begins). The transmitter must be enabled to start a break

0111 Stop break. The TxD line will go high (marking) within two bit times. TxD will remain high for one bit time before the next character, if any, is transmitted.

1000 Assert RTSN. Causes the RTSN output to be asserted (Low).

1001 Negate RTSN. Causes the RTSN output to be negated (High).

1010 Set Timeout Mode On. The register in this channel will restart the C/T as each receive character is transferred from the shift register to the RxFIFO. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset.
Only one receiver should use this mode at a time. However, if both are on, the timeout occurs after both receivers have been inactive for the timeout. The start of the C/T will be on the logical 'OR' of the two receivers.

1011 Set MR Pointer to 0.

1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued.

1101 Reserved.

111x Reserved for testing.

CSR – Clock Select Register

CSR[7:4] – Receiver Clock Select

When using a 3.6864MHz crystal or external clock input, this field selects the baud rate clock for the receiver as shown in Table 3.

The receiver clock is always a 16X clock, except for CSR[7:4] = 1111. I/O2x is external input.

CSR[3:0] – Transmitter Clock Select

This field selects the baud rate clock for the transmitter. The field definition is as shown in Table 3, except as follows:

CSR[3:0]	ACR[7] = 0	ACR[7] = 1
1 1 1 0	I/O3x – 16X	I/O3x – 16X
1 1 1 1	I/O3x – 1X	I/O3x – 1X

Table 4. Baud Rate

	BRG RATE = LOW		BRG RATE = HIGH		TEST 1 = 1	
CSR[7:4]	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0 0 0 0	50	75	50	450	4,800	7,200
0 0 0 1	110	110	110	110	880	880
0 0 1 0	134.5	38.4k	134.5	230.4K	1,076	38.4K
0 0 1 1	200	150	200	900	19.2K	14.4K
0 1 0 0	300	300	1800	1,800	28.8K	28.8K
0 1 0 1	600	600	3,600	3,600	57.6K	57.6K
0 1 1 0	1,200	1,200	7,200	7,200	115.2K	115.2K
0 1 1 1	1,050	2,000	1,050	2,000	1,050	2,000
1 0 0 0	2,400	2,400	14.4K	14.4K	57.6K	57.6K
1 0 0 1	4,800	4,800	28.8K	28.8K	4,800	4,800
1 0 1 0	7,200	1,800	7,200	1,800	57.6K	14.4K
1 0 1 1	9,600	9,600	57.6K	57.6K	9,600	9,600
1 1 0 0	38.4k	19.2k	230.4K	115.2K	38.4K	19.2K
1 1 0 1	Timer	Timer	Timer	Timer	Timer	Timer
1 1 1 0	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X
1 1 1 1	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X

CR[3] – Disable Transmitter
This command terminates transmitter operation and resets the TxRDY and TxEMT status bits. However, if a character is being transmitted or if a character is in the TxFIFO when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

While the transmitter is disabled (or a disable is pending), the TxFIFO may not be loaded.

CR[2] – Enable Transmitter
Enables operation of the transmitter. The TxRDY and TxEMT status bits will be asserted.

CR[1] – Disable Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. However any unread characters in the RxFIFO area are still available. Disable is not the same as a "receiver reset". With a receiver reset any characters not read are lost. The command has no effect on the receiver status bits or any other control registers. If the special wake–up mode is programmed, the receiver operates even if it is disabled (see Wake-up Mode).

CR[0] – Enable Receiver
Enables operation of the receiver. If not in the special wake-up mode, this also forces the receiver into the search for start bit state.

SR – Channel Status Register

SR[7] – Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received; further entries to the FIFO are inhibited until the RxDA line returns to the marking state for at least one-half bit time (two successive edges of the internal or external 1x clock).

When this bit is set, the change in break bit in the ISR (ISR[6 or 2]) is set. ISR[6 or 2] is also set when the end of the break condition, as defined above, is detected. The break detect circuitry is capable of detecting breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must last until the end of the next character in order for it to be detected.

SR[6] – Framing Error (FE)
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SR[5]– Parity Error (PE)
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity. In 'wake-up mode', the parity error bit stores the received A/D (Address/Data) bit.

In the wake-up mode this bit follows the polarity of the A/D parity bit as it is received. A parity of 1 would normally mean address and therefore, the end of a data block.

SR[4] – Overrun Error (OE)
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a reset error status command.

SRA[3] – Channel A Transmitter Empty (TxEMTA)
This bit will be set when the transmitter underruns, i.e., both the TxEMT and TxRDY bits are set. This bit and TxRDY are set when the transmitter is first enabled and at any time it is re-enabled after either (a) reset, or (b) the transmitter has assumed the disabled state. It is always set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission.

It is reset when the THR is loaded by the CPU, a pending transmitter disable is executed, the transmitter is reset, or the transmitter is disabled while in the underrun condition.

SR[2] – Transmitter Ready (TxRDY)
This bit, when set, indicates that the TxFIFO has at least one empty location that may be loaded by the CPU. It sets when the transmitter is first enabled. It is cleared when the TxFIFO is full (eight bytes); the transmitter is reset; a pending transmitter disable is executed; the transmitter is disabled when it is in the underrun condition. When this bit is **not** set characters written to the TxFIFO will not be loaded or transmitted; they are lost.

SR[1] – RxFIFO Full (FFULL)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all eight FIFO positions are occupied. It is reset when the CPU reads the FIFO and there is no character in the receive shift register. If a character is waiting in the receive shift

register because the FIFO is full, FFULL is not reset after reading the FIFO once.

SR[0] – RxFIFO Ready (RxRDY)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RxFIFO, and no more characters are in the FIFO.

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects between two sets of baud rates that are available within each baud rate group generated by the BRG. See Table 3.

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.

Set 2: 75, 110, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, 19.2k, and 38.4k baud.

The selected set of rates is available for use by the receiver and transmitter.

ACR[6:4] – Counter/Timer Mode and Clock Source Select
This field selects the operating mode of the counter/timer and its clock source (see Table 4).

The I/O pins available for counter/timer clock source is I/O1a and I/O1c. The counter/timer clock selection is connected to the I/O1 pin and will accept the signal on this pin regardless of how it is programmed by the I/OPCR.

Table 5. ACR[6:4] C/T Clock and Mode Select

[6:4]	Mode	Clock Source
0 0 0	Counter	I/O1 pin
0 0 1	Counter	I/O1 pin divided by 16
0 1 0	Counter	TxC1XA clock of the transmitter
0 1 1	Counter	TxC1XB clock of the transmitter
1 0 0	Timer	I/O1 pin
1 0 1	Timer	I/O1 pin divided by 16
1 1 0	Timer	Crystal or external clock (X1/CLK)
1 1 1	Timer	Crystal or external clock (X1/CLK) divided by 16
The timer mode generates a squarewave		

ACR[3:0] – I/O1b, I/O0b, I/O1a, I/O0a Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register, ISR[7], to be set and thus allow the Change of State Detectors to enter the bidding process. If a bit is in the 'on' state, the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which may result in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – I/O1b, I/O0b, I/O1a, I/O0a Change-of-State Detectors
These bits are set when a change of state, as defined in the Input Port section of this data sheet, occurs at the respective pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – I/O1b, I/O0b, I/O1a, I/O0a State of I/O Pins
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins during the time the IPCR is read. The IPR is an unlatched register. Data can change during a read.

ISR – Interrupt Status Register

Important: The setting of these bits and those of the IMR are essential to the interrupt bidding process.

This register provides the status of all potential interrupt sources. The contents of this register are masked by the interrupt mask register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', then the interrupt source represented by this bit is allowed to enter the interrupt arbitration process. It will generate an interrupt (the assertion of INTRN low) only if its bid exceeds the interrupt threshold value. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR; the complete status is provided regardless of the contents of the IMR.

ISR[7] – I/O Change-of-State
This bit is set when a change-of-state occurs at the I/O1b, I/O0b, I/O1a, I/O0a input pins. It is reset when the CPU reads the IPCR.

ISR[6] – Channel b Change in Break
This bit, when set, indicates that the receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a reset break change interrupt command.

ISR[5] – Receiver Ready or FIFO Full Channel b
Normally the ISR[5] bit being set to one indicates the RxFIFO is filled with one or more bytes and/or the receiver watch dog timer (when enabled) has timed out.

The meaning of ISR[5] is controlled by the MR0[6] and MR1[6] bits which are normally set to 00. The ISR[5] bit setting to one allows the receiver to present its bid to the arbitration logic. This function is explained in the "Interrupt Note On 68C94" and under the "Receiver Interrupt Fill Level".

ISR[5], if set, will reset when the RxFIFO is read. If the reading of the FIFO does not reduce the fill level below that determined by the MR bits, then ISR[5] sets again within two X1 clock times. Further, if the MR fill level is set at 8 bytes AND there is a byte in the receiver shift register waiting for an empty FIFO location, then a read of the RxFIFO will cause ISR[5] to reset. It will immediately set again upon the transfer of the character in the shift register to the FIFO.

NOTE: The setting of ISR[5] means that the receiver has entered the bidding process. It is necessary for this bit to set for the receiver to generate an interrupt. It does **not** mean it **is** generating an interrupt.

ISR[4] – Transmitter Ready Channel b
The function of this bit is programmed by MR0[5:4] (normally set to 00). This bit is set when ever the number of empty TxFIFO positions exceeds or equals the level programmed in the MR0 register. This condition will almost always exist when the transmitter is first enabled. It will reset when the empty TxFIFO positions are reduced to a level less than that programmed in MR0[5:4] or the transmitter is disabled or reset.

The ISR[4] bit will reset with each write to the TxFIFO. If the write to the FIFO does not bring the FIFO above the fill level determined by the MR bits, the ISR[4] bit will set again within two X1 clock times.

NOTE: The setting of ISR[4] means that the transmitter has entered the bidding process. It is necessary for this bit to set for the transmitter to generate an interrupt. It does **not** mean it **is** generating an interrupt.

ISR[3] – Counter Ready
In the counter mode of operation, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command. It is initialized to '0' when the chip is reset.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time the C/T reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the C/T.

ISR[2] – Channel a Change in Break
This bit, when set, indicates that the receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a reset break change interrupt command.

ISR[1] – Receiver Ready or FIFO Full Channel a
See the description of ISR[5]. The channel 'a' receiver operation is the same as channel 'b'.

ISR[0] – Transmitter Ready Channel a
See the description of ISR[4]. Channel "a" transmitter operates in the same manner as channel "b."

IMR – Interrupt Mask Register

The programming of this register selects which interrupt sources will be allowed to enter the interrupt arbitration process. This register is logically ANDED with the interrupt status register. Its function is to allow the interrupt source it represents to join the bidding process if the corresponding IMR and ISR bits are both 1. It has no effect on the value in the ISR. It does not mask the reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read address at A5–A0 0Eh for C/T ab or read address 1Eh for C/T cd). After this, while in timer mode, the C/T will run continuously. Receipt of a subsequent start counter command causes the C/T to terminate the current timing cycle and to begin a new cycle using the values in the CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a "Stop Counter" command (read address at A5–A0 0Fh for C/T ab or read address 1Fh for C/T cd). The command, however, does not stop the C/T. It only resets the ISR[3] bit; the C/T continues to run. The ISR[3] bit will set again as the counter passes through 0. The generated square wave is output on an I/O pin if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded in CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching the terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter rolls over to 65535 and continues counting until stopped by the CPU. If I/O is programmed to be the output of the C/T, the output remains High until the terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower eight bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower eight bits to the upper eight bits occurs between the times that both halves of the counter is read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

I/O LOGIC

The QUART has four I/O pins for each channel. These pins may be individually programmed as an input or output under control of the I/OPCR (I/O Port Control Register). Functions which may use the I/O pins as inputs (Rx or Tx external clock, for example) are always sensitive to the signal on the I/O pin regardless of it being programmed as an input or an output. For example if I/O1a was programmed to output the RxC1X clock and the Counter/Timer was programmed to use I/O pin as its clock input the result would be the Counter/Timer being clocked by the RxC1X clock.

The 16 I/O ports are accessed and/or controlled by five (5) registers: IPR, ACR, I/OPCR, IPCR, OPR. They are shown in Table 6 of this document. Each UART has four pins. Two of these pins have "Change of State Detectors" (COS). These detectors set whenever the pin to which they are attached changes state. (1 to 0 or 0 to 1) The "Change of State Detectors" are enabled via the ACR. When enabled the COS devices may generate interrupts via the IMR and IPCR registers. Note that when the COS interrupt is enabled that any one or more of the four COS bits in the IPCR will enable the COS bidding. Each of the channel's four I/O lines are configured as inputs on reset.

The Change of State detectors sample the I/O pins at the rate of the 38.4KHz clock. A change on the pin will be required to be stable for at least 26.04µs and as much as 52.08µs for the COS detectors to confirm a change. Note that changes in the X1/clock frequency will effect this stability requirement.

Table 6.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

IPCR (Input Port Change Register ab) The lower four bits replicate the lower four bits of the IPR. The upper four bits reads state of Change detectors. Change detectors are enabled in ACR[3:0]. (DUART ab)

Deltal/O1b	Delta I/O0b	Delta I/O1a	Delta I/O0a	I/O1b	I/O0b	I/O1a	I/O0a
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

IPCR (Input Port Change Register cd) The lower four bits replicate the lower four bits of the IPR. The upper four bits reads state of Change detectors. Change detectors are enabled in ACR[3:0]. (DUART cd)

Delta I/O1d	Delta I/O0d	Delta I/O1c	Delta I/O0c	I/O1d	I/O0d	I/O1c	I/O0c
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

I/OPCR (I/O Port Configuration Register) One register for each UART.

I/O3x CONTROL	I/O2x CONTROL	I/O1x CONTROL	I/O0x CONTROL
Two bits for each I/O pin.			

This register controls the configuration of the I/O ports. It defines them as inputs or outputs and controls what sources will drive them in the case of outputs or which functions they will drive when used as an input. Each pin has four functions and hence two bits to control it. Each UART has one eight bit register to control its four I/O ports.

OPR (Output Port Register cd) for DUART cd

I/O3d	I/O2d	I/O3c	I/O2c	I/O1d	I/O0d	I/O1c	I/O0c
One bit for each pin. When I/O pins are configured as "General Purpose Outputs" the pins will be driven to the complement value of its associated OPR bit.							

OPR (Output Port Register ab) for DUART ab

I/O3b	I/O2b	I/O3a	I/O2a	I/O1b	I/O0b	I/O1a	I/O0a
One bit for each pin. When I/O pins are configured as "General Purpose Outputs" the pins will be driven to the complement value of its associated OPR bit.							

This register contains the data for the I/O ports when they are used as 'General Purpose Outputs' . The bits of the register are controlled by writing to the hex addresses at 0C and 1C. Ones written to the OPR drive the pins to 0; zeros drive the pins to 1. (The pins drive the value of the complement data written to the OPR)

IPR (Input Port Register cd) Reads I/O pins for DUART cd

I/O3d	I/O2d	I/O3c	I/O2c	I/O1d	I/O0d	I/O1c	I/O0c
0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

IPR (Input Port Register ab) Reads I/O pins for DUART ab

I/O3b	I/O2b	I/O3a	I/O2a	I/O1b	I/O0b	I/O1a	I/O0a
0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

This register reads the state of the 'I/O Ports'. The state of the I/O ports is read regardless of being programmed as inputs or outputs. The IPR can be thought of a just another 8 bit parallel port to the system data bus. The lower four bits of this register are replicated in the lower four bits of the IPCR register.

I/O Port Control Channel A (Channel C is similar)

IOPCR	IOPCRa[7:6]	IOPCRa[5:4]	IOPCRa[3:2]	IOPCRa[1:0]
	I/O3A	I/O2A	I/O1A	I/O0A
IOPCR = 00	IPR(5), TxCA in	IPR(4), RxCA in	IPR(1), C/Tab Clk in[1] TxCA in	IPR(0), CTSAN
IOPCR = 01	OPRab(5)	OPRab(4) RTSAN[1]	OPRab(1) RTSAN[2]	OPRab(0)
IOPCR = 10	TxC16A	RxC1A	RxC16A	TxC1A
IOPCR = 11	TxC1A	RxC16A	RxC1A	TxC16A

I/O Port Control Channel B (Channel D is similar)

IOPCR	IOPCRb[7:6]	IOPCRb[5:4]	IOPCRb[3:2]	IOPCRb[1:0]
	I/O3B	I/O2B	I/O1B	I/O0B
IOPCR = 00	IPR(7), TxCB in	IPR(6), RxCB in	IPR(3), TxCB in[1]	IPR(2), CTSBN
IOPCR = 01	OPRab(7)	OPRab(6) RTSBN[1]	OPRab(3) RTSBN[2]	OPRab(2)
IOPCR = 10	TxC16B	RxC1B	RxC16B	TxC1B
IOPCR = 11	TxC1B	RxC16B	RxC1B	TxC16B
The input part of the I/O pins is always active. The programming of the IOPCR bits to 00 merely turns off the out drivers and places the pin at high impedance.				

A read of the IPR register returns the value of the IPR bits as shown above. IPR(5) is at bit position 5 of the data bus. Note that the IPR bit positions do not follow the 0, 1, 2, 3 order of the I/O ports. During a read of the IPR the I/O ports are not latched. Therefore, it is possible to see changing data during the read. Port pins that have clocks on them may not yield valid data during the read.

Since the input circuits of the I/O ports are always active it is possible to direct the port signal back into the port. For example: I/O1 will output the RTS signal. Setting the Counter/Timer (C/T) to be clocked by the I/O1 port will result in the counter counting the number of times RTS goes active. The change of state detectors on I/O0 and I/O1 will, when programmed, always be sensitive to the signal on the port regardless of the source of that port's signal.

NOTES:

1. Normal configurations place RTSN output on I/O1 and place Tx external clock input on I/O3. For the 48 pin Dual In-Line package, I/O3 is not available. The following options allow flexible I/O programming with the 48 pin package:
   When IOPCR(7:6), the I/O3 control, ≠ 00, then I/O1 becomes available to the transmitter as an external clock.
   When IOPCR(5:4), the I/O2 control, = 01, then I/O2 may be the RTSN signal if MR1(7) = 1 and OPR(4) = 1.
2. I/O1 becomes RTSN when IOPCR(3:2) = 01 and MR1(7) = 1 and OPR(1) = 1. (OPR(3) for channel B)

Registers of the Interrupt System

The CIR, and "Global" registers are updated with the IACKN signal or from the "Update CIR" command at hex address 2A. These registers are not updated when IRQN is asserted since there could be a long time between the assertion of IRQN and the start of the interrupt service routine. (See notes following this section).

Current Interrupt Register (CIR)

# Bytes	Type	Chan #
3	3	2

The Channel # field indicates which of the four UARTs has the highest priority interrupt currently outstanding, while the Type field indicates its source within the UART. The Type field is encoded as follows:

000 No Interrupt
001 Change of State
x10 Transmit available
011 Receive available, no error
100 Receiver break change
101 Counter/Timer
111 Receive available, w/errors

With Type = x11, the # Bytes field indicates the count of received bytes available for reading, while with Type = x10 it indicates the number of bytes that can be written to the transmit FIFO.

The CIR is Read only at address 28H.

Global Interrupt Byte Count (GIBC)

00000	# Bytes
5	3

The GIBC is not an actual register but simply outputs the interrupting UART's transmit or receive byte counter value. The count, accurate at the time IACKN asserts, is captured in the CIR. The high order 5 bits are read as '0'. The GIBC is read only at address 2AH.

Global RxFIFO (GRxFIFO)

Received Data
8

Like the GIBC, no physical register implementation exists. The correct receiver's FIFO is popped based on the value of the interrupting channel field of the Current Interrupt Register.

If a receiver is not the cause of the current interrupt, a read of the Global RxFIFO will yield a byte containing all ones and NONE of the UART channels' receive FIFOs will be popped. (IMPORTANT)

The GRxFIFO is Read only at address 2BH.

Global TxFIFO (GTxFIFO)

Data to be Sent
8

Similar to the GRxFIFO, no physical register implementation exists. The byte is pushed into the correct transmitter's FIFO based on the interrupting channel field of the Current Interrupt Register.

If a transmitter is not the cause of the current interrupt, a write to the Global TxFIFO has no effect.

The GTxFIFO is Write only at address 2BH.

Global Interrupting Channel (GICR)

000000	Chan #
6	2

Like the other Global pseudo-registers no hardware register exists. The Channel number field of the Current Interrupt Register padded with leading zeros is output as the GICR. The GICR is Read only at address 29H.

C/Tab indicated by Channel code B 01
C/Tcd indicated by Channel code D 11

Interrupt Control (ICR)

Threshold	IVC
6	2

The Threshold Field is used by the interrupt comparator to determine if a winning interrupt "bid" should result in interrupting the host MPU. The threshold field resets to 00.

The IVC field controls what kind of vector the QUART returns to the host MPU during an Interrupt Acknowledge cycle:

00 Output contents of Interrupt Vector Register
01 Output 6 MSBs of IVR and Channel number as 2 LSBs
10 Output 3 MSBs of IVR, Interrupt Type and Channel number
11 Disable generation of vector during IACK cycle

The IVC field reset to 00. The ICR is read/write at address 2CH.

Bidding Control Registers (BCRs)

Rcv'd Break	State Change	C/T
3	3	2

This register is a transparent latch. It must be set to ensure the expected operation of the arbitration system. The 3 MSBs determine the priority of Received Break Interrupts; they are reset to 000.

Bits 4:2 determine the priority of Change of Input State interrupts, and are reset to 00.
There is one BCR per UART channel; they can be read or written at addresses 20-23H.
BCR Counter/Timer bits reset to 00.

Interrupt Vector (IVR)

Always Used	with IVC = 0x	w/IVC = 01 or 10
3	3	2

Holds the constant bits of the interrupt acknowledge vector. As shown, the three MSBs are always used, while the less significant bits can be replaced by the interrupt type code and/or Channel code bits contained in the CIR. The IVR is write only at address 29H.

DC ELECTRICAL CHARACTERISTICS[5, 6, 7]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL} V_{IH} V_{IH}	Input low voltage Input high voltage (except X1/CLK) Input high voltage (X1/CLK)		 2.0 $0.8V_{CC}$		0.8	V V V
V_{OL} V_{OH}	Output Low voltage Output High voltage (except OD outputs)	I_{OL} = 4.0mA I_{OH} = –400µA I_{OH} = –100µA	 $0.8V_{CC}$ $0.9V_{CC}$		0.4	V V V
I_{IL} I_{IH}	Input current Low, I/O ports Input current High, I/O ports	V_{IN} = 0 V_{IN} = V_{CC}	–10		 10	µA µA
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	–1		1	µA
I_{ILX1} I_{IHX1}	X1/CLK input Low current X1/CLK input High current	V_{IN} = GND, X2 = open V_{IN} = V_{CC}, X2 = open	–100		 100	µA µA
I_{OZH} I_{OZL}	Output off current High, 3–state data bus Output off current Low, 3–state data bus	V_{IN} = V_{CC} V_{IN} = 0	–1		10 1	µA
I_{ODL} I_{ODH}	Open–drain output Low current in off state: IRQN Open–drain output Low current in off state: IRQN	V_{IN} = 0 V_{IN} = V_{CC}	–1		1	µA
I_{CC}	Power supply current Operating mode	TTL input levels 25°C with X1 = 4MHz			50	mA
	Power down mode*				5	mA

* See UART application note for power down currents less than 5µA.

AC ELECTRICAL CHARACTERISTICS[5, 6, 7, 8]

SYMBOL	FIGURE	PARAMETER	LIMITS			UNIT
			Min	Typ	Max	
Reset timing						
t_{RES}	8	Reset pulse width	200			ns
I/O Port timing						
t_{PS}	9	I/O input setup time before RDN Low	0			ns
t_{PH}	9	I/O input hold time after RDN High	0			ns
t_{PD}	9	I/O output valid from WRN High RDN Low			 110 110	 ns ns
Interrupt timing						
t_{IR}	10	INTRN negated or I/O output High from: Read RHR (RxRDY/FFULL interrupt) Write THR (TxRDY interrupt) Reset command (break change interrupt) Reset command (I/O change interrupt) Stop C/T command (counter interrupt) Write IMR (clear of interrupt mask bit) With respect to a 3.6864MHz clock on pin X1/CLK			 100 100 100 100 100 100	 ns ns ns ns ns ns
Clock timing						
t_{CLK}	11	X1/CLK low/high time	125/100			ns
t_{CLK}	11	X1/CLK low/high time (above 4MHz; X1/CLK ÷ 2 active)	56/56			ns
t_{CLK}	11	X1/CLK frequency	0[9]	3.6864	8.0	MHz
t_{CTC}	11	Counter/timer clock high or low time	60			ns
f_{CTC}	11	Counter/timer clock frequency	0[9]		8	MHz
t_{RX}	11	RxC high or low time	30			ns
f_{RX}	11	RxC frequency (16X) RxC frequency (1X)	0[9] 0[9]		16 1.0	MHz MHz
t_{TX}	11	TxC high or low time	30			ns
f_{TX}	11	TxC frequency (16X) TxC frequency (1X)	0[9] 0[9]		16 1.0	MHz MHz
Transmitter timing						
t_{TXD}	12	TxD output delay from TxC low			120	ns
t_{TCS}	12	TxC output delay from TxD output data	–20		+20	ns
Receiver timing						
t_{RXS}	13	RxD data setup time to RxC high	100			ns
t_{RXH}	13	RxD data hold time from RxC high	100			ns

NOTES:

1. Stress above these listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other condition above those indicated in the operation section of the specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range. See ordering information table for applicable temperature range and operating supply range.
5. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of V_{IL} and V_{IH}, as appropriate.
6. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
7. Test condition for interrupt and I/O outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}. Test conditions for rest of outputs: C_L = 150pF.
8. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
9. This value is not tested, but is guaranteed by design. For t_{CLK} minimum test rate is 2.0MHz.

AC ELECTRICAL CHARACTERISTICS[4]

T_A = 25°C; V_{CC} = 5V ± 10%, unless otherwise specified. Limits shown as nn/nn refer to Commercial/Industrial temperature range. Single numbers apply to both ranges.

NO.	FIGURE	CHARACTERISTIC	LIMITS			UNIT
			Min	Typ	Max	
1	3	Setup: A[5:0] valid to CEN Low	10			ns
2	3	Hold: A[5:0] valid after CEN Low	45			ns
3	3	Access: Later of CEN Low and RDN Low, to Dnn valid (read)			110/115	ns
4	3	Later of CEN Low and (RDN or WRN as applicable) Low, to DACKN Low Normal Operation: From Power Down:	 10 + 2 X1 edges[5]		 90/122 + 3 X1 edges[5] 150	ns
5	3	Earlier of CEN High or RDN High, to Dnn released (read)[1]	0		30	ns
6	3	Earlier of CEN High or (RDN or WRN as applicable) High, to DACKN released	0		30	ns
7	3	Earlier of CEN High or (RDN or WRN as applicable) High, in one cycle, to later of CEN Low and (RDN or WRN as applicable) Low, for the next cycle	50			ns
8	3	Setup, Dnn valid (write) to later of CEN Low and WRN Low[2]	–30			ns
9	3	Later of CEN Low and WRN Low, to earlier of CEN High or WRN High	110/115			ns
10	3	Hold: Dnn valid (write) after DACKN Low, CEN High or WRN High[3]	0			ns

NOTES:
1. The minimum time indicates that read data will remain valid until the bus master drives CEN and/or RDN to High.
2. The fact that this parameter is negative means that the Dnn line may actually become valid after CEN and WRN are both Low.
3. In a Write operation, the bus master must hold the write data valid either until drives CEN and/or WRN to High, or until the QUART drives DACKN to Low, whichever comes first.
4. Test condition for interrupt and I/O outputs: C_L = 50pF, forced current for V_{OL} = 5.3mA; forced current for V_{OH} = 400µA, RL = 2.7kΩ to V_{CC}. Test condition for rest of outputs: C_L = 150pF
5. Consecutive write operations to the upper four bits of the Command Register (CR) require at least three X1/CLK edges; four X1/CLK edges in the 'X1/CLK divide by 2 edges' according to register 2E or 2F setting.

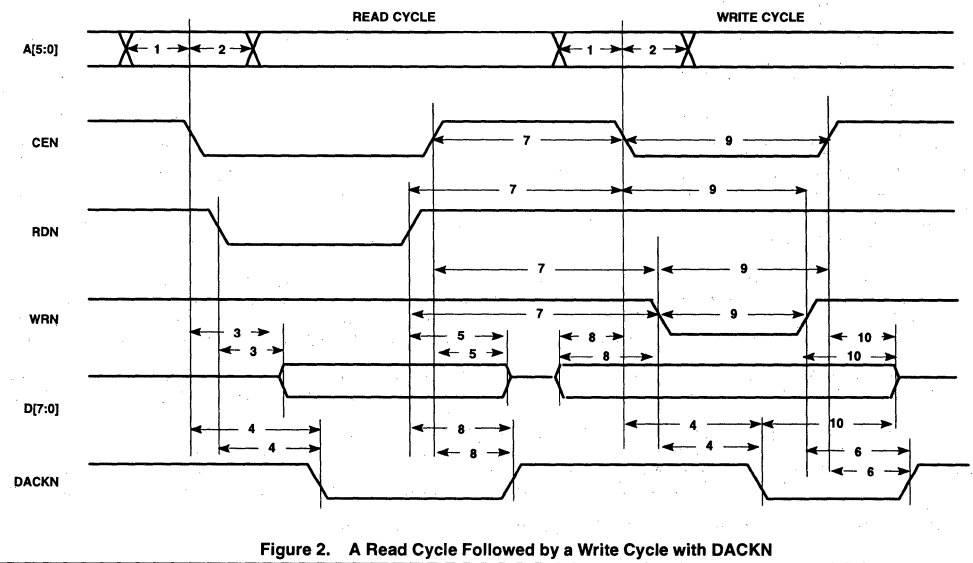


Figure 2. A Read Cycle Followed by a Write Cycle with DACKN

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = 5V \pm 10\%$, unless otherwise specified. Limits shown as nn/nn refer to Commercial/Industrial temperature range. Single numbers apply to both ranges.

NO.	FIGURE	CHARACTERISTIC	LIMITS			UNIT
			Min	Typ	Max	
1	4	D[7:0] Valid after IACKN Low			110/115	ns
2	4	DACKN Low after IACKN Low	10 + 2 X1 edges[1]		90/122 + 3 X1 edges[1]	ns
3	4	D[7:0] floating after IACKN High	0		30	ns
4	4	DACKN High after IACKN High	0		30	ns
5	4	IACKN High after IACKN Low	110/115			ns

NOTE:
1. Consecutive write operations to the upper four bits of the Command Register (CR) require at least three X1/CLK edges; four X1/CLK edges in the 'X1/CLK divide by 2 edges' according to register 2E or 2F setting.

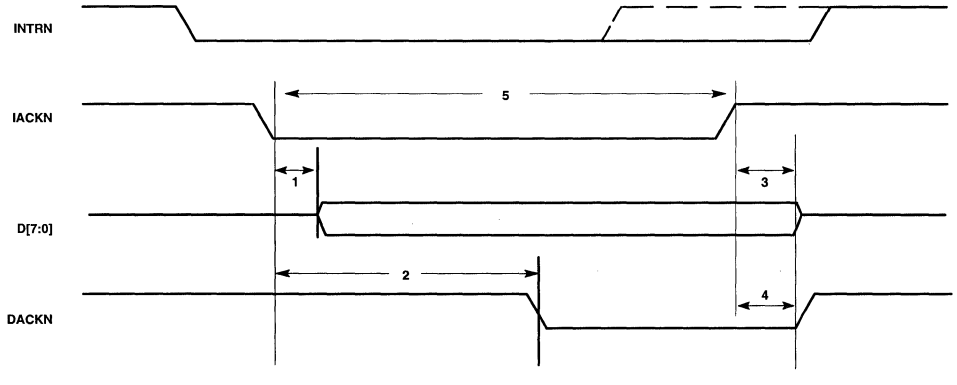


Figure 3. Interrupt Knowledge (IACKN) Timing

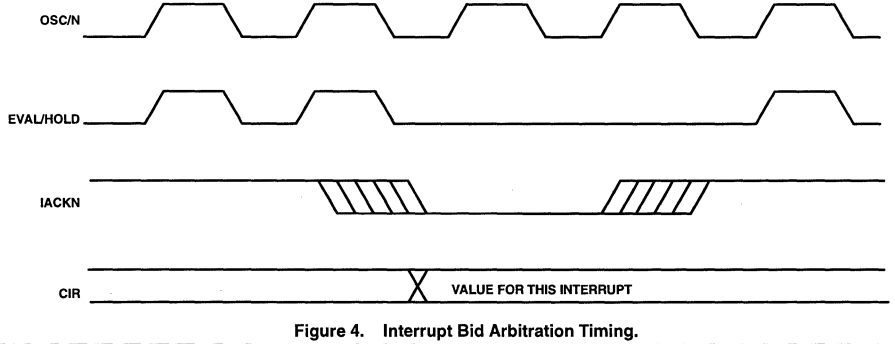


Figure 4. Interrupt Bid Arbitration Timing.

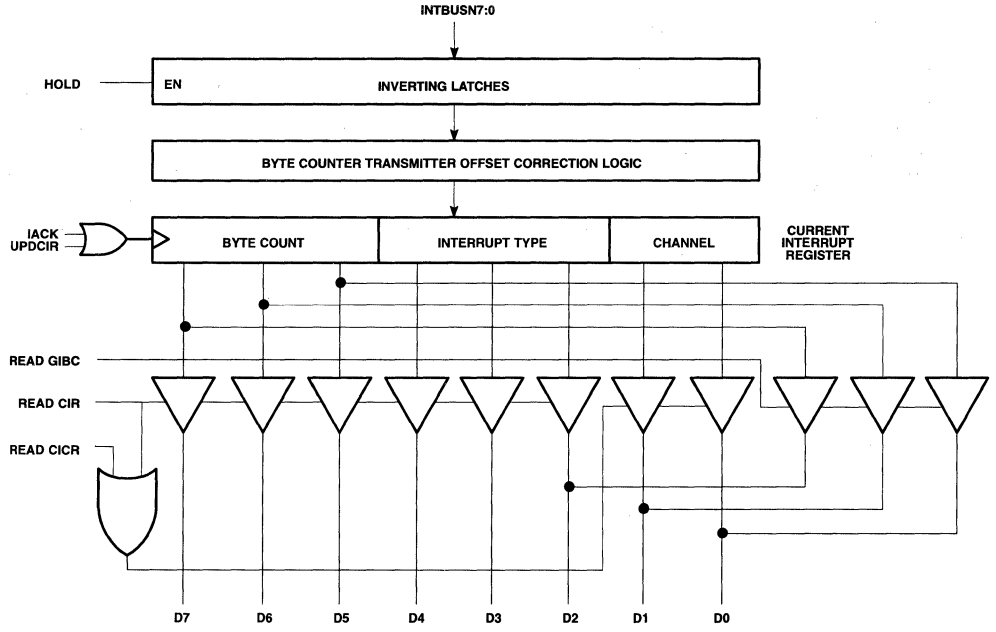


Figure 5. Current Interrupt Register Logic

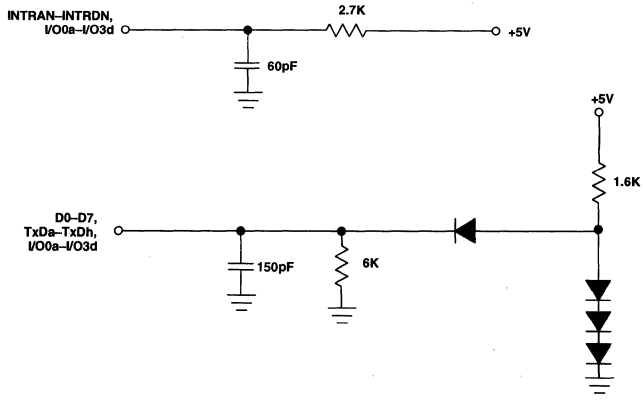


Figure 6. Test Conditions on Outputs

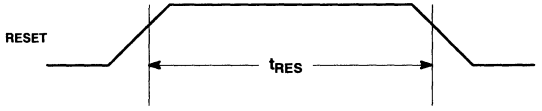
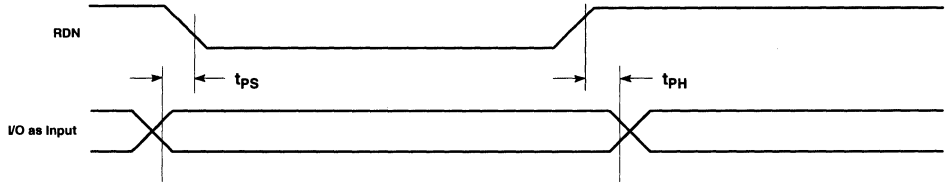
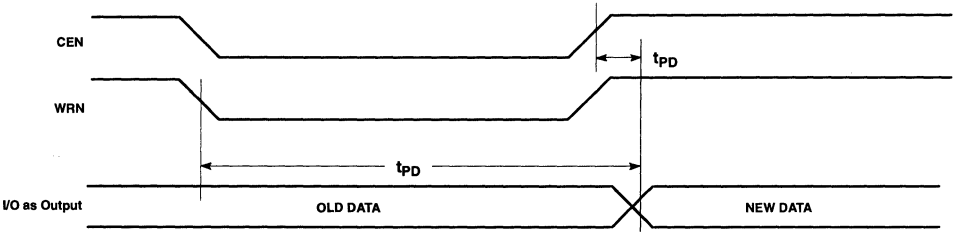


Figure 7. Reset Timing

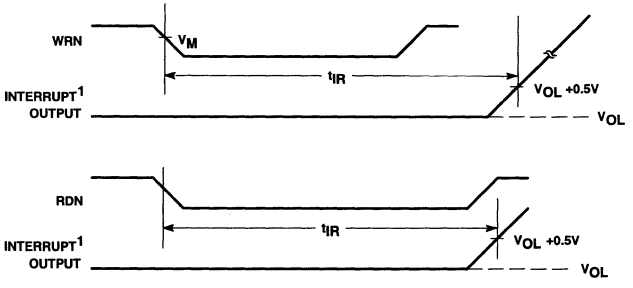


I/O PINS MUST BE STABLE FOR NON-CHANGING BUS DATA DURING THE READ.



NOTE: I/O PIN DATA IS NOT LATCHED

Figure 8. I/O Port Timing



NOTES:
1. INCLUDES I/O WHEN USED AS TxRDY or RxDY/FFULL OUTPUTS AS WELL AS INTRN.
2. THE TEST FOR OPEN DRAIN OUTPUTS IS INTENDED TO GUARANTEE SWITCHING OF THE OUTPUT TRANSISTOR. MEASUREMENT OF THIS RESPONSE IS REFERENCED FROM THE MIDPOINT OF THE SWITCHING SIGNAL, V_M, TO A POINT 0.5V ABOVE V_{OL}. THIS POINT REPRESENTS NOISE MARGIN THAT ASSURES TRUE SWITCHING HAS OCCURRED. BEYOND THIS LEVEL, THE EFFECTS OF EXTERNAL CIRCUITRY AND TEST ENVIRONMENT ARE PRONOUNCED AND CAN GREATLY AFFECT THE RESULTANT MEASUREMENT.

Figure 9. Interrupt Timing

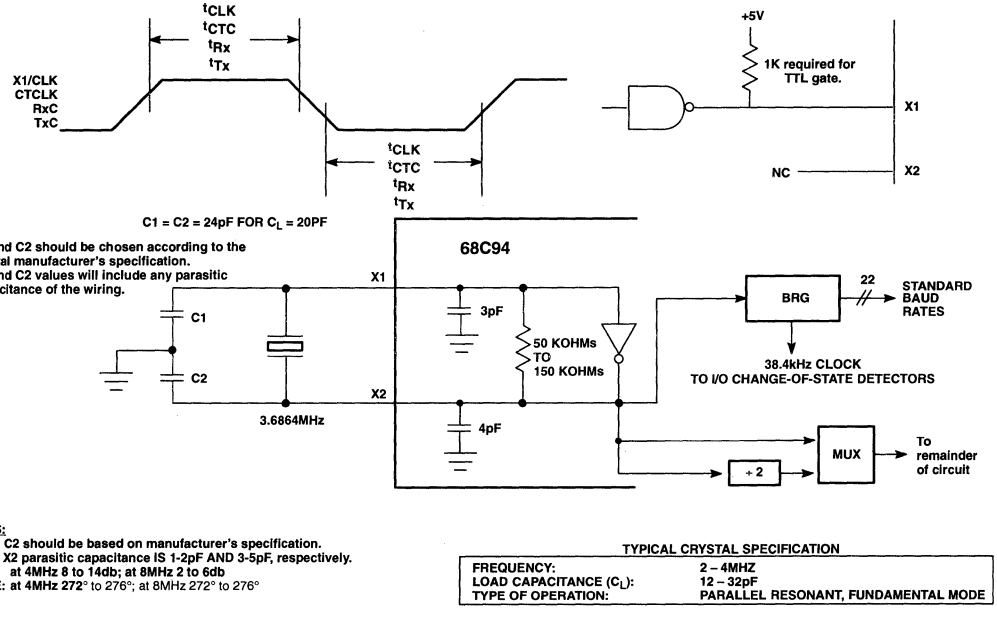


Figure 10. Clock Timing

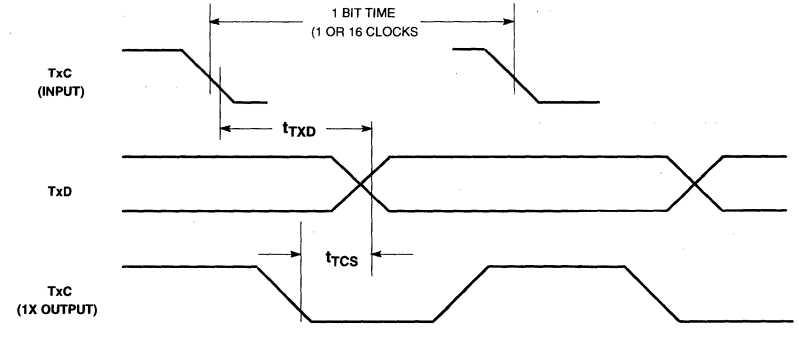


Figure 11. Transmit Clock Timing

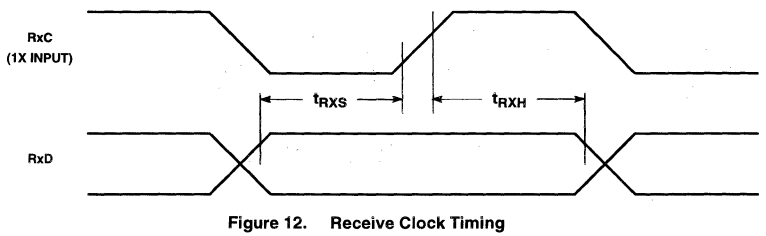


Figure 12. Receive Clock Timing

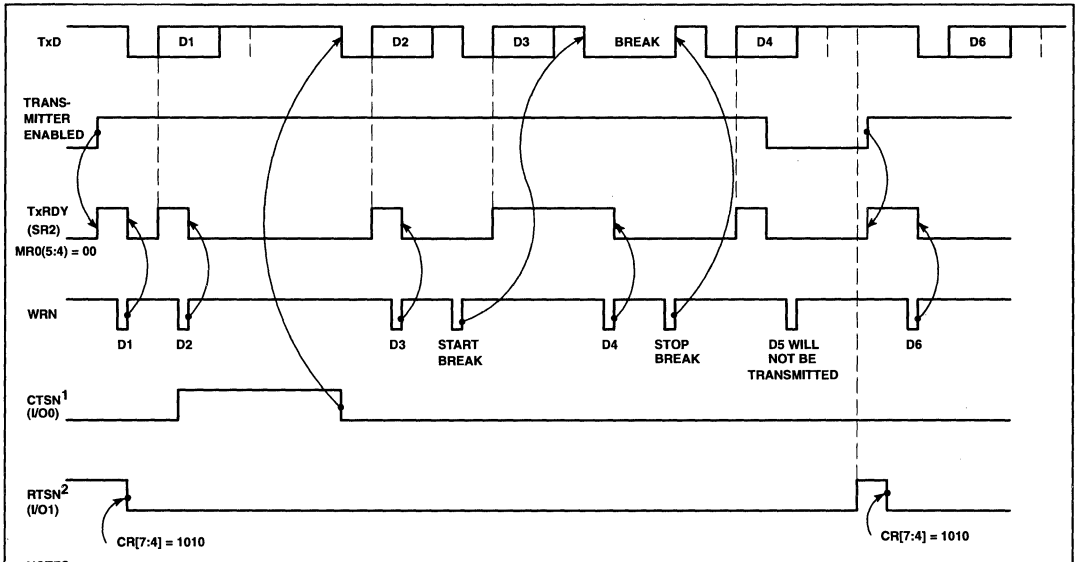


Figure 13. Transmitter Data Timing

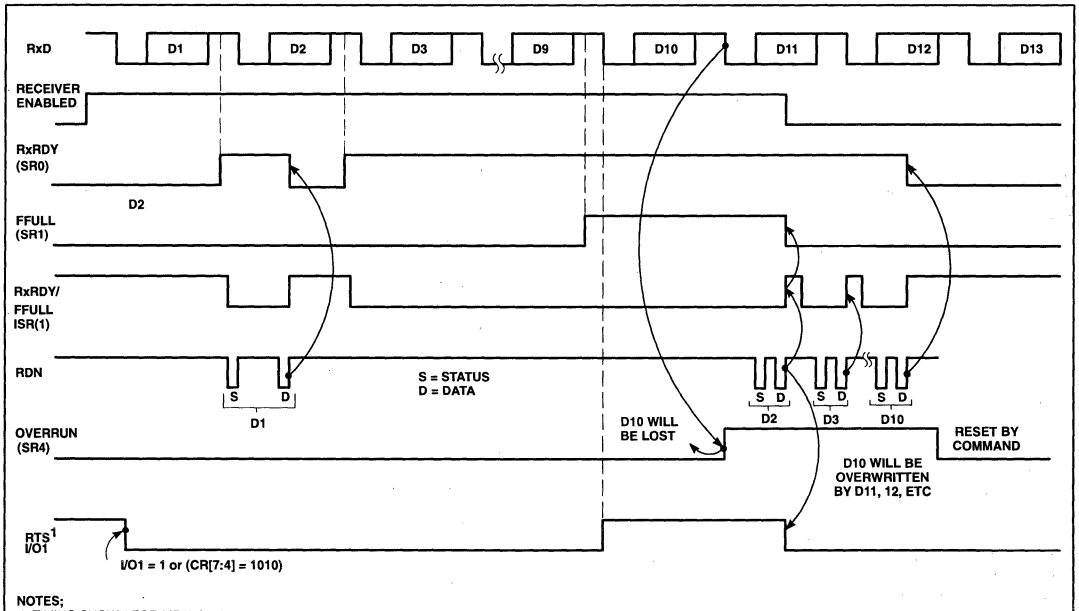


Figure 14. Receiver Data Timing

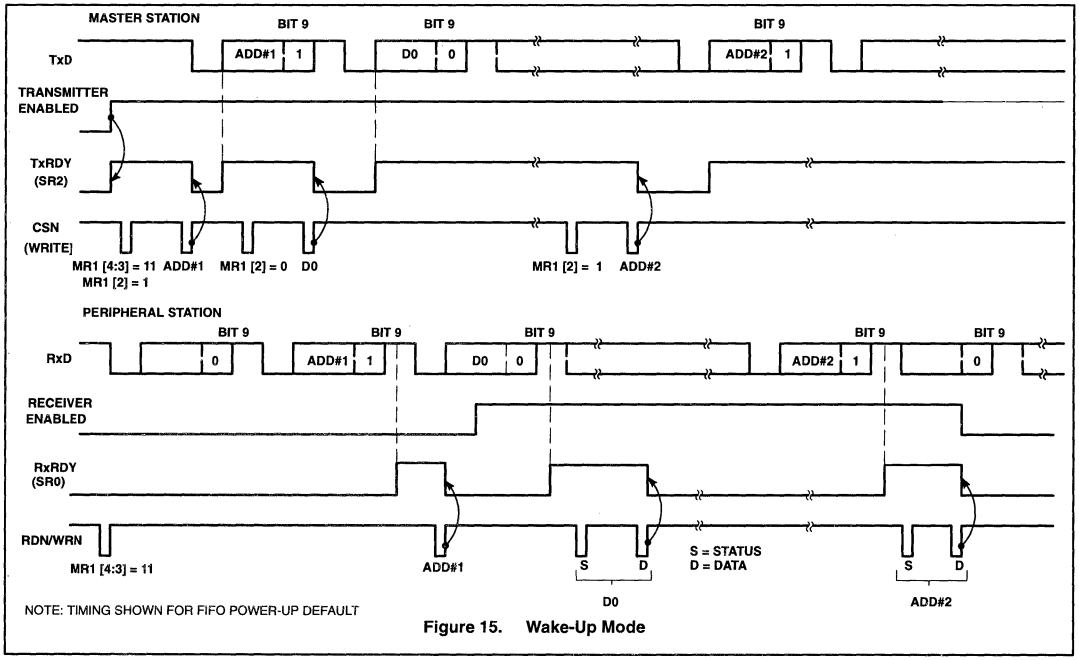


Figure 15. Wake-Up Mode

INTERRUPT NOTES

The following is a brief description of the new QUART "Bidding" interrupt system, interrupt vector and the use of the Global registers.

The new features of the QUARTs have been developed to greatly reduce the microprocessor time required to service uart interrupts. Bus cycle times have also been enhanced. By use of the new Current Interrupt Register (CIR) the speed of a polled system is also improved. For example programming the SCC2692 to interrupt on TxRDY and RxFUL would generate four interrupts for every six characters processed along with at least two additional accesses to the chip for each interrupt. This amounts to two non–data chip accesses per character. In the 68C94 this has been reduced to 0.25 non data accesses per character; an eight fold improvement. In certain conditions use of the global registers will yield a greater improvement.

The QUART has 18 possible sources which can be programmed to generate an interrupt:

- 4 Receiver channels
- 4 Transmitter Channels
- 4 Received "Break" conditions
- 4 Change of State Detectors (a total of 8 ports)
- 2 Counter/Timers

These sources are encoded in such a way that they generate a unique value. This value is defined by chip hardwire programming, user programming, and the source's present condition. The values the sources generate are compared (at the X1 clock rate) to a user defined Interrupt Threshold value contained in the ICR (Interrupt Control Register). When the source's value exceeds the threshold the interrupt is generated. It is the source's value which is captured in the CIR.

The heart of the interrupt speed enhancement is attained by allowing the interrupting source to encode its channel, interrupt type and, if appropriate, the number of FIFO bytes requiring service. This information is coded and transferred the CIR (Current Interrupt Register) at the time IACKN is asserted or the command 'Update CIR' is executed. Upon an interrupt the processor may read this register and in one access determine the "who, what and how much". This CIR value is used to drive the interrupt vector modification (when used) and the new "Global" registers.

"Global" Registers

The "Global Registers" are effectively pointers which use the contents of the CIR to direct a read or write operation to Rx or Tx or other source which is currently interrupting. There are four global registers defined in the register map:

1. Global Interrupting Byte Count
2. Global Interrupting Channel
3. Global Receive FIFO Register
4. Global Transmit FIFO Register

The global receive and transmit registers operate as an indirect address. The data read from the global receive register will be that of the currently interrupting receiver; the data written to the global transmit register will go to the currently interrupting transmitter. The interesting point here is that under certain circumstances an interrupt can be serviced without an interrogation of the chip.

For completeness it should be noted that the global registers are not physical devices. Reads of the Global Byte and Channel registers give the Byte count or Channel number, respectively, (right justified) of the interrupting channel. The CIR data is mapped to these "registers".

Table 7. "Bidding Format"

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION
Rx Byte count			Error 1	1	1	Channel No.		Receiver bid With error
Rx Byte count			no Error 0	1	1	Channel No.		Receiver bid No error
0	Tx Byte Count			1	0	Channel No.		Transmit bid
Programmable			1	0	0	Channel No.		Receive Break
Programmable			0	0	1	Channel No.		Change of State
Programmable		0	1	0	1	Channel No.		Counter/Timer

NOTES:
1. The ones and zeros above represent the hardwired positions.
2. Note the format of bits 4:2. They represent the identity of the interrupting source.
3. Bids with the highest number of contiguous MSBs win the bid.
   - 1 1 1 Receiver with error
   - 0 1 1 Receiver without error
   - x 1 0 Transmitter
   - 1 0 0 Receiver Break detect
   - 0 0 1 Change of State
   - 1 0 1 Counter/Timer
   - 0 0 0 No interrupt

In these identifiers the receivers are biased to have highest priority. The identifier bits and the channel number bits are hardwired on the chip. Normally the non–data interrupts would be programmed to a low value. The programmable fields can, in some cases, make these sources higher than a full receiver.

It would seem that a 11 programmed in the upper counter/timer bits, for example, would cause it to interrupt nearly all the time. This is not true . A counter/timer that has not timed out will not bid. In a similar fashion a receiver FIFO that is empty or a transmitter FIFO that is full will not bid

In general terms the threshold value programmed in the ICR (Interrupt Control Register) will reflect some fill level of the eight character transmit and receive FIFOs that allow processor service without underrun or overrun occurring.

Note that interrupt threshold value in the ICR is 6 bits long. This value is aligned with the bid arbitration logic such that it bids only through the most significant 6 bits. The result of this is that the channel value does not 'bid'. However the logic is such that other parts of the bid being equal the condition of the highest channel will be captured in CIR. The increasing order of the channels is A, B, C, D. Thus channel D is the "strongest" of the four.

It could be that the giving the highest strength to channel D may, from time to time, not be what would be most desired. Further it may be desired to alter the authority of a channel's bid. This may be done by setting the Rx and/or Tx interrupt bits in MR0 and MR1 to values different than zero. This will have the effect of not allowing the associated receiver or transmitter to bid until its FIFO reaches a particular fill level. Although this compromises the idea of the bidding interrupt scheme, it is entirely safe to use. In fact it is setting of MR0 and MR1 interrupt bits to zero that causes the receiver to stop bidding when it is empty and causes the transmitter to stop bidding when it is full. Altering the MR0 and MR1 interrupt bits only changes the level at which the Rx & Tx bidding is stopped.

See the "Interrupt Note on 68C94" which refers to the use of the MR registers in controlling the Rx and Tx bidding.

In normal operation the character of an interrupt will be controlled by the above registers in conjunction with the IMR (Interrupt Mask Register (one for each DUART)) . The function of the IMR will be to enable bidding of any particular source. Recall that the QUART has 18 functions which may generate an interrupt.

The format of the interrupt vector is controlled by the ICR[1:0] bits. The formats are shown in Table 7. The purpose of the vector modification is to allow the interrupting source (either channel or type and channel) to direct the processor to appropriate service routine. We have found that some users wish to use extremely tight loops for the service routines and find the addition of several tests of status bytes to be very 'expensive' in processor time.

NOTE ON QUART INTERFACE TO ITS CONTROLLING PROCESSOR

The QUART, has been designed to interface in either the synchronous interrupt environment (without DACKN) or the asynchronous interrupt environment (with DACKN). The 80xxx devices of Intel design are usually operated in a synchronous interrupt mode while those of Motorola design, 68xxx devices, operate in an asynchronous interrupt mode.

Note: Synchronous and asynchronous interrupt modes are not in any way associated with synchronous or asynchronous data transmission.

The QUART has been designed with the pins required to service either interface. In general then it is probable that in any application some of the interface pins will not be used. This note discusses what is required for the "text book" connections of the two methods. It should be noted that features of either method are not mutually exclusive.

The interface pins are all active low. (at V_{SS} or ground) The pins used for normal reading and writing to the QUART (the generation of a bus cycle) are CEN (Chip Enable), RDN (Read Enable), WRN (Write Enable). The pins used in the interrupt service are IRQN (Interrupt Request), IACKN (Interrupt Acknowledge). The pin used for data transfer is DACKN (Data Acknowledge). IRQN and DACKN are open drain outputs.

DACKN signaling can be enabled or disabled via writing to address 27h or 26h respectively. Note that if DACKN is enabled that writing to the QUART will occur on the falling edge of DACKN. The use of hardware reset (required at power up) enables DACKN.

Table 8. Configuration of Interrupt Vector for the QUART

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Interrupt vector for → ICR[1:0]=00	INTERRUPT VECTOR FORMATS (Controlled by ICR[1:0])							
	IVR[7:0]							
	Full interrupt vector							
Interrupt vector for → ICR[1:0]=01								
	IVR[7:2]						ICR[1:0]	
	Interrupt vector 6 MSBs						Channel number	
Interrupt vector for → ICR[1:0]=10								
	IVR[7:5]			ICR[4:2]			ICR[1:0]	
	Interrupt vector 3 MSBs			Interrupt type			Channel number	
Interrupt vector for → ICR[1:0]=11 (Inhibit)								
	Inhibit vector output. (Set bus to FFh)							
	CURRENT INTERRUPT REGISTER FORMAT CIR[7:0]							
	Rx or Tx byte count			Interrupt type: R/Tx CT COS BRK			Channel number	
	INTERRUPT CONTROL REGISTER FORMAT ICR[0:7]							
	Interrupt threshold ICR[7:2]						Interrupt vector format ICR[1:0]	

The Asynchronous Interface

Those familiar with 68xxx I/O will note the use of the two pins RDN and WRN to be in conflict with 68xxx devices use of the one R/WN pin. The R/WN must be inverted such that the R/WN may drive the WRN input while the inversion of R/WN drives the RDN input. It is good practice to condition the inversion of R/WN such that RDN will not become active on the termination of a write to the QUART while CEN is still asserted. These short periods of read could upset FIFO pointers in the chip.

During a read of the QUART DACKN signals that valid data is on the data bus. During a write to the QUART DACKN signals that data placed on the bus by the control processor has been written to the addressed register. The generation of DACKN begins with the start of a bus cycle (Read, Write or Interrupt Acknowledge) and then requires two edges of the X1 clock plus typically 70ns for its assertion.

In this mode the writing of data to the QUART registers occurs on the falling edge of DACKN or the rising edge of the combination of CEN and WRN which ever occurs first. This requires that the data to be written to the QUART registers be valid with respect to the leading edge of the combination of CEN and WRN. (In the synchronous mode it is the trailing edge)

IACKN updates the CIR (Current Interrupt Register) and places the Interrupt Vector or Modified Interrupt Vector on the bus if the Interrupt Vector is used.

The Synchronous Interface

In this mode the DACKN and IACKN are usually not used. Here data is written to the QUART on the trailing edge of the combination of CEN and WRN. The placing of data on the bus during a read cycle begins with the leading edge of the combination of CEN and RDN.

The read cycle will terminate with the rise of CEN or RDN which ever one occurs first. In this mode bus cycles are usually setup to be the minimum time required by the QUART and hence will be faster than bus cycles that are defined by the DACKN signal. DACKN should be turned off in this mode.

When IACKN is not used or is not available the command at 2Ah should be used to update the CIR (Current Interrupt Register). This register is normally updated by IACKN in response to the IRQN. Note that the CIR is not updated by IRQN since there could be a long time between the assertion of IRQN and the start of the interrupt service routine. During this time it is quite possible that another interrupt with a higher priority occurs. It is the CIR that contains the information that describes the interrupt source and its priority. It is therefor recommended that the first operation upon entering the interrupt service routine is the updating of the CIR. (Recall that the contents of the GLOBAL registers reflect the content of the CIR)

Summary

In the asynchronous mode all of the interface pins are usually used. The synchronous mode usually will not use the IACKN and DACKN. However there is no conflict in the quart if both modes are used in the same application. (i.e. More than one device may control the QUART) The principles to keep in mind are:

1. When IACKN is not used the CIR should be updated via command.
2. If DACKN is not used it should be disabled.
3. When in the asynchronous mode be sure DACKN is enabled.
4. With 68xxx type controllers the RDN signal must be generated.

SC26C94 and SC68C94 (QUARTs) interrupt system and processor interface

Author: Peter Narvaez

INTRODUCTION

The following is a brief description of the new QUART "BIDDING" interrupt system, interrupt vector and the use of the Global registers.

It has long been recognized that our "long standing" Industry Standard UARTs generated a great deal of interrupt overhead when used in higher speed environments along with slow bus cycle times. The new features of the QUARTs (SC26C94 and SC68C94) have been developed to greatly reduce the microprocessor time required to service UART interrupts. Bus cycle times have also been enhanced. By use of the new Current Interrupt Register (CIR) the speed of a poled system is also improved. For example programming the SCC2692 to interrupt on TxRDY and RxFUL would generate four interrupts for every six characters processed along with at least two additional accesses to the chip for each interrupt. This amounts to two non–data chip accesses per character. In the 26C94 this has been reduced to 0.25 non data accesses per character; an eight fold improvement. In certain conditions use of the global registers will yield a greater improvement.

The QUART has 18 possible sources which can be programmed to generate an interrupt:

- 4 Receiver channels
- 4 Transmitter Channels
- 4 Received "Brake" conditions
- 4 Change of State Detectors. (A total of 8 ports)
- 2 Counter/Timers

These sources are encoded in such a way that they generate a unique value. This value is defined by chip hardwire programming, user programming, and the source's present condition. The values the sources generate are compared (at the X1 clock rate) to a user defined Interrupt Threshold value contained in the ICR (Interrupt Control Register). When the source's value exceeds the threshold the interrupt is generated. It is the source's value which is captured in the CIR.

The heart of the interrupt speed enhancement is attained by allowing the interrupting source to encode its channel, interrupt type and, if appropriate, the number of FIFO bytes requiring service. This information is coded and transferred to the CIR (Current Interrupt Register). Upon an interrupt, the processor may read this register and in one access determine the "who, what and how much". This CIR value is used to drive the interrupt vector modification (when used) and the new "Global" registers.

The "Global Registers" are effectively pointers which use the contents of the CIR to direct a read or write operation to Rx or Tx which is currently interrupting. There are four global registers defined in the register map:

1. Global Interrupting Byte Count
2. Global Interrupting Channel
3. Global Receive Holding Register
4. Global Transmit Holding Register

The global receive and transmit registers operate as an indirect address. The data read from the global receive holding register will be that of the currently interrupting receiver; the data written to the global transmit holding register will go to the currently interrupting transmitter. The interesting point here is that under certain circumstances an interrupt can be serviced without an interrogation of the chip.

For completeness it should be noted that the global registers are not physical devices. Reads of the Global Byte and Channel registers give the Byte count or Channel number, respectively, (right justified) of the interrupting channel. The CIR data is mapped to these "registers".

In these identifiers (see Table 1) the receivers are biased to have highest priority. The identifier bits and the channel number bits are hardwired on the chip. Normally the non-data interrupts would be programmed to a low value. The programmable fields can, in some cases, make these sources higher than a full receiver. It would seem that a 11 programmed in the upper counter/timer bits, for example, would cause it to interrupt nearly all the time. **This is not true**. A counter/timer that has not timed out will not bid. In a similar fashion a receiver FIFO that is empty or a transmitter FIFO that is full will not bid.

In general terms the threshold value programmed in the ICR (Interrupt Control Register) will reflect some fill level of the eight character transmit and receive FIFOs that allow processor service without underrun or overrun occurring.

In normal operation the character of an interrupt will be controlled by the above registers in conjunction with the IMR (Interrupt Mask Register (one for each DUART)) . The function of the IMR will be to enable bidding of any particular source. Recall that the QUART has 18 functions which may generate an interrupt.

Table 1. Bidding Format

Bit 7	Bit 6	Bit 5	Bit 4[4]	Bit 3[4]	Bit 2[4]	Bit 1	Bit 0	Function
Rx Byte count			Error 1	1	1	Channel No.		Receiver bid with error
Rx Byte count			no Error 0	1	1	Channel No.		Receiver bid no error
0	Tx Byte count			1	0	Channel No.		Transmit bid
Programmable			1	0	0	Channel No.		Receive Brake
Programmable			0	0	1	Channel No.		Change of State
Programmable		0	1	0	1	Channel No.		Counter/Timer

NOTE:

4. The 1's and 0's represent hardwired bits and show the identity of the interrupting source.
   - 1 1 1 Receiver with error
   - 0 1 1 Receiver without error
   - x 1 0 Transmitter
   - 1 0 0 Receiver brake detect
   - 0 0 1 Change of State
   - 1 0 1 Counter/Timer
   - 0 0 0 No interrupt

SC26C94 and SC68C94 (QUARTs) interrupt system and processor interface

Table 2. Configuration of Interrupt Vector for the QUART

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Interrupt vector for → ICR[1:0] = 00	INTERRUPT VECTOR FORMATS (Controlled by ICR[1:0])							
	IVR[7:0]							
	Full interrupt vector							
Interrupt vector for → ICR[1:0] = 01								
	IVR[7:2]						ICR[1:0]	
	Interrupt vector 6 MSBs						Channel number	
Interrupt vector for → ICR[1:0] = 10								
	IVR[7:5]			ICR[4:2]			ICR[1:0]	
	Interrupt vector 3 MSBs			Interrupt type			Channel number	
Interrupt vector for → ICR[1:0] = 11 (Inhibit)								
	Inhibit vector output (Set bus to FFh)							
	CURRENT INTERRUPT REGISTER FORMAT CIR[7:0]							
	Rx or Tx byte count			Interrupt type: R/Tx CT COS BRK			Channel number	
	INTERRUPT CONTROL REGISTER FORMAT ICR[0:7]							
	Interrupt threshold ICR[7:2]						Interrupt vector format ICR[1:0]	

Note that interrupt threshold value in the ICR is 6 bits long. This value is aligned with the bid arbitration logic such that it bids only through the most significant 6 bits. The result of this is that the channel value does not "bid'. However, the logic is such that, other parts of the bid being equal, the condition of the highest channel will be captured in CIR. The increasing order of the channels is A, B, C, D. Thus channel D is the "strongest~ of the four.

It could be that giving the highest strength to channel D may, from time to time, not be what would be most desired. Further it may be desired to alter the authority of a channel's bid. This may be done by setting the Rx and/or Tx interrupt bits in MR0 and MR1 to values different than zero. This will have the effect of not allowing the associated receiver or transmitter to bid until its FIFO reaches a particular fill level. Although this compromises the idea of the bidding interrupt scheme, it is entirely safe to use. In fact it is the setting of MR0 and MR1 interrupt bits to zero that causes the receiver to stop bidding when it is empty and causes the transmitter to stop bidding when it is full. Altering the MR0 and MR1 interrupt bits only changes the level at which the Rx and Tx bidding is stopped.

The format of the interrupt vector is controlled by the ICR[1:0] bits. The formats are shown in Table 2. The purpose of the vector modification is to allow the interrupting source (either channel or type and channel) to direct the processor to the appropriate service routine. We have found that some users wish to use extremely tight loops for the service routines and find the addition of several tests of status bytes to be very 'expensive' in processor time.

Processor Interface Note

Note: Familiarity with the QUART Interrupt Arbitration system is assumed.

This device, commonly called the QUART, has been designed to Interface in either the synchronous interrupt environment (without DACKN) or the asynchronous interrupt environment (with DACKN). The 80xxx devices of Intel design are usually operated in a synchronous interrupt mode while those of Motorola design, 68xxx devices, operate in an asynchronous interrupt mode.

Note: Synchronous and asynchronous interrupt modes are not in any way associated with synchronous or asynchronous data transmission.

The QUART has been designed with the pins required to service either interface. In general then it is probable that in any application some of the interface pins will not be used. This note discusses what is required for the "text book" connections of the two methods. It should be noted that features of either method are not mutually exclusive.

The interface pins are all active low. (at V_{SS} or ground) The pins used for normal reading and writing to the QUART (the generation of a bus cycle) are CEN (Chip Enable), RDN (Read Enable), WRN (Write Enable). The pins used in the interrupt service are IRQN (Interrupt Request), IACKN (Interrupt Acknowledge). The pin used for data transfer is DACKN (Data Acknowledge). IRQN and DACKN are open drain outputs.

DACKN signaling can be enabled or disabled via writing to address 27h or 26h, respectively. The use of hardware reset (required at power up) enables DACKN.

The Asynchronous Interface

Those familiar with 68xxx I/O will note the use of the two pins RDN and WRN to be in conflict with 68xxx devices use of the one R/WN pin. The R/WN must be inverted such that the R/WN may drive the WRN input while the inversion of R/WN drives the RDN input. It is good practice to condition the inversion of R/WN such that RDN will not become active on the termination of a write to the QUART while CEN is still asserted. These short periods of read could upset FIFO pointers in the Chip.

During a read of the QUART, DACKN signals that valid data is on the data bus. During a write to the QUART, DACKN signals that data placed on the bus by the control processor has been written to the addressed register. The generation of DACKN begins with the start of a bus cycle (Read, Write or Interrupt Acknowledge) and then requires two edges of the X1 clock plus 70ns for its assertion.

In this mode the writing of data to the QUART registers occurs on the falling edge of DACKN or the rising edge of the combination of

SC26C94 and SC68C94 (QUARTs) interrupt system and processor interface

CEN and WRN which ever occurs first. This requires that the data to be written to the QUART registers be valid with respect to the leading edge of the combination of CEN and WRN. (In the synchronous mode it is the trailing edge.)

IACKN updates the CIR (Current Interrupt Register) and places the Interrupt Vector or Modified Interrupt Vector on the bus if the Interrupt Vector is used.

The Synchronous Interface

In this mode the DACKN and IACKN are usually not used. Here data is written to the QUART on the trailing edge of the combination of CEN and WRN. The placing of data on the bus during a read cycle begins with the leading edge of the combination of CEN and RDN. The read cycle will terminate with the rise of CEN or RDN which ever one occurs first. In this mode bus cycles are usually setup to be the minimum time required by the QUART and hence will be faster than bus cycles that are defined by the DACKN signal. DACKN should be turned off in this mode.

When IACKN Is not used or Is not available the command at 2Ah should be used to update the CIR (Current Interrupt Register). This register is normally updated by IACKN in response to the IRQN.

Note that the CIR is not updated by IRQN since there could be a long time between the assertion of IRQN and the start of the interrupt service routine. During this time it is quite possible that another interrupt with a higher priority occurs. It is the CIR that contains the information that describes the interrupt source and its priority. It is, therefore, recommended that the first operation upon entering the interrupt service routine is the updating of the CIR. (Recall that the contents of the GLOBAL registers reflect the content of the CIR)

Summary

In the asynchronous mode all of the interface pins are usually used. The synchronous mode usually will not use the IACKN and DACKN. However, there is no conflict in the QUART if both modes are used in the same application (i.e., more than one device may control the QUART). The principles to keep in mind are:

1. When IACKN is not used the CIR should be updated via command.
2. If DACKN is not used it should be disabled.
3. When in the asynchronous mode be sure DACKN is enabled.
4. With 68xxx type controllers the RDN signal must be generated.

Enhanced octal universal asynchronous receiver/transmitter (Octal UART)

SCC2698B

DESCRIPTION

The SCC2698B Enhanced Octal Universal Asynchronous Receiver/Transmitter (Octal UART) is a single chip MOS-LSI communications device that provides eight full-duplex asynchronous receiver/transmitter channels in a single package. It is fabricated with CMOS technology which combines the benefits of high density and low power consumption.

The operating speed of each receiver and transmitter can be selected independently as one of eighteen fixed baud rates, a 16X clock derived from a programmable counter/timer, or an external 1X or 16X clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the Octal UART particularly attractive for dual-speed channel applications such as clustered terminal systems.

The receiver is quadruple buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote UART transmitter when the receiver buffer is full.

The UART provides a power-down mode in which the oscillator is frozen but the register contents are stored. This results in reduced power consumption on the order of several magnitudes. The Octal UART is fully TTL compatible and operates from a single +5V power supply.

The SCC2698B is an upwardly compatible version of the 2698A Octal UART. In PLCC packaging, it is enhanced by the addition of receiver ready or FIFO full status outputs, and transmitter empty status outputs for each channel on 16 multipurpose I/O pins. The multipurpose I/O pins of the SCC2698B were inputs only on the SCC2698A.

FEATURES

- Eight full-duplex independent asynchronous receiver/transmitters
- Quadruple buffered receiver data register
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- Baud rate for the receiver and transmitter selectable from:
  - 18 fixed rates: 50 to 38.4K baud
    Non-standard rates to 115.2K baud
  - User-defined rates from the programmable counter/timer associated with each of four blocks
  - External 1x or 16x clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal (full-duplex), automatic echo, local loop back, remote loopback
- Four multi-function programmable 16-bit counter/timers
- Four interrupt outputs with eight maskable interrupting conditions for each output
- Receiver ready/FIFO full and transmitter ready status available on 16 multi-function pins in PLCC package
- On-chip crystal oscillator
- TTL compatible
- Single +5V power supply with low power mode
- Eight multi-purpose output pins
- Sixteen multi-purpose I/O pins
- Sixteen multi-purpose Input pins with pull-up resistors

ORDERING INFORMATION

PACKAGES	V_{CC} = +5V ±5%, T_A = 0°C to +70°C	V_{CC} = +5V ±5%, T_A = −40°C to +85°C	DWG #
64-Pin Plastic Dual In-Line Package (DIP)	SCC2698BC1N64	SCC2698BE1N64	0414B
84-Pin Plastic Leaded Chip Carrier (PLCC)	SCC2698BC1A84	SCC2698BE1A84	0399F

NOTE: Pin Grid Array (PGA) package version is available from Philips Components Military Division.

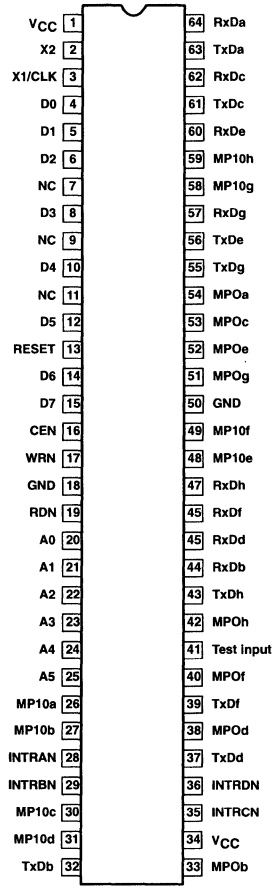
ABSOLUTE MAXIMUM RATINGS[1]

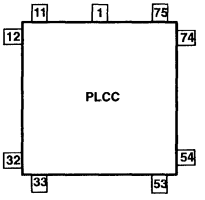
SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range[2]	Note 4	°C
T_{STG}	Storage temperature range	−65 to +150	°C
V_{CC}	Voltage from V_{DD} to GND[3]	−0.5 to +7.0	V
V_S	Voltage from any pin to ground[3]	−0.5 to V_{CC} +0.5	V
P_D	Power dissipation	1	W

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range. See ordering information table for applicable temperature range and operating supply range.

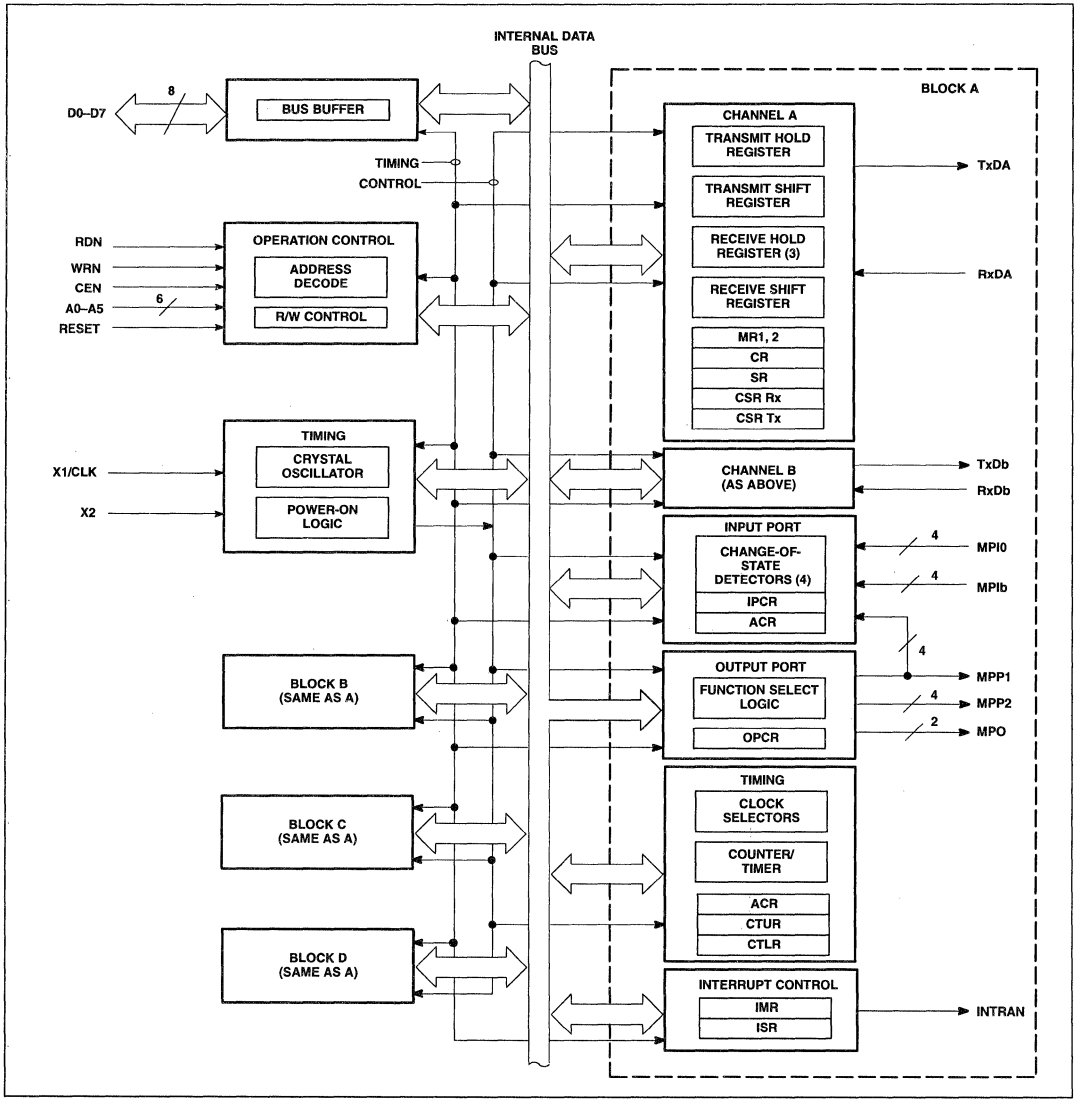
PIN CONFIGURATIONS





Pin	Function	Pin	Function	Pin	Function
1	TxDa	29	A3	57	RxDd
2	MPP2g	30	MPP2b	58	RxDf
3	RxDa	31	A4	59	RxDh
4	MPP2h	32	A5	60	MPI1e
5	V_{CC}	33	MPI0a	61	MPI0e
6	X2	34	MPI0b	62	MPI1f
7	X1/CLK	35	INTRAN	63	MPI0f
8	D0	36	INTRBN	64	MPP1e
9	D1	37	MPI0c	65	GND
10	D2	38	MPI1c	66	MPP1f
11	D3	39	MPI0d	67	MPOg
12	D4	40	MPI1d	68	MPP2e
13	D5	41	TxDb	69	MPOe
14	MPI1a	42	MPP1c	70	MPP2f
15	RESET	43	MPOb	71	MPOc
16	D6	44	MPP1d	72	MPOa
17	D7	45	V_{CC}	73	TxDg
18	CEN	46	INTRCN	74	TxDe
19	WRN	47	INTRDN	75	RxDg
20	GND	48	MPP2c	76	MPI0g
21	MPI1b	49	TxDd	77	MPI0h
22	RDN	50	MPP2d	78	MPI1g
23	A0	51	MPOd	79	RxDe
24	MPP1a	52	TxDf	80	MPIh
25	A1	53	MPOf	81	TxDc
26	MPP1b	54	MPOh	82	MPP1g
27	A2	55	TxDh	83	RxDc
28	MPP2a	56	RxDb	84	MPP1h

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO. DIP	PIN NO. PLCC	TYPE	NAME AND FUNCTION
D0–D7	4–6, 8, 10, 12, 14, 15	8–13, 16, 17	I/O	**Data Bus:** Active–High 8-bit bidirectional 3-State data bus. Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the Octal UART take place over this bus. The direction of the transfer is controlled by the WRN and RDN inputs when the CEN input is low. When the CEN input is High, the data bus is in the 3-State condition.
CEN	16	18	I	**Chip Enable:** Active-Low input. When Low, data transfers between the CPU and the Octal UART are enabled on D0–D7 as controlled by the WRN, RDN and A0–A5 inputs. When CEN is High, the Octal UART is effectively isolated from the data bus and D0–D7 are placed in the 3-State condition.
WRN	17	19	I	**Write Strobe:** Active-Low input. A Low on this pin while CEN is Low causes the contents of the data bus to be transferred to the register selected by A0–A5. The transfer occurs on the trailing (rising) edge of the signal.
RDN	19	22	I	**Read Strobe:** Active-Low input. A Low on this pin while CEN is Low causes the contents of the register selected by A0–A5 to be placed on the data bus. The read cycle begins on the leading (falling) edge of RDN.
A0–A5	20–25	23, 25, 27, 29, 31, 32	I	**Address Inputs:** Active-High address inputs to select the Octal UART registers for read/write operations.
RESET	13	15	I	**Reset:** Master reset. A High on this pin clears the status register (SR), clears the interrupt mask register (IMR), clears the interrupt status register (ISR), clears the output port configuration register (OPCR), places the receiver and transmitter in the inactive state causing the TxD output to go to the marking (High) state, and stops the counter/timer. Clears power-down mode and interrupts. Clears Test Modes, sets MR pointer to MR1.
INTRAN– INTRDN	28, 29, 35, 36	35, 36, 46, 47	O	**Interrupt Request:** This active-Low open drain output is asserted on occurrence of one or more of eight maskable interrupting conditions. The CPU can read the interrupt status register to determine the interrupting condition(s).
X1/CLK	3	7	I	**Crystal 1:** Crystal or external clock input. When using the crystal oscillator, this pin serves as the connection for one side of the crystal. If a crystal is not used, an external clock is supplied at this input. An external clock (or crystal) is required even if the internal baud rate generator is not utilized. This clock is used to drive the internal baud rate generator, as an optional input to the timer/counter, and to provide other clocking signals required by the chip.
X2	2	6	I	**Crystal 2:** Connection for other side of crystal. If an external source is used instead of a crystal, this connection should be left open (see Figure 7).
RxDa–RxDh	64, 44, 62, 45, 60, 46, 57, 47	3, 56, 83, 57, 79, 58, 75, 59	I	**Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified, this input is sampled on the rising edge of the clock. If internal clock is used, the RxD input is sampled on the rising edge of the RxC1x signal as seen on the MPO pin.
TxDa–TxDh	63, 32, 61, 37, 56, 39, 55, 43	1, 41, 81, 49, 74, 52, 73, 55	O	**Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the marking (High) condition when the transmitter is idle or disabled and when the Octal UART is operating in local loopback mode. If external transmitter is specified, the data is shifted on the falling edge of the transmitter clock. If internal clock is used, the TxD output changes on the falling edge of the TxC1x signal as seen on the MPO pin.
MPOa–MPOh	54, 33, 53, 38, 52, 40, 51, 42	72, 43, 71, 51, 69, 53, 67, 54	O	**Multi-Purpose Output:** Each of the four DUARTS has two MPO pins. One of the following eight functions can be selected for this output pin by programming the OPCR (output port configuration register). Note that reset conditions MPO pins to RTSN. **RTSN** – Request to send active-Low output. This output is asserted and negated via the command register. By appropriate programming of the mode registers, (MR1[7])=1 RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted or when the receiver FIFO and shift register are full. RTSN is an internal signal which normally represents the condition of the receiver FIFO not full, i.e., the receiver can request more data to be sent. However, it can also be controlled by the transmitter empty and the commands 8h and 9h written to the CR (command register). **C/TO** – The counter/timer output. **TxC1X** – The 1X clock for the transmitter. **TxC16X** – The 16X clock for the transmitter. **RxC1X** – The 1X clock for the receiver. **RxC16X** – The 16X clock for the receiver. **TxRDY** – Transmitter holding register empty signal. **RxRDY/FFULL** – Receiver FIFO not empty/full signal.
MPI0a–MPI0h	26, 27, 30, 31, 48, 49, 58, 59	33, 34, 37, 39, 61, 63, 76, 77	I	**Multi-Purpose Input 0:** This pin (one in each UART) is programmable. Its state can always be read through the IPCR bit 0, or the IPR bit 0. **CTSN:** By programming MR2[4] to a 1, this input controls the clear-to-send function for the transmitter. It is active low. This pin is provided with a change-of-state detector.

PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
MPI1a–MPI1h	NC	14, 21, 38, 40, 60, 62, 78, 80	I	**Multi-Purpose Input 1:** This pin (one for each unit) is programmable. Its state can always be determined by reading the IPCR bit 1 or IPR bit 1. **C/TCLK** – This input will serve as the external clock for the counter/timer when ACR[5] is set to 0. This occurs only for channels a, c, e, and g since there is one counter/timer for each DUART block. This pin is provided with a change-of-state detector.
MPP1a–MPP1h	NC	24, 26, 42, 44, 64, 66, 82, 84	I/O	**Multi-Purpose Pin 1:** This pin (one for each UART) is programmed to be an input or an output according to the state of OPCR[7]. (0 = input, 1 = output). The state of the multi-purpose pin can always be determined by reading the IPR. When programmed as an input, it will be the transmitter clock (TxCLK). It will be 1x or 16x according to the clock select registers (CSR[3.0]). When programmed as an output, it will be the status register TxRDY bit. As an output, it will be an open drain, and thus requires a pull-up device.
MPP2a–MPP2h	NC	28, 30, 48, 50, 68, 70, 2, 4	I/O	**Multi-Purpose Pin 2:** This pin (one for each UART) is programmed to be an input or an output according to the state of OPCR[7]. (0 = input, 1 = output). The state of the multi-purpose pin can always be determined by reading the IPR. When programmed as an input, it will be the receiver clock (RxCLK). It will be 1x or 16x according to the clock select registers (CSR[7:4). When programmed as an output, it will be the ISR status register RxRDY/FIFO full bit. As an output, it will be an open drain, and thus requires a pull-up device.
Test Input	41	–	I	**Test Input:** This pin is used as an input for test purposes at the factory while in test mode. This pin can be treated as 'N/C' by the user. It can be tied high, or left open.
V_{CC}	1, 34	5, 45	I	**Power Supply:** +5V supply input.
GND	18, 50	20, 65	I	**Ground**

BLOCK DIAGRAM

As shown in the block diagram, the Octal UART consists of: data bus buffer, interrupt control, operation control, timing, and eight receiver and transmitter channels. The eight channels are divided into four different blocks, each block independent of each other (see Figure 1).

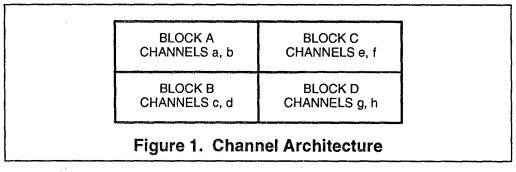


Figure 1. Channel Architecture

Channel Blocks

There are four blocks (Figure 1), each containing two sets of receiver/transmitters. In the following discussion, the description applies to Block A which contains channels a and b. However, the same information applies to all channel blocks.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data buses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the Octal UART.

Interrupt Control

A single interrupt output per block (INTRN) is provided which is asserted on occurrence of any of the following internal events:

–Transmit holding register ready for each channel

–Receive holding register ready or FIFO full for each channel

–Change in break received status for each channel

–Counter reached terminal count

–Change in MPI input

Associated with the interrupt system are the interrupt mask register (IMR) and the interrupt status register (ISR). The IMR can be programmed to select only certain conditions, of the above, to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. However, the bits of the ISR are not masked by the IMR. The transmitter ready status and the receiver ready or FIFO full status can be provided on MPP1a, MPP1b, MPP2a, and MPP2b by setting OPCR[7]. these outputs are not masked by IMR.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The functions performed by the CPU read and write operations are shown in Table 1.

Mode registers 1 and 2 are accessed via an auxiliary pointer. The pointer is set to MR1 by RESET or by issuing a reset pointer command via the command register. Any read or write of the mode register while the pointer is at MR1 switches the pointer to MR2. The pointer then remains at MR2 so that subsequent accesses are to MR2, unless the pointer is reset to MR1 as already described.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer for each block, and two clock selectors.

The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/ CLK and X2 inputs with a minimum of external components. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. If an external clock is used instead of a crystal, X1 must be driven and X2 left floating as shown in Figure 7. The clock serves as the basic timing reference for the baud rate generator (BRG), the counter/timer, and other internal circuits. A clock frequency, within the limits specified in the electrical specifications, must be supplied even if the internal BRG is not used.

Table 1. Register Addressing

Units A and B								Units E and F							
A5	A4	A3	A2	A1	A0	READ (RDN=0)	WRITE (WRN=0)	A5	A4	A3	A2	A1	A0	READ (RDN=0)	WRITE (WRN=0)
0	0	0	0	0	0	MR1a, MR2a	MR1a, MR2a	1	0	0	0	0	0	MR1e, MR2e	MR1e, MR2e
0	0	0	0	0	1	SRa	CSRa	1	0	0	0	0	1	SRe	CSRe
0	0	0	0	1	0	BRG Test	CRa	1	0	0	0	1	0	Reserved*	CRe
0	0	0	0	1	1	RHRa	THRa	1	0	0	0	1	1	RHRe	THRe
0	0	0	1	0	0	IPCRA	ACRA	1	0	0	1	0	0	IPCRC	ACRC
0	0	0	1	0	1	ISRA	IMRA	1	0	0	1	0	1	ISRC	IMRC
0	0	0	1	1	0	CTUA	CTURA	1	0	0	1	1	0	CTUC	CTURC
0	0	0	1	1	1	CTLA	CTLRA	1	0	0	1	1	1	CTLC	CTLRC
0	0	1	0	0	0	MR1b, MR2b	MR1b, MR2b	1	0	1	0	0	0	MR1f, MR2f	MR1f, MR2f
0	0	1	0	0	1	SRb	CSRb	1	0	1	0	0	1	SRf	CSRf
0	0	1	0	1	0	1X/16X Test	CRb	1	0	1	0	1	0	Reserved*	CRf
0	0	1	0	1	1	RHRb	THRb	1	0	1	0	1	1	RHRf	THRf
0	0	1	1	0	0	Reserved*	Reserved*	1	0	1	1	0	0	Reserved*	Reserved*
0	0	1	1	0	1	Input port A	OPCRA	1	0	1	1	0	1	Input port C	OPCRC
0	0	1	1	1	0	Start C/T A	Reserved*	1	0	1	1	1	0	Start C/T C	Reserved*
0	0	1	1	1	1	Stop C/T A	Reserved*	1	0	1	1	1	1	Stop C/T C	Reserved*
Units C and D								**Units G and H**							
0	1	0	0	0	0	MR1c, MR2c	MR1c, MR2c	1	1	0	0	0	0	MR1g, MR2g	MR1g, MR2g
0	1	0	0	0	1	SRc	CSRc	1	1	0	0	0	1	SRg	CSRg
0	1	0	0	1	0	Reserved*	CRc	1	1	0	0	1	0	Reserved*	CRg
0	1	0	0	1	1	RHRc	THRc	1	1	0	0	1	1	RHRg	THRg
0	1	0	1	0	0	IPCRB	ACRB	1	1	0	1	0	0	IPCRD	ACRD
0	1	0	1	0	1	ISRB	IMRB	1	1	0	1	0	1	ISRD	IMRD
0	1	0	1	1	0	CTUB	CTURB	1	1	0	1	1	0	CTUD	CTURD
0	1	0	1	1	1	CTLB	CTLRB	1	1	0	1	1	1	CTLD	CTLRD
0	1	1	0	0	0	MR1d, MR2d	MR1d, MR2d	1	1	1	0	0	0	MR1h, MR2h	MR1h, MR2h
0	1	1	0	0	1	SRd	CSRd	1	1	1	0	0	1	SRh	CSRh
0	1	1	0	1	0	Reserved*	CRd	1	1	1	0	1	0	Reserved*	CRh
0	1	1	0	1	1	RHRd	THRd	1	1	1	0	1	1	RHRh	THRh
0	1	1	1	0	0	Reserved*	Reserved*	1	1	1	1	0	0	Reserved*	Reserved*
0	1	1	1	0	1	Input port B	OPCRB	1	1	1	1	0	1	Input port D	OPCRD
0	1	1	1	1	0	Start C/T B	Reserved*	1	1	1	1	1	0	Start C/T D	Reserved*
0	1	1	1	1	1	Stop C/T B	Reserved*	1	1	1	1	1	1	Stop C/T D	Reserved*

NOTE:

1. Reserved registers should never be read during normal operation since they are reserved for internal diagnostics.

ACR = Auxiliary control register
CR = Command register
CSR = Clock select register
CTL = Counter/timer lower
CTLR = Counter/timer lower register
CTU = Counter/timer upper
CTUR = Counter/timer upper register
MR = Mode register
SR = Status Register
THR = Tx holding register
RHR = Rx holding register
IPCR = Input port change register
ISR = Interrupt status register
IMR = Interrupt mask register
OPCR = Output port configuration register

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. Thirteen of these are available simultaneously for use by the receiver and transmitter. Eight are fixed, and one of two sets of five can be selected by programming ACR[7]. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The clock selectors allow the independent selection, by the receiver and transmitter, of any of these baud rates or an external timing signal.

There are four C/Ts in the Octal UART, one for each block. The C/T operation is programmed by ACR[6:4]. One of eight timing sources can be used as the input to the C/T. The output of the C/T is available to the clock selectors and can also be programmed by OPCR[2:0] for channel a and OPCR[6:4] for channel b, to be output on the MPOa or MPOb pin respectively.

A register read address is reserved to issue a start counter/timer command and a second register read address is reserved to issue a stop counter/timer command for each timer. For example, to issue a stop counter command for the counter-timer in block B, a read of address '1F' must be performed. See Table 1 for register addressing.

In the timer mode, the C/T generates a square wave whose period is twice the number of clock periods loaded into the C/T upper and

lower registers. The counter ready bit in the ISR is set once each cycle of the square wave. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be affected. In this mode the C/T runs continuously and does not recognize the stop C/T command (the command only resets the counter ready bit in the ISR). Receipt of a start C/T command causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR. Counting begins upon receipt of a start counter command. Upon reaching terminal count, the counter ready bit in the ISR is set. The counter continues counting past the terminal count until stopped by the CPU. If MPO is programmed to be the output of the C/T, the output remains High until terminal count is reached, at which time it goes Low. The output returns to the High state and the counter ready bit is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command following a stop counter command. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower eight bits of the counter may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower eight bits to the upper eight bits occurs between the times that both halves of the counter are read. However, a subsequent start counter command causes the counter to begin a new count cycle using the values in CTUR and CTLR.

Receiver and Transmitter

The Octal UART has eight full-duplex asynchronous receiver/transmitters. The operating frequency for the receiver and transmitter can be selected independently from the baud rate generator, the counter/timer, or from an external input.

Registers associated with the communications channel are the mode registers (MR1 and MR2), the clock select register (CSR), the command register (CR), the status register (SR), the transmit holding register (THR), and the receive holding register (RHR).

Transmitter

The transmitter accepts parallel data from the CPU and converts it to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains high and the TxEMT bit in the SR will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character in the THR. In the 16X clock mode, this also re-synchronizes the internal 1X transmitter clock so that transmission of the new character begins with minimum delay.

The transmitter can be forced to send a break (continuous Low condition) by issuing a start break command via the CR. The break is terminated by a stop break command. If the transmitter is disabled, it continues operating until the characters currently being transmitted and the character in the THR, if any, are completely sent out. Characters cannot be loaded in the THR while the transmitter is disabled.

Receiver

The receiver accepts serial data on the RxD pin, converts the serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition, and presents the assembled character to the CPU. The receiver looks for a High-to-Low (mark-to-space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled again each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode).

If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again. If RxD is still Low, a valid start bit is assumed and the receiver samples the input. This continues at one bit time intervals, at the theoretical center of the bit, until the proper number of data bits and the parity bit (if any) have been assembled, and one stop bit has been detected. The data is then transferred to the RHR and the RxRDY bit in the SR is set to a one. If the character length is less than eight bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (i.e. framing error) and RxD remains low for one-half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled). The parity error, framing error and overrun error (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set.

If a break condition is detected (RxD is low for the entire character including the stop bit), only one character consisting of all zeros will be loaded in the FIFO and the received break bit in the SR is set to 1. The RxD input must return to a high condition for two successive clock edges of the 1X clock (internal or external) before a search for the next start bit begins.

TIMEOUT MODE

The timeout mode uses the received data stream to control the counter. Each time a received character is transferred from the shift register to the RHR, the counter is restarted. If a new character is not received before the counter reaches zero count, the counter ready bit is set, and an interrupt can be generated. This mode can be used to indicate when data has been left in the Rx FIFO for more than the programmed time limit. Otherwise, if the receiver has been programmed to interrupt the CPU when the receive FIFO is full, and the message ends before the FIFO is full, the CPU may not know when there is data left in the FIFO, The CTU and CTL value would be programmed for just over one character time, so that the CPU would be interrupted as soon as it has stopped receiving continuous data. This mode can also be used to indicate when the serial line has been marking for longer than the programmed time limit. In this case, the CPU has read all of the characters from the FIFO, but the last character received has started the count. If there is no new data during the programmed time interval, the counter ready bit will get set, and an interrupt can be generated.

This mode is enabled by writing the appropriate command to the command register. Writing an 'Ax' to CRA or CRB will invoke the timeout mode for that channel. Writing a 'Cx' to CRA or CRB will disable the timeout mode. The timeout mode should only be used by one channel at once, since it uses the C/T. CTU and CTL must be

loaded with a value greater than the normal receive character period. The timeout mode disables the regular START/STOP counter commands and puts the C/T into counter mode under the control of the received data stream. Each time a received character is transferred from the shift register to the RHR, the C/T is stopped after one C/T clock, reloaded with the value in CTU and CTL and then restarted on the next C/T clock. If the C/T is allowed to end the count before a new character has been received, the counter ready bit, ISR[3], will be set. If IMR[3] is set, this will generate an interrupt. Since receiving a character restarts the C/T, the receipt of a character after the C/T has timed out will clear the counter ready bit, ISR[3], and the interrupt. Invoking the 'Set Timeout Mode On' command, CRx='Ax', will also clear the counter ready bit and stop the counter until the next character is received.

RECEIVER FIFO

The RHR consists of a first-in-first-out (FIFO) with a capacity of three characters. Data is loaded from the receive shift register into the top-most empty position of the FIFO. The RxRDY bit in the status register (SR) is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR, outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are appended to each data character in the FIFO. Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical OR of the status for all characters coming to the top of the FIFO since the last reset error command was issued. In either mode, reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore, the SR should be read prior to reading the corresponding data character.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exists, the contents of the FIFO are not affected: the character previously in the shift register is lost and the overrun error status bit, SR[4], will be set upon receipt of the start bit of the new (overrunning) character.

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

Receiver Reset and Disable

Receiver disable stops the receiver immediately – data being assembled if the receiver shift register is lost. Data and status in the FIFO is preserved and may be read. A re-enable of the receiver after a disable will cause the receiver to begin assembling characters at the next start bit detected. A receiver reset will discard the present shift register date, reset the receiver ready bit (RxRDY), clear the status of the byte at the top of the FIFO and re-align the FIFO read/write pointers. This has the appearance of "clearing or flushing" the receiver FIFO. In fact, the FIFO is NEVER cleared! The data in the FIFO remains valid until overwritten by another received character. Because of this erroneous reading, the FIFO will miss-align the FIFO pointers and result in the reading of previously read data. A receiver reset will re-align the pointers.

WAKE-UP MODE

In addition to the normal transmitter and receiver operation described above, the Octal UART incorporates a special mode which provides automatic wake-up of the receiver through address frame recognition for multiprocessor communications. This mode is selected by programming bits MR1[4:3] to '11'.

In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, whose receivers are normally disabled, examine the received data stream and 'wake-up' the CPU [by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, an address/data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1[2]; MR1[2] = 0 transmits a zero in the A/D bit position which identifies the corresponding data bits as data; MR1[2] = 1 transmits a one in the A/D bit position which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits in the THR.

While in this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character in the RHR FIFO if the received A/D bit is a one, but discards the received character if the received A/D bit is a zero. If enabled, all received characters are then transferred to the CPU via the RHR. In either case, the data bits are loaded in the data FIFO while the A/D bit is loaded in the status FIFO position normally used for parity error (SR[5]). Framing error, overrun error, and break detect operate normally whether or not the receiver is enabled.

MULTI-PURPOSE INPUT PIN AND MULTI-PURPOSE I/O PINS

The inputs to this unlatched 8-bit port for each block can be read by the CPU, by performing a read operation as shown in Table 1. A High input results in a logic one, while a Low input results in a logic zero. When the input port pins are read on the 84-pin LLCC, they will appear on the data bus in alternating pairs (i.e., DB0 = MP10a, DB1 = MPI1a, DB2 = MPI0b, DB3 = MPI1b, DB4 = MPP1a, DB5 = MPP2a, DB6 = MPP1b, DB7 = MPP2b. Although this example is shown for input port 'A', all ports will have a similar order).

The MPI pin can be programmed as an input to one of several Octal UART circuits. The function of the pin is selected by programming the appropriate control register. Change-of-state detectors are provided for MPI0 and MPI1 for each channel in each block. A High-to-Low or Low-to-High transition of the inputs lasting longer than 25 to 50µs sets the MPI change-of-state bit in the interrupt status register. The bit is cleared via a command. The change-of-state can be programmed to generate an interrupt to the CPU by setting the corresponding bit in the interrupt mask register.

The input port pulse detection circuitry uses a 38.4KHz sampling clock, derived from one of the baud rate generator taps. This produces a sampling period of slightly more than 25µs (assuming a 3.6864MHz oscillator input). The detection circuitry, in order to guarantee that a true change in level has occurred, requires two successive samples be observed at the new logic level. As a consequence, the minimum duration of the signal change is 25µs if the transition occurs coincident with the first sample pulse. (The 50µs time refers to the condition where the change-of-state is just missed and the first change of state is not detected until after an additional 25µs.)

The multi-purpose pins can be programmed as inputs or outputs using OPCR[7]. When programmed as inputs, the functions of the pins are selected by programming the appropriate control registers. When programmed as outputs, the two MPP1 pins (per block) will provide the transmitter ready (TxRDY) status for each channel and the MPP2 pins will provide the receiver ready or FIFO full (RxRDY/FFULL) status for each channel.

MULTI-PURPOSE OUTPUT PIN

This pin can be programmed to serve as a request-to-send output, the counter/timer output, the output for the 1X or 16X transmitter or receiver clocks, the TxRDY output or the RxRDY/FFULL output (see OPCR [2:0] and OPCR [6:4] – MPO Output Select).

REGISTERS

The operation of the Octal UART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. Addressing of the registers is described in Table 1.

The bit formats of the Octal UART registers are depicted in Table 2. These are shown for block A. The bit format for the other blocks is the same.

MR1 – Mode Register 1

MR1 is accessed when the MR pointer points to MR1. The pointer is set to MR1 by RESET or by a set pointer command applied via the CR. After reading or writing MR1, the pointers are set at MR2.

MR1[7] – Receiver Request-to-Send Control
This bit controls the deactivation of the RTSN output (MPO) by the receiver. This output is manually asserted and negated by commands applied via the command register. MR1[7] = 1 causes RTSN to be automatically negated upon receipt of a valid start bit if the receiver FIFO is full. RTSN is reasserted when an empty FIFO position is available. This feature can be used to prevent overrun in the receiver by using the RTSN output signal to control the CTS input of the transmitting device.

MR1[6] – Receiver Interrupt Select
This bit selects either the receiver ready status (RxRDY) or the FIFO full status (FFULL) to be used for CPU interrupts.

MR1[5] – Error Mode Select
This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break). In the character mode, status is provided on a character-by-character basis; the status applies only to the character at the top of the FIFO. In the block mode, the status provided in the SR for these bits is the accumulation (logical-OR) of the status for all characters coming to the top of the FIFO since the last reset error command was issued.

MR1[4:3] – Parity Mode Select
If 'with parity' or 'force parity' is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR1[4:3] = 11 selects the channel to operate in the special wake-up mode.

MR1[2] – Parity Type Select
This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special 'wake-up' mode, it selects the polarity of the transmitted A/D bit.

MR1[1:0] – Bits Per Character Select
This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2 – Mode Register 2

MR2 is accessed when the channel MR pointer points to MR2, which occurs after any access to MR1. Accesses to MR2 do not change the pointer.

MR2[7:6] – Mode Select
The Octal UART can operate in one of four modes. MR2[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2[7:6] = 01 places the channel in the automatic echo mode, which automatically re-transmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is re-clocked and retransmitted on the TxD output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU-to-receiver communication continues normally, but the CPU-to-transmitter link is disabled.

Two diagnostic modes can also be selected. MR2[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxD output is held high.
4. The RxD input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2[7:6] = 11. In this mode:

1. Received data is re-clocked and retransmitted on the TXD output.
2. The receive clock is used for the transmitter.
3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., the transmitted parity bit is as received.

5. The receiver must be enabled, but the transmitter need not be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected, the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes; if the deselection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop bit has been retransmitted.

Table 2. Register Bit Formats

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

MR1 (Mode Register 1)

RxRTS Control	RxINT Select	Error Mode	Parity Mode	Parity Type	Bits per Character
0 = No	0 = RxRDY	0 = Char	00 = With parity	0 = Even	00 = 5
1 = Yes	1 = FFULL	1 = Block	01 = Force parity	1 = Odd	01 = 6
			10 = No parity		10 = 7
			11 = Special mode		11 = 8

MR2 (Mode Register 2)

Channel Mode	TxRTS Control	CTS Enable Tx	Stop Bit Length*			
00 = Normal			0 = 0.563	4 = 0.813	8 = 1.563	C = 1.813
01 = Auto-echo	0 = No	0 = No	1 = 0.625	5 = 0.875	9 = 1.625	C = 1.875
10 = Local loop	1 = Yes	1 = Yes	2 = 0.688	6 = 0.938	A = 1.688	E = 1.938
11 = Remote loop			3 = 0.750	7 = 1.000	B = 1.750	F = 2.000

NOTE: *Add 0.5 to values shown above for 0–7, if channel is programmed for 5 bits/char.

CSR (Clock Select Register)

Receiver Clock Select	Transmitter Clock Select
See text	See text

CR (Command Register)

Miscellaneous Commands	Disable Tx	Enable Tx	Disable Rx	Enable Rx
See text	0 = No	0 = No	0 = No	0 = No
	1 = Yes	1 = Yes	1 = Yes	1 = Yes

NOTE: Access to the upper four bits of the command register should be separated by three (3) edges of the X1 clock. A disabled transmitter cannot be loaded

SR (Status Register)

Rec'd Break*	Framing Error*	Parity Error*	Overrun Error	TxEMT	TxRDY	FFULL	RxRDY
0 = No	0 = No	0 = No	0 = No	0 = No	0 = No	0 = No	0 = No
1 = Yes	1 = Yes	1 = Yes	1 = Yes	1 = Yes	1 = Yes	1 = Yes	1 = Yes

NOTE: *These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits [7:5] from the top of the FIFO together with bits [4:0]. These bits are cleared by a reset error status command. In character mode, they must be reset when the corresponding data character is read from the FIFO.

Table 2. Register Bit Formats (Continued)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

OPCR (Output Port Configuration Register)

MPP Function Select	MPOb Pin Function Select	Power-Down Mode*	MPOa Pin Function Select
0 = input	000 = RTSN	0 = Off	000 = RTSN
1 = output	001 = C/TO	1 = On	001 = C/TO
	010 = TxC (1X)		010 = TxC (1X)
	011 = TxC (16X)		011 = TxC (16X)
	100 = RxC (1X)		100 = RxC (1X)
	101 = RxC (16X)		101 = RxC (16X)
	110 = TxRDY		110 = TxRDY
	111 = RxRDY/FF		111 = RxRDY/FF
NOTE: *Only OPCR[3] in block A controls the power-down mode.			

ACR (Auxiliary Control Register)

BRG Select	Counter/Timer Mode and Source	Delta MPI1bINT	Delta MPI0bINT	Delta MPI1aINT	Delta MPI0aINT
0 = set 1 1 = set 2	See Text	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

IPCR (Input Port Change Register)

Delta MPI1b	Delta MPI0b	Delta MPI1a	Delta MPI0a	MPI1b	MPI0b	MPI1a	MPI0a
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

ISR (Interrupt Status Register)

MPI Port Change	Delta BREAKb	RxRDY/ FFULLb	TxRDYb	Counter Ready	Delta BREAKa	RxRDY/ FFULLa	TxRDYa
0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes

IMR (Interrupt Mask Register)

MPI Port Change INT	Delta BREAKb INT	RxRDY/ FFULLb INT	TxRDYb INT	Counter Ready INT	Delta BREAKa INT	RxRDY/ FFULLa INT	TxRDYa INT
0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

CTUR (Counter/Timer Upper Register)

C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]

CTUR (Counter/Timer Lower Register)

C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]

IPR (Input Port Register) MPP and MPI Pins

MPP2b	MPP1b	MPP2a	MPP1a	MPI1b	MPI0b	MPI1a	MPI0a
0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High	0 = Low 1 = High

NOTE: When TxEMT and TxRDY bits are at one just before a write to the Transmit Holding register, a command to disable the transmitter should be delayed until the TxRDY is at one again. TxRDY will set to one at the end of the start bit time.

MR2[5] – Transmitter Request-to-Send Control

CAUTION: When the transmitter controls the OP pin (usually used for the RTSN signal) the meaning of the pin is not RTSN at all! Rather, it signals that the transmitter has finished the transmission (i.e., end of block).

This bit allows deactivation of the RTSN output by the transmitter. This output is manually asserted and negated by the appropriate commands issued via the command register. MR2[5] set to 1 caused the RTSN to be reset automatically one bit time after the character(s) in the transmit shift register and in the THR (if any) are

completely transmitted (including the programmed number of stop bits) if a previously issued transmitter disable is pending. This feature can be used to automatically terminate the transmission as follows:

1. Program the auto-reset mode: MR2[5]=1
2. Enable transmitter, if not already enabled
3. Assert RTSN via command
4. Send message
5. After the last character of the message is loaded to the THR, disable the transmitter. (If the transmitter is underrun, a special case exists. See note below.)
6. The last character will be transmitted and the RTSN will be reset one bit time after the last stop bit is sent.

NOTE: The transmitter is in an underrun condition when both the TxRDY and the TxEMT bits are set. This condition also exists immediately after the transmitter is enabled from the disabled or reset state. When using the above procedure with the transmitter in the underrun condition, the issuing of the transmitter disable must be delayed from the loading of a single, or last, character until the TxRDY becomes active again after the character is loaded.

MR2[4] – Clear-to-Send Control
The sate of this bit determines if the CTSN input (MPI) controls the operation of the transmitter. If this bit is 0, CTSN has no effect on the transmitter. If this bit is a 1, the transmitter checks the sate of CTSN each time it is ready to send a character. If it is asserted (Low), the character is transmitted. If it is negated (High), the TxD output remains in the marking state and the transmission is delayed until CTSN goes Low. Changes in CTSN, while a character is being transmitted do not affect the transmission of that character. This feature can be used to prevent overrun of a remote receiver.

MR2[3:0] – Stop Bit Length Select
This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1–9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1–1/16 to 2 stop bits can be programmed in increments of 1/16 bit. In all cases, the receiver only checks for a mark condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit if parity is enabled). If an external 1X clock is used for the transmitter, MR2[3] = 0 selects one stop bit and MR2[3] = 1 selects two stop bits to be transmitted.

CSR – Clock Select Register

Table 3. Baud Rate

CSR[7:4]	ACR[7] = 0	ACR[7] = 1
0 0 0 0	50	75
0 0 0 1	110	110
0 0 1 0	134.5	38.4k
0 0 1 1	200	150
0 1 0 0	300	300
0 1 0 1	600	600
0 1 1 0	1,200	1,200
0 1 1 1	1,050	2,000
1 0 0 0	2,400	2,400
1 0 0 1	4,800	4,800
1 0 1 0	7,200	1,800
1 0 1 1	9,600	9,600
1 1 0 0	38.4k	19.2k
1 1 0 1	Timer	Timer
1 1 1 0	MP2 – 16X	MP2 – 16X
1 1 1 1	MP2 – 1X	MP2 – 1X

The receiver clock is always a 16X clock, except for CSR[7:4] = 1111. When MPP2 is selected as the input, MPP2a is for channel a and MPP2b is for channel b. See Table 5.

CSR[7:4] – Receiver Clock Select
When using a 3.6864MHz crystal or external clock input, this field selects the baud rate clock for the receiver as shown in Table 3.

CSR[3:0] – Transmitter Clock Select
This field selects the baud rate clock for the transmitter. The field definition is as shown in Table 3, except as follows:

CSR[3:0]	ACR[7] = 0	ACR[7] = 1
1 1 1 0	MPP1 – 16X	MPP1 – 16X
1 1 1 1	MPP1 – 1X	MPP1 – 1X

When MPP1 is selected as the input, MPP1a is for channel a and MPP1b is for channel b.

CR – Command Register

CR is used to write commands to the Octal UART.

CR[7:4] – Miscellaneous Commands
The encoded value of this field can be used to specify a single command as follows:

NOTE: Access to the upper four bits of the command register should be separated by three (3) edges of the X1 clock.

0000	No command.
0001	Reset MR pointer. Causes the MR pointer to point to MR1.
0010	Reset receiver. Resets the receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO pointer is reset to the first location.
0011	Reset transmitter. Resets the transmitter as if a hardware reset had been applied.
0100	Reset error status. Clears the received break, parity error, framing error, and overrun error bits in the status register (SR[7:4]). Used in character mode to clear OE status (although RB, PE, and FE bits will also be cleared), and in block mode to clear all error status after a block of data has been received.
0101	Reset break change interrupt. Causes the break detect change bit in the interrupt status register (ISR[2 or 6]) to be cleared to zero.
0110	Start break. Forces the TxD output low (spacing). If the transmitter is empty, the start of the break condition will be delayed up to two bit times. If the transmitter is active, the break begins when transmission of the character is completed. If a character is in the THR, the start of break is delayed until that character or any others loaded after it have been transmitted (TxEMT must be true before break begins). The transmitter must be enabled to start a break
0111	Stop break. The TxD line will go high (marking) within two bit times. TxD will remain high for one bit time before the next character, if any, is transmitted.
1000	Assert RTSN. Causes the RTSN output to be asserted (Low).
1001	Negate RTSN. Causes the RTSN output to be negated (High).
1010	Set Timeout Mode On. The register in this channel will restart the C/T as each receive character is transferred from the shift register to the RHR. The C/T is placed in the counter mode, the START/STOP counter commands are disabled, the counter is stopped, and the Counter Ready Bit, ISR[3], is reset.
1011	Reserved.

1100 Disable Timeout Mode. This command returns control of the C/T to the regular START/STOP counter commands. It does not stop the counter, or clear any pending interrupts. After disabling the timeout mode, a 'Stop Counter' command should be issued.

1101 Reserved.

111x Reserved for testing.

CR[3] – Disable Transmitter
This command terminates transmitter operation and resets the TxRDY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CR[2] – Enable Transmitter
Enables operation of the transmitter. The TxRDY status bit will be asserted.

CR[1] – Disable Receiver
This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special wake–up mode is programmed, the receiver operates even if it is disabled (see Wake-up Mode).

CR[0] – Enable Receiver
Enables operation of the receiver. If not in the special wake-up mode, this also forces the receiver into the search for start bit state.

SR – Channel Status Register

SR[7] – Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received; further entries to the FIFO are inhibited until the RxDA line returns to the marking state for at least one-half bit time (two successive edges of the internal or external 1x clock).

When this bit is set, the change in break bit in the ISR (ISR[6 or 2]) is set. ISR[6 or 2] is also set when the end of the break condition, as defined above, is detected. The break detect circuitry is capable of detecting breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must last until the end of the next character in order for it to be detected.

SR[6] – Framing Error (FE)
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SR[5]– Parity Error (PE)
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity. In special 'wake-up mode', the parity error bit stores the received A/D bit.

SR[4] – Overrun Error (OE)
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a reset error status command.

SR[3] – Transmitter Empty (TxEMT)
This bit will be set when the transmitter underruns, i.e., both the transmit holding register and the transmit shift register are empty. It is set after transmission of the last stop bit of a character, If no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU, or when the transmitter is disabled.

SR[2] – Transmitter Ready (TxRDY)
This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, e.g., characters loaded in the THR while the transmitter is disabled will not be transmitted.

SR[1] – FIFO Full (FFULL)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the FIFO and there is no character in the receive shift register. If a character is waiting in the receive shift register because the FIFO is full, FFULL is not reset after reading the FIFO once.

SR[0] – Receiver Ready (RxRDY)
This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR, and no more characters are in the FIFO.

OPCR – Output Port Configuration Register

OPCR[7] – MPP Function Select
When this bit is a zero, the MPP pins function as inputs, to be used as general purpose inputs or as receiver or transmitter external clock inputs. When this bit is set, the MPP pins function as outputs. MPP1 will be a TxRDY indicator, and MPP2 will be an RxRDY/FFULL indicator.

OPCR[6:4] – MPOb Output Select
This field programs the MPOb output pin to provide one of the following:

000 Request-to-send active-Low output (RTSN). This output is asserted and negated via the command register. Mode RTSN can be programmed to be automatically reset after the character in the transmitter is completely shifted out or when the receiver FIFO and receiver shift register are full using MR2[5] and MR1[7], respectively.

001 The counter/timer output. In the timer mode, this output is a square wave with a period of twice the value (in clock periods) of the contents of the CTUR and CTLR. In the counter mode, the output remains high until the terminal count is reached, at which time it goes low. The output returns to the High state when the counter is stopped by a stop counter command.

010 The 1X clock for the transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a non-synchronized 1X clock is output.

011 The 16X clock for the transmitter. This is the clock selected by CSR[3:0], and is a 1X clock if CSR[3:0] = 1111.

100 The 1X clock for the receiver, which is the clock that samples the received data. If data is not being received, a non-synchronized 1X clock is output.

101 The 16X clock for the receiver. This is the clock selected by CSR[7:4], and is a 1X clock if CSR[7:4] = 1111.

110 The transmitter register ready signal, which is the same as SR[2].

111 The receiver ready or FIFO full signal.

OPCR[3] – Power Down Mode Select
This bit, when set, selects the power-down mode. In this mode, the 2698B oscillator is stopped and all functions requiring this clock are suspended. The contents of all registers are saved. It is recommended that the transmitter and receiver be disabled prior to placing the 2698B in this mode. This bit is reset with RESET asserted. Note that this bit must be set to a logic 1 after power up. Only OPCR[3] in block A controls the power-down mode.

OPCR[2:0] – MPOa Output Select
This field programs the MPOa output pin to provide one of the same functions as described in OPCR[6:4].

ACR – Auxiliary Control Register

ACR[7] – Baud Rate Generator Set Select
This bit selects one of two sets of baud rates generated by the BRG.

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05k, 1.2k, 2.4k, 4.8k, 7.2k, 9.6k, and 38.4k baud.

Set 2: 75, 110, 150, 300, 600, 1.2k, 1.8k, 2.0k, 2.4k, 4.8k, 9.6k, 19.2k, and 38.4k baud.

The selected set of rates is available for use by the receiver and transmitter.

ACR[6:4] – Counter/Timer Mode and Clock Source Select
This field selects the operating mode of the counter/timer and its clock source (see Table 4).

The MPI1 pin available as the Counter/Timer clock source is MPI1 a,c,e, and g only.

Table 4. ACR[6:4] Operating Mode

[6:4]	Mode	Clock Source
0 0 0	Counter	MPI1a pin
0 0 1	Counter	MPI1a pin divided by 16
0 1 0	Counter	TxC–1XA clock of the transmitter
0 1 1	Counter	Crystal or MPI pin (X1/CLK) divided by 16
1 0 0	Timer	MPI1a pin
1 0 1	Timer	MPI1a pin divided by 16
1 1 0	Timer	Crystal or external clock (X1/CLK)
1 1 1	Timer	Crystal or MPI pin (X1/CLK) divided by 16
NOTE: The timer mode generates a squarewave.		

ACR[3:0] – MPI1b, MPI0b, MPI1a, MPI0a Change-of-State Interrupt Enable
This field selects which bits of the input port change register (IPCR) cause the input change bit in the interrupt status register, ISR[7], to be set. If a bit is in the 'on' state, the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

IPCR – Input Port Change Register

IPCR[7:4] – MPI1b, MPI0b, MPI1a, MPI0a Change-of-State
These bits are set when a change of state, as defined in the Input Port section of this data sheet, occurs at the respective pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] – MPI1b, MPI0b, MPI1a, MPI0a Change-of-State
These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the inputs pins during the time the IPCR is read.

ISR – Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the interrupt mask register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output is asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR; the true status is provided regardless of the contents of the IMR.

ISR[7] – MPI Change-of-State
This bit is set when a change-of-state occurs at the MPI1b, MPI0b, MPI1a, MPI0a input pins. It is reset when the CPU reads the IPCR.

ISR[6] – Channel b Change in Break
This bit, when set, indicates that the receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a reset break change interrupt command.

ISR[5] – Receiver Ready or FIFO Full Channel b
The function of this bit is programmed by MR1[6]. If programmed as receiver ready, it indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receiver FIFO. If the FIFO contains more characters, the bit will be set again after the FIFO is read.

If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when FIFO is read and there is no character in the receiver shift register. If there is a character waiting in the receive shift register because the FIFO is full, the bit is set again when the waiting character is transferred into the FIFO.

ISR[4] – Transmitter Ready Channel b
This bit is a duplicate of TxRDY (SR[2]).

ISR[3] – Counter Ready
In the counter mode of operation, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command. It is initialized to '0' when the chip is reset.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time the C/T reaches zero count). The bit

is reset by a stop counter command. The command, however, does not stop the C/T.

ISR[2] – Channel a Change in Break
This bit, when set, indicates that the receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a reset break change interrupt command.

ISR[1] – Receiver Ready or FIFO Full Channel a
The function of this bit is programmed by MR1[6]. If programmed as receiver ready, it indicates that a character has been received and is waiting in the FIFO to be ready by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the receiver FIFO. If the FIFO contains more characters, the bit will be set again after the FIFO is read. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when FIFO is read and there is no character in the receiver shift register. If there is a character waiting in the receive shift register because the FIFO is full, the bit is set again when the waiting character is transferred into the FIFO.

ISR[0] – Transmitter Ready Channel a
This bit is a duplicate of TxRDY (SR[2]).

IMR – Interrupt Mask Register

The programming of this register selects which bits in the ISR cause an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is a '1', the INTRN output is asserted (Low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask reading of the ISR.

CTUR and CTLR – Counter/Timer Registers

The CTUR and CTLR hold the eight MSBs and eight LSBs, respectively, of the value to be used by the counter/timer in either the counter or timer modes of operation. The minimum value which may be loaded into the CTUR/CTLR registers is H'0002'. Note that these registers are write-only and cannot be read by the CPU.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. The waveform so generated is often used for a data clock. The formula for calculating the divisor n to load to the CTUR and CTLR for a particular 1X data clock is shown below:

$$n = \frac{\text{C/T Clock Frequency}}{2 \times 16 \times \text{Baud rate desired}}$$

Often this division will result in a non-integer number; 26.3, for example. One can only program integer numbers in a digital divider. Therefore, 26 would be chosen. This gives a baud rate error of 0.3/26.3 which is 1.14%; well within the ability asynchronous mode of operation.

If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half-periods will be. The C/T will not be running until it receives an initial 'Start Counter' command (read at address A3–A0 = 1110). After this, while in timer mode, the C/T will run continuously. Receipt of a subsequent start counter command causes the C/T to terminate the current timing cycle and to begin a new cycle using the values in the CTUR and CTLR.

The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command read with A3–A0 = H'F'). The command, however, does not stop the C/T. The generated square wave is output on MPO if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded in CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching the terminal count H'0000', the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If MPO is programmed to be the output of the C/T, the output remains High until the terminal count is reached, at which time it goes Low. The output returns to the High state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower eight bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower eight bits to the upper eight bits occurs between the times that both halves of the counter is read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

DC ELECTRICAL CHARACTERISTICS[1, 2, 3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL} V_{IH} V_{IH}	Input low voltage Input high voltage (except X1/CLK) Input high voltage (X1/CLK)		 2.0 $0.8V_{CC}$		 0.8	V V V
V_{OL} V_{OH}	Output Low voltage Output High voltage (except OD outputs)	I_{OL} = 2.4mA I_{OH} = −400µA I_{OH} = −100µA	 $0.8V_{CC}$ $0.9V_{CC}$		0.4	V V V
I_{IL} I_{IH}	Input current Low, MPI and MPP pins Input current High, MPI and MPP pins	V_{IN} = 0 V_{IN} = V_{CC}	−50		20	µA µA
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	−10		10	µA
I_{ILX1} I_{IHX1}	X1/CLK input Low current X1/CLK input High current	V_{IN} = GND, X2 = open V_{IN} = V_{CC}, X2 = open	−100		 100	µA µA
I_{OZH} I_{OZL}	Output off current High, 3-State data bus Output off current Low, 3-State data bus	V_{IN} = V_{CC} V_{IN} = 0	−10		10	µA
I_{ODL} I_{ODH}	Open-drain output Low current in off state: IRQN Open-drain output Low current in off state: IRQN	V_{IN} = V_{CC} V_{IN} = 0	−10		 10	µA
I_{CC}	Power supply current Operating mode				30	mA
	Power down mode[9]				2.0	mA

NOTES:
1. Parameters are valid over specified temperature range. See ordering information table for applicable temperature range and operating supply range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK this swing is between 0.4V and 4.4V. All time measurements are referenced at input voltages of V_{IL} and V_{IH}, as appropriate.
3. Typical values are at +25°C, typical supply voltages, and typical processing parameters.
4. Test condition for interrupt and MPP outputs: C_L = 50pF, R_L = 2.7kΩ to V_{CC}. Test conditions for rest of outputs: C_L = 150pF.
5. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.
6. If CEN is used as the 'strobing' input, the parameter defines the minimum high times between one CEN and the next. The RDN signal must be negated for t_{RWD} guarantee that any status register changes are valid.
7. Consecutive write operations to the command register require at least three edges of the X1 clock between writes.
8. This value is not tested, but is guaranteed by design.
9. See UART applications note for power down currents less than 5µA.
10. Operation to 0MHz is assured by design. Minimum test frequency is 2MHz.

AC Electrical characteristics[1, 2, 3, 4]

SYMBOL	FIGURE	PARAMETER	LIMITS			UNIT
			Min	Typ	Max	
Reset timing						
t_{RES}	2	Reset pulse width	200			ns
Bus timing[5]						
t_{HS}	3	A0–A5 setup time to RDN, WRN Low	10			ns
t_{AH}	3	A0–A5 hold time from RDN, WRN Low	100			ns
t_{CS}[6]	3	CEN setup time to RDN, WRN Low	0			ns
t_{CH}[6]	3	CEN hold time from RDN, WRN High	0			ns
t_{RW}	3	WRN, RDN pulse width Low	225			ns
t_{DD}	3	Data valid after RDN Low			200	ns
t_{DF}	3	Data bus floating after RDN High			80	ns
t_{DS}	3	Data setup time before WRN High	100			ns
t_{DH}	3	Data hold time after WRN High	10			ns
t_{RWD}[7]		Time between reads and/or writes	100			ns
MPI and MPO timing[5]						
t_{PS}	4	MPI or MPP input setup time before RDN Low	0			ns
t_{PH}	4	MPI or MPP input hold time after RDN High	0			ns
t_{PD}	4	MPO output valid from WRN High RDN Low			 250 250	 ns ns
Interrupt timing						
t_{IR}	5	INTRN negated or MPP output High from: Read RHR (RxRDY/FFULL interrupt) Write THR (TxRDY interrupt) Reset command (break change interrupt) Reset command (MPI change interrupt) Stop C/T command (counter interrupt) Write IMR (clear of interrupt mask bit)			 270 270 270 270 270 270	 ns ns ns ns ns ns
Clock timing						
t_{CLK}	6	X1/CLK high or low time	120			ns
t_{CLK}	6	X1/CLK frequency[10]	0	3.6864	4.0	MHz
t_{CTC}	6	Counter/timer clock high or low time	120			ns
f_{CTC}	6	Counter/timer clock frequency	0[8]		4.0	MHz
t_{RX}	6	RxC high or low time	200			ns
f_{RX}	6	RxC frequency (16X) RxC frequency (1X)	0[8] 0[8]		2.0 1.0	MHz MHz
t_{TX}	6	TxC high or low time	200			ns
f_{TX}	6	TxC frequency (16X) TxC frequency (1X)	0[8] 0[8]		2.0 1.0	MHz MHz
Transmitter timing						
t_{TXD}	7	TxD output delay from TxC low			350	ns
t_{TCS}	7	TxC output delay from TxD output data	0		150	ns
Receiver timing						
t_{RXS}	8	RxD data setup time to RxC high	50			ns
t_{RXH}	8	RxD data hold time from RxC high	100			ns

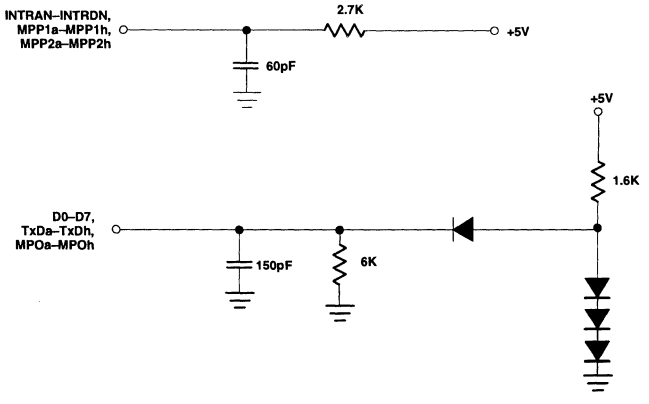


Figure 1. Test Conditions on Outputs

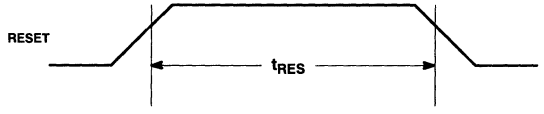


Figure 2. Reset Timing

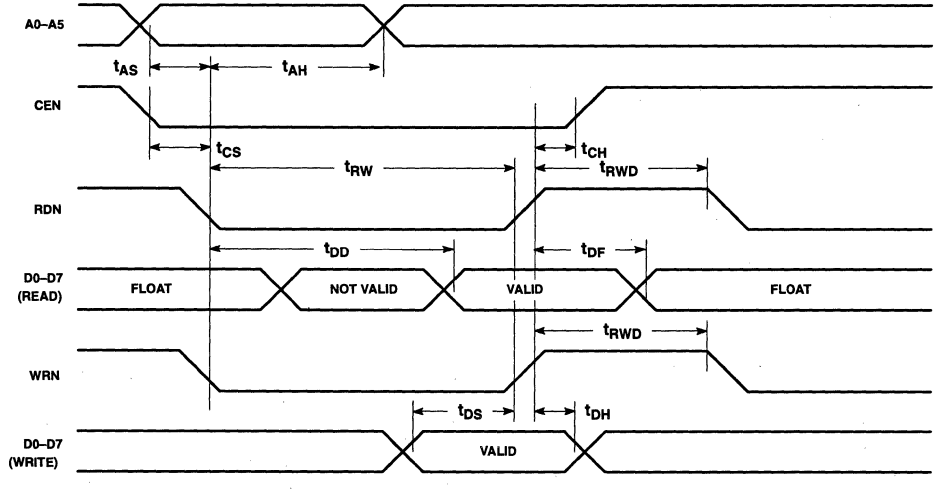


Figure 3. Bus Timing

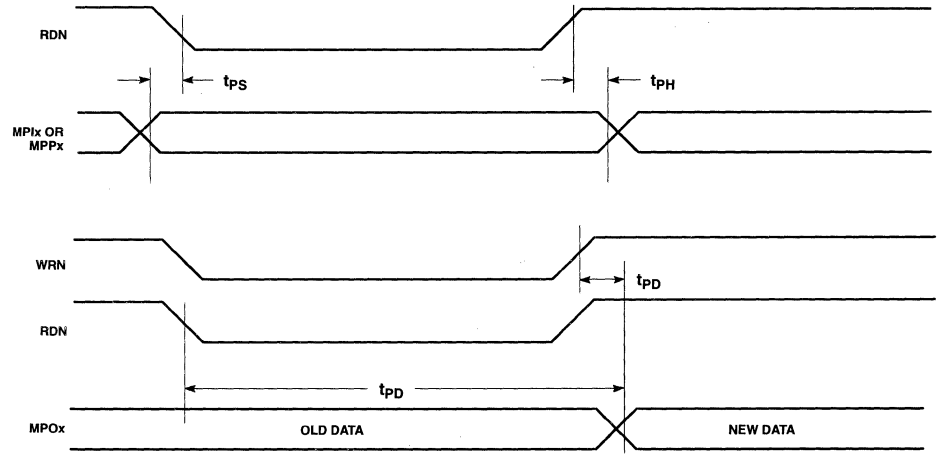
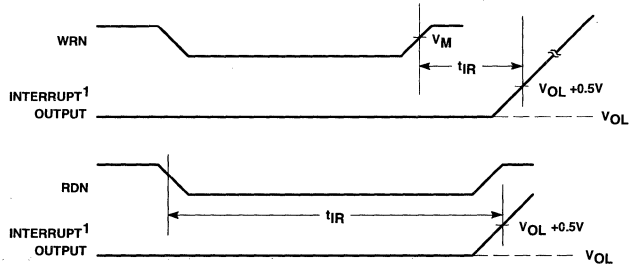


Figure 4. Port Timing



NOTES:
1. INCLUDES MPP WHEN USED AS TxRDY or RxDY/FFULL OUTPUTS AS WELL AS INTRN.
2. THE TEST FOR OPEN DRAIN OUTPUTS IS INTENDED TO GUARANTEE SWITCHING OF THE OUTPUT TRANSISTOR. MEASUREMENT OF THIS RESPONSE IS REFERENCED FROM THE MIDPOINT OF THE SWITCHING SIGNAL, V_M, TO A POINT 0.5V ABOVE V_{OL}. THIS POINT REPRESENTS NOISE MARGIN THAT ASSURES TRUE SWITCHING HAS OCCURRED. BEYOND THIS LEVEL, THE EFFECTS OF EXTERNAL CIRCUITRY AND TEST ENVIRONMENT ARE PRONOUNCED AND CAN GREATLY AFFECT THE RESULTANT MEASUREMENT.

Figure 5. Interrupt Timing

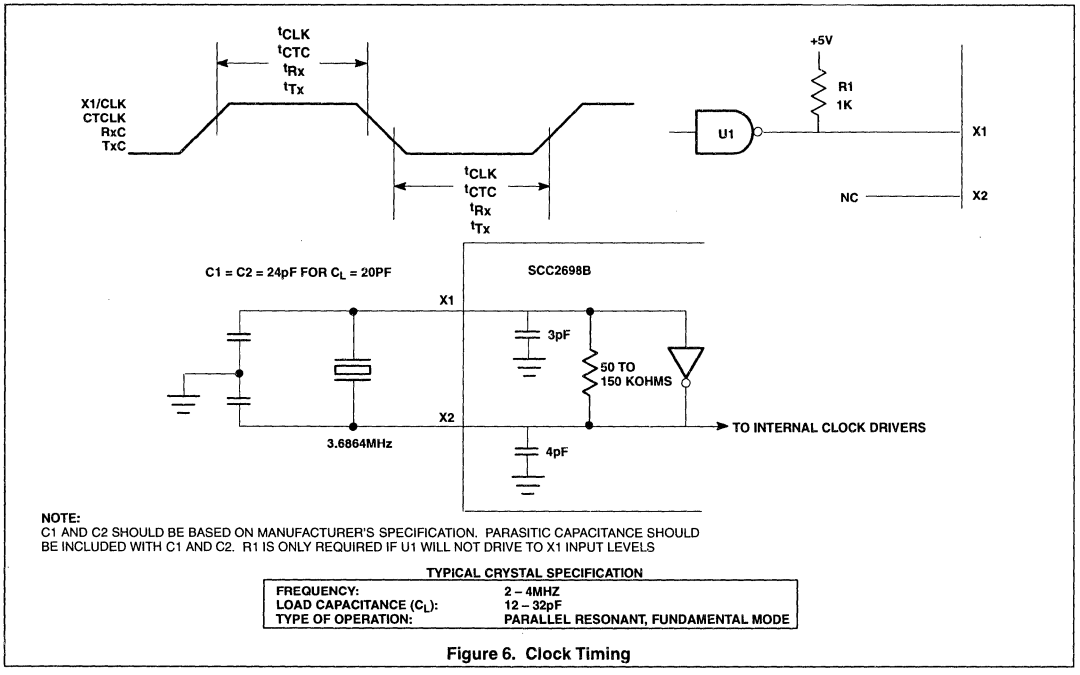
The CTS, RTS, CTS Enable Tx signals

CTS (Clear To Send) is usually meant to be a signal to the transmitter meaning that it may transmit data to the receiver. The CTS input is on pin MPI. The CTS signal is active low; thus, it is called CTS.

RTS is usually meant to be a signal from the receiver indicating that the receiver is ready to receive data. It is also active low and is, thus, called RTSN. RTSN is on pin MP0. A receiver's RTS output will usually be connected to the CTS input of the associated transmitter. Therefore, one could say that RTS and CTS are different ends of the same wire!

MR2(4) is the bit that allows the transmitter to be controlled by the CTS pin (MPI). When this bit is set to one AND the CTS input is driven high, the transmitter will stop sending data at the end of the present character being serialized. It is usually the RTS output of the receiver that will be connected to the transmitter's CTS input. The receiver will set RTS high when the receiver FIFO is full AND the start bit of the fourth character is sensed. Transmission then stops with four valid characters in the receiver. When MR2(4) is set to one, CTSN must be at zero for the transmitter to operate. If MR2(4) is set to zero, the MP pin will have no effect on the operation of the transmitter.

MR1(7) is the bit that allows the receiver to control MP0. When MP0 is controlled by the receiver, the meaning of that pin will be RTS. However, a point of confusion arises in that MP0 may also be controlled by the transmitter. When the transmitter is controlling this pin, its meaning is not RTS at all. It is, rather, that the transmitter has finished sending its last data byte. Programming the MP0 pin to be controlled by the receiver and the transmitter at the same time is allowed, but would usually be incompatible.



NOTE:
C1 AND C2 SHOULD BE BASED ON MANUFACTURER'S SPECIFICATION. PARASITIC CAPACITANCE SHOULD BE INCLUDED WITH C1 AND C2. R1 IS ONLY REQUIRED IF U1 WILL NOT DRIVE TO X1 INPUT LEVELS

TYPICAL CRYSTAL SPECIFICATION

FREQUENCY:	2 – 4MHZ
LOAD CAPACITANCE (C_L):	12 – 32pF
TYPE OF OPERATION:	PARALLEL RESONANT, FUNDAMENTAL MODE

Figure 6. Clock Timing

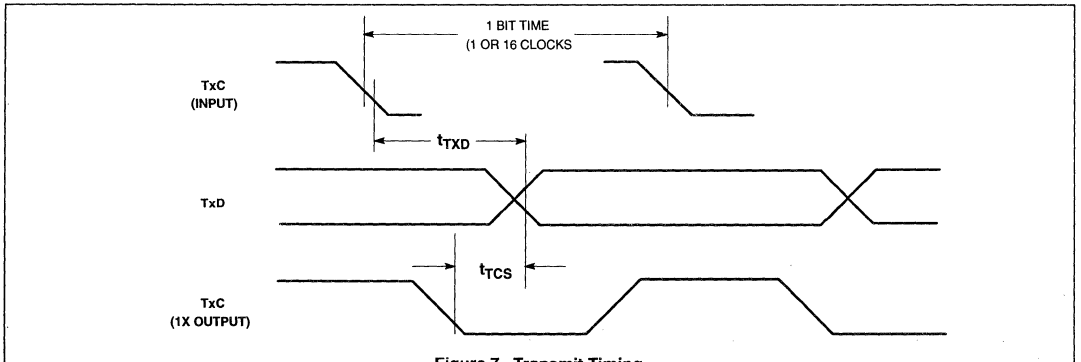


Figure 7. Transmit Timing

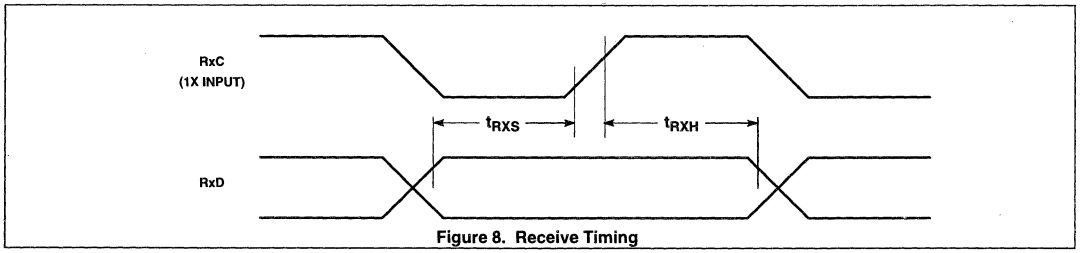
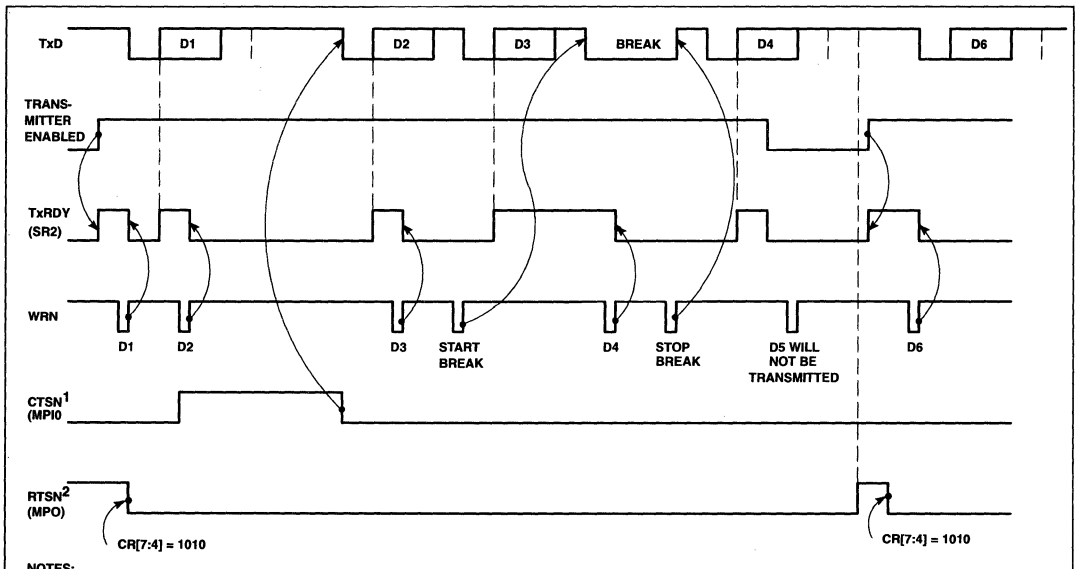
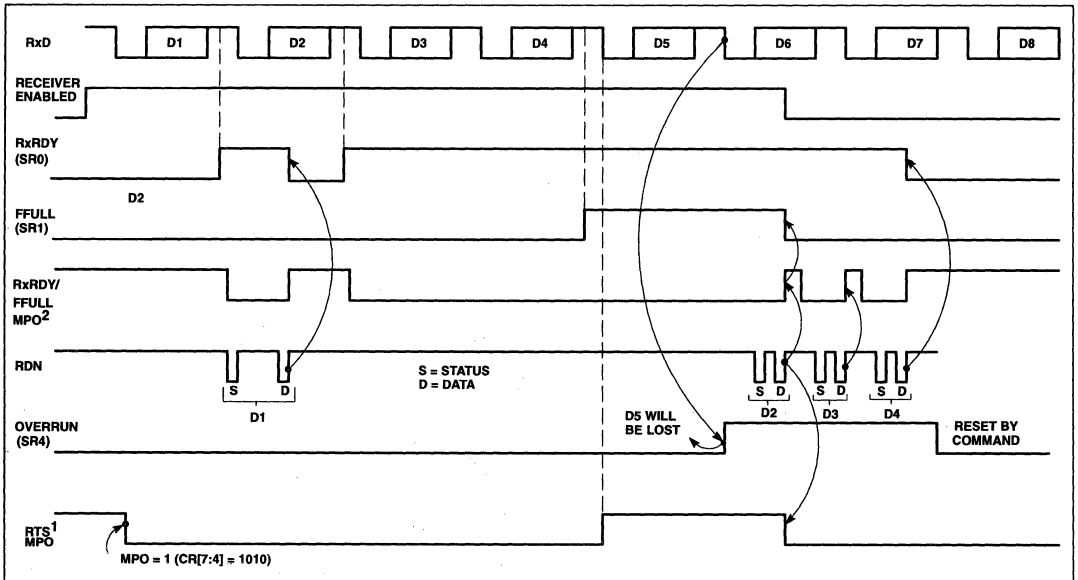


Figure 8. Receive Timing



NOTES:
1. TIMING SHOWN FOR MR2[4] = 1.
2. TIMING SHOWN FOR MR2[5] = 1.

Figure 9. Transmitter Timing



NOTES;
1. TIMING SHOWN FOR MR1[7] = 1.
2. SHOWN FOR OPCR [6:4, 2:0] = 111 AND MR1[6] = 0.

Figure 10. Receiver Timing

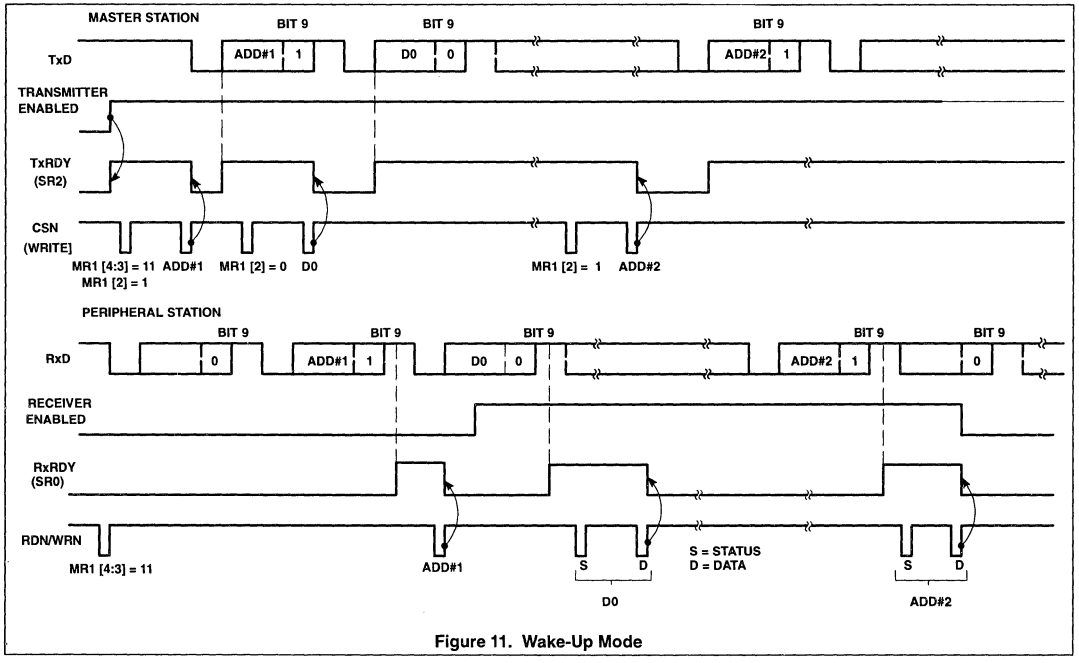


Figure 11. Wake-Up Mode

Output Port Notes

The output ports are controlled from four places: the OPCR register, the OPR register, the MR registers and the command register. The OPCR register controls the source of the data for the output ports OP2 through OP7. The data source for output ports OP0 and OP1 is controlled by the MR and CR registers. When the OPR is the source of the data for the output ports, the data at the ports is inverted from that in the OPR register. The content of the OPR register is controlled by the "Set Output Port Bits Command" and the "Reset Output Bits Command". These commands are at E and F, respectively. When these commands are used, action takes place only at the bit locations where ones exist. For example, a one in bit location 5 of the data word used with the "Set Output Port Bits" command will result in OPR5 being set to one. The OP5 would then be set to zero (V_{SS}). Similarly, a one in bit position 5 of the data word associated with the "Reset Output Ports Bits" command would set OPR5 to zero and, hence, the pin OP5 to a one (V_{DD}).

The CTS, RTS, CTS Enable Tx signals

CTS (Clear To Send) is usually meant to be a signal to the transmitter meaning that it may transmit data to the receiver. The CTS input is on pin IP0 for TxA and on IP1 for TxB. The CTS signal is active low; thus, it is called CTSAN for TxA and CTSBN for TxB.

RTS is usually meant to be a signal from the receiver indicating that the receiver is ready to receive data. It is also active low and is, thus, called RTSAN for RxA and RTSBN for RxB. RTSAN is on pin OP0 and RTSBN is on OP1. A receiver's RTS output will usually be connected to the CTS input of the associated transmitter. Therefore, one could say that RTS and CTS are different ends of the same wire!

MR2(4) is the bit that allows the transmitter to be controlled by the CTS pin (IP0 or IP1). When this bit is set to one AND the CTS input is driven high, the transmitter will stop sending data at the end of the present character being serialized. It is usually the RTS output of the receiver that will be connected to the transmitter's CTS input. The receiver will set RTS high when the receiver FIFO is full AND the start bit of the fourth character is sensed. Transmission then stops with four valid characters in the receiver. When MR2(4) is set to one, CTSN must be at zero for the transmitter to operate. If MR2(4) is set to zero, the IP pin will have no effect on the operation of the transmitter.

MR1(7) is the bit that allows the receiver to control OP0. When OP0 (or OP1) is controlled by the receiver, the meaning of that pin will be RTS. However, a point of confusion arises in that OP0 (or OP1) may also be controlled by the transmitter. When the transmitter is controlling this pin, its meaning is not RTS at all. It is, rather, that the transmitter has finished sending its last data byte. Programming the OP0 or OP1 pin to be controlled by the receiver and the transmitter at the same time is allowed, but would usually be incompatible.

RTS can also be controlled by the commands 1000 and 1001 in the command register. RTS is expressed at the MP0 pin which is still an output port. Therefore, the state of MP0 should be set low (either by commands of the CR register or by writing to the Set Output Ports Register) for the receiver to generate the proper RTS signal. The logic at the output is basically a NAND of the MP0 bit register and the RTS signal as generated by the receiver. When the RTS flow control is selected via the MR(7) bit the state of the MP0 register is

not changed. Terminating the use of "Flow Control" (via the MR registers) will return the MP0 pin to the control of the MP0 register.

Transmitter Disable Note

The sequence of instructions enable transmitter — load transmit holding register — disable transmitter will result in nothing being sent if the time between the end of loading the transmit holding register and the disable command is less that 3/16 bit time in the 16x mode or one bit time in the 1x mode. Also, if the transmitter, while in the enabled state and underrun condition, is immediately disabled after a single character is loaded to the transmit holding register, that character will not be sent.

In general, when it is desired to disable the transmitter before the last character is sent AND the TxEMT bit is set in the status register (TxEMT is always set if the transmitter has underrun or has just been enabled), be sure the TxRDY bit is active immediately before issuing the transmitter disable instruction. TxRDY sets at the end of the "start bit" time. It is during the start bit that the data in the transmit holding register is transferred to the transmit shift register.

Non-standard baud rates are available as shown in Table 5 below, via the BRG Test function.

Table 5. Baud Rates Extended

	Normal BRG		BRG Test	
CSR[7:4]	ACR[7] = 0	ACR[7] = 1	ACR[7] = 0	ACR[7] = 1
0000	50	75	4,800	7,200
0001	110	110	880	880
0010	134.5	38.4K	1,076	38.4K
0011	200	150	19.2K	14.4K
0100	300	300	28.8K	28.8K
0101	600	600	57.6K	57.6K
0110	1,200	1,200	115.2K	115.2K
0111	1,050	2,000	1,050	2,000
1000	2,400	2,400	57.6K	57.6K
1001	4,800	4,800	4,800	4,800
1010	7,200	1,800	57.6K	14.4K
1011	9,600	9,600	9,600	9,600
1100	38.4K	19.2K	38.4K	19.2K
1101	Timer	Timer	Timer	Timer
1110	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X	I/O2 – 16X
1111	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X	I/O2 – 1X

NOTE:
Each read on address H'2' will toggle the baud rate test mode. When in the BRG test mode, the baud rates change as shown to the left. This change affects all receivers and transmitters on the DUART. Also, the RTSN output (MP0) become the transmitter 1x clock.

The test mode at address H'A' changes all transmitters and receivers to the 1x mode and connects the output ports to some internal nodes.

A condition that occurs infrequently has been observed where the receiver will ignore all data. It is caused by a corruption of the start bit generally due to noise. When this occurs the receiver will appear to be asleep or locked up. The receiver must be reset for the UART to continue to function properly.

Reset in the Normal Mode (Receiver Enabled)

Recovery can be accomplished easily by issuing a receiver software reset followed by a receiver enable. All receiver data, status and programming will be preserved and available before reset. The reset will NOT affect the programming.

Reset in the Wake-Up Mode (MR1[4:3] = 11)

Recovery can also be accomplished easily by first exiting the wake-up mode (MR1[4:3] = 00 or 01 or 10), then issuing a receiver software reset followed by a wake-up re-entry (MR1[4:3] = 11). All receiver data, status and programming will be preserved and available before reset. The reset will NOT affect the programming.

The receiver has a digital filter designed to reject "noisy" data and the receiver state machine was designed to reject noisy start bits or noise that might be considered a start bit. In spite of these precautions, corruption of the start bit can occur in 15ns window approximately 100ns prior to the rising edge of the data clock. The probability of this occurring is less than 10^{-5} at 9600 baud.

A corrupted start bit may have some deleterious effects in ASYNC operation if it occurs within a normal data block. The receiver will tend to align its data clock to the next '0' bit in the data stream, thus potentially corrupting the remainder of the data block. A good design practice, in environments where start bit corruption is possible, is to monitor data quality (framing error, parity error, break change and received break) and "data stopped" time out periods. Time out periods can be enabled using the counter/timer in the SCC2691, SCC2692, SCC2698B and SC68692 products. This monitoring can indicate a potential start bit corruption problem.

SCC2698B Octal universal asynchronous receiver/transmitter (Octal-UART)

AN410B

DEVICE ARCHITECTURE

The Philips Semiconductors SCC2698B Octal UART is composed of four blocks, each logically equivalent to a 2681 or 2692 DUART. Each block is composed of two channels, a counter/timer, and an interrupt control section. The channels are matched to the blocks as shown in Figure 1. The blocks are indicated by capital letters A, B, C, and D; the channels are indicated by lower-case letters a, b, c, d, e, f, g, and h. All registers act either on a block or an individual channel.

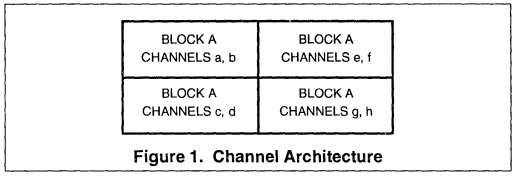


Figure 1. Channel Architecture

Registers that affect a block:
IPCR/ACR
ISR/IMR
CTU/CTUR
CTL/CTLR
IPR/OPCR
START C/T
STOP C/T

Registers that affect a channel:
MR1/MR2
SR/CSR
CR
RHR/THR

NOTE: This application note also applies to the SCC2698A Octal UART unless otherwise indicated.

X1/CLK SOURCES

The SCC2698B must have a clock source connected to the X1 input at all times. It can be supplied by a crystal between the X1 and X2 pins, or by driving an external clock into the X1/CLK input. The frequency must be between 2.0 and 4.0MHz for correct device operation; 3.6864MHz is the nominal frequency which is used to obtain the standard baud rates listed for the internal baud rate generator.

X1/X2 Crystal

The SCC2698B oscillator circuitry consists of an inverting amplifier and a feedback resistor which are used to implement a Pierce oscillator (see Figure 2). This circuitry will cause the crystal attached between the X1 and X2 pins to go into anti-resonant (parallel) operation. So, while a number of crystal and capacitor combinations will work, obtaining a parallel calibrated crystal and adjusting the external capacitor values until the total circuit capacitance matches the capacitance specified for the crystal will result in the most accurate frequency value. Using 24pF capacitors and the parallel crystal recommended below will give accurate, reliable results. The frequency will vary slightly depending on the amount of stray capacitance in the individual circuit, but will typically be off no more than 0.01%. The frequency can be adjusted by trimming the external capacitors; larger capacitors lower the oscillator's frequency and smaller ones raise it.

A source for the 3.6864MHz crystal is: Saronix, Palo Alto, CA. From California, call (800) 422-3355; outside California, call (800) 227-8974. Request part number NYP037-20.

Externally Driven Clock

The most important point in using an external source to drive the X1/CLK input is to meet the V_{IH} specification of $0.8V_{CC}$ (4.0V at V_{CC} = 5.0V). This can be insured by using an open collector buffer with a pull-up resistor to V_{CC} to drive the X1 input. Also, when driving a clock into X1, be sure to leave the X2 pin open; grounding it will kill the oscillation.

BAUD RATE GENERATION TECHNIQUES

There are 18 standard baud rates available using the internal baud rate generator when the X1/CLK frequency is 3.6864MHz. These are selected by ACR[7] and by CSR[7:4] for the receiver and CSR[3:0] for the transmitter.

The baud rate generator table follows:

Table 1. Baud Rate Generator Table

CSR[7:4] (or [3:0])	ACR[7] = 0	ACR[7] = 1
0000	50	75
0001	110	110
0010	134.5	38.4k
0011	200	150
0100	300	300
0101	600	600
0110	1,200	1,200
0111	1,050	2,000
1000	2,400	2,400
1001	4,800	4,800
1010	7,200	1,800
1011	9,600	9,600
1100	38.4k	19.2k

The baud rate generator can also be used to generate other baud rates by using a different X1/CLK frequency. For this case, each ACR[7] and CSR combination gives a different division ratio. The division ratio table follows:

Table 2. Division Ratio Table

CSR[7:4] (or [3:0])	ACR[7] = 0	ACR[7] = 1
0000	73,728	49,152
0001	33,536	33,536
0010	27,392	96
0011	18,432	24,576
0100	12,288	12,288
0101	6,144	6,144
0110	3,072	3,072
0111	3,520	1,840
1000	1,536	1,536
1001	768	768
1010	512	2,048
1011	384	384
1100	96	192

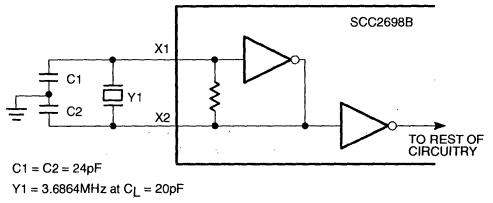


Figure 2. Pierce Oscillator Using On-Board Oscillator Circuitry

The baud rate can be calculated by dividing the X1/CLK frequency by the appropriate division ratio. For example, if the X1/CLK frequency = 3MHz, ACR[7] = 0 and CSR = CC hex, the division ratio is 96 and both the receiver and transmitter will use a 31.25K baud rate.

Externally Generated Baud Rate

An externally generated baud rate clock can be used for each transmitter and receiver using multipurpose pins MPP1 and MPP2. These are only available in the 84-pin PLCC package. OPCR[7] must be programmed to a zero to use these pins as inputs. MPP2 is used as a 16X clock source for the receiver by programming CSR[7:4] = 1110 and as a 1X clock source by programming CSR[7:4] = 1111. MPP1 is used as a 16X clock source for the transmitter by programming CSR[3:0] = 1110 and a 1X clock source by programming CSR[3:0] = 1111. (NOTE: MPP1 and MPP2 on the SCC2698B correspond to MPI2 and MPI3 on the SCC2698A. On the SCC2698A, the state of OPCR[7] does not affect the function of MPI2 and MPI3.) The maximum frequency that can be used as a 16X clock is 2MHz, which results in a baud rate of 125Kbps. The maximum frequency that can be used as a 1X clock is 1MHz, for a maximum baud rate of 1Mbps.

Counter/Timer as 16X Baud Rate Clock

The counter/timer can be used in timer mode to divide the X1/CLK or an external clock. The output of the C/T is internally connected as a 16X clock source for the receiver by programming CSR[7:4] = 1101 and as a 16X clock source for the transmitter by programming CSR[3:0] = 1101. The clock source for the timer is selected by ACR[6:4] as follows:

ACR[6:4]	Timer Clock Source
100	MPI1 pin *
101	MPI1 pin divided by 16*
110	X1/CLK
111	X1/CLK
* The MPI1 pin available as a clock source is MPI1 a, c, e, and g only	

In addition, the CTUR and CTLR registers must be programmed with the divisor value for the timer. The minimum allowable value to program is 0002 hex. The timer will generate a square wave with a period of twice the number of timer clock periods programmed into CTUR/CTLR. The resultant baud rate is calculated by:

$$\left(\frac{\text{timer clock}}{2 \times \text{CTUR/CTLR value}}\right) \div 16$$

The maximum baud rate available in this manner is 62.5Kbps. This is obtained with an X1/CLK = 4MHz and programming as shown in example 1.

Counter/Timer as 1X Baud Rate Clock

The timer can also be used as a 1X clock source for the transmitter by externally connecting the C/T output to MPP1 (MPI2 on the SCC2698A). In addition, the C/T output can be connected to MPP2 (MPI3 on the SCC2698A) to provide a 1X clock source for the receiver, but care must be taken to have the timer output synchronized with the incoming data to ensure accurate data reception. These inputs are only available in the 84-pin PLCC packaged part. The C/T is set up as described in the last section. The resultant baud rate is calculated by:

$$\left(\frac{\text{timer clock}}{2 \times \text{CTUR/CTLR value}}\right)$$

The maximum baud rate available in this manner is 1Mbps. This is obtained with an X1/CLK = 4MHz, MPO externally connected to MPP1 and MPP2 and programmed as shown in example 2.

RTS/CTS FLOW CONTROL

One way to achieve flow control with the SCC2698B is to have the request to send (RTS) output, controlled by the receiver, connected to the clear to send (CTS) input, which enables the transmitter. RTS is controlled by the receiver when MR1[7] = 1, and the multi-purpose output (MPO) is used as the RTS output when OPCR[6:4] = 0 and OPCR[2:0] = 0.

Initially, the RTS output must be asserted by writing CR[7:4] = 1000 immediately after enabling the receiver. After this, RTS will automatically negate upon receipt of a valid start bit if the receiver FIFO is full, and will reassert when an empty FIFO position is available. CTS enables the transmitter and MPI0 is used as the CTS input pin when MR2[4] = 1. When CTS is negated, the transmitter will complete transmitting a character already in progress, but will not transmit a character waiting in the THR. The TxD output will then go into the marking state and the transmitter clock will be stopped. The Tx empty bit will not be set (even if the transmitter is empty) until the transmitter clock starts running again. When CTS is re-asserted, the transmitter will start again, transmitting if a character is waiting in the THR or setting the empty bit if not. Be careful if the transmitting device is not a Philips Semiconductors part, as some devices will transmit both the character in the transmitter shift register and the character in the transmitter holding register when CTS is negated. If this occurs, the receiver may be overrun by a fifth character.

Modem control configurations may require RTS to be controlled by the transmitter, asserted for the entire time the message is being sent, and negated on completion of the transmission. RTS is controlled by the transmitter when MR2[5] = 1, and MPO is used as the RTS output when OPCR[6:4] = 0 and OPCR[7:4] = 1000 after the transmitter has been enabled and before the first byte of the message is loaded into the THR. This last character will be transmitted and RTS will be negated one bit time after the last stop bit.

Example 1.

```
CSD=DD HEX          ;Rx & Tx USE TIMER AS
                     16X BAUD RATE
                    ;CLOCK
ACR[7]=DON'T CARE
ACR[6:4]=110        ;X1/CLK IS TIMER 1X CLOCK
                     SOURCE
CTUR/CTLR=0002 HEX;TIMER HAS DIVISOR OF 2
```

Example 2.

```
CSR=FF HEX          ;Rx USES MPP2 AND Tx USES
                    ;MPP1 AS A 1X BAUD RATE CLOCK
ACR[7]=DON'T CARE
ACR[6:4]=110        ;X1/CLK IS TIMER 1X CLOCK
                    ;SOURCE
CTUR/CTLR=0002 HEX;TIMER HAS DIVISOR OF 2
OPCR[7:4]=0001      ;MP0 IS C/T OUTPUT, MPP1 AND
                    ;MPP2 ARE CLOCK INPUTS
```

Note that this example is shown to further demonstrate the device's versatility in baud rate generation. For most applications, this method is good for the transmit clock, but may not be a recommended method for accurate data reception, unless the timer clock source is synchronized with the incoming data.

Example 3.

```
RXRDY:  MOVE.B   #$00,$3000  ; DUMMY WRITE
        MOVE.B   SR,D3       ; READ STATUS REGISTER
        BTST     #0,D3       ; CHECK FOR RXRDY
        BEQ      RXRDY       ; IF NOT, KEEP CHECKING
```

MULTI-PURPOSE INPUTS

There are four multi-purpose inputs provided for each channel for the 84-pin PLCC package, MPI0 and MPI1, and MPI1 and MPI2 when OPCR[7] is programmed as a zero. The DIP package has one multi-purpose input for each channel, MPI0. The current state for each of these pins can be read from the input port register (IPR). Each input can be used as a general purpose input, to be interpreted as the user desires. In addition, each input can be programmed to provide a specific defined input, as follows:

- Current state also in the input port change register (IPCR)
- Has a change of state indicator in IPCR, which can also be used to generate an interrupt.
- When MR2[4] = 1, it is used as CTSN input to enable the transmitter.

MPI1

- Current state also in the input port change register (IPCR).
- Has a change of state indicator in IPCR, which can also be used to generate an interrupt.
- When ACR[6:4] = 000, MPI1a, MPI1c, MPI1e and MPI1g are used as a 1X counter clock source. When ACR[6:4] = 001, MPI1a, MPI1c, MPI1e and MPI1g are used as a 16X timer clock source.
- For all four of these programmed cases, MPI1b, MPI1d, MPI1f and MPI1h stay as general purpose inputs, since there is only one C/T clock for each block.

MPP1 (MPI2 on SCC2698A)

- When CSR[3:0] = 1110, it is used as the transmitter 16X baud rate clock input.

MPP1 (MPI2 on SCC2698A)

- When CSR[7:4] = 1110, it is used as the receiver 16X baud rate clock input.
- When CSR[7:4] = 1111, it is used as the receiver 1X baud rate clock input.

Rx AND Tx STATUS OUTPUTS

When OPCR[7] of a block is programmed to '1', the MPP pins for that block become active low open drain outputs. MPP1 then becomes the TxRDY status output for its corresponding transmitter, while MPP2 then becomes the RxRDY/FFULL status output for its corresponding receiver. These outputs may be used for interrupts or as DMA request control signals. These outputs are not masked by the IMR register. NOTE: This function is not available on the SCC2698A.

BUS INTERFACE

The internal control signals for strobing read and write cycles are obtained by internally logically ANDing CEN with RDN, and CEN with WRN. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle. However, the RDN line cannot be left asserted with just the CEN line pulsed. The RDN signal must be negated between reads, because the status register can only be updated at that time.

When using a 68000 type bus interface with a static R/WN output, either a hardware or a software method of pulsing the RDN line must be designed in. An example of a hardware solution is to logically AND the CEN signal with the inversion of R/WN to provide RDN (see attached schematic). RDN can also be negated by the software, the inversion of R/WN can be used for RDN, and a dummy write can be performed between consecutive reads. For example, in a polling loop of the status register, see example 3.

POWER DOWN MODE

The 2698B is equipped with a special power down feature which can be used for energy conservation during idle periods. This mode saves the contents of all the internal registers, stops the oscillator and suspends the operation of any function that uses the oscillator. In addition, the I_{CC} current used by the part is reduced to 2mA. The part can be put into power down mode at any time, and restored to normal operation when needed. Since all register values are saved, reinitialization is not necessary.

To put the part into power down mode:

For each channel:
- CR7:4] = 0011 – Reset Tx
- CR[7:4] = 0010 – Reset Rx

Once only:
- OPCRA[3] = 0 – Turn off power down mode

To get out of power down mode:

Once only:
- OPCRA[3] = 0 – Turn off power down mode

For each channel:
- CR[3:0] = 0101 – Enable Rx and Tx

GENERAL INITIALIZATION

Figure 3 shows the flow of a typical initialization. Note that the transmitter and receiver should be disabled before writing to MR1,

MR2, CSR, ACR[7] or OPCR[3] and reset before continuing operation. The other registers, if used, can be changed at any time. A local loopback mode program example is also given to demonstrate the basic initialization and use of the device. This example checks each channel separately, each is initialized in local loopback mode and uses polled operation to send and receive 256 characters, comparing each character received to the one that was sent.

WAKE-UP MODE

The wake-up mode provides automatic wake-up of the receiver through address frame recognition for multi-processor communications. This mode is selected by programming MR1[4:3] = 11. In this mode, the transmitter (in the primary or master station) will send data with the last bit of each character identified as the address/data (A/D) bit. When MR1[2] = 0, the A/D bit will be transmitted as a '0', which will cause the character to be interpreted by the receivers (in the secondary or slave stations) as a data character. When MR1[2] = 1, the A/D bit will be transmitted as a '1', which will cause the character to be interpreted by the slave stations as an address character. The slave stations are normally disabled, but the receivers monitor the received data stream and will load the character into the RHR FIFO and set the RxRDY status bit if the character has the address bit set. The slave station can then examine the address character to see if it should read the subsequent data.

The master station should allow adequate time between sending the address character and the first data character for the slowest slave station to determine if it has an address match. Once a station has an address match, it then enables its receiver to start receiving data.

Some applications have to interface to an existing system, and have no control of the time between the address and data characters. When this time is too short for the CPU to make an address verification, the first data character could be missed. This would generally only be a problem at higher baud rates (192.k, 38.4k). If this is a problem in your application, the CPU can enable the receiver as soon as the address is received. Later, after the compare operation, the CPU can either read the data or reset the receiver depending on whether the address was a match.

Changing between address and data modes in the master station requires a write to MR1. Before doing this, wait for transmitter empty to indicate that the previous character is done and then disable the transmitter and receiver of this station. See Figures 4 and 5, and the wake-up mode program example.

SCC2698B Octal universal asynchronous receiver/transmitter (Octal-UART)

AN410B

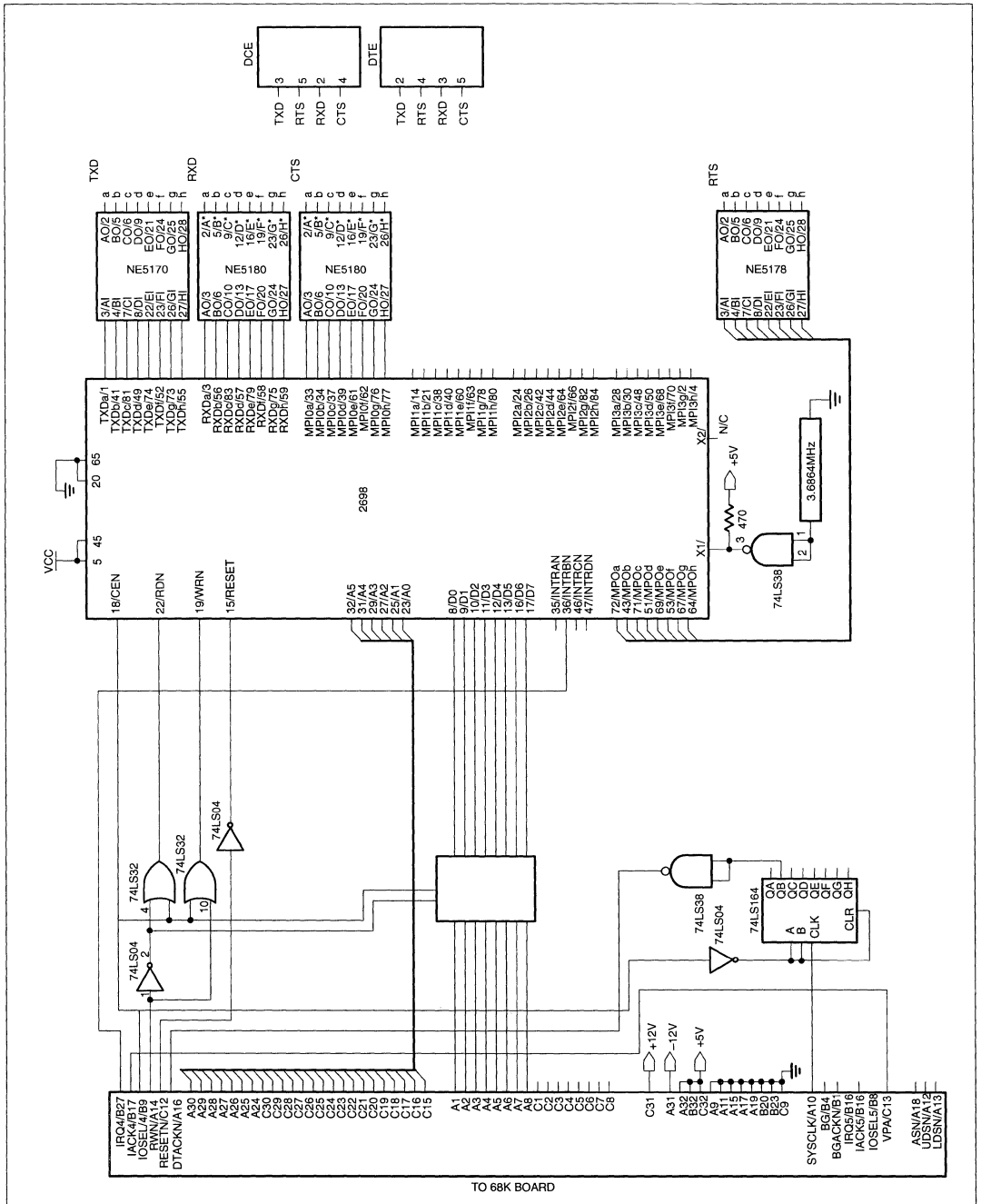


Figure 3. Sample SCC2698 to 68K Interface

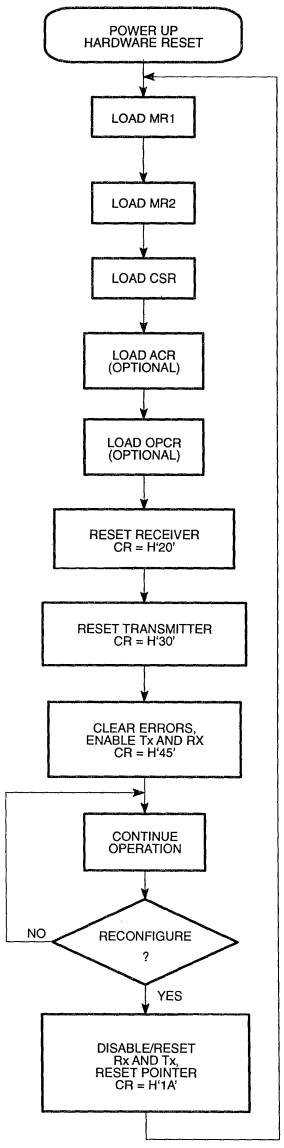


Figure 4. Basic Initialization

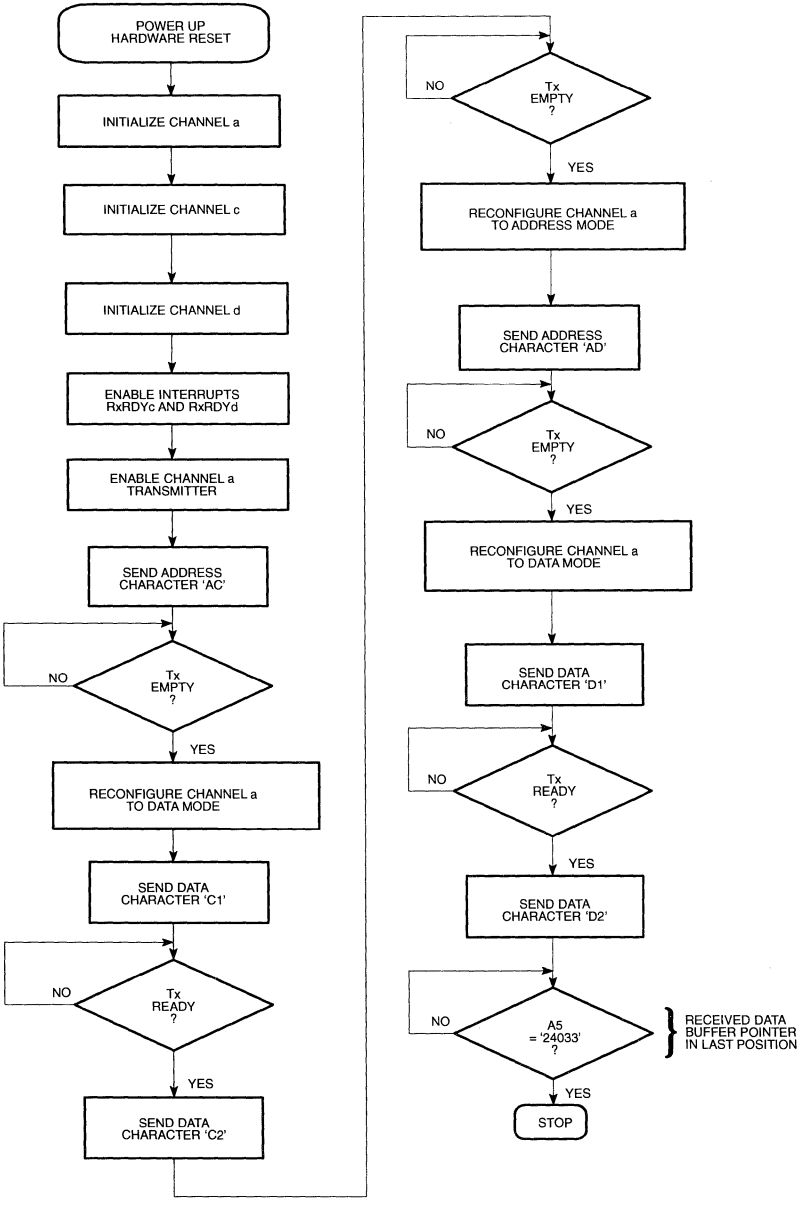


Figure 5. Wake-Up Mode Example, Main Program Flowchart

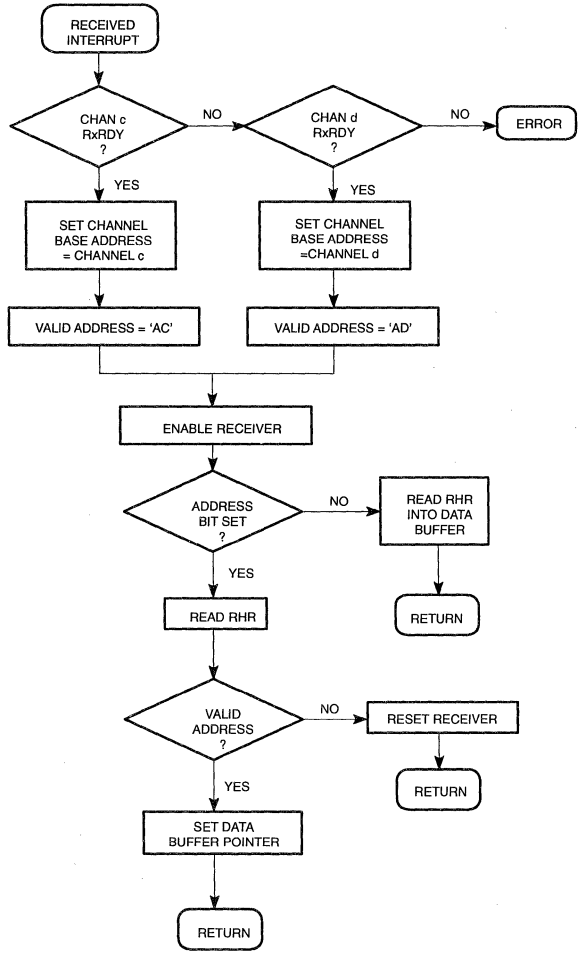


Figure 6. Wake-Up Mode Example, Interrupt Routine Flowchart

LOCAL LOOPBACK MODE PROGRAM EXAMPLE

```
;THIS IS PROGRAM 2698 LOCAL LOOP
;IT SEPARATELY TESTS EACH CHANNEL IN LOCAL LOOPBACK
;MODE, SENDING 256 CHARACTERS AND COMPARING EACH
;CHARACTER SENT WITH EACH ONE RECEIVED.
;D. IBARRA JULY 1987
;           BEGIN
CHANa       EQU         $74001          ;CHANNEL BASE ADDRESSES
CHANb       EQU         $74011
CHANc       EQU         $74021
CHANd       EQU         $74031
CHANe       EQU         $74041
CHANf       EQU         $74051
CHANg       EQU         $74061
CHANh       EQU         $74071
;
BLOCKA      EQU         $74001          ;BLOCK BASE ADDRESSES
BLOCKB      EQU         $74021
BLOCKC      EQU         $74041
BLOCKD      EQU         $74061
;
MR1         EQU         $0              ;CHANNEL REGISTER OFFSETS
MR2         EQU         $0
STATR       EQU         $2
CSR         EQU         $2
CR          EQU         $4
RHR         EQU         $6
THR         EQU         $6
;
IPCR        EQU         $8              ;BLOCK REGISTER OFFSETS
ACR         EQU         $8
ISR         EQU         $A
IMR         EQU         $A
CTU         EQU         $D
CTUR        EQU         $D
CTL         EQU         $E
CTLR        EQU         $E
IPR         EQU         $1A
OPCR        EQU         $1A
STRTCT      EQU         $1C
STOPCT      EQU         $1E
;
START:      MOVEA.L     #CHANa,A2       ;TEST CHAN a
            JSR         INIT
            JSR         TEST
            MOVEA.L     #CHANb,A2       ;TEST CHAN b
            JSR         INIT
            JSR         TEST
            MOVEA.L     #CHANc,A2       ;TEST CHAN c
            JSR         INIT
            JSR         TEST
            MOVEA.L     #CHANd,A2       ;TEST CHAN d
            JSR         INIT
            JSR         TEST
            MOVEA.L     #CHANe,A2       ;TEST CHAN e
            JSR         INIT
            JSR         TEST
            MOVEA.L     #CHANf,A2       ;TEST CHAN f
            JSR         INIT
            JSR         TEST
```

```
                MOVEA.L     #CHANg,A2       ;TEST CHAN g
                JSR         INIT
                JSR         TEST
                MOVEA.L     #CHANh,A2       ;TEST CHAN h
                JSR         INIT
                JSR         TEST
;
                MOVEA.L     #0,A2           ;CLEAR ADDRESS REG.
STOP:           TRAP        #15
;
;———————————SUBROUTINES———————————————————
;
INIT:           MOVE.B      #$1A,CR[A2]     ;DISABLE TX & RX, RESET POINTER
                MOVE.B      #$13,MR1[A2]    ;NO PARITY, 8 BITS
                MOVE.B      #$87,MR2[A2]    ;LOCAL LOOP, STOP=1
                MOVE.B      #$66,CSR[A2]    ;TXC=RXC=BRG,1200 BAUD
                MOVE.B      #$20,CR[A2]     ;RESET RECEIVER
                MOVE.B      #$30,CR[A2]     ;RESET TRANSMITTER
                MOVE.B      #$45,CR[A2]     ;CLR ERRORS, ENABLE TX–RX
                RTS
;
TEST:           MOVE.W      #$100,D7        ;CLEAR SEND REGISTER
AGAIN:          SUBI.B      #$1,D7          ;DEC. SEND CHAR.
                BEQ         DONE            ;UNTIL D7=0, THEN DONE
                MOVE.B      D7,THR[A2]      ;TRANSMIT CHAR
                BSR         RXRDY           ;WAIT FOR RXRDY
                MOVE.B      RHR[A2],D1      ;RECEIVE CHAR INTO D1
                CMP.B       D7,D1           ;SENT CHAR=RECEIVE CHAR ?
                BEQ         AGAIN           ;IF SO, KEEP SENDING
                TRAP        #15             ;STOP IF FAIL
DONE:           RTS
;
RXRDY:          MOVE.B      STATR[A2],D3    ;STATUS REG. TO D3
                BTST        #0,D3           ;IS RECEIVER READY ?
                BEQ         RXRDY           ;IF NOT, WAIT
                RTS

                END         START
```

wake-up MODE PROGRAM EXAMPLE

```
;THIS IS PROGRAM 2698 WAKE-UP
;IT USES CHAN. a AS THE MASTER STATION, AND
;CHANNELS c AND d AS SLAVE RECEIVING STATIONS.
;CHAN. a TRANSMITTER IS EXTERNALLY CONNECTED
;TO c AND d RECEIVERS.  THIS PROGRAM IS INTERRUPT
;DRIVEN, THE SLAVE STATIONS WILL INTERRUPT ON RXRDY.
;
;D. IBARRA JULY 1987
;               BEGIN
;
CHANa           EQU     $74001          ;CHANNEL BASE ADDRESSES
CHANb           EQU     $74011
CHANc           EQU     $74021
CHANd           EQU     $74031
CHANe           EQU     $74041
CHANf           EQU     $74051
CHANg           EQU     $74061
CHANh           EQU     $74071
;
BLOCKA          EQU     $74001          ;BLOCK BASE ADDRESSES
BLOCKB          EQU     $74021
BLOCKC          EQU     $74041
BLOCKD          EQU     $74061
;
MR1             EQU     $0              ;CHANNEL REGISTER OFFSETS
MR2             EQU     $0
STATR           EQU     $2
CSR             EQU     $2
CR              EQU     $4
RHR             EQU     $6
THR             EQU     $6
;
IPCR            EQU     $8              ;BLOCK REGISTER OFFSETS
ACR             EQU     $8
ISR             EQU     $A
IMR             EQU     $A
CTU             EQU     $D
CTUR            EQU     $D
CTL             EQU     $E
CTLR            EQU     $E
IPR             EQU     $1A
OPCR            EQU     $1A
STRTCT          EQU     $1C
STOPCT          EQU     $1E
;
START:          MOVEA.L #CHANa,A1
                MOVEA.L #CHANa,A2       ;INIT CHAN a
                JSR     INIT
                MOVEA.L #CHANc,A2       ;INIT CHAN c
                JSR     INIT
                MOVEA.L #CHANd,A2       ;TEST CHAN d
                JSR     INIT
                MOVEA.L #BLOCKB,A3      ;ENABLE RXRDY INTERRUPTS
                JSR     SETINT
;
                MOVE.B  #$04,CR[A1]     ;ENABLE TX CH. a
                MOVE.B  #$AC,THR[A1]    ;SEND ADDRESS CHAR
                JSR     DTMODE          ;CHANGE TO DATA MODE
```

```
                MOVE.B      #$C1,THR[A1]    ;SEND DATA
                JSR         TXRDY           ;WAIT FOR TXRDY
                MOVE.B      #$C2,THR[A1]    ;SEND DATA
                JSR         ADMODE          ;CHANGE TO ADDRESS MODE
                MOVE.B      #$AD,THR[A1]    ;SEND ADDRESS CHAR
                JSR         DTMODE          ;CHANGE TO DATA MODE
                MOVE.B      #$D1,THR[A1]    ;SEND DATA
                JSR         TXRDY           ;WIAT FOR TXRDY
;
WTDN:           MOVE.L      A5,D1           ;MOVE DATA BUFFER POINTER TO D1
                CMP.L       #$24033,D1      ;IS IT IN LAST POSITION ?
                BNE         WTDN            ;IF NOT, WAIT UNTIL DONE
                MOVEA.L     #0,A2           ;CLEAR ADD. REG.
                TRAP        #15             ;TO INDICATE NORMAL END
;
;————————————SUBROUTINES————————————————————
;
INIT:           MOVE.B      #$1A,CR[A2]     ;DISABLE TX & RX, RESET POINTER
                MOVE.B      #$1F,MR1[A2]    ;WAKE-UP, 8 BITS, A/D=1
                MOVE.B      #$07,MR2[A2]    ;NORMAL, STOP=1
                MOVE.B      #$66,CSR[A2]    ;TXC=RXC=BRG,1200 BAUD
                MOVE.B      #$20,CR[A2]     ;RESET RX
                MOVE.B      #$30,CR[A2]     ;RESET TX
                MOVE.B      #$40,CR[A2]     ;CLEAR ERRORS
                RTS
;
SETINT:         LEA.L       INT,A6          ;PUT INT. ROUTINE ADD. INTO A6
AGAIN:          MOVE.L      A6,$10476       ;ADD. TO AUTO VECTOR #4 LOCATION
                MOVE.B      #$22,IMR[A3]    ;INT. ON RXRDY BOTH CHANNELS
                RTS
;
DTMODE:         JSR         TXEMTY          ;WAIT FOR TXEMPTY
                MOVE.B      #$1A,CR[A1]     ;DISABLE TX AND RX, RESET POINTER
                MOVE.B      #$1B,MR1[A1]    ;WAKE-UP, 8 BITS, A/D=0
                MOVE.B      #$20,CR[A1]     ;RESET RX
                MOVE.B      #$30,CR[A1]     ;RESET TX
                MOVE.B      #$44,CR[A1]     ;CLEAR ERRORS,ENABLE TX
                RTS
;
ADMODE:         JSR         TXEMTY          ;WAIT FOR TXEMPTY
                MOVE.B      #$1A,CR[A1]     ;DISABLE TX AND RX, RESET POINTER
                MOVE.B      #$1F,MR1[A1]    ;WAKE-UP, 8 BITS, A/D=1
                MOVE.B      #$20,CR[A1]     ;RESET RX
                MOVE.B      #$30,CR[A1]     ;RESET TX
                MOVE.B      #$44,CR[A1]     ;CLEAR ERRORS,ENABLE TX
                RTS
;
TXEMTY:         MOVE.B      STATR[A1],D1    ;MOVE STATUS REG. TO D1
                BTST        #3,D1           ;IS TX EMPTY ?
                BEQ         TXEMTY          ;IF NOT, WAIT
                RTS
;
TXRDY:          MOVE.B      STATR[A1],D1    ;MOVE STATUS REG. TO D1
                BTST        #2,D1           ;IS TXRDY ?
                BEQ         TXRDY           ;IF NOT, WAIT
                RTS
;
```

Octal universal asynchronous receiver/transmitter (UART) SC26C198

DESCRIPTION

The Philips 26C198 Octal UART is a single chip CMOS-LSI communications device that provides 8 full-duplex asynchronous channels with significantly deeper 16 byte FIFOs, Automatic in-band flow control using Xon/Xoff characters defined by the user and address recognition in the wake up mode. Synchronous bus interface is used for all communication between hose and OCTART. It is fabricated using Philips Semiconductors 1.0 micron CMOS technology that combines the benefits of low cost, high density and low power consumption.

The operating speed of each receiver and transmitter can be selected independently: from one of 22 fixed baud rates, a 16X clock derived from one of two programmable baud rate counters or one of three external 16X clocks (1 available at 1x). The baud rate generator and counter can operate directly from a crystal or from seven other external or internal clock inputs. The ability to independently program the operating speed of the receiver and transmitter makes the Octal UART particularly attractive for dual speed channel applications such as clustered terminal systems. The receiver is buffered with a FIFO of 16 characters to minimize the potential for receiver overrun and to reduce interrupt overhead. In addition, a handshaking capability and in-band flow control are provided to disable a remote UART transmitter when the receiver buffer is full or nearly so.

To minimize interrupt overhead an interrupt arbitration system is included which reports the context of the interrupting UART via direct access or through the modification of the interrupt vector.

The Octal UART provides a power down mode in which the oscillator is frozen but the register contents are maintained. This results in reduced power consumption of several magnitudes. The Octal UART is fully TTL compatible when operating from a single +5V power supply.

The device also offers operating modes with a 3.3V power supply.

USES

- Statistical Multiplexers
- Data Concentrators
  - Packet-switching networks
  - Process Control
  - Building or Plant Control
  - Laboratory data gathering
  - ISDN front ends
  - Computer Networks
  - Point-of-Sale terminals
- Automotive, cab and engine controls
- Entertainment systems
  - MIDDI keyboard control music systems
  - Theater lighting control
- Terminal Servers
- Computer-Printer/Plotter links

FEATURES:

- Eight Philips industry standard full duplex UART channels
- Sixteen byte receiver FIFOs for each UART
- Sixteen byte transmit FIFOs for each UART
- Single 5V or 3.3V power supply
- In band flow control using programmable Xon/Xoff characters
- Automatic address detection in multi-drop mode
- Three byte general purpose character recognition
- Fast data bus, 30ns data bus release time, 125ns bus cycle time
- Programmable interrupt priorities
- Automatic identification of highest priority interrupt pending
- Global interrupt and control registers ease setup and interrupt handling
- Vectored interrupts with programmable interrupt vector formats
- IACKN and DACKN signal pins
- Watch dog timer for each receiver (64 receive clock counts)
- Programmable Data Formats:
  - 5 to 8 data bits plus parity
  - Odd, even force or no parity
  - 1, 1.5 or 2 stop bits
- Flexible baud rate selection for receivers and transmitters:
  - 22 fixed rates; 50 – 230.4K baud
  - Additional non-standard rates to 460.8K baud
  - Two reload-counters provide additional programmable baud rate generation
  - External 1x or 16x clock
  - Simplified baud rate selection
- 1 MHz 1x mode operation
- Parity, framing and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode
  - Normal(full duplex)
  - automatic echo
  - local loop back
  - remote loop back
- Four I/O ports per UART for modem controls, clocks, RTSN, I/O etc.
- Two global inputs and two global outputs for general purpose I/O
- Power down mode
- On chip crystal oscillator, 2–8 MHz
- TTL compatible at V_{CC} = 5V; modified CMOS levels at V_{CC} = 3V.
- High speed CMOS technology
- 84 pin PLCC
- Commercial and industrial temperature ranges.

PINOUT

Pin	Function	Pin	Function	Pin	Function
1	V_{SS}	29	I/O1d	57	I/O2g
2	V_{CC}	30	I/O2d	58	I/O1g
3	CEN	31	I/O3d	59	I/O0g
4	W_RN	32	RxDd	60	RxDg
5	A2	33	Vss	61	TxDg
6	A1	34	TxDd	62	V_{SS}
7	A0	35	RESETN	63	X1
8	DACKN	36	Gin0	64	X2
9	I/O0a	37	Gout0	65	TxDf
10	I/O1a	38	D0	66	I/O3f
11	RxDa	39	D1	67	I/O2f
12	RxDb	40	D2	68	I/O1f
13	I/O2a	41	D3	69	I/O0f
14	I/O3a	42	V_{SS}	70	TxDe
15	TxDa	43	V_{CC}	71	I/O3e
16	I/O0b	44	D4	72	I/O2e
17	I/O1b	45	D5	73	I/O1e
18	I/O2b	46	D6	74	RxDf
19	I/O3b	47	D7	75	RxDe
20	TxDb	48	Gin1	76	I/O0e
21	I/O0c	49	I/O3h	77	IRQN
22	Vss	50	I/O2h	78	A7
23	I/O1c	51	I/O1h	79	A6
24	I/O2c	52	I/O0h	80	A5
25	I/O3c	53	Vss	81	A4
26	TxDc	54	RxDh	82	A3
27	RxDc	55	TxDh	83	IACKN
28	I/O0d	56	I/O3g	84	SCLK

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature range	See Note 3	°C
T_{STG}	Storage temperature range	-65 to +150	°C
V_{CC}	Voltage from V_{DD} to GND	-0.5 to +7.0	V
V_{SS}	Voltage from any pin to GND	-0.5 to V_{CC} + 0.5	V
PD5	Power Dissipation at V_{CC} = 5.0 Volts	1	W
PD3	Power Dissipation at V_{CC} = 3.3 Volts	0.5	W

NOTES:
1. Stresses above those listed under device. This is a stress rating only

ORDERING CODE

PACKAGES	V_{CC} = 5V ±5%		DWG #
	Commercial 0°C to +70°C	Automotive -40°C to +85°C	
84-Pin Plastic Leaded Chip Carrier (PLCC)	SC26C198C1A	SC26C198A1A	0399F

NOTE: For 3.3V operation and final product specifications, please contact factory.

PIN DESCRIPTION

MNEMONIC	TYPE	DESCRIPTION
SCLK	I	Host system clock. Used to time operations in the Host Interface and clock internal logic. Must be greater than twice the frequency of highest X1, Counter/Timer, TxC (1x) or RxC (1x) input frequency.
CEN	I	Chip select: Active low. When asserted, allows I/O access to OCTART registers by host CPU. W_RN signal indicates direction.
A(7:0)	I	Address lines
A(8)	I	Address line 8 (Reserved Must be set to zero via software)
D(7:0)	I/O	8-bit bidirectional data bus. Carries command and status information between 26C198 and the host CPU. Used to convey parallel data for serial I/O between the host CPU and the 26C198
W_RN	I	Write Read not control: When high indicates that the host CPU will write to a 26C198 register or transmit FIFO. When low, indicates a read cycle. 0 = Read; 1 = Write
DACKN	O	Data Acknowledge: Active low. When asserted, it signals that the last transfer of the D lines is complete. Open drain.
IRQN	O	Interrupt Request: Active low. When asserted, indicates that the 26C198 requires service for pending interrupt(s). Open drain.
IACKN	I	Interrupt Acknowledge: Active low. When asserted, indicates that the host CPU has initiated an interrupt acknowledge cycle.
TD(a-h)	O	Transmit Data: Serial outputs from the 8 UARTs.
RD(a-h)	I	Receive Data: Serial inputs to the 8 UARTs
I/O0(a-h)	I/O	Input/Output 0: Multi-use input or output pin for the UART.
I/O1(a-h)	I/O	Input/Output 1: Multi-use input or output pin for the UART.
I/O2(a-h)	I/O	Input/Output 2: Multi-use input or output pin for the UART.
I/O3(a-h)	I/O	Input/Output 3: Multi-use input or output pin for the UART.
Gin(1:0)	I	Global general purpose inputs, available to any/all channels.
Gout0	O	Global general purpose output, available from any channel. NOTE: Gout0) is available only in packages with pin count above 84
RESETN	I	Master reset: Active Low. Must be asserted at power up and may be asserted at other times to reset and restart the system. See "Reset Conditions.
X1/CCLK	I	Crystal 1 or Communication Clock: This pin may be connected to one side of a 2-8 MHz crystal. It may alternatively be driven by an external clock in this frequency range. Standard frequency = 3.6864 MHz
X2	O	Crystal 2: If a crystal is used, this is the connection to the second terminal. If a clock signal drives X1, this pin must be left unconnected.
Power Supplies	I	5 pins for Vss, 2 pins for Vcc
NOTE: Many output pins will have very fast edges, especially when lightly loaded (less than 20 pf.) These edges may move as fast as 1 to 3 Ns fall or rise time. The user must be aware of the possible generation of ringing and reflections on improperly terminated interconnections.		

BLOCK DIAGRAM

As shown in the block diagram, the Octal UART consists of: an interrupt arbiter, host interface, timing blocks and eight UART channel blocks. The eight channels blocks operate independently, interacting only with the timing, host I/F and interrupt blocks.

OVERALL DESCRIPTION

The SC26C198 is composed of several functional blocks:

- Synchronous host interface block
- A timing block consisting of a common baud rate generator making 22 industry standard baud rates and 2 16-bit counters used for non-standard baud rate generation
- 8 identical UART channel blocks
- Interrupt arbitration system.
- I/O port control section and change of state detectors.

See "Detailed Description" below

HOST INTERFACE

The Host interface is comprised of the signal pins CEN, W/RN, IACKN, DACKN, IRQN and provides all the control for data transfer between the external and internal data buses of the host and the OCTART. The host interface operates in a synchronous mode with the system (SCLK) which has been designed for a nominal operating frequency of 33 MHz. The interface operates in either of two modes; **synchronous** or **asynchronous** to the Sclk However the bus cycle within the OCTART always takes place within four Sclk cycles after CEN is recognized.

Asynchronous bus cycle

The asynchronous mode requires one cycle of the chip select (CSN) for each read or write to the chip.

Synchronous bus cycle

In the synchronous mode a read or write will be done every four cycles of the Sclk. CSN does not require cycling. This provides a burst mode of access to the chip.

In both cases each read or write operation(s) will be completed in four (4) Sclk cycles. The difference in the two modes is only that

the asynchronous mode will not begin another bus cycle if the CEN remains active after the four internal Sclk have completed. Internally the asynchronous cycle will terminate after the four periods of Sclk regardless of how long CSN is held active

In all cases the internal action will terminate at the withdrawal of CEN.

CEN cycles shorter than multiples of four Sclk cycles minus 1 Sclk and asynchronous cycles shorter than four Sclk cycles may cause short read or write cycles and produce corrupted data transfers.

Timing Circuits

The timing block consists of a crystal oscillator, a fixed baud rate generator (BRG), a pair of 16-bit register based counters and a buffer for the System Clock.

Crystal oscillator

The crystal oscillator operates directly from a crystal, tuned between 1.0 and 8.0 MHz, connected across the X1/CCLK and X2 inputs with a minimum of external components. BRG values listed for the clock select registers correspond to a 3.6864 MHz crystal frequency. Use of a 7.3728 MHz crystal will double the Communication Clock frequencies. An external clock in the 100 KHz to 10 MHz frequency range may be connected to X1/CCLK. If an external clock is used instead of a crystal, X1/CCLK **must** be driven and X2 left floating. The X1 clock serves as the basic timing reference for the baud rate generator (BRG) and is available to the BRG timers . The X1 oscillator input may be left unused if the internal BRG is not used and the X1 signal is not selected for any counter input.

Sclk - System Clock

A clock frequency, within the limits specified in the electrical specifications, **must** be supplied for the system clock Sclk. To ensure the proper operation of internal controllers, the Sclk frequency provided, must be strictly greater than twice the frequency of X1, or any external 1x clock input. The system clock serves as the basic timing reference for the host interface and other internal circuits.

Baud Rate Generator BRG

The baud rate generator operates from the oscillator or external X1/CCLK clock input and is capable of generating 22 commonly used data communications baud rates ranging from 50 to 230.4K baud. (See Rceiver and Transmitter Clock Select Register descriptions.) All of these are available simultaneously for use by any receiver or transmitter. The clock outputs from the BRG are at 16X the actual baud rate. The two counters may be used to produce a 16X clock of any other baud rate by counting down the crystal clock an external clock or six other clock sources. The transmitter and receiver clock selectors allow the independent selection, by the receiver and transmitter, of any of these baud rates or an external timing signal.

Channel Blocks

There are eight channel blocks, each containing an I/O port control, a data format control, and a single full duplex UART channel consisting of a receiver and a transmitter with their associated 16 byte FIFOs. Each block has its own status register, interrupt status and interrupt mask registers and their interface to the interrupt arbitration system.

A highly programmable character recognition system is also included in each block. This system is used for the Xon/Xoff flow control and the multi-drop ("9 bit mode') address character recognition. It may also be used for general purpose character recognition.

Four I/O pins are provided for each channel. These pins are controlled individually to be inputs or outputs. As inputs they may be used to bring external data to the bus or as clocks for internal functions. Each of these pins in each block have "Change of State" detectors connected to them. These change detectors are used to signal a change in the signal level at the pin (Either 0 to 1 or 1 to 0) The level change on these pins must be stable for 25 to 50 Us (two edges of the 38.4Khz baud rate clock) before the detectors will signal a valid change. These are typically used for interface signals from modems to the OCTART and from there to the host.

See the description of the "UART channel" under detailed descriptions below.

Interrupt Control

The interrupt system determines when an interrupt should be asserted thorough an arbitration (or bidding) system. This arbitration is exercised over the several systems within the OCTART that may generate an interrupt. These will be referred to as "interrupt sources". There are 64 in all. In general the arbitration is based on the fill level of the receiver FIFO or the empty level of the transmitter FIFO. The FIFO levels are encoded into a four bit number which is concatenated to the channel number and source identification code. All of this is compared (via the bidding or arbitration process) to a user defined "threshold". When ever a source exceeds the numerical value of the threshold the interrupt will be generated.

At the time of interrupt acknowledge (IACKN) the source which has the highest bid (not necessarily the source that caused the interrupt to be generated) will be captured in a "Current Interrupt Register" (CIR). This register will contain the complete definition of the interrupting source: channel, type of interrupt (receiver, transmitter, change of state, etc.), and FIFO fill level. The value of the bits in the CIR are used to drive the interrupt vector and global registers such that controlling processor may be steered directly to the proper service routine. A single read operation to the CIR provides all the information needed to qualify and quantify the most common interrupt sources.

The interrupt sources for each channel are listed below.

- Transmit FIFO empty level for each channel
- Receive FIFO Fill level for each channel
- Change in break received status for each channel
- Receiver with error for each channel
- Change of state on channel input pins
- Receiver Watch-dog Time out Event
- Xon/Xoff character recognition
- Address character recognition

Associated with the interrupt system are the interrupt mask register (IMR) and the interrupt status register (ISR) resident in each UART. Programming of the IMR selects which of the above sources may enter the arbitration process. Only the bidders in the ISR whose associated bit in the IMR is set to one (1) will be permitted to enter the arbitration process. The ISR can be read by the host CPU to determine all currently active interrupting conditions. For convenience the bits of the ISR may be masked by the bits of the IMR. Whether the ISR is read unmasked or masked is controlled by the setting of bit 6 in MR1.

DETAILED DESCRIPTIONS

Receiver and Transmitter

The Octal UART has eight full duplex asynchronous receiver/transmitters. The operating frequency for the receiver and transmitter can be selected independently from the baud rate generator, the counter , or from an external input. Registers that are central to basic full-duplex operation are the mode registers (MR0, MR1 and MR2), the clock select registers (RxCSR and TxCSR), the command register (CR), the status register (SR), the transmit holding register (TxFIFO), and the receive holding register (RxFIFO).

Transmitter

The transmitter accepts parallel data from the CPU and converts it to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Each character is always "framed" by a single start bit and a stop bit that is 9/16 bit time or longer. If a new character is not available in the TxFIFO, the TxD output remains high, the "marking" position, and the TxEMT bit in the SR is set to 1.

Transmitter Status Bits

The SR (Status Register, one per UART) contains two bits that show the condition of the transmitter FIFO. These bits are TxRDY and TxEMT. TxRDY means the TxFIFO has space available for one or more bytes; TxEMT means The TxFIFO is completely empty and the last stop bit has been completed. TxEMT can not be active without TxRDY also being active. These two bits will go active upon initial enabling of the transmitter. They will extinguish on the disable or reset of the transmitter.

Transmission resumes and the TxEMT bit is cleared when the CPU loads at least one new character into the TxFIFO. The TxRDY will not extinguish until the TxFIFO is completely full. The TxRDY bit will always be active when the transmitter is enabled and there is at lease one open position in the TxFIFO.

The transmitter is disabled by reset or by a bit in the command register (CR). The transmitter must be explicitly enabled via the CR before transmission can begin. Note that characters cannot be loaded into the TxFIFO while the transmitter is disabled, hence it is necessary to enable the transmitter and then load the TxFIFO. It is not possible to load the TxFIFO and then enable the transmission.

Note the difference between transmitter disable and transmitter reset. Transmitter reset may be done by a hardware reset or a software reset issued through command 3x of the Command Register (CR). The disable is done by setting the transmitter disable bit, also in the Command Register. If the transmitter is disabled, it continues operating until the character currently being transmitted, if any, is completely sent out, including the stop bit. When reset, the transmitter stops immediately, drives the transmitter serial data output to a high level and discards any data in the TxFIFO.

Transmission of "Break"

Transmission of a break character is often needed as a synchronizing condition in a data stream. The "break" is defined as a start bit followed by all zero data bits by a zero parity bit (if parity is enabled) and a zero in the stop bit position. The forgoing is the minimum time to define a break. The transmitter can be forced to send a break (continuous low condition) by issuing a start break command via the CR. This command does not have any timing associated with it. Once issued the TxD output will be driven low (the spacing condition) and remain there until the host issues a command to "stop break" via the CR or the transmitter is issued a software or hardware reset. In normal operation the break is usually much longer than one character time.

1x and 16x modes, Transmitter

The transmitter clocking has two modes: 16x and 1x. Data is **always** sent at the 1x rate. However the logic of the transmitter may be operated with a clock that is 16 times faster than the data rate or at the same rate as the data i.e. 1x. All clocks selected internally for the transmitter (and the receiver) will be 16x clocks. Only when an external clock is selected may the transmitter logic and state machine operate in the 1x mode. The 1x or 16x clocking makes little difference in transmitter operation. (this is not true in the receiver) In the 16X clock mode the transmitter will recognize a byte in the TxFIFO within 1/16 to 2/16 bit time an thus begin transmission of the start bit; in the 1x mode this delay may be up to 2 bit times.

Transmitter FIFO

The transmitter buffer memory is a 16 byte by 8 bit ripple FIFO. The host writes characters to this buffer . The transmitter state machine reads them out in the order they were received and presents them to the transmitter shift register for serialization. The transmitter adds the required start, parity and stop bits as required the MR register programming. The start bit (always one bit time in length) is sent first followed by the least significant bit (LSB) to the most significant bit (MSB) of the character, the parity bit (if used) and the required stop bit(s).

Logic associated with the FIFO encodes the number of empty positions available in a four bit value.. This value is concatenated with the channel number and type interrupt type identifier and presented to the interrupt arbitration system. The encoding of the "positions empty" value is always 1 less than the number of available positions. Thus, an empty TxFIFO will bid with the value or 15; when full it will not bid at all; one position empty bids with the value 0. A full FIFO will not bid since a character written to it will be lost.

Normally a TxFIFO will present a bid to the arbitration system when ever it has one or more empty positions. The MR0[5:4] allow the user to modify this characterized so that bidding will not start until one of four levels (empty, 3/4 empty, 1/2 empty, not full) have been reached. As will be shown later this feature may be used to make slight improvements in the interrupt service efficiency. A similar system exists in the receiver.

Receiver

The receiver accepts serial data on the RxD pin, converts the serial input to parallel format, checks for start bit, stop bit, parity bit (if any),framing error or break condition, and presents the assembled character and its status condition to the CPU via the RxFIFO. Three status bits are FIFOed with each character received. The RxFIFO is really 11 bits wide; eight data and 3 status. Unused FIFO bits for character lengths less than 8 bits are set to zero. It is important to note that receiver logic considers the entire message to be contained within the start bit to the stop bit. It is not aware that a message may contain many characters. The receiver returns to its idle mode at the end of each stop bit! As described below it immediately begins to search for another start bit which is normally, of course, immediately forth coming.

1x and 16x mode, Receiver

The receiver operates in one of two modes; 1x and 16x. Of the two, the 16x is more robust and the preferred mode. Although the 1x mode may allow a faster data rate is does not provide for the alignment of the receiver 1x data clock to that of the transmitter. This strongly implies that the 1x clock of the remote transmitter is available to the receiver; the two devices are physically close to each other.

The 16x mode operates the receiver logic at a rate 16 times faster than the 1x data rate. This allows for validation of the start bit, validation of level changes at the receiver serial data input (RxD), and a stop bit length as short as 9/16 bit time. Of most importance in the 16x mode is the ability of the receiver logic to align the phase of the receiver 1x data clock to that of the transmitter with an accuracy of less than 1/16 bit time.

When the receiver is enabled (via the CR register) it begins looking for a high to low (mark to space) transition on the RxD input pin. If a transition is detected, an internal counter running at 16 times the data rate is reset to zero. If the RxD remains low and is still low when the counter reaches a count of 7 the receiver will consider this a valid start bit and begin assembling the character. If the RxD input returns to a high state the receiver will reject the previous high to low (mark to space) transition on the RxD input pin. This action is the "validation" of the start bit and also establishes the phase of the receiver 1x clock to that of the transmitter The counter operating at 16x the data rate is the generator for the 1x data rate clock. With the phase of the receiver 1x clock aligned to the falling of the start bit (and thus aligned to the transmitter clock) AND with a valid start bit having been verified the receiver will continue receiving bits by sampling the RxD input on the rising edge of the '1x clock that is being generated by the above mentioned counter running 16 times the data rate. Since the falling edge of the 1x clock was aligned to falling edge of the start bit then the rising of the clock will be in the 'center' of the bit cell.

This action will continue until a full character has been assembled. Parity , framing, and stop bit , and break status is then assembled and the character and its status bits are loaded to the RxFIFO At this point the receiver has finished its task for that character and will immediately begin the search for another start bit.

Receiver Status Bits

There are five (5) status bits that are evaluated with each byte (or character) received: received break, framing error, parity error, overrun error, and change of break. The first three are appended to each byte and stored in the RxFIFO. The last two are not necessarily related to the a byte being received or a byte that is in the RxFIFO. They are however developed by the receiver state machine.

The "received break" will always be associated with a zero byte in the RxFIFO. It means that zero character was a break character and not a zero data byte. The reception of a break condition will always set the "change of break" (see below) status bit in the Interrupt Status Register(ISR).

A framing error occurs when a non zero character was seen and that character has a zero in the stop bit position.

The parity error indicates that the receiver generated parity was not the same as that sent by the transmitter.

The overrun error occurs when the RxFIFO is full, the receiver shift register is full and another start bit is detected. At this moment the receiver has 17 valid characters and the start bit of the 18th has been seen. At this point the host has approximately 7/16 bit time to read a byte from the RxFIFO or the overrun condition will be set and the 18th character will overrun the 17th and the 19th the 18th and so on until an open position in the RxFIFO is seen. The meaning of the overrun is that data has been lost. Data in the RxFIFO remains valid. The receiver will begin placing characters in the RxFIFO as soon as a position becomes vacant.

Note: Precaution must be taken when reading an overrun FIFO. There will be 16 valid characters. Data will begin loading as soon as the first character is read. The 17th character will have been received as valid but it will not be known how many characters were lost between the two characters of the 16th and 17th reads of the RxFIFO.

The "Change of break" means that either a break has been detected or that the break condition has been cleared. This bit is available in the ISR. The beginning of a break will be signaled by the break change bit being set in the ISR AND the received break bit being set in the SR. At the termination of the break condition only the change of break in the ISR will be set. After the break condition is detected the termination of the break will only be recognized when the RxD input has returned to the high state for two successive edges of the 1x clock; 1/2 to 1 bit time.

The receiver is disabled by reset or via CR commands. A disabled receiver will not interrupt the host CPU under any circumstance in the **normal** mode of operation. If the receiver is in the multi-drop or special mode, it will be partially enabled and thus may cause an interrupt. Refer to section on Wake-Up and minor modes and the register description for MR1 for more information.

Receiver FIFO

The receiver buffer memory is a 16 byte ripple FIFO with three status bits appended to each data byte. The FIFO is sixteen 11 bit words. The receiver state machine gathers the bits from the receiver shift register and the status bits from the receiver logic and writes the assembled byte and status bits to the RxFIFO. Logic associated with the FIFO encodes the number of filled positions for presentation to the interrupt arbitration system. The encoding is always 1 less than the number of filled positions. Thus, a full RxFIFO will bid with the value or 15; when empty it will not bit at all; one position occupied bids with the value 0. An empty FIFO will not bid since no character is available. Normally RxFIFO will present a bid to the arbitration system when ever it has one or more filled positions. The MR2[3:2 bits allow the user to modify this characterized so that bidding will not start until one of four levels (one or more filled, 1/2 filled, 3/4 filled, full) have been reached. As will be shown later this feature may be used to make slight improvements in the interrupt service efficiency. A similar system exists in the transmitter.

RxFIFO status. Status reporting modes

The description below applies to the upper three bits in the "Status Register" These three bits are not "in the status register"; They are part of the RxFIFO. The three status bits at the top of the RxFIFO are presented as the upper three bits of the status register included in each UART.

The error status of a character , as reported by a read of the SR (status register upper three bits) can be provided in two ways, as programmed by the error mode control bit in the mode register: the "Character mode " or the "Block Mode". The block mode may be further modified (via a CR command) to set the status bits as the characters enter the FIFO or as they are read from the FIFO.

In the 'character' mode, status is provided on a character by character basis as the characters are read from the RxFIFO: the "status" applies only to the character at the top of the RxFIFO - The next character to be read

In the 'block' mode, the status provided in the SR for these three bits is the logical OR of the status for all characters coming to the top of the RxFIFO, since the last reset error command was issued. In this mode each of the status bits stored in the RxFIFO are passed through a latch as they are sequentially read. If any of the characters has an error bit set then that latch will set and remain set until reset with an "Reset Error" command from the command

register or a receiver reset. The purpose of this mode is indicating an error in the data block as opposed to an error in a character

The latch used in the block mode to indicate "problem data" is usually set as the characters are read out of the RxFIFO. Via a command in the CR the latch may be configured to set the latch as the characters are pushed (loaded to) the RxFIFO. This gives the advantage of indicating "problem data" 16 characters earlier .

In either mode, reading the SR does not affect the RxFIFO. The RxFIFO is 'popped' only when the RxFIFO is read. Therefore, the SR should be read prior to reading the corresponding data character.

If the RxFIFO is full when a new character is received, that character is held in the receive shift register until a RxFIFO position is available. At this time there are 17 valid characters in the RxFIFO. If an additional character is received while this state exists, the contents of the RxFIFO are not affected: the character previously in the shift register is lost and the overrun error status bit, SR[4], will be set upon receipt of the start bit of the new (overrunning) character.

I/O ports
Each of the eight UARTS includes four I/O ports equipped with "change of state" detectors. The pins are individually programmable for an input only function or one of three output functions. These functions are controlled by the "I/O Port Configuration Register (I/OPCR)) They will normally be used for the RTS-CTS, DTR hardware signals, Rx or Tx input or output clocks or switch inputs as well as data output from the I/OPIOR register.

It is important to note that the input circuits are always active. That is the signal on a port, whether it is derived from an internal or external source is always available to the internal circuits associated with an input on that port.

The "Change of State" (COS) detectors are sensitive to both a 1 to 0 or a 0 to 1 transition. The detectors are controlled by the internal 38.4 KHz baud rate and will signal a change when a transition has been stable for two rising edges of this clock. Thus a level on the I/O ports must be stable for 26 s to 52 s. Defining a port as an output will disable the COS detector at that port. The condition of the four I/O pins and their COS detectors is available at any time in the IPR (Input Port Register)

The control of data and COS enable for these ports is through the I/OPIOR register. This register is a read/write and gives individual control to the enabling of the change of state detectors and to the level driven by I/O pins when programmed to drive the level of the four lower bits of the I/OPIOR. It also contains the data to drive the I/O ports when programmed to output that data. A read of this register will indicate the data on the pin at the time of the read and the state of the enabled COS detectors.

General Purpose Pins
In addition to the I/O ports for each UART three other ports are provided. Two are dedicated as inputs and one is an output. The Gin1 and Gin0 are the input pins; Gout0 the output. These ports are multiplexed to nearly every functional unit in the chip. See the registers which describe the multitude of connections available for these pins. The Gout0 pin is the highly multiplexed out put and is controlled by four (4) registers: GPOSR, GPOR, GPOC and GPOD. The Gin0 and Gin1 pins are available to the receivers and transmitters, BRG counters and the Gout0 pin

Global Registers
The "Global Registers", 19 in all, are driven by the interrupt system. These are not real hardware devices. They are defined by the content of the CIR (Current Interrupt Register) as a result of an interrupt arbitration. In other words they are indirect registers pointed to by the content of the CIR. The list of global register follows:

- GIBCR The byte count of the interrupting FIFO
- GICR Channel number of the interrupting channel
- GITR Type identification of interrupting channel
- GRxFIFO Pointer to the interrupting receiver FIFO
- GTxFIFO Pointer to the interrupting transmitter FIFO

A read of the GRxFIFO will give the content of the RxFIFO that presently has the highest bid value. The purpose of this system is to enhance the efficiency of the interrupt system. The global registers and the CIR update procedure are further described in the *Interrupt Arbitration* system

Character Recognition
Note: Character recognition is further described in the *Minor Modes of Operation.*

Character recognition is specific to each of the eight UARTS. Three programmable charters are provided for the character recognition for each cahnnel. The three are general purpose in nature and may be set to only cause an interrupt or to initiate some rather complex operations specific to "Multi-drop" address recognition or in-band Xon/Xoff flow control.

Character recognition is accomplished via CAM memory. The Content Addressable Memory continually examines the incoming data stream. Upon the recognition of a control character appropriate bits are set in the Xon/Xoff Interrupt Status Register and initiates any other of the automatic sequences that may have enabled via the MR0 register.

Xon Xoff Characters

The programming of these characters is usually done individually. However a method has been provided to write to all of registers in one operation. There are "Gang Load" and a "Gang Write" commands provided in the channel a Command Register. When these commands are executed all register are programmed with the same character. The "write" command load a used defined character; the 'Load" command loads the standard Xon/Xoff characters. Xon is x'11, Xoff is x'13. Any enabling of the Xon/Xoff functions will use the contents of the Xon and Xoff character registers as the basis on which recognition is predicated.

Multidrop or Wake up or 9 bit mode
This mode is used to address a particular UART among a group connected to the same serial data source. Normally it is accomplished by redefining the meaning of the parity bit such that it indicates a character as address or data. While this method is fully supported in the SC26C198 it also supports recognition of the character itself. Upon recognition of its address the receiver will be enabled and data pushed onto the RxFIFO.

Further the Address recognition has the ability, if so programmed, to disable (not reset) the receiver when an address is seen that is not recognized as its own. The particular features of "Auto Wake and Auto Doze" are described in the detail descriptions below.

Note: Care should be taken in the programming of the character recognition registers. Programming x'00, for

example, may result in a break condition being recognized as a control character. This will be further complicated when binary data is being processed.

Interrupt Arbitration and IRQN generation

Interrupt arbitration is the process used to determine that an interrupt request should be presented to the host. The arbitration is carried out between the "Interrupt Threshold" and the "sources" whose interrupt bidding is enabled by the IMR. The interrupt threshold is part of the ICR (Interrupt Control Register) and is a value programmed by the user. The "sources" present a value derived from the channel number, type of source, FIFO fill level, and programmable value to the arbiter.. Only when the value of an enabled source exceeds the threshold value in the interrupt control register will the interrupt request (IRQN) be asserted.

Following assertion of the IRQN the host will either assert IACKN(Interrupt Acknowledge) or will use the command to "Update the CIR". At the time either action is taken the CIR will capture the value of the source that is prevailing in the arbitration process. (Call this value the winning bid)

The value in the CIR is the central quantity that results from the arbitration. It contains the identity of the interrupting channel, the type of interrupt in that channel (Rx, Tx, COS etc.) the fill levels of the Rx or Ts FIFOs and , in the case of an Rx interrupt an indicator of error data or good data. It also drives the Global Registers associated with the interrupt. **Most importantly it drives the modification of the Interrupt Vector.**

The arbitration process is driven by the Sclk. It scans the 10 bits of the arbitration bus at the Sclk rate developing a value for the CIR every 22 Sclk cycles. New arbitration values presented to the arbitration block during an arbitration cycle will be evaluated in the next arbitration cycle.

For sources other than receiver and transmitters the user may set the high order bits of an interrupt source's bid value, thus tailoring the relative priority of the interrupt sources. The priority of the receivers and transmitters is controlled by the fill level of their respective FIFOS. The more filled spaces in the RxFIFO the higher the bid value; the more empty spaces in the TxFIFO the higher its priority. Channels whose programmable high order bits are set will be given interrupt priority higher than those with zeros in their high order bits , thus allowing increased flexibility. The transmitter and receiver bid values contain the character counts of the associated FIFOs as high order bits in the bid value. Thus, as a receiver's RxFIFO fills, it bids with a progressively higher priority for interrupt service. Similarly, as empty space in a transmitter's TxFIFO increases, its interrupt arbitration priority increases.

IACK Cycle

When the host CPU responds to the interrupt, it will generate an IACK cycle to determine the interrupting device and as much detail about the interrupt as possible. When IACKN asserts, the last valid interrupt number is frozen in the CIR. The value captured presents most of the important details of the highest priority interrupt. The Octal UART can respond to the IACK cycle with an interrupt vector. The interrupt vector may be a fixed value, the content of the Interrupt Vector Register, or ,when "Interrupt Vector Modification is enabled via ICR, it may contain codes for the interrupt type and/or interrupting channel. This allows the interrupt vector to steer the interrupt service **directly** to the proper service routine. The interrupt value captured in the CIR remains until another IACK cycle occurs or until an "Update CIR" command is given to the Octal UART. The interrupting channel and interrupt type fields of the CIR set the current "interrupt context" of the Octal UART. The channel component of the interrupt context allows the use of Global Interrupt Information registers that appear at fixed positions in the register address map. For instance, a read of the Global RxFIFO, GRxFIFO, will read the channel d RxFIFO while the CIR interrupt context is channel d receiver. At another time, the GRxFIFO may read the channel h RxFIFO (CIR holds a channel h receiver interrupt) and so on. Global registers exist to facilitate qualifying the interrupt parameters and for writing to and reading from FIFOs without explicitly addressing them.

Polling

Many users prefer polled to interrupt driven service where there are a large number of fast data channels and/or the host CPU's other interrupt overhead is low. The Octal UART is functional in this environment.

The most efficient method of polling is the use of the "update CIR" command (with the interrupt threshold set to zero) followed by a read of the CIR. This dummy write cycle will perform the CIR lock function that an IACK falling edge would accomplish in an interrupt driven system. A subsequent read of the CIR, at the same address, will give information about an interrupt, if any. If the CIR contains 0s, no interrupt is awaiting service. If the value is non-zero, the fields of the CIR may be decoded for type, channel and character count information. Optionally, the global interrupt registers may be read for particular information about the interrupt status; use of the global Rx and Tx registers for data transfer as appropriate. The interrupt context will remain in the CIR until another update CIR command or an IACKN cycle is initiated by the host CPU occurs.

Traditional methods of polling status registers may also be used. They of course are less efficient but give the most variable and quickest method of changing the order in which interrupt sources are evaluated.

Enabling and Activating Interrupt sources

An interrupt source becomes enabled when its interrupt capability is set by writing to the Interrupt Mask Register, IMR. An interrupt source can never generate an IRQN or have its "bid" or interrupt number appear in the CIR unless the source has been enabled by the appropriate bit in an IMR.

An interrupt source is active if it is presenting its bid to the interrupt arbiter for evaluation. Most sources have simple activation requirements. The watch-dog timer, break received, Xon/Xoff or Address Recognition and change of state interrupts become active when these events occur.

The transmitter and receiver functions have additional controls to modify the condition upon which the initiation of interrupt "bidding" begins: the TxINT and RxINT fields of the MR registers. These fields can be used to start bidding or arbitration when the RxFIFO is not empty, 50% full, 75% full or 100% full. For the transmitter it is not full, 50% empty, 75% empty and empty.

Example: To increase the probability of transferring the contents of a nearly full RxFIFO, do not allow it to start bidding until 50% or 75% full. This will prevent its relatively high priority from winning the arbitration process at low fill levels. A high threshold level could accomplish the same thing, but may also mask out low priority interrupt sources that must be serviced. Note that for fast channels this configuration must be used with caution since it reduces the time the host CPU has to respond to the interrupt request before receiver overrun occurs.

Table 1.

Type	B9	B8	B7	B6	B5	B4	B3	Bits 2:0
Receiver w/o error	RxFIFO Byte Count -1				0	0	1	Channel No
Receiver w/ error	RxFIFO Byte Count -1				1	0	1	Channel No
Transmitter	0	TxFIFO Byte Count -1				0	0	Channel No
Change of Break	Programmed Field			0	0	1	0	Channel No
Change of State	Programmed Field			0	1	1	0	Channel No
Xon/Xoff	Programmed Field			0	1	1	1	Channel No
Address Recognition	Programmed Field			0	0	1	1	Channel No
Receiver Watch-dog	RxFIFO Byte Count -1				As Rx Above			Channel No
Threshold	Bits 6:0 of Interrupt Control Register							000

Note several characteristics of the above table in bits 6:3. These bits contain the identification of the bidding source as indicated below:

x001	Receiver without error
x101	Receiver with error
xx00	Transmitter
0010	Change of Break
0110	Change of State on I/O Ports
0111	Xon/Xoff Event
0011	Address Recognition

Setting interrupt priorities

The bid or interrupt number presented to the interrupt arbiter is composed of character counts, channel codes, fixed and programmable bit fields. The interrupt numbers are generated for various interrupt sources as shown in the table below:

The codes form bits 6:3 drive part of the interrupt vector modification and the Global Interrupt Type Register. The codes are unique to each source type and Identify them completely. The channel numbering progresses from "a" to "h" as the binary numbers 000 to 111 and identify the interrupting channel uniquely. As the channels arbitrate "h" will have the highest bidding value and "a" the lowest

Note that the transmitter byte count is off-set from that of the receiver by one bit. This is to give the receiver more authority in the arbitration since and over-run receiver corrupts the message but an under-run transmitter is not harmful. This puts some constraints on how the threshold value is selected. If a threshold is chosen that has its MSB set then a transmitter can never generate an interrupt! Of course the counter point to this is the desire to set the interrupt threshold high so interrupts occur only when a maximum or near maximum number of characters may be transferred. To give some control over this dilemma control bits have been provided in the MR registers of each channel to individually control when a receiver or transmitter may interrupt. The use of these bits will prevent a receiver or a transmitter from interrupting the arbitration process even though its FIFO fill level is above that indicated by the threshold value set. The bits in the MR register are named TxINT (MR0[5:4]) and RxINT (MR2[3:2])

The watch-dog is included in the table above to show that it affects the arbitration. It does not have an identity of its own. A barking watch-dog will prevent **any other source type** from entering the arbitration process except **enabled** receivers; including the threshold! The threshold is effectively set to zero when the watch-dog times out. The receivers arbitrate among them selves and the one with the highest fill level will win the process. Note that the receiver wining the bit may not be the one that caused the watch-dog to bark.

The fields labeled "Programmed Field" are the contents of the Bidding Control Registers, BCRs, for these sources. Setting these bits to high values can elevate the interrupt importance of the sources they represent to values almost as high as a full receiver.

There is a single arbiter interrupt number that is not associated with any of the UART channels. It is the "Threshold Value" and is comprised of 7 bits from the Interrupt Control Register, ICR, and three zeros in the channel field. **It is only when the threshold value is exceeded that the IRQN will be asserted.** If the threshold bidding is larger than any other bidder, then the CIR will load with zeros and the IRQN output will be negated. Because the channels are numbered from 0 to 7 (A to H) channel 7 will win the bid when all other parts of the bid are equal.

Note: Based on this coding for the receiver and transmitter, a transmitter would not win a bid in the situation where Count Field = 0 unless the threshold value is equal or less than 0000111. A single empty slot is left in the TxFIFO or a single filled slot in the RxFIFO will bid with a value of zero.

MODES OF OPERATION

Major Modes

Four major modes of operation are provided and are controlled by MR2[7:6].Three of these may be considered diagnostic. See the MR2 register description

The normal mode is the usual mode for data I/O operation. Most reception and transmission will use the normal mode.

In the auto echo mode, the transmitter automatically re transmits any character captured by the channel's receiver. The receiver 1x clock is used for the transmitter. This mode returns the received data back to the sending station one bit time delayed from its departure. Receiver to host communication is normal. Host to transmitter communication has no meaning.

The loop back modes are for diagnostic purposes.

In local loop back, any character pushed into the TxFIFO will be captured, as it would be sent, by the receiver. The data does not actually appear on the TxD outputs, however. This allows the local host to check what the remote receiver would see using this simulated transmission mode. The communication between the transmitter and receiver is entirely within the UART - it is essentially "talking to itself".

The remote loop back is similar to auto echo except that the characters are not sent to the local CPU, nor is the receiver status updated. The receiver and its host will not be participating in any diagnostics.

Minor Modes

The minor modes provide additional features within the major modes. In general the minor modes provide a reduction in the control burden and a less stringent interrupt latency time for the host processor. These modes could be invoked in all of the major modes.. However it may not be reasonable in many situations.

Watch-dog Timer Time-out Mode

Each receiver in the Octal UART is equipped with a watch-dog timer that is enabled by the "Watch-dog Timer Enable Register (WTER). The watch-dog "barks" (times out) if 64 counts of the receiver clock (64 bit times) elapse with no RxFIFO activity. RxFIFO events are a read of the RxFIFO or GRxFIFO, or the push of a received character into the RxFIFO. The timer resets when the (G)RxFIFO is read or if another character is pushed into the RxFIFO. The receiver watch-dog timer is included to allow detection of the very last character(s) of a received message that may be waiting in the RxFIFO, but are too few in number to successfully initiate an interrupt. The watch-dog timer is enabled for counting if the channel's bit in the Watch Dog Timer Control Register (WDTCR) is set. Note: a read of the GRxFIFO will reset the watch-dog timer of only the channel specified in the current interrupt context. Other watch-dogs are unaffected.

The watch-dog timer may generate an input to the interrupt arbiter if IMR[6] is set. The status of the Watch-dog timer can be seen as Bit 6 of the Interrupt Status Register, ISR[6]. When a Watch-dog timer that is programmed to generate an interrupt times out it enters the arbitration process. It will then only allow receivers to enter the enter the arbitration. All other sources are bidding sources are disabled. The receivers arbitrate only amongst themselves.. The receiver only interrupt mode of the interrupt arbiter continues until the last watch-dog timer event has been serviced. While in the receiver only interrupt mode, the control of the interrupt threshold level is also disabled. The receivers arbitrate only between themselves; The receiver with the most FIFO positions filled will win the bid. Hence the user need not reduce the bidding threshold level in the ICR to see the interrupt from a nearly empty RxFIFO that has a watch-dog time-out.

Note: All receivers bid in this situation. There is no increase in the probability of receiver being services causing the overrun of another receiver since they will still have priority based upon received character count.

The interrupt will be cleared automatically upon the push of the next character received or when the RxFIFO or GRxFIFO is read. The ICR is unaffected by the watch-dog time-out interrupt and normal interrupt threshold level sensing resumes after the last watch-dog timer event has been processed. If other interrupt sources are active, the IRQN pin may remain low.

Wake Up Mode

The SC26C198 provides two modes of this common asynchronous "party line" protocol: the new automatic mode with 3 sub modes and the default Host operated mode. The automatic mode has several sub modes (see below). In the full automatic the internal state machine devoted to this function will handle all operations associated with address recognition, data handling, receiver enables and disables. In both modes the meaning of the parity bit is changed. It is often referred to as the A/D bit or the address/data bit. It is used to indicate whether the byte presently in the receiver shift register is an "address" byte or a "data byte". A "1" usually means address; a "0" data.

Its purpose is to allow several receivers connected to the same data source to be individually addressed. Of course addressing could be by group also. Normally the "Master" would send an address byte to all receivers "listening" The receiver would then recognize its address and enable itself receiving the following data stream. Upon receipt of an address not its own it would then disable itself. As described below appropriate status bits are available to describe the operation.

Enabling the Wake Up mode

This mode is selected by programming bits MR1[4:3] to '11'. The sub modes are controlled by bits 6, 1, 0 in the MR0 register. Bit 6 controls the loading of the address byte to the RxFIFO and MR0[1:0] determines the sub mode as shown in the following table.

- MR0[1:0] = 00 Normal Wake Up Mode (default)
- MR0[1:0] = 01 Auto wake. Enable Rx on address recognition, mine
- MR0[1:0] = 10 Auto Doze. Disable Rx on address recognition, not mine
- MR0[1:0] = 11 Auto wake and doze, Both modes above.

Upon recognition of the its assigned address, in the Auto Wake mode, the local receiver will be enabled and normal receiver communications with the host will be established. Upon recognition of an address character that is not its own , in the Auto Doze mode, the receiver will be disabled and the address just received either discarded or pushed to the RxFIFO depending on the programming of MR0[6]. The programming of MR0[1:0] to 11 will enable both the auto wake and auto doze features.

Normal Wake up (The default configuration)

In the default configuration for this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, whose receivers are normally disabled, examine the received data stream and interrupts the CPU (by setting RxRDY) only upon receipt of an address character. The CPU (host) compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again. A transmitted character consists of a start bit, the programmed number of data bits, an address/data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1[2]: MR1[2] = 0 transmits a zero in the A/D bit position which identifies the corresponding data bits as **data**; MR1[2] = 1 transmits a one in the A/D bit position which identifies the corresponding data bits as an **address**. The CPU should program the mode register prior to loading the corresponding data bits into the TxFIFO.

While in this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RxFIFO if the received A/D bit is a one, but discards the received character if the received A/D bit is a zero. If the receiver is enabled, all received

characters are transferred to the CPU via the RxFIFO. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SR[5]). Framing error, overrun error, and break detect operate normally whether or not the receiver is enabled.

Automatic operation, wake-up and doze

The automatic configuration for this mode uses on-board comparators to examine incoming address characters. Each UART channel may be assigned a unique address character. See the address register map and the description of the Address Recognition Character Register (ARCR). The device may be programmed to automatically awaken a sleeping receiver and/or disable an active receiver based upon address characters received. The operation of the basic receiver is the same as described above for the default mode of wake-up operation except that the CPU need not be interrupted to make a change in the receiver status.

Three bits in the Mode Register 0, (MR0), control the address recognition operation. MR0[6] controls the RxFIFO operation of the received character; MR0[1:0] controls the wake up mode options. If MR0[6] is set the address character will be pushed onto the RxFIFO, otherwise the character will be discarded. The MR0[1:0] bits set the options as follows: A b'00 in this field, the default or power-on condition, puts the device in the default (CPU controlled) wake up mode of operation as described above. The auto-wake mode, enabled if MR0[0] is set, will cause the dedicated comparators to examine each address character presented by the receiver. If the received character matches the reference character in ARCR, the receiver will be enabled and all subsequent characters will be FIFOed until another address event occurs or the host CPU disables the receiver explicitly. The auto doze mode, enabled if MR0[1] is set, will automatically disable the receiver if an address is received that does not match the reference character in the ARCR.

The UART channel can present the address recognition event to the interrupt arbiter for IRQN generation. The IRQN generation may be masked by setting bit 5 of the Interrupt Mask Register, IMR. The bid level of an address recognition event is controlled by the Bidding Control Register, BCRA, of the channel.

Note: To ensure proper operation, the host CPU must clear any pending Address Recognition interrupt before enabling a disabled receiver operating in the Special or Wake-up mode. This may be accomplished via the CR commands to clear the Address Interrupt or by resetting the receiver.

Xon/Xoff Operation

Since the receiving FIFO resources in the Octal UART are limited, some means of controlling a remote transmitter is desirable in order to lessen the probability of receiver overrun. The Octal UART provides two methods of controlling the data flow. A hardware assisted means of accomplishing control, the so-called out-of-band flow control, and an in-band flow control method.

The out-of-band flow control is implemented through the CTSN-RTSN signaling via the I/O ports. The operation of these hardware handshake signals is described in the receiver and transmitter discussions. In-band flow control is a protocol for controlling a remote transmitter by embedding special characters within the message stream, itself. Two characters, Xon and Xoff, which do not represent normal printable characters take on flow control definitions when the Xon/Xoff capability is enabled. Flow control characters received may be used to gate the channel transmitter on and off. This activity is referred to as Auto-transmitter mode. To protect the channel receiver from overrun, fixed fill levels (hardware set at 12 characters) of the RxFIFO may be ernployed to automatically insert Xon/Xoff characters in the transmitter's data stream. This mode of operation is referred to as auto-receiver mode Commands issued by the host CPU via the CR can simulate all these conditions

Auto-transmitter mode

When a channel receiver pushes an Xoff character into the RxFIFO, the channel transmitter will finish transmission of the current character and then stop transmitting. A transmitter so idled can be restarted by the receipt of an Xon character by the receiver, by an Xoff resume command to the CR or by a hardware or software reset. The last option results in the loss of the un-transmitted contents of the TxFIFO.

While idle, the TxFIFO may be written to and the transmitter continues to present its fill level to the interrupt arbiter.

Use of '00' as an Xon/Xoff character is complicated by the Receiver break operation which pushes a '00' character on the RxFIFO. The Xon/Xoff character detectors do not discriminate this case from an Xon/Xoff character received via the RxD pin.

Note: to be recognized as an Xon or Xoff character, the receiver must have room in the RxFIFO to accommodate the character. An Xon/Xoff character that is received resulting in a receiver overrun does not effect the transmitter nor is it pushed into the RxFIFO, regardless of the state of the Xon/Xoff transparency bit, MR0(7).

Note: Xon /Xoff characters

The Xon/Xoff characters with errors will be accepted as valid. The user has the option sending or not sending these characters to the FIFO. Error bits associated with Xon/Xoff will be stored normally to the receiver FIFO.

The channel's transmitter may be programmed to automatically transmit an Xoff character without host CPU intervention when the RxFIFO fill level exceeds a fixed limit (12). In this mode, it will conversely transmit an Xon character when the RxFIFO level drops below a second fixed limit (8). A character from the TxFIFO that has been loaded into the Tx shift register will continue to transmit. Character(s) in the TxFIFO that have not been popped are unaffected by the Xon or Xoff transmission. They will be transmitted after the Xon/Xoff activity concludes.

If the fill level condition that initiates Xon activity negates before the flow control character can begin transmission, the flow character transmission will not occur, i.e. either of the following sequences may be transmitted depending on the timing of level changes with respect to the normal character times:

Character Xoff Xon Character

Character Character

Hardware keeps track of Xoff characters sent that are not rescinded by an Xon. This logic is reset by writing MR0(3) to '0'. If the user drops out of Auto-receiver mode while the XISR shows Xon as the last character sent, the Xon/Xoff logic will **not** automatically send the negating Xon.

Host mode

When neither the auto-receiver nor auto-transmitter modes are set, the Xon/Xoff logic is operating in the host mode. In host mode, all activity of the Xon/Xoff logic is initiated by commands to the CRX command forces the transmitter to disable exactly as though an Xoff character had been received by the RxFIFO. The transmitter will remain disabled until the chip is reset or the CRXoffre (re for resume) command is given. In particular, reception of an Xon or

disabling/re enabling the transmitter will **NOT** cause resumption of transmission. Redundant CRTX-- commands, i.e. CRTXon CRTXon, are harmless, although they waste time. A CRTXon may be used to cancel a CRTXoff (and visa versa) but both may be transmitted depending on the timing with the transmit state machine. The kill CRTX command can be used to cleanly terminate any CRTX commands pending with the minimum impact on the transmitter.

Note: In **no** case will an Xon/Xoff character transmission be aborted. Once the character is loaded into the TX Shift Register, transmission continues until completion or a chip reset is encountered.

The kill CRTX command has no effect in either of the Auto modes.

Mode control
Xon/Xoff mode control is accomplished via the MR0. Bits 3 and 2 reset to zero resulting in all Xon/Xoff processing being disabled. If MR0[2] is set, the transmitter may be gated by Xon/Xoff characters received. If MR0[3] is set, the transmitter will transmit Xon and Xoff when triggered by attainment of fixed fill levels in the channel RxFIFO. The MR0[7] bit also has an Xon/Xoff function control. If this bit is set, a received Xon or Xoff character is not pushed into the RxFIFO. If cleared, the power-on and reset default, the received Xon or Xoff character is pushed onto the RxFIFO for examination by the host CPU. The MR0(7) function operates regardless of the value in MR0(3:2)

Xon/Xoff Interrupts
The Xon/Xoff logic generates interrupts **only** in response to recognizing either of the characters in the XonCR or XoffCR. The transmitter activity initiated by the Xon/Xoff logic or any CR command does **not** generate an interrupt. The character comparators operate regardless of the value in MR0(3:2). Hence the comparators may be used as general purpose character detectors by setting MR0(3:2)='00' and enabling the Xon/Xoff interrupt in the IMR.

The Octal UART can present the Xon/Xoff recognition event to the interrupt arbiter for IRQN generation. The IRQN generation may be masked by setting bit 4 of the Interrupt Mask Register, IMR. The bid level of an Xon/Xoff recognition event is controlled by the Bidding Control Register X, BCRX, of the channel. The interrupt status can be examined in ISR[4]. If cleared, no Xon/Xoff recognition event is interrupting. If set, an Xon or Xoff recognition event has been detected. The X Interrupt Status Register, XISR, can be read for details of the interrupt and to examine other, non-interrupting, status of the Xon/Xoff logic. Refer to the XISR in the Register Descriptions.

REGISTER DESCRIPTIONS

The operation of the Octal UART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the host CPU. The Octal UART has two modes of addressing available to the user, initialization and normal. The device powers on and resets into the initialization mode. In this mode, the elements of host interface setup, interrupt arbitration, I/O Port Configuration and UART channel definition that do not change in normal operation may be set. The address map for this mode is shown in the Register Map, Chip Initialization Phase. The normal mode allows addressing of common UART status and control registers that will need frequent access in normal operation. The addressing mode may be set at any time through writing bit 7 of the Global Chip Configuration Register (GCCR[7]) or through a Command Register write to CRa .

MR - Mode Registers

The user must exercise caution when changing the mode of running receivers, transmitters or BRG counter/timers. The selected mode will be activated immediately upon selection, even if this occurs during the reception or transmission of a character. It is also possible to disrupt internal controllers by changing modes at critical times, thus rendering later transmission or reception faulty or impossible. An exception to this policy is switching from auto-echo or remote loop back modes to normal mode. If the deselection occurs just after the receiver has sampled the stop bit (in most cases indicated by the assertion of the channel's RxRDY bit) and the transmitter is enabled, the transmitter will remain in auto-echo mode until the end of the transmission of the stop bit.

Bit 6 controls the operation of the host interface logic. If reset, the power on/reset default, the host interface can accommodate arbitrarily long bus I/O cycles. If the bit is set, the OCTAL UART expects four Sclk cycle bus I/O operations similar to those produced by an i80386 processor in non-pipelined mode. The major differences in these modes are observed in the DACKN pin function. In sync mode, no negation of CEN is required between cycles.

The IVC field controls if and how an interrupt acknowledge vector will be formed for the Octal UART. If b'00, no vector will be presented during an IACK cycle. If the field contains a b'01, the contents of the IVR, Interrupt Vector Register, will be presented as the interrupt vector without modification. If IVC = b'10, the channel code will replace the 3 LSBs of the IVR; if IVC = b'11 then a modified interrupt type and channel code replace the 5 LSBs of the IVR.

Note: The modified type field is:
10 Receiver w/o error
11 Receiver with error
01 Transmitter
00 All remaining sources

Bit 0 controls the power down function. During power down the internal oscillator is disabled, interrupt arbitration and all data transmission/reception activities cease, and all processing for input change detection, BRG counter/timers and Address/Xon./Xoff recognition is disabled.

To switch from the asynchronous to the synchronous bus cycle mode, a single write operation to the GCCR, terminated by a negation of the CEN pin, is required. This cycle may be 4 cycles long if the setup time of the CEN edge to Sclk can be guaranteed. The host CPU must ensure that a minimum of two Sclk cycles elapse before the initiation of the next (synchronous) bus cycle(s).

A hardware or software reset is recommended for the unlikely requirement of returning to the asynchronous bus cycling mode.

Table 2. GCCR - Global Configuration Control Register

Bit 7	Bit 6	Bit 5:3	Bit 2:1	Bit 0
Reserved	sync bus cycles	Reserved	IVC, Interrupt Vector Control	Power Down Mode
Must be set to 0	0 - async cycles 1 - sync, non-pipe-lined cycle		00 - no interrupt vector 01 - IVR 10 - IVR + channel code 11 - IVR + interrupt type + channel code	0 - Device enabled 1 - Power down

Table 3. MR0 - Mode Register 0

Bit 7	Bit 6	Bit 5:4	Bit 3:2	Bit 1:0
Xon/Xoff transparency	Addr Recognition transparency	TxINT	In-band flow control mode	Address Recognition control
0 - flow control characters received are pushed onto the RxFIFO 1 - flow control characters received are not pushed onto the RxFIFO	0 - Address characters received are pushed to RxFIFO 1 - Address characters received are not pushed onto the RxFIFO	TxFIFO interrupt level control 00 - empty 01 - æ empty 10 - Ω empty 11 - not full	00 - host mode, only the host CPU may initiate flow control actions through the CR 01 - Auto Transmitter flow control 10 - Auto Receiver flow control 11 - Auto Receiver and Transmitter flow control	00 - none 01 - Auto wake 10 - Auto doze 11 - Auto wake and auto doze

Table 4. MR1 - Mode Register 1

Bit 7	Bit 6	Bit 5	Bit 4:3	Bit 2	Bit 1:0
RxRTS Control	ISR Read Mode	Error Mode	Parity Mode	Parity Type	Bits per Character
0 - off 1 - on	0 - ISR unmasked 1 - ISR masked	0 = Character 1 = Block	00 - With Parity 01 - Force parity 10 - No parity 11 - Special Mode	0 = Even 1 = Odd	00 - 5 01 - 6 10 - 7 11 - 8

MR0[7:6] Control the handling of recognized Xon/Xoff or Address characters. If set, the character codes are placed on the RxFIFO along with their status bits just as ordinary characters are. If the character is not pushed onto the RxFIFO, its received status will be lost unless the receiver is operating in the block error mode, see MR1[5] and the general discussion on receiver error handling. Interrupt processing is not effected by the setting of these bits.

MR0[5:4] Controls the fill level at which a transmitter begins to present its interrupt number to the interrupt arbitration logic. Use of a low fill level minimizes the number of interrupts generated and maximizes the number of transmit characters per interrupt cycle. It also increases the probability that the transmitter will go idle for lack of characters in the TxFIFO.

MR0[3:2] control the Xon/Xoff processing logic. Auto Transmitter flow control allows the gating of Transmitter activity by Xon/Xoff characters received by the Channel's receiver. Auto Receiver flow control causes the Transmitter to emit an Xoff character when the RxFIFO has loaded to a depth of 12 characters. Draining the RxFIFO to a level of 8 or less causes the Transmitter to emit an Xon character. All transmissions require no host involvement. A setting other than b'00 in this field precludes the use of the command register to transmit Xon/Xoff characters.

Note: Interrupt generation in Xon/Xoff processing is controlled by the IMRs (Interrupt Mask Register) of the individual channels. The interrupt may be cleared by a read of the XISR, the Xon/Xoff Interrupt Status Register. Receipt of a flow control character will always generate an interrupt if the IMR is so programmed. The MR0[3:2] bits have effect on the automatic aspects of flow control only, not the interrupt generation.

MR0[1:0] This field controls the operation of the Address recognition logic. If the device is not operating in the special or "wake-up" mode, this hardware may be used as a general purpose character detector by choosing any combination except b'00. Interrupt generation is controlled by the channel IMR. The interrupt may be cleared by a read of the XISR, the Xon/Xoff Interrupt Status Register.

MR1[7] - Receiver Request to Send Control

This bit controls the deactivation of the RTSN output (I/O2) by the receiver. This output is asserted and negated by commands applied via the command register. MR1[7] = 1 causes RTSN to be automatically negated upon receipt of a valid start bit if the receiver FIFO is _ full or greater. RTSN is reasserted when an the FIFO fill level falls below _ full. This constitutes a change from previous members of Philips (Signets)' UART families where the RTS function triggered on FIFO full. This behavior caused problems with PC UARTs that could not stop transmission at the proper time. . The RTS feature can be used to prevent overrun in the receiver, by using the RTSN output signal, to control the CTS input of the transmitting device.

MR1[6] - Interrupt Status Masking

This bit controls the readout mode of the Interrupt Status Register, ISR. If set, the ISR reads the current status masked by the IMR, i.e. only interrupt sources enabled in the IMR can ever show a '1' in the ISR. If cleared, the ISR shows the current status of the interrupt source without regard to the Interrupt Mask setting.

MR1[5] - Error Mode Select

This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break). In the character mode, status is provided on a character by character basis; the status applies only to the character at. the bottom of the FIFO. In the block mode, the status provided in the SR for these bits is the accumulation (logical OR) of

the status for all characters coming to the top of the FIFO, since the last reset error command was issued.

MR1[4:3] - Parity Mode Select

If 'with parity' or 'force parity' is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR1[4:3] = 11 selects the channel to operate in the special wake up mode.

MR1[2] - Parity Type Select

This bit sets the parity type (odd or even) if the 'with parity' mode is programmed by MR1[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special 'wake up' mode, it selects the polarity of the A/D bit. The parity bit is used to an address or data byte in the 'wake up' mode.

MR1[1:0] - Bits per Character Select

This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, or stop bits.

Table 5. MR2 - Mode Register 2

Bits 7:6	Bit 5	Bit 4	Bit 3:2	Bit 1:0
Channel Mode	TxRTS Control	CTS Enable Tx	RxINT	Stop Length
00 = normal 01 = Auto echo 10 = Local loop 11 = Remote loop	0 = No 1 = Yes	0 = No 1 = Yes	00 = RRDY 01 = Half Full 10 = 3/4 Full 11 = Full	00 = 1.0 01 = 1.5 10 = 2.0 11 = 9/16

The MR2 register provides basic channel setup control that may need more frequent updating.

MR2[7:6] - Mode Select

The Octal UART can operate in one of four modes: MR2[7:6] = b'00 is the normal mode, with the transmitter and receiver operating independently.

MR2[7:6] = b'01 places the channel in the automatic echo mode, which automatically re transmits the received data. The following conditions are true while in automatic echo mode:

- Received data is re-clocked and re-transmitted on the TxD output.
- The receive clock is used for the transmitter.
- The receiver must be enabled, but the transmitter need not be enabled.
- The TxRDY and TxEMT status bits are inactive.
- The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.
- Character framing is checked, but the stop bits are retransmitted as received.
- A received break is echoed as received until the next valid start bit is detected.

CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be selected.

MR2[7:6] = b'10 selects local loop back mode. In this mode:

- The transmitter output is internally connected to the receiver input.
- The transmit clock is used for the receiver.
- The TxD output is held high.
- The RxD input is ignored.
- The transmitter must be enabled, but the receiver need not be enabled.
- CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loop back mode, selected by MR2[7:6] = b'11. In this mode:

- Received data is re-clocked and re-transmitted on the TxD output.
- The receive clock is used for the transmitter.
- Received data is not sent to the local CPU, and the error status conditions are inactive.
- The received parity is not checked and is not regenerated for transmission, i.e., the transmitted parity bit is as received.
- The receiver must be enabled, but the transmitter need not be enabled.
- Character framing is not checked, and the stop bits are retransmitted as received.
- A received break is echoed as received until the next valid start bit is detected.

MR2[5] Transmitter Request to Send Control

This bit controls the deactivation of the RTSN output (I/O2) by the transmitter. This output is manually asserted and negated by appropriate commands issued via the command register. MR2[5] = 1 causes RTSN to be reset automatically one bit time after the characters in the transmit shift register and in the TxFIFO (if any) are completely transmitted (includes the programmed number of stop bits if the transmitter is not enabled). This feature can be used to automatically terminate the transmission of a message as follows:

- Program auto reset mode: MR2[5]= 1.
- Enable transmitter.
- Assert RTSN via command.
- Send message.
- Verify the next to last character of the message is being sent by waiting until transmitter ready is asserted. Disable transmitter after the last character is loaded into the TxFIFO.
- The last character will be transmitted and RTSN will be reset one bit time after the last stop bit.

MR2[4] - Clear to Send Control

The state of this bit determines if the CTSN input (I/O0) controls the operation of the transmitter. If this bit is 0, CTSN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSN each time it is ready to begin sending a character. If it is asserted (low), the character is transmitted. If it is negated (high), the TxD output remains in the marking state and the transmission is delayed

until CTSN goes low. Changes in CTSN, while a character is being transmitted, do not affect the transmission of that character. This feature can be used to prevent overrun of a remote receiver.

MR2[3:2] - RxINT control field

Controls when interrupt arbitration for a receiver begins based on RxFIFO fill level. This field allows interrupt arbitration to begin when the RxFIFO is full, 3/4 full, 1/2 full or when it contains at least 1 character.

Table 6. RxCSR - Receiver Clock Select Register and TxCSR - Transmitter Clock Select Register

Bits 7:5	Bits 4:0
Reserved	Transmitter/Receiver Clock select code, see Clkmux Table below

Both registers consist of single 5 bit field that selects the clock source for the receiver and transmitter respectively. The unused bits in this register read b'111.

Table 7. ClkMux Table

Clock Select Code	Clock selection, CClk = 3.6864 MHz
00000	BRG - 50
00001	BRG - 75
00010	BRG - 150
00011	BRG - 200
00100	BRG - 300
00101	BRG - 450
00110	BRG - 600
00111	BRG - 900
01000	BRG - 1200
01001	BRG - 1800
01010	BRG - 2400
01011	BRG - 3600
01100	BRG - 4800
01101	BRG - 7200
01110	BRG - 9600
01111	BRG - 14.4K
10000	BRG - 19.2K
10001	BRG - 28.2K
10010	BRG - 38.4K
10011	BRG - 57.6K
10100	BRG - 115.2K
10101	BRG - 230.4K
10110	Gin0
10111	Gin1
11000	BRG C/T 0
11001	BRG C/T 1
11010	Reserved
11011	I/O2 rcvr, I/O3 xmit -16x
11100	I/O2 rcvr, I/O3 xmit-1x
11101-11111	Reserved

MR2[1:0] - Stop Bit Length Select

This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16, 1, 1.5 and 2 bits can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1, 1.5 and 2 stop bits can be programmed. In all cases, the receiver only checks for a mark condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit if parity is enabled). If an external 1X clock is used for the transmitter, MR2[1] = 0 selects one stop bit and MR2[1] = 1 selects two stop bits to be transmitted.

CR - Command Register

CR is used to write commands to the Octal UART.

Table 8. CR - Command Register Table

Bits 7:3	Bit 2	Bit 1	Bit 0
Channel Command codes (see Table)	Lock Tx and Rx enables	Enable Tx	Enable Rx

CR[7:3] - Miscellaneous Commands

The encoded value of this field can be used to specify a single command as follows:

00000 No command.

00001 Reserved for channels b-h, for channel a: Change addressing mode to normal.

00010 Reset receiver. Resets the receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO pointer is reset to the first location effectively discarding all unread characters in the FIFO.

00011 Reset transmitter. Resets the transmitter as if a hardware reset had been applied.

00100 Reset error status. Clears the received break, parity error, framing error, and overrun error bits in the status register (SR[7:4]). Used in character mode to clear overrun error status (although RB, PE and FE bits will also be cleared), and in block mode to clear all error status after a block of data has been received.

00101 Reset break change interrupt. Causes the break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.

00110 Start break. Forces the TxD output low (spacing). If the transmitter is empty, the start of the break condition will be delayed up to two bit times. If the transmitter is active, the break begins when transmission of the current character is completed. If there are characters in the TxFIFO, the start of break is delayed until those characters, or any others loaded after it have been transmitted (TxEMT must be true before break begins). The transmitter must be enabled to start a break.

00111 Stop break. The TxD line will go high (marking) within two bit times. TxD will remain high for one bit time before the next character, if any, is transmitted.

01000 Assert RTSN. Causes the RTSN output to be asserted (low).

01001 Negate RTSN. Causes the RTSN output to be negated (high).
Note: The tow commands above actually reset and set , respectively, the I/O2 pin associated the CR register.

01010 Reserved

01011 Reserved for channels b-h, for channel a: Change addressing mode to initialization.

01100 Reserved

01101 Block error status mode. Upon reset of the device or an individual receiver, the block mode of receiver error status accumulates as each character moves to the bottom of the

RxFIFO, the position from which it will be read. In this mode of operation, the RxFIFO may contain a character with non-zero error status for some time. The status will not reflect the error character's presence until it is ready to be popped from the RxFIFO. Command 01101 allows the error status to be updated as each character is **pushed** into the RxFIFO. This allows the earliest detection of a problem character, but complicates the determination of exactly which character is causing the error. This mode of block error accumulation may be exited only by resetting the chip or the individual receiver.

01111 Reserved.

10000 Transmit an Xon Character

10001 Transmit an Xoff Character

10010 Reserved for channels b-h, for channel a: enables a Gang Write of Xon Character Registers. After this command is issued, a write to the channel A Xon Character Register will result in a write to **all** channel's Xon character registers. This command provides a mechanism to initialize all the Xon Character registers with one write. A write to channel A Xon Character Register returns the Octal UART to the individual Xon write mode.

10011 Reserved for channels b-h, for channel a: enables Gang Write of Xoff Character Registers. After this command is issued, a write to the channel A Xoff Character Register will result in a write to **all** channel's Xoff character registers. This command provides a mechanism to initialize all the Xoff Character registers with one write. A write to channel A Xoff Character Register returns the Octal UART to the individual Xoff write mode.

Note: Gang writing of Xon/Xoff Character Commands: Issuing command causes the next write to Xon/Xoff Character Register A to effect a simultaneous write into the other 7 Xon/Xoff character registers. After the Xon/Xoff Character Register A is written, the 26C198 returns to individual write mode for the Xon/Xoff Character Registers. Other intervening reads and writes are ignored. The device resets to individual write mode.

10100 Reserved for channels b-h, for channel a: executes a Gang Load of Xon Character Registers. Executing this command causes a write of the value x'11 to **all** channel's Xon character registers. This command provides a mechanism to initialize all the Xon Character registers to a default value with one write. Execution of this command is immediate and does not effect the timing of subsequent host I/O operations.

10101 Reserved for channels b-h, for channel a: executes a Gang Load of Xoff Character Registers. Executing this command causes a write of the value x'13 to **all** channel's Xoff character registers. This command provides a mechanism to initialize all the Xoff Character registers to a default value with one write. Execution of this command is immediate and does not effect the timing of subsequent host I/O operations.

10110 Xoff resume command (CRXoffre). A command to cancel a previous Host Xoff command. Upon receipt, the channel's transmitter will transfer a character, if any, from the TxFIFO and begin transmission.

10111 Host Xoff command (CRXoff). This command allows tight host CPU control of the flow control of the channel transmitter. When interrupted for receipt of an Xoff character by the receiver, the host may stop transmission of further characters by the channel transmitter by issuing the Host Xoff command. Any character that has been transferred to the Tx shift register will complete its transmission, including the stop bit.

11000 Cancel Host transmit flow control command. Issuing this command will cancel a previous transmit command if the flow control character is not yet loaded into the Tx Shift Register. If there is no character waiting for transmission or if its transmission has already begun, then this command has no effect.

11001 Reserved X

11010 Reserved

11011 Reset Address Recognition Status. This command clears the interrupt status that was set when an address character was recognized by a disabled receiver operating in the special mode.

11100-11101 Reserved

11110 Resets all UART channel registers. This command provides a means to zero all the UART channels that are not reset to x'00 by a reset command or a hardware reset.

11111 Reserved for channels b-h, for channel a: executes a chip wide reset. Executing this command in channel a is equivalent to a hardware reset with the RESETN pin. Executing in channel b-h, has no effect.

Table 9. Command Register Table

Channel Command Code	Channel Command
CR[7:3]	Description
00000	NOP
00001	Reserved
00010	Reset Receiver
00011	Reset Transmitter
00100	Reset Error Status
00101	Reset Break Change Interrupt
00110	Begin Transmit Break
00111	End Transmit Break
01000	Assert RTSN (I/O2
01001	Negate RTSN (I/O2)
01010	Set time-out mode on
01011	Reserved
01100	Set time-out mode off
01101	Block Error Status configure
01110	Reserved
01111	Reserved
10000	Transmit Xon
10001	Transmit Xoff
10010	Gang Write Xon Character Registers *
10011	Gang Write Xoff Character Registers *
10100	Gang Load Xon Character Registers DC1 *
10101	Gang Load Xoff Character Registers DC3 *
10110	Xoff Resume Command
10111	Host Xoff Command
11000	Cancel Transmit X Char command
11001	Reserved
11010	Reserved
11011	Reset Address Recognition Status
11100-11101	Reserved
11110	Reset All UART channel registers
11111	Reset Device *

* CRa only

CR[2] - Lock Tx and Rx enables. If set, the transmitter and receiver enable bits, CR[1:0] are not significant. The enabled/disabled state of a receiver or transmitter can be changed only if this bit is set to zero. The bit provides a mechanism for writing commands to a channel, via CR[7:3], without the necessity of keeping track of or reading the current enable status of the receiver and transmitter.

CR[1] - Enable Transmitter. A one written to this bit enables operation of the transmitter. The TxRDY status bit will be asserted. When disabled by writing a zero to this bit, the command terminates transmitter operation and resets the TxRDY and TxEMT status bits. However, if a character is being transmitted or if characters are loaded in the TxFIFO when the transmitter is disabled, the transmission of the all character(s) is completed before assuming the inactive state.

CR[0] - Enable Receiver. A one written to this bit enables operation of the receiver. If not in the special wake up mode, this also forces the receiver into the search for start bit state. If a zero is written, this command terminates operation of the receiver immediately - a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special wake-up mode is programmed, the receiver operates even if it is disabled (see Wake-up Mode).

Table 10. SR - Channel Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Rcvd Brk	Framing Error	Parity Error	Overrun Error	TxEMT	TxRDY	FFULL	RxRDY
0 - No 1 - Yes	0 - No 1 - Yes	0 - No 1 - Yes	0 - No 1 - Yes	0 - No 1 - Yes	0 - No 1 - Yes	0 - No 1 - Yes	0 - No 1 - Yes

SR[7] - Received Break
This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received; further entries to the FIFO are inhibited until the RxD line returns to the marking state for at least one half bit time (two successive edges of the internal or external 1x clock). When this bit is set, the change in break bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected. The break detect circuitry is capable of detecting breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must last until the end of the next character in order for it to be detected.

SR[6] - Framing Error (FE)
This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SR[5] - Parity Error (PE)
This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity. In the special 'wake up mode', the parity error bit stores the received A/D bit.

SR[4] - Overrun Error (OE)
This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the RxFIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a reset error status command.

SR[3] - Transmitter Empty (TxEMT)
This bit is set when the transmitter underruns, i.e., both the TxFIFO and the transmit shift register are empty.

It is set after transmission of the last stop bit of a character, if no character is in the TxFIFO awaiting transmission. It is reset when the TxFIFO is loaded by the CPU, or when the transmitter is disabled.

SR[2] - Transmitter Ready (TxRDY)
This bit, when set, indicates that the TxFIFO is ready to be loaded with a character. This bit is cleared when the TxFIFO is loaded by the CPU and is set when the last character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, e.g., characters loaded in the TxFIFO while the transmitter is disabled will not be transmitted.

SR[1] - FIFO Full (FFULL)
This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all sixteen RxFIFO positions are occupied. It is reset when the CPU reads the RxFIFO and there is no character in the receive shift register. If a character is waiting in the receive shift register because the RxFIFO is full, FFULL is not reset until the second read of the RxFIFO.

SR[0] - Receiver Ready (RxRDY)
This bit indicates that a character has been received and is waiting in the RxFIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the RxFIFO and reset when the CPU reads the RxFIFO, and no more characters are in the RxFIFO.

Table 11. ISR - Interrupt Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I/O Port	Receiver Watch-dog Timeout	Address recognition event	Xon/off	Always 0	Break	RxRDY	TxRDY

This register provides the status of all potential interrupt sources. When generating an interrupt arbitration value, the contents of this register are masked by the interrupt mask register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', interrupt arbitration for this source will begin. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR can have no affect on the IRQN output. Note that the IMR may or may not mask the **reading** of the ISR as determined by MR1[6]. If MR1[6] is cleared, the reset and power on default, the ISR is read without modification. If MR1[6] is set, the ISR reads a value

ISR[n] AND IMR[n].

ISR[7] - Input Change of State. This bit is set when a change of state occurs at the I/O1 or I/O0 input pins. It is reset when the CPU reads the Input Port Register, IPR.

ISR[6] Watch-dog Timeout. This bit is set when the receiver's watch-dog timer has counted more than 64 bit times since the last RxFIFO event. RxFIFO events are a read of the RxFIFO or GRxFIFO, or the push of a received character into the FIFO. The interrupt will be cleared automatically upon the push of the next character received or when the RxFIFO or GRxFIFO is read. The receiver watch-dog timer is included to allow detection of the very last characters of a received message that may be waiting in the RxFIFO, but are too few in number to successfully initiate an interrupt. Refer to the watch-dog timer description for details of how the interrupt system works after a watch-dog timeout.

ISR[5] - Address Recognition Status Change. This bit is set when a change in receiver state has occurred due to an Address character being received from an external source and comparing to the reference address in ARCR. The bit and interrupt is negated by a write to the CR with command x11011, Reset Address Recognition Status.

ISR[4] - Xon/Xoff Status Change. This bit is set when an Xon/Xoff character being received from an external source. The bit is negated by a read of the channel Xon Interrupt Status Register, XISR.

ISR[3] - Reserved Always reads a 0

ISR[2] - Change in Channel Break Status. This bit, when set, indicates that the receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a reset break change interrupt command via the CR.

ISR[1] - Receiver Ready . The general function of this bit is to indicate that the RxFIFO has data available. The particular meaning of this bit is programmed by MR2[3:2]. If programmed as receiver ready(MR2[3:2] = 00), it indicates that at one character has been received and is waiting in the RxFIFO to be read by the host CPU. It is set when the character is transferred from the receive shift register to the RxFIFO and reset when the CPU reads the last character from the RxFIFO.

If MR2[3:2] is programmed as FIFO full, ISR[1] is set when a character is transferred from the receive holding register to the RxFIFO and the transfer causes the RxFIFO to become full, i.e. all sixteen FIFO positions are occupied. It is reset when ever RxFIFO is not full. If there is a character waiting in the receive shift register because the FIFO is full, the bit is set again when the waiting character is transferred into the FIFO.

The other two conditions of these bits, 3/4 and half full operate in a similar manner. The ISR[1] bit is set when the RxFIFO fill level meets or exceeds the value; it is reset when the fill level is less. See the description of the MR2 register.

Note: This bit must be at a one (1) for the receiver to enter the arbitration process. It is the fact that this bit is zero (0) when the RxFIFO is empty that stops an empty FIFO from entering the interrupt arbitration. Also note that the meaning if this bit is not quite the same as the similar bit in the status register (SR).

ISR[0] - Transmitter Ready . The general function of this bit is to indicate that the TxFIFO has an at least one empty space for data. The particular meaning of the bit is controlled by MR0[5:4] indicates the TxFIFO may be loaded with one or more characters. If MR0[5:4] = 00 (the default condition) this bit will not set until the TxFIFO is empty - sixteen bytes available. If the fill level of the TxFIFO is below the trigger level programmed by the TxINT field of the Mode Register 0, this bit will be set. A one in this position indicates that at least one character can be sent to the TxFIFO. It is turned off as the TxFIFO is filled above the level programmed by MR0[5:4. This bit turns on as the FIFO empties; the RxFIFO bit turns on as the FIFO fills. This often a point of confusion in programming interrupt functions for the receiver and transmitter FIFOs.

Note: This bit must be at a one (1) for the transmitter to enter the arbitration process. It is the fact that this bit is zero (0) when the RxFIFO is full that stops a full FIFO from entering the interrupt arbitration. Also note that the meaning if this bit is not quite the same as the similar bit in the status register (SR).

Table 12. IMR - Interrupt Mask Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I/O Port	Receiver Watch-dog Timeout	Address recognition event	Xon/off	Set to 0	Break	RxRDY	TxRDY

The programming of this register selects which bits in the ISR cause an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is a '1', the interrupt source is presented to the internal interrupt arbitration circuits, eventually resulting in the IRQN output being asserted (low). If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no affect on the IRQN output.

IMR[7] Controls if a change of state in the inputs equipped with input change detectors will cause an interrupt.

IMR[6] Controls the generation of an interrupt by the watch-dog timer event. If set, a count of 64 idle bit times in the receiver will begin interrupt arbitration.

IMR[5] Enables the generation of an interrupt in response to changes in the Address Recognition circuitry of the Special Mode (multi-drop or wake-up mode).

IMR[4] Enables the generation of an interrupt in response to recognition of an in-band flow control character.

IMR[3] Reserved

IMR[2] Enables the generation of an interrupt when a Break condition has been detected by the channel receiver.

IMR[1] Enables the generation of an interrupt when servicing for the RxFIFO is desired.

IMR[0] Enables the generation of an interrupt when servicing for the TxFIFO is desired.

Table 13. RxFIFO Receiver FIFO

Bit[9]	Bit[9]	Bit[8]	Bits [7:0]
Break Received Status	Framing Error Status	Parity Error Status	8 data bits MSBs =0 for 7,6,5 bit data

The FIFO for the receiver is 11 bits wide and 16 "words" deep. The status of each byte received is stored with that byte and is moved along with the byte as the characters are read from the FIFO. The upper three bits are presented in the STATUS register and they change in the status register each time a data byte is read from the FIFO. Therefor the status register should be read BEFORE the byte is read from the RxFIFO if one wishes to ascertain the quality of the byte

The forgoing applies to the "character error" mode of status reporting. See MR1[5] and "RxFIFO Status" descriptions for "block

error" status reporting. Briefly "Block Error" gives the accumulated error of all bytes in the RxFIFO

Table 14. TxFIFO – Transmitter FIFO

Bits 7:0
8 data bits. MSBs set to 0 for 7, 6, 5 bit data

The FIFO for the transmitter is 8 bits wide by 16 bytes deep. For character lengths less than 8 bits the upper bits will be ignored by the transmitter state machine and thus are effectively discarded.

Table 15. IVR - Interrupt Vector Register

Bits 7:6	Bits 5:3	Bits 2:0
Always included in interrupt vector	Will be replaced with current interrupt type if IVC field of GCCR > 1	Will be replaced with interrupting channel number if IVC field of GCCR > 0

This register provides the fixed field(s) used to assemble an interrupt acknowledge vector for output during an interrupt acknowledge cycle. The IVC field of the GCCR, Global Chip Configuration Register, controls the build up of the Interrupt Vector, if supplied.

Table 16. BCRBRK - Bidding Control Register - Break Change

Bits 7:3	Bits 2:0
Reserved	MSB of break change interrupt bid

This register provides the 3 MSBs of the Interrupt Arbitration number for a break change interrupt.

Table 17. BCRCOS - Bidding Control Register - Change of State

Bits 7:3	Bits 2:0
Reserved	MSB of a COS interrupt bid
Read as x'0	

This register provides the 3 MSBs of the Interrupt Arbitration number for a Change of State, COS, interrupt.

Table 18. BCRx - Bidding Control Register - Xon

Bits 7:3	Bits 2:0
Reserved	MSB of an Xon/Xoff interrupt bid

This register provides the 3 MSBs of the Interrupt Arbitration number for an Xon/Xoff interrupt.

Table 19. BCRA - Bidding Control Register - Address

Bits 7:3	Bits 2:0
Reserved	MSB of an address recognition event interrupt bid

This register provides the 3 MSBs of the Interrupt Arbitration number for an address recognition event interrupt.

Table 20. XONCR - Xon Character Register

Bits 7:0
8 Bits of the Xon Character Recognition

An 8 bit character register that contains the compare value for an Xon character.

Table 21. XOFCR - Xoff Character Register

Bits 7:0
8 Bits of the Xoff Character Recognition

An 8 bit character register that contains the compare value for an Xoff character.

Table 22. ARCR - Address Recognition Character Register

Bits 7:0
8 Bits of the Multi-Drop Address Character Recognition

An 8 bit character register that contains the compare value for the wake-up address character

Table 23. WDTRCR - Watch-dog Timer Enable Register

WDT							
h	g	f	e	d	c	b	a
1 on 0 off	1 on 0 off	1 on 0 off	1 on 0 off	1 on 0 off	1 on 0 off	1 on 0 off	1 on 0 off

This register enables the watch-dog Timer for each of the 8 receivers on the Octal UART

Table 24. BRGTRU - BRG Timer Reload Registers, Upper

Bits 7:0
8 MSB of the BRG Timer divisor.

This is the upper byte of the 16 bit value used by the BRG timer in generating a baud rate clock

Table 25. BRGTRL - BRG Timer Reload Registers, Lower

Bits 7:0
8 LSB of the BRG Timer divisor

This is the lower byte of the 16 bit value used by the BRG timer in generating a baud rate clock.

Table 26. BRGTCR - BRG Timer Control Register

Bit 7	Bit 6:4	Bit 3	Bit 2:0
BRGT 1, Register control	BRGT 1, Clock selection	BRGT 0, Register control	BRGT 0, Clock selection
0 - Resets the timer register and holds it stopped 1 - Allows the timer register to run.	000 - Sclk / 16 001 - Sclk / 32 010 - Sclk/ 64 011 - Sclk / 128 100 - X1 101 - X1 / 2 110 - I/O1b 111 - Gln(1)	0 - Resets the timer register and holds it stopped. 1 - Allows the timer register to run.	000 - Sclk / 16 001 - Sclk / 32 010 - Sclk / 64 011 - Sclk / 128 100 - X1 101 - X1 / 2 110 - I/O1a 111 - Gln(0)

Table 27. XISR - Xon-off Interrupt Status Register

Bits 7:6	Bits 5:4	Bits 3:2	Bits 1:0
Received X Character Status	Automatic X Character transmission status	Tx flow status	Tx char status
00 - none 01 - Xoff received 10 - Xon received 11 - both received	00 - none 01 - Xon transmitted 10 - Xoff transmitted 11 - Illegal, does not occur	00 - normal 01 - Tx halt pending 10 - re-enabled 11 - flow disabled	00 - normal Tx data 01 - wait on normal data 10 - Xoff in pending 11 - Xon in pending

XISR[7:6] Received X Character Status. This field can be read to determine if the receiver has encountered an Xon or Xoff character in the incoming data stream. These bits are maintained until a read of the XISR. The field is updated by X character reception regardless of the state of MR0(7, 3:2) or IMR(4). The field can therefore be used as a character detector for the bit patterns stored in the Xon and Xoff Character Registers.

XISR[5:4] Automatic transmission Status. This field indicates the last flow control character sent in the Auto Receiver flow control mode. If Auto Receiver mode has not been enabled, this field will always read b'00. It will likewise reset to b'00 if MR0(3) is reset. If the Auto Receiver mode is exited while this field reads b'10, it is the user's responsibility to transmit an Xon, when appropriate.

XISR[3:2] Tx flow Status. This field tracks the transmitter's flow status as follows:

00 normal. The flow control is under host control.
01 Tx halt pending. After the current character finishes the transmitter will stop. The status will then change to b'00.
10 re-enabled. The transmitter had been halted and restarted. It is sending data characters. After a read of the XISR, it will return to "normal" status.
11 disabled. The transmitter is flow controlled.

XISR[1:0] Tx character Status. This field allows determination of the type of character being transmitted. If XISR(1:0) is b'01, the channel is waiting for a data character to transfer from the TxFIFO. This condition will only occur for a bit time after an Xon or Xoff character transmission unless the TxFIFO is empty.

UCIR - Update CIR

A command based upon an address decode. A write to this 'register' causes the Current Interrupt Register to be updated with the value that is winning interrupt arbitration. The register would be used in systems that poll the interrupt status registers rather than wait for interrupts. Alternatively, the CIR could be updated during an Interrupt Acknowledge Bus cycle in interrupt driven systems.

Table 28. CIR - Current Interrupt Register

Bits 7:6	Bits 5:3	Bits 2:0
Type	Current byte count/type	Channel number
00 - other	000 - no interrupt 001 - Change of State 010 - Address Recognition 011 - Xon/Xoff status 100 - Not used 101 - Break change 110, 111 do not occur	000 - a 001 - b 010 - c . . 111 - h
01 - Transmit 11- Receive w errors 10 - Receive w/o errors	Current count code 0 => 9 or less characters 1 => 10 characters . . 5 => 14 characters 6 => 15 characters 7 => 16	000 - a 001 - b 010 - c . . 111 - h

Note: The GIBCR, Global Interrupting Byte Count Register, may be read to determine an exact character count if 9 or less characters are indicated in the count field of the CIR.

The Current Interrupt Register is provided to speed up the specification of the interrupting condition in the Octal UART. The CIR is updated at the beginning of an interrupt acknowledge bus cycle or in response to an Update CIR command. (see immediately above) Although interrupt arbitration continues in the background, the current interrupt information remains frozen in the CIR until another IACK cycle or Update CIR command occurs. The LSBs of the CIR provide part of the addressing for various Global Interrupt registers including the GIBCR, GICR, GITR and the Global Rx and Tx FIFO. The host CPU need not generate individual addresses for this information since the interrupt context will remain stable at the fixed addresses of the Global Interrupt registers until the CIR is updated. For most interrupting sources, the data available in the CIR alone will be sufficient to set up a service routine.

The CIR may be processed as follows:

If CIR[7] = 1, then a receiver interrupt is pending and the count is CIR[5:3], channel is CIR[2:0]

Else If CIR[6] = 1 then a transmitter interrupt is pending and the count is CIR[5:3], channel is

CIR[2:0]

Else the interrupt is another type, specified in CIR[5:3]

Table 29. GICR - Global Interrupting Channel Register

Bits 7:3	Bits 2:0
Reserved	Channel code
	000 - a 001 - b 010 - c . . 111 - h

A register associated with the interrupting channel as defined in the CIR. It contains the interrupting channel code for all interrupts.

Table 30. GIBCR - Global Interrupting Byte Count Register

Bits 7:4	Bits 3:0
Reserved	Channel byte count code
	0000 - 1 0001 - 2 0010 - 3 . . 1111 - 16

A register associated with the interrupting channel as defined in the CIR. It contains the byte count - 1 for transfer in Transmit and Receiver interrupts. It is undefined for other types of interrupts

Table 31. GITR - Global Interrupting Type Register

Bit 7:6	Bit 5	Bit 4:3	Bit 2:0
Receiver Interrupt	Transmitter Interrupt	Reserved	Other types
0x - not receiver 10 - with receive errors 11 - w/o receive errors	0 - not transmitter 1 - transmitter interrupt	read b'00	000 - not "other" type 001 - Change of State 010 - Address Recognition Event 011 - Xon/Xoff status 100 - Not used 101 - Break Change 11x - do not occur

A register associated with the interrupting channel as defined in the CIR. It contains the type of interrupt code for all interrupts.

Table 32. GRxFIFO - Global RxFIFO Register

Bits 7:0
8 data bits of RxFIFO. MSBs set to 0 for 7, 6, 5 bit data

The RxFIFO of the channel indicated in the CIR channel field. Undefined when the CIR interrupt context is not a receiver interrupt. Global TxFIFO Register

Table 33. GTxFIFO - Global TxFIFO Register

Bits 7:0
8 data bits of TxFIFO. MSBs not used for 7, 6, 5 bit data

The TxFIFO of the channel indicated in the CIR channel field. Undefined when the CIR interrupt context is not a transmitter interrupt. Writing to the GTxFIFO when the current interrupt is not a transmitter event may result in the characters being transmitted on a different channel than intended.

Table 34. IPR - Input Port Register

Bit 7	Bit 6	Bit 7	Bit 6	Bit 3	Bit 2	Bit 1	Bit 0
I/O3	I/O2	I/O1	I/O0	I/O3 state	I/O2 state	I/O1 state	I/O0 state
0 - no change 1 - change	0 - no change 1 - change	0 - no change 1 - change	0 - no change 1 - change				

This register may be read to determine the current level of the I/O pins and examine the output of the change detectors assigned to each pin. If the change detection is not enabled or if the pin is configured as an output, the associated change field will read b'0.

Table 35. I/OPCR - I/O Port Configuration Register

Bits 7:6	Bits 5:4	Bits 3:2	Bits 1:0
I/O3 control	I/O2 control	I/O1 control	I/O0 control
00 - GPI/TxC input 01 - OPR3 output 10 - TxC16x output 11 - TxC1x output	00 - GPI/RxC input 01 - OPR2/RTSN* 10 - RxC1x output 11 - RxC16x output	00 - GPI input 01 - OPR1/RTSN* 10 - Reserved 11 - RxC1x output	00 - GPI/CTS input 01 - OPR0 output 10 - TxC1x output 11 - TxC16x output

* If I/OPCR(5:4) is programmed as '01' then the RTS functionality is assigned to I/O2, otherwise, this function can be implemented on I/O1

This register contains 4, 2 bit fields that set the direction and source for each of the I/O pins associated with the channel. The I/O2 output may be RTSN if MR1[7] is set. or may signal "end of transmission if MR[2[5] is set.(Please see the descriptions of these functions under the MR1 and MR2 register descriptions) If this control bit is cleared, the pin will use the OPR[2] as a source if I/OPCR[5:4] is b'01. The b'00 combinations are always inputs. This register resets to x'0, effectively rendering all I/Os to input pin status on power up or reset. Inputs may be used as Rx, Tx inputs or CTS and General Purpose Inputs simultaneously. All inputs are equipped with change detectors that may be used to generate interrupts or can be polled, as required.

NOTE: To ensure that CTS, RTS and an external RxC are always available, if I/O2 is not selected as the RTSN output, the RTS function is automatically provided on I/O1,

Table 36. I/OPIOR - I/O Port Interrupt and Output Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I/O3 enable	I/O2 enable	I/O1 enable	I/O0 enable	I/O3 output	I/O2 output	I/O1 output	I/O0 output
0 - disable 1 - enable	0 - disable 1 - enable	0 - disable 1 - enable	0 - disable 1 - enable	OPR[3]	OPR[2]	OPR[1]	OPR[0]

The I/OPIOR controls the input change detectors and is the means for writing to the OPR, output port register. The values written into the OPR bits may be selected as the outputs of the I/O pins.

If a pin is configured as an output, a b'1 value written to a ΔI/O field has no effect.

Table 37. GPOSR - General Purpose Output Select Register

Bits 7:4	Bits 3:0
Reserved	General Purpose Output 0 Selection
RESERVED	0000 = Reserved a 0001 = Reserved b 0010 = Reserved c 0011 = Reserved d 0100 = Reserved e 0101 = Reserved f 0110 = Reserved g 0111 = Reserved h 1000 = TxC1x a 1001 = TxC16x a 1010 = RxC16x a 1011 = TxC16x b 1100 = GPOR(3) 1101 = GPOR(2) 1110 = GPOR(1) 1111 = GPOR(0)

Table 38. GPOR - General Purpose Output Register

Bits 7:4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	GPOR(3)	GPOR(2)	GPOR(1)	GPOR(0)

Table 39. GPOC - General Purpose Output Clk Register

Bits 7:6	Bits 5:4	Bits 3:2	Bits 1:0
Clk Sel GPOR(3)	Clk Sel GPOR(2)	Clk Sel GPOR(1)	Clk Sel GPOR(0)
00 = none 01 = GIN0 10 = GIN1 11 = I/O3g	00 = none 01 = GIN0 10 = GIN1 11 = I/O3e	00 = none 01 = GIN0 10 = GIN1 11 = I/O3c	00 = none 01 = GIN0 10 = GIN1 11 = I/O3a

Table 40. GPOD - General Purpose Output Data Register

Bits 7:6	Bits 5:4	Bits 3:2	Bits 1:0
Data Sel GPOR(3)	Data Sel GPOR(2)	Data Sel GPOR(1)	Data Sel GPOR(0)
00 = '1' 01 = '0' 10 = GPOR(3)' 11 = I/O3h	00 = '1' 01 = '0' 10 = GPOR(2)' 11 = I/O3f	00 = '1' 01 = '0' 10 = GPOR(1)' 11 = I/O3d	00 = '1' 01 = '0' 10 = GPOR(0)' 11 = I/O3b

Table 41. ICR - Interrupt Control Register

Bit 7	Bits 6:0
Reserved. Set to 0	Upper seven bits of the Arbitration Threshold

This register provides a single 7 bit field called the interrupt threshold for use by the interrupt arbiter. The field is interpreted as a single unsigned integer. The interrupt arbiter will not generate an external interrupt request, by asserting IRQN, unless the value of the highest priority interrupt exceeds the value of the interrupt threshold. If the highest bidder in the interrupt arbitration is lower than the threshold level set by the ICR, the Current Interrupt Register, CIR, will contain x'00. Refer to the functional description of interrupt generation for details on how the various interrupt source bid values are calculated.

Note: While a watch-dog Timer interrupt is pending, the ICR is not used and only receiver codes are presented for interrupt arbitration. This allows receivers with very low count values (perhaps below the threshold value) to win interrupt arbitration without requiring the user to explicitly lower the threshold level in the ICR. These bits are the upper seven (7) bits of the interrupt arbitration system. The lower three (3) bits represent the channel number.

Register Maps

The registers of the SC26C198 are partitioned into two groups: those used in configuring data channels and those used in handling the actual flow of data and status. Below is shown the general configuration of all the registers addressed. The "Register Map Summary" shows the configuration of the lower four bits of the address that are the same for the individual UARTs. It also shows the several addresses in the address space of UART A and UART B that apply to the total chip configuration. The "Register Map Detail" shows the use of every address in the 8-bit address space.

NOTE: The register maps for channels A and B (UARTs A and B) contain some control registers that configure the entire chip. These are denoted by a (•) symbol.

Table 42. Summary Register Map, Data

Address (hex) ccc = Channel	Register Name	Acronym	Read/Write	Page
	UART A			
1ccc 0000 (x80)	Mode Register 2	MR2	R/W	384
1ccc 0001 (x81)	Status Register	SR	R	387
1ccc 0001 (81)	Command Register	CR	W	385
1ccc 0010 (x82)	Interrupt Status Register	ISR	R	387
1ccc 0010 (82)	Interrupt Mask Register	IMR	W	388
1ccc 0011 (83)	Transmitter FIFO Register	TxFIFO	W	389
1ccc 0011 (x83)	Receiver FIFO Reg	RxFIFO	R	388
1ccc 0100 (x84)	Input Port Reg	IPR	R	391
1ccc 0101 (x85)	I/O Port Interrupt and Output	I/OPIOR	R/W	392
1ccc 0110 (x86)	Xon/Xoff Interrupt Status Reg	XISR	R	390
1000 0111 (x87)	• GP Out Select Reg	GPOSR	R/W	392
1000 1000 (x88)	•BRG Timer Reg Upper a	BRGTRUa	R/W	389
1000 1001 (x89)	•BRG Timer Reg Lower a	BRGTRLa	R/W	389
1000 1010 (x8A)	•BRG Timer Control Reg a	BRGTCRa	R/W	390
1000 1011 (x8B)	• GP Out Clk Reg	GPOC	R/W	393
1000 1100 (x8C)	•Update Current Interrupt Reg	UCIR	W	390
1000 1100 (x8C)	•Current Interrupt Reg	CIR	R	390
1000 1110 (x8E)	•Global Receive Hold Reg	GRxFIFO	R	391
1000 1110 (x8E)	•Global Transmit Hold Reg	GTxFIFO	W	391
1000 1111 (x8F)	•Global Chip Configuration Reg	GCCR	R/W	383
1001 0111 (x97)	•GP Output Reg	GPOR	R/W	392
1001 1000 (x98)	•BRG Timer Reg Upper b	BRGTRUb	R/W	389
1001 1001 (x99)	•BRG Timer Reg Lower b	BRGTRLb	R/W	389
1001 1011 (x9B)	• GP Out Data Reg	GPOD	R/W	393
1001 1100 (x9C)	•Global Interrupt Channel Reg	GICR	R	391
1001 1101 (x9D)	•Global Interrupt Byte Count	GIBCR	R	391
1001 1111 (x9F)	•Global Interrupt Type Register	GITR	R	391

Table 43. Summary Register Map, Control

Address (hex) ccc = channel	Register Name	Acronym	Read / Write	Page
0ccc 0000 (x00)	Mode Register 0 MR0a	MR0	R/W	383
0ccc 0001 (x01)	Mode Register 1 MR1a	MR1	R/W	383
0ccc 0010 (x02)	I/OPort Configuration Reg a I/OPCRa	IOPCR	R/W	392
0ccc 0011 (x03)	Bid Control, Break Change	BCRBRK	R/W	389
0ccc 0100 (x04)	Bid Control, Change of State	BCRCOS	R/W	389
0ccc 0110 (x06)	Bid Control, Xon/Xoff	BCRX	R/W	389
0ccc 0111 (x07)	Bid Control, Address recognition	BCRA	R/W	389
0ccc 1000 (x08)	Xon Character Register	XonCR	R/W	389
0ccc 1001 (x09)	Xoff Character Register	XoffCR	R/W	389
0ccc 1010 (x0A)	Address Recognition Character	ARCR	R/W	389
0ccc 1100 (x0C)	Receiver Clock Select Register	RxCSR	R/W	385
0ccc 1110 (x0E)	Transmitter Clock Select Register	TxCSR	R/W	385
0000 1101 (0D)	•Test Register	Reserved, set to 0		
0000 1111 (x0F)	•Global Chip Configuration Register	GCCR	R/W	383
00011011 (x1B)	•Interrupt Control Register	ICR	R/W	393
0001 1101 (x1D)	•Watch–dog Timer Run Control	WDTRCR	R/W	389
0001 1111(x1F)	•Interrupt Vector Register	IVR	R/W	389

NOTE: The register maps for channels A and B (UARTs A and B) contain some control registers that configure the entire chip. These are denoted by a (•) symbol.

REGISTER MAP DETAIL

Table 44. Register Map, Control

A(7:0)	Read	Write
	UART A	
00000000 (x00)	Mode Register 0 MR0a	Mode Register 0 MR0a
00000001 (x01)	Mode Register 1 MR1a	Mode Register 1 MR1a
00000010 (x02)	I/OPort Configuration Reg a I/OPCRa	I/OPort Configuration Reg a I/OPCRa
00000011 (x03)	BCRBRKa	BCRBRKa
00000100 (x04)	BCRCOSa	BCRCOSa
00000101 (x05)	Reserved	Reserved
00000110 (x06)	BCRXa	BCRXa
00000111 (x07)	BCRAa	BCRAa
00001000 (x08)	Xon Character Reg a (XonCRa)	Xon Character Reg a (XonCRa)
00001001 (x09)	Xoff Character Reg a (XoffCRa)	Xoff Character Reg a (XoffCRa)
00001010 (x0A)	Address Recognition Char a (ARCRa)	Address Recognition Char a (ARCRa)
00001011 (x0B)	Reserved	Reserved
00001100 (x0C)	Receiver Clock Select Register a (RxCSRa)	Receiver Clock Select Register a (RxCSRa)
00001101 (x0D)	•Test Register	•Test Register
00001110 (x0E)	Xmit Clock Select Register a (TxCSRa)	Xmit Clock Select Register a (TxCSRa)
00001111 (x0F)	•Global Chip Configuration Reg (GCCR)	•Global Chip Configuration Reg (GCCR)
	UART B	
00010000 (x10)	Mode Register 0 MR0b	Mode Register 0 MR0b
00010001 (x11)	Mode Register 1 MR1b	Mode Register 1 MR1b
00010010 (x12)	I/OPort Configuration Reg b I/OPCRb	I/OPort Configuration Reg b I/OPCRb
00010011 (x13)	BCRBRKb	BCRBRKb
00010100 (x14)	BCRCOSb	BCRCOSb
00010101 (x15)	Reserved	Reserved
00010110 (x16)	BCRXb	BCRXb
00010111 (x17)	BCRAb	BCRAb
00011000 (x18)	Xon Character Reg b (XonCRb)	Xon Character Reg b (XonCRb)
00011001 (x19)	Xoff Character Reg b (XoffCRb)	Xoff Character Reg b (XoffCRb)
00011010 (x1A)	Address Recognition Char b (ARCRb)	Address Recognition Char b (ARCRb)
00011011 (x1B)	•Interrupt Control Register (ICR)	•Interrupt Control Register (ICR)
00011100 (x1C)	Receiver Clock Select Register b (RxCSRb)	Receiver Clock Select Register b (RxCSRb)
00011101 (x1D)	•Watch–dog Timer Run Ctrl (WDTRCR)	•Watch–dog Timer Run Ctrl (WDTRCR)
00011110 (x1E)	Xmit Clock Select Register b (TxCSRb)	Xmit Clock Select Register b (TxCSRb)
00011111 (x1F)	•Interrupt Vector Register (IVR)	•Interrupt Vector Register (IVR)

NOTE: The register maps for channels A and B (UARTS A and B) contain some control registers that configure the entire chip. **These are denoted by a "•" symbol**

A(7:0)	Read	Write
	UART C	
00100000 (x20)	Mode Register 0 MR0c	Mode Register 0 MR0c
00100001 (x21)	Mode Register 1 MR1c	Mode Register 1 MR1c
00100010 (x22)	I/OPort Configuration Reg c I/OPCRc	I/OPort Configuration Reg c I/OPCRc
00100011 (x23)	BCRBRKc	BCRBRKc
00100100 (x24)	BCRCOSc	BCRCOSc
00100101 (x25)	Reserved	Reserved
00100110 (x26)	BCRXc	BCRXc
00100111 (x27)	BCRAc	BCRAc
00101000 (x28)	Xon Character Reg c (XonCRc)	Xon Character Reg c (XonCRc)
00101001 (x29)	Xoff Character Reg c (XoffCRc)	Xoff Character Reg c (XoffCRc)
00101010 (x2A)	Address Recognition Char c (ARCRc)	Address Recognition Char c (ARCRc)
00101011 (x2B)	Reserved	Reserved
00101100 (x2C)	Receiver Clock Select Register c (RxCSRc)	Receiver Clock Select Register c (RxCSRc)
00101101 (x2D)	Reserved	Reserved
00101110 (x2E)	Xmit Clock Select Register c (TxCSRc)	Xmit Clock Select Register c (TxCSRc)
00101111 (x2F)	Reserved	Reserved
	UART D	
00110000 (x30)	Mode Register 0 MR0d	Mode Register 0 MR0d
00110001 (x31)	Mode Register 1 MR1d	Mode Register 1 MR1d
00110010 (x32)	I/OPort Configuration Reg d I/OPCRd	I/OPort Configuration Reg d I/OPCRd
00110011 (x33)	BCRBRKd	BCRBRKd
00110100 (x34)	BCRCOSd	BCRCOSd
00110101 (x35)	Reserved	Reserved
00110110 (x36)	BCRXd	BCRXd
00110111 (x37)	BCRAd	BCRAd
00111000 (x38)	Xon Character Reg d (XonCRd)	Xon Character Reg d (XonCRd)
00111001 (x39)	Xoff Character Reg d (XoffCRd)	Xoff Character Reg d (XoffCRd)
00111010 (x3A)	Address Recognition Char d (ARCRd)	Address Recognition Char d (ARCRd)
00111011 (x3B)	Reserved	Reserved
00111100 (x3C)	Receiver Clock Select Register d (RxCSRd)	Receiver Clock Select Register d (RxCSRd)
00111101 (x3D)	Reserved	Reserved
00111110 (x3E)	Xmit Clock Select Register d (TxCSRd)	Xmit Clock Select Register d (TxCSRd)
00111111 (x3F)	Reserved	Reserved

A(7:0)	Read	Write
	UART E	
01000000 (x40)	Mode Register 0 MR0e	Mode Register 0 MR0e
01000001 (x41)	Mode Register 1 MR1e	Mode Register 1 MR1e
01000010 (x42)	I/OPort Configuration Reg e I/OPCRe	I/OPort Configuration Reg e I/OPCRe
01000011 (x43)	BCRBRKe	BCRBRKe
01000100 (x44)	BCRCOSe	BCRCOSe
01000101 (x45)	Reserved	Reserved
01000110 (x46)	BCRXe	BCRXe
01000111 (x47)	BCRAe	BCRAe
01001000 (x48)	Xon Character Reg e (XonCRe)	Xon Character Reg e (XonCRe)
01001001 (x49)	Xoff Character Reg e (XoffCRe)	Xoff Character Reg e (XoffCRe)
01001010 (x4A)	Address Recognition Char e (ARCRe)	Address Recognition Char e (ARCRe)
01001011 (x4B)	Reserved	Reserved
01001100 (x4C)	Receiver Clock Select Register e (RxCSRe)	Receiver Clock Select Register e (RxCSRe)
01001101 (x4D)	Reserved	Reserved
01001110 (x4E)	Xmit Clock Select Register e (TxCSRe)	Xmit Clock Select Register e (TxCSRe)
01001111 (x4F)	Reserved	Reserved
	UART F	
01010000 (x50)	Mode Register 0 MR0f	Mode Register 0 MR0f
01010001 (x51)	Mode Register 1 MR1f	Mode Register 1 MR1f
01010010 (x52)	I/OPort Configuration Reg f I/OPCRf	I/OPort Configuration Reg f I/OPCRf
01010011 (x53)	BCRBRKf	BCRBRKf
01010100 (x54)	BCRCOSf	BCRCOSf
01010101 (x55)	Reserved	Reserved
01010110 (x56)	BCRXf	BCRXf
01010111 (x57)	BCRAf	BCRAf
01011000 (x58)	Xon Character Reg f (XonCRf)	Xon Character Reg f (XonCRf)
01011001 (x59)	Xoff Character Reg f (XoffCRf)	Xoff Character Reg f (XoffCRf)
01011010 (x5A)	Address Recognition Char f (ARCRf)	Address Recognition Char f (ARCRf)
01011011 (x5B)	Reserved	Reserved
01011100 (x5C)	Receiver Clock Select Register f (RxCSRf)	Receiver Clock Select Register f (RxCSRf)
01011101 (x5D)	Reserved	Reserved
01011110 (x5E)	Xmit Clock Select Register f (TxCSRf)	Xmit Clock Select Register f (TxCSRf)
01011111 (x5F)	Reserved	Reserved

A(7:0)	Read	Write
	UART G	
01100000 (x60)	Mode Register 0 MR0g	Mode Register 0 MR0g
01100001 (x61)	Mode Register 1 MR1g	Mode Register 1 MR1g
01100010 (x62)	I/OPort Configuration Reg g I/OPCRg	I/OPort Configuration Reg g I/OPCRg
01100011 (x63)	BCRBRKg	BCRBRKg
01100100 (x64)	BCRCOSg	BCRCOSg
01100101 (x65)	Reserved	Reserved
01100110 (x66)	BCRXg	BCRXg
01100111 (x67)	BCRAg	BCRAg
01101000 (x68)	Xon Character Reg g (XonCRg)	Xon Character Reg g (XonCRg)
01101001 (x69)	Xoff Character Reg g (XoffCRg)	Xoff Character Reg g (XoffCRg)
01101010 (x6A)	Address Recognition Char g (ARCRg)	Address Recognition Char g (ARCRg)
01101011 (x6B)	Reserved	Reserved
01101100 (x6C)	Receiver Clock Select Register g (RxCSRg)	Receiver Clock Select Register g (RxCSRg)
01101101 (x6D)	Reserved	Reserved
01101110 (x6E)	Xmit Clock Select Register g (TxCSRg)	Xmit Clock Select Register g (TxCSRg)
01101111 (x6F)	Reserved	Reserved
	UART H	
01110000 (x70)	Mode Register 0 MR0h	Mode Register 0 MR0h
01110001 (x71)	Mode Register 1 MR1h	Mode Register 1 MR1h
01110010 (x72)	I/OPort Configuration Reg h I/OPCRh	I/OPort Configuration Reg h I/OPCRh
01110011 (x73)	BCRBRKh	BCRBRKh
01110100 (x74)	BCRCOSh	BCRCOSh
01110101 (x75)	Reserved	Reserved
01110110 (x76)	BCRXh	BCRXh
01110111 (x77)	BCRAh	BCRAh
01111000 (x78)	Xon Character Reg h (XonCRh)	Xon Character Reg h (XonCRh)
01111001 (x79)	Xoff Character Reg h (XoffCRh)	Xoff Character Reg h (XoffCRh)
01111010 (x7A)	Address Recognition Char h (ARCRh)	Address Recognition Char h (ARCRh)
01111011 (x7B)	Reserved	Reserved
01111100 (x7C)	Receiver Clock Select Register h (RxCSRh)	Receiver Clock Select Register h (RxCSRh)
01111101 (x7D)	Reserved	Reserved
01111110 (x7E)	Xmit Clock Select Register h (TxCSRh)	Xmit Clock Select Register h (TxCSRh)
01111111 (x7F)	Reserved	Reserved

Table 45. Register Map, Data

A(7:0)	Read	Write
	UART A	
10000000 (x80)	Mode Register a (MR2a)	Mode Register a (MR2a)
10000001 (x81)	Status Register a (SRa)	Command Register a (CRa)
10000010 (x82)	Interrupt Status Register a (ISRa)	Interrupt Mask Register a (IMRa)
10000011 (x83)	Receiver FIFO Reg a (RxFIFOa)	Transmitter FIFO Reg a (TxFIFOa)
10000100 (x84)	Input Port Reg a (IPRa)	Reserved
10000101 (x85)	I/O Port Interrupt and Output a (I/OPIORa)	I/O Port Interrupt and Output a (I/OPIORa)
10000110 (x86)	Xon/Xoffnterrupt Status Reg a (XISRa)	Reserved
10000111 (x87)	• GP Out Select Reg (GPOSR)	• GP Out Select Reg (GPOSR)
10001000 (x88)	•BRG Timer Reg Upper a (BRGTRUa)	•BRG Timer Reg Upper a (BRGTRUa)
10001001 (x89)	•BRG Timer Reg Lower a (BRGTRLa)	•BRG Timer Reg Lower a (BRGTRLa)
10001010 (x8A)	•BRG Timer Control Reg (BRGCTCR)	•BRG Timer Control Reg (BRGCTCR)
10001011 (x8B)	• GP Out Clk Reg (GPOC)	• GP Out Clk Reg (GPOC)
10001100 (x8C)	•Current Interrupt Reg (CIR)	•Update CIR
10001101 (x8D)	Reserved	Reserved
10001110 (x8E)	•Global Receive FIFO Reg (GRxFIFO)	•Global Transmit FIFO Reg (GTxFIFO)
10001111 (x8F)	•Global Chip Configuration Reg (GCCR)	•Global Chip Configuration Reg (GCCR)
	UART B	
10010000 (x90)	Mode Register b (MR2b)	Mode Register b (MR2b)
10010001 (x91)	Status Register b (SRb)	Command Register b (CRb)
10010010 (x92)	Interrupt Status Register b (ISRb)	Interrupt Mask Register b (IMRb)
10010011 (x93)	Receiver FIFO Reg b (RxFIFOb)	Transmitter FIFO Reg b (TxFIFOb)
10010100 (x94)	Input Port Reg b (IPRb)	Reserved
10010101 (x95)	I/O Port Interrupt and Output b (I/OPIORb)	I/O Port Interrupt and Output b (I/OPIORb)
10010110 (x96)	Xon/XoffInterrupt Status Reg b (XISRb)	Reserved
10010111 (x97)	GP Output Reg (GPOR)	GP Output Reg (GPOR)
10011000 (x98)	•BRG Timer Reg Upper b (BRGTRUb)	•BRG Timer Reg Upper b (BRGTRUb)
10011001 (x99)	•BRG Timer Reg Lower b (BRGTRLb)	•BRG Timer Reg Lower b (BRGTRLb)
10011010 (x9A)	Reserved	Reserved
10011011 (x9B)	• GP Out Data Reg (GPOD)	• GP Out Data Reg (GPOD)
10011100 (x9C)	•Global Interrupt Channel Reg (GICR)	Reserved
10011101 (x9D)	•Global Interrupt Byte Count (GIBCR)	Reserved
10011110 (x9E)	Reserved	Reserved
10011111 (x9F)	•Global Interrupt Type Register (GITR)	Reserved

A(7:0)	Read	Write
	UART C	
10100000 (xA0)	Mode Register c (MR2c)	Mode Register c (MR2c)
10100001 (xA1)	Status Register c (SRc)	Command Register c (CRc)
10100010 (xA2)	Interrupt Status Register c (ISRc)	Interrupt Mask Register c (IMRc)
10100011 (xA3)	Receiver FIFO Reg c (RxFIFOc)	Transmitter FIFO Reg c (TxFIFOc)
10100100 (xA4)	Input Port Reg c (IPRc)	Reserved
10100101 (xA5)	I/O Port Interrupt and Output c (I/OPIORc)	I/O Port Interrupt and Output c (I/OPIORc)
10100110 (xA6)	Xon/XoffInterrupt Status Reg c (XISRc)	Reserved
10100111 (xA7)	Reserved	Reserved
10101000 (xA8)	Reserved	Reserved
10101001 (xA9)	Reserved	Reserved
10101010 (xAA)	Reserved	Reserved
10101011 (xAB)	Reserved	Reserved
10101100 (xAC)	Reserved	Reserved
10101101 (xAD)	Reserved	Reserved
10101110 (xAE)	Reserved	Reserved
10101111 (xAF)	Reserved	Reserved
	UART D	
10110000 (xB0)	Mode Register d (MR2d)	Mode Register d (MR2d)
10110001 (xB1)	Status Register d (SRd)	Command Register d (CRd)
10110010 (xB2)	Interrupt Status Register d (ISRd)	Interrupt Mask Register d (IMRd)
10110011 (xB3)	Receiver FIFO Reg d (RxFIFOd)	Transmitter FIFO Reg d (TxFIFOd)
10110100 (xB4)	Input Port Reg d (IPRd)	Reserved
10110101 (xB5)	I/O Port Interrupt and Output d (I/OPIORd)	I/O Port Interrupt and Output d (I/OPIORd)
10110110 (xB6)	Xon/XoffInterrupt Status Reg d (XISRd)	Reserved
10110111 (xB7)	Reserved	Reserved
10111000 (xBB)	Reserved	Reserved
10111001 (xB9)	Reserved	Reserved
10111010 (xBA)	Reserved	Reserved
10111011 (xBB)	Reserved	Reserved
10111100 (xBC)	Reserved	Reserved
10111101 (xBD)	Reserved	Reserved
10111110 (xBE)	Reserved	Reserved
10111111 (xBF)	Reserved	Reserved

A(7:0)	Read	Write
	UART E	
11000000 (xC0)	Mode Register e (MR2e)	Mode Register e (MR2e)
11000001 (xC1)	Status Register e (SRe)	Command Register e (CRe)
11000010 (xC2)	Interrupt Status Register e (ISRe)	Interrupt Mask Register e (IMRe)
11000011 (xC3)	Receiver FIFO Reg e (RxFIFOe)	Transmitter FIFO Reg e (TxFIFOe)
11000100 (xC4)	Input Port Reg e (IPRe)	Reserved
11000101 (xC5)	I/O Port Interrupt and Output e (I/OPIORe)	I/O Port Interrupt and Output e (I/OPIORe)
11000110 (xC6)	Xon/XoffInterrupt Status Reg e (XISRe)	Reserved
11000111 (xC7)	Reserved	Reserved
11001000 (xC8)	Reserved	Reserved
11001001 (xC9)	Reserved	Reserved
11001010 (xCA)	Reserved	Reserved
11001011 (xCB)	Reserved	Reserved
11001100 (xCC)	Reserved	Reserved
11001101 (xCD)	Reserved	Reserved
11001110 (xCE)	Reserved	Reserved
11001111 (xCF)	Reserved	Reserved
	UART F	
11010000 (xD0)	Mode Register f (MR2f)	Mode Register f (MR2f)
11010001 (xD1)	Status Register f (SRf)	Command Register f (CRf)
11010010 (xD2)	Interrupt Status Register f (ISRf)	Interrupt Mask Register f (IMRf)
11010011 (xD3)	Receiver FIFO Reg f (RxFIFOf)	Transmitter FIFO Reg f (TxFIFOf)
11010100 (xD4)	Input Port Reg f (IPRf)	Reserved
11010101 (xD5)	I/O Port Interrupt and Output f (I/OPIORf)	I/O Port Interrupt and Output f (I/OPIORf)
11010110 (xD6)	Xon/XoffInterrupt Status Reg f (XISRf)	Reserved
11010111 (xD7)	Reserved	Reserved
11011000 (xD8)	Reserved	Reserved
11011001 (xD9)	Reserved	Reserved
11011010 (xDA)	Reserved	Reserved
11011011 (xDB)	Reserved	Reserved
11011100 (xDC)	Reserved	Reserved
11011101 (xDD)	Reserved	Reserved
11011110 (xDE)	Reserved	Reserved
11011111 (xDF)	Reserved	Reserved

A(7:0)	Read	Write
	UART G	
11100000 (xE0)	Mode Register g (MR2g)	Mode Register g (MR2g)
11100001 (xE1)	Status Register g (SRg)	Command Register g (CRg)
11100010 (xE2)	Interrupt Status Register g (ISRg)	Interrupt Mask Register g (IMRg)
11100011 (xE3)	Receiver FIFO Reg g (RxFIFOg)	Transmitter FIFO Reg g (TxFIFOg)
11100100 (xE4)	Input Port Reg g (IPRg)	Reserved
11100101 (xE5)	I/O Port Interrupt and Output g (I/OPIORg)	I/O Port Interrupt and Output g (I/OPIORg)
11100110 (xE6)	Xon/XoffInterrupt Status Reg g (XISRg)	Reserved
11100111 (xE7)	Reserved	Reserved
11101000 (xE8)	Reserved	Reserved
11101001 (xE9)	Reserved	Reserved
11101010 (xEA)	Reserved	Reserved
11101011 (xEB)	Reserved	Reserved
11101100 (xEC)	Reserved	Reserved
11101101 (xED)	Reserved	Reserved
11101110 (xEE)	Reserved	Reserved
11101111 (xEF)	Reserved	Reserved
	UART H	
11110000 (xF0)	Mode Register h (MR2h)	Mode Register h (MR2h)
11110001 (xF1)	Status Register h (SRh)	Command Register h (CRh)
11110010 (xF2)	Interrupt Status Register h (ISRh)	Interrupt Mask Register h (IMRh)
11110011 (xF3)	Receiver FIFO Reg h (RxFIFOh)	Transmitter FIFO Reg h (TxFIFOh)
11110100 (xF4)	Input Port Reg h (IPRh)	Reserved
11110101 (xF5)	I/O Port Interrupt and Output h (I/OPIORh)	I/O Port Interrupt and Output h (I/OPIORh)
11110110 (xF6)	Xon/XoffInterrupt Status Reg h (XISRh)	Reserved
11110111 (xF7)	Reserved	Reserved
11111000 (xF8)	Reserved	Reserved
11111001 (xF9)	Reserved	Reserved
11111010 (xFA)	Reserved	Reserved
11111011 (xFB)	Reserved	Reserved
11111100 (xFC)	Reserved	Reserved
11111101 (xFD)	Reserved	Reserved
11111110 (xFE)	Reserved	Reserved
11111111 (xFF)	Reserved	Reserved

RESET CONDITONS

Device Configuration after Hardware Reset or CRa cmd=x1F

Cleared registers:

Channel Status Registers (SR)
Channel Interrupt Status Registers (ISR)
Channel Interrupt Mask Registers (IMR)
Channel Interrupt Xon Status Register (XISR)
Interrupt Control Register (ICR)
Global Configuration Control Register (GCCR)
- Hence the device enters the asynchronous bus cycling mode.

Current Interrupt Register (CIR)
Counter/Timer Run Control Register (CTRCR)
Watch-dog Timer Run Control Register (WDTRCR)
Channel Input/Output Port Configuration Registers (I/OPCR)
- Hence all I/O pins have direction = Input after reset

BRG Counter/Timer Registers

Clears Modes for:

Power down
Test modes
Input Port Changed bits
Gang write to Xon or Xoff
Xon/Xoff/Address detection
Receiver error status

Disables:

Transmitters
Receivers
Interrupts, current and future

Halts:

BRG Counters
Bus cycle in progress (hardware RESET only)

Limitations:

Minimum RESETN pin pulse width is 10 SClk cycles **after Vcc reaches operational range**

The user must allow a minimum of 6 SClk cycles to elapse after a reset (RESETN pin or CRa initiated) of the device terminates before initiating a new bus cycle.

ENGINEERING CHANGES FROM 26C94

NEW FEATURES

3.3 volt or 5 volt operation

Address recognition, Xon/Xoff character generation and detection

RAM storage with embedded XOR detection circuitry. New control registers are also RAM based. New logic will be inserted between existing FIFOs and T/RSRGs. Controlling state machines will be random logic or PLA based. Xon/Xoff works by tapping into the CTS (Clear To Send) logic. Address recognition will tie into interrupt logic, status and receive logic.

GP pins

Introduction of small number of General Purpose Input (2) and General Purpose Output (2) pins. These are widely available to all channels, but are primarily intended for use with the new BRG counter/timers.

General Purpose outputs mux selectable for:

- BRG Counter timers
- One of the new Global output register bits
- selected TxC1x, TxC16x, RxC16x from channels
- total of 16 selection

General Purpose inputs selectable for:

- BRG Counter timer
- ETxC of any channel
- ERxC of any channel
- load and/or data signals for GPOs
- total of 40 destinations

NOTE: a GPI may be selected for any or all of these simultaneously

Addition of 3 output bits for General Purpose Output

Available through the General Purpose Output Pin, Gout0

Read/Write interface to the host CPU

May be clocked by and/or capture GP inputs

DC and AC Preliminary

Timing Parameters

Some of these parameters will change as characterization reveals actual values over process parameters, voltage and temperature. Others will be added.

DC ELECTRICAL SPECIFICATIONS (for V_{CC} = 5.0 V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{IL} V_{IH} V_{IH}	Input low voltage (V_{CC} = 3.3V) Input high voltage (except X1/CLK) (V_{CC} = 3.3V) Input high voltage (X1/CLK)		 2.2 V_{CC}-0.1V_{CC} 0.8V_{CC}		0.8 V_{SS}+0.1V_{CC} V_{CC}	V
V_{OL} V_{OH}	Output low voltage Output high voltage (except OD outputs)	I/OL = 2.4mA I/OH = -400µA I/OH = -100µA	 0.8V_{CC} 0.9V_{CC}		0.4	V
I_{IL} I_{IH}	Input current low, I/O pins Input current high, I/O pins	V_{IN} = 0 V_{IN} = V_{CC}	-10		10	µA
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	-5		5	µA
I_{IKX1} I_{IHX1}	X1/CLK input low current X1/CLK input high current	V_{IN}=GND,X2=Open V_{IN}=V_{CC}, X2=Open	-100		+100	µA
I_{OZH} I_{OZL}	Output off current high, 3-state data bus Output off current low, 3-state data bus	V_{IN} = V_{CC} V_{IN} = 0	-10		10	µA
I_{ODL} I_{ODH}	Open-drain output low current in off state Open drain output high current in off state	V_{IN} = V_{CC} V_{IN} = V_{CC}	-10		10	µA
I_{CC}	Power supply current Operating mode Power down mode (no clocks operating)	TTL Input levels CMOS input levels CMOS input levels			225 75 75	mA mA µA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	FIGURE	PARAMETER	LIMITS			UNIT
			MIN	TYP	MAX	
RESET TIMING						
t_{RES}		RESET pulse width	10			Sclk
BUS TIMING						
t_{AS}		A0-A7 setup time before Sclk C3 rising edge	10	3		ns
t_{AH}		A0-A7 hold time after Sclk C3 rising edge	18	12		ns
t_{CS}		CEN setup time before Sclk C1 high (ASYNC)	5			ns
		CEN setup time before Sclk C2 high (SYNC)	5			
t_{CH}		CEN hold time after Sclk C3 high (SYNC)	15	1.5 Sclk		ns
		CEN hold time after Sclk C4 high (ASYNC)[1]	25	1.5 Sclk		ns
t_{STP}		CEN high after C4 end. To terminate cycle (SYNC)			18	Sclk
t_{RWS}		W-Rn setup time before Sclk C2 rising edge	5			ns
t_{RWH}		W-Rn hold time after Sclk C3 rising edge	20	1.5 Sclk		ns
t_{DD}		Read cycle Data valid after Sclk C3 falling edge		25	37	ns
t_{DF}		Read cycle data bus floating after CEN high (ASYNC)		20	35	ns
		Read cycle data bus floating after C4 end (SYNC)		20	35	
t_{DS}		Write cycle data setup time before Sclk C4 rising edge	25	15		ns
t_{DH}		Write cycle data hold time after Sclk C4 rising edge	30	18		ns
t_{RWD}		High time between CEN low (ASYNC)	12	10		ns
I/O PORT PIN TIMING						
t_{PS}		I/O input setup time before Sclk C3 falling edge (Read IPR)	20			ns
t_{PH}		I/O input hold time after Sclk C4 rising edge (Read IPR)	18			ns
t_{PD}		I/O output valid from: Write Sclk C4 rising edge (write to I/OPIOR)			50	ns
INTERRUPT TIMING						
t_{IR}		IRQN from: Internal interrupt source active bid Software reset to IRQN inactive Write IMR (clear IMR bit after C4 end)	22	3	43 50	Sclk Sclk ns
Tx / Rx CLOCK TIMING, External[2]						
t_{RX}		RxC high or low time	20			ns
f_{RX}		RxC frequency (16 X) (1 X)	0 0		16 1	MHz
t_{TX}		TxC high or low time	20			ns
f_{TX}		TxC frequency (16 X) (1 X)	0 0		16 1	MHz
t_{RF}		Tx / Rx clock rise and fall times			20	ns
TRANSMITTER TIMING						
t_{TXD}		TxD output delay from TxC low			100	ns
t_{TCS}		TxC output delay from TxD output data	-20		20	ns
RECEIVER TIMING						
t_{RXS}		RxD data setup time to RxC high (data)	30			ns
RXH		RxD data hold time from RxC high (data)	30			ns
TsSTRT		RxD data setup time to RxC high (Start Bit)	17 / 32			16X clk
Sclk TIMING[3]						
Tsclkl		Min low time at Vil (0.8V)	11			ns
Tsclkh		Min high time at Vih (2.0V)	11			ns
Fsclk		Sclk frequency			33	MHz
T/RFsclk		Sclk rise/fall time (0.8 to 2.0Volts)			3 / 3	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	FIGURE	PARAMETER	LIMITS			UNIT
			MIN	TYP	MAX	
X1 / X2 COMMUNICATION CRYSTAL CLOCK[2]						
Fx1		X1 clock frequency	0	3.6864	8.0	MHz
X1 L / H		X1 Low / High time	20			ns
T/RFx1		X1 Rise / Fall time			10/10	ns
COUNTER / TIMER BAUD RATE CLOCK (EXTERNAL CLOCK INPUT)						
FC/T		Clock frequency	0		16	MHz
TC/TLH		C/T high and low time	30			ns
TC/TO		Delay C/T clock external to output pin			60	ns
DACKN TIMING[4]						
DAKdly		DACK low from Sclk C4 rising edge			25	ns
DAKdlya		DACK high from CEN high (ASYNC)		28	40	ns
DAKdlys		DACK high from C4 end rising edge (SYNC)		28	40	ns
I/O PORT External Clock						
Tgpirtx		GPI to Rx/Tx clock out		TBD		ns
		RxD setup to I/OP rising edge 1X mode		TBD		ns
		I/OP falling edge to TxD out 1X mode		TBD		ns
Gout TIMING						
GPOtdd		GPO valid after write to GPOR		TBD		ns

NOTES:
1. The ASYNC pulse width low must include 4 rising edges plus the setup & hold times. For those applications where the control processor has no knowledge of the Sclk period, this will imply a CEN period of 5 Sclk rising edges.
2. Production test will use rise and fall time less than 7ns. Specified rise and fall times are guaranteed by design.
3. Sclk is required for proper bus timing. Sclk must always be faster than twice the fastest 1X data clock.
4. The meaning of DACKN is that data will be valid before the end of the C4 time.

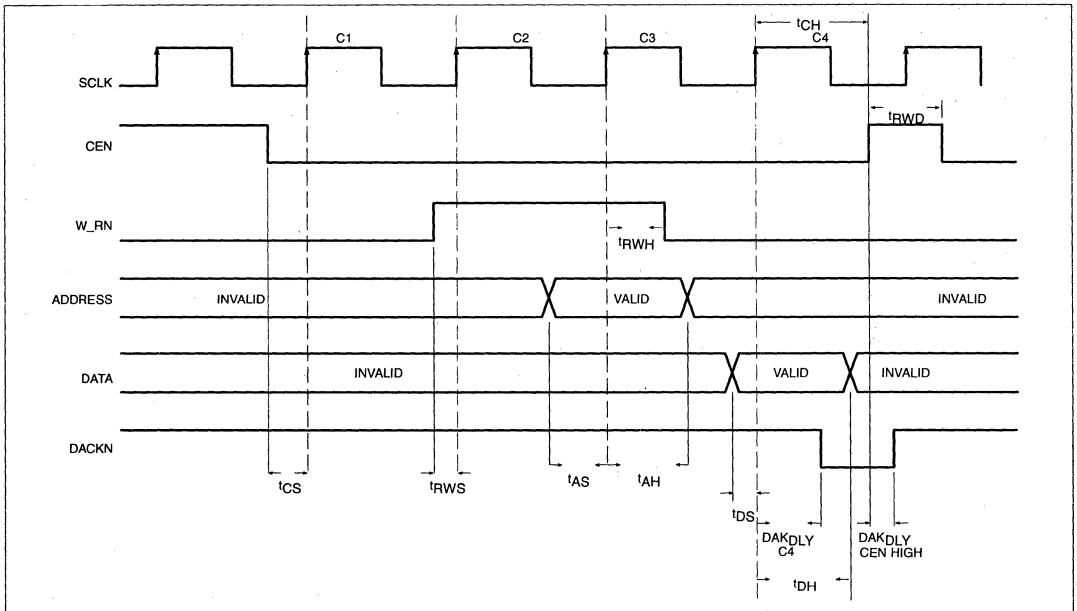


Figure 1. Basic Write Cycle, ASYNC

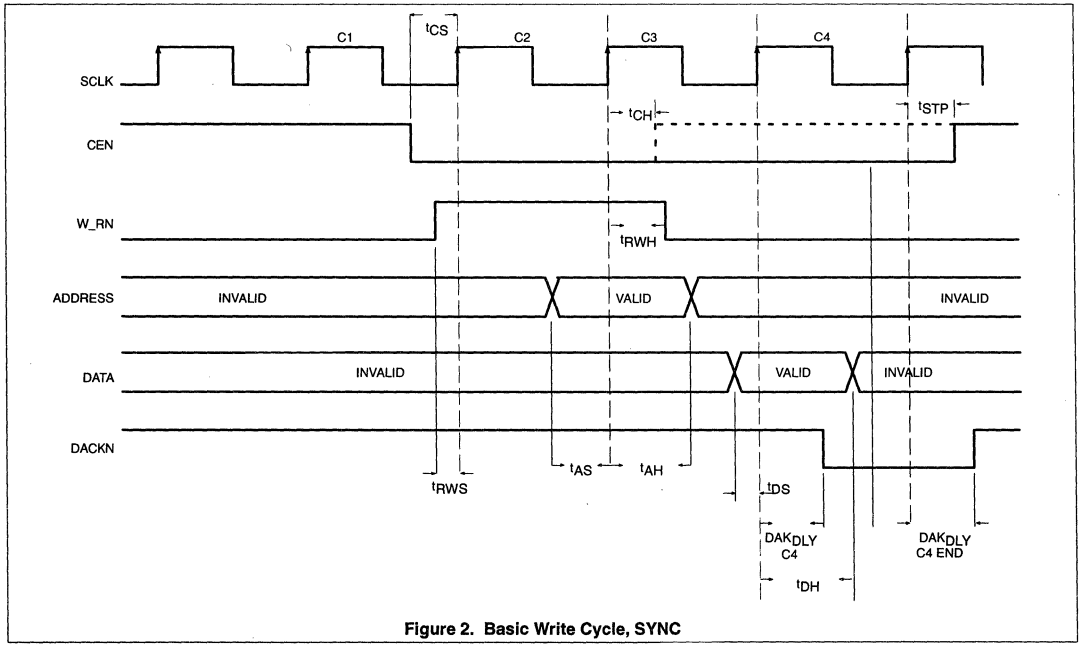


Figure 2. Basic Write Cycle, SYNC

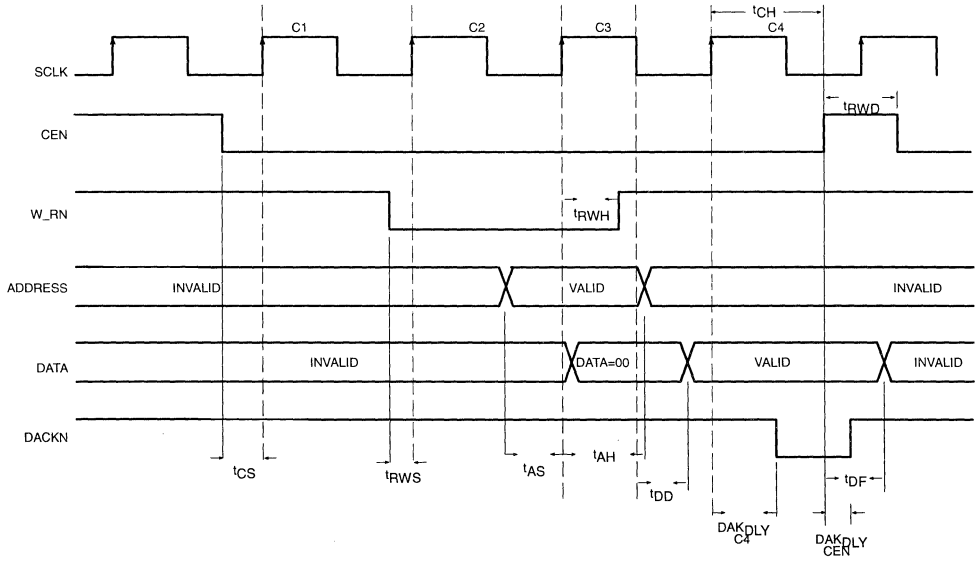


Figure 3. Basic Read Cycle, ASYNC

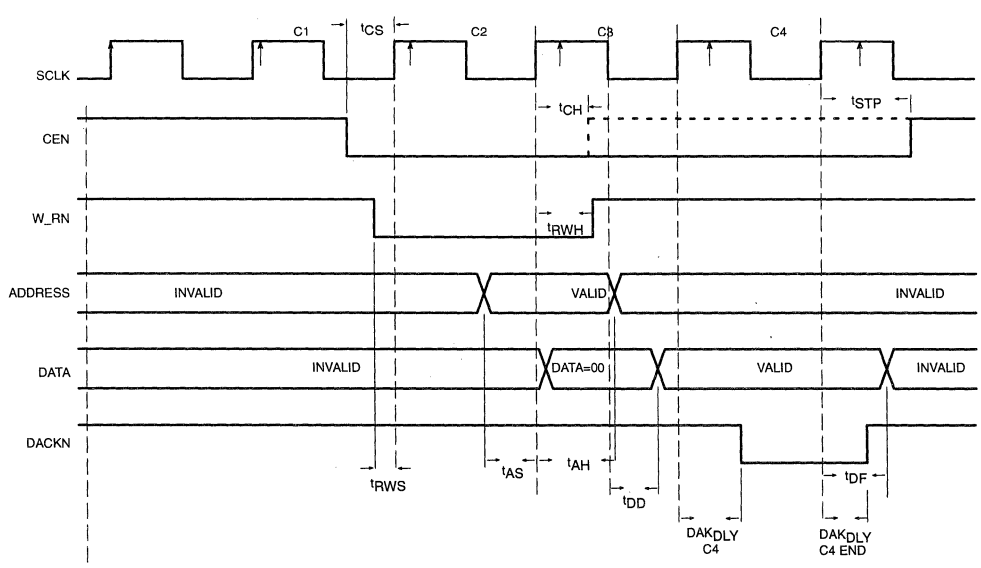


Figure 4. Basic Read Cycle, SYNC

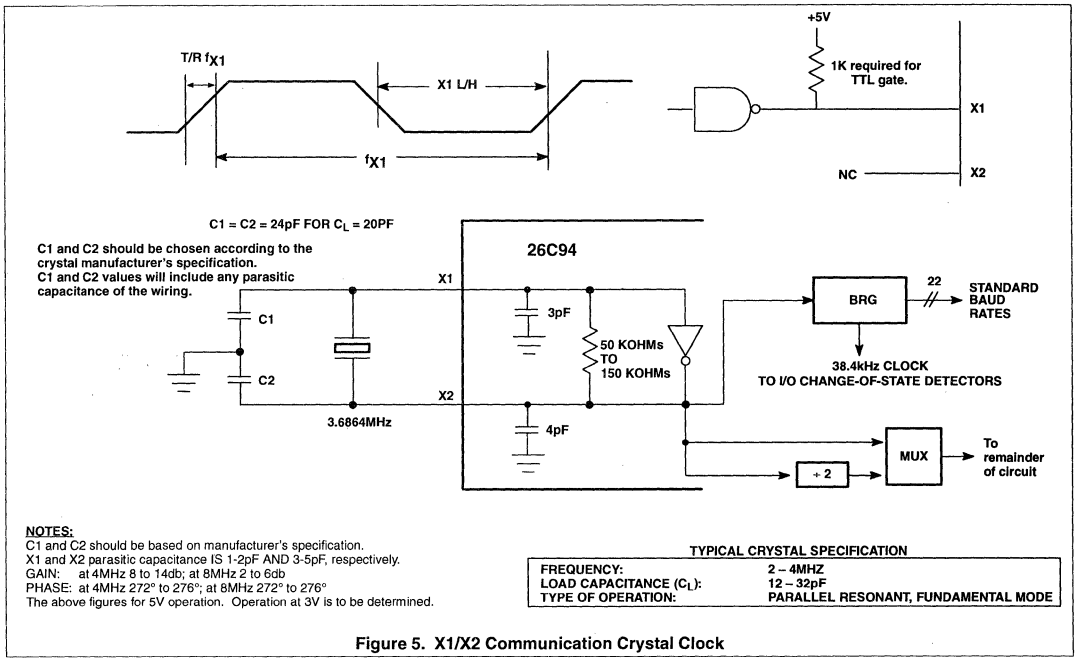


Figure 5. X1/X2 Communication Crystal Clock

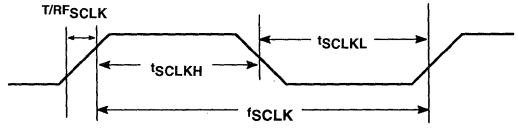


Figure 6. SCLK Timing

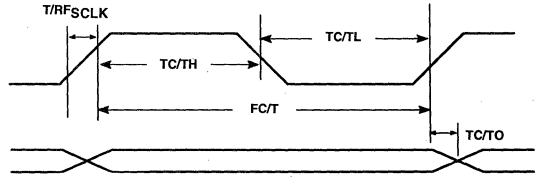


Figure 7. Counter/Timer Baud Rate Clock, External

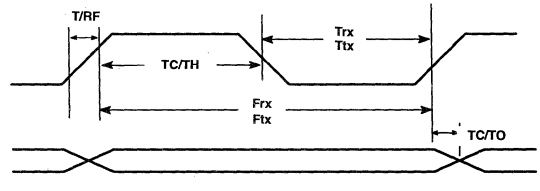


Figure 8. Tx / Rx Clock Timing, External

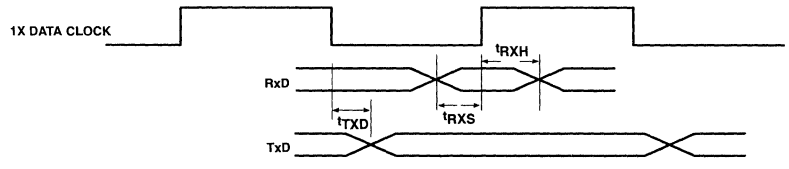


Figure 9. Transmitter and Receiver Timing

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Dual universal serial communications controller (DUSCC) SCN26562

DESCRIPTION

The Philips Semiconductors SCN26562 Dual Universal Serial Communications Controller (DUSCC) is a single-chip MOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SCN26562 interfaces to synchronous bus MPUs and is capable of program-polled, interrupt driven, block-move or DMA data transfers.

The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multi-function counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides 16 common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the DUSCC well suited for dual-speed channel applications. Data rates up to 4Mbits per second are supported.

The transmitter and receiver each contain a four-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to four characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs and outputs are general purpose in nature, they can be optionally programmed for other functions.

This document contains the electrical specifications for the SCN26562. See SCN26562/SCN68562 User's Guide for complete functional description.

FEATURES

General Features

- Dual full-duplex synchronous/asynchronous receiver and transmitter
- Multiprotocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: BISYNC, DDCMP
  - ASYNC: 5–8 bits plus optional parity
- Four character receiver and transmitter FIFOs
- 0 to 4Mbit/sec data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 16 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- and half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Single- or dual-address dual transfers
  - Half- or full-duplex operation
  - Automatic frame termination on counter/timer terminal count or DMA EOPN input
- Interrupt capabilities
  - Vector output (fixed or modified by status)
  - Programmable internal priorities
  - Maskable interrupt conditions
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general purpose pins per channel
  - CTS and DCD programmable auto-enables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X and Tx clock factors
- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search 1/2-bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmits up to 4Mbit/sec data rate Receives up to 2Mbit/sec data rate

Character-Oriented Protocol Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK line-fill on underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun, and underrun error detection

BISYNC Features

- EBCDIC or ASCII header, text and control messages
- SYN, DLE stripping
- EOM (end of message) detection and transmission
- Auto transparent mode switching
- Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
- Control character sequence detection for both transparent and normal text

Bit-Oriented Protocol Features

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for I field
- Zero insertion and detection
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- ABORT, ABORT-FLAGs, or FCS FLAGs line-fill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±5%, T_A = 0°C to +70°C		DWG #
	Serial Data Rate = 2.5Mbps Maximum	Serial Data Rate = 4Mbps Maximum	
48-Pin Plastic Dual In-Line Package (DIP)	SCN26562C2N48	SCN26562C4N48	0416C
52-Pin Plastic Leaded Chip Carrier (PLCC) Package	SCN26562C2A52	SCN26562C4A52	0397E

ABSOLUTE MAXIMUM RATINGS[1]

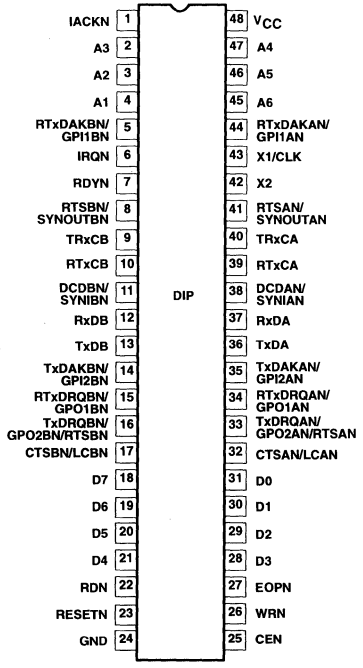
SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature[2]	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	–0.5 to +7.0	V
V_S	Voltage from any pin to ground[3]	–0.5 to V_{CC} +0.5	V

NOTES:

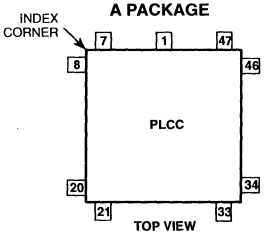
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 36°C/W junction to ambient for ceramic DIP, 40°C/W for plastic DIP, and 42°C/W for PLCC.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

PIN CONFIGURATIONS

N PACKAGE



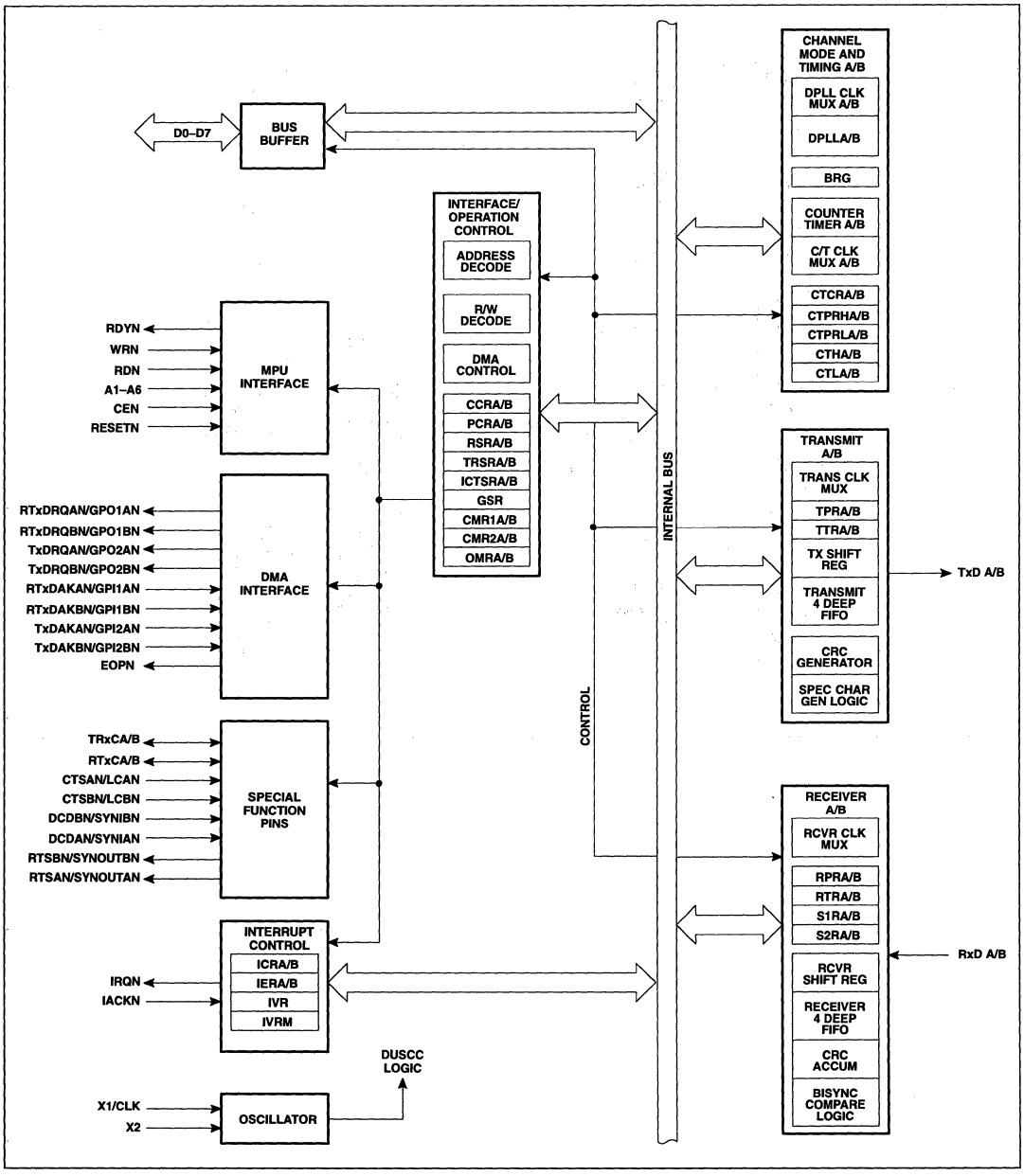
A PACKAGE



TOP VIEW

PIN	FUNCTION	PIN	FUNCTION
1	IACKN	27	CEN
2	A3	28	WRN
3	A2	29	EOPN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
		32	D1
6	IRQN	33	D0
7	NC	34	NC
8	RDYN	35	CTSAN/LCAN
9	RTSBN/ SYNOUTBN	36	TxDRQAN/ GPO2AN/RTSAN
10	TRxCB	37	RTxDRQAN/ GPO1AN
11	RTxCB		
12	DCDBN/ SYNIBN	38	TxDAKAN/ GPI2AN
13	NC	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	NC
16	TxDAKBN/ GPI2BN	42	DCDAN/ SYNIAN
17	RTxDRQBN/ GPO1BN	43	RTxCA
		44	TRxCA
18	TxDRQBN/ GPO2BN/RTSBN	45	RTSAN/ SYNOUTAN
19	CTSBN/LCBN	46	X2
20	D7	47	X1/CLK
21	D6	48	RTxDAKAN/ GPI1AN
22	D5		
23	D4	49	A6
24	RDN	50	A5
25	RESETN	51	A4
26	GND	52	VCC

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A1–A6	4–2, 47–45	4–2, 51–49	I	Address lines.
D0–D7	31–28, 21–18	33–30, 23–20	I/O	Bidirectional data bus.
RDN	22	24	I	Read strobe.
WRN	26	28	I	Write strobe.
CEN	25	27	I	Chip select.
RDYN	7	8	O	Ready.
IRQN	6	6	O	Interrupt request.
IACKN	1	1	I	Interrupt acknowledge.
X1/CLK	43	47	I	Crystal 1 or external clock.
X2	42	46	I	Crystal 2.
RESETN	23	25	I	Master reset.
RxDA, RxDB	37, 12	40, 14	I	Channel A (B) receiver serial data.
TxDA, TxDB	36, 13	39, 15	O	Channel A (B) transmitter serial data.
RTxCA, RTxCB	39, 10	43, 11	I/O	Channel A (B) receiver/transmitter clock.
TRxCA, TRxCB	40, 9	44, 10	I/O	Channel A (B) transmitter/receiver clock.
CTSA/BN, LCA/BN	32, 17	35, 19	I/O	Channel A (B) clear-to-send input or loop control output.
DCDA/BN, SYNIA/BN	38, 11	42, 12	I	Channel A (B) data carrier detected or external sync.
RTxDRQA/BN, GPO1A/BN	34, 15	37, 17	O	Channel A (B) receiver/transmitter DMA service request or general purpose output.
TxDRQA/BN, GPO2A/BN, RTSA/BN	33, 16	36, 18	O	Channel A (B) transmitter DMA service request, general purpose output or request-to-send.
RTxDAKA/BN, GPI1A/BN	44, 5	48, 5	I	Channel A (B) receiver/transmitter DMA acknowledge or general purpose input 1.
TxDAKA/BN, GPI2A/BN	35, 14	38, 16	I	Channel A (B) transmitter DMA acknowledge or general purpose input 2.
EOPN	27	29	I/O	DMA transfer complete.
RTSA/BN, SYNOUTA/BN	41, 8	45, 9	O	Channel A (B) request-to-send or Sync detect.
V_{CC}	48	52	I	Power input.
GND	24	26	I	Signal and power ground.

DC ELECTRICAL CHARACTERISTICS[1, 3] T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage: All except X1/CLK				0.8	V
	X1/CLK				0.4	V
V_{IH}	Input high voltage: All except X1/CLK		2.0			V
	X1/CLK		2.4		V_{CC}	V
V_{OL}	Output low voltage: All except IRQN	I_{OL} = 5.3mA				V
	IRQN	I_{OL} = 8.8mA			0.5	V
V_{OH}	Output high voltage: (Except open drain outputs)	I_{OH} = −400µA	2.4		0.5	V
I_{ILX1} I_{IHX1}	X1/CLK input low current[3] X1/CLK input high current[3]	V_{IN} = 0, X2 = GND V_{IN} = V_{CC}, X2 = GND	−5.5		0.0 1.0	mA mA
I_{ILX2} I_{IHX2}	X2 input low current[3] X2 input high current[3]	V_{IN} = 0, X1 = open V_{IN} = V_{CC}, X1 = open	−100		 100	µA µA
I_{IL}	Input low current RESETN, TxDAKN, RxDAKN	V_{IN} = 0	−40			µA
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	−5		5	µA
I_{OZH} I_{OZL}	Output off current high, 3-State data bus Output off current low, 3-State data bus	V_{IN} = V_{CC} V_{IN} = 0	 −5		5	µA µA
I_{ODL}	Open drain output low current in off state: EOPN	V_{IN} = 0			−25	µA
	IRQN, RDYN		−120			µA
I_{ODH}	Open drain output high current in off state: EOPN, IRQN, RDYN	V_{IN} = V_{CC}	−5		5	µA
I_{CC}	Power supply current	V_O = 0 to V_{CC}			275	mA
C_{IN}	Input capacitance[2]	V_{CC} = GND = 0			10	pF
C_{OUT}	Output capacitance[2]	V_{CC} = GND = 0			15	pF
$C_{I/O}$	Input/output capacitance[2]	V_{CC} = GND = 0			20	pF

NOTES:
1. Parameters are valid over specified temperature range.
2. These values were not explicitly tested; they are guaranteed by design and characterization data.
3. X1/CLK and X2 are not tested with a crystal installed.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3, 4] T_A = 0°C to +70°C, V_{CC} = 5V ±5%

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RELREH}	RESETN low to RESETN high	1.2		1.2		µs

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.8V and 2.0V with a transition time of 20ns maximum. For X1/CLK, this swing is between 0.4V and 2.4V. All time measurements are referenced at input voltages of 0.4V and 2.4V and output voltages of 1.2V and 2.0V, as appropriate.
3. See Figure 16 for test conditions for outputs.
4. Tests for open drain outputs are intended to guarantee switching of the output transistor. Measurement of this response is referenced from midpoint of the switching signal to a point 0.2V above the actual output signal level. This point represents noise margin that assures true switching has occurred.

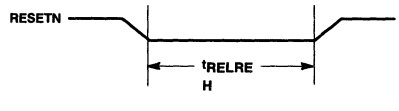
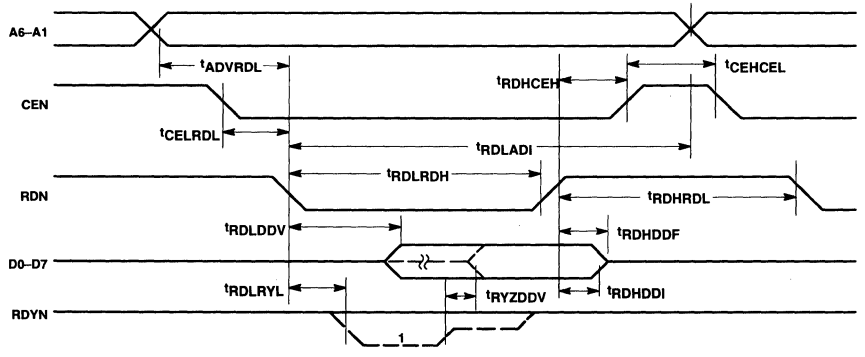


Figure 1. Reset Timing

AC ELECTRICAL CHARACTERISTICS (Continued)



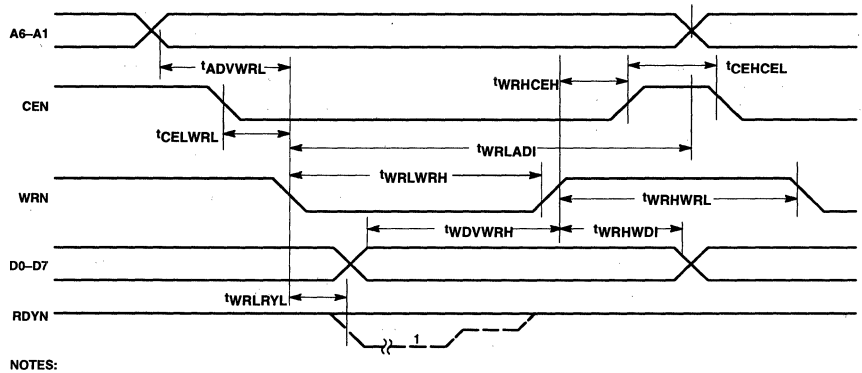
NOTES:

1. Wait on Rx. Receiver FIFO empty.
2. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.

Figure 2. Read Cycle

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{ADVRDL}	Address valid to RDN low	10		10		ns
t_{CELRDL}	CEN low to RDN low	0		0		ns
t_{RDLADI}	RDN low to address invalid	150		150		ns
t_{RDLRYL}	RDN low to RDYN low		275		275	ns
t_{RDLDDV}	RDN low to read data valid		280		300	ns
t_{RDLRDH}	RDN low to RDN high	300		310		ns
t_{RYZDDV}	RDYN high impedance to read data valid		100		100	ns
t_{RDHCEH}	RDN high to CEN high	0		0		ns
t_{CEHCEL}	CEN high to CEN low	160		170		ns
t_{RDHDDI}	RDN high to read data invalid	10		10		ns
t_{RDHRDL}	RDN high to RDN low	160		170		ns
t_{RDHDDF}	RDN high to data bus floating		75		75	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

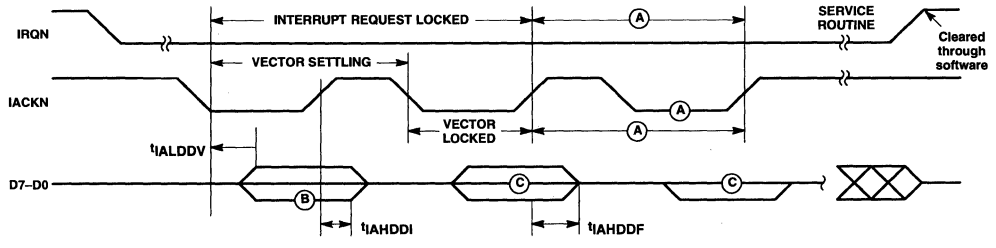


NOTES:
1. Wait on Tx. Transmitter FIFO full.
2. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CEN as the 'strobing' input. CEN and RDN (also CEN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.

Figure 3. Write Cycle

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{ADVWRL}	Address valid to WRN low	10		10		ns
t_{CELWRL}	CEN low to WRN low	0		0		ns
t_{WRLRYL}	WRN low to READY low					ns
t_{WRHCEH}	WRN high to CEN high	0		0		ns
t_{WRLWRH}	WRN low to WRN high	300		310		ns
t_{WDVWRH}	Write data valid to WRN high	100	275	100	275	ns
t_{CEHCEL}	CEN high to CEN low	160		170		ns
t_{WRLADI}	WRN low to address invalid	150		150		ns
t_{WRHWRL}	WRN high to WRN low	160		170		ns
t_{WRHWDI}	WRN high to write data invalid	10		10		ns

AC ELECTRICAL CHARACTERISTICS (Continued)



NOTES:
(A) ICR[5:4] = 01 or 10 (mode 1 or mode 2)
(B) Call instruction (mode 2)
(C) ICR[5:4] = 11 (mode 3)

Figure 4. Interrupt Acknowledge Cycle

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{IALDDV}	IACKN low to data bus valid		280		280	ns
t_{IAHDDF}	IACKN high to data bus floating		150		150	ns
t_{IAHDDI}	IACKN high to data bus invalid	10		10		ns

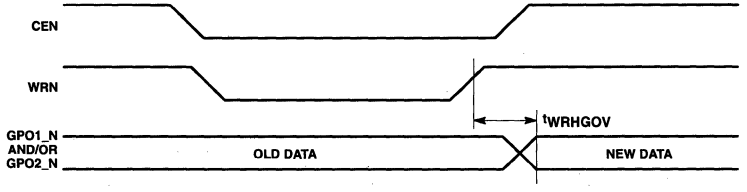


Figure 5. Output Port Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{WRHGOV}	WRN high to GPO output data valid		300		300	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

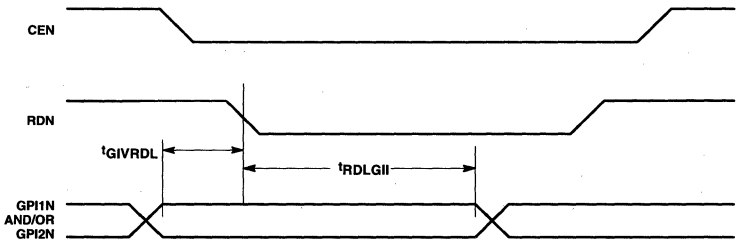


Figure 6. Input Port Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{GIVRDL}	GPI input valid to RDN low	20		20		ns
t_{RDLGII}	RDN low to GPI input invalid	100		100		ns

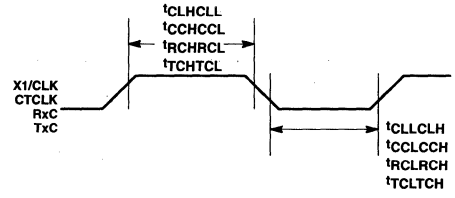


Figure 7. Clock Timing

SYMBOL	PARAMETER	LIMITS						UNIT
		SCN26562C4			SCN26562C2			
		Min	Typ	Max	Min	Typ	Max	
t_{CLHCLL}	X1/CLK high to low time	25			25			ns
t_{CLLCLH}	X1/CLK low to high time	25			25			ns
t_{CCHCCL}	C/T CLK high to low time	100			100			ns
t_{CCLCCH}	C/T CLK low to high time	100			100			ns
t_{RCHRCL}	RxC high to low time	110			150			ns
t_{RCLRCH}	RxC low to high time	110			150			ns
t_{TCHTCL}	TxC high to low time	110			150			ns
t_{TCLTCH}	TxC low to high time	110			150			ns
f_{CL}	X1/CLK frequency	2.0		16.0	2.0		16.0	MHz
f_{CC}	C/T CLK frequency	0	14.7456	4.0	0	14.7456	4.0	MHz
f_{RC}	RxC frequency (16X or 1X)	0		4.0	0		2.5	MHz
f_{TC}	TxC frequency (16X or 1X)	0		4.0	0		2.5	MHz

AC ELECTRICAL CHARACTERISTICS (Continued)

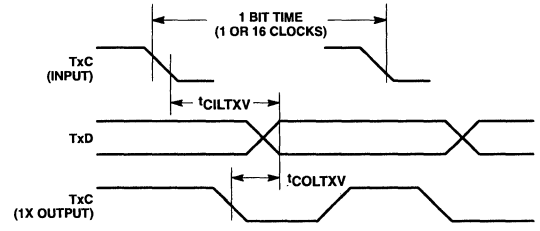


Figure 8. Transmit Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{CILTXV}	TxC input low (1X) to TxD output		240		240	ns
	TxC input low (16X) to TxD output		435		435	ns
t_{COLTXV}	TxC output low to TxD output		50		50	ns

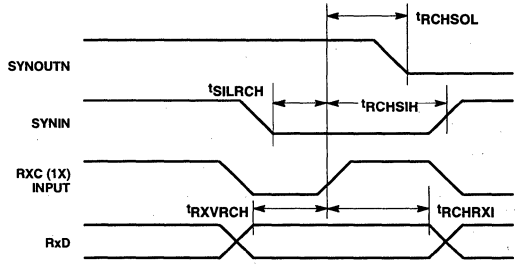
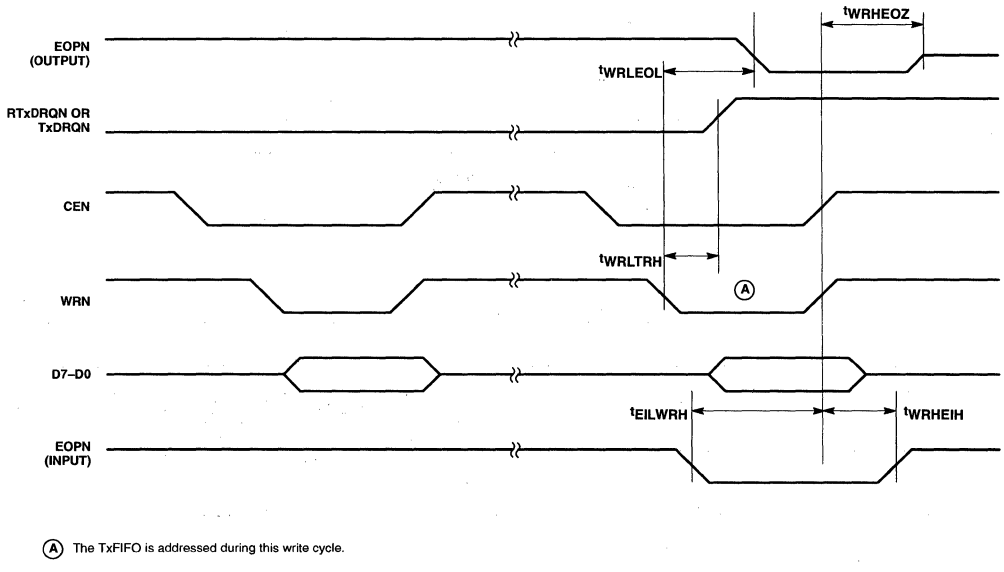


Figure 9. Receive Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RXVRCH}	RxD data valid to RxC high:					
	For NRZ data	50		50		ns
t_{RCHRXI}	For NRZI, Manchester, FM0, FM1 data	120		130		ns
	RxC high to RxD data invalid:					
	For NRZ data	50		50		ns
	For NRZI, Manchester, FM0, FM1 data	10		10		ns
t_{SILRCH}	SYNIN low to RxC high	100		100		ns
t_{RCHSIH}	RxC high to SYNIN high	50		50		ns
t_{RCHSOL}	RxC high to SYNOUT low		300		300	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

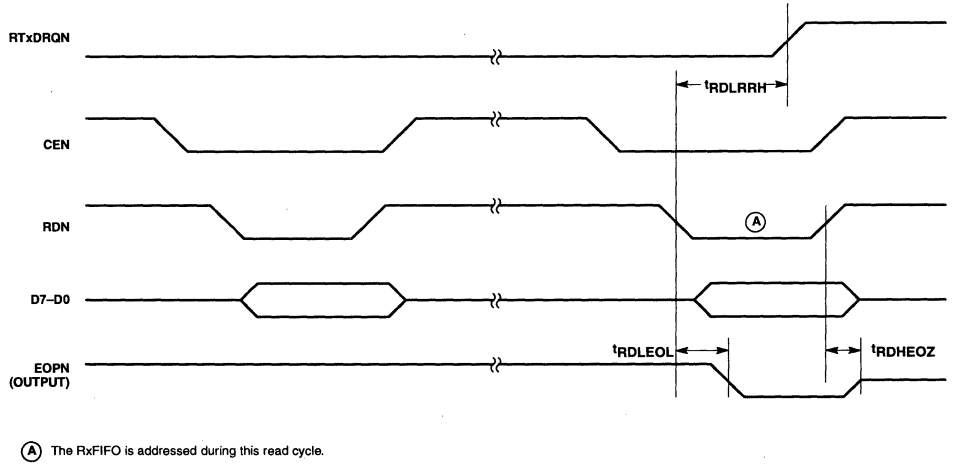


(A) The TxFIFO is addressed during this write cycle.

Figure 10. Transmit Dual Address DMA Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{WRLTRH}	WRN low to Tx DMA REQN high					ns
t_{WRLEOL}	WRN low to EOPN output low		320		320	ns
t_{WRHEOZ}	WRN high to EOPN output high impedance		225		225	ns
t_{EILWRH}	EOPN input low to WRN high	50	225	50	225	ns
t_{WRHEIH}	WRN high to EOPN input high	50		50		ns

AC ELECTRICAL CHARACTERISTICS (Continued)

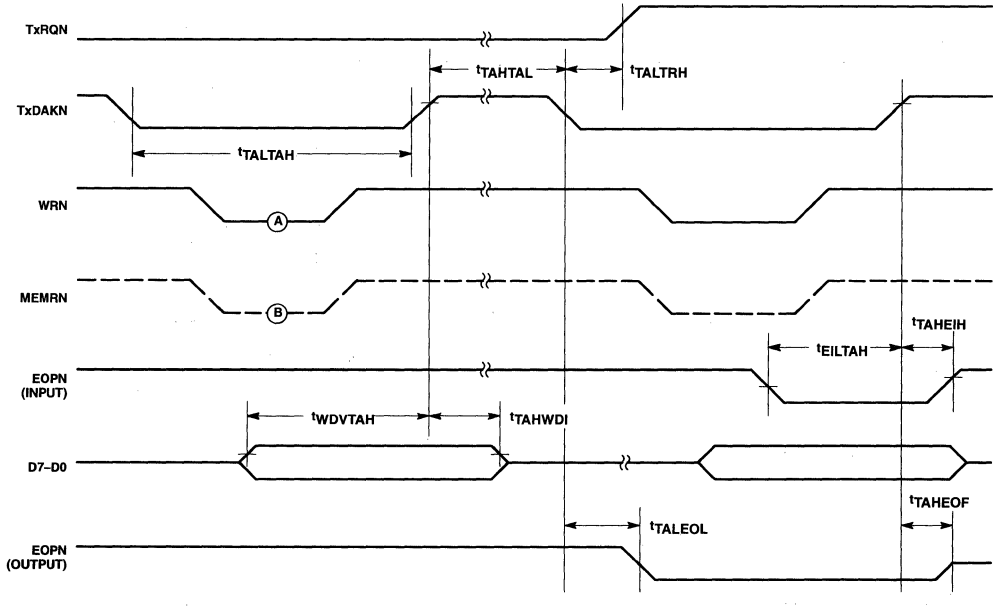


(A) The RxFIFO is addressed during this read cycle.

Figure 11. Receive Dual Address DMA Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RDLRRH}	RDN low to Rx DMA REQN high		320		320	ns
t_{RDLEOL}	RDN low to EOPN output low		300		300	ns
t_{RDHEOZ}	RDN high to EOPN output high impedance		225		225	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

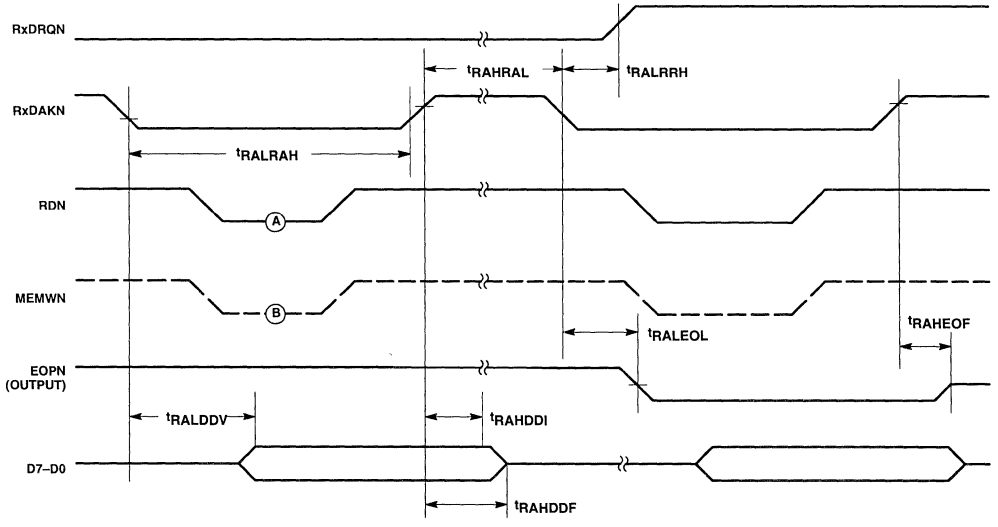


NOTES:
(A) Ignored by the DUSCC since CEN is not asserted, but it can be used externally to qualify TxDAKN.
(B) Memory read signal; not seen by DUSCC.

Figure 12. DMA-Transmit Single Address Mode

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{TAHTAL}	Transmit DMA ACKN high to low time	100		100		ns
t_{TALTAH}	Transmit DMA ACKN low to high time	250		250		ns
t_{TALTRH}	Tx DMA ACKN low to Tx DMA REQN high					ns
t_{WDVTAH}	Write data valid to Tx DMA ACKN high	90	250	90	250	ns
t_{TAHWDI}	Tx DMA ACKN high to write data invalid	30		30		ns
t_{TALEOL}	Tx DMA ACKN low to EOPN output low					ns
t_{TAHEOF}	Tx DMA ACKN high to EOPN output float		170		170	ns
t_{EILTAH}	EOPN input low to Tx DMA ACKN high	50	200	50	200	ns
t_{TAHEIH}	Tx DMA ACKN high to EOPN input high	50		50		ns

AC ELECTRICAL CHARACTERISTICS (Continued)



NOTES:
(A) Ignored by the DUSCC bit; it can be used to qualify RxDAKN.
(B) Memory read signal; not seen by DUSCC.

Figure 13. DMA-Receive Single Address Mode

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RAHRAL}	Receive DMA ACKN high to low time	160		160		ns
t_{RALRAH}	Receive DMA ACKN low to high time	250		250		ns
t_{RALRRH}	Rx DMA ACKN low to Rx DMA REQN high		320		320	ns
t_{RALEOL}	Rx DMA ACKN low to EOPN output low		200		200	ns
t_{RAHEOF}	Rx DMA ACKN high to EOPN output float		225		225	ns
t_{RALDDV}	Rx DMA ACKN low to read data valid		225		225	ns
t_{RAHDDI}	Rx DMA ACKN high to read data invalid	10		10		ns
t_{RAHDDF}	Rx DMA ACKN high to data bus float		125		125	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

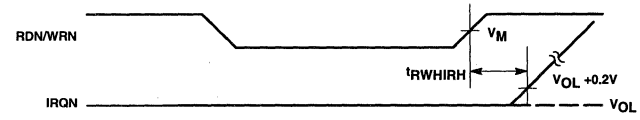


Figure 14. Interrupt Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		SCN26562C4		SCN26562C2		
		Min	Max	Min	Max	
t_{RWHIRH}	RDN/WRN high to IRQN high for:					
	Read RxFIFO (RxRDY interrupt)		450		450	ns
	Write TxFIFO (TxRDY interrupt)		450		450	ns
	Write RSR (Rx condition interrupt)		400		400	ns
	Write TRSR (Rx/Tx interrupt)		400		400	ns
	Write ICTSR (counter/timer interrupt)		400		400	ns

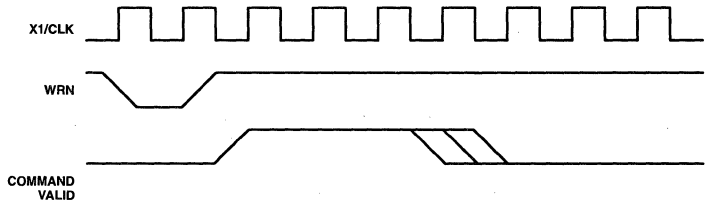


Figure 15. Command Timing

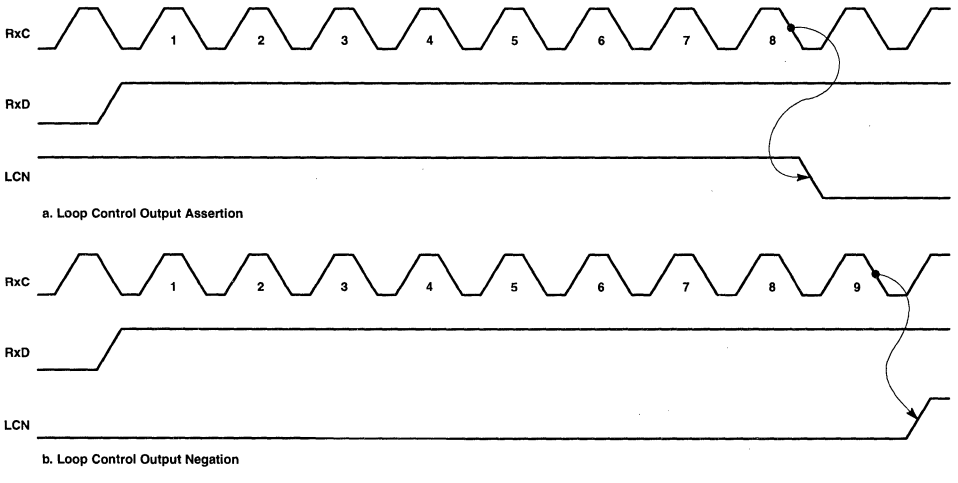
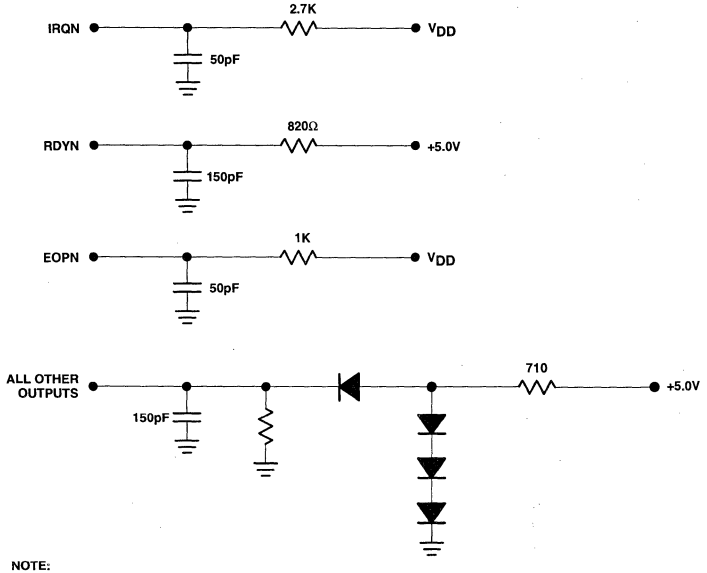


Figure 15. Relationship Between Received Data and the Loop Control Output



NOTE:
All C_L includes 50pF stray capacitance,
i.e., C_L = 150pF = 100pF discrete +50pF stray.

Figure 16. Test Conditions for Outputs

Dual universal serial communications controller (DUSCC) SCN68562

DESCRIPTION

The Philips Semiconductors SCN68562 Dual Universal Serial Communications Controller (DUSCC) is a single-chip MOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SCN68562 interfaces to the 68000 MPUs via asynchronous bus control signals and is capable of program-polled, interrupt driven, block-move or DMA data transfers. The operating mode and data format of each channel can be programmed independently.

Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides 16 common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the DUSCC well suited for dual-speed channel applications. Data rates up to 4Mbits per second are supported.

The transmitter and receiver each contain a four-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to four characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

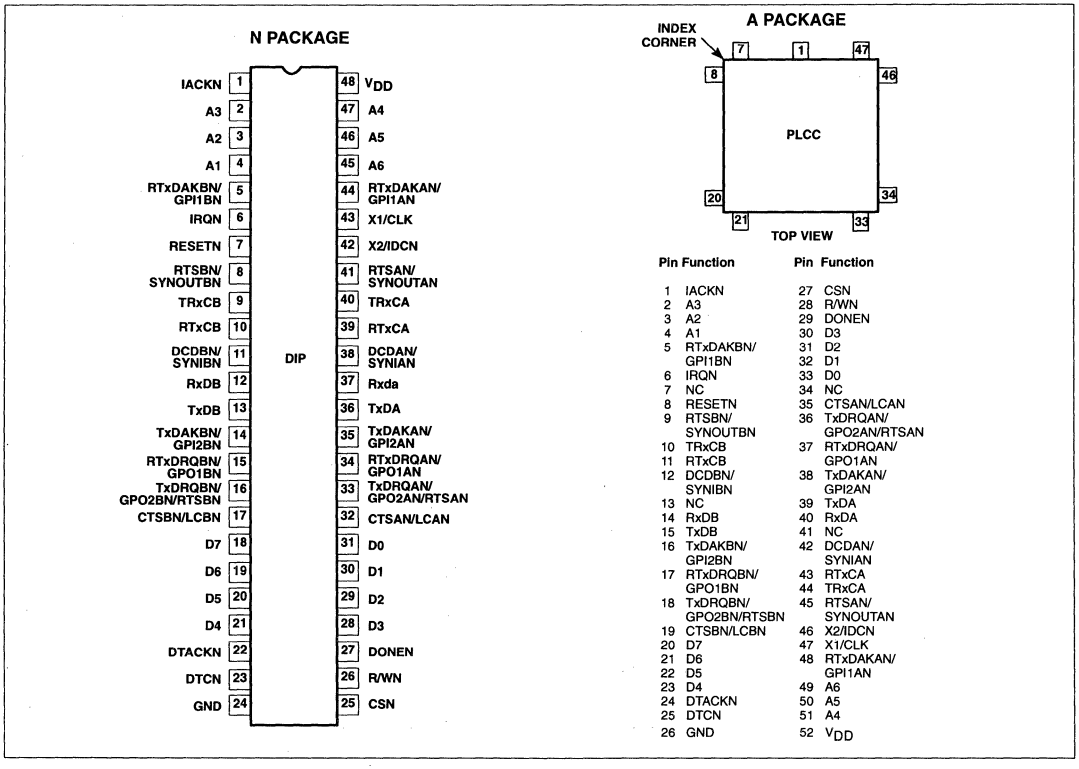
Two modem control inputs (DCD and CTS) and three modem control outputs are provided. These inputs and outputs can be optionally programmed for other functions.

FEATURES

General Features

- Dual full-duplex synchronous/asynchronous receiver and transmitter
- Multiprotocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: BISYNC, DDCMP
  - ASYNC: 5–8 bits plus optional parity
- Four character receiver and transmitter FIFOs

PIN CONFIGURATIONS



Pin	Function	Pin	Function
1	IACKN	27	CSN
2	A3	28	R/WN
3	A2	29	DONEN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
6	IRQN	32	D1
7	NC	33	D0
8	RESETN	34	NC
9	RTSBN/ SYNOUTBN	35	CTSAN/LCAN
10	TRxCB	36	TxDRQAN/ GPO2AN/RTSAN
11	RTxCB	37	RTxDRQAN/ GPO1AN
12	DCDBN/ SYNIBN	38	TxDAKAN/ GPI2AN
13	NC	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	NC
16	TxDAKBN/ GPI2BN	42	DCDAN/ SYNIAN
17	RTxDRQBN/ GPO1BN	43	RTxCA
18	TxDRQBN/ GPO2BN/RTSBN	44	TRxCA
19	CTSBN/LCBN	45	RTSAN/ SYNOUTAN
20	D7	46	X2/IDCN
21	D6	47	X1/CLK
22	D5	48	RTxDAKAN/ GPI1AN
23	D4	49	A6
24	DTACKN	50	A5
25	DTCN	51	A4
26	GND	52	V_{DD}

- 0 to 4MHz data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 16 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- and half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Compatible with the Philips Semiconductors SCB68430 Direct Memory Access Interface (DMAI) and other DMA controllers
  - Single- or dual-address dual transfers
  - Half- or full-duplex operation
  - Automatic frame termination on counter/timer terminal count or DMA DONE
- Interrupt capabilities
  - Daisy chain option
  - Vector output (fixed or modified by status)
  - Programmable internal priorities
  - Maskable interrupt conditions
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general I/O pins per channel
  - CTS and DCD programmable autoenables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X Rx and Tx clock factors
- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search 1/2-bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmits up to 4Mbs and receive up to 2Mbps data rates

Character-Oriented Protocol Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK line-fill on underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun, and underrun error detection

BISYNC Features

- EBCDIC or ASCII header, text and control messages
- SYN, DLE stripping
- EOM (end of message) detection and transmission
- Auto transparent mode switching
- Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
- Control character sequence detection for both transparent and normal text

Bit-Oriented Protocol Features

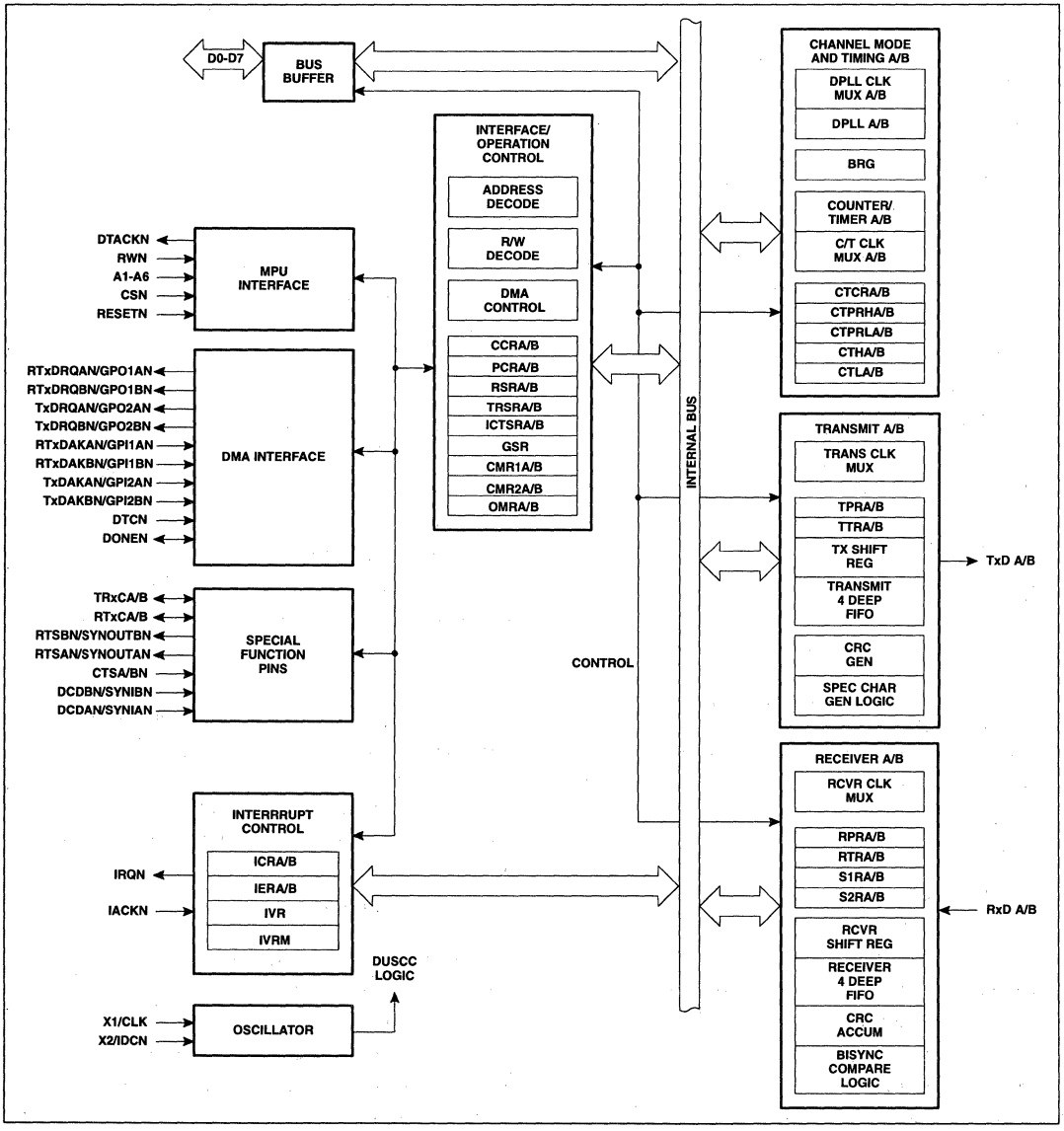
- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for 1 field
- Zero insertion and deletion
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- ABORT, ABORT-FLAGs, or FCS FLAGs line-fill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±5%, T_A = 0°C to +70°C		DWG #
	Serial Data Rate = 2.5Mbps Maximum	Serial Data Rate = 4Mbps Maximum	
48-Pin Plastic Dual In-Line Package (DIP)	SCN68562C2N48	SCN68562C4N48	0416C
52-Pin Plastic Leaded Chip Carrier (PLCC) Package	SCN68562C2A52	SCN68562C4A52	0397E

NOTE: See SCN26562/SCN68562 User's Guide for detailed description of all the features.

BLOCK DIAGRAM



PIN DESCRIPTION

In this data sheet, signals are discussed using the terms 'active' and 'inactive' or 'asserted' and 'negated' independent of whether the signal is active in the High (logic 1) or Low (logic 0) state. N at the end of a pin name signifies the signal associated with the pin is active-Low (see individual pin description for the definition of the active level of each signal.) Pins which are provided for both channels are designated by A/B after the name of the pin and the active-Low state indicator, N, if applicable. A similar method is used for registers provided for both channels: these are designated by either an underline or by A/B after the name.

MNEMONIC	DIP PIN NO.	TYPE	NAME AND FUNCTION
A1 – A6	4-2, 45-47	I	**Address Lines:** Active-High. Address inputs which specify which of the internal registers is accessed for read/write operation.
D0 – D7	31-28, 21-18	I/O	**Bidirectional Data Bus:** Active High, 3-State. Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the DUSCC take place over this bus. The data bus is enabled when CSN is Low, during interrupt acknowledge cycles and single-address DMA acknowledge cycles.
R/WN	26	I	**Read/Write:** A High input indicates a read cycle and a Low input indicates a write cycle when a cycle is initiated by assertion of the CSN input.
CSN	25	I	**Chip Select:** Active-Low input. When Low, data transfers between the CPU and the DUSCC are enabled on D0 – D7 as controlled by the R/WN and A1 – A6 inputs. When CSN is High, the DUSCC is isolated from the data bus (except during interrupt acknowledge cycles and single-address DMA transfers) and D0 – D7 are placed in the 3-State condition.
DTACKN	22	O	**Data Transfer Acknowledge:** Active-Low, 3-State. DTACKN is asserted on a write cycle to indicate that the data on the bus has been latched, and on a read cycle or interrupt acknowledge cycle to indicate valid data is on the bus. The signal is negated when completion of the cycle is indicated by negation of the CSN or IACKN input, and returns to the inactive state (3-State) a short period after it is negated. In a single address DMA mode, data is latched with the falling edge of DTCN. DTACKN is negated when completion of the cycle is indicated by the assertion of DTCN or negation of DMA acknowledge inputs (whichever occurs first), and returns to the inactive state (3-State) a short period after it is negated. When negated, DTACKN becomes an open-drain output and requires an external pull-up resistor.
IRQN	6	O	**Interrupt Request:** Active-Low, open-drain. This output is asserted upon occurrence of any enabled interrupting condition. The CPU can read the general status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the DUSCC to output an interrupt vector on the data bus.
IACKN	1	I	**Interrupt Acknowledge:** Active-Low. When IACKN is asserted, the DUSCC responds by placing the contents of the interrupt vector register (modified or unmodified by status) on the data bus and asserting DTACKN. If no active interrupt is pending, DTACKN is not asserted.
X1/CLK	43	I	**Crystal or External Clock:** When using the crystal oscillator, the crystal is connected between pins X1 and X2. If a crystal is not used, and external clock is supplied at this input. This clock is used to drive the internal bit rate generator, as an optional input to the counter/timer or DPLL, and to provide other required clocking signals.
X2/IDCN	42	O	**Crystal or Interrupt Daisy Chain:** When a crystal is used as the timing source, the crystal is connected between pins X1 and X2. This pin can be programmed to provide and interrupt daisy chain active-Low output which propagates the IACKN signal to lower priority devices, if no active interrupt is pending. This pin should be grounded when an external clock is used on X1 and X2, is not used as an interrupt daisy chain output.
RESETN	7	I	**Master Reset:** Active-Low. A low on this pin resets the transmitters and receivers and resets the registers shown in Table 1. Reset in asynchronous, i.e., no clock is required.
RxDA, RxDB	37, 12	I	**Channel A (B) Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified for the channel, the input is sampled on the rising edge of the clock.
TxDA, TxDB	36, 13	O	**Channel A (B) Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the marking (High) condition when the transmitter is disabled or when the channel is operating in local loopback mode. If external transmitter clock is specified for the channel, the data is shifted on the falling edge of the clock.
RTxCA, RTxCB	39, 10	I/O	**Channel A (B) Receiver/Transmitter Clock:** As an input, it can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, can supply the counter/timer output, the transmitter shift clock (1X), or the receiver sampling clock (1X). The maximum external receiver/transmitter clock frequency is 4MHz.

PIN DESCRIPTION (Continued)

MNEMONIC	DIP PIN NO.	TYPE	NAME AND FUNCTION
TRxCA, TRxCB	40, 9	I/O	**Channel A (B) Transmitter/Receiver Clock:** As an input, it can supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the DPLL output, the transmitter shift clock (1X), the receiver sampling clock (1X), the transmitter BRG clock (16X), The receiver BRG clock (16X), or the internal system clock (X1/2). The maximum external receiver/transmitter clock frequency is 4MHz.
CTSA/BN, LCA/BN	32, 17	I/O	**Channel A (B) Clear-To-Send Input or Loop Control Output:** Active-Low. The signal can be programmed to act as an enable for the transmitter when not in loop mode. The DUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. When operating in the COP loop mode, this pin becomes a loop control output which is asserted and negated by DUSCC commands. This output provides the means of controlling external loop interface hardware to go on-line and off-line without disturbing operation of the loop.
DCDA/BN, SYNIA/BN	38, 11	I	**Channel A (B) Data Carrier Detected or External Sync Input:** The function of this pin is programmable. As a DCD active-Low input, it acts as an enable for the receiver or can be used as a general purpose input for the DCD function, the DUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. As an active-Low external sync input, it is used in COP modes to obtain character synchronization without receipt of a SYN character. This mode can be used in disc or tape controller applications or for the optional byte timing lead in X.21.
RTxDRQA/BN, GPO1A/BN	34, 15	O	**Channel A (B) Receiver/Transmitter DMA Service Request or General Purpose Output:** Active-Low. For half-duplex DMA operation, this output indicates to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or that the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, this output indicates to the DMA controller that data is available in the receiver FIFO. In non-DMA mode, this pin is a general purpose output that can be asserted and negated under program control.
TxDRQA/BN, GPO2A/BN, RTSA/BN	33, 16	O	**Channel A (B) Transmitter DMA Service Request, General Purpose Output, or Request-to-Send:** Active-Low. For full-duplex DMA operation, this output indicates to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full-duplex DMA mode, this pin can be programmed as a general purpose or a Request-to-Send output, which can be asserted and negated under program control (see Detailed Operation).
RTxDAKA/BN, GPI1A/BN	44, 5	I	**Channel A (B) Receiver/Transmitter DMA Acknowledge or General Purpose Input:** Active-Low. For half-duplex single address DMA operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO or load transmitter FIFO) is beginning. For full-duplex single address DMA operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested read receiver FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in single address DMA mode.
TxDAKA/BN, GP12A/BN	35, 14	I	**Channel A (B) Transmitter DMA Acknowledge or General Purpose Input:** Active-Low. When the channel is programmed for full-duplex single address DMA operation, this input is asserted to indicate to the DUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in full-duplex single address DMA mode.
DTCN	23	I	**Device Transfer Complete:** Active-Low. DTCN is asserted by the DMA controller to indicate that the requested data transfer is complete.
DONEN	27	I/O	**Done:** Active-Low, open-drain. See Detailed Operation for a description of the function of this pin.
RTSA/BN, SYNOUTA/BN	41, 8	O	**Channel A (B) Sync Detect or Request-to-Send:** Active-Low. If programmed as a sync output, it is asserted one bit time after the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes) is detected by the receiver. As a Request-to-Send modem control signal, it functions as described previously for the TxDRQN/RTSN pin.
V_{DD}	48	I	+5V ± 10% power input.
GND	24	I	Signal and power ground input.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature[2]	0 to +70	°C
T_{STG}	Storage Temperature	-65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	-0.5 to +7.0	V
V_S	Voltage from any pin to ground[3]	-0.5 to V_{CC} +0.5	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 40°C/W for plastic DIP and 42°C/W for PLCC.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

DC ELECTRICAL CHARACTERISTICS[1, 4]

T_A = 0 to +70°C, V_{CC} = 5.0V ± 5%

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage:					
	All except X1/CLK				0.8	V
	X1/CLK				0.4	V
V_{IH}	Input high voltage:					
	All except X1/CLK		2.0			V
	X1/CLK		2.4		V_{CC}	V
V_{OL}	Output low voltage:					
	All except IRQN, DONEN	I_{OL} = 5.3mA			0.5	V
	IRQN, DONEN	I_{OL} = 8.8mA			0.5	V
V_{OH}	Output high voltage: (Except open drain outputs)	I_{OH} = -400µA	2.4			V
I_{ILX1}	X1/CLK input low current[3]	V_{IN} = 0, X2 = GND	-5.5		0.0	mA
I_{IHX1}	X1/CLK input high current[3]	V_{IN} = V_{CC}, X2 = GND			1.0	mA
I_{ILX2}	X2 input low current[3]	V_{IN} = 0, X1 = open	-100			µA
I_{IHX2}	X2 input high current[3]	V_{IN} = V_{CC}, X1 = open			100	µA
I_{IL}	Input low current DTCN, TxDAKA/BN, RTxDAKA/BN	V_{IN} = 0	-40			µA
I_L	Input leakage current	V_{IN} = 0 to V_{CC}	-5		5	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			5	µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0	-5			µA
I^{ODL}	Open drain output low current in off state: DONEN	V_{IN} = 0	-120		-25	µA
	IRQN, DTACKN		-5			µA
I_{ODH}	Open drain output high current in off state: DONEN, IRQN, DTACKN	V_{IN} = V_{CC}			5	µA
I_{CC}	Power supply current	V_O = 0 to V_{CC}			275	mA
C_{IN}	Input capacitance[2]	V_{CC} = GND = 0			10	pF
C_{OUT}	Output capacitance[2]	V_{CC} = GND = 0			15	pF
$C_{I/O}$	Input/output capacitance[2]	V_{CC} = GND = 0			20	pF

NOTES:
1. Parameters are valid over specified temperature and voltage range.
2. These values were not explicitly tested; they are guaranteed by design and characterization data.
3. X1/CLK and X2 are not tested with a crystal installed.
4. This specification applies to revision D, revision E and later revisions.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3, 4] T_A = -55 to +110°c, V_{CC} = 5V ± 10%

NO.	FIGURE	PARAMETER	LIMITS			UNIT
			Min	Typ	Max	
1	1	RESETN pulse width	1.2			µS
2	2,4	A1 - A6 set-up time to CSN Low	10			nS
3	2,4	A1 - A6 hold time from CSN High	0			nS
4	2,4	RWN set-up time to CSN Low	0			nS
5	2,4	RWN hold time to CSN High	0			nS
6	2,4	CSN High pulse width[4]	160			nS
7	2,5	CSN or IACKN High from DTACKN Low	30			nS
7A	5	IACKN High to DTACKN High			200	nS
8	2,5	Data valid from CSN or IACKN Low			300	nS
9	2	Data bus floating from CSN High[7]			100	nS
10	4	Data hold time from DTACKN Low[5]	0			nS
11	2,4	DTACKN Low from read data ready	0			nS
12	2,4	DTACKN Low from CSN Low			560	nS
12A	4	CSN Low to write data valid			50	nS
13	2,4	DTACKN High from CSN High			150	nS
14	2,4	DTACKN high impedance from CSN High			185	nS
15	5	DTACKN Low from IACKN Low			550	nS
16	6	GPI input set-up time to CSN Low	20			nS
17	6	GPI input hold time from CSN Low	100			nS
18	6	GPO output valid from DTACKN Low			300	nS
19	7	IRQN High from:				
		Read RxFIFO (RxRDY interrupt)			450	nS
		Write TxFIFO (TxRDY interrupt)[8]			450	nS
		Write RSR (Rx condition interrupt)[8]			400	nS
		Write TRSR (Rx/Tx interrupt)[8]			400	nS
		Write ICTSR (port change and CT int.)[8]			400	nS
20	8	X1/CLK High or Low time	25			nS
		X1/CLK frequency	2.0	14.745	16	MHz
		CTCLK High or Low time	100	6		nS
		CTCLK frequency	0		4	MHz
		RxC High or Low time	110			nS
		RxC frequency (16X or 1X)[9]	0		4	MHz
		TxC High or Low time	110			nS
		TxC frequency (16X or 1X)	0		4	MHz
21	9	TxD output from TxC input Low (1X)			240	nS
		(16X)			435	nS
22	9	TxD output from TxC output Low			50	nS
23	10	RxD data set-up time to RxC High	50			nS
24	10	RxD data hold time from RxC High	50			nS
25	11	IACKN Low to daisy chain Low			200	nS
26	13	Data valid from receive DMA ACKN			300	nS
27	12,13	DTCN width	100			nS
28	12,13	RDYN Low to DTCN Low	80			nS
29	13	Data bus float from DTCN Low[7]			200	nS
30	12,13	DMA ACKN Low to RDYN (DTACKN) Low			360	nS
31	12,13	RDYN High from DTCN Low			230	nS
32	12,13	RDYN High impedance from DTCN Low			250	nS
33	13	Receive DMA REQN High from DMA ACKN Low			325	nS
34	13	Receive DMA ACKN width	150			nS
35	12,13	Receive DMA ACKN Low to DONEN Low			250	nS
36	12	Data set-up to DTCN Low	50			nS
37	12	Data hold from DTCN Low[6]	50			nS
38	12	Transmit DMA REQN High from ACKN Low			340	nS
39	12	Transmit DMA ACKN width	150			nS
40	12	Transmit DMA ACKN Low to DONEN Low output			250	nS
40A	12	DTCN Low DONEN output High			260	nS
41	14	CSN Low to transmit DONEN Low output			300	nS
42	14	CSN Low to transmit DMA REQ negated			400	nS
43	14	CSN Low to receive DONEN Low			300	nS
44	14	CSN Low to receive DMA REQ negated			400	nS

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For DC and functional testing, all inputs except X1/CLK swing between 0.8V and 2.0V with a transition time of 20ns maximum. For X1/CLK, this swing is between 0.4V and 2.4V All time measurements are referenced at input voltages of 0.4V and 2.4V for all inputs. Output levels are referenced at 1.2V and 2.0V, as appropriate.
3. Test conditions for outputs: C_L = 150pF, except open-drain outputs. Test condition for open-drain outputs: C_L = 50pF to GND, R_L = 2.7kΩ to V_{CC} except DTACKN whose R_L = 820Ω to V_{CC} and C_L = 150pF to GND and DONEN which requires C_L = 50pF to GND and R_L = 1kΩ to V_{CC}.
4. This specification will impose maximum 68000 CPU CLK to 6MHz. Higher CPU CLK can be used if repeating bus cycles are not performed.
5. Execution of the valid command (after it is latched) requires three falling edges of X1 (see Figure 14).
6. In single address DMA mode write operation, data is latched by the falling edge of DTCN.
7. These values were not explicitly tested, they are guaranteed by design and characterization data.
8. These timings are from the falling edge of DTACKN (not CSN rising).
9. X1/CLK frequency must be at least four times the receiver serial data rate.

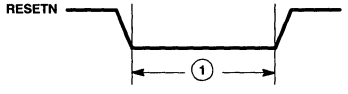


Figure 1. Reset Timing

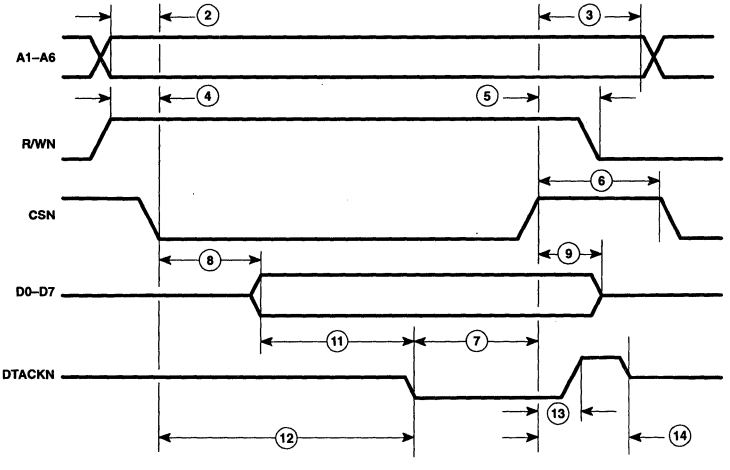


Figure 2. Bus Timing (Read Cycle)

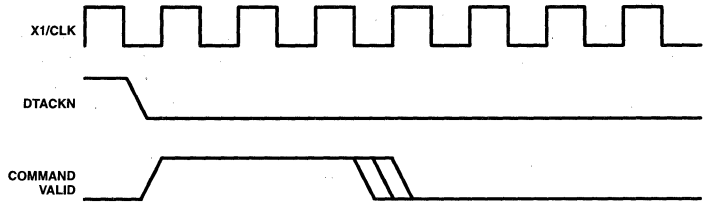


Figure 3. Command Timing

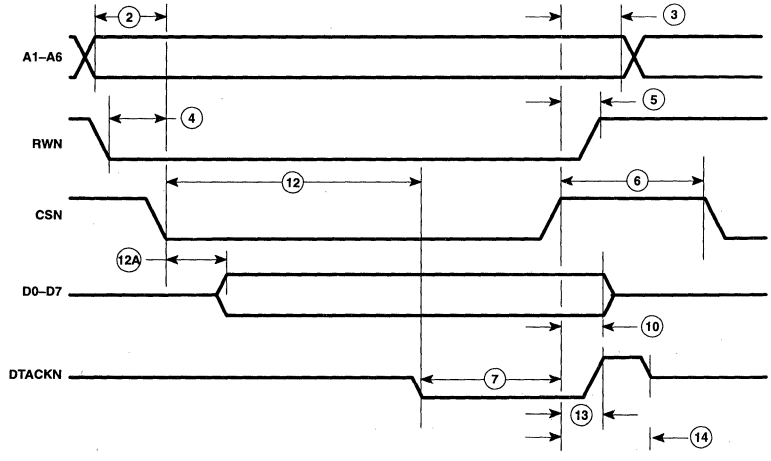


Figure 4. Bus Timing (Write Cycle)

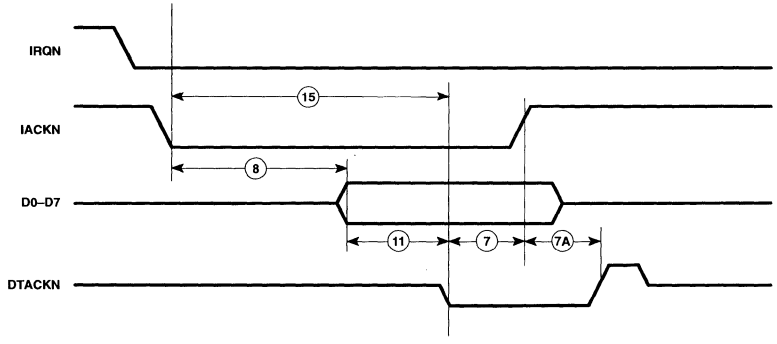


Figure 5. Interrupt Cycle Timing

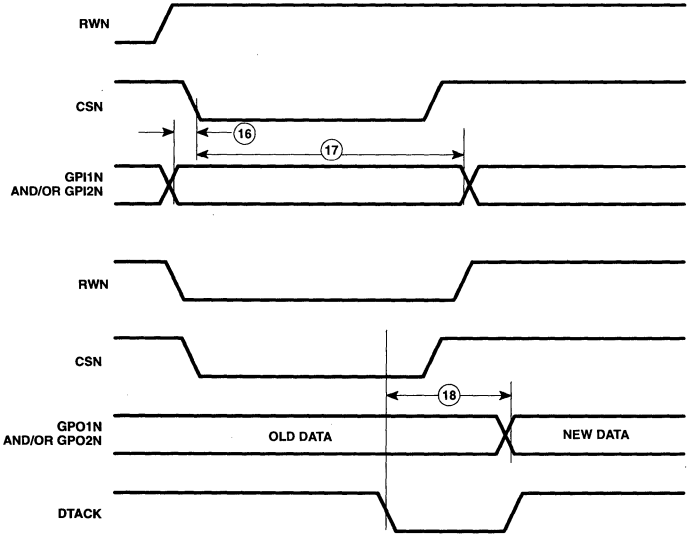


Figure 6. Port Timing

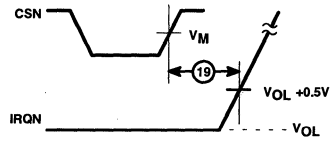


Figure 7. Interrupt Timing

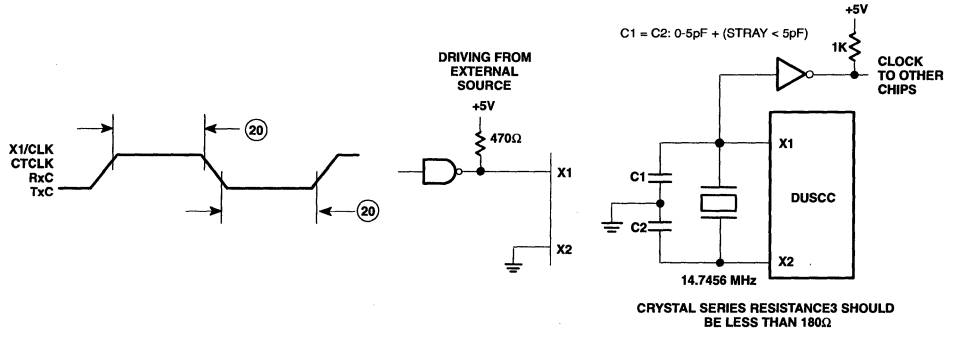


Figure 8. Clock Timing

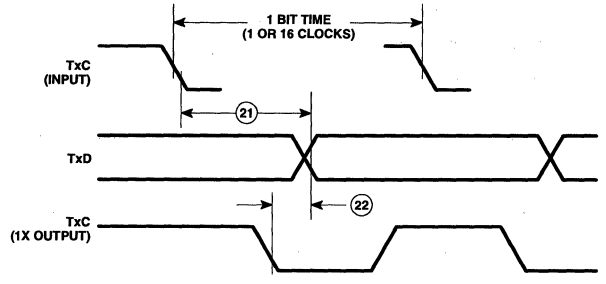


Figure 9. Transmit Timing

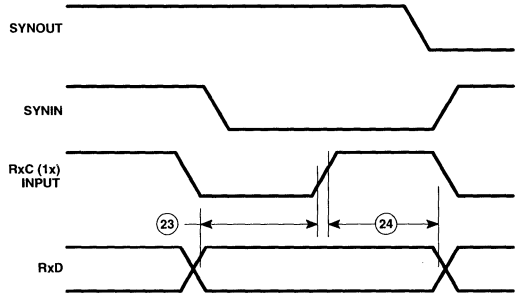


Figure 10. Receive Timing

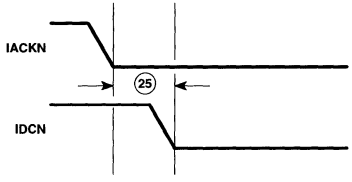


Figure 11. Interrupt Daisy Chain Timing

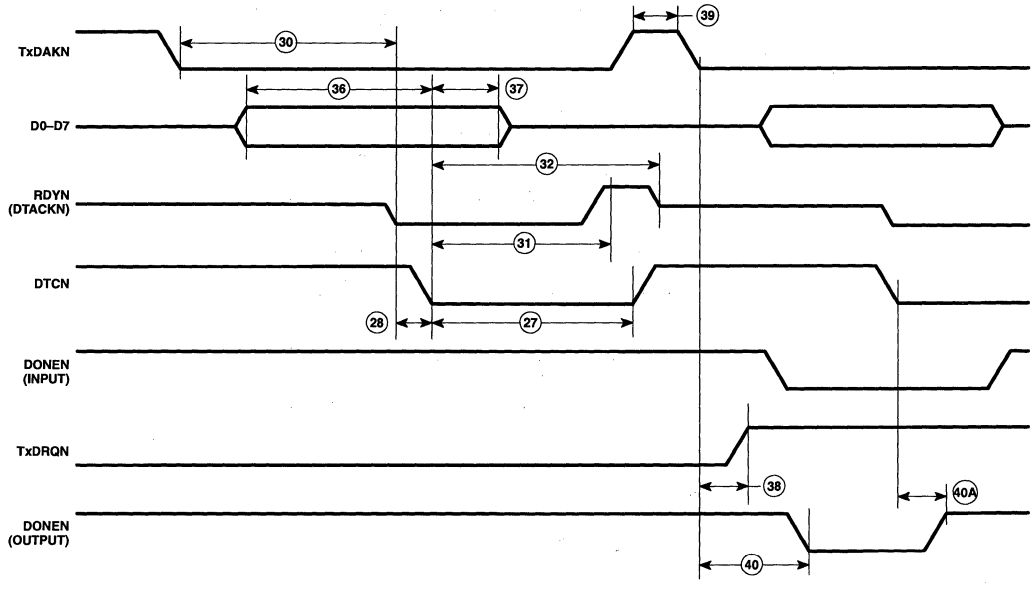


Figure 12. DMA Transmit Write Timing — Single Address DMA Mode

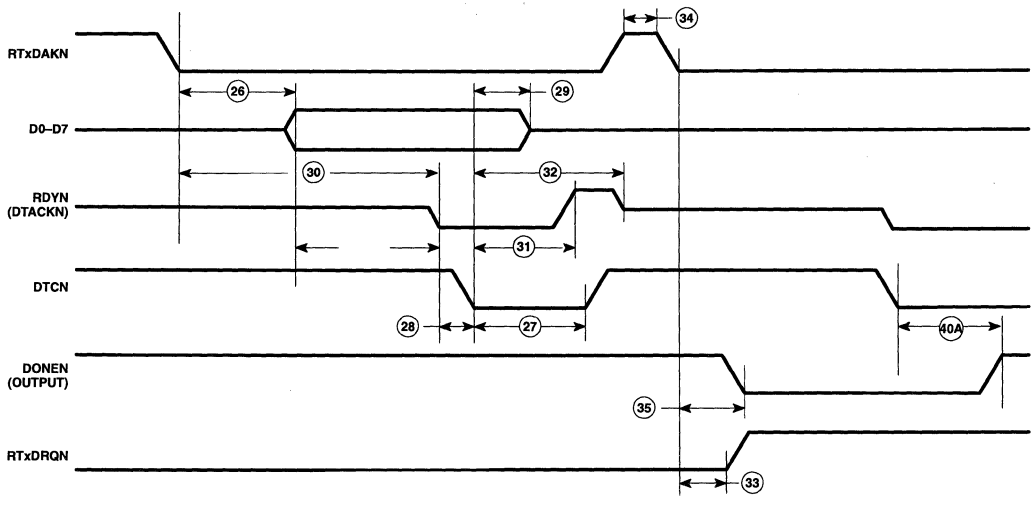


Figure 13. DMA Receive Read Timing — Single Address DMA Mode

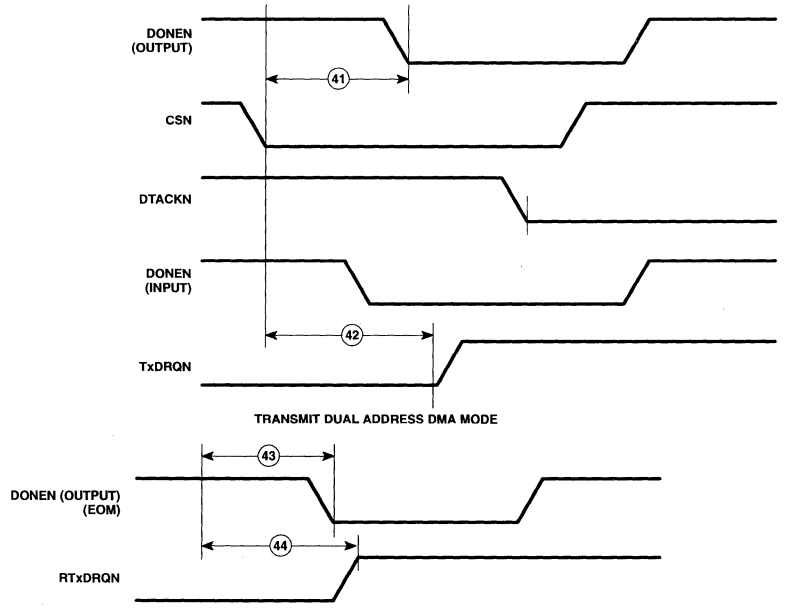


Figure 14. Dual Address DMA Mode Timing

Using the datacomm product's on-chip oscillator — AN413

Author: D. Ibarra

DESCRIPTION

This application note discusses how to use the on-chip oscillator circuitry for the Philips Semiconductors UART and DUSCC/DMSC families of data communications devices; the SCC2691, SCC2692, SCN68681, SCN26562, SCN68562, SCN26542 and SCN68542.

THE CRYSTAL OSCILLATOR

The on-chip oscillator circuitry consists of an inverting amplifier and a feedback resistor which are used to implement a Pierce oscillator (see Figure 1). The addition of an external crystal and external capacitance into the feedback loop provides the positive reactance necessary for oscillation and controls the frequency of oscillation. The oscillator operates at the frequency for which the crystal is anti-resonant (parallel resonant) with the load capacitance across the crystal. The load capacitance is given by:

$C_L = ((C1 \times C2) / (C1 + C2)) + Stray$

The only difference between "parallel" and "series" crystals is how they were calibrated. Crystals are calibrated to achieve their specified frequency either at parallel resonance with a particular load capacitance, or at series resonance (with no load capacitance). Crystals which were calibrated at their series resonant frequency will still operate at parallel resonance in this oscillator, however the resulting frequency will be slightly higher than the frequency specified for the crystal.

In general, the oscillator frequency can be adjusted slightly by trimming the external capacitors, larger capacitors will lower the oscillator's frequency while smaller ones will raise it. The small errors in frequency, due to using a crystal calibrated at a different load capacitance than is present in the circuit, are negligible for typical applications. Reliability is much more important.

SCC2691, SCC2692, SCC68692 AND SCC2698 OSCILLATOR RECOMMENDATIONS

For these parts, the X1/CLK pin is connected to the input of the inverter and the X2 pin is connected to the output. For best results, a parallel calibrated crystal should be adjusted until the total circuit capacitance matches the capacitance specified for the crystal.

Typical crystal parameters:
Frequency – 2–4MHz
Mode of operation – Parallel resonant, fundamental mode
Load Capacitance (C_L) – 12–32pF

For operation at nominal frequency, the values recommended below will give accurate, reliable results. The frequency will vary slightly depending on the amount of stray capacitance in the individual circuit, but will typically be off no more than 0.01%.

C1 = C2 = 24pF
Y1 = Saronix NYP037-20; 3.6864MHz at C_L = 20pF with R_S = 160Ω

SCC26562, SCC68562, SCN26542 AND SCN68542 OSCILLATOR RECOMMENDATIONS

For these parts, the X1/CLK pin is connected to the output of the inverter, the X2 pin is connected to the input, and the inverter is a Schmitt trigger. For best results, a parallel calibrated crystal should be obtained and the external capacitors should be adjusted until the total circuit capacitance matches the capacitance specified for the crystal.

Typical crystal parameters:
Frequency – 2–16MHz
Mode of operation – Parallel resonant, fundamental mode
Load Capacitance (C_L) – 12–32pF

For operation at nominal frequency, the values recommended below will give accurate, reliable results. The frequency will vary slightly depending on the amount of stray capacitance in the individual circuit, but will typically be off no more than 0.01%.

C1 = C2 = 24pF
Y1 = Saronix NYP147-20; 14.7456MHz at C_L = 20pF with R_S = 25Ω

SCN2681 AND SCN68681 OSCILLATOR RECOMMENDATIONS

For these parts, the X1/CLK pin is connected to the output of the inverter, the X2 pin is connected to the input, and the inverter is a Schmitt trigger. Because of the Schmitt trigger inverter, the SCN2681 and SCN68681 are limited to using small value external capacitors. If capacitors of 15pF or greater are used, intermittent power-on problems may be experienced. The oscillator may stay in relaxation mode, oscillating at a frequency much lower than the one the crystal is specified for. For this reason, we recommend using external capacitors of around 5pF, and board supplied stray capacitance of no more than 5pF. It has also been found that adding an external resistor of 100k–1MΩ across X1 and X2 will solve other start up problems for some designs. While we recommend using balanced capacitors (C1 = C2) of 5pF, unbalanced values may be used. Since the X2 pin (input to the inverter) has the most sensitivity to capacitance, many designs use a larger value capacitor (10–15pF) on the X1 pin while leaving 5pF on the X2 pin.

Typical crystal parameters:
Frequency – 2–4MHz
Mode of operation – Parallel resonant, fundamental mode
Load Capacitance (C_L) – 12–32pF

For operation at nominal frequency, the values recommended below will give accurate, reliable results. The frequency will vary slightly depending on the amount of stray capacitance in the individual circuit.

C1 = C2 = 5pF
Y1 = Saronix NYP037-20; 3.6864MHz at C_L = 20pF with R_S = 25Ω, or series calibrated with R_S = 160Ω

USING AN EXTERNAL CLOCK SOURCE

Some designs may have an external clock source available and don't need to use the on-chip oscillator. In this case, the external clock should be applied to the X1/CLK pin for all of the UART and DUSCC/DMSC parts. The X2 pin can be driven with the complement of the signal going to the X1/CLK pin for all parts. If the X2 pin is not driven, it must be left open for the SCC2691 and SCC2698. The SCN2681, SCN68681, SCN26562, SCN68562, SCN26542 and SCN68542 should have the X2 pin grounded when it is not being drive. If the X2 pin is left open, the X1/CLK pin will draw a large amount of input current (see data sheets). The X2 pin on the SCC2692 and SCC68682 can be either grounded or left open when it is not being driven.

See Figures 2 through 5 for oscillator schematics.

Using the datacomm product's on-chip oscillator AN413

REFERENCES FOR FURTHER READING

Parzen, Benjamin, Design of Crystal and Other Harmonic Oscillators, John Wiley and Sons, New York, 1983.

Frerking, Marvin E., Crystal Oscillator Design and Temperature Compensation, Van Nostrand Reinhold Co. Inc., New York, 1978.

Holmbeck, John D., "Frequency Tolerance Limitations with Loagic Gate Oscillators", Proc. 31st Annual Symposium on Frequency Control, U.S. Army Electronics Command, Fort Monmouth, N.J., pp. 390–395, 1977. Copies available from Electronic Industries Association, 2001 Eye St., NW, Washington, D.C. 20006.

THEORETICAL INFORMATION ON DUSCC/DMSC CRYSTAL OSCILLATOR (Oct. 1987)

The information contained in Table 1 is based on computer simulations over the expected process range. It is not based on characterization data or actual device testing.

Table 1. Theoretical Information on DUSCC/DMSC Crystal Oscillators

Parameter	Min	Typ	Max	Units
Feedback resistor[2]	121	160	210	kΩ
X1/ground capacitance	1.0	1.7	3.0	pF
X2/ground capacitance	3.0	4.3	6.0	pF
X1/X2 capacitance	0.5	1.0	2.0	pF
Inverter AC gain (14.7456MHz)[3]		2.8		
Inverter phase shift (14.7456MHz)[3]		249		deg.
Inverter AC gain (16MHz)[3]		2.6		
Inverter phase shift (16MHz)[3]		253		deg.
Inverter AC gain (2MHz)[3]		9.7		
Inverter phase shift (2MHz)[3]		210		deg.
X1/X2 bias level	1.8	2.3	2.9	V
Inverter prop delay[1]	6	11	18	ns

NOTES:
1. 10pF load on output X1. Delay from X2 = 3V to X1 = 3V.
2. Based on I–V characteristics of depletion transistor.
3. V_{OUT} / V_{IN} at bias point. X1 10pF loading.

DUSCC initialization procedures AN419

Author: Debra Ibarra Revised by: A. Kazmi

INTRODUCTION

The Philips Semiconductors Dual Universal Serial Communications Controller (DUSCC) has forty-eight programmable registers many of which have triple functions that vary with the protocol selected. This application note contains basic initialization instructions and examples including: description of the input clock circuit; how to use interrupts with status; how to use the digital phase locked loop (DPLL); how to initialize the counter/timer as a system down counter and as a receive character counter. Also included are software examples for the asynchronous local loop back mode, for two synchronous modes (HDLC and BISYNC), and DMA handling.

X2/IDCN PIN

Initially, the X2/IDCN pin is internally programmed as an input pin (used with a crystal) by the assertion of RESET. If an external clock is used as the timing source in place of a crystal, it is necessary to perform the following:

1. If the X2/IDCN is used as an IDCN output, write PCRA[7] = 1 as soon as possible. This allows the IDCN to be used as a daisy chain without delay.
2. If X2/IDCN is not used as the IDCN output, the X2/IDCN pin must be grounded, and leave PCRA[7] = 0.

X1/CLK SOURCES

The DUSCC must have a clock source connected to the X1 input at all times. It can be supplied by a crystal between the X1 and X2 pin, or by driving an external clock Into the X1/CLK input. The frequency must be between 2.0 and 16.0MHz for correct device operation; 14.7456MHz is the nominal frequency which is used to obtain the standard baud rates listed for the internal baud rate generator.

X1/X2 Crystal

The DUSCC oscillator circuitry consists of an inverting amplifier and a feedback resistor which are used to implement a Pierce oscillator. This circuitry will cause the crystal attached between the X1 and X2 pins to go into anti-resonant (parallel) operation. So, while a number of crystal and capacitor combinations will work, obtaining a parallel calibrated crystal and adjusting the external capacitor values until the total circuit capacitance matches the capacitance specified for the crystal will result in the most accurate frequency value. Using two 24pF capacitors, one from X1 to ground and one from X2 to ground, and the parallel crystal recommended below will give accurate, reliable results. The frequency will vary slightly depending on the amount of stray capacitance in the individual circuit, but will typically be off no more than 0.01%. The frequency can be adjusted by trimming the external capacitors; larger capacitors lower the oscillator's frequency and smaller ones raise it.

A source for the 14.7456MHz crystal is: Saronix, Palo Alto, CA. Request part number NYP147-20.

Externally Driven Clock

The most important point in using an external source to drive the X1/CLK input is to meet the V_{IH} specification and the minimum high and low times of 25ns. Also, when driving a clock into X1, be sure to ground the X2 pin if it is not programmed to be IDCN out.

INTERRUPT STATUS

The DUSCC is equipped with an interrupt vector register (IVR) that can be modified. On power up, the IVR is initialized to a fixed value. If ICR[2] = 1, the status registers will modify the interrupt vector. If the vector is modified, ICR[3] must be programmed to modify either vector bits [2:0] or [4:2]. ICR[7:6] dictates which channel will have the highest priority or whether interrupt priorities are interleaved between channel A and channel B.

If a modified vector is used, the three modified bits in the vector will reflect the interrupting condition. For example, if channel B transmitter is ready, the modified bits = 101. Interrupts can be programmed to occur from either the RSR, the TRSR, the ICTSR registers, or the TXRDY and RXRDY conditions. These registers allow either transmit, receive, input, or C/T status bits to set the appropriate GSR bit and force an interrupt.

EXAMPLES – Option: Channel A in Synchronous Mode

Assume channel A is in the COP mode with the receiver sampling off the DPLL output which is programmed to use FM0 encoding. The user chooses to monitor the following items: EOM detect RSRA[7], CRC errors RSRA[1:0], and check for DPLL errors TRSRA[3].

Because an underrun of the transmitter, or an overrun of the receiver can be a problem, program OMRA[4:3]=00. Writing IERA = 79H, will enable all of the above conditions to interrupt as soon as ICR[1] is set, and the transmitter and receiver are enabled. The status of these bits is reflected in GSR[3:0].

Option: Channel B in Asynchronous Mode

Assume channel B is initialized to check for framing and parity errors (RSRB[1:0]) and the counter/timer is to be used as a system down counter. For the user to know when the C/T reaches zero count (ICTSRB[6]), set CTCRB[7] so that the C/T can generate an interrupt. RXRDY can be set to activate when the FIFO fills (OMRB[3] = 1). However, the receiver could be overrun if the baud rate is high or the CPU is latent in reading the receive FIFO. Writing IERB= 51H, will enable all of the above conditions when ICR[0] is set, and the transmitter and receiver are enabled. The status of these bits is reflected in GSR[7:4]

NOTE: Because the synchronous channel has more of a tendency to underrun, channel A has interleaved priority. This means that channel A takes priority when events of equal weight occur in both channels simultaneously; therefore, ICR = 87H.

The interrupts are activated when the transmitter and receiver are enabled. Although some of these interrupts reset themselves when the interrupt routine services the DUSCC, it is safer to reset the status bits that caused the interrupt by writing 1 to each status bit that is set. Resetting the bits in the RSR, TRSR, and ICTSR registers, automatically resets the corresponding bits in the general status register (GSR). If TXRDY or RXRDY causes the interrupt, these can be cleared by writing/reading data to/from Tx/RxFIFOs.

COUNTER/TIMER

Each channel of the DUSCC contains a counter/timer that can be used as either a down counter, a delay timer, an external event counter, a TX or RX character counter, a bit length measurement tool, or a timer to generate almost any baud rate. The C/T can be clocked from a number of sources.

Table 1 gives the maximum frequency generated by the C/T with various inputs (prescaler = 1).

The C/T must be loaded with a minimum count of N = 2 which will divide the maximum timer output frequency to one-half if the pulsed mode is programmed, or to one-fourth if the square mode is

Table 1. Maximum Frequency Generated by C/T

Clk Source	Maximum Outputs			Notes
	Pulsed	Square		
RTXC or TRXC	2	1	MHz	TRXC/RTXC = 4MHz
X1/CLK divide by 4	2	1	MHz	X1/CLK = 16MHz
RXBRG or TXBRG (16X)	307.2	153.6	kHz	RX/TX = 38.4K

Table 2. Encoding Schemes

Encoding	Where Sampled	How Decoded
NRZ	Center of bit time	Low = 0, high = 1
NRZI	Center of bit time	Transition since cell = 0, no transition from last cell = 1
FM0	1st and 3rd 1/4 of bit time	Cell halves dissimilar = 0, cell halves same = 1
FM1	1st and 3rd 1/4 of bit time	Cell halves same = 0, cell halves dissimilar = 1
Manchester	Center of bit time	Low to high transition = 0, high to low transition = 1

selected. (Pulsed mode forces the output low for N = 1 periods and then high for one period; square mode forces the output low for N periods and high for N periods.) The C/T is controlled by five registers. CTPRH and CTPRL hold the preset counter value that will be loaded when a start counter command is issued. CTH and CTL hold the current value contained in the C/T and can be read at any time. For best results, stop the C/T prior to reading the CTH and CTL. The CTCR register controls the C/T clock source, prescaler, type of output (pulse or square wave) and the direction taken when the C/T counts down and passes zero detect.

Counter/Timer Used as a Down Counter

The following procedures initialize the C/T as a system down counter, set to interrupt the CPU every 2ms:

1. Using (X1/CLK)/4, the typical X1 rate is 14.7456MHz (t = 67.82ns)
2. Divide the X1 rate by 4 ⇒ 3.6864MHz (t = 271.27ns).
3. The following equation determines the preset count:

$$\text{Count value} = \frac{\text{source freq}}{\text{desired freq} \times 2}$$

(for square wave output)

$$\text{Count value} = \frac{\text{source freq}}{\text{desired freq} \times 2}$$

(for on shot pulse output)

$$\text{Count value} = \frac{3.6864 \times 10^6}{(\frac{1}{4} \times 10^{-3}) \times 2}$$

$$= 7372.8 \text{ (dec)}$$

$$= \text{ICCD (hex)}$$

1. Write CTCR = 82H (prescale = 1, X1/4, enable INT (CTCR161 = 0, preset loaded on zero)
2. Write CTPRH = 1CH (preset high value)
3. Write CTPRL = CDH (preset low value)
4. Write ICR = 01 or 02 (enable master interrupt (A or B))
5. Write CCR = 83H (transfer preset value)
6. Write CCR = 80H (issue start C/T command)

After the interrupt occurs:

7. Write ICTSR = 40H (reset C/T status)
8. Wait for next interrupt, preset value automatically reloaded.

Counter/Timer Used as a Character Counter

Assume that characters are being received in the asynchronous mode and the user chooses to accumulate these characters in RAM in blocks of 2048 bytes each. The preset value will be 2048 or 800H. Each time the count reaches zero, the counter/timer interrupts the CPU. The only difference between the C/T as a down counter, and the C/T as a character counter, is that CTCR = 06 which assigns the C/T clock source to be the receive character pulse. The CTPR is loaded with the block count of 800H. Because this particular example is repetitive, the user resets the C/T interrupt (ICTSR = 40H) after each block count has been reached. Since CTCR16] = 0, the preset value will automatically reload on zero detect.

DIGITAL PHASE LOCKED LOOP (DPLL)

The DPLL is designed to be used with the transmission of synchronous data without using a separate transmit clock line. Data is sampled by a 32X clock searching for a transition on data entering the receiver. Once the enter search mode command is issued, the DPLL will start to synchronize on the first data transition. The user must ensure that RXD has no spurious noise which could cause the DPLL to begin to synchronize on the wrong starting edge. Since sampling takes place in parts of the bit cell, the FM mode has the greatest potential for this error.

If noise should trigger the DPLL, it will set TRSR[3]=1, and the DPLL will enter into a search mode automatically.

Table 2 describes five different encoding schemes and where in the bit cell the DPLL will sample data entering the receiver. For reference, see DPLL Waveforms in the DUSCC data sheet.

The DPLL maximum clock frequency is 250KHz. This value can be achieved by using the X1/CLK at 16MHz (divide by 64). A slower speed of 125KHz can be derived by using an external TXC or RXC (TXC or RXC set at 4MHz divided by 32). For complete details of how the DPLL samples a data stream and corrects its clocking edges, refer to the DUSCC data sheet on NRZI and FM mode operation.

An example of how to initialize the receiver sampling data with the DPLL using a 38.4KHz rate in the NRZI mode (BRG clock source) follows.

1. Write RTR = 6FH; (DPLL (BRG), BRG = 38.4K)
2. Write CCR = C3H; (Set DPLL mode = NRZI)
3. Write CCR = 40H; (Reset receiver)
4. Write CCR = C0H; (DPLL enter search mode)

DUSCC initialization procedures AN419

ASYNCHRONOUS MODE

Regardless of the channel connection used in CMR2[7:6], the basic initialization in asynchronous mode is the same. Note that whenever a change is made in the channel mode registers, the transmitter and receiver should first be disabled. Also, before any change is made in the transmit parameter register (TPR) or the transmit timing register (TTR), the transmitter should be disabled.

After a change(s) has been completed, the transmitter should be reset; then enabled.

If changes are made in either the receive parameter register (RPR) or the receive timing register (RTR), the receiver should be disabled. After a change(s) has been completed, the receiver should be reset; then enabled.

The software illustration (Figure 1) demonstrates the minimum number of registers needed to program the DUSCC for asynchronous transmission. This routine is also an example of how the integrity of the system can be checked in local loop back by writing, reading, and verifying 256 characters through each channel. Since the comments in the software examples are extensive, there are no flow charts provided in this application note. If a reset pulse greater than 1.2μs is asserted on the reset input after V_{DD} has stabilized, most registers will be reset to zero. Many of these registers can be disregarded during initialization. The registers that must be programmed are the channel mode registers (CMR1/2), channel command registers (CCR), and the parameter and timing registers (TPR, TTR, RPR, RTR) for both the transmitter and receiver.

SYNCHRONOUS PROTOCOLS

The SCN68562 will work with almost any synchronous protocol at rates exceeding maximum speeds recommended by CCITT standards (USA = 1.5MHz; Europe = 2.04MHz). While asynchronous transmission frames are sent on a character by character basis (including, start, stop, and parity bits), synchronous transmission requires a protocol that works with a predefined frame. Within each transmission frame there exists four main parts:

1. Synchronizing characters
2. A header defining addresses and/or control information
3. The physical data stream
4. 4. Block character check (BCC)

Most synchronous transmissions fall into two main categories, bit-oriented protocols (BOP) and character-oriented protocols (COP). This document describes the two most widely used protocols, an HDLC sample for BOP, and a BISYNC sample for COP.

The SCN68562 handles many of the operations necessary to send and receive a BOP or COP frame. CMR1[2:0] allows the user to select either BOP or COP with options. The synchronous/secondary address registers (S1R, S2R) are used to initialize synchronizing characters (COP) or the frame address (BOP). TPR[7:4] defines underrun control, fill pattern during an idle transmit state, and when TEOM is to be transmitted. RPR[7:3] defines which SYN patterns should be stripped, should the frame check sequence be sent to the RXFIFO, and what action the receiver should take after EOM is received or an overrun occurs. These bits also inform the receiver when external synchronous pulses will be used to synchronize received data, and if parity is to be stripped before assembly.

BOP TRANSMISSION

The software example in Figure 2 demonstrates how the user can initialize the SCN68562 for transmitting with the HDLC protocol using the BOP mode. In this example the channel is set up as a secondary station (CMR1 = 01) using an eight-bit address mode without extended control. This means that an eight-bit address must follow the opening flags of each frame. The address identifies the receiver which is to be the data destination. If this channel was programmed to be a primary (master) station, no address comparison would be necessary. For simplification, CMR2 is set up so that no FCS character is issued when the end of message command is executed. The transmitter parameter register is set to issue ABORT (FF) followed by FLAGs (7E) if the transmitter is underrun. Also, the idle state of TXD is defined as FLAGs (7E) between frames. The receive parameter register is programmed with the overrun mode set to hunt. This will force the receiver to terminate the frame when the RXFIFO and RX shift register are full, and then hunt for flags. Finally, S1R is loaded with the receiver compare address.

The start of message (SOM or TSOM) command must be issued to send out the opening synchronous flags. This is followed by the receiver address and data loaded into the TXFIFO. The frame is ended when the CPU sends an EOM or TSOM command to the command register. This must be done just before the last character is loaded into the TXFIFO. The EOM command is then appended to the next character written into the TXFIFO. After this character is shifted out, the DUSCC will issue the FCS (if programmed to do so) followed by a closing flag.

Note also that the receiver cannot use the BRG directly, unless the asynchronous mode is programmed. Therefore, (RTRA = 6F), the DPLL (at 32X), is selected. In this case the transmitter will not know what encoding scheme to use until the set NRZI command (CCRA = C3) is sent to initialize the DPLL. Immediately before reception starts, the DPLL is turned on with an enter search mode command (CCRA = C0). Since TXD is tied to RXD in this example, the receiver will look for the first byte, after the opening flag, to be an address. The address is compared to the value in S1R, and if a match occurs, the address and all other data are loaded into the RXFIFO.

COP TRANSMISSION

An example using the COP mode follows (see Figure [3]). This example is set up almost identical to BOP. The key character-oriented protocol differences are the synchronize and control characters. Before transmission begins, SYN1 and SYN2 characters are loaded into S1R and S2R. These characters are issued with the TSOM command to open the COP frame. If an underrun occurs in the transmitter, or a frame ends, TXD is filled with SYNC1/SYNC2 characters (TPRA = E3). None of the synchronized characters are transferred to the receive holding register if SYN stripping is invoked (RPRA = 83).

The remaining differences occur with special control characters that define the beginning and ending of text, the header field, and various acknowledgements. A few of these commands can be issued through the command register, but the majority must be part of the data stream.

DUSCC initialization procedures AN419

DUSCC WITH DMA CONTROLS

See Figures 4 and 5 for software examples. The schematic (Figure 6) defines the typical handshake lines necessary for the DUSCC to interface with the SCB68430, Direct Memory Access Interface (DMAI). The DUSCC will interface directly with any of the 68K family of DMA controllers (68430, 68440, 68450).

The DUSCC is shown in the half duplex single address configuration. The request pin (RTXDRQAN) initializes the DMA cycle for both the transmitter and the receiver in this mode. Once the controller has finished arbitration for the bus, acknowledgment is given to the DUSCC on the RTXDAKA input. After acknowledgment is made, RDYN is driven low by the DTACKN output. DTACKN from the DUSCC must be isolated from system DTACKN when the DMA controller has control of the bus. After each character is transferred to the transmitter, or when data is read from the receiver, DTCN is asserted. When transfer count has been reached, DONEN is asserted, ending the DMA.

DMA SOFTWARE

Two simple software programs are provided. Both are initialized with channel A in half duplex single address mode and channel B in normal polled mode. The comments in each sample explain the basic initialization.

The first software sample (Figure 4) is a transmit DMA. TXDA is tied to RXDB by a wire. The CPU loads the RAM with 256 characters and then initializes the the DMA controller. As the transmitter becomes ready and asserts IRQN, the DMA controller will acknowledge by loading the TxFIFO. After instructing the DMAI to start, the CPU reads the GSR looking for the receiver to become ready. Once RXRDY = 1, the character is read and compared against the expected character that was transmitted. The DMA transfer rate in burst mode is faster than the time needed for the 8MHz 68000 to test for and read the received characters. Therefore, flow control is used via RTS and CTS. In this case, the RxB controls RTS/CTS which controls TxA.

The second software example (Figure 5) is a receive DMA. RXDA is tied to TXDB with a wire. This example is the reverse of the previous software routine. The CPU loads 256 characters into the TXB FIFO as it becomes ready. The DMA controller reads RXA FIFO and stores the received data in RAM. When the count is complete, the CPU reads the RAM and verifies whether the data transferred is correct. No flow control is needed since the DMA controller can read the received characters faster than the RXA FIFO can fill up.

DUSCC initialization procedures AN419

NOTE: Please note that the following examples are used for illustration purposes only. User must verify their software in an actual system use.

Basic asynchronous initialization for DUSCC (local loopback mode). This routine will send 256 characters to both channel A and B. The looped back characters are read and verified by the CPU.

```
            Begin
            ;
            ; SETUP    MOVE.B  #07,      CMR1A     ;NO PARITY, ASYN MODE
                       MOVE.B  #07,      CMR1B
                       MOVE.B  #$B8,     CMR2A     ;LOCAL LOOPBACK, POLLED/INT
                       MOVE.B  #$B8,     CMR2B
                       MOVE.B  #$73,     TPRA      ;1 STOP BIT, 8 BIT CHAR
                       MOVE.B  #$73,     TPRB
                       MOVE.B  #$3E,     TTRA      ;TX=BRG CLK, 19.2K BAUD
                       MOVE.B  #$3E,     TTRB
                       MOVE.B  #03,      RPRA      ;8 BIT RX CHAR
                       MOVE.B  #03,      RPRB
                       MOVE.B  #$2E,     RTRA,     ;RX=BRG CLK, 19.2K BAUD
                       MOVE.B  #$2E,     RTRB
                       MOVE.B  #0,       CCRA      ;RESET TX
                       MOVE.B  #0,       CCRB
                       MOVE.B  #$40,     CCRA      ;RESET RX
                       MOVE.B  #$40,     CCRB
                       MOVE.B  #02,      CCRA      ;ENABLE TX
                       MOVE.B  #02,      CCRB
                       MOVE.B  #$42,     CCRA      ;ENABLE RX
                       MOVE.B  #$42,     CCRB
            ;
            ;          WRITE/READ/VERIFY DATA IN LOCAL LOOPBACK MODE
            ;
                       CLR.L   D6                  ;CLR D6
                       MOVE.L  #GSR,A0             ;A0=POINTER TO STATUS REG
            AGAIN:     MOVE.B  D6,       TXFIFA    ;LOAD TX FIFO (A & B)
                       MOVE.B  D6,       TXFIFB
            CHA:       MOVE.B  [A0],     D2        ;CHECK FOR RXA READY
                       BTST    #0,       D2
                       BEQ     CHA                 ; WAIT FOR RX TO COME READY
                       MOVE.B  RXFIFA,   D0        ;READ RX FIFO A
                       CMP.B   D0,       D6        ;DOES RXA CHAR=TXA CHAR?
                       BEQ     CHB                 ;IF YES, THEN CHECK RXB
                       MOVE.W  #1,       D7        ;NO, THEN FLAG ERROR AND
            STOP       TRAP    #15
            CHB:       MOVE.B  RXFIFB,   D1        ;IS TX CHAR = RX CHAR (CHAN B)
                       CMP.B   D1,       D6
                       BEQ     INCD6               ;YES, THEN INC D6
                       MOVE.W  #2        D7        ;NO, THEN FLAG ERROR AND
            STOP       TRAP    #15
            INCD6:     ADDI.B  #1,       D6        ;INC D6
                       CMPI.B  #00       D6        ;HAS D6 ROLLED OVER TO 00?
                       BNE     AGAIN               ;IF NO, KEEP GOING 0–FF
                       MOVE.W  #0,       D7        ;IF YES, CLR ERROR AND STOP
                       TRAP    #15
            ;
                       END     SETUP
```

Figure 1. Minimum Number of Registers Needed to Program the DUSCC

This file sets up channel A to transmit and receive four BOP characters in the HDLC format. TXDA is tied to RXDA by a wire. Note that the end-of-message command is issued to the CCR before the last character is loaded in the transmitters.

```
Begin
;
            MOVE.B  #1,     CMR1A   ;BOP SECONDARY MODE, 8 BIT ADR, 8 BIT CONTROL
            MOVE.B  #$38,   CMR2A   ;POLLED/INT MODE, NORMAL MODE, NO FCS
            MOVE.B  #$3F,   TTRA    ;TX=38.4K BAUD
            MOVE.B  #$6F,   RTRA    ;RX=38.4K, DPLL X32 FROM BRG
            MOVE.B  #$E3,   TPRA    ;TX 8 BIT/CHAR,UNDERRUN=ABORT-FLAG,IDLE=FLAGS
            MOVE.B  #3,     RPRA    ;RX 8 BIT/CHAR,OVERRUN=HUNT,NO FCS OR EXT SYNC
            MOVE.B  #$F7,   OMRA    ;TXRDY=EMPTY, RXRDY=NOT EMPTY, NO RESID CHAR
            MOVE.B  #$FF,   S1RA    ;RX ADDRESS=HEX FF (SETUP FOR 8 BIT ADDRESS)
            MOVE.B  #0,     CCRA    ;RESET TX MOVE.B #$40,CCRA ; RESET TX
            MOVE.B  #2,     CCRA    ;ENABLE TX MOVE.B #$42,CCRA ; ENABLE RX
            MOVE.B  #$C3,   CCRA    ;SET NRZ MODE FOR DPLL
            MOVE.B  #$C0,   CCRA    ;ENTER SEARCH MODE
;
            BSR TXRDY               ;WAIT FOR TXRDY
            MOVE.B  #4,     CCRA    ;TRANSMIT START OF MESSAGE
            MOVE.B  #$FF,   TXFIFA  ;TRANSMIT HEX FF
            MOVE.B  #0,     TXFIFA  ;TRANSMIT HEX 0
            MOVE.B  #$AA,   TXFIFA  ;TRANSMIT HEX AA
            MOVE.B  #6,     CCRA    ;TRANSMIT END OF MESSAGE
            MOVE.B  #$55,   TXFIFA  ;TRANSMIT HEX 55
;
            BSR RXRDY               ;WAIT FOR RXRDY
            MOVE.B  RXFIFA, D0      ;READ FIRST CHAR
;
            BSR RXRDY               WAIT FOR RXRDY
            MOVE.B  RXFIFA, D1      ;READ SECOND CHAR
;
            BSR RXRDY               ;WAIT FOR RXRDY
            MOVE.B  RXFIFA, D2      ;READ THIRD CHAR
;
            BSR RXRDY               ;WAIT FOR RXRDY
            MOVE.B  RXFIFA, D3      ;READ FOURTH CHAR
            TRAP    #15             ;END TEST
;-------------------------------------------------------
;                           SUBROUTINES
;
TXRDY:      MOVE.B  GSR,    D6      ;MOVE GSR TO D6
            BTST    #1,     D6      ;TEST GSR1
            BEQ     TXRDY           ;IF GSR1=0 LOOP
            RTS
;
RXRDY:      MOVE.B  GSR,    D6      ;MOVE GSR TO D6
            BTST    #0,     D6      ;TEST GSR0
            BEQ     RXRDY           ;IF GSR0=0 LOOP
RTS
;           END
```

Figure 2. Example Using BOP Mode

```
This file sets up channel A to transmit and receive four BISYNC characters.  TXDA is tied to RXDA by a wire.

        Begin
        ;
                        MOVE.B  #1,     CMR1A   ;COP BISYNC MODE, EBCDIC
                        MOVE.B  #$3F,   CMR2A   ;POLLED/INT MODE, NORMAL, CCITT PRESET 1'S
                        MOVE.B  #$3F,   TTRA    ;38.4K BAUD
                        MOVE.B  #$6F,   RTRA    ;38.4K, DPLL X32 FROM BRG
                        MOVE.B  #$E3,   TPRA    ;TX=8 BIT/CHAR,UNDERRUN=SYNS, IDLE=SYNS
                        MOVE.B  #$83,   RPRA    ;RX=8 BIT/CHAR, STRIP SYN, NO FCS OR HUNT MODE
                        MOVE.B  #$F7,   OMRA    ;TXRDY=EMPTY, RXRDY=NOT EMPTY, NO RESID CHAR
                        MOVE.B  #$66,   S1RA    ;FIRST SYNC CHARACTER=HEX 66
                        MOVE.B  #$99,   S2RA    ;SECOND SYNC CHARACTER=HEX 99
                        MOVE.B  #0,     CCRA    ;RESET TX
                        MOVE.B  #$40,   CCRA,   ;RESET RX
                        MOVE.B  #$2,    CCRA    ;ENABLE TX
                        MOVE.B  #$42,   CCRA    ;ENABLE RX
                        MOVE.B  #$C3    CCRA    ;SET NRZ MODE FOR DPLL
                        MOVE.B  #$C0    CCRA    ;ENTER SEARCH MODE (DPLL)
        ;
                        BSR TXRDY               ;WAIT FOR TXRDY
                        MOVE.B  #4,     CCRA    ;TRANSMIT START OF MESSAG
                        MOVE.B  #$0D,   CCRA    ;EXCLUDE FROM CRC
                        MOVE.B  #2,     TXFIFA  ;TRANSMIT STX
                        MOVE.B  #$55,   TXFIFA  ;TRANSMIT TEXT (HEX 55)
                        MOVE.B  #$AA,   TXFIFA  ;TRANSMIT TEXT (HEX AA)
                        MOVE.B  #6,     CCRA    ;TRANSMIT END OF MESSAGE
                        MOVE.B  #3,     TXFIFA  ;TRANSMIT ETX
        ;
                        BSR RXRDY               WAIT FOR RXRDY
                        MOVE.B  RXFIFA,  D0     ;READ FIRST CHAR
        ;
                        BSR RXRDY               ;WAIT FOR RXRDY
                        MOVE.B  RXFIFA,  D1     ;READ SECOND CHAR
        ;
                        BSR RXRDY               ;WAIT FOR RXRDY
                        MOVE.B  RXFIFA,  D2     ;READ THIRD CHAR
        ;
                        BSR     RXRDY           ;WAIT FOR RXRDY
                        MOVE.B  RXFIFA,  D3     ;READ FOURTH CHAR.
                        TRAP    #15             ;END TEST
        ;-------------------------------------------------------------------
        ;                                       SUBROUTINES
        TXRDY:          MOVE.B  GSR,    D6      ;MOVE GSR TO D6
                        BTST    #1,     D6      ;TEST GSR1
                        BEQ     TXRDY           ;IF GSR1=0 LOOP
                        RTS
        ;
        RXRDY:          MOVE.B  GSR,    D6      ;MOVE GSR TO D6
                        BTST    #0,     D6      ;TEST GSR0 BEQ
                        RXRDY                   ;IF GSR0=0 LOOP
                        RTS
        ;
          END
```

Figure 3. Example Using COP Mode

This example does a DMA transfer of 256 bytes from memory to chan 'A' transmitter. It is set up in normal mode with TXA tied to RXB, and RTSB tied to CTSA by wire. (Receiver 'B' controls RTS, stopping any overruns). Flow control is imposed since the 8MHz CPU is too slow in testing the GSR and reading received characters.

```
SETUP:      MOVE.B  #0,         CCRA      ;RESET REQN(A) BY RESETTING TXA & RXB
            MOVE.B  #$40,       CCRB
            MOVE.B  #0,         PCRA      ;SET UP PIN CONFIGURATION REGISTER
            MOVE.B  #$20,       PCRB      ;RTS ENABLED FOR CHANNEL 'B'
            MOVE.B  #$7,        CMR1A     ;NO PARITY, ASYN MODE
            MOVE.B  #$7,        CMR1B
            MOVE.B  #0,         CMR2A     ;CHAN A = HALF DUPLEX SINGLE ADDRESS DMA
            MOVE.B  #$38,       CMR2B     ;CHAN B = NORMAL, POLLED/INTERRUPT
            MOVE.B  #$77,       TPRA      ;1 STOP BIT, 8-BIT, TX CONTROL BY CTS
            MOVE.B  #$3F,       TTRA      ;TX = BRG CLK, 38.4K BAUD
            MOVE.B  #13,        RPRB      ;RX = 8-BIT CHARACTERS, RXB CONTROLS RTS
            MOVE.B  #2F,        RTRB      ;RX = BRG CLK, 38.4K BAUD
            MOVE.B  #$F0,       OMRA,     ;TXRDY WITH FIFO NOT FULL (CHAN A)
            MOVE.B  #$F1,       OMRB      ;RXRDY WITH FIFO NOT EMPTY (CHAN B), RTS = 1
            MOVE.B  #0,         CCRA      ;RESET TXA & TXB
            MOVE.B  #0,         CCRB
            MOVE.B  #$40,       CCRB      ;RESET RXA & RXB
            MOVE.B  #$40,       CCRA
            MOVE.B  #2,         CCRA      ;ENABLE TXA
            MOVE.B  #$42,       CCRB      ;ENABLE RXB
            CLR.L   D6                    ;CLR D6
            MOVE.L  #GSR,       A0        ;A0=POINTER TO STATUS REG
            MOVE.L  #$77000,    A1        ;A1=MEMORY POINTER
*************************INITITALIZE MEMORY*************************************************
   AGAIN:   MOVE.W  D6,         [A1]+     ;D6 = DATA VALUE
            ADDI.B  #1,         D6
            CMPI.B  #0,         D6        ;DOES D6=FF ?
            BNE     AGAIN                 ;CONTINUE UNTIL IT DOES
;**********************INITIALIZE DMA CONTROLLER TO WRITE TO TRANSMITTER*****************
SETDMA:     MOVE.B  #$B8,       CSR       ;RESET DMAI
            MOVE.B  #$18,       DCR       ;BURST MODE
            MOVE.B  #$12,       OCR       ;MEMORY TO DEVICE TRANSFER, BYTE
            MOVE.B  #1,         MTCH      ;SET COUNTER TO TRANSFER 256 CHAR
            MOVE.B  #0,         MTCL      ;MEMORY ADDRESS = 77000
            MOVE.B  #$7,        MACMH
            MOVE.B  #$70,       MACML
            MOVE.B  #$0,        MACL
            MOVE.W  #$100,      D6
            CLR.L   D1
            MOVE.B  #$B8,       CSR       ;RESET DMAI
;           MOVE.B  #$80,       CCRX      ;DMAI START OPERATION
;*****************************REA/VERIFY DMA PROCESS*************************************
RXRDYB:     MOVE.B  [A0],       D0        ;CHECK FOR RXB READY
            BTST    #4,         D0
            BEQ     RXRDYB                ;WAIT FOR RX TO COME READY
            MOVE.B  #4,         GSR       ;RESET RXRDY 'B'
            MOVE.B  RXFIFB,     D2
            CMP.B   D1,         D2
            BNE     STOP                  ;IF TX NOT EQUAL TO RX, STOP
            ADDI.B  #1,         D1        ;INC CHARACTER POINTER
            CMP.B   D6,         D1        ;HAVE WE RECEIVED FOUR CHARACTERS?
            BNE     RXRDYB                ;IF NOT, GET THE NEXT RX CHAR
STOP:       TRAP    #15                   ;END TEST
;           END     SETUP
```

Figure 4. DMA Transmit Program

This example does a DMA transfer of 256 bytes from memory to chan 'A' transmitter. It is set up in normal mode with TXB tied to RXA. No flow control is imposed.

```
SETUP:      MOVE.B  #43,        CCRA        ;RESET REQN(A) BY DISABLING RXA
            MOVE.B  #$40,       CCRB        ;DISABLE TXB
            MOVE.B  #7,         CMR1A       ;NO PARITY ASYN MODE
            MOVE.B  #7,         CMR1B
            MOVE.B  #0,         CMR2A       ;CHAN A = HALF DUPLEX SINGLE ADDRESS DMA
            MOVE.B  #$38,       CMR2B       ;CHAN B=NORMAL, POLLED/INTERRUPT
            MOVE.B  #$73,       TPRB        ;1 STOP BIT, 8 BIT CHAR
            MOVE.B  #$3F,       TTRB        ;TX=BRG CLK, 38.4 BAUD
            MOVE.B  #3,         RPRA        ;RX = 8 BIT CHARACTERS
            MOVE.B  #$2F,       RTRA        ;RX = BRG CLK, 38.4K BAUD
            MOVE.B  #$13,       RPRB        ;RXRDY WITH FIFO NOT EMPTY (CHAN A)
            MOVE.B  #$E0,       OMRA        ;RX = BRG CLK, 38.4K BAUD
            MOVE.B  #$E0,       OMRB,       ;TXRDY WITH FIFO NOT FULL (CHAN B)
            MOVE.B  #0,         CCRB        ;RESET TXB
            MOVE.B  #0,         CCRA        ;RESET RXA
            MOVE.B  #2,         CCRB        ;ENABLE TXB
            MOVE.B  #$42,       CCRB        ;ENABLE RXA
            MOVE.B  #GSR,       A0          ;A0 = POINTER TO STATUS REG
            MOVE.B  #RAM,       A1          ;A1 = MEMORY POINTER
;*****************************************CLEAR MEMORY*****************************************
AGAIN:      MOVE.W  #0,         [A1]+
            CMPA.L  #RAMEND, A1
            BNE     AGAIN
;*********************INITITALIZE DMA CONTROLLER TO READ RECEIVER*****************************
SETDMA:     MOVE.B  #$B8,       CSR         ;RESET DMAI
            MOVE.B  #$38,       DCR         ;BURST MODE
            CMPI.B  #$92,       OCR         ;DEVICE TO MEMORY TRANSFER, WORD
            MOVE.B  #1,         MTCH        ;SET COUNTER TO TRANSFER 256
CHAR        MOVE.B  #0,         MTCL
            MOVE.B  #7,         MACMH       ;LOCAL RAM ADDRESS = 77000
            MOVE.B  #$70,       MACML
            MOVE.B  #$0,        MACL
            CLR.L   D1
            MOVE.B  #$80,       CCRX        ;DMAI START OPERATION
;*****************************CPU WRITES TO TXB WHILE DMA READS RXA*********************
TXRDYB:     MOVE.B  [A0],       D0
            BTST    #5,         D0          ;CHECK FOR TXB READY
            BEQ     TXRDYB                  ;WAIT FOR TX TO COME READY
            MOVE.B  D1,         TXFIFB
            ADDI.B  #1,         D1          ;INC CHARACTER POINTER
            CMPI.B  #0,         D1          ;STOP AFTER 256 TXB CHAR-
ACTERS      BNE     TXRDYB                  ;IF NOT, SENT THE NEXT TX CHAR
;*****************************CPU VERIFIES RECEIVED DATA IN MEMORY*****************************************
            CLR.L   D1
            MOVE.L  #RAM,       A1          ;MEM START ADDRESS
VERIFY      MOVE.W  [A1]+,      D2          ;READ NEXT RAM LOCATION
            CMP.B   D1,         D2
            BNE     STOP                    ;STOP IF RX CHAR NOT EQUAL TO TX CHAR
            ADDI.B  #1,         D1
            CMP.L   RAMEND,     A1          ;HAVE WE COMPARED ALL RXA CHAR?
            BNE     VERIFY                  ;IF NOT, KEEP LOOPING
STOP:       TRAP    #15                     ;END TEST
;           END     SETUP
```

Figure 5. DMA Receive Program

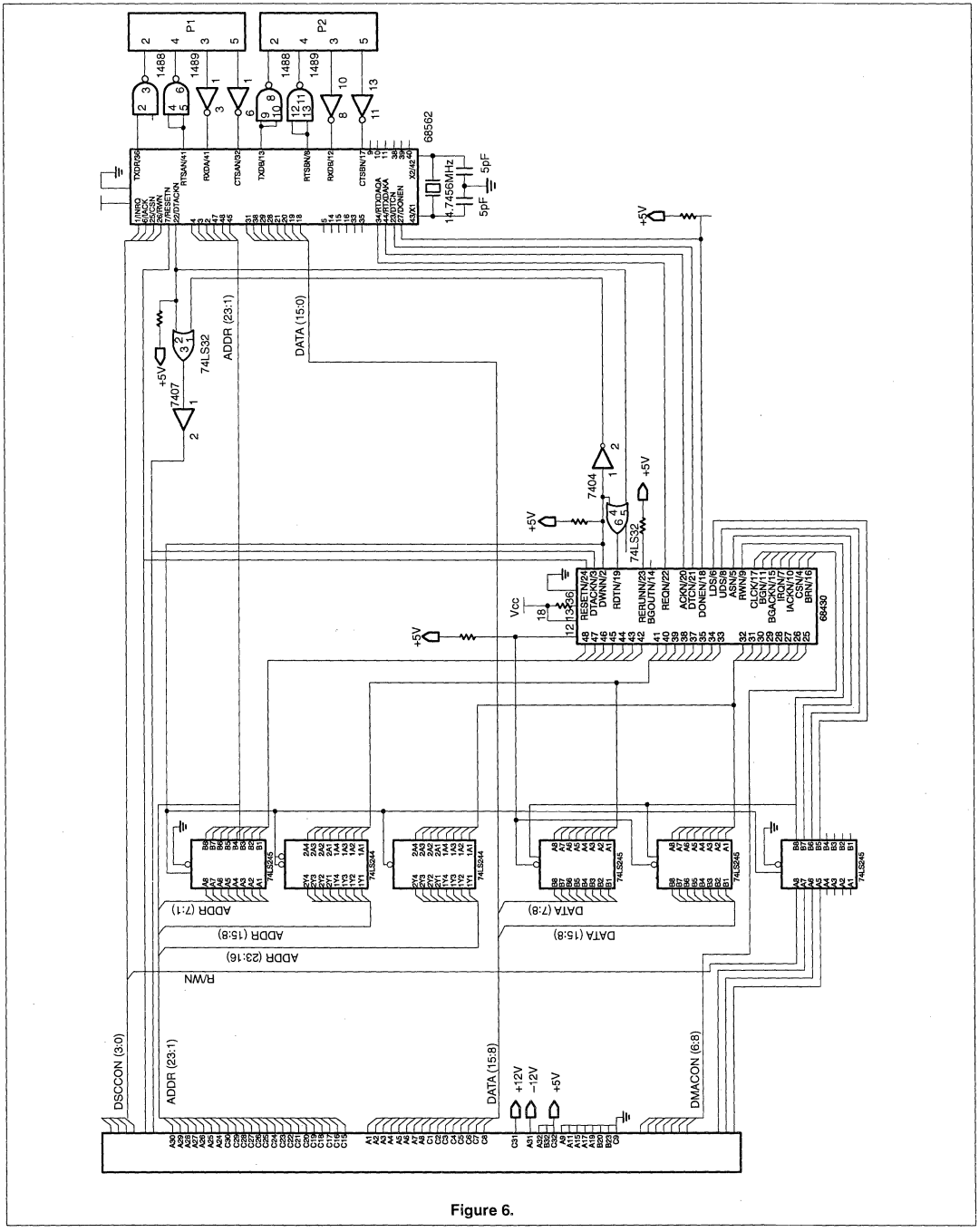

P1
P2
1488
1489
68562
14.7456MHz
5pF
74LS32
7407
7404
ADDR (23:1)
DATA (15:0)
+5V
Vcc
68430
74LS245
74LS244
ADDR (7:1)
ADDR (15:8)
ADDR (23:16)
DATA (7:8)
DATA (15:8)
R/WN
DSCCON (3:0)
ADDR (23:1)
DATA (15:8)
DMACON (6:8)
+12V
−12V
+5V

Figure 6.

CMOS dual universal serial communications controller (CDUSCC) — SC26C562

DESCRIPTION

The Philips Semiconductors SC26C562 Dual Universal Serial Communications Controller (CDUSCC) is a single-chip CMOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SC26C562 interfaces to synchronous bus MPUs and is capable of program-polled, interrupt driven, block-move or DMA data transfers.

The SC26C562 (CDUSCC) is (PIN) hardware and (REGISTER) software compatible with the existing SCN26562 (DUSCC). CDUSCC will automatically configure to the NMOS DUSCC register map (default mode) on power up.

The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides sixteen common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the CDUSCC well-suited for dual-speed channel applications. Data rates up to 10Mbits per second are supported.

The transmitter and receiver each contain a sixteen-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to sixteen characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs and outputs are general purpose in nature, they can be optionally programmed for other functions.

The SC26C562 CDUSCC is optimized to interface with processors using a synchronous bus interface, such as the 8086, and iAPX86 family. For systems using an asynchronous bus, such as the 68000 and 68010, refer to the SC68C562 documentation.

Refer to the CMOS Dual Universal Serial Communication Controller (CDUSCC) User's Manual for a complete operational description.

FEATURES

General Features

- Dual full-duplex synchronous/ asynchronous receiver and transmitter
- Multi-protocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: Single SYNC, dual SYNC, BiSYNC, DDCMP
  - ASYNC: 5-8 bits plus optional parity
- Sixteen character receive and transmit FIFOs with interrupt threshold control
- FIFO'ed status bits
- Watchdog timer
- 0 to 10 Mbit/sec data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 19 fixed rates: 50 to 64K baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- or half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Compatible with Synchronous and Asynchronous bus DMA controllers
  - Half- or full-duplex operation
  - Single or dual address data transfers
  - Automatic frame termination on counter/ timer terminal count or DMA DONE (EOPN)
- Transmit path clear status
- High speed data bus interface: 160ns bus cycle
- DPLL operation up to 312.5kHz with internal clock
- Interrupt capabilities
  - Vector output (fixed or modified by status)
  - Individual interrupt enable bits
  - Programmable internal priorities
  - Maskable interrupt conditions
  - 80XX/X compatible
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general purpose I/O pins per channel
  - CTS and DCD programmable auto-enables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits

CMOS dual universal serial communications controller (CDUSCC) SC26C562

- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X Rx and Tx clock factors
- Parity, overrun and framing error detection
- False start bit detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmit and receive up to 10Mbps at 1x or 1Mbps at 16x data rates

Bit-Oriented Protocol

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for I field
- Zero insertion and deletion
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Transmit 7 or 8 bit ABORT
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

Character-Oriented Protocols

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK line-fill or underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun and underrun error detection
- Optional SYNC exclusion from FCS
- BISYNC features
  - EBCDIC or ASCII header, text and control messages
  - SYN, DLE stripping
  - EOM (end of message) detection and transmission
  - Auto transparency mode switching
  - Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
  - Control character sequence detection for both transparent and normal text
  - Parity generation for data and LRC characters

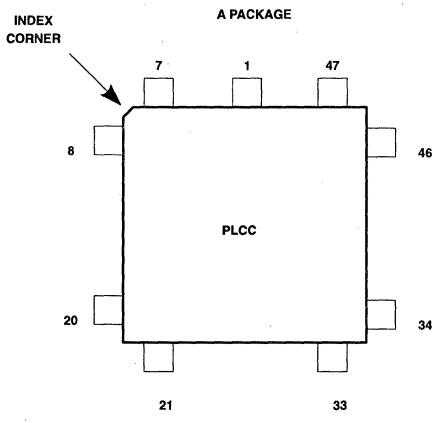
ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±10%, T_A = 0 to +70°C	V_{CC} = +5V ±10%, T_A = –40 to +85°C	DWG #
	Serial Data Rate = 10Mbps Maximum	Serial Data Rate = 8Mbps Maximum	
48-Pin Plastic Dual In-Line Package (DIP)	SC26C562C1N	Not available	0416C
52-Pin Plastic Leaded Chip Carrier (PLCC) Package	SC26C562C1A	SC26C562A8A	0397E

ABSOLUTE MAXIMUM RATINGS[1]

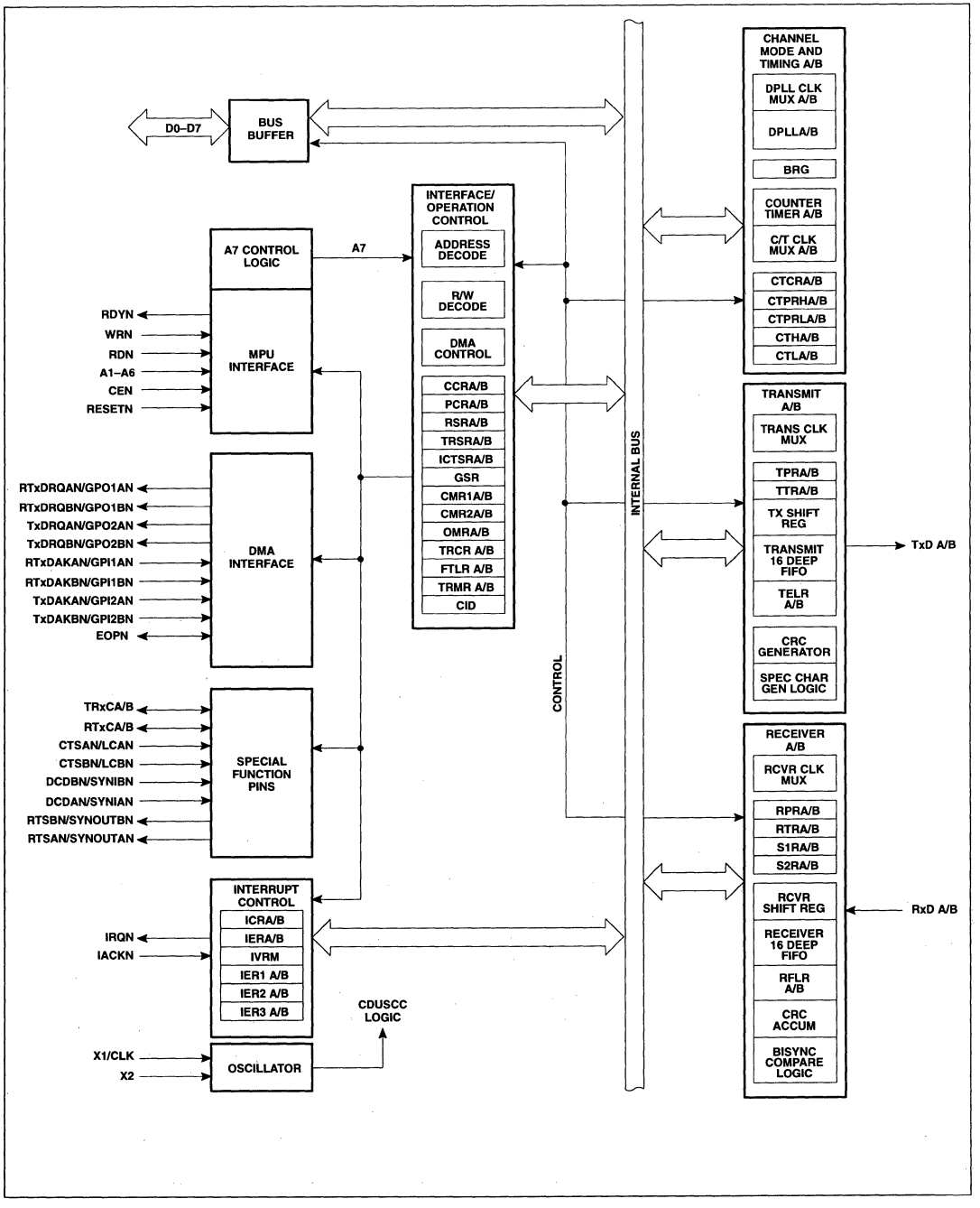
SYMBOL	PARAMETER	RATING		UNIT
		Commercial	Automotive	
T_A	Operating ambient temperature[2]	0 to +70	-40 to +85	°C
T_{STG}	Storage temperature	-65 to +150	-65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	–0.5 to +7.0	–0.5 to +7.0	V
V_S	Voltage from any pin to ground[3]	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V

PIN CONFIGURATIONS



PIN	FUNCTION	PIN	FUNCTION
1	IACKN	27	CSN
2	A3	28	WRN
3	A2	29	EOPN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
6	IRQN	32	D1
7	GND	33	D0
8	RDYN	34	V_{CC}
9	RSTBN/ SYNOUTBN	35	CTSAN/LCAN
10	TRxCB	36	TxDRQAN/ GPO2AN/ RTSAN
11	RTxCB	37	RTxDRQAN/ GPO1AN
12	DCDBN/ SYNIBN	38	TxDAKAN/ GPI2AN
13	GND	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	GND
16	TxDAKBN/ GPI2BN	42	DCDAN/ SYNIAN
17	RTxDRQBN/ GPO1BN	43	RTxCA
18	TxDRQBN/ GPO2BN/ RTSBN	44	TRxCA
19	CTSBN/LCBN	45	RTSAN/ SYNOUTAN
20	D7	46	X2
21	D6	47	X1/CLK
22	D5	48	RTxDAKAN/ GPI1AN
23	D4	49	A6
24	RDN	50	A5
25	RESETN	51	A4
26	GND	52	V_{CC}

BLOCK DIAGRAM — SC26C562



PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A1–A6	4-2, 47-45	4-2, 51-49	I	**Address Lines:** Active-high. Address inputs which specify which of the internal registers is accessed for read/write operation.
D0–D7	31-28, 21-18	33-30, 23-20	I/O	**Bidirectional Data Bus:** Active-high, 3-State. Bit 0 is the LSB and bit 7 is the MSB. All data, command and status transfers between the CPU and the CDUSCC take place over this bus. The data bus is enabled when CSN and RDN, or CSN and WRRN are low during interrupt acknowledge cycles and single address DMA acknowledge cycles.
RDN	22	24	I	**Read Strobe:** Active-low input. When active and CSN is also active, causes the content of the addressed register to be present on the data bus. RDN is ignored unless CSN is active.
WRN	26	28	I	**Write Strobe:** Active-low input. When active and CSN is also active, the content of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of WRN. WRN is ignored unless CEN is active.
CSN	25	27	I	**Chip Select:** Active-low input. When active, data transfers between the CPU and the CDUSCC are enabled on D0–D7 as controlled by RDN or WRN and A1–A6 inputs. When CSN is high, the data lines are placed in the 3-State condition (except during interrupt acknowledge cycles and single address DMA transfers).
RDYN	7	8	O	**Ready:** Active-low, open drain. Used to synchronize data transfers between the CPU and the CDUSCC. It is valid only during read and write cycles where the CDUSCC is configured in 'wait on Rx', 'wait on Tx' or 'wait on Tx or Rx' modes, otherwise it is always inactive. RDYN becomes active on the leading edge of RDN and WRN if the requested operation cannot be performed (viz, no data in RxFIFO in the case of a read or no room in the TxFIFO in the case of a write).
IRQN	6	6	O	**Interrupt Request:** Active-low, open-drain. This output is asserted upon occurrence of any enabled interrupting condition. The CPU can read the general status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the CDUSCC to output an interrupt vector on the data bus.
IACKN	1	1	I	**Interrupt Acknowledge:** Active-low. When IACKN is asserted, the CDUSCC responds by either forcing the bus into high-impedance, placing a vector number, call instruction or zero on the data bus. The vector number can be modified or unmodified by the status. If no interrupt is pending, IACKN is ignored and the data bus placed in high-impedance.
X1/CLK	43	47	I	**Crystal or External Clock:** When using the crystal oscillator, the crystal is connected between pins X1 and X2. If a crystal is not used, an external clock is supplied at this input. This clock is used to drive the internal bit rate generator, as an optional input to the counter/timer or DPLL, and to provide other required clocking signals. When a crystal is used, a capacitor must be connected from this pin to ground.
X2	42	46	O	**Crystal 2:** Connection for other side of crystal. When a crystal is used, a capacitor must be connected from this pin to ground. If an external clock is used on X1, this pin should be left floating.
RESETN	23	25	I	**Master Reset:** Active-low. A low on this pin resets the transmitters and receivers and resets the registers shown in Table 1 of the CDUSCC Users' Guide. Reset is asynchronous, i.e., no clock is required.
RxDA, RxDB	37, 12	40, 14	I	**Channel A (B) Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified for the channel, the input is sampled on the rising edge of the clock.
TxDA, TxDB	36, 13	39, 15	O	**Channel A (B) Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is in the marking (high) condition when the transmitter is disabled or when the channel is operating in local loopback mode. If external transmitter clock is specified for the channel, the data is shifted on the falling edge of the clock.
RTxCA, RTxCB	39, 10	43, 11	I/O	**Channel A (B) Receiver/Transmitter Clock:** As an input, it can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the transmitter shift clock (1X), or the receiver sampling clock (1X).
TRxCA, TRxCB	40, 9	44, 10	I/O	**Channel A (B) Transmitter/Receiver Clock:** As an input, it can supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the DPLL output, the transmitter shift clock (1X), the receiver sampling clock (1X), the transmitter BRG clock (16X), The receiver BRG clock (16X), or the internal system clock (X1 ÷ 2).

PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO. DIP	PIN NO. PLCC	TYPE	NAME AND FUNCTION
CTSA/BN, LCA/BN	32, 17	35, 19	I/O	**Channel A (B) Clear-to-Send Input or Loop Control Output:** Active-low. The signal can be programmed to act as an enable for the transmitter when not in loop mode. The CDUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. When operating in the BOP loop mode, this pin becomes a loop control output which is asserted and negated by CDUSCC commands. This output provides the means of controlling external loop interface hardware to go on-line and off-line without disturbing operation of the loop.
DCDA/BN, SYNIA/BN	38, 11	42, 12	I	**Channel A (B) Data Carrier Detected or External Sync Input:** The function of this pin is programmable. As a DCD active-low input, it acts as an enable for the receiver or can be used as a general purpose input. For the DCD function, the CDUSCC detects logic level transitions on this pin and can be programmed to generate an interrupt when a transition occurs. As an active-low external sync input, it is used in COP mode to obtain character synchronization for the receiver without receipt of a SYN character. This mode can be used in disc or tape controller applications or for the optional byte timing lead in X.21.
RTxDRQA/BN, GPO1A/BN	34, 15	37, 17	O	**Channel A (B) Receiver/Transmitter DMA Service Request or General Purpose Output:** Active-low. For half-duplex DMA operation, this output indicates to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or that the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, this output indicates to the DMA controller that data is available in the receiver FIFO. In non-DMA mode, this pin is a general purpose output that can be asserted and negated under program control.
TxDRQA/BN, GPO2A/BN, RTSA/BN	33, 16	36, 18	O	**Channel A (B) Transmitter DMA Service Request, General Purpose Output, or Request-to-Send:** Active-low. For full-duplex DMA operation, this output indicates to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full-duplex DMA mode, this pin can be programmed as a general purpose or a Request-to-Send output, which can be asserted and negated under program control.
RTxDAKA/BN, GPI1A/BN	44, 5	48, 5	I	**Channel A (B) Receiver/Transmitter DMA Acknowledge or General Purpose Input:** Active-low. For half-duplex single address operation, this input indicates to the CDUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO when the receiver is enabled or load transmitter FIFO when the transmitter is enabled) is beginning. For full-duplex single address DMA operation, this input indicates to the CDUSCC that the DMA controller has acquired the bus and that the requested read receiver FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in single address DMA mode.
TxDAKA/BN, GPI2A/BN	35, 14	38, 16	I	**Channel A (B) Transmitter DMA Acknowledge or General Purpose Input:** Active-low. When the channel is programmed for full-duplex single address DMA operation, this input is asserted to indicate to the CDUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in full-duplex single address DMA mode.
EOPN	27	29	I/O	**Done (EOP):** Active-low, open-drain. EOPN can be used and is active in both DMA and non-DMA modes. As an input, EOPN indicates the last DMA transfer cycle to the TxFIFO. As an output, EOPN indicates either the last DMA transfer from the RxFIFO or that the transmitted character count has reached terminal count.
RTSA/BN, SYNOUTA/BN	41, 8	45, 9	O	**Channel A (B) Sync Detect or Request-to-Send:** Active-low. If programmed as a sync output, it is asserted one bit time after the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes) is detected by the receiver. As a Request-to-Send modem control signal, it functions as described previously for the TxDRQN/RTSN pin.
V_{CC}	48	34, 52	I	**+5V Power Input**
GND	24	26, 13, 41, 7	I	**Signal and Power Ground Input**

DC ELECTRICAL CHARACTERISTICS[4,5] T_A = 0°C to +70°C, V_{CC} = 5.0V ±10%[4,5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input low voltage:					
V_{IL}	All except X1/CLK				0.8	V
	X1/CLK				0.8	V
	Input high voltage:					
V_{IH}	All except X1/CLK		2.0 (Comm)			V
			2.3 (Auto)			V
	X1/CLK		0.8 x V_{CC}		V_{CC}	V
V_{OL}	Output low voltage:					
	All except IRQN[7]	I_{OL}=5.3mA(Comm), 4.8mA(Auto)				V
	IRQN	I_{OL}=8.8mA(Comm), 7.8mA(Auto)			0.5	V
V_{OH}	Output high voltage:				0.5	
	(Except open drain outputs)	I_{OH} = –400µA	V_{CC}–0.5			V
I_{ILX1}	X1/CLK input low current[10]	V_{IN} = 0, X2 = open	–150		0.0	µA
I_{IHX1}	X1/CLK input high current[10]	V_{IN} = V_{CC}, X2 = GND			150	µA
I_{SCX2}	X2 short circuit current	X1 = open, V_{IN} = 0			–15	mA
		V_{IN} = V_{CC}			+15	mA
I_{IL}	Input low current RESETN, TxDAKN, RxDAKN	V_{IN} = 0	–15		–0.5	µA
I_I	Input leakage current	V_{IN} = 0 to V_{CC}	–1 (Comm) –10 (Auto)		+1 (Comm) +10 (Auto)	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			+1 (Comm) +10 (Auto)	µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0	–1 (Comm) –10 (Auto)			µA
I_{ODL}	Open drain output low current in off state: EOPN, RDYN	V_{IN} = 0	–15		–0.5	µA
	IRQN		–1			µA
I_{ODH}	Open drain output high current in off state: EOPN, IRQN, RDYN	V_{IN} = V_{CC}	–1		1	µA
I_{CC}	Power supply current (see Figure 17 for graphs)	V_O = 0 to V_{CC} Rx and Tx clocks at 10MHz X1 clock at 10MHz		25	80 (Comm) 95 (Auto)	mA
C_{IN}	Input capacitance[9]	V_{CC} = GND = 0			10	pF
C_{OUT}	Output capacitance[9]	V_{CC} = GND = 0			15	pF
$C_{I/O}$	Input/output capacitance[9]	V_{CC} = GND = 0			20	pF

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
2. Clock may be stopped (DC) for testing purposes, or when CDUSCC is in non-operational modes.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.2V and 3.0V with a transition time of 20ns maximum. For X1/CLK, this swing is between 0.2V and 4.4V. All time measurements are referenced at input voltages of 0.2V and 3.0V and output voltages of 0.8V and 2.0V, as appropriate.
6. See Figure 18 for test conditions for outputs.
7. Tests for open drain outputs are intended to guarantee switching of the output transistor. Measurement of this response is referenced from midpoint of the switching signal to a point 0.2V above the actual output signal level. This point represents noise margin that assures true switching has occurred.
8. Execution of the valid command (after it is latched) requires 3 rising edges of X1 (see Figure 15).
9. These values were not explicitly tested; they are guaranteed by design and characterization data.
10. X1/CLK and X2 are not tested with a crystal installed.
11. X1/CLK frequency must be at least the faster of the receiver or transmitter serial data rate.
12. Timing is illustrated and referenced to the WRN and RDN inputs. The device may also be operated with CSN as the 'strobing' input. CSN and RDN (also CSN and WRN) are ANDed internally. As a consequence, the signal asserted last initiates the cycle and the signal negated first terminates the cycle.

AC ELECTRICAL CHARACTERISTICS[4,5,6,7] T_A = 0°C to +70°C, V_{CC} = 5V ±10%

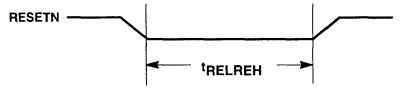


Figure 1. Reset Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{RELREH}	RESETN low to RESETN high	200		200		ns

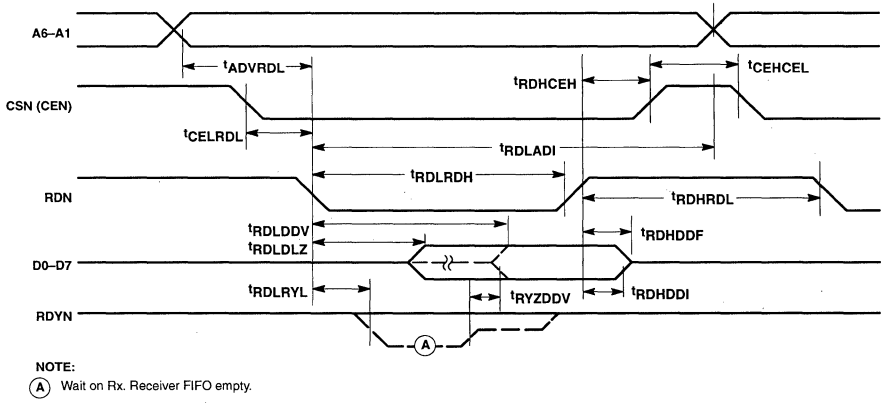


Figure 2. Read Cycle[12]

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{ADVRDL}	Address valid to RDN low	10		5		ns
t_{CELRDL}	CEN low to RDN low	10		0		ns
t_{RDLADI}	RDN low to address invalid	60		50		ns
t_{RDLRYL}	RDN low to RDYN low		160		150	ns
t_{RDLDDV}	RDN low to read data valid		150		130	ns
t_{RDLRDH}	RDN low to RDN high	150		130		ns
t_{RYZDDV}	RDYN high impedance to read data valid[9]		90		90	ns
t_{RDHCEH}	RDN high to CEN high	10		0		ns
t_{CEHCEL}	CEN high to CEN low	50		30		ns
t_{RDHDDI}	RDN high to read data invalid	5		5		ns
t_{RDHRDL}	RDN high to RDN low	50		30		ns
t_{RDHDDF}	RDN high to data bus floating		50		40	ns
t_{RDLDLZ}	RDN low to data bus low impedance[9]	5		10		ns

AC ELECTRICAL CHARACTERISTICS (Continued)

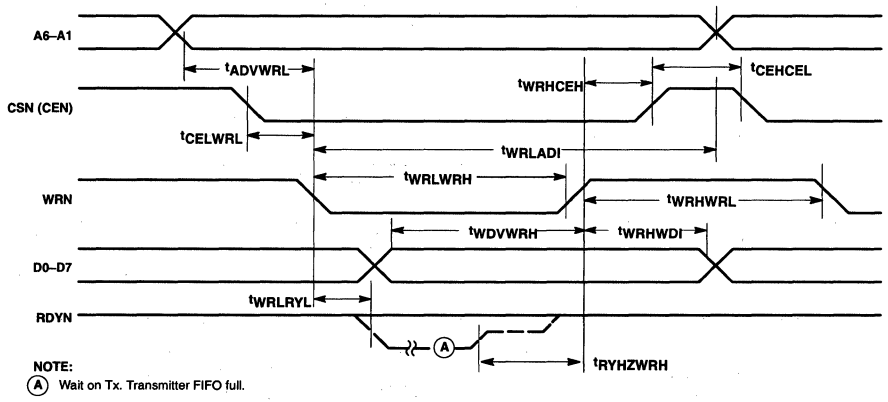
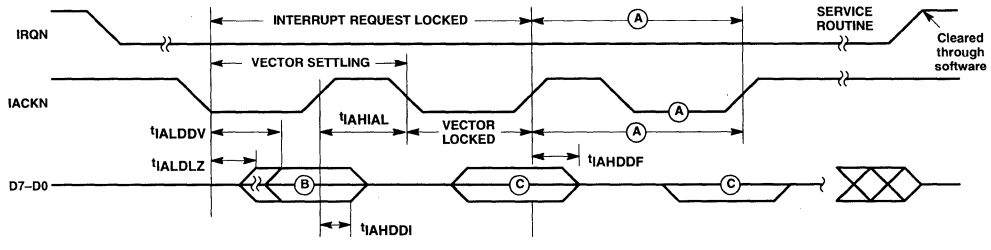


Figure 3. Write Cycle[12]

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{ADVWRL}	Address valid to WRN low	10		5		ns
t_{CELWRL}	CSN low to WRN low	10		0		ns
t_{WRLRYL}	WRN low to RDYN low					ns
t_{WRHCEH}	WRN high to CSN high	10		0		ns
t_{WRLWRH}	WRN low to WRN high	110		100		ns
t_{WDVWRH}	Write data valid to WRN high	65		60		ns
t_{CEHCEL}	CEN high to CEN low	50	160	30	150	ns
t_{WRLADI}	WRN low to address invalid	60		50		ns
t_{WRHWRL}	WRN high to WRN low	50		30		ns
t_{WRHWDI}	WRN high to write data invalid	10		5		ns
$t_{RYHZWRH}$	RDYN hi impedance to WRN high[9]	10		0		ns

AC ELECTRICAL CHARACTERISTICS (Continued)



NOTES:
(A) ICR[5:4] = 01 or 10 (mode 1 or mode 2)
(B) Call instruction (mode 2)
(C) ICR[5:4] = 11 (mode 3)

Figure 4. Interrupt Acknowledge Cycle

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{IALDDV}	IACKN low to data bus valid					ns
t_{IAHDDF}	IACKN high to data bus floating		140		130	ns
t_{IAHDDI}	IACKN high to data bus invalid	5	60	5	60	ns
t_{IALDLZ}	IACKN low to data bus low impedance[9]	5		10		ns
t_{IAHIAL}	IACKN high to low	40		30		ns

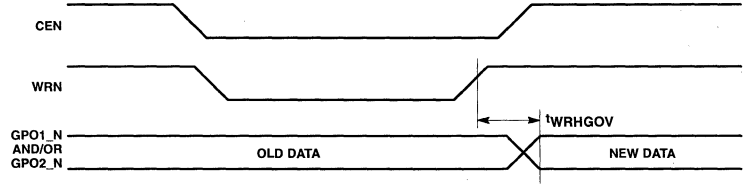


Figure 5. Output Port Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{WRHGOV}	WRN high to GPO output data valid		100		100	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

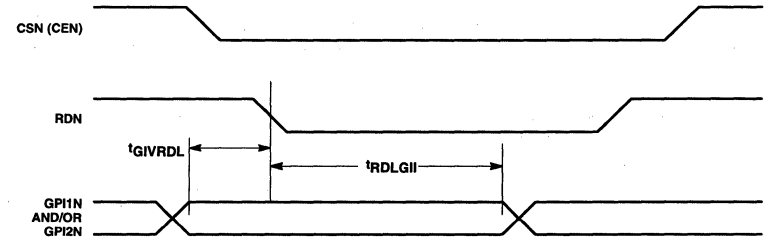


Figure 6. Input Port Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{GIVRDL}	GPI input valid to RDN low	20		20		ns
t_{RDLGII}	RDN low to GPI input invalid	40		40		ns

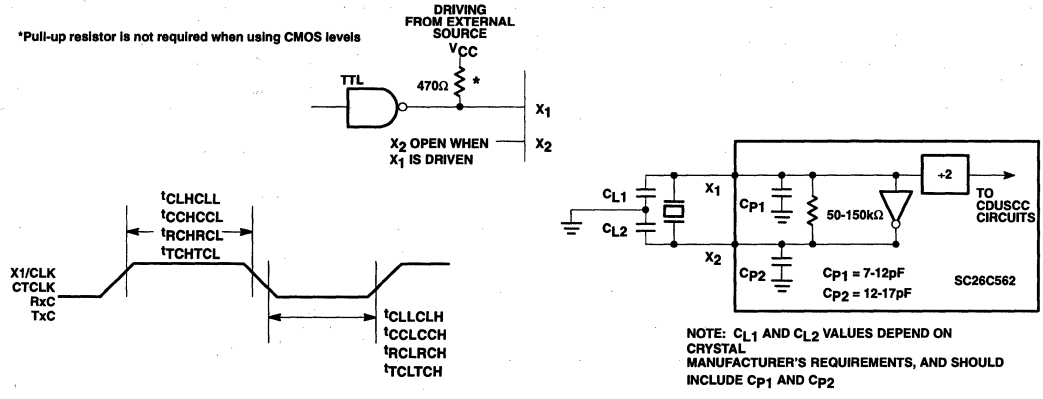
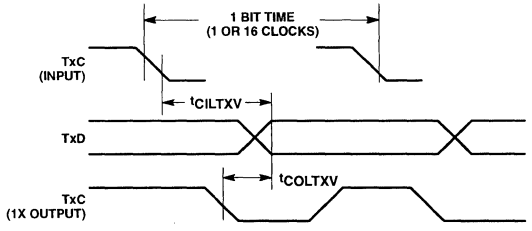


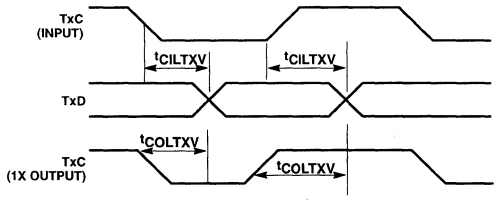
Figure 7. Clock Timing

SYMBOL	PARAMETER	LIMITS						UNIT
		AUTOMOTIVE SC26C562			COMMERCIAL SC26C562			
		Min	Typ	Max	Min	Typ	Max	
t_{CLHCLL}	X1/CLK high to low time	25			25			ns
t_{CLLCLH}	X1/CLK low to high time	25			25			ns
t_{CCHCCL}	C/T CLK high to low time	50			45			ns
t_{CCLCCH}	C/T CLK low to high time	50			45			ns
t_{RCHRCL}	RxC high to low time	55			50			ns
t_{RCLRCH}	RxC low to high time	55			50			ns
t_{TCHTCL}	TxC high to low time	55			50			ns
t_{TCLTCH}	TxC low to high time	55			50			ns
f_{CL}	X1/CLK frequency[11]	0		16.0	0		16.0	MHz
f_{CC}	C/T CLK frequency	0		8	0		10	MHz
f_{RC}	RxC frequency (16X or 1X @ 50% duty cycle)	0	14.7456	8	0	14.7456	10	MHz
f_{TC}	TxC frequency (16X or 1X @ 50% duty cycle)	0		8	0		10	MHz
f_{RTC}	Tx/Rx frequency for FM/Manchester encoding			4			5	MHz

AC ELECTRICAL CHARACTERISTICS (Continued)



a. Transmit Timing NRZ

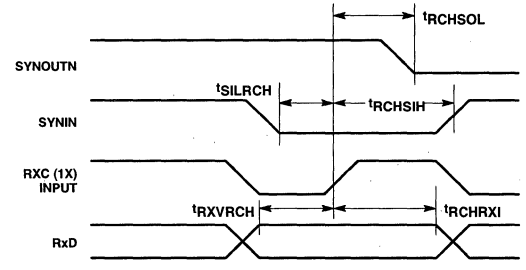


b. Transmit Timing FM0/1, Manchester Encoding

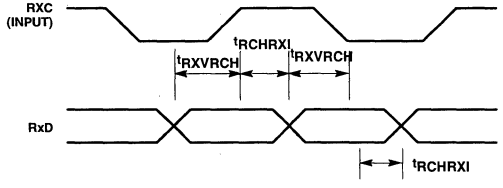
Figure 8.

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{CILTXV}	TxC input low (1X) to TxD output		120		120	ns
	TxC input low (16X) to TxD output		120		120	ns
t_{COLTXV}*	TxC output low to TxD output[9] (NRZ, NRZI)		25		20	ns
	FM, MAN		35		30	ns

*Characterized with no loads on TxD and TxC outputs



a. Receive Timing NRZ



b. Receive Timing FM0/1, Manchester Encoding

Figure 9.

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{RXVRCH}	RxD data valid to RxC high:					
	For NRZ data	25		20		ns
	For NRZI, Manchester, FM0, FM1 data	30		30		ns
t_{RCHRXI}	RxC high to RxD data invalid:					
	For NRZ data	25		20		ns
	For NRZI, Manchester, FM0, FM1 data	30		30		ns
t_{SILRCH}	SYNIN low to RxC high	50		50		ns
t_{RCHSIH}	RxC high to SYNIN high	20		20		ns
t_{RCHSOL}	RxC high to SYNOUT low		110		100	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

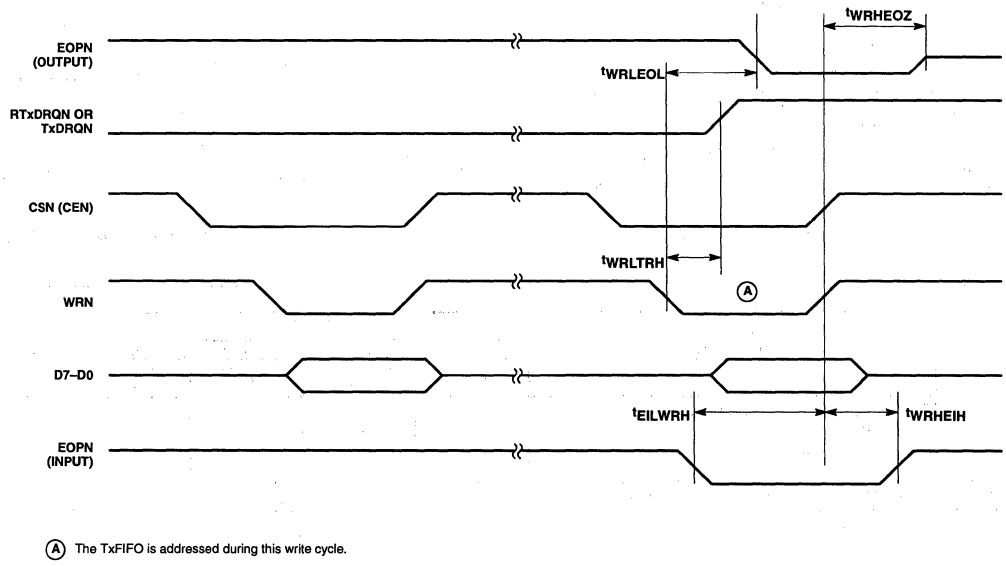
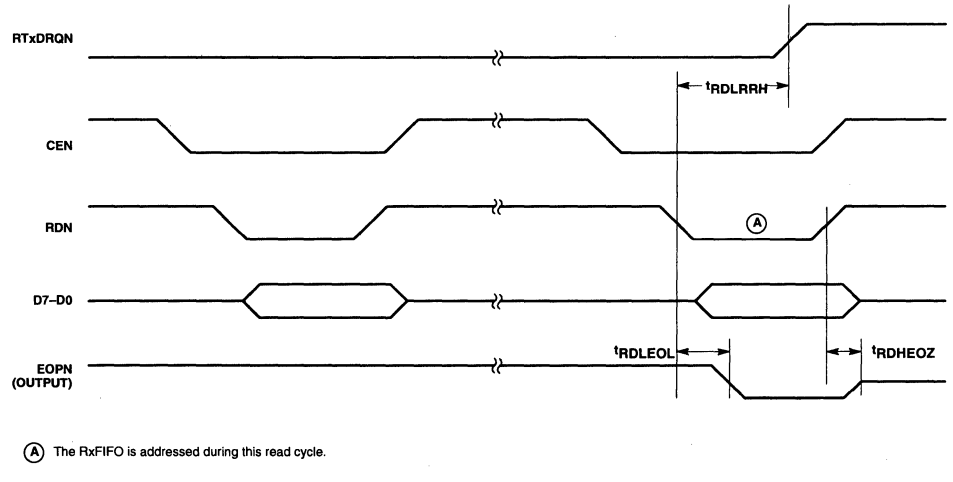


Figure 10. Transmit Dual Address DMA Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{WRLTRH}	WRN low to Tx DMA REQN high					ns
t_{WRLEOL}	WRN low to EOPN output low		110		100	ns
t_{WRHEOZ}	WRN high to EOPN output high impedance		110		100	ns
t_{EILWRH}	EOPN input low to WRN high	35	70	30	60	ns
t_{WRHEIH}	WRN high to EOPN input high	30		25		ns

AC ELECTRICAL CHARACTERISTICS (Continued)

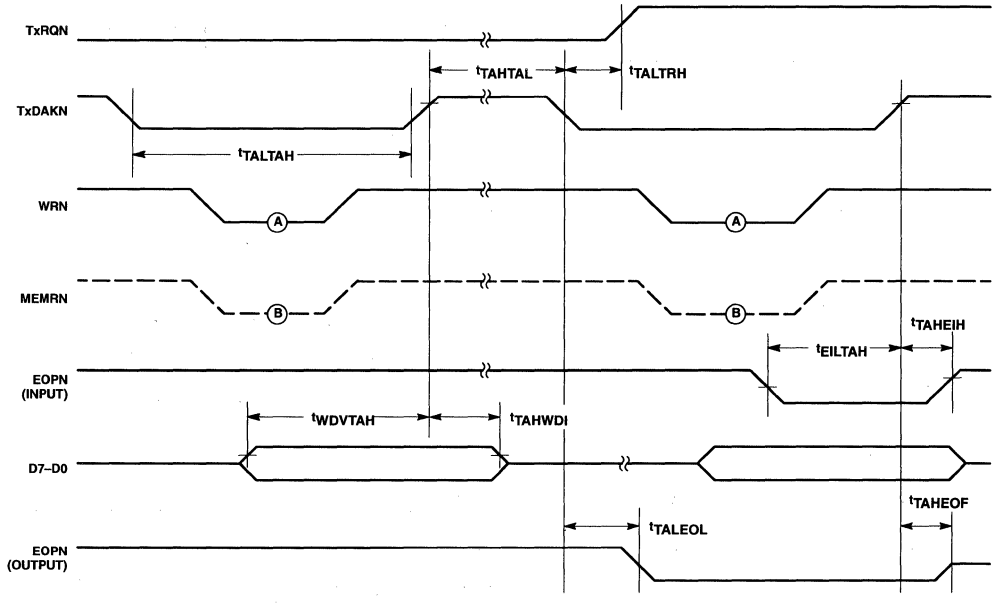


(A) The RxFIFO is addressed during this read cycle.

Figure 11. Receive Dual Address DMA Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{RDLRRH}	RDN low to Rx DMA REQN high		110		100	ns
t_{RDLEOL}	RDN low to EOPN output low		110		100	ns
t_{RDHEOZ}	RDN high to EOPN output high impedance		70		60	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

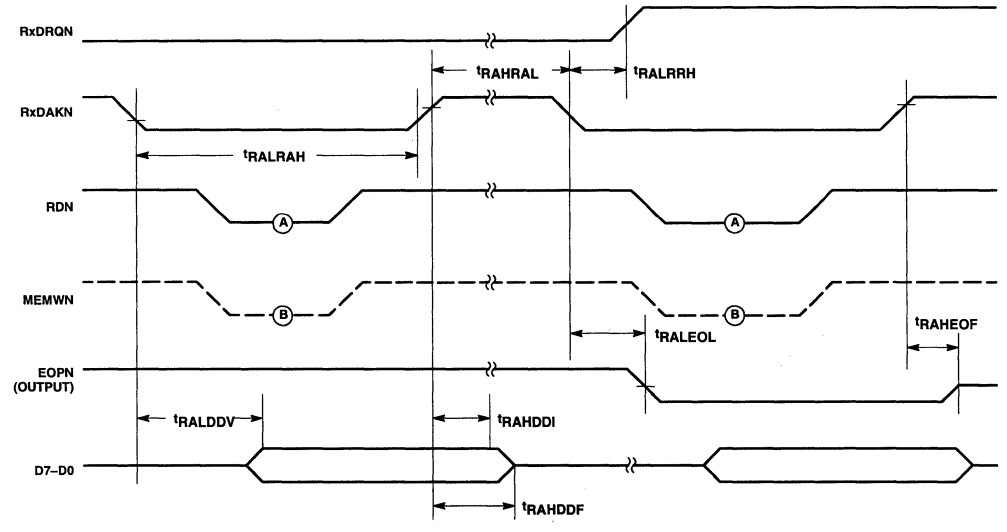


NOTES:
(A) Ignored by the CDUSCC since CEN is not asserted, but it can be used externally to qualify TxDAKN.
(B) Memory read signal; not seen by CDUSCC.

Figure 12. DMA-Transmit Single Address Mode

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{TAHTAL}	Transmit DMA ACKN high to low time	40		30		ns
t_{TALTAH}	Transmit DMA ACKN low to high time	110		100		ns
t_{TALTRH}	Tx DMA ACKN low to Tx DMA REQN high					ns
t_{WDVTAH}	Write data valid to Tx DMA ACKN high	60	110	40	100	ns
t_{TAHWDI}	Tx DMA ACKN high to write data invalid	15		10		ns
t_{TALEOL}	Tx DMA ACKN low to EOPN output low					ns
t_{TAHEOF}	Tx DMA ACKN high to EOPN output float		100		80	ns
t_{EILTAH}	EOPN input low to Tx DMA ACKN high	40	70	30	60	ns
t_{TAHEIH}	Tx DMA ACKN high to EOPN input high	30		25		ns

AC ELECTRICAL CHARACTERISTICS (Continued)



NOTES:
(A) Ignored by the CDUSCC bit; it can be used to qualify RxDAKN.
(B) Memory read signal; not seen by CDUSCC.

Figure 13. DMA-Receive Single Address Mode

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{RAHRAL}	Receive DMA ACKN high to low time	50		30		ns
t_{RALRAH}	Receive DMA ACKN low to high time	140		130		ns
t_{RALRRH}	Rx DMA ACKN low to Rx DMA REQN high		100		100	ns
t_{RALEOL}	Rx DMA ACKN low to EOPN output low		100		100	ns
t_{RAHEOF}	Rx DMA ACKN high to EOPN output float		70		60	ns
t_{RALDDV}	Rx DMA ACKN low to read data valid		140		130	ns
t_{RAHDDI}	Rx DMA ACKN high to read data invalid	5		5		ns
t_{RAHDDF}	Rx DMA ACKN high to data bus float		60		60	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

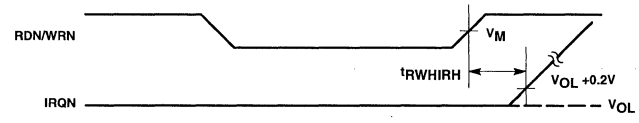


Figure 14. Interrupt Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC26C562		COMMERCIAL SC26C562		
		Min	Max	Min	Max	
t_{RWHIRH}	RDN/WRN high to IRQN high for:					
	Read RxFIFO (RxRDY interrupt)		100		90	ns
	Write TxFIFO (TxRDY interrupt)		100		90	ns
	Write RSR (Rx condition interrupt)		100		90	ns
	Write TRSR (Rx/Tx interrupt)		100		90	ns
	Write ICTSR (counter/timer interrupt)		100		90	ns
	Write TRMSR (Tx Path, Patt. Det.)		100		90	ns

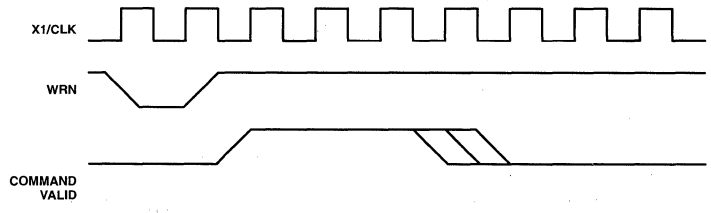


Figure 15. Command Timing

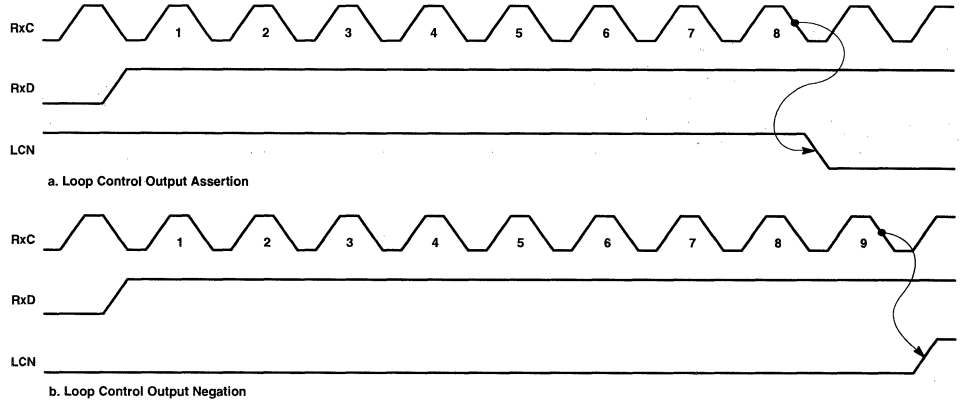
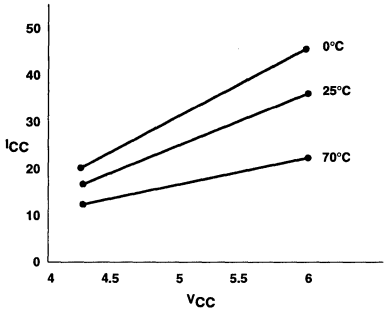
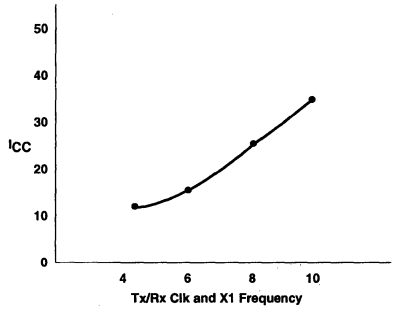


Figure 16. Relationship Between Received Data and the Loop Control Output

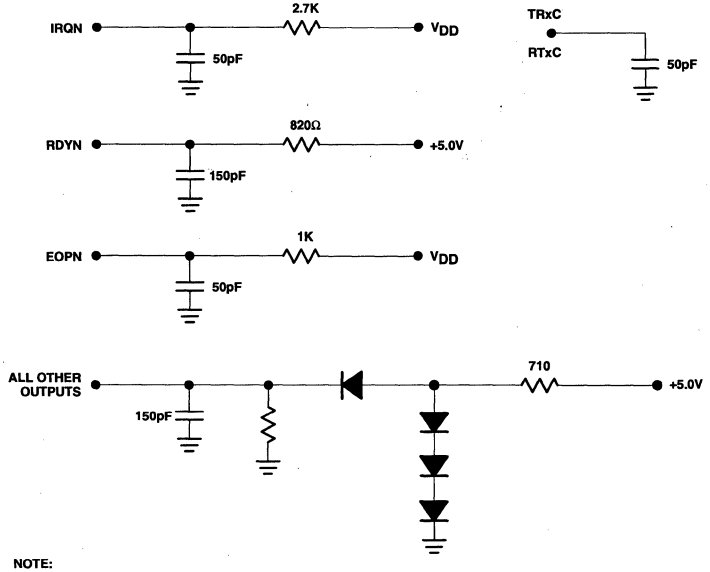


Test Condition: Tx/Rx and X1 Frequency @ 10MHz



Test Condition: V_{CC} = 5V @ 25°C

Figure 17.



NOTE:
All C_L includes 50pF stray capacitance,
i.e., C_L = 150pF = 100pF discrete +50pF stray.

Figure 18. Test Conditions for Outputs

CMOS Dual universal serial communications controller (CDUSCC) SC68C562

DESCRIPTION

The Philips Semiconductors SC68C562 Dual Universal Serial Communications Controller (CDUSCC) is a single-chip CMOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SC68C562 interfaces to the 68000 MPUs via asynchronous bus control signals and is capable of program-polled, interrupt driven, block-move or DMA data transfers.

The SC68C562 is hardware (pin) and software (Register) compatible with SCN68562 (NMOS version). It will automatically configure to NMOS DUSCC register map on power-up or reset.

The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides 16 common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock.

This makes the CDUSCC well suited for dual speed channel applications. Data rates up to 10Mb/s are supported.

Each transmitter and each receiver is serviced by a 16 byte FIFO. The receiver FIFO also stores 9 status bits for each character received; the transmit FIFO is able to store transmitter commands with each byte. This permits reading and writing of up to 16 bytes at a time, thus minimizing the

potential for transmitter underrun, receiver overrun and reducing interrupt or DMA overhead.

In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full. Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs are general purpose in nature, they can be optionally programmed for other functions. This document contains the electrical specifications for the SC68C562. Refer to the CMOS Dual Universal Serial Communications Controller (CDUSCC) User Manual for a complete operational description of this product.

FEATURES

- Full hardware and software upward compatibility with previous NMOS device

General Features

- Dual full-duplex synchronous/ asynchronous receiver and transmitter
- Low power CMOS process
- Multiprotocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: BISYNC, DDCMP
  - ASYNC: 5–8 bits plus optional parity
- Sixteen character receiver and transmitter FIFOs
- 0 to 10MHz data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 19 fixed rates: 50 to 64k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- and half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Compatible with the Philips Semiconductors SCB68430 Direct Memory Access Interface (DMAI) and other DMA controllers
  - Single- or dual-address dual transfers
  - Half- or full-duplex operation
  - Automatic frame termination on counter/timer terminal count or DMA DONE
- Transmit path clear status
- Interrupt capabilities
  - Daisy chain option
  - Vector output (fixed or modified by status)
  - Programmable internal priorities
  - Interrupt at any FIFO fill level
  - Maskable interrupt conditions
- FIFO'd status bits
- Watchdog timer
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general I/O pins per channel
  - CTS and DCD programmable auto-enables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments

CMOS Dual universal serial communications controller (CDUSCC) — SC68C562

- 1X or 16X Rx and Tx clock factors
- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search 1/2-bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmits up to 10Mb/s at 1X and receive up to 1Mb/s at 16X data rates

Character-Oriented Protocol Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK line fill on underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun, and underrun error detection

BISYNC Features

- EBCDIC or ASCII header, text and control messages
- SYN, DLE stripping
- EOM (end of message) detection and transmission
- Auto transparent mode switching
- Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
- Control character sequence detection for both transparent and normal text

Bit-Oriented Protocol Features

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for I field
- Zero insertion and deletion
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- ABORT, ABORT-FLAGs, or FCS FLAGs line fill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

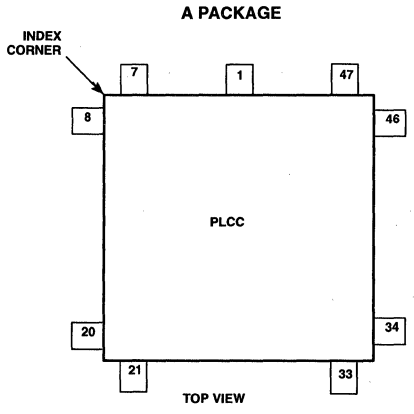
ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±10%, T_A = 0 to +70°C Serial Data Rate = 10Mbps Maximum	V_{CC} = +5V ±10%, T_A = –40 to +85°C Serial Data Rate = 8Mbps Maximum	DWG #
48-Pin Plastic Dual In-Line Package (DIP)	SC68C562C1N	Not available	0416C
52-Pin Plastic Leaded Chip Carrier (PLCC) Package	SC68C562C1A	SC68C562A8A	0397E

ABSOLUTE MAXIMUM RATINGS[1]

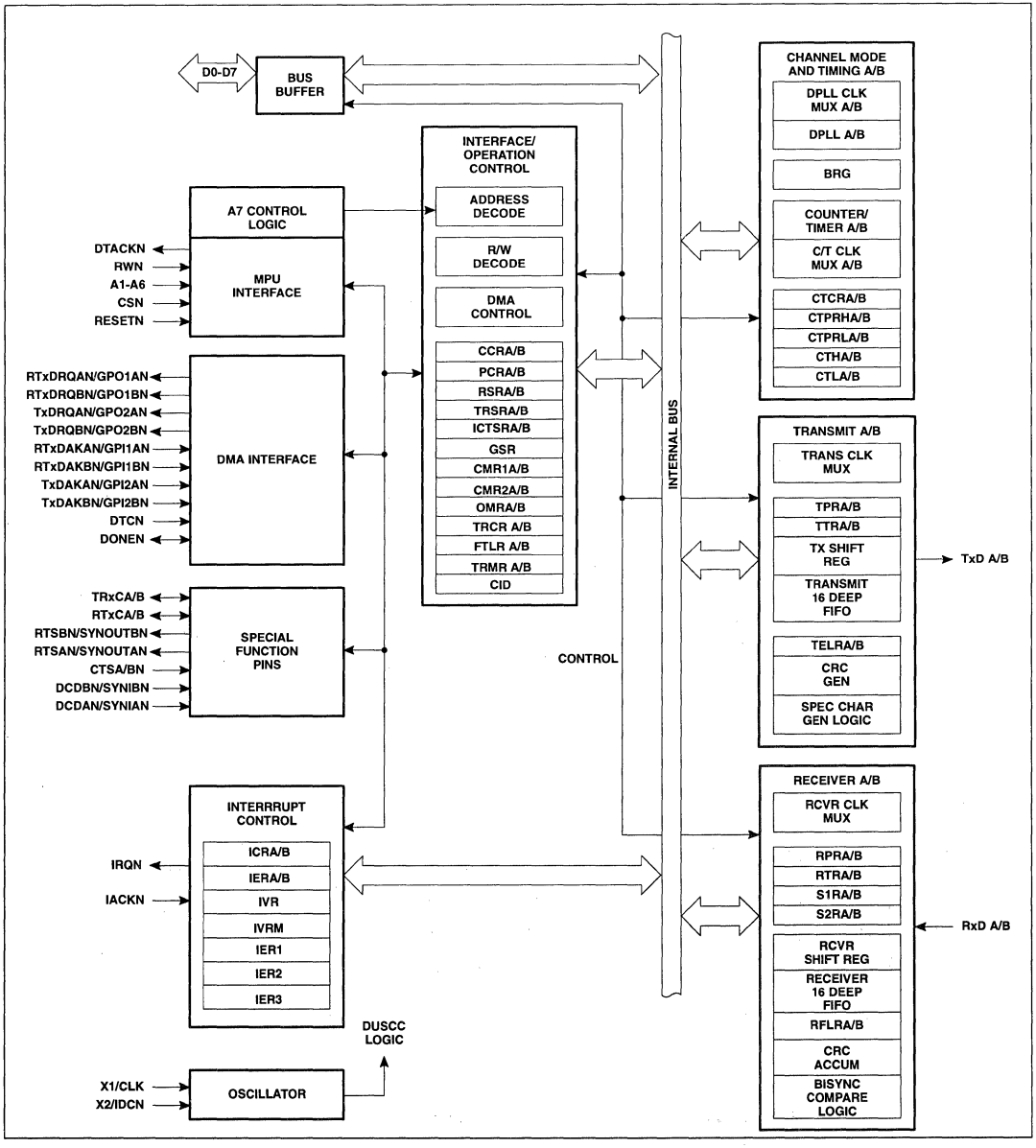
SYMBOL	PARAMETER	RATING		UNIT
		Commercial	Automotive	
T_A	Operating ambient temperature[2]	0 to +70	-40 to +85	°C
T_{STG}	Storage temperature	-65 to +150	-65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	–0.5 to +7.0	–0.5 to +7.0	V
V_S	Voltage from any pin to ground[3]	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V

PIN CONFIGURATIONS



Pin	Function	Pin	Function
1	IACKN	27	CSN
2	A3	28	R/WN
3	A2	29	DONEN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
		32	D1
6	IRQN	33	D0
7	GND	34	V_{CC}
8	RESETN	35	CTSAN/LCAN
9	RTSBN/ SYNOUTBN	36	TxDRQAN/ GPO2AN/RTSAN
10	TRxCB	37	RTxDRQAN/ GPO1AN
11	RTxCB		
12	DCDBN/ SYNIBN	38	TxDAKAN/ GPI2AN
13	GND	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	GND
16	TxDAKBN/ GPI2BN	42	DCDAN/ SYNIAN
17	RTxDRQBN/ GPO1BN	43	RTxCA
		44	TRxCA
18	TxDRQBN/ GPO2BN/RTSBN	45	RTSAN/ SYNOUTAN
19	CTSBN/LCBN	46	X2/IDCN
20	D7	47	X1/CLK
21	D6	48	RTxDAKAN/ GPI1AN
22	D5		
23	D4	49	A6
24	DTACKN	50	A5
25	DTCN	51	A4
26	GND	52	V_{CC}

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A1–A6	4-2, 47-45	4-2, 51-49	I	**Address Lines:** Active-high. Address inputs which specify which of the internal registers is accessed for read/write operation.
D0–D7	31-28, 21-18	33-30, 23-20	I/O	**Bidirectional Data Bus:** Active-high, 3-State. Bit 0 is the LSB and bit 7 is the MSB. All data, command and status transfers between the CPU and the CDUSCC take place over this bus. The data bus is enabled when CSN and R/WN or during interrupt acknowledge cycles and single address DMA acknowledge cycles.
R/WN	26	28	I	**Read/Write:** A high input indicates a read cycle and a low indicates a write cycle when CEN is active.
CSN	25	27	I	**Chip Select:** Active-low input. When active, data transfers between the CPU and the CDUSCC are enabled on D0–D7 as controlled by R/WN and A1–A6 inputs. When CSN is high, the data lines are placed in the 3-State condition (except during interrupt acknowledge cycles and single address DMA transfers).
IRQN	6	6	O	**Interrupt Request:** Active-low, open-drain. This output is asserted upon occurrence of any enabled interrupting condition. The CPU can read the general status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the CDUSCC to output an interrupt vector on the data bus.
IACKN	1	1	I	**Interrupt Acknowledge:** Active-low. When IACKN is asserted, the CDUSCC responds by either forcing the bus into high-impedance, placing a vector number, call instruction or zero on the data bus. The vector number can be modified or unmodified by the status. If no interrupt is pending, IACKN is ignored and the data bus placed in high-impedance.
X1/CLK	43	47	I	**Crystal or External Clock:** When using the crystal oscillator, the crystal is connected between pins X1 and X2. If a crystal is not used, an external clock is supplied at this input. This clock is used to drive the internal bit rate generator, as an optional input to the counter/timer or DPLL, and to provide other required clocking signals. When a crystal is used, a capacitor must be connected from this pin to ground.
X2/IDCN	42	46	O	**Crystal or Interrupt Daisy Chain:** When a crystal is used as the timing source, the crystal is connected between pins X1 and X2. This pin can be programmed to provide an interrupt daisy chain active-low output which propagates the IACKN signal to lower priority devices, if no active interrupt is pending. This pin should be left floating when an external clock is used on X1 and X2 is not used as an interrupt daisy chain output. When a crystal is used, a capacitor must be connected from this pin to ground.
RESETN	7	8	I	**Master Reset:** Active-low. A low on this pin resets the transmitters and receivers and resets the registers shown in Table 1 of the CDUSCC Users' Guide. Reset is asynchronous, i.e., no clock is required.
RxDA, RxDB	37, 12	40, 14	I	**Channel A (B) Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified for the channel, the input is sampled on the rising edge of the clock.
TxDA, TxDB	36, 13	39, 15	O	**Channel A (B) Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is in the marking (high) condition when the transmitter is disabled or when the channel is operating in local loopback mode. If external transmitter clock is specified for the channel, the data is shifted on the falling edge of the clock.
RTxCA, RTxCB	39, 10	43, 11	I/O	**Channel A (B) Receiver/Transmitter Clock:** As an input, it can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the transmitter shift clock (1X), or the receiver sampling clock (1X).
TRxCA, TRxCB	40, 9	44, 10	I/O	**Channel A (B) Transmitter/Receiver Clock:** As an input, it can supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the DPLL output, the transmitter shift clock (1X), the receiver sampling clock (1X), the transmitter BRG clock (16X), The receiver BRG clock (16X), or the internal system clock (X1 ÷ 2).
CTSA/BN, LCA/BN	32, 17	35, 19	I/O	**Channel A (B) Clear-to-Send Input or Loop Control Output:** Active-low. The signal can be programmed to act as an enable for the transmitter when not in loop mode. The CDUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. When operating in the BOP loop mode, this pin becomes a loop control output which is asserted and negated by CDUSCC commands. This output provides the means of controlling external loop interface hardware to go on-line and off-line without disturbing operation of the loop.

PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
DCDA/BN, SYNIA/BN	38, 11	42, 12	I	**Channel A (B) Data Carrier Detected or External Sync Input:** The function of this pin is programmable. As a DCD active-low input, it acts as an enable for the receiver or can be used as a general purpose input. For the DCD function, the CDUSCC detects logic level transitions on this pin and can be programmed to generate an interrupt when a transition occurs. As an active-low external sync input, it is used in COP mode to obtain character synchronization for the receiver without receipt of a SYN character. This mode can be used in disc or tape controller applications or for the optional byte timing lead in X.21.
RTxDRQA/BN, GPO1A/BN	34, 15	37, 17	O	**Channel A (B) Receiver/Transmitter DMA Service Request or General Purpose Output:** Active-low. For half-duplex DMA operation, this output indicates to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or that the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, this output indicates to the DMA controller that data is available in the receiver FIFO. In non-DMA mode, this pin is a general purpose output that can be asserted and negated under program control.
TxDRQA/BN, GPO2A/BN, RTSA/BN	33, 16	36, 18	O	**Channel A (B) Transmitter DMA Service Request, General Purpose Output, or Request-to-Send:** Active-low. For full-duplex DMA operation, this output indicates to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full-duplex DMA mode, this pin can be programmed as a general purpose or a Request-to-Send output, which can be asserted and negated under program control.
RTxDAKA/BN, GPI1A/BN	44, 5	48, 5	I	**Channel A (B) Receiver/Transmitter DMA Acknowledge or General Purpose Input:** Active-low. For half-duplex single address operation, this input indicates to the CDUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO when the receiver is enabled or load transmitter FIFO when the transmitter is enabled) is beginning. For full-duplex single address DMA operation, this input indicates to the CDUSCC that the DMA controller has acquired the bus and that the requested read receiver FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in single address DMA mode.
TxDAKA/BN, GPI2A/BN	35, 14	38, 16	I	**Channel A (B) Transmitter DMA Acknowledge or General Purpose Input:** Active-low. When the channel is programmed for full-duplex single address DMA operation, this input is asserted to indicate to the CDUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in full-duplex single address DMA mode.
DONEN	27	29	I/O	**Done:** Active-low, open-drain. DONEN can be used and is active in both DMA and non-DMA modes. As an input, DONEN indicates the last DMA transfer cycle to the TxFIFO. As an output, DONEN indicates either the last DMA transfer from the RxFIFO or that the transmitted character count has reached terminal count.
RTSA/BN, SYNOUTA/BN	41, 8	45, 9	O	**Channel A (B) Sync Detect or Request-to-Send:** Active-low. If programmed as a sync output, it is asserted one bit time after the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes) is detected by the receiver. As a Request-to-Send modem control signal, it functions as described previously for the TxDRQN/RTSN pin.
DTACKN	22	24	O	**Data Transfer Acknowledge:** Active-low, 3-state. DTACKN is asserted on a write cycle to indicate that the data on the bus has been latched, and on a read cycle or interrupt acknowledge cycle to indicate valid data is on the bus. In a write bus cycle, input data is latched by the assertion (falling edge) of DTACKN or by the negation (rising edge) of CSN, whichever occurs first. The signal is negated when completion of the cycle is indicated by negation of CSN or IACKN input, and returns to the inactive state (3-state) a short period after it is negated. In single address DMA mode, input data is latched by the assertion (falling edge) of DTCN or by the negation (rising edge) of the DMA acknowledge input, whichever occurs first. DTACK is negated when completion of the cycle is indicated by the assertion of DTCN or negation of DMA acknowledge inputs (whichever occurs first), and returns to the inactive state (3-state) a short period after it is negated. When inactive, DTACKN requires an external pull-up resistor.
DTC	23	25	I	**Device Transfer Complete:** Active-low. DTCN is asserted by the DMA controller to indicate that the requested data transfer is complete.
V_{CC}	48	34, 52	I	**+5V Power Input**
GND	24	26, 13, 41, 7	I	**Signal and Power Ground Input**

DC ELECTRICAL CHARACTERISTICS[4, 5] T_A = 0 to +70°C, V_{CC} = 5.0V ± 10%

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage:					
	All except X1/CLK				0.8	V
	X1/CLK				0.8	V
V_{IH}	Input high voltage:					
	All except X1/CLK		2.0 (Comm)			V
	X1/CLK		2.3 (Auto)			V
			0.8xV_{CC}		V_{CC}	V
V_{OL}	Output low voltage:[14]					
	All except IRQN	I_{OL} = 5.3mA (Comm), 4.8mA (Auto)			0.5	V
	IRQN[7]				0.5	V
	Output high voltage:[14]	I_{OL} = 8.8mA (Comm), 7.8mA (Auto)				
V_{OH}	(Except open drain outputs)		V_{CC}–0.5			V
		I_{OH} = -400µA				
I_{ILX1}	X1/CLK input low current[10]	V_{IN} = 0, X2 = GND	–150		0.0	µA
I_{IHX1}	X1/CLK input high current[10]	V_{IN} = V_{CC}, X2 = GND			150	µA
I_{SCX2}	X2 short circuit current (X2 mode)	X1 open V_{IN} = 0			–15	mA
		V_{IN} = V_{CC}			+15	mA
I_{IL}	Input low current RESETN, DTCN, TxDAKA/BN, RTxDAKA/BN	V_{IN} = 0	-15		–0.5	µA
I_L	Input leakage current	V_{IN} = 0 to V_{CC}	-1 (Comm) –10 (Auto)		+1 (Comm) +10 (Auto)	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			+1 (Comm) +10 (Auto)	µA µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0	-1 (Comm) –10 (Auto)			µA µA
I_{ODL}	Open drain output low current in off state: DONEN, DTACKN (3-state)	V_{IN} = 0	-15		-0.5	µA
	IRQN		-1			µA
I_{ODH}	Open drain output high current in off state: DONEN, IRQN, DTACKN (3-state)	V_{IN} = V_{CC}	–1		+1	µA
I_{CC}	Power supply current (See Figure 17 for graphs)	V_O = 0 to V_{CC}, Rx/Tx at 10MHz and X1 at 10MHz		25	80 (Comm) 95 (Auto)	mA
C_{IN}	Input capacitance[9]	V_{CC} = GND = 0			10	pF
C_{OUT}	Output capacitance[9]	V_{CC} = GND = 0			15	pF
$C_{I/O}$	Input/output capacitance[9]	V_{CC} = GND = 0			20	pF

NOTES:

1. Stresses above those listed under Abs. Max Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
2. Clock may be stopped (DC) for testing purposes or when the CDUSCC is in non-operational modes. Operation down to 0 rate clocks is implied by a full static CMOS design, but is not verified in testing or characterization.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature and voltage range.
5. All voltage measurements are referenced to ground (GND). For testing, all inputs except X1/CLK swing between 0.2V and 3.0V with a transition time of 20ns maximum. For X1/CLK, this swing is between 0.2V and 4.4V. All time measurements are referenced at input voltages of 0.2V and 3.0V and output voltages of 0.8V and 2.0V, as appropriate.
6. See Figure 18 for test conditions for outputs.
7. Tests for open drain outputs are intended to guarantee switching of the output transistor. Measurement of this response is referenced from midpoint of the switching signal to a point 0.2V above the actual output signal level. This point represents noise margin that assures that the true switching has occurred.
8. Execution of the valid command (after it is latched) requires a minimum of three rising edges of X1 (see Figure 19).
9. These values were no explicitly tested; they are guaranteed by design and characterization data.
10. X1/CLK and X2 are not tested with a crystal installed.
11. X1/CLK frequency must be at least as fast as the faster of the receiver or transmitter data rate.
12. The X1 clock is used in the timing of DTACKN, Baud Rate Generator, command register and the update of the FIFO fill level encoders. The Command Register requires three X1 clocks between two commands; FIFO fill level encoding requires 2.5 to 3.5 X1 cycles. The Baud Rate Generator is driven by the X1 clock.
13. The 68562 bus interface may be operated in two modes; a 68000 compatible mode with automatic DTACK generation and a short chip select mode. DTACKN should not be used externally in the short chip select mode. The DTACKN signal is generated by the assertion of the chip select, and data is latched by assertion of DTACKN or by de-assertion of the chip select, whichever comes first. In single address DMA, the DTACK signal will be de-asserted by the assertion of the DTCN or from the de-assertion of the TxDAKN, whichever occurs first.
14. Also includes X2/IDCN pin in IDC mode.
15. In case of 3-state output, output levels V_{OL} + 0.2 are considered float or high impedance.

Figure 1. Reset Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC68C562		COMMERCIAL SC68C562		
		Min	Max	Min	Max	
t_{RELREH}	RESETN low to RESETN high	200		200		ns

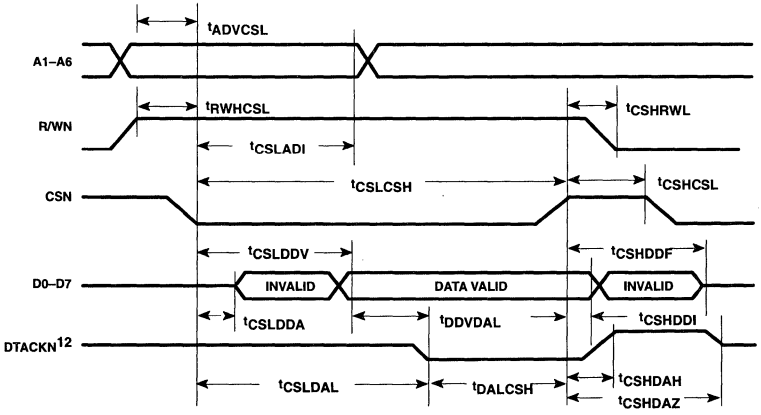


Figure 2. Read Cycle Bus Timing

Times represent an X1 clock frequency of 14.745MHz

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC68C562		COMMERCIAL SC68C562		
		Min	Max	Min	Max	
t_{ADVCSL}	A0-A6 valid to CSN low	10		5		ns
t_{RWHCSL}	RWN high to CSN low	10		5		ns
t_{CSHRWL}	CSN high to RWN low	20		10		ns
t_{CSHCSL}	CSN high to CSN low[8]	50		30		ns
t_{CSLDDV}	CSN low to read data valid		150		130	ns
t_{CSHDDF}	CSN high to data bus float		50		40	ns
t_{DDVDAL}	Read data valid to DTACKN low[9]	20		20		ns
t_{DALCSH}	DTACKN low to CSN high[9]	0		0		ns
t_{CSLDAL}	CSN low to DTACKN low[9]	$30 + \frac{1}{f_{CL}}$	$140 + \frac{1.5}{f_{CL}}$	$40 + \frac{1}{f_{CL}}$	$130 + \frac{1.5}{f_{CL}}$	ns
t_{CSHDAH}	CSN high to DTACKN high		60		60	ns
t_{CSHDAZ}	CSN high to DTACKN high impedance		90		90	ns
t_{CSLADI}	CSN low to address invalid	60		50		ns
t_{CSLCSH}	CSN low to CSN high	150		130		ns
t_{CSLDDA}	CSN low to data bus driver active[9]	5		10		ns
t_{CSHDDI}	CSN high to data invalid	5		5		ns

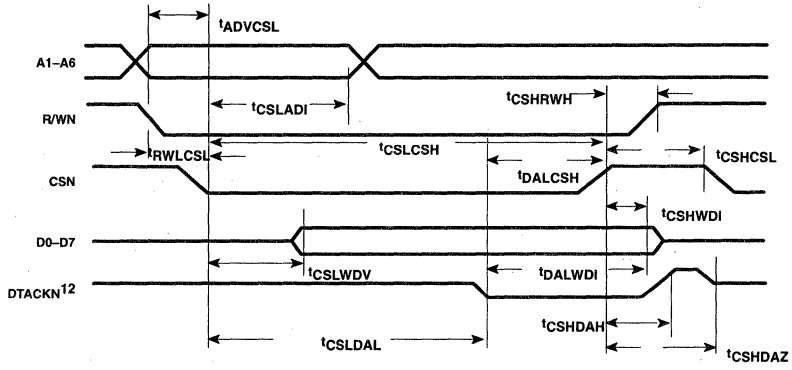


Figure 3. Write Cycle Bus Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC68C562		COMMERCIAL SC68C562		
		Min	Max	Min	Max	
t_{ADVCSL}	A0-A6 valid to CSN low	10		5		ns
t_{CSLADI}	CSN low to A0-A6 invalid	60		50		ns
t_{RWLCSL}	RWN low to CSN low	0		0		ns
t_{CSHRWH}	CSN high to RWN high	0		0		ns
t_{CSHCSL}	CSN high to CSN low[8]	50		30		ns
t_{DALCSH}	DTACKN low to CSN high[9]	0		0		ns
t_{DALWDI}	DTACKN low to write data invalid[9]	0		0		ns
t_{CSLDAL}	CSN low to DTACKN low[9]	$30 + \frac{1}{f_{CL}}$	$140 + \frac{1.5}{f_{CL}}$	$40 + \frac{1}{f_{CL}}$	$130 + \frac{1.5}{f_{CL}}$	ns
t_{CSHDAH}	CSN high to DTACKN high		60		60	ns
t_{CSHDAZ}	CSN high to DTACKN high impedance		90		90	ns
t_{CSLCSH}	CSN low to CSN high	150		130		ns
t_{CSLWDV}	CSN low to write data valid	30		35		ns
t_{CSHWDI}	CSN high to write data invalid	10		5		ns

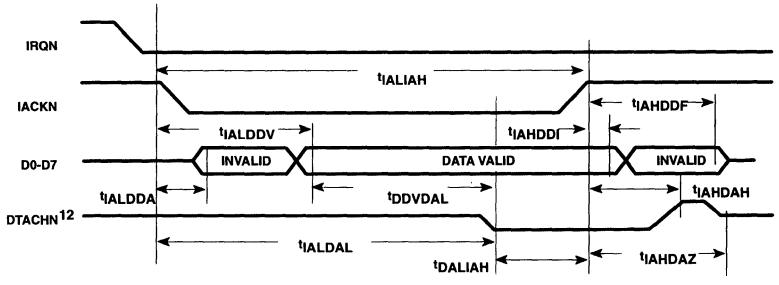


Figure 4. Interrupt Cycle Timing

SYMBOL	PARAMETER[12]	LIMITS				UNIT
		AUTOMOTIVE SC68C562		COMMERCIAL SC68C562		
		Min	Max	Min	Max	
t_{IALIAH}	IACKN low to IACKN high	140		130		ns
t_{IALDDA}	IACKN low to data bus drivers active[9]	5		10		ns
t_{IALDDV}	IACKN low to read data valid		140		130	ns
t_{IAHDDF}	IACKN high to data bus floating		60		60	ns
t_{DDVDAL}	Read data valid to DTACKN low[9]	20		20		ns
t_{IAHDAH}	IACKN high to DTACKN high		80		70	ns
t_{IAHDAZ}	IACKN high to DTACKN high impedance		110		100	ns
t_{IALDAL}	IACKN low to DTACKN low[9]	$30 + \frac{1}{f_{CL}}$	$140 + \frac{1.5}{f_{CL}}$	$40 + \frac{1}{f_{CL}}$	$130 + \frac{1.5}{f_{CL}}$	ns
t_{IAHDI}	IACKN high to data bus invalid	5		5		ns
t_{DALIAH}	DTACKN low to IACKN high[9]	0		0		ns

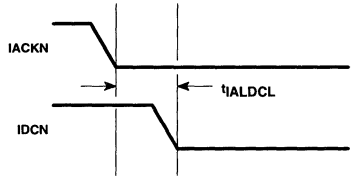


Figure 5. Interrupt Daisy Chain Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC68C562		COMMERCIAL SC68C562		
		Min	Max	Min	Max	
t_{IALDCL}	IACKN low to IDCN (daisy chain) low		70		60	ns

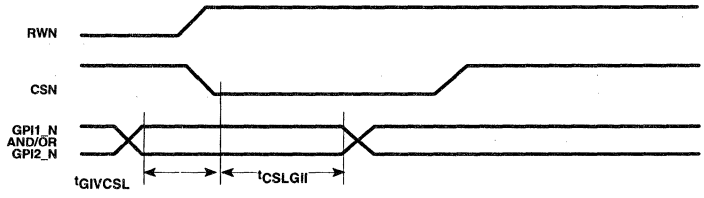


Figure 6. Input Port Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC68C562		COMMERCIAL SC68C562		
		Min	Max	Min	Max	
t_{GIVCSL}	GPI input valid to CSN low	20		20		ns
t_{CSLGII}	CSN low to GPI input invalid	40		40		ns

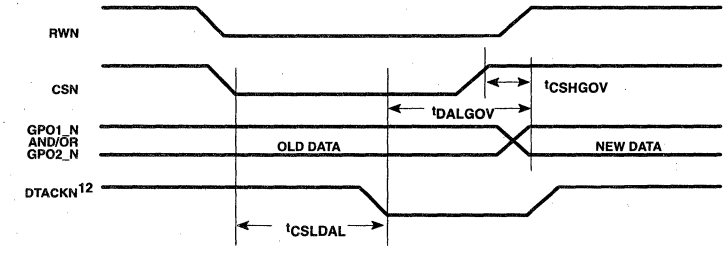


Figure 7. Output Port Timing

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC68C562		COMMERCIAL SC68C562		
		Min	Max	Min	Max	
t_{DALGOV}	DTACKN low to GPO output data valid[9]		40		40	ns
t_{CSLDAL}	CSN low to DTACKN low[9]	$30 + \frac{1}{f_{CL}}$	$140 + \frac{1.5}{f_{CL}}$	$40 + \frac{1}{f_{CL}}$	$130 + \frac{1.5}{f_{CL}}$	ns
t_{CSHGOV}	CSN high to GPO output data valid		100		100	ns

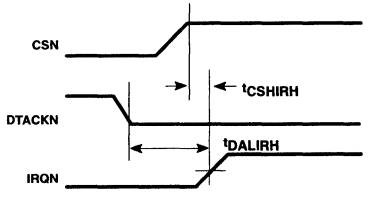


Figure 8. Interrupt Timing, Write Cycle

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC68C562		COMMERCIAL SC68C562		
		Min	Max	Min	Max	
t_{DALIRH}	DTACKN low to IRQN high, write cycle[9]					
	Write TxFIFO (TxRDY interrupt)[9]		40		40	ns
	Write RSR (Rx condition interrupt)[9]		40		40	ns
	Write TRSR (Rx/Tx interrupt)[9]		40		40	ns
	Write ICTSR (port change and CT interrupt)[9]		40		40	ns
	Write TRMSR (Tx Path, Patt recognition)[9]		40		40	ns
t_{CSHIRH}	CSN high to IRQN high, write cycle					
	Write TxFIFO (TxRDY interrupt)		100		90	ns
	Write RSR (Rx condition interrupt)		100		90	ns
	Write TRSR (Rx/Tx interrupt)		100		90	ns
	Write ICTSR (port change and CT interrupt)		100		90	ns
	Write TRMSR (Tx Path, Patt recognition)[9]		100		90	ns

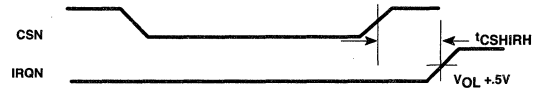


Figure 9. Interrupt Timing, Read Cycle

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC68C562		COMMERCIAL SC68C562		
		Min	Max	Min	Max	
t_{CSHIRH}	CSN high to IRQN high, read cycle					
	Read RxFIFO (RxRDY interrupt)		100		90	ns

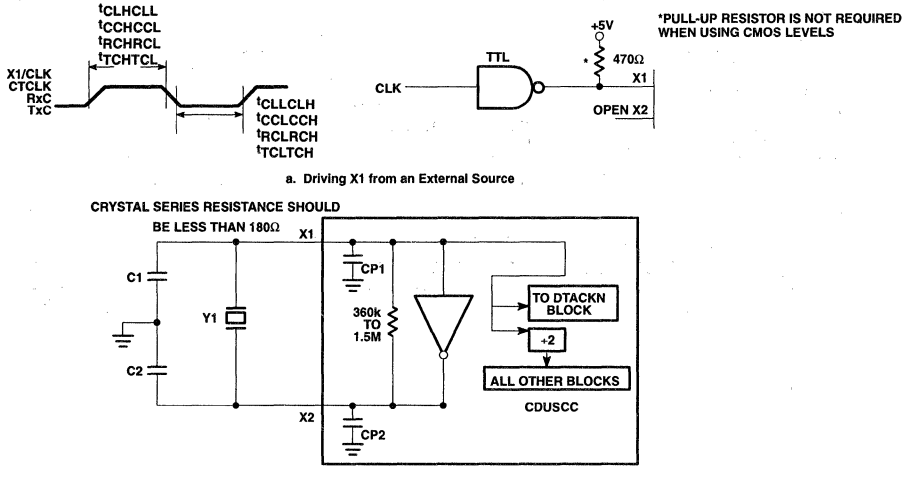
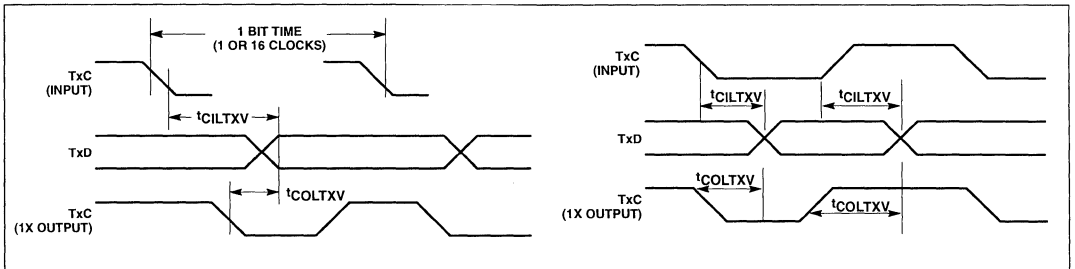


Figure 10. Receive, Dual Address DMA

SYMBOL	PARAMETER	LIMITS						UNIT
		AUTOMOTIVE SC68C562			COMMERCIAL SC68C562			
		Min	Typ	Max	Min	Typ	Max	
t_{CLHCLL}	X1/CLK high to low time	25			25			ns
t_{CLLCLH}	X1/CLK low to high time	25			25			ns
t_{CCHCCL}	CT and DPLL CLK high to low time	50			45			ns
t_{CCLCCH}	CT and DPLL CLK low to high time	50			45			ns
t_{RCHRCL}	RxC high to low time	55			50			ns
t_{RCLRCH}	RxC low to high time	55			50			ns
t_{TCHTCL}	TxC high to low time	55			50			ns
t_{TCLTCH}	TxC low to high time	55			50			ns
f_{CL}	X1/CLK frequency[11, 2]	0	14.7456	16.0	0	14.7456	16.0	MHz
f_{CC}	CT CLK frequency	0		8	0		10	MHz
f_{RC}	RxC frequency (16X or 1X)	0		8	0		10	MHz
f_{TC}	TxC frequency (16X or 1X)	0		8	0		10	MHz
f_{RTC}	Tx/Rx frequency for FM/Manchester encoding			4			5	MHz

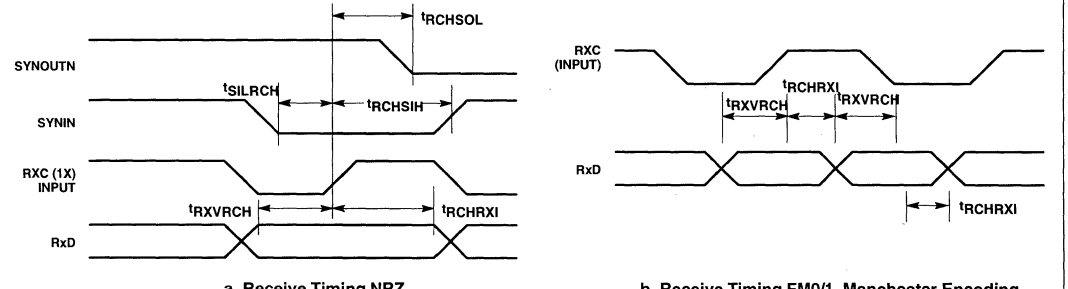


a. Transmit Timing NRZ

b. Transmit Timing FM0/1, Manchester Encoding

Figure 11.

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC68C562		COMMERCIAL SC68C562		
		Min	Max	Min	Max	
t_{CILTXV}	TxC input low (1X) to TxD output		120		120	ns
	TxC input low (16X) to TxD output		125		120	ns
t_{COLTXV}*	TxC output low to TxD output (NRZ, NRZI)[9]		25		20	ns
	(FM, Manchester)[9]		35		30	ns
NOTE: Characterized with no loads on TxD and TxC outputs.*						



a. Receive Timing NRZ

b. Receive Timing FM0/1, Manchester Encoding

Figure 12.

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC68C562		COMMERCIAL SC68C562		
		Min	Max	Min	Max	
t_{RXVRCH}	RxD data valid to RxC high:					
	For NRZ data	25		20		ns
	For NRZI, Manchester, FM0, FM1 data	30		30		ns
t_{RCHRXI}	RxC high to RxD data invalid:					
	For NRZ data	25		20		ns
	For NRZI, Manchester, FM0, FM1 data	30		30		ns
t_{SILRCH}	SYNIN low to RxC high	50		50		ns
t_{RCHSIH}	RxC high to SYNIN high	20		20		ns
t_{RCHSOL}	RxC high to SYNOUT low		110		100	ns

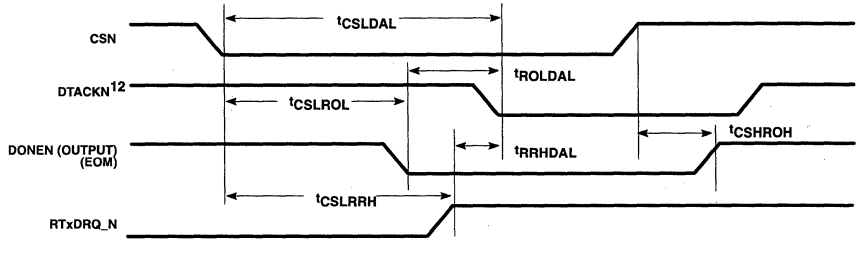


Figure 13. Receive, Dual Address DMA

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC68C562		COMMERCIAL SC68C562		
		Min	Max	Min	Max	
t_{CSLROL}	CSN low to Rx DONEN output low		110		100	ns
t_{CSLRRH}	CSN low to Rx DMA REQN high		110		100	ns
t_{CSHROH}	CSN high to Rx DONEN output high		70		60	ns
t_{ROLDAL}	Rx DONEN output low to DTACKN low[9]	40		40		ns
t_{RRHDAL}	Rx DMA REQN high to DTACKN low[9]	40		40		ns
t_{CSLDAL}	CSN low to DTACKN low[9]	$30 + \frac{1}{f_{CL}}$	$140 + \frac{1.5}{f_{CL}}$	$40 + \frac{1}{f_{CL}}$	$130 + \frac{1.5}{f_{CL}}$	ns

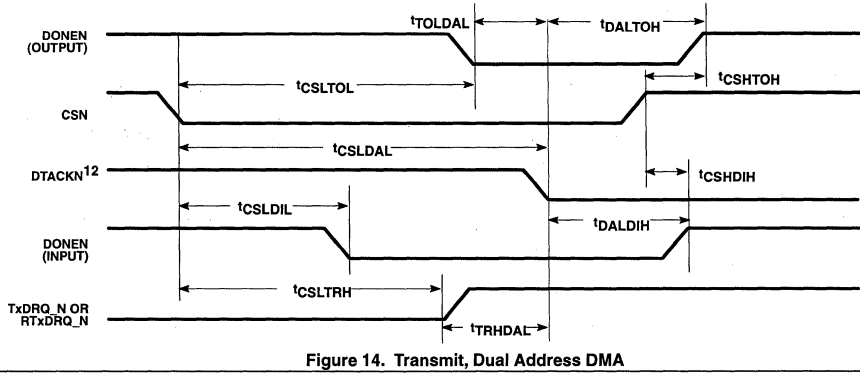


Figure 14. Transmit, Dual Address DMA

SYMBOL	PARAMETER	LIMITS		LIMITS		UNIT
		AUTOMOTIVE SC68C562		COMMERCIAL SC68C562		
		Min	Max	Min	Max	
t_{CSLTOL}	CSN low to Tx DONEN output low		110		100	ns
t_{CSLTRH}	CSN low to Tx DMA REQN high		110		100	ns
t_{DALDIH}	DTACKN low to Tx DONEN input high[9]	0		0		ns
t_{DALTOH}	DTACKN low to Tx DONEN output high[9]		20		20	ns
t_{TOLDAL}	Tx DONEN output low to DTACKN low[9]	40		40		ns
t_{TRHDAL}	Tx DMA REQN high to DTACKN low[9]	40		40		ns
t_{CSLDAL}	CSN low to DTACKN low[9]	$30 + \frac{1}{f_{CL}}$	$140 + \frac{1.5}{f_{CL}}$	$40 + \frac{1}{f_{CL}}$	$130 + \frac{1.5}{f_{CL}}$	ns
t_{CSLDIL}	CSN low to Tx DONEN input low	35		40		ns
t_{CSHTOH}	CSN high to Tx DONEN output high		70		60	ns
t_{CSHDIH}	CSN high to Tx DONEN input high	30		25		ns

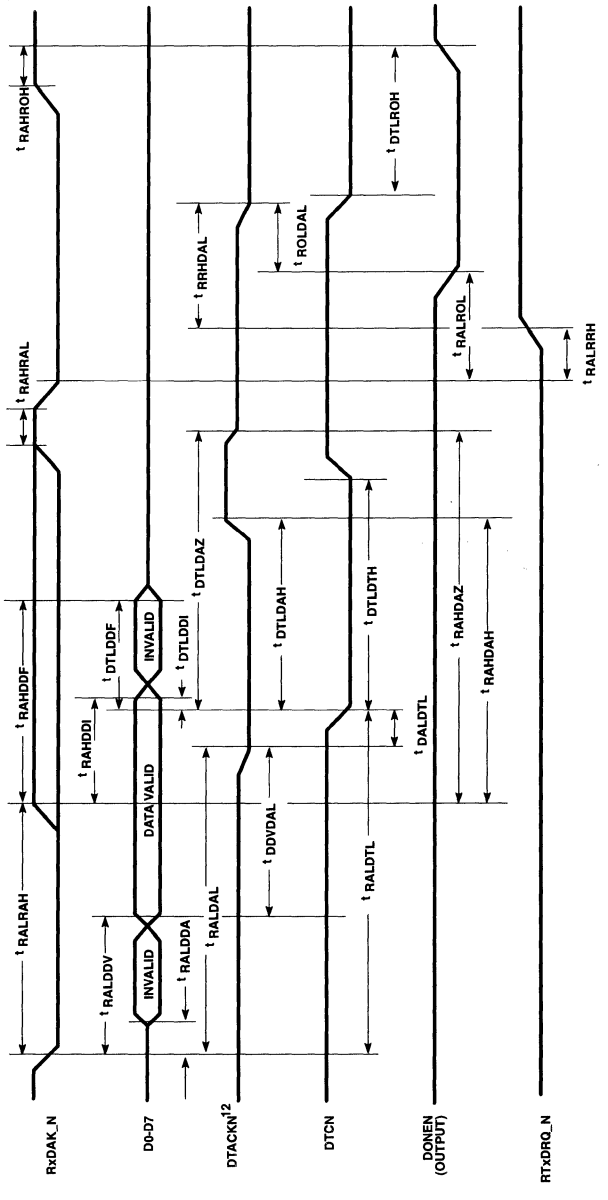


Figure 15. DMA Rx Read Timing — Single Address DMA

DMA Rx Read Timing — Single Address DMA

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC68C562		COMMERCIAL SC68C562		
		Min	Max	Min	Max	
t_{RALDDV}	Receive DMA ACKN low to read data valid		140		130	ns
t_{DTLDTH}	DTCN low to DTCN high	50		40		ns
t_{DALDTL}	DTACKN low to DTCN low[9]	0		0		ns
t_{DTLDDF}	DTCN low to data bus float		70		60	ns
t_{RALDAL}	Rx DMA ACK low to DTACKN low[9]	$30 + \frac{1}{f_{CL}}$	$140 + \frac{1.5}{f_{CL}}$	$40 + \frac{1}{f_{CL}}$	$130 + \frac{1.5}{f_{CL}}$	ns
t_{DDVDAL}	Read data valid to DTACKN low[9]	20		20		ns
t_{DTLDAH}	DTCN low to DTACKN high		80		80	ns
t_{DTLDAZ}	DTCN low to DTACKN high impedance		110		110	ns
t_{RRHDAL}	Rx DMA REQN high to DTACKN low[9]	40		40		ns
t_{ROLDAL}	Rx DONEN output low to DTACKN low[9]	40		40		ns
t_{RALRRH}	Rx DMA ACKN low to receive DMA REQN high		100		100	ns
t_{RAHRAL}	Receive DMA ACKN high to low time	50		30		ns
t_{RALROL}	Rx DMA ACK low to Rx DONEN output low		100		100	ns
t_{DTLROH}	DTCN low to Rx DONEN output high		80		70	ns
t_{RALRAH}	Rx DMA ACKN low to Rx DMA ACKN high	140		130		ns
t_{RAHDDF}	Rx DMA ACKN high to data bus float		60		60	ns
t_{RALDDA}	Rx DMA ACKN low to data bus drivers active[9]	5		10		ns
t_{RAHDDI}	Rx DMA ACKN high to data bus invalid	5		5		ns
t_{DTLDDI}	DTCN low to data bus invalid	5		5		ns
t_{RALDTL}	Rx DMA ACKN low to DTCN low	140		130		ns
t_{RAHDAH}	Rx DMA ACKN high to DTACKN high		80		70	ns
t_{RAHDAZ}	Rx DMA ACKN high to DTACKN high impedance		110		100	ns
t_{RAHROH}	Rx DMA ACKN high to DONEN output high		70		60	ns

DMA Tx Write Timing — Single Address DMA

SYMBOL	PARAMETER	LIMITS				UNIT
		AUTOMOTIVE SC68C562		COMMERCIAL SC68C562		
		Min	Max	Min	Max	
t_{DTLDTH}	DTCN low to DTCN high	50		40		ns
t_{DALDTL}	DTACKN low to DTCN low[9]	0		0		ns
t_{TALDAL}	Tx DMA ACK low to DTACKN low[9]	$30 + \frac{1}{f_{CL}}$	$140 + \frac{1.5}{f_{CL}}$	$40 + \frac{1}{f_{CL}}$	$130 + \frac{1.5}{f_{CL}}$	ns
t_{DTLDAH}	DTCN low to DTACKN high		80		80	ns
t_{DTLDAZ}	DTCN low to DTACKN high impedance		110		110	ns
t_{TRHDAL}	Tx DMA REQN high to DTACKN low[9]	40		40		ns
t_{TOLDAL}	Tx DONEN output low to DTACKN low[9]	40		40		ns
t_{DTLTOH}	DTCN low to Tx DONEN output high		80		70	ns
t_{WDVDTL}	Write data valid to DTCN low	40		40		ns
t_{DTLWDI}	DTCN low to write data invalid	30		20		ns
t_{TALTRH}	Tx DMA ACKN low to transmit DMA REQN high		110		100	ns
t_{TAHTAL}	Transmit DMA ACKN high to low time	40		30		ns
t_{TALTOL}	Tx DMA ACKN low to Tx DONEN output low		100		90	ns
t_{DILDTL}	Transmit DONEN input low to DTCN low	40		30		ns
t_{DTLDIH}	DTCN low to transmit DONEN input high	40		30		ns
t_{TALTAH}	Tx ACKN low to Tx ACKN high	110		100		ns
t_{TAHWDI}	Tx ACKN high to write data invalid	15		10		ns
t_{WDVTAH}	Write data valid to Tx DAKN high	60		40		ns
t_{TAHDAH}	Tx DAKN high to DTACKN high		80		70	ns
t_{TAHDAZ}	Tx DAKN high to DTACKN high impedance		110		100	ns
t_{TAHTOH}	Tx DAKN high to DONEN output high		70		60	ns
t_{DILTAH}	DONEN input low to Tx DAKN high	40		30		ns
t_{TAHDIH}	Tx DAKN high to DONEN input high	30		25		ns
t_{TALDTL}	Tx DAKN low to DTCN low	110		100		ns

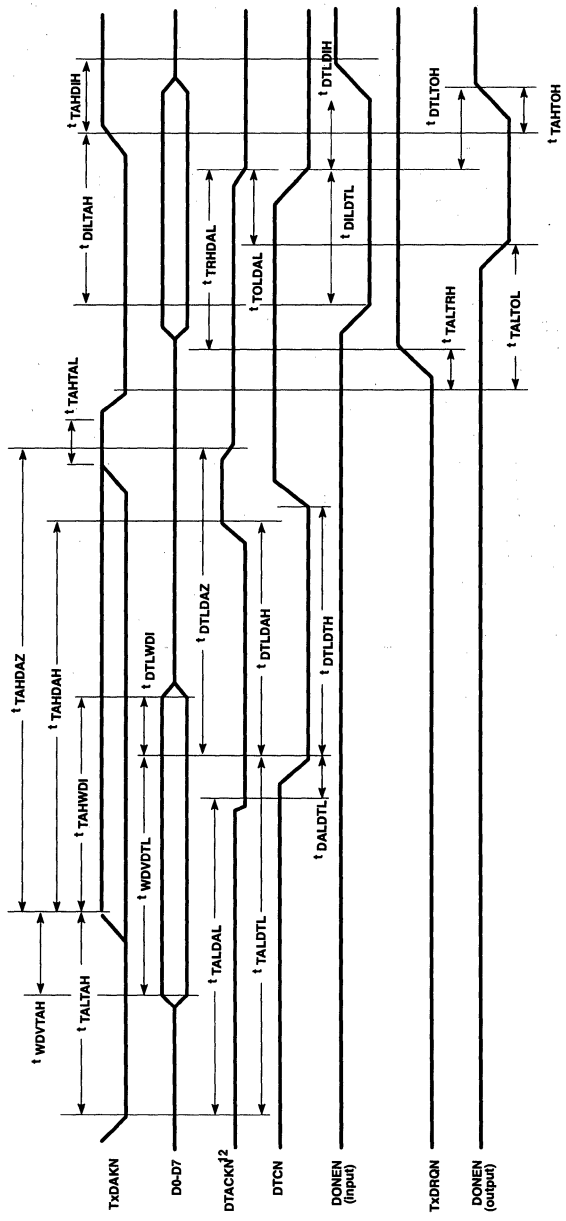
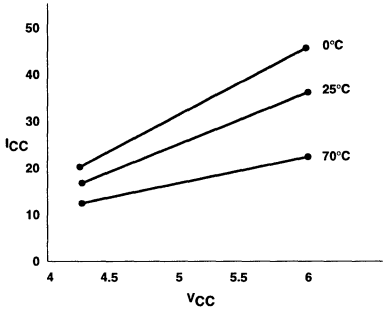
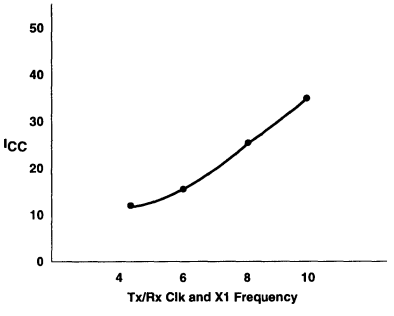


Figure 16. DMA Tx Write Timing — Single Address DMA

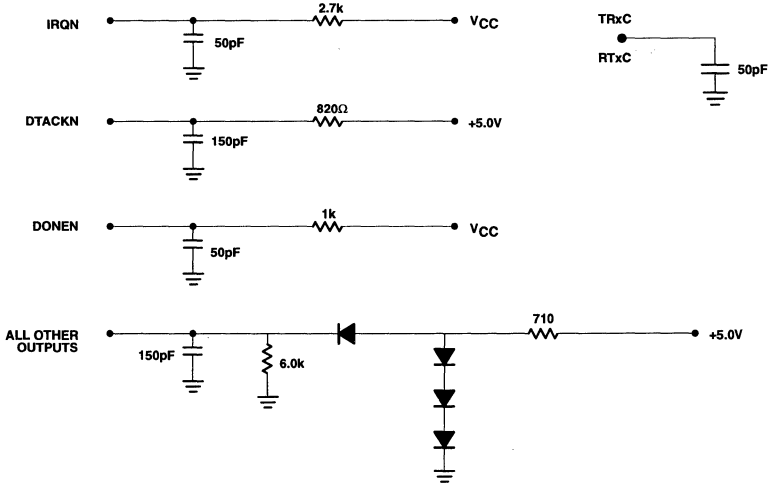


Test Condition: Tx/Rx and X1 Frequency @ 10MHz



Test Condition: V_{CC} = 5V @ 25°C

Figure 17.



NOTE:
All C_L includes 50pF stray capacitance, i.e., C_L = 150pF = (100pF discrete + 50pF stray).

Figure 18. Test Conditions for Outputs

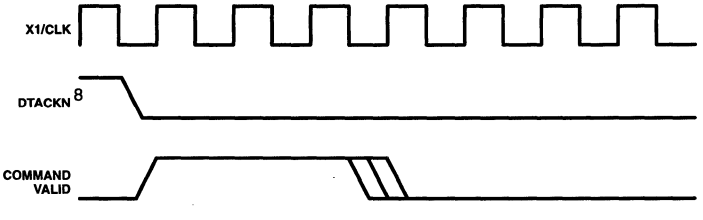


Figure 19. Command Timing

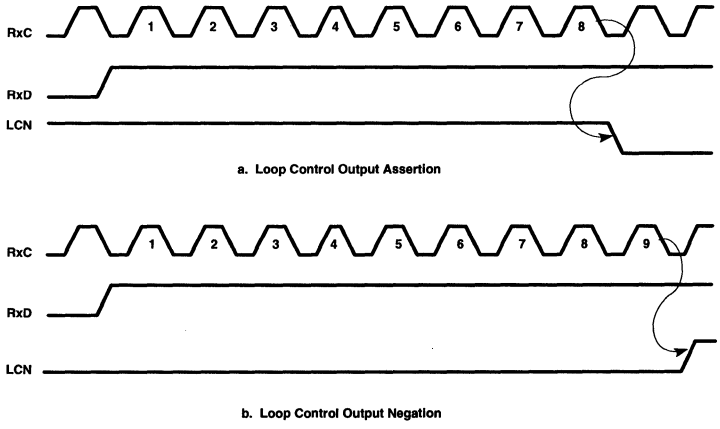


Figure 20. Relationship Between Received Data and the Loop Control Output

User notes for the SCN68/26562 (NDUSCC) and SC68/26C562 (CDUSCC)

AN416

Revised by: A. Kazmi

BISYNC Protocol Questions and Answers

This is a list of some questions and answers for the DUSCC/CDUSCC using BISYNC protocol.

Question:

What is the recommended way for ending a transmit operation?

Answer:

The way to end the transmit operation is to:

– CCR = H' 06' ; TEOM after next character

– Put H'03' into Tx FIFO ; Send ETX
– Put H 'FF' into Tx FIFO ; **Optional** Transmit trailing pad

Now you need to disable TxRDY from interrupting by writing to IER register.

Question:

When is TRSR[7] (TxUnderrun) set at the end of frame?

Answer:

Refer to the Transmitter data path in the data sheet. The status bit TRSR[7] is set when the Tx shift register is empty and no other characters (from the TxFIFO special char. or Sync char.) are waiting to fill it. There can be a one bit time delay due to the Data Encoder after the Tx SR is empty and before the last bit of the character is seen on the TxD pin. The TEOM command causes the FCS to be sent after the next character put into the Tx FIFO is sent. The CRC generation takes place after the Tx SR, so TRSR[7] will be set after the FIFOed character is serialized but before FCS is sent. Another status bit, Frame Complete, TRSR[5] is set when transmission of the FCS begins.

Question:

Are SYN's in the Tx FIFO excluded from Tx BCC accumulation without using 'Exclude from CRC' command (normal mode)?

Answer:

YES.

Question:

Are DLE & SYN in the Tx FIFO excluded from Tx BCC accumulation without using 'exclude from CRC' command while in transparent mode?

Answer:

No, not if they are in the FIFO. If DLE is transmitted by TDLE command in the command register, it won't be accumulated because it won't go through the FIFO. Any/all characters transmitted through the FIFO in transparent mode will be included in the CRC accumulation. If you don't want one accumulated, use the 'exclude from CRC' command before sending it, or if it is at beginning of frame, use the 'reset CRC' command after sending it.

Question:

For BISYNC DMA transfer, is there any way to automatically insert SYNs?

Answer:

One way would be to:

– Program Tx to underrun with SYN s (TPR[7:6] = 11)

– Count down characters to when you want SYN stop the DMA and let the DUSCC Tx underrun

– Start the DMA again after sufficient time to let the DUSCC transmit the SYN

Using this method would preclude using the Tx underrun (TPR[7:6]) to do anything else like underrun with FCS-idle for automatic EOM.

Question:

How could I insert ONLY ONE DLE-SYN in text (in transparent mode)?

Answer:

If you're not in DMA mode at the point where you want the single DLE-SYN:

– Transmit DLE command (CCR=H'08')

– Exclude from CRC command (CCR=H'0D')

– Put SYN character into FIFO

– Proceed with transmitting data characters

If you re using a DMA:

– Program Tx to underrun with SYN s (TPR[7:6] = 11)

– Count down characters (with DMA) to when you want SYN stop the DMA interrupt CPU with DMA let the DUSCC/CDUSCC Tx underrun.

– CPU sets up DMA polls DUSCC/CDUSCC TRSR register and waits for bit 7, Tx empty to get set. The CPU starts DMA again.

This will give at least one DLE-SYN. If CPU is polling TRSR before bit 7 gets set, you will get ONLY ONE DLE-SYN. If the DUSCC/CDUSCC underruns before the CPU is polling for this condition, you may get more than one.

Question:

Does the DUSCC/CDUSCC set the parity bit for ASCII data?

Answer:

The DUSCC/CDUSCC requires that 'no parity' be programmed in the CMR1 register and it really doesn't implement parity. Programming CMR1 [5] = 1 selects that the DUSCC/CDUSCC use its 7-bit odd–parity ASCII look–up table for special character transmission and for reception compares. The CPU must present the DUSCC/CDUSCC with 8-bit data 7 bits plus odd-parity. This requires that the look-up table the CPU uses for the ASCII characters have all 8 bits instead of just 7.

Question:

Does the DUSCC/CDUSCC still receive characters when the BCC check results in a CRC error (after 'ITB' received)?

Answer:

Yes.

User notes for the SCN68/26562 (NDUSCC) and SC68/26C562 (CDUSCC)

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Question:

What exactly does RPR[7] SYN stripping do while in transparent data mode?

Answer:

A first clarification is that when RPR[7]=0 and you are in BISYNC transparent mode, all odd DLEs are not included in BCC calculation, but are sent through to the Rx FIFO. In BISYNC transparent mode when RPR[7]=1, all odd DLEs will also be stripped so they do not go into the Rx FIFO. Also all occurrences of SYN1 preceded by an odd DLE will be stripped.

In BISYNC normal mode or COP dual SYN mode RPR[7]=1 will enable stripping for all occurrences of SYN1 – SYN2. In single SYN COP mode RPR[7]=1 will enable stripping of all occurrences of SYN1.

Leading SYN patterns (DLE–SYN1 SYN1–SYN2 or SYN1 as appropriate) are always stripped for all modes.

EXAMPLE: Tx Transparent Mode in BISYNC

Assume the part is initialized as follows:

```
INIT:
    CMR1=05H    ;COP BISYNC MODE, EBCDIC
    CMR2=3FH    ;POLLED/INT MODE, NORMAL, CCIT PRESET 1'S
    TTR=3FH     ;38.4K BAUD
    RTR=6FH     ;38.4K BAUD
    TPR=E3H     ;8 BIT CHAR, UNDERRUN = SYNS, IDLE = SYNS
    RPR=83H     ;8 BIT CHAR, STRIP SYN NO FCS TO FIFO OR HUNT
    OMR=F7H     ;TXRDY=EMTY, RXRDY=NOT EMPTY, NO RESID CHAR
    S1R=66H     ;FIRST SYNC CHAR.=HEX 66
    S2R=99H     ;SECOND SYNC CHAR.= HEX 99
    CCR=00H     ;RESET TX
    CCR=40H     ;RESET RX
    CCR=02H     ;ENABLE TX
    CCR=42H     ;ENABLE RX
```

Then to start a transparent frame:

```
    TXFIFO=55H  ;Put leading pad into TxFIFO, if needed
    CCR=05H     ;transmit SOM with PAD command
    TRSR[4]=1 ? ;wait for SOM ACK to be set
    CCR=08H     ;transmit DLE before next character command
    TXFIFO=02H  ;transmit STX
    CCR=01H     ;Reset Tx CRC
```

Now transmit block of transparent data...(can be done with interrupts). Then, to end a transparent frame:

```
    CCR=08H     ;transmit DLE before next character command
    CCR=006H    ;transmit EOM at end of next character command
    TXFIFO=03H  ;transmit ETX
    TXFIFO=FFH  ;transmit trailing PAD, if needed
```

Now, do something to keep the transmitter from interrupting until you want to start the next message... (if transmission was interrupt driven)
The receiver will receive: 10 02...XX XX XX...03 (DLE STX ... DATA DATA DATA...ETX) in the receiver FIFO.

User notes for the SCN68/26562 (NDUSCC) and SC68/26C562 (CDUSCC)

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BISYNC TRANSMISSION

Transmit SOM Sequences for Transparent Mode:

(a) SYN1–SYN2–DLE–STX

- Transmit SOM command CCR=04H
- Exclude from CRC command CCR=0DH
- Put DLE into TxFIFO TxFIFO=10H
- Exclude from CRC command CCR=0DH
- Put STX into TxFIFO TxFIFO=02H

–or–

- Transmit SOM command CCR=04H
- Transmit DLE command CCR=08H
- Put STX into TxFIFO TxFIFO=02H
- Reset Tx CRC command CCR=01H

(b) PAD–SYN1–SYN2–DLE–STX

- Put leading pad into TxFIFO TxFIFO=55H
- Transmit SOM w/pad command CCR=05H
- Wait for SOM ACK set TRSR[4]=1 ?
- Transmit DLE command CCR=08H
- Put STX into TxFIFO TxFIFO=02H
- Reset Tx CRC command CCR=01H

Transmit EOM for Transparent Mode:

DLE–ETX–CRC–CRC–(PAD)

- Transmit DLE command CCR_=008H
- Transmit EOM command CCR_=06H
- Put ETX into TxFIFO TxFIFO=03H
- (optional) Put closing pad into TxFIFO TxFIFO=FFH

Transmit SOM Sequences for Non–Transparent Mode:

(a) SYN1–SYN2–STX

- Transmit SOM command CCR=04H
- Exclude from CRC command CCR=0DH
- Put STX into TxFIFO TxFIFO=02H

(b) PAD–SYN1–SYN2–STX

- Put leading PAD into TxFIFO TxFIFO=55H
- Transmit SOM w/PAD command CCR=05H
- Wait for SOM ACK set TRSR[4]=1 ?
- Exclude from CRC command CCR=0DH
- Put STX into TxFIFO TxFIFO=02H

DLE–SYN Insertion for Transparent Mode:

DLE–SYN1

(a) Not in DMA mode
At point where you want it inserted:

- Transmit DLE command CCR_=08H
- Exclude from CRC command CCR_=0DH
- Put SYN1 into TxFIFO TxFIFO=66H

Proceed on with data transmission (b) In DMA mode

(b) In DMA mode

- Underrun with SYN's programmed at initialization TPR[7:6]=11
- Can use a counter (in DMA or CDUSCC) to time out when you want SYN's
- When counter times out, let the transmitter underrun
- Start transmitting after sufficient time to let the CDUSCC transmit the DLE SYN. You can wait for TRSR[7] = 1 (TxEMPTY) as an indicator of enough time.
- Will get at least one DLE–SYN

Transmit EOM Sequences for Non–Transparent Mode:

ETX–CRC–CRC–(PAD)

(a) Not in DMA mode

- Transmit EOM command CCR=06H
- Put ETX into TxFIFO TxFIFO=03H
- (optional) Put closing pad into TxFIFO TxFIFO=FFH

(b) In DMA mode

- TEOM on zero count or done programmed at initialization TPR[4]=1
- Have ETX as last character in Tx buffer, assert DONEN signal when ETX is written to the CDUSCC

–or–

- If you have programmed to count transmitted characters, program TPR[4] as above,
- ETX should be last character in Tx buffer
- Loading ETX to TxFIFO causes count to go to zero

–or–

- Underrun with FCS–idle programmed at initialization TPR[7:6]=00
- Have ETX as last character in Tx buffer, put into TxFIFO, let Tx underrun.

User notes for the SCN68/26562 (NDUSCC) and SC68/26C562 (CDUSCC)

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SYN Insertion for Non–Transparent Mode:

SYN1–SYN2

(a) Not in DMA mode

- Put SYN1 into TxFIFO — TxFIFO=66H
- Put SYN2 into TxFIFO — TxFIFO=99H

(b) In DMA mode

- Underrun with SYN's programmed at initialization, TPR[7:6]=11
- You can use a counter (in DMA or CDUSCC) to time out when you want SYN's
- When counter times out, let the transmitter underrun
- Start transmitting after sufficient time to let the CDUSCC transmit the SYN1–SYN2. You can wait for TRSR[7]=1 (Tx Underrun) as an indicator of enough time.
- You will get at least one SYN1–SYN2

BISYNC PROTOCOL WITH DMA

This is an abbreviated flow of the control necessary for BISYNC message transmission and reception under DMA control.

Header Field Transmission Under DMA Control

CPU => Initialization: 1 sec. transmit time-out => Counter
CPU => Initialization: TXU SYN, TEOM on DONE => CDUSCC
CPU => SOH character => Buffer
CPU => Header characters => Buffer
CPU => ETB character => Buffer
CPU => Initialization: TX Buffer address & message length => DMAC
CPU => TXRST => CDUSCC
CPU => ENTX => CDUSCC
CPU => Pad characters => CDUSCC
CPU => Enable TSOM ACK int. => CDUSCC
CPU => TSOM with PAD => CDUSCC
DUSCC =>Int: TSOM ACK => CPU
CPU => Disable TSOM ACK int. => CDUSCC
CPU => EX CRC => CDUSCC
CPU => Enable => DMAC
Buffer => SOH character => CDUSCC
Buffer => Header characters => CDUSCC
Counter =>Int: 1 sec. transmit timeout => CPU
CPU => Disable => DMAC
CPU => Clear TXU status => CDUSCC
CPU => Enable TXU int. => CDUSCC
DUSCC =>DUSCC => Int: TXU => CPU
CPU => Disable TXU int. => CDUSCC
CPU => Enable => DMAC
Buffer => Header characters => CDUSCC

Header Field Terminated Normally:

DMAC => DONE=> CDUSCC
Buffer => ETB character => CDUSCC
DMAC => Int: Count exhausted => CPU
CPU => Disable => DMAC
CPU => Pad character => CDUSCC
CPU => DISTX => CDUSCC
CPU => Initialization: 3 sec. receive timeout => Counter
CPU => Enable SYN detect int. => CDUSCC

Header Field Terminated Prematurely:

CPU => Disable => DMAC
CPU => ENQ character => CDUSCC
CPU => DISTX => CDUSCC
CPU => Initialization: 3 sec. receive timeout => Counter
CPU => Enable SYN detect int. => CDUSCC

Header Field Reception Under DMA Control

CPU => Initialization: RX SYN strip, No FCS to FIFO => CDUSCC
CPU => Initialization: RX Buffer address => DMAC
CPU => Enable => DMAC
CPU => RXRST => CDUSCC
CPU => ENRX => CDUSCC
DUSCC =>Int: SYN detect => CPU
CPU => Clear receive timeout => Counter
DUSCC =>SOH character => Buffer
DUSCC =>Header characters => Buffer
DUSCC =>Int: SYN detect => CPU
CPU => Clear receive timeout => Counter

Header Field Terminated Normally:

DUSCC =>ETB character => Buffer
DUSCC =>DONE => DMAC
DMAC => Int: Frame finished => CPU
DUSCC =>Int: PAD or CRC error => CPU
CPU => DISRX => CDUSCC
CPU => Disable => DMAC

Header Field Terminated Prematurely:

DUSCC =>Int: REOM on ENQ character => CPU
CPU => DISRX => CDUSCC
CPU => Disable => DMAC

Text Field Transmission Under DMA Control

CPU => Initialization: 1 sec. transmit timeout => Counter
CPU => Initialization: TXU SYN, no TEOM on DONE => CDUSCC
CPU => Text characters => Buffer
CPU => Initialization: TX Buffer address & message length => DMAC
CPU => TXRST => CDUSCC
CPU => ENTX => CDUSCC

CPU => Pad characters => CDUSCC
CPU => TSOM with PAD => CDUSCC
CPU => Enable TSOM ACK int. => CDUSCC
DUSCC =>Int: TSOM ACK => CPU
CPU => Disable TSOM ACK int. => CDUSCC
CPU => DLE character => CDUSCC
CPU => STX character => CDUSCC
CPU => RST TX CRC => CDUSCC
CPU => Enable => DMAC
Buffer => Text characters => CDUSCC
Counter =>Int: 1 sec. transmit timeout => CPU
CPU => Disable => DMAC
CPU => Clear TXU status => CDUSCC
CPU => Enable TXU int. => CDUSCC
DUSCC =>Int: TXU => CPU
CPU => Disable TXU int. => CDUSCC
CPU => Enable => DMAC
Buffer => Text characters => CDUSCC
DMAC =>Int: Count exhausted => CPU
CPU => Disable => DMAC
CPU => TDLE => CDUSCC
CPU => TEOM => CDUSCC
CPU => ETX character => CDUSCC
CPU => Pad character => CDUSCC
CPU => DISTX => CDUSCC
CPU => Initialization: 3 sec. receive timeout => Counter
CPU => Enable SYN detect int. => CDUSCC

Text Field Reception Under DMA Control

RX SYN strip, No FCS to FIFO => CDUSCC
CPU => Initialization: RX Buffer address => DMAC
CPU => Enable => DMAC
CPU => RXRST => CDUSCC
CPU => ENRX => CDUSCC
DUSCC =>Int: SYN detect => CPU
CPU => Clear receive timeout => Counter
DUSCC =>DLE character => Buffer
DUSCC =>STX character => Buffer
DUSCC =>Text characters => Buffer
DUSCC =>Int: SYN detect => CPU
CPU => Clear receive timeout => Counter
DUSCC =>ETX character => Buffer
DUSCC =>DONE => DMAC
DMAC => Int: Frame finished => CPU
DUSCC =>Int: PAD or CRC error => CPU
CPU => DISRX => CDUSCC
CPU => Disable => DMAC

Control Field Transmission

CPU => Initialization: 1 sec. transmit timeout => Counter
CPU => Initialization: TXU SYN, no TEOM on DONE => CDUSCC
CPU => TXRST => CDUSCC
CPU => ENTX => CDUSCC
CPU => Pad characters => CDUSCC
CPU => TSOM with PAD => CDUSCC
CPU => Enable TSOM ACK int. => CDUSCC
DUSCC =>Int: TSOM ACK => CPU
CPU => Disable TSOM ACK int. => CDUSCC
CPU => Control characters => CDUSCC
Counter =>Int: 1 sec. transmit timeout => CPU
CPU => Clear TXU status => CDUSCC
CPU => Enable TXU int. => CDUSCC
DUSCC =>Int: TXU => CPU
CPU => Disable TXU int. => CDUSCC
CPU => Control characters => CDUSCC
CPU => Pad characters => CDUSCC
CPU => DISTX => CDUSCC
CPU => Initialization: 3 sec. receive timeout => Counter
CPU => Enable SYN detect int. => CDUSCC

Control Field Reception

CPU => Initialization: RX SYN strip, No FCS to FIFO => CDUSCC
CPU => RXRST => CDUSCC
CPU => ENRX => CDUSCC
DUSCC =>Int: SYN detect => CPU
CPU => Clear receive timeout => Counter
DUSCC =>Control characters => Buffer
DUSCC =>Int: REOM on control character terminator => CPU
DUSCC =>Int: PAD error => CPU
CPU => DISRX => CDUSCC;

```
;INTERRUPT DRIVEN, TRANSPARENT MODE BISYNC EXAMPLE
;
;THIS IS PROGRAM BISYNC_INT. IT RUNS WITH AN APPLICATIONS 68K
;BOARD, THE DUSCC BENCH BOARD, AND CH A EXT. CONNECTED TO CH B,
;
;D. IBARRA JAN. 1988
          BEGIN
OMRA      EQU       $74017        ;OUTPUT & MISC. A & B
OMRB      EQU       $74057
CMR1A     EQU       $74001        ;CHAN MODE REGS
CMR1B     EQU       $74041
CMR2A     EQU       $74003
CMR2B     EQU       $74043
S1RA      EQU       $74005        ;SYN1
S1RB      EQU       $74045
S2RA      EQU       $74007        ;SYN2
S2RB      EQU       $74047
TPRA      EQU       $74009
TTRA      EQU       $740OB        ;TXA PARAMETER
TPRB      EQU       $74049        ;TXA TIMING
TTRB      EQU       $7404B
RPRA      EQU       $740OD
RTRA      EQU       $7400F
RPRB      EQU       $7404D        ;RXB PARAMETER
RTRB      EQU       $7404F        ;RXB TIMING
GSR       EQU       $74037        ;GENERAL STATUS REG
CCRA      EQU       $7401F        ;CHAN COMMAND REG A & B
CCRB      EQU       $7405F
TXFIFA    EQU       $74021        ;TXA FIFO
TXFIFB    EQU       $74061
RXFIFA    EQU       $74029
RXFIFB    EQU       $74069        ;RXB FIFO
PCRA      EQU       $7401D
PCRB      EQU       $7405D
TRSRA     EQU       $74033        ;TX/RX STATUS REG
TRSRB     EQU       $74073
RSRA      EQU       $74031
RSRB      EQU       $74071
IVR       EQU       $7403D
IVRM      EQU       $7407D
ICR       EQU       $7403F
IERA      EQU       $74039
IERB      EQU       $74079
;
START:    BSR       INIT          ;INITIALIZE DUSCC
          BSR       SETINT        ;SET UP INTERRUPTS
          LEA       TXBUF,A1      ;TX BUFFER POINTER
          LEA       RXBUF,A2      ;RX BUFFER POINTER
          MOVE.B    #$C3,CCRA     ;SET NRZ MODE FOR DPLL
          MOVE.B    #$C3,CCRB     ;SET NRZ MODE FOR DPLL
          MOVE.B    #$C0,CCRB     ;ENTER SEARCH MODE (DPLL)
          BSR       STFRM         ;TRANSMIT START OF TRNSP. FRAME
          MOVE.B    #$40,IERA     ;ENABLE TX A INT.
          MOVE.B    #$10,IERB     ;ENABLE RX B INT.
;
WT        STOP      #$2000        ;SUPERVISOR MODE,ANY INT,NO TRAP
          JMP       WT            ;
```

```
;
;——————————INITIALIZATION ROUTINES——————————
;
;INIT:       MOVE.B    #5,CMR1A        ;COP BISYNC MODE, EBCDIC
             MOVE.B    #5,CMR1B        ;COP BISYNC MODE, EBCDIC
             MOVE.B    #$3F,CMR2A      ;POLLED/INT MODE, NORMAL, CCIT PRESET 1'S
             MOVE.B    #$3F,CMR2B      ;POLLED/INT MODE, NORMAL, CCIT PRESET 1'S
             MOVE.B    #$3F,TTRA       ;38.4K BAUD
             MOVE.B    #$3F,TTRB       ;38.4K BAUD
             MOVE.B    #$6F,RTRA       ;38.4K BAUD
             MOVE.B    #$6F,RTRB       ;38.4K BAUD
             MOVE.B    #$E3,TPRA       ;TX=8 BIT/CHAR, UNDERRUN=SYNS, IDLE=SYNS
             MOVE.B    #$E3,TPRB       ;TX=8 BIT/CHAR, UNDERRUN=SYNS, IDLE=SYNS
             MOVE.B    #$83,RPRA       ;RX=8 BIT/CHAR,STRIP SYN
             MOVE.B    #$83,RPRB       ;RX=8 BIT/CHAR,STRIP SYN
             MOVE.B    #$E7,OMRA       ;TXRDY=NOT FULL, RXRDY=NOT EMPTY, NO RESID CHAR
             MOVE.B    #$E7,OMRB       ;TXRDY=NOT FULL, RXRDY=NOT EMPTY, NO RESID CHAR
             MOVE.B    #$66,S1RA       ;FIRST SYNC CHAR.=HEX 66
             MOVE.B    #$66,S1RB       ;FIRST SYNC CHAR.=HEX 66
             MOVE.B    #$99,S2RA       ;SECOND SYNC CHAR.=HEX 99
             MOVE.B    #$99,S2RB       ;SECOND SYNC CHAR.=HEX 99
             MOVE.B    #0,CCRA         ;RESET TX A
             MOVE.B    #0,CCRB         ;RESET TX B
             MOVE.B    #$40,CCRA       ;RESET RX A
             MOVE.B    #$40,CCRB       ;RESET RX B
             MOVE.B    #2,CCRA         ;ENABLE TX A
             MOVE.B    #2,CCRB         ;ENABLE TX B
             MOVE.B    #$42,CCRA       ;ENABLE RX A
             MOVE.B    #$42,CCRB       ;ENABLE RX B
             RTS
;
SETINT:      MOVEA.L   $110,A6         ;GET ADDRESS AT VECTOR 68
             MOVE.L    #RXB,2[A6]      ;RXB INT. ROUTINE ADD. TO JUMP INST.
             MOVEA.L   $104,A6         ;GET ADDRESS AT VECTOR 65
             MOVE.L    #TDBUF,2[A6]    ;TDBUF INT. ROUTINE ADD. TO JUMP INST.
             MOVE.B    #64,IVR         ;INT. VECTOR V64 INTO DUSCC
             MOVE.B    #$C7,ICR        ;INTRLVD, B PRTY, A&B ENBL, VECT. INC. STATUS
             RTS
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;; TRANSMIT ROUTINES ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
;SEQ. TO START TRANSPARENT DATA FRAME
;
STFRM:       MOVE.B    #$55,TXFIFA     ;PUT LEADING PAD INTO TXFIFA
             MOVE.B    #$05,CCRA       ;TRANSMIT SOM WITH PAD
WTSOM        MOVE.B    TRSRA,D5        ;READ STATUS
             BTST      #4,D5           ;IS SOM ACK SET?
             BEQ       WTSOM           ;IF NOT, WAIT 'TILL IT IS
             MOVE.B    #$08,CCRA       ;TRANSMIT DLE BEFORE NEXT CHAR.
             MOVE.B    #$02,TXFIFA     ;TRANSMIT STX
             MOVE.B    #$01,CCRA       ;RESET TX CRC
             RTS
;
;TRANSMIT FROM DATA BUFFER, INTERRUPT ROUTINE
;
TDBUF:       MOVE.B    [A1]+,TXFIFA    ;SEND NEXT CHAR.
             CMPA.L    #RXBUF,A1       ;AT END OF CHAR. BUFFER?
             BEQ       ETFRM           ;IF LAST CHAR, END FRAME
             RTE
```

```
;
;SEQ. TO END TRANSPARENT DATA FRAME
;
ETFRM:      BSR WTXRDY                ;WAIT FOR TXRDY
            MOVE.B      #$08,CCRA     ;TRANSMIT DLE BEFORE NEXT CHARACTER
            MOVE.B      #$06,CCRA     ;TRANSMIT EOM AT END OF NEXT CHARACTER
            MOVE.B      #$03,TXFIFA   ;TRANSMIT ETX
;
;-----------CAN'T DO YET, BECAUSE OF ANOMALY---------------------------
;           BSR         WTXRDY        ;WAIT FOR TXRDY                       ;
;           MOVE.B      #$FF,TXFIFA   ;TRANSMIT TRAILING PAD                ;
;---------------------------------------------------------------------;
;THIS WILL KEEP TX FROM INTERRUPTING UNTIL WANT TO START NEXT MESSAGE
;
RSTRDY:     MOVE.B      #$85,ICR      ;TURN OFF CH A INTERRUPT
;
;-----------CAN'T DO YET, BECAUSE OF ANOMALY---------------------------
            RSTRDY:     BSR WTXRDY    ;WAIT FOR TXRDY                       ;
;           MOVE.B      #$02,GSR      ;RESET TXRDY BIT                      ;
;---------------------------------------------------------------------
            RTE
;
;THIS SUBROUTINE WAITS FOR TXRDY
;
WTXRDY:     MOVE.B      GSR,D0        ;READ GSR TO D0
            BTST        #1,D0         ;IS TXRDY A SET ?
            BEQ         WTXRDY        ;IF NOT, WAIT TILL IT IS
            RTS
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;; RX READY INTERRUPT ROUTINE ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
RXB:        MOVE.B      RSRB,D3       ;READ RECEIVER STATUS REG.
            MOVE.B      TRSRB,D4      ;READ TX/RX STATUS REG.
            MOVE.B      TRSRA,D2      ;TEMP. READ OF TX STATUS
            BTST        #5,D3         ;OVERRUN ERROR ?
            BNE         RXERR         ;IF YES, GO TO ERROR HANDLER
            BTST        #7,D3         ;EOM DETECT ?
            BNE         RXEND         ;IF YES, GO TO RECEIVED END
            MOVE.B      RXFIFB, [A2]+ ;READ CHAR. TO BUFFER
            RTE
;
RXEND:      BTST        #1,D3         ;CRC ERROR ?
            BNE         RXERR         ;IF YES, GO TO ERROR HANDLER
            MOVE.B      RXFIFB, [A2]+ ;READ CHAR. TO BUFFER
            TRAP        #15           ;STOP AND DISPLAY STATUS
;
RXERR:      TRAP        #15           ;CRC ERROR ?
            BNE         RXERR         ;IF YES, GO TO ERROR HANDLER
            MOVE.B      RXFIFB, [A2]+ ;READ CHAR. TO BUFFER
            TRAP        #15           ;STOP AND DISPLAY STATUS
;
RXERR:      TRAP        #15           ;STOP AND DISPLAY STATUS
;
;-------------------- DATA BUFFERS ---------------------
;
TDBUF:      DC.B        0,1,2,3,4,5,6,7,8,9,10
RXBUF       DS.B        15
;
            END START
```

User notes for the SCN68/26562 (NDUSCC) and SC68/26C562 (CDUSCC)

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HANDLING DDCMP IN THE DUSCC/CDUSCC RECEIVER

There are two operations that require special handling:

1. The text field character count is contained in the header field and must be loaded in the counter/timer before the text field begins.
2. In non-BISYNC COP, the CRC error status bit (RSR[1]) is updated every time a character is loaded in the receive FIFO. The CRC accumulates to the proper value only during the last byte of the CRC, so all other characters are appended with a CRC error. RSR[1] does not clear after each character so it must be reset by the CPU after the first byte of the CRC to accurately reflect the CRC status of the second byte of CRC.

The following can be done to perform these functions:

1. The counter timer counts the number of characters in the header field. The second and third bytes of this field contain the text field character count. When this value is received it is loaded into the counter timer preset register so that when the counter reaches zero at the end of the header field it will be loaded with the text field character count.
2. It is important to know when the first byte of the CRC is at the top of the FIFO, because RSR[1] must be reset by the CPU before the second byte of the CRC is at the top of the FIFO. Therefore, load the counter timer with a count which is one less than the length of the frame so an interrupt will occur when the first byte of CRC is at the top of the FIFO.

The following sequence illustrates how a typical DDCMP frame can be handled in the receiver:

– Initialize for DDCMP protocol.

– Set Receive characters as C/T clock source, CTCR[2:O] = 1 1 0.

– Load the C/T with a count which is one less than the length of header field so that Char. Count Complete indicator, RSR[7], will be set when the first byte of CRC is at the top of the FIFO.

– Enable receiver

– Start C/T

– Start receiving header field characters. As soon as text field character count is received, load it into the C/T (CTPRH/L registers). This will not affect the current count in progress. It will be loaded by C/T when current count is complete.

– Continue receiving header field characters, look for RSR[1] to be set (Char. Count Complete indicator) before reading each character from FIFO.

– When RSR[7l is set, CRC1 byte is at the top of the FIFO. Before reading CRC1 from FIFO, clear RSR[1] (CRC error) and RSR[7]. Read CRC1 from FIFO.

– CRC2 is now at the top of FIFO. RSR[1] will now correctly indicate whether the header has had a CRC error.

– Read CRC2 from FIFO

– Char. Count Complete, RSR[7], can generate an interrupt by setting IER[3] (enable interrupt for RSR[7:6]), and setting the master interrupt enable in ICR.

BOP PROTOCOL QUESTIONS AND ANSWERS

Question:

Using the DUSCC/CDUSCC in BOP mode, you would like the DUSCC/CDUSCC transmitter to negate RTS when done with a frame, but if you have back-to-back frames, you don't want it to negate until after the last frame.

Answer:

Should have no problem with this. During the initialization program TPR[3] = 1, the transmitter controls RTS. When you first enable the transmitter, you need to manually assert RTS by writing to OMR. Disable the transmitter after loading the last character into the FIFO, and RTS will negate five bit times after transmission of the last bit of the closing FLAG. If the transmitter is re-enabled for transmission of a subsequent frame before the five bit time delay has elapsed, RTS will not negate.

Question:

You want to transmit a break in between transmission of data characters; also you want data character, break, mark, and then data again to go out on the line. What is the best way to do this? Can data characters be left in the TxFIFO while you transmit the break?

Answer:

Data cannot be left in the TxFIFO when you give the Rx BREAK command. Invoking the Transmit BREAK command will cause the transmitter FIFO to be flushed. A data character in the Tx Shift Register will still be transmitted after you give the Tx BREAK command before the BREAK is transmitted.

The transmitter looks at the state of Tx enabled or disabled at the character boundary when it is done sending the break. If it is disabled, it goes to mark; if it is enabled, it will send another break. The TxFIFO is actually flushed when the Tx BREAK ACK is set to indicate the BREAK has started transmission. So, you need to know when the BREAK is done before having the Tx re-enabled. A good way to know when it is done is to ask for a second BREAK, and when you get the BREAK ACK for it, we know the first one has gone out. Then, we need to do a Tx RESET to kill it, since a quick disable/enable will be seen as enable at the second end of BREAK boundary. Tx RESET will immediately bring the Tx output pin high and the second break will be ignored. So, the recommended sequence is to:

– Wait for GSR[7]=1, TxRDY (with OMR[4] = 1, TxRDY = FIFOEMTY)

– Issue Tx BREAK command, CCR=H'07'

– Wait for TRSR[4]=1, Tx BREAK ACK set

– Write '1' to TRSR[4]

– Issue Tx BREAK command, CCR=H'07'

– Wait for TRSR[4]=1

– Issue Tx RESET command, CCR=H'00'

– Issue Tx ENABLE command, CCR=H'02'

– Put data into Tx FIFO

Output of Tx will look like:

– DATA – BREAK – MARK – DATA –

Question:
Can the sequence 'TxABORT–TSOM–Data to FIFO' be done in this sequence with no problems? What is the best way to transmit ABORT and continue on with next frame?

Answer:
Invoking the Tx ABORT command will flush any characters in the TxFIFO, as mentioned above. This is done right before the Tx ABORT is sent out, so you don't want to do the exact sequence in the question. The TSOM command can be invoked as soon as TRSR[4], ABORT ACK, is set. New data characters can be loaded into the Tx FIFO one bit time after TRSR[4] is set. This one bit time is needed because the internal command to clear the Tx FIFO is asserted when the ACK is set, and it lasts one bit time. So, the sequence should be:

– Tx ABORT command

– Wait for TRSR[4]=1, ABORT ACK set

– TSOM command

– Delay, if needed, to have one bit time delay

– New data char. into Tx FIFO

Question:
I'm not getting my last character transmitted in my interrupt routine after TEOM is set.

Answer:
If you had residual character length set at the default value (OMR[7:5]–000) of 1 bit. So, the Tx sent out 1 bit of the last character. The solution is to program the residual character length to be same as the Tx character length (OMR[7:5] – 111).

Question:
At slower speeds, I see a time difference in getting EOM and Flag detect interrupts. Aren't these caused by the same event? Why the time difference?

Answer:
In BOP mode, receiving the closing Flag does indicate the end of frame. When the receiver detects the closing flag, it uses the 16 bits it received prior as the CRC, and appends EOM detect indicator to the last character in the FIFO (this is usually the last character in the information field, but if CRC is sent to FIFO, this will be appended to the last byte of CRC). Now, as far as the RSR bits are concerned, the Flag detect bit will always be set first. This is because the Flag detect is set as soon as the Flag is received. The EOM detect bit is set when the last character reaches the top of the FIFO, which always happens at least two bit times after Flag detect is set (longer if CRC is sent to FIFO or FIFO has previous characters still in it).

Question:
Customer is using SDLC protocol, they want to send an abort sequence followed by a 2 byte preframe before the normal frame. How is the preframe sent?

Answer:
To send the preframe they need to do the following after sending their abort sequence:

– Load the 2 characters they want to use for the preframe into the TxFIFO

– Transmit start of message with pad, CCRA[7,0] – 00XX0101

– After start of message has been sent, load TxFIFO with the message. You can check for this by polling TRSR[4] until it sets.

Question:
What is a way to get the TxD output continuously '0' for the call sequence?

Answer:
There are two ways to do this, one uses only software and the other needs external hardware. The software implementation is to put all zero characters into the TxFIFO and use the transmit start of message with PAD command (TSOMP). Be sure to keep the TxFIFO full of zero characters for as long as the continuous zero is needed. The other way is to use the GPO output on the DUSCC to control whether TxD or '0' is output on the data line. The hardware would implement TxD ANDed with GPO to get TxD. When GPO is negated (high) the Tx Data will go through, when GPO is asserted (low) the Tx Data line will be continuously low.

Question:
How can the transmitter be synchronized with an external sync. signal to implement transmitter byte timing?

Answer:
There is no way internal to the DUSCC to synchronize the transmitter with an external sync. signal. The 'External Sync Input' cannot be used for the transmitter. The transmitter byte timing synchronization would need to be done external to the chip. This would require a fair amount of external hardware to implement (estimate at least 3 packages). The transmitter byte timing requirement is fill option in the X.21 spec., some countries have standards which use this and others don't.

```
; INTERRUPT DRIVEN, BOP PROTOCOL EXAMPLE
; THIS IS PROGRAM BOP_INT.
; CHA SENDS AND RECEIVES CHARACTERS IN BOP
; USING INTERRUPT ROUTINES.
; CHA RX AND TX EXTERNALLY TIED
;
; D. IBARRA AUG., 1987, UPDATED DEC. 1988
;
                    BEGIN

OMRA        EQU     $74017      ;OUTPUT & MISC. A & B
OMRB        EQU     $74057
CMR1A       EQU     $74001      ;CHAN MODE REGS
CMR1B       EQU     $74041
CMR2A       EQU     $74003
CMR2B       EQU     $74043
TPRA        EQU     $74009      ;TXA PARAMETER
TTRA        EQU     $7400B      ;TXA TIMING
TPRB        EQU     $74049
TTRB        EQU     $7404B
RPRA        EQU     $7400D
RTRA        EQU     $7400F
RPRB        EQU     $7404D      ;RXB PARAMETER
RTRB        EQU     $7404F      ;RXB TIMING
GSR         EQU     $74037      ;GENERAL STATUS REG
CCRA        EQU     $7401F      ;CHAN COMMAND REG A & B
CCRB        EQU     $7405F
S1RA        EQU     $74005      ;SECONDARY ADDRESS REGISTER
TXFIFA      EQU     $74021      ;TXA FIFO
TXFIFB      EQU     $74061
RXFIFA      EQU     $74029
RXFIFB      EQU     $74069      ;RXB FIFO
PCRA        EQU     $7401D
PCRB        EQU     $7405D
RSRA        EQU     $74031
TRSRA       EQU     $74033      ;TX/RX STATUS REG
IERA        EQU     $74039
IVR         EQU     $7403D
ICR         EQU     $7403F
;
START:      BSR     INIT        ;INITIALIZE PART
            BSR     SETINT      ;SET UP INTERRUPTS
            LEA     TXBUF,A1    ;TX BUFFER POINTER
            LEA     RXBUF,A2    ;RX BUFFER POINTER
            MOVE.B  #$C2,CCRA   ;MANCHESTER
            MOVE.B  #$C0,CCRA   ;DPLL ENTER SEARCH MODE
            MOVE.B  #$04,CCRA   ;TSOM
            MOVE.B  #$01,CCRA   ;RESET TX CRC
            MOVE.B  #$50,IERA   ;ENABLE TXRDY AND RXRDY INT.
;
WTDN:       STOP    #$2000      ;WAIT FOR INTERRUPT ROUTINES TO END PROGRAM
            JMP     WTDN        ;
```

```
;------------------------------------------------------------------------
;--------------------------SUBROUTINES-----------------------------------
;------------------------------------------------------------------------
INIT:      MOVE.B    #$00,CCRA        ;RESET TX
           MOVE.B    #$40,CCRA        ;RESET RX
           MOVE.B    #$00,CMR1A       ;8-BIT ADD., BOP PRIMARY
           MOVE.B    #$3F,CMR2A       ;NORMAL, POLLED/INT.
           MOVE.B    #$06,PCRA        ;TXC ON TRXC
           MOVE.B    #$23,TPRA        ;UNDRN=FCS=FLAG–IDLE,IDLE=FLAGS, 8 BITS
           MOVE.B    #$23,RPRA        ;OVRN=CONTINUE FRAME, 8 BITS
           MOVE.B    #$3D,TTRA        ;TXC=BRG 9600 BAUD
           MOVE.B    #$6D,RTRA        ;RXC=DPLL, 9600 BAUD FROM BRG
           MOVE.B    #$E0,OMRA        ;TXRDY=NOT FULL, RXRDY=NOT EMPTY
           MOVE.B    #$00,CCRA        ;RESET TX
           MOVE.B    #$40,CCRA        ;RESET RX
           MOVE.B    #$02,CCRA        ;ENABLE TX
           MOVE.B    #$42,CCRA        ;ENABLE RX
           RTS
;
SETINT:    MOVE.L    #RXINT,$100      ;RX INT. ROUTINE ADD. TO VECTOR 64
           MOVE.L    #TXINT,$104      ;TX INT. ROUTINE ADD. TO VECTOR 65
           MOVE.B    #64,IVR          ;INT. VECTOR 64 INTO DUSCC
           MOVE.B    #$06,ICR         ;CHA ENABLE, VECTOR INC. STATUS
           RTS
           MOVE.B    #$C7,ICR         ;INTRLVD, B PRTY, A&B ENBL, VECT. INC. STATUS
           RTS
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;INTERRUPT ROUTINES;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
TXINT:     SUBA.L    #1,A1            ;DECREMENT TX BUFFER POINTER
           CMPA.L    #RXBUF,A1        ;LAST CHAR ?
           BNE       SEND             ;IF NOT, SEND NEXT CHAR
           MOVE.B    #$06,CCRA        ;TEOM
           MOVE.B    A1,TXFIFA        ;SEND LAST CHAR.
           MOVE.B    #$10,IERA        ;INT. ON RXRDY ONLY
           MOVE.B    #$03,CCRA        ;DISABLE TX
           RTE
SEND:      MOVE.B    [A1],TXFIFA      ;SEND NEXT CHAR.
           RTE
;
RXINT:     MOVE.B    RSRA,D3          ;RECEIVER STATUS TO D3
           MOVE.B    TRSRA,D4         ;TX/RX STATUS TO D4
           BTST      #7,D3            ;EOM DETECT?
           BNE       RXEND            ;IF YES, GO TO RECEIVED END
           MOVE.B    RXFIFA,[A2]+     ;READ CHAR. TO BUFFER
           RTE
;
RXEND:     MOVE.B    RXFIFA,,[A2]+    ;READ CHARACTER TO BUFFER
           TRAP      #15              ;STOP AND DISPLAY STATUS
;
;--------------------------DATA BUFFERS----------------------------------
TXBUF      DC.B      0,1,2,3,4,5,6,7,8,9,10
RXBUF      DS.B      15
;
           END       START
```

User notes for the SCN68/26562 (NDUSCC) and SC68/26C562 (CDUSCC)

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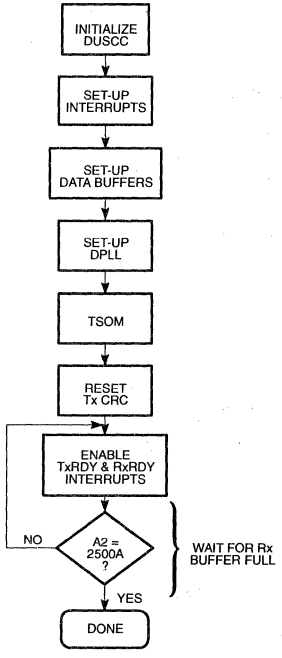
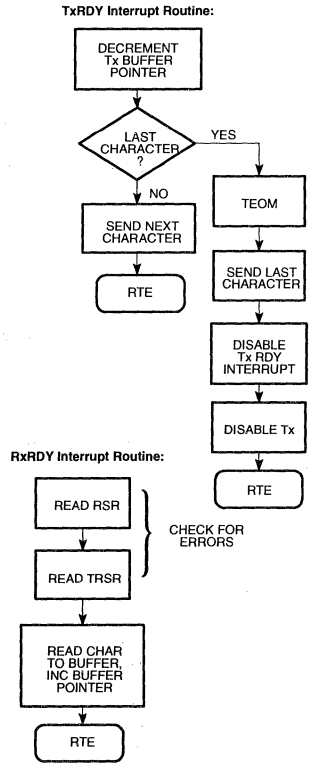


DUSCC_BOP_INT, Main Program Flow Chart



DUSCC_BOP INT TxRDY and RxRDY Flow Chart

```
; INTERRUPT DRIVEN, ASYNCHRONOUS PROTOCOL EXAMPLE
; THIS IS PROGRAM ASYNC INT. IT RUNS WITH AN APPLICATIONS 68K
; BOARD, THE DUSCC BENCH BOARD, AND CH A EXT. CONNECTED TO CH. B
;
; D. IBARRA NOV. 1988
;
                    BEGIN

OMRA        EQU     $74017      ;OUTPUT & MISC. A & B
OMRB        EQU     $74057
CMR1A       EQU     $74001      ;CHAN MODE REGS
CMR1B       EQU     $74041
CMR2A       EQU     $74003
CMR2B       EQU     $74043
S1RA        EQU     $74005      ;SYN1
S1RB        EQU     $74045
S2RA        EQU     $74007      ;SYN2
S2RB        EQU     $74047
TPRA        EQU     $74009      ;TXA PARAMETER
TTRA        EQU     $7400B      ;TXA TIMING
TPRB        EQU     $74049
TTRB        EQU     $7404B
RPRA        EQU     $7400D
RTRA        EQU     $7400F
RPRB        EQU     $7404D      ;RXB PARAMETER
RTRB        EQU     $7404F      ;RXB TIMING
GSR         EQU     $74037      ;GENERAL STATUS REG
CCRA        EQU     $7401F      ;CHAN COMMAND REG A & B
CCRB        EQU     $7405F
TXFIFA      EQU     $74021      ;TXA FIFO
TXFIFB      EQU     $74061
RXFIFA      EQU     $74029
RXFIFB      EQU     $74069      ;RXB FIFO
PCRA        EQU     $7401D
PCRB        EQU     $7405D
TRSRA       EQU     $74033      ;TX/RX STATUS REG
TRSRB       EQU     $74073
RSRA        EQU     $74031
RSRB        EQU     $74071
IVR         EQU     $7403D
IVRM        EQU     $7407D
ICR         EQU     $7403F
IERA        EQU     $74039
IERB        EQU     $74079
;
START:      BSR     INIT        ;INITIALIZE DUSCC
            BSR     SETINT      ;SET UP INTERRUPTS
            LEA     TXBUF,A1    ;TX BUFFER POINTER
            LEA     RXBUF,A2    ;RX BUFFER POINTER
            MOVE.B  #$40,IERA   ;ENABLE TX A INT.
            MOVE.B  #$10,IERB   ;ENABLE RX B INT.
;
WT:         STOP    #$2000      ;SUPERVISOR MODE, ANY INT, NO TRAP
            JMP     WT          ;
;
;-------------------------INITIALIZATION ROUTINES-------------------------
;
INIT:       MOVE.B #7,CMR1A     ;ASYNC, NO PARITY
            MOVE.B #7,CMR1B     ;ASYNC, NO PARITY
            MOVE.B #$38,CMR2A   ;POLLED/INT MODE, NORMAL
            MOVE.B #$38,CMR2B   ;POLLED/INT MODE, NORMAL
            MOVE.B #$3F,TTRA    ;38.4K BAUD
            MOVE.B #$3F,TTRB    ;38.4K BAUD
            MOVE.B #$2F,RTRA    ;38.4K BAUD
```

```
                MOVE.B    #$2F,RTRB      ;38.4K BAUD
                MOVE.B    #$F3,TPRA      ;TX=8 BIT/CHAR,2 STOP BITS
                MOVE.B    #$F3,TPRB      ;TX=8 BIT/CHAR,2 STOP BITS
                MOVE.B    #$03,RPRA      ;RX=8 BIT/CHAR
                MOVE.B    #$03,RPRB      ;RX=8 BIT/CHAR
                MOVE.B    #$00,OMRA      ;TXRDY=NOT FULL, RXRDY=NOT EMPTY
                MOVE.B    #$00,OMRB      ;TXRDY=NOT FULL, RXRDY=NOT EMPTY
                MOVE.B    #0,CCRA        ;RESET TX A
                MOVE.B    #0,CCRB        ;RESET TX B
                MOVE.B    #2,CCRA        ;ENABLE TX A
                MOVE.B    #2,CCRB        ;ENABLE TX B
                RTS
;
SETINT:         MOVEA.L   $110,A6        ;GET ADDRESS AT VECTOR 68
                MOVE.L    #RXB,2[A6]     ;RXB INT. ROUTINE ADD. TO JUMP INST.
                MOVEA.L   $104.A6        ;GET ADDRESS AT VECTOR 65
                MOVE.L    #TDBUF,2[A6]   ;TDBUFF INT. ROUTINE ADD. TO JUMP INST.
                MOVE.B    #64,IVR        ;INT. VECTOR V64 INTO DUSCC
                MOVE.B    #$C7,ICR       ;INTRLVD, B PRTY, A&B ENBL, VECT. INC. STATUS
                RTS
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;TX READY INTERRUPT ROUTINE;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
TDBUF:          MOVE.B    [A1]+,TXFIFA   ;SEND NEXT CHAR.
                CMPA.L    #RXBUF,A1      ;AT END OF CHAR. BUFFER?
                BEQ       DISINT         ;IF LAST CHAR, DISABLE INTERRUPT
                RTE

;
;THIS WILL KEEP TX FROM INTERRUPTING UNTIL WANT TO START NEXT MESSAGE
;
DISINIT:        MOVE.B    #$85,ICR       ;TURN OFF CH A INTERRUPT
                RTE
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;RX READY INTERRUPT ROUTINE;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
RXB:            MOVE.B    RSRB,D3        ;READ RECEIVER STATUS REG.
                BTST      #5,D3          ;OVERRUN ERROR?
                BNE       RXERR          ;IF YES, GO TO ERROR HANDLER
                MOVE.B    RXFIFB,[A2]+   ;READ CHAR. TO BUFFER
                CMPA.L    #DONE,A2       ;AT END OF CHAR BUFFER?
                BEQ       STOP           ;IF LAST CHAR, STOP
                RTE
;
RXERR:          TRAP      #15            ;STOP AND DISPLAY STATUS
STOP:           TRAP      #15            ;STOP AND DISPLAY STATUS
;
;-------------------------------------------DATA BUFFERS------------------------------------------
;
TXBUF           DC.B      0,1,2,3,4,5,6,7,8,9,10
RXBUF           DS.B      11
;
DONE:           END       START
```

User notes for the SCN68/26562 (NDUSCC) and SC68/26C562 (CDUSCC)

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DESIGN CAUTIONS

– The system clock must be at least four times faster than the Tx/Rx clock for NDUSCC and faster than the Tx/Rx clock for CDUSCC.

– TRSR[7], TxEMPTY, is not the same as TxRDY on FIFO EMPTY, GSR[5], when OMR[4]=1. In this case, GSR[5] will be asserted when the last character from the FIFO is loaded into the shift register, making the FIFO empty. TRSR[7] is asserted later, when the last available character has been completely serialized and transmitted, and both the FIFO and the shift register are empty.

– Some unused inputs on the part should not be left floating, specifically:

- When not using vectored interrupts, IACKN must be tied high
- When not using DTCN, it can be left open or tied high
- When not using DONEN, it must still have a pull–up resistor to 5V.

– A channel cannot be dynamically reconfigured. Do not write to CMR1, CMR2, S1R, S2R or PCR when the channel is in use (receiver or transmitter enabled). Do not write to RPR or RTR if the receiver is enabled. Do not write to TPR or TTR if the transmitter is enabled. And, do not write to CTCR, CTPRH or CTPRL if the counter/timer is enabled.

–The REOM status bit is about 150ns before the RxRDY status bit, so that in an interrupt driven system, if IACKN is asserted during the window, the REOM status will be recognized as the highest priority interrupt and the interrupt vector will reflect this.

– An Enable Transmitter command will be ignored if it is given after a Disable Transmitter command and there is still data in the TxFIFO. The DUSCC will wait for the TxFIFO to empty and will then disable the transmitter. A work around for this situation is to wait for the TxFIFO empty bit to be set before enabling the transmitter.

–The BISYNC protocol, when used with ASCII data, requires a Frame Check Sequence (FCS) that uses LRC7 plus odd parity. The NDUSCC/CDUSCC does not provide a LRC7 FCS. The FCS calculations need to be performed by the CPU, the actual Block Check Character will be sent and received by the DUSCC/CDUSCC as a data character in this case, the DUSCC/CDUSCC would be programmed to use no FCS (NDUSCC only).

– When using a bi–phase data encoding method (i.e., Manchester, FM0, or FM1) and an externally provided receiver baud rate clock, be aware that there is a baud rate speed limitation. For this case, the data setup time to the rising edge of the receiver clock is 120ns, while the data hold time is 10ns. Since the clock edges are usually synchronized with the center of the bit halves, this will limit you to a baud rate of just over 2Mbps (1/(120ns x 4) = 2.08Mbps). If the external clock can be skewed to make use of the short hold time required, the maximum baud late available will be just over 3.8Mbs (1/130ns x 2) = 3.85Mbps) for the DUSCC (NDUSCC only).

– In a single address DMA cycle, care should be taken not to read the Rx FIFO when the FIFO is empty. A read of the empty RxFIFO using the RTXDAKN input will cause the FIFO pointers to go out of sequence and will result in previously read data to be output onto the data bus. A 'reset receiver' command or a hardware reset will always set the RxFIFO pointers back to their correct initial state if the pointers have been incremented due to this erroneous access. The RxFIFO condition is indicated by the DUSCC negating the RTxDRQN output. This caution only applies to the DUSCC.

–The SCN68562 and SC68C562 do not support the use of a 'retry' operation during a single address DMA cycle. A 684xx DMA controller has the capability to terminate the current bus cycle and then start it again when it receives a 'retry' exception code. It terminates the cycle by immediately negating its DMA ACK output, it will not assert its DTC output. However, the DUSCC will assume a valid DMA cycle and will complete the DMA operation (either reading data off the bus or placing data onto the bus) when it receives DTC asserting or DMA ACK negating, WHICHEVER OCCURS FIRST.

Initialization Caution for Asynchronous Mode Local Loop Operation

This caution only applies to situations where the local loop channel connection (CMR2[7]=10) is being used with the asynchronous channel protocol (CMR1[2:0]= 111). When initializing for this mode, there must be a one bit time wait period between having three basic initialization steps done (software Tx reset, put in local loop mode, and set a Tx clock) and enabling the receiver. The software Tx reset ensures that the transmitter output is high, then the part must be in local loop mode for the connection between the transmitter and receiver to be made, and a transmitter clock must be provided to clock the transmitter output through to the receiver. This high Tx output signal will take one bit time (as determined by the Tx clock) to clock through to the receiver shift register input.

Not allowing enough time between these three steps and enabling the receiver can cause the receiver to receive incorrect data. If the state of the receiver shift register input is low when the receiver is enabled, this low signal will be interpreted as a start bit, and the receiver will start assembling a character. The receiver shift register input can be either low or high on power up due to the part's internal logic, so this setup time is always needed.

When running at slower baud rates, it can be desirable to speed up this propagation time, since, for example, one bit time is 104µs at 9600 baud and is 20ms at 50 baud. The highest speed available with the internal baud rate generator in the part is 38.4k baud (NDUSCC only), and one bit time at this baud rate is only 26µs. So, to get the shortest propagation delay, do the following:

1. Power–up, hardware reset
2. Program CCR = H'00', Software Tx Reset
3. Program CMR2, to make the Local Loop connections
4. Program TTR = H'3F', Tx use BRG at 38.4k baud as clock
5. Additional register programming for device initialization
6. If needed, additional delay to bring total time between steps 4 and 7 to 26µs.
7. Program TTR to set up desired baud rate for the Tx
8. Program CCR = H'00', Software Tx reset
9. Program CCR = H'40', Software Rx reset
10. Program CCR = H'02', Enable Tx
11. Program CCR = H'42', Enable Rx

User notes for the SCN68/26562 (NDUSCC) and SC68/26C562 (CDUSCC)

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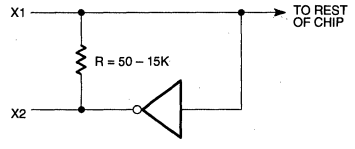
Theoretical Information on DUSCC/CDUSCC Crystal Oscillator

The information contained in Table 3 is based on computer simulations over the expected process range. It is not based on characterization data or actual device testing.

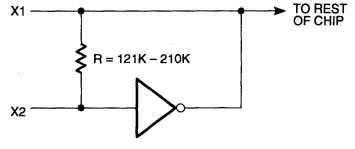
Table 3.

Parameter	Max	Typ	Min	Units
NDUSCC				
Feedback resistor[2]	210	160	121	kΩ
X1/ground capacitance	3.0	1.7	1.0	pF
X2/ground capacitance	6.0	4.3	3.0	pF
X1/X2 capacitance	2.0	1.0	0.5	pF
Inverter AC gain (14.7456MHz)[3]		2.8		dB
Inverter phase shift (14.7456MHz)[3]		249		deg.
Inverter AC gain (16MHz)[3]		2.6		dB
Inverter phase shift (16MHz)[3]		253		deg.
Inverter AC gain (2MHz)[3]		9.7		dB
Inverter phase shift (2MHz)[3]		210		deg.
X1/X2 bias level	2.9	2.3	1.8	V
Inverter prop delay[1]	18	11	6	ns
CDUSCC				
X1/ground capacitance	20	15	10	pF
X2/ground capacitance	20	15	10	pF
X1/X2 capacitance	2.0	1.0	0.5	pF
Inverter AC gain (14.7456MHz)[4]	8.5	7.3	6.0	dB
Inverter phase shift gain (14.7456MHz)[4]	260	250	240	deg.
Inverter AC gain (16MHz)[4]	7.9	7.3	6.0	dB
Inverter phase shift gain[4]	320	300	250	deg.
Inverter AC gain (2MHz)[4]	15.5	13.6	7.6	dB
Inverter phase shift (2MHz)[4]	210	190	185	deg.
X1/X2 bias level	2.9	2.3	1.8	V

NOTES:
1. 10pF load on output X1. Delay from X2 = 3V to X1 = 3V.
2. Based on I–V characteristics of depletion transistor.
3. V_{OUT}/V_{IN} at bias point. X1 10pF loading.
4. V_{OUT}/V_{IN} at bias point, X1 10pF loading.



CDUSCC Oscillator



NDUSCC Oscillator

Inverter propagation delay = 6 – 18ns
Inverter AC gain = 2.6 – 9.7

DUSCC/CDUSCC Oscillator

Section 3
CDUSCC User's Guide

CONTENTS

Table of Contents

TABLES

CMOS DUSCC User's Guide

FORWARD

This document provides a complete description of the operational modes of the Philips Semiconductors SC26C562 and 68C562 CMOS Dual Universal Serial Communications Controller (CDUSCC). AC and DC specifications for the CDUSCC are not contained in this document, but can be found in the companion documents, the **SC26C562 or SC68C562 data sheet.**

Due to the complexity of the many protocols supported by CDUSCC, this User's Guide has been organized into three major sections.

Section 1 — Quick reference data and summary information for CDUSCC

Section 2 — CDUSCC overview and protocol independent feature descriptions

Section 3 — CDUSCC protocol dependent feature descriptions

In addition to these sections, an extensive set of appendices have been provided to supply general protocol background information and helpful guidance to successful CDUSCC application.

Throughout this document references will be made to the CDUSCC default and extended modes. The CDUSCC default mode is identical to the predecessor NMOS component NDUSCC. Thus the majority of information in this user's guide is applicable to existing NDUSCC applications. No special actions are required to achieve operation in default mode. The extended mode implies the use of features present on CDUSCC that did not exist on NDUSCC. The only action required to operate in extended mode is to access registers not present in NDUSCC by setting A7 bit (see Table 3). There is no specific default or extended bit or flag, A7 needs to be set or reset to access the registers, but it is not needed to be set/reset for actual operation. There are references made to default/extended Modes, Protocol Modes and DMA Modes. Once should be careful when interpreting the word 'Mode'. To avoid confusion the acronym CDUSCC will be used except when specific reference to the predecessor component must be made. Any reference to the SCN26562 and SCN68562 will use the acronym NDUSCC.

In this document, signals are discussed using the terms 'active' and 'inactive' or 'asserted' and 'negated' independent of whether the signal is active in the High (logic 1) or Low (logic 0) state. An 'N' at the end of a pin name signifies the signal associated with the pin is Active-Low (see individual pin description for the definition of the active level of each signal.) Pins which are provided for both channels are designated by an 'A/B' after the name of the pin and the active-Low state indicator, N, if applicable.

Three aids have been incorporated for locating information in this document:

1. Table of Contents
2. Cross Reference Index
3. Table 1 (Register Map) identifies the page number that provides details of the register modes and operations.

CMOS DUSCC User's Guide

DESCRIPTION

The Philips Semiconductors SC26C562/SC68C562 CMOS Dual Universal Serial Communications Controller (CDUSCC) is a single-chip CMOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SC26C562 interfaces to synchronous bus and SC68C562 interfaces with asynchronous bus MPUs and are capable of program-polled, interrupt driven, block-move or DMA data transfers.

The CDUSCC is fully hardware (pin) and software (register) compatible with the existing NDUSCC. CDUSCC will automatically configure to the NDUSCC register map (default mode) on power up.

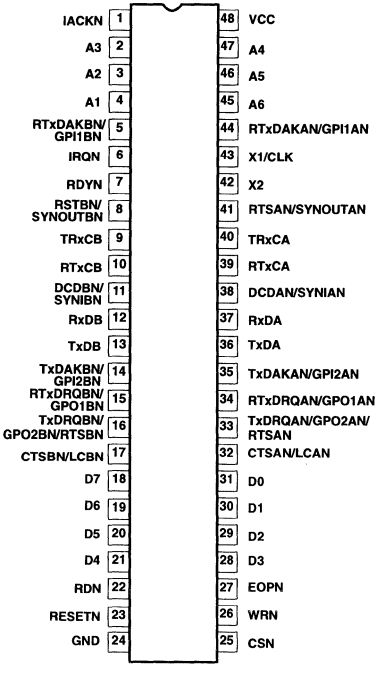
The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides sixteen common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the CDUSCC well-suited for dual-speed channel applications. Data rates up to 10Mbits per second are supported.

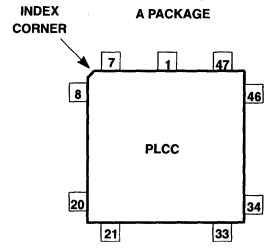
The transmitter and receiver each contain a sixteen-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to sixteen characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs and outputs are general purpose in nature, they can be optionally programmed for other functions.

The SC26C562 is optimized to interface with processors using a synchronous bus interface, such as the 80xxx family. The SC68C562 is used with asynchronous bus, such as the 68xxx processor family.

PIN CONFIGURATIONS — SC26C562

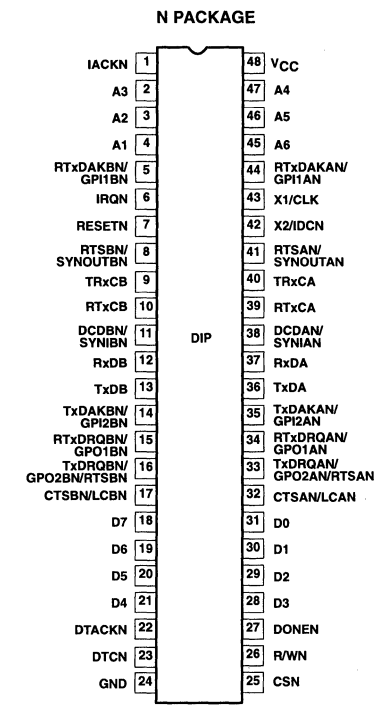


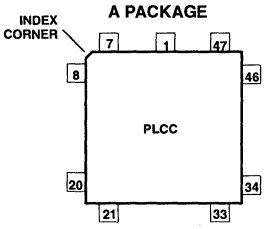


PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	IACKN	19	CTSBN/LCBN	37	RTxDRQAN/ GPO1AN/
2	A3	20	D7	38	TxDAKAN/ GPI2AN
3	A2	21	D6	39	TxDA
4	A1	22	D5	40	RxDA
5	RTxDAKBN/ GPI1BN	23	D4	41	GND
6	IRQN	24	RDN	42	DCDAN/ SYNIAN
7	GND	25	RESETN	43	RTxCA
8	RDYN	26	GND	44	TRxCA
9	RSTBN/ SYNOUTBN	27	CSN	45	RTSAN/ SYNOUTAN
10	TRxCB	28	WRN	46	X2
11	RTxCB	29	EOPN	47	X1/CLK
12	DCDBN/ SYNIBN	30	D3	48	RTxDAKAN/ GPI1AN
13	GND	31	D2	49	A6
14	RxDB	32	D1	50	A5
15	TxDB	33	D0	51	A4
16	TxDAKBN/ GPI2BN	34	V_{CC}	52	V_{CC}
17	RTxDRQBN/ GPO1BN/	35	CTSAN/LCAN		
18	TxDRQBN/ GPO2BN/ RTSBN	36	TxDRQAN/ GPO2AN/ RTSAN		

CMOS DUSCC User's Guide

PIN CONFIGURATIONS — SC68C562





Pin	Function	Pin	Function
1	IACKN	27	CSN
2	A3	28	R/WN
3	A2	29	DONEN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
		32	D1
6	IRQN	33	D0
7	GND	34	V_{CC}
8	RESETN	35	CTSAN/LCAN
9	RTSBN/ SYNOUTBN	36	TxDRQAN/ GPO2AN/RTSAN
10	TRxCB	37	RTxDRQAN/ GPO1AN
11	RTxCB	38	TxDAKAN/ GPI2AN
12	DCDBN/ SYNIBN	39	TxDA
13	GND	40	RxDA
14	RxDB	41	GND
15	TxDB	42	DCDAN/ SYNIAN
16	TxDAKBN/ GPI2BN	43	RTxCA
17	RTxDRQBN/ GPO1BN	44	TRxCA
18	TxDRQBN/ GPO2BN/RTSBN	45	RTSAN/ SYNOUTAN
19	CTSBN/LCBN	46	X2/IDCN
20	D7	47	X1/CLK
21	D6	48	RTxDAKAN/ GPI1AN
22	D5	49	A6
23	D4	50	A5
24	DTACKN	51	A4
25	DTCN	52	V_{CC}
26	GND		

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±10%, T_A = 0 to +70°C Serial Data Rate = 10Mbps Maximum		DWG #
48-Pin Plastic Dual In-Line Package (DIP)	SC26C562C1N	SC68C562C1N	0416C
52-Pin Plastic Leaded Chip Carrier (PLCC) Package	SC26C562C1A	SC68C562C1A	0397E

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND	-0.5 to +7.0	V
T_{STG}	Voltage from any pin to GND	-0.5 to V_{CC} +0.5	V

CMOS DUSCC User's Guide

FEATURES

General Features

- Dual full-duplex synchronous/ asynchronous receiver and transmitter
- Multi-protocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: Single SYNC, dual SYNC, BiSYNC, DDCMP
  - ASYNC: 5-8 bits plus optional parity
- Sixteen character receive and transmit FIFOs with interrupt threshold control
- FIFO'd status bits
- Watchdog timer
- 0 to 10 Mbit/sec data rate
- High speed data bus interface: 160ns bus cycle
- Programmable bit rate for each receiver and transmitter selectable from:
  - 19 fixed rates: 50 to 64K baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- or half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Compatible with Synchronous and Asynchronous bus DMA controllers
  - Half- or full-duplex operation
  - Single or dual address data transfers
  - Automatic frame termination on counter/ timer terminal count or DMA DONE (EOPN)
  - Frame status byte
- DPLL operation up to 312.5kHz with external clock
- Interrupt capabilities
  - Vector output (fixed or modified by status)
  - Individual interrupt enable bits
  - Programmable internal priorities
  - Maskable interrupt conditions
  - Intel's 80XX compatible
  - Interrupt Daisy Chain (68C562 only)
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general purpose I/O pins per channel
  - CTS and DCD programmable auto-enables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- Transmit path clear status
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X Rx and Tx clock factors
- Parity, overrun and framing error detection
- False start bit detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmit and receive up to 10Mbps at 1x data rate

Bit-Oriented Protocol

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for I field
- Zero insertion and deletion
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Transmit 7 or 8 bit ABORT
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

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Character-Oriented Protocols

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK linefill or underrun
- Idle in MARKs or SYNs
- Parity, FCS, overrun and underrun error detection
- Optional SYN exclusion from FCS
- BISYNC features
  - EBCDIC or ASCII header, text and control messages
  - SYN, DLE stripping
  - EOM (end of message) detection and transmission
  - Auto transparency mode switching
  - Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
  - Control character sequence detection for both transparent and normal text
  - Parity generation for data and LRC characters

PIN DESCRIPTION

MNEMONIC	*	PIN NO.		TYPE	NAME AND FUNCTION
		DIP	PLCC		
A1–A6	B	4-2, 47-45	4-2, 51-49	I	**Address Lines:** Active-high. Address inputs which specify which of the internal registers is accessed for read/write operation.
D0–D7	B	31-28, 21-18	33-30, 23-20	I/O	**Bi-directional Data Bus:** Active-high, 3-State. Bit 0 is the LSB and bit 7 is the MSB. All data, command and status transfers between the CPU and the CDUSCC take place over this bus. The data bus is enabled when CSN and RDN, or CSN and WRN are low or during interrupt acknowledge cycles and single address DMA acknowledge cycles.
RDN	26	22	24	I	**Read Strobe:** Active-low input. When active and CSN is also active, causes the content of the addressed register to be present on the data bus. RDN is ignored unless CSN is active. (26C562 only)
WRN	26	26	28	I	**Write Strobe:** Active-low input. When active and CSN is also active, the content of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of WRN or CSN, whichever occurs first. WRN is ignored unless CSN is active. (26C562 only)
R/WN	68	26	28	I	**Read/Write:** A high input indicates a read cycle and a low indicates a write cycle when CEN is active. (68C562 only)
CSN (CEN)	26 68	25	27	I	**Chip Select (Chip Enable):** Active-low input. When active, data transfers between the CPU and the CDUSCC are enabled on D0–D7 as controlled by RDN or WRN and A1–A6 inputs. When CSN is high, the data lines are placed in the 3-State condition (except during interrupt acknowledge cycles and single address DMA transfers).
RDYN	26	7	8	O	**Ready:** Active-low, open drain. Used to synchronize data transfers between the CPU and the CDUSCC. It is valid only during read and write cycles where the CDUSCC is configured in 'wait on Rx', 'wait on Tx' or 'wait on Tx or Rx' modes, otherwise it is always inactive. RDYN becomes active on the leading edge of RDN and WRN if the requested operation cannot be performed (viz, no data in RxFIFO in the case of a read or no room in the TxFIFO in the case of a write). (26C562 only)
IRQN	B	6	6	O	**Interrupt Request:** Active-low, open-drain. This output is asserted upon occurrence of any enabled interrupting condition. The CPU can read the general status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the CDUSCC to output an interrupt vector on the data bus.
IACKN[1]	B	1	1	I	**Interrupt Acknowledge:** Active-low. When IACKN is asserted, the CDUSCC responds by either forcing the bus into high-impedance, placing a vector number, call instruction or zero on the data bus. The vector number can be modified or unmodified by the status. If no interrupt is pending, IACKN is ignored and the data bus placed in high-impedance.
X1/CLK	B	43	47	I	**Crystal 1 or External Clock:** When using the crystal oscillator, the crystal is connected between pins X1 and X2. If a crystal is not used, an external clock is supplied at this input. This clock is used to drive the internal bit rate generator, as an optional input to the counter/timer or DPLL, and to provide other required clocking signals. When a crystal is used, a capacitor must be connected from this pin to ground.
X2	26	42	46	O	**Crystal 2:** Connection for other side of crystal. When a crystal is used, a capacitor must be connected from this pin to ground. If an external clock is used on X1, this pin should be left floating. (26C562 only)

PIN DESCRIPTION (Continued)

MNEMONIC	*	PIN NO.		TYPE	NAME AND FUNCTION
		DIP	PLCC		
X2/IDCN	68	42	46	O	**Crystal or Interrupt Daisy Chain:** When a crystal is used as the timing source, the crystal is connected between pins X1 and X2. When crystal is not used, this pin can be programmed to provide an interrupt daisy chain active-low output which propagates the IACKN signal to lower priority devices, if no active interrupt is pending. This pin should be left floating when an external clock is used on X1 and X2 is not used as an interrupt daisy chain output. When a crystal is used, a capacitor must be connected from this pin to ground. (68C562 only)
RESETN	26	23	25	I	**Master Reset:** Active-low. A low on this pin resets the transmitters and receivers and resets the registers shown in Table 1 of CDUSCC User's Guide. Reset is asynchronous, i.e., no clock is required. (26C562)
RESETN	68	7	8	I	**Master Reset:** Active-low. A low on this pin resets the transmitters and receivers and resets the registers shown in Table 1 of CDUSCC User's Guide. Reset is asynchronous, i.e., no clock is required. (68C562)
RxDA, RxDB	B	37, 12	40, 14	I	**Channel A (B) Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified for the channel, the input is sampled on the rising edge of the clock.
TxDA, TxDB	B	36, 13	39, 15	O	**Channel A (B) Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is in the marking (high) condition when the transmitter is disabled or when the channel is operating in local loopback mode. If external transmitter clock is specified for the channel, the data is shifted on the falling edge of the clock.
RTxCA, RTxCB	B	39, 10	43, 11	I/O	**Channel A (B) Receiver/Transmitter Clock:** As an input, it can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the transmitter shift clock (1X), or the receiver sampling clock (1X).
TRxCA, TRxCB	B	40, 9	44, 10	I/O	**Channel A (B) Transmitter/Receiver Clock:** As an input, it can supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the DPLL output, the transmitter shift clock (1X), the receiver sampling clock (1X), the transmitter BRG clock (16X), the receiver BRG clock (16X), or the internal system clock (X1 ÷ 2).
DTACKN	68	22	24	O	**Data Transfer Acknowledge:** Active-low, 3-state. DTACKN is asserted on a write cycle to indicate that the data on the bus has been latched, and on a read cycle or interrupt acknowledge cycle to indicate valid data is on the bus. In a write bus cycle, input data is latched by the assertion (falling edge) of DTACKN or by the negation (rising edge) of CSN, whichever occurs first. The signal is negated when completion of the cycle is indicated by negation of CSN or IACKN input, and returns to the inactive state (3-state) a short period after it is negated. In single address DMA mode, input data is latched by the assertion (falling edge) of DTCN or by the negation (rising edge) of the DMA acknowledge input, whichever occurs first. DTACK is negated when completion of the cycle is indicated by the assertion of DTCN or negation of DMA acknowledge inputs (whichever occurs first), and returns to the inactive state (3-state) a short period after it is negated. When inactive, DTACKN requires an external pull-up resistor. (68C562 only)
DTCN	68	23	25	I	**Device Transfer Complete:** Active-low. DTCN is asserted by the DMA controller to indicate that the requested data transfer is complete. (68C562 only)
CTSA/BN, LCA/BN	B	32, 17	35, 19	I/O	**Channel A (B) Clear-to-Send Input or Loop Control Output:** Active-low. The signal can be programmed to act as an enable for the transmitter when not in loop mode. The CDUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. When operating in the BOP loop mode, this pin becomes a loop control output which is asserted and negated by CDUSCC commands. This output provides the means of controlling external loop interface hardware to go on-line and off-line without disturbing operation of the loop.
DCDA/BN, SYN1A/BN	B	38, 11	42, 12	I	**Channel A (B) Data Carrier Detected or External Sync Input:** The function of this pin is programmable. As a DCD active-low input, it acts as an enable for the receiver or can be used as a general purpose input. For the DCD function, the CDUSCC detects logic level transitions on this pin and can be programmed to generate an interrupt when a transition occurs. As an active-low external sync input, it is used in COP single SYN mode to obtain character synchronization for the receiver without receipt of a SYN character. This mode can be used in disc or tape controller applications or for the optional byte timing lead in X.21.

PIN DESCRIPTION (Continued)

MNEMONIC	*	PIN NO.		TYPE	NAME AND FUNCTION
		DIP	PLCC		
RTxDRQA/BN, GPO1A/BN	B	34, 15	37, 17	O	**Channel A (B) Receiver/Transmitter DMA Service Request or General Purpose Output:** Active-low. For half-duplex DMA operation, this output indicates to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or that the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, this output indicates to the DMA controller that data is available in the receiver FIFO. In non-DMA mode, this pin is a general purpose output that can be asserted and negated under program control.
TxDRQA/BN, GPO2A/BN, RTSA/BN	B	33, 16	36, 18	O	**Channel A (B) Transmitter DMA Service Request, General Purpose Output, or Request-to-Send:** Active-low. For full-duplex DMA operation, this output indicates to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full-duplex DMA mode, this pin can be programmed as a general purpose or a Request-to-Send output, which can be asserted and negated under program control.
RTxDAKA/BN, GPI1A/BN	B	44, 5	48, 5	I	**Channel A (B) Receiver/Transmitter DMA Acknowledge or General Purpose Input:** Active-low. For half-duplex single address operation, this input indicates to the CDUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO when the receiver is enabled or load transmitter FIFO when the transmitter is enabled) is beginning. For full-duplex single address DMA operation, this input indicates to the CDUSCC that the DMA controller has acquired the bus and that the requested read receiver FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in single address DMA mode.
TxDAKA/BN, GPI2A/BN	B	35, 14	38, 16	I	**Channel A (B) Transmitter DMA Acknowledge or General Purpose Input:** Active-low. When the channel is programmed for full-duplex single address DMA operation, this input is asserted to indicate to the CDUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in full-duplex single address DMA mode.
EOPN[1] (DONEN)	26 68	27	29	I/O	**EOPN (DONEN):** Active-low, open-drain. EOPN (DONEN) can be used and is active in both DMA and non-DMA modes. As an input, EOPN indicates the last DMA transfer cycle to the TxFIFO. As an output, EOPN indicates either the last DMA transfer from the RxFIFO or that the transmitted character count has reached terminal count.
RTSA/BN, SYNOUTA/BN	B	41, 8	45, 9	O	**Channel A (B) Sync Detect or Request-to-Send:** Active-low. If programmed as a sync output, it is asserted one bit time after the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes) is detected by the receiver. As a Request-to-Send modem control signal, it functions as described previously for the TxDRQN/RTSN pin.
V_{CC}	B	48	34, 52	I	**+5V Power Input**
GND	B	24	26, 13, 41, 7	I	**Signal and Power Ground Input**

* B: Both 68C562 and 26C562
  26: Intel version only (26C562)
  68: Motorola version only (68C562)

NOTES:
1. These pins should be "pulled-up" with an external resistor to V_{CC} if not used.
2. Please refer to data sheet (Product Specification) for timing information.

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Philips Semiconductors

Data Communications

SECTION 1

QUICK REFERENCE DATA

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NDUSCC AND CDUSCC COMPATIBILITY

Hardware Compatibility

Users familiar with the NMOS version of DUSCC (SCN26562) should be aware that the CDUSCC is fully hardware pin compatible with NDUSCC. However, Philips Semiconductors recommends for optimum performance that the following measures be taken for new card designs utilizing CDUSCC in the PLCC package.

1. Provide additional ground connections to Pins 7, 13 and 41 (previously not connected).
2. Provide additional V_{CC} connection and de-coupling to Pin 34 (previously not connected)

Failure to follow the above guidelines (i.e., use of the CDUSCC in printed circuit cards designed for NDUSCC) can result in reduced noise margins for the device. Performance of a CDUSCC device in an NDUSCC socket will be as good as that for the NMOS device, but not up to the full potential of the CMOS device with respect to noise margin.

Designs using external TTL drive to X1 should float X2 when using CDUSCC (vs grounding X2 for NDUSCC). CDUSCC may be safely operated with X2 grounded, but power dissipation of the IC will be increased. In the event that X2 cannot be floated when using TTL drive (i.e., CDUSCC in an NDUSCC socket) power dissipation can be reduced by disabling the X2 driver via software (set PCRA [7] = 1, see Figure 42).

Designs with critical AC timing should review the CMOS DUSCC data sheet, since many AC timings have been improved over the NMOS DUSCC, and timing problems might occur if the user hardware is not capable of supporting these improved timings.

Software Compatibility

The CDUSCC supports an extended register set which is accessed via two previously unused registers in the NDUSCC register space (addresses 011101 and 111101), the user should verify that no I/O writes occur to these register locations. Some users use a block write to initialize all registers, which will write to these locations. Software that accesses either of these locations and is not intended to make use of the extended capabilities of CDUSCC should be modified to eliminate the access.

Since the data FIFOs of CDUSCC are deeper than NDUSCC, it is possible that software expecting data to overrun the FIFOs' would not get overrun and data will not be lost. In most cases this is not a problem, but some users may have utilized such techniques for diagnostic purposes. In that case the diagnostic code should be modified.

New Capabilities

CDUSCC adds the following major features:

- 8 bit data bus with 160ns bus cycle
- 0 to 10Mbit per second line data rate
- RxFIFO
  - 16 x 8 data FIFO
  - RxRDY triggered by programmable filled level of FIFO
  - Watch dog timer
  - Status bits for the filled level of RxFIFO
  - FIFO all error status bits
  - DMA frame status byte
- TxFIFO
  - 16 x 8 data FIFO
  - TxRDY triggered by programmable filled level of FIFO
  - Status bits for the empty level of TxFIFO
- Baud Rate Generator — from 50bps up to 64Kbps
- Interrupt control
  - Individual interrupt enable bits
- Support X.21 pattern recognition
- Improved BiSYNC support
  - Parity/LRC
  - SYN exclusion
  - ITB block handling
  - Header only handling
- Lower power consumption

To access some of these capabilities, additional registers are required. The technique used to access these additional registers is to re-use the addresses of eight registers not normally accessed after initial configuration. The setting of the A7 bit will toggle to the alternate register set. In this document the term 'Extended Mode' will be used to indicate that the A7 bit had been set at some point, and the value of the alternate register set changed to invoke some of the new CDUSCC features. It is not necessary for the A7 bit to remain set for the extended mode features to operate. A7 bit must be reset to 0 to access some of the old registers, as listed below (see Table 1). The term 'Default Mode' will be used to indicate that none of the new features were selected, and NDUSCC register compatibility is being maintained.

A7 = 0	A7 = 1
S1R	IER1
S2R	IER2
TTR	IER3
RTR	TRCR
PCR	RFLR
IER	FTLR
IVR/IVRM	TRMSR
ICR/MRR	TELR

REGISTERS

The addressable registers of the CDUSCC are shown in Table 4. The following rules apply to all registers:

1. A read from the SEA location in the map results in all ones for data.
2. Unused bits of a defined register are read as zeros, unless ones have been loaded after master reset.
3. Bits that are unused in the chosen mode but are used in others are readable and writable but their contents are ignored in the chosen mode.
4. All registers are addressable as 8-bit quantities only.

The operation of the CDUSCC is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The contents of certain control registers are initialized on MASTER RESET. Care should be exercised if the contents of a register are

changed during operation, since certain changes may cause operational problems, e.g., changing the channel mode at an inappropriate time may cause the reception or transmission of an incorrect character. In general, the contents of registers which control transmitter or receiver operation, or the counter/timer, should be changed only when they are not enabled.

The CDUSCC registers can be separated into five groups to facilitate their usage:

1. Channel mode configuration and pin description registers
2. Transmitter and receiver parameter and timing registers
3. Counter/timer control and value registers
4. Interrupt control and status registers
5. Command registers

This arrangement is used in the following description of the CDUSCC registers. Register bit map is described in the same order as register address map in Table 3.

FUNCTIONAL DESCRIPTION

Functional Description

As illustrated in the Block Diagram, the CDUSCC consists of eight major functional blocks:

- **Host Interface and Bus Buffer**
- **DMA Interface**
- **Special Function Pins**
- **Interrupt Control**
- **Channel Timing**
- **Operation Control**
- **Transmitter**
- **Receiver**

Other than the Operation Control section, which is very much dependent upon the communications protocol selected, most of the functional blocks of CDUSCC operate in essentially the same manner regardless of protocol mode. The description of CDUSCC will be separated into PROTOCOL INDEPENDENT RESOURCES (Section 2), the operation of which is not affected by selection of protocol mode, and PROTOCOL DEPENDENT RESOURCES (Section 3), which behave quite differently depending on the protocol selected.

Host Interface

Two versions of the CDUSCC exist, each supporting a different Host Interface. The 26C562 supports Intel-like MPUs; the 68C562 supports Motorola-like 68k CPUs.

The host interface of the 26C562 consists of an 8-bit, bi-directional data bus (D0-D7), 6 address lines (A1-A6), four control inputs (RDN, WRN, CSN, RESETN) and one control output (RDYN). This host interface is compatible with iAPX hosts without additional logic (other than address decoding).

The host interface of the 68C562 consists of an 8-bit, bi-directional data bus (D0-D7), 6 address lines (A1-A6), three control inputs (R/WN, CSN, RESETN) and one control output (DTACK). This host interface is compatible with 68000 hosts without additional logic (other than address decoding).

Address 7: The CDUSCC has a register space of 128 bytes, but only 6 address lines are physically present. A7, the 7th address bit, is generated internally by a flip-flop. Upon reset, the flip-flop is reset (A7 = 0). The A7 bit can be set or cleared by writing FFh to the SEA or REA registers at the following addresses:

Table 1. A7 Bit Control

ADDRESS	WRITE		READ
1Dh	REA	Reset A7	CID
3Dh	SEA	Set A7	Not Allowed

By setting the A7 address bit, the user has made available the complete resource set of the CDUSCC, at the cost of some register level compatibility with the NDUSCC predecessor part. Only the eight register pairs indicated in the table on the previous page are affected by the A7 bit. All other registers have the same function and bit definitions regardless of the A7 state. It should be noted that many of the registers in the default mode state (A7 = 0) must be properly initialized prior to switching to extended mode (A7 = 1). Once in extended mode, it is not normally necessary to return to default mode unless a radical change to the channel operation or protocol is required.

Chip Identification: A read from the CID register at address 1Dh returns a software signature that identifies the version of CDUSCC installed on the card. This feature enables a single software driver to be self adapting to the capabilities of the hardware installed (NDUSCC, CDUSCC or future derivatives).

Table 2. CID Definitions

Read Data	Part Version
FFh	NDUSCC – all revisions
7Fh	CDUSCC Rev –
BFh	CDUSCC Rev A

Master Reset: The contents of each register following a master reset is shown in Table 3, the CDUSCC Register Address Map. For 68C562, master reset can only be achieved by assertion of the RESETN signal line (called Hardware Reset). For 26C562, reset can be achieved by either assertion of the RESETN signal or by writing FFh to MRR register. The MRR is used to perform reset function by software. For 26C562, the MRR register must be read no matter what method is used for reset (Power-up, Hardware Reset, Software Reset) prior to operation of the CDUSCC.

Wait Mode: Either the receiver or the transmitter or both may be programmed for wait mode operation, independently for each channel, via CMR2[5:3].

In this mode, if the host attempts a write to the transmit FIFO and an empty FIFO position is not available, the RDYN (for 26C562) or DTACKN (for 68C562) line will not assert until a position empties. The data will then be written into the FIFO and RDYN will be negated to signify that the transfer is complete. Similarly, a read of an empty receive FIFO will be held off until data is available to be transferred.

CAUTION: This mode can potentially cause the host system to hang up if, for example, a read request was made and no further data was available.

NOTE: Unless the CMR2 register has been programmed for this mode of operation, RDYN output is always inactive. It cannot be used to introduce Wait States in other bus cycles, i.e., command or status register I/O.

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Table 3. CDUSCC Register Address Map

Hex Address			Acro-nym	Register Name	Mode[5]	R/W	Affected By	Page
Ch. A	Comm.	Ch. B					Master Reset	Ref.
00h		20h	CMR1	Channel Mode Register 1	Both	R/W	Yes — 00	580, 586, 595
01h		21h	CMR2	Channel Mode Register 2	Both	R/W	Yes — 00	581, 587, 596
02h[1]		22h[1]	S1R	SYN 1/Secondary Address 1 Register	Default	R/W	Yes — 00	582, 588, 596
03h[1]		23h[1]	S2R	SYN 2/Secondary Address 2 Register	Default	R/W	Yes — 00	588 597
04h		24h	TPR	Transmitter Parameter Register	Both	R/W	Yes — 00	582, 588, 597
05h[1]		25h[1]	TTR	Transmitter Timing Register	Default	R/W	Yes — 00	560
06h		26h	RPR	Receiver Parameter Register	Both	R/W	Yes — 00	583, 590, 599
07h[1]		27h[1]	RTR	Receiver Timing Register	Default	R/W	Yes — 00	561
08h		28h	CTPRH	Counter/Timer Preset Register High	Both	R/W	No	565
09h		29h	CTPRL	Counter/Timer Preset Register Low	Both	R/W	No	565
0Ah		2Ah	CTCR	Counter/Timer Control Register	Both	R/W	Yes — 00	564
0Bh		2Bh	OMR	Output and Miscellaneous Register	Both	R/W	Yes — 00	568
0Ch		2Ch	CTH	Counter/Timer High	Both	R	No	565
0Dh		2Dh	CTL	Counter/Timer Low	Both	R	No	566
0Eh[1]		2Eh[1]	PCR	Pin Configuration Register	Default	R/W	Yes — 00	567
0Fh		2Fh	CCR	Channel Command Register[8]	Both	R/W	Yes — 00	570
10h		30h	TxFIFO	Transmitter FIFO	Both	W[4]	Yes — 00	553
14h		34h	RxFIFO	Receiver FIFO	Both	R[4]	Yes — 00	554
18h		38h	RSR	Receiver Status Register	Both	R/W[2]	Yes — 00	584, 590, 591, 600
19h		39h	TRSR	Transmitter and Receiver Status Register	Both	R/W[2]	Yes — 00	585, 592, 601,
1Ah		3Ah	ICTSR	Input and Counter/Timer Status Register	Both	R/W[2]	Yes — 00	537
	1Bh		GSR	General Status Register	Both	R/W[2]	Yes — 00	536
1Ch[1]		3Ch[1]	IER	Interrupt Enable Register	Default	R/W[2]	Yes — 00	544
	1Dh		REA	Reset A7 bit	Both	W	Yes A7 = 0	528
	1Dh		CID	Chip ID Register	Extended	R	No	528
	1Eh[1]		IVR	Interrupt Vector Register — Unmodified	Default	R/W	Yes — 0Fh	546
	1Fh[1]		ICR	Interrupt Control Register	Default	R/W	Yes — 00	543
	3Dh		SEA	Set A7 bit	Both	W	Yes A7=0	528
	3Eh[1]		IVRM	Interrupt Vector Register — Modified	Default	R	Yes — FFh	546
	3Fh[1]		MRR	Master Reset Register	Default	R/W	Yes[6]	528
02h[3]		22h[3]	IER1	Interrupt Enable Register 1	Extended	R/W	Yes — 00	545, 585, 592, 601
03h[3]		23h[3]	IER2	Interrupt Enable Register 2	Extended	R/W	Yes — 00	545, 585, 592, 601
05h[3]		25h[3]	IER3	Interrupt Enable Register 3	Extended	R/W	Yes — 00	545
07h[3]		27h[3]	TRCR	Tx/Rx Command Register	Extended	R/W	Yes — 00	569
0Eh[3]		2Eh[3]	RFLR	RxFIFO fill level register[7]	Extended	R	Yes — 00	556
1Ch[3]		3Ch[3]	FTLR	FIFO threshold level register	Extended	R/W	Yes — 33h	557
1Eh[3]		3Eh[3]	TRMSR	Tx/Rx Misc Status Register	Extended	R/W[2]	Yes — 00	538
1Fh[3]		3Fh[3]	TELR	TxFIFO empty level register[7]	Extended	R	Yes — 10h	556

NOTES:
1. Internal A7 bit should be set to '0' thru REA register to access these registers.
2. A write to this register may perform a status resetting operation.
3. Internal A7 bit should be set to '1' thru SEA register to access these registers.
4. FIFOs are addressable at any of four adjacent addresses to allow them to be addressed as byte/word/double word with the iAPX86 Family MOV instruction.
5. The mode identifies if this register is used in NDUSCC (default), CDUSCC (extended) or both modes of operation. Default and extended mode registers are mutually exclusive in the address space.
6. SC26C562 version only, a read of MRR must be performed after H/W reset or power-up and before any operation of the 26C562 is enabled.
7. FIFO fill level and empty levels are updated after 5-7 X1 clocks at reset.
8. Minimum of three X1 clocks are required while CEN/CSN is high between two commands for the same channel.

Table 4. Register Bit Assignment Table

Addr A / B	Register	Mode	7	6	5	4	3	2	1	0
00h/20h	CMR1	ASYNC	data encoding		parity type	parity mode		1	1	1
		BOP	data encoding		extended ctrl	address mode		0	channel protocol mode	
		COP	data encoding		char code	parity mode		1	channel protocol mode	
01/21h	CMR2	ASYNC	channel connection		data transfer interface			0	0	0
		SYNC	channel connection		data transfer interface			frame check sequence select		
02/22h	S1R	ASYNC	character compare (5-8 bits)							
		BOP	first address octet							
		COP	SYN1 (5-8 bits)							
03/23h	S2R	BOP	second address octet							
		COP	SYN2 (5-8 bits)							
04/24h	TPR	ASYNC	stop bits per character				TxRTS control	CTS enable Tx	Tx character length	
		BOP	underrun control		IDLE	TEOM on Zero or Done	TxRTS Control	CTS enable Tx	Tx character length	
		COP	underrun control		IDLE	TEOM on Zero or Done	TxRTS Control	CTS enable Tx	Tx character length	
05/25h	TTR	all	ext. TxC source	transmitter clock select			bit rate select from internal BRG			
06/26h	RPR	ASYNC	0	0	0	RxRTS control	strip parity	DCD enable Rx	Rx character length	
		BOP	0	FCS to FIFO	overrun mode	0	all party address	DCD enable Rx	Rx character length	
		COP	SYN strip	FCS to FIFO	auto hunt & pad ck	external sync	strip parity	DCD enable Rx	Rx character length	
07/27h	RTR	all	ext. RxC source	receiver clock select			bit rate select from internal BRG			
08/28h	CTPRH	all	most significant bits of counter/timer preset value							
09/29h	CTPRL	all	least significant bits of counter/timer preset value							
0A/2Ah	CTCR	all	zero detect interrupt	zero detect control	output control	prescaler		clock source		
0B/2Bh	OMR	all	Tx residual character length			TxRDY activate	RxRDY activate	OUT2	OUT1	RTS
0C/2Ch	CTH	all	most significant bits of counter/timer							
0D/2Dh	CTL	all	least significant bits of counter/timer							
0E/2Eh	PCR	all	X2/IDC*	GPO2/ RTS	SYNOUT/ RTS	RTxC pin usage		TRxC pin usage		
0F/2Fh	CCR	all	command word							
10/30h	TxFIFO	all	transmit data port							
14/34h	RxFIFO	all	receive data port							
18/38h	RSR	ASYNC	character compare	RTS negated	overrun error	not used	BRK end detect	BRK start detect	framing error	parity error
		BOP	EOM detect	abort detect	overrun error	short frame det	idle detect	flag detect	CRC error	RCL not zero
		BOP loop	EOM detect	abort/ EOP det	overrun error	short frame det	turn-around det	flag detect	CRC error	RCL not zero
		COP	EOM detect	pad error	overrun error	not used	not used	SYN detect	CRC error	parity error

* PCRA only, not used in PCRB

Register Bit Assignment Table (continued)

Addr A / B	Register	Mode	7	6	5	4	3	2	1	0
19/39h	TRSR	ASYNC	Tx underrun	CTS underrun	not used	send break ack	DPLL error	not used	not used	not used
		BOP	Tx underrun	CTS underrun	frame complete	send SOM/ abort ack	DPLL error	Rx residual character length		
		BOP loop	Tx underrun	Loop sending	frame complete	send SOM/ abort ack	DPLL error	Rx residual character length		
		COP	Tx underrun	CTS underrun	frame complete	send SOM/ ack	DPLL error	not used	Rx hunt mode	Rx xpnt mode
1A/3Ah	ICTSR	all	C/T running	C/T zero count	delta DCD	delta CTS/LC	DCD	CTS/LC	GPI2	GPI1
1Bh	GSR	all	external or C/T status (chan B)	Rx/Tx status (chan B)	TxRDY (chan B)	RxRDY (chan B)	external or C/T status (chan A)	Rx/Tx status (chan A)	TxRDY (chan A)	RxRDY (chan A)
1C/3Ch	IER	all	DCD/CTS	TxRDY	TRSR[7:3]	RxRDY	RSR [7:6]	RSR [5:4]	RSR [3:2]	RSR [1:0]
1Dh	*REA*	all	reset internal A7 to 0							
1Dh	*CID*	all	chip identification							
1Eh	IVR	all	8-bit interrupt vector — unmodified							
1Fh	ICR	all	channel A/B interrupt priority		vector mode		bits to modify	vector includes status	chan A master int enable	chan B master int enable
3Dh	*SEA*	all	set internal A7 to 1							
3Eh	IVRM	all	8-bit interrupt vector — modified							
3Fh	MRR	all	master reset register (26C562/26562 only)							
02/22h	*IER1*	ASYNC	character compare	RTS negated	overrun	reserved	BRK end	BRK start	frame error	parity error
		BOP	EOM detect	ABORT detect	overrun	short frame	idle	flag detect	CRC error	RCL not zero
		BOP loop	EOM detect	EOP detect	overrun	short frame	turn-around det	flag detect	CRC error	RCL not zero
		COP	EOM det	PAD error	overrun	reserved	reserved	SYN det	CRC/LRC error	parity error
03/23h	*IER2*	ASYNC	Tx path empty	reserved	Tx underrun	CTS underrun	send BRK ACK	DPLL error	Δ CTS det	Δ DCD det
		BOP	Tx path empty	Tx frame complete	Tx underrun	CTS underrun	send SOM ack	DPLL error	Δ CTS det	Δ DCD det
		BOP loop	Tx path empty	Tx frame complete	Tx underrun	CTS underrun	send SOM ack	DPLL error	Δ CTS det	Δ DCD det
		COP	Tx path empty	Tx frame complete	Tx underrun	CTS underrun	send SOM ack	DPLL error	Δ CTS det	Δ DCD det
05/25h	*IER3*	all	ch master int enable	TxRDY int enable	RxRDY int enable	patt recog int enable	reserved	reserved	reserved	reserved
07/27h	*TRCR*	all	watchdog timer enable	DMA status byte enable	pattern recog 0 enable	pattern recog 1 enable	pattern recog 01 enable	extended int mask enable	extended bit rate enable	7-bit abort ena (BOP only)
0E/2Eh	*RFLR*	all	reserved	reserved	reserved	Rx FIFO fill level				
1C/3Ch	*FTLR*	all	TxFIFO threshold level				RxFIFO threshold level			
1E/3Eh	*TRMSR*	all	reserved	reserved	reserved	reserved	Tx path empty	pattern 0 status	pattern 1 status	pattern alt 0/1 status
1F/3Fh	*TELR*	all	reserved	reserved	reserved	TxFIFO empty level				

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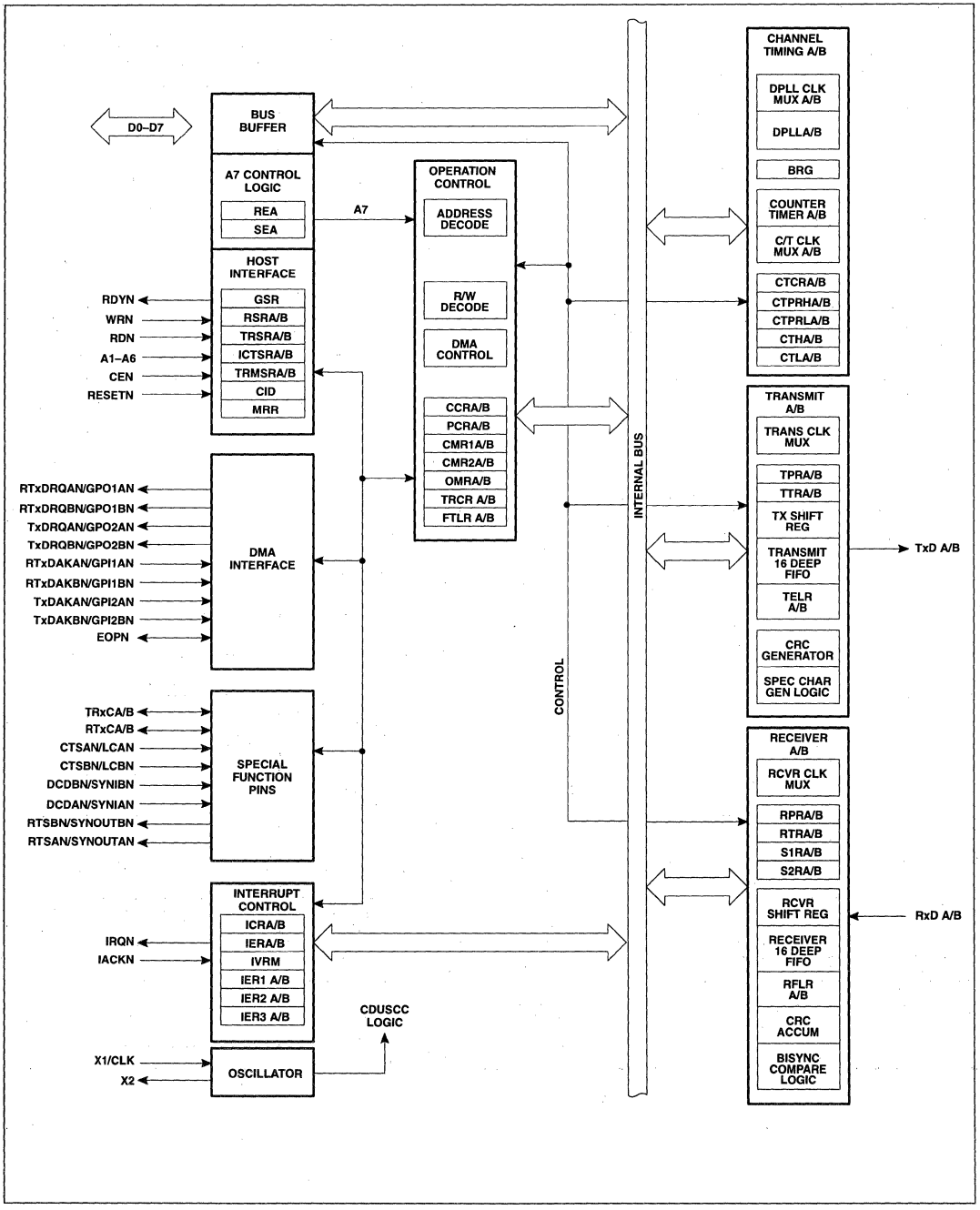
BLOCK DIAGRAM — SC26C562



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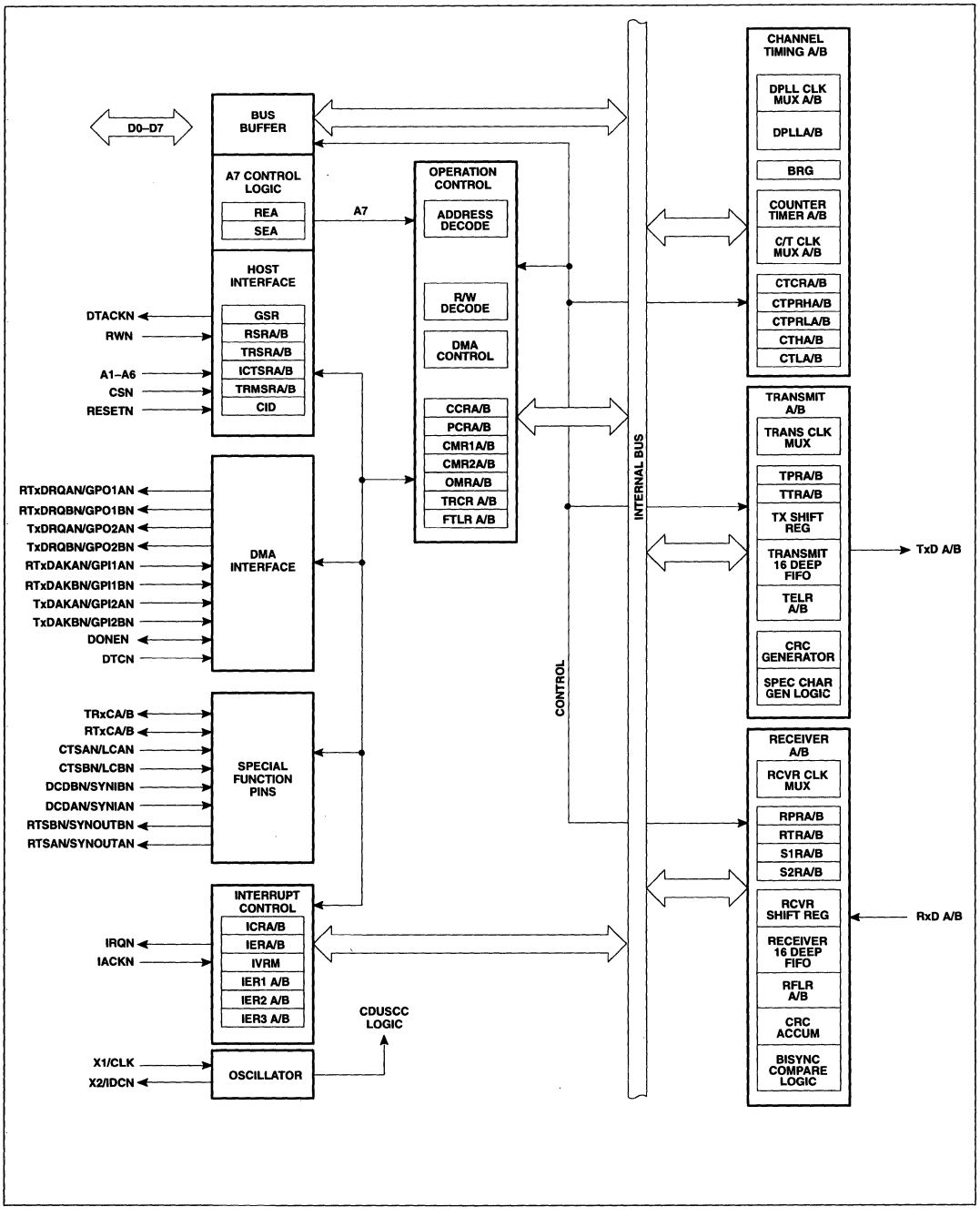
BLOCK DIAGRAM — SC68C562



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Philips Semiconductors

Data Communications

SECTION 2

PROTOCOL INDEPENDENT FEATURES

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STATUS

This group of registers define mechanisms for communications between the CDUSCC and the host processor and contain the CDUSCC status information. Selection of the CDUSCC 'Extended Mode' (via SEA) will alter both the number of registers in this group and functionality of the interface. Extended Mode provides the greater degree of flexibility and is recommended for all new designs. The 'Default Mode' has been provided to maintain software compatibility for NDUSCC drivers that must operate with CDUSCC components. Eight registers comprise this group which consists of the following:

- **Status Registers**
  - Default Mode
    GSR, RSRA/B, TRSRA/B, ICTSRA/B
  - Extended Mode
    GSR, RSRA/B, TRSRA/B, ICTSRA/B
    TRMSRA/B
- **Interrupt Control Registers**
  - Default Mode
    IERA/B, IVR, IVRM, ICR
  - Extended Mode
    IVR, IVRM, ICR, IER1, IER2, IER3

Status Registers

The status registers of CDUSCC have been organized with three objectives in mind:

- **'Quick Look' to minimize programmed I/O overhead**
- **Accumulation of data integrity status until reset (non-FIFOed status mode)**
- **Compatibility with NDUSCC**

The 'Quick Look' is provided by the General Status Register (GSR) which in a single byte provides information on both the A and B channels complete 'default mode' status (Figure 1). Since the state of all pertinent status bits are reflected in the GSR, it is usually not necessary to read the other status registers unless an error bit is set in the GSR bits [7:6] or [3:2].

The majority of status bits in all status registers except the GSR are NOT reset when the event that causes them ceases. Either the status bit must be reset directly by writing a '1' to that bit position of the status register, or indirectly by issuing a reset or similar action to the section controlling that bit (see detailed discussion in status register bit definitions). This was done so that in protocols where entire blocks (frames) of data are accepted or rejected as a whole, the need for status checking could be reduced to a single check at the end of the block. Of course the user must be careful to ensure that all status bits are reset prior to beginning the next block processing.

For FIFOed status bits, every RxFIFO read updates these bits based on the status of the current character on top of the RxFIFO. For non-FIFOed status bits, status of these bits is accumulated (ORed) unless they are cleared by writing '1' in the specific bit position in the appropriate registers or by resetting the receiver by CCR command.

By keeping the status bits associated to new CDUSCC enhancements in separate (TRMSRA/B) registers, software compatibility has been maintained with NDUSCC (Figure 2). The GSR[2] (Ch A) and GSR[6] (Ch B) reflect the status of TRMSR[3:0], TRSR[7:3] and RSR[7:0]. Thus, the GSR continues to provide a "quick look" status in the extended mode.

When operating in synchronous protocols with DMA, the user of CDUSCC has the option of enabling the DMA Frame Status Byte (DFSB). This byte will alleviate the need to check status registers by programmed I/O when DMA is used for data transfer. The status bits are appended onto a byte transferred to the host via DMA following the last data byte of the frame. The DFSB is fully described in the DMA section on page 548.

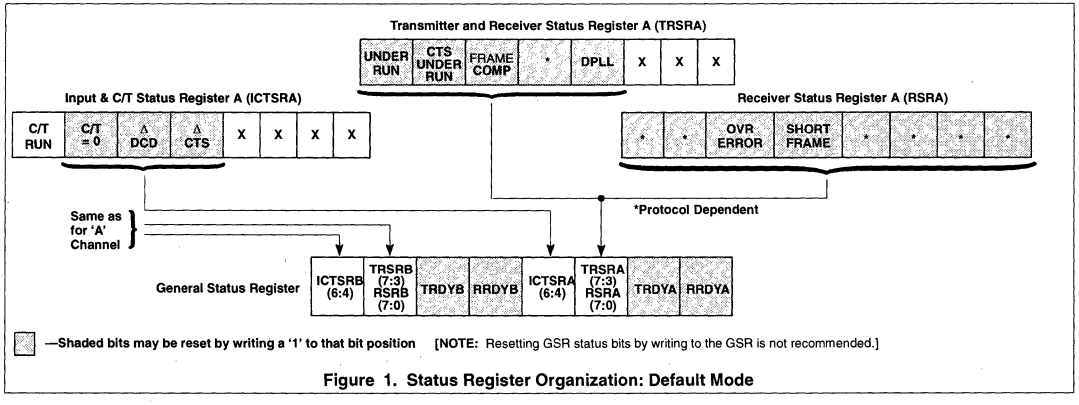

Figure 1. Status Register Organization: Default Mode

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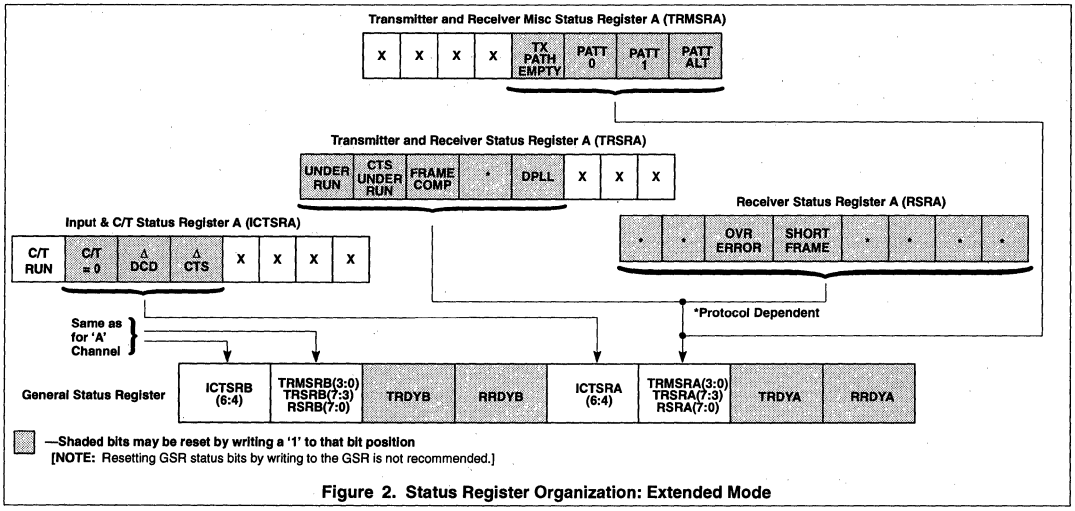
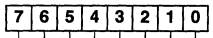


Figure 2. Status Register Organization: Extended Mode

Figure 3. GSR General Status Register [All Protocol Modes]



CHANNEL A

Ch. A RxRDY The assertion of this bit indicates that one or more characters are available in the Channel A receiver FIFO to be read by the CPU. This bit is also set when EOM or WDT bits are set. See OMR[3]. RxRDY is initially reset (negated) by a chip reset or when a 'reset channel A receiver' command is invoked.

Ch. A TxRDY The assertion of this bit indicates that one or more characters may be loaded into the channel A transmitter FIFO to be serialized by the transmit shift register. See description of OMR[4]. The true status of this bit can be read only when the transmitter is enabled. The ResetTx command (not the DisableTx command) initially clears the TxFIFO and the internal TxRDY signal. After the next EnableTx command, the then current status of the bit may be determined again by reading GSR.

Ch. A Rx/Tx status This bit indicates that one of the following status bits is asserted: RSRA[7:0], TRSRA[7:3], TRMSR[3:0]

Ch. A External or C/T status This bit indicates that one of the following status bits is asserted: ICTSRA[6:4].

CHANNEL B

Ch. B RxRDY The assertion of this bit indicates that one or more characters are available in the channel B receiver FIFO to be read by the CPU. See description of OMR[3]. This bit is also set when EOM or WDT bits are set. RxRDY is initially reset (negated) by a chip reset or when a 'reset channel B receiver' command is invoked.

Ch. B TxRDY The assertion of this bit indicates that one or more characters may be loaded into the Channel B transmitter FIFO to be serialized by the transmit shift register. See description of OMR[4].

Ch. B Rx/Tx status This bit indicates that one of the following status bits is asserted: RSRB[7:0], TRSRB[7:3], TRMSR[3:0]

Ch. B External or C/T status This bit indicates that one of the following status bits is asserted: ICTSRB[6:4].

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General Status Register (GSR)

This register provides a 'quick look' at the overall status of both channels of the CDUSCC. Resetting bits in the GSR can be achieved as follows: For TxRDY and RxRDY (Bits 5 and 1, or 4 and 0, respectively), writing a 'one' to that bit position of the GSR will reset the status bit. Multiple bits can be reset simultaneously, and writing 'one' to a bit position not set will have no effect. The other status bits are reset by resetting the individual status bits that they point to in the respective source register (RSR, TRSR, ICTSR, TRMSR).

CAUTION: The TxRDY and RxRDY bits in GSR are edge triggered and are not synchronized to a write operation to GSR. It is recommended that the GSR bits NOT be reset via a write operation when transmitter or receiver are active.

Receiver and Transmitter Status Registers (RSR, TRSR)

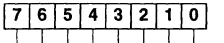
RSR informs the CPU of receiver status. Bits indicated as 'not used' in a particular mode will read as zero. The logical OR of these bits is presented in GSR[2] or GSR[6] (ORed with the bits of TRSR) for channels A and B, respectively. Unless otherwise indicated, asserted status bits are reset only by performing a write operation to the status register with the bits to be reset being ones in the accompanying data word, or when the RESETN input is asserted, or when a 'reset receiver' command is issued.

Certain status bits are specified as being FIFOed. This means that they occupy positions in a status FIFO that correspond to the data FIFO. As the data is brought to the top of the FIFO (the position read wen the RxFIFO is read), the FIFOed status bits are logically ORed with the previous contents of the corresponding bits in the status register. This permits the user to obtain status either character by character or on a block basis. For character by character status, the SR bits should be read and then cleared before reading the character data from RxFIFO. For block status, the status register is initially cleared and then read after the message is received. Asserted status bits can be programmed to generate an interrupt (see Interrupt Enable Registers).

TRSR informs the CPU of transmitter and receiver status. Bits indicated as not used in a particular mode will read as zero, except for bits [2:0], which may not be zero. The logical-OR of bits [7:3] is presented in GSR[2] or GSR[6] (ORed with the bits of RSR) for channels A and B, respectively. Unless otherwise indicated, asserted status bits are reset only:

1. By performing a write operation to the status register with the bits to be reset being ones in the accompanying data word [7:3].
2. When the RESETN input is asserted.
3. For [7:4], when a 'reset transmitter' command is issued.
4. For [3:0], when a 'reset receiver' command is issued.
5. For [2:0], see description in BOP mode.

Figure 4. ICTSRA (B) Input and Counter/Timer Status Register [All Protocol Modes]



GPI1, **GPI2** — These bits provide the current state of the channel's general purpose input pins. The bits' values are latched at the beginning of the read cycle.

CTS/LC, **DCD** — ICTSRx[3] reflects the state of the DCDxN input pin, while ICTSRx[2] reflects the state of CTSxN. When the bits are 0, the inputs are high, when they are 1, the pins are low. In SDLC loop mode, bit [2] reflects the state of LC output. Sampling method for the state of these pins is same as described for bits 4 and 5.

* **Delta CTS/LC** — When not in loop mode, the CTS input is sampled approximately every 6.8us using the 32X, 4800 baud output from the BRG. After synchronizing with the sampling clock, at least two consecutive samples at the same level are required to establish the level. As a consequence, a change of state at the CTS input, lasting at least 17us, will set this bit. The reset circuitry initializes the sampling circuits so that a change is not falsely indicated at power on time. The assertion of this bit causes an interrupt to be generated if the interrupt enable bit and the channel's master interrupt enable are asserted.

In SDLC loop mode, this bit is set upon transitions of the LC output. LC is asserted in response to the 'go on-loop' command when the receiver detects a zero followed by seven ones, and negated in response to the 'go off-loop' command when the receiver detects a sequence of eight ones.

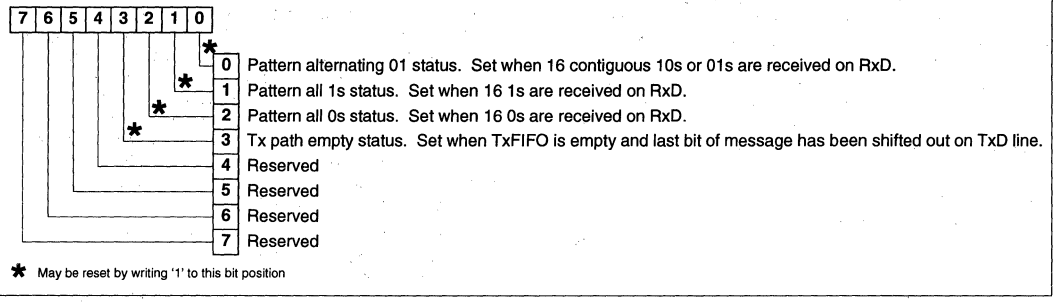
* **Delta DCD** — The DCD input is sampled approximately every 6.8us using the 32X, 4800 baud output from the BRG. After synchronizing with the sampling clock, at least two consecutive samples at the same level are required to establish the level. As a consequence, a change of state at the DCD input, lasting at least 17us, will set this bit. The reset circuitry initializes the sampling circuits so that a change is not falsely indicated at power on time. The assertion of this bit causes an interrupt to be generated if the interrupt enable bit and the channel's master interrupt enable are asserted.

* **C/T zero count** — Set when the counter/timer reaches zero count, or when the bit length measurement is enabled (CTCR [2:0] = 011) and the RxD input has returned High. The assertion of this bit causes an interrupt to be generated if CTCR[7] and the channel's master interrupt enable are asserted.

C/T running — Set when the C/T is started by start C/T command and reset when it is stopped by a stop C/T command.

* May be reset by writing '1' to this bit position

Figure 5. TRMSRA (B) Transmitter/Receiver Miscellaneous Status Register [All Protocol Modes]



Asserted status bits in [7:3] can be programmed to generate an interrupt. (See Interrupt Enable Registers.)

These registers have bit formats that vary with operating mode of the channel. Refer to the detailed operation descriptions of ASYNC, COP, BOP/BOPL modes in Section 3 for individual bit definition.

Input and Counter/Timer Status Register (ICTSRA, ICTSRB)

This register informs the CPU of status of the counter/timer and inputs. The logical-OR of bits [6:4] is presented in GSR[3] or GSR[7] for channels A and B, respectively. Bits [6:4] of the ICTSR are reset only:

1. By performing a write operation to the ICTSR with a '1' in the bits to be reset (ones in the accompanying data word).
2. When a Master RESET is issued (bits [7:4] only).

Transmitter/Receiver Miscellaneous Status Register (TRMSR)

This register provides pattern recognition status bits and Tx path empty status bit.

Tx Path Empty status bit (bit 3): This bit is set when the last bit of the data (ASYNC) or FLAG/SYN(SYN) is being shifted out of TxD while no more characters are in the FIFO or in the transmitter data path. A '1' written to this bit can clear the status bit. This bit is also cleared if the Rx RESET or Master RESET is issued.

Tx path is considered empty after at least one character has been transmitted and TxFIFO and TxSR are empty; in BOP mode, after the last bit of EOM flag is shifted out; in COP mode, after the last bit of FCS or last bit of first Mark character; in ASYNCHRONOUS mode, after last stop bit (1X mode) or last stop bit plus two transmit clocks (16X mode).

The Tx path empty status bit is not initially set until at least one data byte has passed through the transmitter path.

Pattern Recognition: The receiver can detect following patterns and generate interrupt (if enabled by IER3[4]) for the host through IRQN signal.

Pattern 0 status bit (bit 2): This bit is set when Rx receives 16 contiguous 0s after the pattern recognition is enabled. A '1' written to this bit can clear the status bit. This bit is also cleared if the Rx RESET or Master RESET is issued.

Pattern 1 status bit (bit 1): This bit is set when Rx receives 16 contiguous 1s after pattern recognition is enabled. A '1' written to this bit can clear the status bit. This bit is also cleared if the Rx RESET or Master RESET is issued.

Pattern alternating 01 status bit (bit 0): This bit is set when Rx receives 16 contiguous alternating 01 or 10 after pattern recognition is enabled. A '1' written to this bit can clear the status bit. This bit is also cleared if the Rx RESET or Master RESET is issued.

Use of the Status Registers

The host may generally keep informed of the CDUSCC's communication channel status by one of three methods:

1. Establish a polling loop in software
2. Enabling interrupts by CDUSCC when certain conditions are met
3. For synchronous protocols when DMA transfers are used, enabling the DMA Frame Status Byte (DFSB)

The method chosen depends upon many factors, including:

1. The number of channels to be serviced
2. The data rate of channels
3. The interrupt overhead of the host CPU
4. The amount of buffering interval to the communication channel
5. The non-communication processing requirements on the host CPU

In a polled system, the host CPU periodically reads the status registers of devices that may need service. In the CDUSCC, this register is the GSR. In one read operation, the host may obtain a summary of all enabled interrupt sources on CDUSCC. If an interruptible condition exists, the data in GSR will indicate which other status registers to read to get more detailed information:

1. RSRA or B for receivers
2. TRSRA or B for transmitters and receivers
3. ICTSRA or B for counter timer, modem control or external I/O
4. TRMSRA or B for Tx path empty and pattern recognition

If no interrupt conditions are seen in the GSR read, the host may continue the polling loop by reading a status register in another peripheral device.

INTERRUPTS

Interrupt Driven Systems

Most host CPUs have provision for temporarily suspending programmed flow and entering a new subprogram called an "interrupt service routine". This change of context can occur as a result of executing a particular instruction or, more normally, because an external "interrupt" input has been asserted. Before the interrupt service routine can be entered, the interrupting device and the type of interrupt must be determined unambiguously. Three commonly used methods for making the determination are:

1. In host CPUs with more than one interrupt input, the interrupting device may be determined by which pin the interrupt arrives on or as a coded value on these pins.
2. Once the interrupting device is determined, the interrupt details may be learned by reading the device's status register(s).
3. The interrupting device and possibly some details of the interrupt type may be determined by reading the byte or word returned by a special read cycle called an interrupt acknowledge cycle. This is commonly called a vectored interrupt system.

CDUSCC supports all these methods through the use of a single, open drain interrupt request output, general and specific status registers and the ability to respond to an IACK cycle with an "interrupt vector".

Interrupt Control

A single interrupt output (IRQN) is provided which is activated upon the occurrence of any of the following conditions:
Channel A external or C/T special condition,
Channel B external or C/T special condition,
Channel A Rx/Tx error or special condition,
Channel B Rx/Tx error or special condition,
Channel A TxRDY,
Channel B TxRDY,
Channel A RxRDY,
Channel B RxRDY.
Each of the above conditions occupies a bit in the general status register (GSR). If ICR[2] is set, the eight conditions are encoded into three bits which are inserted into bits [2:0] or [4:2] of the interrupt vector register. This forms the content of the IVRM during an interrupt acknowledge cycle. Unmodified and modified vectors can be read directly through specified registers. Two of the conditions are the inclusive OR of several other maskable conditions:

- External or C/T special condition: Delta DCD, delta CTS or C/T zero count (ICTSR[6:4]).
- Rx/Tx error or special condition: Any condition in the Receiver Status Register (RSR[7:0]) or a transmitter or DPLL condition in the transmitter and Receiver Status Register (TRSR[7:3]). The TxRDY and RxRDY conditions are defined by OMR[4] and OMR[3], respectively.

Also associated with the interrupt system are the Interrupt Enable Register (IER, IER1, IER2, IER3), one bit in the Counter/Timer Control Register (CTCR), and the Interrupt Control Register (ICR). In the default mode, the IER is programmed to enable specified conditions or groups of conditions to cause an interrupt by asserting the corresponding bit. A negated bit prevents an interrupt from occurring when the condition is active and hence masks the interrupt. In the extended mode, the bits of IER1, 2 and 3 provide finer resolution of interrupts. Asserting a bit in any of the IERs will allow the interrupt masked by that bit to cause an interrupt request (if master interrupt enable is set). In addition to the IER, CTCR[7] could be programmed to enable or disable an interrupt upon the C/T zero count condition. The interrupt priorities within a channel are fixed. Priority between channels is controlled by ICR[7:6]. Refer to Table 6 (page 546) and ICR[7:6] (Figure 9).

The ICR and IER3 contain the master interrupt enables for each channel (ICR[1] and ICR[0]) which must be set if the corresponding channel is to cause an interrupt. The CPU vector mode is specified by ICR[5:4] which selects either vectored or non-vectored operation. If vectored mode is selected, the content of the IVR or IVRM is placed on the data bus when IACK is activated. If ICR[2] is set, the content of IVRM is output which contains the content of IVR and the encoded status of the interrupting condition.

The SC26C562, upon receiving the first interrupt acknowledge edge, locks its current interrupt status until the end of the acknowledge cycles. Thereafter, the CDUSCC responds as mandated by ICR[5:4]. As shown in Figure 6, the internal interrupt priorities within a channel and among channels stabilize during the first IACKN. The leading edge of the second IACKN locks the interrupt status and allows the highest IVRM value to be placed on the data bus. The interrupt status is unlocked with the trailing edge of the last IACKN. Note that the interrupt request is inhibited during the IACKN sequence, this means that if the CDUSCC receives an IACKN sequence and it did not issue an interrupt request, it inhibits its interrupt request until the last IACKN is received (second IACKN in mode 0, third IACKN in modes 1 and 2, and trailing edge of IACKN in mode 3).

The SC68C562, upon receiving an interrupt acknowledge, locks its current interrupt status until the end of the acknowledge cycle (see Figure 7). If it has an active interrupt pending, it responds with the appropriate vector and then asserts DTACKN. If it does not have an interrupt, it propagates the acknowledge through its X2/IDCN output if this function is programmed in PCRA[7]; otherwise, the IACKN is ignored. Locking the interrupt

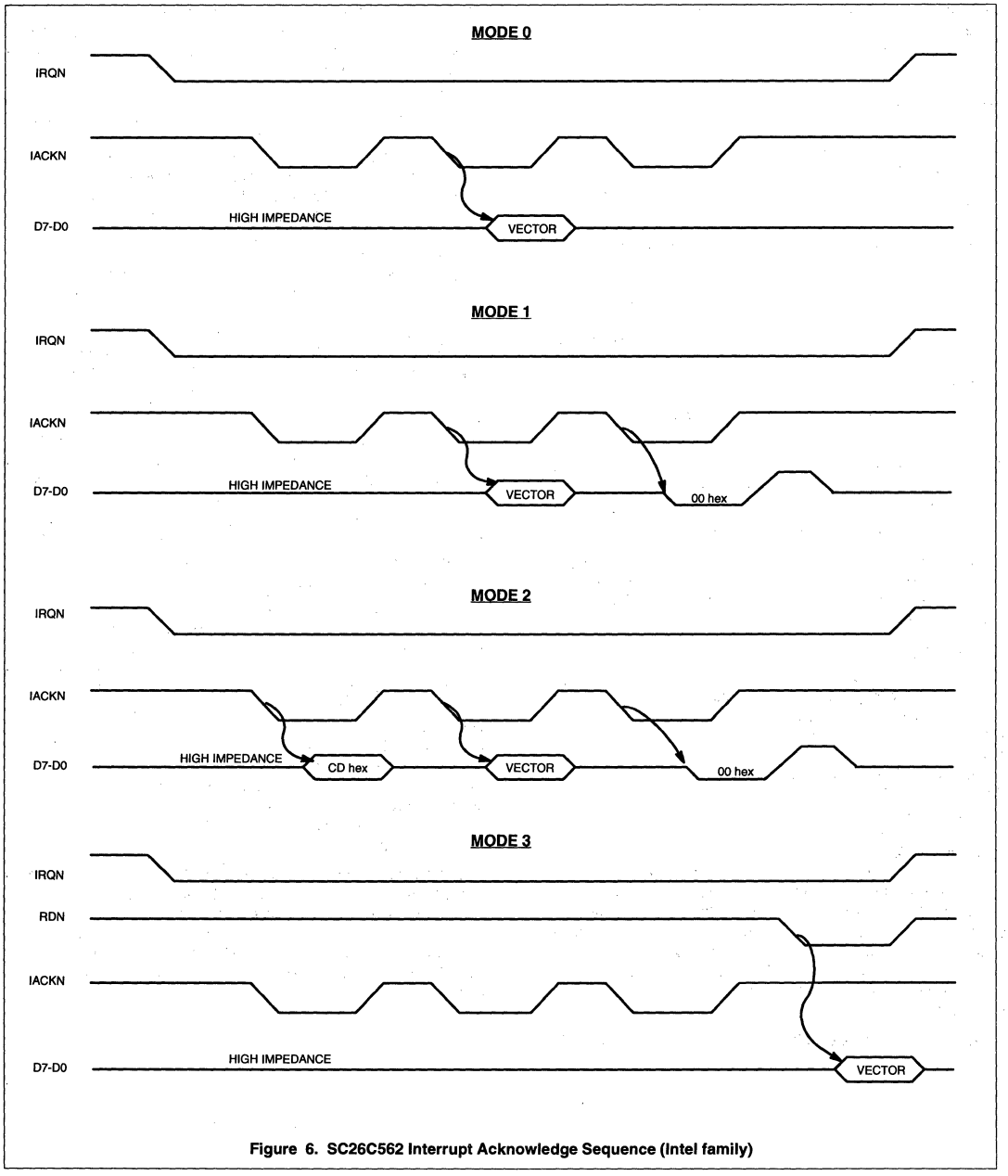


Figure 6. SC26C562 Interrupt Acknowledge Sequence (Intel family)

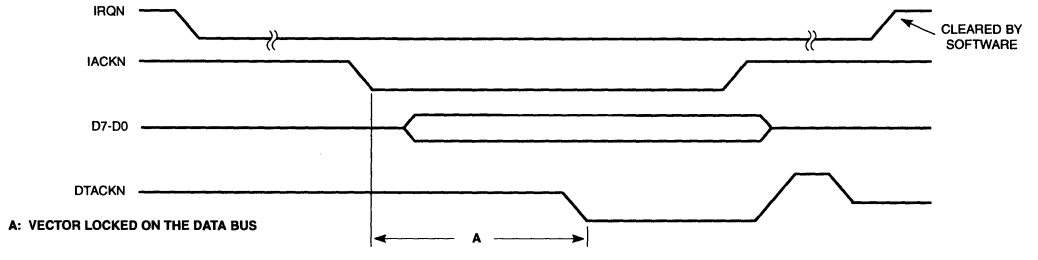


Figure 7. SC68C562 Interrupt Acknowledge Sequence (Motorola family)

status at the leading edge of IACKN prevents a device at a High position in the interrupt daisy chain from responding to an IACK issued for a lower priority device while the acknowledge is being propagated to that device.

CDUSCC Interrupt Modes

There are two major modes of interrupt generation and acknowledge in CDUSCC: Default and Extended.

The Default Interrupt Mode is fully NDUSCC compatible and is entered upon reset. The Extended Interrupt Mode is entered by setting the 'Extended Interrupt Mask Enable' bit in the Tx/Rx Command Register of the Extended register set (TRCR [2]). To return to the Default Interrupt Mode, TRCR[2] can simply be reset to '0'. In the Default Interrupt Mode not every interrupt source has a unique enable bit. Additionally, in the Default Interrupt Mode several 'Extended Mode' interrupt sources are not accessible for interrupt generation. It is recommended that the Extended Interrupt Mode be used for all new software development. The Extended Interrupt Mode provides more capabilities and a much finer level of control than the Default mode. Functions and controls in Default mode are not available in Extended mode and vice versa. Each mode provides a complete and workable interrupt context. Choice of mode is a matter of selecting how much interrupt support can or should be moved from the CPU's interrupt service routine to the CDUSCC hardware.

The ICR, Interrupt Control Register, and IVR/IVRM, Interrupt Vector Register (Modified), serve the same function in both modes.

The interrupt enable registers used by the two modes are different and disjoint as shown in Table 5. Use of the IER is mutually exclusive of IER1, 2 and 3.

Table 5. Interrupt Modes

Default	Extended
IERA,B	IER1A,B IER2A,B IER3A,B

The interrupt logic in CDUSCC is level sensitive in both Default and Extended Modes. This means that Interrupt Request (IRQN) will be asserted as long as a status bit capable of generating an interrupt remains set, and is gated 'thru' the appropriate Interrupt Enable Register. The interrupt acknowledge cycle does not reset any status bits. The interrupt service routine software must reset the appropriate status bit prior to concluding. If an interrupt is pending while interrupt is in progress on another interrupt, the IRQN line will remain asserted until the pending interrupt(s) is serviced. Level, not edge sensitive interrupt controllers, must be used to ensure that no interrupt requests are lost.

Default Interrupt Mode

This mode provides basic interrupt control and acknowledge for receivers, transmitters and modem controls. See Figures 9, 10, 12 and 13 for register bit formats and Figure 8 for register relationships. The transmit and receive status register formats are also shown for reference. Refer to the mode dependent sections for details on the bit definitions in these registers. For example, in Figure 2 GSR[2] is the logical OR of TRSRA[7:3], TRMSRA[3:0] and RSRA[7:0]. For example, on the A channel an interrupt to the host will occur:

If Channel 'A' Master Interrupt Enable is set (ICR[1]=1)

— AND —

If an Interrupt Enable (Mask) bit is set (IERA[7:0] or ICTSRA[6])

— AND —

A condition exists that will set a status bit in the general status register 'A' channel position (GSR[3:0])

Extended Interrupt Mode

The Extended Interrupt Mode provides an interrupt enable bit for virtually every status register bit which can indicate an interruptible condition. Figure 14 shows the relationship between the IER1-3 bits and corresponding bits in the status registers. Also, see Figures 11 through 13.

NOTE: ICR[1:0] and IER3[7] for A and B channels are redundant. This arrangement allows the master interrupt enables to be written without resorting to a command to reset the A7 address bit.

Use of the IER1-3 registers is straightforward. Setting an IER bit will enable generation of an interrupt if the master enable for the channel is also set. Figure 14 shows the definitions of all the IER bits for the Extended Interrupt Mode. The register bit descriptions for IER1 and IER2 which are protocol dependent appear in Section 3 in the context of each protocol.

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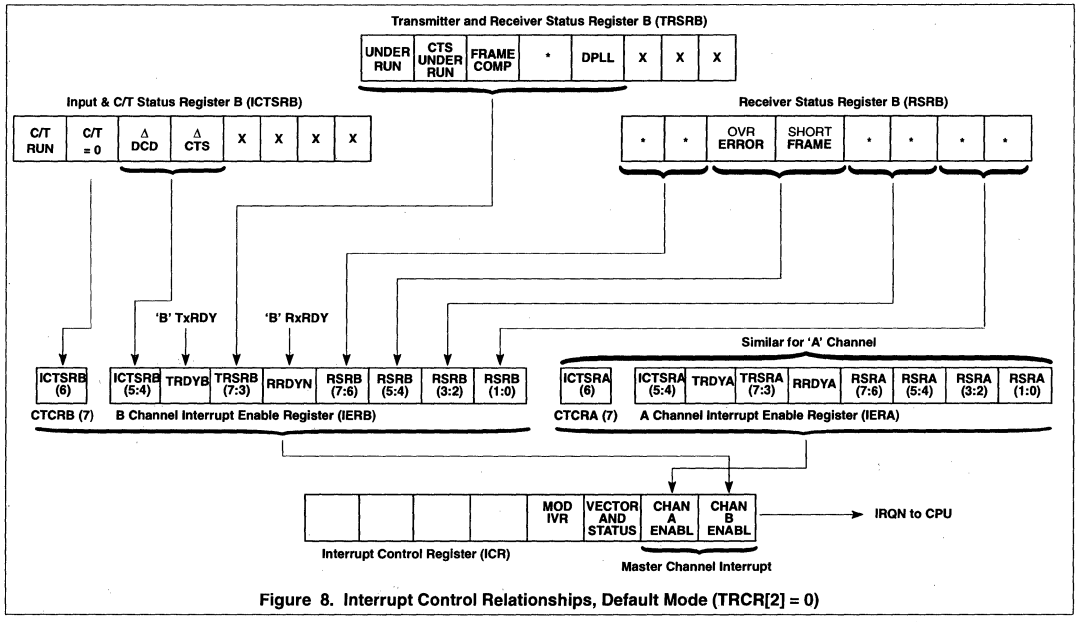


Figure 8. Interrupt Control Relationships, Default Mode (TRCR[2] = 0)

Figure 9. ICR Interrupt Control Register [All Protocol Modes]

7 6 5 4 3 2 1 0

— Channel B Master Interrupt Enable —

0 Channel B interrupts are disabled
1 Channel B interrupts are enabled

— Channel A Master Interrupt Enable —

0 Channel A interrupts are disabled
1 Channel A interrupts are enabled

— Vector Includes Status — Selects whether the modified (includes status) (IVRM) or unmodified vector (IVR) is output in response to an interrupt acknowledge (see Interrupt Vector Register).

0 Unmodified vector
1 Modified vector

— Vector Bits to Modify — Selects which bits of the vector stored in the IVR are to be modified to indicate the highest priority interrupt pending in the CDUSCC. See Interrupt Vector Register.

0 Modify bits 2:0 of the vector
1 Modify bits 4:2 of the vector

— Vector Mode — (Applies to SC26C562) The value of this field determines the response of the CDUSCC when an interrupt acknowledge sequence occurs: Interrupting bit(s) should not be reset before IACK cycle.

— For SC68C562 Vector Mode see note at bottom.

0 0 Vectored: 8XX86/88 Mode 0. In this mode, the CDUSCC expects two IACKNs. The bus is put in high impedance on the first IACKN. The vector is output on the second.

0 1 Vectored: 8080/8085 Mode 1. In this mode, the CDUSCC expects three IACKNs. The bus is put in high impedance on the first, the vector is output on the second, and on the third IACKN, the CDUSCC places H'00' on the data bus.

1 0 Vectored: 8080/8085 Mode 2. In this mode, the CDUSCC expects three IACKNs. A CALL instruction (H'CD') is placed on the data bus during the first, the vector is output on the second, and on the third IACKN, the CDUSCC places H'00' on the data bus.

1 1 Non-vectored: Non-vectored mode, mode 3. In this mode, the bus is put in high impedance during any IACKN sequence. The internal interrupt status is locked while a read of the IVR is performed. As in the vectored mode, interrupts are prioritized and if programmed accordingly, the vector is modified.

If an IACKN sequence is received for which there is no interrupt pending, the CDUSCC will place its data bus in 3-State during each IACKN assertion in modes 0 and I; in mode 2, a call instruction H'CD' is placed on the data bus during the first IACKN and it is placed in 3-State during the other two IACKNs. If an IACKN is received and the sequence is not completed, the next IACKN occurrence is considered the sequence continuation.

— Channel A/B Interrupt Priority — Selects the relative priority between channels A and B. The state of this bit determines the value of the interrupt vector (see Interrupt Vector Register). The priority within each channel, from highest to lowest, is as follows:

0 - Receiver ready
1 - Transmitter ready
2 - Rx/Tx status
3 - External or C/T status

0 0 Channel A: Channel A has the highest priority. The CDUSCC interrupt priorities from highest to lowest are as follows: A(0), A(1), A(2), A(3), B(0), B(1), B(2), B(3)

0 1 Channel B: Channel B has the highest priority. The CDUSCC interrupt priorities from highest to lowest are as follows: B(0), B(1), B(2), B(3), A(0), A(1), A(2), A(3)

1 0 Interleaved A: Priorities are interleaved between channels, but channel A has the highest priority between events of equal channel priority. The CDUSCC interrupt priorities from highest to lowest are as follows: A(0), B(0), A(1), B(1), A(2), B(2), A(3), B(3)

1 1 Interleaved B: Priorities are interleaved between channels, but channel B has the highest priority between events of equal channel priority. The CDUSCC interrupt priorities from highest to lowest are as follows: B(0), A(0), B(1), A(1), B(2), A(2), B(3), A(3)

NOTE: For 68C562, all three values of bits [5,4]00, 01, 10 will select single vector mode (see next page).

Vectored Mode (68C562)

Upon interrupt acknowledge, the DUSCC locks its current interrupt status until the end of the acknowledge cycle. If it has an active interrupt pending, it responds with the appropriate vector and then asserts DTACKN. If it does not have an interrupt, it propagates the acknowledge through its X2/IDCN output if this function is programmed in PCRA[7]. Otherwise, the IACKN is ignored. Locking the interrupt status at the leading edge of IACKN prevents a device at a High position in the interrupt daisy chain from responding to an IACK issued for a lower priority device while the acknowledge is being propagated to that device.

Interrupt Enable Register (IERA, IERB)

This register controls whether the assertion of bits in the channel's status registers causes an interrupt to be generated. An additional condition for an interrupt to be generated is that the channel's master interrupt enable bit, ICR[0] or ICR[1], be asserted. This register is used only in Default Interrupt Mode. For extended mode TRCR[2] is used to disable default mode.

Figure 10. IERA (B) Interrupt Enable Register [All Protocol Modes]

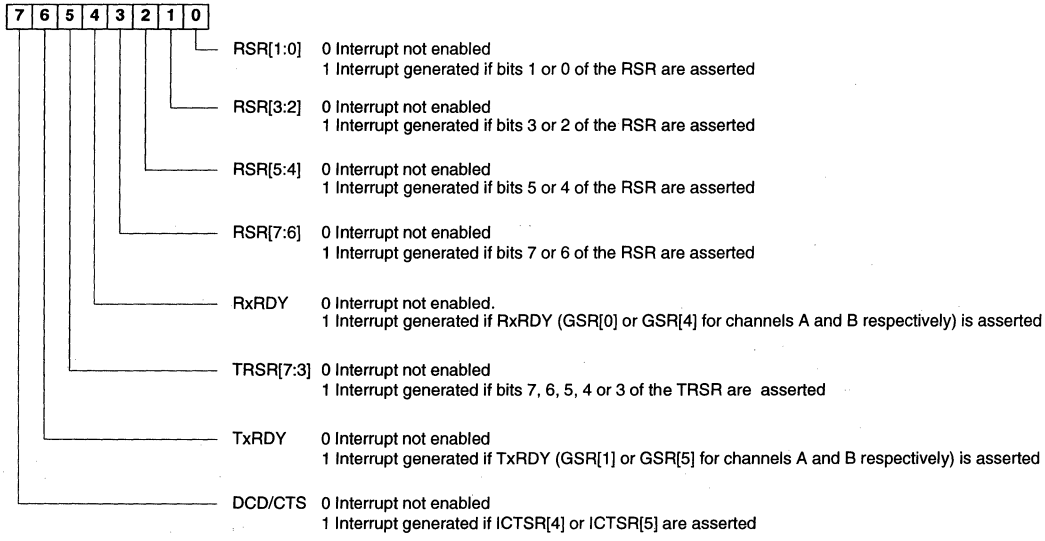
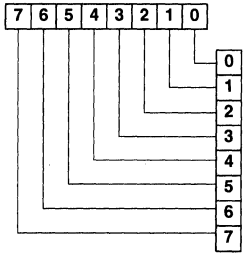


Figure 11. IER1,2,3A (B) Interrupt Enable Register 1,2,3 [All Protocol Modes]

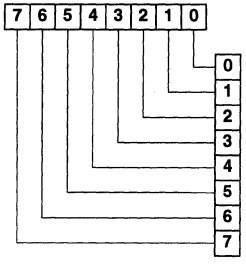
NOTE: IER1 and 2 are protocol mode sensitive, but they are shown here for illustration purpose. See Section 3 for protocol dependent features.

IER1A (B) Interrupt Enable Register 1



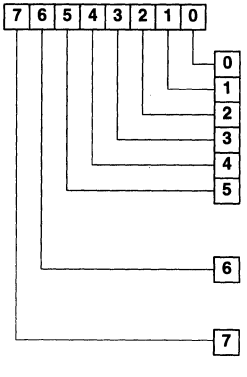
This register allows user to enable each individual status bit to cause interrupt. Writing '1' in the bit position will enable this feature. Master interrupt should also be enabled through ICR or IER3.

IER2A (B) Interrupt Enable Register 2



This register allows user to enable each individual status bit to cause interrupt. Writing '1' in the bit position will enable this feature. Master interrupt should also be enabled through ICR or IER3.

IER3A (B) Interrupt Enable Register 3



IER3 — Interrupt Enable Register 3. This register is active only when individual interrupt enable mode is selected, by setting TRCR[2] to '1'.

Interrupt Vector Register (IVR) and Modified Vector Register (IVRM)

Two separate but related registers are used to create vector values for interrupt vectoring.

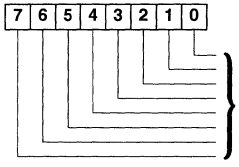
The IVR Register can be loaded by the CPU with an 8-bit vector value. This value will be output on the data bus when the CDUSCC receives an interrupt acknowledge cycle if the unmodified vector mode has been selected (ICR[2] = 0). The IVR Register can be read by the CPU by a bus read cycle at any time, regardless of if an interrupt is pending or not. The IVR is initialized to '0F' on master reset.

The IVRM Register will copy the value contained in the IVR Register, and modify either bits 2:0 or 4:2 to identify the highest priority interrupt currently active. The vector value is locked at the beginning of the IACK cycle until the cycle is completed. The vector in IVRM is not modified if unmodified vector mode has been selected (ICR[2] = 0), or regardless of the value of ICR[2] if the CPU has not written an initial vector into the IVR register. The value contained in the IVRM Register will be output on the data bus when the CDUSCC issues an interrupt acknowledge cycle if the modified vector mode has been selected (ICR[2] = 1). The IVRM Register can be read by the CPU at any time, but will always read as 'FF' if no interrupt is pending. If an interrupt is pending, the actual value of the IVRM will be read by the CPU. The vector value is locked at the beginning of the read cycle until the cycle is completed.

If 'vector includes status' is specified by ICR[2] = 1, bits [2:0] or [4:2] (depending on ICR[3]) of the vector are modified as shown in Table 6 to indicate the highest priority interrupt currently active. The priority is programmable through the ICR. This modified vector is stored in the IVRM. When ICR[2] = 1, the content of the IVRM is output on to the data bus on the interrupt acknowledge. The vector is not modified, regardless of the value of ICR[2], if the CPU has not written an initial vector into the IVR register.

Either the modified or unmodified vector can also be read by the CPU via a normal bus read cycle. The vector value is locked at the beginning of the IACK or read cycle until the cycle is completed. The contents of IVR may be read by a bus read cycle at any time, regardless if an interrupt is pending or not. IVRM always reads as H'FF' if no interrupt is pending. If an interrupt is pending, either the modified (for ICR[2] = 1) or the unmodified (for ICR[2] = 0) vector is placed on the data bus when reading IVRM.

Figure 12. IVR Interrupt Vector Register [All Protocol Modes]



If ICR[2] = 0, the content of the IVR register is output on the data bus when the CDUSCC has issued an interrupt request and the responding interrupt acknowledge (IACKN) is received. On master reset, IVR is initialized to '0F'

Figure 13. IVRM Interrupt Vector Modified Register [All Protocol Modes]

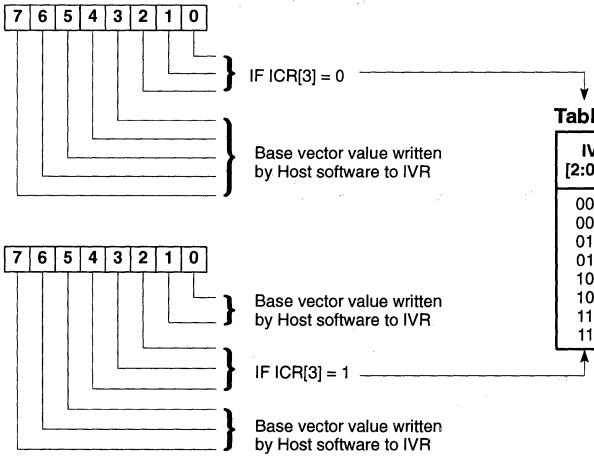


Table 6. Interrupt Status Encoding

IVRM [2:0]/[4:2]	Highest Priority Interrupt Condition
000	Chan. A receiver ready
001	Chan. A transmitter ready
010	Chan. A Rx/Tx status
011	Chan. A external or C/T status
100	Chan. B receiver ready
101	Chan. B transmitter ready
110	Chan. B Rx/Tx status
111	Chan. B external or C/T status

NOTE:
If ICR[2] = 0 the value contained in the IVRM is the same as the IVR.

If the CPU has not written an initial vector into the IVR register, the IVRM vector will not be modified and the value contained in the IVRM is 'FF'.

On Master Reset the value contained in the IVRM is initialized to 'FF'.

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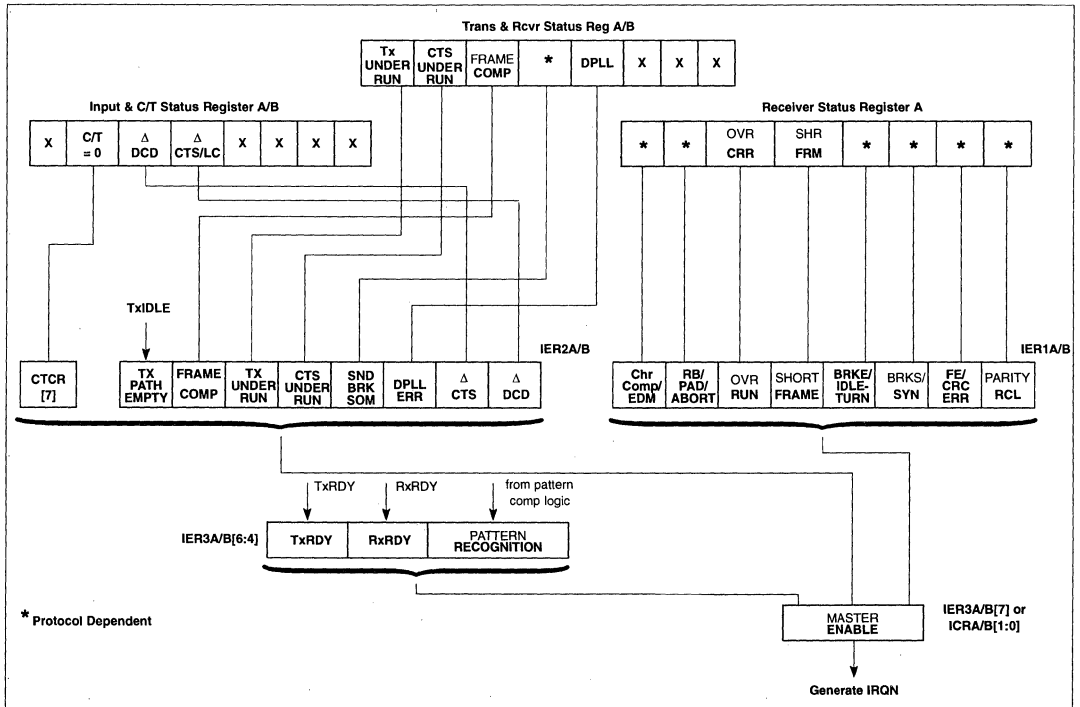

Figure 14. Interrupt Control Relationships, Extended Mode (TRCR[2] = 1)

DMA CONTROL

DMA Interface

The DMA control section provides the interface to allow the CDUSCC to operate with an external DMA controller. One of four modes of DMA can be programmed for each channel independently via CMR2[5:3]:

- Half-duplex single address. In this mode a single pin provides both DMA read and write requests. Acknowledgment of the requests is via a single DMA acknowledge pin. The data transfer is accomplished in a single bus cycle - the DMA controller places the memory address of the source or destination of the data on the address bus and then issues the acknowledge signal, which causes the CDUSCC to either write the data into its transmit FIFO (write request) or to output the contents of the top of the receive FIFO (read request). Transmit mode is selected by enabling the transmitter and receive mode is selected by enabling the receiver. This mode can be used when channel operation is half-duplex (e.g. BISYNC) and allows a single DMA channel to service the receiver and transmitter. The receiver and transmitter should not be enabled at the same time when half-duplex mode is programmed.

- Half-duplex dual address. In this mode, a single pin provides both DMA read and write requests. Acknowledgment of the request is via normal bus read and write cycles. The data transfer requires two bus cycles - the DMA controller acquires the data from the source (memory for a Tx DMA or CDUSCC for a Rx DMA) on the first cycle and deposits it at the destination (CDUSCC for a Tx DMA or memory for a Rx DMA) on the second bus cycle. This mode is used when channel operation is half-duplex (e.g., BISYNC) and allows a single DMA channel to service the receiver and transmitter. The receiver and transmitter should not be enabled at the same time when half-duplex mode is programmed.

Table 7. CDUSCC DMA Modes

4 Modes (Select via CMR2 [5:3]			
Single Address	Half Duplex	1 Request Pin	1 Acknowledge Pin
Dual Address	Half Duplex	1 Request Pin	PGM'd Acknowledge
Single Address	Full Duplex	2 Request Pin	2 Acknowledge Pins
Dual Address	Full Duplex	2 Request Pin	PGM'd Acknowledge

- Full-duplex single address. This mode is similar to half- duplex single address mode but provides separate request and acknowledge pins for the receiver and transmitter.

- Full-duplex dual address. This mode is similar to half- duplex dual address mode but provides separate request and acknowledge pins for the receiver and transmitter.

Figures 15 through 18 describe operation of the CDUSCC in the various DMA environments. Table 7 summarizes pins used for the

DMA request and acknowledge function for the transmitter and receiver for the different DMA modes.

The DMA request signals are functionally identical to the TxRDY and RxRDY status signals for each serial channel except that the DMA request signals are negated on the leading edge of the acknowledge cycle when the subsequent transfer causes the FIFO to become full (transmitter request) or empty (receiver request). In non-DMA operation, TxRDY and RxRDY signals are automatically negated only after the transfer is completed.

The DMA read request can be programmed through OMR[3] to be asserted either when any character is in the receive FIFO or only when the receive FIFO reaches threshold level. Likewise, the DMA write request can be programmed through OMR[4] to be asserted either when the transmit FIFO is not full or only when the transmit FIFO reaches threshold level. The request signals are automatically negated when the respective data transfer cycle is completed and the FIFO becomes full (transmitter request) or empty (receiver request). If a transfer is completed and the FIFO is not left full (transmitter) or empty (receiver), the request stays low. The request may be negated by the CPU with a status reset write cycle. Although EOPN terminates all DMA transfers, it has no effect on the requests.

The requests are a function of the FIFO status, but they can be negated by writing into the GSR. It is recommended that user should not write to GSR while transmitter or receiver are active. When the serial channel is not operating in DMA mode, the request pins for the channel can be programmed for other functions (see pin descriptions).

DMA (DONEN) EOPN Operation

The DMA completion I/O line is named EOPN for the 26C562 and DONE for the 68C562. The behavior of this bi-directional pin is essentially the same for either device. The terms EOPN and DONE are interchangeably used in the following text.

As an input, EOPN is asserted by the DMA controller concurrent with the corresponding DMA acknowledge to indicate to the CDUSCC that the character being transferred into the TxFIFO is the last character of the transmission frame. In synchronous modes, the CDUSCC can be programmed through TPR[4] to automatically transmit the frame termination sequence (e.g., FCS-FLAG in BOP mode) upon receipt of this signal.

As an output, EOPN is asserted by the CDUSCC under the following conditions:

a. In response to the DMA acknowledge for a receiver DMA request if the FIFO'd RECEIVED EOM status bit (RSR[7]) is set for the character being transferred. In async mode, RSR[7] (= char. complete) does not assert EOPN.

b. In response to the DMA acknowledge for a transmitter DMA request if the counter/timer has been programmed to count transmitted characters and the terminal count has occurred.

If short frame/Abort on DONEN(EOPN) mode is used, a short frame will set DONE(EOPN) but it will not set EOM flag in status register (RSR[7]). (See CCR Commands for DMA, Table 13 on page 570.)

DMA Frame Status Byte (DFSB)

In synchronous modes of receive operation with DMA transfers to the host, the DFSB offers an efficient method of acquiring the receive status bits for an entire DMA block. The DFSB will allow the host to obtain status information for a frame in a single byte rather than reading RSR and TRSR after every character. The DFSB is accumulated in a register as frames are received. It is updated frame by frame by logically ORing the present status byte for the frame into the DFSB. The DFSB, therefore, contains a running summary of all frame status bytes (see Table 8).

When this mode is enabled by programming TRCR[6] = 1, the DFSB will be output after the last data character of the block. The status bits for the last data byte will be attached to that byte except EOM. Status bits FIFOed with the DFSB byte are ignored except EOM, Overrun and DPLL error. The byte containing the DFSB will have the EOM status bit set. The EOPN will not be set until DFSB pops to the top of the RxFIFO.

An ABORT condition can cause the DMA frame to be closed if CCR command 'EDONE' is used.

If 'EDONE' command (Table 13 on page 570) and DFSB are enabled (TRCR[6] = 1), then an 'ABORT detect' condition will push contents of DFSB into RxFIFO and DFSB will be cleared for next frame. If DFSB is not enabled (TRCR[6] = 0), a dummy byte is pushed into RxFIFO. Whenever either the DFSB or dummy byte pop to the top of the RxFIFO, the DONE(EOPN) signal will be asserted.

If 'EDONE' command is not enabled, a dummy byte is pushed into the RxFIFO on 'ABORT detect' condition irrespective of DFSB enable or disable (TRCR[6]). If DFSB is enabled, it is not cleared and its contents are accumulated with next frame.

A 'short frame' condition will also cause DFSB to be pushed into RxFIFO if 'EDONE' command and DFSB (TRCR[6]) are enabled. When DFSB reaches the top of the RxFIFO, it will generate DONEN(EOPN) signal.

Table 8. DFSB Bit Formats

	7	6	5	4	3	2	1	0
COP	Reserved			PAD error	DPLL error	OVERRUN error	BCC* error	Parity error
Status Register Reference				RSR[6]	TRSR[5]	RSR[5]	RSR[1]	RSR[0]
BOP/BOPL	Residual Character Length			ABORT	DPLL error	OVERRUN error	CRC error	Short Frame
Status Register Reference	TRSR[2:0]			RSR[6]	TRSR[3]	RSR[5]	RSR[1]	RSR[4]
* The BCC error for non-BISYNC COP mode is only valid when EOM is generated due to C/T timeout.								

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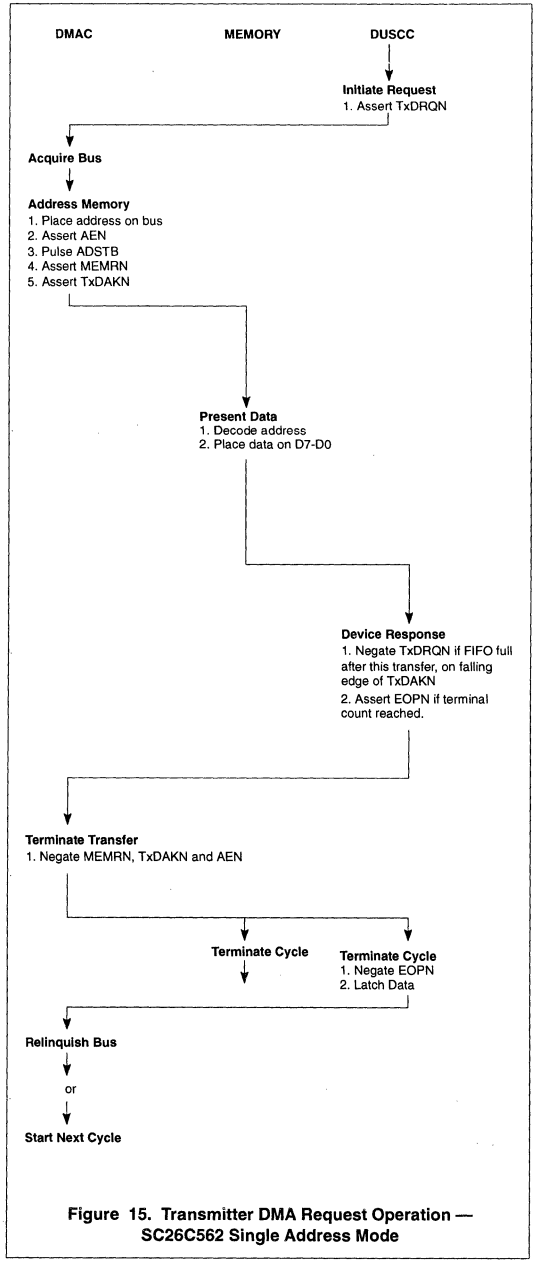

Figure 15. Transmitter DMA Request Operation — SC26C562 Single Address Mode

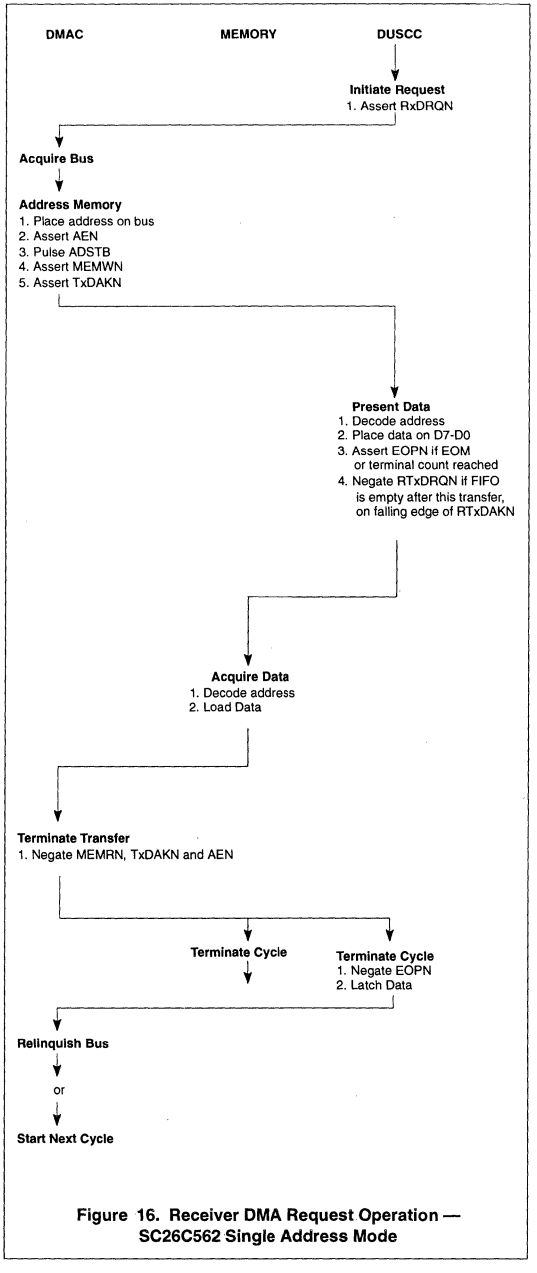

Figure 16. Receiver DMA Request Operation — SC26C562 Single Address Mode

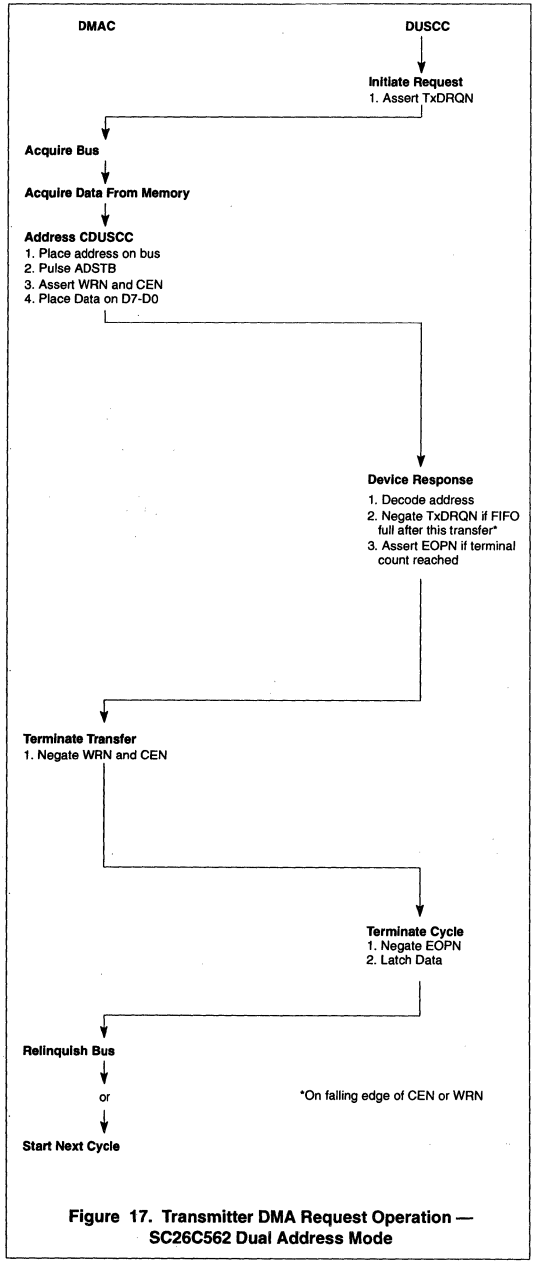

Figure 17. Transmitter DMA Request Operation — SC26C562 Dual Address Mode

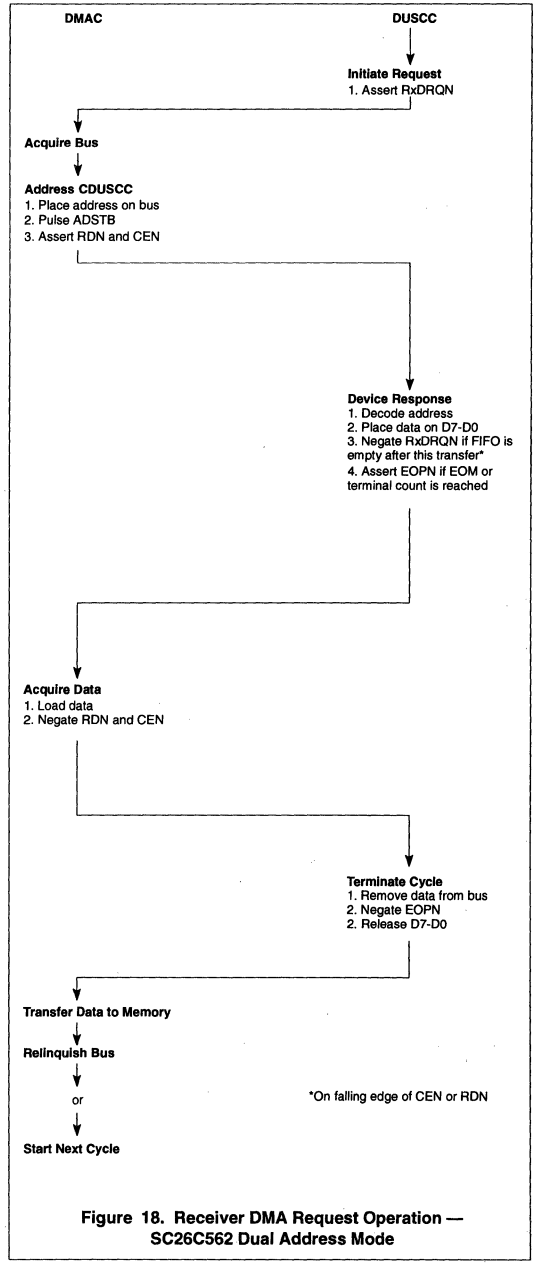

Figure 18. Receiver DMA Request Operation — SC26C562 Dual Address Mode

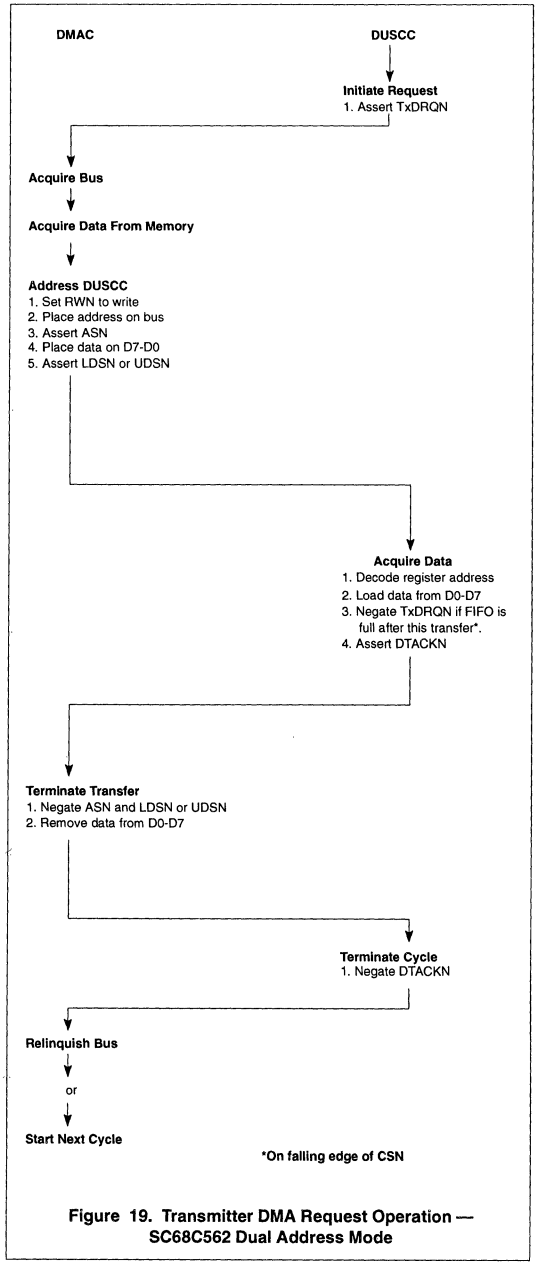

Figure 19. Transmitter DMA Request Operation — SC68C562 Dual Address Mode

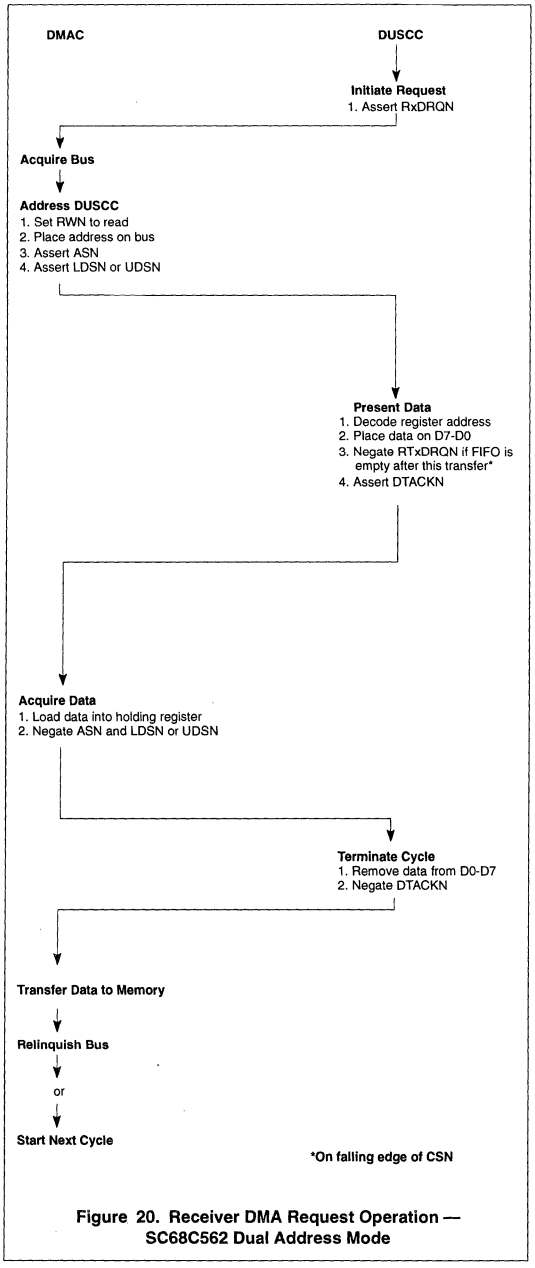

Figure 20. Receiver DMA Request Operation — SC68C562 Dual Address Mode

CMOS DUSSC User's Guide

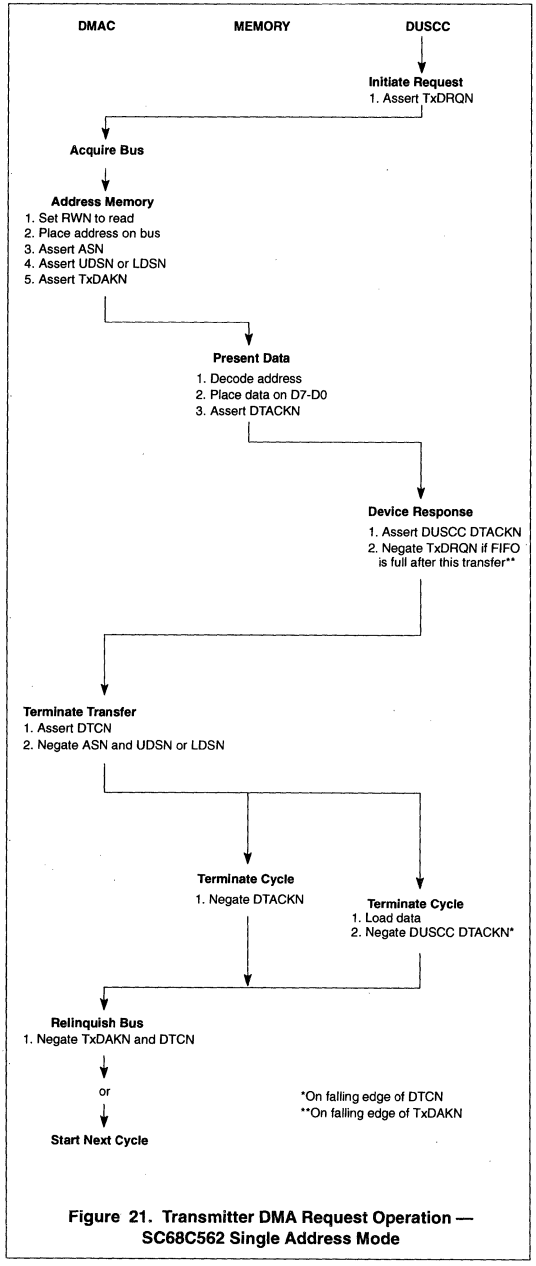

Figure 21. Transmitter DMA Request Operation — SC68C562 Single Address Mode

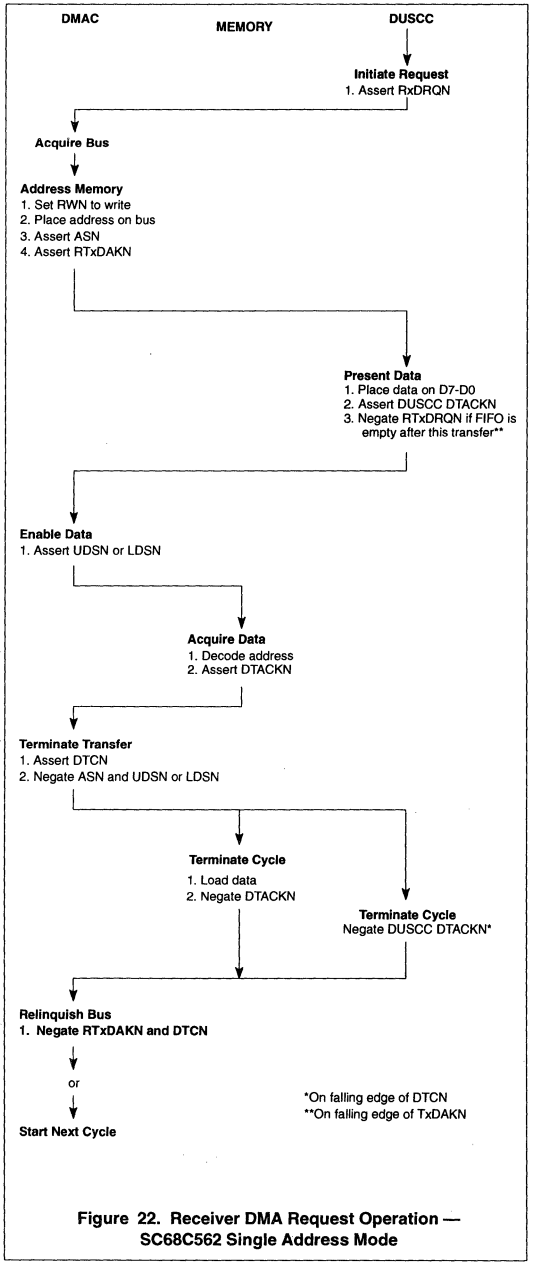

Figure 22. Receiver DMA Request Operation — SC68C562 Single Address Mode

FIFOs

Each channel's transmitter and receiver is buffered by a FIFO with a depth of 16 characters. The FIFO helps to match differences in data transfer rates between the serial channels and the host interface. The FIFOs also provide the storage area that makes burst DMA transfers feasible.

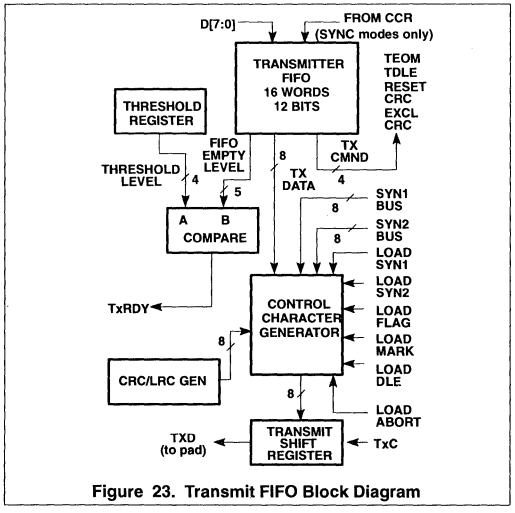

Figure 23. Transmit FIFO Block Diagram

TxFIFO

The major blocks associated with the transmitter FIFO are shown in Figure 23. The TxFIFO is partitioned into words consisting of 8 bits of character data and 4 bits of command code. The FIFO is 16 words deep. The character data is provided by the host interface or via a DMA transfer using the D[7:0] data bus. The TxFIFO may be addressed at any of four consecutive locations (see Table 1) to allow use of multiple byte/word instructions (however, only one byte is transferred to the FIFO at a time). A write to any valid address always writes data to the next empty FIFO location (individual byte locations cannot be accessed in the TxFIFO).

In synchronous modes, the remaining 4 bits are used to append transmit command codes to particular data characters.

These 4 bit 'command codes' associated with each data byte are invoked via the Channel Command Register (CCR), Table 13. The commands associated with each data byte will travel with that data byte down the FIFO for execution before or after the serialization of data byte.

The command FIFO is capable of appending more than one command to a particular data character. A command appended to a character may be executed before, during or after transmission of the character. An example of this is EOM appended to the last character of a message. The last character is transmitted before the EOM activates closing the frame and the message. Likewise, exclude CRC command is executed before the appended character. Refer to Table 13.

TxFIFO output data may be moved to the Transmit Shift Register without modification, always the case in the asynchronous mode, or may be modified or replaced by the Control Character logic. This logic inserts special characters, i.e., SYN or DLE, to support the various synchronous protocols.

The character to be transmitted is shifted out, one bit at a time (LSB first) from the transmit shift register. The TxC, transmitter clock, selected from numerous sources is the shift clock for the transmit shift register.

Data Transfer to TxFIFO

The TxRDY flag (GSR[1] or GSR[5] is used to indicate that the TxFIFO has room to accept data from the host. Initially the TxRDY does not become valid until the transmitter is enabled. Characters can be loaded into the TxFIFO prior to the initial enabling of the transmitter, however this is not recommended, due to the possibility of writing data to a full TxFIFO which would result in data loss. If data is transferred to the TxFIFO prior to the initial enabling of the transmitter, the only indication of space available in the TxFIFO is via reading the TxFIFO empty level register (TELR). The TxRDY flag initially becomes valid once the transmitter has been enabled. The TxRDY flag will remain valid if the transmitter is disabled only if the TxFIFO was not empty prior to disabling the transmitter. If the TxFIFO is allowed to become empty while the transmitter is disabled, the TxRDY flag will again become invalid. When the TxRDY flag is invalid, the state of the flag is unasserted (0) even though the TxFIFO is not full.

Once TxRDY is asserted, the CDUSCC does not clear it automatically until the TxFIFO is full. The host may reset TxRDY by a status reset write cycle to the GSR. If the host clears the TxRDY bit, it will re-assert when the TxFIFO threshold criteria is next satisfied. Due to the possibility of the host resetting the TxRDY simultaneously with the CDUSCC attempt to set the TxRDY, host clearing of the TxRDY flag via writing to the GSR is not recommended if the transmitter is active.

TxFIFO Threshold Criteria

The TxFIFO is always present in the data path as a 16-byte deep FIFO. The TxRDY assertion can be programmed to occur at any level (number of empty bytes) in the TxFIFO. The Output and Miscellaneous Register (OMR) selects which of two threshold criteria are to be used. TxRDY assertion depends on the state of OMR[4]:

1. If OMR[4] is 0, TxRDY is asserted whenever there is any space in the TxFIFO. If it is not reset by the host, TxRDY remains asserted until the TxFIFO becomes full, at which time it is automatically negated. If it is reset by the host, it will remain negated, regardless of the current state of the TxFIFO, until a new character is transferred to or from the TxFIFO.

2. If OMR[4] is 1, TxRDY is asserted whenever the number of empty locations in the TxFIFO is equal to or greater than the threshold level specified in the FIFO Threshold Level Register (FTLR). If it is not reset by the host, TxRDY remains asserted until the TxFIFO becomes full, at which time it is automatically negated. If it is reset by the host, it will remain negated, regardless of the current state of the TxFIFO, until sufficient characters are transferred from the TxFIFO to the TxSR so that the number of empty locations in the TxFIFO is equal to or greater than the level specified in the FTLR.

CAUTION: Re-setting TxRDY by the host writing to the GSR is not recommended. See GSR description (page 536).

The assertion of TxRDY can generate an interrupt if the proper interrupt enables are set. Refer to the section on Interrupts for details.

If DMA operation is programmed, either RTxDRQN (half-duplex) or TxDRQN (full-duplex) follows the state of TxRDY. These operations differ from normal TxRDY in that the request signal is negated on the leading edge of the DMA acknowledge write cycle when the subsequent transfer causes the transmit FIFO to become full, while the TxRDY signal is negated only after the transfer is completed.

Underrun status TRSR[7] set indicates that one or more data characters (not PAD characters) have been transmitted and the TxFIFO and TxSR are both empty.

In 'wait on Tx' (CMR2 [5:3] = 101 or 110), a write to a full FIFO causes the write cycle to be extended until a FIFO position is available. RDYN (for 26C562) or DTACKN (for 68C562) is asserted to extend the cycle, and negates when a FIFO position becomes available. In non wait modes, write to a full FIFO is not allowed. Data on the top of the TxFIFO may be lost if it is overwritten and no indication of this occurrence is provided.

The TxFIFO is cleared on Master RESET, or by a reset transmitter or transmit ABORT/BREAK command. Disabling the transmitter does not affect the TxFIFO.

RxFIFO

The major blocks associated with the receiver FIFO are shown in Figure 24.

The RxFIFO is partitioned into words consisting of 8 bits of character data and 9 bits of status information. The FIFO is 16 words deep. The character data inputs are always from the RxSR, Receive Shift Register, except at the end of a DMA frame in some of the synchronous modes. Here, an optional DFSB, DMA Frame Status Byte,

may be output as the last character of the DMA block. The DFSB is a running accumulation (logical OR) of all the status bits received during the DMA block. Refer to the DFSB description or the BOP/COP detailed operation section for more details.

The status bits for each received character are FIFO'd with the data. These bits are character count complete indication (all protocol modes), character compare indication (ASYNC), EOM indication (BISYNC/BOP), and parity, framing, and CRC errors.

Caution must be exercised when reading RxFIFO and Status Registers (RSR, TRMSR) back-to-back. For some versions of CDUSCC of course, it is possible that fast host processor I/O, meeting the minimum AC timing specifications of CDUSCC, could attempt to access status information before that information has been established at the top of the FIFO. Refer to the latest "Device Variances and Design Cautions" sheet for more information.

Data is loaded into the RxFIFO from the RxSR and extracted (read) by the host or DMA controller via the data bus. A RxFIFO read creates an empty RxFIFO position for new data from the RxSR. RxRDY assertion depends on the state of OMR[3]:

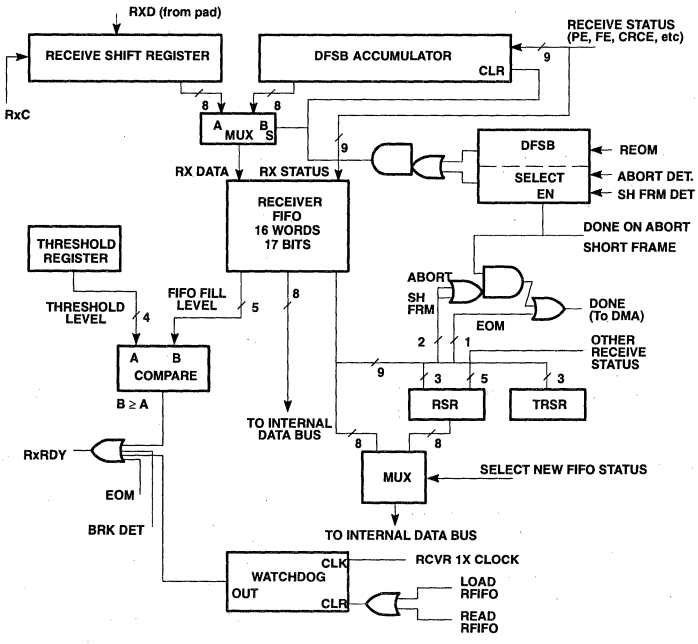

Figure 24. Receive FIFO Block Diagram

1. If OMR[3] is 0 (FIFO not empty), RxRDY is asserted each time a character is transferred from the receive shift register to the receive FIFO. If it is not reset by the host, RxRDY remains asserted until the receive FIFO becomes empty, at which time it is automatically negated. If it is reset by the host, it will remain negated, regardless of the current state of the receive FIFO, until a new character is transferred from the RxSR to the RxFIFO, or WDT is timed out.

2. If OMR[3] is 1 (FIFO full), RxRDY is asserted:
   a. When a character transfer from the receive shift register causes fill level to reach threshold level for RxFIFO.
   b. When a character with a tagged EOM status bit is loaded into the FIFO (BISYNC or BOP) regardless of RxFIFO full condition.
   c. When the counter/timer is programmed to count received characters and the character which causes it to reach zero count is loaded into the FIFO (ICTSR [6]).
   d. When the beginning of a break is detected in ASYNC mode regardless of the RxFIFO full condition.
   e. When WDT times out.

If it is not reset by the host, RxRDY remains asserted until the FIFO becomes empty, at which time it is automatically negated. If it is reset by the host, it will remain negated regardless of the current state of the receive FIFO, until it is asserted again due to one of the above conditions.

CAUTION: Re-setting TxRDY by the host writing to the GSR is not recommended. See GSR description (page 536).

The assertion of RxRDY causes an interrupt to be generated if IER[4], IER3[5] and the channel's master interrupt enable (ICR[0], ICR[1], or IER3[7]) are asserted.

When DMA operation is programmed, the RxRDY status bit is routed to the DMA control circuitry for use as the channel receiver DMA request. Assertion of RxRDY results in assertion of RTxDRQN output.

Several status bits are appended to each character in the RxFIFO. When the FIFO is read, causing it to be 'popped', the status bits associated with the new character at the top of the RxFIFO are logically ORed into the RSR. Therefore, the user should read RSR before reading the RxFIFO in response to RxRDY activation. If character-by-character status is desired, the RSR should be read and cleared each time a new character is received. The user may elect to accumulate status over several characters or over a frame by clearing RSR at appropriate times.

In 'wait of Rx' mode, a read of empty FIFO causes the read cycle to be extended until a character is available in the FIFO. RDYN (for 26C562) or DTACKN (for 68C562) is asserted to extend the cycle. If wait mode as specified in CMR2[5:3] is not being used, a read of empty RxFIFO is not allowed.

In all protocol modes, the CDUSCC protects the contents of the FIFO and the RxSR from overrun. If a character is received while the FIFO is full and a character is already in the RxSR waiting to be transferred into the FIFO, the overrunning character is discarded and the OVERRUN status bit (RSR[5]) is asserted. If the overrunning character is an end-of-message character, the character is lost but the FIFO'd EOM status bit will be asserted when the character in the RxSR is loaded into the FIFO.

The RxFIFO is cleared on master reset, or by a reset receiver command. Disabling the receiver does not effect the RxFIFO, RxRDY or DMA request operations.

The FIFO Level Registers

The CDUSCC provides a set of registers that allows reading the current levels of the Tx and Rx FIFOs. Another register allows users to control TxRDY and RxRDY generation by comparison of current FIFO level to a programmable limit. TELR register (Figure 25) indicates the TxFIFO empty level, RFLR register (Figure 26) indicates the RxFIFO fill level and FTLR register (Figure 27) is used to set threshold levels for TxRDY and RxRDY signals.

Figure 25. TELRA (B) TxFIFO Empty Level Register [All Protocol Modes]

TxFIFO Empty Level Register (TELRA,TELRB) indicates the TxFIFO empty level. A read from this register returns the count on available empty locations in the channel's TxFIFO.

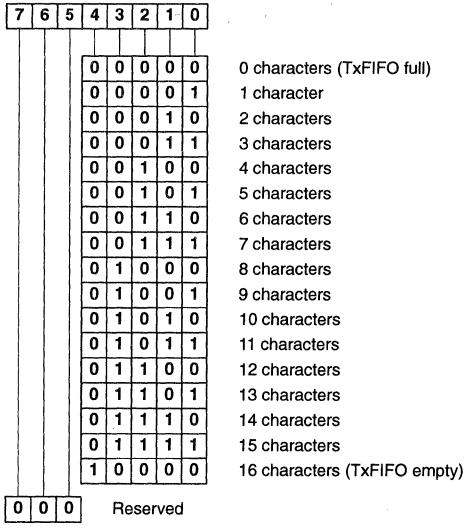

Figure 26. RFLRA (B) RxFIFO Filled Level Register [All Protocol Modes]

RxFIFO filled Level Register (RFLRA,RFLRB) indicates the RxFIFO fill level. A read from this register returns the count on available characters in the channel's RxFIFO.

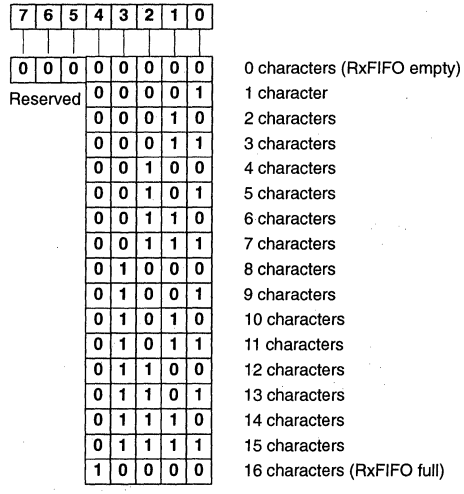

Figure 27. FTLRA (B) FIFO Threshold Level Register [All Protocol Modes]

7	6	5	4	3	2	1	0

FIFO Threshold Level Register (FTLRA, FTLRB) controls both TxFIFO and RxFIFO interrupt threshold levels.

— **RxFIFO Threshold Level** — This field controls the RxFIFO threshold level. When RxFIFO is filled to the threshold level, RxRDY status bit will be asserted.

0	0	0	0	1 byte (only one space available)
0	0	0	1	2 bytes
0	0	1	0	3 bytes
0	0	1	1	4 bytes (default mode, set by reset)
0	1	0	0	5 bytes
0	1	0	1	6 bytes
0	1	1	0	7 bytes
0	1	1	1	8 bytes
1	0	0	0	9 bytes
1	0	0	1	10 bytes
1	0	1	0	11 bytes
1	0	1	1	12 bytes
1	1	0	0	13 bytes
1	1	0	1	14 bytes
1	1	1	0	15 bytes
1	1	1	1	16 bytes

— **TxFIFO Threshold Level** — This field controls the TxFIFO threshold level. When TxFIFO is emptied below threshold level, TxRDY status bit will be asserted.

0	0	0	0	1 character
0	0	0	1	2 characters
0	0	1	0	3 characters
0	0	1	1	4 characters (default mode, set by master reset)
0	1	0	0	5 characters
0	1	0	1	6 characters
0	1	1	0	7 characters
0	1	1	1	8 characters
1	0	0	0	9 characters
1	0	0	1	10 characters
1	0	1	0	11 characters
1	0	1	1	12 characters
1	1	0	0	13 characters
1	1	0	1	14 characters
1	1	1	0	15 characters
1	1	1	1	16 characters

TIMERS AND TIMING REGISTERS

Watchdog Timer

The CDUSCC contains a 7-bit 'watchdog' timer (WDT) for each receiver channel. If the RxFIFO threshold criteria have not been met, it is possible that data could be left in the RxFIFO with no indication to the host. This is very likely in asynchronous serial formats, since no 'end of message' identifier exists and the final characters of the message might be fewer than the RxFIFO threshold level. In most synchronous formats, the 'end of message' identifier will automatically cause assertion of RxRDY regardless of threshold criteria. [CAUTION: COP protocols with the exception of BiSync, have no specific end of message identifier.] The WDT can be used to prevent data remaining in the RxFIFO from becoming 'stale'.

The WDT functions by counting receiver clock cycles occuring since the last transaction with the RxFIFO. If 127 consecutive Rx bit times occur with no RxFIFO transaction, and the RxFIFO is not empty, the RxRDY status bit will be automatically asserted. The RxRDY may in turn be used to generate an interrupt or DMA transfer request. Since the receiver clock (RxC) is the source of the WDT clock, care should be exercised when external RxC is used (i.e., DCE clock in synchronous formats). If the RxC is stopped the WDT will never timeout.

Upon master reset, the WDT is disabled. The WDT operation is enabled/disabled via the Transmit/Receiver bit 7 (TRCR[7]). If enabled, the WDT will assert the RxRDY status bit if a timeout occurs. If interrupts have been enabled for the RxRDY, or if DMA handshake mode has been selected, the assertion of RxRDY will cause the interrupt or DMA transaction to occur. The WDT count is

automatically initialized when a RxFIFO transaction occurs, or a reset receiver command is issued.

Timing Circuits

The timing block for each channel consists of a crystal oscillator, a bit rate generator (BRG), a digital phase locked loop (DPLL) and a 16-bit counter/timer (C/T). See Figures 29 and 30.

Crystal Oscillator

The crystal oscillator operates directly from a crystal (normally 14.7456MHz if the internal BRG is to be used) connected across the X1/CLK and X2 pins with two external capacitors. If an external clock of the appropriate frequency is available, it may be connected to the X1/CLK pin, and the X2 pin should be open. This signal is divided by two to provide the internal system clock (see Figure 28).

The on-chip oscillator circuitry consists of an inverting amplifier and a feedback resistor which are used to implement a Pierce oscillator (see Figure 28). The addition of an external crystal and external capacitance into the feedback loop provides the positive reactance necessary for oscillation and controls the frequency of oscillation. The oscillator operates at the frequency of oscillation. The oscillator operates at the frequency for which the crystal is anti-resonant (parallel resonant) with the load capacitance across the crystal. The load capacitance is given by:

$$C_L = ((C1 \cdot C2) / (C1 + C2)) + Stray$$

The only difference between "parallel" and "series" crystals is how they were calibrated. Crystals are calibrated to achieve their specified frequency either at parallel resonance with a particular load capacitance, or at series resonance (with no load capacitance). Crystals which were calibrated at their series resonant frequency will still operate at parallel resonance in this oscillator, however the resulting frequency will be slightly higher than the frequency specified for the crystal.

In general, the oscillator frequency can be adjusted slightly by trimming the external capacitors, larger capacitors will lower the oscillators frequency while smaller ones will raise it. The small errors in frequency, due to using a crystal calibrated at a different load capacitance than is present in the circuit, are negligible for typical applications. Reliability is much more important.

For best results, a parallel calibrated crystal should be obtained and the external capacitors should be adjusted until the total circuit capacitance matches the capacitance specified for the crystal.

Typical crystal parameters:
Frequency — 2–16MHz
Mode of operation — parallel resonant, fundamental mode
Load Capacitance (C_L) — 12–32pF

For operation at nominal frequency, the values recommended below will give accurate, reliable results. The frequency will vary slightly, depending on the amount of stray capacitance in the individual circuit, but will typically be off no more than 0.01%.

C1 = C2 = 24pF
Y1 = Saronix NYP147-20; 14.7456MHz at
C_L = 20pF with R_S = 25Ω.

Using An External Clock Source

Some designs may have an external clock source available and do not need to use the on-chip oscillator. In this case, the external clock should be applied to the X1/CLK pin.

Theoretical Information on CDUSCC Crystal Oscillator
The information contained in Table NO TAG in Appendix II is based on computer simulations over the expected process range and actual device testing at room temperature.

Bit Rate Generator

The BRG operates from the oscillator or external clock and is capable of generating 19 bit rates. These are available to the receiver, transmitter, DPLL, and C/T. The BRG output is at 32X the base bit rate. Since all nineteen rates are generated simultaneously, each receiver and transmitter may select its bit rate independently. The transmitter and receiver timing registers include a 4-bit field for this purpose
(TTR[3:0], RTR[3:0]).

Bit rates of 14.4k, 56k and 64k are available on CDUSCC only. To make these rates available, TRCR[1], Tx/Rx command registers must be set. On reset, these rates are not available. TTR[3:0] control bits can be used to select these rates. Refer to Transmit Timing Register for selection details.

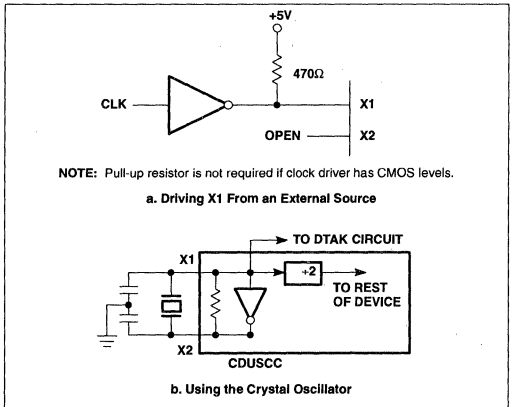

Figure 28. Providing an X1/CLK Source

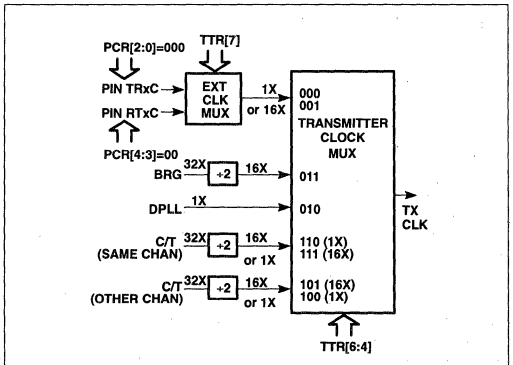

Figure 29. Transmitter Clock Sources

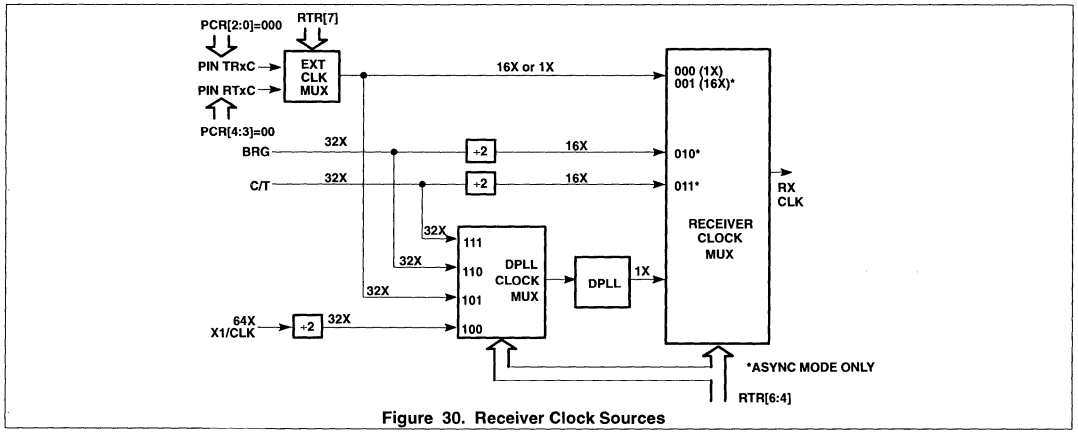

Figure 30. Receiver Clock Sources

Clock Selection Circuits

Transmitter

The selection control for the transmitter clock is shown in Figure 29.

Receiver

Clock selection circuitry for the receiver is shown in Figure 30.

DPLL (Digital Phase-Locked Loop) Operation

Digital Phase-Locked Loop

Each channel of the CDUSCC includes a DPLL used in synchronous modes to recover clock information from a received data stream. The DPLL is driven by a clock at nominally 32 times the data rate. This clock can be programmed via RTR (7:4), to be supplied from an external input, from the receiver BRG, from the C/T or directly from the crystal oscillator.

Table 9. NRZI Mode Count Length

Count When Transition Detected	Count Length Adjustment	Counter Reset After Count Reaches
0-7	-2	29
8-15	-1	30
16-23	+1	32
24-30	+2	33
None Detected	0	31

The DPLL uses this clock, along with the data stream to construct a data clock which may then be used as the CDUSCC receive clock, transmit clock, or both. The output of the DPLL is a square wave at 1X the data rate. The derived clock can also be programmed to be output on a CDUSCC pin, only the DPLL receiver output clock is available at the TRxC pin. Four CCR commands are associated with DPLL operation: Enter search mode, set FM mode, set NRZI mode, and disable DPLL. The commands are described in the channel command register description (See Table 13.). Waveforms associated with the DPLL are illustrated in Figure 34.

If DPLL is selected as receiver clock (RTR[6]) and transmitter clock (RTR[6:4]), transmitter clock is free-running until receiver enters the search mode and finds a transition. After receiver clock has been established, transmit clock will synchronize with it. Master Reset disables the DPLL and sets it to NRZI mode.

Table 10. FM Mode Count Length

Count When Transition Detected	Count Length Adjustment	Counter Reset After Count Reaches
8-15	-1	30
16-23	+1	32
24-7	Disabled	
None Detected	0	31

DPLL NRZI Mode Operation

This mode is used with NRZ and NRZI data encoding. With this type of encoding, the transitions of the data stream occur at the beginning of the bit cell. The DPLL has a six bit counter which is incremented by a 32X clock. The Enter Search Mode command sets the counter to 16 and forces the DPLL clock output to zero. The first edge detected during search mode begins operation. The DPLL output clock then rises at a count of 0 and falls at 16. Data is sampled on the rising edge of the clock. When a transition in the data stream is detected, the count length is adjusted by one or two counts, depending on the counter value when the transition occurs (see Table 9). A transition detection at the roll-over point (third column in Table 9) is treated as a transition occurring at zero count.

The count length adjustments cause the rising edge of the DPLL output clock to converge to the nominal center of the bit cell. In the worst case, which occurs when a DPLL pulse is coincident with the data edge, the DPLL converges after 12 data transitions.

For the DPLL to start up correctly, a pre-frame synchronizing pattern needs to be sent. For NRZ encoded data, a stream of alternating ones and zeros should be used and for NRZI encoded data, a stream of zeros should be used.

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Figure 31. TTRA (B) Transmitter Timing Register [All Protocol Modes]

7	6	5	4	3	2	1	0

— Bit Rate Select — This field selects an output from the bit rate generator to be used by the transmitter circuits. The actual frequency output from the BRG is 32X the bit rate shown in Table 11. The BRG output is divided by two before being applied to the transmitter clock multiplexer (see Figure 29). With a crystal or external clock of 14.7456 MHz the bit rates are as given in Table 11.

Table 11. Transmitter Baud Rates

				TRCR[1] = 0	TRCR[1] = 1 *
				Bit Rate	Bit Rate
0	0	0	0	50	14.4k
0	0	0	1	75	56k
0	0	1	0	110	64k
0	0	1	1	134.5	134.5
0	1	0	0	150	150
0	1	0	1	200	200
0	1	1	0	300	300
0	1	1	1	600	600
1	0	0	0	1050	1050
1	0	0	1	1200	1200
1	0	1	0	2000	2000
1	0	1	1	2400	2400
1	1	0	0	4800	4800
1	1	0	1	9600	9600
1	1	1	0	19.2k	19.2k
1	1	1	1	38.4k	38.4k

— Transmitter Clock Select — This field selects the clock for the transmitter.

0 0 0	1x external	000 External clock from TRxC or RTxC at 1X the shift (baud) rate.
0 0 1	16x external	001 External clock from TRxC or RTxC at 16X the shift rate.
0 1 0	DPLL	010 Internal clock from the phase locked loop at 1X the bit rate. It should be used only in half-duplex operation since the DPLL will periodically re-sync itself to the received data if in full-duplex operation. DPLL clock source is passed to Tx even if DPLL is disabled.
0 1 1	BRG	011 Internal clock from the bit rate generator at 32X the shift rate. The clock signal is divided by two before use in the transmitter which operates at 16X the baud rate. Rate selected by [3:0].
1 0 0	2x other channel C/T	100 Internal clock from counter/timer of other channel. The C/T should be programmed to produce a clock at 2X the shift rate.
1 0 1	32x other channel C/T	101 Internal clock from counter/timer of other channel. The C/T should be programmed to produce a clock at 32X the shift rate.
1 1 0	2x own channel C/T	110 Internal clock from the counter/timer of own channel. The C/T should be programmed to produce a clock at 2X the shift rate.
1 1 1	32x own channel C/T	111 Internal clock from the counter/timer of own channel. The C/T should be programmed to produce a clock at 32X the shift rate.

— External Source — This bit selects the RTxC pin or the TRxC pin of the channel as the transmitter clock input when [6:4] specifies external. When used for input, the selected pin must be programmed as an input in the PCR [4:3] or [2:0].

0	RTxC Pin	0 External input from RTxC pin.
1	TRxC Pin	1 External input from TRxC pin.

* extended mode only

Figure 32. RTRA (B) Receiver Timing Register [All Protocol Modes]

7	6	5	4	3	2	1	0

— [3:0] Bit Rate Select — This field selects an output from the bit rate generator to be used by the receiver circuits. The actual frequency output from the BRG is 32X the bit rate shown in Table 12. The BRG output is divided by two before being applied to the receiver clock multiplexer (see Figure 30). With a crystal or external clock of 14.7456MHz, the bit rates are as given in Table 12.

Table 12. Receiver Baud Rates

				TRCR[1] = 0	TRCR[1] = 1
				Bit Rate	Bit Rate
0	0	0	0	50	14.4k
0	0	0	1	75	56k
0	0	1	0	110	64k
0	0	1	1	134.5	134.5
0	1	0	0	150	150
0	1	0	1	200	200
0	1	1	0	300	300
0	1	1	1	600	600
1	0	0	0	1050	1050
1	0	0	1	1200	1200
1	0	1	0	2000	2000
1	0	1	1	2400	2400
1	1	0	0	4800	4800
1	1	0	1	9600	9600
1	1	1	0	19.2k	19.2k
1	1	1	1	38.4k	38.4k

— Receiver Clock Select — This field selects the clock for the receiver.

0 0 0	1x external	000 External clock from TRxC or RTxC at 1X the shift (baud) rate.
0 0 1	16x external (ASYNC only)	001 External clock from TRxC or RTxC at 16X the shift rate. Used for ASYNC mode only.
0 1 0	BRG (ASYNC only)	010 Internal clock from the bit rate generator at 32X the shift rate. Clock is divided by two before use by the receiver logic, which operates at 16X the baud rate. Rate selected by [3:0]. Used for ASYNC mode only.
0 1 1	C/T of channel (ASYNC only)	011 Internal clock from counter/timer of own channel. The C/T should be programmed to produce a clock at 32X the shift rate. Clock is divided by two before use in the receiver logic. Used for ASYNC mode only.
1 0 0	DPLL, source = 64 X1/CLK	100 Internal clock from the digital phase locked loop. The clock for the DPLL is a 64X clock from the crystal oscillator or system clock input. (The input to the oscillator is divided by two).
1 0 1	DPLL, source = 32 external	101 Internal clock from the digital phase locked loop. The clock for the DPLL is an external 32X clock from the RTxC or TRxC pin, as selected by [7].
1 1 0	DPLL, source = 32x BRG	110 Internal clock from the digital phase locked loop. The clock for the DPLL is a 32X clock from the BRG. The frequency is programmed by [3:0].
1 1 1	DPLL, source = 32x C/T	111 Internal clock from the digital phase locked loop. The clock for the DPLL is a 32X clock from the counter/ timer of the channel.

— External Source — This bit selects the RTxC pin or the TRxC pin of the channel as the receiver or DPLL clock input, when [6:4] specifies external. When used for input, the selected pin must be programmed as an input in the PCR [4:3] or [2:0].

0	RTxC 0 External input from RTxC pin.
1	TRxC 1 External input from TRxC pin.

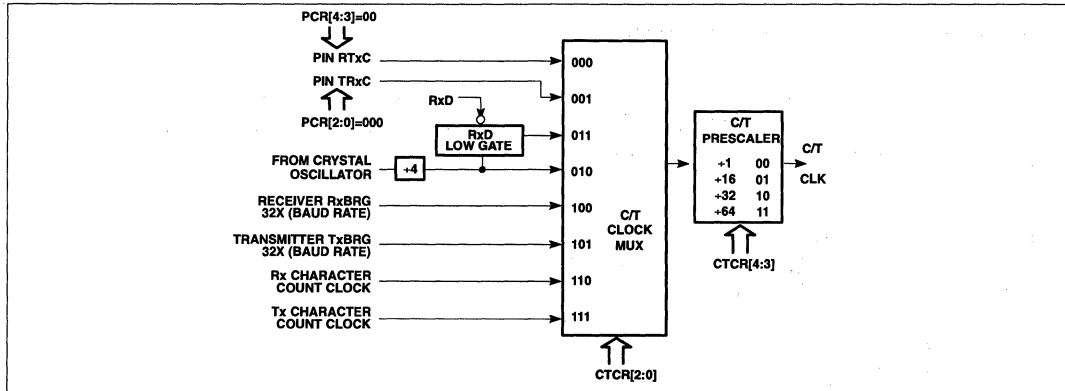

Figure 33. Counter/Timer Clock Sources

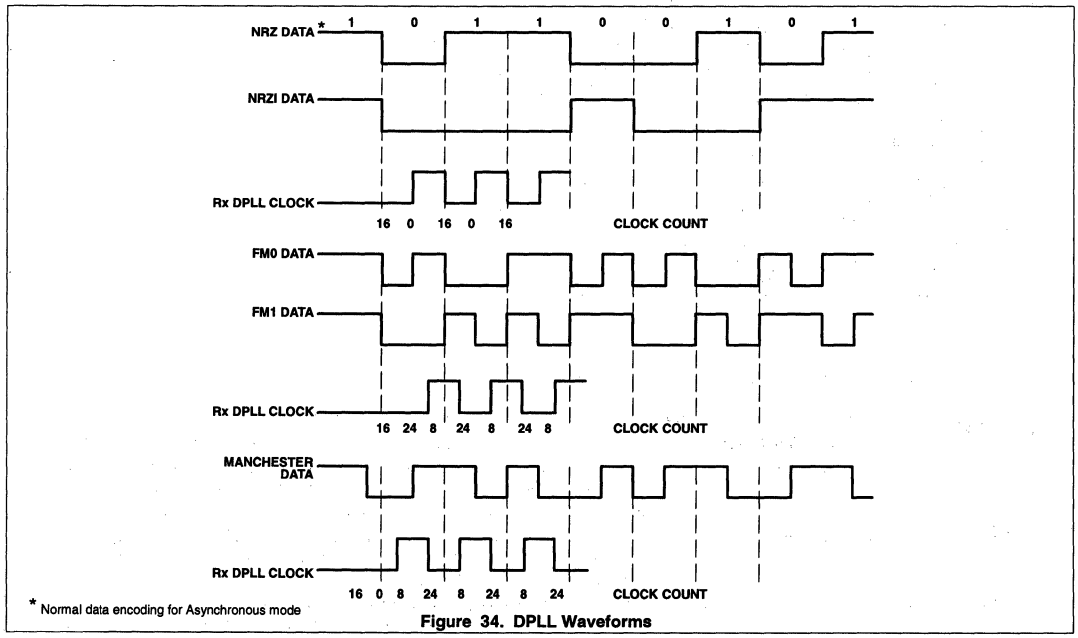

Figure 34. DPLL Waveforms

DPLL FM Mode Operation

FM operation is used with FM0, FM1, and Manchester data encoding. With this type of encoding, transitions in the data stream always occur at the beginning of the bit cell for FM0 and FM1, or at the center of the bit cell for Manchester. The DPLL 6-bit counter is incremented by a 32X clock. The Enter Search Mode command sets the counter to 16 and forces the DPLL clock output to zero. The first edge detected during search mode begins operation. The DPLL receiver clock then rises on a count of 8 and falls on 24. (The DPLL transmitter clock output falls on a count of 16. It rises on a count of 0 if a transition has been detected between counts of 16 and 23. For other cases, it rises 1/2 count of the 32X input clock before the zero count is reached.) This provides a 1X clock with edges positioned at the nominal centers of the two halves of the bit cell. The transition detection circuit is enabled between counts of 8 and 23, inclusive. When a transition is detected, the count length is adjusted by one, depending on when the transition occurs (see Table 10).

If a transition is not detected for two consecutive data bits, the DPLL is forced into search mode and the DPLL error status bit (TRSR[3]) is asserted. This feature is disabled when the DPLL output, in addition to being used as the receiver clock, also is used as the transmitter clock. For the DPLL to start up correctly, a pre-frame synchronizing pattern needs to be sent. For FM0, a stream of at least 16 ones should be sent initially. For FM1, a minimum stream of 16 zeros should be sent and for Manchester encoding the initial data stream should consist of alternating ones and zeros. For FM0

format, a separate pre-frame is not necessary if the RxD input is held marking (receiving logical '1's in FM0) for at least 16 bit times while the Enter Search Mode command is given and until the arrival of the first data bit.

Counter/Timers

Each CDUSCC channel has a dedicated counter/timer resource. The counter/timer, C/T, can be used to generate baud rates, count external events, count characters received or transmitted. The C/T value can be preset automatically and read.

Counter/Timer Clock Selection

Clock selection for the Counter/Timers is also available. (See Figure 33). The TRxC and RTxC pins must be configured as inputs if they are to serve as a C/T clock source. The C/T clock also allows divisor 16, 32 or 64 prescaling factor, if desired.

The C/T prescale factor and clock fields are in the CTCR, Counter/Timer Control Register. Refer to the section on the Counter/Timer for a description of this register. C/T output is set to '0' at reset.

A block diagram of C/T is shown in Figure 35. The zero detect of C/T can be used to generate an interrupt or be used to provide a clock source for the receiver and transmitter.

Counter/Timer Control and Value Registers

There are five registers in this set, the format of each is shown below. The control register contains the operational information for each counter/timer. The preset registers contain the count which is loaded into the counter/timer circuits. The last two registers contain the current value of the counter/timer as it operates.

Counter/Timer Operation

Once the registers associated to the Counter/Timer have been loaded, operation of C/T is controlled via Command Register (CCR) explained in Table 13. A typical sequence of operation is as follows:

- program CTCR
- load CTPRH
- load CTPRL
- CPRES (preset load) command via CCR register
- CSTRT (C/T Start) command via CCR register

Counter/Timer Example

A frequent use of the C/T is to generate non-standard baud rates. It it is desired to produce an ASYNC protocol baud rate, the C/T must be programmed to generate a 32x clock rate, as discussed in the previous section (RTR, TTR). Since a 'square' wave is needed, another factor of 2x must be incorporated. Thus:

$$CTPR = \frac{X1/4}{(32)\ (2)\ (Baud\ Rate)}$$

The value CTPR is the 16 bit combination of CTPRH and CTPRL. With a 'standard' X1 frequency (14.7456MHz), the formula simplifies to:

$$CTPR = \frac{57600}{Baud\ Rate}$$

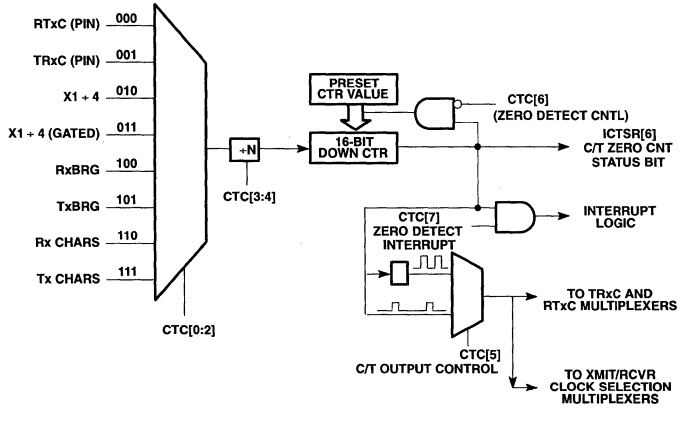

Figure 35. Counter/Timer Control and Value Registers

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Figure 36. CTCRA (B) Counter/Timer Control Register [All Protocol Modes]

7	6	5	4	3	2	1	0

— Clock Source — This field selects the clock source for the counter timer.

0	0	0	RTxC pin	000 RTxC pin. Pin must be programmed as input.
0	0	1	TRxC pin	001 TRxC pin. Pin must be programmed as input.
0	1	0	X1/CLK ÷ 4	010 Source is the crystal oscillator or system clock input divided by four.
0	1	1	X1/CLK ÷ 4 gated by RxD	011 This selects a special mode of operation. In this mode the counter, after receiving the 'start C/T' command, delays the start of counting until the RxD input goes low. It continues counting until the RxD input goes High, then stops and sets the C/T zero count status bit. The CPU can use the value in the C/T to determine the bit rate of the incoming data. The clock is the crystal oscillator or system clock input divided by four.
1	0	0	Rx BRG	100 Source is the 32X BRG output selected by RTR[3:0] of own channel.
1	0	1	Tx BRG	101 Source is the 32X BRG output selected by TTR[3:0] of own channel.
1	1	0	Rx characters	110 Source is the internal signal which loads received characters from the receive shift register into the receiver FIFO. When operating in this mode the FIFO'd EOM status bit (RSR[7]) will be set when the character which causes the count to go to zero is loaded into the receive FIFO.
1	1	1	Tx characters	111 Source is the internal signal which transfers characters from the data bus into the transmit FIFO. When operating in this mode, and if the TEOM on zero count control bit (TPR[4]) is asserted, the FIFO'd Send EOM command will be automatically asserted when the character which causes the count to go to zero is loaded into the transmit FIFO.

— Clock Select — This field selects whether the clock selected by [2:0] is prescaled prior to being applied to the input of the C/T.

0	0	No prescaling
0	1	Divide clock by 16
1	0	Divide clock by 32
1	1	Divide clock by 64

— Counter/Timer Output Control - This bit selects the output waveform when the counter/timer is selected to be output on TRxC or RTxC.

0	Square	0	The output toggles each time the C/T reaches zero count. The output is cleared to Low by either of the preset counter/timer commands.
1	Pulse	1	The output is a positive pulse each time the C/T reaches zero count. The duration of this pulse is one clock period. For the same pre-load value, the O/P frequency of the pulse waveform is twice that of square waveform.

— Zero Detect Control — This bit determines the action of the counter upon reaching zero count.

0	Preset	0	The counter/timer is preset to the value contained in the counter/timer preset registers (CTPRL, CTPRH) at the next clock edge.
1	Continue	1	The counter/timer continues counting without preset. The value at the next clock edge will be H'FFFF'.

— Zero Detect Interrupt — This bit determines whether the assertion of the C/T ZERO COUNT status bit (ICTSR[6]) causes an interrupt to be generated.

0	Disable	0 Interrupt disabled.
1	Enable	1 Interrupt enabled if master interrupt enable (IER3[7] or ICR[1:0]) is asserted.

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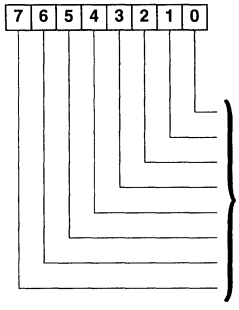
Figure 37. CTPRHA (B) Counter/Timer Preset Register High [All Protocol Modes]



— **MSB** — This register contains the eight most significant bits of the value loaded into the counter/timer upon receipt of the load C/T from preset register command or when the counter/timer reaches zero count and the zero detect control bit (CTCR[6]) is set to zero. The minimum 16-bit counter/timer preset value is H'0002'.

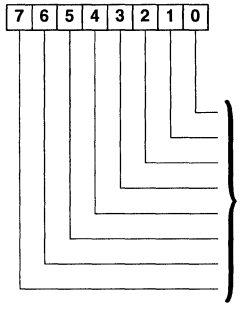
Most significant bits of counter/timer preset value

For CTPRH and CTPRL, 16-bit value may be calculated as follows:

$$\text{Value when CTCR[5] is 0} = \frac{\text{Source frequency (CTCR [2 : 0])}}{\text{desired frequency} \cdot 2}$$

$$\text{Value when CTCR[5] is 1} = \frac{\text{Source frequency (CTCR [2 : 0])}}{\text{desired frequency}}$$

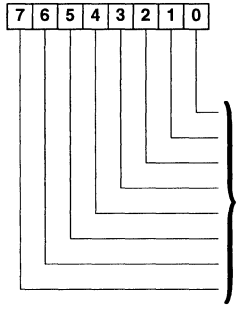
Figure 38. CTPRLA (B) Counter/Timer Preset Register Low [All Protocol Modes]



— **LSB** — This register contains the eight least significant bits of the value loaded into the counter/timer upon receipt of the load C/T from preset register command or when the counter/timer reaches zero count and the zero detect control bit (CTCR[6]) is set to zero. The minimum 16-bit counter/timer preset value is H'0002'.

Least significant bits of counter/timer preset value

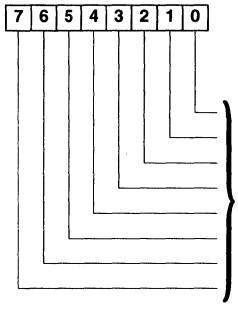
Figure 39. CTHA (B) Counter/Timer Register High [All Protocol Modes]



— **MSB** — A read of this 'register' provides the eight most significant bits of the current value of the counter/timer. It is recommended that the C/T be stopped via a stop counter command before it is read to prevent errors which may occur due to the read being performed while the C/T is changing. This count may be continued after the register is read.

Most significant bits of counter/timer value

Figure 40. CTLA (B) Counter/Timer Register Low [All Protocol Modes]



— **LSB** — A read of this 'register' provides the eight least significant bits of the current value of the counter/timer. It is recommended that the C/T be stopped via a stop counter command before it is read, in order to prevent errors which may occur due to the read being performed while the C/T is changing. This count may be continued after the register is read.

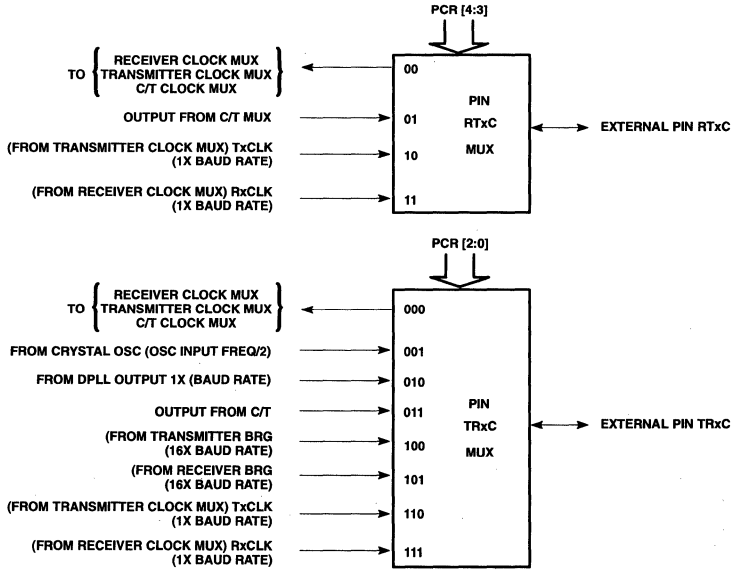


Figure 41. TRxC and RTxC Function Select

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I/O AND CLOCK PIN CONFIGURATION

Pin Configuration Register (PCRA, PCRB)

This register selects the functions for multipurpose I/O pins. (See Figure 41.)

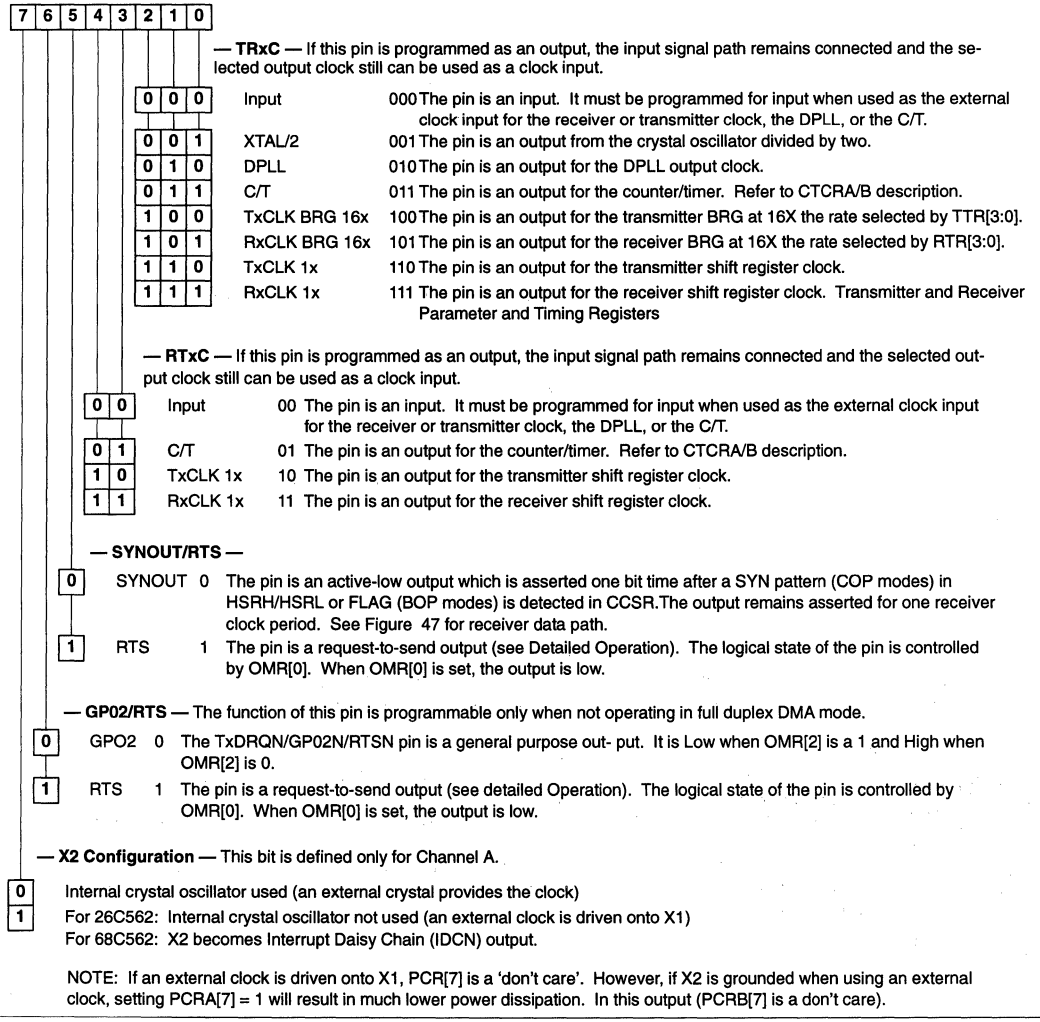
The CDUSCC allows two pins, GPO2/RTSN and RTSN/SYNOUT to output signals selectable by the PCR, Pin Configuration Register. This register also controls the TRxC and RTxC function as shown in Figure 42.

General Purpose I/O

The CDUSCC provides two GPIs, General Purpose Inputs, and two GPOs, General Purpose Outputs, per channel. The GP I/O pins are shared with the DMA request and acknowledge pins. If not required for use by DMA handshake, the GP I/O pins can be user-defined I/O. The values may always be read as ICTSRA/B[1:0]. When the ICTSR is read, the values of the GPI inputs are latched to mask any changes that may occur while the read cycle is in progress.

The GPO2 output must be configured as General Purpose Output (not RTSN output) before use. The outputs are driven by writing inverse data into the channel's OMR[2] bit for GPO2 and/or OMR[1] for GPO1.

Figure 42. PCRA (B) Pin Configuration Register [All Protocol Modes]



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Output and Miscellaneous Register (OMRA, OMRB)

This register is used to set the state of various output pins. It also provides several miscellaneous functions such as Tx, RxFIFO activation, and Tx residual character length (see Figure 43 for details).

TxRDY Activate Mode

FIFO not full: The channel's TxRDY status bit is asserted each time a character is transferred from the transmit FIFO to the transmit shift register. If not reset by the CPU, TxRDY remains asserted until the FIFO is full, at which time it is automatically negated.

FIFO empty: The channel's TxRDY status bit is asserted when a character transfer from the transmit FIFO to the transmit shift register causes the FIFO to become empty. If not reset by the CPU, TxRDY remains asserted until the FIFO is full, at which time it is negated.

If the TxRDY status bit is reset by the CPU, it will remain negated regardless of the current state of the transmit FIFO, until it is asserted again due to the occurrence of one of the above conditions.

RxRDY Activate Mode

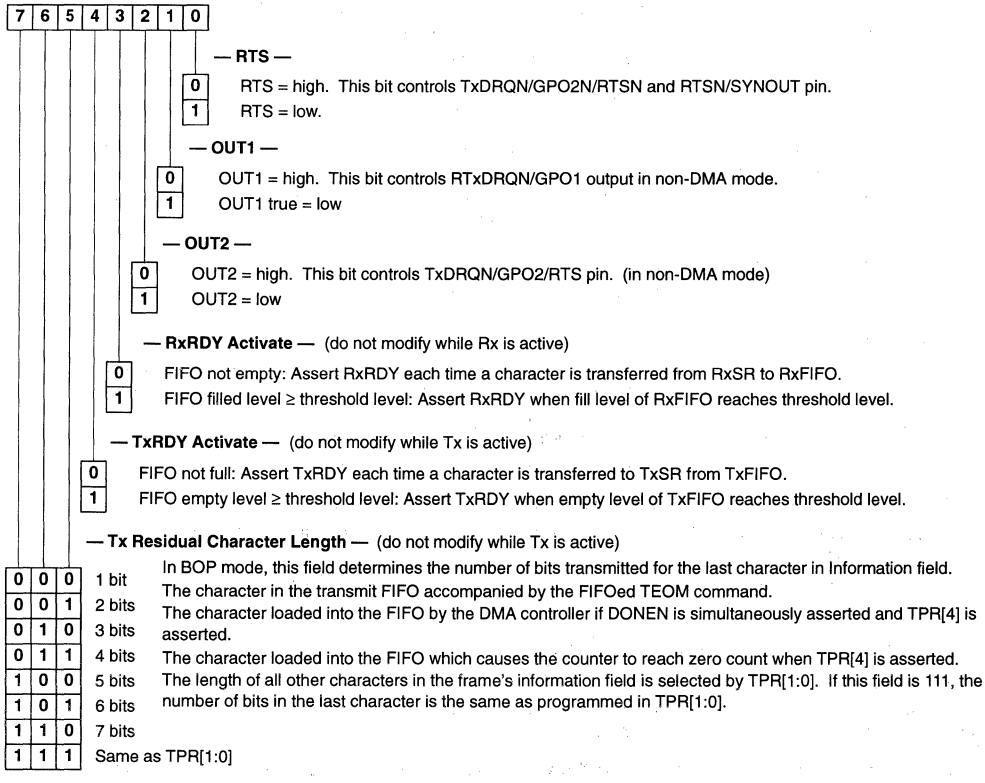
FIFO not empty: The channel's RxRDY status bit is asserted each time a character is transferred from the receive shift register to the receive FIFO. If not reset by the CPU, RxRDY remains asserted until the receive FIFO is empty, at which time it is automatically negated.

FIFO full: The channel's RxRDY status bit is asserted when a character transfer from the receive shift register to the receive FIFO causes the FIFO to become full. If not reset by the CPU, RxRDY remains asserted until the FIFO is empty, at which time it is negated.

The RxRDY status bit will also be asserted, regardless of the receiver FIFO full condition, when an end-of-message character is loaded in the RxFIFO (BOP/BISYNC), when a BREAK condition (ASYNC mode) is detected in RSR[2], or when the counter/timer is programmed to count received characters and the character which causes it to reach zero is loaded in the FIFO (all protocol modes). (Refer to the detailed operation of the receiver.)

If reset by the CPU, the RxRDY status bit will remain negated, regardless of the current state of the receiver FIFO, until it is asserted again due to one of the above conditions.

Figure 43. OMRA (B) Output and Miscellaneous Register [All Protocol Modes]



COMMAND REGISTERS

Tx/Rx Command Register (TRCRA/B)

This register is used to enable some of the features of CDUSCC which were not available in NDUSCC. At initialization the contents of this register are 00h, that means all the new features are disabled. To enable one or more of the features, the user must write '1' in the bit location for that feature. Care must be taken when writing to this register. Writing a '0' in the bit location that was enabled earlier will disable this feature.

Channel Command Register (CCRA/B)

Dynamic control of the CDUSCC is achieved by issuing 'commands' written to the Channel Control Register (CCR). In the sections that follow, the term 'command' will refer to the commands of Table 13 issued via write cycles to the CCR.

Transmitter CCR Commands

These commands are executed by the transmitter either immediately upon receipt, or are 'attached' to the data byte and FIFO'd for execution at a known time with respect to the data byte being serialized. Table 13 identifies the commands for the transmitter, and if these are immediate or FIFO'd in their operation. Commands to the CDUSCC are entered through the Channel Command Register. Transmitter commands are as follows:

TRST – Reset transmitter (00h): Causes the transmitter to cease operation immediately. The transmit FIFO is cleared and the TxD output goes into the marking state. Also clears the transmitter status bits (TRSR[7:4]) and resets the TxRDY status bit (GSR[1] or GSR[5] for channels A and B, respectively). The counter/timer and other registers are not affected.

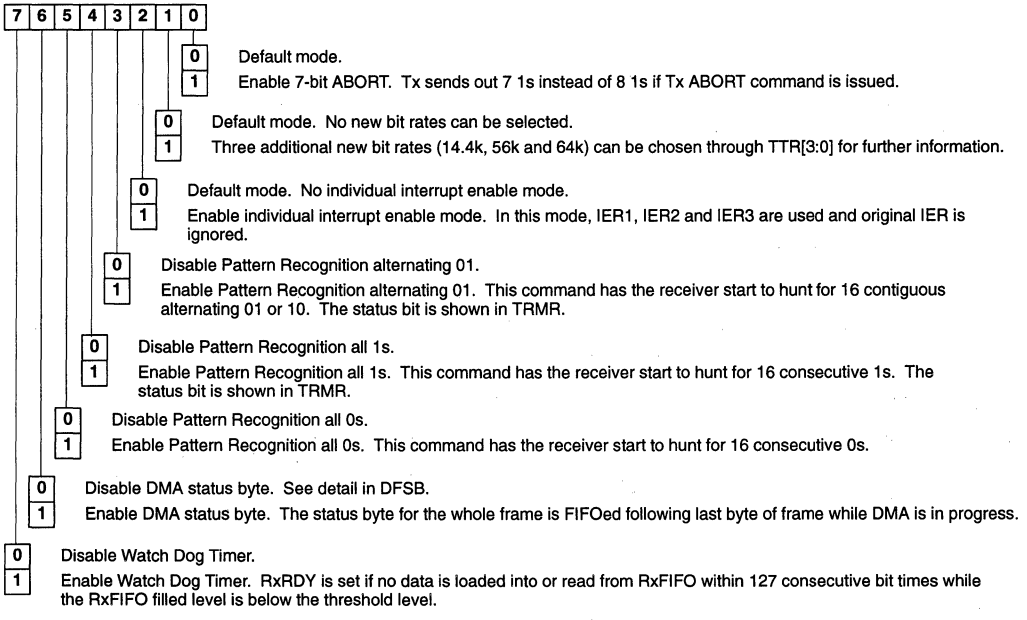
TRCRC – Reset transmit CRC (01h): This command is appended to and FIFOed along with the next character loaded into the transmit FIFO. It causes the transmitter CRC generator to be reset to its initial state prior to beginning transmission of the appended character.

TENB – Enable transmitter (02h): Enables transmitter operation, conditioned by the state of the CTS ENABLE Tx bit, TPR[2]. Has no effect if invoked when the transmitter has previously been enabled.

TDIS – Disable transmitter (03h): Terminates transmitter operation and places the TxD output in the marking state at the next occurrence of a transmit FIFO empty condition. All characters currently in the FIFO, or any loaded subsequently prior to attaining an empty condition, will be transmitted.

When the transmitter is first enabled, transmission will not begin until this command (or the transmit SOM with PAD command, see below) is issued. The command causes the SYN (COP) or FLAG (BOP) pattern to be transmitted. SEND SOM ACK (TRSR[4]) is set when transmission of the SYN/FLAG begins. The CPU may then re-invoke the command if multiple SYN/FLAGs are to be transmitted. Transmission of the FIFO characters begins when the command is no longer re-invoked. If the FIFO is empty,

Figure 44. TRCRA (B) Tx/Rx Command Register [All Protocol Modes]



NOTES:
– Reset receiver command (CCR) will not reset pattern recognition counter unless pattern recognition is disabled first.

Table 13. Channel Command Register

COMMAND	COMMAND DESCRIPTION	COMMAND NAME	FIFO'd	WHEN	FLUSH	RESPONSE
	Transmitter Commands					
00h	reset Tx	TRST	NO	--	YES	
01h	reset TxCRC	TRCRC	YES	PRE	NO	
02h	enable Tx	TENB	NO	--	NO	
03h	disable Tx	TDIS	NO	EMPTY	NO	
04h	transmit SOM	TSOM	NO	--	NO	TRSR[4] SEND SOM ACK
05h	transmit SOM with PAD	TSOMP	NO	EMPTY	NO	TRSR[4] SEND SOM ACK
06h	transmit EOM	TEOM	YES	POST	NO	TRSR[5] FRAME COMPLETE
07h	transmit ABORT/BREAK	TABRK	NO	--	YES	TRSR[4] SEND ABORT ACK
08h	transmit DLE	TDLE	YES	PRE	NO	
09h	go active on poll	TGAP				TRSR[6] LOOP SENDING
0Ah	reset go active on poll	TRGAP				
0Bh	go on-loop	TGONL				ICTSR[4] LCN → Asserted
0Ch	go off-loop	TGOFL				ICTSR[4] LCN → Negated
0Dh	exclude from CRC	TXCRC	YES	PRE	NO	
0Eh	include Tx SYN in CRC accum	TISCRC				
0Fh	exclude Tx SYN from CRC accum	TXSCRC				
	Receiver Commands					
40h	reset Rx	RRST				
42h	enable Rx	RENB				
43h	disable Rx	RDIS				
44h	disable new FIFOed status bits	RDFSB				
45h	enable new FIFOed status bits	REFSB				
	Counter/Timer Commands					
80h	start	CSTRT				
81h	stop	CSTOP				
82h	preset to FFFF	CPFF				
83h	preset from CTPRH/CTPRL	CPRES				
	DPLL Commands					
C0h	enter search mode	PSRCH				
C1h	disable DPLL	PDIS				
C2h	set FM mode	PFM				
C3h	set NRZI mode	PNRZI				
	Test Mode Commands					
C5h	BRG test	BRGTEST				
C6h	Tx PLA test	TTEST				
C7h	Rx PLA test	RTEST				
	DMA Commands					
C8h	Disable DONE(EOPN) on ABORT/SF	DDONE				
C9h	Enable DONE(EOPN) on ABORT/SF	EDONE				

NOTE: — Values not defined explicitly in Table 13 are reserved for future use and should not be programmed.
— Back-to-back write to CCR must have delay equal or greater than three X1 clocks between two commands.
PRE = command internally executed before the new data (data loaded in FIFO after this command) is transmitted.
EMPTY = command internally executed after TxFIFO becomes empty.
POST = command internally executed after the transmission of data byte that was loaded in TxFIFO immediately after this command.

SYN/FLAGs continue to be transmitted until a character is loaded into the FIFO, but the status bit (TRSR[4]) is not set. Insertion of SYN/FLAGs between frames can be accomplished by invoking this command after the frame complete status bit (TRSR[5]) has been asserted in response to transmission of the end-of-message sequence.

TSOM – Transmit start of message (04h): Used in COP and BOP modes to initiate transmission of a frame after the transmitter is first enabled, prior to sending the contents of the FIFO. Can also be used to precisely control the number of SYN/FLAGs at the beginning of transmission or in between frames. TSOM command may be issued before or after the transmitter enabled, but it will be executed when the transmitter is enabled.

TSOMP – Transmit start of message with opening PAD (05h): Used in COP and BOP modes after the transmitter is first enabled to send a bit pattern for DPLL synchronization prior to transmitting the opening SYN (COP) or FLAG (BOP). The SYN/FLAG is sent at the next occurrence of a transmit FIFO empty condition. Once an opening SYN/FLAG has been transmitted, the TSOMP command will be ignored until the transmitter is either reset or disabled and re-enabled. All characters currently in the FIFO, or any loaded subsequently prior to attaining an empty condition, will be transmitted. While the PAD characters are transmitted, the character length is set to 8 bits, (regardless of the programmed length), and parity generation (COP), zero insertion (BOP), and LRC/CRC accumulation are disabled. SEND SOM ACK (TRSR[4]) is set when transmission of the SYN/FLAG begins. The CPU may then invoke the transmit SOM command if multiple SYN/FLAGs are to be transmitted.

The TSOM/TSOMP commands, described above, are sampled by the controller in alternate bit times of the transmitter clock. As a consequence, the first bit time of a COP/BOP frame will be transmitted on the TxD pin, after a maximum of three bit times, after the command is issued. (The additional 1-bit delay in the data path is due to the data encoding logic.)

TEOM – Transmit end-of-message (06h): This command is appended to the next character loaded into the transmit FIFO. It causes the transmitter to send the end-of-message sequence (selected FCS in COP modes, FCS–FLAG in BOP modes) after the appended character is transmitted. Frame complete (TRSR[5]) is set when transmission of the FCS begins. This command is also asserted automatically if the TEOM on zero count or done control bit (TPR[4]) is asserted, and the counter/timer is programmed to count transmitted characters when the character which causes the count to got to zero is loaded into the transmit FIFO. TEOM is not recognized if the transmitter FIFO is full.

TABRK – Transmit Abort (BOP) /Transmit Break (ASYNC) (07h): In BOP modes, causes an abort (eight 1s) to be transmitted after transmission of the character currently in the shift register is completed. The transmitter then sends MARKs or FLAGs depending on the state of underrun control (TPR[7:6]). Send SOM/Abort ack (TRSR[4]) is set when the transmission of the abort begins. If the command is re-asserted before transmission of the previous ABORT is completed, the process will be repeated. This can be used to send the idle sequence. The 'transmit SOM' command must be used to initiate transmission of a new message. In either mode, invoking this command causes the transmit FIFO to be flushed (characters are not transmitted).

In ASYNC mode, causes a break (space) to be transmitted after transmission of the character currently in the shift register is completed. Send break ack (TRSR[4]) is set when the transmission of the break begins. The transmitter keeps track of character times. If the command is re-asserted, send break ack will be set again at the beginning of the next character time. The user can use this mechanism to control the length of the break in character time multiples. Transmission of the break is terminated by issuing a 'reset Tx' or 'disable Tx' command.

TDLE – Transmit DLE (08h): Used in COP modes only. This command is appended to and FIFOed with the next character loaded into the transmitter FIFO. It causes the transmitter to send a DLE, (EBCDIC H'10', ASCII H'10') prior to transmitting the appended character. If the transmitter is operating in BISYNC transparent mode, the transmitter control logic automatically causes a second DLE to be transmitted whenever a DLE is detected at the top of the FIFO. In this case, the TDLE command should not be invoked. An extra (third) DLE, however, will not be sent if the transmit DLE command is invoked.

TGAP – Go active on poll (09h): Used in BOP loop mode only. Causes the transmitter, if it is enabled, to begin sending when an EOP sequence consisting of a zero followed by seven ones is detected. The last one of the EOP is changed to zero, making it another FLAG, and then the transmitter operates as described in the detailed operation section. The loop sending status bit (TRSR[6]) is asserted concurrent with the beginning of transmission.

TRGAP – Reset go active on poll (0Ah): Clears the stored 'go active on poll' command.

TGONL – Go on-loop (0Bh): Used in BOP loop mode to control the assertion of the LCN output. This output provides the means of controlling external loop interface hardware to go on-loop and off-loop. When the command is asserted, the CDUSCC will look for the receipt of a zero followed by seven 1s, at which time it will assert the LCN output and set the delta DCD/LC status bit (ICTSR[4]). This allows the CDUSCC to break into the loop without affecting loop operation. This command must be used to initiate loop mode operation.

TGOFL – Go off-loop (0Ch): Used in BOP loop mode to control the negation of the LCN output. This output provides the means of controlling external loop interface hardware to go on-loop and off-loop. When the command is asserted, the CDUSCC will look for the receipt of eight contiguous 1s, at which time it will negate the LCN output and set the delta DCD/LC status bit (ICTSR[4]). This allows the CDUSCC to get off the loop without affecting loop operation. This command is normally used to terminate loop mode operation.

TXCRC – Exclude from CRC (0Dh): This command is appended to and FIFOed along with the next character loaded into the transmit FIFO. It causes the transmitter CRC generator to be disabled while appended character is being transmitted. Thus, that character is not included in the CRC accumulation.

TISCRC – Disable/SYN Exclusion from CRC (0Eh): Disable Tx SYN exclusion from Tx CRC accumulation.

TXSCRC – Enable SYN Exclusion from CRC (0Fh): In this mode, all of the SYN characters in COP mode will be excluded from TxCRC accumulation including SYN1, SYN1+SYN2, or DLE+SYN1 in BISYNC XPNT mode.

Receiver Commands

These commands are executed by receiver either immediately upon receipt, or upon completion of serialization of the data byte currently in the RxSR. FIFOing of status bits (RDFSB/REFSB) should not be executed or disabled while receiver is enabled.

RRST – Reset receiver (40h): Causes the receiver to cease operation, clears the receiver FIFO, clears the data path, and clears the receiver status (RSR[7:0]), TRSR[3:0], and either GSR[0] or GSR[4] for channels A and B, respectively). The counter/timer and other registers are not affected.

RENB – Enable receiver (42h): Causes receiver operation to begin, conditioned by the state of the DCD ENABLE Rx bit, RPR[2]. Receiver goes into START, SYN, or FLAG search mode depending on channel protocol mode. Has no effect if invoked when the receiver has previously been enabled.

RDIS – Disable receiver (43h): Terminates operation of the receiver. Any character currently being assembled will be lost. Does not affect FIFO or any status. While in COP mode, disabling the receiver does not clear the data path; in all other cases, it does.

RDFSB – Disable new FIFOed status bits (44h): Causes only those status bits to be FIFOed that were in NDUSCC (default mode). Other status bits which were not FIFOed in NDUSCC are still active, but are not FIFOed (i.e., will be set immediately). On master reset the CDUSCC will be automatically set in this mode (i.e., equivalent operation to NDUSCC). This mode is not recommended for new software development.

REFSB – Enable new FIFOed status bits (45h): Causes all status bits to be FIFOed. Note that since abort detect (BOP/BOPL) does not have a data byte to "attach" to, a dummy data byte (FFh) is generated by CDUSCC for status attachment. In BOP/BOPL mode, TRSR[2:0] are always FIFOed regardless of RDFSB/REFSB setting. See following Table for specific bits that are FIFOed in this mode.

ASYNC	
RSR[7]*	Character compare
RSR[5]	Overrun
RSR[2]	BRK start
RSR[1]*	FE
RSR[0]*	PE
COP	
RSR[7]*	EOM
RSR[6]	Pad error
RSR[5]	Overrun
RSR[1]*	LRC/CRC error
RSR[0]*	PE
BOP/BOPL	
RSR[7]*	EOM
RSR[6]	ABORT/EOP
RSR[5]	Overrun
RSR[4]	Short frame
RSR[1]*	CRC error
RSR[0]*	RCL not zero
TRSR[2:0]*	Residual character length
* FIFOed status bits in default (NMOS) mode	

In this mode above status bits in RSR and TRSR are not accumulation (ORed) of all previous status conditions for the current frame. They are updated with every RxFIFO read and reflect the status of the current character on top of the RxFIFO.

Caution must be exercised when reading RSR and RxFIFO back-to-back. For some versions of CDUSCC it is possible that fast host processor I/O, meeting the minimum AC timing specifications of CDUSCC, could attempt to access status information before that information has been established at the top of the FIFO. Refer to the latest "Device Variances and Design Cautions" sheet for more information. A delay or NOP is recommended between RxFIFO and RSR read if its is done back-to-back.

Counter/Timer Commands

These commands are executed immediately by the counter/timer. Commands to preset the counter/timer should only be issued once the counter/timer has been stopped.

CSTRT – Start (80h): Starts the counter/timer and prescaler.

CSTOP – Stop (81h): Stops the counter/timer and prescaler. Since the command may be asynchronous with the selected clock source, the counter/timer and/or prescaler may count one or more additional cycles before stopping.

CPFF – Preset to FFFF (82h): Presets the counter timer to H'FFFF' and the prescaler to its initial value. This command causes the C/T output to go Low. Preset commands should not be issued while C/T is running.

CPRES – Preset from CTPRH/CTPRL (83h): Transfers the current value in the counter/timer preset registers to the counter/timer and presets the prescaler to its initial value. This command causes the C/T output to go Low. Preset commands should not be issued while C/T is running.

Digital Phase-Locked Loop Commands

These commands are executed immediately by the DPLL. The DPLL mode (set FM or set NRZI) should be set prior to entering search mode.

PSRCH – Enter Search Mode (C0h): This command causes the DPLL counter to be set to the value 16 and the clock output will be forced low. The counter will be disabled until a transition on the data line is detected, at which point it will start incrementing. After the counter reaches a count of 30, it will reset to zero and cause the clock output to go from Low to High. The DPLL will then continue normal operation. This allows the DPLL to be locked onto the data without pre-frame transitions. This command should not be used if the DPLL is programmed to supply the clock for the transmitter and the transmitter is active.

PDIS – Disable DPLL (C1h): Disables operation of the DPLL.

PFM – Set FM Mode (C2h): Sets the DPLL to the FM mode of operation, used when FM0, FM1, or Manchester (NRZ) is selected by CMR1[7:6].

PNRZI – Set NRZI Mode (C3h): Sets the DPLL to the NRZI mode of operation, used when NRZ or NRZI is selected by CMR1[7:6].

Test Modes

The test modes are included to improve the test coverage and reduce testing time and cost. The results of each test mode are reported as a serial data stream value output via the TxD/SYNOUT pins. With knowledge of this value, this mode can assist in board level diagnostics and self-test.

These commands should only be used for diagnostic purposes as described in Appendix 3.

BRGTST – BRG Test (C5h):
The BRG test mode may be enabled by writing F5h to the CCRA (NOTE: Use a general device reset [RESTN or MRR] to remove the CDUSCC from the BRG test mode).

TTEST – TxPLA Test Mode (C6h):
This test mode can be enabled by writing C6h to the channel's CCR. To disable TxPLA test, a TxRST command must be issued. To test the PLA, RTxC must be used as the clock and the TRxC can be used to initialize the PLA test.

RTEST – RxPLA Test Mode (C7h):
This PLA test mode is enabled by writing C7h to the channel's CCR. To disable the RxPLA test, an RxRST command can be issued. RTxC is the clock input and TRxC initializes the test.

DMA Commands

The ability to signal DMA completion on an ABORT or SHORT FRAME ERROR (BOP only) is provided by these commands. These commands should not be issued when receiver is enabled.

DDONE – Disable DONE (EOPN) or ABORT/SHORT FRAME (C8h): Causes the occurrence of an ABORT status or SHORT FRAME detect status (BOP) to not generate a DMA completion signal (DONE or EOPN). This is the mode of operation for NDUSCC, and is automatically selected following a master reset. This mode is not recommended for new software development.

EDONE – Enable DONE (EOPN) on ABORT/SHORT FRAME (C9h): Causes the occurrence of an ABORT status or SHORT FRAME detect status (BOP) to generate a DMA completion signal (DONE or EOPN).

TRANSMITTER

Overview

The transmitter of CDUSCC, like any other UART or USART device consists primarily of a buffered data path followed by a shift register to serialize the data. In the case of CDUSCC additional capabilities have been added to meet the specific needs of the various protocols supported. To minimize confusion, this overview section will not explicitly describe the subtleties of each of the operating modes. For clarification of protocol or mode specific operation the user is directed to section 3 which discusses each supported protocol in detail.

Transmitter States

Regardless of operating mode (ASYNC or Synchronous) the CDUSCC transmitter has the ability to be in one of two major states, the QUIESCENT STATE or the ACTIVE STATE. In synchronous protocols there is a third major state, the IDLE STATE, which the transmitter may enter. Figure 46 illustrates the relationship between these major states. It should be noted that this Figure is greatly simplified, and that depending upon protocol some of the single major states of this diagram are actually composed of several functionally similar, but separate, states. For example, the 'single' active state of the diagram reflects five different actual active states (1-ASYNC, 2-COP, 2-BOP). However, from the user's point of view the behavior of the transmitter appears the same, so a single simplified active state is used in this discussion.

THE USER SHOULD BE AWARE OF THESE THREE MAJOR STATES, SINCE IT IS NOT ALWAYS POSSIBLE TO DETERMINE BY STATUS INFORMATION ALONE EXACTLY WHAT STATE THE TRANSMITTER IS IN

The QUIESCENT STATE is entered following a power on reset (POR), transmitter reset command (TxRST) or at the completion of data transfer (i.e., Tx disabled and TxFIFO empty). Only in the QUIESCENT STATE can changes be made to the 'STATIC' control registers of the transmitter without the possibility of data loss or unpredictable results.

The ACTIVE STATE is entered once the transmitter is enabled, data sent to the TxFIFO, and the serialization process of the TxSR begun. It should be noted that for synchronous protocols a unique command is required (via the CCR) to start the serialization process. Once entered, the ACTIVE STATE is NOT exited until either the Tx is reset, the TxFIFO and TxSR are empty or CTS (if used) is de-asserted.

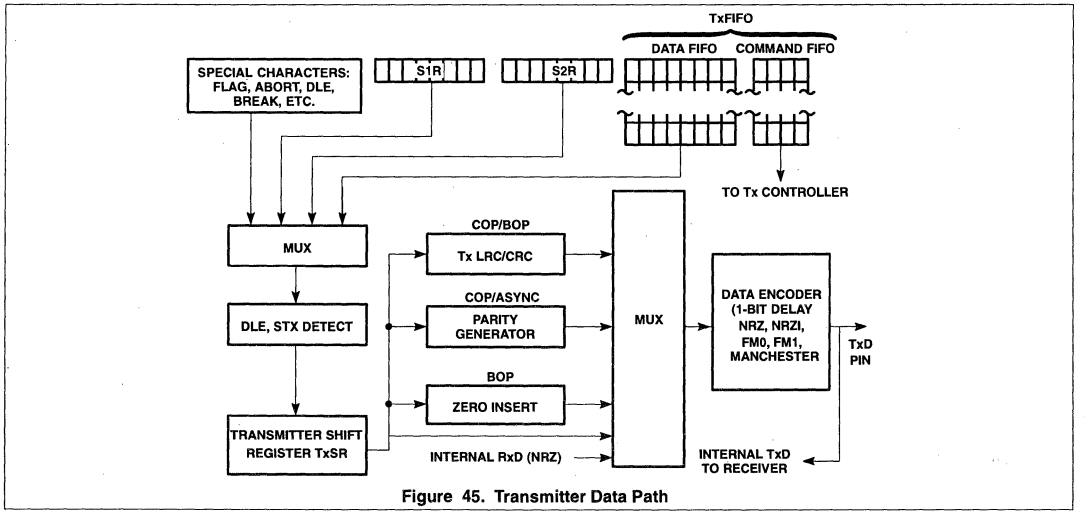


Figure 45. Transmitter Data Path

CMOS DUSSC User's Guide

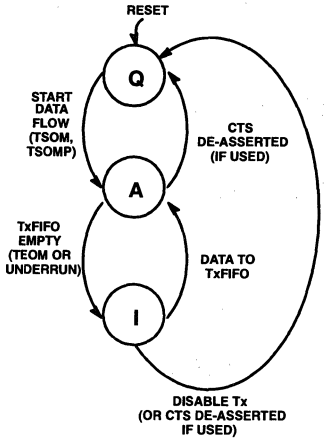
DUSCC/CDUSCC Tx Operation (SYNC Protocols)

Simplified State Diagram

Q = Quiescent State
- Tx output is 'MARK'
- Entered on RESET (Tx or MRR)
- Entered on Tx DISABLED
  - •TxFIFO EMPTY
- Entered on CTS de-assertion (If CTS control enabled)
- TxFIFO can be empty or non-empty
- Tx can be enabled or disabled

A = Active State
- Tx output is DATA, FLAG or SYN
- Entered when ready to flow data
- Tx can be ENABLED or DISABLED
- TxFIFO cannot be empty
- CTS flow control (if used) will cause exit to Q-State if de-asserted

I = IDLE State
- Tx output is FLAG, SYN or MARK
- Entered when TxFIFO becomes empty
  - IDLE (between frames)
  - UNDERRUN (within a frame)
- TxFIFO must be empty
- Tx must be ENABLED
- CTS flow control (if used) will cause exit to Q-State if de-asserted



NOTE: This state diagram is very simplified and does not completely reflect all internal DUSCC states

Figure 46. Transmitter Status

Simply disabling the transmitter WILL NOT cause the CDUSCC to exit the ACTIVE STATE. In fact, operation of the transmitter in this fashion (disabled) is a common technique in synchronous protocols once the frame has been started. Data transfer handshake will continue even after the transmitter has been disabled once the ACTIVE STATE has been entered.

Simply disabling the transmitter WILL NOT cause the CDUSCC to exit the ACTIVE STATE. In fact, operation of the transmitter in this fashion (disabled) is a common technique in synchronous protocols once the frame has been started. Data transfer handshake will continue even after the transmitter has been disabled once the ACTIVE STATE has been entered.

The IDLE STATE is unique to synchronous protocols. It is entered when the TxFIFO and TxSR are both empty. If the transmitter is left enabled while in the IDLE STATE, data flow will resume immediately (without the need for a CCR command) upon the loading of data into the Tx data path from the host. Depending upon protocol, data transfer to the CDUSCC, and CMR set-up parameters, the CDUSCC can be in the IDLE STATE either during underrun or in between legitimate frames. Underrun is considered to occur only while within a frame (i.e., after SOM and before EOM), and is usually recoverable without data loss only in COP protocols. Line idle, the time between frames (i.e., after EOM and before SOM) will never result in data loss since, by definition, there is no data transfer at this time. Line idle can be with marks or SYN/FLAGs depending on CMR set-up parameters.

Transmitter Sections

The transmitter of CDUSCC consists of a DATA PATH section and a CONTROL section. The data path section, illustrated in Figure 45 provides the TxSR with data from any of four possible sources. These sources are:

- Special character logic (e.g., flag, DLE, break, etc)
- S1R & S2R Registers (e.g., SYN1 & SYN2 patterns)
- TxFIFO (e.g., data from host)

The TxSR shifts out the LSB first, thus right justification of characters less than eight bits wide must be done by the CPU prior to sending these characters to the CDUSCC. The output of the TxSR is routed directly to the data encoder. Additionally the output of the TxSR is provided to the CRC/LRC/PARITY generation circuitry. Depending on operating mode selected the appropriate check code can be multiplexed to the data encoder when required. In this manner no additional pipeline delay is introduced into the Tx data path for check code generation.

Transmitter Control

Control of the transmitter can be divided into two categories, static and dynamic. The static control refers to parameters that once set, define the transmitter operation, but are not changed 'on the fly' as data is flowing through the transmitter. Dynamic control deals with conditions that might be required to alter transmitter operation at times when data is flowing through the transmitter data path.

The static control of the CDUSCC transmitter is achieved by adjustment to the contents of the registers listed in the following Table. Setting of bits in these registers will define the protocol, data rates, clock source, etc for the transmitter. The contents of these registers should be altered ONLY when the transmitter is disabled AND in the QUIESCENT STATE, or else unpredictable results can occur.

Channel Mode Registers 1 and 2	CMR1, CMR2	Default
SYN1 and SYN2 Registers	S1R, S2R	Default
Transmitter Parameter Register	TPR	Default
Transmitter Timing Register	TTR	Default
Pin Configuration Register	PCR[5:0]	Default
Output and Misc. Register	OMR[7:3]	Default
Tx/Rx Command Register	TRCR	Extended
FIFO Threshold Level Register	FTLR	Extended

Enabling the Transmitter

The transmitter is enabled with the enable transmitter command (TxENB) via the CCR. If operating in ASYNC modes, the transmitter will enter the ACTIVE STATE once both the transmitter is enabled AND data is placed in the TxFIFO. If operating in SYNCHRONOUS modes, it is also necessary to issue a start command (TSOM or TSOMP) in addition to enabling the transmitter and loading the TxFIFO for the transmitter to enter the ACTIVE STATE. When the disable transmitter command (TxDIS) is issued and the transmitter is in the ACTIVE STATE, THE TRANSMITTER CONTINUES TO OPERATE UNTIL THE TxFIFO and TxSR BECOME EMPTY. It should be kept in mind that enabling or disabling the transmitter does not directly cause entry or exit of the ACTIVE or QUIESCENT STATES. The status of the TxFIFO at the time of (or following) the enable or disable command determines the state.

TxRDY

TxRDY is the primary indicator for data transfer to the TxFIFO. When this signal is asserted it signifies that the transmitter is able to accept additional data into the TxFIFO. TxRDY is the 'source' for other signals used in data transfer handshake. These other signals are the RTxDRN or TxDRQN lines for DMA transfers and the IRQN line for interrupts to the CPU. Data should not be written to the TxFIFO if TxRDY is not asserted. Use of 'wait on Tx' mode of CPU interface or reading the TxFIFO Empty Level Register provide suitable means by which writing to a full TxFIFO can be averted (regardless of transmitter state). Writing to the TxFIFO when full can result in unpredictable transmitter operation and data loss.

Initially the transmitter is in the QUIESCENT STATE and TxRDY does not become asserted until the transmitter is enabled. Characters can be loaded into the TxFIFO while the transmitter is in the QUIESCENT STATE as long as the precautions stated above are taken to ensure that no attempt is made to load data into a full TxFIFO. If the FIFO is full when the transmitter is enabled while in the QUIESCENT STATE, TxRDY will not be asserted until the condition of TxRDY occurs again.

It is up to the user to select how the TxFIFO will request data from the CPU via the Output and Misc Register (OMR). Request can be made as space becomes available in the TxFIFO (FIFO not full – OMR[4] = 0), or when the TxFIFO empty level is equal to or larger than the threshold level (FTLR[7:4] while OMR[4] = 1). For clarity in the following discussion the phrase 'TxFIFO is available' will mean that either the TxFIFO is not full and OMR[4] = 0 or TxFIFO is at or above threshold and OMR[4] = 1.

TxRDY is asserted when the transmitter is enabled or in the ACTIVE STATE and the TxFIFO is available. Once asserted TxRDY will not be reset until the TxFIFO is full.

The CPU may reset TxRDY through a status reset write cycle (writing a 'one' to the TxRDY bit position – GSR[5]). If this is done, TxRDY will not be asserted until a character is transferred to the TxSR and the TxFIFO is available. The assertion of TxRDY will generate interrupt request if both the TxRDY interrupt enable bit and channel master interrupt enable are set.

NOTE: It is not recommended to reset bits in the GSR by writing directly to the GSR.

If DMA operation is programmed, either RTxDRQN (half duplex) or TxDRQN (full–duplex) follows the state of TxRDY regardless of transmitter being enabled or disabled. These operations differ from normal TxRDY in that the request signal is negated on the leading edge of the DMA acknowledge signal when the subsequent transfer causes the transmit FIFO to become full, while the TxRDY signal is negated only after the transfer is completed. Underrun status TRSR[7] set indicates that one or more data characters (not PAD characters) have been transmitted and the TxFIFO and TxSR are both empty.

In 'wait on Tx' mode, a write to a full FIFO causes the write cycle to be extended until a FIFO position is available. For 68C562, DTACKN signal and for 26C562 RDYN signal is asserted to acknowledge acceptance of the data. In non–wait modes, a write to the full FIFO is not allowed. In this event, the results are unpredictable and the transmitter should be reset (TxRST) before resuming data transmission.

TxRTS Control

If TxRTS CONTROL, TPR[3], is programmed, the channel's RTS output is negated six bit times after the last bit (stop bit in ASYNC MODE) of the last character is transmitted. RTS is normally asserted and negated by writing to OMR[0]. Therefore, RTS should be asserted after the transmitter is enabled. Setting of TPR[3] causes RTS to be negated automatically (if the transmitter is disabled before the last data character has been shifted out) after all characters in the transmitter FIFO (if any) are transmitted and five bit times after the 'last character' is shifted out. This feature can be used to automatically terminate the transmission of a message as follows:

- Program auto-reset mode: TPR[3] = 1
- Enable transmitter
- Assert RTSN: OMR[0] = 1
- Send message
- Disable transmitter after the last character is loaded into the TxFIFO
- The last character will be transmitted and OMR[0] will be reset five bit times after the last bit, causing RTSN to be negated. The TxD output will remain in the marking state until the transmitter is enabled again.

The 'last bit' in ASYNC is simply the last stop bit of the character. In BOP and COP, the last character is defined either explicitly by appending it with TEOM or implicitly through the selection of the frame underrun control sequence, TPR[7:6] (transmitter parameter register).

TxCTS Operation

If CTS enable Tx, TPR[2], is set, the CTSN input must be asserted for the transmitter to operate. Changes in CTSN while a character is being transmitted do not affect transmission of that character. However, if the CTSN input becomes negated when TPR[2] is set and the transmitter is enabled and ready to start sending a new character, CTS underrun, TRSR[6], is asserted and the TxD output is placed in the marking (high) state. A CTS underrun does not

cause the TxFIFO to be flushed. In ASYNC mode, operation resumes when CTSN is asserted again. In COP and BOP modes, the transmission of the message is terminated and operation of the transmitter will not resume until CTSN is asserted and a TSOM or TSOMP command is invoked. Prior to issuing the command and re-transmitting the message, the transmitter should be reset, to flush the TxFIFO.

CTSN 'asserted/negated' always refers to the internal CTSN signal after being sampled by the input sampling circuit (see ICTSR[4]). After a change-of-state of CTSN is established by the input sampling circuits (refer to the description of ICTSR[4]), it is sampled by the Tx controller 1 1/2 bit times before each new character is serialized out of the Tx shift register. (This is 2 1/2 bits before the LSB of the new character appears on the TxD pin; there is an additional 1 bit delay in the transmitter data path due to the data encoding logic.)

RECEIVER

The receiver data path includes two holding registers, HSRH and HSRL, an 8-bit character comparison register, CCSR, two synchronizing flip flops, a receiver shift register, RxSR, the SYN comparison registers, S1R and S2R, and BISYNC character comparison logic. The CDUSCC configures this circuitry and utilizes it according to the mode selected for the channel through the two mode registers CMR1 and CMR2. For all paths, character data is assembled according to the character bit count in the RxSR, and is moved to the RxFIFO with any appended status bits when assembly is completed. Figure 47 depicts the four data paths created in the CDUSCC for the various protocols.

Receiver RxFIFO, RxRDY

The receiver converts received serial data on RxD (LSB first) into parallel data according to the transmission format programmed. Data is shifted through a synchronizing flip flop and one or more shift registers, the last of which is the 8-bit receiver shift register (RxSR). Bits are shifted into the RxSR on the rising edge of each 1X receive clock until the LSB is in RxSR[0]. Hence, the received character is right justified, with all unused bits in the RxSR cleared to zero. A receive character length counter generates a character boundary signal for synchronization of character assembly, character comparisons, break detection (ASYNC), and RxSR to RxFIFO transfers (except for BOP residual characters). During COP and BOP hunt phases, the SYN/FLAG comparison is made each receive bit time, as are ABORT and IDLE comparisons in BOP modes.

An internal clock from the BRG, the DPLL or the counter/timer, or an external 1X or 16X clock may be used as the receiver clock in ASYNC mode. The BRG or counter/timer should not be used directly for the receiver clock in synchronous modes, since these modes require a 1X receive clock that is in phase with the received data. This clock may come externally from the RTxC or TRxC pins, or it may be derived internally from the DPLL. Received data is internally converted to NRZ format for the receiver circuits by using clock pulses generated by the DPLL.

When a complete character has been assembled in the RxSR, it is loaded into the receive FIFO with appended status bits. The most significant data bits of the character are set to zero if the character length is less than eight bits. In ASYNC and COP modes the user may select, via RPR[3], whether the data transferred to the FIFO includes the received parity bit or not. The receiver indicates to the CPU or DMA controller that it has data in the FIFO by asserting the channel's RxRDY status bit (GSR[4] or GSR[0] and, if in DMA mode, the corresponding receiver DMA request pin.

The RxFIFO consists of sixteen 8-bit holding registers with appended status bits for character count complete indications (all protocol modes), character compare indication (ASYNC), EOM indication (BISYNC/BOP), and parity, framing, CRC errors and other status bits. Data is loaded into the RxFIFO from the RxSR and extracted (read) by the CPU or DMA controller via the data bus. A RxFIFO read creates an empty RxFIFO position for new data from the RxSR. RxRDY assertion depends on the state of OMR[3]:

1. If OMR[3] is 0 (FIFO not empty), RxRDY is asserted each time a character is transferred from the receive shift register to the receive FIFO. If it is not reset by the CPU, RxRDY remains asserted until the receive FIFO becomes empty, at which time it is automatically negated. If it is reset by the CPU, it will remain negated, regardless of the current state of the receive FIFO, until a new character is transferred from the RxSR to the RxFIFO.

2. If OMR[3] is 1 (FIFO full), RxRDY is asserted:
   a. When a character transfer from the receive shift register causes RxFIFO to reach threshold levels.
   b. When a character with a tagged EOM status bit is loaded into the FIFO (BISYNC or BOP) regardless of RxFIFO full condition.
   c. When the counter/timer is programmed to count received characters and the character which causes it to reach zero count is loaded into the FIFO (ICTSR[6]).
   d. When the beginning of a break is detected in ASYNC mode regardless of the RxFIFO full condition.
   e. WDT is timed out.

If it is not reset by the CPU, RxRDY remains asserted until the FIFO becomes empty, at which time it is automatically negated. If it is reset by the CPU, it will remain negated regardless of the current state of the receive FIFO, until it is asserted again due to one of the above conditions. A write operation to GSR register is not recommended while Rx/Tx are active.

The assertion of RxRDY causes an interrupt to be generated if IER[4] and the channel's master interrupt enable (ICR[0]) or ICR[1]) are asserted.

When DMA operation is programmed, the RxRDY status bit is routed to the DMA control circuitry for use as the channel receiver DMA request. Assertion of RxRDY results in assertion of RTxDRQN output.

Several status bits are appended to each character in the RxFIFO. When the FIFO is read, causing it to be 'popped', the status bits associated with the new character at the top of the RxFIFO are logically ORed into the RSR. Therefore, the user should read RSR before reading the RxFIFO in response to RxRDY activation. If character-by-character status is desired, the RSR should be read and cleared each time a new character is received. The user may elect to accumulate status over several characters or over a frame by clearing RSR at appropriate times. This mode would normally also be used when operating in DMA mode.

DMA Frame Status Byte: In RxDMA cycle, this status byte can be loaded into the FIFO following last byte of frame (last byte means data with EOM status bit set). This byte is updated frame-by-frame by logical 'ORing' of prior status bytes with the present status of the frame and only used for COP or BOP/BOPL modes while DMA transfers are in progress. The EOM status (RSR[7]) will not be set until this byte pops to the top of the FIFO. The DONEN(EOPN) is asserted while this byte is being read out from RxFIFO.

DONEN(EOPN) in DFSB Mode:

(i) If ABORT generate DONEN output: ABORT detect will push DFSB into FIFO, if DFSB enabled, and then clear DFSB for the next frame. (No dummy byte for this case.) If DFSB is not enabled, a dummy byte is pushed into FIFO. Whenever either the DFSB or dummy byte pops to the top of the RxFIFO, the DONEN signal will be asserted.

(ii) If ABORT not generate DONEN: No matter whether DFSB is enabled or not, a dummy byte is always pushed into the FIFO to indicate the location where the ABORT occurs. DFSB, if enabled, is not cleared and accumulated with next frame.

(iii) Short frame is similar to ABORT except short frame doesn't generate dummy byte. If DFSB and DONE/Short Frame are enabled, then DFSB is forced into FIFO when short frame occurs while Rx shift register is enabled. Otherwise no DFSB can be forced into FIFO.

On the subject of ABORT/DONEN, case (ii) is meant for a default NMOS compatible mode. If the command has not been set, the CDUSCC will operate like the existing NMOS. In this case, the CDUSCC could still use the DFSB without generating DONEN on ABORT. What the CDUSCC will do when it encounters an ABORT is simply set the ABORT status bit, reset the receiver and look for the next frame. The DFSB is not cleared and is accumulating through the next frame until a closing flag is found. It is important to point out if this mode is used, the user will see the ABORT bit set in the DFSB and that means he has at least two frames within the data buffer he received. The first n–1 frames have been terminated with an ABORT sequence (n is the total number of frames in the buffer).

In all protocol modes, the CDUSCC protects the contents of the FIFO and the RxSR from overrun. If a character is received while the FIFO is full and a character is already in the RxSR waiting to be transferred into the FIFO, the overrunning character is discarded and the OVERRUN status bit (RSR[5]) is asserted. If the overrunning character is an end-of-message character, the character is lost but the FIFOed EOM status bit will be asserted when the character in the RxSR is loaded into the FIFO.

Operation of the receiver is controlled by the enable receiver command. When this command is issued, the CDUSCC goes into the search for start bit state (ASYNC), search for SYN state (COP modes), or search for FLAG state (BOP modes). When the disable receiver command is issued, the receiver ceases operation immediately, but RxFIFO will retain its contents. The RxFIFO is cleared on master reset, or by a reset receiver command. However, disabling the receiver does not affect the RxFIFO, RxRDY, or DMA request operation.

Receiver DCD Control

If DCD enable Rx, RPR[2], is asserted, the DCD input must be asserted for the receiver to operate. If RPR[2] is asserted and the sampling circuit detects that the DCD input has been negated while a character is being received, the receiver terminates receipt of the current message (this action, in effect, disables the receiver). If DCD is subsequently asserted, the receiver will search for the start bit, SYN pattern, or FLAG, depending on the channel protocol. A change of state detector is provided on the DCD input of each channel. The required duration of the DCD level change is described in the discussion of ICTSR[5]. The user may program a change of state to cause an interrupt to be generated so that appropriate action can be taken.

Receiver RTS Control

In ASYNC mode, RPR[4] can be programmed to control the deactivation of the RTSN output by the receiver. RTSN can be manually asserted and negated by writing to OMR[0]. However, the assertion of RPR[4] causes RTS to be negated automatically upon receipt of a valid start bit if the channel's receive FIFO is already full (16 characters). When this occurs, the RTSN negated status bit, RSR[6], is set. The RTSN will be re-asserted again when RxFIFO becomes "not full". This may be used as a flow control feature to prevent overrun in the receiver by using the RTSN output signal to control the CTSN input of the remote transmitter. The new character will be assembled in the RxSR, but its transfer to the FIFO will be delayed until the CPU reads the FIFO, making the FIFO position available for the new character.

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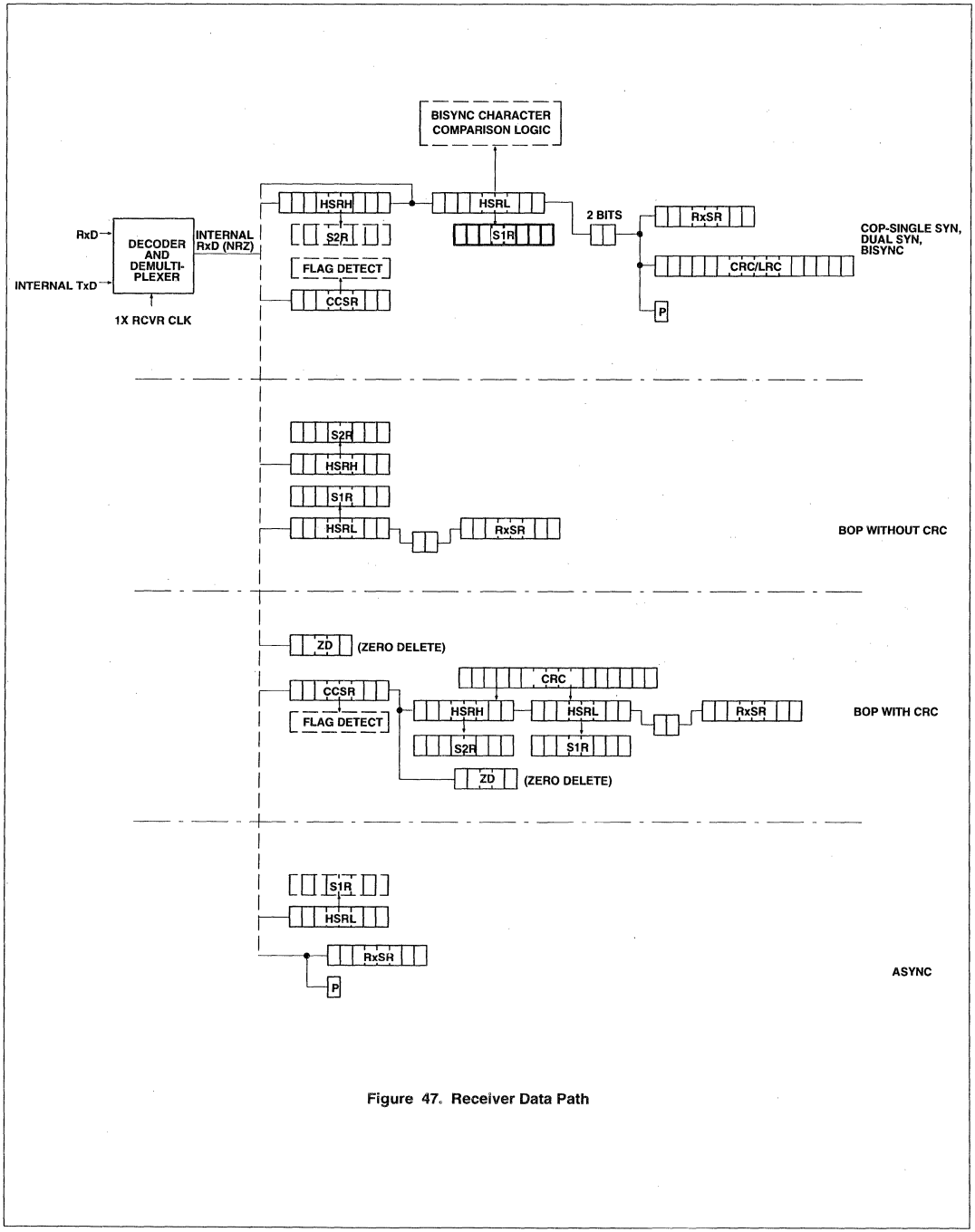

Figure 47. Receiver Data Path

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Data Communications

SECTION 3

PROTOCOL DEPENDENT FEATURES

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ASYNC OPERATIONAL MODE

To operate a channel of the CDUSCC in ASYNC Mode, the Channel Mode Register 1 (CMR1) must specify ASYNC via bits [2:0] = 111. In ASYNC Mode, the CMR1, CMR2, S1R, TPR, and RPR take on the bit definitions illustrated in Figures 48 through 56.

Tx ASYNC Mode

When in the active state, serialization will begin when the TxFIFO data is loaded into the TxSR. The transmitter first sends a start bit, then programmed number of bits/character (TPR[1:0]), a parity bit (if specified), and the programmed number of stop bits. Following the transmission of the stop bits, if a new character is not available in the TxFIFO, the TxD output goes to marking and the underrun condition (TRSR[7]) is set. A new character could be unavailable to the TxSR because of any of three conditions:

- The TxFIFO is empty
- A disable Tx or Reset Tx has been sent to the CCR
- CTS has been de-asserted and CTS enable Tx operation was selected (TPR[2] is set).

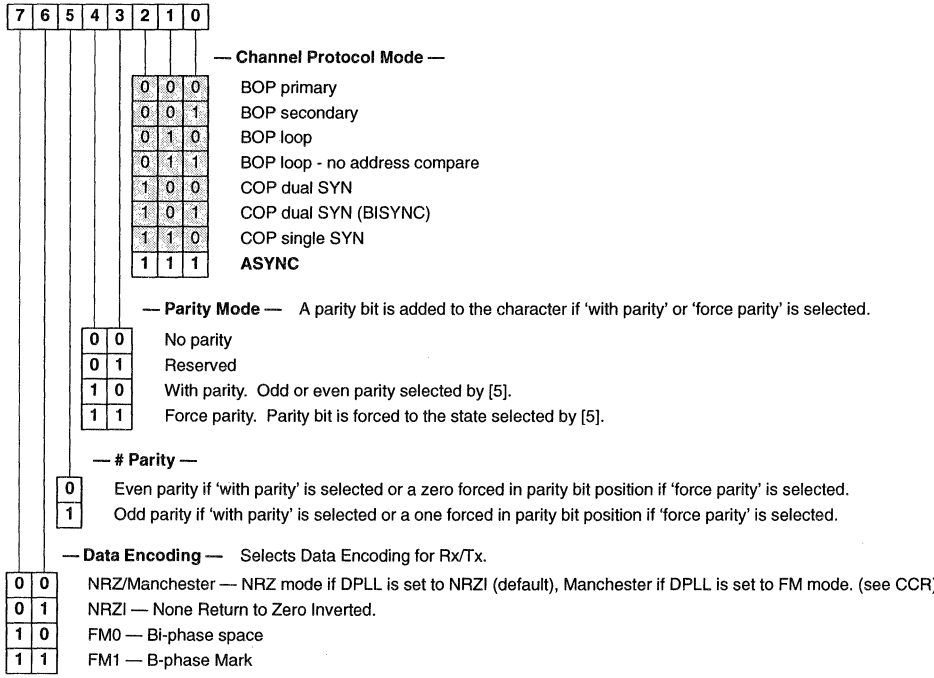
Any of the above conditions will return the transmitter to the quiescent state.

The Transmitter re-enters the active state because of either of the following:

- A new character is loaded into the TxFIFO
- A 'SEND BREAK' command (TABRK) is sent to the CCR

While the transmitter is enabled and CTS is asserted (if CTS enable Tx mode has been selected), the send break command clears the TxFIFO and forces a continuous space (low) on the TxD output after the character in TxSR (if any) is serialized. A send break acknowledge (TRSR[4]) is returned to the CPU to facilitate re-assertion of the send break command in order to send an integral number of break characters. The send break condition is cleared when the reset Tx or disable Tx command is issued.

Figure 48. CMR1A (B) Channel Mode Register 1 [ASYNC Mode]



NOTE: No encoding is supported for ASYNC mode with fractional stop bits selected in TPR[7:4].

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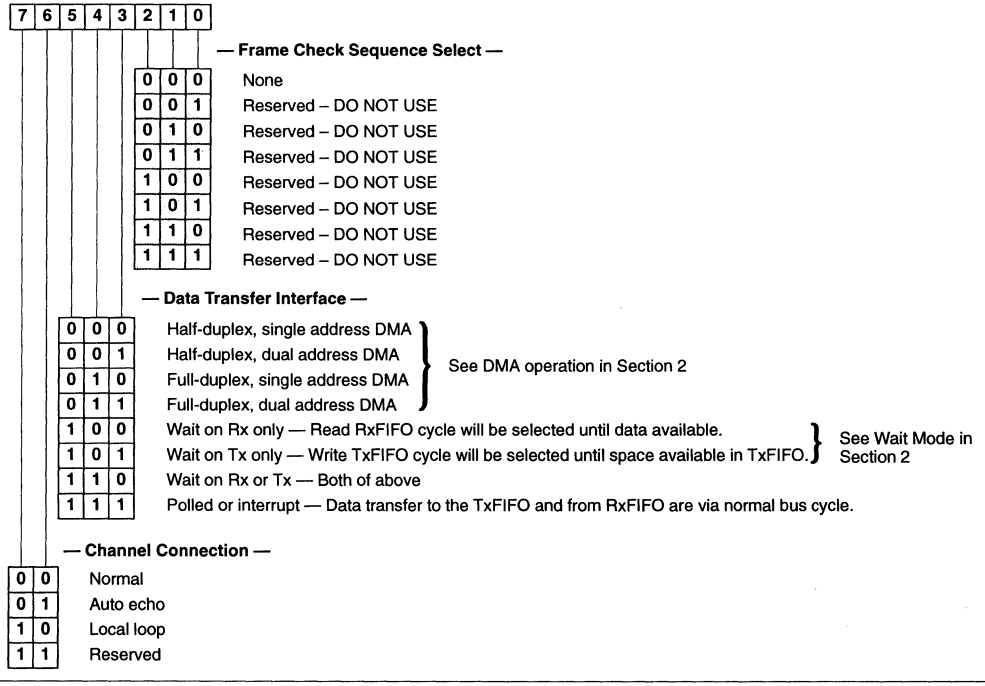
Figure 49. CMR2A (B) Channel Mode Register 2 [ASYNC Mode]



Channel Mode Register 2 (CMR2A, CMR2B)

Channel Connection

This field selects the mode of operation of the channel. The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character.

Normal mode: The transmitter and receiver operate independently in either half- or full-duplex, controlled by the respective enable commands.

Automatic echo mode: Automatically re-transmits the received data with a half-bit time delay (ASYNC, 16X clock mode) or a two-bit time delay (all other modes). The following conditions are true while in automatic echo mode:

1. Received data is re-clocked and re-transmitted on the TxD output.
2. The receiver clock is used for the transmitter for Async 16X clock mode. For other modes the transmitter clock must be selected and supplied through normal methods as described in Section 2.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The TxRDY and underrun status bits are inactive.
5. The received parity and/or FCS are checked if required, but are not regenerated for transmission, i.e., transmitted parity and/or FCS are as received.
6. In ASYNC mode, character framing is checked, but the stop bits are re-transmitted as received. A received break is echoed as received.
7. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Local loopback mode: In this mode:

1. The transmitter data output and clock are internally connected to the receiver.
2. The transmit clock is used for the receiver if NRZI or NRZ encoding is used. For FM or Manchester encoding because the receiver clock is derived from the DPLL, the DPLL source clock must be maintained.
3. The TxD output is held High.
4. The RxD input is ignored.
5. The receiver and transmitter must be enabled.
6. CPU to transmitter and receiver communications continue normally.

The above discussion for CMR2 also applies to COP and BOP modes.

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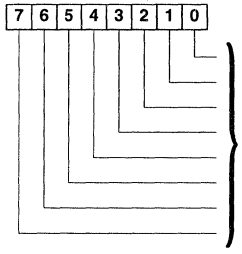
Figure 50. S1RA (B) SYN1/Secondary Address Register 1 [ASYNC Mode]



The value loaded into this register will be compared to the value clocked into the RxSR. If an exact match occurs, a status bit is set (RSR[7] in Receiver Status Register (RSR)). The comparison is always made on entire 8-bit value. If character is received with parity error (if specified) the comparison will not occur. For characters less than 8-bits long, the bits should be right justified with the 'unused' MSBs set to zero.
The Status is FIFOed and will appear in the RSR when matched character reaches top of the RxFIFO.

Figure 51. TPRA (B) Transmitter Parameter Register [ASYNC Mode]

7 6 5 4 3 2 1 0

— Tx Character Length — This field selects the number of data bits transmitted per character.

0 0	5 bits
0 1	6 bits
1 0	7 bits
1 1	8 bits

— CTS Enable Tx — This bit determines if the CTSN input controls the operation of Tx. See Tx CTS operation in Section 2

0	No
1	Yes

— Tx RTS Control — This bit controls the de-activation of the RTSN output by the Tx. See Tx RTS operation in Section 2

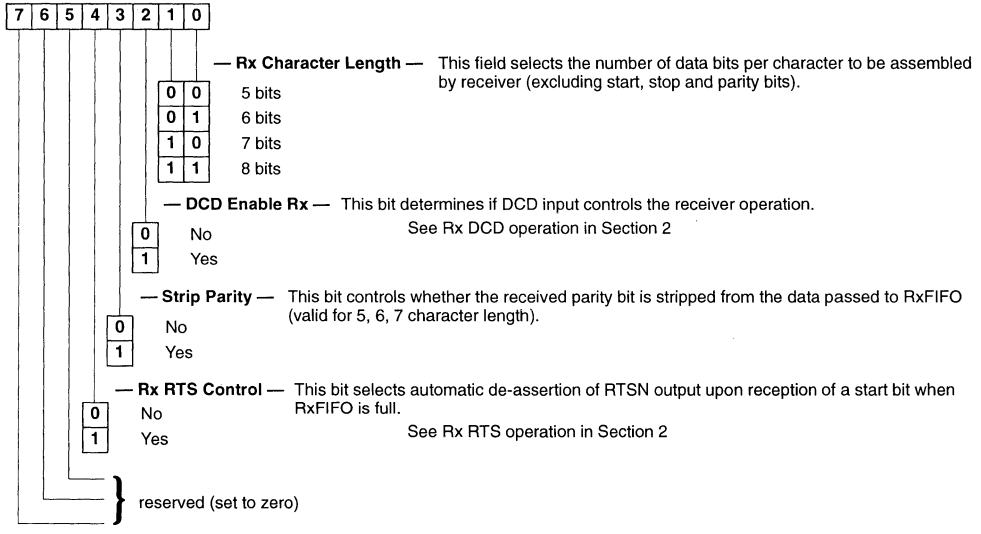
0	No
1	Yes

— Stop Bits Per Character — This field selects the number of stop bits to be transmitted with each character.

STOP BIT VALUE

				5 BITS/ CHAR	6,7 OR 8 BITS/CHAR
0	0	0	0	1.063	0.563
0	0	0	1	1.125	0.625
0	0	1	0	1.188	0.688
0	0	1	1	1.250	0.750
0	1	0	0	1.313	0.813
0	1	0	1	1.375	0.875
0	1	1	0	1.438	0.938
0	1	1	1	1.500	1.000
1	0	0	0	1.563	1.563
1	0	0	1	1.625	1.625
1	0	1	0	1.688	1.688
1	0	1	1	1.750	1.750
1	1	0	0	1.813	1.813
1	1	0	1	1.875	1.875
1	1	1	0	1.938	1.938
1	1	1	1	2.000	2.000

Figure 52. RPRA (B) Receiver Parameter Register [ASYNC Mode]



Rx ASYNC Mode

When first enabled, the receiver goes into the search for start bit state, looking for a high-to-low (mark-to-space) transition of the start bit on the RxD input. If a transition is detected, the state of the RxD pin is sampled again each 16X clock for 7 1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start is invalid and the search for a valid start bit begins again.

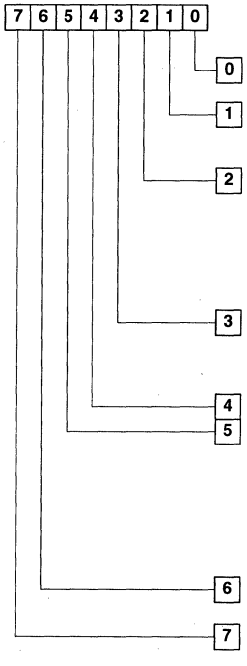
If RxD is still Low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals (16 periods of the 16X Rx clock; one period of the 1X Rx clock) at the theoretical center of the bit, until the proper number of data bits and the parity bit (if specified) have been assembled, and the first stop bit has been detected.

The assembled character is then transferred to the RxFIFO with appended parity error (if parity is specified) and framing error status bits. The CDUSCC can be programmed to compare this character to the contents of S1R. The appended character compare status bit, RSR[7], is set if the data matches and there is no parity error.

After the stop bit is sampled, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (i.e. framing error) and RxD remains Low for one-half of the bit period after the stop bit has been received, the receiver operates as if a new start bit transition (without high-to-low transition) had been detected.

If a break condition is detected (RxD Low for entire character time including optional parity and first stop bit), only one character consisting of all zeros will be loaded into the RxFIFO and break start detect, RSR[2], will be set. The RxD input must return to a High condition for at least one half to one bit time (16X clock mode) or for one bit time (1X clock mode) before the break condition is terminated and the search for the next start bit begins. At that time, the break end detect condition, RSR[3], is set.

Figure 53. RSRA (B) Receiver Status Register [ASYNC Mode]



The logical OR of these bits is presented in GSR[2] or GSR[4]. Certain bits are FIFOed in status FIFO. As the data is brought to the top of RxFIFO, the status bits are logically ORed. This register should be cleared if character-by-character status is desired.

0 Parity error*# – The parity bit of the received character was not as expected. A parity error does not affect the parity bit put into the FIFO as part of the character when strip parity (RPR[3]) is negated.

1 Framing error*# – At the first stop bit position the RxD input was in the Low (space) state. The receiver only checks for framing error at the nominal center of the first stop bit regardless of the number of stop bits programmed in TPR[7:4]. This bit is not set for BREAKS.

2 BRK start detect* – An all zero character, including parity (if specified) and first stop bit, was received. The receiver will be capable of detecting breaks which begin in the middle of a previous character. Only a single all-zero character will be put into the FIFO when a break is detected. Additional entries to the FIFO are inhibited until the end of break has been detected (see above) and a new character is received. The RxRDY status bit is asserted immediately upon a Break Start Detect (regardless of RxFIFO threshold) so that transfer of any data bytes in the RxFIFO (including the Break 00h character) will not be delayed.

3 BRK end detect – 1X clock mode: The RxD input has returned to the marking state for at least one period of the 1X receiver clock after detecting a BREAK. 16X clock mode: The RxD input has returned to the marking (High) state for at least one-half bit time after detecting a BREAK. A half-bit time is defined as eight clock cycles of the 16X receiver clock.

4 Not used

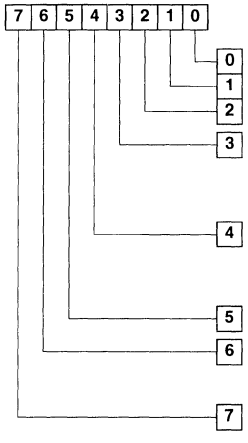
5 Overrun error* – A new character was received while the receive FIFO was full and a character was already waiting in the receive shift register to be transferred to the FIFO. The DUSCC protects the 17 characters previously assembled (16 in RxFIFO, 1 in the Rx shift register) and discards the overrunning character(s). After the CPU reads the FIFO, the character waiting in the RxSR will be loaded into the available FIFO position. This releases the RxSR and a new character assembly will start at the next character boundary. In this way, only valid characters will be assembled, i.e., no partial character assembly will occur regardless of when the RxSR became available during the incoming data stream.

6 RTS negated – The RTSN output was negated due to receiving the start bit of a new character while the RxFIFO was full (see RPR[4]).

7 Character compare*# – If the counter/timer is programmed to count received characters, this bit is asserted when the character which causes the count to go to zero is loaded into the receive FIFO. It is also asserted to indicate that the character currently at the top of RxFIFO matched the contents of S1R. A character will not compare if it is received with parity error even if the data portion matches.

*FIFOed with data in extended mode (CDUSCC)
#FIFOed with data in default mode (NDUSCC)

Figure 54. TRSRA (B) Transmitter and Receiver Status Register [ASYNC Mode]



All these bits are reset by asserting RESETN or by writing '1' in the bit locations. Bits [7:4] are reset by Reset Tx and bits [3:0] by Reset Rx commands.

Not used (set to 0)

DPLL error – Set while the DPLL is operating in FM mode to indicate that a data transition was not detected within the detection window for two consecutive bits and that the DPLL was forced into search mode. This feature is disabled when the DPLL is specified as the clock source for the transmitter via TTR[6:4].

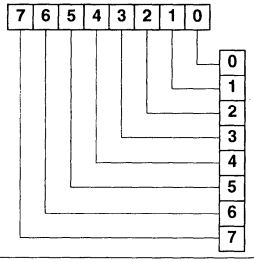
Send break ACK – Set when the transmitter begins transmission of a break in response to the send break command. If the command is reinvoked, the bit will be set again at the beginning of the next character time. The user can control the length of the break by counting character times through this mechanism.

Not used (set to 0)

CTS underrun – This bit is set only if CTS enable Tx (TPR[2]) is asserted. It indicates that the transmit shift register was ready to begin serializing a character and found the CTSN input negated. In ASYNC mode, this bit will be reasserted if cleared by the CPIU while the CTSN input is negated.

Transmitter underrun – Indicates that the transmit shift register has completed serializing a character and found no other character to serialize in the TxFIFO. The bit is not set until at least one character from the transmit FIFO has been serialized. The TxD output is held in the MARK state until another character is loaded into the TxFIFO. Normal operation then continues.

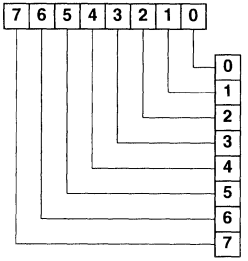
Figure 55. IER1A (B) Interrupt Enable Register 1 [ASYNC Mode]



This register allows user to enable each individual status bit to cause interrupt. Writing '1' in the bit position will enable this feature. Master interrupt should also be enabled through ICR or IER3.

0 Parity error
1 Frame error
2 BRK start
3 BRK end
4 Reserved
5 Overrun
6 RTS negated
7 Character comparison

Figure 56. IER2A (B) Interrupt Enable Register 2 [ASYNC Mode]



This register allows user to enable each individual status bit to cause interrupt. Writing '1' in the bit position will enable this feature. Master interrupt should also be enabled through ICR or IER3.

0 Delta DCD detect
1 Delta CTS detect
2 DPLL error
3 Send break ACK
4 CTS underrun
5 Tx underrun
6 Reserved
7 Tx path empty — Enables interrupt when Tx is enabled, data serialized from TxFIFO has been transmitted and there is no data in TxFIFO and TxSR.

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Synchronous Operation Overview

Operation of CDUSCC in synchronous modes differs substantially from ASYNC operation. This is due in part to the requirements set forth by the synchronous protocols, and in part due to the need for the sequence.

In the description that follows, the following terminology will be used (see also Appendix II):

SYN - A unique pattern of bits used to establish BYTE or FRAME synchronization in COP protocols.

FLAG - A unique pattern of bits (01111110) used to establish FRAME synchronization in BOP protocols.

PAD - Protocol often requires an 'opening PAD' which is a bit pattern used to synchronize the clock recovery hardware at the receiving end. The CDUSCC transmitter is capable of producing an opening PAD by use of the '**T**ransmit **S**tart **O**f **M**essage with **P**AD' (TSOMP) command issued via the CCR.

FRAME - The message information, including header and error correction information. The frame is bounded by a SYN (or FLAG) pattern at its start and end. The SYN (or FLAG) may be optionally preceded by an opening PAD. The ending SYN (FLAG) may be optionally followed by a closing PAD. The frame is sometimes referred to as a 'BLOCK' in some protocols.

IDLE - The state of the line when a frame is not being transmitted.

UNDERRUN - The state of the line when a frame is being transmitted, but the transmitter has run out of actual data for the moment, and needs 'LINE-FILL' characters to maintain bit and byte synchronization at the receiver end.

FCS - Frame Check Sequence, the error detection pattern (CRC, LRC) included at the end of the frame to ensure the integrity of the data of the frame. Sometimes referred to as the BCC or Block Check Character in some protocols.

BIT ORIENTED PROTOCOL

BOP Operational Mode

To operate a channel of the CDUSCC in BOP Mode, the channel Mode Register 1 (CMR1) must specify BOP via bits [2:0] = 000 through 011. In BOP Mode the CMR1, CMR2, S1R,S2R, TPR and RPR take on the bit definitions illustrated in Figures 57 through 62, respectively,

TxBOP Modes

Transmitter commands associated with BOP modes are TSOM, TSOMP, TEOM and transmit ABORT (TABRK).

Figure 57. CMR1A (B) Channel Mode Register 1 [BOP Mode]

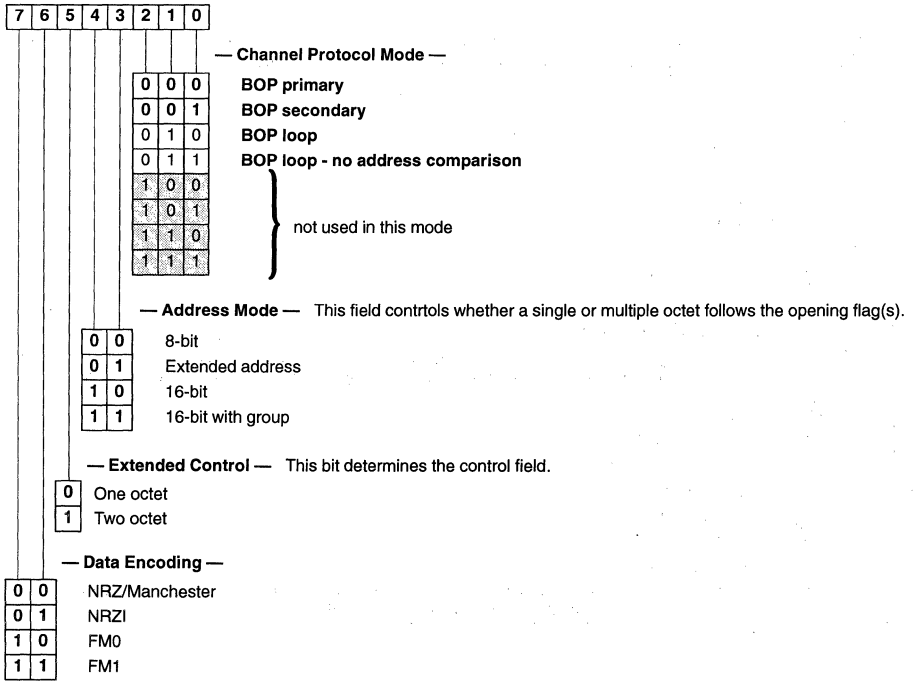

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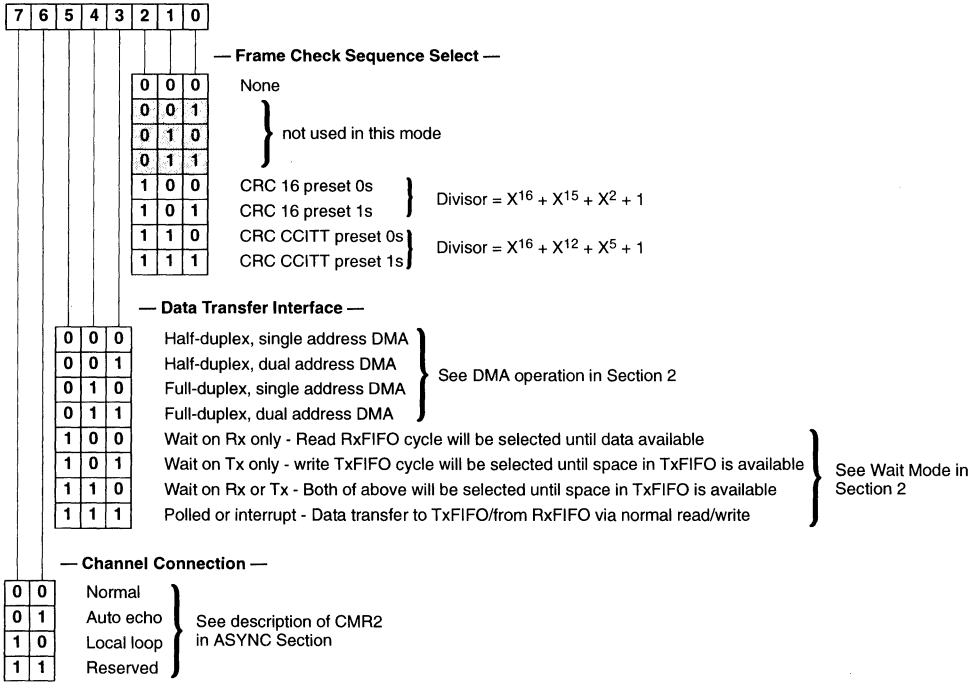
Figure 58. CMR2A (B) Channel Mode Register 2 [BOP Mode]



Starting Transmission

A TSOM or TSOMP command must be issued to start BOP transmission. TSOM (without PAD) causes the TxCRC/LRC generator to be initialized and a FLAG character to be loaded into the TxSR and shifted out on the TxD output.

Send SOM acknowledge (TRSR[4]) is asserted when the FLAG output begins. The user may re-invoke the command to cause multiple FLAGs to be transmitted. If the command is not re-invoked and the TxFIFO is empty, FLAG patterns continue to be transmitted until the TxFIFO is loaded. If data is present in the FIFO, the first character is loaded into the TxSR and serialization of the data begins. Note that the TxFIFO may be pre-loaded with data before the TSOM is issued.

The TSOMP command causes all characters in the TxFIFO (PAD characters) to be loaded into the TxSR and serialized if the Tx is enabled. Unlike the transmit SOM without PAD command, data (non-PAD characters) cannot be pre-loaded into the TxFIFO. If data is loaded into TxFIFO during transmission of PAD, it will be treated as PAD character. While the PAD is transmitted, the character length is automatically set to 8 bits regardless of the value in TPR[1:0]. When the TxFIFO becomes empty after the PAD, the TxCRC/LRC generator is initialized, the FLAG is transmitted, and send SOM acknowledge asserted. Operation then proceeds in the same manner as the TSOM command; the user has the option to invoke the TSOM command to cause multiple FLAGs to be transmitted.

There is no zero insertion (see below) during transmission of the PAD characters, and they are not preceded by a FLAG or accumulated in the CRC. Character length of the PAD characters is automatically set to 8 bits regardless of TPR[1:0].

Address and Control Field Transmission

In this protocol, the first characters loaded into the TxSR from the TxFIFO are the address and control fields, which have fixed character lengths of eight bits. The number of address field bytes is determined by CMR1[4:3]. If extended address field is specified, the field is terminated if the first address octet is H'00' or if the LSB of the octet is a 1. The number of control field bytes is selected by CMR1[5]. If any information field characters follow the control field (forming an I field), they are transmitted with the number of bits per character programmed in TPR[1:0].

Figure 59. S1RA (B) SYN1/Secondary Address Register 1 [BOP]

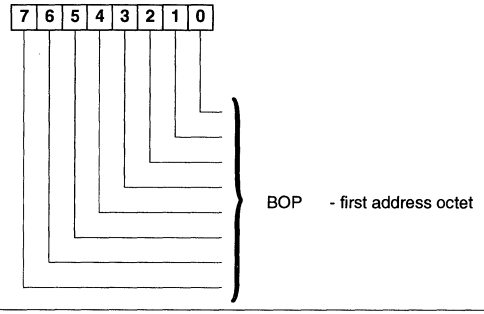


Figure 60. S2RA (B) SYN2/Secondary Address Register 2 [BOP]

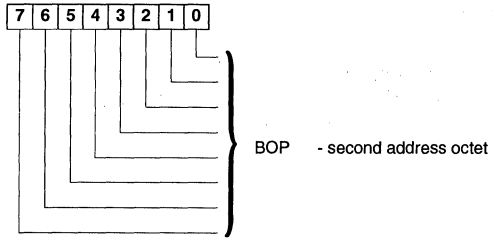
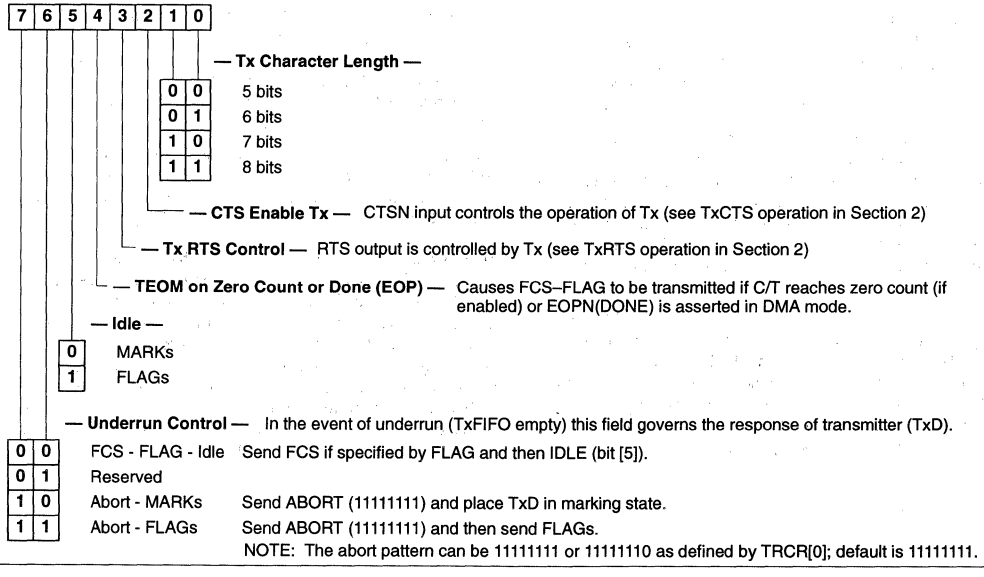


Figure 61. TPRA (B) Transmitter Parameter Register [BOP Mode]



Information Field Transmission and Underrun

After the opening FLAG and first address octet have been transmitted, an underrun occurs (TRSR[7] = 1) if the TxFIFO is empty when the transmitter requires a new character. The underrun control bits (TPR[7:6]) determine whether the transmitter line fills with either ABORT-MARKs, ABORT-FLAGs (see below), or ends transmission with the 'normal' end of message sequence. For ABORT-MARKs (TPR[7:6] = 10) and for ABORT-FLAGs (TPR[7:6] = 11), and also after a 'Transmit Abort' command, a new TSOM command must be issued to resume transmission. For FCS-FLAG-idle (TPR[7:6] = 00), see below. Regardless of TPR[7:6], a TSOMP command is ignored, except after a CTS underrun, unless the transmitter is disabled or reset and then re-enabled.

EOM on underrun is functionally similar to EOM due to an appended TEOM command. If the EOM is due to underrun, the normal character length applies to the last data character. After the last character is transmitted, the FCS (inverted CRC) and closing FLAG are sent, frame complete (TRSR[5]) is set and the TxCRC is initialized. If the TxFIFO is empty after the closing FLAG has been sent, TxD will assume the programmed idle state of FLAGs or MARKs (TPR[5]). For TPR[5] = 1 (idle = FLAGs), transmission will resume, with or without a TSOM command, when data are loaded into the TxFIFO. For TPR[5] = 0 (idle = MARKs), a new TSOM command must be issued. If the TxFIFO is not empty at that time, the TxFIFO data will be loaded into the TxSR and serialized. In that case, the closing FLAG is the opening FLAG of the next frame.

Ending Transmission

An appended TEOM command also terminates the frame as described above. It occurs after transmission of the character to which the TEOM is appended. The TEOM command can be explicitly asserted through the channel command register. If TPR[4] = '1', the TEOM is automatically appended to a character in DMA mode, if the EOPN input is asserted when that character is loaded into the TxFIFO, or if the counter/timer is counting transmitted characters, when the character which causes the counter to reach zero count is loaded.

Tx Residual Character Length

The information field of a BOP frame can be any arbitrary number of bits. Since the CDUSCC operates on a byte or character basis (TPR[1:0] number of bits/character). A method has been provided to easily transmit the residual bits remaining in a frame that is not an integer multiple of the specified character length, with a resolution of one bit.

When the character with the appended TEOM is loaded from the TxFIFO, it is transmitted with the character length specified by OMR[7:5]. In this way, a residual character of 1-8 bits is transmitted with out requiring the CPU to change the Tx character length for this last character.

Caution

If the Tx residual character length is not programmed, it will default to value of 1 bit (OMR[7:5] = 000). So, the Tx will send out only 1 bit of the last character. Be sure to program the Tx residual character length correctly.

Control of Number of FLAGs Between Frame

The CDUSCC provides automatic generation of FLAGs between frames (TPR[5] = 1). In certain situations the user may wish to control the precise number of FLAGs between frames. In that case, the user controls the number of FLAGs between frames by invoking the TSOM command after frame complete is asserted. The CDUSCC then operates in the same manner as for transmission of multiple FLAGs at the start of a frame.

When the command is no longer re-invoked, transmission of the TxFIFO data will begin. If the FIFO is empty, FLAGs continue to be transmitted.

Zero Insertion

The CDUSCC provides automatic zero insertion in the data stream to prevent erroneous transmission of the FLAG sequence. All data characters loaded into the TxSR from the TxFIFO and characters transmitted from the CRC generator are subject to zero insertion. For this feature a zero is inserted in the serial data stream each time five consecutive ones (regardless of character boundaries) have been transmitted.

Abort Transmission

A TABRK command clears the TxFIFO and inserts an ABORT character of eight or seven ones (not subject to zero insertion) into the TxSR for transmission after the current character has been serialized. A send ABORT ACK (TRSR[4]) facilitates re-assertion of send abort by the user to guarantee transmission of multiple abort characters. This feature can be used to send the 15-ones IDLE sequence.

The transmitter sends either marks or FLAGs after the abort character(s) has been transmitted, depending on TPR[7:6]. Operation resumes with the transmission of a FLAG when a TSOM command is invoked. A TSOMP command is ignored, except after a CTS underrun, unless the transmitter is disabled or reset and then re-enabled.

TxCRC Accumulation

CRC accumulation can be specified in all BOP modes. The type of CRC is specified via CMR2[2:0], and is normally selected as CRC-CCITT preset to ones, although any option is valid. Note that LRC8 option is not allowed in BOP modes.

The TSOM/TSOMP command sets the CRC accumulator to its initial state and accumulation begins with the first address octet after the initial FLAG(s). Accumulation stops when transmission of the first character of the FCS begins. The CPU can set the accumulator to its initial state prior to the transmission of any character by using the appended reset CRC command and can exclude any character from the accumulation by use of the exclude from CRC command, but these features would not normally be used in BOP modes. The CRC generator is also automatically initialized after EOM or an ABORT is sent.

Table 15. Underrun Control

TPRA[7:6]	Protocol	TxD Line During Underrun
00	BOP	FLAG following either FCS (if selected) or last data character, then idle
	COP	Last byte of FCS (if selected) or last data character, then idle
10	BOP	Abort sequence after last data character, then send MARKs
	COP	MARKs
11	BOP	Abort sequence after last data character, then send FLAGs
	COP	Last character of SYN sequence, the SYN sequence being SYN1, SYN1/2 or DLE/SYN1 for single SYN, dual SYN and BISYNC, respectively.

Figure 62. RPRA (B) Receiver Parameter Register [BOP Mode]

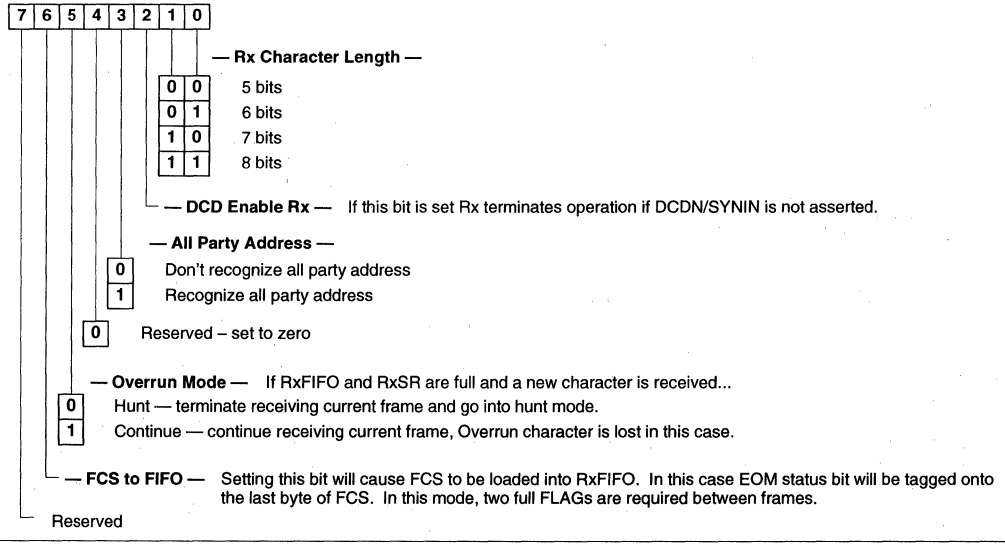


Figure 63. RSRA (B) Receiver Status Register [BOP Mode]

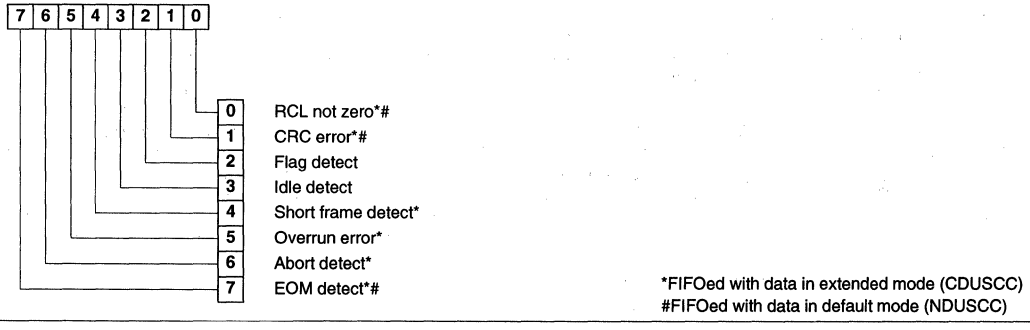
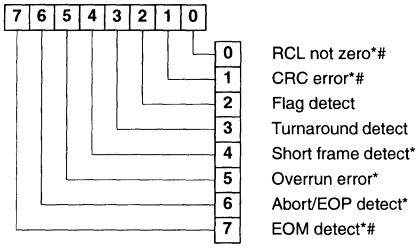


Figure 64. RSRA (B) Receiver Status Register [BOP - Loop Mode]



Receiver Status Register (RSRA, RSRB)

This register informs the CPU of receiver status. Bits indicated as 'not used' in a particular mode will read as zero. The logical OR of these bits is presented in GSR[2] or GSR[6] (ORed with the bits of TRSR) for channels A and B, respectively. Unless otherwise indicated, asserted status bits are reset only by performing a write operation to the status register with the bits to be reset being ones in the accompanying data word, or when the RESETN input is asserted, or when a 'reset receiver' command is issued.

Certain status bits are specified as being FIFOed. This means that they occupy positions in a status FIFO that correspond to the data FIFO. As the data is brought to the top of the FIFO (the position read when the RxFIFO is read), the FIFOed status bits are logically ORed with the previous contents of the corresponding bits in the status register. This permits the user to obtain status either character-by-character or on a block basis. For character-by-character status, the SR bits should be read and then cleared before reading the character data from RxFIFO. For block status, the status register is initially cleared and then read after the message is received. Asserted status bits can be programmed to generate an interrupt (see Interrupt Enable Register).

Bit[7] EOM Detect:
If the counter/timer is programmed to count received characters, this bit is asserted when the character which causes the count to go to zero is loaded into the receive FIFO. It is also asserted to indicate that the character currently at the top of the FIFO was the last character of the frame. If transfer FCS to FIFO (RPR[6]) is asserted, the EOM will be tagged instead onto the last byte of the FCS. Note that if an overrun occurs, the EOM character may be lost, but this status bit will still be asserted to indicate that an EOM was received. This bit will not be set when an abort is received.

Bit[6] ABORT:
BOP: An ABORT sequence consisting of a zero followed by seven ones was received after receipt of the first address octet but before receipt of the closing FLAG. The user should read RxFIFO until it is empty and determine if any valid characters from a previous frame are in the FIFO. If no character with a tagged EOM detect ([7]) is found, all characters are from the current frame and should be discarded along with any previously read by the CPU. An ABORT detect causes the receiver to automatically go into search for FLAG state. An abort during a valid frame does not cause the CRC to reset; this will occur when the next frame begins.

LOOP: Performs the ABORT detect function as described for BOP without the restriction that the pattern be detected during an active frame. A zero followed by seven ones is the end-of-poll sequence which allows the transmitter to go active if the 'go active on poll' command has been invoked.

Bit[5] Overrun Error (all modes):
A new character was received while the receive FIFO was full and a character was already waiting in the receive shift register to be transferred to the FIFO. The CDUSCC protects the characters previously assembled and discards the overrunning character(s). After the CPU read the FIFO, the character waiting in the RxSR will be loaded into the available FIFO position. This releases the RxSR and a new character assembly will start at the next character boundary. In this way, only valid characters will be assembled, i.e., no partial character assembly will occur regardless of when the RxSR became available during the incoming data stream.

Bit[4] Short Frame (BOP/LOOP):
A closing flag was received with missing fields in the frame. See RxBOP mode on following pages for details.

Bit[3] IDLE (BOP), Turnaround (LOOP):
BOP: An IDLE sequence consisting of a zero followed by fifteen ones was received. During a valid frame, an abort must precede an idle. However, outside of a valid frame, an idle is recognized and abort is not.

LOOP: A turnaround sequence consisting of eight contiguous zeros was detected outside of an active frame. This should normally be used to terminate transmitter operation and return the system to the 'echoing RxD' mode.

Bit[2] FLAG Detect (BOP/LOOP):
A FLAG sequence (01111110) was received. Set one bit time after FLAG is detected in CCSR.

Bit[1] CRC Error:
This bit is set upon receipt of the FCS byte(s), if any, to indicate that the received FCS was in error. The bit is normally FIFOed with the last byte of the I field (the character preceding the first FCS byte). However, if transfer FCS to FIFO (RPR[6]) is asserted, this bit is FIFOed with the last FCS byte.

Bit[0] RCL Not Zero (BOP/LOOP):
The last character of the I field did not have the character length specified in RPR[1:0]. The actual received character length of this byte can be read in TRSR[2:0]. This bit is FIFOed with the EOM character but TRSR[2:0] is not. An exception occurs if the command to transfer the FCS to the FIFO is active. In this case, the bit will be FIFOed with the last byte of the FCS, i.e., with REOM. In the event that residual characters from two consecutive frames are received and are both in the FIFO, the length in TRSR[2:0] applies to the last received residual character.

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Figure 65. TRSRA (B) Transmitter and Receiver Status Register [BOP Mode]

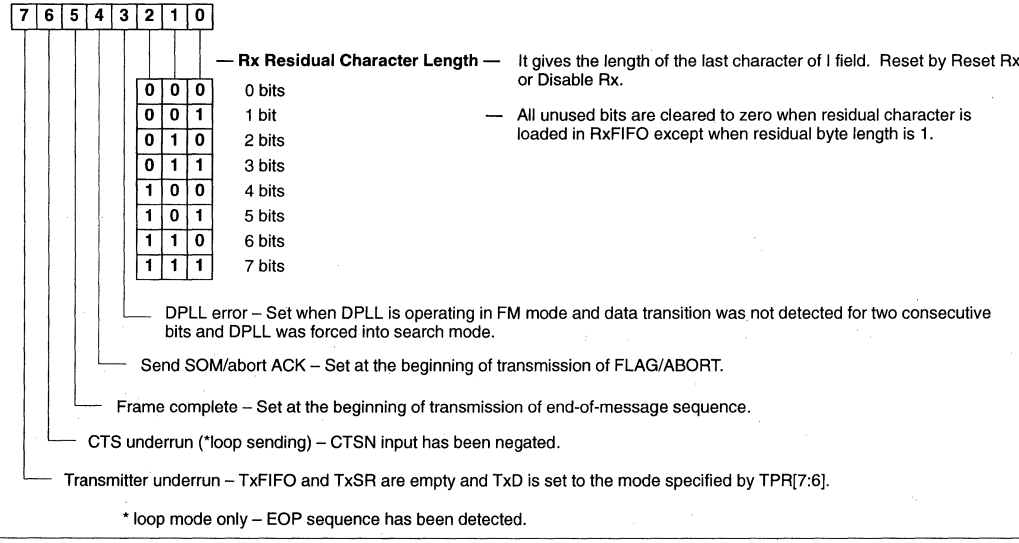


Figure 66. IER1A (B) Interrupt Enable Register 1 [BOP Mode]

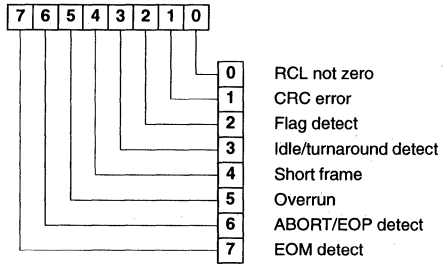
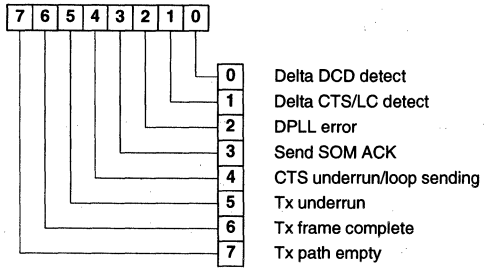


Figure 67. IER2A (B) Interrupt Enable Register 2 [BOP Mode]



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TxBOP Loop Mode

The loop modes are used by secondary stations on the loop, while the primary station operates in the BOP primary mode. Both the transmitter and receiver must be enabled and should be programmed to use the same clock source. Loop operation is initiated by issuing the 'go on-loop' command. The receiver looks for the receipt of seven contiguous ones and then asserts the LCN output to cause external loop control hardware to put the CDUSCC into the loop, with the TxD output echoing the RxD input with a 2-bit time delay. The echoing process continues until a go active on poll (GAP) command is invoked. The CDUSCC then looks for receipt of an EOP bit pattern (a zero followed by seven ones, 11111110) and changes the last one of the EOP into a zero making it an opening FLAG. Loop sending (TRSR[6]) is asserted at that time. The action of the transmitter after sending the initial FLAG depends on the status of the transmit FIFO.

If the transmit FIFO is not empty, a normal frame transmission begins. The operation is then similar to normal BOP operation with the following differences:

1. An ABORT command, an underrun, or receipt of the turn around sequence (H'00') or a FLAG cause the transmitter to cease operation and to revert to echoing the RxD input with a 2-bit time delay. A new transmission cannot begin until the GAP command is re-invoked and a new EOP sequence is received.

2. Subsequent to sending the EOM sequence of FCS-FLAG, the CDUSCC examines the internal GAP flip-flop. If it is not set (having been reset by the 'reset GAP' command), the CDUSCC reverts to echoing the received data. If the internal GAP flip-flop is still set, transmission of a new frame begins, with the user having control of sending multiple FLAGs between frames by use of the 'TSOM' command. If the FIFO is empty at this time, the CDUSCC continues to send FLAGs until the data is loaded into the FIFO or until GAP is reset. If the latter occurs, it reverts to echoing RxD. When the CDUSCC reverts to echoing RxD in any of the above cases, the last transmitted zero and seven ones will form an EOP for the next station down the loop. If the TxFIFO is empty when the EOP is recognized, the transmitter continues to send FLAGs until there is data in the FIFO. If a turnaround sequence or the reset GAP command is received before the FIFO is loaded, the transmitter switches to echoing RxD without any data transmission. Otherwise a frame transmission begins as above when a character is loaded into the FIFO. The mechanism provides time for the CPU to examine the received frame (the frame preceding the EOP) to determine if it should respond or not, while holding its option to initiate a transmission.

Termination of operation in the loop mode should be accomplished by use of the 'go off loop' command. When the command is invoked, the CDUSCC looks for the receipt of seven contiguous ones. It then negates the LCN output to cause the external loop control hardware to remove the CDUSCC from the loop without affecting operation of other units remaining on the loop.

RxBOP MODE

In BOP mode, the receiver may be in any one of four phases: hunt phase, address field (A) phase, control field (C) phase, or information field (I) phase. The character length for the A and C phases is always 8 bits. The I field character length is specified in RPR[1:0].

Note that if the residual character length is not zero, the unused most significant bits in the receiver FIFO are not necessarily zero. The unused bits should be ignored, this will not cause a CRC error.

After an enable receiver command is executed, the receiver enters hunt phase, in which a comparison for the FLAG string (01111110) is done every Rx bit time. The FLAG delineates the beginning (and end) of a received frame and establishes the character boundary. Each FLAG match in CCSR causes the FLAG detect status bit (RSR[2]) to be set. FLAGs with an overlapping zero will be detected. All FLAGs are deleted from the data stream.

Rx Address Field Phase

Once a FLAG has been detected, the receiver will exit hunt phase and enter address phase. The handling of the address field is determined by the values programmed in CMR1[2:0], which selects one of the BOP modes.

The length of the A field may be a single octet, a dual octet, or more octets, as described below. A primary station or an extended address secondary station does not perform an address comparison, and all characters in the A, C, and I fields after the flag are transferred to the FIFO. Although address field comparisons are not performed, the length of the address field is still determined by CMR1[4:3]. For the other secondary address modes, if there is a match, or the received character(s) match either of the other enabling conditions (group or all-parties address), all characters in the A, C, and I fields are transferred to the FIFO. If there is no match, the receiver returns to the FLAG hunt phase.

The BOP secondary address modes are selected by CMR1[4:3] and function as in the description that follows.

Rx Single-Octet Address

For receive, the address comparison for a secondary station is made on the first octet following the opening FLAG. A match occurs if the first octet after the FLAG matches the contents of S1R, or if all parties address (RPR[3]) is asserted and the first octet is equal to H'FF'.

Rx Dual-Octet Address

For receive, the address comparison for a secondary station is made on the first two octets following the opening FLAG. A match occurs if the first two octets after the FLAG match the contents of S1R and S2R respectively, or if all parties address (RPR[3]) is asserted and the first two octets are equal to H'FF, FF'.

Rx Dual Address with Group Mode

For receive, the address comparison for a secondary station is made on the first two octets following the opening FLAG. A match occurs for one of three possible conditions. If the first two octets after the FLAG match the contents of S1R and S2R, respectively, or if the first octet is H'FF' and the second matches the contents of S2R (group mode), or when all parties address (RPR[3]) is asserted and the first two octets are equal to H'FF, FF'. The second condition (group mode) allows a selected group of stations to receive a message.

Rx Extended Address Mode

Extends address field to the next octet if the LSB of the current address octet is zero. Address field is terminated if the LSB of the address is a one. The address field will be terminated after the first octet if the null address H'00' is received as the first address octet. For this mode the receiver does not perform an address comparison

(all received characters after the opening FLAG are transferred to the FIFO) but does determine when the address field is terminated.

Rx Control Field Phase
C phase begins after A phase is terminated. The receiver receives one or two control characters, CMR1[5]. After this phase is terminated, the character length is switched automatically from 8 bits to the number of bits specified in RPR[1:0] and the information field phase is entered.

Rx Information Field Phase
Data received in the I Field will be transferred to the RxFIFO 5 to 8 bits at a time, as specified by the character length (RPR[1:0]). Normally 8 bit character length is specified. If a shorter length is used, the received bits are right justified with the unused MSB(s) set to 0. If the I Field is not an integer multiple of the specified character length, a residual will remain. This is indicated by the RCL not zero status bit (RSR[0]) which is FIFOed with the last Rx character of the frame.

RCL not zero RSR[0] is set if the length of the last character of the I field does not have the length programmed in RPR[1:0]. The residual character length in TRSR[2:0] is also valid at that time, indicating the number of bits valid (right justified) of the last Rx character, required to complete the frame.

Rx Frame Termination
The frame is terminated when a closing FLAG is detected. The same FLAG can also serve as the opening FLAG of the next frame if RPR[6] = 0. For RPR[6] = 1, see description of RPR[6].

Rx CRC Accumulation
The 16 bits received prior to the closing FLAG form the frame check sequence (if an FCS is specified in CMR2[2:0]). All non-FLAG characters of the frame are accumulated in the CRC checker and the result is compared to the expected remainder. Failure to match will set CRC error flag. EOM detect RSR[7], RCL not zero RSR[0], and CRC error RSR[1] are normally FIFO'd with the last character of the I field. The CRC characters themselves are normally not passed to the RxFIFO. However, if the transfer FCS to FIFO control bit RPR[6] is asserted, the FCS bytes will be transferred to the FIFO. In this case the EOM, CRC error, and RCL not zero status bits will be tagged onto the last byte of the CRC sequence instead of to the last character of the message. Following the last data byte, the DFSB will be pushed into FIFO if it is specified (TRCR[6] = 1).

Rx Short Frame Detection
If the closing FLAG is received prior to receipt of the appropriate number of A field, C field as programmed in CMR1[5:3], and FCS field octets, a short frame will be detected and RSR[4] will be set. The I field need not be present in a valid frame.

Rx Abort Detection
An abort (a zero followed by seven ones) comparison is done after an opening FLAG has been received and up to receipt of the closing FLAG. A match causes the receiver to enter hunt (FLAG search) phase. The Abort detect status bit (RSR[6]) is set only if an Abort was received after receipt of the first address octet and before receipt of the closing FLAG. The abort is stripped from the received data stream.

Rx Idle Detection
If a zero followed by 15 contiguous ones is detected, the idle detect status bit RSR[3] is set. This comparison is done whenever the receiver is enabled. Therefore, it can occur before or after a received frame.

Rx Zero Detection
Zero deletion is performed during BOP receive. A zero after 5 contiguous ones is deleted from the data stream regardless of character boundaries. Deleted zeros are not subject to CRC accumulation. FLAG, ABORT, and IDLE comparisons are done prior to zero deletion.

BOP Loop Mode

Operation of the receiver in BOP loop mode is similar to operation in other BOP modes, except that only certain frame formats are supported. Several character detection functions that interact with the operation of the transmitter or transmitter commands are added:

1. When the 'go on-loop' command is invoked the receiver looks for the receipt of a zero followed by seven ones and then asserts the LCN output.

2. When the 'go off-loop' command is invoked, the receiver looks for the receipt of seven contiguous ones and then negates the LCN output.

3. The TxD output normally echoes the receive input with a two bit time delay. When the 'go active on poll' command is asserted, the receiver looks for an EOP (a zero followed by seven ones) and then switches the TxD output line to the normal transmitter output. Receipt of an EOP or an ABORT sets RSR[6].

4. Receipt of a turnaround sequence (eight contiguous zeros) or FLAG terminates the transmitter operation, if any, and returns the TxD output to echoing the RxD input, RSR[3] is set if a turn-around is received. See transmitter operation for additional details.

CHARACTER ORIENTED PROTOCOL

COP Operational Mode

To operate a channel of the CDUSCC in COP Mode, the Channel Mode Register 1 (CMR1) must specify COP via bits [2:0] = 100 through 110. In COP Mode the CMR1, CMR2, S1R,S2R, TPR and RPR take on the bit definitions illustrated in Figures 68 through 73, respectively (S1R and S2R should be loaded with the SYN character).

TxCOP Modes

Transmitter commands associated with all COP modes are: transmit SOM (TSOM, transmit start of message), transmit SOM with PAD (TSOMP), transmit EOM (TEOM, transmit end of message), reset TxCRC, exclude from CRC, and transmit DLE. The TSOM and TSOMP commands are identical to BOP modes except that s SYN character(s) is used as the start of message sequence instead of a FLAG (01111110).

Starting Transmission

A TSOM or TSOMP command must be issued to start COP transmission. TSOM (without PAD) causes the TxCRC/LRC generator to be initialized and one or two SYN characters from S1R/S2R to be loaded into the TxSR and shifted out on the TxD output.

A parity bit, if specified, is appended to each SYN character after the MSB. Send SOM acknowledge (TRSR[4]) is asserted when the SYN output begins. The user may re-invoke the command to cause multiple SYNs to be transmitted. If the command is not re-invoked

and the TxFIFO is empty, SYN patterns continue to be transmitted until the TxFIFO is loaded. If data is present in the FIFO, the first character is loaded into the TxSR and serialization of the data begins. Note that the TxFIFO may be pre-loaded with data before the TSOM is issued.

The TSOMP command causes all characters in the TxFIFO (PAD characters) to be loaded into the TxSR and serialized if the Tx is enabled. Unlike the transmit SOM without PAD command, data (non-PAD characters) cannot be pre-loaded into the TxFIFO. While the PAD is transmitted, parity is disabled and character length is automatically set to 8 bits regardless of the value in TPR[1:0]. When the TxFIFO becomes empty after the PAD, the TxCRC/LRC generator is initialized, the SYN character(s) are transmitted with optional parity appended, and send SOM acknowledge asserted. Operation then proceeds in the same manner as the TSOM command; the user has the option to invoke the TSOM command to cause multiple SYNs to be transmitted.

Figure 68. CMR1A (B) Channel Mode Register 1 [COP Mode]

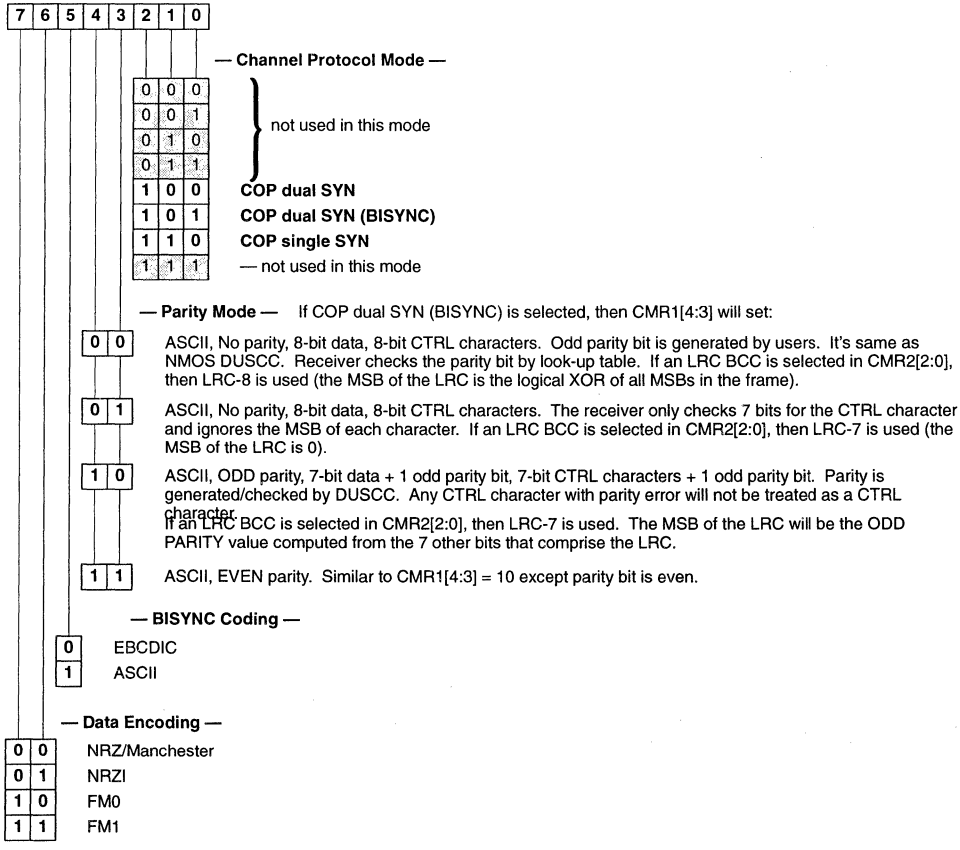

Figure 69. CMR2A (B) Channel Mode Register 2 [COP Mode]

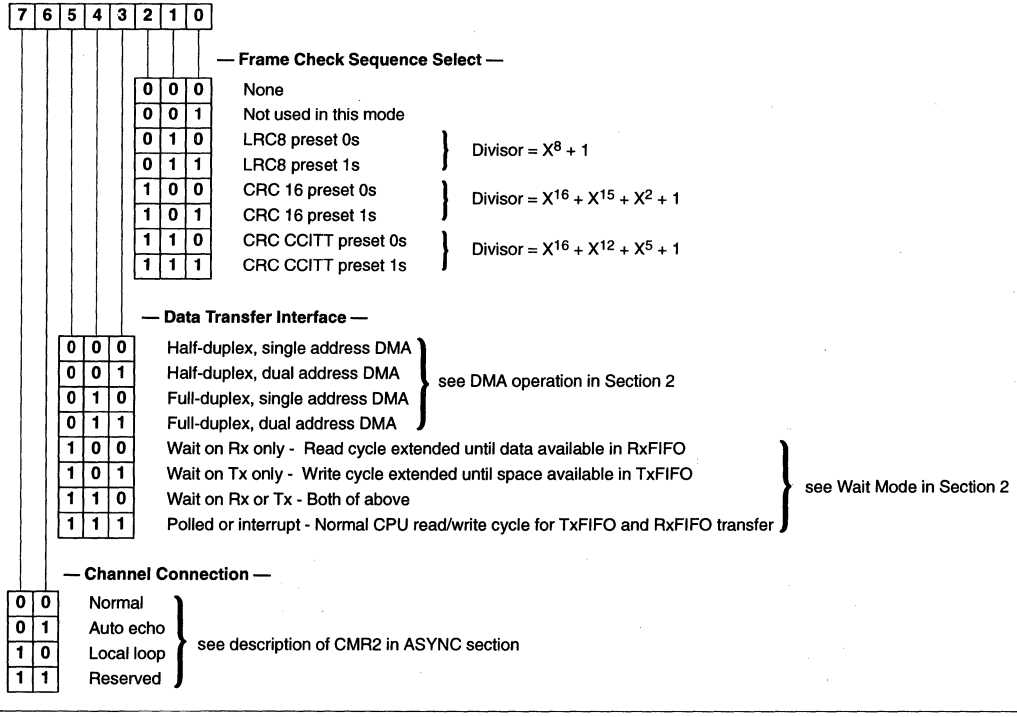

Figure 70. S1RA (B) SYN1/Secondary Address Register 1 [COP]

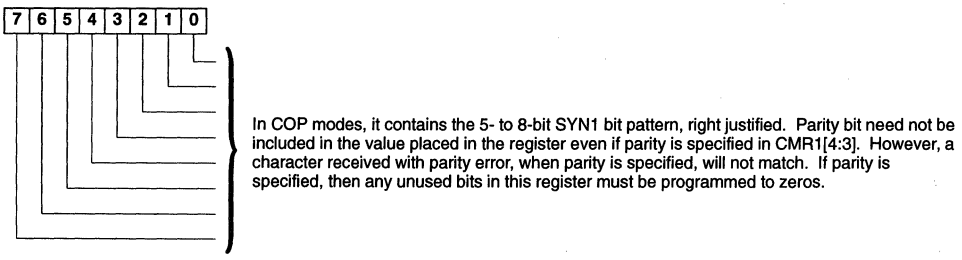

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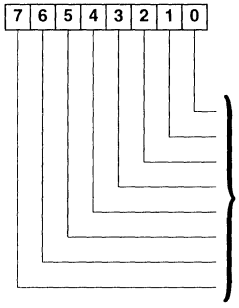
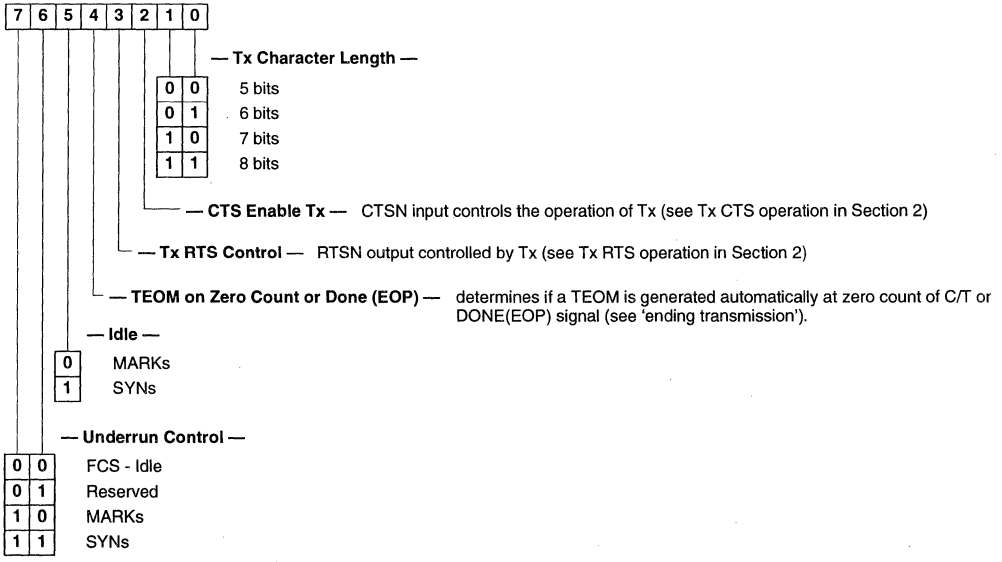
Figure 71. S2RA (B) SYN2/Secondary Address Register 2 [COP]



In COP dual SYN modes, it contains the 5- to 8-bit SYN2 bit pattern, right justified. Parity bit need not be included in the value placed in the register even if parity is specified in CMR1[4:3]. However, a character received with parity error, when parity is specified, will not match. If parity is specified, then any unused bits in this register must be programmed to zeros.

Figure 72. TPRA (B) Transmitter Parameter Register [COP Mode]



Data Transmission and Underrun

After the TSOM/TSOMP command is executed, characters in the TxFIFO are loaded into the TxSR and shifted out with a parity bit, if specified, appended after the MSB. If, after the opening SYN(s) and at least one data byte has been transmitted, the TxFIFO is empty, a data underrun condition results and the Tx Underrun Status Bit (TRSR[7]) is asserted. The transmitter's action on data underrun is determined by the Tx Underrun Control Bits (TPR[7:6]) and the COP protocol. If the Tx Underrun Control is set for 'MARKs' (TPR[7:6] = '10'), the transmitter line fills with MARK characters until a character is loaded into the FIFO. If the Tx Underrun Control is set for 'SYNs' (TPR[7:6] = '11'), the transmitter line fills with SYN, SYN1-SYN2, or DLE-SYN1 for mono sync, dual sync, and BISYNC transparent modes, respectively. If the Tx Underrun Control is set for 'FCS-IDLE (TPR[7:6] = '00'), the FCS (BCC) characters are transmitted and frame complete (TRSR[5]) and Underrun (TRSR[7] are set. TxD then assumes the programmed idle state (TPR[5]) of MARKs or SYN1/SYN1-SYN2.

For FCS-IDLE Underrun Control (TPR[7:6] = 00), transmitter operation resumes immediately (without transmitting a 'SYN') when data is loaded into the TxFIFO or resumes with the transmission of a SYN sequence when a TSOM command is invoked. A TSOMP

command is ignored, except after a CTS underrun, unless the transmitter is disabled or reset and then re-enabled.

For 'MARK' or 'SYN' Underrun Control (TPR[7:6] = 10 or 11), transmission resumes immediately (without transmitting a 'SYN') when data are loaded into the TxFIFO. Both a TSOM and a TSOMP command are not executed unless the transmitter is disabled or reset and then re-enabled or, after a CTS underrun, CTSN is asserted again.

Ending Transmission

User may end the transmission by issuing TEOM command (CCR) after loading last character in the TxFIFO. In DMA mode, assertion of DONE(EOPN) signal will append TEOM command to the last character if TPR[4]=1. If counter/timer is counting transmitted characters, TEOM is tagged with the character that causes counter to reach zero count. After EOM is transmitted, TxD signal will go 'IDLE'.

BISYNC

The TDLE command, when appended to a character in the TxFIFO, causes the DLE character to be loaded into the TxSR and serialized before the TxFIFO character is loaded into the TxSR and serialized. This feature is particularly useful for BISYNC operation. The DLE character will be excluded from the CRC accumulation in BISYNC transparent mode (see below), but will be included in all other COP modes.

In BISYNC mode, transmission of a DLE-STX character sequence (either via a send TDLE command appended to the STX character, or via DLE and STX loaded into the TxFIFO) puts the transmitter into the transparent mode of operation and sets TRSR[0]. In this mode, normally restricted character sequences can be transmitted as 'normal' bit sequences. The switch occurs after transmission of the two characters, so that the DLE and STX are included in the FCS (BCC) accumulation. If the DLE-STX is to be excluded from the CRC, the user should issue a 'reset CRC' command prior to loading the next character.

Another method of excluding the two characters from the CRC is to invoke the 'exclude from CRC' command prior to loading the character(s) into the FIFO. While in transparent mode, the transmitter line fills with DLE-SYN1 and automatically transmits an extra DLE if it finds a DLE in the TxFIFO ('DLE stuffing'). The transmitter reverts to non-transparent mode when the frame complete status is set in TRSR[5].

Frame Check Sequence

CRC/LRC accumulation can be specified in all COP modes; the type is specified via CMR2[2:0]. The TSOM/TSOMP commands set the CRC/LRC accumulator to its initial state and accumulation begins with the first non-SYN character after the initial SYN(s) are transmitted. PAD characters are not subject to CRC accumulation. In non-BISYNC or BISYNC normal modes, all transmitted characters except linefill characters (SYNs or MARKs) are subject to accumulation. In BISYNC transparent mode, odd (stuffed) DLEs and the DLE- SYN1 linefill are excluded from the accumulation. Characters can be selectively excluded from the accumulation by invoking the 'exclude from CRC' command prior to loading the character into the FIFO.

Accumulation stops when transmission of the first character of the FCS (BCC) begins. The CPU can set the accumulator to its initial state prior to the transmission of any character by using the appended reset CRC command. The CRC generator is also automatically initialized after the EOM is sent.

RxCOP Modes

When the receiver is enabled in COP modes, it first goes into the SYN hunt phase, testing the received data each bit time for receipt of the appropriate SYN pattern, plus parity if specified, to establish character boundaries. Receipt of the SYN bit pattern terminates hunt phase and places the receiver in the data phase, in which all leading SYNs are stripped and the RxFIFO begins to load starting with the first non-SYN character. In COP single SYN protocol mode, S1R contains the SYN character required to establish character synchronization. In COP dual SYN and BISYNC protocol modes, S1R and S2R contain the first and second SYN characters, respectively, required to establish character synchronization. The SYN character length is the same as the character length programmed in RPR[1:0], plus the parity bit if parity is specified. SYN characters received with a parity error, when parity is specified, are considered invalid and will not cause synchronization to be achieved.

In COP mode, resetting the receiver clears the receiver data path, while disabling the receiver does not. If not reset, partial sync patterns remaining in the receiver will be recognized when it is enabled.

If external synchronization is programmed (RPR[4] = 1), the internal SYN detection and special character recognition logic are disabled and receipt of SYN characters is not required. A pulse on the SYNIN input pin will establish character synchronization and terminate hunt phase. The SYNIN pin is ignored after the first input on the SYNIN pin is received. The receiver must be disabled and then re-enabled to re-synchronize or to return to normal mode. This must be programmed in conjunction with CMR1[2:0] = 110. Refer to the description of RPR[4] for further details (Figure 73).

The SYN detect status bit, RSR[2], is set whenever SYN1, SYN1-SYN2, or DLE-SYN1 is detected for single SYN, dual SYN/BISYNC normal, and BISYNC transparent modes, respectively. SYNC detect bit (RSR[2]) is set when SYN1 and/or SYN2 are detected by internal logic irrespective of the normal or transparent BiSYNC operation. After character sync has been attained, the receiver enters the data phase and assembles characters in the RxSR, beginning with the first non-SYN character, with the least significant bit received first. It computes the FCS (BCC) if specified, checks parity if specified and checks for overrun errors.

The operation of the FCS (BCC) logic depends on the particular COP mode in use. The FCS (BCC) is initialized upon first entering the data phase. For non-BISYNC modes, all received characters after entering data phase are included in the FCS (BCC) computation, except for leading SYNs and SYNs which are specified to be stripped by RPR[7]. As each received character is transferred from the RxSR to the FIFO, the current value of the FCS (BCC) characters is checked and the CRC ERROR status bit (RSR[1]) is set if the value of the CRC remainder is not the expected value. RSR[1] gets set when the character reaches the top of the FIFO. The EOM status bit, RSR[7], is not set since there is no defined end-of-message character. Therefore, user has to know when to check BCC to get exactly BCC status. The receiver computes the FCS (BCC) for text messages automatically when operating in BISYNC protocol mode.

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Figure 73. RPRA (B) Receiver Parameter Register [COP Mode]

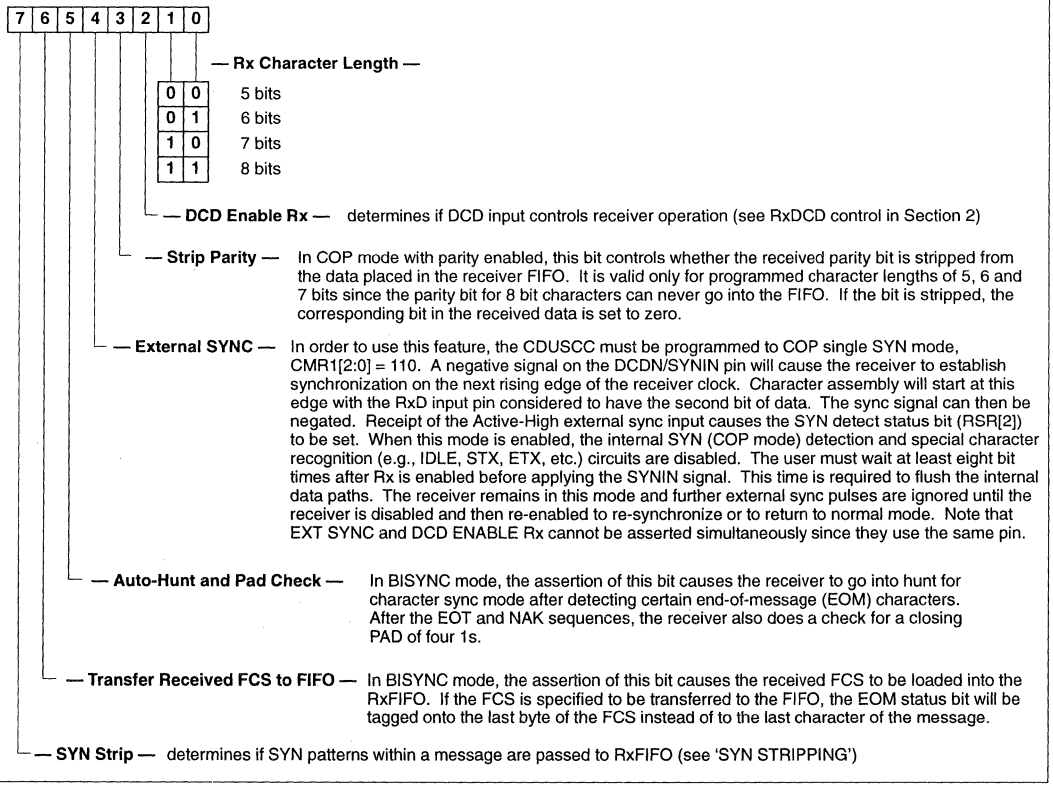
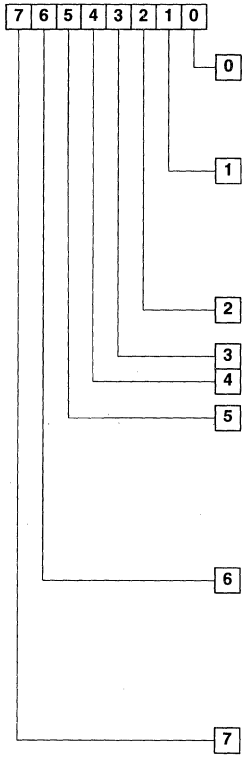


Figure 74. RSRA (B) Receiver Status Register [COP Mode]



0 Parity error*# – The parity bit of the received character was not as expected. A parity error does not affect the parity bit put into the FIFO as part of the character when strip parity (RPR[3]) is negated. A SYN or other character received with parity error is treated as a data character. Thus, a SYN with parity error received while in SYN search state will not establish character sync. Characters received with parity error while in the SYN search state will not set the error bit.

1 CRC error*# – In BISYNC COP mode, this bit is set upon receipt of the BCC byte(s), if any, to indicate that the received BCC was in error. The bit is normally FIFOed with the last byte of the frame (the character preceding the first BCC byte). However, if transfer FCS to FIFO (RPR[6]) is asserted, this bit is FIFOed with the last BCC byte. The value of this bit should be ignored for non-text messages or if the received frame was aborted via an ENQ. In non-BISYNC COP modes, the bit is set with each received character if the current value of the CRC checker is not equal to the non-error value (see CMR2[2:0]).

2 SYN detect– A SYN pattern was received. Refer to Detailed Operation for definition of SYN patterns. Set one bit time after detection of SYN pattern in HSRH, HSRL.

3 Not used, set to 0

4 Not used, set to 0

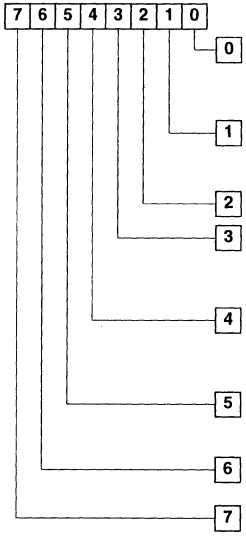
5 Overrun error* – A new character was received while the receive FIFO was full and a charcter was already waiting in the receive shift register to be transferred to the FIFO. The DUSCC protects the five characters previously asssembled (four in RxFIFO, one in Rx shift register) and discards the overrunning character(s). After the CPU read the FIFO, the character waiting in the RxSR will be loaded into the available FIFO position. This releases the RxSR and a new character assembly will start at the next character boundary. In this way, only valid characters will be asssembled, i.e., no partial character assembly will occur regardless of when the RxSR became available during the incoming data stream.

6 PAD error (BISYNC only)* – PAD error detected (see RPR[5]). An ABORT sequence consisting of a zero followed by seven ones was received after receipt of the first address octet but before receipt of the closing FLAG. The user should read RxFIFO until it is empty and determine if any valid characters from a previous frame are in the FIFO. If no character with a tagged EOM detect ([7]) is found, all characters are from the current frame and should be discarded along with any previously read by the CPU. An ABORT detect causes the receiver to automatically go into search for FLAG state. An abort during a valid frame does not cause the CRC to reset; this will occur when the next frame begins.

7 Rx character zero count detect (EOM detect – BISYNC only)*# –The character at the top of the FIFO was either a text message terminator or a control sequence received outside of a text or header field. See Detailed Operation of COP Receiver. If transfer FCS to FIFO (RPR[6]) is set, the EOM will instead be tagged onto the last byte of the FCS. Note that if an overrun occurs during receipt of a message, the EOM character may be lost, but this status bit will still be asserted to indicate that an EOM was received. For two-byte EOM comnparisons, only the second byte is tagged (assuming the CRC is not transferred to the FIFO).

*FIFOed with data in extended mode (CDUSCC)
#FIFOed with data in default mode (NDUSCC)

Figure 75. TRSRA (B) Transmitter and Receiver Status Register [COP Mode]



0 – Rx Transparent mode – Indicates that a DLE-STX sequence was received and the receiver is operating in BISYNC transparent mode. Set two bit times after detection of STX in HSRL. Transparent mode operation is terminated and the bit is negated automatically when one of the terminators for transparent text mode is received (DLE-ETX/ETB/ITB/ENQ).

1 – Rx Hunt mode – This bit is asserted after the receiver is reset or disabled. It indicates that the receiver is in the hunt mode, searching the data stream for a SYN sequence to establish character synchronization. The bit is negated automatically when character sync is achieved.

2 – Not used

3 – DPLL error – Set while the DPLL is operating in FM mode to indicate that a data transition was not detected within the detection window for two consecutive bits and that the DPLL was forced into search mode. This feature is disabled when the DPLL is specified as the clock source for the transmitter via TTR[6:4].

4 – Send SOM ACK – Set when the transmitter begins transmission of a SYN pattern in response to the TSOM or TSOMP command. If the command is reinvoked, the bit will be set again at the beginning of the next transmitted SYN pattern. The user can control the number of SYNs which are sent through this mechanism.

5 – Frame complete – Asserted at the beginning of transmission of the end of message sequence invoked by which is either a TEOM command, or when TPR[4]=1, or TPR[7:6]=00. The CPU can invoke the TSOM command after this bit is set to control the number of SYNs between transmitted frames.

6 – CTS underrun – This bit is set only if CTS enable Tx (TPR[2]) is asserted. It indicates that the transmit shift register was ready to begin serializing a character and found the CTSN input negated.

7 – Transmitter underrun – Indicates that the transmit shift register has completed serializing a character and found no other character to serialize in the TxFIFO. The bit is not set unitl at least one character from the transmit FIFO (not including PAD characters in synchronous modes) has been serialized. The transmitter action after transmitter empty depends on function.

Figure 76. IER1A (B) Interrupt Enable Register 1 [COP Mode]

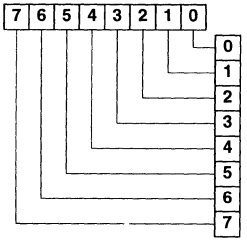
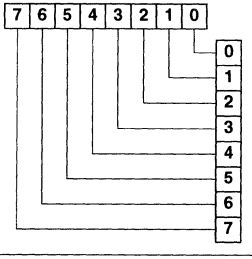


Figure 77. IER2A (B) Interrupt Enable Register 2 [COP Mode]



SYN Pattern Stripping

Leading SYNs (before a message) are always stripped and excluded from the FCS, but SYN patterns within a message are treated by the receiver according to the RPR[7] bit. SYN character patterns are defined for the various COP modes as follows:

COP single SYN mode - SYN1

COP dual SYN mode - SYN1, and SYN2 when immediately preceded by SYN1.

BISYNC normal mode - SYN1 and SYN2 when immediately preceded by SYN1, SYN1 is always stripped, even if it is not followed by SYN2 when stripping is selected.

BISYNC transparent mode - DLE - SYN1, where the DLE is the last of an odd number of consecutive DLEs.

RPR[7]

0 Strip only leading SYNs and do not accumulate in FCS.

1 Strip all SYNs. Additionally, strip odd DLEs when operating in BISYNC transparent mode. Do not accumulate stripped characters in FCS.

NOTE: In BISYNC transparent mode, odd DLEs are never included in FCS. RPR[7] chooses whether they go to the RxFIFO or not.

Processing of the SYN patterns is determined by the RPR[7] bit, the COP mode, and the position of the pattern in the frame. This is summarized in Table 16.

The value of the RPR[7] field does not affect the setting of the SYN DETECT status bit, RSR[2], and the generation of a SYNOUT pulse when a SYN pattern is received.

BISYNC FEATURES

The CDUSCC provides support for both BISYNC normal and transparent operations. The following summarizes the features provided. Both EBCDIC and ASCII text messages can be handled by the CDUSCC as selected by CMR1[5]. The receiver has the capability of recognizing special characters for the BISYNC protocol mode (see Table 17). All sequences in Table 17, except SOH and STX, when detected explicitly cause a status to be affected.

The first character received when entering data phase for a header or text message should be an SOH, an STX, or a DLE-STX two-character sequence. Receipt of any of these initializes the CRC generator and starts the CRC accumulation. The SOH places the receiver in header mode, receipt of the STX places it in text mode, and receipt of the DLE-STX sequence (at any time) automatically places the receiver in transparent mode and sets the XPNT mode status bit, TRSR[0]. There is no explicit status associated with SOH and STX. If any other characters are received when entering the data phase, the message is treated as a control message and will not be accumulated in CRC.

After the data phase is established, the receiver searches the data stream for an end of message control character(s):

Header field: ENQ, ETB, or ITB

Normal text field: ENQ, ETX, ETB, or ITB

Transparent text field: DLE-ENQ, DLE-ETX, DLE-ETB, or DLE-ITB

Control message field: EOT, NAK, ACK0, ACK1, WACK, RVI or TTD

Detection of any one of these sequences causes the EOM status bit, RSR[7], to be set. Also if RPR[5] is set and the receiver does not detect a closing PAD (four 1's) after the 'EOT' or 'NAK', the PAD error status bit, RSR[6], is set. When the abort sequence ENQ or DLE-ENQ is detected, the character is tagged with an EOM status and transferred to the FIFO, but the appended CRC error status bit should be ignored. For the other EOM control sequences, the receiver waits for the next two bytes (the CRC bytes) to be received, checks the value of the CRC generator, and tags the transferred character with a CRC error, RSR[1], if the CRC remainder is not correct. See Figure 78 for an example of FCS (BCC) accumulation in various BISYNC messages.

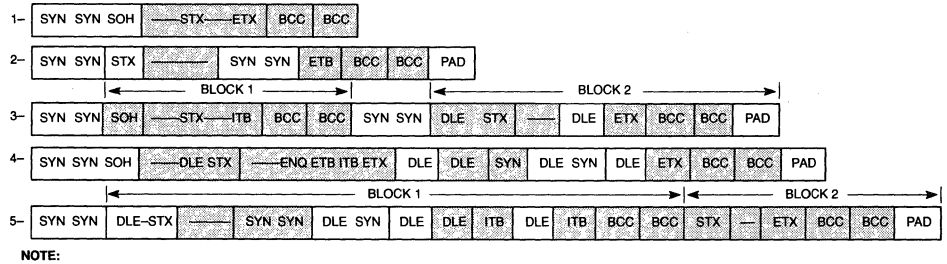
The CRC bytes are normally not transferred to the FIFO, unless the transfer FCS to FIFO control bit, RPR[6], is asserted. In this case the EOM and CRC error status bits will be tagged onto the last byte of the last FCS byte instead of to the last character of the message. After detecting one of the end-of-message (EOM) character sequences and setting RSR[7], the receiver automatically goes into auto hunt mode for the SYNC characters and PAD check if RPR[5] is set.

Table 16. SYN Pattern Processing

Mode	RPR[7]	Leading SYNs	Within a Message
BISYNC	0	no FCS	no FCS
		no FIFO	Pattern into FIFO
	1	no FCS	no FCS
		no FIFO	no FIFO
COP	0	no FCS	Accumulate in FCS
		no FIFO	Pattern into FIFO
	1	no FCS	no FCS
		no FIFO	no FIFO

Table 17. BISYNC Features

Sequence	ASCII	EBCDIC	Description
BISYNC — Single Character Sequence			
SOH	01H	01H	Start of header
STX	02H	02H	Start of text
ETX	83H	03H	End of text
EOT	04H	37H	End of transmission
ENQ	85H	2DH	Enquiry
DLE	10H	10H	Data link escape
NAK	15H	3DH	Negative ack
ETB	97H	26H	End of transmission block
ITB	1FH	1FH	End of intermediate transmission block
BISYNC — Two Character Sequence			
ACK0	H'10,B0'	10,70H	Acknowledge 0
ACK1	H'10,31'	10,61H	Acknowledge 1
WACK	H'10,3B'	10,6BH	Wait before transmit positive ack
RVI	H'10,BC'	10,7CH	Reverse interrupt
TTD	H'02,85'	02,2DH	Temporary text delay
BISYNC — (Transparent Text Mode) — Two Character Sequences			
DLE-ENQ	H'10,85'	10,2DH	Enquiry
DLE-ITB	H'10,1F'	10,1FH	End of intermediate transmission block
DLE-ETB	H'10,97'	10,26H	End of transmission block
DLE-ETX	H'10,83'	10,03H	End of text
DLE-STX	H'10,02'	10,02H	Start of transparent mode



NOTE:

1. The BCC accumulator is stopped after the end of message character sequence. All shaded areas are accumulated.
2. ENQ (DLE-ENQ) in a text message should be treated as an abort.
3. Opening SYNs will be stripped by the receiver.

Figure 78. BISYNC BCC Accumulation Examples

Table 18. Summary of COP Features

COP Dual SYN Mode	
SYN detect	SYN1–SYN2
Linefill	SYN1–SYN2
SYN stripping	SYN1–SYN2 used to establish character sync, i.e., leading SYNs. Subsequent to this (after receiving first non-SYN character), SYN1 and SYN1–SYN2 if stripping is specified by RPR[7].
Excluded from FCS[1]	SYN1 and SYN1–SYN2 before beginning of message, i.e., leading SYNs and, if SYN stripping is specified by RPR[7] anywhere else in the message for the Rx; linefill SYN1–SYN2 for Tx regardless of RPR[7]. (If SYN stripping is not specified, then SYNs within a message will be included in FCS by Rx.)
BISYNC Normal Mode	
SYN detect	SYN1–SYN2
Linefill	SYN1–SYN2
SYN stripping	SYN1–SYN2 used to establish character synchronization, i.e., leading SYNs. Subsequent to this (after receiving first non-SYN character), SYN1 and SYN1–SYN2 if stripping is specified by RPR[7].
Excluded from FCS	All SYNs either before or within a message, regardless of RPR[7], plus additional characters as required by the protocol, e.g., the first character of header or text is SOH, STX or DLE+STX.
BISYNC Transparent Mode	
SYN detect	DLE–SYN1[1]
Linefill	DLE–SYN1
SYN stripping	DLE–SYN1 and odd DLEs if stripping is specified by RPR[7]
Excluded from FCS	DLE–SYN1 and odd DLEs, regardless of RPR[7]
COP Single SYN Mode	
SYN detect	SYN1
Linefill	SYN1
SYN stripping	SYN1 used to establish character synchronization, i.e., leading SYNs. Subsequent to this (after receiving first non-SYN character), SYN1 is stripping if specified by RPR[7].
Excluded from FCS[2]	SYN1 before beginning of message, i.e., leading SYNs and, if SYN stripping is specified by RPR[7] anywhere else in the message for the Rx; linefill SYN1 for Tx regardless of RPR[7]. (If SYN stripping is not specified, then SYNs within a message will be included in FCS by Rx.)

NOTES:

1. In non-BISYNC COP modes (single or dual SYN case), if SYN stripping is off, i.e., RPR[7] = 0, then SYNs within a message will be included in FCS by receiver. Therefore, the remote transmitter should be careful not to let the TxFIFO underrun since the linefill SYN characters are not accumulated in FCS by the Transmitter regardless of RPR[7]. Letting the TxFIFO underrun will result in a CRC error in the receiver.
2. DLE indicates last DLE of an odd number of consecutive DLEs.

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APPENDIX 1

Data Communications

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FUNDAMENTAL CDUSCC FUNCTIONS

The design of the CDUSCC has been directed at providing a device which relieves the system processor from the numerous and varied tasks associated with synchronous protocols. These tasks include clock recovery (digital phase-locked loop) from data stream; generation, detection and deletion of various control characters; error detection; modem control; baud rate generation; character counting and miscellaneous time interval generation. The CDUSCC also provides asynchronous communication.

ASYNCHRONOUS vs SYNCHRONOUS TRANSMISSION

Asynchronous data is typically produced by low-speed terminals with bit rates ≤ 9600bps. In asynchronous systems (Figure 79a), the transmission line is in a mark (binary 1) condition in its idle state. As each character is transmitted, it is preceded by a start bit, or transition from mark to space (binary 0), which indicates to the receiving terminal that a character is being transmitted. The receiving device detects the start bit and the data bits that make up the character. At the end of the character transmission, the line is returned to a mark condition by one or more stop bit(s), and is ready for the beginning of the next character. An asynchronous character varies in length depending on the information code employed: five bits for Baudot code, seven for ASCII (plus an optional parity bit) and eight for EBCDIC. This process is repeated character-by-character until the entire message has been sent. The start and stop bits permit the receiving terminal to synchronize itself to the transmitter on a character-by-character basis.

Synchronous transmission (Figure 79b) makes use of an internal clocking source within the modem to synchronize the transmitter and receiver. Once a synchronization character (SYN or FLAG) has been sensed by the receiving terminal, data transmission proceeds character-by-character without intervening start and stop bits. The incoming stream of data bits is interpreted on the basis of the receive clock supplied by the modem. This

clock is usually derived from the received data through a phase locked loop. The receiving device accepts data from the modem until it detects a special ending character or a character terminal count at which time it knows that the message is over.

The message block is usually composed of one or two synchronization characters, a number of data and control characters (typically 100 to 10,000), a terminating character, and one or two error control characters. Between messages, the communication line may idle in SYN or FLAG characters or be held to mark.

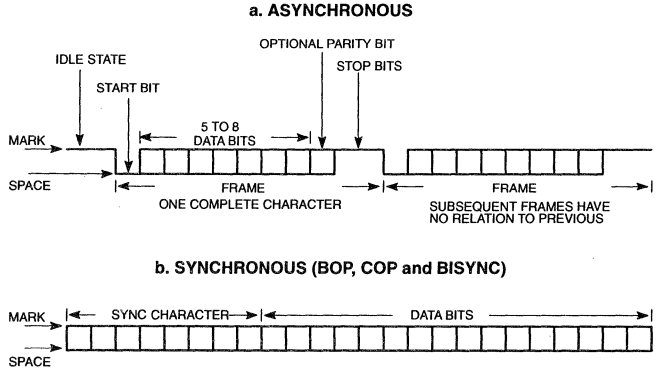
Note that synchronous modems can be used to transmit asynchronous data and conversely, asynchronous modems can be used for synchronous data if the receiving terminal can derive the clock from the data.

Asynchronous transmission is advantageous when transmission is irregular (such as that initiated by a keyboard operator's typing speed). It is also inexpensive due to the simple interface logic and circuitry required. Synchronous transmission, on the other hand, makes far better use of the transmission facility by eliminating the start and stop bits on each character. Furthermore, synchronous data is suitable for multi-level modulation which combines two or four bits in one signal element (baud). This can facilitate data rate of 4.8Kb/s or 9.6Kb/s over a bandwidth of 2.4KHz. Synchronous modems offer higher transmission speeds, but are more expensive because they require precisely synchronized clock and data.

Synchronous communication offers more efficient use of a channel capacity. For example, in async mode, efficiency could be as low as 5/9 and not higher than 8/9.5. Here the imposition of start, stop and parity reduces channel efficiency. In synchronous protocols, the inefficiency is caused by the SYN characters, address, FCS and closing sequence. The data in between may be as long as one wishes.

CHARACTERISTICS OF DATA LINK CONTROLS

Data Link Control (DLC) can be classified into Character Oriented Protocols (COP) and Bit Oriented Protocols (BOP). In COP a defined set of communication control characters effects the orderly operation of the data link. These control characters are part of an information code set, such as ASCII or EBCDIC. The code set also



Choice of the proper timing mode depends on the application. Asynchronous transmission (a) is used mostly with man-machine interfaces while synchronous transmission (b) offers the high speed necessary for machine-machine communication.

Figure 79. Serial Data Stream Formats

consists of graphic characters (alphanumeric, $, ., etc.). COP messages are transmitted in blocks which are composed of a header or control field, a body or text field and trailer or error checking field. Specific end/begin characters are used as field or block delimiters for IBMs Binary Synchronous Communications (BISYNC) protocol. Examples are SOH (Start of Header), STX (Start of Text), ETX (End of text), ITB (Intermediate Transmission Block), and EOT (End of Transmission). In the Digital Data Communications Message Protocol (DDCMP) developed by Digital Equipment Corporation, character count is used to determine the length of the text field while a SOH character delimits the header field.

BOPs make use of only two or three specific control characters for operation of the data link. These characters are used to delimit the beginning (FLAG) and end (FLAG, ABORT) of a message frame, Upon receipt of the opening FLAG, positional significance is used to delineate the bit sequence that follows into prescribed fields. These fields are address, control, information, and frame check sequence. The address, control and frame check fields are of fixed length; the information field length is variable and may be zero. Examples of BOPs are IBM's Synchronous Data Link Control (SDLC), ANSI's Advanced Data Communication Control Procedures (ADCCP), ISO's High-Level Data Link Control (HDLC), Burrough's Data Link Control (BDLC), and various other protocols developed by computer mainframe manufacturers. All of the above-mentioned protocols are similar and can be treated as subsets of ADCCP.

Automatic Request for Repeat (ARQ)

The two types of ARQs are stop-and-wait and continuous ARQ. Each provides defined methods for acknowledging correct (error free) reception of transmitted blocks of information.

When a connection is established in the stop-and-wait ARQ, the transmitter sends one block and then stops. Eventually, the receiver acquires that block, subjects the block to an error check, and then sends an ACK control character to the transmitter to indicate that the block is correct or a NAK control character to indicate an error. If an ACK is returned, the transmitter sends the next block in sequence. If a NAK is returned, that block is re-transmitted. Thus, the stop-and-wait mode involves periods of idleness, including propagation delays between each block, so that the line is not communicating nearly at its rated capacity. A line efficiency of 25% to 50% is not uncommon, depending on the error rate on the line. IBM's BISYNC protocol is the most popular implementation of stop-and-wait type of ARQ.

In continuous ARQ, the transmitter keeps sending one block after another without stopping. The receiver and transmitter retain individual counts of the blocks outstanding and provide buffer storage to retain those blocks. Only when an erroneous block is detected does the receiver tell the transmitter to re-send that block and all subsequent in-transit, but unacknowledged blocks. Some DLCs permit up to 127 blocks to be unacknowledged at any one time. IBM's SDLC, Burrough's Data Link Control (BDLC), and Digital Equipment Corporation's DDCMP employ continuous ARQ. Under ideal conditions, the link can exceed 90% efficiency with this type of ARQ.

COP Messages

As stated earlier, COP messages are transmitted in units called blocks. The components of a transmission block are shown in Figure 78. The Header field contains auxiliary information that identifies the address of the message destination or source, the job number (if any), the type of message (data or control), the control action, and a positive or negative acknowledgment to insure error-free reception of a previous message(s).

Control actions are used to reset or initialize a secondary station, to acknowledge good or bad reception of blocks, to inquire why a response or acknowledgment has not occurred within a specific time period, or to abort a transfer sequence. Examples of typical control function inquiries or responses are given below:

This is Station A transmitting

I have a message for Station B

Are you ready to receive?

I received your last message.

I'm finished; now it's your turn to transmit.

Do you have anything to send me?

I can't listen now, so don't send me anything.

I don't hear you, so I'm hanging up.

The control information is conveyed via special characters or character sequences.

The **Text** field contains the data, if any, being transmitted. This variable length field is absent in control messages. The Text may be characters of the information code set or may be transparent to that code set. In the latter case, pure data (binary, packed decimal, floating point), specialized codes, or machine language computer programs must be distinguished from characters in the code set being used. This is accomplished through the use of a transparent mode whose implementation depends on the specific DLC.

To assure correct reception of information over communication facilities, a sequence of check bits, often called Block Check Character(s) or BCC, are generated and transmitted as the **Error Check** field. Each block of data transmitted is error-checked at the receiving station in one of several ways, depending on the code and functions employed. These checking methods include:

1. Vertical Redundancy Check (VRC a parity check on each character) in conjunction with a Longitudinal Redundancy Check (LRC a horizontal parity, i.e., exclusive OR, on the characters) that is sent as the Error Check field. Note that certain control characters and transparent mode information is not subject to LRC.

2. Cyclic Redundancy Check (CRC) which involves a polynomial division of the bit stream by a CRC polynomial. The dividend polynomial is initially preset to 0 and the 1s and 0s of the data stream become the coefficients of the dividend polynomial. The division uses subtraction modulo 2 (no carries) and the remainder is transmitted as the Error Check field. The receiving station compares the transmitted remainder with its own computed remainder and an equal condition indicates that no error has occurred. The polynomial value depends on the protocol and code set being used.

BOP Messages

Bit Oriented Protocols (BOPs) are more straightforward and universal than the COPs just discussed. BOP messages are transmitted in frames and all messages adhere to one standard from format shown in Figure 79.

Common characteristics of BOPs are:

- Independence of codes, line configurations, and peripherals.
- Positional significance is used instead of control characters or character counts
- There is one standard frame format for messages
- Continuous ARQ operation allows up to 7 outstanding frames (127 when a seven-bit frame count is maintained)
- Half or full-duplex operation is possible
- Information transparency is achieved through zero insertion and deletion
- Error checking is on a complete frame

As shown in Figure 79, a frame starts with the 8-bit FLAG sequence, 01111110, followed in position by an ADDRESS sequence, a CONTROL sequence, an INFORMATION sequence (if present), a FRAME CHECK SEQUENCE, and ending with another FLAG sequence. Each station attached to the data link continuously searches for the FLAG sequence and an ADDRESS sequence. In multi-point operation, for example, a secondary station must detect a FLAG immediately followed by its own ADDRESS to enable the receiver.

When the primary station transmits, the station ADDRESS sequence it designates which secondary station is to receive the balance of the transmitted frame. When a secondary station transmits, the ADDRESS tells the primary station which secondary station originated the frame. A secondary station must recognize its valid address before it can accept a frame and take any action on the contents of that frame. Also, the primary station will accept a frame only when it contains the address of a secondary station that has been given permission to transmit. To ensure the integrity of the data being transmitted, the ADDRESS sequence appears within each frame. This enhances flexibility in that the primary station can interleave receptions from several secondary stations without intermixing individual station information transfer. Using straight binary coding, an 8-bit ADDRESS sequence can differentiate between 256 terminals or stations.

Some BOPs (ADCCP and HDLC) permit the use of an extended ADDRESS field to address more than 256 terminals. To do this, the least-significant bit of an ADDRESS byte is set to zero if another ADDRESS byte is to follow; a one is used to indicate that the current address byte is the last one. Since only 7 bits are used for the actual station address, each ADDRESS byte can differentiate between (up to) 128 terminals. There is no limit to the number of ADDRESS bytes in an extended ADDRESS field.

An "all parties" or "global address" of eight 1s can be interpreted as a legitimate secondary station address (in addition to the specified secondary station address) which will activate the receiver. This pattern must follow the opening FLAG.

The CONTROL field follows the ADDRESS sequence. It is the heart of the BOP message for it determines the type of message, the send-and-receive frame sequence counts (for continuous ARQ), a poll command from the primary station or final response from the secondary station. The primary station uses CONTROL to tell (command) the addressed secondary station what operation to perform. The secondary station uses CONTROL to react (respond) to the primary station.

The CONTROL field takes on any one of three formats depending on whether the field is to indicate:

- Information transfer
- Supervisory commands/responses
- Non-sequenced commands/responses

Actual implementation of these three message types is beyond the scope of this handbook. Refer to the appropriate BOP DLC specification listed in Chapter 7.

A one byte CONTROL field uses three bits for transmit and three bits for receive sequence counts. This means up to seven frames can be unacknowledged at any one time. To increase the number of outstanding frames, a second byte is used to provide four additional bits for transmit and four for receive sequence counts. This extended CONTROL field enables up to 127 frames to be outstanding. Note that buffer storage is required to contain all of the outstanding frames, for they may have to be re-transmitted if they are received in error.

The INFORMATION field may vary in length, including different lengths in sequential frames making up a complete transmission. The data may be configured in any code structure, including straight binary, binary coded decimal, packed decimal, EBCDIC, ASCII, and Baudot. The INFORMATION field may be used to convey any kind of code. However, the content of the field must be self-defining by actual or implied means. For example, peripheral device control characters, such as CARRIAGE RETURN, will actually be part of the INFORMATION field, while the code being used, whether it be ASCII or EBCDIC, may be implied in the address of a specific terminal designed for a specific code. Furthermore, whether a frame contains an INFORMATION field at all depends on the particular CONTROL format transmitted.

Because there is no restriction on the bit patterns that may appear between the end of the start FLAG and the beginning of the end FLAG, the transmitted data stream may contain six or more contiguous ones and this pattern could be interpreted as a FLAG, and inadvertently terminate an incomplete frame. To circumvent this, once the start FLAG has been completed the transmitting station starts counting the number of contiguous 1s; when five 1s occur, the transmitter automatically inserts a 0 following the fifth 1. The receiver, too, counts the number of contiguous 1s. When the number is five, it inspects the sixth bit; if the sixth bit is 0, the receiving station drops the 0, resets its counter and continues receiving. But if the sixth bit is a 1, the receiving station continues to receive and act on the pending FLAG.

The FRAME CHECK SEQUENCE (FCS) is included in all BOP frames to detect errors which may occur during transmission. This field is 16 bits long and immediately precedes the end-of-frame FLAG. The contents of the FCS field, based on a cyclic redundancy check, is an inverted remainder derived from a division of the transmitted data by a generator polynomial. The dividend is initially preset to 1s, and the data stream that follows becomes the dividend. The generator polynomial for CRC-CCITT is:

$$G(x) = X^{16} + X^{12} + X^5 + 1$$

All data transmitted between the start FLAG and the end FLAG is included in the checking accumulation, except those 0 bits inserted to prevent unwanted FLAGS. Because the received CRC is subject to CRC accumulation, the result of a transmission correctly received is the hexadecimal constant F0B8.

A comparison of common DLCs is given in Table 19.

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Table 19. Protocol Characteristics

FEATURE	DDCMP	BISYNC	SDLC	ADCCP	HDLC
Full Duplex	Yes	No	Yes	Yes	Yes
Half Duplex	Yes	Yes	Yes	Yes	Yes
Serial	Yes	Yes	Yes	Yes	Yes
Parallel	Yes	No	No	No	No
Data Transparency	Count	Character Stuffing	Bit Stuffing	Bit Stuffing	Bit Stuffing
Asynchronous Operation	Yes	No	No	No	No
Synchronous Operation	Yes	Yes	Yes	Yes	Yes
Point-to-Point	Yes	Yes	Yes	Yes	Yes
Multi-point	Yes	Yes	Yes	Yes	Yes
Error Detection (CRC)	CRC-16	CRC-16	CRC-CCITT	CRC-CCITT	CRC-CCITT
Re-Transmit Error Recovery	Yes	Yes	Yes	Yes	Yes
Bootstrapping Capability	Yes	No	No	No	No

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APPENDIX 2

Data Communications

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TEST MODES

CDUSCC has three test modes which can be exercised as described below:

BRG Test

All the internal baud rates of the BRG can be tested through TRxC output pin. A simple set up will allow a user to quickly check if the BRG is working correctly. Rx, Tx and DPLL blocks need not be enabled in this setup. The RTxC pin is ignored in these tests.

To test the receiver baud rates on TRxCA pin:

After resetting the chip, load the following two registers:

```
PCRA = '05'   ; TRxCA pin is an output for
                receiver BRG @ 16X
RTRA = '2F'   ; Receive clock select is from
                BRG @ 32X the shift rate
              ; In this case the bit rate is
                38.4k x 32.
```

Then give enough time for the output to come out.

To test the transmitter baud rates on TRxCA pin:

After resetting the chip, load the following two registers:

```
PCRA = '04'   ; TRxCA pin is an output for
                receiver BRG @ 16X
TTRA = '2F'   ; Receive clock select is from
                BRG @ 32X the shift rate.
              ; In this case the bit rate is
                38.4k x 32.
```

Then give enough time for the output to come out.

By varying the value in the RTRA/TTRA register from hex '2F' to '20' all the baud rates can be tested. These tests can be done with a single loop count. When switching one baud rate to another on the fly, make sure that you don't strobe for the output wave forms during these periods. Three new baud rates can be selected by enabling TRCR[1] and appropriate TTR bits.

Tx PLA Test

Tx PLA test can be done by following steps given below:

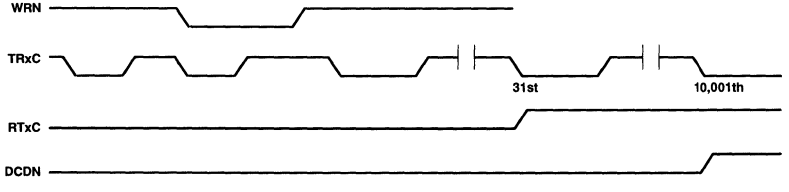
- Force RTxCA pin low
- Force DCDNA pin low
- PCRA = 00 ; TRxC/RTxC as 1X external clocks
- TTRA = 80 ; TRxC external clock
- RTRA = 80 ; TRxC external clock
- CCRA = C6 ; enable Tx PLA test (see timing)
- Force RTxCA pin high at falling edge of 31st TRxC clocks
- Test TxDA pin high on falling edge of 10,001th TRxC clocks
- Force DCDNA pin high to shift signature bits per two clocks
- signature = 0FBEE Hex (18 bits 10,001th to 10,036th clock, LSB first)
- CCRA = 03 ; Tx disable command
- CCRA = 00 ; Reset Tx command

Rx PLA Test

Tx PLA test can be done by following steps given below:

- Force RTxCA pin low
- Force DCDNA pin low
- PCRA = 00 ; TRxC/RTxC as 1X external clocks
- TTRA = 80 ; TRxC external clock
- RTRA = 80 ; TRxC external clock
- CCRA = C7 ; enable Rx PLA test (see timing)
- Force RTxCA pin high at falling edge of 31st TRxC clocks
- Test SYNOUTAN output on falling edge of 10,001th TRxC clocks
- Force DCDNA pin high to shift signature bits per two clocks
- signature = 7045 Hex (16 bits 10,001th to 10,032nd clock, LSB first)
- CCRA = 43 ; Rx disable command
- CCRA = 40 ; Reset Rx command

TIMING



Rising edge of WRN must be followed by falling edge of TRxC when Tx/Rx PLA test is being enabled through CCR command Channels A and B, Tx and Rx PLA can be tested together by writing to both channels and enabling RTxC and DCDN accordingly.

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CROSS-REFERENCE

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Section 4
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Dual universal serial communications controller (DUSCC) SCN68562/ SCN26562

DESCRIPTION

The Philips Semiconductors SCN68/26562 Dual Universal Serial Communications Controller (DUSCC) is a single-chip MOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SCN68562 interfaces to the 68000 MPUs via asynchronous bus control signals and is capable of program-polled, interrupt driven, block-move or DMA data transfers.

The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides 16 common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the DUSCC well suited for dual-speed channel applications. Data rates up to 4Mbits per second are supported.

The transmitter and receiver each contain a four-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to four characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs and outputs are general purpose in nature, they can be optionally programmed for other functions.

FEATURES

General Features

- Dual full-duplex synchronous/asynchronous receiver and transmitter
- Multiprotocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: BISYNC, DDCMP
  - ASYNC: 5–8 bits plus optional parity
- Four character receiver and transmitter FIFOs
- 0 to 4MHz data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 16 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- and half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Compatible with the Philips Semiconductors SCB68430 Direct Memory Access Interface (DMAI) and other DMA controllers
  - Single- or dual-address dual transfers
  - Half- or full-duplex operation
  - Automatic frame termination on counter/timer terminal count or DMA DONE
- Interrupt capabilities
  - Daisy chain option
  - Vector output (fixed or modified by status)
  - Programmable internal priorities
  - Maskable interrupt conditions
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general I/O pins per channel
  - CTS and DCD programmable autoenables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X Rx and Tx clock factors
- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search 1/2-bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmits up to 4Mbs and receive up to 2Mbps data rates

Character-Oriented Protocol Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking

- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK linefill on underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun, and underrun error detection

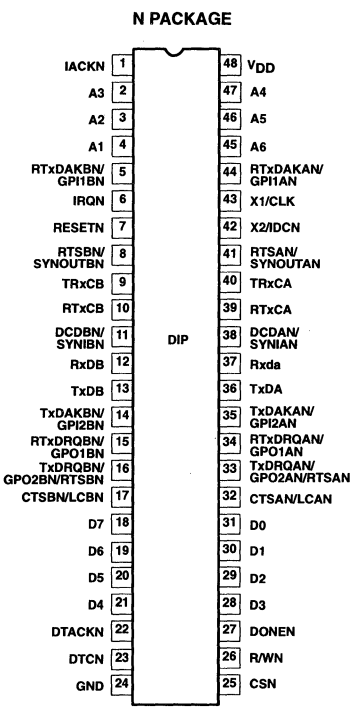
BISYNC Features

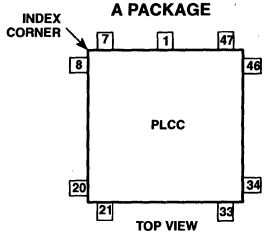
- EBCDIC or ASCII header, text and control messages
- SYN, DLE stripping
- EOM (end of message) detection and transmission
- Auto transparent mode switching
- Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
- Control character sequence detection for both transparent and normal text

Bit-Oriented Protocol Features

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for 1 field
- Zero insertion and deletion
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- ABORT, ABORT-FLAGs, or FCS FLAGs linefill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

PIN CONFIGURATIONS (SCN686562)



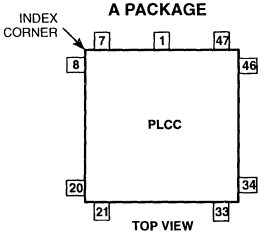


Pin	Function	Pin	Function
1	IACKN	27	CSN
2	A3	28	R/WN
3	A2	29	DONEN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
		32	D1
6	IRQN	33	D0
7	NC	34	NC
8	RESETN	35	CTSAN/LCAN
9	RTSBN/ SYNOUTBN	36	TxDRQAN/ GPO2AN/RTSAN
10	TRxCB	37	RTxDRQAN/ GPO1AN
11	RTxCB		
12	DCDBN/ SYNIBN	38	TxDAKAN/ GPI2AN
13	NC	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	NC
16	TxDAKBN/ GPI2BN	42	DCDAN/ SYNIAN
17	RTxDRQBN/ GPO1BN	43	RTxCA
		44	TRxCA
18	TxDRQBN/ GPO2BN/RTSBN	45	RTSAN/ SYNOUTAN
19	CTSBN/LCBN	46	X2/IDCN
20	D7	47	X1/CLK
21	D6	48	RTxDAKAN/ GPI1AN
22	D5		
23	D4	49	A6
24	DTACKN	50	A5
25	DTCN	51	A4
26	GND	52	V_{DD}

PIN CONFIGURATIONS (SCN266562)

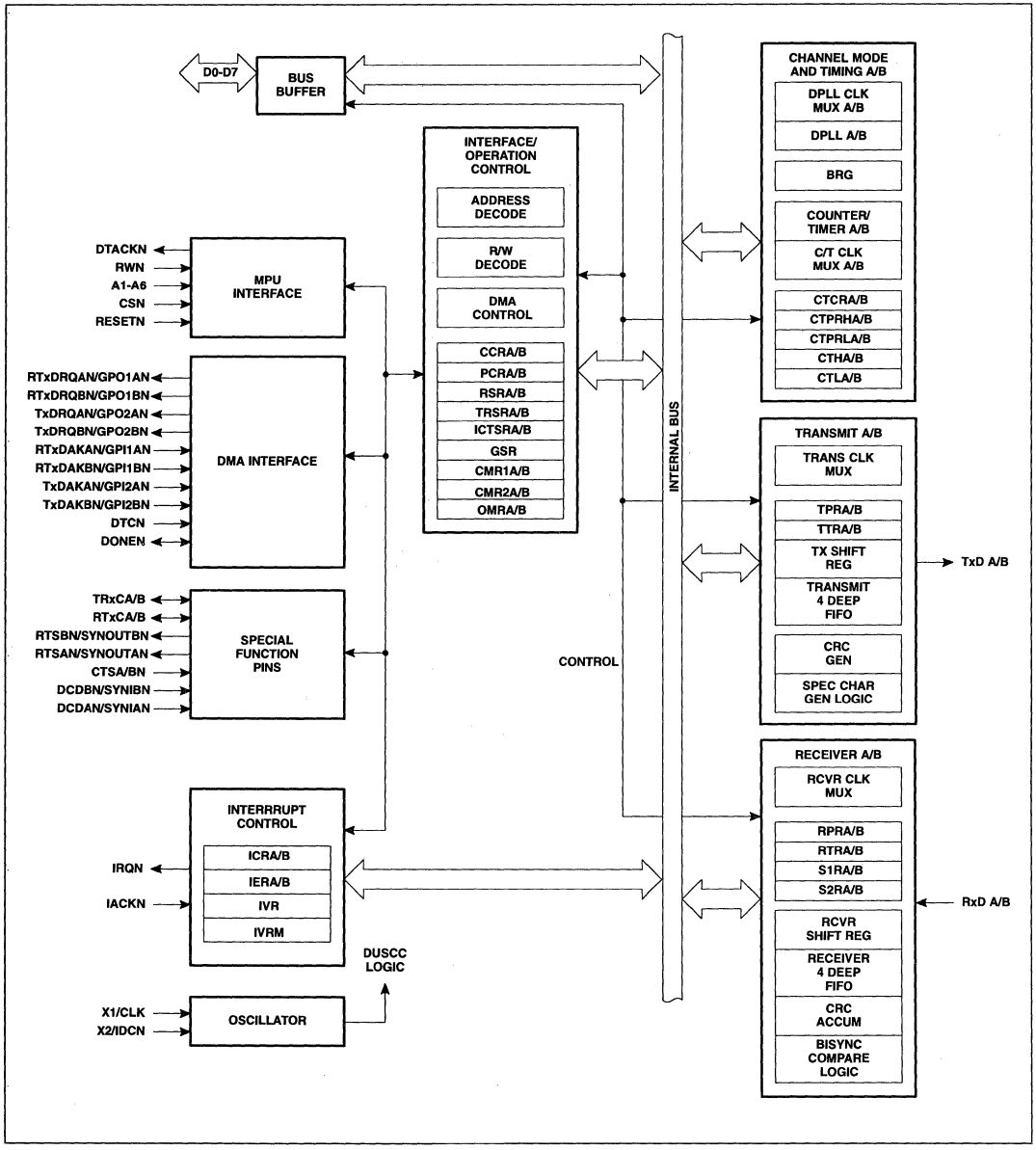
N PACKAGE

A PACKAGE



PIN	FUNCTION	PIN	FUNCTION
1	IACKN	27	CEN
2	A3	28	WRN
3	A2	29	EOPN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
		32	D1
6	IRQN	33	D0
7	NC	34	NC
8	RDYN	35	CTSAN/LCAN
9	RTSBN/ SYNOUTBN	36	TxDRQAN/ GPO2AN/RTSAN
10	TRxCB	37	RTxDRQAN/ GPO1AN
11	RTxCB		
12	DCDBN/ SYNIBN	38	TxDAKAN/ GPI2AN
13	NC	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	NC
16	TxDAKBN/ GPI2BN	42	DCDAN/ SYNIAN
17	RTxDRQBN/ GPO1BN	43	RTxCA
		44	TRxCA
18	TxDRQBN/ GPO2BN/RTSBN	45	RTSAN/ SYNOUTAN
19	CTSBN/LCBN	46	X2
20	D7	47	X1/CLK
21	D6	48	RTxDAKAN/ GPI1AN
22	D5		
23	D4	49	A6
24	RDN	50	A5
25	RESETN	51	A4
26	GND	52	VCC

BLOCK DIAGRAM



PIN DESCRIPTION (SCN68562)

In this data sheet, signals are discussed using the terms 'active' and 'inactive' or 'asserted' and 'negated' independent of whether the signal is active in the High (logic 1) or Low (logic 0) state. N at the end of a pin name signifies the signal associated with the pin is active-Low (see individual pin description for the definition of the active level of each signal.) Pins which are provided for both channels are designated by A/B after the name of the pin and the active-Low state indicator, N, if applicable. A similar method is used for registers provided for both channels: these are designated by either an underline or by A/B after the name.

MNEMONIC	DIP PIN NO.	TYPE	NAME AND FUNCTION
A1 – A6	4-2, 45-47	I	**Address Lines:** Active-High. Address inputs which specify which of the internal registers is accessed for read/write operation.
D0 – D7	31-28, 21-18	I/O	**Bidirectional Data Bus:** Active High, 3-State. Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the DUSCC take place over this bus. The data bus is enabled when CSN is Low, during interrupt acknowledge cycles and single-address DMA acknowledge cycles.
R/WN	26	I	**Read/Write:** A High input indicates a read cycle and a Low input indicates a write cycle when a cycle is initiated by assertion of the CSN input.
CSN	25	I	**Chip Select:** Active-Low input. When Low, data transfers between the CPU and the DUSCC are enabled on D0 – D7 as controlled by the R/WN and A1 – A6 inputs. When CSN is High, the DUSCC is isolated from the data bus (except during interrupt acknowledge cycles and single-address DMA transfers) and D0 – D7 are placed in the 3-State condition.
DTACKN	22	O	**Data Transfer Acknowledge:** Active-Low, 3-State. DTACKN is asserted on a write cycle to indicate that the data on the bus has been latched, and on a read cycle or interrupt acknowledge cycle to indicate valid data is on the bus. The signal is negated when completion of the cycle is indicated by negation of the CSN or IACKN input, and returns to the inactive state (3-State) a short period after it is negated. In a single address DMA mode, data is latched with the falling edge of DTCN. DTACKN is negated when completion of the cycle is indicated by the assertion of DTCN or negation of DMA acknowledge inputs (whichever occurs first), and returns to the inactive state (3-State) a short period after it is negated. When negated, DTACKN becomes an open-drain output and requires an external pull-up resistor.
IRQN	6	O	**Interrupt Request:** Active-Low, open-drain. This output is asserted upon occurrence of any enabled interrupting condition. The CPU can read the general status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the DUSCC to output an interrupt vector on the data bus.
IACKN	1	I	**Interrupt Acknowledge:** Active-Low. When IACKN is asserted, the DUSCC responds by placing the contents of the interrupt vector register (modified or unmodified by status) on the data bus and asserting DTACKN. If no active interrupt is pending, DTACKN is not asserted.
X1/CLK	43	I	**Crystal or External Clock:** When using the crystal oscillator, the crystal is connected between pins X1 and X2. If a crystal is not used, and external clock is supplied at this input. This clock is used to drive the internal bit rate generator, as an optional input to the counter/timer or DPLL, and to provide other required clocking signals.
X2/IDCN	42	I/O	**Crystal or Interrupt Daisy Chain:** When a crystal is used as the timing source, the crystal is connected between pins X1 and X2. This pin can be programmed to provide and interrupt daisy chain active-Low output which propagates the IACKN signal to lower priority devices, if no active interrupt is pending. This pin should be grounded when an external clock is used on X1 and X2, is not used as an interrupt daisy chain output.
RESETN	7	I	**Master Reset:** Active-Low. A low on this pin resets the transmitters and receivers and resets the registers shown in Table 1. Reset in asynchronous, i.e., no clock is required.
RxDA, RxDB	37, 12	I	**Channel A (B) Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified for the channel, the input is sampled on the rising edge of the clock.
TxDA, TxDB	36, 13	O	**Channel A (B) Transmitter Serial Data Output:** The least signifiicant bit is transmitted first. This output is held in the marking (High) condition when the transmitter is disabled or when the channel is operating in local loopback mode. If external transmitter clock is specified for the channel, the data is shifted on the falling edge of the clock.
RTxCA, RTxCB	39, 10	I/O	**Channel A (B) Receiver/Transmitter Clock:** As an input, it can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, can supply the counter/timer output, the transmitter shift clock (1X), or the receiver sampling clock (1X). The maximum external receiver/transmitter clock frequency is 4MHz.
TRxCA, TRxCB	40, 9	I/O	**Channel A (B) Transmitter/Receiver Clock:** As an input, it can supply the receiver, transmitter, counter/ timer, or DPLL clock. As an output, it can supply the counter/timer output, the DPLL output, the transmitter shift clock (1X), the receiver sampling clock (1X), the transmitter BRG clock (16X), The receiver BRG clock (16X), or the internal system clock (X1/2). The maximum external receiver/transmitter clock frequency is 4MHz.

PIN DESCRIPTION (SCN68562) (Continued)

MNEMONIC	DIP PIN NO.	TYPE	NAME AND FUNCTION
CTSA/BN, LCA/BN	32, 17	I/O	**Channel A (B) Clear-To-Send Input or Loop Control Output:** Active-Low. The signal can be programmed to act as an enable for the transmitter when not in loop mode. The DUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. When operating in the COP loop mode, this pin becomes a loop control output which is asserted and negated by DUSCC commands. This output provides the means of controlling external loop interface hardware to go on-line and off-line without disturbing operation of the loop.
DCDA/BN, SYNIA/BN	38, 11	I	**Channel A (B) Data Carrier Detected or External Sync Input:** The function of this pin is programmable. As a DCD active-Low input, it acts as an enable for the receiver or can be used as a general purpose input for the DCD function, the DUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. As an active-Low external sync input, it is used in COP modes to obtain character synchronization without receipt of a SYN character. This mode can be used in disc or tape controller applications or for the optional byte timing lead in X.21.
RTxDRQA /BN, GPO1A/B N	34, 15	O	**Channel A (B) Receiver/Transmitter DMA Service Request or General Purpose Output:** Active-Low. For half-duplex DMA operation, this output indicates to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or that the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, this output indicates to the DMA controller that data is available in the receiver FIFO. In non-DMA mode, this pin is a general purpose output that can be asserted and negated under program control.
TxDRQA/ BN, GPO2A/B N, RTSA/BN	33, 16	O	**Channel A (B) Transmitter DMA Service Request, General Purpose Output, or Request-to-Send:** Active-Low. For full-duplex DMA operation, this output indicates to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full-duplex DMA mode, this pin can be programmed as a general purpose or a Request-to -Send output, which can be asserted and negated under program control (see Detailed Operation).
RTxDAKA/ BN, GPI1A/BN	44, 5	I	**Channel A (B) Receiver/Transmitter DMA Acknowledge or General Purpose Input:** Active-Low. For half-duplex single address DMA operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO or load transmitter FIFO) is beginning. For full-duplex single address DMA operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested read receiver FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in single address DMA mode.
TxDAKA/B N, GP12A/BN	35, 14	I	**Channel A (B) Transmitter DMA Acknowledge or General Purpose Input:** Active-Low. When the channel is programmed for full-duplex single address DMA operation, this input is asserted to indicate to the DUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in full-duplex single address DMA mode.
DTCN	23	I	**Device Transfer Complete:** Active-Low. DTCN is asserted by the DMA controller to indicate that the requested data transfer is complete.
DONEN	27	I/O	**Done:** Active-Low, open-drain. See Detailed Operation for a description of the function of this pin.
RTSA/BN, SYNOUTA /BN	41, 8	O	**Channel A (B) Sync Detect or Request-to-Send:** Active-Low. If programmed as a sync output, it is asserted one bit time after the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes) is detected by the receiver. As a Request-to-Send modem control signal, it functions as described previously for the TxDRQN/RTSN pin.
V_{DD}	48	I	+5V ± 10% power input.
GND	24	I	Signal and power ground input.

PIN DESCRIPTION (SCN26562)

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A1–A6	4–2, 47–45	4–2, 51–49	I	Address lines.
D0–D7	31–28, 21–18	33–30, 23–20	I/O	Bidirectional data bus.
RDN	22	24	I	Read strobe.
WRN	26	28	I	Write strobe.
CEN	25	27	I	Chip select.
RDYN	7	8	O	Ready.
IRQN	6	6	O	Interrupt request.
IACKN	1	1	I	Interrupt acknowledge.
X1/CLK	43	47	I	Crystal 1 or external clock.
X2	42	46	I	Crystal 2.
RESETN	23	25	I	Master reset.
RxDA, RxDB	37, 12	40, 14	I	Channel A (B) receiver serial data.
TxDA, TxDB	36, 13	39, 15	O	Channel A (B) transmitter serial data.
RTxCA, RTxCB	39, 10	43, 11	I/O	Channel A (B) receiver/transmitter clock.
TRxCA, TRxCB	40, 9	44, 10	I/O	Channel A (B) transmitter/receiver clock.
CTSA/BN, LCA/BN	32, 17	35, 19	I/O	Channel A (B) clear-to-send input or loop control output.
DCDA/BN, SYNIA/BN	38, 11	42, 12	I	Channel A (B) data carrier detected or external sync.
RTxDRQA/BN, GPO1A/BN	34, 15	37, 17	O	Channel A (B) receiver/transmitter DMA service request or general purpose output.
TxDRQA/BN, GPO2A/BN, RTSA/BN	33, 16	36, 18	O	Channel A (B) transmitter DMA service request, general purpose output or request-to-send.
RTxDAKA/BN, GPI1A/BN	44, 5	48, 5	I	Channel A (B) receiver/transmitter DMA acknowledge or general purpose input 1.
TxDAKA/BN, GPI2A/BN	35, 14	38, 16	I	Channel A (B) transmitter DMA acknowledge or general purpose input 2.
EOPN	27	29	I/O	DMA transfer complete.
RTSA/BN, SYNOUTA/BN	41, 8	45, 9	O	Channel A (B) request-to-send or Sync detect.
V_{CC}	48	52	I	Power input.
GND	24	26	I	Signal and power ground.

REGISTERS

The addressable registers of the DUSCC are shown in Table 1. The following rules apply to all registers:

1. A read from a reserved location in the map results in a read from the 'null register'. The null register returns all ones for data and results in a normal bus cycle. A write to one of these locations results in a normal bus cycle without a write being performed.

2. Unused bits of a defined register are read as zeros, unless ones have been loaded after master reset.

3. Bits that are unused in the chosen mode but are used in others are readable and writable but their contents are ignored in the chosen mode.

4. All registers are addressable as 8-bit quantities. To facilitate operation with the 68000 MOVEP instruction, addresses are ordered such that certain sets of registers may also be accessed as words or long words.

The operation of the DUSCC is programmmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The contents of certain control registers are initialized on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems, e.g., changing the channel mode at an inappropriate time may cause the reception or transmission of an incorrect character. In general, the contents of registers which control transmitter or receiver operation, or the counter/timer, should be changed only when they are not enabled.

The DUSCC registers can be separated into five groups to facilitate their usage:

1. Channel mode configuration and pin description registers.

2. Transmitter and receiver parameter and timing registers.
3. Counter/timer control and value registers.
4. Interrupt control and status registers.
5. Command register.

This arrangement is used in the following description of the DUSCC registers.

Channel Mode Configuration and Pin Description Registers

There are five registers in this group for each channel. The bit format for each of these registers is contained in Table 2. The primary function of these registers is to define configuration of the channels and the function of the programmable pins. A channel cannot be dynamically reconfigured. Do not write to CMR1 or CMR2 if the receiver or transmitter is enabled.

Channel Mode Register 1 (CMR1A, CMR1B)

[7:6] Data Encoding — These bits select the data encoding for the received and transmitted data:

00 If the DPLL is set to NRZI mode (see DPLL commands), it selects positive logic (1 = High, 0 = Low). If the DPLL is set to FM mode (see DPLL commands), Manchester (bi-phase level) encoding is selected.

01 NRZI. Non-return-to-zero inverted.

10 FM0. Bi-phase space.

11 FM1. Bi-phase mark.

[5] Extended Control (BOP) —

0 No. A one-octet control field follows the address field.

1 Yes. A two-octet control field follows the address field.

[5] Parity (COP/ASYNC), Code Select (BISYNC) —

0 Even parity if with parity is selected by [4:3] or a 0 in the parity bit position if force parity is selected by [4:3]. In BISYNC protocol mode, internal character comparisons are made using EBCDIC coding.

1 Odd parity if with parity is selected by [4:3] or a 1 in the parity bit position if force parity is selected by [4:3]. In BISYNC protocol mode, internal character comparisons are made using 7-bit plus odd parity ASCII coding. (Note: The receiver should be programmed for 7-bit characters, RPR[1:0] = 11, with no parity, CMR1[4:3] = 00.)

[4:3] Address Mode (BOP) — This field controls whether a single octet or multiple octets follow the opening FLAG(s) for both the receiver and the transmitter. This field is activated by selection of BOP secondary mode through the channel protocol mode bits CMR1[2:0] (see Detailed Operation).

00 Single-octet address.

01 Extended address.

10 Dual-octet address.

11 Dual-octet address with group.

[4:3] Pairty Mode (COP/ASYNC) — This field selects the parity mode for both the receiver and the transmitter. A parity bit is added to the programed character length if with parity or force parity is selected:

00 No pairty. Required when BISYNC protocol mode is programmed.

01 Reserved.

10 With parity. Odd or even parity is selected by [5].

11 Force parity. The parity bit is forced to the state selected by [5].

[2:0] Channel Protocol Mode — This field selects the operational protocol and submode for both the receiver and transmitter:

000 BOP Primary. No address comparison is performed. For receive, all characters received after the opening FLAG(s) are transferred to the FIFO.

001 BOP Secondary. This mode activates the address modes selected by [4:3]. Except in the case of extended address ([4:3] = 01), and address comparison is performed to determine if a frame should be received. Refer to Detailed Operation for details of the various addressing modes. If a valid comparison occurs, the receiver is activated and the address octets and all subsequent received characters of the frame are transferred to the receive FIFO.

010 BOP Loop. The DUSCC acts as a secondary station in a loop. The GO-ON-LOOP and GO-OFF-LOOP commands are used to cause the DUSCC to go on and off the loop. Normally, the TxD output echos the RxD input with a two-bit time delay. If the transmitter is enabled and the 'go active on poll' command has been asserted, the transmitter will begin sending when an EOP sequence consisting of a zero followed by seven ones is detected. The DUSCC changes the last one of the EOP to zero, making it another FLAG, and then operates as described in the Detailed Operation section. The loop sending status bit (TRSR[6]_ is asserted concurrent with the beginning of transmission. The frame should normally be terminated with an EOM followed by an echo of the marking RxD line so that secondary stations further down the loop can append their messages to the messages from up-loop stations by the same process. If the 'go active on poll' command is not asserted, the transmitter remains inactive (other than echoing the received data) even when the EOP sequence is received.

011 BOP Loop without address comparison. Same as normal loop mode except that address field comparisons are disabled. All received frames are transmitted to the CPU.

100 COP Dual SYN. Character sync is achieved upon receipt of a bit sequence matching the contents of the appropriate bits of S1R and S2R (SYN1-SYN2), including parity bits if any.

101 COP Dual SYN (BISYNC). Character sync is achieved upon receipt of a bit sequence matching the contents of the appropriate bits of S1R and S2R (SYN1-SYN2). In this mode, special transmitter and receive logic is activated. Transmitter and receiver character length must be programmed to 8 bits and no parity (see Detailed Operation).

110 COP Single SYN. Character sync is achieved upon receipt of a bit sequence matching the contents of the appropriate bits of S1R (SYN1), including parity bit if any. This mode is required when the external sync mode is selected (see description of RPR[4], BOP/COP).

111 Asynchronous. Start/stop format.

Table 1. DUSCC Register Address Map

ADDRESS BITS* 6 5 4 3 2 1	ACRONYM	REGSITER NAME	MODE	AFFECTED BY RESET
c 0 0 0 0 0	CMR1	Channel Mode Register 1	R/W	Yes—00
c 0 0 0 0 1	CMR2	Channel Mode Register 2	R/W	Yes—00
c 0 0 0 1 0	S1R	SYN 1/Secondary Address 1 Register	R/W	No
c 0 0 0 1 1	S2R	SYN 2/Secondary Address 2 Register	R/W	No
c 0 0 1 0 0	TPR	Transmitter Parameter Register	R/W	Yes—00
c 0 0 1 0 1	TTR	Transmitter Timing Register	R/W	No
c 0 0 1 1 0	RPR	Receiver Parameter Register	R/W	Yes—00
c 0 0 1 1 1	RTR	Receiver Timing Register	R/W	No
c 0 1 0 0 0	CTPRH	Counter/Timer Preset Register High	R/W	No
c 0 1 0 0 1	CTPRL	Counter/Timer Preset Register Low	R/W	No
c 0 1 0 1 0	CTCR	Counter/Timer Control Register	R/W	Yes—00
c 0 1 0 1 1	OMR	Output and Miscellaneous Register	R/W	Yes—00
c 0 1 1 0 0	CTH	Counter/Timer High	R	No
c 0 1 1 0 1	CTL	Counter/Timer Low	R	No
c 0 1 1 1 0	PCR	Pin Configuration Register	R/W	Yes—00
c 0 1 1 1 1	CCR	Channel Command Register	R/W	No
c 1 0 0 X X	TxFIFO	Transmitter FIFO	W	No
c 1 0 1 X X	RxFIFO	Receiver FIFO	R	No
c 1 1 0 0 0	RSR	Receiver Status Register	R/W**	Yes—00
c 1 1 0 0 1	TRSR	Transmitter and Receiver Status Register	R/W**	Yes—00
c 1 1 0 1 0	ICTSR	Input and Counter/TImer Status Register	R/W**	Yes
d 1 1 0 1 1	GSR	General Status Register	R/W**	Yes—00
c 1 1 1 0 0	IER	Interrupt Enable Register	R/W	Yes—00
c 1 1 1 0 1		Not used		
0 1 1 1 1 0	IVR	Interrupt Vector Register— Unmodified	R/W	Yes—0F
1 1 1 1 1 0	IVRM	Interrupt Vector Register— Modified	R	Yes—FF
0 1 1 1 1 1	ICR	Interrupt Control Register	R/W	Yes—00
1 1 1 1 1 1		Not used		

NOTES:
* c = 0 for Channel A, c = 1 for Channel B.
d = don't care — register may be accessed as either channel.
x = don't care — FIFOs are addressable at any of four adjacent addresses to allow them to be addressed as byte/word/long word with the 68000 MOVEP instruction.
** A write to this register may perform a status resetting operation.

Channel Mode Register 2 (CMR2A, CMR2B)

[7:6] Channel Connection — This field selects the mode of operation of the channel. The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character.

00 Normal mode. The transmitter and receiver operate independently in either half- or full-duplex, controlled by the respective enable commands.

01 Automatic echo mode. Automatically retransmits the received data with a half-bit time delay (ASYNC, 16X clock mode) or a two-bit time delay (all other modes). The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxD output.
2. The receiver clock is used for the transmitter for ASYNC 16X clock mode. For other modes the transmitter clock must be supplied.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The TxRDY and underrun status bits are inactive.
5. The received parity and/or FCS are checked if required, but are not regenerated for transmission, i.e., transmitted parity and/or FCS are as received.
6. In ASYNC mode, character framing is checked, but the stop bits are retransmitted as received. A received break is echoed as received.
7. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

10 Local loopback mode. In this mode:

1. The transmitter data output and clock are internally connected to the receiver.
2. The transmit clock is used for the receiver if NRZI or NRZ encoding is used. For FM or Manchester encoding because the receiver clock is derived from the DPLL, the DPLL source clock must be maintained.
3. The TxD output is held High.
4. The RxD input is ignored.
5. The receiver and transmitter must be enabled.
6. CPU to transmitter and receiver communications continue normally.

11 Reserved.

[5:3] Data Transfer Interface — This field specifies the type of data transfer between the DUSCC's Rx and TxFIFOs and the CPU. All interrupt and status functions operate normally regardless of the data transfer interface programmed. Refer to Detailed Operation for details of the various DMA transfer interfaces.

000 Half-duplex single address DMA.

001 Half-duplex dual address DMA.

010 Full-duplex single address DMA.

011 Full-duplex dual address DMA.

100 Wait on receive only. In this mode a read of a non-empty receive FIFO results in a normal bus cycle. However, if the receive FIFO of the channel is empty when a read Rx FIFO cycle is initiated, the DTACKN output remains negated until a character is received and loaded into the FIFO. DTACKN is then asserted and the cycle is completed normally.

101 Wait on transmit only. In this mode a write to a non-full transmit FIFO results in a normal bus cycle. However, if the transmit FIFO of the channel is full when a write TxFIFO cycle is initiated, the DTACKN output remains negated until a FIFO position becomes available for the new character. DTACKN is then asserted and the cycle is completed normally.

110 Wait on transmit and receive. As above for both wait on receive and transmit operations.

111 Polled or interrupt. DMA and wait function of the channel are not activated. Data transfers to the Rx and TxFIFOs are via normal bus read and write cycles in response to polling of the status registers and/or interrupts.

[2:0] Frame Check Sequence Select — This field selects the optional frame check sequence (FCS) to be appended at the end of a transmitted frame. When CRC is selected in COP, then no pairty and 8-bit character length must be used. The selected FCS is transmitted as follows:

1. Following transmission of a FIFOed character tagged with the 'send EOM' command.
2. If underrun control (TPR[7:6]) is programmed for TEOM, upon occurrence of an underrun.
3. If TEOM on zero count or done (TPR[4]) is asserted and the counter/timer is counting transmitted characters, after transmission of the character which causes the counter to reach zero count.
4. In DMA mode with TEOM on zero count or done (TPR[4]) set, after transmission of a character if DONEN is asserted when that character was loaded into the TxFIFO by the DMA controller.

000 No frame check sequence.

001 Reserved

010 LRC8: Divsior = $x^8 + 1$, dividend preset to zeros. The Tx sends the calculated LRC non-inverted. The Rx indicates and error if the computed LRC is not equal to 0. Valid for COP modes only.

011 LRC8: Divisor = $x^8 + 1$, dividend preset to ones. The Tx sends the calculated LRC non-inverted. The Rx indicates an error if the computed LRC is not equal to 0. Valid for COP modes only.

100 CRC16: Divisor - $x^{16} + x^{15} + x^2 + 1$, dividend preset to zeros. The Tx sends the calculated CRC non-inverted. The Rx indicates an error if the comuted CRC is not equal to 0. Not valid for ASYNC mode.

101 CRC16: Divisor = $x^{16} + x^{15} + x^2 + 1$, dividend preset to ones. The Tx sends the calculated CRC non-inverted. The Rx indicates an error if the computed CRC is not equal to 0. Not valid for ASYNC mode.

110 CRC-CCITT: Divisor = $x^{16} + x^{12} + x^5 + 1$, dividend preset to zeros. The Tx sends the calculated CRC non-inverted. The Rx indicates an error if the computed CRC is not equal to 0. Not valid for ASYNC mode.

111 CRC-CCITT: Divisor = $x^{16} + x^{12} + x^5 + 1$, dividend preset to ones. The Tx sends the calculated CRC inverted. The Rx indicates an error if the computed CRC is not equal to H'F0B8'. Not valid for ASYNC mode.

SYN1/Secondary Address 1 Register (S1RA, S1RB)

[7:0} Character Compare — In ASYNC mode this register holds a 5- to 8-bit long bit pattern which is ocmpared with received characters. if a match occurs, the character compare status bit (RSR[7]) is set. This field is ignored if the receiver is in a break condition.

In COP modes, this register contains the 5- to 8-bit SYN1 bit pattern, right justified. Parity bit need not be included in the value placed in the register even is parity is specified in CMR1[4:3]. However, a character received with parity error, when parity is specified, will not match. In ASYNC, or COP modes, if parity is specified, then any unused bits in this register must be programmed to zeros. In BOP secondary mode it contains the address used to compare the first received address octet. The register is not used in BOP primary mode or secondary modes where address comparisons are not made, such as when extended addressing is specified.

SYN2/Secondary Address 2 Register (S2RA, S2RB)

[7:0] — This register is not used in ASYNC, COP single SYN, BOP primary modes, BOP secondary modes with single address field, and BOP secondary modes where address comparisons are not made, such as when extended addressing is specified.

In COP dual SYN modes, it contains the 5- to 8-bit SYN2 bit pattern, right justified, Parity bit need not be included in the value placed in the register even if parity is specified in CMR1[4:3]. However, a character received with parity error, when parity is specified, will not match. If parity is specified, then any unused bits in this register must be programmed to zeros. In BOP secondary mode using two address octets, it contains the partial address used to compare the second received address octet.

Table 2. Channel Configuration/Pin Definition Registers Bit Formats

CHANNEL MODE REGISTER 1

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Data Encoding		Extended Control	Address Mode (BOP)		Channel Protocol Mode		
(CMR1A, CMR1B)	00 — NRZ/Manchester 01 — NRZI 10 — FM0 11 — FM1		BOP only 0 — no 1 — yes	00 — 8-bit 01 — extended address 10 — 16-bit 11 — 16-bit w/group		000 — BOP primary 001 — BOP secondary 010 — BOP loop 011 — BOP loop – no adr. comp.		
			Parity*	Parity Mode (COP/ASYNC)				
			0 — even 1 — odd	00 — no parity 01 — reserved 10 — with parity 11 — force parity		100 — COP dual SYN 101 — COP dual SYN (BISYNC) 110 — COP single SYN 111 — asynchronous		

NOTE:
* In BISYNC protocol mode, 0 = EBCDIC, 1 = ASCII coding.

CHANNEL MODE REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Channel Connection		Data Transfer Interface			Frame Check Sequence Select		
(CMR2A, CMR2B)	00 — normal 01 — auto echo 10 — local loop 11 — reserved		000 — half-duplex single address DMA 001 — half-duplex dual address DMA 010 — full-duplex single address DMA 011 — full-duplex dual address DMA 100 — wait on Rx only 101 — wait on Tx only 110 — wait on Rx or Tx 111 — polled or interrupt			000 — none 001 — reserved 010 — LRC8 preset 0s 011 — LRC8 preset 1s 100 — CRC 16 preset 0s 101 — CRC 16 preset 1s 110 — CRC CCITT preset 0s 111 — CRC CCITT preset 1s		

SYN1/SECONDARY ADDRESS REGISTER 1

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(S1RA, S1RB)	ASYNC — Character compare (5 – 8 bits) COP — SYN1 (5 – 8 bits) BOP — First address octet							

SYN2/SECONDARY ADDRESS REGISTER 2

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(S2RA, S2RB)	ASYNC — not used COP — SYN2 (5 – 8 bits) BOP — Second address octet							

PIN CONFIGURATION REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	X2/IDS	GPO2/RTS	SYNOUT/RTS	RTxC Pin		TRxC Pin		
(PCRA, PCRB)	* 0 — X2 1 — IDC	0 — GPO2 1 — RTS	0 — SYNOUT 1 — RTS	00 — input 01 — C/T 10 — TxCLK 1X 11 — RxCLK 1X		000 — input 001 — XTAL/2 010 — DPLL 011 — C/T	100 — TxCLK 16X 101 — RxCLK 16X 110 — TxCLK 1X 111 — RxCLK 1X	

NOTE:
* PCRA only. Not used in PCRB.

Pin Configuration Register (PCRA, PCRB)

This register selects the functions for multipurpose I/O pins.

[7] X2/IDC — This bit is defined only for PCRA. It is not used in PCRB.

0 The X2/IDCN pin is used as a crystal connection.

1 The X2/IDCN pin is the interrupt daisy chain output.

[6] GPO2/RTS — The function of this pin is programmable only when not operating in full-duplex DMA mode.

0 The TxDRQN/GPO2N/RTSN pin is a general purpose output. It is Low when OMR[2] is a 1 and High when OMR[2] is a 0.

1 The pin is a request-to-send output (see Detailed Operation). The logical state of the pin is controlled by OMR[0]. When OMR[0] is set, the output is Low.

[5] SYNOUT/RTS —

0 The SYNOUTN/RTSN pin is an active-Low output which is asserted one bit time after a SYN pattern (COP modes) in HSRH/HSRL or FLAG (BOP modes) is detected in CCSR. The output remains asserted for one receiver clock period. See Figure 1 for receiver data path.

1 The pin is a request-to-send output (see Detailed Operation). The logical state of the pin is controlled by OMR[0] when OMR[0] is set, the output is Low.

[4:3] RTxC —

00 The pin is an input. It must be programmed for input when used as the input for the receiver or transmitter clock, the DPLL, or the C/T.

01 The pin is an output for the counter/timer. Refer to CTCRA/B description.

10 The pin is an output for the transmitter shift register clock.

11 The pin is an output for the receiver shift register clock.

[2:0] TRxC —

000 The pin is an input. It must be programmed for input when used as the input for the receiver or transmitter clock, the DPLL, or the C/T.

001 The pin is an output from the crystal oscillator divided by two.

010 The pin is an output for the DPLL output clock.

011 The pin is an output for the counter/timer. Refer to CTCRA/B description.

100 The pin is an output for the transmitter BRG at 16X the rate selected by TTR [3:0].

101 The pin is an output for the receiver BRG at 16X the rate selected by RTR [3:0].

110 The pin is an output for the transmitter shift register clock.

111 The pin is an output for the receiver shift register clock.

Transmitter and Receiver Parameter and Timing Registers

This set of five registers contains the information which controls the operation of the transmitter and receiver for each channel. Table 3 shows the bit map format for each of these registers. The registers of this group are:

1. Transmitter parameter and timing registers (TPRA/B and TTRA/B)
2. Receiver parameter and timing registers (RPRA/B and RTRA/B)
3. Output and miscellaneous register (OMRA/B).

The first and second group of registers define the transmitter and receiver parameters and timing. Included in the receiver timing registers are the programming parameters for the DPLL. The last register of the group, OMR contains additional transmitter and receiver information and controls the logical state of the output pins when they are not used as a part of the channel configuration.

A channel cannot be dynamically reconfigured. Do not write to the RPR if the receiver is enabled, and do not write to the TPR if the transmitter is enabled.

Table 3. Transmitter and Receiver Parameter and Timing Register Bit Format

TRANSMITTER PARAMETER REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(TPRA, TPRB)	**Underrun Control**		**Idle**	**TEOM on Zero Cnt or Done**	**Tx RTS Control**	**CTS Enable Tx**	**Tx Character Length**	
COP	00 — FCS-idle 01 — reserved 10 — MARKs 11 — SYNs		0 — MARKs 1 — SYNs	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	00 — 5 bits 01 — 6 bits 10 — 7 bits 11 — 8 bits	
	Underrun Control		**Idle**	**TEOM on Zero Cnt or Done**				
BOP	00 — FCS-FLAG-idle 01 — reserved 10 — ABORT-MARKs 11 — ABORT-FLAGs		0 — MARKs 1 — FLAGs	0 — no 1 — yes				
	Stop Bits Per Character							
ASYNC	9/16 to 1, 17/16 to 1.5, 25/16 to 2 programmable in 1/16-bit increments							

TRANSMITTER TIMING REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(TTRA, TTRB)	**External Source**	**Transmitter Clock Select**			**Bit Rate Select**			
	0 — RTxC 1 — TRxC	000 — 1X external 001 — 16X external 010 — DPLL 011 — BRG 100 — 2X other channel C/T 101 — 32X other channel C/T 110 — 2X own channel C/T 111 — 32X own channel C/T			one of sixteen rates from BRG			

RECEIVER PARAMETER REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(RPRA, RPRB)	not used	not used	not used	**Rx RTS Control**	**Strip Parity**	**DCD Enable Rx**	**Rx Character Length**	
ASYNC				0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	00 — 5 bits 01 — 6 bits	
COP	**SYN Strip**	**FCS to FIFO**	**Auto Hunt & Pad Chk**	**Ext Sync**	**Strip Parity**		10 — 7 bits 11 — 8 bits	
	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes			
	not used	**FCS to FIFO**	**Overrun Mode**	not used	**All Parity Address**			
BOP		0 — no 1 — yes	0 — hunt 1 — cont		0 — no 1 — yes			

Table 3. Transmitter and Receiver Parameter and Timing Register Bit Format (Continued)

RECEIVER TIMING REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(RTRA, RTRB)	External Source	Receiver Clock Select			Bit Rate Select			
	0 — RTxC 1 — TRxC	000 — 1X external 001 — 16X external 010 — BRG 011 — C/T of channel 100 — DPLL, source = 64X X1/CLK 101 — DPLL, source = 32X External 110 — DPLL, source = 32X BRG 111 — DPLL, source = 32X C/T		ASYNC protocol mode only	one of sixteen rates from BRG			

OUTPUT AND MISC REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(OMRA, OMRB)	Tx Residual Character Length			TxRDY Activate	RxRDY Activate	OUT 2	OUT 1	RTS
	000 — 1 bit 001 — 2 bits 010 — 3 bits 011 — 4 bits 100 — 5 bits 101 — 6 bits 110 — 7 bits 111 — same as TPR[1:0]			0 — FIFO not full 1 — FIFO empty	0 — FIFO not empty 1 — FIFO full	Bit Pin 0 — H 1 — L	Bit Pin 0 — H 1 — L	Bit Pin 0 — H 1 — L

Transmitter Parameter Register (TPRA, TPRB)

[7:6] Underrun Control — In BOP and COP modes, this field selects the transmitter response in the event of an underrun (i.e., the TxFIFO is empty).

00 Normal end of message termination. In BOP, the transmitter sends the FCS (if selected by CMR2[2:0]) followed by a FLAG and then either MARKs or FLAGs, as specified by [5]. In COP, the transmitter sends the FCS (if selected by CMR2[2:0]) and then either MARKs or SYNs, as specified by [5].

01 Reserved.

10 In BOP, the transmitter sends an ABORT (11111111) and then places the TxD output in a marking condition until receipt of further instructions. In COP, the transmitter places the TxD output in a marking condition until receipt of further instructions.

11 In BOP, the transmitter sends an ABORT (11111111) and then sends FLAGs until receipt of further instruction. In COP, the transmitter sends SYNs until receipt of further instructions.

[5] Idle — In BOP and COP modes, this bit selects the transmitter output during idle. Idle is defined as the state following a normal end of message until receipt of the next transmitter command.

0 Idle in marking condition.

1 Idle sending SYNs (COP) or FLAGs (BOP).

[4] Transmit EOM on Zero Count or Done — In BOP and COP modes, the assertion of this bit causes the end of message (FCS in COP, FCS-FLAG in BOP) to be transmitted upon the following events:

1. If the counter/timer is counting transmitted characters, after transmission of the character which causes the counter to reach zero count. (DONEN is also asserted as an output if the channel is in a DMA operation.)
2. If the channel is operating in DMA mode, after transmission of a character if DONEN was asserted when that character was loaded into the TxFIFO by the DMA controller.

[7:4] Stop Bits per character — In ASYNC mode, this field programs the length of the stop bit appended to the transmitted character as shown in Table 4.

Table 4. Stop Bits — Transmitted Character

[7:4]	5 BITS/CHAR	6, 7 or 8 BITS/ CHAR
0000	1.063	0.563
0001	1.125	0.625
0010	1.188	0.688
0011	1.250	0.750
0100	1.313	0.813
0101	1.375	0.875
0110	1.438	0.938
0111	1.500	1.000
1000	1.563	1.563
1001	1.625	1.625
1010	1.688	1.688
1011	1.750	1.750
1100	1.813	1.813
1101	1.875	1.875
1110	1.938	1.938
1111	2.000	2.000

Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16-bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16-bit. The receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit if parity is enabled) in all cases.

If an external 1X clock (or a 2X clock for counter/timer) is used for the transmitter, [7] = 0 selects one stop bit and [7] = 1 selects two stop bits to be transmitted. If Manchester, NRZI, or FM data encoding is selected, only integral stop bit lengths should be used.

[3] Transmitter Request-to-Send Control — This bit controls the deactivation of the RTSN output by the transmitter (see Detailed Operation).

0 RTSN is not affected by status of transmitter.

1 RTSN changes state as a function of transmitter status.

[2] Clear-to-Send Enable Transmitter — The state of this bit determines if the CTSN input controls the operation of the channel's transmitter (see Detailed Operation). The duration of CTS level change is described in the discussion of ICTSR[4].

0 CTSN has no affect on the transmitter.

1 CTSN affects the state of the transmitter.

[1:0] Transmitted Bits per Character — This field selects the number of data bits per character to be transmitted. The character length does not includes the start, parity, and stop bits in ASYNC or the parity bit in COP. In BOP modes the character length for the address and control field is always 8 bits, and the value of this field only applies to the information (I) field, except for the last character of the I field, whose length is specified by OMR[7:5].

Transmitter Timing Register (TTRA, TTRB)

[7] External Source — This bit selects the RTxC pin or the TRxC pin of the channel as the transmitter clock input when [6:4] specifies external. When used for input, the selected pin must be programmed as an input in the PCR [4:3] or [2:0].

0 External input form RTxC pin.

1 External input from TRxC pin.

[6:4] Transmitter Clock Select — This field selects the clock for the transmitter.

000 External clock from TRxC or RTXC at 1X the shift (baud) rate.

001 External clock from TRXC or RTxC at 16X the shift rate.

010 Internal clock from the phase-locked loop at 1X the bit rate. It should be used only in half-duplex operation since the DPLL will periodically resync itself to the received data if in full-duplex operation.

011 Internal clock from the bit rate generator at 32X the shift rate. The clock signal is divided by two before use in the transmitter which operates at 16X the baud rate. Rate selected by [3:0].

100 Internal clock from counter/timer of other channel. The C/T should be programmed to produce a clock at 2X the shift rate.

101 Internal clock from counter/timer of other channel. The C/T should be programmed to produce a clock at 32X the shift rate.

110 Internal clock from the counter/timer of own channel. The C/T should be programmed to produce a clock at 2X the shift rate.

111 Internal clock from the counter/timer of own channel. The C/T should be programmed to produce a clock at 32X the shift rate.

[3:0] Bit Rate Select — This field selects an output from the bit rate generator to be used by the transmitter circuits. The actual frequency output from the BRG is 32X the bit rate shown in Table 5. With a crystal or external clock of 14.7456MHz the bit rates are as given in Table 5 (this input is divided by two before being applied to the oscillator circuit).

Table 5. Receiver/Transmitter Baud Rates

[3:0]	BIT RATE	[3:0]	BIT RATE
0000	50	1000	1050
0001	75	1001	1200
0010	110	1010	2000
0011	134.5	1011	2400
0100	150	1100	4800
0101	200	1101	9600
0110	300	1110	19.2K
0111	600	1111	38.4K

Receiver Parameter Resgister (RPRA, RPRB)

[7] SYN Stripping — This bit controls the DUSCC processing in COP modes of SYN 'character patterns' that occur after the initial character synchronization. Refer to Detailed Operation of the receiver for details and definition of SYN 'patterns', and their accumulation of FCS.

0 Strip only leading SYN 'patterns' (i.e. before a message).

1 Strip all SYN 'patterns' (including all odd DLE's in BISYNC transparent mode).

[6] Transfer Received FCS to FIFO — In BISYNC and BOP modes, the assertion of this bit causes the received FCS to be loaded into the RxFIFO. When this bit is set, BOP mode operates correctly only if a minimum of two extra FLAGs (without shared zeros) are appended to the frame. If the FCS is specified to be transferred to the FIFO, the EOM status bit will be tagged onto the last byte of the FCS instead of to the last character of the message.

0 Do not transfer FCS to RxFIFO.

1 Transfer FCS to RxFIFO.

[5] Auto-Hunt and Pad Check (BISYNC) — In BISYNC mode, the assertion of this bit causes the receiver to go into hunt for character sync mode after detecting certain End-Of-Message (EOM) characters. These are defined in the Detailed Operations section for COP receiver operation. After the EOT and NAK sequences, the receiver also does a check for a closing PAD of four 1s.

0 Disable auto-hunt and PAD check.

1 Enable auto-hunt and PAD check.

[5] Overrun Mode (BOP) — The state of this control bit determines the operation of the receiver in the event of a data overrun, i.e., when a character is received while the RxFIFO and the Rx shift register are both full.

0 The receiver terminates receiving the current frame and goes into hunt phase, looking for a FLAG to be received.

1 The receiver continues receiving the current frame. The overrunning character is lost. (The five characters already assembled in the RxFIFO and Rx shift register are protected).

[4] Receiver Request-to-Send Control (ASYNC) — See Detailed Operation.

0 Receiver does not control RTSN output.

1 Receiver can negate RTSN output.

[4] External Sync (COP) — In COP single SYN mode, the assertion of this bit enables external character synchronization and receipt of SYN patterns is not required. In order to use this feature, the DUSCC must be programmed to COP single SYN mode, CMR 1[2:0] = 110, which is used to set up the internal data paths. In all other respects, however, the external sync mode operation is protocol transparent. A negative signal on the DCDN/SYNIN pin will cause the receiver to establish synchronization on the next rising

edge of the receiver clock. Character assembly will start at this edge with the RxD input pin considered to have the second bit of data. The sync signal can then be negated. Receipt of the Active-High external sync input causes the SYN detect status bit (RSR[2]) to be set and the SYNBOUTN pin to be asserted for one bit time. When this mode is enable, the internal SYN (COP mode) detection and special character recognition (e.g., IDLE, STX, ETX, etc.) circuits are disabled. Character assembly begins as if in the I-field with character length as programmed in RPR[1:)]. Incoming COP frames with parity specified optionally can have it stripped by programming RPR[3]. The user must wait at least eight bit times after Rx is enabled before applying the SYNIN signal. This time is required to flush the internal data paths. The receiver remains in this mode and further external sync pulses are ignored until the receiver is disabled and then reenabled to resynchronize or to return to normal mode. See Figure 2.

0 External sync not enabled.

1 External sync enabled.

Note that EXT SYNC and DCD ENABLE Rx cannot be asserted simultaneously since they use the same pin.

[3] Strip Parity — In COP and ASYNC modes with parity enabled, this bit controls whether the received parity bit is stripped from the data placed in the receiver FIFO. It is valid ony for programmed character lengths of 5, 6, and 7 bits. If the bit is stripped, the corresponding bit in the received data is set to zero.

0 Transfer parity bit as received.

1 Stop parity bit from data.

[3] All Parties Address — In BOP secondary modes, the assertion of this bit causes the receiver to 'wake-up' upon receipt of the address H'FF' or H'FF, FF', for single- and dual-octet address modes, respectively, in addition to its normal station address. This feature allows all stations to receive a message.

0 Don't recognize all parties address.

1 Recognize all parties address.

[2] DCD Enable Receiver — If this bit is asserted, the DCDN/SYNIN input must be Low in order for the receiver to operate. If the input is negated (goes High) while a character is being received, the receiver terminates receipt of the current message (this action in effect disables the receiver). If DCD is subsequently asserted, the receiver will search for the start bit, SYN pattern, or FLAG, depending on the channel protocol. (Note that the change of input can be programmed to generate an interrupt; the duration of the DCD level change is described in the discussion of the input and counter/timer status register (CTSR[5]).

0 DCD not used to enabled receiver.

1 DCD used to enabled receiver.

EXT SYNC and DCD ENABLE Rx cannot be asserted simultaneously since they use the same pin.

[1:0] Received Bits per Character — This field selects the number of data bits per character to be assembled by the receiver. The character length does not include the start, parity, and stop bits in the ASYNC or the parity bit in COP. In BOP modes, the character length for the address and control field is always 8 bits, and the value of this field only applies to the information field. If the number of bits assembled for the last character of the I-field is less than the value programmed in this field, RCL not zero (RSR[0]) is asserted and the actual number of bits received is given in TRSR[2:0].

Receiver Timing Register (RTRA, RTRB)

[7] External Source — This bit selects the RTxC pin or the TRxC pin of the channel as the receiver or DPLL clock input, when [6:4] specifies external. When used for input, the selected pin must be programmed as an input in the PCR [4:3] or [2:0].

0 External input form RTxC pin.

1 External input form TRxC pin.

[6:4] Receiver Clock Select — This field selects the clock for the receiver.

000 External clock from TRxC or RTxC at 1X the shift (baud) rate.

001 External clock fromTRxC or RTxC at 16X the shift rate. Used for ASYNC mode only.

010 Internal clock from the bit rate generator at 32X the shift rate. Clock is divided by two before used by the receiver logic, which operates at 16X the baud rate. Rate selected by [3:0]. Used for ASYNC mode only.

011 Internal clock from counter/timer of own channel. The C/T should be programmed to produce a clock at 32X the shift rate. Clock is divided by two before use in the receiver logic. Used for ASYNC mode only.

100 Internal clock from the digital phase- locked loop. The clock for the DPLL is a 64X clock from the crystal oscillator or system clock input. (The input to the oscillator is divided by two).

101 Internal clock from the digital phase- locked loop. The clock for the DPLL is an external 32X clock from the RTxC or TRxC pin, as selected by [7].

110 Internal clock from the digital phase- locked loop. The clock for the DPLL is a 32X clock from the BRG. The frequency is programmed by [3:0].

111 Internal clock from the digital phase- locked loop. The clock for the DPLL is a 32X clock from the counter/timer of the channel.

[3:0] Bit Rate Select — This field selects an output from the bit rate generator to be used by the receiver circuits. The actual frequency output from the BRG is 32X the bit rate shown in Table 5.

Output and Miscellaneous Register (OMRA, OMRB)

[7:5] Transmitted Residual Character Length — In BOP modes, this field determines the number of bits transmitted for the last character in the information field. This length applies to:

- The character in the transmit FIFO accompanied by the FIFOed TEOM command.
- The character loaded into the FIFO by the DMA controller if DONEN is simultaneously asserted and TPR[4} is asserted.
- The character loaded into the FIFO which causes the counter to reach zero count when TPR[4] is asserted.

The length of all other characters in the frame's information field is selected by TPR[1:0]. If this field is 111, the number of bits in the last character is the same as programmed in TPR[1:0].

[4] TxRDY Activate Mode —

0 FIFO not full. The channel's TxRDY status bit is asserted each time a character is transferred from the transmit FIFO to the transmit shift register. If not reset by the CPU, TxRDY remains asserted until the FIFO is full, at which time it is automatically negated.

1 FIFO empty. The channel's TxRDY status bit is asserted when a character transfer from the transmit FIFO to the

transmit shift register causes the FIFO to become empty. If not reset by the CPU, TxRDY remains asserted until the FIFO is full, at which time it is negated.

If the TxRDY status bit is reset by the CPU, it will remain negated regardless of the current state of the transmit FIFO, until it is asserted again due to the occurrence of one of the above conditions.

[3] RxRDY Activate Mode —

0 FIFO not empty. The channel's RxRDY status bit is asserted each time a character is transferred from the receive shift register to the receive FIFO. If not reset by the CPU, RxRDY remains asserted until the receive FIFO is empty, at which time it is automatically negated.

1 FIFO full. The channel's RxRDY status bit is asserted when a character transfer from the receive shift register to the receive FIFO causes the FIFO to become full. If not reset by the CPU, RxRDY reamins asserted until the FIFO is empty, at which time it is negated.

The RxRDY status bit will also be asserted, regardless of the receiver FIFO full condition, when an end-of-message character is loaded in the RxFIFO (BOP/BISYNC), when a BREAK condition (ASYNC mode) is detected in RSR[2], or when the counter/timer is programmed to count received characters and the character which causes it to reach zero is loaded in the FIFO (all modes). (Refer to the Detailed Operation of the receiver.)

If reset by the CPU, the RxRDY status bit will remain negated, regardless of the current state of the receiver FIFO, until it is asserted again due to one of the above conditions.

[2] General Purpose Output 2 — This general purpose bit is used to control the TxDRQN/GPO2/RTSN pin, when it is used as an output. The output is High when the bit is a 0 and is Low when the bit is a 1.

[1] General Purpose Output 1 — This bit is used to control the RTxDRQN/GPO1N output, which is a general purpose output when the channel is not in DMA mode. The output is High when the bit is a 0 and is Low when the bit is a 1.

[0] Request-to-Send Output — This bit controls the TxDRQN/GPO2N/RTSN and SYNOUTN/RTSN pin, when either is used as a RTS output. The output is High when the bit is a 0 and is Low when the bit is a 1.

Counter/Timer Control and Value Registers

There are five registers in this set consisting of the following:

1. Counter/timer control register (CTCRA/B).
2. Counter/timer preset Highland Low registers (CTPRHA/B, CTPRLA/B).
3. Counter/timer (current value) High and Low registers (CTHA/B, CTLA/B)

The format of each of the registers of this set is contained in Table 6. The control register contains the operational information for the counter/timer. The preset registers contain the count which is loaded into the counter/timer circuits. The third group contains the current value of the counter/timer as it operates.

Counter/Timer Control Register (CTCRA/CTCRB)

[7] Zero Detect Interrupt — This bit determines whether the assertion of the C/T ZERO COUNT status bit (ICTSR[6]) causes an interrupt to be generated.

0 Interrupt disabled.

1 Interrupt enabled if master interrupt enabled (ICR[1] or ICR[0]) is asserted.

[6] Zero Detect Control — This bit determines the action of the counter upon reaching zero count.

0 The counter/timer is preset to the value contained in the counter/timer preset registers (CTPRL, CTPRH) at the next clock edge.

1 The counter/timer continues counting without preset. The value at the next clock edge will be H'FFFF'.

[5] Counter/Timer Output Control — This bit selects the output waveform when the counter/timer is selected to be output on TRxC or RTxC.

1 The output is a single clock positive width pulse each time the C/T reaches zero count. (The duration of this pulse is one clock period.)

0 The output toggles each time the C/T reaches zero count. The output is cleared to Low by either of the preset counter/timer commands.

[4:3] Clock Select — This field selects whether the clock selected by [2:0] is prescaled prior to being applied to the input of the C/T.

00 No prescaling.

01 Divide clock by 16.

10 Divide clock by 32.

11 Divide clock by 64.

[2:0] Clock Source — This field selects the clock source for the counter/timer.

000 RTxC pin. Pin must be programmed as input.

001 TRxC pin. Pin must be programmed as input.

010 Source is the crystal oscillator or system clock input divided by four.

011 This selects a special mode of operation. In this mode the counter, after receiving the 'start C/T' command, delays the start of counting until the RxD input goes Low. It continues counting until the RxD input goes High, then stops and sets the C/T zero count status bit. The CPU can use the value in the C/T to determine the bit rate of the incoming data. The clock is the crystal oscillator or system clock input divided by four.

100 Source is the 32X BRG output selected by RTR[3:0] of own channel.

101 Source is the 32X BRG output selected by TTR[3:0] of own channel.

110 Source is the internal signal which loads received characters from the receive shift register into the receiver FIFO. When operating in this mode, the FIFOed EOM status bit (RSR[7]) shall be set when the character which causes the count to go to zero is loaded into the receive FIFO.

111 Source is the internal signal which transfers characters from the data bus into the transmit FIFO. When operating in this mode, and if the TEOM on zero count or done control bit (TPR[4]) is asserted, the FIFOed send EOM command will be automatically asserted when the character which causes the count to go to zero is loaded into the transmit FIFO.

Table 6. Counter/Timer Control and Value Register Bit Formats

COUNTER/TIMER CONTROL REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CTCRA, CTCRB)	Zero Detect Interrupt	Zero Detect Control	Output Control	Prescaler		Clock Source		
	0 — disable 1 — enabled	0 — preset 1 — continue	0 — square 1 — pulse	00 — 1 01 — 16 10 — 32 11 — 64		000 — RTxC pin 001 — TRxC pin 010 — X1/CLK divided by 4 011 — X1/CLK divided by 4 gated by RxD 100 — Rx BRG 101 — Tx BRG 110 — Rx characters 111 — Tx characters		

COUNTER/TIMER PRESET REGISTER HIGH

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CTPRHA, CTPRHB)	Most significant bits of counter/timer preset value.							

COUNTER/TIMER PRESET REGISTER LOW

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CTPRLA, CTPRLB)	Least significant bits of counter/timer preset value.							

COUNTER/TIMER REGISTER HIGH

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CTHA, CTHB)	Most significant bits of counter/timer.							

COUNTER/TIMER REGISTER LOW

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CTLA, CTLB)	Least significant bits of counter/timer.							

Counter/Timer Preset High Register (CTPRHA, CTPRHB)

[7:0] MSB — This regsiter contains the eight most significant bits of the value loaded into the counter/timer upon receipt of the load C/T from preset regsiter command or when the counter/timer reaches zero count and the zero detect control bit (CTCR[6]) is negated. The minimum 16-bit counter/timer preset value is H'0002'.

Counter/Timer Preset Low Register (CTPRLA, CTPRLB)

[7:0] LSB — This register contains the eight least significant bits of the value loaded into the counter/timer upon receipt of the load C/T from preset register command or when the counter/timer reaches zero count and the zero detect control bit (CTCR[6]) is negated. The minimum 16-bit counter/timer preset value is H'0002'.

Counter/Timer High Register (CTHA, CTHB)

[7:0] MSB — A read of this 'register' provides the eight most significant bits of the current value of the counter/timer. It is recommended that the C/T be stopped via a stop counter command before it is read in order to prevent errors which may occur due to the read being performed while the C/T is changing. This count may be continued after the register is read.

Counter/Timer Low Register (CTLA, CTLB)

[7:0] LSB — A read of this 'register' provides the eight least significant bits of the current value of the counter/timer. It is recommended that the C/T be stopped via a stop counter command before it is read, in order to prevent errors which may occur due to the read being performed while the C/T is changing. This count may be continued after the register is read.

Interrupt Control and Status Registers

This group of registers define mechanisms for communications between the DUSCC and the processor and contain the device status information. Four registers, available for each channel, and four common device registers comprise this group which consists of the following:

1. Interrupt Enable Register (IERA/B).
2. Receiver Status Register (RSRA/B).
3. Transmitter and Receiver Status Register (TRSRA/B).
4. Input and Coutner/Timer Status Register (ICTSRA/B).
5. Interrupt Vector Register (IVR) and Modified Interrupt Vector Register (IVRM).
6. Interrupt control register (ICR).
7. General status register (GSR)

See Table 7 for bit formats and Figure 3 for table relationships.

Interrupt Enable Register (IERA, IERB)

This register controls whether the assertion of bits in the channel's status registers causes an interrupt to be generated. An additional condition for an interrupt to be generated is that the channel's master interrupt enabled bit, ICR[0] or ICR[1], be asserted.

[7] DCD/CTS —

0 Interrupt not enabled.

1 Interrupt generated if ICTSR[4] or ICTSR[5] are asserted.

[6] TxRDY —

0 Interrupt not enabled.

1 Interrupt generated if TxRDY (GSR[1] or GSR[5] for Channels A and B, respectively) is asserted.

[5] TRSR 73 —

0 Interrupt not enabled.

1 Interrupt generated if bits 7, 6, 5, 4 or 3 of the TRSR are asserted.

[4] RxRDY —

0 Interrupt not enabled.

1 Interrupt generated if RxRDY (GSR[0] or GSR[4] for Channels A and B, respectively) is asserted.

[3] RSR 76 —

0 Interrupt not enabled.

1 Interrupt generated if bits 7 or 6 of the RSR are asserted.

[2] RSR 54 —

0 Interrupt not enabled.

1 Interrupt generated if bits 5 or 4 of the RSR are asserted.

[1] RSR 32 —

0 Interrupt not enabled.

1 Interrupt generated if bits 3 or 2 of the RSR are asserted.

[0] RSR 10 —

0 Interrupt not enabled.

1 Interrupt generated if bits 1 or 0 of the RSR are asserted.

Table 7. Interrupt Control and Status Register Bit Format

RECEIVER STATUS REGISTER

	*BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(RSRA, RSRB) ASYNC	# Char compare	RTS negated	Overrun error	not used	BRK end detect	BRK start detect	# Framing error	# Parity error
COP	# EOM detect +	PAD error +	Overrun error	not used	not used	Syn detect	# CRC error	# Parity error
BOP	# EOM detect	Abort detect	Overrun error	Short frame detect	Idle detect	Flag detect	# CRC error	# RCL not zero
LOOP	# EOM detect	Abort/EOP detect	Overrun error	Short frame detect	Turn-around detect	Flag detect	# CRC error	# RCL not zero

NOTES:
Status bit is FIFOed.
+ COP BISYNC mode only
* All modes indicate character count complete.

TRANSMITTER AND RECEIVER STATUS REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(TRSRA, TRSRB) ASYNC	Transmitter underrun	CTS underrun	not used	Send break ack	DPLL error	not used	not used	not used
COP	Transmitter underrun	CTS underrun	Frame complete	Send SOM ack	DPLL error	not used	Rx hunt mode	Rx xpnt mode
BOP	Transmitter underrun	CTS underrun / Loop sending*	Frame complete	Send SOM/ abort ack	DPLL error	Rx Residual Character Length: 000 — 0 bit, 001 — 1 bits, 010 — 2 bits, 011 — 3 bits, 100 — 4 bits, 101 — 5 bits, 110 — 6 bits, 111 — 7 bits		

NOTE:
* Loop mode only.

INPUT AND COUNTER/TIMER STATUS REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(ICTSRA, ICTSRB)	C/T running	C/T zero count	Delta DCD	Delta CTS/LC	DCD	CTS/LC	GPI2	GPI1

Table 7. Interrupt Control and Status Register Bit Format (Continued)

INTERRUPT ENABLE REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(IERA, IERB)	DCD/CTS	TxRDY	TRSR [7:3]	RxRDY	RSR[7:6]	RSR [5:4]	RSR [3:2]	RSR [1:0]
	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes

INTERRUPT VECTOR REGISTER AND INTERRUPT VECTOR MODIFIED REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(IVR, IVRM)	8-bit interrupt vector							

GENERAL STATUS REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(GSR)	Channel B				Channel A			
	External or C/T Status	Rx/Tx status	TxRDY	RxRDY	External or C/T status	Rx/Tx status	TxRDY	RxRDY

INTERRUPT CONTROL REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(ICR)	Channel A/B Interrupt Priority		Vector Mode		Bits to Modify	Vector Includes Status	Channel A Master Int Enable	Channel B Master Int Enable
	00 — Channel A 01 — Channel B 10 — interleaved A 11 — interleaved B		00 — vectored 01 — vectored 10 — vectored 11 — non vectored		0 — 2:0 1 — 4:2	0 — no 1 — yes	0 — no 1 — yes	0 — no 1 — yes

Receiver Status Register (RSRA, RSRB)

This register informs the CPU of receiver status. Bits indicated as 'not used' in a particular mode will read as zero. The logical OR of these bits is presented in GSR[2] or GSR[6] (ORed with the bits of TRSR) for Channels A and B, respectively. Unless otherwise indicated, asserted status bits are reset only be performing a write operation to the status register with the bits to be reset being ones in the accompanying data word, or when the RESETN input is asserted, or when a 'reset receiver' command is issued.

Certain status bits are specified as being FIFOed. This means that they occupy positions in a status FIFO that correspond to the data FIFO. As the data is brought to the top of the FIFO (the position read when the RxFIFO is read), the FIFOed status bits are logically ORed with the previous contents of the corresponding bits in the status register. This permits the user to obtain status either character by character or on a block basis. For character by character status, the SR bits should be read and then cleared before reading the character data from RxFIFO. For block status, the status register is initially cleared and then read after the message is received. Asserted status bits can be programmed to generate an interrupt (see Interrupt Enable Register).

[7] Character Count Complete (All Modes), Character compare (ASYNC), EOM (BISYNC/BOP/LOOP) — If the counter/timer is programmed to count received characters, this bit is asserted when the character which causes the count to go to zero is loaded into the receive FIFO. It is also asserted to indicate the following conditions:

ASYNC The character currently at the top of RxFIFO matched the contents of S1R. A character will not compare if it is received with parity error even if the data portion matches.

BISYNCThe character currently at the top of the FIFO was either a text message terminator or a control sequence received outside of a text or header field. See Detailed Operation of COP Receiver. If transfer FCS to FIFO (RPR[6]) is set, the EOM will instead be tagged onto the last byte of the FCS. Note that if an overrun occurs during receipt of a message, the EOM character may be lost, but this status bit will still be asserted to indicate that an EOM was received. For 2 byte EOM comparisons, only the second byte is tagged (assuming the CRC is not transferred to the FIFO).

BOP, The character currently at the top LOOP of the FIFO was the last character of the frame. If trnasfer FCS to FIFO (RPR[6]) is asserted, the EOM will be tagged instead onto the last byte of the FCS. Note that if an overrun occurs, the EOM character may be lost, but this status bit will still be asserted to indicate that an EOM was received. This bit will not be set when an abort is received.

[6] RTS Negated (ASYNC), PAD Error (BISYNC), ABORT (BOP) —

ASYNC The RTSN output was negated due to receiving the start bit of a new character while the RxFIFO was full (see RPR[4]).

BISYNC PAD error detected (see RPR[5]). LOOP
An ABORT sequence consisting of a zero followed by seven ones was received after receipt of the first address octet but before receipt of the closing FLAG. The user should read RxFIFO until it is empty and determine if any valid characters from a previous frame are in the FIFO. If no character with a tagged EOM detect ([7]) is found, all characters are from the current frame and should be discarded along with any previously read by the CPU. An ABORT detect causes the receiver to automatically go into search for FLAG state. An

abort during a valid frame does not cause the CRC to reset; this will occur when the next frame begins.

LOOP Performs the ABORT detect function as described for BOP without the restriction that the pattern be detected during an active frame. A zero followed by seven ones is the end-of-poll sequence which allows the transmitter to go active if the 'go active on poll' command has been invoked.

[5] Overrun Error (All Modes) — A new character was received while the receive FIFO was full and a character was already waiting in the receive shift register to be transferred to the FIFO. the DUSCC protects the five characters previously assembled (four in RxFIFO, one in the Rx shift register) and discards the overrunning character(s). After the CPU reads the FIFO, the character waiting in the RxSR will be loaded into the available FIFO position. This releases the RxSR and a new character assembly will start at the next character boundary. In this way, only valid characters will be assembled, i.e., no partial character assembly will occur regardless of when the RxSR became available during the incoming data stream.

[4] Short Frame (BOP/LOOP) —

ASYNC Not used

COP Not used

BOP, A closing flag was received with LOOP missing fields in the frame. See detailed operation for BOP receiver.

[3] BREAK End Detect (ASYNC), IDLE (BOP), Turnaround (LOOP) —

ASYNC 1X clock mode: The RxD input has returned to the marking state for at least one period of the 1X receiver clock after detecting a BREAK.
16X clock mode: The RxD input has returned to the marking (High) state for a least one-half bit time after detecting a BREAK. A half-bit time is defined as eight clock cycles of the 16X receiver clock.

COP Not used.

BOP An IDLE sequence consisting of a zero followed by fifteen ones was received. During a valid frame, an abort must precede an idle. However, outside of a valid frame, an idle is recognized and abort is not.

LOOP A turnaround sequence consisting of eight contiguous zeros was detected outside of an active frame. This should normally be used to terminate transmitter operation and return the system to the 'echoing RxD' mode.

[2] BREAK Start Detect (ASYNC), SYN Detect (COP), FLAG Detect (BOP/LOOP) —

ASYNC An all zero character, including parity (if specified) and first stop bit, was received. The receiver shall be capable of detecting breaks which begin in the middle of a previous character. Only a single all-zero character shall be put into the FIFO when a break is detected. Additional entries to the FIFO are inhibited until the end of break has been detected (see above) and a new character is received.

COP A SYN pattern was received. Refer to Detailed Operation for definition of SYN patterns. Set one bit time after detection of SYN pattern in HSRH, HSRL. See Figure 1 for receiver data path.

BOP, A FLAG frequency (01111110) was LOOP received. Set one bit time after FLAG is detected in CCSR. See Figure 1 for receiver data path.

[1] Framing Error (ASYNC), CRC Error (COP/BOP/LOOP) —

ASYNC At the first stop bit position the RxD input was in the Low (space) state. The receiver only checks for framing error at the nominal center of the first stop bit regardless of the number of stop bits programmed in TPR[7:4]. This bit is not set for BREAKS.

COP In BISYNC COP mode, this bit is set upon receipt of the BCC byte(s), if any, to indicate that the received BCC was in error. The bit is normally FIFOed with the last byte of the frame (the character preceding the first BCC byte). However, if transfer FCS to FIFO (RPR[6]) is asserted, this bit is FIFOed with the last BCC byte. The value of this bit should be ignored for non-test messages or if the received frame was aborted via an ENQ. In non-BISYNC COP modes, the bit is set with each received character if the current value of the CRC checker is not equal to the non-error value (see CMR2[2:0]).

BOP This bit is set upon receipt of the LOOP FCS byte(s), if any, to indicate that the received FCS was in error. The bit is normally FIFOed with the last byte of the I field (the character preceding the first FCS byte). However, if transfer FCS to FIFO (RPR[6]) is asserted, this bit is FIFOed with the last FCS byte.

[0] Parity Error (ASYNC/COP), RCL Not Zero (BOP/LOOP) —

ASYNC The parity bit of the received character was not as expected. A parity error does not affect the parity bit put into the FIFO as part of the character when strip parity (RPR[3]) is negated.

COP The parity bit of the received character was not as expected. A parity error does not affect the parity bit put into the FIFO as part of the character when strip parity (RPR[3]) is negated. A SYN or other character received with parity error is treated as a data character. Thus, a SYN with parity error received while in SYN search state will not establish character sync. Characters received with parity error while in the SYN search state will not set the error bit.

BOP The last character of the I field did not LOOP have the character length specified in RPR[1:0]. The actual received character length of this byte can be read in TRSR[2:0]. This bit is FIFOed with the EOM character but TRSR[2:0] is not. An exception occurs if the command to transfer the FCS to the FIFO is active. In this case, the bit will be FIFOed with the last byte of the FCS, i.e., with REOM. In the event that residual characters from two consecutive frames are received and are both in the FIFO, the length in TRSR[2:0] applies to the last received residual character.

Transmitter/Receiver Status Register (TRSRA, TRSRB)

This register informs the CPU of transmitter and receiver status. Bits indicated as not used in a paritcular mode will read as zero, except for bits [2:0], which may not be zero. The logical-OR of bits [7:3] is presented in GSR[2] or GSR[6] (ORed with the bits of RSR) for channels A and B, respectively. Unless otherwise indicated, asserted status bits are reset only:

1. By performing a write operation to the status register with the bits to be reset being ones in the accompanying data word [7:3].
2. When the RESETN input is asserted.
3. For [7:4], when a 'reset transmitter' command is issued.
4. For [3:0], when a 'reset receiver' command is issued.
5. For [2:0], see description in BOP mode.

Asserted status bits in [7:3] can be programmed to generate an interrupt. See IER.

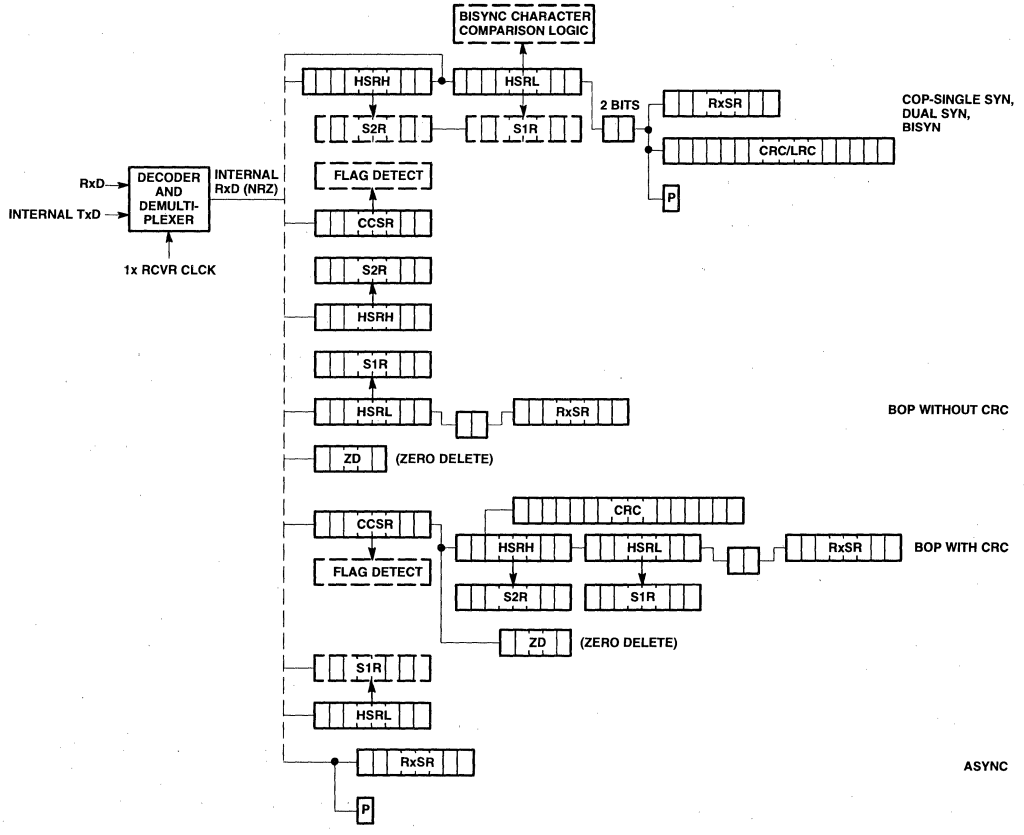


Figure 1. Receiver Data Path

[7] Transmitter Underrun — Indicates that the transmit shift register has completed serializing a character and found no other character to serialize in the TxFIFO. The bit is not set until at least one character from the transmit FIFO (not including PAD characters in synchronous modes) has been serialized. The transmitter action after transmitter empty depends on operating mode:

ASYNC The TxD output is held in the MARK state until another character is loaded into the TxFIFO. Normal operation then continues.

COP Action is specified by TPR[7:6].

BOP, LOOP Action is specified by TPR[7:6].

[6] CTS Underrun (ASYNC/COP/BOP), Loop sending (LOOP) —

ASYNC, COP, BOP This bit is set only if CTS enable Tx (TPR[2]) is asserted. It indicates that the transmit shift register was ready to begin serializing a character and found the CTSN input negated. In ASYNC mode, this bit will be reasserted if cleared by the CPU while the CTSN input is negated.

LOOP Asserted when the go active on poll command has been invoked and an EOP sequence has been invoked and an EOP sequence has been detected, causing the transmitter to go active by changing the EOP to a FLAG (see Detailed Operation of transmitter).

[5] Frame Complete (COP/BOP) —

ASYNC Not used.

COP Asserted at the beginning of transmission of the end of message sequence invoked by which is either a TEOM command, or when TPR[4] = 1, or TPR[7:6] = 00. The CPU can invoke the TSOM command after this bit is set to control the number of SYNs between transmitted frames.

BOP Asserted at the beginning of transmission of the end of message sequence which is invoked by either a TEOM command, or when TPR[4] = 1, or TPR[7:6] = 00. The CPU can invoke the TSOM command after this bit is set to control the number of FLAGs between transmitted frames. In COP/BOP modes, the frame complete status bit is set during the next-to-last bit (on TxD pin) of the last character in the data/information field. In BOP mode, if a 1-bit residual character is selected through OMR[7:5], then this

bit is set during the next-to-last bit (on TxD pin) of the last full length character of the information field.

[4] Send Break Ack (ASYNC)/Send SOM ACK (COP)/Send SOM-Abort Ack (BOP —

ASYNC Set when the transmitter begins transmission of a break in response to the send break command. If the command is reinvoked, the bit will be set again at the beginning of the next character time. The user can control the length of the break by counting character times through this mechanism.

COP Set when the transmitter begins transmission of a SYN pattern in response to the TSOM or TSOMP command. If the command is reinvoked, the bit will be set again at the beginning of the next transmitted SYN pattern. The user can control the number of SYNs which are sent through this mechanism.

BOP Set when the transmitter begins transmission of a FLAG/ABORT in response to the TSOM or TSOMP or TABRK command. If the command is reinvoked, the bit will be set again at the beginning of the next transmitted FLAG/ABORT. The user can control the number of FLAGs/ABORTs which are sent through this mechanism.

[3] DPLL Error — Set while the DPLL is operating in FM mode to indicate that a data transition was not detected within the detection window for two consecutive bits and that the DPLL was forced into search mode. This feature is disabled when the DPLL is specified as the clock source for the transmitter via TTR[6:4].

[2:0] Received Residual Character Length (BOP) —

BOP This field should be examined to determine the length of the last character of the I field (character tagged with REOM status bit) if RSR[0] is set to indicate that the length was not equal to the character length specified in RPR[1:0]. This field is negated when a reset receiver or disabled receiver command is issued, or when the first control character for the next frame of data is in HSRL (see Figure 1). Care must be taken to read TRSR[2:0] before these bits are cleared.

[1] Receiver in Hunt Mode (COP) —

COP This bit is asserted after the receiver is reset or disabled. It indicates that the receiver is in the hunt mode, searching the data stream for a SYN sequence to establish character synchronization. The bit is negated automatically when character sync is achieved.

[0] Receiver in Transparent Mode (BISYNC) —

COP Indicates that a DLE-STX sequence was received and the receiver is operating in BISYNC transparent mode. Set two bit times after detection of STX in HSRL. See Figure 1 for receiver data path. Transparent mode operation is terminated and the bit is negated automatically when one of the terminators for transparent text mode is received (DLE-ETX/ETB/ITB/ENQ).

Input and Counter/Timer Status Register (ICTSRA, ICTSRB)

This register informs the CPU of status of the counter/timer and inputs. The logical-OR of bits [6:4] is presented in GSR[3] or GSR[7] for Channels A and B, respectively. Unless otherwise specified, bits of this register are reset only:

1. By performing a write operation to the status register with the bits to be reset (ones in the accompanying data word for bits [6:4] only).
2. When the RESETN input is asserted (bits [7:4]) only.

[7] Counter/Timing Running — Set when the C/T is started by start C/T command and reset when it is stopped by a stop C/T command.

[6] Counter/Timer Zero Detect — Set when the counter/timer reaches zero count, or when the bit length measurement is enabled (CTCR [2:0] = 011) and the RxD input has returned High. The assertion of this bit causes an interrupt to be generated if ICTCR[7] and the channel's master interrupt enable (ICR[1] or ICR[0]) are asserted.

[5] Delta DCD — The DCD input is sampled approximately every 6.8µs using the 32X, 4800 baud output from the BRG. After synchronizing with the sampling clock, at least two consecutive samples at the same level are required to establish the level. As a consequence, a change of state at the DCD input, lasting at least 17µs, will set this bit. The reset circuitry initializes the sampling circuits so that a change is not falsely indicated at power on time. The assertion of this bit causes an interrupt to be generated if IER[7] and the channel's master interrupt enable (ICR[1] or ICR[0]) are asserted.

[4] Delta CTS/LC — When not in loop mode, the CTS input is sampled approximately every 6.8µs using the 32X, 4800 baud output form the BRG. After synchronizing with the sampling clock, at least two consecutive samples at the same level are required to establish the level. As a consequence, a change of state at the CTS input, lasting at least 17µs, will set this bit. The reset circuitry initializes the sampling circuits so that a change is not falsely indicated at power on time. The assertion of this bit causes an interrupt to be generated if IER[7] and the channel's master interrupt enable (ICR[1] or ICR[0]) are asserted.

In SDLC loop mode, this bit is set upon transitions of the LC output. LC is asserted in response to the 'go on-loop' command when the receiver detects a zero followed by seven ones, and negated in response to the 'go off-loop' command when the receiver detects a sequence of eight ones.

[3:2] State of DCD and CTS — ICTSRx[3] reflects the state of the DCDxN input pin, while ICTSRx[2] reflects the state of CTSxN. When the bits are 0, the inputs are High, when they are 1, the pins are Low.

[1:0] Current State of GPI2 and GPI1 — These fields provide the current state of the channels general purpose input pins. The bits valve are latched at the beginning of the read cycle.

Interrupt Vector Register (IVR) and Modified Vector Register (IVRM)

[7:0] Register Content — If ICR[2] = 0, the content of IVR register is output on the data bus when the DUSCC has issued an interrupt request and the responding interrupt acknowledge (IACKN) is received. The value in the IVR is initialized to H'0F' on master reset. If 'vector includes status' is specified by ICR[2] = 1, bit [2:0] or [4:2] (depending on ICR[3]), of the vector are modified as shown in Table 9 to indicate the highest priority interrupt currently active. The priority is programmable through the ICR. This modified vector is stored in the IVRM. When ICR[2] = 1, the content of the IVRM is output on to the data bus on the interrupt acknowledge. The vector

is not modified, regardless of the value of ICR[2], if the CPU has not written an initial vector into this register.

Either the modified or unmodified vector can also be read by the CPU via a normal bus read cycle (see Table 1). The vector value is locked at the beginning of the IACK or read cycle until the cycle is completed. If no interrupt is pending, an H'FF' is output when reading the IVRM.

Interrupt Control Register (ICR)

[7:6] Channel A/B Interrupt Priority — Selects the relative priority between Channels A and B. The state of this bit determines the value of the interrupt vector (see Interrupt Vector Register). The priority within each channel, from highest to lowest, is as follows:

0 Receiver ready.

1 Transmitter ready

2 Rx/Tx status.

3 External or C/T status.

00 Channel A has the highest priority. The DUSCC interrupt priorities from highest to lowest are as follows: A(0), A(1), A(2), A(3), B(0), B(1), B(2), B(3).

01 Channel B has the highest priority. the DUSCC interrupt priorities from highest to lowest are as follows: B(0), B(1), B(2), B(3), A(0), A(1), A(2), A(3).

10 Priorities are interleaved between channels, but Channel A has the highest priority between events of equal channel priority. The DUSCC interrupt priorities from highest to lowest are as follows: A(0), B(0), A(1), B(1), A(2), B(2), A(3), B(3)

11 Priorities are interleaved between channels, but Channel B has the highest priority between events of equal channel priority. The DUSCC interrupt priorities from highest to lowest are as follows: B(0), A(0), B(1), A(1), B(2), A(2), B(3), A(3).

Table 8. Interrupt Status Encoding

IVRM [2:0]/ [4:2]	HIGHEST PRIORITY INTERRUPT CONDITION
000	Channel A receiver ready
001	Channel A transmitter ready
010	Channel A Rx/Tx status
011	Channel A external or C/T status
100	Channel B receiver ready
101	Channel B transmitter ready
110	Channel B Rx/Tx status
111	Channel B external or C/T status

[5:4] Vector Mode — The value of this field determines the response of the DUSCC when the interrupt acknowledge (IACKN) is received from the CPU.

00 or 01 or 10 Vectored mode. Upon interrupt acknowledge, the DUSCC locks its current interrupt status until the end of the acknowledge cycle. If it has an active interrupt pending, it responds with the appropriate vector and then asserts DTACKN. If it does not have an interrupt, it propagates the acknowledge through its X2/IDCN output if this function is programmed in PCRA[7]. Otherwise, the IACKN is ignored. Locking the interrupt status at the leading edge of IACKN prevents a device at High position in the interrupt daisy chain from responding to an IACK issued for a lower priority device while the acknowledge is being propagated to that device.

11 Non-vectored mode. The DUSCC ignores an IACK if one is received; the interrupt vector is not placed on the data bus. The internal interrupt status is locked when a read of the IVR or IVRM is performed. Except for the absence of the vector on the bus, the DUSCC performs as it does in vectored mode — the vector is prioritized and modified if programmed.

[3] Vector Bits to Modify — Selects which bits of the vector stored in the IVR are to be modified to indicate the highest priority interrupt pending in the DUSCC. See Interrupt Vector Register.

0 Modify bits 2:0 of the vector.

1 Modify bits 4:2 of the vector.

[2] Vector Includes Status — Selects whether the modified (includes status) (IVRM) or unmodified vector (IVR) is output in response to an interrupt acknowledge (see Interrupt Vector Register).

0 Unmodified vector.

1 Modified vector.

[1] Channel A Master Interrupt Enable —

0 Channel A interrupts are disabled.

1 Channel A interrupts are enabled.

[0] Channel B Master Interrupt Enable —

0 Channel B interrupts are disabled.

1 Channel B interrupts are enabled.

General Status Register (GSR)

This register provides a 'quick look' at the overall status of both channels of the DUSCC. A write to this register with 1s at the corresponding bit positions causes TxRDY (bits 5 and 1) and/or RxRDY (bits 4 and 0) to be reset. The other status bits can be reset only by resetting the individual status bits that they point to.

[7] Channel B External or Coutner/Timer Status — This bit indicates that one of the following status bits is asserted: ICTSRB[6:4].

[6] Channel B Receiver or Transmitter Status — This bit indicates that one of the following status bits is asserted: RSRB[7:)], TRSRB[7:3].

[5] Channel B Transmitter Ready — The assertion of this bit indicates that one or more characters may be loaded into the Channel B transmitter FIFO to be serialized by the transmit shift register. See description of OMR[4]. This bit can be asserted only when the transmitter is enabled. Resetting the transmitter negates TxRDY.

[4] Channel B Receiver Ready — The assertion of this bit indicates that one or more characters are available in the Channel B receiver FIFO to be read by the CPU. See description of OMR[3]. RxRDY is initially reset (negated) by a chip reset or when a 'reset Channel B receiver' command is invoked.

[3] Channel A External or Counter/Timer Status — This bit indicates that one of the following status bits is asserted: ICTSRA[6:4].

[2] Channel A Receiver or Transmitter Status — This bit indicates that one of the following status bits is asserted: RSRA[7:0], TRSRA[7:3].

[1] Channel A Transmitter Ready — The assertion of this bit indicates that one or more characters may be loaded into the Channel A transmitter FIFO to be serialized by the transmit shift register. See description of OMR[4]. This bit can be asserted only when the transmitter is enabled. Resetting the transmitter negates TxRDY.

[0] Channel A Receiver Ready — The assertion of this bit indicates that one or more characters are available in the Channel A receiver FIFO to be read by the CPU. See description of OMR[3]. RxRDY is initially reset (negated) by a chip reset or when a 'reset Channel A receiver' command is invoked.

Channel Command Register (CCRA, CCRB) — Commands to the DUSCC are entered through the channel command register. The format of that register is shown in Table 9. A read of this register returns the last invoked command (with bits 4 and 5 set to 1).

Transmitter Commands

0000 Reset transmitter. Causes the transmitter to cease operation immediately. The transmit FIFO is cleared and the TxD output goes into the marking state. Also clears the transmitter status bits (TRSR[7:4]) and resets the TxRDY status bit (GSR[1] or GSR[5] for Channels A and B, respectively). The counter/timer and other registers are not affected.

0001 Resest transmit CRC. This command is appended to and FIFOed along with the next character loaded into the transmit FIFO. It causes the transmitter CRC generator to be reset to its initial state prior to beginning transmission of the appended character.

0010 Enable transmitter. Enables transmitter operation, conditioned by the state of the CTS ENABLE Tx bit, TPR[2]. Has no effect if invoked when the transmitter has previously been enabled.

0011 Disable transmitter. Terminates transmitter operation and places the TxD output in the marking state at the next occurrence of a transmit FIFO empty condition. All characters currently in the FIFO, or any loaded subsequently prior to attaining an empty condition, will be transmitted.

0100 Transmit start of message. Used in COP and BOP modes to initiate transmission of a frame after the transmitter is first enabled, prior to sending the contents of the FIFO. Can also be used to precisely control the number of SYN/FLAGs at the beginning of transmission or in between frames.

When the transmitter is first enabled, transmission will not begin untill this command (or the transmit SOM with PAD command, see below) is issued. The command causes the SYN (COP) or FLAG (BOP) pattern to be transmitted. SEND SOM ACK (TRSR[4]) is set when transmission of the SYN/FLAG begins. The CPU may then reinvoke the command if multiple SYN/FLAGs are to be transmitted. Transmission of the FIFO characters begin when the command is no longer invoked. If the FIFO is empty, SYN/FLAGs continue to be transmitted until a character is loaded into the FIFO, but the status bit (TRSR[4]) is not set. Insertion of SYN/FLAGs between frames can be accomplished by invoking this command after the frame complete status bit (TRSR[5]) has been asserted in response to transmission of the end-of message sequence.

0101 Transmit start of message with opening PAD. Used in COP and BOP modes after the transmitter is first enabled to send a bit pattern for DPLL synchronization prior to transmitting the opening SYN (COP) or FLAG (BOP). the SYN/FLAG is sent at the next occurrence of a transmit FIFO empty condition. All characters currently in the FIFO, or any loaded subsequently prior to attaining an empty condition, will be transmitted. While the PAD characters are transmitted, the character length is set to 8 bits, (regardless of the programmed length), and parity generation (COP), zero insertion (BOP) and LRC/CRC accumulation are disabled. SEND SOM ACK (TRSR[4]) is set when transmission of the SYN/FLAG begins. The CPU may then invoke the transmit SOM command if multiple SYN/FLAGs are to be transmitted.

The TSOM/TSOMP commands, described above, are sampled by the controller in alternate bit times of the transmitter clock. As a consequence, the first bit time of a COP/BOP frame will be transmitted on the TxD pin, after a maximum of three bit times, after the command is issued. (The additional 1-bit delay in the data path is due to the data encoding logic.)

0110 Transmit end-of-message. This command is appended to the next character loaded into the transmit FIFO. It causes the transmitter to send the end-of message sequence (selected FCS in COP modes, FCS-FLAG in BOP modes) after the appended character is transmitted. Frame complete (TRSR[5]) is set when transmission of the FCS begins. This command is also asserted automatically if the TEOM on zero count or one control bit (TPR[4]) is asserted, and the counter/timer is programmed to count transmitted characters when the character which causes the count to go to zero is loaded into the transmit FIFO. TEOM is not recognized if the transmitter FIFO is full.

0111 Transmit Abort BOP/Transmit Break ASYNC. In BOP modes, causes an abort (eight ones) to be transmitted after transmission of the character currently in the shift register is completed. The transmitter then sends MARKs or FLAGs depending on the state of underrun control (TPR[7:6]). Send SOM/abort ack (TRSR[4]) is set when the transmission of the abort begins. If the command is reasserted before transmission of the previous ABORT is completed, the process will be repeated. This can be used to send the idle sequence. The 'transmit SOM' command must be used to initiate transmission of a new message. In either mode, invoking this command causes the transmit FIFO to be flushed (characters are not transmitted).

In ASYNC mode, causes a break (space) to be transmitted after transmission of the character currently in the shift register is completed. Send break ack (TRSR[4]) is set when the transmission of the break begins. The transmitter keeps track of character times. If the command is reasserted, send break ack will be set again at the beginning of the next character time. The user can use this mechanism to control the length of the break in character time multiples. Transmission of the break is terminated by issuing a 'reset Tx' or 'disableTx' command.

1000 Transmit DLE. Used in COP modes only. This command is appended to and FIFOed with the next character loaded into the transmitter FIFO. It causes the transmitter to send a DLE, (EBCDIC H'10', ASCII H'10') prior to transmitting the appended character. If the transmitter is operating in BISYNC transparent mode, the transmitter control logic automatically causes a second DLE to be transmitted whenever a DLE is detected at the top of the FIFO. In this case, the TDLE command should not be invoked. An extra (third) DLE, however, will not be sent if the transmit DLE command is invoked.

1001 Go active on poll. Used in BOP loop mode only. Causes the transmitter, if it is enabled, to begin sending when an EOP sequence consisting of a zero followed by seven ones is detected. The last one of the EOP is changed to zero, making it another FLAG, and then the transmitter operates as described in the detailed operation section. The loop sending status bit (TRSR[6]) is asserted concurrent with the beginning of transmission.

1010 Reset go active on poll. Clears the stored 'go active on poll' command.

1011 Go on-loop. Used in BOP loop mode to control the assertion of the LCN output. This output provides the means of controlling external loop interface hardware to go on-loop and off-loop. When the command is asserted, the DUSCC will look for the receipt of a zero followed by seven ones, at which time it will assert the LCN output and set the delta DCD/LC status bit (ICTSR[4]). This allows the DUSCC to break into the loop without affecting loop operation. This command must be used to initiate loop mode operation.

1100 Go off-loop. Used in BOP loop mode to control the negation of the LCN output. This output provides the means of controlling external loop interface hardware to go on-loop and off-loop. When the command is asserted, the DUSCc will look for the receipt of eight contiguous ones, at which time it will negate the LCN output and set the delta DCD/LC status bit (ICTSR[4]). This allows the DUSCC to get off the loop operation. This command is normally used to terminate loop mode operation.

1101 Exclude from CRC. This command is appended to and FIFOed along with the next character loaded into the transmit FIFO. It causes the transmitter CRC generator to be disabled while the appended character is being transmitted. Thus, that character is not included in the CRC accumulation.

Receiver Commands

0000 Reset Receiver. Causes the receiver to cease operation, clears the receiver FIFO, clears the data path, and clears the receiver status (RSR[7:0], TRSR[3:0], and either GSR[0] or GSR[4] for Channels A and B, respectively). The counter/timer and other registers are not affected.

0001 Reserved.

0010 Enable receiver. Causes receiver operation to begin, conditioned by the state of the DCD ENABLED Rx bit, RPR[2]. Receiver goes into START, SYN, or FLAG search mode depending on channel protocol mode. Has no effect if invoked when the receiver has previously been enabled.

0011 Disable receiver. Terminates operation of the receiver. Any character currently being assembled will be lost. Does not affect FIFO or any status. While in COP mode, disabling the receiver does not clear the data path; in all other cases, it does.

Counter/Timer Commands

0000 Start. Starts the counter/timer and prescaler.

0001 Stop. Stops the counter/timer and prescaler. Since the command may be asynchronous with the selected clock source, the counter/timer and/or prescaler may count one or more additional cycles before stopping.

0010 Preset to FFFF. Presets the counter timer to H'FFFF' and the prescaler to its initial value. This command causes the C/T output to go Low.

0011 Preset from CTPRH/CTPRL. Transfers the current value in the counter/timer preset registers to the counter/timer and presets the prescaler to its initial value. This command causes the C/T output to go Low.

Digital Phase-Locked Loop Commands

0000 Enter Search Mode. This command causes the DPLL counter to be set to the value 15 and the clock output will be forced Low. The counter will be disabled until a transition on the data line is detected, at which point it will start incrementing. After the counter reaches a count of 31, it will reset to zero and cause the clock output to go from Low to High. The DPLL will then continue normal operaton. This allows theDPLL to be locked onto the data without pre-frame transitions. This command should not be used if the DPLL is programmed to supply the clock for the transmitter is active.

0001 Disable DPLL. Disables operation of the DPLL.

0010 Set FM Mode. Sets the DPLL to the FM mode of operation, used when FM0, FM1, or Manchester (NMRZ) is selected by CMR1[7:6].

0011 Set NRZI Mode. Sets the DPLL to the NRZI mode of operation, used when NRZ or NRZI is selected by CMR1[7:6].

0100 Reserved for test.

0101 Reserved for test.

DETAILED OPERATION

Interrupt Control

A single interrupt output (IRQN) is provided which is activated upon the occurrence of any of the following conditions:

Channel A external or C/T special condition

Channel B external or C/T special condition

Channel A Rx/Tx error or special condition

Channel B Rx/Tx error or special condition

Channel A TxRDY

Channel B TxRDY

Channel A RxRDY

Channel B RxRDY

Each of the above conditions occupies a bit in the General Status Register (GSR). If ICR[2] is set, the eight conditions are encoded into three bits which are inserted into bits [2:0] or [4:2] of the interrupt vector register. This forms the content of the IVRM during an interrupt acknowledge cycle. Unmodified and modified vectors can read directly through specified registers. Two of the conditions are the inclusive OR of several other maskable conditions:

– External or C/T special condition: Delta DCD, Delta CTS or C/T zero count (ICTSR[6:4]).

Table 9. Command Register Bit Format

CHANNEL COMMAND REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CCRA, CCRB)					**Transmitter Command**			
	00 = Transmitter CMD		don't care	don't care	0000 — reset Tx 0001 — reset TxCRC* 0010 — enable Tx 0011 — disable Tx 0100 — transmit SOM (TSOM) 0101 — transmit SOM with PAD (TSOMP) 0110 — transmit EOM (TEOM)* 0111 — transmit ABORT/BREAK (TABRK) 1000 — transmit DLE (TDLE)* 1001 — go active on poll 1010 — reset go active on poll 1011 — go on-loop 1100 — go off-loop 1101 — exclude form CRC*			
	01 = Receiver CMD		don't care	don't care	**Receiver Command** 0000 — reset Rx 0001 — reserved 0010 — enable Rx 0011 — disable Rx			
	10 = C/T CMD		don't care	don't care	**Counter/Timer Command** 0000 — start 0001 — stop 0010 — preset to FFFF 0011 — preset from CTPRH/CTPRL			
	11 = DPLL CMD		don't care	don't care	**DPLL Command** oooo — enter search mode 0001 — disable DPLL 0010 — set FM mode 0011 — set NRZI mode 0100 — reserved for test 0101 — reserved for test			

– Rx/Tx error or special condition: any condition in the Receiver Status Register (RSR[7:0]) or a transmitter or DPLL condition in the Transmitter and Receiver Status Register (TRSR[7:3]).

The TxRDY and RxRDY conditions are defined by OMR[4] and OMR[3], respectively. Also associated with the interrupt system are the Interrupt Enable Register (IER), one bit in the Counter/Timer Control Register (CTCR), and the Interrupt Control Register (ICR).

The IER is programmed to enable specified conditions or groups of conditions to cause an interrupt by asserting the corresponding bit. A negated bit prevents an interrupt from occurring when the condition is active and hence masks the interrupt. In addition to the IER, CTCR[7] could be programmed to enable or disable an interrupt upon the C/T zero count condition. The interrupt priorities within a channel are fixed. Priority between channels is controlled by ICR[7:6]. Refer to Table 8 and ICR[7:6].

The ICR contains the master interrupt enables for each channel (ICR[1] andICR[0]) which must be set if the corresponding channel is to cause an interrupt. The CPU vector mode is specified by ICR[5:4] which selects either vectored or non-vectored operation. If vectored mode is selected, the content of the IVR or IVRM is placed on the data bus when IACK is activated. If ICR[2] is set, the content of IVRM is output which contains the content of IVR and the encoded status of the interrupting condition.

Upon receiving an interrupt acknowledge, the DUSCC locks its current interrupt status until the end of the acknowledge cycle. If it has an active interrupt pending, it responds with the appropriate vector and then asserts DTACKN. If it does not have an interrupt, it propagates the acknowledge through its X2/IDCN output if this function is programmed in PCRA[7]; otherwise, the IACKN is ignored. Locking the interrupt status at the leading edge of IACKN prevents a device at a High position in the interrupt daisy chain from responding to an IACK issued for a lower priority device while the acknowledge is being propagated to that device.

DMA Control

The DMA control section provides the interface to allow the DUSCC to operate with an external DMA controller. One of four modes of DMA can be programmed for each channel independently via CMR2[5:3]:

– Half-duplex single address. In this mode, a single pin provides both DMA read and write requests. Acknowledgement of the requests is via a single DMA acknkowledge pin. The data transfer is accomplished in a single bus cycle — the DMA controller places the memory address of the source or destination of the data on the address bus and then issues the acknowledge signal, which causes the DUSCC to either write the data into its transmit FIFO (write request) or to output the contents of the top of the recieve FIFO (read request). The cycle is completed when the DTCN input is asserted by the DMA controller. This mode can be used when channel operation is half-duplex (e.g., BISYNC) and allows a single DMA channel to service the receiver and

transmitter. The receiver and transmitter should not be enabled at the same time when half-duplex mode is programmed.

– Half-duplex dual address. In this mode, a single pin provides both DMA read and write requests. Acknowledgement of the requests is via normal bus read and write cycles. The data transfer requires two bus cycles — the DMA controller acquires the data from the source (memory for a Tx DMA or DUSCC for a Rx DMA) on the first cycle and deposits it at the destination (DUSCC for a Tx DMA or memory for a Rx DMA) on the second bus cycle. This mode is used when channel operation is half-duplex (e.g., BISYNC) and allows a single DMA channel to service the receiver and transmitter.

– Full-duplex single address. This mode is similar to half-duplex single address mode but provides separate request and acknowledge pins for the receiver and transmitter.

– Full-duplex dual address. This mode is similar to half-duplex dual address mode but provides duplex dual address mode and provides separate request pins for the receiver and transmitter

Figures 4 through 7 describe operation of the DUSCC in the various DMA environments. Table 10 summarizes pins used for the DMA request and acknowledge function for the transmitter and receiver for the different DMA modes.

The DMA request signals are functionally identical to the TxRDY and RxRDY status signals for each serial channel except that the DMA request signals are negated on the leading edge of the acknowledge signal when the subsequent transfer causes the FIFO to become full (transmitter request) or empty (receiver request).

In non-DMA operation TxRDY and RxRDY signals are automatically negated only after the transfer is completed. The DMA read request can be programmed through OMR[3] be asserted either when any character is in the receive FIFO or only when the receive FIFO is full. Likewise, the DMA write request can be programmed through OMR[4] to be asserted either when the transmit FIFO is not full or only when the transmit FIFO is empty (The transmitter must be enabled for a DMA request to be asserted). The request signals are automatically negated when the respective data transfer cycle is completed and the FIFO becomes full (transmitter request) or empty (receiver request). If a transfer is completed and the FIFO is not left full (transmitter) or empty (receiver), the request stays Low. The request may be negated by the CPU with a status reset write cycle. (Although DONEN terminates all DMA transfers, it has no effect on the requests. The requests are a function of the FIFO status, but they can be negated by writing into the GSR.) When the serial channel is not operating in DMA mode, the request and acknowledge pins for the channel can be programmed for other functions (see Pin Descriptions).

DMA DONEN Operation

As an input, DONEN is asserted by the DMA controller concurrent with the corresponding DMA acknowledge to indicate to the DUSCC that the character being transferred into the TxFIFO is the last character of the transmission frame. In synchronous modes, the DUSCC can be programmed through TPR[4] to automatically transmit the frame termination sequence (e.g., FCS-FLAG in BOP mode) upon receipt of this signal.

As an output, DONEN is asserted by the DUSCC under the following conditions:

a. In response to the DMA acknowledge for a receiver DMA request if the FIFOed RECEIVED EOM status bit (RSR[7]) is set for the character being transferred.

b. In response to the DMA acknowledge for a receiver DMA request if the counter/timer has been programmed to count transmitted characters and the terminal count has occurred.

Block Transfers Using DTACK

The DTACKN line may be used to synchronize data transfers to and from the DUSCC utilizing a 'wait' state. Either the receive or the transmitter or both may be programmed for this mode of operation, independently for each channel, via CMR2[5:3].

In this mode, if the CPU attempts a write to the transmit FIFO and an empty FIFO position is not available, the DTACKN line will remain negated until a position empties. The data will then be written into the FIFO and DTACKN will be asserted to signify that the transfer is complete.

Similarly, a read of an empty receive FIFO will be held off until data is available to be transferred. Potentially, this mode can cause the microcomputer system to hang up if, for example, a read request was made and no further data was available.

Timing Circuits

The timing block for each channel consists of a crystal oscillator, a Bit Rate Generator (BRG), a Digital Phase-Locked Loop (DPLL) and a 16-bit Counter/Timer (C/T) (see Figure 8).

Crystal Oscillator

The crystal oscillator operates directly from a crystal (normally 14.7456MHz if the internal BRG is to be used) connected across the X1/CLK and X2/IDCN pins with a minimum of external components. If an external clock of the appropriate frequency is available, it may be connected to the X1/CLK pin. This signal is divided by two to provide the internal system clock.

Bit Rate Generator

The BRG operates from the oscillator or external clock and is capable of generating 16-bit rates. These are available to the receiver, transmitter, DPLL, and C/T. The BRG output is at 32X the base bit rate. Since all sixteen rates are generated simultaneously, each receiver and transmitter may select its bit rate independently. The transmitter and receiver timing registers include a 4-bit field for this purpose (TTR[3:0], RTR[3:0]).

Digital Phase-Locked Loop

Each channel of the DUSCC includes a DPLL used in synchronous modes to recover clock information from a received data stream. The DPLL is driven by a clock at nominally 32 times the data rate. This clock can be programmed, via RTR[7:4], to be supplied from an external input, from the receiver BRG, from the C/T, or directly from the crystal oscillator.

The DPLL uses this clock, along with the data stream to construct a data clock which may then be used as the DUSCC receive clock, transmit clock, or both. The output of the DPLL is a square wave at 1X the data rate. The derived clock can also be programmed to be output on a DUSCC pin; only the DPLL receiver output clock is available at the TRxC pin. Four commands are associated with DPLL operation: Enter search mode, set FM mode, set NRZI mode, and disable DPLL. The commands are described in the Command Register Description. Waveforms associated with the DPLL are illustrated in Figure 9.

Table 10. DMA REQ and ACK Pins for Operational Modes

FUNCTION	HALF DUPLEX SINGLE ADDR DMA	HALF DUPLEX DUAL ADDR DMA	FULL DUPLEX SINGLE ADDR DMA	FULL DUPLEX DUAL ADDR DMA
RCVR REQ	RTxDRQN	RTxDRQN	RTxDRQN	RTxDRQN
TRAN REQ	Same as RCVR REQ	Same as RCVR REQ	TxDRQN	TxDRQN
RCVR ACK	RTxDAKN	Normal read RCVR FIFO	RTxDAKN	Normal read RCVR FIFO
TRAN ACK	Same as RCVR ACK	Normal write TRAN FIFO	TxDAKN	Normal write TRAN FIFO

DPLL NRZI Mode Operation — This mode is used with NRZ and NRZI data encoding. With this type of encoding, the transitions of the data stream occur at the beginning of the bit cell. The DPLL has a six-bit counter which is incremented by a 32X clock. The first edge detected during search mode sets the counter to 16 and begins operation. The DPLL output clock then rises at a count of 0 and falls at 16. Data is sampled on the rising edge of the clock. When a transition in the data stream is detected, the count length is adjusted by one or two counts, depending on the counter value when the transition occurs (see Table 11). A transition detection at the roll-over point (third column in Figure 11) is treated as a transition occurring at zero count.

The count length adjustments cause the rising edge of the DPLL output block to converge to the nominal center of the bit cell. In the worst case, which occurs when a DPLL pulse is coincident with the data edge, the DPLL converges after 12 data transitions.

For NRZ encoded data, a stream of alternating ones and zeros should be used as a synchronizing pattern. For NRZI encoded data, a stream of zeros should be used.

Table 11. NRZI Mode Count Length

COUNT WHEN TRANSITION DETECTED	COUNT LENGTH ADJUSTMENT	COUNTER RESET AFTER COUNT REACHES
0 — 7	-2	29
8 — 15	-1	30
16 — 23	+1	32
24 — 30	+2	33
None detected	0	31

DPLL FM Mode Operation — FM operation is used with FM0, FM1, and Manchester data encoding. With this type of encoding, transitions in the data stream always occur at the beginning of the bit cell for FM0 and FM1, or at the center of the bit cell for Manchester. The DPLL 6-bit counter is incremented by a 32X clock. The first edge detected during search mode sets the counter to 16 and begins operation. The DPLL receiver clock then rises on a count of 8 and falls on 24. (The DPLL transmitter clock output falls on a count of 16. It rises on a count of 0 if a transition has been detected between count of 16 and 23. For other cases, it rises 1/2 count of the 32X input clock sooner.) This provides a 1X clock with edges positioned at the nominal centers of the two halves of the bit cell. The transition detection circuit is enabled between counts of 8 and 23, inclusive. When a transition is detected, the count length is adjusted by one, depending on when the transition occurs (see Table 12).

If a transition is not detected for two consecutive data bits, the DPLL is forced into search mode and the DPLL error status bit (TRSR[3]) is asserted. This feature is disabled when the DPLL output is used only as the transmitter clock.

To prevent the DPLL from locking on the wrong edges of the data stream, an opening PAD sequence should be transmitted. For FM0, a stream of at least 16 ones should be sent initially. For FM1, a minimum stream of 16 zeros should be sent and for Manchester encoding the initial data stream should consist of alternating ones and zeros.

Table 12. FM Mode Count Length

COUNT WHEN TRANSITION DETECTED	COUNT LENGTH ADJUSTMENT	COUNTER RESET AFTER COUNT REACHES
8 — 15	-1	30
16 — 23	+1	32
24 — 7	Disabled	
None detected	0	31

Counter/Timer

Each channel of the DUSCC contains a Counter/Timer (C/T) consisting of a 16-bit down counter, a 16-bit preset register, and associated control circuits. Operation of the counter/timer is programmed via the Counter/Timer Control Register (CTCR). There are also four commands associated with C/T operation, as described in the Command Description section.

The C/T clock source, clock prescaling, and operating mode are programmed via CTCR[2:0], CTCR[4:3], and CTCR[6], respectively. The preset register is loaded with minimum of 2 by the CPU and its contents can be transferred into the down counter by a command, or automatically upon reaching terminal count if CTCR[6] is negated. Commands are also available to stop and start the C/T and to preset it to an initial value of FFFF. Counting is triggered by the falling edge of the clocking input. The C/T zero count status bit, ICTSR[6], is set when the C/T reaches the terminal count of zero and ICTSR[7] indicates whether the counter is currently enabled or not.

An interrupt is generated upon reaching zero count if CTCR[7] and the channel's master interrupt enable are asserted. The output of the C/T can be programmed to be output on the channel's RTxC or TRxC pin (via PCR[4:0]) as either a single pulse or a square wave, as programmed in CTCR[5]. The contents of the C/T can be read at any time by the CPU, but the C/T should normally be stopped before this is done. Several C/T operating modes can be selected by programming of the counter/timer control register. Typical applications include:

1. Programmable divider. The selected clock source, optionally prescaled, is divided by the contents of the preset register. The counter automatically reloads itself each time the terminal count is reached. In this mode, the C/T may be programmed to be used as the Rx or Tx bit rate generator, as the input to the DPLL, or it may be output on a pin as either a pulse or a square wave. The C/T interrupt should be disabled in this mode.
2. Periodic interrupt generator. This mode is similar to the programmable divider mode, except that the C/T interrupt is enabled, resulting in a periodic interrupt to the CPU.

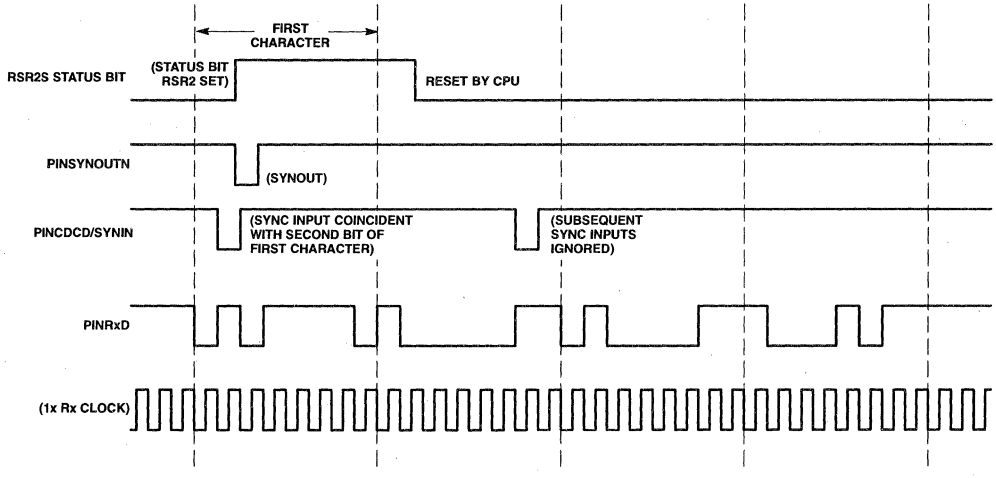


Figure 2. External Sync Mode

3. Delay timer. The counter is preset from the preset register and a clock source, optionally prescaled, is selected. An interrupt is generated upon reaching terminal count. The C/T continues counting without reloading itself and its contents may be read by the CPU to allow additional delay past the zero count to be determined.

4. Character counter. The counter is preset to FFFF by command and the clock source becomes the internal signal used to control loading of the Rx or Tx characters. This operation is selected by CTCR[2:0]. The C/T counts characters loaded into the RxFIFO by the receiver or loaded into the transmit FIFO by the CPU, respectively. The current character count can be determined by the CPU by reading the contents of the C/T and taking its ones complement. Optionally, a preset number may be loaded into the counter and an interrupt generated when the count is exhausted. When counting Tx characters, the terminal count condition can be programmed through TPR[4] to cause an end of message sequence to be transmitted. When counting received characters, the FIFOed EOM status bit is asserted when the character which causes the count to go to zero is loaded into the receive FIFO. The channel's 'reset Tx' or 'reset Rx' commands have no effect on the operation of the C/T.

5. External event counter. The counter is preset to FFFFF by command and an external clock source is selected. The current count can be determined by the CPU by reading the contents of the C/T and taking its ones complement. Optionally, a preset number may be loaded into the counter and an interrupt generated when the count is exhausted.

6. Bit length measurement. The counter is preset to FFFF by command and the X1/CLK/4 clock input gated by RxD mode (optionally prescaled) is programmed. The C/T starts counting when RxD goes Low and stops counting when RxD goes High. At this time, ICTSR[6] is set and an interrupt (if enabled) is generated. The resulting count in the counter can be read by the CPU to determine the bit rate of the input data. Normally this function is used for asynchronous operation.

Communication Channels A and B

Each communication channel of the DUSCC is a full-duplex receiver and transmitter that supports ASYNC, COP, and BOP transmission formats. The bit rate clock for each receiver and transmitter can be selected independently to come from the bit rate generator, C/T, DPLL, or an external input (such as a modem generated clock).

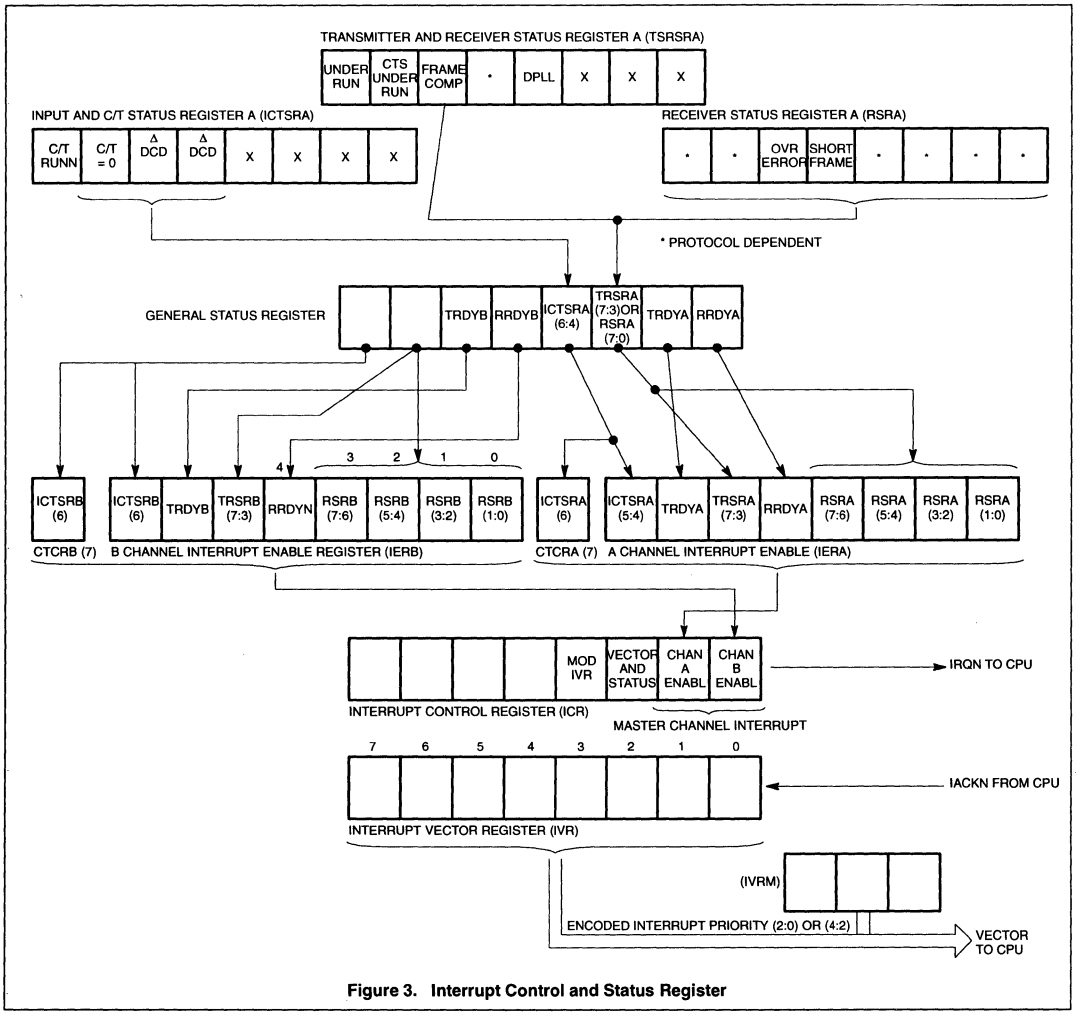


Figure 3. Interrupt Control and Status Register

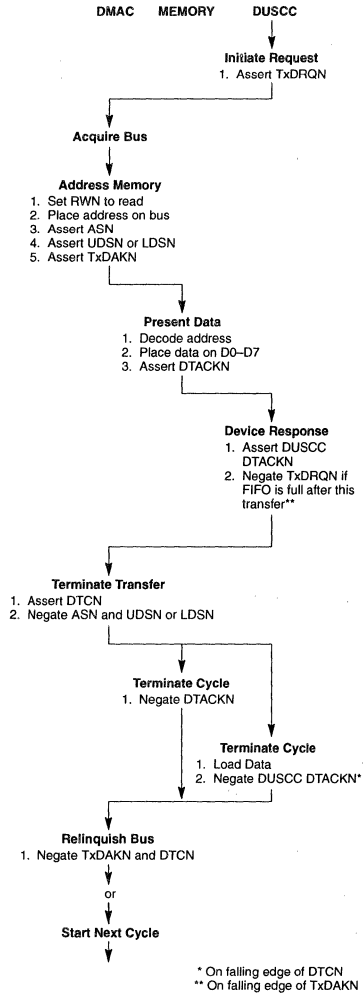


Figure 4. TransmitterDMA Request Operation — Single Address Mode

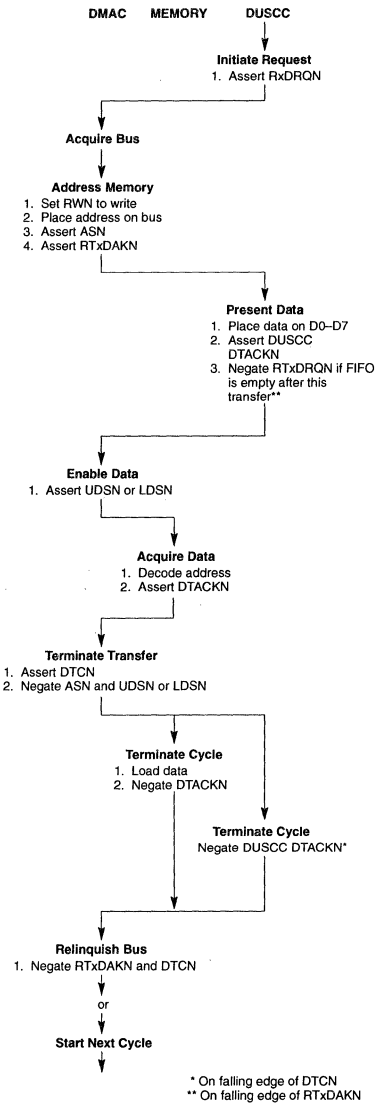


Figure 5. Receiver DMA Request Operation — Single Address Mode

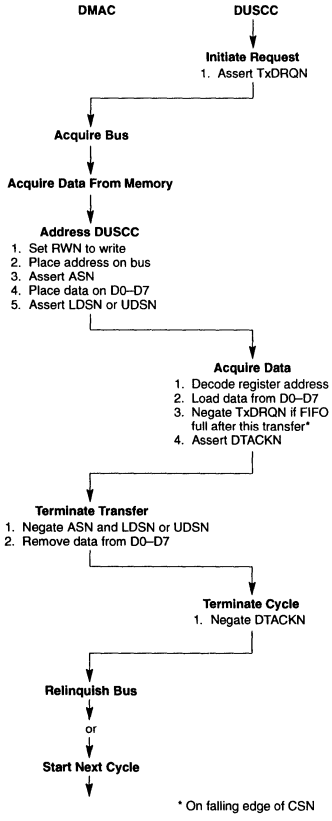


Figure 6. Transmitter DMA Request Operation — Dual Address Mode

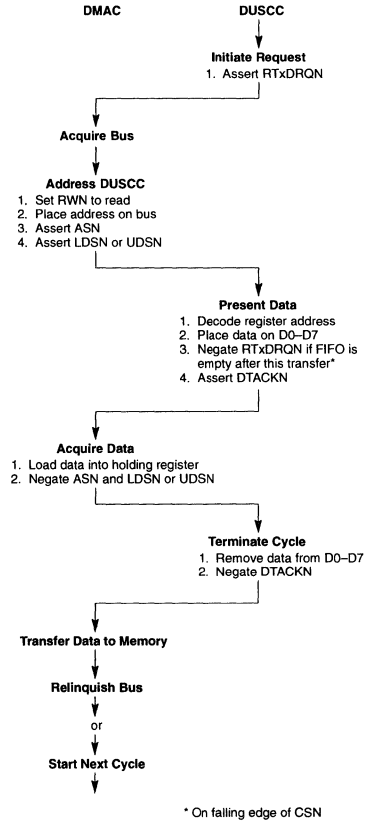


Figure 7. Receiver DMA Request Operation — Dual Address Mode

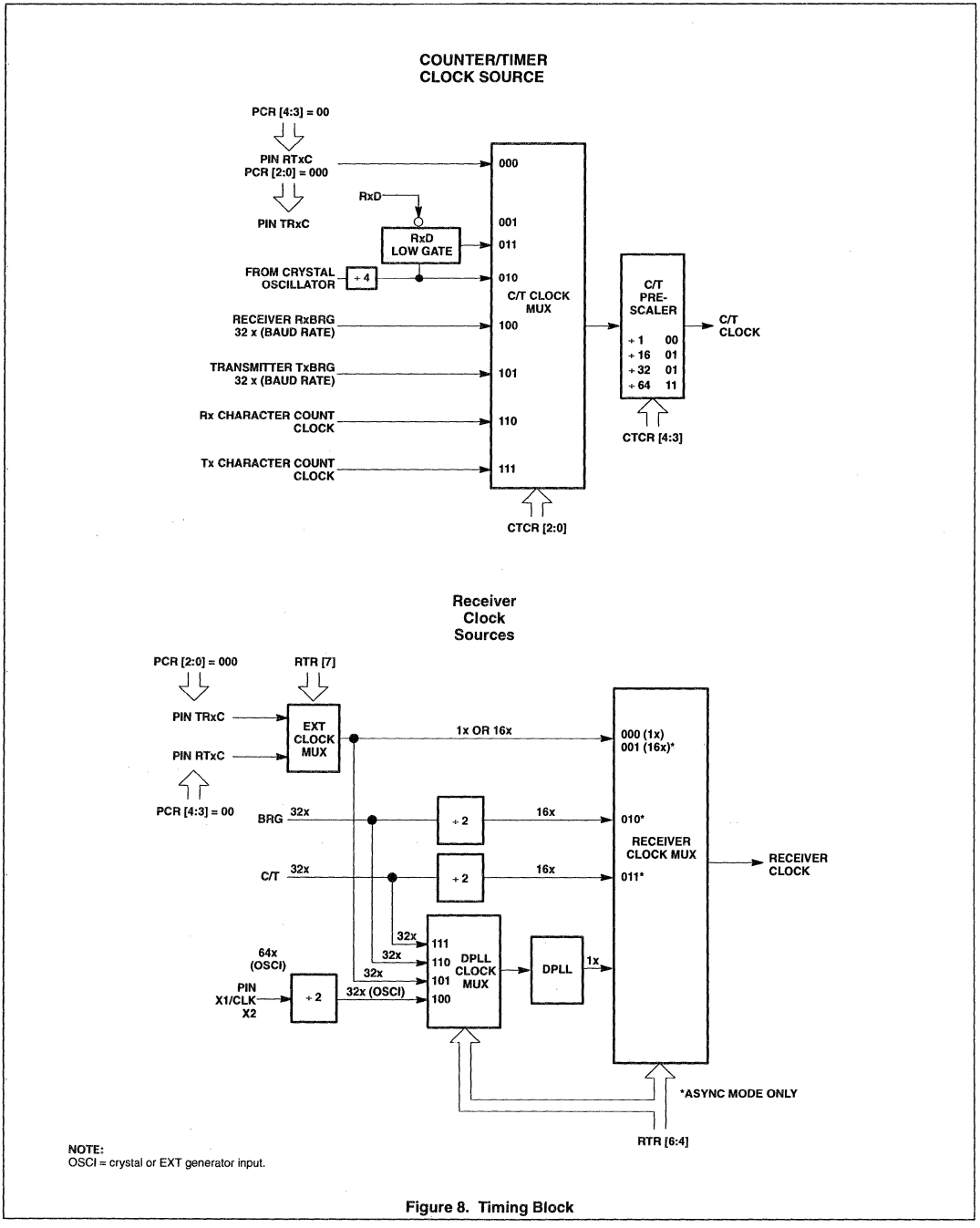
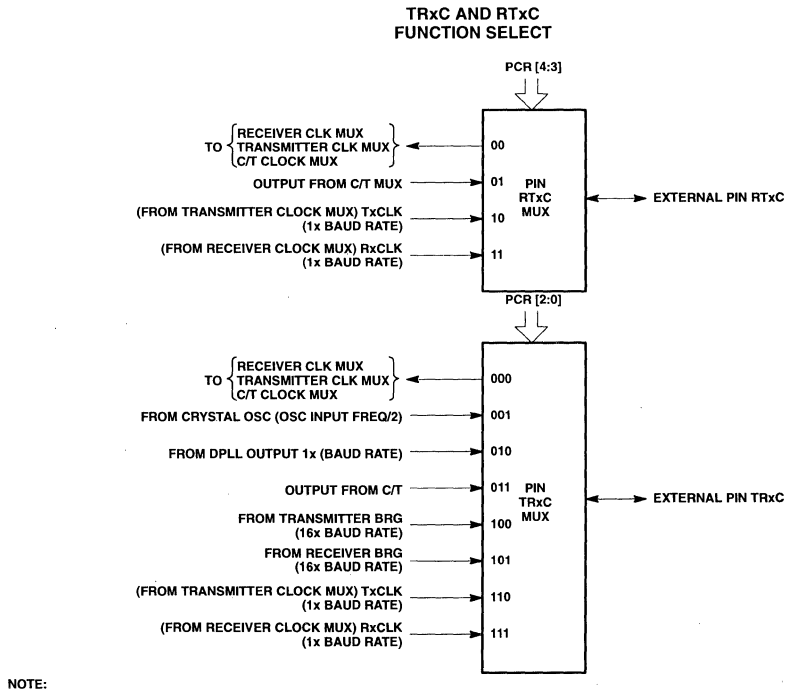


Figure 8. Timing Block



NOTE:
OSCI = crystal or EXT generator input.

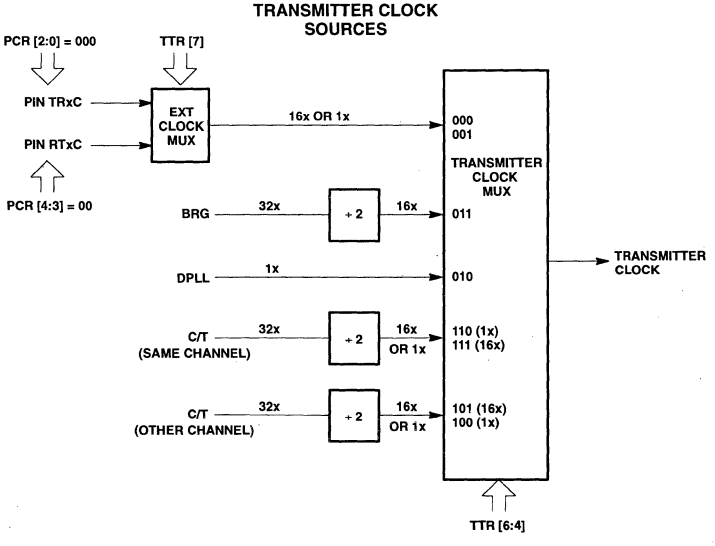


Figure 9. Timing Block (Continued)

TRANSMITTER

Transmitter TxFIFO and TxRDY

The transmitter accepts parallel data from the data bus and loads it into the TxFIFO, which consists of four 8-bit holding registers. This data is then moved to the Transmitter Shift Register (TxSR) which serializes the data according to the transmission format programmed. The TxSR is loaded from the TxFIFO, from special character logic, or from the CRC/LRC generator. The LSB is transmitted first, which requires right justification of characters by the CPU. TxRDY (GSR[5] or GSR[1]) and underrun (TRSR[7]) indicate the state of the TxFIFO. The TxFIFO may be addressed at any of four consecutive locations (see Table 1) to allow use of multiple byte work instructions. A write to any valid address always writes data to the next empty FIFO location.

TxRDY is set when the transmitter is enabled and there is an empty position in the TxFIFO (OMR[4] = 0) or when the TxFIFO becomes empty (OMR[4] = 1). The CPU may reset TxRDY through a status reset write cycle. If this is done, it will not be reasserted until a character is transferred to the TxST (OMR[4] = 0) or when the TxFIFO becomes empty again (OMR[4] = 1). The assertion of TxRDY, enabling of the IER [6] and the enabling of the channel master interrupt ICR[0] or [1] allow an interrupt to be generated.

If DMA operation is programmed, either RTxDRN (half-duplex) or TxDRQN (full-duplex) follows the state of TxRDY if the transmitter is enabled. These operations differ from normal ready in that the request signal is negated on the leading edge of the DMA acknowledge signal when the subsequent transfer causes the transmit FIFO to become full, while the TxRDY signal is negated only after the transfer is completed. Underrun status TRS[7] set indicates that one or more data character (not PAD characters) have been transmitted and the TxFIFO and TxSR are both empty.

In 'wait on Tx', a write to a full FIFO causes the write cycle to be extended until a FIFO position is available. DTACKN is asserted to acknowledge acceptance of the data. In non-wait modes, if an attempt is made to load data into a full TxFIFO, the TxFIFO data is preserved and the overrun data character(s) is lost. A normal DTACKN will be issued, and no indication of this occurrence is provided. The transmitter is enabled by the enable transmitter command. When the disable transmitter command is issued, the transmitter continues to operate until the TxFIFO becomes empty. The TxRDY does not become valid until the transmitter is enabled. Characters can be loaded into the FIFO while disabled. However, if the FIFO is full when the transmitter is enabled, TxRDY is not asserted.

TxRTS Control

If TxRTS CONTROL, TPR[3], is programmed, the channel's RTS output is negated 5-bit times after the last bit (stop bit in ASYNC mode) of the last character is transmitted. RTS is normally asserted and negated by writing to OMR[0]. Setting of TPR[3] causes RTS to be reset automatically (if the transmitter is not enabled) after all characters in the transmitter FIFO (if any) are transmitted and five bit times after the 'last character' is shifted out. This feature can be used to automatically terminate the transmission of a message as follows:

- Program auto-reset mode: TPR[3] = 1.
- Enable transmitter.
- Assert RTSN: OMR[0] = 1.
- Send message.
- Disable transmitter after the last character is loaded into the TxFIFO.
- The last character will be transmitted and OMR[0] will be reset five bit times after the last bit, causing RTSN to be negated. The TxD output will remain in the marking state until the transmitter is enabled again.

The 'last bit' in ASYNC is simply the last stop bit of the character. In BOP and COP, the last character is defined either explicitly by either appending it with TEOM or implicitly through the selection of the frame underrun control sequence, TPR[7:6] (Transmitter Parameter Register). Table 13 summarizes the relationship of the selected underrun sequence and the protocol mode.

Tx CTS Operation

If CTS enable Tx, TPR[2], is set, the CTSN input must be asserted for the transmitter to operate. Changes in CTSN while a character is being transmitted do not affect transmission of that character. However, if the CTS input becomes negated when TPR[2] is set and the transmitter is enabled and ready to start sending a new character, CTS underrun, TRSR[6], is asserted and the TxD output is placed in the marking (High) state. In ASYNC mode, operation resumes when CTSN is asserted again. In COP and BOP modes, the transmission of the message is terminated and operation of the transmitter will not resume until CTS is asserted and a TSOM or TSOMP command is invoked. Prior to issuing the command and retransmitting the message, the transmitter must be reset. After a change-of-state STS is established by the input sampling circuits (refer to the description of ICTSR[4], it is sampled by the Tx controller 1-1/2 bit times before each new character is serialized out of the Tx shift register. (This is 2-1/2 bits before the LSB of the new character appears on the TxD pin; there is an additional 1-bit delay in the transmitter data path due to the data encoding logic.)

Tx Special Bit Pattern Transmission

The DUSCC provides features transmit special bit patterns (see Table 14).

The TxD pin is held marking after a hardware reset, a reset Tx command, when the transmitter is not enabled, and during underrun/idle, if this feature is selected through TPR[7:5]. The TxD pin is also held marking if the transmitter is enabled, and the TxFIFO is empty (ASYNC), or if a TSOM or TSOMP command has not been issued (SYNC modes).

The following command bits can be appended to characters in the TxFIFO: TEOM, TDLE, exclude from CRC, and reset TxCRC. An invoked command(s) is appended to the next character loaded into the TxFIFO and follows the character through the FIFO until that character is ready to be loaded into the TxSR. The transmitter for the various protocols.

Tx ASYNC Mode

Serialization begins when the TxFIFO data is loaded into the TxSR. The transmitter first sends a start bit, then the programmed number of bits/character (TPR[1,0]), a parity bit (if specified), and the programmed number of stop bits. following the transmission of the stop bits, if a new character is not available in the TxFIFO, the TxD output goes to marking and the underrun condition (TRSSR[7]) is set.

Transmission resumes when the CPU loads a new character into the TxFIFO or issues a send break command. The send break command clears the TxFIFO and forces a continuous space (Low) on the TxD output after the character in TxSR (if any) is serialized. A send break acknowledge (TRSR[4]) is returned to the CPU to facilitate reassertion of the send break command in order to send an integral number of break characters. The send break condition is cleared when the reset Tx or disable Tx command is issued.

Tx COP Modes
Transmitter commands associated with all COP modes are: transmit SOM (TSOM, transmit start of message), transmit SOM with PAD (TSOMP0, transmit EO (TEOM, transmit end of message), reset TxCRC, exclude from CTC, and transmit DLE.

A TSOM or send TSOMP command must be issued to start COP transmission. TSOM (without PAD) causes the TxCRC/LRC generator to be initialized and one or two SYN characters from S1R/S2R to be loaded into the TXSR and shifted out on the TxD output. A parity bit, if specified, is appended to each SYN character after the MSB. Send SOM acknowledge (TRSR[4]) is asserted when the SYN output begins. The user may reinvoke the command to cause multiple SYNs to be transmitted. If the command is not reinvoked and the TxFIFO is empty, SYN patterns continue to be transmitted until the TxFIFO is loaded. If data is present in the FIFO, the first character is loaded into the TxSR and serialization of the data begins. Note that the TxFIFO may be preloaded with data before the TSOM is issued.

The TSOMP command causes all characters in the TxFIFO (PAD characters) to be loaded into the TxSR and serialized if the Tx is enabled. Unlike the transmit SOM without PAD command, data (non-PAD characters) cannot be preloaded into the TxFIFO. While the PAD is transmitted, parity is disabled and character length is automatically set to 8 bits regardless of the value in TPR[1:0]. When the TxFIFO becomes empty after the PAD, the TxCRC/LRC generator is initialized, the SYN character(s) are transmitted with optional parity appended, and send SOM acknowledge asserted. Operation then proceeds in the same manner as the TSOM command; the user has the option to invoke the TSOM command to cause multiple SYNs to be transmitted.

After the TSOM/TSOMP command is executed, characters in the TxFIFO are loaded into the TxSR and shifted out with a parity bit, if specified, appended after the MSB. If, after the opening SYN(s) and at least one data has been transmitted, the TxFIFO is empty, a data underrun condition results and TRSR[7] is asserted. The transmitter's action on data underrun is determined by TPR[7:6] and the COP protocol. If TRP[7:6] = '10', the transmitter line fills with MARK characters until a character is loaded into the FIFO. I TRP[7:6] and the COP protocol. If TPR[7:6] = '11' is selected, the transmitter line fills with SYN, SYN1-SYN2, or DLE-SYN1 for monosync, dual sync, and BISYNC transparent modes, respectively. If TPR[7:6] = '00', the BCC characters are transmitted and frame complete (TRSR[6]) is set. TxD then assumes the programmed idle state (TPR[5]) of MARKs or SYN1/SYN1-SYN2.

Operation resumes with the transmission of a SYN sequence when a TSOM command is invoked. A TSOMP command is ignored unless the transmitter is disabled and then reenabled.

An appended TEOM command also terminates the frame as described above. It occurs after transmission of the character to which the TEOM is appended. The TEOM command can be explicitly asserted through the channel command register. If TPR[4] = '1', the TEOM is automatically appended to a character in DMA mode, if the DONEN input is asserted when that character is loaded into the TxFIFO, or if the counter/timer is counting transmitted characters when the character which causes the counter to reach zero count is loaded.

The TDLE command when appended to a character in the TxFIFO, causes the DLE character to be loaded into the the TxSR and serialized before the TxFIFO character is loaded into the TxSR and serialized. This feature is particularly useful for BISYNC operation. The DLE character will be excluded from the CRC accumulation in BISYNC transparent mode (see below), but will be included in all other COP modes.

In BISYNC mode, transmission of a DLE-STX character sequence (either via a send TDLE command appended to the STX character, or via DLE and STX loaded into the TxFIFO) puts the transmitter into the transparent test mode of operation. In this mode, normally restricted character sequences can be transmitted as 'normal' bit sequences. The switch occurs after transmission of the two characters, so that the DLE and STX are included in the BCC accumulation. If the DLE-STX is to be excluded from the CRC, the user should issue a 'reset CRC' command prior to loading the next character.

Another method of excluding the two characters from the CRC is to invoke the 'exclude from CRC' command prior to loading the character(s) into the FIFO. While in transparent mode, the transmitted line fills with DLE-SYN1 and automatically transmits an extra DLE if it finds a DLE in the TxFIFO ('DLE stuffing'). The transmitter reverts to non-transparent mode when the frame complete status is set in TRSR[5].

CRC/LRC accumulation can be specified in all COP modes; the type of CRC is specified via CMR2[2:0]. The TSOM/TSOMP commands set the CRC/LRC accumulator to its initial state and accumulation begins with the first non-SYN character after the initial SYN(s) are transmitted. PAD characters are not subject to CRC accumulation. In non-BISYNC or BISYNC normal modes, all transmitted characters except linefill characters (SYNs or MARKs) are subject to accumulation. In BISYNC transparent mode, odd (stuffed) DLEs and the DLE-SYN1 linefill are excluded from the accumulation. Characters can be selectively excluded from the accumulation by invoking the 'exclude form CRC' command prior to loading the character into the FIFO.

Accumulation stops when transmission of the first character of the BCC begins. The CPU can set the accumulator to its initial state prior to the transmission of any character by using the appended reset CRC command. The CRC generator is also automatically initialized after the EOM is sent.

Table 13. Abort Sequence — Protocol Mode

TPRA[7:6]	PROTOCOL	LAST CHARACTER
00	BOP	FLAG following either FCS (if selected) or last data character
	COP	Last byte of FCS before line begins SYN or MARKing
10	BOP	Abort sequence (11111111) prior to MARKing
	COP	Last byte of FCS before line begins SYN or MARKing
11	BOP	Abort sequence (11111111) prior to FLAG
	COP	First SYN of SYN sequence

Table 14. Special Bit Patterns

PROTOCOL	BIT PATTERN
ASYNC-BREAK	An all 0's character including parity bit (if specified) and stop bits. Used for send break command.
COP-SYN	Contained in S1R (single SYN mode) or in S1R/S2R (dual SYN modes). Used for TSOM and TSOMP commands and for non-transparent mode linefill and IDLE.
COP-DLE	Used for TDLE command and for BISYNC transparent mode linefill and to generate BISYNC control sequences.
COP-CRC	16/8 bits from the CRC/LRC accumulator used for TEOM command or for auto-EOM modes.
BOP-FLAG	01111110. Used for TSOM, TSOMP, and TEOM commands, for auto-EOM modes, and as an IDLE line fill.
BOP-ABORT	11111111. Used for send ABORT command or during TxFIFO underrun.
BOP-CRC	16 bits from the CRC accumulator used for TEOM command or for auto-EOM modes.
BOP/COP MARK	All 1's pattern on data line.

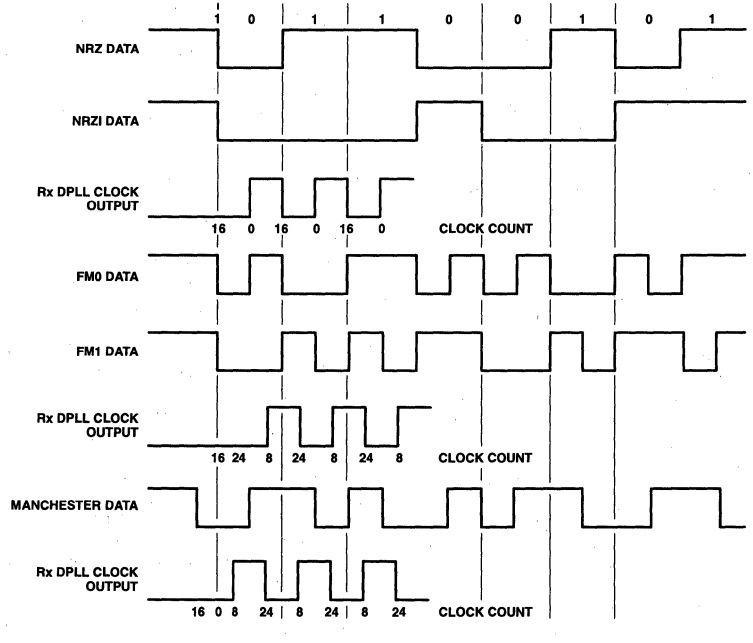


Figure 10. DPLL Waveforms

TxBOP Modes

Transmitter commands associated with BOP modes are TSOM, TSOMP, TEOM, and transmit ABORT (TABRK). The TSOM and TSOMP commands are identical to COP modes except that a FLAG character (01111110) is used as the start of message sequence instead of the SYNs, and FLAG(s) that continue to be sent until the TxFIFO is loaded. There is no zero insertion (see below) during transmission of the PAD characters, and they are not preceded by a FLAG or accumulated in the CRC. Character length is automatically set to 8 bits regardless of TPR[1:0].

The first characters loaded into the TxSR from the TxFIFO are the address and control fields, which have fixed character lengths of eight bits. The number of address field bytes is determined by CMR1[4:3]. If extended address field is specified, the field is terminated if the first address octet is H'00' or if the LSB of the octet is a 1. The number of control field bytes is selected by CMR1[5]. If any information field characters follow the control field (forming an I field), they are transmitted with the number of bits per character programmed in TPR[1:0]. The TEOM command can be appended to the last character whether explicitly or automatically as described

for COP mode. When the character with the appended TEOM is loaded from the TxFIFO, it is transmitted with the character length specified by OMR[7:5]. In this way, a residual character of 1 - 8 bits is transmitted without requiring the CPU to change the Tx character length for this last character.

After opening the FLAG and first address octet have been transmitted, an underrun occurs (TRSR[7] = 1) if the TxFIFO is empty when the transmitter requires a new character. The underrun control bits (TPR[7:6]) determine whether the transmitter line fills with either ABORT-MARKs, ABORT-FLAGs (see below), or ends transmission with the 'normal' end of message sequence.

EOM on underrun is functionally similar to EOM due to an appended TEOM command. If the EOM is due to underrun, the normal character length applies to the last data character. After the last character is transmitted, the FCS (inverted CRC) and closing FLAG are sent, frame complete (TRSR[5]) is set, and the TxCRC is initialized. If the TxFIFO is empty after the closing FLAG has been sent, TXD will assume the programmed idle state of FLAGs or MARKs (TPR[5]) and wait for a character to be loaded into the FIFO or for a TSOM command to be issued. If the TXFIFO is not empty at that time, the TxFIFO data will be loaded into the TxSR and serialized. In that case, the closing FLAG is the opening FLAG of the next frame.

The user can control the number of FLAGs between frames by invoking the TSOM command after frame complete is asserted. The DUSCC then operates in the same manner as for transmission of multiple FLAGs at the beginning of a frame. When the command is no longer reinvoked, transmission of the TxFIFO data will begin. If the FIFO is empty, FLAGs continue to be transmitted.

The DUSCC provides automatic zero insertion in the data stream to prevent erroneous transmission of the FLAG sequence. All data characters loaded into the TxSR from the TxFIFO and characters transmitted from the CRC generator are subject to zero insertion. For this feature a zero is inserted in the serial data stream each time five consecutive ones (regardless of character boundaries) have been transmitted.

A send ABORT command clears the TxFIFO and inserts an ABORT character of eight ones (not subject to zero insertion) into the TxSR for transmission after the current character has been serialized. A send abort ack (TRSR[4]) facilitates reassertion of send abort by the user to guarantee transmission of multiple abort characters. This feature can be used to send the 15-ones idle sequence.

The transmitter sends either marks or FLAGs after the abort character(s) has been transmitted, depending on TPR[7:6]. Operation resumes with the transmission of a FLAG when a TSOM command is invoked. A TSOMP command is ignored unless the transmitter is disabled and then reenabled.

CRC accumulation can be specified in all BP modes. The type of CRC is specified via CMR2[2:0], and is normally selected as CRC-CCITT preset to ones, although any option is valid. Note that LRC8 option is not allowed in BOP modes.

The TSOM/TSOMP command sets the CRC accumulator to its initial state and accumulation begins with the first address octet after the initial FLAG(s). Accumulation stops when transmission of the first character of the FCS begins. The CPU can set the accumulator to its initial state prior to the transmission of any character by using the appended reset CRC command and can exclude any character from the accumulation by use of the exclude from CRC command, but these features would not normally be used in BOP modes. The

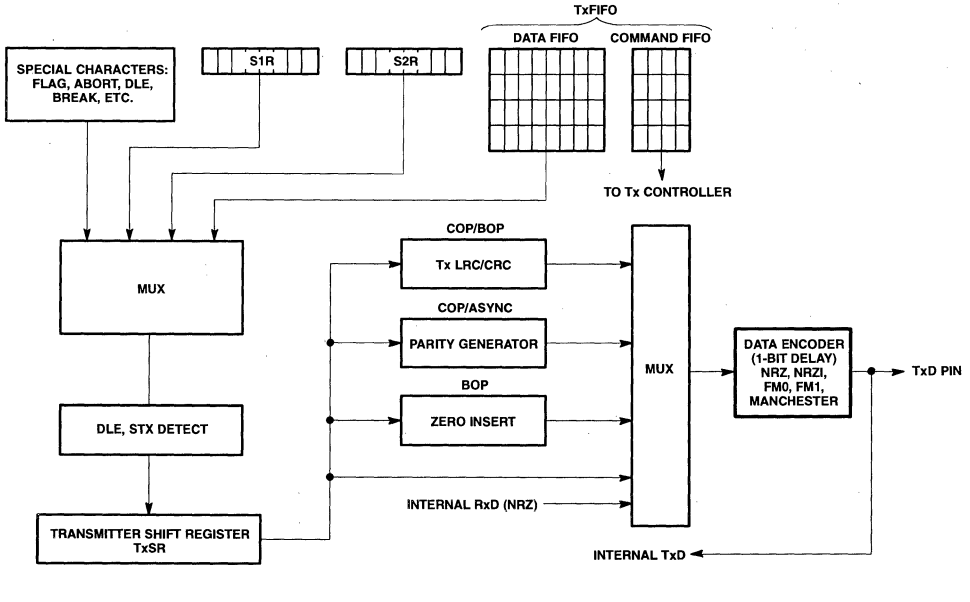


Figure 11. Transmitter Data Path

The CRC generator is also automatically initialized after the EOM or an ABORT are sent.

TxBOP Loop Mode

The loop modes are used by secondary stations on the loop, while the primary station operates in the BOP primary mode. Both the transmitter and receiver must be enabled and should be programmed to use the same clock source. Loop operation is initiated by issuing the 'go on-loop' command. The receiver looks for the receipt of seven contiguous ones and then asserts the LCN output to cause external loop control hardware to put the DUSCC into the loop, with the TxD output echoing the RxD input with a 2-bit time delay. The echoing process continues until a Go Active on Poll (GAP) command is invoked. The DUSCC then looks for receipt of an EOP bit pattern (a zero followed by seven ones, 11111110) and changes the last one of the EOP into a zero making it an opening FLAG. Loop sending (TRSR[6]) is asserted at that same time. The action of the transmitter after sending the initial FLAG depends on the status of the transmit FIFO.

If the transmit FIFO is not empty, a normal frame transmission begins. The operation is then similar to normal BOP operation with the following differences:

1. An ABORT command, an underrun, or receipt of the turnaround sequence (H'00') or FLAG cause the transmitter to cease operation and to revert to echoing the RxD input with a 2-bit time delay. A new transmission cannot begin until the GAP command is reinvoked and a new EOP sequence is received.
2. Subsequent to sending the EOM sequence of FCS-FLAG, the DUSCC examines the internal GAP flip-flop. If it is not set (having been reset by the 'reset GAP' command, the DUSCC reverts to echoing the received data. If the internal GAP flip-flop is still set, transmission of a new frame begins, with the user having control of sending multiple FLAGs between frames by use of the 'send SOM' command. If the FIFO is empty at this time, the DUSCC continues to send FLAGs until the data is loaded into the FIFO or until GAP is reset. If the latter occurs, it reverts to echoing RxD.

   When the DUSCC reverts to echoing RxD in any of the above cases, the last transmitted zero and seven ones will form an EOP for the next station down the loop.

   If the TxFIFO is empty when the EOP is recognized, the transmitter continues to send FLAGs until there is data in the FIFO. If a turnaround sequence or the reset GAP command is received before the FIFO is loaded, the transmitter switches to echoing RxD without any data transmission. Otherwise a frame transmission begins as above when a character is loaded into the FIFO. The mechanism provides time for the CPU to examine the received frame (the frame preceding the EOP) to determine if it should respond or not, while holding its option to initiate a transmission.

Termination of operation in the loop mode should be accomplished by use of the 'go off-loop' command. When the command is invoked, the DUSCC looks for the receipt of eight contiguous ones. It then negates the LCN output to cause the external loop control hardware to remove the DUSCC from the loop without affecting operation of other units remaining on the loop.

RECEIVER

The receiver data path includes two 9-bit holding registers, HSRH and HSRL, an 8-bit character comparison register, CCSR, two synchronizing flip-flops, a receiver shift register, RxST, the programmable SYN comparison registers, S1R and S2R, and BISYNC character comparison logic. The DUSCC configures the circuitry and utilizes it according to the operational mode selected for the channel through the two mode registers CMR1 and CMR2. For all data paths, character data is assembled according to the character bit count, in the RxSR, and is moved to the RxFIFO with any appended statuses when assembly is completed. Figure 1 depicts the four data paths created in the DUSCC for the previous protocols.

Receiver RxFIFO, RxRDY

The receiver converts received serial data on RxD (LSB first) into parallel data according to the transmission format programmed. Data is shifted through a synchronizing flip-flop and one or more shift registers, the last of which is the 8-bit receiver shift register (RxST). Bits are shifted into the RxSR on the rising edge of each 1X receive clock until the LSB is in RxSR[0]. Hence, the received character is right justified, with all unused bits in the RxSR cleared to zero. A receive character length counter generates a character boundary signal for synchronization of character assembly, character comparisons, break detection (ASYNC), and RxSR to RxFIFO transfers (except for BOP residual characters). During COP and BOP hunt phases, the SYN/GLAG comparison is made each receive bit time, as abort, and idle comparisons in BOP modes.

An internal clock from the BRG, the DPLL or the counter/timer, or an external 1X or 16X clock may be used as the receiver clock in ASYNC mode. The BRG or counter/timer cannot be used directly for the receiver clock in synchronous modes, since these modes require a 1X receive clock that is in phase with the received data. This clock may come externally from the RTxC or TRxC pins, or it may be derived internally from the DPLL. Received data is internally converted to NRZ format for the receiver circuits by using clock pulses generated by the DPLL.

When a complete character has been assembled in the RxSR, it is loaded into the receive FIFO with appended status bits. The most significant data bits of the character are set to zero if the character length is less than eight bits. In ASYNC and COP modes the user may select, via RPR[3], whether the data transferred to the FIFO includes the received parity bit or not. The receiver indicates to the CPU or DMA controller that it has data in the FIFO by asserting the channel's RxRDY status bit (GSR[4] or GSR[0] and, if in DMA mode, the corresponding receiver DMA request pin.

The RxFIFO consists of four 8-bit holding registers with appended status bits for character count complete indications (all modes), character compare indication (ASYNC), EOM indication (BISYNC/BOP), and parity, framing, and CRC errors. Data is loaded into the RxFIFO from the RxSR and extracted (read) by the CPU or DMA controller via the data bus. AN RxFIFO read create an empty RxFIFO position for new data from the RxSR.

RxRDY assertion depends on the state of OMR[3]:

1. If OMR[3] is 0 (FIFO not empty), RxRDY is asserted each time a character is transferred form the receive shift register to the receive FIFO. If it is not reset by the CPU, RxRDY remains asserted until the receive FIFO becomes empty, at which time it is automatically negated. If it is reset by the CPU, it will remain negated, regardless of the current state of the receive FIFO, until a new character is transferred from the RxSR to the RxFIFO.

2. If OMR[3] is 1 (FIFO full), RxRDY is asserted:

a. When a character transfer from the receive shift register to the receive FIFO causes it to become full.

b. When a character with a tagged EOM status bit is loaded into the FIFO (BISYNC or BOP) regardless of RxFIFO full condition.

c. When the counter/timer is programmed to count received characters and the character which causes it to reach zero count is loaded into the FIFO (ICTSR[6]).

d. When the beginning of break is detected in ASYNC mode regardless of the RxFIFO full condition.

If it is not reset by the CPU, RxRDY remains asserted until the FIFO becomes empty, at which time it is automatically negated. If it is reset by the CPU, it will remain negated regardless of the current state of the receive FIFO, until it is asserted again due to one of the above conditions.

The assertion of RxRDY causes an interrupt to be generated if IER[4] and the channel's master interrupt enable (ICR[0] or ICR[1]) are asserted.

When DMA operation is programmed, the RxRDY status bit is routed to the DMA control circuitry for use as the channel receiver DMA request. Assertion of RxRDY results in assertion of RTxDRQN output.

Several status bits are appended to each character in the RxFIFO. When the FIFO is read, causing it to be 'popped', the status bits associated with the new character at the top of the RxFIFO are logically ORed into the RSR. Therefore, the user should read RSR before reading the RxFIFO in response to RxRDY activation. If character-by character status is desired, the RSR should be read and cleared each time a new character is received. The user may elect to accumulate status over several characters or over a frame by clearing RSR at appropriate times. This mode would normally also be used when operating in DMA mode. If the RxFIFO is empty when a read is attempted, and wait mode as specified in CMR2[5:3], is not being used, a H'FF' is output on the data bus.

In all modes, the DUSCC protects the contents of the FIFO and the RxSR from overrun. If a character is received while in FIFO is full and a character is already in the RxSR waiting to be transferred into the FIFO, the overrunning character is discarded and the OVERRUN status bit (RSR[5]) is asserted. If the overruning character is an end-of-message character, the character is lost but the FIFOed EOM status bit will be asserted when the character in the RxSR is loaded into the FIFO.

Operation of the receiver is controlled by the enable receiver command. When this command is issued, the DUSCC goes into the search for start bit state (ASYNC), search for SYN state (COP modes), or search for FLAG state (BOP modes). When the disable receiver command is issued, the receiver ceases operation immediately. The RxFIFO is cleared on master reset, or by a rest receiver command. However, disabling the receiver does not affect the RxFIFO, RxRDY, or DMA request operation.

Receiver DCD and RTS Controls

If DCD enable Rx, RPR[2], is asserted, the DCD input must be asserted and the sampling circuit detects that the DCD input has been negated, the receiver ceases operation immediately. Operation resumes when the sampled DCD is asserted again. A change of state detector is provided on the DCD input of each channel. The required duration of the DCD level change is described in the discussion of ICTSR[5]. The user may program a change of state to cause an interrupt to be generated (master interrupt enable ICR[0] or [1] and IER[7] must be set) so that appropriate action can be taken.

In ASYNC mode, RPR[4] can be programmed to control the deactivation of the RTSN output by the receiver. RTSN can be manually asserted and negated by writing to OMR[0]. However, the assertion of RPR[4] causes RTS to be negated automatically upon receipt of a valid start bit if the channel's receive FIFO is already full. When this occurs, the RTSN negated status bit, RSR[6], is set. This may be used as a flow control feature to prevent overrun in the receiver by using the RTSN output signal to control the CTSN input of the remote transmitter. The new character will be assembled in the RxSR, but its transfer to the FIFO will be delayed until the CPU reads the FIFO, making the FIFO position available for the new character.

Once enabled, receiver operation depends on channel protocol mode. The following describes the receiver operation for the various protocols.

RxASYNC Mode

When first enabled, the receiver goes into the search for start bit state, looking for a High-to-Low (mark-to-space) transition of the start bit on the RxD input. If a transition is detected, the state of the RxD pin is sampled again each 16X clock for 71/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again.

If RxD is still Low, a valid start bit assumed and the receiver continues to sample the input at one bit time intervals (16 periods of the 16X Rx clock; one period of the 1X Rx clock) at the theoretical center of the bit, until the proper number of data bits and the parity bit (if specified) have been assembled, and the first stop bit has been detected.

The assembled character is then transferred to the RxFIFO with appended parity error (if parity is specified) and framing error status bits. The DUSCC can be programmed to compare this character to the contents of S1R. The appended character compare status bit, RSR[7], is set if the data matches and there is no parity error.

After the stop bit is sampled, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (i.e., framing error) and RxD remains Low for one-half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

If a break condition is detected (RxD Low for entire character time including optional parity and first stop bit), only one character consisting of all zeros will be loaded into the RxFIFO and break start detect, RSR[2], will be set. The RxD input must return to a High condition for at least one half of a bit time (16X clock mode) or for one bit time (1X clock mode) before the break condition is terminated and the search for the next start bit begins. At that time, the break end detect condition, RSR[3], is set. Note that the maximum speed in the receiver when in asynchronous mode must not exceed 2Mbs.

Rx COP Modes

When the receiver is enabled in COP modes, it first goes into the SYN hunt phase, testing the received data each bit time for receipt of the appropriate SYN bit pattern, Plus parity if specified, to establish character boundaries. Receipt of the SYN bit pattern terminates hunt phase and places the receive in the data phase, in which all leading SYNs are stripped and the RxFIFO begins to load starting with the first non-SYN character. In COP single SYN protocol mode, S1R contains the SYN character required to establish character synchronization. In COP dual SYN and BISYNC protocol modes, S1R and S2R contain the first and second SYN

characters, respectively, required to establish character synchronization. The SYN character length is the same as the character length programmed in RPR[1:0], plus the parity bit if parity is specified. SYN characters received with a parity error, when parity is specified, are considered invalid and will not cause synchronization to be achieved.

In COP mode, resetting the receiver clears the receiver data path, while disabling the receiver does not. If not reset, partial sync patterns remaining in the receiver will be recognized when it is enabled.

If external synchronization is programmed (RPR[4] = 1), the internal SYN detection and special character recognition logic are disabled and receipt of SYN characters is not required. A pulse on the SYNI input pin will establish character synchronization and terminate hunt phase. The SYNI pin is ignored after the first input on the SYNIN pin is received. The receiver must be disabled and then reenabled to resynchronize or to return to normal mode. This must be programmed in conjunction with CMR1[2:0] = 110. Refer to the description of RPR[4] for further details

The SYN detect status bit RSR[2], is set whenever SYN1, SYN1-SYN2, or DLE-SYN1 is detected for single SYN, dual SYN/BISYNC normal, and BISYNC transparent modes, respectively, and the SYNOUT pin will go active for one receive clock period one bit time after SYN detection in HSRH/HSRL. After character sync has been attained, the receiver enters the data phase and assembles characters in the RxSR, beginning with the first non-SYN character, with the least significant bit received first. It computes the BCC if specified, checks parity if specified, and checks for overrun errors.

The operation of the BCC (CRC/LRC) logic depends on the particular COP mode in use. The BCC is initialized upon first entering the data phase. For non-BISYNC modes, all received characters after entering data phase are included in the BCC computation, except for leading SYNs and SYNs which are specified to be stripped by RPR[7]. As each received character is transferred from the RxSR to the FIFO, the current value of the BCC characters is checked and the CRC ERROR status bit (RSR[1]) is set if the value of the CRC remainder is not the expected value. RSR[1] gets set when the character reaches the top of the FIFO. The EOM status bit, RSR[7], is not set since there is no defined end-of-message character. The receiver computes the BCC for test messages automatically when operating in BISYNC protocol mode.

BISYNC Features

The DUSCC provides support for both BISYNC normal and transparent operations. The following summarizes the features provided. Both EBCDIC and ASCII text messages can be handled by the DUSCC as selected by CMR1[5]. The receiver has the capability of recognizing special characters for the BISYNC protocol mode (see Table 15).

All sequences in Table 15, except SOH and STX, when detected explicitly cause a status to be affected. The following describes the conditions when this occurs.

The first character received when entering data phase for a header or text message should be an SOH, an STX, or a DLE-STX two-character sequence. Receipt of any of these initializes the CRC generator and starts the CRC accumulation. The SOH places the receiver in header mode, receipt of the STX places it in text mode, the receipt of the DLE-STX sequence (at any time) automatically places the receiver in transparent mode and sets the XPNT mode status bit, TRSR[0]. There is no explicit status associated with SOH and STX. If any characters are received when entering the data phase, the message is treated as a control message and will not be accumulated in CRC.

After the data phase is established, the receiver searches the data stream for an end of message control character(s):

Header field: ENQ, ETB, or ITB

Normal text field: ENQ, ETX, ETB, or ITB

Transparent text field: DLE-ENQ, DLE-ETX, DLE-ETB, or DLE-ITB

Control message field: EOT, NAK, ACK0, ACK1, WACK, RVI or TTD

Detection of any one of these sequences causes the EOM status bit, RSR[7], to be set. Also if RPR[5] is set and the receiver does not detect a closing PAD (four 1's) after the 'EOT' or 'NAK', the PAD error status bit, RSR[6], is set. When the abort sequence ENQ or DLE-ENQ is detected, the character is tagged with an EOM status and transferred to the FIFO, but the appended CRC error status bit should be ignored. For the other EOM control sequences, the receiver waits for the next two bytes (the CRC bytes) to be received, checks the value of the CRC generator, and tags the transferred character with a CRC error, RSR[1], if the CRC remainder is not correct. See Figure 11 for an example of BCC accumulation in various BISYNC messages.

The CRC bytes are normally not transferred to the FIFO, unless the transfer FCS to FIFO control bit, RPR[6], is asserted. In this case the EOM and CRC error status bits will be tagged onto the last byte of the last FCS byte instead of to the last character of the message. After detecting one of the End-Of-Message (EOM) character sequences and setting RSR[7], the receiver automatically goes into auto hunt mode for the SYNC characters and PAD check if RPR[5] is set.

SYN Pattern Stripping

Leading SYNs (before a message) are always stripped and excluded from the FCS, but SYN patterns within a message are treated by the receiver according to the RPR[7] bit. SYN character patterns are defined for the various COP modes as follows:

COP single SYN mode — SYN1

COP dual SYN mode — SYN1, and SYN2 when immediately preceded by SYN1.

BISYNC normal mode — SYN1, and SYN2 when immediately preceded by SYN1. SYN1 is always stripped, even if it is not followed by SYN2 when stripping is selected.

BISYNC transparent mode — DLE-SYN1, where the DLE is the last of an odd number of consecutive DLEs.

0 Strip only RPR[7] leading the SYN and do not accumulate in FCS.

1 Strip all SYNs. Additionally, strip odd DLEs when operating in BISYNC transparent mode. Do not accumulate stripped characters in FCS.

Processing of the SYN patterns is determined by the RPR[7] bit, the COP mode, and the position of the pattern in the frame. This is summarized in Table 16.

The value of the RPR[7] field does not affect the setting of the SYN DETECT status bit, RSR[2], and the generation of a SYNOUT pulse when a SYN pattern is received.

RxBOP Mode

In BOP protocol mode, the receiver may be in any one of four phases: hunt phase, address field (A) phase, control field (C) phase,

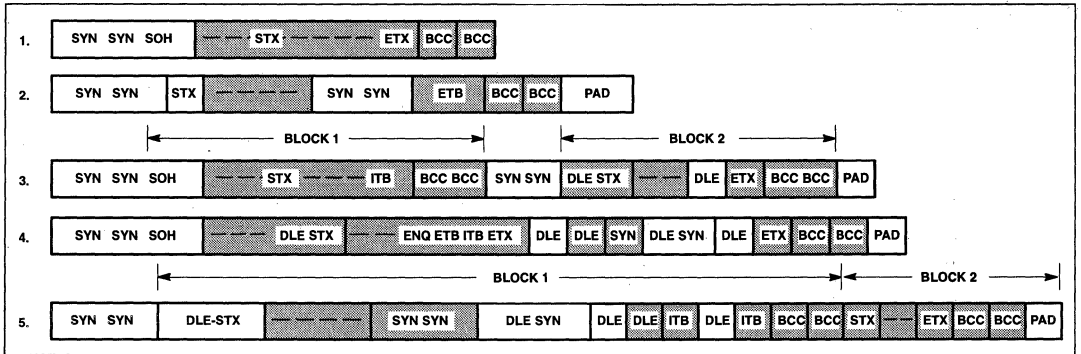
or information field (I) phase. The character length for the A and C phases is always 8 bits. The I field character length is specified in RPR[1:0].

Note that if the residual character length is not zero, the unused most significant bits in the receiver FIFO are not necessarily zero. the unused bits should be ignored, this will not cause a CRC error.

After an enable receiver command is executed, the receiver enters hunt phase, in which a comparison for the string (01111110) is done every Rx bit time. The FLAG delineates the beginning (and end) of a received frame and establishes the character boundary. Each FLAG match in CCSR causes the FLAG detect status bit (RSR[2]) to be set and SYNOUTN pin to be activated one bit time later for one receive clock period. FLAGs with an overlapping zero will be detected. All FLAGs are deleted from the data stream.

Table 15. BISYNC Features

BISYNC — Single-Character Sequences			
Sequences	**ASCII**	**EBCDIC**	**Description**
SOH	H'01'	H'01'	Start of header
STX	H'02'	H'02'	Start of text
ETX	H'83'	H'03'	End of text
EOT	H'04'	H'37'	End of transmission
ENQ	H'85'	H'2D'	Enquiry
DLE	H'10'	H'10'	Data link escape
NAK	H'15'	H'3D'	Negative ack
ETB	H'97'	H'26'	End of transmission block
ITB	H'1F'	H'1F'	End of intermediate transmission block
BISYNC — Two-Character Sequences			
Sequence	**ASCII**	**EBCDIC**	**Description**
ACK0	H'10,B0'	H'10,70'	Acknowledge 0
ACK1	H'10,31'	H'10,61'	Acknowledge 1
WACK	H'10,3B'	H'10,6B'	Wait before transmit positive ack
RVI	H'10,BC'	H'10,7C'	Reverse interrupt
TTD	H'02,85'	H'02,2D'	Temporary text delay
BISYNC — (Transparent Text Mode) — Two-Character Sequences			
Sequence	**ASCII**	**EBCDIC**	**Description**
DLE-ENQ	H'10,85'	H'10,2D'	Enquiry
DLE-ITB	H'10,1F'	H'10,1F'	End of intermediate transmission block
DLE-ETB	H'10,97'	H'10,26'	End of transmission block
DLE-ETX	H'10,83'	H'10,03'	End of text
DLE-STX	H'10,02'	H'10,02'	Start of transparent text mode



NOTES:
3. The BCC accumulator is stopped after the end of message character sequence is accumulated. All shaded areas are accumulated.
4. ENQ (DLE - ENQ) in a text message should be treated as an abort.
5. Opening SYNs will be stripped by the receiver.

Figure 12. Example of BCC Accumulation in Various BISYNC Messages

Table 16. SYN Pattern Processing

MODE	RPR [7]	LEADING SYNs	WITHIN A MESSAGE
BISYNC	0	no FCS no FIFO	no FCS Pattern into FIFO
	1	no FCS no FIFO	no FCS no FIFO Accumulate in FCS
COP	0	no FCS no FIFO	Pattern into FIFO no FCS no FIFO
	1	no FCS no FIFO	

Once a FLAG has been detected, the receiver will exit hunt phase and enter address phase. The handling of the address field is determined by the values programmed in CMR1[2:0], which selects one of the BOP modes. The BOP secondary address modes are selected by CMR1[4:3] and function as in the description that follows.

Single-Octet Address
For receive, the address comparison for a secondary station is made on the first octet following the opening FLAG. A match occurs if the first octet after the FLAG matches occurs if the first octet after the FLAG matches the contents of S1R, or if all parties address (RPR[3]) is asserted and the first octet is equal to H'FF'.

Dual Octet Address
For receive, the address comparison for a secondary station is made on the first two octets following the opening FLAG.

A match occurs if the first two octets after the FLAG match the contents of S1R and S2R respectively, or if all parties address (RPR[3]) is asserted and the first two octets are equal to H'FF, FF'.

Dual Address with Group Mode
For receive, the address comparison for a secondary station is made on the first two octets following the opening FLAG. A match occurs for one of three possible conditions. If the first two octets after the FLAG match the contents of S1R and S2R, respectively, or if the first octet is H'FF' and the second matches the contents of S2R (group mode), or when all parties address (RPR[3]) is asserted and the first two octets are equal to H'FF,FF'. The second condition (group mode) allows a selected group of stations to receive a message.

Extended Address Mode
Extend address field to the next octet if the LSB of the current address octet is zero. Address field is terminated if the LSB of the address is a one. The address field will be terminated after the first octet if the null address H'00' is received/transmitted as the first address octet. For this mode the receiver does not perform an address comparison (all received characters after the opening FLAG are transferred to the FIFO) but does determine when the address field is terminated.

The length of the A field may be a single octet, a dual octet, or more octets, as described above. A primary station or an extended address secondary station does not perform an address comparison, and all characters in the A, C, and I fields after the flag are transferred to the FIFO. Although address field comparisons are not performed, the length of the address field is still determined by CMR1[4:3]. For the other secondary address modes, if there is a match, or the received character(s) match either of the other enabling conditions (group or all-parties address), all characters in the A, C, and I field are transferred to the FIFO. If there is no match, the receiver returns to the FLAG hunt phase.

C phase begins after A phase is terminated. The receiver receives one or two control characters, CMR1[5]. After this phase is terminated, the character length is switched automatically from 8 bits to the number of bits specified in RPR[1:0] and the information field phase is entered.

The frame is terminated when a closing FLAG is detected. The same FLAG can also serve as the opening FLAG of the next frame. The 16 bits received prior to the closing FLAG form the frame check sequence (if an FCS is specified in CMR2[2:0]). All non-FLAG characters of the frame are accumulated in the CRC checker and the result is compared to the expected remainder. Failure to match will cause a CRC error. EOM detect RSR[7], RCL not zero RSR[0], and CRC error RSR[1] are normally FIFOed with the last character of the I field. RCL not zero RSR[0] is set if the length of the last character of the I field does not have the length programmed in RPR[1:0]. The residual character length in TRSR[2:0] is also valid at that time. The CRC characters themselves are normally not passed to the RxFIFO. However, if the transfer FCS to FIFO control bit RPR[6] is asserted, the FCS bytes will be transferred to the FIFO. In this case the EOM, CRC error, and RCL not zero status bits will be tagged onto the last byte of the CRC sequence instead of to the last character of the message.

If the closing FLAG is received prior to receipt of the appropriate number of A field, C field as programmed in CMR1[5:3], and FCS field octets, a short frame will be detected and RSR[4] will be set. The I field need not be present in a valid frame. An abort (11111110) comparison is done after an opening FLAG has been received and up to receipt of the closing FLAG. A match causes the abort detect status bit (RSR[6]) to be set. The receiver then enters FLAG search mode. The abort is stripped from the received data stream.

If a zero followed by 15 contiguous ones is detected, the idle detect status bit RSR[3] is set. This comparison is done whenever the receiver is enabled. Therefore, it can occur before or after a received frame.

Zero deletion is performed during BOP receive. A zero after 5 contiguous ones is deleted from the data stream regardless of character boundaries. Deleted zeros are not subject to CRC accumulation. FLAG, ABORT, and IDLE comparisons are done prior to zero deletion.

If external synchronization is programmed (RPR[4] - 1), the internal FLAG detection and address comparison logic is disabled and receipt of FLAGs is not required. In this arrangement, a pulse on the SYNI-N input pin will establish synchronization and terminate hunt phase. The receiver will then go immediately into the I-field mode with zero deletion disabled, assembling and transferring characters into the FIFO with the character length specified in RPR[1:)]. The SYNI-N pin is ignored after the first input on the SYNI-N pin is received. The receiver must be disabled and then reenabled to resynchronize or to return to normal operating mode.

This mode must be programmed in conjunction with CMR1[2:0] = 110. Refer to the description of RPR[4] for further details.

BOP Loop Mode
Operation of the receiver in BOP loop protocol mode is similar to operation in other BOP modes, except that only certain frame

formats are supported. Several character detection functions that interact with the operation of the transmitter commands are added:

1. When the 'go on-loop' command is invoked, the receiver looks for the receipt of a zero followed by seven ones and then asserts the LCN output.
2. When the 'go off-loop' command is invoked, the receiver looks for the receipt of eight contiguous ones and then negates the LCN output.
3. The TxD output normally echoes the receive input with a two bit time delay. When the 'go active on poll' command is asserted, the receiver looks for an EOP (a zero followed by seven ones) and then switches the TxD output line to the normal transmitter output. Receipt of an EOP or an ABORT sets RSR[6].
4. Receipt of a turnaround sequence (eight contiguous zeros) terminates the transmitter operation, if any, and returns the TxD output to echoing the RxD input. RSR[3] is set if a turnaround is received.

See transmitter operation for additional details.

SUMMARY OF COP FEATURES

COP Dual SYN Mode	
SYN detect	SYN1-SYN2
Linefill	SYN1-SYN2
SYN stripping	SYN1-SYN2 used to establish character sync, i.e., leading SYNs. Subsequent to this (after receiving first non-SYN character), SYN1 and SYN1-SYN2 if stripping is specified by RPR[7].
Excluded form FCS**	SYN1 and SYN1-SYN2 before beginning of message, i.e., leading SYNs and, if SYN stripping is specified by RPR[7] anywhere else in the message for the Rx; linefill SYN1-SYN2 for Tx regardless of RPR[7]. (If SYN stripping is not specified, then SYNs within a message will be included in FCS by Rx.)
BISYNC normal mode	
SYN detect	SYN1-SYN2
Linefill	FYN1-SYN2
SYN stripping	SYN1-SYN2 used to establish character sync, i.e., leading SYNs. Subsequent to this (after receiving first non-SYN character), SYN1 and SYN1-SYN2 if stripping is specified by RPR[7].
Excluded from FCS	All SYNs either before or within a message, regardless of RPR[7], plus additional characters as required by the protocol.
BISYNC transparent mode	
SYN detect	*DLE-SYN1
Linefill	*DLE-SYN1
SYN/DLE stripping	*DLE-SYN1 and odd DLEs if stripping is specified by RPR[7].
Excluded from FCS	*DLE-SYN1 and odd DLEs, regardless of RPR[7] plus additional characters as required by the protocol.
COP single SYN mode	
SYN detect	SYN1
Linefill	SYN1
SYN stripping	SYN1 used to establish character sync, i.e., leading SYNs. Subsequent to this, SYN1 if stripping is specified by RPR[7].
Excluded from FCS**	SYN1 before beginning of message, i.e., leading SYNs, and if SYN stripping is specified by RPR[7], anywhere else in the message for the Rx; linefill SYN1 for Tx regardless of RPR[7]. (If SYN stripping is not specified, then SYNs within a message will be included in FCS by Rx.)

NOTES:

* DLE indicates last DLE of an odd number of consecutive DLEs.

** In non-BISYNC COP modes (single or dual SYN case), if SYN stripping is off, i.e., RPR[7] = 0, then SYNs within a message will be included in FCS by receiver. Therefore, the remote DUSCC transmitter should be careful not to let the TxFIFO underrun since the linefill SYN characters are not accumulated in FCS by the transmitter regardless of RPR[7]. Letting the TxFIFO underrun will result in a CRC error in the receiver.

Section 5
Linear Data Communications Data Sheets

CONTENTS

EIA-232-D/V.28 driver/receiver | MC145406

DESCRIPTION

The MC145406 is a silicon-gate CMOS IC that combines 3 drivers and 3 receivers to fulfill the electrical specifications of standards EIA-232-D and CCITT V.28. The drivers feature true TTL input compatibility, slew-rate limited output, 300Ω power-off source impedance, and output typically switching to within 25% of the supply rails. The receivers can handle up to ±25V while presenting 3 to 7kΩ impedance. Hysteresis in the receiver aids reception of noisy signals. By combining both drivers and receivers in a single CMOS chip, the MC145406 provides efficient, low-power solutions for EIA-232-D and V.28 applications.

APPLICATIONS

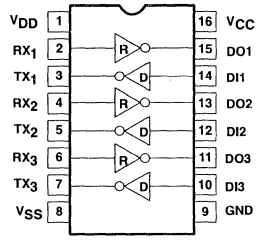
- Modem interface
- Voice/data telephone interface
- Lap-top computers
- UART interface

FEATURES

- **Drivers**
- ±5 to ±12V supply range
- 300Ω power-off source impedance
- Output current limiting
- TTL compatible
- Maximum slew rate = 30V/µs
- **Receivers**
- ±25V input voltage range over the full supply range
- 3 to 7kΩ input impedance
- Hysteresis on input switchpoint
- **General**
- Very low supply currents for long battery life
- Operation is independent of power supply sequencing

PIN CONFIGURATION

D and N Packages



NOTE:
D = Driver
R = Receiver

ORDERING INFORMATION

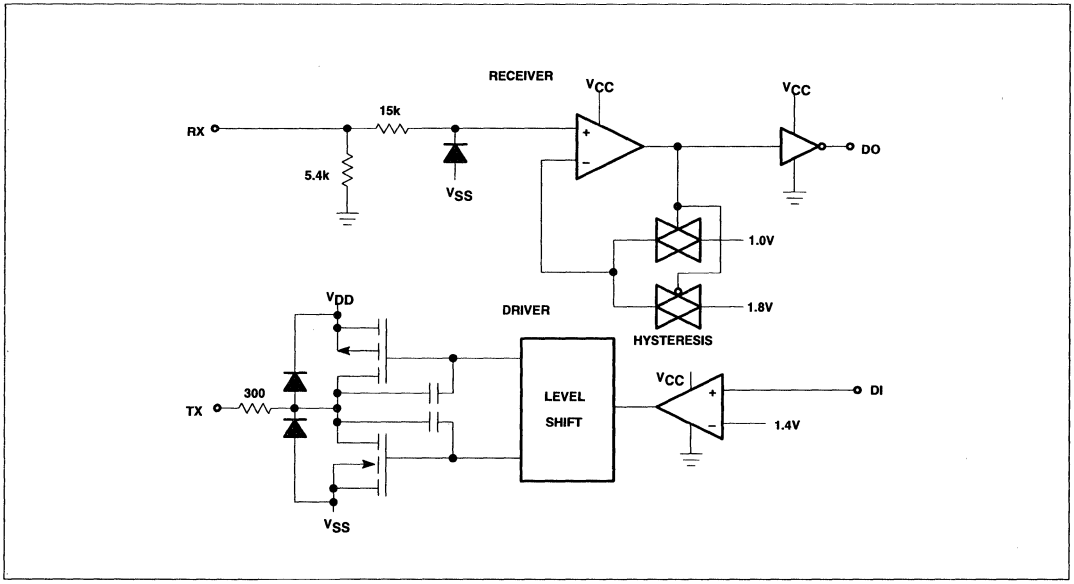
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line (DIP) Package	0 to +70°C	MC145406N	0406C
16-Pin Small Outline Large (SOL) Package	0 to +70°C	MC145406D	0171B

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +6.0	V
V_{DD}	Supply voltage	-0.5 to +13.5	V
V_{SS}	Supply voltage	+0.5 to -13.5	V
V_{IR}	Input voltage range RX_{1-3} inputs DI_{1-3} inputs	 (V_{SS} - 15) to (V_{DD} + 15) -0.5 to (V_{CC} + 0.5)	V
	DC current per pin	±100	mA
P_D	Power dissipation (package)	1.0	W
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
θ_{JA}	Thermal impedance N package D package	80 105	°C/W

NOTE: This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range GND ≤ V_{DI} ≤ V_{DD} and GND ≤ V_{DO} ≤ V_{CC}. Also, the voltage at the RX pin should be constrained to ±25V, and TX should be constrained to V_{SS} ≤ V_{TX1-3} ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI, and V_{SS} or V_{DD} for RX).

BLOCK DIAGRAM



PIN #	SYMBOL	PIN DESCRIPTION
1	V_{DD}	**Positive power supply.** The most positive power supply pin, which is typically 5 to 12 volts.
8	V_{SS}	**Negative power supply.** The most negative power supply pin, which is typically -5 to -12 volts.
16	V_{CC}	**Digital power supply.** The digital supply pin, which is connected to the logic power supply (maximum +5.5V).
9	GND	**Ground.** Ground return pin is typically connected to the signal ground pin of the EIA-232-D connector (Pin 7) as well as to the logic power supply ground.
2, 4, 6	RX_1, RX_2, RX_3	**Receive Data Input.** These are the EIA-232-D receive signal inputs whose voltages can range from +25 to -25V. A voltage between +3 and +25 is decoded as a space and causes the corresponding DO pin to swing to ground (0V); a voltage between -3 and -25V is decoded as a mark and causes the DO pin to swing up to V_{CC}. The actual turn-on input switchpoint is typically biased at 1.8V above ground, and includes 800mV of hysteresis for noise rejection. The nominal input impedance is 5kΩ. An open or grounded input pin is interpreted as a mark, forcing the DO pin to V_{CC}.
11, 13, 15	DO1, DO2, DO3	**Data Output.** These are the receiver digital output pins, which swing from V_{CC} to GND. A space on the RX pin causes DO to produce a logic zero; a mark produces a logic one. Each output pin is capable of driving one LSTTL input load.
10, 12, 14	DI1, DI2, DI3	**Data Input.** These are the high-impedance digital input pins to the drivers. TTL compatibility is accomplished by biasing the input switchpoint at 1.4V above ground. However, 5V CMOS compatibility is maintained as well. Input voltage levels on these pins must be between V_{CC} and GND.
3, 5, 7	TX1, TX2, TX3	**Transmit Data Output.** These are the EIA-232-D transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic one at a DI input causes the corresponding TX output to swing toward V_{SS}. A logic zero causes the output to swing toward V_{DD} (the output voltages will be slightly less than V_{DD} or V_{SS} depending upon the output load). Output slew rates are limited to a maximum of 30V/μs. When the MC145406 is off (V_{DD} = V_{SS} = V_{CC} = GND), the minimum output impedance is 300Ω.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.5 to +6.0	V
V_{DD}	Supply voltage	-0.5 to +13.5	V
V_{SS}	Supply voltage	+0.5 to -13.5	V
V_{IR}	Input voltage range RX_{1-3} inputs DI_{1-3} inputs	 $(V_{SS} - 15)$ to $(V_{DD} + 15)$ -0.5 to $(V_{CC} + 0.5)$	V
	DC current per pin	±100	mA
P_D	Power dissipation (package)	1.0	W
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
θ_{JA}	Thermal impedance N package D package	80 105	°C/W

NOTE: This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range GND ≤ V_{DI} ≤ V_{DD} and GND ≤ V_{DO} ≤ V_{CC}. Also, the voltage at the RX pin should be constrained to ±25V, and TX should be constrained to V_{SS} ≤ V_{TX1-3} ≤ V_{DD}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI, and V_{SS} or V_{DD} for RX).

DC ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; GND = 0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
DC supply voltage						
V_{DD}			4.5	5 to 12	13.2	V
V_{SS}			-4.5	-5 to -12	-13.2	V
V_{CC}			4.5	5.0	5.5	V
Quiescent supply current (outputs unloaded, inputs low)						
I_{DD}		V_{DD} = +12V		20	400	µA
I_{SS}		V_{SS} = -12V		280	600	µA
I_{CC}		V_{CC} = +5V		260	450	µA

RECEIVER ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; GND = 0V; V_{DD} = +5 to +12V; V_{SS} = -5 to -12V; V_{CC} = +5V ±5%, unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNITS
				MIN	TYP	MAX	
V_{ON}	Input turn-on threshold	RX_{1-3}	$V_{DO1-3} = V_{OL}$, V_{CC} = 5.0V ±5%	1.35	1.80	2.35	V
V_{OFF}	Input turn-off threshold	RX_{1-3}	$V_{DO1-3} = V_{OH}$, V_{CC} = 5.0V ±5%	0.75	1.00	1.25	V
V_{ON}-V_{OFF}	Input threshold hysteresis	RX_{1-3}	V_{CC} = 5.0V ±5%	0.6	0.8		V
R_{IN}	Input resistance	RX_{1-3}	$(V_{SS}$-15V) ≤ V_{RX1-3} ≤ $(V_{DD}$+15V)	3.0	5.0	7.0	kΩ
V_{OH}	High level output voltage V_{RX1-3} = -3V to $(V_{SS}$-15V)[1]	DO_{1-3}	I_{OH} = -20µA, V_{CC} = +5.0V	4.9	5.0		V
			I_{OH} = -1mA, V_{CC} = +5.0V	3.8	4.4		
V_{OL}	Low level output voltage V_{RX1-3} = +3V to $(V_{DD}$+15V)[1]	DO_{1-3}	I_{OL} = +20µA, V_{CC} = +5.0V		0.005	0.1	V
			I_{OL} = +2mA, V_{CC} = +5.0V		0.15	0.5	
			I_{OL} = +4mA, V_{CC} = +5.0V		0.3	0.7	

NOTE:
1. This is the range of input voltages as specified by EIA-232-D to cause a receiver to be in the high or low logic state.

DRIVER ELECTRICAL CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; GND = 0V; V_{CC} = +5V ±5%, unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNITS
				MIN	TYP	MAX	
V_{IL}	Digital input voltage	DI_{1-3}	Logic 0			0.8	V
V_{IH}	Digital input voltage	DI_{1-3}	Logic 1	2.0			V
I_{IN}	Input current	DI_{1-3}	$V_{DI1-3} = V_{CC}$			±1.0	µA
V_{OH}	Output high voltage V_{DI1-3} = Logic 0, R_L = 3.0kΩ	TX_{1-3}	V_{DD} = +5.0V, V_{SS} = -5.0V	3.5	4.1		V
			V_{DD} = +6.0V, V_{SS} = -6.0V	4.3	5.0		
			V_{DD} = +12.0V, V_{SS} = -12.0V	9.2	10.4		
V_{OL}	Output low voltage[1] V_{DI1-3} = Logic 0, R_L = 3.0kΩ	TX_{1-3}	V_{DD} = +5.0V, V_{SS} = -5.0V	-4.0	-4.3		V
			V_{DD} = +6.0V, V_{SS} = -6.0V	-4.5	-5.2		
			V_{DD} = +12.0V, V_{SS} = -12.0V	-10.0	-10.3		
	Off source resistance Figure 1	TX_{1-3}	V_{DD}=V_{SS}=GND=0V, V_{TX1-3} = ±2.0V	300			Ω
I_{SC}	Output short-circuit current V_{DD} = +12.0V, V_{SS} = -12.0V	TX_{1-3}	TX_{1-3} shorted to GND[2]		±22	+60	mA
			TX_{1-3} shorted to ±15.0V[3]		±60	±100	mA

NOTE:
1. The voltage specifications are in terms of absolute values.
2. Specification is for one TX output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits will be exceeded.
3. This condition could exceed package limitations.

SWITCHING CHARACTERISTICS

Typical values are at T_A = 0 to 70°C; V_{CC} = +5V ±5%, unless otherwise specified. (See Figures 2 and 3)

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNITS
				MIN	TYP	MAX	
Drivers							
t_{PLH}	Propagation delay time	TX_{1-3}	Low-to-High R_L = 3kΩ, C_L = 50pF		300	500	ns
t_{PHL}	Propagation delay time	TX_{1-3}	High-to-Low R_L = 3kΩ, C_L = 50pF		300	500	ns
SR	Output slew rate (minimum load)	TX_{1-3}	R_L = 7kΩ, C_L = 0pF, V_{DD} = 6 to 12.0V, V_{SS} = -6 to -12V		±6	±30	V/µs
	Output slew rate (maximum load)	TX_{1-3}	R_L = 7kΩ, C_L = 2500pF, V_{DD} = 12V, V_{SS} = -12V		±3.0		
Receivers (C_L = 50pF)							
t_{PLH}	Propagation delay time	DO_{1-3}	Low-to-High		150	425	ns
t_{PHL}	Propagation delay time	DO_{1-3}	High-to-Low		150	425	ns
t_R	Output rise time	DO_{1-3}			120	400	ns
t_F	Output fall time	DO_{1-3}			40	100	ns

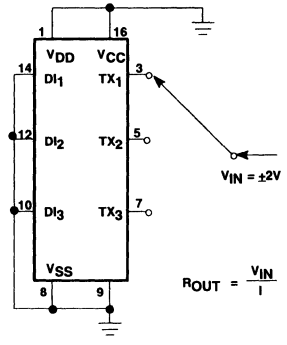


Figure 1. Power-Off Source Resistance (Drivers)

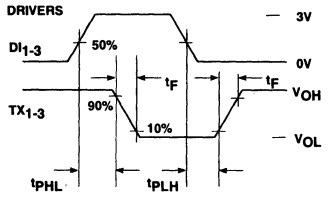


Figure 2. Switching Characteristics

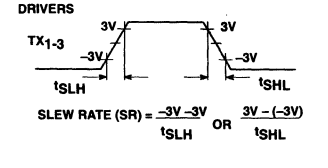


Figure 3. Slew Rate Characteristics

APPLICATIONS INFORMATION

The MC145406 has been designed to meet the electrical specifications of standards EIA-232-D/CCITT V.28 and as such, defines the electrical and physical interface between Data Communication Equipment (DCE) and Data Terminal Equipment (DTE). A DCE is connected to a DTE using a cable that typically carries up to 25 leads, which allow the transfer of timing, data, control, and test signals. The MC145406 provides the necessary level shifting between the TTL/CMOS logic levels and the high voltage levels of EIA-232-D (ranging from ±3 to ±25V).

DRIVERS

As defined by the specification, an EIA-232-D driver presents a voltage of between ±5 to ±15V into a load of between 3 to 7kΩ. A logic one at the driver input results in a voltage of between -5 to -15V. A logic zero results in a voltage between ±5 to ±15V. When operating at ±7 to ±12V, the MC145406 meets this requirement. When operating at ±5V, the MC145406 drivers produce less than ±5V at the output (when terminated), which does not meet the EIA-232-D specification. However, the output voltages when using a ±5V power supply are high enough (around ±4V) to permit proper reception by an EIA-232-D receiver, and can be used in applications where strict compliance to EIA-232-D is not required.

Another requirement of the MC145406 drivers is that they withstand a short to another driver in the EIA-232-D cable. The worst-case condition that is permitted by EIA-232-D is a ±15V source that is current limited to 500mA. The MC145406 drivers can withstand this condition momentarily. In most short circuit conditions the source driver will have a series 300Ω output impedance needed to satisfy the EIA-232-D driver requirements. This will reduce the short circuit current to under 40mA which is an acceptable level for the MC145406 to withstand.

Unlike some other drivers, the MC145406 drivers feature an internally-limited output slew rate that does not exceed 30V/µs.

RECEIVERS

The job of an EIA-232-D receiver is to level-shift voltages in the range of -25 to +25V down to TTL/CMOS logic levels (0 to +5V). A voltage of between -3 and -25V on RX_1 is defined as a mark and produces a logic one at DO_1. A voltage between +3 and +25V is a space and produces a logic zero. While receiving these signals, the RX inputs must present a resistance between 3 and 7kΩ. Nominally, the input resistance of the RX_{1-3} inputs is 5.0kΩ.

The input threshold of the RX_{1-3} inputs is typically biased at 1.8V above ground (GND) with typically 800mV of hysteresis included to improve noise immunity. The 1.8V bias forces the appropriate DO pin to a logic one when its RX input is open or grounded as called for in EIA-232-D specification. Notice that TTL logic levels can be applied to the RX inputs in lieu of normal EIA-232-D signal levels. This might be helpful in situations where access to the modem or computer through the EIA-232-D connector is necessary with TTL devices. However, it is important not to connect the EIA-232-D outputs (TX_1) to TTL inputs since TTL operates off +5V only, and may be damaged by the high output voltage of the MC145406.

The DO outputs are to be connected to a TTL or CMOS input (such as an input to a modem chip). These outputs will swing from V_{CC} to ground, allowing the designer to operate the DO and DI pins from the digital power supply. The TX and RX sections are independently powered by V_{DD} and V_{SS} so that one may run logic at +5V and the EIA-232-D signals at ±12V.

Octal line driver — NE5170

DESCRIPTION

The NE5170 is an octal line driver which is designed for digital communications with data rates up to 100kb/s. This device meets all the requirements of EIA standards RS-232C/RS-423A and CCITT recommendations V.10/X.26. Three programmable features:

(1) output slew rate, (2) output voltage level, and (3) three-state control (high-impedance) are provided so that output characteristics may be modified to meet the requirements of specific applications.

FEATURES

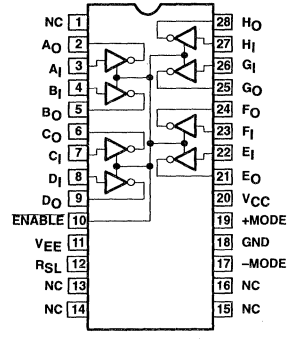
- Meets EIA RS-232C/423A and CCITT V.10/X.26
- Simple slew rate programming with a single external resistor
- 0.1 to 10V/μs slew rate range
- High/low programmable voltage output modes
- TTL compatible inputs

APPLICATIONS

- High-speed modems
- High-speed parallel communications
- Computer I/O ports
- Logic level translation

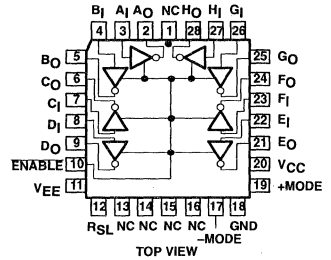
PIN CONFIGURATION

N Package



TOP VIEW

A Package



TOP VIEW

FUNCTION TABLE

ENABLE	Logic Input	OUTPUT VOLTAGE (V)		
		RS-423A[1]	RS-232C	
			Low Output Mode[1]	High Output Mode[2]
L	L	5 to 6V	5 to 6V	≥ 9V
L	H	–5 to 6V	–5 to 6V	≤ –9V
H	X	High-Z	High-Z	High-Z

NOTES:
1. V_{CC} = +10V and V_{EE} = –10V; R_L = 3kΩ
2. V_{CC} = +12V and V_{EE} = –12V; R_L = 3kΩ

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
28-Pin Plastic Dual In-Line (DIP) Package	0 to +70°C	NE5170N	0408B
28-Pin Plastic Lead Chip Carrier (PLCC) Package	0 to +70°C	NE5170A	0401F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage and + MODE	15	V
V_{EE}	Supply voltage and – MODE	–15	V
I_{OUT}	Output current[1]	±150	mA
V_{IN}	Input voltage ($\overline{\text{Enable}}$, Data)	–1.5 to +7	V
V_{OUT}	Output voltage[2]	±15	V
	Minimum slew resistor[3]	1	kΩ
P_D	Power dissipation	1200	mW

NOTES:
1. Maximum current per driver. Do not exceed maximum power dissipation if more than one output is on.
2. High impedance mode.
3. Minimum value of the resistor used to set the slew rate.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ±10%; V_{EE} = –10V ±10%; ±MODES = 0V; R_{SL} = 2kΩ, 0°C ≤ T_A ≤ 70°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
V_{OH}	Output high voltage	V_{IN} = 0.8V, R_L = 3kΩ[2]	5	6	V
		R_L = 450Ω[2]	4.5	6	
		R_L = 3kΩ[3], C_L = 2500pF	V_{CC}–3		
V_{OL}	Output low voltage	V_{IN} = 2.0V, R_L = 3kΩ[2]	–6	–5	V
		R_L = 450Ω[2]	–6	–4.5	
		R_L = 3kΩ[3], C_L = 2500pF		V_{EE}+3	
V_{OU}	Output unbalance voltage	V_{CC} = |V_{EE}|, R_L = 450Ω[2]		0.4	V
I_{CEX}	Output leakage current	|V_O| = 6V, ENABLE = 2V or V_{CC} = V_{EE} = 0V	–100	100	µA
V_{IH}	Input high voltage		2.0		V
V_{IL}	Input low voltage			0.8	V
I_{IL}	Logic "0" input current	V_{IN} = 0.4V	–400	0	µA
I_{IH}	Logic "1" input current	V_{IN} = 2.4V	0	40	µA
I_{OS}	Output short circuit current[1]	V_O = 0V	–150	150	mA
V_{CL}	Input clamp voltage	I_{IN} = –15mA	–1.5		V
I_{CC}	Supply current	NO LOAD		35	mA
I_{EE}		NO LOAD	–45		mA

NOTES:
1. Maximum current per driver. Do not exceed maximum power dissipation if more than one output is on.
2. V_{OH}, V_{OL} at R_L = 450Ω will be ≥ 90% of V_{OH}, V_{OL} at R_L = ∞.
3. High Output Mode; +MODE pin = V_{CC}; –MODE pin = V_{EE}; 9V ≤ V_{CC} ≤ 13V; –9V ≥ V_{EE} ≥ –13V.

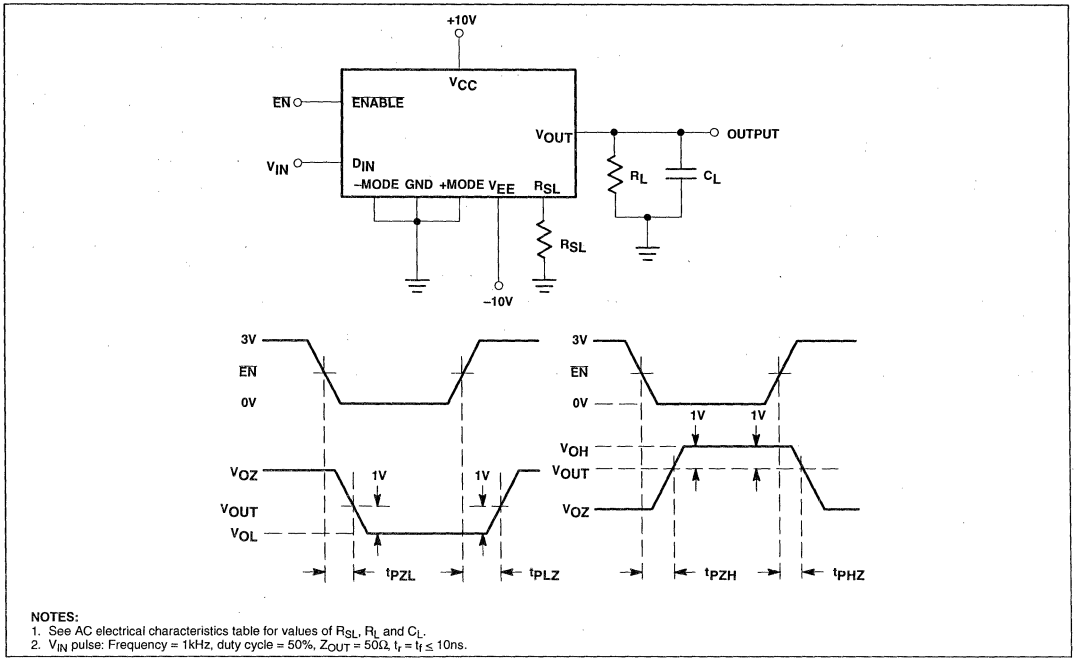
AC ELECTRICAL CHARACTERISTICS

V_{CC} = +10V; V_{EE} = −10V; Mode = GND, 0°C ≤ T_A ≤ 70°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_{PLZ}	Propagation delay output high to high impedance	R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		5	µs
t_{PLZ}	Propagation delay output low to high impedance	R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		5	µs
t_{PZH}	Propagation delay high impedance to high output	R_{SL} = 200k R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		150	µs
t_{PZL}	Propagation delay high impedance to low output	R_{SL} = 200k R_L = 450, C_L = 50pF or R_L = 3k, C_L = 2500pF		150	µs
SR	Output slew rate	R_{SL} = 2k	8	12	V/µs
		R_{SL} = 20k	0.8	1.2	
		R_{SL} = 200k	0.06	0.14	

NOTE:
SR: Load condition. (A) For R_{SL} < 4kΩ use R_L = 450Ω; C_L = 50pF; (B) for R_{SL} > 4kΩ use either R_L = 450Ω, C_L = 50pF or R_L = 3kΩ, C_L = 2500pF.

AC PARAMETER TEST CIRCUIT AND WAVEFORMS



NOTES:
1. See AC electrical characteristics table for values of R_{SL}, R_L and C_L.
2. V_{IN} pulse: Frequency = 1kHz, duty cycle = 50%, Z_{OUT} = 50Ω, $t_r = t_f \leq 10$ns.

SLEW RATE PROGRAMMING

Slew rate for the NE5170 is set using a single external resistor connected between the R_{SL} pin and ground. Adjustment is made according to the formula:

$$R_{SL} \text{ (in k}\Omega) = \frac{20}{\text{Slew Rate}}$$

where the slew rate is in V/μs. The slew resistor can vary between 2 and 200kΩ which gives a slew rate range of 10 to 0.1V/μs. This adjustment of the slew rate allows tailoring output characteristics to recommendations for cable length and data rate found in EIA standard RS–423A. Approximations for cable length and data rate are given by:

Max. data rate (in kb/s) = 300/t

Cable length (in feet) = 100×t

where t is the rise time in microseconds. The absolute maximum data rate is 100kb/s and the absolute maximum cable length is 4000 feet.

OUTPUT MODE PROGRAMMING

The NE5170 has two programmable output modes which provide different output voltage levels. The low output mode meets the specifications of EIA standards RS–423A and RS–232C. The high output mode meets the specifications of RS–232C only, since higher output voltages result from programming this mode. The high output mode provides the greater output voltages where higher attenuation levels must be tolerated. Programming the high output mode is accomplished by connecting the +MODE pin to V_{CC} and the –MODE pin to V_{EE}. The low output mode results when both of these pins are connected to ground.

APPLICATION

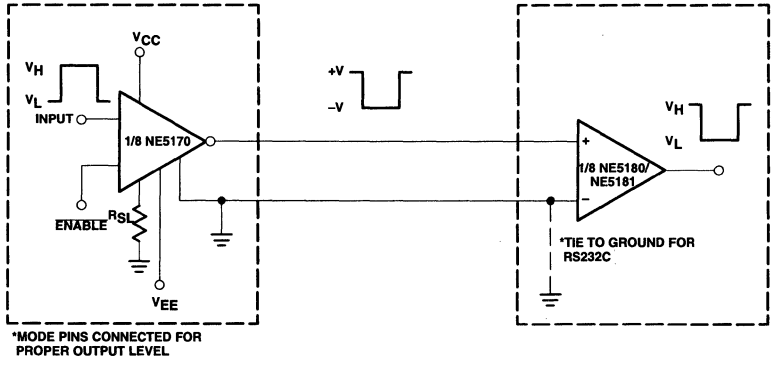


Figure 1. RS-232C/RS-423A Data Transmission

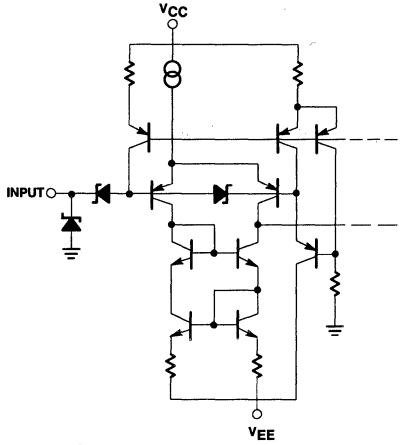


Figure 2. Input Stage Schematic

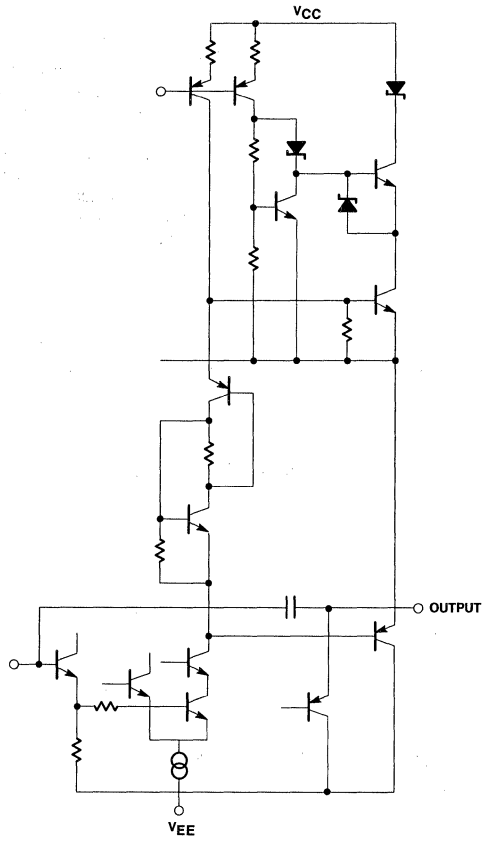


Figure 3. Output Stage Schematic

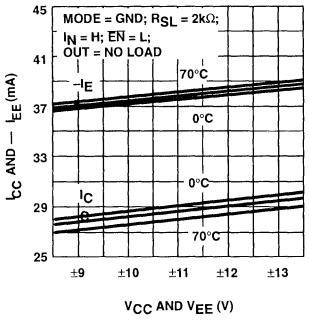


Figure 4. Typical I_{CC} and I_{EE} vs Supply Voltages

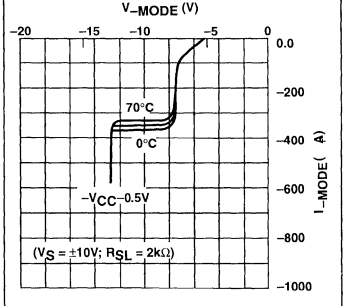


Figure 7. Typical –MODE Current vs –MODE Voltage

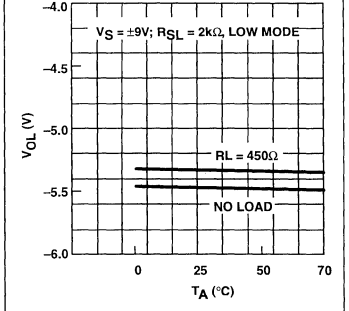


Figure 10. Typical Output Low Voltage vs Temperature

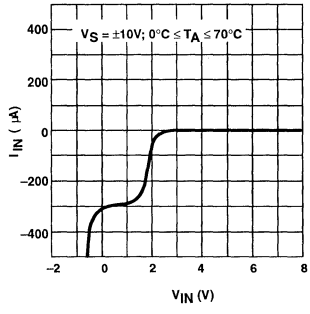


Figure 5. Typical Input Current vs Input Voltage

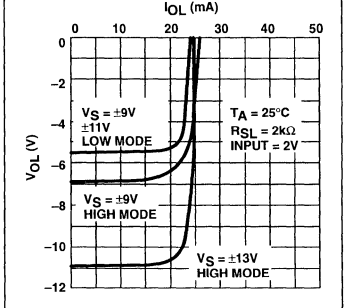


Figure 8. Typical Output Low Voltage vs Load Current

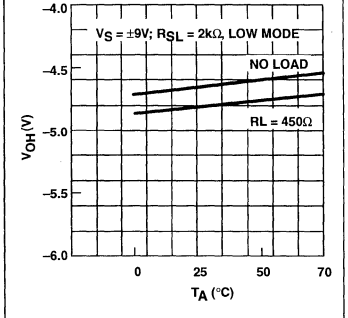


Figure 11. Typical Output High Voltage vs Temperature

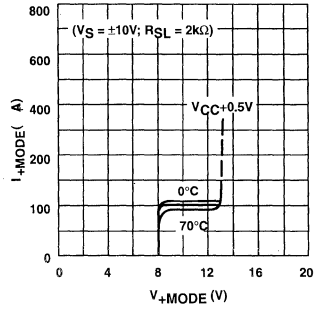


Figure 6. Typical +MODE Current vs +MODE Voltage

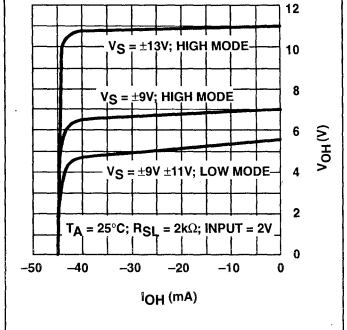


Figure 9. Typical Output High Voltage vs Load Current

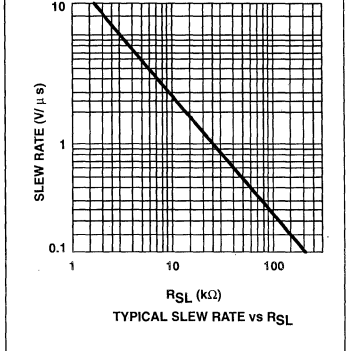


Figure 12. Typical Slew Rate vs R_{SL}

Octal differential line receiver | NE5180/NE5181

DESCRIPTION

The NE5180 and NE5181 are octal line receivers designed to interface data terminal equipment with data communications equipment. These devices meet the requirements of EIA standards RS-232C, RS-423A, RS-422A, and CCITT V.10, V.11, V.28, X.26 and X.27. The NE5180 is intended for use where the data transmission rate is up to 200 kb/s. The NE5181 covers the entire range of data rates up to 10 Mb/s. The difference in data rates for the two devices results from the input filtering of the NE5180. These devices also provide a failsafe feature which protects against certain input fault conditions.

FEATURES

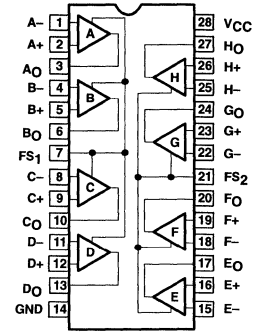
- Meets EIA RS-232C/423A/422A and CCITT V.10, V.11, V.28
- Single +5V supply—TTL compatible outputs
- Differential inputs withstand ±25V
- Failsafe feature
- Input noise filter (NE5180 only)
- Internal hysteresis
- Available in SMD PLCC

APPLICATIONS

- High-speed modems
- High-speed parallel communications
- Computer I/O ports
- Logic level translation

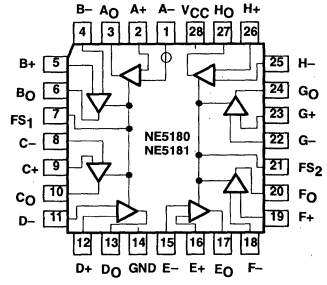
PIN CONFIGURATION

N Package



TOP VIEW

A Package



TOP VIEW

FUNCTION TABLE

INPUT	FAILSAFE INPUT	LOGIC OUTPUT
$V_{ID} < 200mV$[1]	X	H
$V_{ID} < -200mV$[1]	X	L
Both inputs open or grounded	0V	L
	V_{CC}	H

NOTE:
1. V_{ID} is defined as the non-inverting terminal input voltage minus the inverting terminal input voltage.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
28-Pin Plastic Dual In-Line (DIP) Package	0 to +70°C	NE5180N	0413B
28-Pin Plastic Dual In-Line (DIP) Package	0 to +70°C	NE5181N	0413B
28-Pin Plastic Lead Chip Carrier (PLCC) Package	0 to +70°C	NE5180A	0401F
28-Pin Plastic Lead Chip Carrier (PLCC) Package	0 to +70°C	NE5181A	0401F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
P_D	Power dissipation	800	mW
V_{CC}	Supply voltage	7	V
V_{CM}	Common mode range	±15	V
V_{ID}	Differential input voltage	±25	V
I_{SINK}	Outputsink current	50	mV
V_{FS}	Failsafe voltage	–0.3 to V_{CC}	V
J_{OS}	Output short-circuit time	1	sec

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V ±5%, 0°C ≤ T_A ≤ +70°C, input common-mode range ±7V

SYMBOL	PARAMETER	TEST CONDITIONS		NE5180		NE5181		UNIT
				Min	Max	Min	Max	
R_{IN}	DC input resistance	3V ≤ $\|V_{IN}\|$ ≤ 25V		3	7	3	7	kΩ
V_{OFS}	Failsafe output voltage	Inputs open or shorted to GND	0 ≤ I_{OUT} ≤ 8mA, $V_{failsafe}$ = 0V		0.45		0.45	V
			0 ≥ I_{OUT} ≥ –400µA, $V_{failsafe}$ = V_{CC}	2.7		2.7		
V_{th}	Differential input high[4] threshold	V_{OUT} ≥ 2.7V, I_{OUT} = –440µA	R_S = 0[1]		0.2		0.2	V
			R_S = 500[1]		0.4		0.4	
V_{tl}	Differential input low[4] threshold	V_{OUT} ≤ 0.45V, I_{OUT} = 8mA	R_S = 0[1]	–0.2		–0.2		V
			R_S = 500[1]	–0.4		–0.4		
V_H	Hysteresis[4]	FS = 0V or V_{CC} (See Figure 1)		50	140	50	140	mV
V_{IOC}	Open-circuit input voltage				2		2	V
C_I	Input capacitance	V_{ID} = 1V, I_{OUT} = –440µA			30		30	pF
V_{OH}	High level output voltage	V_{ID} = –1V		2.7		2.7		V
V_{OL}	Low level output voltage		I_{OUT} = 4mA[2]		0.4		0.4	V
			I_{OUT} = 8mA[2]		0.45		0.45	
I_{OS}	Short-circuit output current	V_{ID} = 1V [3]		20	100	20	100	mA
I_{CC}	Supply current	4.75V ≤ V_{CC} ≤ 5.25V, V_{ID} = –1V; FS = 0V			100		100	mA
I_{IN}	Input current	Other inputs grounded	V_{IN} = +10V		3.25		3.25	mA
			V_{IN} = –10V	–3.25		–3.25		

NOTES:
1. R_S is a resistor in series with each input.
2. Measured after 100ms warm-up (at 0°C).
3. Only 1 output may be shorted at a time and then only for a maximum of 1 second.
4. See Figure 1 for threshold and hysteresis definitions.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V ±5%, 0°C ≤ T_A ≤ +70°C

SYMBOL	PARAMETER	TEST CONDITIONS	NE5180		NE5181		UNIT
			Min	Max	Min	Max	
t_{PLH}	Propagation delay—low to high	C_L = 50pF, V_{ID} = ±1V		500		100	ns
t_{PHL}	Propagation delay—high to low	C_L = 50pF, V_{ID} = ±1V		500		100	ns
f_a	Acceptable input frequency	Unused input grounded, V_{ID} = ±200mV[1]		0.1		5.0	MHz
f_r	Rejectable input frequency	Unused input grounded, V_{ID} = ±500mV	5.5		NA		MHz

NOTE:
1. V_{ID} = ±1V for NE5181.

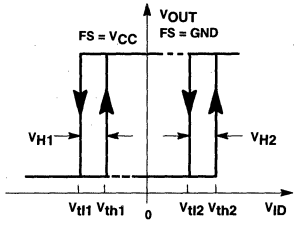
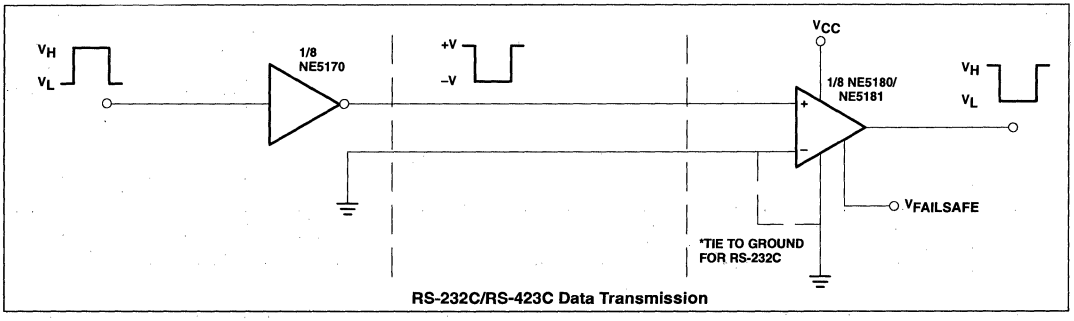


Figure 1. V_{tl}, V_{th}, V_H Definitions

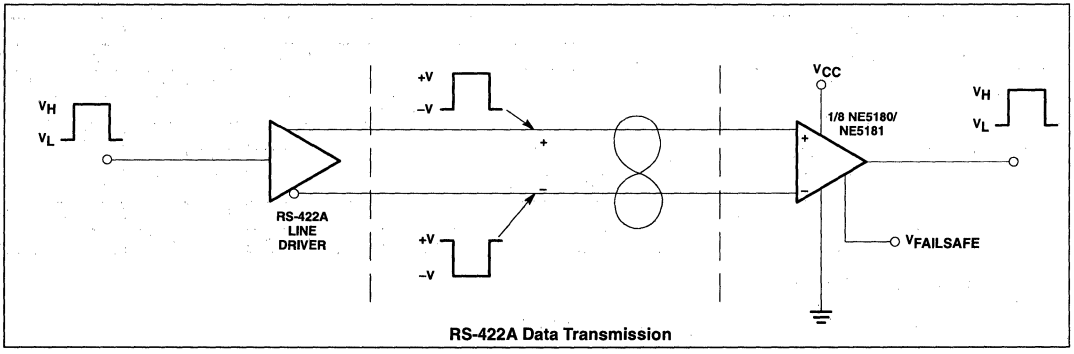
FAILSAFE OPERATION

These devices provide a failsafe operating mode to guard against input fault conditions as defined in RS-422A and RS-423A standards. These fault conditions are (1) driver in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to V_{CC} or ground. A connection to

APPLICATIONS

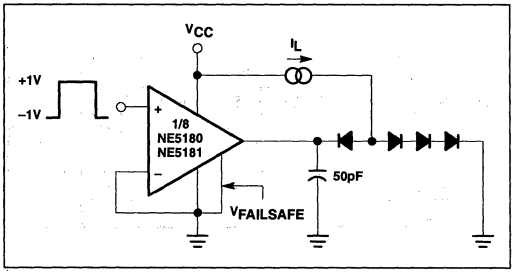


RS-232C/RS-423C Data Transmission

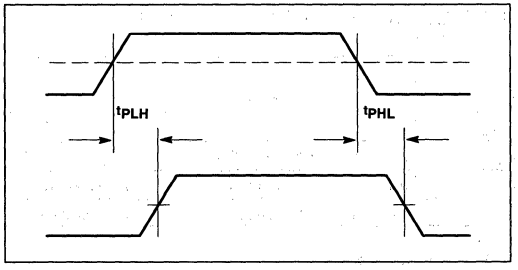


RS-422A Data Transmission

AC TEST CIRCUIT



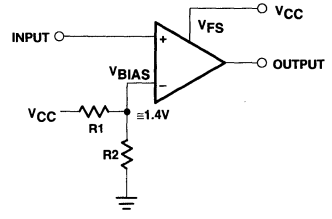
VOLTAGE WAVEFORMS



V_{CC} provides a logic "1" output under fault conditions, while a connection to ground provides a logic "0". There are two failsafe pins (F_{S1} and F_{S2}) on the NE5180 or NE5181 where each provides common failsafe control for four receivers.

RS-232 FAILSAFING

The internal failsafe circuitry works by providing a small input offset voltage which can be polarity-switched by using the failsafe control pins. This offset is kept small (approximately 80mV) to avoid degradation of the ±200mV input threshold for RS-423 or RS-422 operation. If the positive and negative inputs to any receiver are both shorted to ground or open circuited, the internal offset drives that output to the programmed failsafe state. If only one input open circuits (as may be the case for RS-232 operation), that input will rise to the "input open circuit voltage" (approximately 700mV). Since this is much greater than the 200mV threshold, the output will be driven to a state that is independent of the failsafe programming. Failsafe programming can be achieved for non-inverting single-ended applications by raising or lowering the unused input bias voltage as shown in Figure 2. For $V_{BIAS} \cong 1.4$, an open (or grounded) INPUT line will be approximately 700mV (0V) and the output will failsafe low. If the resistor divider is not used and V_{BIAS} is connected to ground, the output will failsafe high due to the internal failsafe offset for the INPUT grounded and the 700mV "open circuit input voltage" for the INPUT open circuited. Similar operation holds for an inverting configuration, with V_{BIAS} applied to the positive input and V_{FS} = ground.



NOTE:
Two silicon diodes may be used in place of R2.

Figure 2. Single-Input Failsafe Programming

INPUT FILTERING (NE5180)

The NE5180 has input filtering for additional noise rejection. This filtering is a function of both signal level and frequency. For the specified input (5.5MHz at ±500mV) the input stage filter attenuates the signal such that the output stage threshold levels are not exceeded and no change of state occurs at the output. As the signal amplitude decreases (increases) the rejected frequency decreases (increases).

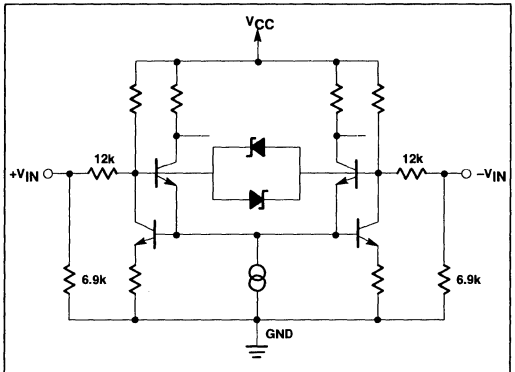


Figure 3. Differential Input Stage

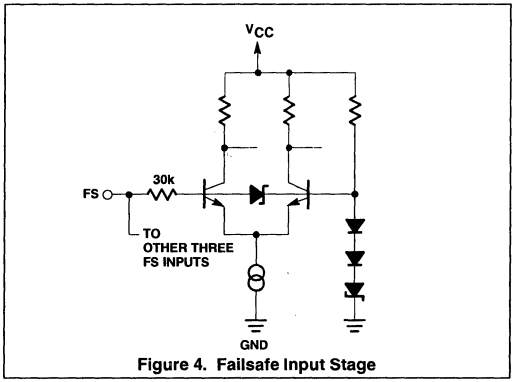


Figure 4. Failsafe Input Stage

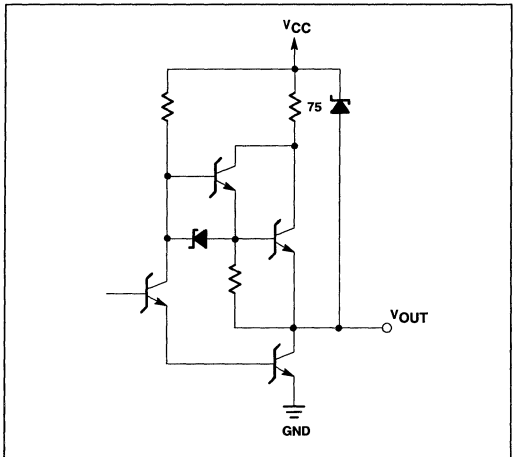


Figure 5. Output Stage

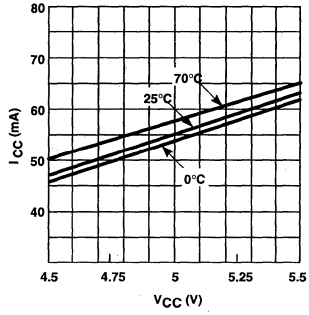


Figure 6. Typical Supply Current vs Supply Voltage

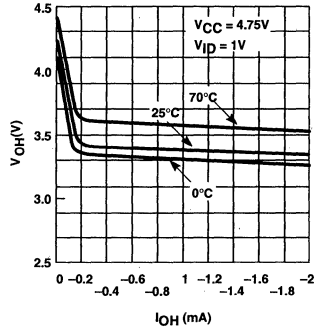


Figure 7. Typical High Level Output Voltage vs Output Current

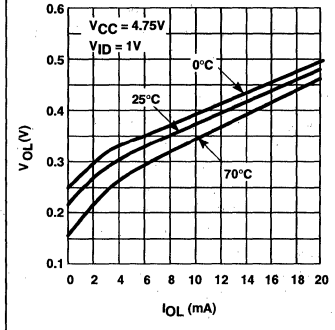
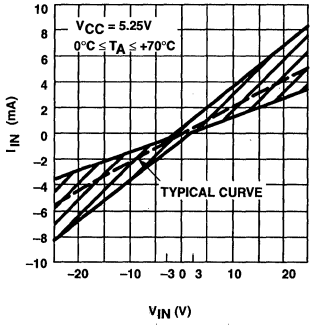


Figure 8. Typical Low Level Output Voltage vs Output Current



*This graph applies for all receiver inputs, provided that the opposite polarity input of the amplifier being measured is grounded.

Figure 9. Input Current vs Input Applied Voltage*

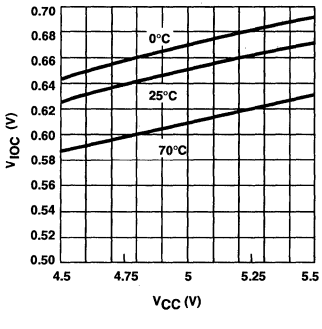


Figure 10. Typical V_{IOC} vs V_{CC}

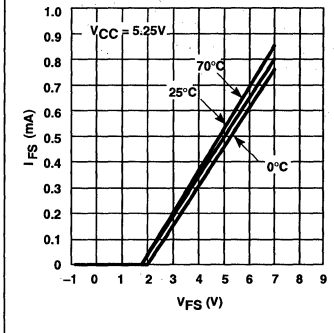


Figure 11. Typical FS Input Current vs FS Applied Voltage

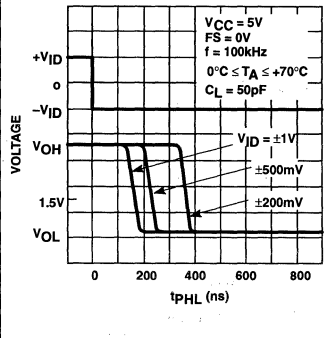


Figure 12. NE5180: Propagation Delay at Various Input Amplitudes

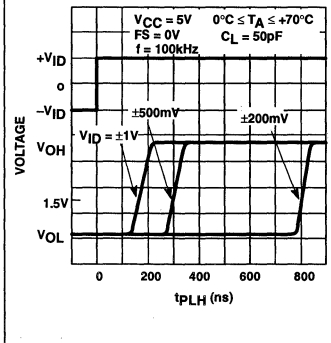


Figure 13. NE5180: Propagation Delay at Various Input Amplitude

Quad high-speed differential line driver — AM26LS31

DESCRIPTION

The AM26LS31 is a quad differential line driver, designed for digital data transmission over balanced lines. The AM26LS31 meets all the requirements of EIA standard RS-422 and Federal standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines. The circuit provides an enable and disable function common to all four drivers. The AM26LS31 features 3-State outputs and logical ORed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

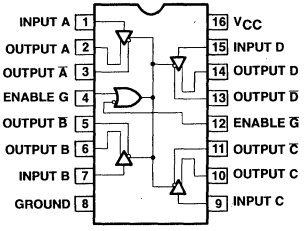
The AM26LS31 is constructed using advanced Low Power Schottky processing.

FEATURES

- Output skew of 2.0ns typical
- Input to output delay: 12ns
- Operation from single +5V
- 16-pin DIP and SO packages
- Four line drivers in one package
- Output short-circuit protection
- Complementary outputs
- Meets EIA standard RS-422
- High output drive capability for 100Ω terminated transmission lines
- Available in military and commercial temperature range
- Advanced low power Schottky processing
- Outputs won't load line when V_{CC} = 0V

PIN CONFIGURATION

D, F, and N Packages



TOP VIEW

APPLICATIONS

- Data communications equipment
- Computer peripherals
- Workstations
- Automatic test equipment

FUNCTION TABLE (Each Driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	A	$\overline{A}$
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

NOTES:
H = High level
L = Low level
X = Irrelevant
Z = High-impedance (OFF)

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0°C to +70°C	AM26LS31CN	0406C
16-Pin Small Outline (SO) Package	0°C to +70°C	AM26LS31CD	0005D
16-Pin Plastic Dual In-Line Package (DIP)	–40°C to +85°C	AM26LS31IN	0406C
16-Pin Small Outline (SO) Package	–40°C to +85°C	AM26LS31ID	0005D
16-Pin Plastic Dual In-Line Package (DIP)	–55°C to +125°C	AM26LS31MN	0406C

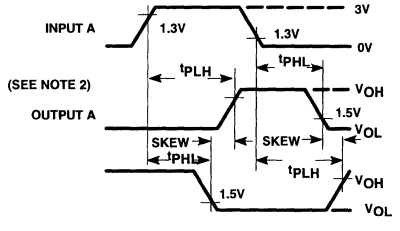
DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%, T_A = –55 to +125°C for AM26LS31MF and AM26LS31MN; V_{CC} = 5V ±5%, T_A = –40 to +85°C for AM26LS31IN and AM26LS31ID; V_{CC} = 5V ±5%, T_A = 0 to +70°C for AM26LS31CN and AM26LS31CD, unless otherwise specified.

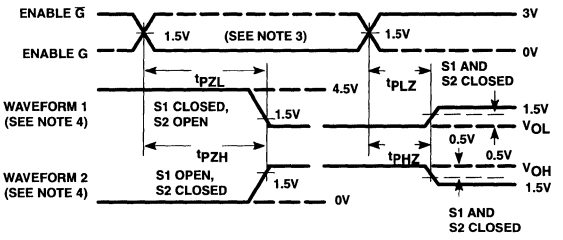
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[1]	Max	
V_{OH}	Output High voltage	V_{CC} = Min., I_{OH} = –20mA	2.5	3.0		V
V_{OL}	Output Low voltage	V_{CC} = Min., I_{OL} = 20mA		0.3	0.5	V
V_{IH}	Input High voltage	V_{CC} = Min.	2.0			V
V_{IL}	Input Low voltage	V_{CC} = Max.			0.8	V
I_{IL}	Input Low current	V_{CC} = Max., V_{IN} = 0.4V		–0.26	–0.36	mA
I_{IH}	Input High current	V_{CC} = Max., V_{IN} = 2.7V		0.001	20	µA
I_I	Input reverse current	V_{CC} = Max., V_{IN} = 7.0V		0.001	0.1	mA
I_O	OFF-state (high-impedance) output current	V_{CC} = Max., V_O = 5.5V V_O = 0.5V		0.6 –0.050	20 –20	µA µA
V_I	Input clamp voltage	V_{CC} = Min., I_{IN} = –18mA		–0.8	–1.5	V
I_{SC}	Output short-circuit current	V_{CC} = Max.	–30		–150	mA
I_{CC}	Power supply current	V_{CC} = Max; all outputs disabled		40	80	mA
t_{PLH}	Input to output	T_A = 25°C, load[2]		9	20	ns
t_{PHL}	Input to output	T_A = 25°C, load[2]		9	20	ns
SKEW	Output to output	T_A = 25°C, load[2]		2	6	ns
t_{LZ}	Enable to output	T_A = 25°C, C_L = 10pF		17	35	ns
t_{HZ}	Enable to output	T_A = 25°C, C_L = 10pF		12	30	ns
t_{ZL}	Enable to output	T_A = 25°C, load[2]		14	45	ns
t_{ZH}	Enable to output	T_A = 25°C, load[2]		12	40	ns

NOTES:
1. All typical values are T_A = +25°C; V_{CC} = 5.0V.
2. C_L = 30pF; V_{IN} = 1.3V to V_{OUT} = 1.3V; V_{PULSE} = 0V to 3.0V.

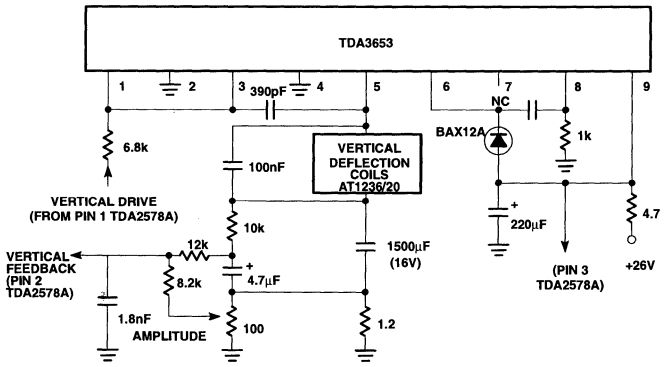
TIMING DIAGRAMS



Propagation Delay Times and Skew



Enable and Disable Times



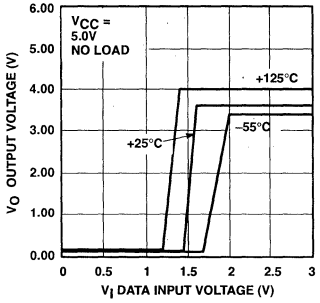
Test Circuit

NOTES:

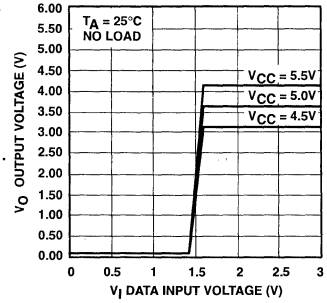
1. All pauses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_{OUT} = 50W, 1R ≤ 15ns, 1F ≤ 6ns
2. When measuring propagation delay times and skew, switches S1 and S2 are open.
3. Each enable is tested separately.
4. Waveform 1 is for an output with internal condition such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal condition such that the output is high except when disabled by the output control.
5. C_L includes probe and jig coapacitance.

TYPICAL PERFORMANCE CHARACTERISTICS

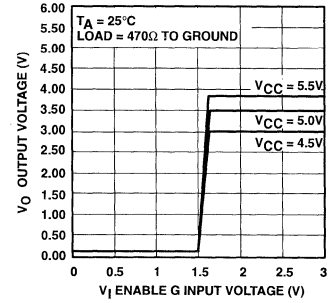
Output Voltage vs Data Input Voltage



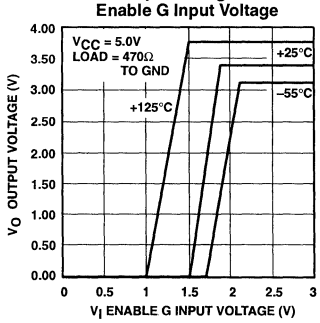
Output Voltage vs Data Input Voltage



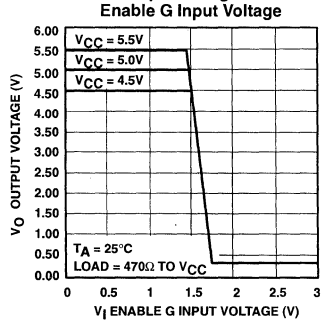
Output Voltage vs Enable G Input Voltage



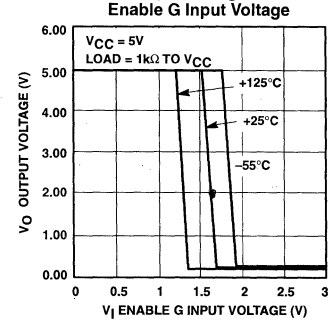
Output Voltage vs Enable G Input Voltage



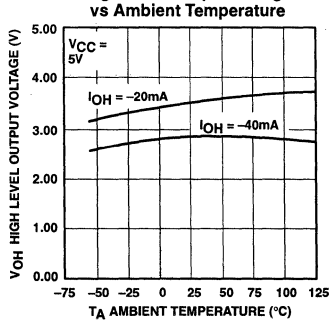
Output Voltage vs Enable G Input Voltage



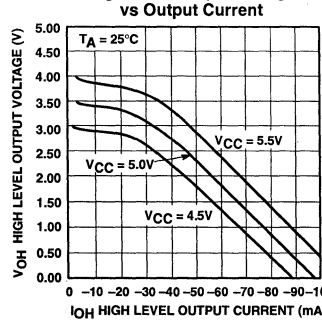
Output Voltage vs Enable G Input Voltage



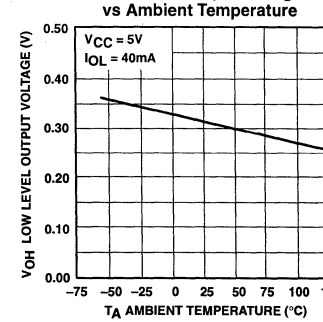
High Level Output Voltage vs Ambient Temperature



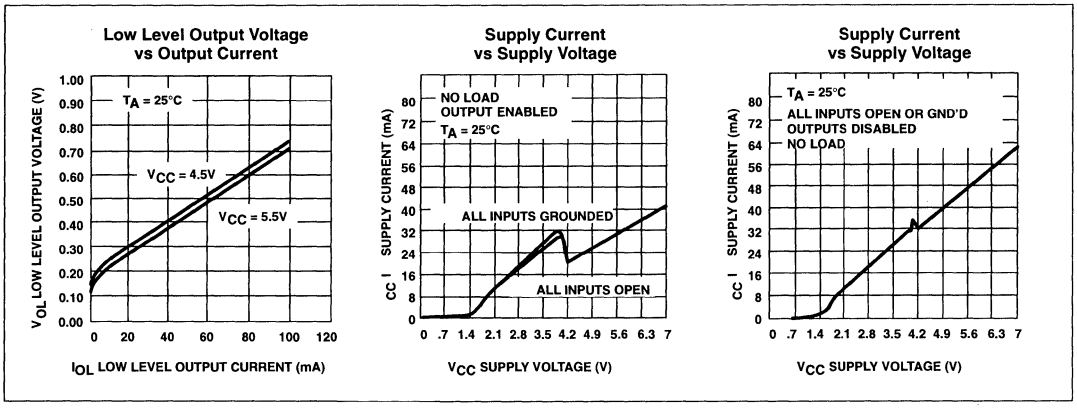
High Level Output Voltage vs Output Current



Low Level Output Voltage vs Ambient Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



Quad high-speed differential line receivers

AM26LS32/ AM26LS33

DESCRIPTION

The AM26LS32 and AM26LS33 are quad line receivers designed to meet all of the requirements of RS-422 and RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The AM26LS32 features an input sensitivity of ±200mV over the common mode input range of ±7V.

The AM26LS33 features an input sensitivity of ±500mV over the common mode input voltage range of ±15V.

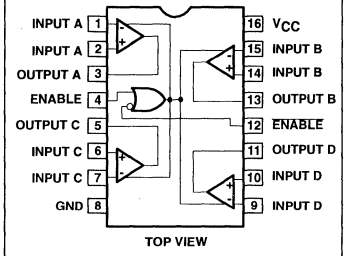
The AM26LS32 and AM26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-State outputs with 8mA sink capability and incorporate a fail-safe input-output relationship which forces the outputs high when the inputs are open.

FEATURES

- Input voltage range of 15V (differential or common mode) on AM26LS33; 7V (differential or common mode) on AM26LS32
- ±0.2V sensitivity over the input voltage range on AM26LS32
- ±0.5V sensitivity on AM26LS33
- 6kΩ minimum input impedance
- The AM26LS32 meets all the requirements of RS-422 and RS-423
- Operation from single +5V supply
- Fail safe input-output relationship. Output always high when inputs are open
- 3-State drive, with choice of complementary output enables, for receiving directly onto a data bus
- 3-State outputs disabled during power up and power down

PIN CONFIGURATION

F, D and N Packages



TOP VIEW

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0°C to +70°C	AM26LS32CN	0406C
16-Pin Small Outline (SO) Package	0°C to +70°C	AM26LS32CD	0005D
16-Pin Plastic Dual In-Line Package (DIP)	–40°C to +85°C	AM26LS32IN	0406C
16-Pin Small Outline (SO) Package	–40°C to +85°C	AM26LS32ID	0005D
16-Pin Plastic Dual In-Line Package (DIP)	–55°C to +125°C	AM26LS32MN	0406C
16-Pin Plastic Dual In-Line Package (DIP)	0°C to +70°C	AM26LS33CN	0406C
16-Pin Small Outline (SO) Package	0°C to +70°C	AM26LS33CD	0005D
16-Pin Plastic Dual In-Line Package (DIP)	–40°C to +85°C	AM26LS33IN	0406C
16-Pin Small Outline (SO) Package	–40°C to +85°C	AM26LS33ID	0005D
16-Pin Plastic Dual In-Line Package (DIP)	–55°C to +125°C	AM26LS33MN	0406C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	7	V
V_{IN}	Power supply	7	V
	Output sink current	50	mA
	Common mode range	±25	V
V_{TH}	Differential input voltage	±25	V
T_{STG}	Storage temperature range	–65 to +150	°C

DISSIPATION OPERATING TABLE

PACKAGE	POWER DISSIPATION	DERATING FACTOR	ABOVE T_A
F	1,524mW	12.19mW/°C	25°C
N	1,275mW	10.2mW/°C	25°C
D	1,262W	10.1mW/°C	25°C

DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10% for AM26LS32/33MX, V_{CC} = 5.0V ±5% for AM26LS32/33CX and AM26LS32/33IX over operating temperature range unless otherwise specified.

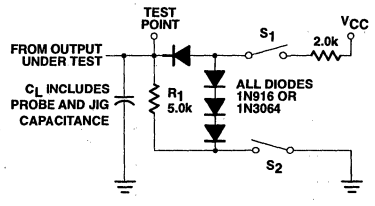
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS AM26LS32/33 Min	Typ[1]	Max	UNIT
V_{TH}	Differential input voltage	$V_{OUT} = V_{OL}$ or V_{OH} AM26LS32, −7V ≤ V_{CM} ≤ +7V		−0.2	0.06	0.2	V
		AM26LS33, −15V ≤ V_{CM} ≤ +15V		−0.5	0.06	0.5	
R_{IN}	Input resistance	−15V ≤ V_{CM} ≤ +15V (One input AC ground)		6.0	9.8		kΩ
I_{IN}	Input current (under test)	V_{IN} = +15V Other input −10V ≤ V_{IN} ≤ +15V				2.3	mA
I_{IN}	Input current (under test)	V_{IN} = −15V Other input +10V ≤ V_{IN} ≤ −15V				−2.8	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., I_{OH} = −440µA ΔV_{IN} = +1.0V $V_{\overline{ENABLE}}$ = 0.8V	Com'l	2.7	3.4		V
			Mil	2.5	3.4		
V_{OL}	Output LOW voltage	V_{CC} = Min., $V_{\overline{ENABLE}}$ = 0.8V ΔV_{IN} = +1.0V	I_{OL} = 4.0mA		0.3	0.4	V
			I_{OL} = 8.0mA			0.45	
V_{IL}	Enable LOW voltage					0.8	V
V_{IH}	Enable HIGH voltage			2.0			V
V_I	Enable clamp voltage	V_{CC} = Min., I_{IN} = −18mA				−1.5	V
I_O	Off state (high impedance) output current	V_{CC} = Max.	V_O = 2.4V			20	µA
			V_O = 0.4V			−20	
I_{IL}	Enable LOW current	V_{IN} = 0.4V			−0.2	−0.36	mA
I_{IH}	Enable HIGH current	V_{IN} = 2.7V			0.5	20	µA
I_I	Enable input HIGH current	V_{IN} = 5.5V			1	100	µA
I_{SC}	Output short circuit current	V_{CC} = Max., ΔV_{IN} = +1V, V_{OUT} = 0V		−15	−60	−85	mA
I_{CC}	Power supply current	V_{CC} = Max.; All V_{IN} = GND outputs disabled			52	70	mA
V_{HYST}	Input hysteresis	T_A = 25°C, V_{CC} = 5.0V, V_{CM} = 0V	AM26LS32		120		mV
			AM26LS33		120		
t_{PLH}	Input to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF (see test condition)			10	25	ns
t_{PHL}	Input to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF (see test condition)			10	25	ns
t_{LZ}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 5pF (see test condition)			15	30	ns
t_{HZ}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 5pF (see test condition)			12	22	ns
t_{ZL}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF (see test condition)			8	22	ns
t_{ZH}	Enable to output	T_A = 25°C, V_{CC} = 5.0V C_L = 15pF			9	22	ns

NOTE:
1. All typical values are T_A = 25°C, V_{CC} = 5.0V.

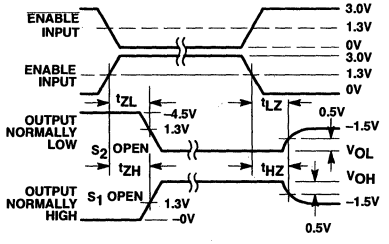
FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUT	ENABLES E	ENABLES $\overline{E}$	OUTPUT
$V_{ID} \geq V_{TH}$	H	X	H
	X	L	H
$V_{TL} \leq V_{ID} \leq V_{TH}$	H	X	?
	X	L	?
$V_{ID} \leq V_{TL}$	X	L	L
	H	X	X
X	L	H	Z

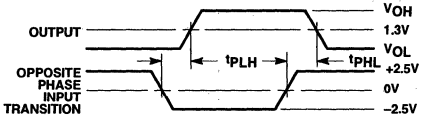
NOTES:
H = High level, L = Low level, X = Irrelevant
Z = High impedance (off), ? = Indeterminate
E = Enable, $\overline{E}$ = $\overline{Enable}$



Load Test Circuit for 3-State Outputs



Enable and Disable Tmes[2, 3, 4]



Propagation Delay[1, 4]

NOTES:
1. Diagram shown for $\overline{Enable}$ Low.
2. Enable is tested with $\overline{Enable}$ High; $\overline{Enable}$ is tested with Enable Low.
3. S_1 and S_2 of Load Circuit are closed except where shown.
4. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_O = 50Ω; $t_r \leq 15ns$; $t_f \leq 6.0ns$.

Quad high-speed differential line receivers AM26LS32B

DESCRIPTION

The AM26LS32B is a quad line receiver designed to meet all of the requirements of RS-422 and RS-423, CCITT V.10 and V.11 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

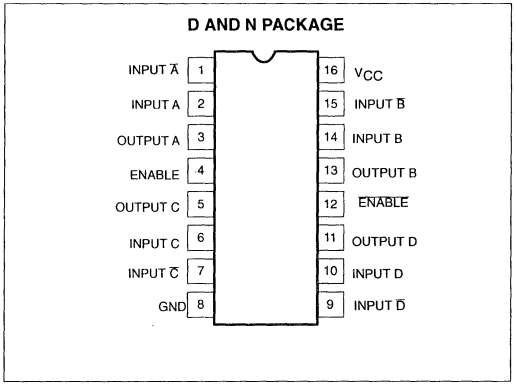
The AM26LS32B features an input sensitivity of +100mV over the common mode input voltage range of 0V to +5V and +200mV over the common mode input voltage range of -7V to +12V.

The AM26LS32B guarantees a minimum hysteresis and propagation delay skew resulting in a higher noise margin and better system performance.

The AM26LS32B provides an enable and disable function common to all four receivers. It features 3-state outputs with 24mA sink capability and incorporates a fail-safe input-output relationship which keeps the outputs high when the inputs are open.

PIN CONFIGURATION

D AND N PACKAGE



FEATURES

- ±100mV sensitivity over the input range of 0V to 5V
- +200mV sensitivity over the V_{CM} range
- Typical input voltage hysteresis of 120mV
- 3V maximum open circuit voltage
- Three state outputs disabled power up and power down
- All AC and DC parameters guaranteed over operating temp range
- Single +5V supply
- Advance low-power Schottky processing

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	AM26LS32BCN	0406C
16-Pin Small Outline (SO) Package	0 to +70°C	AM26LS32BCD	0005D
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	AM26LS32BIN	0406C
16-Pin Small Outline (SO) Package	-40 to +85°C	AM26LS32BID	0005D
16-Pin Plastic Dual In-Line Package (DIP)	-55 to +125°C	AM26LS32BMN	0406C

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	7	V
V_{IN}	Enable voltage	7	V
	Output sink current	50	mA
	Common mode range	±25	V
V_{TH}	Differential input voltage	±30	V
T_{STG}	Storage temperature range	-55 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec.)	300	°C
θ_{JA}	Thermal impedance		°C/W

PACKAGE POWER DISSIPATION DERATING TABLE

PACKAGE	POWER DISSIPATION AT T_A = 25°C	DERATING FACTOR ABOVE T_A
N	1,275mW	10.2mW/°C
D	1,262mW	10.1mW/°C

DC ELECTRICAL CHARACTERISTICS

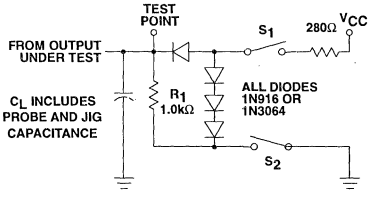
V_{CC} = 5.0V ±10% for Am26LS32BMX, V_{CC} = 5.0V ±5% for Am26LS32BCX over operating temperature range unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				MIN	TYP	MAX	
V_{TH}	Differential input voltage	$V_{OUT} = V_{OL}$ or V_{OH}	0V ≤ V_{CM} ≤ 5V	-100		+100	mV
			-7V ≤ V_{CM} ≤ +12V	-200		+200	
R_{IN}	Input resistance	-15V ≤ V_{CM} ≤ +15V (one input AC ground)		6.0			kΩ
I_{IN}	Input current (under test)	V_{IN} = +15V Other input -15V ≤ V_{IN} ≤ +15V				2.3	mA
I_{IN}	Input current (under test)	V_{IN} = -15V Other input +15V ≤ V_{IN} ≤ -15V		-2.8			mA
V_{OH}	Output HIGH voltage	V_{CC} = min., ΔV_{IN} = +1.0V V_{EN} = 0.8V	I_{OH} = -12mA	2.0			V
			I_{OH} = -1mA	2.4			
V_{OL}	Output LOW voltage	V_{CC} = min., ΔV_{IN} = -1.0V V_{EN} = 0.8V	I_{OH} = 16mA			0.4	V
			I_{OH} = 24mA			0.5	
V_{IL}	Enable LOW voltage	V_{CC} = max				0.8	V
V_{IH}	Enable HIGH voltage			2.0			V
V_I	Enable clamp voltage	V_{CC} = min, I_{IN} = -1.8mA		-1.5			V
I_O	Off state (high impedance) output current	V_{CC} = max	V_O = 2.4V			20	µA
			V_O = 0.4V			-20	
I_{IL}	Enable LOW current	V_{IN} = 0.4V				-0.36	mA
I_{IH}	Enable HIGH current	V_{IN} = 2.7V				20	µA
I_I	Enable input HIGH current	V_{IN} = 5.5V				100	µA
I_{SC}	Output short circuit current	V_{CC} = max, ΔV_{IN} = +1V, V_{OUT} = GND		-30		-120	mA
I_{CC}	Power supply current	V_{CC} = max, all V_{IN} = GND outputs disabled				70	mA
V_{HYST}	Input hysteresis	V_{CC} = 5.0V, V_{CM} = 0V		80		200	mV
V_{IOC}	Open circuit input voltage			1		3	V

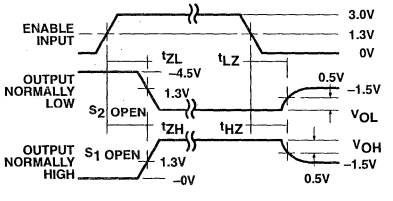
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS				UNIT
			ROOM TEMPERATURE[2]		COMMERCIAL/ MILITARY[1]		
			TYP	MAX	TYP	MAX	
t_{PLH}	Propagation delay, input to output	C_L = 50pF (see test circuit)		21		26	ns
t_{PHL}				21		26	
t_{SKEW}	Propagation delay skew, t_{PLH} - t_{PHL}			3.0		4.0	
t_{ZL}	Output enable time, EN to OUTPUT			22		33	
t_{ZH}				16		22	
t_{LZ}	Output disable time, EN to OUTPUT	C_L = 5pF (see test circuit)		18		27	ns
t_{HZ}				18		27	

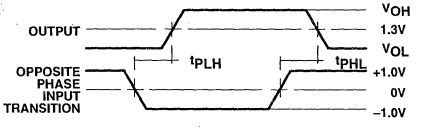
NOTES:
1. AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.
2. V_{CC} = 5V



SWITCHING TEST CIRCUIT FOR THREE STATE OUTPUTS



ENABLE AND DISABLE TIMES (Notes 2 and 3)



PROPAGATION DELAY (Notes 1 and 3)

NOTE:
1. Diagram fhown for Enable LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_O = 50Ω; t_r ≤ 2.5ns; t_f ≤ 2.5ns.

Figure 1.

Power line modem — NE5050

DESCRIPTION

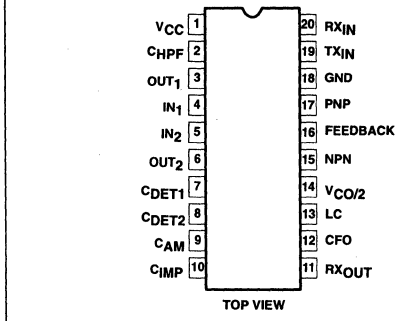
The NE5050 is a modem for power line, coaxial cable, and twisted-pair communications. The modem incorporates features to overcome line impulse noise and line impedance modulation. The modem's transmitter incorporates a Colpitts oscillator, positive logic, carrier-on/-off switch, and a line driver. The receiver has an amplifier, a limiter, an amplitude detector, an amplitude modulation cancelling stage, an impulse filter, and an SR flip-flop. One NE5050 can be used to transmit and receive with Amplitude Shift Key (ASK) carrier-on/-off modulation. With two NE5050s, Frequency Shift Key (FSK) modulation can be implemented. The transmitter input and the receiver output accept TTL or CMOS serial data.

FEATURES

- High receiver sensitivity — typ. 1.5mV$_{RMS}$
- Receiver input overload protected for signals up to 70V$_{P-P}$
- High data rates — 300kbit/s ASK NRZ over twisted-pair
- The modem reaches the Nyquist limit of 1 bit per carrier cycle
- Has listen-while-talking for carrier sense multiple access/collision detect (CSMA/CD) networking capability
- Increased noise immunity with balance interstage ports for bandpass filtering
- Flexible oscillator can be made with LC tank (Colpitts), with crystal (Pierce), or accept external clock
- Signals are processed in real-time making this modem suitable for repeater/carrier translation applications

PIN CONFIGURATION

D[1] and N Packages



TOP VIEW

NOTE:
1. SOL — Released in large SO package only.

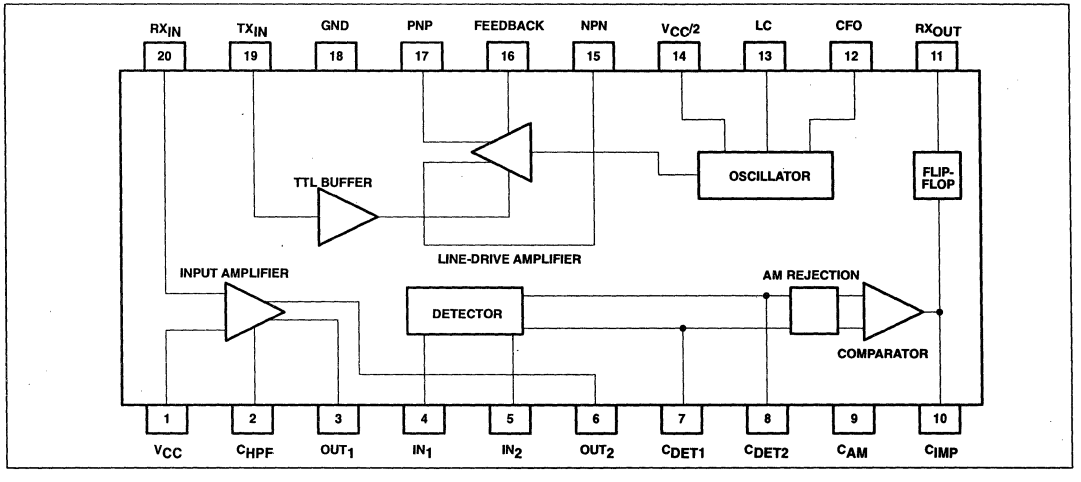
APPLICATIONS

- Twisted-pair communications
- Coaxial cable communications
- 120/277V$_{RMS}$, 50 or 60Hz, power line communications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5050N	0408B
20-Pin Plastic Small Outline Large (SOL) Package	0 to +70°C	NE5050D	0172D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	18	V
V_{LOGIC}	Logic supply voltage	18	V
T_A	Ambient temperature range	0 to +70	°C
T_J	Junction temperature range	−55 to +150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
P_{DMAX}	Maximum power dissipation[1]	700	mW

NOTE:
1. The power dissipation is based on V_{CC} = 12V, T_J = +150°C, TX_{OFF}: I_{CC} = 20mA, TX_{ON}: I_{CC} = 50mA, θ_{JA} = 61°C/W 20-pin plastic package.

DC ELECTRICAL CHARACTERISTICS

T_A = +25°C, V_{CC} = 12V, F carrier = 120kHz, data = NRZ, 50% duty cycle unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		10	12	16	V
I_{CC}	Supply current	TX_{OFF}	5	8	11	mA
I_{CC}	Supply current	TX_{ON}[1]	18	24	30	mA
V_{LOGIC}	Logic voltage			5	16	V
P_D	Power dissipation	RX_{OFF}, TX_{OFF} RX_{ON}, TX_{ON}, 100Ω load		100 300	220 660	mW
V_{IHMIN}	TX TTL input	TX_{ON}, Pin 19	2.4			V
V_{ILMAX}	TX TTL input	TX_{OFF}, Pin 19			0.8	V
V_{OLMAX}	RX open-collector output	I_{OL} = 5mA, Pin 11			0.4	V
I_{OLMAX}	RX open-collector output	Pin 11			5	mA
	TX data rate[2]	f_{CXR} = 120kHz, 500kHz	DC	1k	300k	bit/s
	RX data rate[2]	f_{CXR} = 120kHz, 500kHz	0.1	1k	300k	bit/s
	Carrier cycles per bit, TX and RX[2]		1			cycle
Broadband I/O ports, carrier						
	RX input sensitivity	1:1 input transformer	3.5	1.5		mV_{RMS}
	RX input signal level	V_{CC} ±35V = −25V, +51V			70	V_{P-P}
	RX input impedance	Pin 20		9		kΩ
	RX line impedance modulation rejection	120HzAM 2V/20mV, 1kbit/s	40			dB
	RX carrier frequency[2]		0.1	120	500	kHz
	RX detector differential input irnpedance	Pin 4, Pin 5, each		27		kΩ
PSRR	RX power supply rejection ratio	60Hz and 120Hz		80		dB
	Broadband port impedance	RX_{OFF} and TX_{OFF}		7.3		kΩ
	TX output signal level	TX_{ON}, 100Ω load		8		V_{P-P}
	TX driver output impedance	TX_{OFF}		40		kΩ
	TX driver output impedance	TX_{ON}		1.2		Ω
	TX amplitude temperature drift	External oscillator		+140		ppm/°C
	TX amplitude temperature drift	LC oscillator		+0.23		%/°C
	TX output current capability	TX_{ON}, Pins 15, 17		40		mA peak
	TX output THD (total harmonic distortion)	TX_{ON}, LC oscillator		1	2	%
	TX line drive amplifier BW	At 6dB gain		500		kHz
	TX carrier frequency[2]		DC	120	500	kHz
	TX oscillator temperature drift	Temperature range		+60		ppm/°C
	TX oscillator initial frequency accuracy	Sam LC tank		±1		%
	TX carrier feedthrough (leakage)	TX_{OFF}		−90		dBmO

ABBREVIATIONS:
TX = transmitter
RX = receiver
NOTES:
1. TX looped back to RX, data = 1kbit/s TTL, NRZ, 50% duty cycle ASK.
2. The NE5050 modem reaches the theoretical maximum data density for a given (fixed) carrier frequency. This limit is set by the maximum data bandwidth required before intersymbol interference occurs. The minimum specified limits are not tested in production. They are guaranteed by design.

PIN FUNCTION DESCRIPTION

Pin 1: $+V_{CC}$
For de-coupling V_{CC} to ground a 0.1µF capacitor must be placed close to Pin 1 and Pin 18.

Pin 2: C_{HPF}
High-pass filter, rejects 60Hz and its harmonics, rejects low frequencies, directing them to ground. Capacitor to ground: C_{HPF} = 10nF for f_{CXR} = 120kHz and C_{HPF} = 4.7nF for f_{CXR} = 300kHz. The input amplifier provides a high-pass function: a +20dB/decade frequency response, with a DC attenuation of –50dB. A frequency of 100kHz is amplified by +24dB. The –3dB point of this high-pass filter is given by the equation:

$10^9/C_{HPF}$ (F) = f_{-3dB} (Hz)

Pin 3: OUT_1
RX amplifier differential (+) output. Low impedance output. See Pin 6. Pin 3 can be connected to Pin 4 directly. A differential, bandpass filter can be connected from Pins 3, 6 to Pins 4, 5. If LC values are used, they are the same as the oscillator LC values (see Pins 13 and 14). The BW_{-3dB} is controlled by the series resistors R_1 and R_2. An external active filter providing gain can improve the RX sensitivity and filter out CW interference.

Pin 4, Pin 5: IN_1, IN_2
AM detector (±) inputs. High-impedance inputs = 27kΩ each. The require DC bias voltage from Pins 3 and 6 or around 4.5V. Pin 3 can be connected to Pin 4 directly. Pin 6 can be connected to Pin 5 directly. A differential bandpass filter can be connected from Pins 3, 6 to Pins 4, 5. If LC values are used, they are the same as the oscillator LC values (see Pins 13 and 14). The BW_{-3dB} is controlled by series resistors. An external active filter providing gain can improve the RX sensitivity and filter out CW interference.

Pin 6: OUT_2
RX amplifier differential (–) output. Low impedance output. See Pin 3. Pin 6 can be connected to Pin 5 directly.

Pin 7, Pin 8: C_{DET}
Amplitude detector (±) output capacitor between Pins 7 and 8. t_{DET} is the time it takes for C_{DET} to charge from 0mV to 50mV, where 50mV is the detection threshold. The detector delay time, t_{DET}, affects the receiver's jitter. t_{DET} is a term in a sum of delays, the sum being the total receiver delay, t_D. See below in 'Receiver Delays' the relation between t_D and the maximum bit rate. The C_{DET} capacitor value is given by:

C_{DET} (F) = t_{DET} (sec)/10^5

Pin 9: C_{AM}
Line impedance modulation rejection capacitor. A 0.1µF capacitor to ground provides about 4s of delay for the transition from receive data to standby. The C_{AM} value is determined in function of the bit string or in the preamble. It is a measure of the "readiness" of the receiver to switch from the "standby" mode to the "receive data mode" with no loss of leading bits. A low C_{AM} value will make the modem react faster (shorter delays) in both transition directions: from "standby" to "receive data" (incoming or departing messages) and from "receive data" to "standby" (absence of data traffic). Its value should be

C_{AM} (F) = 10–4/bit rate [bits/s]

Pin 10: C_{IMP}
Impulse noise rejection capacitor. At 1kbit/s a 10nF capacitor to ground provides 350µs of delay and impulse rejection. This capacitor determines the receiver impulse noise immunity (transmission channel with non-Gaussian noise). t_{IMP} is the time it takes to ramp up or down the C_{IMP} voltage (the beginning of the ramp is delayed by t_{DET}). The shortest bit should last longer than the widest impulse. t_{IMP} is a term in a sum of delays, the sum being the total receiver delay, t_D. See 'Receiver Delays' for the relation between t_D and the maximum bit rate. The C_{IMP} capacitor value is determined by the equation:

C_{IMP} (F) = t_{IMP} (s)/85kΩ

The following equation determines t_{IMP}:

Maximum rejected or expected impulse noise width (s) < t_{IMP} (s)

Pin 11: RX Data Output
Open-collector RX output. RX data output.

I_{OLMAX} = 5mA = $V_{LOGIC}/R_{PULL-UP}$

Pin 12: C_{F0}
Oscillator feedback input. C_{F0} = 27 to 51pF capacitor between Pins 12 and 13. C_{F1} = capacitor between Pins 12 and GND. If the on-chip oscillator is used, C_{F1} may be omitted. If external oscillations are injected at Pin 13, C_{F0} must be removed and C_{F1} must be connected to GND. Grounding Pin 12 disables the oscillator.

Pin 13: Oscillator I/O
Colpitts LC oscillator tank, Pierce crystal oscillator, or external oscillator input.

On-chip LC oscillator — oscillator output. External oscillator tank present. Parallel LC components attached between Pins 13 and 14. C_{F0} attached between Pin 12 and Pin 13. A resistor between Pins 13 and 14 can decrease the oscillation amplitude to the desired level. Amplitudes above 2V peak may have THD > 2%. C_{F1} is not used. The amplitude varies with temperature; thermistor compensation recommended at Pin 16.

On-chip crystal oscillator — oscillator output. Two external capacitors in series, C_{13} and C_{14}. C_{13} is connected to Pin 13 and C_{14} is connected to Pin 14. The external crystal is attached between Pin 13 and the connection of C_{13} and C_{14}. An optional inductor L, attached between Pins 13 and 14, tuned at the oscillation

frequency by C_{13} and C_{14} prevents oscillations at the crystal overtones. C_{F0} and C_{F1} are not used.

External oscillator — oscillator input. Parallel LC components attached between Pins 13 and 14 provide bias to Pin 13 and perform bandpass filtering. If a square wave is generated from a microprocessor by clock division, a series LC from the divider output to Pin 13 will perform additional bandpass filtering. C_{F1} = 0.1µF is connected to ground. C_{F0} is not used. If a sinusoidal wave is available, a 50Ω resistor may replace the parallel LC bandpass filter and a 0.1µF capacitor may replace the series LC bandpass filter. The amplitude is constant over temperature.

Pin 14: $+V_{CC}/2$

Oscillator bias at $+V_{CC}/2$. A 0.1µF de-coupling capacitor to GND is optional. Parallel LC components attached between Pins 13 and 14.

Pin 15: TX Carrier Output (NPN Transistor Base)

Transmitter broadband output. Can drive 40mA peak (80mA peak non-repetitive).

NPN external Darlington translator drive — Drives 1Ω loads.

NPN external translator drive — 1Ω – 0.5W – R_{E1} to Pin 16 for 10Ω loads.

On-chip driver — 10Ω R_{E1} between Pins 15 and 16 for 50Ω loads.

Pin 16: TX Line Drive Feedback

$R_{FEEDBACK}$ adjusts the driver amplifier gain. Minimum gain ($R_{FEEDBACK}$ = 0) is 2 (6dB). A thermistor can compensate the LC oscillator amplitude variation. R_{E1} resistor (and NPN EB junction) to Pin 15. R_{E2} resistor (and PNP EB junction) to Pin 17. The C_{DRIVE} coupling capacitor is in series with the R_{DRIVE} resistor from Pin 16 to Pin 20. The R_{DRIVE} value is the assumed line impedance. The C_{DRIVE} impedance is $1/(2 \times f_{CXR} C_{DRIVE})$.

Pin 17: TX Carrier Output (PNP Transistor Base)

Transmitter broadband output. Can drive 40mA peak (80mA peak non-repetitive).

PNP external Darlington translator — Drives 1Ω loads.

PNP external translator drive — 1Ω – 5.0W – R_{E2} to Pin 16 for 10Ω loads.

On-chip driver — 10Ω R_{E2} between Pins 16 and 17 for 50Ω loads.

Pin 18: Ground

Pin 19: TX Data Input

Transmitter TTL data input. Logic 1 will turn the transmit driver on, and sinusoidal carrier will be sent to the line from a low impedance source. Logic 0 will turn the driver off, to high output impedance.

Pin 20: RX Carrier Input

Receiver carrier input. Withstands an over-voltage of $+V_{CC}$ ±35V. DC bias connected through the line coupling transformer secondary to $+V_{CC}$ (Pin 1). The C_{DRIVE} coupling capacitor is in series with the R_{DRIVE} resistor from Pin 16 to Pin 20.

DESCRIPTION OF OPERATION

The NE505 modem has been designed for transmitting and receiving control and data signals over the AC power lines, coaxial cables and twisted-pair cables. The modem overcomes line impulse noise and line impedance modulation. Two carrier modulation methods can be used: carrier on/off ASK, NRZ data and non-coherent FSK.

The power line is not an ideal medium for communication. The line noise, interference and losses are caused by: impulse noise, CW interference, line impedance modulation, and distribution transformer attenuation. NE5050 was designed to support both ASK and non-coherent FSK communications in this environment.

Listen-While-Talk

The IC modem is always in the receive mode, even when transmitting (it receives its own carrier). This capability permits remote RX and TX functionality testing for each system node. In the receive mode, the modem receives carrier signals from other transmitters. In the transmit mode, the modem transmits carrier to other receivers and receives its own carrier.

On-Chip Collision Detection

The listen-while-talk capability enables this IC to perform CSMA/CD (carrier-sense, multiple-access/collision detect) networks. Collision is detected when the local TX intends to transmit and the line is not clear.

In Dense Data Traffic

The RX data output (RX_{OUT}) does not have time to go into the standby (lower power consumption, inverted logic) mode. In this case the RX_{OUT} is in positive logic (carrier-on = 1, carrier-off = 0). A collision is detected at the local node when the local TX is off and the local RX_{OUT} = 1. Collision: remote carrier present and detected. Abort local transmission. If, however, standby occurs (bursts of high-speed data) a proper value of C_{AN} will insure capture of all leading bits except for the first "10" transition.

In Rare Data Traffic

The RX_{OUT} is in standby most of the time. In this case the RX_{OUT} logic mode is inverted due to a designed-in offset present in the AM rejection and impulse filter circuits. A logic sequence from the local TX insures proper RX offset adjustment (preamble, the first "10" bits). The collision detection proceeds as in the dense data traffic case. The transition time from the last received bit "1" to the standby mode is proportional to the value of the AM rejection capacitor at Pin 9. For C_{AM} = 10nF, the "receive data" to "standby" transition occurs after 4 seconds from the last "1". Therefore, long strings of "0"s can be transmitted and received. The standby function may be disabled with proper bias at Pin 9 (external components).

TX-to-RX and RX-to-TX Switching Times

With the listen-while-talk capability the TX-to-RX and the RX-to-TX switching times have the meaning of TX_{ON}-to-TX_{OFF} and TX_{OFF}-to-TX_{ON} switching times, respectively. The TX-to-RX and RX-to-TX minimum switching times can be calculated from the maximum data rate. Since one bit can last a minimum of 3µs (NRZ ASK data), this may be considered the minimum switching time.

Data Rate

The maximum data rate is 300kbit/s NRZ ASK. This data rate was achieved on a twisted-pair cable with a 150kHz, 50% duty cycle square wave fro data. The data rate depends on the BPF (between Pins 3 – 4 and 5 – 6), on the AM detector capacitor for delay, C_{DET} (between Pins 7 and 8), on C_{AM} (Pin 9) for capture of leading bits, and on the desired impulse noise immunity for delay, C_{IMP} (Pin 10).

AC Line Coupling Network

One or two (120V or 240V and 277V AC RMS) coupling capacitors rated 600V are connected in series with the primary of a 1:1 transformer and connected to the AC line. The transformer secondary may be tuned to the carrier frequency by a capacitor (TOKO transformer, low data rates) or no secondary tuning capacitor for higher data rates (AIE Magnetics transformer). Two back-to-back zener diodes must be placed between Pins 1 and 20 for the IC transient protection (1N4744 or 1N6275). The transformer secondary carries DC bias current between Pins 1 and 20 of the IC. This coupling network itself attenuates to below the RX input sensitivity the 50 or 60Hz and their harmonic frequencies. In a coaxial cable application the transformer can be replaced with a coupling capacitor.

Receiver (RX)

The typical RX sensitivity is $1.5mV_{RMS}$. For less sensitivity, adjust the turn ratio of the coupling transformer or insert loss in the bandpass filter. The RX-only function can be implemented by not using the oscillator and by grounding the TX input. The maximum data rate is 300kbit/s. The power supply rejection ratio (PSRR) is 80dB for 60Hz and 120Hz. The RX is composed of the following blocks:

The Input Amplifier/Limiter limits its output signals to $1.2V_{P-P}$. The maximum input carrier signal can be $70V_{P-P}$. The gain is 24dB. The input amplifier bandpass characteristic has the upper –3dB frequency internally fixed at 300kHz. The lower –3dB frequency is adjustable with the C_{HPF} capacitor from Pin 2 to GND. For maximum RX sensitivity CHPF = 10nF at f_{CXR} = 120kHz. A C_{HPF} = 0.1µF value attenuates 60Hz by 50dB and 120Hz by 45dB.

The Bandpass Filter is differential RLC bandpass filter which can be connected from Pins 3, 6 to Pins 4, 5. The LC values are the same as the oscillator LC values (see Pins 13 and 14). The formulae relating the BW_{-3dB} to the RLC values are:

$$\frac{BW_{-3dB}}{\omega_{CXR}} = \frac{(\omega_{CXR} \cdot L)}{(2 \cdot R)} = \frac{1}{Q}$$

$$\frac{BW_{-3dB}}{\omega_{CXR}} = \frac{1}{(\omega_{CXR} \cdot 2 \cdot C \cdot R)} = \frac{1}{Q}$$

$$BW_{-3dB} = \frac{(\omega_{CXR} \cdot \omega_{CXR} \cdot L)}{(2 \cdot R)}$$

$$BW_{-3dB} = \frac{1}{(2 \cdot C \cdot R)} \quad \text{and}$$

$$\omega_{CXR} = 2 \cdot f_{CXR}$$

If no bandpass filter is required, connect Pin 3 to 4 and Pin 5 to 6 ($R_1 = R_2 = 0\Omega$).

The Amplitude Detector is a Gilbert phase detector with a single differential input. The compared signals are always in phase and the demodulated output is a full rectified wave, function of the bias current, the carrier amplitude, and the collector load. The detected voltage is developed across a differential capacitive load between Pin 7 (+) and Pin 8 (–). DC offset is caused by the line impedance modulation.

The AM Rejection Circuit stabilizes the DC average value of the envelope by adding or subtracting a series voltage to the voltage of the detector capacitor. The AM rejection is 40dB at a modulation rate of 120Hz. The value of the AM rejection capacitor CAM (Pin 9 to GND) determines the transition times to and from receive data and standby.

The Slicing Comparator has current output and a fixed threshold of 50mV.

The Impulse Filter consists of a capacitor, C_{IMP}, at the output of the comparator, from Pin 10 to GND. This capacitor is charged or discharged with constant current from the comparator, causing the voltage variation to be a constant slope in time. Narrow current impulses will not last long enough to fully charge or discharge the capacitor.

$2V_{BE}$ Voltage Hysteresis provides a voltage interval in which the C_{IMP} voltage ramps and in which both inputs to the SR flip-flop are zero.

The Flip-Flop is an SR type, with an open-collector transistor output at Pin 11. The transistor can switch a maximum load of 5mA.

Receiver Delays and Maximum Data Rate

The total receiver delay is a sum of delays, where t_{DET} (sec) is the detector delay, t_{IMP} (sec) is the impulse filter delay, and 2µs is the approximate receiver delay with no C_{DET} and no C_{IMP}:

t_D (sec) = total receiver delay
= t_{DET} (sec) + t_{IMP} (sec) + 2µs

The maximum bit rate, in the no-return-to-zero, amplitude shift keying data format is determined by: Maximum bit rate MRZ ASK (bit/sec) < $1/t_D$ (sec^{-1})

NOTE:
The C_{DET} and C_{IMP} values so calculated are for guidance and the user shall determine the optimal performance values in a range between 0.1 times to 10 times the calculated values (power line environment assumed). For twisted-pair or coaxial cables the calculated values are close to optimal. Based on power line applications made at 100bits/sec and at 50kbits/sec, the C_{IMP} / C_{DET} capacitor ratio ranges from 100:1 to 1:1.

Transmitter, TX

The transmitter includes an oscillator, a line driver, and a drive switch.

The TTL Switch is a low power TTL gate that switches on/off the bias current for the line driver. A logic "1" at Pin 19 (TXIN) enables the line driver and carrier is being sent on the line. A logic "0" disables the driver.

The Oscillator is a differential transistor pair. It can be configured as a Colpitts LC oscillator, as a Pierce crystal oscillator, or used with external input (microprocessor clock divided to the carrier frequency). When the TX drive is off, the carrier leak is less than –90dBmO. Pin 18 can be used as input for an external oscillator. Grounding Pin 12 disables the oscillation process.

The Line Driver is a class AB push-pull stage with optional external complementary transistor pair for increased current capability. The TX output impedance is 40Ω in the off-state (receive mode) and less than 2Ω in the on-state (transmit mode). Note that in the transmit mode one receives its own signal. To increase the amplitude of the transmitter, add a feedback resistor in the driver amplifier feedback path at Pin 16.

By itself the NE5050 is capable of driving consumer line impedance of 50Ω (40mA peak/80mA peak non-repetitive), the THD being less than 2%. With complementary transistors, 10Ω industrial loads can be driven. With complementary Darlington transistors, 1Ω industrial loads can be driven.

One design objective was to provide the user with a flexible IC modem for residential as well as for industrial AC lines, for

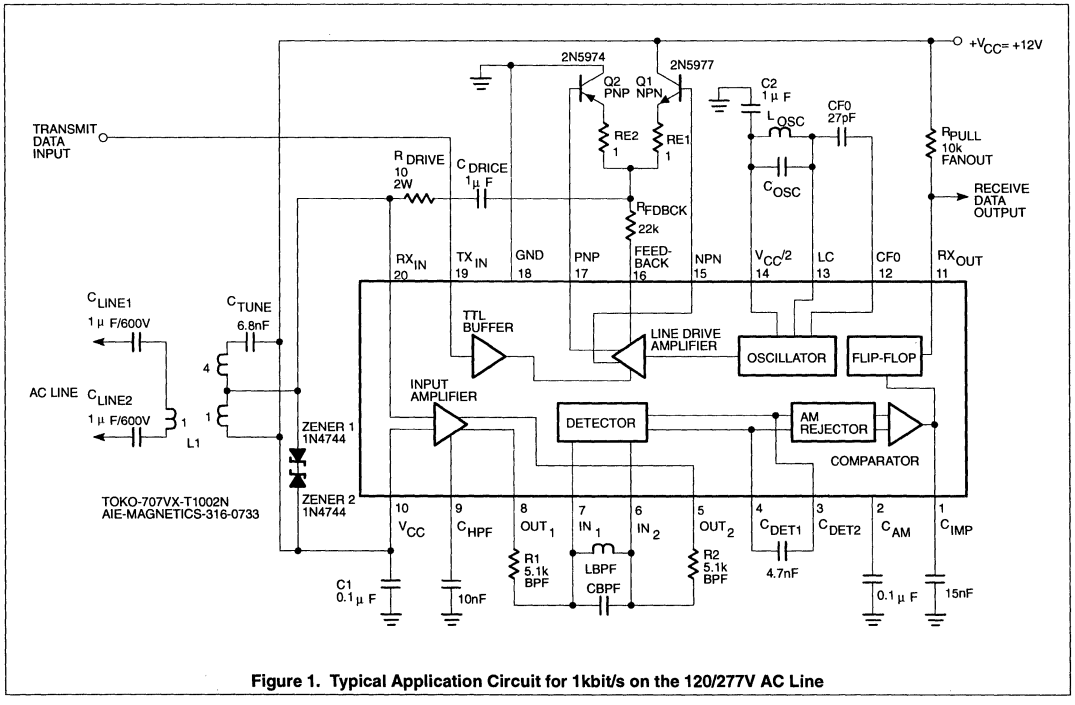


Figure 1. Typical Application Circuit for 1kbit/s on the 120/277V AC Line

twisted-pair, and for coaxial cables. The IC modem can be used for control functions and data applications. Practical observations of power line noise point to a data rate upper boundary of 1kbit/sec. The main sources of interference are the light dimmers. Software for error correction can be used for improved error rates. Two system configurations can be implemented: an ASK system and a non-coherent FSK system. The non-coherent FSK system can continue to transmit ASK data if the other channel is made unusable by CW interference. High-voltage transient protection and filtering are accomplished with user-selected external components.

Additional flexibility is provided by the chip architecture: one-IC real-time repeater, one-IC dual-frequency gateway, external oscillator input port, the listen-while-talk capability (CSMA/CD), immediate TX-to-RX switching, ASK and FSK, and ASK-multinode single-frequency network.

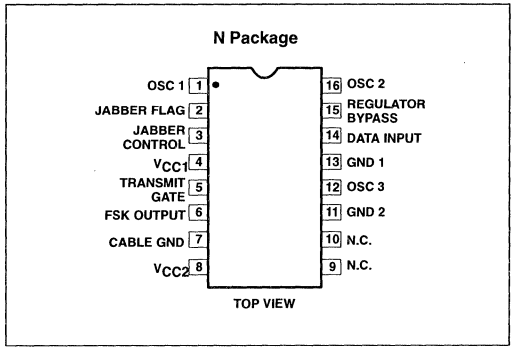
The modem can be used for control systems and data applications in homes and other consumer environments and in industry.

High-speed FSK modem transmitter — NE5080

DESCRIPTION

The NE5080 is the transmitter chip, of a two-chip set, designed to be the heart of an FSK modem. (The NE5081 is the receiver chip.) The chips are compatible with the IEEE 802.4 standard for a "Single-Channel" Phase-Continuous-FSK Token Bus." The specifications shown in this data sheet are those guaranteed when the transmitter is tuned for the frequencies given in the 802 standard. However, both the NE5080 and the NE5081 may be used at other frequencies. The ratio of logic high to logic low frequencies is normally at 1.67 to 1.00 at any center frequency; however, it can be varied externally. (See AN1950.)

PIN CONFIGURATION



FEATURES

- Meets IEEE 802.4 standard
- Data rates to several Megabaud
- Half- or full-duplex operation
- Jabber function on-chip

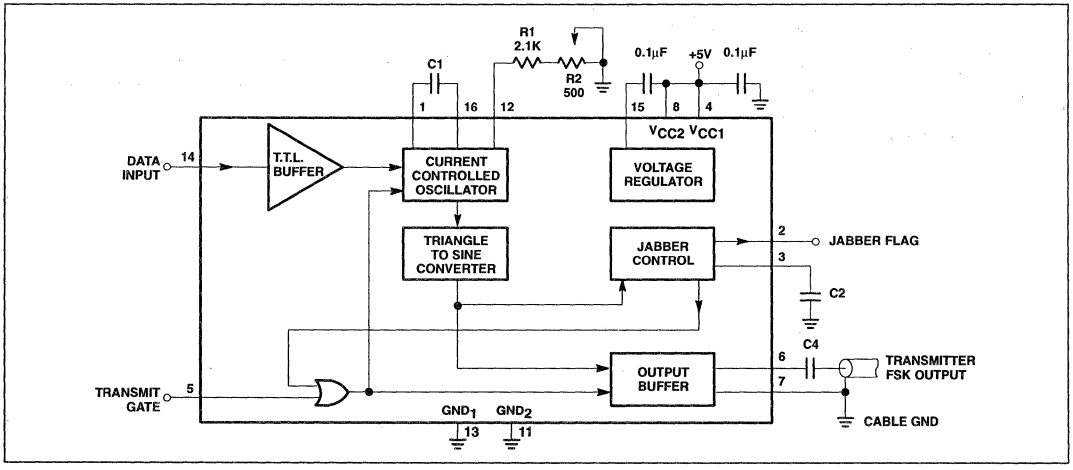
APPLICATIONS

- Local Area Networks
- Point-to-point communications
- Factory automation
- Process control
- Office automation

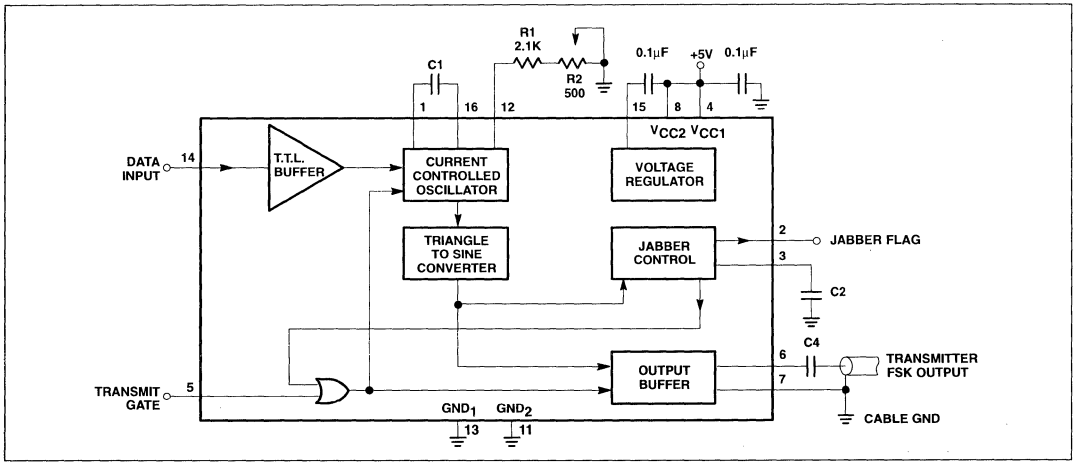
ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5080N	0406C

BLOCK DIAGRAM



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC1} V_{CC2}	Supply voltage	+6	V
V_{IN}	Input voltage range (Data, Gate)	–0.3 to V_{CC}	V
P_D	Power dissipation	800	mW
T_A	Operating temperature range	0 to + 70	°C
T_J	Maximum junction temperature	+150	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead temperature (soldering, 10 sec)	300	°C

NE5080 PIN FUNCTION

PIN	FUNCTION
1	**OSC 1:** One end of the external capacitor used to set the carrier frequency.
2	**Jabber Flag:** This pin goes to a logic high if the transmitter attempts to transmit for a longer time than allowed by the Jabber control function.
3	**Jabber Control:** Used to control transmit time. See note on Jabber function.
4	**V_{CC1}:** Voltage supply.
5	**Transmit Gate:** A logic flow on this pin will enable the transmitter; a logic high will disable it.
6	**Transmitter FSK Output**
7	**Cable Ground:** The shield of the coax cable should be connected to this pin and to Pin 11.
8	**V_{CC2}:** Connect to Pin 4 close to device.
9	**No Connection**
10	**No Connection**
11	**Ground 2:** Connect to Analog ground close to device.
12	**OSC 3:** A variable resistor between this point and ground is used to set the carrier frequencies.
13	**Ground 1:** Connect to Analog close to device.
14	**Data Input**
15	**Regulator Bypass:** A bypass capacitor between this pin and V_{CC1} is required for the internal voltage regulator function.
16	**OSC 2:** One end of a capacitor that is between Pin 1 and Pin 16 and is used to set the carrier frequency.

High-speed FSK modem transmitter | NE5080

GENERAL DESCRIPTION

The NE5080 is designed to transmit high frequency asynchronous data on coaxial cable, at rates from DC to 2M baud (see Note 1). The chip accepts serial data and transmits it as a periodic signal whose frequency depends on whether the data is high or low.

The device is meant to operate at a frequency of 6.25MHz for a logic high and 3.75MHz for a logic low (see Note 2). The frequency is set up by external trimming components; however, the ratio of the high and low frequencies is set internally and cannot be altered.

The FSK output can be turned off by use of the transmit gate pin. When turned off, the transmitter has a high output impedance and the oscillator is disabled.

The length of time a transmitter can transmit can be controlled by the use of the Jabber control pin (see description of Jabber Control Pin).

Jabber Control Pin

During the time the transmitter is transmitting, this pin sources a current. This current can be used to set the maximum time that the transmitter can be on. There are three options that can be used:

1. Use the current to charge a capacitor. When the voltage across the cap gets to approximately 1.4V, the transmitter will turn off. A logic low applied to Pin 3 will reset the Jabber function; an open collector output should be used for this purpose. A logic high applied to the pin will disable the transmitter.
2. Use to externally sense the current and have external circuitry to control the length of time the transmitter is on.
3. The pin can be tied to ground and is then not active. Transmission is then controlled solely by the signal at the transmit gate pin.

Jabber Flag Pin

This pin will go to a logic high when the Jabber Control pin is used to shut off the transmitter. It will latch and can be reset by applying a logic low to the Jabber Control pin.

NOTES:
1. The NE5080 is capable of transmitting up to 1M baud of differential Manchester code at a center frequency of 5MHz.
2. Although the chip is designed to meet the requirements of IEEE standard 802.4 (Token-Passing Single-Channel Phase-Continuous-FSK Bus), it can be used at other frequencies.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
t_S	Setup time	Data in	Gate on	Figure 1	2	0.1		µs
t_A	Delay time	Output freq. change	Data transition	Figure 2			150	ns
t_B	Delay time	Output disabled	Gate off	Figure 3		0.4	2	µs
t_C	Delay time	Output disabled	Jabber control	Figure 4			100	ns
t_D	Delay time	Jabber flag	Jabber control	Figure 5			100	ns
	Jabber control reset Pulse width (Logic low)				100			ns

DC ELECTRICAL CHARACTERISTICS

$V_{CC1,2}$ = 4.75–5.25V, T_A = 0°C to +70°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_1	Output frequency (Logic high)	Data input ≥2.0V (See Note 1)	6.17	6.25	6.33	MHz
f_0	Output frequency (Logic low)	Data input ≤0.8V (See Note 1)	3.67	3.75	3.83	MHz
V_O	Output amplitude	Data input ≥2.0V or ≤0.8V Output Load = 37.5Ω	0.5		1.0	V_{RMS}
R_{OFF}	Output impedance (gated off)	Transmit gate ≥2.0V	100			kΩ
R_{ON}	Output impedance (gated on)	Transmit gate ≤0.8V			37.5	Ω
C_O	Output capacitance	Transmit gate ≥2.0V or ≤0.8V			10	pF
V_F	Feedthrough	Transmit gate ≥2.0V 2.0MHz sq. wave (TTL levels) input			1	mV_{RMS}
I_J	Jabber current	Transmit gate ≤0.8V Input ≥2.0V or ≤0.8V		1.25		µA
I_{CC}	Supply current	V_{CC1} connected to V_{CC2}		75	100	mA
Logic levels						
	Data Input					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V
I_{IH}	Input current	V_{IN} = 2.4V			40	µA
I_{IL}	Input current	V_{IN} = 0.4V			–1.6	mA
	Transmit gate					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V
I_{IH}	Input current	VG = 2.4V			40	µA
I_{IL}	Input current	VG = 0.4V			–1.6	mA
	Jabber flag					
V_{OH}	Logic high	I_{OH} = –400µA	2.4			V
V_{OL}	Logic low	I_{OL} = 4.0mA			0.4	V
	Jabber control					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V

NOTE:
1. Tuned per instructions in AN195.

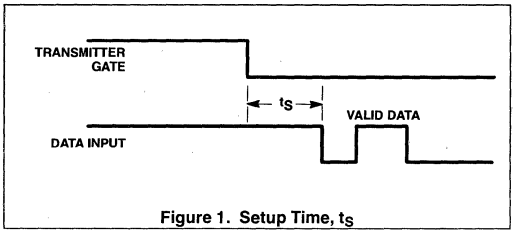


Figure 1. Setup Time, t_S

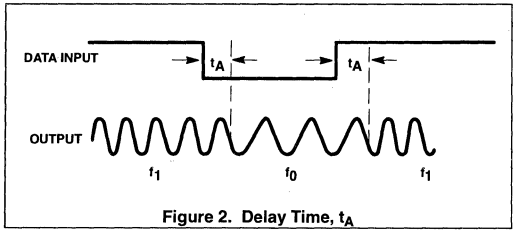


Figure 2. Delay Time, t_A

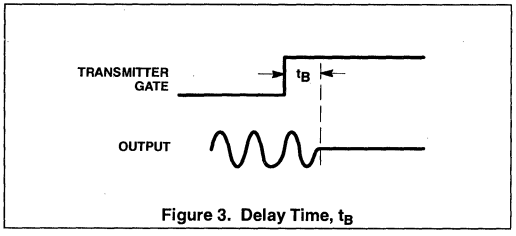


Figure 3. Delay Time, t_B

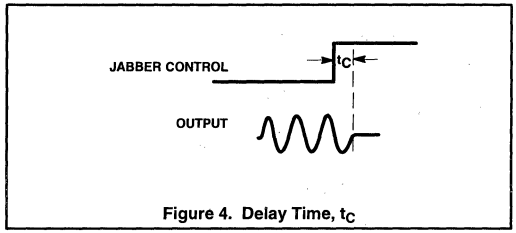


Figure 4. Delay Time, t_C

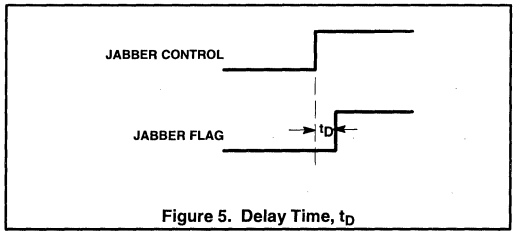


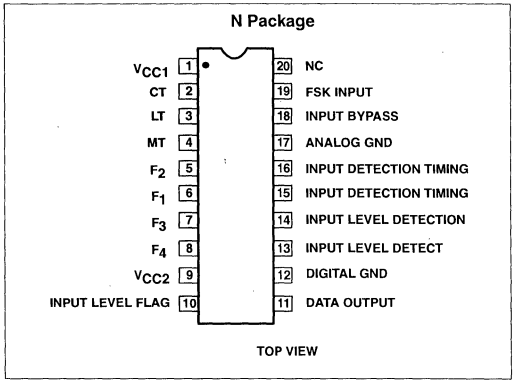
Figure 5. Delay Time, t_D

High-speed FSK modem receiver — NE5081

DESCRIPTION

The NE5081 is the receiver chip of a two-chip set designed to operate as an FSK modem (the NE5080 is the transmitter chip). The chips are compatible with the IEEE 802.4 standard for a "Single-Channel Phase-Continuous-FSK Token Bus." The specifications given in this data sheet are those guaranteed when the receiver is tuned to the frequencies given in the 802 standard. However, the receiver will work at other frequencies.

PIN CONFIGURATION



FEATURES

- Meets IEEE 802.4 standard
- Data rates to several Megabaud
- Half- or full-duplex operation
- Low bit rate error (10^{-12} typical)

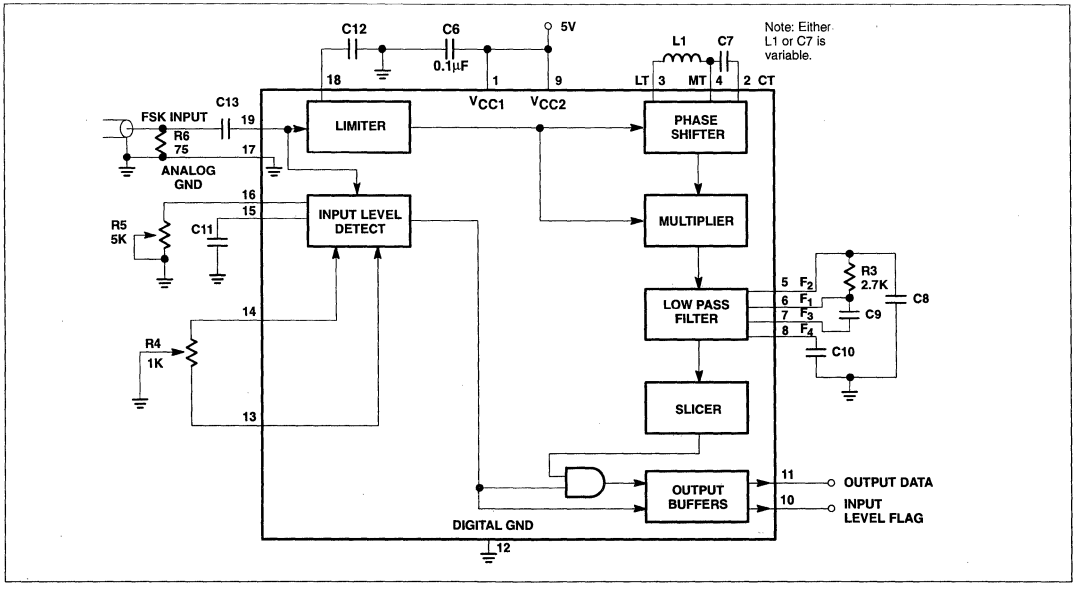
APPLICATIONS

- Local Area Networks
- Point-to-point communications
- Factory automation
- Process control
- Office automation

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Dual In-Line Package (DIP)	0°C to +70°C	NE5081N	0408B

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$

SYMBOL	PARAMETER	RATING	UNIT
V_{CC1} V_{CC2}	Supply voltage	+6	V
V_{IN}	Input voltage range	−0.3 to $+V_{CC}$	V
I_{DO}	Output (Data, Level detect) Max sink current	20	mA
P_D	Maximum power dissipation, $T_A = 25°C$, (still-air)[1] N package	1690	mW
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec. max)	300	°C
	Max differential voltage between analog and digital grounds	100	mV

NOTE:
1. Derate above 25°C as follows:
   N package at 13.5mW/°C.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1, 2} = 4.75–5.25V$. External LC circuit tuned to 5MHz. Input level detect set at $16mV_{RMS}$, $T_A = 0°C$ +70°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_0	Logic Low Frequency	External LC tuned to 5MHz	3.67	3.75	3.83	MHz
f_1	Logic High Frequency	External LC tuned to 5MHz	6.17	6.25	6.33	MHz
IN_{DL}	Minimum Input Detect Level	Minimum input level that is detected as carrier (See Note 2 in General Description)	5		50	mV_{RMS}
	Logic Levels:					
V_{OL}	Data Output	$I_{OL} = 4.0mA$ $V_{IN} > 16mV_{RMS}$ Freq = f_0			0.4	V
V_{OH}	Data Output	$I_{OH} = -400\mu A$ $V_{IN} > 16mV_{RMS}$ Freq = f_1	2.4			V
V_{OH}	Data Output	$I_{OH} = -400\mu A$ $V_{IN} < 5mV_{RMS}$ Freq = f_0	2.4			V
V_{OL}	Input Detect Flag	$I_{OL} = 4.0mA$ $V_{IN} = 0V_{RMS}$			0.4	V
V_{OH}		$I_{OH} = -400\mu A$ $V_{IN} > 16mV$	2.4			V
I_{CC}	Supply Current	$V_{CC} = 5.25V$ (V_{CC1} connected to V_{CC2}) $V_{IN} = 1.0V_{RMS}$ Freq = f_1 or f_0			50	mA
BER	Bit Error Rate	Input Signal > $16mV_{RMS}$ maximum in-band noise = $1.6mV_{RMS}$		10^{-12}	10^{-9}	

AC ELECTRICAL CHARACTERISTICS (AN195, Figure 5 with a 100KHz $1V_{P-P}$)

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
t_B	Delay Time	Input Level Detect Flag	Input On	Figure 1		0.05	1	µs
t_C	Delay Time	Input Level Detect Flag	Input Off	Figure 1	0.5	1.5	2.5	µs
t_D	Delay Time	Output Enabled	Input On	Figure 2			2	µs
t_E	Delay Time	Output Disabled	Input Off	Figure 2	0.5	1.5	2.5	µs
	Required Delay	Carrier Turn Off	Valid Data End		2			µs

GENERAL DESCRIPTION

The NE5081 will accept an FSK-encoded signal and provide the demodulated digital data at the output. It is optimized to work at frequencies specified in IEEE 802.4—Token-Passing Single-Channel Phase-Continuous-FSK Bus—(i.e., 3.75MHz and 6.25MHz). However, it will work at other frequencies.[1]

Its normal acceptable input signal level range is from $16mV_{RMS}$ to $1V_{RMS}$. This can be adjusted.[2]

The receiver will yield an undetected "Bit Error Rate" of 10^{-9} or lower when receiving signals with a 20dB signal-to-noise ratio. It has a maximum output Jitter of $\pm$ 40ns.[3]

NOTES:

1. The receiver can be tuned to accept different frequencies by adjustment of the LC circuit shown in Figure 7. However, the external components have been optimized for 3.75MHz and 6.25MHz. See "Determining Component Values" for use at other frequencies.
2. Input Level Detect
   This is a method of turning off the output of the receiver when the input signal falls below an acceptable level. This level is adjustable within the range given in the electrical specification section. The purpose of this function is to minimize the effect of noise on receiver performance and to indicate when there is an acceptable signal present at the input. All specifications given in this data sheet are with the input level detection set at $16mV_{RMS}$.
3. Jitter (Definition)
   This is a measure of the ability of the receiver to accurately reproduce the timing of its FSK-coded digital input. The spec indicates the error band in the timing of a logic level change.

FUNCTION TABLE

PIN	FUNCTION
1	**V_{CC1}:** Should be connected to the 5V supply and Pin 9.
2	**CT:** One end of an external capacitor that is used to tune the receiver.
3	**LT:** One end of an indicator that is used to tune the receiver.
4	**MT:** The junction of the capacitor and inductor used for tuning the receiver.
5	**F2**
6	**F1** Pins 5, 6, 7, 8 are used for a low-pass filter to remove carrier
7	**F3** harmonics from the data output.
8	**F4**
9	**V_{CC2}:** Connect to Pin 1 (see Pin 1 function) close to the device.
10	**Input Level Flag:** This pin is used to indicate when there is a signal at the input that is greater than the level set by the input level detection circuitry. A logic high indicates an input greater than the set level.
11	**Data Output:** Supplies T^2L level data that corresponds to the FSK input received.
12	**Digital Ground:** Should be connected to digital ground.
13, 14	**Input Level Detect:** These pins are used to set the level of input signal that the device will accept as valid.
15	**Input Detection Timing:** An external capacitor between this pin and ground is used to determine the time from carrier turn-off to output disable.
16	**Input Detection Timing:** Same as Pin 15, except that a resistor goes between this pin and ground. The values of the C and R depend on the carrier frequency. The values given in this data sheet are for a 5MHz carrier center frequency.
17	**Analog Ground:** Connect to analog ground close to the device.
18	**Input Bypass:** A capacitor between this pin and ground is used to bypass the input bias circuitry.
19	**Input:** The FSK signal from the cable goes to this pin.
20	**No Connection.**

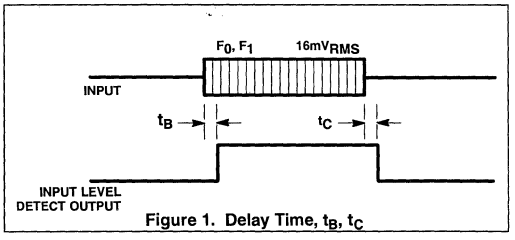


Figure 1. Delay Time, t_B, t_C

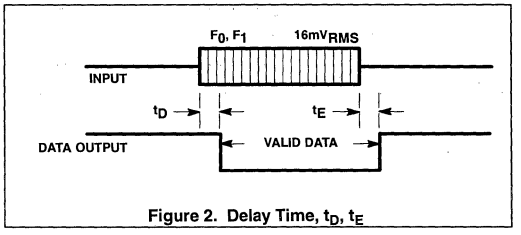


Figure 2. Delay Time, t_D, t_E

Coaxial transceiver interface for Ethernet/Thin Ethernet — NE8392A

DESCRIPTION

The NE8392A Coaxial Transceiver Interface (CTI) is a coaxial line driver/receiver for Ethernet (10base5) and Thin Ethernet (10base2) local area networks. The CTI is connected between the coaxial cable and the Data Terminal Equipment (DTE) and consists of a receiver, transmitter, collision detector, heartbeat generator and jabber timer (see Block Diagram). The transmitter output connects directly to a doubly terminated 50Ω cable, while the receiver output, collision detector output and transmitter input are connected to the DTE through isolation transformers. Isolation between the CTI and the DTE is an IEEE 802.3 requirement that can be met on signal lines by using a set of pulse transformers normally available in a standard 16-pin DIP. Power isolation for the CTI is achieved using DC-to-DC conversion through a power transformer (see Figure 1, Connection Diagram).

During transmission the jabber timer is initiated to disable the CTI transmitter in the event of a longer than legal length data packet. Collision detection circuitry monitors the signals on the coaxial cable to determine the presence of colliding packets and signals the DTE in the event of a collision. At the end of every transmission the heartbeat generator creates a pseudo collision for a short time to ensure that the collision circuitry is functioning correctly. The heartbeat function can be disabled for repeater applications.

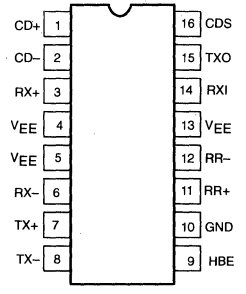
The CTI is normally part of a three chip set that implements a complete Ethernet/ Thin Ethernet network interface for a DTE (see Figure 2, Interface Diagram). The other chips are a Serial Network Interface (SNI) and a Network Interface Controller (NIC). The SNI provides Manchester Encoding and Decoding while the NIC handles the media access protocol and buffer management tasks.

FEATURES

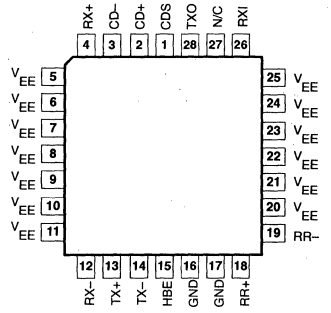
- Compatible with Ethernet II, IEEE 802.3 10base5 and 10base2, and ISO 8802/3 interface specifications
- Integrates all transceiver electronics except signal and power isolation
- Only one external resistor required for setting coaxial signaling current
- Jabber timer function integrated on chip
- Heartbeat generator can be externally disabled for operation as IEEE 802.3 compatible repeaters
- On-chip precision voltage reference for receive mode collision detection

PIN CONFIGURATION

N PACKAGE



A PACKAGE



- Squelch circuitry on all signal inputs rejects noise
- Full ESD protection
- Standard 16-pin DIP with special lead frame minimizes the operating die temperature
- Power-on reset prevents glitches on coaxial cable during power up.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE8392AN	0406C
28-Pin Plastic Lead Chip Carrier (PLCC)	0 to +70°C	NE8392AA	0401F

PIN DESCRIPTIONS

PIN NO. N PKG	PIN NO. PLCC	SYMBOL	DESCRIPTION
1 2	2 3	CD+ CD–	Collision Outputs. Balanced differential line driver outputs which send a 10MHz oscillation signal to the DTE in the event of a collision, jabber interrupt or heartbeat test.
3 6	4 12	RX+ RX–	Receiver Outputs. Balanced differential line driver outputs which send the received signal to the DTE.
7 8	13 14	TX+ TX–	Transmitter Inputs. Balanced differential line receiver inputs which accept the transmission signal from the DTE and apply it to the coaxial cable at TXO.
9	15	HBE	Heartbeat Enable. The heartbeat function is disabled when this pin is connected to V_{EE} and enabled when connected to GND or left floating.
11 12	18 19	RR+ RR–	External Resistor. A 1kΩ (1%) resistor connected between these pins establishes the signaling current at TXO. RR– is internally connected to V_{EE}.
14	26	RXI	Receiver Input. This pin is connected directly to the coaxial cable. Received signals are equalized, amplified, and sent to the DTE through the RX± pins.
15	28	TXO	Transmitter Output. This pin is connected directly (Thin Ethernet) or through an external isolating diode (Ethernet) to the coaxial cable.
16	1	CDS	Collision Detect Sense. Ground sense connection for the collision detection circuitry. This pin should be directly connected to the coaxial cable shield to prevent ground drops affecting the collision threshold voltage.
10	16 17	GND	Positive Supply Pin.
4 5 13	5 to 11 20 to 25	V_{EE}	Negative supply pins. These pins also serve as a low thermal resistance path for extracting heat from the die. They should, therefore, be connected to a large metal area on the PC board.

NOTE:
1. The IEEE 802.3 name for CD is CI; for RX is DI; for TX is DO.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage[1]	–12	V
V_{IN}	Voltage at any input[1]	0 to –12	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec.)	+300	°C
T_J	Recommended max junction temperature[2]	+130	°C
θ_{JA}	Thermal impedance (N and A packages)	60	°C/W

NOTE:
1. 100% measured in production.
2. The junction temperature is calculated from the following expression:

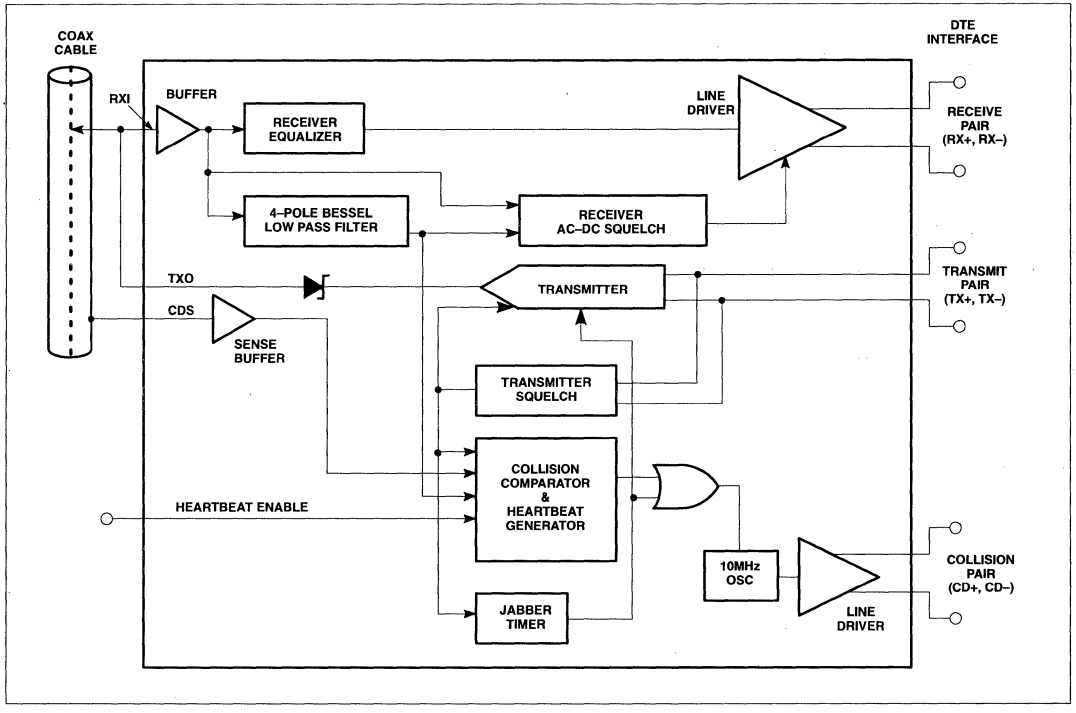
$$T_J = T_A + \theta_{JA}[V_{EE}(0.075 + n \times 0.05/100) + 8(V_{EE} - 2) / R]$$

where

T_A = Ambient temperature in °C.
θ_{JA} = Thermal resistance of package.
V_{EE} = Normal operating supply voltage in volts.
n = Percentage transmitter duty cycle.
R = Pull down resistors on the RX and CD pins in Ω.

The N package is specially designed to have a low θ_{JA} by directly connecting the four center Pins 4, 5, 12, and 13 to the die attachment area. These four pins then provide a conductive heat flow path from the die to the PCB where they should be soldered to a large area V_{EE} track. For the A package, Pins 5 to 11 and 19 to 25 should similarly be soldered to a large area V_{EE} and rack.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

V_{EE} = –9V ±5%; T_A = 0°C to +70°C unless otherwise specified[1,2]. No external isolation

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{POR}	Power–on reset voltage. Transmitter disabled for $\|V_{EE}\| < \|V_{POR}\|$			–6.5		V
I_{EE}	Supply current non–transmitting			–80	–130	mA
	Supply current transmitting			–125	–180	mA
I_{RXI}	Receive input bias current	V_{RXI} = 0V	–2		+25	µA
I_{CDS}	Cable sense input bias current	V_{CDS} = 0V		+2	+6	µA
V_{IH}	HBE input HIGH voltage		V_{EE} +1.4			V
V_{IL}	HBE input LOW voltage				V_{EE} +0.4	V
I_{IH}	HBE input HIGH current	V_{HBE} = 0V		250	500	µA
I_{IL}	HBE input LOW current	V_{HBE} = V_{EE}		–500	–1000	µA
I_{TDC}	Transmit output DC current level[3]		–37		–45	mA
I_{TAC}	Transmit output AC current level[3]		±28		±I_{TDC}	mA
I_{TX10}	Transmit current	V_{TXO} = –10V	–250		+250	µA
V_{TCOM}	Transmitter output voltage compliance[4]				–3.7	V
V_{CD}	Collision threshold[5]	Measured by applying DC voltage at RXI	–1450	–1530	–1580	mV
V_{OD}	Differential output voltage – non idle at RX± and CD±[6]		±600		±1200	mV
V_{OB}	Differential output voltage imbalance – idle at RX± and CD±[7]				±40	mV
V_{OC}	Output common mode voltage at RX± and CD±		–1.5	–2	–2.5	V
V_{RS}	Receiver squelch threshold	V_{RXI} average DC	–130	–250	–370	mV
V_{TS}	Transmitter squelch threshold	(V_{TX+} – $V_{TX–}$) peak	–175	–225	–300	mV
R_{RXI}	Shunt resistance at RXI non–transmitting		100			kΩ
C_{RXI}	Input capacitance at RXI			2		pF
R_{TXO}	Shunt resistance at TXO transmitting			10		kΩ

NOTES:

1. Currents flowing into device pins are positive. All voltages are referenced to ground unless otherwise specified. For ease of interpretation, the parameter limit that appears in the MAX column is the largest value of the parameter, irrespective of sign. Similarly, the value in the MIN column is the smallest value of the parameter, irrespective of sign.
2. All typicals are for V_{EE} = –9V and T_A = 27°C.
3. I_{TDC} is measured as (V_{MAX} + V_{MIN})/(2 x 25) where V_{MAX} and V_{MIN} are the max and min voltages at TXO with a 25Ω load between TXO and GND. I_{TAC} is measured as (V_{MAX} – V_{MIN})/(2 x 25).
4. The TXO pin shall continue to sink at least I_{TDC} min when the idle (no signal) voltage on this pin is –3.7V.
5. Collision threshold for an AC signal is within 10% of V_{CD}.
6. Measured on secondary side of isolation transformer (see Connection Diagram, Figure 1). The transformer has a 1:1 turns ratio with an inductance between 30 and 100µH at 5MHz.
7. Measured as the voltage difference between the RX pins or the CD pins with the transformer removed.

TIMING CHARACTERISTICS

V_{EE} = –9V ±5%; T_A = 0 to 70°C, unless otherwise specified[1]. No external isolation diode on TXO.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{RON}	Receiver start up delay RXI to RX± (Figure 3) First received bit on RX±	V_{RXI} = –2V peak			5	bits
	First validly timed bit on RX±				t_{RON} +2	bits
t_{RD}	Receiver prop. delay RXI to RX±	V_{RXI} = –2V peak		35	50	ns
t_{RR}	Differential output rise time on RX± and CD±[2,3]			5		ns
t_{RF}	Differential output fall time on RX± and CD±[2,3]			5		ns
t_{OS}	Differential output settling time on RX± and CD± to V_{OB} = 40mV[2] (see Figure 5)			1		µs
t_{RJ}	Receiver and cable total jitter			±3		ns
t_{RHI}	Receiver high to idle time	Measured to +210mV	150		850	ns
t_{RM}	Rise and fall time matching on RX± and CD±	$t_{RF} - t_{RR}$		0.4		ns
t_{TST}	Transmitter start–up delay TX± to TXO (Figure 4)	$V_{TX±}$ = –1V peak				
	First transmitted bit on TXO			1	2	bits
	First validly timed bit				t_{TST} + 2	bits
t_{TD}	Transmitter prop delay TX± to TXO (see Figure 4)	$V_{TX±}$ = 1V peak		35	50	ns
t_{TR}	Transmitter rise time 10% to 90% (see Figure 4)			25		ns
t_{TF}	Transmitter fall time 10% to 90% (see Figure 4)			25		ns
t_{TM}	$t_{TF} - t_{TR}$ mismatch			±2		ns
t_{TS}	Transmitter added skew[4]			±2		ns
t_{TON}	Transmitter turn on pulse width (see Figure 4)	$V_{TX±}$ = 1V peak	10		40	ns
t_{TOFF}	Transmitter turn off pulse width (see Figure 4)	$V_{TX±}$ = 1V peak	150	250	340	ns
t_{CON}	Collision turn on delay (see Figure 6)	0V to –2V step at RXI			13	bits
t_{COFF}	Collision turn off delay (see Figure 6)	–2V to 0V step at RXI			16	bits
t_{CHI}	Collision high to idle time (see Figure 6)	Measured to +210mV	150		850	ns
f_{CD}	Collision frequency (see Figure 6)		8.0	10	12.5	MHz
t_{CP}	Collision signal pulse width (see Figure 6)		35		70	ns
t_{HON}	Heartbeat turn on delay (see Figure 7)		0.6		1.6	µs
t_{HW}	Heartbeat test duration (see Figure 7)		0.5		1.5	µs
t_{JA}	Jabber activation delay measured from TX± to CD± (see Figure 8)		20		60	ms
t_{JR}	Jabber reset delay measured from TX± to CD± (see Figure 8)		250		750	ms

NOTES:
1. All typicals are for V_{EE} = –9V and T_A = 27°C.
2. Measured on secondary side of isolation transformer (see Figure 1, Connection Diagram). The transformer has a 1:1 turn ratio with an inductance between 30 and 100µH at 5MHz.
3. The rise and fall times are measured as the time required for the differential voltage to change from –225mV to +225mV, or +225mV to –225mV, respectively.
4. Difference in propagation delay between rising and falling edges at TXO.

FUNCTIONAL DESCRIPTION

The NE8392A contains four main functional blocks (see Block Diagram). These are:

a. The receiver which takes data from the coaxial cable and sends it to the DTE.

b. The transmitter which receives data from the DTE and sends it onto the coaxial cable.

c. The collision detection and heartbeat generation circuitry which indicates to the DTE any collision on the coaxial cable and tests for collision circuitry functionality at the end of every transmission.

d. The jabber timer which disables the transmitter in the event of a longer than legal length data packet.

Receiver Functions

The receiver consists of an input buffer, a cable equalizer, a 4-pole Bessel low pass filter, a squelch circuit and a differential line driver.

The buffer provides high input resistance and low input capacitance to minimize loading and reflections on the coaxial cable.

The equalizer is a high pass filter that compensates for the low pass effect of the coaxial cable and results in a flatband response over all signal frequencies to minimize signal distortion.

The 4-pole Bessel low pass filter extracts the average DC voltage level on the coaxial cable for use by the receiver squelch and collision detection circuits.

The receiver squelch circuit prevents noise on the coaxial cable from falsely triggering the receiver in the absence of a true signal. At the beginning of a packet, the receiver turns on when the DC level from the low pass filter is lower than the DC squelch threshold. For normal signal levels this will take less than 500ns, or 5 bits. However, at the end of a packet, a fast receiver turn off is needed to reject both dribble bits on the coaxial cable and spurious responses due to settling of the on-chip bandpass filter. This is accomplished by an AC timing circuit that disables the receiver if the signal level on the coaxial cable remains high for typically 250ns and only enables the receiver again after approximately 1µs. Figures 3 and 5 illustrate receiver timing.

The differential line driver provides typically ±900mV signals to the DTE with less than 7ns rise and fall times. When in idle state (no received signal) its outputs provide <20mV differential voltage offset to minimize DC standing current in the isolation transformer. The line driver outputs are emitter followers and, for Ethernet applications where they drive a 78Ω transmission line, require a 500Ω pull-down resistor to V_{EE}. For Thin Ethernet applications where the AUI cable is not used, the pull-down resistor can be increased to 1.5kΩ to save power consumption.

Transmitter Functions

The transmitter has differential inputs and an open collector current driver output. The differential input common mode voltage is established by the CTI and should not be altered by external circuitry. Controlled rise and fall times of 25ns (±5ns) minimize higher harmonic components in the transmitted spectrum, while matching of these rise and fall times to typically 2ns minimizes signal jitter. The drive current levels of the CTI are set by an on-chip bandgap voltage reference and an external 1% resistor. An on-chip isolation diode is provided to reduce the transmitter's coaxial cable load capacitance. For Thin Ethernet applications, no further external isolation diode is required, since the NE8392A meets the capacitive loading specifications. For Ethernet applications a further external diode should be added to reduce loading capacitance.

The transmitter squelch circuit ensures that the transmitter can only be enabled by negative-going differential signals of typically greater than 225mV in magnitude and 15ns in duration. The transmitter will be disabled at the end of a packet if there are no negative going signals of greater than 225mV for more than typically 250ns. Figure 4 illustrates transmitter timing.

Collision Functions

The collision detection scheme implemented in the NE8392A is receive mode detection, which detects a collision between any two stations on the network with certainty at all times, irrespective of whether or not the local DTE is producing one of the colliding signals. This is the only detection scheme allowed by the IEEE 802.3 standard for both repeater and non-repeater nodes.

The collision circuitry consists of the 4-pole Bessel low pass filter, a comparator, a precision voltage reference that sets up the collision threshold, a heartbeat generator, a 10MHz oscillator, and a differential line driver.

The collision comparator monitors the DC level at the output of the low pass filter and enables the line driver if it is more negative than the collision threshold. A collision condition is indicated to the DTE by a 10MHz oscillation signal at the CD outputs and typically occurs within 700ns of the onset of the collision. The collision signal begins with a negative-going pulse and ends with a continuous high-to-idle state longer than 170ns. Figure 6 illustrates collision timing.

At the end of every transmission, the heartbeat generator creates a pseudo collision to ensure that the collision circuitry is properly functioning. This pseudo collision consists of a 1µs burst of 10MHz oscillation at the line driver outputs approximately 1µs after the end of the transmission. The heartbeat function can be disabled externally by connecting the HBE (heartbeat enable) to V_{EE}. This allows the CTI to be used in repeater applications. Figure 7 illustrates heartbeat timing.

As with the receiver outputs, the collision outputs also require a pull down resistor to V_{EE} and maintain <20mV differential voltage offset in the idle state to minimize DC standing current in the isolation transformers.

Jabber Functions

The jabber timer monitors the transmitter and inhibits transmission if it is active for longer than typically 30ms. The jabber circuit then enables the collision outputs for the remainder of the data packet and for typically 450ns (unjab time) after it has ended. At this point the transmitter becomes uninhibited. Figure 6 illustrates jabber timing.

Detection of Coaxial Cable Faults

In the NE8392A there is no internal loopback path from the TX inputs to the RX outputs. This means that, when the local DTE is transmitting, the signal will only be present at the receiver outputs RX+ and RX– if it appears on the coaxial cable and is larger than the receiver squelch threshold V_{RS}. If a short circuit fault condition occurs at the cable connector to the CTI, then no signal will appear at the receiver outputs. An intelligent DTE can, therefore, detect this fault. If the fault is an open circuit, then a continuous collision signal will be sent to the DTE, provided the average DC voltage at the RXI pin is greater than the typical collision threshold of –1.53V.

If a short or open circuit occurs elsewhere on the coaxial cable, the resulting reflections can result in an impedance at the CTI of any value between a short circuit and 50Ω, depending on the distance of the CTI from the fault. The upper limit of 50Ω results from the fact that the coaxial cable is terminated in 50Ω at both ends. Faults on the cable itself are, therefore, not guaranteed to be detected by simply monitoring the RX and CD pins when in the transmit mode, and more sophisticated schemes may be necessary.

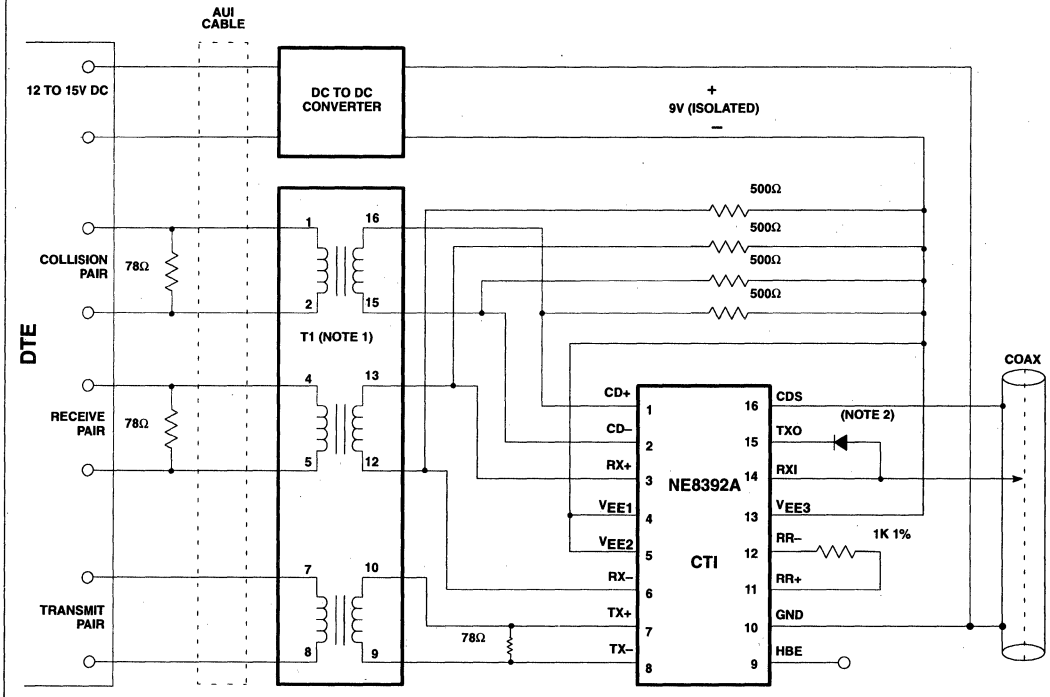


Figure 1. Connection Diagram

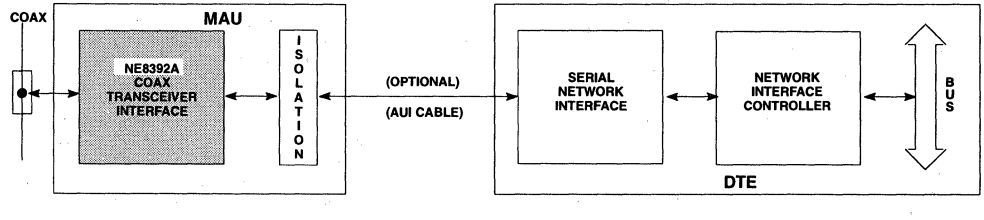


Figure 2. Interface Diagram for Ethernet/Thin Ethernet Local Area Network

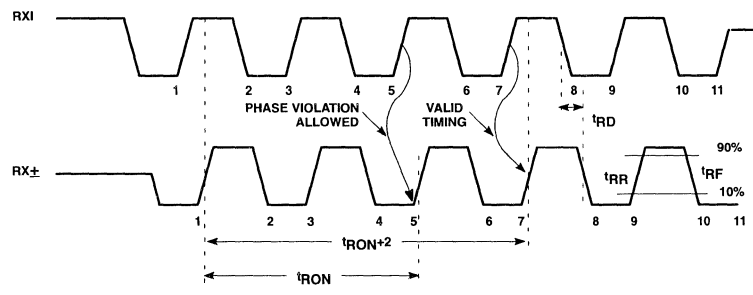


Figure 3. Receiver Timing

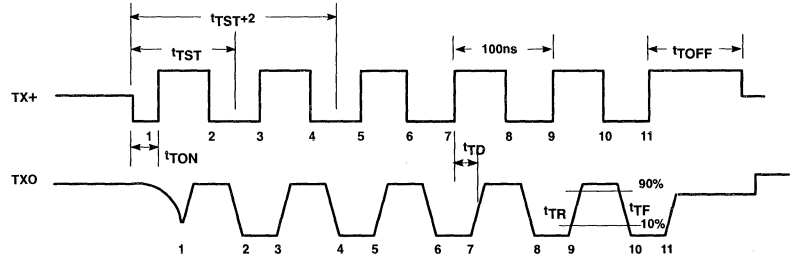


Figure 4. Transmitter Timing

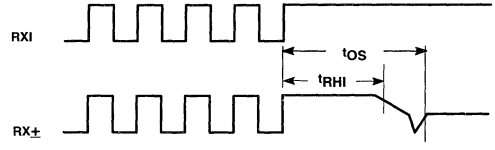


Figure 5. Receiver End–of–Packet Timing

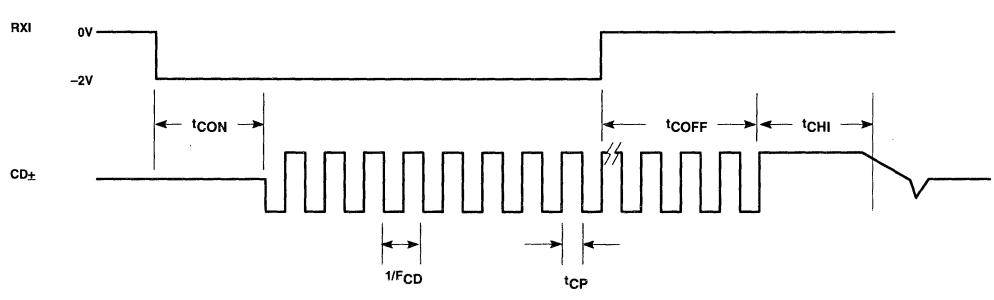


Figure 6. Collision Timing

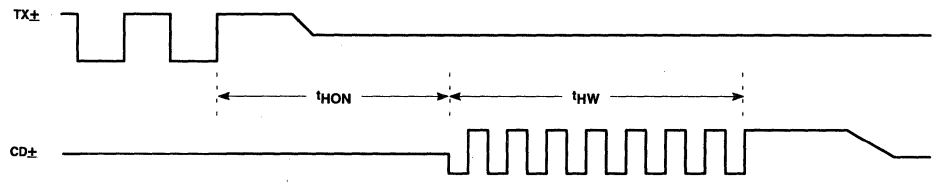


Figure 7. Heartbeat Timing

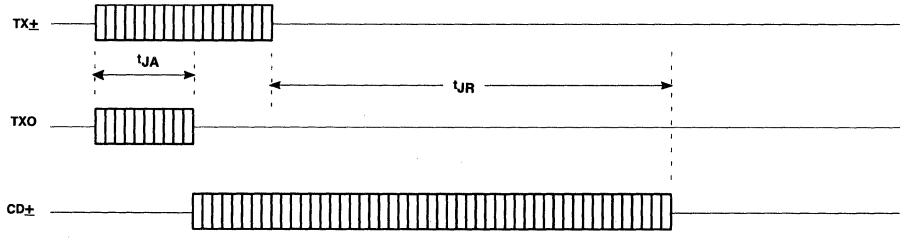


Figure 8. Jabber Timing

Coaxial transceiver interface for Ethernet/Thin Ethernet — NE8392C

DESCRIPTION

The NE8392C Coaxial Transceiver Interface (CTI) is a coaxial line driver/receiver for Ethernet (10base5) and Thin Ethernet (10base2) local area networks. The CTI is connected between the coaxial cable and the Data Terminal Equipment (DTE) and consists of a receiver, transmitter, collision detector, heartbeat generator and jabber timer (see Block Diagram). The transmitter output connects directly to a doubly terminated 50Ω cable, while the receiver output, collision detector output and transmitter input are connected to the DTE through isolation transformers. Isolation between the CTI and the DTE is an IEEE 802.3 requirement that can be met on signal lines by using a set of pulse transformers normally available in a standard 16-pin DIP. Power isolation for the CTI is achieved using DC-to-DC conversion through a power transformer (see Figure 1, Connection Diagram).

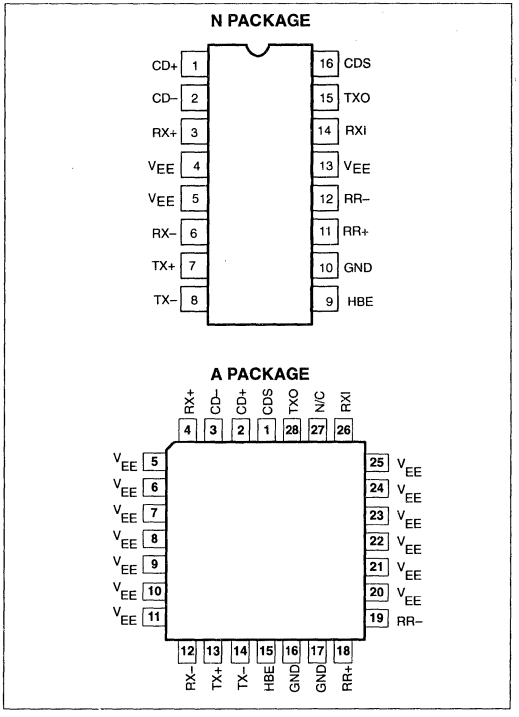
During transmission the jabber timer is initiated to disable the CTI transmitter in the event of a longer than legal length data packet. Collision detection circuitry monitors the signals on the coaxial cable to determine the presence of colliding packets and signals the DTE in the event of a collision. At the end of every transmission the heartbeat generator creates a pseudo collision for a short time to ensure that the collision circuitry is functioning correctly. The heartbeat function can be disabled for repeater applications.

The CTI is normally part of a three chip set that implements a complete Ethernet/ Thin Ethernet network interface for a DTE (see Figure 2, Interface Diagram). The other chips are a Serial Network Interface (SNI) and a Network Interface Controller (NIC). The SNI provides Manchester Encoding and Decoding while the NIC handles the media access protocol and buffer management tasks.

FEATURES

- Compatible with Ethernet II, IEEE 802.3 10base5 and 10base2, and ISO 8802/3 interface specifications
- Integrates all transceiver electronics except signal and power isolation
- Only one external resistor required for setting coaxial signaling current
- Jabber timer function integrated on chip
- Heartbeat generator can be externally disabled for operation as IEEE 802.3 compatible repeaters
- On-chip precision voltage reference for receive mode collision detection

PIN CONFIGURATION



- Squelch circuitry on all signal inputs rejects noise
- Full ESD protection
- Standard 16-pin DIP with special lead frame minimizes the operating die temperature
- Power-on reset prevents glitches on coaxial cable during power up.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE8392CN	0406C
28-Pin Plastic Lead Chip Carrier (PLCC)	0 to +70°C	NE8392CA	0401F

PIN DESCRIPTIONS

PIN NO. N PKG	PIN NO. PLCC	SYMBOL	DESCRIPTION
1 2	2 3	CD+ CD–	Collision Outputs. Balanced differential line driver outputs which send a 10MHz oscillation signal to the DTE in the event of a collision, jabber interrupt or heartbeat test.
3 6	4 12	RX+ RX–	Receiver Outputs. Balanced differential line driver outputs which send the received signal to the DTE.
7 8	13 14	TX+ TX–	Transmitter Inputs. Balanced differential line receiver inputs which accept the transmission signal from the DTE and apply it to the coaxial cable at TXO.
9	15	HBE	Heartbeat Enable. The heartbeat function is disabled when this pin is connected to V_{EE} and enabled when connected to GND or left floating.
11 12	18 19	RR+ RR–	External Resistor. A 1kΩ (1%) resistor connected between these pins establishes the signaling current at TXO. RR– is internally connected to V_{EE}.
14	26	RXI	Receiver Input. This pin is connected directly to the coaxial cable. Received signals are equalized, amplified, and sent to the DTE through the RX± pins.
15	28	TXO	Transmitter Output. This pin is connected directly (Thin Ethernet) or through an external isolating diode (Ethernet) to the coaxial cable.
16	1	CDS	Collision Detect Sense. Ground sense connection for the collision detection circuitry. This pin should be directly connected to the coaxial cable shield to prevent ground drops affecting the collision threshold voltage.
10	16 17	GND	Positive Supply Pin.
4 5 13	5 to 11 20 to 25	V_{EE}	Negative supply pins. These pins also serve as a low thermal resistance path for extracting heat from the die. They should, therefore, be connected to a large metal area on the PC board.

NOTE:
1. The IEEE 802.3 name for CD is CI; for RX is DI; for TX is DO.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage[1]	–12	V
V_{IN}	Voltage at any input[1]	0 to –12	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec.)	+300	°C
T_J	Recommended max junction temperature[2]	+130	°C
θ_{JA}	Thermal impedance (N and A packages)	60	°C/W

NOTE:
1. 100% measured in production.
2. The junction temperature is calculated from the following expression:

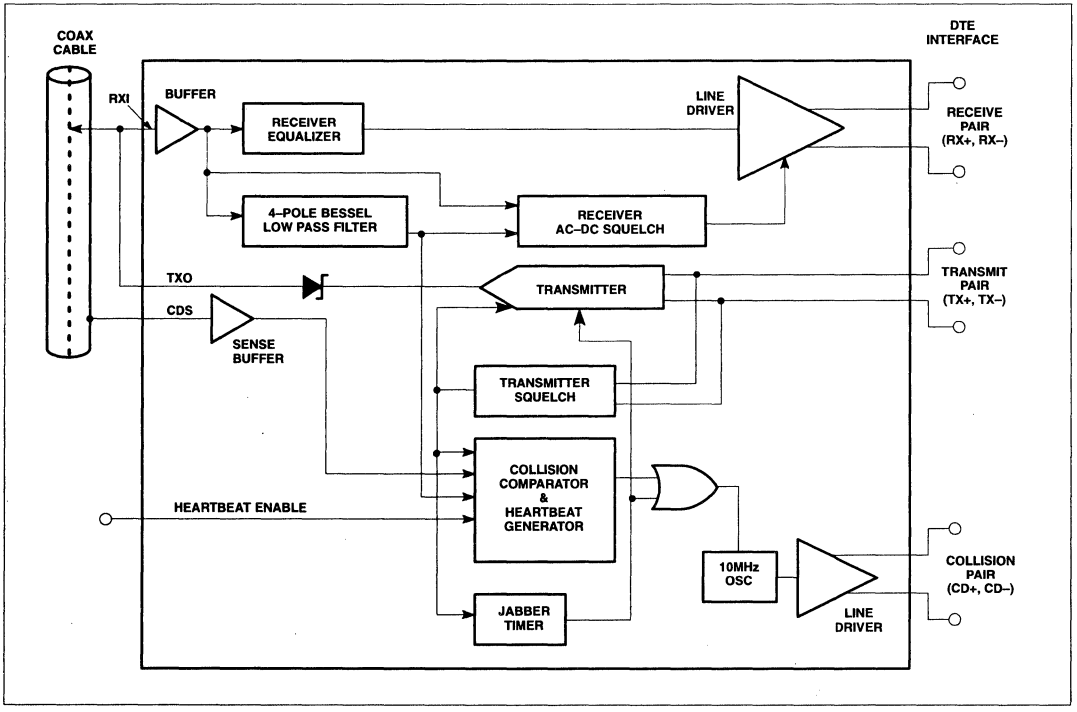
$$T_J = T_A + \theta_{JA}[V_{EE}(0.08 + n \times 0.05/100) + 8(V_{EE} - 2)/R]$$

where

T_A = Ambient temperature in °C.
θ_{JA} = Thermal resistance of package.
V_{EE} = Normal operating supply voltage in volts.
n = Percentage transmitter duty cycle.
R = Pull down resistors on the RX and CD pins in Ω.

The N package is specially designed to have a low θ_{JA} by directly connecting the four center Pins 4, 5, 12, and 13 to the die attachment area. These four pins then provide a conductive heat flow path from the die to the PCB where they should be soldered to a large area V_{EE} track. For the A package, Pins 5 to 11 and 19 to 25 should similarly be soldered to a large area V_{EE} and rack.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

V_{EE} = –9V ±5%; T_A = 0°C to +70°C unless otherwise specified[1,2]. No external isolation

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{POR}	Power–on reset voltage. Transmitter disabled for $\|V_{EE}\| < \|V_{POR}\|$			–6.5		V
I_{EE}	Supply current non–transmitting			–80	–130	mA
	Supply current transmitting			–125	–180	
I_{RXI}	Receive input bias current	V_{RXI} = 0V	–2		+25	µA
I_{CDS}	Cable sense input bias current	V_{CDS} = 0V		+2	+6	µA
V_{IH}	HBE input HIGH voltage		V_{EE} +1.4			V
V_{IL}	HBE input LOW voltage				V_{EE} +0.4	V
I_{IH}	HBE input HIGH current	V_{HBE} = 0V		250	500	µA
I_{IL}	HBE input LOW current	$V_{HBE} = V_{EE}$		–500	–1000	µA
I_{TDC}	Transmit output DC current level[3]		–37	–41	–45	mA
I_{TAC}	Transmit output AC current level[3]		±28		$\pm I_{TDC}$	mA
I_{TX10}	Transmit current	V_{TXO} = –10V	–250		+250	µA
V_{TCOM}	Transmitter output voltage compliance[4]				–3.7	V
V_{CD}	Collision threshold[5]	Measured by applying DC voltage at RXI	–1450	–1530	–1580	mV
V_{OD}	Differential output voltage – non idle at RX± and CD±[6]		±600		±1200	mV
V_{OB}	Differential output voltage imbalance – idle at RX± and CD±[7]				±40	mV
V_{OC}	Output common mode voltage at RX± and CD±		–1.5	–2	–2.5	V
V_{RS}	Receiver squelch threshold	V_{RXI} average DC	–130	–250	–370	mV
V_{TS}	Transmitter squelch threshold	$(V_{TX+} - V_{TX-})$ peak	–175	–225	–300	mV
R_{RXI}	Shunt resistance at RXI non–transmitting		100			kΩ
C_{RXI}	Input capacitance at RXI			2		pF
R_{TXO}	Shunt resistance at TXO transmitting			10		kΩ

NOTES:

1. Currents flowing into device pins are positive. All voltages are referenced to ground unless otherwise specified. For ease of interpretation, the parameter limit that appears in the MAX column is the largest value of the parameter, irrespective of sign. Similarly, the value in the MIN column is the smallest value of the parameter, irrespective of sign.
2. All typicals are for V_{EE} = –9V and T_A = 27°C.
3. I_{TDC} is measured as $(V_{MAX} + V_{MIN})/(2 \times 25)$ where V_{MAX} and V_{MIN} are the max and min voltages at TXO with a 25Ω load between TXO and GND. I_{TAC} is measured as $(V_{MAX} - V_{MIN})/(2 \times 25)$.
4. The TXO pin shall continue to sink at least I_{TDC} min when the idle (no signal) voltage on this pin is –3.7V.
5. Collision threshold for an AC signal is within 10% of V_{CD}.
6. Measured on secondary side of isolation transformer (see Connection Diagram, Figure 1). The transformer has a 1:1 turns ratio with an inductance between 30 and 100µH at 5MHz.
7. Measured as the voltage difference between the RX pins or the CD pins with the transformer removed.

TIMING CHARACTERISTICS

V_{EE} = –9V ±5%; T_A = 0 to 70°C, unless otherwise specified[1]. No external isolation diode on TXO.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{RON}	Receiver start up delay RXI to RX± (Figure 3) First received bit on RX±	V_{RXI} = –2V peak			5	bits
	First validly timed bit on RX±				t_{RON} +2	
t_{RD}	Receiver prop. delay RXI to RX±	V_{RXI} = –2V peak		35	50	ns
t_{RR}	Differential output rise time on RX± and CD±[2,3]			5		ns
t_{RF}	Differential output fall time on RX± and CD±[2,3]			5		ns
t_{OS}	Differential output settling time on RX± and CD± to V_{OB} = 40mV[2] (see Figure 5)			1		µs
t_{RJ}	Receiver and cable total jitter			±3		ns
t_{RHI}	Receiver high to idle time	Measured to +210mV	150		850	ns
t_{RM}	Rise and fall time matching on RX± and CD±	$t_{RF} - t_{RR}$		0.4		ns
t_{TST}	Transmitter start–up delay TX± to TXO (Figure 4) First transmitted bit on TXO	$V_{TX±}$ = –1V peak		1	2	bits
	First validly timed bit				t_{TST} + 2	
t_{TD}	Transmitter prop delay TX± to TXO (see Figure 4)	$V_{TX±}$ = 1V peak		35	50	ns
t_{TR}	Transmitter rise time 10% to 90% (see Figure 4)			25		ns
t_{TF}	Transmitter fall time 10% to 90% (see Figure 4)			25		ns
t_{TM}	$t_{TF} - t_{TR}$ mismatch			±2		ns
t_{TS}	Transmitter added skew[4]			±2		ns
t_{TON}	Transmitter turn on pulse width (see Figure 4)	$V_{TX±}$ = 1V peak	10		40	ns
t_{TOFF}	Transmitter turn off pulse width (see Figure 4)	$V_{TX±}$ = 1V peak	150	250	340	ns
t_{CON}	Collision turn on delay (see Figure 6)	0V to –2V step at RXI			13	bits
t_{COFF}	Collision turn off delay (see Figure 6)	–2V to 0V step at RXI			16	bits
t_{CHI}	Collision high to idle time (see Figure 6)	Measured to +210mV	150		850	ns
f_{CD}	Collision frequency (see Figure 6)		8.0	10	12.5	MHz
t_{CP}	Collision signal pulse width (see Figure 6)		35		70	ns
t_{HON}	Heartbeat turn on delay (see Figure 7)		0.6		1.6	µs
t_{HW}	Heartbeat test duration (see Figure 7)		0.5		1.5	µs
t_{JA}	Jabber activation delay measured from TX± to CD± (see Figure 8)		20		60	ms
t_{JR}	Jabber reset delay measured from TX± to CD± (see Figure 8)		250		750	ms

NOTES:
1. All typicals are for V_{EE} = –9V and T_A = 27°C.
2. Measured on secondary side of isolation transformer (see Figure 1, Connection Diagram). The transformer has a 1:1 turn ratio with an inductance between 30 and 100µH at 5MHz.
3. The rise and fall times are measured as the time required for the differential voltage to change from –225mV to +225mV, or +225mV to –225mV, respectively.
4. Difference in propagation delay between rising and falling edges at TXO.

FUNCTIONAL DESCRIPTION

The NE8392C contains four main functional blocks (see Block Diagram). These are:

a. The receiver which takes data from the coaxial cable and sends it to the DTE.

b. The transmitter which receives data from the DTE and sends it onto the coaxial cable.

c. The collision detection and heartbeat generation circuitry which indicates to the DTE any collision on the coaxial cable and tests for collision circuitry functionality at the end of every transmission.

d. The jabber timer which disables the transmitter in the event of a longer than legal length data packet.

Receiver Functions

The receiver consists of an input buffer, a cable equalizer, a 4-pole Bessel low pass filter, a squelch circuit and a differential line driver.

The buffer provides high input resistance and low input capacitance to minimize loading and reflections on the coaxial cable.

The equalizer is a high pass filter that compensates for the low pass effect of the coaxial cable and results in a flatband response over all signal frequencies to minimize signal distortion.

The 4-pole Bessel low pass filter extracts the average DC voltage level on the coaxial cable for use by the receiver squelch and collision detection circuits.

The receiver squelch circuit prevents noise on the coaxial cable from falsely triggering the receiver in the absence of a true signal. At the beginning of a packet, the receiver turns on when the DC level from the low pass filter is lower than the DC squelch threshold. For normal signal levels this will take less than 500ns, or 5 bits. However, at the end of a packet, a fast receiver turn off is needed to reject both dribble bits on the coaxial cable and spurious responses due to settling of the on-chip bandpass filter. This is accomplished by an AC timing circuit that disables the receiver if the signal level on the coaxial cable remains high for typically 250ns and only enables the receiver again after approximately 1µs. Figures 3 and 5 illustrate receiver timing.

The differential line driver provides typically ±900mV signals to the DTE with less than 7ns rise and fall times. When in idle state (no received signal) its outputs provide <20mV differential voltage offset to minimize DC standing current in the isolation transformer. The line driver outputs are emitter followers and, for Ethernet applications where they drive a 78Ω transmission line, require a 500Ω pull-down resistor to V_{EE}. For Thin Ethernet applications where the AUI cable is not used, the pull-down resistor can be increased to 1.5kΩ to save power consumption.

Transmitter Functions

The transmitter has differential inputs and an open collector current driver output. The differential input common mode voltage is established by the CTI and should not be altered by external circuitry. Controlled rise and fall times of 25ns (±5ns) minimize higher harmonic components in the transmitted spectrum, while matching of these rise and fall times to typically 2ns minimizes signal jitter. The drive current levels of the CTI are set by an on-chip bandgap voltage reference and an external 1% resistor. An on-chip isolation diode is provided to reduce the transmitter's coaxial cable load capacitance. For Thin Ethernet applications, no further external isolation diode is required, since the NE8392C meets the capacitive loading specifications. For Ethernet applications a further external diode should be added to reduce loading capacitance.

The transmitter squelch circuit ensures that the transmitter can only be enabled by negative-going differential signals of typically greater than 225mV in magnitude and 15ns in duration. The transmitter will be disabled at the end of a packet if there are no negative going signals of greater than 225mV for more than typically 250ns. Figure 4 illustrates transmitter timing.

Collision Functions

The collision detection scheme implemented in the NE8392C is receive mode detection, which detects a collision between any two stations on the network with certainty at all times, irrespective of whether or not the local DTE is producing one of the colliding signals. This is the only detection scheme allowed by the IEEE 802.3 standard for both repeater and non-repeater nodes.

The collision circuitry consists of the 4-pole Bessel low pass filter, a comparator, a precision voltage reference that sets up the collision threshold, a heartbeat generator, a 10MHz oscillator, and a differential line driver.

The collision comparator monitors the DC level at the output of the low pass filter and enables the line driver if it is more negative than the collision threshold. A collision condition is indicated to the DTE by a 10MHz oscillation signal at the CD outputs and typically occurs within 700ns of the onset of the collision. The collision signal begins with a negative-going pulse and ends with a continuous high-to-idle state longer than 170ns. Figure 6 illustrates collision timing.

At the end of every transmission, the heartbeat generator creates a pseudo collision to ensure that the collision circuitry is properly functioning. This pseudo collision consists of a 1µs burst of 10MHz oscillation at the line driver outputs approximately 1µs after the end of the transmission. The heartbeat function can be disabled externally by connecting the HBE (heartbeat enable) to V_{EE}. This allows the CTI to be used in repeater applications. Figure 7 illustrates heartbeat timing.

As with the receiver outputs, the collision outputs also require a pull down resistor to V_{EE} and maintain <20mV differential voltage offset in the idle state to minimize DC standing current in the isolation transformers.

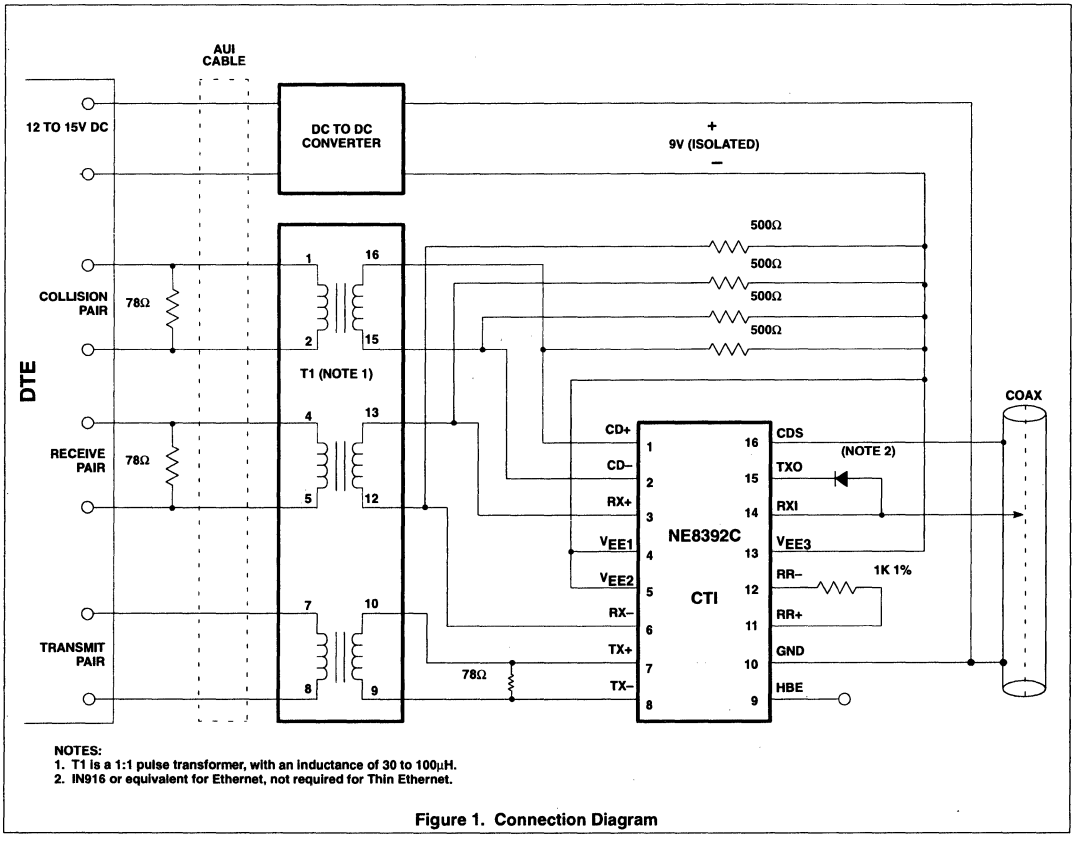
Jabber Functions

The jabber timer monitors the transmitter and inhibits transmission if it is active for longer than typically 30ms. The jabber circuit then enables the collision outputs for the remainder of the data packet and for typically 450ns (unjab time) after it has ended. At this point the transmitter becomes uninhibited. Figure 6 illustrates jabber timing.

Detection of Coaxial Cable Faults

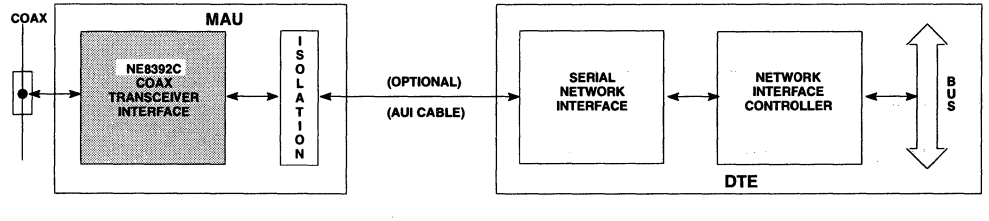
In the NE8392C there is no internal loopback path from the TX inputs to the RX outputs. This means that, when the local DTE is transmitting, the signal will only be present at the receiver outputs RX+ and RX– if it appears on the coaxial cable and is larger than the receiver squelch threshold V_{RS}. If a short circuit fault condition occurs at the cable connector to the CTI, then no signal will appear at the receiver outputs. An intelligent DTE can, therefore, detect this fault. If the fault is an open circuit, then a continuous collision signal will be sent to the DTE, provided the average DC voltage at the RXI pin is greater than the typical collision threshold of –1.53V.

If a short or open circuit occurs elsewhere on the coaxial cable, the resulting reflections can result in an impedance at the CTI of any value between a short circuit and 50Ω, depending on the distance of the CTI from the fault. The upper limit of 50Ω results from the fact that the coaxial cable is terminated in 50Ω at both ends. Faults on the cable itself are, therefore, not guaranteed to be detected by simply monitoring the RX and CD pins when in the transmit mode, and more sophisticated schemes may be necessary.



NOTES:
1. T1 is a 1:1 pulse transformer, with an inductance of 30 to 100μH.
2. IN916 or equivalent for Ethernet, not required for Thin Ethernet.

Figure 1. Connection Diagram



MAU = Medium Attachment Unit
AUI Cable = Attachment Unit Interface Cable (not used in Thin Ethernet applications)

Figure 2. Interface Diagram for Ethernet/Thin Ethernet Local Area Network

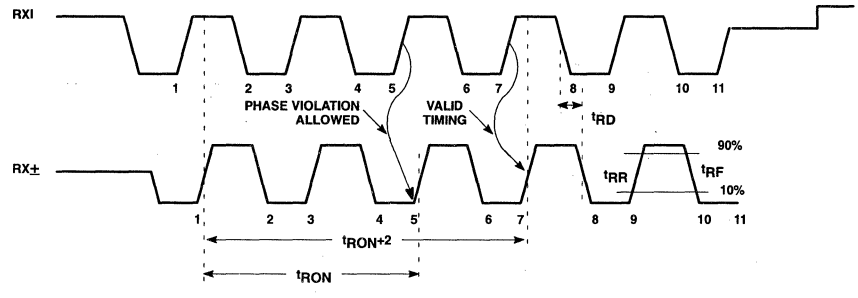


Figure 3. Receiver Timing

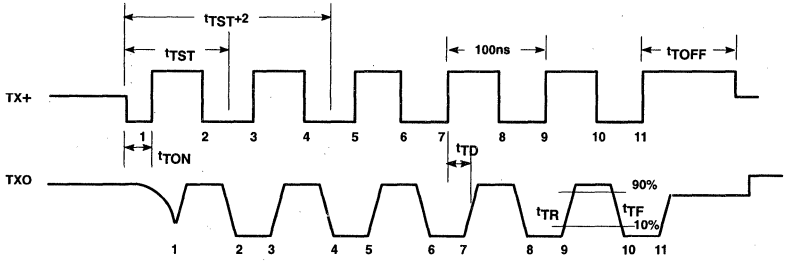


Figure 4. Transmitter Timing

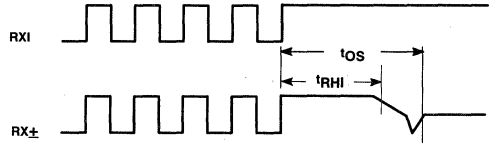


Figure 5. Receiver End–of–Packet Timing

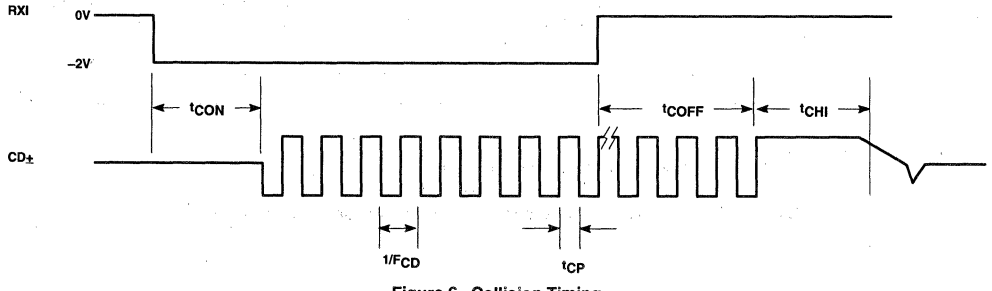


Figure 6. Collision Timing

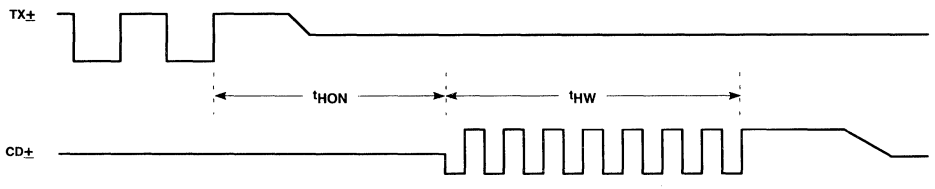


Figure 7. Heartbeat Timing

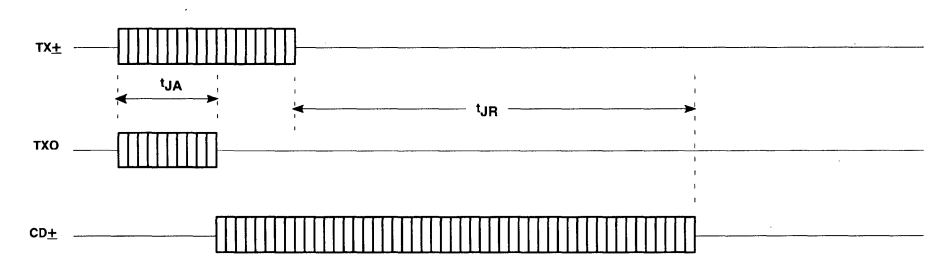


Figure 8. Jabber Timing

Coaxial transceiver interface for Ethernet/Thin Ethernet NE8392C-2

DESCRIPTION

The NE8392C-2 Coaxial Transceiver Interface (CTI) is a coaxial line driver/receiver for Ethernet (10base5) and Thin Ethernet (10base2) local area networks. The CTI is connected between the coaxial cable and the Data Terminal Equipment (DTE) and consists of a receiver, transmitter, collision detector, heartbeat generator and jabber timer (see Block Diagram). The transmitter output connects directly to a doubly terminated 50Ω cable, while the receiver output, collision detector output and transmitter input are connected to the DTE through isolation transformers. Isolation between the CTI and the DTE is an IEEE 802.3 requirement that can be met on signal lines by using a set of pulse transformers normally available in a standard 16-pin DIP. Power isolation for the CTI is achieved using DC-to-DC conversion through a power transformer (see Figure 1, Connection Diagram).

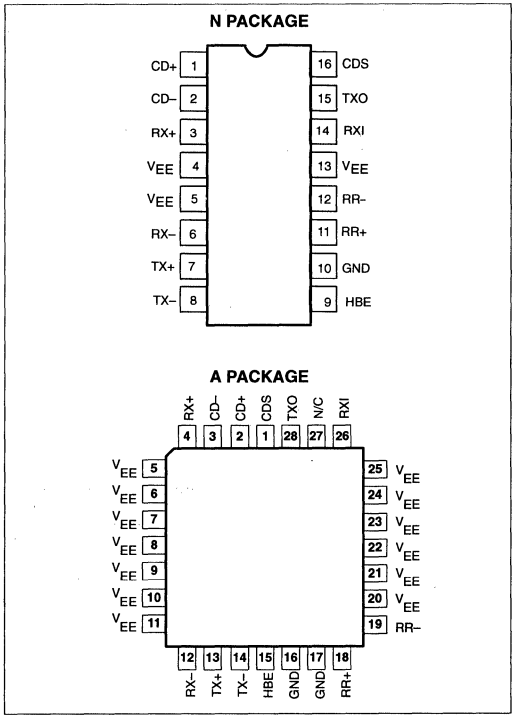
During transmission the jabber timer is initiated to disable the CTI transmitter in the event of a longer than legal length data packet. Collision detection circuitry monitors the signals on the coaxial cable to determine the presence of colliding packets and signals the DTE in the event of a collision. At the end of every transmission the heartbeat generator creates a pseudo collision for a short time to ensure that the collision circuitry is functioning correctly. The heartbeat function can be disabled for repeater applications.

The CTI is normally part of a three chip set that implements a complete Ethernet/ Thin Ethernet network interface for a DTE (see Figure 2, Interface Diagram). The other chips are a Serial Network Interface (SNI) and a Network Interface Controller (NIC). The SNI provides Manchester Encoding and Decoding while the NIC handles the media access protocol and buffer management tasks.

FEATURES

- Compatible with Ethernet II, IEEE 802.3 10base5 and 10base2, and ISO 8802/3 interface specifications
- Integrates all transceiver electronics except signal and power isolation
- Only one external resistor required for setting coaxial signaling current
- Jabber timer function integrated on chip
- Heartbeat generator can be externally disabled for operation as IEEE 802.3 compatible repeaters
- On-chip precision voltage reference for receive mode collision detection

PIN CONFIGURATION



- Open circuit disables CD when cable is open or unterminated
- Squelch circuitry on all signal inputs rejects noise
- Full ESD protection
- Standard 16-pin DIP with special lead frame minimizes the operating die temperature
- Power-on reset prevents glitches on coaxial cable during power up.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE8392C-2N	0406C
28-Pin Plastic Lead Chip Carrier (PLCC)	0 to +70°C	NE8392C-2A	0401F

PIN DESCRIPTIONS

PIN NO. N PKG	PIN NO. PLCC	SYMBOL	DESCRIPTION
1 2	2 3	CD+ CD–	Collision Outputs. Balanced differential line driver outputs which send a 10MHz oscillation signal to the DTE in the event of a collision, jabber interrupt or heartbeat test.
3 6	4 12	RX+ RX–	Receiver Outputs. Balanced differential line driver outputs which send the received signal to the DTE.
7 8	13 14	TX+ TX–	Transmitter Inputs. Balanced differential line receiver inputs which accept the transmission signal from the DTE and apply it to the coaxial cable at TXO.
9	15	HBE	Heartbeat Enable. The heartbeat function is disabled when this pin is connected to V_{EE} and enabled when connected to GND or left floating.
11 12	18 19	RR+ RR–	External Resistor. A 1kΩ (1%) resistor connected between these pins establishes the signaling current at TXO. RR– is internally connected to V_{EE}.
14	26	RXI	Receiver Input. This pin is connected directly to the coaxial cable. Received signals are equalized, amplified, and sent to the DTE through the RX± pins.
15	28	TXO	Transmitter Output. This pin is connected directly (Thin Ethernet) or through an external isolating diode (Ethernet) to the coaxial cable.
16	1	CDS	Collision Detect Sense. Ground sense connection for the collision detection circuitry. This pin should be directly connected to the coaxial cable shield to prevent ground drops affecting the collision threshold voltage.
10	16 17	GND	Positive Supply Pin.
4 5 13	5 to 11 20 to 25	V_{EE}	Negative supply pins. These pins also serve as a low thermal resistance path for extracting heat from the die. They should, therefore, be connected to a large metal area on the PC board.

NOTE:
1. The IEEE 802.3 name for CD is CI; for RX is DI; for TX is DO.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage[1]	–12	V
V_{IN}	Voltage at any input[1]	0 to –12	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec.)	+300	°C
T_J	Recommended max junction temperature[2]	+130	°C
θ_{JA}	Thermal impedance (N and A packages)	60	°C/W

NOTE:
1. 100% measured in production.
2. The junction temperature is calculated from the following expression:

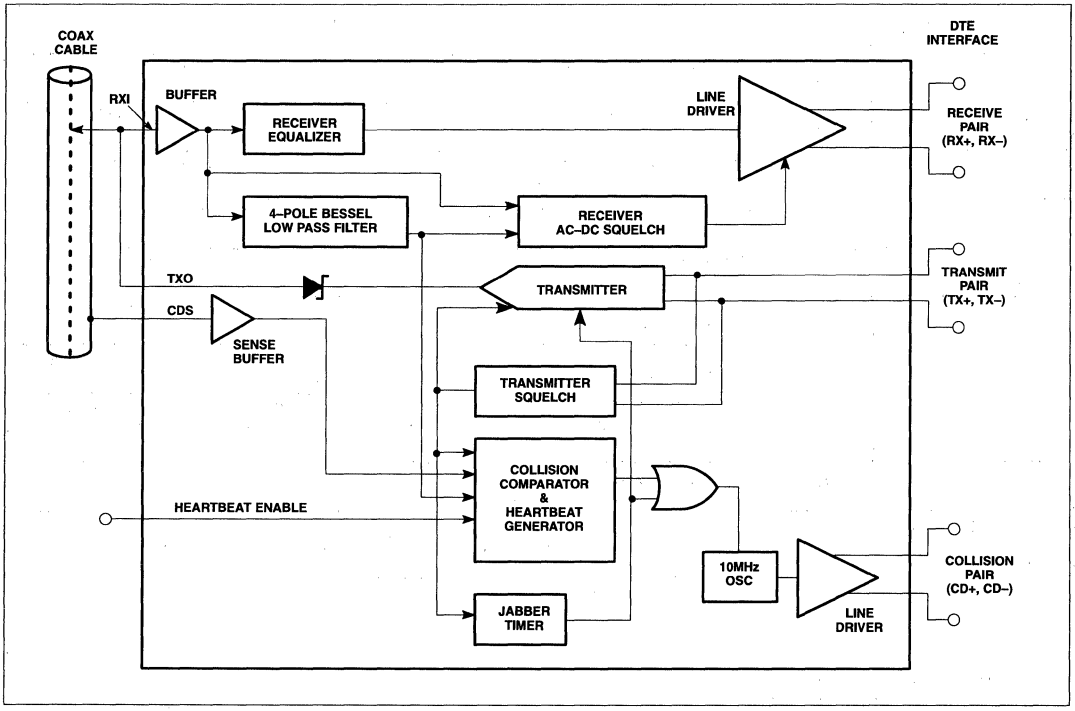
$$T_J = T_A + \theta_{JA}[V_{EE}(0.08 + n \times 0.05/100) + 8(V_{EE} - 2) / R]$$

where

T_A = Ambient temperature in °C.
θ_{JA} = Thermal resistance of package.
V_{EE} = Normal operating supply voltage in volts.
n = Percentage transmitter duty cycle.
R = Pull down resistors on the RX and CD pins in Ω.

The N package is specially designed to have a low θ_{JA} by directly connecting the four center Pins 4, 5, 12, and 13 to the die attachment area. These four pins then provide a conductive heat flow path from the die to the PCB where they should be soldered to a large area V_{EE} track. For the A package, Pins 5 to 11 and 19 to 25 should similarly be soldered to a large area V_{EE} and rack.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

V_{EE} = –9V ±5%; T_A = 0°C to +70°C unless otherwise specified[1,2]. No external isolation

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{POR}	Power–on reset voltage. Transmitter disabled for $\|V_{EE}\| < \|V_{POR}\|$			–6.5		V
I_{EE}	Supply current non–transmitting			–80	–130	mA
	Supply current transmitting			–125	–180	mA
I_{RXI}	Receive input bias current	V_{RXI} = 0V	–2		+25	µA
I_{CDS}	Cable sense input bias current	V_{CDS} = 0V		+2	+6	µA
V_{IH}	HBE input HIGH voltage		V_{EE} +1.4			V
V_{IL}	HBE input LOW voltage				V_{EE} +0.4	V
I_{IH}	HBE input HIGH current	V_{HBE} = 0V		250	500	µA
I_{IL}	HBE input LOW current	V_{HBE} = V_{EE}		–500	–1000	µA
I_{TDC}	Transmit output DC current level[3]		–37	–41	–45	mA
I_{TAC}	Transmit output AC current level[3]		±28		±I_{TDC}	mA
I_{TX10}	Transmit current	V_{TXO} = –10V	–250		+250	µA
V_{TCOM}	Transmitter output voltage compliance[4]				–3.7	V
V_{CD}	Collision threshold[5]	Measured by applying DC voltage at RXI	–1450	–1530	–1580	mV
V_{OD}	Differential output voltage – non idle at RX± and CD±[6]		±600		±1200	mV
V_{OB}	Differential output voltage imbalance – idle at RX± and CD±[7]				±40	mV
V_{OC}	Output common mode voltage at RX± and CD±		–1.5	–2	–2.5	V
V_{RS}	Receiver squelch threshold	V_{RXI} average DC	–130	–250	–370	mV
V_{TS}	Transmitter squelch threshold	(V_{TX+} – V_{TX-}) peak	–175	–225	–300	mV
R_{RXI}	Shunt resistance at RXI non–transmitting		100			kΩ
C_{RXI}	Input capacitance at RXI			2		pF
R_{TXO}	Shunt resistance at TXO transmitting			10		kΩ

NOTES:

1. Currents flowing into device pins are positive. All voltages are referenced to ground unless otherwise specified. For ease of interpretation, the parameter limit that appears in the MAX column is the largest value of the parameter, irrespective of sign. Similarly, the value in the MIN column is the smallest value of the parameter, irrespective of sign.
2. All typicals are for V_{EE} = –9V and T_A = 27°C.
3. I_{TDC} is measured as (V_{MAX} + V_{MIN})/(2 x 25) where V_{MAX} and V_{MIN} are the max and min voltages at TXO with a 25Ω load between TXO and GND. I_{TAC} is measured as (V_{MAX} – V_{MIN})/(2 x 25).
4. The TXO pin shall continue to sink at least I_{TDC} min when the idle (no signal) voltage on this pin is –3.7V.
5. Collision threshold for an AC signal is within 10% of V_{CD}.
6. Measured on secondary side of isolation transformer (see Connection Diagram, Figure 1). The transformer has a 1:1 turns ratio with an inductance between 30 and 100µH at 5MHz.
7. Measured as the voltage difference between the RX pins or the CD pins with the transformer removed.

TIMING CHARACTERISTICS

V_{EE} = –9V ±5%; T_A = 0 to 70°C, unless otherwise specified[1]. No external isolation diode on TXO.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{RON}	Receiver start up delay RXI to RX± (Figure 3) First received bit on RX±	V_{RXI} = –2V peak			5	bits
	First validly timed bit on RX±				t_{RON} +2	bits
t_{RD}	Receiver prop. delay RXI to RX±	V_{RXI} = –2V peak		35	50	ns
t_{RR}	Differential output rise time on RX± and CD±[2,3]			5		ns
t_{RF}	Differential output fall time on RX± and CD±[2,3]			5		ns
t_{OS}	Differential output settling time on RX± and CD± to V_{OB} = 40mV[2] (see Figure 5)			1		µs
t_{RJ}	Receiver and cable total jitter			±3		ns
t_{RHI}	Receiver high to idle time	Measured to +210mV	150		850	ns
t_{RM}	Rise and fall time matching on RX± and CD±	$t_{RF} - t_{RR}$		0.4		ns
t_{TST}	Transmitter start–up delay TX± to TXO (Figure 4)	$V_{TX±}$ = –1V peak				bits
	First transmitted bit on TXO			1	2	
	First validly timed bit				t_{TST} + 2	
t_{TD}	Transmitter prop delay TX± to TXO (see Figure 4)	$V_{TX±}$ = 1V peak		35	50	ns
t_{TR}	Transmitter rise time 10% to 90% (see Figure 4)			25		ns
t_{TF}	Transmitter fall time 10% to 90% (see Figure 4)			25		ns
t_{TM}	$t_{TF} - t_{TR}$ mismatch			±2		ns
t_{TS}	Transmitter added skew[4]			±2		ns
t_{TON}	Transmitter turn on pulse width (see Figure 4)	$V_{TX±}$ = 1V peak	10		40	ns
t_{TOFF}	Transmitter turn off pulse width (see Figure 4)	$V_{TX±}$ = 1V peak	150	250	340	ns
t_{CON}	Collision turn on delay (see Figure 6)	0V to –2V step at RXI			13	bits
t_{COFF}	Collision turn off delay (see Figure 6)	–2V to 0V step at RXI			16	bits
t_{CHI}	Collision high to idle time (see Figure 6)	Measured to +210mV	150		850	ns
f_{CD}	Collision frequency (see Figure 6)		8.0	10	12.5	MHz
t_{CP}	Collision signal pulse width (see Figure 6)		35		70	ns
t_{HON}	Heartbeat turn on delay (see Figure 7)		0.6		1.6	µs
t_{HW}	Heartbeat test duration (see Figure 7)		0.5		1.5	µs
t_{JA}	Jabber activation delay measured from TX± to CD± (see Figure 8)		20		60	ms
t_{JR}	Jabber reset delay measured from TX± to CD± (see Figure 8)		250		750	ms

NOTES:
1. All typicals are for V_{EE} = –9V and T_A = 27°C.
2. Measured on secondary side of isolation transformer (see Figure 1, Connection Diagram). The transformer has a 1:1 turn ratio with an inductance between 30 and 100µH at 5MHz.
3. The rise and fall times are measured as the time required for the differential voltage to change from –225mV to +225mV, or +225mV to –225mV, respectively.
4. Difference in propagation delay between rising and falling edges at TXO.

FUNCTIONAL DESCRIPTION

The NE8392C-2 contains four main functional blocks (see Block Diagram). These are:

a. The receiver which takes data from the coaxial cable and sends it to the DTE.

b. The transmitter which receives data from the DTE and sends it onto the coaxial cable.

c. The collision detection and heartbeat generation circuitry which indicates to the DTE any collision on the coaxial cable and tests for collision circuitry functionality at the end of every transmission.

d. The jabber timer which disables the transmitter in the event of a longer than legal length data packet.

Receiver Functions

The receiver consists of an input buffer, a cable equalizer, a 4-pole Bessel low pass filter, a squelch circuit and a differential line driver.

The buffer provides high input resistance and low input capacitance to minimize loading and reflections on the coaxial cable.

The equalizer is a high pass filter that compensates for the low pass effect of the coaxial cable and results in a flatband response over all signal frequencies to minimize signal distortion.

The 4-pole Bessel low pass filter extracts the average DC voltage level on the coaxial cable for use by the receiver squelch and collision detection circuits.

The receiver squelch circuit prevents noise on the coaxial cable from falsely triggering the receiver in the absence of a true signal. At the beginning of a packet, the receiver turns on when the DC level from the low pass filter is lower than the DC squelch threshold. For normal signal levels this will take less than 500ns, or 5 bits. However, at the end of a packet, a fast receiver turn off is needed to reject both dribble bits on the coaxial cable and spurious responses due to settling of the on-chip bandpass filter. This is accomplished by an AC timing circuit that disables the receiver if the signal level on the coaxial cable remains high for typically 250ns and only enables the receiver again after approximately 1µs. Figures 3 and 5 illustrate receiver timing.

The differential line driver provides typically ±900mV signals to the DTE with less than 7ns rise and fall times. When in idle state (no received signal) its outputs provide <20mV differential voltage offset to minimize DC standing current in the isolation transformer. The line driver outputs are emitter followers and, for Ethernet applications where they drive a 78Ω transmission line, require a 500Ω pull-down resistor to V_{EE}. For Thin Ethernet applications where the AUI cable is not used, the pull-down resistor can be increased to 1.5kΩ to save power consumption.

Transmitter Functions

The transmitter has differential inputs and an open collector current driver output. The differential input common mode voltage is established by the CTI and should not be altered by external circuitry. Controlled rise and fall times of 25ns (±5ns) minimize higher harmonic components in the transmitted spectrum, while matching of these rise and fall times to typically 2ns minimizes signal jitter. The drive current levels of the CTI are set by an on-chip bandgap voltage reference and an external 1% resistor. An on-chip isolation diode is provided to reduce the transmitter's coaxial cable load capacitance. For Thin Ethernet applications, no further external isolation diode is required, since the NE8392C-2 meets the capacitive loading specifications. For Ethernet applications a further external diode should be added to reduce loading capacitance.

The transmitter squelch circuit ensures that the transmitter can only be enabled by negative-going differential signals of typically greater than 225mV in magnitude and 15ns in duration. The transmitter will be disabled at the end of a packet if there are no negative going signals of greater than 225mV for more than typically 250ns. Figure 4 illustrates transmitter timing.

Collision Functions

The collision detection scheme implemented in the NE8392C-2 is receive mode detection, which detects a collision between any two stations on the network with certainty at all times, irrespective of whether or not the local DTE is producing one of the colliding signals. This is the only detection scheme allowed by the IEEE 802.3 standard for both repeater and non-repeater nodes.

The collision circuitry consists of the 4-pole Bessel low pass filter, two comparators, a precision voltage reference that sets up the collision threshold, a heartbeat generator, a 10MHz oscillator, and a differential line driver.

The collision comparator monitors the DC level at the output of the low pass filter and enables the line driver if it is more negative than the collision threshold. A collision condition is indicated to the DTE by a 10MHz oscillation signal at the CD outputs and typically occurs within 700ns of the onset of the collision. The collision signal begins with a negative-going pulse and ends with a continuous high-to-idle state longer than 170ns. Figure 6 illustrates collision timing.

The second comparator monitors to detect an un-terminated or open circuit condition on the coaxial cable. When detected, the CD output is disabled, even though the average DC level has fallen below the collision threshold.

At the end of every transmission, the heartbeat generator creates a pseudo collision to ensure that the collision circuitry is properly functioning. This pseudo collision consists of a 1µs burst of 10MHz oscillation at the line driver outputs approximately 1µs after the end of the transmission. The heartbeat function can be disabled externally by connecting the HBE (heartbeat enable) to V_{EE}. This allows the CTI to be used in repeater applications. Figure 7 illustrates heartbeat timing.

As with the receiver outputs, the collision outputs also require a pull down resistor to V_{EE} and maintain <20mV differential voltage offset in the idle state to minimize DC standing current in the isolation transformers.

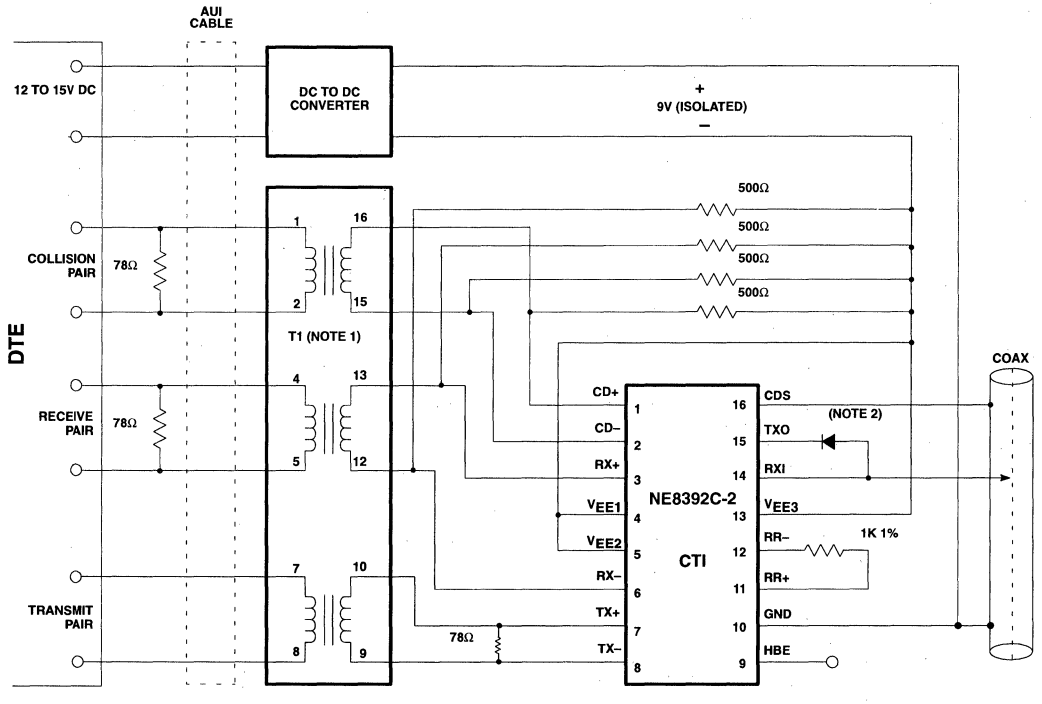
Jabber Functions

The jabber timer monitors the transmitter and inhibits transmission if it is active for longer than typically 30ms. The jabber circuit then enables the collision outputs for the remainder of the data packet and for typically 450ns (unjab time) after it has ended. At this point the transmitter becomes uninhibited. Figure 6 illustrates jabber timing.

Detection of Coaxial Cable Faults

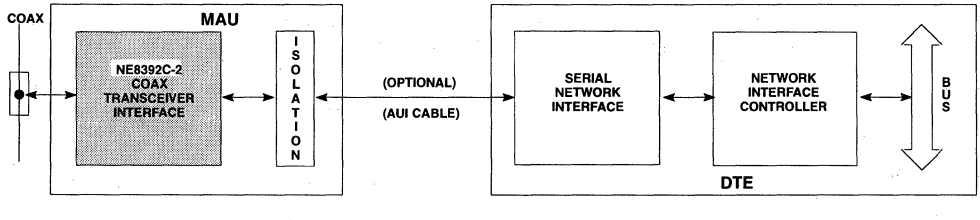
In the NE8392C-2 there is no internal loopback path from the TX inputs to the RX outputs. This means that, when the local DTE is transmitting, the signal will only be present at the receiver outputs RX+ and RX– if it appears on the coaxial cable and is larger than the receiver squelch threshold V_{RS}. If a short circuit fault condition occurs at the cable connector to the CTI, then no signal will appear at the receiver outputs. An intelligent DTE can, therefore, detect this fault. If the fault is an open circuit, then a continuous collision signal will be sent to the DTE, provided the average DC voltage at the RXI pin is greater than the typical collision threshold of –1.53V.

If a short or open circuit occurs elsewhere on the coaxial cable, the resulting reflections can result in an impedance at the CTI of any value between a short circuit and 50Ω, depending on the distance of the CTI from the fault. The upper limit of 50Ω results from the fact that the coaxial cable is terminated in 50Ω at both ends. Faults on the cable itself are, therefore, not guaranteed to be detected by simply monitoring the RX and CD pins when in the transmit mode, and more sophisticated schemes may be necessary.



NOTES:
1. T1 is a 1:1 pulse transformer, with an inductance of 30 to 100μH.
2. IN916 or equivalent for Ethernet, not required for Thin Ethernet.

Figure 1. Connection Diagram



MAU = Medium Attachment Unit
AUI Cable = Attachment Unit Interface Cable (not used in Thin Ethernet applications)

Figure 2. Interface Diagram for Ethernet/Thin Ethernet Local Area Network

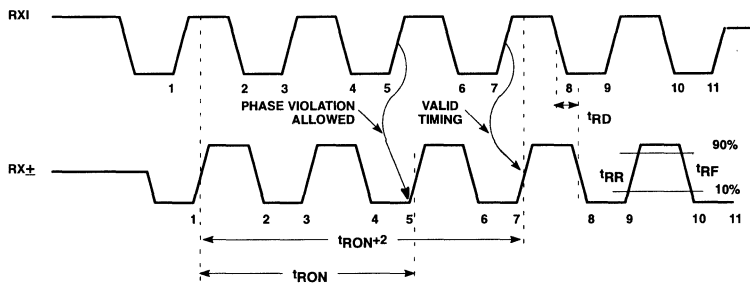


Figure 3. Receiver Timing

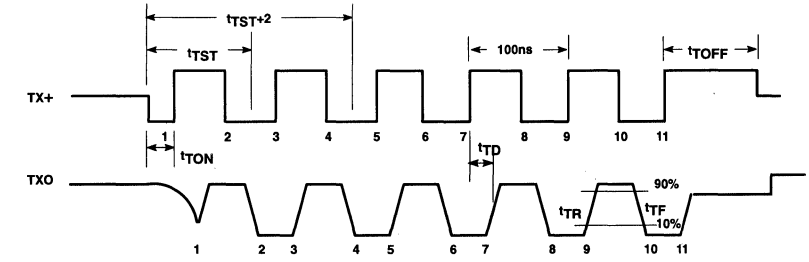


Figure 4. Transmitter Timing

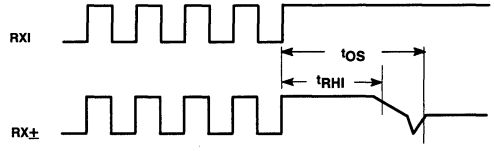


Figure 5. Receiver End–of–Packet Timing

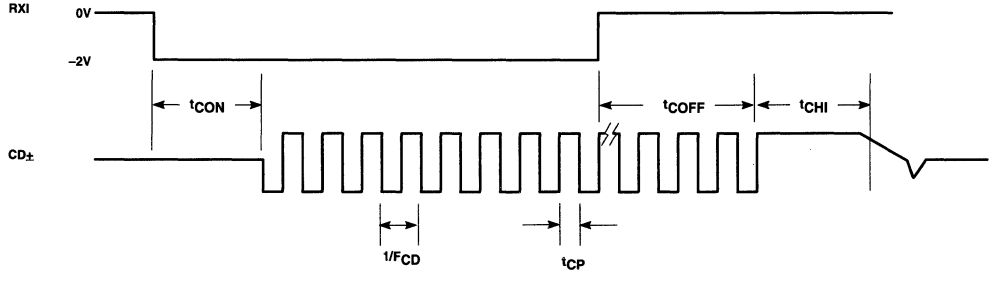


Figure 6. Collision Timing

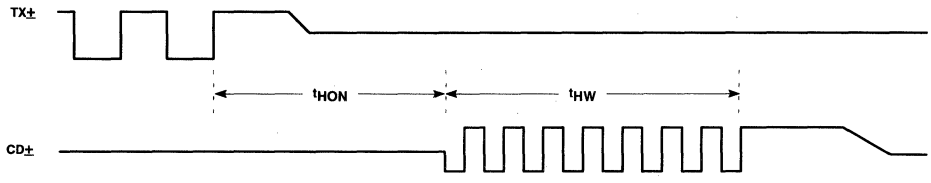


Figure 7. Heartbeat Timing

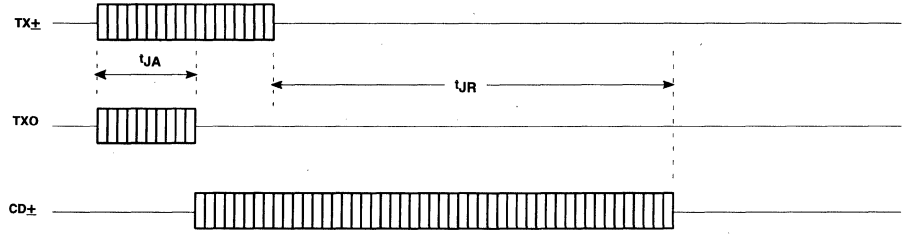


Figure 8. Jabber Timing

Twisted-pair transceiver interface — NE86C92

DESCRIPTION

The NE86C92 is a twisted-pair transceiver that implements the IEEE 802.3 10BASE-T Ethernet specification. The circuit provides the connection between the Manchester encoder/decoder and the twisted-pair cable and includes a receiver, transmitter, collision detector, heartbeat generator, jabber timer, link integrity monitor, and control circuits and drivers for five LED status indicators.

The NE86C92 includes receive polarity detection with automatic polarity correction, smart squelch on all signal inputs for improved noise immunity, and a highly reliable crystal oscillator to set pre-distortion timing and the collision signal frequency.

The NE86C92 also allows for automatic selection between AUI and twisted-pair (RJ-45) connections; thus eliminating the need for end-users to remove the interface board and move jumpers to switch between connections. An application note is available which describes implementation of this feature.

The twisted-pair outputs and inputs connect to the twisted-pair cable through transmit and receive filters while the receiver output, collision detector output and transmitter input are connected to the Manchester encoder/decoder through pulse transformers. This interface to the encoder/decoder is, therefore, directly compatible with current 10Base2/10Base5 connections and allows easy expansion of existing interface cards for twisted-pair wiring.

During transmission the jabber timer is initiated to disable the NE86C92 in the event of a longer than legal length data packet. Collision detection circuitry monitors both the transmit path and the receiver input to determine the presence of colliding packets and signals the Manchester encoder/decoder in the event of a collision. At the end of every transmission the heartbeat generator creates a pseudo collision for a short time to ensure that the collision circuity is functioning correctly. The link integrity monitor emits pulses onto the twisted-pair cable and expects to receive pulses from the twisted-pair cable at regular intervals. If no pulses or packets are received, a link failure has occurred; this is indicated by the RLED status indicator. Both heartbeat and link integrity monitor functions can be disabled.

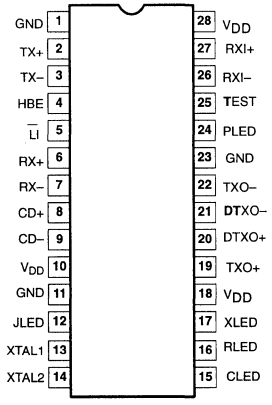
The NE86C92 is normally part of a three chip set for implementing a complete twisted-pair Ethernet network interface. The other chips are the Manchester encoder/decoder, such as the NE502A, and a Network Interface Controller, such as the NE86950.

APPLICATIONS

- 10BASE-T network interfaces for computers and workstations
- External 10BASE-T transceiver units

PIN CONFIGURATION

D and N Packages



FEATURES

- Compatible with IEEE 802.3 10BASE-T specifications
- Integrates all transceiver functions, with selectable heartbeat and link test generators
- Twisted-pair polarity detection and automatic correction
- Smart squelch on all data inputs
- Internal transmitter pre-distortion generator
- Supports automatic selection between AUI and RJ-45 connections
- Five LED status signals with on-chip drivers for transmit, receive and link integrity, collision, jabber status and twisted pair polarity reversal
- Advanced CMOS process uses single 5V supply
- Extremely low power operation: 24mA typical idle current

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
28-Pin Plastic Dual In-Line Package (DIP) (.600 in. wide)	0 to 70°C	NE86C92N	0413B
28-Pin Plastic Small Outline Large (SOL) Package	0 to 70°C	NE86C92D	0006C

PIN DESCRIPTIONS

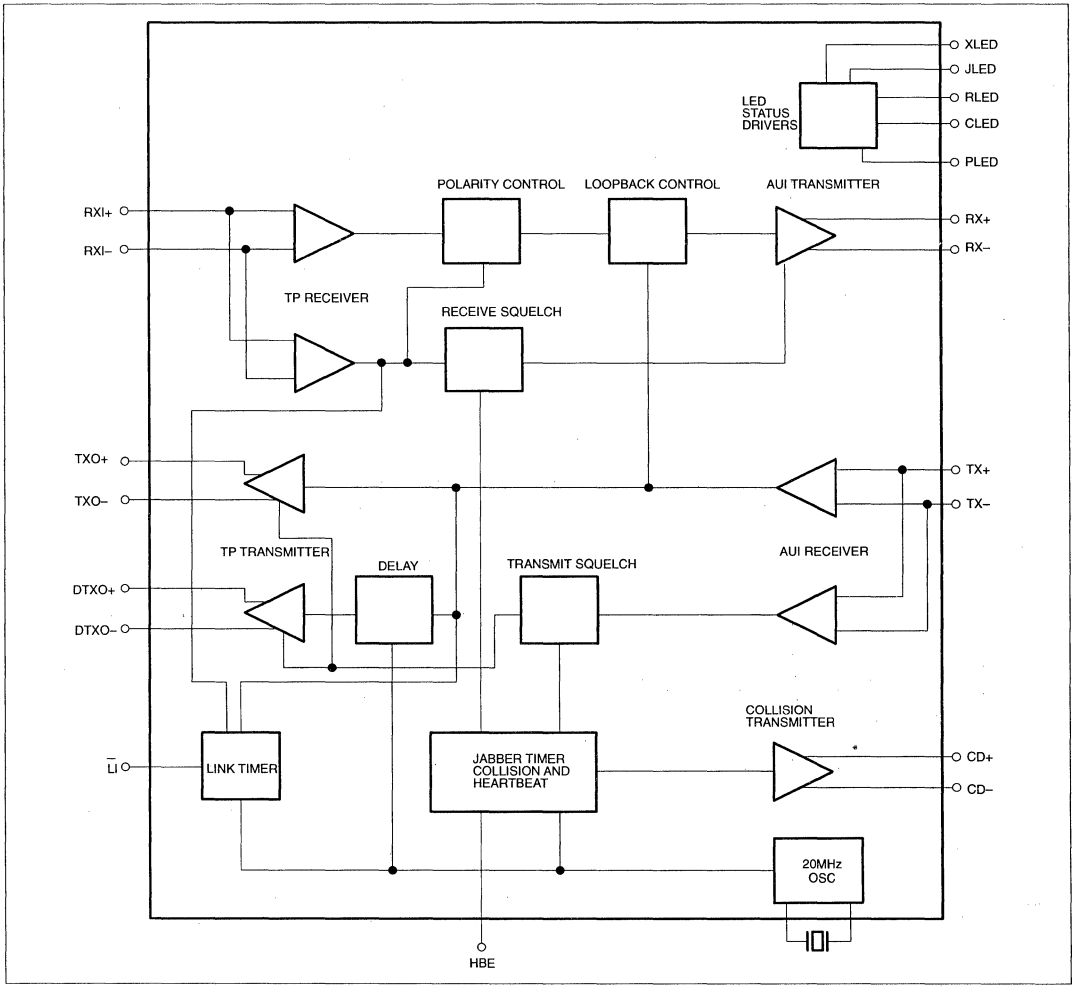
Pin No.	Symbol	Description
1	GND	Ground
2, 3	TX+, TX–	Transmitter inputs. Balanced differential line receiver. Inputs which accept the transmission signal from the Manchester encoder/decoder and apply it to the Twisted-Pair cable at TXO+, DTXO+, TXO– and DTXO-.
4	HBE	Heartbeat Enable. The heartbeat function is disabled when this pin is connected to GND and enabled when connected to V_{DD} or left floating.
5	$\overline{LI}$	Link Integrity. The link integrity function is disabled when this pin is connected to V_{DD} or left floating and enabled when connected to GND.
6, 7	RX+, RX-	Receive Outputs. Balanced differential line driver outputs which send the received signal to the Manchester encoder/decoder.
8, 9	CD+, CD-	Collision Outputs. Balanced differential line driver outputs which send a 10MHz oscillation signal to the Manchester encoder/decoder in the event of a collision, jabber interrupt or heart beat test.
10	V_{DD}	Positive power supply
11	GND	Ground.
12	JLED	Jabber Indicator. Indicates that the jabber timer has timed out and the twisted-pair drivers are disabled.
13	XTAL1	Crystal pin. One terminal of 20MHz crystal; or 20MHz external clock input.
14	XTAL2	Crystal Pin. One terminal of 20MHz crystal.
15	CLED	Collision Indicator. Indicates that a collision has been detected.
16	RLED	Receive Indicator. Indicates a packet is being received from the twisted-pair cable.
17	XLED	Transmit Indicator. Indicates a packet is being transmitted onto the twisted-pair cable.
18	V_{DD}	Positive power supply
19 20 21 22	TXO+, DTXO+, DTXO-, TXO-	Twisted-Pair drivers. These four outputs provide twisted-pair drive with pre-distortion. TXO+ and TXO- are balanced differential outputs that follow the signal at the TX+ and TX- inputs. DTXO+ and DTXO- are delayed and inverted with respect to TXO– and TXO+. Combining these outputs through an external resistor network provides the necessary pre-distortion to overcome the twisted-pair cable attenuation characteristics.
23	GND	Ground.
24	PLED	Polarity reversal indicator. Indicates polarity reversal of the twisted-pair receiver wires. A no-connect at this pin enables auto-correction although there is no LED indication. Connecting to GND disables auto-correction.
25	TEST	Test. No Connection, or connect to ground.
26, 27	RXI-, RXI+	Receiver inputs. These inputs receive the data from the twisted-pair cable and pass it on to RX+ and RX-.
28	V_{DD}	Positive power supply.

NOTE: The IEEE 802.3 designation for CD is CI, for RX is DI, for TX is DO, for RXI is RD and for TXO and DTXO combined is TD.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage with respect to GND	-0.5 to +6.5	V
V_{IN}	Voltage at any input to GND	-0.5 to V_{DD} +0.5	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec)	+300	°C
T_J	Recommended max junction temperature	+125	°C
θ_{JA}	Thermal impedance N package D package	55 70	°C/W °C/W

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

V_{DD} = +5V ±10%, T_A = 0°C to 70°C; unless otherwise stated. Typical values measured at V_{DD} = +5V, T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Power supply threshold and currents						
V_{DDEN}	Enable V_{DD} threshold			3.4		V
V_{DDDIS}	Disable V_{DD} threshold			1.2		V
I_{DDI}	Supply current (no traffic)			20		mA
I_{DDT}	Supply current transmitting	TXO± RXI± active, 90% duty cycle		65	100	mA
Digital input voltage (HBE, $\overline{LI}$)						
V_{IL}	Input LOW voltage		GND - 0.3		0.8	V
V_{IH}	Input HIGH voltage		2.0		V_{DD} + 0.3	V
Digital input current (HBE, $\overline{LI}$, PLED)						
I_{IN}	Input current	GND - 0.3 < V_{IN} < V_{DD} + 0.3	-500		0	µA
LED driver output voltage						
V_{OL}	Output LOW voltage	I_{OUT} = 10mA			0.4	V
LED driver leakage current						
I_{OL}	Output leakage current, output inactive	GND < V_{OUT} < V_{DD} + 0.3			+10	µA
I_{OLPLED}	PLED output leakage current, inactive	GND < V_{OUT} < V_{DD} + 0.3			+250	µA
Transmitter, receiver and collision indicator						
V_{OC}	TX±, RXI± open circuit input voltage		1.5		3.5	V
I_{ITR}	TX+, TX-, RXI+, RXI- input current	GND - 0.3 < V_{IN} < V_{DD} + 0.3	-500		+500	µA
R_{TX}	TX± differential input resistance		16			kΩ
V_{TS}	Transmitter squelch threshold		-150	-200	-300	mV
V_{OH}	Output HIGH voltage TXO±, DTXO±	Load = 500Ω to GND	V_{DD} – 0.1			V
V_{OL}	Output LOW voltage TXO±, DTXO±	Load = 500Ω to V_{DD}			0.1	V
R_{RXI}	RXI± differential input resistance		20			kΩ
V_{RS}	Receive squelch threshold		±300	±400	±585	mV
V_{OD}	Differential output voltage non-idle at RX±, CD±	R_L = 78Ω	±600	±825	±1200	mV
V_{OB}	Differential output voltage imbalance at RX±, CD±, idle and non-idle	R_L = 78Ω	-40		+40	mV
V_{TPOD}	Peak differential output voltage	R_L = 100, R_1 = 48, R_2 = 464		2.8		V
V_{TOB}	Differential output voltage imbalance at TXO±, DTXO± idle and non-idle		-40		+40	mV
R_{TS}	TXO±, DTXO± output resistance	I = 25mA		7	10	Ω

TIMING CHARACTERISTICS

V_{DD} = +5V ±10%, T_A = 0°C to 70°C; unless otherwise stated. Typical values measured at V_{DD} = +5V, T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Receiver and collision signal						
t_{RST}	Receive start-up delay	$V_{RXI\pm}$ = 1V peak		250	500	ns
t_{RBL}	Bits lost at receiver start-up	$V_{RXI\pm}$ = 1V peak		2	4	bits
	First validly timed bit on RX±				t_{RBL} + 2	bits
t_{RD}	Receiver propagation delay RXI± to RX±	Include receive filter		40	100	ns
t_{ROFF}	Receiver turn-off pulse width		150		230	ns
t_{RHI}	Receiver high-to-idle time	Measured to ±210mV	200		400	ns
t_{CHI}	Collision high-to-idle time	Measured to ±210mV	400		500	ns
t_{RR}	Differential output rise time on RX±, CD±				5	ns
t_{RF}	Differential output fall time on RX±, CD±				5	ns
t_{RM}	Rise and fall time matching on RX±, CD±	t_{RF} - t_{RR}	-2		2	ns
t_{RJ}	Receiver added jitter RXI± to RX±	$V_{RXI\pm}$ = 1V peak	-1.5		+1.5	ns
t_{CMJ}	Receiver added common-mode jitter RXI± to RX±	$V_{RXI\pm}$ = 2.5V at receive filter input	-2.5		+2.5	ns
Transmitter						
t_{TST}	Transmit start-up delay	$V_{TX\pm}$ = 1V peak		280	400	ns
t_{TBL}	Bits lost at transmitter start-up	$V_{TX\pm}$ = 1V peak			2	bits
	First validly timed bit				t_{TBL+2}	bits
t_{TD}	Transmit propagation delay	$V_{TX\pm}$ = 1V peak (include transmitter filter)		50	100	ns
t_{TS}	Transmitter added jitter	Load = 100Ω and cable model	-3.5		+3.5	ns
t_{TOFF}	Transmitter turn off pulse width	$V_{TX\pm}$ = 1V	150		200	ns
t_{THI}	Transmitter high to idle time		250		450	ns
t_{PDPW}	Pre-distortion pulse width		45		55	ns
Link integrity						
t_{LTSD}	Transmit silence duration		8	16	24	ms
t_{LTPW}	Link test pulse width	With 100Ω load/measure at 585mV amplitude point	80		120	ns
t_{ICLTP}	Time period for ignored consecutive link pulses	$V_{RXI\pm}$ = 1V peak	2	5	7	ms
t_{CCLTP}	Time period for counted consecutive link pulses	$V_{RXI\pm}$ = 1V peak	25	48	150	ms
t_{LLD}	Link loss detect time		50	110	150	ms
Collision and jabber						
f_{CD}	Collision frequency		8.5	10.0	11.5	MHz
t_{CP}	Collision signal pulse width		40	50	60	ns
t_{CON}	Collision turn-on delay				9	bits
t_{COFF}	Collision turn-off delay				9	bits
t_{HON}	Heartbeat turn-on delay		0.6	1.1	1.6	µs
t_{HW}	Heartbeat test duration		0.5	1.0	1.5	µs
t_{JA}	Jabber activation delay		20	50	150	ms
t_{JR}	Jabber reset delay		250	450	750	ms

TIMING CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Loopback						
t_{LBON}	Loopback start-up delay				9	bits
t_{LBE}	Loopback enable time RXI± to RX±				9	bits
t_{LBD}	Loopback disable time RXI± to RX±				9	bits
t_{LBPD}	Loopback propagation delay TXI± to RX±				200	ns
LEDs						
t_{LED}	Turn-on or turn-off delay of LEDs				10	µs
$t_{XLEDOFF}$	XLED maximum off time		95		135	ms
t_{XLEDON}	XLED minimum on time		5		10	ms
$t_{RLEDOFF}$	RLED maximum off time	$\overline{LT}$ = high (V_{DD})	95		135	ms
t_{RLEDON}	RLED minimum on time		5		10	ms
t_{RLEDLL}	RLED turn-off time for link loss[1]			t_{LL}		ms
t_{RLEDLE}	RLED on time after link re-established	$\overline{LT}$ = low (GND)	0.5		1.5	sec
t_{CLEDON}	CLED minimum on time		10	11.5	14	ms
t_{JLEDON}	JLED on time[2]	ON while jabber is active		t_{JON}		ms
$t_{JLEDOFF}$	JLED off time[3]	OFF while jabber is inactive		t_{JOFF}		ms

NOTES:
1. t_{LL} = duration of link loss
2. t_{JON} = jabber active time.
3. t_{JOFF} = jabber inactive time

FUNCTIONAL DESCRIPTION

The NE86C92 contains eight main functional blocks (see Block Diagram). These are:

1. The receiver which takes data from the twisted-pair cable and sends it to the Manchester encoder/decoder.
2. The receive polarity detector and correction control which detects the polarity of the received signal and internally corrects the polarity of a reversed polarity connection.
3. The transmitter which receives data from the Manchester encoder/decoder and sends it onto the twisted-pair cable.
4. The collision detection and heartbeat generation circuitry which indicates to the Manchester encoder/decoder any collision resulting from a coincident transmit and receive activity and tests for collision circuitry functionality at the end of every transmission.
5. The jabber timer which disables the transmitter in the event of a longer than legal length data packet.
6. The link integrity monitor which periodically tests the integrity of the twisted-pair link and indicates if a link failure occurs.
7. A crystal controlled oscillator which provides all on-chip timing functions for control, pre-distortion and the 10MHz collision signal.
8. LED control circuitry and drivers for indicating the transmit, receive and link integrity, collision, jabber and Twisted-Pair polarity status of the NE86C92.

Receiver Functions

The receiver section consists of a differential twisted-pair receiver, a squelch circuit and a differential line driver for the AUI cable.

The twisted-pair receiver is connected to the output of a bandpass filter whose input is transformer coupled to the twisted- pair cable. The receiver has a high differential input impedance to allow accurate external resistors to be used for matching to the bandpass filter. The common mode voltage of the input buffer is set internally on the chip.

The receiver squelch circuit prevents noise on the twisted-pair cable from falsely triggering the receiver in the absence of true data. The twisted-pair receiver will be activated if the differential signal at the RXI pins exceeds typically ±400mV and has a low-high-low sequence with both the positive and negative pulse widths exceeding 50ns. Once activated the squelch threshold reduces to ±200mV to ensure reception. The fifth bit of the Manchester code is always received. The receiver is de-activated by a continuous high of between 150ns and 230ns. The receiver is then inhibited for a further 500ns at the end of a packet in order to reject dribble bits or the twisted-pair cable.

The data packet passed on to the Manchester encoder/decoder will typically have a high-to-idle time of 300ns.

The differential line driver provides typically ±825mV signals into a 78Ω transmission line connecting the transceiver to the Manchester encoder/decoder with rise and fall times less than 5ns. When in the idle state (no received or transmitted signal) both outputs are pulled to GND and provide < 40mV differential voltage offset to minimize DC standing current in the transformer.

Polarity Control Functions

The polarity control circuitry consists of a polarity detector and a polarity correction circuit. The polarity detector is activated following

a link failure or power-on reset. It then waits for the detection of four consecutive link test pulses of the same polarity, or the reception of a data frame to determine the correct polarity. Having determined the correct polarity, the correction circuit provides the correct data polarity to the receiver and the link integrity pulse detector.

The PLED pin provides a buffered output indication of the status of the polarity correction circuit. This output may be used to drive an LED directly (through an external current limiting resistor to V_{DD}) for visual indication of polarity.

The polarity detection and correction circuit may be externally DISABLED by connecting PLED (Pin 24) to ground.

Transmitter Functions

The transmitter consists of a differential receiver, a squelch circuit and a differential twisted-pair cable driver with pre-distortion. When data is being transmitted, and there is no collision or link integrity failure, the transmitted data is looped back to the receiver output ports RX+ and RX-.

The common mode voltage of the differential input buffer is set internally with a differential input resistance of typically 40 kΩ.

The transmitter squelch circuit prevents false triggering of the transmitter from noise on the AUI cable. The transmitter will be activated if the differential signal at the TX± pins exceeds typically ±200mV and has a high-low sequence with both the positive and negative pulse widths exceeding 50ns. The third bit of the Manchester data is always transmitted. The transmitter is de-activated by a continuous high of between 150ns and 200ns.

Pre-distortion of the transmitted waveform is included to reduce the bit dependent jitter at the end of a twisted-pair cable caused by it's inherent low pass characteristics. The pre-distortion is achieved by using two pairs of differential twisted-pair drivers. One pair of drivers produces a signal delayed by 50ns compared to the other. By combining the four driver outputs through an external resistor network, the signal on the twisted-pair is pre-emphasized for the first 50ns following a voltage transition. The pre-emphasis can be changed by selection of different external resistance values.

Collision Functions

The collision circuitry consists of logic for detecting simultaneous transmission and reception, a heartbeat generator, a 10MHz signal source and a differential line driver.

The collision detection scheme implemented in the NE86C92 is transmit mode detection which detects a collision if both the transmitter and receiver are active at the same time. A collision condition is indicated to the Manchester encoder/decoder by a 10MHz signal at the CD outputs of the differential line driver and occurs within 900ns of the onset of a collision. The collision signal begins with a negative going pulse and ends with a continuous high-to-idle state of typically 450ns.

When a collision occurs the internal loopback is disabled and the signal received at the RXI inputs is passed to the RX outputs. At the end of a collision the loopback is enabled again.

At the end of every transmission the heartbeat generator creates a pseudo collision to ensure that the collision circuitry is properly functioning. The pseudo collision consists of a 1μs burst of 10MHz signal at the CD outputs approximately 1us after the end of the transmission. The heartbeat function can be disabled externally by connecting the HBE (heartbeat enable) to GND. This allows the NE86C92 to be used in hub or repeater applications.

As with the receiver outputs the collision outputs CD+ and CD- are pulled low in the idle state and maintain < 40mV offset to minimize DC standing current in the transformer.

Jabber Functions

The jabber timer monitors the transmitter and inhibits transmission if it is active for longer than typically 50ms. The jabber circuit then enables the collision outputs for the remainder of the data frame and for typically 450ms (unjab time) after it has ended. At this point the transmitter becomes uninhibited.

Link Integrity Functions

This circuit monitors the integrity of the twisted-pair cable connected to the RXI inputs. In the event of a fault, the transmit, loopback and receive functions of the NE86C92 are disabled and the fail status is indicated by turning off the LED connected to RLED.

The twisted-pair cable integrity is monitored by detecting periodic link-integrity pulses at the RXI inputs. These pulses are 100ns in duration, with pre-distortion, followed by a return to idle. The receiver does not recognize these as data and is not enabled by them.

When no data frames are being received the NE86C92 provides a link-integrity reception window during which a link pulse is expected to arrive. The window opens nominally 5ms after receipt of the previous link pulse or the end of a data frame and remains open for 110ms. If a link pulse is received before the window opens then it is ignored. If a link pulse arrives while it is open then the internal window timers are reset. If no link pulse is received after 110ms, then the transmit, receive and loopback functions are disabled and a link failure is indicated by turning OFF the LED connected to RLED.

The NE86C92 can only re-enable the transmit, loopback and receive functions if it receives four consecutive link pulses within the link pulse window, or if a data frame is received. In either case the NE86C92 waits until both the transmit and receive paths are idle before re-enabling the transmit, loopback and receive paths.

When the link integrity circuit is enabled ($\overline{LI}$ connected to GND) a link integrity pulse is transmitted onto the twisted-pair cable typically once every 16ms irrespective of whether the transmitter is jabbed or there is a link integrity failure.

If the link integrity circuit is disabled ($\overline{LI}$ connected to V_{DD}) no link pulses are transmitted, the received link pulses are ignored and the RLED indicator remains ON in the absence of receive traffic.

Crystal Controlled Oscillator

Clock signals for the 50ns pre-distortion delay for transmitted data, the 10MHz collision signal and all on-chip timing functions are produced by a 20MHz crystal controlled oscillator.

An external MOS-level or TTL clock can also be applied directly to the XTAL1 input. In the case XTAL2 provides a buffered output of the signal applied to XTAL1; and may be left disconnected, used to drive other devices, or connected ground.

Any commercially available parallel resonant crystal may be used, but it is recommended that the total capacitance on each of the XTAL pins should be kept below 20pF.

LED Status Functions

The NE86C92 provides output drivers for five LED status indicators.

The LED connected to XLED indicates transmit status; (see Figure 8)

- The LED is ON when no transmission is in progress.
- The LED turns OFF when a data frame is transmitted and remains OFF for typically 115ms.
- The LED then turns back ON for a minimum of typically 6.4ms until turned OFF by the next transmission.

The LED connected to RLED indicates receive status and behaves differently depending on whether the link integrity circuit is disabled or enabled.

When the link integrity circuit is disabled; (see Figure 10)

- The LED is ON when no reception is in progress.
- The LED turns OFF when a data frame is received and remains OFF for typically 115ms.
- The LED then turns back ON for a minimum of typically 6.4ms until turned OFF by the next reception.

When the link integrity circuit is enabled the LED behavior is the same as above except that; (see Figure 2)

- The LED is ON when both no reception is in progress and link integrity pulses are being successfully received.
- The LED turns OFF in the event of a link failure
- The LED turns back ON for nominally 1sec when the the link is re-established.

The LED connected to CLED indicates collision status; (see Figure 9)

- The LED is OFF for no collision.
- The LED turns ON for nominally 12ms in the event of a collision.
- The LED remains ON if a further collisions occur during this time and remains ON for the nominal on-time following the last transition.
- There is no minimum OFF time. The LED will turn ON immediately another collision is detected.

The LED connected to JLED indicates jabber status; (see Figure 7)

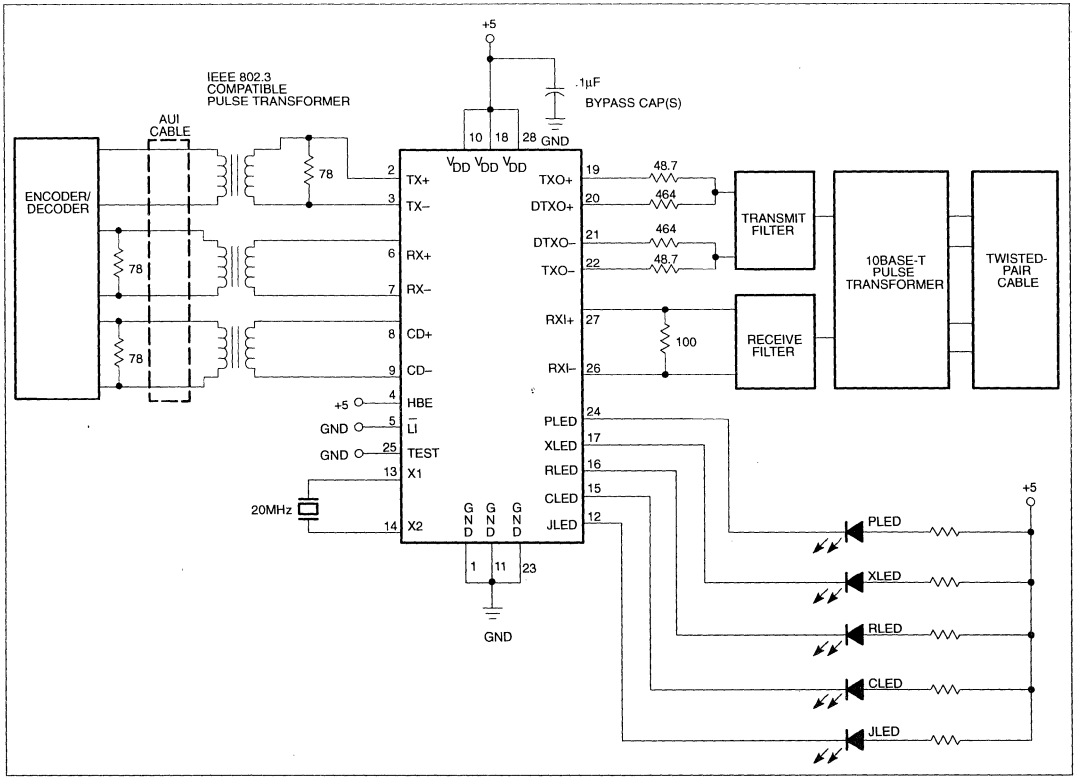
- The LED is OFF for a no-jab condition.
- The LED turns ON when the twisted-pair drivers are jabbed.
- The LED turns back OFF when the twisted-pair drivers are unjabbed.

The LED connected to PLED (when used) indicates polarity reversal status;

- The LED is ON when there is no polarity reversal of the twisted-pair receive wires.
- The LED is OFF when the polarity is reversed.
- The LED flashes during link-fail before polarity has been determined.

The LED drivers require an external resistor in series with the LED (see connection diagram) to limit the LED current.

TYPICAL APPLICATION DIAGRAM



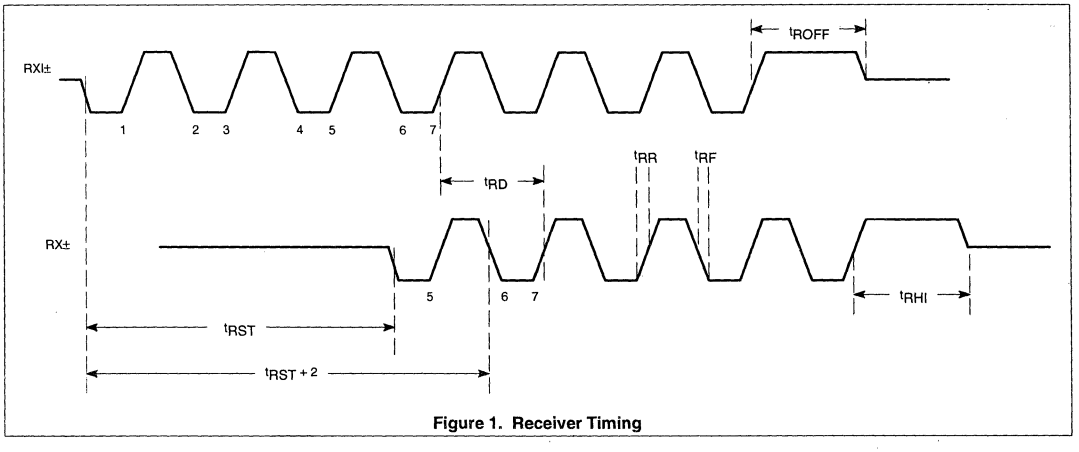


Figure 1. Receiver Timing

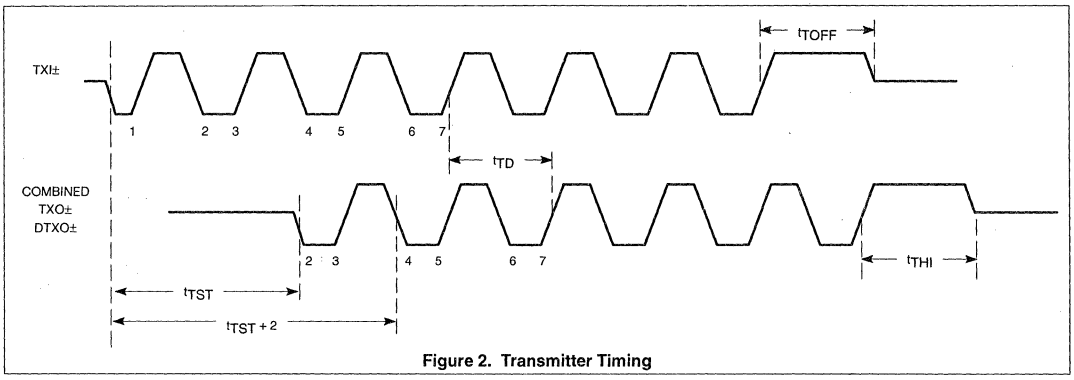


Figure 2. Transmitter Timing

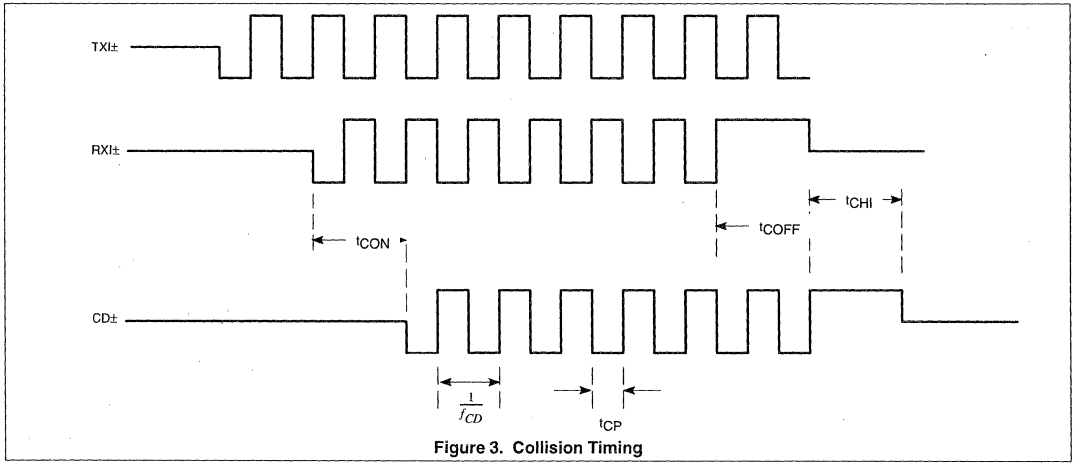


Figure 3. Collision Timing

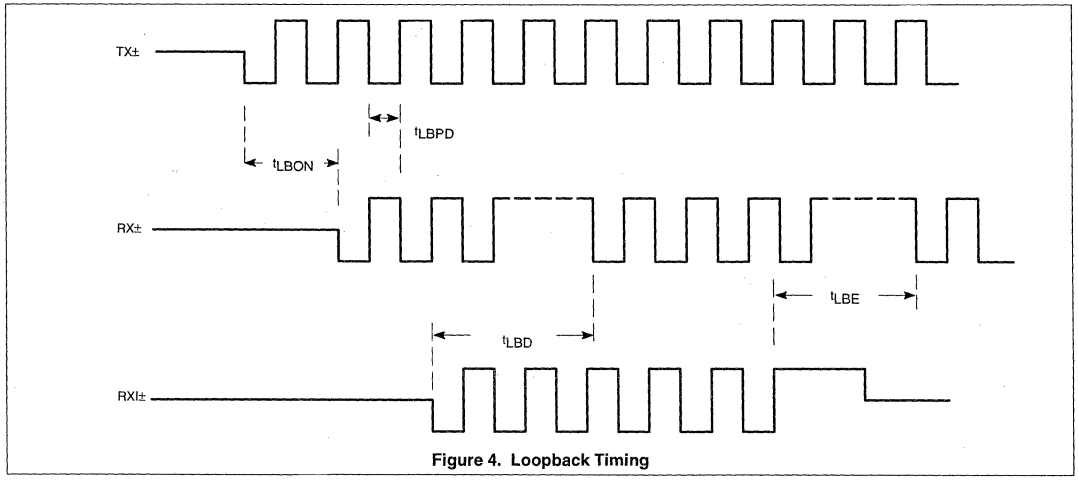


Figure 4. Loopback Timing

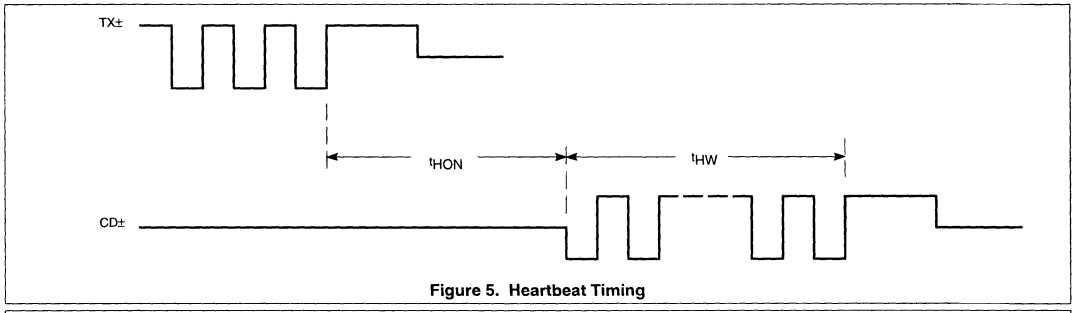


Figure 5. Heartbeat Timing

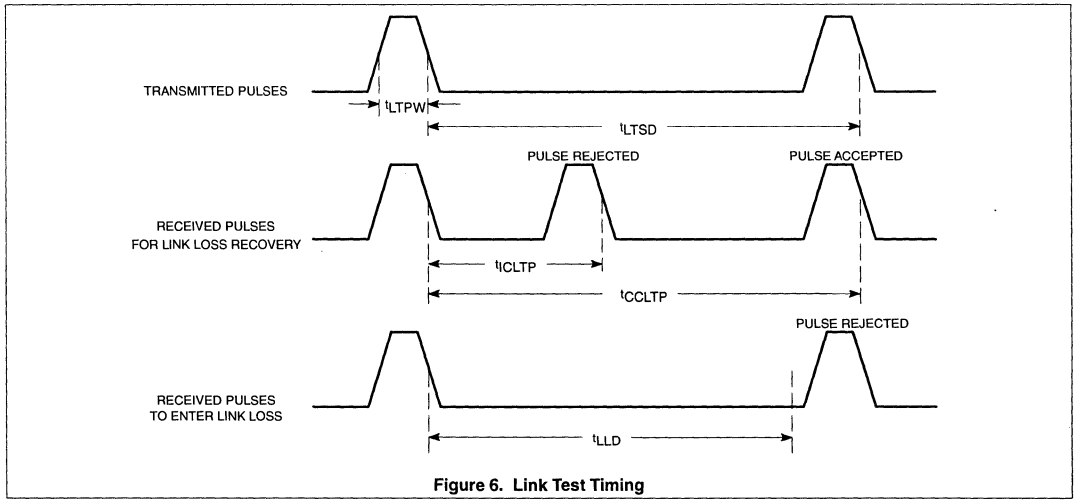


Figure 6. Link Test Timing

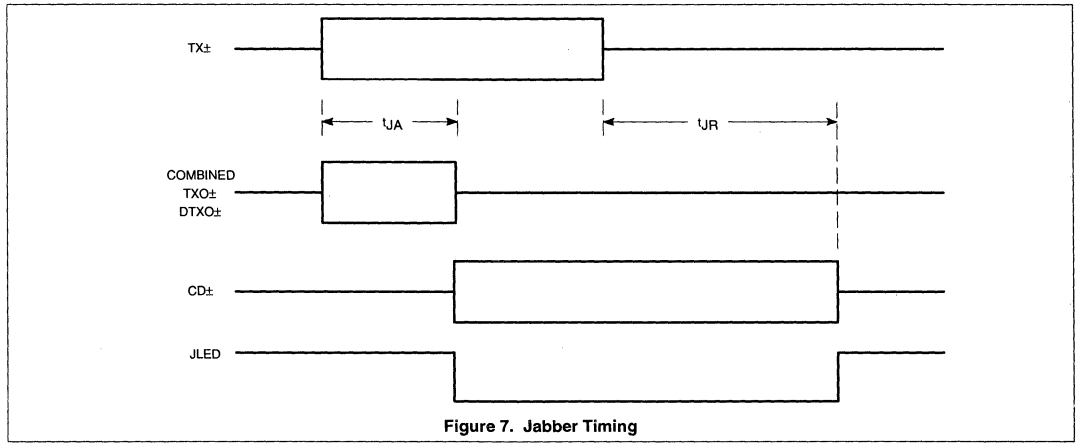


Figure 7. Jabber Timing

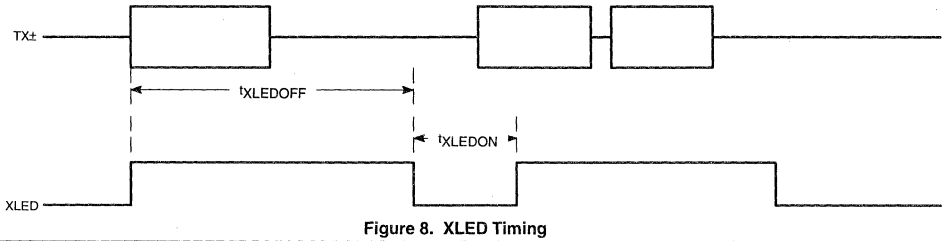


Figure 8. XLED Timing

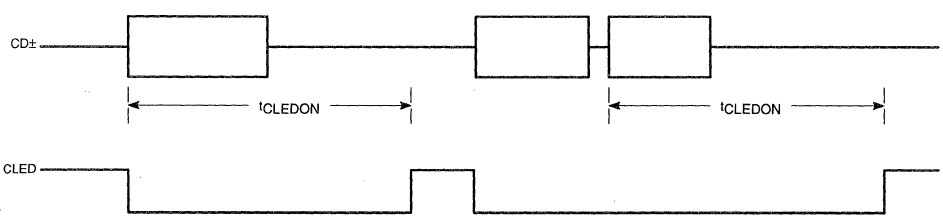


Figure 9. CLED Timing

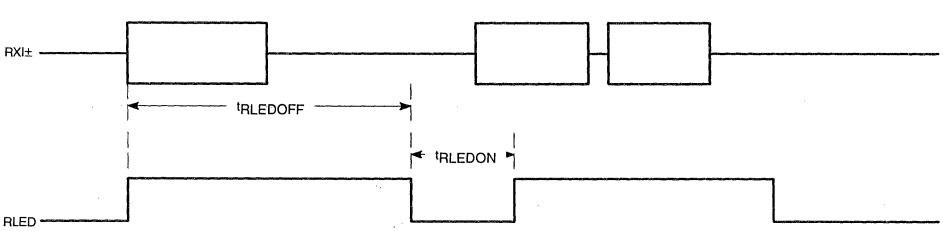


Figure 10. RLED Timing (LI Disabled)

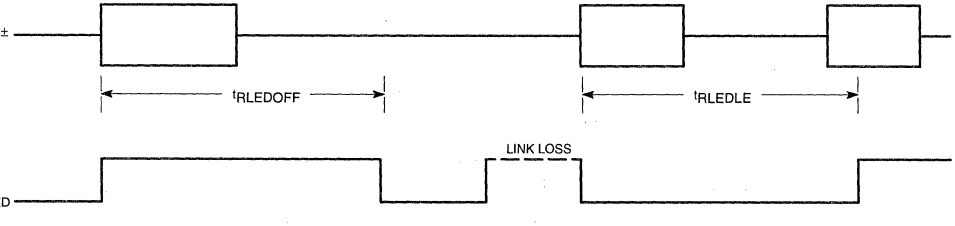


Figure 11. RLED Timing (LI Enabled)

Using the NE86C92 10BASE-T transceiver in AT&T T7220 applications

AN4001

INTRODUCTION

The NE86C92 transceiver offers a number of advanced features over the AT&T T7220, including automatic polarity correction, substantially lower power consumption and reduced external parts count. The NE86C92 can be easily incorporated into existing designs which use the AT&T T7220 twisted-pair transceiver. The conversion is quite simple, often requiring only component deletions from the existing circuit. The information provided herein will allow conversion of virtually any T7220 based design to utilize the NE86C92.

ADDITIONAL FEATURES AVAILABLE WITH THE NE86C92

When upgrading to the NE86C92 from the T7220 the following features are immediately realized:

- Automatic polarity correction
- Substantially lower current consumption
- Reduced external parts count

The following additional features are also available with minor design modifications:

- Automatic selection between AUI and twisted-pair ports
- Polarity indication

DESCRIPTION

The circuit shown in 1 is a typical application of the T7220. Upgrading to use the NE86C92 twisted-pair transceiver is often requires only deletion or removal of several external resistors and capacitors. Figure 2 illustrates the changes required to convert the circuit in Figure 1 for use with the NE86C92.

The T7220 requires use of a double-ended termination scheme on the AUI cable's DI and CI circuits. This approach requires additional parts and increases overall current consumption since the drivers see only a 39Ω load. The NE86C92 requires only the standard single termination at the signal destination. Therefore, the 78Ω terminations across the RX± and the CD± output pairs should be eliminated.

When using an external 20MHz crystal, the T7220 based circuit requires a minor modification to work with the NE86C92. The T7220 uses a single-ended crystal oscillator with one side connected to ground (Pin 14). Rather than a single-ended oscillator, the NE86C92 uses a highly reliable two-pin oscillator circuit. This requires that Pin 14 be isolated from ground and connected only to the crystal.

The T7220's AUI output drivers have a large AC common-mode component requiring the use of capacitors from each of the transformer secondary pins to ground in order to bring the output waveforms within the IEEE waveform specifications. The NE86C92 does not require these capacitors and it is recommended that they be removed although it will still function satisfactorily with these parts installed.

Twisted-pair receiver termination and the AUI DO± terminations are required to be referenced to an external common mode voltage, V_{COM}, of $V_{DD/2}$ for use with the T7220. When using the NE86C92, the external common mode voltage is strictly optional as it is set internally. This referenced termination network may be replaced with a single terminating resistor between the TX± lines and also between the RXI± lines.

If polarity indication is also desired, an additional LED and current limiting resistor may be added and connected between PLED (Pin 24) and +5 volts. However, even with no LED installed, the polarity correction feature will be active. (Unless Pin 24 is connected to ground to disable polarity control.)

SHORTCUT FOR APPLICATIONS USING AN EXTERNAL CLOCK SOURCE

The NE86C92 can be used as a direct replacement for the T7220 in applications which use an external 20MHz clock source in place of the external crystal by simply removing two (2) external resistors.

To use the the NE86C92 in this application, remove the 78Ω resistors across the RCV and CLSN outputs of the transceiver. The other changes specified in 2 may be incorporated, but only the removal of the two resistors is required.

The NE86C92 will operate correctly even if Pin 14 of the T7220 was connected to ground. The device will draw approximately 10mA of additional current due to the crystal output pin being connected to ground. However, leaving Pin 14 grounded does not effect the performance of the device.

PROVISIONS FOR ALTERNATE SOURCING

For designs requiring alternate sourcing of critical components, a special circuit implementation which allows use of either the NE86C92 or the T7220 is shown in 3. This option can be implemented either as a loading option or a jumper option. Because of the lower external parts count of the NE86C92, implementation as a loading option with the default configuration using the NE86C92 is recommended.

SUMMARY

The NE86C92 can be easily incorporated into existing AT&T based 10BASE-T designs providing enhanced features, lower power consumption and reduced external parts count.

Using the NE86C92 10BASE-T transceiver in AT&T T7220 applications

AN4001

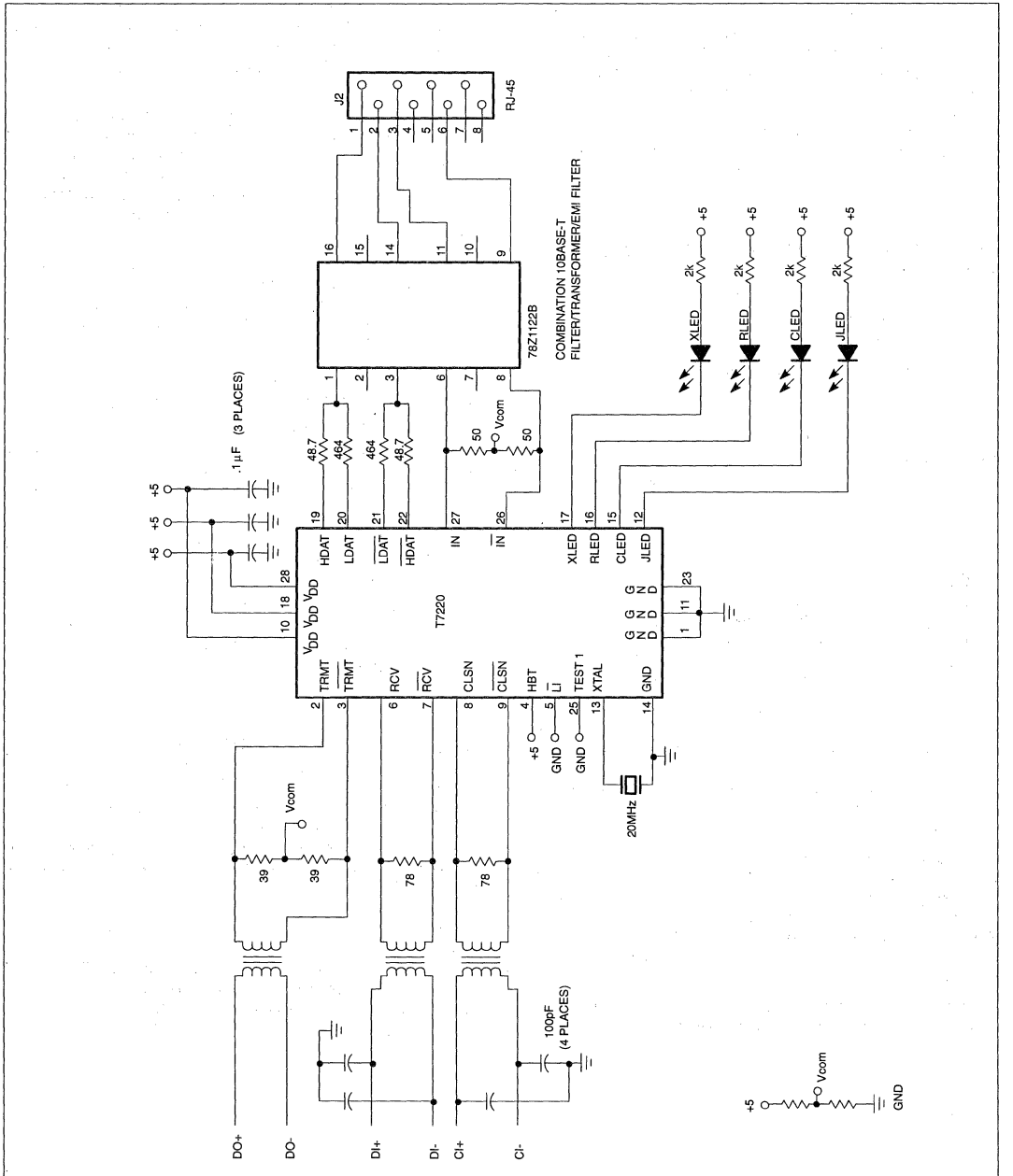


Figure 1. Typical T7220 Application

Using the NE86C92 10BASE-T transceiver in AT&T T7220 applications

AN4001

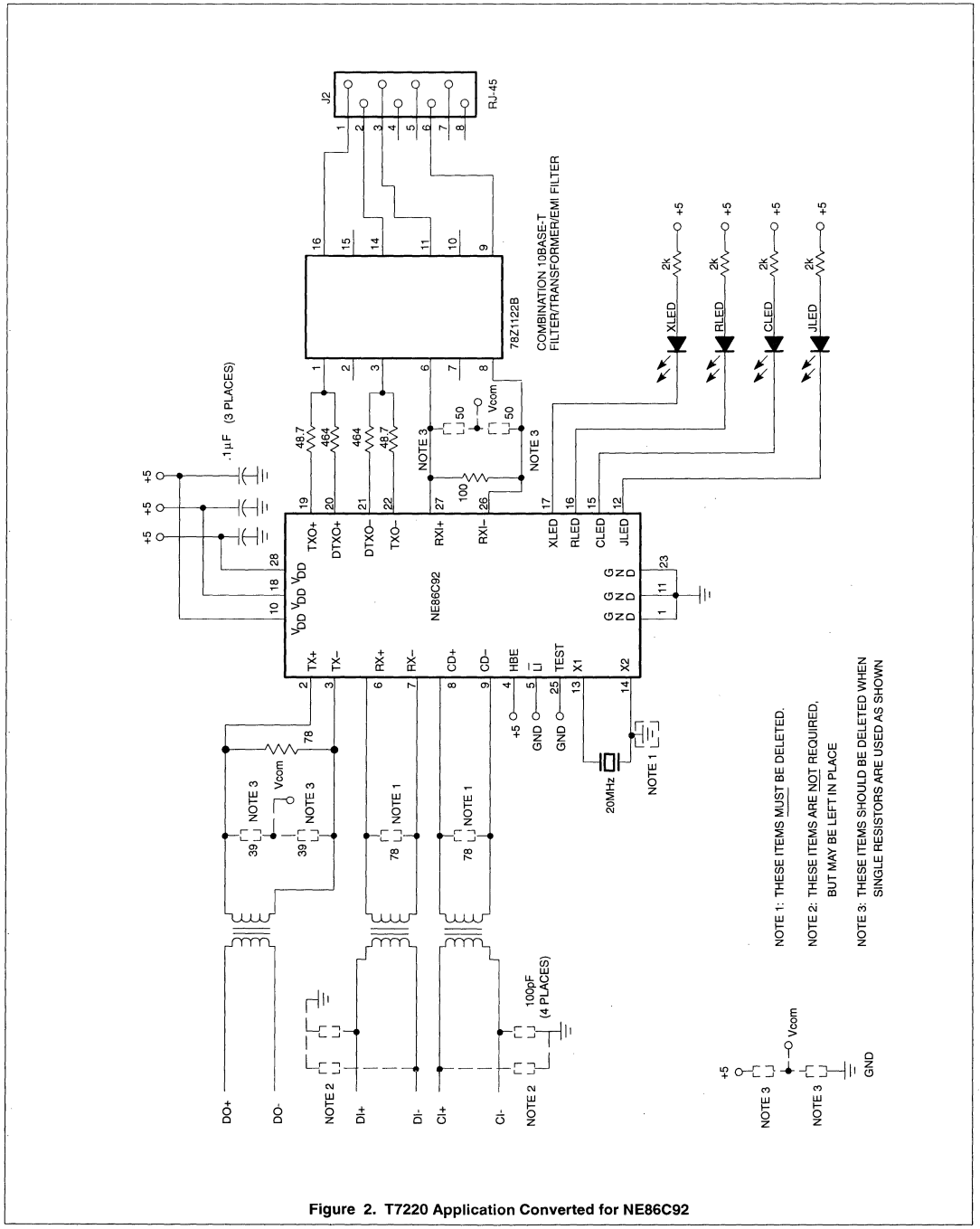


Figure 2. T7220 Application Converted for NE86C92

Using the NE86C92 10BASE-T transceiver in AT&T T7220 applications

AN4001

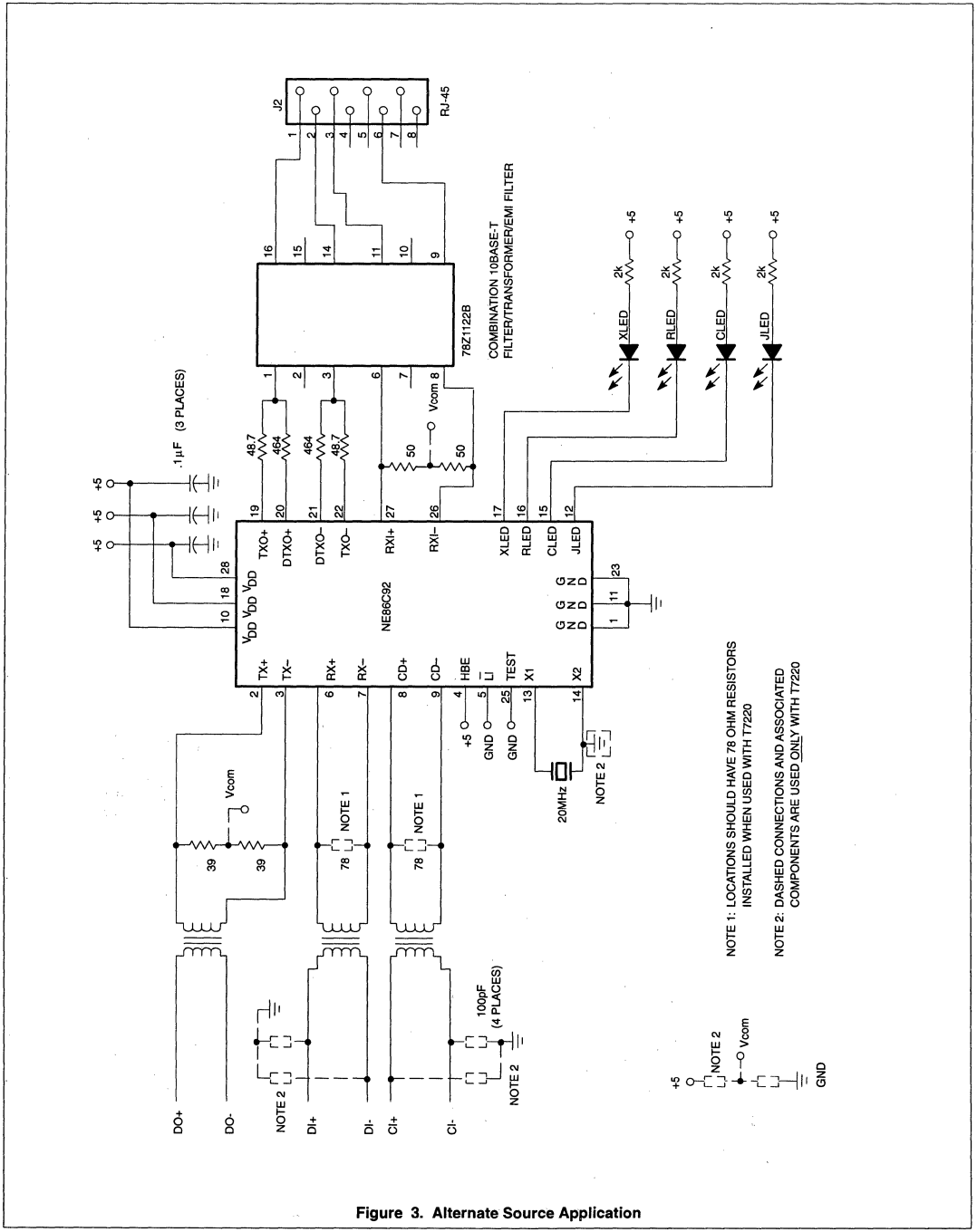


Figure 3. Alternate Source Application

Automatic selection between AUI port and internal NE86C92 10BASE-T transceiver

AN4002

INTRODUCTION

The NE86C92 provides the designer of a 10BASE-T Ethernet interface card the ability to design a card without having to provide a switch or jumper array to change between AUI and twisted-pair connections. The NE86C92 provides automatic changeover whenever the external cable connection is changed. This feature provides not only a cost savings to the manufacturer, but it is also of great value to the end-user since the task of interchanging between a twisted-pair cable and an AUI device or cable drop no longer requires opening of the computer to change switches or jumpers.

DESCRIPTION

Figure 1 shows a block diagram of a typical network interface card application. In this example, if the computer or workstation is moved from the twisted-pair cable connection to the AUI cable connection, it would be necessary to open the computer, remove the network interface card, change switch or jumper settings, re-install the card and close the computer. This all requires some degree of expertise in order to accomplish the task successfully without causing damage to the computer or interface card.

Figure 2 illustrates the same application, this time using the NE86C92 in the jumperless configuration. Note the absence of any jumper or switch selection in the data paths between the EN/DEC, transceiver and AUI connector. Automatic selection is accomplished using the circuit implementation as shown in Figure 2.

The NE86C92 automatically selects the AUI port by placing the RX± and CD± outputs in a high-impedance state in the absence of incoming signals from the twisted-pair line. When the twisted-pair cable is disconnected, all incoming receive signals disappear and the device places the RX and CD outputs in their high-impedance state. With the device in this state, an external AUI device may be connected and used.

The TX± inputs are high-impedance inputs. Note that the usual 78Ω terminating resistor across the inputs has been deleted, thus eliminating the double termination condition when using an external device connected to the AUI port. Signal levels present at the TX input to the NE86C92 will be slightly higher than with the terminating resistor, but this will have no significant effect on performance.

Changing back to the twisted-pair connection is accomplished by simply disconnecting the AUI cable and re-connecting the twisted-pair cable. Selection of the twisted-pair port occurs automatically upon re-connection.

CAPACITIVE VS TRANSFORMER COUPLING

Note that in the application schematic provided in Figure 3, the signals to and from the EN/DEC are capacitively, rather than transformer coupled. In the controlled environment of an interface card, there is no substantial difference in the signal characteristics when using capacitive vs. transformer coupling. There is however, a notable improvement in signal quality over long AUI cables when the local (internal) transceiver is capacitively, rather than transformer coupled.

LAYOUT CONSIDERATIONS

Layout of Ethernet boards is always an important consideration. However, since both the AUI connector and the internal transceiver are always connected to the circuit, special care should be taken in board layout. The following recommendations will help to insure successful implementation of this feature:

- Coupling capacitors in the DO, DI and CI lines should be located as close as practical to the transceiver chip (preferably within 1/2 - 1 inch).
- Care should be taken to avoid creation of "stubs" on the DO, DI or CI signal traces. As in all ethernet designs, it is recommended that the length of these traces be kept to a minimum.
- If long parallel runs of separate signal pairs are necessary (i.e., DI runs parallel to DO), they should be separated by a ground trace to minimize crosstalk.

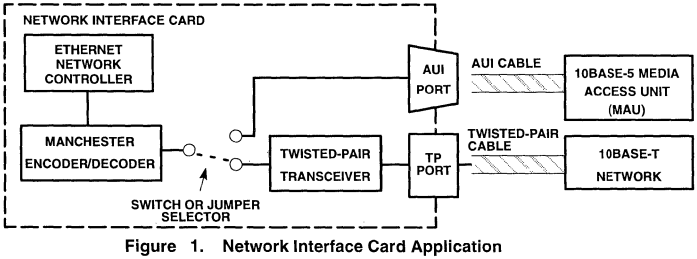


Figure 1. Network Interface Card Application

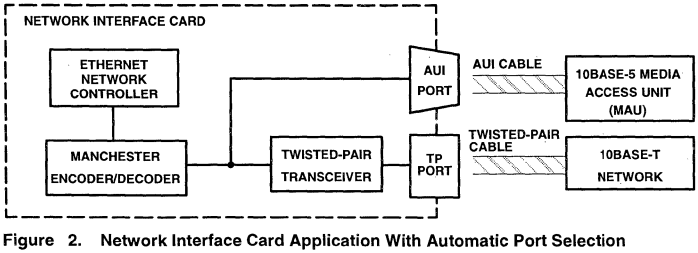


Figure 2. Network Interface Card Application With Automatic Port Selection

Automatic selection between AUI port and internal NE86C92 10BASE-T transceiver

AN4002

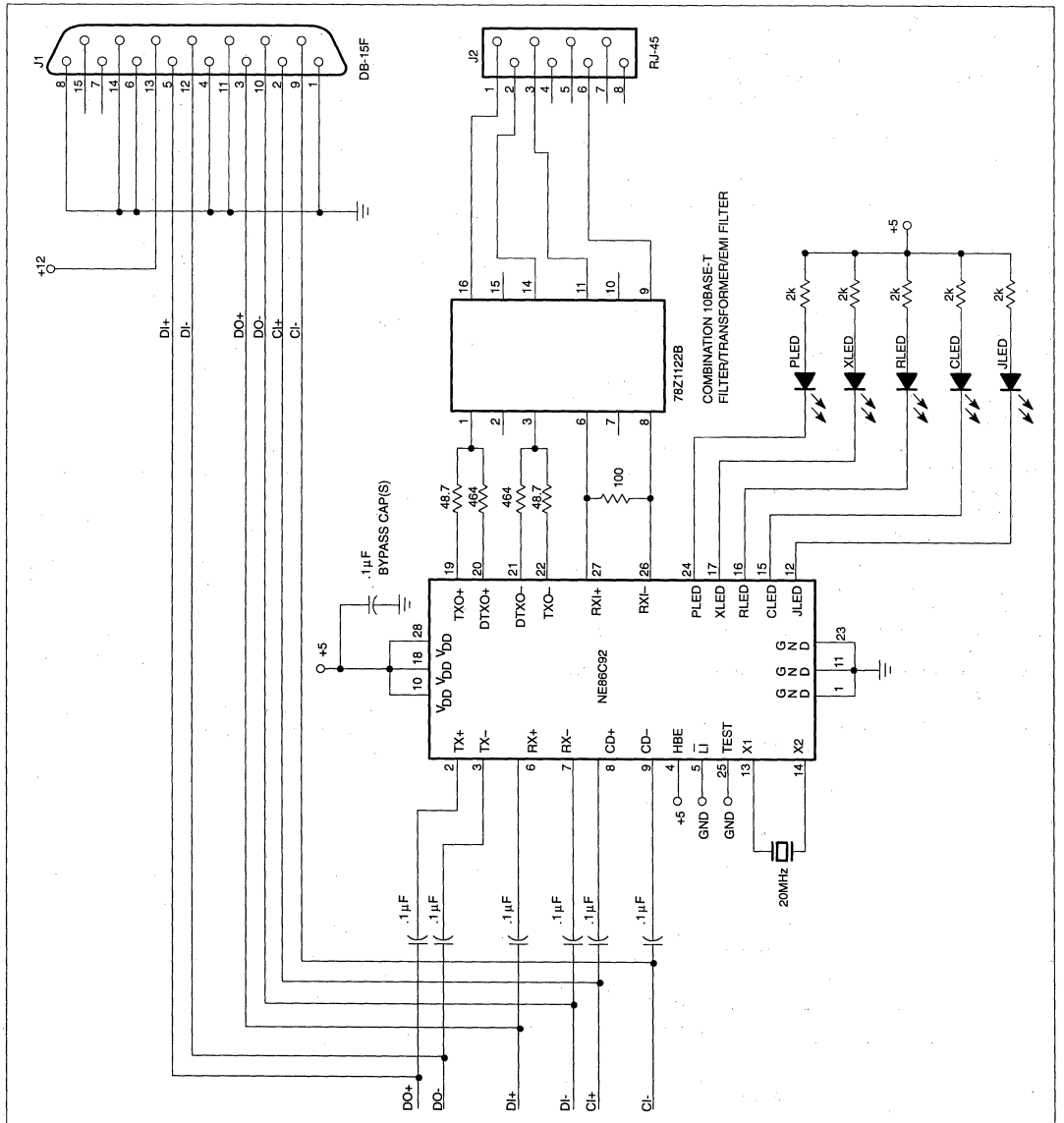


Figure 3. Internal 10BASE-T MAU With Automatic Port Selection

SUMMARY

The NE86C92 provides an extremely simple and cost-effective method for elimination of port selection hardware on 10BASE-T network interface boards; thus providing higher reliability, and reduced maintenance and configuration costs.

Low-power coaxial Ethernet transceiver — NE83Q92

DESCRIPTION

The NE83Q92 is a low power coaxial transceiver interface (CTI) for Ethernet (10base5) and Thin Ethernet (10base2) local area networks. The CTI is connected between the coaxial cable and the Data Terminal Equipment (DTE) and consists of a receiver, transmitter, collision detector, heartbeat generator and jabber timer (see Block Diagram). The transmitter output connects directly to a doubly terminated 50Ω cable, while the receiver output, collision detector output and transmitter input are connected to the DTE through isolation transformers. Isolation between the CTI and the DTE is an IEEE 802.3 requirement that can be met on signal lines by using a set of pulse transformers normally available in a standard 16-pin DIP. Power isolation for the CTI is achieved using DC-to-DC conversion through a power transformer (see Figure 1, Connection Diagram).

The part is fully pin compatible with the industry standard 8392A, but has substantially lower current consumption, is fully compliant with the IEEE802.3 standard, and has additional features such as a low current standby mode with automatic selection between AUI and coaxial connections, and extended mode collision default.

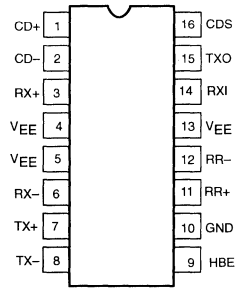
The NE83Q92 is manufactured on an advanced BiCMOS process and is ideally suited to lap-top personal computers or systems where low power consumption and no changing of board jumper positions is required.

FEATURES

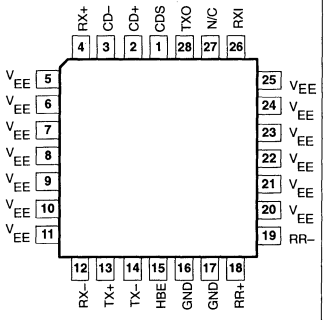
- Fully compliant with Ethernet II, IEEE 802.3 10BASE-5 and 10BASE-2, and ISO 8802/3 interface specifications
- 100% drop-in compatible with industry standard 8392 sockets
- Lowest overall current consumption allows operation using 1 Watt DC-DC converter
- Lowest power configuration provides reduced external parts count
- High efficiency AUI drivers minimize current consumption under idle conditions
- Automatically enters standby mode when no coaxial cable is connected
- Standby mode allows automatic selection between AUI and Coaxial connections when no coaxial cable is connected
- Smart squelch on data inputs eliminates false activations
- Advanced BiCMOS process for extremely low power operation
- Available in 16-pin DIP, 16-pin SOL and 28-pin PLCC
- Expanded version (NE83Q93) available for repeater and advanced system applications

PIN CONFIGURATION

D, N Packages



A PACKAGE



ORDERING INFORMATION

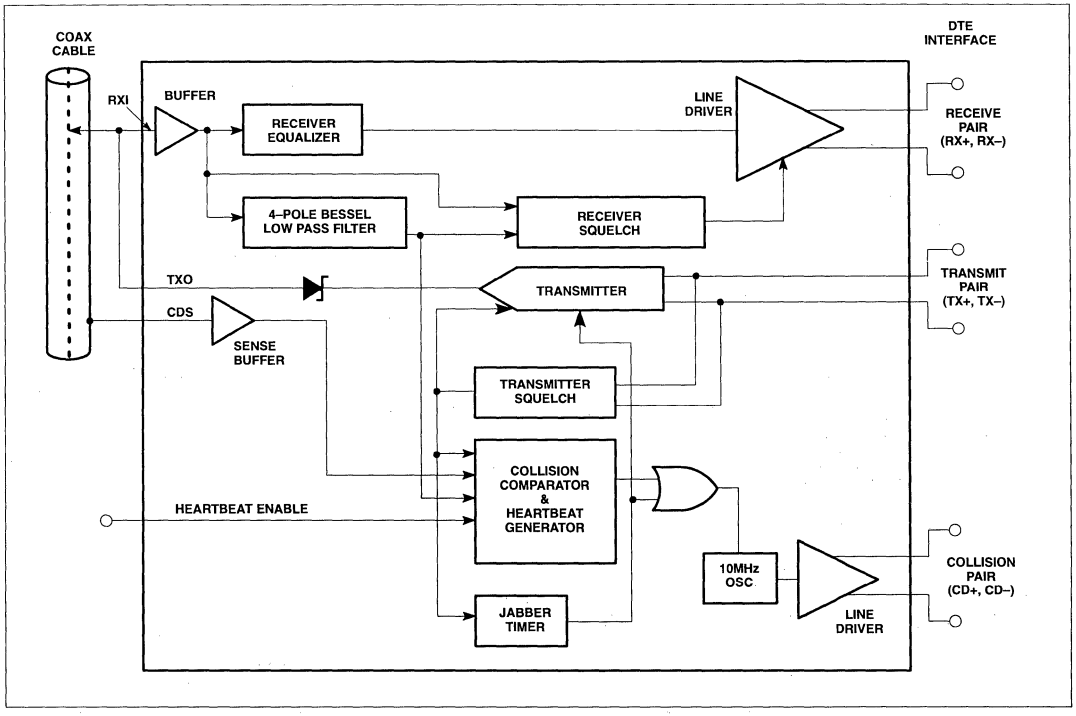
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package	0 to +70°C	NE83Q92N	0406C
16-Pin Plastic Small Outline Large	0 to +70°C	NE83Q92D	0171B
28-Pin Plastic Leaded Chip Carrier	0 to +70°C	NE83Q92A	0401F

PIN DESCRIPTIONS

PIN NO. N PKG	PIN NO. PLCC	SYMBOL	DESCRIPTION
1 2	2 3	CD+ CD–	**Collision Outputs.** Balanced differential line driver outputs which send a 10MHz signal to the DTE in the event of a collision, jabber interrupt or heartbeat test.
3 6	4 12	RX+ RX–	**Receiver Outputs.** Balanced differential line driver outputs which send the received signal to the DTE.
7 8	13 14	TX+ TX–	**Transmitter Inputs.** Balanced differential line receiver inputs which accept the transmission signal from the DTE and apply it to the coaxial cable at TXO.
9	15	HBE	**Heartbeat Enable.** The heartbeat function is disabled when this pin is connected to V_{EE} and enabled when connected to GND or left floating.
11 12	18 19	RR+ RR–	**External Resistor.** A 1kΩ (1%) resistor connected between these pins establishes the signaling current at TXO.
14	26	RXI	**Receiver Input.** This pin is connected directly to the coaxial cable. Received signals are equalized, amplified, and sent to the DTE through the RX± pins.
15	28	TXO	**Transmitter Output.** This pin is connected directly (Thin Ethernet) or through an external isolating diode (Ethernet) to the coaxial cable.
16	1	CDS	**Collision Detect Sense.** Ground sense connection for the collision detection circuitry. This pin should be connected directly to the coaxial cable shield for standard Ethernet operation. Leaving CDS unconnected will default the collision threshold to extended mode thin Ethernet operation.
10	16 17	GND	**Positive Supply Pin.**
4 5 13	5 to 11 20 to 25	V_{EE}	**Negative supply pins.**

NOTE:
1. The IEEE 802.3 name for CD is CI; for RX is DI; for TX is DO.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage[1]	–12	V
V_{IN}	Voltage at any input[1]	0 to –12	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec.)	+300	°C
T_J	Recommended max junction temperature[2]	+150	°C
θ_{JA}	Thermal impedance (N and A packages)	60	°C/W

NOTE:

1. 100% measured in production.
2. The junction temperature is calculated from the following expression:

$$T_J = T_A + \theta_{JA} (V_{EE} \times 0.015 \times n_{IDL}) + (V_{EE} \times 0.033 \times n_{RX}) + (V_{EE} \times 0.075 \times n_{TX})$$

where

T_A = Ambient temperature in °C.
θ_{JA} = Thermal resistance of package.
V_{EE} = Normal operating supply voltage in volts.
n_{IDL} = Percentage of duty cycle idle
n_{RX} = Percentage of duty cycle receiving
n_{TX} = Percentage of duty cycle transmitting

ELECTRICAL CHARACTERISTICS

V_{EE} = –9V ±6%; T_A = 0°C to +70°C unless otherwise specified[1,2]. No external isolation

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{UVL}	Under voltage lockout. Transceiver disabled for $\|V_{EE}\| < \|V_{UVL}\|$			–7.5		V
I_{EE}	Supply current idle			–15	–20	mA
	Supply current transmitting	Without AUI resistors		–60	–85	mA
I_{RXI}	Receive input bias current	V_{RXI} = 0V	–2		+25	µA
I_{CDS}	Cable sense input bias current	V_{CDS} = 0V		+1	+3	µA
V_{IH}	HBE input HIGH voltage		V_{EE} +2.4			V
V_{IL}	HBE input LOW voltage				V_{EE} +1.6	V
I_{IH}	HBE input HIGH current	V_{HBE} = 0V			+10	µA
I_{IL}	HBE input LOW current	V_{HBE} = V_{EE}	–20			µA
I_{TDC}	Transmit output DC current level[3]		–37		–45	mA
I_{TAC}	Transmit output AC current level[3]		±28		±I_{TDC}	mA
I_{TX10}	Transmit current	V_{TXO} = –10V	–250		+250	µA
V_{TCOM}	Transmitter output voltage compliance[4]				–3.7	V
V_{CD}	Collision threshold[5]	Measured by applying DC voltage at RXI (CDS = 0V)	–1450	–1530	–1580	mV
V_{DIS}	AUI disable voltage at RXI	Measured as DC voltage at RXI		–3.5		V
V_{OD}	Differential output voltage – non idle at RX± and CD±[6]		±600		±1100	mV
V_{OB}	Differential output voltage imbalance – idle at RX± and CD±[7]				±40	mV
V_{OC}	Output common mode voltage at RX± and CD±	RXI = 0V	–4.5	–5.5	–6.5	V
V_{RS}	Receiver squelch threshold	V_{RXI} average DC (CDS = 0V)	–150	–250	–350	mV
V_{TS}	Transmitter squelch threshold	(V_{TX+} – V_{TX-}) peak	–175	–225	–275	mV
R_{RXI}	Shunt resistance at RXI non–transmitting		100			kΩ
C_{RXI}	Input capacitance at RXI			1	2	pF
R_{TXO}	Shunt resistance at TXO transmitting		7.5	10		kΩ
R_{AUIZ}	Differential impedance at RX± and CD± with no coaxial cable connected			3		kΩ
R_{TX}	Differential impedance at TX±			20		kΩ

NOTES:

1. Currents flowing into device pins are positive. All voltages are referenced to ground unless otherwise specified. For ease of interpretation, the parameter limit that appears in the MAX column is the largest value of the parameter, irrespective of sign. Similarly, the value in the MIN column is the smallest value of the parameter, irrespective of sign.
2. All typicals are for V_{EE} = –9V and T_A = 27°C.
3. I_{TDC} is measured as (V_{MAX} + V_{MIN})/(2 x 25) where V_{MAX} and V_{MIN} are the max and min voltages at TXO with a 25Ω load between TXO and GND. I_{TAC} is measured as (V_{MAX} – V_{MIN})/(2 x 25).
4. The TXO pin shall continue to sink at least I_{TDC} min when the idle (no signal) voltage on this pin is –3.7V.
5. Collision threshold for an AC signal is within 5% of V_{CD}.
6. Measured on secondary side of isolation transformer (see Connection Diagram, Figure 1). The transformer has a 1:1 turns ratio with an inductance between 30 and 100µH at 5MHz.
7. Measured as the voltage difference between the RX pins or the CD pins with the transformer removed.

TIMING CHARACTERISTICS

V_{EE} = –9V ±6%; T_A = 0 to 70°C, unless otherwise specified[1]. No external isolation diode on TXO.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{RON}	Receiver start up delay RXI to RX± (Figure 4) First received bit on RX±	V_{RXI} = –2V peak		3	5	bits
	First validly timed bit on RX±				t_{RON} +2	bits
t_{RD}	Receiver prop. delay RXI to RX±	V_{RXI} = –2V peak		20	50	ns
t_{RR}	Differential output rise time on RX± and CD±[2,3]			5	7	ns
t_{RF}	Differential output fall time on RX± and CD±[2,3]			5	7	ns
t_{OS}	Differential output settling time on RX± and CD± to V_{OB} = 40mV[2] (see Figure 5)			1		µs
t_{RJ}	Receiver and cable total jitter			±2	±6	ns
t_{RHI}	Receiver high to idle time	Measured to +210mV	200		850	ns
t_{RM}	Rise and fall time matching on RX± and CD±	$t_{RF} - t_{RR}$		0.4	±2	ns
t_{TST}	Transmitter start–up delay TX± to TXO (Fig. 6) First transmitted bit on TXO	$V_{TX±}$ = –1V peak		1	2	bits
	First validly timed bit				t_{TST} + 2	bits
t_{TD}	Transmitter prop delay TX± to TXO (see Figure 6)	$V_{TX±}$ = 1V peak	5	20	50	ns
t_{TR}	Transmitter rise time 10% to 90% (see Figure 6)		20	25	30	ns
t_{TF}	Transmitter fall time 10% to 90% (see Figure 6)		20	25	30	ns
t_{TM}	$t_{TF} - t_{TR}$ mismatch				±2	ns
t_{TS}	Transmitter added skew[4]				±2	ns
t_{TON}	Transmitter turn on pulse width (see Figure 6)	$V_{TX±}$ = 1V peak	10		35	ns
t_{TOFF}	Transmitter turn off pulse width (see Figure 6)	$V_{TX±}$ = 1V peak	125		225	ns
t_{CON}	Collision turn on delay (see Figure 7)	0V to –2V step at RXI			13	bits
t_{COFF}	Collision turn off delay (see Figure 7)	–2V to 0V step at RXI			16	bits
t_{CHI}	Collision high to idle time (see Figure 7)	Measured to +210mV	200		850	ns
f_{CD}	Collision frequency (see Figure 7)		8.5	10	11.5	MHz
t_{CP}	Collision signal pulse width (see Figure 7)		35		70	ns
t_{HON}	Heartbeat turn on delay (see Figure 8)		0.6		1.6	µs
t_{HW}	Heartbeat test duration (see Figure 8)		0.5		1.5	µs
t_{JA}	Jabber activation delay measured from TX± to CD± (see Figure 9)		20		60	ms
t_{JR}	Jabber reset delay measured from TX± to CD± (see Figure 9)		250		650	ms

NOTES:
1. All typicals are for V_{EE} = –9V and T_A = 27°C.
2. Measured on secondary side of isolation transformer (see Figures 1 and 2, Connection Diagram). The transformer has a 1:1 turn ratio with an inductance between 30 and 100µH at 5MHz.
3. The rise and fall times are measured as the time required for the differential voltage to change from –225mV to +225mV, or +225mV to –225mV, respectively.
4. Difference in propagation delay between rising and falling edges at TXO.

FUNCTIONAL DESCRIPTION

The NE83Q92 is a low power coaxial Ethernet transceiver which complies with the IEEE 802.3 specification and offers a number of additional features. These features are:

a. Low current consumption of typically 15mA when idle and 80mA with full traffic (transmitting and colliding) allows smaller DC-DC converter to be used for the isolated power supply.

b. Automatic selection between AUI cable and coaxial connections by placing the AUI outputs in a high impedance state when the coaxial cable is disconnected. This eliminates the need for changing a jumper position on the Ethernet board when selecting either Thin Ethernet or remote transceiver connections.

c. High efficiency AUI drivers for the RX± and CD± ports which automatically power down when idle. The NE83Q92 requires no external pull-down resistors on these ports, but will still operate if they are present.

Receiver Functions

The receiver consists of an input buffer, a cable equalizer, a 4-pole Bessel low pass filter, a squelch circuit and a differential line driver.

The buffer provides high input resistance and low input capacitance to minimize loading and reflections on the coaxial cable.

The equalizer is a high pass filter that compensates for the low pass effect of the coaxial cable and results in a flatband response over all signal frequencies to minimize signal distortion.

The 4-pole Bessel low pass filter extracts the average DC voltage level on the coaxial cable for use by the receiver squelch and collision detection circuits.

The receiver squelch circuit prevents noise on the coaxial cable from falsely triggering the receiver in the absence of a true signal. At the beginning of a packet, the receiver turns on when the DC level from the low pass filter exceeds the DC squelch threshold and the received packet has started with a 01 bit sequence with acceptable timing parameters. For normal signal levels this will take less than 500ns, or 5 bits. However, at the end of a packet, a fast receiver turn off is needed to reject both dribble bits on the coaxial cable and spurious responses due to settling of the on-chip bandpass filter. This is accomplished by an AC timing circuit that disables the receiver if the signal level on the coaxial cable remains high for typically 250ns and only enables the receiver again after approximately .5µs. Figures 4 and 5 illustrate receiver timing.

The differential line driver provides typically ±900mV signals to the DTE with less than 7ns rise and fall times. When in idle state (no received signal) its outputs provide <20mV differential voltage offset to minimize DC standing current in the isolation transformer. The line driver outputs (RX± and CD±) require no external pull-down resistors and will drive a 78Ω transmission line directly. They automatically power down under idle conditions and are powered up when a receive signal is detected. The drivers will still operate with external resistors present so can be retro-fitted into existing 8392A boards. However, an extra current of 7mA/output (for 500Ω resistors) would be generated by these resistors irrespective of whether the transceiver is idle or responding to traffic.

Transmitter Functions

The transmitter has differential inputs and an open collector current driver output. The differential input common mode voltage is established by the CTI and should not be altered by external circuitry. Controlled rise and fall times of 25ns (±5ns) minimize higher harmonic components in the transmitted spectrum, while matching of these rise and fall times to typically 2ns minimizes signal jitter. The drive current levels of the CTI are set by an on-chip bandgap voltage reference and an external 1% resistor. An on-chip isolation diode is provided to reduce the transmitter's coaxial cable load capacitance. For Thin Ethernet applications, no further external isolation diode is required, since the NE83Q92 meets the capacitive loading specifications. For Ethernet applications a further external diode should be added to reduce loading capacitance.

The transmitter squelch circuit ensures that the transmitter can only be enabled if the transmitted packet begins with a 01 bit sequence where the negative-going differential signals are typically greater than 225mV in magnitude and 25ns in duration.

The transmitter will be disabled at the end of a packet if there are no negative going signals of greater than 225mV for more than typically 150ns. Figure 6 illustrates transmitter timing.

Collision Functions

The collision detection scheme implemented in the NE83Q92 is receive mode detection, which detects a collision between any two stations on the network with certainty at all times, irrespective of whether or not the local DTE is producing one of the colliding signals. This is the only detection scheme allowed by the IEEE 802.3 standard for both repeater and non-repeater nodes.

The collision circuitry consists of the 4-pole Bessel low pass filter, a comparator, a precision voltage reference that sets up the collision threshold, a heartbeat generator, a 10MHz oscillator, and a differential line driver.

The collision comparator monitors the DC level at the output of the low pass filter and enables the line driver if it is more negative than the collision threshold. A collision condition is indicated to the DTE by a 10MHz oscillation signal at the CD outputs and typically occurs within 700ns of the onset of the collision. The collision signal begins with a negative-going pulse and ends with a continuous high-to-idle state longer than 170ns. Figure 7 illustrates collision timing.

At the end of every transmission, the heartbeat generator creates a pseudo collision to ensure that the collision circuitry is properly functioning. This pseudo collision consists of a 1µs burst of 10MHz oscillation at the line driver outputs approximately 1µs after the end of the transmission. The heartbeat function can be disabled externally by connecting the HBE (heartbeat enable) to V_{EE}. This allows the CTI to be used in repeater applications. Figure 8 illustrates heartbeat timing.

As with the receiver AUI drivers, the CD± outputs require no external pull-down resistors, although they still operate if the resistors are present, and automatically power down under idle conditions.

Jabber Functions

The jabber timer monitors the transmitter and inhibits transmission if it is active for longer than typically 30ms. The jabber circuit then enables the collision outputs for the remainder of the data packet and for typically 450ns (unjab time) after it has ended. At this point the transmitter becomes uninhibited. Figure 9 illustrates jabber timing.

AUI Selection/Under Voltage Lockout

The transmit and receive squelch circuits of the NE83Q92 remain active if the absolute value of V_{EE} is less than the threshold for under voltage lockout, V_{UVL}. This prevents glitches from appearing on either the AUI or coaxial cable during power up and power down.

There is no collision announcement during power up and the transceiver waits for 400ms before becoming enabled.

If RXI is disconnected from the coaxial cable after power up, its voltage will fall towards

V_{EE}. If the absolute value of this voltage exceeds the AUI disable voltage, V_{DIS}, for longer than 800ms, the transmit and receive squelch circuits remain active and, in addition, the AUI drivers become high impedance. This permits AUI connections to be hard wired together, e.g., the coaxial transceiver and a 10BASE-T transceiver, with the signal path determined by which transceiver is connected to its external cable.

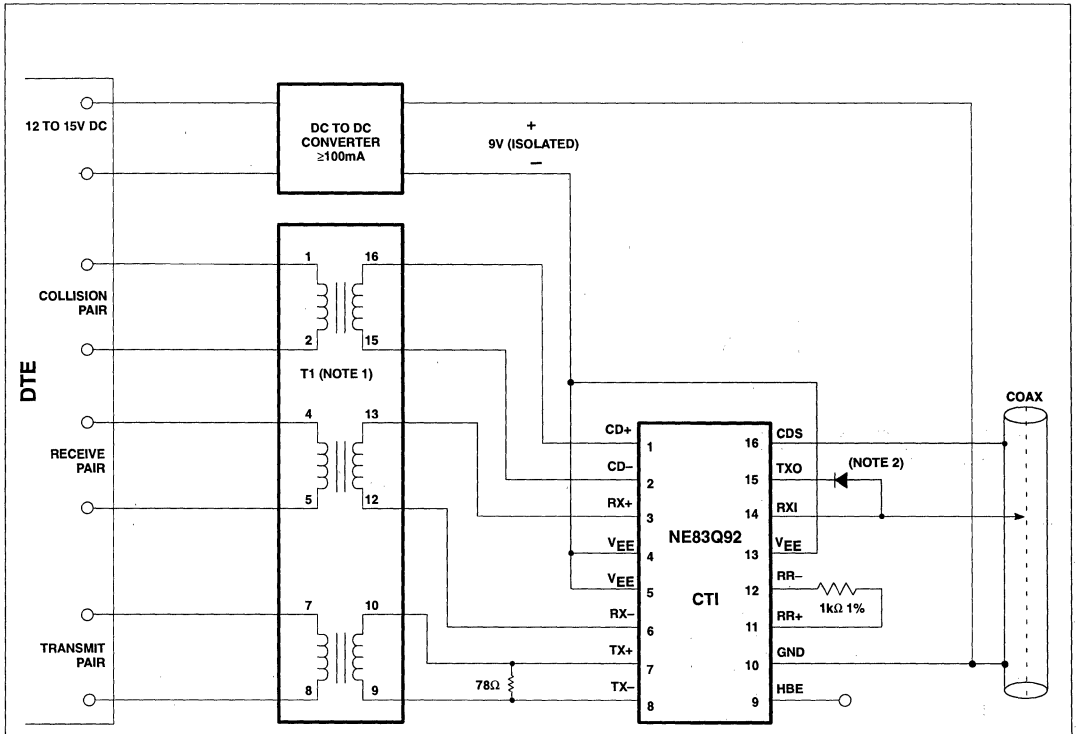
There is no collision announcement on disconnecting RXI, but there is a 400ms announcement on re-connection before the transceiver is enabled.

Detection of Coaxial Cable Faults

In the NE83Q92 there is no internal loopback path from the TX inputs to the RX outputs. This means that, when the local DTE is transmitting, the signal will only be present at the receiver outputs RX+ and RX– if it appears on the coaxial cable and is larger than the receiver squelch threshold V_{RS}. If a short circuit fault condition occurs at the cable connector to the CTI, then no signal will appear at the receiver outputs.

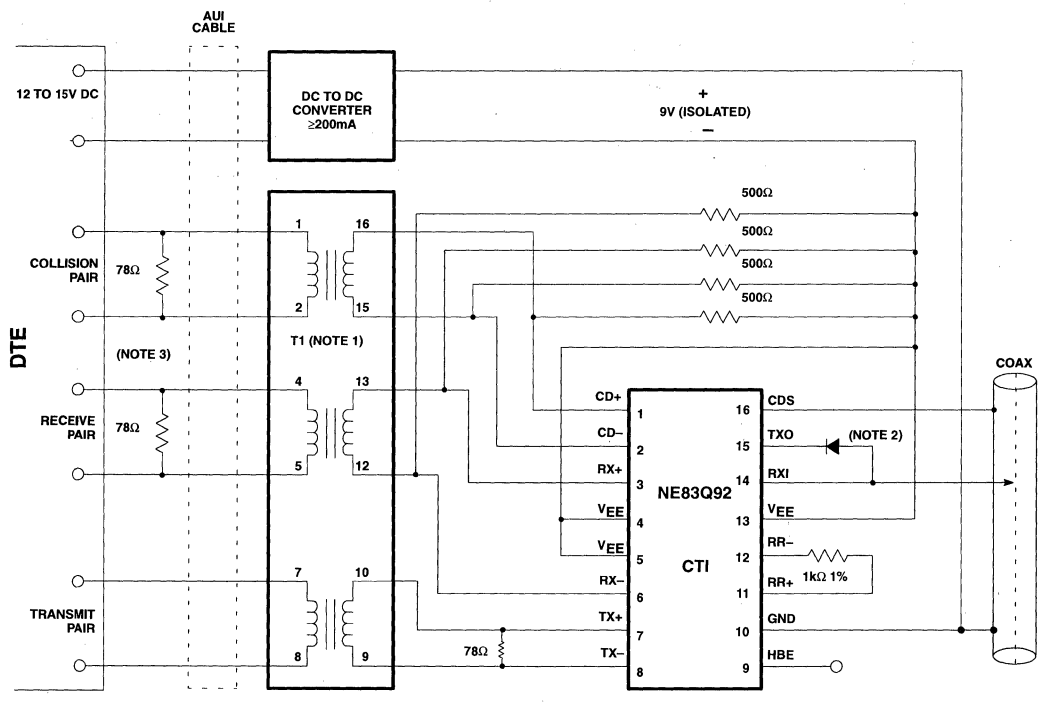
In the case of an open circuit at the coaxial cable connector there will also be no signal at the receiver outputs due to the AUI disabling mode of the NE83Q92. However, a heartbeat signal will be present following a transmission attempt for the short circuit condition, but not for the open circuit.

A coaxial cable with only a single 50Ω termination will generate a collision not only at every transmission attempt, but also for every reception attempt due to the receive mode collision detection of the NE83Q92.



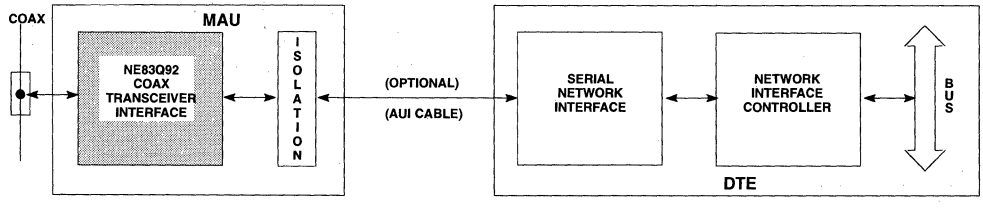
NOTES:
1. T1 is a 1:1 pulse transformer, with an inductance of 30 to 100μH.
2. IN916 or equivalent for Ethernet, not required for Thin Ethernet.

Figure 1. Connection Diagram for Minimum Current Consumption



NOTES:
1. T1 is a 1:1 pulse transformer, with an inductance of 30 to 100μH.
2. IN916 or equivalent for Ethernet, not required for Thin Ethernet.
3. 78Ω resistors not required if AUI cable not present.

Figure 2. Connection Diagram for Standard 8392 Applications



MAU = Medium Attachment Unit
AUI Cable = Attachment Unit Interface Cable (not used in Thin Ethernet applications)

Figure 3. Interface Diagram for Ethernet/Thin Ethernet Local Area Network

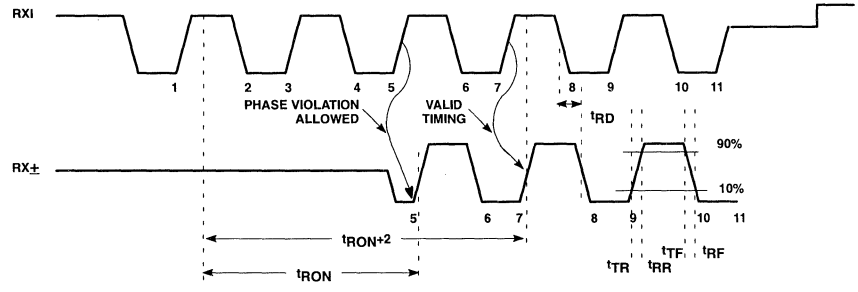


Figure 4. Receiver Timing

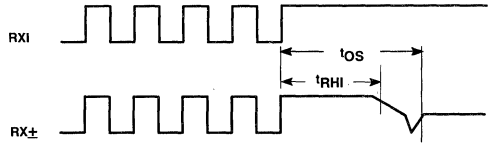


Figure 5. Receiver End–of–Packet Timing

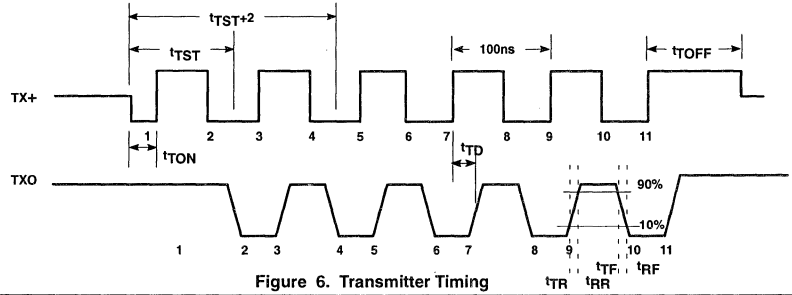


Figure 6. Transmitter Timing

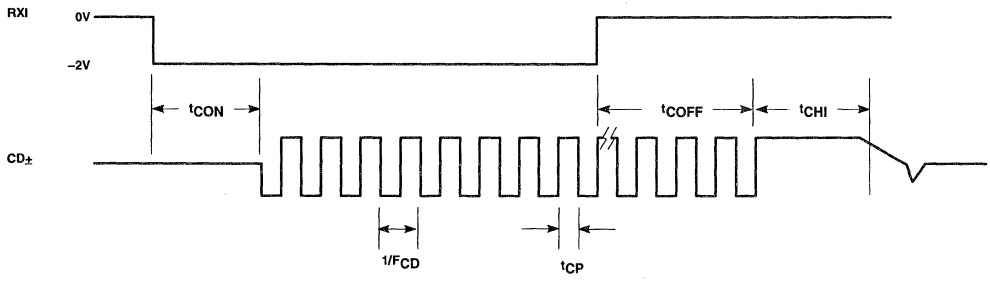


Figure 7. Collision Timing

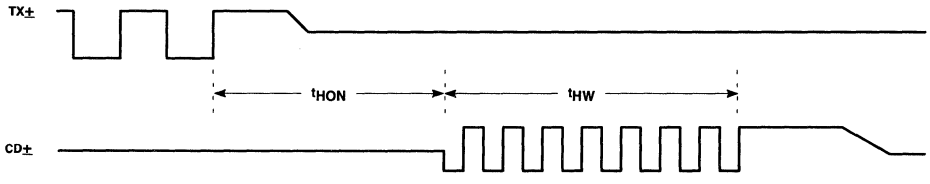


Figure 8. Heartbeat Timing

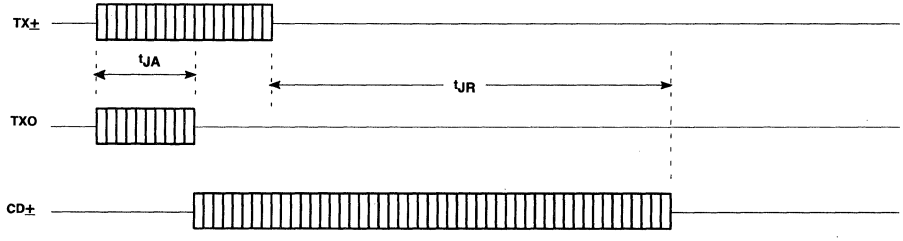


Figure 9. Jabber Timing

Enhanced coaxial Ethernet transceiver — NE83Q93

DESCRIPTION

The NE83Q93 is a low power coaxial transceiver interface (CTI) for Ethernet (10base5) and Thin Ethernet (10base2) local area networks. The CTI is connected between the coaxial cable and the Data Terminal Equipment (DTE) and consists of a receiver, transmitter, collision detector, heartbeat generator and jabber timer (see Block Diagram). The transmitter output connects directly to a doubly terminated 50Ω cable, while the receiver output, collision detector output and transmitter input are connected to the DTE through isolation transformers. Isolation between the CTI and the DTE is an IEEE 802.3 requirement that can be met on signal lines by using a set of pulse transformers normally available in a standard 16-pin DIP. Power isolation for the CTI is achieved using DC-to-DC conversion through a power transformer (see Figure 1, Connection Diagram).

The part is fully pin compatible with the industry standard 8392A, but has substantially lower current consumption, is fully compliant with the IEEE802.3 standard, and has additional features such as a low current standby mode with automatic selection between AUI and coaxial connections, extended mode collision default, a transmit enable input, a carrier detect output and five status LED driver outputs.

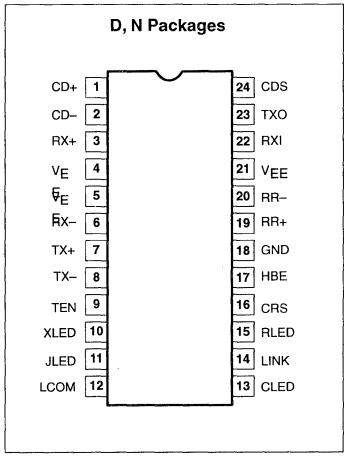
The NE83Q93 is manufactured on an advanced BiCMOS process and is ideally suited to lap-top personal computers or systems where low power consumption and no changing of board jumper positions is required.

FEATURES

- Fully compliant with Ethernet II, IEEE 802.3 10BASE-5 and 10BASE-2, and ISO 8802/3 interface specifications
- Functionally compatible with industry standard 8392 applications
- Lowest overall current consumption allows operation using 1 Watt DC-DC converter
- Lowest power configuration provides reduced external parts count
- High efficiency AUI drivers minimize current consumption under idle conditions
- Automatically enters standby mode when no coaxial cable is connected
- Standby mode allows automatic selection between AUI and Coaxial connections when no coaxial cable is connected
- Smart squelch on data inputs eliminates false activations
- Transmit enable input and carrier sense output for repeater applications
- Five LED status drivers for transmit, receive, collision, jabber and link fail indication
- Advanced BiCMOS process for extremely low power operation
- Available in 24-pin DIP and 24-pin SOL packages

PIN CONFIGURATION

D, N Packages



ORDERING INFORMATION

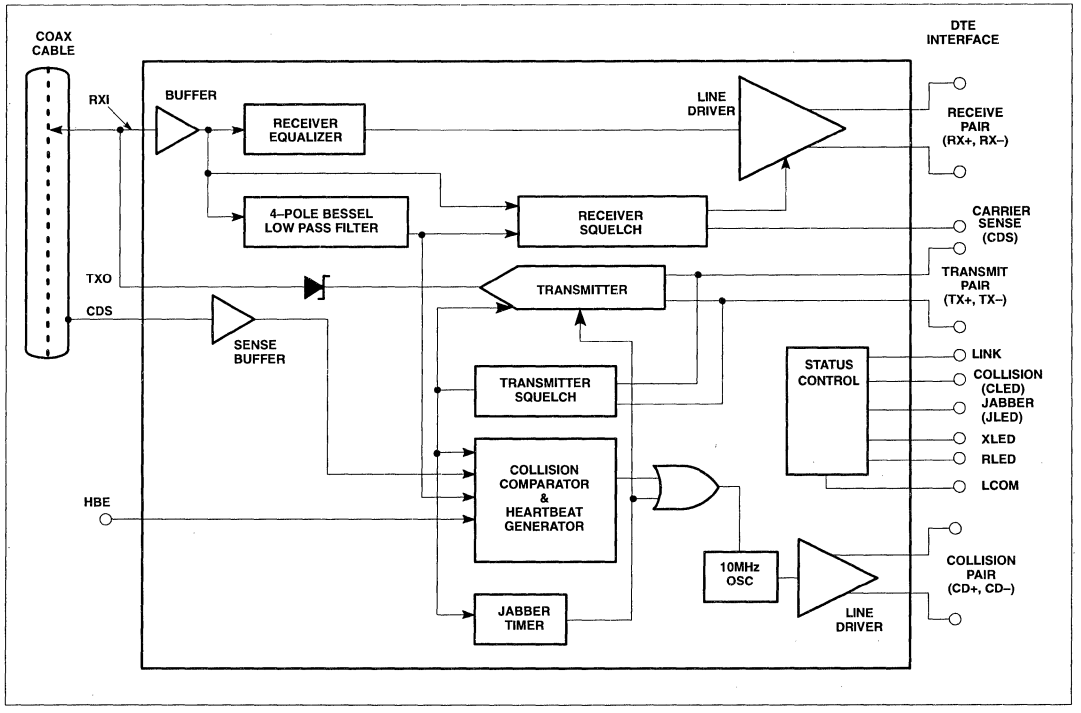
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
24-Pin Plastic Dual In-Line Package	0 to +70°C	NE83Q93N	0410A
24-Pin Plastic Small Outline Large	0 to +70°C	NE83Q93D	0173D

PIN DESCRIPTIONS

PIN NO. D, N PKG	SYMBOL	DESCRIPTION
1 2	CD+ CD–	**Collision Outputs.** Balanced differential line driver outputs which send a 10MHz signal to the DTE in the event of a collision, jabber interrupt or heartbeat test.
3 6	RX+ RX–	**Receiver Outputs.** Balanced differential line driver outputs which send the received signal to the DTE.
7 8	TX+ TX–	**Transmitter Inputs.** Balanced differential line receiver inputs which accept the transmission signal from the DTE and apply it to the coaxial cable at TXO.
9	TEN	**Transmit Enable.** A CMOS compatible input requiring an input voltage range of V_{EE} to V_{EE} + 5V. The transmitter and loopback functions are disabled when TEN is LOW and enabled when TEN is HIGH or left floating. TEN is normally driven through an opto-coupler.
10	XLED	**Transmit Indicator.** Indicates a packet is being transmitted onto the coaxial cable.
11	JLED	**Jabber Indicator.** Indicates that the jabber timer has timed out and the coaxial driver is disabled.
12	LCOM	**LED Common.** The anodes of all status indicator LEDs are connected to this pin. It's voltage is V_{EE} + 5V.
13	CLED	**Collision Indicator.** Indicates that a collision has been detected.
14	LINK	**Link Indicator.** Indicates that a connection is present to the coaxial cable network.
15	RLED	**Receive Indicator.** Indicates that a packet is being received from the coaxial cable.
16	CRS	**Carrier Sense.** A real time output that indicates the presence of a carrier on the coaxial cable. CRS is normally used to drive an opto-coupler.
17	HBE	**Heartbeat Enable.** The heartbeat function is disabled when this pin is connected to V_{EE} and enabled when connected to GND or left floating.
11 12	RR+ RR–	**External Resistor.** A 1kΩ (1%) resistor connected between these pins establishes the signaling current at TXO.
22	RXI	**Receiver Input.** This pin is connected directly to the coaxial cable. Received signals are equalized, amplified, and sent to the DTE through the RX± pins.
23	TXO	**Transmitter Output.** This pin is connected directly (Thin Ethernet) or through an external isolating diode (Ethernet) to the coaxial cable.
24	CDS	**Collision Detect Sense.** Ground sense connection for the collision detection circuitry. This pin should be connected directly to the coaxial cable shield for standard Ethernet operation. Leaving CDS unconnected will default the collision threshold to extended mode thin Ethernet operation.
18	GND	**Positive Supply Pin.**
4 5 21	V_{EE}	**Negative supply pins.**

NOTE:
1. The IEEE 802.3 name for CD is CI; for RX is DI; for TX is DO.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage[1]	–12	V
V_{IN}	Voltage at any input[1]	0 to –12	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec.)	+300	°C
T_J	Recommended max junction temperature[2]	+150	°C
θ_{JA}	Thermal impedance (N and A packages)	60	°C/W

NOTE:
1. 100% measured in production.
2. The junction temperature is calculated from the following expression:

$$T_J = T_A + \theta_{JA}[V_{EE} \times 0.015 \times n_{IDL}) + [V_{EE} \times 0.033 \times n_{RX}) + [V_{EE} \times 0.075 \times n_{TX})$$

where

T_A = Ambient temperature in °C.
θ_{JA} = Thermal resistance of package.
V_{EE} = Normal operating supply voltage in volts.
n_{IDL} = Percentage of duty cycle idle
n_{RX} = Percentage of duty cycle receiving
n_{TX} = Percentage of duty cycle transmitting

ELECTRICAL CHARACTERISTICS

V_{EE} = –9V ±6%; T_A = 0°C to +70°C unless otherwise specified[1,2]. No external isolation.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{UVL}	Under voltage lockout. Transceiver disabled for $\|V_{EE}\| < \|V_{UVL}\|$			–7.5		V
I_{EE}	Supply current idle			–15	–20	mA
	Supply current transmitting	No LED loads		–60	–85	mA
I_{RXI}	Receive input bias current	V_{RXI} = 0V	–2		+25	µA
I_{CDS}	Cable sense input bias current	V_{CDS} = 0V		+1	+3	µA
V_{IH}	HBE input HIGH voltage		V_{EE} +2.4			V
V_{IL}	HBE input LOW voltage				V_{EE} +1.6	V
I_{IH}	HBE input HIGH current	V_{HBE} = 0V			+10	µA
I_{IL}	HBE input LOW current	V_{HBE} = V_{EE}	–20			µA
V_{TENH}	Input HIGH voltage at TEN			V_{EE} + 2		V
V_{TENL}	Input LOW voltage at TEN			V_{EE} + 1		V
I_{TENL}	Input LOW current at TEN		–50		–100	µA
I_{TDC}	Transmit output DC current level[3]		–37		–45	mA
I_{TAC}	Transmit output AC current level[3]		±28		±I_{TDC}	mA
I_{TX10}	Transmit current	V_{TXO} = –10V	–250		+250	µA
V_{TCOM}	Transmitter output voltage compliance[4]				–3.7	V
V_{CD}	Collision threshold[5]	Measured by applying DC voltage at RXI (CDS = 0V)	–1450	–1530	–1580	mV
V_{DIS}	AUI disable voltage at RXI	Measured as DC voltage at RXI		–3.5		V
V_{OD}	Differential output voltage – non idle at RX± and CD±[6]		±600		±1100	mV
V_{OB}	Differential output voltage imbalance – idle at RX± and CD±[7]				±40	mV
V_{OC}	Output common mode voltage at RX± and CD±	RXI = 0V	–4.5	–5.5	–6.5	V
V_{RS}	Receiver squelch threshold	V_{RXI} average DC (CDS = 0V)	–150	–250	–350	mV
V_{TS}	Transmitter squelch threshold	(V_{TX+} – V_{TX-}) peak	–175	–225	–275	mV
R_{RXI}	Shunt resistance at RXI non–transmitting		100			kΩ
C_{RXI}	Input capacitance at RXI			1	2	pF
R_{TXO}	Shunt resistance at TXO transmitting		7.5	10		kΩ
R_{AUIZ}	Differential impedance at RX± and CD± with no coaxial cable connected			3		kΩ
R_{TX}	Differential impedance at TX±			20		kΩ
LED driver and CRS output						
V_{OL}	Output LOW voltage	I_{OUT} = 8mA			V_{EE} +1.4	V
I_{OL}	Output leakage current inactive	$V_{EE} < V_{OUT} < V_{EE}$ + 5			10	µA

NOTES:

1. Currents flowing into device pins are positive. All voltages are referenced to ground unless otherwise specified. For ease of interpretation, the parameter limit that appears in the MAX column is the largest value of the parameter, irrespective of sign. Similarly, the value in the MIN column is the smallest value of the parameter, irrespective of sign.
2. All typicals are for V_{EE} = –9V and T_A = 27°C.
3. I_{TDC} is measured as (V_{MAX} + V_{MIN})/(2 x 25) where V_{MAX} and V_{MIN} are the max and min voltages at TXO with a 25Ω load between TXO and GND. I_{TAC} is measured as (V_{MAX} – V_{MIN})/(2 x 25).
4. The TXO pin shall continue to sink at least I_{TDC} min when the idle (no signal) voltage on this pin is –3.7V.
5. Collision threshold for an AC signal is within 5% of V_{CD}.
6. Measured on secondary side of isolation transformer (see Connection Diagram, Figure 1). The transformer has a 1:1 turns ratio with an inductance between 30 and 100µH at 5MHz.
7. Measured as the voltage difference between the RX pins or the CD pins with the transformer removed.

TIMING CHARACTERISTICS

V_{EE} = –9V ±6%; T_A = 0 to 70°C, unless otherwise specified[1]. No external isolation diode on TXO.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{RON}	Receiver start up delay RXI to RX± (Figure 4) First received bit on RX±	V_{RXI} = –2V peak		3	5	bits
	First validly timed bit on RX±				t_{RON} +2	bits
t_{RD}	Receiver prop. delay RXI to RX±	V_{RXI} = –2V peak		20	50	ns
t_{RR}	Differential output rise time on RX± and CD±[2,3]			5	7	ns
t_{RF}	Differential output fall time on RX± and C±[2,3]			5	7	ns
t_{OS}	Differential output settling time on RX± and CD± to V_{OB} = 40mV[2] (see Figure 5)			1		µs
t_{RJ}	Receiver and cable total jitter			±2	±6	ns
t_{RHI}	Receiver high to idle time	Measured to +210mV	200		850	ns
t_{RM}	Rise and fall time matching on RX± and CD±	$t_{RF} - t_{RR}$		0.4	±2	ns
t_{TST}	Transmitter start–up delay TX± to TXO (Fig. 6) First transmitted bit on TXO	$V_{TX±}$ = –1V peak		1	2	bits
	First validly timed bit				t_{TST} + 2	bits
t_{TD}	Transmitter prop delay TX± to TXO (see Figure 6)	$V_{TX±}$ = 1V peak	5	20	50	ns
t_{TR}	Transmitter rise time 10% to 90% (see Figure 6)		20	25	30	ns
t_{TF}	Transmitter fall time 10% to 90% (see Figure 6)		20	25	30	ns
t_{TM}	$t_{TF} - t_{TR}$ mismatch				±2	ns
t_{TS}	Transmitter added skew[4]				±2	ns
t_{TON}	Transmitter turn on pulse width (see Figure 6)	$V_{TX±}$ = 1V peak	10		35	ns
t_{TOFF}	Transmitter turn off pulse width (see Figure 6)	$V_{TX±}$ = 1V peak	125		225	ns
t_{CON}	Collision turn on delay (see Figure 7)	0V to –2V step at RXI			13	bits
t_{COFF}	Collision turn off delay (see Figure 7)	–2V to 0V step at RXI			16	bits
t_{CHI}	Collision high to idle time (see Figure 7)	Measured to +210mV	200		850	ns
f_{CD}	Collision frequency (see Figure 7)		8.5	10	11.5	MHz
t_{CP}	Collision signal pulse width (see Figure 7)		35		70	ns
t_{HON}	Heartbeat turn on delay (see Figure 8)		0.6		1.6	µs
t_{HW}	Heartbeat test duration (see Figure 8)		0.5		1.5	µs
t_{JA}	Jabber activation delay measured from TX± to CD± (see Figure 9)		20		60	ms
t_{JR}	Jabber reset delay measured from TX± to CD± (see Figure 9)		250		650	ms
LEDs						
t_{LED}	Turn-on or turn-off delay of LEDs				10	µs
t_{XLEDON}	XLED maximum on time		90	115	135	ms
$t_{XLEDOFF}$	XLED minimum off time		5	7	10	ms
t_{RLEDON}	RLED maximum on time		90	115	135	ms
$t_{RLEDOFF}$	RLED minimum off time		5		10	ms
t_{CLEDON}	CLED minimum on time		10	14	18	ms
t_{JLEDON}	JLED maximum on time	ON while jabber active				
$t_{JLEDOFF}$	JLED minimum off time	OFF while jabber inactive				

NOTES:
1. All typicals are for V_{EE} = –9V and T_A = 27°C.
2. Measured on secondary side of isolation transformer (see Figures 1 and 2, Connection Diagram). The transformer has a 1:1 turn ratio with an inductance between 30 and 100µH at 5MHz.
3. The rise and fall times are measured as the time required for the differential voltage to change from –225mV to +225mV, or +225mV to –225mV, respectively.
4. Difference in propagation delay between rising and falling edges at TXO.

FUNCTIONAL DESCRIPTION

The NE83Q93 is a low power coaxial Ethernet transceiver which complies with the IEEE 802.3 specification and offers a number of additional features. These features are:

a. Low current consumption of typically 15mA when idle and 80mA with full traffic (transmitting and colliding) allows smaller DC-DC converter to be used for the isolated power supply.

b. Automatic selection between AUI cable and coaxial connections by placing the AUI outputs in a high impedance state when the coaxial cable is disconnected. This eliminates the need for changing a jumper position on the Ethernet board when selecting either Thin Ethernet or remote transceiver connections.

c. High efficiency AUI drivers for the RX± and CD± ports which automatically power down when idle. The NE83Q93 requires no external pull-down resistors on these ports, but will still operate if they are present.

d. Transmit enable input and carrier sense output for direct use in repeater appliications.

e. LED control circuitry and drivers for indicating the transmit, receive, collision, jabber and link status of the NE83Q93.

Receiver Functions

The receiver consists of an input buffer, a cable equalizer, a 4-pole Bessel low pass filter, a squelch circuit and a differential line driver.

The buffer provides high input resistance and low input capacitance to minimize loading and reflections on the coaxial cable.

The equalizer is a high pass filter that compensates for the low pass effect of the coaxial cable and results in a flatband response over all signal frequencies to minimize signal distortion.

The 4-pole Bessel low pass filter extracts the average DC voltage level on the coaxial cable for use by the receiver squelch and collision detection circuits.

The receiver squelch circuit prevents noise on the coaxial cable from falsely triggering the receiver in the absence of a true signal. At the beginning of a packet, the receiver turns on when the DC level from the low pass filter exceeds the DC squelch threshold and the received packet has started with a 01 bit sequence with acceptable timing parameters. For normal signal levels this will take less than 500ns, or 5 bits. However, at the end of a packet, a fast receiver turn off is needed to reject both dribble bits on the coaxial cable and spurious responses due to settling of the on-chip bandpass filter. This is accomplished by an AC timing circuit that disables the receiver if the signal level on the coaxial cable remains high for typically 250ns and only enables the receiver again after approximately .5µs. Figures 4 and 5 illustrate receiver timing.

The differential line driver provides typically ±900mV signals to the DTE with less than 7ns rise and fall times. When in idle state (no received signal) its outputs provide <20mV differential voltage offset to minimize DC standing current in the isolation transformer. The line driver outputs (RX± and CD±) require no external pull-down resistors and will drive a 78Ω transmission line directly. They automatically power down under idle conditions and are powered up when a receive signal is detected. The drivers will still operate with external resistors present so can be retro-fitted into existing 8392A boards. However, an extra current of 7mA/output (for 500Ω resistors) would be generated by these resistors irrespective of whether the transceiver is idle or responding to traffic.

Transmitter Functions

The transmitter has differential inputs and an open collector current driver output. The differential input common mode voltage is established by the CTI and should not be altered by external circuitry. Controlled rise and fall times of 25ns (±5ns) minimize higher harmonic components in the transmitted spectrum, while matching of these rise and fall times to typically 2ns minimizes signal jitter. The drive current levels of the CTI are set by an on-chip bandgap voltage reference and an external 1% resistor. An on-chip isolation diode is provided to reduce the transmitter's coaxial cable load capacitance. For Thin Ethernet applications, no further external isolation diode is required, since the NE83Q93 meets the capacitive loading specifications. For Ethernet applications a further external diode should be added to reduce loading capacitance.

The transmitter squelch circuit ensures that the transmitter can only be enabled if the transmitted packet begins with a 01 bit sequence where the negative-going differential signals are typically greater than 225mV in magnitude and 25ns in duration.

The transmitter will be disabled at the end of a packet if there are no negative going signals of greater than 225mV for more than typically 150ns. Figure 6 illustrates transmitter timing.

Collision Functions

The collision detection scheme implemented in the NE83Q93 is receive mode detection, which detects a collision between any two stations on the network with certainty at all times, irrespective of whether or not the local DTE is producing one of the colliding signals. This is the only detection scheme allowed by the IEEE 802.3 standard for both repeater and non-repeater nodes.

The collision circuitry consists of the 4-pole Bessel low pass filter, a comparator, a precision voltage reference that sets up the collision threshold, a heartbeat generator, a 10MHz oscillator, and a differential line driver.

The collision comparator monitors the DC level at the output of the low pass filter and enables the line driver if it is more negative than the collision threshold. A collision condition is indicated to the DTE by a 10MHz oscillation signal at the CD outputs and typically occurs within 700ns of the onset of the collision. The collision signal begins with a negative-going pulse and ends with a continuous high-to-idle state longer than 170ns. Figure 7 illustrates collision timing.

At the end of every transmission, the heartbeat generator creates a pseudo collision to ensure that the collision circuitry is properly functioning. This pseudo collision consists of a 1µs burst of 10MHz oscillation at the line driver outputs approximately 1µs after the end of the transmission. The heartbeat function can be disabled externally by connecting the HBE (heartbeat enable) to V_{EE}. This allows the CTI to be used in repeater applications. Figure 8 illustrates heartbeat timing.

As with the receiver AUI drivers, the CD± outputs require no external pull-down resistors, although they still operate if the resistors are present, and automatically power down under idle conditions.

Jabber Functions

The jabber timer monitors the transmitter and inhibits transmission if it is active for longer than typically 30ms. The jabber circuit then enables the collision outputs for the remainder of the data packet and for typically 450ns (unjab time) after it has ended. At this point the transmitter becomes uninhibited. Figure 9 illustrates jabber timing.

Control Interface Signals

The NE83Q93 provides two input and one output signal for mode control and interfacing within repeaters. The output signal is Carrier Sense (CRS) and the input signals are

Heartbeat Enable (HBE) and Transmit Enable (TEN).

The HBE input controls the transmission of the heartbeat (or SQE) signal to the DTE for testing the collision detection function. It is normally hardwired to V_{EE} or GND.

a. The heartbeat (SQE) function is DISABLED when HBE is connected to V_{EE}

b. The heartbeat (SQE) function is ENABLED when HBE is connected to GND or left floating

The TEN input controls the coaxial transmitter. It is a CMOS compatible input requiring a driving signal with a voltage range of V_{EE} to V_{EE} + 5V. It is normally driven through an opto-coupler to provide electrical isolation. A typical application circuit is shown in Figure [].

a. The coaxial transmitter is DISABLED when a LOW is applied to TEN or it is directly connected to V_{EE}. Since the loopback function of the NE83Q93 occurs through the coaxial connection the loopback function is also disabled.

b. The coaxial transmitter is ENABLED when a HIGH is applied to TEN or it is directly connected to GND or left floating.

The CRS output indicates the presence of a carrier signal on the coaxial cable. It is open drain output designed to drive the LED of an opto-coupler connected between CRS and LCOM through a current limiting series resistor. A LOW at CRS is V_{EE} and a HIGH is the voltage at LCOM (V_{EE} + 5V).

a. CRS is HIGH (no current) when no carrier is present

b. CRS is LOW (current sinking) when carrier is present

On applying a HIGH to TEN through an opto-coupler the transmitter is enabled after it has then recognized the normal squelch deactivation conditions of a 01 bit sequence and negative-going differential signals meeting the necessary magnitude and duration requirements. The set-up time needed from application of a HIGH at TEN to recognizing the first 01 bit sequence is typically 25ns. The propagation delay through an opto-coupler is of the order of 200ns.

AUI Selection/Under Voltage Lockout

The transmit and receive squelch circuits of the NE83Q93 remain active if the absolute value of V_{EE} is less than the threshold for under voltage lockout, V_{UVL}. This prevents glitches from appearing on either the AUI or coaxial cable during power up and power down.

There is no collision announcement during power up and the transceiver waits for 400ms before becoming enabled.

If RXI is disconnected from the coaxial cable after power up, its voltage will fall towards V_{EE}. If the absolute value of this voltage exceeds the AUI disable voltage, V_{DIS}, for longer than 800ms, the transmit and receive squelch circuits remain active and, in addition, the AUI drivers become high impedance. This permits AUI connections to be hard wired together, e.g., the coaxial transceiver and a 10BASE-T transceiver, with the signal path determined by which transceiver is connected to its external cable.

There is no collision announcement on disconnecting RXI, but there is a 400ms announcement on re-connection before the transceiver is enabled.

Detection of Coaxial Cable Faults

In the NE83Q93 there is no internal loopback path from the TX inputs to the RX outputs. This means that, when the local DTE is transmitting, the signal will only be present at the receiver outputs RX+ and RX– if it appears on the coaxial cable and is larger than the receiver squelch threshold V_{RS}. If a short circuit fault condition occurs at the cable connector to the CTI, then no signal will appear at the receiver outputs.

In the case of an open circuit at the coaxial cable connector there will also be no signal at the receiver outputs due to the AUI disabling mode of the NE83Q93. However, a heartbeat signal will be present following a transmission attempt for the short circuit condition, but not for the open circuit.

A coaxial cable with only a single 50Ω termination will generate a collision not only at every transmission attempt, but also for every reception attempt due to the receive mode collision detection of the NE83Q93.

Status Indicator Functions

The NE83Q93 provides five status outputs, the open drain device connected to each is capable of directly driving an LED or opto-coupler, or other logic circuits if an external pull-up resistor is used. The functional descriptions below are for an LED connected between the output and LCOM (V_{EE} + 5V) through a current limiting series resistor.

The LINK signal indicates the status of the coaxial connection.

- The LED is ON when the transceiver is connected to a properly terminated coaxial cable.
- The LED is OFF when the coaxial cable is disconnected from the transceiver, or if the coaxial connection is unterminated.

The XLED signal indicates the status of the transmitter.

- The LED is OFF when there is no transmission in progress
- The LED is turned ON when data is being transmitted and remains ON for typically 115ms.

The RLED signal indicates the status of the receiver.

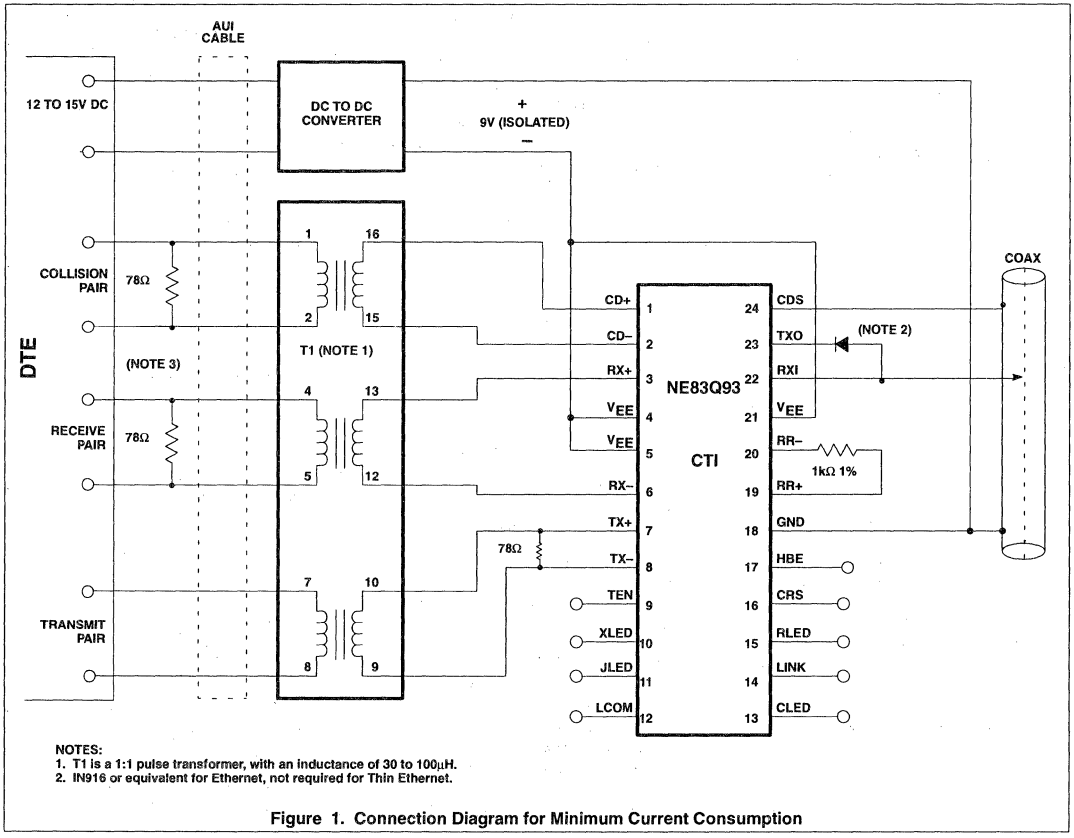
- The LED is OFF when no signal is being received.
- The LED is turned ON when data is received and remains ON for typically 115ms.

The CLED signal indicates the status of the collision detection circuit.

- The LED is OFF for no collision.
- The LED turns ON when a collision is detected and remains ON for typically 12ms after the end of the collision.
- In the event of another collision during the latter 6ms of the 12 ms delay period after the end of the last collision, the LED will turn off for typically 6ms then back ON to indicate the new collision.

The JLED signal indicates the status of the jabber control circuit.

- The LED is OFF for a no-jab condition.
- The LED turns ON when the coaxial transmitter output is jabbed.
- The LED turns back off when the transmitter is unjabbed.



NOTES:
1. T1 is a 1:1 pulse transformer, with an inductance of 30 to 100μH.
2. IN916 or equivalent for Ethernet, not required for Thin Ethernet.

Figure 1. Connection Diagram for Minimum Current Consumption

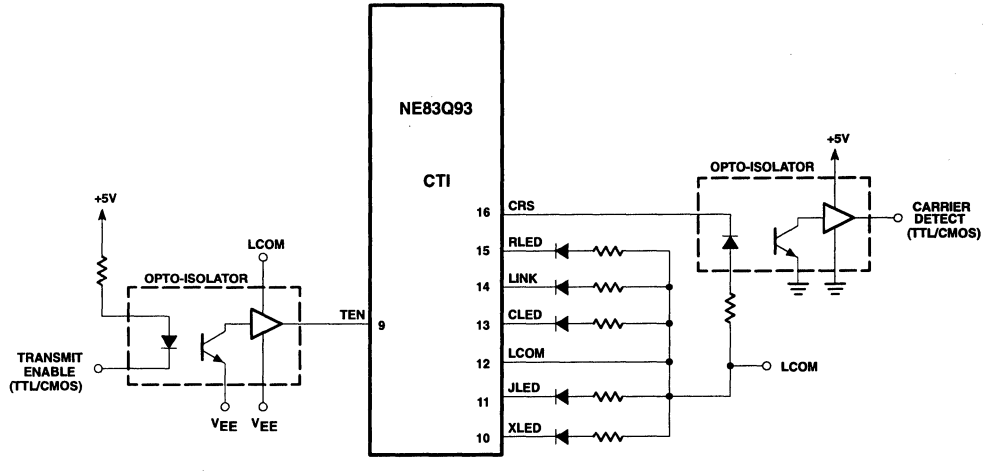
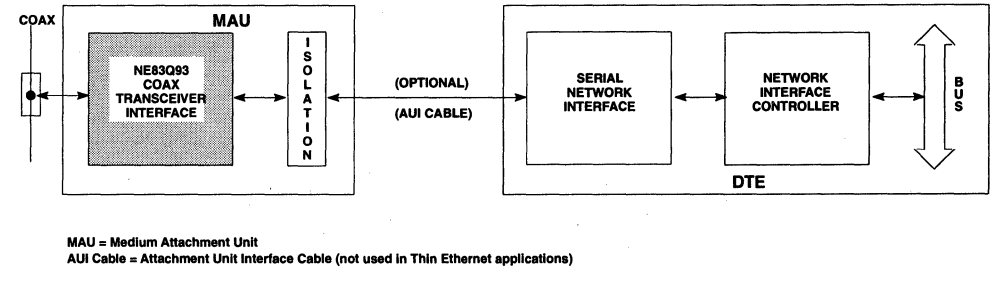


Figure 2. Control Interface Connectors



MAU = Medium Attachment Unit
AUI Cable = Attachment Unit Interface Cable (not used in Thin Ethernet applications)

Figure 3. Interface Diagram for Ethernet/Thin Ethernet Local Area Network

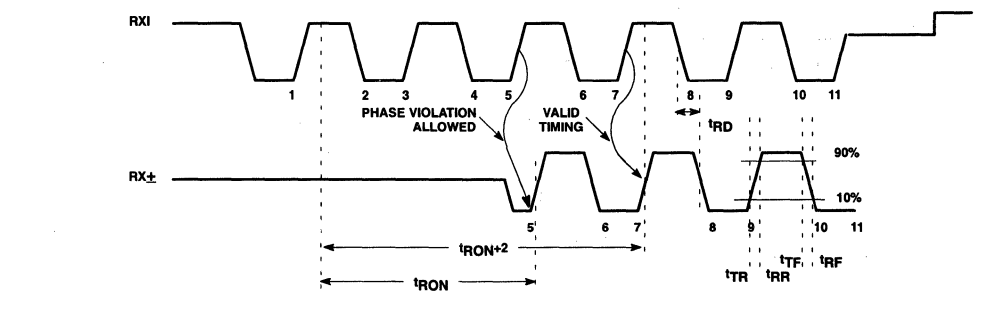


Figure 4. Receiver Timing

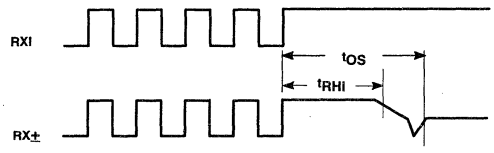


Figure 5. Receiver End–of–Packet Timing

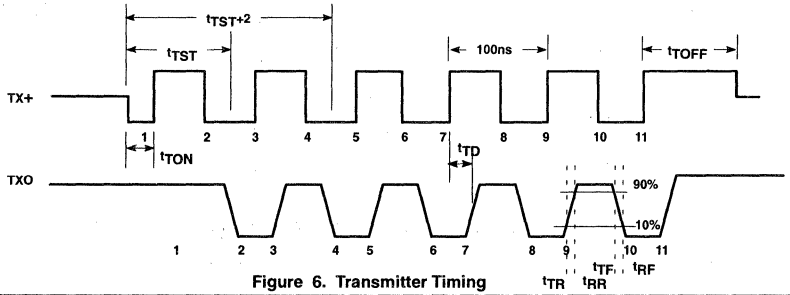


Figure 6. Transmitter Timing

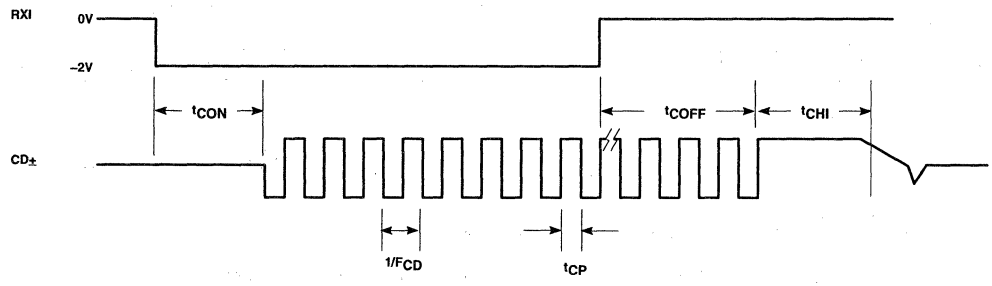


Figure 7. Collision Timing

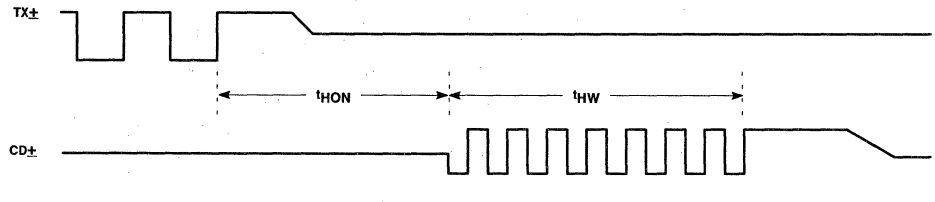


Figure 8. Heartbeat Timing

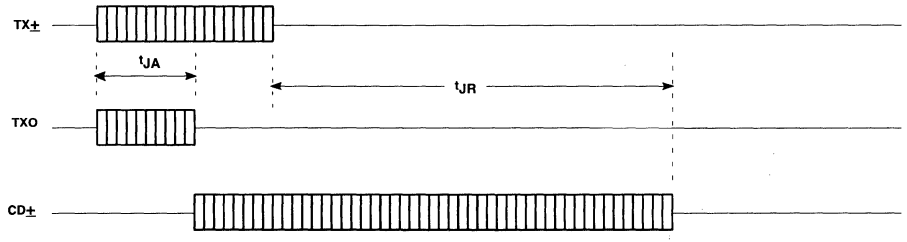


Figure 9. Jabber Timing

Low-power coaxial Ethernet transceiver — NE83C92

DESCRIPTION

The NE83C92 is a low power coaxial transceiver interface (CTI) for Ethernet (10base5) and Thin Ethernet (10base2) local area networks. The CTI is connected between the coaxial cable and the Data Terminal Equipment (DTE) and consists of a receiver, transmitter, collision detector, heartbeat generator and jabber timer (see Block Diagram). The transmitter output connects directly to a doubly terminated 50Ω cable, while the receiver output, collision detector output and transmitter input are connected to the DTE through isolation transformers. Isolation between the CTI and the DTE is an IEEE 802.3 requirement that can be met on signal lines by using a set of pulse transformers normally available in a standard 16-pin DIP. Power isolation for the CTI is achieved using DC-to-DC conversion through a power transformer.

The part is fully pin compatible with the industry standard 8392A, but has substantially lower current consumption, is fully compliant with the IEEE802.3 standard, and has additional features such as a low current standby mode with automatic selection between AUI and coaxial connections, and extended mode collision default.

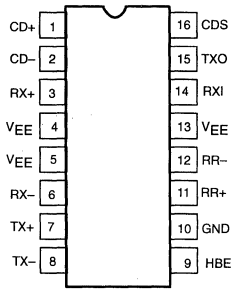
The NE83C92 is manufactured on an advanced BiCMOS process and is ideally suited to lap-top personal computers or systems where low power consumption and no changing of board jumper positions is required.

FEATURES

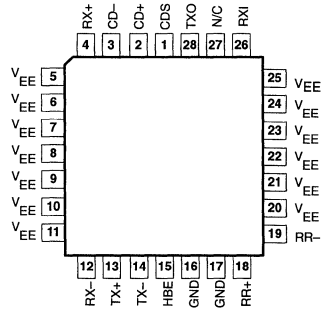
- Fully compliant with Ethernet II, IEEE 802.3 10BASE-5 and 10BASE-2, and ISO 8802/3 interface specifications
- 100% drop-in compatible with industry standard 8392 sockets
- Lowest overall current consumption
- High efficiency AUI drivers minimize current consumption under idle conditions
- Smart squelch on data inputs eliminates false activations
- Advanced BiCMOS process for extremely low power operation
- Available in 16-pin DIP and 28-pin PLCC
- Expanded version (NE83Q93) available for repeater and advanced system applications

PIN CONFIGURATION

D, N Packages



A PACKAGE



ORDERING INFORMATION

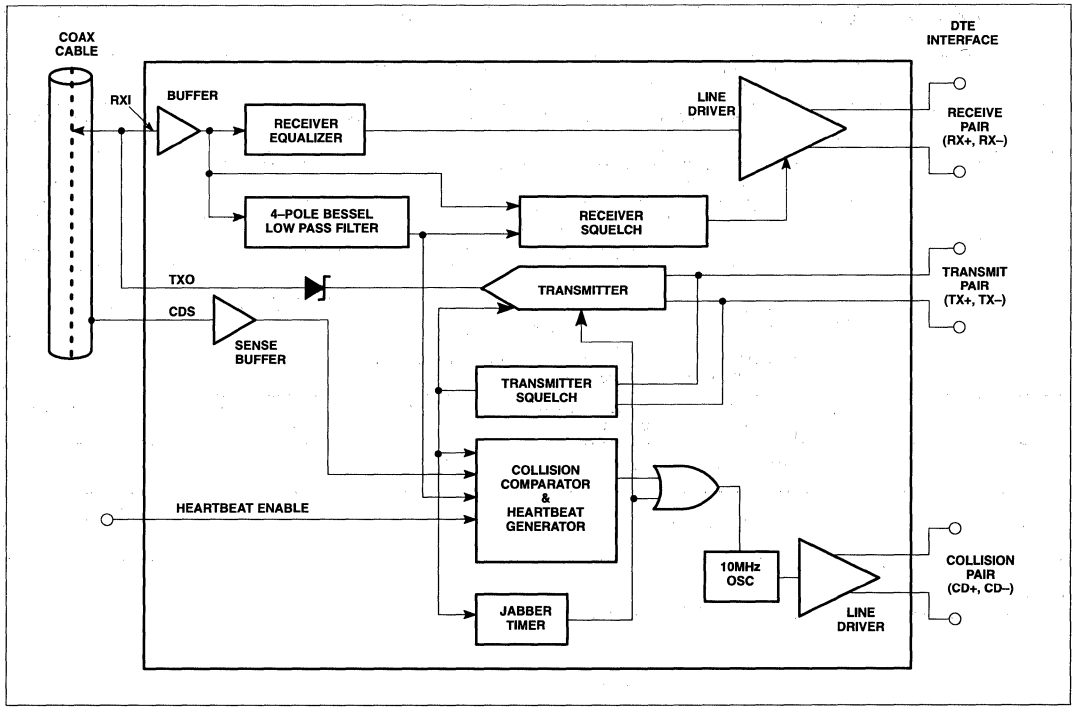
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package	0 to +70°C	NE83C92N	0406C
28-Pin Plastic Leaded Chip Carrier	0 to +70°C	NE83C92A	0401F

PIN DESCRIPTIONS

PIN NO. N PKG	PIN NO. PLCC	SYMBOL	DESCRIPTION
1 2	2 3	CD+ CD–	**Collision Outputs.** Balanced differential line driver outputs which send a 10MHz signal to the DTE in the event of a collision, jabber interrupt or heartbeat test.
3 6	4 12	RX+ RX–	**Receiver Outputs.** Balanced differential line driver outputs which send the received signal to the DTE.
7 8	13 14	TX+ TX–	**Transmitter Inputs.** Balanced differential line receiver inputs which accept the transmission signal from the DTE and apply it to the coaxial cable at TXO.
9	15	HBE	**Heartbeat Enable.** The heartbeat function is disabled when this pin is connected to V_{EE} and enabled when connected to GND or left floating.
11 12	18 19	RR+ RR–	**External Resistor.** A 1kΩ (1%) resistor connected between these pins establishes the signaling current at TXO.
14	26	RXI	**Receiver Input.** This pin is connected directly to the coaxial cable. Received signals are equalized, amplified, and sent to the DTE through the RX± pins.
15	28	TXO	**Transmitter Output.** This pin is connected directly (Thin Ethernet) or through an external isolating diode (Ethernet) to the coaxial cable.
16	1	CDS	**Collision Detect Sense.** Ground sense connection for the collision detection circuitry. This pin should be connected directly to the coaxial cable shield for standard Ethernet operation.
10	16 17	GND	**Positive Supply Pin.**
4 5 13	5 to 11 20 to 25	V_{EE}	**Negative Supply Pins.**

NOTE:
1. The IEEE 802.3 name for CD is CI; for RX is DI; for TX is DO.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage[1]	–12	V
V_{IN}	Voltage at any input[1]	0 to –12	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec.)	+300	°C
T_J	Recommended max junction temperature[2]	+150	°C
θ_{JA}	Thermal impedance (N and A packages)	60	°C/W

NOTE:
1. 100% measured in production.
2. The junction temperature is calculated from the following expression:
   $T_J = T_A + \theta_{JA} [V_{EE} \times 0.015 \times n_{IDL}) + [V_{EE} \times 0.033 \times n_{RX}) + [V_{EE} \times 0.075 \times n_{TX})$
   where
   T_A = Ambient temperature in °C.
   θ_{JA} = Thermal resistance of package.
   V_{EE} = Normal operating supply voltage in volts.
   n_{IDL} = Percentage of duty cycle idle
   n_{RX} = Percentage of duty cycle receiving
   n_{TX} = Percentage of duty cycle transmitting

ELECTRICAL CHARACTERISTICS

V_{EE} = –9V ±6%; T_A = 0°C to +70°C unless otherwise specified[1,2]. No external isolation

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{UVL}	Under voltage lockout. Transceiver disabled for $\|V_{EE}\| < \|V_{UVL}\|$			–7.5		V
	Supply current idle			–15	–20	mA
I_{EE}	Supply current transmitting			–60	–85	mA
I_{RXI}	Receive input bias current	V_{RXI} = 0V	–2		+25	µA
I_{CDS}	Cable sense input bias current	V_{CDS} = 0V		+1	+3	µA
V_{IH}	HBE input HIGH voltage		V_{EE} +2.4			V
V_{IL}	HBE input LOW voltage				V_{EE} +1.6	V
I_{IH}	HBE input HIGH current	V_{HBE} = 0V			+10	µA
I_{IL}	HBE input LOW current	V_{HBE} = V_{EE}	–20			µA
I_{TDC}	Transmit output DC current level[3]		–37		–45	mA
I_{TAC}	Transmit output AC current level[3]		±28		±I_{TDC}	mA
I_{TX10}	Transmit current	V_{TXO} = –10V	–250		+250	µA
V_{TCOM}	Transmitter output voltage compliance[4]				–3.7	V
V_{CD}	Collision threshold[5]	Measured by applying DC voltage at RXI (CDS = 0V)	–1450	–1530	–1580	mV
V_{DIS}	AUI disable voltage at RXI	Measured as DC voltage at RXI		–3.5		V
V_{OD}	Differential output voltage – non idle at RX± and CD±[6]		±600		±1100	mV
V_{OB}	Differential output voltage imbalance – idle at RX± and CD±[7]				±40	mV
V_{OC}	Output common mode voltage at RX± and CD±	RXI = 0V	–4.5	–5.5	–6.5	V
V_{RS}	Receiver squelch threshold	V_{RXI} average DC (CDS = 0V)	–150	–250	–350	mV
V_{TS}	Transmitter squelch threshold	(V_{TX+} – $V_{TX–}$) peak	–175	–225	–275	mV
R_{RXI}	Shunt resistance at RXI non–transmitting		100			kΩ
C_{RXI}	Input capacitance at RXI			1	2	pF
R_{TXO}	Shunt resistance at TXO transmitting		7.5	10		kΩ
R_{AUIZ}	Differential impedance at RX± and CD± with no coaxial cable connected			3		kΩ
R_{TX}	Differential impedance at TX±			20		kΩ

NOTES:

1. Currents flowing into device pins are positive. All voltages are referenced to ground unless otherwise specified. For ease of interpretation, the parameter limit that appears in the MAX column is the largest value of the parameter, irrespective of sign. Similarly, the value in the MIN column is the smallest value of the parameter, irrespective of sign.
2. All typicals are for V_{EE} = –9V and T_A = 27°C.
3. I_{TDC} is measured as $(V_{MAX} + V_{MIN})/(2 \times 25)$ where V_{MAX} and V_{MIN} are the max and min voltages at TXO with a 25Ω load between TXO and GND. I_{TAC} is measured as $(V_{MAX} – V_{MIN})/(2 \times 25)$.
4. The TXO pin shall continue to sink at least I_{TDC} min when the idle (no signal) voltage on this pin is –3.7V.
5. Collision threshold for an AC signal is within 5% of V_{CD}.
6. Measured on secondary side of isolation transformer. The transformer has a 1:1 turns ratio with an inductance between 30 and 100µH at 5MHz.
7. Measured as the voltage difference between the RX pins or the CD pins with the transformer removed.

TIMING CHARACTERISTICS

V_{EE} = –9V ±6%; T_A = 0 to 70°C, unless otherwise specified[1]. No external isolation diode on TXO.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{RON}	Receiver start up delay RXI to RX± (Figure 4) First received bit on RX±	V_{RXI} = –2V peak		3	5	bits
	First validly timed bit on RX±				t_{RON} +2	bits
t_{RD}	Receiver prop. delay RXI to RX±	V_{RXI} = –2V peak		20	50	ns
t_{RR}	Differential output rise time on RX± and CD±[2,3]			5	7	ns
t_{RF}	Differential output fall time on RX± and CD±[2,3]			5	7	ns
t_{OS}	Differential output settling time on RX± and CD± to V_{OB} = 40mV[2] (see Figure 5)			1		µs
t_{RJ}	Receiver and cable total jitter			±2	±6	ns
t_{RHI}	Receiver high to idle time	Measured to +210mV	200		850	ns
t_{RM}	Rise and fall time matching on RX± and CD±	$t_{RF} - t_{RR}$		0.4	±2	ns
t_{TST}	Transmitter start-up delay TX± to TXO (Fig. 6) First transmitted bit on TXO	$V_{TX±}$ = –1V peak		1	2	bits
	First validly timed bit				t_{TST} + 2	bits
t_{TD}	Transmitter prop delay TX± to TXO (see Figure 6)	$V_{TX±}$ = 1V peak	5	20	50	ns
t_{TR}	Transmitter rise time 10% to 90% (see Figure 6)		20	25	30	ns
t_{TF}	Transmitter fall time 10% to 90% (see Figure 6)		20	25	30	ns
t_{TM}	$t_{TF} - t_{TR}$ mismatch				±2	ns
t_{TS}	Transmitter added skew[4]				±2	ns
t_{TON}	Transmitter turn on pulse width (see Figure 6)	$V_{TX±}$ = 1V peak	10		35	ns
t_{TOFF}	Transmitter turn off pulse width (see Figure 6)	$V_{TX±}$ = 1V peak	125		200	ns
t_{CON}	Collision turn on delay (see Figure 7)	0V to –2V step at RXI			13	bits
t_{COFF}	Collision turn off delay (see Figure 7)	–2V to 0V step at RXI			16	bits
t_{CHI}	Collision high to idle time (see Figure 7)	Measured to +210mV	200		850	ns
f_{CD}	Collision frequency (see Figure 7)		8.5	10	11.5	MHz
t_{CP}	Collision signal pulse width (see Figure 7)		35		70	ns
t_{HON}	Heartbeat turn on delay (see Figure 8)		0.6		1.6	µs
t_{HW}	Heartbeat test duration (see Figure 8)		0.5		1.5	µs
t_{JA}	Jabber activation delay measured from TX± to CD± (see Figure 9)		20		60	ms
t_{JR}	Jabber reset delay measured from TX± to CD± (see Figure 9)		250		650	ms

NOTES:
1. All typicals are for V_{EE} = –9V and T_A = 27°C.
2. Measured on secondary side of isolation transformer (see Figure 2). The transformer has a 1:1 turn ratio with an inductance between 30 and 100µH at 5MHz.
3. The rise and fall times are measured as the time required for the differential voltage to change from –225mV to +225mV, or +225mV to –225mV, respectively.
4. Difference in propagation delay between rising and falling edges at TXO.

FUNCTIONAL DESCRIPTION

The NE83C92 is a low power coaxial Ethernet transceiver which complies with the IEEE 802.3 specification and offers a number of additional features. These features are:

a. Low current consumption of typically 15mA when idle and 80mA with full traffic (transmitting and colliding).

Receiver Functions

The receiver consists of an input buffer, a cable equalizer, a 4-pole Bessel low pass filter, a squelch circuit and a differential line driver.

The buffer provides high input resistance and low input capacitance to minimize loading and reflections on the coaxial cable.

The equalizer is a high pass filter that compensates for the low pass effect of the coaxial cable and results in a flatband response over all signal frequencies to minimize signal distortion.

The 4-pole Bessel low pass filter extracts the average DC voltage level on the coaxial cable for use by the receiver squelch and collision detection circuits.

The receiver squelch circuit prevents noise on the coaxial cable from falsely triggering the receiver in the absence of a true signal. At the beginning of a packet, the receiver turns on when the DC level from the low pass filter exceeds the DC squelch threshold and the received packet has started with a 01 bit sequence with acceptable timing parameters. For normal signal levels this will take less than 500ns, or 5 bits. However, at the end of a packet, a fast receiver turn off is needed to reject both dribble bits on the coaxial cable and spurious responses due to settling of the on-chip bandpass filter. This is accomplished by an AC timing circuit that disables the receiver if the signal level on the coaxial cable remains high for typically 250ns and only enables the receiver again after approximately .5µs. Figures 4 and 5 illustrate receiver timing.

The differential line driver provides typically ±900mV signals to the DTE with less than 7ns rise and fall times. When in idle state (no received signal) its outputs provide <20mV differential voltage offset to minimize DC standing current in the isolation transformer. The line driver outputs (RX± and CD±) require external pull-down resistors to drive a 78Ω transmission line.

Transmitter Functions

The transmitter has differential inputs and an open collector current driver output. The differential input common mode voltage is established by the CTI and should not be altered by external circuitry. Controlled rise and fall times of 25ns (±5ns) minimize higher harmonic components in the transmitted spectrum, while matching of these rise and fall times to typically 2ns minimizes signal jitter. The drive current levels of the CTI are set by an on-chip bandgap voltage reference and an external 1% resistor. An on-chip isolation diode is provided to reduce the transmitter's coaxial cable load capacitance. For Thin Ethernet applications, no further external isolation diode is required, since the NE83C92 meets the capacitive loading specifications. For Ethernet applications a further external diode should be added to reduce loading capacitance.

The transmitter squelch circuit ensures that the transmitter can only be enabled if the transmitted packet begins with a 01 bit sequence where the negative-going differential signals are typically greater than 225mV in magnitude and 25ns in duration.

The transmitter will be disabled at the end of a packet if there are no negative going signals of greater than 225mV for more than typically 150ns. Figure 6 illustrates transmitter timing.

Collision Functions

The collision detection scheme implemented in the NE83C92 is receive mode detection, which detects a collision between any two stations on the network with certainty at all times, irrespective of whether or not the local DTE is producing one of the colliding signals. This is the only detection scheme allowed by the IEEE 802.3 standard for both repeater and non-repeater nodes.

The collision circuitry consists of the 4-pole Bessel low pass filter, a comparator, a precision voltage reference that sets up the collision threshold, a heartbeat generator, a 10MHz oscillator, and a differential line driver.

The collision comparator monitors the DC level at the output of the low pass filter and enables the line driver if it is more negative than the collision threshold. A collision condition is indicated to the DTE by a 10MHz oscillation signal at the CD outputs and typically occurs within 700ns of the onset of the collision. The collision signal begins with a negative-going pulse and ends with a continuous high-to-idle state longer than 170ns. Figure 7 illustrates collision timing.

At the end of every transmission, the heartbeat generator creates a pseudo collision to ensure that the collision circuitry is properly functioning. This pseudo collision consists of a 1µs burst of 10MHz oscillation at the line driver outputs approximately 1µs after the end of the transmission. The heartbeat function can be disabled externally by connecting the HBE (heartbeat enable) to V_{EE}. This allows the CTI to be used in repeater applications. Figure 8 illustrates heartbeat timing.

Jabber Functions

The jabber timer monitors the transmitter and inhibits transmission if it is active for longer than typically 30ms. The jabber circuit then enables the collision outputs for the remainder of the data packet and for typically 450ns (unjab time) after it has ended. At this point the transmitter becomes uninhibited. Figure 9 illustrates jabber timing.

POR/Under Voltage Lockout

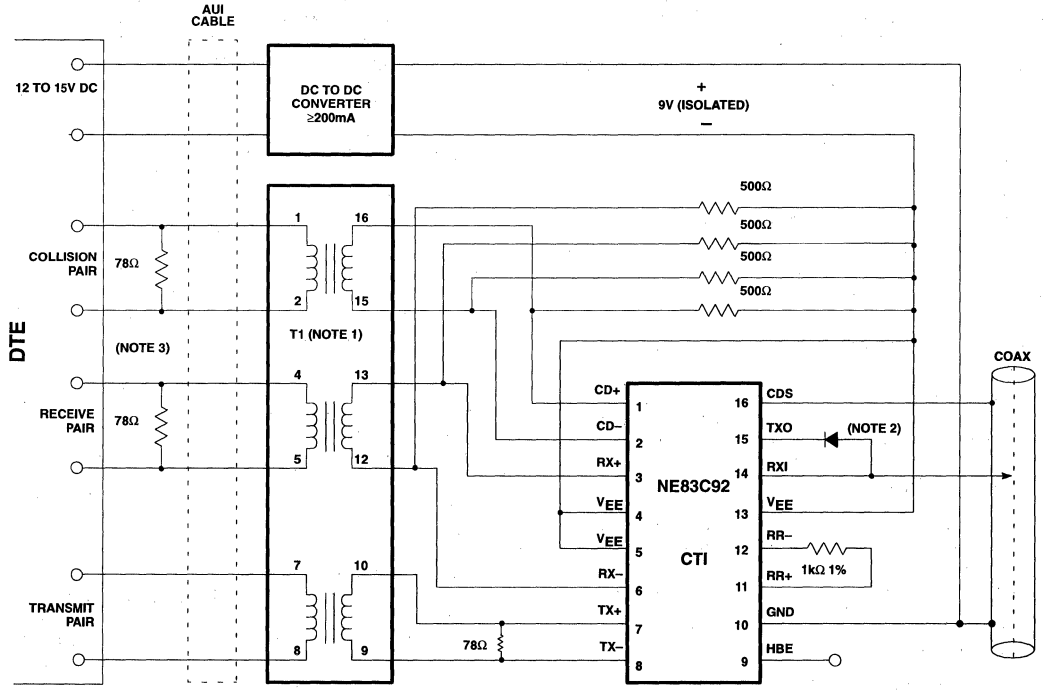
The transmit and receive squelch circuits of the NE83C92 remain active if the absolute value of V_{EE} is less than the threshold for under voltage lockout, V_{UVL}. This prevents glitches from appearing on either the AUI or coaxial cable during power up and power down.

There is no collision announcement during power up and the transceiver waits for 400ms before becoming enabled.

Detection of Coaxial Cable Faults

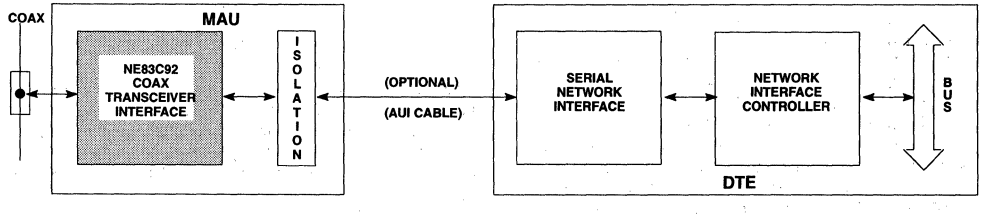
In the NE83C92 there is no internal loopback path from the TX inputs to the RX outputs. This means that, when the local DTE is transmitting, the signal will only be present at the receiver outputs RX+ and RX– if it appears on the coaxial cable and is larger than the receiver squelch threshold V_{RS}. If a short circuit fault condition occurs at the cable connector to the CTI, then no signal will appear at the receiver outputs.

A coaxial cable with only a single 50Ω termination will generate a collision not only at every transmission attempt, but also for every reception attempt due to the receive mode collision detection of the NE83C92.



NOTES:
1. T1 is a 1:1 pulse transformer, with an inductance of 30 to 100μH.
2. IN916 or equivalent for Ethernet, not required for Thin Ethernet.
3. 78Ω resistors not required if AUI cable not present.

Figure 1. Connection Diagram for Standard 8392 Applications



MAU = Medium Attachment Unit
AUI Cable = Attachment Unit Interface Cable (not used in Thin Ethernet applications)

Figure 2. Interface Diagram for Ethernet/Thin Ethernet Local Area Network

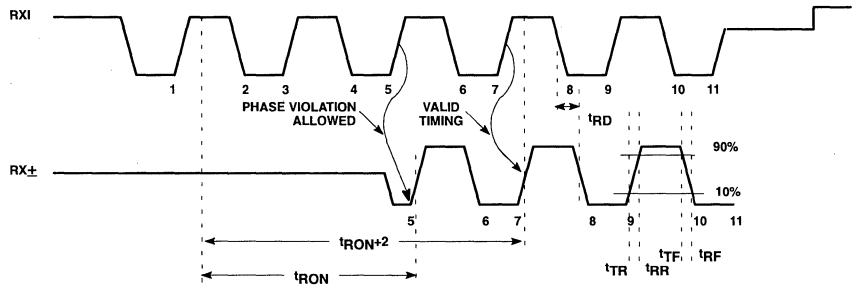


Figure 3. Receiver Timing

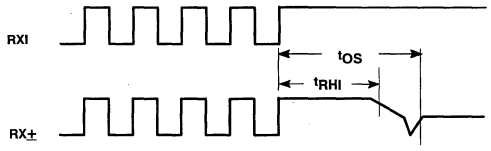


Figure 4. Receiver End-of-Packet Timing

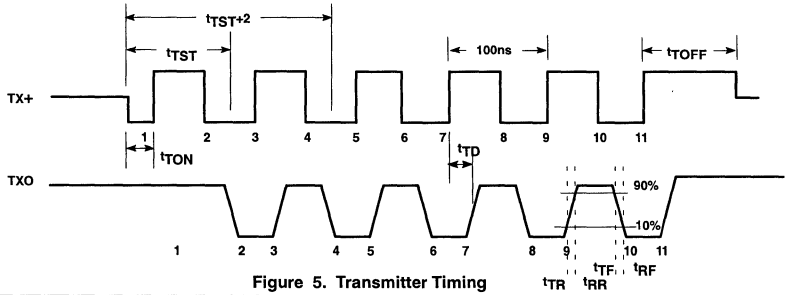


Figure 5. Transmitter Timing

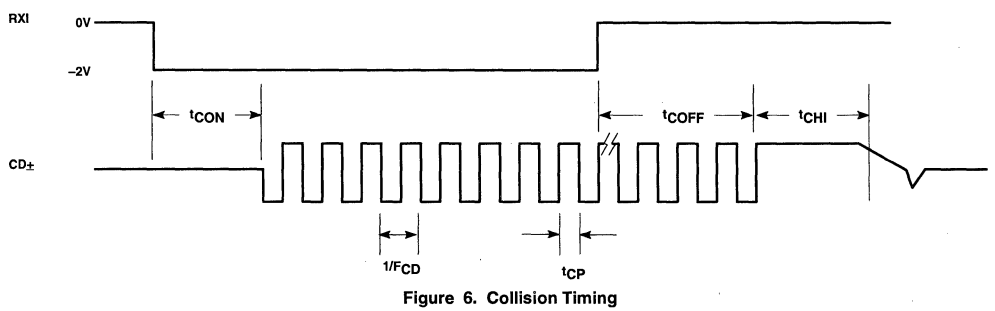


Figure 6. Collision Timing

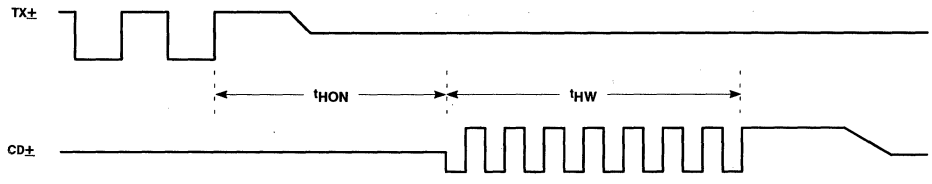


Figure 7. Heartbeat Timing

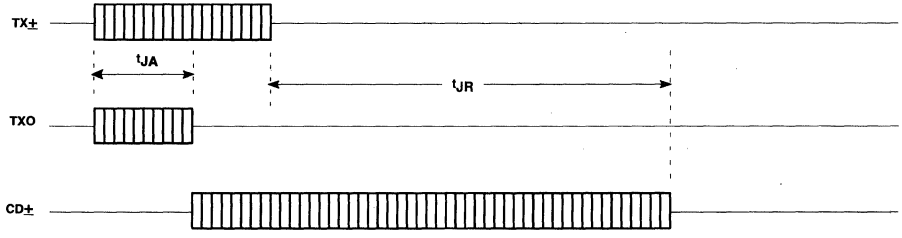


Figure 8. Jabber Timing

Miniature coaxial Ethernet transceiver — NE83Q94

DESCRIPTION

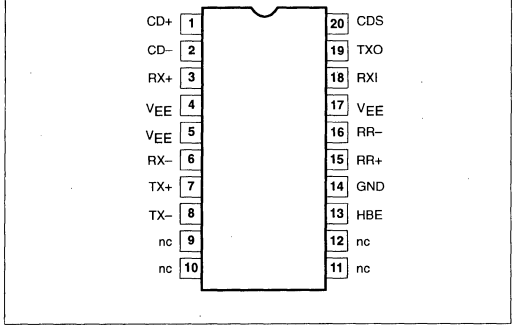
The NE83Q94 is a low power coaxial transceiver interface (CTI) for Ethernet (10base5) and Thin Ethernet (10base2) local area networks. The CTI is connected between the coaxial cable and the Data Terminal Equipment (DTE) and consists of a receiver, transmitter, collision detector, heartbeat generator and jabber timer (see Block Diagram). The transmitter output connects directly to a doubly terminated 50Ω cable, while the receiver output, collision detector output and transmitter input are connected to the DTE through isolation transformers. Isolation between the CTI and the DTE is an IEEE 802.3 requirement that can be met on signal lines by using a set of pulse transformers. Power isolation for the CTI is achieved using DC-to-DC conversion through a power transformer (see Figure 1, Connection Diagram).

The part is functionally compatible with the industry standard 8392A, but has substantially lower current consumption, is fully compliant with the IEEE802.3 standard, and has additional features such as a low current standby mode with automatic selection between AUI and coaxial connections, and extended mode collision default.

The NE83Q94 is manufactured on an advanced BiCMOS process and is ideally suited to lap-top personal computers or systems where low power consumption and no changing of board jumper positions is required.

PIN CONFIGURATION

DK Package



FEATURES

- Smallest coaxial Ethernet transceiver available, ideal for PCMCIA and space critical applications
- Fully compliant with Ethernet II, IEEE 802.3 10BASE-5 and 10BASE-2, and ISO 8802/3 interface specifications
- 100% functionally compatible with industry standard 8392
- Lowest overall current consumption allows operation using 1 Watt DC-DC converter
- Reduced external parts count
- High efficiency AUI drivers minimize current consumption under idle conditions
- Automatically enters standby mode when no coaxial cable is connected
- Standby mode allows automatic selection between AUI and Coaxial connections when no coaxial cable is connected
- Smart squelch on data inputs eliminates false activations
- Advanced BiCMOS process for extremely low power operation
- Expanded version (NE83Q93) available for repeater and advanced system applications

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Shrink Small Outline Package (SSOP)	0 to +70°C	NE83Q94DK	1563–

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{EE}	Supply voltage[1]	–12	V
V_{IN}	Voltage at any input[1]	0 to –12	V
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec.)	+300	°C
T_J	Recommended max junction temperature[2]	+150	°C
θ_{JA}	Thermal impedance (N and A packages)	110	°C/W

NOTE:
1. 100% measured in production.
2. The junction temperature is calculated from the following expression:

$$T_J = T_A + \theta_{JA}[(V_{EE} \times 0.015 \times n_{IDL}) + (V_{EE} \times 0.033 \times n_{RX}) + (V_{EE} \times 0.075 \times n_{TX})]$$

where

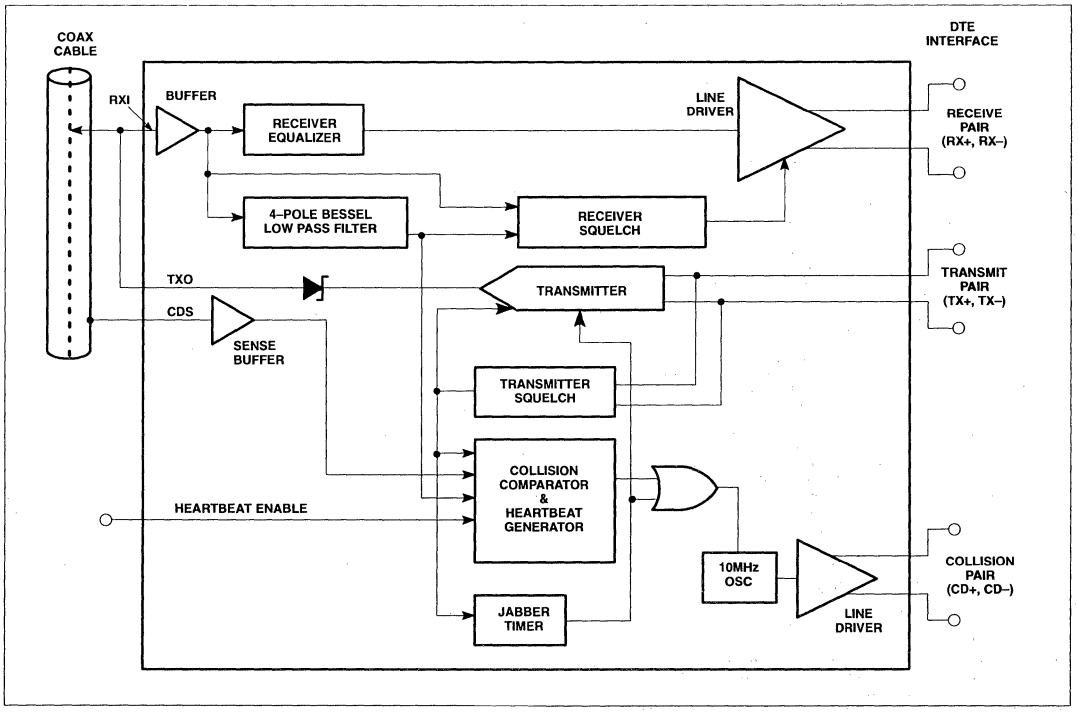
T_A = Ambient temperature in °C.
θ_{JA} = Thermal resistance of package.
V_{EE} = Normal operating supply voltage in volts.
n_{IDL} = Percentage of duty cycle idle
n_{RX} = Percentage of duty cycle receiving
n_{TX} = Percentage of duty cycle transmitting

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1 2	CD+ CD–	**Collision Outputs.** Balanced differential line driver outputs which send a 10MHz signal to the DTE in the event of a collision, jabber interrupt or heartbeat test.
3 6	RX+ RX–	**Receiver Outputs.** Balanced differential line driver outputs which send the received signal to the DTE.
7 8	TX+ TX–	**Transmitter Inputs.** Balanced differential line receiver inputs which accept the transmission signal from the DTE and apply it to the coaxial cable at TXO.
13	HBE	**Heartbeat Enable.** The heartbeat function is disabled when this pin is connected to V_{EE} and enabled when connected to GND or left floating.
15 16	RR+ RR–	**External Resistor.** A 1kΩ (1%) resistor connected between these pins establishes the signaling current at TXO.
18	RXI	**Receiver Input.** This pin is connected directly to the coaxial cable. Received signals are equalized, amplified, and sent to the DTE through the RX± pins.
19	TXO	**Transmitter Output.** This pin is connected directly (Thin Ethernet) or through an external isolating diode (Ethernet) to the coaxial cable.
20	CDS	**Collision Detect Sense.** Ground sense connection for the collision detection circuitry. This pin should be connected directly to the coaxial cable shield for standard Ethernet operation. Leaving CDS unconnected will default the collision threshold to extended mode thin Ethernet operation.
14	GND	**Positive Supply Pin.**
4 5 17	V_{EE}	**Negative Supply Pins.**

NOTE:
1. The IEEE 802.3 name for CD is CI; for RX is DI; for TX is DO.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

V_{EE} = –9V ±6%; T_A = 0°C to +70°C unless otherwise specified[1,2]. No external isolation

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{UVL}	Under voltage lockout. Transceiver disabled for $\|V_{EE}\| < \|V_{UVL}\|$			–7.5		V
I_{EE}	Supply current idle			–15	–20	mA
	Supply current transmitting			–60	–85	mA
I_{RXI}	Receive input bias current	V_{RXI} = 0V	–2		+25	µA
I_{CDS}	Cable sense input bias current	V_{CDS} = 0V		+1	+3	µA
V_{IH}	HBE input HIGH voltage		V_{EE} +2.4			V
V_{IL}	HBE input LOW voltage				V_{EE} +1.6	V
I_{IH}	HBE input HIGH current	V_{HBE} = 0V			+10	µA
I_{IL}	HBE input LOW current	V_{HBE} = V_{EE}	–20			µA
I_{TDC}	Transmit output DC current level[3]		–37		–45	mA
I_{TAC}	Transmit output AC current level[3]		±28		±I_{TDC}	mA
I_{TX10}	Transmit current	V_{TXO} = –10V	–250		+250	µA
V_{TCOM}	Transmitter output voltage compliance[4]				–3.7	V
V_{CD}	Collision threshold[5]	Measured by applying DC voltage at RXI (CDS = 0V)	–1450	–1530	–1580	mV
V_{DIS}	AUI disable voltage at RXI	Measured as DC voltage at RXI		–3.5		V
V_{OD}	Differential output voltage – non idle at RX± and CD±[6]		±600		±1100	mV
V_{OB}	Differential output voltage imbalance – idle at RX± and CD±[7]				±40	mV
V_{OC}	Output common mode voltage at RX± and CD±	RXI = 0V	–4.5	–5.5	–6.5	V
V_{RS}	Receiver squelch threshold	V_{RXI} average DC (CDS = 0V)	–150	–250	–350	mV
V_{TS}	Transmitter squelch threshold	(V_{TX+} – V_{TX-}) peak	–175	–225	–275	mV
R_{RXI}	Shunt resistance at RXI non–transmitting		100			kΩ
C_{RXI}	Input capacitance at RXI			1	2	pF
R_{TXO}	Shunt resistance at TXO transmitting		7.5	10		kΩ
R_{AUIZ}	Differential impedance at RX± and CD± with no coaxial cable connected			3		kΩ
R_{TX}	Differential impedance at TX±			20		kΩ

NOTES:

1. Currents flowing into device pins are positive. All voltages are referenced to ground unless otherwise specified. For ease of interpretation, the parameter limit that appears in the MAX column is the largest value of the parameter, irrespective of sign. Similarly, the value in the MIN column is the smallest value of the parameter, irrespective of sign.
2. All typicals are for V_{EE} = –9V and T_A = 27°C.
3. I_{TDC} is measured as (V_{MAX} + V_{MIN})/(2 x 25) where V_{MAX} and V_{MIN} are the max and min voltages at TXO with a 25Ω load between TXO and GND. I_{TAC} is measured as (V_{MAX} – V_{MIN})/(2 x 25).
4. The TXO pin shall continue to sink at least I_{TDC} min when the idle (no signal) voltage on this pin is –3.7V.
5. Collision threshold for an AC signal is within 5% of V_{CD}.
6. Measured on secondary side of isolation transformer (see Connection Diagram, Figure 1). The transformer has a 1:1 turns ratio with an inductance between 30 and 100µH at 5MHz.
7. Measured as the voltage difference between the RX pins or the CD pins with the transformer removed.

TIMING CHARACTERISTICS

V_{EE} = –9V ±6%; T_A = 0 to 70°C, unless otherwise specified[1]. No external isolation diode on TXO.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{RON}	Receiver start up delay RXI to RX± (Figure 4) First received bit on RX±	V_{RXI} = –2V peak		3	5	bits
	First validly timed bit on RX±				t_{RON} +2	bits
t_{RD}	Receiver prop. delay RXI to RX±	V_{RXI} = –2V peak		20	50	ns
t_{RR}	Differential output rise time on RX± and CD±[2,3]			5	7	ns
t_{RF}	Differential output fall time on RX± and CD±[2,3]			5	7	ns
t_{OS}	Differential output settling time on RX± and CD± to V_{OB} = 40mV[2] (see Figure 5)			1		µs
t_{RJ}	Receiver and cable total jitter			±2	±6	ns
t_{RHI}	Receiver high to idle time	Measured to +210mV	200		850	ns
t_{RM}	Rise and fall time matching on RX± and CD±	$t_{RF} - t_{RR}$		0.4	±2	ns
t_{TST}	Transmitter start–up delay TX± to TXO (Fig. 6) First transmitted bit on TXO	$V_{TX±}$ = –1V peak		1	2	bits
	First validly timed bit				t_{TST} + 2	bits
t_{TD}	Transmitter prop delay TX± to TXO (see Figure 6)	$V_{TX±}$ = 1V peak	5	20	50	ns
t_{TR}	Transmitter rise time 10% to 90% (see Figure 6)		20	25	30	ns
t_{TF}	Transmitter fall time 10% to 90% (see Figure 6)		20	25	30	ns
t_{TM}	$t_{TF} - t_{TR}$ mismatch				±2	ns
t_{TS}	Transmitter added skew[4]				±2	ns
t_{TON}	Transmitter turn on pulse width (see Figure 6)	$V_{TX±}$ = 1V peak	10		35	ns
t_{TOFF}	Transmitter turn off pulse width (see Figure 6)	$V_{TX±}$ = 1V peak	125		225	ns
t_{CON}	Collision turn on delay (see Figure 7)	0V to –2V step at RXI			13	bits
t_{COFF}	Collision turn off delay (see Figure 7)	–2V to 0V step at RXI			16	bits
t_{CHI}	Collision high to idle time (see Figure 7)	Measured to +210mV	200		850	ns
f_{CD}	Collision frequency (see Figure 7)		8.5	10	11.5	MHz
t_{CP}	Collision signal pulse width (see Figure 7)		35		70	ns
t_{HON}	Heartbeat turn on delay (see Figure 8)		0.6		1.6	µs
t_{HW}	Heartbeat test duration (see Figure 8)		0.5		1.5	µs
t_{JA}	Jabber activation delay measured from TX± to CD± (see Figure 9)		20		60	ms
t_{JR}	Jabber reset delay measured from TX± to CD± (see Figure 9)		250		650	ms

NOTES:
1. All typicals are for V_{EE} = –9V and T_A = 27°C.
2. Measured on secondary side of isolation transformer (see Figures 1 and 2, Connection Diagram). The transformer has a 1:1 turn ratio with an inductance between 30 and 100µH at 5MHz.
3. The rise and fall times are measured as the time required for the differential voltage to change from –225mV to +225mV, or +225mV to –225mV, respectively.
4. Difference in propagation delay between rising and falling edges at TXO.

FUNCTIONAL DESCRIPTION

The NE83Q94 is a low power coaxial Ethernet transceiver which complies with the IEEE 802.3 specification and offers a number of additional features. These features are:

1. Low current consumption of typically 15mA when idle and 80mA with full traffic (transmitting and colliding) allows smaller DC-DC converter to be used for the isolated power supply.
2. Automatic selection between AUI cable and coaxial connections by placing the AUI outputs in a high impedance state when the coaxial cable is disconnected. This eliminates the need for changing a jumper position on the Ethernet board when selecting either Thin Ethernet or remote transceiver connections.
3. High efficiency AUI drivers for the RX± and CD± ports which automatically power down when idle. The NE83Q94 requires no external pull-down resistors on these ports.

Receiver Functions

The receiver consists of an input buffer, a cable equalizer, a 4-pole Bessel low pass filter, a squelch circuit and a differential line driver.

The buffer provides high input resistance and low input capacitance to minimize loading and reflections on the coaxial cable.

The equalizer is a high pass filter that compensates for the low pass effect of the coaxial cable and results in a flatband response over all signal frequencies to minimize signal distortion.

The 4-pole Bessel low pass filter extracts the average DC voltage level on the coaxial cable for use by the receiver squelch and collision detection circuits.

The receiver squelch circuit prevents noise on the coaxial cable from falsely triggering the receiver in the absence of a true signal. At the beginning of a packet, the receiver turns on when the DC level from the low pass filter exceeds the DC squelch threshold and the received packet has started with a 01 bit sequence with acceptable timing parameters. For normal signal levels this will take less than 500ns, or 5 bits. However, at the end of a packet, a fast receiver turn off is needed to reject both dribble bits on the coaxial cable and spurious responses due to settling of the on-chip bandpass filter. This is accomplished by an AC timing circuit that disables the receiver if the signal level on the coaxial cable remains high for typically 250ns and only enables the receiver again after approximately .5µs. Figures 4 and 5 illustrate receiver timing.

The differential line driver provides typically ±900mV signals to the DTE with less than 7ns rise and fall times. When in idle state (no received signal) its outputs provide <20mV differential voltage offset to minimize DC standing current in the isolation transformer. The line driver outputs (RX± and CD±) require no external pull-down resistors and will drive a 78Ω transmission line directly. They automatically power down under idle conditions and are powered up when a receive signal is detected.

Transmitter Functions

The transmitter has differential inputs and an open collector current driver output. The differential input common mode voltage is established by the CTI and should not be altered by external circuitry. Controlled rise and fall times of 25ns (±5ns) minimize higher harmonic components in the transmitted spectrum, while matching of these rise and fall times to typically 2ns minimizes signal jitter. The drive current levels of the CTI are set by an on-chip bandgap voltage reference and an external 1% resistor. An on-chip isolation diode is provided to reduce the transmitter's coaxial cable load capacitance. For Thin Ethernet applications, no further external isolation diode is required, since the NE83Q94 meets the capacitive loading specifications. For Ethernet applications a further external diode should be added to reduce loading capacitance.

The transmitter squelch circuit ensures that the transmitter can only be enabled if the transmitted packet begins with a 01 bit sequence where the negative-going differential signals are typically greater than 225mV in magnitude and 25ns in duration.

The transmitter will be disabled at the end of a packet if there are no negative going signals of greater than 225mV for more than typically 150ns. Figure 6 illustrates transmitter timing.

Collision Functions

The collision detection scheme implemented in the NE83Q94 is receive mode detection, which detects a collision between any two stations on the network with certainty at all times, irrespective of whether or not the local DTE is producing one of the colliding signals. This is the only detection scheme allowed by the IEEE 802.3 standard for both repeater and non-repeater nodes.

The collision circuitry consists of the 4-pole Bessel low pass filter, a comparator, a precision voltage reference that sets up the collision threshold, a heartbeat generator, a 10MHz oscillator, and a differential line driver.

The collision comparator monitors the DC level at the output of the low pass filter and enables the line driver if it is more negative than the collision threshold. A collision condition is indicated to the DTE by a 10MHz oscillation signal at the CD outputs and typically occurs within 700ns of the onset of the collision. The collision signal begins with a negative-going pulse and ends with a continuous high-to-idle state longer than 170ns. Figure 7 illustrates collision timing.

At the end of every transmission, the heartbeat generator creates a pseudo collision to ensure that the collision circuitry is properly functioning. This pseudo collision consists of a 1µs burst of 10MHz oscillation at the line driver outputs approximately 1µs after the end of the transmission. The heartbeat function can be disabled externally by connecting the HBE (heartbeat enable) to V_{EE}. This allows the CTI to be used in repeater applications. Figure 8 illustrates heartbeat timing.

As with the receiver AUI drivers, the CD± outputs require no external pull-down resistors, although they still operate if the resistors are present, and automatically power down under idle conditions.

Jabber Functions

The jabber timer monitors the transmitter and inhibits transmission if it is active for longer than typically 30ms. The jabber circuit then enables the collision outputs for the remainder of the data packet and for typically 450ns (unjab time) after it has ended. At this point the transmitter becomes uninhibited. Figure 9 illustrates jabber timing.

AUI Selection/Under Voltage Lockout

The transmit and receive squelch circuits of the NE83Q94 remain active if the absolute value of V_{EE} is less than the threshold for under voltage lockout, V_{UVL}. This prevents glitches from appearing on either the AUI or coaxial cable during power up and power down.

There is no collision announcement during power up and the transceiver waits for 400ms before becoming enabled.

If RXI is disconnected from the coaxial cable after power up, its voltage will fall towards V_{EE}. If the absolute value of this voltage exceeds the AUI disable voltage, V_{DIS}, for longer than 800ms, the transmit and receive squelch circuits remain active and, in addition,

the AUI drivers become high impedance. This permits AUI connections to be hard wired together, e.g., the coaxial transceiver and a 10BASE-T transceiver, with the signal path determined by which transceiver is connected to its external cable.

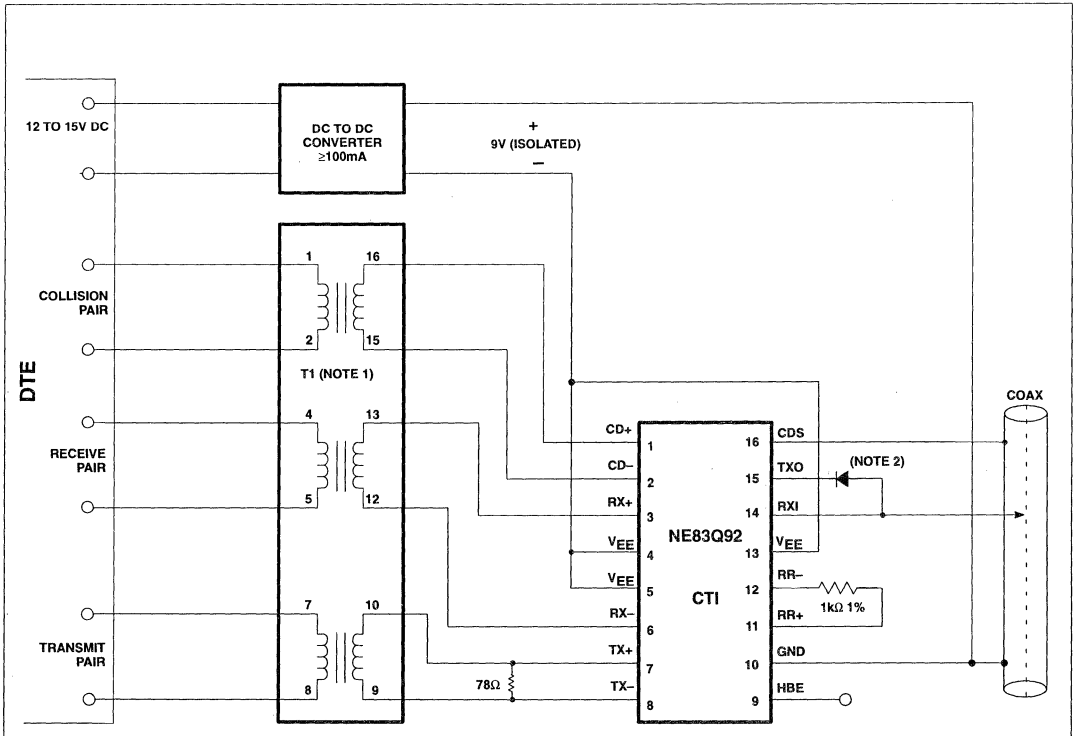
There is no collision announcement on disconnecting RXI, but there is a 400ms announcement on re-connection before the transceiver is enabled.

Detection of Coaxial Cable Faults

In the NE83Q94 there is no internal loopback path from the TX inputs to the RX outputs. This means that, when the local DTE is transmitting, the signal will only be present at the receiver outputs RX+ and RX– if it appears on the coaxial cable and is larger than the receiver squelch threshold V_{RS}. If a short circuit fault condition occurs at the cable connector to the CTI, then no signal will appear at the receiver outputs.

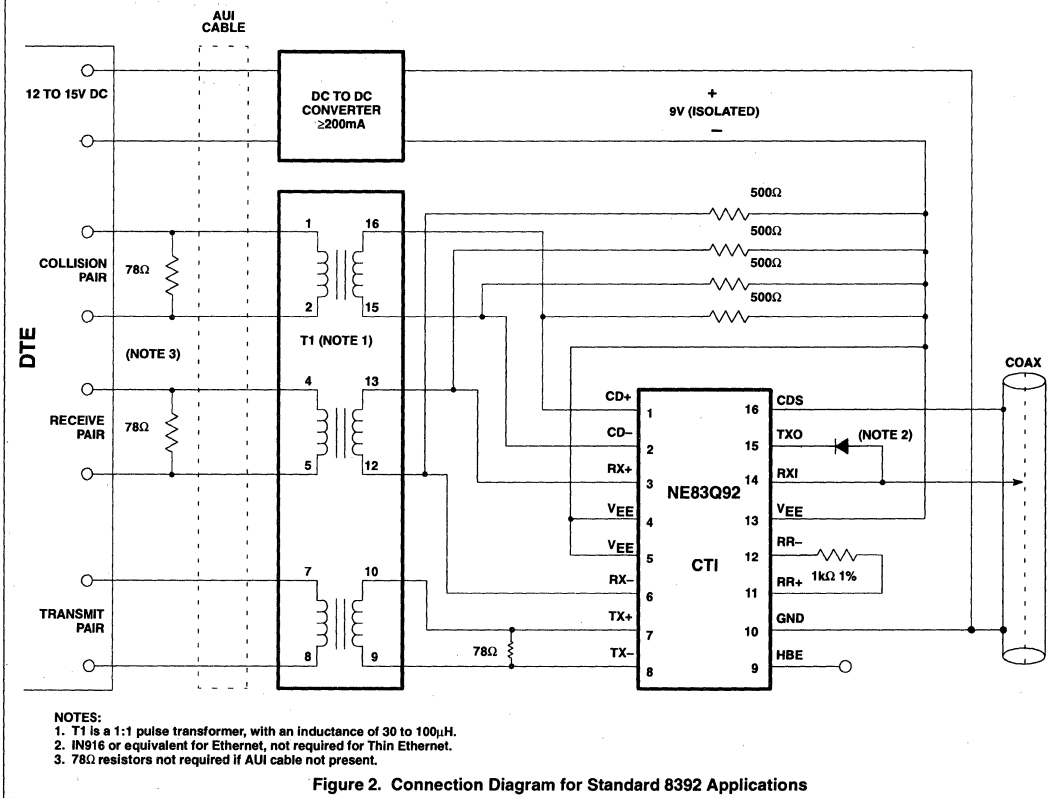
In the case of an open circuit at the coaxial cable connector there will also be no signal at the receiver outputs due to the AUI disabling mode of the NE83Q94. However, a heartbeat signal will be present following a transmission attempt for the short circuit condition, but not for the open circuit.

A coaxial cable with only a single 50Ω termination will generate a collision not only at every transmission attempt, but also for every reception attempt due to the receive mode collision detection of the NE83Q94.



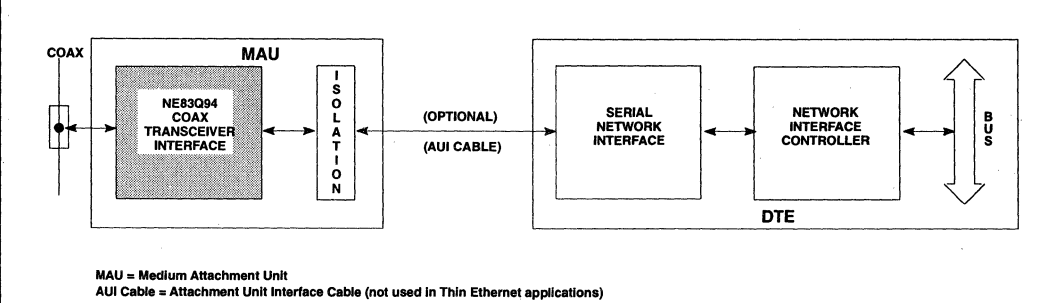
NOTES:
1. T1 is a 1:1 pulse transformer, with an inductance of 30 to 100μH.
2. IN916 or equivalent for Ethernet, not required for Thin Ethernet.

Figure 1. Connection Diagram for Minimum Current Consumption



NOTES:
1. T1 is a 1:1 pulse transformer, with an inductance of 30 to 100μH.
2. IN916 or equivalent for Ethernet, not required for Thin Ethernet.
3. 78Ω resistors not required if AUI cable not present.

Figure 2. Connection Diagram for Standard 8392 Applications



MAU = Medium Attachment Unit
AUI Cable = Attachment Unit Interface Cable (not used in Thin Ethernet applications)

Figure 3. Interface Diagram for Ethernet/Thin Ethernet Local Area Network

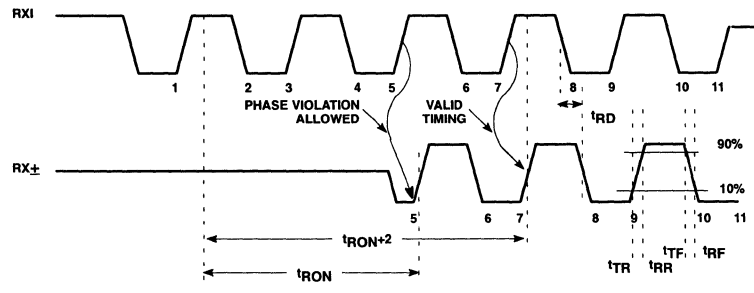


Figure 4. Receiver Timing

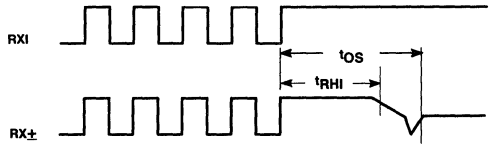


Figure 5. Receiver End–of–Packet Timing

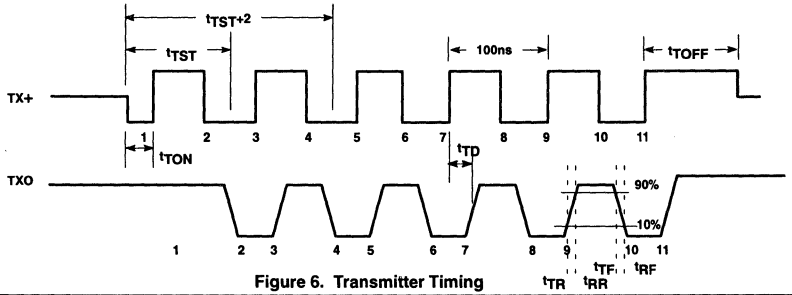


Figure 6. Transmitter Timing

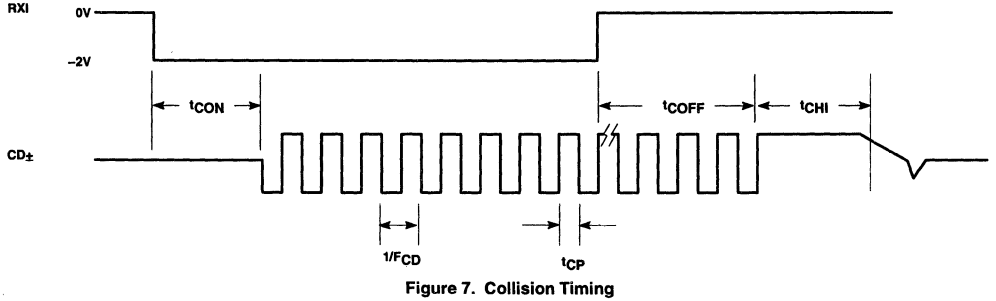


Figure 7. Collision Timing

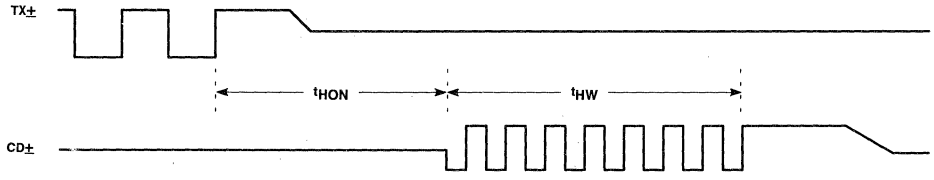


Figure 8. Heartbeat Timing

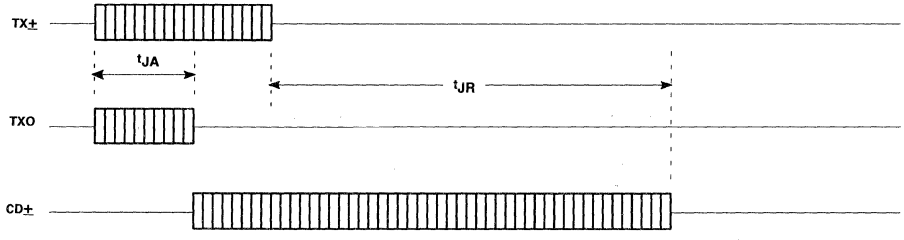


Figure 9. Jabber Timing

Section 6
Fibre Optic Products
Data Sheets

CONTENTS

A phase locked fiber optic system using FM modulation — AN1434

Author: Les Hadley

SYSTEM OPERATION SUMMARY

The purpose of the fiber link is to transmit broadband video and sound over moderate distances (2.5km) with existing low cost components and minimal complexity.

Figure 1 depicts a complete system implementation. The application makes use of a very wideband VCO to generate an FM modulated carrier at 28.6MHz followed by a fast TTL LED driver to emit saturated 850nm light signals for entry in to the glass fiber. A PIN diode receiver is coupled to a 140MHz bandwidth transimpedance preamplifier for increasing the detected signal amplitude and then fed to a phase-locked loop demodulator for recovering the original modulation signals.

The wideband FM sound subcarrier (150kHz deviation) is summed with baseband video at 10.7MHz and transmitted at a reduced level relative to the 3.58MHz color reference signal. Cross modulation between sound and picture information is minimized in this way. FM demodulation of the sound subcarrier is accomplished after passing through an IF gain block by a quadrature-type phase discriminator. The present sound circuit does not automatically frequency-lock to the transmitted subcarrier, but is fixed-tuned to 10.7MHz. A tracking PLL sound demodulator could be used to eliminate drift problems between transmitted sound subcarrier and the receiver in future designs.

SYSTEM DESCRIPTION AND OPERATION

Transmitter Unit: Video Channel

The transmitter circuit consists of a wideband differential amplifier (NE592), a VCO (NE564) and an LED driver, the NE522 high speed comparator (see Figure 2) The video signal is AC coupled into the modulator preamplifier and followed by a sync tip clamp to provide DC restoration of the composite video signal and to prevent variation of modulation deviation with varying picture content. (A complete video clamp and sync processor may be designed using the TDA9045 and TDA2595 combination. This particular application was not tested at the time of this publication.)

A video signal level of 250 to 300mV peak is required to maintain optimum picture modulation. Since there is no AGC circuit in this particular design, this is a critical parameter and must be con- trolled to prevent over-modulation and picture degradation. Addition of an AGC using the above-mentioned parts would be a definite improvement for varying input level video. Using the present limited design, however, -10dB of attenuation was used with a 1V peak NTSC signal source at 75Ω. This is the common level available from most standard video signal systems.

Frequency compensation (pre-emphasis) is inserted in the form of a passive RC lead network at the Pin 14 input to the NE592 differential amplifier. This compensates for degenerative frequency distortion and provides better color balance in transmission.

The main FM modulator consists of an NE564 used only as a linear wideband VCO. The other sections of the device are not used. Differential DC coupling to the VCO terminals is attained via the loop filter terminals, Pins 4 and 5. The NE564 VCO is designed as a differential current controlled balanced multivibrator. It possesses an extremely linear transfer function as illustrated in Figure 3. The graph shows how the VCO frequency varies with applied DC voltage across Pins 4 and 5. The VCO center frequency is determined by value of the capacitance across Pins 12 and 13. In this particular example, the transmitter operates at 14.3MHz with the VCO set to 26.6MHz.

The slope of the VCO transfer function is termed K_O and is measured in radians per second per volt or simply Herz per volt. Thus, to obtain the magnitude of the differential voltage for a given frequency deviation the relationship below is used:

$$V_{D(voltsDC)} = \frac{\Delta f}{k_O} \frac{MHz}{MHz/V}$$

$$I_{B2} = \text{Constant}$$

K_O is dependent upon the control bias generator current at Pin 2 as is noted from the graph. Higher current into Pin 2 results in a higher conversion gain, K_O. For a center frequency of 1MHz and an 800µA bias current into Pin 2, K_O is 1.7MHz/V across Pins 4 and 5 (V_O).

The value of K_O also increases linearity with center frequency so that at 30MHz K_O becomes 30X 1.7 or 51MHz/V. Note that in this application the bias current is set at 320µA; that is the device is sinking current into Pin 2. This lowers K_O below the given value for 800µA shown on the graph in Figure 3 and requires a higher number of V/MHz to modulate the VCO. The signal to the VCO is DC coupled from the differential output of the NE592 in order to preserve bandwidth and to maintain proper biasing relative to the NE564.

Setting FM Deviation

In order to calculate the approximate frequency deviation, a linear relationship between ΔK_O and ΔI_{B2} is assumed. The value of K_O for a Pin 2 bias of 320µA is determined by the following relationship:

$$k_O = \left[\frac{(1.7 - 0.95) \cdot 320}{2 \cdot 800} + 0.95\right] MHz/Volt$$

$= 1.1MHz/V @ 1MHz$

$= 33MHz/V @ 30MHz$

The measured differential voltage between Pins 4 and 5 for normal operating signal levels and standard NTSC color bars transmitted is $80mV_{P-P}$. The estimated total deviation is then 1.3MHz. This results in a Video channel bandwidth for the 3.58MHz color signal of approximately:

$= 2(1.3 + 3.58)MHz$

$= 9.8MHz$

This is rather a small deviation for wideband video transmission and the decision was made to use the 2nd harmonic of the fundamental VCO frequency to obtain twice the deviation. The VCO modulator is then set at an I_B of 320µA which provides sufficient 2nd harmonic content for this to operate successfully. This is shown in Figure 5 with the fundamental at 14.3MHz with the middle spectral plot showing required 28.6MHz carrier harmonic with improved deviation ratio.

Total FM Signal Bandwidth

For a total video bandwidth of 4.2MHz the transmission bandwidth is:

$BW = 2x2(1.3 + 4.2) = 22MHz$

Note that a bandpass filter could be installed in the signal path between the NE592 preamp/buffer to reduce noise bandwidth, but

A phase locked fiber optic system using FM modulation AN1434

this improvement was not tried. Adequate signal space for the baseband video and the 10.7MHz subcarrier would be 11MHz. (Filter characteristics must provide good differential gain and phase response.)

A second bandpass filter could be added in the path between the modulator and the LED driver stage (22MHz bandwidth). This would improve the overall video signal-to-noise ratio.

The NE592 is biased with +5V and -1.8V to achieve the critical dynamic swing to properly slew the VCO over the required range without sacrificing faithful waveform reproduction in the transformation to linear FM modulation. Video signals contain both very low and high frequencies which are transient and phase sensitive. The unused input pins to the phase detector, Pins 6 and 7 bypassed to ground. Pin 3 is grounded.

The 28.6MHz FM signal from the NE564 is taken from the Pin 9 open collector VCO output port which requires a 470Ω pull-up resistor to 5V. A100Ω resistor is added to Pin 11 to improve the fall time of the output waveform. The signal is then fed into the NE522 (74F3040) high speed comparator where a threshold level is set up on the inverting terminal to provide duty cycle adjustment and noise threshold. The NE522 has an open collector output which lends itself easily to driving the LED transmitter diode (CQF24); the 74F3040 has a source-sink output stage which requires that the LED be connected as shown in Figure 2a.

The CQF24 generates 100μW of 850nm optical energy with a typical rise and fall time of 10ns. It is rated at 250mW dissipation and 100mA continuous current.

Spectral frequency plots taken under normal operating conditions with NTSC color bar signal input for the sections of the transmitter described above appear in Figures 4 through 6.

The Sound Channel

As shown in the block diagram in Figure 2, audio input is fed through a 2:1 compressor which consist of the NE575 low voltage compandor. This device compresses all audio signals according to the transfer function shown in Figure 7. It is required to limit the peak FM deviation for the10.7MHz VCO to ±75kHz for 0dBV input ($1V_{IN}$ 600Ω RMS). Audio compression also improves intelligibility in systems with limited signal-to-noise ratio. This device, NE575, operates at unity gain for an input level of $100mV_{RMS}$ audio input which is 0dB for the NE575. The 2:1 compression factor refers to the AC signal level in dB above or below $100mV_{RMS}$.[2] Output from the NE575 is fed to the second NE564 modulator with a VCO center frequency set at 10.7MHz. Refer to Figure 8 for typical circuit diagram. The 10.7MHz subcarrier is fed to the NE592 for summing with the main baseband video signal. The level of the sound subcarrier is adjusted to a level 20dB below the 3.58MHz color video sideband (28.6MHz signal) by adjustment of the output level potentiometer at the emitter follower, Q1 (see Figure 9). This can be accomplished most easily by monitoring the combined 28.6MHz signal from the main modulator (Pin 9 NE564) using a spectrum analyzer. The 10.7MHz carrier deviation is adjusted using 0dBm ($775mV_{RMS}$ into 600Ω) input to the compressor at 1kHz and adjusting the deviation with the input potentiometer, R7, which feeds the NE564 (see Figure 9 for the 10.7MHz schematic). Figure 10 displays the proper frequency deviation spectrum as set by the R7 adjustment. A 0dBm (775mV) input to the compressor is 16dB above the compandor 100mV reference level and the compressor will reduce this +18dB input level to approximately $260mV_{RMS}$ at the NE5750 output on Pin14. The pot. R7, provides the calibration adjustment for maximum 10.7MHz deviation.

The actual 10.7MHz level to the 30MHz modulator is set by pot R6 and is adjusted by monitoring the spectral level at the output, Pin 9, of the NE564 with a spectrum analyzer. The relative sound carrier (lower 28.6MHz sideband) is set approximately 20dB below the 3.58MHz color reference signal. This is accomplished by first noting the sideband level of the video information (Figure 5), removing the video modulation and setting the 10.7MHz level with R8 on the sound modulator board.

The Receiver Unit

Light energy from the fiber optic cable is fed to the BPF24 PIN diode and transformed to a small current typically in the 1 to 5μA range. This photodiode current carries all of the FM carrier information in the signal bandwidth of approximately 22MHz centered at 28.6MHz. The photo- current is now amplified and transformed into a differential signal voltage by the NE5212 transimpedance amplifier (Pin 1 input). In this particular application, however, the output is not used differentially, but a single-ended signal is taken from Pin 5 of the NE5212 and AC coupled to Pin 6 of the NE564.

The NE5212 has a differential transresistance of 14k. This translates to 14μV/mA of input current, yielding 35mV of differential output voltage for 2.5μA input current. Since the device is used single ended, only half, or 17.5mV, output is available to drive the phase detector of the NE564. (See Figure 12 for actual output signal from NE5212). The low signal level input to the PLL makes it necessary to run the gain setting bias at a higher level than usual; this, in addition to the wide bandwidth, requires a bias current of 2.2mA sinking into Pin 2 of the NE564. Another modification to the nominal NE564 operating conditions is the choice of a higher supply voltage on the phase detector portion of the device (+8V on Pin 1) to increase the linearity and dynamic range for fast video signals. The VCO section is supplied from +8V through a 200Ω dropping resistor and operates on 4.5V at Pin 10. (Note that the absolute maximum voltages for the phase detector and VCO are 14 and 6V, respectively).

VCO Frequency Adjustment

The NE564 receiver PLL is operated at the same frequency as the 2nd harmonic of the transmitter fundamental 28.6MHz. Prior to making any adjustments, the bias current to Pi n 2 is set to 2.2mA. The spectrum of the receiver VCO without a fiber link signal, fiber disconnected, is shown in Figure 13. When making the initial center frequency adjustment to the VCO trimmer cap (NE564 Pin 12, 13, 2-20pF) the fiber cable is disconnected. (Note that a thermal stabilization time of 1 hour is recommended prior to any transmitter or receiver calibration adjustments.)

With the link connected and a proper signal present at the input to the NE554 Pin 5, the PLL will lock onto and track the incoming wideband FM signal. (See Figure 14 for VCO spectrum.) Note that the unwanted harmonic signals number one and three have not been filtered out in this application example.

The demodulated baseband video plus 10.7MHz signal then appears on the analog output port, Pin14. A wideband amplifier with low differential gain and phase error (NE5539) is used to boost the combined signal with the composite video level raised to 1V peak into 7Ω. The actual measured value of the video using an NTSC color bar signal is $1V_{P-P}$ on the output port. The NE554 output to the NE564 from Pin14 is $250mV_{P-P}$.

A phase locked fiber optic system using FM modulation AN1434

Figure 15 shows the composite baseband video plus 10.7MHz subcarrier spectrum.

The final stage of the video channel is the NE5539 which drives directly into the video monitor. Biasing the DC offset of the postamplifier is necessary to prevent sync distortion and optimum video response. This is accomplished by adjusting R2 (1MΩ pot on Pin 1 of NE5539) for 0V average at the output. Note that a lead-lag network is connected across Pins 1 and 14 to stabilize the op amp which has a closed loop bandwidth of approximately100MHz for a closed loop gain of 4. This excessive bandwidth creates noise in the picture information and is reduced by the 20pF capacitor from Pin 12 to 14. (See Figure 11.)

Sound Channel Operation and Adjustment

A portion of the output signal from the NE5539 is also sent to the NE604A to be amplified and demodulated (see Figure 5). The composite signal contains both the video and the 10.7MHz subcarrier. A ceramic 10.7MHz bandpass filter is used before the NE604A to remove all but the subcarrier. The NE604A contains a high gain IF amplifier and an LC quadrature detector for demodulating the FM sound Information.

Adjustment of the sound channel Is carried out after the system has been on for one hour to allow thermal stabilization. A 1kHz test signal is injected into the audio input port of the NE575 compressor board and set to 775mV$_{RMS}$ terminated in 600Ω. Using a spectrum analyzer adjust R7 while observing the 10.7MHz output on a spectrum analyzer and set the deviation for 150kHZ maximum. At this point make sure that the 10.7MHz VCO (NE564) is on frequency, and make any trim adjustments to the VCO trim capacitor. Finally adjust R8 for a carrier amplitude by monitoring the output of the transmitter VCO lower sideband, and set the10.7MHz signal 20dB below the 3.58MHz sideband relative to 28.6MHz. The last adjustment is the setting of the quadrature coil on the NE604A demodulator for maximum sound with the best signal-to-noise. (Refer to Figure 17 for the input signal spectrum to the NE604A.)

CONCLUSION

The system example described Is capable of transmitting single channel color video and sound transmission at 850nm with glass or plastic fiber optic cable of ≥2.5km. Signal transmission is of adequate quality for Industrial inspection, security and other applications of this limited nature. The most notable feature is its minimal cost. It Is not meant to be used in broadcast quality environments. The user Is invited to make improvements and alterations to the system to attain greater stability and higher quality.

The audio amplifier and control section shown in Figure 1 is not included in this application note. For further detail on the audio portion and applications examples, please refer to Section 7 of the Philips Semiconductors IC-11: General-Purpose Linear ICs.

Suggested areas of improvement are: 1. The addition of bandpass filters to improve transmitter and receiver signal-to-noise; 2. Video sync tip or black level clamp with AGC at transmitter modulation input; 3. Addition of an AGC stage after the receiver transimpedance amplifier to improve optical path dynamic range.

Power Supply Requirements

The regulated voltages required to operate the system are as follows:

+5.00V

-5.00V

+8.00V

-8.00V

Test Equipment

1. HP8568B Spectrum Analyzer
2. Tektronix PC6202 FET Probe 10X
3. Philips 5510 Color Generator

Footnotes

1. Philips Semiconductors Linear Data Manual, Volume 1, Communications, 1987
2. *Ibid.*

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Philips Semiconductors, *Linear Data Manual, Volume 1, Communications*, 1987.

1. AN140: Compensation Techniques for Use with the NE/SE5539
2. AN175: Automatic Level Control: NE572
3. AN176: Compandor Cookbook
4. AN179: Circuit Description of the NE564
5. AN1991: Audio Decibel Level Detector with Meter Drive (NE604)

Philips Semiconductors, Linear Data Manual, Volume 3, Communications, 1987.

AN146; Wideband FM Composite Video Fiber Optic Link, Philips Semiconductors 1985

A phase locked fiber optic system using FM modulation AN1434

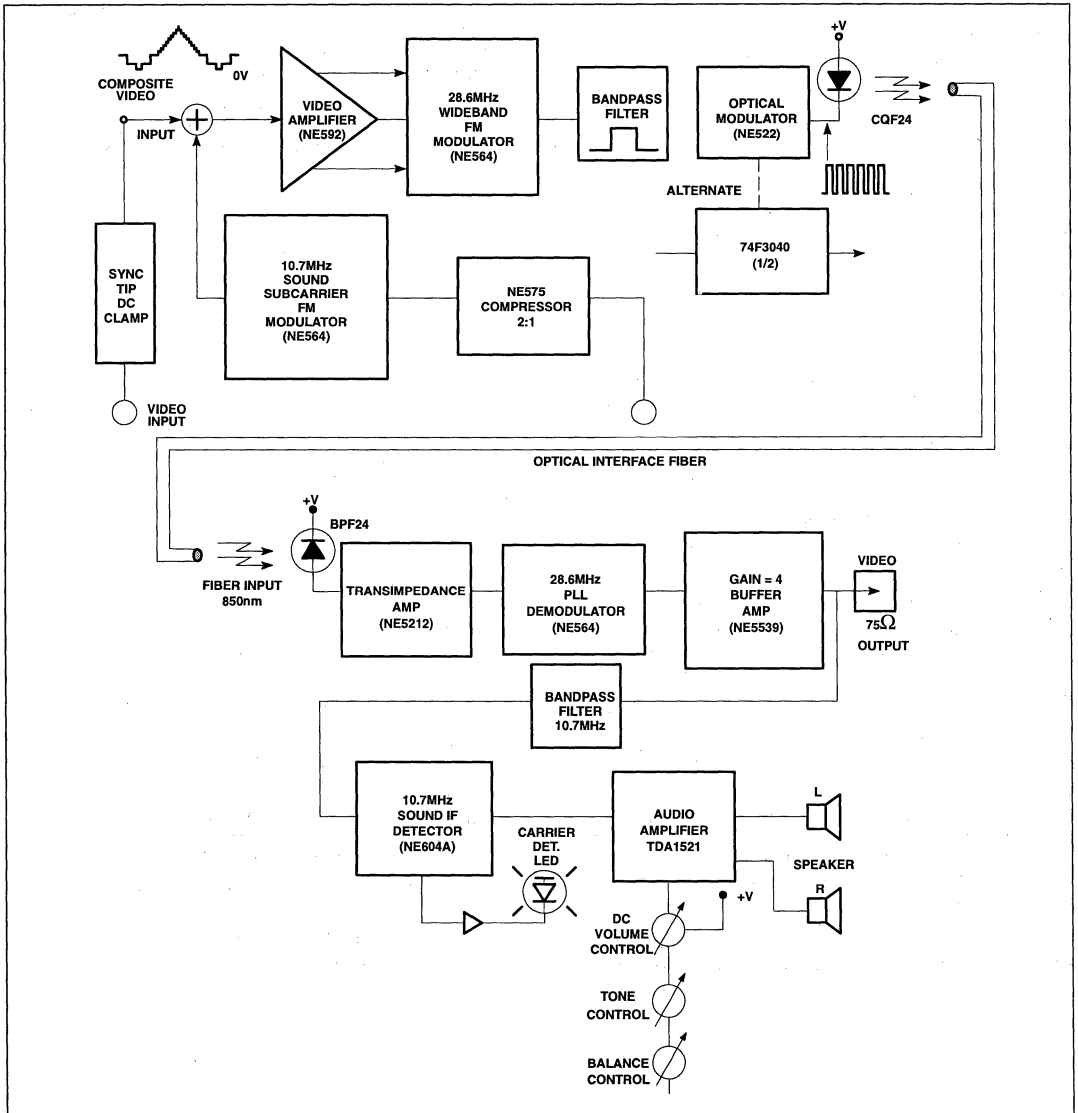
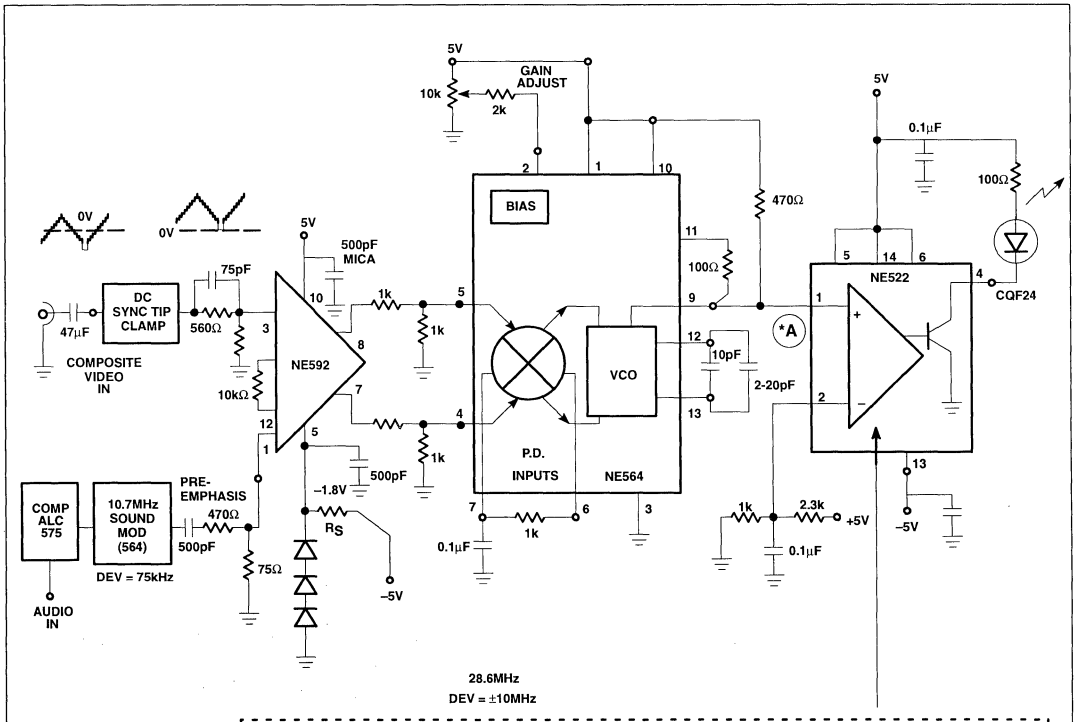


Figure 1. Video Fiber Transmission System

A phase locked fiber optic system using FM modulation AN1434



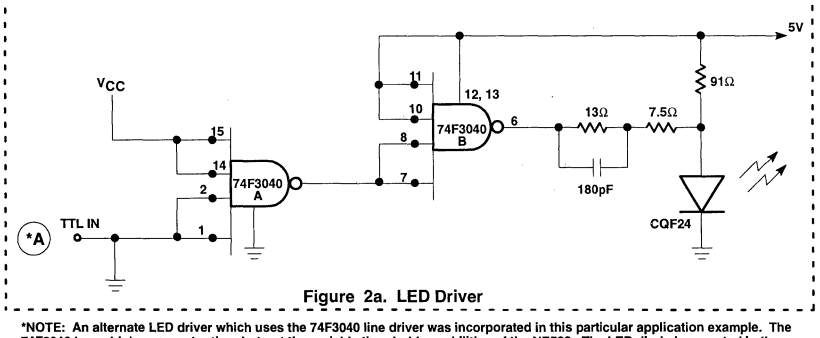


Figure 2a. LED Driver

*NOTE: An alternate LED driver which uses the 74F3040 line driver was incorporated in this particular application example. The 74F3040 has a higher current rating, but not the variable threshold capabilities of the NE522. The LED diode is operated in the saturated on-off mode for best signal-to-noise.

Figure 2. Fiber Optic Transmitter Block Diagram

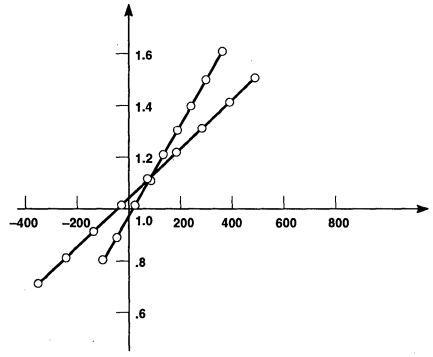


Figure 3. NE564 VCO Transfer Function, K_O

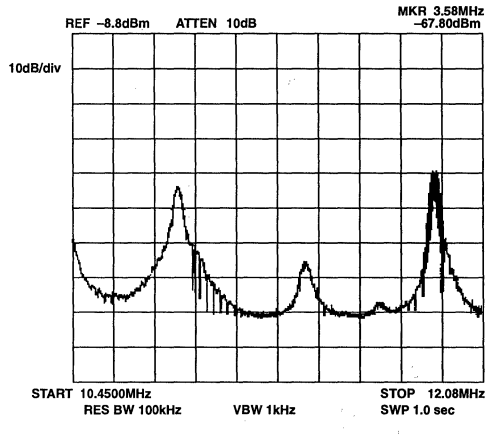


Figure 4. NE592 Output Signal NTSC Video Plus 10.7MHz Subcarrier (Probe 10X ATTN)

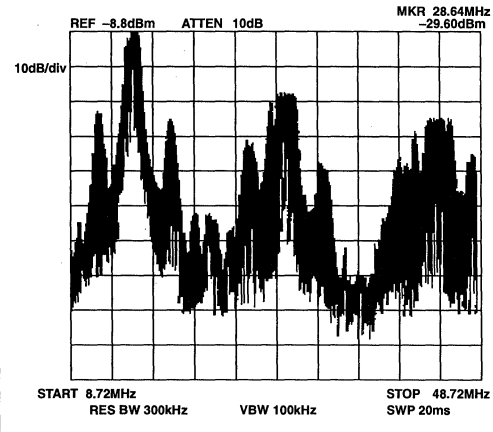


Figure 5. Transmitter PLL Output with NTSC Color Bar Test Pattern Input (Input Video -10dB Attenuation Below 1V Peak) (10X FET Probe at Pin 9 NE564)

A phase locked fiber optic system using FM modulation AN1434

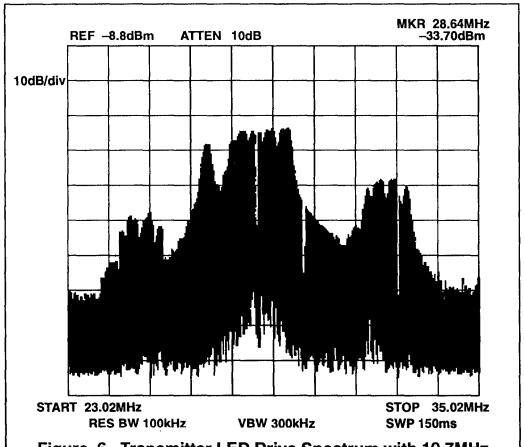


Figure 6. Transmitter LED Drive Spectrum with 10.7MHz Sound Subcarrier and NTSC Video Test Signal Input (10x ATTN)

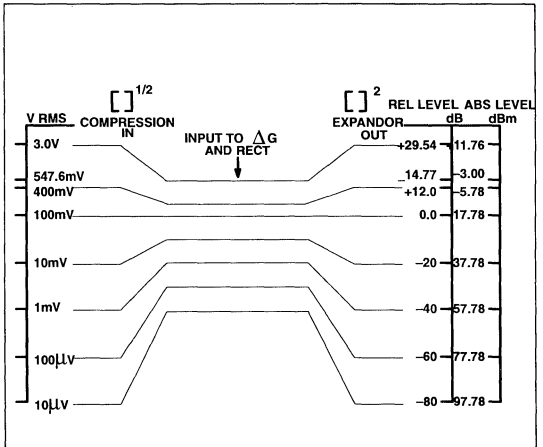


Figure 7. NE575 Compressor Transfer Function

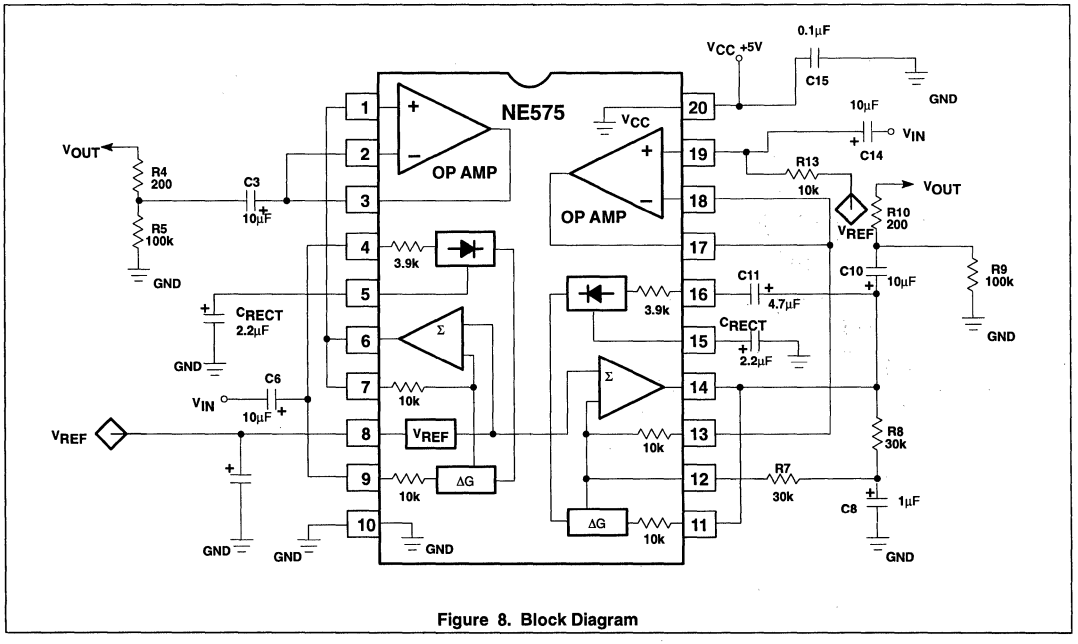


Figure 8. Block Diagram

A phase locked fiber optic system using FM modulation AN1434

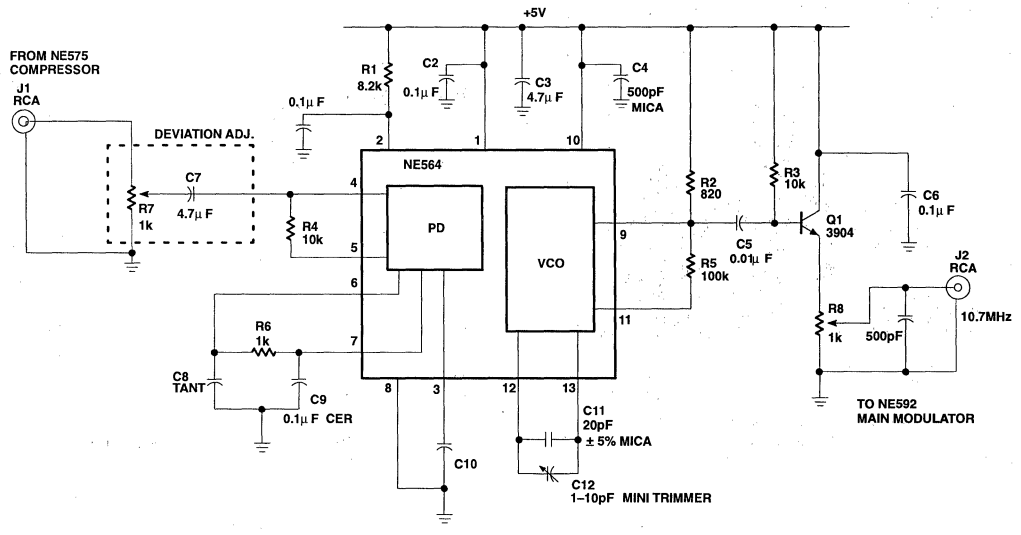


Figure 9. 10.7MHz Modulator

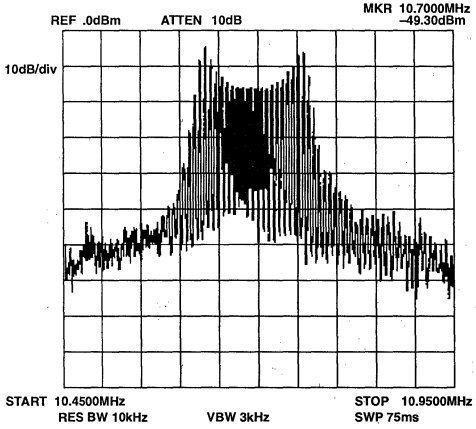


Figure 10. 10.7MHz Sound Subcarrier PLL Output with 1kHz Input After Compression (Probe 10x ATTN)

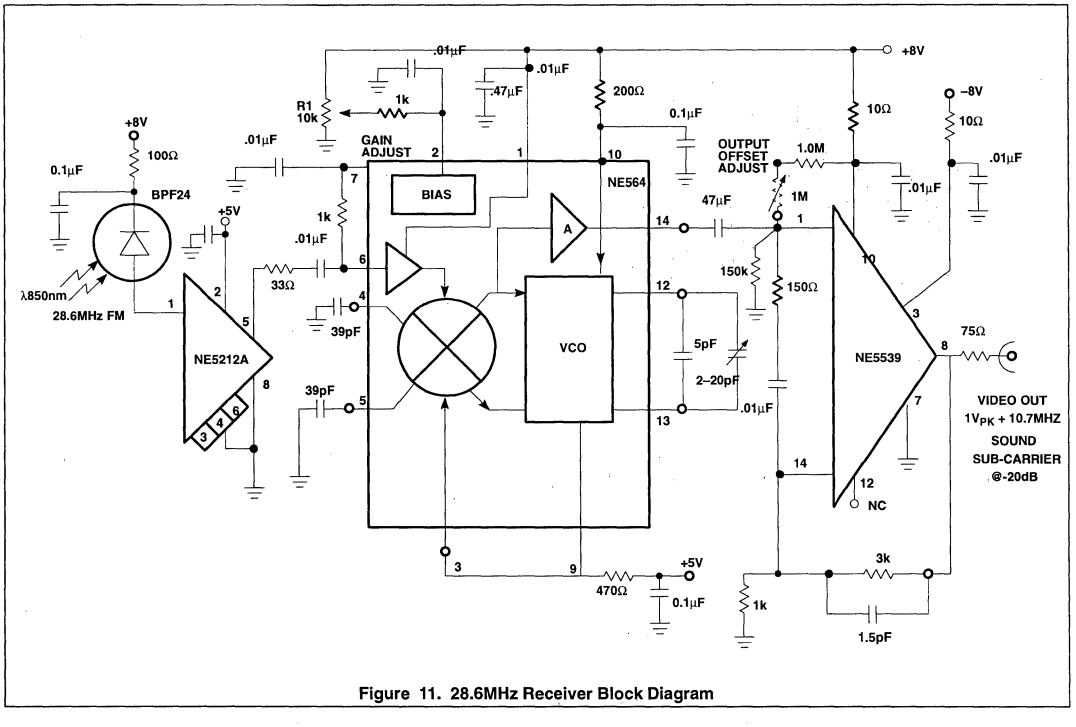


Figure 11. 28.6MHz Receiver Block Diagram

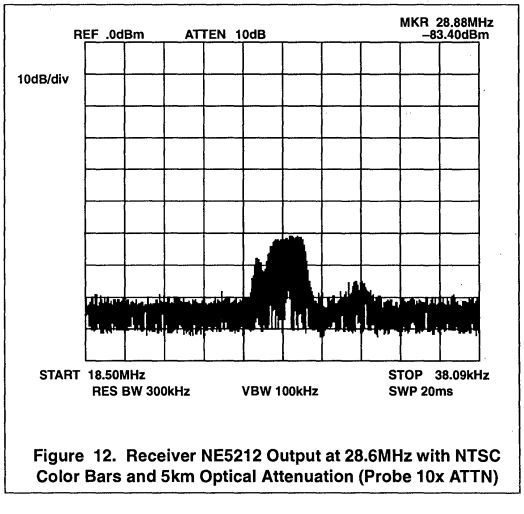


Figure 12. Receiver NE5212 Output at 28.6MHz with NTSC Color Bars and 5km Optical Attenuation (Probe 10x ATTN)

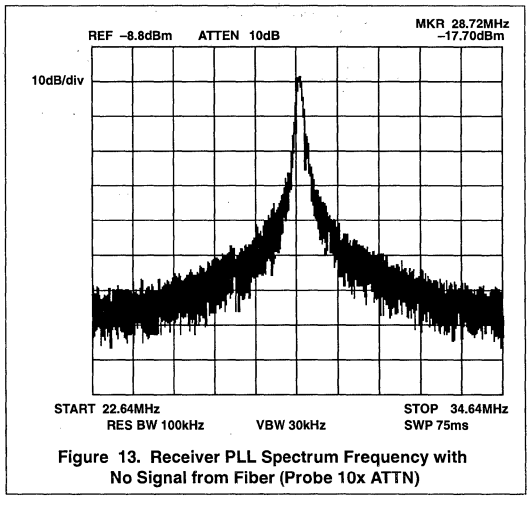


Figure 13. Receiver PLL Spectrum Frequency with No Signal from Fiber (Probe 10x ATTN)

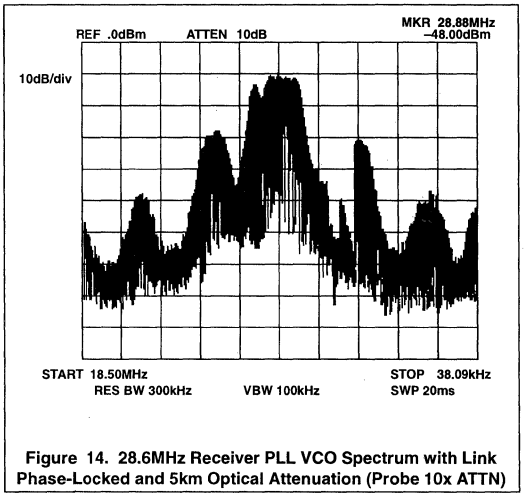


Figure 14. 28.6MHz Receiver PLL VCO Spectrum with Link Phase-Locked and 5km Optical Attenuation (Probe 10x ATTN)

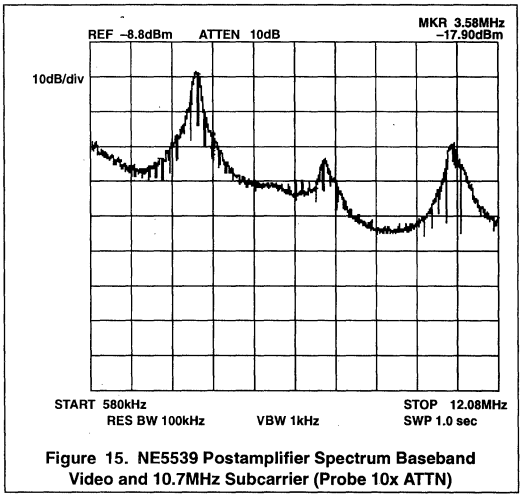


Figure 15. NE5539 Postamplifier Spectrum Baseband Video and 10.7MHz Subcarrier (Probe 10x ATTN)

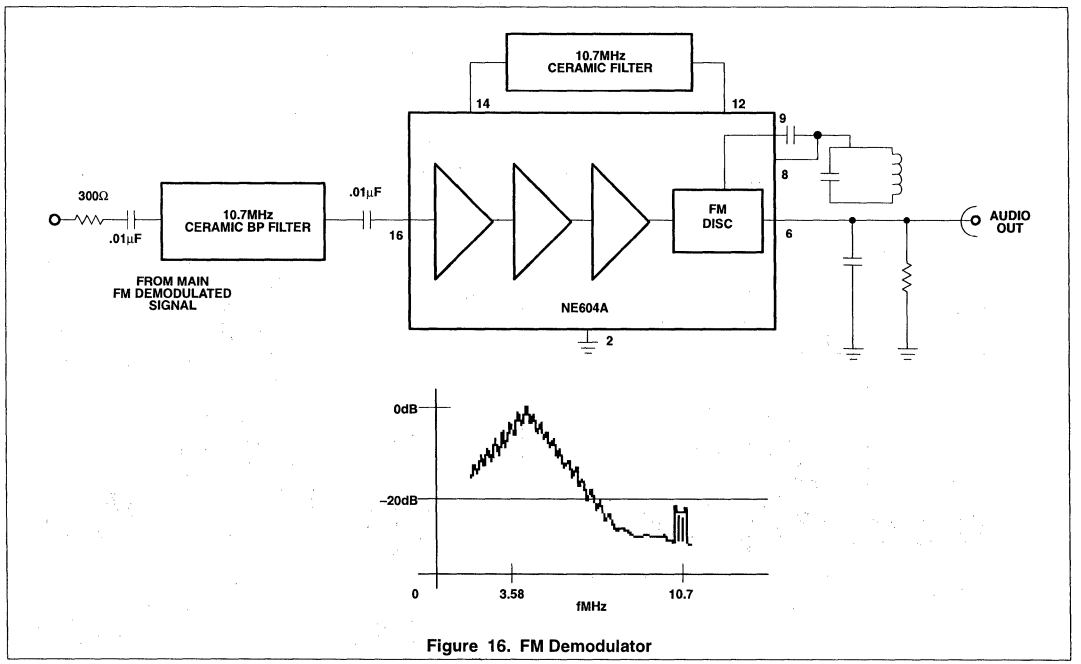


Figure 16. FM Demodulator

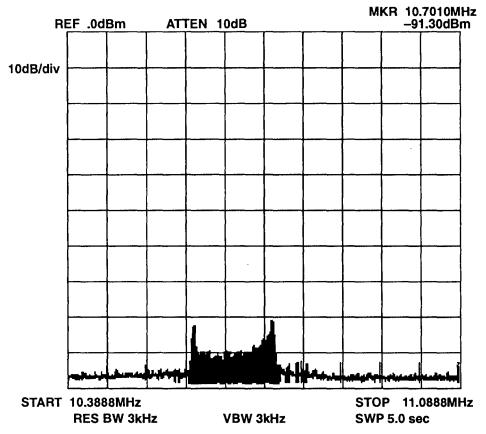


Figure 17. 10.7MHz Recovered Signal Input to FM IF Amplifier/Discriminator NE604A (Probe 10x ATTN)

Low cost, TTL fiber optic receivers for up to 100Mb/s NRZ — AN1443

Author: Michael J. Sedayao

INTRODUCTION

This application note describes circuits belonging to the receiver part of the Philips Semiconductors HiFI-100 (High-performance Fiber-optic Interface) Fiber Optic Chip Set. It should be noted that the performance of each board reflects the capabilities of the system along with its external components and does not represent the maximum capabilities of the individual Integrated Circuits. Performance may vary depending on layout and/or external component values.

Because of the advantages offered by fiber optics, such as high bandwidth, EMI immunity, light weight, etc, many users are switching from coaxial or twisted pair links to optical fiber. However, since most systems are not yet able to take full advantage of the data bandwidth of fiber (up to several Gb/s), users are looking for an inexpensive migration path to optical fiber. They would like to make the switch, but they want unit costs to be competitive with those of copper links. They also want enough flexibility so that if they want to increase their data rate, the upgrade costs in hardware would be minimal. The Philips Semiconductors HiFI-100 chip set lets users create inexpensive data links for transmission rates up to 100Mb/s NRZ (typical).

The HiFI-100 series comes in several flavors, each flavor describes a different combination of preamplifier and postamplifier. The most popular combinations are the HiFI-100A, HiFI-100B, and HiFI-100C. These are defined as follows:

Chip-Set	Preamp	Postamp
HiFI-100A	NE5211	NE5214
HiFI-100B	NE5210	NE5217
HiFI-100C	NE5211	NE5217
HiFI-100D	NE5212	NE5217

Each combination has its own advantages and disadvantages with respect to sensitivity, bandwidth and RZ or NRZ operation. Deciding which combination to use is the subject of the section on systems considerations. Experimental results on the HiFI-100C will be presented later.

System Considerations

Figure 1 shows a typical point-to-point fiber optic information channel. Assuming that the data was sent out on a parallel bus (8, 16, or 32-bits wide), it must be converted to a serial stream of data. At this point it may be encoded to optimize transmission. To reduce bandwidth, it may be changed from RZ to NRZ. To facilitate clock recovery it may be converted from NRZ to NRZI or Manchester, which would increase the bandwidth, so there are several trade-offs to consider. After the encoding stage, the signal goes to an electrical-to-optical converter. From there the information (as light) travels over the fiber medium. For lower speed applications, multi-mode fiber cables and LEDs of 850nm wavelengths are used. For higher bandwidth, longer distance applications, single-mode fiber is the cable of choice. For transmitting at these frequencies (up to several Gb/s), lasers and light of 1300nm or 1550nm are used .

On the receiving side, we have the reverse set up. An optical-to-electrical converter is used to raise the signal to either TTL or ECL levels. Also, the signal must be processed to recover the clock which had been embedded during the previous encoding stages. This recovered signal is then sent to the decoding section and then to the next logical section, serial-to-parallel conversion.

A Typical Fiber Optic Data Link

The domain of the HiFI-100 chip set covers the E/O, O/E and the clock recovery sections as shown in the blocks above. Figure 2 shows how this breaks down to functional blocks. In the transmitter, one block takes the serial, encoded signal and uses the signal to drive an LED. In the receiver, a photodiode accepts the light signal and converts it into a current which is then input to the preamplifier. This preamplifier converts the signal into a differential voltage which is then input to a postamplifier which shifts the signal to an appropriate logic level (TTL for the HiFI-100). The clock recovery section recovers the clock from the transitions in this signal, and then re-times the data for further processing.

The focus of this application note will be on the receiver section, excluding clock recovery. We will concentrate on the preamplifier and postamplifiers, and on the trade-offs involved with each combination.

Noise Considerations

The most important noise sources to consider are at the front end of the receiver since successive stages will only amplify whatever noise occurs here. The preamplifier is primarily concerned with two types of noise: that which comes from the preamplifier, itself, and the noise that comes onto the input current from the photodetector. Several publications provide detailed explanations of these effects.

Data Patterns

The type of data pattern input to the receiver will play a large role in determining the performance or sensitivity of the receivers. For the HiFI-100 series, the type of postamplifier chosen depends on the type of data pattern received. The following analysis will provide a guide to choosing the proper postamplifier.

The choice of preamplifier will be determined primarily by user requirements on sensitivity, noise, dynamic range and bandwidth. The tradeoffs associated with each of the three preamplifiers will be discussed in the preamplifier section.

To understand the types of data patterns being transmitted, Figure 3 shows the types of patterns considered. On the top row we have the data that we wish to transmit. Each '1' or '0' occupies a single bit cell. If we assume that a voltage level V+ corresponds to a logic '1 ' and that a level V- corresponds to a logic '0', the total swing is 2V.

Manchester

Manchester encoding is most often recognized by its regular transitions in the middle of each bit cell. A logic '1' is characterized by a low-to-high transition
in the middle of each cell while a logic '0' has a high-to-low transition. The advantage of Manchester is that the regular transitions make it ideal for clock recovery systems. One disadvantage is the bandwidth requirement. For a 50MHz system, it can transmit only 50Mb/s maximum. An equivalent NRZ system can transmit twice the number of bits, giving Manchester only 50% of the efficiency of NRZ.

Return-to-Zero (RZ)

The significance of RZ data is that for a logic '1' it stays high for the first half of the bit cell, but returns to the logic '0' level by the end of the bit cell. For logic '0' it stays at the zero level throughout the bit cell. For long strings of zeroes, the input signal resembles a DC-level, which would cause problems in AC coupled systems.

Non-Return-to-Zero (NRZ)

The major difference between NRZ and RZ is that the logic level stays the same throughout the bit cell. This means that the

Low cost, TTL fiber optic receivers for up to 100Mb/s NRZ AN1443

maximum transmission rate for the data in bits/sec is just twice the maximum frequency transmitted in Hz. For example, the highest frequency transmitted in a 100Mb/s NRZ system would be a 50MHz square wave. Potential problems with NRZ systems occur with long strings of ones and zeroes. These strings placed back-to-back look like low-frequency signals that could cause problems in AC-coupled systems. Because of the relative lack of transitions, clock recovery would also be more difficult.
NRZI is a variation of NRZ where a "1" is designed by either a low-to-high or high-to-low transition.

Low Frequency Operation

Low-frequency cut-off is another problem that could be considered data-dependent. This usually occurs in RZ or NRZ systems with long strings of ones or zeroes . For RZ, only the long strings of zeroes could cause problems. For NRZ, both logic states could introduce problems. Clearly, the larger the number of bit cells before a transition occurs, the more it looks like a low-frequency signal. For systems with Auto-Zero Loops (such as the NE5214 and NE5217), these lower frequency signals are rejected as input offset when they should be passed through as valid information. This is not to say that systems with Auto-Zero loops are bad because in cost sensitive applications, saving the cost and board space of an additional coupling capacitor (one Auto-Zero capacitor versus two coupling capacitors) is significant, and the AZ-loop takes out DC offsets that would be amplified.

In general, users should ask themselves what the lowest frequency possible sent will be given the transmitter's encoding scheme. Based upon this, they can then choose what value of Auto-Zero capacitor to use for sensing the lower-frequency pole or what value of coupling capacitors to use in an AC-coupled system.

AC-coupling

The advantage of AC-coupling when using components from different manufacturers is clear: it lets you use components that have different DC-bias levels. This is often the case when a user wants to mix and match different preamplifiers and postamplifiers because of the differences in their input and output bias levels.

Unfortunately, AC-coupling has its own set of disadvantages. The first would be component cost and space for the two capacitors needed. In hybrid applications where the physical dimensions of the data link is critical, this could pose a major problem. Another problem typically associated with low frequency pseudo-random data is baseline wander.

Looking at Figure 4, we have the same waveforms described above, but with their DC averages superimposed on them. With the transmitted data patterns, as the DC average (or baseline) wanders or moves, the switching threshold also moves. The problem occurs when this threshold moves away from the ideal point in the middle of the two logic states. For instance, if the threshold moves much closer to a logic '1', it needs much more voltage to switch to logic '1' if it was already in a logic '0' state. This corresponds to a degradation in the part's sensitivity. Conversely, if the threshold is much closer to a logic '1', any noise signal that may not have been large enough to change the state may do so now because of the decreased Signal-to-Noise Ratio.

Examining the individual waveforms, we can see that the Manchester waveform with its regular low-to-high and high-to-low transitions has almost zero baseline wander, making it the ideal data pattern for AC-coupled systems.

The RZ waveform has its baseline wander determined by the number of consecutive zeroes since each of the ones contain two successive transitions. The problem with NRZ is that, depending on encoding protocol, the baseline usually sits between zero and the midpoint giving a worse Signal-to-Noise ratio for the logic '0' condition.

The NRZ waveform has twice the problem that RZ has since the data sits at either extreme for both ones and zeroes. Again, depending on the encoding scheme, the baseline wander moves between both extremes and is the worst of the three cases examined. An additional problem is that the long ones and zeroes strings look more and more like lower-frequency signals presenting the same types of problems listed in the previous section.

An example of the effects on the sensitivity of each of the parts will be covered in the performance evaluation of the NE5211/ NE5217 combination.

Preamplifiers

Each of the preamplifiers that Philips Semiconductors offers is of the transimpedance type. The only difference in each is the available gain and bandwidth of the device. This lets the user mix and match preamplifiers and postamplifiers depending on his application. For a broader summary of the preamplifiers, see references 1 and 2.

NE5212

The NE5212 is the workhorse of the HiFI-100 preamplifiers. With 14kΩ of differential transresistance and 140MHz bandwidth, the NE5212 is suitable for most general purpose applications. With a low input noise current density of $2.5pA/\sqrt{Hz}$, it offers reliable operation with most photodiodes. The NE5212 is offered in 8-pin plastic, ceramic, and surface-mount packages. A more detailed description of the NE5212 is offered in reference 3 listed at the end of the article.

NE5211

The NE5211, with 28kΩ transresistance offers the highest sensitivity of any of the preamplifiers. It also has the lowest noise at $1.8pA/\sqrt{Hz}$. Because of the high gain, however, this part has the smallest dynamic range of the preamplifiers with a maximum input current of ±60μA.

NE5210

The NE5210 has the lowest transresistance, 7kΩ differential, of any of the preamplifiers, but it has the highest bandwidth of any preamplifier at 280MHz. Because of the lower transresistance, it has the largest dynamic range of the preamplifiers at ±240μA maximum input.

Postamplifiers

The function of the postamplifier is to take the small signals put out by the preamplifier and to square them up to proper levels so they can be interfaced with TTL. The postamplifier output is then usually sent to a clock recovery and data retiming section . Both postamplifiers in the HiFI-100 chip set, the NE5214 and NE5217, are designed for a minimum bandwidth of 60MHz and typical gain of about 60dB. The data sheet, however, is specified in two ways: one for the minimum sensitivity corresponding to a specific BER, and one for the minimum signal required to trigger the threshold according to certain combinations of R_{THRESH} and R_{HYST}.

The postamplifiers also provide a Signal Detect function, FLAG, that is also TTL compatible. When FLAG is HIGH it means that a signal below the preset threshold has been detected. When FLAG is LOW, it means that the signal detected is above the preset threshold level and is likely to be valid data.

Another function designed to work in conjunction with the FLAG is the JAM. The function of the JAM is to disable the forward path of the amplifier. This is important when the output is supposed to be quiet for signals below the threshold level. This is accomplished by connecting the FLAG output to the JAM input (TTL-compatible). If left unconnected, the JAM will float HIGH, disabling the amplifier's forward path. Therefore, if the FLAG/JAM combination is not desired, the JAM should be tied to ground.

The postamplifier also has an LED pin which offers a visual verification for the FLAG function. By tying the cathode of an LED to this pin through a current limiting resistor (100Ω is fine), you will get the following correspondence: FLAG(HIGH) = LED OFF and FLAG(LOW) = LED ON. Therefore, the LED OFF state represents a noisy condition at the postamp input.

For additional details on the functions in each postamplifier or to find out more detailed specifications, see Reference 5 and each respective data sheet.

NE5214 (Figure 5)

The NE5214 is a postamplifier designed for RZ or Manchester encoded operation. It has a typical bandwidth of 75MHz and comes in an SO-20 package. Distinguishing features are an optional interstage filter between input amplifier A1 and gated amplifier A2. If the filter is not used, Pins 13 and 14 may be shorted together along with Pins 15 and 16.

NE5217 (Figure 6)

The NE5217 is similar to the NE5214 except that it is designed for NRZ operation. The major difference between the NE5214 and NE5217 is that there is no interstage filter between A1 and A2, but the outputs of A2 and the inputs of the Schmitt Trigger A8 are pinned out so that coupling capacitors may be connected between A2 and A8. The coupling capacitors act like a differentiator, passing only the transitions of the incoming data. The Schmitt Trigger has 400mV of hysteresis to insure that the output comparator doesn't change state on noise spikes. The functions of the FLAG and JAM are unchanged.

Considerations for External Components

In our applications, we recommend using a100pF capacitor across the inputs as a low-pass filter to prevent high frequency noise signals from passing through to the output. This capacitor makes a significant (3dB min) improvement in sensitivity.

Auto-Zero Capacitor

The Auto-Zero Capacitor sets the low frequency pole for the input signal. This pole is determined by C_{AZ} as follows: $f_{-3dB} = 640 \times (2 \times \pi \times 1.6k\Omega \times C_{AZ})^{-1}$. The lowest frequency transmitted should be at least 10 times larger than this frequency if it is to be passed through the amplifier. Otherwise, it may be zeroed out by the Auto-Zero loop which functions as a DC to low-frequency feedback loop. For proper operation, the C_{AZ} must be large compared to the coupling capacitors C_{14} and C_{15}.

Coupling Capacitors C_{14} and C_{15} (NE5217)

The optimum value for capacitors C_{14} and C_{15} is 18pF. This has been verified by experiment. For minimal functionality of the part, the ratio between the Auto-Zero capacitor and the coupling capacitors should be a minimum of 250:1. With a 0.1µF capacitor and 18pF, this ratio is about 5500. For better performance, this ratio should be increased by increasing the Auto-Zero capacitor, not shrinking the coupling capacitor.

R_{THRESH} and R_{HYST}

These resistors set the threshold for the FLAG function and the amount of hysteresis built into FLAG function (not to be confused with the hysteresis of the Schmitt Trigger in the forward path). To find the appropriate resistor for your application, refer to the charts given in Figure 7.

R_{PEAK} and C_{PEAK}

R_{PEAK} and C_{PEAK} set the time constant used to determine how long it takes before the FLAG changes from a HIGH (signal absent) to a LOW (signal present). It comes from the following facts:

1.) C_{PEAK} (connected between pin and ground) is in parallel with an internal capacitor of 10pF.

2.) The time constant is proportional to the slew rate specified by $dV/dt = I_{PEAK}/C_{TOT}$, where $C_{TOT} = C_{PEAK} \parallel 10pF$.

3) I_{PEAK} is set by R_{PEAK} (connected between pin and V_{CC}) by the following formula: $I_{PEAK} = (V_{CC} - 0.8V) / (67.7k\Omega \parallel R_{PEAK})$.

Performance of the NE5211/5217 Receiver Combination

To verify some of the ideas presented in the system considerations section, one receiver combination, the HiFI-100C which consists of the NE5211 preamplifier along with the NE5217 postamplifier, had its sensitivity tested over several conditions. Variations were made with respect to frequency, data pattern, and external components. In each case, the sensitivity was measured such that the BER rate at that level of input power was 10^{-9}. The receiver tested used a Philips BPF-31 850nm photodetector as an optical front-end. A schematic of this combination is shown in Figure 8. The photodiode was mounted in an SMA-female connector, 2.5mm ferrule connector. The optical cables used to connect to the receiver were 62.5/125µm core/cladding multi-mode fiber terminated in an SMA-male connector.

CAUTION!

This board was designed for good isolation between V_{CC} and Ground to avoid feedback loops and potential oscillations for zero input signal conditions (optical cable not connected). To facilitate this, the top or component side of the board is surrounded by a ground plane. On the bottom side of the board are three V_{CC} sections: one for the photodiode and preamplifier, one for the analog section of the postamplifier, and one for the digital section of the postamplifier.

The danger posed by this situation is that if you wanted to probe the board for various waveforms, you would probably use a probe with an attached alligator-style ground clip. Your first impulse would be to attach this clip to the top and bottom of the board. DON'T DO THIS! This will short ground to any of the three V_{CC} sections and is likely to destroy either the photodiode or the NE5211 . If you need to do any probing, attach the ground clip to the ground posts on the top of the board. Of course, this is not a concern if you have one of the laminated boards.

Measurement Considerations

To make sure that we were measuring the forward amplification path of the postamplifier and were not shutting it down for specific threshold voltages, the JAM was disconnected from the FLAG and grounded to insure that the forward path was always active.

Data Patterns

We tested the receiver with three patterns: a square wave, a PRBS of 2^7-1, and a Pseudo Random Bit Sequence (PRBS) of 2^{23}-1 . Each signal transmitted was in NRZ mode so that for a 50MHz clock

signal, the maximum data rate transmitted would be 25MHz. A square wave was used to test the zero baseline wander case and to approximate Manchester code. PRBS=2^7-1 was used as a moderate test of baseline wander, since there could be no more than 7 consecutive ones or zeroes. PRBS=2^{23}-1 was used to approximate some extreme cases of baseline wander by having a maximum of 23 consecutive ones or 22 consecutive zeroes. Harsher baseline wander conditions would occur by using burst-type signals with greater amounts of DC in the signal. Burst data will be discussed in more detail later.

Frequency

The frequencies tested were f_{CLOCK} = 1, 2, 4, 8, 10, 20, 40, 80,100, and 200MHz. Since these were transmitted via NRZ, they correspond to a maximum f_{DATA} = 0.5,1, 2, 4, 8,10, 20, 40, 80, and 100Mb/s respectively. For the minimum frequency signal in each case, take the corresponding f_{DATA} and divide by 7 or 23 depending on which PRBS is used. Of course, for a square wave there is only one frequency transmitted, f_{DATA}.

Sensitivity

For sensitivity values to be meaningful, optical power must be converted to input current for the preamplifier and then into differential volts for the postamplifier. To do this, certain parameters are needed. First of all, the photodiodes responsivity must be considered. As an example, find the voltage input to the postamplifier that corresponds to an input optical power of -33dBm. To find the power in watts, we realize, by definition, that -33dBm is equal to 10 x log (P_{OUT}/P_{IN}) where P_{IN} is 1mW. This gives us P_{OUT} = 500nW. The photodiode's responsivity is R = 0.35Amps/Watt. So multiplying through we get the input current to the preamplifier I_{IN} = P_{OUT} x R = 175nA. To find what differential voltage at the output of the preamplifier is, we can multiply the input current by the differential transimpedance of the NE5211, TZ = 28kΩ. So, V_{DIFF} = I_{IN} x TZ = 4.9mV_{P-P}. This is just a typical value calculation. To find the full range of sensitivity, temperature and voltage variations must be considered.

Bit-Error Rate

Another thing to be considered is how does this input signal compare with the Bit-Error Rate? For the NE5211, the input noise current is 1.8pA/$Hz^{1/2}$. To find out what the Signal-to-Noise Ratio (SNR) is,we have to find what the actual noise current is based upon the density. Suppose that the signal measured in the previous paragraph was taken at 60MHz. The square root of this gives 7.75x$10^3$$Hz^{1/2}$. Multiplying the two together gives a noise current of 13.9nA. The SNR would then be 138nA/ 13.9nA = 12.6 or 22.0dB. Using a chart in Figure 9 from reference 4, we note that this roughly corresponds to a BER between 10^{-6} and 10^{-7}. So, we can conclude that for a desired BER of 10^{-9}, the power level is too low. You can also work backwards, finding the minimum power level needed for a specified BER.

For accuracy, each measurement was tested with at least 3x10^{10} bits. For a desired BER of 10^{-9}, this gives us an accuracy of (1 - [(10^{-9}) x (3x10^{10})]$^{-1}$) x 100 = 96.7%. Of course, for more accuracy more bits could be sent but the time needed to test the receiver would grow accordingly.

Results

Figure 10 shows the results for board A, where the Auto-Zero capacitor to coupling capacitor ratio is 1:1 . This is clearly the worst case. The square wave gives us the best sensitivity because it has the least amount of baseline wander. The next best sensitivity is for PRBS=2^7-1 because of the seven consecutive ones and zeroes in the pattern. The worst case is for PRBS = 2^{23}-1 which has lower frequency components which are not even passed for values lower than 8MHz regardless of the strength of the input. As expected for the pseudo-random sequences, the sensitivity goes down as the frequency goes down, as the low frequency components of the PRBS data stream are cancelled out by the Auto-Zero loop.

Figure 11 shows case B where the capacitor ratio has increased to 1000. We get significant improvements for the PRBS = 2^{23}-1 case, but not too much more for the other two data patterns.

Figure 12 shows case C which has increased the ratio even more, to 10,000, by increasing C_{AZ} to 1μF. This improves the performance of PRBS = 2^{23}-1 even more. It should be noted that the sensitivity in all cases (A, B, and C) goes down beyond 80MHz because of the natural -3dB roll-off of the postamplifier. It appears that the best operation is around 20MHz for these particular external components.

Figure 13 shows how boards A, B, and C performed for a square-wave input. Judging by the y-axis scale, there is no appreciable difference in either of the cases for this type of input.

Figure 14 shows how boards A, B, and C performed for an input of PRBS = 2^7-1 . C offers the best performance at lower frequencies.

Figure 15 shows an interesting comparison of how board C (with C_{14} = C_{15} =100pF) performs compared with the capacitors shorted (the equivalent of the NE5214). Board C is consistently 2 to 3dB better at frequencies lower than 20MHz.

Figure 16 shows the performance of boards A, B, and C along with board C using 18pF coupling capacitors for an input of PRBS = 2^{23}-1. The 18pF value performs better at more points than the 100pF value and is thus chosen as our optimum coupling capacitor value. (Values lower than 18pF actually degraded the sensitivity.)

Burst Data Transmission

One of the most difficult types of data to transmit is so-called "burst" or "bursty" data. Burst data can best be described as a pulse or series of pulses followed by a long period of no transitions. The problem caused by burst data is clearly the lack of transitions in the data stream. For DC-coupled, Auto-Zero loops, a forced high or low voltage would not cause problems. In DC-coupled, Auto-Zero systems, as the length of the not transition or "dead time" increases, the likelihood that the signal will be canceled out by the Auto-Zero loop increases. This will result in bit side errors being transmitted. In AC-coupled systems, this causes a drift to the DC-bias levels on either side of the capacitor, usually resulting once again in bit errors. It is for this reason that many encoding schemes require a minimum number of transitions per parallel word.

However, other types of faults may look like burst data transmission which should be recognized as some type of error condition. For instance, if the link is cut off for some reason and no data gets through, should this be recognized as a zero or a one? In an AC-coupled system, how would the receiver distinguish between a broken link which balances the inputs versus a long series of ones or zeroes? More often than not, a coding scheme designed to flag after a certain amount of time of no transitions or a SIGNAL DETECT function that would respond only to DC signals would have to be implemented.

One receiver, an NE5210/NE5217 combination was tested under burst-data conditions. Two data patterns were used. The first pattern used had twelve 40ns pulses or 11 and a half cycles of 25MHz square wave cycled over 2048 pulses of the same size (2048x40ns = 81.92μs for a 12.207kHz repetition rate). The duty

cycle for the pulse burst is (12x2/pulses)/2048 pulses = 1.17% or 11,719ppm. This input signal burst is shown in Figure 17 (top trace). The output trace (output of NE5217) is shown in the bottom trace. In this configuration, the FLAG output is connected to the JAM input. This presents a problem.

Because the JAM function is implemented at the A2 amplifier and not at the gate, a charge is stored on the coupling capacitors to the Schmitt Trigger, C14 and C15 "freezing" the output in the logic '1' state for 100ns before it changes state to zero, 60ns longer than it should be.

To see if this problem is at all related to the number of pulses transmitted or to the burst repetition rate, a worst-case testing was attempted by sending a single 40ns pulse at a repetition rate of 24 pulses = 24x40ns = 960ns or 1.04MHz. This gave us a duty cycle of 1/24 = 4.17%. The output is shown in Figure 18. The JAM is still connected to FLAG and the FLAG signal is shown in the top trace. Note that the part can only transmit through the A2 amplifier when FLAG = JAM is low. During the no-transition periods, the part considers it to be a loss of signal. This would be the same case as if the input were cut off as a result of a break in the link. The middle trace has the TX input and the bottom trace shows the pulse stretched output similar to the previous output trace.

To check performance independent of the state of FLAG/JAM, we tried the same thing but with the JAM grounded. In Figure 19, we see that JAM grounded in the top trace. In the middle trace we have the input signal. It is inverted in this instance because of a trigger change. The output of the NE5217 is shown in the bottom trace with no evidence of the pulse stretching. To verify the performance, we took this signal and measured it to a sensitivity of -24.5dBm optical with 850nm light to a BER of $\leq 10^{-9}$ (measured with a minimum of $3x10^{10}$ bits). If we used an NE5211 we might expect performance around -30dBm to -32dBm.

If transmission of burst data is a necessity and the FLAG function is essential, you could JAM the part externally with an OR gate. When no signal/no transition is the case, the FLAG would be high and the output would always be HIGH. With the FLAG LOW (signal present), you would get whatever the NE5217 output is. This is shown in Figure 20.

REFERENCES

1. "A Wide-Band Low-Noise Monolithic Transimpedance Amplifier", by Robert G. Meyer and Robert A. Blauschild, Journal of Solid State Circuits, Volume SC-21, Number 4, pg 530, August 1986.

2. "Optical Fiber Communications", by John M. Senior, Prentice-Hall International Series in Optoelectronics, 1985.

3. "A Low Cost 100MBaud Fiber Optic Receiver", by William D. Mack, Robert G. Meyer, and Ki. Y. Suh, Philips Semiconductors Company, presented at FOC/LAN (Fiber Optic Communications/ Local Area Networks), October 1987.

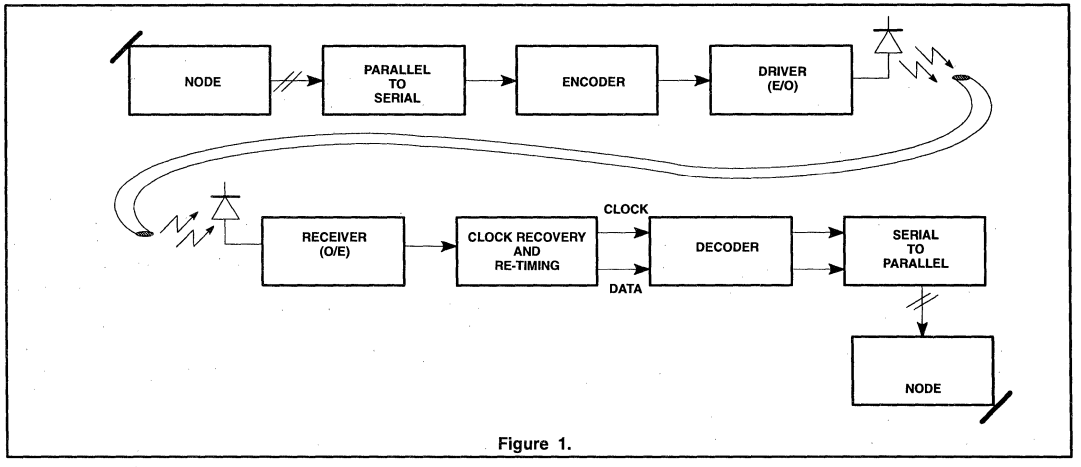


Figure 1.

Low cost, TTL fiber optic receivers for up to 100Mb/s NRZ AN1443

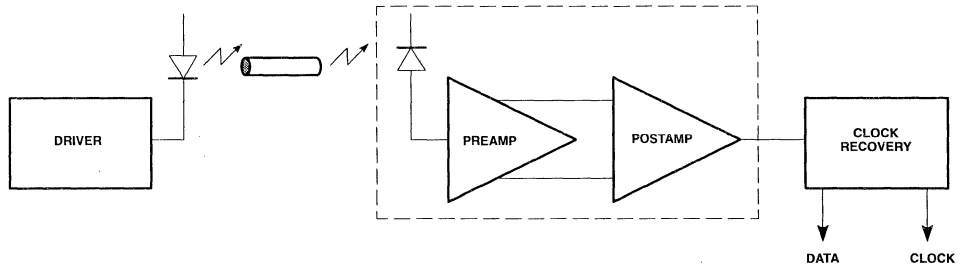


Figure 2.

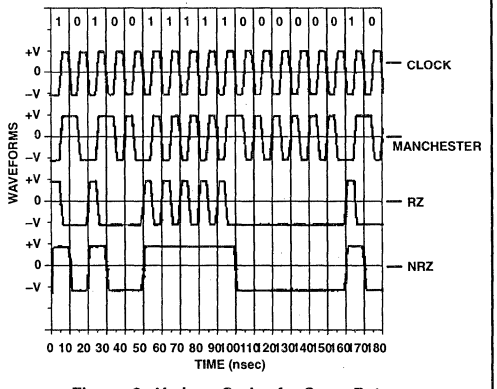


Figure 3. Various Codes for Same Data

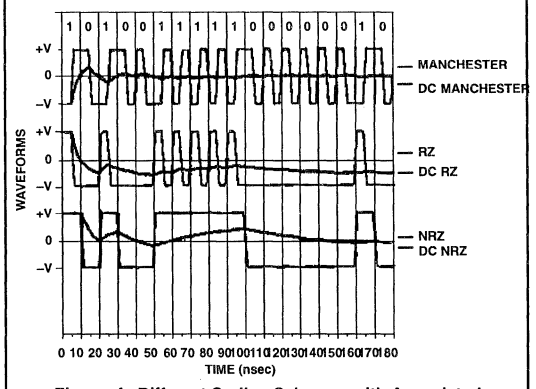


Figure 4. Different Coding Schemes with Associated DC Averages; Baseline Wander is from 0.

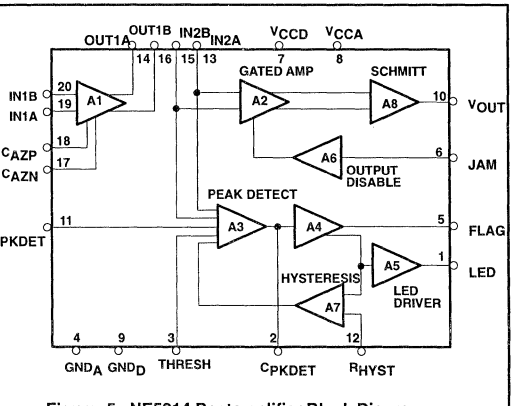


Figure 5. NE5214 Postamplifier Block Diagram

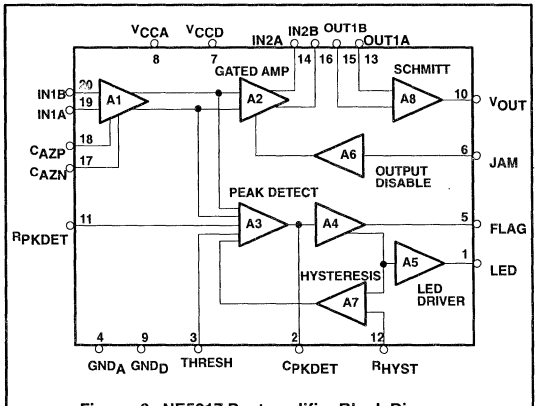


Figure 6. NE5217 Postamplifier Block Diagram

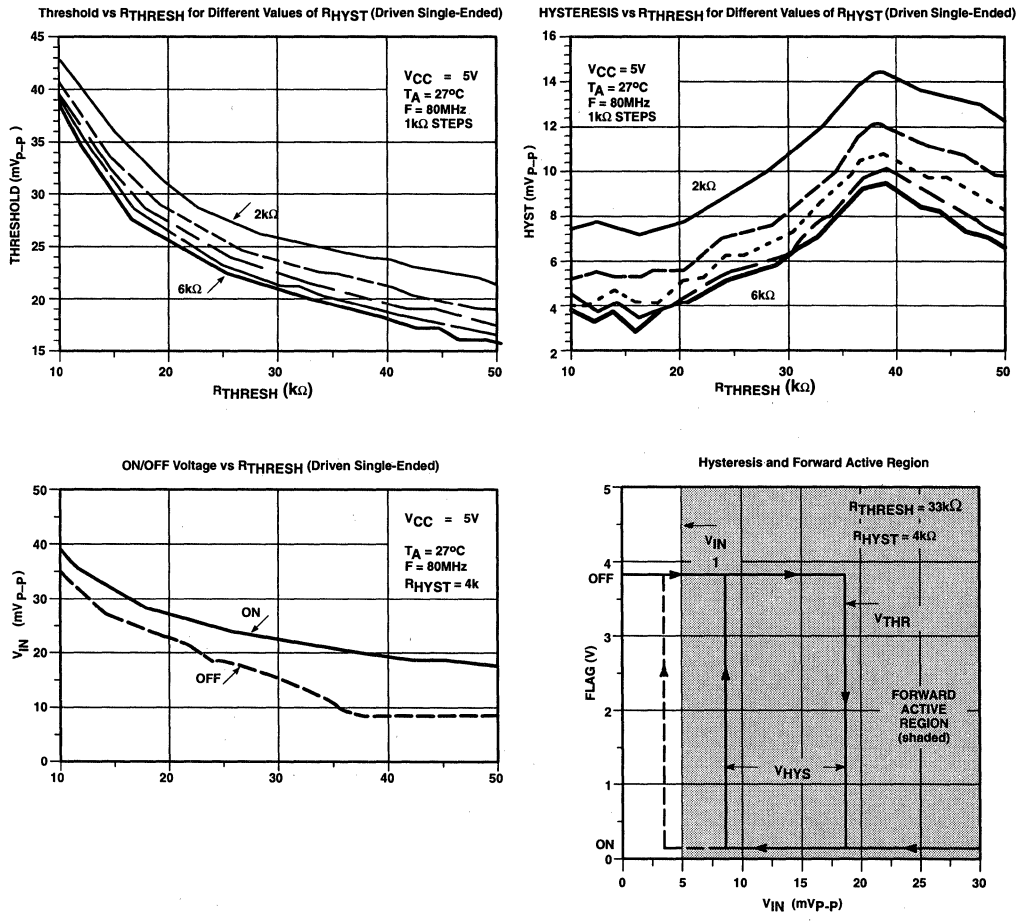
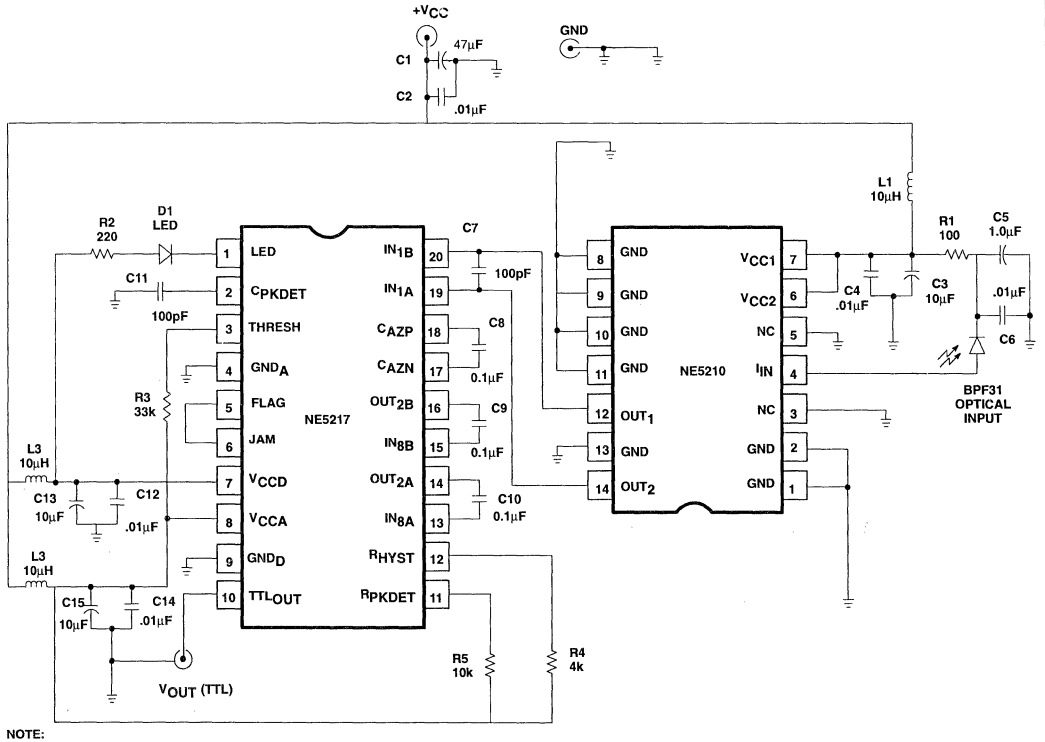


Figure 7. Typical Performance Characteristics

Low cost, TTL fiber optic receivers for up to 100Mb/s NRZ AN1443



NOTE:
THE NE5210/NE5217 combination can operate at data rates in excess of 100Mb/s NRZ

Figure 8. A 50Mb/s Fiber Optic Receiver

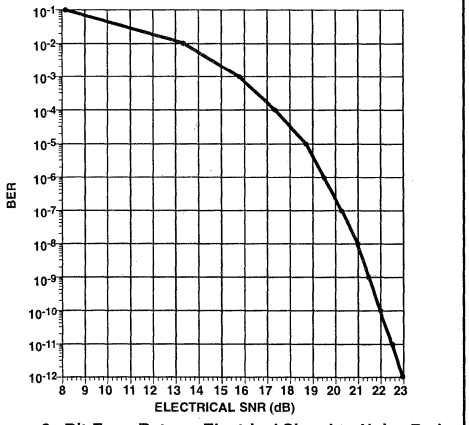


Figure 9. Bit-Error Rate vs Electrical Signal-to-Noise Ratio

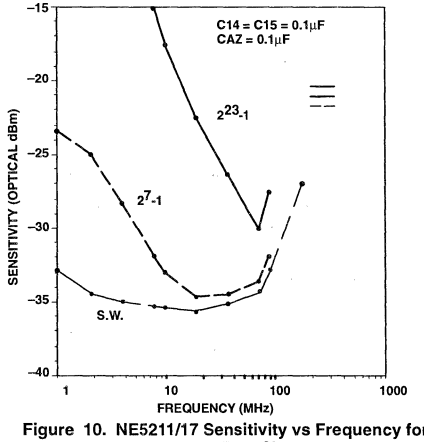


Figure 10. NE5211/17 Sensitivity vs Frequency for Square Wave, 2^7-1, 2^{23}-1 Patterns

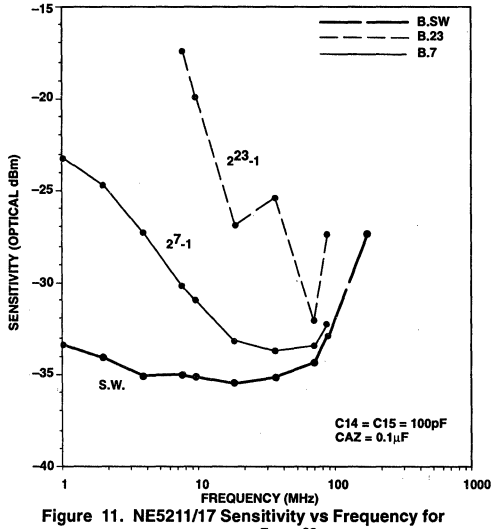


Figure 11. NE5211/17 Sensitivity vs Frequency for Square Wave, 2^7-1, 2^{23}-1 Patterns

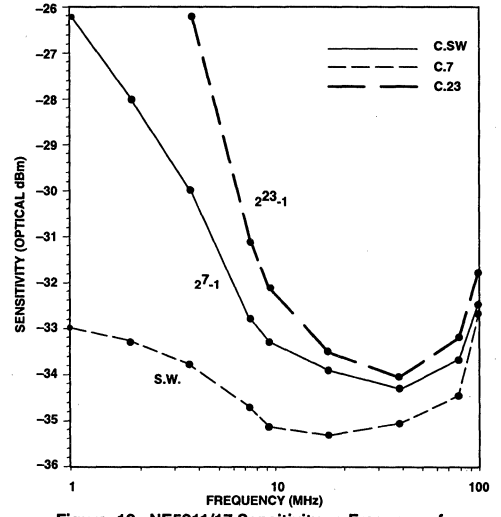


Figure 12. NE5211/17 Sensitivity vs Frequency for Square Wave, 2^7-1, 2^{23}-1 Patterns

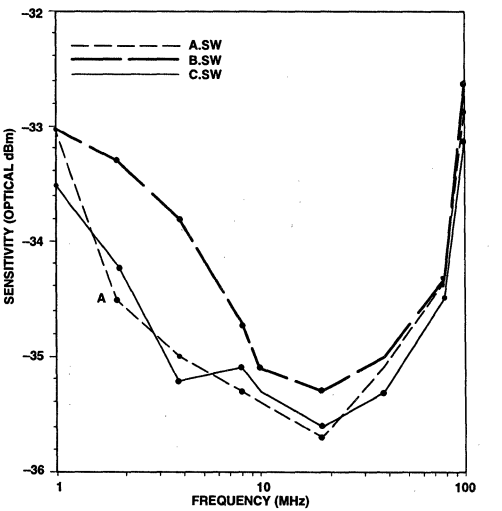


Figure 13. Optical Sensitivity versus Frequency for Square Wave Input (Configurations A, B, C)

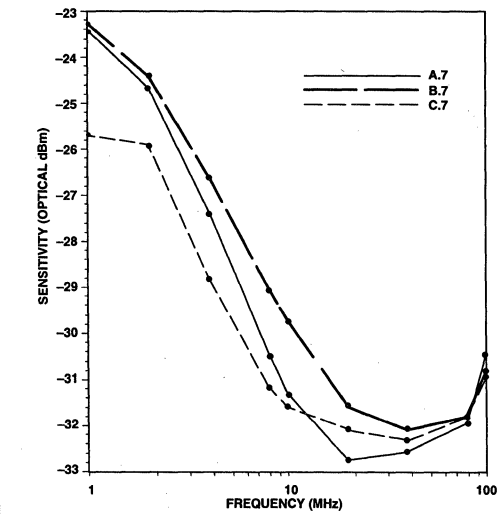


Figure 14. NE5211/17 Sensitivity vs Frequency for PRBS = 2^7-1, Input (Configurations A, B, C)

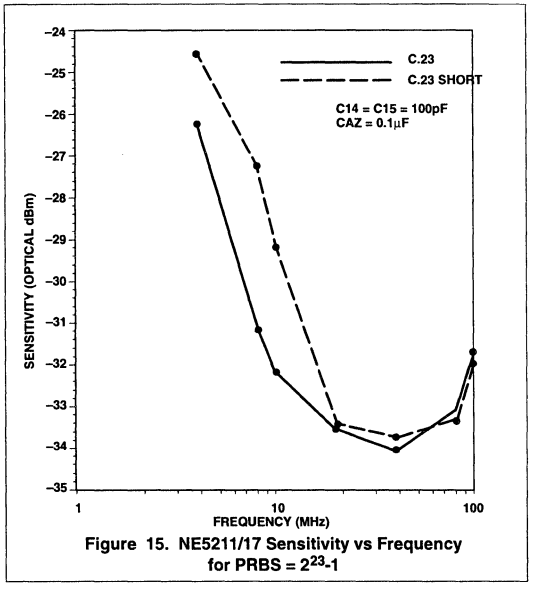


Figure 15. NE5211/17 Sensitivity vs Frequency for PRBS = 2^{23}-1

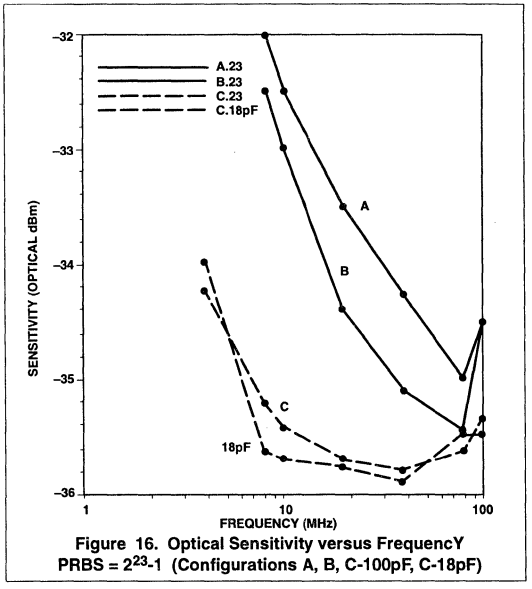


Figure 16. Optical Sensitivity versus FrequencY PRBS = 2^{23}-1 (Configurations A, B, C-100pF, C-18pF)

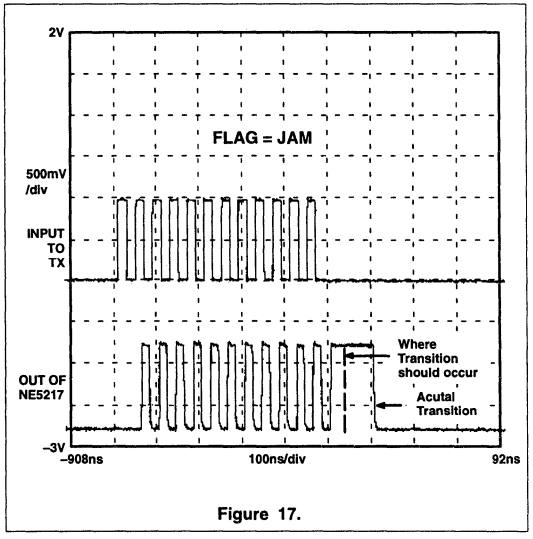


Figure 17.

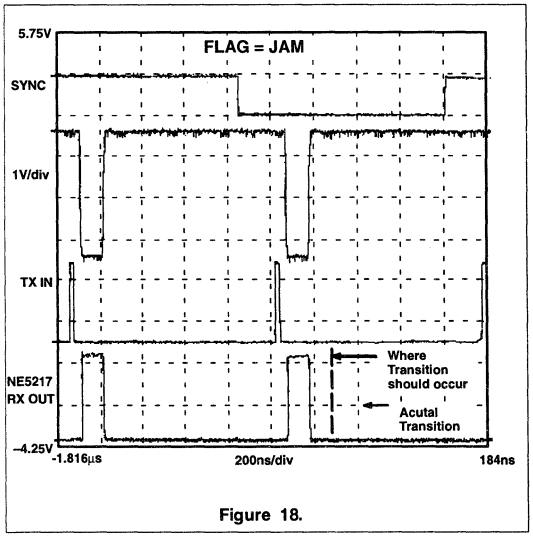


Figure 18.

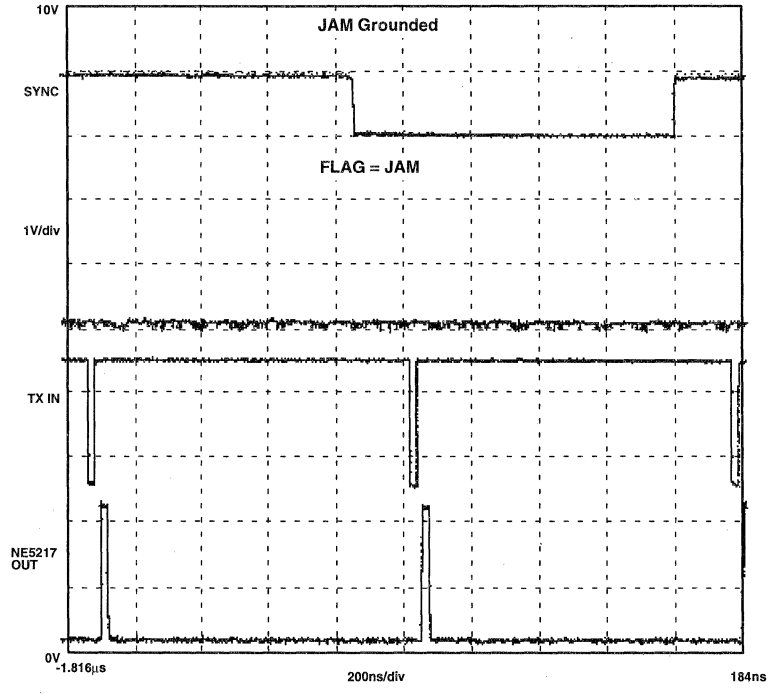
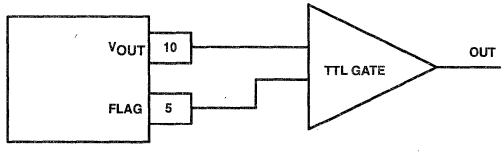


Figure 19.



	VOUT	FLAG	OUT
SIGNAL PRESENT	0	0	0
	1	0	1
SIGNAL ABSENT	0	1	1
	1	1	1

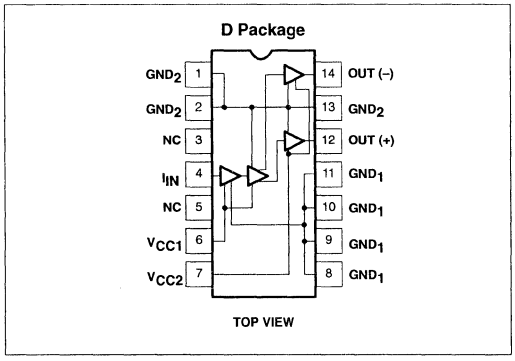
Figure 20. Externally Jamming Part

Transimpedance amplifier (280MHz) NE5210

DESCRIPTION

The NE5210 is a 7kΩ transimpedance wide band, low noise amplifier with differential outputs, particularly suitable for signal recovery in fiber-optic receivers. The part is ideally suited for many other RF applications as a general purpose gain block.

PIN CONFIGURATION



FEATURES

- Low noise: 3.5pA/√Hz
- Single 5V supply
- Large bandwidth: 280MHz
- Differential outputs
- Low input/output impedances
- High power supply rejection ratio
- High overload threshold current
- Wide dynamic range
- 7kΩ differential transresistance

APPLICATIONS

- Fiber-optic receivers, analog and digital
- Current-to-voltage converters
- Wideband gain block
- Medical and scientific instrumentation
- Sensor preamplifiers
- Single-ended to differential conversion
- Low noise RF amplifiers
- RF signal processing

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE5210D	0175D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply	6	V
T_A	Operating ambient temperature range	0 to +70	°C
T_J	Operating junction temperature range	-55 to +150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
P_{DMAX}	Power dissipation, T_A=25°C (still air)[1]	1.0	W
I_{INMAX}	Maximum input current[2]	5	mA

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance: θ_{JA}=125°C/W.
2. The use of a pull-up resistor to V_{CC} for the PIN diode, is recommended.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	4.5 to 5.5	V
T_A	Ambient temperature range	0 to +70	°C
T_J	Junction temperature range	0 to +90	°C

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over operating temperature range at V_{CC}=5V, unless otherwise specified. Typical data applies at V_{CC}=5V and T_A=25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IN}	Input bias voltage		0.6	0.8	0.95	V
$V_{O\pm}$	Output bias voltage		2.8	3.3	3.7	V
V_{OS}	Output offset voltage			0	80	mV
I_{CC}	Supply current		21	26	32	mA
I_{OMAX}	Output sink/source current[1]		3	4		mA
I_{IN}	Input current (2% linearity)	Test Circuit 8, Procedure 2	±120	±160		µA
I_{INMAX}	Maximum input current overload threshold	Test Circuit 8, Procedure 4	±160	±240		µA

NOTES:
1. Test condition: output quiescent voltage variation is less than 100mV for 3mA load current.

AC ELECTRICAL CHARACTERISTICS

Typical data and Min/Max limits apply at V_{CC}=5V and T_A=25°C.

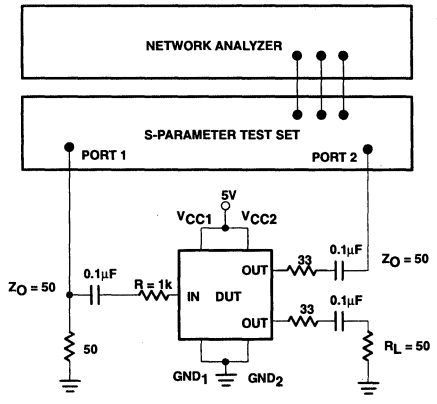
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
R_T	Transresistance (differential output)	DC tested, R_L=∞ Test Circuit 8, Procedure 1	4.9	7	10	kΩ
R_O	Output resistance (differential output)	DC tested	16	30	42	Ω
R_T	Transresistance (single-ended output)	DC tested, R_L=∞	2.45	3.5	5	kΩ
R_O	Output resistance (single-ended output)	DC tested	8	15	21	Ω
f_{3dB}	Bandwidth (-3dB)	Test Circuit 1, T_A=25°C	200	280		MHz
R_{IN}	Input resistance			60		Ω
C_{IN}	Input capacitance			7.5		pF
ΔR/ΔV	Transresistance power supply sensitivity	V_{CC}=5±0.5V		9.6	20	%/V
ΔR/ΔT	Transresistance ambient temperature sensitivity	$\Delta T_A = T_{A\,MAX} - T_{A\,MIN}$		0.05	0.1	%/°C
I_N	RMS noise current spectral density (referred to input)	f=10MHz, T_A=25°C Test Circuit 2		3.5	6	pA/√Hz
I_T	Integrated RMS noise current over the bandwidth (referred to input) C_S=0[1]	T_A=25°C Test Circuit 2				nA
		Δf=100MHz		37		
		Δf=200MHz		56		
		Δf=300MHz		71		
	C_S=1pF	Δf=100MHz		40		
		Δf=200MHz		66		
		Δf=300MHz		89		
PSRR	Power supply rejection ratio[2] (V_{CC1}=V_{CC2})	DC tested, ΔV_{CC}=0.1V Equivalent AC test circuit 3	20	36		dB
PSRR	Power supply rejection ratio[2] (V_{CC1})	DC tested, ΔV_{CC}=0.1V Equivalent AC test circuit 4	20	36		dB
PSRR	Power supply rejection ratio[2] (V_{CC2})	DC tested, ΔV_{CC}=0.1V Equivalent AC test circuit 5		65		dB
PSRR	Power supply rejection ratio[2] (ECL configuration)	f=0.1MHz, Test Circuit 6		23		dB

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OMAX}	Maximum output voltage swing differential	R_L=∞ Test Circuit 8, Procedure 3	2.4	3.2		V_{P-P}
V_{INMAX}	Maximum input amplitude for output duty cycle of 50±5%[3]	Test Circuit 7	650			mV_{P-P}
t_R	Rise time for 50 mV_{P-P} output signal[4]	Test Circuit 7		0.8	1.2	ns

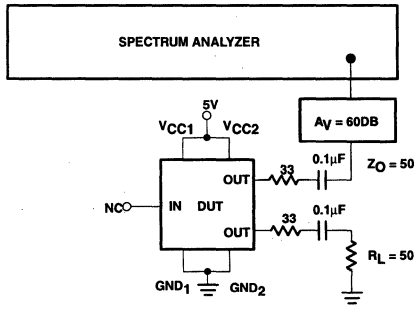
NOTES:
1. Package parasitic capacitance amounts to about 0.2pF
2. PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use RF filter in V_{CC} line.
3. Guaranteed by linearity and overload tests.
4. t_R defined as 20-80% rise time. It is guaranteed by a -3dB bandwidth test.

TEST CIRCUITS



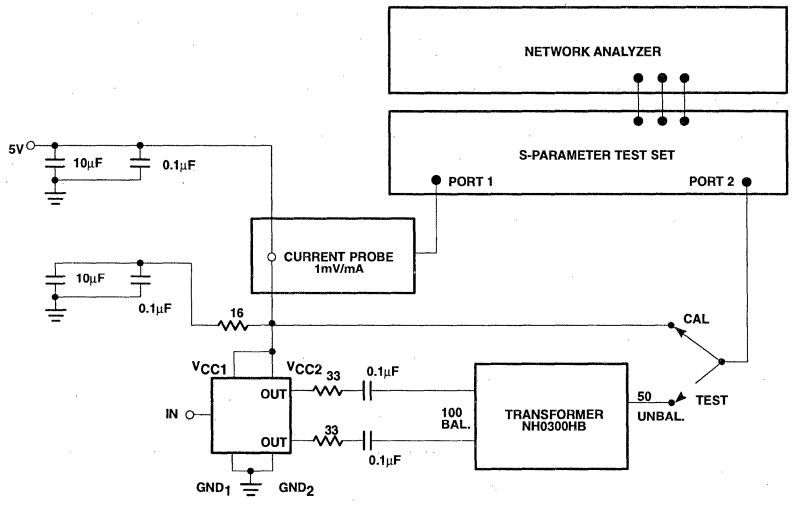
SINGLE-ENDED	DIFFERENTIAL
$R_T \approx \frac{V_{OUT}}{V_{IN}} R = 2 \cdot S21 \cdot R$	$R_T = \frac{V_{OUT}}{V_{IN}} R = 4 \cdot S21 \cdot R$
$R_O \approx Z_O \frac{\lvert 1 + S22 \rvert}{\lvert 1 - S22 \rvert} - 33$	$R_O = 2Z_O \frac{\lvert 1 + S22 \rvert}{\lvert 1 - S22 \rvert} - 66$

Test Circuit 1

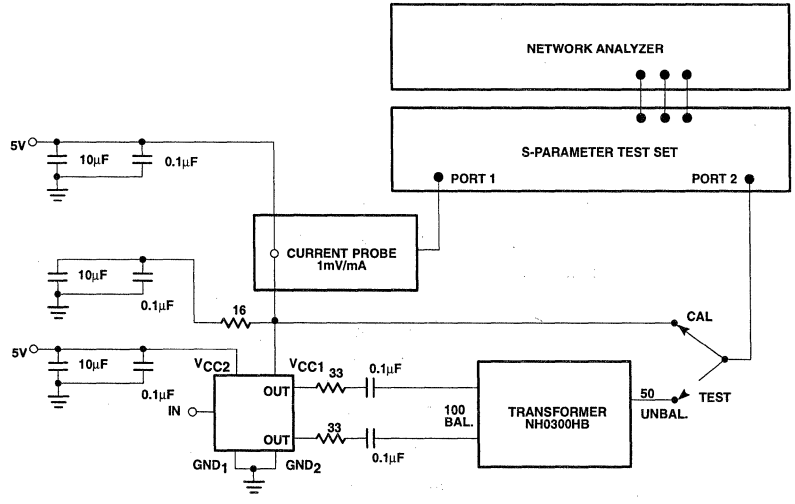


Test Circuit 2

TEST CIRCUITS (Continued)

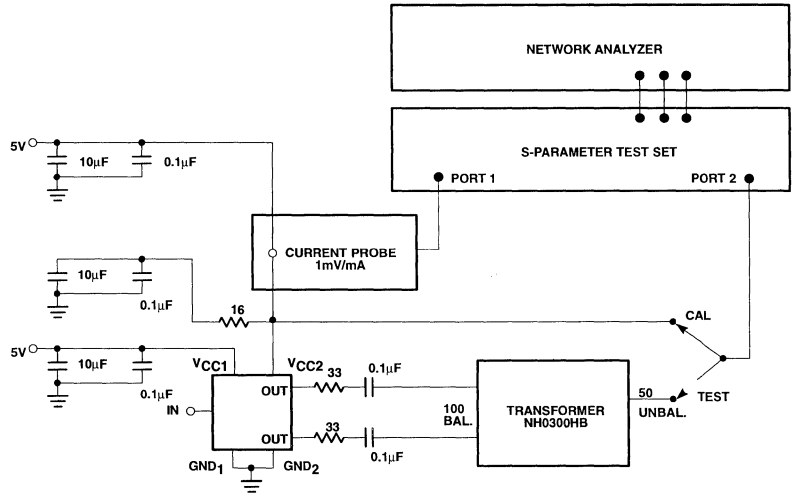


Test Circuit 3



Test Circuit 4

TEST CIRCUITS (Continued)



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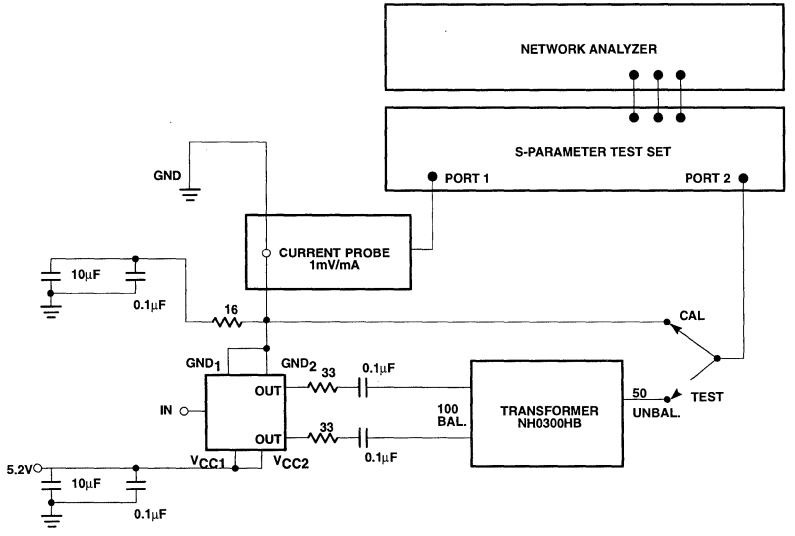
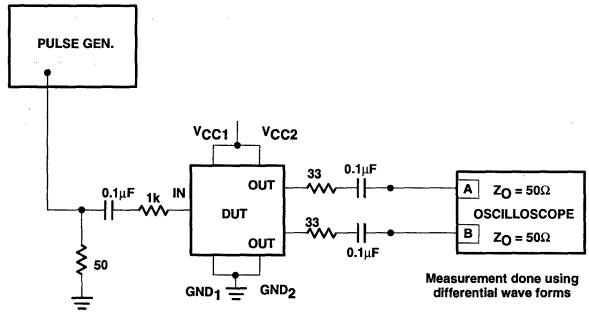


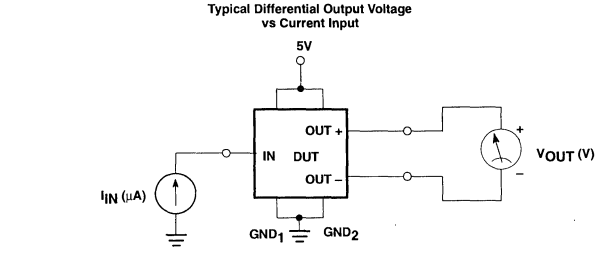
Test Circuit 6

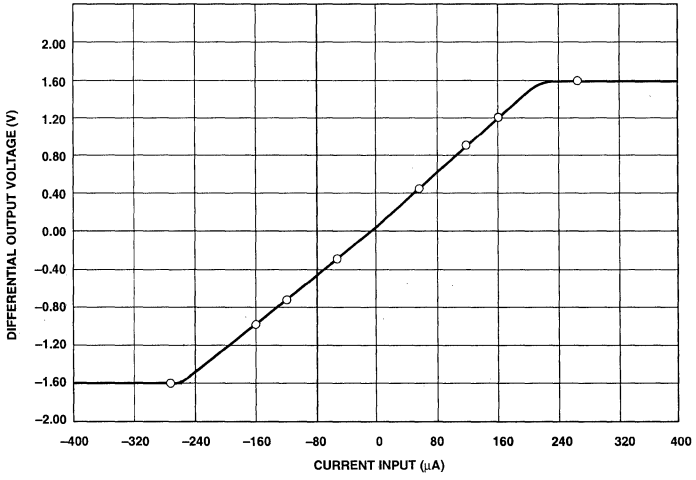
TEST CIRCUITS (Continued)



Test Circuit 7

TEST CIRCUITS (Continued)





NE5210 TEST CONDITIONS

Procedure 1

R_T measured at 60μA
$R_T = (V_{O1} - V_{O2})/(+60\mu A - (-60\mu A))$
Where: V_{O1} Measured at I_{IN} = +60μA
V_{O2} Measured at I_{IN} = –60μA

Procedure 2

Linearity = 1 – ABS(($V_{OA} - V_{OB}$) / ($V_{O3} - V_{O4}$))
Where: V_{O3} Measured at I_{IN} = +120μA
V_{O4} Measured at I_{IN} = –120μA
$V_{OA} = R_T \cdot (+ 120\mu A) + V_{OB}$
$V_{OB} = R_T \cdot (- 120\mu A) + V_{OB}$

Procedure 3

$V_{OMAX} = V_{O7} - V_{O8}$
Where: V_{O7} Measured at I_{IN} = +260μA
V_{O8} Measured at I_{IN} = –260μA

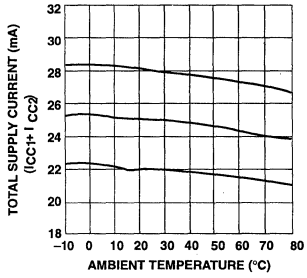
Procedure 4

I_{IN} Test Pass Conditions:
$V_{O7} - V_{O5} > 20mV$ and $V_{O6} - V_{O5} > 20mV$
Where: V_{O5} Measured at I_{IN} = +160μA
V_{O6} Measured at I_{IN} = –160μA
V_{O7} Measured at I_{IN} = +260μA
V_{O8} Measured at I_{IN} = –260μA

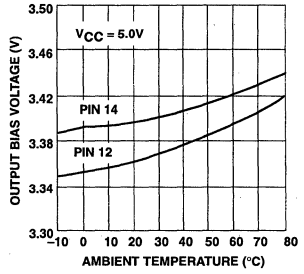
Test Circuit 8

TYPICAL PERFORMANCE CHARACTERISTICS

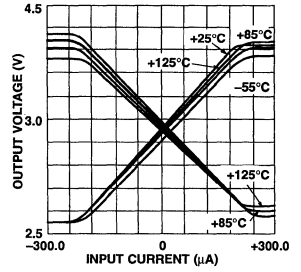
NE5210 Supply Current vs Temperature



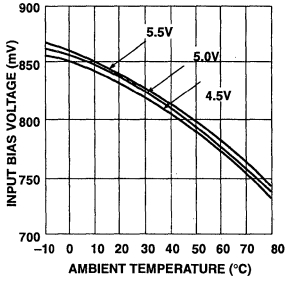
NE5210 Output Bias Voltage vs Temperature



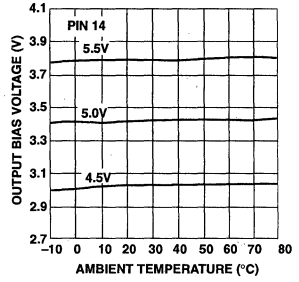
Output Voltage vs Input Current



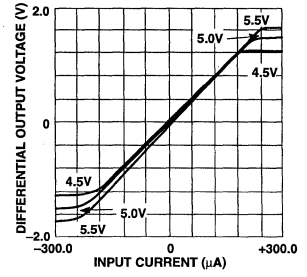
NE5210 Input Bias Voltage vs Temperature



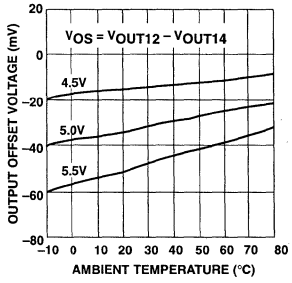
NE5210 Output Bias Voltage vs Temperature



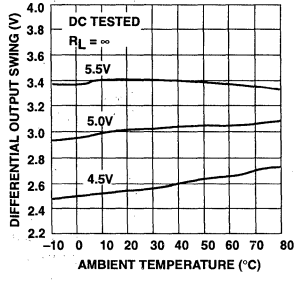
Differential Output Voltage vs Input Current



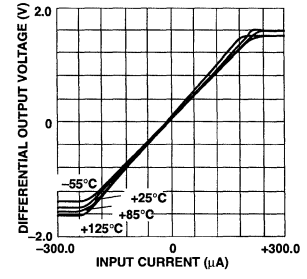
NE5210 Output Offset Voltage vs Temperature



NE5210 Differential Output Swing vs Temperature

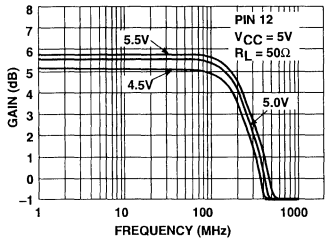


Differential Output Voltage vs Input Current

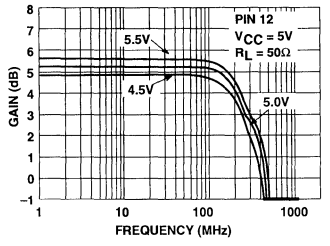


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

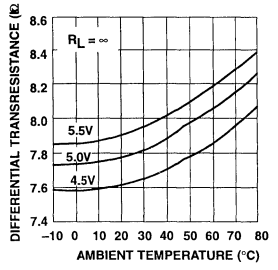
Gain vs Frequency



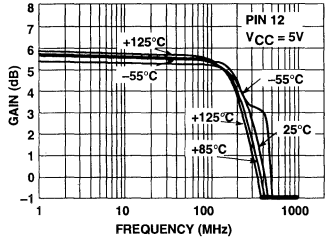
Gain vs Frequency



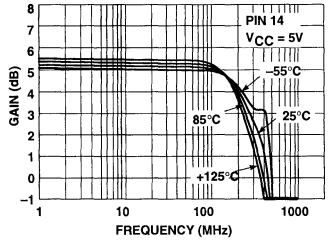
NE5210 Differential Transresistance vs Temperature



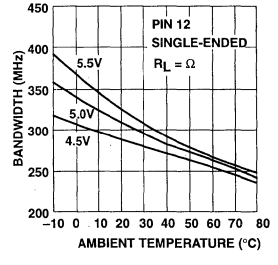
Gain vs Frequency



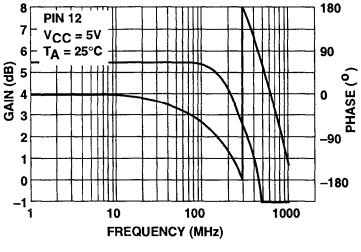
Gain vs Frequency



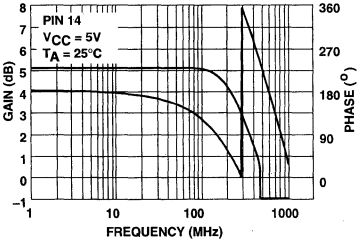
NE5210 Bandwidth vs Temperature



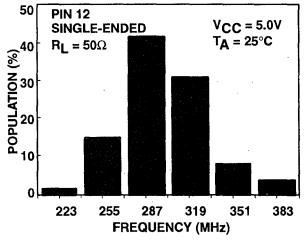
Gain and Phase Shift vs Frequency



Gain and Phase Shift vs Frequency

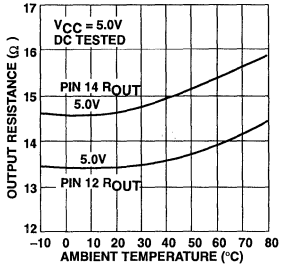


NE5210 Typical Bandwidth Distribution (70 Parts from 4 Wafer Lots)

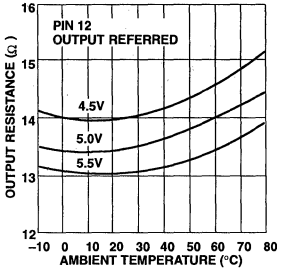


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

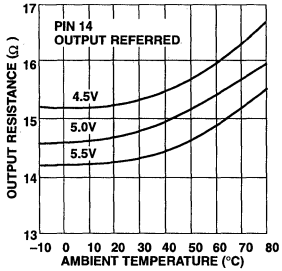
NE5210 Output Resistance vs Temperature



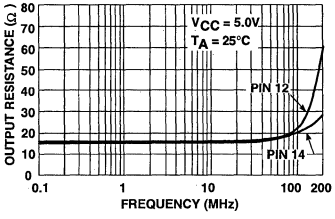
NE5210 Output Resistance vs Temperature



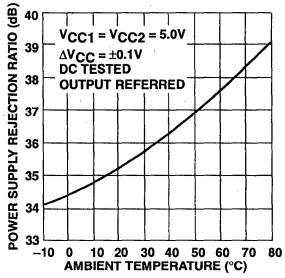
NE5210 Output Resistance vs Temperature



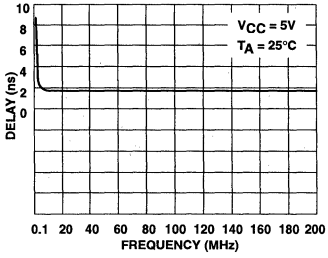
Output Resistance vs Frequency



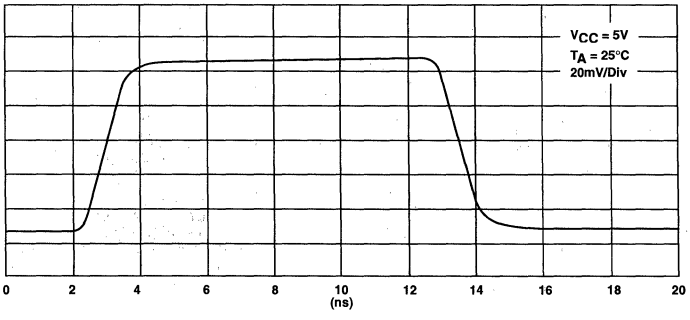
NE5210 Power Supply Rejection Ratio vs Temperature



Group Delay



Output Step Response



Transimpedance amplifier (280MHz) NE5210

THEORY OF OPERATION

Transimpedance amplifiers have been widely used as the preamplifier in fiber-optic receivers. The NE5210 is a wide bandwidth (typically 280MHz) transimpedance amplifier designed primarily for input currents requiring a large dynamic range, such as those produced by a laser diode. The maximum input current before output stage clipping occurs at typically 240μA. The NE5210 is a bipolar transimpedance amplifier which is current driven at the input and generates a differential voltage signal at the outputs. The forward transfer function is therefore a ratio of the differential output voltage to a given input current with the dimensions of ohms. The main feature of this amplifier is a wideband, low-noise input stage which is desensitized to photodiode capacitance variations. When connected to a photodiode of a few picoFarads, the frequency response will not be degraded significantly. Except for the input stage, the entire signal path is differential to provide improved power-supply rejection and ease of interface to ECL type circuitry. A block diagram of the circuit is shown in Figure 1. The input stage (A1) employs shunt-series feedback to stabilize the current gain of the amplifier. The transresistance of the amplifier from the current source to the emitter of Q_3 is approximately the value of the feedback resistor, R_F=3.6kΩ. The gain from the second stage (A2) and emitter followers (A3 and A4) is about two. Therefore, the differential transresistance of the entire amplifier, R_T is

$$R_T = \frac{V_{OUT}(diff)}{I_{IN}} = 2R_F = 2(3.6K) = 7.2k\Omega$$

The single-ended transresistance of the amplifier is typically 3.6kΩ.

The simplified schematic in Figure 2 shows how an input current is converted to a differential output voltage. The amplifier has a single input for current which is referenced to Ground 1. An input current from a laser diode, for example, will be converted into a voltage by the feedback resistor R_F. The transistor Q1 provides most of the open loop gain of the circuit, A_{VOL}≈70. The emitter follower Q_2 minimizes loading on Q_1. The transistor Q_4, resistor R_7, and V_{B1} provide level shifting and interface with the $Q_{15} - Q_{16}$ differential pair of the second stage which is biased with an internal reference, V_{B2}. The differential outputs are derived from emitter followers $Q_{11} - Q_{12}$ which are biased by constant current sources. The collectors of $Q_{11} - Q_{12}$ are bonded to an external pin, V_{CC2}, in order to reduce the feedback to the input stage. The output impedance is about 17Ω single-ended. For ease of performance evaluation, a 33Ω resistor is used in series with each output to match to a 50Ω test system.

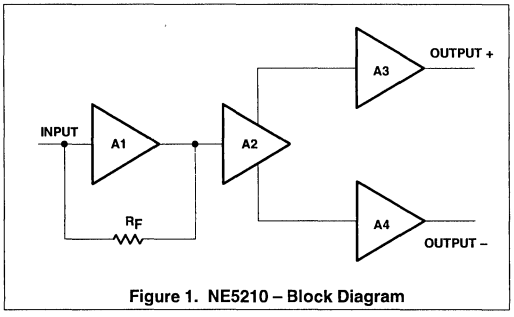


Figure 1. NE5210 – Block Diagram

BANDWIDTH CALCULATIONS

The input stage, shown in Figure 3, employs shunt-series feedback to stabilize the current gain of the amplifier. A simplified analysis can determine the performance of the amplifier. The equivalent input capacitance, C_{IN}, in
parallel with the source, I_S, is approximately 7.5pF, assuming that C_S=0 where C_S is the external source capacitance.

Since the input is driven by a current source the input must have a low input resistance. The input resistance, R_{IN}, is the ratio of the incremental input voltage, V_{IN}, to the corresponding input current, I_{IN} and can be calculated as:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}} = \frac{3.6K}{71} = 51\Omega$$

More exact calculations would yield a higher value of 60Ω.

Thus C_{IN} and R_{IN} will form the dominant pole of the entire amplifier;

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Assuming typical values for R_F = 3.6kΩ, R_{IN} = 60Ω, C_{IN} = 7.5pF

$$f_{-3dB} = \frac{1}{2\pi\ 7.5pF\ 60} = 354MHz$$

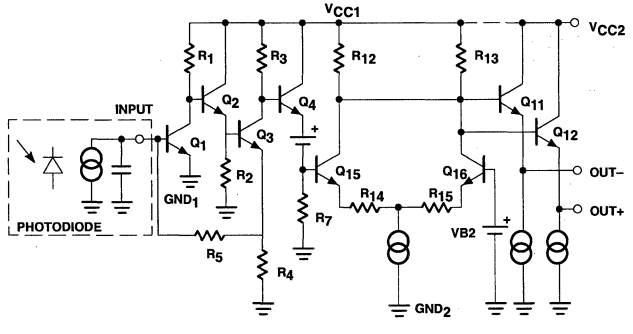


Figure 2. Transimpedance Amplifier

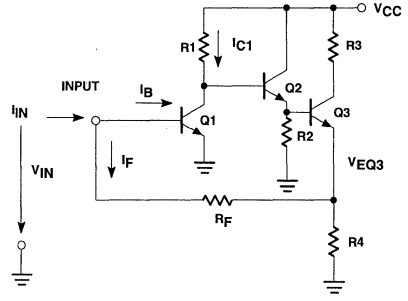


Figure 3. Shunt-Series Input Stage

The operating point of Q1, Figure 2, has been optimized for the lowest current noise without introducing a second dominant pole in the pass-band. All poles associated with subsequent stages have been kept at sufficiently high enough frequencies to yield an overall single pole response. Although wider bandwidths have been achieved by using a cascode input stage configuration, the present solution has the advantage of a very uniform, highly desensitized frequency response because the Miller effect dominates over the external photodiode and stray capacitances. For example, assuming a source capacitance of 1pF, input stage voltage gain of 70, R_{IN} = 60Ω then the total input capacitance, C_{IN} = (1+7.5) pF which will lead to only a 12% bandwidth reduction.

NOISE

Most of the currently installed fiber-optic systems use non-coherent transmission and detect incident optical power. Therefore, receiver noise performance becomes very important. The input stage achieves a low input referred noise current (spectral density) of 3.5pA/√Hz. The transresistance configuration assures that the external high value bias resistors often required for photodiode biasing will not contribute to the total noise system noise. The equivalent input $_{RMS}$ noise current is strongly determined by the quiescent current of Q_1, the feedback resistor R_F, and the bandwidth; however, it is not dependent upon the internal Miller-capacitance. The measured wideband noise was 66nA$_{RMS}$ in a 200MHz bandwidth.

DYNAMIC RANGE CALCULATIONS

The electrical dynamic range can be defined as the ratio of maximum input current to the peak noise current:

Electrical dynamic range, D_E, in a 200MHz bandwidth assuming I_{INMAX} = 240μA and a wideband noise of I_{EQ}=66nA$_{RMS}$ for an external source capacitance of C_S = 1pF.

$$D_E = 20\log\frac{\text{(Max. input current) (PK)}}{\text{(Peak noise current) (RMS)} \cdot \sqrt{2}}$$

$$= 20\log\frac{(240 \cdot 10^{-6})}{(\sqrt{2}\ 66\ 10^{-9})} = 68\text{dB}$$

In order to calculate the optical dynamic range the incident optical power must be considered.

For a given wavelength λ; (meters)

$$\text{Energy of one Photon} = \frac{hc}{\lambda} \text{ watt sec (Joule)}$$

Where h=Planck's Constant = 6.6×10^{-34} Joule sec.
c = speed of light = 3×10^8 m/sec
c / λ = optical frequency (Hz)
No. of incident photons/sec= where P=optical incident power

$$\text{No. of incident photons/sec} = \frac{P}{\frac{hs}{\lambda}}$$

where P = optical incident power

$$\text{No. of generated electrons/sec} = \eta \cdot \frac{P}{\frac{hs}{\lambda}}$$

where η = quantum efficiency

$$= \frac{\text{no. of generated electron hole paris}}{\text{no. of incident photons}}$$

$$\therefore I = \eta \cdot \frac{P}{\frac{hs}{\lambda}} \cdot e \text{ Amps (Coulombs/sec.)}$$

where e = electron charge = 1.6×10^{-19} Coulombs

$$\text{Responsivity } R = \frac{\eta \cdot e}{\frac{hs}{\lambda}} \text{Amp/watt}$$

$$I = P \cdot R$$

Assuming a data rate of 400 Mbaud (Bandwidth, B=200MHz), the noise parameter Z may be calculated as:[1]

$$Z = \frac{I_{EQ}}{qB} = \frac{66 \cdot 10^{-9}}{(1.6 \cdot 10^{-19})(200 \cdot 10^6)} = 2063$$

where Z is the ratio of $_{RMS}$ noise output to the peak response to a single hole-electron pair. Assuming 100% photodetector quantum efficiency, half mark/half space digital transmission, 850nm lightwave and using Gaussian approximation, the minimum required optical power to achieve 10^{-9} BER is:

$$P_{avMIN} = 12\frac{hc}{\lambda}B\ Z = 12\ 2.3 \cdot 10^{-19}$$

$$200 \cdot 10^6\ 2063$$

$$= 1139\text{nW} = -29.4\text{dBm}$$

where h is Planck's Constant, c is the speed of light, λ is the wavelength. The minimum input current to the NE5210, at this input power is:

$$I_{avMIN} = qP_{avMIN}\frac{\lambda}{hc}$$

$$= \frac{1139 \cdot 10^{-9} \cdot 1.6 \cdot 10^{-19}}{2.3 \cdot 10^{-19}}$$

$$= 792\text{nA}$$

Choosing the maximum peak overload current of I_{avMAX}=240μA, the maximum mean optical power is:

$$P_{avMAX} = \frac{hcI_{avMAX}}{\lambda q} = \frac{2.3 \cdot 10^{-19}}{1.6 \cdot 10^{-19}}240 \cdot 10^{-6}$$

Thus the optical dynamic range, D_O is:

$D_O = P_{avMAX} - P_{avMIN}$ = -4.6 -(-29.4) = 24.8dB.

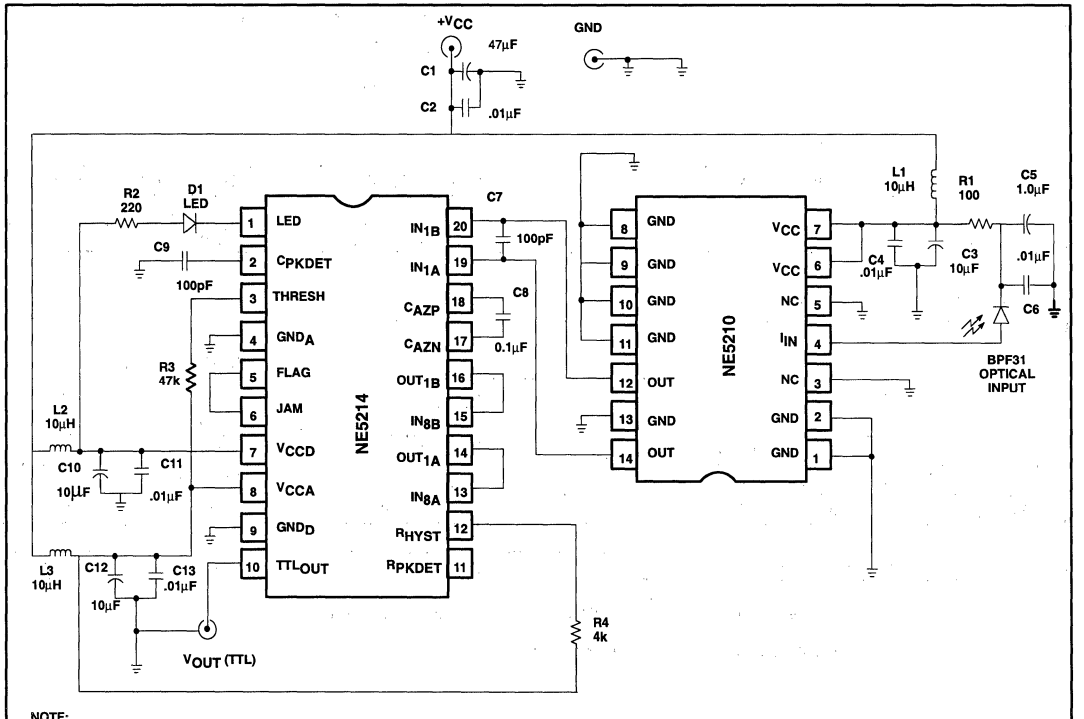
This represents the maximum limit attainable with the NE5210 operating at 200MHz bandwidth, with a half mark/half space digital transmission at 850nm wavelength.

APPLICATION INFORMATION

Package parasitics, particularly ground lead inductances and parasitic capacitances, can significantly degrade the frequency response. Since the NE5210 has differential outputs which can feed back signals to the input by parasitic package or board layout capacitances, both peaking and attenuating type frequency response shaping is possible. Constructing the board layout so that Ground 1 and Ground 2 have very low impedance paths has produced the best results. This was accomplished by adding a ground-plane stripe underneath the device connecting Ground 1, Pins 8–11, and Ground 2, Pins 1 and 2 on opposite ends of the SO14 package. This ground-plane stripe also provides isolation between the output return currents flowing to either V_{CC2} or Ground 2 and the input photodiode currents to flowing to Ground 1. Without this ground-plane stripe and with large lead inductances on the board, the part may be unstable and oscillate near 800MHz. The easiest way to realize that the part is not functioning normally is to measure the DC voltages at the outputs. If they are not close to their quiescent values of 3.3V (for a 5V supply), then the circuit may be oscillating. Input pin layout necessitates that the photodiode be physically very close to the input and Ground 1. Connecting Pins 3 and 5 to Ground 1 will tend to shield the input but it will also tend to increase the capacitance on the input and slightly reduce the bandwidth.

As with any high-frequency device, some precautions must be observed in order to enjoy reliable performance. The first of these is the use of a well-regulated power supply. The supply must be capable of providing varying amounts of current without significantly changing the voltage level. Proper supply bypassing requires that a good quality 0.1µF high-frequency capacitor be inserted between V_{CC1} and V_{CC2}, preferably a chip capacitor, as close to the package pins as possible. Also, the parallel combination of 0.1µF capacitors with 10µF tantalum capacitors from each supply, V_{CC1} and V_{CC2}, to the ground plane should provide adequate decoupling. Some applications may require an RF choke in series with the power supply line. Separate analog and digital ground leads must be maintained and printed circuit board ground plane should be employed whenever possible.

Figure 4 depicts a 50Mb/s TTL fiber-optic receiver using the BPF31, 850nm LED, the NE5210 and the NE5214 post amplifier.



NOTE:
The NE5210/NE5217 combination can operate at data rates in excess of 100Mb/s NRZ
The capacitor C7 decreases the NE5210 bandwidth to improve overall S/N ratio in the DC–50MHz band, but does create extra high frequency noise on the NE5210 V_{CC} pin(s).

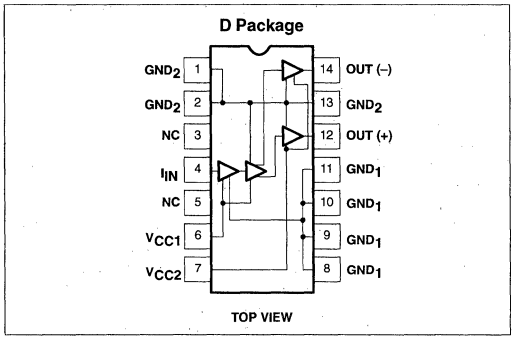
Figure 4. A 50Mb/s Fiber Optic Receiver

Transimpedance amplifier (180MHz) NE/SA5211

DESCRIPTION

The NE/SA5211 is a 28kΩ transimpedance, wide-band, low noise amplifier with differential outputs, particularly suitable for signal recovery in fiber optic receivers. The part is ideally suited for many other RF applications as a general purpose gain block.

PIN CONFIGURATION



FEATURES

- Extremely low noise: $1.8pA / \sqrt{Hz}$
- Single 5V supply
- Large bandwidth: 180MHz
- Differential outputs
- Low input/output impedances
- High power supply rejection ratio
- 28kΩ differential transresistance

APPLICATIONS

- Fiber optic receivers, analog and digital
- Current-to-voltage converters
- Wide-band gain block
- Medical and scientific Instrumentation
- Sensor preamplifiers
- Single-ended to differential conversion
- Low noise RF amplifiers
- RF signal processing

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE5211D	0175D
14-Pin Plastic Small Outline (SO) Package	-40 to +85°C	SA5211D	0175D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNIT
		NE5211	SA5211	
V_{CC}	Power supply	6	6	V
T_A	Operating ambient temperature range	0 to +70	-40 to +85	°C
T_J	Operating junction temperature range	-55 to +150	-55 to +150	°C
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C
$P_{D\ MAX}$	Power dissipation, T_A=25°C (still-air)[1]	1.0	1.0	W
$I_{IN\ MAX}$	Maximum input current[2]	5	5	mA
θ_{JA}	Thermal resistance	125	125	°C/W

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance: θ_{JA}=125°C/W
2. The use of a pull-up resistor to V_{CC}, for the PIN diode is recommended.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	4.5 to 5.5	V
T_A	Ambient temperature range NE Grade SA Grade	 0 to +70 -40 to +85	°C
T_J	Junction temperature range NE Grade SA Grade	 0 to +90 -40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over operating temperature range at V_{CC}=5V, unless otherwise specified. Typical data apply at V_{CC}=5V and T_A=25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5211			SA5211			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IN}	Input bias voltage		0.6	0.8	0.95	0.55	0.8	1.00	V
$V_{O\pm}$	Output bias voltage		2.8	3.4	3.7	2.7	3.4	3.7	V
V_{OS}	Output offset voltage			0	120		0	130	mV
I_{CC}	Supply current		21	24	30	20	26	31	mA
I_{OMAX}	Output sink/source current[1]		3	4		3	4		mA
I_{IN}	Input current (2% linearity)	Test Circuit 8, Procedure 2	±30	±40		±20	±40		µA
$I_{IN\ MAX}$	Maximum input current overload threshold	Test Circuit 8, Procedure 4	±40	±60		±30	±60		µA

NOTES:
1. Test condition: output quiescent voltage variation is less than 100mV for 3mA load current.

AC ELECTRICAL CHARACTERISTICS

Typical data and Min and Max limits apply at V_{CC}=5V and T_A=25°C

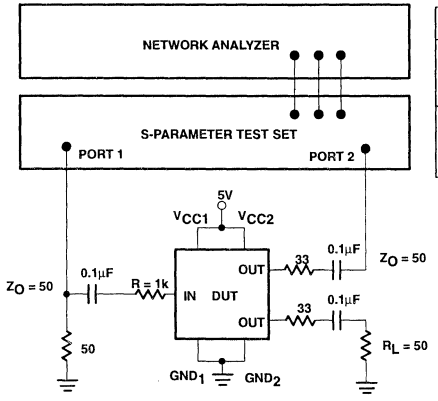
SYMBOL	PARAMETER	TEST CONDITIONS	NE5211			SA5211			UNIT
			Min	Typ	Max	Min	Typ	Max	
R_T	Transresistance (differential output)	DC tested $R_L = \infty$ Test Circuit 8, Procedure 1	22	28	35	21	28	36	kΩ
R_O	Output resistance (differential output)	DC tested		30			30		Ω
R_T	Transresistance (single-ended output)	DC tested $R_L = \infty$	11	14	17.5	10.5	14	18.0	kΩ
R_O	Output resistance (single-ended output)	DC tested		15			15		Ω
f_{3dB}	Bandwidth (-3dB)	T_A = 25°C Test circuit 1		180			180		MHz
R_{IN}	Input resistance			200			200		Ω
C_{IN}	Input capacitance			4			4		pF
$\Delta R/\Delta V$	Transresistance power supply sensitivity	V_{CC} = 5±0.5V		3.7			3.7		%/V
$\Delta R/\Delta T$	Transresistance ambient temperature sensitivity	$\Delta T_A = T_{A\,MAX} - T_{A\,MIN}$		0.025			0.025		%/°C
I_N	RMS noise current spectral density (referred to input)	Test Circuit 2 f = 10MHz T_A = 25°C		1.8			1.8		pA/√Hz
I_T	Integrated RMS noise current over the bandwidth (referred to input)	T_A = 25°C Test Circuit 2							
	C_S=0[1]	Δf = 50MHz Δf = 100MHz Δf = 200MHz		13 20 35			13 20 35		nA
	C_S=1pF	Δf = 50MHz Δf = 100MHz Δf = 200MHz		13 21 41			13 21 41		nA
PSRR	Power supply rejection ratio[2] ($V_{CC1} = V_{CC2}$)	DC tested, ΔV_{CC} = 0.1V Equivalent AC Test Circuit 3	26	32		23	32		dB
PSRR	Power supply rejection ratio[2] (V_{CC1})	DC tested, ΔV_{CC} = 0.1V Equivalent AC Test Circuit 4	26	32		23	32		dB
PSRR	Power supply rejection ratio[2] (V_{CC2})	DC tested, ΔV_{CC} = 0.1V Equivalent AC Test Circuit 5	45	65		45	65		dB
PSRR	Power supply rejection ratio (ECL configuration)[2]	f = 0.1MHz Test Circuit 6		23			23		dB
V_{OMAX}	Maximum differential output voltage swing	$R_L = \infty$ Test Circuit 8, Procedure 3	2.4	3.2		1.7	3.2		V_{P-P}
$V_{IN\,MAX}$	Maximum input amplitude for output duty cycle of 50±5%[3]	Test Circuit 7	160			160			mV_{P-P}
t_R	Rise time for 50mV output signal[4]	Test Circuit 7		0.8	1.2		0.8	1.8	ns

NOTES:

1. Package parasitic capacitance amounts to about 0.2pF
2. PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use RF filter in V_{CC} lines.
3. Guaranteed by linearity and overload tests.
4. t_R defined as 20-80% rise time. It is guaranteed by -3dB bandwidth test.

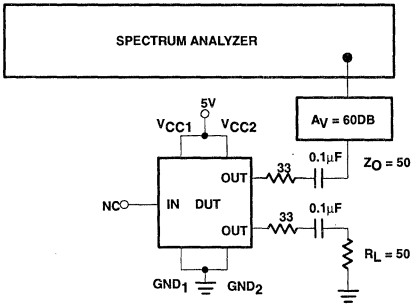
Transimpedance amplifier (180MHz) NE/SA5211

TEST CIRCUITS



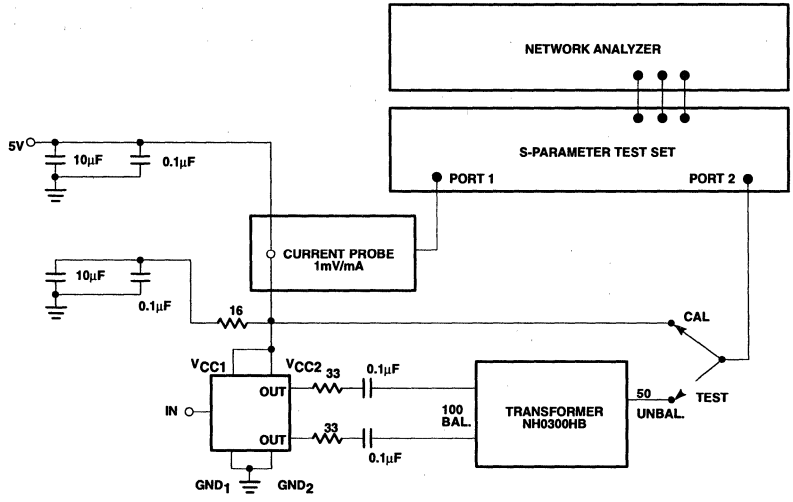
SINGLE-ENDED	DIFFERENTIAL
$R_T \approx \frac{V_{OUT}}{V_{IN}} R = 2 \cdot S21 \cdot R$	$R_T = \frac{V_{OUT}}{V_{IN}} R = 4 \cdot S21 \cdot R$
$R_O \approx Z_O \frac{\lvert 1 + S22 \rvert}{\lvert 1 - S22 \rvert} - 33$	$R_O = 2Z_O \frac{\lvert 1 + S22 \rvert}{\lvert 1 - S22 \rvert} - 66$

Test Circuit 1

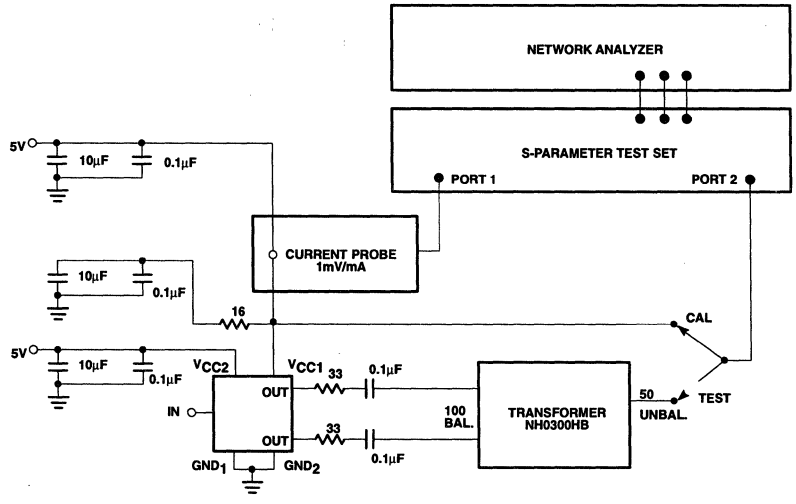


Test Circuit 2

TEST CIRCUITS (Continued)

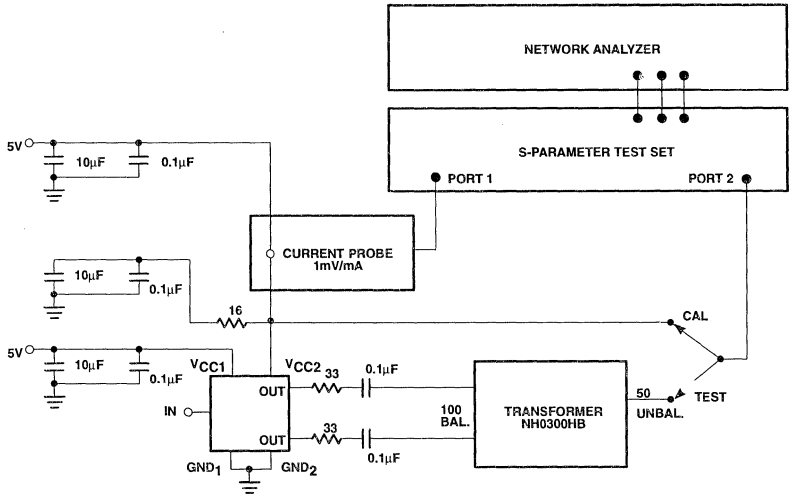


Test Circuit 3

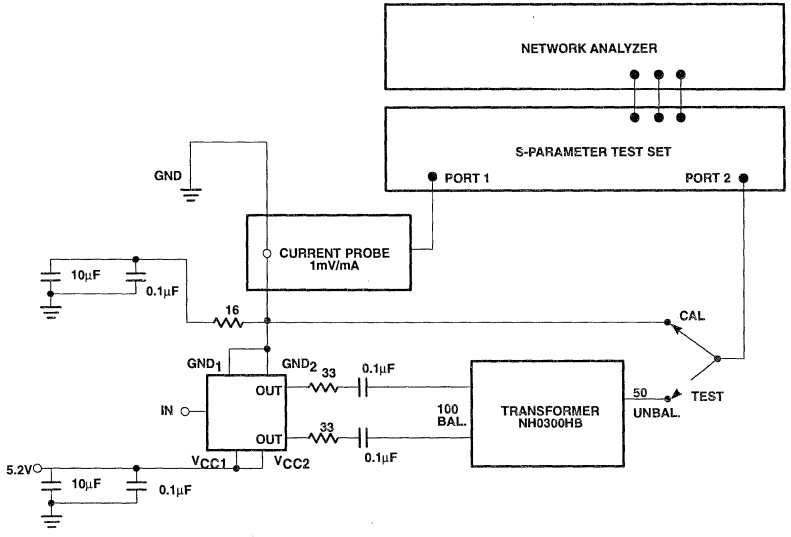


Test Circuit 4

TEST CIRCUITS (Continued)

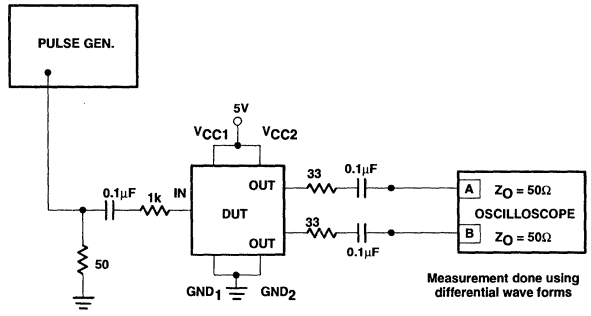


Test Circuit 5



Test Circuit 6

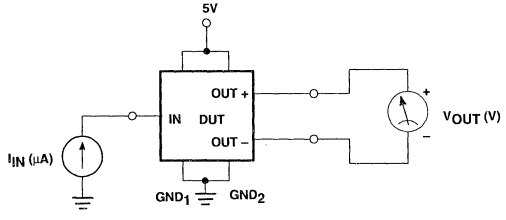
TEST CIRCUITS (Continued)

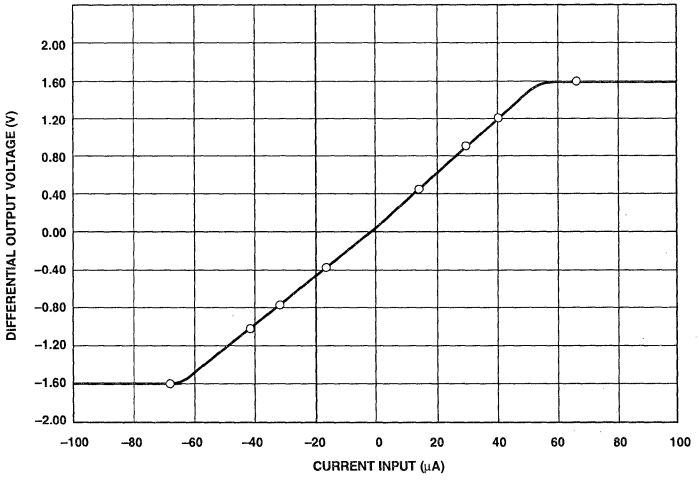


Test Circuit 7

TEST CIRCUITS (Continued)

Typical Differential Output Voltage vs Current Input





NE5211 TEST CONDITIONS

Procedure 1

R_T measured at 15μA

$R_T = (V_{O1} - V_{O2})/(+15\mu A - (-15\mu A))$

Where: V_{O1} Measured at I_{IN} = +15μA

V_{O2} Measured at I_{IN} = –15μA

Procedure 2

Linearity = 1 – ABS(($V_{OA} - V_{OB}$) / ($V_{O3} - V_{O4}$))

Where: V_{O3} Measured at I_{IN} = +30μA

V_{O4} Measured at I_{IN} = –30μA

$V_{OA} = R_T \cdot (+ 30\mu A) + V_{OB}$

$V_{OB} = R_T \cdot (- 30\mu A) + V_{OB}$

Procedure 3

$V_{OMAX} = V_{O7} - V_{O8}$

Where: V_{O7} Measured at I_{IN} = +65μA

V_{O8} Measured at I_{IN} = –65μA

Procedure 4

I_{IN} Test Pass Conditions:

$V_{O7} - V_{O5} > 20mV$ and $V_{O6} - V_{O5} > 50mV$

Where: V_{O5} Measured at I_{IN} = +40μA

V_{O6} Measured at I_{IN} = –400μA

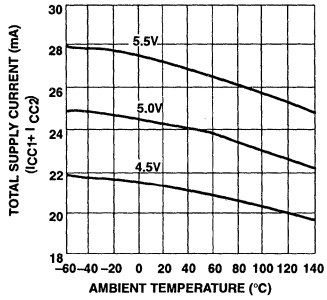
V_{O7} Measured at I_{IN} = +65μA

V_{O8} Measured at I_{IN} = –65μA

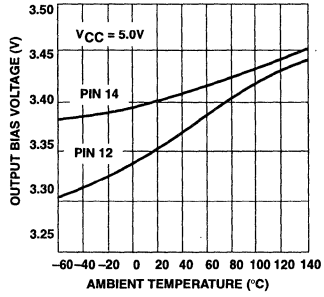
Test Circuit 8

TYPICAL PERFORMANCE CHARACTERISTICS

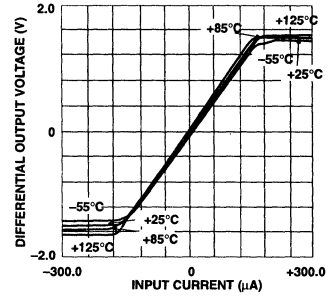
NE5211 Supply Current vs Temperature



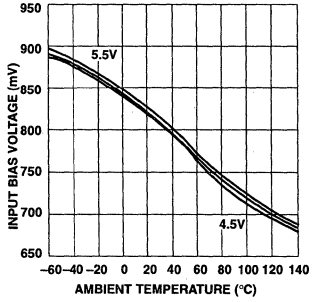
NE5211 Output Bias Voltage vs Temperature



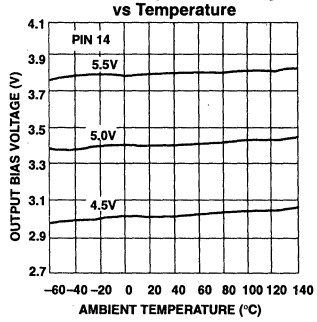
NE5211 Output Voltage vs Input Current



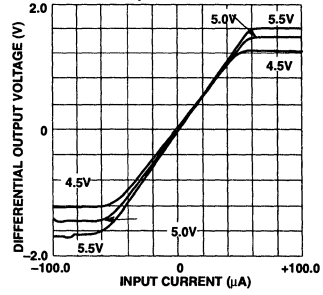
NE5211 Input Bias Voltage vs Temperature



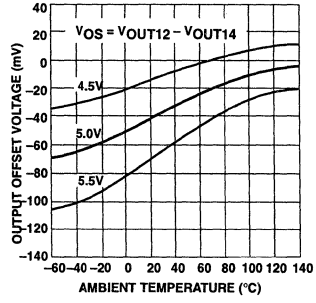
NE5211 Output Bias Voltage vs Temperature



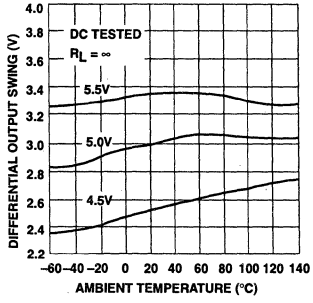
NE5211 Differential Output Voltage vs Input Current



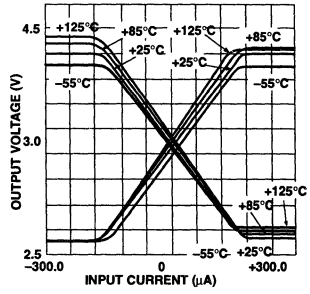
NE5211 Output Offset Voltage vs Temperature



NE5211 Differential Output Swing vs Temperature

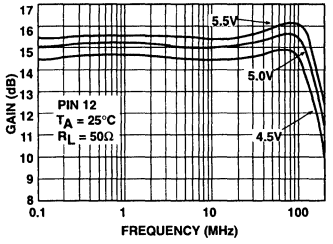


NE5211 Differential Output Voltage vs Input Current

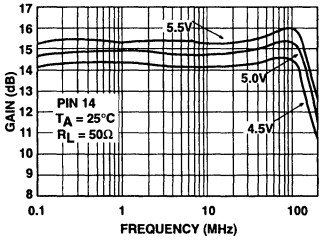


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

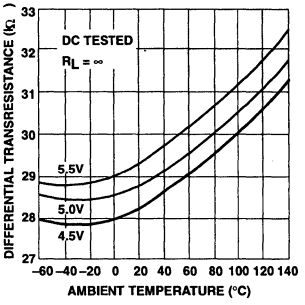
NE5211 Gain vs Frequency



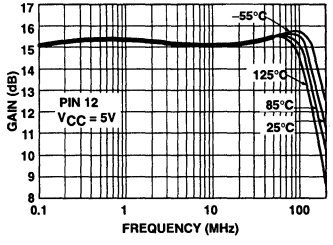
NE5211 Gain vs Frequency



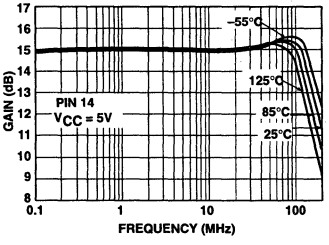
NE5211 Differential Transresistance vs Temperature



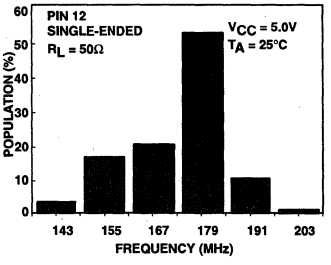
NE5211 Gain vs Frequency



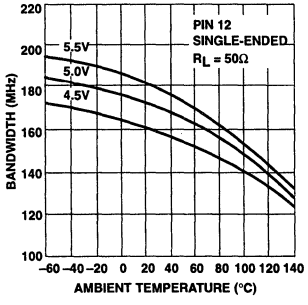
NE5211 Gain vs Frequency



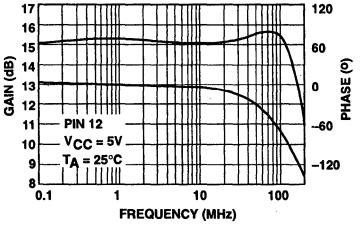
NE5211 Typical Bandwidth Distribution (70 Parts from 3 Wafer Lots)



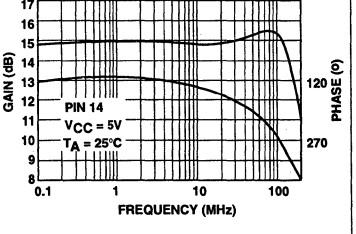
NE5211 Bandwidth vs Temperature



NE5211 Gain and Phase Shift vs Frequency

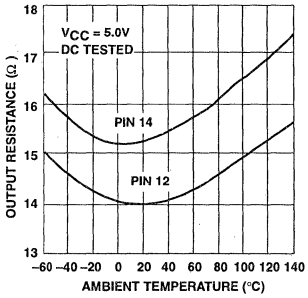


NE5211 Gain and Phase Shift vs Frequency

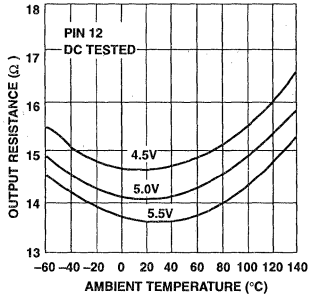


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

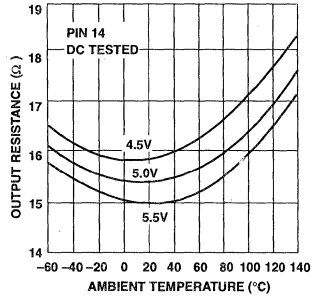
NE5211 Output Resistance vs Temperature



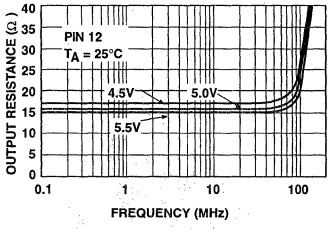
NE5211 Output Resistance vs Temperature



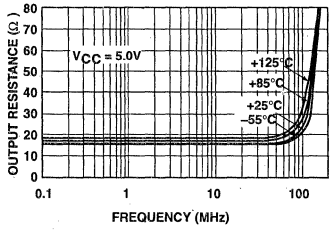
NE5211 Output Resistance vs Temperature



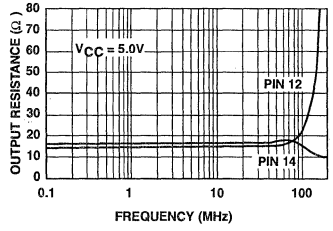
NE5211 Output Resistance vs Frequency



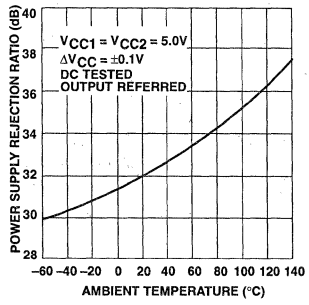
NE5211 Output Resistance vs Frequency



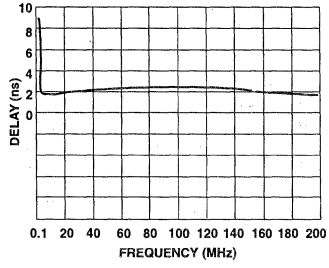
NE5211 Output Resistance vs Frequency



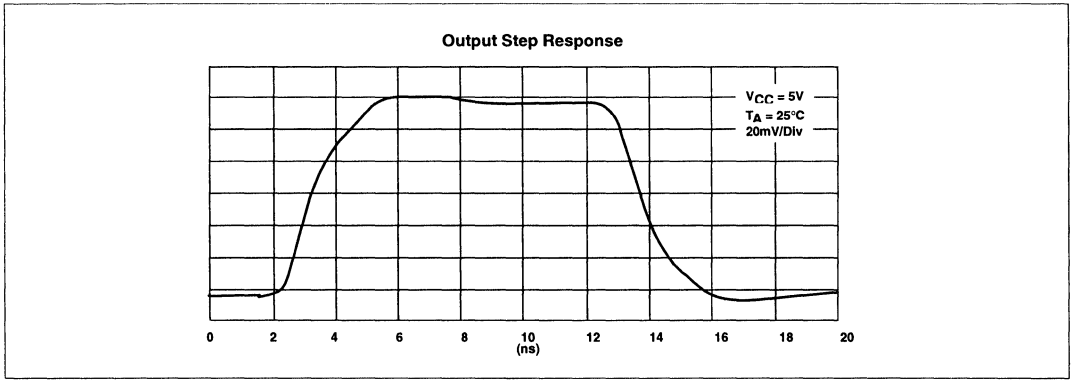
NE5211 Power Supply Rejection Ratio vs Temperature



NE5211 Group Delay vs Frequency



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



THEORY OF OPERATION

Transimpedance amplifiers have been widely used as the preamplifier in fiber-optic receivers. The NE5211 is a wide bandwidth (typically 180MHz) transimpedance amplifier designed primarily for input currents requiring a large dynamic range, such as those produced by a laser diode. The maximum input current before output stage clipping occurs at typically 50μA. The NE5211 is a bipolar transimpedance amplifier which is current driven at the input and generates a differential voltage signal at the outputs. The forward transfer function is therefore a ratio of the differential output voltage to a given input current with the dimensions of ohms. The main feature of this amplifier is a wideband, low-noise input stage which is desensitized to photodiode capacitance variations. When connected to a photodiode of a few picoFarads, the frequency response will not be degraded significantly. Except for the input stage, the entire signal path is differential to provide improved power-supply rejection and ease of interface to ECL type circuitry. A block diagram of the circuit is shown in Figure 1. The input stage (A1) employs shunt-series feedback to stabilize the current gain of the amplifier. The transresistance of the amplifier from the current source to the emitter of Q_3 is approximately the value of the feedback resistor, R_F=14.4kΩ. The gain from the second stage (A2) and emitter followers (A3 and A4) is about two. Therefore, the differential transresistance of the entire amplifier, R_T is

$$R_T = \frac{V_{OUT}(diff)}{I_{IN}} = 2R_F = 2(14.4K) = 28.8k\Omega$$

The single-ended transresistance of the amplifier is typically 14.4kΩ.

The simplified schematic in Figure 2 shows how an input current is converted to a differential output voltage. The amplifier has a

single input for current which is referenced to Ground 1. An input current from a laser diode, for example, will be converted into a voltage by the feedback resistor R_F. The transistor Q1 provides most of the open loop gain of the circuit, A_{VOL}≈70. The emitter follower Q_2 minimizes loading on Q_1. The transistor Q_4, resistor R_7, and V_{B1} provide level shifting and interface with the $Q_{15} - Q_{16}$ differential pair of the second stage which is biased with an internal reference, V_{B2}. The differential outputs are derived from emitter followers $Q_{11} - Q_{12}$ which are biased by constant current sources. The collectors of $Q_{11} - Q_{12}$ are bonded to an external pin, V_{CC2}, in order to reduce the feedback to the input stage. The output impedance is about 17Ω single-ended. For ease of performance evaluation, a 33Ω resistor is used in series with each output to match to a 50Ω test system.

BANDWIDTH CALCULATIONS

The input stage, shown in Figure 3, employs shunt-series feedback to stabilize the current gain of the amplifier. A simplified analysis can determine the performance of the amplifier. The equivalent input capacitance, C_{IN}, in parallel with the source, I_S, is approximately 7.5pF, assuming that C_S=0 where C_S is the external source capacitance.

Since the input is driven by a current source the input must have a low input resistance. The input resistance, R_{IN}, is the ratio of the incremental input voltage, V_{IN}, to the corresponding input current, I_{IN} and can be calculated as:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}} = \frac{14.4K}{71} = 203\Omega$$

More exact calculations would yield a higher value of 60Ω.

Thus C_{IN} and R_{IN} will form the dominant pole of the entire amplifier;

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Assuming typical values for R_F = 14.4kΩ, R_{IN} = 200Ω, C_{IN} = 4pF

$$f_{-3dB} = \frac{1}{2\pi\ 4pF\ 200\Omega} = 200MHz$$

The operating point of Q1, Figure 2, has been optimized for the lowest current noise without introducing a second dominant pole in the pass-band. All poles associated with subsequent stages have been kept at sufficiently high enough frequencies to yield an overall single pole response. Although wider bandwidths have been achieved by using a cascade input stage configuration, the present solution has the advantage of a very uniform, highly desensitized frequency response because the Miller effect dominates over the external photodiode and stray capacitances. For example, assuming a source capacitance of 1pF, input stage voltage gain of 70, R_{IN} = 60Ω then the total input capacitance, C_{IN} = (1+7.5) pF which will lead to only a 12% bandwidth reduction.

NOISE

Most of the currently installed fiber-optic systems use non-coherent transmission and detect incident optical power. Therefore, receiver noise performance becomes very important. The input stage achieves a low input referred noise current (spectral density) of 3.5pA/$\sqrt{Hz}$. The transresistance configuration assures that the external high value bias resistors often required for photodiode biasing will not contribute to the total noise system noise. The equivalent input $_{RMS}$ noise current is strongly determined by the quiescent current of Q_1, the feedback resistor R_F, and the bandwidth; however, it is not dependent upon the internal Miller-capacitance. The measured wideband noise was 66nA in a 200MHz bandwidth.

DYNAMIC RANGE CALCULATIONS

The electrical dynamic range can be defined as the ratio of maximum input current to the peak noise current:

Electrical dynamic range, D_E, in a 200MHz bandwidth assuming I_{INMAX} = 60μA and a wideband noise of I_{EQ}=41nA$_{RMS}$ for an external source capacitance of C_S = 1pF.

$$D_E = \frac{\text{(Max. input current)}}{\text{(Peak noise current)}}$$

$$D_E(dB) = 20\log\frac{(60 \cdot 10^{-6})}{(\sqrt{2}\ 41\ 10^{-9})}$$

$$D_E(dB) = 20\log\frac{(60\mu A)}{(58nA)} = 60dB$$

In order to calculate the optical dynamic range the incident optical power must be considered.

For a given wavelength λ;

Energy of one Photon = $\frac{hc}{\lambda}$ watt sec (Joule)

Where h=Planck's Constant = 6.6×10^{-34} Joule sec.

c = speed of light = 3×10^8 m/sec

c / λ = optical frequency

No. of incident photons/sec= $\frac{P}{\frac{hs}{\lambda}}$ where P=optical incident power

No. of generated electrons/sec = $\eta \cdot \frac{P}{\frac{hs}{\lambda}}$

where η = quantum efficiency

$$= \frac{\text{no. of generated electron hole paris}}{\text{no. of incident photons}}$$

$$\therefore I = \eta \cdot \frac{P}{\frac{hs}{\lambda}} \cdot e \text{ Amps (Coulombs/sec.)}$$

where e = electron charge = 1.6×10^{-19} Coulombs

Responsivity R = $\frac{\eta \cdot e}{\frac{hs}{\lambda}}$ Amp/watt

$I = P \cdot R$

Assuming a data rate of 400 Mbaud (Bandwidth, B=200MHz), the noise parameter Z may be calculated as:[1]

$$Z = \frac{I_{EQ}}{qB} = \frac{41 \cdot 10^{-9}}{(1.6 \cdot 10^{-19})(200 \cdot 10^6)} = 1281$$

where Z is the ratio of $_{RMS}$ noise output to the peak response to a single hole-electron pair. Assuming 100% photodetector quantum efficiency, half mark/half space digital transmission, 850nm lightwave and using Gaussian approximation, the minimum required optical power to achieve 10^{-9} BER is:

$$P_{avMIN} = 12\frac{hc}{\lambda} B\ Z = 12 \cdot 2.3 \cdot 10^{-19}$$

$$200 \cdot 10^6\ (1281) = 719nW = -31.5dBm$$

$$= 1139nW = -29.4dBm$$

where h is Planck's Constant, c is the speed of light, λ is the wavelength. The minimum input current to the NE5211, at this input power is:

$$I_{avMIN} = qP_{avMIN}\frac{\lambda}{hc}\ \ \frac{1}{\text{Joule}} \cdot \frac{\text{Joule}}{\text{sec}} \cdot q = I$$

$$= \frac{707 \cdot 10^{-9} \cdot 1.6 \cdot 10^{-19}}{2.3 \cdot 10^{-19}}$$

$$= 500nA$$

Choosing the maximum peak overload current of I_{avMAX}=60μA, the maximum mean optical power is:

$$P_{avMAX} = \frac{hcI_{avMAX}}{\lambda q} = \frac{2.3 \cdot 10^{-19}}{1.6 \cdot 10^{-19}}\ 60 \cdot 10\mu A$$

$$= 86\mu W \text{ or } -10.6dBm \text{ (optical)}$$

Thus the optical dynamic range, D_O is:

$D_O = P_{avMAX} - P_{avMIN}$ = -4.6 -(-29.4) = 24.8dB.

$$D_O = P_{avMAX} - P_{avMIN} = -31.5 - (-10.6)$$

$$= 20.8dB$$

1. S.D. Personick, *Optical Fiber Transmission Systems*, Plenum Press, NY, 1981, Chapter 3.

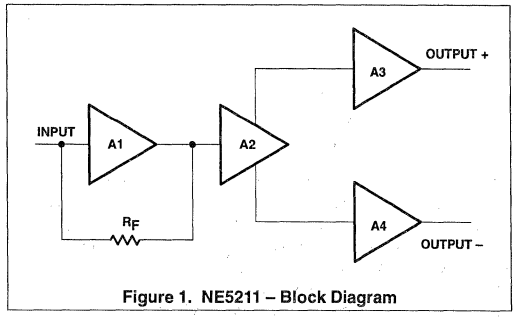


Figure 1. NE5211 – Block Diagram

This represents the maximum limit attainable with the NE5211 operating at 200MHz bandwidth, with a half mark/half space digital transmission at 850nm wavelength.

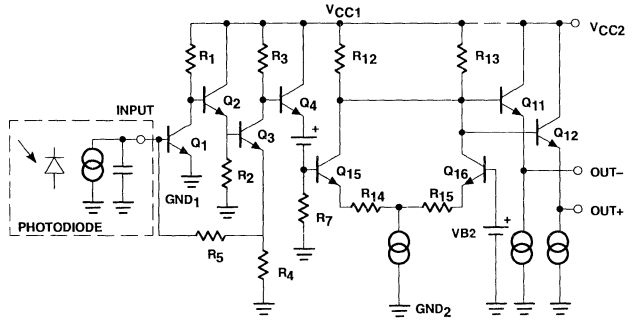


Figure 2. Transimpedance Amplifier

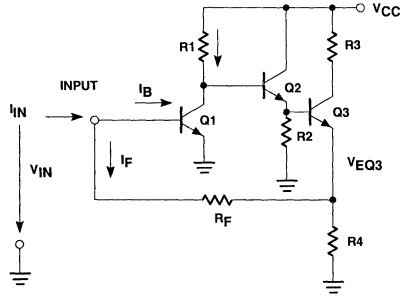


Figure 3. Shunt-Series Input Stage

APPLICATION INFORMATION

Package parasitics, particularly ground lead inductances and parasitic capacitances, can significantly degrade the frequency response. Since the NE5211 has differential outputs which can feed back signals to the input by parasitic package or board layout capacitances, both peaking and attenuating type frequency response shaping is possible. Constructing the board layout so that Ground 1 and Ground 2 have very low impedance paths has produced the best results. This was accomplished by adding a ground-plane stripe underneath the device connecting Ground 1, Pins 8–11, and Ground 2, Pins 1 and 2 on opposite ends of the SO14 package. This ground-plane stripe also provides isolation between the output return currents flowing to either V_{CC2} or Ground 2 and the input photodiode currents to flowing to Ground 1. Without this ground-plane stripe and with large lead inductances on the board, the part may be unstable and oscillate near 800MHz. The easiest way to realize that the part is not functioning normally is to measure the DC voltages at the outputs. If they are not close to their quiescent values of 3.3V (for a 5V supply), then the circuit may be oscillating. Input pin layout necessitates that the photodiode be physically very close to the input and Ground 1. Connecting Pins 3 and 5 to Ground 1 will tend to shield the input but it will also tend to increase the capacitance on the input and slightly reduce the bandwidth.

As with any high-frequency device, some precautions must be observed in order to enjoy reliable performance. The first of these is the use of a well-regulated power supply. The supply must be capable of providing varying amounts of current without significantly changing the voltage level. Proper supply bypassing requires that a good quality 0.1µF high-frequency capacitor be inserted between V_{CC1} and V_{CC2}, preferably a chip capacitor, as close to the package pins as possible. Also, the parallel combination of 0.1µF capacitors with 10µF tantalum capacitors from each supply, V_{CC1} and V_{CC2}, to the ground plane should provide adequate decoupling. Some applications may require an RF choke in series with the power supply line. Separate analog and digital ground leads must be maintained and printed circuit board ground plane should be employed whenever possible.

Figure 4 depicts a 50Mb/s TTL fiber-optic receiver using the BPF31, 850nm LED, the NE5211 and the NE5214 post amplifier.

Transimpedance amplifier (180MHz) NE/SA5211

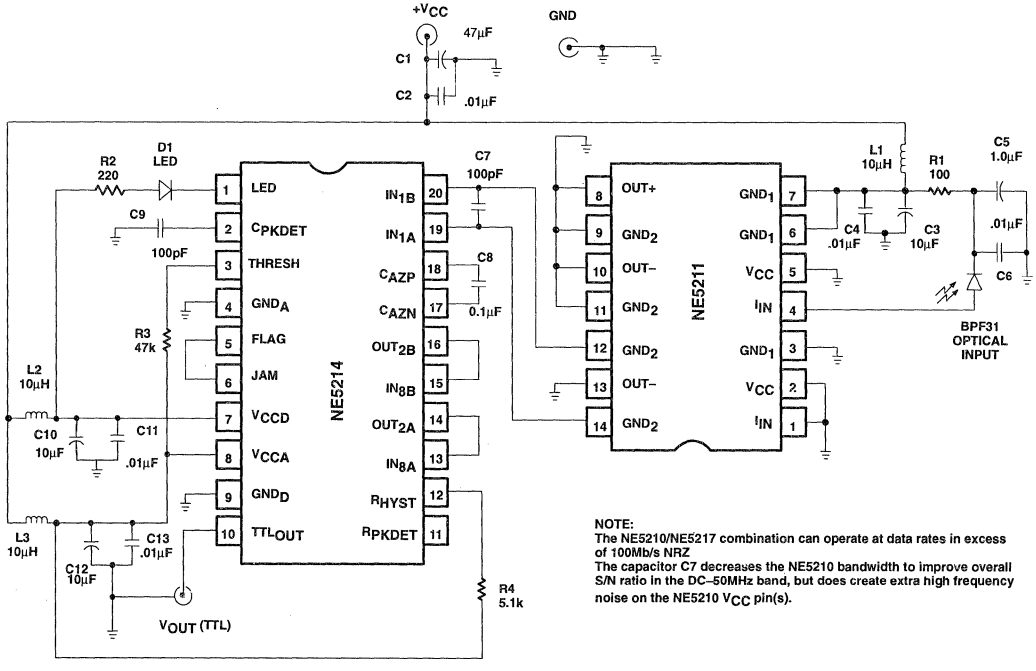


Figure 4. A 50Mb/s Fiber Optic Receiver

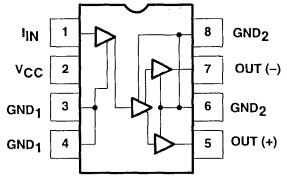
Transimpedance amplifier (140MHz) NE/SA/SE5212A

DESCRIPTION

The NE/SA/SE5212A is a 14kΩ transimpedance, wideband, low noise differential output amplifier, particularly suitable for signal recovery in fiber optic receivers and in any other applications where very low signal levels obtained from high-impedance sources need to be amplified.

PIN CONFIGURATION

N, FE, D Packages



FEATURES

- Extremely low noise: 2.5pA/√Hz
- Single 5V supply
- Large bandwidth: 140MHz
- Differential outputs
- Low input/output impedances
- 14kΩ differential transresistance
- ESD hardened

APPLICATIONS

- Fiber-optic receivers, analog and digital
- Current-to-voltage converters
- Wideband gain block
- Medical and scientific instrumentation
- Sensor preamplifiers
- Single-ended to differential conversion
- Low noise RF amplifiers
- RF signal processing

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5212AN	0404B
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE5212AD	0174C
8-Pin Ceramic Dual In-Line Package (DIP)	0 to +70°C	NE5212AFE	0580A
8-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	SA5212AD	0174C
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA5212AN	0404B
8-Pin Ceramic Dual In-Line Package (DIP)	-40°C to +85°C	SA5212AFE	0580A
8-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE5212AN	0404B
8-Pin Ceramic Dual In-Line Package (DIP)	-55°C to +125°C	SE5212AFE	0580A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING			UNIT
		NE5212A	SA5212A	SE5212A	
V_{CC}	Power Supply	6	6	6	V
$P_{D\ MAX}$	Power dissipation, T_A=25°C (still air)[1]				
	8-Pin Plastic DIP	1100	1100	1100	mW
	8-Pin Plastic SO	750	750	750	mW
	8-Pin Cerdip	750	750	750	mw
$I_{IN\ MAX}$	Maximum input current[2]	5	5	5	mA
T_A	Operating ambient temperature range	0 to 70	-40 to 85	-55 to 125	°C
T_J	Operating junction	-55 to 150	-55 to 150	-55 to 150	°C
T_{STG}	Storage temperature range	-65 to 150	-65 to 150	-65 to 150	°C

NOTES:

1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance:
   8-Pin Plastic DIP: 110°C/W
   8-Pin Plastic SO: 160°C/W
   8-Pin Cerdip: 165°C/W
2. The use of a pull-up resistor to V_{CC}, for the PIN diode, is recommended

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	4.5 to 5.5	V
T_A	Ambient temperature ranges		
	NE Grade	0 to +70	°C
	SA Grade	-40 to +85	°C
	SE Grade	-55 to +125	°C
T_J	Junction temperature ranges		
	NE Grade	0 to +90	°C
	SA Grade	-40 to +105	°C
	SE Grade	-55 to +145	°C

DC ELECTRICAL CHARACTERISTICS

Minimum and Maximum limits apply over operating temperature range at V_{CC}=5V, unless otherwise specified. Typical data applies at V_{CC}=5V and T_A=25°C[1].

SYMBOL	PARAMETER	TEST CONDITIONS	NE5212A			SA/SE5212A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IN}	Input bias voltage		0.6	0.8	0.95	0.55	0.8	1.05	V
$V_{O\pm}$	Output bias voltage		2.8	3.3	3.7	2.5	3.3	3.8	V
V_{OS}	Output offset voltage				80			120	mV
I_{CC}	Supply current		21	26	32	20	26	33	mA
I_{OMAX}	Output sink/source current		3	4		3	4		mA
I_{IN}	Maximum input current (2% linearity)	Test Circuit 6, Procedure 2	±60	±80		±40	±80		µA
$I_{N\ MAX}$	Maximum input current overload threshold	Test Circuit 6, Procedure 4	±80	±120		±60	±120		µA

NOTES:
1. As in all high frequency circuits, a supply bypass capacitor should be located as close to the part as possible.

AC ELECTRICAL CHARACTERISTICS

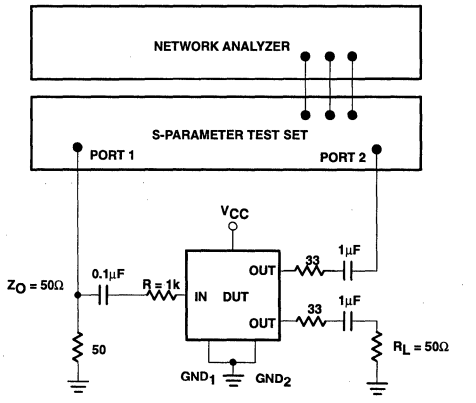
Minimum and Maximum limits apply over operating temperature range at V_{CC}=5V, unless otherwise specified. Typical data applies at V_{CC}=5V and T_A=25°C[5].

SYMBOL	PARAMETER	TEST CONDITIONS	NE5212A			SA/SE5212A			UNIT
			Min	Typ	Max	Min	Typ	Max	
R_T	Transresistance (differential output)	DC tested, $R_L = \infty$ Test Circuit 6, Procedure 1	9.8	14	18.2	9.0	14	19	kΩ
R_O	Output resistance (differential output)	DC tested	14	30	42	14	30	46	Ω
R_T	Transresistance (single-ended output)	DC tested, $R_L = \infty$	4.9	7	9.1	4.5	7	9.5	kΩ
R_O	Output resistance (single-ended output)	DC tested	7	15	21	7	15	23	Ω
f_{3dB}	Bandwidth (-3dB)	Test Circuit 1 D package, T_A = 25°C N, FE packages, T_A = 25°C	100 100	140 120		100 100	140 120		MHz
R_{IN}	Input resistance		75	110	143	70	110	150	Ω
C_{IN}	Input capacitance			10	15		10	18	pF
$\Delta R/\Delta V$	Transresistance power supply sensitivity	V_{CC} = 5 ±0.5V		9.6			9.6		%/V
$\Delta R/\Delta T$	Transresistance ambient temperature sensitivity	D package $\Delta T_A = T_{A\,MAX} - T_{A\,MIN}$		0.05			0.05		%/°C
I_N	RMS noise current spectral density (referred to input)	Test Circuit 2 f = 10MHz T_A = 25°C		2.5			2.5		pA/√Hz
I_T	Integrated RMS noise current over the bandwidth (referred to input) $C_S = 0$[1]	T_A = 25°C Test Circuit 2 Δf = 50MHz		20			20		nA
		Δf = 100MHz		27			27		
		Δf = 200MHz		40			40		
	C_S = 1pF	Δf = 50MHz		22			22		
		Δf = 100MHz		32			32		
		Δf = 200MHz		52			52		
PSRR	Power supply rejection ratio[2]	Any package DC tested ΔV_{CC} = 0.1V Equivalent AC Test Circuit 3	26	33		20	33		dB
PSRR	Power supply rejection ratio[2] (ECL configuration)	Any package f = 0.1MHz[1] Test Circuit 4		23			23		dB
$V_{O\,MAX}$	Maximum differential output voltage swing	$R_L = \infty$ Test Circuit 6, Procedure 3	2.4	3.2		1.7	3.2		V_{P-P}
$V_{IN\,MAX}$	Maximum input amplitude for output duty cycle of 50 ±5%[3]	Test Circuit 5		325			325		mV_{P-P}
t_R	Rise time for 50mV output signal[4]	Test Circuit 5		2.0			2.0		ns

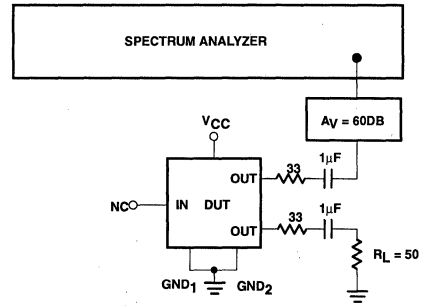
NOTES:
1. Package parasitic capacitance amounts to about 0.2pF.
2. PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use RF filter in V_{CC} line.
3. Guaranteed by linearity and over load tests.
4. t_R defined as 20-80% rise time. It is guaranteed by -3dB bandwidth test.
5. As in all high frequency circuits, a supply bypass capacitor should be located as close to the part as possible.

TEST CIRCUITS

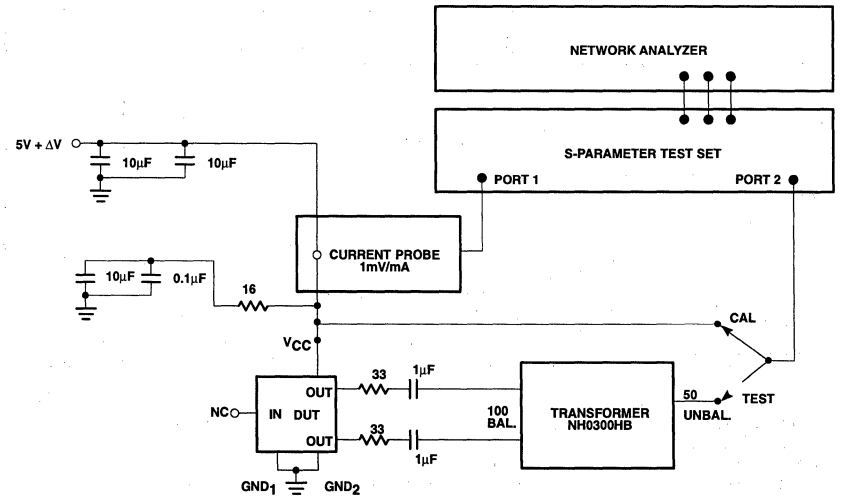
SINGLE-ENDED	DIFFERENTIAL
$R_t = \frac{V_{OUT}}{V_{IN}} 2 \cdot S21 \cdot R$	$R_t = \frac{V_{OUT}}{V_{IN}} 4 \cdot S21 \cdot R$
$R_O = Z_O \left\lvert \frac{1 + S22}{1 - S22} \right\rvert - 33$	$R_O = 2Z_O \left\lvert \frac{1 + S22}{1 - S22} \right\rvert - 66$



Test Circuit 1

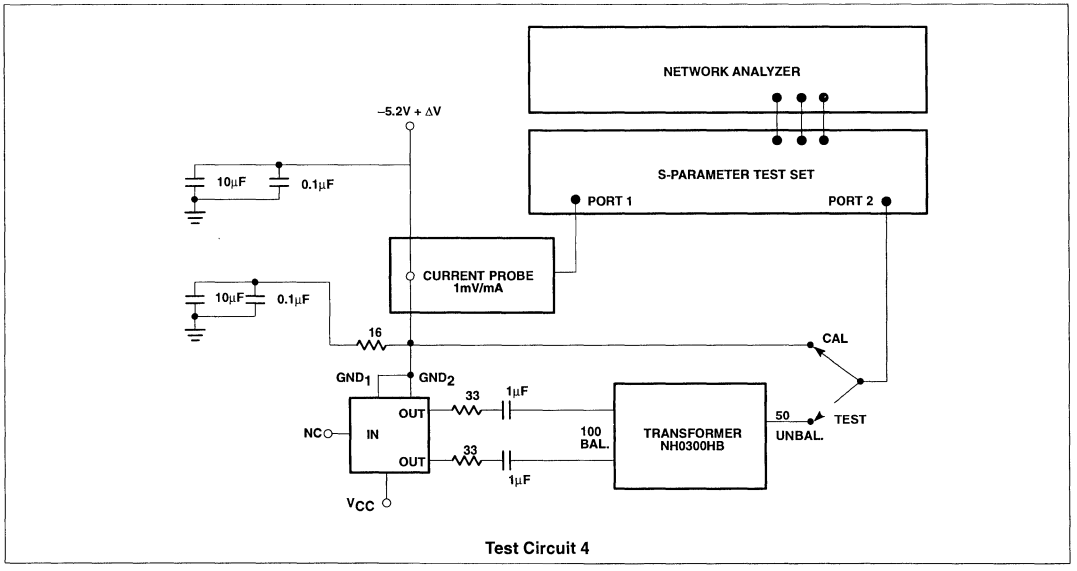


Test Circuit 2

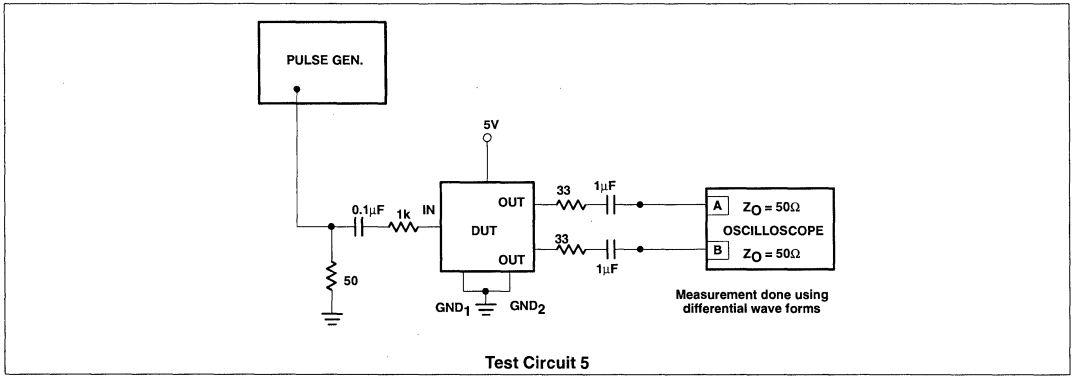


Test Circuit 3

TEST CIRCUITS (Continued)



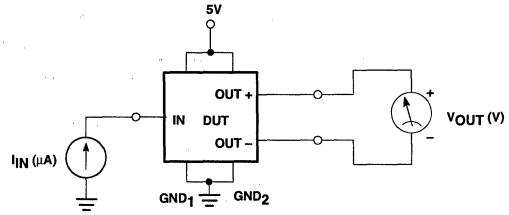
Test Circuit 4

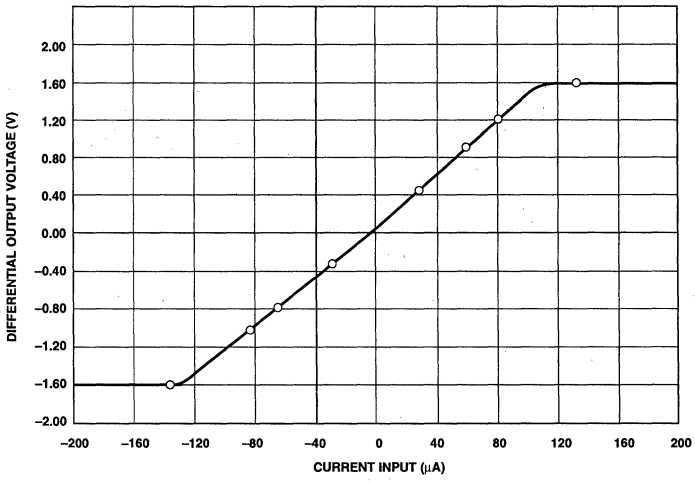


Test Circuit 5

TEST CIRCUITS (Continued)

Typical Differential Output Voltage vs Current Input





NE5212A TEST CONDITIONS

Procedure 1

R_T measured at 30μA

$R_T = (V_{O1} - V_{O2})/(+30\mu A - (-30\mu A))$

Where: V_{O1} Measured at $I_{IN} = +30\mu A$

V_{O2} Measured at $I_{IN} = -30\mu A$

Procedure 2

Linearity = $1 - ABS((V_{OA} - V_{OB}) / (V_{O3} - V_{O4}))$

Where: V_{O3} Measured at $I_{IN} = +60\mu A$

V_{O4} Measured at $I_{IN} = -60\mu A$

$V_{OA} = R_T \cdot (+ 60\mu A) + V_{OB}$

$V_{OB} = R_T \cdot (- 60\mu A) + V_{OB}$

Procedure 3

$V_{OMAX} = V_{O7} - V_{O8}$

Where: V_{O7} Measured at $I_{IN} = +130\mu A$

V_{O8} Measured at $I_{IN} = -130\mu A$

Procedure 4

I_{IN} Test Pass Conditions:

$V_{O7} - V_{O5} > 20mV$ and $V_{O6} - V_{O5} > 20mV$

Where: V_{O5} Measured at $I_{IN} = +800\mu A$

V_{O6} Measured at $I_{IN} = -80\mu A$

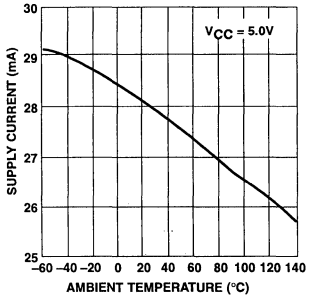
V_{O7} Measured at $I_{IN} = +130\mu A$

V_{O8} Measured at $I_{IN} = -130\mu A$

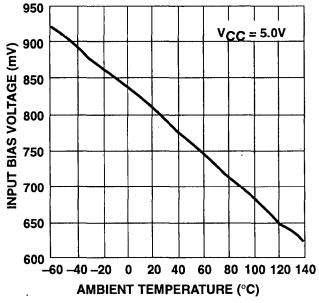
Test Circuit 8

TYPICAL PERFORMANCE CHARACTERISTICS

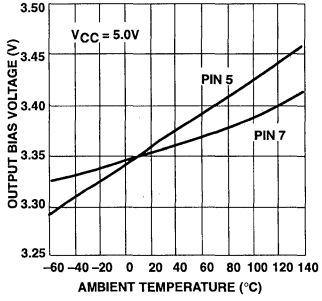
NE5212A Supply Current vs Temperature



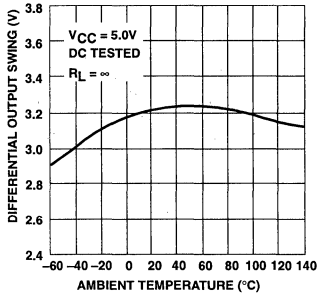
NE5212A Input Bias Voltage vs Temperature



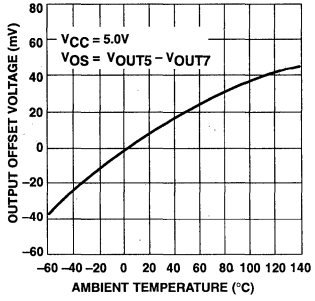
NE5212A Output Bias Voltage vs Temperature



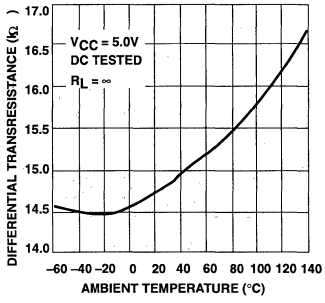
NE5212A Differential Output Swing vs Temperature



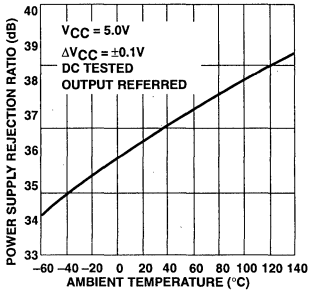
NE5212A Output Offset Voltage vs Temperature



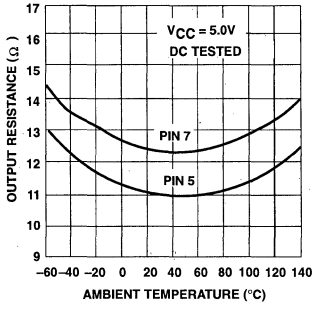
NE5212A Differential Transresistance vs Temperature



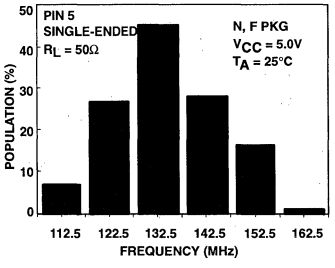
NE5212A Power Supply Rejection Ratio vs Temperature



NE5212A Output Resistance vs Temperature

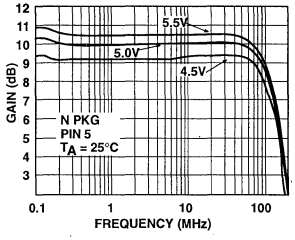


NE5212A Typical Bandwidth Distribution (75 Parts from 3 Wafer Lots)

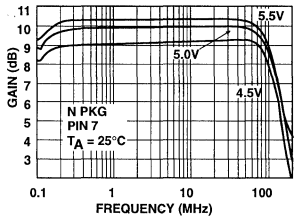


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

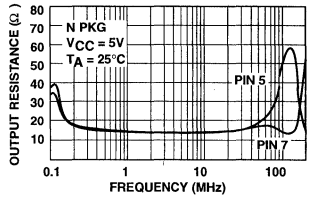
Gain vs Frequency



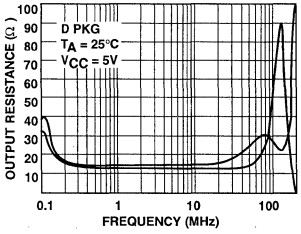
Gain vs Frequency



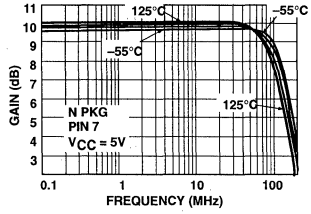
Output Resistance vs Frequency



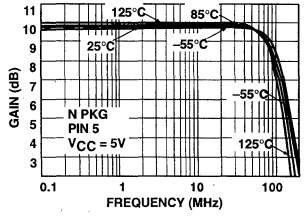
Output Resistance vs Frequency



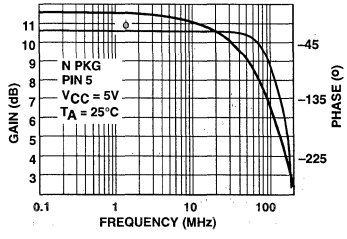
Gain vs Frequency



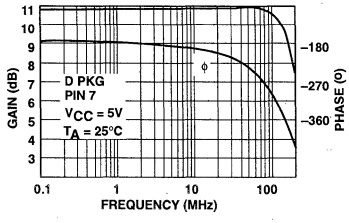
Gain vs Frequency



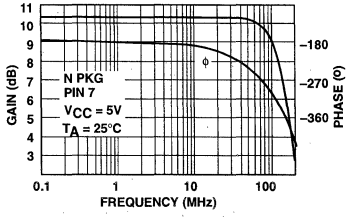
Gain and Phase Shift vs Frequency



Gain and Phase Shift vs Frequency

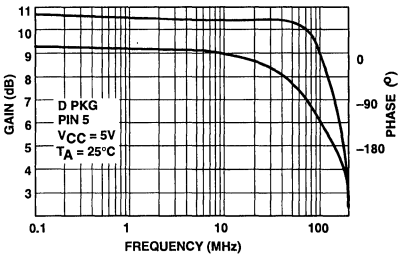


Gain and Phase Shift vs Frequency

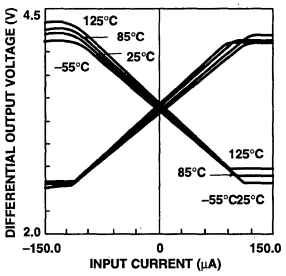


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

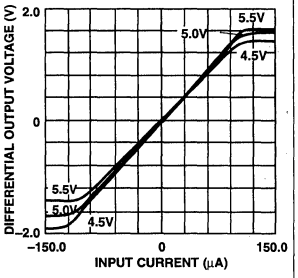
Gain and Phase Shift vs Frequency



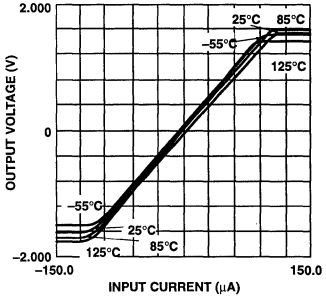
Output Voltage vs Input Current



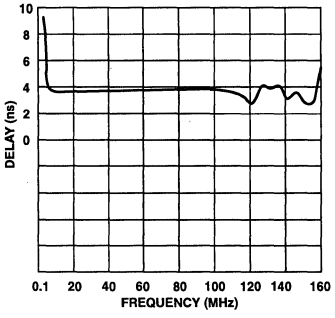
Differential Output Voltage vs Input Current



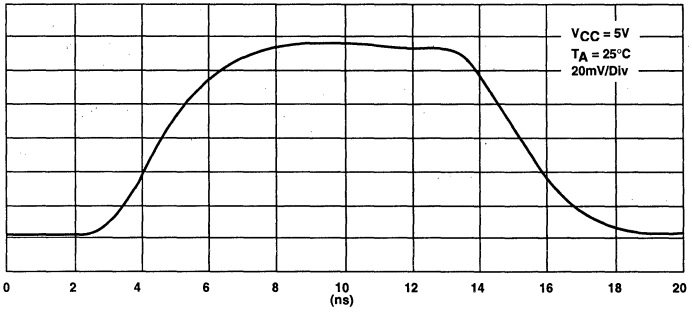
Differential Output Voltage vs Input Current



Group Delay vs Frequency



Output Step Response



THEORY OF OPERATION

Transimpedance amplifiers have been widely used as the preamplifier in fiber-optic receivers. The NE5212A is a wide bandwidth (typically 280MHz) transimpedance amplifier designed primarily for input currents requiring a large dynamic range, such as those produced by a laser diode. The maximum input current before output stage clipping occurs at typically 240μA. The NE5212A is a bipolar transimpedance amplifier which is current driven at the input and generates a differential voltage signal at the outputs. The forward transfer function is therefore a ratio of the differential output voltage to a given input current with the dimensions of ohms. The main feature of this amplifier is a wideband, low-noise input stage which is desensitized to photodiode capacitance variations. When connected to a photodiode of a few picoFarads, the frequency response will not be degraded significantly. Except for the input stage, the entire signal path is differential to provide improved power-supply rejection and ease of interface to ECL type circuitry. A block diagram of the circuit is shown in Figure 1. The input stage (A1) employs shunt-series feedback to stabilize the current gain of the amplifier. The transresistance of the amplifier from the current source to the emitter of Q_3 is approximately the value of the feedback resistor, R_F=3.6kΩ. The gain from the second stage (A2) and emitter followers (A3 and A4) is about two. Therefore, the differential transresistance of the entire amplifier, R_T is

$$R_T = \frac{V_{OUT}(diff)}{I_{IN}} = 2R_F = 2(7.2K) = 14.4k\Omega$$

The single-ended transresistance of the amplifier is typically 3.6kΩ.

The simplified schematic in Figure 2 shows how an input current is converted to a differential output voltage. The amplifier has a single input for current which is referenced to Ground 1. An input current from a laser diode, for example, will be converted into a voltage by the feedback resistor R_F. The transistor Q1 provides most of the open loop gain of the circuit, A_{VOL}≈70. The emitter follower Q_2 minimizes loading on Q_1. The transistor Q_4, resistor R_7, and V_{B1} provide level shifting and interface with the $Q_{15} - Q_{16}$ differential pair of the second stage which is biased with an internal reference, V_{B2}. The differential outputs are derived from emitter followers $Q_{11} - Q_{12}$ which are biased by constant current sources. The collectors of $Q_{11} - Q_{12}$ are bonded to an external pin, V_{CC2}, in order to reduce the feedback to the input stage. The output impedance is about 17Ω single-ended. For ease of performance evaluation, a 33Ω resistor is used in series with each output to match to a 50Ω test system.

BANDWIDTH CALCULATIONS

The input stage, shown in Figure 3, employs shunt-series feedback to stabilize the current gain of the amplifier. A simplified analysis can determine the performance of the amplifier. The equivalent input capacitance, C_{IN}, in parallel with the source, I_S, is approximately 7.5pF, assuming that C_S=0 where C_S is the external source capacitance.

Since the input is driven by a current source the input must have a low input resistance. The input resistance, R_{IN}, is the ratio of the incremental input voltage, V_{IN}, to the corresponding input current, I_{IN} and can be calculated as:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}} = \frac{7.2K}{70} = 103\Omega$$

More exact calculations would yield a higher value of 110Ω.

Thus C_{IN} and R_{IN} will form the dominant pole of the entire amplifier;

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Assuming typical values for R_F = 7.2kΩ, R_{IN} = 110Ω, C_{IN} = 10pF

$$f_{-3dB} = \frac{1}{2\pi (110)\ 10 \cdot 10^{-12}} = 145MHz$$

The operating point of Q1, Figure 2, has been optimized for the lowest current noise without introducing a second dominant pole in the pass-band. All poles associated with subsequent stages have been kept at sufficiently high enough frequencies to yield an overall single pole response. Although wider bandwidths have been achieved by using a cascade input stage configuration, the present solution has the advantage of a very uniform, highly desensitized frequency response because the Miller effect dominates over the external photodiode and stray capacitances. For example, assuming a source capacitance of 1pF, input stage voltage gain of 70, R_{IN} = 60Ω then the total input capacitance, C_{IN} = (1+7.5) pF which will lead to only a 12% bandwidth reduction.

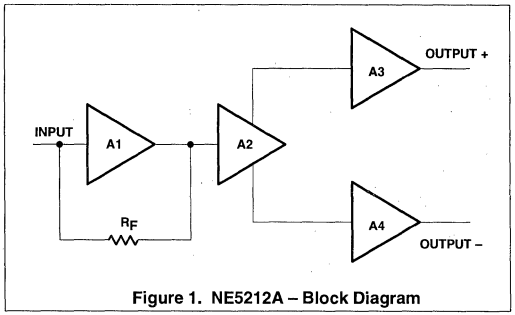


Figure 1. NE5212A – Block Diagram

NOISE

Most of the currently installed fiber-optic systems use non-coherent transmission and detect incident optical power. Therefore, receiver noise performance becomes very important. The input stage achieves a low input referred noise current (spectral density) of 3.5pA/√Hz. The transresistance configuration assures that the external high value bias resistors often required for photodiode biasing will not contribute to the total noise system noise. The equivalent input $_{RMS}$ noise current is strongly determined by the quiescent current of Q_1, the feedback resistor R_F, and the bandwidth; however, it is not dependent upon the internal Miller-capacitance. The measured wideband noise was 66nA in a 200MHz bandwidth.

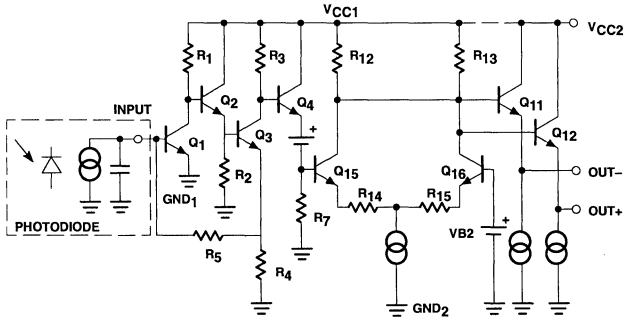


Figure 2. Transimpedance Amplifier

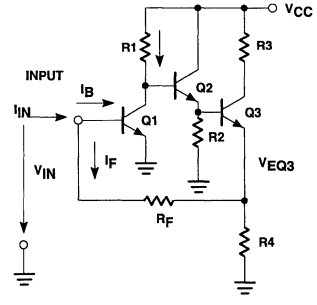


Figure 3. Shunt-Series Input Stage

DYNAMIC RANGE

The electrical dynamic range can be defined as the ratio of maximum input current to the peak noise current:

Electrical dynamic range, D_E, in a 200MHz bandwidth assuming I_{INMAX} = 240μA and a wideband noise of I_{EQ}=52nA$_{RMS}$ for an external source capacitance of C_S = 1pF.

$$D_E = \frac{(Max.\ input\ current)}{(Peak\ noise\ current)}$$

$$D_E(dB) = 20\log\frac{(120 \cdot 10^{-6})}{(\sqrt{2}\ 52nA)}$$

$$D_E(dB) = 20\log\frac{(120\mu A)}{(73nA)} = 64dB$$

In order to calculate the optical dynamic range the incident optical power must be considered.

For a given wavelength λ;

Energy of one Photon = $\frac{hc}{\lambda}$ watt sec (Joule)

Where h=Planck's Constant = 6.6×10^{-34} Joule sec.

c = speed of light = 3×10^8 m/sec

c / λ = optical frequency

No. of incident photons/sec= where P=optical incident power

$$\text{No. of incident photons/sec} = \frac{P}{\frac{hs}{\lambda}}$$

where P = optical incident power

$$\text{No. of generated electrons/sec} = \eta \cdot \frac{P}{\frac{hs}{\lambda}}$$

where η = quantum efficiency

$$= \frac{\text{no. of generated electron hole paris}}{\text{no. of incident photons}}$$

$$\therefore I = \eta \cdot \frac{P}{\frac{hs}{\lambda}} \cdot e \text{ Amps (Coulombs/sec.)}$$

where e = electron charge = 1.6×10^{-19} Coulombs

$$\text{Responsivity } R = \frac{\eta \cdot e}{\frac{hs}{\lambda}} \text{ Amp/watt}$$

$$I = P \cdot R$$

Assuming a data rate of 400 Mbaud (Bandwidth, B=200MHz), the noise parameter Z may be calculated as:[1]

$$Z = \frac{I_{EQ}}{qB} = \frac{52 \cdot 10^{-9}}{(1.6 \cdot 10^{-19})(200 \cdot 10^6)} = 1625\left(\frac{Amp}{Amp}\right)$$

where Z is the ratio of $_{RMS}$ noise output to the peak response to a single hole-electron pair. Assuming 100% photodetector quantum efficiency, half mark/half space digital transmission, 850nm lightwave and using Gaussian approximation, the minimum required optical power to achieve 10^{-9} BER is:

$$P_{avMIN} = 12\frac{hc}{\lambda}B\ Z = 12\ (2.3 \cdot 10^{-19})$$

$$200 \cdot 10^6\ 1625 = 897nW = -30.5dBm,$$

where h is Planck's Constant, c is the speed of light, λ is the wavelength. The minimum input current to the NE5212A, at this input power is:

$$I_{avMIN} = qP_{avMIN}\frac{\lambda}{hc}$$

$$= \frac{897 \cdot 10^{-9} \cdot 1.6 \cdot 10^{-19}}{2.3 \cdot 10^{-19}}$$

$$= 624nA$$

Choosing the maximum peak overload current of I_{avMAX}=120μA, the maximum mean optical power is:

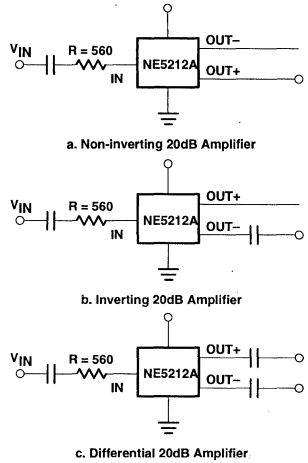


Figure 4. Variable Gain Circuit

$$P_{avMAX} = \frac{hcI_{avMAX}}{\lambda q} = \frac{2.3 \cdot 10^{-19}(120 \cdot 10^{-6})}{1.6 \cdot 10^{-19}}$$

$$= 172\mu W \text{ or } -7.6dBm$$

Thus the optical dynamic range, D_O is:

$D_O = P_{avMAX} - P_{avMIN} = -30.5 - (-7.6) = 22.8dB$.

This represents the maximum limit attainable with the NE5212A operating at 200MHz bandwidth, with a half mark/half space digital transmission at 820nm wavelength.

APPLICATION INFORMATION

Package parasitics, particularly ground lead inductances and parasitic capacitances, can significantly degrade the frequency response. Since the NE5212A has differential outputs which can feed back signals to the input by parasitic package or board layout capacitances, both peaking and attenuating type frequency response shaping is possible. Constructing the board layout so that Ground 1 and Ground 2 have very low impedance paths has produced the best results. This was accomplished by adding a ground-plane stripe underneath the device connecting Ground 1, Pins 8–11, and Ground 2, Pins 1 and 2 on opposite ends of the SO14 package. This ground-plane stripe also provides isolation between the output return currents flowing to either V_{CC2} or Ground 2 and the input photodiode currents to flowing to Ground 1. Without this ground-plane stripe and with large lead inductances on the board, the part may be unstable and oscillate near 800MHz. The easiest way to realize that the part is not functioning normally is to measure the DC voltages at the outputs. If they are not close to their quiescent values of 3.3V (for a 5V supply), then the circuit may be oscillating. Input pin layout necessitates that the photodiode be physically very close to the input and Ground 1. Connecting Pins 3 and 5 to Ground 1 will tend to shield the input but it will also tend to increase the capacitance on the input and slightly reduce the bandwidth.

As with any high-frequency device, some precautions must be observed in order to enjoy reliable performance. The first of these is the use of a well-regulated power supply. The supply must be capable of providing varying amounts of current without significantly changing the voltage level. Proper supply bypassing requires that a good quality 0.1µF high-frequency capacitor be inserted between V_{CC1} and V_{CC2}, preferably a chip capacitor, as close to the package pins as possible. Also, the parallel combination of 0.1µF capacitors with 10µF tantalum capacitors from each supply, V_{CC1} and V_{CC2}, to the ground plane should provide adequate decoupling. Some applications may require an RF choke in series with the power supply line. Separate analog and digital ground leads must be maintained and printed circuit board ground plane should be employed whenever possible.

BASIC CONFIGURATION

A trans resistance amplifier is a current-to-voltage converter. The forward transfer function then is defined as voltage out divided by current in, and is stated in ohms. The lower the source resistance, the higher the gain. The NE5212A has a differential transresistance of 14kΩ typically and a single-ended transresistance of 7kΩ typically. The device has two outputs: inverting and non-inverting. The output
voltage in the differential output mode is twice that of the output voltage in the single-ended mode. Although the device can be used without coupling capacitors, more care is required to avoid upsetting the internal bias nodes of the device. Figure 4 shows some basic configurations.

VARIABLE GAIN

Figure 5 shows a variable gain circuit using the NE5212A and the NE5230 low voltage op amp. This op amp is configured in a non-inverting gain of five. The output drives the gate of the SD210 DMOS FET. The series resistance of the FET changes with this output voltage which in turn changes the gain of the NE5212A. This circuit has a distortion of less than 1% and a 25dB range, from -42.2dBm to -15.9dBm at 50MHz, and a 45dB range, from -60dBm to -14.9dBm at 10MHz with 0 to 1V of control voltage at V_{CC}.

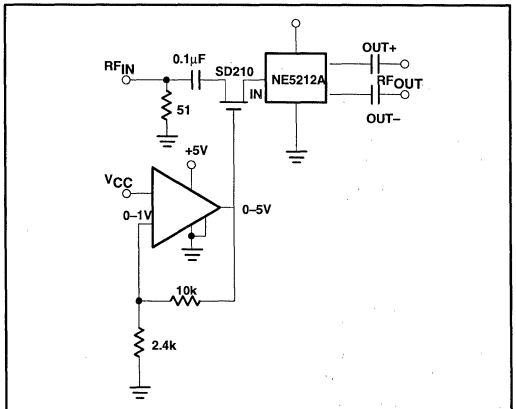


Figure 5. Variable Gain Circuit

16MHZ CRYSTAL OSCILLATOR

Figure 6 shows a 16MHz crystal oscillator operating in the series resonant mode using the NE5212A. The non-inverting input is fed back to the input of the NE5212A in series with a 2pF capacitor. The output is taken from the inverting output.

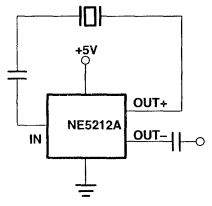


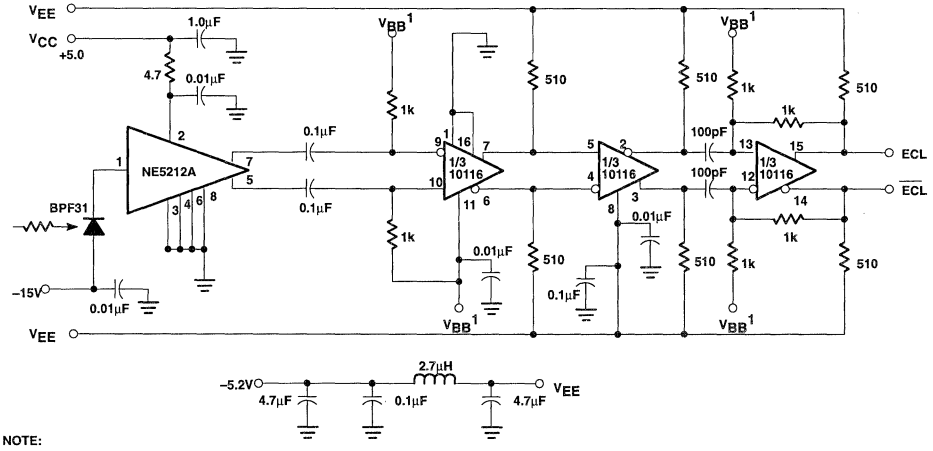
Figure 6. 16MHz Crystal Oscillator

DIGITAL FIBER OPTIC RECEIVER

Figures 7 and 8 show a fiber optic receiver using off-the-shelf components.

The receiver shown in Figure 7 uses the NE5212A, the Philips Semiconductors 10116 ECL line receiver, and Philips/Amperex BPF31 PIN diode. The circuit is a capacitor-coupled receiver and utilizes positive feedback in the last stage to provide the hysteresis. The amount of hysteresis can be tailored to the individual application by changing the values of the feedback resistors to maintain the desired balance between noise immunity and sensitivity. At room temperature, the circuit operates at 50Mbaud with a BER of 10E-10 and over the automotive temperature range at 40Mbaud with a BER of 10E-9. Higher speed experimental diodes have been used to operate this circuit at 220Mbaud with a BER of 10E-10.

Figure 8 depicts a TTL receiver using the NE5212A and the NE5214 fast amplifier system along with the Philips/Amperex PIN diode. The system shown is optimized for 50 Mb/s Non Return to Zero (NRZ) data. A link status indication is provided along with a jamming function when the input level is below a user-programmable threshold level.



NOTE:
1. Tie all V_{BB} points together.

Figure 7. ECL Fiber Optic Receiver

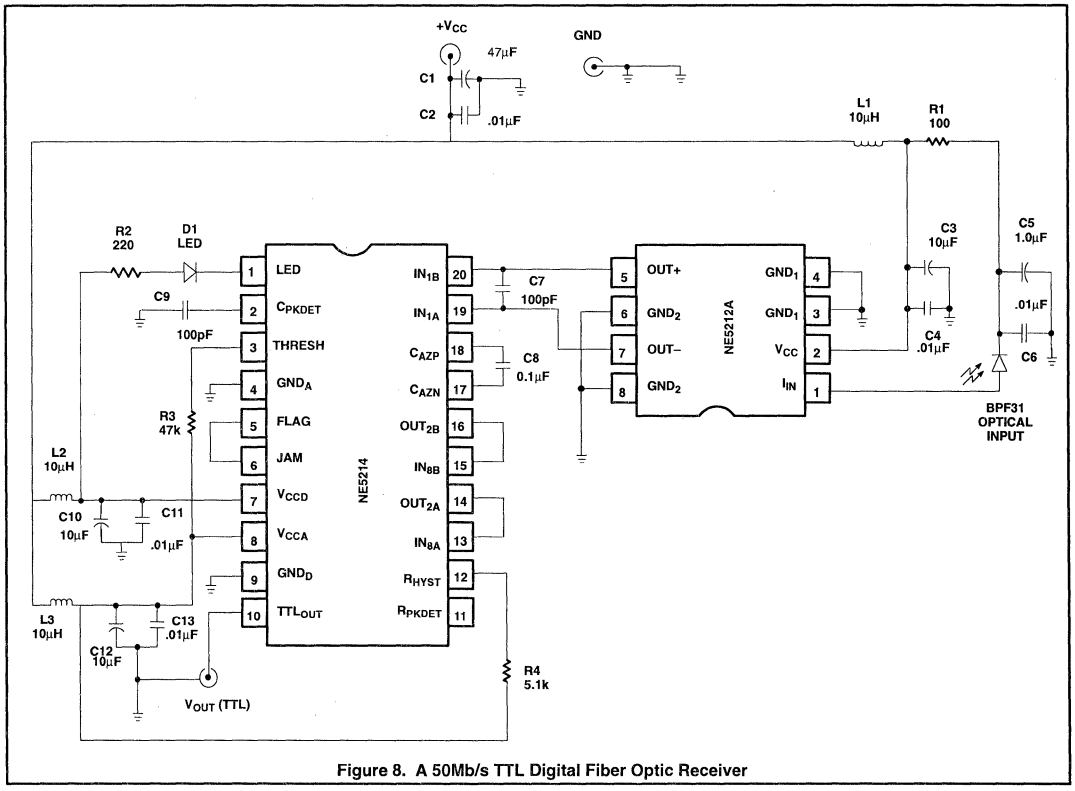


Figure 8. A 50Mb/s TTL Digital Fiber Optic Receiver

Postamplifier with link status indicator — NE/SA5214

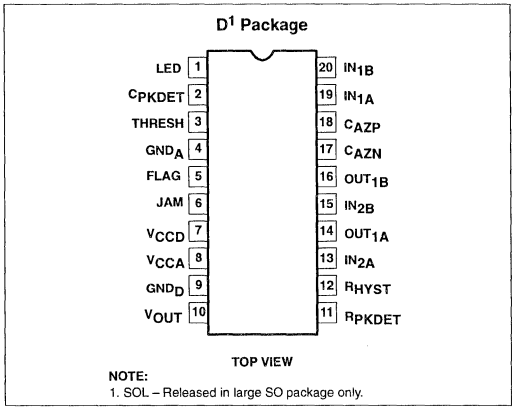
DESCRIPTION

The NE/SA5214 is a 75MHz postamplifier system designed to accept low level high-speed signals. These signals are converted into a TTL level at the output. The NE5214 can be DC coupled with the previous transimpedance stage using NE5210, NE5211 or NE5212 transimpedance amplifiers. This "system on a chip" features an auto-zeroed first stage with noise shaping, a symmetrical limiting second stage, and a matched rise/fall time TTL output buffer. The system is user-configurable to provide noise filtering, adjustable input thresholds and hysteresis. The threshold capability allows the user to maximize signal-to-noise ratio, insuring a low Bit Error Rate (BER). An Auto-Zero loop can be used to minimize the number of external coupling capacitors to one. A signal absent flag indicates when signals are below threshold. Additionally, the low signal condition forces the overall TTL output to a logical Low level. User interaction with this "jamming" system is available. The NE/SA5214 is packaged in a standard 20-pin surface-mount package and typically consumes 42mA from a standard 5V supply. The NE/SA5214 is designed as a companion to the NE/SA5211/5212 transimpedance amplifiers. These differential preamplifiers may be directly coupled to the post-amplifier inputs. The NE/SA5212/5214 or NE/SA5211/5214 combinations convert nanoamps of photodetector current into standard digital TTL levels.

APPLICATIONS

- Fiber optics
- Communication links in Industrial and/or Telecom environment with high EMI/RFI
- Local Area Networks (LAN)
- Metropolitan Area Networks (MAN)
- Synchronous Optical Networks (SONET)
- RF limiter

PIN CONFIGURATION



NOTE:
1. SOL – Released in large SO package only.

FEATURES

- Postamp for the NE/SA5211/5212 preamplifier family
- Wideband operation: typical 75MHz (100MBaud NRZ)
- Interstage filtering/equalization possible
- Single 5V supply
- Low signal flag
- Low signal output disable
- Link status threshold and hysteresis programmable
- LED driver (normally ON with above threshold signal)
- Fully differential for excellent PSRR
- Auto-zero loop for DC offset cancellation
- 2kV ElectroStatic Discharge (ESD) protection

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) Package	0 to +70°C	NE5214D	0172D
20-Pin Plastic Small Outline Large (SOL) Package	-40°C to +85°C	SA5214D	0172D

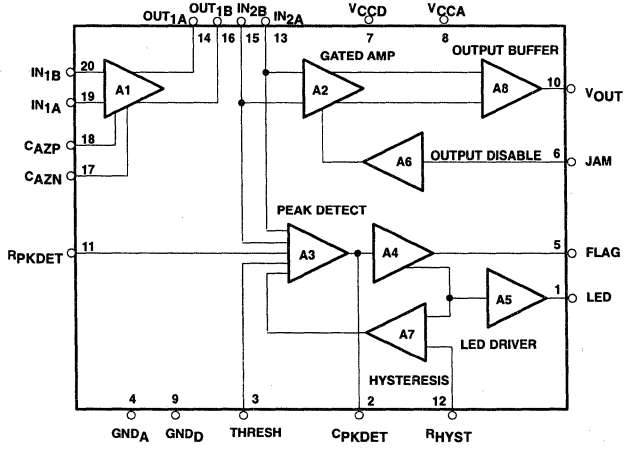
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNIT
		NE5214	SA5214	
V_{CCA}	Power supply	+6	+6	V
V_{CCD}	Power supply	+6	+6	V
T_A	Operating ambient temperature range	0 to +70	-40 to +85	°C
T_J	Operating junction temperature range	-55 to +150	-55 to +150	°C
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C
P_D	Power dissipation	300	300	mW
V_{IJ}	Jam input voltage	-0.5 to 5.5	-0.5 to 5.5	V

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	LED	Output for the LED driver. Open collector output transistor with 125Ω series limiting resistor. An above threshold signal turns this transistor ON.
2	C_{PKDET}	Capacitor for the peak detector. The value of this capacitor determines the detector response time to the signal, supplementing the internal 10pF capacitor.
3	THRESH	Peak detector threshold resistor. The value of this resistor determines the threshold level of the peak detector.
4	GND_A	Device analog ground pin.
5	FLAG	Peak detector digital output. When this output is LOW, there is data present above the threshold. This pin is normally connected to the JAM pin and has a TTL fanout of two.
6	JAM	Input to inhibit data flow. Sending the pin HIGH forces TTL DATA OUT ON, Pin 10, LOW. This pin is normally connected to the FLAG pin and is TTL-compatible.
7	V_{CCD}	Power supply pin for the digital portion of the chip.
8	V_{CCA}	Power supply pin for the analog portion of the chip.
9	GND_D	Device digital ground pin.
10	V_{OUT}	TTL output pin with a fanout of five.
11	R_{PKDET}	Peak detector current resistor. The value of this resistor determines the amount of discharge current available to the peak detector capacitor, C_{PKDET}.
12	R_{HYST}	Peak detector hysteresis resistor. The value of this resistor determines the amount of hysteresis in the peak detector.
13	IN_{2A}	Non-inverting input to amplifier A2.
14	OUT_{1A}	Non-inverting output of amplifier A1.
15	IN_{2B}	Inverting input to amplifier A2.
16	OUT_{1B}	Inverting output of amplifier A1.
17	C_{AZN}	Auto-Zero capacitor pin (Negative terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
18	C_{AZP}	Auto-Zero capacitor pin (Positive terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
19	IN_{1A}	Non-inverting input of the preamp A1.
20	IN_{1B}	Inverting input of the preamp A1.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING		UNIT
		NE5214	SA5214	
V_{CCA}	Supply voltage	4.75 to 5.25	4.75 to 5.25	V
V_{CCD}	Power supply	4.75 to 5.25	4.75 to 5.25	V
T_A	Ambient temperature range	0 to +70	-40 to +85	°C
T_J	Operating junction temperature range	0 to +95	-40 to +110	°C
P_D	Power dissipation	250	250	mW

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at V_{CCA}=V_{CCD}=+5.0V unless otherwise specified. Typical data applies at V_{CCA}=V_{CCD}=+5.0V and T_A=25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5214			SA5214			
			Min	Typ	Max	Min	Typ	Max	
I_{CCA}	Analog supply current			30	36		30	37.2	mA
I_{CCD}	Digital supply current (TTL, Flag, LED)			10	13.3		10	13.5	mA
V_{I1}	A1 input bias voltage (+/- inputs)		3.11	3.4	3.68	3.08	3.4	3.70	V
V_{O1}	A1 output bias voltage (+/- outputs)		3.17	3.8	4.45	3.10	3.8	4.50	V
A_{V1}	A1 DC gain (without Auto-Zero)			30			30		dB
$A1_{PSRR}$	A1 PSRR (v_{CCA}, V_{CCD})	V_{CCA}=V_{CCD}=4.75 to 5.25V		60			60		dB
$A1_{CMRR}$	A1 CMRR	ΔV_{CM}=200mV		60			60		dB
V_{I2}	A2 input bias voltage (+/- inputs)		3.59	3.7	3.85	3.56	3.7	3.86	V
V_{OH}	High-level TTL output voltage	I_{OH}=-200µA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level TTL output voltage	I_{OL}=8mA		0.3	0.4		0.3	0.4	V
I_{OH}	High-level TTL output current	V_{OUT}=2.4V		-40	-26		-40	-24.4	mA
I_{OL}	Low-level TTL output current	V_{OUT}=0.4V	8.0	30		7.0	30		mA
I_{OS}	Short-circuit TTL output current	V_{OUT}=0.0V		-95			-95		mA
V_{THRESH}	Threshold bias voltage	Pin 3 Open		0.75			0.75		V
V_{RPKDET}	RPKDET	Pin 11 Open		0.72			0.72		V
V_{RHYST}	RHYST bias voltage	Pin 12 Open		0.72			0.72		V
V_{IHJ}	High-level jam input voltage		2.0			2.0			V
V_{ILJ}	Low-level jam input voltage				0.8			0.8	V
I_{IHJ}	High-level jam input current	V_{IJ}=2.7V			20			30	µA
I_{ILJ}	Low-level jam input current	V_{IJ}=0.4V	-450	-240		-485	-240		µA
V_{OHF}	High-level flag output voltage	I_{OH}=-80µA	2.4	3.8		2.4	3.8		V
V_{OLF}	Low-level flag output voltage	I_{OL}=3.2mA		0.33	0.4		0.33	0.4	V
I_{OHF}	High-level flag output current	V_{OUT}=2.4V		-18	-5.3		-18	-5	mA
I_{OLF}	Low-level flag output current	V_{OUT}=0.4V	3.6	10		3.25	10		mA
I_{SCF}	Short-circuit flag output current	V_{OUT}=0.0V	-60	-40	-25	-61	-40	-26	mA
I_{LEDH}	LED ON maximum sink current	V_{LED}=3.0V	13	22	80	8	22	80	mA

AC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5214			SA5214			
			Min	Typ	Max	Min	Typ	Max	
f_{OP}	Maximum operating frequency	Test circuit	60	75		60	75		MHz
BW_{A1}	Small signal bandwidth (differential OUT_1/IN_1)	Test circuit		75			75		MHz
V_{INH}	Maximum Functional A1 input signal (single ended)	Test Circuit		1.6			1.6		V_{P-P}
V_{INL}	Minimum Functional A1 input signal (single ended)	Test CIrcuit[1]		12			12		mV_{P-P}
R_{IN1}	Input resistance (differential at IN_1)			1200			1200		Ω
C_{IN1}	Input capacitance (differential at IN_1)			2			2		pF
R_{IN2}	Input resistance (differential at IN_2)			1200			1200		Ω
C_{IN2}	Input capacitance (differential at IN_2)			2			2		pF
R_{OUT1}	Output resistance (differential at OUT_1)			25			25		Ω
C_{OUT1}	Output capacitance (differential at OUT_1)			2			2		pF
V_{HYS}	Hysteresis voltage	Test circuit		3			3		mV_{P-P}
V_{THR}	Threshold voltage range (FLAG ON)	Test circuit, @ 50MHz R_{RHYST}=5k R_{THRESH}=47k		12			12		mV_{P-P}
t_{TLH}	TTL Output Rise Time 20% to 80%	Test Circuit		1.3			1.3		ns
t_{THL}	TTL Output Fall Time 80% to 20%	Test Circuit		1.2			1.2		ns
t_{RFD}	t_{TLH}/t_{THL} mismatch			0.1			0.1		ns
t_{PWD}	Pulse width distortion of output	$50mV_{P-P}$, 1010. . .input Distortion= $\left\lvert\frac{T_H-T_L}{T_H+T_L}\right\rvert 10^2$		2.5			2.5		%

NOTES:

1. The NE/SA5214 is capable of detecting a much lower input level. Operation under $12mV_{P-P}$ cannot be guaranteed by present day automatic testers.

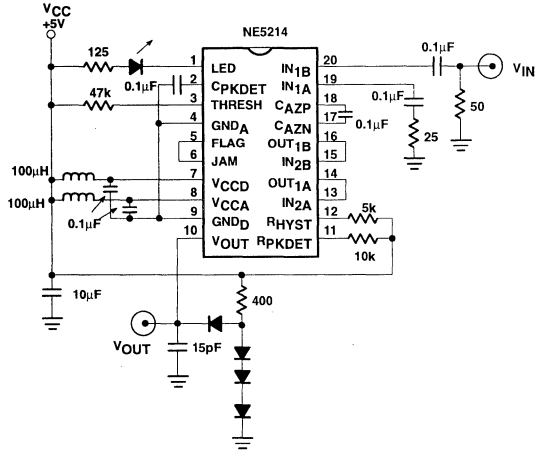
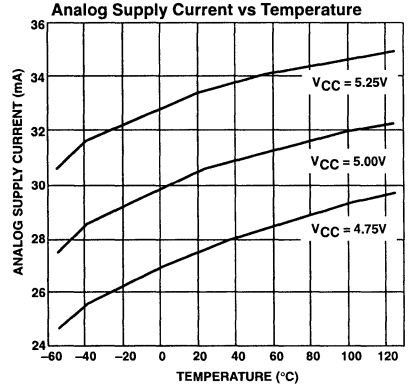
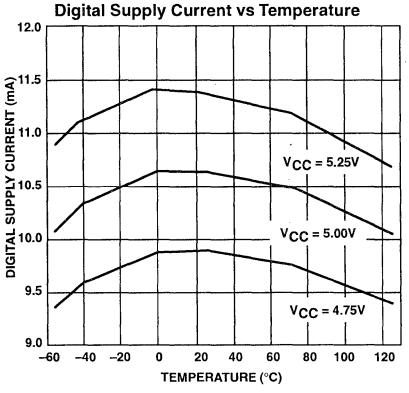
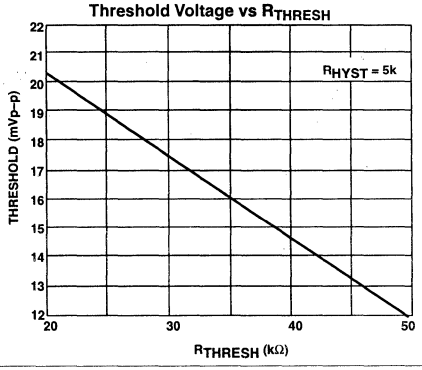


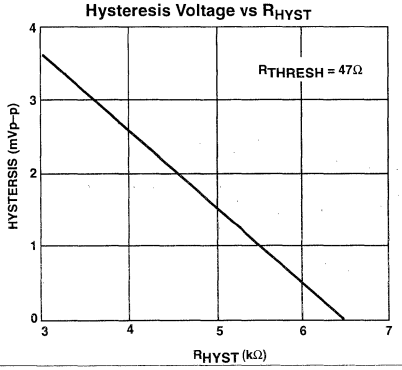
Figure 1. AC Test Circuit

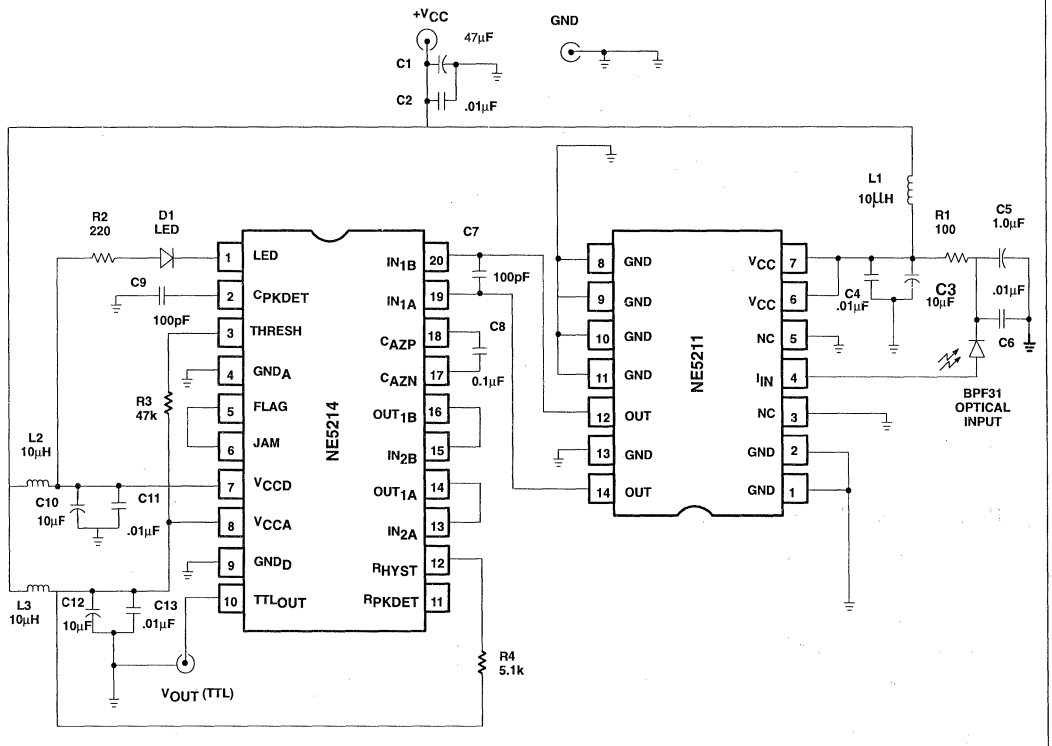
TYPICAL PERFORMANCE CHARACTERISTICS











NOTE:
The NE5211/NE5214 combination can operate at data rates in excess of 100Mb/s NRZ.

Figure 2. A 50Mb/s Fiber Optic Receiver

THEORY OF OPERATION AND APPLICATION INFORMATION

The NE 5214 postamplifier system is a highly integrated chip that provides up to 60dB of gain at 60MHz, to bring mV level signals up to TTL levels.

The NE5214 contains eight amplifier blocks (see Block Diagram). The main signal path is made up of a cascade of limiting stages: A1, A2 and A8. The A3-A4-A7 path performs a wideband full-wave rectification of the input signal with adjustable hysteresis and decay times. It outputs a TTL HIGH on the "FLAG" output (Pin 5) when the input is below a user adjustable threshold. An on-chip LED driver turns the external LED to the ON state when the input signal is above the threshold. In a typical application the "FLAG" output is tied back to the "JAM" input; this forces the TTL data OUT into a LOW state when no signal is present at the input.

An auto zero loop allows the NE5214 to be directly connected to a transimpedance amplifier such as the NE5210, NE5211, or NE5212 without coupling capacitors. This auto-zero loop cancels the transimpedance amplifier's DC offset, the NE5214 A1 offset, and the data-dependent offset in the PIN diode/transimpedance amplifier combination. For more information on the NE5214 Theory of Operation, please refer to paper titled "A Low Cost 100 MBaud Fiber-Optic Receiver" by W. Mack et al.

A typical application of the NE5214 postamplifier is depicted in Figure 2. The system uses the NE5211 transimpedance amplifier which has a 28k differential transimpedance gain and a -3dB bandwidth of 140MHz. This typical application is optimized for a 50 Mb/s Non Return to Zero (NRZ) bit stream.

As the system's gain bandwidth product is very high, it is crucial to employ good RF design and printed circuit board layout techniques to prevent the system from becoming unstable.

For more information on this application, please refer to AB 1432.

Postamplifier with link status indicator — NE/SA5217

DESCRIPTION

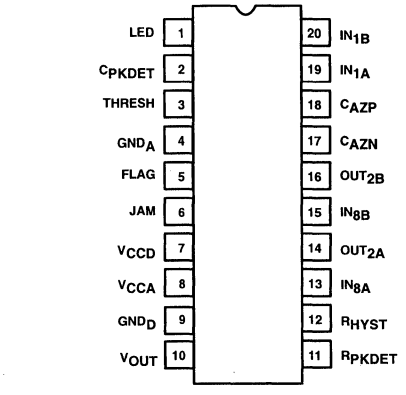
The NE/SA5217 is a 75MHz postamplifier system designed to accept low level high-speed signals. These signals are converted into a TTL level at the output. The NE5217 can be DC coupled with the previous transimpedance stage using NE5210, NE5211 or NE5212A transimpedance amplifiers. The main difference between the NE5217 and the NE5214 is that the NE5217 does not make the output of A1 and input of A2 accessible; instead, it brings out the output of A2 and the input of A8 thus activating the on-chip Schmitt trigger function by connecting two external capacitors. The result is that a much longer string of 1s and 0s, in the bit stream, can be tolerated. This "system on a chip" features an auto-zeroed first stage with noise shaping, a symmetrical limiting second stage, and a matched rise/fall time TTL output buffer. The system is user-configurable to provide adjustable input threshold and hysteresis. The threshold capability allows the user to maximize signal-to-noise ratio, thereby insuring a low Bit Error Rate (BER). An auto-zero loop can be used to replace two input coupling capacitors with a single Auto Zero (AZ) capacitor. A signal absent flag indicates when signals are below threshold. The low signal condition forces the TTL output to the last logic state. User interaction with this "jamming" system is available. The NE/SA5217 is packaged in a standard 20-pin surface-mount package and typically consumes 40mA from a standard 5V supply. The NE/SA5217 is designed as a companion to the NE/SA5211/5212A and NE5210 transimpedance amplifiers. These differential preamplifiers may be directly coupled to the postamplifier inputs. The NE5210/5217, NE/SA5211/5217 or NE/SA5212A/5217 combinations convert nanoamps of photodetector current into standard digital TTL levels.

APPLICATIONS

- Fiber optics
- Communication links in Industrial and/or Telecom environment with high EMI/RFI
- Local Area Networks (LAN)
- Synchronous Optical Networks (SONET) STS-1
- RF limiter
- Good for 2^{23} -1 pseudo random bit stream

PIN CONFIGURATION

D[1] Package



NOTE:
1. SOL - Released in large SO package only.

FEATURES

- Postamp for the NE/SA5211/5212A. NE5210 preamplifier family
- Wideband operation: typical 75MHz (150MBaud NRZ)
- Interstage filtering/equalization possible
- Single 5V supply
- Low signal flag
- Output disable
- Link status threshold and hysteresis programmable
- LED driver (normally ON with above threshold signal)
- Fully differential for excellent PSRR
- Auto-zero loop for DC offset cancellation
- 2kV ElectroStatic Discharge (ESD) protection

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) Package	0 to +70°C	NE5217D	0172D
20-Pin Plastic Small Outline Large (SOL) Package	-40 to +85°C	SA5217D	0172D

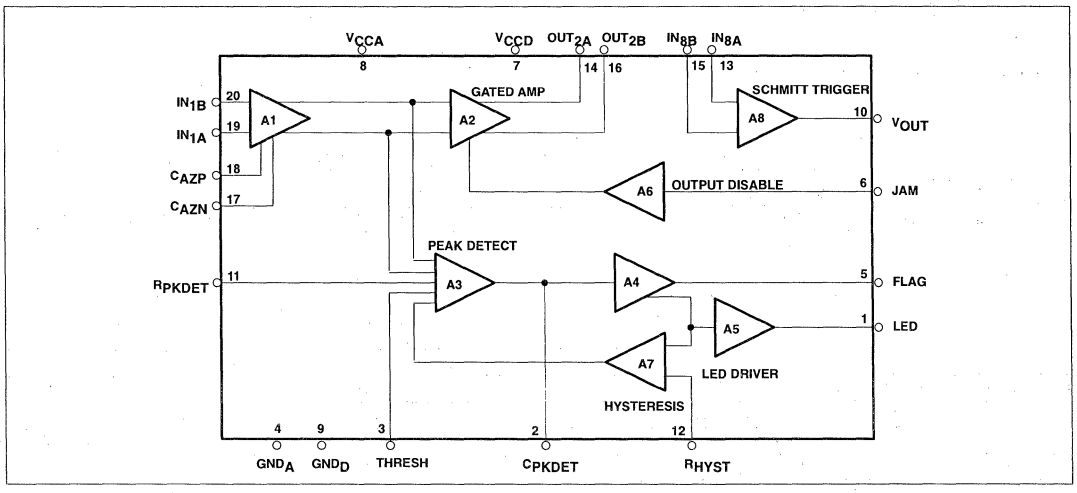
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNIT
		NE5214	SA5214	
V_{CCA}	Power supply	+6	+6	V
V_{CCD}	Power supply	+6	+6	V
T_A	Operating ambient temperature range	0 to +70	-40 to +85	°C
T_J	Operating junction temperature range	-55 to +150	-55 to +150	°C
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C
P_D	Power dissipation	1.4	1.4	W
V_{IJ}	Jam input voltage	-0.5 to 5.5	-0.5 to 5.5	V

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	LED	Output for the LED driver. Open collector output transistor with 125Ω series limiting resistor. An above threshold signal turns this transistor ON.
2	C_{PKDET}	Capacitor for the peak detector. The value of this capacitor determines the detector response time to the signal, supplementing the internal 10pF capacitor.
3	THRESH	Peak detector threshold resistor. The value of this resistor determines the threshold level of the peak detector.
4	GND_A	Device analog ground pin.
5	FLAG	Peak detector digital output. When this output is LOW, there is data present above the threshold. This pin is normally connected to the JAM pin and has a TTL fanout of two.
6	JAM	Input to inhibit data flow. Sending the pin HIGH forces TTL DATA OUT ON, Pin 10, LOW. This pin is normally connected to the FLAG pin and is TTL-compatible.
7	V_{CCD}	Power supply pin for the digital portion of the chip.
8	V_{CCA}	Power supply pin for the analog portion of the chip.
9	GND_D	Device digital ground pin.
10	V_{OUT}	TTL output pin with a fanout of five.
11	R_{PKDET}	Peak detector current resistor. The value of this resistor determines the amount of discharge current available to the peak detector capacitor, C_{PKDET}.
12	R_{HYST}	Peak detector hysteresis resistor. The value of this resistor determines the amount of hysteresis in the peak detector.
13	IN_{8A}	Non-inverting input to amplifier A8.
14	OUT_{2A}	Non-inverting output of amplifier A2.
15	IN_{8B}	Inverting input to amplifier A8.
16	OUT_{2B}	Inverting output of amplifier A2.
17	C_{AZN}	Auto-Zero capacitor pin (Negative terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
18	C_{AZP}	Auto-Zero capacitor pin (Positive terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
19	IN_{1A}	Non-inverting input of the preamp A1.
20	IN_{1B}	Inverting input of the preamp A1.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING		UNIT
		NE5217	SA5217	
V_{CCA}	Power supply	4.5 to 5.5	4.5 to 5.5	V
V_{CCD}	Power supply	4.5 to 5.5	4.5 to 5.5	V
T_A	Ambient temperature range	0 to +70	-40 to +85	°C
T_J	Operating junction temperature range	0 to +95	-40 to +110	°C
P_D	Power dissipation	300	300	mW

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5217			SA5217			
			Min	Typ	Max	Min	Typ	Max	
I_{CCA}	Analog supply current			30	36		30	37.2	mA
I_{CCD}	Digital supply current (TTL, Flag, LED)			10	13.3		10	13.5	mA
V_{I1}	A1 input bias voltage (A,B inputs)		3.11	3.4	3.68	3.08	3.4	3.70	V
V_{O2}	A1 output bias voltage (A,B outputs)		3.17	3.8	4.45	3.10	3.8	4.50	V
V_{I8L}	A8 input bias voltage Low (A,B inputs)		3.40	3.55	3.68	3.40	3.55	3.68	V
V_{I8H}	A8 input bias voltage High (A,B inputs)		3.70	3.91	4.10	3.68	3.91	4.12	V
V_{OH}	High-level TTL output voltage	I_{OH}=-200µA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level TTL output voltage	I_{OL}=8mA		0.3	0.4		0.3	0.4	V
I_{OH}	High-level TTL output current	V_{OUT}=2.4V		-40	-26		-40	-24.4	mA
I_{OL}	Low-level TTL output current	V_{OUT}=0.4V	8.0	30		7.0	30		mA
I_{OS}	Short-circuit TTL output current	V_{OUT}=0.0V		-95			-95		mA
V_{THRESH}	Threshold bias voltage	Pin 3 Open		0.75			0.75		V
V_{RPKDET}	RPKDET	Pin 11 Open		0.72			0.72		V
V_{RHYST}	RHYST bias voltage	Pin 12 Open		0.72			0.72		V
V_{IHJ}	High-level jam input voltage		2.0			2.0			V
V_{ILJ}	Low-level jam input voltage				0.8			0.8	V
I_{IHJ}	High-level jam input current	V_{IJ}=2.7V			20			30	µA
I_{ILJ}	Low-level jam input current	V_{IJ}=0.4V	-450	-240		-485	-240		µA
V_{OHF}	High-level flag output voltage	I_{OH}=-80µA	2.4	3.8		2.4	3.8		V
V_{OLF}	Low-level flag output voltage	I_{OL}=3.2mA		0.33	0.4		0.33	0.4	V
I_{OHF}	High-level flag output current	V_{OUT}=2.4V		-18	-5.3		-18	-5	mA
I_{OLF}	Low-level flag output current	V_{OUT}=0.4V	3.6	10		3.25	10		mA
I_{SCF}	Short-circuit flag output current	V_{OUT}=0.0V	-60	-40	-25	-61	-40	-26	mA
I_{LEDH}	LED ON maximum sink current	V_{LED}=3.0V	13	22	80	8	22	80	mA

AC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5217			SA5217			
			Min	Typ	Max	Min	Typ	Max	
f_{OP}	Maximum operating frequency	Test circuit	60	75		60	75		MHz
V_{INH}	Maximum Functional A1 input signal (single ended)	Test Circuit		1.6			1.6		V_{P-P}
V_{INL}	Minimum Functional A1 input signal (single-ended)	Test CIrcuit		6			6		mV_{P-P}
	Minimum Functional A1 input signal (differential)			3			3		
	Minimum input sensitivity for output BER $\leq 10^{-9}$ (single-ended)	PRBS = $2^{23}-1$		9			9		mV_{P-P}
	Minimum input sensitivity for output BER $\leq 10^{-9}$ (differential)			4.5			4.5		
R_{IN1}	Input resistance (differential at IN_1)	PRBS = $2^{23}-1$		1200			1200		Ω
C_{IN1}	Input capacitance (differential at IN_1)			2			2		pF
R_{IN8}	Input resistance (differential at IN_2)			2000			2000		Ω
C_{IN2}	Input capacitance (differential at IN_2)			2			2		pF
R_{OUT2}	Output resistance (differential at OUT_2)			25			25		Ω
C_{OUT2}	Output capacitance (differential at OUT_2)			2			2		pF
V_{HYS}	Hysteresis voltage range (single-ended)	Test circuit, $T_A = 25°C$ R_{RHYST}=5k R_{THRESH}=33k		10			10		mV_{P-P}
	Hysteresis voltage range (differential)			5			5		
V_{THR}	Threshold voltage (single-ended)	(FLAG Low) Test circuit, @ 50MHz		19			19		mV_{P-P}
	Threshold voltage (differential)	R_{RHYST}=4k R_{THRESH}=33k		9.5			9.5		
t_{TLH}	TTL Output Rise Time 20% to 80%	Test Circuit		1.3			1.3		ns
t_{THL}	TTL Output Fall Time 80% to 20%	Test Circuit		1.2			1.2		ns
t_{RFD}	t_{TLH}/t_{THL} mismatch			0.1			0.1		ns
t_{PWD}	Pulse width distortion of output	50mV_{P-P}, 1010. . .input Distortion = $\frac{T_H - T_L}{T_H + T_L} 10^2$		TBD			TBD		%

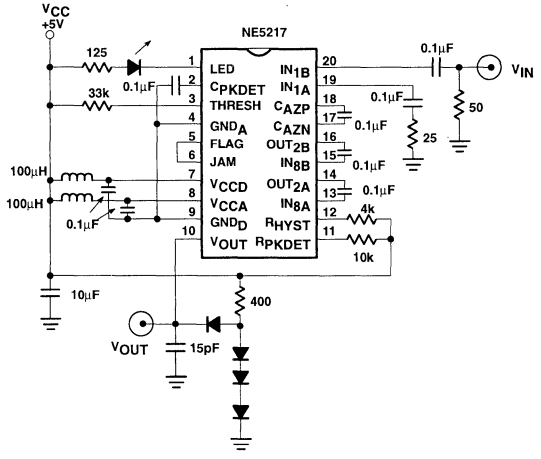
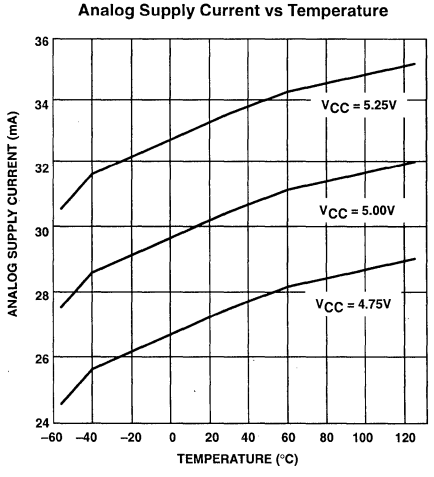
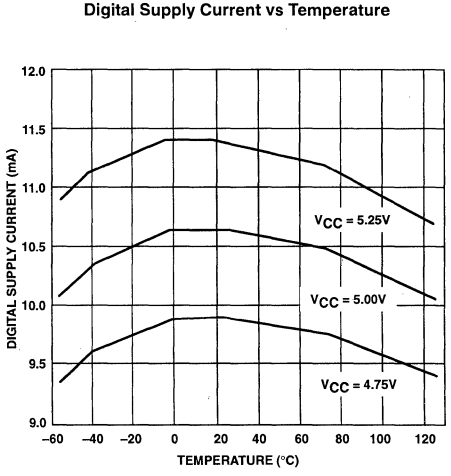


Figure 1. AC Test Circuit

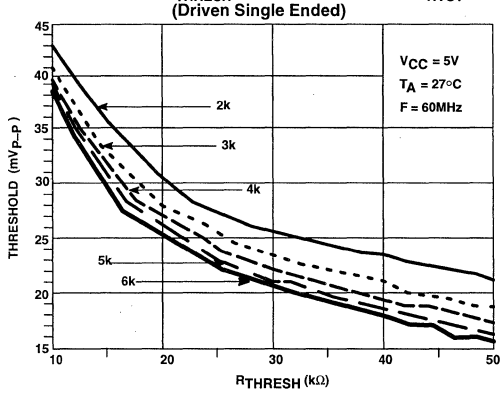
TYPICAL PERFORMANCE CHARACTERISTICS



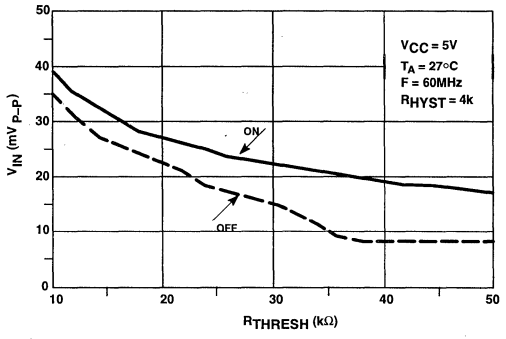


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

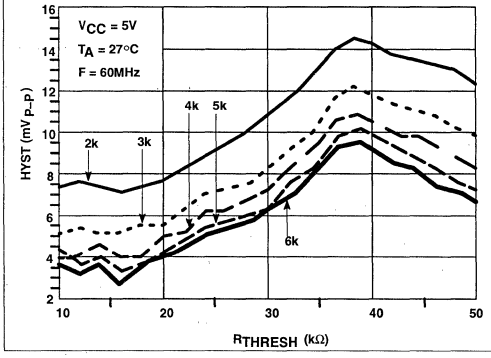
Threshold vs R_{THRESH} for Different Values of R_{HYST} (Driven Single Ended)



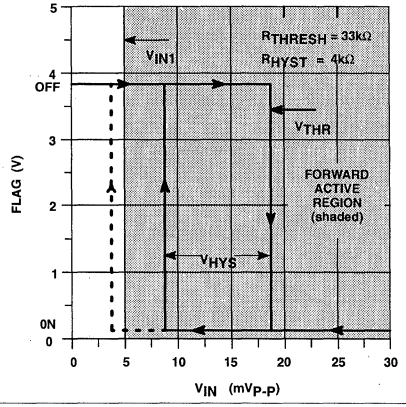
On/Off Voltage vs R_{THRESH} (Driven Single Ended)



Hysteresis vs R_{THRESH} for Different Values of R_{HYST} (Driven Single Ended)



Hysteresis and Forward Active Region



THEORY OF OPERATION AND APPLICATION

The NE5217 postamplifier is a highly integrated chip that provides up to 60dB of gain at 60MHz, to bring mV level signals up to TTL levels.

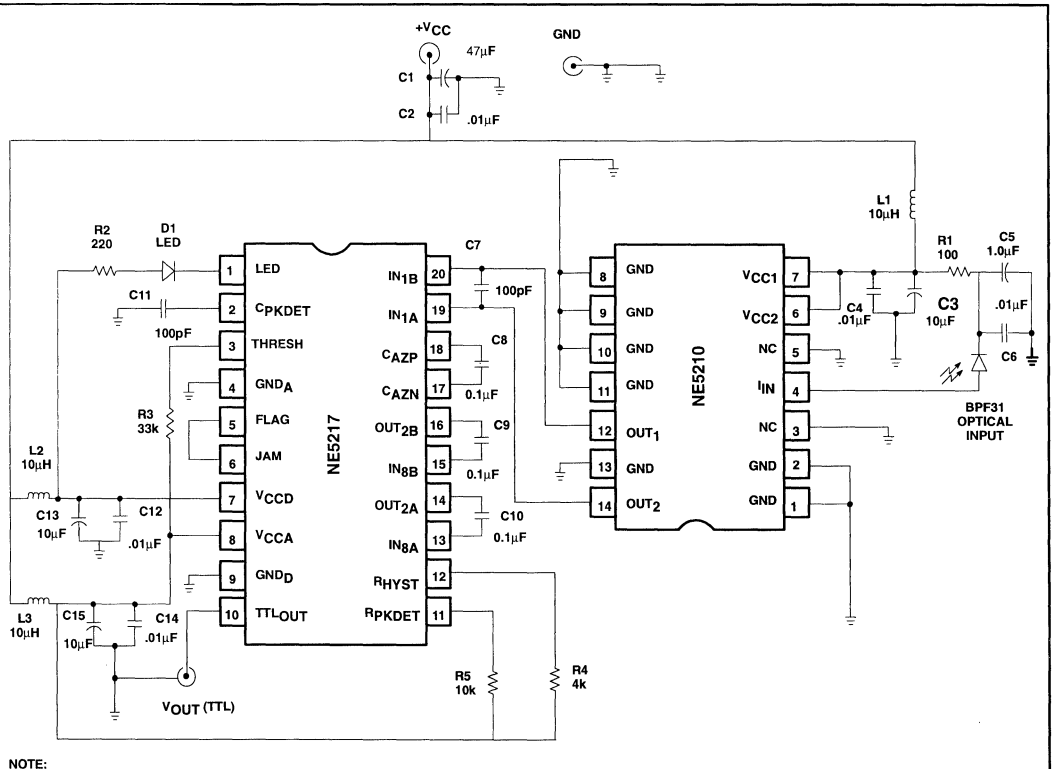
The NE5217 contains eight amplifier blocks (see Block Diagram). The main signal path is made up of a cascade of limiting stages: A1, A2 and A8. The A3-A4-A7 path performs a wideband full-wave rectification of the input signal with adjustable hysteresis and decay times. It outputs a TTL High on the "FLAG" output (Pin 5) when the input is below a user adjustable threshold. An on-chip LED driver turns the external LED to the On state when the input signal is above the threshold. In a typical application the "FLAG" output is tied back tot he "JAM" input; forcing the "JAM" input to TTL High will latch the TTL Data Out at the last logical state.

Threshold voltage and hysteresis voltage range are adjustable with resistors R_{THRESH} and R_{HYST}. The typical values given in the data sheet will result in performance shown in the graph "Hysteresis and Forward Active Region". A minority of parts may be sensitive enough that FLAG High (Off) occurs below the minimum functional input signal level, V_{IN1}. This condition is shown by the dotted line in the graph. Such parts may require adjustment of R_{THRESH} if it is important to guarantee that an output signal is present for the full hysteresis range. If this is not important, R_{THRESH} may be adjusted to give a FLAG Low for lower level input signals.

An auto-zero loop allows the NE5217 to be directly connected to a transimpedance amplifier such as the NE5210, NE5211, or NE5212A without coupling capacitors. This auto-zero loop cancels the transimpedance amplifier's DC offset, the NE5217 A1 offset, and the data-dependent offset in the PIN diode/transimpedance amplifier combination.

A typical application of the NE5217 postamplifier is depicted in Figure 2. The system uses the NE5211 transimpedance amplifier which has a 28k differential transimpedance gain and a -3dB bandwidth of 140MHz. this typical application is optimized for a 50Mb/s Non Return to Zero (NRZ) bit stream.

As the system's gain bandwidth product is very high, it is crucial to employ good RF design and printed circuit board layout techniques to prevent the system from becoming unstable.



NOTE:
THE NE5210/NE5217 combination can operate at data rates in excess of 100Mb/s NRZ

Figure 2. A 50Mb/s Fiber Optic Receiver

For more information on this application, please refer to Application Brief AB1432.

Low-power FDDI transimpedance amplifier SA5222

DESCRIPTION

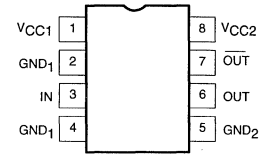
The NE/SA5222 is a low-power, wide-band, low noise transimpedance amplifier with differential outputs, optimized for signal recovery in FDDI fiber optic receivers. The part is also suited for many other RF and fiber optic applications as a general purpose gain block.

FEATURES

- Extremely low noise: $2.0pA/\sqrt{Hz}$
- Single 5V supply
- Low supply current: 9mA
- Large bandwidth: 165MHz
- Differential outputs
- Low output offset
- Low input/output impedances
- High power-supply-rejection ratio: 55dB
- Tight transresistance control
- High input overload: 115μA
- ESD protected

PIN DESCRIPTION

D Package



APPLICATIONS

- FDDI preamp
- Current-to-voltage converters
- Wide-band gain block
- Medical and scientific instrumentation
- Sensor preamplifiers
- Single-ended to differential conversion
- Low noise RF amplifiers
- RF signal processing

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) package	-40 to +85°C	SA5222D	0174C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
$V_{CC1,2}$	Power supply voltage	6	V
T_A	Ambient temperature range	-40 to +85	°C
T_J	Junction temperature range	-55 to +150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
P_D	Power dissipation T_A = 25°C (still air)[1]	0.78	W
I_{INMAX}	Maximum input current	5	mA

NOTE:

1. Maximum power dissipation is determined by the operating ambient temperature and the thermal resistance θ_{JA} = 158°C/W. Derate 6.2mW/°C above 25°C.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
$V_{CC1,2}$	Power supply voltage	4.5 to 5.5	V
T_A	Ambient temperature range: SA grade	-40 to +85	°C
T_J	Junction temperature range: SA grade	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

Typical data and Min and Max limits apply at $T_A = 25^{\circ}C$, and $V_{CC1} = V_{CC2} = +5V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SA5222			UNIT
			Min	Typ	Max	
V_{IN}	Input bias voltage		1.3	1.55	1.8	V
$V_{O\pm}$	Output bias voltage		2.9	3.2	3.5	V
V_{OS}	Output offset voltage			0	±100	mV
I_{CC}	Supply current		6	9	12	mA
I_{OMAX}	Output sink/source current		1.5	2		mA
I_{IN}	Input current (2% linearity)	Test circuit 5, Procedure 2	±60	±90		µA
I_{INMAX}	Maximum input current overload threshold	Test circuit 5, Procedure 4	±80	±115		µA
V_{OMAX}	Maximum differential output voltage swing	$R_L = \infty$, Test Circuit 5, Procedure 3		3.6		V_{P-P}

AC ELECTRICAL CHARACTERISTICS

Typical data and Min and Max limits apply at $T_A = 25^{\circ}C$ and $V_{CC1} = V_{CC2} = +5V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SA5222			UNIT
			Min	Typ	Max	
R_T	Transresistance (differential output)	DC tested, $R_L = \infty$, Test Circuit 5, Procedure 1	13.3	16.6	19.9	kΩ
R_O	Output resistance (differential output)	DC tested	30	60	90	Ω
R_T	Transresistance (single-ended output)	DC tested, $R_L = \infty$	6.65	8.3	9.95	kΩ
R_O	Output resistance (single-ended output)	DC tested	15	30	45	Ω
f_{3dB}	Bandwidth (-3dB)[1]	Test Circuit 1	110	140		MHz
R_{IN}	Input resistance			150		Ω
C_{IN}	Input capacitance[2]			1		pF
$\Delta R/\Delta V$	Transresistance power supply sensitivity	$V_{CC1} = V_{CC2} = 5 \pm 0.5V$		1.0		%/V
$\Delta R/\Delta T$	Transresistance ambient temperature sensitivity	$\Delta T_A = T_{A\,MAX} - T_{A\,MIN}$		0.07		%/°C
I_{IN}	RMS noise current spectral density (referred to input)	Test Circuit 2, f = 10MHz		2.0		$pA/\sqrt{Hz}$
I_T	Integrated RMS noise current over the bandwidth (referred to input) C_S = 0pF	Test circuit 2, Δf = 50MHz		15		nA
		Δf = 100MHz		25		
		Δf = 150MHz		36		
	C_S = 1pF	Δf = 50MHz		17		
		Δf = 100MHz		35		
		Δf = 150MHz		55		
PSRR	Power supply rejection ratio	DC Tested, $\Delta V_{CC} = \pm 0.5V$		–55		dB
PSRR	Power supply rejection ratio[3]	f = 1.0MHz, Test Circuit 3		–34		dB

AC ELECTRICAL CHARACTERISTICS (continued)

I_{INMAX}	Maximum input amplitude for output duty cycle of 50 ±5%[4]	Test circuit 4		±120		µA
t_r, t_f	Rise and fall times	10 – 90%		2.2		ns
t_D	Group delay	f = 10MHz		2.2		ns

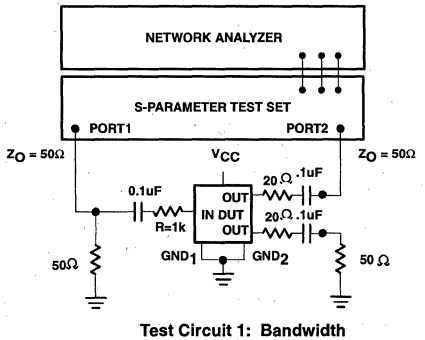
NOTES:

1. Bandwidth is tested into 50Ω load. Bandwidth into 1kΩ load is approximately 165MHz.

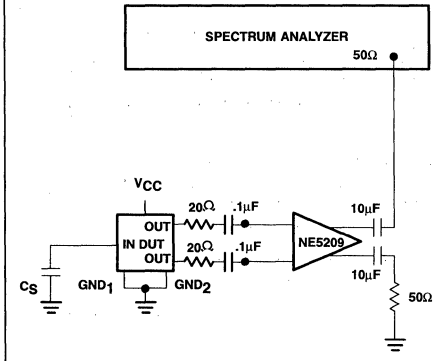
2. Does not include Miller-multiplied capacitance of input device.
3. PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use a RF filter in V_{CC} line.
4. Monitored in production via linearity and over load tests.

TEST CIRCUITS

SINGLE-ENDED	DIFFERENTIAL
$R_T = \frac{V_{OUT}}{V_{IN}} R = 2 \cdot S_{21} \cdot R$	$R_T = \frac{V_{OUT}}{V_{IN}} R = 4 \cdot S_{21} \cdot R$
$R_O = Z_O \left\| \frac{1 + S22}{1 - S22} \right\|$ -20	$R_O = 2Z_O \left\| \frac{1 + S22}{1 - S22} \right\|$ -40

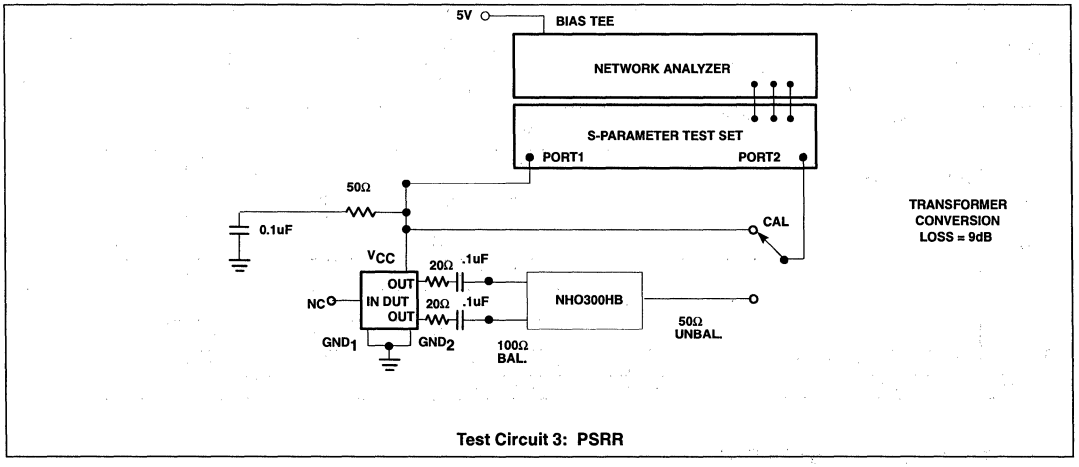


Test Circuit 1: Bandwidth



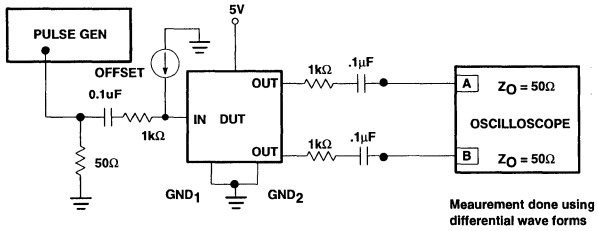
Test Circuit 2: Noise

TEST CIRCUITS (continued)



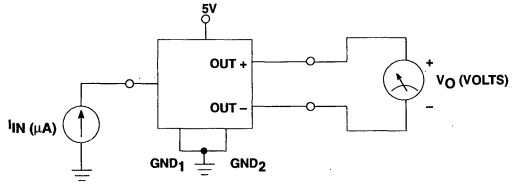
Test Circuit 3: PSRR

TEST CIRCUITS (continued)

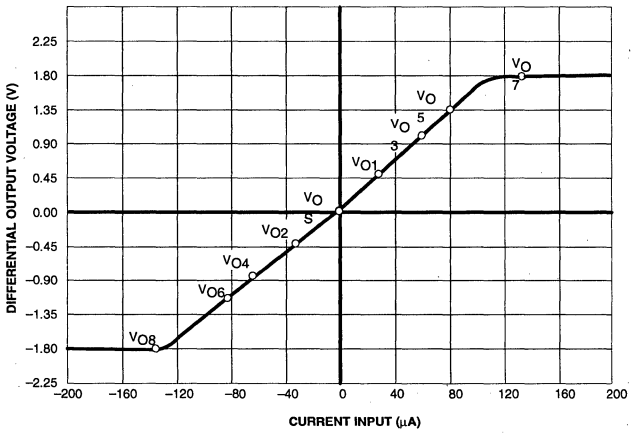


Test Circuit 4: Duty Cycle Distortion

TEST CIRCUITS (continued)



Typical V_O (Differential) vs I_{IN}



SA5222 TEST CONDITIONS

Procedure 1 R_T measured at 30µA
$R_T = (V_{O1} - V_{O2}) / (+30\mu A - (-30\mu A))$
Where: V_{O1} Measure at $I_{IN} = +30\mu A$
V_{O2} Measured at $I_{IN} = -30\mu A$

Procedure 2 Linearity = 1 - ABS((V_{OA} - V_{OB} / (V_{O3} - V_{O4}))
Where: V_{O3} Measured at $I_{IN} = +60\mu A$
V_{O4} Measured at $I_{IN} = -60\mu A$
$V_{OA} = R_T \times (+60\mu A) + V_{OS}$
$V_{OB} = R_T \times (-60\mu A) + V_{OS}$

Procedure 3 $V_{OMAX} = V_{O7} - V_{O8}$
Where: V_{O7} Measured at $I_{IN} = +130\mu A$
V_{O8} Measured at $I_{IN} = -130\mu A$

Procedure 4 I_{INMAX} Test Pass Conditions:
$V_{O7} - V_{O5} > 50mV$ and $V_{O6} - V_{O8} < 50mV$
Where: V_{O5} Measured at $I_{IN} = +80\mu A$
V_{O6} Measured at $I_{IN} = -80\mu A$
V_{O7} Measured at $I_{IN} = +130\mu A$
V_{OB} Measured at $I_{IN} = -130\mu A$

Test Circuit 5: DC Tests

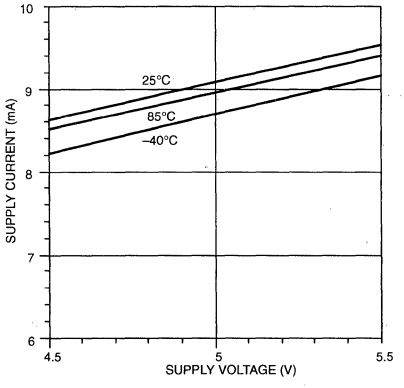


Figure 1. I_{CC} vs. V_{CC} and Temperature

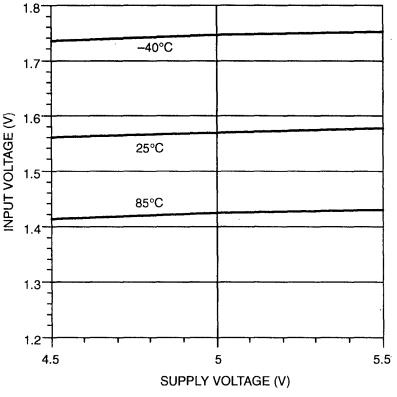


Figure 2. Input Voltage vs. V_{CC} and Temperature

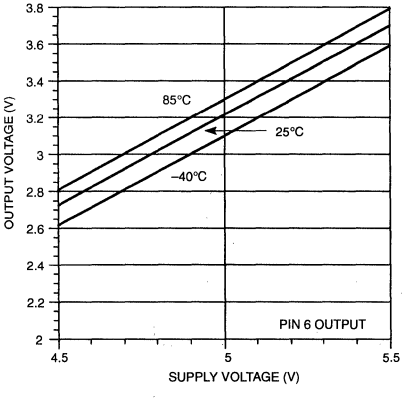


Figure 3. Output Voltage vs. V_{CC} and Temperature

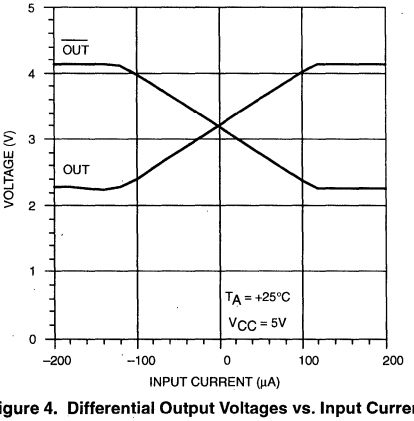


Figure 4. Differential Output Voltages vs. Input Current

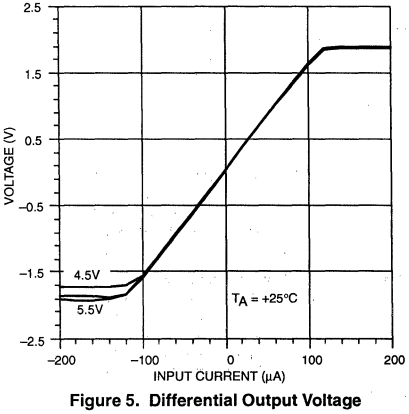


Figure 5. Differential Output Voltage vs Input Current and V_{CC}

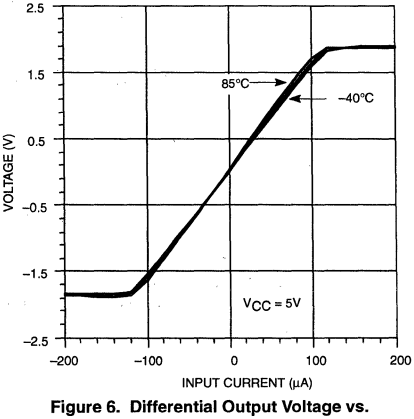


Figure 6. Differential Output Voltage vs. Input Current and Temperature

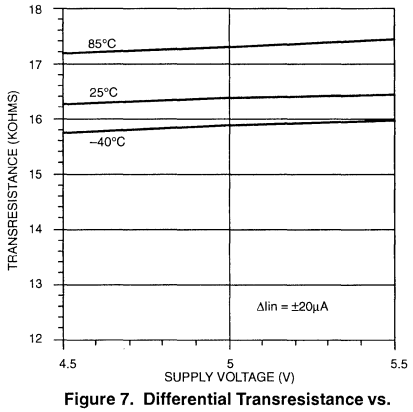


Figure 7. Differential Transresistance vs. V_{CC} and Temperature

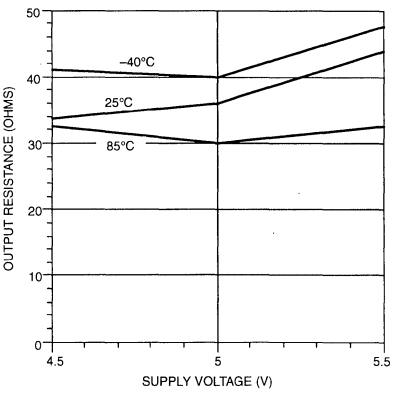


Figure 8. Output Resistance vs. V_{CC} and Temperature

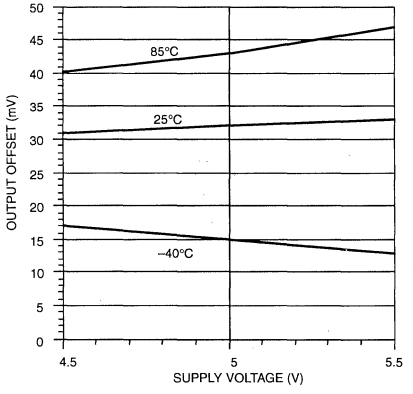


Figure 9. Output Offset Voltage vs. V_{CC} and Temperature

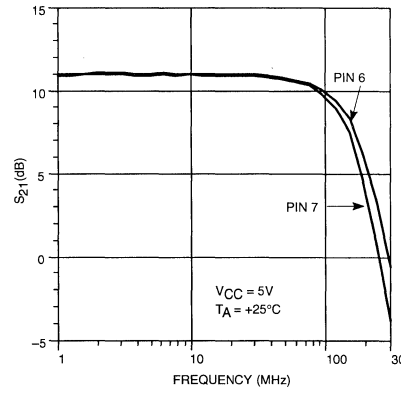


Figure 10. Insertion Gain vs. Frequency

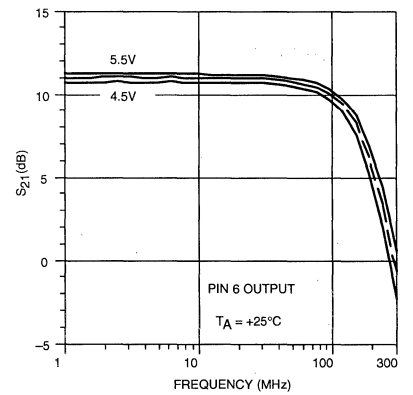


Figure 11. Insertion Gain vs. Frequency and V_{CC}

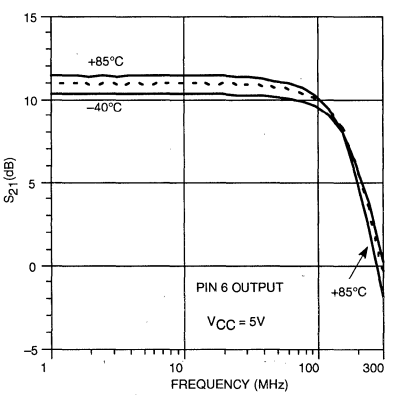


Figure 12. Insertion Gain vs. Frequency and Temperature

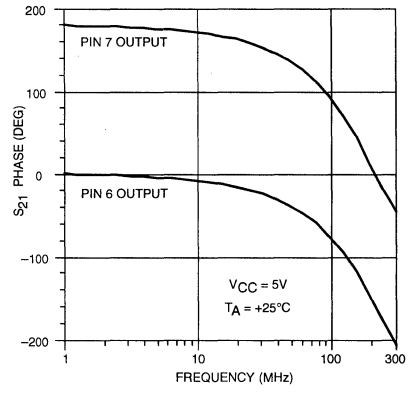


Figure 13. Phase vs. Frequency

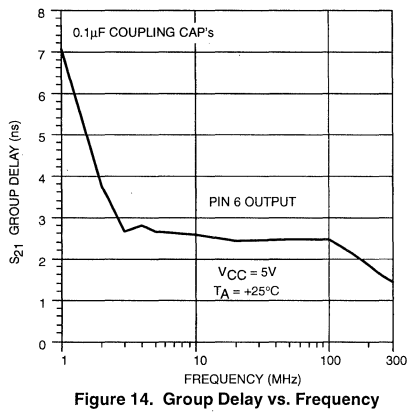


Figure 14. Group Delay vs. Frequency

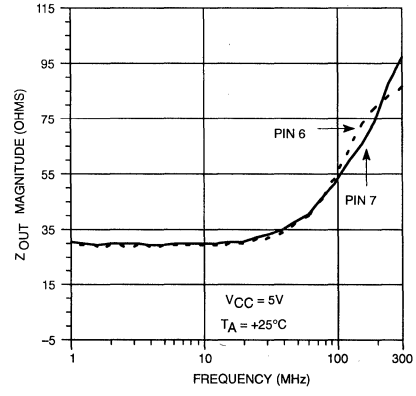


Figure 15. Output Impedance vs. Frequency

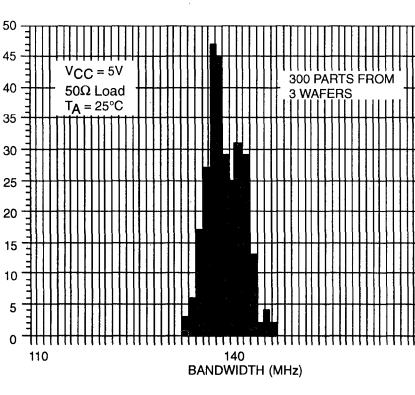


Figure 16. –3dB Bandwidth Distribution

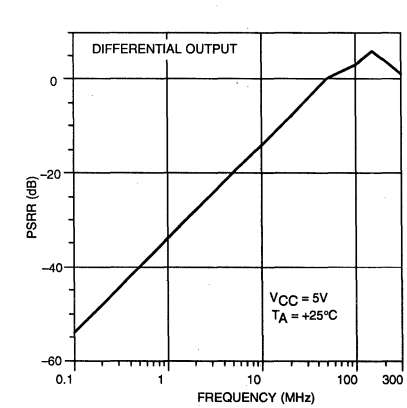


Figure 17. Power–Supply Rejection Ratio vs. Frequency

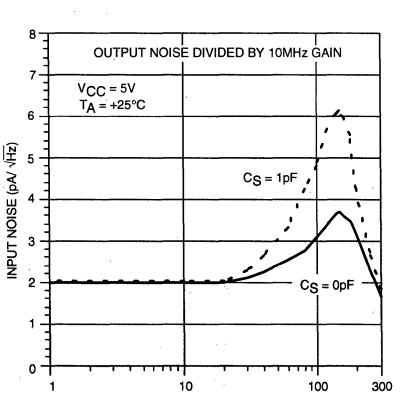


Figure 18. Input Noise Spectral Density vs. Frequency

Fiber optic receiver applications note — AN4003

I. A NEW FIBER OPTIC RECEIVER CHIP SET FOR 100Mb/s FDDI DATA LINKS

- SA5222 Transimpedance Amplifier.
- NE/SA5224 and NE/SA5225 Post Amplifiers

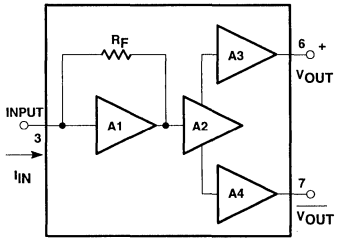


Figure 1. SA5222 Low Power Transimpedance Amplifier

The 140MHz Transimpedance Amplifier (Figure 1)

Designed specifically to meet the requirements of the ANSI Fiber Distributed Data Interface (FDDI) 100Mb/s LAN systems, the SA5222 is a new addition to Philips Semiconductors family of fiber optic devices. Table 1 shows a comparison of the features of this device in relation to the existing transimpedance amplifiers.

Particular attention has been paid to improving the power supply rejection ratio (PSRR). This reduces the chance of oscillation due to coupling onto the supply line. The PSRR specification, as noted in Table 1, is 57dB. In addition the supply current is reduced to 9mA, a particular advantage in remote, high density applications.

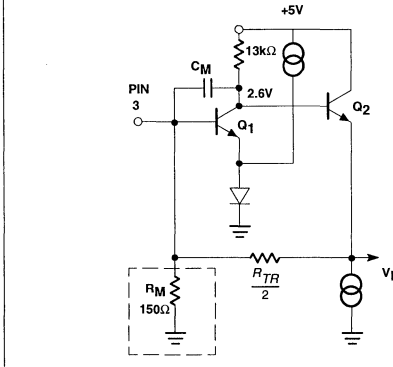


Figure 2. SA5222 Input Stage (Simplified)

Table 1.

	Differential Transresistance	Bandwidth	i_n	Input Max µA	I_{CC}	PSRR
SA5222	16.6kΩ	140MHz	1.8pA/√Hz	±115µA	9mA	57dB
NE5212	14kΩ	140MHz	2.5pA/√Hz	±120µA	26mA	33dB
NE5211	28kΩ	180MHz	1.8pA/√Hz	±60µA	24mA	32dB
NE5210	7kΩ	280MHz	3.5pA/√Hz	±240µA	26mA	36dB

Theory of Operation – SA5222

The SA5222 is an all-bipolar amplifier with a -3dB bandwidth of 140MHz. The device operates in the inverting mode with the first stage loop closed by a shunt feedback resistance (see Figure 2). The advantage in this topology is its inherent insensitivity to shunt capacitance at the input. The node at Pin 3 of the amplifier acts to sum the input current from the photo or PIN diode with the negative feedback from the shunt resistance. The input node is dominated by the Miller feedback capacitance from the collector-base junction of Q1 (C_M). This capacitance in conjunction with the Miller resistance ($R_M = R_{IN}$), acts to set the upper frequency bandwidth of the amplifier.

$$f_{-3dB} = \frac{1}{2 \cdot \pi \cdot R_{IN} \cdot C_{IN}}$$

The first stage Miller capacitance is approximately 7pF and the Miller resistance is equal to the rated input resistance of 150Ω.

The upper 3dB bandwidth is then

$$f_{-3dB} = \frac{1}{2 \cdot \pi \cdot 150 \cdot 7 \cdot 10^{-12}\ F} = 150MHz$$

which agrees with the device specifications.
The virtual capacitance now dominates the frequency response of the amplifier desensitizing it to small values of input shunt capacitance.

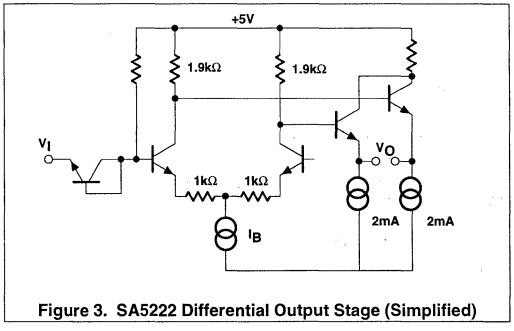


Figure 3. SA5222 Differential Output Stage (Simplified)

The major advantage of this configuration over a cascade amplifier with FET input is that the input frequency response limit is stabilized and the noise gain is not drastically affected by the external circuit capacitances.

For example, with the rated 1pF package capacitance plus 1pF of external capacitance combined with 150Ω, the input bandwidth is approximately 120MHz. This demonstrates the amplifier's intolerance to shunt capacitance. Adding external shunt

capacitance *will lower* the input stage bandwidth. This will also *increase* the noise gain, however. The shunt capacitance acts inversely with increasing frequency to increase the gain of the amplifier to internal noise currents.

The input stage is followed by a differential buffer driver which provides the necessary interface and level shifting for the output emitter followers (see Figure 3). The second stage converts the single-ended input signal to a differential signal raised to a common mode voltage of 3.2V. The amplifier has a source/sink output capability of 2mA. The second stage provides a gain of slightly over two. NPN current sources are bandgap referenced to provide highly stable biasing in the amplifier giving it an advantage in power supply rejection and linearity.

The SA5222 differential output resistance is typically 60Ω and is, therefore, capable of driving low impedance circuitry. However, the output voltage of the SA5222 is 3.2V which limits the external DC load resistance to ground to a value which does not draw more than the rated 2mA of sink current. It is typically necessary to include capacitive coupling between the SA5222 and the post amplifier in order to allow the threshold comparators to automatically detect the bit amplitude and provide proper level conversion independent of preamp DC offset.

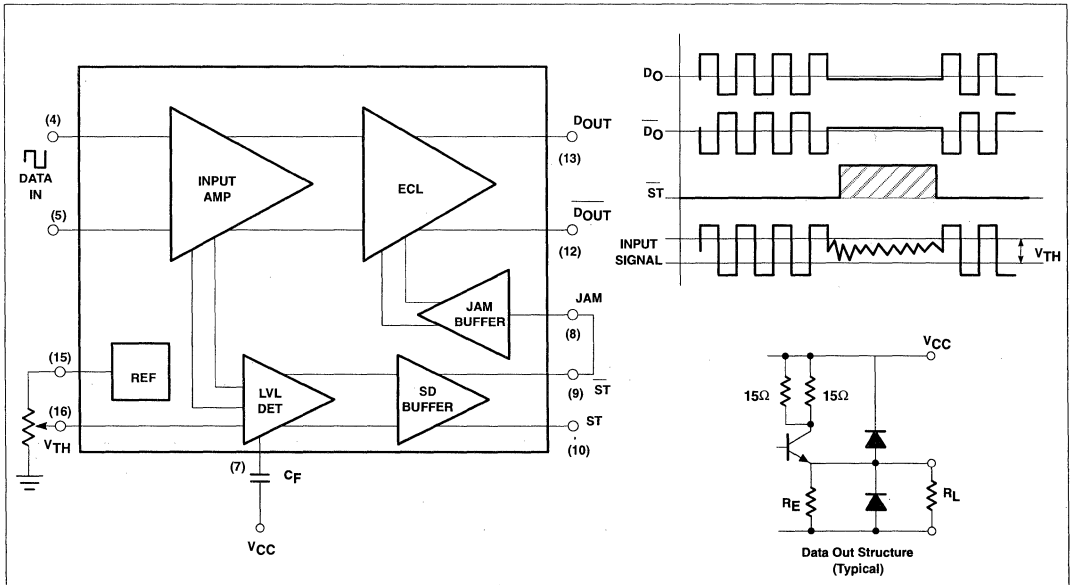


Figure 4. NE/SA5224 Postamplifier Output Disable Using Jam Functions

Input Sensitivity and Signal-to- Noise Ratio

Example of Optical Conversion gain.

Consider a 10μW optical signal incident upon a 0.45A/Watt responsivity PIN diode. This corresponds to –20dB optical relative to 1mW (-20dBmo*). The current generated at the input node of the SA5222 is 4.5μA. The resultant differential output voltage is

$$4.5\mu A \cdot 16.6k\Omega = 75mV_{P-P}$$

between Pins 6 and 7.

The dynamic signal-to-noise ratio at this level is calculated below using the rated 1.8pA/√Hz over a 150MHz bandwidth

$$20 \log \frac{(75 \cdot 10^{-3})\ V_{P-P}}{(1.8 \cdot 10^{-12})\ \sqrt{150 \cdot 10^{6}} \cdot 16.6K\Omega} = 47dB$$

Whereas, a 1μW (–30dBmo) input into a typical 0.3A/Watt responsivity photo diode or PIN will result in a theoretical signal-to-noise ratio of

$$20 \log \frac{5 \cdot 10^{-3}\ V_{P-P}}{(22 \cdot 10^{-9} A_{RMS})\ 16.6k\Omega V_{RMS}} = 23dB$$

This does not include the optical noise of the fiber or the receiver diode. In this case the SA5222 output voltage due to the 1μW optical input signal is $5mV_{P-P}$. (NOTE: A 12:1 ratio or 21.6dB corresponds to a BER of 10^{-9}.)

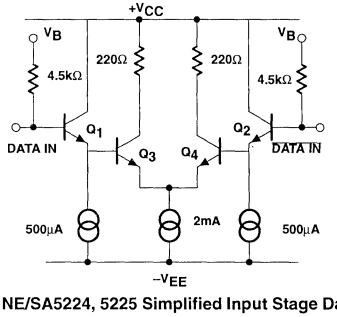
*NOTE: dBmo = dBm optical relative to 1mW.

Postamplifier Selection (NE/SA5224 and 5225)

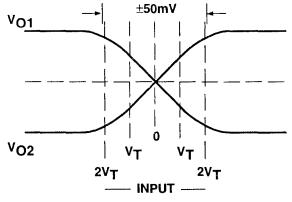
In selecting the correct signal interface to meet user data communications system specifications, two different devices are available to the designer. For the Fiber Data Distributed Interface (FDDI), the NE/SA5224 is recommended. This device provides 100k ECL compatibility for the differential data output, Status output and Jam input.

For industrial fiber communications applications, the NE/SA5225 is recommended. It provides 10k ECL compatibility. With the

exception of different hysteresis specifications, the two devices are fully pin-for-pin compatible.



a. NE/SA5224, 5225 Simplified Input Stage Data



b. NE/SA5224 Input Stage Transfer Functions

Figure 5.

Theory of Operation*

Referring to the Operational Block Diagram in Figure 4, the device consists of a main signal path that is fully differential from input to output. The input amplifier consists of a differential pair limited to an I_{CC} of 2mA (see Figure 5a). The amplifier is a limiting type with gain reduction above 2 V_t, or about 100mV_{P-P}. The input common mode voltage is approximately 2.9V with a V_{CC} of 5V. The input resistance of the device is typically 4.5kΩ. This, then, allows the calculation of the minimum coupling capacitor for the lowest data frequency component. (See Figure 5b.)

The NE/SA5224 Postamplifier

The NE/SA5224 is designed to operate within the FDDI specification data rate of 125Mb/s using the 4B/5B format. At 100Mb/s this requires the data clock to operate at 62.5MHz and presumes the use of an NRZ format. The NE/SA5224 is rated to operate over a frequency range of 1kHz to 120MHz, but will operate higher in frequency with some loss of sensitivity.

The first stage input capacitance is on the order of 1.5pF including the ESD diode junction capacitance plus the input device and package contributions.

Following the first stage are the intermediate gain stages from which a sample of the amplified signal is fed to the level detector.

(*Unless stated, also applies to NE/SA5225.)

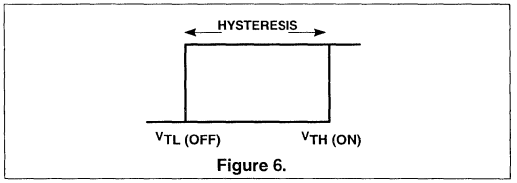


Figure 6.

Level Detector

This section provides the programmable threshold function of the device. Adjustment of the voltage on Pin 16 determines the point at which the input signal decision level occurs. The threshold levels are rated for the single-ended voltage trip level of 2 to 12mV_{P-P} which corresponds to twice this value or 4 to 24mV_{P-P} differentially (see Table 2).

Threshold sensing may be combined with the output signal function through use of the data out Jam functions). This allows you to force the output to a fixed state when the input falls below the predetermined level as programmed on Pin 16. This function is provided by connecting Pins 8 and 9 together.

Table 2.

V_{SET}	V_{TL}	V_{TH}	$V_{P-P(avg)}$	R_1	R_2
0.5V	3.6mV	6.4mV	5.0mV	4050Ω	950Ω
1.0V	7.2mV	12.8mV	10.0mV	3110Ω	1890Ω
1.5V	10.8mV	19.2mV	15.0mV	2160Ω	2840Ω
2.0V	14.4mV	26.0mV	20.0mV	1210Ω	37900Ω

The signal level detector controls the status detector, which has complimentary outputs at Pins 9 and 10. Pin 9 is forced to a high state whenever the input to the NE/SA5224 falls below the user determined voltage threshold as set on Pin 16 (V_{SET}) (see Figure 4). In the Jam state, the ECL data outputs are forced into predetermined states, D_{OUT} = low and $\overline{D_{OUT}}$ = high. The complimentary ST output at Pin 10 may be used as a system status enable providing an ECL high when the input signal level is above the threshold level.

The status circuit operates on the basis of a full wave rectifier averaging detector with a nominal response time of 1µs. Additional filtering may be added at Pin 7, (C_F pin) which has characteristic internal resistance of 24kΩ. This allows the user to select the time constant of the low-pass filter to meet a specific application by adding external capacitance at this pin. Note that the capacitor is returned to the plus V_{CC} line.

The hysteresis characteristic of the NE/SA5224 is fixed internally between 4 and 6dB. The plot in Figure 6 shows how this relates to the threshold levels discussed above. The typical value in dB is determined by taking 20 times the log of the ratio of V_{TH} (on) to V_{TL} (off) and for the NE/SA5224 this equals 5dB. The NE/SA5225, however, has a typical hysteresis value of 3dB with a tested range of 2 to 4dB.

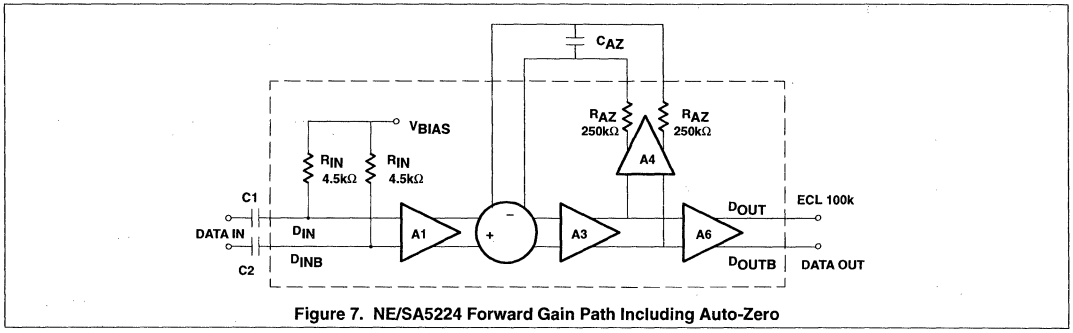


Figure 7. NE/SA5224 Forward Gain Path Including Auto-Zero

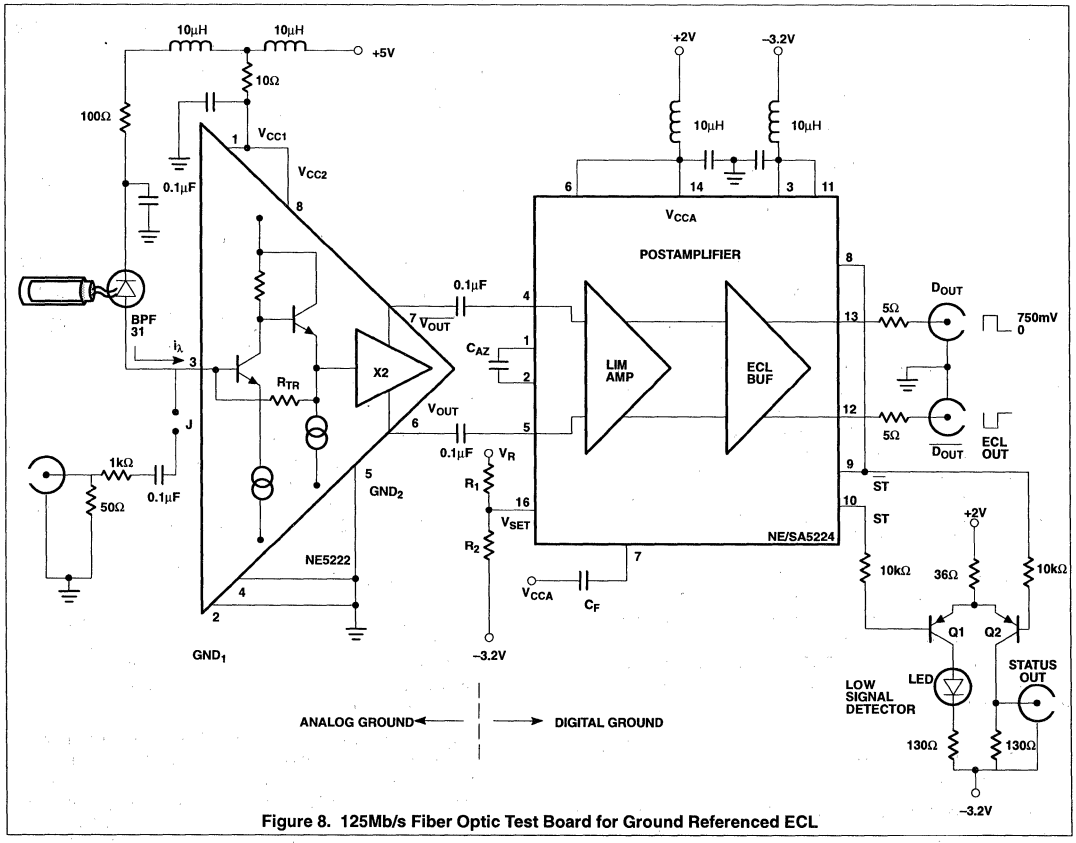


Figure 8. 125Mb/s Fiber Optic Test Board for Ground Referenced ECL

The Auto-Zero Loop

The auto-zero circuit provides closed loop feedback inside the NE/SA5224 which cancels the offset voltage of the forward signal path (Figure 7).

Essentially, the auto-zero circuit acts to cancel bias errors at the comparator due to component offsets and the data's average DC bias. The circuit is capable of cancelling the offset effect of long strings of zeros in transmission preventing a drift to a false output logic level.

The C_{AZ} capacitor is determined according to the relationship

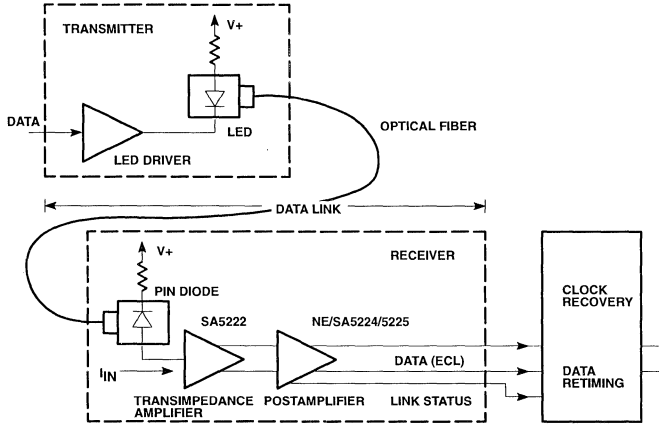


Figure 9. Fiber Optic-based Point-to-Point Communication Link

$$f_{-3dB} = \frac{150}{2\pi \cdot R_{AZ} \cdot C_{AZ}}$$

where R_{AZ} is specified by the data sheet.

For example if a 0.1uF capacitor is used for C_{AZ}, and R_{AZ} = 250kΩ.

$$f_{-3dB} = \frac{150}{2\pi \cdot 250x10^{3}\Omega \cdot 1x10^{-7}farad} = 1kHz$$

The lowest data frequency component must be above the –3dB frequency by an order of magnitude in order to reliably be reproduced at the ECL output. Lower frequencies will be filtered out by the AZ loop. The customer is referred to AN1443 for a more in-depth discussion of data rate response time versus the auto-zero function.

Setting The Threshold Level

A user programmable signal level detector is provided in both the NE/SA5224 and 5225. This circuit allows you to inhibit input signals which are below the predefined level as desired to provide a high quality output ECL signal, free of baseband noise. Setting the threshold is simply a matter of choosing a resistor divider ratio, R_1:R_2 as shown in Table 2 above, which connects from V_{REF}, Pin 15 to V_{SET}, Pin 16 (see Figure 4).

This provides the level detector with a threshold reference voltage. A scaled, rectified and filtered copy of the input signal is then compared to this threshold voltage. The programmable range is 4–24mV_{P-P} at the input and is a function of V_{SET}/100, a value which represents the average of V_{THIGH} and V_{TLOW}.

The actual threshold levels are:

$$V_{Tlow} = \frac{V_{SET}}{139} \quad \text{where } R_1 + R_2 = 5k\Omega \text{ is constant}$$

$$V_{Thigh} = \frac{V_{SET}}{78}$$

For example for V_{SET} = 1.2V, V_{TL} = 8.6mV and V_{TH} = 15.4mV. Table 2 shows various combinations of R_1 and R_2 with corresponding values of V_{SET} and threshold voltages.

$V_{HYST} = V_{TH} - V_{TL}$

Threshold levels as low as 4mV_{P-P} can be reliably set up for signal detection at the NE/SA5224,25 input. For sufficiently high signal levels the threshold may be maintained at an elevated clipping plateau allowing good rejection of incoming baseband noise.

(NOTE: 4mV_{P-P} corresponds to ≅ –33dBmo for an input PIN diode conversion efficiency of 0.45A/W.)

II. A TYPICAL RECEIVER TEST BOARD WITH ECL OUTPUT

The circuit shown in Figure 8 represents a simple printed circuit receiver capable of 100MB/s data processing from fiber.

The input photo optic device is a Philips BPF31 PIN diode optimized for a wavelength of 850nm.

The various waveforms (Figures 11–18) show signal levels produced within the receiver, for different optical power and data rates.

Supply voltages have been set for 5V on the SA5222 and +2V; –3.2V on the SA5224. This allows grounded 50Ω loads to be used at the output of the receiver.

The differential output of the transimpedance preamplifier is AC coupled to the NE5224 postamplifier to prevent any DC bias offset in the preamp from affecting the threshold accuracy of the output stage.

The coupling capacitors are made sufficiently large (0.1μF) in order to pass the lowest frequency data component.

The threshold voltage is set to 1.0V by R_1 and R_2 at Pin 16 of the NE5224 postamplifier. As noted in Table 2 this sets the threshold level, Vth, at $12.8mV_{P-P}$.

This corresponds to an input current on Pin 3 of the SA5222 of

$$I_{IN} = \frac{12.8mV}{16.6 \times 10^3\Omega} = 0.75\mu A$$

or $$P_{OPT} = \frac{0.75 \cdot 10^{-6}A}{0.45A/W} = 1.7\mu W$$

or –28dBmo, minimum.

ClAZl is 0.1µF for a low frequency data limit of 1KHz.

The status detector allows visual output to determine when the input signal level is above the receiver threshold described above. The light is on when signal level is below threshold. (Figure 8).

The Optical Receiver Board Construction (Figure 19)

Supply decoupling is obtained by splitting up the various parts of the receiver with 10µH chokes combined with low inductance chip capacitors placed in close proximity to the IC supply pin and grounded to wide ground plane copper areas.

Observe that the top and bottom of the printed circuit board is covered with copper ground plane within which the circuit traces are embedded. In addition, the bottom and top planes are tied together with connecting pins (soldered carefully) and placed at numerous points around the board. In particular this must be done where critical ground returns such as ground 1 and 2 of the SA5222 are brought out of the SMD device. A good rule is to place top to bottom ground plane pins every half inch in critical areas.

The supply is isolated between the input preamplifier, SA5222 and the post amplifier, SA5224. Ground traces are also separated into input stage (analog) and output stage (digital) grounds. This technique provides a more stable circuit, in addition to allowing ground referenced ECL signal into 50Ω loads at the output.

Noise Immunity

Level detection is set to automatically block reception when input signals fall below the threshold.

If left disconnected the JAM function is inactive. The NE/SA5224 (100K ECL output) and the NE/SA5225 (10K ECL output) easily provide sufficient signal detection and level translation accuracy for 100MB/s signal reproduction.

The signal-to-noise ratio is primarily determined by the receiver input stage so that equivalent input noise versus input signal current and signal bandwidth sets the limits on the signal-to-noise ratio of the combined receiver.

The noise immunity of the receiver proper, including the PC board, is determined by how well the layout is done. Ground plane construction of the signal preamplifier and post amplifier (with regard to RF technique) is required. No high level signal traces should be returned near the input sections in order to prevent feedback oscillation. The overall gain of preamplifier and post amplifier is in excess of 100dB with very wide bandwidth. This makes physical as well as electrical layout critical but reasonable once the rules are understood. Good bypassing of the V_{CC} lines, a low inductance ground plane and high quality passive components are required.

Note that 1" of copper trace 1/16th" wide is equivalent to 15nH of inductance. Wide traces on all V_{CC} and ground bus connections are mandatory. The same applies to the PIN diode signal traces at the input stage.

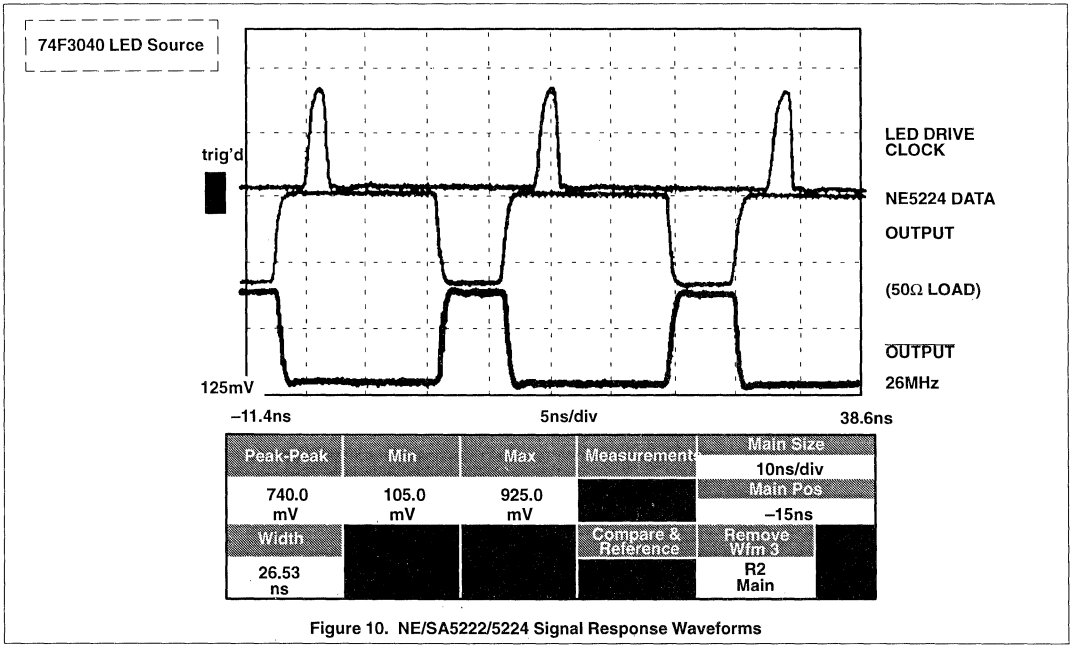


Figure 10. NE/SA5222/5224 Signal Response Waveforms

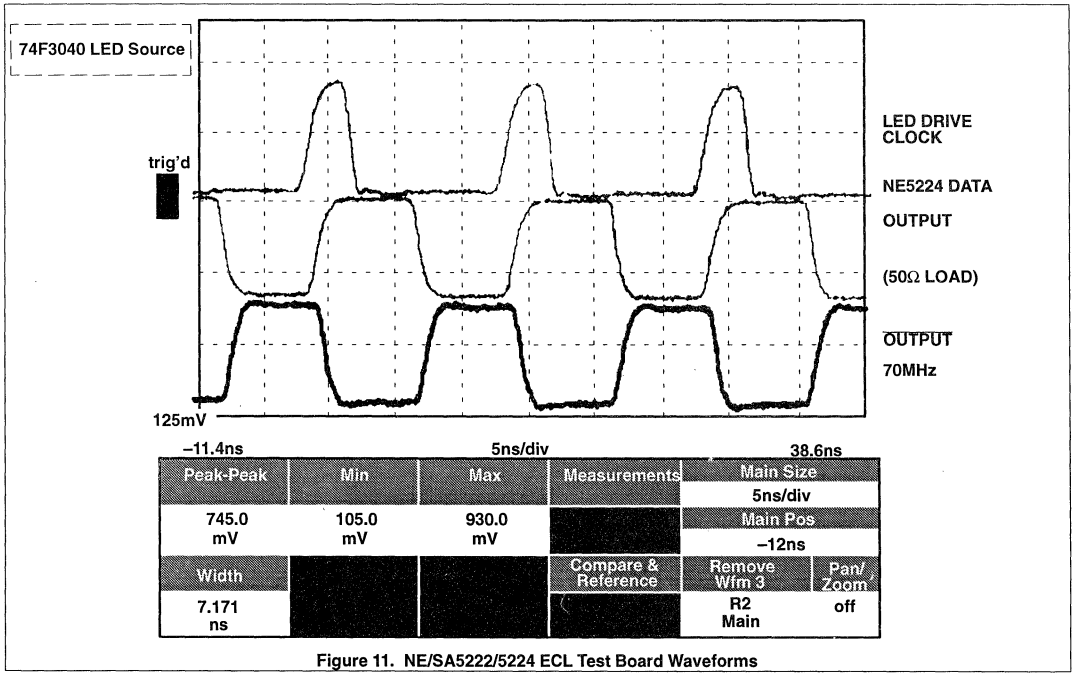


Figure 11. NE/SA5222/5224 ECL Test Board Waveforms

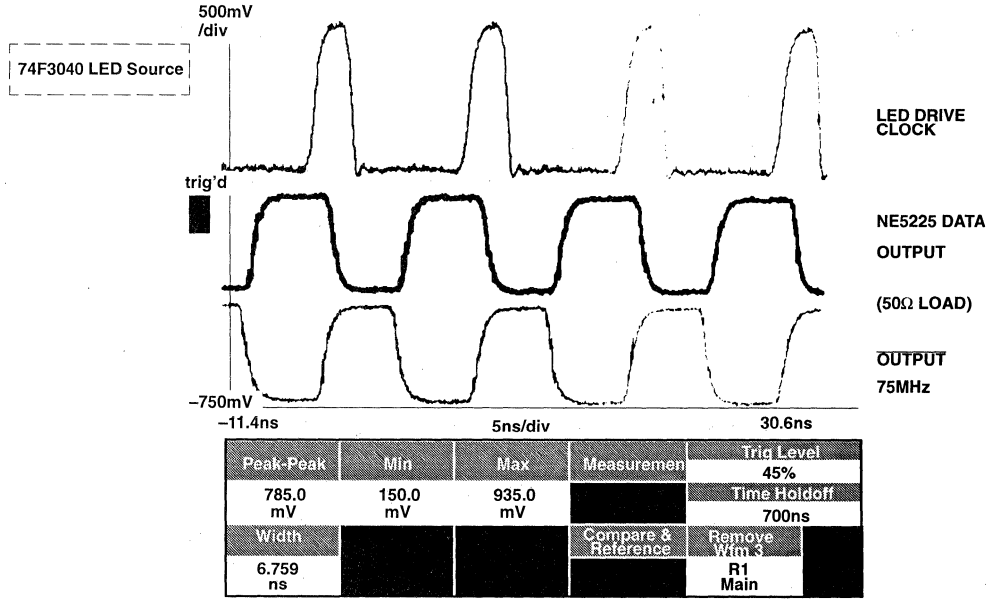


Figure 12. NE/SA5225 Signal Response Waveforms

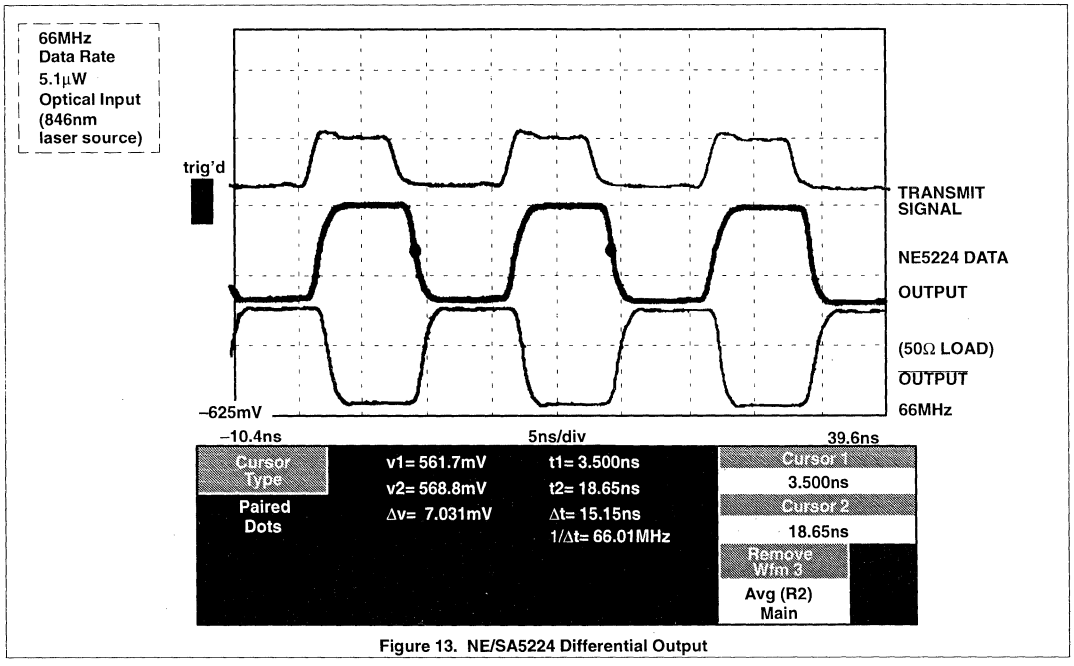


Figure 13. NE/SA5224 Differential Output

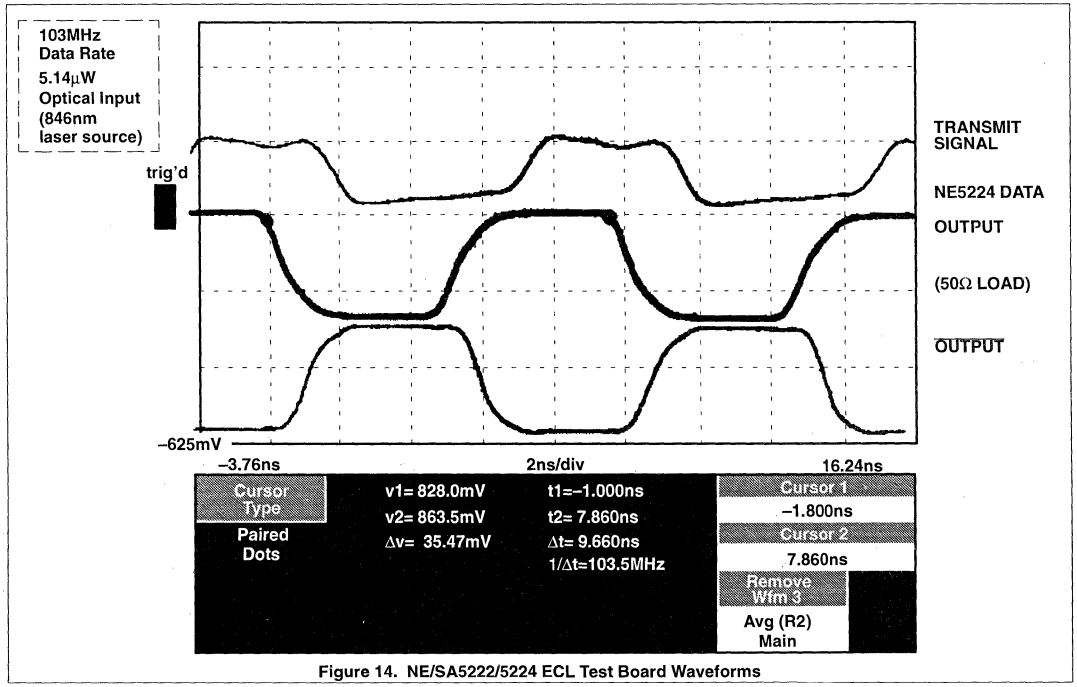


Figure 14. NE/SA5222/5224 ECL Test Board Waveforms

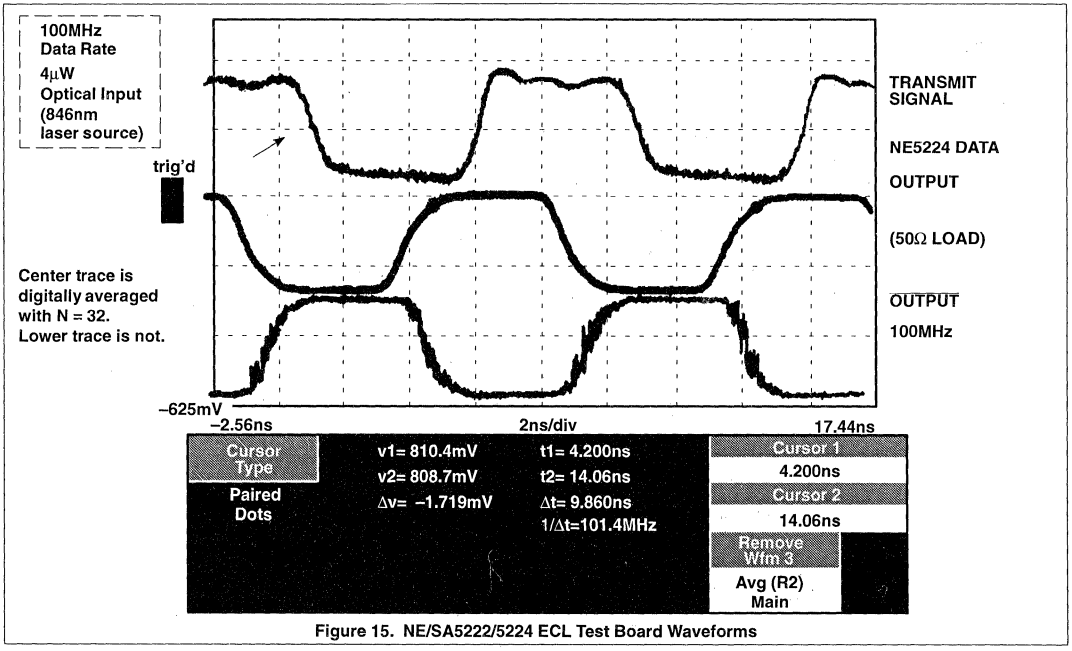


Figure 15. NE/SA5222/5224 ECL Test Board Waveforms

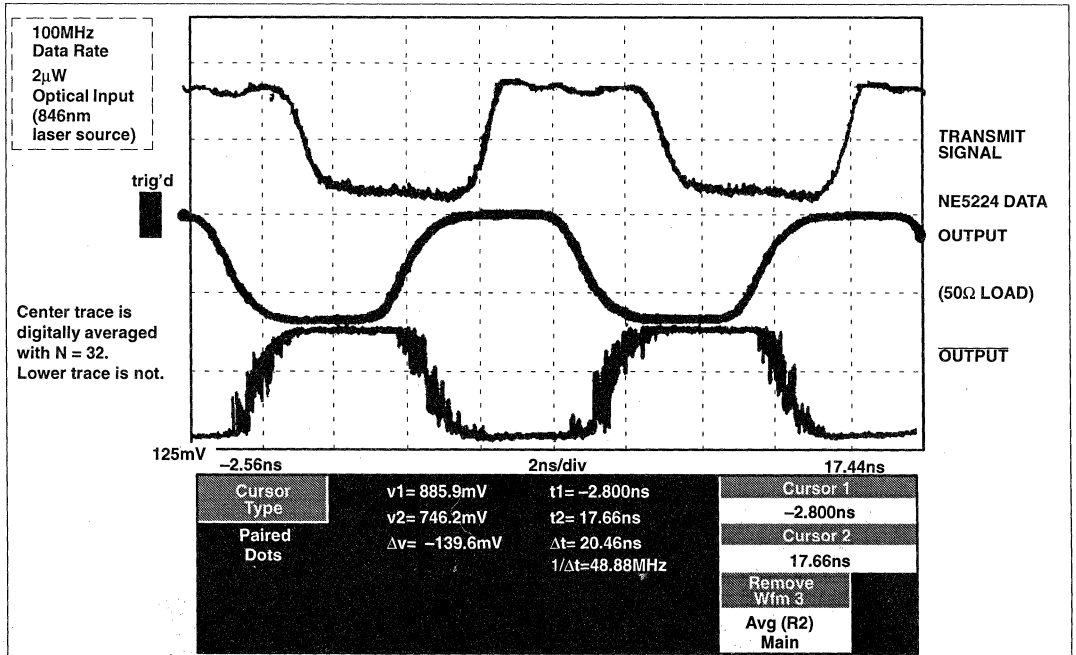


Figure 16. NE/SA5222/5224 ECL Test Board Waveforms

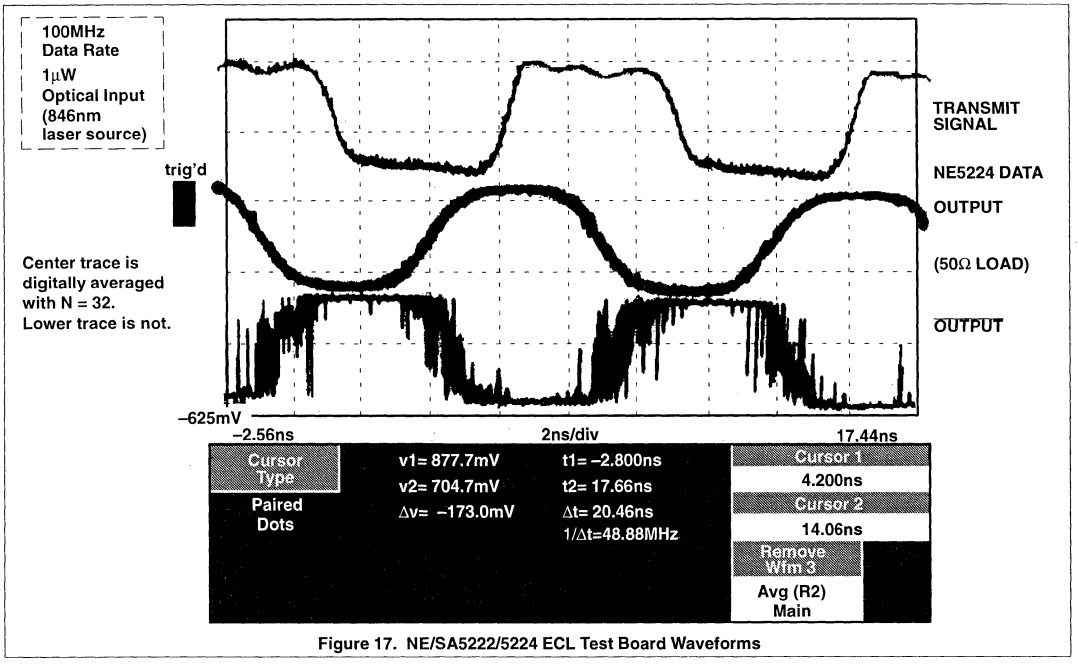


Figure 17. NE/SA5222/5224 ECL Test Board Waveforms

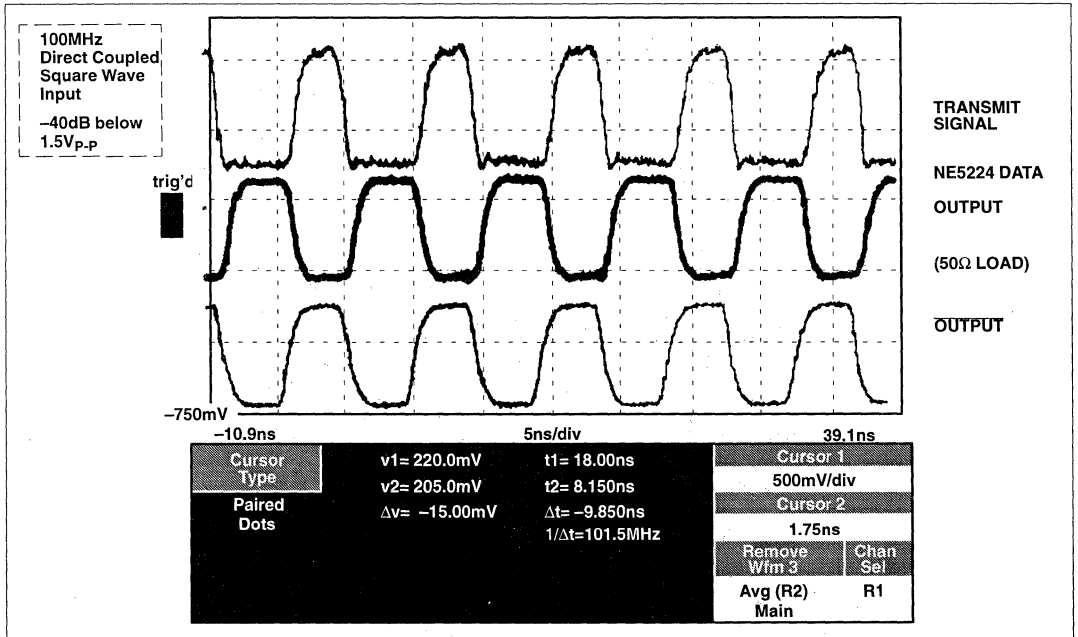


Figure 18. NE/SA5222/5224 ECL Test Board Waveforms

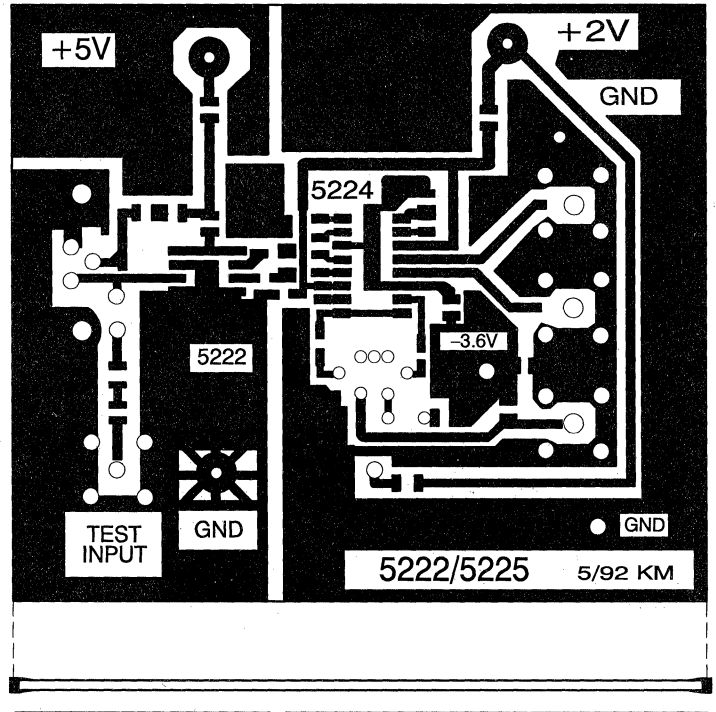


Figure 19. PC Board Layout

Wide-dynamic-range AGC — SA5223

DESCRIPTION

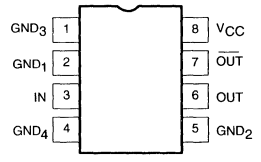
The SA5223 is a wide-band, low-noise transimpedance amplifier with differential outputs, incorporating AGC and optimized for signal recovery in wide-dynamic-range fiber optic receivers, such as SONET. The part is also suited for many other RF and fiber optic applications as a general purpose gain block.

FEATURES

- Extremely low noise: $1.0pA/\sqrt{Hz}$
- Single 5V supply
- Low supply current: 22mA
- Large bandwidth: 165MHz
- Differential outputs
- Low output offset
- Low input/output impedances
- High power-supply-rejection ratio: 55dB
- Tight transresistance control
- High input overload: 4mA
- ESD protected

PIN DESCRIPTION

D Package



APPLICATIONS

- SONET preamp
- Current-to-voltage converters
- Wide-band gain block
- Medical and scientific instrumentation
- Sensor preamplifiers
- Single-ended to differential conversion
- Low noise RF amplifiers
- RF signal processing

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline	-40 to +85°C	SA5223D	0174C

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Power supply voltage	6	V
T_A	Ambient temperature range	-40 to +85	°C
T_J	Junction temperature range	-55 to +150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
P_D	Power dissipation T_A = 25°C (still air)[1]	0.78	W
I_{INMAX}	Maximum input current	5	mA

NOTE:

1. Maximum power dissipation is determined by the operating ambient temperature and the thermal resistance θ_{JA} = 158°C/W. Derate 6.2mW/°C above 25°C.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Power supply voltage	4.3 to 5.5	V
T_A	Ambient temperature range: SA grade	-40 to +85	°C
T_J	Junction temperature range: SA grade	-40 to +105	°C

DC ELECTRICAL CHARACTERISTICS

Typical data and Min and Max limits apply at $T_A = 25°C$, and $V_{CC} = +5V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SA5223			UNIT
			Min	Typ	Max	
V_{IN}	Input bias voltage		1.3	1.55	1.8	V
$V_{O\pm}$	Output bias voltage		2.9	3.2	3.5	V
V_{OS}	Output offset voltage			0	±100	mV
I_{CC}	Supply current		15	22	29	mA
I_{OMAX}	Output sink/source current		1.5	2		mA
V_{OMAX}	Maximum differential output voltage swing			3.6		V_{P-P}

AC ELECTRICAL CHARACTERISTICS

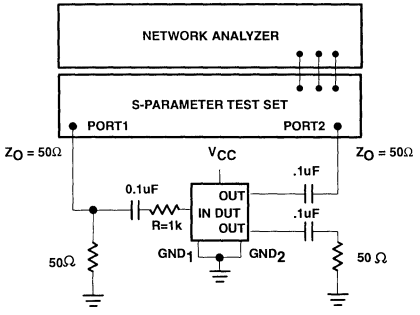
Typical data and Min and Max limits apply at $T_A = 25°C$ and $V_{CC} = +5V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SA5223			UNIT
			Min	Typ	Max	
R_T	Transresistance (differential output)	DC tested, $R_L = \infty$		100		kΩ
R_O	Output resistance (differential output)	DC tested		100		Ω
R_T	Transresistance (single-ended output)	DC tested, $R_L = \infty$		50		kΩ
R_O	Output resistance (single-ended output)	DC tested		50		Ω
f_{3dB}	Bandwidth (-3dB)[1]	Test Circuit 1	110	140		MHz
R_{IN}	Input resistance			250		Ω
C_{IN}	Input capacitance[2]			1		pF
$\Delta R/\Delta V$	Transresistance power supply sensitivity	$V_{CC1} = V_{CC2} = 5 \pm 0.5V$		3		%/V
$\Delta R/\Delta T$	Transresistance ambient temperature sensitivity	$\Delta T_A = T_{A\,MAX} - T_{A\,MIN}$		0.09		%/°C
I_{IN}	RMS noise current spectral density (referred to input)	Test Circuit 2, f = 10MHz		1.0		$pA/\sqrt{Hz}$
I_T	Integrated RMS noise current over the bandwidth (referred to input) $C_S = 0.1pF$	Test circuit 2, $\Delta f = 50MHz$		7		nA
		$\Delta f = 100MHz$		12		
		$\Delta f = 150MHz$		16		
	$C_S = 0.4pF$	$\Delta f = 50MHz$		8		
		$\Delta f = 100MHz$		13		
		$\Delta f = 150MHz$		18		
PSRR	Power supply rejection ratio	DC Tested, $\Delta V_{CC} = \pm 0.5V$		–55		dB
PSRR	Power supply rejection ratio[3]	f = 1.0MHz, Test Circuit 3		–20		dB
V_{OLMAX}	Maximum differential output AC voltage	I_i = 0–2mA peak AC		70		mV
$\frac{dR_T}{dt}$	AGC loop time constant parameter	Gain droop after signal interruption with AGC on		1		dB/ms
I_{INMAX}	Maximum input amplitude for output duty cycle of 50 ±5%[4]	Test circuit 4		+4		mA
t_r, t_f	Rise and fall times	10 – 90%		2.2		ns
t_D	Group delay	f = 10MHz		2.2		ns

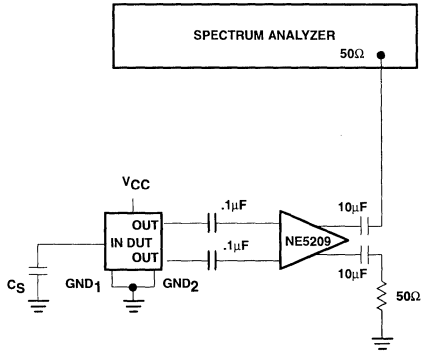
NOTES:
1. Bandwidth is tested into 50Ω load. Bandwidth into 1kΩ load is approximately 165MHz.
2. Does not include Miller-multiplied capacitance of input device.
3. PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use a RF filter in V_{CC} line.
4. Monitored in production via linearity and over load tests.

TEST CIRCUITS

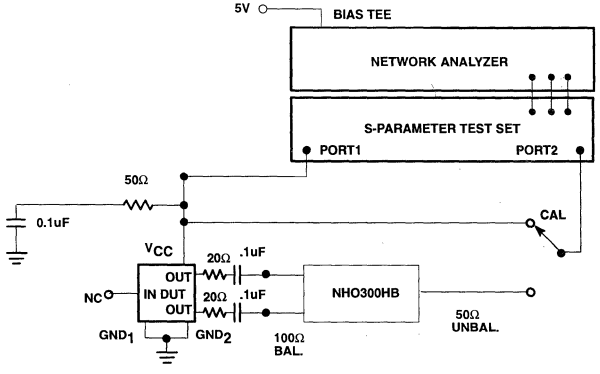
SINGLE-ENDED	DIFFERENTIAL
$R_T = \frac{V_{OUT}}{V_{IN}} R = 2 \cdot S_{21} \cdot R$	$R_T = \frac{V_{OUT}}{V_{IN}} R = 4 \cdot S_{21} \cdot R$
$R_O = Z_O \left\lvert \frac{1 + S22}{1 - S22} \right\rvert$	$R_O = 2Z_O \left\lvert \frac{1 + S22}{1 - S22} \right\rvert$



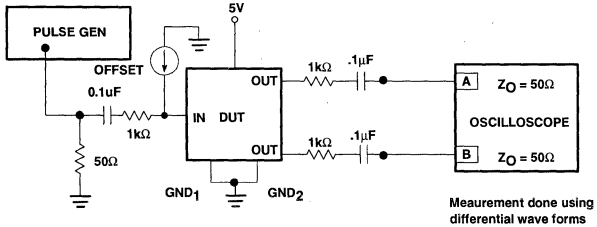
Test Circuit 1: Bandwidth



Test Circuit 2: Noise



Test Circuit 3: PSRR



Test Circuit 4: Duty Cycle Distortion

FDDI fiber optic postamplifier — NE/SA5224

DESCRIPTION

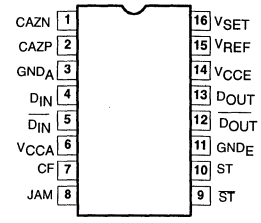
The NE/SA5224 is a high-gain limiting amplifier that is designed to process signals from fiber optic preamplifiers. Capable of operating at 125Mb/s, the chip is FDDI compatible and has input signal level-detection with a user-adjustable threshold. The DATA and LEVEL-DETECT outputs are differential for optimum noise margin and ease of use. Also available is the NE/SA5225 which is an ECL 10K version of the NE/SA5224.

FEATURES

- Wideband operation: 1.0kHz to 120MHz typical
- Operation with single +5V or –5.2V supply
- Differential 100k ECL outputs
- Programmable input signal level-detection
- Fully differential for excellent PSRR to 1GHz

PIN DESCRIPTION

D Package



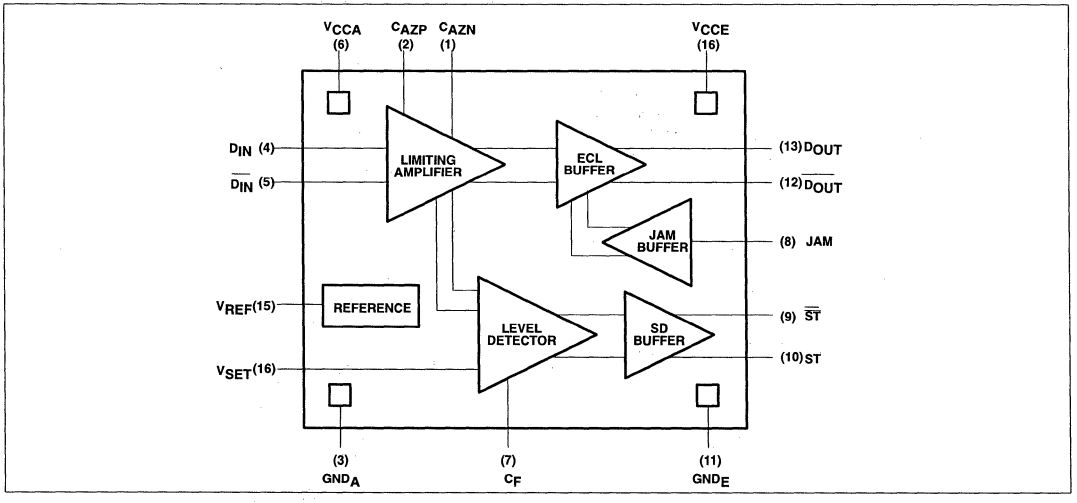
APPLICATIONS

- FDDI
- Data communication in noisy industrial environments
- LANs

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5224D	0005D
16-Pin Plastic Small Outline (SO) package	–40 to +85°C	SA5224D	0005D

BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NO.	NAME	FUNCTION
1	C_{AZN}	Auto-zero capacitor pin. Connecting a capacitor between this pin and C_{AZP} will cancel the offset voltage of the limiting amplifier.
2	C_{AZP}	Auto-zero capacitor pin. Connecting a capacitor between this pin and C_{AZN} will cancel the offset voltage of the limiting amplifier.
3	GND_A	Analog GND pin. Connect to ground for +5V upshifted ECL operation. Connect to –5.2V for standard ECL operation. Must be at same potential as GND_E (Pin 11).
4	D_{IN}	Differential input. DC bias level is set internally at approximately 2.9V. Complimentary to $\overline{D_{IN}}$ (Pin 5).
5	$\overline{D_{IN}}$	Differential input. DC bias level is set internally at approximately 2.9V. Complimentary to D_{IN} (Pin 4).
6	V_{CCA}	Analog power supply pin. Connect to a +5V supply for upshifted ECL operation. Connect to ground for standard ECL operation. Must be at same potential as V_{CCE} (Pin 14).
7	C_F	Filter capacitor for level detector. Capacitor should be connected between this pin and V_{CCA}.
8	JAM	This ECL-compatible input controls the output buffers $\overline{D_{OUT}}$ and D_{OUT} (Pins 12 and 13). When an ECL LOW signal is applied, the outputs will follow the input signal. When an ECL HIGH signal is applied, the D_{OUT} and $\overline{D_{OUT}}$ pins will latch into LOW and HIGH states, respectively. When left unconnected, this pin is actively pulled-low (JAM OFF).
9	$\overline{ST}$	Input signal level-detect $\overline{STATUS}$. This ECL output is high when the input signal is below the user programmable threshold level.
10	ST	ECL compliment of $\overline{ST}$ (Pin 9).
11	GND_E	Digital GND pin. Connect to ground for +5V upshifted ECL operation. Connect to a negative supply for normal ECL operation. Must be at the same potential as GND_A (Pin 3).
12	$\overline{D_{OUT}}$	ECL-compatible output. Nominal level is V_{CCE}–1.3V. When JAM is HIGH, this pin will be forced into an ECL HIGH condition. Complimentary to D_{OUT} (Pin 13).
13	D_{OUT}	ECL-compatible output. Nominal level is V_{CCE}–1.3V. When JAM is HIGH, this pin will be forced into an ECL LOW condition. Complimentary to $\overline{D_{OUT}}$ (Pin 12).
14	V_{CCE}	Digital power supply pin. Connect to a +5V supply for upshifted ECL operation. Connect to ground during normal ECL operation. Must be at the same potential as V_{CCA} (Pin 6).
15	V_{REF}	Reference voltage for threshold level voltage divider. Nominal value is approximately 2.64V.
16	V_{SET}	Input threshold level setting circuit. This input can come from a voltage divider between V_{REF} and GND_A.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE	SA	
V_{CC}	Power supply (V_{CC} - GND)	6	6	V
T_A	Operating ambient	0 to +70	–45 to +85	°C
T_J	Operating junction	–55 to +150	–55 to +150	°C
T_{STG}	Storage	–65 to +150	–65 to +150	°C
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-pin Plastic SO	1100	1100	mW

NOTE:
1. Maximum dissipation is determined by the ambient temperature and the thermal resistance,
θ_{JA}: 16-pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	4.5 to 5.5	V
T_A	Ambient temperature ranges NE grade SA grade	 0 to +70 –40 to +85	 °C °C
T_J	Junction temperature ranges NE grade SA grade	 0 to +95 –40 to +110	 °C °C

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over operating temperature at V_{CC} = 5V ±10%, unless otherwise specified. Typical data apply at T_A = 25°C and V_{CC} = +5V.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA5224			UNIT
			Min	Typ	Max	
V_{IN}	Input signal voltage single-ended differential		 .002 .004		 1.5 3.0	V_{P-P}
V_{OS}	Input offset voltage[2]				50	µV
V_N	Input RMS noise[2]				60	µV
V_{TH}	Input level-detect programmability single-ended	V_{IN} = 200kHz square wave	2		12	mV_{P-P}
V_{HYS}	Level-detect hysteresis		4	5	6	dB
I_{CC}	V_{CCA} + V_{CCE} supply current	No ECL loading		27	35	mA
I_{INL}	JAM input current	Pin 8 = 0V	–10		10	µA
V_{OHMAX}	Maximum logic high[1]				–0.880	V_{DC}
V_{OHMIN}	Minimum logic high[1]		–1.055			V_{DC}
V_{OLMAX}	Maximum logic low[1]				–1.620	V_{DC}
V_{OLMIN}	Minimum logic low[1]		–1.870			V_{DC}
V_{IH}	Minimum input for JAM = high[1]		–1.165			V_{DC}
V_{IL}	Maximum input for JAM = low[1]				–1.490	V_{DC}

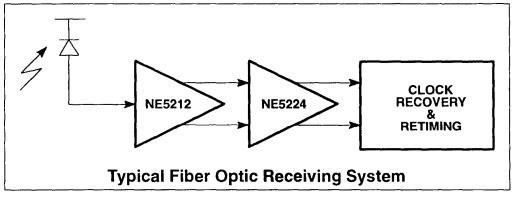
NOTES:
1. These ECL specifications are referenced to the V_{CCE} rail and apply for T_A = 0°C to 85°C.
2. Guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

Typical data apply at T_A = 25°C and V_{CC} = +5V. Min and Max limits apply for 4.5 ≤ V_{CC} ≤ 5.5V and specified NE or SA temperature range.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA5224			UNIT
			Min	Typ	Max	
BW_1	Lower –3dB bandwidth	C_{AZ} = 0.1µF	0.5	1.0	1.5	kHz
BW_2	Upper –3dB bandwidth		90	120	150	MHz
R_{IN}	Input resistance	Pin 4 or 5	2.9	4.5	7.6	kΩ
C_{IN}	Input capacitance	Pin 4 or 5			2.5	pF
t_r, t_f	ECL output[3] risetime, falltime	R_L = 50Ω To V_{CCE} - 2V 20-80%	1.2		2.2	ns
t_{PWD}	Pulsewidth distortion				0.3	ns_{P-P}
R_{AZ}	Auto zero output resistance	Pin 1 or 2	155	250	423	kΩ
R_F	Level-detect filter resistance	Pin 7	14	24	41	kΩ
t_{LD}	Level-detect time constant	C_F = 0	0.5	1.0	2.0	µs

NOTES:
1. Both outputs should be terminated identically to minimize differential feedback to the device inputs on a PC board or substrate.



Typical Fiber Optic Receiving System

INPUT BIASING

The DATA INPUT pins (4 and 5) are DC biased at approximately 2.9V by an internal reference generator. The NE5224 can be DC coupled, but the driving source must operate within the allowable 1.4V to 4.4V input signal range (for V_{CC} = 5V). If AC coupling is used to remove any DC compatibility requirement, the coupling capacitors C1 and C2 must be large enough to pass the lowest input frequency of interest. For example, .001µF coupling capacitors react with the internal 4.5k input bias resistors to yield a lower –3dB frequency of 35kHz. This then sets a limit on the maximum number of consecutive "1"s or "0"s that can be sensed accurately at the system data rate. Capacitor tolerance and resistor variation (2.9k to 7.6k) must be included for an accurate calculation.

AUTO-ZERO CIRCUIT

Figure 1 also shows the essential details of the auto-zero circuit. A feedback amplifier (A4) is used to cancel the offset voltage of the forward signal path, so the input to the internal ECL comparator (A6) is at its toggle point in the absence of any input signal. The time constant of the cancelling circuitry is set by an external capacitor (C_{AZ}) connected between Pins 1 and 2. The formula for the lower –3dB frequency is:

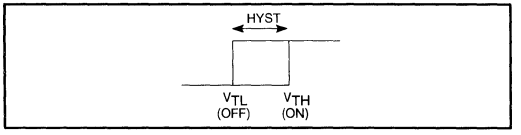
$$f_{-3dB} = \frac{150}{2\pi \cdot R_{AZ} \cdot C_{AZ}}$$

where R_{AZ} is the internal driving impedance which can vary from 155k to 423k over temperature and device fabrication limits. The input coupling time constant must also be considered in determining the lower frequency response of the NE5224.

INPUT SIGNAL LEVEL-DETECTION

The NE5224 allows for user programmable input signal level-detection and can automatically disable the switching of its ECL data outputs if the input is below a set threshold. This prevents the outputs from reacting to noise in the absence of a valid input signal, and insures that data will only be transmitted when the input signal-to-noise ratio is sufficient for low bit-error-rate system operation. Complimentary ECL flags (ST and STB) indicate whether the input signal is above or below the desired threshold level.

Figure 2 shows a simplified block diagram of the NE5224 level-detect system. The input signal is amplified and rectified before being compared to a programmable reference. A filter is included to prevent noise spikes from triggering the level-detector. This filter has a nominal 1µs time constant, and additional filtering can be achieved by using an external capacitor (CF) from Pin 7 to V_{CCA} (the internal driving impedance is nominally 24k). The resultant signal is then compared to a programmable level, V_{SET}, which is set by an internal voltage reference (2.64V) and an external resistor divider (R1 and R2). The value of R1 + R2 should be maintained at approximately 5k.



The circuit is designed to operate accurately over a differential 2-12mV_{P-P} square-wave input level detect range. This level, $V_{SET}/100$, is the average of V_{TH} and V_{TL}.

Nominal hysteresis of 5dB is provided by the complimentary ECL output comparator yielding $V_{TL} = \frac{V_{SET}}{139}$ and $V_{TH} = \frac{V_{SET}}{78}$. For example, with V_{SET} = 1.2V, a 15.4mV_{P-P} square-wave differential input will drive the ST pin high, and an input level below 8.6mV_{P-P} will drive the ST pin low.

Since a "JAM" function is provided (Pin 8) and can force the data outputs to a predetermined state (D_{OUT} = LOW, $\overline{D_{OUT}}$ = HIGH), the $\overline{ST}$ and JAM pins can be connected together to automatically disable signal transmission when the chip senses that the input signal is below the desired threshold. JAM (Pin 8) low enables the Data Outputs. $\overline{ST}$ will be in a high ECL state for input signals below threshold.

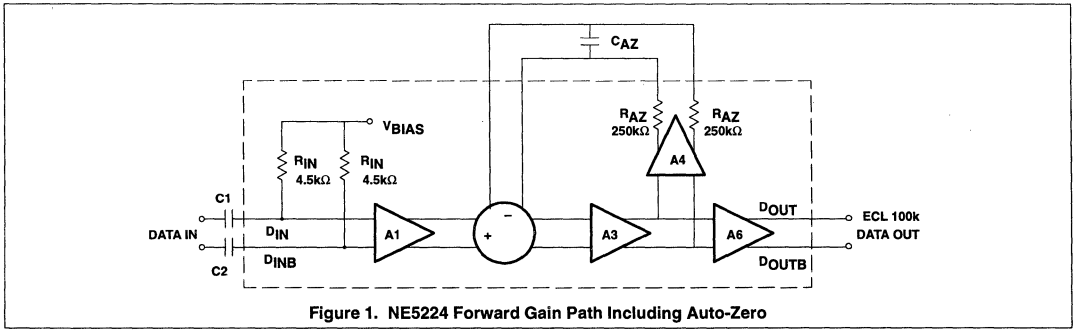


Figure 1. NE5224 Forward Gain Path Including Auto-Zero

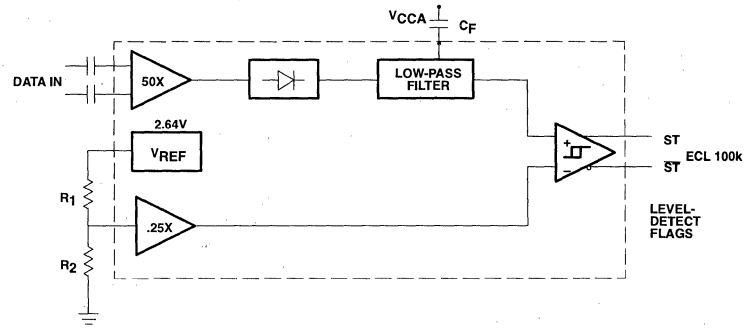


Figure 2. NE5224 Input Signal Level-Detect System

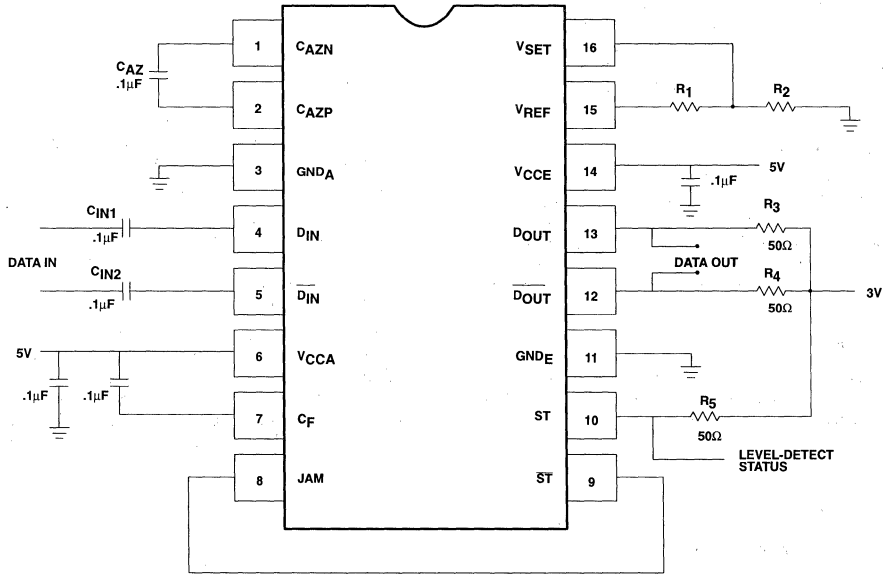


Figure 3. Application with V_{CC} = 5.0V

NOTE: A 50Ω resistor is required from Pin 9 to 3V only if the $\overline{ST}$ pin is required to meet 100k ECL specifications.

Fiber optic postamplifier — NE/SA5225

DESCRIPTION

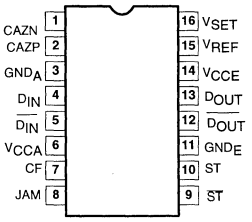
The NE/SA5225 is a high-gain limiting amplifier that is designed to process signals from fiber optic preamplifiers. Capable of operating at 125Mb/s, the chip has input signal level-detection with a user-adjustable threshold. The DATA and LEVEL-DETECT outputs are differential for optimum noise margin and ease of use. Also available is the NE/SA5224 which is optimized for FDDI applications.

FEATURES

- Wideband operation: 1.0kHz to 120MHz typical
- Operation with single +5V or –5.2V supply
- Differential 10k ECL outputs
- Programmable input signal level-detection
- Fully differential for excellent PSRR to 1GHz

PIN DESCRIPTION

D Package



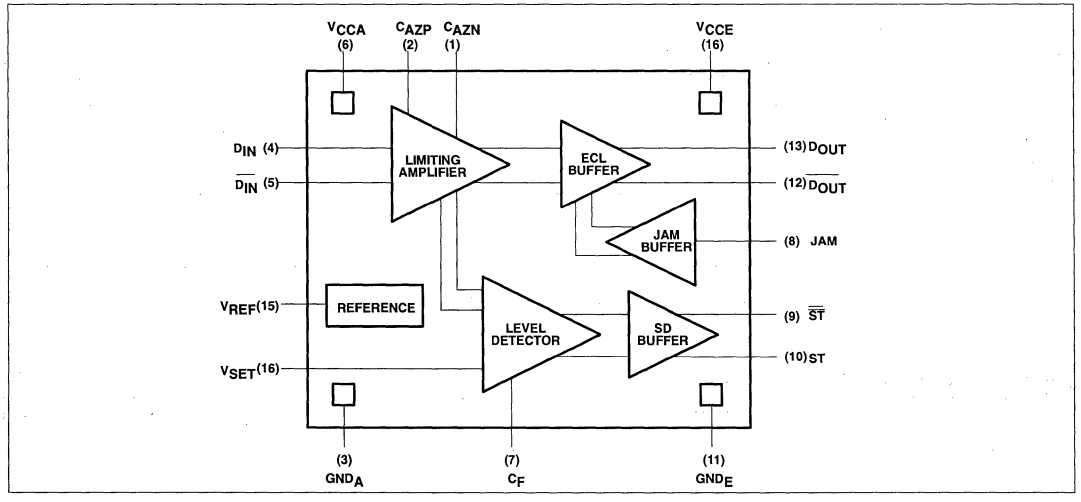
APPLICATIONS

- Data communication in noisy industrial environments
- LANs

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE5225D	0005D
16-Pin Plastic Small Outline (SO) Package	–40 to +85°C	SA5225D	0005D

BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NO.	NAME	FUNCTION
1	C_{AZN}	Auto-zero capacitor pin. Connecting a capacitor between this pin and C_{AZP} will cancel the offset voltage of the limiting amplifier.
2	C_{AZP}	Auto-zero capacitor pin. Connecting a capacitor between this pin and C_{AZN} will cancel the offset voltage of the limiting amplifier.
3	GND_A	Analog GND pin. Connect to ground for +5V upshifted ECL operation. Connect to –5.2V for standard ECL operation. Must be at same potential as GND_E (Pin 11).
4	D_{IN}	Differential input. DC bias level is set internally at approximately 2.9V. Complimentary to $\overline{D_{IN}}$ (Pin 5).
5	$\overline{D_{IN}}$	Differential input. DC bias level is set internally at approximately 2.9V. Complimentary to D_{IN} (Pin 4).
6	V_{CCA}	Analog power supply pin. Connect to a +5V supply for upshifted ECL operation. Connect to ground for standard ECL operation. Must be at same potential as V_{CCE} (Pin 14).
7	C_F	Filter capacitor for level detector. Capacitor should be connected between this pin and V_{CCA}.
8	JAM	This ECL-compatible input controls the output buffers $\overline{D_{OUT}}$ and D_{OUT} (Pins 12 and 13). When an ECL LOW signal is applied, the outputs will follow the input signal. When an ECL HIGH signal is applied, the D_{OUT} and $\overline{D_{OUT}}$ pins will latch into LOW and HIGH states, respectively. When left unconnected, this pin is actively pulled-low (JAM OFF).
9	$\overline{ST}$	Input signal level-detect $\overline{STATUS}$. This ECL output is high when the input signal is below the user programmable threshold level.
10	ST	ECL compliment of $\overline{ST}$ (Pin 9).
11	GND_E	Digital GND pin. Connect to ground for +5V upshifted ECL operation. Connect to a negative supply for normal ECL operation. Must be at the same potential as GND_A (Pin 3).
12	$\overline{D_{OUT}}$	ECL-compatible output. Nominal level is V_{CCE}–1.3V. When JAM is HIGH, this pin will be forced into an ECL HIGH condition. Complimentary to D_{OUT} (Pin 13).
13	D_{OUT}	ECL-compatible output. Nominal level is V_{CCE}–1.3V. When JAM is HIGH, this pin will be forced into an ECL LOW condition. Complimentary to $\overline{D_{OUT}}$ (Pin 12).
14	V_{CCE}	Digital power supply pin. Connect to a +5V supply for upshifted ECL operation. Connect to ground during normal ECL operation. Must be at the same potential as V_{CCA} (Pin 6).
15	V_{REF}	Reference voltage for threshold level voltage divider. Nominal value is approximately 2.64V.
16	V_{SET}	Input threshold level setting circuit. This input can come from a voltage divider between V_{REF} and GND_A.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE	SA	
V_{CC}	Power supply (V_{CC} - GND)	6	6	V
T_A	Operating ambient	0 to +70	–45 to +85	°C
T_J	Operating junction	–55 to +150	–55 to +150	°C
T_{STG}	Storage	–65 to +150	–65 to +150	°C
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-pin Plastic SO	1100	1100	mW

NOTE:
1. Maximum dissipation is determined by the ambient temperature and the thermal resistance,
θ_{JA}: 16-pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	4.5 to 5.5	V
T_A	Ambient temperature ranges NE grade SA grade	 0 to +70 –40 to +85	 °C °C
T_J	Junction temperature ranges NE grade SA grade	 0 to +95 –40 to +110	 °C °C

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over operating temperature at V_{CC} = 5V ±10%, unless otherwise specified. Typical data apply at T_A = 25°C and V_{CC} = +5V.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA5225			UNIT
			Min	Typ	Max	
V_{IN}	Input signal voltage single-ended differential		 .002 .004		 1.5 3.0	V_{P-P}
V_{OS}	Input offset voltage[2]				50	µV
V_N	Input RMS noise[2]				60	µV
V_{TH}	Input level-detect programmability single-ended	V_{IN} = 200kHz square wave	2		12	mV_{P-P}
V_{HYS}	Level-detect hysteresis[3]		2	3	4	dB
I_{CC}	V_{CCA} + V_{CCE} supply current	No ECL loading		27	35	mA
I_{INL}	JAM input current	Pin 8 = 0V	–10		10	µA
V_{IH}	Minimum input for JAM = high[1]		–1.165			V_{DC}
V_{IL}	Maximum input for JAM = low[1]				–1.490	V_{DC}

NOTES:
1. These ECL specifications are referenced to the V_{CCE} rail and apply for T_A = 0°C to 85°C.
2. Guaranteed by design.
3. Also see the NE/SA5224 which has 5dB ±1dB hysteresis for FDDI compatibility.

TABLE 1: 10K ECL VOLTAGE LEVELS (REFERENCED TO V_{CCE})

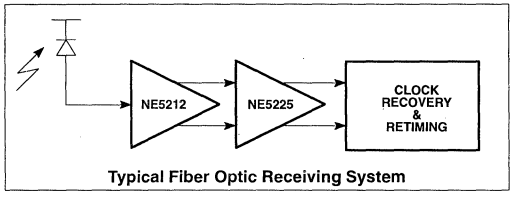
PARAMETER	-30°C	0°C	25°C	75°C	85°C	UNIT
V_{OHMAX}	-0.890	-0.840	-0.810	-0.735	-0.700	V_{DC}
V_{OHMIN}	-1.060	-1.020	-.980	-.920	-.890	V_{DC}
V_{OLMAX}	-1.650	-1.630	-1.630	-1.600	-1.615	V_{DC}
V_{OHMIN}	-1.890	-1.950	-1.950	-1.950	-1.920	V_{DC}

AC ELECTRICAL CHARACTERISTICS

Typical data apply at T_A = 25°C and V_{CC} = +5V. Min and Max limits apply for 4.5 ≤ V_{CC} ≤ 5.5V and specified NE or SA temperature range.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA5225			UNIT
			Min	Typ	Max	
BW_1	Lower –3dB bandwidth	C_{AZ} = 0.1µF	0.5	1.0	1.5	kHz
BW_2	Upper –3dB bandwidth		90	120	150	MHz
R_{IN}	Input resistance	Pin 4 or 5	2.9	4.5	7.6	kΩ
C_{IN}	Input capacitance	Pin 4 or 5			2.5	pF
t_r, t_f	ECL output[1] risetime, falltime	R_L = 50Ω To V_{CCE} - 2V 20-80%	1.2		2.2	ns
t_{PWD}	Pulsewidth distortion				0.3	ns_{P-P}
R_{AZ}	Auto zero output resistance	Pin 1 or 2	155	250	423	kΩ
R_F	Level-detect filter resistance	Pin 7	14	24	41	kΩ
t_{LD}	Level-detect time constant	C_F = 0	0.5	1.0	2.0	µs

NOTES:
1. Both outputs should be terminated identically to minimize differential feedback to the device inputs on a PC board or substrate.



Typical Fiber Optic Receiving System

INPUT BIASING

The DATA INPUT pins (4 and 5) are DC biased at approximately 2.9V by an internal reference generator. The NE5225 can be DC coupled, but the driving source must operate within the allowable 1.4V to 4.4V input signal range (for V_{CC} = 5V). If AC coupling is used to remove any DC compatibility requirement, the coupling capacitors C1 and C2 must be large enough to pass the lowest input frequency of interest. For example, .001µF coupling capacitors react with the internal 4.5k input bias resistors to yield a lower –3dB frequency of 35kHz. This then sets a limit on the maximum number of consecutive "1"s or "0"s that can be sensed accurately at the system data rate. Capacitor tolerance and resistor variation (2.9k to 7.6k) must be included for an accurate calculation.

AUTO-ZERO CIRCUIT

Figure 1 also shows the essential details of the auto-zero circuit. A feedback amplifier (A4) is used to cancel the offset voltage of the forward signal path, so the input to the internal ECL comparator (A6) is at its toggle point in the absence of any input signal. The time constant of the cancelling circuitry is set by an external capacitor (C_{AZ}) connected between Pins 1 and 2. The formula for the lower –3dB frequency is:

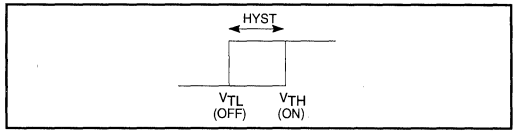
$$f_{-3dB} = \frac{150}{2\pi \cdot R_{AZ} \cdot C_{AZ}}$$

where R_{AZ} is the internal driving impedance which can vary from 155k to 423k over temperature and device fabrication limits. The input coupling time constant must also be considered in determining the lower frequency response of the NE5225.

INPUT SIGNAL LEVEL-DETECTION

The NE5225 allows for user programmable input signal level-detection and can automatically disable the switching of its ECL data outputs if the input is below a set threshold. This prevents the outputs from reacting to noise in the absence of a valid input signal, and insures that data will only be transmitted when the input signal-to-noise ratio is sufficient for low bit-error-rate system operation. Complimentary ECL flags (ST and STB) indicate whether the input signal is above or below the desired threshold level.

Figure 2 shows a simplified block diagram of the NE5225 level-detect system. The input signal is amplified and rectified before being compared to a programmable reference. A filter is included to prevent noise spikes from triggering the level-detector. This filter has a nominal 1µs time constant, and additional filtering can be achieved by using an external capacitor (CF) from Pin 7 to V_{CCA} (the internal driving impedance is nominally 24k). The resultant signal is then compared to a programmable level, V_{SET}, which is set by an internal voltage reference (2.64V) and an external resistor divider (R1 and R2). The value of R1 + R2 should be maintained at approximately 5k.



The circuit is designed to operate accurately over a differential 2-12mV_{P-P} square-wave input level detect range. This level, V_{SET}/100, is the average of V_{TH} and V_{TL}.

Nominal hysteresis of 3dB is provided by the complimentary ECL output comparator yielding $V_{TL} = \frac{V_{SET}}{121}$ and $V_{TH} = \frac{V_{SET}}{85}$. For example, with V_{SET} = 1.2V, a 14.05mV_{P-P} square-wave differential input will drive the ST pin high, and an input level below 9.95mV_{P-P} will drive the ST pin low.

Since a "JAM" function is provided (Pin 8) and can force the data outputs to a predetermined state (D_{OUT} = LOW, $\overline{D_{OUT}}$ = HIGH), the $\overline{ST}$ and JAM pins can be connected together to automatically disable signal transmission when the chip senses that the input signal is below the desired threshold. JAM (Pin 8) low enables the Data Outputs. $\overline{ST}$ will be in a high ECL state for input signals below threshold.

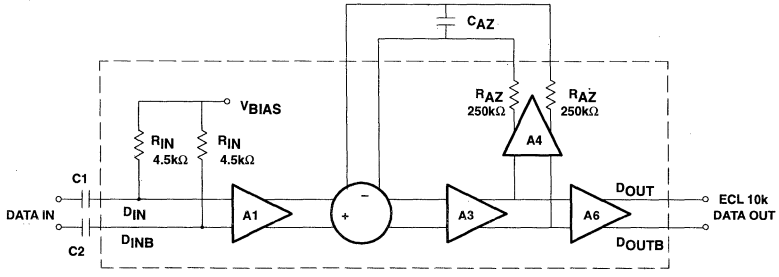


Figure 1. NE5225 Forward Gain Path Including Auto-Zero

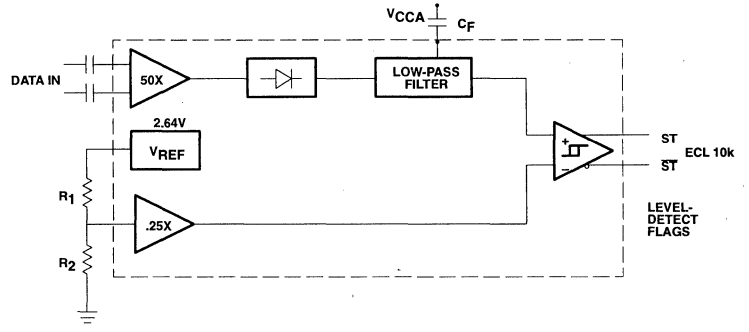


Figure 2. NE5225 Input Signal Level-Detect System

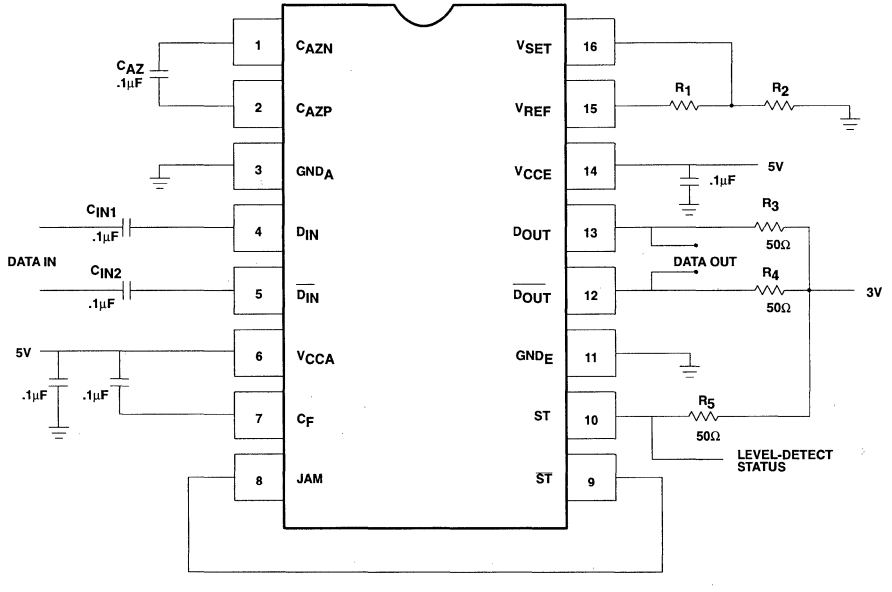


Figure 3. Application with V_{CC} = 5.0V

NOTE: A 50Ω resistor is required from Pin 9 to 3V only if the $\overline{ST}$ pin is required to meet 10k ECL specifications.

A family of wideband low noise transimpedance amplifiers AN1435

INTRODUCTION

Despite numerous advantages, the relatively high cost of fiber optic transmission prevented its wide-spread industrial acceptance. High bandwidth-distance products, a prerequisite for cost-effectiveness, could not be achieved with relatively inexpensive components. The latest technological advances on both transmitter and receiver sides, however, are about to change that.

Transmitter

Starting at the transmitter side (Figure 1), the two major problems of the past were the lack of inexpensive, light emitting diode (LED) transmitters, capable of 10-20MHz modulation rates, and the compounded problem of cost and reliability of laser diodes, required for large channel capacity, single mode, long-distance systems.

In examining the present status of the fiber optic industry we observe, however, that new generations of LEDs, used in most short range, multi-mode transmitters, can achieve wide modulation bandwidths, enabling system designers to develop cost-effective systems. For example, commercially available 820-820nm AlGaAs surface emitting devices have significantly decreased in price and can be used up to and beyond 100MHz (200MBaud). InGaAsP LEDs can be used in the 1.3µm range. Their highly doped versions can be modulated up to bandwidths of several hundred MHz at the expense of lower output power.

InGaAsP laser diodes can go well beyond 1GHz. Their higher output power and an order of magnitude narrower spectral widths make these devices the ideal choice for long-range, very high data rate telecommunication systems.

Receiver

The key to cost effectiveness at the receiver side is the ability to offer monolithic IC building blocks that can match those high transmitter data rates with bandwidth, large dynamic range and low noise. These kinds of IC building blocks weren't readily available in the past. Consequently, system designers had to choose between limiting data rates to below 20MBaud or using costly hybrid modules.

Philips Semiconductors solution to the problem is the introduction of a family of transimpedance amplifiers (TiA). These are the NE5210, NE5211 and NE5212.

Although the real meaning is different, "transresistance" and "transimpedance" are, in practice, used interchangeably. These names designate that these types of amplifiers are current-driven at their inputs and generate voltage at their outputs. The transmitter function is, therefore, a ratio of output voltage to input current with dimensions of ohms. Since the input is current driven, the input resistance must be low, which means low input voltage- swings, no capacitive charge/discharge currents and wide frequency response with a generous phase margin. Alternative approaches to the TIA, such as high input impedance FET preamplifiers with a shunt input resistor, tend to be more bandwidth limited. They exhibit integrating characteristics, and therefore must be equalized by a differentiating second stage to achieve broad frequency response. The integrating input stage, however, is prone to overload with signals that have high low-frequency content. If the amplifier overloads for any reason, the integrated waveform cannot be restored by differentiation and dynamic range suffers despite the low noise characteristics.

Since the transimpedance configuration does not have this problem, its superior dynamic range, inherently large bandwidth and compatibility with low cost IC technologies make it an attractive approach.

Transimpedance Amplifier Family

The NE5210, NE5211 and NE5212 TIA is a low noise, wide band integrated circuit with single signal input and differential outputs, ideally suited for fiber optic receivers, both digital and analog, in addition to many other RF applications. Table 1 depicts the differences between the three amplifiers. As shown in Figure 2, a differential output configuration was chosen to achieve good power supply rejection ratio and to provide ease of interface with ECL type postamplifier circuitry. The input stage (A1) has a low noise shunt-series feedback configuration. The open loop gain of A1 (R_F = infinite) is about 70; therefore, we can assume with good approximation an input stage transresistance equal to the value of R_F. Since the second stage differential amplifier (A2) and the output emitter-followers (A3 and A4) have a voltage gain of about two, the input to output transresistance is twice the value of R_F. The single-ended transresistance is half of this value.

Returning to the input stage (Figure 3), a simple analysis can be used to determine the performance of the TiA. The input resistance, R_{IN}, can be calculated as:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}}$$

For the NE5210: $R_{IN} \cong \frac{3.6k}{1 + 70} = 60\Omega$

For the NE5211: $R_{IN} \cong \frac{14.4k}{1 + 70} = 200\Omega$

For the NE5212: $R_{IN} \cong \frac{7.2k}{1 + 70} = 110\Omega$

Typical input capacitance of the TIA, C_{IN}, are 7.5pF, 4pF and 10pF for NE5210, NE5211 and NE5212, respectively.

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

= 350MHz (NE5210)
= 200MHz (NE5211)
= 145MHz (NE5212)

Thus, while neglecting driving source and stray capacitances, R_{IN} and C_{IN} will form the dominant hole of the entire amplifier: Although significantly wider bandwidths could have been achieved by a cascade input stage configuration, the present solution has the advantage of a very uniform, highly desensitized frequency response because the Miller-effect dominates over external photodiode and stray capacitances. Consequently, the NE5210, NE5211, NE5212 will be relatively insensitive to PIN photodiode source capacitance variations. Since the dominant pole of the amplifier is at the input node, PIN diode source capacitance will not degrade phase margin.

Package Parasitics

Package parasitics, particularly ground-lead inductances, can significantly degrade frequency response. To minimize parasitics, multiple grounds are used in order to minimize ground wire-bond inductances.

Further bandwidth modifications can be achieved by a small capacitance between input and output or input and ground. Since each of the NE5210, NE5211 and NE5212 has differential outputs, both peaking and attenuating type frequency response shaping are possible.

A family of wideband low noise transimpedance amplifiers

AN1435

Table 1. Wideband Transimpedance Amplifier Family

PART	DIFFERENTIAL TRANSRESISTANCE kΩ (typ.)	BANDWIDTH -3dB (typ.)	INPUT NOISE CURRENT (typ.)	MAX. INPUT CURRENT
NE5212	14	140MHz	2.5pA/√Hz	±120μA
NE5211	28	180MHz	1.8pA/√Hz	±60μA
NE5210	7	280MHz	3.5pA/√Hz	±240μA

Fighting Noise

Since most currently installed and planned fiber optic systems use non-coherent transmission and detect incident optical power, receiver noise performance becomes important. The NE5210, NE5211 and NE5212 go a long way towards solving this problem. Their input stage configurations achieve a respectably low input referred noise current spectral density of 3.5pA/√Hz for the NE5210, 1.8pA/√Hz for the NE5211 and 2.5pA/√Hz for the NE5212, measured at 10MHz. This low value is nearly flat over the entire bandwidth. The transresistance configuration assures that the external high value bias resistors, often required for photodiode biasing, will not contribute to total system noise. As shown in the following equation, the equivalent input $_{RMS}$ noise current is determined by the quiescent operating point of Q_1, the feedback resistor, R_F, and the bandwidth, Δf^*, however, it is not dependent on the internal Miller-capacitance. The noise current equation is then

$$\overline{i_{eq2}} = 4kT \frac{\Delta f}{R_F} + 2q I_{BQ1} \Delta f$$
$$+ 2q I_{CQ1} \frac{1}{g_m^2} \omega^2 (C_S + C_{\pi 1})^2 \Delta f$$
$$+ 4kT r_{bQ1} \omega^2 C_S^2 \Delta f$$

The resulting integrated noise over 100MHz with C_S = 1pF is
40nA for NE5210
21nA for NE5211
32nA for NE5212

Testing the NE5212

The remaining portion of this paper deals specifically with the NE5212 and is directly applicable to the NE5211 and the NE5210.

Connecting the NE5212 in an actual fiber optic preamplifier configuration, dynamic range, transient response, noise and overload recovery tests are easily measured (Figure 4). In order to replicate actual parasitic capacitances, effects of the photodiode bias network and circuit layout effects, the test circuit should closely resemble the real application conditions. If the intention is to use the device in die form, then the actual hybrid circuit mounting techniques should be used while testing.

In the test circuit shown, an 850nm modulated laser light source feeds an HP-HFBR2202 PIN photodiode which is mounted in close proximity to the NE5212 input. The RC filter in series with the photodiode eliminates possible disturbances from the power supply. Both differential outputs are AC coupled through 33Ω resistors in order to match to the 50Ω test system. In most applications these matching resistors are unnecessary. Performance evaluation in the linear region, including amplitude and phase response and power supply rejection, can be accomplished by a network analyzer and S parameter test set (Figure 5). The simple equations given in the figure for the calculation of transresistance, R_T, are accurate for $R >> R_{IN}$, where R_{IN} is the input resistance of the NE5212.

General Purpose RF Applications

Besides the main fiber optic receiver applications, many other interesting possibilities exist for the NE5212. Simplicity and ease-of-use are the prevailing characteristics of this device. For instance, amplifiers with 20dB gain can be built requiring only one external gain setting resistor (Figure 6). The voltage gain of the differential configuration with no load at the outputs can be calculated as follows:

$$V_{OUT} = I_{IN} \times R_T = \frac{V_{IN}}{R_S + R + R_{IN}} \quad R_T \text{ and}$$

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{R_T}{R_S + R + R_{IN}}$$

where R_S is the signal-source resistance, R is the external gain setting resistor and R_{IN} is the input resistance of the NE5212. Substituting the actual values:

$$A_V = \frac{14000}{R_S + R + 110}$$

where all values are in ohms. The graph of Figure 6 is an experimental verification of this formula in a single-ended, 50Ω system, using the test configuration of Figure 5. Note the 6dB loss due to the single-ended configuration and another 6dB due to the 50Ω load. As in all other RF applications, attention to power supply bypassing clean grounds and minimization of input stray capacitances are required for optimum performance.

Another useful application of the NE5212 is as a voltage controlled amplifier, using a DMOS FET device biased into the linear region (Figure 7). An operational amplifier with supply-to-ground output swing and supply-to-ground input common mode range (such as the Philips Semiconductors NE5230) can provide adequate gate control voltage even with a single 5V power supply. This type of circuit can have 25dB AGC range at 50MHz and 45dB at 10MHz with less than 1% harmonic content. AGC range is determined by the ON resistance range of the FET and capacitive drain to source feedthrough. If lowest RF feedthrough were required, the FET should be used in a shunt configuration rather than in a series.

Turning towards an entirely different area of application, where contrary to the NE5212's capabilities, poor phase margins are mandatory, a simple crystal oscillator with buffered output can be built using a minimum number of external components (Figure 8). The feedback signal is taken from the non-inverting output, while the inverting output provides a low impedance (15Ω) output drive. The crystal operates in its series resonance mode. Figure 9 shows a varactor tuned version with a large tuning range. In Figure 10 the circuit has been optimized for stability at the expense of tuning range.

In RF amplifier applications it is often desirable to limit the amplifier bandwidth in order to minimize noise and RFI. The 100-150MHz bandwidth of the NE5212 can be easily modified by connecting a capacitor to the input pin. The device bandwidth then becomes

A family of wideband low noise transimpedance amplifiers AN1435

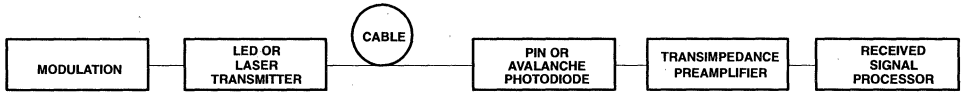


Figure 1. Fiber Optic Transmission System Using Transresistance Preamplifier

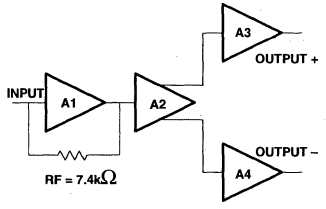
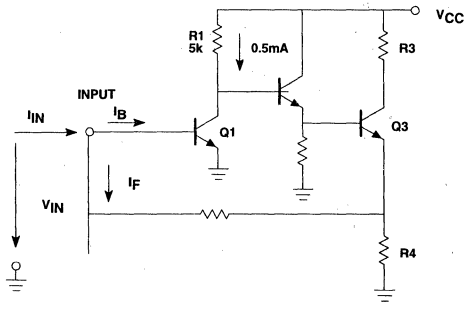


Figure 2. NE5212 Block Diagram Showing the Transresistance Preamplifier with the Internal Feedback Resistor and the Buffered Differential Outputs.

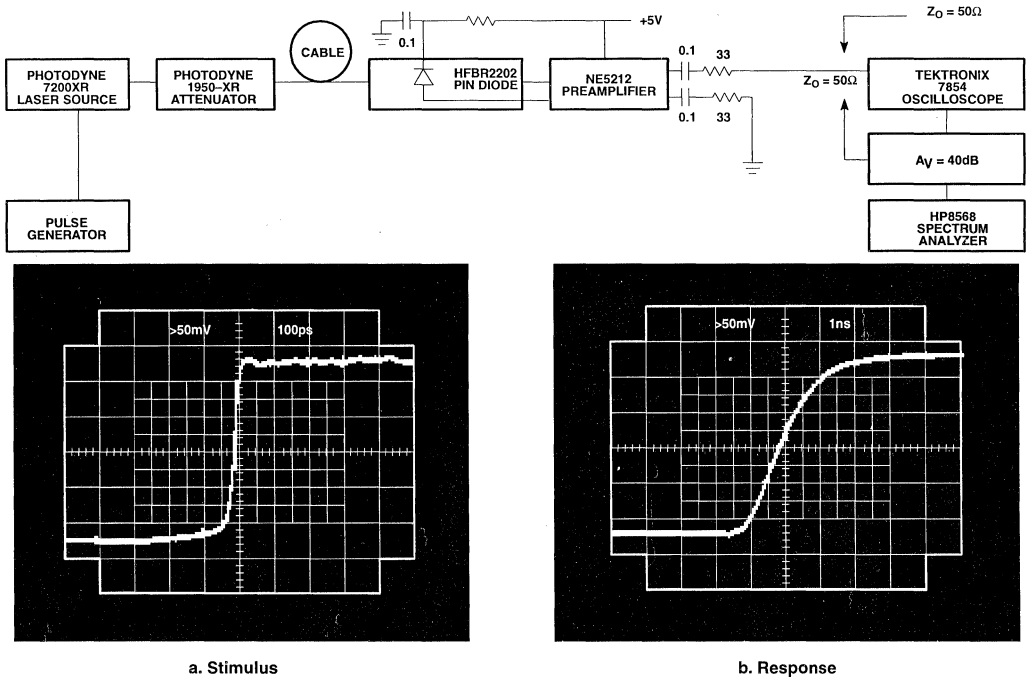


This simple shunt-series input stage has some hidden features besides its very low noise. Due to the Miller-effect, the collector-base capacitance of Q1, multiplied by a voltage gain of 70, forms the dominant pole with RF, while desensitizing frequency response to source capacitance variations.

Figure 3.

$$f_{-3dB} = \frac{1}{2\pi R_{IN} (C_{IN} + C_{EXT})}$$

where R_{IN} is the input resistance, C_{IN} is the input capacitance as specified in the data sheet and C_{EXT} is the external capacitance. For example, a C_{EXT} = 33pF will reduce the amplifier bandwidth to 42MHz with a single pole roll-off. The penalty is an increase in noise current. The transfer curve is shown in Figure 11. Another way to limit the bandwidth is to connect a capacitor across the differential output. Single-ended to differential conversion is another useful application for the device. Impedance matching is easily accomplished by resistors connected in series with the outputs.



a. Stimulus b. Response

Figure 4. Dynamic Range, Impulse Response and Noise Test Circuit

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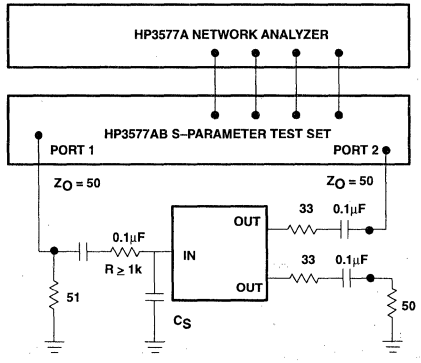
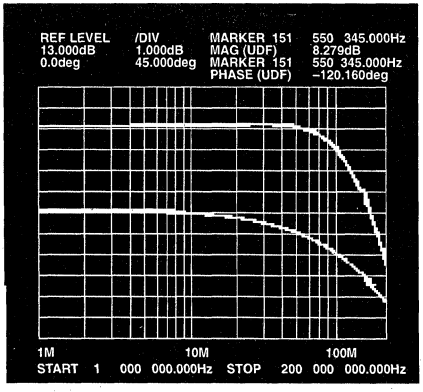
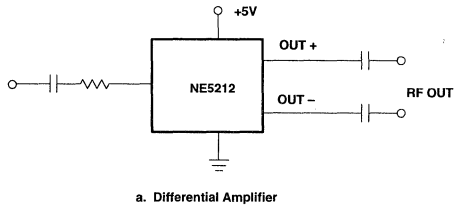


SINGLE-ENDED	DIFFERENTIAL
$R_t = \frac{V_{OUT}}{V_{IN}}$ R = S21 x R	$R_t = \frac{V_{OUT}}{V_{IN}}$ R = 2 x S21 x R
$R_O = Z_O \left\lvert \frac{1 + S22}{1 - S22} \right\rvert$ - 33	$R_O = 2Z_O \left\lvert \frac{1 + S22}{1 - S22} \right\rvert$ - 66

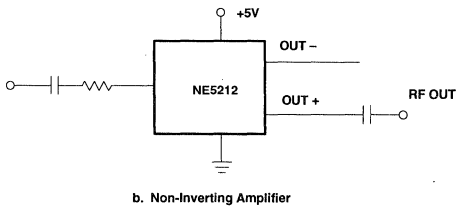


The frequency response can be conveniently measured with an S-parameter network analyzer. The 1k Ohm input resistor acts as a voltage to current converter and the resistors at the output do the impedance matching. The curves show a smooth, wideband response with ample phase margin. Transresistance and output resistance can be calculated from the S-parameters as shown in the table.

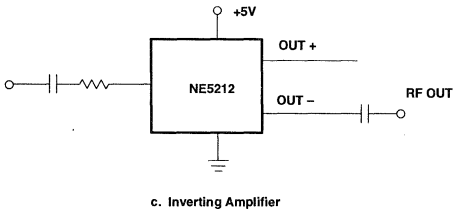
Figure 5.



a. Differential Amplifier

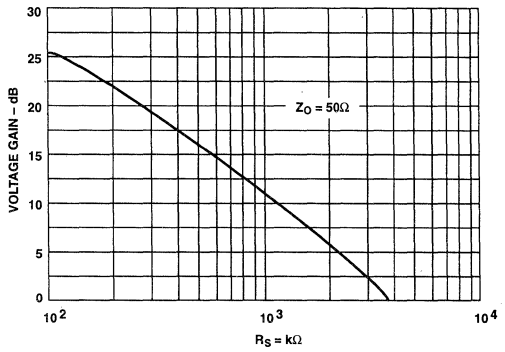


b. Non-Inverting Amplifier



c. Inverting Amplifier

A 150MHz, 20dB amplifier requires only one external gain setting resistor. Differential or single-ended opeation with or without inversion is possible.



Single-Ended Gain vs R

Figure 6.

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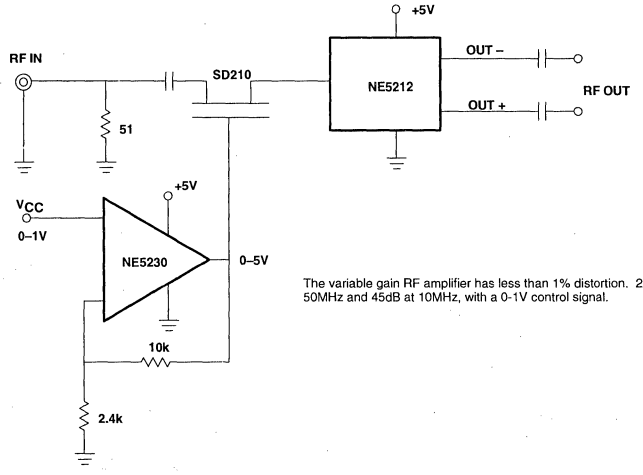


The variable gain RF amplifier has less than 1% distortion. 25dB range at 50MHz and 45dB at 10MHz, with a 0-1V control signal.

Figure 7.

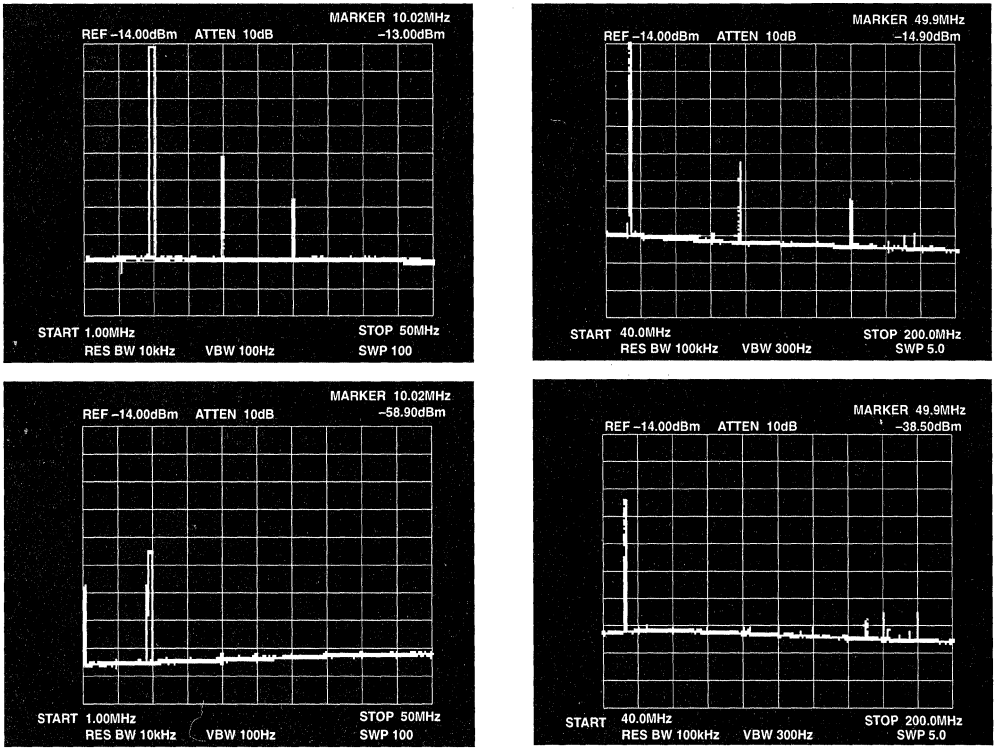
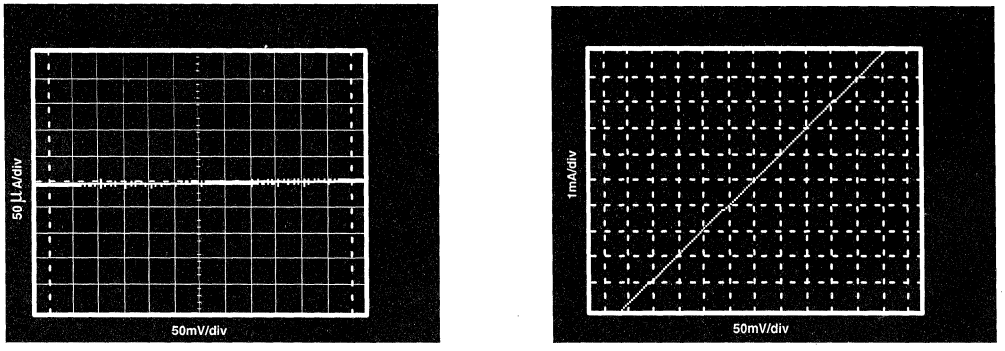
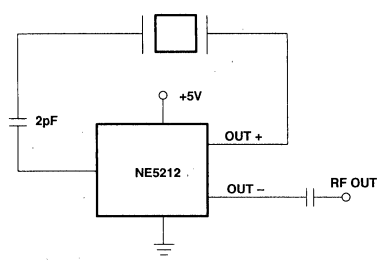


Figure 8. Performance Data of the RF Attenuator of Figure 7



FET resistance in its linear region at V_{GS} = 0V (left) and at V_{GS} = 5V (right).

Figure 9.



This 16MHz crystal oscillator has minimum component count and operates in the series resonant mode. Output provides independent 50 Ohm drive capability.

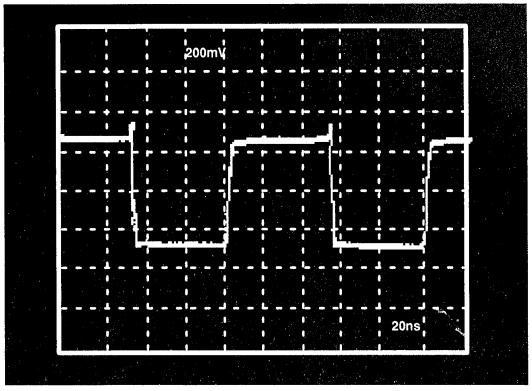
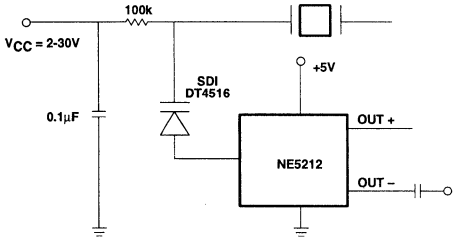


Figure 10.



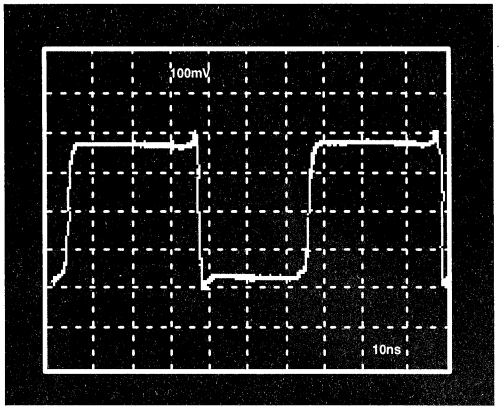
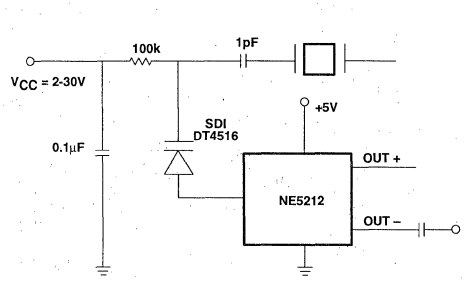


Figure 11. Varactor Tuned Crystal Oscillator with 0.28% Tuning Range



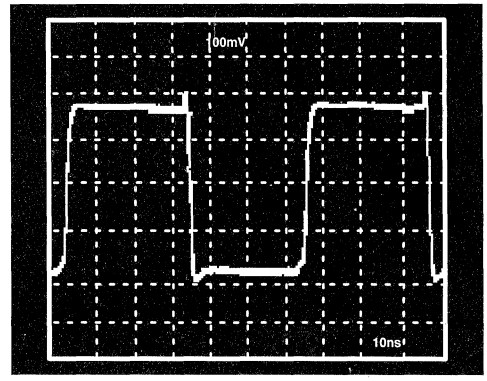
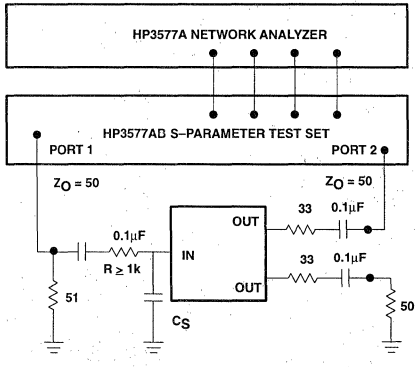


Figure 12. Varactor Tuned Oscillator with 1ppm/V Supply Sensitivity



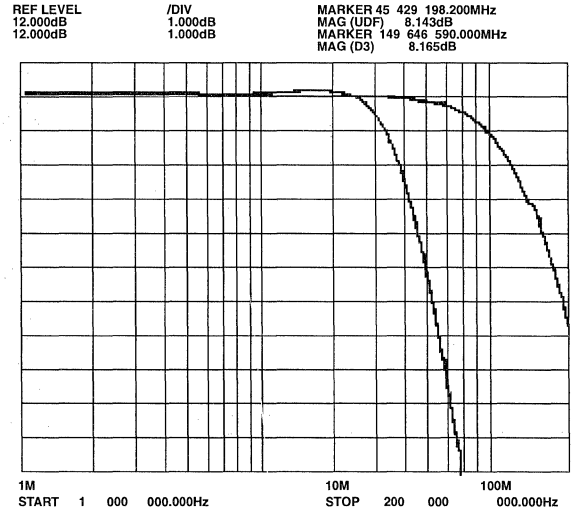


Figure 13. Setting Bandwidth with Shunt Input Capacitor, C_S

Section 7
Futurebus+ Products
Data Sheets

CONTENTS

Futurebus+ / BTL: A high performance standard for advanced computing and communication systems

INTRODUCTION

INTRODUCTION

Futurebus+ specifications were developed by several participants from commercial and non-commercial sectors worldwide. These participants represent system-level companies, component manufacturers, equipment manufacturers and other engineering professionals. Philips Semiconductors has been actively involved in the development of the specifications. We now offer the most essential parts of Futurebus+ specification — the Arbitration Controller and BTL Transceivers.

Futurebus+ is an IEEE specification (IEEE896.1) that also includes the Backplane Transceiver Logic (BTL) specification (IEEE 1194). It is especially designed for high performance backplane-based computing that permits architectural consistency across a broad range of systems. It provides a 64-bit architecture and datapath extensions up to 256 bits.

Some of the major benefits of the protocol are due to its efficient support of fault tolerance, live insertion (a.k.a., hot insertion or hot swapping), high speed – low power dissipation, and room for extension. These benefits mainly stem from the BTL level support for the backplane.

BTL logic requires implementation of Schottky Diode, Bipolar output structures and CMOS internal logic. All these requirements necessitate the use of BiCMOS technology. Philips has implemented these ICs in the industry's most advanced BiCMOS process technology (QUBiC). Philips implements several logic ICs and ASSPs (Application Specific Standard Products) in this technology. Since the late 1980s, Philips has produced several million ICs using this process technology. Applications of QUBiC are ABT driver family, Custom ICs for automotive manufacturers, Mass Storage Electronics, and RF/Wireless Communication chip-sets, to name but a few.

Major Applications:

Figure 1 shows a typical computing or communications environment that utilizes the key features of Futurebus+ and BTL. Figure 2 shows a typical configuration of Philips Futurebus+ chip-set.

Figure 1 depicts an environment that needs live insertion and high-reliability all the time, such as Massively Parallel Computers, Fault Tolerant Computers, or Network Controller Systems, etc. Any such environment that requires a high speed backplane bus can use the Futurebus+/BTL transceivers. The main requirements of such backplane bus are Low Power Dissipation at high speed and the ability to swap boards while the system remains powered-up (i.e., Live Insertion).

Several of our major customers make use of the 7-bit, 8-bit or 9-bit BTL transceivers for conversion of BTL signals from the bus to TTL signals on board. These transceivers are now fully qualified and characterized for high volume production.

Table 1. Philips Futurebus+/BTL Product Offering

Part Number	Description	Special Feature
FB2031BB	Futurebus+ 9-bit transceiver	0 – 70°C
FB2031IBB	Futurebus+ 9-bit transceiver	–40 – +85°C
FB2041BB	Futurebus+ 7-bit transceiver	0 – 70°C
FB2041IBB	Futurebus+ 7-bit transceiver	–40 – +85°C
FB2033BB	Futurebus+ 8-bit transceiver	0 – 70°C
FB2040ABB	Futurebus+ 8-bit transceiver	0 – 70°C
FB2012AA	Futurebus+ Centralized Arbitration Controller	0 – 70°C

NOTES:
1. BB = 52-Pin Plastic Quad Flat Pack;
   A = 68-Pin Plastic Leaded Chip Carrier

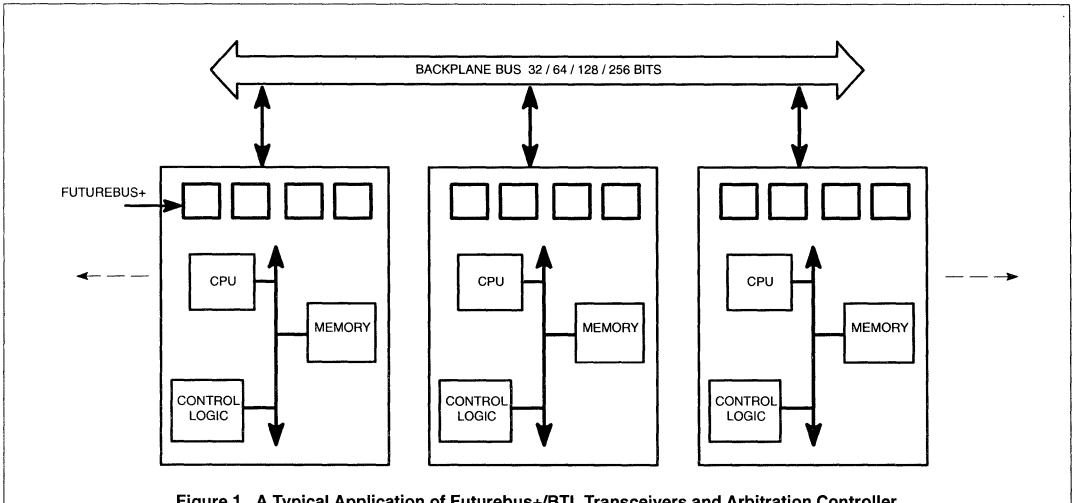


Figure 1. A Typical Application of Futurebus+/BTL Transceivers and Arbitration Controller

Futurebus+ / BTL: A high performance standard for advanced computing and communication systems

INTRODUCTION

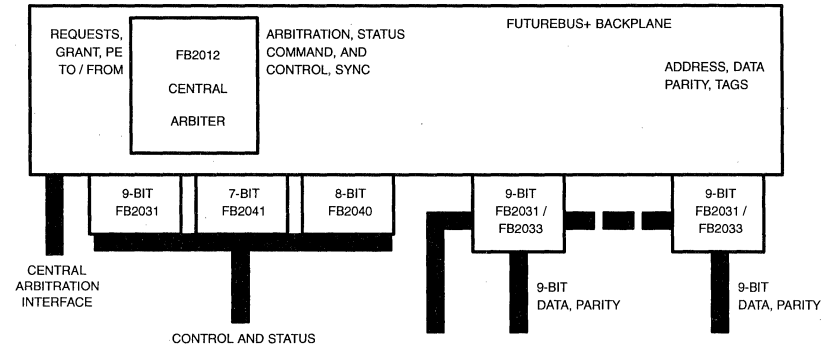


Figure 2. Futurebus+ Implementation with Philips Semiconductors Futurebus+ Chip-set

Key Features of Philips Futurebus+/BTL Chip-set:

The key features of Philips Futurebus+/BTL chip-set are as follows:

- Compatible with IEEE specifications of Futurebus+ (IEEE896) and BTL (IEEE1194)
- Most of the parts fully characterized over Commercial as well as Industrial temperature range
- Manufactured in high volume state-of-the-art 0.9µm BiCMOS technology (QUBiC)
- Arbitration Controllers implemented using centralized bus arbitration scheme providing higher performance than distributed arbitration
- 7-bit, 8-bit and 9-bit transceivers with:
  - An excellent EMI shielding due to isolated GND planes between BTL and TTL sides
  - Low propagation delays and well-controlled edge rates
- Product availability: Fully qualified and characterized products available for high volume production
- All four transceivers are Alternate Sourced by Texas Instruments

For more detailed information and samples, please contact the nearest Philips Semiconductors Sales Office.

Futurebus+ central arbitration controller — FB2012A

GENERAL DESCRIPTION OF THE FB2012A

The FB2012A is the central arbitration controller for the Futurebus+ product family. When a module needs to send data to or obtain data from another module, it must first gain tenure of the bus. The FB2012A controls or arbitrates tenure of the bus to one module at a time.

The FB2012A includes BTL drivers and receivers for signals that use the Futurebus+ backplane. Since the request and grant lines are point-to-point, they need to be terminated only at the receiver. Request lines are terminated at the FB2012A, and grant lines are terminated at the individual Futurebus+ modules. If stub lengths to the FB2012A create problems for the RE* and PE* signals, an external BTL receiver may be used for RE* and and an external BTL driver may be sourced by the TTL PE* signal. If the external BTL receiver is inverting, the resulting TTL signal (RE*) must be inverted as well.

GENERAL DESCRIPTION OF THE FUTUREBUS+ CENTRAL ARBITRATION PROTOCOL

A requesting module asserts either a level-1 (RQH*) or a level-0 (RQL*) request to obtain bus mastership. A low-priority (level-0) request may become a high-priority request by leaving the low-priority request asserted while also asserting the corresponding high-priority (level-1) request.

A module may release the request(s) anytime after a grant is received from the FB2012A if the need for a bus transaction vanishes. Once a request is made, it may not be removed until the corresponding grant has been received (according to IEEE 896.1). (The FB2012A gives the user the option to release a request before the corresponding grant is asserted or to follow IEEE 896.1.)

A requesting module becomes the bus master only after it receives the bus grant and the current bus master releases its tenure (the current bus master has released its request, but may still be in the middle of a transaction). This condition is indicated by the continued assertion of ET*. When the current bus master has finished its transaction and has released the address/data bus, it releases ET*. Once the module with the asserted bus grant detects the release of ET*, it becomes the bus master and may begin its transaction. The bus master's request(s) must remain asserted until it asserts ET*. Refer to FUNCTIONAL WAVEFORMS.

The central arbiter asserts PE* to indicate that a preemptive condition exists and that the current bus master should relinquish the bus. The definition of the preemptive condition is described in the FUNCTIONAL DESCRIPTION section below.

FEATURES

- The Philips Semiconductors Central Arbitration Controller is compatible with the IEEE P896.1 Futurebus+ standard
- 14 level-1 first-come-first-served requests
- 14 level-0 first-come-first-served requests
- 14 bus grants
- Priority preemption
- Timing for Futurebus+ RE* signal
  - Bus initialization
  - System reset
- 68-pin PLCC package

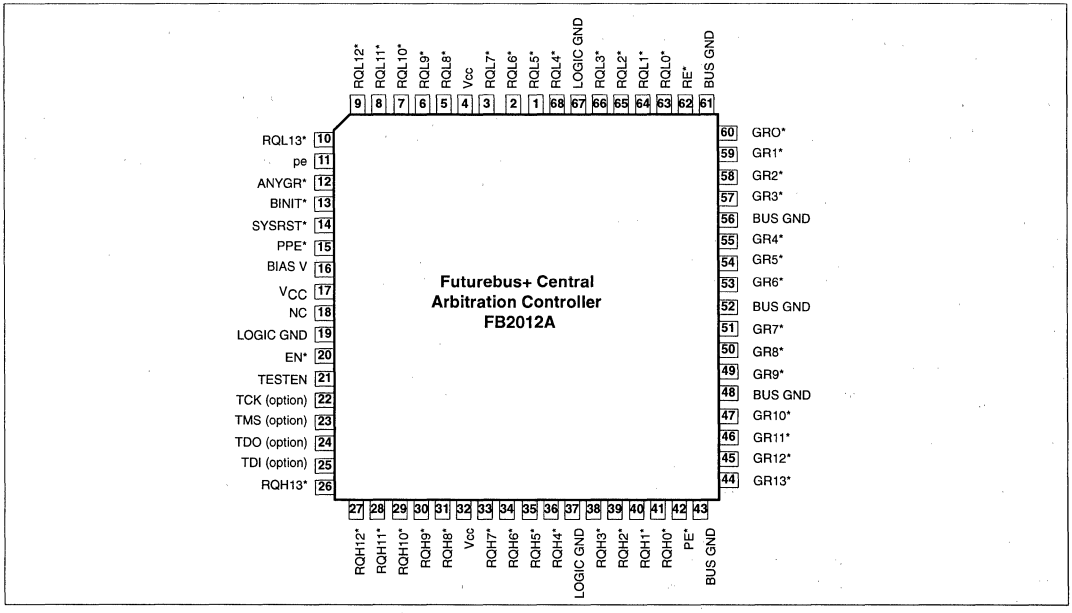
QUICK REFERENCE DATA

SYMBOL	PARAMETER		TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay RQXn to GRn		1.4 5.4	ns
C_O	Output capacitance		6	pF
I_{OL}	Output current	TTL outputs	4	mA
		BTL outputs	80	
I_{CC}	Supply current		80	mA

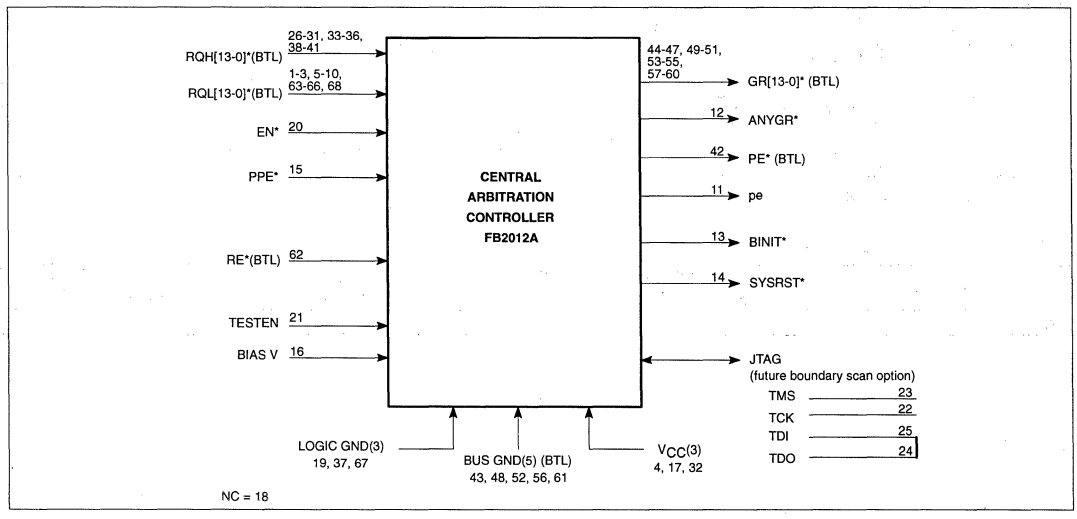
ORDERING INFORMATION

PACKAGE	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0 to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10%; T_{amb} = -40 to +85°C	DWG No.
68-pin PLCC	FB2012AA	FB2012AA	0398E

PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION OF THE FB2012A

The FB2012A has two priority levels, each with 14 inputs. For ease of labeling, the two priority levels, labeled RQ1* and RQ0* in the Futurebus+ 896.1 specification, are labeled RQHn* (level-1) and RQLn* (level-0), respectively, on the FB2012A, where 'n' is the module number from 0 through 13. The assignment of a module to a particular request line has no significance; all requests (of a particular priority level) are treated identically. Once asserted, a request should remain asserted until the corresponding grant is received (according to IEEE 896.1). (If the user chooses to release a request before the corresponding grant is asserted, he may do so; the FB2012A allows this option.) Level-0 and level-1 requests may be asserted simultaneously. Refer to FUNCTIONAL WAVEFORMS for general functionality.

A grant will become active only after any metastable conditions involving its request(s) are resolved. Only one of the 14 grant lines will be active at a time. The order of serviced requests for each level is first-come-first-served (FCFS) — the request that has been asserted the longest receives the grant. However, level-0 requests are serviced only when no level-1 requests are asserted.

The grant outputs are enabled when the EN* input is Low. However, when EN* is released while a grant is active, the grant will remain active until the corresponding request(s) are released. Also, whenever a grant is asserted, the ANYGR* output signal will also be asserted.

The FB2012A has two preemption modes:

1. If the PPE* input is asserted (priority preemption mode), PE* and pe will be asserted whenever there is a level-1 request that is not being serviced while another grant is asserted. That is, the preemption lines will be asserted if more than one level-1 request is asserted or if a level-0 request is being serviced when a level-1 request(s) is asserted.
2. If PPE* is not asserted, PE* and pe will be asserted whenever two or more requests, regardless of their priority levels, are asserted. (Assertion of a level-1 request and a level-0 request from the same module is considered as a single request.)

The action taken by a module when PE* (and pe) are asserted is strictly up to the designer.

The FB2012A monitors RE* to detect the signaling of the bus initialize and system reset conditions. If the RE* input is asserted less than 2.0ms, neither BINIT* (bus initialize) nor SYSRST* (system reset) will be asserted. If RE* is asserted longer than 2.0ms, BINIT* may be asserted; and after 3.9ms BINIT* is guaranteed to be asserted. If RE* is asserted longer than 30ms, SYSRST* may be asserted; and after 60ms SYSRST* is also guaranteed to be asserted. If asserted, BINIT* and SYSRST* will be released after RE* has been released at least 60ns and no more than 140ns.

When BINIT* is asserted, future grants are disabled in the same way that they are disabled in response to the de-assertion of the EN* signal. (Normally all requests are removed during bus initialization). When SYSRST* is asserted, PE* (and pe) will also be forced into the asserted state indiependently of pre-emption conditions. After RE* has been continuously released for at least 1μs and for not more than 2.2μs, the grants are re-enabled and PE* (with pe) is released from its forced assertion, if it had entered one. (Insome systems, the assertion of PE* for at least 1μs after the release of RE* (following system reset) is a condition that signals the presence of a central arbiter.)

To accommodate the possibility of a system requirement for redundant and removable FB2012A, a BIAS V input is provided to bias the internal BTL circuity. This way the redundant FB2012A may be live inserted without disrupting system operation.

For designs with a single FB2012A, the BIAS V input should be connected to V_{CC}.

METASTABILITY CHARACTERISTICS OF THE FB2012A

One of the concerns when dealing with an asynchronous arbiter is understanding what would happen when competing requests arrive at the same time. Input requests are processed by a bank of mutual-exclusion elements. A mutual-exclusion element (ME) is a state-holding device that arbitrates between a pair of inputs. This is the point at which metastabilities can occur. The design of the ME precludes anomalous signaling by suppressing output assertion until metastabilities are resolved.

To determine the Mean Time Between Unacceptable Delays (MTBUD) the following formula is used:

$$\text{MTBUD} = \frac{\exp(\frac{t'}{\tau})}{(T_O)(f_{r1}f_{r2})}$$

t' is the maximum acceptable delay between the request edge (RQXn) and the corresponding grant output signal (GR*); and f_{rx} is the frequency of the request inputs.

The central arbiter has metastability characteristics of τ of 93ps, T_O of 2.3E33 seconds, and a normal propagation of 8.76ns measured at room temperature and 5V V_{CC}. (Those unfamiliar with these parameters may consult Philips Semiconductors application note AN219, "A Metastability Primer".)

The following example shows that at an individual ME, metastability induced delays of appreciable size are extremely rare.

Assume that there are two possible requests and the average request frequency for each is 250kHz. From the formula above, with a t' of 10.76ns (8.76ns + 2ns), the MTBUD is calculated to be 341 hours. If t' was 12.76ns, the MTBUD would be about 85 million years. Notice that 12.76ns is only an additional four nanosecond delay above the normal propagation delay. (This example assumes that a module may make a request immediately upon releasing tenure.)

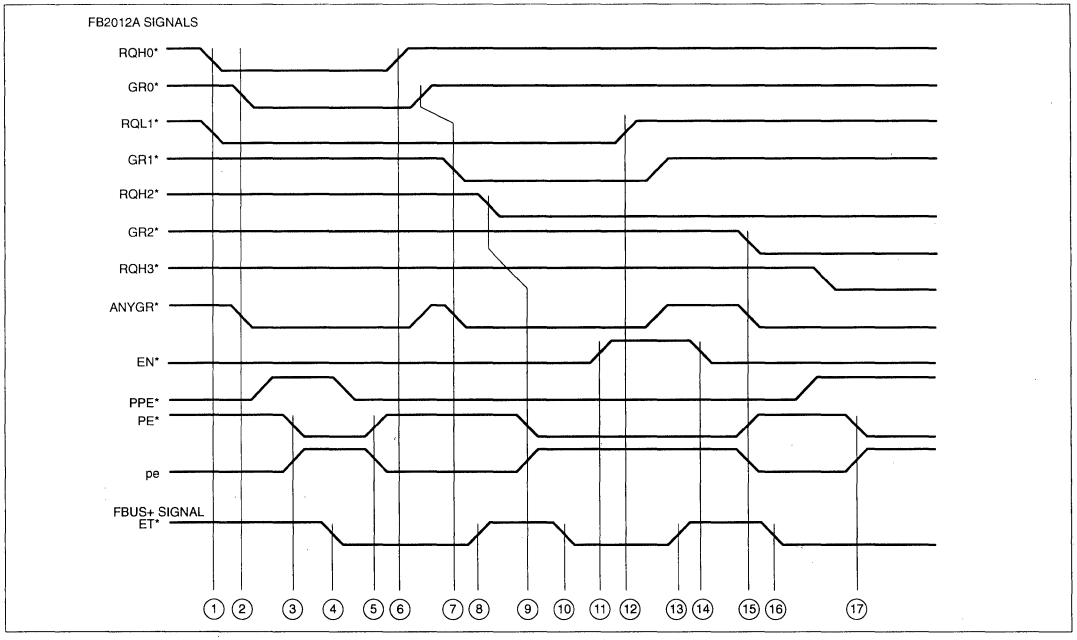
The example illustrates only two modules competing for the bus. In real systems more request channels are active and more MEs are involved. If 'n' channels are active, then n(n-1)/2 MEs are active. Note, however, that any metastabilities that occur while a grant is active undesired delay would be noticed.

It is difficult to imagine that a user would ever experience a grant delay that cannot be tolerated.

PIN DESCRIPTION

SYMBOL	TYPE	PIN NUMBER	FROM/TO	FUNCTION
RQH[13-0]*	I-BTL	26, 27, 28, 29, 30, 31, 33, 34, 35, 36, 38, 39, 40, 41	Futurebus+	These are level 1 requests. Grants are allocated on a first-come-first-served (FCFS) basis. The request that has been asserted the longest receives the grant.
RQL[13-0]*	I-BTL	10, 9, 8, 7, 6, 5, 3, 2, 1, 68, 66, 65, 64, 63	Futurebus+	These are level 0 requests. Level 0 requests are serviced when no level 1 requests are asserted. Requests are serviced according to the order of assertion (FCFS). The request that has been asserted the longest receives the grant.
GR[13-0]*	O-BTL	44, 45, 46, 47, 49, 50, 51, 53, 54, 55, 57, 58, 59, 60	Futurebus+	Each GRn* corresponds to an RQHn* and RQLn*. Once asserted a request must remain asserted until its corresponding grant is asserted. A grant GRn* is de-asserted when both the corresponding RQHn* and RQLn* are de-asserted. (Open-collector)
ANYGR*	O-TTL	12	Module	If any GR* pin is asserted ANYGR* is also asserted.
BINIT*	O-TTL	13	Module	Signals other controllers to initialize their Futurebus+ signals. This pin is driven Low after RE* is Low has been asserted for more than 2.0ms. Will return High after RE* has been released for at least 60ms.
EN*	I-TTL	20	Module	When high, all GR* lines that are not asserted will remain not asserted. An asserted GRn* will remain asserted until both the associated RQHn* line and RQLn* line are released.
pe	O-TTL	11	Futurebus+	pe is the inverted TTL equivalent of the BTL PE* pin.
PE*	O-BTL	42	Futurebus+	When PPE* is Low, PE* will be asserted whenever there is a level-1 request that is not being serviced while another grant is asserted. When PPE* is High, PE* will be asserted if more than one request (level-1
PPE*	I-TTL	15	Module	and/or level-0) is asserted. If level-1 and level-0 requests from the same module (i.e., RQH1 and RQL1), they are considered as one request. (PE* is Open-collector)
RE*	I-BTL	62	Futurebus+	Futurebus+ reset.
SYSRST*	O-TTL	14	Module	Indicates a system reset has been signaled on the Futurebus. (Open-collector)
TESTEN	I-TTL	21	Tester	Used only for out-of-board testing (users should hold this pin low).
BIAS V	I-TTL	16		Low current input to properly bias the BTL drivers during live insertion or withdrawal. If live insertion or withdrawal is not a design consideration, this pin should be connected to V_{CC}.
LOGIC GND	G-TTL	19, 37, 67		TTL ground.
BUS GND	G-BTL	43, 48, 52, 56, 61		BTL ground.
V_{CC}	V	4, 17, 32		Power supply.
JTAG[TDI, TDO, TMS, TCK]	I/O-TTL	25, 24, 23, 22	Module	These four pins are reserved for future implementation of the JTAG standard. TDI and TDO are shorted together. TMS and TCK are not connected.
NC	NC	18		No connect (reserved for future use).

FUNCTIONAL WAVEFORMS



1. Module 0 and module 1 make request (**RQH0** and **RQL1**) — grant given to module 0 due to level-1 priority request.
2. Central Arbitration Controller asserts **GR0*** and **ANYGR***.
3. The preemption outputs (**PE*** and **pe**) are asserted indicating that multiple modules are requesting grants.
4. The current bus master, module 0, asserts **et*** after beginning a transaction.
5. The priority preemption input (**PPE***) has gone low which causes the preemption outputs (**PE*** and **pe**) to be released.
6. Module 0 finishes its need for bus tenure and releases its request.
7. The Central Arbitration Controller detects the release of the module 0 request and releases the corresponding grant. The Module 1 request is then serviced — **GR1*** is asserted (and **ANYGR*** also). Module 1 is now the bus master elect.
8. The bus master (module 0) releases **et*** to indicate to module 1 that it, module 1, is the new bus master.
9. A new level-1 request is received from module 2. Since **PPE*** is asserted it causes **PE*** and pe to be asserted indicating that there is an unserviced level-1 request.
10. Module 1 asserts **et*** after beginning a transaction.
11. The **EN*** pin is released blocking service to any unserviced requests. The asserted grant (**GR1***) remains asserted until the corresponding requests are released.
12. Module 1 releases its request. Because **EN*** is High no new grants are asserted.
13. Module 1 releases **et***.
14. **EN*** is again asserted.
15. The module 2 grant (**GR2***) becomes asserted. **PE*** and pe are released because the level-1 request is now serviced.
16. Module 2, now the bus master, asserts **et*** after beginning a transaction.
17. When module 3 asserts its request, **PE*** and **pe** become asserted because now two requests are asserted at the same time (and **PPE*** is High).

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-1.2 to +7.0	V
I_{IN}	Input current		-18 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	TTL outputs except SYSRST*	8	mA
		SYSRST*	24	
		GR0* - GR13, PE*	80	
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS		UNIT
			Min	Max	
V_{CC}	DC supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage	TTL inputs	2.0		V
		RQX0* - RQX13*, RE*	1.62		V
V_{IL}	Low-level input voltage	TTL inputs		0.8	V
		RQX0* - RQX13*, RE*		1.47	V
I_{IK}	Input diode current			-18	mA
I_{OH}	High level output current	TTL except SYSRST*		-1	mA
I_{OL}	Low-level output current	TTL except SYSRST*		4	mA
		SYSRST*		24	
		GR0* - GR13, PE*		80	
C_O	Output capacitance	GRn*, PE*		7	pF
T_{amb}	Operating free-air temperature range		0	+70	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				MIN	TYP[2]	MAX	
I_{OH}	High level output current	SYSRST*	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 4.5V			100	µA
	High level output current	GRn*, PE*	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V			100	µA
I_{OFF}	Power-off output current	GRn*, PE*	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V			100	µA
V_{OH}	High level output voltage	ANYGR*, BINIT, pe[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = −1mA	2.5	2.85		V
V_{OL}	Low level output voltage	ANYGR*, BINIT, pe[4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 4mA		0.33	0.5	V
		SYSRST*	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 24mA		0.33	0.5	
		GRn*, PE*	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 80mA	.75	1.0	1.10	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−1.2	V
I_I	Input current at maximum input voltage	EN*, PPE*, TESTEN	V_{CC} = MAX, V_I = GND or 5.5V			±50	µA
		RQXn*, RE*				±100	
I_{OS}	Short circuit output current[3]	ANYGR*, BINIT, pe	V_{CC} = MAX, V_O = 0V	−30		−100	mA
I_{CC}	Supply current (total)		V_{CC} = MAX, Outputs High or Low		80	120	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are V_{IH} = 1.8V and V_{IL} = 1.3V for BTL inputs.

LIVE INSERTION SPECIFICATIONS

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			MIN	TYP[2]	MAX	
V_{BIASV}	Bias pin voltage	V_{CC} = 0 to 5.25V, $\overline{Bn}$ = 0 to 2.0V	4.5		5.5	V
I_{BIASV}	Bias pin DC current	V_{CC} = 0 to 4.75V, $\overline{Bn}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V			1	mA
		V_{CC} = 4.5 to 5.5V, $\overline{Bn}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V			10	
√Bn	Bus voltage during prebias	$\overline{B0}$–$\overline{B8}$ = 0V, Bias V = 5.0V	1.62		2.1	V
I_{LM}	Fall current during prebias	$\overline{B0}$–$\overline{B8}$ = 2V, Bias V = 4.5 to 5.5V	1			µA
I_{HM}	Rise current during prebias	$\overline{B0}$–$\overline{B8}$ = 1V, Bias V = 4.5 to 5.5V	-1			µA
$I_{\overline{Bn}PEAK}$	Peak bus current during insertion	V_{CC} = 0 to 5.25V, $\overline{B0}$ to $\overline{B8}$= 0 to 2.0V, Bias V = 4.5 to 5.5V, OEB0 = 0.8V, t_r = 2ns			10	mA
$I_{\overline{OL}OFF}$	Power up current	V_{CC} = 0 to 5.25V, OEB0 = 0.8V			100	µA
		V_{CC} = 0 to 2.2V, OEB0 = 0 to 5V			100	
t_{GR}	Input glitch rejection	V_{CC} = 5.0V		1.35	1.0	ns

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	TTL LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0 - +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay RQHn* or RQLn* to pe (PPE* = High)	Waveform 2	5.3 4.5	10.2 9.4	12.0 11.8	4.3 3.3	12.3 12.1	ns
t_{PLH}	Propagation delay RQHn* to pe (PPE* = Low)	Waveform 2	5.1	8.4	10.5	4.2	10.9	ns
t_{PHL}	Propagation delay RQHa* to pe (PPE* = Low)[1]	Waveform 2	5.5	8.5	10.2	4.8	11.5	ns
t_{PLH} t_{PHL}	Propagation delay RQHn* or RQLn* to ANYGR*	Waveform 1	3.7 5.0	8.6 9.7	10.5 12.0	3.0 4.2	11.0 12.2	ns
t_{PHL}	Propagation delay EN* to ANYGR*	Waveform 1	6.6	9.0	10.6	5.2	10.9	ns
SYMBOL	PARAMETER	TEST CONDITIONS	TTL LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 16.5Ω			T_{amb} = 0 - +70°C, V_{CC} = 5V ±10%, C_D = 30pF, R_U = 16.5Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay RGHn* or RQLn* to GRn*	Waveform 1	2.0 2.0	5.2 8.6	7.0 11.5	2.0 2.0	7.5 11.9	ns
t_{PHL}	Propagation delay RGHa* or RQLa* to GRb*[1]	Waveform 2	4.5	12.0	15.3	4.3	15.5	ns
t_{PLH} t_{PHL}	Propagation delay RQHn* or RQLn* to PE* (PPE* = High)	Waveform 1	3.0 2.7	9.3 8.4	11.9 10.2	2.0 2.0	12.4 10.5	ns
t_{PHL}	Propagation delay RQHn* to PE* (PPE* = Low)	Waveform 1	2.6	7.0	8.7	1.7	8.9	ns
t_{PLH}	Propagation delay RGHa* to PE* (PPE* = Low)[1]	Waveform 1	3.7	8.3	10.0	3.6	10.3	ns
t_{PHL}	Propagation delay EN* to GRn*	Waveform 1	2.6	6.9	8.4	2.0	8.8	ns

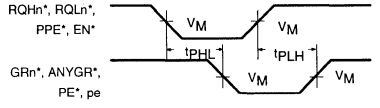
NOTE:

1. RQHa or RQLa represent requests that already have a corresponding GRa* grant asserted. GRb* represents a grant not yet asserted, but GRb* becomes asserted when GRa* is released, if RQHb and/or RQLb are asserted.

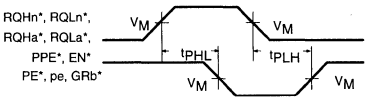
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	TTL LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 16.5Ω, C_L = 50pF, R_L = 500Ω			T_{amb} = 0 - +70°C, V_{CC} = 5V ±10%, C_D = 30pF, R_U = 16.5Ω, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_{W}(L)$	RE* pulse width, Low (to assert BINIT*)		2.0		3.9	2.0	3.9	ms
$t_{W}(L)$	RE* pulse width, Low (to assert SYSRST*)		30.0		60	30.0	60	ms
t_{rec}	Recovery time RE* to BINIT* or SYSRST*		60.0	100	140	60.0	140	ns
t_{rec}	Recovery time RE* to GRn*		1.0		2.2	1.0	2.2	µs

AC WAVEFORMS



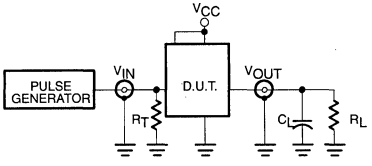
Waveform 1. Propagation Delay For Non-Inverting Paths



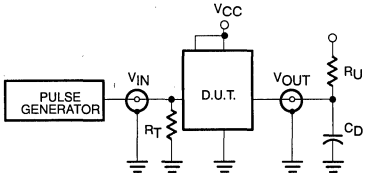
Waveform 2. Propagation Delay For Inverting Paths

NOTE: V_M = 1.55V for RQHn*, RQLn*, RQHa*, RQLa*, GRn*, GRb* or PE*, V_M = 1.5V for all others.
The Shaded areas indicate when the inputs is permitted to change for predictable output performance.

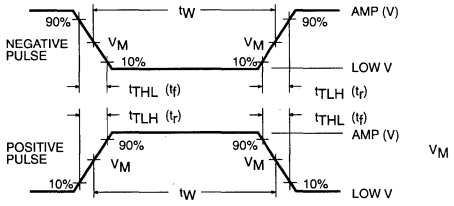
TEST CIRCUIT AND WAVEFORMS



Test Circuit For Outputs On TTL Port



Test Circuit For Outputs On BTL Port



V_M = 1.55V for RQHn*, RQLn* or RE*,
V_M = 1.5V for all others
Input Pulse Definition

FAMILY FB+	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep Rate	t_W	t_{TLH}	t_{THL}
TTL Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
BTL Port	2.0V	1.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_U = Pull up resistor; see AC CHARACTERISTICS for value.

9-bit latched/registered/pass-thru Futurebus+ transceiver FB2031

FEATURES

- Latched, registered or straight through in either A to B or B to A path
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω.
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Each BTL driver has a dedicated Bus GND for a signal return
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch-free power up/power down operation
- Low I_{CC} current
- Tight output skew
- Supports live insertion

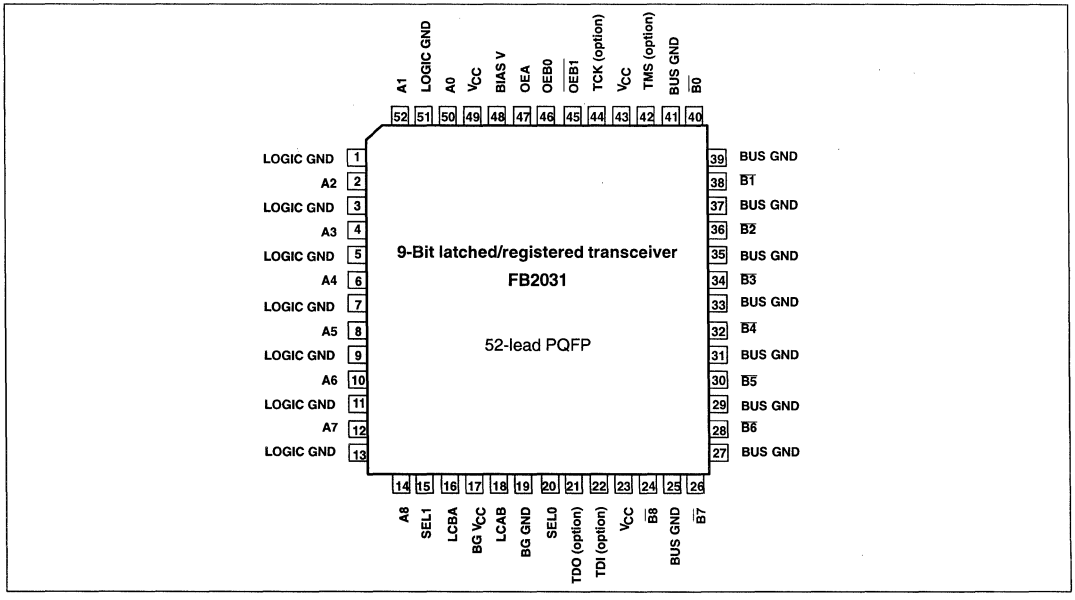
QUICK REFERENCE DATA

SYMBOL	PARAMETER		TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to $\overline{Bn}$		2.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{Bn}$ to An		4.4 4.2	ns
C_O	Output capacitance ($\overline{B0}$ – $\overline{Bn}$ only)		6	pF
I_{OL}	Output current ($\overline{B0}$ – $\overline{Bn}$ only)		100	mA
I_{CC}	Supply current	AIn to $\overline{Bn}$ (outputs Low or High)	17	mA
		$\overline{Bn}$ to AOn (outputs Low)	50	mA
		$\overline{Bn}$ to AOn (outputs High)	25	

ORDERING INFORMATION

PACKAGE	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10%; T_{amb} = –40°C to +85°C	DRAWING NUMBER
52-pin Plastic Quad Flat Pack (QFP)	FB2031BB	FB2031IBB	1418B

PIN CONFIGURATION



9-bit latched/registered/pass-thru Futurebus+ transceiver FB2031

DESCRIPTION

The FB2031 is a 9-bit latched/registered transceiver featuring a latched, registered or pass-thru mode in either the A-to-B or B-to-A direction. The FB2031 is intended to provide the electrical interface to a high performance wired-OR bus.

The TTL-level side (A port) has a common I/O. The common I/O, open collector B port operates at BTL signal levels. The logic element for data flow in each direction is controlled by two mode select inputs (SEL0 and SEL1). A "00" configures latches in both directions. A "10" configures thru mode in both directions. A "01" configures register mode in both directions. A "11" configures register mode in the A-to-B direction and latch mode in the B-to-A direction.

When configured in the buffer mode, the inverse of the input data appears at the output port. In the register mode, data is stored on the rising edge of the appropriate clock input (LCAB or LCBA). In the latch mode, clock pins serve as transparent-Low latch enables. Regardless of the mode, data is inverted from input to output.

The 3-State A port is enabled by asserting a High level on OEA. The B port has two output enables, OEB0 and $\overline{OEB1}$. Only when OEB0 is High and $\overline{OEB1}$ is Low is the output enabled.

When either OEB0 is Low or $\overline{OEB1}$ is High, the B port is inactive and is pulled to the level of the pullup voltage. New data can be entered in the register and latched modes or can be retained while the associated outputs are in 3-State (A port) or inactive (B port).

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The B-port interfaces to "Backplane Transceiver Logic" (see the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1V p-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

Output clamps are provided on the BTL outputs to further reduce switching noise. The "V_{OH}" clamp reduces inductive ringing effects during a Low-to-High transition. The "V_{OH}" clamp is always active. The other clamp, the "trapped reflection" clamp, clamps out ringing below the BTL 0.5V V_{OL} level. This clamp remains active for approximately 100ns after a High-to-Low transition.

To support live insertion, OEB0 is held Low during power on/off cycles to insure glitch-free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 5V level while V_{CC} is Low. The BIAS V pin is a low current input which will reverse-bias the BTL driver series Schottky diode, and also bias the B port output pins to a voltage between 1.62V and 2.1V. This bias function is in accordance with IEEE BTL Standard 1194.1. If live insertion is not a requirement, the BIAS V pin should be tied to a V_{CC} pin.

The LOGIC GND and BUS GND pins are isolated inside the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a "hard" signal failure occurs instead of a pattern dependent error that may be infrequent and impossible to troubleshoot.

As with any high power device, thermal considerations are critical. It is recommended that airflow (300lfpm) and/or thermal mounting be used to ensure proper junction temperature.

PACKAGE THERMAL CHARACTERISTICS

PARAMETER	CONDITION	52-PIN PLASTIC QFP
θja	Still air	80°C/W
θja	300 Linear feet per minute air flow	58°C/W
θjc	Thermally mounted on one side to heat sink	20°C/W

PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
A0 – A8	50, 52, 2, 4, 6, 8, 10, 12, 14	I/O	BiCMOS data inputs/3-State outputs (TTL)
$\overline{B0}$ – $\overline{B8}$	40, 38, 36, 34, 32, 30, 28, 26, 24	I/O	Data inputs/Open Collector outputs, High current drive (BTL)
OEB0	46	Input	Enables the B outputs when High
$\overline{OEB1}$	45	Input	Enables the B outputs when Low
OEA	47	Input	Enables the A outputs when High
BUS GND	25, 27, 29, 31, 33, 35, 37, 39, 41	GND	Bus ground (0V)
LOGIC GND	51, 1, 3, 5, 7, 9, 11, 13	GND	Logic ground (0V)
V_{CC}	23, 43, 49	Power	Positive supply voltage
BIAS V	48	Power	Live insertion pre-bias pin
BG V_{CC}	17	Power	Band Gap threshold voltage reference
BG GND	19	GND	Band Gap threshold voltage reference ground
SEL0	20	Input	Mode select
SEL1	15	Input	Mode select
LCAB	18	Input	A to B clock/latch enable (transparent latch when Low)
LCBA	16	Input	B to A clock/latch enable (transparent latch when Low)
TMS	42	Input	Test Mode Select (optional, if not implemented then no connect)
TCK	44	Input	Test Clock (optional, if not implemented then no connect)
TDI	22	Input	Test Data In (optional, if not implemented then no connect)
TDO	21	Output	Test Data Out (optional, if not implemented then shorted to TDI)

FUNCTION TABLE

MODE	INPUTS									OUTPUTS	
	An	$\overline{Bn}$*	OEB0	$\overline{OEB1}$	OEA	LCAB	LCBA	SEL0	SEL1	An	$\overline{Bn}$
An to $\overline{Bn}$ thru mode	L	—	H	L	L	X	X	H	L	input	H**
	H	—	H	L	L	X	X	H	L	input	L
An to $\overline{Bn}$ transparent latch	L	—	H	L	L	L	X	L	L	input	H**
	H	—	H	L	L	L	X	L	L	input	L
An to $\overline{Bn}$ latch and read	l	—	H	L	L	↑	X	L	L	input	H**
	h	—	H	L	L	↑	X	L	L	input	L
$\overline{Bn}$ outputs latched and read (preconditioned latch)	X	—	H	L	X	H	X	L	L	X	latched data
An to $\overline{Bn}$ register	l	—	H	L	L	↑	X	X	H	input	H**
	h	—	H	L	L	↑	X	X	H	input	L
$\overline{Bn}$ to An thru mode	—	L	Disable		H	X	X	H	L	H	input
	—	H	Disable		H	X	X	H	L	L	input
$\overline{Bn}$ to An transparent latch	—	L	Disable		H	X	L	L	L	H	input
	—	H	Disable		H	X	L	L	L	L	input
	—	L	Disable		H	X	L	H	H	H	input
	—	H	Disable		H	X	L	H	H	L	input
$\overline{Bn}$ to An latch and read	—	l	Disable		H	X	↑	L	L	H	input
	—	h	Disable		H	X	↑	L	L	L	input
	—	l	Disable		H	X	↑	H	H	H	input
	—	h	Disable		H	X	↑	H	H	L	input
An outputs latched and read (preconditioned latch)	—	X	X	X	H	X	H	L	L	latched data	X
	—	X	X	X	H	X	H	H	H	latched data	X
$\overline{Bn}$ to An register	—	l	Disable		H	X	↑	L	H	H	input
	—	h	Disable		H	X	↑	L	H	L	input
Disable $\overline{Bn}$ outputs	X	X	L	X	X	X	X	X	X	X	H**
	X	X	X	H	X	X	X	X	X	X	H**
Disable An outputs	X	X	X	X	L	X	X	X	X	Z	X

FUNCTION SELECT TABLE

MODE SELECTED	SEL0	SEL1
Thru mode	H	L
Register mode (An to Bn)	X	H
Latch mode (An to Bn)	L	L
Register mode (Bn to An)	L	H
Latch mode (Bn to An)	L	L
	H	H

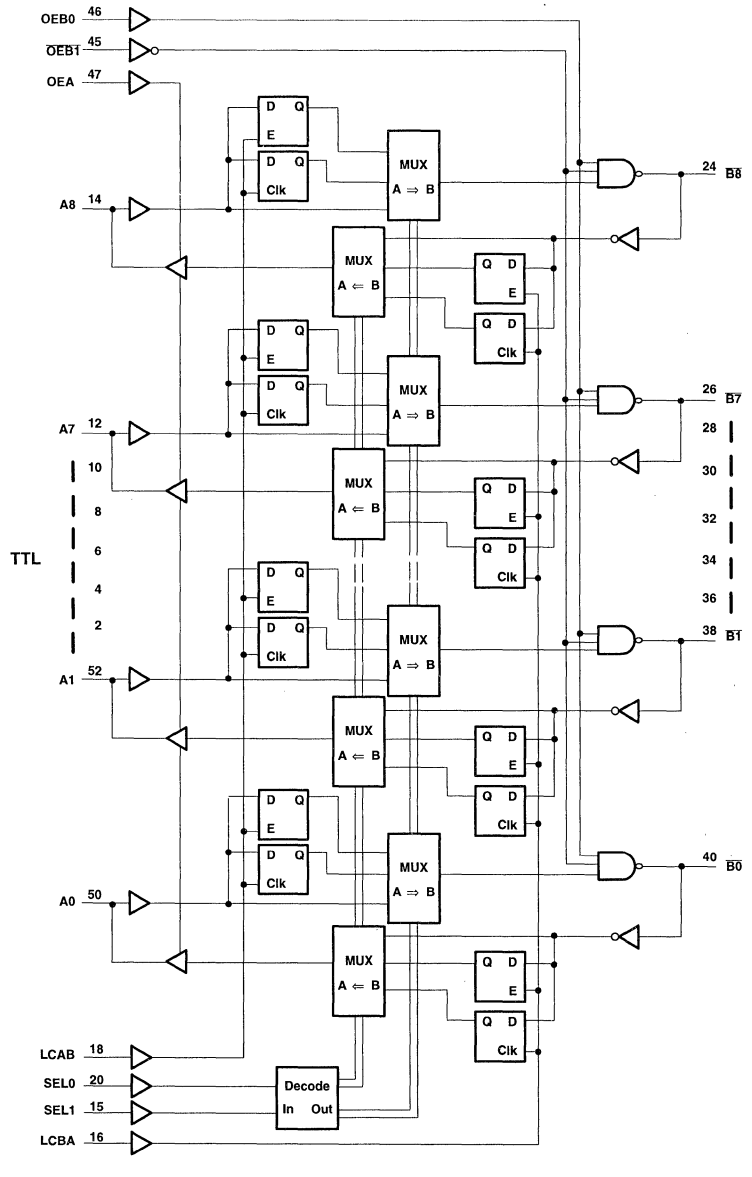
NOTES:

H = High voltage level
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High LCXX transition
h = High voltage level one set-up time prior to the Low-to-High LCXX transition

X = Don't care
Z = High-impedance (OFF) state
— = Input not externally driven
↑ = Low-to-High transition
H** = Goes to level of pull-up voltage

$\overline{Bn}$* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.
Disable = OEB0 is Low or $\overline{OEB1}$ is High.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage	All inputs except $\overline{B0} - \overline{B8}$	-1.2 to +7.0	V
		$\overline{B0} - \overline{B8}$	-1.2 to +3.5	
I_{IN}	Input current		-40 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A0 – A8	48	mA
		$\overline{B0} - \overline{B8}$	200	
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (Industrial)

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except $\overline{B0}$–$\overline{B8}$	2.0			V
		$\overline{B0} - \overline{B8}$	1.62	1.55		
V_{IL}	Low-level input voltage	Except $\overline{B0} - \overline{B8}$			0.8	V
		$\overline{B0} - \overline{B8}$			1.47	
I_{IK}	Input clamp current	Control inputs			-40	mA
		$\overline{B0} - \overline{B8}$ & A0 – A8			-18	
I_{OH}	High-level output current	A0 – A8			-3	mA
I_{OL}	Low-level output current	A0 – A8			24	mA
		$\overline{B0} - \overline{B8}$			100	
I_{IA}	Off device input current	Except $\overline{B0} - \overline{B8}$, V_I = 0 to 5.5V, V_{CC} = 0V			100	µA
C_{OB}	Output capacitance of B port			6	7	pF
T_{amb}	Operating free-air temperature range		–40		+85	°C

RECOMMENDED OPERATING CONDITIONS (Commercial)

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except $\overline{B0}$–$\overline{B8}$	2.0			V
		$\overline{B0} - \overline{B8}$	1.62	1.55		
V_{IL}	Low-level input voltage	Except $\overline{B0} - \overline{B8}$			0.8	V
		$\overline{B0} - \overline{B8}$			1.47	
I_{IK}	Input clamp current	Control inputs			-40	mA
		$\overline{B0} - \overline{B8}$ & A0 – A8			-18	
I_{OH}	High-level output current	A0 – A8			-3	mA
I_{OL}	Low-level output current	A0 – A8			24	mA
		$\overline{B0} - \overline{B8}$			100	
I_{IA}	Off device input current	Except $\overline{B0} - \overline{B8}$, V_I = 0 to 5.5V, V_{CC} = 0V			100	µA
C_{OB}	Output capacitance of B port			6	7	pF
T_{amb}	Operating free-air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS (Industrial)

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				MIN	TYP[2]	MAX	
I_{OH}	High level output current	$\overline{B0}$ – $\overline{B8}$	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 1.9V			100	µA
I_{OFF}	Power-off output current	$\overline{B0}$ – $\overline{B8}$	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 1.9V			200	µA
V_{OH}	High-level output voltage	A0 – A8 [4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = -24mA	2.0			V
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = -3mA	2.5	2.85		
V_{OL}	Low-level output voltage	A0 – A8 [4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 24mA			0.5	V
		$\overline{B0}$ – $\overline{B8}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 80mA	.75	1.0	1.1	
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 100mA			1.15	
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 80mA			1.15	
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 4mA	0.5			
V_{IK}	Input clamp voltage	Control pins	V_{CC} = MIN, I_I = I_{IK}			-0.5	V
		A0 – A8 $\overline{B0}$ – $\overline{Bn}$	V_{CC} = MIN, I_I = -18mA			-1.2	
I_I	Input current at maximum input voltage	Except $\overline{B0}$–$\overline{B8}$	V_{CC} = MAX, V_I = 0.5V or 5.5V			±50	µA
I_{IH}	High-level input current	Except $\overline{B0}$–$\overline{B8}$	V_{CC} = MAX, V_I = 2.7V			20	µA
		$\overline{B0}$ – $\overline{B8}$	V_{CC} = MAX, V_I = 1.9V			100	
			V_{CC} = MAX, V_I = 3.5V [5]	100			mA
I_{IL}	Low-level input current	Except $\overline{B0}$–$\overline{B8}$	V_{CC} = MAX, V_I = 0.5V			-20	µA
		$\overline{B0}$ – $\overline{B8}$	V_{CC} = MAX, V_I = 0.75V			-100	
I_{IH} + I_{OZH}	Off-state I/O High current	A0 – A8	V_{CC} = MAX, V_O = 2.7V			50	µA
I_{IL} + I_{OZL}	Off-state I/O Low current	A0 – A8	V_{CC} = MAX, V_O = 0.5V			-50	µA
I_{OS}	Short-circuit output current [3]	A0 – A8 only	V_{CC} = MAX, V_O = 0.0V	-45		-150	mA
I_{CC}	Supply current (total)	An to $\overline{Bn}$	V_{CC} = MAX, outputs Low or High		17	30	mA
		$\overline{Bn}$ to An	V_{CC} = MAX, outputs Low		50	78	
		$\overline{Bn}$ to An	V_{CC} = MAX, outputs High		25	45	
		I_{CCZ}	V_{CC} = MAX, outputs 3-State		28	50	
		Worst case	V_{CC} = MAX, all A and B outputs on		50	78	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are V_{IH} = 1.8V and V_{IL} = 1.3V for the B side.
5. For B port input voltage between 3 and 5 volts I_{IH} will be greater than 100µA, but the parts will continue to function normally.
6. $\overline{B0}$ – $\overline{B8}$ clamps remain active for a minimum of 80ns following a High-to-Low transition.
7. Temperature range: 0 to +85°C.
8. Temperature range: –40 to 0°C.

DC ELECTRICAL CHARACTERISTICS (Commercial)

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				MIN	TYP[2]	MAX	
I_{OH}	High level output current	$\overline{B0}$ – $\overline{B8}$	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 1.9V			100	µA
I_{OFF}	Power-off output current	$\overline{B0}$ – $\overline{B8}$	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 1.9V			100	µA
V_{OH}	High-level output voltage	A0 – A8 [4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = -24mA	2.0			V
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = -3mA	2.5	2.85		
V_{OL}	Low-level output voltage	A0 – A8 [4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 24mA			0.5	V
		$\overline{B0}$ – $\overline{B8}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 80mA	.75	1.0	1.1	
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 100mA			1.15	
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 4mA	0.5			
V_{IK}	Input clamp voltage	Control pins	V_{CC} = MIN, I_I = I_{IK}			-0.5	V
		A0 – A8 $\overline{B0}$ – $\overline{Bn}$	V_{CC} = MIN, I_I = -18mA			-1.2	
I_I	Input current at maximum input voltage	Except $\overline{B0}$–$\overline{B8}$	V_{CC} = MAX, V_I = 0.5V or 5.5V			±50	µA
I_{IH}	High-level input current	Except $\overline{B0}$–$\overline{B8}$	V_{CC} = MAX, V_I = 2.7V			20	µA
		$\overline{B0}$ – $\overline{B8}$	V_{CC} = MAX, V_I = 1.9V			100	
			V_{CC} = MAX, V_I = 3.5V [5]	100			mA
I_{IL}	Low-level input current	Except $\overline{B0}$–$\overline{B8}$	V_{CC} = MAX, V_I = 0.5V			-20	µA
		$\overline{B0}$ – $\overline{B8}$	V_{CC} = MAX, V_I = 0.75V			-100	
I_{IH} + I_{OZH}	Off-state I/O High current	A0 – A8	V_{CC} = MAX, V_O = 2.7V			50	µA
I_{IL} + I_{OZL}	Off-state I/O Low current	A0 – A8	V_{CC} = MAX, V_O = 0.5V			-50	µA
I_{OS}	Short-circuit output current [3]	A0 – A8 only	V_{CC} = MAX, V_O = 0.0V	-45		-150	mA
I_{CC}	Supply current (total)	An to $\overline{Bn}$	V_{CC} = MAX, outputs Low or High		17	30	mA
		$\overline{Bn}$ to An	V_{CC} = MAX, outputs Low		50	78	
		$\overline{Bn}$ to An	V_{CC} = MAX, outputs High		25	45	
		I_{CCZ}	V_{CC} = MAX, outputs 3-State		28	50	
		Worst case	V_{CC} = MAX, all A and B outputs on		50	78	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are V_{IH} = 1.8V and V_{IL} = 1.3V for the B side.
5. For B port input voltage between 3 and 5 volts I_{IH} will be greater than 100µA, but the parts will continue to function normally.
6. $\overline{B0}$ – $\overline{B8}$ clamps remain active for a minimum of 80ns following a High-to-Low transition.

LIVE INSERTION SPECIFICATIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{BIASV}	Bias pin voltage	V_{CC} = 0 to 5.25V, $\overline{Bn}$ = 0 to 2.0V	4.5		5.5	V
I_{BIASV}	Bias pin DC current	V_{CC} = 0 to 4.75V, $\overline{Bn}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V			1	mA
		V_{CC} = 4.5 to 5.5V, $\overline{Bn}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V			10	µA
$V_{\overline{Bn}}$	Bus voltage during prebias	$\overline{B0}$ – $\overline{B8}$ = 0V, Bias V = 5.0V	1.62		2.1	V
I_{LM}	Fall current during prebias	$\overline{B0}$ – $\overline{B8}$ = 2V, Bias V = 4.5 to 5.5V	1			µA
I_{HM}	Rise current during prebias	$\overline{B0}$ – $\overline{B8}$ = 1V, Bias V = 4.5 to 5.5V	-1			µA
$I_{\overline{Bn}PEAK}$	Peak bus current during insertion	V_{CC} = 0 to 5.25V, $\overline{B0}$ – $\overline{B8}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V, OEB0 = 0.8V, t_r = 2ns			10	mA
$I_{OL}OFF$	Power up current	V_{CC} = 0 to 5.25V, OEB0 = 0.8V			100	µA
		V_{CC} = 0 to 2.2V, OEB0 = 0 to 5V			100	
t_{GR}	Input glitch rejection	V_{CC} = 5.0V		1.35	1.0	ns

AC ELECTRICAL CHARACTERISTICS (Industrial)

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = –40 to +85°C, V_{CC} = 5V±10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 4	120	150		100		MHz
t_{PLH} t_{PHL}	Propagation delay (thru mode) $\overline{Bn}$ to An	Waveform 1, 2	2.5 2.4	4.4 4.2	5.9 5.5	2.3 2.4	7.0 6.2	ns
t_{PLH} t_{PHL}	Propagation delay (transparent latch) $\overline{Bn}$ to An	Waveform 1, 2	2.9 2.8	4.6 4.3	6.2 5.9	2.7 2.5	7.1 7.0	ns
t_{PLH} t_{PHL}	Propagation delay LCBA to An	Waveform 1, 2	2.6 2.4	4.1 4.7	5.5 6.1	2.0 2.0	6.2 6.8	ns
t_{PLH} t_{PHL}	Propagation delay SEL0 or SEL1 to An	Waveform 1, 2	1.5 1.7	3.8 3.9	5.2 6.0	1.2 1.5	6.2 6.5	ns
t_{PZH} t_{PZL}	Output enable time from High or Low OEA to An	Waveform 5, 6	2.1 2.0	3.5 3.8	4.8 5.3	1.8 1.7	6.0 6.3	ns
t_{PHZ} t_{PLZ}	Output disable time to High or Low OEA to An	Waveform 5, 6	1.9 1.7	3.4 3.2	4.8 4.8	1.6 1.5	5.5 5.5	ns
t_{TLH} t_{THL}	Output transition time, An Port 10% to 90%, 90% to 10%	Test Circuit and Waveforms				3.0 1.7	7.5 4.0	ns
$t_{SK(o)}$	Output to output skew for multiple channels[1]	Waveform 3		0.5	1.0		1.5	ns
$t_{SK(p)}$	Pulse skew [2] $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 2		0.5	1.0		1.0	ns

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are V_{IH} = 1.8V and V_{IL} = 1.3V for the B side.
5. For B port input voltage between 3 and 5 volts I_{IH} will be greater than 100µA, but the parts will continue to function normally.
6. $\overline{B0}$ – $\overline{B8}$ clamps remain active for a minimum of 80ns following a High-to-Low transition.

AC ELECTRICAL CHARACTERISTICS (Industrial)

SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 16.5Ω			T_{amb} = −40 to +85°C, V_{CC} = 5V±10%, C_D = 30pF, R_U = 16.5Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay (thru mode) An to $\overline{Bn}$	Waveform 1, 2	1.0 1.0	3.0 2.7	5.0 4.0	1.5 1.5	5.7 4.5	ns
t_{PLH} t_{PHL}	Propagation delay (transparent latch) An to $\overline{Bn}$	Waveform 1, 2	1.0 1.0	3.2 3.1	5.0 4.2	1.5 1.5	5.5 5.0	ns
t_{PLH} t_{PHL}	Propagation delay LCBA to $\overline{Bn}$	Waveform 1, 2	2.0 1.5	4.0 4.0	5.5 5.5	1.5 1.5	6.5 6.0	ns
t_{PLH} t_{PHL}	Propagation delay SEL0 or SEL1 to $\overline{Bn}$	Waveform 1, 2	2.0 1.5	3.5 2.3	5.5 4.5	2.0 1.0	6.1 5.5	ns
t_{PZH} t_{PZL}	Enable/disable time OEB0 or $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1, 2	1.5 1.2	3.0 2.4	5.0 4.5	1.0 1.0	5.7 5.5	ns
t_{TLH} t_{THL}	Output transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.0 0.6		2.0 3.0	0.9 0.6	3.0 3.0	ns
$t_{SK(o)}$	Output to output skew for multiple channels[1]	Waveform 3	1.0	0.4		1.6	1.6	ns
$t_{SK}(p)$	Pulse skew[2] $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 2		0.3	1.0		1.5	ns

NOTES:

1. $\lvert t_{PN}\text{actual} - t_{PM}\text{actual} \rvert$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).
2. $t_{SK}(p)$ is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle (50MHz input frequency and 50% duty cycle, tested on data paths only).

AC ELECTRICAL CHARACTERISTICS (Commercial)

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0 to +70°C, V_{CC} = 5V±10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 4	120	150		100		MHz
t_{PLH} t_{PHL}	Propagation delay (thru mode) $\overline{Bn}$ to An	Waveform 1, 2	2.5 2.4	4.4 4.2	5.9 5.5	2.3 2.4	6.6 5.9	ns
t_{PLH} t_{PHL}	Propagation delay (transparent latch) $\overline{Bn}$ to An	Waveform 1, 2	2.9 2.8	4.6 4.3	6.2 5.9	2.7 2.5	7.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay LCBA to An	Waveform 1, 2	2.6 2.4	4.1 4.7	5.5 6.1	2.0 2.0	6.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay SEL0 or SEL1 to An	Waveform 1, 2	1.5 1.7	3.8 3.9	5.2 6.0	1.2 1.5	6.0 6.5	ns
t_{PZH} t_{PZL}	Output enable time from High or Low OEA to An	Waveform 5, 6	2.1 2.0	3.5 3.8	4.8 5.3	1.8 1.7	5.8 6.0	ns
t_{PHZ} t_{PLZ}	Output disable time to High or Low OEA to An	Waveform 5, 6	1.9 1.7	3.4 3.2	4.8 4.8	1.6 1.5	5.4 5.4	ns
t_{TLH} t_{THL}	Output transition time, An Port 10% to 90%, 90% to 10%	Test Circuit and Waveforms				2.0 1.0	7.5 3.5	ns
$t_{SK(o)}$	Output to output skew for multiple channels[1]	Waveform 3		0.5	1.0		1.5	ns
$t_{SK(p)}$	Pulse skew [2] $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 2		0.5	1.0		1.0	ns

NOTES:

1. $\lvert t_{PN}\text{actual} - t_{PM}\text{actual} \rvert$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).
2. $t_{SK}(p)$ is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle (50MHz input frequency and 50% duty cycle, tested on data paths only).

AC ELECTRICAL CHARACTERISTICS (Commercial)

SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 16.5Ω			T_{amb} = 0 to +70°C, V_{CC} = 5V±10%, C_D = 30pF, R_U = 16.5Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay (thru mode) An to $\overline{Bn}$	Waveform 1, 2	1.0 1.0	3.0 2.7	5.0 4.0	1.0 0.5	5.5 4.5	ns
t_{PLH} t_{PHL}	Propagation delay (transparent latch) An to $\overline{Bn}$	Waveform 1, 2	1.0 1.0	3.2 3.1	5.0 4.2	1.0 0.8	5.5 4.5	ns
t_{PLH} t_{PHL}	Propagation delay LCBA to $\overline{Bn}$	Waveform 1, 2	2.0 1.5	4.0 4.0	5.5 5.5	1.5 1.0	6.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay SEL0 or SEL1 to $\overline{Bn}$	Waveform 1, 2	2.0 1.5	3.5 2.3	5.5 4.5	2.0 1.0	6.0 5.0	ns
t_{PZH} t_{PZL}	Enable/disable time OEB0 or $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1, 2	1.5 1.5	3.0 2.4	5.0 4.5	1.0 0.8	5.5 5.5	ns
t_{TLH} t_{THL}	Output transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.0 0.6		2.0 3.0	1.0 0.6	2.3 2.3	ns
$t_{SK(o)}$	Output to output skew for multiple channels[1]	Waveform 3		0.4	1.0		1.6	ns
$t_{SK(p)}$	Pulse skew[2] $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 2		0.3	1.0		1.5	ns

NOTES:
1. $\lvert t_{PN}actual - t_{PM}actual \rvert$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).
2. $t_{SK}(p)$ is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle (50MHz input frequency and 50% duty cycle, tested on data paths only).

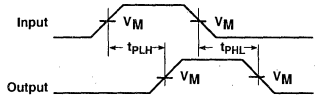
AC SETUP REQUIREMENTS (Industrial)

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V,			T_{amb} = –40 to +85°C, V_{CC} = 5V±10%,		
			C_L = 50pF (A side) / C_D = 30pF (B side) R_L = 500Ω (A side) / R_U = 16.5Ω (B side)					
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time An to LCAB	Waveform 4	1.0 1.0			1.5 1.0		ns
$t_h(H)$ $t_h(L)$	Hold time An to LCAB	Waveform 4	1.0 1.0			2.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{Bn}$ to LCBA	Waveform 4	2.0 2.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time $\overline{Bn}$ to LCBA	Waveform 4	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low LCAB or LCBA	Waveform 4	3.0 3.0			3.0 3.0		ns

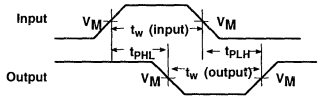
AC SETUP REQUIREMENTS (Commercial)

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF (A side) / C_D = 30pF (B side) R_L = 500Ω (A side) / R_U = 16.5Ω (B side)			T_{amb} = 0 to +70°C, V_{CC} = 5V±10%, C_L = 50pF (A side) / C_D = 30pF (B side) R_L = 500Ω (A side) / R_U = 16.5Ω (B side)		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time An to LCAB	Waveform 4	1.0 1.0			1.5 1.0		ns
t_h(H) t_h(L)	Hold time An to LCAB	Waveform 4	1.0 1.0			2.0 1.0		ns
t_s(H) t_s(L)	Setup time $\overline{Bn}$ to LCBA	Waveform 4	2.0 2.0			3.0 3.0		ns
t_h(H) t_h(L)	Hold time $\overline{Bn}$ to LCBA	Waveform 4	0.0 0.0			0.0 0.0		ns
t_w(H) t_w(L)	Pulse width, High or Low LCAB or LCBA	Waveform 4	3.0 3.0			3.0 3.0		ns

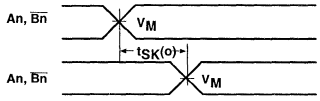
AC WAVEFORMS



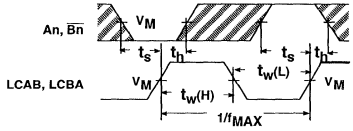
Waveform 1. Propagation Delay for Data or Output Enable to Output



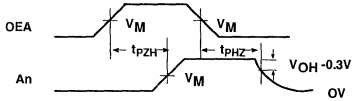
Waveform 2. Propagation Delay for Data or Output Enable to Output



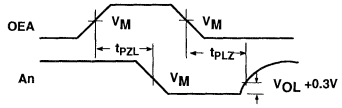
Waveform 3. Output to Output Skew



Waveform 4. Setup and Hold Times, Pulse Widths and Maximum Frequency



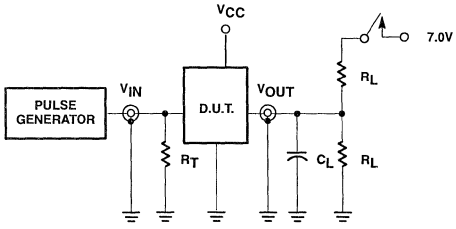
Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.
The shaded areas indicate when the input is permitted to change for predictable output performance.

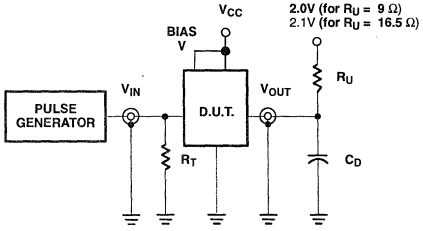
TEST CIRCUIT AND WAVEFORMS



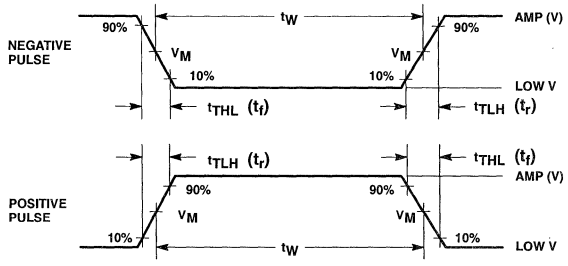
Test Circuit for 3-State Outputs on A Port

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test Circuit for Outputs on B Port



V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.

Input Pulse Definitions

Family FB+	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:
R_L = Load Resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_U = Pull up resistor; see AC CHARACTERISTICS for value.

8-bit latched/registered/pass-thru Futurebus+ universal interface transceiver

FB2033

FEATURES

- 8-bit transceivers
- Latched, registered or straight through in either A to B or B to A path
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω.
- High drive 100mA BTL Open Collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Each BTL driver has a dedicated Bus GND for a signal return
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch-free power up/power down operation
- Low I_{CC} current
- Tight output skew
- Supports live insertion

QUICK REFERENCE DATA

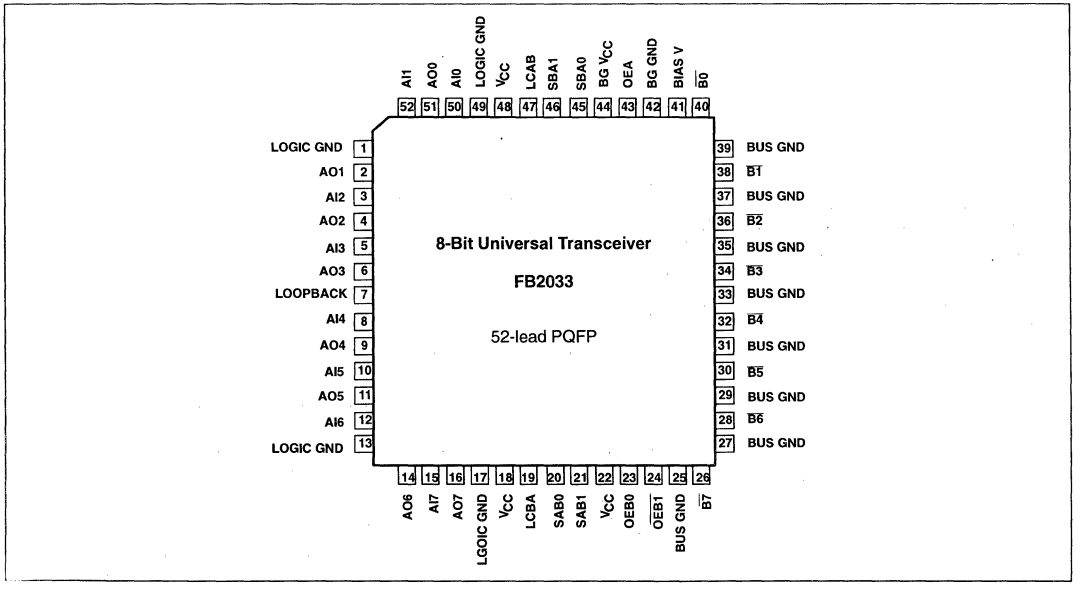
SYMBOL	PARAMETER		TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay AIn to $\overline{Bn}$		3.0 3.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{Bn}$ to AOn		4.3 4.1	ns
C_{OB}	Output capacitance ($\overline{B0}$ – $\overline{Bn}$ only)		6	pF
I_{OL}	Output current ($\overline{B0}$ – $\overline{Bn}$ only)		100	mA
I_{CC}	Supply current	AIn to $\overline{Bn}$ (outputs Low or High)	24	mA
		$\overline{Bn}$ to AOn (outputs Low)	45	
		$\overline{Bn}$ to AOn (outputs High)	22	

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0°C to +70°C	DRAWING NUMBER
52-pin Plastic Quad Flat Pack (QFP)	FB2033BB	1418B

NOTE: Thermal mounting or forced air is recommended

PIN CONFIGURATION



8-bit latched/registered/pass-thru Futurebus+ universal interface transceiver

FB2033

DESCRIPTION

The FB2033 is an 8-bit transceiver featuring a split input (AI) and output (AO) bus on the TTL-level side.

The common I/O, open collector B port operates at BTL signal levels. The logic element for data flow in each direction is controlled by two pairs of mode select inputs (SBA0 and SBA1 for B-to-A, SAB0 and SAB1 for A-to-B). It can be configured as a buffer, a register, or a D-type latch.

When configured in the buffer mode, the inverse of the input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock input (LCAB or LCBA). In the latch mode, clock pins serve as transparent-High latch enables. Regardless of the mode, data is inverted from input to output.

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the Loopback input. When the Loopback input is High the output of the selected A-to-B logic element (not inverted) becomes the B-to-A input.

The 3-State AO port is enabled by asserting a High level on OEA. The B port has two output enables, OEB0 and $\overline{OEB1}$. Only when OEB0 is High and $\overline{OEB1}$ is Low is the output enabled. When either OEB0 is Low or $\overline{OEB1}$ is High, the B-port is inactive and is pulled to the level of the pull-up voltage. New data can be entered in the flip-flop and latched modes or can be retained while the associated outputs are in 3-State (AO port) or inactive (B port).

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port ensure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The B-port interfaces to "Backplane Transceiver Logic" (see the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1V p-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

Output clamps are provided on the BTL outputs to further reduce switching noise. The "V_{OH}" clamp reduces inductive ringing effects during a Low-to-High transition. The "V_{OH}" clamp is always active. The other clamp, the "trapped reflection" clamp, clamps out ringing below the BTL 0.5V V_{OL} level. This clamp remains active for approximately 100ns after a High-to-Low transition.

To support live insertion, OEB0 is held Low during power on/off cycles to ensure glitch- free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 5V level while V_{CC} is Low. The BIAS V pin is a low current input which will reverse-bias the BTL driver series Schottky diode, and also bias the B port output pins to a voltage between 1.62V and 2.1V. This bias function is in accordance with IEEE BTL Standard 1194.1. If live insertion is not a requirement, the BIAS V pin should be tied to a V_{CC} pin.

The LOGIC GND and BUS GND pins are isolated inside the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a "hard" signal failure occurs instead of a pattern dependent error that may be very infrequent and impossible to trouble- shoot.

As with any high power device thermal considerations are critical. It is recommended that airflow (300lfpm) and/or thermal mounting be used to ensure proper junction temperature.

PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
AI0 – AI7	50, 52, 3, 5, 8, 10, 12, 15	Input	Data inputs (TTL)
AO0 – AO7	51, 2, 4, 6, 9, 11, 14, 16	Output	3-State outputs (TTL)
$\overline{B0}$ – $\overline{B7}$	40, 38, 36, 34, 32, 30, 28, 26	I/O	Data inputs/Open Collector outputs, High current drive (BTL)
OEB0	23	Input	Enables the B outputs when High
$\overline{OEB1}$	24	Input	Enables the B outputs when Low
OEA	43	Input	Enables the AO outputs when High
BUS GND	39, 37, 35, 33, 31, 29, 27, 25	GND	Bus ground (0V)
LOGIC GND	1, 13, 17, 49	GND	Logic ground (0V)
V_{CC}	18, 22, 48	Power	Positive supply voltage
BIAS V	41	Power	Live insertion pre-bias pin
BG V_{CC}	44	Power	Band Gap threshold voltage reference
BG GND	42	GND	Band Gap threshold voltage reference ground
SABn	20, 21	Input	Mode select from AI to $\overline{B}$
SBAn	45, 46	Input	Mode select from $\overline{B}$ to AO
LCAB	47	Input	A-to-B clock/latch enable (transparent latch when High)
LCBA	19	Input	B-to-A clock/latch enable (transparent latch when High)
Loopback	7	Input	Enables loopback function when High (from AIn to AOn)

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FUNCTION TABLE

MODE	INPUTS									OUTPUTS	
	AIn	$\overline{Bn}$*	OEB0	$\overline{OEB1}$	OEA	LCAB	LCBA	SAB_{1_0}	SBA_{1_0}	AOn	$\overline{Bn}$
AIn to $\overline{Bn}$ thru mode	L	—	H	L	L	X	X	LL	XX	Z	H**
	H	—	H	L	L	X	X	LL	XX	Z	L
AIn to $\overline{Bn}$ transparent latch	L	—	H	L	L	H	X	HX	XX	Z	H**
	H	—	H	L	L	H	X	HX	XX	Z	L
AIn to $\overline{Bn}$ latch and read	l	—	H	L	L	↓	X	HX	XX	Z	H**
	h	—	H	L	L	↓	X	HX	XX	Z	L
AIn to $\overline{Bn}$ register	L	—	H	L	L	↑	X	LH	XX	Z	H**
	H	—	H	L	L	↑	X	LH	XX	Z	L
$\overline{Bn}$ outputs latched and read (preconditioned latch)	X	—	H	L	L	L	X	HX	XX	Z	latched data
$\overline{Bn}$ to AOn thru mode	X	L	L	H	H	X	X	XX	LL	H	input
	X	H	L	H	H	X	X	XX	LL	L	input
$\overline{Bn}$ to AOn transparent latch	X	L	L	H	H	X	H	XX	HX	H	input
	X	H	L	H	H	X	H	XX	HX	L	input
$\overline{Bn}$ to AOn latch and read	X	l	L	H	H	X	↓	XX	HX	H	input
	X	h	L	H	H	X	↓	XX	HX	L	input
$\overline{Bn}$ to AOn register	X	L	L	H	H	X	↑	XX	LH	H	input
	X	H	L	H	H	X	↑	XX	LH	L	input
AOn outputs latched and read (preconditioned latch)	X	X	L	H	H	X	L	XX	HX	latched data	X
Disable $\overline{Bn}$ outputs	X	X	L	X	X	X	X	XX	XX	X	H**
	X	X	X	H	X	X	X	XX	XX	X	H**
Disable AOn outputs	X	X	X	X	L	X	X	XX	XX	Z	X

FUNCTION SELECT TABLE

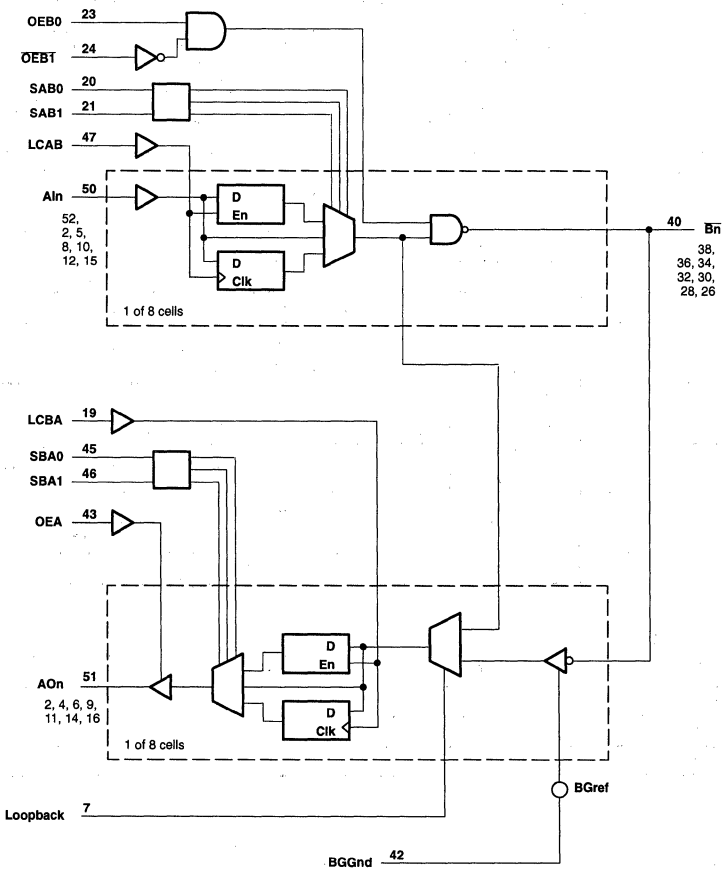
MODE SELECTED	SXX1	SXX0
Thru mode	L	L
Register mode	L	H
Latch mode	H	X

NOTES:

H = High voltage level
L = Low voltage level
h = High voltage level one set-up time prior to the High-to-Low LCXX transition
l = Low voltage level one set-up time prior to the High-to-Low LCXX transition
X = Don't care
Z = High-impedance (OFF) state
— = Input not externally driven
↑ = Low-to-High transition
↓ = High-to-Low transition
H** = Goes to level of pull-up voltage
$\overline{Bn}$* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.

NOTE: In Loopback mode (Loopback = High), AIn inputs are routed to the AOn outputs. The $\overline{Bn}$ inputs are blocked out.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage	All inputs except $\overline{B0} - \overline{Bn}$	-1.2 to +7.0	V
		$\overline{B0} - \overline{Bn}$	-1.2 to +3.5	
I_{IN}	Input current		-40 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	AO0 – AOn	48	mA
		$\overline{B0} - \overline{Bn}$	200	
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except $\overline{B0} - \overline{Bn}$	2.0			V
		$\overline{B0} - \overline{Bn}$	1.62	1.55		
V_{IL}	Low-level input voltage	Except $\overline{B0} - \overline{Bn}$			0.8	V
		$\overline{B0} - \overline{Bn}$			1.47	
I_{IK}	Input clamp current	Except $\overline{B0} - \overline{Bn}$			-40	mA
		$\overline{B0} - \overline{Bn}$			-50	
I_{OH}	High-level output current	AO0 – AOn			-3	mA
I_{OL}	Low-level output current	AO0 – AOn			24	mA
		$\overline{B0} - \overline{Bn}$			100	
I_{IA}	Off device input current	Except $\overline{B0} - \overline{Bn}$, V_I = 0 to 5.5V, V_{CC} = 0V			100	µA
C_{OB}	Output capacitance of B port			6	7	pF
T_{amb}	Operating free-air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				MIN	TYP[2]	MAX	
I_{OH}	High level output current	$\overline{B0} - \overline{Bn}$	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 1.9V			100	µA
I_{OFF}	Power-off output current	$\overline{B0} - \overline{Bn}$	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 1.9V			100	µA
V_{OH}	High-level output voltage	AO0 – AOn [4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = -3mA	2.5	2.85		V
V_{OL}	Low-level output voltage	AO0 – AOn [4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 24mA			0.5	V
		$\overline{B0} - \overline{Bn}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 100mA	.75	1.0	1.15	
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 4mA	0.5			
V_{IK}	Input clamp voltage	Except $\overline{B0}$–$\overline{Bn}$	V_{CC} = MIN, I_I = I_{IK}			-0.5	V
		$\overline{B0} - \overline{Bn}$	V_{CC} = MIN, I_I = I_{IK} [6]	0.3			
			V_{CC} = MIN, I_I = -18mA			-1.2	
I_I	Input current at maximum input voltage	Except $\overline{B0}$–$\overline{Bn}$	V_{CC} = MAX, V_I = 0.5V or 5.5V			±50	µA
I_{IH}	High-level input current	Except $\overline{B0}$–$\overline{Bn}$	V_{CC} = MAX, V_I = 2.7V, $\overline{Bn}$ = AIn = 0V			20	µA
		$\overline{B0} - \overline{Bn}$	V_{CC} = MAX, V_I = 1.9V			100	
			V_{CC} = MAX, V_I = 3.5V [5]	100			mA
I_{IL}	Low-level input current	Except $\overline{B0}$–$\overline{Bn}$	V_{CC} = MAX, V_I = 0.5V			-20	µA
		$\overline{B0} - \overline{Bn}$	V_{CC} = MAX, V_I = 0.75V			-100	
I_{OZH}	Off-state output current	AO0 – AOn	V_{CC} = MAX, V_O = 2.7V			50	µA
I_{OZL}	Off-state output current	AO0 – AOn	V_{CC} = MAX, V_O = 0.5V			-50	µA
I_{OS}	Short-circuit output current [3]	AO0 – AOn only	V_{CC} = MAX, V_O = 0.0V	-45		-150	mA
I_{CC}	Supply current (total)	AIn to $\overline{Bn}$	V_{CC} = MAX, outputs Low or High		24	50	mA
		$\overline{Bn}$ to AOn	V_{CC} = MAX, outputs Low		45	75	
		$\overline{Bn}$ to AOn	V_{CC} = MAX, outputs High		22	44	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are V_{IH} = 1.8V and V_{IL} = 1.3V for the B side.
5. For B port input voltage between 3 and 5 volts I_{IH} will be greater than 100µA, but the parts will continue to function normally.
6. $\overline{B0} - \overline{B7}$ clamps remain active for a minimum of 80ns following a High-to-Low transition.

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LIVE INSERTION SPECIFICATIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{BIASV}	Bias pin voltage	V_{CC} = 0 to 5.25V, $\overline{Bn}$ = 0 to 2.0V	4.5		5.5	V
I_{BIASV}	Bias pin DC current	V_{CC} = 0 to 4.75V, $\overline{Bn}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V			1	mA
		V_{CC} = 4.5 to 5.5V, $\overline{Bn}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V			10	µA
$V_{\overline{Bn}}$	Bus voltage during pre-bias	$\overline{B0}$ – $\overline{B8}$ = 0V, Bias V = 5.0V	1.62		2.1	V
I_{LM}	Fall current during pre-bias	$\overline{B0}$ – $\overline{B8}$ = 2V, Bias V = 4.5 to 5.5V	1			µA
I_{HM}	Rise current during pre-bias	$\overline{B0}$ – $\overline{B8}$ = 1V, Bias V = 4.5 to 5.5V	-1			µA
$I_{\overline{Bn}PEAK}$	Peak bus current during insertion	V_{CC} = 0 to 5.25V, $\overline{B0}$ – $\overline{B8}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V, OEB0 = 0.8V, t_r = 2ns			10	mA
$I_{OL}OFF$	Power up current	V_{CC} = 0 to 5.25V, OEB0 = 0.8V			100	µA
		V_{CC} = 0 to 2.2V, OEB0 = 0 to 5V			100	
t_{GR}	Input glitch rejection	V_{CC} = 5.0V	1.0	1.35		ns

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0 to 70°C, V_{CC} = 5V±10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 4	100	150		100		MHz
t_{PLH} t_{PHL}	Propagation delay (thru mode) $\overline{Bn}$ to AOn	Waveform 1, 2	2.2 2.0	4.3 4.1	6.0 6.0	2.0 1.8	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay (transparent latch) $\overline{Bn}$ to AOn	Waveform 1, 2	1.5 2.4	4.5 4.4	6.5 6.5	1.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay LCBA to AOn	Waveform 1, 2	2.0 2.2	3.8 4.3	5.5 6.0	1.8 1.7	6.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay SBAn to AOn	Waveform 1, 2	1.4 1.4	2.9 3.1	5.0 5.5	1.0 1.0	6.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay (Loopback mode) AIn to AOn	Waveform 1, 2	2.0 2.0	3.8 3.9	6.0 6.0	2.8 2.3	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay (Loopback mode) Loopback to AOn	Waveform 1, 2	1.2 1.2	3.4 3.2	5.0 5.5	1.0 1.0	6.0 6.5	ns
t_{PZH} t_{PZL}	Output enable time from High or Low OEA to AOn	Waveform 5, 6	1.0 2.6	3.1 4.0	5.1 5.5	1.0 2.4	5.5 5.8	ns
t_{PHZ} t_{PLZ}	Output disable time to High or Low OEA to AOn	Waveform 5, 6	1.0 1.0	3.5 3.3	5.0 4.6	1.7 1.7	5.6 5.2	ns
t_{TLH} t_{THL}	Output transition time, AOn Port 10% to 90%, 90% to 10%	Test Circuit and Waveforms				2.0 2.0	5.0 5.0	ns
$t_{SK(o)}$	Output to output skew, A port [1]	Waveform 3		0.5	1.0		1.5	ns
$t_{SK(p)}$	Pulse skew [2] $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 2		0.3	1.0		1.5	ns

NOTES:
1. $\overline{Bn}$ to AOn propagation delays are extended for 5 nanoseconds following B port excursions above 3.1 volts.
2. $\lvert t_{PN}actual - t_{PM}actual \rvert$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).
3. $t_{SK}(p)$ is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle (50MHz input frequency and 50% duty cycle, tested on data paths only).

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 9Ω			T_{amb} = 0 to 70°C, V_{CC} = 5V±10%, C_D = 30pF, R_U = 9Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay (thru mode) AIn to $\overline{Bn}$	Waveform 1, 2	1.2 1.0	2.9 2.9	4.3 4.4	1.0 1.0	4.8 4.6	ns
t_{PLH} t_{PHL}	Propagation delay (transparent latch) AIn to $\overline{Bn}$	Waveform 1, 2	1.4 1.0	3.1 3.3	4.5 4.8	1.0 1.0	5.1 5.1	ns
t_{PLH} t_{PHL}	Propagation delay LCAB to $\overline{Bn}$	Waveform 1, 2	2.7 2.2	4.4 5.1	5.7 6.6	2.4 2.0	6.4 7.1	ns
t_{PLH} t_{PHL}	Propagation delay SABn to $\overline{Bn}$	Waveform 1, 2	1.8 1.0	3.6 3.3	5.0 4.9	1.4 1.0	5.7 5.2	ns
t_{PZH} t_{PZL}	Enable/disable time OEB0 or $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1, 2	1.4 1.0	3.0 3.1	4.5 5.0	1.0 1.0	5.0 5.6	ns
$\Delta V/\Delta t$	Output transition rate, $\overline{Bn}$ Port 20% to 80%, 80% to 20%	Test Circuit and Waveforms				0.4	1.2	V/ns
$t_{SK}(o)$	Output to output skew, B port [1]	Waveform 3		0.8	1.5		2.0	ns
$t_{SK}(p)$	Pulse skew [2] $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 2		0.3	1.5			ns
SYMBOL	**PARAMETER**	**TEST CONDITION**	**R_U = 16.5Ω**			**R_U = 16.5Ω**		**UNIT**
t_{PLH} t_{PHL}	Propagation delay (thru mode) AIn to $\overline{Bn}$	Waveform 1, 2	1.2 1.0	3.0 3.0	4.4 4.5	1.0 1.0	4.9 4.7	ns
t_{PLH} t_{PHL}	Propagation delay (transparent latch) AIn to $\overline{Bn}$	Waveform 1, 2	1.4 1.0	3.2 3.4	4.6 4.9	1.0 1.0	5.2 5.2	ns
t_{PLH} t_{PHL}	Propagation delay LCAB to $\overline{Bn}$	Waveform 1, 2	2.7 2.2	4.5 5.2	5.8 6.7	2.4 2.0	6.5 7.2	ns
t_{PLH} t_{PHL}	Propagation delay SABn to $\overline{Bn}$	Waveform 1, 2	1.8 1.0	3.7 3.4	5.1 5.0	1.4 1.0	5.8 5.3	ns
t_{PZH} t_{PZL}	Enable/disable time OEB0 or $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1, 2	1.4 1.0	3.1 3.2	4.6 5.1	1.0 1.0	5.1 5.7	ns
$\Delta V/\Delta t$	Output transition rate, $\overline{Bn}$ Port 20% to 80%, 80% to 20%	Test Circuit and Waveforms				0.2	0.6	V/ns
$t_{SK}(o)$	Output to output skew, B port [1]	Waveform 3		0.5	1.0		1.5	ns
$t_{SK}(p)$	Pulse skew [2] $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 2		0.3	1.0		1.5	ns

NOTES:

1. $\lvert t_{PN}\text{actual} - t_{PM}\text{actual} \rvert$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).
2. $t_{SK}(p)$ is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle (50MHz input frequency and 50% duty cycle, tested on data paths only).

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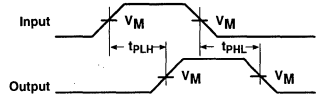
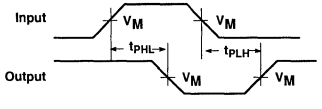
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V			T_{amb} = 0 to 70°C, V_{CC} = 5V±10%		
			C_L = 50pF (A side) / C_D = 30pF (B side) R_L = 500Ω (A side) / R_U = 9Ω (B side)					
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time AIn to LCAB or $\overline{Bn}$ to LCBA	Waveform 4	3.0 3.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time AIn to LCAB or $\overline{Bn}$ to LCBA	Waveform 4	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low LCAB or LCBA	Waveform 4	3.0 3.0			4.0 4.0		ns
SYMBOL	PARAMETER	TEST CONDITION	C_L = 50pF (A side) / C_D = 30pF (B side) R_L = 500Ω (A side) / R_U = 16.5Ω (B side)					UNIT
$t_s(H)$ $t_s(L)$	Setup time AIn to LCAB or $\overline{Bn}$ to LCBA	Waveform 4	3.0 3.0			4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time AIn to LCAB or $\overline{Bn}$ to LCBA	Waveform 4	0.0 0.0			0.0 0.0		ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low LCAB or LCBA	Waveform 4	3.0 3.0			4.0 4.0		ns

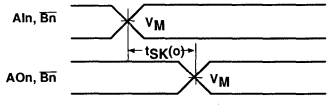
AC WAVEFORMS



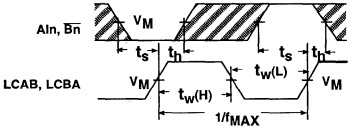
Waveform 7. Propagation Delay for Data or Output Enable to Output



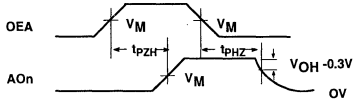
Waveform 8. Propagation Delay for Data or Output Enable to Output



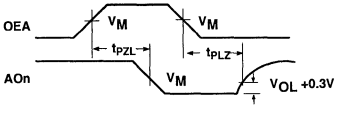
Waveform 9. Output to Output Skew



Waveform 10. Setup and Hold Times, Pulse Widths and Maximum Frequency



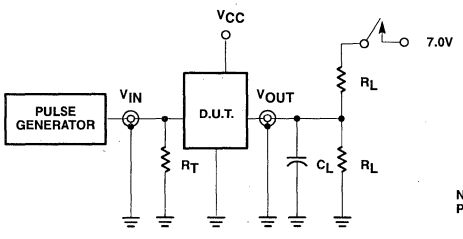
Waveform 11. 3-State Output Enable Time to High Level and Output Disable Time from High Level



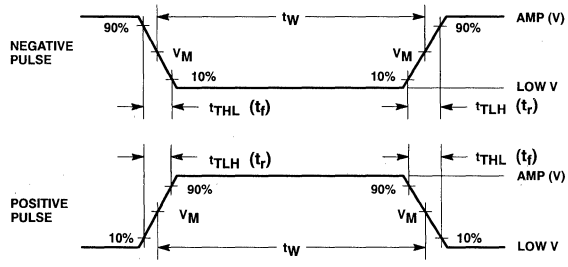
Waveform 12. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs on A Port

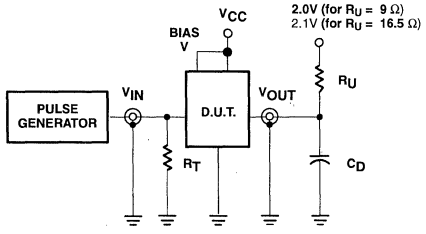


V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.

Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test Circuit for Outputs on B Port

Family FB+	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load Resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_U = Pull up resistor; see AC CHARACTERISTICS for value.

8-bit Futurebus+ transceiver — FB2040A

FEATURES

- 8-bit BTL transceivers
- Separate I/O on TTL A-port
- Inverting
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω.
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Controlled output ramp and multiple GND pins minimize ground bounce
- Each BTL driver has a dedicated Bus GND for a signal return
- Glitch-free power up/power down operation
- Low I_{CC} current
- Tight output skew
- Supports live insertion
- Pins for the optional JTAG boundary scan function are provided
- High density packaging in plastic Quad Flat Pack

QUICK REFERENCE DATA

SYMBOL	PARAMETER		TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay AIn to $\overline{Bn}$		4.4 3.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{Bn}$ to AOn		3.4 3.2	ns
C_{OB}	Output capacitance ($\overline{B0}$ – $\overline{B7}$ only)		4	pF
I_{OL}	Output current ($\overline{B0}$ – $\overline{B7}$ only)		100	mA
I_{CC}	Supply current	Standby	4	mA
		AIn to $\overline{Bn}$ (outputs Low or High)	4	
		$\overline{Bn}$ to AOn (outputs Low)	22	
		$\overline{Bn}$ to AOn (outputs High)	12	

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0°C to +70°C	DRAWING NUMBER
52-pin Plastic Quad Flat Pack (QFP)	FB2040BB	1418B

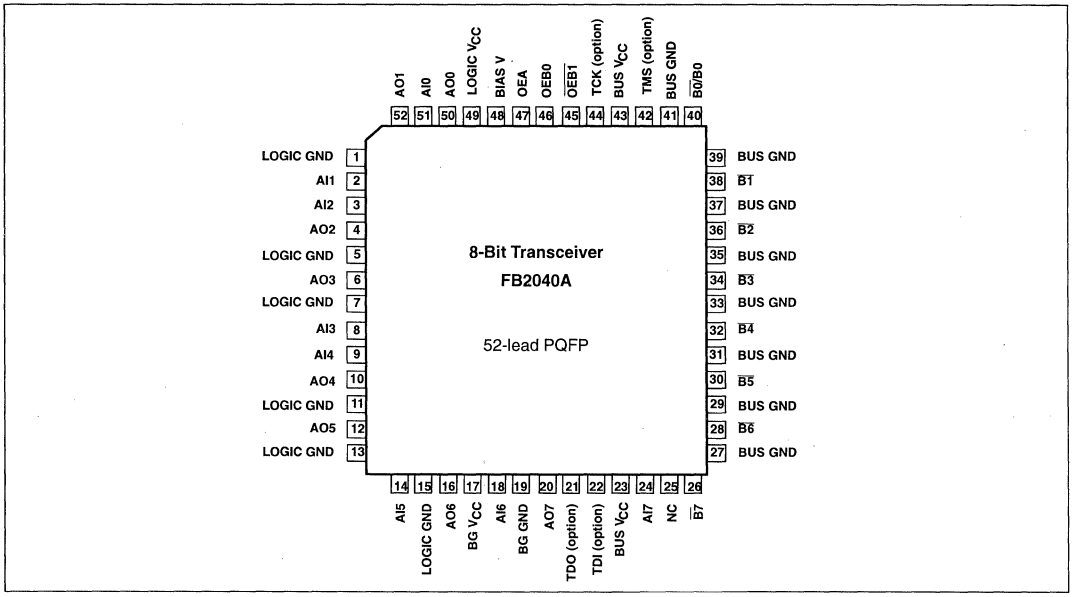
ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage	AI0 – AI7, OEB0, $\overline{OEB1}$, OEA	-1.2 to +7.0	V
		$\overline{B0}$ – $\overline{B7}$	-1.2 to +5.5	
I_{IN}	Input current		-18 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A0 – A7	48	mA
		$\overline{B0}$ – $\overline{B7}$	200	
T_{amb}	Operating free-air temperature range		-40 to ++85	°C
T_{STG}	Storage temperature		-65 to +150	°C

8-bit Futurebus+ transceiver FB2040A

PIN CONFIGURATION



DESCRIPTION

The FB2040A is an 8-bit bidirectional BTL transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. The FB2040A is an inverting transceiver.

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The B-port interfaces to "Backplane Transceiver Logic" (See the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1Vp-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

The A-port operates at TTL levels with separate I/O. The 3-state A-port drivers are enabled when OEA goes High after an extra 6ns delay which is built in to provide a break-before-make function. When OEA goes Low, A-port drivers become High impedance without any extra delay. During power on/off cycles, the A-port drivers are held in a High impedance state when V_{CC} is below 2.5V.

The B-port has two output enables, OEB0 and $\overline{OEB1}$. When OEB0 is High and $\overline{OEB1}$ is Low the output is enabled. When OEB0 is Low or if $\overline{OEB1}$ is High, the B-port is inactive and is at the level of the backplane signal.

To support live insertion, OEB0 is held Low during power on/off cycles to insure glitch free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 5V level while V_{CC} is Low. If live insertion is not a requirement, the BIAS V pin should be tied to a V_{CC} pin.

The LOGIC GND and BUS GND pins are isolated in the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a "hard" signal failure occurs instead of a pattern dependent error that may be very infrequent and impossible to trouble-shoot.

The LOGIC V_{CC} and BUS V_{CC} pins are also isolated internally to minimize noise and may be externally decoupled separately or simply tied together.

JTAG boundary scan pins are provided with signals TMS, TCK, TDI and TDO. TMS and TCK are no-connects (no bond wires) and TDI and TDO are shorted together internally. Boundary scan functionality is not implemented at this time.

PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
AI0 – AI7	51, 2, 3, 8, 9, 14, 18, 24	Input	Data inputs (TTL)
AO0 – AO7	50, 52, 4, 6, 10, 12, 16, 20	Output	3-state outputs (TTL)
$\overline{B0}$ – $\overline{B7}$	40, 38, 36, 34, 32, 30, 28, 26	I/O	Data inputs/Open Collector outputs. High current drive (BTL)
OEB0	46	Input	Enables the B outputs when High
$\overline{OEB1}$	45	Input	Enables the B outputs when Low
OEA	47	Input	Enables the A outputs when High
BUS GND	41, 39, 37, 35, 33, 31, 29, 27	GND	Bus ground (0V)
LOGIC GND	1, 5, 7, 11, 13, 15	GND	Logic ground (0V)
BUS V_{CC}	23, 43	Power	Positive supply voltage
LOGIC V_{CC}	49	Power	Positive supply voltage
BG V_{CC}	17	Power	Band Gap threshold voltage reference
BG GND	19	GND	Band Gap threshold voltage reference ground
BIAS V	48	Power	Live insertion pre-bias pin
TMS	42	Input	Test Mode Select (optional, if not implemented then no-connect)
TCK	44	Input	Test Clock (optional, if not implemented then no-connect)
TDI	22	Input	Test Data In (optional, if not implemented then shorted to TDO)
TDO	21	Output	Test Data Out (optional, if not implemented then shorted to TDI)
NC	25	NC	No Connect

FUNCTION TABLE

MODE	INPUTS					OUTPUTS	
	AIn	$\overline{Bn}$*	OEB0	$\overline{OEB1}$	OEA	AOn	$\overline{Bn}$*
AIn to $\overline{Bn}$	L	—	H	L	L	Z	H**
	H	—	H	L	L	Z	L
	L	—	H	L	H	L	H**
	H	—	H	L	H	H	L
Disable $\overline{Bn}$ outputs	X	X	L	X	X	X	H**
	X	X	X	H	X	X	H**
$\overline{Bn}$ to AOn	X	L	L	X	H	H	Input
	X	H	X	H	H	L	Input
	X	L	X	H	H	H	Input
	X	H	L	X	H	L	Input
Disable AOn outputs	—	X	X	X	L	Z	X

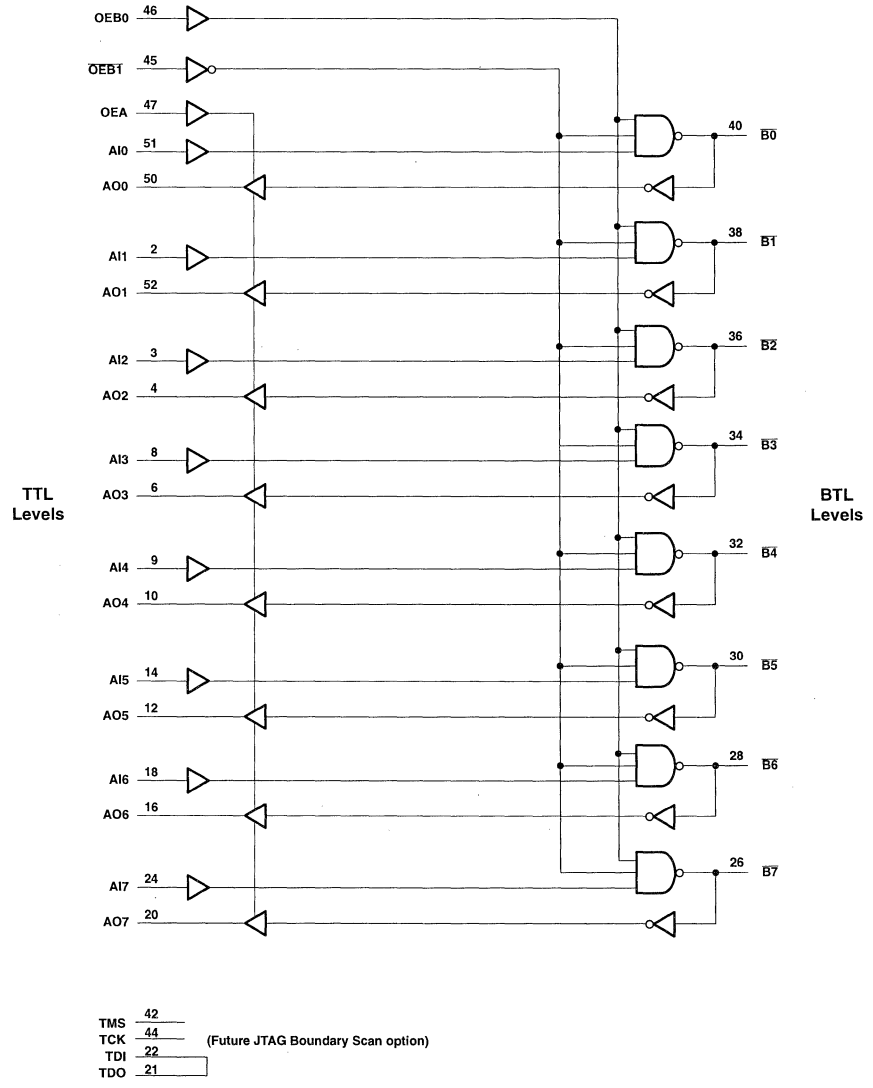
H** = Goes to level of pull-up voltage

B* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except $\overline{B0}$–$\overline{B7}$	2.0			V
		$\overline{B0}$ – $\overline{B7}$	1.62	1.55		
V_{IL}	Low-level input voltage	Except $\overline{B0}$–$\overline{B7}$			0.8	V
		$\overline{B0}$ – $\overline{B7}$			1.47	
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	AO0 – AO7			-3	mA
I_{OL}	Low-level output current	AO0 – AO7			24	mA
		$\overline{B0}$ – $\overline{B7}$			100	
C_{OB}	Output capacitance on B port				5	pF
T_{amb}	Operating free-air temperature range		0		+70	°C

LOGIC DIAGRAM FOR FB2040



NC = 25
LOGIC V_{CC} = 49
LOGIC GND = 1, 5, 7, 11, 13, 15
BUS V_{CC} = 23, 24
BUS GND = 27, 29, 31, 33, 35, 37, 39, 41
BIAS V = 48
BG V_{CC} = 17
BG GND = 19

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				MIN	TYP[2]	MAX	
I_{OH}	High level output current	$\overline{B0}$ – $\overline{B7}$	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V			100	µA
I_{OFF}	Power-off output current	$\overline{B0}$ – $\overline{B7}$	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V			100	µA
V_{OH}	High-level output voltage	AO0 – AO7[3]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = -3mA	2.5	2.85		V
V_{OL}	Low-level output voltage	AO0 – AO7[3]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 24mA		0.33	0.5	V
		$\overline{B0}$ – $\overline{B7}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 80mA	.75	1.0	1.10	
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 100mA			1.15	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-1.2	V
I_I	Input current at maximum input voltage	OEB0, $\overline{OEB1}$, OEA, AI0–AI7	V_{CC} = MAX, V_I = GND or 5.5V			±50	µA
I_{IH}	High-level input current	OEB0, $\overline{OEB1}$, OEA, AI0–AI7	V_{CC} = MAX, V_I = 2.7V			20	µA
		$\overline{B0}$ – $\overline{B7}$	V_{CC} = MAX, V_I = 2.1V			100	
I_{IL}	Low-level input current	OEB0, $\overline{OEB1}$, OEA, AI0–AI7	V_{CC} = MAX, V_I = 0.5V			-20	µA
		$\overline{B0}$ – $\overline{B7}$	V_{CC} = MAX, V_I = 0.75V			-100	
I_{OZH}	Off-state output current	AO0 – AO7	V_{CC} = MAX, V_O = 2.7V			50	µA
I_{OZL}	Off-state output current	AO0 – AO7	V_{CC} = MAX, V_O = 0.5V			-50	µA
I_{OS}	Short-circuit output current[4]	AO0 – AO7 only	V_{CC} = MAX, V_O = 0.0V	-30		-150	mA
I_{CC}	Supply current (total)	I_{CCZ} (standby)	V_{CC} = MAX		19	30	mA
		I_{CCB}, AIn to $\overline{Bn}$	V_{CC} = MAX, outputs Low or High		40	60	
		I_{CCA}, $\overline{Bn}$ to AOn	V_{CC} = MAX, outputs Low		22	35	
		I_{CCA}, $\overline{Bn}$ to AOn	V_{CC} = MAX, outputs High		19	35	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Due to test equipment limitations, actual test conditions are V_{IH} = 1.8V and V_{IL} = 1.3V for the B side.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

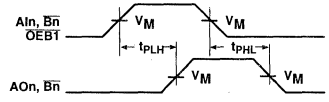
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0 to 70°C, V_{CC} = 5V±10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay, $\overline{Bn}$ to AOn	Waveform 1, 2	1.8 1.6	3.4 3.2	5.0 4.9	1.6 1.6	5.6 5.3	ns
t_{PZH} t_{PZL}	Output enable time, OEA to AOn	Waveform 5, 6	1.0 1.0		5.0 5.0	1.5 1.5	5.5 5.5	ns
t_{PHZ} t_{PLZ}	Output disable time, OEA to AOn	Waveform 5, 6	1.5 1.5	3.3 3.3	4.8 5.4	1.2 1.3	5.0 5.9	ns
t_{TLH} t_{THL}	Transition time, AOn Port (10% to 90% or 90% to 10%)	Test Circuit and Waveforms	1.5 1.5	2.2 2.4	3.5 3.5	1.0 1.0	4.5 4.5	ns
$t_{SK(o)}$	Output skew between receivers in same package[1]	Waveform 3		0.4	1.0		1.0	ns
SYMBOL	**PARAMETER**	**TEST CONDITION**	**B PORT LIMITS**					**UNIT**
			T_{amb} = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 9Ω			T_{amb} = 0 to 70°C, V_{CC} = 5V±10%, C_D = 30pF, R_U = 9Ω		
t_{PLH} t_{PHL}	Propagation delay, AIn to $\overline{Bn}$	Waveform 1, 2	2.9 1.6	4.4 3.3	5.0 4.8	2.3 1.5	5.5 5.1	ns
t_{PLH} t_{PHL}	Enable/disable time, OEB0 to $\overline{Bn}$	Waveform 2	2.9 1.9	4.7 3.5	5.9 5.1	2.6 1.8	7.8 5.7	ns
t_{PLH} t_{PHL}	Enable/disable time, $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1	3.0 1.7	5.3 3.2	6.3 4.8	2.7 1.5	8.0 5.7	ns
t_{TLH} t_{THL}	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.0 0.5	1.4 1.1	3.0 3.0	1.0 0.5	3.0 3.0	ns
$t_{SK(o)}$	Output skew between drivers in same package[1]	Waveform 3		0.3	1.0		1.0	ns
SYMBOL	**PARAMETER**	**TEST CONDITION**	**R_U = 16.5Ω**			**R_U = 16.5Ω**		**UNIT**
t_{PLH} t_{PHL}	Propagation delay, AIn to $\overline{Bn}$	Waveform 1, 2	3.0 1.7	4.5 3.3	6.4 4.8	2.3 1.6	6.9 5.1	ns
t_{PLH} t_{PHL}	Enable/disable time, OEB0 to $\overline{Bn}$	Waveform 2	3.0 2.0	4.8 3.5	6.0 5.2	2.7 1.9	7.9 5.7	ns
t_{PLH} t_{PHL}	Enable/disable time, $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1	3.1 1.8	5.4 3.3	6.4 4.9	2.8 1.6	8.1 5.7	ns
t_{TLH} t_{THL}	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.0 0.5	1.5 1.1	3.0 3.0	1.0 0.5	3.0 3.0	ns
$t_{SK(o)}$	Output skew between drivers in same package[1]	Waveform 3		0.3	1.0		1.0	ns

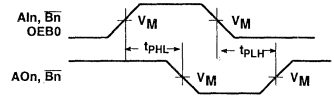
NOTES:

1. $|t_{PN}actual - t_{PM}actual|$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).

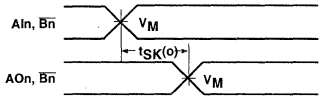
AC WAVEFORMS



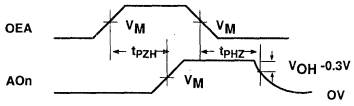
Waveform 13. Propagation Delay for Data or Output Enable to Output



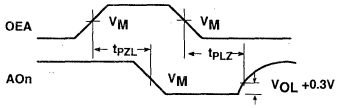
Waveform 14. Propagation Delay for Data or Output Enable to Output



Waveform 15. Output Skews



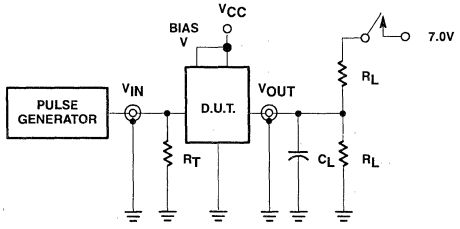
Waveform 16. 3-State Output Enable Time to High Level and Output Disable Time from High Level



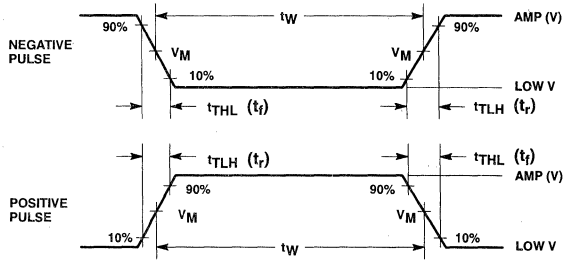
Waveform 17. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs on A Port

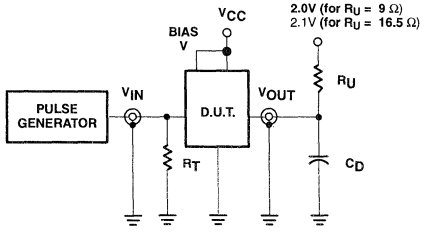


V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.

Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL} All other	closed open



Test Circuit for Outputs on B Port

Family FB+	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_U = Pull up resistor; see AC CHARACTERISTICS for value.

7-bit Futurebus+ transceiver — FB2041

DESCRIPTION

The FB2041 is a 7-bit bidirectional BTL transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. The FB2041 is an inverting transceiver.

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

FEATURES

- 7-bit BTL transceiver
- Separate I/O on TTL A-port
- Inverting
- Three separate pairs of driver enables in a 1 bit, 3 bit, 3 bit arrangement
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω.
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Controlled output ramp and multiple GND pins minimize ground bounce
- Each BTL driver has a dedicated Bus GND for a signal return
- Glitch-free power up/power down operation
- Low I_{CC} current
- Tight output skew
- Supports live insertion
- Pins for the optional JTAG boundary scan function are provided
- High density packaging in plastic Quad Flatpack

QUICK REFERENCE DATA

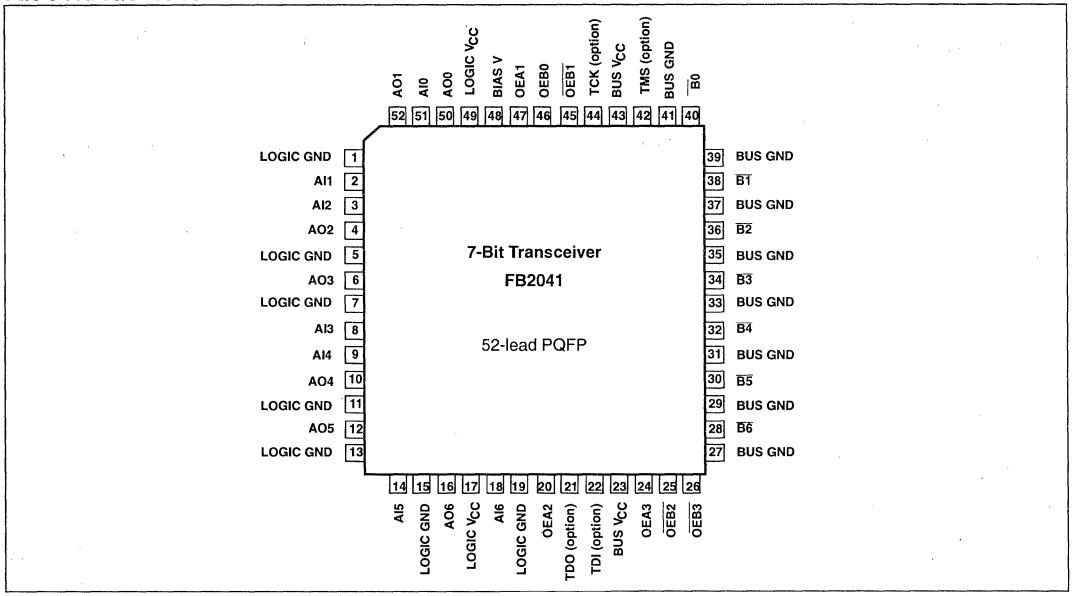
SYMBOL	PARAMETER		TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay AIn to $\overline{Bn}$		3.7 2.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{Bn}$ to AOn		3.4 3.2	ns
C_{OB}	Output capacitance ($\overline{B0}$ - $\overline{B6}$ only)		6	pF
I_{OL}	Output current ($\overline{B0}$ - $\overline{B6}$ only)		100	mA
I_{CC}	Supply Current	Standby	19	mA
		AIn to $\overline{Bn}$ (outputs Low or High)	40	
		$\overline{Bn}$ to AOn (outputs Low)	22	
		$\overline{Bn}$ to AOn (outputs High)	19	

ORDERING INFORMATION

PACKAGE	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0 to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10%; T_{amb} = -40 to +85°C	DWG No.
52-pin Plastic Quad Flatpack	FB2041BB	FB2041IBB	1418B

7-bit Futurebus+ transceiver FB2041

PIN CONFIGURATION



The B-port interfaces to "Backplane Transceiver Logic" (See the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1Vp-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

There are three separate pairs of driver enables in a 1 bit, 3 bit, 3 bit arrangement. The TTL/BTL output drivers for bit 0 are enabled with OEA1/$\overline{\text{OEB1}}$, output drivers for bits 1–2–3 are enabled with OEA2/$\overline{\text{OEB2}}$ and output drivers for bits 4–5–6 are enabled with OEA3/$\overline{\text{OEB3}}$.

The A-port operates at TTL levels with separate I/O. The 3-state A-port drivers are enabled when OEAn goes High after an extra 6ns delay which is built in to provide a break-before-make function. When OEAn goes Low, A-port drivers become High impedance without any extra delay. During power on/off cycles, the A-port drivers are held in a High impedance state when V_{CC} is below 2.5V.

The B-port has an output enable, OEB0, which affects all seven drivers. When OEB0 is High and $\overline{\text{OEBn}}$ is Low the output driver will be enabled. When OEB0 is Low or if $\overline{\text{OEBn}}$ is High, the B-port drivers will be inactive and at the level of the backplane signal.

To support live insertion, OEB0 is held Low during power on/off cycles to insure glitch free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 5V level while V_{CC} is Low. If live insertion is not a requirement, the BIAS V pin should be tied to a V_{CC} pin.

The LOGIC GND and BUS GND pins are isolated in the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a "hard" signal failure occurs instead of a pattern dependent error that may be very infrequent and impossible to trouble-shoot.

The LOGIC V_{CC} and BUS V_{CC} pins are also isolated internally to minimize noise and may be externally decoupled separately or simply tied together.

JTAG boundary scan functionality is provided as an option with signals TMS, TCK, TDI and TDO. When this option is not present, TMS and TCK are no-connects (no bond wires) and TDI and TDO are shorted together internally.

PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
AI0 – AI6	51, 2, 3, 8, 9, 14, 18	Input	Data inputs (TTL)
AO0 – AO6	50, 52, 4, 6, 10, 12, 16	Output	3-state outputs (TTL)
$\overline{B0}$ – $\overline{B6}$	40, 38, 36, 34, 32, 30, 28	I/O	Data inputs/Open Collector outputs, High current drive (BTL)
OEB0	46	Input	Enables the Bn outputs when High
$\overline{OEB1}$	45	Input	Enables the B0 output when Low
$\overline{OEB2}$	25	Input	Enables the B1 – B3 outputs when Low
$\overline{OEB3}$	26	Input	Enables the B4 – B6 outputs when Low
OEA1	47	Input	Enables the A0 outputs when High
OEA2	20	Input	Enables the A1 – A3 outputs when High
OEA3	24	Input	Enables the A4 – A6 outputs when High
BUS GND	41, 39, 37, 35, 33, 31, 29, 27	GND	Bus ground (0V)
LOGIC GND	1, 5, 7, 11, 13, 15, 19	GND	Logic ground (0V)
BUS V_{CC}	23, 43	Power	Positive supply voltage
LOGIC V_{CC}	17, 49	Power	Positive supply voltage
BIAS V	48	Power	Positive supply voltage
TMS	42	Input	Test Mode Select (no-connect)
TCK	44	Input	Test Clock (no-connect)
TDI	22	Input	Test Data In (shorted to TDO)
TDO	21	Output	Test Data Out (TDI)

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage	AI0 – AI6, OEB0, $\overline{OEBn}$, OEAn	-1.2 to +7.0	V
		$\overline{B0}$ – $\overline{B6}$	-1.2 to +5.5	
I_{IN}	Input current		-18 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	AO0 – AO6	48	mA
		$\overline{B0}$ – $\overline{B6}$	200	
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		COMMERCIAL LIMITS V_{CC} = 5V±10%; T_{amb} = 0 to +70°C			INDUSTRIAL LIMITS V_{CC} = 5V±10%; T_{amb} = -40 to +85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except $\overline{B0}$–$\overline{B6}$	2.0			2.0			V
		$\overline{B0}$ – $\overline{B6}$	1.62	1.55		1.62	1.55		
V_{IL}	Low-level input voltage	Except $\overline{B0}$–$\overline{B6}$			0.8			0.8	V
		$\overline{B0}$ – $\overline{B6}$			1.47			1.47	
I_{IK}	Input clamp current				-18			-18	mA
I_{OH}	High-level output current	AO0 – AO6			-3			-3	mA
I_{OL}	Low-level output current	AO0 – AO6			24			24	mA
		$\overline{B0}$ – $\overline{B6}$			100			100	
C_{OB}	Output capacitance on B port			6	7		6	7	pF
T_{amb}	Operating free-air temperature range		0		+70	-40		+85	°C

FUNCTION TABLE

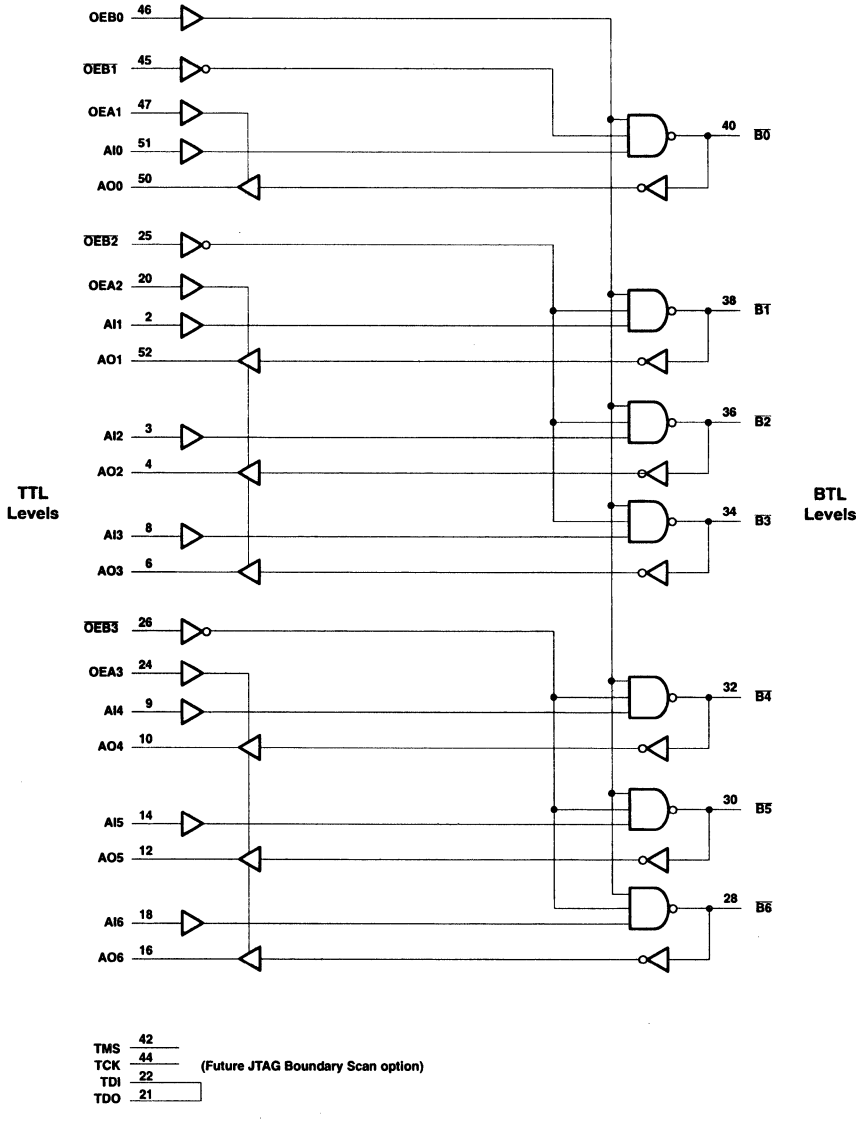
MODE	INPUTS									OUTPUTS	
	AIn	$\overline{Bn}$*	OEB0	$\overline{OEB1}$	$\overline{OEB2}$	$\overline{OEB3}$	OEA1	OEA2	OEA3	AOn	$\overline{Bn}$*
AIn to $\overline{Bn}$	L	—	H	L	L	L	L	L	L	Z	H**
	H	—	H	L	L	L	L	L	L	Z	L
	L	—	H	L	L	L	H	H	H	L	H**
	H	—	H	L	L	L	H	H	H	H	L
AI0 to $\overline{B0}$	L	—	H	L	X	X	L	L	L	Z	H**
	H	—	H	L	X	X	L	L	L	Z	L
	L	—	H	L	X	X	H	H	H	L	H**
	H	—	H	L	X	X	H	H	H	H	L
AI1 – AI3 to $\overline{B1}$ – $\overline{B3}$	L	—	H	X	L	X	L	L	L	Z	H**
	H	—	H	X	L	X	L	L	L	Z	L
	L	—	H	X	L	X	H	H	H	L	H**
	H	—	H	X	L	X	H	H	H	H	L
AI4 – AI6 to $\overline{B4}$ – $\overline{B6}$	L	—	H	X	X	L	L	L	L	Z	H**
	H	—	H	X	X	L	L	L	L	Z	L
	L	—	H	X	X	L	H	H	H	L	H**
	H	—	H	X	X	L	H	H	H	H	L
Disable $\overline{Bn}$ outputs	X	X	L	X	X	X	X	X	X	X	H**
	X	X	X	H	H	H	X	X	X	X	H**
Disable $\overline{B0}$ outputs	X	X	H	H	X	X	X	X	X	X	H**
Disable $\overline{B1}$ – $\overline{B3}$ outputs	X	X	H	X	H	X	X	X	X	X	H**
Disable $\overline{B4}$ – $\overline{B6}$ outputs	X	X	H	X	X	H	X	X	X	X	H**
$\overline{Bn}$ to AOn	X	L	L	X	X	X	H	H	H	H	Input
	X	H	L	X	X	X	H	H	H	L	Input
	X	L	X	H	H	H	H	H	H	H	Input
	X	H	X	H	H	H	H	H	H	L	Input
$\overline{B0}$ to AO0	X	L	L	X	X	X	H	X	X	H	Input
	X	H	L	X	X	X	H	X	X	L	Input
	X	L	X	H	H	H	H	X	X	H	Input
	X	H	X	H	H	H	H	X	X	L	Input
$\overline{B1}$ – $\overline{B3}$ to AO1 – AO3	X	L	L	X	X	X	X	H	X	H	Input
	X	H	L	X	X	X	X	H	X	L	Input
	X	L	X	H	H	H	X	H	X	H	Input
	X	H	X	H	H	H	X	H	X	L	Input
$\overline{B4}$ – $\overline{B6}$ to AO4 – AO6	X	L	L	X	X	X	X	X	H	H	Input
	X	H	L	X	X	X	X	X	H	L	Input
	X	L	X	H	H	H	X	X	H	H	Input
	X	H	X	H	H	H	X	X	H	L	Input
Disable AOn outputs	X	X	X	X	X	X	L	L	L	Z	X
Disable AO0 outputs	X	X	X	X	X	X	L	X	X	Z	X
Disable AO1 – AO3 outputs	X	X	X	X	X	X	X	L	X	Z	X
Disable AO4 – AO6 outputs	X	X	X	X	X	X	X	X	L	Z	X

NOTES:

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state
— = Input not externally driven
H** = Goes to level of pull-up voltage
B* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.

Z = High-impedance (OFF) state
— = Input not externally driven
H** = Goes to level of pull-up voltage
B* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.

LOGIC DIAGRAM



LOGIC V_{CC} = 17, 49
LOGIC GND = 1, 5, 7, 11, 13, 15, 19
BUS V_{CC} = 23, 24
BUS GND = 27, 29, 31, 33, 35, 37, 39, 41
BIAS V = 48

LIVE INSERTION SPECIFICATIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	TYP	MAX	
V_{BIASV}	Bias pin voltage	V_{CC} = 0 to 5.25V, $\overline{Bn}$ = 0 to 2.0V	4.5		5.5	V
I_{BIASV}	Bias pin DC current	V_{CC} = 0 to 4.75V, $\overline{Bn}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V			1	mA
		V_{CC} = 4.5 to 5.5V, $\overline{Bn}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V			10	µA
$V_{\overline{Bn}}$	Bus voltage during prebias	$\overline{B0}$ – $\overline{B8}$ = 0V, Bias V = 5.0V	1.62		2.1	V
I_{LM}	Fall current during prebias	$\overline{B0}$ – $\overline{B8}$ = 2V, Bias V = 4.5 to 5.5V	1			µA
I_{HM}	Rise current during prebias	$\overline{B0}$ – $\overline{B8}$ = 1V, Bias V = 4.5 to 5.5V	-1			µA
$I_{\overline{Bn}PEAK}$	Peak bus current during insertion	V_{CC} = 0 to 5.25V, $\overline{B0}$ – $\overline{B8}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V, OEB0 = 0.8V, t_r = 2ns			10	mA
$I_{OL}OFF$	Power up current	V_{CC} = 0 to 5.25V, OEB0 = 0.8V			100	µA
		V_{CC} = 0 to 2.2V, OEB0 = 0 to 5V			100	
t_{GR}	Input glitch rejection	V_{CC} = 5.0V	1.0	1.35		ns

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				MIN	TYP[2]	MAX	
I_{OH}	High level output current	$\overline{B0}$ – $\overline{B6}$	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V			100	µA
I_{OFF}	Power-off output current	$\overline{B0}$ – $\overline{B6}$	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 2.1V			100	µA
V_{OH}	High-level output voltage	AO0 – AO6 [3]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = -3mA	2.5	2.85		V
V_{OL}	Low-level output voltage	AO0 – AO6 [3]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 24mA		0.33	0.5	V
		$\overline{B0}$ – $\overline{B6}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 80mA	.75	1.0	1.10	
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 100mA			1.15	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-1.2	V
I_I	Input current at maximum input voltage	OEB0, $\overline{OEBn}$, OEAn, AI0 – AI6	V_{CC} = MAX, V_I = GND or 5.5V			±50	µA
I_{IH}	High-level input current	OEB0, $\overline{OEBn}$, OEAn, AI0 – AI6	V_{CC} = MAX, V_I = 2.7V			20	µA
		$\overline{B0}$ – $\overline{B6}$	V_{CC} = MAX, V_I = 2.1V			100	
I_{IL}	Low-level input current	OEB0, $\overline{OEBn}$, OEAn, AI0 – AI6	V_{CC} = MAX, V_I = 0.5V			-20	µA
		$\overline{B0}$ – $\overline{B6}$	V_{CC} = MAX, V_I = 0.75V			-100	
I_{OZH}	Off-state output current	AO0 – AO6	V_{CC} = MAX, V_O = 2.7V			50	µA
I_{OZL}	Off-state output current	AO0 – AO6	V_{CC} = MAX, V_O = 0.5V			-50	µA
I_O	Output current	AO0 – AO6 only	V_{CC} = MAX	-30	-55	-150	mA
I_{CC}	Supply current (total)	I_{CCZ} (standby)	V_{CC} = MAX		19	30	mA
		I_{CCB}, AIn to $\overline{Bn}$	V_{CC} = MAX, outputs Low or High		40	60	
		I_{CCA}, $\overline{Bn}$ to AOn	V_{CC} = MAX, outputs Low		22	35	
		I_{CCA}, $\overline{Bn}$ to AOn	V_{CC} = MAX, outputs High		19	35	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Due to test equipment limitations, actual test conditions are V_{IH} = 1.8V and V_{IL} = 1.3V for the B side.

AC ELECTRICAL CHARACTERISTICS (Commercial)

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0 to 70°C, V_{CC} = 5V±10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay, $\overline{Bn}$ to AOn	Waveform 1, 2	1.8 1.6	3.4 3.2	5.0 4.9	1.6 1.6	5.5 5.0	ns
t_{PZH} t_{PZL}	Output enable time, OEA to AOn	Waveform 5, 6	2.2 2.0	5.0 4.0	8.0 6.5	2.0 1.8	10.0 8.0	ns
t_{PHZ} t_{PLZ}	Output disable time, OEA to AOn	Waveform 5, 6	1.5 1.8	3.3 3.0	4.8 5.0	1.2 1.5	5.0 5.5	ns
t_{TLH} t_{THL}	Transition time, AOn Port (10% to 90% or 90% to 10%)	Test Circuit and Waveforms	1.5 1.5	2.2 2.4	3.0 3.0	1.5 1.5	3.5 3.5	ns
$t_{SK(o)}$	Output skew between receivers in same package[1]	Waveform 3		0.4	1.0		1.0	ns
SYMBOL	**PARAMETER**	**TEST CONDITION**	**B PORT LIMITS**					**UNIT**
			T_{amb} = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 9Ω			T_{amb} = 0 to 70°C, V_{CC} = 5V±10%, C_D = 30pF, R_U = 9Ω		
t_{PLH} t_{PHL}	Propagation delay, AIn to $\overline{Bn}$	Waveform 1, 2	2.4 1.5	3.7 2.7	4.9 4.4	1.9 1.5	5.7 5.0	ns
t_{PLH} t_{PHL}	Enable/disable time, OEB0 to $\overline{Bn}$	Waveform 2	2.4 1.9	3.7 3.5	4.9 4.9	1.9 1.8	6.4 5.4	ns
t_{PLH} t_{PHL}	Enable/disable time, $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1	2.4 1.9	4.0 3.6	5.5 5.5	1.9 2.5	5.9 5.9	ns
t_{TLH} t_{THL}	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.0 0.5	1.4 1.1	3.0 3.0	1.0 0.5	3.0 3.0	ns
$t_{SK(o)}$	Output skew between drivers in same package[1]	Waveform 3		0.3	1.0		1.0	ns
SYMBOL	**PARAMETER**	**TEST CONDITION**	R_U = 16.5Ω			R_U = 16.5Ω		**UNIT**
t_{PLH} t_{PHL}	Propagation delay, AIn to $\overline{Bn}$	Waveform 1, 2	2.5 1.6	3.8 2.8	5.0 4.5	2.0 1.6	5.8 5.1	ns
t_{PLH} t_{PHL}	Enable/disable time, OEB0 to $\overline{Bn}$	Waveform 2	2.5 2.0	3.8 3.6	5.0 5.0	2.0 1.9	6.5 5.5	ns
t_{PLH} t_{PHL}	Enable/disable time, $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1	2.5 2.0	4.1 3.7	5.6 5.6	2.0 2.6	6.0 6.0	ns
t_{TLH} t_{THL}	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.0 0.5	1.5 1.1	3.0 3.0	1.0 0.5	3.0 3.0	ns
$t_{SK(o)}$	Output skew between drivers in same package[1]	Waveform 3		0.3	1.0		1.0	ns

NOTES:

1. $|t_{PN}actual - t_{PM}actual|$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).

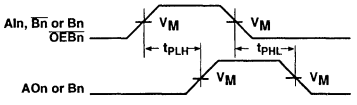
AC ELECTRICAL CHARACTERISTICS (Industrial)

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = -40 to +85°C, V_{CC} = 5V±10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay, $\overline{Bn}$ to AOn	Waveform 1, 2	1.8 1.6	3.4 3.2	5.0 4.9	1.6 1.6	5.5 5.0	ns
t_{PZH} t_{PZL}	Output enable time, OEA to AOn	Waveform 5, 6	2.2 2.0	5.0 4.0	8.0 6.5	2.0 1.5	11.0 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time, OEA to AOn	Waveform 5, 6	1.5 1.5	3.3 3.0	4.8 5.0	1.2 1.2	6.0 6.0	ns
t_{TLH} t_{THL}	Transition time, AOn Port (10% to 90% or 90% to 10%)	Test Circuit and Waveforms	1.5 1.5	2.2 2.4	3.0 3.0	1.5 1.5	3.5 3.5	ns
$t_{SK(o)}$	Output skew between receivers in same package[1]	Waveform 3		0.4	1.0		1.0	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 9Ω			T_{amb} = -40 to +85°C, V_{CC} = 5V±10%, C_D = 30pF, R_U = 9Ω		
t_{PLH} t_{PHL}	Propagation delay, AIn to $\overline{Bn}$	Waveform 1, 2	2.4 1.5	3.7 2.7	4.9 4.4	1.9 1.5	5.7 5.0	ns
t_{PLH} t_{PHL}	Enable/disable time, OEB0 to $\overline{Bn}$	Waveform 2	2.4 1.9	3.7 3.5	4.9 4.9	1.9 1.8	6.4 5.9	ns
t_{PLH} t_{PHL}	Enable/disable time, $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1	2.4 1.9	4.0 3.6	5.5 5.5	1.9 1.5	5.9 5.9	ns
t_{TLH} t_{THL}	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.0 0.5	1.4 1.1	3.0 3.0	1.0 0.5	3.0 3.0	ns
$t_{SK(o)}$	Output skew between drivers in same package[1]	Waveform 3		0.3	1.0		1.0	ns
SYMBOL	PARAMETER	TEST CONDITION	R_U = 16.5Ω			R_U = 16.5Ω		UNIT
t_{PLH} t_{PHL}	Propagation delay, AIn to $\overline{Bn}$	Waveform 1, 2	2.5 1.6	3.8 2.8	5.0 4.5	2.0 1.6	5.8 5.1	ns
t_{PLH} t_{PHL}	Enable/disable time, OEB0 to $\overline{Bn}$	Waveform 2	2.5 2.0	3.8 3.6	5.0 5.0	2.0 1.9	6.5 6.0	ns
t_{PLH} t_{PHL}	Enable/disable time, $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1	2.5 2.0	4.1 3.7	5.5 5.5	2.0 1.6	6.0 6.0	ns
t_{TLH} t_{THL}	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.0 0.5	1.5 1.1	3.0 3.0	1.0 0.5	3.0 3.0	ns
$t_{SK(o)}$	Output skew between drivers in same package[1]	Waveform 3		0.3	1.0		1.0	ns

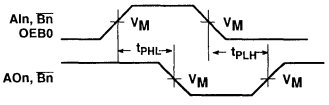
NOTES:

1. $|t_{PN}actual - t_{PM}actual|$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).

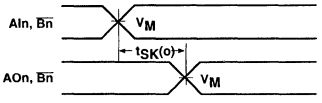
AC WAVEFORMS



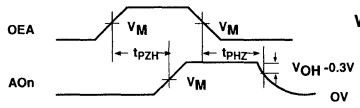
Waveform 1. Propagation Delay for Data or Output Enable to Output



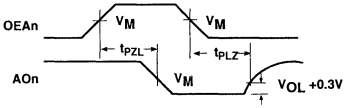
Waveform 2. Propagation Delay for Data or Output Enable to Output



Waveform 3. Output Skews



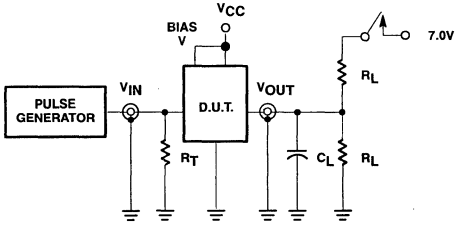
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



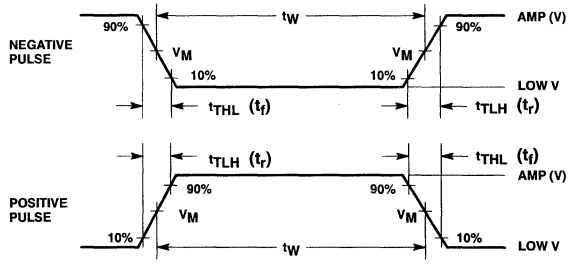
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs on A Port

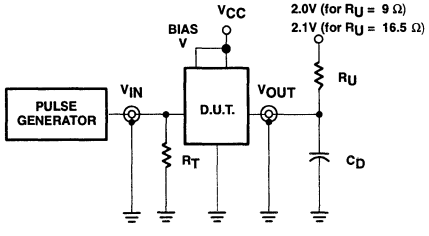


V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.

Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test Circuit for Outputs on B Port

Family FB+	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

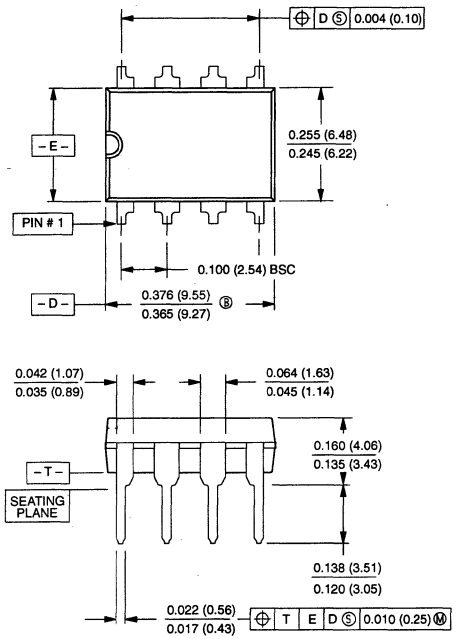
R_L = Load Resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_U = Pull up resistor; see AC CHARACTERISTICS for value.

Section 8
Package Outlines

CONTENTS

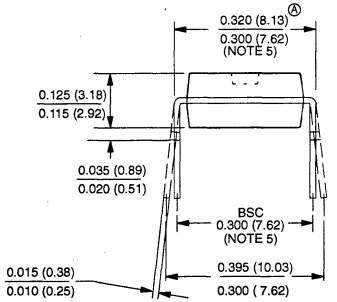
Package outlines

0404B 8-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



NOTES

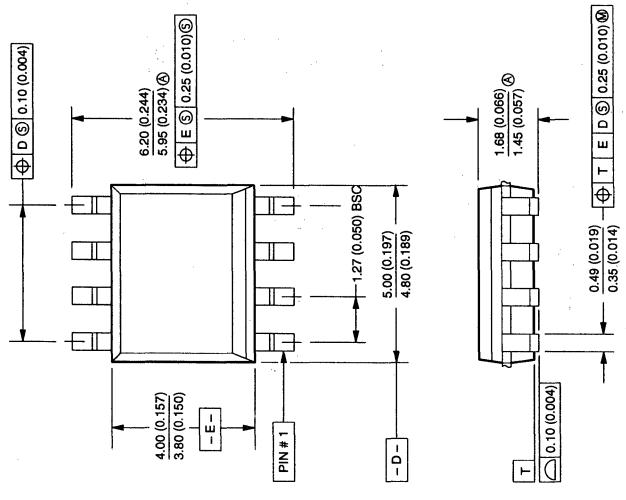
1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AB for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 8 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #8 when viewed from the top.



853-0404B 07236

Package outlines

0174C 8-PIN (157 mils wide) PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D) PACKAGE



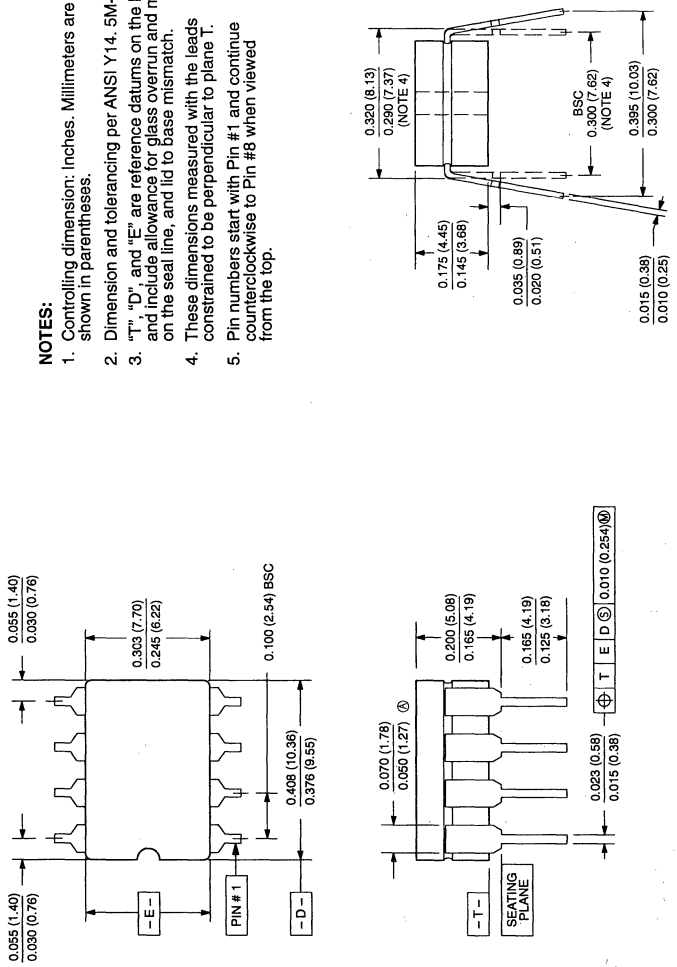
NOTES

1. Package dimensions conform to JEDEC Specification MS-012-AA for standard Small Outline (SO) package, 8 leads, 3.75mm (0.150") body width (Issue A, June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "D" and "E" are reference datums on the molded body and do not include mold flash/protrusions. Mold flash/protrusions at "D" shall not exceed 0.15mm (0.006") per side. Inter-lead flash/protrusions at "E" shall not exceed 0.25mm (0.010") per side.
5. The lead width above the seating plane shall not exceed a maximum value of 0.61mm (0.024").
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #8 when viewed from top.
7. Signetics ordering code for a product packages in a plastic Small Outline (SO) package is the suffix D after the product number.

853–0174C 04697

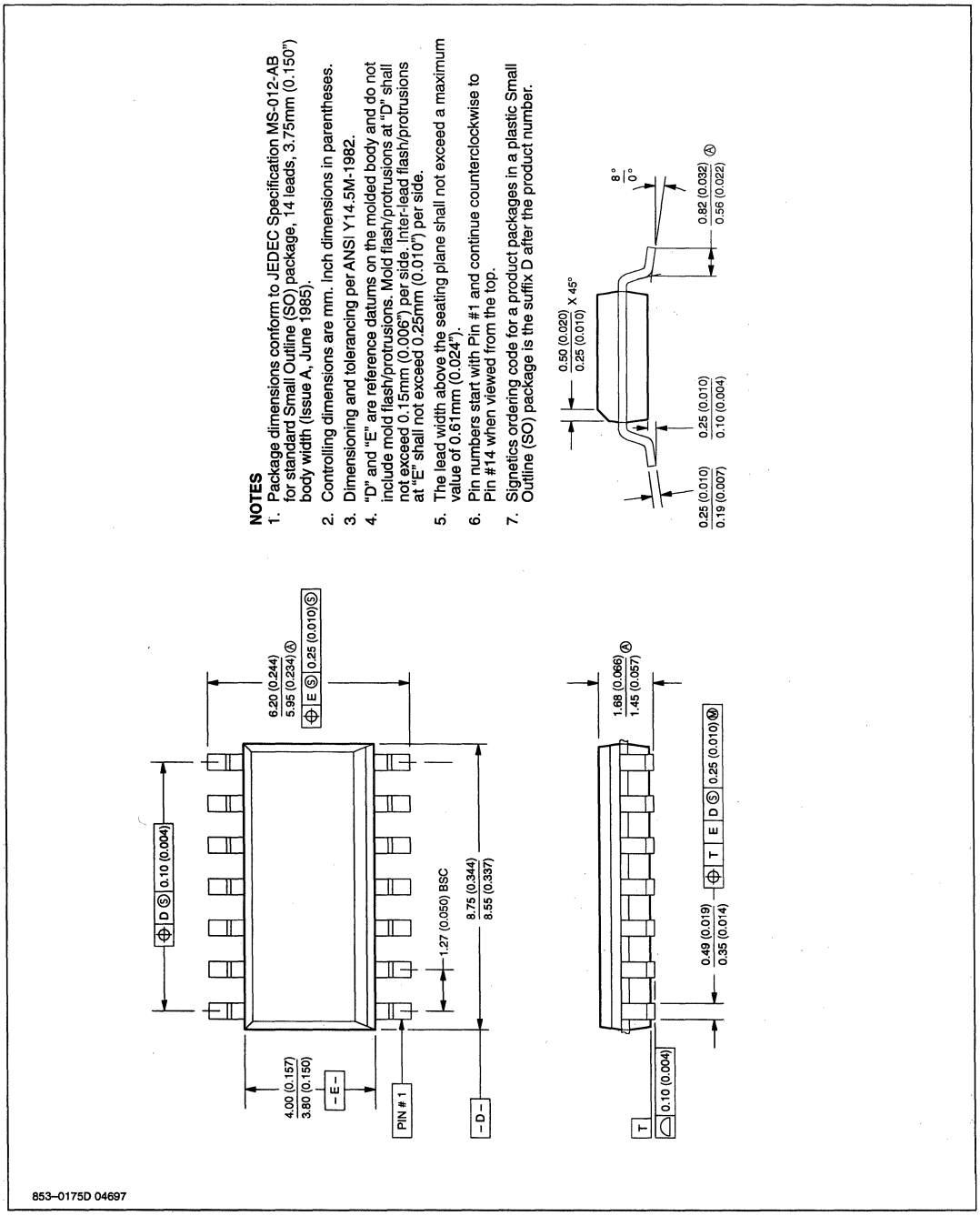
Package outlines

0580A 8-PIN (300 mils wide) CERAMIC DUAL IN-LINE (F) PACKAGE



Package outlines

0175D 14-PIN (157 mils wide) PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D) PACKAGE



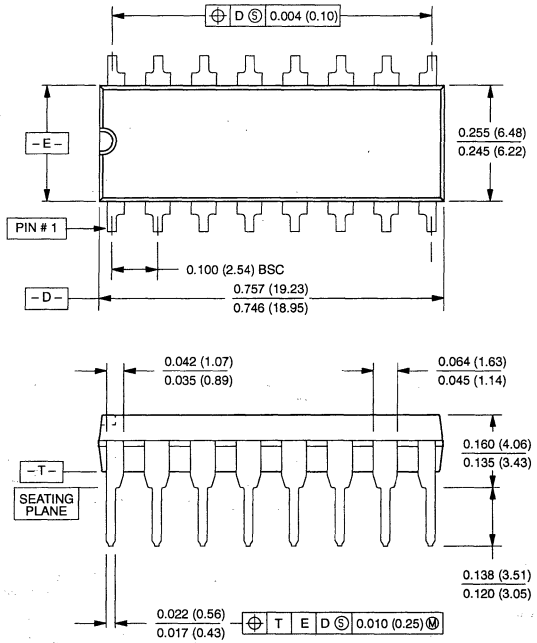
Package outlines

0406C 16-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE

DASH NO. NEXT ASSEMBLY

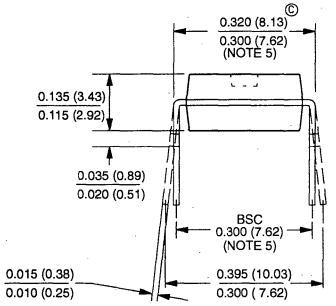
853-0406C 02880

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
——	GENERATE. PLACE IN SPEC CENTER AS PER ECN-081232	11-11-85	
A	SPEC CHANGE PER ECN-001615	1-31-91	
B	SPEC CHANGE PER ECN-001771	2-25-91	
C	SPEC CHANGE PER ECN-002880	6-13-91	Y.K. Kim 6-26-91



NOTES

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AA for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 16 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #16 when viewed from the top.



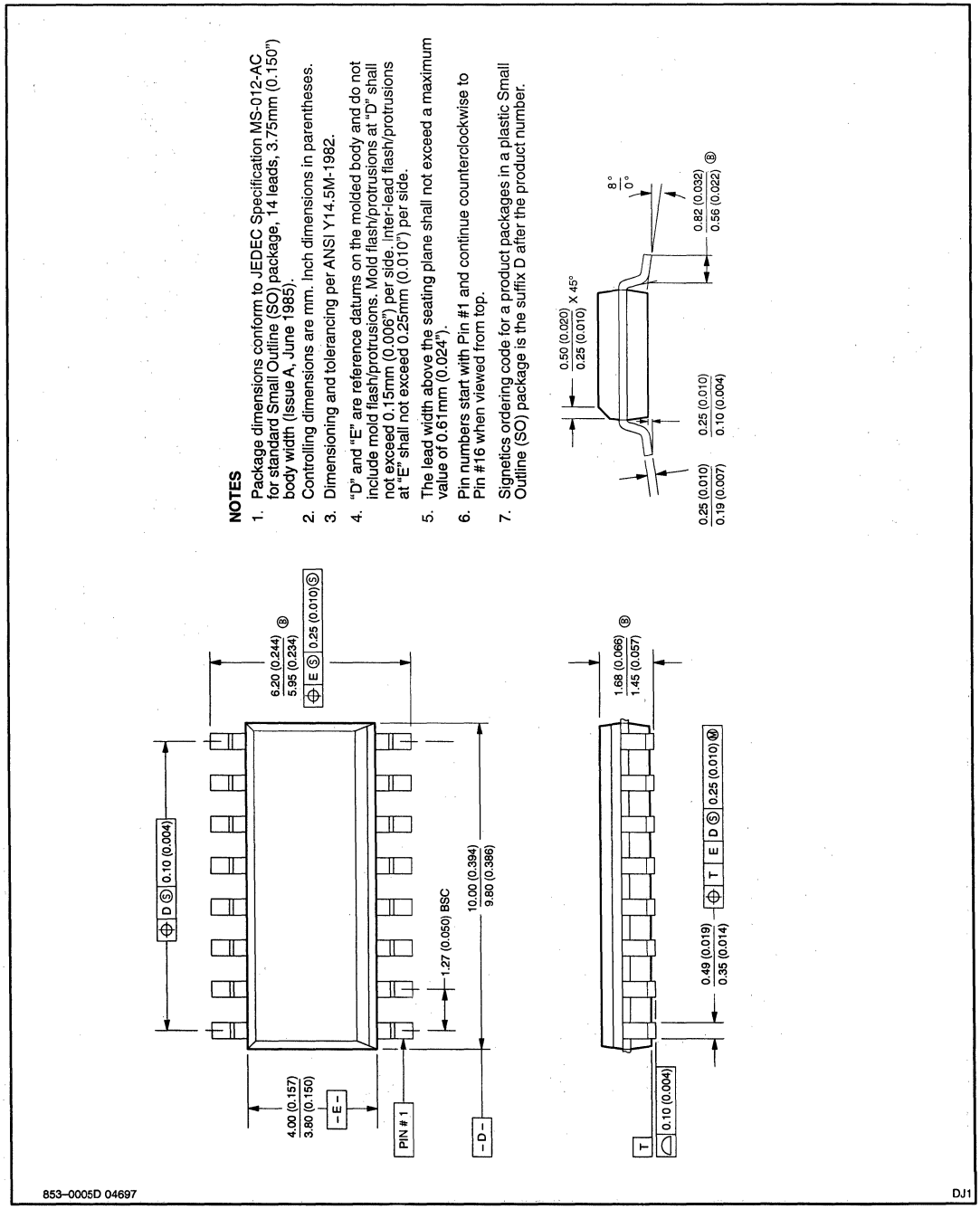
QTY REQ	DOCUMENT/PART NUMBER	TITLE/DESCRIPTION	ITEM NO
LIST OF MATERIALS AND APPLICABLE DOCUMENTS			

DRAWN J. PUMA	TITLE CPT PLAS PROD – NJ1 OUTLINE, PDIP 16 .300 C/L	Signetics a subsidiary of North American Philips Corp. 811 East Arques Avenue P.O. Box 3409 Sunnyvale, California 94088-3409 Telephone (408) 991-2000		
DESIGNER				
CHECKED				
APPROVED				
TOLERANCES UNLESS OTHERWISE SPECIFIED ANGULAR± FRAC± XXX± XX ± XXXX±	MATERIAL	DWG NO D853-0406		REV C
	FINISH			
	CAGE 18324	INTERLEAF: 0406C	SCALE 3X	SHT 1 OF 1

NJ1

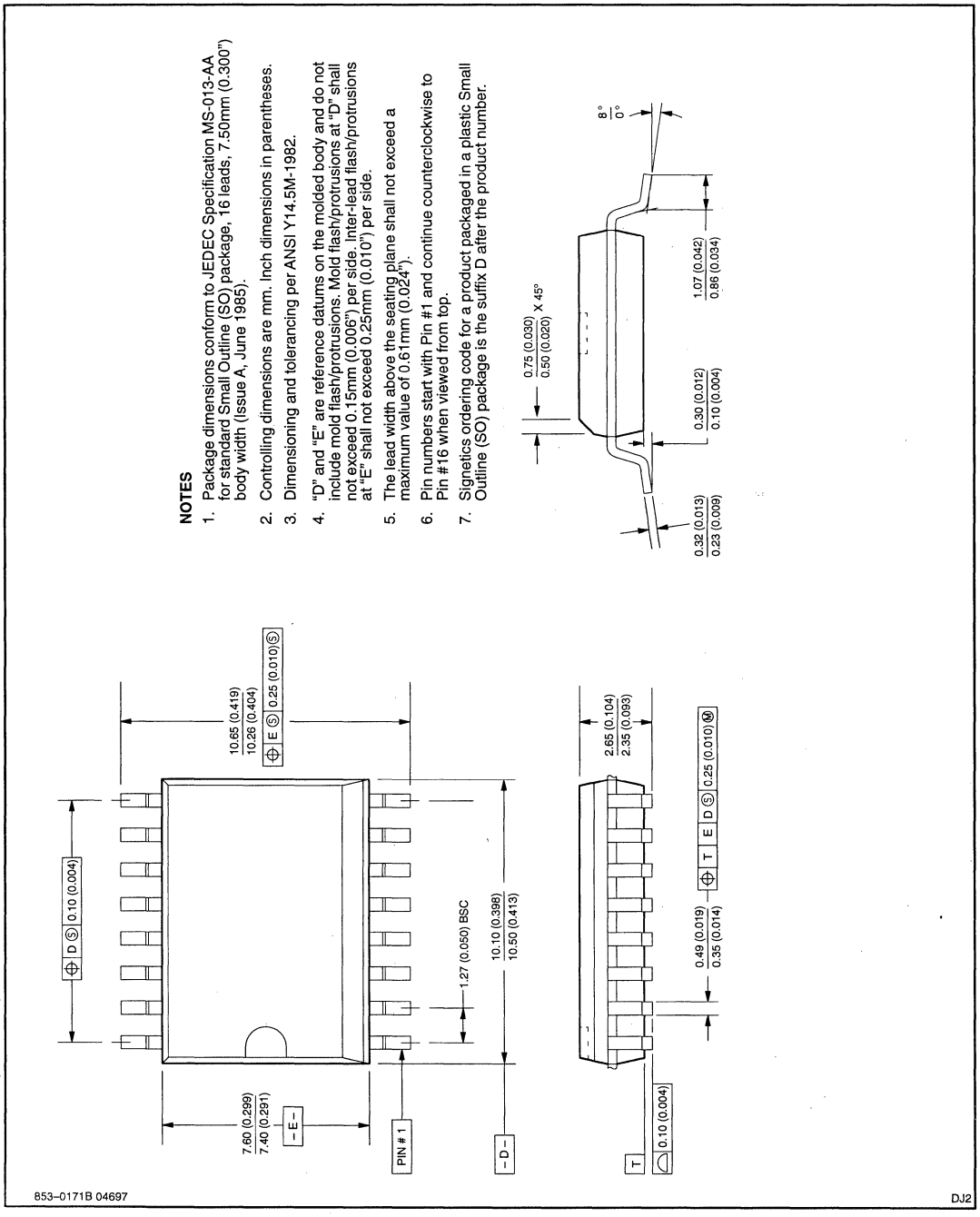
Package outlines

0005D 16-PIN (157 mils wide) PLASTIC SO (SMALL OUTLINE) DUAL IN-LINE (D) PACKAGE



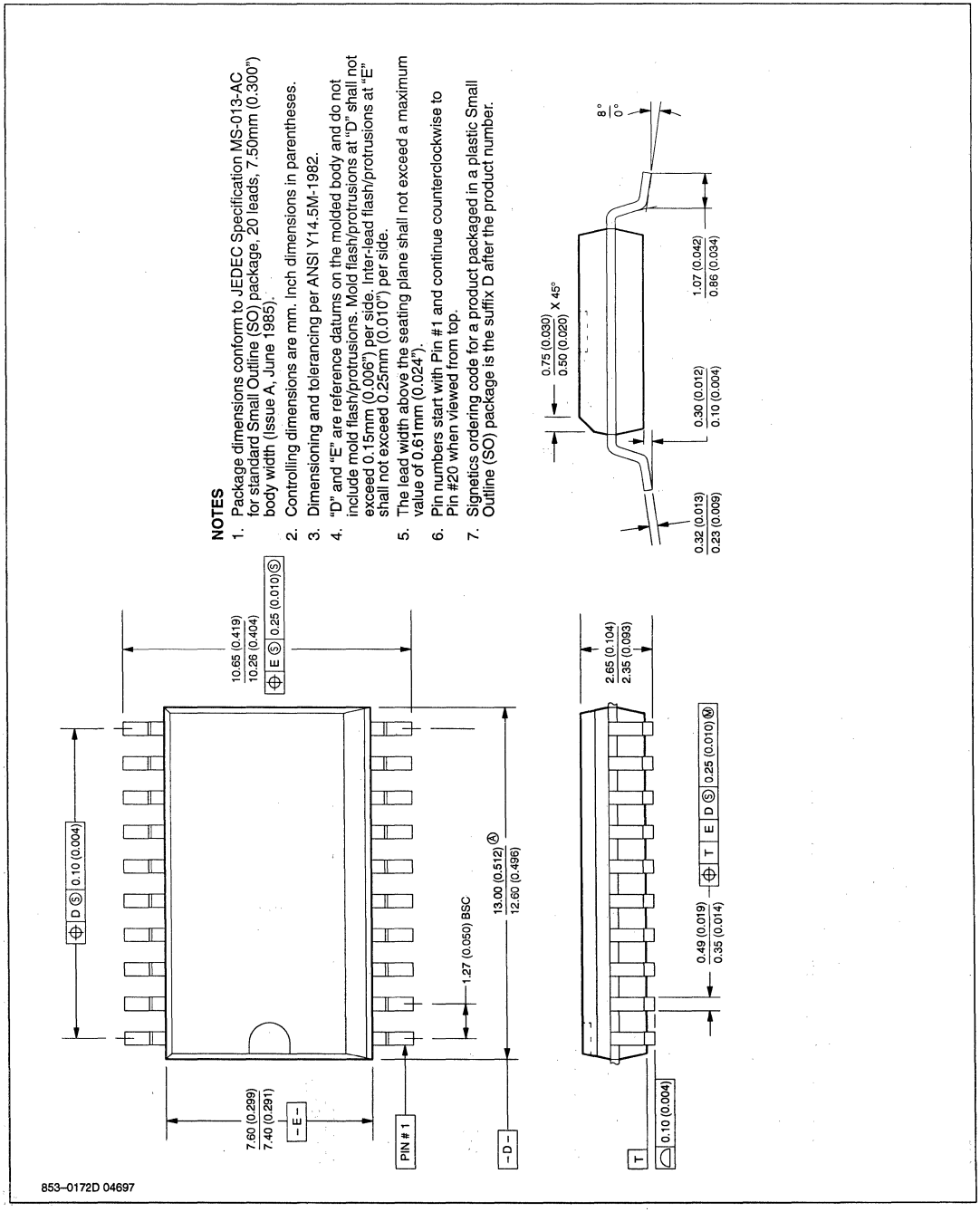
Package outlines

0171B 16-PIN (300 mils wide) PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D) PACKAGE



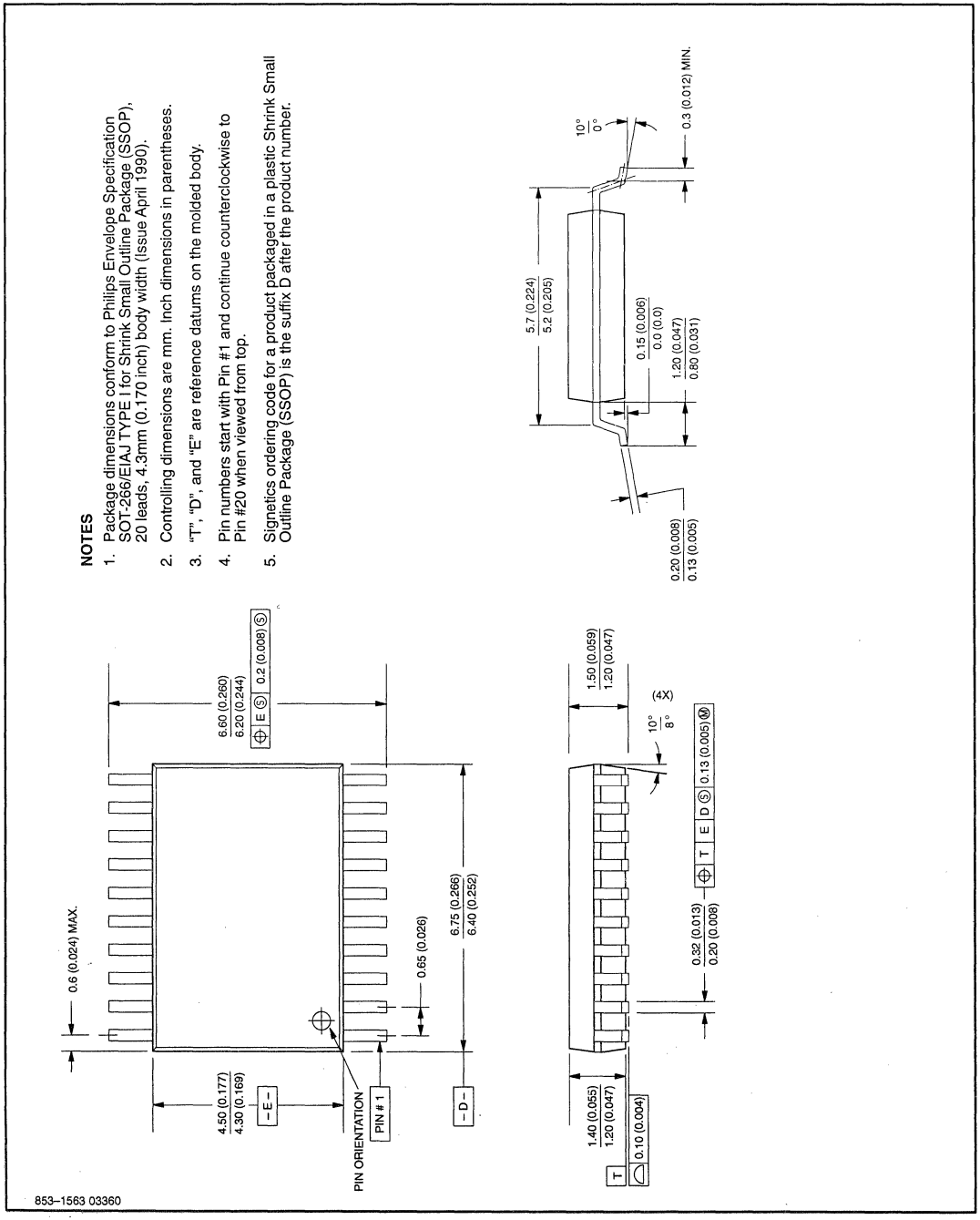
Package outlines

0172D 20-PIN (300 mils wide) PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D) PACKAGE



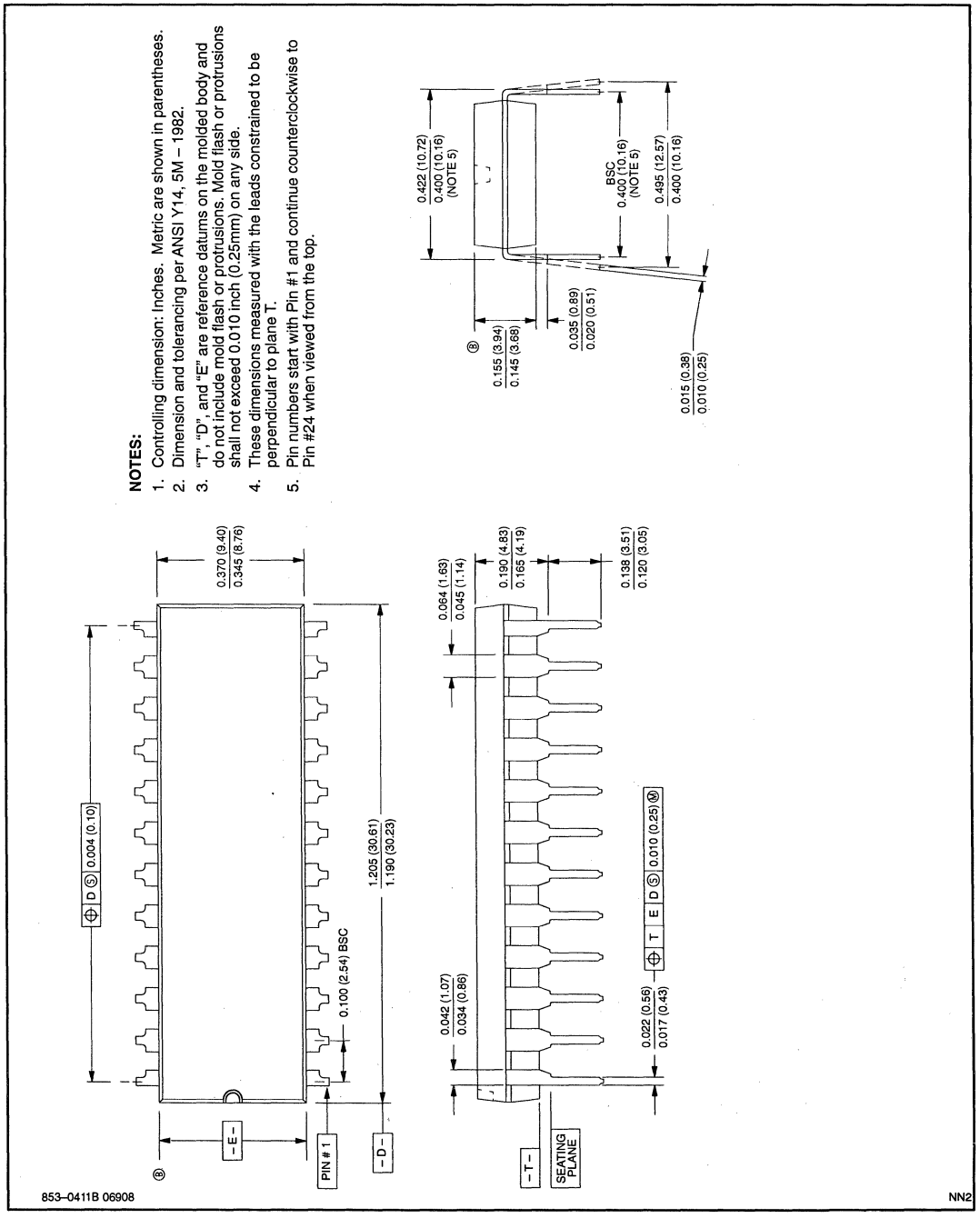
Package outlines

1563– 20-PIN PLASTIC (170 mils wide) SHRINK SMALL OUTLINE PACKAGE DUAL IN-LINE (D) PACKAGE



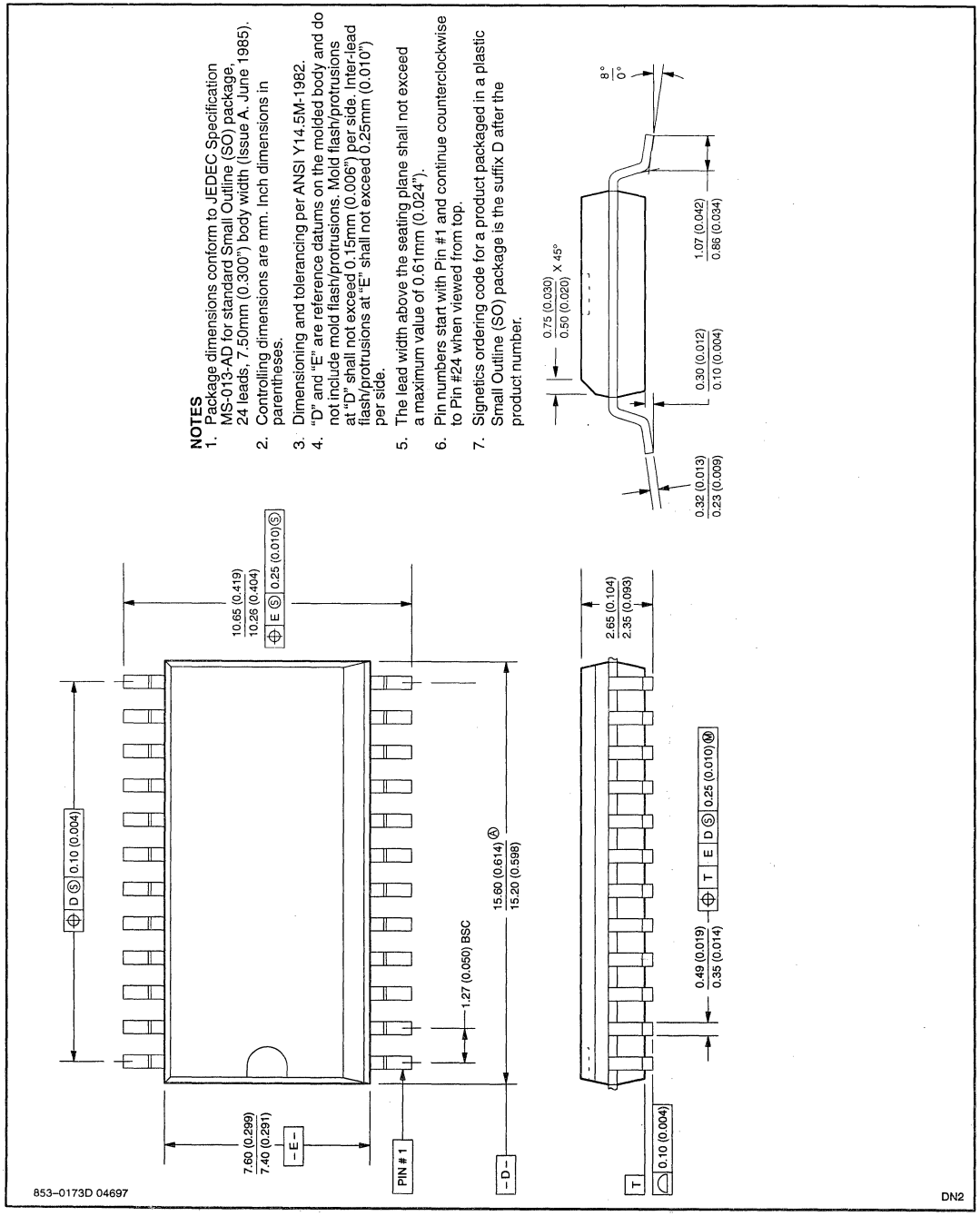
Package outlines

0411B 24-PIN (400 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



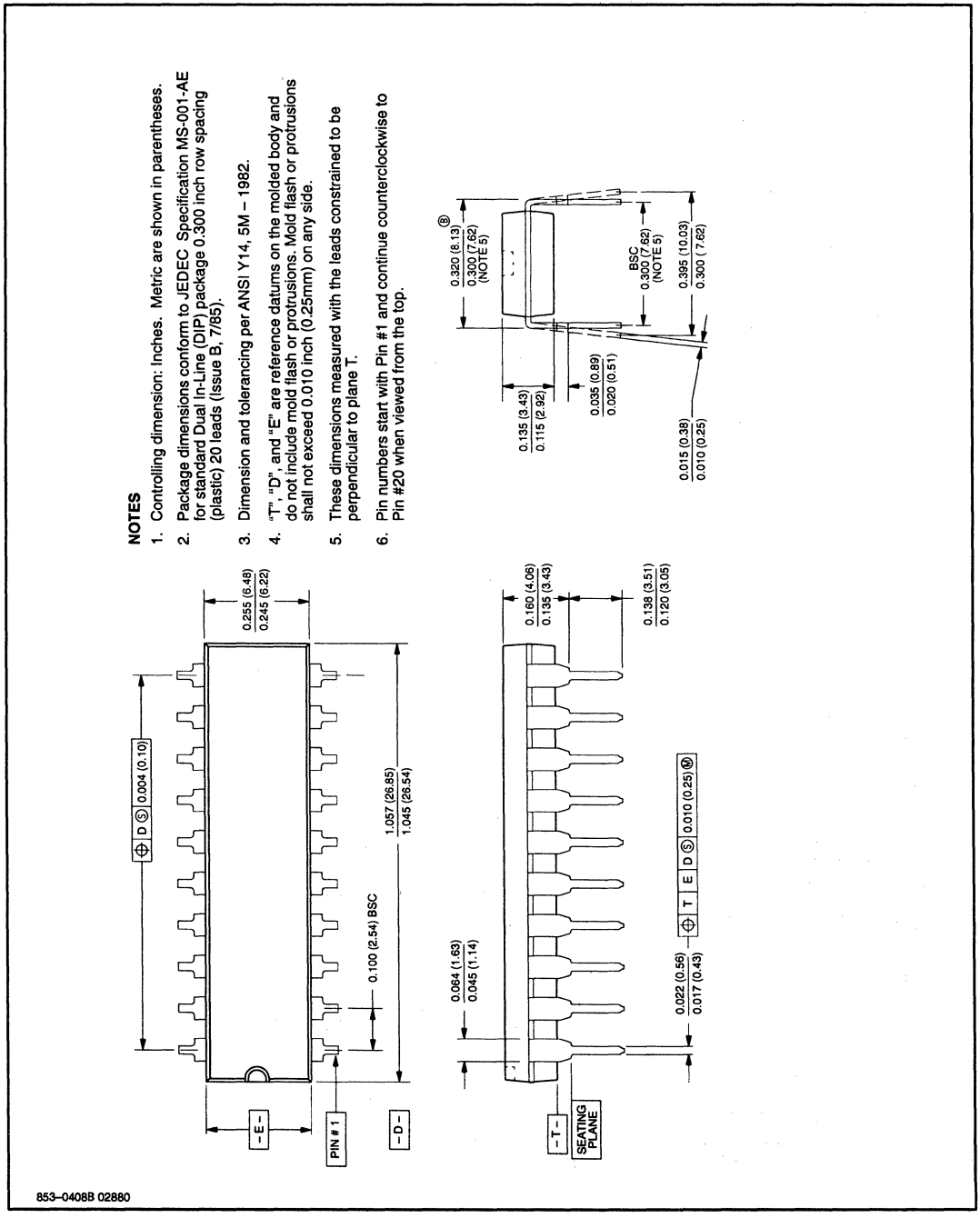
Package outlines

0173D 24-PIN (300 mils wide) Plastic SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D) PACKAGE



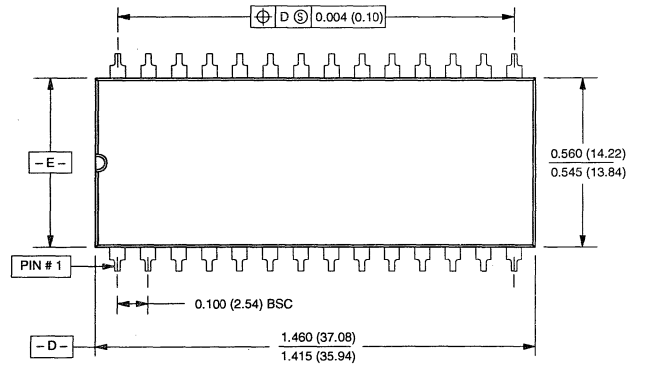
Package outlines

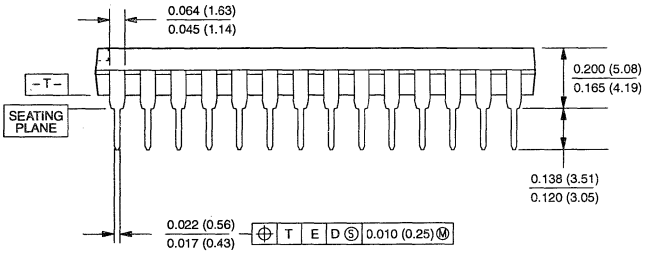
0408B 20-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



Package outlines

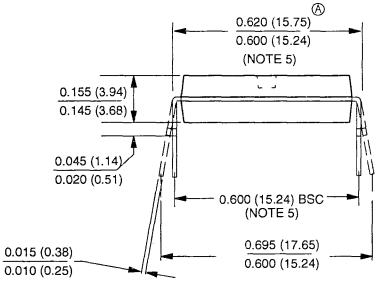
0413B 28-PIN (600 mils wide) Plastic Dual In-Line (N) Package





NOTES:

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-011-AB for standard Dual In-Line (DIP) package 0.600 inch row spacing (plastic) 28 leads (Issue B, 7/84).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #28 when viewed from the top.

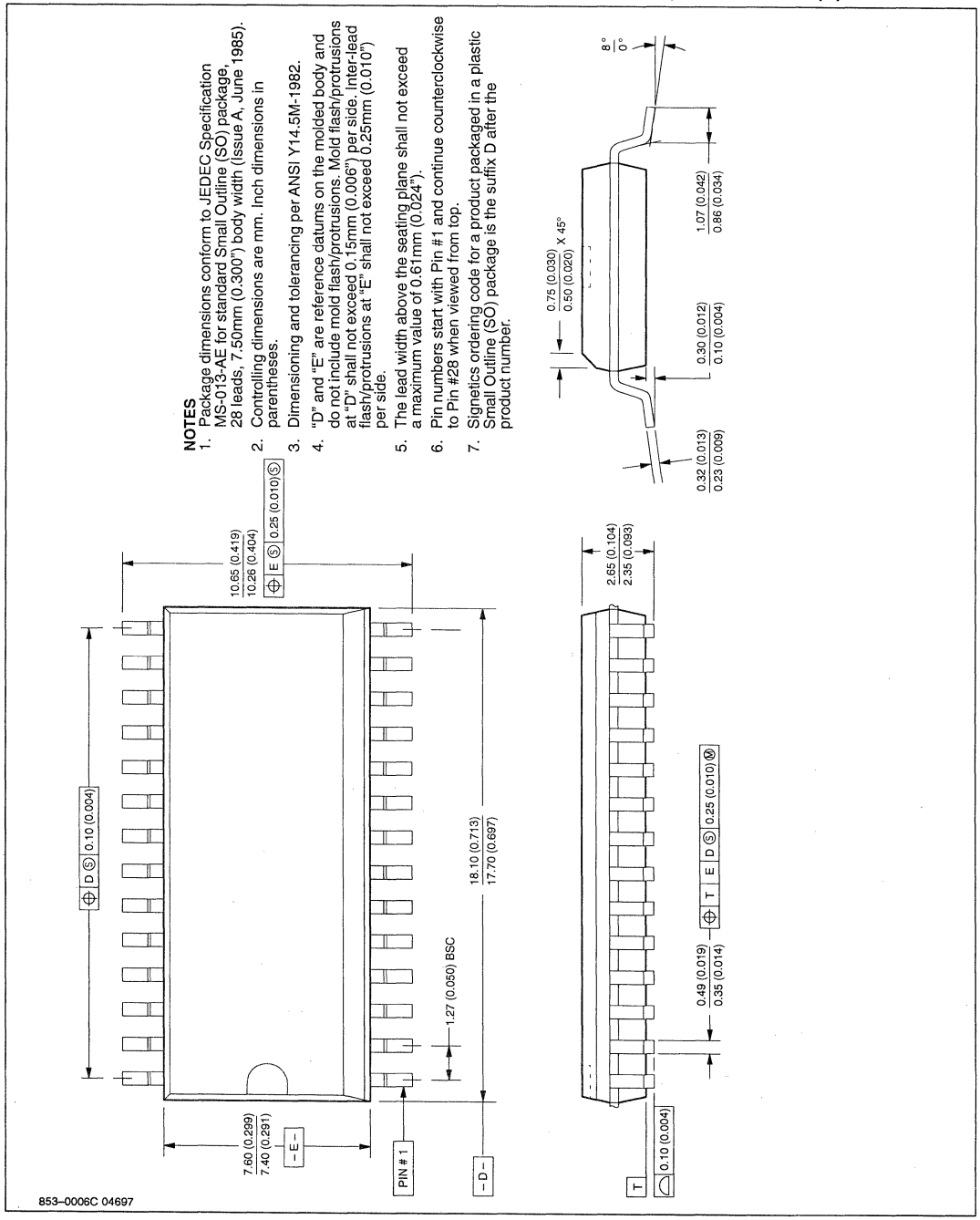


853-0413B 01988

NQ3

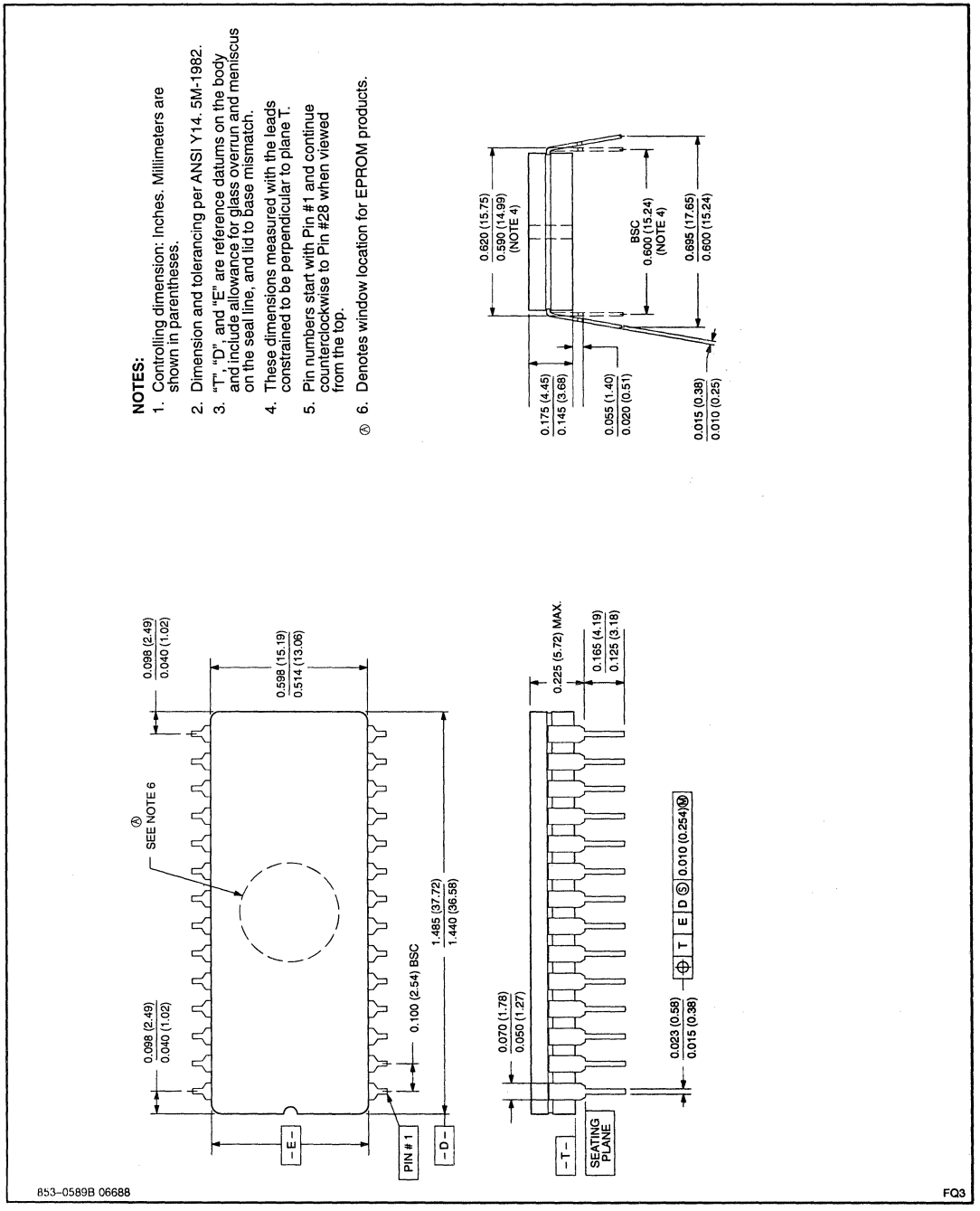
Package outlines

0006C 28-PIN (300 mils wide) PLASTIC SOL (SMALL OUTLINE LARGE) DUAL IN-LINE (D) PACKAGE



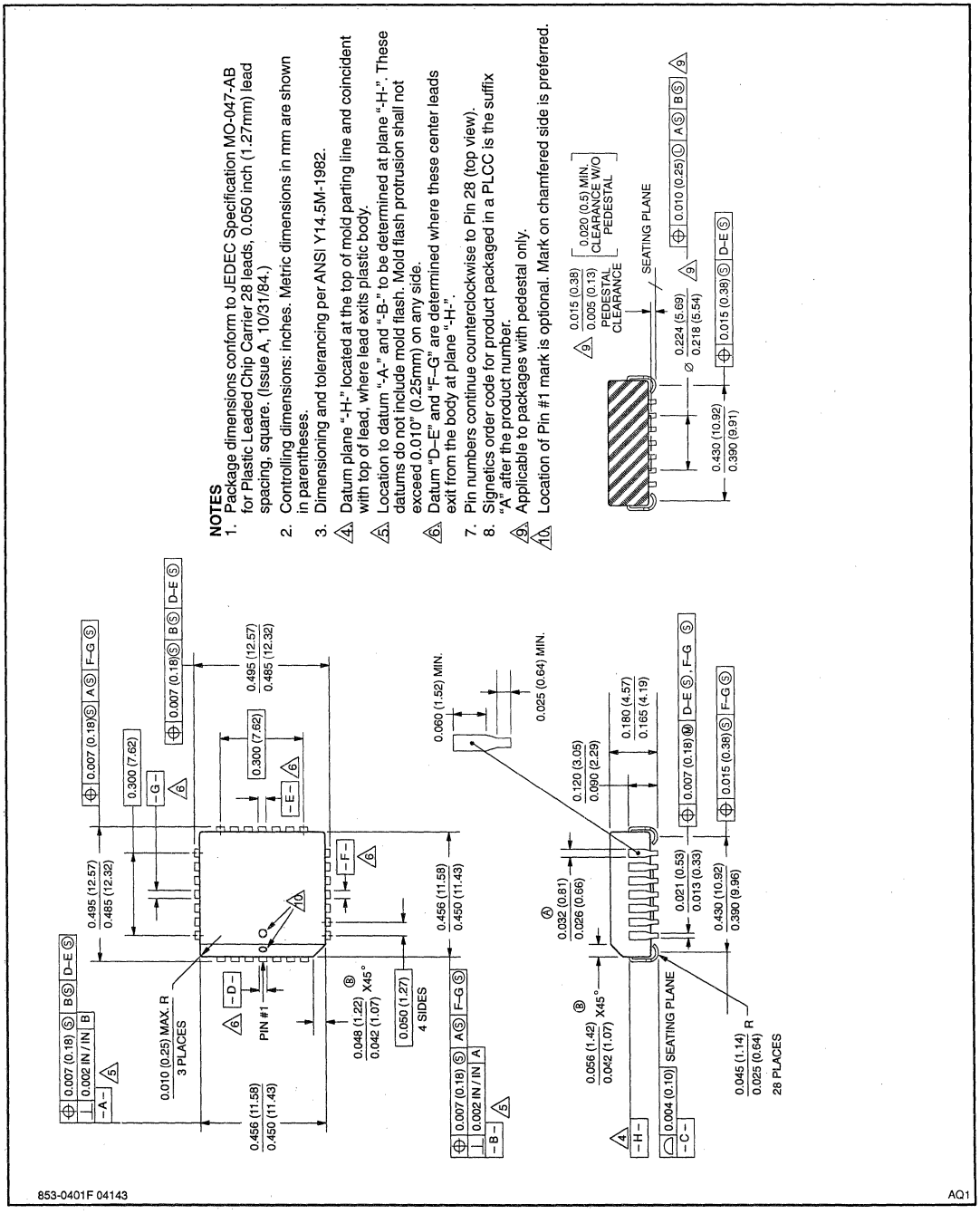
Package outlines

0589B 28-PIN (600 mils wide) CERAMIC DUAL IN-LINE (F) WITH WINDOW (FA) PACKAGE



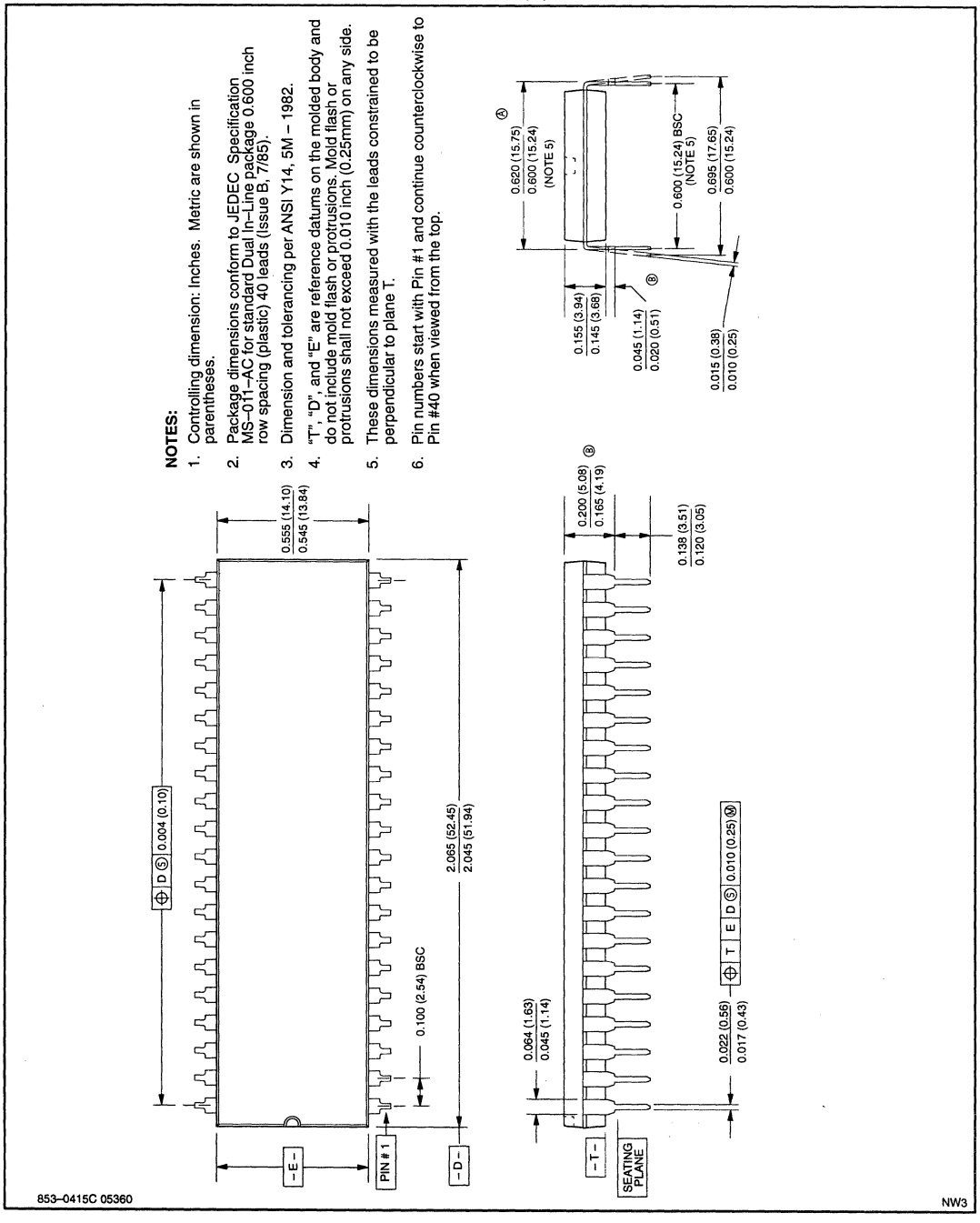
Package outlines

0401F 28-PIN PLASTIC LEADED CHIP CARRIER (A) PACKAGE



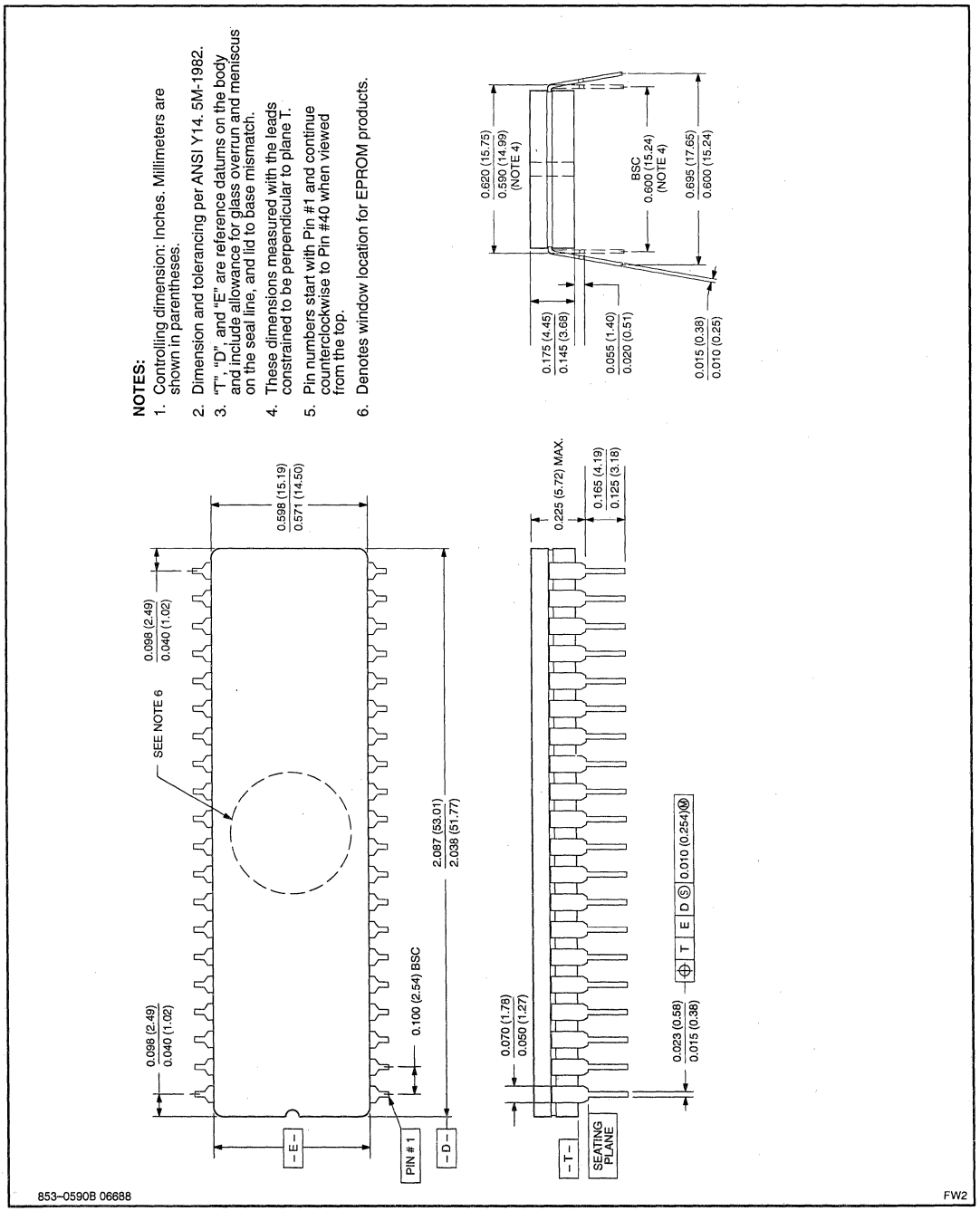
Package outlines

0415C 40-PIN (600 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



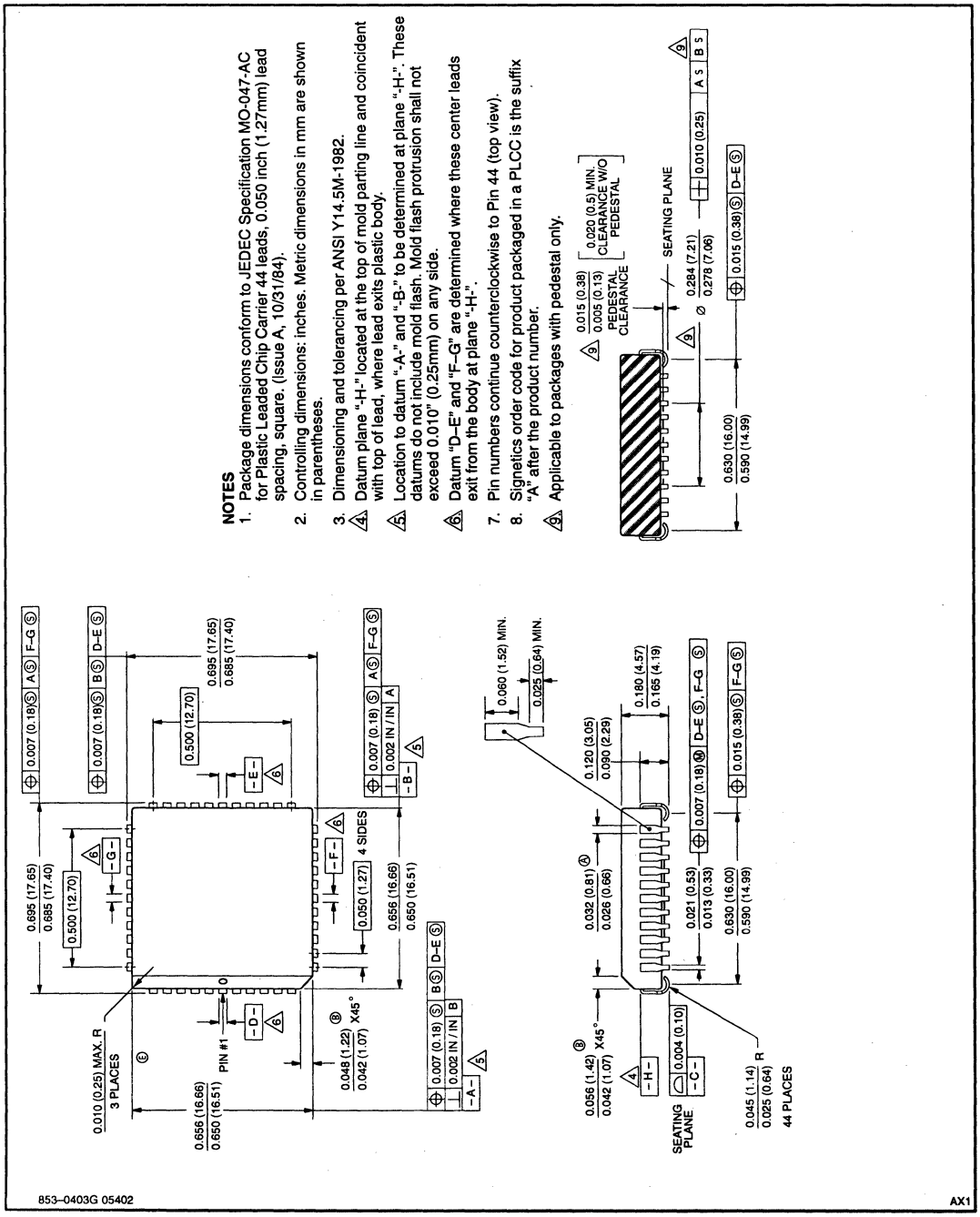
Package outlines

0590B 40-PIN (600 mils wide) CERAMIC DUAL IN-LINE (F) WITH WINDOW (FA) PACKAGE



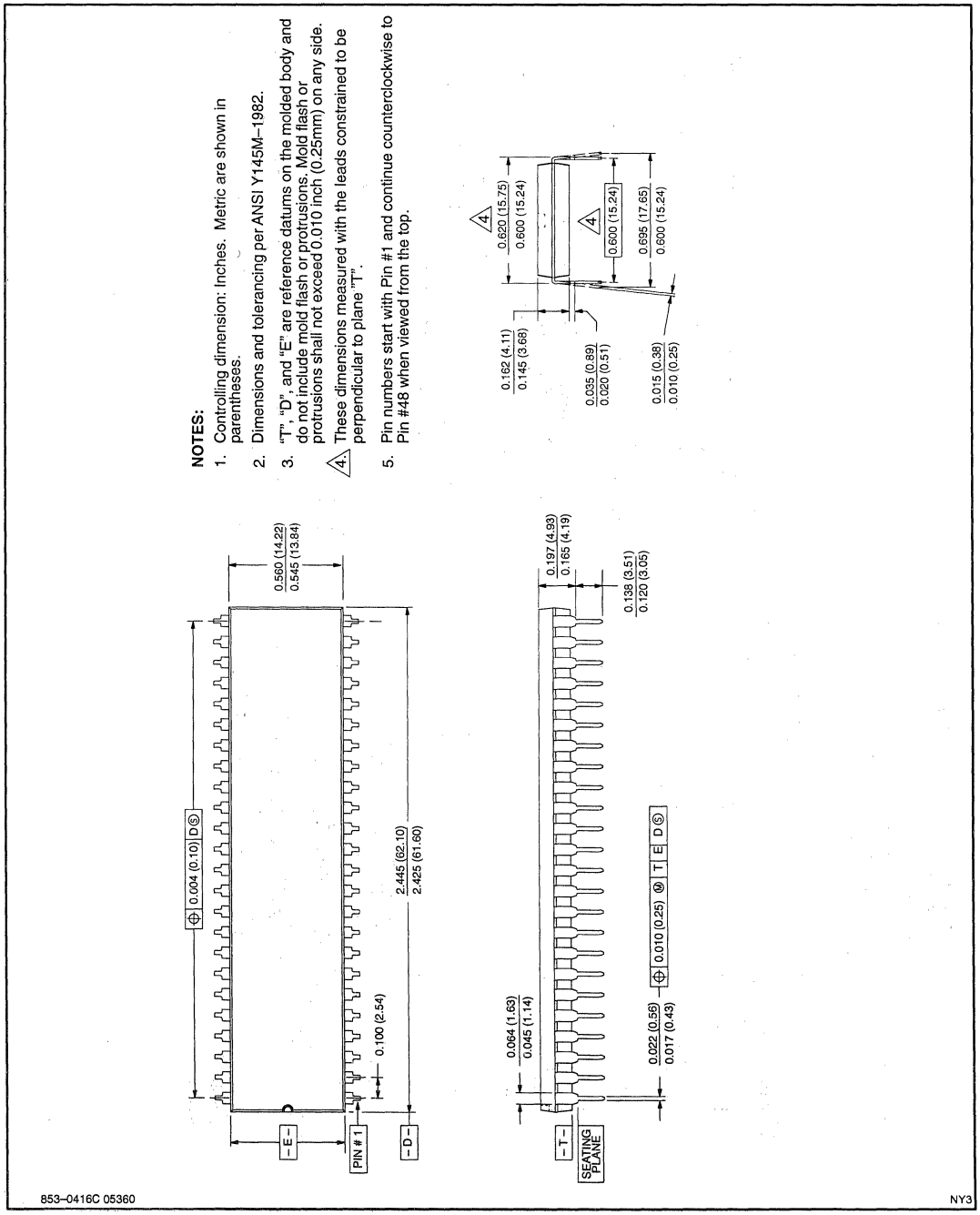
Package outlines

0403G 44-PIN PLASTIC LEADED CHIP CARRIER (A) PACKAGE



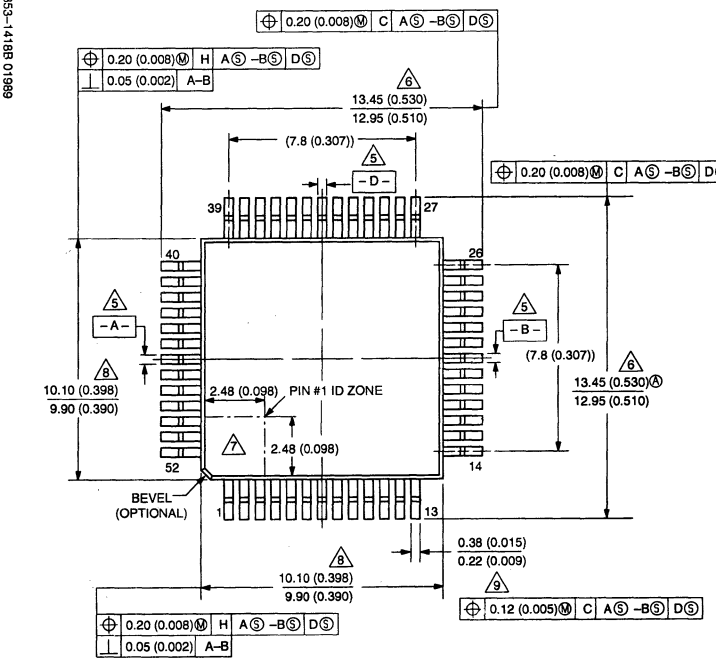
Package outlines

0416C 48-PIN (600 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



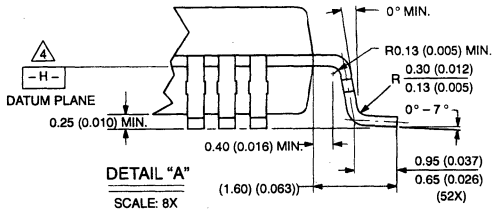
Package outlines

1418B 52-PIN PLASTIC QUAD FLAT PACK (B) PACKAGE



NOTES:

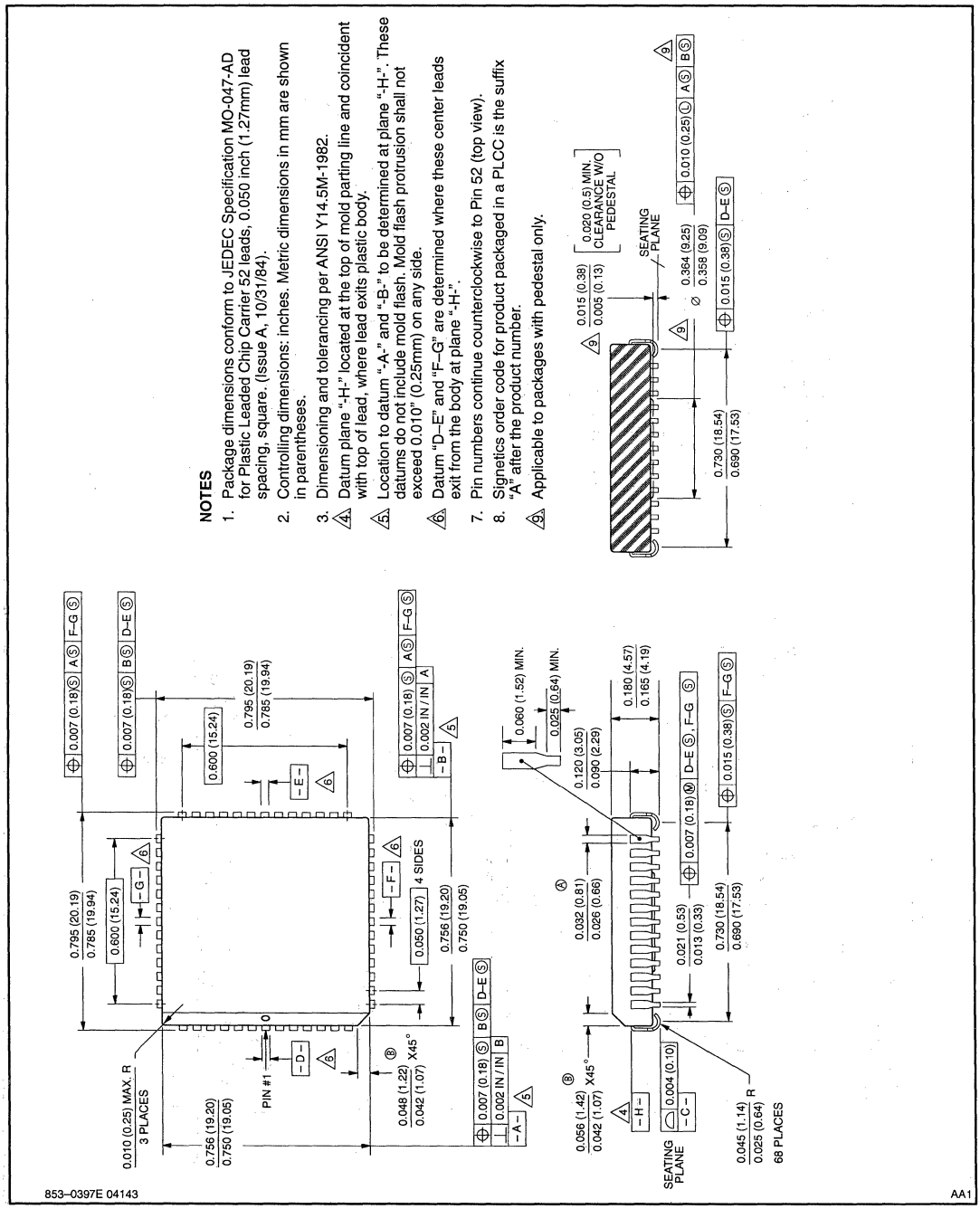
1. Package dimensions conform to JEDEC registration MO-108-1990.
2. Controlling dimensions: millimeters. Dimensions in inches are shown in parentheses.
3. Dimension and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" is located at the mold parting line and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
5. Datums "A-B" and "D" to be determined at datum plane "H".
6. To be determined at seating plane "C".
7. Details of Pin 1 identifier are optional but must be located within the zone indicated.
8. These dimensions to be determined at datum plane "H".
9. Lead width does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm / 0.003" total in excess of this dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.



853–1418B 01989

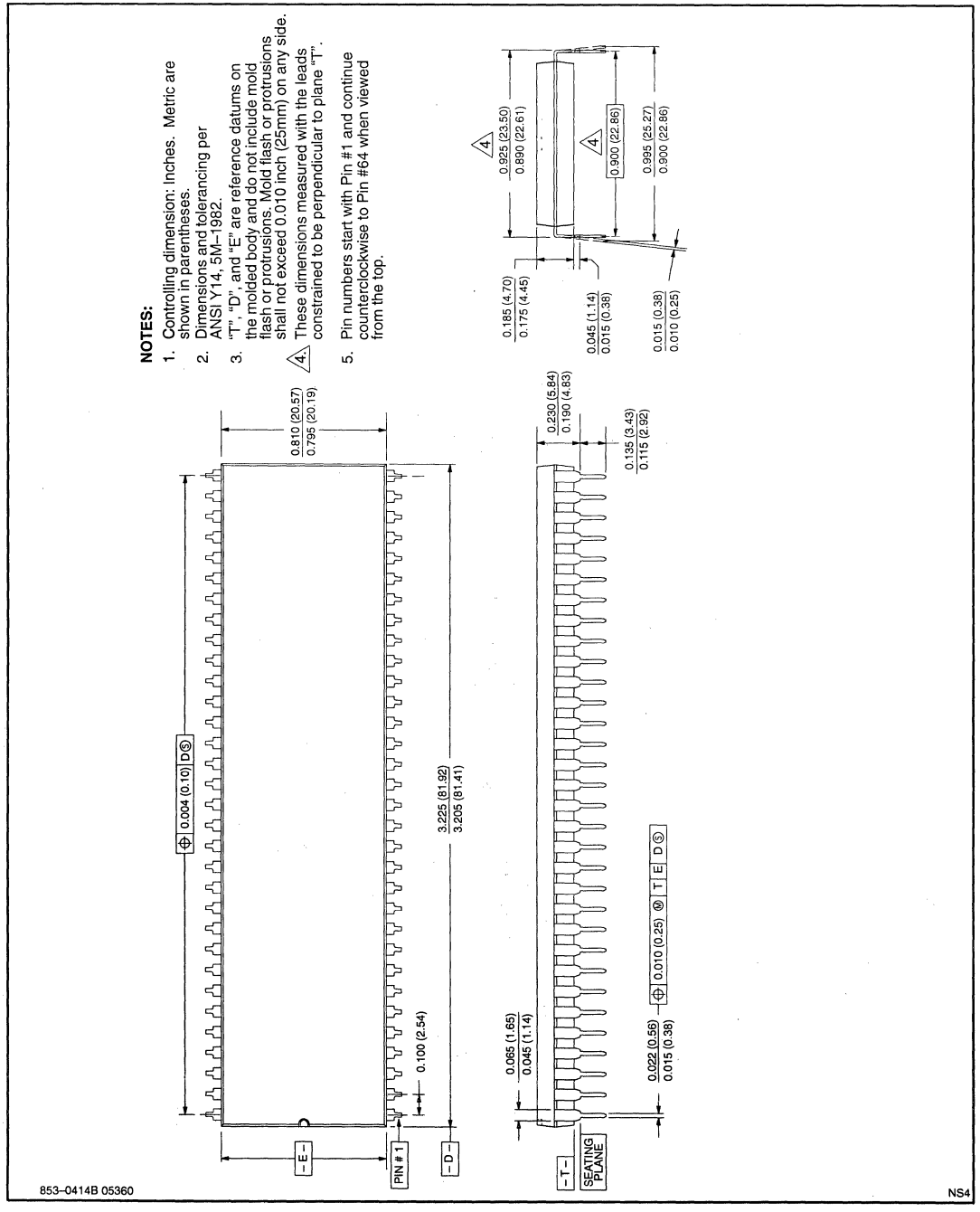
Package outlines

0397E 52-PIN PLASTIC LEADED CHIP CARRIER (A) PACKAGE



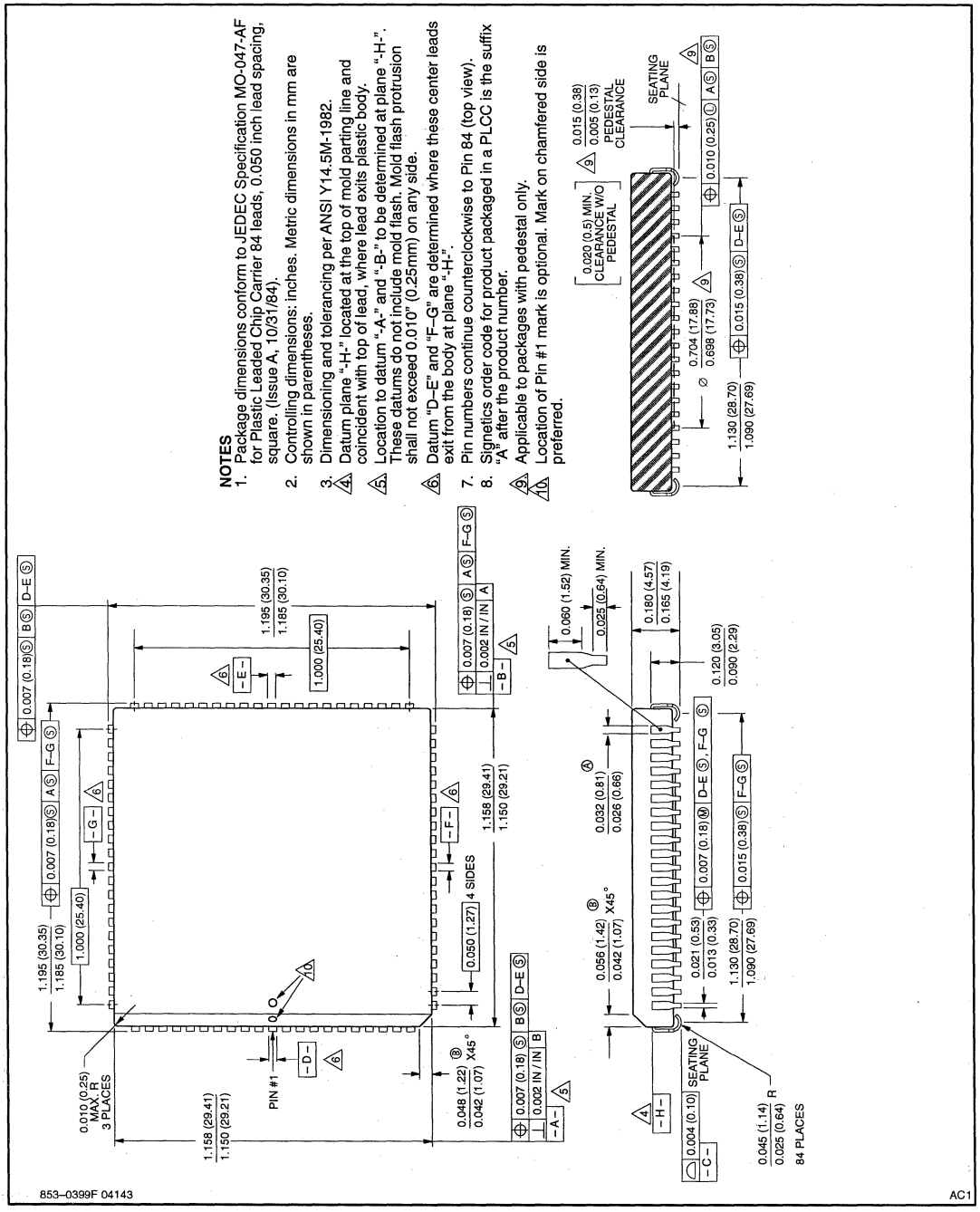
Package outlines

0414B 64-PIN (900 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE



Package outlines

0399F 84-PIN PLASTIC LEADED CHIP CARRIER (A) PACKAGE



Package outlines

SOLDERING

Plastic mini-packs, PLCC and QFP

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260°C, and maximum duration of package immersion in solder bath is 10 seconds; if allowed to cool to less than 150°C, within 6 seconds. Typical dwell time is 4 seconds at 250°C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapor-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250°C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45°C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 seconds at up to 300°C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 seconds at between 270 and 320°C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260°C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating place, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply the soldering iron below th seating place (or not more than 2 mm above it). If its temperature is below 300°C, it must not be in contact for more than 10 seconds; if between 300 and 400°C, for not more than 5 seconds.

SOLDERING

Tab modules

FLUXING

Use a flux that does not have to be removed, or a water-soluble flux.

SOLDERING

The reflow soldering method using a pulse-heated tool is usually suitable. Limit the soldering operation to 3 seconds at 250°C at the leads.

CLEANING

Avoid cleaning if possible. If cleaning is necessary, use cold or hot water. A detergent may be added to the water. Finally rinse with de-ionized water.

Do **not** use ultrasonic cleaning methods as these may damage the inner or outer leads.

Do **not** use solvents.

Section 9
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03/28/94

Data handbook system — Appendix A

DATA HANDBOOK SYSTEM

Philips Semiconductors data handbooks contain all pertinent data available at the time of publication and each is revised and reissued regularly.

Loose data sheets are sent to subscribers to keep them up-to-date on additions or alterations made during the lifetime of a data handbook.

Catalogs are available for selected product ranges (some catalogs are also on floppy discs).

Our data handbook titles are listed here.

Integrated Circuits

Book	*Title*
IC01	Semiconductors for Radio and Audio Systems
IC02	Semiconductors for Television and Video Systems
IC03	Semiconductors for Telecom Systems
IC04	CMOS HE4000B Logic Family
IC05	Advanced Low-power Schottky (ALS) Logic Series
IC06	High-speed CMOS Logic Family
IC08	100K ECL Logic Families
IC10	Memories
IC11	General-purpose/Linear ICs
IC12	Display Drivers and Microcontroller Peripherals (planned)
IC13	Programmable Logic Devices (PLD)
IC14	8048-based 8-bit Microcontrollers
IC15	FAST TTL Logic Series
IC16	ICs for Clocks and Watches
IC18	Semiconductors for In-car Electronics and General Industrial Applications (planned)
IC17	RF/Wireless Communications
IC19	Semiconductors for Datacom: LANs, UARTs, Multi-protocol Controllers and Fibre Optics
IC20	80C51-based 8-bit Microcontrollers
IC21	68000-based 16-bit Microcontrollers (planned)
IC22	ICs for Multi-media Systems (planned)
IC23	QUBiC Advanced BiCMOS Bus Interface Logic ABT, MULTIBYTE™
IC24	Low Voltage CMOS & BiCMOS Logic

Discrete Semiconductors

Book	*Title*
SC01	Diodes
SC02	Power Diodes
SC03	Thyristors and Triacs
SC04	Small-signal Transistors
SC05	Low-frequency Power Transistors and Hybrid IC Power Modules
SC06	High-voltage and Switching NPN Power Transistors
SC07	Small-signal Field-effect Transistors
SC08a	RF Power Bipolar Transistors
SC08b	RF Power MOS Transistors
SC09	RF Power Modules
SC10	Surface Mounted Semiconductors
SC13	Power MOS Transistors including TOPFETs and IGBTs
SC14	RF Wideband Transistors, Video Transistors and Modules
SC15	Microwave Transistors
SC16	Wideband Hybrid IC Modules
SC17	Semiconductor Sensors

Professional Components

PC01	High-power Klystrons and Accessories
PC06	Circulators and Isolators

MORE INFORMATION FROM PHILIPS SEMICONDUCTORS?

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Data handbook system — Appendix A

OVERVIEW OF PHILIPS COMPONENTS DATA HANDBOOKS

Our sister product division, Philips Components, also has a comprehensive data handbook system to support their products. Their data handbook titles are listed here.

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Book	*Title*
DC01	Colour Display Components Colour TV Picture Tubes and Assemblies Colour Monitor Tube Assemblies
DC02	Monochrome Monitor Tubes and Deflection Units
DC03	Television Tuners, Coaxial Aerial Input Assemblies
DC05	Flyback Transformers, Mains Transformers and General-purpose FXC Assemblies

Magnetic Products

MA01	Soft Ferrites
MA03	Piezoelectric Ceramics Specialty Ferrites
MA04	Dry-reed Switches

Passive Components

PA01	Electrolytic Capacitors
PA02	Varistors, Thermistors and Sensors
PA03	Potentiometers and Switches
PA04	Variable Capacitors
PA05	Film Capacitors
PA06	Ceramic Capacitors
PA07	Quartz Crystals for Special and Industrial Applications
PA08	Fixed Resistors
PA10	Quartz Crystals for Automotive and Standard Applications
PA11	Quartz Oscillators

Professional Components

PC04	Photo Multipliers
PC05	Plumbicon Camera Tubes and Accessories
PC07	Vidicon and Newvicon Camera Tubes and Deflection Units
PC08	Image Intensifiers
PC12	Electron Multipliers

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