MICROPERIPHERAL PRODUCTS
INTEGRATED CIRCUITS

silicon systems®

1989 DATA BOOK

Silicon Systems, Inc.

Silicon Systems, Inc. specializes in the marketing, design, and manufacturing of Application Specific Integrated Circuits (ASICs). It offers a sophisticated line of custom and standard ICs primarily aimed at the microperipheral, communications and industrial marketplace.

The Company was founded in 1972 and is headquartered in Tustin, California, 30 miles south of Los Angeles. At first it offered only design services, but in the mid-70s began to subcontract the manufacturing of finished products. In 1981, through initial public funding (SLCN/NASDAQ), the Company launched its own wafer manufacturing capability, which was completed and put into production in 1982. A fully integrated assembly and test operation in Singapore was implemented in 1985. In August, 1988, Silicon Systems announced the acquisition of its second wafer fabrication facility and opened its fourth design center in Santa Cruz, California.

Present industry projections show the worldwide semiconductor market growing to $40 billion in 1990, a compound annual growth rate of more than 15 percent. Within that marketplace, the ASIC segment is expected to grow in excess of 30 percent annually; whereas general purpose products growth rates are forecasted at 13 percent. Silicon Systems has positioned its capabilities to participate in the communications, computer and industrial ASIC market segments. The Company achieved an $81.7 million sales level in 1987 and is expected to reach $110-120 million in 1988. In recognition of its first $100 million year, the Company announced in August, 1988, its listing on the New York Stock Exchange (SIL/NYSE).

Silicon Systems possesses all the capabilities necessary to design, produce, market and deliver ASICs to its growing worldwide customer base. This includes its wafer fabs in Tustin and Santa Cruz, California; assembly and test facilities in Singapore; and Design Engineering capabilities in Tustin, Santa Cruz and Grass Valley, California, as well as Singapore.

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Numerical Index

SSI Device Number	Head Type	# of Channels	Max Input Noise nV/√Hz	Max Input Capacitance (pF)	Read Gain (typ)	Write Current Range (mA)	Power Supplies	Read/Write Data Port(s)
HDD READ/WRITE AMPLIFIERS								
SSI 32R104C	Ferrite	4	2.4	23	35	15 to 45	+6V,-4V	Differential, Bi-directional
SSI 32R104CLN	Ferrite	4	1.7	23	35	15 to 45	+6V,-4V	Differential, Bi-directional
SSI 32R114	Thin Film	4	1.1	65	123	55 to 110	±5V	Differential/Differential
SSI 32R115	Ferrite	2, 4, 5	1.8	20	40	30 to 50	±5V	Differential, Bi-directional
SSI 32R117	Ferrite	2, 4, 6	2.1	23	100	10 to 50	+5V,+12V	Differential/TTL
SSI 32R117A	Ferrite	2, 4, 6	1.7	20	100	10 to 50	+5V,+12V	Differential/TTL
SSI 32R188	Ferrite	4	2.4	18	43	35 to 70	+6V,-5V	Differential, Bi-directional
SSI 32R501	Ferrite	4, 6, 8	1.5	23	100	10 to 50	+5V,+12V	Differential/TTL
SSI 32R510A	Ferrite	2, 4, 6	1.5	20	100	10 to 40	+5V,+12V	Differential/TTL
SSI 32R511	Ferrite	4, 6, 8	1.5	20	100	10 to 40	+5V,+12V	Differential/TTL
SSI 32R512	Thin Film	8, 9	0.9	32	150	10 to 40	+5V,+12V	Differential/TTL
SSI 32R514	Ferrite	2, 4, 6	1.5	20	150	10 to 40	+5V,+12V	Differential/TTL
SSI 32R515	Ferrite	9, 10	1.5	20	100	10 to 50	+5V, +12V	Differential/TTL
SSI 32R520	Thin Film	4	0.9	65	123	30 to 75	±5V	Differential/Differential
SSI 32R521	Thin Film	6	0.9	65	100	20 to 70	+5V,+12V	Differential/TTL
SSI 32R522	Thin Film	4, 6	1.0	32	100	6 to 35	+5V,+12V	Differential/TTL
SSI 32R524R	Thin Film	8	0.8	56	100	20 to 60	+5V, +12V	Differential/Differential
SSI 32R525	Thin Film	4	0.8	35	150	25 to 40	+5V, -5V	Differential/Differential

SSI Device Number	Circuit Function	Features
HDD PULSE DETECTION		
SSI 32P540	Read Data Processor	Time Domain Filter
SSI 32P541	Read Data Processor	AGC, Amplitude & Time Pulse Qualification, RLL Compatible
SSI 32P544	Pulse Detector	32P541-type pulse detector with embedded servo electronics
SSI 32P546	Pulse Detector	32P541-type pulse detector with pulse slimming compatibility
HDD DATA RECOVERY		
SSI 32D531	Data Synchronizer	Data Synchronizer/Write Precompensation
SSI 32D5321	Data Separator	Data Synchronizer/2, 7 RLL ENDEC
SSI 32D534	Data Separator	Data Synchronizer/MFM ENDEC/Write Precompensation
SSI 32D535	Data Separator	Data Synchronizer/2, 7 RLL ENDEC/Write Precompensation
SSI 32D536	Data Separator	Data Synchronizer/1, 7 RLL ENDEC/Write Precompensation
HDD HEAD POSITIONING		
SSI 32H101A	Preamplifier-Ferrite Head	AV = 93, BW = 10MHZ, e_n = 7.0 nV/√Hz
SSI 32H116	Preamplifier-Thin Film Head	AV = 250, BW = 20MHz, e_n = 0.94 nV/√Hz
SSI 32H523R	Servo Read/Write	Single-channel thin-film read/write device
SSI 32H566	Servo Read/Write	Single-channel ferrite read/write device
SSI 32H567	Servo Demodulator	Di-bit Quadrature Servo Pattern: PLL Synchronization
SSI 32H568	Servo Controller	Track & Seek Mode Operation; Microprocessor Interface
SSI 32H569	Servo Motor Driver	Head Parking, Spindle Motor Braking
HDD SPINDLE MOTOR CONTROL		
SSI 32M590	2-Phase Motor Speed Control	±0.035% Speed Accuracy; Unipolar Operation
SSI 32M591	3-Phase Motor Speed Control	±0.05% Speed Accuracy; Unipolar Operation
SSI 32M593	3-Phase Motor Speed Control	±0.037% Speed Accuracy; Bipolar Operation, 5-1/4" Drives
SSI 32M594	Motor Speed Control	±0.037% Speed Accuracy; Bipolar Operation, 3-1/2", 5-1/4" Drives
HDD CONTROLLER/INTERFACE		
SSI 32B450A	SCSI Controller	Async transfer to 2 MBPS; Initiate/Target Modes; Internal Drivers; CMOS
SSI 32B451	SCSI Controller	Async transfer to 1.5 MBPS; Internal Drivers; AIC 500L compatible
SSI 32C452	Storage Controller	20Mbits/sec; CMOS; Programmable; AIC-010 Compatible
SSI 32C452A	Storage Controller	15Mbits/sec; CMOS; Programmable; AIC-010F Compatible
SSI 32C453	Buffer Controller	Non-mux addressing to 16K; CMOS; AIC-300 Compatible
SSI 32B545	Support Logic	Includes ST506 Bus Drivers/Receivers
FLOPPY DISK DRIVES		
SSI 34D441	Data Separator	High Performance Analog Data Separator, NEC 765 Compatible
SSI 34P570	Read Data Path	2 Channel Read/ Write With Read Data Path
SSI 34R575	Read/Write	2, 4 Channel Read/Write Circuit
SSI 34B580	Support Logic	Port Expander, Includes SA400 Interface Drivers/Receivers
TAPE DRIVER CIRCUITS		
SSI 35P550	Read Data Path	4 Channel Read/Write With Read Data Path

Section

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HDD READ/WRITE AMPLIFIERS

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SSI 32R104C, 32R104CL, 32R104CM, 32R104CLM, 32R108, 32R122 4-Channel Thin Film Read/Write Device

August, 1988

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DESCRIPTION

The SSI 32R104 is a monolithic bipolar integrated circuit for use in high performance disk drive systems where it is desirable to locate the control circuitry directly on the data arm. Each circuit controls four heads and has three modes of operation: Read, Write and Idle.

The SSI 32R104L is a low-noise version of the SSI 32R104 with all other parameters identical. Both are available in 24-pin flatpack, and 24-pin small outline (SOL) packages.

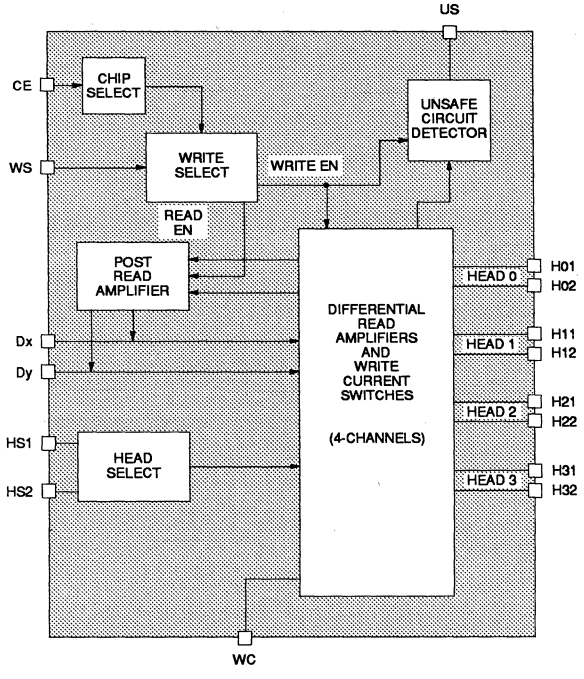
The SSI 32R108 and SSI 32R122 are identical in performance to the SSI 32R104. The SSI 32R108 is packaged in a 24-pin DIP package, while the SSI 32R122 is packaged in a 22-pin DIP.

The "M" version is functionally identical to the standard SOL device, except that the pinout is the mirror image to simplify multi-chip layouts.

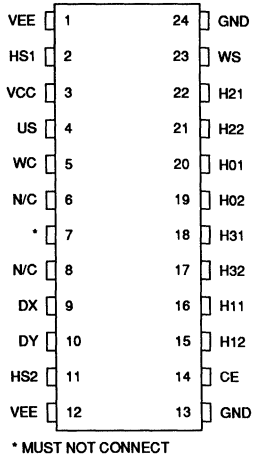
FEATURES

- IBM 3350 compatible performance
- IBM compatible power supply voltages and logic levels
- Four read/write channels
- Safety circuits

BLOCK DIAGRAM



PIN DIAGRAM



* MUST NOT CONNECT

32R104, 32R108 Pinout

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

WRITE MODE

In the write mode, the circuit functions as a current gate. Externally supplied write current is gated by the state of the head select and data inputs to one side of one head. Head voltage swings are monitored by the head transition detect circuit. Absence of proper head voltage swings, indicating an open or short on either side of the head or absence of write current, will cause a fault current to flow into the unsafe pin.

READ MODE

In the read mode, the circuit functions as a low noise differential amplifier. The state of the head select inputs determines which amplifier is active. Data is differentially read from one of four heads and an open collector differential signal is put across the Data X and Data Y pins. If a fault condition exists such that write current is applied to the chip when the chip is in read mode, the write current will be drawn from the unsafe pin and the fault will be detected.

HEAD SELECT TABLE

HEAD SELECTED	HS2	HS1
0	1	1
1	1	0
2	0	1
3	0	0

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 5.7 ≤ VCC ≤ 6.7, -4.2 ≤ VEE ≤ -3.8, 0° ≤ Tj, ≤ 110 °C.

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
Positive Supply Voltage VCC	7.0	V
Negative Supply Voltage, VEE	-5.5	V
Storage Temperature	-65 to 150	°C
Input Voltages		
Head Select (HS)	VEE -0.3 to + 0.3	V
Unsafe (US)	-0.3 to VCC +0.5	V
Write Current (WC)	VEE -2 to + 0.3	V
Data (Dx, Dy)	VEE -0.3 to + 0.3	V
Chip Enable (CE)	VEE -0.3 to VCC +0.5	V
Write Select (WS)	-0.3 to VCC + 0.3	V

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Positive Supply Current (ICC)	Read/Write	11.5		23	mA
Positive Supply Current (ICC)	Idle			75 + ICE	mA
Negative Supply Current (IEE)	Read/Write			70	mA
Negative Supply Current (IEE)	Idle			52	mA

LOGIC SIGNALS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Chip Enable Low voltage (VLCE)	Read/Write	0.0		0.7	V
Chip Enable High Voltage (VHCE)	Idle	VCC –1.0		VCC +0.3	V
Chip Enable Low Current (ILCE)	VCE = 0.0V	-1.45		-0.47	mA
Chip Enable High Current (IHCE1)	VCE = VCC – 1.0	-350		-100	µA
Chip Enable High Current (IHCE2)	VCE = VCC + .3V			+100	µA
Write Select High Voltage (VHWS)	Write/Idle	3.2		3.8	V
Write Select Low Voltage (VLWS)	Read/Idle	-0.1		0.1	V
Write Select High Current (IHWS)	Write/Idle, VWS = 3.8V				
	Transition unsafe current off	0.6		3.2	mA
	Transition unsafe on	0.6		4.2	mA
Write Select Low Current (ILWS)	Read/Idle, VWS = 3.8V			0.1	mA
Head Select High Voltage (VHHS)		-1.12		-0.72	V
Head Select Low Voltage (VLHS)		-2.38		-1.51	V
Head Select High Current (IHHS)				240	µA
Head Select Low Current (ILHS)				60	µA
Total Head Input Current	Sum of all head input currents with IWC = 0				
	Write, VCT = 3.5V			3.7	mA
	Read, VCT = 0.0V			0.16	mA
	Idle			1.25	mA

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Gain	Vin = ImV p-p, 0VDC, f = 300 KHz				
	Tj = 22 °C	28		43	V/V
	Tj = 0 °C	28		46	V/V
	Tj = 110 °C	22.2		43	V/V
Common Mode Rejection Ratio	Vin = 100 mVpp, 0VDC, f ≤ 5 MHz	45			dB
Power Supply Rejection Ratio	Vin = 0V, f ≤ 5 MHz ΔVCC or ΔVEE = 100 mVpp	45			dB
Bandwidth	Zin = 0Ω, Vin = 1 mVPP, f midband = 300 KHz	30			MHz
Input Noise	Vin = 0V, Zin = 0Ω, Power Bandwidth = 15 MHz			9.3	μVRMS
Input Noise (SSI 32R104L)	Vin = 0V, Zin = 0Ω, Power Bandwidth = 15 MHz			6.6	μVRMS
Input Current	Vin = 0V			26	μA
Differential Input Capacitance	Vin = 0V			23.5	pF
Differential Input Resistance	Vin = 0V				
	Tj = 22 °C	585		915	Ω
	Tj = 0 °C	565		915	Ω
	Tj = 110 °C	585		1070	Ω
Output Offset Voltage	Zin = 0			120	mV
Common Mode Output Voltage	Vin = 0	-0.78		-0.32	V
Unsafe Current	Write Current = 0 mA			0.1	mA
	Write Current = -45 mA	40		45	mA
Dynamic Range	DC input voltage where AC gain falls to 90% of 0VDC input value. Measured with 0.5 mVpp AC input, Tj = 30 °C	2.0			mVp
Channel Separation	Vin = 1 mVpp, 0VDC, f = 5 MHz 3 channels driven	40			dB

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Input Voltage		0.175			V
Single Ended Input voltage		-0.68		-0.45	V
Write Current		-45			mA
Current Gain	IWC = -45 mA	0.95		1.0	
Write Current Voltage	IWC = -45 mA	VEE+0.25		VEE+1.0V	V
Unsafe Voltage	IUS = +45 mA	4		VCC +.3	V
Head Center Tap Voltage		3.2		3.8	V
Differential Head Voltage	IWC = -45 mA, Lh = 10 µH	5.7		7.2	Vp
Single Ended Head Voltage	IWC = -45 mA, unselected heads at 3.5V Selected Side of Selected Head Current = 0 mA	0.0		0.9	V
	= 90 mA	1.4+VCC		3.7+VCC	V
Unsafe Current	IWC = -30 mA, f = 2 MHz:			1.0	mA
	Lh = 9 µH, VUS = 5.0V – 6.3V,	15		45	mA
	Lh = 0, IWC = 45 mA, Rh = ∞ one side of head only	15		45	mA
Unselected Head Current	IWC = -45 mA, f = 2 MHz, Lh = 9.5 µH			2.0	mAp
DX DY Input Current		-2.0		2.0	mA

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Idle to Read/Write Transition Time				0.5	µs
Read/Write to Idle Transition Time				0.5	µs
Read to Write Transition Time				0.5	µs
Write To Read Transition Time				0.5	µs
Head Select Switching Delay				50.0	ns
Head Current Transition Time	IWC = -45 mA, Lh = 0, f = 5 MHz			15	ns
Head Current Switching Delay Time	IWC = -45 mA, Lh = 0, f = 5 MHz			15	ns
Head Current Switching Hysteresis	IWC = -45 mA, Lh = 0, f = 5 MHz Data rise and fall time ≤ 1 nSec			2	ns
Unsafe Switching Delay Time Delay Time	IWC = -30 mA, f = 2 MHz; Lh = 9 µH			1	µs
	Lh = 0 µH	0.8		5.1	µs

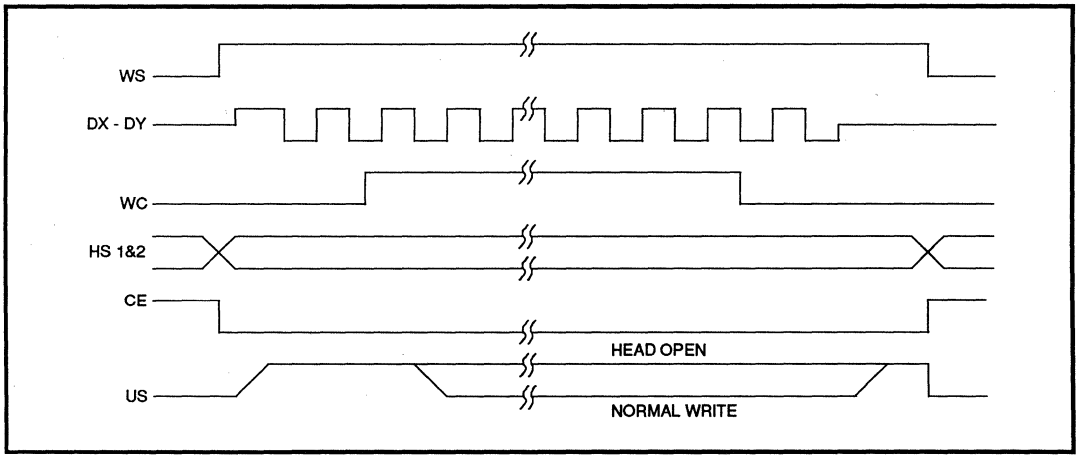
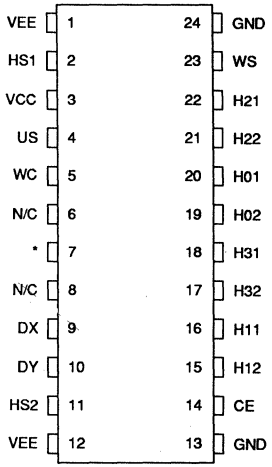


FIGURE 1: Write Mode Timing System

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



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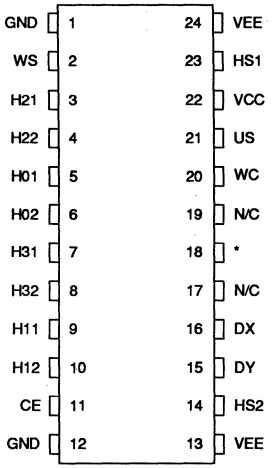
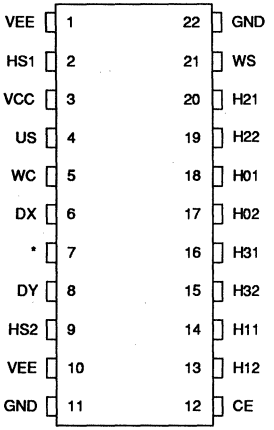
32R104, 32R108
24-Pin



* MUST NOT CONNECT

32R104M
24-Pin SOL



* MUST NOT CONNECT

32R122
22-Pin PDIP

THERMAL CHARACTERISTICS: Ø ja

22-Lead	PDIP	65°C/W
24-Lead	PDIP	115°C/W
24-Lead	SOL	80°C/W
24-Lead	Flatpack	105°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32R104C Read/Write IC		
24-Lead Flatpack	SSI 32R104C-F	SSI 32R104C-F
24-Lead SOL	SSI 32R104C-CL	SSI 32R104C-CL
SSI 32R104CL Low Noise Read/Write IC		
24-Lead Flatpack	SSI 32R104CL-F	SSI 32R104CL-F
SSI 32R104CM Mirror Image Read/Write IC		
24-Lead SOL	SSI 32R104CM-CL	SSI 32R104CM-CL
SSI 32R108 Read/Write IC		
24-Lead PDIP	SSI 32R108C-P	SSI 32R108C-P
SSI 32R122 Read/Write IC		
22-Lead PDIP	SSI 32R122B-P	SSI 32R122B-P

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NOTES:

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INNOVATORS IN INTEGRATION

SSI 32R114
4-Channel Thin Film Read/Write Device

Not Available. Please see SSI 32R520 & SSI 32R525.

August, 1988

1

DESCRIPTION

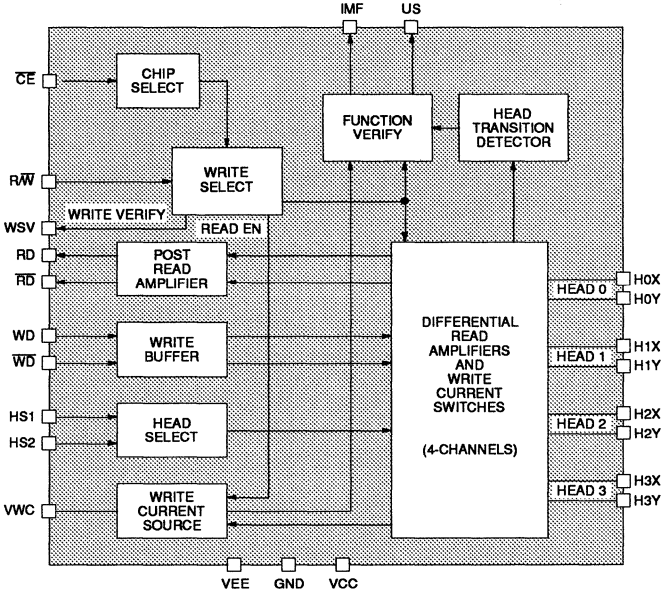
The SSI 32R114 is an integrated read/write circuit designed for use with non-center tapped thin film heads in disk drive systems. Each chip controls four heads and has three modes of operation: read, write, and idle. The circuit contains four channels of read amplifiers and write drivers and also has an internal write current source.

A current monitor (IMF) output is provided that allows a multichip enable fault to be detected. An enabled chip's output will produce one unit of current. An open collector output, write select verify (WSV), will go low if the write current source transistor is forward biased. The circuit operates on +5 volt, and -5 volt power and is available in a 24-pin flatpack.

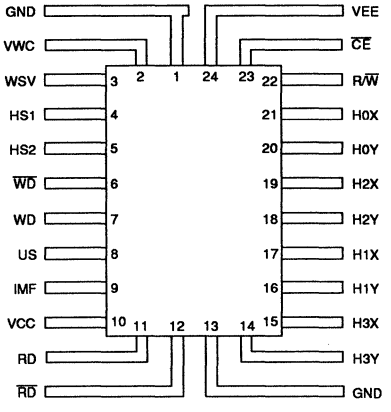
FEATURES

- **Thin film head compatible performance**
- **Four Read/Write channels**
- **TTL - compatible logic levels**
- **Operates on standard +5V, -5V power supplies**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

WRITE MODE

In the write mode (R/$\overline{W}$ and $\overline{CE}$ low) the circuit functions as a differential current switch. The Head Select Inputs (HS1 and HS2) determine the selected head. The Write Data Inputs (WD, $\overline{WD}$) determine the polarity of the head current. The write current magnitude is adjustable by an external 1% resistor, Rx from VWC to VCC, where:

$$I_W = \frac{K_W}{R_X\left(1+\frac{R_h}{R_d}+\frac{R_h}{1_k}\right)} - 0.7\,mA$$

Where Kw = Current Gain Factor = 130 Amp-Ohms

Rh = Head plus External Wire Resistance

Rd = Damping Resistance

READ MODE

In the Read Mode, (R/$\overline{W}$ high and $\overline{CE}$ low), the circuit functions as a differential amplifier. The amplifier input terminals are determined by the Head Select inputs.

HEAD SELECT TABLE

HEAD SELECTED	HS2	HS1
0	0	0
1	1	0
2	0	1
3	1	1

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 4.75 ≤ VCC ≤ 5.25, -5.5 ≤ VEE ≤ -4.95V, 25° ≤ T (junction) ≤ 125°C.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive Supply Voltage, Vcc	6	V
Negative Supply Voltage, VEE	-6	V
Operating Junction Temperature	25 to 125	°C
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering, 10 sec)	260	°C
Input Voltages		
Head Select (HS)	-0.4 to Vcc + 0.3	V
Chip Enable ($\overline{CE}$)	-0.4 to Vcc+ 0.3	V
Read Select (R/$\overline{W}$)	-0.4V or -2 mA to Vcc + 0.3	V
Write Data (WD, $\overline{WD}$)	VEE to 0.3	V
Head Inputs (Read Mode)	-0.6 to +0.4	V
Outputs		
Read Data (RD, $\overline{RD}$)	0.5 to Vcc + 0.3	V
Write Unsafe (WUS)	-0.4 to Vcc + 0.3 and 20 mA	V
Write Select Verify (WSV)	-0.4 to Vcc + 0.3 and 20 mA	V

ABSOLUTE MAXIMUM RATINGS (Continued)

PARAMETER	RATING	UNIT
Outputs (Continued)		
Current Monitor (IMF)	-0.4 to Vcc + 0.3	V
Current Reference (VWC)	VEE to Vcc + 0.3 and 8 mA	V
Head Outputs (Write Mode)	Iw max = 150	mA

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Power Dissipation	All modes, 25 ≤ Tj ≤ 100			612+6.7Iw	mW
	100° ≤ Tj ≤ 125 °C			563+6.7Iw	mW
Positive Supply Current (ICC)	Idle Mode			10+ Iw/19	mA
Positive Supply Current (ICC)	Read Mode			40+ Iw/19	mA
Positive Supply Current (ICC)	Write Mode			38+ Iw/19	mA
Negative Supply Current (IEE)	Idle Mode	-12– Iw/19			mA
Negative Supply Current (IEE)	Read Mode	-66– Iw/19			mA
Negative Supply Current (IEE)	Write Mode	-75–1.16Iw			mA

LOGIC SIGNALS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Chip Enable Low Voltage (VLCE)	Read or Write Mode			0.8	V
Chip Enable High Voltage (VHCE)	Idle Mode	2.0			V
Chip Enable Low Current (ILCE)	VLCE = 0V	-1.60			mA
Chip Enable High Current (IHCE)	VHCE = 2.0V			-0.3	mA
Read Select High Voltage (VHR/W)	Read or Idle Mode	2.0			V
Read Select Low Voltage (VLR/W)	Write or Idle Mode			0.8	V
Read Select High Current (IHR/W)	VHR/W = 2.0V			0.015	mA

LOGIC SIGNALS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Read Select Low Current (ILR/W)	VLR/W = 0V	-0.015			mA
Head Select High Voltage (VHHS)		2.0			V
Head Select Low Voltage (VLHS)				0.8	V
Head Select High Current (IHHS)	VHHS = VCC			0.25	mA
Head Select Low Current (ILHS)	VLHS = 0V	-0.1		0.25	mA
WUS, WSV Low Level Voltage	ILUS = 8 mA (denotes safe condition)			0.5	V
WUS, WSV High Level Current	VHUS = 5.0V (denotes unsafe condition)			100	µA
IMF on Current		2.20		3.70	mA
IMF off Current				0.02	mA
IMF Voltage Range		0		VCC + 0.3	V

READ MODE

Tests performed with 100Ω load resistors from RD and $\overline{RD}$ through series isolation diodes to VCC.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Voltage Gain	Vin = 1m Vpp, f = 300 KHz	75		170	V/V
Voltage Bandwidth (-3dB)	Zs < 5Ω, Vin = 1m Vpp f midband = 300 KHz	45			MHz
Input Noise Voltage	Zs = 0Ω , Vin = 0V, Power Bandwidth = 15 MHz			1.1	$nV\sqrt{Hz}$
Differential Input Capacitance	Vin = 0V, f = 5 MHz			65	pF
Differential Input Resistance	Vin = 0V, f = 5 MHz	45		96	Ω
Input Bias Current (per side)	Vin = 0V			0.17	mA
Dynamic Range	DC input voltage where AC gain falls to 90% of the gain with .5m Vpp input signal	-3.0		3.0	mV
CMRR	Vin = 100m Vpp, 0V DC 1 MHz ≤ f ≤a 10 MHz	54			dB
	10 MHz ≤ f ≤ 20 MHz	48			dB
Power Supply Rejection Ratio	VCC or VEE = 100m Vpp 1 MHz ≤ f ≤ 10 MHz	54			dB
	10 MHz ≤ f ≤ 20 MHz	36			dB

READ MODE (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Channel Separation	The three unselected channels are driven with Vin = 100m Vpp 1 MHz ≤ f ≤ 10 MHz	43			dB
	10 MHz ≤ f ≤ 20 MHz	37			dB
Output Offset Voltage		-360		360	mV
Output Leakage Current	Idle Mode			0.01	mA
Output Common Mode Voltage		VCC - 1.1		VCC - 0.3	V
Single Ended Output Resistance		10			KΩ
Single Ended Output Capacitance				10	pF

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Current Range (Iw)		55		110	mA
Current Tolerance	Current set to nominal value by Rx, Rh= 7Ω ± 10%, Tj = 50 °C, Rd = 59Ω	-8		+8	%
(Iw) (Rh) Product		0.24		1.30	V
Differential Head Voltage Swing	Iw = 100 mA, Lh = 0.2 µH Rh = 10Ω	3.8			Vpp
Unselected Head Transient Current	Iw = 100 mA, Lh = 0.2 µH, Rh = 10Ω, Non adjacent heads tested to minimize external coupling effects			2	mAp
Head Differential Load Resistance, Rd		48		97	Ω
Head Differential Load Capacitance				30	pF
Differential Data Voltage, (WD – $\overline{WD}$)		0.20			V
Data Input Voltage Range		-1.87		+0.1	V
Data Input Current (per side)	Chip Enabled			150	µA
Data Input Capacitance	Per side to GND			10	pF

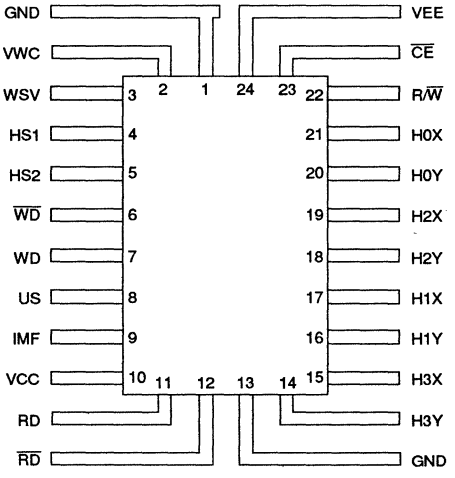
SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Idle to Read/Write Transition Time				1.0	µs
Read/Write to Idle Transition Time				1.0	µs
Read to Write Transition Time	VLCE = 0.8V, Delay to 90% of Iw			0.6	µs
Write to Read Transition Time	VLCE = 0.8V, Delay to 90% of 20 MHz Read Signal envelope, Iw decay to 10%			1.0	µs
Head Select Switching Delay	Read or Write Mode			0.40	µs
Shorted Head Current Transition Time	Iw = 100 mA, Lh = < 0.05 µH, Rh =0			13	ns
Shorted Head Current Switching Delay Time	Iw = 100 mA, Lh < 0.05 µH, Rh = 0, measured from 50% of input to 50% of current change			18	ns
Head Current Switching Time Symmetry	Iw = 100 mA, Lh = 0.2 µH, Rh = 10Ω, WD & $\overline{WD}$ transitions 2 ns, switching time symmetry 0.2 ns			1.5	ns
WSV Transition Time	Delay from 50% of write select swing to 90% of final WSV voltage, Load = 2KΩ // 20 pF			1.0	µs
Unsafe to Safe Delay After Write Data Begins (WUS)	f(data) = 10 MHz			1.0	µs
Safe to Unsafe Delay, (WUS)	Non-switching write data, no write current, or shorted head close to chip	0.6		3.6	µs
Safe to Unsafe Delay, (WUS)	Head open or head select input open			0.6	µs
IMF Switching Time	Delay from 50% of CE to 90% of final IMF current			1.0	µs

PACKAGE PIN DESIGNATIONS
(TOP VIEW)

THERMAL CHARACTERISTICS: Ø ja

24-Pin Flatpack	144°C/W (Still Air)
	30°C/W



24-Pin Flatpack

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32R114 24-Pin Flatpack	SSI 32R114-F	SSI 32R114-F

silicon systems™
Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

NOTES:

SSI 32R115
2, 4, 5-Channel Read/Write Device

August, 1988

1

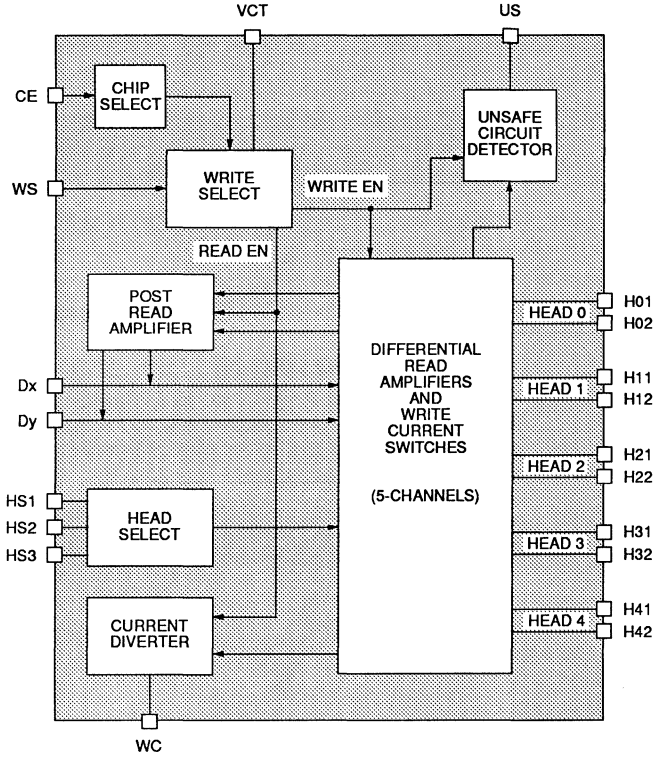
DESCRIPTION

The SSI 32R115 is a monolithic bipolar integrated circuit designed for use with 8-inch and 5-1/4-inch Winchester disk drive magnetic recording heads. The circuit interfaces with up to five magnetic recording heads providing the required read/write electronic functions as well as various control and data protect functions. The circuit operates on +5 volt and -5 volt (or -5.2 volt) power and is available in a variety of packages.

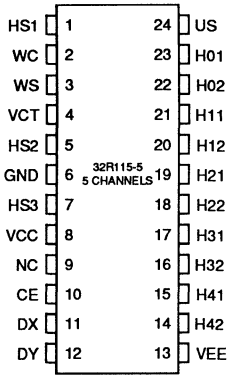
FEATURES

- Electrically compatible with 8-inch and 5-1/4-inch Winchester disk drive magnetic recording heads
- Supports up to five recording heads per circuit
- Detects and indicates unsafe write conditions
- On-chip current diverter eliminates the need for external write current switching
- Control signals are TTL compatible
- Operates on standard +5 volt and -5 volt (or -5.2 volt) power sources

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

WRITE MODE

With both the chip enable and write select signals activated, SSI 32R115 is switched to the write mode and the circuit operates as a differential current switch. The center tap head voltage (VCT) is turned on, the unsafe circuit detector is activated, and the current diverter is disabled. The head select signals (HS1, HS2, HS3) select one of five differential current switches. The selected current switch senses the polarity of the data input signal (Dx–Dy) and gates write current to the corresponding side of the head (HN1 or HN2). Head overshoot voltages that occur during normal write operation are sensed to determine safe or unsafe head circuit conditions. The detector senses the following unsafe conditions: no data transitions, head open, or no write current.

READ MODE

With chip enable active and write select disabled, the SSI 32R115 is switched to the read mode and the circuit operates as a differential amplifier. The center tap head voltage is turned off, the unsafe circuit detector is deactivated, and the write current diverter is enabled. The differential head input signal (HN1–HN2), selected by the head select signals, is amplified by a differential read amplifier and appears as a differential output signal on the data lines (Dx, Dy).

During the read and idle modes, the on-chip current diverter circuit prevents write current from flowing in the head circuits. Therefore, external gating of the write current source is not required.

TABLE 1: Head Select

HEAD	HS3	HS2	HS1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0

Note: Invalid Head Select input codes (5, 6 and 7) have the effect of not selecting any heads.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
Positive Supply Voltage, VCC	6	V
Negative Supply Voltage, VEE	-6	V
Write Current (IWC)	70	mA
Operating Junction Temperature	25 to 135	°C
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering, 10 SEC)	260	°C
INPUT VOLTAGES		
Head Select (HS)	-0.4 to VCC +0.3	V
Unsafe (US) (IHUS ≤ 15 mA)	-0.3 to VCC +0.3	V
Write Current (WC) Voltage in read idle modes. (Write mode must be current limited to -70 mA)	VEE -0.3 to 0.3	V

ABSOLUTE MAXIMUM RATINGS (Continued)

PARAMETER	RATING	UNIT
INPUT VOLTAGES (Continued)		
Data (Dx, Dy)	VEE to 0.3	V
Chip Enable ($\overline{CE}$)	-0.4 to VCC +0.3	V
Write Select ($\overline{WS}$)	-0.4 to VCC +0.3	V

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
DC Supply Voltage	VCC	4.75	5	5.25	V
DC Supply Voltage	VEE	-5.5	-5	-4.75	V
Write Current (0-pk)	IWC	-30	-45	-50	mA
Head Inductance	LH		10		µH
Junction Temperature Range	Tj	25		135	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Total Power Dissipation (PD)	Write Mode, IWC ≤ 45 mA, Tj ≥ 125 °C			700	mW
Positive Supply Current (ICC)	Read/Write Mode			35 + IWC	mA
Positive Supply Current (ICC)	Idle Mode			10	mA
Negative Supply Current (IEE)	Read/Write Mode	-65			mA
Negative Supply Current (IEE)	Idle Mode	-10			mA

LOGIC SIGNALS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Chip Enable Low voltage (VLCE)	Read or Write Mode	-0.3		0.8	V
Chip Enable Low Current (ILCE)	VLCE = 0V	-2.4			mA
Chip Enable High Current (IHCE)	Idle Mode	-250			µA
Write Select Low Voltage (VLWS)	Write or Idle Mode	-0.3		0.8	V
Write Select Low Current (ILWS)	VLWS = 0V	-3.2			mA
Write Select High Current (IHWS)	Read or Idle Mode	-250			µA

LOGIC SIGNALS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Head Select High Level Voltage (VHHS)		2.0		VCC	V
Head Select High Level Current (IHHS)	VHHS = VCC			100	µA
Head Select Low Level Voltage (VLHS)		-0.3		0.8	V
Head Select Low Level Current (ILHS)	VLHS = 0V	-0.6			mA
Unsafe Low Level Voltage (VLUS)*	ILUS = 8 mA (Denotes Unsafe Condition)			0.5	V
Unsafe High Level Current (IHUS)*	VHUS = 5.0V (Denotes Safe Condition)			100	µA
*Note: Unsafe is an open collector output.					

READ MODE (Tests performed with 50 load resistors from Dx and Dy to ground.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Common Mode Range		-0.6		0.1	V
Total Input Bias Current	-0.6V ≤ Vin ≤ 0.1V			60	µA
Differential Voltage Gain	Vin = 1 mVpp, f = 300 KHz	26		52	V/V
Voltage Bandwidth (-3dB)	Zs ≤ 10Ω, Vin = 1 mVpp, f midband = 300 KHz	30			MHz
Input Noise Voltage	Zs = 0, Vin = 0V, Power Bandwidth = 15 MHz			7	µVrms
Differential Input Capacitance	Vin = 0, f = 5 MHz			20	pF
Differential Input Resistance (Internal Damping Resistor)	Vin =0, f = 300 KHz	560		1070	Ω
Output Offset Voltage				120	mV
Differential Head Current	IWC = 45 mA, LH = 10 µH, f = 2 MHz			2	mAp
Output Common Mode Voltage		-0.4		-.125	V
Single Ended Output Resistance	f = 300 KHz	10			KΩ
Single Ended Output Capacitance				10	pF
Dynamic Range	DC input voltage where the AC gain falls to 90% of its 0VDC input value (Measured with 0.5 mVpp AC input voltage)	2			mVp
Common Mode Rejection Ratio	Vin = 100 mVpp, 0VDC, f = 5 MHz	50			dB

READ MODE (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Power Supply Rejection Ratio	ΔVCC or ΔVEE, 100 mVpp, f = 5 MHz	45			dB
Channel Seperation	The four unselected channels are driven with Vin = 100mVpp, f = 5MHz	45			dB
Write Current Voltage	IWC = 45 mA	-2.7		-0.5	V
Total Head Input Current	IWC = 0			200	μA

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Current Gain (IH/IWC)	IWC = 45 mA, IH≙ Head Current	0.95		1.0	
Write Current Pin Voltage	IWC - 45 mA	-3.7		-1.5	V
Center Tap Head Voltage (VCT)	IWC = 45 mA	3.0		VCC -0.5	V
Differential Head Voltage Swing	3.0 ≤ VCT ≤ VCC -0.5V IWC = 45 mA, LH = 10 μH	5.7		7.7	V
Differential Data Voltage (Dx – Dy)		.175			V
Single Ended Data Input Voltage (Dx, Dy)		-0.9		0.1	V
Data Input Current	-0.9 ≤ VDx, VDy ≤ 0.1	-10		100	μA
Data Input Differential Resistance	f = 300 KHz	5			KΩ
Data Input Capacitance				10	pF
Unselected Diff. Head Current	IWC = 45 mA, LH = 10 μH, f = 2 MHz			2	mAp
Write Current Range		30		50	mA
Total Head Input Current	IWC = 0			500	μA

IDLE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Write Current Pin Voltage	IWC = 45 mA	VEE			V
Differential Head Current	IWC = 45 mA, LH = 10 μH, f = 2 MHz			2	mAp
Total Head Input Current	IWC = 0			500	μA

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Idle to Read/Write Transition Time				0.6	µs
Read/Write to Idle Transition Time				0.6	µs
Read to Write Transition Time	0 ≤ VLCE ≤ 0.8V (Circuit Enabled)			0.6	µA
Write to Read Transition Time	0 ≤ VLCE ≤ 0.8V (Circuit Enabled)			0.6	µs
Head Select Switching Delay Time				0.25	µs
Head Current Transition Time	(10% to 90% points) IWC = 45 mA, LH = 0H, RH = 0Ω			15	ns
Head Current Switching Delay Time ($TD_1 - TD_2$)	IWC = 45 mA, LH = 0H, RH = 0Ω, f = 5 MHz (See Figure 1)			19	ns
Head Current Switching Hysteresis TH = ($TD_1 - TD_2$)	IWC = 45 mA, LH = 0H, RH = 0Ω, f = 5 MHz, (VDx – VDy) Rise Time = 2ns (See Figure 1)			3	ns
Unsafe to Safe Delay After Write Data Begins (TD_3)	IWC = 30 mA, LH = 10 µH, f = 2 MHz (See Figure 2A)			1.0	µs
Safe to Unsafe Delay (TD_4)	LH = 10 µH, f = 2 MHz, IWC = 45 mA (See Figure 2B)	1.6		8.0	µs

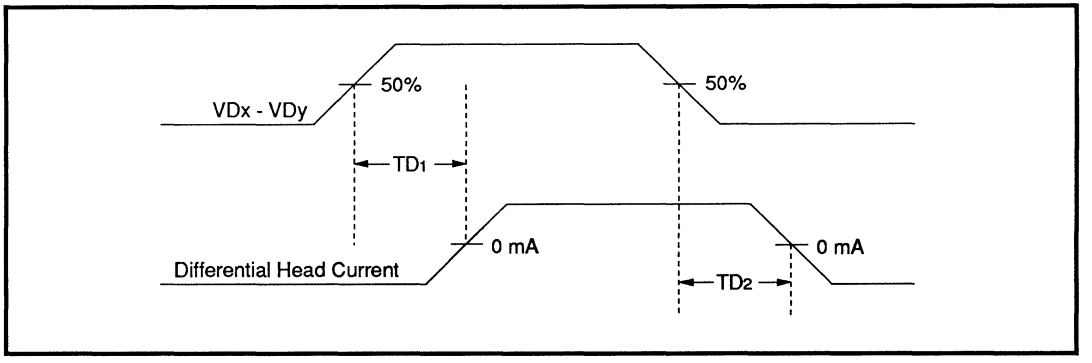


FIGURE 1: Head Current Timing

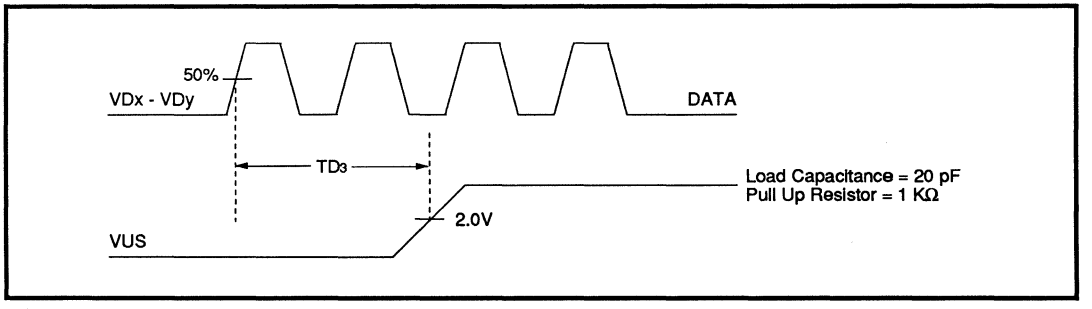


FIGURE 2A: Unsafe to Safe Timing

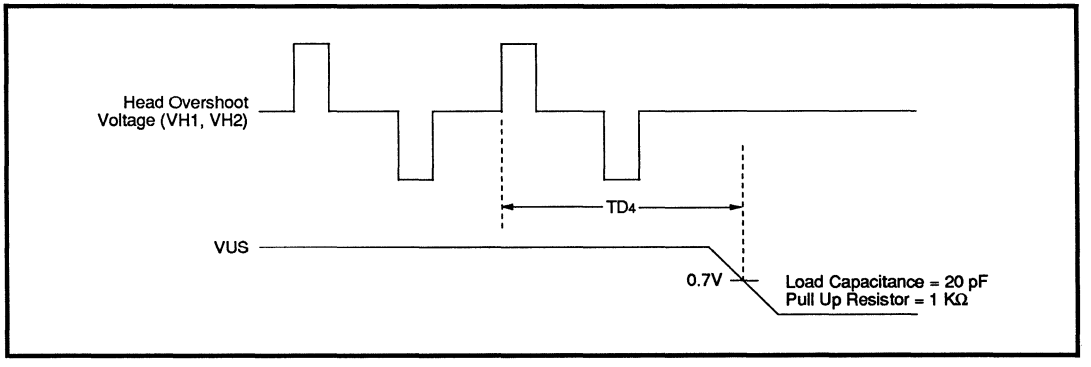
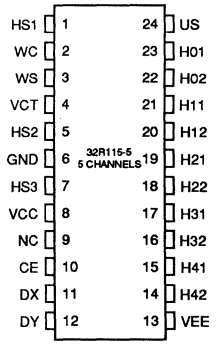


FIGURE 2B: Safe to Unsafe Timing

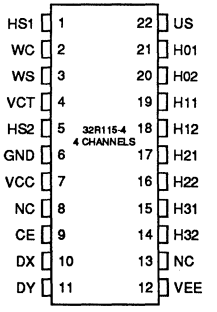
SSI 32R115
2, 4, 5-Channel
Read/Write Device

PACKAGE PIN DESIGNATIONS

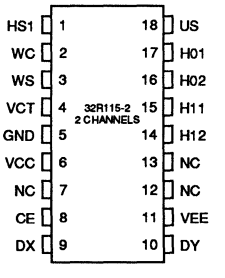
(TOP VIEW)



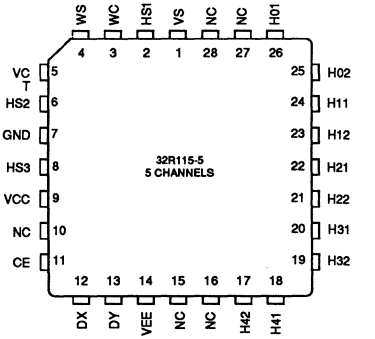
24-Pin PDIP, Flatpack, SOL



22-Pin PDIP



18-Pin PDIP



28-Pin PLCC

THERMAL CHARACTERISTICS: Øja

18-lead	PDIP	140°C/W	24-lead	PDIP	115°C/W
22-lead	PDIP	65°C/W	24-lead	Flatpack	105°C/W
28-lead	PLCC	65°C/W	24-lead	SOL	80°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32R115		
2-Channel PDIP	SSI 32R115-2P	SSI 32R115-2P
4-Channel PDIP	SSI 32R115-4CP	SSI 32R115-4CP
5-Channel PDIP	SSI 32R115-5P	SSI 32R115-5P
5-Channel SOL	SSI 32R115-5CL	SSI 32R115-5CL
5-Channel Flatpack	SSI 32R115-5F	SSI 32R115-5F
5-Channel PLCC	SSI 32R115-5CH	SSI 32R115-5CH

Silicon Systems™

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

SSI 32R117/117R
2, 4, 6 Channel Read/Write Circuit

July, 1988

1

DESCRIPTION

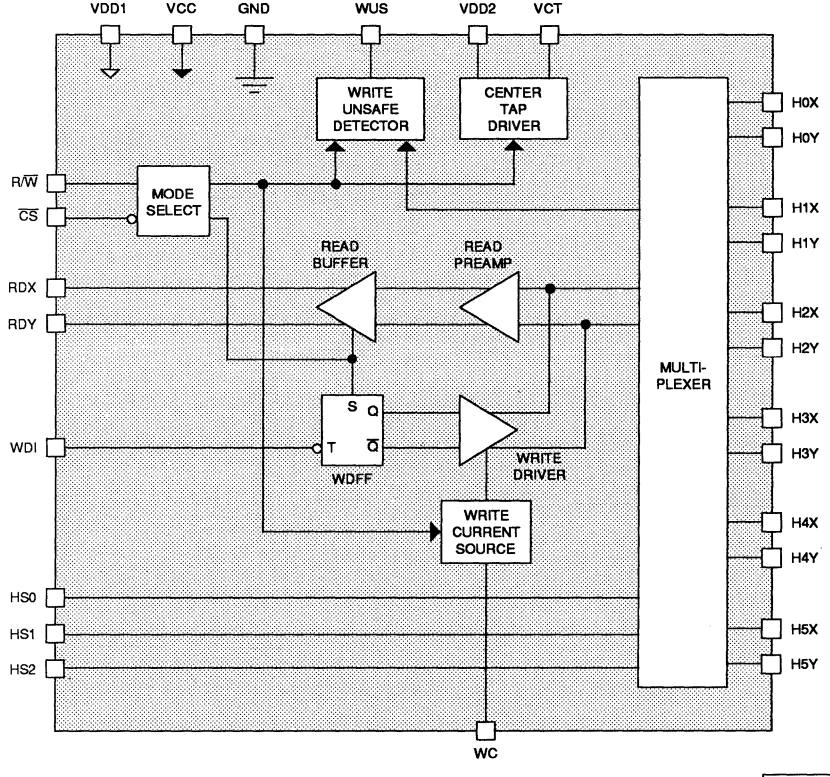
The SSI 32R117 devices are bipolar monolithic integrated circuits designed for use with center-tapped ferrite recording heads. They provide a low noise read path, write current control, and data protection circuitry for as many as six channels. The SSI 32R117 requires +5V and +12V power supplies and is available in 2, 4 or 6 channel versions with a variety of packages.

The SSI 32R117R differs from the SSI 32R117 by having internal damping resistors.

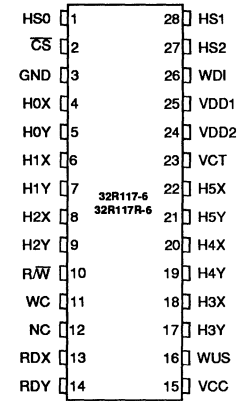
FEATURES

- **+5V, +12V power supplies**
- **Single or multi-platter Winchester drives**
- **Designed for center-tapped ferrite heads**
- **Programmable write current source**
- **Available in 2, 4 or 6 channels**
- **Easily multiplexed for larger systems**
- **Includes write unsafe detection**
- **TTL compatible control signals**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32R117 functions as a write driver or as a read amplifier for the selected head. Head selection and mode control are described in Tables 1 & 2. Both R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition.

WRITE MODE

The Write mode configures the SSI 32R117 as a current switch and activates the Write Unsafe Detector. Head current is toggled between the X- and Y-side of the recording head on the falling edges of WDI, Write Data Input. Note that a preceding read operation initializes the Write Data Flip-Flop, WDFF, to pass current through the X-side of the head. The magnitude of the write current, given by

Iw = K/Rwc, where K = Write Current Constant

is set by the external resistor, Rwc, connected from pin WC to GND.

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- Head open
- Head center tap open
- WDI frequency too low
- Device in Read mode
- Device not selected
- No write current

After the fault condition is removed, two negative transitions on WDI are required to clear WUS.

Power dissipation in write mode may be reduced by placing a resistor (RCT) between VDD1 & VDD2. The optimum resistor value is 130Ω x 50/Iw (Iw in mA). At low write currents (<15 mA) read mode dissipation is higher than write mode and RCT, though recommended, may not be considered necessary. In this case VDD2 is connected directly to VDD1.

READ MODE

In the Read mode the SSI 32R117 is configured as a low noise differential amplifier, the write current source and the write unsafe detector are deactivated, and the write data flip-flop is set. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports. They should be AC coupled to the load.

Note that the internal write current source is deactivated for both the Read and the Chip Deselect mode. This eliminates the need for external gating of the write current source.

IDLE MODE

Taking CS high selects the idle mode which switches the RDX, RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wire OR'ed.

TABLE 1: MODE SELECT

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	x	Idle

TABLE 2: HEAD SELECT

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	x	None

0 = Low level 1 = High level x = Don't care

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0-HS2	I	Head Select: selects up to six heads
$\overline{CS}$	I	Chip Select: a low level enables device
R/$\overline{W}$	I	Read/Write: a high level selects read mode
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition (open collector)
WDI	I	Write Data In: negative transition toggles the direction of the head current
H0X-H5X H0Y-H5Y	I/O	X,Y head connections
RDX, RDY	O*	X, Y Read Data: differential read signal out
WC	-	Write Current: used to set the magnitude of the write current
VCT	-	Voltage Center Tap: voltage source for head center tap
VCC	-	+5V
VDD1	-	+12V
VDD2	-	Positive power supply for the center tap voltage source
GND	-	Ground

*When more than one R/W device is used, these signals can be wire OR'ed.

ABSOLUTE MAXIMUM RATINGS (Operation above absolute maximum ratings may permanently damage the device. All voltages referenced to GND.)

PARAMETER		VALUE	UNITS
VDD1	DC Supply Voltage	-0.3 to +14	VDC
VDD2	DC Supply Voltage	-0.3 to +14	VDC
VCC	DC Supply Voltage	-0.3 to +6	VDC
VIN	Digital Input Voltage Range	-0.3 to VCC + 0.3	VDC
VH	Head Port Voltage Range	-0.3 to VDD + 0.3	VDC
Vwus	WUS Port Voltage Range	-0.3 to +14	VDC
Iw	Write Current	60	mA
Io	RDX, RDY Output Current	-10	mA
IVCT	VCT Output Current	-60	mA
Iwus	WUS Output Current	+12	mA
Tstg	Storage Temperature Range	-65 to +150	°C
Lead Temperature, PDIP, Flatpack (10 sec soldering)		260	°C
Package Temperature, PLCC, SOL (20 sec reflow)		215	°C

RECOMMENDED OPERATION CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DC Supply Voltage	VDD1		10.8	12.0	13.2	VDC
DC Supply Voltage	VCC		4.5	5.0	5.5	VDC
Head Inductance	Lh		5		15	µH
Damping Resistor	RD	32R117 only	500		2000	Ω
RCT Resistor	RCT		125.0	130	135.0	Ω
Write Current	Iw		25		50	mA
Junction Temperature Range	Tj		25		125	°C

DC CHARACTERISTICS
(Unless otherwise specified, recommended operating conditions apply.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VCC Supply Current		Read/Idle Mode			25	mA
		Write Mode			30	mA
VDD Supply Current		Idle Mode			25	mA
		Read Mode			50	mA
		Write Mode			30+Iw	mA
Power Dissipation (Tj = +125°C)		Idle Mode			400	mW
		Read Mode			600	mW
		Write Mode, Iw = 50 mA, RCT = 130Ω			700	mW
		Write Mode, Iw = 50 mA, RCT = 0Ω			1050	mW
Digital Inputs						
Input Low Voltage	VIL		-0.3		0.8	VDC
Input High Voltage	VIH		2.0		VCC+0.3	VDC
Input Low Current	IIL	VIL = 0.8V	-0.4			mA
Input High Current	IIH	VIH = 2.0V			100	µA
WUS Output	VOL	IOL = 8 mA			0.5	VDC
WUS Output	IOH	VOH = 5.0V			100	µA
Center Tap Voltage	VCT	Write Mode		6.0		VDC
		Read Mode		4.0		VDC

WRITE CHARACTERISTICS (Unless otherwise specified: recommended operating conditions apply, IW = 45 mA, Lh = 10 µH, Rd = 750Ω (32R117 only), f(Data) = 5 MHz, CL(RDX, RDY) ≤ 20 pF)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Write Current Range		10		50	mA
Write Current Constant "K"		133		147	V
Differential Head Voltage Swing		8.0			V(pk)
Unselected Head Transient Current				2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	32R117	10K			Ω
	32R117R	562		938	Ω
WDI Transition Frequency	WUS = low	250			kHz
Iwc to Head Current Gain	Iw/Iwc		20		mA/mA
Unselected Head Leakage Current	Sum of X & Y side leakage current			85	µA

READ CHARACTERISTICS
(Unless otherwise specified: recommended operating conditions apply, IW = 45 mA, Lh = 10 µH, Rd = 750Ω (32R117 only), f(Data) = 5 MHz, CL(RDX, RDY) ≤ 20 pF, Vin is referenced to VCT)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain	Vin = 1 mVpp @ 300 KHz RL(RDX), RL(RDY) = 1 KΩ	80		120	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10%, Vin = Vi + 0.5 mVpp @ 300 KHz	-3		+3	mV
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	30			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			2.1	nV/√Hz
Differential Input Capacitance	f = 5 MHz			20	pF
Differential Input Resistance	32R117, f = 5 MHz	2K			Ω
	32R117R, f = 5 MHz	390		810	Ω
Input Bias Current (per side)				45	µA
Common Mode Rejection Ratio	Vcm = VCT + 100 mVpp @ 5 MHz	50			dB

READ CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VDD1, VDD2 or VCC	45			dB
Channel Separation	Unselected Channels: Vin=100 mVpp @ 5 MHz; Selected Channel: Vin = 0 mVpp	45			dB
Output Offset Voltage		-480		+480	mV
Common Mode Output Voltage	Read Mode	5		7	V
	Write/Idle Mode		4.3		V
Single Ended Output Resistance	f = 5 MHz			30	Ω
Leakage Current, RDX, RDY	RDX, RDY = 6V Write/Idle Mode	-100		+100	µA
Output Current	AC Coupled Load, RDX to RDY	2			mA

SWITCHING CHARACTERISTICS (Unless otherwise specified: recommended operating conditions apply, IW = 45 mA, Lh = 10 µH, Rd = 750Ω (32R117) only, f(Data) = 5 MHz)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
R/$\overline{W}$ To Write	Delay to 90% of write current			1.0	µs
R/$\overline{W}$ to Read	Delay to 90% of 100 mV 10 MHz read signal envelope or to 90 % decay of write current			1.0	µs
$\overline{CS}$ to Select	Delay to 90% of write current or to 90% of 100mV 10MHz read signal envelope			1.0	µs
$\overline{CS}$ to Unselect	Delay to 90% decay of write current			1.0	µs

SWITCHING CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
HS0 - HS2 to any head	Delay to 90% of 100 mV 10 MHz read signal envelope			1.0	µs
WUS - Safe to Unsafe - TD1	Iw = 50 mA	1.6		8.0	µs
WUS - Unsafe to Safe - TD2	Iw = 20 mA			1.0	µs
Head Current (Lh = 0 µH, Rh = 0Ω)					
Prop. Delay - TD3	From 50% points			25	ns
Asymmetry	WDI has 50% duty cycle and 1ns rise/fall time			2	ns
Rise/Fall Time	10% - 90% points			20	ns

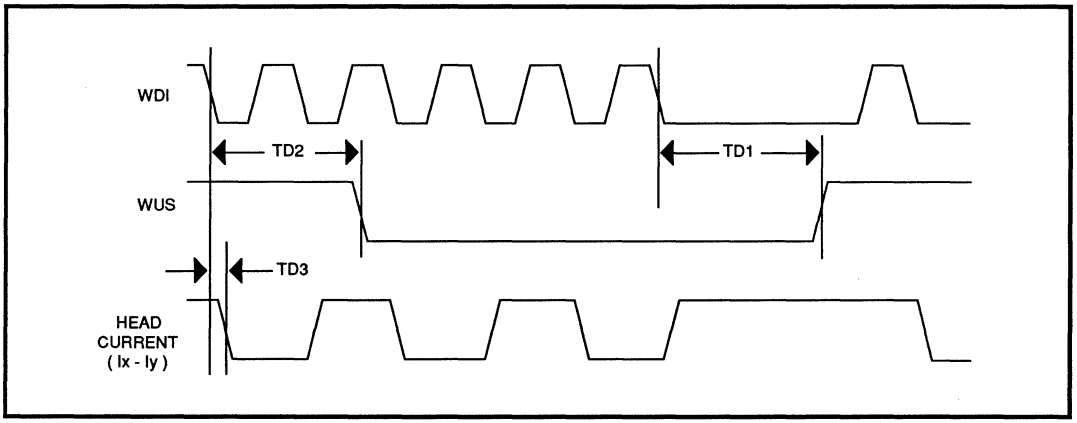
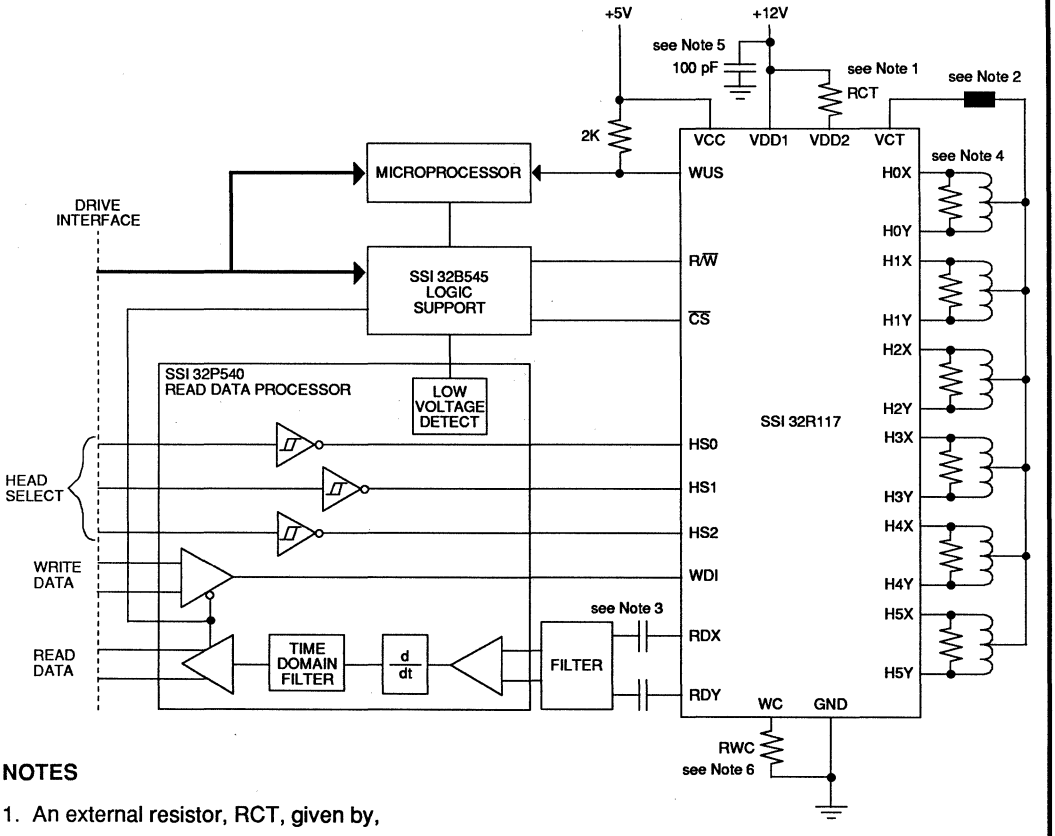


FIGURE 1: Write Mode Timing Diagram



NOTES

1. An external resistor, RCT, given by,

   RCT = 130(55/Iw)Ω, where Iw is in mA,

   can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.

2. A ferrite bead (Ferroxcube 5659065/4A6) can be used to suppress write current overshoot and ringing induced by flex cable parasitics.

3. Limit DC current from RDX and RDY to 100 μA and load capacitance to 20 pF.

4. Damping resistors not required on 32R117R version.

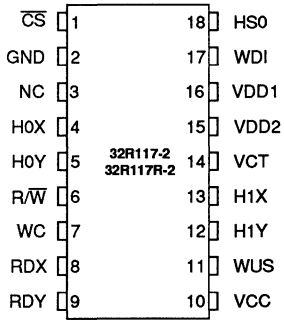
5. The power bypassing capacitor must be located close to the 32R117 with its ground returned directly to device ground with as short a path as possible.

6. To reduce ringing due to stray capacitance this resistor should be located close to the 32R117. Where this is not desirable a series resistor can be used to buffer a long WC line.

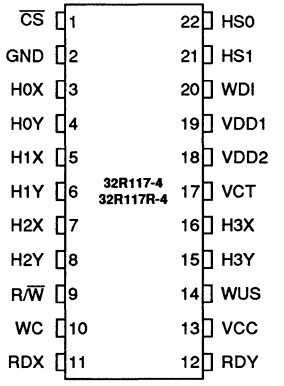
FIGURE 2: Applications Information

PACKAGE PIN DESIGNATIONS

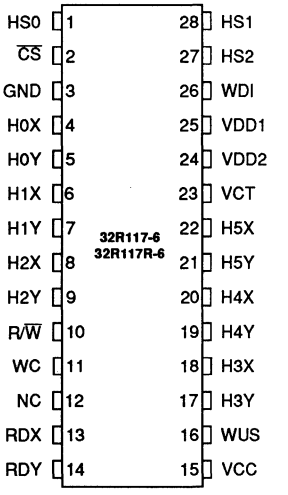
(TOP VIEW)



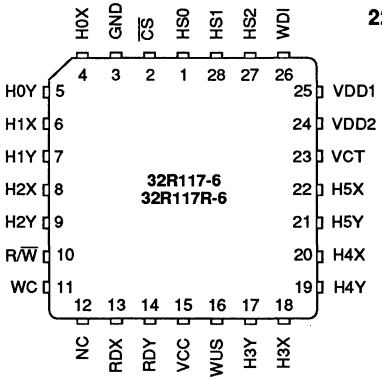
18-lead PDIP



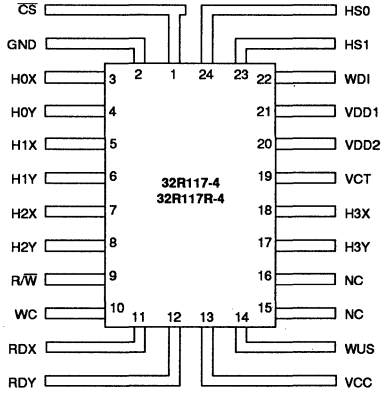
22-lead PDIP



28-lead PDIP,
Flatpack, SOL



28-lead PLCC



24-lead Flatpack, SOL

THERMAL CHARACTERISTICS

PACKAGE	Øja
18-lead PDIP	140°C/W
22-lead PDIP	65°C/W
24-lead Flatpack	110°C/W
SOL	80°C/W
28-lead PDIP	55°C/W
Flatpack	100°c/W
PLCC	65°C/W
SOL	70°C/W

SSI 32R117/117R
2, 4, 6-Channel
Read/Write Circuit

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R117		
2-Channel PDIP	SSI 32R117-2P	32R117-2P
4-Channel PDIP	SSI 32R117-4CP	32R117-4CP
4-Channel SOL	SSI 32R117-4CL	32R117-4CL
4-Channel Flatpack	SSI 32R117-4F	32R117-4F
6-Channel PDIP	SSI 32R117-6CP	32R117-6CP
6-Channel SOL	SSI 32R117-6CL	32R117-6CL
6-Channel Flatpack	SSI 32R117-6F	32R117-6F
6-Channel PLCC	SSI 32R117-6CH	32R117-6CH
SSI 32R117R with Internal Damping Resistor		
2-Channel PDIP	SSI 32R117R-2P	32R117R-2P
4-Channel PDIP	SSI 32R117R-4CP	32R117R-4CP
4-Channel SOL	SSI 32R117R-4CL	32R117R-4CL
4-Channel Flatpack	SSI 32R117R-4F	32R117R-4F
6-Channel PDIP	SSI 32R117R-6CP	32R117R-6CP
6-Channel SOL	SSI 32R117R-6CL	32R117R-6CL
6-Channel Flatpack	SSI 32R117R-6F	32R117R-6F
6-Channel PLCC	SSI 32R117R-6CH	32R117R-6CH

silicon systems™
14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

SSI 32R117A/117AR
2, 4, 6 Channel Read/Write Circuit

August, 1988

DESCRIPTION

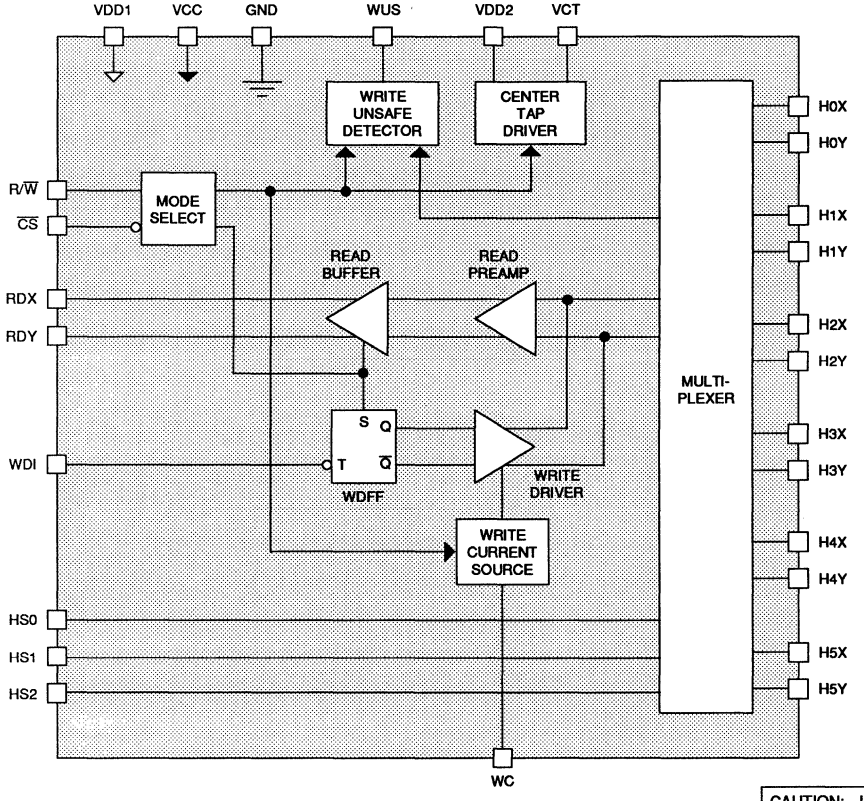
The SSI 32R117A devices are bipolar monolithic integrated circuits designed for use with center-tapped ferrite recording heads. They provide a low noise read path, write current control, and data protection circuitry for as many as six channels. The SSI 32R117A requires +5V and +12V power supplies and is available in 2, 4 or 6 channel versions with a variety of packages.

The SSI 32R117AR differs from the SSI 32R117A by having internal damping resistors.

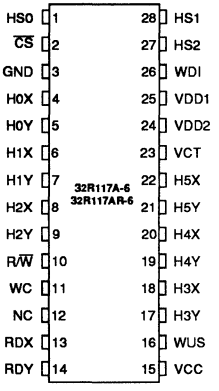
FEATURES

- **+5V, +12V power supplies**
- **Single or multi-platter Winchester drives**
- **Designed for center-tapped ferrite heads**
- **Programmable write current source**
- **Available in 2, 4 or 6 channels**
- **Easily multiplexed for larger systems**
- **Includes write unsafe detection**
- **TTL compatible control signals**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32R117A functions as a write driver or as a read amplifier for the selected head. Head selection and mode control are described in Tables 1 & 2. Both R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition.

WRITE MODE

The Write mode configures the SSI 32R117A as a current switch and activates the Write Unsafe Detector. Head current is toggled between the X- and Y-side of the recording head on the falling edges of WDI, Write Data Input. Note that a preceding read operation initializes the Write Data Flip-Flop, WDFF, to pass current through the X-side of the head. The magnitude of the write current, given by

Iw = K/Rwc, where K = Write Current Constant

is set by the external resistor, Rwc, connected from pin WC to GND.

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output:

- Head open
- Head center tap open
- WDI frequency too low
- Device in Read mode
- Device not selected
- No write current

After the fault condition is removed, two negative transitions on WDI are required to clear WUS.

Power dissipation in write mode may be reduced by placing a resistor (RCT) between VDD1 & VDD2. The optimum resistor value is 130Ω x 50/Iw (Iw in mA). At low write currents (<15 mA) read mode dissipation is higher than write mode and RCT, though recommended, may not be considered necessary. In this case VDD2 is connected directly to VDD1.

READ MODE

In the Read mode the SSI 32R117A is configured as a low noise differential amplifier, the write current source and the write unsafe detector are deactivated, and the write data flip-flop is set. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports. They should be AC coupled to the load.

Note that the internal write current source is deactivated for both the Read and the Chip Deselect mode. This eliminates the need for external gating of the write current source.

IDLE MODE

Taking CS high selects the idle mode which switches the RDX, RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wire OR'ed.

TABLE 1: MODE SELECT

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	x	Idle

TABLE 2: HEAD SELECT

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	x	None

0 = Low level 1 = High level x = Don't care

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0-HS2	I	Head Select: selects up to six heads
$\overline{CS}$	I	Chip Select: a low level enables device
R/$\overline{W}$	I	Read/Write: a high level selects read mode
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition (open collector)
WDI	I	Write Data In: negative transition toggles the direction of the head current
H0X-H5X H0Y-H5Y	I/O	X,Y head connections
RDX, RDY	O*	X, Y Read Data: differential read signal out
WC	-	Write Current: used to set the magnitude of the write current
VCT	-	Voltage Center Tap: voltage source for head center tap
VCC	-	+5V
VDD1	-	+12V
VDD2	-	Positive power supply for the center tap voltage source
GND	-	Ground

*When more than one R/W device is used, these signals can be wire OR'ed.

ABSOLUTE MAXIMUM RATINGS (Operation above absolute maximum ratings may permanently damage the device. All voltages referenced to GND.)

PARAMETER		VALUE	UNITS
VDD1	DC Supply Voltage	-0.3 to +14	VDC
VDD2	DC Supply Voltage	-0.3 to +14	VDC
VCC	DC Supply Voltage	-0.3 to +6	VDC
VIN	Digital Input Voltage Range	-0.3 to VCC + 0.3	VDC
VH	Head Port Voltage Range	-0.3 to VDD + 0.3	VDC
Vwus	WUS Port Voltage Range	-0.3 to +14	VDC
Iw	Write Current	60	mA
Io	RDX, RDY Output Current	-10	mA
Ivct	VCT Output Current	-60	mA
Iwus	WUS Output Current	+12	mA
Tstg	Storage Temperature Range	-65 to +150	°C
Lead Temperature PDIP, Flatpack (10 sec soldering)		260	°C
Package Temperature PLCC, SOL (20 sec reflow)		215	°C

RECOMMENDED OPERATION CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DC Supply Voltage	VDD1		10.8	12.0	13.2	VDC
DC Supply Voltage	VCC		4.5	5.0	5.5	VDC
Head Inductance	Lh		5		15	µH
Damping Resistor	RD	32R117A only	500		2000	Ω
RCT Resistor	RCT		125.0	130	135.0	Ω
Write Current	Iw		25		50	mA
Junction Temperature Range	Tj		25		125	°C

DC CHARACTERISTICS

(Unless otherwise specified, recommended operating conditions apply.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VCC Supply Current		Read/Idle Mode			25	mA
		Write Mode			30	mA
VDD Supply Current		Idle Mode			25	mA
		Read Mode			50	mA
		Write Mode			30+Iw	mA
Power Dissipation (Tj = +125°C)		Idle Mode			400	mW
		Read Mode			600	mW
		Write Mode, Iw = 50 mA, RCT = 130Ω			700	mW
		Write Mode, Iw = 50 mA, RCT = 0Ω			1050	mW
Digital Inputs						
Input Low Voltage	VIL		-0.3		0.8	VDC
Input High Voltage	VIH		2.0		VCC+0.3	VDC
Input Low Current	IIL	VIL = 0.8V	-0.4			mA
Input High Current	IIH	VIH = 2.0V			100	µA
WUS Output	VOL	IOL = 8 mA			0.5	VDC
WUS Output	IOH	VOH = 5.0V			100	µA
Center Tap Voltage	VCT	Write Mode		6.0		VDC
		Read Mode		4.0		VDC

WRITE CHARACTERISTICS (Unless otherwise specified: recommended operating conditions apply, IW = 45 mA, Lh = 10 µH, Rd = 750Ω (32R117A only), f(Data) = 5 MHz, CL(RDX, RDY) ≤ 20 pF)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Write Current Range		10		50	mA
Write Current Constant "K"		133		147	V
Differential Head Voltage Swing		8.0			V(pk)
Unselected Head Transient Current				2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	32R117A	10K			Ω
	32R117AR	638		863	Ω
WDI Transition Frequency	WUS = low	250			kHz
Iwc to Head Current Gain	Iw/Iwc		20		mA/mA
Unselected Head Leakage Current	Sum of X & Y side leakage current			85	µA

READ CHARACTERISTICS
(Unless otherwise specified: recommended operating conditions apply, IW = 45 mA, Lh = 10 µH, Rd = 750Ω (32R117A only), f(Data) = 5 MHz, CL(RDX, RDY) ≤ 20 pF, Vin is referenced to VCT)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain	Vin = 1 mVpp @ 300 KHz RL(RDX), RL(RDY) = 1 KΩ	90		110	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10%, Vin = Vi + 0.5 mVpp @ 300 KHz	-3		+3	mV
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	30			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			1.7	nV/√Hz
Differential Input Capacitance	f = 5 MHz			20	pF
Differential Input Resistance	32R117A, f = 5 MHz	2K			Ω
	32R117AR, f = 5 MHz	450		750	Ω
Input Bias Current (per side)				45	µA
Common Mode Rejection Ratio	Vcm = VCT + 100 mVpp @ 5 MHz	50			db

READ CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VDD1, VDD2 or VCC	45			dB
Channel Separation	Unselected Channels: Vin=100 mVpp @ 5 MHz; Selected Channel: Vin = 0 mVpp	45			dB
Output Offset Voltage		-440		+440	mV
Common Mode Output Voltage	Read Mode	5		7	V
	Write/Idle Mode		4.3		V
Single Ended Output Resistance	f = 5 MHz			30	Ω
Leakage Current, RDX, RDY	RDX, RDY = 6V Write/Idle Mode	-100		+100	µA
Output Current	AC Coupled Load, RDX to RDY	2			mA

SWITCHING CHARACTERISTICS (Unless otherwise specified: recommended operating conditions apply, IW = 45 mA, Lh = 10 µH, Rd = 750Ω (32R117A only), f(Data) = 5 MHz)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
R/$\overline{W}$ To Write	Delay to 90% of write current			1.0	µs
R/$\overline{W}$ to Read	Delay to 90% of 100 mV 10 MHz read signal envelope or to 90 % decay of write current			1.0	µs
$\overline{CS}$ to Select	Delay to 90% of write current or to 90% of 100mV 10MHz read signal envelope			1.0	µs
$\overline{CS}$ to Unselect	Delay to 90% decay of write current			1.0	µs

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
HS0 - HS2 to any head	Delay to 90% of 100 mV 10 MHz read signal envelope			1.0	µs
WUS - Safe to Unsafe - TD1	Iw = 50 mA	1.6		8.0	µs
WUS - Unsafe to Safe - TD2	Iw = 20 mA			1.0	µs
Head Current (Lh = 0 µH, Rh = 0Ω)					
Prop. Delay - TD3	From 50% points			25	ns
Asymmetry	WDI has 50% duty cycle and 1ns rise/fall time			2	ns
Rise/Fall Time	10% - 90% points			20	ns

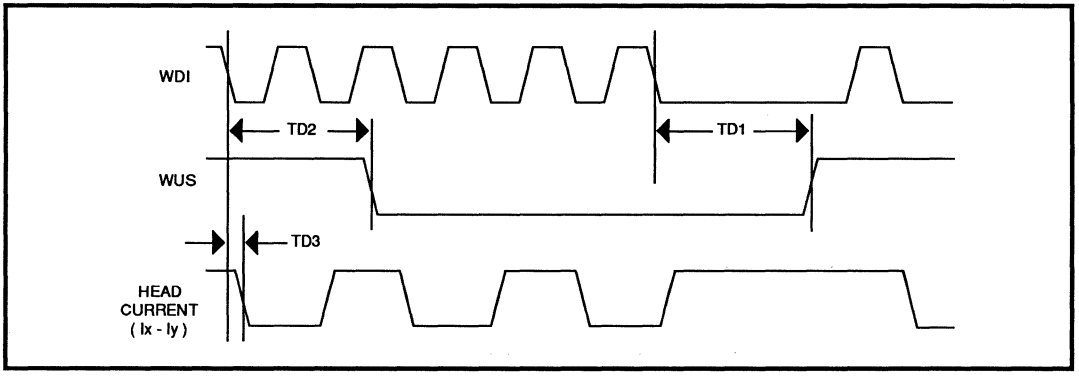
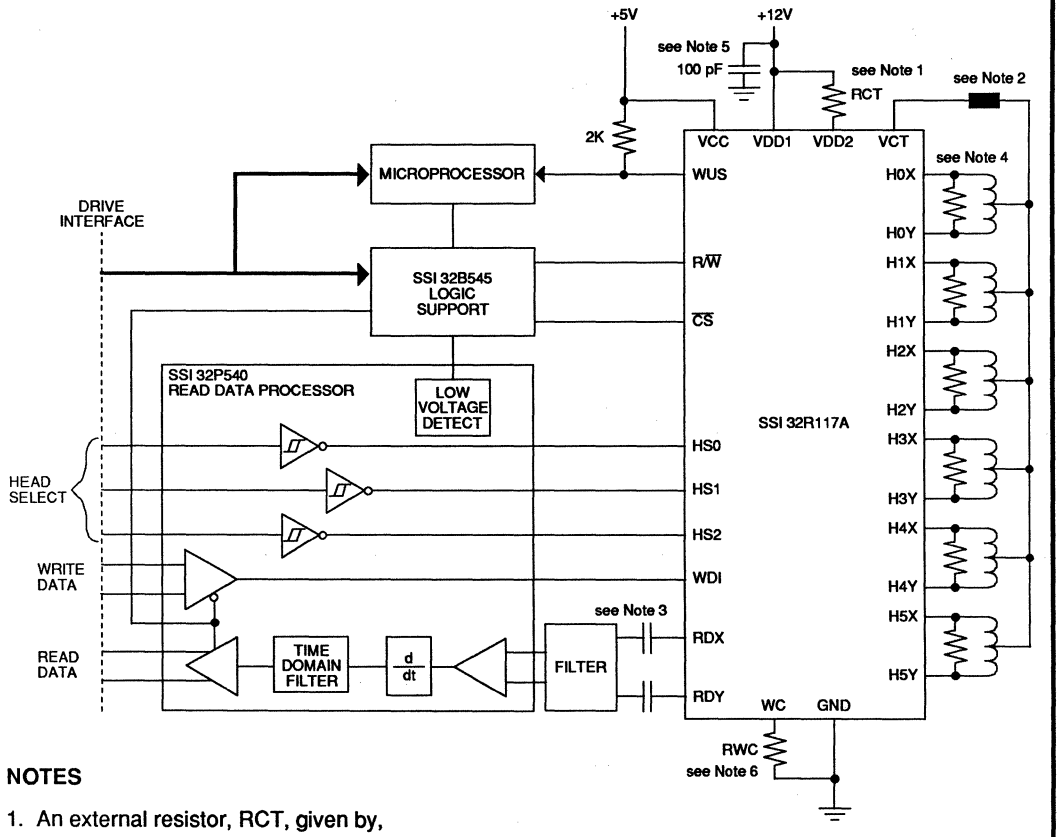


FIGURE 1: Write Mode Timing Diagram



NOTES

1. An external resistor, RCT, given by,

   RCT = 130(50/Iw)Ω, where Iw is in mA,

   can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.

2. A ferrite bead (Ferroxcube 5659065/4A6) can be used to suppress write current overshoot and ringing induced by flex cable parasitics.

3. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF.

4. Damping resistors not required on 32R117AR version.

5. The power bypassing capacitor must be located close to the 32R117A with its ground returned directly to device ground with as short a path as possible.

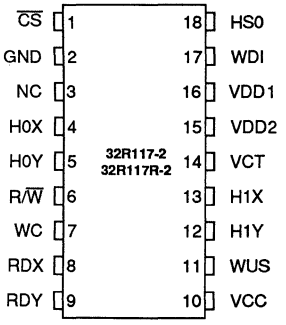
6. To reduce ringing due to stray capacitance this resistor should be located close to the 32R117A. Where this is not desirable a series resistor can be used to buffer a long WC line.

FIGURE 2: Applications Information

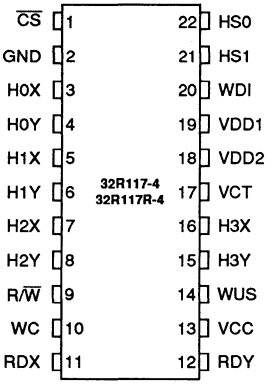
1

PACKAGE PIN DESIGNATIONS

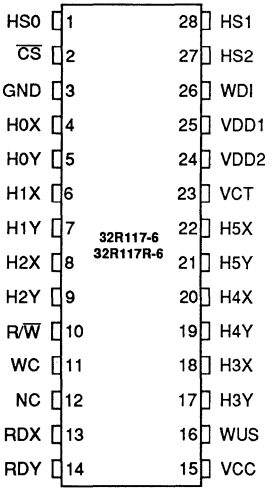
(TOP VIEW)



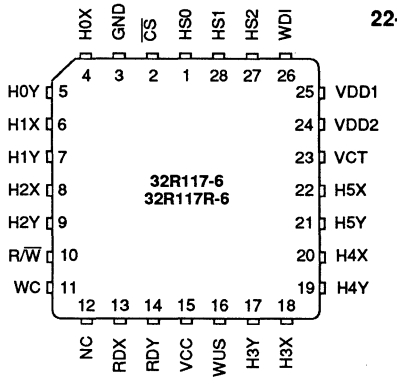
18-lead PDIP



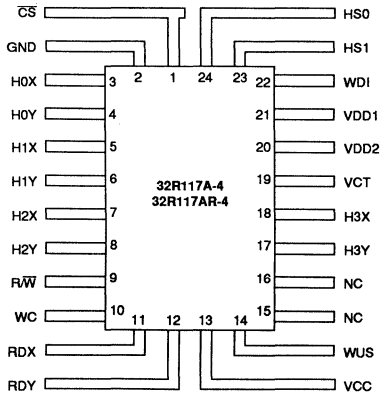
22-lead PDIP



28-lead PDIP,
Flatpack, SOL



28-lead PLCC



24-lead Flatpack, SOL

THERMAL CHARACTERISTICS

PACKAGE		Øja
18-lead PDIP		140°C/W
22-lead PDIP		65°C/W
24-lead Flatpack		110°C/W
	SQL	80°C/W
28-lead PDIP		55°C/W
	Flatpack	100°c/W
	PLCC	65°C/W
	SOL	70°C/W

SSI 32R117A/117AR
2, 4, 6-Channel
Read/Write Circuit

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R117A		
2-Channel PDIP	SSI 32R117A-2P	32R117A-2P
4-Channel PDIP	SSI 32R117A-4CP	32R117A-4CP
4-Channel SOL	SSI 32R117A-4CL	32R117A-4CL
4-Channel Flatpack	SSI 32R117A-4F	32R117A-4F
6-Channel PDIP	SSI 32R117A-6CP	32R117A-6CP
6-Channel SOL	SSI 32R117A-6CL	32R117A-6CL
6-Channel Flatpack	SSI 32R117A-6F	32R117A-6F
6-Channel PLCC	SSI 32R117A-6CH	32R117A-6CH
SSI 32R117AR with Internal Damping Resistor		
2-Channel PDIP	SSI 32R117AR-2P	32R117AR-2P
4-Channel PDIP	SSI 32R117AR-4CP	32R117AR-4CP
4-Channel SOL	SSI 32R117AR-4CL	32R117AR-4CL
4-Channel Flatpack	SSI 32R117AR-4F	32R117AR-4F
6-Channel PDIP	SSI 32R117AR-6CP	32R117AR-6CP
6-Channel SOL	SSI 32R117AR-6CL	32R117AR-6CL
6-Channel Flatpack	SSI 32R117AR-6F	32R117AR-6F
6-Channel PLCC	SSI 32R117AR-6CH	32R117AR-6CH

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INNOVATORS IN INTEGRATION

SSI 32R188
4-Channel Read/Write Circuit

July, 1988

1

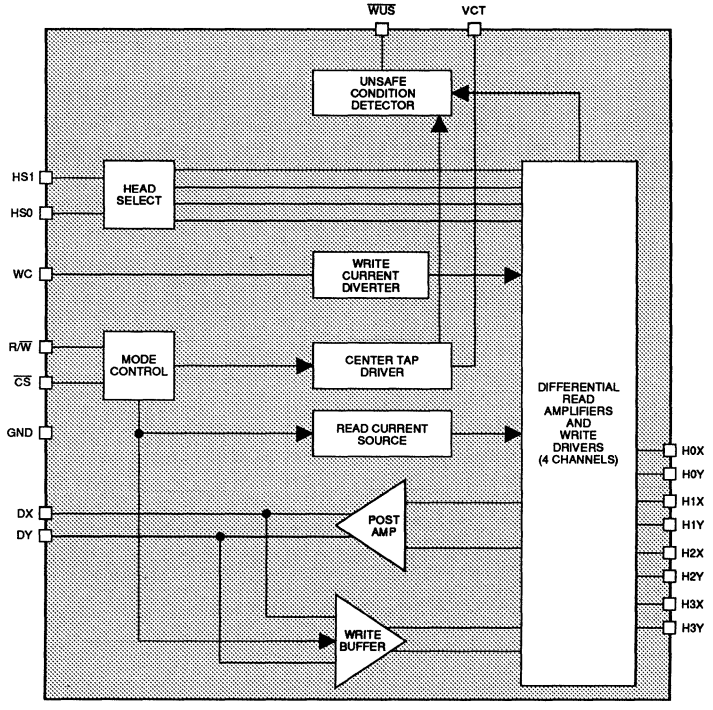
DESCRIPTION

The SSI 32R188 is a high-performance, bipolar integrated read/write circuit for use with center tapped, ferrite heads. It provides a low noise read path, write control circuitry and data protection circuitry for 4-channels. The SSI 32R188 requires +6.5V and -5.2V power supplies. It is available in a 24-pin flat pack.

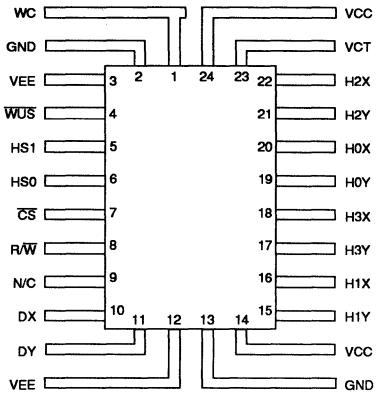
FEATURES

- **Fast switching characteristics**
- **TTL compatible control signals**
- **Four head capacity**
- **Designed for center-tapped ferrite heads**
- **Includes write unsafe detection**
- **Easily multiplexed**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32R188
4-Channel
Read/Write Circuit

FUNCTIONAL DESCRIPTION

The SSI 32R188 has three selectable modes of operation as illustrated in Table 1. The R/$\overline{W}$ and $\overline{CS}$ inputs which determine these modes have internal resistor pullups to prevent an accidental write condition. Depending on the mode selected, the chip performs as a write gate or read amplifier for the selected head. Table 2 shows proper head addressing. In the Idle mode all inputs and outputs are in a high-impedance state, except the WC pin which is diverted to GND.

WRITE MODE

In this mode, externally supplied write current is gated to the "X" side of the chosen head when the DX input is low and to the "Y" side when DY is low. The write unsafe detector is activated when the SSI 32R188 is in the write mode. A low on the $\overline{WUS}$ pin indicates one of the following unsafe conditions:

- Head open or shorted
- No write current
- No write data transitions

During a normal write cycle the pin is initially low and then goes high after the differential input makes two transitions. Two transitions are also needed to clear WUS after a fault condition.

READ MODE

The SSI 32R188 amplifies the differential signal on the addressed head when in the read mode. The amplified signal is output on the open-collector DX and DY pins, with a gain dependent on external resistors tied from each pin to ground. The nominal values listed in this data sheet were obtained with 50Ω resistors and can be doubled by using100Ω resistors. Polarity is such that the DX output is more positive when the "X" side of the head is more positive. External gating of the write current source is not necessary because an on-chip diverter circuit prevents the write current from flowing in the head circuits during the read and idle modes.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TABLE 2: Head Select

HS1	HS0	HEAD
0	0	0
0	1	1
1	0	2
1	1	3

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HS0 - HS1	I	Head Select: selects up to four heads
$\overline{CS}$	I	Chip Select: a low level enables device
R/$\overline{W}$	I	Read/Write: a high level selects Read mode
$\overline{WUS}$	O	Write Unsafe: open collector output, low indicates unsafe condition
H0X-H3X H0Y-H3Y	I/O	X, Y head connections
DX, DY	I/O	X, Y Read/Write Data: differential read data in/write data out signal
WC	-	Write Current: external write current generator connected to this pin
VCT	-	Voltage Center Tap: voltage source for head center tap
VCC	-	+6.5V
VEE	-	-5.2V
GND	-	Ground

ABSOLUTE MAXIMUM RATINGS (Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER		RATING	UNIT
DC Supply Voltages	VCC	7.5	VDC
	VEE	-6.0	VDC
Digital Input Voltage Range		-0.3 to VCC + 0.3	VDC
Head Input (Read Mode)		-0.6 to 0.4	VDC
Head Select (HS0, HS1)		-0.4 (or -2 mA) to VCC + 0.3	VDC
$\overline{WUS}$ Port Voltage Range		-0.4 to VCC + 0.3	VDC
Write Current (Iw)		-80	mA
Output Current	VCT	-80	mA
	$\overline{WUS}$	10	mA
DX, DY Voltage		-0.1 to + 0.3	VDC
Differential Voltage, $\lvert V_{R/\overline{W}} - V_{\overline{CS}} \rvert$		6.5	VDC
Storage Temperature Range (Tstg)		-65 to + 150	°C
Lead Temperature (10 sec soldering)		260	°C

RECOMMENDED OPERATION CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DC Supply Voltage	VCC		6.2	6.5	6.8	VDC
DC Supply Voltage	VEE		-5.5	-5.2	-4.9	VDC
Head Inductance	Lh		1.5		15	µH
Write Current	Iw		35		70	mA
Junction Temperature Range	Tj		25		125	°C

DC CHARACTERISTICS
(Unless otherwise specified, VCC = 6.5 ± 5%, VEE = -5.2 ± 5%, +25°C < Tj < +125°C.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VCC Supply Current		Idle Mode			35	mA
		Read Mode			80	mA
		Write Mode			40+Iw	mA
VEE Supply Current		Idle Mode	-20			mA
		Read Mode	-75			mA
		Write Mode	-30			mA
Digital Inputs		HS0, HS1, R/$\overline{W}$, $\overline{CS}$				
Input Low Voltage	VIL				0.8	VDC
Input High Voltage	VIH		2.0			VDC
Head Select						
Input Low Current	IIL	VIL = 0.8V	-0.1		0.2	mA
Input High Current	IIH	VIH = 2.0V	-0.1		0.2	mA
Chip Select & Read/Write						
Input Low Current	IIL	VIL = 0.8V	-1.6		-0.1	mA
Input High Current	IIH	VIH = 2.0V	-1.4		-0.1	mA
$\overline{WUS}$ Output	VOL	IOL = 8 mA			0.5	VDC
$\overline{WUS}$ Output	IOH	VOH = 5.0V	-100		100	µA
Center Tap Voltage	VCT	Read Mode		0.0		VDC
		Write Mode		4.2		VDC

WRITE CHARACTERISTICS (Unless otherwise specified: VCC = 6.5 ± 5%, VEE = -5.2 ± 5%, Iw = 70 mA, Lh = 1.8 µH, Rd = 230Ω)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Write Current Range		35		70	mA
Current Gain	Head Current/Iwc	0.95		1.01	-
Differential Head Voltage Swing		10.5			V(pk)
Unselected Diff. Head Current				3	mA(pk)
Data Input Capacitance	Per side to GND			10	pF
Data Input Resistance		5			KΩ
WC Voltage		-4.5		-0.5	V
Differential Data Input Voltage		300			mV
Data Input Voltage Range		-0.8		+0.1	V
Data Input Current	Per side			100	µA

READ CHARACTERISTICS
(Unless otherwise specified: VCC = 6.5 ± 5%, VEE = -5.2 ± 5%, Lh = 1.8 µH, Rd = 230Ω, f(Data) = 5 MHz, RL(DX, DY) = 50Ω to GND, Vin is referenced to VCT)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain	Vin = 1 mVpp @ 300 KHz	25		60	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10%, Vin = Vi + 0.5 mVpp @ 300 KHz	-2		+2	mV
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	48			MHz
Input Noise Voltage	BW = 15 MHz, Vin = 0.0 VDC Lh = 0, Rh = 0			2.4	nV/√Hz
	Lh = 0, Rh = 115Ω per side			3.3	nV/√Hz
Differential Input Capacitance	Vin = 0.0 VDC			18	pF
Differential Input Resistance	V = 0.0 VDC	1.5			KΩ
Input Bias Current (per side)	Vin = 0.0 VDC			100	µA
Common Mode Rejection Ratio	Vcm = 100 mVpp @ 12 MHz	45			dB
Power Supply Rejection Ratio	100 mVpp on VCC or VEE	45			dB

READ CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Channel Separation	Unselected Channels: Vin=100 mVpp @ 12 MHz; Selected Channel: Vin = 0 mVpp	34			dB
Input Offset Voltage		-10		+10	mV
Common Mode Output Voltage		-1.3		-0.2	V
Single Ended Output Resistance		5			KΩ
Single Ended Output Capacitance				10	pF
WC Voltage	IWC = 70 mA	-3.2		-0.4	VDC
Total Head Input Current IVCT	IWC = 0	-500		+500	µA

SWITCHING CHARACTERISTICS (Unless otherwise specified: VCC = 6.5 ± 5%, VEE = -5.2V ± 5%, Tj = 25°C, Iw = 70 mA, Lh = 1.8 µH, Rd = 230Ω, f(Data) = 5 MHz)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
R/$\overline{W}$ To Write	Delay to 90% of write current			0.6	µs
R/$\overline{W}$ to Read	Delay to 90% of 100 mV 10 MHz read signal envelope or to 90 % decay of write current			0.6	µs
$\overline{CS}$ to Select	Delay to 90% of write current or to 90% of 100mV 10MHz read signal envelope			0.6	µs
$\overline{CS}$ to Unselect	Delay to 90% decay of write current			0.6	µs
HS0 - HS2 to any head	Delay to 90% of 100 mV 10 MHz read signal envelope			0.25	µs
$\overline{WUS}$ - Safe to Unsafe	TD1, Iw = 70 mA	0.4		4.0	µs
$\overline{WUS}$ - Unsafe to Safe	TD2, Iw = 35 mA			1.0	µs
Head Current	Lh = 0 µH, Rh = 25Ω per side				
Prop. Delay	TD3, From 50% points			19	ns
Asymmetry	2 ns max input switching			2	ns
Rise/Fall Time	10% - 90% points			15	ns

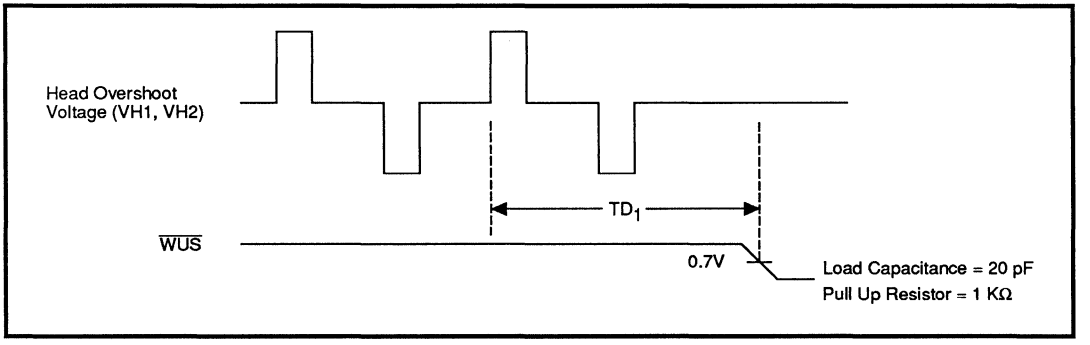


FIGURE 1: Safe to Unsafe Timing

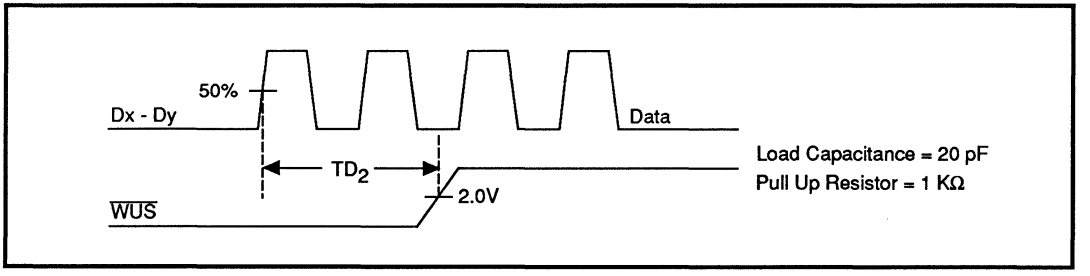


FIGURE 2: Unsafe to Safe Timing

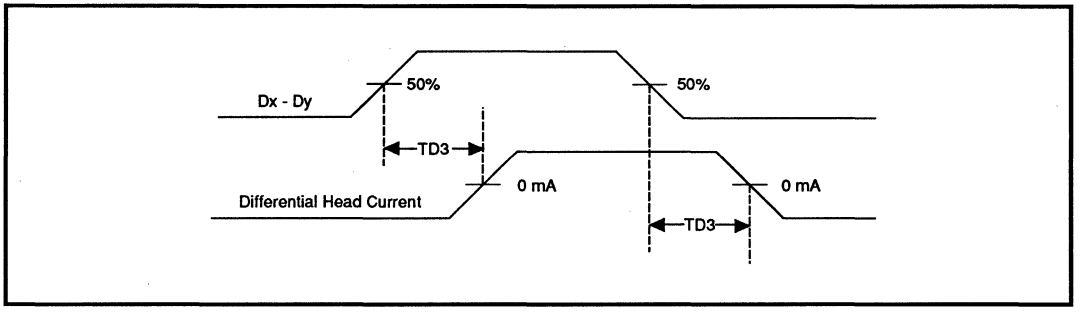


FIGURE 3: Head Current Timing

TEMPERATURE MONITORING

Two sets of series diodes are included on the chip for junction temperature monitoring. Between both the HS0 and HS1 pads to GND, two diodes are connected in series as shown in Figure 4.

To calibrate the diodes remove power from the SSI 32R188, pull down on the HS0 or HS1 pin with a constant current and measure the diode forward bias voltage as the temperature is varied. To monitor temperature measure the diode forward bias voltage in either read or write mode and compare to the previously determined calibration curve.

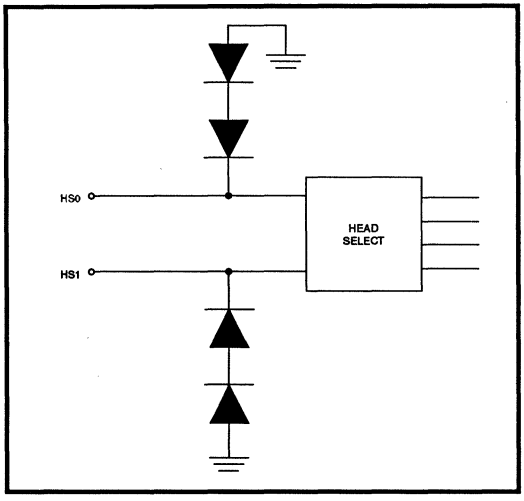


FIGURE 4

APPLICATIONS

The circuits shown in Figures 5, 6, and 7 are suggested for interfacing the differential DX and DY lines and either ECL or TTL data.

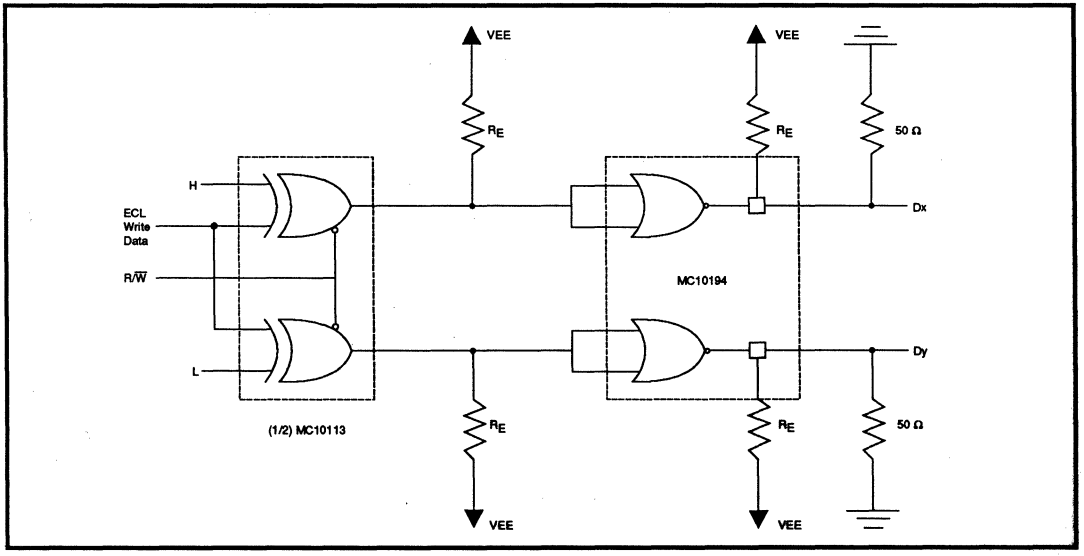


FIGURE 5

APPLICATIONS (Continued)

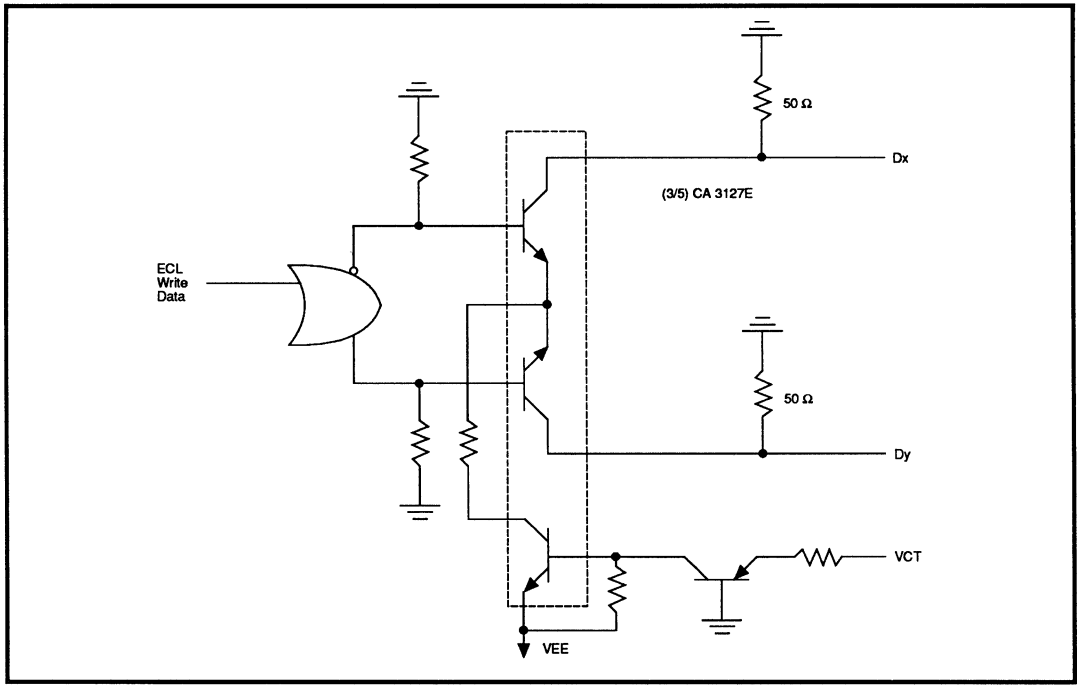


FIGURE 6

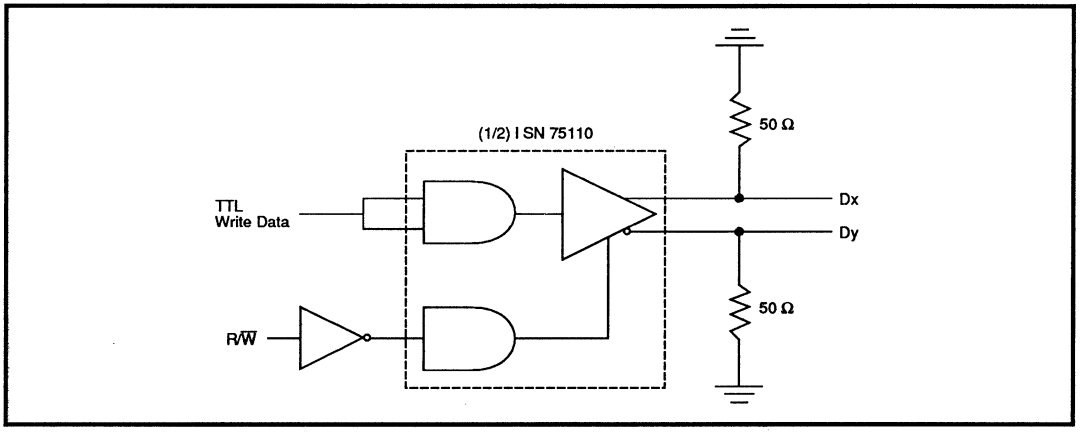
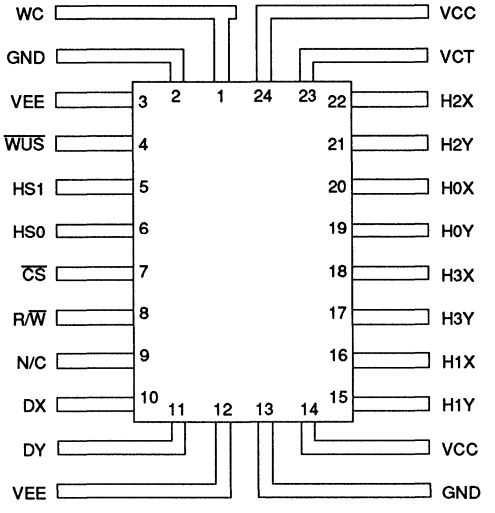


FIGURE 7

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



Øja = 105°C/W

24-Pin Flatpack

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R188 24-Pin Flatpack	SSI 32R188-4F	32R188-4F

Silicon Systems™

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, TWX 910-595-2809

SSI 32R501/501R
4, 6, 8-Channel Ferrite Read/Write Circuit

August, 1988

1

DESCRIPTION

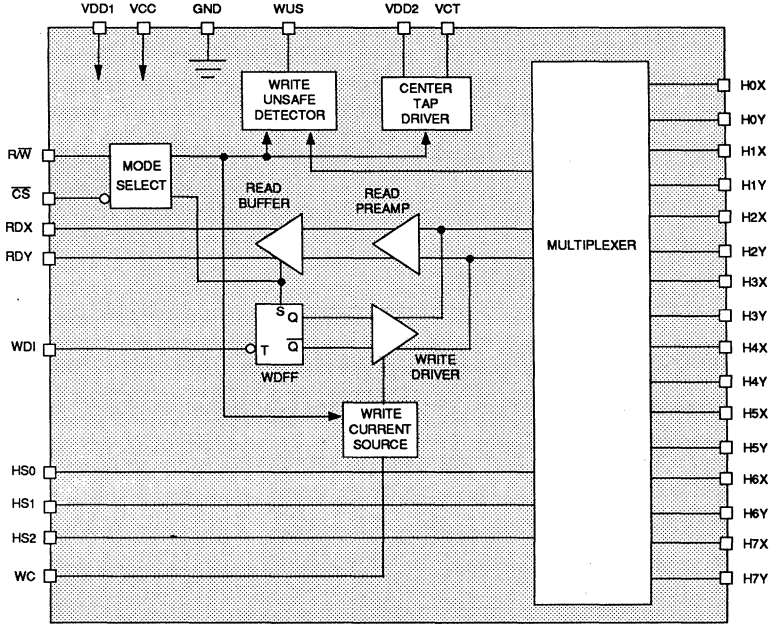
The SSI 32R501 is a bipolar monolithic integrated circuit designed for use with a center-tapped ferrite recording head. It provides a low noise read path, write current control, and data protection ciruitry for as many as 8 channels. The SSI 32R501 requires +5V and +12V power supplies and is available in a variety of packages.

The SSI 32R501R performs the same function as the SSI 32R501 with the addition of internal damping resistors.

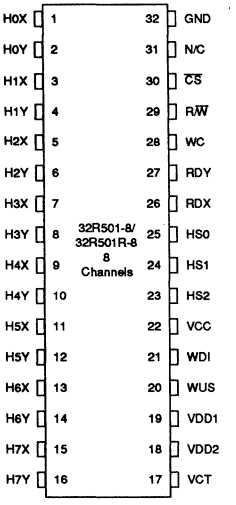
FEATURES

- **Single or multi-platter Winchester drives**
- **Designed for center-tapped ferrite heads**
- **Programmable write current source**
- **Easily multiplexed for larger systems**
- **Includes write unsafe detection**
- **TTL compatible control signals**
- **1.5 nV/√Hz maximum input noise voltage**
- **+5V, +12V power supplies**

BLOCK DIAGRAM



PIN DIAGRAM



32-LEAD SOW

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32R501 gives the user the ability to address up to eight center-tapped ferrite heads and provide write drive or read amplification. Head selection and mode control is accomplished using the HSn, $\overline{CS}$ and R/$\overline{W}$ inputs as shown in Tables 1 & 2. Internal pullups are provided for the $\overline{CS}$ & R/$\overline{W}$ inputs to force the device into a non-writing condition if either control line is opened accidentally.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TABLE 2: Head Select

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

0 = Low level 1 = High level

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SSI 32R501 as a current switch and activates the Write Unsafe (WUS) detector circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding read mode selection initializes the Write Data Flip-Flop, WDFF, to pass write current through the "X" side of the head. The zero-peak write current magnitude is programmed by an external resistor Rwc from pin WC to GND and is given by:

Iw = K/Rwc, where K = Write Current Constant

The Write Unsafe detection circuitry monitors voltage transitions at the selected head connections and flags any of the following conditions as a high level on the Write Unsafe open collector output:

- Head open
- WDI frequency too low
- Device not selected
- Head center tap open
- Device in read mode
- No write current

Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

Power dissipation in write mode may be reduced by placing a resistor (RCT) between VDD1 & VDD2. The optimum resistor value is 120Ω x 50/Iw (Iw in mA). At low write currents (<15 mA) read mode dissipation is higher than write mode and RCT, though recommended, may not be considered necessary. In this case VDD2 is connected directly to VDD1.

READ MODE

Taking $\overline{CS}$ low and R/$\overline{W}$ high selects read mode which configures the SSI 32R501 as a low noise differential amplifier for the selected head. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The internal write current source is gated off in read mode eliminating the need for any external gating.

Read mode selection also initializes the Write Data Flip-Flop (WDFF) to pass write current through the "X" side of the head at a subsequent write mode selection.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX, RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wire OR'ed.

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0-HS2	I	Head Select
$\overline{CS}$	I	Chip Select: a low level enables device
R/$\overline{W}$	I	Read/Write: a high level selects read mode
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition
WDI	I	Write Data In: negative transition toggles direction of head current
H0X-H7X H0Y-H7Y	I/O	X,Y head connections
RDX, RDY	O*	X, Y Read Data: differential read signal out
WC		Write Current: used to set the magnitude of the write current
VCT		Voltage Center Tap: voltage source for head center tap
VCC		+5V
VDD1		+12V
VDD2		Positive power supply for the center tap voltage source
GND		Ground
* When more than one R/$\overline{W}$ device is used these signals can be wire OR'ed.		

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (All voltages referenced to GND. Currents into device are positive.)

PARAMETER		VALUE	UNITS
DC Supply Voltage	VDD1	-0.3 to +14	VDC
DC Supply Voltage	VDD2	-0.3 to +14	VDC
DC Supply Voltage	VCC	-0.3 to +6	VDC
Digital Input Voltage Range	VIN	-0.3 to VCC + 0.3	VDC
Head Port Voltage Range	VH	-0.3 to VDD1 + 0.3	VDC
WUS Pin Voltage Range	Vwus	-0.3 to +14	VDC
Write Current Zero Peak	Iw	60	mA
Output Current	RDX, RDY Io	-10	mA
Output Current	Ivct	-60	mA
Output Current	Iwus	+12	mA
Storage Temperature Range	Tstg	-65 to 150	°C
Lead Temp. PDIP, Flatpack (10 sec Soldering)		260	°C
Package Temperature PLCC, SO (20 sec Reflow)		215	°C

RECOMMENDED OPERATION CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DC Supply Voltage	VDD1		10.8	12.0	13.2	VDC
DC Supply Voltage	VCC		4.5	5.0	5.5	VDC
Head Inductance	Lh		5		15	µH
Damping Resistor	RD	32R501 only	500		2000	Ω
RCT Resistor	RCT*	Iw = 50 mA	114	120	126	Ω
Write Current	Iw		22		50	mA
Junction Temperature Range	Tj		+25		+135	°C
*For Iw = 50 mA. At other Iw levels refer to Applications Information that follows this specification.						

DC CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Supply Current	Read/Idle Mode			25	mA
	Write Mode			30	mA
VDD Supply Current	Idle Mode			25	mA
(sum of VDD1 and VDD2)	Read Mode			50	mA
	Write Mode			30 + Iw	mA
Power Dissipation (Tj = +135°C)	Idle Mode			400	mW
	Read Mode			600	mW
	Write Mode, Iw = 50 mA, RCT = 0Ω			1050	mW
	Write Mode, Iw = 50 mA RCT = 120Ω			750	mW

DC CHARACTERISTICS (Continued)

DIGITAL I/O

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VIL	Input Low Voltage		-0.3		0.8	VDC
VIH	Input High Voltage		2.0		VCC + 0.3	VDC
IIL	Input Low Current	VIL = 0.8V	-0.4			mA
IIH	Input High Current	VIH = 2.0V			85	µA
VOL	WUS Output Low Voltage	IOL = 8 mA			0.5	VDC
IOH	WUS Output High Current	VOH = 5.0V			100	µA

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Center Tap Voltage VCT	Write Mode		6.0		VDC
Write Current Range		10		50	mA
Write Current Constant "K"		129		151	
Iwc to Head Current Gain			20		mA/mA
Unselected Head Leakage Current				85	µA
RDX, RDY Common Mode Output Voltage	Write/Idle Mode		4.3		VDC
RDX, RDY Leakage	RD 3.0 < RDX, RDY < 8.0V Write/Idle Mode	-50		+50	µA

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Center Tap Voltage	Read Mode		4.0		VDC
Input Bias Current (differential)				100	µA
Output Offset Voltage	Read Mode	-480		+480	mV
Common Mode Output Voltage	Read Mode	5		7	VDC

DYNAMIC CHARACTERISTICS AND TIMING

Unless otherwise specified, recommended operating conditions apply and Iw = 45 mA, Lh = 10 µH, Rd = 750Ω 32R501 only, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 20 pF.)

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Head Voltage Swing		7.5			V(pk)
Unselected Head Transient Current	5 µH ≤ Lh ≤ 9.5 µH			2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	32R501	10K			Ω
	32R501R	600		960	Ω
WDI Transition Frequency	WUS = low	250			KHz

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain	Vin = 1 mVpp @ 300 kHz, RL(RDX), RL(RDY) = 1 KΩ	80		120	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10%. Vin = Vi + 0.5 mVpp @ 300 kHz	-3		+3	mV
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	30			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			1.5	nV/√Hz
Differential Input Capacitance	f = 5 MHz			23	pF
Differential Input Resistance	32R501, f = 5 MHz	2K			Ω
Differential Input Resistance	32R501R, f = 5 MHz	460		860	Ω
Common Mode Rejection Ratio	Vcm = VCT + 100 mVpp @ 5 MHz	50			dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VDD1, VDD2 or VCC	45			dB
Channel Separation	Unselected Channels: Vin=100 mVpp @ 5 MHz; Selected Channel: Vin = 0 mVpp	45			dB
Single Ended Output Resistance	f = 5 MHz			30	Ω

READ MODE (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Output Current	AC Coupled Load, RDX to RDY	2.0			mA
External Resistance Load	AC coupled to output per side to GND	100			Ω
Center tap output impedance	$0 \le f \le 5$ MHz			150	Ω

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
R/$\overline{W}$ To Write	Delay to 90% of Write Current			600	ns
R/$\overline{W}$ to Read	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope or to 90% decay of Write Current			600	ns
$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100 mV, 10 MHz Read Signal Envelope			600	ns
$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current			600	ns
HS0 - HS2 to any head	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope			600	ns
WUS-Safe to Unsafe - TD1	Iw = 50 mA	1.6		8.0	µs
WUS-Unsafe to Safe - TD2	Iw = 20 mA			1.0	µs
Head Current (Lh = 0 µH, Rh = 0Ω)					
Prop. Delay - TD3	From 50% Points			30	ns
Asymmetry	WDI has 50% Duty Cycle and 1ns Rise/Fall Time			2	ns
Rise/Fall Time	10% - 90% Points			20	ns

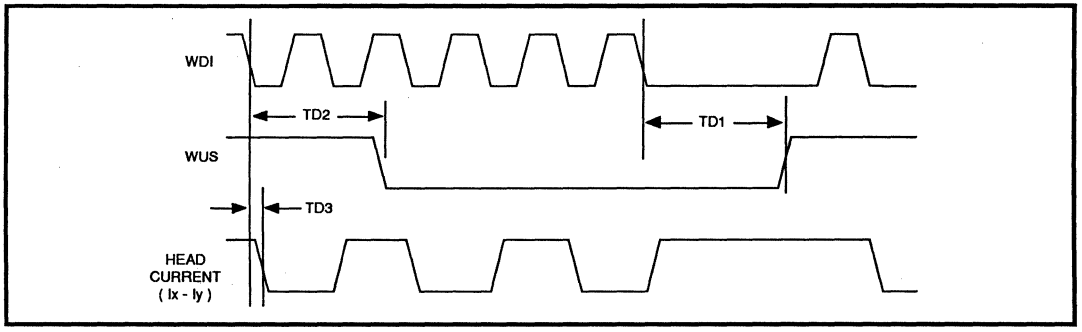
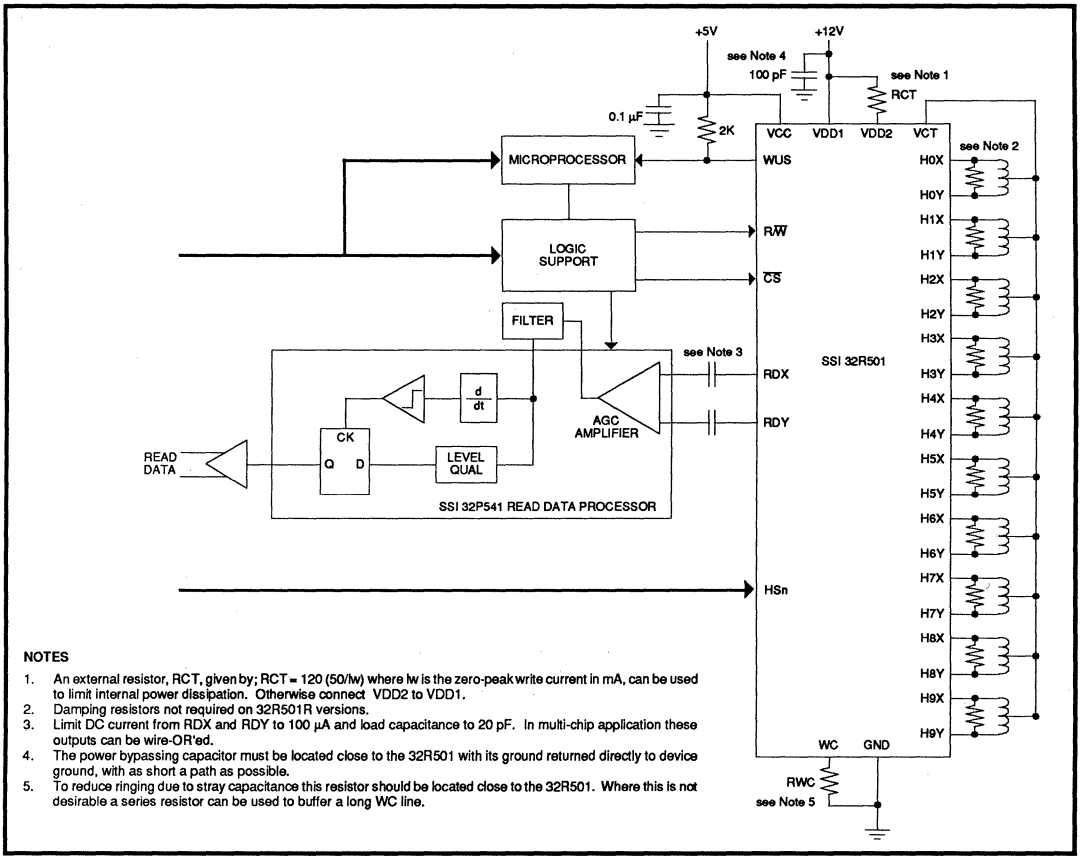


FIGURE 1: Write Mode Timing Diagram



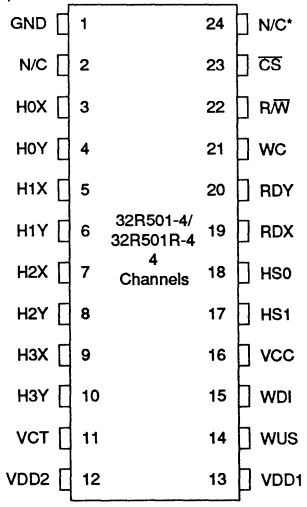
NOTES

1. An external resistor, RCT, given by; RCT = 120 (50/Iw) where Iw is the zero-peak write current in mA, can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.
2. Damping resistors not required on 32R501R versions.
3. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire-OR'ed.
4. The power bypassing capacitor must be located close to the 32R501 with its ground returned directly to device ground, with as short a path as possible.
5. To reduce ringing due to stray capacitance this resistor should be located close to the 32R501. Where this is not desirable a series resistor can be used to buffer a long WC line.

FIGURE 2: Applications Information

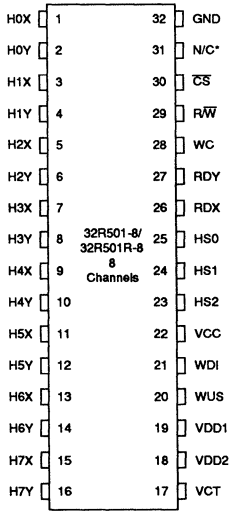
PACKAGE PIN DESIGNATIONS

(TOP VIEW)



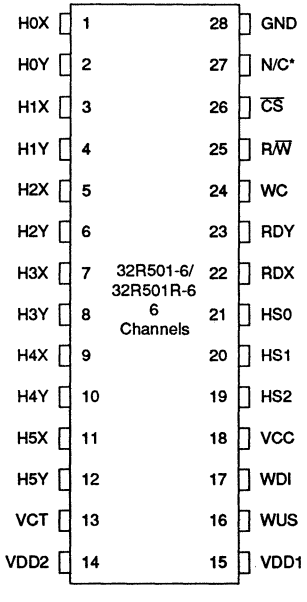
* Must remain open

24-Lead SOL



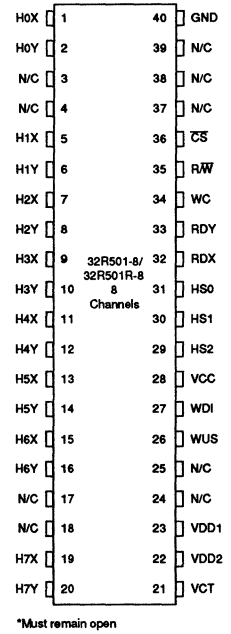
*Must remain open

32-Lead Flatpack, SOW



*Must remain open

28-Lead PDIP, SOL, Flatpack

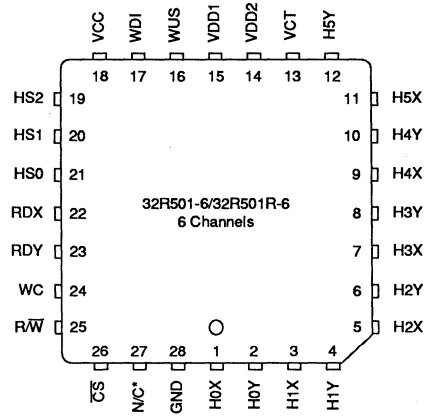


*Must remain open

40-Lead PDIP

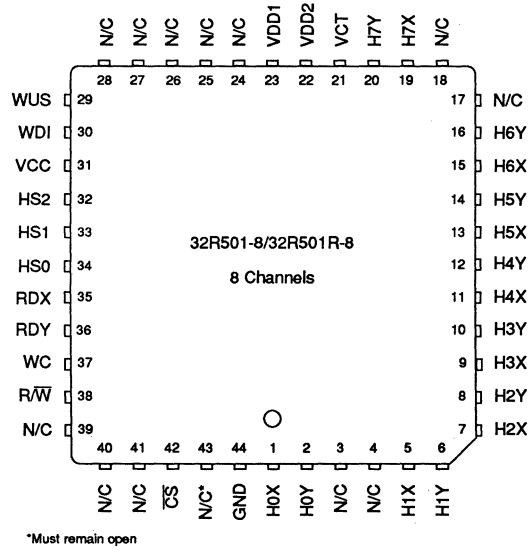
SSI 32R501/501R
4, 6, 8-Channel Ferrite Read/Write Circuit

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



*Must remain open

28-Lead PLCC



*Must remain open

44-Lead PLCC

THERMAL CHARACTERISTICS: 0ja

24-lead	SOL	80°C/W	32-lead	FLATPACK	95°C/W
28-lead	PDIP	55°C/W		SOW	55°C/W
	PLCC	65°C/W	40-lead	PDIP	45°C/W
	SOL	70°C/W	44-lead	PLCC	60°C/W
	Flatpack	100°C/W			

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R501		
4-Channel SOL	SSI 32R501-4CL	32R501-4CL
6-Channel Flatpack	SSI 32R501-6F	32R501-6F
6-Channel PLCC	SSI 32R501-6CH	32R5O1-6CH
6-Channel SOL	SSI 32R501-6CL	32R501-6CL
6-Channel PDIP	SSI 32R501-6CP	32R501-6CP
8-Channel Flatpack	SSI 32R501-8F	32R501-8F
8-Channel SOW	SSI 32R501-8CW	32R501-8CW
8-Channel PDIP	SSI 32R501-8CP	32R501-8CP
8-Channel PLCC	SSI 32R501-8CH	32R501-8CH
SSI 32R501R		
4-Channel SOL	SSI 32R501R-4CL	32R501R-4CL
6-Channel Flatpack	SSI 32R501R-6F	32R501R-6F
6-Channel PLCC	SSI 32R501R-6CH	32R501R-6CH
6-Channel SOL	SSI 32R501R-6CL	32R501R-6CL
6-Channel PDIP	SSI 32R501R-6CP	32R501R-6CP
8-Channel Flatpack	SSI 32R501R-8F	32R501R-8F
8-Channel SOW	SSI 32R501R-8CW	32R501R-8CW
8-Channel PDIP	SSI 32R501R-8CP	32R501R-8CP
8-Channel PLCC	SSI 32R501R-8CH	32R501R-8CH

silicon systems™
Silicon Systems, Inc., 14351 Myford Road, Tustin CA 92680, (714) 731-7110, TWX 910-595-2809

NOTES:

SSI 32R510A/510AR
2, 4, 6-Channel Read/Write Device

July, 1988

1

DESCRIPTION

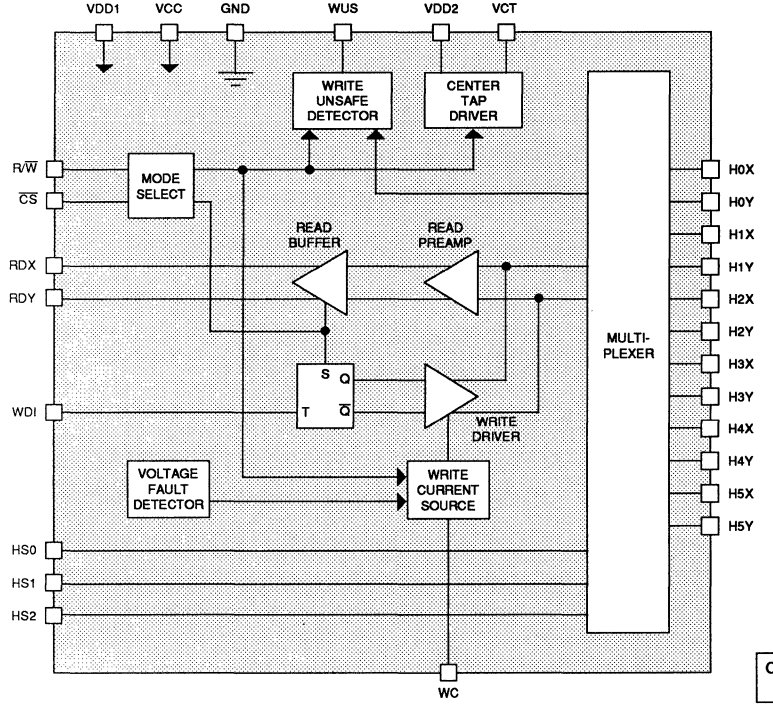
The SSI 32R510A is a bipolar monolithic integrated circuit designed for use with a center-tapped ferrite recording head. It provides a low noise read path, write current control, and data protection circuitry for as many as 6 channels. The SSI 32R510A requires +5V and +12V power supplies and is available in a variety of packages.

The SSI 32R510AR performs the same function as the SSI 32R510A with the addition of internal 750Ω damping resistors.

FEATURES

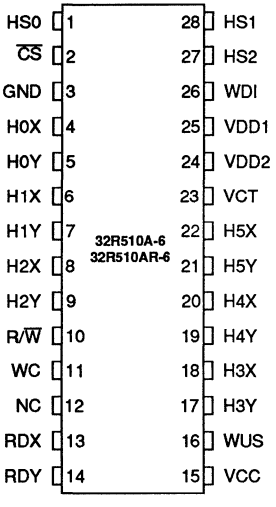
- **High performance:**
  - **Read mode gain = 100 V/V**
  - **Input noise = 1.5 nV/√Hz max.**
  - **Input capacitance = 20 pF max.**
  - **Write current range = 10 mA to 40 mA**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Plug compatible to the SSI 32R117**
- **Designed for center-tapped ferrite heads**
- **Programmable write current source**
- **Write unsafe detection**
- **TTL compatible control signals**
- **+5V, +12V power supplies**

BLOCK DIAGRAM



PIN DIAGRAM

(6-Channel)



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32R510A has the ability to address up to 6 center-tapped ferrite heads and provide write drive or read amplification. Head selection and mode control are accomplished using the HSn, $\overline{CS}$ and R/$\overline{W}$ inputs as shown in tables 1 & 2. Internal pullups are provided for the $\overline{CS}$ & R/$\overline{W}$ inputs to force the device into a non-writing condition if either control line is opened accidentally.

TABLE 1: MODE SELECT

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	x	Idle

TABLE 2: HEAD SELECT

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	x	None

0 = Low level 1 = High level x = Don't care

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SSI 32R510A as a current switch and activates the Write Unsafe (WUS) detector circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding read mode selection initializes the Write Data Flip-Flop, WDFF, to pass write current through the "X" side of the head. The zero-peak write current magnitude is programmed by an external resistor Rwc from pin WC to GND and is given by:

Iw = K/Rwc, where K = Write Current Constant

The Write Unsafe detection circuitry monitors voltage transitions at the selected head connections and flags any of the following conditions as a high level on the Write Unsafe open collector output:

- Head open
- WDI frequency too low
- Device not selected
- Head center tap open
- Device in read mode
- No write current

Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

To further assure data security a voltage fault detection circuit prevents application of write current during power loss or power sequencing.

To enhance write to read recovery time the change in RDX, RDY common mode voltage is minimized by biasing these outputs to a level within the read mode range when in write mode.

Power dissipation in write mode may be reduced by placing a resistor (RCT) between VDD1 & VDD2. The optimum resistor value is 150Ω x 40 /Iw (Iw in mA). At low write currents (<15mA) read mode dissipation is higher than write mode and RCT, though recommended, may not be considered necessary. In this case VDD2 is connected directly to VDD1.

READ MODE

Taking $\overline{CS}$ low and R/$\overline{W}$ high selects read mode which configures the SSI 32R510A as a low noise differential amplifier for the selected head. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head paths. These outputs should be AC coupled to the load. The internal write current source is gated off in read mode eliminating the need for any external gating.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX, RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0-HS2	I	Head Select
$\overline{CS}$	I	Chip Select: a low level enables device
R/$\overline{W}$	I	Read/Write: a high level selects read mode
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition
WDI	I	Write Data In: negative transition toggles direction of head current
H0X-H5X H0Y-H5Y	I/O	X,Y head connections
RDX, RDY	O*	X, Y Read Data: differential read signal out
WC	*	Write Current: used to set the magnitude of the write current
VCT		Voltage Center Tap: voltage source for head center tap
VCC		+5V
VDD1		+12V
VDD2		Positive power supply for the center tap voltage source
GND		Ground

*When more than one R/W device is used, these signals can be wire OR'ed.

ABSOLUTE MAXIMUM RATINGS (Operation above absolute maximum ratings may permanently damage the device. All voltages referenced to GND. Currents into device are positive.)

PARAMETER		VALUE	UNITS
DC Supply Voltage	VDD1	-0.3 to +14	VDC
DC Supply Voltage	VDD2	-0.3 to +14	VDC
DC Supply Voltage	VCC	-0.3 to +6	VDC
Digital Input Voltage Range	VIN	-0.3 to VCC + 0.3	VDC
Head Port Voltage Range	VH	-0.3 to VDD1 + 0.3	VDC
WUS Pin Voltage Range	Vwus	-0.3 to +14	VDC
Write Current (Zero Peak)	IW	60	mA
RDX, RDY Output Current	Io	-10	mA
VCT Output Current	Ivct	-60	mA
WUS Output Current	Iwus	+12	mA
Storage Temperature Range	Tstg	-65 to 150	°C
Lead Temperature PDIP, Flat Pack (10 sec Soldering)		260	°C
Package Temperature PLCC, SO (20 sec Reflow)		215	°C

RECOMMENDED OPERATION CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DC Supply Voltage	VDD1		10.8	12.0	13.2	VDC
DC Supply Voltage	VCC		4.5	5.0	5.5	VDC
Head Inductance	Lh		5		15	µH
Damping Resistor	RD	32R510A only	500		2000	Ω
RCT Resistor	RCT	Iw = 40 mA, see Note	124	130	136	Ω
Write Current	IW		10		40	mA
Junction Temperature Range	Tj		+25		+135	°C

Note: For Iw = 40mA. At other Iw levels refer to Applications Information that follows this specification.

DC CHARACTERISTICS

(Unless otherwise specified, recommended operating conditions apply.)

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Supply Current	Read/Idle Mode			35	mA
	Write Mode			30	mA
VDD Supply Current (sum of VDD1 and VDD2)	Idle Mode			20	mA
	Read Mode			35	mA
	Write Mode			20 + Iw	mA
Power Dissipation (Tj = +125°C)	Idle Mode			400	mW
	Read Mode			600	mW
	Write Mode, IW = 40 mA, RCT = 0Ω			800	mW
	Write Mode, IW = 40 mA, RCT = 130Ω			600	mW

DC CHARACTERISTICS (continued)

DIGITAL I/O

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VIL	Input Low Voltage				0.8	VDC
VIH	Input High Voltage		2.0			VDC
IIL	Input Low Current	VIL = 0.8V	-0.4			mA
IIH	Input High Current	VIH = 2.0V			100	µA
VOL	WUS Output Low Voltage	IOL = 8 mA			0.5	VDC
IOH	WUS Output High Current	VOH = 5.0V			100	µA

WRITE MODE

Center Tap Voltage (VCT)	Write Mode		6.0		VDC
Head Current (per side)	Write Mode, 0≤VCC≤3.7V, 0≤VDD1≤8.7V	-200		+200	µA
Write Current Range		10		40	mA
Write Current Constant "K"		2.375		2.625	
Iwc to Head Current Gain			0.99		mA/mA
Unselected Head Leakage Current				85	µA
RDX, RDY Output Offset Voltage	Write/Idle Mode	-20		+20	mV
RDX, RDY Common Mode Output Voltage	Write/Idle Mode		5.3		VDC
RDX, RDY Leakage	RDX, RDY = 6V Write/Idle Mode	-100		+100	µA

READ MODE

Center Tap Voltage	Read Mode		4.0		VDC
Head Current (per side)	Read or Idle Mode 0 ≤ VCC ≤ 5.5V 0 ≤ VDD1 ≤ 13.2V	-200		+200	µA
Input Bias Current (per side)				45	µA
Input Offset Voltage	Read Mode	-440		+440	mV
Common Mode Output Voltage	Read Mode	4.5		6.5	VDC

DYNAMIC CHARACTERISTICS AND TIMING

(Unless otherwise specified, recommended operating conditions apply, IW = 35 mA, Lh = 10 µH, Rd = 750Ω, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 20 pF.)

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Head Voltage Swing		7.0			V(pk)
Unselected Head Transient Current				2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	32R510A	10K			Ω
	32R510AR	600		960	Ω
WDI Transition Frequency	WUS = low	250			kHz

READ MODE

Differential Voltage Gain	Vin = 1 mVpp @ 300 KHz RL(RDX), RL(RDY) = 1 KΩ	85		115	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10%, Vin = Vi + 0.5 mVpp @ 300 KHz	-3		+3	mV
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	30			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			1.5	nV/√Hz
Differential Input Capacitance	f = 5 MHz			20	pF
Differential Input Resistance	32R510A, f = 5 MHz	2K			Ω
	32R510AR, f = 5 MHz	460		860	Ω
Common Mode Rejection Ratio	Vcm = VCT + 100 mVpp @ 5 MHz	50			dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VDD1, VDD2 or VCC	45			dB
Channel Separation	Unselected Channels: Vin=100 mVpp @ 5 MHz; Selected Channel: Vin = 0 mVpp	45			dB
Single Ended Output Resistance	f = 5 MHz			30	Ω
Output Current	AC Coupled Load, RDX to RDY	2.1			mA

DYNAMIC CHARACTERISTICS AND TIMING (continued)

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
R/$\overline{W}$ To Write	Delay to 90% of write current			1.0	µs
R/$\overline{W}$ to Read	Delay to 90% of 100 mV 10 MHz read signal envelope or to 90 % of write current			1.0	µs
$\overline{CS}$ to Select	Delay to 90% of write current or to 90% of 100mV 10MHz read signal envelope			1.0	µs
$\overline{CS}$ to Unselect	Delay to 90% decay of write current			1.0	µs
HS0 - HS2 to any head	Delay to 90% of 100 mV 10 MHz read signal envelope			1.0	µs
WUS, Safe to Unsafe - TD1	Iw = 35 mA	1.6		8.0	µs
WUS, Unsafe to Safe - TD2	Iw = 35 mA			1.0	µs
Head Current (Lh = 0 µH, Rh = 0Ω)					
Prop. Delay - TD3	From 50% points			25	ns
Asymmetry	WDI has 50% duty cycle and 1ns rise/fall time			2	ns
Rise/Fall Time	10% - 90% points			20	ns

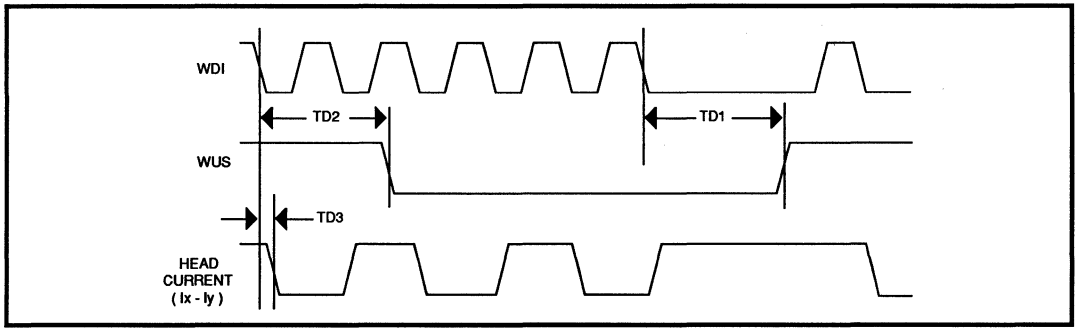
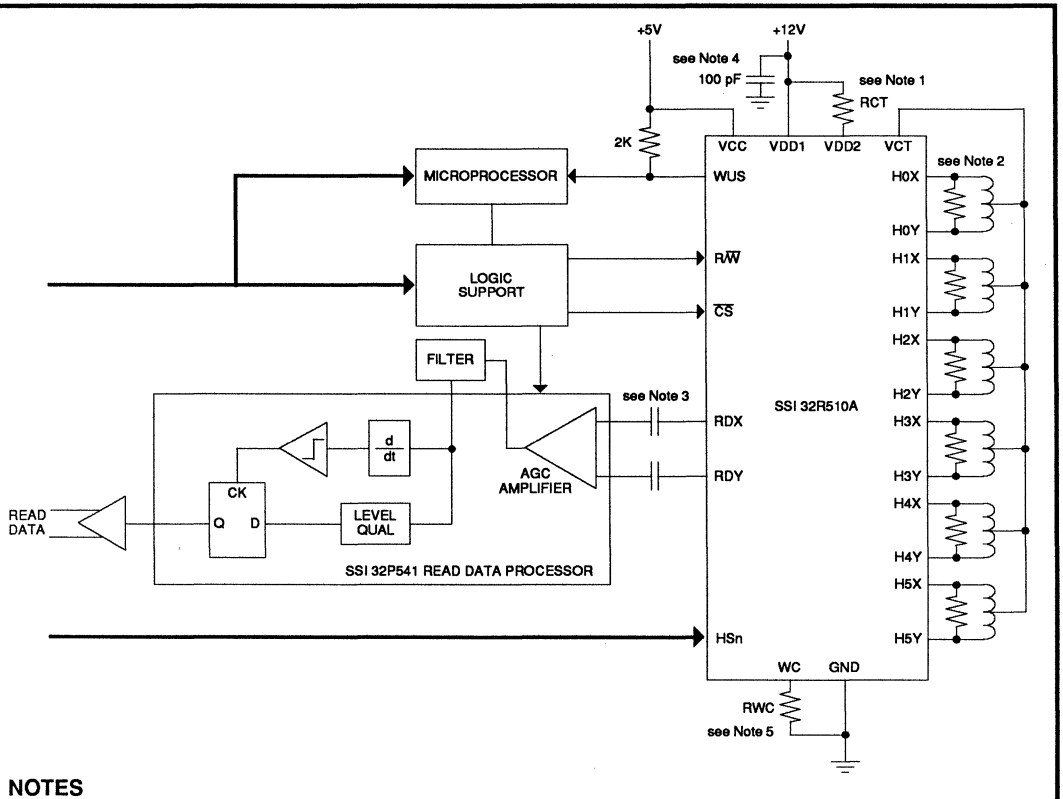


FIGURE 1: Write Mode Timing Diagram



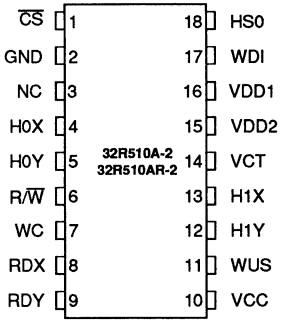
NOTES

1. An external resistor, RCT, given by; RCT = 130 (40/Iw) where Iw is the zero-peak write current in mA, can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.
2. Damping resistors not required on 32R510AR versions.
3. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire-OR'ed.
4. The power bypassing capacitor must be located close to the 32R510A with its ground returned directly to device ground, with as short a path as possible.
5. To reduce ringing due to stray capacitance this resistor should be located close to the 32R510A. Where this is not desirable a series resistor can be used to buffer a long WC line. In multi-chip applications a single resistor common to all chips may be used.

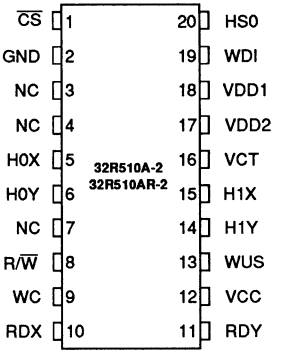
FIGURE 2: Applications Information

PACKAGE PIN DESIGNATIONS

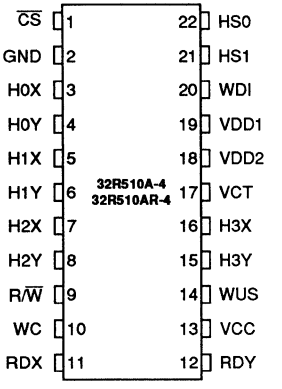
(TOP VIEW)



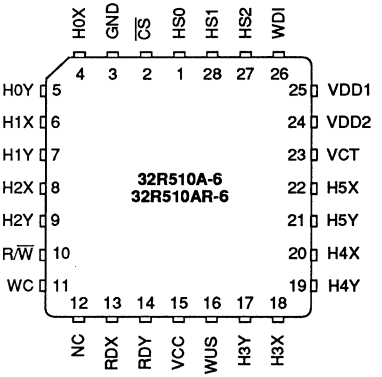
18-lead PDIP



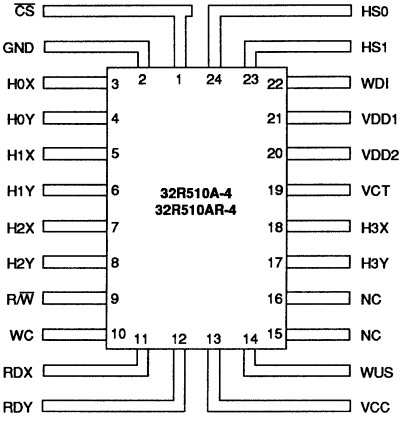
20-lead SOL



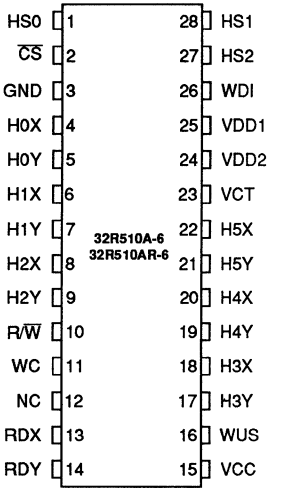
22-lead PDIP



28-lead PLCC



24-lead Flatpack, SOL



28-lead PDIP, Flatpack, SOL

THERMAL CHARACTERISTICS

PACKAGE		Øja	PACKAGE		Øja
18-lead	PDIP	140	28-lead	Flatpack	100
20-lead	SOL	95		PLCC	65
22-lead	PDIP	65		PDIP	55
24-lead	Flatpack	105		SOL	70
	SOL	80			

SSI 32R510A/510AR
2, 4, 6-Channel
Read/Write Device

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R510A		
2-Channel PDIP	SSI 32R510A-2P	32R510A-2P
2-Channel SOL	SSI 32R510A-2L	32R510A-2L
4-Channel SOL	SSI 32R510A-4CL	32R510A-4CL
4-Channel Flatpack	SSI 32R510A-4F	32R510A-4F
4-Channel PDIP	SSI 32R510A-4CP	32R510A-4CP
6-Channel PDIP	SSI 32R510A-6CP	32R510A-6CP
6-Channel SOL	SSI 32R510A-6CL	32R510A-6CL
6-Channel Flatpack	SSI 32R510A-6F	32R510A-6F
6-Channel PLCC	SSI 32R510A-6CH	32R510A-6CH
SSI 32R510AR with Internal Damping Resistor		
2-Channel PDIP	SSI 32R510AR-2P	32R510AR-2P
2-Channel SOL	SSI 32R510AR-2L	32R510AR-2L
4-Channel SOL	SSI 32R510AR-4CL	32R510AR-4CL
4-Channel Flatpack	SSI 32R510AR-4F	32R510AR-4F
4-Channel PDIP	SSI 32R510AR-4CP	32R510AR-4CP
6-Channel PDIP	SSI 32R510AR-6CP	32R510AR-6CP
6-Channel SOL	SSI 32R510AR-6CL	32R510AR-6CL
6-Channel Flatpack	SSI 32R510AR-6F	32R510AR-6F
6-Channel PLCC	SSI 32R510AR-6CH	32R510AR-6CH

silicon systems™
14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

SSI 32R511/511R
4, 6, 8-Channel Ferrite Read/Write Device

silicon systems™
INNOVATORS IN INTEGRATION

1

August, 1988

DESCRIPTION

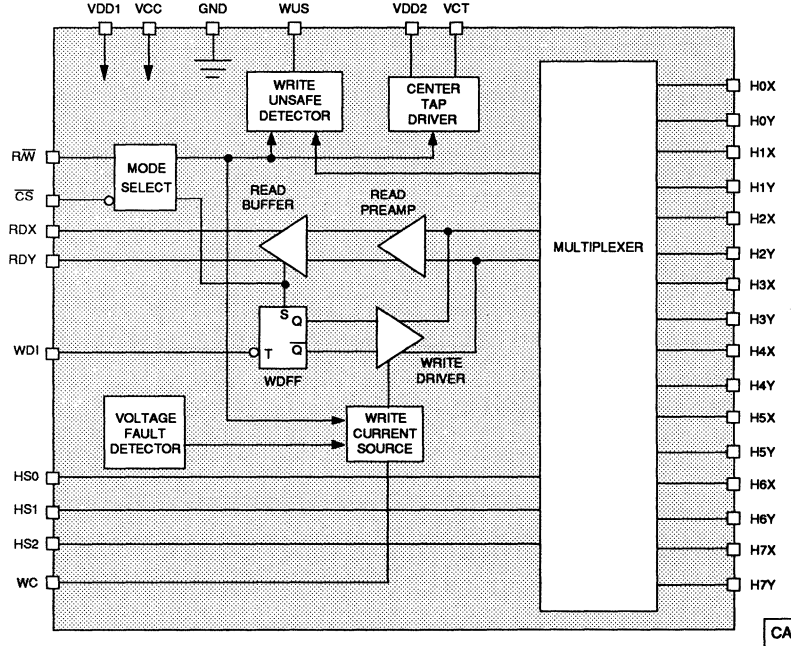
The SSI 32R511 is a bipolar monolithic integrated circuit designed for use with a center-tapped ferrite recording head. The SSI 32R511 offers the performance upgrades of the SSI 32R510A, along with the improved pin arrangement of the SSI 32R501. It provides a low noise read path, write current control, and data protection ciruitry for as many as 8 channels. The SSI 32R511 requires +5V and +12V power supplies and is available in a variety of packages.

The SSI 32R511R performs the same function as the SSI 32R511 with the addition of internal 750Ω damping resistors. The SSI 32R511M and SSI 32R511RM are functionally equivalent to the SSI 32R511 and SSI 32R511R however, they have the mirror image pin arrangement to simplify layout when using multiple devices.

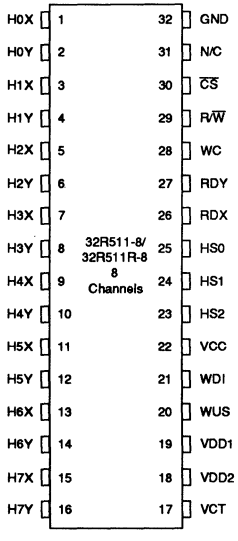
FEATURES

- **High performance**
  - **Read mode gain = 100 V/V**
  - **Input noise = 1.5 nV/√Hz maximum**
  - **Input capacitance = 20 pF**
  - **Write current range = 10 mA to 40 mA**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Pin compatible with the SSI 32R501/501R**
- **Designed for center-tapped ferrite heads**
- **Programmable write current source**
- **Easily multiplexed for larger systems**
- **Includes write unsafe detection**
- **TTL compatible control signals**
- **+5V, +12V power supplies**
- **Mirror image pin arrangements**

BLOCK DIAGRAM



PIN DIAGRAM



32-LEAD SOW

CAUTION: Use handling procedures necessary for a static sensitive component.

0888

CIRCUIT OPERATION

The SSI 32R511 gives the user the ability to address up to 8 center-tapped ferrite heads and provide write drive or read amplification. Head selection and mode control is accomplished using the HSn, $\overline{CS}$ and R/$\overline{W}$ inputs as shown in tables 1 & 2. Internal pullups are provided for the $\overline{CS}$ & R/$\overline{W}$ inputs to force the device into a non-writing condition if either control line is opened accidentally.

TABLE 1: MODE SELECT

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TABLE 2: HEAD SELECT

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

0 = Low level 1 = High level

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SSI 32R511 as a current switch and activates the Write Unsafe (WUS) detector circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding read mode selection initializes the Write Data Flip-Flop, WDFF, to pass write current through the "X" side of the head. The zero-peak write current magnitude is programmed by an external resistor Rwc from pin WC to GND and is given by:

Iw = K/Rwc, where K = Write Current Constant

The Write Unsafe detection circuitry monitors voltage transitions at the selected head connections and flags any of the following conditions as a high level on the Write Unsafe open collector output:

- Head open
- Head center tap open
- WDI frequency too low
- Device in read mode
- Device not selected
- No write current

Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

To further assure data security a voltage fault detection circuit prevents application of write current during power loss or power sequencing.

To enhance write to read recovery time the change in RDX, RDY common mode voltage is minimized by biasing these outputs to a level within the read mode range when in write mode.

Power dissipation in write mode may be reduced by placing a resistor (RCT) between VDD1 & VDD2. The optimum resistor value is 120Ω x 40 /Iw (Iw in mA). At low write currents (<15 mA) read mode dissipation is higher than write mode and RCT, though recommended, may not be considered necessary. In this case VDD2 is connected directly to VDD1.

READ MODE

Taking $\overline{CS}$ low and R/$\overline{W}$ high selects read mode which configures the SSI 32R511 as a low noise differential amplifier for the selected head. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The internal write current source is gated off in read mode eliminating the need for any external gating.

Read mode selection also initializes the Write Data Flip-Flop (WDFF) to pass write current through the "X" side of the head at a subsequent write mode selection.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX, RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0-HS2	I	Head Select
$\overline{CS}$	I	Chip Select: a low level enables device
R/$\overline{W}$	I	Read/Write: a high level selects read mode
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition
WDI	I	Write Data In: negative transition toggles direction of head current
H0X-H7X H0Y-H7Y	I/O	X,Y head connections
RDX, RDY	O*	X, Y Read Data: differential read signal out
WC	*	Write Current: used to set the magnitude of the write current
VCT	-	Voltage Center Tap: voltage source for head center tap
VCC	-	+5V
VDD1	-	+12V
VDD2	-	Positive power supply for the center tap voltage source
GND	-	Ground

*When more than one R/W device is used, these signals can be wire OR'ed.

ABSOLUTE MAXIMUM RATINGS (All voltages referenced to GND. Currents into device are positive.)

PARAMETER		VALUE	UNITS
DC Supply Voltage	VDD1	-0.3 to +14	VDC
DC Supply Voltage	VDD2	-0.3 to +14	VDC
DC Supply Voltage	VCC	-0.3 to +6	VDC
Digital Input Voltage Range	VIN	-0.3 to VCC + 0.3	VDC
Head Port Voltage Range	VH	-0.3 to VDD1 + 0.3	VDC
WUS Pin Voltage Range	Vwus	-0.3 to +14	VDC
Write Current Zero Peak	IW	60	mA
RDX, RDy Output Current	Io	-10	mA
VCT Output Current	IVCT	-60	mA
WUS Output Current	Iwus	+12	mA
Storage Temperature Range	Tstg	-65 to 150	°C
Lead Temperature PDIP, Flat Pack (10 sec Soldering)		260	°C
Package Temperature PLCC, SO (20 sec Reflow)		215	°C

RECOMMENDED OPERATION CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DC Supply Voltage	VDD1		10.8	12.0	13.2	VDC
DC Supply Voltage	VCC		4.5	5.0	5.5	VDC
Head Inductance	Lh		5		15	µH
Damping Resistor	RD	32R511 only	500		2000	Ω
RCT Resistor	RCT*	Iw = 40 mA	114	120	126	Ω
Write Current	IW		10		40	mA
Junction Temperature Range	Tj		+25		+135	°C

*For Iw = 40 mA. At other Iw levels refer to Applications Information that follows this specification.

DC CHARACTERISTICS

(Unless otherwise specified, recommended operating conditions apply.)

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Supply Current	Read/Idle Mode			35	mA
	Write Mode			30	mA
VDD Supply Current	Idle Mode			20	mA
(sum of VDD1 and VDD2)	Read Mode			35	mA
	Write Mode			20 + Iw	mA
Power Dissipation (Tj = +125°C)	Idle Mode			400	mW
	Read Mode			600	mW
	Write Mode, IW = 40 mA, RCT = 0Ω			800	mW
	Write Mode, IW = 40 mA, RCT = 120Ω			610	mW

DC CHARACTERISTICS (continued)

DIGITAL I/O

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VIL	Input Low Voltage				0.8	VDC
VIH	Input High Voltage		2.0		VCC + 0.3	VDC
IIL	Input Low Current	VIL = 0.8V	-0.4			mA
IIH	Input High Current	VIH = 2.0V			100	µA
VOL	WUS Output Low Voltage	IOL = 8 mA			0.5	VDC
IOH	WUS Output High Current	VOH = 5.0V			100	µA

WRITE MODE

Center Tap Voltage	VCT	Write Mode		6.0		VDC
Head Current (per side)		Write Mode, 0 ≤ VCC ≤ 3.7V, 0 ≤ VDD1 ≤ 8.7V	-200		200	µA
Write Current Range			10		40	mA
Write Current Constant "K"			2.375		2.625	
Iwc to Head Current Gain				0.99		mA/mA
Unselected Head Leakage Current					85	µA
RDX, RDY Output Offset Voltage		Write/Idle Mode	-20		+20	mV
RDX, RDY Common Mode Output Voltage		Write/Idle Mode		5.3		VDC
RDX, RDY Leakage		RDX, RDY = 6V Write/Idle Mode	-100		100	µA

READ MODE

Center Tap Voltage	Read Mode		4.0		VDC
Head Current (per side)	Read or Idle Mode 0 ≤ VCC ≤ 5.5V 0 ≤ VDD1 ≤ 13.2V	-200		200	µA
Input Bias Current (per side)				45	µA
Input Offset Voltage	Read Mode	-4		+4	mV
Common Mode Output Voltage	Read Mode	4.5		6.5	VDC

DYNAMIC CHARACTERISTICS AND TIMING

(Unless otherwise specified, recommended operating conditions apply and IW = 35 mA, Lh = 10 µH, Rd = 750Ω 32R511 only, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 20 pF.)

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Head Voltage Swing		7.0			V(pk)
Unselected Head Transient Current				2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	32R511	10K			Ω
	32R511R	600		960	Ω
WDI Transition Frequency	WUS = low	250			KHz

READ MODE

Differential Voltage Gain	Vin = 1 mVpp @ 300 kHz, RL(RDX), RL(RDY) = 1 KΩ	85		115	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10%. Vin = Vi + 0.5 mVpp @ 300 kHz	-3		+3	mV
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	30			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			1.5	$nV/\sqrt{Hz}$
Differential Input Capacitance	f = 5 MHz			20	pF
Differential Input Resistance	32R511, f = 5 MHz	2K			Ω
Differential Input Resistance	32R511R, f = 5 MHz	460		860	Ω
Common Mode Rejection Ratio	Vcm = VCT + 100 mVpp @ 5 MHz	50			dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VDD1, VDD2 or VCC	45			dB
Channel Separation	Unselected Channels: Vin=100 mVpp @ 5 MHz; Selected Channel: Vin = 0 mVpp	45			dB
Single Ended Output Resistance	f = 5 MHz			30	Ω
Output Current	AC Coupled Load, RDX to RDY	±2.1			mA

DYNAMIC CHARACTERISTICS AND TIMING (continued)

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
R/$\overline{W}$ To Write	Delay to 90% of Write Current			1.0	µs
R/$\overline{W}$ to Read	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope or to 90% decay of Write Current			1.0	µs
$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100 mV, 10 MHz Read Signal Envelope			1.0	µs
$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current			1.0	µs
HS0 - HS2 to any head	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope			1.0	µs
WUS, Safe to Unsafe - TD1	Iw = 35 mA	1.6		8.0	µs
WUS, Unsafe to Safe - TD2	Iw = 35 mA			1.0	µs
Head Current (Lh = 0 µH, Rh = 0Ω)					
Prop. Delay - TD3	From 50% Points			25	ns
Asymmetry	WDI has 50% Duty Cycle and 1ns Rise/Fall Time			2	ns
Rise/Fall Time	10% - 90% Points			20	ns

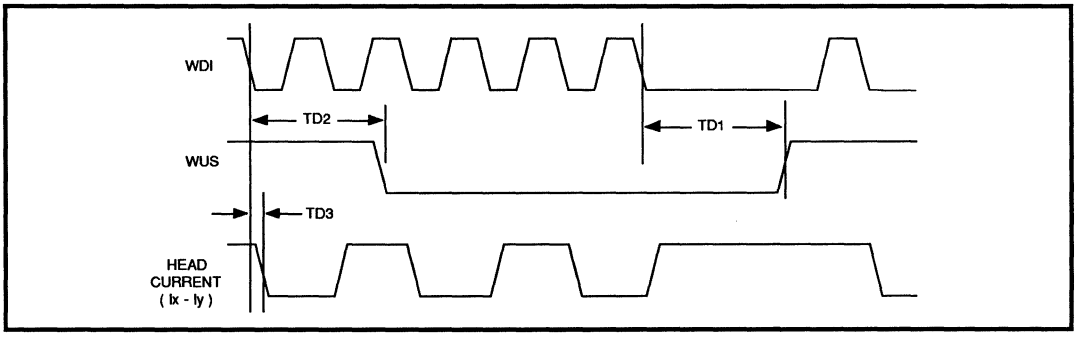
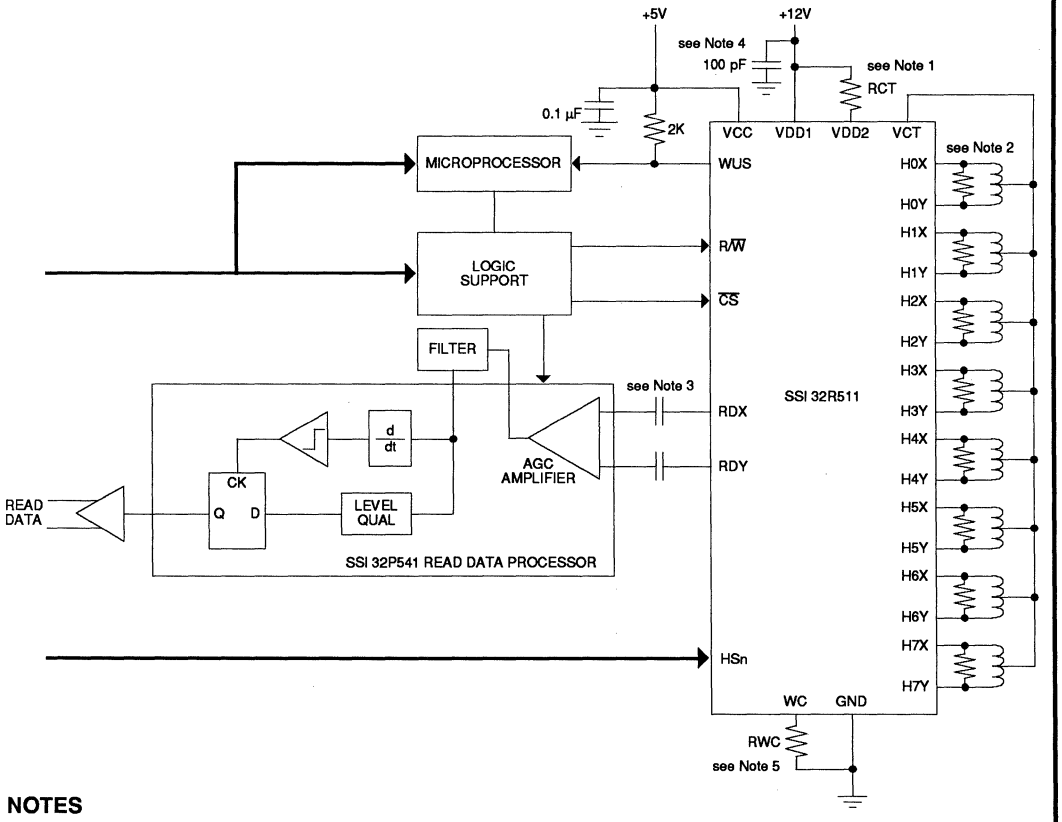


FIGURE 1: WRITE MODE TIMING DIAGRAM



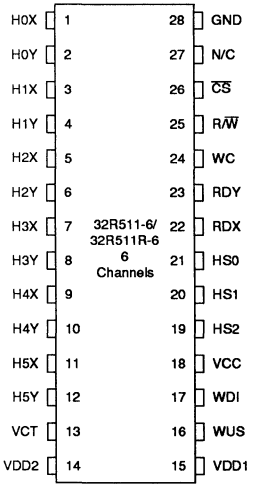
NOTES

1. An external resistor, RCT, given by; RCT = 120 (40/Iw) where Iw is the zero-peak write current in mA, can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.
2. Damping resistors not required on 32R511R versions.
3. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire-OR'ed.
4. The power bypassing capacitor must be located close to the 32R511 with its ground returned directly to device ground, with as short a path as possible.
5. To reduce ringing due to stray capacitance this resistor should be located close to the 32R511. Where this is not desirable a series resistor can be used to buffer a long WC line. In multi-chip applications a single resistor common to all chips may be used.

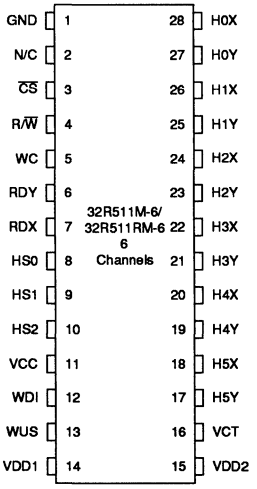
FIGURE 2: APPLICATIONS INFORMATION

1

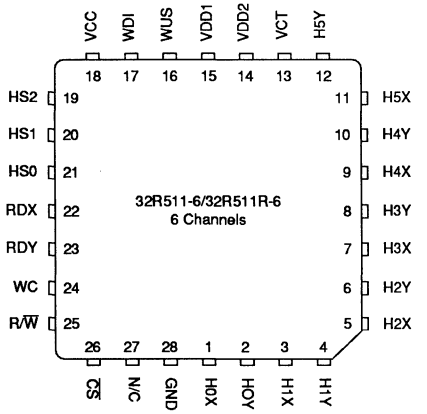
PACKAGE PIN DESIGNATIONS (Top View)



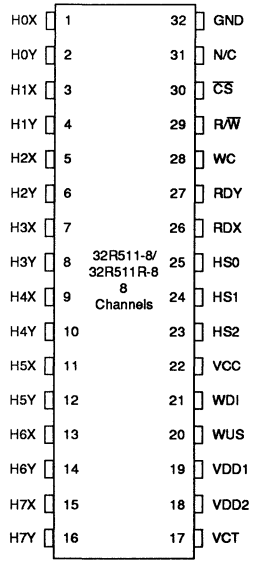
28-Lead SOL



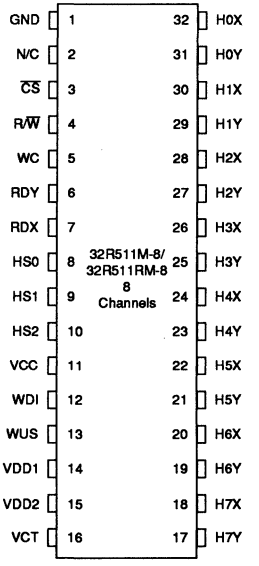
28-Lead SOL
Mirror Image



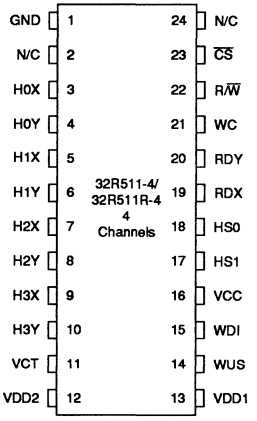
28-Lead PLCC



32-Lead Flatpack, SOW

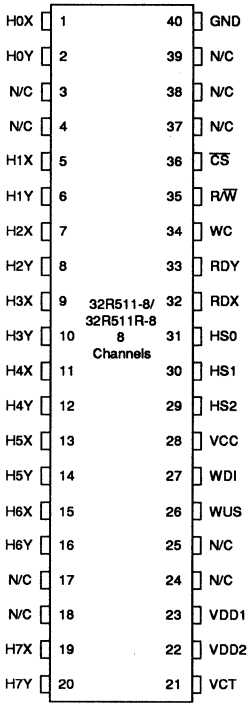


32-Lead SOW
Mirror Image

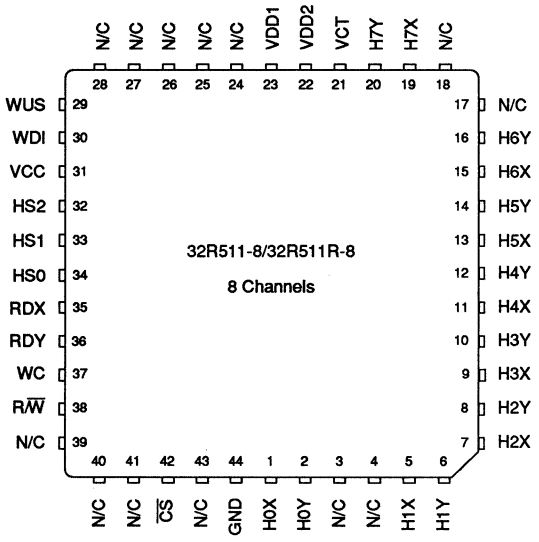


24-Lead SOL

PACKAGE PIN DESIGNATIONS (Continued)



40-Lead PDIP



44-Lead PLCC

THERMAL CHARACTERISTICS: Øja

24-lead	SOL	80°C/W
28-lead	PLCC	65°C/W
	SOL	70°C/W
32-lead	FLATPACK	95°C/W
	SOW	55°C/W
40-lead	PDIP	45°C/W
44-lead	PLCC	60°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R511		
4-Channel SOL	SSI 32R511-4CL	32R511-4CL
6-Channel PLCC	SSI 32R511-6CH	32R511-6CH
6-Channel SOL	SSI 32R511-6CL	32R511-6CL
8-Channel Flat Pack	SSI 32R511-8F	32R511-8F
8-Channel SOW	SSI 32R511-8CW	32R511-8CW
8-Channel PDIP	SSI 32R511-8CP	32R511-8CP
8-Channel PLCC	SSI 32R511-8CH	32R511-8CH
SSI 32R511R		
4-Channel SOL	SSI 32R511R-4CL	32R511R-4CL
6-Channel PLCC	SSI 32R511R-6CH	32R511R-6CH
6-Channel SOL	SSI 32R511R-6CL	32R511R-6CL
8-Channel Flat Pack	SSI 32R511R-8F	32R511R-8F
8-Channel SOW	SSI 32R511R-8CW	32R511R-8CW
8-Channel PDIP	SSI 32R511R-8CP	32R511R-8CP
8-Channel PLCC	SSI 32R511R-8CH	32R511R-8CH
SSI 32R511M		
6-Channel SOL	SSI 32R511M-6CL	32R511M-6CL
8-Channel SOW	SSI 32R511M-8CW	32R511M-8CW
SSI 32R511RM		
6-Channel SOL	SSI 32R511RM-6CL	32R511RM6CL
8-Channel SOW	SSI 32R511RM-8CW	32R511RM-8CW

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NOTES:

SSI 32R512/512R
8 & 9-Channel Thin Film Read/Write Device

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INNOVATORS IN INTEGRATION

1

August 1988

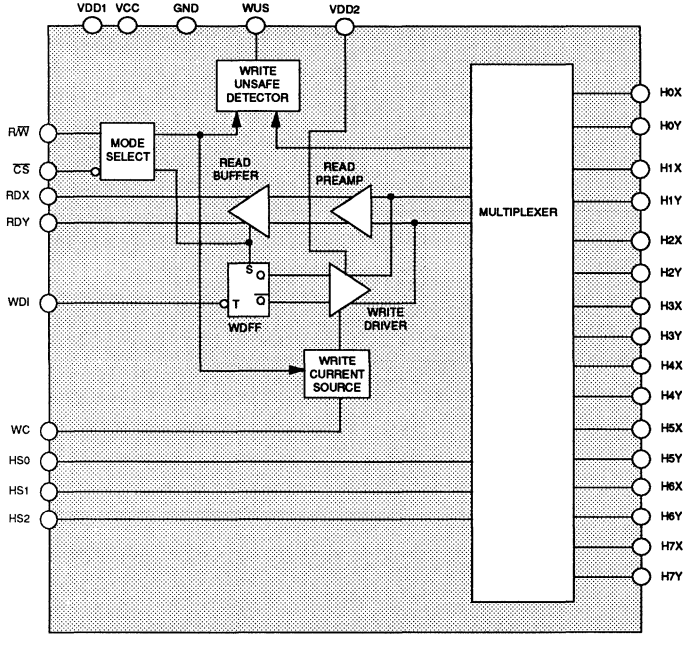
DESCRIPTION

The SSI 32R512/512R Read/Write devices are bipolar monolithic integrated circuits designed for use with two terminal thin film recording heads. They provide a low noise read amplifier, write current control and data protection circuitry for eight or nine channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. They require +5V and +12V power supplies and are available in a variety of package configurations. A mirror image pinout option is available to simplify flex circuit layout in multiple R/W device applications. The SSI 32R512R option provides internal 1000Ω damping resistors.

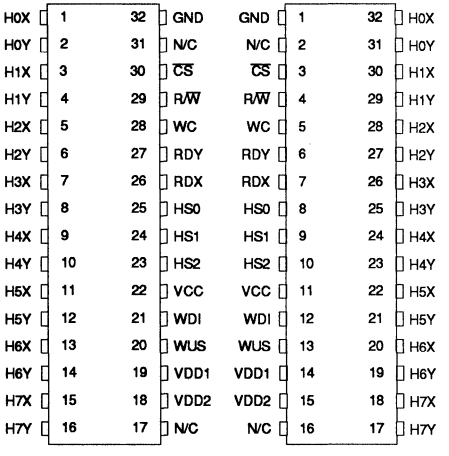
FEATURES

- **High performance:**
  - **Read mode gain = 150 V/V**
  - **Input noise = 0.85 nV/√Hz max.**
  - **Input capacitance = 40 pF max.**
  - **Write current range = 10 mA to 40 mA**
  - **Head voltage swing = 7 Vpp**
  - **Write current rise time = 9 nsec**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Plug compatible to the SSI 32R501 & SSI 32R511**
- **Compatible with two & three terminal thin film heads**
- **Write unsafe detection**
- **+5V, +12V power supplies**
- **Mirror image pinout option**

BLOCK DIAGRAM



PIN DIAGRAM



32-LEAD SOW, FLATPACK

32-LEAD SOW MIRROR

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32R512/512R
8 & 9-Channel Thin Film Read/Write Device

CIRCUIT OPERATION

The SSI 32R512 addresses up to nine two-terminal thin film heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

WRITE MODE

The write mode configures the SSI 32R512 as a current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high to low transition on pin WDI, Write Data Input.

A preceding read operation initializes the Write Data Flip Flop (WDFF) to pass write current in the X-direction of the head.

The magnitude of the write current (0-pk) given by:

$$Iw = \frac{Vwc}{RWC}$$

where Vwc (WC pin voltage) = 1.65V ± 5%, is programmed by an external resistor RWC, connected from pin WC to ground. In multiple device applications, a single RWC resistor may be made common to all devices. The actual head current Ix, y is given by:

$$Ix,y = \frac{Iw}{1 + Rh/Rd}$$

where:
Rh = head resistance + external wire resistance, and
Rd = damping resistance.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on pin WDI, after the fault is corrected, are required to clear the WUS flag.

- WDI frequency too low
- Device not selected
- Device in read mode
- No write current

Power dissipation in Write Mode may be reduced by placing a resistor, Rw, between VDD1 and VDD2. The resistor value should be chosen such that Iw Rw ≤ 3.0V for an accompanying reduction of $(Iw)^2$ Rw in power dissipation. If a resistor is not used, VDD2 should be connected to VDD1. Note that Rw will also provide current limiting in the event of a head short.

READ MODE

The read mode configures the SSI 32R512 as a low noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent Pulse Detection circuitry.

IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

TABLE 1: MODE SELECT

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: HEAD SELECT

HS3	HS2	HS1	HS0	HEAD
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

0 = Low level 1 = High level

PIN DESCRIPTIONS

NAME	TYPE	DESCRIPTION
HS0 - HS3	I	Head Select
$\overline{CS}$	I	Chip Select: a low level enables the device
R/$\overline{W}$	I	Read/Write: a high level selects Read mode
WUS	O*	Write Unsafe: Open collector output, a high level indicates an unsafe writing condition
WDI	I	Write Data In: a negative transition toggles the direction of the head current
H0X - H8X H0Y - H8Y	I/O	X, Y Head Connections: Current in the X-direction flows into the X-port
RDX, RDY	O*	X, Y Read Data: differential read data output
WC	*	Write Current: used to set the magnitude of the write current
VCC	-	+5V Logic Circuit Supply
VDD1	-	+12V
VDD2	-	Positive Power Supply for Write current drivers
GND	-	Ground

*When more than one R/W device is used, these signals can be wire OR'ed.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	VALUE	UNITS
DC Supply Voltage		VDD1, 2	-0.3 to +14	VDC
		VCC	-0.3 to +7	VDC
Write Current		Iw	100	mA
Digital Input Voltage		Vin	-0.3 to VCC +0.3	VDC
Head Port Voltage		VH	-0.3 to VDD2 +0.3	VDC
WUS Pin Voltage Range		Vwus	-0.3 to +14	VDC
Output Current	RDX, RDY	Io	-10	mA
	WUS	Iwus	+12	mA
Storage Temperature		Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	VDD1	12 ± 10%	VDC
	VDD2	VDD1 - 3.0 to VDD1	VDC
	VCC	5 ± 10%	VDC
Operating Temperature	Tj	+25 to +135	°C

DC CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD1 Supply Current	Read Mode	-	-	34	mA
	Write Mode	-	-	38	mA
	Idle Mode	-	-	14	mA
VDD2 Supply Current	Read Mode	-	-	200	µA
	Write Mode	-	-	IW+0.4	mA
	Idle Mode	-	-	200	µA
VCC Supply Current	Read Mode	-	-	75	mA
	Write Mode	-	-	56	mA
	Idle Mode	-	-	60	mA
Power Dissipation (Tj = +135°C)	Read Mode	-	-	800	mW
	Write Mode: Iw = 20 mA, VDD2 = VDD1	-	-	1000	mW
	Write Mode: Iw = 40 mA, VDD1 - VDD2 = 3.0V	-	-	1140	mW
	Idle Mode	-	-	500	mW
Input Low Voltage (VIL)		-	-	0.8	VDC
Input High Voltage (VIH)		2.0	-	-	VDC
Input Low Current (IIL)	VIL = 0.8v	-0.4	-	-	mA
Input High Current (IHL)	VIH = 2.0v	-	-	100	µA
WUS Output Low Voltage (VOL)	Iol = 8 mA	-	-	0.5	VDC
VDD Fault Voltage		8.5	-	10.0	VDC
VCC Fault Voltage		3.5	-	4.2	VDC
Head Current (HnX, HnY)	Write Mode, 0≤VCC ≤3.5V 0≤VDD1 ≤8.5V	-200	-	+200	µA
	Read/Idle Mode 0≤VCC ≤5.5V 0≤VDD1 ≤13.2V	-200	-	+200	µA

WRITE CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 1.0 µH, Rh = 30Ω and f(WDI) = 5 MHz.

PARAMETER	CONDITIONS	MIN.	NOM	MAX	UNITS
WC Pin Voltage (Vwc)		-	1.65 ±5%	-	V
Differential Head Voltage Swing		7	-	-	Vpp
Unselected Head Current		-	-	1	mA(pk)
Differential Output Capacitance		-	-	25	pF
Differential Output Resistance	32R512R	800	1000	1350	Ω
	32R512	4K	-	-	Ω
WDI Transition Frequency	WUS = low	1.7	-	-	MHz
Write Current Range		10	-	40	mA

READ CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply CL (RDX, RDY) < 20pF and RL (RDX,RDY) = 1KΩ.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain		Vin=1mVpp @ 300 kHz	125	-	175	V/V
Bandwidth	-1dB	|Zs|<5Ω, Vin=1 mVpp @ 300 kHz	25	-	-	MHz
	-3dB	|Zs|<5Ω, Vin=1 mVpp @ 300 kHz	45	-	-	MHz
Input Noise Voltage		BW = 15 MHz, Lh = 0, Rh = 0	-	0.62	0.85	nV/√Hz
Differential Input Capacitance		Vin = 1 mVpp, f = 5 MHz	-	-	40	pF
Differential Input Resistance	32R512R	Vin = 1 mVpp, f = 5 MHz	390	-	-	Ω
	32R512	Vin = 1 mVpp, f =5 MHz	640	-	-	Ω
Dynamic Range		DC input voltage where gain falls to 90% of its 0 VDC value, Vin = VDC +0.5 mVpp, f = 5 MHz	-3	-	3	mV
Common Mode Rejection Ratio		Vin = 0 VDC+100 mVpp @ 5 MHz	54	-	-	dB
Power Supply Rejection Ratio		100 mVpp @ 5 MHz on VDD1 100 mVpp @ 5 MHz on VCC	54	-	-	dB
Channel Separation		Unselected channels driven with 100 mVpp @ 5 MHz, Vin = 0 mVpp	45	-	-	dB
Output Offset Voltage			-360	-	+360	mV
RDX, RDY Common Mode		Read Mode	2.2	2.9	3.6	VDC
Output Voltage		Write Mode	-	2.9	-	VDC
Single Ended Output Resistance		f = 5 MHz	-	-	30	Ω
Output Current		AC Coupled Load, RDX to RDY	3.2	-	-	mA

SWITCHING CHARACTERISTICS (See Figure 1)
Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 1.0 µH, Rh = 30Ω and f(WDI) = 5 MHz.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
R/$\overline{W}$				
R/$\overline{W}$ to Write Mode	Delay to 90% of write current	-	0.6	µs
R/$\overline{W}$ to Read Mode	Delay to 90% of 100mV 10MHz Read signal envelope or to 90% decay of write current	-	0.6	µs
$\overline{CS}$				
$\overline{CS}$ to Select	Delay to 90% of write current or to 90% of 100mV 10MHz Read signal envelope	-	0.6	µs
$\overline{CS}$ to Unselect	Delay to 90% of write current	-	0.6	µs
HSn				
HS0, 1, 2 to any Head	Delay to 90 % of 100mV 10MHz Read signal envelope	-	0.4	µs
WUS				
Safe to Unsafe - TD1		0.6	3.6	µs
Unsafe to Safe - TD2		-	1	µs
Head Current				
Prop. Delay - TD3	From 50 % points, Lh=0µh, Rh=0Ω	-	32	ns
Asymmetry	WDI has 50 % duty cycle and 1ns rise/fall time, Lh=0µh, Rh=0Ω	-	1	ns
Rise/Fall Time	10% - 90% points, Lh=0µh, Rh=0Ω	-	9	ns

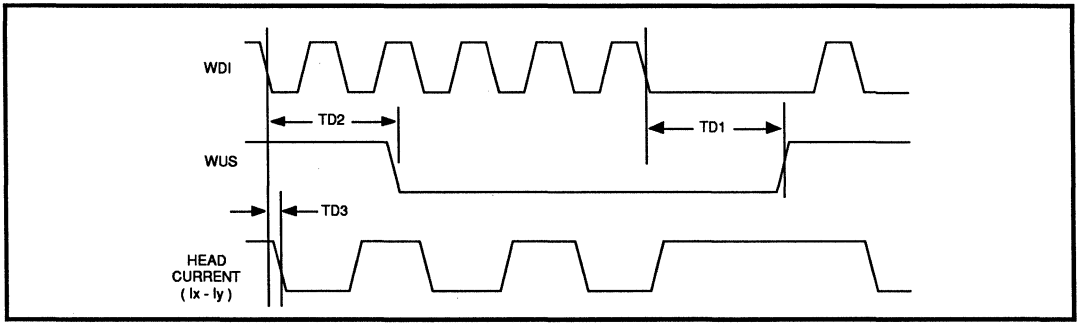


FIGURE 1: WRITE MODE TIMING DIAGRAM

APPLICATIONS INFORMATION

The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher input impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representative of actual performance.

TABLE 3: KEY PARAMETERS UNDER WORST CASE INPUT NOISE CONDITIONS

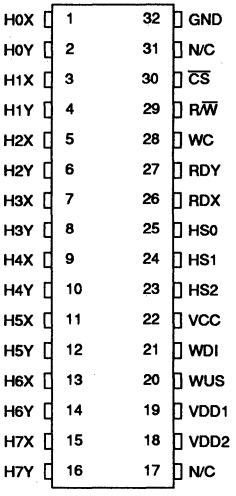
PARAMETER		Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Max.)		0.70	0.85	nV/√Hz
Differential Input Resistance (Min.)	32R512R	539	595	Ω
	32R512	1200	1500	Ω
Differential Input Capacitance (Max.)		34	36	pF

TABLE 4: KEY PARAMETERS UNDER WORST CASE INPUT IMPEDANCE CONDITIONS

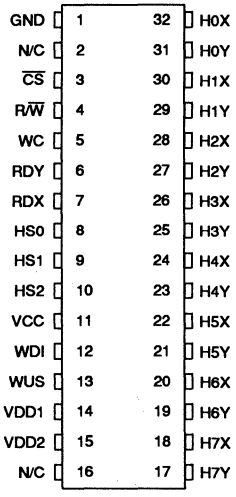
PARAMETER		Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Max.)		0.58	0.71	nV/√Hz
Differential Input Resistance (Min.)	32R512R	391	458	Ω
	32R512	643	846	Ω
Differential Input Capacitance (Max.)		38	40	pF

SSI 32R512/512R
8 & 9-Channel Thin Film Read/Write Device

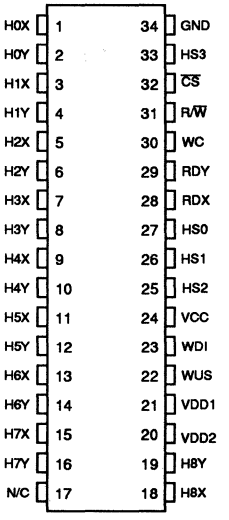
PACKAGE PIN DESIGNATIONS (Top View)



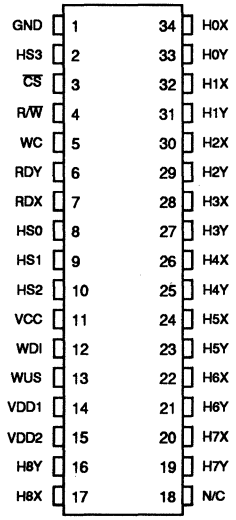
8-Channel 32-Lead SOW



8-Channel 32-Lead SOW Mirror



9-Channel 34-Lead SOL



9-Channel 34-Lead SOL Mirror

THERMAL CHARACTERISTICS: Øja

32-Lead SOW	55°C/W
34-Lead SOL	60°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R512 Read/Write IC		
8-Channel SOW	SSI 32R512-8CW	32R512-8CW
9-Channel SOL	SSI 32R512-9CL	32R512-9CL
SSI 32R512R with Internal Damping Resistor		
8-Channel SOW	SSI 32R512R-8CW	32R512R-8CW
9-Channel SOL	SSI 32R512R-9CL	32R512R-9CL
SSI 32R512M Mirror Image		
8-Channel SOW	SSI 32R512M-8CW	32R512M-8CW
9-Channel SOL	SSI 32R512M-9CL	32R512M-9CL
SSI 32R512RM Mirror Image with Damping Resistor		
8-Channel SOW	SSI 32R512RM-8CW	32R512RM-8CW
9-Channel SOL	SSI 32R512RM-9CL	32R512RM-9CL

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INNOVATORS IN INTEGRATION

SSI 32R514/514R
2, 4, 6-Channel Read/Write Device

August, 1988

1

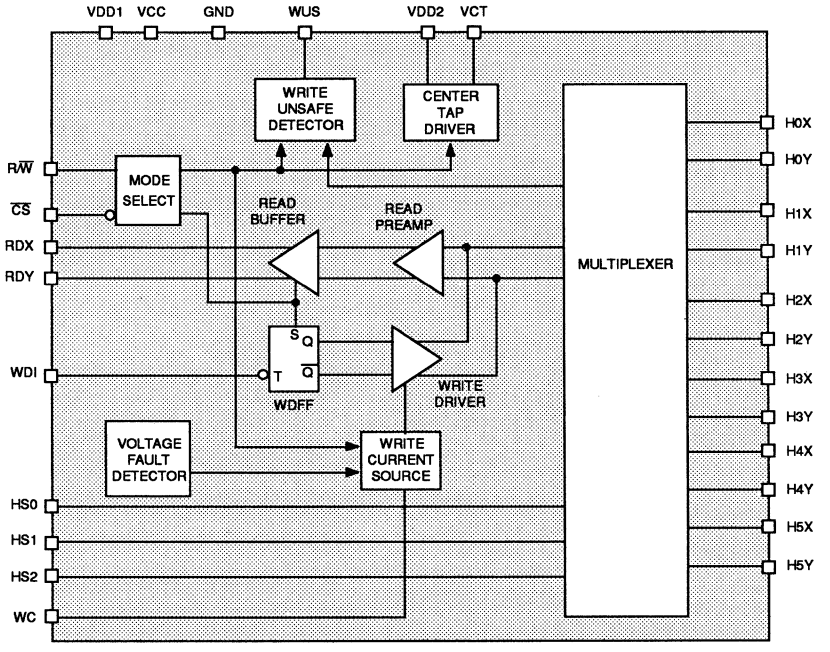
DESCRIPTION

The SSI 32R514/514R Read/Write devices are bipolar monolithic integrated circuits designed for use with center-tapped ferrite recording heads. They provide a low noise read amplifier, write current control and data protection circuitry for as many as six channels. The SSI 32R514R option provides internal 750Ω damping resistors. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. The SSI 32R514 is available in a variety of package and channel configurations.

FEATURES

- **High performance:**
  - **Read mode gain = 150 V/V**
  - **Input noise = 1.5 nV/√Hz max.**
  - **Input capacitance = 20 pF max.**
  - **Write current range = 10 mA to 40 mA**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Plug compatible to the SSI 32R117 & SSI 32R510A**
- **Designed for center-tapped ferrite heads**
- **Programmable write current source**
- **Write unsafe detection**
- **TTL compatible control signals**
- **+5V, +12V power supplies**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32R514 addresses up to six center-tapped ferrite heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$, and R/$\overline{W}$, as shown in Tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$ and R/$\overline{W}$, will force the device into a non-writing condition if either control line is opened accidentally.

TABLE 1: MODE SELECT

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TABLE 2: HEAD SELECT

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	X	None

0 = Low level 1 = High level X=Don't care

WRITE MODE

The write mode configures the SSI 32R514 as a current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI).

The magnitude of the write current (0-pk) is programmed by an external resistor RWC, connected from pin WC to ground and is given by:

$$Iw = \frac{K}{RWC}$$

where K is the Write Current Constant. In multiple device applications, a single RWC resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry monitors voltage transitions at the selected head connections and flags any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on pin WDI, after the fault is corrected, are required to clear the WUS flag.

- Head open
- WDI frequency too low
- Device not selected
- Head center tap open
- Device in read mode
- No write current

To reduce internal power dissipation, an optional external resistor, RCT, given by RCT ≤ 130Ω x 40/Iw (Iw in mA), is connected between pins VDD1 and VDD2. Otherwise connect pin VDD1 to VDD2.

To initialize the Write Data Flip Flop (WDFF) to pass current through the X-side of the head, pin WDI must be low when the previous read mode was commanded.

READ MODE

The read mode configures the SSI 32R514 as a low noise differential amplifier and deactivates the write current generator and write unsafe circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent pulse detection circuitry.

IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector, and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0-HS2	I	Head Select
$\overline{CS}$	I	Chip Select: a low level enables device
R/$\overline{W}$	I	Read/Write: a high level selects Read mode
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition
WDI	I	Write Data In: negative transition toggles direction of head current
H0X-H5X H0Y-H5Y	I/O	X,Y head connections
RDX, RDY	O*	X, Y Read Data: differential read signal output
WC	*	Write Current: used to set the magnitude of the write current
VCT	-	Voltage Center Tap: voltage source for head center tap
VCC	-	+5V
VDD1	-	+12V
VDD2	-	Positive power supply for the center-tap voltage source
GND	-	Ground

*When more than one R/W device is used, these signals can be wire OR'ed.

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND. Currents into device are positive.)

PARAMETER		VALUE	UNITS
DC Supply Voltage	VDD1	-0.3 to +14	VDC
DC Supply Voltage	VDD2	-0.3 to +14	VDC
DC Supply Voltage	VCC	-0.3 to +6	VDC
Digital Input Voltage Range	VIN	-0.3 to VCC + 0.3	VDC
Head Port Voltage Range	VH	-0.3 to VDD1 + 0.3	VDC
WUS Pin Voltage Range	Vwus	-0.3 to +14	VDC
Write Current (0-pk)	Iw	60	mA
RDX, RDY Output Current	Io	-10	mA
VCT Output Current	Ivct	-60	mA
WUS Output Current	Iwus	+12	mA
Storage Temperature Range	Tstg	-65 to 150	°C
Lead Temperature PDIP, (10 sec Soldering)		260	°C
Package Temperature PLCC, SO (20 sec Reflow)		215	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VDD1	DC Supply Voltage		10.8	12.0	13.2	VDC
VCC	DC Supply Voltage		4.5	5.0	5.5	VDC
Lh	Head Inductance		5		15	µH
RD	Damping Resistor	32R514 only	500		2000	Ω
RCT*	RCT Resistor	Iw = 40 mA	123	130	137	Ω
Iw	Write Current (0-pk)		10		40	mA
Tj	Junction Temperature Range		+25		+135	°C

*For Iw = 40 mA. At other Iw levels refer to Applications Information that follows this specification.

DC CHARACTERISTICS

(Recommended operating conditions apply unless otherwise specified.)

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Supply Current	Read/Idle Mode			35	mA
	Write Mode			30	mA
VDD Supply Current	Idle Mode			20	mA
(sum of VDD1 and VDD2)	Read Mode			35	mA
	Write Mode			20 + Iw	mA
Power Dissipation (Tj = +135°C)	Idle Mode			400	mW
	Read Mode			600	mW
	Write Mode, Iw = 40 mA, RCT = 0Ω			800	mW
	Write Mode, Iw = 40 mA, RCT = 130Ω			600	mW

DC CHARACTERISTICS (continued)

DIGITAL I/O

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VIL Input Low Voltage				0.8	VDC
VIH Input High Voltage		2.0			VDC
IIL Input Low Current	VIL = 0.8V	-0.4			mA
IIH Input High Current	VIH = 2.0V			100	µA
VOL WUS Output Low Voltage	IOL = 8 mA			0.5	VDC
IOH WUS Output High Current	VOH = 5.0V			100	µA

WRITE MODE

VCT Center Tap Voltage	Write Mode		6.7		VDC
Head Current (per side)	Write Mode, 0 ≤ VCC ≤ 3.7V, 0 ≤ VDD1 ≤ 8.7V	-200		200	µA
Write Current Range		10		40	mA
Write Current Constant "K"		2.375		2.625	
Iwc to Head Current Gain			0.99		mA/mA
Unselected Head Leakage Current				85	µA
RDX, RDY Output Offset Voltage	Write/Idle Mode	-20		+20	mV
RDX, RDY Common Mode Output Voltage	Write/Idle Mode		5.3		VDC
RDX, RDY Leakage	RDX, RDY = 6V Write/Idle Mode	-100		100	µA

READ MODE

VCT Center Tap Voltage	Read Mode		4.0		VDC
Head Current (per side)	Read or Idle Mode 0 ≤ VCC ≤ 5.5V 0 ≤ VDD1 ≤ 13.2V	-200		200	µA
Input Bias Current (per side)				45	µA
Output Offset Voltage	Read Mode	-615		+615	mV
Common Mode Output Voltage	Read Mode	4.5		6.5	VDC

DYNAMIC CHARACTERISTICS AND TIMING

Iw = 35 mA, Lh = 10 µH, Rd = 750 Ω 32R514 only, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 20 pF. Recommended operating conditions apply unless otherwise specified.

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Head Voltage Swing		7.0			V(pk)
Unselected Head Transient Current				2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	32R514	10K			Ω
	32R514R	600		960	Ω
WDI Transition Frequency	WUS = low	250			KHz

READ MODE

Differential Voltage Gain	Vin = 1 mVpp @ 300 kHz ZL(RDX), ZL(RDY) = 1 KΩ	125		175	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10% Vin = Vi + 0.5 mVpp @ 300 KHz	-2		+2	mV
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	30			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			1.5	nV/√Hz
Differential Input Capacitance	f = 5 MHz			20	pF
Differential Input Resistance	32R514, f = 5 MHz	3.2K			Ω
	32R514R, f = 5 MHz	500		1000	Ω
Common Mode Rejection Ratio	Vcm = VCT + 100 mVpp @ 5 MHz	50			dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VDD1, VDD2 or VCC	45			dB
Channel Separation	Unselected Channels: Vin=100 mVpp @ 5 MHz; Selected Channel: Vin = 0 mVpp	45			dB
Single Ended Output Resistance	f = 5 MHz			30	Ω
Output Current	AC Coupled Load, RDX to RDY	±2.1			mA

DYNAMIC CHARACTERISTICS AND TIMING (continued)

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
R/$\overline{W}$ To Write Mode	Delay to 90% of Write Current			1.0	µs
R/$\overline{W}$ to Read Mode	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope or to 90% decay of Write Current			1.0	µs
$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100 mV, 10 MHz Read Signal Envelope			1.0	µs
$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current			1.0	µs
HS0 - HS2 to any head	Delay to 90% of 100mV 10 MHz Read Signal Envelope			1.0	µs
WUS, Safe to Unsafe - TD1	Iw = 35 mA, see Figure 1	1.6		8.0	µs
WUS, Unsafe to Safe - TD2	Iw = 35 mA, see Figure 1			1.0	µs
Head Current (Lh = 0 µH, Rh = 0Ω, see Figure 1)					
Prop. Delay - TD3	From 50% Points			25	ns
Asymmetry	WDI has 50% Duty Cycle and 1ns Rise/Fall Time			2	ns
Rise/Fall Time	10% - 90% Points			20	ns

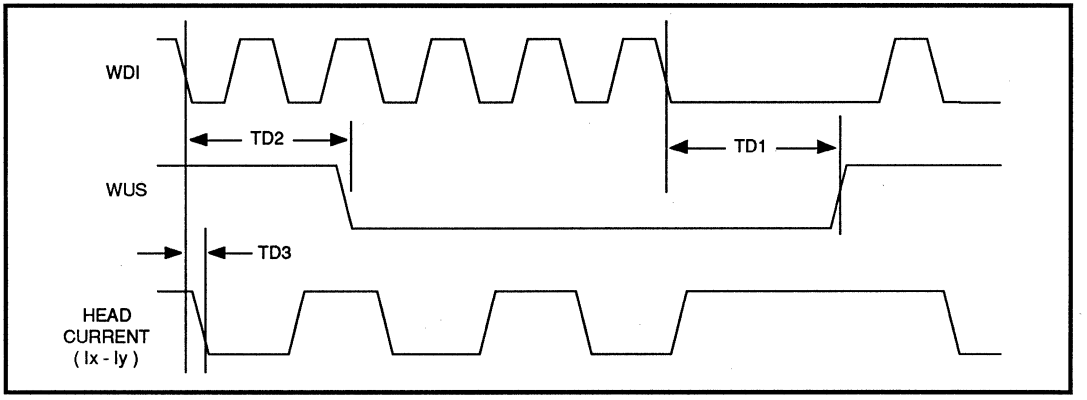


FIGURE 1: WRITE MODE TIMING DIAGRAM

APPLICATIONS INFORMATION

The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher input impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representative of actual performance.

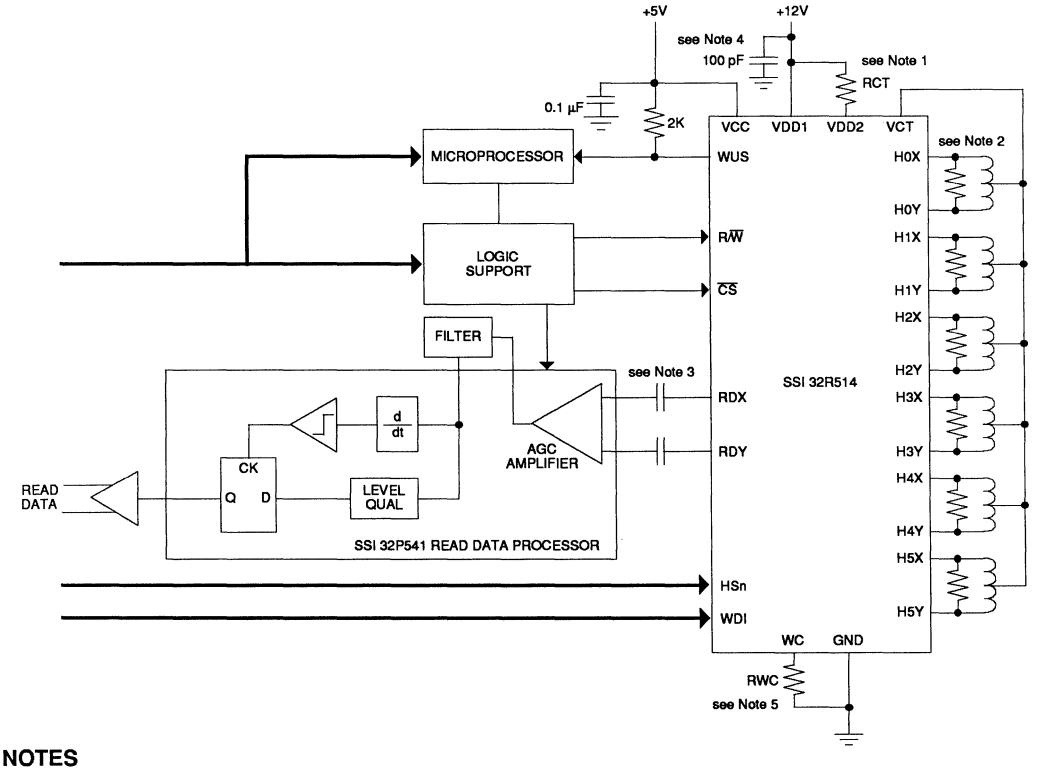
TABLE 3: KEY PARAMETERS UNDER WORST CASE INPUT NOISE CONDITIONS

PARAMETER		Tj=25°C	Tj=135°C	UNITS
Inputs Noise Voltage (max.)		1.1	1.5	nV/√Hz
Differential Input Resistance (min.)	32R514R	850	1000	Ω
	32R514	15.4	29.4	KΩ
Differential Input Capacitance (max.)		11.6	10.8	pF

TABLE 4: KEY PARAMETERS UNDER WORST CASE INPUT IMPEDANCE CONDITIONS

PARAMETER		Tj=25°C	Tj=135°C	UNITS
Inputs Noise Voltage (max.)		0.92	1.2	nV/√Hz
Differential Input Resistance (min.)	32R514R	500	620	Ω
	32R514	3.2	6.1	KΩ
Differential Input Capacitance (max.)		10.1	10.3	pF

APPLICATIONS INFORMATION (continued)



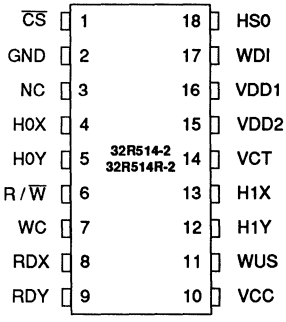
NOTES

1. An external resistor, RCT, given by; RCT ≤ 130 (40/Iw) where Iw is the zero-peak write current in mA, can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.
2. Damping resistors not required on 32R514R versions.
3. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire OR'ed.
4. The power bypassing capacitor must be located close to the device with its ground returned directly to device ground, with as short a path as possible.
5. To reduce ringing due to stray capacitance this resistor should be located close to the device. Where this is not desirable a series resistor can be used to buffer a long WC line. In multi-chip applications a single resistor common to all chips may be used.

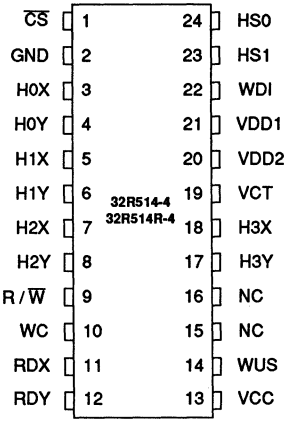
FIGURE 2: TYPICAL APPLICATION DIAGRAM

SSI 32R514/514R
2, 4, 6-Channel
Read/Write Device

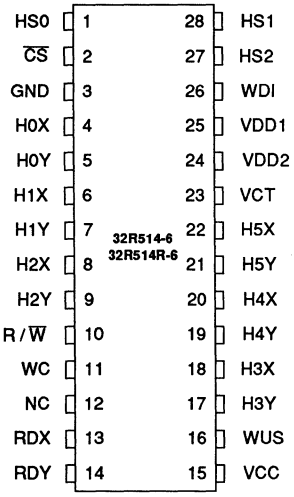
PACKAGE PIN DESIGNATIONS (TOP VIEW)



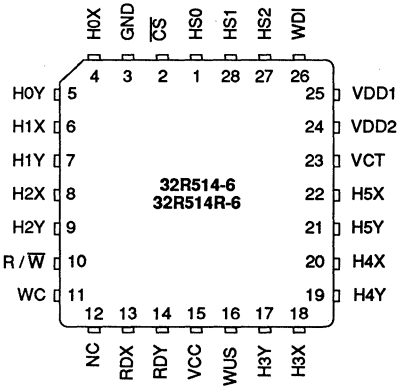
18-LEAD SOL



24-LEAD SOL



28-LEAD SOL



28-LEAD PLCC

THERMAL CHARACTERISTICS

PACKAGE		θja
18-Lead	SOL	100°C/W
24-Lead	SOL	80°C/W
28-Lead	SOL	70°C/W
28-Lead	PLCC	65°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R514 Read/Write IC		
2-Channel SOL	SSI 32R514-2CL	32R514-2CL
4-Channel SOL	SSI 32R514-4CL	32R514-4CL
6-Channel SOL	SSI 32R514-6CL	32R514-6CL
6-Channel PLCC	SSI 32R514-6CH	32R514-6CH
SSI 32R514R Read/Write IC-with internal damping resistors		
2-Channel SOL	SSI 32R514R-2CL	32R514R-2CL
4-Channel SOL	SSI 32R514R-4CL	32R514R-4CL
6-Channel SOL	SSI 32R514R-6CL	32R514R-6CL
6-Channel PLCC	SSI 32R514R-6CH	32R514R-6CH

silicon systems™
Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, TWX 910-595-2809

NOTES:

SSI 32R515/515R
9, 10-Channel Ferrite Read/Write Device

August 1988

1

DESCRIPTION

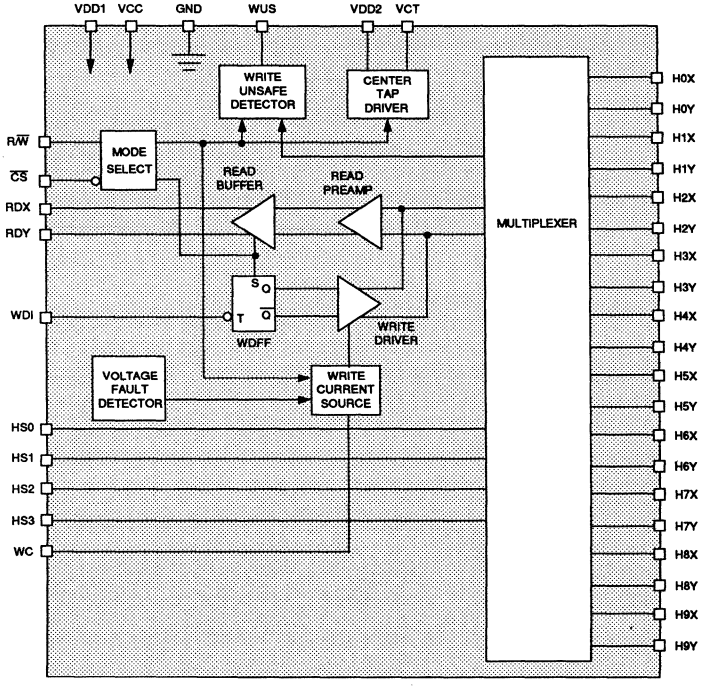
The SSI 32R515 is a bipolar monolithic integrated circuit designed for use with a center-tapped ferrite recording head. It provides a low noise read path, write current control, and data protection ciruitry for as many as 10 channels. The SSI 32R515 requires +5V and +12V power supplies and is available in a variety of packages.

The SSI 32R515R performs the same function as the SSI 32R515 with the addition of internal damping resistors. The SSI 32R515M and SSI 32R515RM are functionally equivalent to the SSI 32R515 and SSI 32R515R however, they have the mirror image pin arrangement to simplify layout when using multiple devices.

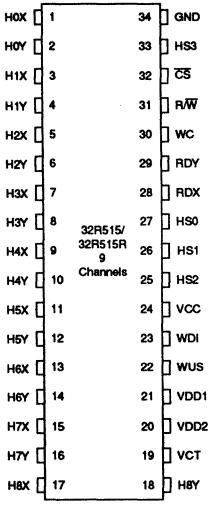
FEATURES

- **High Performance**
  - **Read Mode Gain = 100V/V**
  - **Input Noise = 1.5 nV/$\sqrt{Hz}$ max.**
  - **Input Capacitance = 20 pF**
  - **Write Current Range = 10 mA to 50 mA**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Designed for center-tapped ferrite heads**
- **Programmable write current source**
- **Includes write unsafe detection**
- **TTL compatible control signals**
- **+5V, +12V power supplies**
- **Mirror image package option**

BLOCK DIAGRAM



PIN DIAGRAM



34-LEAD SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32R515 gives the user the ability to address up to 10 center-tapped ferrite heads and provide write drive or read amplification. Head selection and mode control is accomplished using the HSn, $\overline{CS}$ and R/$\overline{W}$ inputs as shown in tables 1 & 2. Internal pullups are provided for the $\overline{CS}$ & R/$\overline{W}$ inputs to force the device into a non-writing condition if either control line is opened accidentally.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TABLE 2: Head Select

HS3	HS2	HS1	HS0	HEAD
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

0 = Low level 1 = High level

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SSI 32R515 as a current switch and activates the Write Unsafe (WUS) detector circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding read mode selection initializes the Write Data Flip-Flop, WDFF, to pass write current through the "X" side of the head. The zero-peak write current magnitude is programmed by an external resistor Rwc from pin WC to GND and is given by:

Iw = K/Rwc, where K = Write Current Constant

The Write Unsafe detection circuitry monitors voltage transitions at the selected head connections and flags any of the following conditions as a high level on the Write Unsafe open collector output:

- Head open
- WDI frequency too low
- Device not selected
- Head center tap open
- Device in read mode
- No write current

Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

To further assure data security a voltage fault detection circuit prevents application of write current during power loss or power sequencing.

To enhance write to read recovery time the change in RDX, RDY common mode voltage is minimized by biasing these outputs to a level within the read mode range when in write mode.

Power dissipation in write mode may be reduced by placing a resistor (RCT) between VDD1 & VDD2. The optimum resistor value is 96Ω x 50/Iw (Iw in mA). At low write currents (<15 mA) read mode dissipation is higher than write mode and RCT, though recommended, may not be considered necessary. In this case VDD2 is connected directly to VDD1.

READ MODE

Taking $\overline{CS}$ low and R/$\overline{W}$ high selects read mode which configures the SSI 32R515 as a low noise differential amplifier for the selected head. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The internal write current source is gated off in read mode eliminating the need for any external gating.

Read mode selection also initializes the Write Data Flip-Flop (WDFF) to pass write current through the "X" side of the head at a subsequent write mode selection.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX, RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0-HS3	I	Head Select
$\overline{CS}$	I	Chip Select: a low level enables device
R/$\overline{W}$	I	Read/Write: a high level selects read mode
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition
WDI	I	Write Data In: negative transition toggles direction of head current
H0X-H9X H0Y-H9Y	I/O	X,Y head connections
RDX, RDY	O*	X, Y Read Data: differential read signal out
WC	*	Write Current: used to set the magnitude of the write current
VCT	-	Voltage Center Tap: voltage source for head center tap
VCC	-	+5V
VDD1	-	+12V
VDD2	-	Positive power supply for the center tap voltage source
GND	-	Ground
* When more than one Read/Write device is used, these signals can be wire OR'ed.		

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (All voltages referenced to GND. Currents into device are positive.)

PARAMETER		VALUE	UNITS
DC Supply Voltage	VDD1	-0.3 to +14	VDC
DC Supply Voltage	VDD2	-0.3 to +14	VDC
DC Supply Voltage	VCC	-0.3 to +6	VDC
Digital Input Voltage Range	VIN	-0.3 to VCC + 0.3	VDC
Head Port Voltage Range	VH	-0.3 to VDD1 + 0.3	VDC
WUS Pin Voltage Range	Vwus	-0.3 to +14	VDC
Write Current Zero Peak	Iw	60	mA
Output Current	RDX, RD Io	-10	mA
Output Current	IVCT	-60	mA
Output Current	Iwus	+12	mA
Storage Temperature Range	Tstg	-65 to 150	°C
Package Temperature PLCC, SO (20 sec Reflow)		215	°C.

RECOMMENDED OPERATION CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DC Supply Voltage	VDD1		10.8	12.0	13.2	VDC
DC Supply Voltage	VCC		4.5	5.0	5.5	VDC
Head Inductance	Lh		3		15	µH
Damping Resistor	RD	32R515 only	500		2000	Ω
RCT Resistor	RCT*	Iw = 50 mA	91	96	101	Ω
Write Current	IW		10		80	mA
Junction Temperature Range	Tj		+25		+135	°C
*For Iw = 50 mA. At other Iw levels refer to Applications Information that follows this specification.						

DC CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Supply Current	Read/Idle Mode			35	mA
	Write Mode			30	mA
VDD Supply Current	Idle Mode			20	mA
(sum of VDD1 and VDD2)	Read Mode			35	mA
	Write Mode			20 + Iw	mA
Power Dissipation (Tj = +125°C)	Idle Mode			400	mW
	Read Mode			600	mW
	Write Mode, Iw = 50 mA, RCT = 0Ω			900	mW
	Write Mode, IW = 50 mA RCT = 96Ω			660	mW

DC CHARACTERISTICS (Continued)

DIGITAL I/O

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VIL	Input Low Voltage				0.8	VDC
VIH	Input High Voltage		2.0		VCC + 0.3	VDC
IIL	Input Low Current	VIL = 0.8V	-0.4			mA
IIH	Input High Current	VIH = 2.0V			100	µA
VOL	WUS Output Low Voltage	IOL = 8 mA			0.5	VDC
IOH	WUS Output High Current	VOH = 5.0V			100	µA

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Center Tap Voltage VCT	Write Mode		6.0		VDC
Head Current (per side)	Write Mode, 0 ≤ VCC ≤ 3.7V, 0 ≤ VDD1 ≤ 8.7V	-200		200	µA
Write Current Range		10		50	mA
Write Current Constant "K"		2.375		2.625	
Iwc to Head Current Gain			0.99		mA/mA
Unselected Head Leakage Current				100	µA
RDX, RDY Output Offset Voltage	Write/Idle Mode	-20		+20	mV
RDX, RDY Common Mode Output Voltage	Write/Idle Mode		5.3		VDC
RDX, RDY Leakage	RDX, RDY = 6V Write/Idle Mode	-100		100	µA

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Center Tap Voltage	Read Mode	3.0	4.0	5.0	VDC
Head Current (per side)	Read or Idle Mode 0 ≤ VCC ≤ 5.5V 0 ≤ VDD1 ≤ 13.2V	-200		200	µA
Input Bias Current (differential)				100	µA
Input Offset Voltage	Read Mode	-4		+4	mV
Common Mode Output Voltage	Read Mode	4.5		6.5	VDC

DYNAMIC CHARACTERISTICS AND TIMING

Unless otherwise specified, recommended operating conditions apply and Iw = 35 mA, Lh = 10 µH, Rd = 750Ω 32R515 only, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 20 pF.)

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Head Voltage Swing		7.0			V(pk)
Unselected Head Transient Current				.5	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	32R515	10K			Ω
	32R515R	458	610	763	Ω
WDI Transition Frequency	WUS = low	250			KHz

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain	Vin = 1 mVpp @ 300 kHz, RL(RDX), RL(RDY) = 1 KΩ	85		115	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10%. Vin = Vi + 0.5 mVpp @ 300 kHz	-3		+3	mV
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	30			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			1.5	$nV/\sqrt{Hz}$
Differential Input Capacitance	f = 5 MHz			20	pF
Differential Input Resistance	32R515, f = 5 MHz	2K			Ω
Differential Input Resistance	32R515R, f = 5 MHz	373		735	Ω
Common Mode Rejection Ratio	Vcm = VCT + 100 mVpp @ 5 MHz	50			dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VDD1, VDD2 or VCC	45			dB
Channel Separation	Unselected Channels: Vin=100 mVpp @ 5 MHz; Selected Channel: Vin = 0 mVpp	45			dB
Single Ended Output Resistance	f = 5 MHz			30	Ω
Output Current	AC Coupled Load, RDX to RDY	±2.1			mA

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
R/$\overline{W}$ To Write	Delay to 90% of Write Current			1.0	µs
R/$\overline{W}$ to Read	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope or to 90% decay of Write Current			1.0	µs
$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100 mV, 10 MHz Read Signal Envelope			1.0	µs
$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current			1.0	µs
HS0 - HS3 to any head	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope			600	ns
WUS-Safe to Unsafe - TD1	Iw = 35 mA	1.6		8.0	µs
WUS-Unsafe to Safe - TD2	Iw = 35 mA			1.0	µs
Head Current (Lh = 0 µH, Rh = 0Ω)					
Prop. Delay - TD3	From 50% Points			25	ns
Asymmetry	WDI has 50% Duty Cycle and 1ns Rise/Fall Time			2	ns
Rise/Fall Time	10% - 90% Points			20	ns

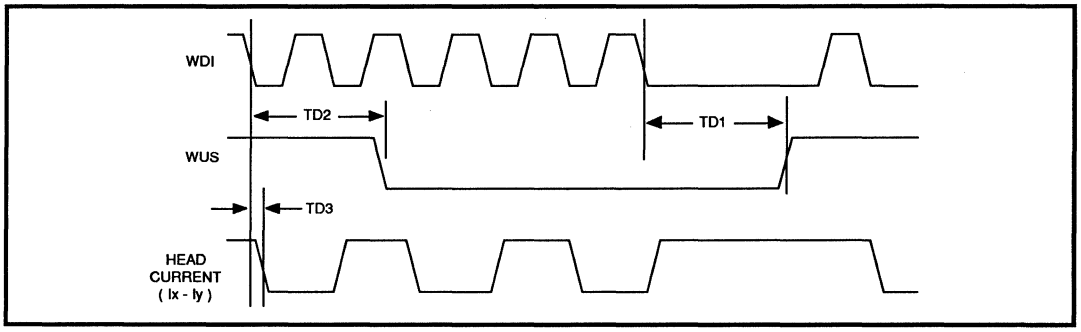
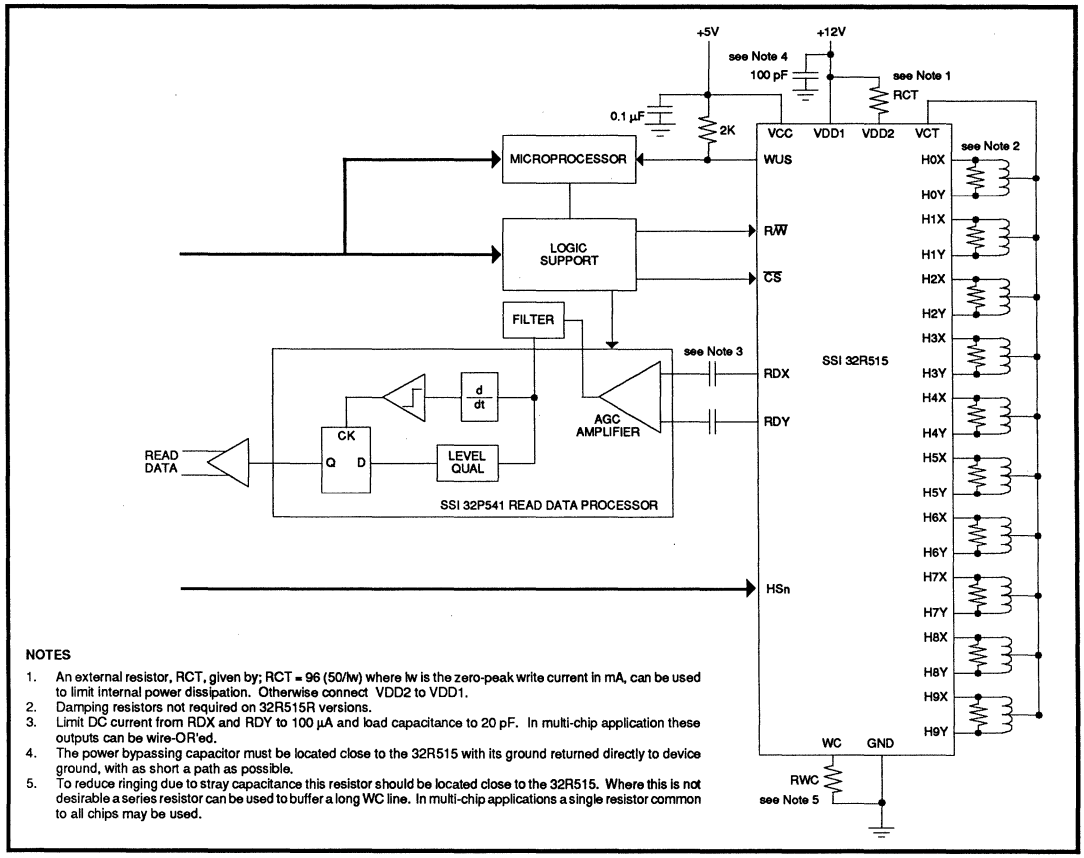


FIGURE 1: Write Mode Timing Diagram



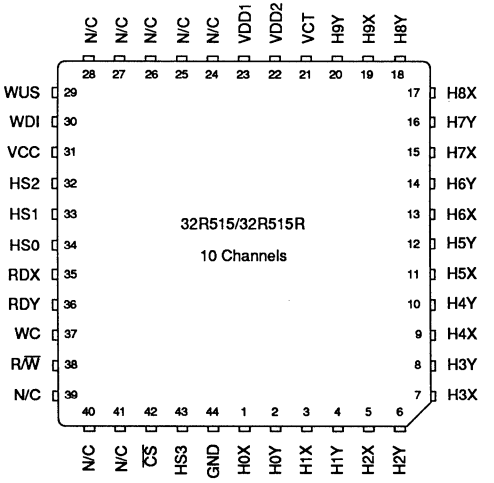
NOTES

1. An external resistor, RCT, given by; RCT = 96 (50/Iw) where Iw is the zero-peak write current in mA, can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.
2. Damping resistors not required on 32R515R versions.
3. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire-OR'ed.
4. The power bypassing capacitor must be located close to the 32R515 with its ground returned directly to device ground, with as short a path as possible.
5. To reduce ringing due to stray capacitance this resistor should be located close to the 32R515. Where this is not desirable a series resistor can be used to buffer a long WC line. In multi-chip applications a single resistor common to all chips may be used.

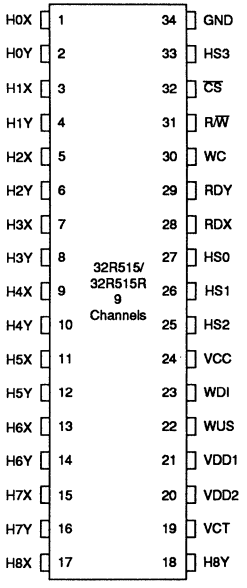
FIGURE 2: Applications Information

PACKAGE PIN DESIGNATIONS

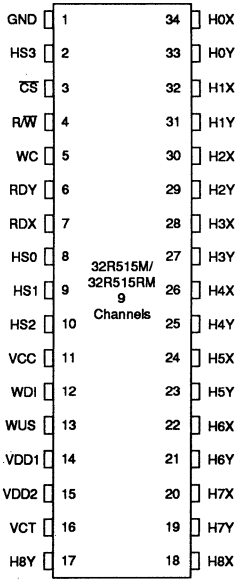
(TOP VIEW)



44-Lead PLCC



34-Lead SOL



34-Lead SOL
Mirror Image

THERMAL CHARACTERISTICS: Ø ja

34-Lead	SOL	50°C/W
44-Lead	PLCC	60°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R515		
9-Channel SOL	SSI 32R515-9CL	32R515-9CL
10-Channel PLCC	SSI 32R515-10CH	32R515-10CH
SSI 32R515R		
9-Channel SOL	SSI 32R515R-9CL	32R515R-9CL
10-Channel PLCC	SSI 32R515R-10CH	32R515R-10CH
SSI 32R515M		
9-Channel SOL	SSI 32R515M-9CL	32R515M-9CL
SSI 32R515RM		
9-Channel SOL	SSI 32R515RM-9CL	32R515RM-9CL

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INNOVATORS IN INTEGRATION

SSI 32R520/520R
4-Channel Thin Film Read/Write Device

August, 1988

1

DESCRIPTION

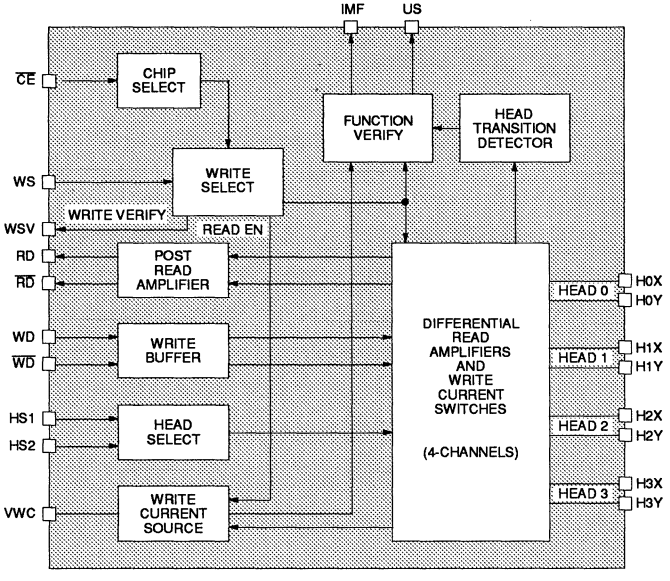
The SSI 32R520 is an integrated read/write circuit designed for use with non-center tapped thin film heads in disk drive systems. Each chip controls four heads and has three modes of operation: read, write, and idle. The circuit contains four channels of read amplifiers and write drivers and also has an internal write current source.

A current monitor (IMF) output is provided that allows a multi-chip enable fault to be detected. An enabled chip's output will produce one unit of current. An open collector output, write select verify (WSV), will go low if the write current source transistor is forward biased. The circuit operates on +5 volt, and -5 volt power and is available in a 24-pin flatpack. The SSI 32R520R differs from the SSI 32R520 by having internal 200Ω damping resistors.

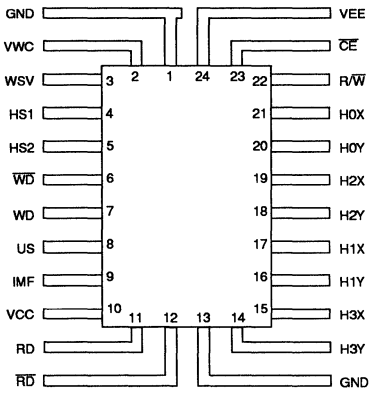
FEATURES

- High performance
  - Read mode gain = 120V/V
  - Input noise = 0.9nV/$\sqrt{Hz}$
  - Input capacitance = 65 pF
  - Write current range = 30 mA to 75 mA
  - Head voltage swing = 3.8 Vpp
  - Write current risetime = 13 nsec
- Write unsafe detection
- TTL - compatible logic levels
- Operates on standard +5 volt and -5 volt power supplies

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32R520/520R
4-Channel Thin Film
Read/Write Device

CIRCUIT DESCRIPTION

WRITE MODE

In the write mode (R/$\overline{W}$ and CE low) the circuit functions as a differential current switch. The Head Select inputs (HS1 and HS2) determine the selected head. The Write Data Inputs (WD, $\overline{WD}$) determine the polarity of the head current. The write current magnitude is adjustable by an external 1% resistor, Rwc, from VWC to VEE, where:

$$I_w = \frac{V_{wc}}{R_{wc}(1 + \frac{Rh}{Rd})}$$

Where: Vwc = Write Current Pin Voltage = 1.65 ± 5%

Rh = Head Plus External Wire Resistance

Rd = Damping Resistance

READ MODE

In the Read Mode, (R/$\overline{W}$ high and CD low), the circuit functions as a differential amplifier. The amplifier input terminals are determined by the Head Select inputs.

HEAD SELECT TABLE

HEAD SELECTED	HS2	HS1
0	0	0
1	0	1
2	1	0
3	1	1

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 4.75 ≤ Vcc ≤ 5.25, -5.5 ≤ VEE ≤ -4.95V, 25° ≤ T (junction) ≤ 125 °C.

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
Positive Supply Voltage, Vcc	6	V
Negative Supply Voltage, VEE	-6	V
Operating Junction Temperature	25 to 125	°C
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering, 10 sec)	260	°C
Input Voltages		
Head Select (HS)	-0.4 to Vcc +0.3	V
Chip Enable ($\overline{CE}$)	-0.4 to Vcc +0.3	V
Read Select (R/$\overline{W}$)	-0.4 or -2 mA to Vcc +0.3	V
Write Data (WD, $\overline{WD}$)	VEE to + 0.3	V
Head Inputs (Read Mode)	-0.6 to + 0.4	V

ABSOLUTE MAXIMUM RATINGS (Continued)

PARAMETER	RATING	UNIT
Outputs		
Read Data (RD, $\overline{RD}$)	0.5 to Vcc +0.3	V
Write Unsafe (WUS)	-0.4 to Vcc +0.3 and 20 mA	V
Write Select Verify (WSV)	-0.4V to Vcc +0.3V and 20	mA
Current Monitor (IMF)	-0.4 to Vcc +0.3	V
Current Reference (VWC)	VEE to Vcc +0.3 and 8 mA	V
Head Outputs (Write Mode)	Iw max = 150	mA

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Power Dissipation	All modes, 25 ≤ Tj ≤ 100			612+6.7Iw	mW
	100° ≤ Tj ≤ 125 °C			563+6.7Iw	mW
Positive Supply Current (ICC)	Idle Mode			10+Iw/19	mA
Positive Supply Current (ICC)	Read Mode			40+Iw/19	mA
Positive Supply Current (ICC)	Write Mode			38+Iw/19	mA
Negative Supply Current (IEE)	Idle Mode	-12–Iw/19			mA
Negative Supply Current (IEE)	Read Mode	-66–Iw/19			mA
Negative Supply Current (IEE)	Write Mode	-75–1.16Iw			mA

LOGIC SIGNALS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Chip Enable Low Voltage (VLCE)	Read or Write Mode			0.8	V
Chip Enable High Voltage (VHCE)	Idle Mode	2.0			V
Chip Enable Low Current (ILCE)	VLCE = 0V	-1.60			mA
Chip Enable High Current (IHCE)	VHCE = 2.0V			-0.3	mA
Read Select High Voltage (VHR/W)	Read or Idle Mode	2.0			V
Read Select Low Voltage (VLR/W)	Write or Idle Mode			0.8	V
Read Select High Current (IHR/W)	VHR/W = 2.0V			0.015	mA
Read Select Low Current (ILR/W)	VLR/W = 0V	-0.15			mA
Head Select High Voltage (VHHS)		2.0			V
Head Select Low Voltage (VLHS)				0.8	V
Head Select High Current (IHHS)	VHHS = VCC			0.25	mA

LOGIC SIGNALS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Head Select low Current (ILHS)	VLHS = 0V	-0.1		0.25	mA
WUS, WSV Low Level Voltage	ILUS = 8 mA (denotes safe condition)			0.5	V
WUS, WSV High Level Current	VHUS = 5.0V (denotes unsafe condition)			100	µA
IMF ON Current		2.20		3.70	mA
IMF OFF Current				0.02	mA
IMF Voltage Range		0		VCC+0.3	V

READ MODE

Tests performed with 100Ω load resistors from RD and $\overline{RD}$ through series isolation diodes to VCC.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Voltage Gain	Vin = 1 mVpp, f = 300 KHz; 25 °C≤ Tj ≤ 125 °C	75		170	V/V
	Tj = 70 °C	85		150	V/V
Voltage Bandwidth (-3 dB)	Zs < 5Ω, Vin = 1 mVpp f midband = 300 KHz	45			MHz
Input Noise Voltage	Zs = 0Ω, Vin = 0V, Power Bandwidth = 15 MHz			0.9	$nV/\sqrt{Hz}$
Differential Input Capacitance	Vin = 1 mVpp, f = 5 MHz			65	pF
Differential Input Resistance	Vin = 1 mVpp, f = 5 MHz 32R520	1K			Ω
	32R520R	130		270	Ω
Input Bias Current (per side)	Vin = 0V			0.17	mA
Dynamic Range	DC input voltage where AC gain falls to 90% of the gain with .5 mVpp input signal	-3.0		3.0	mV
CMRR	Vin = 100 mVpp, 0V DC 1 MHz ≤ f ≤ 10 MHz	54			dB
	10 MHz ≤ f ≤ 20 MHz	48			dB
Power Supply Rejection Ratio	VCC or VEE = 100 mVpp 1 MHz ≤ f ≤ 10 MHz	54			dB
	10 MHz ≤ f ≤ 20 MHz	40			dB
Channel Separation	The three unselected channels are driven with Vin = 100 mVpp 1 MHz ≤ f ≤ 10 MHz	43			dB
	10 MHz ≤ f ≤ 20 MHz	37			dB

READ MODE (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Output Offset Voltage		-360		360	mV
Output Leakage Current	Idle Mode			0.01	mA
Output Common Mode Voltage	(Without series isolation diodes)	VCC-1.1		VCC-0.13	V
Single Ended Output Resistance		10			KΩ
Single Ended Output Capacitance				10	pF

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Current Range (Iw)		30		75	mA
Current Tolerance	Current set to nomial value by Rx, Rh = 15Ω ± 10%, Tj = 50 °C, Rd = 200Ω	-8		+8	%
(Iw) (Rh) Product		0.24		1.30	V
Differential Head Voltage Swing	Iw = 40 mA, Lh = 0.3 µH, Rh = 15Ω	3.8			Vpp
Unselected Head Transient Current	Iw = 40 mA, Lh = 0.3 µH, Rh = 15Ω Non-adjacent heads tested to minimize external coupling effects			2	mAp
Head Differential Load Resistance, Rd	32R520	1K			Ω
	32R520R 25 °C ≤ Tj ≤ 125 °C	130		270	Ω
	60 °C ≤ Tj ≤ 120 °C	140		260	Ω
	Tj = 70 °C	150		250	Ω
Head Differential Load Capacitance				30	pF
Differential Data Voltage, (WD – $\overline{WD}$)		0.20			V
Data Input Voltage Range		-1.87		+0.1	V
Data Input Current (per side)	Chip Enabled			150	µA
Data Input Capacitance	Per side to GND			10	pF

SWITCHING CHARACTERISTICS

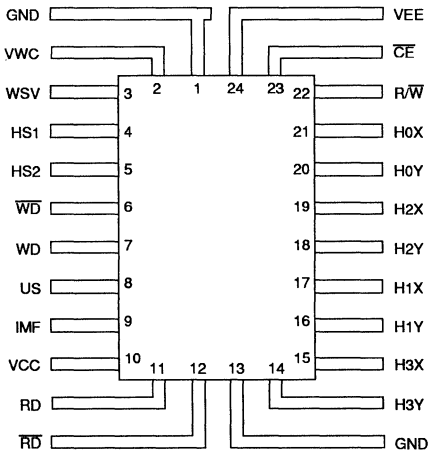
PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Idle to Read/Write Transition Time				1.0	µs
Read/Write to Idle Transition Time				1.0	µs
Read to Write Transition Time	VLCE = 0.8V, Delay to 90% of Iw			0.6	µs
Write to Read Transition Time	VLCE = 0.8V, Delay to 90% of 20 MHz Read Signal envelope, Iw decay to 10%			0.6	µs
Head Select Switching Delay	Read or Write Mode			0.40	µs
Shorted Head Current Transition Time	Iw = 40 mA, Lh < 0.05 µH, Rh = 0			13	ns
Shorted Head Current Switching Delay Time	Iw = 40 mA, Lh < 0.05 µH, Rh = 0, measured from 50% of input to 50% of current change			18	ns
Head Current Switching Time Symmetry	Iw = 40 mA, Lh = 0.2 µH, Rh = 10Ω, WD & $\overline{WD}$ transitions 2 ns, switching time symmetry 0.2 ns			1.0	ns
WSV Transition Time	Delay from 50% of write select swing to 90% of final WSV voltage, Load = 2 KΩ // 20 pF			1.0	µs
Unsafe to Safe Delay After Write Data Begins (WUS)	f(data) = 10 MHz			1.0	µs
Safe to Unsafe Delay, (WUS)	Non-switching write data, no write current	0.6		3.6	µs
Safe to Unsafe Delay, (WUS)	Head open or head select input open			0.6	µs
IMF Switching Time	Delay from 50% of CE to 90% of final IMF current			1.0	µs

PACKAGE PIN DESIGNATIONS

(TOP VIEW)

THERMAL CHARACTERISTICS: Ø ja

24-Lead	Flatpack	105°C/W



24-Pin Flatpack

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32R520 Read/Write IC		
24-Pin Flatpack	SSI 32R520-F	SSI 32R520-F
SSI 32R520R Read/Write IC with Damping Resistors		
24-Pin Flatpack	SSI 32R520R-F	SSI 32R520R-F

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Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

NOTES:

SSI 32R521/521R
Thin Film-6-Channel Read/Write Device

August, 1988

1

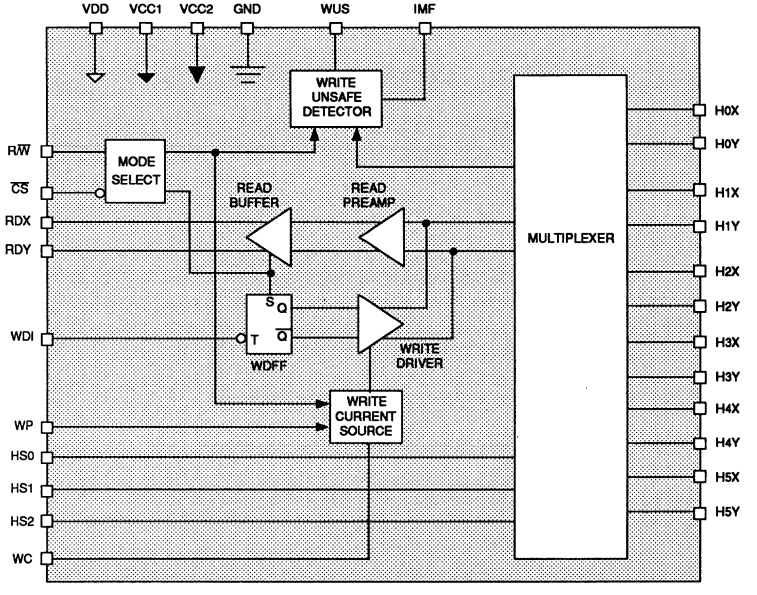
DESCRIPTION

The SSI 32R521 is a bipolar monolithic integrated circuit designed for use with non-center tapped thin film recording heads. It provides a low noise read path, write current control, and data protection circuitry for up to six channels. The SSI 32R521 requires +5V and +12V power supplies and is available in a variety of packages. The SSI 32R521R differs from the SSI 32R521 by having 200Ω internal damping resistors.

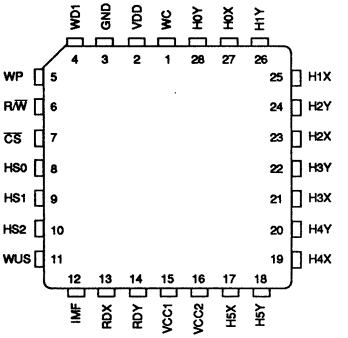
FEATURES

- **Designed for thin film heads**
- **+5V, +12V power supplies**
- **Ideal for multi-platter Winchester applications**
- **Programmable write current source**
- **Easily multiplexed for larger systems**
- **Includes write unsafe detection**

BLOCK DIAGRAM



PIN DIAGRAM



28-LEAD PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32R521 functions as a write driver or as a read amplifier for the selected head. Head selection and mode control are described in Tables 1& 2. The inputs R/$\overline{W}$, $\overline{CS}$ and WP have internal pull-up resistors to prevent an accidental write condition.

WRITE MODE

The Write mode configures the SSI 32R521 as a current switch and activates the Write Unsafe Detector. Head current is toggled between the X- and Y-directions of the recording head on the falling edges of WDI, Write Data Input. The magnitude of the write current, given by:

$$Iw = \frac{Vwc}{Rwc}$$

is controlled by an external resistor, Rwc, connected from pin WC to GND.

$$\text{Head Current Ix, y} = \frac{Iw}{1 + Rh/Rd}$$

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in Read mode
- Chip disabled
- No write current

After fault condition is removed, two negative transitions on WDI are required to clear WUS. The Current monitor output (IMF) sinks one unit of current when the device is selected. This allows a multichip enable fault to be detected.

NOTE: If it is desirable to initialize the Write Data flip-flop to pass current in the Y-direction of the head when entering Write Mode, the WDI input must go low in Read mode for 20 ns minimum.

READ MODE

In the Read mode, the SSI 32R521 is configured as a low noise differential amplifier, the write current source and the write unsafe detector are deactivated, and the write data flip-flop can be set. The RDX and RDY outputs are driven by emitter followers. They should be AC coupled to load. Note that the internal write current source is deactivated for both the Read and chip deselected modes.

IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

TABLE 1: MODE SELECT

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: HEAD SELECT

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	none
1	1	1	none

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HSO - HS2	I	Head Select: selects one of six heads
$\overline{CS}$	I	Chip Select: a high inhibits chip
R/$\overline{W}$	I	Read/Write: a high selects Read mode
WP	I	Write Protect: a low enables the write current source
WUS	O*	Write Unsafe: a high indicates an unsafe writing condition
IMF	O*	Current Monitor Function: allows multichip enable fault detection
WDI	I	Write Data In: changes the direction of the current in the recording head
HOX - H5X HOY - H5Y	I/O	X, Y Head Connections: Current in the X-direction flows into the X-port
RDX, RDY	O*	X, Y Read Data: differential read data output
WC	*	Write Current: used to set the magnitude of the write current
VCC1	-	+5V Logic Circuit Supply
VCC2	-	+5V Write Current Supply
VDD	-	+12V
GND	-	Ground

*When more than one device is used, these signals can be wire OR'ed.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	VALUE	UNITS
DC Supply Voltage		VDD	-0.3 to +14	VDC
		VCC	-0.3 to +7	VDC
Write Current		IW	100	mA
Digital Input Voltage		Vin	-0.3 to VCC +0.3	VDC
Head Port Voltage		VH	-0.3 to VDD +0.3	VDC
Output Current:	RDX, RDY	Io	-10	mA
	WUS	Iwus	+12	mA
Storage Temperature		Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	VDD	12 ± 5%	VDC
	VCC1	5 ± 5%	VDC
	VCC2	5 ± 5%	VDC
Operating Temperature	Tj	+25 to +135	°C

DC CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
VDD Supply Current	Read Mode		34	mA
	Write Mode		38	mA
	Idle Mode		9	mA
VCC Supply Current	Idle Mode		49	mA
	Read Mode		62	mA
	Write Mode		49 + IW	mA
Power Dissipation (Tj = +135°C)	Idle Mode		400	mW
	Read Mode		800	mW
	Write Mode, IW = 70 mA		990	mW

DC CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
Digital Inputs					
Input Low Voltage (VIL)			-0.3	0.8	VDC
Input High Voltage (VIH)			2.0	VCC+0.3	VDC
Input Low Current		VIL = 0.8V	-0.4		mA
Input High Current		VIH = 2.0V		100	µA
RDX, RDY Common Mode Output Voltage			3	5	VDC
WUS Output	VOL	Iol = 8 mA		0.5	VDC
IMF Output		$\overline{CS}$ = 0	0.73	1.23	mA
		$\overline{CS}$ = 1		0.02	mA

WRITE CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply, and IW = 40 mA, Lh = 200 nH, Rh = 16Ω, f(Data) = 5 MHz, CL(RDX, RDY) < 20 pF, RL(RDX,RDY) = 1 KΩ.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Write Current Voltage Vwc			1.65±5%		V
Differential Head Voltage Swing		3.4			V(pk)
Unselected Head Current				2	mA(pk)
Differential Output Capacitance				30	pF
Differential Output Resistance	32R521R	160	200	240	Ω
	32R521	2K			Ω
WDI Transition Frequency	WUS=low	1.7			MHz
Write Current Range		20		70	mA

READ CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply.

PARAMETER		CONDITIONS	MIN	MAX	UNITS
Differential Voltage Gain		Vin = 1 mVpp @ 300 KHz RL(RDX), RL(RDY) = 1 KΩ	75	125	V/V
Voltage BW	-1dB	|Zs| < 5Ω, Vin = 1 mVpp @ 300 KHz	25		MHz
	-3dB		45		MHz

READ CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			0.9	nV/√Hz
Differential Input Capacitance	f = 5 MHz			65	pF
Differential Input Resistance	521R, f = 5 MHz		200		Ω
	521, f = 5 MHz	600			Ω
Input Bias Current				170	mA
Dynamic Range	DC input voltage where gain falls to 90% of its 0 VDC value Vin=VDC+0.5mVpp, f=5MHz	-3		3	mV
Common Mode Rejection Ratio	Vin=0VDC+100mVpp@5MHz	54			dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VDD	54	90		dB
	100 mVpp @ 5 MHz on VCC		49		
Channel Separation	Unselected channels driven with 100 mVpp @ 5 MHz Vin = 0 mVpp	45			dB
Output Offset Voltage		-360		360	mV
Single Ended Output Resistance	f = 5 MHz			30	Ω
Output Current	AC Coupled Load, RDX to RDY	3.2			mA

SWITCHING CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply, and IW = 40 mA, Lh = 200 nH, Rh = 16Ω, f(Data) = 5 MHz.

PARAMETER		CONDITIONS	MIN	MAX	UNITS
R/$\overline{W}$	R/$\overline{W}$ to Write	To 90% of write current		0.6	µs
	R/$\overline{W}$ to Read	To 90% of 100 mV, 10 MHz Read signal envelope		0.6	µs
$\overline{CS}$	$\overline{CS}$ to Select	To 90% of write current		1	µs
	$\overline{CS}$ to Unselect	To 90% of 100 mV, 10 MHz Read signal envelope		1	µs
HS0, 1, 2 to any Head		To 90% of 100 mV, 10 MHz Read signal envelope		0.4	µs
WUS	Safe to Unsafe TD1		0.6	3.6	µs
	Unsafe to Safe TD2			1	µs
IMF	Transition Time	Delay from 50% point of CS to 90%of IMF current		0.6	µs
Head Current		Lh = 0, Rh = 0			
	WDI to (Ix-Iy) TD3	From 50% points		32	ns
	Asymmetry	WDI has 50% duty cycle and 1ns rise/fall time		1.0	ns
	Rise/Fall Time	10% - 90% points		13	ns

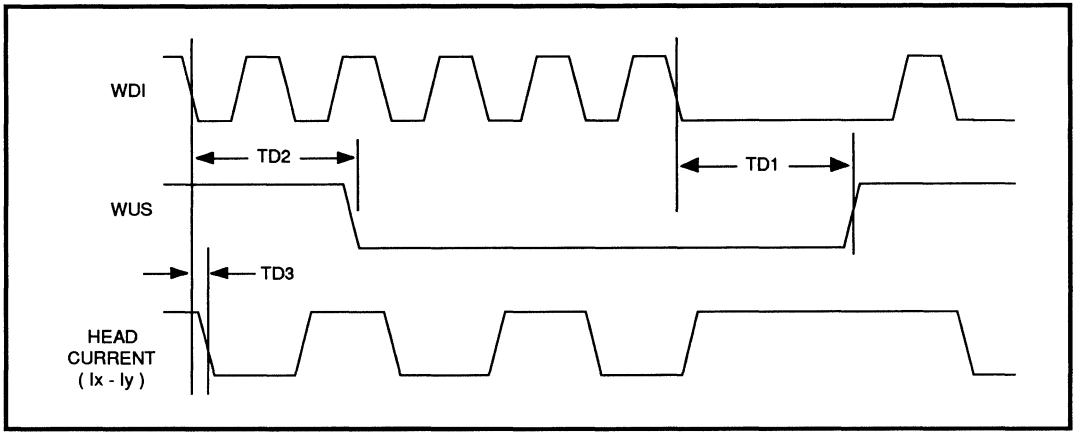


FIGURE 1: Write Mode Timing Diagram

APPLICATIONS INFORMATION

Read mode input port parameter limits, as given in the specifications, are over extremes of temperature, voltage and process. The tabulation below shows parameter correlation as a function of base sheet resistance, a processing parameter. Use of these limits, for worst case analysis, will be more representative of actual performance.

EXAMPLE 1: Base Sheet Resistance = Maximum

PARAMETER		Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Maximum)		0.69	0.9	nV/√Hz
Differential Input Resistance (Minimum)	521R	146	150	Ω
	521	1025	1240	Ω
Differential Input Capacitance (Maximum)		43	47	pF

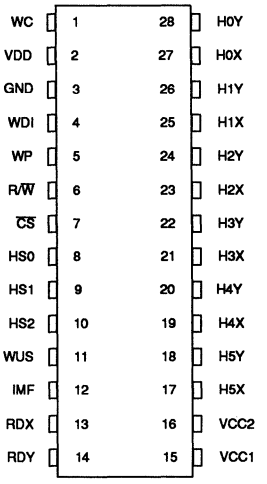
EXAMPLE 2: Base Sheet Resistance = Minimum

PARAMETER		Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Maximum)		0.58	0.75	nV/√Hz
Differential Input Resistance (Minimum)	521R	133	140	Ω
	521	600	760	Ω
Differential Input Capacitance (Maximum)		51	56	pF

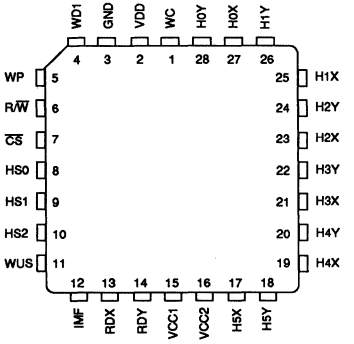
SSI 32R521/521R
Thin Film-6-Channel
Read/Write Device

PACKAGE PIN DESIGNATIONS

(Top View)



28-Lead SOL, Flatpack



28-Lead PLCC

THERMAL CHARACTERISTICS: Øja

28-Lead	SOL	75°C/W
	PLCC	65°C/W
	Flatpack	100°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R521 - Read/Write IC		
6 - Channel SOL	SSI 32R521-6L	32R521-6L
6 - Channel PLCC	SSI 32R521-6CH	32R521-6CH
6 - Channel Flatpack	SSI 32R521-6F	32R521-6F
SSI 32R521R - with Internal Damping Resistors		
6 - Channel SOL	SSI 32R521R-6L	32R521R-6L
6 - Channel PLCC	SSI 32R521R-6CH	32R521R-6CH
6 - Channel Flatpack	SSI 32R521R-6F	32R521R-6F

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SSI 32R522/522R
4, 6-Channel Thin Film Read/Write Device

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INNOVATORS IN INTEGRATION

1

August, 1988

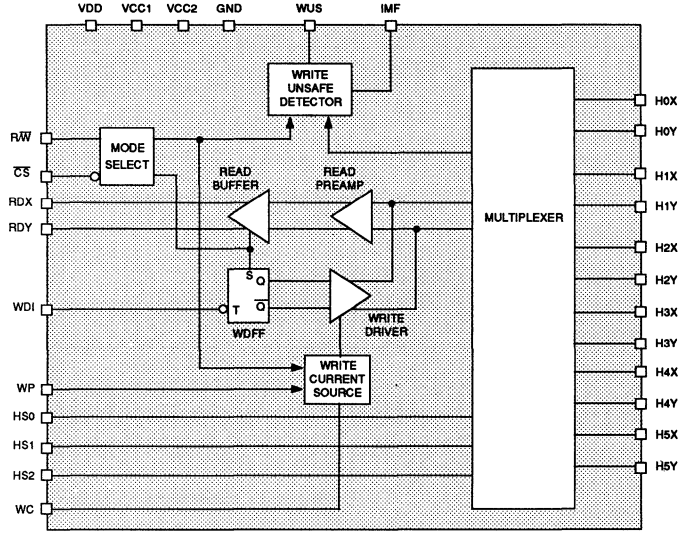
DESCRIPTION

The SSI 32R522/522R Read/Write devices are bipolar monolithic integrated circuits designed for use with two terminal thin film recording heads. They provide a low noise read amplifier, write current control and data protection circuitry for as many as six channels. They require +5V and +12V power supplies and are available in a variety of package and channel configurations. The 32R522R option provides internal 1000Ω damping resistors.

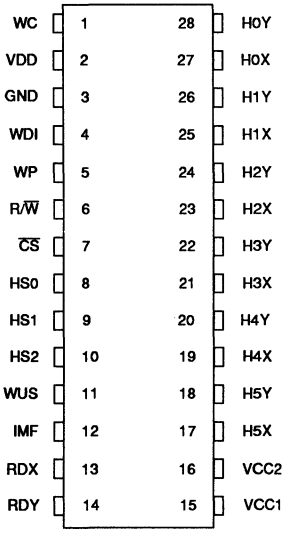
FEATURES

- **High performance:**
  - **Read mode gain = 100 V/V**
  - **Input noise = 1.0 nV/√Hz max.**
  - **Input capacitance = 32 pF max.**
  - **Write current range = 6 mA to 35 mA**
- **Compatible with two & three terminal thin film heads**
- **Programmable write current source**
- **Write unsafe detection**
- **TTL compatible control signals**
- **+5, +12V power supplies**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32R522 addresses up to six two-terminal thin film heads providing write current drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$, R/$\overline{W}$ and WP will force the device into a non-writing condition if either control line is opened accidentally.

WRITE MODE

The write mode configures the SSI 32R522 as a current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high to low transition on pin WDI, Write Data Input.

The magnitude of the write current (0-pk) given by:

$$Iw = \frac{Vwc}{RWC}$$

where Vwc (WC pin voltage) = 1.7V ± 5%, is programmed by an external resistor RWC, connected from pin WC to ground. In multiple device applications, a single RWC resistor may be made common to all devices. The actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

where:
Rh = Head resistance + external wire resistance, and
Rd = Damping resistance.

The write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on pin WDI, after the fault is corrected, are required to clear the WUS flag.

- WDI frequency too low
- Device in read mode
- Device not selected
- No write current

A multiple device enable condition can be detected by monitoring the voltage across a resistor connected from VCC to the wire OR'ed IMF (Current Monitor Function) pins. Pin IMF sinks one unit of current when the device is enabled.

To initialize the Write Data Flip Flop (WDFF) to pass current through the Y-direction of the head, pin WDI must be low when the previous read mode was commanded.

READ MODE

The read mode configures the SSI 32R522 as a low noise differential amplifier and deactivates the write current generator and write unsafe circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load.

IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

TABLE 1: MODE SELECT

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: HEAD SELECT

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	X	none

0 = Low level, 1 = High level, X = Don't care

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0 - HS2	I	Head Select: selects one of six heads
$\overline{CS}$	I	Chip Select: a low level enables the device
R/$\overline{W}$	I	Read/Write: a high level selects read mode
WP	I	Write Protect: a low level enables the write current source
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition
IMF	O*	Current Monitor Function: allows multichip enable fault detection
WDI	I	Write Data In: a negative transition toggles the direction of the head current
H0X - H5X H0Y - H5Y	I/O	X, Y Head Connections: Current in the X-direction flows into the X-port
RDX, RDY	O*	X, Y Read Data: differential read data output
WC	*	Write Current: used to set the magnitude of the write current
VCC1	-	+5V Logic Circuit Supply
VCC2	-	+5V Write Current Supply
VDD	-	+12V
GND	-	Ground

*When more than one device is used, these signals can be wire OR'ed.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	VALUE	UNITS
DC Supply Voltage		VDD	-0.3 to +14	VDC
		VCC1, 2	-0.3 to +7	VDC
Write Current		Iw	100	mA
Digital Input Voltage		Vin	-0.3 to VCC +0.3	VDC
Head Port Voltage		VH	-0.3 to VDD +0.3	VDC
Output Current	RDX, RDY	Io	-10	mA
	WUS	Iwus	+12	mA
Storage Temperature		Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	VDD	12 ± 5%	VDC
	VCC1	5 ± 5%	VDC
	VCC2	5 ± 5%	VDC
Operating Temperature	Tj	+25 to +135	°C

DC CHARACTERISTICS

Unless otherwise specified: recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
VDD Supply Current	Read Mode	-	34	mA
	Write Mode	-	38	mA
	Idle Mode	-	9	mA
VCC Supply Current	Read Mode	-	62	mA
	Write Mode	-	49+IW	mA
	Idle Mode	-	49	mA
Power Dissipation (Tj=+135°C)	Read Mode	-	800	mW
	Write Mode, Iw = 35 mA	-	950	mW
	Idle Mode	-	400	mW
Input Low Voltage (VIL)		-	0.8	VDC
Input High Voltage (VIH)		2.0	-	VDC
Input Low Current (IIL)	VIL = 0.8V	-0.4	-	mA
Input High Current (IIH)	VIH = 2.0V	-	100	µA

DC CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
RDX, RDY Common Mode Output Voltage	Read Mode	3	5	VDC
WUS Output Low Voltage (VOL)	Iol = 8 mA	-	0.5	VDC
IMF Output Current	$\overline{CS}$ = 0	0.73	1.23	mA
	$\overline{CS}$ = 1	-	0.02	mA

WRITE CHARACTERISTICS
Unless otherwise specified: recommended operating conditions apply, Iw = 10 mA, Lh = 1.5 µH, Rh = 30Ω and f(Data) = 5 MHz.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
WC Pin Voltage (Vwc)		1.61	1.7	1.79	V
Differential Head Voltage Swing		3.4	-	-	V(pk)
Unselected Head Current	Iw = 50 mA	-	-	1	mA(pk)
Differential Output Capacitance		-	-	30	pF
Differential Output Resistance	32R522R	800	1000	1350	Ω
	32R522	2400	-	-	Ω
WDI Transition Frequency	WUS=low	1.7	-	-	MHz
Write Current Range		6	-	35	mA

READ CHARACTERISTICS
Unless otherwise specified: recommended operating conditions apply, CL(RDX, RDY) < 20 pF and RL(RDX, RDY) = 1 KΩ.

PARAMETER		CONDITIONS	MIN	MAX	UNITS
Differential Voltage Gain		Vin = 1 mVpp @ 300 KHz	75	125	V/V
Bandwidth	-1dB	|Zs|<5Ω, Vin = 1 mVpp @ 300 KHz	25	-	MHz
	-3dB	|Zs|<5Ω, Vin = 1 mVpp @ 300 KHz	45	-	MHz
Input Noise Voltage		BW = 15 MHz, Lh = 0, Rh = 0	-	1.0	nV/√Hz
Differential Input Capacitance		Vin = 1 mVpp, f = 5 MHz	-	32	pF
Differential Input Resistance	32R522R	Vin = 1 mVpp, f = 5 MHz	460	-	Ω
	32R522	Vin = 1 mVpp, f = 5 MHz	770	-	Ω
Dynamic Range		DC input voltage where gain falls to 90% of its 0 VDC value, Vin = VDC + 0.5 mVpp, f = 5 MHz	-3	3	mV
Common Mode Rejection Ratio		Vin = 0 VDC + 100 mVpp @ 5 MHz	54	-	dB
Power Supply Rejection Ratio		100 mVpp @ 5 MHz on VDD 100 mVpp @ 5 MHz on VCC	54	-	dB

READ CHARACTERISTICS (continued)

PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNITS
Channel Separation	Unselected channels driven with 100 mVpp @ 5 MHz, Vin = 0 mVpp	45	-	dB
Output Offset Voltage		-300	+300	mV
Single Ended Output Resistance	f = 5 MHz	-	30	Ω
Output Current	AC Coupled Load, RDX to RDY	3.2	-	mA

SWITCHING CHARACTERISTICS
Unless otherwise specified: recommended operating conditions apply, IW = 10 mA, Lh = 1.5 µH, Rh = 30Ω and f(Data) = 5 MHz. Reference Figure 1.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
R/$\overline{W}$				
R/$\overline{W}$ to Write Mode	Delay to 90% of write current	-	0.6	µs
R/$\overline{W}$ to Read Mode	Delay to 90% of 100 mV, 10 MHz Read signal envelope or to 90% decay of write current	-	0.6	µs
$\overline{CS}$				
$\overline{CS}$ to Select	Delay to 90% of write current or to 90% of 100 mV, 10 MHz Read signal envelope	-	1	µs
$\overline{CS}$ to Unselect	Delay to 90% of write current	-	1	µs
HSn				
HS0, 1, 2 to any Head	Delay to 90% of 100 mV, 10 MHz Read signal envelope	-	0.4	µs
WUS				
Safe to Unsafe-TD1		0.6	3.6	µs
Unsafe to Safe-TD2		-	1	µs
IMF				
Propagation Delay	Delay from 50% point of $\overline{CS}$ to 90% of IMF current	-	0.6	µs
Head Current				
Prop. Delay-TD3	From 50% points, Lh=0µh, Rh=0Ω	-	32	ns
Asymmetry	WDI has 50% duty cycle and 1ns rise/fall time, Lh=0µh, Rh=0Ω	-	0.5	ns
Rise/Fall Time	10% - 90% points, Lh=0µh, Rh=0Ω	-	10	ns

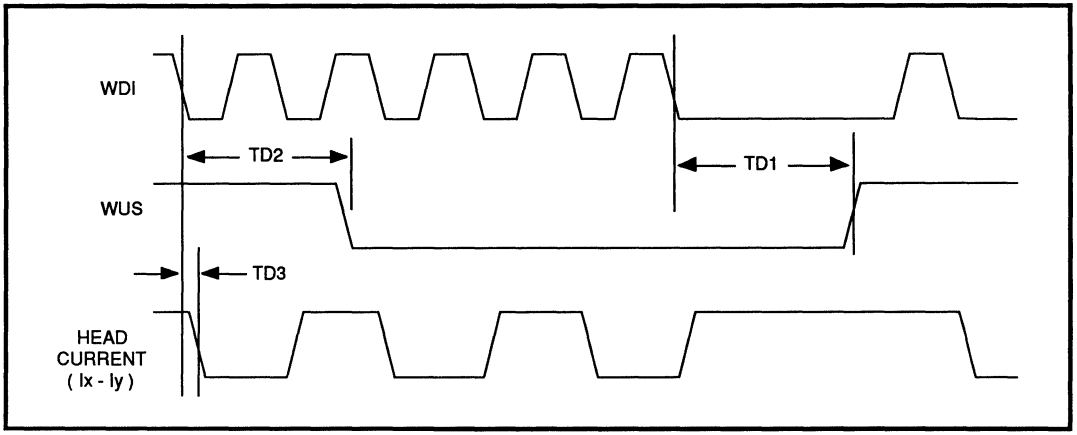


FIGURE 1: WRITE MODE TIMING DIAGRAM

APPLICATIONS INFORMATION

The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher input impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representative of actual performance.

TABLE 3: KEY PARAMETERS UNDER WORST CASE INPUT NOISE CONDITIONS

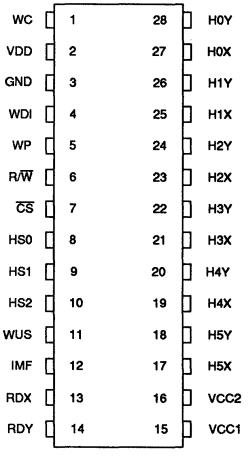
PARAMETER		Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Max.)		0.76	1.0	nV/√Hz
Differential Input Resistance (Min.)	32R522R	602	645	Ω
	32R522	1245	1455	Ω
Differential Input Capacitance (Max.)		25	28	pF

TABLE 4: KEY PARAMETERS UNDER WORST CASE INPUT IMPEDANCE CONDITIONS

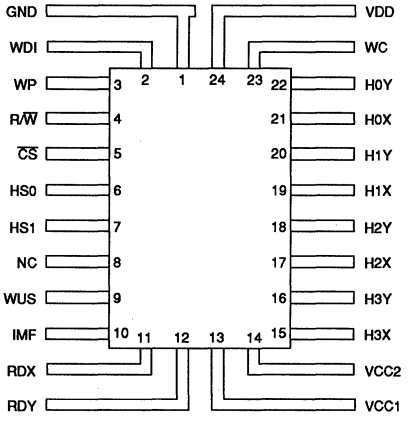
PARAMETER		Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Max.)		0.63	0.82	nV/√Hz
Differential Input Resistance (Min.)	32R522R	460	526	Ω
	32R522	770	960	Ω
Differential Input Capacitance (Max.)		30	32	pF

SSI 32R522/522R
4 or 6-Channel Thin Film Read/Write Device

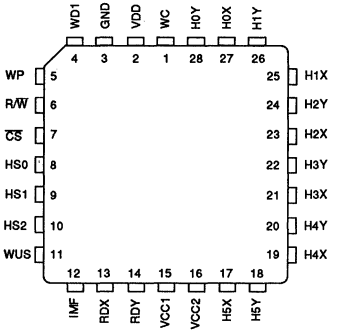
PACKAGE PIN DESIGNATIONS
(TOP VIEW)



28 - LEAD SOL



24 - LEAD FLATPACK



28 - LEAD PLCC

THERMAL CHARACTERISTICS: θja	
24 - Lead FLAT PACK	105°C/W
28 - Lead SOL	70°C/W
28 - Lead PLCC	65°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R522 - Read/Write IC		
4 - Channel Flat Pack	SSI 32R522 - 4F	32R522 - 4F
6 - Channel SOL	SSI 32R522 - 6L	32R522 - 6L
6 - Channel PLCC	SSI 32R522 - 6CH	32R522 - 6CH
SSI 32R522R- w/Internal Damping Resistors		
4 - Channel Flat Pack	SSI 32R522R - 4F	32R522R - 4F
6 - Channel SOL	SSI 32R522R - 6L	32R522R - 6L
6 - Channel PLCC	SSI 32R522R - 6CH	32R522R - 6CH

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SSI 32R524R
8-Channel Thin Film Read/Write Device

August, 1988

1

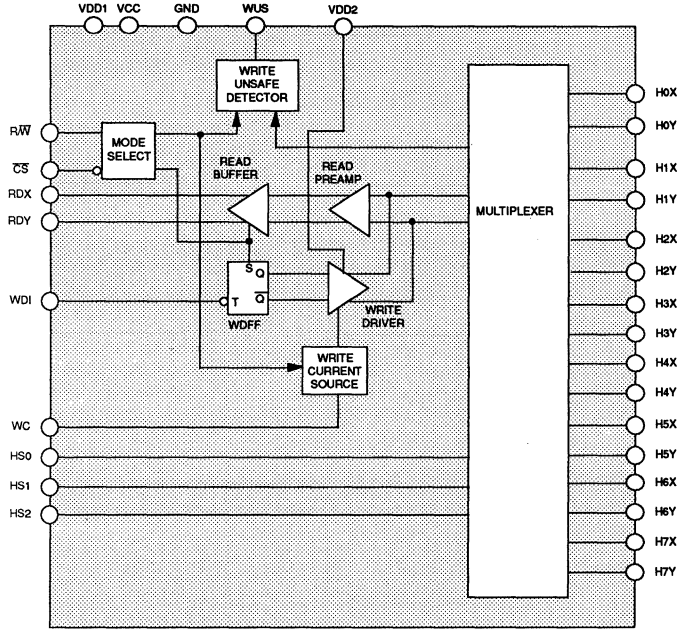
DESCRIPTION

The SSI 32R524R Read/Write device is a bipolar monolithic integrated circuit designed for use with two terminal thin film recording heads. It provides a low noise read amplifier, write current control and data protection circuitry for eight channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. It requires +5V and +12V power supplies and is available in a variety of package configurations. A mirror image pinout option is available to simplify flex circuit layout in multiple R/W device applications. The SSI 32R524R provides internal 740Ω damping resistors.

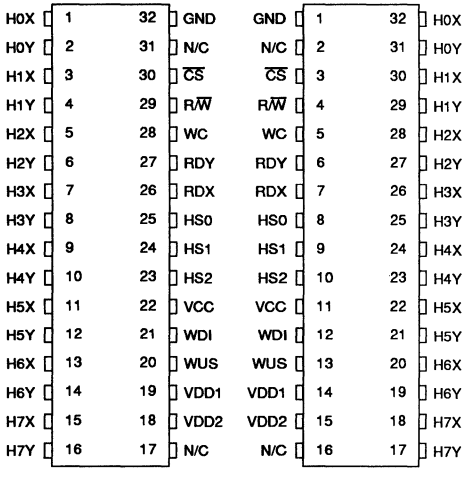
FEATURES

- **High performance:**
  - **Read mode gain = 100V/V**
  - **Input noise = 0.75 nV/√Hz max.**
  - **Input capacitance = 60 pF max.**
  - **Write current range = 20 to 60 mA**
  - **Head voltage swing = 7 Vpp**
  - **Write current rise time = 9 nsec**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Plug compatible to the SSI 32R501, SSI 32R511 & SSI 32R512**
- **Compatible with two & three terminal thin film heads**
- **Write unsafe detection**
- **+5V, +12V power supplies**
- **Mirror image pinout option**

BLOCK DIAGRAM



PIN DIAGRAM



32-LEAD SOW **32-LEAD SOW MIRROR**

CAUTION: Use handling procedures necessary for a static sensitive component.

0888

SSI 32R524R
8-Channel Thin Film Read/Write Device

CIRCUIT OPERATION

The SSI 32R524R addresses eight two-terminal thin film heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

WRITE MODE

The write mode configures the SSI 32R524R as a differential current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y directions of the selected head on each high to low transition on pin WDI, Write Data Input.

A preceding read operation initializes the Write Data Flip Flop (WDFF) to pass write current in the X-direction of the head, which is defined as entering from the Y-side and flowing to the X-side.
The magnitude of the write current (0-pk) given by:

$$Iw = \frac{K}{RWC}$$

where K (Write Current Constant) = 70 ± 5%, is programmed by an external resistor RWC, connected from pin WC to ground. The actual head current Ix, y is given by:

$$Iw,y = \frac{Iw}{1 + Rh/Rd}$$

where:
Rh = head resistance + external wire resistance, and
Rd = damping resistance.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on pin WDI, after the fault is corrected, are required to clear the WUS flag.

- Open head
- WDI frequency too low
- Device not selected
- Device in read mode
- No write current

Power dissipation in Write Mode may be reduced by placing a resistor, Rw, between VDD1 and VDD2. The resistor value should be chosen such that Iw Rw ≤ 3.0V for an accompanying power dissipation reduction of $(Iw)^2Rw$. If a resistor is not used, VDD2 should be connected to VDD1. Note that Rw will also provide current limiting in the event of a head short.

READ MODE

The read mode configures the SSI 32R524R as a low noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent Pulse Detection circuitry.

IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector, and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire OR'ed.

TABLE 1: MODE SELECT

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: HEAD SELECT

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

0 = Low level, 1 = High level

PIN DESCRIPTIONS

NAME	TYPE	DESCRIPTION
HSO - HS2	I	Head Select: selects one of eight heads
$\overline{CS}$	I	Chip Select: a low level enables the device
R/$\overline{W}$	I	Read/Write: a high level selects Read Mode
WUS	O*	Write Unsafe: Open collector output, a high level indicates an unsafe writing condition
WDI	I	Write Data In: a negative transition toggles the direction of the head current
H0X - H7X H0Y - H7Y	I/O	X, Y Head Connections: Current in the X-direction flows into the X-port
RDX, RDY	O*	X, Y Read Data: differential read data output
WC	-	Write Current: used to set the magnitude of the write current
VCC	-	+5V Logic Circuit Supply
VDD1	-	+12V
VDD2	-	Positive Power Supply for Write current drivers
GND	-	Ground
* When more than one R/W device is used, these signals can be wire OR'ed.		

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	VALUE	UNITS
DC Supply Voltage		VDD1, 2	-0.3 to +14	VDC
		VCC	-0.3 to +7	VDC
Write Current		Iw	100	mA
Digital Input Voltage		Vin	-0.3 to VCC +0.3	VDC
Head Port Voltage		VH	-0.3 to VDD2 +0.3	VDC
WUS Pin Voltage Range		Vwus	-0.3 to +14	VDC
Output Current	RDX, RDY	Io	-10	mA
	WUS	Iwus	+12	mA
Storage Temperature		Tstg	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	VDD1	12 ± 10%	VDC
	VDD2	≥VDD1 - 3.0V	VDC
	VCC	5 ± 10%	VDC
Junction Temperature	Tj	+25 to +135	°C

DC CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD1 Supply Current	Read Mode	-	-	50	mA
	Write Mode	-	-	45	mA
	Idle Mode	-	-	25	mA
VDD2 Supply Current	Read Mode	-	-	200	µA
	Write Mode	-	-	Iw+0.4	mA
	Idle Mode	-	-	200	µA
VCC Supply Current	Read Mode	-	-	60	mA
	Write Mode	-	-	50	mA
	Idle Mode	-	-	45	mA
Power Dissipation (Tj = +135°C)	Read Mode	-	-	900	mW
	Write Mode Iw = 40mA, VDD2 = VDD1	-	-	1300	mW
	Write Mode Iw = 60mA, VDD1 - VDD2 = 3.0V	-	-	1425	mW
	Idle Mode	-	-	500	mW
Input Low Voltage (VIL)		-	-	0.8	VDC
Input High Voltage (VIH)		2.0	-	-	VDC
Input Low Current (IIL)	VIL = 0.8v	-0.8	-	-	mA
Input High Current (IHL)	VIH = 2.0v	-	-	100	µA
WUS Output Low Voltage (VOL)	Iol = 8mA	-	-	0.5	VDC
VDD Fault Voltage		8.5	-	10.0	VDC
VCC Fault Voltage		3.5	-	4.2	VDC
Head Current (HnX, HnY)	Write Mode, 0≤VCC ≤3.5V 0≤VDD1 ≤8.5V	-200	-	+200	µA
	Read/Idle Mode 0≤VCC ≤5.5V 0≤VDD1 ≤13.2V	-200	-	+200	µA

WRITE CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply, Iw = 40mA, Lh = 500nH, Rh = 30Ω and f(WDI) = 5MHz.

PARAMETER	CONDITIONS	MIN.	NOM	MAX	UNITS
Write Current Constant "K"		66.5	-	73.5	V
Differential Head Voltage Swing		7	-	-	Vpp
Unselected Head Current		-	-	1	mA(pk)
Differential Output Capacitance		-	-	35	pF
Differential Output Resistance		400	740	1000	Ω
WDI Transition Frequency	WUS = low	1.0	-	-	MHz
Write Current Range		20	-	60	mA

READ CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply, CL (RDX, RDY) < 20pF and RL (RDX,RDY) = 1KΩ.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain		Vin=1 mVpp @ 300 kHz	80	100	120	V/V
Bandwidth	-1dB	|Zs|<5Ω, Vin=1 mVpp @ 300 kHz	25	-	-	MHz
	-3dB	|Zs|<5Ω, Vin=1 mVpp @ 300 kHz	45	-	-	MHz
Input Noise Voltage		BW = 15 MHz, Lh = 0, Rh = 0	-	0.55	0.75	nV/√Hz
Differential Input Capacitance		Vin = 1 mVpp, f = 5 MHz	-	-	60	pF
Differential Input Resistance		Vin = 1 mVpp, f = 5 MHz	220	-	-	Ω
Dynamic Range		DC input voltage where gain falls to 90% of its 0 VDC value, Vin = VDC +0.5 mVpp, f = 5 MHz	-3	-	3	mV
Common Mode Rejection Ratio		Vin = 0 VDC+100 mVpp @ 5 MHz	54	-	-	dB
Power Supply Rejection Ratio		100 mVpp @ 5 MHz on VDD1 100 mVpp @ 5 MHz on VCC	54	-	-	dB
Channel Separation		Unselected channels driven with 100 mVpp @ 5 MHz, Vin = 0 mVpp	45	-	-	dB
Output Offset Voltage			-360	-	+360	mV
RDX, RDY Common Mode		Read Mode	2.2	2.9	3.6	VDC
Output Voltage		Write Mode	-	2.9	-	VDC
Single Ended Output Resistance		f = 5 MHz	-	-	30	Ω
Output Current		AC Coupled Load, RDX to RDY	3.2	-	-	mA

SWITCHING CHARACTERISTICS (See Figure 1)
Unless otherwise specified, recommended operating conditions apply, Iw = 40mA, Lh = 500nH, Rh = 30Ω and f(WDI) = 5MHz.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
R/$\overline{W}$				
R/$\overline{W}$ to Write Mode	Delay to 90% of write current	-	0.6	µs
R/$\overline{W}$ to Read Mode	Delay to 90% of 100mV 10MHz Read signal envelope or to 90% decay of write current	-	0.6	µs
$\overline{CS}$				
$\overline{CS}$ to Select	Delay to 90% of write current or to 90% of 100mV 10MHz Read signal envelope	-	0.6	µs
$\overline{CS}$ to Unselect	Delay to 10% of write current	-	0.6	µs
HSn				
HS0, 1, 2 to any Head	Delay to 90% of 100mV 10MHz Read signal envelope	-	0.4	µs
WUS				
Safe to Unsafe - TD1		0.6	5.0	µs
Unsafe to Safe - TD2		-	1	µs
Head Current				
Prop. Delay - TD3	From 50% points, Lh=0µh, Rh=0Ω	-	32	ns
Asymmetry	WDI has 50% duty cycle and 1ns rise/fall time, Lh=0µh, Rh=0Ω	-	1	ns
Rise/Fall Time	10%-90% points, Lh=0µh, Rh=0Ω	-	9	ns
Rise/Fall Time	10%-90% points, R(HnX, HnY)=10Ω	-	10	ns

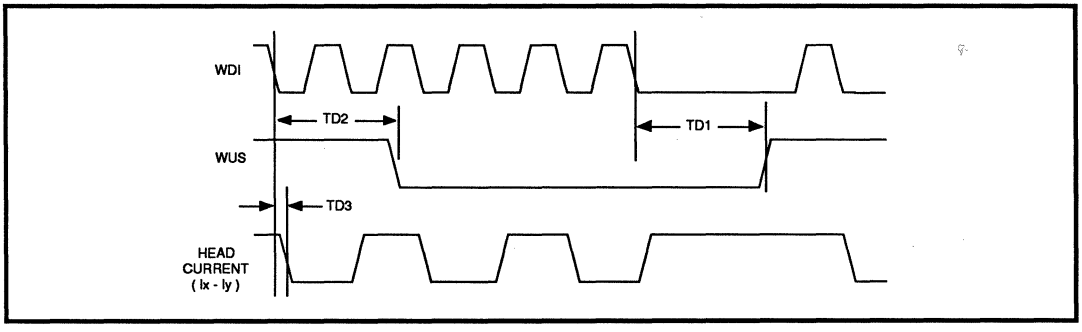


FIGURE 1: WRITE MODE TIMING DIAGRAM

APPLICATIONS INFORMATION

The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher input impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representative of actual performance.

TABLE 3: KEY PARAMETERS UNDER WORST CASE INPUT NOISE CONDITIONS

PARAMETER	Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Max.)	0.5	0.75	$nV/\sqrt{Hz}$
Differential Input Resistance (Min.)	292	318	Ω
Differential Input Capacitance (Max.)	43	48	pF

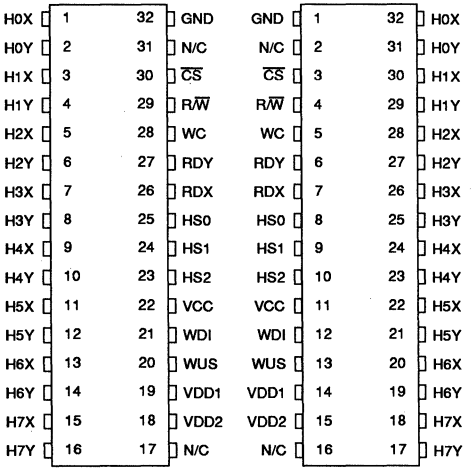
TABLE 4: KEY PARAMETERS UNDER WORST CASE INPUT IMPEDANCE CONDITIONS

PARAMETER	Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Max.)	0.45	0.6	$nV/\sqrt{Hz}$
Differential Input Resistance (Min.)	220	260	Ω
Differential Input Capacitance (Max.)	55	60	pF

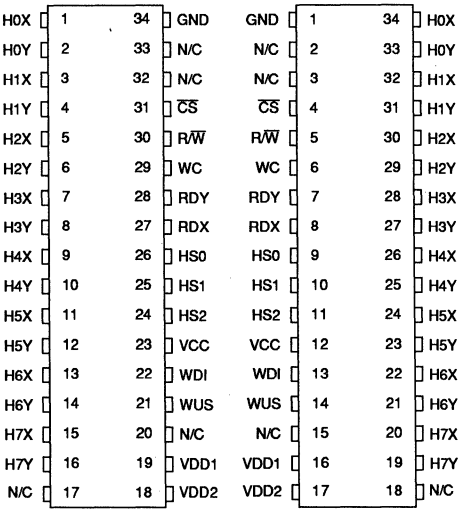
SSI 32R524R
8-Channel Thin Film
Read/Write Device

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



32-LEAD SOW **32-LEAD SOW MIRROR**



34-LEAD SOL **34-LEAD SOL MIRROR**

THERMAL CHARACTERISTICS: θja

32-Lead SOW	55°C/W
34-Lead SOL	50°C/W

ORDERING INFORMATION

PART DESCRIPTION		ORDER NO.	PKG. MARK
SSI 32R524R	8-Channel SOW	SSI 32R524R-8W	32R524R-8W
	8-Channel SOL	SSI 32R524R-8L	32R524R-8L
SSI 32R524RM	8-Channel SOW	SSI 32R524RM-8W	32R524RM-8W
	8-Channel SOL	SSI 32R524RM-8L	32R524RM-8L

silicon systems™

Silicon Systems, Inc., 14351 Myford Road, Tustin CA 92680, (714) 731-7110, TWX 910-595-2809

SSI 32R525R
4-Channel Thin Film Read/Write Device

August, 1988

1

DESCRIPTION

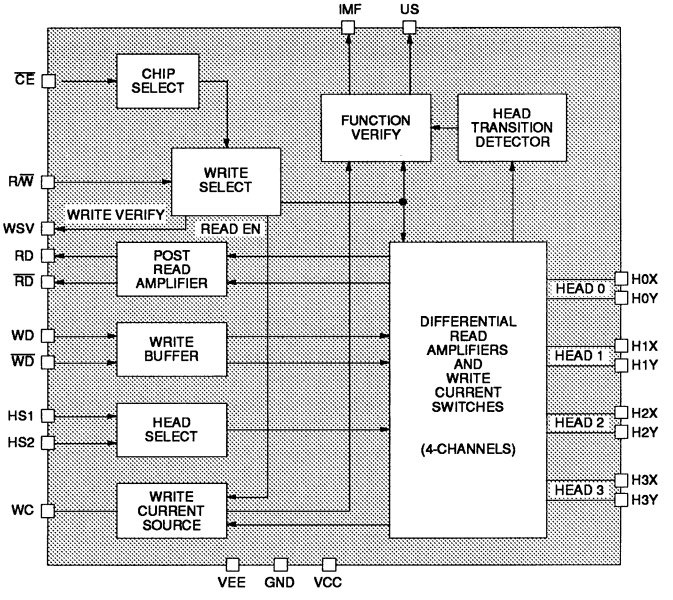
The SSI 32R525 is an integrated read/write circuit designed for use with non-center tapped thin film heads in disk drive systems. Each chip controls four heads and has three modes of operation: read, write, and idle. The circuit contains four channels of read amplifiers and write drivers and also has an internal write current source.

A current monitor (IMF) output is provided that allows a multichip enable fault to be detected. An enabled chip's output will produce one unit of current. An open collector output, write select verify (WSV), will go low if the write current source transistor is forward biased. The circuit operates on +5 volt, and -5 volt power and is available in 24-pin flatpack and SOL packages.

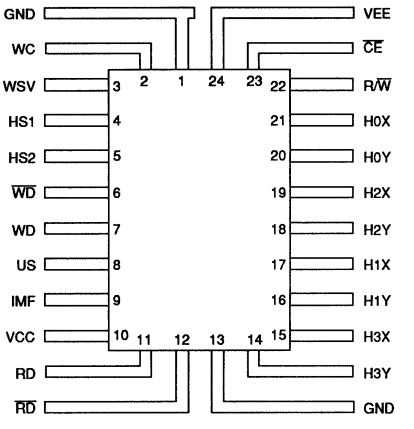
FEATURES

- **High performance**
  - **Read Mode Gain = 150 V/V**
  - **Input Noise = 0.8 nV/$\sqrt{Hz}$ max**
  - **Input Capacitance = 35 pF**
  - **Write Current Range = 25 mA to 40 mA**
  - **Write Current Rise Time = 10 nsec**
  - **Head Voltage Swing = 3.8 Vpp min**
- **Write unsafe detection**
- **-5V, +5V power supplies**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32R525R
4-Channel Thin Film
Read/Write Device

FUNCTIONAL DESCRIPTION

WRITE MODE

In write mode (R/$\overline{W}$ and $\overline{CE}$ low) the circuit functions as a differential current switch. The Head Select Inputs (HS1 and HS2) determine the selected head. The Write Data Inputs (WD, $\overline{WD}$) determine the polarity of the head current. The write current magnitude is adjustable by an external 1% resistor, Rx from WC to VCC, where:

$$I_w = \frac{80}{Rx} \text{ Adc}$$

READ MODE

In the Read Mode, (R/$\overline{W}$ high and $\overline{CE}$ low), the circuit functions as a differential amplifier. The amplifier input terminals are determined by the Head Select inputs.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RD and $\overline{RD}$ outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

HEAD SELECT TABLE

HEAD SELECTED	HS2	HS1
0	0	0
1	0	1
2	1	0
3	1	1

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 4.75 ≤ VCC ≤ 5.25, -5.35 ≤ VEE ≤ -4.75V, 0° ≤ T (junction) ≤ 100°C.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive Supply Voltage, Vcc	6	V
Negative Supply Voltage, VEE	-6	V
Operating Junction Temperature	125	°C
Storage Temperature	-65 to 150	°C
Lead Temperature (Soldering, 10 sec)	260	°C
Input Voltages		
Head Select (HS)	-0.4 to Vcc + 0.3	V
Chip Enable ($\overline{CE}$)	-0.4 to Vcc+ 0.3	V
Read Select (R/$\overline{W}$)	-0.4V or -2 mA to Vcc + 0.3	V
Write Data (WD, $\overline{WD}$)	VEE to 0.3	V
Head Inputs (Read Mode)	-0.6 to 0.4	V
Outputs		
Read Data (RD, $\overline{RD}$)	0.5 to Vcc + 0.3	V
Write Unsafe (WUS)	-0.4V to Vcc + 0.3 and 20 mA	V
Write Select Verify (WSV)	-0.4V to Vcc + 0.3 and 20 mA	V

ABSOLUTE MAXIMUM RATINGS (Continued)

PARAMETER	RATING	UNIT
Outputs (Continued)		
Current Monitor (IMF)	-0.4 to Vcc + 0.3	V
Current Reference (WC)	VEE to Vcc + 0.3 and 8 mA	V
Head Outputs (Write Mode)	Iw max = 150	mA

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Power Dissipation	Write mode, Iw = 40 mA			500	mW
Positive Supply Current (ICC)	Idle Mode			10	mA
Positive Supply Current (ICC)	Read Mode			25	mA
Positive Supply Current (ICC)	Write Mode			12	mA
Negative Supply Current (IEE)	Idle Mode			8	mA
Negative Supply Current (IEE)	Read Mode			45	mA
Negative Supply Current (IEE)	Write Mode			40 + Iw	mA

LOGIC SIGNALS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Chip Enable Low Voltage (VLCE)	Read or Write Mode			0.8	V
Chip Enable High Voltage (VHCE)	Idle Mode	2.0			V
Chip Enable Low Current (ILCE)	VLCE = 0V			-0.40	mA
Chip Enable High Current (IHCE)	VHCE = 2.0V			20	µA
Read Select High Voltage (VHR/W)	Read or Idle Mode	2.0			V
Read Select Low Voltage (VLR/W)	Write or Idle Mode			0.8	V

LOGIC SIGNALS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Read Select high Current (IHR/W)	VHR/W = 2.0V			-0.40	mA
Read Select Low Current (ILR/W)	VLR/W = 0V			20	µA
Head Select High Voltage (VHHS)		2.0			V
Head Select Low Voltage (VLHS)				0.8	V
Head Select High Current (IHHS)	VHHS = VCC			0.25	mA
Head Select Low Curren (ILHS)	VLHS = 0V	-0.1		0.25	mA
WUS, WSV Low Level Voltage	ILUS = 8 mA (denotes safe condition)			0.5	V
WUS, WSV High Level Current	VHUS = 5.0V (denotes unsafe condition)			100	µA
IMF on Current		2.40		3.50	mA
IMF off Current				0.02	mA
IMF Voltage Range		0		VCC + 0.3	V

READ MODE
Tests performed with 100Ω load resistors from RD and $\overline{RD}$ through series isolation diodes to VCC.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Voltage Gain	Vin = 1m Vpp, f = 300 KHz	100		150	V/V
Voltage Bandwidth (-3dB)	Zs < 5z, Vin = 1m Vpp f midband = 300 KHz	55		100	MHz
Input Noise Voltage	Zs = 0Ω , Vin = 0V, Power Bandwidth = 15 MHz			0.8	nV√Hz
Differential Input Capacitance	Vin = 0V, f = 5 MHz			35	pF
Differential Input Resistance	Vin = 0V, f = 5 MHz	500		1800	Ω
Input Bias Current (per side)	Vin = 0V			0.17	mA
Dynamic Range	DC input voltage where AC gain falls to 90% of the gain with .5m Vpp input signal	-3.0		3.0	mV
CMRR	Vin = 100m Vpp, 0V DC 1 MHz ≤ f ≤a 10 MHz	54			dB
	10 MHz ≤ f ≤ 20 MHz	48			dB

READ MODE (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Power Supply Rejection Ratio	VCC or VEE = 100m Vpp 1 MHz ≤ f ≤ 10 MHz	54			dB
	10 MHz ≤ f ≤ 20 MHz	36			dB
Channel Separation	The three unselected channels are driven with Vin = 100m Vpp 1 MHz ≤ f ≤ 10 MHz	43			dB
	10 MHz ≤ f ≤ 20 MHz	37			dB
Output Offset Voltage		-360		360	mV
Output Leakage Current	Idle Mode			0.01	mA
Output Common Mode Voltage		VCC - 1.1		VCC - 0.3	V
Single Ended Output Resistance		10			KΩ
Single Ended Output Capacitance				10	pF

WRITE MODE

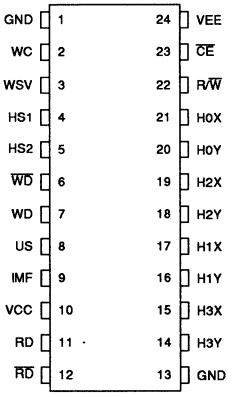
PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Current Range (Iw)		25		40	mA
Current Tolerance	Current set to nominal value by Rx = 2K to 3.2K, Tj = 50 °C	-8		+8	%
(Iw) (Rh) Product		0.24		1.30	V
Differential Head voltage Swing	Iw = 40 mA	3.8			Vpp
Unselected Head Transient Current	Iw = 40 mA, Lh = 0.5 µH, Rh = 20Ω, Non adjacent heads tested to minimize external coupling effects			2	mAp
Head Differential Load Resistance, Rd		1700		2600	Ω
Head Differential Load Capacitance				10	pF
Differential Data Voltage, (WD – $\overline{WD}$)		0.20			V
Data Input Voltage Range		-1.87		+0.1	V
Data Input Current (per side)	Chip Enabled			150	µA
Data Input Capacitance	per side to GND			10	pF

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Idle to Read/Write Transition Time				0.6	µs
Read/Write to Idle Transition Time				0.3	µs
Read to Write Transition Time	VLCE = 0.8V, Delay to 90% of Iw			0.6	µs
Write to Read Transition Time	VLCE = 0.8V, Delay to 90% of 20 MHz Read Signal envelope, Iw decay to 10%			0.3	µs
Head Select Switching Delay	Read or Write Mode			0.3	µs
Head Current Transition Time 10% to 90%	Iw = 40 mA, Lh = 0.15 µH, Rh = 20Ω			10	ns
Head Current Overshoot	Iw = 40 mA, Lh = 0.15 µH, Rh = 20Ω, relative to total current charge			25	%
Head Current Switching Time Symmetry	Iw = 40 mA, Lh = 0.15 µH, Rh = 20Ω, WD & $\overline{WD}$ transitions 2nS, switching time symmetry 0.2 nS			1.5	ns
WSV Transition Time	Delay from 50% of write select swing to 90% of final WSV voltage, Load = 2KΩ // 20 pF			0.3	µs
Unsafe to Safe Delay After Write Data Begins (WUS)	f(data) = 5 MHz			0.3	µs
Safe to Unsafe Delay, (WUS)	Head open or shorted to GND, no write current, head select input open			0.3	µs
Safe to Unsafe Delay, (WUS)	Non-switching write data	0.5		2.0	µs
IMF Switching Time	Delay from 50% of CE to 90% of final IMF current			0.3	µs

SSI 32R525R
4-Channel Thin Film Read/Write Device

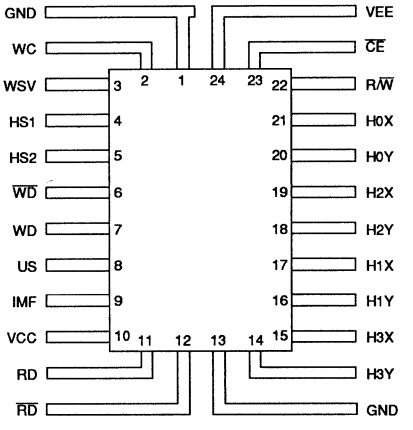
PACKAGE PIN DESIGNATIONS
(TOP VIEW)



24-Pin SOL

THERMAL CHARACTERISTICS: Ø ja

24-Pin Flatpack	100°C/W
24-Pin SOL	80°C/W



24-Pin Flatpack

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32R525R		
24-Pin Flatpack	SSI 32R525R-4F	SSI 32R525R-4F
24-Pin SOL	SSI 32R525R-4L	SSI 32R525R-4L

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NOTES:

Section 2

HDD PULSE DETECTION

SSI 32P540-Series
Read Data Processor

August, 1988

DESCRIPTION

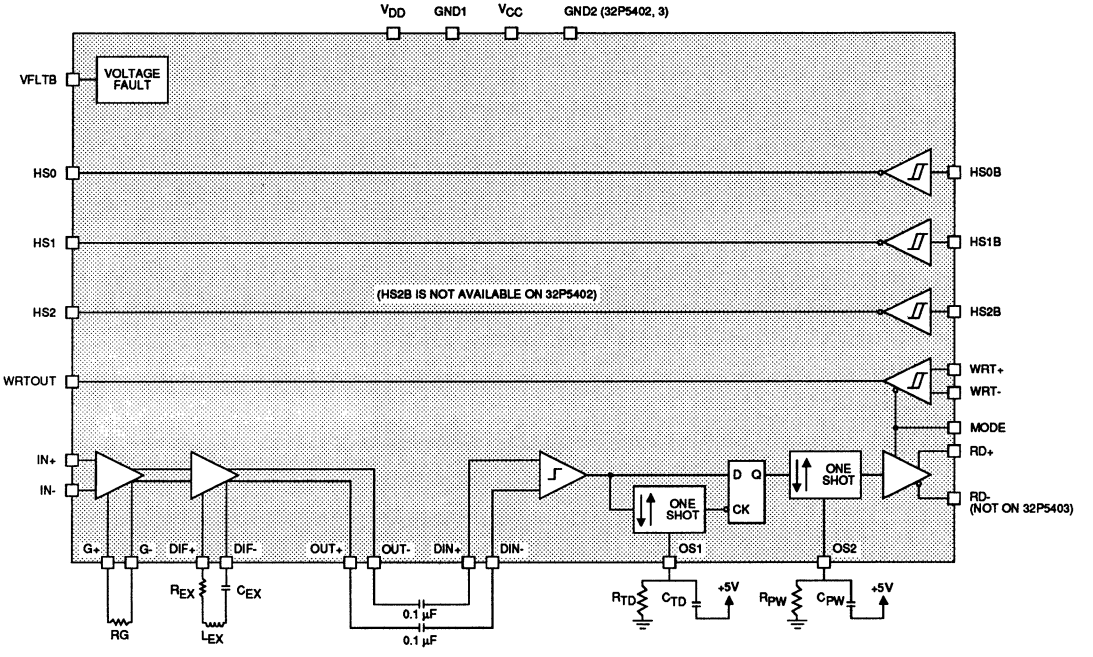
The SSI 32P540 is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of MFM read signals from rigid media. ST506 compatible interfacing is provided for write data signals, head select lines and recovered read data as applicable.

In read mode the SSI 32P540 provides amplification, differentiation and time domain qualification of head preamplifier outputs. The recovered data is available at the output of a differential line driver that conforms to the ST506 interface specification. In write mode the SSI 32P540 provides a differential line receiver conforming with ST506 requirements. Schmitt Trigger inputs on head select lines and an open collector output for voltage fault indication are provided for interface compatibility. (Continued)

FEATURES

- Differential Read and Write Ports
- Schmitt Trigger Head Select Inputs for Higher Noise Immunity
- Programmable Gain
- Time Domain Pulse Qualification Supports MFM Encoded Data Retrieval
- Supply Voltage Fault Detection
- +12 Volt and +5 Volt Power Supplies
- I/O Meets ST506 Requirements
- Dual-in-Line and Surface Mount Packages Available
- Adjustable Time Domain Filter and Output Pulse Width Settings

BLOCK DIAGRAM



DESCRIPTION (Continued)

The SSI 32P5402 is a dual-ground version for use in noisier environments. In order to provide this feature the number of head select lines is reduced to two. The SSI 32P5403 has dual grounds and an open-collector RD output instead of a differential line-driver output.

When used with a read/write preamplifier (i.e. SSI 32R117 or SSI 32R501), the SSI 32P540 or SSI 32P5402 and required external passive components perform all read/write signal processing necessary between the heads and the interface connector of an ST506 compatible Winchester disk drive. A line driver is required with the SSI 32P5403 .

CIRCUIT OPERATION

In both read and write modes, Schmitt Trigger inputs are used to buffer the three head select lines providing the increased noise immunity required of a ST506 interface. A power supply monitoring function, VFLTB, is provided to flag a low voltage fault condition if either supply is low. A low voltage fault condition results in a low level output on the VFLTB pin.

READ MODE

In the read mode (MODE input high) the read signal is detected, time domain qualified and made available at RD+ and RD- as differential MFM encoded data, or at the RD+ open collector output. This is accomplished by the on-board Amplifier, Differentiator, Zero Crossing Detector, Time Domain Filter, Output One Shot and Line Driver circuits.

The amplified and filtered read back signal, which contains pulses corresponding to magnetic transitions in the media is AC coupled into the input amplifier. A resistor, Rg, connected between pins G+ and G- is used to adjust the 1st stage amplifier gain according to the following expression.

$$Av1 = \frac{628}{17 + Rx} \quad \text{Where } Rx = \frac{94 \times (Rg + 42)}{230 + Rg}$$

First Stage gain can be monitored at the DIF+ and DIF- pins.

The amplifier is followed by an active differentiator whose external network serves to transform peaks in the input signal into zero-crossings while maintaining the time relationship of the original input peaks. Differentiator response is set by an external capacitor or more complex series LRC network between the DIF+ and DIF- pins. The transfer function with such a network is:

$$Av2 = \frac{-1420\,Cex\,s}{Lex\,Cex\,s^2 + (Rex + 46)\,Cex\,s + 1}$$

where Cex = external capacitor (50 pF to 250 pF)

Rex = external resistor

Lex = external inductor

$s = js = j2\pi f$

Total gain from IN+ and IN- to OUT+ and OUT- is:

$Av = Av1 \times Av2$

To reduce pulse pairing (bit shift), it is essential that the input to the zero-crossing detector be maximized to reduce the effect of any comparator offset. This means that the above gains should be chosen such that the differential voltage at OUT+ and OUT- approaches 5 Vpp at max input and frequency.

The Differentiator output is AC coupled into a zero-crossing detector that provides an output level change at each positive or negative zero transition on its input. The zero-crossing detector output is coupled to a Time Domain Filter that eliminates false triggering of the output one-shot by spurious zero-crossings. The validity decision is based on a minimum duration between zero crossings that can be set externally by an RC network on the TD pin.

The output of the Time Domain Filter triggers a one-shot that defines the output pulsewidth based on an external RC network on the PW pin. These output pulses are fed into a line driver that provides a high-current differential output at RD+ and RD-, or are made available as an open-collector output at RD+.

WRITE MODE

In the write mode (MODE input low) the differential line receiver is enabled. This receiver accepts the differential data from the ST506 interface and outputs a TTL signal for the write data input of an external R/W

amplifier. A low on the MODE input also puts the read outputs in a high impedance state, allowing several SSI 32P540's to be multiplexed on a bus.

LAYOUT CONSIDERATIONS

The SSI 32P540 is a high gain wide bandwidth device that requires care in layout. The designer should keep analog signal lines as short as possible and balanced. Analog test points should be provided with a probe ground in the immediate vicinity. Do not run digital signals under the chip or next to analog inputs. Use of a ground plane is recommended along with supply bypassing and separation of the SSI 32P540 ground from other circuits on the disk drive PCB.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 4.5V < Vcc < 5.5V, 10.8V < Vdd < 13.2V, 25 °C < T(junction) < 135 °C.

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum rating may permanently damage the device.

PARAMETER	RATING	UNIT
5V Supply Voltage, Vcc	6	V
12V Supply Voltage, Vdd	14	V
Storage Temperature	-65 to +150	°C
Operating Temperature, Tj	+25 to +135	°C
Lead Temperature (soldering 10 sec)	260	°C
Pin Voltages: IN+, IN-, G+, G-, DIF +, DIF-, OUT +, OUT-, DIN + DIN -	0.3 to Vdd + 0.3	V
RD +, RD - , WRTOUT, HSO, HS1, HS2, VFLTB	-0.3 to Vcc + 0.3 or 100 mA	V
TD, PW, MODE, WRT +, WRT-, HS0B, HS1B, HS2B	-0.3 to Vcc + 0.3	V

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Icc - Vcc Supply Current	Read mode, no TTL or RD ± loads		35.0	46	mA
	Write/Disable mode, no TTL loads		36.5	43	mA
Idd - Vdd Supply Current	Read mode		33.5	48	mA
	Write/Disable mode		34.5	50	mA
Pd - Power Dissipation	Tj = 135 °C Read/Write modes			820	mW

LOGIC SIGNALS - MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Low Voltage (V_{IL})		-0.3		+0.8	V
Input Low Current (I_{IL})	V_{IL} = 0.4V			-0.8	mA
Input High Voltage (V_{IH})		2.0		Vcc + 0.3	V
Input High Current (I_{IH})	V_{IH} = 2.4V			100	µA

LOGIC SIGNALS - HSnB

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Threshold Voltage, VT + Positive-Going	Vcc = 5.0V	1.4		2.0	V
Threshold Voltage, VT - Negative-Going	Vcc = 5.0V	0.6		1.15	V
Input Low Current (I_{IL})	V_{IL} = 0.4V			- 0.4	mA
Input High Current (I_{IH})	V_{IH} = 2.4V			100	µA

LOGIC SIGNALS - WRTOUT, HSn

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Output Low Voltage (V_{OL})	I_{OL} = 1.6 ma			0.4	V
Output High Voltage (V_{OH})	I_{OH} = -500 µA	2.4			V

LOGIC SIGNALS - VFLTB & RD Open Collector Output

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Output Low Voltage (V_{OL})	I_{OL} = 1.6 mA 4.5 < Vcc < 5.5 I_{OL} = 0.5 mA,1.0 < Vcc < 4.5V (VFLTB Only)			0.4	V
Output High Current (I_{OH})				25	µA

MODE CONTROL

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Read to Write Transition Time				1.0	µs
Write to Read Transition Time				1.0	µs

SUPPLY VOLTAGE FAULT DETECT

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Vdd Fault Threshold	VFLTB transition from high to low	9.5		10.8	V
Vcc Fault Threshold	VFLTB transition from high to low	4.3		4.6	V

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Input Voltage		±0.4			V
Input Hysteresis			±40		mV
Single Ended Input Resistance		4.0			KΩ
Input Common Mode Voltage Range		0.0		5.0	V
Input Pulse Width		20			ns
Propagation Delay (WRT + & WRT - TO WRTOUT)	V (WRT+ - WRT-) = 0 to WRTOUT = 1.3V See Note & Fig. 1 T_{PD}			40	ns
Output Rise and Fall times	WRTOUT transition from 0.7 to 1.9V, See Note & Fig. 1			15	ns
Note: WRTOUT load is 30 pF to GND and 2.5 KΩ to Vcc					

READ MODE

Unless otherwise specified RD+ and RD- are loaded with 100Ω differentially and 30 pF per side to GND, IN+ and IN - are AC coupled, G+ and G- are open. An 800Ω resistor is tied between the DIF+ and DIF - pins with each pin loaded to GND with < 3 pF. The OUT+ and OUT- pins are loaded with < 3 pF in parallel with > 5 KΩ AC coupled (i.e. no DC current).

AMPLIFIER & ACTIVE DIFFERENTIATOR

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential	RG = ∞, Rex = 800Ω	7.2		12.6	V/V
Voltage Gain (IN± to OUT±)	RG = 0Ω, Rex = 200Ω	72		155	V/V
Bandwidth	-3 dB point	30			MHz
Common Mode Input Impedance (IN±)			3.5		KΩ
Differential Input Resistance (IN±)	V(IN+ - IN-) = 100 mVpp, 2.5 MHz, AC coupled		6.0		KΩ
Differential Input Capacitance (IN±)	V(IN+ - IN-) = 100 mVpp, 2.5 MHz, AC coupled			8	pF

AMPLIFIER & ACTIVE DIFFERENTIATOR (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Noise (IN±)	Inputs shorted together RG = 0Ω, Rex = 200Ω			10	nV/√Hz
V(DIF+ DIF-) Output Swing	Set by RG			3.2	Vpp
V(OUT+ -) Output Swing	Set by Rex, Lex, Cex Impedance			5	Vpp
Dynamic Range	Common mode DC input where gain falls to 90% of 0.0V DC common mode input. 10 mVpp AC input, RG = ∞, Rex = 1200Ω	-240		+240	mV
DIF+ to DIF- pin Current		±1.9			mA
OUT+ to OUT- pin Current		±3.8			mA
CMRR (input referred)	V(IN+) = V(IN-) = 100 mVpp, 5 MHz, RG = 0Ω, Rex = 200Ω	40			dB
PSRR (input referred)	Vdd or Vcc = 100 mVpp, 5 Mhz, RG = 0Ω, Rex = 200Ω	40			dB

ZERO CROSSING DETECTOR

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Offset Voltage				5.0	mV
Input Signal Range				5.0	Vpp
Differential Input Impedance (DIN±)			4.4		KΩ

LINE DRIVE (SSI 32P540 & SSI 32P5402 only)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Output Sink Current	V_{OL} = 0.5V, V(MODE) = 2.0V	20			mA
Output Source Current	V_{OH} = 2.5V, V(MODE) = 2.0V	-2			mA
Output Current	Vo=0V to Vcc, V(MODE) = 0V	-50		50	µA
Output Rise Time	Vo = 0.7V to 1.9V 100Ω between RD+ and RD-, 30 pF to GND	2		30	ns
Output Fall Time	Vo = 1.9V to 0.7V 100Ω between RD+ and RD-, 30 pF to GND	2		30	ns

TIME DOMAIN FILTER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Delay Range	T_{TD1} = 0.184 X R_{TD} X C_{TD}, R_{TD} = 1.5 KΩ to 3.1 KΩ, CTD = 50 pF to 200 pF, V(DIN+ - DIN-) = 100 mVpp, 5 MHz, AC coupled square wave. See Figure 2	13.8		114	ns
Delay Range Accuracy	Vcc = 5.0V, Tj = 60 °C			±15	ns
	Variation with supply and temperature			12	ns
Propagation Delay	Delay = T_{D2} - T_{D1} See Fig. 2			80	ns

DATA PULSE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Pulse Width	T_{PW} = 0.184 x R_{PW} x C_{PW}, R_{PW} = 2 KΩ, C_{PW} = 150 pF. See Figure 2	30		80	ns
Skew	V(DIN = - DIN -) = 100 mVpp, 5 MHz, AC coupled square wave w/2 nsec rise & fall times			5	ns

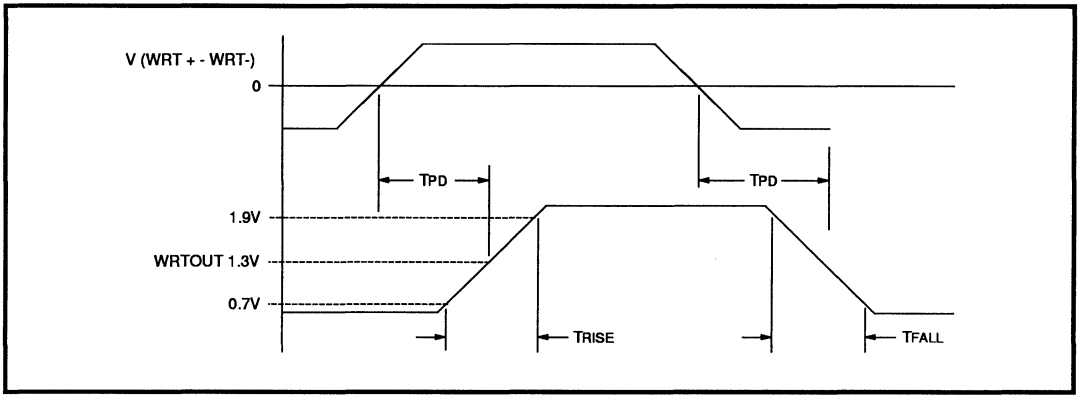


FIGURE 1: Write Mode Timing

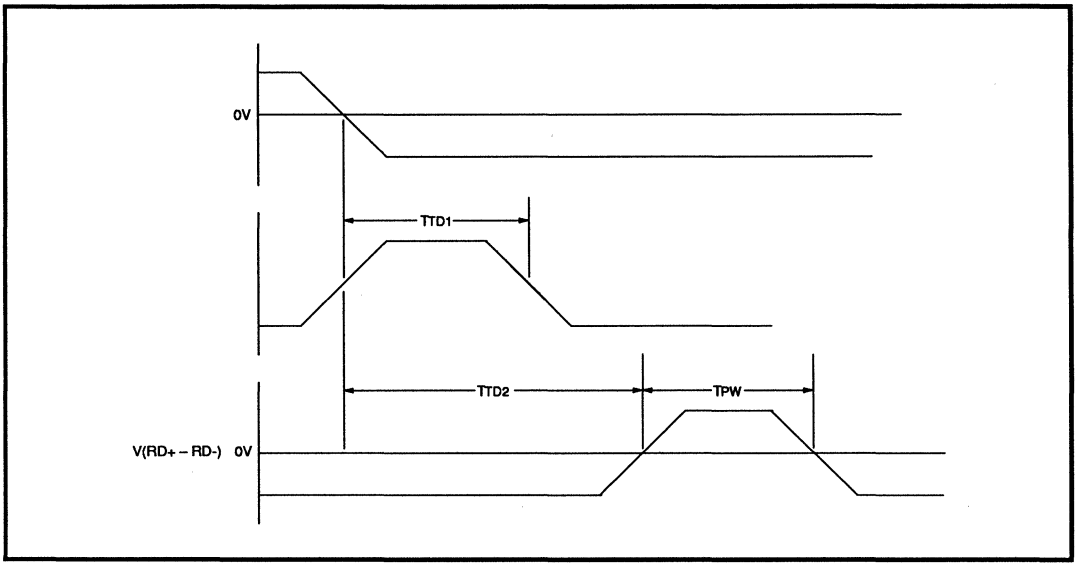


FIGURE 2: Read Mode Timing

APPLICATIONS INFORMATION

DESIGN EXAMPLE

As a design example a system using a 4-Channel SSI 32R117 Read/Write preamplifier will be used.

Assumptions
- coding scheme is MFM
- data rate is 5 Mbits/second
- Ferrite head output is 1 mVpp min. and 2 mVpp max.

The output from the SSI 32R117 is 80 mVpp to 240 mVpp. Assuming a 6 dB loss through the external low pass filter the input to the SSI 32P540 at IN+, IN- is:

40 mVpp to 120 mVpp differential voltage.

For this analysis the ± 37% tolerance on gain from IN+, IN- to OUT+, OUT- will be equally divided between the gain stage and the differentiator, so each will contribute a ±17% variance from nominal values. The objective is to get a 5 Vpp signal at OUT+, OUT- at max input and maximum frequency. For MFM the 2f frequency in a 5 Mbits/s data rate is 2.5 MHz, 1f is 1.25 MHz.

GAIN SETTING

Maximum gain from the amplifier occurs when RG = 0. So calculating for nominal gain:

$$Rx = \frac{94 \times 42}{230} = 17.17$$

$$Av_1 = \frac{628}{17 + 17.17} = \begin{array}{c}\text{19.9 nominal or} \\ \text{16.52 min. to 23.28 max.}\end{array}$$

The voltage swing at the DIF+, DIF- pins is:

120 mVpp x 22.25 = 2.79 Vpp maximum.

40 mVpp x 17.55 = 0.661 Vpp minimum.

This is within the 3.2 Vpp maximum guaranteed by this specification, so maximum gain will be used.

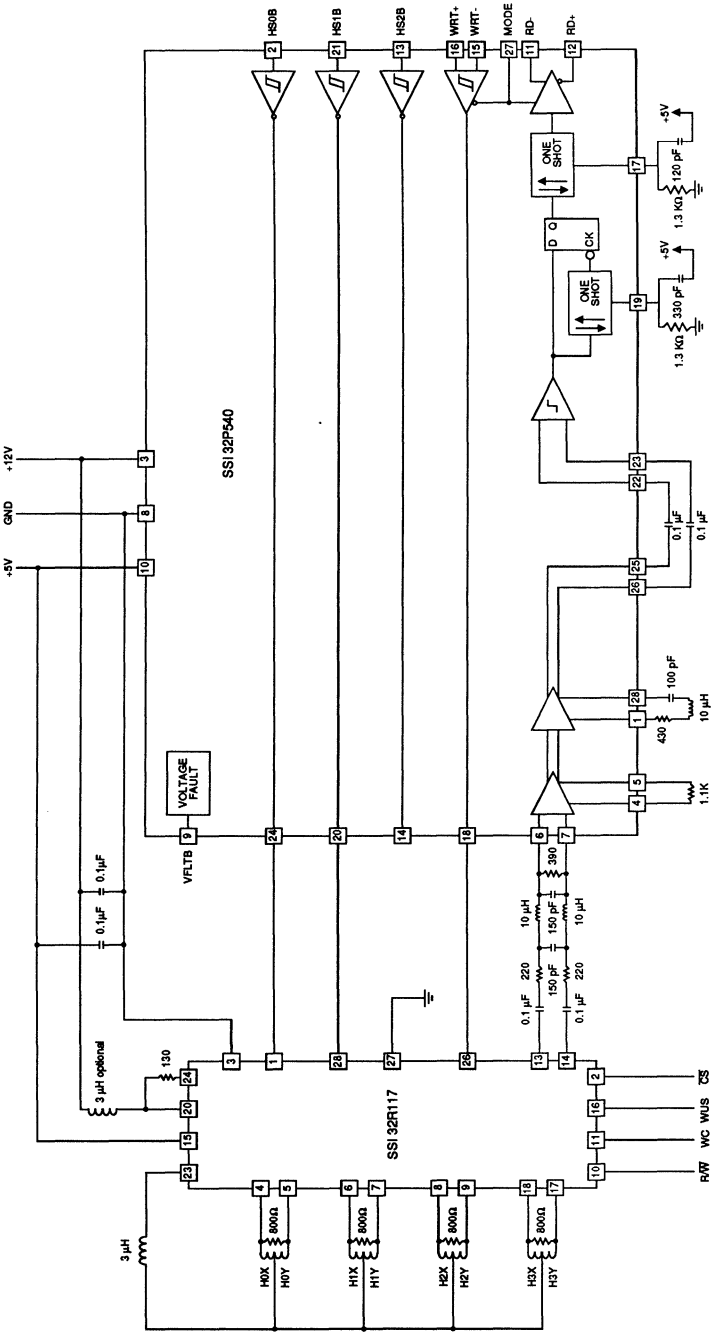


FIGURE 3: Typical Application

DIFFERENTIATOR DESIGN

The differentiator can be as simple as a capacitor or as complex as a series RLC network. In order not to violate the 5 Vpp maximum specification at OUT+, OUT- the maximum differential voltage gain is:

$$\frac{5}{2.79} = 1.79 \text{ maximum gain}$$

which is nominally a gain of 1.53

For Cex only:

$$Cex \frac{1.53}{2\pi f\sqrt{(1420)^2-(1.53 \times 46)^2}} = 68 \text{ pF}$$

check for current saturation:

Ic = Cex x Vp x $2\pi f$ must be less than 1.9 mA

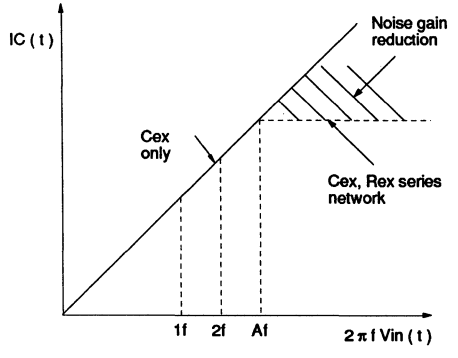
For Cex, Rex network:

The following two formulas are used:

$$1.53 = \frac{j\,1420\,Cex\,2\pi f}{j(Rex+46)\,Cex\,2\pi f+1}$$

$$Rex+46 = \frac{1}{Cex\,A\,2\pi f \text{maximum}}$$

where A is chosen for position of corner frequency to reduce high frequency noise gain from the single capacitor network. Graphically the method is as follows:



Check for current saturation using the following formula:

$$Ip = \frac{j\,Vp2\pi f\,Cex}{1+j\,2\pi f\,Cex\,(R+46)}$$

For Rex, Cex, and Lex networks, the following formulae are used:

$$\text{Gain } G = \frac{-j\,1420\,Cex\,2\pi f}{1-Lex\,Cex\,(2\pi f)^2+j\,(Rex+46)\,Cex\,2\pi f}$$

$$= \frac{1420\,Cex\,2\pi f}{\sqrt{\left[1-Lex\,Cex\,(2\pi f)^2\right]^2+\left[(Rex+46)\,Cex\,2\pi f\right]^2}}$$

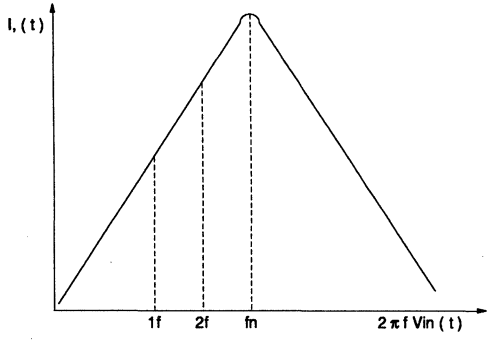
$$\left[-\frac{\pi}{2}-\tan^{-1}\left[\frac{(Rex+46)\,(Cex\,2\pi f)}{1-Lex\,Cex\,(2\pi f)^2}\right]\right]$$

$$\text{Center Frequency } f_n = \frac{1}{2\pi\sqrt{Lex\,Cex}}$$

$$\text{Damping Factor } \zeta = \frac{(Rex+46)\,Cex}{2\sqrt{Lex\,Cex}}$$

$$\text{Group Delay } \frac{dQ}{df} = \frac{2\zeta}{2\pi f_n}\left[\frac{\left(1+\frac{f}{f_n}\right)^2}{1+(4\zeta^2-2)\left(\frac{f}{f_n}\right)^2+\left(\frac{f}{f_n}\right)^4}\right]$$

This technique adds another pole to the differentiator response to attenuate high frequency noise. The center frequency damping ratio and group delay are chosen to meet system requirements. Values for the center frequency are usually from 2 to 10 fmax and the damping factor may be from 0.3 to 1. Graphically the method is as follows:



As with the previous Rex, Cex example, care must be taken to insure a 90° phase shift at the frequencies of interest (1f and 2f or 1.25 MHz and 2.5 MHz). This requirement is modified by any need to compensate for phase distortion caused by preceding signal processing.

EFFECT OF GAIN TOLERANCE

At minimum gain the 1 mVpp input at 1.25 MHz frequency has the following effects:

Using the capacitor only results with Cex = 68 pF

$$\text{Differential Gain} = \frac{1420\,Cex\,2\pi f}{\sqrt{1+(46\,Cex\,2\pi f)^2}} = 0.758 \text{ nom.}$$

Using ± 17% tolerance, min gain = 0.629

So with a 661 mVpp input the minimum voltage @OUT+, OUT- is 416 mVpp.

Thus, with all tolerances considered, a 1 mVpp to 2 mVpp input to the SSI 32R117 will result in a 5 Vpp to 416 mVpp input to the zero-crossing detector.

ONE-SHOT CONSIDERATIONS

The timing for both one shots conform to the same equation:

$t = 0.184 \times C \times R$

Setting of the time domain one-shot reflects the expected base line shouldering effect at the 1f frequency and is set accordingly. In this example the output pulse width has been set at approximately 30 nsec and the time domain filter at approximately 80 nsec.

EXTERNAL FILTER

The filter on the output of the read/write amplifier, limits the bandwidth of the input to the SSI 32P540. This reduces the noise input to the differentiator which can produce spurious zero-crossings. The design of this filter is not discussed here, but general aspects of its transfer function will be discussed.

On the outer tracks of an ST506 compatible drive using a MFM coding technique, the output pulses return to baseline or exhibit shouldering as shown in Figure 3.

This waveform has a high third harmonic content. In order to preserve this waveform the filter must not add any distortion to this harmonic. For this reason, the most common filter type used is a Bessel Filter which has a constant group delay $\left(\frac{d\Phi}{df}\right)$ or linear phase shift.

Thus for a 5 Mbit/s MFM waveform a Bessel Filter with constant group delay and a -3 dB point of 3.75 MHz is required. This is the type of filter is used in the design example.

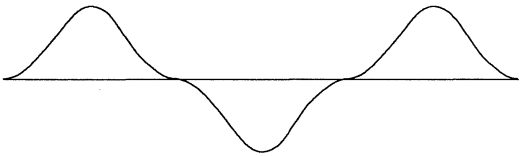


FIGURE 3: Outer Track Waveform

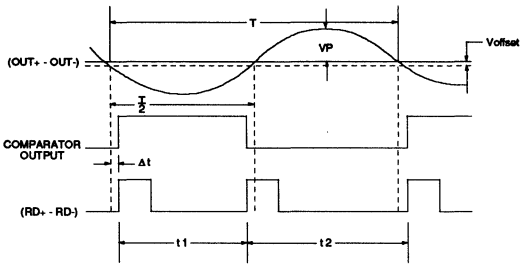


FIGURE 4:
Effect of Comparator Offset on Output Waveform

BIT SHIFT OR PULSE PAIRING

Theoretical consideration of this aspect of pulse replication relative solely to the SSI 32P540 indicates that comparator offset is the major contributing parameter. For sinusoidal inputs the offset produces a non-symmetric waveform as shown in Figure 4.

The RD+, RD- output pulses have been offset from true position (zero-crossing) by an amount Δt, that is dependent on Voffset and OUT+, OUT- amplitude.

This relationship is:

$$\Delta t = \frac{1}{w}\sin^{-1}\left(-\frac{Voff}{Vp}\right) \text{(radians)}$$

So, referring to previous results:

when OUT+, OUT- = 5 Vpp @2.5 MHz

Δt = 0.13 nsec

when OUT+, OUT- = 416 mVpp @1.25 MHz

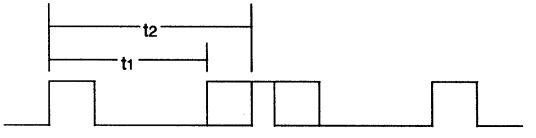
Δt = 3.1 nsec

As can be seen in Figure 4, the center pulse has been shifted from its true position by 2 Δt. So for this example the Bit Shift contributed by the SSI 32P540 is:

0.26 nsec at maximum input and frequency

6.2 nsec at minimum input and frequency

In some literature this effect is called Pulse Pairing. If the RD+, RD- waveform is displayed on an oscilloscope with the trigger holdoff adjusted to fire on succeeding pulses the following waveform is observed:



Pulse Pairing

where $t_2 - t_1$, = 4 Δt or 2 x (Bit Shift)

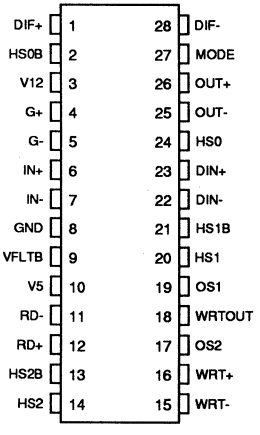
Using this technique and a sinusoidal input to DIN± of varying amplitude at 1.25 MHz and 2.5 MHz, the following results were obtained.

DIN± Input	RD± Pulse Jitter (4Δt) nsec	
Vp-p	1.25 MHz	2.5 MHz
5	0.6	1.0
3	0.6	0.8
1	0.6	0.0
.7	1.4	0.0
.3	1.6	0.5
.1	3.8	1.2
.07	5.6	2.4
.06	6.2	3.2
.05	7.0	3.5
.04	9.6	4.5
.03	11.8	6.0

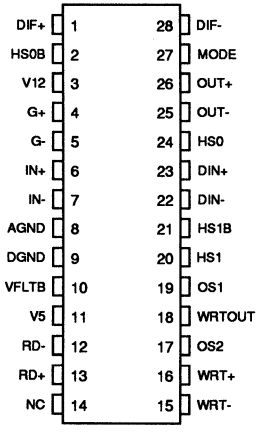
PACKAGE PIN DESIGNATIONS

(TOP VIEW)

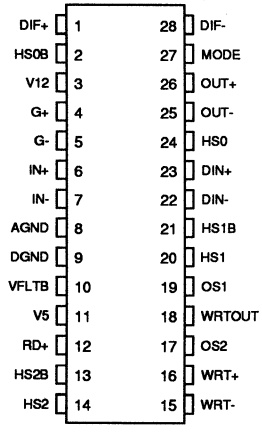
CAUTION: Use handling procedures necessary for a static sensitive component.



32P540
28-Pin PDIP



32P5402
28-Pin PDIP



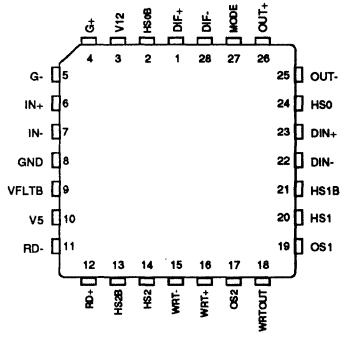
32P5403
28-Pin PDIP

PACKAGE PIN DESIGNATIONS (Continued)

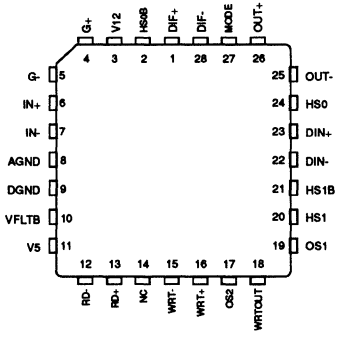
(TOP VIEW)

THERMAL CHARACTERISTICS: Ø ja

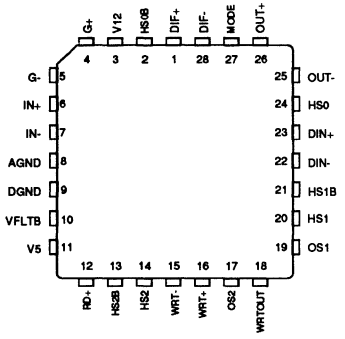
28-Pin PDIP	55°C/W
28-Pin PLCC	65°C/W



32P540
28-Pin PLCC



32P5402
28-Pin PLCC



32P5403
28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32P540 Read Data Processor		
28-Pin PDIP	SSI 32P540-CP	SSI 32P540-CP
Dual GND PDIP	SSI 32P5402-CP	SSI 32P5402-CP
28-Pin PLCC	SSI 32P540-CH	SSI 32P540-CH
Dual GND PLCC	SSI 32P540-CH	SSI 32P540-CH
Dual GND/Open Collector PDIP	SSI 32P5403-CP	SSI 32P5403-CP
Dual GND/Open Collector PLCC	SSI 32P5403-CH	SSI 32P5403-CH

silicon systems™
Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

NOTES:

SSI 32P541
Read Data Processor

August, 1988

DESCRIPTION

The SSI 32P541 is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of MFM or RLL encoded read signals. The circuit will handle data rates up to 15 Mbits/sec.

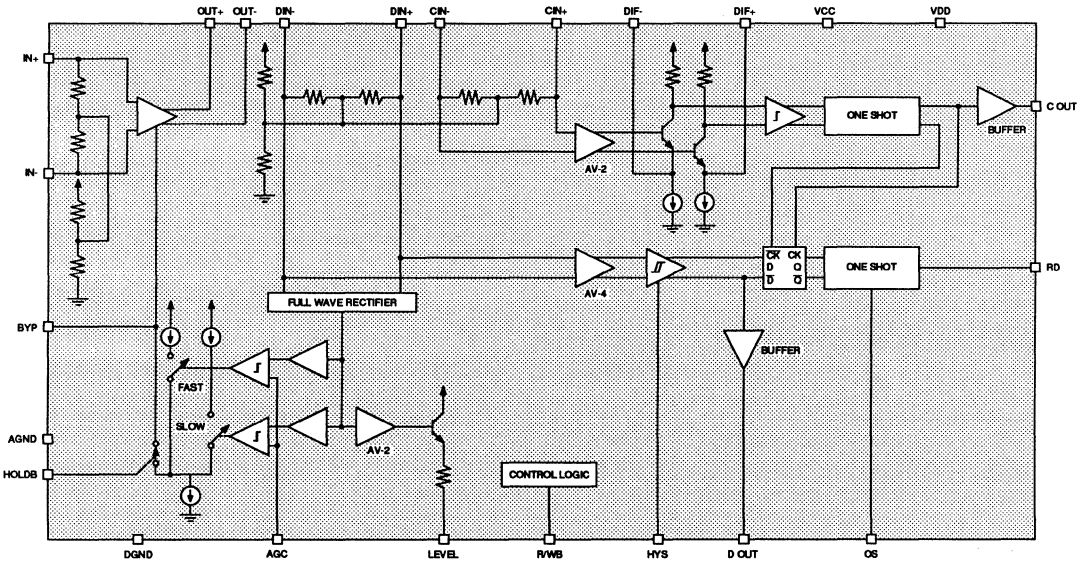
In read mode the SSI 32P541 provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

In write mode the circuitry is disabled and the AGC gain stage input impedance is switched to a lower level to allow fast setting of the input coupling capacitors during a write to read transition. The SSI 32P541 requires +5V and +12V power supplies and is available in a 24–pin DIP and 28–pin PLCC.

FEATURES

- Level qualification supports high resolution MFM and RLL encoded data retrieval
- Wide bandwidth AGC input amplifier
- Supports data rates up to 15 Mbits/sec
- Standard 12V ± 10% and 5V ± 10% supplies
- Supports embedded servo pattern decoding
- Write to read transient suppression
- Fast and slow AGC attack regions for fast transient recovery

BLOCK DIAGRAM



CIRCUIT OPERATION

READ MODE

In the read mode (R/WB input high or open) the input read signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks.

The amplified head signals are AC coupled to the IN + and IN - pins of the AGC amplifier that is gain controlled by full wave rectifying and amplifying the (DIN+ - DIN–) voltage level and comparing it to a reference level at the AGC pin. A fast attack mode, which supplies a 1.7 mA charging current for the capacitor at the BYP pin, is entered whenever the instantaneous DIN ± level is more than 125% of set level. Between 100% and 125% the slow attack mode is invoked, providing 0.18 mA of charging current. The two attack modes allow rapid AGC recovery from a write to read transition while reducing zero crossing distortion once the amplifier is in range.

The level at the AGC pin should be set such that the differential voltage level at the DIN+, DIN- pins is 1.00 Vpp at the OUT+, OUT- pins which allows for up to 6 dB loss in any external filter connected between the OUT+, OUT- outputs and the DIN+, DIN- inputs.

Gain of the AGC section is nominally

$$\frac{Av2}{Av1} = \exp - \frac{V2 - V1}{5.8 + Vt}$$

Where: Av1 and Av2 are initial and final amplifier gains. V1, V2 are initial and final voltages on the BYP pin.

Vt = (K x T)/q = 26 mV at room temperature.

One filter for both data (DIN+, DIN- input) and clock (CIN+, CIN- input) paths, or a separate filter for each path may be used. If two filters are used, care must be exercised to control time delays so that each path is timed properly. A multi-pole Bessell filter is typically used for its linear phase or constant group delay characteristics.

The filtered data path signal is fed into a hysteresis comparator that is set at a fraction of the input signal level by using an external filter/network between the LEVEL and HYS pins. Using this approach allows setting the AGC slow attack and decay times slow enough to minimize distortion of the clock path signal. This "feed-forward" technique, utilizing a fraction of the rectified data path input available at the LEVEL pin as the hysteresis threshold, is especially useful in the slow decay mode of the AGC loop. By using a short time constant for the hysteresis level, the qualification method can continue as the AGC amplifier gain is slowly ramped up. This level will also shorten the write to read transient recovery time without affecting data timing as the circuit will be properly decoding before the AGC gain has settled to its final value. The comparator output is the "D" input of a D type flip-flop. The DOUT pin provides a buffered test point for monitoring this function.

The filtered clock path signal is differentiated to transform signal peaks to zero-crossings which clock an edge-trigger circuit to provide output pulses at each zero-crossing. The pulses are used to clock the D type flip-flop. The COUT pin is a buffered test point for monitoring this function.

The differentiator function is set by an external network between the DIF+, DIF- pins. The transfer function is:

$$AV = \frac{-2000Cs}{LCs^2 + (R + 92)Cs + 1}$$

Where: C = external capacitor (20 pF to 150 pF)

L = external inductor

R = external resistor

$s = jw = j2\pi f$

During normal operation the differentiator circuit clocks the D flip-flop on every positive and negative peak of the signal input to CIN+, CIN-. The D input to the flip–flop only changes state when the signal applied to the DIN+, DIN- inputs exceeds the hysteresis comparator threshold opposite in polarity to the previous peak that exceeded the threshold.

The clocking path, then, determines signal timing and the data path determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold.

The delays from CIN+, CIN- inputs to the flip-flop clock input and from the DIN+, DIN- inputs to the flip-flop D input are well matched.

WRITE (DISABLED) MODE

In the write or disabled mode (R/WB input low) the digital circuitry is disabled and the AGC amplifier input impedance is reduced. In addition the AGC amplifier, gain is set to maximum so that the loop is in its fast attack mode when changing back to Read Mode. The lowered input impedance facilitates more rapid settling of the write to read transient by reducing the time constant of the network between the SSI 32P541 and read/write preamplifier, such as the SSI 32R510.

Internal SSI 32P541 timing is such that this settling is accomplished before the AGC loop is activated when going to read mode. Coupling capacitors should be chosen with as low a value as possible, consistent with bandwidth requirements, to allow more rapid settling.

LAYOUT CONSIDERATIONS

The SSI 32P541 is a high gain wide bandwidth device that requires care in layout. The designer should keep analog signal lines as short as possible and well balanced. Use of a ground plane is recommended along with supply bypassing and separation of the SSI 32P541 and associated circuitry grounds from other circuits on the disk drive PCB.

RW/B	HOLDB	MODE
1	1	READ - Read amp on, AGC active, Digital section active
1	0	HOLD - Read amp on, AGC gain held constant Digital section active
0	X	WRITE - AGC gain switched to maximum, Digital section inactive, common mode input resistance reduced

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VCC		5 volt power supply
VDD		12 volt power supply
AGND, DGND		Analog and Digital ground pins
R/WB	I	TTL compatible read/write control pin
IN+, IN-	I	Analog signal input pins
OUT+, OUT-	O	AGC Amplifier output pins
BYP		The AGC timing capacitor is tied between this pin and AGND
HOLDB	I	TTL compatible pin that holds the AGC gain when pulled low
AGC	I	Reference input voltage level for the AGC circuit
DIN+, DIN-	I	Analog input to the hysteresis comparator
HYS	I	Hysteresis level setting input to the hysteresis comparator
LEVEL	O	Provides rectified signal level for input to the hysteresis comparator
DOUT	O	Buffered test point for monitoring the flip-flop D input
CIN+, CIN-	I	Analog input to the differentiator
DIF+, DIF-		Pins for external differentiating network
COUT	O	Buffered test point for monitoring the clock input to the flip-flop
OS		Connection for read output pulse width setting capacitor
RD	O	TTL compatible read output

ELECTRICAL CHARACTERISTICS

Unless otherwise specified 4.5 ≤ VCC ≤ 5.5V, 10.8V ≤ VDD ≤ 13.2V, 25 °C ≤ Tj ≤ 135 °C.

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
5V Supply Voltage, VCC	6	V
12V Supply Voltage, VDD	14	V
Storage Temperature	-65 to 150	°C
Lead Temperature	260	°C
R/WB, IN+, IN-, HOLD	-0.3 to VCC + 0.3	V
RD	-0.3V to VCC + 0.3V or +12	mA
All others	-0.3 to VDD + 0.3	V

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC - VCC Supply Current	Outputs unloaded			14	mA
IDD - VDD Supply Current	Outputs unloaded			70	mA
Pd - Power Dissipation	Outputs unloaded, Tj = 135°C			730	mW

LOGIC SIGNALS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VIL - Input Low Voltage		-0.3		0.8	V
VIH - Input High Voltage		2.0			V
IIL - Input Low Current	VIL = 0.4V	0.0		-0.4	mA
IIH - Input High Current	VIH = 2.4V			100	µA
VOL - Output Low Voltage	IOL = 4.0 mA			0.4	V
VOH - Output High Voltage	IOH = -400 µA	2.4			V

MODE CONTROL

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Read to Write Transition Time				1.0	µs
Write to Read Transition Time	AGC settling not included, transition to high input resistance	1.2		3.0	µs
Read to Hold Transition Time				1.0	µs

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Common Mode Input Impedance (both sides)	R/WB pin = low		250		Ω

READ MODE

Unless otherwise specified IN+ and IN- are AC coupled, OUT+, and OUT- are loaded differentially with > 600Ω and each side is loaded with < 10 pF to GND, a 2000 pF capacitor is connected between BYP and GND, OUT+ is AC coupled to DIN+, OUT- is AC coupled to DIN-, AGC pin voltage is 2.2 VDC.

AGC AMPLIFIER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Input Resistance	V(IN+ – IN-) = 100 mVpp @ 2.5 MHz		5K		Ω
Differential Input Capacitance	V(IN+ – IN-) = 100 mVpp @ 2.5 MHz			10	pF
Common Mode Input Impedance	R/WB pin high		1.8		KΩ
(both sides)	R/WB pin low		0.25		KΩ
Minimum Gain Range	1.0 Vpp ≤ V(OUT+ – OUT-) ≤ 2.5 Vpp	4.0		83	V/V
Input Noise Voltage	Gain set to maximum			30	nV/√Hz
Bandwidth	Gain set to maximum -3 dB point	30			MHz
Maximum Output Voltage Swing	Set by AGC pin voltage	3.0			Vpp
OUT+ to OUT- Pin Current	No DC path to GND	±3.2			mA
Output Resistance		13		32	Ω
Output Capacitance				15	pF
(DIN+ – DIN-) Input Voltage Swing VS AGC Input Level	30 mVpp V(IN+ – IN-) ≤ 550 mVpp 0.5 Vpp ≤ V(DIN+ – DIN-) ≤ 1.5 Vpp	0.37		0.56	Vpp/V
(DIN+ – DIN-) Input Voltage Swing Variation	30 mVpp V(IN+ – IN-) ≤ 550 mVpp AGC Fixed, over supply & temperature			8	%
Gain Decay Time (Td)	Vin = 300 mVpp–> 150 mVpp at 2.5 MHz, Vout to 90% of final value Figure 1a		50		µs
Gain Attack time (Ta)	From Write to Read transition to Vout at 110% of final value Vin = 400 mVpp @ 2.5 MHz. Figure 1b		4		µs

AGC AMPLIFIER (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Fast AGC Capacitor Charge Current	V(DIN+ - DIN-) = 1.6V V(AGC) = 2.2V	1.3		2.0	mA
Slow AGC Capacitor Charge Current	V(DIN+ – DIN-) = 1.6V Vary V(AGC) until slow discharge	0.14		0.22	mA
Fast to Slow Attack Switchover Point	$\frac{V(DIN+-DIN-)}{V(DIN+-DIN-)\ Final}$		1.25		
AGC Capacitor Discharge Current	V(DIN+ – DIN-) = 0.0V Read Mode		4.5		µA
	Hold Mode	-0.2		+0.2	µA
CMRR (Input Referred)	V(IN+) = V(IN-) = 100 mVpp @ 5 MHz,gain at max.	40			dB
PSRR (Input Referred)	ΔVCC or ΔVDD = 100 mVpp @ 5 MHz, gain at max.	30			dB

HYSTERESIS COMPARATOR

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vpp
Differential Input Resistance	V(DIN+ – DIN-) = 100 mVpp @ 2.5 MHz	5		11	KΩ
Differential Input Capacitance	V(DIN+ – DIN-) = 100 mVpp @ 2.5 MHz			6.0	pF
Common Mode Input Impedance	(both sides)		2.0		KΩ
Comparator Offset Voltage	HYS pin at GND, ≤ 1.5 KΩ across DIN+, DIN-			10	mV
Peak Hysteresis Voltage vs HYS pin voltage (input referred)	At DIN+, DIN- pins 1V < V (HYS) < 3V	0.16		0.25	V/V
HYS Pin Input Current	1V < V (HYS) < 3V	0.0		-20	µA
Level Pin Output Voltage vs V(DIN+ – DIN-)	0.6 < | V (DIN+ – DIN-) | <1.3 Vpp, 10 KΩ from LEVEL pin to GND	1.5		2.5	V/Vpp
LEVEL Pin Max Output Current		3.0			mA
LEVEL Pin Output Resistance	I(LEVEL) = 0.5 mA		180		Ω
DOUT Pin Output Low Voltage	0.0 ≤ IOL ≤ 0.5 mA	VDD -4.0		VDD -2.8	V
DOUT Pin Output High Voltage	0.0 ≤ IOH ≤ 0.5 mA	VDD -2.5		VDD -1.8	V

ACTIVE DIFFERENTIATOR

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vpp
Differential Input Resistance	V(CIN+ – CIN-) = 100 mVpp @ 2.5 MHz	5.8		11.0	KΩ
Differential Input Capacitance	V(CIN+ – CIN-) = 100 mVpp @ 2.5 MHz			6.0	pF
Common mode Input Impedance	(both sides)		2.0		KΩ
Voltage Gain From CIN± to DIF±	R(DIF+ to DIF-) = 2 KΩ	1.7		2.2	V/V
DIF+ to DIF- Pin Current	Differentiator Impedance must be set so as not to clip signal at this current level	±1.3			mA
Comparator Offset Voltage	DIF+, DIF- are AC Coupled			10.0	mV
COUT Pin Output Low Voltage	0.0 ≤ IOH ≤ 0.5 mA		VDD -3.0		V
COUT Pin Output Pulse voltage V(high) - V(low)	0.0 ≤ IOH ≤ 0.5 mA		+0.4		V
COUT Pin Output Pulse Width	0.0 ≤ IOH ≤ 0.5 mA		30		ns

OUTPUT DATA CHARACTERISTICS (See Figure 2)
Unless otherwise specified V(CIN+ – CIN-) = V(DIN+ – DIN-) = 1.0 Vpp AC coupled since wave at 2.5 MHz differentiating network between DIF+ and DIF- is 100Ω in series with 65 pF, V (Hys) = 1.8 DC, a 60 pF capacitor is connected between OS and VCC, RD- is loaded with a 4 KΩ resistor to VCC and a 10 pF capacitor to GND.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
D-Flip-Flop Set Up Time (Td1)	Min delay from V(DIN+ DIN-) exceeding threshold to V(DIF+ – DIF-) reaching a peak	0			ns
Propagation Delay (Td3)				110	ns
Output Data Pulse Width Variation	Td5 = 670 Cos, 50 pF ≤ Cos ≤ 200 pF			±15	%
Logic Skew Td3 - Td4				3	ns
Output Rise Time	VOH = 2.4V			14	ns
Output Fall Time	VOL = 0.4V			18	ns

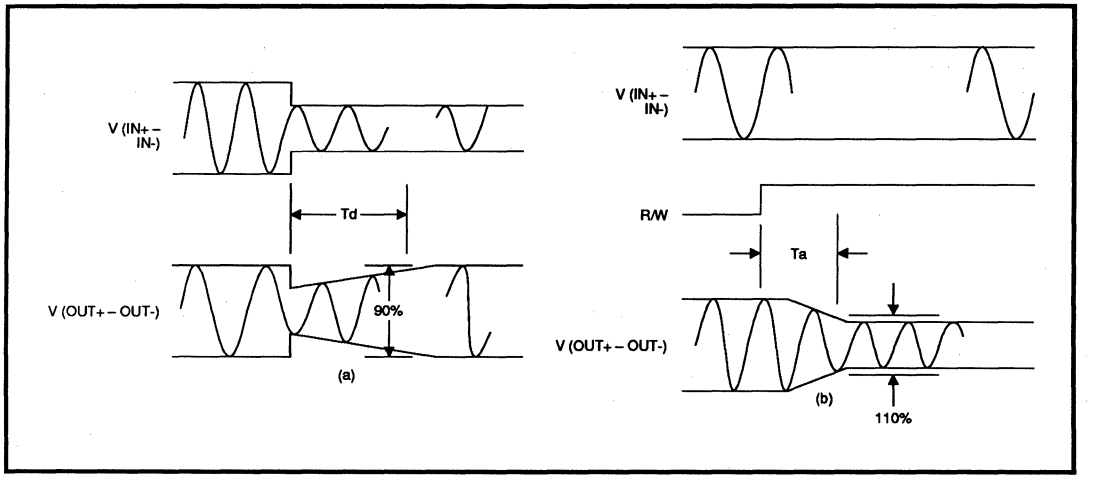


FIGURE 1(a), (b): AGC Timing Diagrams

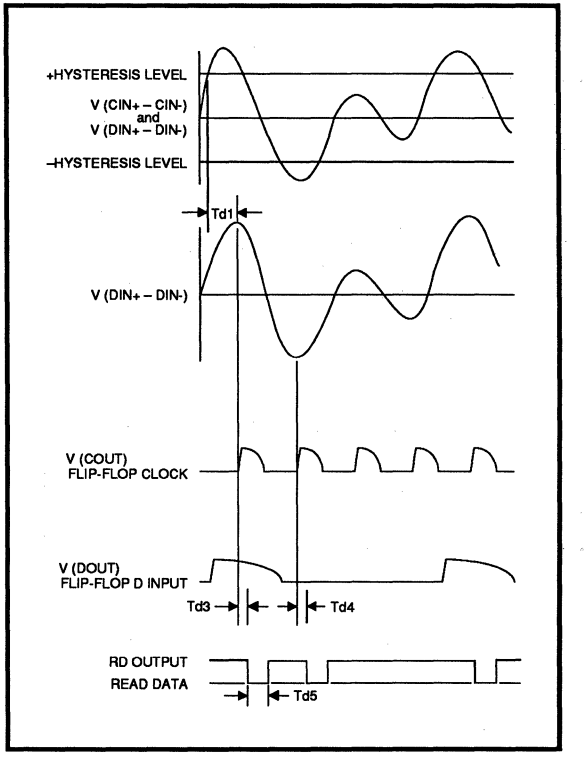
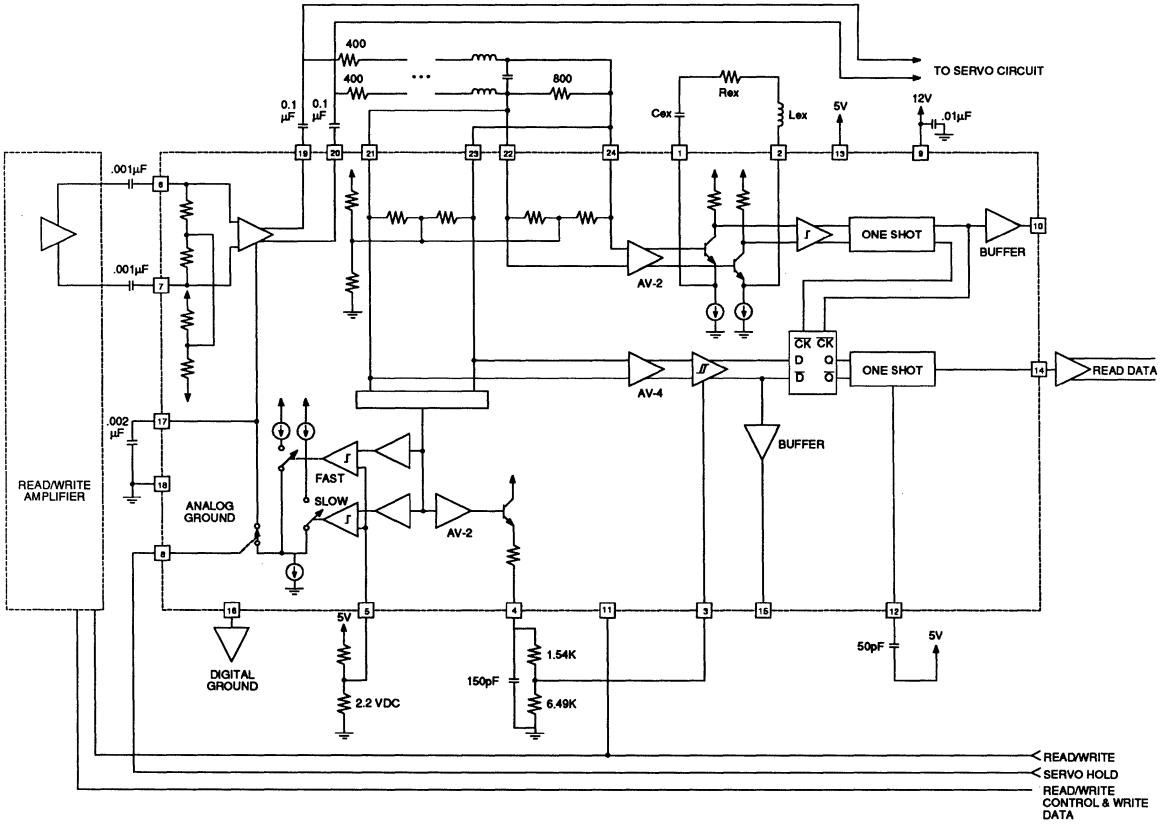


FIGURE 2: Timing Diagram



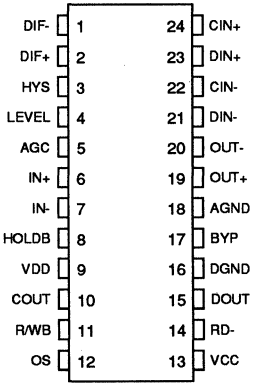
NOTE: Circuit traces for the 12V bypass capacitor and the AGC Hold Capacitor should be as short as possible with both capacitors returned to the Analog Ground Pin.
NOTE: Component values, where given, are for a 5Mbits/s system.

FIGURE 3: Typical Read/Write Electronics Set Up

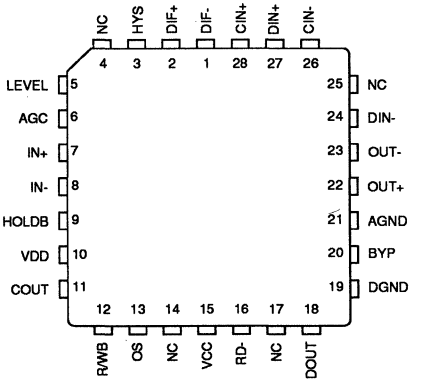
SSI 32P541
Read Data Processor

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



24-Lead PDIP, SOL



28-Lead PLCC

THERMAL CHARACTERISTICS: Ø ja

24-Lead PDIP	115°C/W
24-Lead SOL	80°C/W
28-Lead PLCC	65°C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32P541 Read Data Processor		
24-Lead PDIP	SSI 32P541-P	SSI 32P541-P
28-Lead PLCC	SSI 32P541-CH	SSI 32P541-CH
24-Lead SOL	SSI 32P541-CL	SSI 32P541-CL

silicon systems™
Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

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INNOVATORS IN INTEGRATION

SSI 32P544
Read Data Processor and Servo Demodulator

August, 1988

2

DESCRIPTION

The SSI 32P544 Read Data Processor and Servo Demodulator has a fully integrated bipolar circuit that detects and validates amplitude peaks in the output from a disk drive read amplifier, as well as detecting embedded servo information to provide position error signals used for read head positioning.

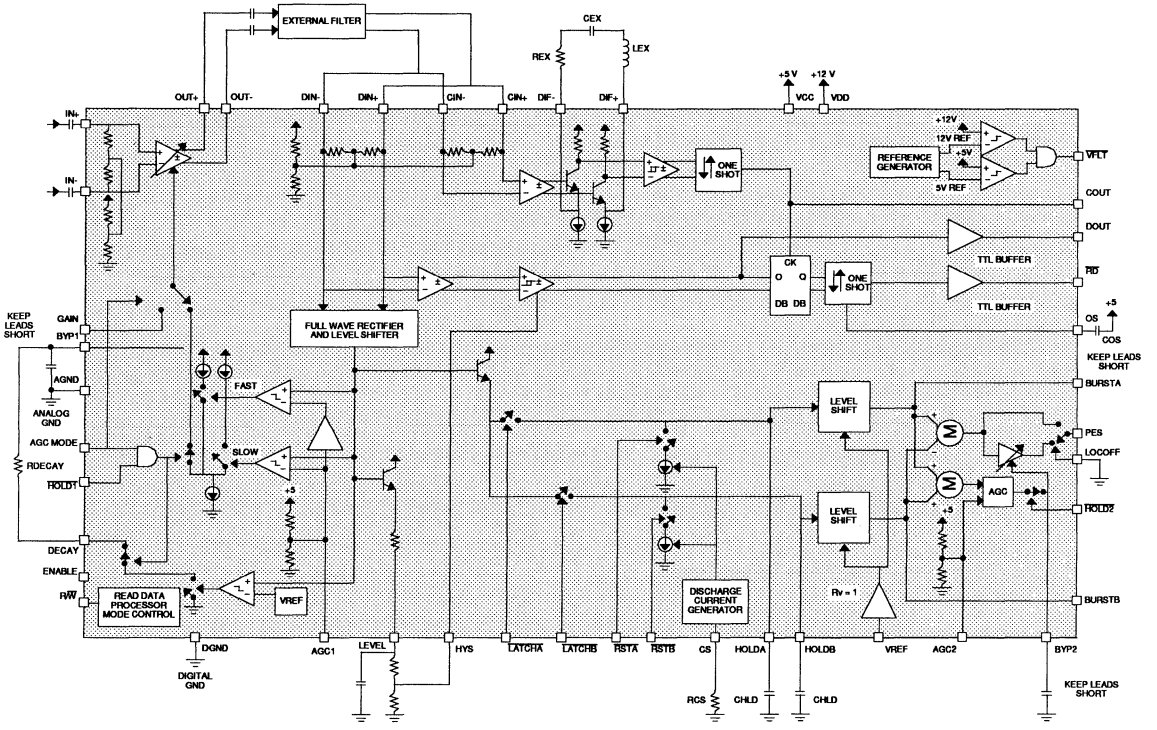
Time and amplitude qualification are used to provide a TTL compatible output that accurately duplicates the time position of input signal peaks. An AGC control loop, using a dual rate charge pump, provides a constant imput amplitude for the level qualifier. Level qualification can be implemented as a fixed threshold or a constant percentage that tracks signal amplitude that enhances qualification during AGC loop transients.

(Continued)

FEATURES

- **Wide bandwidth AGC input amplifier**
- **Level qualification supports MFM and RLL encoded data retrieval**
- **Fast and slow AGC attack and decay regions for fast transient recovery**
- **Embedded servo channel provides servo burst capture and difference circuits**
- **Local servo AGC provided based on servo burst output amplitude sum**
- **Standard ±10%, 12V and 5V supplies**
- **Write to Read transient suppression**

BLOCK DIAGRAM



DESCRIPTION (Continued)

The Servo Demodulator consists of two peak detector channels that capture rectified servo data peaks. Buffered individual channel outputs are provided along with a difference output. Servo channel gain can be controlled by an AGC signal based on maintaining the amplitude of the sum of both channels.

The circuit also provides a voltage fault flag that indicates a low voltage condition on either supply.

The SSI 32P544 requires standard +10% tolerance +5V and +12V supplies and is available in a 44-pin PLCC package.

CIRCUIT OPERATION

READ MODE

In Read Mode the SSI 32P544 is used to process either data or servo signals. In the Data Read Mode the input signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks. In the Servo Read Mode the input signal is amplified and an error signal based on amplitude comparison is made available.

DATA READ MODE

An amplified head output signal is AC coupled to the IN+ and IN- pins of the AGC amplifier. Gain control is accomplished by full wave rectifying and amplifying the [(DIN+) - (DIN-)] voltage level and comparing it to a reference voltage level at the AGC1 pin.

Two attack modes are entered depending on the instantaneous level at DIN+/-. For DIN+/- levels above 125% of desired level a fast attack mode is invoked that supplies 1.7 mA charging current to the network on the BYP1 pin. Between 125% and 100% of the desired level the circuit enters a slow attack mode and supplies 0.18 mA of charging current. This allows the AGC to rapidly recover during a write to read transition but reduces distortion once the AGC amplifier is in range.

Two decay modes are available that apply a discharge current to the BYP1 pin network when DIN+/- falls below the desired level. An internal decay current sink will supply 4.5 µA of discharge current. Also, if |(DIN+)–(DIN-)| is above 200 mVo-p a decay current, controlled by a resistor from BYP1 to DECAY, is switched in to decrease decay time. The amount of charge pulled from the AGC timing capacitor on each data pulse is:

$$Q_{DECAY} = K_1(Ton + Ts)/R_{DECAY}$$

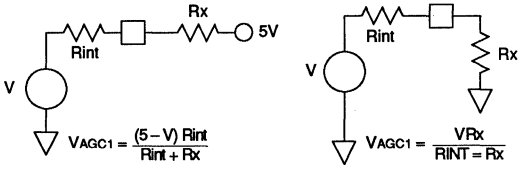
Where:

K_1 = Constant defined in spec (4.0V, typ)

Ton = Time in seconds that the data pulse at DIN+/- is greater than 200 mVo-p

Ts = Switching time in seconds (4 ns, typ)

The AGC1 pin is internally biased so that the target differential voltage input at DIN+/- is 1.0 Vp-p at nominal conditions. The AGC1 voltage can be modified by tying a resistor between AGC1 and ground or VCC. A resistor to ground decreases the voltage level while a resistor to VCC increases it. The resultant AGC1 voltage level is:



Where:

V = Voltage at AGC1 with pin open (2.2V, nom.)

Rint = AGC1 pin input impedance (6.7 KΩ, typ.)

Rx = External resistor.

The new DIN+/- input target level is nominally 0.48 Vp–p/V_{AGC1}

The AGC amplifier can swing 3.0 Vp-p at OUT+/- which allows for up to 6 dB loss in any external filter between OUT+/- and DIN+/-.

Gain of the AGC amplifier is nominally:

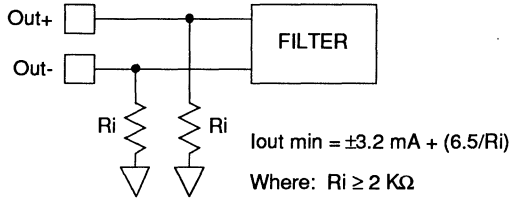
$$Av1/Av2 = e^{[6.9(V2 - V1)]}$$

Where:

Av1, Av2 are initial and final amplifier gains.

V1, V2 are initial and final voltages on the BYP1 pin.

The minimum output current from the AGC amplifier is ±3.2 mA. In cases where more current is required to drive a low impedance load the current can be increased by connecting load resistors Ri from OUT+/- to GND, as shown below.



One filter for both amplitude (DIN+/- input) and time (CIN+/- input) channels, or a separate filter for each may be used. If two filters are used, attention must be paid to time delays so that each channel is timed properly. A multi-pole Bessel filter is typically used for its linear phase or constant group delay characteristics.

In the amplitude channel the signal is sent to a hysteresis comparator. The hysteresis threshold level is set so that it will be tripped only by valid signal pulses and not by baseband noise. It can be fixed level or a fraction of the DIN+/- voltage level.

The latter approach is accomplished by using an external filter/network between the LEVEL and HYS pins. This allows setting the AGC slow attack and decay times slow enough to minimize time channel distortion and setting a shorter time constant for the hysteresis level. The LEVEL pin output is a rectified and amplified version of DIN+/-, 1.0 Vp-p at DIN+/- results in 2.0 Vo–p nominally, at the LEVEL pin. A voltage divider is used from LEVEL to ground to set the Hysteresis threshold at a percentage of the peak DIN+/- voltage. For example, if DIN+/- is 1.0 Vp-p, then using an equal valued resistor divider will result in 1.0 Vo-p at the HYS pin. This will result in a nominal ±0.210V threshold or a 42% threshold of a ±0.500V DIN+/- input. The capacitor is chosen to set an appropriate time constant. This "feed forward" technique speeds up transient recovery by allowing qualification of the input pulses while the AGC is still settling. This helps in the two critical areas of write to read and head change recovery. Some care in the selection of the hysteresis level time constant must be exercised so as to not miss pattern (resolution) induced lower amplitude signals. The output of the hysteresis comparator is the "D" input of a D type flip-flop. The DOUT pin provides a buffered TTL compatible comparator output signal for testing purposes or for use in the servo circuit if required.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from CIN+/- to the comparator input (not DIF+/-) is:

$$Av = \frac{-1000(Abuf)(Cs)}{2LCs^2 + C(R+92)s + 1}$$

Where: C, L, R are external passive components
20 pF < C < 150 pF
Abuf = Gain From CIN+/- to DIF+/-
$s = J\omega = J2\pi f$

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the CIN+/- input. The D input to the flip-flop only changes state when the DIN+/- input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched.

The D flip-flop output triggers a one-shot that sets the $\overline{RD}$ output pulse width. Width is controlled by an external capacitor from the OS pin to VCC.

SERVO READ MODE

A position error signal (PES) is generated based on the relative amplitude of two servo signals, A and B. Several methods are made available for maintaining channel gain during servo signal processing.

SERVO READ MODE (Continued)

Rectified servo signal peaks are captured on hold capacitors at the HOLDA/B pins. This is accomplished by pulling $\overline{\text{LATCHA}}$ or $\overline{\text{LATCHB}}$ low for a sample period. Addiitonally, a hold capacitor discharge current of up to 3.5 mA can be turned on by pulling $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$ low. The discharge current is determined by a resistor tied between CS and ground. Its magnitude is:

$$Ics = 2.6/(Rcs + 750) \quad A, typ.$$

Where: Rcs = resistor from CS to ground

Outputs BURSTA/B & PES are referenced to an external reference applied to the VREF pin.

As noted, several methods are used to determine channel gain in Servo Read Mode. These methods make use of the data read mode AGC loop, the servo AGC loop and external or fixed AGC loop gain. Two methods are used that control the channel gain based on maintaining the sum of A & B channel amplitudes.

In one case (see Figure 1) the BYP2 pin is connected to the GAIN pin and the servo channel gain is determined by the read channel gain as controlled by the sum of the A and B amplitudes. In this case a current is sourced/sinked to/from the capacitor on the GAIN/BYP2 pin whenever the $\overline{\text{HOLD2}}$ pin is pulled high. The current magnitude and direction is determined by:

$$Ic = K_4[(K_5 \bullet V_{AGC2}) - Va(DIN)p\text{-}p - Vb(DIN)p\text{-}p]$$

Where:

V_{AGC2} = AGC2 pin voltage

$K_4 = 270\ \mu A/Vp\text{-}p$

$K_5 = 0.41\ V/V$

Va/b(DIN)p-p = peak to peak A or B servo pattern Signal voltages at DIN+/-

The other case (see Figure 2) controls the channel by fixing the Read Data channel gain by taking $\overline{\text{HOLD1}}$ low and closing the loop about the Servo Channel AGC (LOCOFF is held low for this mode).

$\overline{\text{HOLD2}}$ is used to update the control voltage on the AGC capacitor at the BYP2 pin. This loop has a time constant defined by:

$$\text{Time Constant} = K6 \bullet C_{BYP2}$$

Where: $K_6 = 1.8$ to 7.5 KΩ

C_{BYP2} = BYP2 pin capacitor value in farads

Another method (see Figure 5) uses either a fixed voltage at the GAIN pin to determine channel gain or a gain based on preamble data amplitude. In this case no AGC methods are used that are based on servo signal amplitudes. Gain, as determined by an external voltage has been covered above. In the preamble method $\overline{\text{HOLD1}}$ is taken low during a preamble and the channel gain, determined by that necessary to maintain DIN+/- as programmed by the AGC1 voltage, is held during servo data processing.

WRITE MODE

In Write Mode the SSI 32P544 is disabled and preset for the following Read Mode. The digital circuitry is disabled, the input AGC amplifier gain is set to maximum and the AGC amplifier input impedance is reduced.

Resetting the AGC amplifier gain and input impedance shortens system Write to Read recovery times. With the AGC gain at maximum when returning to Read mode the AGC loop is in fast attack mode.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 32P544 and a read preamplifier such as the SSI 32R510A. Write to read timing is controlled to maintain the reduced impedance for 1.2 to 3.0 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

POWER DOWN MODE

A power down mode is provided to reduce power usage during the idle periods. Taking ENABLE pin low selects this mode. Recovery from this state can be slow due to the necessity of charging external capacitors.

LOW VOLTAGE FAULT DETECTION

A low voltage detection circuit monitors both supplies and pulls an open collector TTL output low whenever either supply drops below their trip point.

MODE CONTROL

The SSI 32P544 circuit mode is controlled by the ENABLE, R/$\overline{W}$, AGCMODE, $\overline{HOLD1}$, $\overline{HOLD2}$, and LOCOFF pins as shown in Table 1.

Data Read Mode

AGC active and controlled by data, Digital section active

Data Read Mode, Hold

AGC gain held constant, Digital section active. Gain will drift higher at rate determined by C_{BYP1} and Hold mode discharge current.

Servo Read Mode I (See Figures 1 & 3)

The BYP2 and GAIN pins are tied together. Read amplifier AGC control voltage developed from sum of Servo signal levels. $\overline{HOLD2}$ is toggled to update the control voltage after each Servo frame.

Servo Read Mode II (See Figures 2 & 4)

Read amplifier AGC gain held fixed ($\overline{HOLD1}$ low). Servo AGC loop activated with $\overline{HOLD2}$ toggled to update or hold gain based on a constant servo signal sum.

Servo Mode III (See Figure 5)

Read channel gain determined by voltage on GAIN pin.

Write

Read amplifier input impedance reduced. BYP1 pin voltage pulled low to select maximum amplifier gain. Digital section deactivated.

Power Down

Circuit switched to a low current disabled mode.

Note: When AGCMODE is switched to a low state the voltage at the BYP1 pin will be held subject to Hold mode discharge current induced drift. So, when returning to Data Read Mode, the channel gain will be the same as it was prior to AGCMODE switching or slightly higher.

TABLE 1: SSI 32P544 Circuit Mode Control

ENABLE	R/$\overline{W}$	AGC MODE	$\overline{HOLD1}$	$\overline{HOLD2}$	LOCOFF	READ PATH MODES
1	1	1	1	-	-	Data Read Mode
1	1	1	0	-	-	Data Read Mode Hold
1	1	0	-	1	1	Servo Read Mode I
1	1	0	-	0	1	
1	1	1	0	0	0	Servo Read Mode II
1	1	1	0	1	0	
1	1	0	-	-	-	Servo Mode III
1	0	-	-	-	-	Write
0	-	-	-	-	-	Power Down

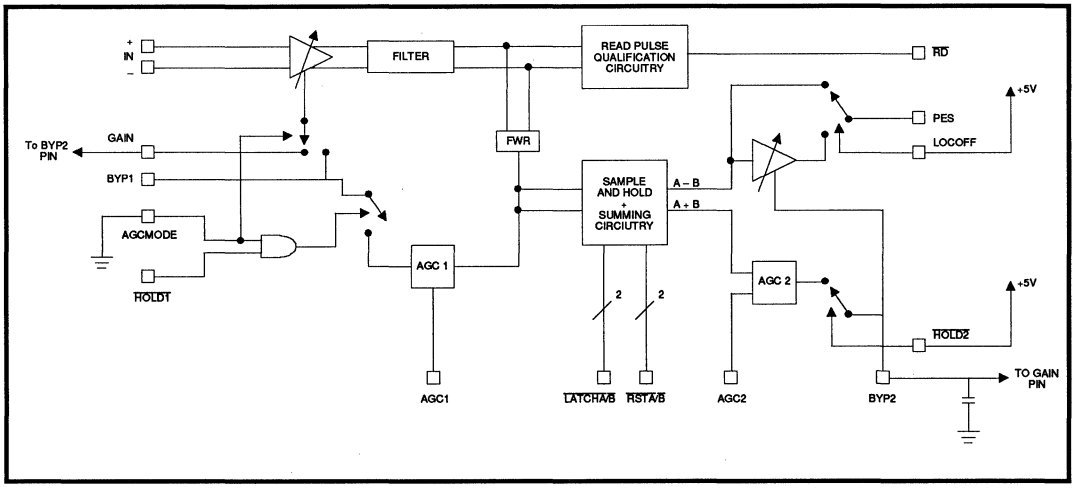


FIGURE 1: Servo Read Mode I

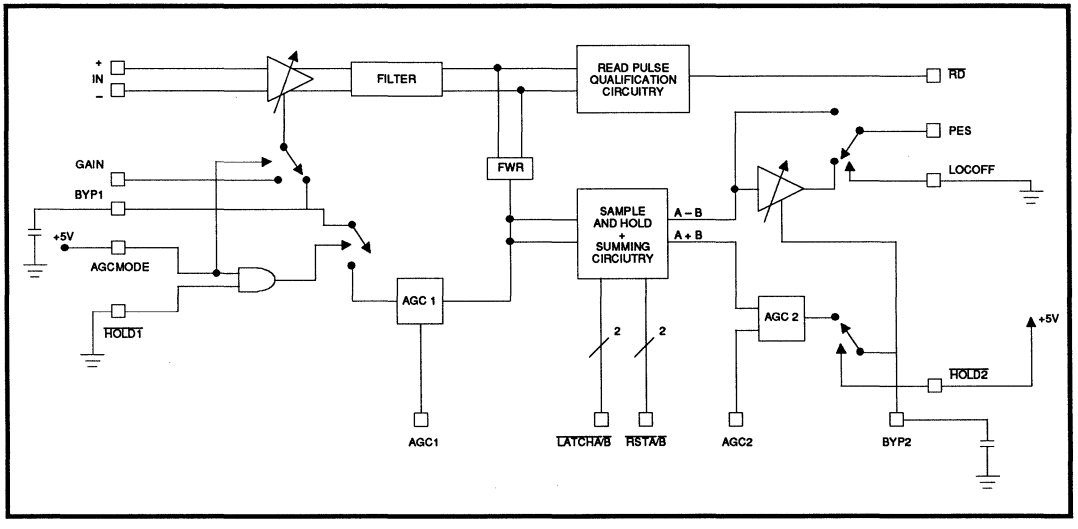


FIGURE 2: Servo Read Mode II

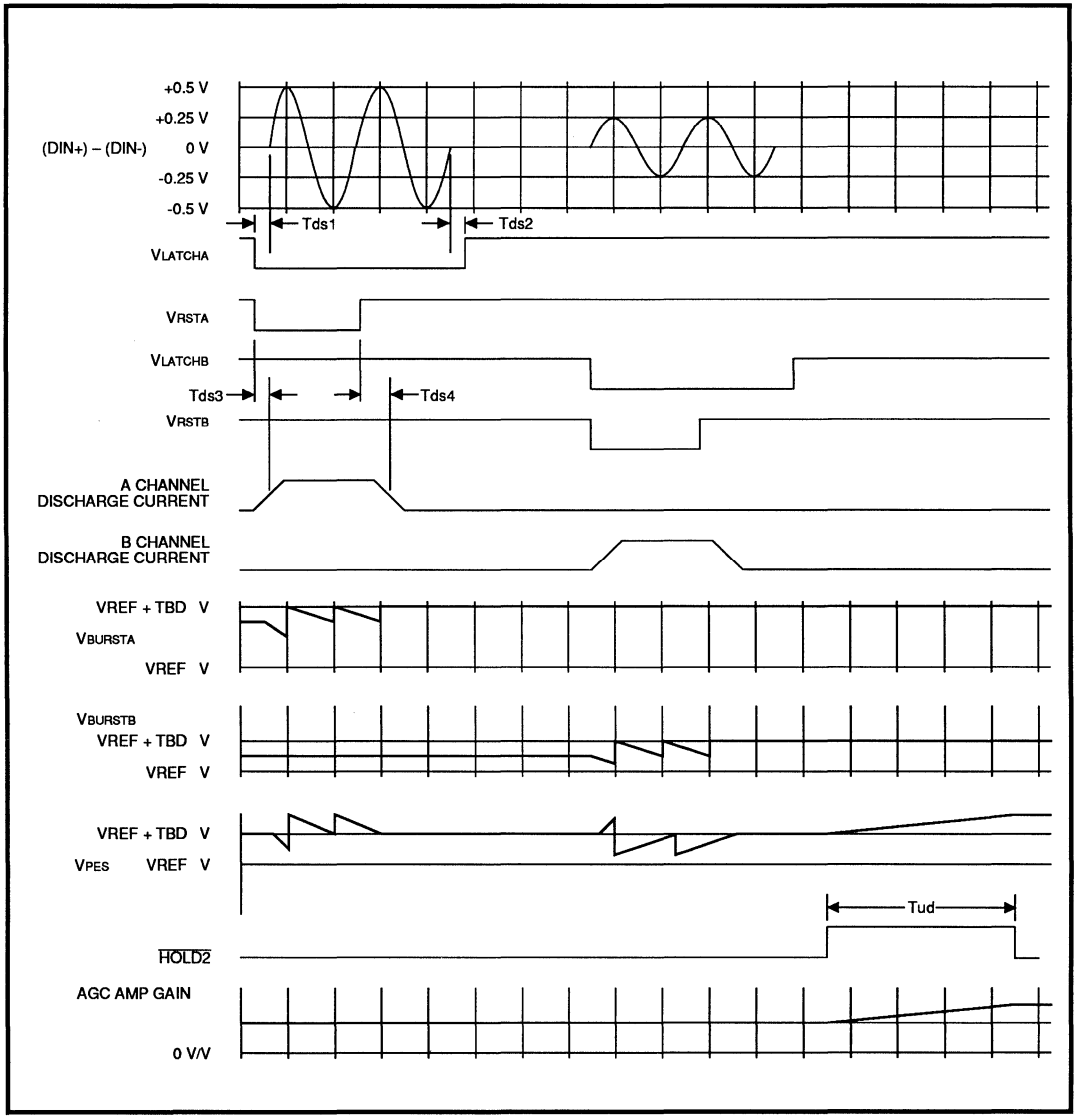


FIGURE 3: Servo Read Mode I Timing Diagram

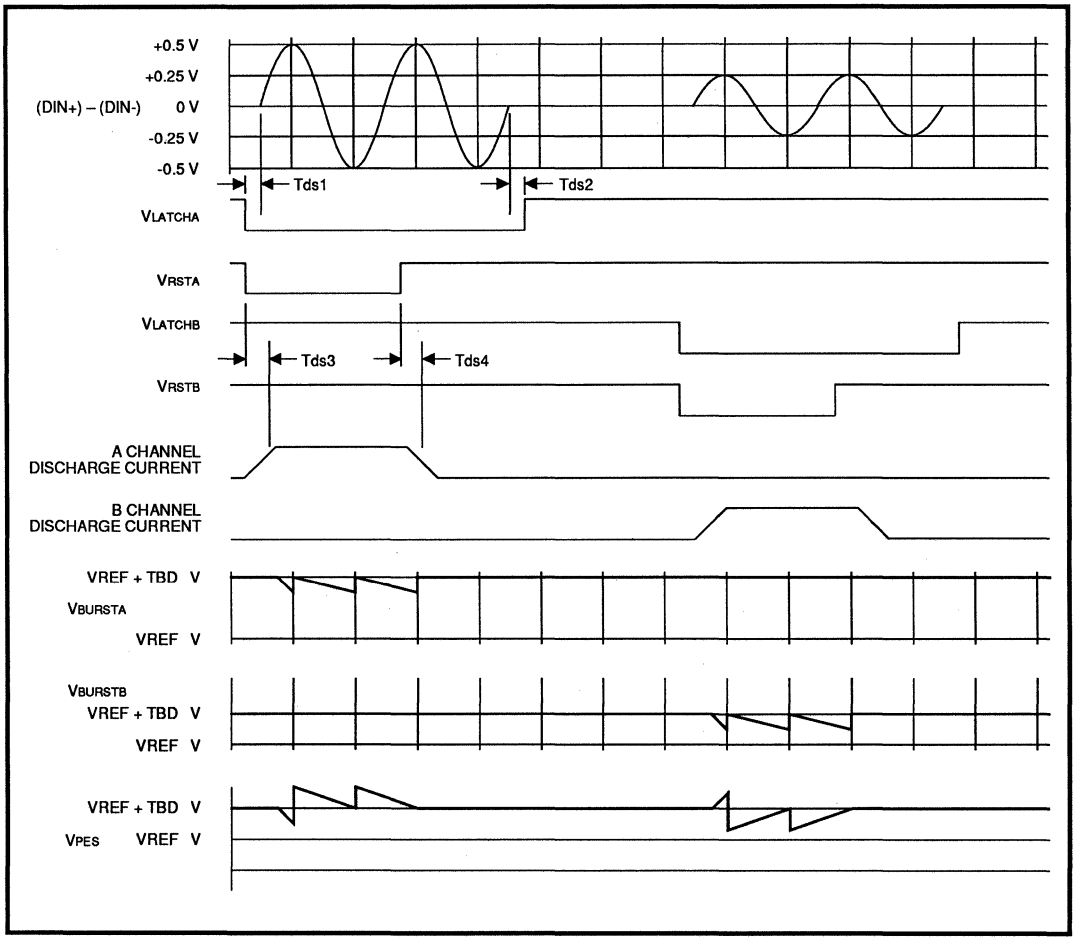


FIGURE 4: Servo Read Mode II Timing Diagram

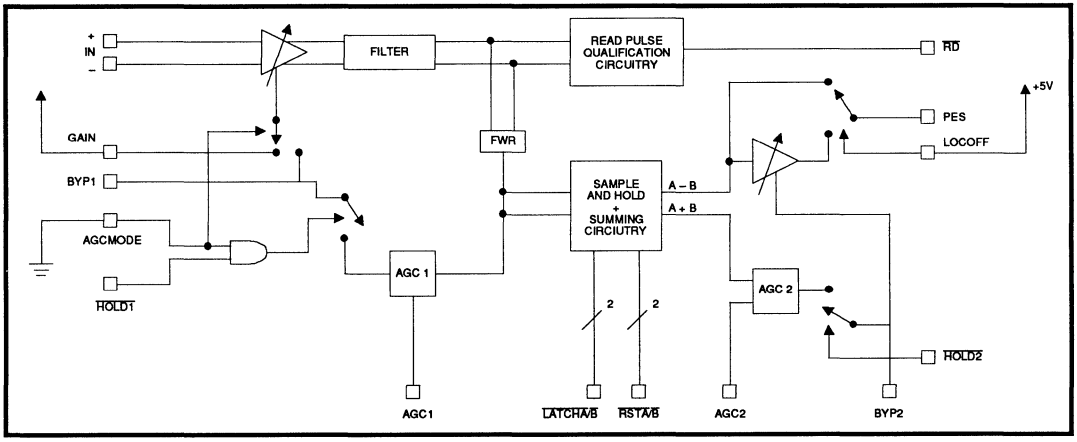


FIGURE 5: Servo Read Mode III

PIN DESCRIPTIONS

POWER SUPPLY AND CONTROL

NAME	DESCRIPTION
VCC	5 volt power supply.
VDD	12 volt power supply.
AGND, DGND	Analog and digital ground pins.
R/$\overline{W}$*	TTL compatible read/write control pin
ENABLE*	TTL compatible power up control pin. A low input selects a low power state.
$\overline{VFLT}$	Open collector output that goes low when a low power supply fault is detected.

AGC GAIN STAGE

IN+, IN-	Analog signal input pins.
OUT+, OUT-.	Read path AGC amplifier output pins.
AGC1	Reference input voltage level for the read path AGC loop.
AGCMODE*	TTL compatible pin that selects the AGC loop control input. A high selects BYP1, a low GAIN.
BYP1	An AGC timing capacitor or network is tied between this pin and AGND.
GAIN	A voltage at this pin may be used to control AGC gain.
DECAY	A resistor to control the AGC loop decay time constant may be tied between this pin and BYP1.
$\overline{HOLD1}$*	TTL compatible control pin that holds the read path AGC loop gain constant when low.

PIN DESCRIPTIONS (Continued)

DIGITAL PROCESSING STAGE

NAME	DESCRIPTION
DIN+, DIN-	Analog input to the hysteresis comparator.
CIN+, CIN	Analog input to the differentiator.
DIF+, DIF-	Pins for external differentiating network.
LEVEL	Output from full wave rectifier that may be used for input to the hysteresis-comparator.
HYS	Threshold setting input to the hysteresis-comparator.
DOUT	Buffered TTL output for monitoring the flip-flop D input. Provided for testing or servo use.
COUT	Test point for monitoring the flip-flop clock input.
OS	Connection for output pulse width setting capacitor.
$\overline{RD}$	TTL compatible read output.

SERVO BURST CAPTURE STAGE

$\overline{LATCHA}$, $\overline{LATCHB}$	TTL compatible inputs that switch channels A or B into peak acquisition mode when low.
HOLDA, HOLDB	Peak holding capacitors are tied from each of these pins to AGND.
$\overline{RSTA}$, $\overline{RSTB}$	TTL compatible inputs that enable discharge of Channel A or B hold capacitors when low.
CS	Hold capacitor discharge current magnitude is controlled by a resistor from this pin to ground.
VREF	Reference voltage input for servo outputs.
AGC2	Reference input voltage level for the servo AGC loop.
BYP2	An AGC timing capacitor or network is tied between this pin and AGND.
$\overline{HOLD2}$	TTL compatible control pin that holds the servo AGC loop gain constant when low.
BURSTA, BURSTB	Buffered hold capacitor voltage outputs.
PES	Position error signal A minus B output.
LOCOFF*	TTL compatible input to select path for PES signal.

* These inputs have internal pull-ups, so an open connection is the same as a high input.

ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING	UNIT
5V Supply Voltage, VCC	6.0	V
12V Supply Voltage, VDD	14.0	V
Pin Voltage GAIN, BYP1/2, AGC1/2 LEVEL, HYS, HOLDA/B, VREF BURSTA/B, PES, COUT, DIF+/-, OUT+/-	-0.3 to VDD + 0.3	V
Pin Voltage IN +/-, AGCMODE, $\overline{\text{HOLD1/2}}$, ENABLE, R/$\overline{\text{W}}$, $\overline{\text{LATCHA/B}}$, $\overline{\text{RSTA/B}}$, CS, LOCOFF, OS, CIN+/-, DIN+/-	-0.3 to VCC + 0.3	V
Pin Voltage RD, DOUT, DECAY, VFLTB	-0.3 to VCC + 0.3 or +12 mA	V
Storage Temperature	65 to 150	°C
Lead Temperature (Soldering 10 sec.)	260	°C

RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC Supply Voltage		4.5	5.0	5.5	V
VDD Supply Voltage		10.8	12.0	13.2	V
Tj Junction Temperature		25		145	°C

ELECTRICAL CHARACTERISTICS

POWER SUPPLY

Recommended conditions apply unless otherwise specified

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
ICC	VCC Supply Current	Outputs unloaded, ENABLE = high or open			16	mA
IDD	VDD Supply Current	Outputs unloaded, ENABLE = high or open			90	mA

POWER SUPPLY (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Pd	Power description	Tj = 145°C, ENABLE = high, Outputs unloaded			1.0	W
		ENABLE = low, Outputs unloaded			0.3	W

LOGIC SIGNALS

VIL	Input Low Voltage		-0.3		0.8	V
VIH	Input High Voltage		2.0		VCC+0.3	V
IIL	Input Low Current	VIL = 0.4V	0.0		-0.4	mA
IIH	Input Low Current	VIH = 2.4V			100	µA
VOL	Output Low Voltage	IOL = 4.0 mA			0.4	V
VOH	Output High Voltage	IOH = 400 µA	2.4			V
	Output rise time	VOH = 2.4V*			9.0	ns
	Output full time	VOL = 0.4V*			9.0	ns

*Output load is a 4K resistor to 5V and a 10 pF capacitor to DGND

MODE CONTROL

Enable to/from Disable Transition Time	Setting time of external capacitors not included ENABLE pin high to/from low			50	µs
Read to Write Transition Time	R/$\overline{W}$ pin high to low			1.0	µs
Write to Read Transition Time	R/$\overline{W}$ pin low to high AGC setting not included	1.2		3.0	µs
AGC On to/from AGC Off Transition Time	AGCMODE pin high to/from low			2.0	µs
$\overline{HOLD1}$ On to/from $\overline{HOLD2}$ Off Transition Time	$\overline{HOLD1}$ pin high to/from low			1.0	µs
$\overline{HOLD2}$ On to $\overline{HOLD2}$ Off Transition Time	$\overline{HOLD2}$ pin high to/from low			1.0	µs

WRITE MODE

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Common Mode Input Impedance	R/$\overline{W}$ pin = low		250		Ω

READ MODE

READ PATH AGC AMPLIFIER

Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN+/-. OUT+/- are loaded differentially with >600Ω, and each side is loaded with < 10 pF to AGND, and AC coupled to DIN+/-. A 2000 pF capacitor is connected between BYP1 and AGND. AGC1 pin is open. R/$\overline{W}$ is high.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Gain Range	1.0 Vp-p ≤ (OUT+) - (OUT-) ≤ 3.0 Vp-p	4		83	V/V
Output Offset Voltage	Over entire gain range	-400		+400	mV
Maximum Output Voltage Swing	Set by BYP1 pin	3.0			Vp-p
Differential Input Resistance	(IN+) - (IN-) = 100 mVp-p @ 2.5 MHz		5.0		KΩ
Differential Input Capacitance	(IN+) - (IN-) = 100 mVp-p @ 2.5 MHz			10	pF
Common Mode Input Impedance	R/$\overline{W}$ = high			1.8	KΩ
	R/$\overline{W}$ = Low			250	Ω
Input Noise Voltage	Gain set to maximum			15	nV/$\sqrt{Hz}$
Bandwidth	-3 dB bandwidth at maximum gain	30			MHz
OUT+ to OUT- Pin Current	No DC path to AGND	±3.2			mA
Output Resistance		26		64	Ω
Output Capacitance				TBD	pF
CMRR (Input Referred)	(IN+) = (IN-)= 100 mVp-p @ 5MHz, gain set to max	40			dB

READ PATH AGC AMPLIFIER (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
PSRR (Input Referred)	VDD or VCC = 100 mVp-p @ 5 MHz, gain set to max	30			dB
Externally controlled Gain Constants $AV = K_2 \cdot e^{(K_3 \cdot VGAIN)}$ V/V	K_2, AGCMODE = Low K_3, AGCMODE = Low	1.33 1.98		1.87 2.1	
Gain pin parasitic Input current	AGCMODE & $\overline{HOLD1}$ = low	0.2		+0.2	µA
(DIN+) - (DIN-) Input Swing vs. AGC1 Input	30 mVp-p ≤ (IN+) - (IN-) ≤ 550mVp-p 0.5 Vp-p ≤ (DIN+) - (DIN-) ≤ 1.5 Vp-p, AGCMODE & $\overline{HOLD1}$ = high	0.37		0.56	Vp-p/V
(DIN+) - (DIN-) Input Voltage Swing Variation	30 mVp-p ≤ (IN+) - (IN-) ≤ 550mVp-p			8.0	%
AGC1 Voltage	AGC1 open		TBD		V
AGC1 Pin Input Impedance		5.0		8.3	KΩ
Fast Decay Threshold (DIN+) - (DIN-)	AGCMODE = high		±0.2		V
Slow AGC Capacitor Discharge Current	(DIN+) - (DIN-) = 0V		4.5		µA
AGC Capacitor Leakage Current	AGCMODE = high, $\overline{HOLD1}$ = low	-0.2		+0.2	mA
Slow AGC Capacitor Charge Current	(DIN+) - (DIN-) = 0.8 VDC, vary AGC1 until slow charge begins	-0.14		-0.22	mA
Fast AGC Capacitor Charge Current	(DIN+) - (DIN-) = 0.8 VDC, V_{AGC1} = 3.0V	-1.3		-2.0	mA
Fast to Slow Attack Switchover Point	[(DIN+)-(DIN-)] - [(DIN+)-(DIN-)]$_{FINAL}$		0.25		V

READ PATH AGC AMPLIFIER (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Gain Decay Time (Td) (See Figure 6a)	(IN+) - (IN-) = 300 mVp-p to 150mVp-p @ 2.5 MHz DECAY pin open, (OUT+) - (OUT-) to 90% final value.		50		µs
Gain Attack Time (Ta) (See Figure 6b)	R/$\overline{W}$ = low to high (IN+) - (IN-) = 400 mVp-p @ 2.5 MHz, (OUT+) - (OUT-) to 110% final value		4		µs

HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC coupled, 1.0 Vp-p, 2.5 MHz sine wave. 1.8 VDC is applied to the HYS pin. ENABLE and R/$\overline{W}$ pins are high.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vp-p
Differential Input Resistance	(DIN+) - (DIN-) = 100 mVp-p @ 2.5MHz	10		16.5	KΩ
Differential Input Capacitance	(DIN+) - (DIN-) = 100 mVp-p @ 2.5MHz			4.0	pF
Common Mode Input Impedance (Both Sides)		3.0		5.0	KΩ
Level Pin Output Voltage vs. (DIN+) - (DIN-)	0.6 Vp-p < (DIN+) - (DIN-) < 1.5 Vp-p, 10K between LEVEL and AGND	1.5		2.5	V/Vp-p
Level Pin Output Impedance	I_{LEVEL} = 0.5 mA		180		
Level pin Maximum Output Current		3.0			mA
Hysteresis Voltage at DIN+/- vs. HYS Pin Voltage	1 V < HYS < 3V	0.16		0.25	V/V
HYS Pin Current	1 V < HYS < 3V	0.0		-20	µA
Comparator Offset Voltage	HYS pin at AGND ≤ 1.5 KΩ across DIN +/-			10.0	mV

ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input (CIN+) - (CIN-) is an AC-coupled, 1.0 Vp-p, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vp-p
Differential Input Resistance	(CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz	10		16.5	KΩ
Differential Input Capacitance	(CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz			4.0	pF
Common Mode Input Impedance	Both sides	3.0		5.0	KΩ
Voltage Gain From CIN+/- to DIF+/-	(DIF+ to DIF-) = 2 KΩ	1.7		2.2	V/V
DIF+ to DIF- PIn Current	Differentiator impedance must be set so as to not clip the signal for this current level	±1.3			mA
Comparator Offset Voltage	DIF+, DIF- are AC-coupled			10.0	mV
COUT Pin Output Low Voltage	0 ≤ IOL ≤ 0.5 mA		VDD-3.0		V
COUT pin Output Pulse Voltage, VHIGH - VLOW	0 ≤ IOL ≤ 0.5 mA		0.4		V
COUT pin Output Pulse Width	0 ≤ IOH ≤ 0.5 mA		30		ns

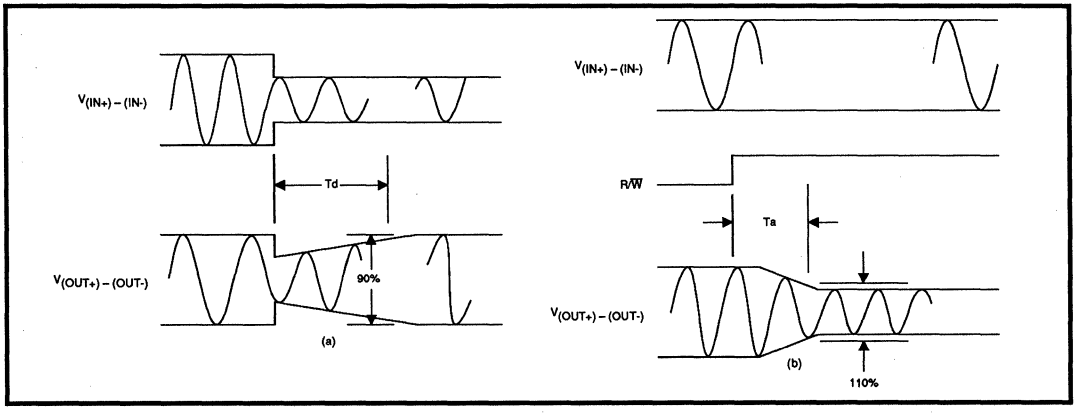


Figure 6: AGC Timing Diagram

OUTPUT DATA CHARACTERISITICS (See Figure 7)

Unless otherwise specified, recommended operating conditions apply. Inputs (CIN+) - (CIN-) and (DIN+) - (DIN-) are in-place as a coupled, 1.0Vp-p, 2.5MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-. 1.8V is applied to the HYS pin. A 60 pF capacitor is tied between OS and VCC. $\overline{RD}$ is loaded with a 4 KΩ resistor to VCC and a 10 pF capacitor to DGND. ENABLE and R/$\overline{W}$ pins are high.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Td1	D Flip-Flop Set Up Time	Minimum allowable time delay from (DIN+) - (DIN-) exceeding hysterisis point to (DIF+) - (DIF-) hitting a peak value.	0			ns
Td3	Propagation Delay				110	ns
Td5	Output Pulse Width Variation	Td5 = 900(Cos) @ V_{RD} = 1.4V 50 pF ≤ Cos ≤ 200 pF			±15	%
|Td3-Td4|	Logic Skew				1.5	ns

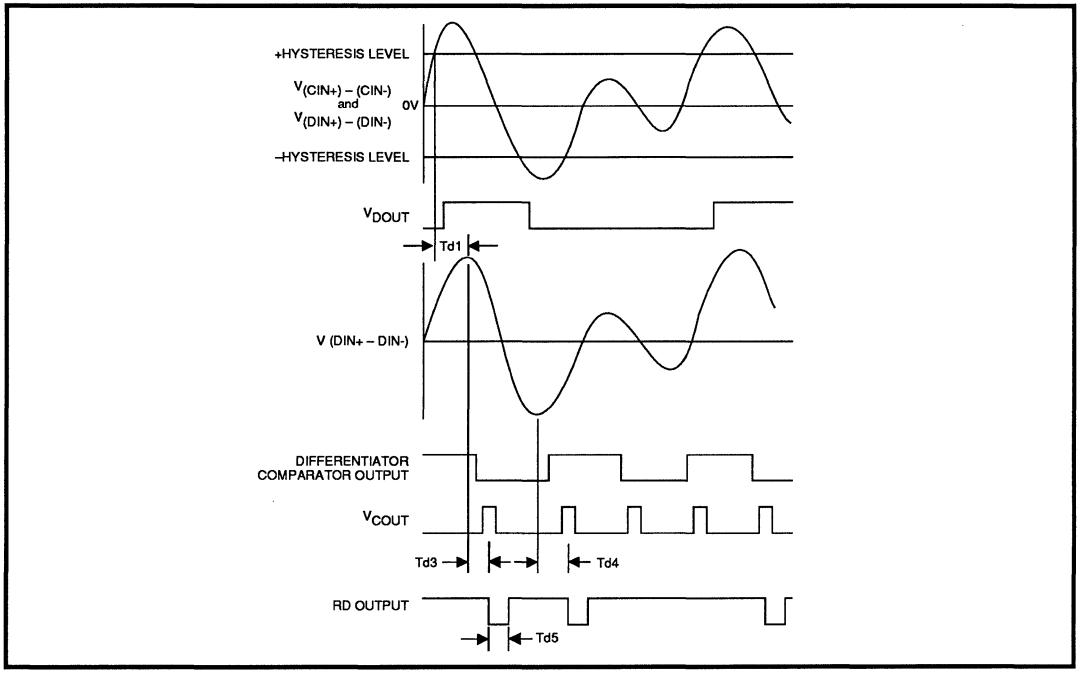


Figure 7: Read Mode Digital Section Timing Diagram

SERVO SECTION (Unless otherwise specified, recommended operating conditions apply.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VREF Voltage Range		3.9		6.0	V
AGC2 Pin Voltage	AGC2 Pin Open		3.4		V
AGC2 Pin Input Impedance		5.0		8.3	KΩ
BURSTA/B pin Output Voltage vs (DIN+) - (DIN-)	$\overline{LATCHA/B}$ = Low $\frac{V_{BURSTAB} - VREF}{(DIN+) - (DIN-)}$		1.7		V/Vp-p
BURSTA/B Output Offset Voltage V_{BURST} - VREF	$\overline{LATCHA/B}$ = Low, (DIN+) = (DIN-), RCS = 38.3 KΩ	-50		+50	mV
BURSTA - BURSTB Output Offset Match	$\overline{LATCHA/B}$ = low (DIN+) = (DIN-)	-10		+10	mV
Maximum PES Pin Output Voltage	Controlled by AGC2			5.0	Vp-p
PES Pin Output Offset Voltage	V_{PES} - VREF, (DIN+) = (DIN-) $\overline{LATCHA/B}$ = Low	-10		+10	mV
Output Resistance, BURSTA/B & PES pins				20	Ω
HOLDA/B Discharge Current Tolerance	$\overline{RSTA/B}$ = low, ICS = 2.6V/(RSC + 750Ω)		TBD		%
	$\overline{RSTA/B}$ = high, $\overline{LATCHA/B}$ = high	-0.5		+0.5	µA
Load Resistance BURSTA/B, PES pins	Resistors to VREF	10.0			KΩ
Load Capacitance BURSTA/B, PES pins				20	pF
$\overline{LATCHA/B}$ pin set up time	(Tds1 in Figures 3 & 4)	150			ns
$\overline{LATCHA/B}$ pin Hold Time	(Tds2 in Figures 3 & 4)	150			ns
Channel A/B Discharge Current Turn On time	(Tds3 in Figures 3 & 4)			150	ns

SERVO SECTION (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Channel A/B discharge Current Turn Off time	(Tds4 in Figures 3 & 4)			150	µs
BYP2 Pin Parasitic Input Current	$\overline{HOLD2}$ = Low	-9.0		+9.0	µA
K_6 loop parameter	Loop Time Constant = K_6 • CBYP2 LOCOFF = Low (Local AGC Mode)	1.8		7.5	KΩ
BYP2 Pin Charge/Discharge Current $I_C = K_4[(K_5 \bullet V_{AGC2}) - V_{A(DIN)}p\text{-}p - V_{B(DIN)}p\text{-}p]$	K_4, $\overline{HOLD2}$ = High	229	270	310	µA/Vp-p
	K_5, $\overline{HOLD2}$ = High	0.39	0.41	0.43	V/V
*PES Pin Output Voltage	LOCOFF=Low	0.6		6.0	V/Vp-p
vs. $V_{A(DIN)}p\text{-}p - V_{B(DIN)}p\text{-}p$	LOCOFF=High	1.62	1.7	1.79	V/Vp-p
V_{PES} p-p vs. V_{AGC2}	V_{PES} p-p/V_{AGC2}	1.31	1.38	1.45	Vp-p/V
	V_{PES} p-p/V_{AGC2} AGC2=Open	4.46	4.7	4.94	Vp-p
BURSTA/B Pin Output vs. V_{AGC2}	$(V_A + V_B - 2VREF)/V_{AGC2}$		0.66		V/V
	$V_A + V_B$ - 2VREF, AGC2=Open		2.3		V

*Av = (VPES - VREF)/($V_{A(DIN)}p\text{-}p - V_{B(DIN)}p\text{-}p$)

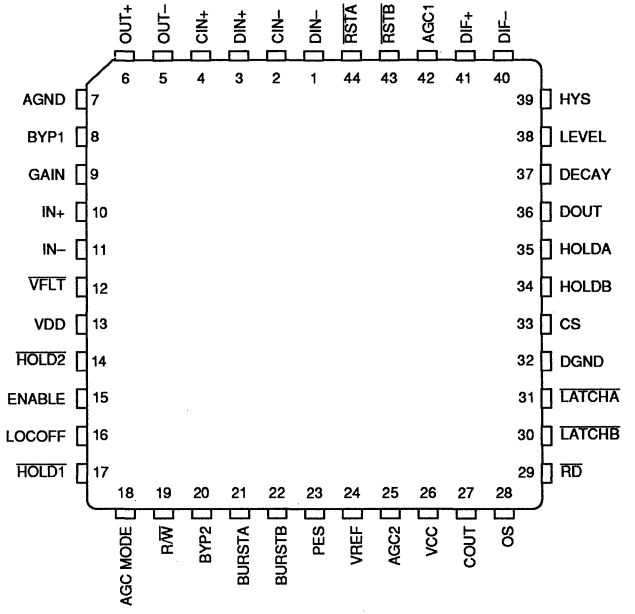
SUPPLY VOLTAGE FAULT DETECTION

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VDD Fault Threshold		9.1		10.3	V
VCC Fault Threshold		4.1		4.4	V
VOL Output Low Voltage	4.5 < VCC < 5.5V, IOL=1.6 mA			0.4	V
	1.0 < VCC < 4.5, IOL=0.5 mA			0.4	V
IOH Output High Current				25	µA

SSI 32P544
Read Data Processor and Servo Demodulator

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



44-pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32P544 - 44-pin PLCC	SSI 32P544-CH	32P544-CH

silicon systems™
Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, TWX 910-595-2809

SSI 32P546
Read Data Processor with Pulse Slimming

August, 1988

DESCRIPTION

The SSI 32P546 is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of MFM or RLL encoded read signals.

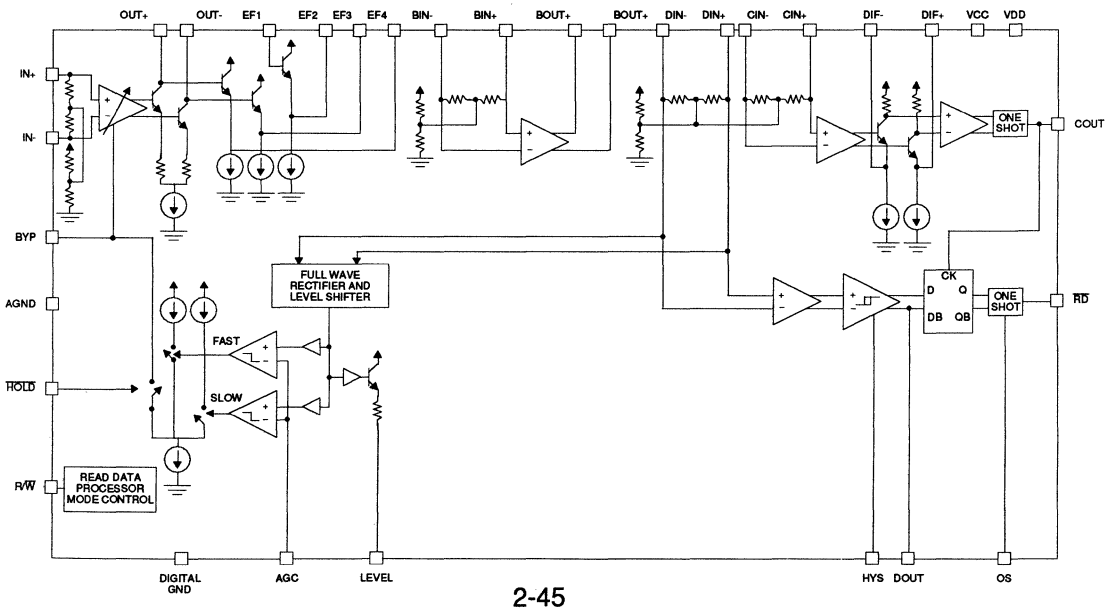
In read mode the SSI 32P546 provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. Signal processing can be further enhanced with pulse slimming techniques supported by on-chip emitter followers and buffer amplifier. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

In write mode the circuitry is disabled and the AGC gain stage input impedance is switched to a lower level to allow fast setting of the input coupling capacitors during a write to read transition. The SSI 32P546 requires +5V and +12V power supplies and is available in a 32–pin DIP.

FEATURES

- Level qualification supports high resolution MFM and RLL encoded data retrieval
- Wide bandwidth AGC input amplifier
- Supports data rates up to 15 Mbits/sec
- Standard 12V ±10% and 5V ±10% supplies
- Write to read transient suppression
- Fast and slow AGC attack regions for fast transient recovery
- Buffers and Amplifier to implement Pulse Slimming

BLOCK DIAGRAM



CIRCUIT OPERATION

READ MODE

In the read mode (R/$\overline{W}$ input high or open) the input read signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks.

The amplified head signals are AC coupled to the IN+ and IN- pins of the AGC amplifier that is gain controlled by full wave rectifying and amplifying the (DIN+ - DIN–) voltage level and comparing it to a reference level at the AGC pin. A fast attack mode, which supplies a 1.7 mA charging current for the capacitor at the BYP pin, is entered whenever the instantaneous DIN ± level is more than 125% of set level. Between 100% and 125% the slow attack mode is invoked, providing 0.18 mA of charging current. The two attack modes allow rapid AGC recovery from a write to read transition while reducing zero crossing distortion once the amplifier is in range.

The level at the AGC pin should be set such that the differential voltage level at the DIN+, DIN- pins is 1.00 Vpp at nominal conditions. The circuit can swing 2.5 Vpp at the BOUT+, BOUT- pins which allows for up to 6 dB loss in any external filter connected between the BOUT+, BOUT- outputs and the DIN+, DIN- inputs.

Gain of the AGC section is nominally

$$\frac{Av2}{Av1} = \exp -\left(\frac{V2 - V1}{5.8 + Vt}\right)$$

Where: Av1 and Av2 are initial and final amplifier gains. V1, V2 are initial and final voltages on the BYP pin.

Vt = (K x T)/q = 26 mV at room temperature.

Manipulation of pulse characteristics can be accomplished using the emitter followers and buffer amplifier (gain = 4) that follow the AGC amplifier. As illustrated in the application section, pulse slimming requires an external delay line and attenuator.

One filter for both data (DIN+, DIN- input) and clock (CIN+, CIN- input) paths, or a separate filter for each path may be used. If two filters are used, care must be exercised to control time delays so that each path is timed properly. A multi-pole Bessell filter is typically used for its linear phase or constant group delay characteristics.

The filtered data path signal is fed into a hysteresis comparator that is set at a fraction of the input signal level by using an external filter/network between the LEVEL and HYS pins. Using this approach allows setting the AGC slow attack and decay times slow enough to minimize distortion of the clock path signal. This "feed-forward" technique, utilizing a fraction of the rectified data path input available at the LEVEL pin as the hysteresis threshold, is especially useful in the slow decay mode of the AGC loop. By using a short time constant for the hysteresis level, the qualification method can continue as the AGC amplifier gain is slowly ramped up. This level will also shorten the write to read transient recovery time without affecting data timing as the circuit will be properly decoding before the AGC gain has settled to its final value. The comparator output is the "D" input of a D type flip-flop. The DOUT pin provides a buffered test point for monitoring this function.

The filtered clock path signal is differentiated to transform signal peaks to zero-crossings which clock an edge-trigger circuit to provide output pulses at each zero-crossing. The pulses are used to clock the D type flip-flop. The COUT pin is a buffered test point for monitoring this function.

The differentiator function is set by an external network between the DIF+, DIF- pins. The transfer function is:

$$AV = \frac{-2000Cs}{LCs^2 + (R + 92)\,Cs + 1}$$

Where: C = external capacitor (20 pF to 150 pF)

L = external inductor

R = external resistor

$s = jw = j2\pi f$

During normal operation the differentiator circuit clocks the D flip-flop on every positive and negative peak of the signal input to CIN+, CIN-. The D input to the flip–flop only changes state when the signal applied to the DIN+, DIN- inputs exceeds the hysteresis comparator threshold opposite in polarity to the previous peak that exceeded the threshold.

The clocking path, then, determines signal timing and the data path determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold.

The delays from CIN+, CIN- inputs to the flip-flop clock input and from the DIN+, DIN- inputs to the flip-flop D input are well matched.

WRITE (DISABLED) MODE

In the write or disabled mode (R/$\overline{W}$ input low) the digital circuitry is disabled and the AGC amplifier input impedance is reduced. In addition the AGC amplifier, gain is set to maximum so that the loop is in its fast attack mode when changing back to Read Mode. The lowered input impedance facilitates more rapid settling of the write to read transient by reducing the time constant of the network between the SSI 32P546 and read/write preamplifier, such as the SSI 32R510A.

Internal SSI 32P546 timing is such that this settling is accomplished before the AGC loop is activated when going to read mode. Coupling capacitors should be chosen with as low a value as possible, consistent with bandwidth requirements, to allow more rapid settling.

LAYOUT CONSIDERATIONS

The SSI 32P546 is a high gain wide bandwidth device that requires care in layout. The designer should keep analog signal lines as short as possible and well balanced. Use of a ground plane is recommended along with supply bypassing and separation of the SSI 32P546 and associated circuitry grounds from other circuits on the disk drive PCB.

R/$\overline{W}$	$\overline{HOLD}$	MODE
1	1	READ - Read amp on, AGC active, Digital section active
1	0	HOLD - Read amp on, AGC gain held constant Digital section active
0	X	WRITE - AGC gain switched to maximum, Digital section inactive, common mode input resistance reduced

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VCC		5 volt power supply
VDD		12 volt power supply
AGND, DGND		Analog and Digital ground pins
R/$\overline{W}$	I	TTL compatible read/write control pin
IN+, IN-	I	Analog signal input pins
OUT+, OUT-	O	AGC Amplifier output pins
BYP		The AGC timing capacitor is tied between this pin and AGND
$\overline{HOLD}$	I	TTL compatible pin that holds the AGC gain when pulled low
AGC	I	Reference input voltage level for the AGC circuit
DIN+, DIN-	I	Analog input to the hysteresis comparator
HYS	I	Hysteresis level setting input to the hysteresis comparator
LEVEL	O	Provides rectified signal level for input to the hysteresis comparator
DOUT	O	Buffered test point for monitoring the flip-flop D input

PIN DESCRIPTION (Continued)

NAME	TYPE	DESCRIPTION
CIN+, CIN-	I	Analog input to the differentiator
DIF+, DIF-		Pins for external differentiating network
COUT	O	Buffered test point for monitoring the clock input to the flip-flop
OS		Connection for read output pulse width setting capacitor
$\overline{RD}$	O	TTL compatible read output
EF1	I	Emitter follower input
EF2, 3, 4	O	Emitter follower outputs
BIN+, BIN-	I	Analog input to buffer amplifier
BOUT+, BOUT-	O	Buffer amplifier output pins

ELECTRICAL CHARACTERISTICS

Unless otherwise specified 4.5 ≤ VCC ≤ 5.5V, 10.8V ≤ VDD ≤ 13.2V, 25 °C ≤ Tj ≤ 135 °C.

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
5V Supply Voltage, VCC	6	V
12V Supply Voltage, VDD	14	V
Storage Temperature	-65 to 150	°C
Lead Temperature	260	°C
R/$\overline{W}$, IN+, IN-, $\overline{HOLD}$	-0.3 to VCC + 0.3	V
$\overline{RD}$	-0.3 to VCC + 0.3 or +12 mA	V
All others	-0.3 to VDD + 0.3	V

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC - VCC Supply Current	Outputs unloaded			14	mA
IDD - VDD Supply Current	Outputs unloaded			90	mA
Pd - Power Dissipation	Outputs unloaded, Tj = 135°C			1000	mW

LOGIC SIGNALS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VIL - Input Low Voltage		-0.3		0.8	V
VIH - Input High Voltage		2.0			V
IIL - Input Low Current	VIL = 0.4V	0.0		-0.4	mA
IIH - Input High Current	VIH = 2.4V			100	µA
VOL - Output Low Voltage	IOL = 4.0 mA			0.4	V
VOH - Output High Voltage	IOH = -400 µA	2.4			V

MODE CONTROL

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Read to Write Transition Time				1.0	µs
Write to Read Transition Time	AGC settling not included, transition to high input resistance	1.2		3.0	µs
Read to Hold Transition Time				1.0	µs

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Common Mode Input Impedance (both sides)	R/$\overline{W}$ pin = low		250		Ω

READ MODE

Unless otherwise specified IN+ and IN- are AC coupled, OUT+, and OUT- are loaded with 150Ω to VDD, a 2000 pF capacitor is connected between BYP and GND, BOUT+ is AC coupled to DIN+, BOUT- is AC coupled to DIN-, AGC pin voltage is 2.2 VDC.

AGC AMPLIFIER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Input Resistance	V(IN+ – IN-) = 100 mVpp @ 2.5 MHz		5		KΩ
Differential Input Capacitance	V(IN+ – IN-) = 100 mVpp @ 2.5 MHz			10	pF
Common Mode Input Impedance	R/$\overline{W}$ pin high		1.8		KΩ
(both sides)	R/$\overline{W}$ pin low		0.25		KΩ
Gain Range	VOUT+ = 0.75 Vpp	1.0		31	V/V
Input Noise Voltage	Gain set to maximum			30	nV/$\sqrt{Hz}$
Bandwidth	Gain set to maximum -3 dB point	30			MHz

AGC AMPLIFIER (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Maximum Output Voltage Swing	Set by BYP pin voltage Z (load) = 150Ω to VDD	0.75			Vpp
(DIN+ – DIN-) Input Voltage Swing VS AGC Input Level	30 mVpp V(IN+ – IN-) ≤ 550 mVpp, 0.5 Vpp ≤ V(DIN+ – DIN-) ≤ 1.5 Vpp	0.37		0.56	Vpp/V
(DIN+ – DIN-) Input Voltage Swing Variation	30 mVpp V(IN+ – IN-) ≤ 550 mVpp AGC Fixed, over supply & temperature			8	%
Gain Decay Time (Td)	Vin = 300 mVpp–> 150 mVpp at 2.5 MHz, Vout to 90% of final value Figure 1a		50		µs
Gain Attack time (Ta)	From Write to Read transition to Vout at 110% of final value Vin = 400 mVpp @ 2.5 MHz. Figure 1b		4		µs
Fast AGC Capacitor Charge Current	V(DIN+ - DIN-) = 1.6V V(AGC) = 2.2V	1.3		2.0	mA
Slow AGC Capacitor Charge Current	V(DIN+ – DIN-) = 1.6V Vary V(AGC) until slow discharge	0.14		0.22	mA
Fast to Slow Attack Switchover Point	$\frac{V(DIN+-DIN-)}{V(DIN+-DIN-)\ Final}$		1.25		
AGC Capacitor Discharge Current	V(DIN+ – DIN-) = 0.0V Read Mode		4.5		µA
	Hold Mode	-0.2		+0.2	µA
CMRR (Input Referred)	V(IN+) = V(IN-) = 100 mVpp @ 5 MHz,gain at max.	40			dB
PSRR (Input Referred)	VCC or VDD = 100 mVpp @ 5 MHz, gain at max.	30			dB

UNITY GAIN BUFFERS: (EMITTER FOLLOWERS)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Gain			1		V/V
Maximum Output Voltage Swing	Z(load diff.) = 1 KΩ AC Coupled	1.0			Vpp
Input Bias Current	EF1		50		µA
Output Resistance			30		Ω
Output Current		750			µA

DIFFERENTIAL BUFFER AMPLIFIER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Gain $\frac{(BOUT+ - BOUT-)}{(BIN+ - BIN-)}$	Differential Gain		4		V/V
Input Noise	Input (BIN+, BIN-) Referred			100	nV/$\sqrt{Hz}$
Bandwidth	-3 dB bandwidth	30			MHz
Maximum Output Voltage Swing	Z (load diff.) = 1 KΩ	3.0			Vpp
Differential Input Resistance	V (IN+ - IN-) = 100 mVpp, 2.5 MHz		20.0		KΩ
Differential Input Capacitance	V (IN+ - IN-) = 100 mVpp, 2.5 MHz			10.0	pF
Common Mode Input Impedance (Both Sides)			5.0		KΩ
BOUT+ to BOUT- Pin Current	No DC path from OUT+/- to GND	±2.4			mA
Output Resistance		17		43	Ω
Common mode Rejection Ratio (Input Referred)	V (BIN+) = V (BIN-) = 100 mVpp, 5 MHz	40			dB
Power Supply Rejection Ratio Input Referred	V (12) or V(5) = 100 mVpp, 5MHz	30			dB

HYSTERESIS COMPARATOR

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vpp
Differential Input Resistance	V (DIN+ – DIN-) = 100 mVpp @ 2.5 MHz	5		11	KΩ
Differential Input Capacitance	V (DIN+ – DIN-) = 100 mVpp @ 2.5 MHz			6.0	pF
Common Mode Input Impedance	(both sides)		2.0		KΩ
Comparator Offset Voltage	HYS pin at GND, ≤ 1.5 KΩ across DIN+, DIN-			10	mV
Peak Hysteresis Voltage vs HYS pin voltage (input referred)	At DIN+, DIN- pins 1V < V (HYS) < 3V	0.16		0.25	V/V
HYS Pin Input Current	1V < V (HYS) < 3V	0.0		-20	µA
Level Pin Output Voltage vs V(DIN+ – DIN-)	0.6 < | V (DIN+ – DIN-) | <1.3 Vpp 10 KΩ from LEVEL pin to GND	1.5		2.5	V/Vpp

HYSTERESIS COMPARATOR (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
LEVEL Pin Max Output Current		3.0			mA
LEVEL Pin Output Resistance	I(LEVEL) = 0.5 mA		180		Ω
DOUT Pin Output Low Voltage	0.0 ≤ IOL ≤ 0.5 mA	VDD -4.0		VDD -2.8	V
DOUT Pin Output High Voltage	0.0 ≤ IOH ≤ 0.5 mA	VDD -2.5		VDD -1.8	V

ACTIVE DIFFERENTIATOR

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range				1.5	Vpp
Differential Input Resistance	V(CIN+ – CIN-) = 100 mVpp @ 2.5 MHz	5.8		11.0	KΩ
Differential Input Capacitance	V(CIN+ – CIN-) = 100 mVpp @ 2.5 MHz			6.0	pF
Common mode Input Impedance	(both sides)		2.0		KΩ
Voltage Gain From CIN± to DIF±	R(DIF+ to DIF-) = 2 KΩ	1.7		2.2	V/V
DIF+ to DIF- Pin Current	Differentiator Impedance must be set so as not to clip signal at this current level	±1.3			mA
Comparator Offset Voltage	DIF+, DIF = AC Coupled			10.0	mV
COUT Pin Output Low Voltage	0.0 ≤ IOH ≤ 0.5 mA		VDD -3.0		V
COUT Pin Output Pulse voltage V(high) - V(low)	0.0 ≤ IOH ≤ 0.5 mA		+0.4		V
COUT Pin Output Pulse Width	0.0 ≤ IOH ≤ 0.5 mA		30		ns

OUTPUT DATA CHARACTERISTICS (See Figure 2)
Unless otherwise specified V(CIN+ – CIN-) = V(DIN+ – DIN-) = 1.0 Vpp AC coupled since wave at 2.5 MHz differentiating network between DIF+ and DIF- is 100Ω in series with 65 pF, V (Hys) = 1.8 DC, a 60 pF capacitor is connected between OS and VCC, RD- is loaded with a 4 KΩ resistor to VCC and a 10 pF capacitor to GND.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
D-Flip-Flop Set Up Time (Td1)	Min delay from V(DIN+ DIN-) exceeding threshold to V(DIF+ – DIF-) reaching a peak	0			ns
Propagation Delay (Td3)				110	ns
Output Data Pulse Width Variation	Td5 = 670 Cos, 50 pF ≤ Cos ≤ 200 pF			±15	%
Logic Skew Td3 - Td4				3	ns
Output Rise Time	VOH = 2.4V			14	ns
Output Fall Time	VOL = 0.4V			18	ns

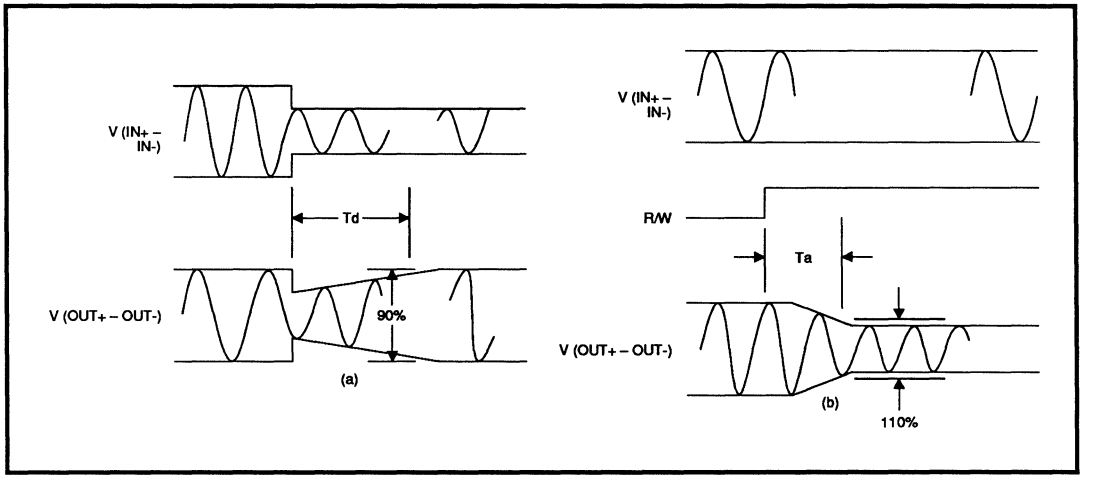


FIGURE 1(a), (b): AGC Timing Diagrams

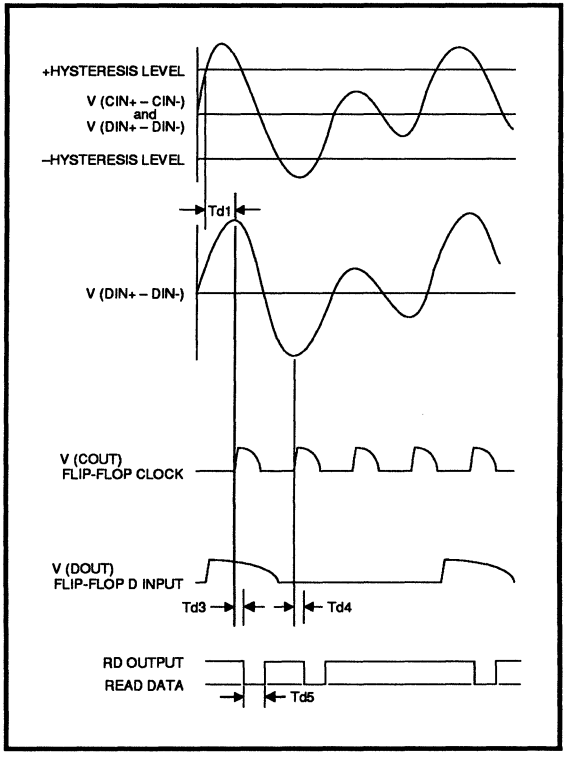
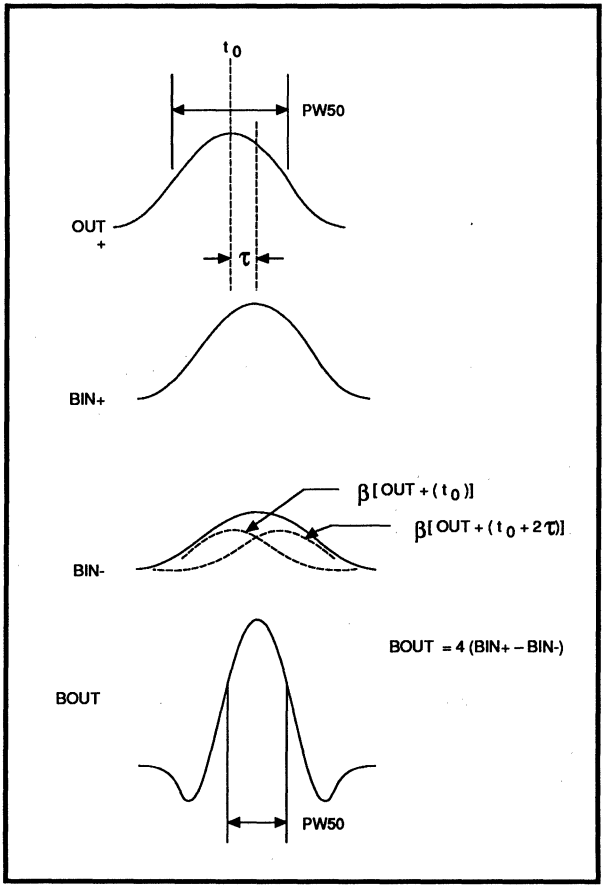


FIGURE 2: Timing Diagram

PULSE SLIMMING

The "Cosine Equalization" technique used in the SSI 32P546 relies on an external delay line to affect pulse slimming. This method is illustrated below:



The PW5O reduction is dependent on the amplitude of τ and the attenuation (β) between EF3 and BIN-.

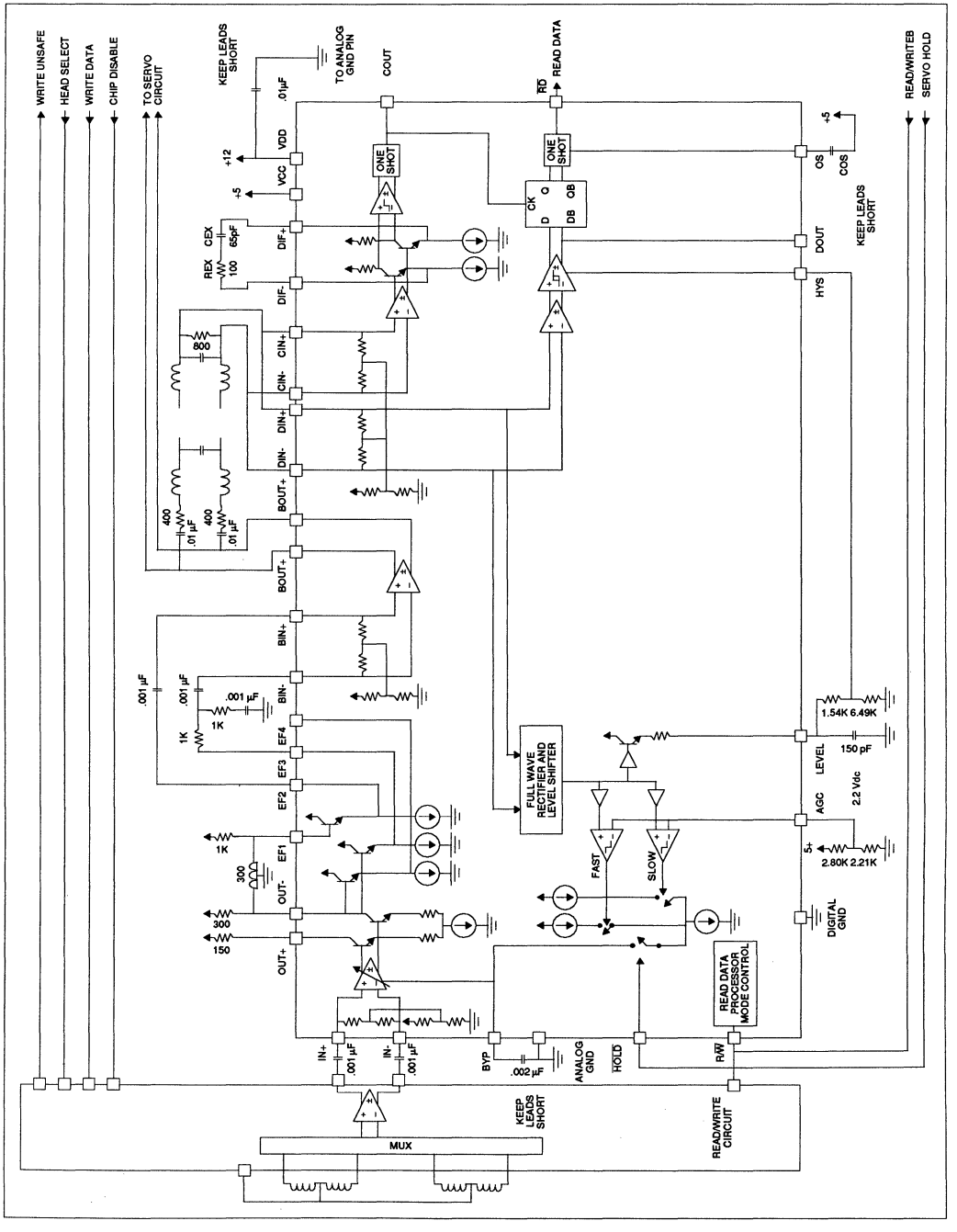
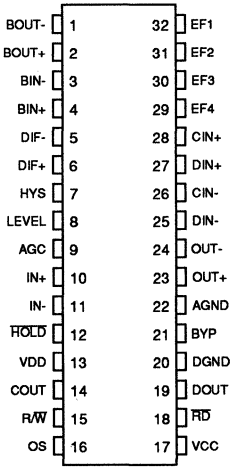


FIGURE 3: Typical Application

SSI 32P546
Read Data Processor with Pulse Slimming

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



32-Lead SOW

THERMAL CHARACTERISTICS: Ø ja

32-Lead SOW	55°C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32P546 Read Data Processor		
32-Lead SOW	SSI 32P546-CW	SSI 32P546-CW

silicon systems™
Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

Section

HDD DATA RECOVERY

3

SSI 32D531
Data Separator and Write Precompensation Device

August, 1988

DESCRIPTION

The SSI 32D531 Data Separator performs data synchronization and write precompensation of encoded data. The interface of the SSI 32D531 is optimum for use with Western Digital's WD1010/WD2010 controller family.

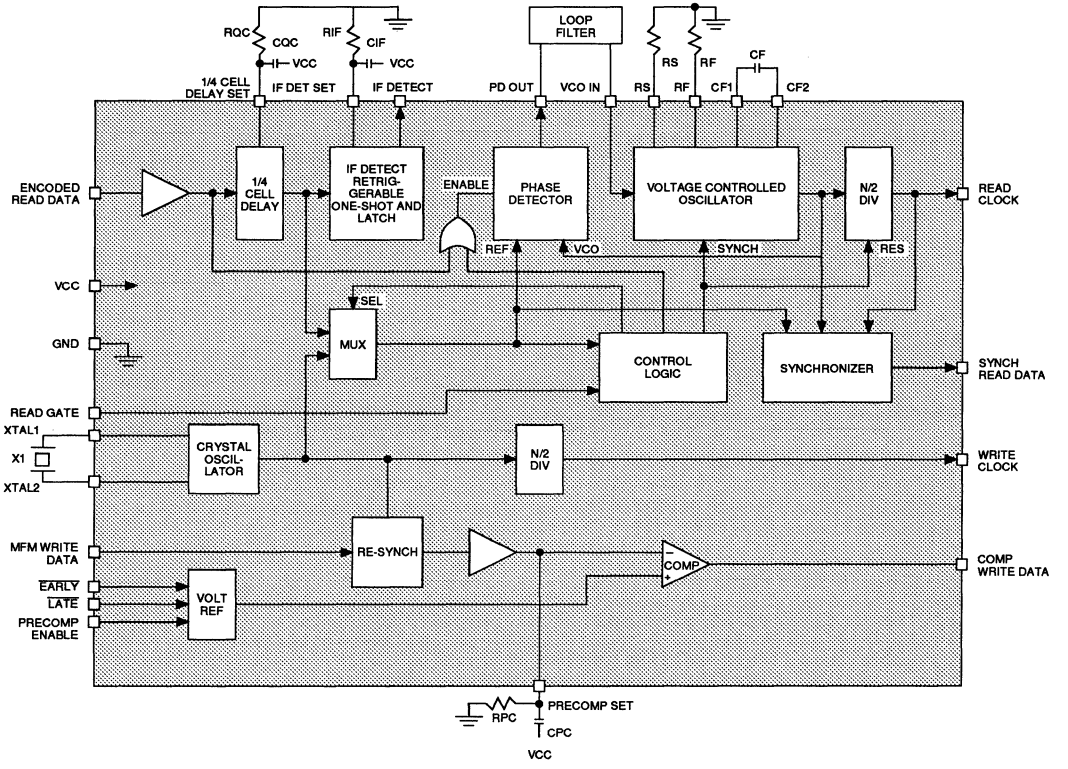
The SSI 32D531 contains a high performance Phase Locked Loop for read data synchronization, a crystal controlled reference oscillator for write data synchronization, and write precompensation circuitry. The SSI 32D531 employs an advanced bipolar technology which affords precise bit cell control without the need for external active components. The SSI 32D531 requires a single +5V power supply and is available in 24-pin DIP and 28-pin PLCC packages.

FEATURES

- **MFM & RLL Data Synchronization.**
- **Optimized for use with the WD1010/WD2010 controller family**
- **Fast acquisition Phase Locked Loop**
- **1F detection**
- **Write precompensation**
- **Write data resynchronized for reduced jitter**
- **No external delay line or varactor diode required**
- **Single +5V power supply**

3

BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

DATA SYNCHRONIZATION

Read Data synchronization is accomplished with a high performance, fast acquisition Phase Locked Loop (PLL). The input from the disk drive, ENCODED READ DATA, is phase locked with the VCO clock. The synchronized Read Data and the VCO clock divided by two are made available for external data extraction at the SYNCH READ DATA and READ CLOCK pins, respectively.

The synchronized Read Data is synchronized in a jitter-free manner such that leading edge transitions occur at the center of READ CLOCK half cycles. This is accomplished by internally decoding and re-encoding using the READ CLOCK as a reference.

When READ GATE changes state, the VCO is stopped and restarted in phase with the PLL input which can be either the internal Crystal Oscillator or ENCODED READ DATA. In this manner the lock time is reduced due to small angles of phase error. Limiting the phase error by restarting the VCO in phase with the input prevents the PLL from locking to harmonics and short lock times are assured. The correct phase of READ CLOCK is also ensured by resetting the n/2 Divider at the same time as the VCO restart.

When READ GATE is high, the 1/4 CELL DELAY allows the Phase Detector to be enabled prior to when an edge of the encoded input is to occur. This updates the PLL on a sampled basis and corrects for any phase error with each subsequent input pulse. When READ GATE is low the Phase Detector is continuously enabled and the PLL is both phase and frequency locked to the reference oscillator. By locking the VCO to the reference oscillator it is virtually at the correct frequency when the PLL is switched to track ENCODED READ DATA.

The waveforms in Figure 1 are graphic representation of the PLL alternately locking to ENCODED READ DATA and the Crystal Oscillator.

With an ENCODED READ DATA input of 5 MHz, the final DC level of the VCO waveform is constant as shown with transients occurring at each edge of the READ GATE. The amplitude and duration of the VCO locking transient is dependent on the initial phase error on switching (max is 0.5 rad.) as well as the damping factor and natural frequency of the loop. The lower two waveforms in Figure 1 are an expansion of the ENCODED READ DATA and VCO IN signals showing the effect of disabling the VCO during reference switching and the subsequent stairstep characteristic of the VCO waveform as the PLL locks to the new input.

The synchronizer circuit separates the data and clock pulses using windows derived from the VCO output. The window edges are aligned with the opposite edge from that used to phase lock the VCO. Using a VCO running at twice the expected input frequency allows accurate centering of these windows about the expected bit positions.

1F DATA DETECTION

The SSI 32D531 provides a flag, 1F DETECT, that indicates a continuous stream of "1's" or "0's."

The period of the 1F Detect Retriggerable One-Shot is set so that the sum of the 1/4 Cell Delay and the One-Shot is nominally 1-1/4 time the 2F frequency data period. This results in the 1F DETECT output remaining high during a continuous high frequency input representing a field of "1's" and "0's." External components R1F and C1F at the 1F DETECT SET pin are used to set the One-Shot delay. A Latch operates in conjunction with the One-Shot to guarantee a minimum 1F DETECT output pulse width of one data period.

WRITE PRECOMPENSATION

Write precompensation reduces the effect of intersymbol interference caused by magnetic transition proximity in the disk medial. Compensation consists of shifting written data pulses in time to counteract the read back bit shifting caused by such interaction. The severity of the intersymbol interference is a function of radial velocity of the media, the magnitude of the write pulse and the data pattern. Typically, write precompensation is enabled at the same time as the write current level is reduced.

The COMP WRITE DATA output is a re-synchronized version of the MFM WRITE DATA input that has been time shifted, if needed, to reduce intersymbol interference. Re-synchronization, to the internal crystal oscillator, is performed to minimize bit jitter in the output waveform. The magnitude of the time shift, TC, is

determined by the RC network at the PRECOMP SET pin and is applied as noted in Table 1 according to the states of $\overline{EARLY}$, $\overline{LATE}$ and PRECOMP ENABLE. Figure 2 is a further illustration of these timing relationships.

TABLE 1: Write Precompensation Truth Table

PRECOMP ENABLE	EARLY	LATE	DELAY
0	X	X	Constant
1	0	0	Illegal State
1	0	1	TN-TC
1	1	0	TN + TC
1	1	1	TN

TN = Nominal Pulse Delay
TC = Magnitude of Time Shift

REFERENCE OSCILLATOR

The crystal controlled oscillator serves as the system master clock for the write functions. Its frequency divided by two provides a WRITE CLOCK for an external MFM encoder. It is also used to re-synchronize the MFM WRITE DATA for precise timing control when writing data to the disk. A series resonant crystal should be used.

Additionally, the oscillator output is used as a standby reference for the PLL when READ GATE is low. This enables the PLL to lock rapidly to incoming data when required.

When an external system clock, is available it may be connected to XTAL1, and XTAL2 should be left open.

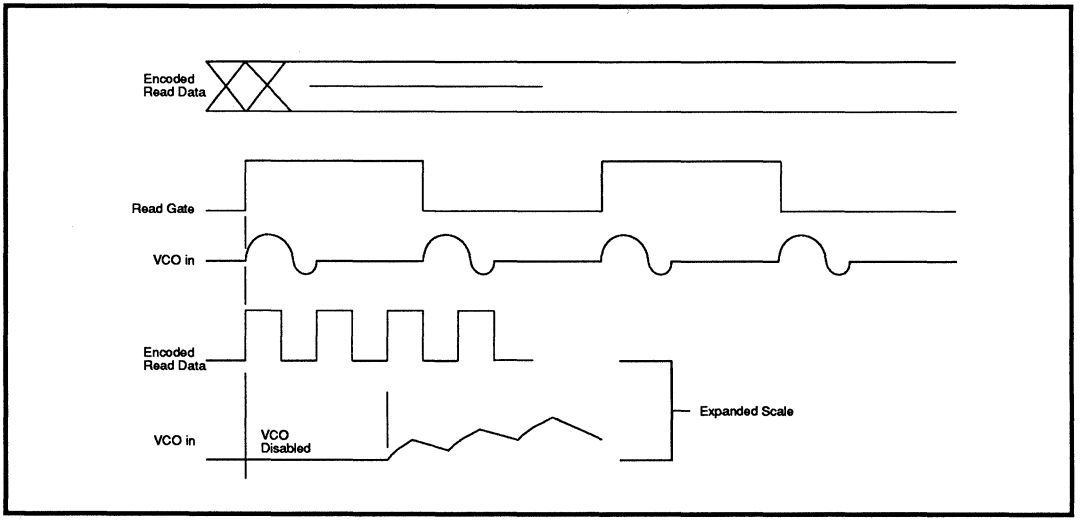


FIGURE 1 : Encoded Read Data Waveforms

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
MFM WRITE DATA	I	Write data to be resynchronized and precompensated. Synchronous with WRITE CLOCK.
PRECOMP ENABLE	I	Enables precompensation to be controlled by -EARLY or –LATE.
EARLY	I	When low causes the MFM WRITE DATA pulses to be written late.
ENCODED READ DATA	I	MFM encoded read data pulses from the read amplifier circuits.
READ GATE	I	Selects the reference input to the PLL. Selects ENCODED READ DATA when high, crystal oscillator when low.
VCC	I	+5V
GND	I	Power and signal ground connection.
WRITE CLOCK	O	Crystal-controlled reference oscillator frequency divided by two. Used by the controller to generate MFM WRITE DATA.
COMP WRITE DATA	O	Re-synchronized and precompensated write data.
READ CLOCK	O	Voltage-controlled oscillator output divided by two. SYNC READ DATA is synchronized to this signal.
SYNC READ DATA	O	Synchronized read data output. Leading-edge transitions occur at center of READ CLOCK half cycles.
1F DETECT	O	Flag used to locate strings of MFM-encoded 1's or 0's in the ENCODED READ DATA input.
XTAL1, XTAL2	I/O	Connections for oscillator crystal. If oscillator is not required, XTAL1 may be driven by TTL logic signal at twice the data rate and XTAL2 left open.
PRECOMP SET	I/O	Pin for R-C network to control write precompensation early and late times
1F DETECT SET	I/O	Pin for R-C network to control the 1F detect period. Component values are dependent on the minimum data period that will keep 1F DETECT high.
1/4 CELL DELAY SET	I/O	Pin for R-C network to control the 1/4 CELL DELAY. This allows the Phase Detector to be enabled 1/4 of the data period prior to receiving an MFM data input.
CF1,CF2	I/O	Pins for the capacitor used in conjunction with RF and RS to set the VCO center frequency.
RF, RS	I/O	Pin for resistors used in conjunction with capacitor to set the VCO center frequency.
PD OUT	I/O	Output of phase detector, input to loop filter.
VCO IN	I/O	Control input of the VCO, for connection of the loop filter output.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
Storage Temperature	-65 to +150	°C
Ambient Operating Temperature, TA	0 to +70	°C
Junction Operating Temperature	0 to +130	°C
Supply Voltage, VCC	-0.5 to +7.0	Vdc
Voltage Applied to Logic Inputs	-0.5 Vdc to VCC +0.5	Vdc
Maximum Power Dissipation	800	mW

DC CHARACTERISTICS

Unless otherwise specified 4.75 < VCC < 5.25V, Ta = 0 to 50 °C, RPC = 3.3K, CPC = 24 pF, R1F = 16K, C1F = 120 pF, RQC = 8.2K, CQC = 56 pF, RF = 499, RS = 499, CF = 56 pF, and X1 = 8 MHz to 10.5 MHz crystal conforming to military type HC19A/U.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
High Level Input Voltage, VIH		2.0			V
Low Level Input Voltage, VIL				0.8	V
High Level Input Current, IIH	VIH = 2.7V			20	µA
Low Level Input Current IIL	VIL = 0.4V			-0.36	mA
High Level Output Voltage, VOH					
Comp Write Data	IOH = -400 µA	2.7			V
All Others	IOH = -50 µA	4.6			V
Low Level Output Voltage, VOL					
Comp Write Data	IOL = 4 mA			0.4	V
All Others	IOL = 1 mA			0.4	
Power Supply Current, Icc	All Outputs Open			100	mA

DATA DETECTION CHARACTERISTICS (SEE FIGURE 1)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ENCODED READ DATA Pulse Width, TERD		10		$\frac{TRCF}{2}+10$	ns
ENCODED READ DATA Positive Transition Time, TERDPT	0.8V to 2.0V, CL = 15 pF			20	ns
READ CLOCK Repetition Period Range, TRCF		0.85 TWCF		1.15 TWCF	ns

DATA DETECTION CHARACTERISTICS (SEE FIGURE 1)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
READ CLOCK Pulse Width, TRC		$\frac{TRCF}{2}-1$		$\frac{TRCF}{2}+7$	ns
READ CLOCK Positive Transition Time, TRCPT	0.9V to 4.2V, CL = 15 pF			15	ns
READ CLOCK Negative Transition Time, TRCNT	4.2V to 0.9V, CL = 15 pF			10	ns
SYNC READ DATA TSRDD1		0		TRCF -20	ns
Delay TSRDD2		0		TRCF-TRC -20	ns
SYNC READ DATA Pulse width, TSRD1,2		19		$\frac{TRCF}{2}$	ns
SYNC READ DATA Positive Transition Time, TSRDPT	0.9V to 4.2V, CL = 15 pF			15	ns
1F DETECT Delay T1FD Accuracy	TD = 0.086 (RIF) (CIF + 7pF) +TQC,C1F = 100 pF to 180 pF	0.9TD		1.1TD	sec
1/4 CELL DELAY, TQC Accuracy	TDQ = 0.095 (RQC)(CQC + 7pF) CQC = 43 pF to 82 pF	0.85 TDQ		1.15 TDQ	sec
PHASE LOCKED LOOP CHARACTERISTICS					
VCO Period Accuracy, TVCO	Oscillator period, TO = 1.7(RF + RS) CF, CF = 20 pF to 82 pF, RF = RS = 499Ω	0.9TO		1.1TO	sec
VCO Frequency Range	VCO IN = 0.85V to Vcc -0.85V, Vcc = 5.0V	±20		±30	%
Phase Detector Gain, KD	w/respect to 5 Mbit/sec data rate, Vcc = 5.0V	30		45	µA/rad
VCO Control Gain, KVCO	Wo = Vco radian center frequency V=VCO IN voltage change VCO IN = 0.85V to Vcc -0.85V	$\frac{0.12Wo}{V}$		$\frac{0.18Wo}{V}$	rad/ (sec.V)
VCO Phase Preset Error				±0.5	rad
Data Detection Window Centering Accuracy		±0.02 TRCF ±4			ns
Number of Read Clock Period Delay From ENC RD DATA Input to SYNC RD DATA Output				2	
Number of READ CLOCK periods that VCO may be disabled during reference switching				3	

WRITE PRECOMPENSATION SWITCHING CHARACTERISTICS (SEE FIGURE 2)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
WRITE CLOCK Repetition Period, TWCF	Controlled by X1 Freq.	190		250	ns
WRITE CLOCK Pulse, Width, TWC		$\frac{TWCF}{2}-15$		$\frac{TWCF}{2}+10$	ns
WRITE CLOCK Positive Transition Time, TWCPT	0.9V to 4.2V, CL = 15 pF			15	ns
WRITE CLOCK Negative Transition Time, TWCNT	4.2V to 0.9V, CL = 15 pF			10	ns
MFM WRITE DATA Set Up Time, TWDS1,2		15			ns
MFM WRITE DATA Hold Time, TWDH1,2		10			ns
MFM WRITE DATA Release Time, TWDR1, 2		15			ns
$\overline{\text{EARLY}}$ or $\overline{\text{LATE}}$ Set Up Time TELS1,2		125			ns
$\overline{\text{EARLY}}$ or $\overline{\text{LATE}}$ Hold Time TELH1,2		10			ns
COMPENSATED WRITE DATA, Pulse Width, TCWD	CL = 15 pF	40		$\frac{TWCF}{2}$	ns
COMPENSATED WRITE DATA "Nom" Pulse Width Delay, TN				$\frac{TWCF}{2}$	ns
COMPENSATION WRITE DATA Compensation Accuracy, TE, TL	TC = 0.15 (RCP) (CPC) CPC = 15 pF to 36 pF	0.8TC		1.2TC	sec
COMPENSATED WRITE DATA Positive Transition Time, TCWDPT	0.8V to 2.0V, CL = 15 pF			10	ns

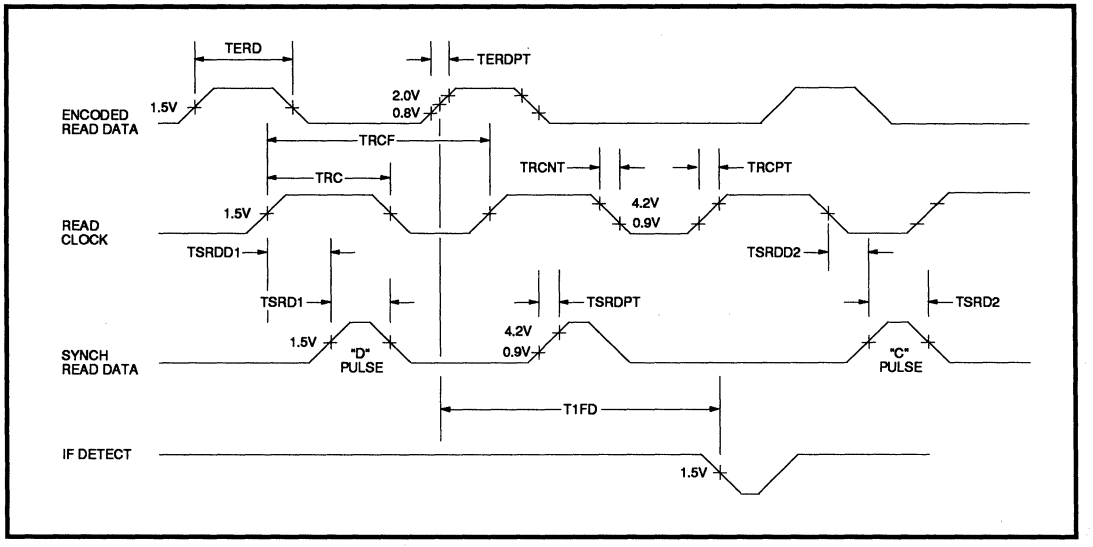


FIGURE 2: Data Detection and Synchronizing Waveforms

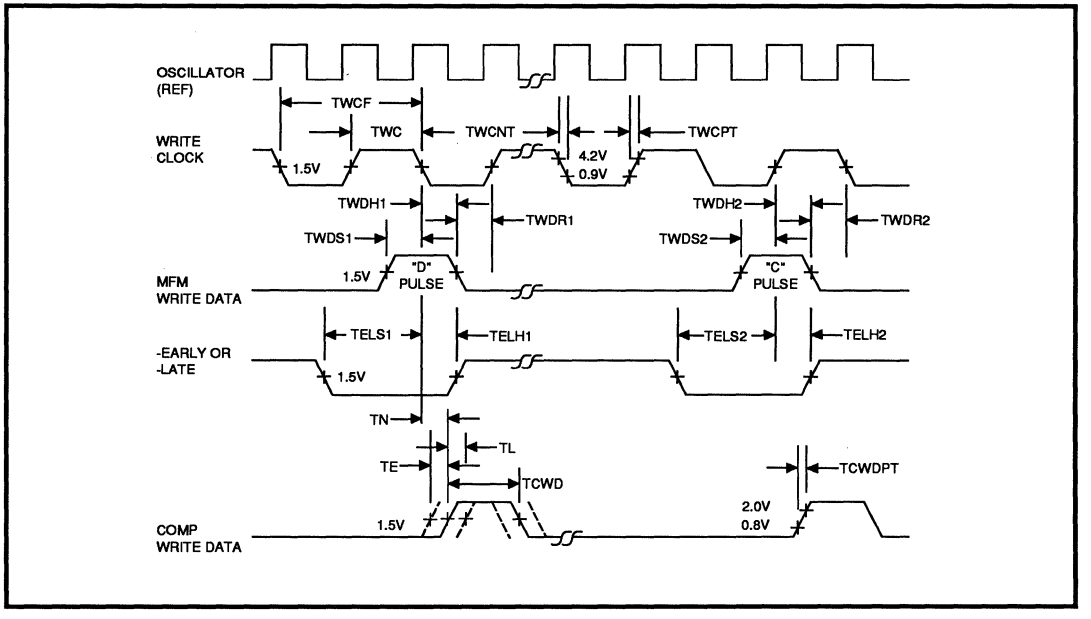


FIGURE 3: Write Precompensation Waveforms

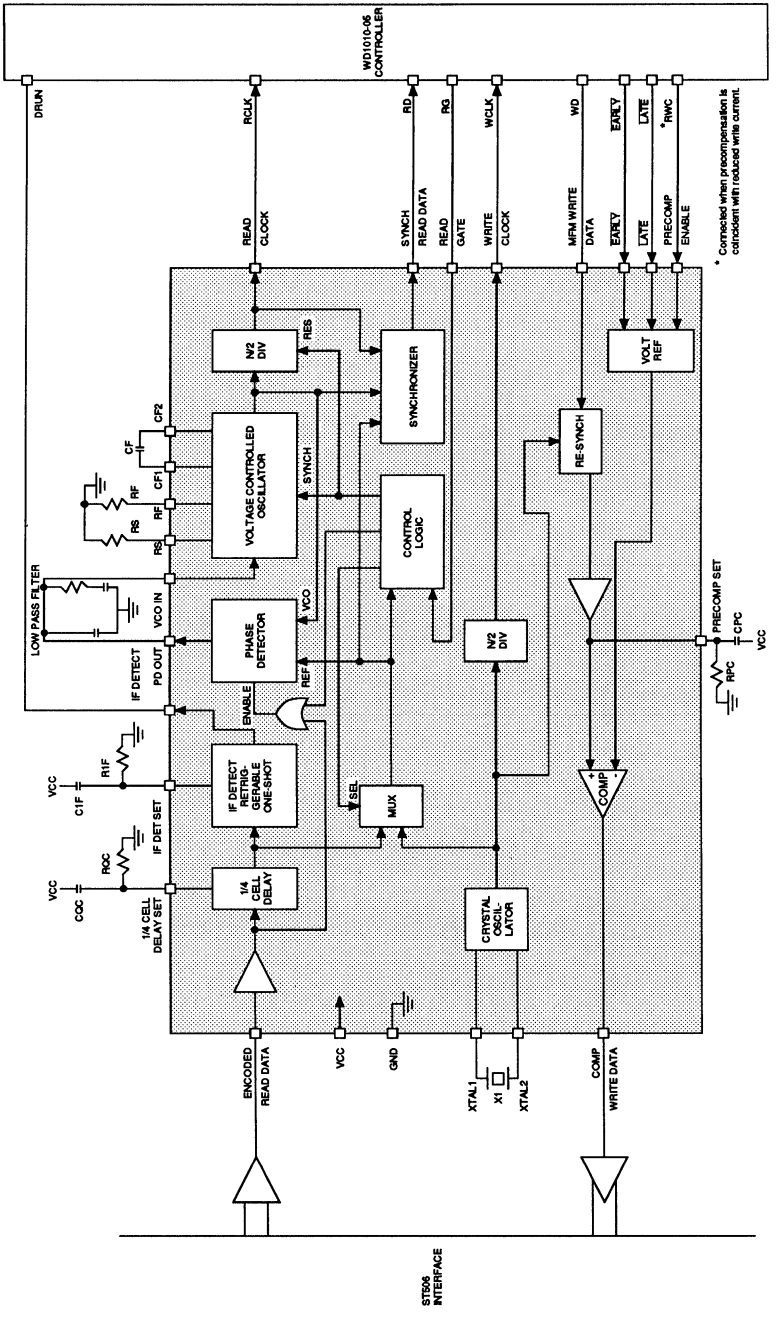


FIGURE 4: Typical System Connections

Application Information

In a typical application the SSI 32D531 is used with a Western Digital WD1010-05 Winchester Disk Controller as shown in Figure 4. Interface to the disk drive consists of the Read data input signal from the drive and the Write data output signal from the SSI 32D531. All the other connections are with the WD1010 and external components.

LOOP FILTER

The low pass filter serves several purposes, it attenuates high frequency components of the phase error signal from the phase detector and modifies the dynamics of the PLL. In lock mode, the PLL can be approximated by the linear model shown in Figure 5.

Standard linear system analysis methods can then be used for analysis. The transfer functions of each of the blocks are as follows:
KD = conversion factor for phase detector in μA/radian
KVCO = VCO gain factor in radians/second volt
F(s) = Low pass filter transfer function

Thus the closed loop transfer function is

$$H(s) = \frac{\frac{KDKVCO}{N} F(s)}{S + \frac{KDKVCO}{N} F(s)}$$

where N = ratio between 5M bit/sec and f_{in} (i.e. for preamble N = 1, for crystal reference N = 0.5)

The transient performance and frequency response is highly dependent on the filter transfer function F(s).

To obtain a zero phase error, a type 2 or higher system must be used. This necessitates the use of a filter transfer function with at least one pole at the origin to obtain two poles at the loop gain origin. A detailed analysis supporting this choice can be found in Phaselock Techniques by Gardner[1]. The filter shown in Figure 6 can be used which will give independent control of the damping factor and natural frequency of the closed loop function. Proper choice of capacitors C1 and C2 will effect loop settling time and stability. More complex filters can be used that give finer control over loop parameters and enhance performance even further.

1. Gardner F.M. Phaselock Techniques, Wiley N.Y., Second Ed., 1967

Vco FREE RUNNING FREQUENCY

The external components RF, RS and CF, are chosen to set the VCO frequency at twice the ENCODED READ DATA bit rate. For a symmetrical window, equal values of RF and RS are used. Increasing the ratio RF/RS causes the detection window to occur earlier in time with respect to ENCODED READ DATA. Decreasing the ratio has the opposite effect, the value of the time shift is:

T = TVCO (RF - RS)/(RF + RS)

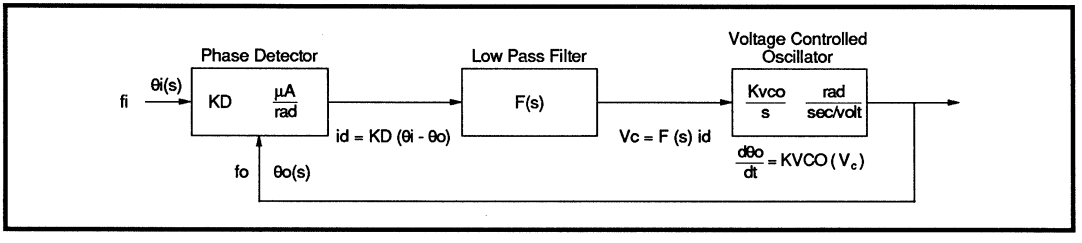


FIGURE 5 : Phase Locked Loop

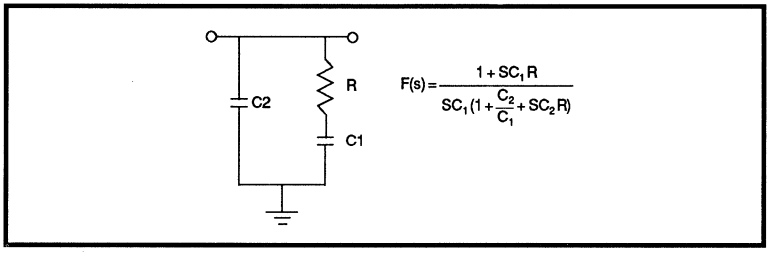
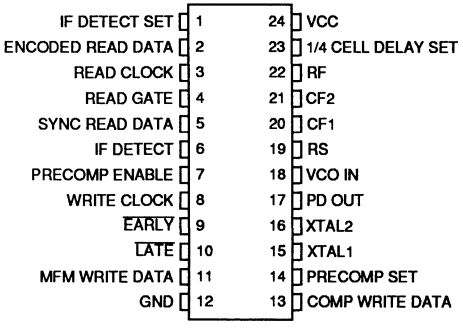


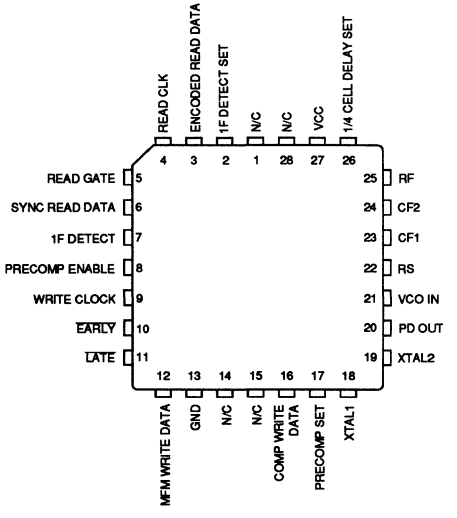
FIGURE 6 : Loop Filter Example

PACKAGE PIN DESIGNATIONS
(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.



24-Lead PDIP



28-Lead PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32D531		
24-Pin PDIP	32D531-CP	32D531-CP
28-Pin PLCC	32D531-CH	32D531-CH

silicon systems™
Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

NOTES:

SSI 32D5321
Data Synchronizer/ 2, 7 RLL ENDEC

silicon systems™
INNOVATORS IN INTEGRATION

January 1988

3

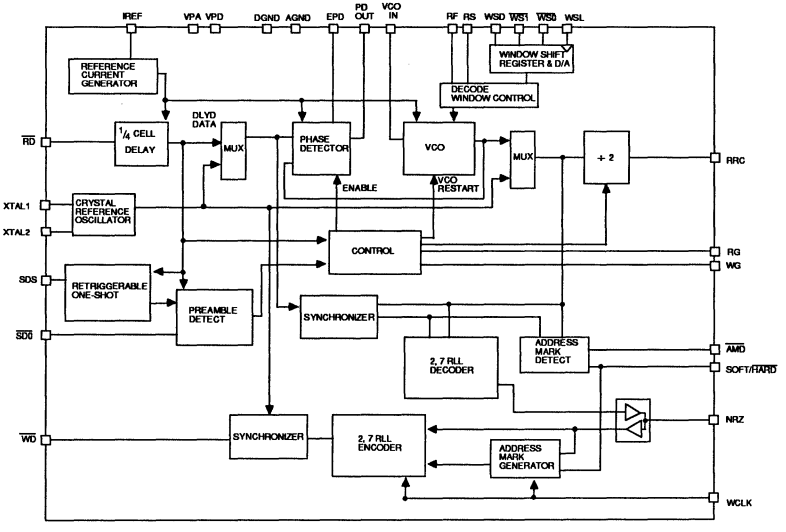
DESCRIPTION

The SSI 32D5321 Data Synchronizer / 2, 7 RLL ENDEC provides data recovery and data encoding for storage systems which employ a 2, 7 RLL encoding format. Data synchronization is performed with a fully integrated high performance PLL. A zero phase restart technique is used to minimize PLL acquisition time. The SSI 32D5321 has been optimized for operation as a companion device to the SSI 32C452A and the AIC 010 controllers. The VCO frequency setting elements are incorporated within the SSI 32D5321 for enhanced performance and reduced board space. Data rate is established with a single external programming resistor. The SSI 32D5321 utilizes an advanced bipolar process technology which affords precise decode window control without the requirement of an accurate 1/4 cell delay or external devices. To enhance disk drive testability, decode window symmetry control is available through a digital µP port and/or two analog pins. This feature can facilitate defect mapping, automatic calibration, systematic error cancellation, window margin testing and error recovery. The SSI 32D5321 requires a single +5V power supply and is available in 28 pin DIP and PLCC packages.

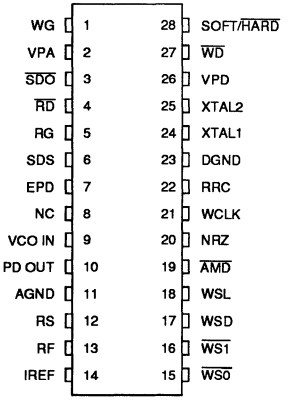
FEATURES

- **Data Synchronizer and 2, 7 RLL ENDEC**
- **7.5 to 15 Mbits/sec Operation Programmed with a Single External Resistor**
- **Optimized for Operation with the SSI 32C452A and AIC 010 Controllers**
- **Programmable Decode Window Symmetry via a µP Port and/or Analog Pins**
- **Fast Acquisition Phase Locked Loop**
  - **Zero Phase Restart Technique**
- **Fully Integrated Data Separator**
  - **No External Delay Lines or Active Devices Required**
- **Crystal Controlled Reference Oscillator**
- **Hard/Soft Sector Operation**
- **+5V Operation**
- **28 Pin DIP and PLCC Packages**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

PIN DESCRIPTIONS

INPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{RD}$	I	READ DATA: Encoded Read Data from the disk drive read channel, active low.
RG	I	READ GATE: Selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the $\overline{RD}$ input and enables the Read Mode/Address Mark Detection sequences. A low level selects the crystal reference oscillator. Pin RG has an internal resistor pull-up.
WG	I	WRITE GATE: Enables the write mode. Pin WG has an internal resistor pull-up.
WSL	I	WINDOW SYMMETRY LATCH: Used to latch the input window symmetry control bits WSD, $\overline{WS0}$ and $\overline{WS1}$ into the internal DAC. An active high level latches the input bits. Pin WSL has an internal resistor pull-up.
WSD	I	WINDOW SYMMETRY DIRECTION: Controls the direction of the optional window symmetry shift. Pin WSD has an internal resistor pull-up.
$\overline{WS0}$	I	WINDOW SYMMETRY CONTROL BIT: A low level introduces a window shift of 1.5 % TORC (Read Reference Clock Period) in the direction established by WSD. Pin $\overline{WS0}$ has an internal resistor pull-up.
$\overline{WS1}$	I	WINDOW SYMMETRY CONTROL BIT: A low level introduces a window shift of 6% TORC (Read Reference Clock Period) in the direction established by WSD. A low level at both $\overline{WS0}$ and $\overline{WS1}$ will produce the sum of the two window shifts. Pin $\overline{WS1}$ has an internal resistor pull-up.
SOFT/$\overline{HARD}$	I	SOFT/$\overline{HARD}$ SECTOR: Selects the address mark and the Preamble field patterns. A high level (Soft Sector) selects a 3T Preamble Field pattern and a non-violating 2, 7 address mark, N7V. A low level (Hard Sector) selects a 4T Preamble Field pattern and disables the address mark circuitry. Pin SOFT/$\overline{HARD}$ has an internal resistor pull-up.
WCLK	I	WRITE CLOCK: Write Clock input. Must be synchronous with the Write Data input on the NRZ Data Port. For small cable delays, WCLK may be connected directly to pin RRC (Read/Reference Clock).
EPD	I	ENABLE PHASE DETECTOR: A low level (Coast Mode) disables the phase detector and allows the VCO to coast. Pin EPD has an internal resistor pull up.

BIDIRECTIONAL PINS

NRZ	I/O	NRZ DATA PORT: Read Data output when RG is high and Write Data input when WG is high. In the idle mode NRZ is in a high impedance state.

PIN DESCRIPTIONS (Cont.)

OUTPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{WD}$	O	WRITE DATA: Encoded write data output, active low.
RRC	O	READ/REFERENCE CLOCK: A multiplexed clock source used by the controller. In the read mode, this clock is the VCO frequency divided by two (1/TORC) and in the write mode it is the crystal reference frequency divided by two (1/TORO). No short clock pulses are generated during a mode change.
$\overline{AMD}$	O	ADDRESS MARK DETECT: In the soft sector Read Mode, a latched low level output indicates that an address mark has been detected. In non-Read modes $\overline{AMD}$ is configured as a high impedance output.
$\overline{SDO}$	O	SYNC DETECT OUTPUT: An active low output that indicates successful detection of the 3T Preamble sync field. THE $\overline{SD0}$ pin is not a TTL level signal.

ANALOG PINS

IREF	I	TIMING PROGRAM PIN: The VCO center frequency and the 1/4 Cell Delay are a function of the current source into pin IREF. The current is set by an external resistor, RR, connected from IREF to VPA.
XTAL1, XTAL2	I	CRYSTAL OSCILLATOR CONNECTIONS: If a crystal oscillator is not desired, XTAL1 maybe driven by a TTL source with XTAL2 open. The frequency must be at twice the data rate.
PD OUT	O	PHASE DETECTOR OUTPUT: Drives the Loop Filter input.
VCO IN	I	VCO CONTROL INPUT: Driven by the Loop Filter output.
SDS	I	SYNC DETECT SET: Used to program the sync detect retriggerable one-shot timing with an external R-C network. Connect the capacitor, Cd, to VPA and the resistor, Rd, to AGND.
RF, RS	I	WINDOW SYMMETRY ADJUST PINS: Provides analog control over the decode window symmetry; typically used to null out any window symmetry offset. A resistor connected from either RF or RS to AGND will provide magnitude and direction control. They can be used in conjunction with the digital control port WSD, $\overline{WS0}$, $\overline{WS1}$.

POWER

DGND, AGND	I	DIGITAL AND ANALOG GROUND
VPA	I	ANALOG +5V
VPD	I	DIGITAL +5V

OPERATION

The SSI 32D5321 is designed to perform data recovery and data encoding in rotating memory systems which utilize a 2, 7 RLL encoding format. In the Read Mode the SSI 32D5321 performs Data Synchronization, Sync Field Search and Detect, Address Mark Detect and Data Decoding. In the Write Mode, the SSI 32D5321 converts NRZ data into the 2,7 RLL format described in Table 1, it generates the Preamble Field, and inserts Address Marks as requested. The interface electronics and architecture of the SSI 32D5321 have been optimized for use as a companion device to the SSI 32C452A or AIC 010 controllers.

The SSI 32D5321 can operate with data rates ranging from 7.5 to 15 Mbits/sec. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/4 cell delay. The value of this resistor is given by:

$$RR = \frac{40.67}{DR} - 0.5\ (K\Omega)$$

where: DR = Data Rate in Mbits/sec.

An internal crystal reference oscillator, operating at twice the data rate, generates the standby reference for the PLL. A series resonant crystal between XTAL1 and XTAL2 should be selected at twice the Data Rate. If a crystal oscillator is not desired, then an external TTL compatible reference may be applied to XTAL1, leaving XTAL2 open.

The SSI 32D5321 employs a Dual Mode Phase Detector; Harmonic in the Read Mode and Non-Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DLYD DATA pulse. In the Write and Idle Modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. Figure 1 depicts the average output current as a function of the input phase error (relative to the VCO period).

The READ GATE (RG), and WRITE GATE (WG), inputs control the device mode as described in Table 2. RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the $\overline{RD}$ input and a low level selects the crystal reference oscillator.

In the Read Mode the rising edge of DLYD DATA enables the Phase Detector while the falling edge is phase compared to the rising edge of the VCO. As depicted in Figure 2, DLYD DATA is a 1/4 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of $\overline{RD}$. An accurate and symmetrical decode window is developed from the VCO clock. The decode window is generated from the falling edges of the VCO clock. By utilizing a fully integrated symmetrical VCO running at twice the data rate, the decode window is insured to be accurate and centered symmetrically about the falling edges of DLYD DATA. The accuracy of the 1/4 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of the decode window.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the DLYD DATA pulse within the decode window. This powerful capability easily facilitates defect mapping, automatic calibration, window margin testing, error recovery, and systematic error cancellation. For enhanced disk drive testability and error recovery, decode window control is

provided via a µP port (WSL, WSD, $\overline{WS0}$, $\overline{WS1}$) as described in Table 3. In applications not utilizing this feature, WSL should be connected to ground, while WSD, $\overline{WS0}$, and $\overline{WS1}$ can be left open.

Window shifts in the range of ±1.5% to ±7.5% of TORC are easily programmed by latching the appropriate control word into the Window Shift Register with the WSL pin. Shifts in the positive or negative directions result in early or late decode windows respectively, as depicted in Figure 3. Additionally, for small systematic error cancellation, a resistor, R, connected from either RS (Early) or RF (Late) to ground will provide analog control over the decode window. The magnitude of this shift, TSA is determined by:

$$TSA = 0.125\ TORC\left(1 - \frac{680 + R}{1180 + R}\right)$$

where: R is in ohms

Pins RF and RS are intended to be used as a trim and should be restricted to ±1.5% window shifts. They can be used in conjunction with the digital control port.

In Non-Read Modes, the PLL is locked to the crystal reference oscillator. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset. By minimizing the phase alignment in this manner (phase error ≤ 0.5 rads), the acquisition time is substantially reduced.

The SSI 32D5321 provides two sync modes for controlling the PLL locking sequence; Soft Sector and Hard Sector.

SOFT SECTOR MODE

The Soft Sector Mode activates the Preamble Search and Address Mark detection circuitry. As depicted in Figure 4, when RG transitions high, the counter is reset and the SSI 32D5321 requires 10 high to low transitions (Preamble '1' bits) before switching the reference input to the PLL, 48 high to low transitions before switching the Read Reference Clock to the VCO clock divided by two and activating the Address Mark Detect circuitry; then it must detect the Address Mark prior to 80 high to low transitions in order to enter the Read Mode. This sequence repeats after 95 input '1' bits until the read mode is successfully entered or until RG is cancelled.

When RG transitions high, the following PLL locking sequence begins:

a) **PREAMBLE SEARCH:**

The 3T detect circuitry initiates the PLL locking sequence once it has detected 10 consecutive '100' bit groups from the 3T preamble field. The 3T detect timing is set by the sum of the 1/4 cell delay and the retriggerable one-shot delay. The 1/4 cell timing capacitor is included on-chip and its timing is externally set by resistor RR. The retriggerable one-shot timing is externally set by resistor Rd and capacitor Cd. The sum of their delays is set to 3.5 bit cell times. Therefore, a continuous stream of input pulses with a 3T bit cell time pulse rate keeps the one-shot reset, and a 4T or longer bit cell time input period allows the one-shot to time out producing a 4T detect pulse. The 4T detect pulse resets the Input Counter and the search is started over.

b) **PLL ACQUISITION:**

Once 10 consecutive '100' bit groups are detected, the reference input to the PLL is switched from the crystal reference oscillator to the DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, and PLL acquistion begins. When an additional 38 '100' bit groups are detected, the Read Reference Clock output (RRC) is switched to the VCO clock divided by 2, the 4T Detect circuitry is inhibited, and the Address Mark Detection circuitry is enabled. If a 4T detect pulse occurs before 48 Preamble '1' bits are detected, then the PLL is locked back to the crystal reference oscillator, the RRC output is switched to the crystal reference oscillator divided by 2, the Input Counter reset, and the sequence is restarted. No short duration glitches will occur at the RRC output during this switching.

c) **ADDRESS MARK DETECTION:**

The circuit searches for the occurrence of the 5EAx16 Address Mark. If an Address Mark is detected prior to the Input Counter reaching count 80, the correct phase of the RRC is ensured by resetting the n/2 divider, the $\overline{AMD}$ output is latched low, the PLL training sequence is terminated, and the Read Mode is entered allowing the data field to be read. If the Input Counter reaches count 80 before the Address Mark is detected, the PLL is locked back to the crystal reference oscillator, the RRC output is switched to the crystal reference oscillator divided by 2, and the PLL training sequence is restarted when the Input Counter reaches count 96. Figure 5 depicts the Address Mark detection sequence.

HARD SECTOR MODE

In the Hard Sector mode (SOFT/$\overline{HARD}$ = 0) the SSI 32D5321 utilizes a 4T (1000) Preamble Field and disables the Preamble Search and Address Mark detection circuitry. It allows the PLL to be controlled directly by RG for Hard Sector format operation. With the absence of an Address Mark, the 4T Preamble Field is utilized to properly set the bit cell alignment boundaries for proper decoding.

When RG transitions high, as depicted in Figure 6, reference input to the PLL is switched from the crystal reference oscillator to DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, and the PLL acquisition begins. When 32 '1' Preamble bits are detected, the RRC output is switched to the VCO clock divided by 2, and the Read Mode is entered allowing the data field to be read.

In the Hard Sector mode, the NRZ output is inverted and will remain low until the data field is read, as shown in Figure 7. Since the Preamble Search circuitry is not utilized, the external one-shot timing components (Cd, Rd) are not required and the SDS pin can be left open.

WRITE OPERATION

In the Write Mode the SSI 32D5321 converts NRZ data from the controller into 2, 7 RLL formatted data for storage onto the disk. The SSI 32D5321 can operate with a soft or hard sectored disk drive. In the Soft Sector Mode, (SOFT/$\overline{HARD}$ = 1) the device generates a 3T Preamble Field and can insert a N7V Address Mark. The N7V Address Mark is a valid 2, 7 RLL pattern which is not contained in the code set. In the Hard Sector Mode, (SOFT/$\overline{HARD}$ = 0) the device generates a 4T Preamble Field and no Address Mark. Serial NRZ data is clocked into the SSI 32D5321 and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK input. In a SCSI or ST506 operation, WCLK is connected directly to the RRC output.

SOFT SECTOR MODE

In the Soft Sector Mode, when WRITE GATE (WG), transitions high and the NRZ input is held low, the SSI 32D5321 automatically generates the 3T (100) Preamble Field at the WRITE DATA ($\overline{WD}$), output. The 3T Preamble Field will continue to be generated until the first low to high transition on the NRZ line. As shown in Figure 8, the first low to high transition occurs with the second bit '1' of the 5_{16} (0101) in the 5EAx16 Address Mark generation pattern. To generate the Address Mark, the SSI 32D5321 automatically changes the '1' in the eleventh position (see note 3) of the 2, 7 RLL encoded sequence, to a '0'. This generates a pattern of seven zero's followed by two zero's. This unique pattern satisfies the 2, 7 RLL constraints, but will never occur during a normal encoding sequence. The x_{16} of the 5EAx16 Address Mark generation pattern can be selected, a 'C_{16}' (1100) was utilized in this example.

HARD SECTOR MODE

In the Hard Sector Mode, when WG goes high and the NRZ input is held low, the SSI 32D5321 automatically generates the 4T (1000) Preamble Field at the WRITE DATA, $\overline{WD}$, output. Note that in the Hard Sector mode, the NRZ input is inverted, therefore a constant low is equivalent to an '11 . . . ' input which generates the 4T '1000 . . . ' Preamble Field. The 4T Preamble Field will be generated between the time WG goes high and the first low to high transition on the NRZ line. The 32D5321 requires a minimum of 32 4T (1000) bit groups prior to the data field.

NRZ	2, 7 RLL
10	0100
11	1000
000	000100
010	100100
011	001000
0010	00100100
0011	00001000

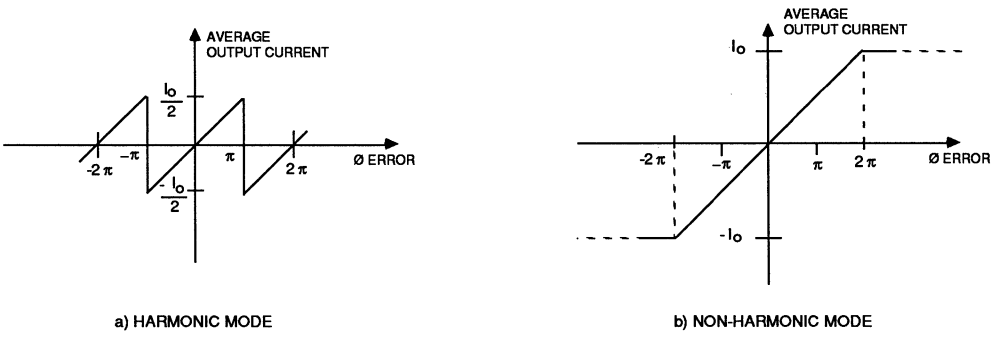
TABLE 1: 2, 7 RLL CODE SET

WG	RG	MODE
0	0	IDLE
0	1	READ
1	0	WRITE
1	1	ILLEGAL

TABLE 2: MODE CONTROL

Ts, NOMINAL WINDOW SHIFT	WSD	$\overline{WS1}$	$\overline{WS0}$
+TS3	0	0	0
+TS2	0	0	1
+TS1	0	1	0
0	0	1	1
-TS3	1	0	0
-TS2	1	0	1
-TS1	1	1	0
0	1	1	1

TABLE 3 : DECODE WINDOW SYMMETRY CONTROL



a) HARMONIC MODE

b) NON-HARMONIC MODE

Note 1) Io is the magnitude of the charge pump current.
2) Phase error is relative to the VCO period

FIGURE 1: PHASE DETECTOR TRANSFER FUNCTION

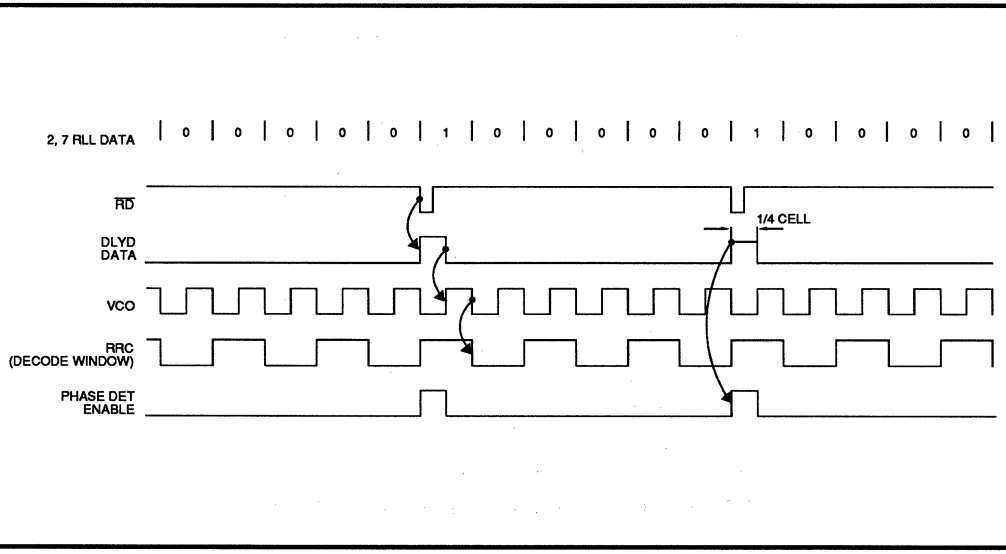


FIGURE 2: DATA SYNCHRONIZATION WAVEFORM DIAGRAM

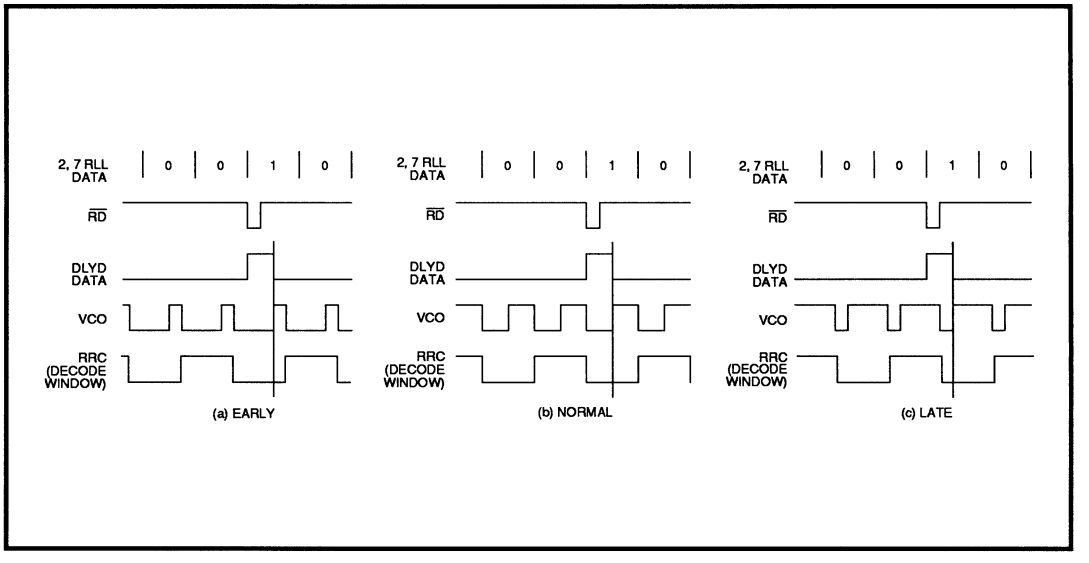


FIGURE 3: DECODE WINDOW

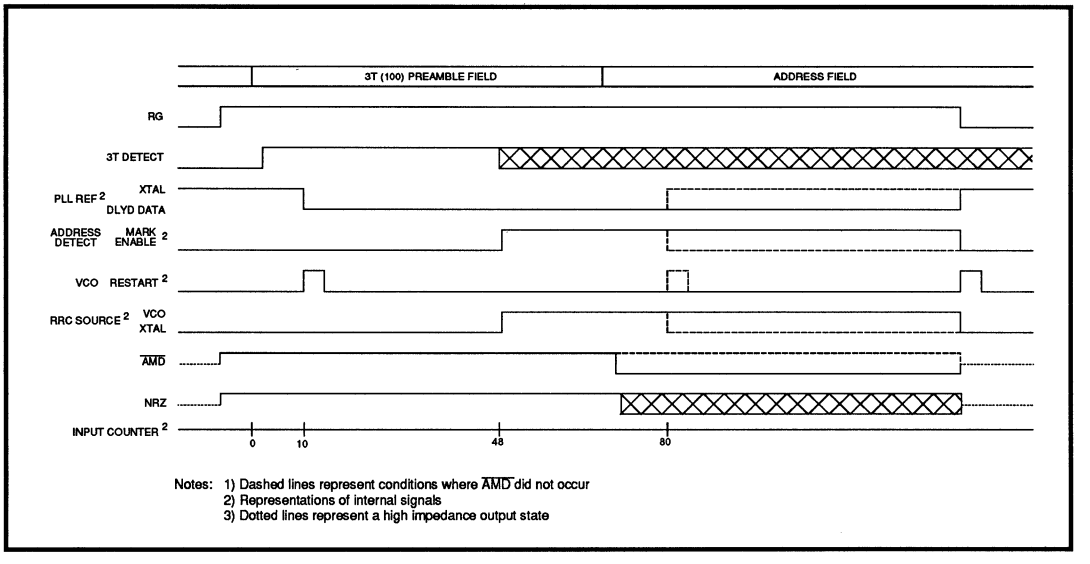


FIGURE 4: SOFT SECTOR MODE TIMING DIAGRAM

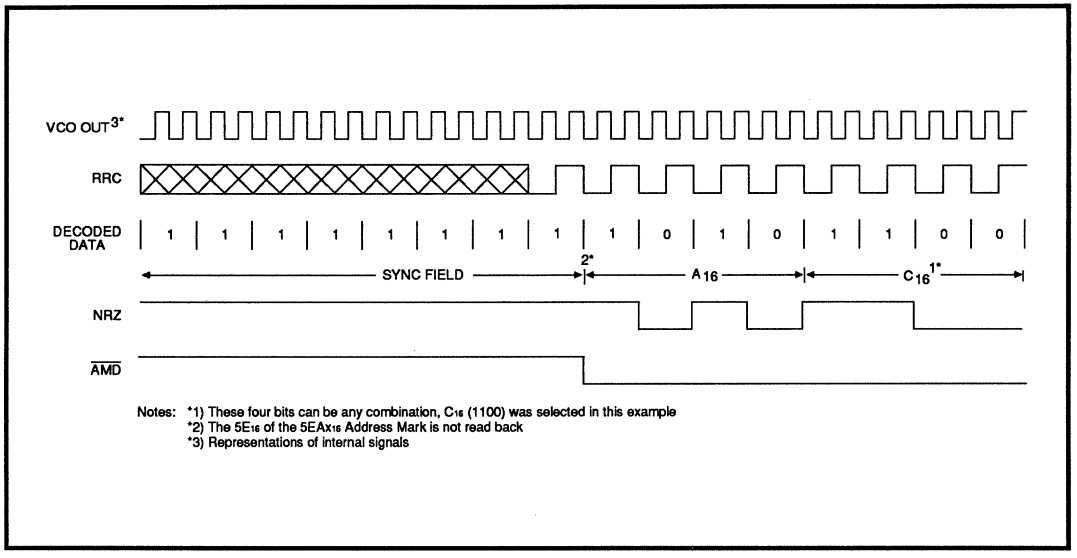


FIGURE 5: ADDRESS MARK DETECTION AND NRZ OUTPUT WAVEFORM

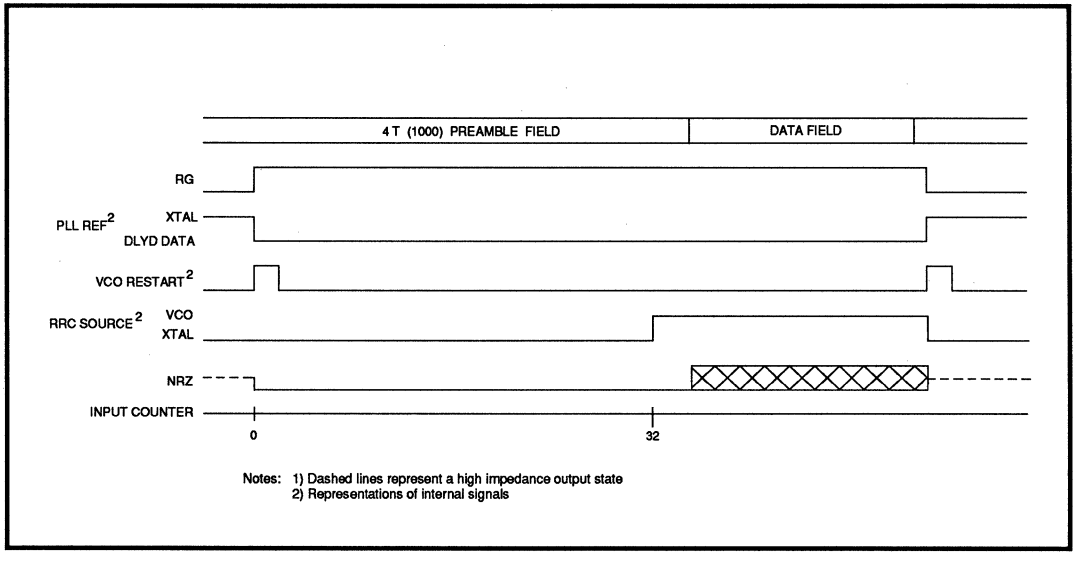


FIGURE 6: HARD SECTOR MODE TIMING DIAGRAM

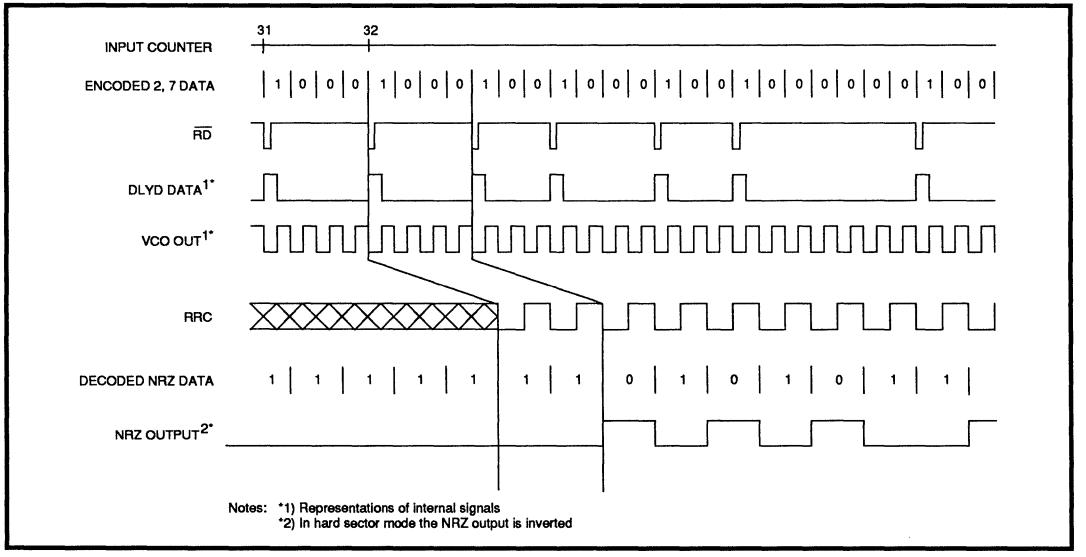


FIGURE 7: HARD SECTOR MODE DECODE TIMING

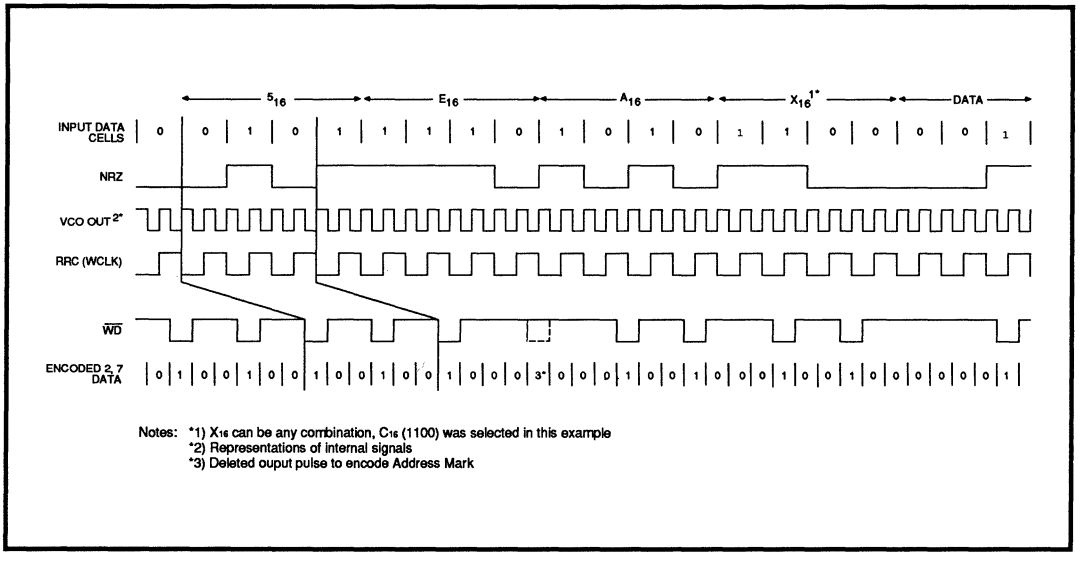


FIGURE 8: WRITE ADDRESS MARK GENERATION

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATINGS	UNIT
Storage Temperature	-65 to +150	° C
Ambient Operating Temperature, TA	0 to +70	° C
Junction Operating Temperature	0 to +130	° C
Supply Voltage, VCC	-0.5 to 7	Vdc
Voltage Applied to Logic inputs	-0.5 to VCC +0.5	Vdc
Maximum Power Dissipation	950	mW

DC ELECTRICAL CHARACTERISTICS - unless otherwise specified, 4.75V < VCC < 5.25V, TA = 0°C to 70°C, 7.5MHz < 1/TORC < 15MHz , 15MHz < 1/TVCO < 30MHz

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VIH, High Level Input Voltage		2.0			V
VIL, Low Level Input Voltage				0.8	V
IIH, High Level Input Current	VIH = 2.7V			20	µA
IIL, Low Level Input Current	VIL = 0.4V			-0.36	mA
VOH, High Level Output Voltage	IOH = -400µA	2.7			V
VOL, Low Level Output Voltage	IOL = 4mA			0.5	V
ICC, Power Supply Current	All outputs open			165	mA

DYNAMIC CHARACTERISTICS AND TIMING

READ MODE (See figure 9)

TRD, Read Data Pulse Width		20		TORC-40	nS
TFRD, Read Data Fall Time	2.0V to 0.8V, CL ≤ 15 pF			15	nS
TRRC, Read Clock Rise Time	0.8V to 2.0V, CL ≤ 15pF			8	nS
TFRC, Read Clock Fall Time	2.0V to 0.8V, CL ≤ 15pF			5	nS
TPNRZ, NRZ (out) Propagation Delay		-15		15	nS
TPAMD, $\overline{AMD}$ Propagation Delay		-15		15	nS
1/4 Cell + Retriggerable One-Shot Detect Stability		-4		+4	%

READ MODE (Cont.)

PARAMETER	CONDITIONS	MIN	MAX	UNIT
1/4 Cell + Retriggerable One-Shot Delay*	TD=6.14(RR +0.5) + 0.172Rd (Cd +11.5) RR = KΩ Rd = KΩ Cd = 68pF to 100pF	0.89TD	1.11TD	nS
Note: * = Excludes External Capacitor and Resistor Tolerances				

WRITE MODE (See figure 10)

TWD, Write Data Pulse Width	CL ≤15pF	(TORO/2) -12	(TORO/2) +12	nS
TFWD, Write Data Fall Time	2.0V to 0.8V, CL ≤ 15pF		8	nS
TOWC Write Data Clock Repetition Period		TORO -12	TORO +12	nS
TRWC Write Data Clock Rise Time	0.8V to 2.0V		10	nS
TFWC Write Data Clock Fall Time	2.0V to 0.8V		8	nS
TSNRZ, NRZ (in) Set Up Time		20		nS
THNRZ, NRZ (in) Hold Time		7		nS

DATA SYNCHRONIZATION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TVCO VCO Center Frequency Period	VCO IN = 2.7V TO = 1.23E - 11 (RR +500) VCC = 5.0V	0.8TO		1.2TO	sec
VCO Frequency Dynamic Range	1.0V ≤ VCO IN ≤ VCC -0.6V VCC = 5.0V	±27		±40	%
KVCO VCO Control Gain	ωo = 2π / TO 1.0V ≤ VCO IN ≤ VCC -0.6V	0.14ωo		0.20ωo	rad / sec-V
KD Phase Detector Gain	KD = 0.309 / (RR + 500) VCC = 5.0V	0.83KD		1.17 KD	A/rad
KVCO x KD Product Accuracy		-28		+28	%
VCO Phase Restart Error		-0.5		+0.5	rad
Decode Window Centering Accuracy				± (0.01 TORC + 2)	nS
Decode Window		(TORC/2) -2			nS

DATA SYNCHRONIZATION (Cont.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TS1	Decode Window Time Shift Magnitude	TS1 = 0.015 TORC	0.85 TS1		1.15 TS1	sec
TS2	Decode Window Time Shift Magnitude	TS2 = 0.06 TORC	0.90 TS2		1.1 TS2	sec
TS3	Decode Window Time Shift Magnitude	TS3 = 0.075 TORC	0.90 TS3		1.1TS3	sec
TSA	Decode Window Time Shift Magnitude	$TSA = 0.125\,TORC\left(1 - \frac{680 + R}{1180 + R}\right)$ with: R in ohms	0.65 TSA		1.35TSA	sec

CONTROL CHARACTERISTICS (See figure 11)

TSWS, $\overline{WS0}$, $\overline{WS1}$, WSD Set Up Time		50			nS
THWS, $\overline{WS0}$, $\overline{WS1}$, WSD Hold Time		0			nS
RG, WG, SOFT/$\overline{HARD}$ Time Delay				100	nS

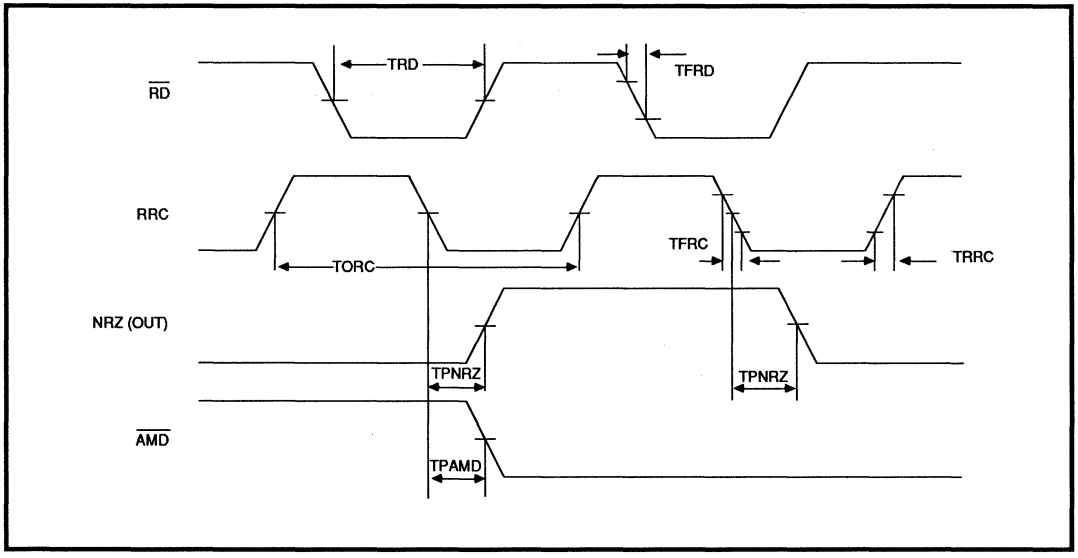


FIGURE 9: READ TIMING

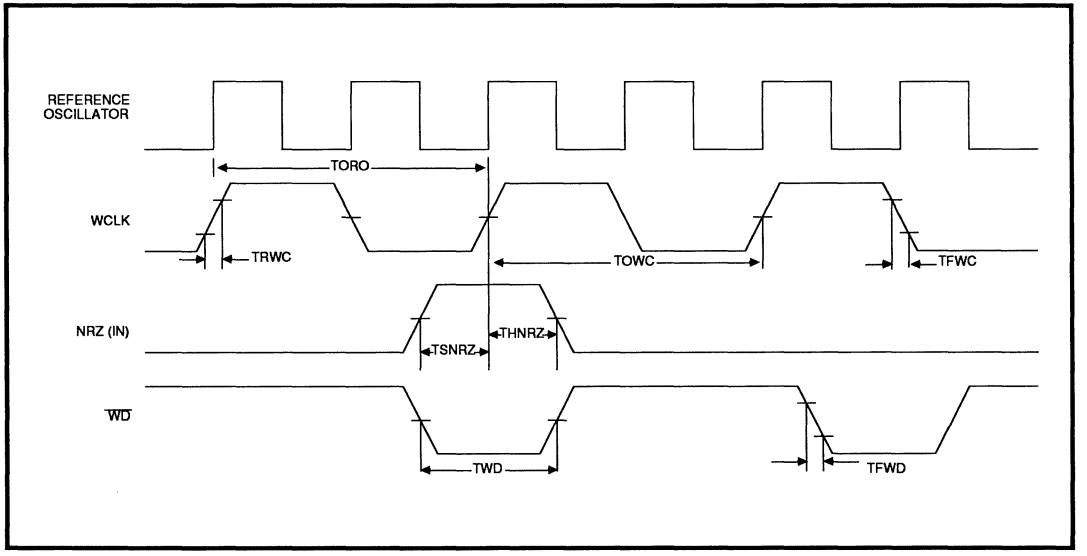


FIGURE 10: WRITE TIMING

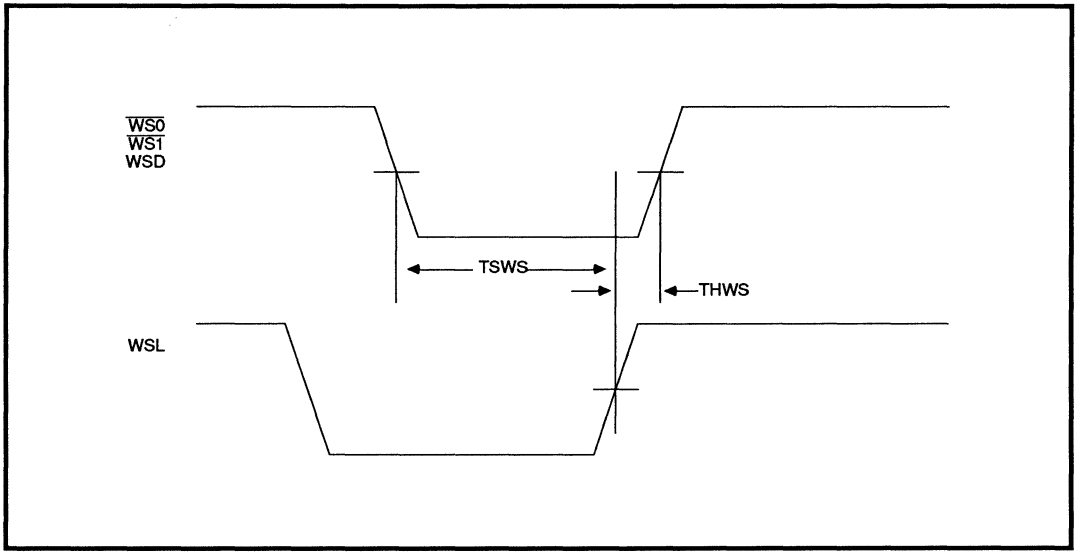
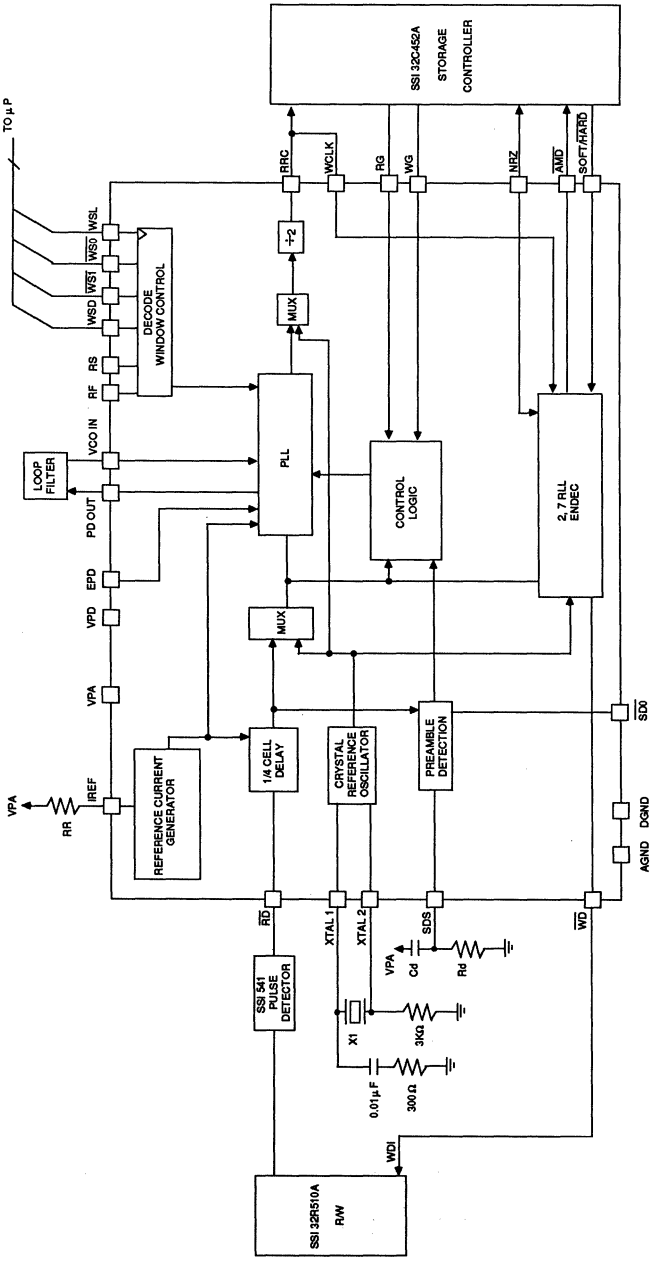


FIGURE 11: CONTROL TIMING



TYPICAL SSI 32D5321 APPLICATION

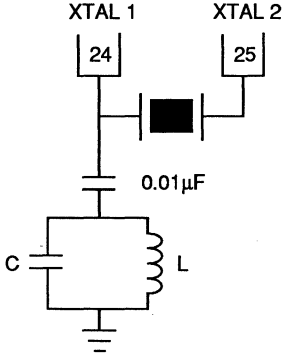
APPLICATIONS INFORMATION

REFERENCE OSCILLATOR

An internal reference oscillator, operating at twice the data rate, generates the standby reference for the PLL. A series resonant crystal between XTAL1 and XTAL2, should be selected at twice the Data Rate. If a crystal oscillator is not desired, then an external TTL compatible reference may be applied to XTAL1, leaving XTAL2 open.

An R-C network is employed on the demonstration board for operation with the crystal oscillator. The purpose of this network is to minimize the coupling of noise into the clock. The 3KΩ resistor from XTAL2 to ground helps to speed up the oscillator transitions, while the R-C network from XTAL1 to ground lowers the impedance to reduce capacitive coupling effects. In applications utilizing a TTL compatible reference signal, this network should be removed.

If it is desired to operate a crystal at a non-fundamental or harmonic frequency, then the following network is suggested:



$$\omega_o = 2\pi F_o = \frac{1}{\sqrt{LC}}$$

$$Q_o = \omega_o C R_{in}$$

The typical input impedance looking into XTAL1 is approximately Rin = 250Ω. It is recommended to design the value of Q_o at approximately 10 to 15. Therefore, a resonant frequency of F_o = 20MHz would result in L ≅ 0.16μH and C ≅ 380pF.

LOOP FILTER

The performance of the SSI 32D5321 is directly related to the selection of the loop filter. The loop filter characteristics should be optimized for:

(A) Fast Acquisition

The ability of the loop to quickly obtain lock when the input signal to the Phase Detector is switched between the reference oscillator (crystal) and the Read Data ($\overline{RD}$). Fast acquisition implies a large loop bandwidth so that it can quickly respond to changes at the input.

(B) Data Margin

The ability of the loop to ignore bit shifts (jitter) and maintain a well centered window about the data pulse train. In general, it is not desirable to allow the loop to respond to a single shifted bit as this would cause the subsequent bit to be poorly centered within its window and possibly cause an error. This requirement implies a small loop bandwidth reducing the sensitivity to high frequency jitter.

(C) Data Tracking

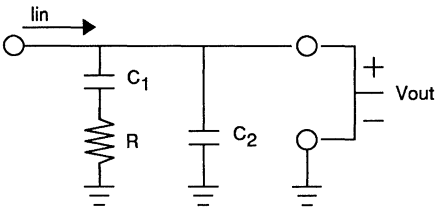
The ability to respond to instantaneous changes in phase and frequency of the data. This can be a result of such phenomena as disk rotational speed variations which cause changes in the characteristics of the incoming data stream. In general, this requirement is consistent with that of fast acquisition, however, this depends upon the application.

Although the loop performance characteristics place conflicting requirements on the loop bandwidth, the architecture of the SSI 32D5321 significantly simplifies the design by minimizing the "step in phase" and "step in frequency" encountered when switching the Phase Detector input reference signal. A zero phase restart technique is employed to minimize the initial phase error while the standby reference oscillator keeps the VCO at the center frequency during non-read modes.

One approach in determining the initial loop filter selection is to consider the requirements imposed during acquisition. This includes both acquiring lock to the crystal reference in non-read modes, as well as locking to the preamble field prior to decoding data. The format of the sector will dictate which of these two criteria imposes the tightest restriction on acquisition.

The requirements for acquiring lock to the crystal oscillator are application specific and usually depend upon the length of the Write Splice gap. Therefore, the design approach employed in this analysis will be based upon the requirements during acquisition to the preamble field. The length (in time) of the preamble field is set by the SSI 32D5321 locking sequence. Knowing this length in time, and that our initial phase error is less than 0.5 radians, we can determine an acceptable loop bandwidth (ωn) and damping factor (ζ).

One possible loop filter configuration is as follows:



The role of C1 is as an integrating element. The larger this capacitance, the longer the acquisition time; the smaller the capacitance, the greater the ability to track high frequency jitter. The resistor R reduces the phase shift induced by C1. The capacitor C2 will suppress high frequency transients and will have minimal effect on the loop response if it is small relative to C1 (typically C2 = C1/10)

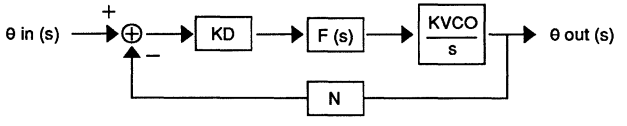
The loop filter transfer function is:

$$F(s) = \frac{Vout}{Iin} = \frac{1 + sRC_1}{sC_1\left(1 + sC_2\,R + C_2/C_1\right)}$$

If C2 << C1, then:

$$F(s) = \frac{Vout}{Iin} = \frac{1 + sRC_1}{sC_1}$$

The overall block diagram for the phaselock loop can be described as:



Where,

KD = Phase Detector gain [A/rad]

F(s) = Loop filter impedance [V/A]

KVCO/s = VCO control gain [rad/sec-V]

N = The ratio of the reference input frequency to the VCO output frequency

The closed loop transfer function is;

$$T(s) = \frac{\theta out(s)}{\theta in(s)} = \frac{G(s)}{1 + G(s)H(s)}$$

$$= \frac{KD \cdot KVCO\left[(1 + sRC_1)/C_1\right]}{s^2 + s\left[N \cdot KD \cdot KVCO \cdot R\right] + \frac{N \cdot KD \cdot KVCO}{C_1}}$$

by putting the characteristic equation (denominator) in the form of;

$$s^2 + 2s\zeta\omega n + \omega n^2$$

we can solve for ωn and ζ to get;

$$\omega n^2 = \frac{N \cdot KD \cdot KVCO}{C1} \qquad \zeta = \frac{N \cdot KD \cdot KVCO \cdot R}{2\omega n}$$

Now we can solve for R, C1 and C2:

$$C1 = \frac{N \cdot KD \cdot KVCO}{\omega n^2}$$

$$R = \frac{2\zeta\omega n}{N \cdot KD \cdot KVCO}$$

$$C_2 = \frac{C_1}{10}$$

where: ωn = loop bandwidth

ζ = loop damping factor

Because of the nature of Run Length Limited (RLL) codes, the Phase Detector will only be enabled during a data pulse. This technique allows the VCO to run at a center frequency with period, TVCO, equal to one encoded data bit cell time.

Figure 12 represents the relationship between the VCO output when locked to various Phase Detector input signals.

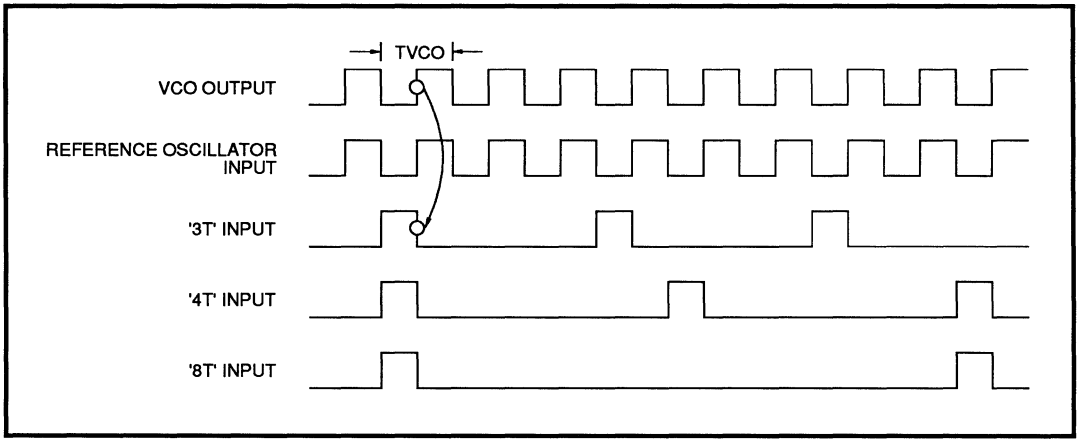


FIGURE 12: RELATIONSHIP OF VCO OUTPUT TO PHASE DETECTOR INPUT

The average amplitude of the Phase Detector gain depends upon the Phase Detector input signal. When the PLL is locked to the reference oscillator, the Phase Detector is continuously enabled and the gain is at its maximum. When the PLL is tracking data and the input is an "8T" pattern, then the Phase Detector gain is at its minimum. The following indicates the value of "N" for various input conditions:

N = 1.0 , for θin = reference oscillator

N = 0.33 , for θin = 3T (100) preamble field (maximum data frequency)

N = 0.25 , for θin = 4T (1000) preamble field

N = 0.125 , for θin = 8T (minimum data frequency)

Throughout this analysis the PLL has been considered as a continuous time system. In actuality the characteristics of the Phase Detector result in a sampled data system. By utilizing an integrating loop filter to average and smooth the Phase Detector change pump output pulses, this analogy should be reasonable.

LOOP FILTER - Example for a 10Mbit/sec Soft Sector Application

In the Soft Sector mode the PLL locking sequence allows the VCO to be within a determined amount of error after 38 x '3T' (100) bit groups. At 10Mbit/sec each data bit cell time, TVCO, is equal to 50nS. This results in:

$$t_{max} = (38)\ (3)\ (50nS) = 5.7\mu S$$

Therefore, the PLL has 5.7μS to settle to within an acceptable amount of error before tracking and decoding data. Because the SSI 32D5321 employs a zero phase restart technique, the initial phase error is less than 8% TORC (0.5rad) or:

$$\Delta\theta e < (0.08)(100nS)$$

$$\Delta\theta e < 8nS$$

Determining an acceptable amount of phase error after locking to the preamble field depends upon the system requirements. In addition, it may be necessary to consider the effects of frequency steps in applications where motor speed control tolerances are significant. Generally, an acceptable amount of error is defined to be that amount which when added to all other timing error contributors, results in the data being within its timing window by the required margin.

In general, it is desirable to have the loop damping factor "ζ" between 0.5 and 1.0 during acquisition. For a high gain, second-order loop this results in minimal noise bandwidth. For this example we will let ζ = 0.7.

Figure 13 represents the phase errors response in time to a transient step in phase as a function of the loop bandwidth and damping factor. Figure 14 indicates the response of the VCO control voltage to compensate for this step in phase.

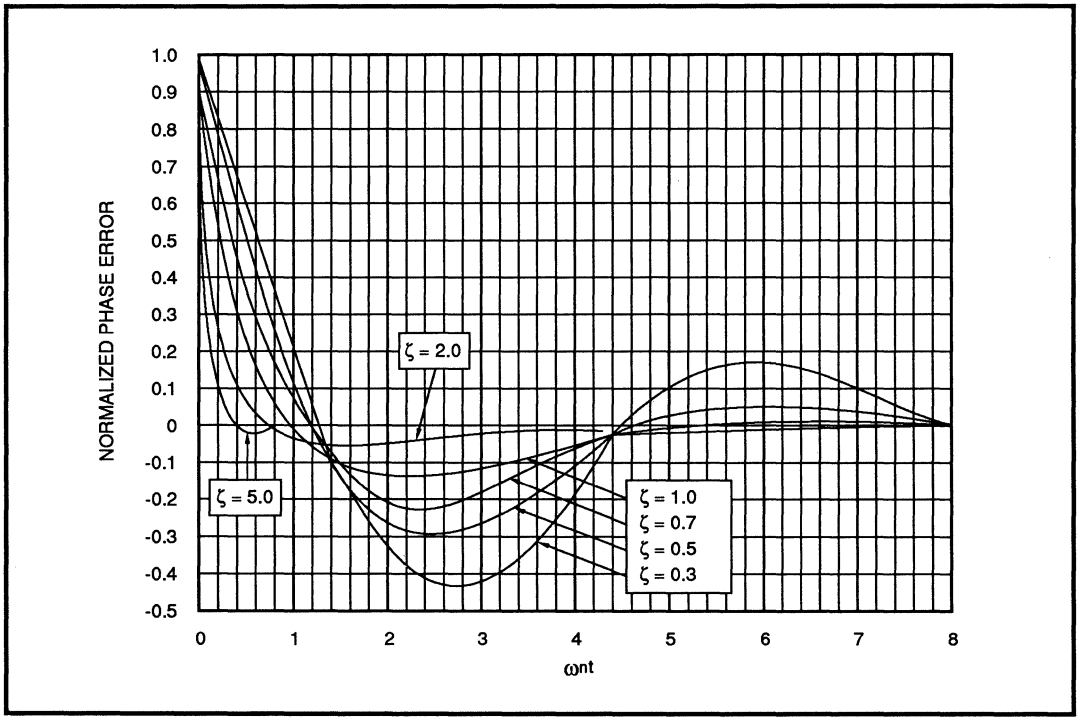


FIGURE 13: TRANSIENT PHASE ERROR θe(t) DUE TO A STEP IN PHASE Δθ

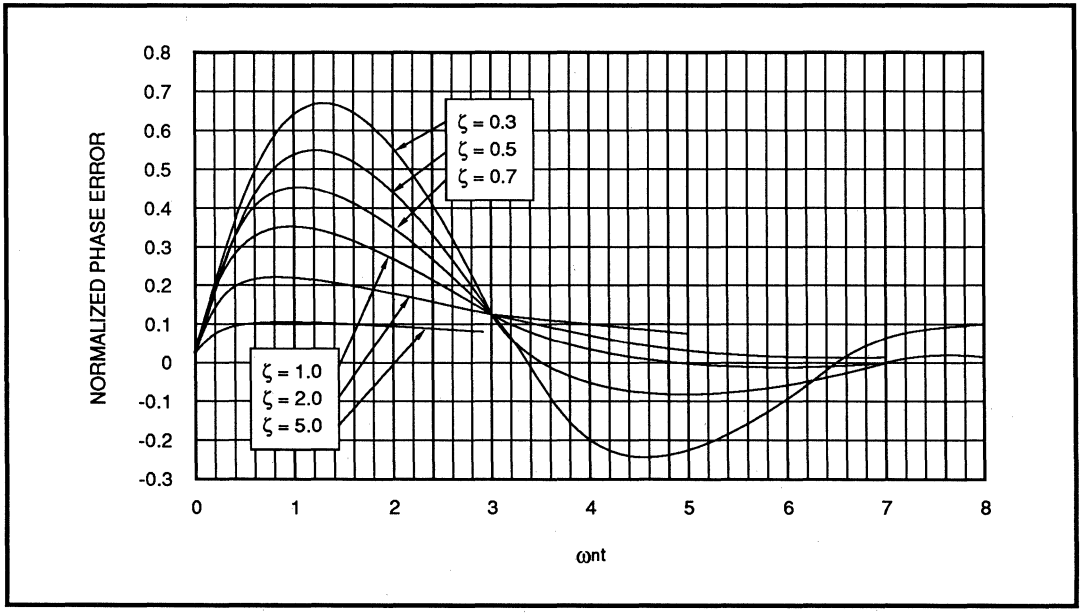


FIGURE 14: TRANSIENT PHASE ERROR θe(t) DUE TO A STEP IN FREQUENCY Δω

As shown in Figure 13, with $\zeta = 0.7$, our initial transient phase error will be at most 22% of its original value at $\omega nt = 2.3$, 7.5% at $\omega nt = 4.0$, etc. For this example we want the final phase error to be less than 1% of its original level. This results in a ωnt between 5 and 6. To simplify the results, let $\omega nt = 5.7$.

Now,

$\omega nt = 5.7$

and $t_{max} = 5.7\mu S$

$\therefore \omega n = 1.0 \cdot 10^6$ rad/sec

with $\zeta = 0.7$

Since we are evaluating the loop response during acquisition to the '3T' preamble, N = 0.33.

Now we have all the information required to calculate the loop filter component values.

$RR = 3567\Omega$

$\omega n = 1.0 \cdot 10^6$ rad/sec

$\zeta = 0.7$

$KD(typ) = 0.309/(RR+500) = 7.6 \cdot 10^{-5}$ A/rad

$KVCO(typ) = 0.17\omega o = 0.17(2\pi)/T0 = 2.14 \cdot 10^7$ rad/sec-volt

$N = 0.33$

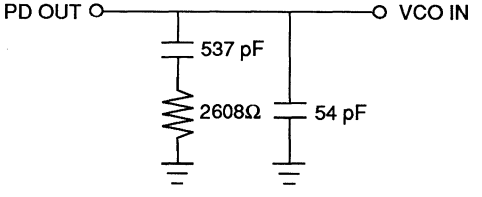
which results in:

$$R = \frac{2\zeta\omega n}{N \cdot KD \cdot KVCO} = 2608\Omega$$

$$C_1 = \frac{N \cdot KD \cdot KVCO}{\omega n^2} = 537pF$$

$$C_2 = \frac{C_1}{10} = 54pF$$

or,



This loop filter configuration and its component values should be considered a starting point. The final value of ωn depends upon the system requirements and can certainly be optimized for a specific application. In the table below, we have listed some suggested external component values for several common data rates.

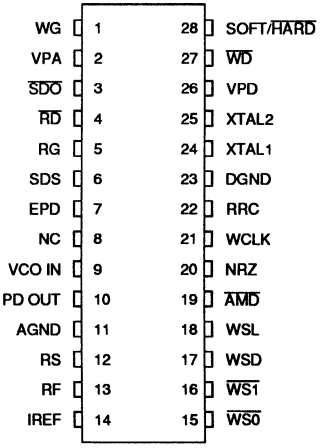
DATA RATE (Mbit/SEC)	DAMPING FACTOR,	LOCK TIME t_{max} (μS)	ωnt	BANDWIDTH $\omega n\left(\frac{rad}{sec}\right)$	EXTERNAL COMPONENT VALUES					
					RR (KΩ)	Cd (pF)	Rd (KΩ)	R (KΩ)	C_1 (pF)	C_2 (pF)
7.5	0.7	7.5	5.0	6.67×10^5	4.92	100	11.0	3.0	687	69
10.0	0.7	5.7	5.7	1.0×10^6	3.57	82	10.0	2.7	510	51
15.0	0.7	3.8	5.7	1.5×10^6	2.21	100	6.22	1.8	510	51

LAYOUT CONSIDERATIONS

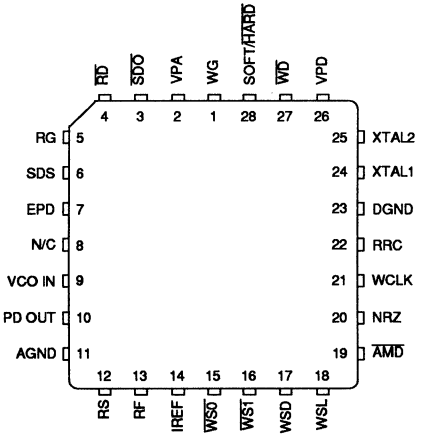
As with other high frequency analog devices the SSI 32D5321 requires care in layout. The designer should keep analog signal lines as short as possible and well balanced. Use of a ground plane is recommended, along with supply bypassing to separate the SSI 32D5321, and associated circuitry, from other circuits on the PCB.

SSI 32D5321
Data Synchronizer/
2, 7 RLL ENDEC

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32D5321 28 Pin PLCC	SSI 32D5321 - C28H	32D5321 - CH
SSI 32D5321 28 Pin Plastic DIP	SSI 32D5321 - C28P	32D5321 - CP

silicon systems™
Silicon Systems, Inc., 14351 Myford Road, Tustin CA 92680, (714) 731-7110, TWX 910-595-2809

NOTES:

SSI 32D534
Data Synchronizer/ MFM ENDEC

July, 1988

DESCRIPTION

The SSI 32D534 Data Synchronizer/MFM ENDEC is intended to provide data recovery and data encoding in storage systems which employ an MFM encoding format. Data synchronization is performed with a fully integrated high performance PLL and encoding is performed in soft/hard sector formats with optional write precompensation through the internal delay line. The SSI 32D534 has been optimized for operation as a companion device to the SSI 32C452 and the AIC 010 family of controllers. The frequency setting elements are incorporated within the SSI 32D534 for enhanced performance and reduced board space. Data rate, adjustable from 5 to 10Mbits/sec, is established with a single external programming resistor for Direct Sync operation or with two external resistors for Auto Sync operation.

The SSI 32D534 utilizes an advanced bipolar process technology that affords precise decode window control without the requirement of an accurate 1/4 cell delay or

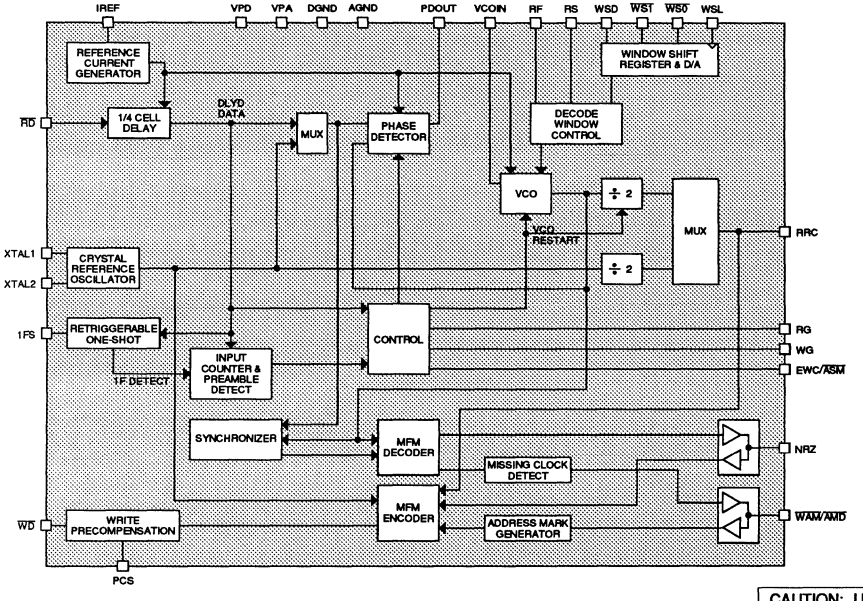
(Continued)

FEATURES

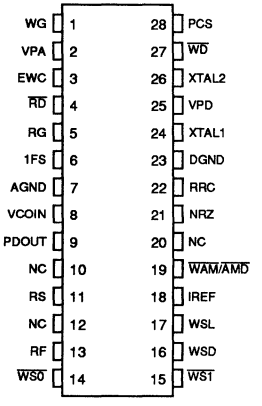
- **Data Synchronizer and MFM ENDEC**
- **5 to 10 Mbits/sec operation programmed with a single external resistor**
- **Optimized for operation with the SSI 32C452 and AIC 010 family of controllers**
- **Programmable decode window symmetry via a µP port and/or analog pins**
- **Programmable write precompensation**
- **Fast acquisition phase locked loop - zero phase restart technique**
- **Fully integrated data separator - no external delay lines or active devices required**
- **+5V operation**
- **28 pin DIP and PLCC packages**

3

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

external devices. To enhance disk drive testability, decode window symmetry control is available through a digital microprocessor port and/or two analog pins. This feature can facilitate automatic calibration, systematic error cancellation, and window margin testing. A zero phase restart technique is used to minimize PLL acquisition time. The SSI 32D534 requires a single +5V power supply and is available in 28-pin DIP and PLCC packages.

PIN DESCRIPTION

INPUT PINS

NAME	DESCRIPTION
$\overline{RD}$	READ DATA. MFM encoded Read Data from the disk drive read channel, active low.
RG	READ GATE. Selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the $\overline{RD}$ input and enables the Read Mode/Address Mark Detection sequences. A low level selects the crystal reference oscillator.
WG	WRITE GATE. Enables the write mode.
WSL	WINDOW SYMMETRY LATCH. Used to latch the input window symmetry control bits WSD, $\overline{WS0}$ and $\overline{WS1}$ into an internal DAC. An active high level latches the input bits.
WSD	WINDOW SYMMETRY DIRECTION. Controls the direction of the optional window symmetry shift.
$\overline{WS0}$	WINDOW SYMMETRY CONTROL BIT. A low level introduces a window shift of 1.5% of TORC (Read Reference Clock Period) in the direction established by WSD.
$\overline{WS1}$	WINDOW SYMMETRY CONTROL BIT. A low level introduces a window shift of 6% of TORC (Read Reference Clock Period) in the direction established by WSD. A low level at both $\overline{WS0}$ and $\overline{WS1}$ will produce the sum of the two window shifts.
EWC/$\overline{ASM}$	ENABLE WRITE PRECOMP/AUTO SYNC MODE. Selects the synchronization sequence required in order to enter Read Mode, a low level selects the Auto Sync Mode. In the Write Mode, a high level enables write precompensation.

OUTPUT PINS

NAME	DESCRIPTION
$\overline{WD}$	WRITE DATA. MFM encoded write data output, active low. Precompensation is enabled with the EWC/$\overline{ASM}$ input pin.
RRC	READ/REFERENCE CLOCK. A multiplexed clock source used by the controller. In the read mode, this clock is the VCO frequency divided by two (1/TORC) and in the write mode it is the crystal reference frequency divided by two (1/TORO).

PIN DESCRIPTION (Continued)

BIDIRECTIONAL PINS

NAME	DESCRIPTION
NRZ	NRZ DATA PORT. Read data output when RG is high and write data input when WG is high.
$\overline{WAM}/\overline{AMD}$	WRITE ADDRESS MARK/ADDRESS MARK DETECT. In the Write Mode, used to delete clock/data pulses in the MFM encoded output stream, $\overline{WD}$, active low. In the Read Mode, a latched low level output indicates that an address mark has been detected.

ANALOG PINS

NAME	DESCRIPTION
IREF	TIMING PROGRAM PIN. The VCO center frequency, 1/4 cell delay and the 1F Detect Retriggerable One Shot timing is a function of the current sourced into pin IREF. The current is set by an external resistor, RR, connected from IREF to VCC.
XTAL1, XTAL2	CRYSTAL OSCILLATOR CONNECTIONS. If a crystal oscillator is not desired, XTAL1 may be driven by a TTL signal with XTAL2 open. The frequency must be at twice the data rate.
PD OUT	PHASE DETECTOR OUTPUT. Drives the Loop Filter input.
VCO IN	VCO CONTROL INPUT. Driven by the Loop Filter output.
1FS	1F DETECT SET. Used to program the 1F detect timing with an external resistor, RT, connected from pin 1FS to ground. The 1F Detect period is the sum of the 1/4 cell delay, TQC, plus the Retriggerable One-Shot delay, TOS, and is normally set to 1 1/4 bit cell times.
RF, RS	WINDOW SYMMETRY ADJUST PINS. Provides analog control over the decode window symmetry; typically used to null out any window symmetry offset. A resistor connected from either RF or RS to ground will provide magnitude and direction control. They can be used in conjunction with the digital control port WSD, WS0, and WS1.
PCS	PRECOMP SET. Pin for R-C network to program write precompensation early and late times. Connect the capacitor, CPC, to VPA and the resistor, RPC, to either ground.
VPD, VPA	DIGITAL AND ANALOG +5V.
DGND, AGND	DIGITAL AND ANALOG GROUND.

SSI 32D534
Data Synchronizer/
MFM ENDEC

FUNCTIONAL DESCRIPTION

The SSI 32D534, a high performance data synchronizer and MFM ENDEC, performs data separation, data encoding with optional write precompensation, Preamble detection, and Write Address Mark/Address Mark detection. The interface electronics and the architecture of the SSI 32D534 has been optimized for use as a companion device to the SSI 32C452 or AIC 010 type Storage Controllers. It includes a zero phase restart PLL for fast acquisition, a crystal reference oscillator, the write precompensation delay line, a multiplexed Read/Reference clock output, and a bidirectional NRZ data interface.

Data rate is programmed with a single 1% external resistor, RR, connected from pin IREF to VCC, given by:

$$RR = \frac{30.67}{DR} - 0.5\ (K\Omega)$$

Where: DR = Data Rate in Mbits/sec.
RR = KΩ

Resistor RR establishes a reference current which controls the VCO center frequency, the phase detector gain, the 1/4 cell delay and, indirectly, the decode window shift (RF, RS).

The internal crystal reference oscillator, operating at twice the data rate, generates the standby reference input to the PLL. This minimizes the frequency step and the associated acquisition time encountered when locking the PLL onto Encoded Read Data. Additionally, in non-Read modes the RRC (Read Reference Clock) output is generated from the reference oscillator divided by two. A series resonant crystal at twice the data rate should be used. If a crystal oscillator is not desired, an external TTL compatible reference may be applied to XTAL1 with XTAL2 open.

READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input, a high level (Read Mode) selects the $\overline{RD}$ input and a low level selects the crystal reference oscillator.

The SSI 32D534 provides two sync modes for controlling the PLL locking sequence, Auto Sync and Direct Sync. The Auto Sync mode provides preamble search and address mark detection while the Direct Sync mode provides direct control over the input to the PLL. These modes extend the applicability of the SSI 32D534 to a variety of controller and interface requirements. The appropriate mode should be selected for the given application, see Table 1.

TABLE 1: Mode Control

MODE	WG	RG	EWC/$\overline{ASM}$
Idle	0	0	X
Read (Auto Sync)	0	1	0
Read (Direct Sync)	0	1	1
Write (Disable Precomp)	1	0	0
Write (Enable Precomp)	1	0	1
Illegal	1	1	X

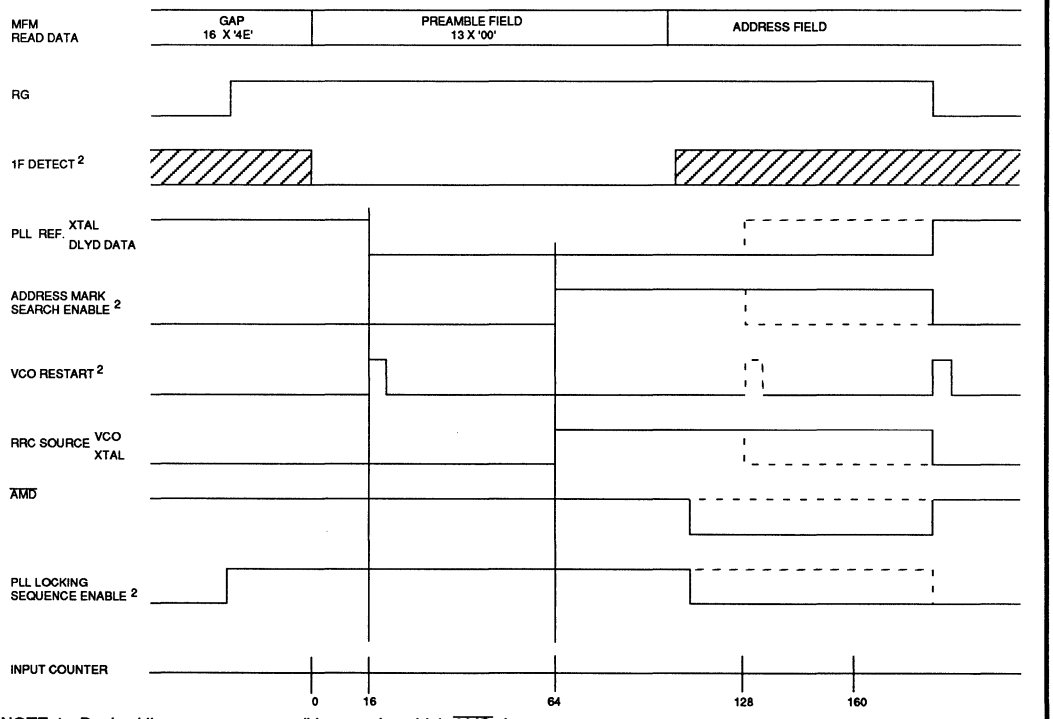
(X = Don't Care)

AUTO SYNC MODE

The Auto Sync mode, typically used for Soft Sector formats, activates the preamble search and address mark detection circuitry. As depicted in Figure 1, the SSI 32D534 requires16 continuous preamble bits before switching the reference input to the PLL, 64 preamble bits before switching the Read Reference Clock to the VCO clock divided by two, and a detected address mark prior to an additional 64 input bits in order to enter the Read Mode. This sequence repeats after 160 input bits until Read mode is successfully entered or until RG is cancelled.

When RG transitions high, the following PLL locking sequence begins:

a) PREAMBLE SEARCH: The SSI 32D534 searches for 16 continous preamble bits. The Preamble fields consist of a stream of MFM encoded 0's. The sum of the delays from the Re-triggerable One



NOTE 1: Dashed lines represent conditions under which $\overline{AMD}$ does not occur.
NOTE 2: Representations of internal signals

FIGURE 1: Auto Sync Mode Waveform Diagram

Shot, TOS, and the 1/4 Cell Delay, TQC, is set to 1 1/4 bit cell times with the external programming resistor, RT. The Preamble stream has a pulse rate of 1 bit cell time (2F frequency) which continuously resets the one-shot while a 2 bit cell period (1F frequency) allows the one-shot to time out producing a 1F detect pulse. The 1F detect pulse resets the Input counter and the search is started over.

b) PLL ACQUISITION: When 16 continuous preamble '0' bits are detected, the reference input to the PLL is switched from the crystal reference oscillator to the DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, PLL acquisition begins, and the VCO clock divider is reset. When 64 '0' preamble bits are detected, the Read Reference Clock output (RRC) is switched to the VCO clock divided by 2, and the Address Mark Detection circuitry is enabled. If a 1F detect pulse occurs before 64 preamble bits are detected, the PLL is locked back to the crystal reference oscillator, the RRC output is switched to the crystal reference oscillator divided by 2, the Input Counter is reset, and the sequence is restarted. No short duration glitches will occur during this switching.

c) ADDRESS MARK DETECTION: The circuit searches for the occurrence of the Address Mark. The 1F detect circuitry remains active so that, during the search, once a 1F is detected, the Address Mark must be found within the next five counts of the Read Data input pulses. If an Address Mark is detected, prior to the Input Counter reaching count 128, the $\overline{WAM}/\overline{AMD}$ output is latched low, the PLL training sequence is terminated, and

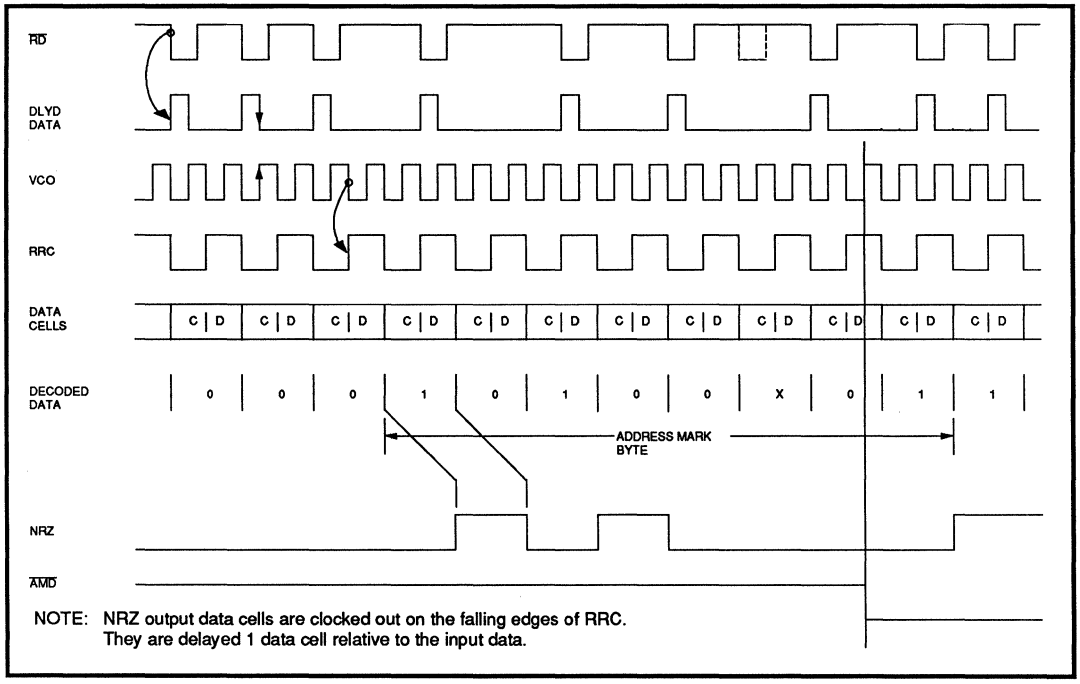


FIGURE 2: Address Mark Detection and NRZ Waveform Diagram

AUTO SYNC MODE (Continued)

the Read Mode is entered allowing the data field to be read. If the input counter reaches count 128 before the Address Mark is detected, the PLL is locked back to the crystal reference oscillator, the RRC output is switched to the crystal reference oscillator divided by 2, and the PLL training sequence is restarted when the Input Counter reaches count 160. Figure 2 depicts the Address Mark detection sequence.

DIRECT SYNC MODE

Direct Sync Mode disables the preamble search and address mark detection circuitry. It allows the PLL to be controlled directly by RG, for Hard Sector format operation.

When RG transitions high, the reference input to the PLL is switched from the crystal reference oscillator to DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, PLL acquisition begins, the VCO clock divider is reset, and the RRC output is switched to the VCO clock divided by 2.

Read Gate, RG, is an asynchronous input and may be initiated or terminated at any position on the disk. Terminating RG locks the PLL to the crystal reference oscillator and switches the RRC output to the crystal reference oscillator divided by 2.

In non-Read modes the PLL is locked to the crystal reference oscillator. This forces the VCO to run at a frequency that is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When the reference input to the PLL is switched, the VCO is stopped momentarily and then restarted in an accurate phase alignment with the next PLL reference input pulse and the VCO clock divider is reset. By minimizing the phase misalignment in this manner (phase error $\leq \pm 0.5$ rads), the acquisition time is substantially reduced.

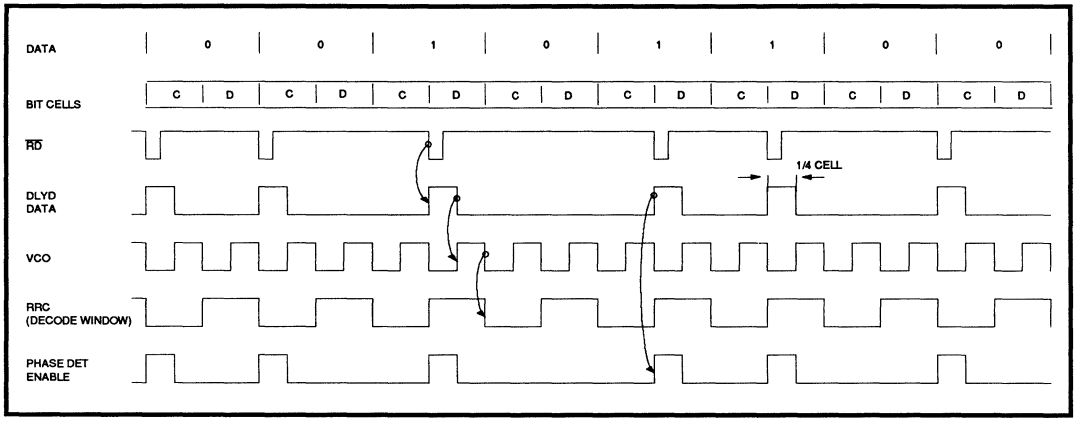
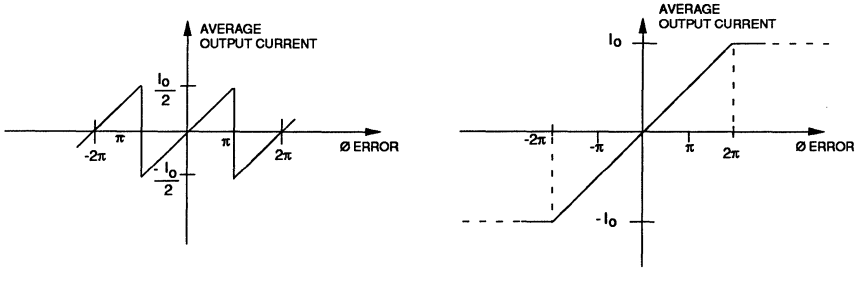


FIGURE 3: Data Synchronization Waveform Diagram

DIRECT SYNC MODE (Continued)

The SSI 32D534 employs a dual mode phase detector; harmonic in Read mode and non-harmonic in Idle/ Write modes. The harmonic phase detector only updates the PLL with each occurrence of a DLYD DATA pulse. This allows the PLL to remain phase locked to actual Read Data. The rising edge of DLYD DATA enables the phase detector and the falling edge is phase compared to the rising edge of the VCO. As depicted in Figure 3, DLYD DATA is a 1/4 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of $\overline{RD}$. In Idle/Write modes, both phase and frequency lock (non-harmonic) to the crystal reference oscillator is accomplished by continuously enabling the phase detector. With both phase and frequency lock to the crystal reference oscillator and the zero phase restart acquisition technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. Figure 4 depicts the average output current as a function of the input phase error (relative to the VCO period).



NOTE 1: Io is the magnitude of the charge pump current.
NOTE 2: Phase error is relative to the VCO period.

FIGURE 4: Phase Detector Transfer Function

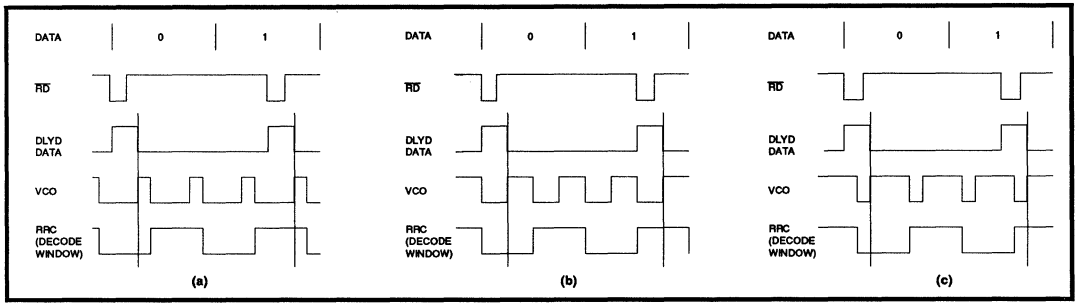


FIGURE 5: Decode Window a) Early, b) Normal, c) Late

DIRECT SYNC MODE (Continued)

An accurate and symmetrical decode window is developed from the VCO clock. The rising edges of the VCO clock are phase locked to the falling edges of DLYD DATA as shown in Figure 3. The decode window is then generated from the falling edges of the VCO clock. By utilizing a fully integrated symmetrical VCO running at twice the data rate, the decode window is ensured to be accurate and centered symmetrically about the falling edges of DLYD DATA. The accuracy of the 1/4 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of the decode window.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the DLYD DATA pulse within the decode window. This powerful capability easily facilitates automatic calibration, window margin testing, error recovery, and systematic error cancellation. For enhanced disk drive testability and error recovery, decode window control is provided via a µP port (WSL, WSD, $\overline{WS0}$, $\overline{WS1}$) as described in Table 2.

Window shifts in the range of ±1.5% to ±7.5% of TORC are easily programmed by latching the appropriate control word into the Window Shift Register with the WSL pin. Shifts in the positive or negative directions result in early or late decode windows respectively, as depicted in Figure 5. For applications not utilizing this feature, WSL should be tied to ground, while WSD, $\overline{WS0}$ & $\overline{WS1}$ should be left floating. Additionally, for small systematic error cancellation a resistor, R, connected from either RS (Early) or RF (Late) to ground will provide analog control over the decode window. The magnitude of this shift, Tsa, is determined by :

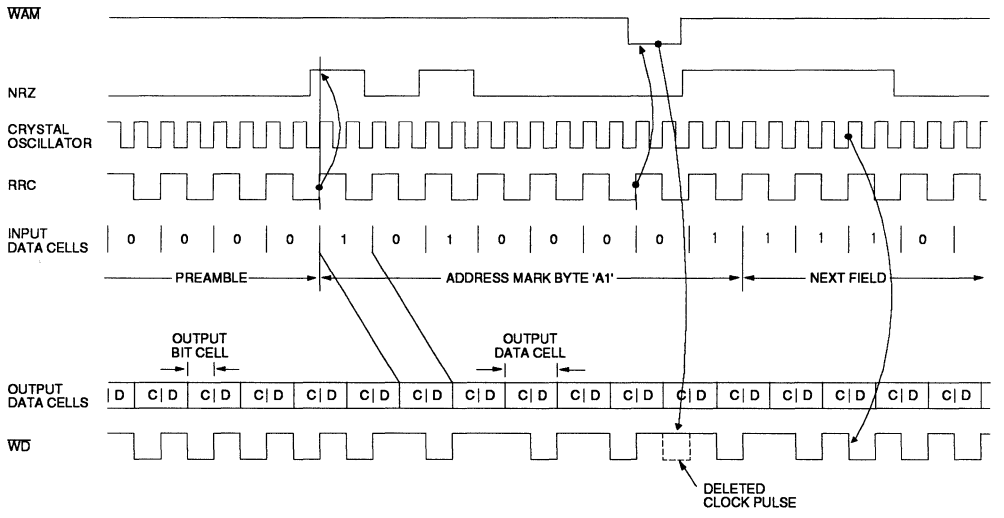
$$Tsa = \frac{(0.25)TORC}{R + 0.7}$$

Where: R is in KΩ.

Pins RF and RS are intended to be used as a trim and should be restricted to ± 1.5% window shifts. They can be used in conjunction with the digital control port.

TABLE 2: Decode Window Symetry Control

Ts, NOMINAL WINDOW SHIFT	WSD	$\overline{WS1}$	$\overline{WS0}$
0	0	1	1
+TS1	0	1	0
+TS2	0	0	1
+TS3	0	0	0
0	1	1	1
–TS1	1	1	0
–TS2	1	0	1
–TS3	1	0	0



NOTE 1: NRZ and WAM inputs are clocked in on the rising edges of RRC (input data cell boundaries).
NOTE 2: WD output data cells are defined in terms of the falling edges of RRC. They are delayed 1 1/2 data cells relative to the input data cells.

FIGURE 6: Write Address Mark /Address Write Data Waveform Diagram

WRITE OPERATION

In the Write Mode, the SSI 32D534 converts NRZ data (from the Controller) into MFM data, for storage onto the disk. It performs write precompensation, if enabled, and inserts Address Marks as requested. Serial NRZ data is clocked into the SSI 32D534 and latched on defined data cell boundaries. NRZ data must be synchronous with the rising edges of the RRC clock output. During a Write Data Operation, the SSI 32D534 processes data and ECC fields and in a Write Format Operation, Address Marks, Preamble, ECC, Gaps, and ID fields are processed. Write Gate is an asynchronous input and may be initiated or terminated at any position on the disk. MFM encoded output write data, $\overline{WD}$, is delayed from input NRZ data by 1.5 Data Cells. For the successful completion of a write operation, Write Gate, WG, should not be terminated prior to the last output Write Data pulse.

Address Marks can be inserted into the MFM encoded data stream, $\overline{WD}$, with the pin $\overline{WAM}$ (Write Address Mark). When $\overline{WAM}$ is asserted, the data/ clock pulse in the corresponding bit cell of the MFM encoded data stream is deleted. This allows specially encoded sequences (illegal MFM patterns) to be encoded using the SSI 32D534. $\overline{WAM}$ is synchronous with the RRC clock and is internally delayed by 0.5 data cells. To generate the missing clock A1 Address Mark pattern, $\overline{WAM}$ is asserted during the sixth data cell of the NRZ A1 data pattern. Figure 6 depicts the Address Mark generation sequence.

Write Precompensation reduces the effect of intersymbol interference caused by the proximity of magnetic transitions on the disk media. The interference is caused by specific data patterns where flux reversals are positioned closely together. Compensation consists of shifting write data pulses in time to counteract for the shifting normally exhibited in the corresponding Read Back signal. When Precompensation is enabled, see Table1, the SSI 32D534 recognizes these data patterns and appropriately shifts the write data pulses. Table 3 describes the Precompensation Algorithm relative to the current data bit, n, to be written.

WRITE OPERATION (Continued)

The SSI 32D534 utilizes an internal analog delay line to time shift the encoded write data pulses. The magnitude of the time shift, TPC, is determined by the external RC network (RPC, CPC) at pin PCS (Precomp Set) and is given by:

TPC = 0.21 x RPC x (CPC + 2pF),
with RPC in KΩ & CPC in pF

An Early/Late compensated bit results in a pulse shifted TPC seconds before/after the nominal unshifted pulse position.

TABLE 3: Write Precompensation Algorithm

BIT n-2	BIT n-1	BIT n	BIT n+1	COMPENSATION Bit n
X	0	1	1	LATE
X	1	1	0	EARLY
1	0	0	0	LATE
0	0	0	1	EARLY

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
Storage Temperature	-65 to +150	°C
Junction Operating Temperature	0 to +130	°C
Supply Voltage, VCC	-0.5 to 7	Vdc
Voltage Applied to Logic inputs	-0.5 to VCC + 0.5	Vdc

ELECTRICAL CHARACTERISTICS

Unless otherwise specified 4.75 ≤ VCC ≤ 5.25V, 0°C ≤ TA ≤ 70°C, 5MHz ≤ 1/TORC ≤ 10 MHz; 10 MHz ≤ 1/TVCO ≤ 20 MHz.

PARAMETER		CONDITIONS	MIN	MAX	UNIT
VIH	High Level Input Voltage		2.0		V
VIL	Low Level Input Voltage			0.8	V
IIH	High Level Input Current	VIH = 2.7V		20	µA
IIL	Low Level Input Current	VIL = 0.4V		-0.36	mA
VOH	High level Output Voltage	IOH = -400µA	2.7		V
VOL	Low Level Output Voltage	IOL = 4mA		0.5	V
ICC	Power Supply Current	All outputs open		180	mA
	Power Dissipation	Tj = 130°C		850	mW

CONTROL CHARACTERISTICS (Refer to Figure 7)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
TSWS	$\overline{WS0}$, $\overline{WS1}$, WSD Set Up Time		15		ns
THWS	$\overline{WS0}$, $\overline{WS1}$, WSD Hold Time		5		ns
TSERG	Set up time EWC to RG		10		ns
THERG	Hold time EWC from RG		0		ns
TSEWG	Set up time EWC to WG		0		ns
THEWG	Hold time EWC from WG		0		ns

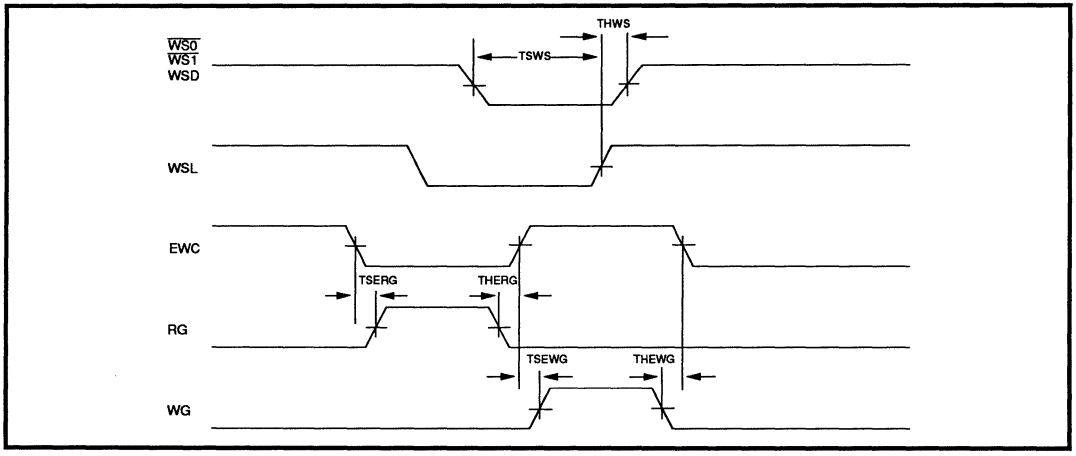


FIGURE 7: Control Timing

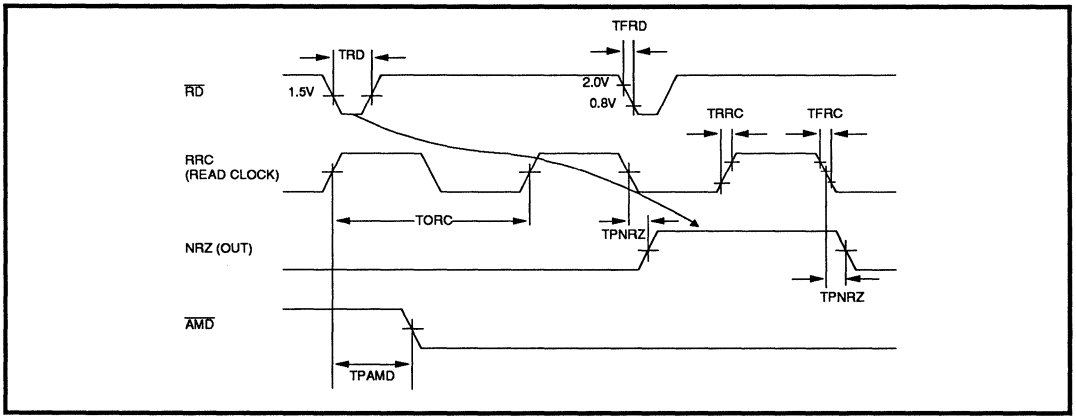


FIGURE 8: Read Timing

ENDEC CHARACTERISTICS

READ MODE (Refer to Figure 8)

PARAMETERS		CONDITIONS	MIN	MAX	UNIT
TRD	Read Data Pulse Width		20	TORC - 40	ns
TFRD	Read Data Fall Time	2.0 to 0.8V		20	ns
TRRC	Read ClockRise Time	0.8 to 2.0V; $C_L \leq 15pF$		10	ns
TFRC	Read Clock Fall Time	2.0V to 0.8V; $C_L \leq 15pF$		8	ns
TPNRZ	NRZ (out) Propagation Delay		-20	+10	ns
TPAMD	AMD Propagation Delay		$\frac{TVCO}{2}$	$\frac{TVCO}{2}+15$	ns
TQC	1/4 Cell Delay Accuracy	TQC = 0.25 TORO	0.8TQC	1.2TQC	sec
TOS	Retriggerable One-shot Delay Accuracy	TOS = RT (8.96E-12) 12K ≤ RT ≤ 36K	0.84TOS	1.16TOS	sec
TORC	Read Clock Period		0.8TORO	1.2TORO	ns

WRITE MODE (Refer to Figure 9)

PARAMETERS		CONDITIONS	MIN	MAX	UNIT
TWD	Write Data Pulse Width	$C_L \leq 15pF$	$\frac{TORO}{2}$ - 2TPC-10	$\frac{TORO}{2}+10$	ns
TPC	PrecompensationTime Shift Magnitude Accuracy	2K ≤ RPC ≤ 6K 15pF ≤ CPC ≤ 36 pF See Note	0.8TPC	1.2 TPC	sec
TFWD	Write Data Fall Time	2.0V to 0.8V; $C_L \leq 15pF$		8	ns
TRRO	Reference Clock RiseTime	0.8 to 2.0V; $C_L \leq 15pF$		8	ns
TFRO	Reference Clock Fall Time	2.0V to 0.8V; $C_L \leq 15pF$		8	ns
TSNRZ	NRZ(in) Set Up Time		25		ns
THNRZ	NRZ(in) Hold Time		7		ns
TSWAM	$\overline{WAM}$ Set-up Time		25		ns
THWAM	$\overline{WAM}$ Hold Time		7		ns

Note: TPC=0.21(RPC)(CPC+2pF)

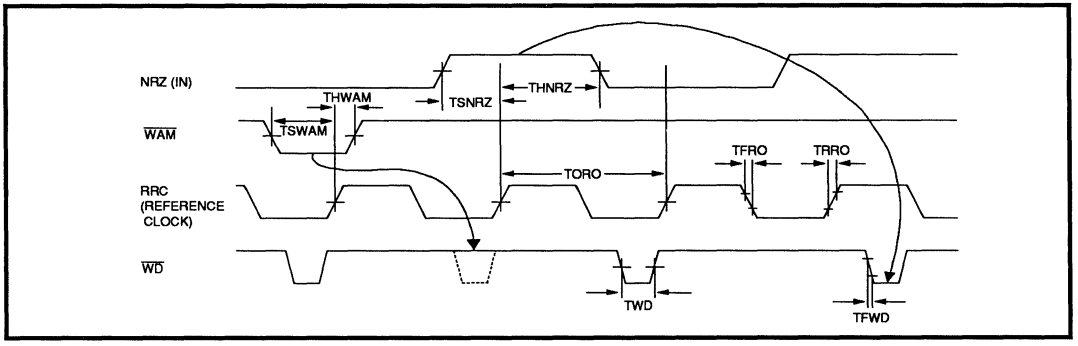


FIGURE 9: Write Timing

DATA SYNCHRONIZATION CHARACTERISTICS

PARAMETERS		CONDITIONS	MIN	MAX	UNIT
TVCO	VCO Center Frequency Period	VCOIN = 2.7V, TO = 1.63E - 11(RR+500) VCC = 5.0V, 2400 ≤ RR ≤ 6000Ω	0.78TO	1.22TO	sec
	VCO Frequency Dynamic Range	VCC = 5.0V, 1V≤VCOIN ≤ VCC-0.6V	±27	±40	%
KVCO	VCO Control Gain	1V ≤ VCOIN ≤ VCC-0.6 V, $\omega_0 = 2\pi/TO$	$0.14\omega_0$	$0.20\omega_0$	$\frac{rad}{sec\text{-}volts}$
KD	Phase Detector Gain	KD = 0.308/(RR+500); VCC = 5.0 V, 2400 ≤ RR ≤ 6000Ω	0.83KD	1.17KD	$\frac{A}{rad}$
	KVCO x KD Product Accuracy	2400 ≤ RR ≤ 6000Ω, VCC = 5.0V	-28	+28	%
	VCO Phase Restart Error		-0.5	+0.5	rad
	Decode Window Centering Accuracy			See Note	ns
	Decode Window		$\frac{TORC}{2} - 4$		ns
TS1	Decode Window Time Shift Magnitude	TS1 = 0.015TORC	0.85TS1	1.15TS1	sec
TS2	Decode Window Time Shift Magnitude	TS2 = 0.06TORC	0.90TS2	1.10TS2	sec
TS3	Decode Window Time Shift Magnitude	TS3 = 0.075TORC	0.90TS3	1.10TS3	sec
TSA	Decode Window Time Shift Magnitude	$TSA = \frac{(0.25)TORC}{R+0.7}$; (R in KΩ)	0.65 TSA	1.35TSA	sec

Note: ±(.015TORC+3)

APPLICATION

LOOP FILTER

The element in the phase lock loop which controls the loop dynamics is known as the loop filter. Acquisition time, data margin, and data tracking can be optimized by the loop filter selection. One possible loop filter configuration is shown in Figure 10, where the function of C_1 is as an integrating element. The larger the capacitance of C_1, the longer will be the lock time. If the capacitance is too small, the loop will tend to track high frequency jitter. The role of the resistor R is to reduce the phase shift induced by C_1. This is necessary since the loop will oscillate at the frequency where the gain is unity. The capacitor C_2 will suppress high frequency transients when switching occurs. This capacitor will have a minimal effect of the loop response if it is small compared to C_1 (typically, $C_2 = C_1/10$).

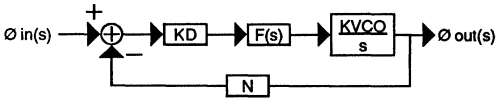
The loop filter transfer function is:

$$F(s) = \frac{Vout}{Iin} = \frac{1 + sRC_1}{sC_1\left(1 + sC_2R + \frac{C_2}{C_1}\right)}$$

if $C_2 < C_1$
then,

$$F(s) = \frac{Vout}{Iin} = \frac{1 + sRC_1}{sC_1}$$

The phase lock loop can be described as:



where,

KD = phase detector gain [A/rad]
F(s) = Filter impedance [V/A]
$\frac{KVCO}{s}$ = oscillator transfer function [rad /volt - sec]
N = ratio of reference input frequency vs. VCO output frequency.

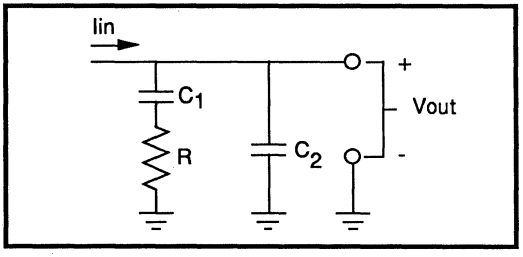


FIGURE 10: Loop Filter

Therefore, the closed loop transfer function is now:

$$T(s) = \frac{Ø\,out(s)}{Ø\,in(s)} = \frac{G(s)}{1 + G(s)H(s)} =$$

$$\frac{KD \times KVCO\left(\frac{1 + sRC_1}{C_1}\right)}{s^2 + s(N \times KD \times KVCO \times R) + \frac{N \times KD \times KVCO}{C_1}}$$

now we can put the characteristic equation (denominator) in the form:

$$s^2 + 2s\zeta\omega_n + \omega_n^2$$

$$\therefore \omega_n^2 = \frac{N \times KD \times KVCO}{C_1} \text{ and } \zeta = \frac{N \times KD \times KVCO \times R}{2\omega_n}$$

which results in:

$$C_1 = \frac{N \times KD \times KVCO}{\omega_n^2}$$

$$R = \frac{2\zeta\omega_n}{N \times KD \times KVCO} \text{ and } C_2 = \frac{C_1}{10}$$

For a $\zeta = 0.8$, the relationship between ω_n and lock time is:

$$\omega_n = \frac{4.5}{\text{lock time}}$$

Therefore, the loop filter components C_1, C_2, and R can be evaluated for a required lock time and coding scheme (N) frequency relationship to the VCO frequency.

With MFM coding:

N = 1, for Øin = reference oscillator
N = 0.5, for Øin = maximum data frequency
N = 0.25 for Øin = minimum data frequency

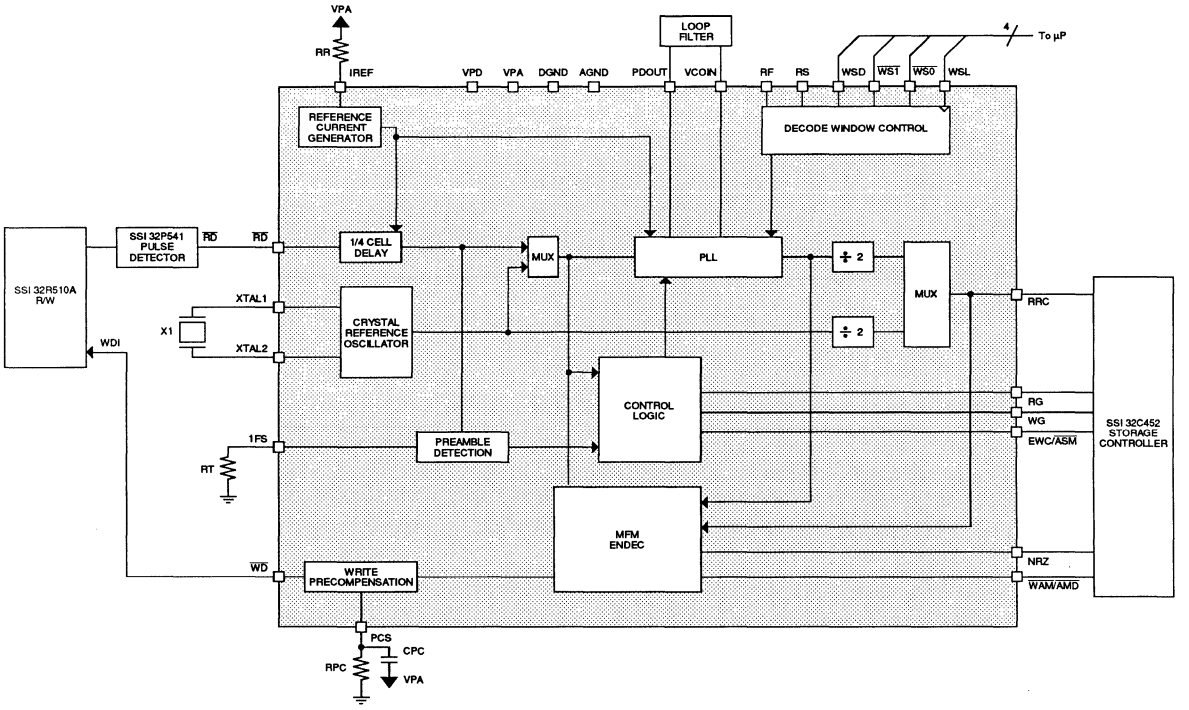


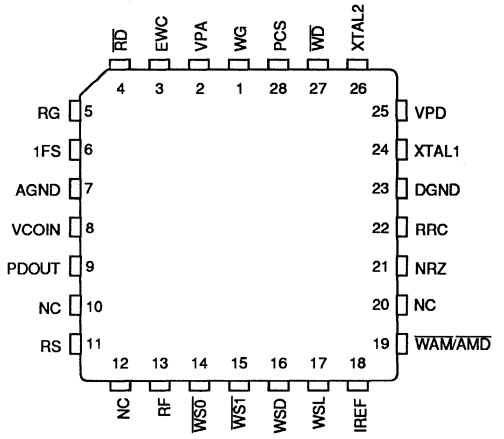
FIGURE 11: Typical Application

Typical External Component Values for a 5 Mbit/Sec. MFM Application:

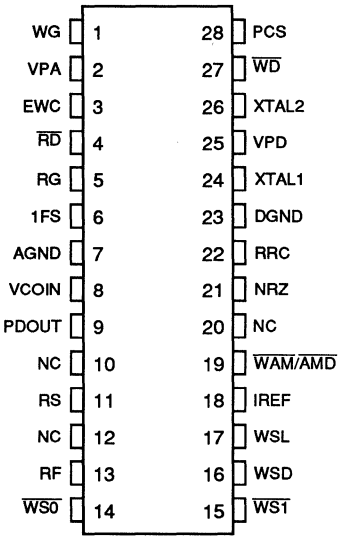
COMPONENT	CONDITIONS	VALUE	UNITS
X1	Series resonant crystal	10	MHz
RR		5.62	KΩ
RT		24.8	KΩ
RPC		2	KΩ
CPC		15	pF
Loop Filter			
R		5.1	KΩ
C_1		270	pF
C_2		33	pF

SSI 32D534
Data Synchronizer/
MFM ENDEC

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



28-pin PLCC



28-pin DIP

THERMAL CHARACTERISTICS: Øja

28-pin PLCC	65°C/W
28-pin PDIP	55°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32D534 28-pin PLCC	SSI 32D534-CH	32D534-CH
SSI 32D534 28-pin PDIP	SSI 32D534-CP	32D534-CP

silicon systems™
14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

SSI 32D535
Data Synchronizer/ 2, 7 RLL ENDEC with Write Precompensation

January, 1988

DESCRIPTION

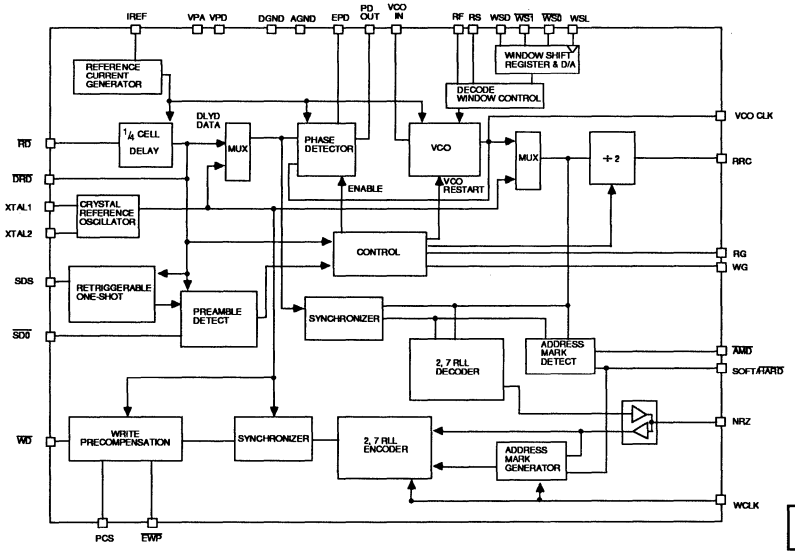
The SSI 32D535 Data Separator provides data recovery, data encoding, and write precompensation for storage systems which employ a 2, 7 RLL encoding format. Data synchronization is performed with a fully integrated high performance PLL. A zero phase restart technique is used to minimize PLL acquisition time. The SSI 32D535 has been optimized for operation as a companion device to the SSI 32C452A and the AIC 010 controllers. The VCO frequency setting elements are incorporated within the SSI 32D535 for enhanced performance and reduced board space. Data rate is established with a single external programming resistor. The SSI 32D535 utilizes an advanced bipolar process technology which affords precise decode window control without the requirement of an accurate 1/4 cell delay or external devices. To enhance disk drive testability, decode window symmetry control is available through a digital µP port and/or two analog pins. This feature can facilitate defect mapping, automatic calibration, systematic error cancellation, window margin testing, and error recovery. The SSI 32D535 requires a single +5V power supply and is available in 32-pin DIP and SOW packages.

FEATURES

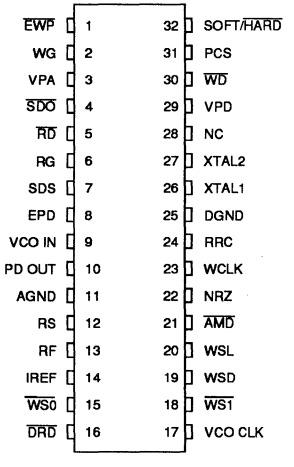
- **Data Synchronizer and 2, 7 RLL ENDEC**
- **Write Precompensation**
- **7.5 to 15 Mbits/sec Operation Programmed with a Single External Resistor**
- **Optimized for Operation with the SSI 32C452A and AIC 010 Controllers**
- **ESDI compatible**
- **Programmable Decode Window Symmetry via a µP Port and/or Analog Pins**
- **Fast Acquisition Phase Locked Loop**
  - **Zero Phase Restart Technique**
- **Fully Integrated Data Separator**
  - **No External Delay Lines or Active Devices Required**
- **Crystal Controlled Reference Oscillator**
- **Hard/Soft Sector Operation**
- **+5V Operation**
- **32-Pin DIP and SOW Packages**

3

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

0188

PIN DESCRIPTIONS

INPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{RD}$	I	READ DATA: Encoded Read Data from the disk drive read channel, active low.
RG	I	READ GATE: Selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the $\overline{RD}$ input and enables the Read Mode/Address Mark Detection sequences. A low level selects the crystal reference oscillator. Pin RG has an internal resistor pull-up.
WG	I	WRITE GATE: Enables the write mode. Pin WG has an internal resistor pull-up.
WSL	I	WINDOW SYMMETRY LATCH: Used to latch the input window symmetry control bits WSD, $\overline{WS0}$ and $\overline{WS1}$ into the internal DAC. An active high level latches the input bits. Pin WSL has an internal resistor pull-up.
WSD	I	WINDOW SYMMETRY DIRECTION: Controls the direction of the optional window symmetry shift. Pin WSD has an internal resistor pull-up.
$\overline{WS0}$	I	WINDOW SYMMETRY CONTROL BIT: A low level introduces a window shift of 1.5 % TORC (Read Reference Clock Period) in the direction established by WSD. Pin $\overline{WS0}$ has an internal resistor pull-up.
$\overline{WS1}$	I	WINDOW SYMMETRY CONTROL BIT: A low level introduces a window shift of 6% TORC (Read Reference Clock Period) in the direction established by WSD. A low level at both $\overline{WS0}$ and $\overline{WS1}$ will produce the sum of the two window shifts. Pin $\overline{WS1}$ has an internal resistor pull-up.
SOFT/$\overline{HARD}$	I	SOFT/$\overline{HARD}$ SECTOR: Selects the address mark and the Preamble field patterns. A high level (Soft Sector) selects a 3T Preamble Field pattern and a non-violating 2, 7 address mark, N7V. A low level (Hard Sector) selects a 4T Preamble Field pattern and disables the address mark circuitry. Pin SOFT/$\overline{HARD}$ has an internal resistor pull-up.
WCLK	I	WRITE CLOCK: Write Clock input. Must be synchronous with the Write Data input on the NRZ Data Port. For small cable delays, WCLK may be connected directly to pin RRC (Read/Reference Clock).
EPD	I	ENABLE PHASE DETECTOR: A low level (Coast Mode) disables the phase detector and allows the VCO to coast. Pin EPD has an internal resistor pull up.
$\overline{EWP}$	I	ENABLE WRITE PRECOMPENSATION: A low level enables Write Precompensation. Pin $\overline{EWP}$ has an internal resistor pull-up.

PIN DESCRIPTIONS (Cont.)

OUTPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{WD}$	O	WRITE DATA: Encoded write data output, active low.
RRC	O	READ/REFERENCE CLOCK: A multiplexed clock source used by the controller. In the read mode, this clock is the VCO frequency divided by two (1/TORC) and in the write mode it is the crystal reference frequency divided by two (1/TORO). No short clock pulses are generated during a mode change.
$\overline{AMD}$	O	ADDRESS MARK DETECT: In the soft sector Read Mode, a latched low level output indicates that an address mark has been detected. In non-Read modes $\overline{AMD}$ is configured as a high impedance output.
$\overline{SDO}$	O	SYNC DETECT OUTPUT: An active low output that indicates successful detection of the 3T Preamble sync field. THE $\overline{SD0}$ pin is not a TTL level signal.
VCO CLK	O	VCO CLK: An open emitter VCO clock test point. Two external resistors are required to utilize this output, they can be removed during normal operaton for reduced power dissipation.
$\overline{DRD}$	O	DELAYED READ DATA: Test point. The positive edges of this open emitter ouput signal indicate the data bit position. The positive edges of the $\overline{DRD}$ and the VCO CLK signals can be used to estimate window centering. The time jitter of $\overline{DRD}$'s positive edge is an indication of media bit shift. Two external resistors are required to perform this test, they can be removed during normal operation for reduced power dissipation.

BIDIRECTIONAL PINS

NRZ	I/O	NRZ DATA PORT: Read Data output when RG is high and Write Data input when WG is high. In the idle mode NRZ is in a high impedance state.

ANALOG PINS

IREF	I	TIMING PROGRAM PIN: The VCO center frequency and the 1/4 Cell Delay are a function of the current source into pin IREF. The current is set by an external resistor, RR, connected from IREF to VPA.
PCS	I	PRECOMP SET: Used to set the magnitude of the Write Precompensation time shift via an external capacitor, Cp to VPA and an external resistor, Rp to AGND.
XTAL1, XTAL2	I	CRYSTAL OSCILLATOR CONNECTIONS: If a crystal oscillator is not desired, XTAL1 maybe driven by a TTL source with XTAL2 open. The frequency must be at twice the data rate.
PD OUT	O	PHASE DETECTOR OUTPUT: Drives the Loop Filter input.
VCO IN	I	VCO CONTROL INPUT: Driven by the Loop Filter output.

PIN DESCRIPTIONS (Cont.)

OUTPUT PINS (Cont.)

NAME	TYPE	DESCRIPTION
SDS	I	SYNC DETECT SET: Used to program the sync detect retriggerable one-shot timing with an external R-C network. Connect the capacitor, Cd, to VPA and the resistor, Rd, to AGND.
RF, RS	I	WINDOW SYMMETRY ADJUST PINS: Provides analog control over the decode window symmetry; typically used to null out any window symmetry offset. A resistor connected from either RF or RS to AGND will provide magnitude and direction control. They can be used in conjunction with the digital control port WSD, $\overline{WS0}$, $\overline{WS1}$.

POWER

DGND, AGND	I	DIGITAL AND ANALOG GROUND
VPA	I	ANALOG +5V
VPD	I	DIGITAL +5V

OPERATION

The SSI 32D535 is designed to perform data recovery and data encoding in rotating memory systems which utilize a 2, 7 RLL encoding format. In the Read Mode the SSI 32D535 performs Data Synchronization, Sync Field Search and Detect, Address Mark Detect and Data Decoding. In the Write Mode, the SSI 32D535 converts NRZ data into the 2,7 RLL format described in Table 1, performs write precompensation, generates the Preamble Field, and inserts Address Marks as requested. The interface electronics and architecture of the SSI 32D535 have been optimized for use as a companion device to the SSI 32C452A or AIC 010 controllers.

The SSI 32D535 can operate with data rates ranging from 7.5 to 15 Mbits/sec. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/4 cell delay. The value of this resistor is given by:

$$RR = \frac{40.67}{DR} - 0.5\ (K\Omega)$$

where: DR = Data Rate in Mbits/sec.

An internal crystal reference oscillator, operating at twice the data rate, generates the standby reference for the PLL. A series resonant crystal between XTAL1 and XTAL2 should be selected at twice the Data Rate. If a crystal oscillator is not desired, then an external TTL compatible reference may be applied to XTAL1, leaving XTAL2 open.

The SSI 32D535 employs a Dual Mode Phase Detector; Harmonic in the Read Mode and Non-Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DLYD DATA pulse. In the Write and Idle Modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. Figure 1 depicts the average output current as a function of the input phase error (relative to the VCO period).

The READ GATE (RG), and WRITE GATE (WG), inputs control the device mode as described in Table 2. RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the $\overline{RD}$ input and a low level selects the crystal reference oscillator.

In the Read Mode the rising edge of DLYD DATA enables the Phase Detector while the falling edge is phase compared to the rising edge of the VCO. As depicted in Figure 2, DLYD DATA is a 1/4 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of $\overline{RD}$. An accurate and symmetrical decode window is developed from the VCO clock. The decode window is generated from the falling edges of the VCO clock. By utilizing a fully integrated symmetrical VCO running at twice the data rate, the decode window is insured to be accurate and centered symmetrically about the falling edges of DLYD DATA. The accuracy of the 1/4 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of the decode window.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the DLYD DATA pulse within the decode window. This powerful capability easily facilitates defect mappings, automatic calibration, window margin testing, error recovery, and systematic error cancellation. For enhanced disk drive testability and error recovery, decode window control is provided via a µP port (WSL, WSD, $\overline{WS0}$, $\overline{WS1}$) as described in Table 3. In applications not utilizing this

feature, WSL should be connected to ground, while WSD, $\overline{WS0}$, and $\overline{WS1}$ can be left open.

Window shifts in the range of ±1.5% to ±7.5% of TORC are easily programmed by latching the appropriate control word into the Window Shift Register with the WSL pin. Shifts in the positive or negative directions result in early or late decode windows respectively, as depicted in Figure 3. Additionally, for small systematic error cancellation, a resistor, R, connected from either RS (Early) or RF (Late) to ground will provide analog control over the decode window. The magnitude of this shift, TSA is determined by:

$$TSA = 0.125\ TORC\left(1 - \frac{680 + R}{1180 + R}\right)$$

where: R is in ohms

Pins RF and RS are intended to be used as a trim and should be restricted to ±1.5% window shifts. They can be used in conjunction with the digital control port.

The VCO CLK and $\overline{DRD}$ ouputs can be used to estimate window centering and data bit shift. The rising edges of VCO CLK indicate the data detection window edges. The rising edge of $\overline{DRD}$ indicates the data bit position relative to the decode window. Two external resistors are required during such testing. A pull-up resistor of 130Ω should be connected to VPD, while a pull-down resistor of 200Ω should be connected to DGND. The resistors can be removed during normal operation to reduce power dissipation.

In Non-Read Modes, the PLL is locked to the crystal reference oscillator. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset. By minimizing the phase alignment in this manner (phase error ≤ 0.5 rads), the acquisition time is substantially reduced.

The SSI 32D535 provides two sync modes for controlling the PLL locking sequence; Soft Sector and Hard Sector.

SOFT SECTOR MODE

The Soft Sector Mode activates the Preamble Search and Address Mark detection circuitry. As depicted in Figure 4, when RG transitions high, the counter is reset and the SSI 32D535 requires 10 high to low transitions (Preamble '1' bits) before switching the reference input to the PLL, 48 high to low transitions before switching the Read Reference Clock to the VCO clock divided by two and activating the Address Mark Detect circuitry; then it must detect the Address Mark prior to 80 high to low transitions in order to enter the Read Mode. This sequence repeats after 95 input '1' bits until the read mode is successfully entered or until RG is cancelled.

When RG transitions high, the following PLL locking sequence begins:

a) PREAMBLE SEARCH:

The 3T detect circuitry initiates the PLL locking sequence once it has detected 10 consecutive '100' bit groups from the 3T preamble field. The 3T detect timing is set by the sum of the 1/4 cell delay and the retriggerable one-shot delay. The 1/4 cell timing capacitor is included on-chip and its timing is externally set by resistor RR. The retriggerable one-shot timing is externally set by resistor Rd and capacitor Cd. The sum of their delays is set to 3.5 bit cell times. Therefore, a continuous stream of input pulses with a 3T bit cell time pulse rate keeps the one-shot reset, and a 4T or longer bit cell time input period allows the one-shot to time out producing a 4T detect pulse. The 4T detect pulse resets the Input Counter and the search is started over.

b) PLL ACQUISITION:

Once 10 consecutive '100' bit groups are detected, the reference input to the PLL is switched from the crystal reference oscillator to the DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, and PLL acquistion begins. When an additional 38 '100' bit groups are detected, the Read Reference Clock output (RRC) is switched to the VCO clock divided by 2, the 4T Detect circuitry is inhibited, and the Address Mark Detection circuitry is enabled. If a 4T detect pulse occurs

before 48 Preamble '1' bits are detected, then the PLL is locked back to the crystal reference oscillator, the RRC output is switched to the crystal reference oscillator divided by 2, the Input Counter reset, and the sequence is re-started. No short duration glitches will occur at the RRC output during this switching.

c) **ADDRESS MARK DETECTION:**

The circuit searches for the occurrence of the $5EA_{X16}$ Address Mark. If an Address Mark is detected prior to the Input Counter reaching count 80, the correct phase of the RRC is ensured by resetting the n/2 divider, the $\overline{AMD}$ output is latched low, the PLL training sequence is terminated, and the Read Mode is entered allowing the data field to be read. If the Input Counter reaches count 80 before the Address Mark is detected, the PLL is locked back to the crystal reference oscillator, the RRC output is switched to the crystal reference oscillator divided by 2, and the PLL training sequence is restarted when the Input Counter reaches count 96. Figure 5 depicts the Address Mark detection sequence.

HARD SECTOR MODE

In the Hard Sector mode (SOFT/$\overline{HARD}$ = 0) the SSI 32D535 utilizes a 4T (1000) Preamble Field and disables the Preamble Search and Address Mark detection circuitry. It allows the PLL to be controlled directly by RG for Hard Sector format operation. With the absence of an Address Mark, the 4T Preamble Field is utilized to properly set the bit cell alignment boundaries for proper decoding.

When RG transitions high, as depicted in Figure 6, reference input to the PLL is switched from the crystal reference oscillator to DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, and the PLL acquisition begins. When 32 '1' Preamble bits are detected, the RRC output is switched to the VCO clock divided by 2, and the Read Mode is entered allowing the data field to be read.

In the Hard Sector mode, the NRZ output is inverted and will remain low until the data field is read, as shown in Figure 7. Since the Preamble Search circuitry is not utilized, the external one-shot timing components (Cd, Rd) are not required and the SDS pin can be left open.

WRITE OPERATION

In the Write Mode the SSI 32D535 converts NRZ data from the controller into 2, 7 RLL formatted data for storage onto the disk. The SSI 32D535 can operate with a soft or hard sectored disk drive. In the Soft Sector Mode, (SOFT/$\overline{HARD}$ = 1) the device generates a 3T Preamble Field and can insert a N7V Address Mark. The N7V Address Mark is a valid 2, 7 RLL pattern which is not contained in the code set. In the Hard Sector Mode, (SOFT/$\overline{HARD}$ = 0) the device generates a 4T Preamble Field and no Address Mark. Serial NRZ data is clocked into the SSI 32D535 and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK input. The WCLK input is a feature provided for operation in an ESDI application to compensate for large cable delays. In a SCSI or ST506 operation, WCLK is connected directly to the RRC output.

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The SSI 32D535 recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back bit shift. The magnitude of the time shift, TC, is determined by an external R-C network on the PSC pin given by:

$$TC = 0.15\,(RP)(CP)$$

When the ENABLE WRITE PRECOMP, $\overline{EWP}$, input is low the SSI 32D535 performs write precompensation according to the algorithm outlined in Table 4.

SOFT SECTOR MODE

In the Soft Sector Mode, when WRITE GATE (WG), transitions high and the NRZ input is held low, the SSI 32D535 automatically generates the 3T (100) Preamble Field at the WRITE DATA ($\overline{WD}$), output. The 3T Preamble Field will continue to be generated until the first low to high transition on the NRZ line. As shown in Figure 8, the first low to high transition occurs with the second bit '1' of the 5_{16} (0101) in the $5EAx_{16}$ Address Mark generation pattern. To generate the Address Mark, the SSI 32D535 automatically changes the '1' in the eleventh position (see note 3) of the 2, 7 RLL encoded sequence, to a '0'. This generates a pattern of seven zero's followed by two zero's. This unique pattern satisfies the 2, 7 RLL constraints, but will never occur during a normal encoding sequence. The x_{16} of the $5EAx_{16}$ Address Mark generation pattern can be selected, a 'C_{16}' (1100) was utilized in this example.

HARD SECTOR MODE

In the Hard Sector Mode, when WG goes high and the NRZ input is held low, the SSI 32D535 automatically generates the 4T (1000) Preamble Field at the WRITE DATA, $\overline{WD}$, output. Note that in the Hard Sector mode, the NRZ input is inverted, therefore a constant low is equivalent to an '11 . . .' input which generates the 4T '1000 . . . ' Preamble Field. The 4T Preamble Field will be generated between the time WG goes high and the first low to high transition on the NRZ line. The 32D535 requires a minimum of 32 4T (1000) bit groups prior to the data field.

NRZ	2, 7 RLL
10	0100
11	1000
000	000100
010	100100
011	001000
0010	00100100
0011	00001000

TABLE 1: 2, 7 RLL Code Set

WG	RG	MODE
0	0	IDLE
0	1	READ
1	0	WRITE
1	1	ILLEGAL

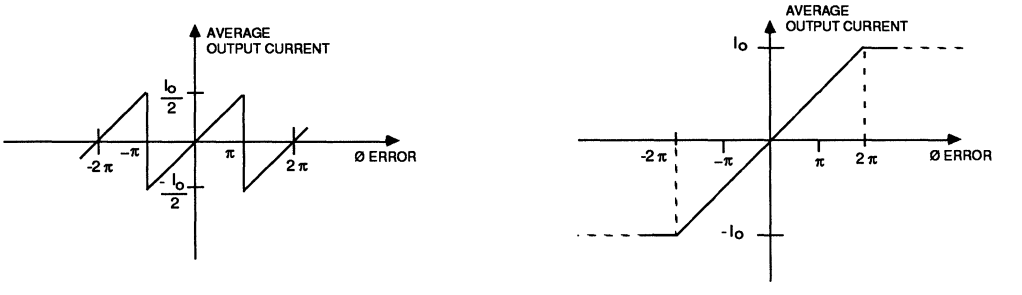
TABLE 2: Mode Control

Ts, NOMINAL WINDOW SHIFT	WSD	$\overline{WS1}$	$\overline{WS0}$
+TS3	0	0	0
+TS2	0	0	1
+TS1	0	1	0
0	0	1	1
-TS3	1	0	0
-TS2	1	0	1
-TS1	1	1	0
0	1	1	1

TABLE 3 : Decode Window Symmetry Control

ENCODED 2, 7 RLL DATA PATTERN							
BIT n - 3	BIT n - 2	BIT n - 1	BIT n	BIT n + 1	BIT n + 2	BIT n + 3	COMPENSATION BIT n
0	0	0	1	0	0	0	none
1	0	0	1	0	0	1	none
1	0	0	1	0	0	0	early
0	0	0	1	0	0	1	late

TABLE 4 : Write Precompensatiom Algorithm



a) HARMONIC MODE

b) NON-HARMONIC MODE

Note 1) Io is the magnitude of the charge pump current.
2) Phase error is relative to the VCO period

FIGURE 1: Phase Detector Transfer Funtion

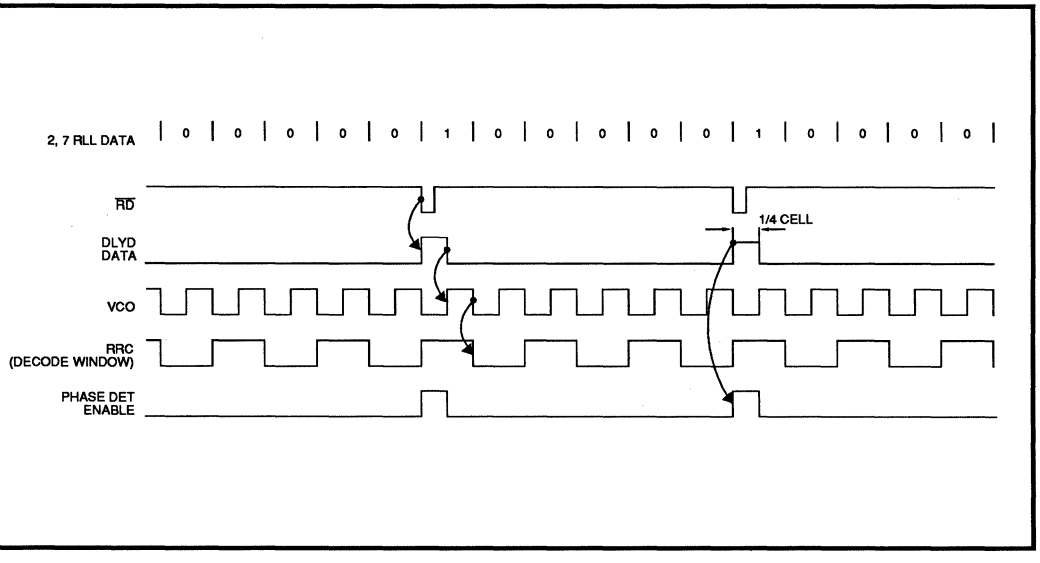


FIGURE 2: Data Synchronization Waveform Diagram

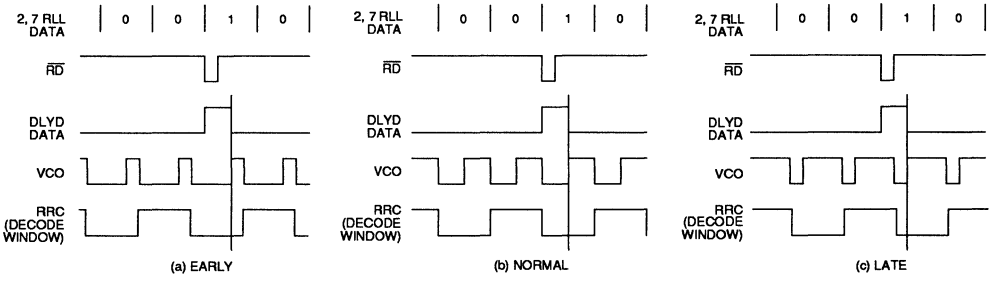


FIGURE 3: Decode Window

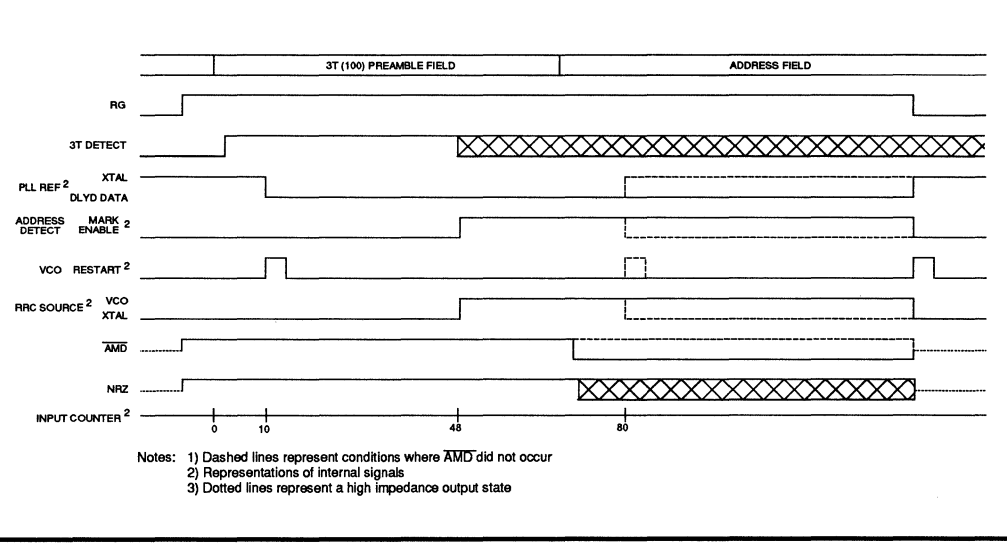


FIGURE 4: Soft Sector Mode Timing Diagram

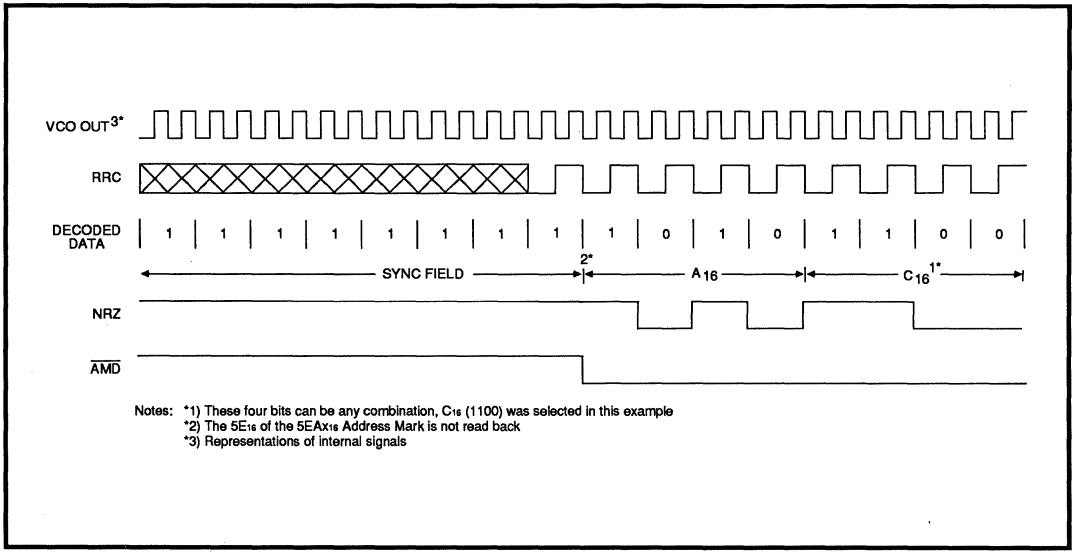


FIGURE 5: Address Mark Detection and NRZ Output Waveform

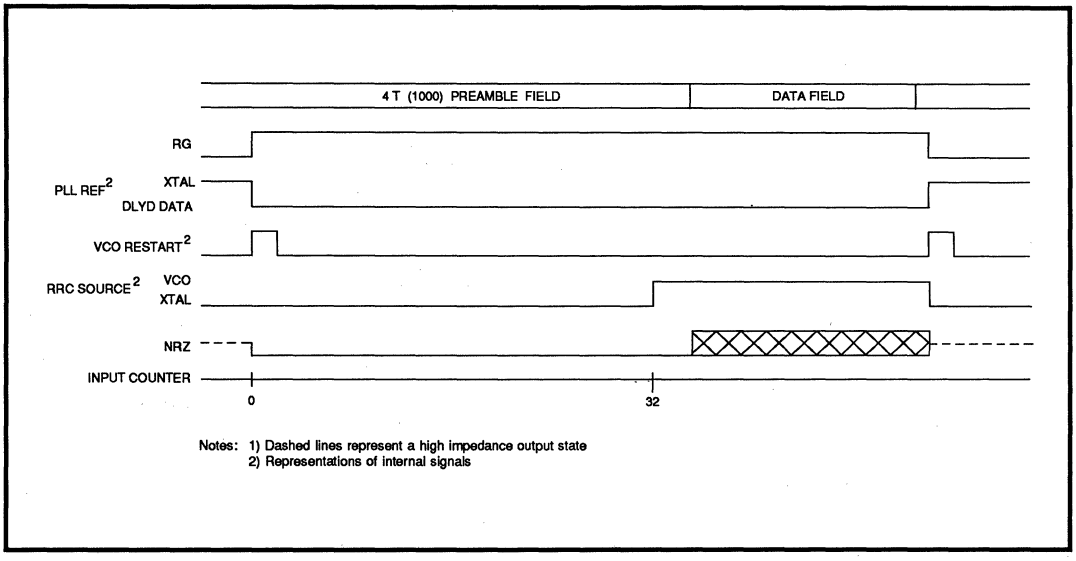


FIGURE 6: Hard Sector Mode Timing Diagram

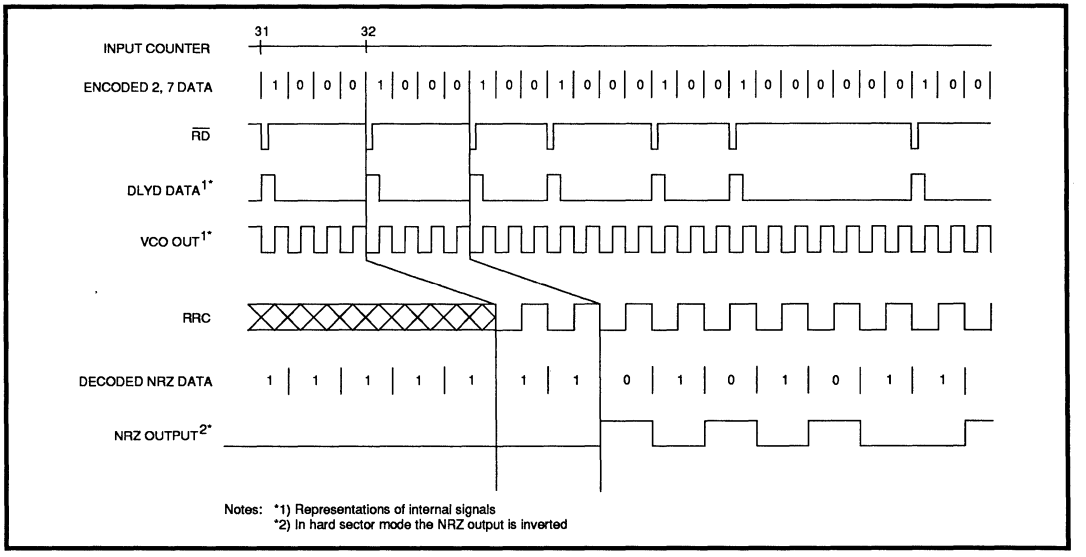


FIGURE 7: Hard Sector Mode Decode Timing

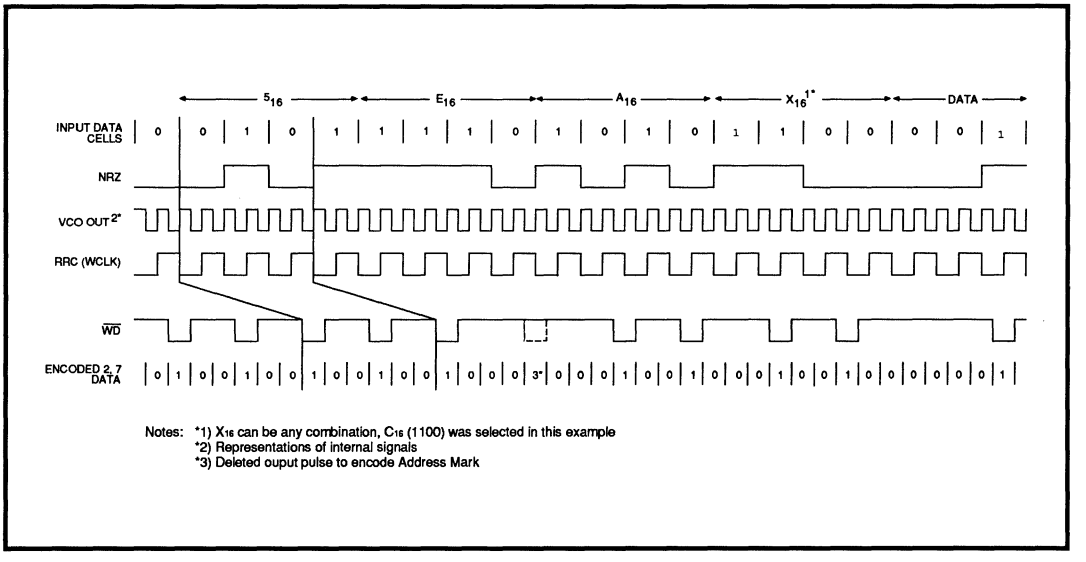


FIGURE 8: Write Address Mark Generation

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATINGS	UNIT
Storage Temperature	-65 to +150	° C
Ambient Operating Temperature, Ta	0 to +70	° C
Junction Operating Temperature, Tj	0 to +130	° C
Supply Voltage, VCC	-0.5 to 7	Vdc
Voltage Applied to Logic inputs	-0.5 to VCC +0.5	Vdc
Maximum Power Dissipation	950	mW

DC ELECTRICAL CHARACTERISTICS - unless otherwise specified, 4.75V < VCC < 5.25V, Ta = 0°C to 70°C, 7.5 MHz < 1/TORC < 15 MHz, 15 MHz < 1/TVCO < 30 MHz

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TTL Inputs:					
VIH, High Level Input Voltage		2.0			V
VIL, Low Level Input Voltage				0.8	V
IIH, High Level Input Current	VIH = 2.7V			20	µA
IIL, Low Level Input Current	VIL = 0.4V			-0.36	mA
TTL Outputs:					
VOH, High Level Output Voltage	IOH = -400 µA	2.7			V
VOL, Low Level Output Voltage	IOL = 4 mA			0.5	V
Test Point Outputs: $\overline{DRD}$, VCO CLK (See Figure 12)					
VOH, High Level Ouput Voltage	RL= 130Ω to VPD, 200Ω to DGND	VPD-0.720			V
VOL, Low Level Output Voltage	RL= 130Ω to VPD, 200Ω to DGND			VPD - 1.625	V
ICC, Power Supply Current	All outputs open			180	mA

DYNAMIC CHARACTERISTICS AND TIMING

READ MODE (See figure 9)

TRD, Read Data Pulse Width		20		TORC-40	ns
TFRD, Read Data Fall Time	2.0V to 0.8V, CL ≤ 15 pF			15	ns
TRRC, Read Clock Rise Time	0.8V to 2.0V, CL ≤ 15pF			8	ns
TFRC, Read Clock Fall Time	2.0V to 0.8V, CL ≤ 15pF			5	ns

READ MODE (Cont.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TPNRZ, NRZ (out) Propagation Delay		-15		15	ns
TPAMD, $\overline{AMD}$ Propagation Delay		-15		15	ns
1/4 Cell + Retriggerable One-Shot Detect Stability	4.5V < VCC < 5.5V	-4		+4	%
1/4 Cell + Retriggerable One-Shot Delay*	TD = 6.14(RR +0.5) + 0.172Rd(Cd +11.5) RR = KΩ Rd = KΩ Cd = 68 pF to 100 pF	0.89TD		1.11TD	ns
Note: * = Excludes External Capacitor and Resistor Tolerances					

WRITE MODE (See Figure 10)

PARAMETER	CONDITIONS	MIN	MAX	UNIT
TWD, Write Data Pulse Width	CL ≤15 pF	(TORO/2)-12	(TORO/2) +12	ns
TFWD, Write Data Fall Time	2.0V to 0.8V, CL ≤ 15 pF		8	ns
TOWC Write Data Clock Repetition Period		TORO-12	TORO +12	ns
TRWC Write Data Clock Rise Time	0.8V to 2.0V		10	ns
TFWC Write Data Clock Fall Time	2.0V to 0.8V		8	ns
TSNRZ, NRZ (in) Set Up Time		20		ns
THNRZ, NRZ (in) Hold Time		7		ns
TWDC Compensated Write Data Pulse Width	CL ≤ 15 pF	(TORO/2)-2TC-12		ns
TE, TL Write Data Compensation Accuracy	TC = 0.15(Rp)(Cp) Cp = 15 pF to 36 pF	0.8TC	1.2TC	ns

DATA SYNCHRONIZATION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TVCO VCO Center Frequency Period	VCO IN = 2.7V TO = 1.23E - 11(RR +500) VCC = 5.0V	0.8TO		1.2TO	sec
VCO Frequency Dynamic Range	1.0V ≤ VCO IN ≤ VCC -0.6V VCC = 5.0V	±27		±40	%

DATA SYNCHRONIZATION (Cont.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
KVCO	VCO Control Gain	$\omega o = 2\pi / TO$ $1.0V \leq VCO\ IN \leq VCC - 0.6V$	$0.14\omega o$		$0.20\omega o$	$\frac{rad}{sec\text{-}V}$
KD	Phase Detector Gain	KD = 0.309 / (RR + 500) VCC = 5.0V	0.83KD		1.17 KD	A/rad
	KVCO x KD Product Accuracy		-28		+28	%
	VCO Phase Restart Error		-0.5		+0.5	rad
	Decode Window Centering Accuracy				± (0.01 TORC + 2)	ns
	Decode Window		(TORC/2) -2			ns
TS1	Decode Window Time Shift Magnitude	TS1 = 0.015 TORC	0.85 TS1		1.15 TS1	sec
TS2	Decode Window Time Shift Magnitude	TS2 = 0.06 TORC	0.90 TS2		1.1 TS2	sec
TS3	Decode Window Time Shift Magnitude	TS3 = 0.075 TORC	0.90 TS3		1.1TS3	sec
TSA	Decode Window Time Shift Magnitude	$TSA = 0.125\ TORC\left(1 - \frac{680 + R}{1180 + R}\right)$ with: R in ohms	0.65 TSA		1.35TSA	sec

CONTROL CHARACTERISTICS (See figure 11)

TSWS, $\overline{WS0}$, $\overline{WS1}$, WSD Set Up Time		50			ns
THWS, $\overline{WS0}$, $\overline{WS1}$, WSD Hold Time		0			ns
RG, WG, SOFT/$\overline{HARD}$ Time Delay				100	ns

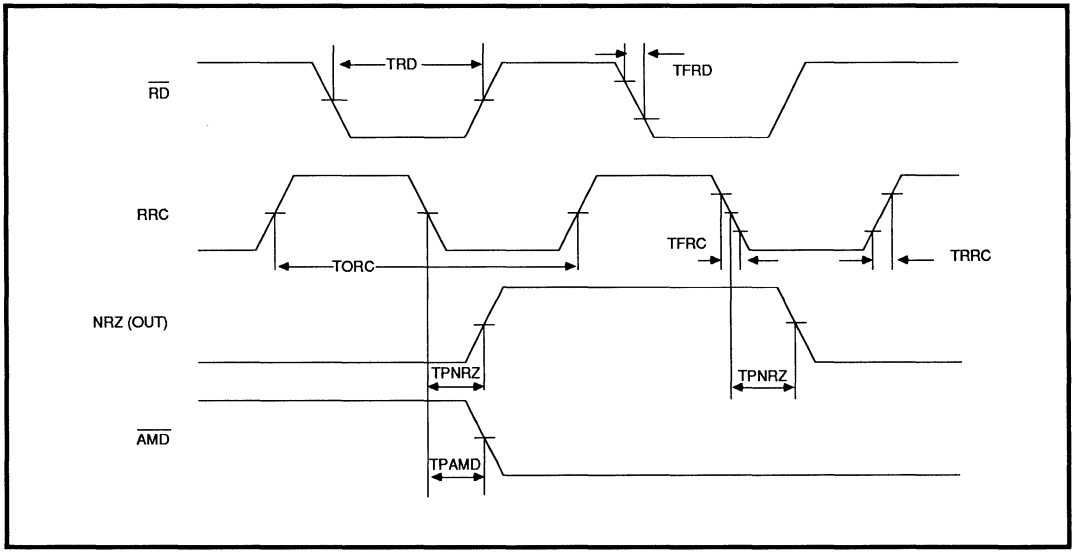


FIGURE 9: Read Timing

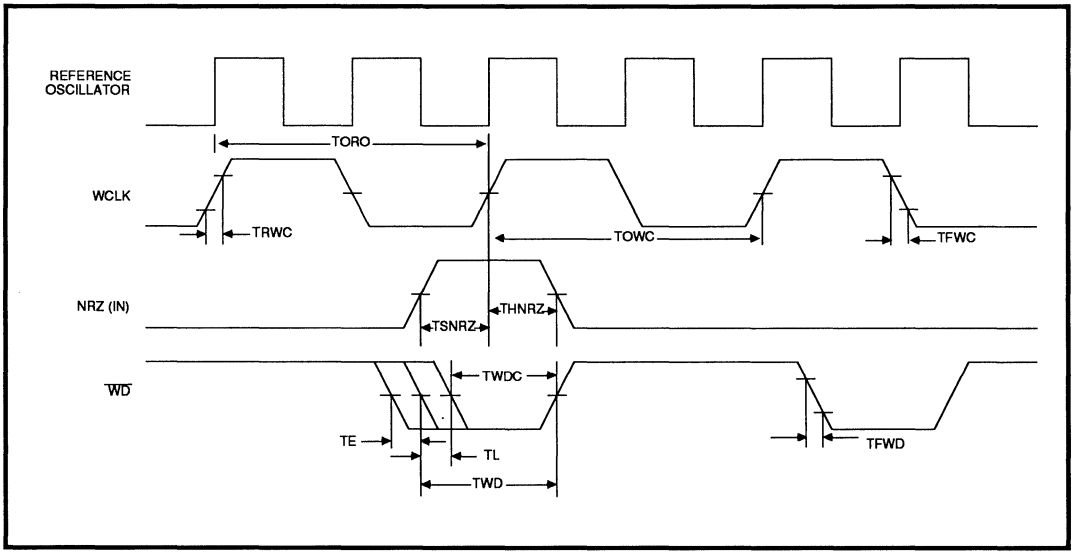


FIGURE 10: Write Timing

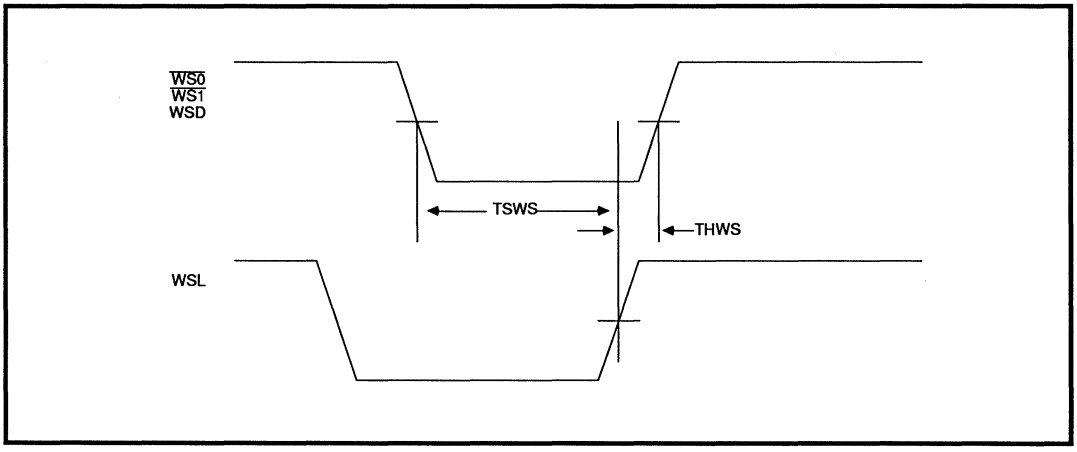


FIGURE 11: Control Timing

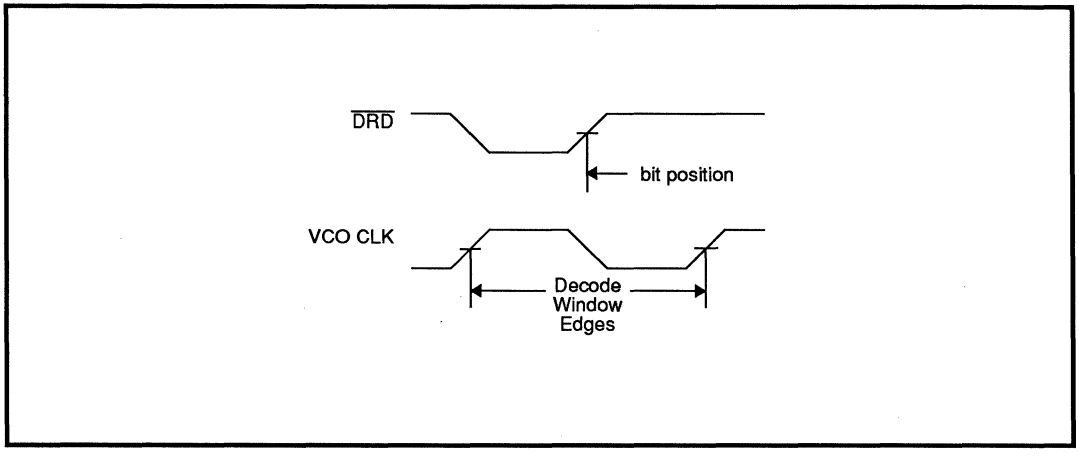
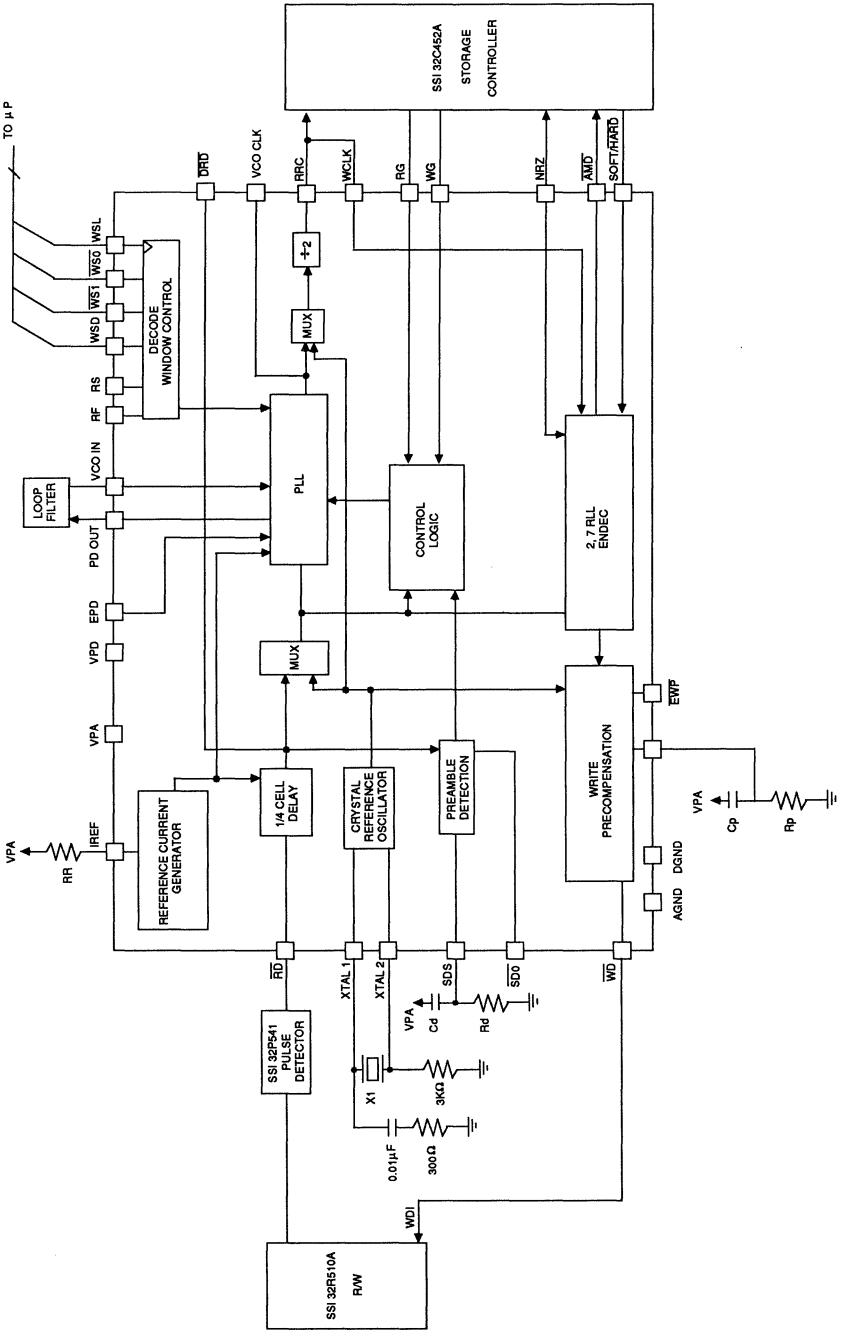


FIGURE 12: Test Point Timing



TYPICAL SSI 32D535 APPLICATION

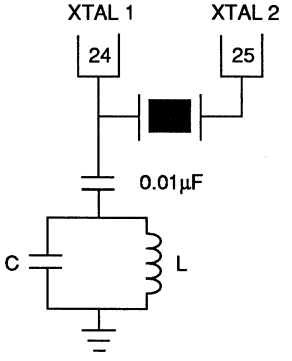
APPLICATIONS INFORMATION

REFERENCE OSCILLATOR

An internal reference oscillator, operating at twice the data rate, generates the standby reference for the PLL. A series resonant crystal between XTAL1 and XTAL2, should be selected at twice the Data Rate. If a crystal oscillator is not desired, then an external TTL compatible reference may be applied to XTAL1, leaving XTAL2 open.

An R-C network is employed on the demonstration board for operation with the crystal oscillator. The purpose of this network is to minimize the coupling of noise into the clock. The 3 KΩ resistor from XTAL2 to ground helps to speed up the oscillator transitions, while the R-C network from XTAL1 to ground lowers the impedance to reduce capacitive coupling effects. In applications utilizing a TTL compatible reference signal, this network should be removed.

If it is desired to operate a crystal at a non-fundamental or harmonic frequency, then the following network is suggested:



$$\omega_o = 2\pi F_o = \frac{1}{\sqrt{LC}}$$

$$Q_o = \omega_o \, C \, Rin$$

The typical input impedance looking into XTAL1 is approximately Rin = 250Ω. It is recommended to design the value of Q_o at approximately 10 to 15. Therefore, a resonant frequency of F_o = 20 MHz would result in L ≅ 0.16 μH and C ≅ 380 pF.

LOOP FILTER

The performance of the SSI 32D535 is directly related to the selection of the loop filter. The loop filter characteristics should be optimized for:

(A) Fast Acquisition

The ability of the loop to quickly obtain lock when the input signal to the Phase Detector is switched between the reference oscillator (crystal) and the Read Data ($\overline{RD}$). Fast acquisition implies a large loop bandwidth so that it can quickly respond to changes at the input.

(B) Data Margin

The ability of the loop to ignore bit shifts (jitter) and maintain a well centered window about the data pulse train. In general, it is not desirable to allow the loop to respond to a single shifted bit as this would cause the subsequent bit to be poorly centered within its window and possibly cause an error. This requirement implies a small loop bandwidth reducing the sensitivity to high frequency jitter.

(C) Data Tracking

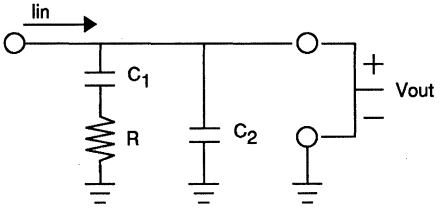
The ability to respond to instantaneous changes in phase and frequency of the data. This can be a result of such phenomena as disk rotational speed variations which cause changes in the characteristics of the incoming data stream. In general, this requirement is consistent with that of fast acquisition, however, this depends upon the application.

Although the loop performance characteristics place conflicting requirements on the loop bandwidth, the architecture of the SSI 32D535 significantly simplifies the design by minimizing the "step in phase" and "step in frequency" encountered when switching the Phase Detector input reference signal. A zero phase restart technique is employed to minimize the initial phase error while the standby reference oscillator keeps the VCO at the center frequency during non-read modes.

One approach in determining the initial loop filter selection is to consider the requirements imposed during acquisition. This includes both acquiring lock to the crystal reference in non-read modes, as well as locking to the preamble field prior to decoding data. The format of the sector will dictate which of these two criteria imposes the tightest restriction on acquisition.

The requirements for acquiring lock to the crystal oscillator are application specific and usually depend upon the length of the Write Splice gap. Therefore, the design approach employed in this analysis will be based upon the requirements during acquisition to the preamble field. The length (in time) of the preamble field is set by the SSI 32D535 locking sequence. Knowing this length in time, and that our initial phase error is less than 0.5 radians, we can determine an acceptable loop bandwidth (ω_n) and damping factor (ζ).

One possible loop filter configuration is as follows:



The role of C1 is as an integrating element. The larger this capacitance, the longer the acquisition time; the smaller the capacitance, the greater the ability to track high frequency jitter. The resistor R reduces the phase shift induced by C1. The capacitor C2 will suppress high frequency transients and will have minimal effect on the loop response if it is small relative to C1 (typically C2 = C1/10)

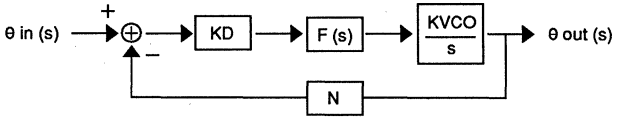
The loop filter transfer function is:

$$F(s) = \frac{Vout}{Iin} = \frac{1 + sRC_1}{sC_1\left(1 + sC_2R + C_2/C_1\right)}$$

If C2 << C1, then:

$$F(s) = \frac{Vout}{Iin} = \frac{1 + sRC_1}{sC_1}$$

The overall block diagram for the phaselock loop can be described as:



Where,

KD = Phase Detector gain [A/rad]

F(s) = Loop filter impedance [V/A]

$\frac{KVCO}{s}$ = VCO control gain [rad/sec-V]

N = The ratio of the reference input frequency to the VCO output frequency

The closed loop transfer function is;

$$T(s) = \frac{\theta out(s)}{\theta in(s)} = \frac{G(s)}{1 + G(s)H(s)}$$

$$= \frac{KD \cdot KVCO\left[(1 + sRC_1)/C_1\right]}{s^2 + s\left[N \cdot KD \cdot KVCO \cdot R\right] + \frac{N \cdot KD \cdot KVCO}{C_1}}$$

by putting the characteristic equation (denominator) in the form of;

$$s^2 + 2s\zeta\omega n + \omega n^2$$

we can solve for ωn and ζ to get;

$$\omega n^2 = \frac{N \cdot KD \cdot KVCO}{C1} \qquad \zeta = \frac{N \cdot KD \cdot KVCO \cdot R}{2\omega n}$$

Now we can solve for R, C1 and C2:

$$C1 = \frac{N \cdot KD \cdot KVCO}{\omega n^2}$$

$$R = \frac{2\zeta\omega n}{N \cdot KD \cdot KVCO}$$

$$C_2 = \frac{C_1}{10}$$

where: ωn = loop bandwidth

ζ = loop damping factor

Because of the nature of Run Length Limited (RLL) codes, the Phase Detector will only be enabled during a data pulse. This technique allows the VCO to run at a center frequency with period, TVCO, equal to one encoded data bit cell time.

Figure 13 represents the relationship between the VCO output when locked to various Phase Detector input signals.

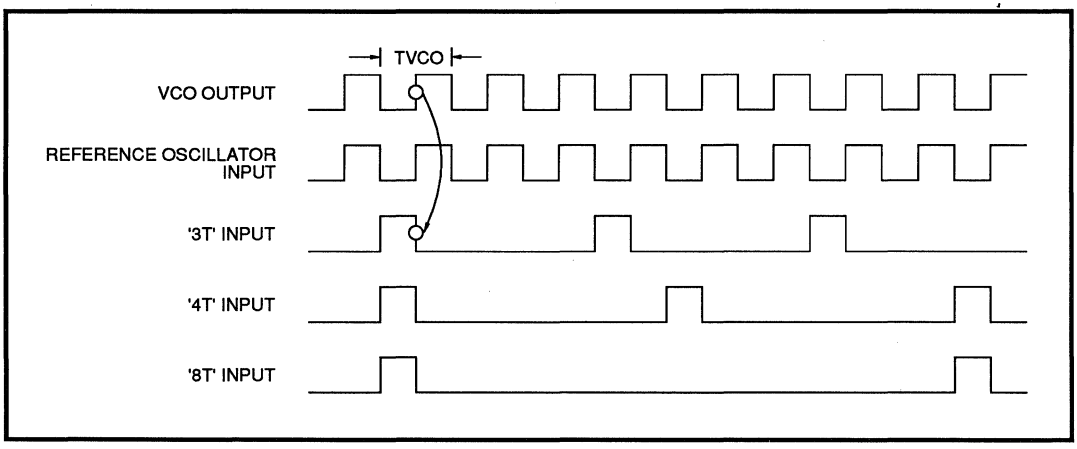


FIGURE 13: Relationship of VCO Output to Phase Detector Input

The average amplitude of the Phase Detector gain depends upon the Phase Detector input signal. When the PLL is locked to the reference oscillator, the Phase Detector is continuously enabled and the gain is at its maximum. When the PLL is tracking data and the input is an "8T" pattern, then the Phase Detector gain is at its minimum. The following indicates the value of "N" for various input conditions:

N = 1.0 , for θin = reference oscillator

N = 0.33 , for θin = 3T (100) preamble field (maximum data frequency)

N = 0.25 , for θin = 4T (1000) preamble field

N = 0.125 , for θin = 8T (minimum data frequency)

Throughout this analysis the PLL has been considered as a continuous time system. In actuality the characteristics of the Phase Detector result in a sampled data system. By utilizing an integrating loop filter to average and smooth the Phase Detector change pump output pulses, this analogy should be reasonable.

LOOP FILTER - Example for a 10 Mbits/s Soft Sector Application

In the soft Sector mode the PLL locking sequence allows the VCO to be within a determined amount of error after 38 x '3T' (100) bit groups. At 10 Mbits/s each data bit cell time, TVCO, is equal to 50 ns. This results in:

$t_{max} = (38)(3)(50ns) = 5.7\ \mu s$

LOOP FILTER (Continued)

Therefore, the PLL has 5.7 μs to settle to within an acceptable amount of error before tracking and decoding data. Because the SSI 32D535 employs a zero phase restart technique, the initial phase error is less than 8% TORC (0.5rad) or:

$\Delta\theta e < (0.08)(100ns)$

$\Delta\theta e < 8ns$

Determining an acceptable amount of phase error after locking to the preamble field depends upon the system requirements. In addition, it may be necessary to consider the effects of frequency steps in applications where motor speed control tolerances are significant. Generally, an acceptable amount of error is defined to be that amount which when added to all other timing error contributors, results in the data being within its timing window by the required margin.

In general, it is desirable to have the loop damping factor "ζ" between 0.5 and 1.0 during acquisition. For a high gain, second-order loop this results in minimal noise bandwidth. For this example we will let $\zeta = 0.7$.

Figure 14 represents the phase errors response in time to a transient step in phase as a function of the loop bandwidth and damping factor. Figure 15 indicates the response of the VCO control voltage to compensate for this step in phase.

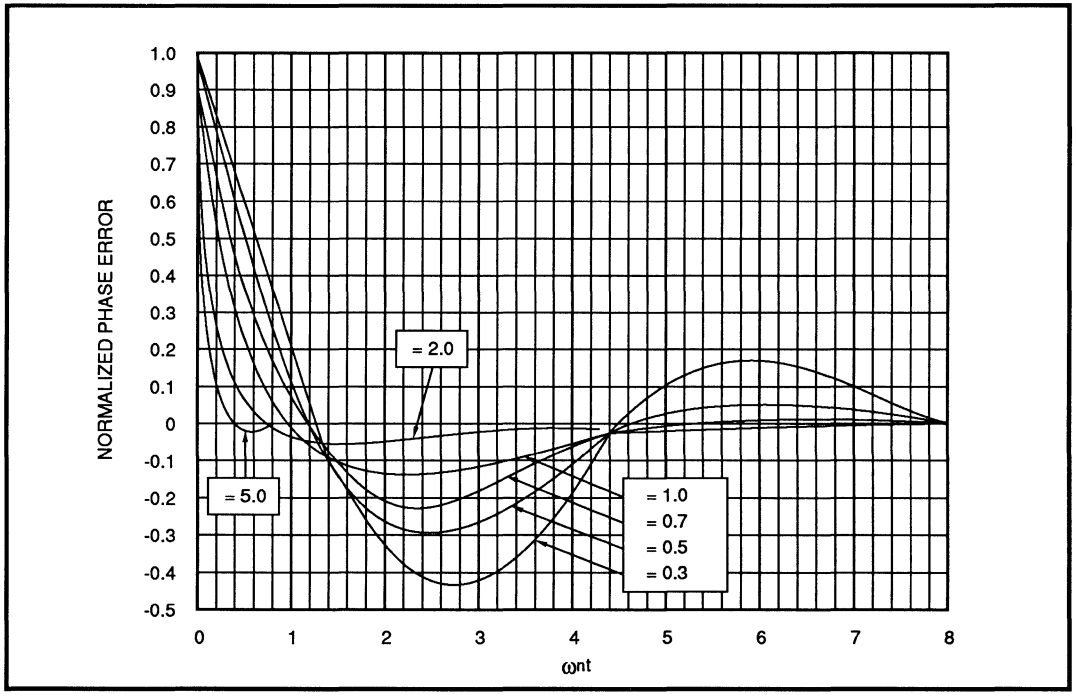


FIGURE 14: TRANSIENT PHASE ERROR θe(t) DUE TO A STEP IN PHASE Δθ

0188

LOOP FILTER (Continued)

As shown in Figure 14, with $\zeta = 0.7$, our initial transient phase error will be at most 22% of its original value at $\omega nt = 2.3$, 7.5% at $\omega nt = 4.0$, etc. For this example we want the final phase error to be less than 1% of its original level. This results in a ωnt between 5 and 6. To simplify the results, let $\omega nt = 5.7$.

Now,

$\omega nt = 5.7$

and $t_{max} = 5.7\mu S$

$\therefore \omega n = 1.0 \cdot 10^6$ rad/sec

with $\zeta = 0.7$

Since we are evaluating the loop response during acquisition to the '3T' preamble, N = 0.33.

Now we have all the information required to calculate the loop filter component values.

$RR = 3567\Omega$

$\omega n = 1.0 \cdot 10^6$ rad/sec

$\zeta = 0.7$

$KD(typ) = 0.309/(RR+500) = 7.6 \cdot 10^{-5}$ A/rad

$KVCO(typ) = 0.17\omega o = 0.17(2\pi)/T0 = 2.14 \cdot 10^7$ rad/sec-volt

$N = 0.33$

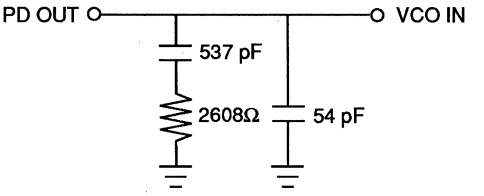
which results in:

$$R = \frac{2\zeta\omega n}{N \cdot KD \cdot KVCO} = 2608\Omega$$

$$C_1 = \frac{N \cdot KD \cdot KVCO}{\omega n^2} = 537pF$$

$$C_2 = \frac{C_1}{10} = 54pF$$

or,



LOOP FILTER (Continued)

This loop filter configuration and its component values should be considered a starting point. The final value of ωn depends upon the system requirements and can certainly be optimized for a specific application. In the table below, we have listed some suggested external component values for several common data rates.

DATA RATE (Mbit/s)	DAMPING FACTOR	LOCK TIME tmax (µs)	ωnt	BANDWIDTH $\omega n \left(\frac{rad}{sec}\right)$	EXTERNAL COMPONENT VALUES					
					RR(KΩ)	Cd(pF)	Rd(KΩ)	R(KΩ)	C1(pF)	C2(pF)
7.5	0.7	7.5	5.0	6.67×10^5	4.92	100	11.0	3.0	687	69
10.0	0.7	5.7	5.7	1.0×10^6	3.57	82	10.0	2.7	510	51
15.0	0.7	3.8	5.7	1.5×10^6	2.21	100	6.22	1.8	510	51

LAYOUT CONSIDERATIONS

As with other high frequency analog devices the SSI 32D535 requires care in layout. The designer should keep analog signal lines as short as possible and well balanced. Use of a ground plane is recommended, along with supply bypassing to separate the SSI 32D535, and associated circuitry, from other circuits on the PCB.

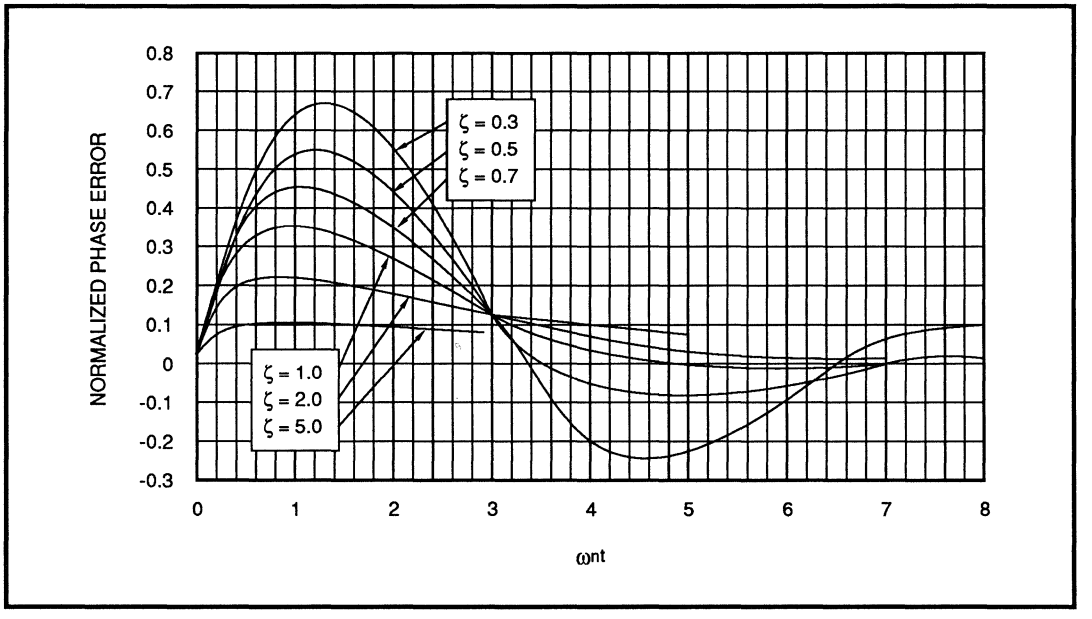
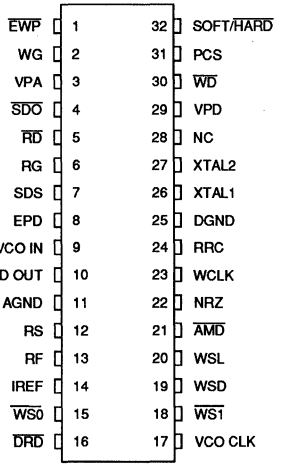


FIGURE 15: TRANSIENT PHASE ERROR θe(t) DUE TO A STEP IN FREQUENCY Δω

SSI 32D535
Data Synchronizer/ 2, 7 RLL ENDEC with Write Precompensation

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



32 LEAD SOW, DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32D535 32 Pin Small Outline - Wide	SSI 32D535 - CW	32D535 - CW
SSI 32D535 32 Pin Plastic DIP	SSI 32D535 - CP	32D535 - CP

silicon systems™
Silicon Systems, Inc., 14351 Myford Road, Tustin CA 92680, (714) 731-7110, TWX 910-595-2809

SSI 32D536
Data Synchronization/ 1, 7 RLL ENDEC with Write Precompensation

August, 1988

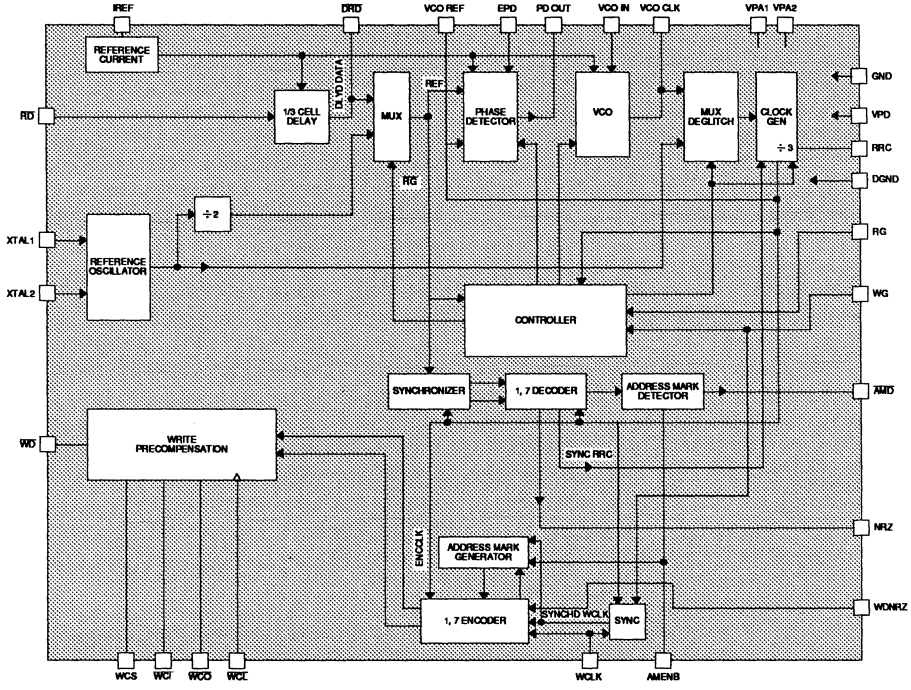
DESCRIPTION

The SSI 32D536 Data Synchronizer/1,7 RLL ENDEC provides data recovery and data encoding for storage systems which employ a 1,7 RLL encoding format. Data synchronization is performed with a fully integrated high performance PLL. A zero phase restart technique is used to minimize PLL acquisition time. The SSI 32D536 has been optimized for operation as a companion device to the SSI 32C452 and AIC 010 controllers. The VCO frequency setting elements are incorporated within the SSI 32D536 for enhanced performance and reduced board space. Data rate is established with a single external programming resistor. The SSI 32D536 utilizes an advanced bipolar process technology which affords precise decode window control without the requirement of an accurate 1/3 cell delay or external devices. The SSI 32D536 requires a single +5V supply.

FEATURES

- Data Synchronizer and 1,7 RLL ENDEC
- 7.5 to 15 Mbits/sec operation
  -Data Rate programmed with a single external resistor
- Optimized for operation with the SSI 32C452 and AIC 010 controllers.
- Fast acquisition phase lock loop
  - Zero phase restart technique
- Fully integrated data separator
  - No external delay lines or active devices required
- Programmable write precompensation
- Hard and soft sector operation
- Crystal controlled reference oscillator
- +5V operation
- 28-pin PLCC & 28-pin DIP packages

BLOCK DIAGRAM



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OPERATION

The SSI 32D536 is designed to perform data recovery and data encoding in rotating memory systems which utilize a 1,7 RLL encoding format. In the Read Mode the SSI32D536 performs Data Synchronization, Sync Field Search and Detect, Address Mark Detect, and Data Decoding. In the Write Mode, the SSI 32D536 converts NRZ data into the 1,7 RLL format described in Table 1, performs Write Precompensation, generates the Preamble Field, and inserts Address Marks as requested. The interface electronics and architecture of the SSI 32D536 have been optimized for use as a companion device to the SSI 32C452 or AIC 010 controllers.

The SSI 32D536 can operate with data rates ranging from 7.5 to 15 Mbits/sec. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 cell delay. The value of this resistor is given by:

$$RR = \frac{92.6}{DR} - 2.3\ (K\Omega)$$

where: DR = Data Rate in Mbits/sec.

An internal crystal reference oscillator, operating at three times the data rate, generates the standby reference for the PLL. A series resonant crystal between XTAL1 and XTAL2 should be selected at three times the Data Rate. If a crystal oscillator is not desired, then an external TTL compatible reference may be applied to XTAL1, leaving XTAL2 open.

The SSI 32D536 employs a Dual Mode Phase Detector; Harmonic in the Read Mode and Non Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DYLD DATA pulse. In the Write and Idle modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The READ GATE (RG), and WRITE GATE (WG) inputs control the device mode.

RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

READ OPERATION

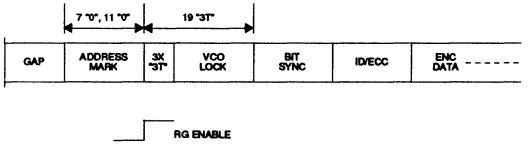
The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the $\overline{RD}$ input and a low level selects the crystal reference oscillator.

In the Read Mode the falling edge of $\overline{DRD}$ enables the Phase Detector while the rising edge is phase compared to the rising edge of the VCO/2. As depicted in Figure 1, $\overline{DRD}$ is a 1/3 cell wide (TVCO) pulse whose leading edge is defined by the leading edge of $\overline{RD}$. An accurate and symmetrical decode window is developed from the VCO/2 clock. By utilizing a fully integrated symmetrical VCO running at three times the data rate, the decode window is insured to be accurate and centered symmetrically about the rising edges of $\overline{DRD}$. The accuracy of the 1/3 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of the decode window.

In Non-Read Modes, the PLL is locked to the crystal reference oscillator. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset. By minimizing the phase alignment in this manner (phase error $\leq$ 1 rads), the acquisition time is substantially reduced.

SOFT SECTOR OPERATION

Disk Operation Lock Sequence in Read Mode Soft Sector Operation



ADDRESS MARK DETECT

In Soft Sector Read Operation the SSI 32D536 must first detect an address mark to be able to initiate the rest of the read lock sequence. An address mark for the SSI 32D536 consists of two (2) 7 "0" patterns followed by two 11 "0" patterns. To begin the read lock sequence the Address Mark Enable (AMENB) is asserted by the controller. The SSI 32D536 Address Mark Detect ($\overline{AMD}$) circuitry then initiates a search of the read data ($\overline{RD}$) for an address mark. First the $\overline{AMD}$ looks for a set of 6 "0's" within the 7 "0" patterns. Having detected a 6 "0" the $\overline{AMD}$ then looks for a 9 "0" set within the 11 "0's". If $\overline{AMD}$ does not detect 9 "0's" within 5 $\overline{RD}$ bits after detecting 6 "0's" it will restart the Address Mark Detect sequence and look for 6 "0's." When the $\overline{AMD}$ has acquired a 6 "0," 9 "0" sequence the $\overline{AMD}$ transitions low disabling AMENB after one "zero" time period delay; one encoded clock time period later the $\overline{AMD}$ transitions back high and the SSI 32D536 is ready for a preamble search when the Read Gate is asserted.

PREAMBLE SEARCH

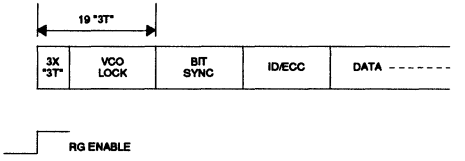
After the Address Mark (AM) has been detected a Read Gate (RG) can be asserted initiating the remainder of the read lock sequence. When RG is asserted an internal counter counts negative transitions of the incoming Read Data ($\overline{RD}$) looking for (3) consecutive 3T preamble. Once the counter reaches count 3 (finds (3) consecutive 3T preamble) the internal read gate enables switching the phase detector from the reference oscillator to the delayed Read Data input ($\overline{DRD}$); at the same time a zero phase (internal) restart signal restarts the VCO in phase with the read reference clock. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

VCO LOCK & BIT SYNC ENABLE

When the internal counter counts 16 more "3T" or a total of 19 negative transitions from RG enable, an internal VCO lock signal enables. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. Also, at count 19, the RRC source switches from the reference oscillator to VCO clock signal which is phase locked to $\overline{DRD}$. The VCO is assumed locked at this point. A maximum of 2 RRC time periods may occur for the RRC transition, however, no short duration glitches will occur. After the bit sync circuitry sets the proper decode window (VCO in sync with RRC and RRC in sync with data) NRZ is enabled and data is toggled in to be decoded for the duration of the read gate.

HARD SECTOR OPERATION

Disk Operation Lock Sequence in Read Mode Hard Sector Operation



In hard sector operation the SSI 32D536's Address Mark Detection circuitry is not enabled by a AMENB signal and $\overline{AMD}$ remains inactive. A hard sector read operation does not require an address mark search but starts with a preamble search as with soft sector and sequences identically. In all respects, with exception to the address mark search sequence, hard sector read operation is the same as soft sector read.

WRITE MODE

In the write mode the SSI 32D536 converts NRZ data from the controller into 1,7 RLL formatted data for storage on the disk. The SSI 32D536 can operate with a soft or hard sector hard drive.

In soft sector operation the device generates a "7, 11" Address Mark, and a preamble pattern.

In the hard sector operation the device generates a 3 x "3T" preamble pattern but no preceding Address Mark. Serial NRZ data is clocked into the SSI 32D536 and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the

WCLK input. The WCLK input is a feature provided for operation in an ESDI application to compensate for large cable delays. In SCSI or ST506 operation, WCLK is connected directly to the RRC output.

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The SSI 32D536 recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back bit shift. The magnitude of the time shift, TC, is determined by an external R C network on the WCS pin given by:

$$TPC = WP(0.053)(Rc)(Cc + Cs)$$

When the write precompensation control latch, $\overline{WCL}$ is low, the SSI 32D536 performs write precompensation according to the algorithm outlined in Table 3.

SOFT SECTOR

In soft sector operation, when Read Gate (RG) transitions low, VCO source and RRC source switch from $\overline{RD}$ and VCO/3, respectively, to the reference crystal. At the same time the VCO (internal) lock goes inactive but the VCO is locked to the reference crystal. After a delay of 1 NRZ time period (min) from RG low, the Write Gate (WG) can be enabled while WDNRZ is maintained (NRZ write data) low. The Address Mark Enable (AMENB) is made active (high) a minimum of 1 NRZ time period later. The Address Mark (consisting of 7 "0's," 7 "0's," 11 "0's, "11 "0's") and the 3 x "3T" Preamble is then written by $\overline{WDO}$. WDNRZ goes active at this point and after a delay of 5 NRZ time periods begins to toggle out $\overline{WDO}$ encoded data. Finally, at the end of the write cycle, 5 NRZ of blank encoded time passes to insure the encoder is flushed of data; WG then goes low.

HARD SECTOR

In hard sector operation, when read gate (RG) transitions low, VCO source and RRC switch references and VCO lock (internal) goes inactive as with soft sector but the AMENB (address mark enable) is low.

The SSI 32D536 then sequences from RG disable to WG enable and WDNRZ active as in soft sector operation.

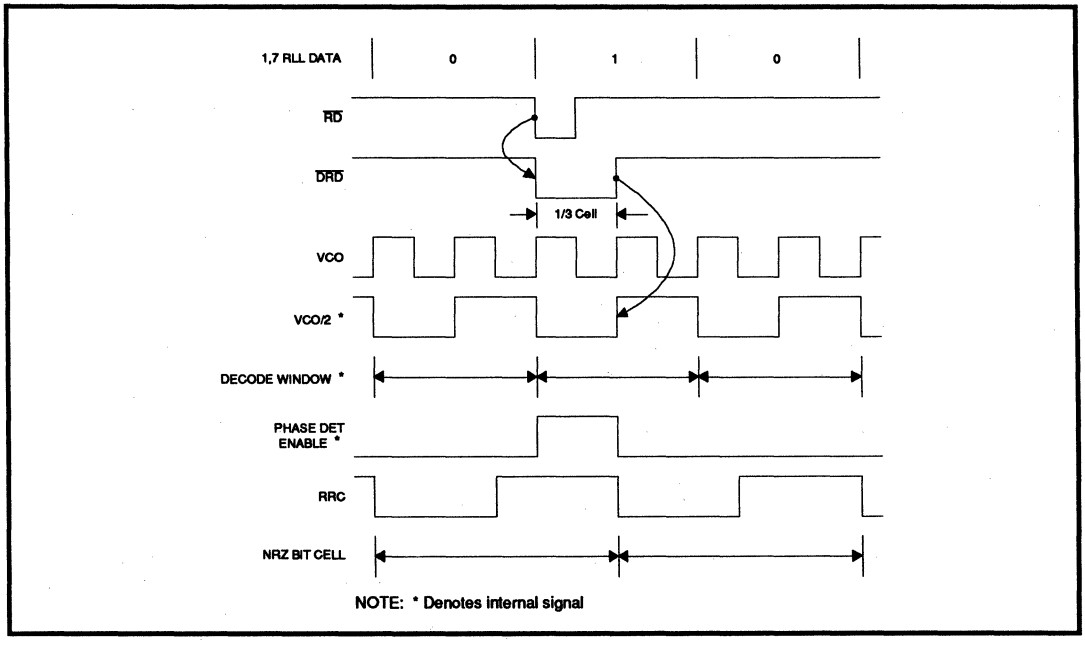


FIGURE 1: Data Synchronization Waveform

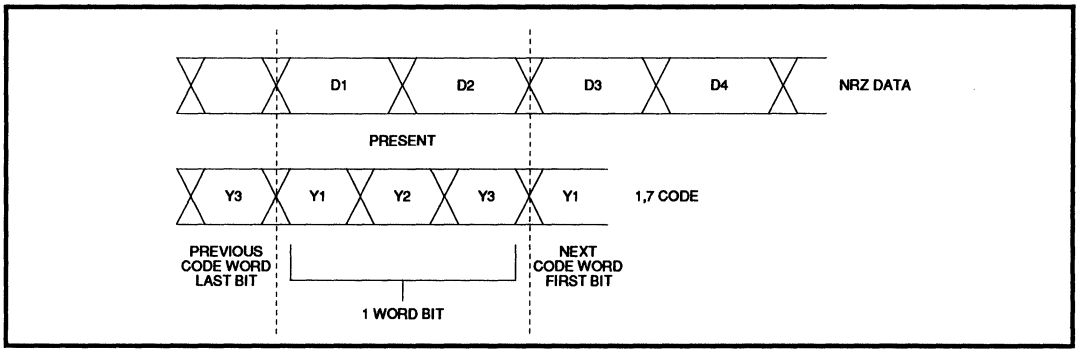


FIGURE 2: NRZ Data Word Comparision to 1, 7 Code Word Bit (See Table 1, for Decode Scheme)

TABLE 1: 1,7 RLL Code Set

PREVIOUS CODE WORD LAST BIT	DATA BITS PRESENT		NEXT		CODE BITS		
0	1	0	0	X	1	0	1
0	1	0	1	X	0	1	0
0	1	1	0	0	0	1	0
0	1	1	*	*	1	0	0
0	0	0	0	X	0	0	1
0	0	0	1	X	0	0	0
0	0	1	0	X	0	0	1
0	0	1	1	X	0	0	0
1	0	0	0	X	0	0	1
1	0	0	1	X	0	1	0
1	0	1	0	0	0	1	0
1	0	1	*	*	0	0	0
Y3	D1	D2	D3	D4	Y1	Y2	Y3

X = Don't care
* = Not all zeros

TABLE 2: Clock Frequency

WG	RG	VCO REF	RRC	DECCLK	ENCCLK	MODE
0	0	XTAL/2	XTAL/3	XTAL/2	XTAL/2	IDLE
0	1	$\overline{RD}$	VCO/3	VCO/2	XTAL/2	READ
1	0	XTAL/2	XTAL/3	XTAL/2	XTAL/2	WRITE
1	1	XTAL/2	XTAL/3	XTAL/2	XTAL/2	IDLE

Note 1: Until the VCO locks to the new source, the VCO/2 entries will be XTAL/2.

2: Until the VCO locks to the new source, the VCO/3 entries will be XTAL/3.

TABLE 3: Write Precompensation Algorithm

BIT	BIT	BIT	BIT	BIT	COMPENSATION
n-2	n-1	n	n+1	n+2	BIT n
1	0	1	0	1	NONE
0	0	1	0	0	NONE
1	0	1	0	0	EARLY
0	0	1	0	1	LATE

LATE: Bit n is time shifted (delayed) from its nominal time position towards the bit n+1 time position.

EARLY: Bit n is time shifted (advanced) from its nominal time position towards the bit n-1 time position.

TABLE 4: Write Precompensation Magnitude

$\overline{WCI}$	$\overline{WCO}$	MAGNITUDE.WP
0	0	3
0	1	2
1	0	1
1	1	0

The nominal magnitude, (TPC = WP x 0.053 (Rc) (Cc+Cs), is externally set with an R-C network on pin WCS.

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{RD}$	I	READ DATA: Encoded Read Data from the disk drive read channel, active low.
RG	I	READ GATE: Selects the PLL reference input (REF), see Table 1. A change in state on RG initiates the PLL synchronization sequence.
WG	I	WRITE GATE: Enables the write mode, see Table 2.
WCLK	I	WRITE CLOCK: Write Clock input. Must be synchronous with the NRZ Write Data input. For small cable delays, WCLK may be connected directly to pin RRC.
EPD	I	ENABLE PHASE DETECTOR: A low level (Coast Mode) disables the phase detector. This opens the PLL and the VCO will run at the frequency commanded by the voltage on pin VCO IN. Pin EPD has an internal resistor pull up.
AMENB	I	ADDRESS MARK ENABLE: Used to enable the address mark detection and address mark generation circuitry, active high.
$\overline{WC0}$, $\overline{WC1}$	I	WRITE PRECOMPENSATION CONTROL BITS: Pins $\overline{WC1}$, and $\overline{WC0}$ control the magnitude of the write precompensation, see Table 4. Internal resistor pull ups are provided.
$\overline{WCL}$	I	WRITE PRECOMPENSATION CONTROL LATCH: Used to latch the write precompensation control bits $\overline{WC1}$ and $\overline{WC0}$ into the internal DAC. An active low level latches the input bits. Pin $\overline{WCL}$ has an internal resistor pull up.
WDNRZ	I	NRZ WRITE DATA INPUT PIN: This pin can be connected to the NRZ pin to form a bidirectional data port.

OUTPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{WD}$	O	WRITE DATA: Encoded write data output, active low. The data is automatically resynchronized (independent of the delay between RRC and WCLK) to one edge of the XTAL 1 input clock.
RRC	O	READ/REFERENCE CLOCK: A multiplexed clock source used by the controller, see Table 2. During a mode change, no glitches are generated and no more than two lost clock pulses will occur. When RG goes high, RRC is synchronized to the NRZ Read Data after 19 read data pulses.
$\overline{AMD}$	O	ADDRESS MARK DETECT: Tristate output pin that is in its high impedance state when WG is high or AMENB is low. A latched low level output indicates that an address mark has been detected. A low level on pin AMENB resets pin $\overline{AMD}$.

OUTPUT PINS (Continued)

NAME	TYPE	DESCRIPTION
VCO REF	O	VCO REFERENCE: An open emitter ECL output test point. The VCO reference input to the phase detector, the negative edges are phase locked to DLYD DATA. The positive edges of this open emitter output signal indicate the edges of the decode window. Two external resistors are required to perform this test, they should be removed during normal operation for reduced power dissipation.
VCO CLK	O	VCO CLOCK: An open emitter ECL output test point. Two external resistors are required to perform this test. They should be removed during normal operation for reduced power dissipation.
$\overline{\text{DRD}}$	O	DELAYED READ DATA: An open emitter ECL output test point. The positive edges of this open emitter output signal indicates the data bit position. The positive edges of the $\overline{\text{DRD}}$ and the VCO REF signals can be used to estimate window centering. The time jitter of DRD's positive edge is an indication of media bit shift. Two external resistors are required to perform this test. They should be removed during normal operation for reduced power dissipation.
NRZ	O	NRZ READ DATA OUTPUT: Tristate output pin that is enabled when read gate is high. This pin can be connected to the WDNRZ pin to form a bidirectional data port.

ANALOG PINS

NAME	TYPE	DESCRIPTION
IREF	I	TIMING PROGRAM PIN: The VCO center frequency and the 1/3 cell delay are a function of the current sourced into pin IREF.
XTAL1, 2	I	CRYSTAL OSCILLATOR CONNECTIONS: The pin frequency is at three times the data rate. If the crystal oscillator is used, an AC coupled parallel LC circuit must be connected from XTAL1 to ground. If the crystal oscillator is not desired, XTAL1 may be driven by a TTL source with XTAL2 open. The source duty cycle should be close to 50% as possible since its duty cycle will affect the RRC clock duty cycle when XTAL is its source. The additional RRC duty cycle error will be one third the source duty cycle error.
PD OUT	O	PHASE DETECTOR OUTPUT: Drives the loop filter input.
VCO IN	I	VCO CONTROL INPUT: Driven by the loop filter output.
WCS	I	WRITE PRECOMPENSATION SET: Pin for RC network to program write precompensation magnitude value.
DGND, AGND	I	Digital and Analog Ground
VPA1, VPA2	I	Analog +5V Supplies
VPD	I	Digital +5V Supply

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING	UNIT
Storage Temperature	-65 to + 150	°C
Junction Operating Temperature, Tj	+150	°C
Supply Voltage, VPA1, VPA2, VPD	-0.5 to 7	V
Voltage Applied to Logic Inputs	-0.5 to VPD + 0.5	V
Maximum Power Dissipation	1.1	W

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING	UNIT
Supply Voltage, VPA1 = VPA2 = VPD = VCC	4.75 < VCC < 5.25	V
Junction Temperature, Tj	0 < Tj < 135	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 4.75V< VCC <5.25V, 10 MHz< 1/TORC <15 MHz, 30 MHz< 1/TVCO <45 MHz, 0 °C< Tj <135 °C.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIH	High Level Input Voltage		2.0			V
VIL	Low Level Input Voltage				0.8	V
IIH	High Level Input Current	VIH = 2.7V			2.0	µA
IIL	Low Level Input Current	VIL = 0.4V			-1.5	mA
VOH	High Level Output Voltage	IOH = 400 µA	2.7			V
VOL	Low Level Output Voltage	IOL = 4 mA			0.5	V
ICC	Power Supply Current	All outputs open, Tj = 135 °C			240	mA
PWR	Power Dissipation	Tj = 135 °C, test point pins open			1.1	W

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VOHT	Test Point Output High Level $\overline{DRD}$, VCO CLK, VCO REF	262Ω to VPD 402Ωto GND VPD=5.0V VOHT - VPD	-1.02			V
VOLT	Test Point Output Low Level $\overline{DRD}$, VCO CLK, VCO REF	262 Ω to VPD 402Ω to GND VPD = 5.0V VOLT - VPD			-1.625	V

DYNAMIC CHARACTERISTICS AND TIMING

READ MODE (See Figure 3)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TRD	Read Data Pulse Width		15		TORC-20	ns
TFRD	Read Data Fall Time	2.0V to 0.8V, C1 ≤ 15 pF			15	ns
TRRC	Read Clock Rise Time	0.8V to 2.0V, C1 ≤ 15 pF			8	ns
TFRC	Read Clock Fall Time	2.0V to 0.8V, C1 ≤ 15 pF			5	ns
TPNRZ	NRZ (out) Set Up/Hold Time		.31 TORC			ns
TPAMD	$\overline{AMD}$ Propogation Delay		10			ns
	1/3 Cell Delay	TD = 5.05E -12 (RR+530)	0.8TD		1.2TD	ns

WRITE MODE (See Figure 4)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TWD	Write Data Pulse Width	C1 ≤ 15 pF	2TOWC/3 -2TPC -5		2TOWC/3 -2TPC +15	ns
TFWD	Write Data Fall Time	2.0V to 0.8V, C1 ≤ 15 pF			8	ns
TRWC	Write Data Clock Rise Time	0.8V to 2.0V			10	ns
TFWC	Write Data Clock Fall Time	2.0V to 0.8V			8	ns
TSNRZ	WDNRZ Set up Time		5			ns
THNRZ	WDNRZ Hold Time		5			ns

WRITE MODE (Continued)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
TPC	Precompensation Time Shift Magnitude Accuracy	TPCO=.053 (Cc+Cs) (Rc) Rc=1K to 2K Cs=stray capacity $\overline{WC0}$ = 1 $\overline{WC1}$ = 1	0	0	ns
		$\overline{WC0}$ = 0 $\overline{WC1}$ = 1	0.8TPCO-0.2	1.2TPCO+0.2	ns
		$\overline{WC0}$ = 1 $\overline{WC1}$ = 0	0.8(2)TPCO	1.2(2)TPCO	ns
		$\overline{WC0}$ = 0 $\overline{WC1}$ = 0	0.8(3)TPCO	1.2(3)TPCO	ns

DATA SYNCHRONIZATION

PARAMETER		CONDITIONS	MIN	MAX	UNIT
TVCO	VCO Center Frequency Period	VCO IN = 2.7V TO = 3.6E-12 (RR+2300) VCC = 5.0V RR = 3.5K to 5.7K	0.8TO	1.2TO	ns
	VCO Frequency Dynamic Range	1V ≤ VCO IN ≤ VCC-0.6V VCC = 5.0	±25	±45	%
KVCO	VCO Control Gain	$\omega o = 2\pi/TO$ 1V ≤ VCO IN ≤ VCC 0.6V	0.14ωo	0.26ωo	rad/ sec V
KD	Phase Detector Gain	KD = 0.19/(RR+530) VCC = 5.0V, PLL REF = $\overline{RD}$ 3T ("100") pattern	0.83KD	1.17KD	A/rad
	KVCO * KD Product Accuracy		-28	-28	%
	VCO Phase Restart Error	Referred to RRC	-1	1	rad
	Decode Window Centering Accuracy			±2	ns
	Decode Window		(2TORC/3) - 2		ns

CONTROL CHARACTERISTICS (See Figure 5)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TSWS	$\overline{WC0}$ $\overline{WC1}$ SET UP TIME		50			ns
THWS	$\overline{WC0}$, $\overline{WC1}$ HOLD TIME		0			ns

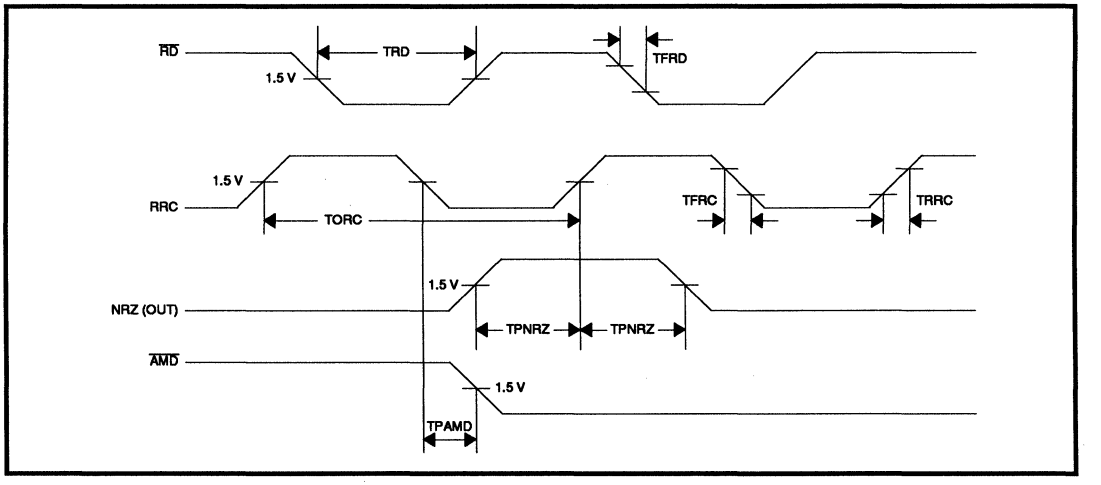


FIGURE 3: Read Timing

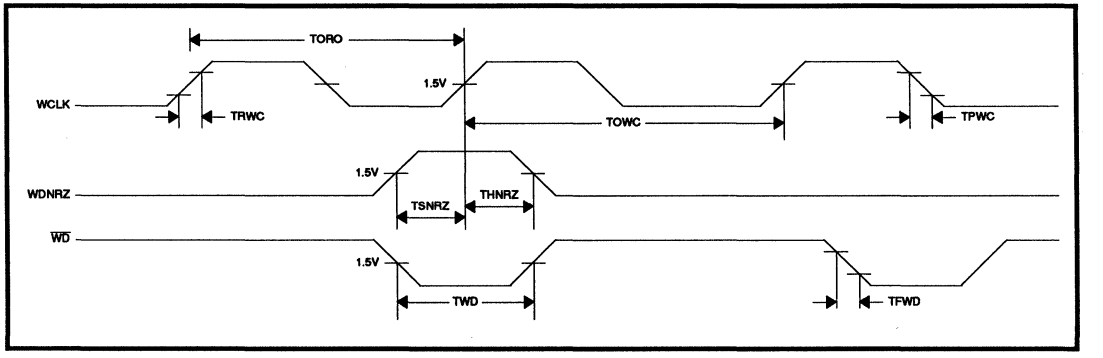


FIGURE 4: Write Timing

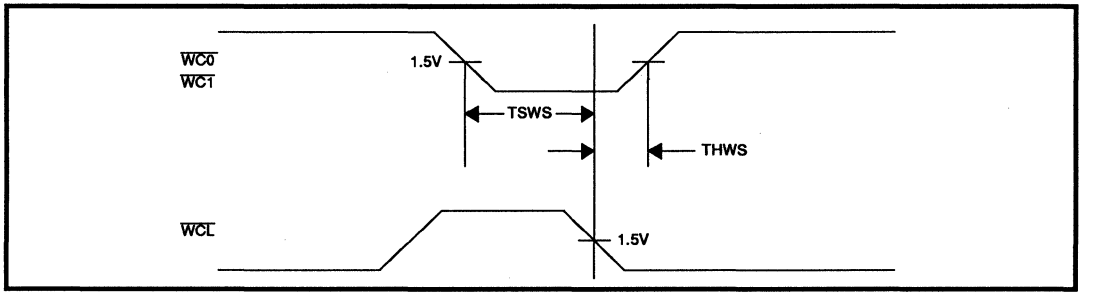


FIGURE 5: Control Timing

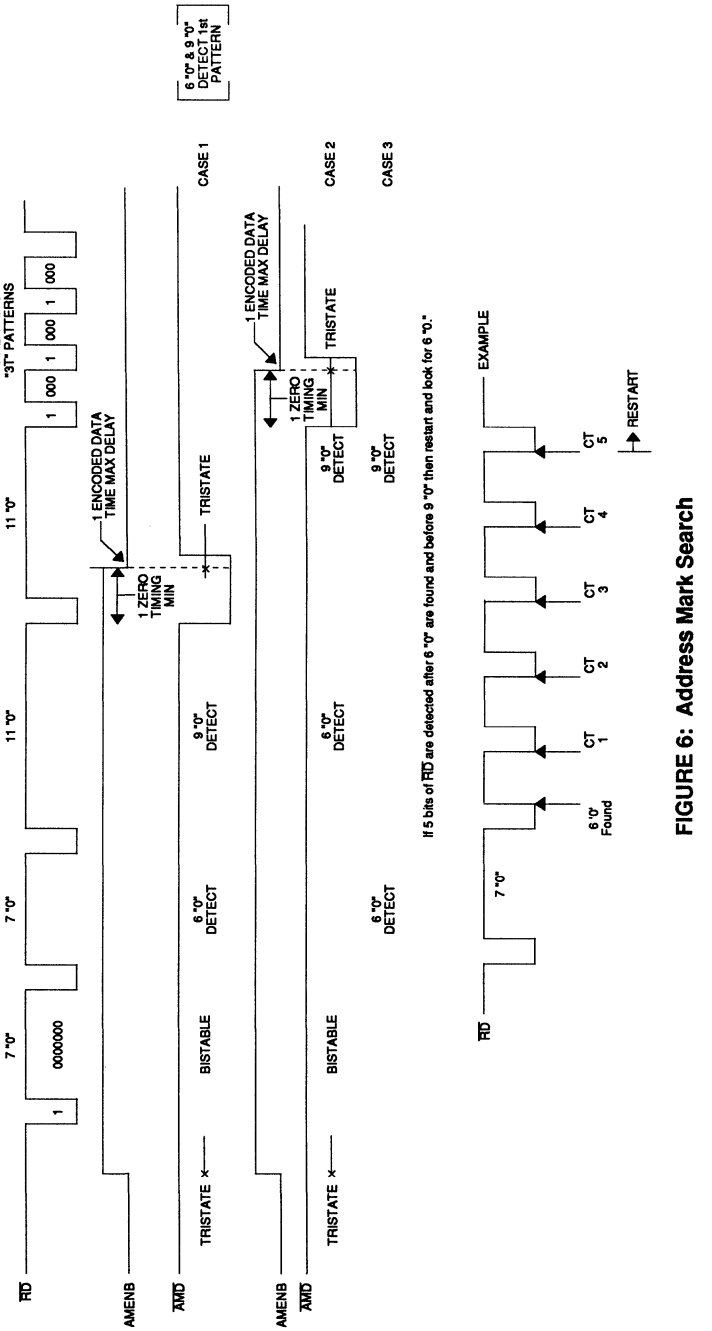


FIGURE 6: Address Mark Search

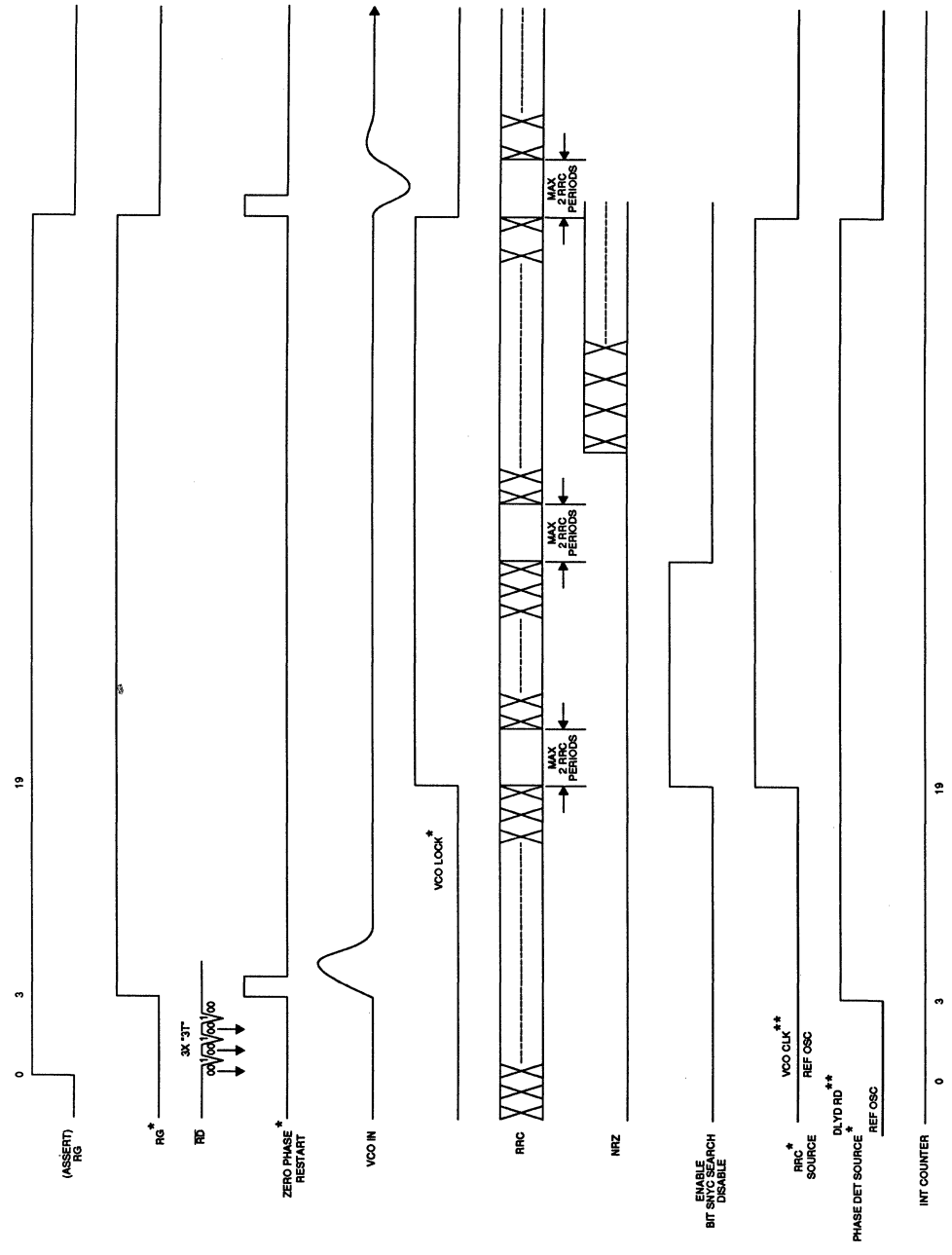


FIGURE 7: Read Mode Locking Sequence (Soft and Hard Sector)

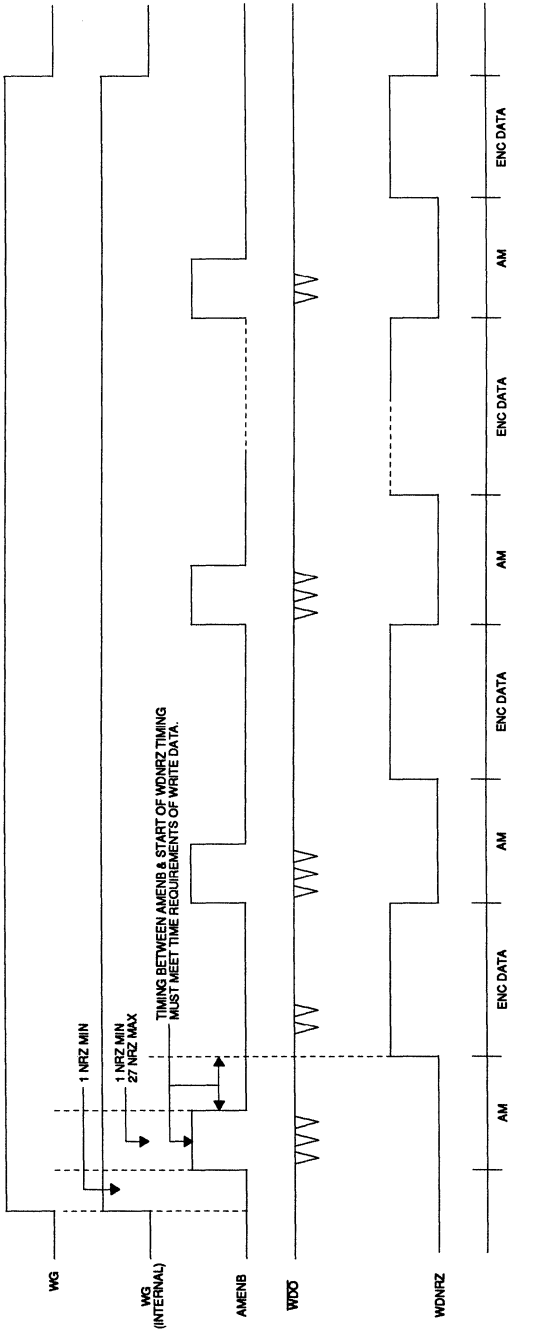


FIGURE 8: Multiple Address Mark Write

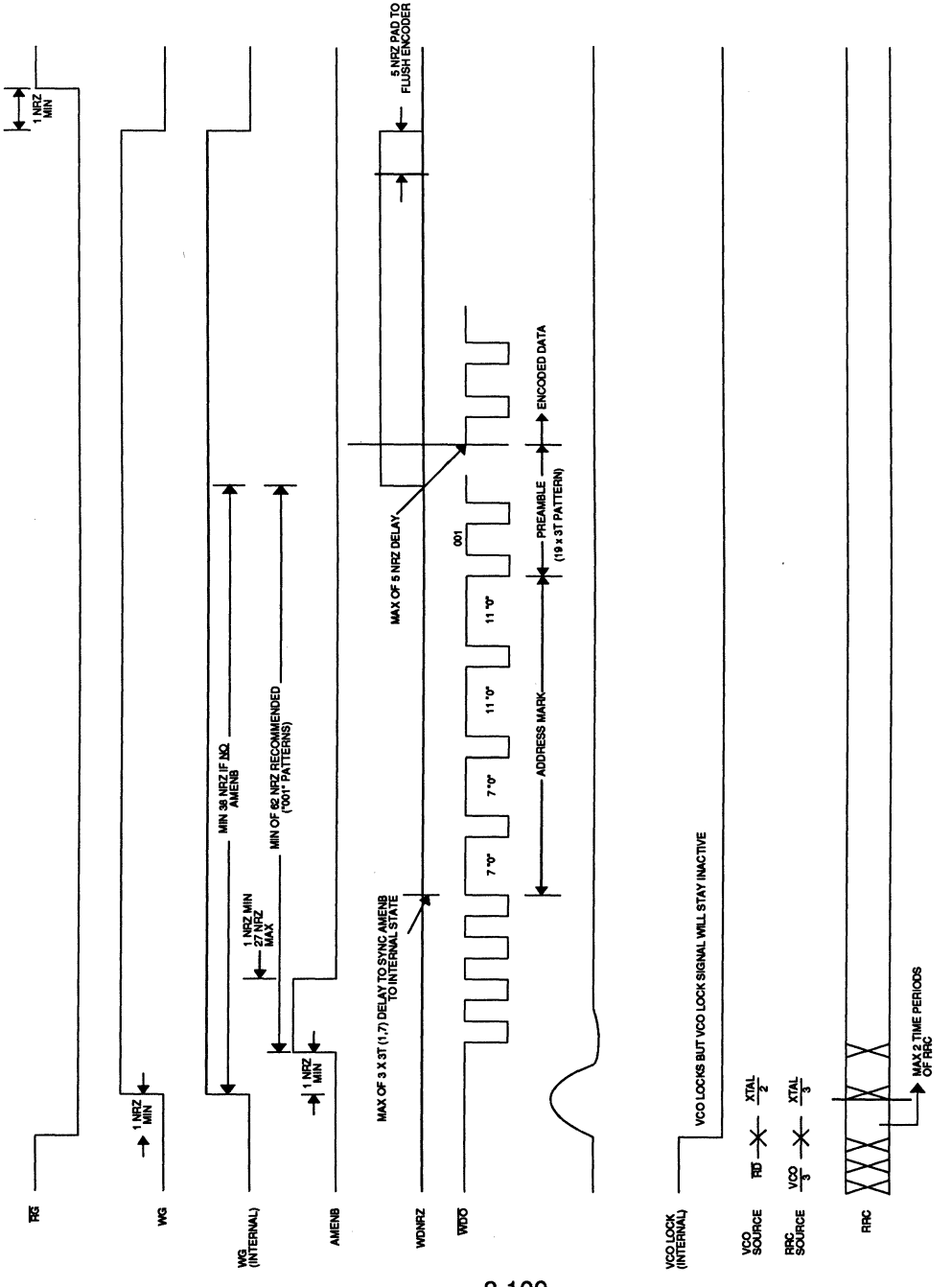


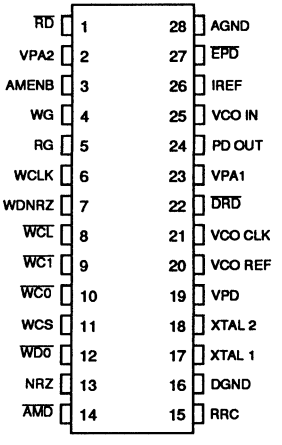
FIGURE 9: Write Data

0888

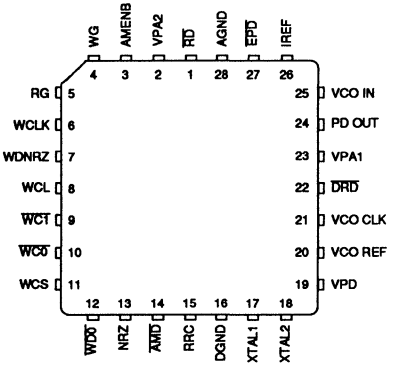
SSI 32D536
Data Synchronization/1, 7 RLL ENDEC with Write Precompensation

PACKAGE PIN DESIGNATIONS
(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.



28-Pin DIP



28-Pin PLCC

3

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32D536		
28-Pin DIP	SSI 32D536-CP	SSI 32D536-CP
28-Pin PLCC	SSI 32D536-CH	SSI 32D536-CH

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NOTES:

Section 4

HDD HEAD POSITIONING

SSI 32H101A
Differential Amplifier

August, 1988

DESCRIPTION

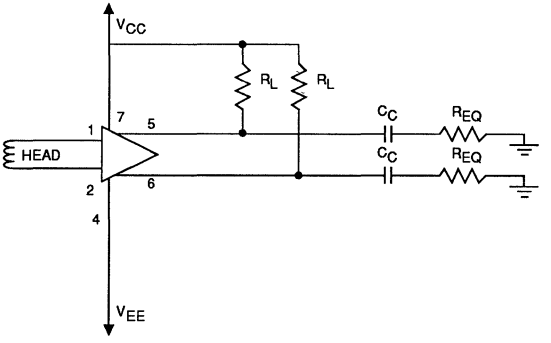
The SSI 32H101A is a two stage differential amplifier applicable for use as a preamplifier for the magnetic servo head circuit of Winchester technology disk drives.

FEATURES

- **Very narrow gain range**
- **30 MHz bandwidth**
- **Electrically characterized at two power supply voltages: IBM Model 3340 compatible (8.3V) and standard OEM industry compatible (10V)**
- **Mechanically compatible with Model 3348 type head arm assembly**
- **SSI 32H1012A available to operate with a 12V power supply**
- **Packages include 8-pin DIP or SON**

4

CONNECTION DIAGRAM



RECOMMENDED LOAD CONDITIONS

1. Input must be AC coupled
2. Cc's are AC coupling capacitors
3. RL's are DC bias and termination resistors (recommended 130Ω)
4. REQ represents equivalent load resistance
5. For gain calculations $R_P = \frac{R_L \cdot R_{EQ}}{R_L + R_{EQ}}$
6. Differential gain = 0.72 Rp (± 18%) (Rp in Ω)
7. Ceramic capacitors (0.1 μF) are recommended for good power supply noise filtering

CAUTION: Use handling procedures necessary for a static sensitive component.

ELECTRICAL CHARACTERISTICS

TA = 25 °C, (V_{CC}-V_{EE}) = 8.3 to 10V ±10% (12V ±10% for 101A-2)

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
Power Supply Voltage (V_{CC} - V_{EE})	12	V
SSI 32H1012A	14	V
Differential Input Voltage	±1	V
Storage Temperature Range	-65 to 150	°C
Operating Temperature Range	0 to 70	°C

DC ELECTRICAL CHARACTERISTICS

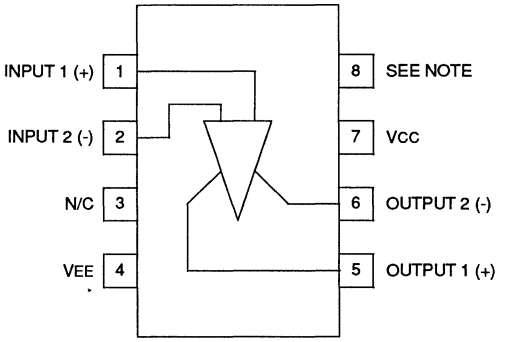
PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Gain (differential)	Rp = 130Ω	77	93	110	
Bandwidth (3dB)	Vi = 2 mVpp	10	20		MHz
Input Resistance		750		1200	Ω
Input Capacitance			3		pF
Input Dynamic Range (Differential)	R_L = 130Ω	3			mVpp
Power Supply Current	(V_{CC} - V_{EE}) = 9.15V		26	35	mA
	(V_{CC} - V_{EE}) = 11V		30	40	mA
	(V_{CC} - V_{EE}) = 13.2V (32H101A-2)		35	45	mA
Output Offset (Differential)	Rs = 0, R_L = 130Ω			600	mV
Equivalent Input Noise	Rs = 0, R_L = 130Ω, BW = 4 MHz		8	14	µV
PSRR, Input Referred	Rs = 0, f ≤ 5 MHz	50	65		dB
Gain Sensitivity (Supply)	Δ (V_{CC} - V_{EE}) = ±10%, RL = 130Ω		±1.3		%
Gain Sensitivity (Temp.)	TA = 25 °C to 70 °C, R_L = 130Ω		-0.2		%/°C
CMRR, Input Referred	f ≤ 5 MHz	55	70		dB

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Supply Voltage (V_{CC} - V_{EE})		7.45	8.3	9.15	V
		9.0	10.0	11.0	V
	32H1012A only	10.8	12.0	13.2	V
Input Signal Vi			2		mVpp
Ambient Temp. T_A		0		70	C

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



8-Pin PDIP, SON

Note : Pin must be left open and not connected to any circuit etch.

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32H101A Differential Amplifier		
8-Pin PDIP	SSI 32H101A-8P	32H101A-CP
8-Pin SON	SSI 32H101A-8N	32H101A-8N
SSI 32H1012A Differential Amplifier		
8-Pin PDIP	SSI 32H1012A-8P	32H1012A-8P
8-Pin SON	SSI 32H1012A-8N	32H1012A-8N

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NOTES:

SSI 32H116
Differential Amplifier

August, 1988

DESCRIPTION

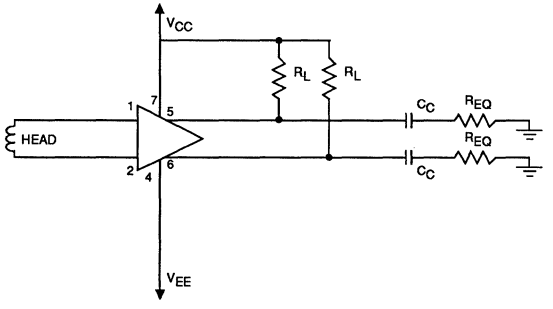
The SSI 32H116 is a high performance differential amplifier applicable for use as a preamplifier for the magnetic servo thin film head in Winchester disk drives.

FEATURES

- **Narrow gain range**
- **50 MHz bandwidth**
- **IBM 3370/3380-compatible performance**
- **Operates on either IBM-compatible voltages (8.3V) or OEM-compatible (10V)**
- **Packages include 8-pin CERDIP, Plastic DIP or SON and custom 10-pin flatpack**
- **SSI 32H1162 available to operate with a 12V power supply**

4

CONNECTION DIAGRAM



RECOMMENDED LOAD CONDITIONS

1. Input must be AC coupled
2. Cc's are AC coupling capacitors
3. RL's are DC bias and termination resistors, 100Ω recommended
4. REQ. represents equivalent load resistance
5. Ceramic capacitors (0.1 μF) are recommended for good power supply noise filtering

CAUTION: Use handling procedures necessary for a static sensitive component.

ELECTRICAL CHARACTERISTICS

Tj = 15 °C to 125 °C, (Vcc-VEE) = 7.9V to 10.5V (to 13.2V for 32H1162)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power Supply Voltage (VCC-VEE)	12	V
SSI 32H1162	14	V
Operating Power Supply Range	7.9 to 10.5	V
SSI 32H1162	7.9 to 13.2	V
Differential Input Voltage	±1	V
Storage Temperature Range	-65 to 150	°C
Operating Ambient Temperature (TA)	15 to 60	°C
Operating Junction Temperature (TJ)	15 to 125	°C
Output Voltage	VCC -2.0 to VCC +0.4	V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Gain (Differential)	Vin = 1mVpp, T_A = 25 °C, F = 1 MHz	200	250	310	mV/mV
Bandwidth (3dB)	Vin = 1mVpp, C_L = 15 pF	20	50		MHz
Gain Sensitivity (Supply)				1.0	%/V
Gain Sensitivity (Temp.)	15 °C < T_A < 55 °C		-0.16		%/C
Input Noise Voltage	Input Referred, Rs = 0		0.7	0.94	$nV/\sqrt{Hz}$
Input Capacitance (Differential)	Vin = 0,f = 5 MHz		40	60	pF
Input Resistance (Differential)			200		Ω
Common Mode Rejection Ratio Input Referred	Vin = 100 mVpp, f = 1 MHz	60	70		dB
Input Signal Level	Common Mode			300	mVpp
Power Supply Rejection Ratio Input Referred	Vee + 100 mVpp, f - 1 MHz	46	52		dB
Input Dynamic Range (Differential)	DC input voltage where AC gain is 90% of gain with 0.2 mVpp input signal			±0.75	mV
Output Offset Voltage (Differential)	Vin = 0	-600		600	mV
Output Voltage (Common Mode)	Inputs shorted together and Outputs shorted together	Vcc-0.45	Vcc-0.6	Vcc-1.0	V
Single Ended Output Resistance		10			Ω

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Single Ended Output Capacitance				10	pF
Power Supply Current	V_{CC}-V_{EE} = 9.15V		28	40	mA
	V_{CC}-V_{EE} = 11V		29	42	
	V_{CC}-V_{EE} = 13.2V, 32H1162 only		39	50	
Input DC Voltage	Common Mode		V_{EE} +2.6		V
Input Resistance	Common Mode		80		Ω

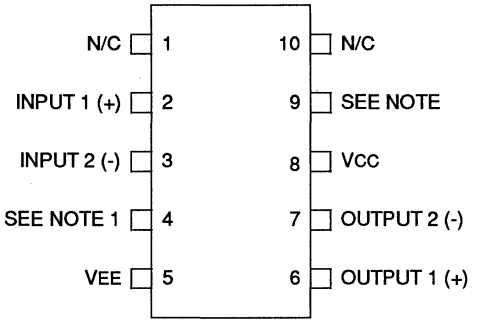
RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage (V_{CC}-V_{EE})		7.45	8.3	9.15	V
		9.0	10.0	11.0	V
	SSI 32H1162 only	10.8	12.0	13.2	V
Input Signal Vin			1		mVpp
Ambient Temp T_A		15		65	°C

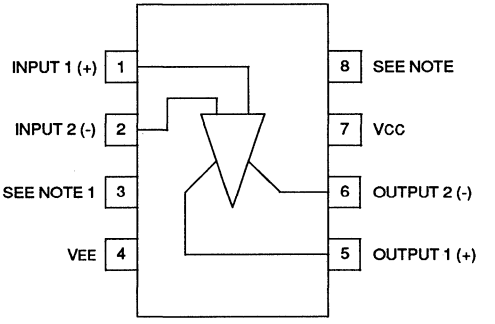
4

SSI 32H116
Differential Amplifier

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



10-Pin Flatpack



8-Pin PDIP, SON

NOTE : Pin must be left open and not connected to any circuit etch.

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32H116 Differential Amplifier		
10-Pin Flatpack	SSI 32H116-CF	32H116-CF
8-Pin SON	SSI 32H116-CN	32H116-CN
8-Pin PDIP	SSI 32H116-CP	32H116-CP
SSI 32H1162		
10-Pin Flatpack	SSI 32H1162-CF	32H1162-CF
8-Pin SON	SSI 32H1162-CN	32H1162-CN
8-Pin PDIP	SSI 32H1162-CP	32H1162-CP

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SSI 32H523R
Thin Film Single Channel Servo Read/Write Device

August, 1988

DESCRIPTION

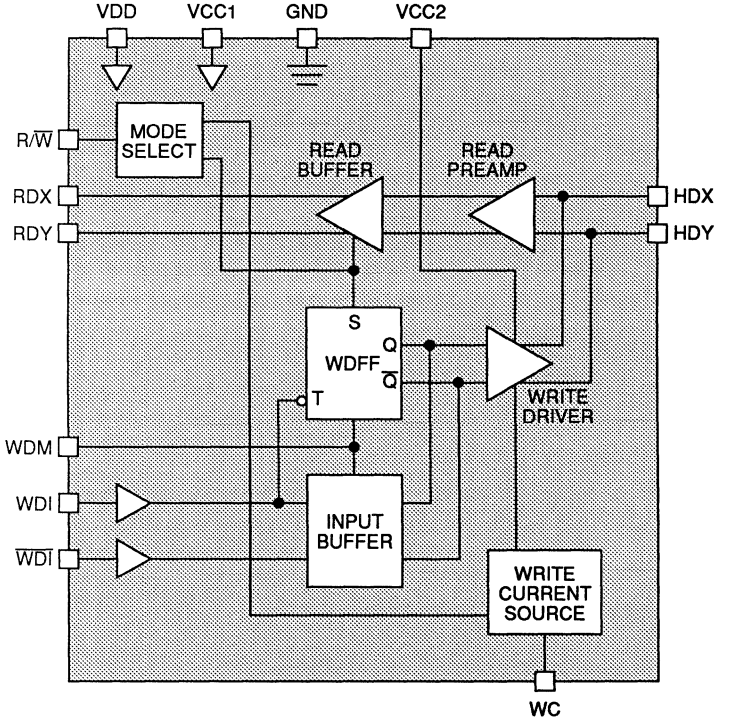
The SSI 32H523R Read/Write device is a bipolar monolithic integrated circuit designed for use with a two terminal thin film recording head. It provides a low noise read amplifier and write current control. In its servo application, the device will be used in write mode once then switched permanently to read mode. Data protection is provided in both write and read modes to guarantee servo data security. Power supply fault protection is effective in both write and read modes while head short circuit protection is provided in write mode. Further data security can be provided in read mode by removing the write current source voltage. It requires +5V and +12V power supplies and is available in a 14-pin SON surface mount package. Internal 1000Ω damping resistors are provided.

FEATURES

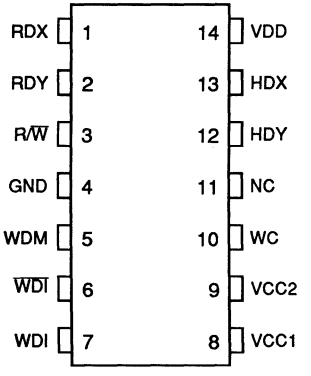
- **High performance:**
  - **Read mode gain = 250 V/V**
  - **Input noise = 1.0 nV/√Hz max.**
  - **Input capacitance = 45 pF max.**
  - **Write current range = 10 mA to 40 mA**
  - **Head voltage swing = 3.4 Vpp min.**
  - **Write current rise time = 13 nsec**
- **Highest level of data security provided**
- **Power supply fault protection**
- **Head to ground short circuit protection**
- **+5V, +12V power supplies**

4

BLOCK DIAGRAM



PIN DIAGRAM



14-PIN SON

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32H523R provides write drive or read amplification. Mode control is accomplished with pins WDM, Write Data Mode, and R/$\overline{W}$, as shown in Table 1. An internal resistor pullup on R/$\overline{W}$ will force the device into a non-writing condition if the line is opened accidentally.

WRITE MODE

The write mode configures the SSI 32H523R as a differential current switch. The WDM pin state determines whether write current transitions are controlled by a single-ended TTL input, WDI, or by differential (ECL-like) inputs, WDI and $\overline{WDI}$. With WDM open, write current is toggled between the X and Y direction of the head on each high to low transition on pin WDI, Write Data Input. A preceding read operation initializes the Write Data Flip-Flop (WDFF) to pass write current in the X-direction of the head.

With WDM grounded the head current direction is controlled by differential inputs WDI, $\overline{WDI}$. For (WDI - $\overline{WDI}$) > 200mV the current is in the X-direction.

The magnitude of the write current (0-pk) given by:

$$Iw = \frac{Vwc}{Rwc}$$

where Vwc (WC pin voltage) = 1.65V ± 5%, is programmed by an external resistor Rwc, connected from pin WC to ground. The actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

where:
Rh = head resistance + external wire resistance, and
Rd = damping resistance.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. In addition a head to ground short circuit protection circuit will shut off the write driver and current to prevent excessive current and power dissipation. Triggering of this feature occurs when the DC voltage at either HDX or HDY is less than 2.0V ± 15% in write mode

READ MODE

The read mode configures the SSI 32H523R as a low noise differential amplifier and deactivates the write current generator. The RDX and RDY outputs are open collectors and are in phase with the "X" and "Y" head ports.

In read mode, the write data channel is powered down to reduce power consumption. Note that in write mode, the read amplifier is deactivated and will not pull any current from the load resistor.

For maximum data security in read mode VCC2 is left open or grounded. This eliminates the voltage source for write current.

TABLE 1: MODE SELECT

WDM	R/$\overline{W}$	MODE
GND	0	Write Differential input
OPEN	0	Write Single-ended input
X	1	Read

PIN DESCRIPTIONS

NAME	TYPE	DESCRIPTION
R/$\overline{W}$	I	Read/Write: a high level selects Read mode
WDI, $\overline{WDI}$	I	Write Data In: toggles the direction of the head current
HDX, HDY	I/O	X, Y Head Connections: current in the X-direction flows into the X-port
RDX, RDY	O	X, Y Read Data: differential read data output
WC	-	Write Current: used to set the magnitude of the write current
WDM	I	Write Data Mode: Ground this pin for direct differential input using both WDI and $\overline{WDI}$, leave open to select TTL input using WDI and the internal Write Data Flip-Flop.
VCC1	-	+5V logic circuit supply
VDD	-	+12V supply for read
VCC2	-	+5V power supply for write current drivers (see note)
GND	-	Ground

Note: To ensure maximum data integrity in write-once servo applications, this pin should be left open or shorted to ground after writing servo information.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	VDD	-0.3 to +14	VDC
	VCC1, 2	-0.3 to +7	VDC
Write Current	Iw	60	mA
Digital Input Voltage	Vin	-0.3 to VCC1 +0.3	VDC
Head Port Voltage	VH	-0.3 to VCC2 +0.3	VDC
RDX, RDY Output Current	Io	-10	mA
Storage Temperature	Tstg	-65 to +150	°C
Package Temperature (20 sec Reflow)		215	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	VALUE	UNITS
DC Supply Voltage	Read Mode	VDD	12 ± 10%	VDC
		VCC1	5 ± 10%	VDC
	Write Mode	VDD	12 ± 5%	VDC
		VCC1	5 ± 5%	VDC
		VCC2	5 ± 5%	VDC
Output Pullup Resistors (to VCC1)		RL	100	Ω
Ambient Temperature	Read Mode	TAR	0 - 70	°C
	Write Mode	TAW	20 - 43	°C
Operating Junction Temperature		Tj	0 to +135	°C

DC CHARACTERISTICS (Unless otherwise specified, recommended operating conditions apply.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply Current		Read Mode	-	-	26	mA
		Write Mode	-	-	10	mA
VCC1 Supply Current		Read Mode	-	-	35	mA
		Write Mode	-	-	36	mA
VCC2 Supply Current		Read Mode, see Note 1	-	-	2	mA
		Write Mode	-	-	12 + Iw	mA
Power Dissipation (Tj = +135°C)		Read Mode, VCC2 = 0	-	-	500	mW
		Write Mode: Iw = 40mA	-	-	500	mW
Input Low Voltage (VIL)		Includes WDI w/WDM = open	-	-	0.8	VDC
Input High Voltage (VIH)		Includes WDI w/WDM = open	2.0	-	-	VDC
Input Low Current (IIL)		VIL = 0.8v	-0.4	-	-	mA
Input High Current (IHL)		VIH = 2.0v	-	-	100	µA
Input Voltage (WDI, $\overline{WDI}$)		WDM = GND	3.0	-	VCC1	VDC
Differential Input Voltage (WDI, $\overline{WDI}$)		WDM = GND	200	-	-	mVDC
VDD Fault Voltage			8. 5	-	10.0	VDC
VCC1 Fault Voltage			3.5	-	4.1	VDC
Head Current (HDX, HDY)	Write Mode	0 ≤ VDD ≤ 8.5V 0 ≤ VCC1 ≤ 3.5V	-200	-	+200	µA
	Write Mode	VCC2 = open or ground	-200	-	+200	µA
	Read Mode	0 ≤ VCC1 ≤ 5.5V 0 ≤ VDD ≤ 13.2V	-200	-	+200	µA

Note 1: If VCC2 is at ground or open this current is zero.

WRITE CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply, Iw = 15mA, Lh = 1.5µH, Rh = 30Ω
f(DATA) = 5MHz, and +20°C < Tj < + 135°C

PARAMETER	CONDITIONS	MIN.	NOM	MAX	UNITS
WC Pin Voltage (Vwc)		-	1.65 ± 5%	-	V
Differential Head Voltage Swing		3.4	-	-	Vpp
Differential Output Capacitance		-	-	25	pF
Differential Output Resistance		800	1000	1400	Ω
Write Current Range		10	-	40	mA

4

READ CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply, CL (RDX, RDY) < 20pF

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain		Vin=1mVpp @1MHz, T_A = 25°C	200	250	300	V/V
Gain Sensitivity		15°C < T_A < 55°C	-	-0.16	-	%/°C
Bandwidth	-1dB	|Zs|<5Ω, Vin = 1mVpp @ 300kHz	10	20	-	MHz
	-3dB	|Zs|<5Ω, Vin = 1mVpp @ 300kHz	20	45	-	MHz
Input Noise Voltage		BW=15MHz, Lh=0 µH, R =0Ω	-	0.7	1.0	nV/√Hz
Differential Input Capacitance		Vin = 1mVpp, f = 5MHz	-	40	45	pF
Differential Input Resistance		Vin = 1mVpp, f = 5MHz	460	750	1.4K	Ω
Dynamic Range		AC input voltage where gain falls to 90% of its small signal gain value, f=5MHz	±2	-	-	mV
Common Mode Rejection Ratio		Vin = 0VDC+100mVpp @ 5MHz	54	-	-	dB
Power Supply Rejection Ratio		100m Vpp @ 5MHz on VDD, 100m Vpp @ 5MHz on VCC1	54	-	-	dB
Output Offset Voltage		Vin = 0V	-600	-	+600	mV
Output Voltage (Common Mode)		Inputs shorted together, and outputs shorted together	**	-	*	VDC

*VCC1 - 0.42
**VCC1 - 1.0

SWITCHING CHARACTERISTICS (See Figure 1)
Unless otherwise specified, recommended operating conditions apply, Iw = 15mA, Lh = 0, Rh = 0, f(DATA) = 5MHz, and +20°C < T_A < +43°C

PARAMETER	CONDITIONS	MIN	MAX	UNITS
R/$\overline{W}$				
R/$\overline{W}$ to Write Mode	Delay to 90% of write current	-	0.6	µs
R/$\overline{W}$ to Read Mode	Delay to 90% of 100mV 10MHz Read signal envelope or to 90% decay of write current	-	0.6	µs
Head Current				
Prop. Delay - TD1	From 50 % points, Lh=0µh, Rh=0Ω	-	32	ns
Asymmetry	Input has 50 % duty cycle and 1ns rise/fall time, Lh=0µh, Rh=0Ω	-	1	ns
Rise/Fall Time	10% - 90% points, Lh=0µh, Rh=0Ω	-	13	ns

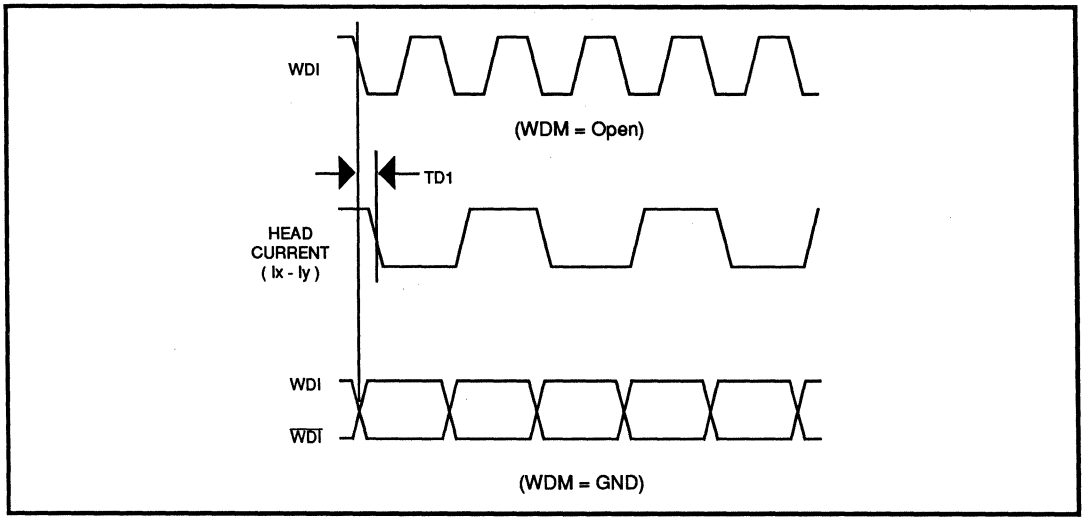


FIGURE 1: WRITE MODE TIMING DIAGRAM

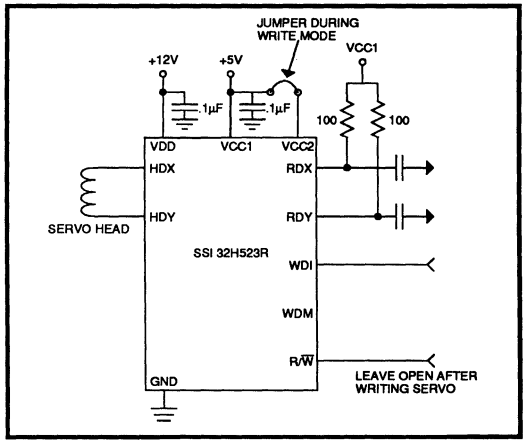


FIGURE 2: TYPICAL APPLICATION

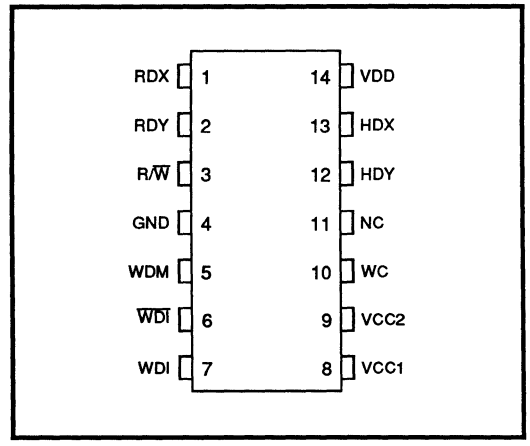


FIGURE 3: PACKAGE PIN DESIGNATIONS
(TOP VIEW)
14-PIN SON

4

ORDERING INFORMATION

PART DESCRIPTON	ORDER NO.	PKG. MARK
SSI 32H523R Read/Write IC	SSI 32H523R-N	32H523R-N

silicon systems™
Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

NOTES:

SSI 32H566R
Ferrite Single-Channel Servo Read/Write Device

August, 1988

DESCRIPTION

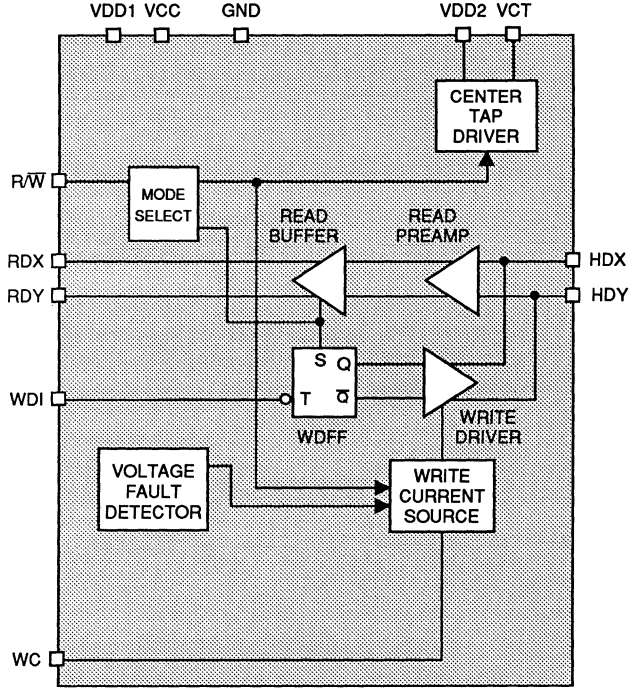
The SSI 32H566R Read/Write device is a bipolar monolithic integrated circuit designed for use with center-tapped ferrite recording heads. It provides a low noise read amplifier, write current control and data protection circuitry for a single channel. The SSI 32H566R provides internal 750Ω damping resistors. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode.

FEATURES

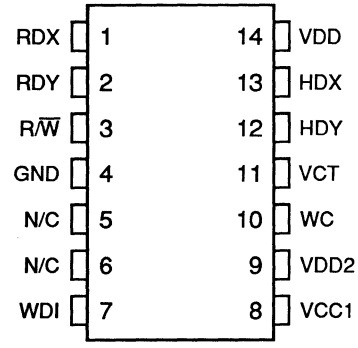
- **High performance:**
  - **Read mode gain = 150 V/V**
  - **Input noise = 1.5nV/√Hz max.**
  - **Input capacitance = 20 pF max.**
  - **Write current range = 10 mA to 40 mA**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Designed for center-tapped ferrite heads**
- **Programmable write current source**
- **TTL compatible control signals**
- **+5V, +12V power supplies**
- **Socket compatible with the SSI 32H523R**

4

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32H566R provides center-tapped ferrite head write drive or read amplification. Mode control is accomplished with pin R/$\overline{W}$. Internal resistor pullups, provided on pin R/$\overline{W}$, will force the device into a non-writing condition if a control line is opened accidentally.

WRITE MODE

The write mode configures the SSI 32H566R as a current switch. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI).

The magnitude of the write current (0-pk) is programmed by an external resistor RWC, connected from pin WC to ground and is given by:

$$Iw = \frac{K}{RWC}$$

where K is the Write Current Constant.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing.

To reduce internal power dissipation, an optional external resistor, RCT, given by RCT ≤ 130Ω x 40/Iw (Iw in mA), is connected between pins VDD1 and VDD2. Otherwise connect pin VDD1 to VDD2.

To initialize the Write Data Flip Flop (WDFF) to pass current through the X-side of the head, pin WDI must be low when the previous read mode was commanded.

READ MODE

The read mode configures the SSI 32H566R as a low noise differential amplifier and deactivates the write current generator. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent pulse detection circuitry.

PIN DESCRIPTIONS

NAME	TYPE	DESCRIPTION
R/$\overline{W}$	I	Read/Write - A high level selects Read Mode
WDI	I	WRITE DATA IN - Negative transition toggles direction of head current
HDX, HDY	I/O	X,Y head connections
RDX, RDY	O	X, Y READ DATA - Differential read signal output
WC	I	WRITE CURRENT - Used to set the magnitude of the write current
VCT	O	VOLTAGE CENTER TAP - Voltage source for head center tap
VCC	-	+5V
VDD1	-	+12V
VDD2	-	Positive power supply for the center-tap voltage source
GND	-	GROUND

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

All voltages referenced to GND. Currents into device are positive. Maximum limits indicate when permanent device damage occurs. Continuous operation at these levels is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

PARAMETER		RATING	UNIT
VDD1	DC Supply Voltage	-0.3 to +14	VDC
VDD2	DC Supply Voltage	-0.3 to +14	VDC
VCC	DC Supply Voltage	-0.3 to +7	VDC
VIN	Digital Input Voltage Range	-0.3 to VCC + 0.3	VDC
VH	Head Port Voltage Range	-0.3 to VDD1 + 0.3	VDC
Iw	Write Current (0-pk)	60	mA
	RDX, RDY (lo) Output Current	-10	mA
	VCT Output Current	-60	mA
Tstg	Storage Temperature Range	-65 to 150	°C
	Lead Temperature PDIP, Flat Pack (10 sec Soldering)	260	°C
	Package Temperature PLCC, SO (20 sec Reflow)	215	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VDD1	DC Supply Voltage		10.8	12.0	13.2	VDC
VCC	DC Supply Voltage		4.5	5.0	5.5	VDC
Lh	Head Inductance				15	µH
RCT*	RCT Resistor	Iw = 40 mA	123	130	137	Ω
Iw	Write Current (0-pk)		10		40	mA
Tj	Junction Temperature Range		+25		+135	°C

*For Iw = 40 mA. At other Iw levels refer to Applications Information that follows this specification.

DC CHARACTERISTICS (Recommended operating conditions apply unless otherwise specified.)

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC Supply Current					
Read	Read Mode			13	mA
Write	Write Mode			25	mA
VDD Supply Current (sum of VDD1 and VDD2)					
Read	Read Mode			33	mA
Write	Write Mode			10+Iw	mA
Power Dissipation (Tj = +135°C)					
Read	Read Mode			500	mW
Write	Write Mode, Iw = 40 mA, RCT = 0Ω			700	mW
	Write Mode, Iw = 40 mA, RCT = 130Ω			500	mW

DIGITAL I/O

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIL	Input Low Voltage				0.8	VDC
VIH	Input High Voltage		2.0			VDC
IIL	Input Low Current	VIL = 0.8V	-0.4			mA
IIH	Input High Current	VIH = 2.0V			100	µA

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCT Center Tap Voltage	Write Mode		6.7		VDC
Head Current (per side)	Write Mode, 0 ≤ VCC ≤ 3.7V, 0 ≤ VDD1 ≤ 8.7V	-200		200	µA
Write Current Range		10		40	mA
Write Current Constant "K"		2.375		2.625	
Iwc to Head Current Gain			0.99		mA/mA
RDX, RDY Output Offset Voltage	Write/Idle Mode	-20		+20	mV

WRITE MODE (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
RDX, RDY Common Mode Output Voltage	Write/Idle Mode		5.3		VDC
RDX, RDY Leakage	RDX, RDY = 6V Write/Idle Mode	-100		100	µA

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCT Center Tap Voltage	Read Mode		4.0		VDC
Head Current (per side)	Read or Idle Mode 0 ≤ VCC ≤ 5.5V 0 ≤ VDD1 ≤ 13.2V	-200		200	µA
Input Bias Current (per side)				45	µA
Output Offset Voltage	Read Mode	-615		+615	mV
Common Mode Output Voltage	Read Mode	4.5		6.5	VDC

DYNAMIC CHARACTERISTICS AND TIMING
(Iw = 35 mA, Lh = 10 µH, Rd = 750Ω, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 20 pF. Recommended operating conditions apply unless otherwise specified.)

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Head Voltage Swing		7.0			V(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance		600		960	Ω

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Voltage Gain	Vin = 1 mVpp @ 300 KHz ZL(RDX), ZL(RDY) = 1 KΩ	125		175	V/V
Dynamic Range	AC Input Voltage, Vi, @ 300 KHz Where Gain Falls by 10%.	±2			mV

READ MODE (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	30			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			1.5	nV/√Hz
Differential Input Capacitance	f = 5 MHz			20	pF
Differential Input Resistance	f = 5 MHz	500		1000	Ω
Common Mode Rejection Ratio	Vcm = VCT + 100 mVpp @ 5 MHz	50			db
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VDD1, VDD2 or VCC	45			db
Single Ended Output Resistance	f = 5 MHz			30	Ω
Output Current	AC Coupled Load, RDX to RDY	±2.1			mA

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
R/$\overline{W}$					
R/$\overline{W}$ To Write Mode	Delay to 90% of Write Current			1.0	µs
R/$\overline{W}$ to Read Mode	Delay to 90% of 100 mV 10 MHz Read Signal Envelope or to 90% decay of Write Current			1.0	µs
Head Current (Lh = 0µH, Rh = 0Ω)					
Prop Delay - TD1	From 50% points			25	ns
Asymmetry	WDI has 50% duty cycle and 1 ns Rise/Fall Time			2	ns
Rise/Fall Time	10% - 90% points			20	ns

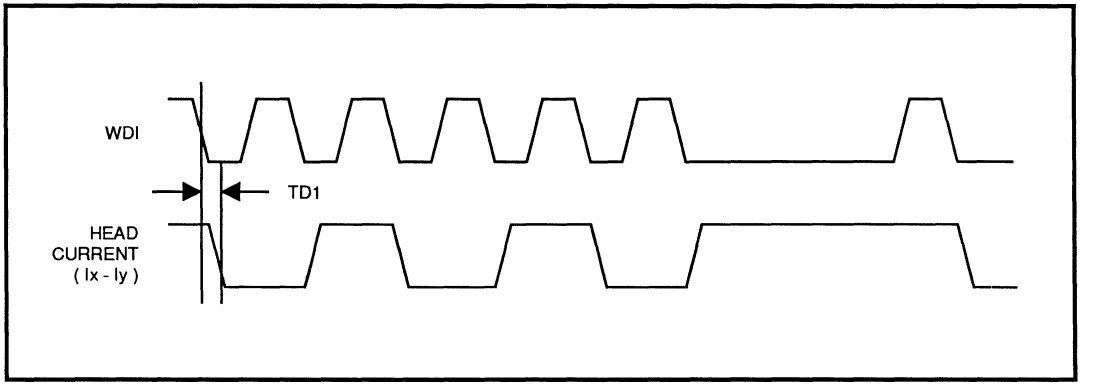


FIGURE 1: Write Mode Timing Diagram

APPLICATIONS INFORMATION

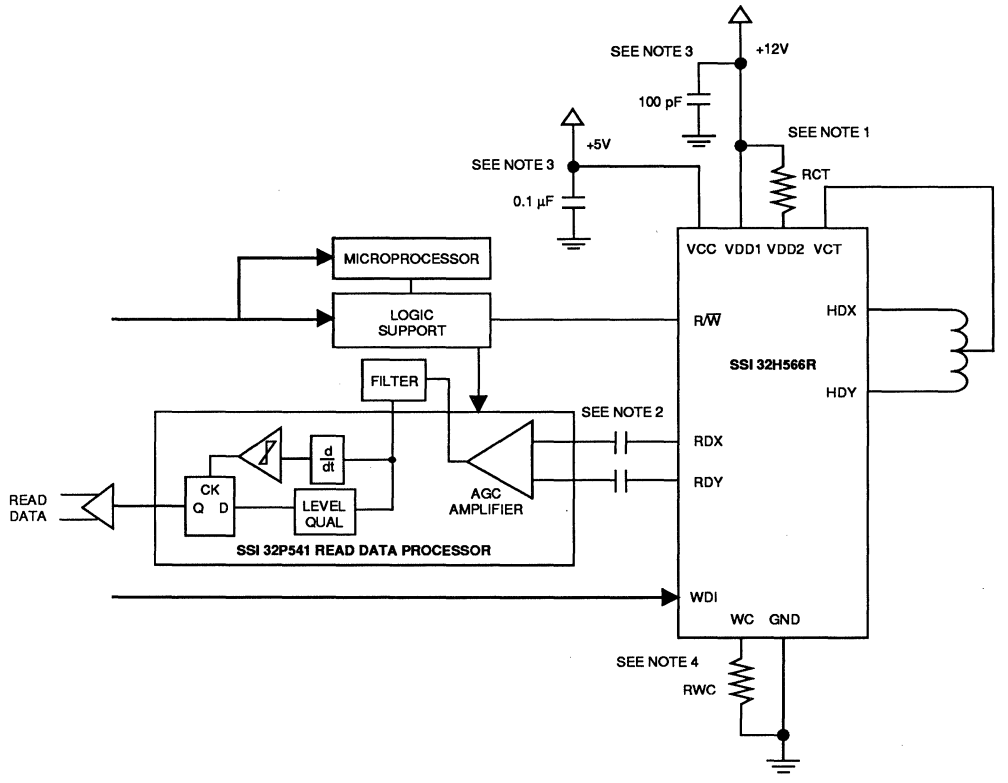
The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher input impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representative of actual performance.

TABLE 3: KEY PARAMETERS UNDER WORST CASE INPUT NOISE CONDITIONS

PARAMETER	Tj=25°C	Tj=125°C	UNIT
Inputs Noise Voltage (max.)	1.1	1.5	nV/√Hz
Differential Input Resistance (min.)	850	1000	Ω
Differential Input Capacitance (max.)	11.6	10.8	pF

TABLE 4: KEY PARAMETERS UNDER WORST CASE INPUT IMPEDANCE CONDITIONS

PARAMETER	Tj=25°C	Tj=125°C	UNIT
Inputs Noise Voltage (max.)	0.92	1.2	nV/√Hz
Differential Input Resistance (min.)	500	620	Ω
Differential Input Capacitance (max.)	10.1	10.3	pF



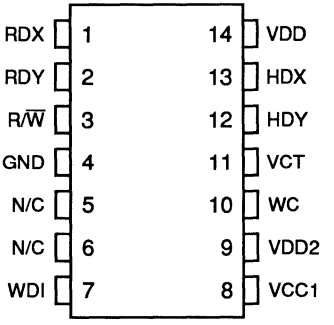
NOTES

1. An external resistor, RCT, given by; RCT ≤ 130 (40/Iw) where Iw is the zero-peak write current in mA, can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.
2. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF.
3. The power bypassing capacitor must be located close to the device with its ground returned directly to device ground, with as short a path as possible.
4. To reduce ringing due to stray capacitance this resistor should be located close to the device. Where this is not desirable a series resistor can be used to buffer a long WC line.

FIGURE 2: Typical Application

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



14-Pin SON

THERMAL CHARACTERISTICS: Øja = 130 °C/W

4

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32H566R Servo Ferrite Single Channel Read/Write Device		
14-Pin SON	SSI 32H566R-N	32H566R-N

silicon systems™
Silicon Systems, Inc., 14351 Myford Road, Tustin, CA. 92680 (714) 731-7110, TWX 910-595-2809

NOTES:

SSI 32H567
Servo Demodulator

silicon systems™
INNOVATORS IN INTEGRATION

August, 1988

DESCRIPTION

The SSI 32H567 Servo Demodulator is a bipolar device intended for use in Winchester disk drives with dedicated surface head positioning systems. It processes a di-bit quadrature pattern read from the servo surface by a preamplifier, such as the SSI 32H101 or SSI 32H116, and generates normal and quadrature (N and Q) position reference signals. These signals provide the servo controller with position error feedback. A complete position control system can be realized with the SSI 32H567 and its companion devices, the SSI 32H568 Servo Controller and SSI 32H569 Servo Motor Driver.

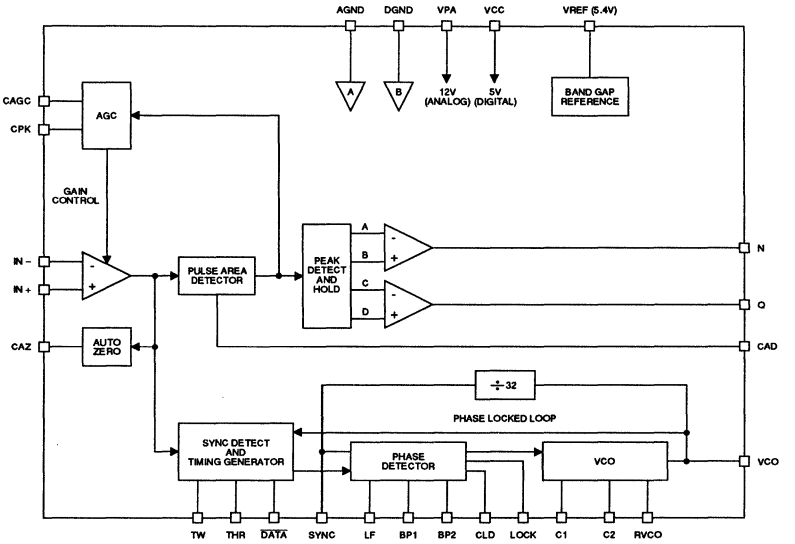
The SSI 32H567 incorporates an input amplifier with automatic gain control and offset cancellation, a phase locked loop and sync separator to recover timing information, and pulse area detectors to recover the position information embedded in a di-bit quadrature servo pattern. In addition, a bandgap voltage generator provides an analog reference level for the entire servo electronics path. External components are used to set the operating characteristics of the SSI 32H567, such as AGC response, VCO center frequency, PLL response and sync separator threshold. Its high performance analog/digital circuitry is capable of supporting servo frame rates of up to 500 KHz.

FEATURES

- **Servo signal demodulation for Winchester disk drives with dedicated surface head positioning systems**
- **Supports industry standard di-bit quadrature servo pattern with frame rates up to 500 KHz**
- **N, Q outputs convey track crossing and position error information**
- **Pulse area detection technique for superior noise immunity**
- **PLL for timing recovery and synchronization**
- **Adjustable sync separator threshold**
- **Auto-zeroing AGC input amplifier**
- **Precision bandgap voltage reference output**
- **Advanced bipolar process dissipates less than 850 mW (5V, 12V)**
- **Available in 28-pin PLCC or 28-pin DIP**

4

BLOCK DIAGRAM



0888

FUNCTIONAL DESCRIPTION

(Refer to block diagram, and typical application, Fig.2)

The SSI 32H567 processes servo position information which is read from a dedicated surface by a pre-amplifier. The servo information must conform to the 'di-bit quadrature' pattern which is illustrated in Figure 3. Servo frames, consisting of data and sync pulses followed by four information pulses (A, B, C, D) are prerecorded along each track of the servo surface. All the servo frames on an individual track are identical, but in the radial direction four different frame types are encountered, with every fourth track being identical. The N signal generated by the SSI 32H567 is proportional to the difference in sizes of pulses A and B, while the Q signal is proportional to the difference between pulses C and D. When the read head is off track, the read signal is effectively a linear interpolation between the prerecorded information of two adjacent tracks, making it possible to sense the head displacement exactly.

The SSI 32H567 has a differential input amplifier which incorporates offset voltage cancellation and automatic gain control. An external read preamplifier must provide a differential input signal of 23 to 400 mV peak to peak from the servo read head. This signal is applied to a pulse area detector whose output is proportional to the area under the positive half of the input pulse. The external capacitor C_{AD} integrates the incoming pulses while they are positive, and is discharged when they go negative. This area detection technique provides improved noise immunity over voltage detection.

An AGC circuit adjusts the input gain so that the maximum pulse area detector output is 2V peak. The AGC circuit incorporates a peak detector which stores the maximum pulse area signal on the external capacitor C_{PK}. This signal is compared to an internal amplitude reference and the input amplifier gain is adjusted until they are equal. The capacitor C_{AGC} determines the response time of the gain control circuit. An offset cancellation circuit , whose response is set with the external capacitor C_{AZ}, ensures that the average level at the differential amplifier output is zero.

All internal analog signals are referenced to a 5.4V bandgap reference voltage. This level is available at the VREF output, which is capable of supplying 10 mA to the rest of the servo path electronics.

In a standard servo frame, the data and sync pulses are more closely spaced than the information pulses (A-D). This allows the sync detect circuit to recover the SYNC pulses. A threshold, which is defined as percentage of the peak signal at the output of the AGC amplifier, is set externally with R_{TH}. Pulses which exceed this threshold are defined as valid pulses (ie. potentially SYNC or DATA). As illustrated in Figure 5, at the end of the positive going half of a valid pulse, a window set by Rw and Cw is opened. If a second valid pulse occurs within this window, it is recognized as a SYNC pulse. This pulse becomes the input signal to a phase locked loop whose VCO clock frequency is 32 times the SYNC frequency (servo frame rate). The $\overline{DATA}$ output pin is low whenever a SYNC pulse is detected. The example illustrated in Figure 5 includes the case of a missing DATA pulse. The SYNC clock output, which marks the start of a new servo frame, is derived from the VCO output so that the clock continues to run when a data pulse is missing. Absolute positioning information such as track 0 and guardband flags may be encoded on the servo surface by the omission of data pulses.

The phase detector compares the detected sync pulses with the SYNC output. A current pulse proportional to the phase error is applied to an external loop filter network connected to the LF pin, to generate the VCO control voltage. If improved power supply rejection is required, bypassing may be provided at pins BP1 and BP2. The VCO center frequency is determined by the external components R_{VCO} and C_{VCO}.

A lock detect circuit measures the phase difference between the detected sync pulses and the sync output. When this difference exceeds half of a VCO clock cycle, a pulse of discharge current is applied to CLD. Otherwise a pulse of charging current is applied to CLD.

A clamp circuit limits the swing of the CLD pin and also insures that a small amount of hysteresis is present. When the voltage on CLD falls below the upper clamp level by more than the "lock margin," the LOCK output transistor is turned on. Likewise, when the voltage on CLD rises above the lower clamp level by more than the "unlock margin," the LOCK output transistor is turned off.

Internal timing windows are generated from the recovered SYNC pulse and VCO clock. These windows, WA, WB, WC, and WD, in Figure 4, enable the integra-

FUNCTIONAL DESCRIPTION (Continued)

tion of the A, B, C, D pulses, respectively. Four peak detectors at the output of the pulse area detector are enabled in succession to capture the A, B, C and D information pulses, and the N and Q analog outputs are formed by differencing adjacent pulses. These outputs change during a servo frame and only become valid after the D pulse has been detected. N and Q should be sampled by the servo controller on the next falling edge of the SYNC output clock.

An example of an entire servo path implemented with the SSI 32H567 and its companion devices, the SSI 32H568 and SSI 32H569, is shown in Figure 7.

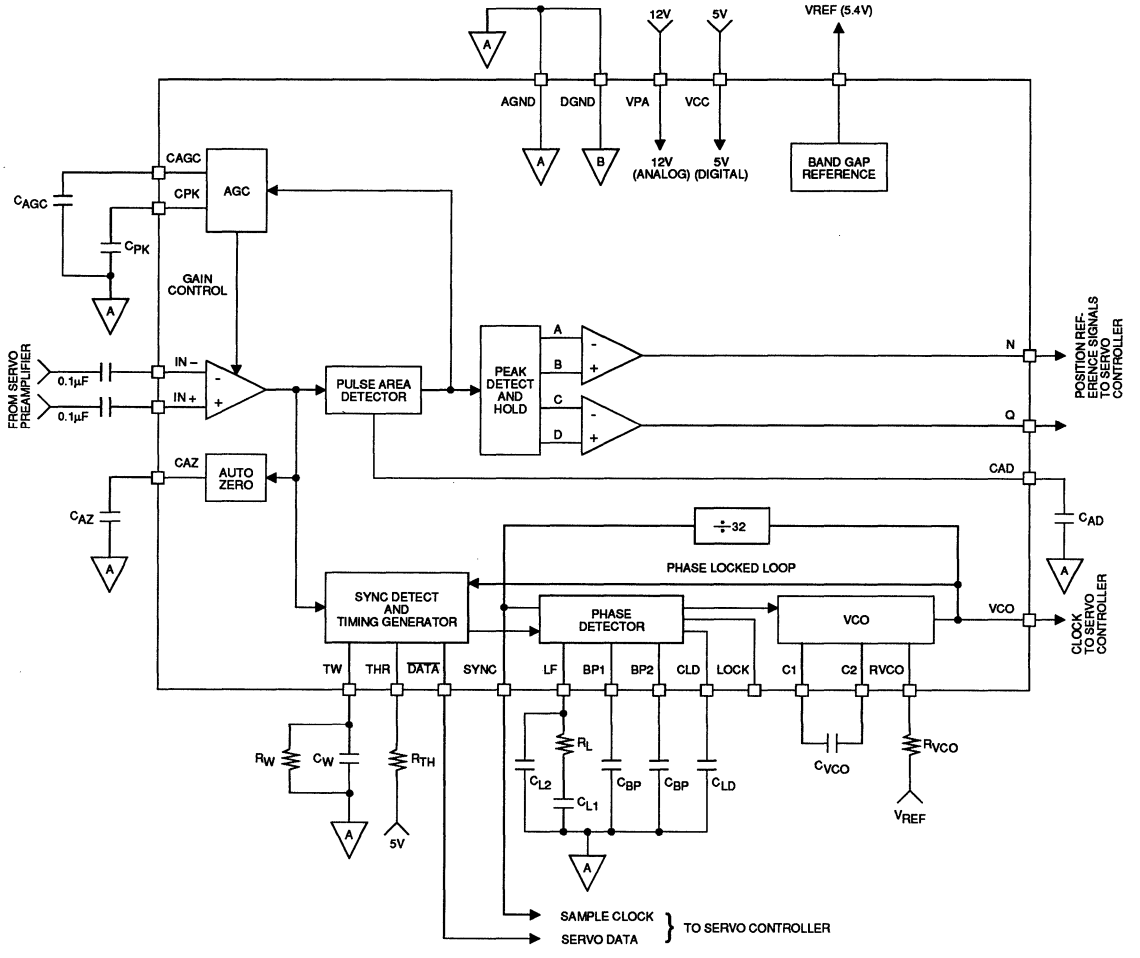


FIGURE 2: TYPICAL APPLICATION

PIN DESCRIPTION

POWER

NAME	TYPE	DESCRIPTION
VREF	O	REFERENCE VOLTAGE - 5.4V output. All analog signals are referenced to this voltage.
AGND	-	ANALOG GROUND
VPA	-	ANALOG SUPPLY - 12V power supply.
VCC	-	DIGITAL SUPPLY - 5V power supply.
DGND	-	DIGITAL GROUND

INPUT AMPLIFIER

NAME	TYPE	DESCRIPTION
CAZ	-	AUTOZERO CAPACITOR - A capacitor which sets the response of the input amplifier offset cancellation circuit should be connected between this pin and analog ground.
IN +	I	NON-INVERTING INPUT - AGC input amplifier connection. The non-inverting output of the differential servo pre-amplifier should be AC coupled to this pin.
IN -	I	INVERTING INPUT - AGC input amplifier connection. The inverting output of the differential servo pre-amplifier should be AC coupled to this pin.
CPK	-	PEAK HOLD CAPACITOR - A capacitor which is used by the peak detector of the AGC circuitry must be connected between this pin and analog ground.
CAGC	-	AGC CAPACITOR - A capacitor which sets the AGC attack and decay times must be connected between this pin and analog ground.

TIMING RECOVERY

NAME	TYPE	DESCRIPTION
VCO	O	VCO OUTPUT - TTL compatible digital clock which is 32 times the sync frequency (servo frame rate).
C2,C1	-	VCO CAPACITOR - Connection points for a capacitor which sets the VCO center frequency in conjunction with an external resistor connected to RVCO.
BP1,BP2	-	PLL BYPASS - Bypass capacitors may be connected between these pins and analog ground to provide additional power supply rejection in the phase locked loop.

TIMING RECOVERY (Continued)

NAME	TYPE	DESCRIPTION
LF	-	PHASE LOCKED LOOP FILTER - An external RC network which sets the PLL loop characteristics must be connected between this pin and analog ground.
RVCO	-	VCO RESISTOR - Connection for a resistor which sets the VCO center frequency, in conjunction with the capacitor between pins C1 and C2. The resistor must be connectedbetween this pin and the VREF output.
SYNC	O	SYNC OUTPUT - TTL compatible digital clock whose falling edge indicates the presence of valid analog signals on the N and Q outputs. There is one SYNC cycle per servo frame.
$\overline{\text{DATA}}$	O	DATA OUTPUT - Active low TTL compatible digital output that indicates the presence of a data pulse in the servo frame. This signal is updated on the falling edge of the SYNC output.
TW	-	TIMING WINDOW - A resistor and capacitor must be connected in parallel between this pin and analog ground to set a timing window which is used in detecting SYNC pulses.
THR	-	PULSE THRESHOLD - A resistor which sets a threshold for SYNC and $\overline{\text{DATA}}$ pulse detection must be connected between this pin and VCC (digital 5V supply).
CLD	-	LOCK DETECT CAPACITOR - The value of this capacitor determines how quickly the LOCK output responds.
LOCK	O	LOCK OUTPUT - An open collector output that indicates the lock status of the PLL.

POSITION INFORMATION

NAME	TYPE	DESCRIPTION
CAD	-	AREA DETECTOR CAPACITOR - A capacitor, which forms an integrator to sense the pulse area of the servo position signals, must be connected between this point and analog ground.
N	O	N OUTPUT - This sampled analog signal is the normal position reference output. N is referenced to VREF and is periodic in radial displacement, with a period of 4 tracks.
Q	O	Q OUTPUT - This sampled analog signal is the quadrature position reference output. Q is referenced to VREF and is periodic in radial displacement, with a period of 4 tracks. It is 90 degrees out of phase with N.
No connects on PLCC package: 4, 7		

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicates where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC voltage		0		8	V
VPA voltage		0		16	V
Voltage on PLL inputs		-0.5		VCC+0.5	V
Voltage on other inputs		0		14	V
Storage Temp.		-45		160	°C
Solder Temp.	10 sec. duration			260	°C

RECOMMENDED OPERATION CONDITIONS (Unless otherwise noted, the following conditions are valid throughout this document.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VPA, analog supply		10.8	12	13.2	V
Supply noise	F<1 MHz			0.1	Vp-p
VCC, digital supply		4.75	5	5.25	V
Ta, ambient temperature		0		70	°C

DC CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IPA, VPA current				50	mA
ICC, VCC current				52	mA
VOH, digital output high	|IOH|<40 µA	2.4			V
VOL, digital output low	|IOL|<1.6 mA			0.4	V
IREF, VREF output current capacity		10			mA
VREF output voltage	|IREF|<10 mA	5.1	5.4	5.7	V

ELECTRICAL SPECIFICATIONS (Continued)

AC CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VREF output impedance	IOUT = 0-10 mA 1 µF bypass to AGND Frequency<15MHz			7	Ω
N, Q outputs					
Output impedance	F = 1 MHz			100	Ω
Load resistance	To VREF	10			KΩ
Load capacitance				50	pF
Peak output voltage	Referenced to VREF 23-400 mVp-p differential	1.8	2	2.2	V
Offset voltage				10	mV
Input amplifier					
Input resistance		5			KΩ
Input resistance mismatch				1	%
Input capacitance				20	pF
Bandwidth		10	20		MHz
Input referred noise	10 Hz<F<40 MHz		30		nV/√Hz
CMRR	F<1MHz	60			dB
PSRR	F<0.5MHz	45			dB
AGC dynamic range	C_{AD}(pF)=720/fvco(MHz)	26			dB
AGC headroom		2			dB
AGC bandwidth	Open loop unity gain C_{AGC}=0.04 µF C_{PK}=1500 pF	5		15	KHz
Autozero pole	C_{AZ} in µF		220/C_{AZ}		Hz
SYNC detector					
Timing window	Rw in Ω, Cw in pF		0.4(Rw • Cw)		s
Valid pulse threshold	R_{TH} in KΩ (% of full scale)		55/R_{TH}		%
LOCK Detector					
CLD up current	RVCO = 11K ± 1%	0.7		3	µA
CLD down current	RVCO = 11K ± 1%	3		10	µA
CLD lock margin		0.7		1.3	V
CLD unlock marign		0.7		1.3	V
CLD hysteresis		0.1		0.4	V

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AC CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Phase locked loop					
Capture range		20			%
VCO phase shift	Missing DATA pulse			0.005	rad/frame
VCO phase delay	Relative to sync pulse zero crossing			30	ns
VCO center frequency range		4		16	MHz
Center frequency error	Cvco, Rvco 1%			15	%
VCO gain	fvco in Hz		10.47 fvco		rad/s/V
Phase detector gain			15.92		uA/rad

TIMING CHARACTERISTICS
(Digital output load capacitance Cl<15 pF, VCO frequency fvco <16 MHz, timing measurements for digital signals are measured at 1.3V, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TDD, data delay				20	ns
TW, sync pulse width		40			ns
TSKW, SYNC to VCO skew		0		40	ns
SYNC fall time		15			ns
TADS, N or Q output setup time		260			ns
TADH, N or Q output hold time		0			ns
T1 accuracy, T1-32/fvco		-8		8	ns
T2 accuracy, T2-6/fvco		-4		4	ns
T3 accuracy, T3-12/fvco		-4		4	ns
T4 accuracy, T4-18/fvco		-4		4	ns
T5 accuracy, T5-24/fvco		-4		4	ns
T6 accuracy, T6-1.5/fvco		-5		10	ns
T7 accuracy, T7-2/fvco		-5		10	ns

APPLICATIONS INFORMATION

A typical SSI 32H567 application is shown in Figure 2. The selection criteria for the external components shown are discussed below.

INPUT AMPLIFIER

The autozero circuit is effectively a high pass filter, whose pole frequency is given by:

$$f_{AZ} = \frac{220}{C_{AZ}(\mu F)} Hz$$

With a value of 10 µF for C_{AZ}, the autozero circuit's corner frequency will be 22 Hz. This is sufficient for DC offset rejection and it will not interfere with the servo signal.

The AGC response may be characterized in terms of the open loop unity gain bandwidth of its control loop. The nominal value for this loop is set by C_{AGC} as follows:

$$f_{BW} = \frac{390}{C_{AGC}(\mu F)} Hz$$

For a nominal bandwidth of10 kHz, C_{AGC} should be 0.039 µF. With a 1% capacitor, the variation in actual bandwidth will be +/- 50% due to the tolerance of internal components. The AGC peak detector capacitor should always be set to 1500 pF. This represents a reasonable tradeoff between leakage current tolerance and storage aperture time.

The pulse area detector storage capacitor must be chosen to keep the AGC circuit operating within its linear range. Its value is related to the VCO frequency as follows:

$$C_{AD} = \frac{720}{f_{VCO}(MHz)} pF, \text{ where } f_{VCO} \text{ is the VCO freq.}$$

Larger values for C_{AD} are required with lower VCO frequencies in order to maintain constant signal levels within the device, since the integration time is increased.

SYNC DETECTOR

Two sync detector parameters may be adjusted with external components. The first is the valid pulse threshold. The threshold is expressed as a percentage of a full scale pulse (since the sync detector follows the AGC and input amplitude variations are removed). The threshold is determined with resistor R_{TH} as follows:

$$\text{Threshold} = \frac{0.37}{R_{TH}(K\Omega)} \cdot 100(\%)$$

For example, a value of R_{TH} = 1 KΩ sets the valid pulse threshold at 37% of full scale. This prevents false triggering on noisy signals, but does not unduly shorten the sync pulse.

A timing window is used to detect sync pulses, since the sync and data pulses are more closely spaced than any other pulses in a valid servo signal. The delay from the zero crossing of the data pulse to the leading edge of the sync pulse is 1.5 cycles of the VCO clock. The next most closely spaced pulses (which must be rejected by the sync detect circuit) are separated by 3 VCO cycles. Thus the timing window should be set for 2.25 cycles of the VCO clock, to allow reliable detection of the sync pulse. The timing window is determined as follows:

$$\text{Window} = 0.4(R_W \cdot C_W)(s)$$

The resistor Rw should always be set to 5.6 KΩ, which means that for a 2.25 cycle window, Cw is given by:

$$C_W = \frac{1000}{f_{VCO}(MHz)} pF$$

For a 16 MHz clock, Cw should be chosen as 63 pF.

LOCK DETECTOR

The LOCK detector behavior is controlled by the value of C_{LD}. A value too small will be prone to unlock prematurely and give false warnings to the system. A typical value for C_{LD} is 0.01 µF.

APPLICATIONS INFORMATION (Continued)

PHASE LOCKED LOOP

The VCO center frequency is determined by Rvco and Cvco. Rvco should always be set to 11 KΩ ± 1%. Cvco may then be chosen by:

$$C_{VCO} = \frac{830}{f_{VCO}} - 10.6\,pF,$$

where fvco is the desired center frequency in MHz.

For fvco = 16 MHz, Cvco = 41 pF and for fvco = 4 MHz, Cvco = 200 pF. If 1% tolerance external components are used, the VCO absolute frequency accuracy will be 15%. The VCO output frequency is related to the control voltage at the loop filter pin, V_{LF}, as follows:

$$\frac{f_O}{f_{VCO}} = 1 + 1.667\,(V_{LF} - V_{LFBIAS})$$

This means that the VCO gain, Ko, is given by:

$$K_O = 2 \cdot \pi \cdot f_{VCO}(Hz) \cdot 1.667\ rad/s/V$$

The phase detector is a digitally controlled charge pump, which injects a current into the loop filter whose average value is proportional to the phase error. The detector gain, Kd, is fixed at 15.92 µA/rad. If a loop filter consisting of a series resistor and capacitor is used, as shown in Figure 2, the phase locked loop becomes a second order system with the following transfer function:

$$\frac{\text{phase error}}{\text{input phase}}(s) = \frac{(s/\omega n)^2}{1 + 2 \cdot z \cdot s/\omega n + (s/\omega n)^2}$$

where:

$$\omega n\,(\text{natural freq.}) = \sqrt{((K_d \cdot K_O/(32 \cdot C_{L1}))}\ rad/s$$

$$z\,(\text{damping factor}) = 0.5 \cdot R_L \cdot C_{L1} \cdot \omega n$$

As an example, the values for Cvco, RL and CL are derived for a system with the following specifications:

$$f_{VCO} = 16\,MHz \quad \omega n\,(2 \cdot \pi) = 4600\,Hz \quad z = 0.68$$

$$C_{VCO} = \frac{830}{f_{VCO}} - 10.6 = 41\,pF$$

$$C_{L1} = \frac{K_d K_O}{32 \cdot \omega n^2} = \frac{(15.92 \cdot 10e\text{-}6)\,(10.47 \cdot f_{VCO})}{32\,(2 \cdot \pi \cdot 4600)^2} = 0.1\,\mu F$$

$$R_L = \frac{2 \cdot z}{C_{L1} \cdot \omega n} = 470\,\Omega$$

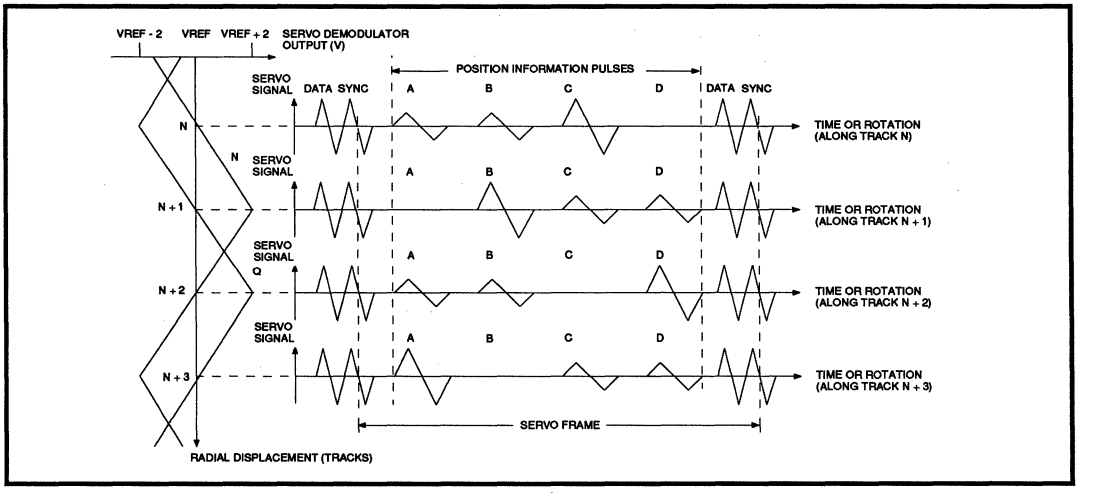


FIGURE 3: PRE-RECORDED SERVO SIGNAL AND SERVO DEMODULATOR OUTPUT VS. RADIAL DISPLACEMENT

0888

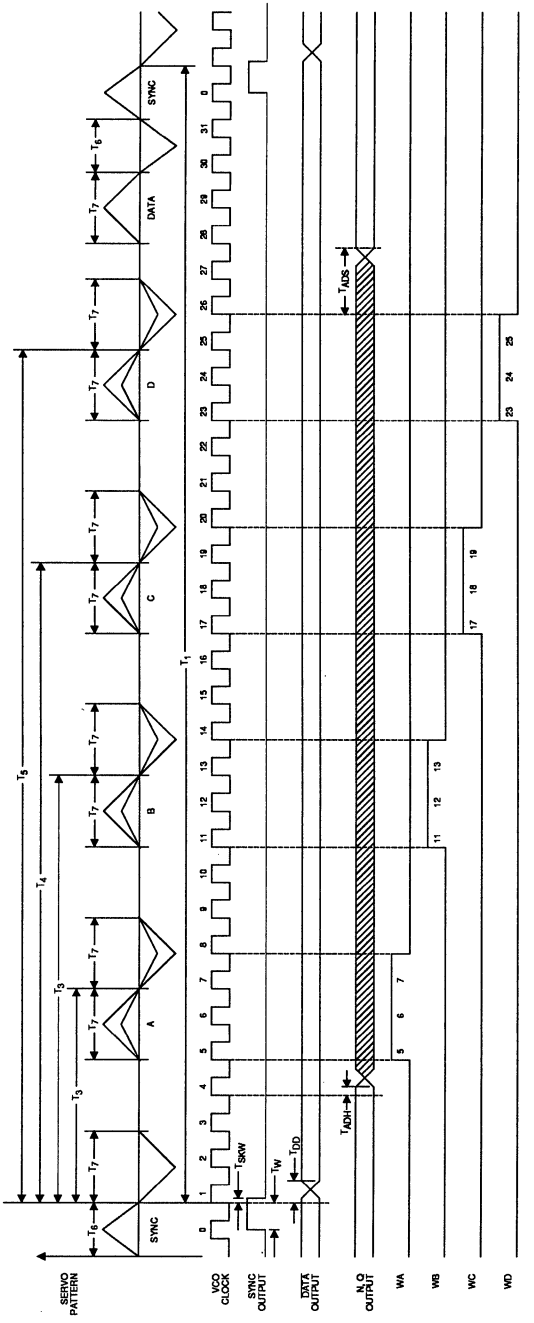


FIGURE 4: TIMING DIAGRAM

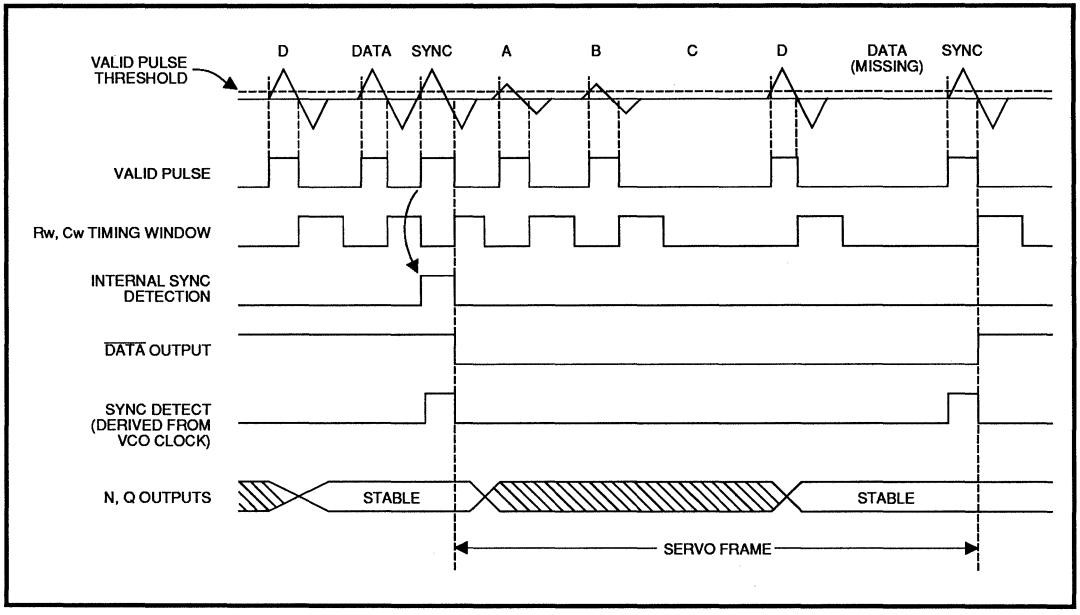


FIGURE 5 : SYNC AND $\overline{\text{DATA}}$ PULSE DETECTION

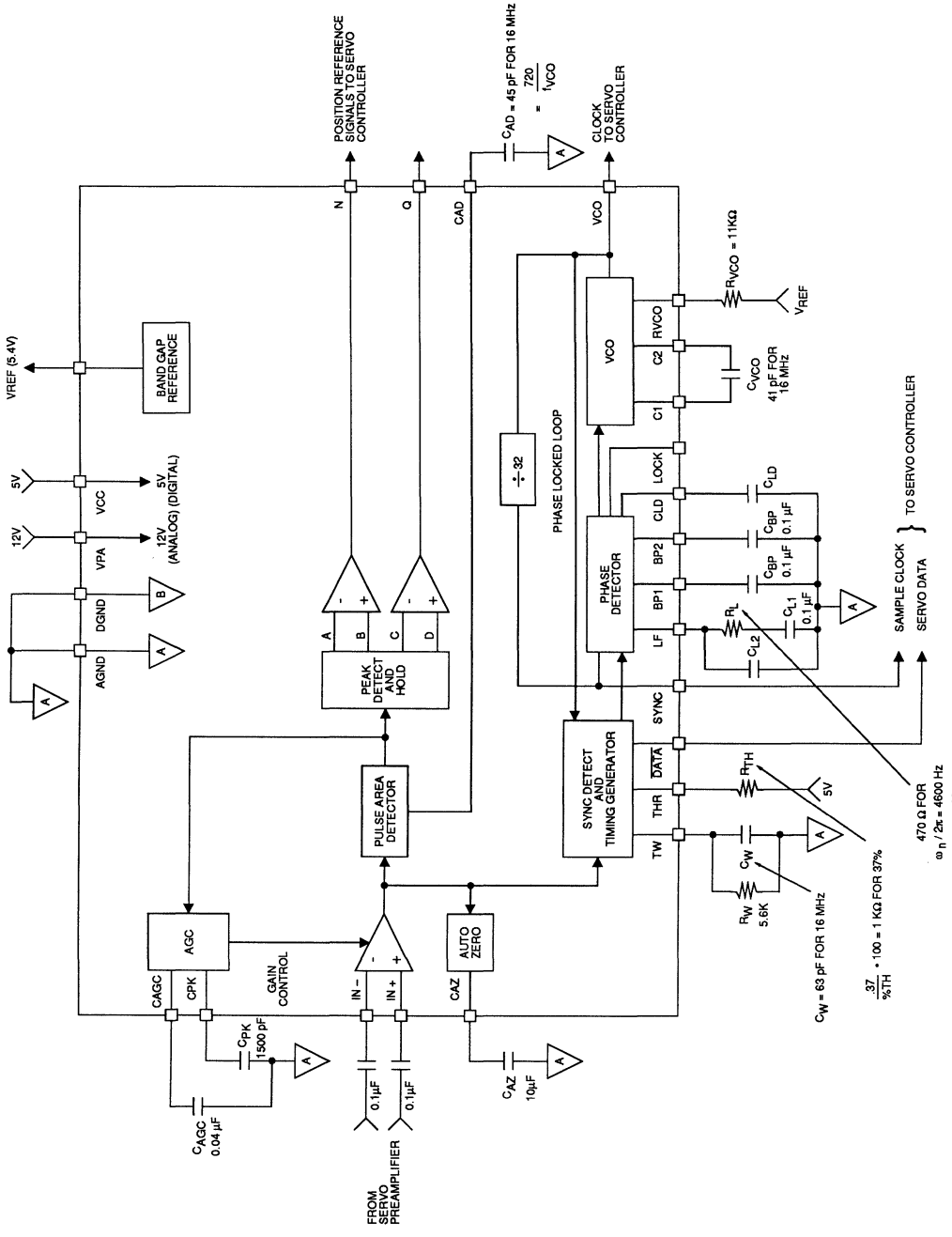


FIGURE 6: DESIGN EXAMPLE FOR 500 KHz FRAME RATE

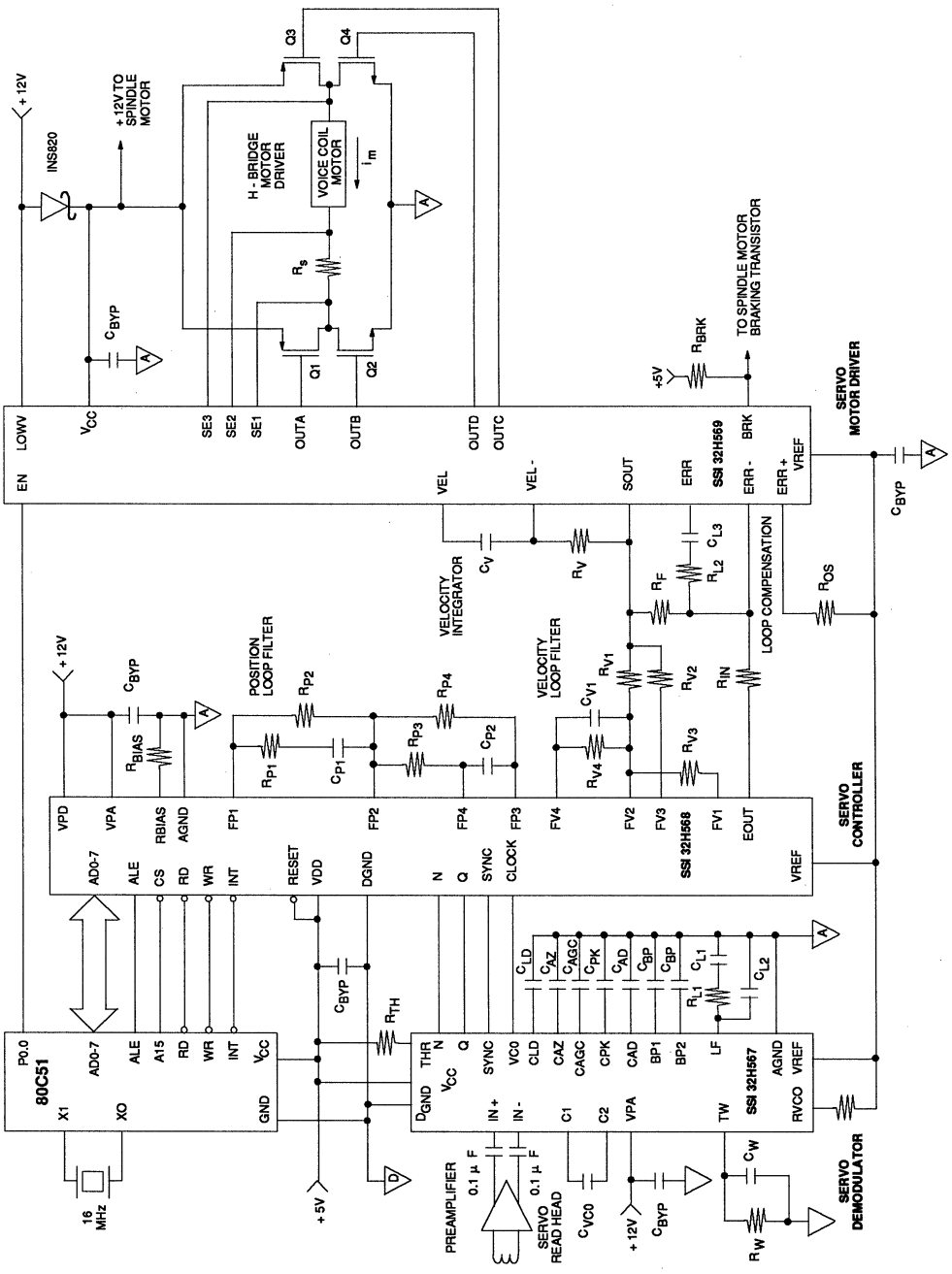
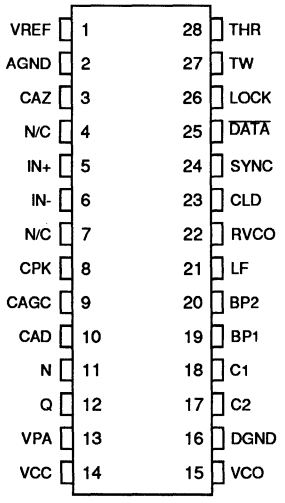


FIGURE 7:
COMPLETE EXAMPLE OF SERVO PATH ELECTRONICS USING SSI 32H567/568/569

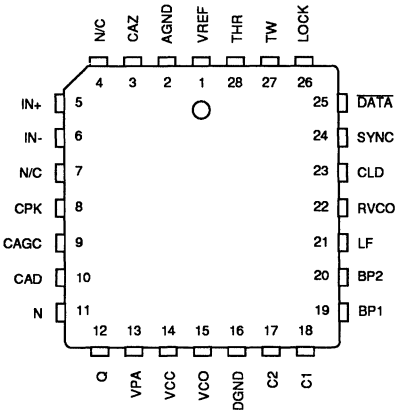
PACKAGE PIN DESIGNATIONS

(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.



28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32H567, Servo Demodulator		
28-Pin DIP	SSI 32H567-CP	32H567-CP
28-Pin PLCC	SSI 32H567-CH	32H567-CH

silicon systems™
Silicon Systems, Inc., 14351 Myford Road, Tustin CA 92680, (714) 731-7110, TWX 910-595-2809

NOTES:

SSI 32H568
Servo Controller

August, 1988

DESCRIPTION

The SSI 32H568 Servo Controller is a CMOS device intended for use in Winchester disk drive head positioning systems. When used in conjunction with a position reference, such as the SSI 32H567 Servo Demodulator, and a motor driver, such as the SSI 32H569 Servo Motor Driver, the device allows the construction of a high performance, dedicated surface head positioning system which operates under microprocessor control.

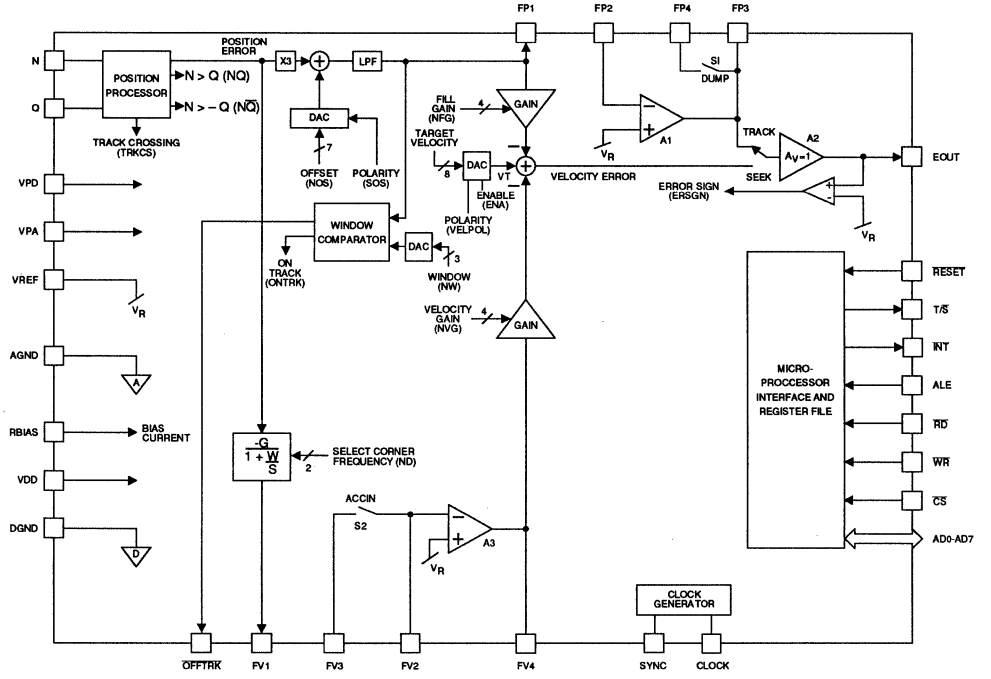
The SSI 32H568 generates position and track crossing information from standard di-bit quadrature position signals, derived from a dedicated servo surface. In its seek mode, the controller attempts to match the actual head velocity to a programmed target value, while in its track mode, it keeps the head centered on a track. Internal status and control registers allow a microprocessor to select operating modes, monitor track information and establish velocity targets. (Continued)

FEATURES

- **Servo control for Winchester disk drives with dedicated surface head positioning systems**
- **Accepts standard di-bit quadrature position information**
- **500 KHz maximum servo frame rate**
- **Microprocessor bus interface compatible with 16 MHz 8051**
- **Seek and track modes**
- **Programmable velocity profile and loop gains**
- **Internal offset cancellation capability**
- **Track crossing interrupt**
- **Low power CMOS design**
- **Available in 32-pin DIP or 44-pin PLCC packaging**

4

BLOCK DIAGRAM



DESCRIPTION (Continued)

The microprocessor bus interface is optimized for use with multiplexed address/data bus microprocessors such as Intel's 8051, operating at up to16 MHz.

The SSI 32H568 is a low power, CMOS device and is available in 32-pin DIP and 44-pin PLCC packaging.

FUNCTIONAL DESCRIPTION

The SSI 32H568 receives position information from a servo demodulator through the analog inputs N and Q, which are sampled on the falling edge of SYNC. FSYNC, the maximum SYNC frequency (which is the servo frame rate) is 500 KHz. The position processor compares the analog N signal with both Q and –Q, to generate the digital signals NQ and N$\overline{Q}$. Since the N and Q signals have a period of four tracks, NQ and N$\overline{Q}$ provide additional information on which track the head is positioned over. Figure 6 shows the behavior of various position signals as radial displacement changes. A track crossing signal (TRKCS) may be programmed to provide an indication of each track crossing, or alternate track crossings. Internal timing hysteresis forces the NQ and N$\overline{Q}$ bits to remain constant for at least two servo frames. This prevents noise at the N and Q inputs from causing multiple track crossing indications at low head velocities.

The SSI 32H568 has two modes of operation, track and seek, which are selected under microprocessor control. In the track mode, the control loop drives the position error signal to zero. In the seek mode, the loop attempts to match the head velocity to a velocity target programmed through the microprocessor interface.

In track mode, the head position error signal is summed with an 8-bit programmable offset signal which may be used to null out circuit offsets or to permit reading of off-track data. This adjusted position error signal is available on pin FP1. A lowpass filter with a corner frequency above 0.1 • FSYNC provides a small amount of smoothing. A position loop filter may be constructed from external RC components and amplifier A1, whose output is switched to buffer amplifier A2 while track mode is selected (control bit T/$\overline{S}$=1). Switch S1, controlled by the DUMP bit, is used to keep the feedback capacitor in the position loop filter discharged while the controller is in seek mode. The output of A2 is the error signal (EOUT) which should be connected to the servo motor driver circuitry. The position error is also applied to a window comparator with programmable limits that provide a digital indication of whether the head is on track or not, through the ONTRK bit in the status register. In systems employing the SSI 32H569, EOUT should be connected to the SSI 32H569 ERR- pin through an input resistor.

The SSI 32H568 has a calibration control which permits the cancellation of position error offsets. When the control bit CAL is set, the inputs to the position processor are switched to VREF instead of N and Q. A comparator connected to the EOUT pin senses the sign of the error signal (ERSGN), allowing the microprocessor to alter the offset DAC input word until an LSB change causes ERSGN to change state. At this point internal offsets in the position error path have been cancelled.

In seek mode, the position error is differentiated by a switched capacitor differencer, to produce a velocity estimate. The differencer does not sample the position error immediately after the discontinuity that occurs when a track boundary is crossed. This prevents the discontinuity from disturbing the differentiator output. The velocity estimate is applied to a velocity loop filter consisting of external RC components and amplifier A3. A signal proportional to motor current may also be summed in at A3, to compensate for the fact that during rapid acceleration the high pass filter does not accurately model a differentiator. Switch S2, controlled by the ACCIN bit, allows the motor current feedback to be altered under microprocessor control. A velocity error term is computed as the difference between the velocity target and the actual head velocity. The velocity target is generated by a DAC from the digital word stored in the TARGET register. The output of the velocity loop filter (pin FV4) is proportional to the actual head velocity and is scaled by a 4-bit programmable velocity gain before being subtracted from the velocity target. Also, a fill signal which is generated by multiplying the position error by a 4-bit programmable fill gain is subtracted from the velocity error. The fill signal compensates for the 8-bit quantization of the velocity target signal, which becomes a factor as the head velocity approaches zero. As the head nears the destination track at the end of a seek operation, the target velocity is zero, so if a fill term which is proportional to position error is subtracted from the velocity error term, the velocity loop will cause the head to come to rest at the center of the track. Without this additional fill signal,

the velocity loop would not necessarily center the head in the destination track. In seek mode, the velocity error signal is switched to buffer amplifier A2, which drives the EOUT pin.

The actual velocity profile of the head is determined by the values written to the target velocity DAC. Typically, a new velocity target is written at each track crossing. An automatic update feature (enabled when UPDATE=1) causes the next velocity target to be loaded from a holding register when a track crossing occurs, so that the microprocessor does not have to perform this time-critical operation.

The SSI 32H568 has 8 registers, described in "Register Description", which are accessed through a microprocessor interface optimized for multiplexed address/data bus processors. A 3-bit register address is latched from the bus on the falling edge of ALE (address latch enable) and a bus cycle occurs if $\overline{CS}$ (chip select) and either $\overline{RD}$ (read strobe) or $\overline{WR}$ (write strobe) are asserted. An open drain interrupt line ($\overline{INT}$) may be used to cause a microprocessor interrupt when a track crossing occurs.

4

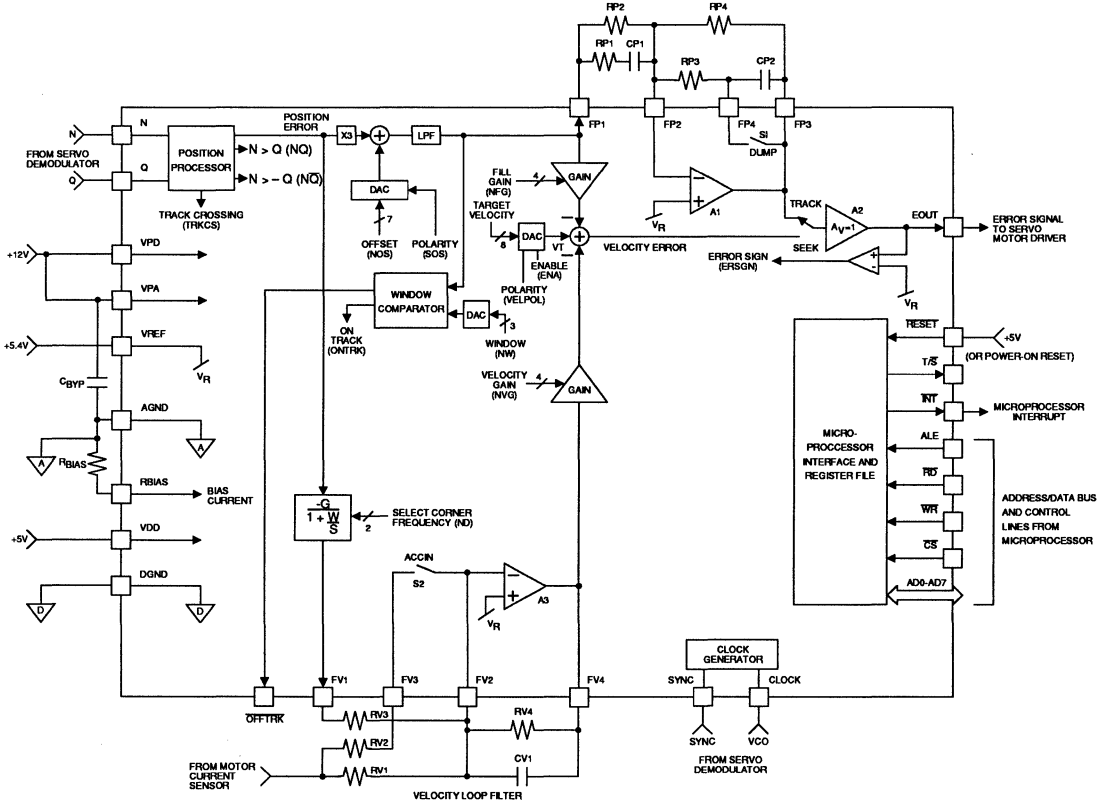


FIGURE 2: SSI 32H568 TYPICAL APPLICATION

PIN DESCRIPTION

POWER

NAME	32-pin DIP	44-pin PLCC	TYPE	DESCRIPTION
RBIAS	11	16	I	BIAS INPUT - This input sets the internal opamp bias currents. A 20 KΩ 1% resistor should be connected between RBIAS and AGND.
VREF	12	17	I	REFERENCE VOLTAGE - 5.4V input which is used as the DC reference level for all analog signals. (This level is available as an output from the SSI 32H567).
AGND	13	19		ANALOG GROUND
DGND	18	27		DIGITAL GROUND
VDD	19	28		DIGITAL 5V SUPPLY - 5 volt supply for the microprocessor interface circuitry.
VPD	31	43		DIGITAL 12V SUPPLY - 12 volt supply for the switched capacitor filter clocks.
VPA	32	44		ANALOG 12V SUPPLY - 12 volt supply for all analog circuitry.

POSITION REFERENCE INTERFACE

Q	9	14	I	QUADRATURE INPUT - Analog position signal from servo demodulator.
N	10	15	I	NORMAL INPUT - Analog position signal from servo demodulator (90 degrees or 1 track out of phase with Q signal).
SYNC	29	40	I	SYNC INPUT - The falling edge of this clock causes the analog information on the N, Q inputs to be sampled. There is one SYNC pulse per servo frame and the maximum rate is 500 KHz. This signal is generated by the SSI 32H567.
CLOCK	30	41	I	CLOCK INPUT - This clock must be either 32 or 72 times the rate of the SYNC clock (selected by the FRFMT bit in STATUS register). It is usually supplied by the VCO output of the servo demodulator (eg. SSI 32H567).

MICROPROCESSOR INTERFACE

$\overline{CS}$	14	21	I	CHIP SELECT - Active low signal enables device to respond to microprocessor read or write.
ALE	15	22	I	ADDRESS LATCH ENABLE - Falling edge latches register address from pins AD0-AD2.
$\overline{RD}$	16	23	I	READ STROBE - Active low signal causes the contents of the addressed register to be placed on the address/data bus (AD0–7) if $\overline{CS}$ is also active.

MICROPROCESSOR INTERFACE (Continued)

NAME	32-pin DIP	44-pin PLCC	TYPE	DESCRIPTION
$\overline{WR}$	17	24	I	WRITE STROBE - Active low signal causes the data on the address/data bus to be written to the addressed register if $\overline{CS}$ is also active.
$\overline{INT}$	20	29	O	INTERRUPT - This active low open drain output is asserted when a track crossing is detected. It is released when the internal track crossing status bit (TRKCS) is read by the microprocessor.
T/$\overline{S}$	-	30	O	TRACK/SEEK - This output reflects the state of the T/$\overline{S}$ bit in the STATUS register. It is high when the device is in track mode and low when it is in seek mode (PLCC package only).
AD7 -AD0	21-28	31-32 34-39	I/O	ADDRESS/DATA BUS - 8-bit bus which carries register address information and bi-directional data.
$\overline{RESET}$	-	42	I	RESET - This active low input is used to force all the internal registers to their reset condition (PLCC package only).
$\overline{OFFTRK}$	-	26	O	OFFTRACK - This open drain output is asserted whenever the head position is outside the window specified by NW. It is always asserted in seek mode (PLCC package only).

CONTROL LOOP

FV4	1	1	O	VELOCITY FILTER OUTPUT - This is the output of amplifier A3 which forms part of the velocity loop filter. This signal is internally amplified and compared to the target velocity.
FV3	2	3	I	VELOCITY FILTER INPUT (SWITCHED) - This input is connected to the inverting input of amplifier A3 through a switch which is closed when control bit ACCIN is set and open when ACCIN is cleared.
FV2	3	5	I	VELOCITY FILTER INPUT - Direct connection to the inverting input of amplifier A3.
FV1	4	7	O	ESTIMATED VELOCITY OUTPUT - Output of the position error differentiating high pass filter.
EOUT	5	9	O	LOOP ERROR SIGNAL - Buffered output which is the position error in track mode (T/$\overline{S}$ = 1) or the velocity error in seek mode (T/$\overline{S}$ = 0). This signal should be connected to the servo motor driver circuitry. In systems using the SSI 32H569 servo driver, EOUT is connected to the SSI 32H569 pin ERR- through a resistor.
FP4	*	11	O	POSITION FILTER CAPACITOR - The external position loop filter feedback capacitor should be connected between this pin and FP3. When the DUMP bit in register WINDOW is set, an internal switch (S1) shorts FP3 to FP4. This allows the external capacitor to be kept discharged during seek mode.

CONTROL LOOP (Continued)

NAME	32-pin DIP	44-pin PLCC	TYPE	DESCRIPTION
FP3	6	10	O	POSITION FILTER OUTPUT - Output of position loop filter amplifier A1. In track mode this signal is the position error and is internally connected to buffer amplifier A2.
FP2	7	12	I	POSITION FILTER INPUT - Inverting input to opamp A1.
FP1	8	13	O	POSITION ERROR OUTPUT - Offset-corrected output of the position processing circuitry, which is proportional to the radial displacement of the head from the center of the current track.

The actual transfer function from N, Q to FP1 is:

$$H(z) = \frac{3}{2z-1} \cdot \frac{\sin(\omega T/2)}{\omega T/2} \quad \text{where: } T = 1/FSYNC, \; z = e^{sT}$$

This transfer function exhibits a high frequency roll off with a 3dB point at f = 0.11 FSYNC.

Unused pins on PLCC package: 2,4,6,8,18,20,25,33

* FP4 tied to FP2, Pin 7, internally on 32 pin DIP package.

REGISTER DESCRIPTION

The SSI 32H568 has 8 internal registers which contain status, control and loop parameter information. A three bit register address is latched from inputs AD0-AD2 on the falling edge of ALE. The corresponding register is accessed if $\overline{CS}$ is then asserted, with the direction of access being determined by $\overline{RD}$ or $\overline{WR}$. The registers are summarized in Figure 3.

REGISTER	ADDRESS	ACCESS	D7	D6	D5	D4	D3	D2	D1	D0
GAIN	0	READ/ WRITE	NFG				NVG			
TARGET	1	READ/ WRITE	TARGET VELOCITY							
NEXT	2	READ/ WRITE	NEXT TARGET VELOCITY							
VELCON	3	READ/ WRITE	UNUSED			ND		UPDATE	ENA	VELPOL
WINDOW	4	READ/ WRITE	CAL	UNUSED	DUMP	T/$\overline{S}$	UNUSED	NW		
STATUS	5	AS NOTED	ERSGN (READ ONLY)	ACCIN (READ/WRITE)	CSMOD (READ/WRITE)	FRFMT (READ/WRITE)	ONTRK (READ ONLY)	NO (READ ONLY)	NO (READ ONLY)	TRKCS (READ ONLY)
OFFSET	6	READ/ WRITE	SOS	NOS						
RESET	7	WRITE ONLY	RESET (ANY VALUE)							

FIGURE 3: SSI 32H568 REGISTER MAP

REGISTER DESCRIPTION (Continued)

GAIN **Address 0** **Read/Write**

GAIN SETTINGS - Used to set the velocity gain and fill gain. These settings are only significant in the seek mode.

BIT	NAME	DESCRIPTION
0-3	NVG0-3	VELOCITY GAIN - 4-bit quantity which sets the gain applied to the velocity signal at the output of opamp A3.
4-7	NFG0-3	FILL GAIN - 4-bit quantity which sets the gain applied to the position error which is added to the velocity signal.

If NVG and NFG are represented as integers ranging from 0 to 15, then for a zero velocity target, the error output in seek mode is given by:

$$EOUT - VREF = \frac{NVG}{15}(FV4 - VREF) + \frac{NFG}{255}(FP1 - VREF)$$

TARGET **Address 1** **Read/Write**

CURRENT VELOCITY TARGET - This register selects the 8 bit velocity target which is subtracted from the actual velocity to yield velocity error in seek mode. The sign of the velocity target is determined by the VELPOL bit in register VELCON. If TARGET is represented as an integer from 0 to 255, then the voltage at the output of the velocity target DAC, VT, is given by:

$$VT = VREF\left(1 - \frac{TARGET}{340}\right), VELPOL = 0$$

$$VREF\left(1 + \frac{TARGET}{340}\right), VELPOL = 1$$

The SSI 32H568 has an update feature which allows this register to be loaded automatically with the contents of the next target register when a track crossing occurs. The target register may also be written to directly by the microprocessor to cause an immediate change in target velocity.

NEXT **Address 2** **Read/Write**

NEXT TARGET VELOCITY - This register contains an 8-bit value that will be loaded automatically into the velocity target register when a track crossing occurs, if the UPDATE bit in VELCON is set. This register is unused if UPDATE is cleared.

REGISTER DESCRIPTION (Continued)

VELCON Address 3 Read/Write

BIT	NAME	DESCRIPTION
0	VELPOL	VELOCITY TARGET POLARITY - If this bit is set, the velocity target will be positive (with respect to VREF) and if it is reset, the velocity target will be negative.
1	ENA	ENABLE VELOCITY TARGET DAC - If ENA is set, the velocity target DAC will be enabled and if it is cleared the output of the DAC will be clamped to VREF.
2	UPDATE	UPDATE MODE SELECT - When this bit is set, the contents of the NEXT register will be transferred to TARGET automatically when a track crossing occurs. If it is cleared, new velocity targets must be written directly to the TARGET register by the microprocessor.
3-4	ND0-ND1	DIFFERENTIATOR CHARACTERISTIC SELECT - These bits select the characteristic of the differentiator high pass filter as follows: $H(s) = \frac{-G}{1 + \frac{W}{s}}$, $W = \frac{1}{2T}\left(1 + \frac{ND}{1.75}\right)$ rad/sec $G = 14.3$ Where T is the period of the SYNC clock input in seconds, s is the complex frequency variable in radians/second and ND is an integer from 0 to 3. For s<<W the high pass filter H(s) acts like a differentiator. For a SYNC rate of 500 kHz, the corner frequency W will be: ND1 | ND0 — W/2π (kHz) 00 — 39.8 01 — 62.5 10 — 85.3 11 — 108
		The actual transfer function from N, Q, to FV1 is: $H(z) = \frac{-100(z-1)}{z[7(z-1)+(3.5+2ND)]z} \frac{\sin(\omega T/2)}{\omega T/2}$ where: $T = 1/FSYNC$, $z = e^{sT}$ This transfers function is approximated throughout this data sheet with an s domain approximation that is accurate for f< .05 • FSYNC.
5-7	unused	

REGISTER DESCRIPTION (Continued)

WINDOW Address 4 Read/Write

WINDOW CONTROL - This register is used to program the on-track window comparator and also contains several control bits.		
BIT	**NAME**	**DESCRIPTION**
0-2	NW0-NW2	WINDOW SELECT BITS - This 3 bit word selects the window comparator threshold voltage. The on track indicator bit will be true as long as: $\|FP1 - VREF\| < VREF[(1 + NW)/32]$ where NW is an integer from 0 to 7.
3	unused	
4	T/S	TRACK/SEEK MODE SELECT - When this bit is set, track mode is selected and when it is reset, seek mode is selected.
5	DUMP	POSITION LOOP FILTER DUMP CONTROL - When this bit is set, pins FP3 and FP4 are switched together internally by S1. This causes the external position loop filter feedback capacitor to be discharged.
6	unused	
7	CAL	CALIBRATION MODE - When this bit is reset, the N and Q inputs are connected to the position processor and normal operation occurs. When CAL is set, the processor inputs are connected to VREF, causing the FP1 output to reflect the offset voltage errors in the position sensing path.

STATUS Address 5 Read/Write access as noted

STATUS REGISTER - Contains track status information and several control bits.		
BIT	**NAME**	**DESCRIPTION**
0	TRKCS	TRACK CROSSING INDICATOR - The function of TRKCS is determined by the CSMOD bit in this register. When CSMOD is set, TRKCS will be set every time NQ or $N\overline{Q}$ change state (ie. on every track crossing). When CSMOD is reset, TRKCS will be set every time NQ changes state (ie. on alternate track crossings). TRKCS is reset every time STATUS is read by the microprocessor. The $\overline{INT}$ interrupt output is the inverse of TRKCS. (TRCKS is read only.)
1	$N\overline{Q}$	TRACK QUADRANT - This bit is set when: N-VREF > VREF-Q and reset otherwise. ($N\overline{Q}$ is read only)
2	NQ	TRACK QUADRANT - This bit is set when: N-VREF > Q-VREF and reset otherwise. (NQ is read only)

REGISTER DESCRIPTION (Continued)

BIT	NAME	DESCRIPTION
3	ONTRK	ON TRACK INDICATOR - This bit is set when the voltage on pin FP1 is within the window selected by the WINDOW register. It is reset otherwise (ONTRK is read only).
4	FRFMT	FRAME FORMAT - Used to indicate the relationship between CLOCK and SYNC. If this bit is set, the VCO clock rate must be 32 times the SYNC clock rate. If it is reset, the VCO clock rate must be 72 times the SYNC clock rate. (FRFMT is read/write).
5	CSMOD	CROSSING INDICATOR MODE - If this bit is reset, TRKCS will be set on alternate track crossings. If it is set, TRKCS will be set on every track crossing. (CSMOD is read/write).
6	ACCIN	ACCELERATION INPUT CONTROL - When this bit is set, the FV3 and FV2 inputs are connected internally. This allows motor current feedback to be switched in and out of the velocity loop under microprocessor control. (ACCIN is read/write).
7	ERSGN	ERROR VOLTAGE SIGN - This bit is set when: EOUT-VREF < 0 and reset otherwise. It is used to determine the sign of the offset voltage during calibration. (ERSGN is read only.)

OFFSET **Address 6** **Read/Write**

OFFSET VOLTAGE REGISTER - The 8-bit value in this register drives the offset DAC which adds a correcting voltage to the position error signal.

BIT	NAME	DESCRIPTION
0-6	NOS0-NOS6	OFFSET MAGNITUDE
7	SOS	OFFSET SIGN

The offset correction voltage, VOS, is given by:

$$VOS = -0.89 \left(\frac{NOS}{127}\right) V \text{ , } SOS=0$$

$$0.89 \left(\frac{NOS}{127}\right) V \text{ , } SOS=1$$

RESET **Address 7** **Write only**

RESET REGISTER - When any value is written to this register, all writeable register bits in the SSI 32H568 are reset.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicate where permanent device damage occurs. Continous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VPA		0		14	V
Voltage on any pin		0		VPA+0.1V	V
Storage Temp.		-45		165	°C
Solder Temp.	10 sec duration			260	°C

RECOMMENDED OPERATION CONDITIONS (Unless otherwise noted, the following conditions are valid throughout this document.)

VPA, VPD		10.8		13.2	V
VDD		4.5		5.5	V
VREF		5.1	5.4	5.7	V
Operating temp.		0		70	°C
RBIAS, bias resistor to AGND		22.3	22.6	22.9	KΩ

DC CHARACTERISTICS

IVP	Total VPA and VPD current				40	mA
IDD	VDD current				10	mA
IREF	VREF current				3	mA

DIGITAL I/O

Digital Inputs					
VIH	|IIH|<10uA	2			V
VIL	|IIL|<10uA			0.7	V
Digital Outputs (AD0-AD7, T/$\overline{S}$)					
VOH	|IOH|<40uA	2.4			V
VOL	|IOL|<1.6mA			0.4	V
Open Drain Digital Outputs ($\overline{INT}$, $\overline{OFFTRK}$)					
VOL	|IOL|<1.6mA			0.4	V
Off leakage	VOH = VPD			10	µA

MICROPROCESSOR INTERFACE TIMING (see figure 4(a) and figure 4(b)). (Timing measurements for digital signals are measured at 1.3V, unless otherwise noted.)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
TLHLL	ALE pulse width		45			ns
TAVLL	Address setup time		8			ns
TLLAX	Address hold time		20			ns
TRLVD	$\overline{RD}$ to data valid				145	ns
TRHDX	data hold time after $\overline{RD}$		0		50	ns
TRLRH	$\overline{RD}$ pulse width		200			ns
TLLWL	ALE to $\overline{RD}$ or $\overline{WR}$		25			ns
TRLCL	$\overline{RD}$ or $\overline{WR}$ to $\overline{CS}$ low				20	ns
TRHCH	$\overline{RD}$ or $\overline{WR}$ to $\overline{CS}$ high		10			ns
TWLWH	$\overline{WR}$ pulse width		100			ns
TQVWH	data set up to $\overline{WR}$ high		70			ns
TWHQX	data hold after $\overline{WR}$ high		10			ns

ANALOG I/O

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
N, Q Inputs						
Input resistance			50			KΩ
Input capacitance					25	pF
Offset voltage			-15		15	mV
Common mode range		About VREF	4			V
N, Q Timing (see figure 5)						
Fc	VCO input frequency		4		16	MHz
TSKW	SYNC skew		0		6	ns
TSYNC	SYNC pulse width		40			ns
Nc	VCO/SYNC	FRFMT=1	32		32	
	frequency ratio	FRFMT=0	72		72	
TADS	N or Q analog setup time		260			ns
TADH	N or Q analog hold time		180			ns

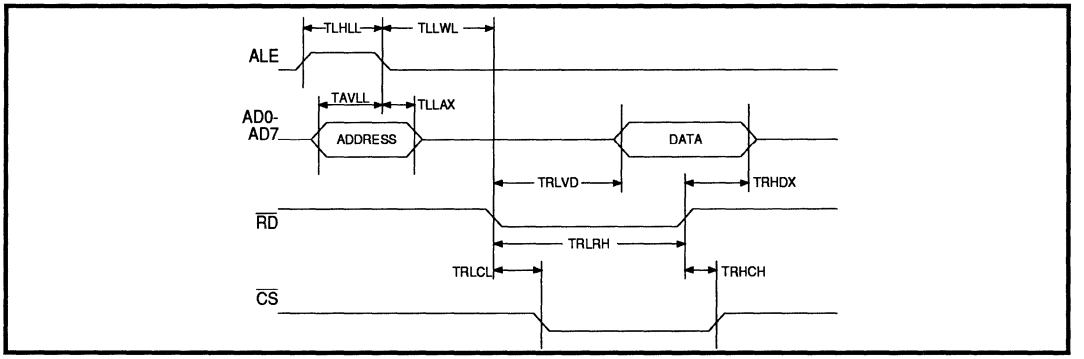


FIGURE 4(a): READ CYCLE TIMING

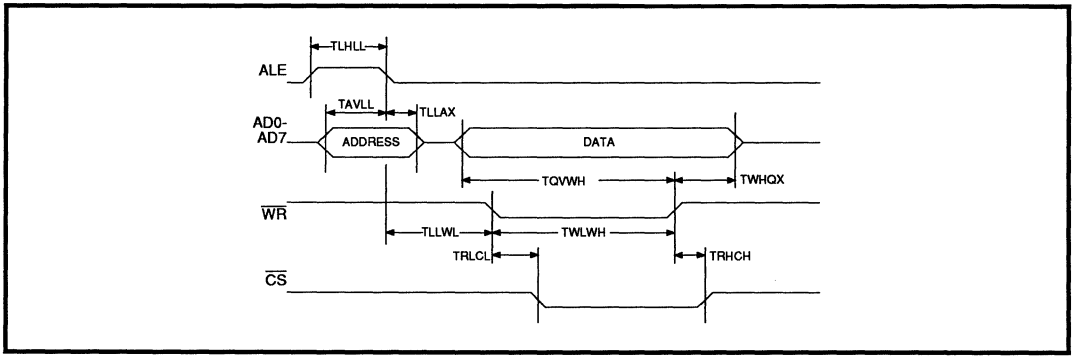


FIGURE 4(b): WRITE CYCLE TIMING

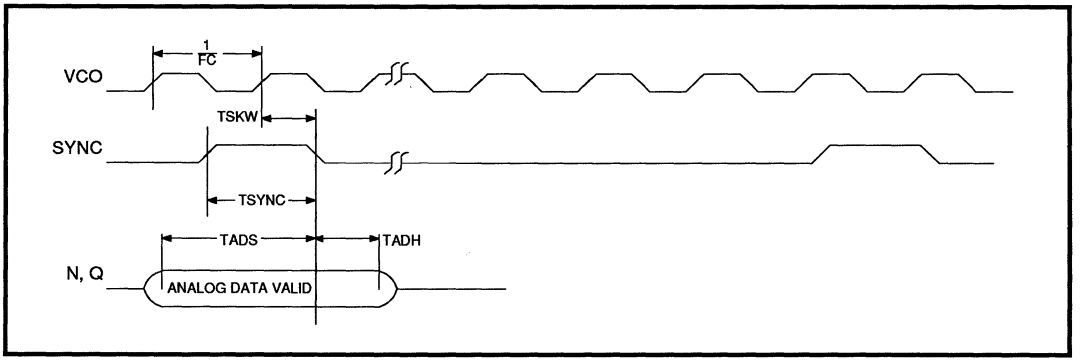


FIGURE 5: ANALOG TIMING

ANALOG I/O (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FP2, FV2, FV3 Inputs					
Input resistance	About VREF	100			KΩ
Input capacitance				20	pF
Offset voltage		-15		15	mV
Switch resistance (S1, S2)				100	Ω
Analog Outputs					
Output impedance	|Vo-VREF|<3V			20	Ω
Resistive loading	About VREF	5			KΩ
Capacitive loading				40	pF
Output swing (FP1, FV1)	About VREF	4			V
Output swing (FP3, FV4)	About VREF	3.5			V
Output swing (EOUT)	About VREF	3.7			V
Gain (FP1 from N or Q)		9.45	9.55	9.65	dB
Gain (Amplifier A1, A3)	Open loop DC gain	66			dB
Gain (Amplifier A2)		-0.1		0.1	dB
Unity gain bandwidth (Amplifier A1, A3)	Open loop	1			MHz
Unity gain bandwidth (Amplifier A2)	Open loop	0.5			MHz

WINDOW COMPARATOR

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Threshold step size accuracy	Nominal=VREF/32	-30		30	%

FILL GAIN

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum gain	NFG=15	58	59	60	mV/V
Gain step size		3	4	5	mV/V

VELOCITY GAIN

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum gain	NVG=15	.98	1	1.02	V/V
Gain step size		48	67	82	mV/V

TARGET VELOCITY DAC

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Full scale/VREF	VELPOL=1	1.72	1.75	1.78	V/V
	VELPOL=0	.22	.25	.28	V/V
Step size/VREF		1.9	2.9	3.7	mV/V
Offset Match	TARGET=0 VELPOL=0, 1			20	mV

OFFSET CORRECTION DAC

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Full scale/VREF	NOS=127, SOS=1	.15	.16	.18	V/V
	NOS=127, SOS=0	-0.15	-0.16	-0.18	V/V
Step size/VREF		.83	1.3	1.76	mV/V

DIFFERENTIATOR

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High pass gain		13.7	14.3	14.9	V/V
Corner frequency	FSYNC = 500 KHz				
	ND=0	37.4		42.2	KHz
	ND=1	57.3		66	KHz
	ND=2	81.2		89.9	KHz
	ND=3	102.7		113.8	KHz

APPLICATIONS INFORMATION

In the example shown in figure 7, the SSI 32H568 is used with its companion devices, the SSI 32H567 and SSI 32H569, as well as a microprocessor and some external components, to implement a complete head positioning system.

Position Reference

The position feedback signal for the servo loop is generated by a servo demodulator from information prerecorded on the disk drive's servo surface. The SSI 32H567 provides quadrature position signals (N and Q), recovered clocks (SYNC and VCO) and an analog reference level (VREF) for the rest of the system. The SSI 32H567 translates the radial displacement of the servo read head to a voltage with a gain of 2 volts/track. The SSI 32H568 has a front end gain of 3, so the gain from actual position error to the voltage at pin FP1 (the input to the position loop filter) is 6 volts/track.

In order to produce the position error signal illustrated in figure 6, the position processor in the SSI 32H568 selects either N, Q or an inverted signal, based on the value of the digital signals NQ and $N\overline{Q}$. The resulting error signal is zero (equal to VREF) when the head is perfectly centered on a track. The error signal has a maximum absolute value in the vicinity of a track boundary (ie. when the head is displaced one half track from a track center) and has a polarity that indicates the direction of the position error.

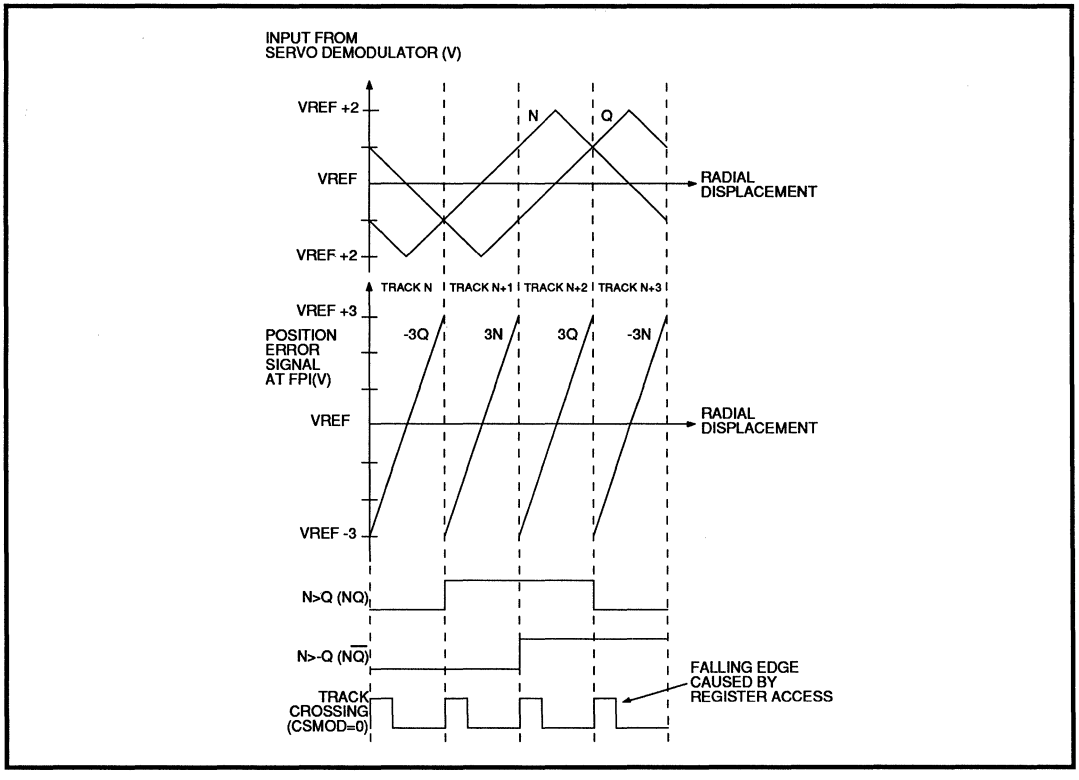


FIGURE 6: POSITION SIGNAL WAVEFORMS

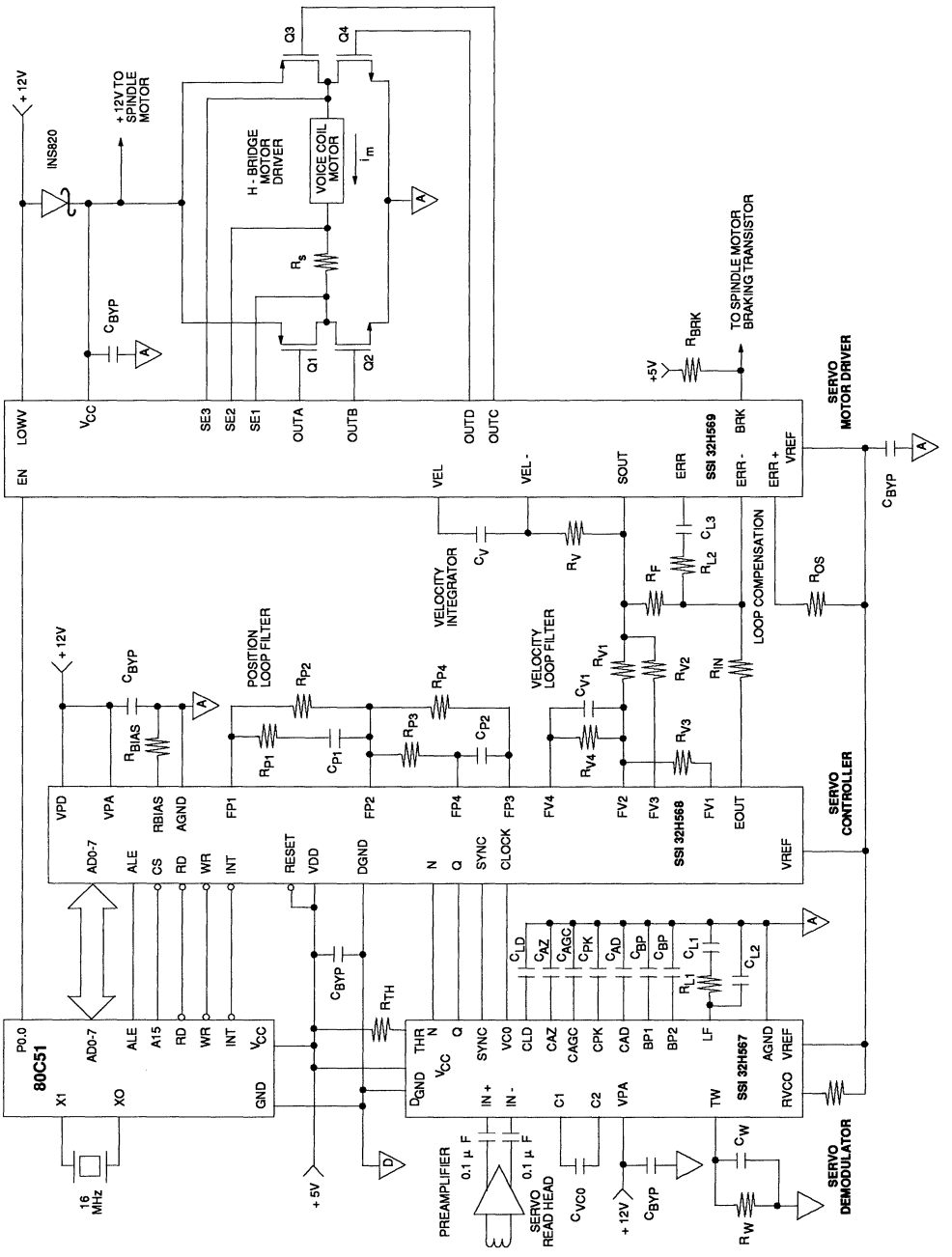


FIGURE 7: COMPLETE EXAMPLE OF SERVO PATH ELECTRONICS USING SSI 32H567/568/569 CHIP SET

4

Servo Motor and Driver

For the purposes of illustration, the following simple model for the servo motor in figure 7 is assumed.

$$i_m = \frac{J\theta}{K_m} \cdot \frac{d\omega}{dt} \qquad e = K_m \cdot \omega$$

Definition of terms:

i_m	Armature current (A)
ω	Motor speed (rad/s)
$J\theta$	Rotor moment of inertia (kg • m²)
Km	Torque constant (V • s)
e	Motor back EMF (V)
Lm	Winding inductance (H)
Rm	Winding resistance (Ohm)

Under the assumption that the electrical and mechanical poles of the motor above are widely separated ($Rm/Lm >> J\theta \cdot Rm/Km^2$), the servo driver loop compensation components, R_{L2} and C_{L3}, may be chosen to cancel the effect of Lm, as follows:

$$C_{L3} = \frac{68 R_S}{2\pi R_F (R_m + R_S) BW}, \quad R_{L2} = \frac{L_m}{C_{L3}(R_m + R_S)}$$

where BW is the desired servo driver open loop bandwidth (Hz). This results in the following relationship between motor current (i_m) and error voltage at the servo controller output (EOUT).

$$\frac{i_m}{EOUT}(s) = \frac{-R_F}{4 R_{in} R_S \left(1 + \frac{s}{2\pi BW}\right)}$$

This simple first order approximation of the servo motor behaviour neglects effects such as resonance due to the motor inductance, Lm, or the pole due to servo driver transconductance. However, it is sufficient to illustrate the design goals for the velocity and position loop filters that are required with the SSI 32H568. A more detailed description of the SSI 32H569 may be found in the SSI 32H569 data sheet.

TRACK MODE

Loop Compensation

Track mode is engaged when the head has reached its destination and the current position must be maintained. The control objective is to drive the position error signal at FP1 to zero and minimize excursions of the head due to noise and other perturbations of the system. The transfer function of the complete servo loop in track mode is shown in figure 8(a), using the servo motor model derived above. The gain G_1 is the combined effect of the SSI 32H567 and the front end gain of the SSI 32H568, and has a nominal value of 6 volts/track. The gain G_2 is a property of the head transport system, and has units of tracks/radian for rotary servo motors and tracks/meter for linear motors. (The nomenclature chosen for the motor model is that of rotary motors but the results are applicable to linear motors as well, if appropriate units are substituted). To ensure that the control loop has negative feedback, positive motor current (as indicated in figure 7) must result in negative motor acceleration. This inversion is accomplished in the prerecorded servo pattern and is accounted for in the transfer function by showing G2 to be negative.

Since the servo driver/motor combination has a double pole at the origin and an additional real pole at frequency BW (which is selectable with external components in the SSI 32H569), the position loop filter is essential to ensure a stable system. The effect of the position filter used in this example is to provide lag-lead compensation. Systems of this type are usually designed by trial and error, but a further simplification of the transfer function may be made to obtain an initial solution. If the pole at BW is ignored, RP4 is removed and RP2 made large (RP2 is necessary to provide a DC path for leakage current at pin FP2) then the system illustrated in figure 8(b) is obtained. The compensation has been reduced to lead compensation only. If the following quantities are defined:

$$Gtot = \left(\frac{G_1 G_2 C_{P1}}{C_{P2}}\right)\left(\frac{R_F}{4 R_m R_S}\right)\left(\frac{K_m}{J\theta}\right)\left(s^2\right)$$

PM = Desired closed loop phase margin (degrees)

FB = Desired open loop unity gain bandwidth (rad/s)

then appropriate values for the time constants of the lead compensation circuit (T_1, T_2) may be chosen using the following relationships, assuming $1/T_2 << FB << 1/T_1$:

$$FB = Gtot \cdot T_2 \text{ (rad/s)}$$

$$PM = 90 - \arctan(FB \cdot T_1) \text{ (degrees)}$$

The values for T_1 and T_2 thus chosen form a starting point for the selection of appropriate values for the more complex lag-lead compensator required by the real system.

Position Loop Filter Initialization

Switch S1, which is controlled by the DUMP bit in the WINDOW register, may be used to short out the external feedback capacitor C_{P2}, discharging it. S1 is usually closed during seek a operation, so that when the system is switched to track mode no sudden transients occur due to charge stored on C_{P2}. Disturbances to the position signal when the system is switching to track mode can greatly extend the disk drive's access time, since the system response is much slower in this mode.

Offset Cancellation

The position error path in the servo loop is DC coupled and can be affected by offset voltages internal to the SSI 32H568, especially during a transition from seek to track mode. The following procedure may be used to cancel out any offsets in the position error path:

1) Set T/$\overline{S}$. (Enter track mode).
2) Set both the CAL and DUMP bits. (This switches the N and Q inputs to VREF and shorts out C_{P2}).
3) Set NOS=0. (This sets the offset DAC magnitude to zero).
4) Copy the ERSGN bit to SOS. (If the offset causes EOUT to be negative, then it is necessary to make the input of inverting amplifier A1 more negative, and vice versa).

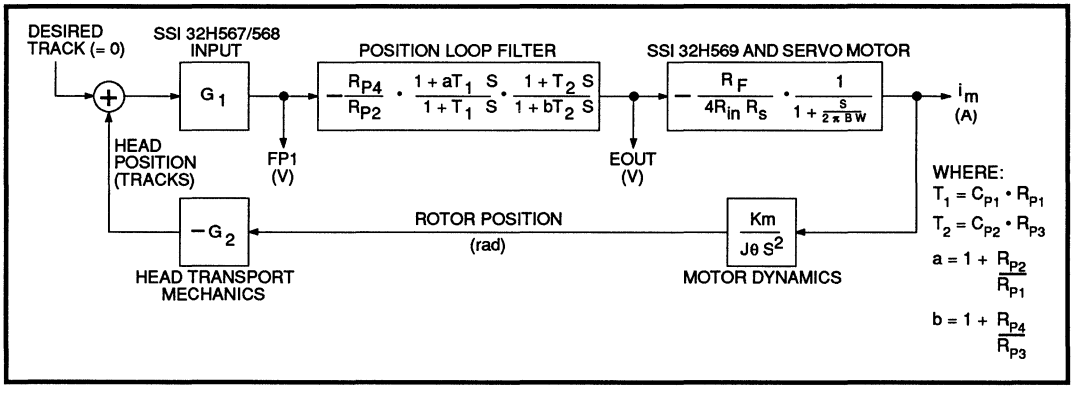


FIGURE 8(a): SYSTEM TRANSFER FUNCTION IN TRACK MODE

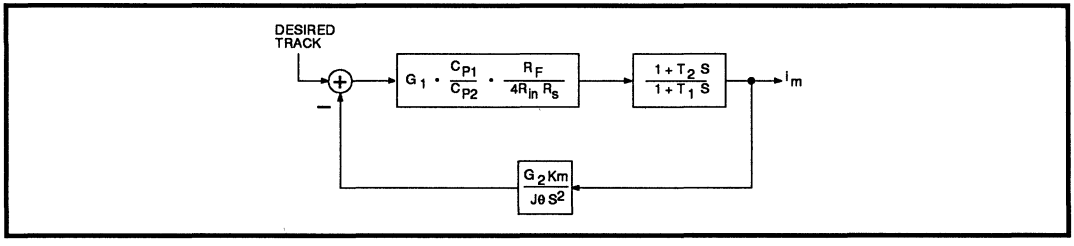


FIGURE 8(b): SIMPLIFIED TRACK MODE TRANSFER FUNCTION

5) Increase NOS in steps of one LSB until ERSGN changes sign. At this point the position error offset will have been cancelled to the greatest extent possible.
6) Clear both DUMP and CAL to resume normal track mode operation.

On Track Window

The on track window comparator may be used to monitor the positioning accuracy of the head. The position error voltage at pin FP1 is compared to a signal selected by the bits NW0-2 in the WINDOW register. The ONTRK bit in register STATUS is set if the position error is within the specified limits and cleared if it is outside the limits (in either the positive or the negative direction). The programmable excursion limits (expressed as a percentage of a track) range from 2.8% to 22.5% in 8 equal steps. By monitoring the ONTRK bit, the microprocessor can determine when the head has settled sufficiently for read and write operations to commence. The ONTRK bit may also be used to decide when it is appropriate to switch from seek to track mode at the end of a period of decceleration.

SEEK MODE

Velocity Profile

The velocity profile that results in the shortest seek time, subject to motor current and head velocity limitations, is as follows:

1) Maximum acceleration (maximum motor current) until the half-way point or maximum velocity is reached.
2) Constant velocity motion until it is time to commence decceleration (if maximum velocity was reached).
3) Maximum decceleration until head comes to rest over the destination track. The decceleration period is of approximately the same duration as the acceleration period.

The microprocessor computes a velocity profile according to the rules above, based on the current head location and destination track. During the final approach to the destination track, updates to the velocity DAC become more infrequent since the track crossing rate is approaching zero. The fill signal which is derived from the position error can be used to provide a smooth target velocity profile between track crossing updates.

Figure 9 shows a set of typical waveforms as the head approaches the destination track. The fill gain is adjusted at each track crossing so that the fill signal interpolates smoothly between target DAC settings. In the destination track, where the target DAC output is zero, the fill signal is especially important, since it becomes zero only when the head is centered on the track. The velocity control loop thus causes the head to come to rest at the center of the destination track.

Loop Compensation

The transfer function for the controller electronics of figure 7 is shown in figure 10(a). This transfer function may be simplified as shown in figure 10(b), under the following conditions:

$$\omega^2 >> \frac{(GG_1G_2)(K_m R_X)}{J\theta R_{V3}}$$

$$R_{V4} C_{V1} = \frac{J\theta \omega R_{V3}}{(GG_1G_2)(K_m R_X)}$$

where Rx is RV1 (ACCIN=0) or RV1//RV2 (ACCIN=1)

The value of ω, the corner frequency of the internal position differentiator, is dependent on the sync rate, but the above condition is generally satisfied by most systems. The condition on RV4 and CV1 sets the position of the zero due to the external components in the velocity loop filter, whose function is described below. The resulting system has two real poles, one of which is at the origin, and is thus unconditionally stable.

The position of the SSI 32H568 internal differentiator pole is selectable under microprocessor control. It is desireable to select as low a frequency as is consistent with the required seek performance. This pole prevents the differentiator from amplifiying high frequency noise. In order to provide feedback of a velocity signal for frequencies above the differentiator pole, the external velocity loop filter is configured to act as an integrator which integrates the motor current sense output of the SSI 32H569, SOUT. Since SOUT is proportional to motor acceleration, this integration produces a signal proportional to velocity. Thus, at low frequencies the velocity feedback is generated by differentiating the position error signal and at high frequencies, the velocity term results from integrating motor current. It is more accurate to estimate velocity from a direct observation of head position, but at higher frequencies it is necessary to provide increased noise immunity. The system described above balances these two considerations.

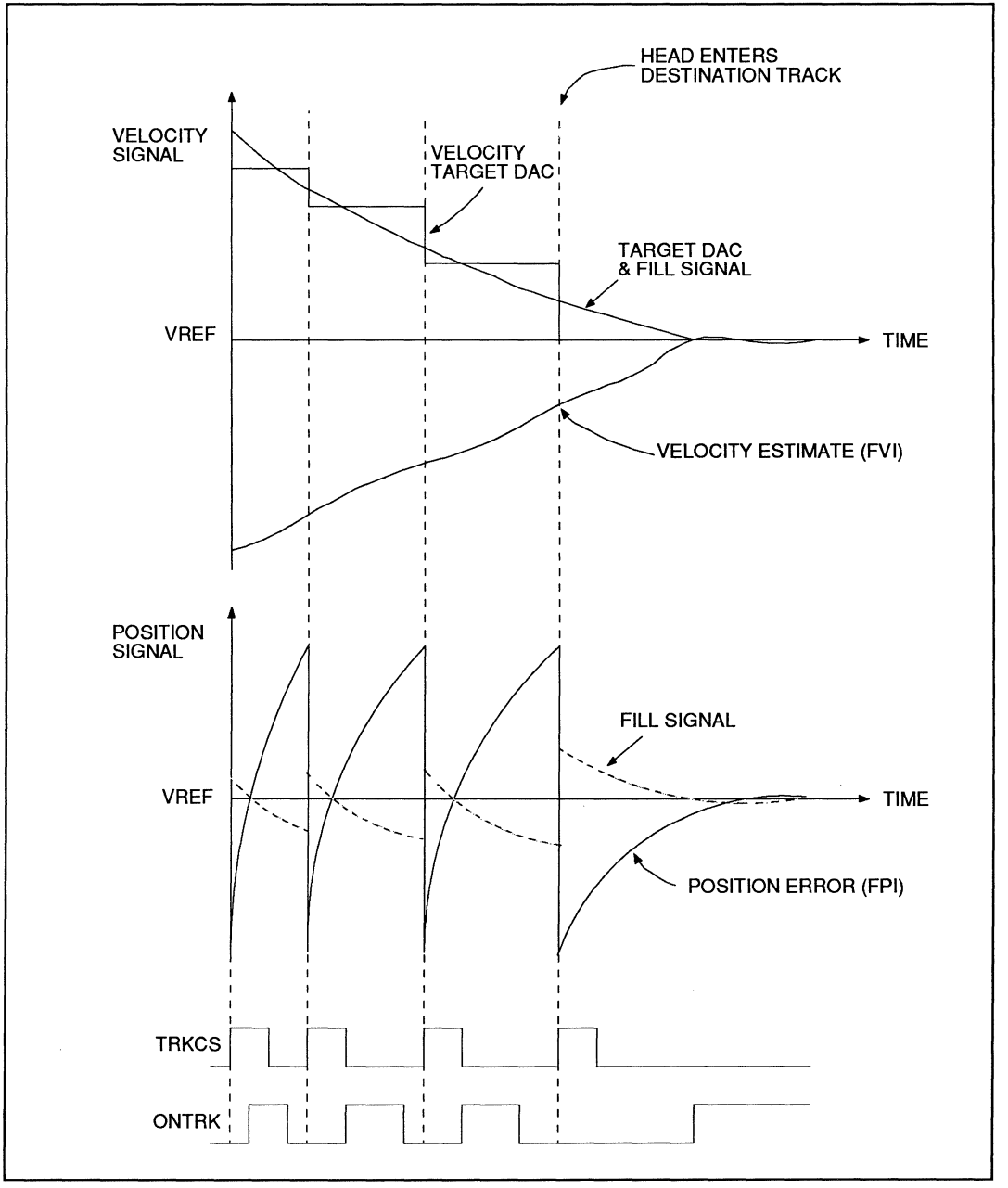


FIGURE 9: TYPICAL WAVEFORMS DURING FINAL DECELERATION MODE

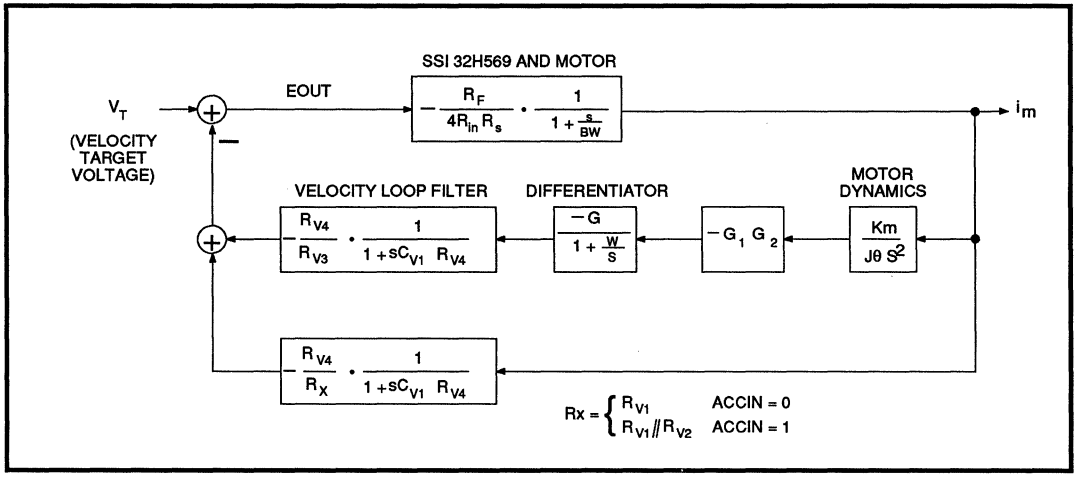


FIGURE 10(a): TRANSFER FUNCTION OF SSI 32H568 IN SEEK MODE

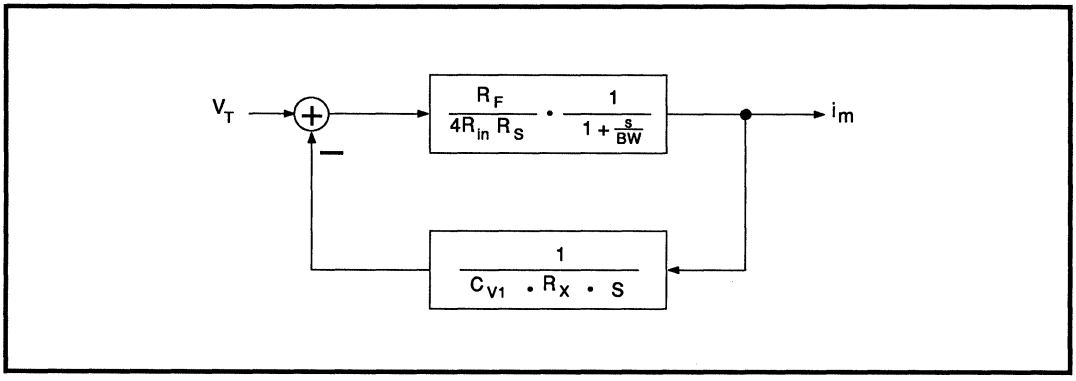


FIGURE 10(b): SIMPLIFIED TRANSFER FUNCTION OF SSI 32H568 IN SEEK MODE

$$\omega^2 >> \frac{(GG_1G_2)(K_m R_X)}{J\theta R_{V3}}$$

$$R_{V4}C_{V1} = \frac{J\theta\,\omega R_{V3}}{(GG_1G_2)(K_m R_X)}$$

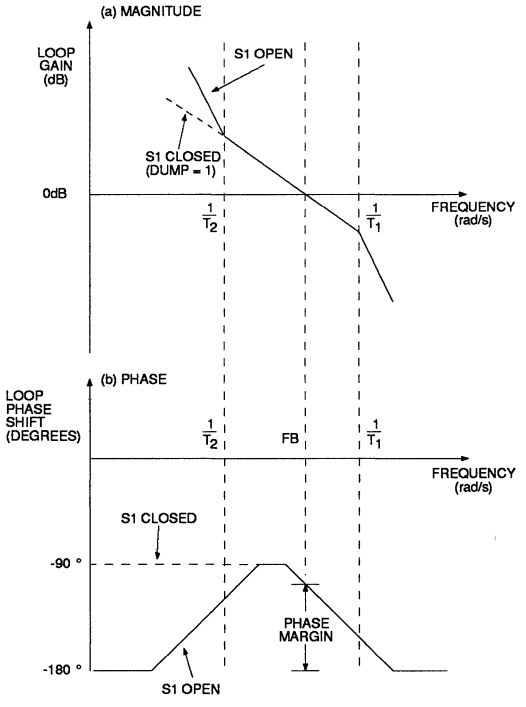


FIGURE 11: BODE PLOT OF SIMPLIFIED TRACK MODE TRANSFER FUNCTION

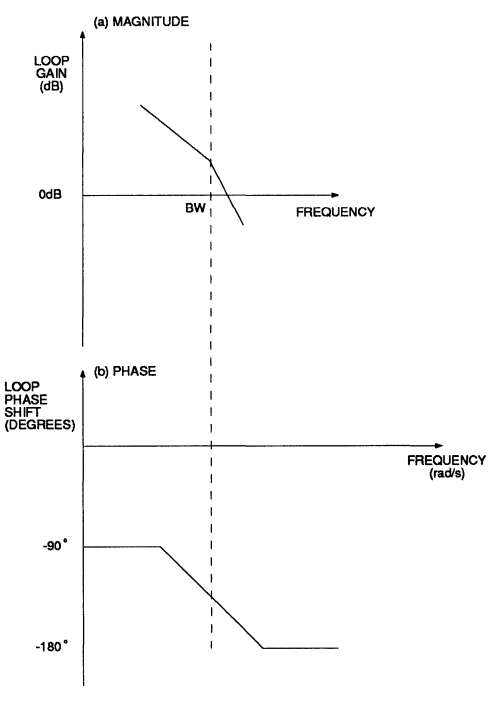
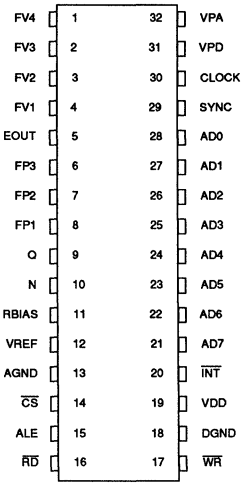


FIGURE 12: BODE PLOT OF SIMPLIFIED SEEK MODE TRANSFER FUNCTION

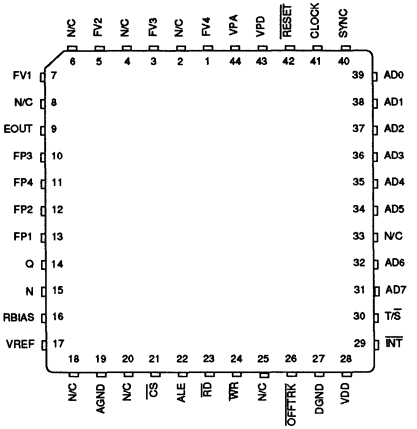
SSI 32H568
Servo Controller

PACKAGE PIN DESIGNATIONS
(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.



32-Pin DIP



44-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32H568, Servo Controller		
32-Pin DIP	SSI 32H568-CP	32H568-CP
44-Pin PLCC	SSI 32H568-CH	32H568-CH

silicon systems™
Silicon Systems, Inc., 14351 Myford Road, Tustin CA 92680, (714) 731-7110, TWX 910-595-2809

SSI 32H569
Servo Motor Driver

August, 1988

DESCRIPTION

The SSI 32H569 Servo Motor Driver is a bipolar device intended for use in Winchester disk drive head positioning systems employing linear or rotary voice coil motors. When used in conjunction with a position controller, such as the SSI 32H568 Servo Controller, and a position reference, such as the SSI 32H567 Servo Demodulator, the device allows the construction of a high performance, dedicated surface head positioning system.

The SSI 32H569 serves as a transconductance amplifier by driving 4 MOSFETs in an H-bridge configuration, performs motor current sensing and limits motor current and velocity. In its linear tracking mode, class B operation is guaranteed by crossover protection circuitry, which ensures that only one MOSFET in each leg of the H-bridge is active. The MOSFET drivers are disabled when motor velocity or current exceed externally programmable limits. In addition, automatic head retraction and spindle braking may be initiated by a low voltage condition or upon external command.

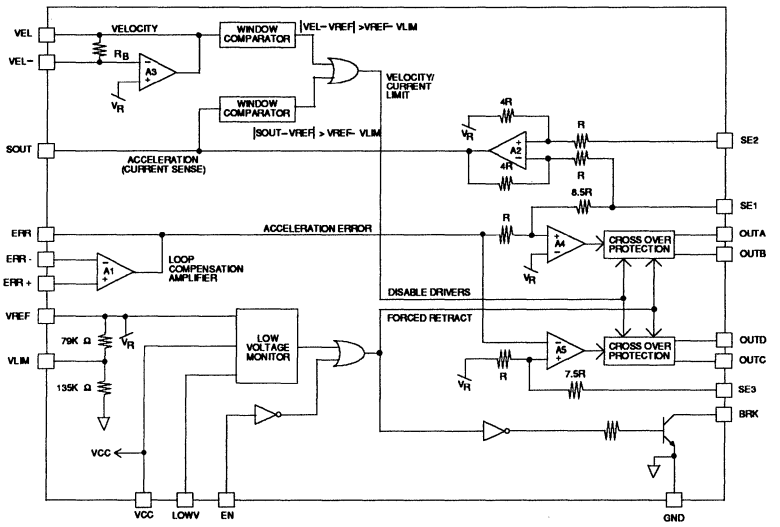
(Continued)

FEATURES

- **Predriver for linear and rotary voice coil motors**
- **Interfaces directly to MOSFET H-Bridge motor driver**
- **Class B linear mode and constant velocity retract mode**
- **Precision differential amplifier for motor current sensing**
- **Motor current and velocity limiting circuitry**
- **Automatic head retract and spindle braking signal on power failure**
- **External digital enable**
- **Servo loop parameters programmed with external components**
- **Advanced bipolar IC requires under 240 mW from 12V supply**
- **Available in 20-pin DIP or SO packaging**

4

BLOCK DIAGRAM



DESCRIPTION (Continued)

The SSI 32H569 is implemented in an advanced bipolar process and dissipates less than 240 mW from a 12V supply. The IC is available in 20-pin DIP and 20-pin SO packaging.

FUNCTIONAL DESCRIPTION

(Refer to block diagram and typical application Fig.2)

The SSI 32H569 has two modes of operation, linear and retract. The retract mode is activated by a power supply failure or when the control signal EN is false. Otherwise the device operates in linear mode.

During linear operation, an acceleration signal from the servo controller is applied through amplifier A1, whose three connections are all available externally. RC components may be used to provide loop compensation at this stage. The ERR signal drives two precision amplifiers, each with a gain of 8.5. The first of these amplifiers is inverting, and is formed from opamp A4, an on-chip resistor divider and an off-chip complementary MOSFET pair. The second is non-inverting, and is formed in a similar manner from opamp A5. Feedback from the MOSFET drains, on sense inputs SE1 and SE3, allows the amplifiers gains to be established precisely. The voice coil motor and a series current sense resistor are connected between SE1 and SE3.

Crossover protection circuitry between the outputs of A4 and A5, and the external MOSFETs, ensures class B operation by allowing only one MOSFET in each leg of the H-bridge to be in conduction. The crossover separation threshold, illustrated in Figure 5, is the maximum drive on any MOSFET gate when the motor voltage changes sign. The crossover circuitry can also disable all MOSFETS simultaneously (to limit motor current or velocity) or apply a constant voltage across the motor (to retract the heads at a constant velocity).

Motor current is sensed by a small resistor placed in series with the motor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 4 (A2 and associated resistors), whose inputs are SE1 and SE2. The resulting voltage, SOUT, is proportional to motor current, and hence acceleration. This signal is externally fed back to A1, so that the signal ERR represents the difference between the desired acceleration (from the servo controller) and the actual motor acceleration. If SOUT is integrated, using opamp A3 and an external RC network, the resulting signal, VEL, is proportional to the motor velocity.

Both SOUT and VEL are connected to window comparators, which are used to detect excessive motor current or velocity. The comparator outputs disable the MOSFET drivers until the motor comes within limits again. The VLIM pin may be used to program the voltage limits for the window comparators. The maximum voltage excursion allowed about VREF is (VREF-VLIM). An on-chip resistor divider sets a default value for VLIM and if VLIM is connected to ground, the windowing is effectively disabled.

The SSI 32H569 has low voltage monitor circuitry that will detect a loss of voltage on the VREF, VCC or LOWV pins. The power supply pin, VCC, should be connected to the disk drive's spindle motor so that its stored rotational energy may be used to hold up VCC briefly during a power failure. LOWV is used to detect a system power supply failure. When a low voltage condition is detected, the MOSFET drivers switch from linear operation to retract mode. In this mode a constant voltage is applied across the motor which will cause the heads to move at a constant speed. A mechanical stop must be provided for the heads when they reach a safe location. The current limiting circuitry will disable the MOSFET drivers when motor current increases due to loss of the velocity-induced back EMF. An open collector output, BRK, which is active while the device is in retract mode, is provided for spindle motor braking. An external RC delay may be used to defer braking until the heads are retracted. For proper operation of the SSI 32H569, a pullup resistor on BRK is required even if the BRK output is not used.

An example of an entire servo path implemented with the SSI 32H569 and its companion devices, the SSI 32H567 and 32H568, is shown in Figure10.

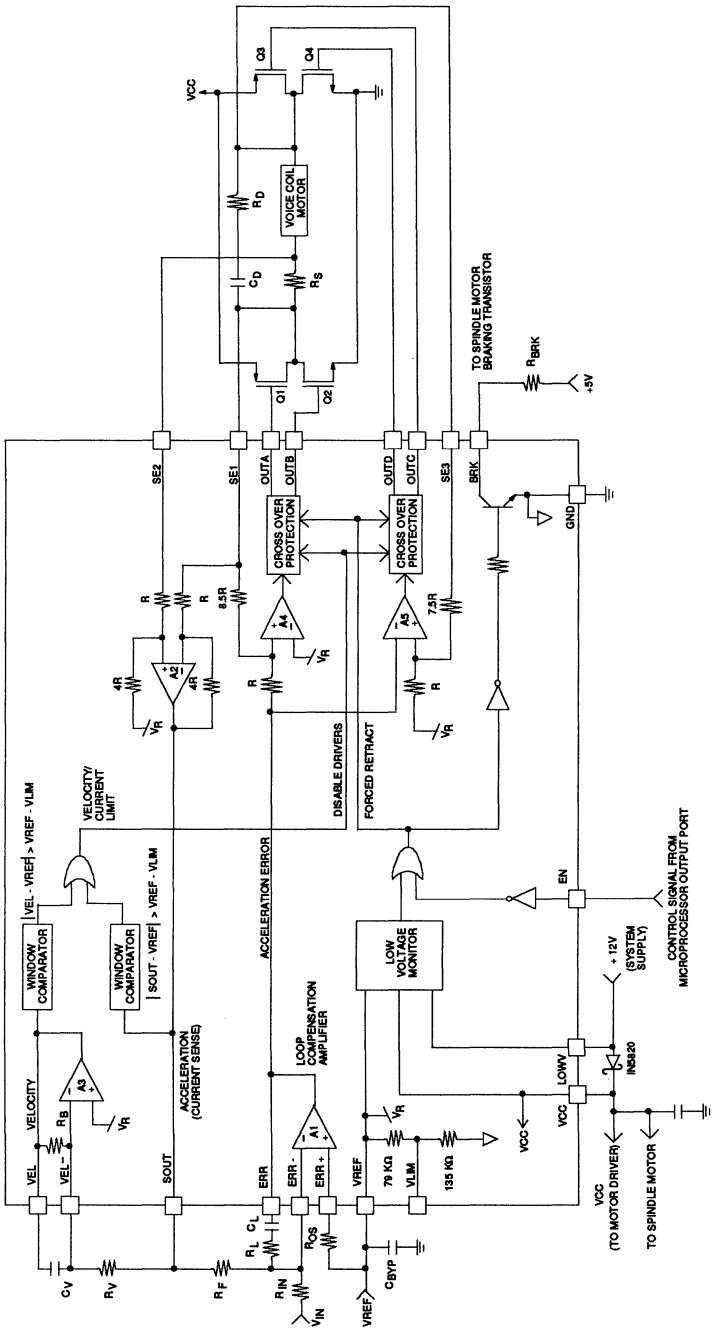


FIGURE 2: TYPICAL APPLICATION

4

PIN DESCRIPTION

POWER

NAME	PIN	TYPE	DESCRIPTION
VCC	20		POSITIVE SUPPLY - 12V power supply. Usually taken from spindle motor supply. Spindle motor stored energy permits head retraction during power failure. If VCC falls below 9V, a forced head retraction occurs.
LOWV	19	I	LOW VOLTAGE - System 12V supply. If this input falls below 9V, a forced head retraction occurs.
VREF	4	I	REFERENCE VOLTAGE - 5.4V input. All analog signals are referenced to this voltage. If VREF falls below 4.3V, a forced head retraction occurs.
GND	10		GROUND

CONTROL

NAME	PIN	TYPE	DESCRIPTION
ERR	1	O	POSITION ERROR- Loop compensation amplifier output. This signal is amplified by the MOSFET drivers and applied to the motor by an external MOSFET H-bridge, as follows: SE3-SE1 = 17(ERR-VREF)
ERR-	2	I	POSITION ERROR INVERTING INPUT - Inverting input to the loop compensation amplifier.
ERR+	3	I	POSITION ERROR NON-INVERTING INPUT - Non-inverting input to the loop compensation amplifier.
SOUT	5	O	MOTOR CURRENT SENSE OUTPUT - This output provides a voltage proportional to the voltage drop across the external current sense resistor, as follows: SOUT-VREF=4(SE2-SE1)
VEL-	6	I	VELOCITY INVERTING INPUT - Inverting input to the velocity integrating amplifier. The non-inverting input is connected internally to VREF.
VEL	7	O	VELOCITY OUTPUT - Output of the velocity integration amplifier. This signal is internally applied to a window comparator whose output limits motor drive current when the voltage at VEL exceeds a set limit.
BRK	8	O	BRAKE OUTPUT - Active high, open collector output which may be used to enable an external spindle motor braking transistor upon power failure or deassertion of EN.
VLIM	11	I	LIMITING VOLTAGE - The voltage at this pin sets motor current and velocity limits. Limiting occurs when: |SOUT-VREF|>VREF-VLIM or |VEL-VREF|>VREF-VLIM. An internal resistor divider establishes a default value that may be externally adjusted.

CONTROL (Continued)

NAME	PIN	TYPE	DESCRIPTION
SE2	14	I	MOTOR CURRENT SENSE INPUT - Non-inverting input to the current sense differential amplifier. It should be connected to one side of an external current sensing resistor in series with the motor. The inverting input of the differential amplifier is connected internally to SE1.
EN	18	I	ENABLE - Active high TTL compatible input enables linear tracking mode. A low level will initiate a forced head retract.

FET DRIVE

NAME	PIN	TYPE	DESCRIPTION
SE3	9	I	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the non-inverting MOSFET driver amplifier. It is connected to one side of the motor. The gain to this point is: SE3-VREF = 8.5(ERR-VREF)
OUTC	12	O	P-FET DRIVE (NON-INVERTING) - Drive signal for a P channel MOSFET connected between one side of the motor and VCC. This MOSFET drain is connected to SE3.
OUTD	13	O	N-FET DRIVE (NON-INVERTING) - Drive signal for an N channel MOSFET connected between one side of the motor and GND. This MOSFET drain is connected to SE3. Crossover protection circuitry ensures that the P and N channel devices driven by OUTC and OUTD are never enabled simultaneously.
SE1	15	I	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the inverting MOSFET driver amplifier. It is connected to the current sensing resistor which is in series with the motor. The gain to this point is: SE1-VREF = -8.5(ERR-VREF) This input is internally connected to the current sense differential amplifier inverting input.
OUTB	16	O	N-FET DRIVE (INVERTING) - Drive signal for an N channel MOSFET connected between the current sense resistor and GND. This MOSFET drain is also connected to SE1.
OUTA	17	O	P-FET DRIVE (INVERTING) - Drive signal for a P channel MOSFET connected between the current sense resistor and VCC. This MOSFET drain is also connected to SE1. Crossover protection circuitry ensures that the P and N channel devices driven by OUTC and OUTD are never enabled simultaneously.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicates where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC		0		16	V
VREF		0		10	V
All other pins		0		14	V
Storage temperature		-45		165	°C
Solder temperature	10 sec duration			260	°C

RECOMMENDED OPERATION CONDITIONS (Unless otherwise noted, the following conditions are valid throughout this document.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC	Normal Mode	9	12	13.2	V
	Retract Mode	3.5V		14	V
VREF		5		7	V
Operating temperature		0		70	°C

DC CHARACTERISTICS

ICC, VCC current				20	mA
IREF, VREF current				2	mA

A1, LOOP COMPENSATION AMPLIFIER

Input bias current				500	nA
Input offset voltage				3	mV
Voltage swing	About VREF	2			V
Common mode range	About VREF	±1			V
Load resistance	To VREF	4			KΩ
Load capacitance				100	pF
Gain		80			dB
Unity gain bandwidth		1			MHz
CMRR	f<20 kHz	60			dB
PSRR	f<20 kHz	60			dB

A2, CURRENT SENSE AMPLIFIER

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input impedance	SE1 to SE2	3.5	5		KΩ
Input offset voltage				2	mV
Output voltage swing		VREF-4		VCC-1.2	V
Common mode range		0		VCC-0.2	V
Load Resistance	To VREF	4			KΩ
Load Capacitance				100	pF
Output impedance	f<40 KHz			20	Ω
Gain (SOUT-VREF)/(SE1-SE2)		3.9	4	4.1	V/V
Unity gain bandwidth		1			MHz
CMRR	f<20 KHz	52			dB
PSRR	f<20 KHz	60			dB

A3, VELOCITY INTEGRATING AMPLIFIER

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input bias current				250	nA
Input offset voltage				2	mV
Voltage swing		VREF-4		VCC-1.2	V
Common mode range		4.5		6	V
Load resistance	To VREF	10			KΩ
Load capacitance				100	pF
RB, internal feedback resistor		80		150	KΩ

WINDOW COMPARATORS AND LIMITING

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Window comparator threshold (SOUT-VREF or VEL-VREF)		VREF-VLIM			V
Threshold hysteresis		35	50	65	%
VLIM voltage	No external parts	VREF-1.8		VREF-2.2	V
VLIM input resistance		50			KΩ

POWER SUPPLY MONITOR

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC fail threshold		8.5	9	9.8	V
LOWV fail threshold	|ILowv| < 0.5 mA	8.5	9	9.8	V
VREF fail threshold		3.9	4.3	4.8	V
Hysteresis (LOWV, VCC)			250		mV
Hysteresis (VREF)			110		mV
EN input low voltage	|IIL| < 0.5 mA	0.8			V
EN input high voltage	|IIH| < 40 uA			2	V
BRK voltage	normal mode, |IOL| < 1 mA			0.4	V
BRK leakage current	retract mode			10	µA
BRK delay (from power fail or EN false to BRK floating)				1	ms

MOSFET DRIVERS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SE3 Input impedance	To VREF	10	25		KΩ
OUTA, OUTC voltage swing |Io|<1 mA		0.7		VCC-1	V
OUTB, OUTD voltage swing |Io|<1 mA		1		VCC-1	V
VTH, Crossover separation threshold				2	V
Slew rate (OUTA, OUTB, OUTC, OUTD)	Cl<1000 pF	1.4			V/µs
Crossover time	300 mV step at ERR			5	µs
Output impedance (OUTA,B,C,D)			50		KΩ
Transconductance I(OUTA,B,C,D)/(ERR-VREF)			8		mA/V
Gain (-(SE1-VREF)/(ERR-VREF) or (SE3-VREF)/(ERR-VREF))		8	8.5	9	V/V
Offset current	R_S = 0.2Ω, R_F = R_{IN}, V_{IN}=VREF			20	mA
Retract motor voltage (SE1-SE3)		0.7	1	1.3	V

APPLICATIONS INFORMATION

A typical SSI 32H569 application is shown in Figure 2. The selection criteria for the external components shown are discussed below. Figure 3 shows the equivalent circuit and equations for the DC motor used in the following derivations. While the nomenclature chosen is for a rotating motor, the results are equally applicable to linear motors.

MOTOR CURRENT SENSE AND LIMITING

The series resistor which senses motor current, Rs, is chosen to be small compared to the resistance of the motor, Rm. A value of Rs = 0.2Ω is typical in disk drive applications. The window comparator threshold, programmed by VLIM, must be chosen to cause limiting when the motor current reaches its maximum permissible value. If iMAX is the maximum motor current in Amps, then this value may be chosen as follows:

$$VLIM = VREF - 4 \cdot R_s \cdot iMAX \ (V)$$

VLIM may be set with a resistor divider whose thevenin resistance is substantially less than the output resistance of the VLIM pin (50 KΩ). The window comparators have hysteresis (typically 50% of their threshold, VREF-VLIM) to prevent multiple triggerings of the driver disable signal.

VELOCITY LIMITING

The values of Rv and Cv in the velocity integrator are chosen to produce a voltage excursion of VREF-VLIM, when the motor speed is at its maximum permissible value. Rv must be large enough to prevent overloading of opamp A2. The following equation ignores the effect of RB, the internal resistor between VEL and VEL- which prevents saturation of A3 due to offsets. For the motor in Figure 3, with maximum velocity ωMAX (rad/s) these components may be chosen as follows:

$R_V // R_F > 4\ K\Omega$ (A2 output loading restriction)

$$C_V = \frac{4 R_s \cdot J\theta \cdot \omega MAX}{(VREF - VLIM) \cdot R_V \cdot K_m} \ (F)$$

LOOP COMPENSATION

The transfer function of the SSI 32H569 in the application of Figure 2 is shown in figure 4(a). If the zero due to RL and CL in the loop compensation circuit is chosen to cancel the pole due to the motor inductance, Lm, then the transfer function can be simplified as shown in figure 4(b), under the assumption that this pole and the pole due to the motor mechanical response are widely separated. CL may then be chosen to set the desired open loop unity gain bandwidth.

$$C_L = \frac{68 \cdot R_s}{2 \cdot \pi \cdot R_F \cdot (R_m + R_s) \cdot BW}$$

where BW is the unity gain open loop bandwidth

$$R_L = \frac{L_m}{C_L \cdot (R_m + R_s)}$$

The closed loop response of the servo driver and motor combination, using the component values and simplifying assumptions given above, is given by:

$$\frac{i_m}{V_{in}}(s) = -\frac{1}{R_{in}} \cdot \frac{R_F}{4 \cdot R_s} \cdot \frac{1}{(1 + \frac{s}{2 \cdot \pi \cdot BW})}$$

(This analysis neglects the pole due to the output impedance of the MOSFET drivers and the MOSFET gate capacitance, an effect that may be significant in some systems).

RF is chosen to be sufficiently large to avoid overloading A2 ($R_F // R_V > 4K\Omega$). The input resistor, RIN, sets the conversion factor from servo controller output voltage to servo motor current. RIN is chosen such that the servo controller internal voltages are scaled conveniently. The resistor Ros is optional and cancels out the effect of the input bias current of A1.

$$R_{os} = R_{in} // R_F$$

The external components RD and CD have no effect on the motor dynamics, but may be used to improve the stability of the MOSFET drivers. The load represented by the motor, ZM, is given by:

$$ZM = (R_s + R_m)(1 + s\frac{L_m}{R_s + R_m})(1 + \frac{K_m^2}{s \cdot J\theta \cdot (R_s + R_m)}) \ (\Omega)$$

At frequencies above $(Rs+Rm)/(2 \cdot \pi \cdot Lm)$ Hz, this load becomes entirely inductive, which is undesireable. RD and CD may be used to add some parallel resistive loading at these frequencies.

H-BRIDGE MOSFETS

The MOSFETs chosen for the H-bridge should have gate capacitances in the range of 500-1000 pF. The MOSFET input capacitance forms part of the compensation for the MOSFET drivers, so values below 500 pF may cause some driver instability. Excessive input capacitance will degrade the slew mode performance of the drivers.

When the motor voltage is changing polarity, the crossover protection circuits at outputs OUTA-OUTD ensure that the maximum MOSFET gate drive is less than 2V (the crossover separation threshold), as illustrated in Figure 5. The thresholds of the MOSFET devices chosen should be as large as possible to minimize conduction in this region. If the device thresholds are significantly less than the crossover separation threshold, the N and P channel devices in each leg of the H-bridge will conduct simultaneously, causing unnecessary power dissipation.

POWER FAILURE OPERATION

The power supply for the SSI 32H569, VCC, should be taken from the system 12V supply through a schottky diode (maximum 0.5V drop at If = 3A) and connected to the disk drive spindle motor. If the system power fails, the IC will continue to operate as the spindle motor becomes a generator. The SSI 32H569 will detect the power failure and cause a forced head retract, continuing to operate with VCC as low as 3.5V. The power fail mode will commence if either VCC or LOWV falls below 9V, or VREF falls below 4.3V, or EN is false. Hysteresis on the low voltage thresholds prevents the device from oscillating between operating modes when the power supply is marginal.

The BRK output, which is pulled low during normal operation, floats during a power failure. This allows an external transistor to be enabled for spindle motor braking. An external RC delay may be added to defer braking until head retraction is complete, since the spindle motor is required to generate the supply voltage during retraction.

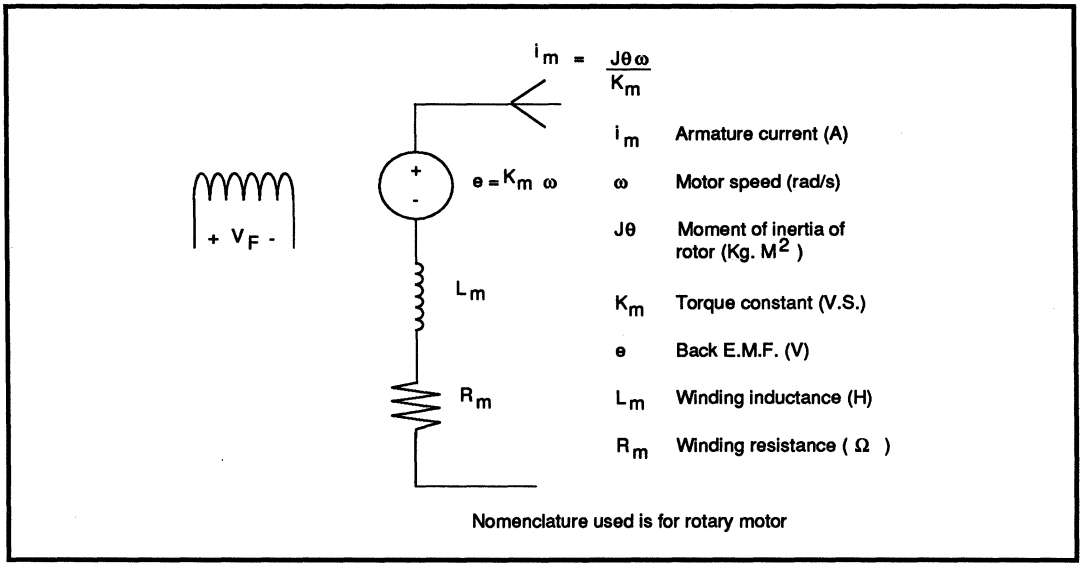


FIGURE 3: EQUIVELANT CIRCUIT FOR FIXED FIELD DC MOTOR

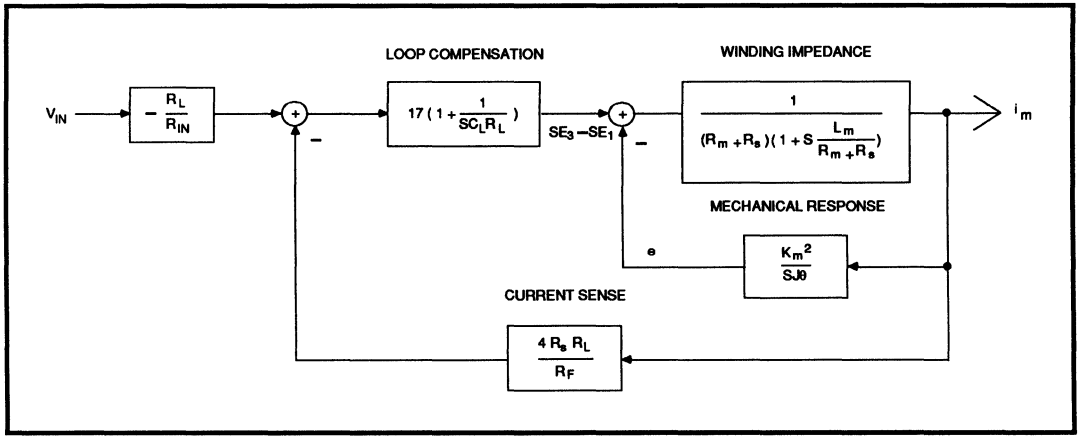


FIGURE 4(A): TRANSFER FUNCTION OF SSI 32H569 IN TYPICAL APPLICATION WITH FIXED FIELD DC MOTOR

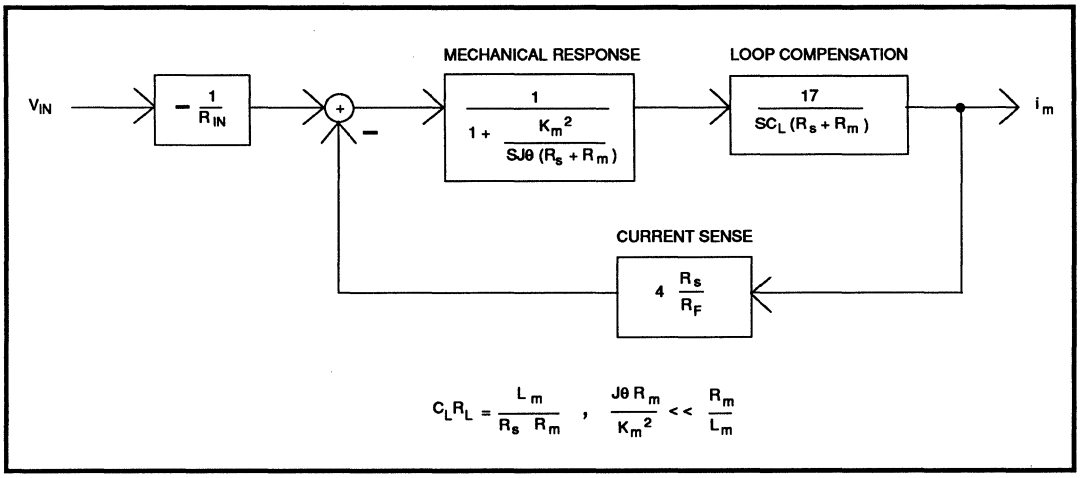


FIGURE 4(B): SIMPLIFIED TRANSFER FUNCTION OF SSI 32H569 IN DC MOTOR APPLICATION

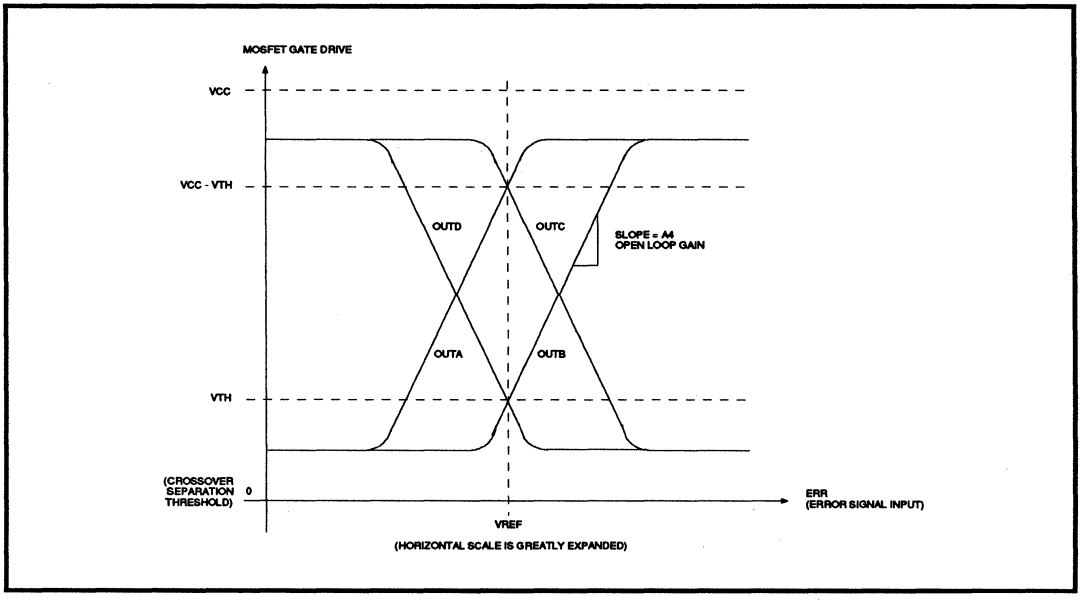


FIGURE 4(B): SIMPLIFIED TRANSFER FUNCTION OF SSI 32H569 IN DC MOTOR APPLICATION

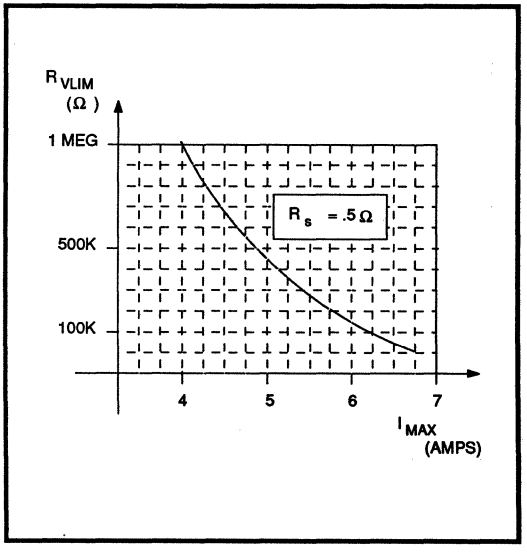


FIGURE 6: RVLIM TO GROUND TYPICAL MOTOR CURRENT LIMIT

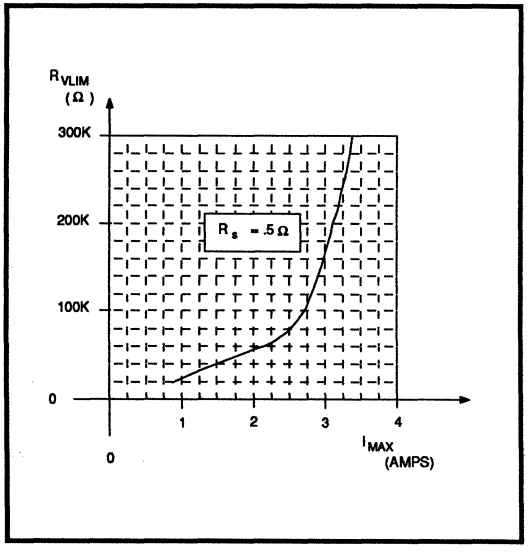


FIGURE 7: RVLIM TO VREF TYPICAL MOTOR CURRENT LIMIT

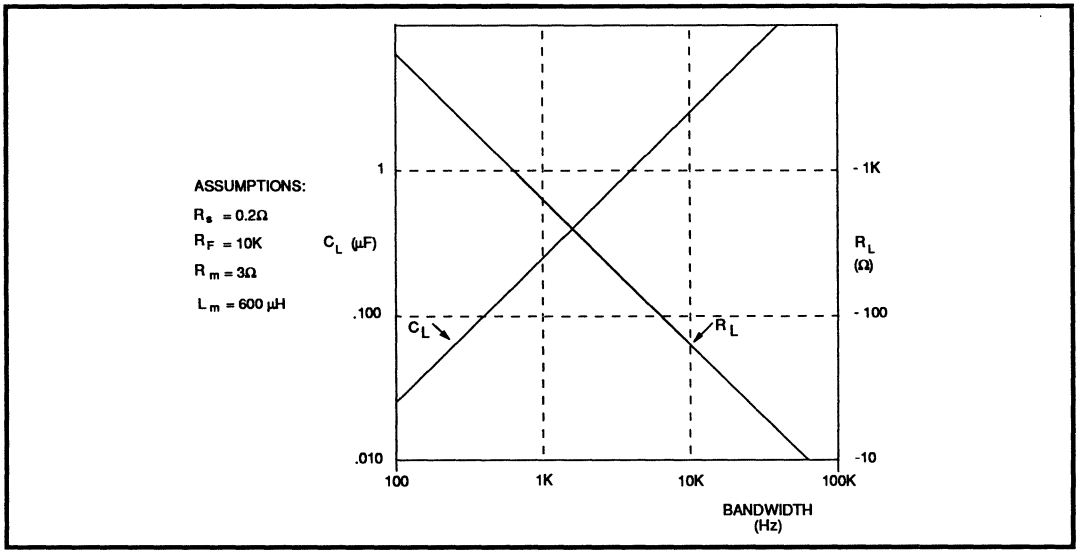


FIGURE 8: TYPICAL MOTOR DRIVER COMPENSATION

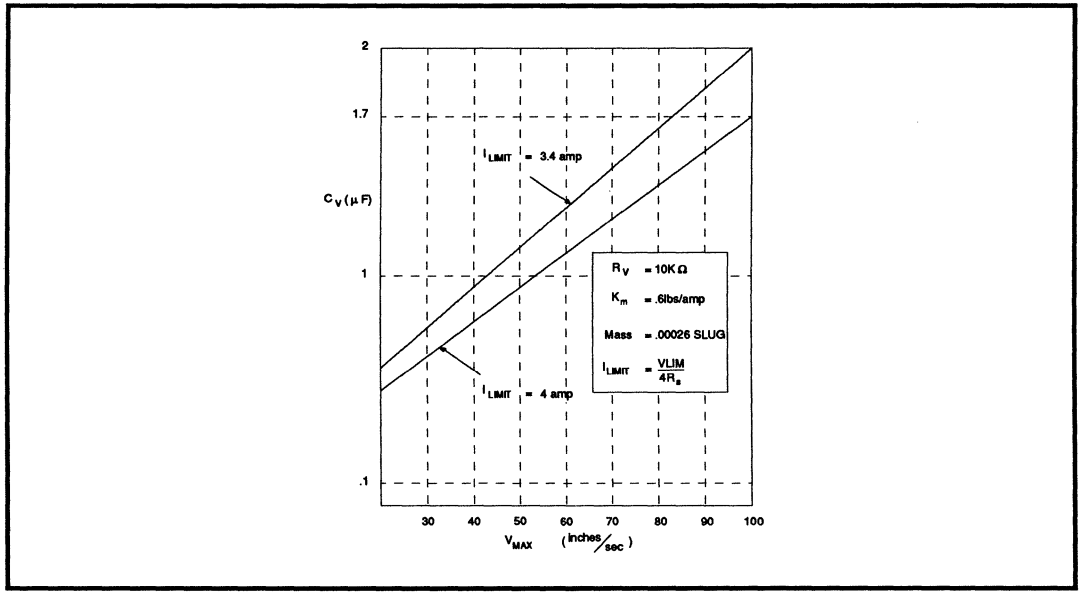


FIGURE 9: TYPICAL MOTOR VELOCITY LIMIT

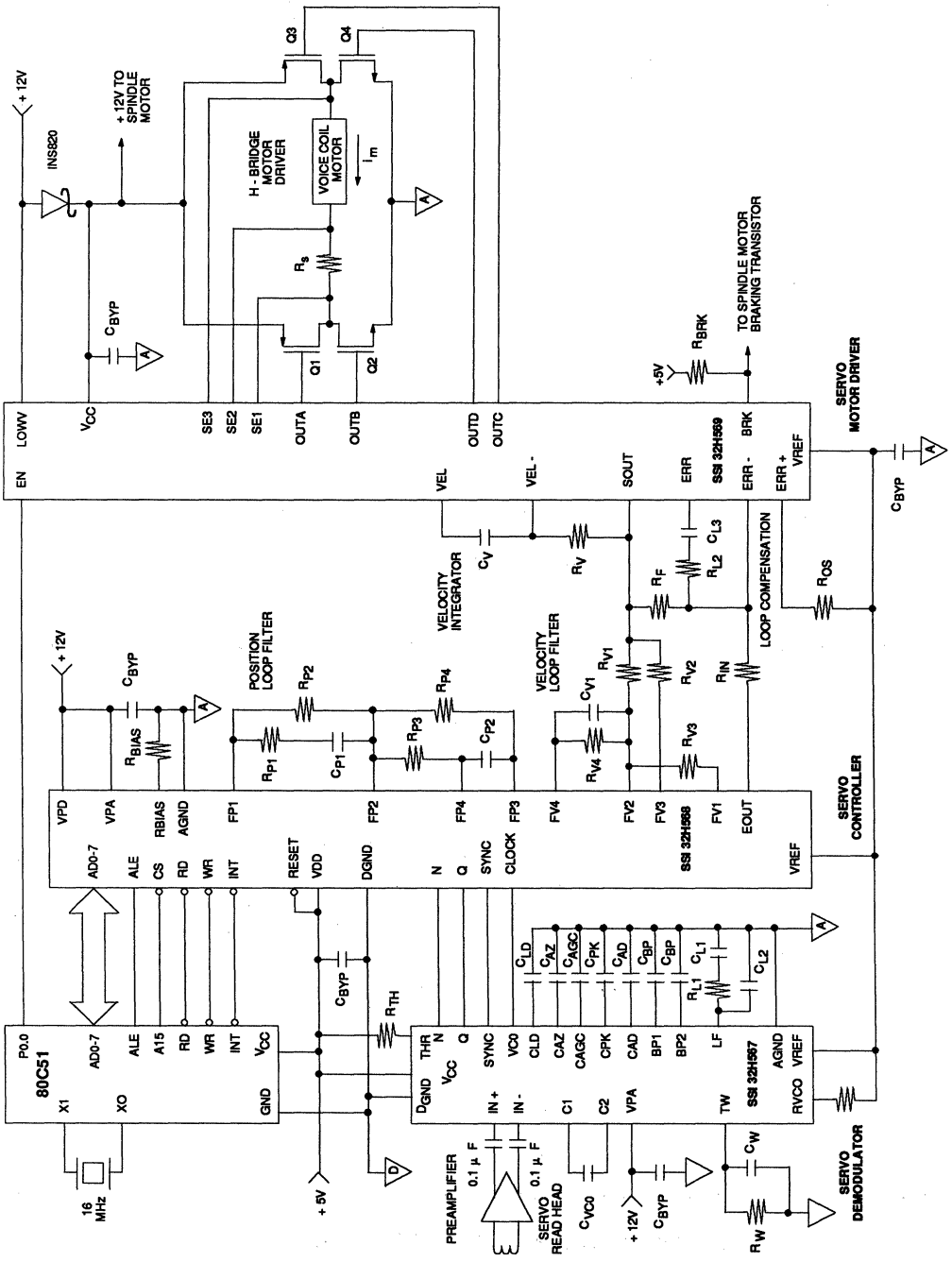
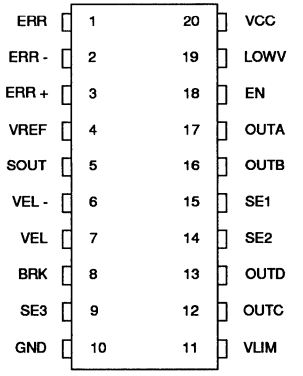


FIGURE 10: COMPLETE EXAMPLE OF SERVO PATH ELECTRONICS USING THE SSI 32H567/568/569 CHIP SET

0888

PACKAGE PIN DESIGNATIONS
(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.



20-Pin SO, DIP

4

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32H569, Servo Motor Driver		
20-Pin DIP	SSI 32H569-CP	32H569-CP
20-Pin SOL	SSI 32H569-CS	32H569-CS

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NOTES:

Section 5

HDD SPINDLE MOTOR CONTROL

silicon systems™
INNOVATORS IN INTEGRATION

SSI 32M590-Series
5-1/4 Inch Motor Speed Control

August, 1988

DESCRIPTION

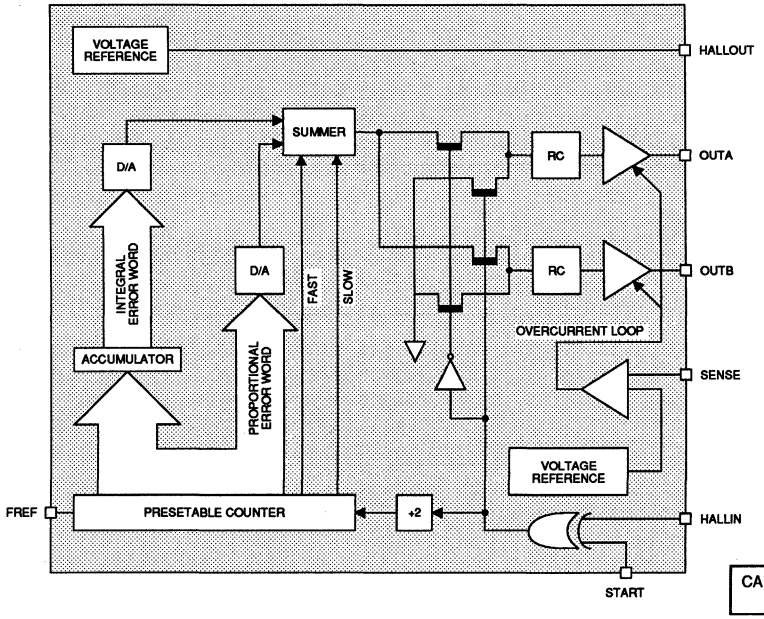
The SSI 32M590-Series consisting of SSI 32M5901 and SSI 32M5902 are motor controller ICs designed to provide all timing and control functions necessary to start, drive and brake a two-phase, four-pole, brushless DC spindle motor. The IC requires two external power transistors (such as Darlington power transistors), three external resistors, and an external frequency reference. The motor HALL sensor is directly driven and decoded by the device. The controller is optimized for a 3600 rpm disc drive motor using a 2 Mega-Hertz clock. Motor protection features include stuck rotor shutdown, coil over-current detection and control, and supply fault detection. The device's linear control loop controls the power drivers using Pulse Amplitude Modulation.

FEATURES

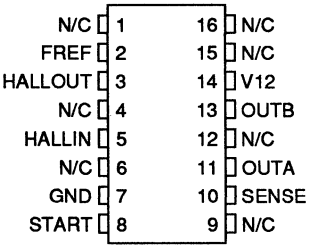
- **Available in 8-pin DIP (SSI 32M5901), 14-pin DIP (SSI 32M5902) or 16-pin SOL (SSI 32M5902)**
- **CMOS with single +12 volt power supply**
- **All motor START, DRIVE and STOP timing and control**
- **Includes HALL-Effect sensor drive and input pins**
- **Highly Accurate speed regulation of ±.035%**
- **Active braking function (32M5902 only)**
- **On-chip digital filtering requires no external compensation or adjustments**
- **Provides protection against stuck rotor, coil over-current, and supply fault**
- **Regenerative braking with shutdown**

5

BLOCK DIAGRAM



PIN DIAGRAM



SSI 32M5902

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The device incorporates both analog and digital circuit techniques to utilize the advantages of each. The analog portion of the loop uses switched capacitor filter technology to eliminate external components. The control loop uses a Pulse Amplitude Modulation (PAM) control scheme to avoid the switching transients and torque ripple inherent in Pulse Width Modulation (PWM) schemes.

A binary counter is preset once per motor revolution by an index signal generated by the HALL position sensor. On the next index pulse, the remaining least significant bits are loaded into the proportional D/A and accumulated by a saturation accumulator. The most significant bits are loaded into the integral D/A. The size of the accumulator and the bit locations determine the major scaling (within a factor of two) for the gain and zero location of the filter. To prevent overflow in the proportional D/A the counter is decoded to detect overflow, and the proportional D/A is saturated as needed. The overflow also generates a boost signal used in the summer. The range of the accumulator is larger than the linear range of the proportional channel to help filter small load disturbances that tend to saturate the proportional channel. The entire counter is also used to provide a time-out feature to protect the motor and external circuitry.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
FREF	I	Frequency Reference Input. A TTL compatible input used by the device to set and maintain the desired motor speed and operate circuit blocks.
HALLOUT	O	Provides a regulated bias voltage for the HALL effect sensor inside the motor.
HALLIN	I	HALL Sensor Input. The TTL open-collector type output of the motor's Hall switch feeds this input which has a resistor pullup to the HALLOUT bias voltage. Refer to Figure 1 for input timing.
OUTA, OUTB	O	Driver Outputs. These two driver outputs drive the external power transistors, such as TIP120 NPN Darlington power transistors as shown in the typical application. The power transistors control the motor current through the current setting resistor Re. The motor current is V (sense)/Re. During normal operation, the drive voltages are adjusted as necessary to maintain the proper motor speed and drive current. Regenerative braking is accomplished with self biasing of the power transistors thru resistors Rb with power shutdown. Refer to Figure 1 for output timing.
SENSE	I	Coil Current Sense Line. Senses the coil current and limits the sense voltage to the threshold by limiting the drive to the external power transistors.
START	I	Active Brake Control, only available on 14-pin package. The active brake is enabled by applying a logic "0" to the START pin. During active braking the output phasing is reversed to apply a reverse torque to the motor until the motor period drops below the reverse shutdown speed at which time the drivers turn off the external power transistors to deny power to the motor. Active braking is shown in Figure 1.
N/C	-	No Connection, 14-pin package only. These pins must remain unconnected and floating.

PROTECTION FEATURES

LOW VOLTAGE DETECTION

If the supply drops below the detect threshold the device will turn off all of the external power transistors to prevent damage to the motor and the power devices.

STUCK ROTOR SHUTDOWN

If the delay from power onset to a positive Index transition or the time interval between successive Index transitions is greater than the prescribed time, the device interprets this delay as a stuck rotor and reduces the motor current to zero until such time as one positive HALLIN transition is detected or until power is removed and reapplied.

MOTOR COIL OVER-CURRENT

Refer to SENSE input description. Sense voltage is generated by current through Re shown in the typical application. The SENSE input threshold limits the maximum coil current.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive Supply Voltage, VDD	14	V
Storage Temperature	-65 to +125	°C
Ambient Operating Temperature	0 to 70	°C
HALLIN, FREF, START, and SENSE Input Voltages	-0.3 to VDD +0.3	V
HALLOUT Current	10	mA
Lead Temperature (soldering, 10 sec.)	260	°C
Power Dissipation	400	mW

5

RECOMMENDED OPERATING CONDITIONS

Unless otherwise specified, 10.8V ≤ V12 ≤ 13.2V; 0 °C ≤ TA ≤ 70 °C; FREF = 2.00 MHz; Re = 0.4Ω ± 10% (2 watt); Rb = 4.7 KΩ ± 10% (1/4 watt); 0.8 ≤ Darlington Vbe ≤ 1.8

Motor Parameters: (1 to 3 platters)

KT	Torque constant	= 0.015 Nt-m/amp ±10%
J	Inertia	= 0.000489 Nt-m/s/s ±33%
KD	Damping factor	= 0.0000318 Nt-m/rad/sec ± 33%

where: $\frac{\text{Motor Frequency (s)}}{\text{Motor Current (s)}} = \frac{KT}{J \times s + KD}$

DC ELECTRICAL CHARACTERISTICS

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
POWER SUPPLY CURRENT					
ICC (Includes Drive Outputs)		(17 typ)		30	mA
FREF AND START INPUTS					
Input Low Voltage	Iil = 500 µA			0.8	V
Input High Voltage	Iih = 100 µA	2.0			V

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
HALL SENSOR INTERFACE					
HALLOUT Bias voltage	I = 5 mA	5.0		6.8	V
HALLOUT Pullup Resistance	To HALLOUT Pin	5		20	KΩ
Input Low Voltage				1.0	V
Input High Voltage		4.0			V
DRIVER OUTPUTS					
Sink Capability	VOUTA or VOUTB = 0.5 Volts	5.0			mA
Source Capability	VOUTA or VOUTB = 3.0 Volts	-5.0			mA
Capacity Load Drive Capability				50.0	pF
SENSE INPUT					
Threshold Voltage		0.9		1.1	V
Input Current		-100		100	µA
Input Capacitance				25.0	pF
STUCK ROTOR DETECTION					
Shutdown Time	Power On To Driver	0.815		0.935	sec
LOW VOLTAGE DETECTION					
Detect Threshold		6.0		9.0	V
CONTROL LOOP - DESCRIPTION*					
Divider Ratio	FREF/Avg. Motor Frequency	16664		16672	
Index to Index Jitter	Total Jitter			8.0	µsec
Loop Gain H (2 X π X f)	f = 2 Hz		0 Typical		dB
Loop Zero	Kp/Ki	0.97		1.03	Hz
CONTROL LOOP Vs SUPPLY VARIATION					
$\frac{Kp\,(V12 = 13.2V)}{Kp\,(V12 = 10.8V)}$		0.96		1.04	
$\frac{Ki\,(V12 = 13.2V)}{Ki\,(V12 = 10.8V)}$		0.96		1.04	
START/STOP VELOCITY PROFILES					
Power on Delay to FHALL Greater than FREF/16668	1 Platter	7.0		11.0	sec
	2 Platters	9.0		13.0	sec
	3 Platters	11.0		15.0	sec
Speed Overshoot $\frac{FHALL - (FREF/16668)}{(FREF/16668)}$	1 Platter	0.5		2.0	%
	2 Platters	0.5		2.0	%
	3 Platters	0.5		2.0	%

START/STOP VELOCITY PROFILES (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
Setting Time: Motor Frequency Settles to 0.05%	1 Platter	9.0		13.0	sec
	2 Platters	11.0		15.0	sec
	3 Platters	13.0		17.0	sec
Stop Time (Regenerative): Motor Frequency Slows to 30% after Power is Removed	1 Platter	7.0		13.0	sec
	2 Platters	8.0		15.0	sec
	3 Platters	9.0		17.0	sec
Stop Time (Active):		4.0			sec

*The continuous Time Transfer Function of the on-chip control can be modeled as follows:

$$H(s) = \frac{Vc(s)}{F(s)} = Ki \times \frac{(1+s/(2\times\pi\times(Kp/Ki)))}{s}$$

Ki = Integral gain
Kp = Proportional gain

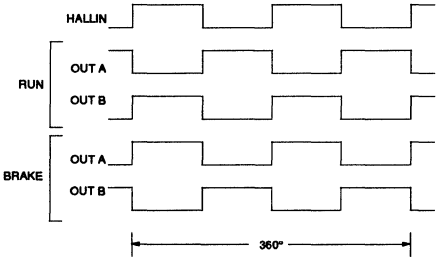
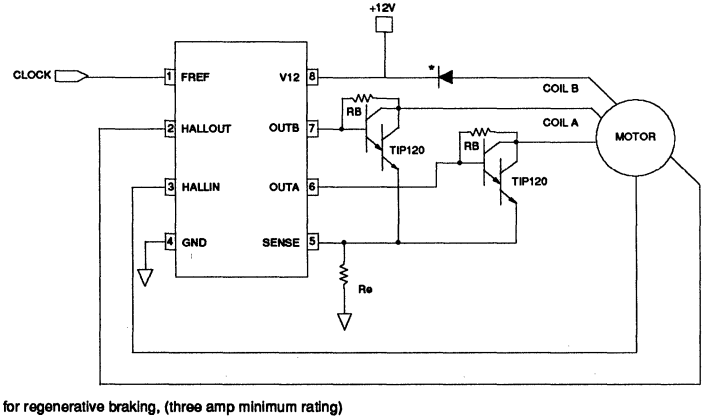


FIGURE 1: Firing Order

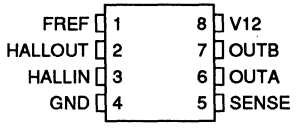


*NOTE: Diode required for regenerative braking, (three amp minimum rating)

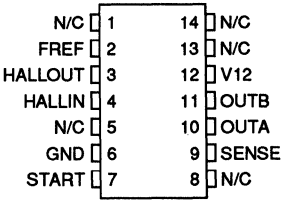
FIGURE 2: Typical Application

SSI 32M590-Series
5-1/4 Inch
Motor Speed Control

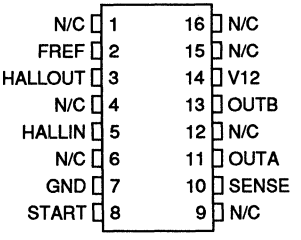
PACKAGE PIN DESIGNATIONS
(TOP VIEW)



SSI 32M5901
8-Pin PDIP



SSI 32M5902
14-Pin PDIP



SSI 32M5902
16-Pin SOL

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32M590-Series		
8-Pin PDIP	SSI 32M5901-CP	SSI 32M5901-CP
14-Pin PDIP	SSI 32M5902-CP	SSI 32M5902-CP
16-Pin SOL	SSI 32M5902-CL	SSI 32M5902-CL

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SSI 32M591
Three-Phase 5-1/4 Inch Winchester Motor Speed Control

August, 1988

DESCRIPTION

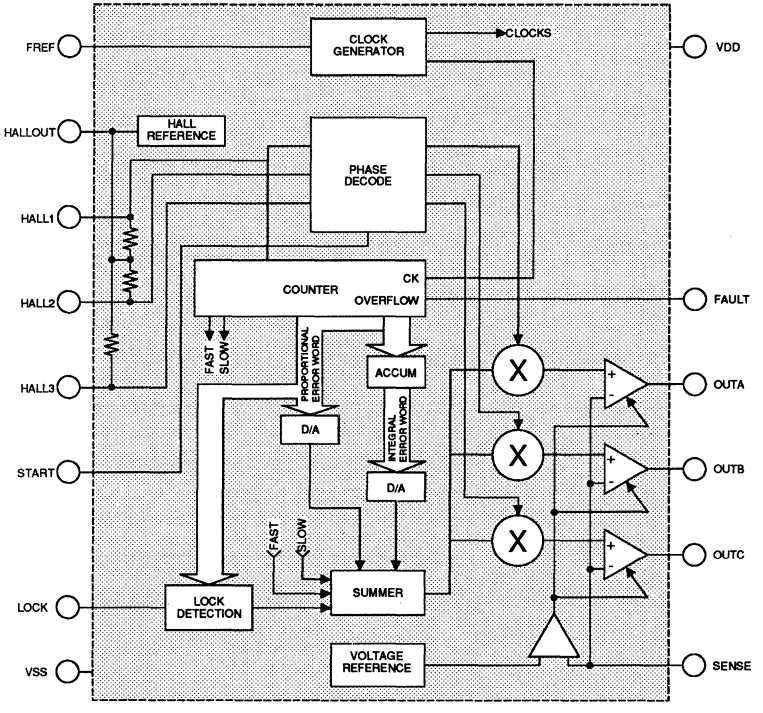
The SSI 32M591 is a motor controller IC designed to provide all timing and control functions necessary to start, drive and brake a three-phase brushless DC spindle motor. The IC requires three external power transistors (such as Darlington power transistors), one external power resistor, and an external frequency reference. The three motor HALL sensors are directly driven and decoded by the device. The controller is optimized for a 3600 rpm disk drive motor using a 2 Mega-Hertz clock. Motor protection features include stuck rotor shutdown, supply and clock fault detection, all of which are indicated by a FAULT signal, and coil over-current detection and control. A LOCK signal is provided to indicate that the motor is at speed. The device's linear control loop controls the power drivers using Pulse Amplitude Modulation.

FEATURES

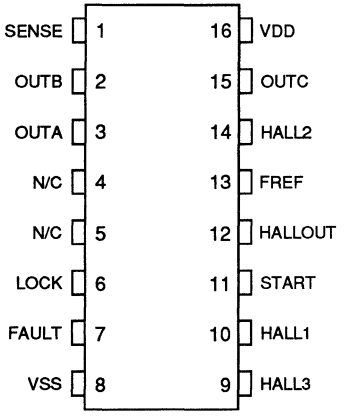
- **CMOS with TTL/LSTTL compatible control functions**
- **Single +12 volt power supply**
- **All motor START, DRIVE, and STOP timing and control**
- **Includes HALL-Effect sensor drive and input pins**
- **Highly accurate speed regulation of ±.05 %**
- **Active braking function**
- **On-chip digital filtering requires no external compensation of adjustments**
- **Provides protection against stuck rotor, motor coil over-current, supply fault, or clock fault**
- **At speed indication provided**

5

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATIONS

The device incorporates both analog and digital circuit techniques to utilize the advantages of each. The analog portion of the loop uses switched capacitor filter technology to eliminate external components. The control loop uses a Pulse Amplitude Modulation (PAM) control scheme to avoid the switching transients and torque ripple inherent in Pulse Width Modulation (PWM) schemes.

PIN DESCRIPTION

SYMBOL	I/O	DESCRIPTION
VDD	I	+12V Power supply
VSS	I	Ground
FREF	I	FREQUENCY REFERENCE INPUT: A TTL compatible input used by the device to set and maintain the desired motor speed and operate circuit blocks. This input level must not exceed VDD at any time.
HALLOUT	O	HALL SENSOR BIAS OUTPUT: Provides a regulated bias voltage for the Hall effect sensors, inside the motor.
HALL1, HALL2, HALL3	I	HALL SENSOR INPUTS: The TTL open-collector type outputs of the motor's Hall switches feed these inputs which have a resistor pullup to the HALLOUT bias voltage. The HALL1 input is used to index the control loop counter. Refer to figure 1 for input timing.
OUTA, OUTB, OUTC	O	DRIVER OUTPUTS: These three driver outputs drive the external power transistors, such as TIP120 NPN Darlington power transistors shown in the typical application. The power transistors control the motor current through the current setting resistor Re. The motor current is V(sense)/Re. During normal operation, the driver output voltages are adjusted as necessary to maintain the proper motor speed and drive current. Refer to figure 1 for output timing.
SENSE	I	COIL CURRENT SENSE INPUT: Senses the coil current and limits the sense voltage to the threshold by limiting the drive to the external power transistors.
LOCK	O	AT SPEED INDICATOR OUTPUT: An open drain LSTTL compatible output that indicates with an active low that the period of the motor is within the controller's linear range. Because of the accuracy of the loop, the LOCK pin is a good "at speed" indicator.
START	I	ACTIVE BRAKE CONTROL INPUT: The active brake is enabled by applying a logic "0" to the START pin. During active braking the driver output's phasing is changed to apply a reverse torque to the motor until the motor period drops below the reverse shutdown speed at which time the drivers turn off the external power transistors to deny power to the motor. Active braking timing is shown in figure 1. Do not enable active braking at motor speeds below 120 rpm.
FAULT	O	FAULT INDICATOR OUTPUT: Goes high when the motor is determined to be stalled, VDD is low, or FREF clock is too slow.
N/C	-	NO CONNECTION: These pins must be left unconnected and floating.

FUNCTIONAL DESCRIPTIONS

A binary counter is preset once per motor revolution by an index signal developed from the HALL1 input. On the next index pulse, the remaining least significant bits are loaded into the proportional D/A and accumulated by a saturating accumulator. The most significant bits are loaded into the integral D/A. The size of the accumulator and the bit locations determine the major scaling (within a factor of two) for the gain and zero location of the filter. To prevent overflow in the proportional D/A , the counter is decoded to detect overflow and the proportional D/A is saturated as needed. The overflow also generates a boost signal used in the summer. The range of the accumulator is larger than the linear range of the proportional channel to help filter small load disturbances that tend to saturate the proportional channel. The entire counter is also used to provide a time-out feature to protect the motor and external circuitry.

PROTECTION FEATURES

Low Voltage Detection
If the supply drops below the detect threshold, the device will turn off all of the external power transistors to prevent damage to the motor and the power devices. The FAULT pin goes high in this condition.

Stalled Rotor Shutdown
If the delay from power onset to a positive index transition or the time interval between successive index transitions is greater than the prescribed time, the device interprets this delay as a stalled rotor and reduces the motor current to zero until such time as one positive index transition is detected or until power is removed and reapplied. The FAULT output goes high when the motor is determined to be stalled.

Motor Coil Over-Current
Refer to SENSE input description. The voltage generated by motor coil current through Re is sensed as shown in the typical application. The sense input threshold limits the maximum coil current.

FREF Clock Fault
If the FREF frequency drops below the specified minimum frequency, the driver will shut down and the FAULT pin will go high.

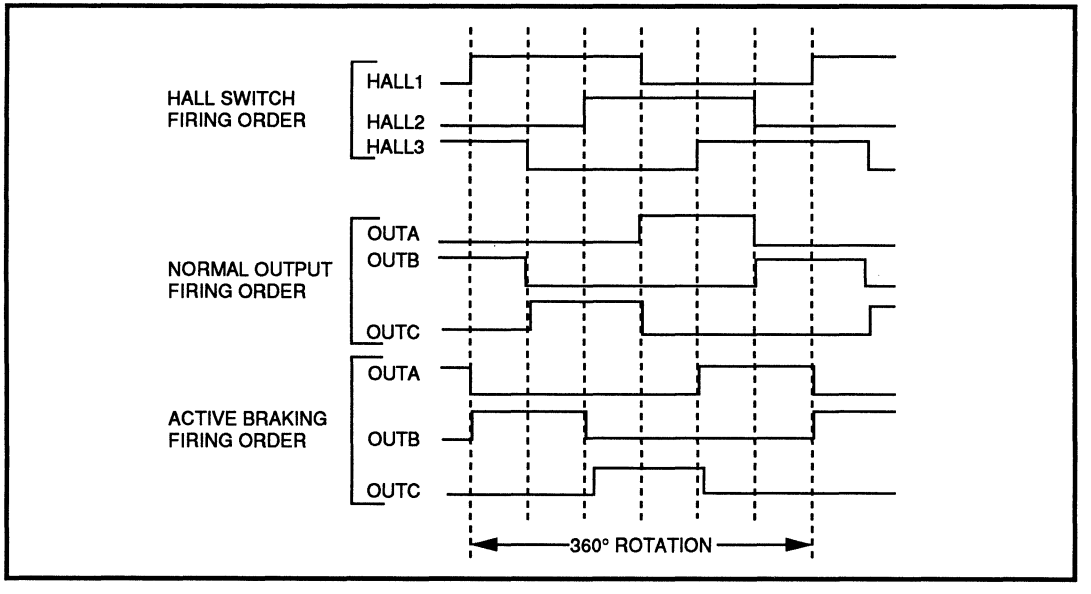


FIGURE 1: HALL Switch/Driver Timing Relationship

ELECTRICAL CHARACTERSTICS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

PARAMETER	RATING	UNIT
Positive Supply Voltage, VDD	14	V
Storage Temperature	-65 to + 125	°C
Pin Voltage (except FAULT and LOCK)	-0.3 to VDD +0.3	V
FAULT and LOCK Pin Voltage	-0.3 to VDD +5.0	V
HALLOUT Current	20	mA
Lead Temperature (soldering, 10 sec)	260	°C

RECOMMENDED OPERATION CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
DC Supply Voltage, VDD		10.8	12.0	13.2	V
Input Clock, FREF		1.9998	2	2.0002	MHz
Ambient Temperature, Ta		0		70	°C
Emitter Resistor, Re		.392	.4	.408	Ω
Power Darlington Vbe		0.8		1.8	V
Motor Parameters (1)	$\frac{\text{Motor Frequency (s)}}{\text{Motor Current (s)}} = \frac{KT}{Js + KD}$				
KT, Torque Constant Range	(0.15 Nt-m/A nom)	-10		+10	%
J, Inertia Range	(489×10^{-6} Nt-m-sec^2 nom)	-33		+33	%
KD, Damping Factor Range	(31.8×10^{-6} Nt-m/rad/sec nom)	-33		+33	%
Winding resistance (2)			2.0		Ohms
Winding inductance			2.0		mH
Back EMF (2)			0.0159		V/rad/sec

Notes:

(1) The motor parameters given are for a typical motor. The device will work for a range of motors near this nominal motor.

(2) The motor must have a back EMF less than 10 volts peak (measured from center tap to drive transistor collector/drain) at speed to insure linear operation of drive transistors and a coil resistance small enough to insure adequate start current.

DC ELECTRICAL CHARACTERISTICS.
Unless otherwise specified, 10.8V≤VDD≤13.2V: 0°C≤TA≤70°C; FREF = 2.000MHz; Re = 0.4 Ohms; Motor Configuration is 4-pole 3-phase center-tap "Y".

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Power Supply Current					
ICC	Clock Active 1(HALLOUT) = 15mA 1 Driver loaded to = 5 mA 2 Drivers unloaded			30	mA
Power Dissipation				400	mW
Fault Detection					
Low Voltage Detect Threshold		6.8		9.0	V
Input Logic Signals - 'FREF' and 'START' Inputs					
Vil, Input Low Voltage				0.08	V
Iil, Input Low Current	Vin = 0	–500			µA
Vih, Input High Voltage		2.0			V
IiH, Input High Current	Vin = 5			100	µA
Output Logic Signals - 'LOCK' and 'FAULT' Pins					
Vol	Isink = 2mA			0.4	V
Ioh	Vout = VDD			10	µA
HALL Sensor Interface					
HALLOUT Bias Voltage	I = 0 to –15mA	5.0		6.8	V
HALL1,2,3 Pullup Resistance	To HALLOUT pin	5		20	KΩ
Input Low Voltage				1.0	V
Input High Voltage		4.0			V
Driver Outputs					
Sink Capability	Vol = 0.5V	1.0			mA
Source Capability	Voh = 3.0V	–5.0			mA
Capacitive Load Drive Capability			50.0		pF
Sense Input And Over-Current Control					
Threshold Voltage		0.9		1.1	V
Input Current		–100		100	µA

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 10.8V ≤ VDD ≤ 13.2V; 0°C ≤ TA ≤ 70°C; FREF = 2.000 MHz; Re=0.4 Ohms.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Fault Detection					
Stalled Rotor Shutdown Time	Power On to driver	0.850		0.900	sec
Low FREF Shutdown Threshold				100	Hz
Lock Indication					
Lock Range	Motor Speed	3585		3615	Hz
Control Loop Parameters*					
Divider Ratio	FREF/Fmotor		33,336		
Instantaneous Speed Error	Referenced to 60Hz	–0.035	0.01	0.015	%
Index to Index Jitter (16/FREF)	Total jitter			8	µs
Loop Bandwidth	Nominal motor Re = 0.40Ω		2		Hz
Loop Zero	Ki/Kp		1.0		Hz
Maximum Running Current	Re = 0.40Ω	1.50			Amps
Minimum Running Current	Re = 0.40Ω			0	Amps
Start Current	Re = 0.40Ω	2.25		2.75	Amps
Input Logic Signals-'FREF' and 'START' Pins					
Input Capacitance				25	pF
Hall Sensor Interface					
Input Capacitance				25	pF
Sense Input and Over-current Control					
Input Capacitance				25	pF

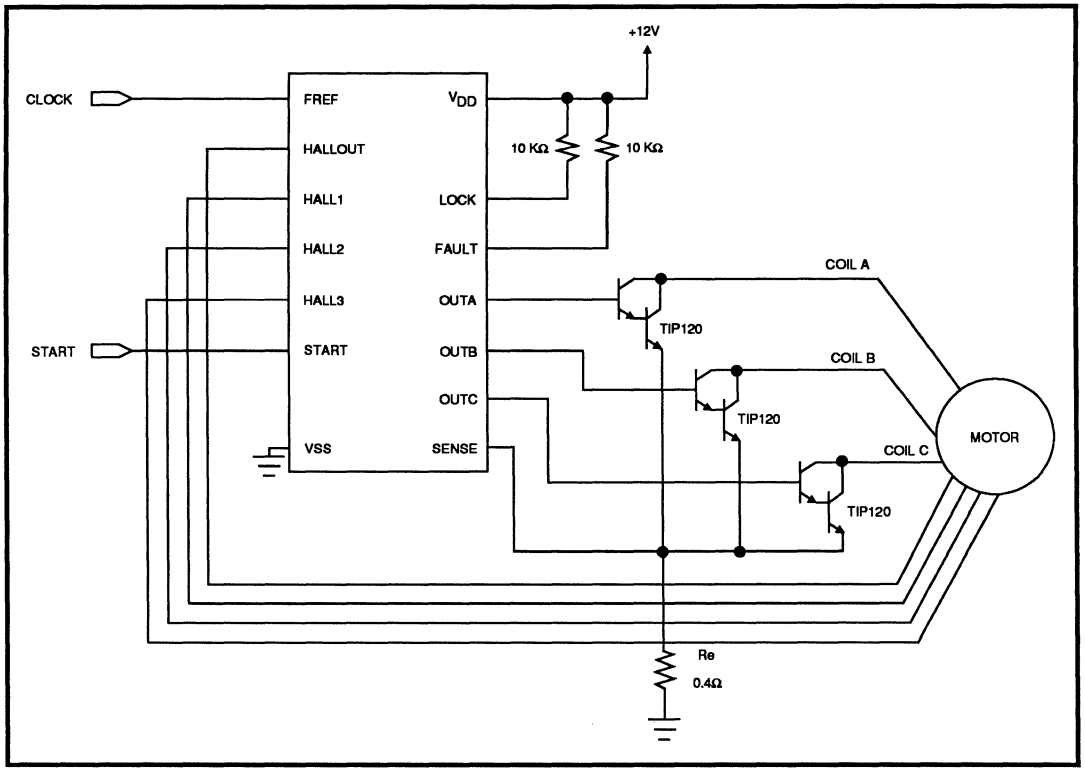
*Control Loop Notes:

Running current limits refer to capabilities during speed correction.

The motor control loop consists of counters, logic, and digital-to-analog converters that provide loop time constants. The continuous time transfer function of the on chip control can be modeled as follows:

$$H(s) = \frac{Vc(s)}{Fm(s)} = \frac{Ki}{s} + Kp$$

Vc(s) is the voltage applied to the external setting resistor Re by the modulator. By adjusting the value of Re the gain the motor sees can be adjusted, as can the starting current.



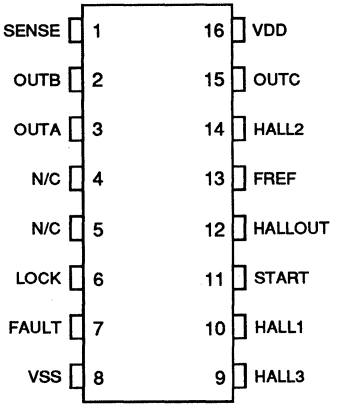
Typical Application Diagram

SSI 32M591
Three-Phase 5-1/4 Inch
Winchester Motor Speed Control

PIN DIAGRAM
(TOP VIEW)

THERMAL CHARACTERISTICS: Øja

16-Pin DIP	75°C/W
16-Pin SOL	105°C/W



16-Pin DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32M591 16-Pin Plastic DIP	SSI 32M591-CP	32M591-CP
SSI 32M591 16-Pin SOL	SSI 32M591-CL	32M591-CL

Silicon Systems™

Silicon Systems, Inc., 14351 Myford Road, Tustin CA 92680, (714) 731-7110, TWX 910-595-2809

SSI 32M593
Three-Phase Delta Motor Speed Controller

June, 1988

DESCRIPTION

The SSI 32M593 is a motor speed control IC designed to provide all timing and control functions necessary to start, drive, and brake a 3-phase, 4 or 8 pole brushless DC spindle motor. External Darlington power transistors or external power FETs may be used by the SSI 32M593 to drive the spindle motor.

The motor Hall sensors are directly driven and decoded by the device. The controller is optimized for a 3600 rpm motor using a 2 MHz clock. Motor protection features include jammed platter shutdown, supply and clock fault detection, all of which are indicated by a FAULT signal, and coil over-current detection and control. A LOCK signal is provided to indicate that the motor is at speed. The device's linear control loop controls the power drivers using Pulse Amplitude Modulation.

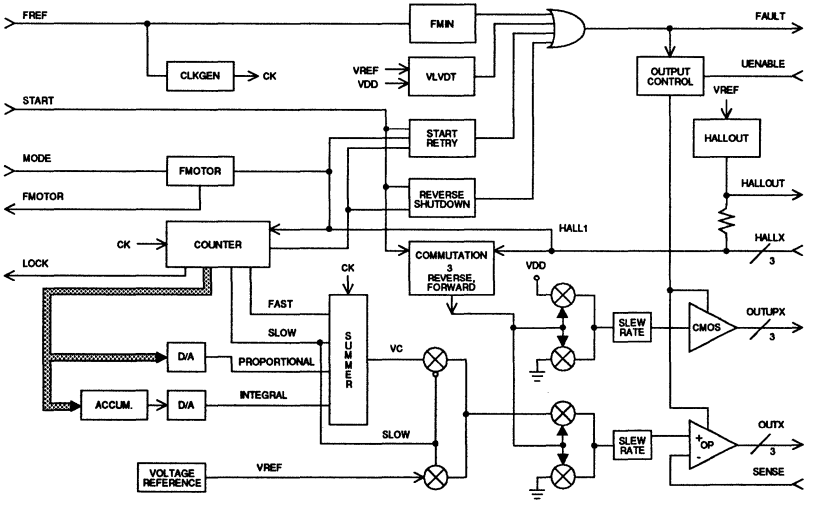
The SSI 32M593 requires a +12V power supply, and is available in 20-pin DIP or SO packages.

FEATURES

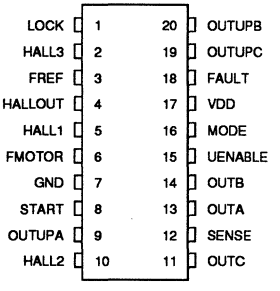
- **3-phase bipolar or unipolar operation**
- **4 or 8-pole operation**
- **3600 rpm speed control using a 2 MHz clock**
- **Highly accurate speed regulation of ±0.037%**
- **On-chip digital filter**
- **At speed indication provided**
- **Active braking function**
- **Output pre-driver for center tap or non-center tap windings**
- **Drives complementary Darlington power transistors or complementary power FETs**
- **Power supply fault protection**
- **Motor over-current protection**
- **Multiple retry on jammed spindle**
- **Single +12 volt power supply**

5

BLOCK DIAGRAM



PIN DIAGRAM



20-PIN DIP or SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32M593 uses a mix of analog and digital techniques to accomplish speed control. The control signal is generated by analog conversion of a digital speed error term developed by examining the contents of a count-down counter once per motor revolution. The sign and magnitude of the remainder controls the amplitude of a correction signal applied to the motor. Commutation timing, developed from motor generated HALL signals, applies the correction in the proper phase sequence.

The device uses a Pulse Amplitude Modulation (PAM) scheme rather than Pulse Width Modulation (PWM) to avoid the switching transients and torque ripple inherent in PWM.

In operation, the SSI 32M593 is installed in a closed loop control system that maintains the speed of a 3–Phase Brushless DC motor. By monitoring the HALL signal outputs of the motor, a control voltage is developed using both digital and analog techniques. The analog portion of the control loop uses switched capacitor techniques to eliminate the need for any external passive components required for loop compensation. An operation description of the circuit follows.

CONTROL LOOP

Referring to the block diagram, the major sections of the control loop are a 19-stage Counter, Integral and Proportional channels, D/A's and a Summer.

The speed error is determined by examining the contents of the counter once per revolution. The counter is preset once per revolution by an INDEX signal developed from the HALL1 input, at the same time any remainder resulting from a 500 KHz count-down rate is loaded into a latch.

The lower LSB's of the latch, except for the LSB, are used to drive the Proportional D/A while the entire contents of the latch are accumulated to control the Integral Channel. The MSB's of the accumulator drive the Integral D/A.

If the contents of the counter indicate that the speed is outside the linear regulation range (±0.037%), this is decoded as a "FAST" or "SLOW" condition. Under these conditions the Proportional D/A output is driven to either end of its range, as appropriate. Under a slow condition, a fixed reference voltage is supplied to the output drives.

The Summer then outputs a control voltage (VC) consisting of a bias voltage plus or minus the sum of the two D/A outputs.

The Integral and Proportional channels perform several functions related to the operation of the control loop. One function is to control loop stability by maintaining the loop zero at 1 Hz. In operation this translates to the Integral channel responding to major bias point changes while the Proportional channel takes care of minor perturbations to the loop.

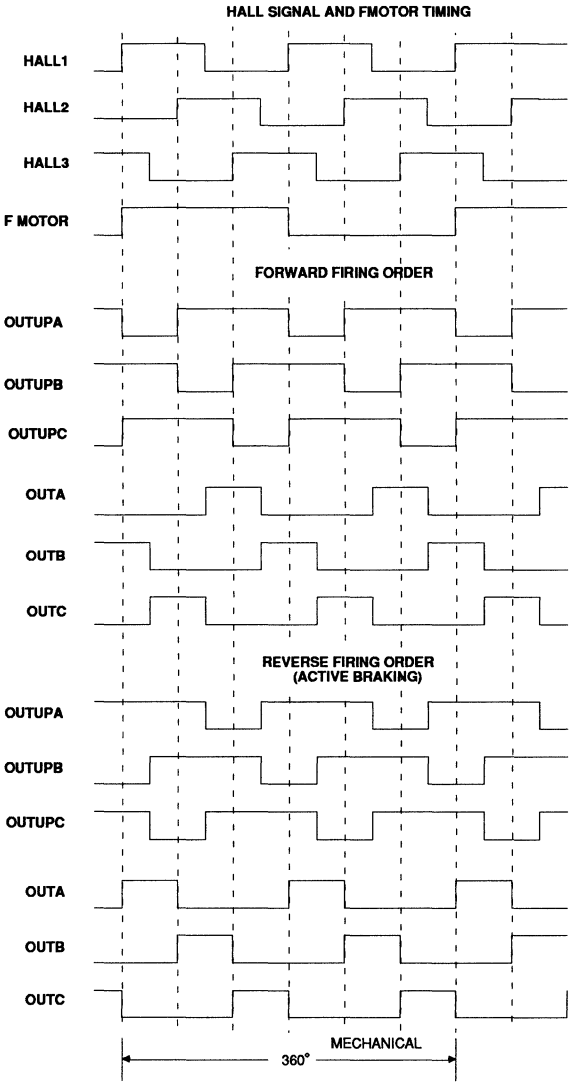
COMMUTATION

The summer output is channeled to the appropriate OUTA, B, C output according to the timing shown in Figure 1. To reduce switching transients, the outputs are slew rate controlled during each transition.

OUTUPA, B, C outputs cycle between approximately VDD in the OFF state and GND in the ON state also according to Figure 1. Again, rise and fall times are controlled during transitions.

MOTOR COIL OVER-CURRENT

Refer to SENSE input description. Sense voltage is generated by current through Re shown in the typical application. The SENSE input threshold limits the maximum coil current.



NOTE: Figure shows commutation of a 4-pole device. 8-pole devices apply same firing order twice per revolution.

FIGURE 1: COMMUTATION TIMING DIAGRAM

FUNCTIONAL DESCRIPTION (Continued)

FAULT CONDITIONS

Four conditions cause an active high on the FAULT output pin, also disabling all drivers except as noted :

(1) Low power supply - VDD < Vlvdt

(2) No FREF clock - FREF < Fmin

(3) Stalled motor. If the delay from power onset to a positive HALL index transition or the time interval between successive HALL index transitions is greater than the specified time, the device interprets this delay as a stalled motor, reduces the motor current to zero and performs three retry cycles. If the motor continues to be stalled after three retries, then motor current is reduced to zero until such time as one positive HALL index transition is detected, the START pin is toggled, or power or FREF is removed and re-applied. After the fourth try, FAULT goes high. (See Figure 2.)

(4) Reverse shutdown speed. During active braking (START=0) the HALL sensor's phasing is changed to apply a reverse torque to the motor until the motor speed drops below the reverse shutdown speed at which time the drivers turn off to deny power to the motor and FAULT goes high. If UENABLE is high (non-center tapped motor) the device will perform passive braking after the motor speed drops below the reverse shutdown speed by enabling the lower drivers, OUTX, to dissipate any remaining coil energy. The upper drivers OUTUPX are off. (See Figure 3.)

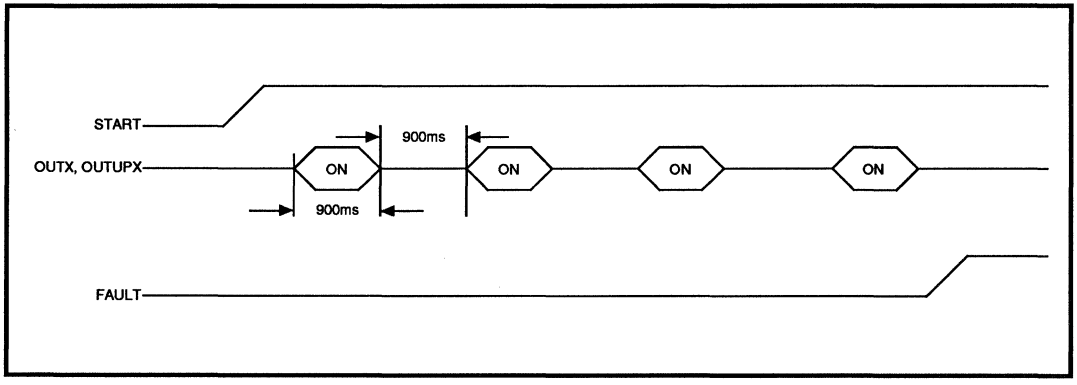


FIGURE 2: JAMMED PLATTER SEQUENCE

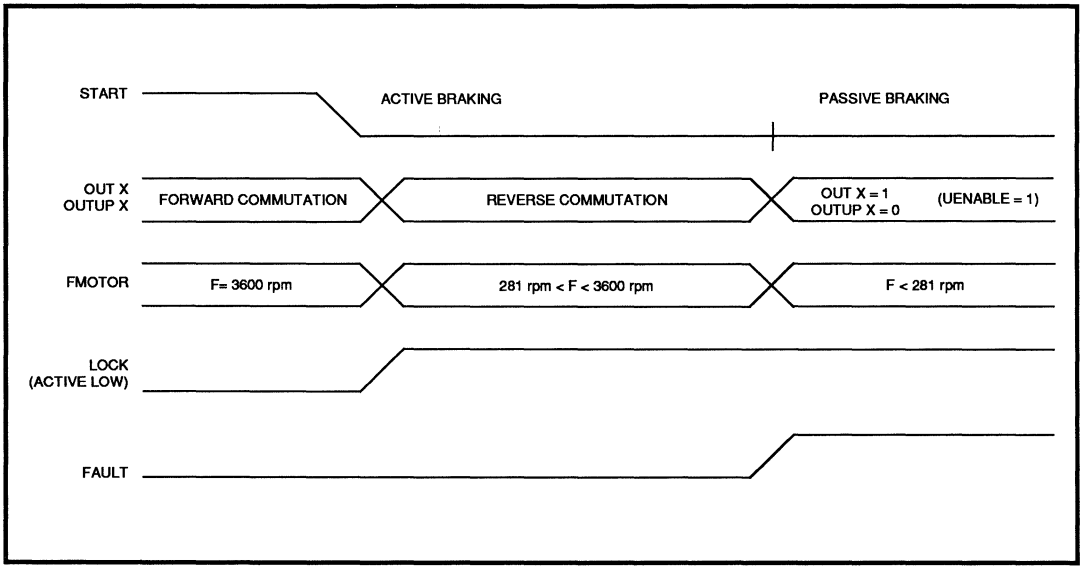


FIGURE 3: ACTIVE BRAKING SEQUENCE

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VDD	I	+12V Power Supply
GND	I	Ground
FREF	I	The reference clock input used to set motor speed and operate circuit blocks.
START	I	Spin start is enabled by applying a logic "one" to the START pin. It may be connected to VDD in systems that do not require active braking. Active braking is enabled by applying a logic "zero" to the START pin. During active braking the commutation is changed to apply a reverse torque to the motor until the motor velocity drops below 281 rpm.
MODE	I	Mode Control. When tied high (to VDD) selects 8-pole operation where HALL1 signal is divided by four to generate an index signal. When left open, 4-pole operation is selected and HALL1 is divided by two.
UENABLE	I	Tying UENABLE to GND forces all upper outputs to their off state and disables passive braking. UENABLE must be tied to GND for unipolar center-tapped motors. Tied high or floating, UENABLE = 1 and drives bipolar motors.
FAULT	O	FAULT goes active high indicating low VDD, no FREF, a stalled motor, or motor velocity below the reverse shutdown speed.
LOCK	O	LOCK goes active low when the motor frequency is within a specified lock range.
FMOTOR	O	FMOTOR frequency indicates the motor speed, nominally 3600 rpm. FMOTOR is derived from HALL1.
SENSE	I	Coil Current Sense Input. Senses the coil current and limits the sense voltage to the specified threshold by limiting the voltage from the lower drivers. (OUTX)
HALLOUT	O	Hall Sensor Bias Output. Provides a regulated bias voltage for the hall effect sensors.
HALL1, 2, 3	I	Hall Sensor inputs that determine commutation. The TTL open-collector type motor outputs drive these inputs, which have internal resistor pullups referenced to the HALLOUT bias voltage.
OUTUPA, B, C	O	Upper motor CMOS level outputs that drive either Darlingtons or PFETs.
OUTA, B, C	O	Lower Driver Outputs. These three driver outputs drive external Bipolar or NFET power transistors to control the motor current through the current setting resistor Re. The motor current is V(sense)/Re. During normal operation, the drive voltages are adjusted as necessary to maintain the proper motor speed and drive current.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	-0.5 to +14V	V
Storage Temperature	-65 to +150	°C
Lead Temperature, PDIP (10 sec. soldering)	260	°C
Package Temperature, SO (20 sec. reflow)	215	°C
Input, Output pins	-0.3 to VDD +0.3	V
Inputs and outputs are protected from static charge using built-in ESD and Latchup protection devices.		

ELECTRICAL CHARACTERISTICS (Unless otherwise specified Vlvdt <Vdd<13.2V.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VDD supply voltage		10.8	12	13.2	V
IDD supply current	includes output driver current	-	20	38	mA
PDD power dissipation	IoutA or B, or C = -10 mA IoutupA, or B, or C = 10 mA IHALLOUT = -10 mA	-	240	375	mW
FREF clock frequency		1.998	2	2.002	MHz
TA ambient temperature		0	-	70	°C
TTL Inputs START, FREF, UENABLE					
Vil input low voltage	Iil ≤500 µA	-	-	0.8	V
Vih input high voltage	Iih ≤100 µA	2.0	-	-	V
MODE Input					
Vil input low voltage		-	-	0.5	V
Vih input high voltage	Iih ≤500 µA	VDD-.5	-	-	V
HALLX Input					
Vil input low voltage		-	-	1.0	V
Vih input high voltage	External pullup current ≤1.7 mA	3.0	-	-	V
Input Pullup-Pulldown Resistance					
Internal pullup resistance	START, FREF, UENABLE	40	-	-	KΩ
Internal pullup resistance	HALLX inputs	5	-	20	KΩ
Internal pulldown resistance	MODE input	40	-	-	KΩ
Input capacitance	All inputs	-	-	25	pF

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
SENSE Input						
SENSE voltage threshold		if exceeded, driver voltage is limited	0.9	1.0	1.1	V
Input current			-100	-	+100	µA
Open Drain Outputs LOCK, FMOTOR, FAULT						
Vol output low voltage		I_{OL} = 2 mA	-	-	0.5	V
Typical external pullup resistor			-	10	-	KΩ
FAULT Indication						
Vlvdt, low voltage			8.0	-	9.5	V
Fmin, loss of FREF			-	-	100	Hz
Stuck motor, start pulses		drivers on, drivers off	-	0.90	-	sec
Number of start pulses			-	4	-	-
Reverse shutdown speed		START = 0	-	281	-	rpm
LOCK Indication						
Lock range		Measure at FMOTOR, FREF =	3594	3600	3607	rpm
Speed error		2 MHz, 10.8 < V_{DD} < 13.2	-.037		+.037	%
HALL Sensor Interface						
HALLOUT bias voltage		10.8 < VDD < 13.2, Iload = -5 mA	5.0		6.8	V
		10.8 < VDD < 13.2, Iload = -10 mA	5.0			V
Driver Outputs (FHALLX ≥ 100 Hz, V_{lvdt} < VDD ≤ 13.2, CL ≤ 500 pF unless otherwise specified.)						
Slew rate		All driver outputs	150	-	400	V/msec
OUTX	Voh	Iload = -7.5 mA	3.75	-	-	V
	Voh	Iload = -100 µA, 10.8 ≤ V_{DD} ≤ 13.2	8.0	-	-	V
	Vol off state	Iload = 3.4mA, 5.0 ≤ V_{DD} ≤ 13.2	-	-	0.5	V
OUTUPX	Vol	Iload = 10 mA	-	-	3.0	V
	Voh off state	Iload = -5 mA	V_{DD}-0.5	-	-	V
	Voh off state	Iload = -2 mA, 5.0 ≤ VDD ≤ V_{lvdt}	V_{DD}-0.5	-	-	V

APPLICATION INFORMATION

PARAMETER	RECOMMENDED	MIN	NOM	MAX	UNIT
Power Transistors					
Re, Emitter Resistor		.392	.4	.408	Ω
Power Darlington Vbe	Typical device: TIP 125, TIP 120	0.8	-	1.8	V
Power FET Vth	Typical device: IRFT 001	2	-	6	V
Power FET Rds (on)		-	-	0.4	Ω
Power FET BVds		30	-	-	V

Motor Parameters

The SSI 32M593 MSC is optimized for use with a 5 1/4" three-platter Winchester motor. The device will work for a range of motors near this nominal motor. Attempts to use a significantly different motor may require careful choice of a sense resistor for good spin-up and regulation.

KT, Torque Constant Range	(0.015 Nt-m/A nom.)	-10	-	+10	%
J, Inertia Range	(489 x 10^{-6} Nt-m-sec^2 nom.)	-33	-	+33	%
KD, Damping Factor Range	(31.8 x 10^{-6} Nt-m/rad/sec nom.)	-33	-	+33	%
Note: $\frac{\text{Motor Frequency (s)}}{\text{Motor Current (s)}} = \frac{KT}{Js + KD}$					

Control Loop Parameters

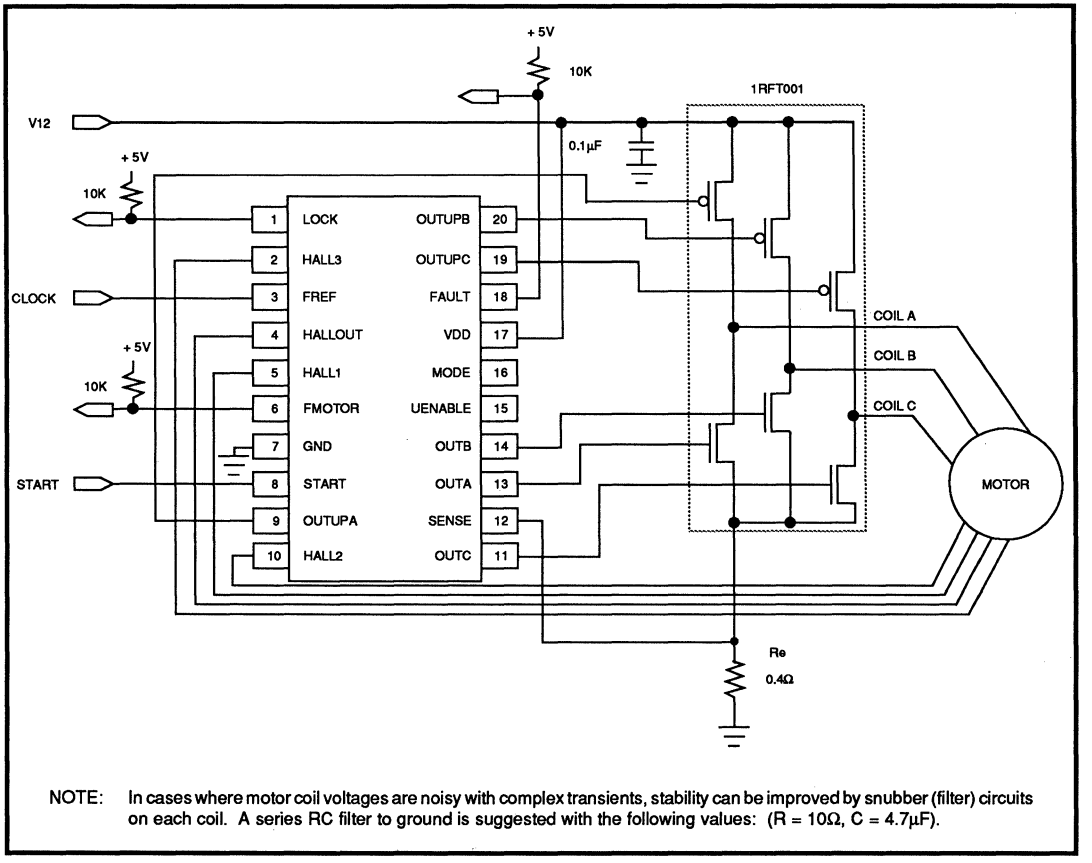
The motor control loop consists of counter, logic, and digital-to-analog converters that provide loop time constants. The continuous time transfer function of the on-chip control can be modeled as follows:

$$H(s) = \frac{Vc(s)}{Fm(s)} = \frac{Ki}{s} + Kp$$

Where: Ki = Integral Channel Gain
Kp = Proportional Channel Gain

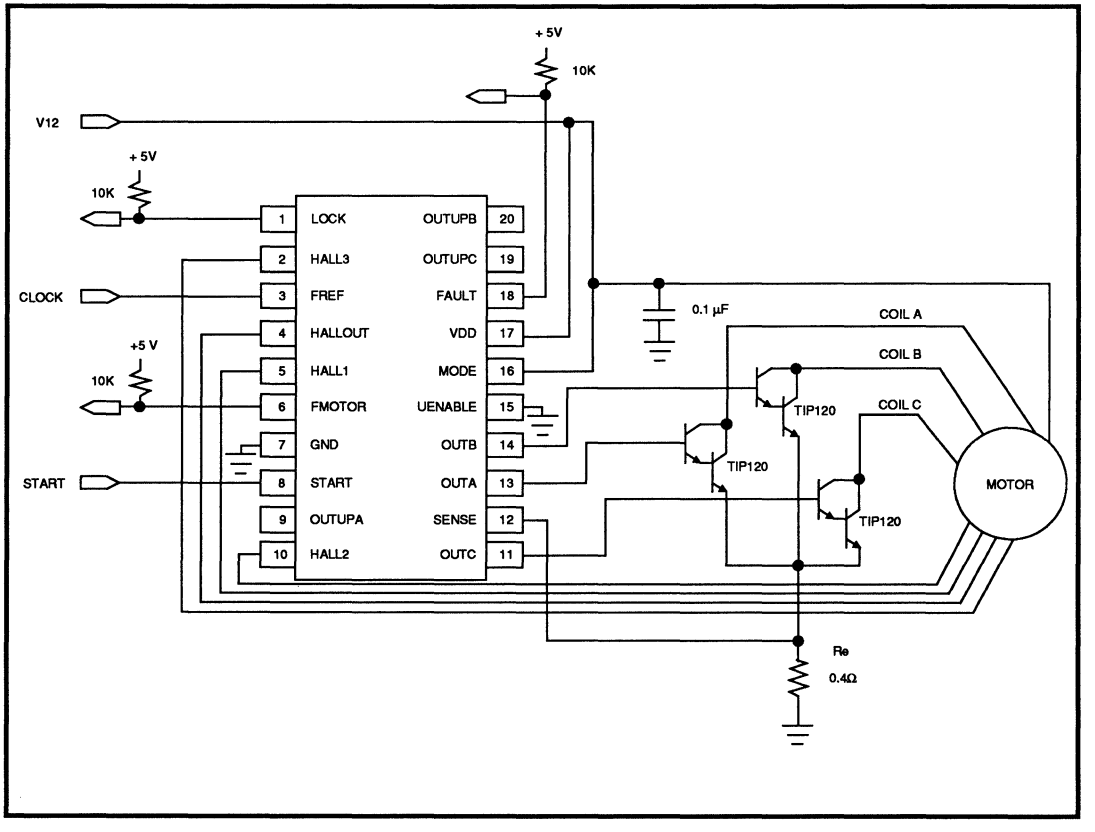
Vc(s) is the voltage applied to the external sense resistor (Re) by the modulator. By adjusting the value of Re, the gain the motor sees can be adjusted as can the starting current.

Loop Bandwidth	Nominal motor, Re=.4Ω		2		Hz
Loop Zero	Ki/Kp		1.0		Hz
Kp, Proportional Channel Gain		0.198	0.213	0.227	V/rad/s
Ki, Integral Channel Gain		1.23	1.33	1.42	V/rad
Start current	Re = 0.40Ω		2.5		Amps
Running current	Re = 0.40Ω		1.5		Amps



NOTE: In cases where motor coil voltages are noisy with complex transients, stability can be improved by snubber (filter) circuits on each coil. A series RC filter to ground is suggested with the following values: (R = 10Ω, C = 4.7µF).

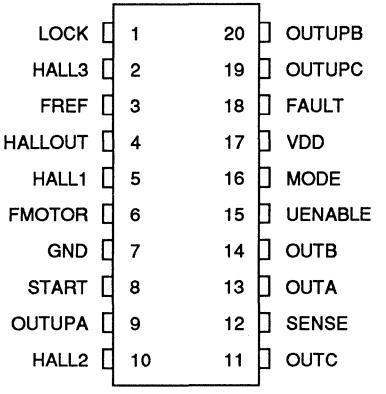
**TYPICAL THREE-PHASE, 4-POLE, BIPOLAR,
NON-CENTER TAPPED MOTOR USING A POWER FET MODULE**



**TYPICAL THREE-PHASE, 8-POLE, UNIPOLAR,
CENTER TAPPED MOTOR USING A POWER DARLINGTONS. UENABLE MUST BE TIED TO GND.**

SSI 32M593
Three-Phase Delta
Motor Speed Controller

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



20-Pin DIP or SOL

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32M593 Three-Phase SOL	SSI 32M593-CL	32M593-CL
SSI 32M593 Three-Phase PDIP	SSI 32M593-CP	32M593-CP

silicon systems™
Silicon Systems, Inc., 14351 Myford Road, Tustin CA 92680, (714) 731-7110, TWX 910-595-2809

SSI 32M594
Three-Phase Delta Motor Speed Controller

August, 1988

DESCRIPTION

The SSI 32M594 is a motor speed control IC designed to provide all timing and control functions necessary to start, drive, and brake a 3-phase, 4 or 8 pole brushless DC spindle motor. External Darlington power transistors or external power FETs may be used by the SSI 32M594 to drive the spindle motor.

The motor Hall sensors are directly driven and decoded by the device. The controller is optimized for a 3600 rpm motor using a 2 MHz clock. Motor protection features include jammed platter shutdown, supply and clock fault detection, all of which are indicated by a FAULT signal, and coil over-current detection and control. A $\overline{\text{LOCK}}$ signal is provided to indicate that the motor is at speed. The device's linear control loop controls the power drivers using Pulse Amplitude Modulation.

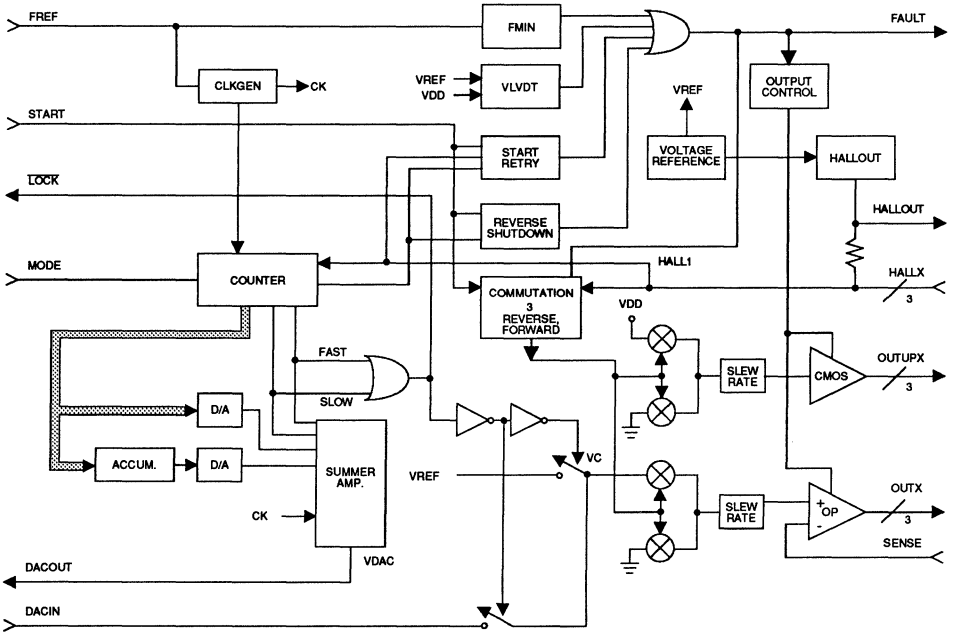
The SSI 32M594 requires a +12V power supply, and is available in 20-pin DIP or SO packages.

FEATURES

- **Supports wide range of DC brushless 3-phase motors, including 3 1/2" motors**
- **4 or 8-pole operation**
- **3600 rpm speed control using a 2 MHz clock**
- **Highly accurate speed regulation of ±0.037%**
- **Provides for gain scaling of the motor current voltage**
- **On-chip digital filter**
- **At speed indication provided**
- **Active braking function**
- **Output pre-driver for center tap or non-center tap windings**
- **Drives complementary Darlington power transistors or complementary power FETs**
- **Power supply fault protection**
- **Motor over-current protection**
- **Multiple retry on jammed spindle**
- **Single +12 volt power supply**

5

BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

The SSI 32M594 uses a mix of analog and digital techniques to accomplish speed control. The control signal is generated by analog conversion of a digital speed error term developed by examining the contents of a count-down counter once per motor revolution. The sign and magnitude of the remainder controls the amplitude of a correction signal applied to the motor. Commutation timing, developed from motor generated HALL signals, applies the correction in the proper phase sequence.

The device uses a Pulse Amplitude Modulation (PAM) scheme rather than Pulse Width Modulation (PWM) to avoid the switching transients and torque ripple inherent in PWM.

The SSI 32M594 generates a motor current voltage which is related to the motor speed error. This is implemented on the IC by digital/analog techniques, converting a motor frequency error derived from a reference clock and digital counter into a voltage using switched capacitor D/A's. The voltage Vc translates into a motor current across Re regulating motor speed.

In operation, the SSI 32M594 is installed in a closed loop control system that maintains the speed of a 3–Phase Brushless DC motor. By monitoring the HALL signal outputs of the motor, a control voltage is developed using both digital and analog techniques. The analog portion of the control loop uses switched capacitor techniques to eliminate the need for any external passive components required for loop compensation. An operation description of the circuit follows.

CONTROL LOOP

Referring to the block diagram, the major sections of the control loop are a 19-stage Counter, Integral and Proportional channels, D/A's and a Summer.

The speed error is determined by examining the contents of the counter once per revolution. The counter is preset once per revolution by an INDEX signal developed from the HALL1 input, at the same time any remainder resulting from a 500 KHz count-down rate is loaded into a latch.

The lower LSB's of the latch, except for the LSB, are used to drive the Proportional D/A while the entire contents of the latch are accumulated to control the Integral Channel. The MSB's of the accumulator drive the Integral D/A.

If the contents of the counter indicate that the speed is outside the linear regulation range (±0.037%), this is decoded as a "FAST" or "SLOW" condition. Under these conditions the Proportional D/A output is driven to either end of its range, as appropriate. Under a slow condition, a fixed reference voltage is supplied to the output drives resulting in a start current of Vref/Re.

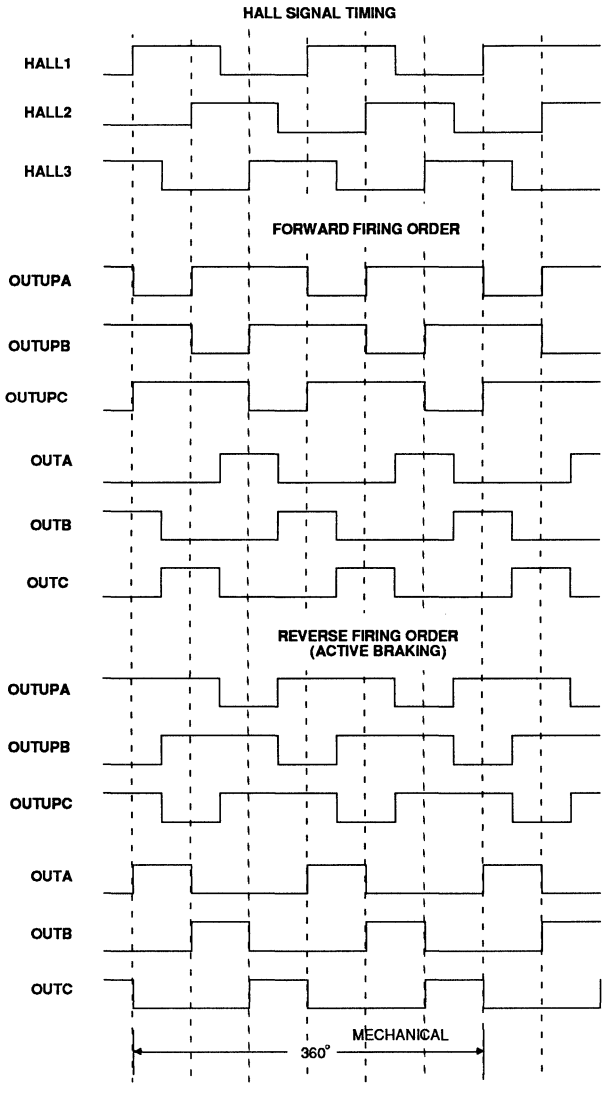
When $\overline{LOCK}$ is low, the control voltage, VDAC, from the summer is used to generate the motor running current. VDAC is a summation of integral channel voltage which cancels out offsets in the loop and motor losses, and a proportional channel voltage which tracks speed variations from the counter. The two channel voltages are then summed and weighted. The control voltage applied is externally scaleable by resistors R1 and R2 at DACOUT and DACIN (see Typical Application diagram) to fit a wide range of motors including those used in 3 1/2" drives. Note that Re affects start current while R1 and R2 affect running current as Irunning = V_{DACIN}/Re.

The Integral and Proportional channels perform several functions related to the operation of the control loop. One function is to control loop stability by maintaining the loop zero at 1 Hz. In operation this translates to the Integral channel responding to major bias point changes while the Proportional channel takes care of minor perturbations to the loop.

COMMUTATION

The summer output is channeled to the appropriate OUTA, B; C output according to the timing shown in Figure 1. To reduce switching transients, the outputs are slew rate controlled during each transition.

OUTUPA, B, C outputs cycle between approximately VDD in the OFF state and GND in the ON state also according to Figure 1. Again, rise and fall times are controlled during transitions.



NOTE: Figure shows commutation of a 4-pole device. 8-pole devices apply same firing order twice per revolution.

FIGURE 1: Commutation Timing Diagram

FUNCTIONAL DESCRIPTION (Continued)

MOTOR COIL OVER-CURRENT

Refer to SENSE input description. Sense voltage is generated by current through Re shown in the typical application. The SENSE input threshold limits the maximum coil current.

FAULT CONDITIONS

Four conditions cause an active high on the FAULT output pin, also disabling all drivers except as noted :

(1) Low power supply - VDD < Vlvdt

(2) No FREF clock - FREF < Fmin

(3) Stalled motor. If the delay from power onset to a positive HALL index transition or the time interval between successive HALL index transitions is greater than the specified time, the device interprets this delay as a stalled motor, reduces the motor current to zero and performs three retry cycles. If the motor continues to be stalled after three retries, then motor current is reduced to zero until such time as one positive HALL index transition is detected, the START pin is toggled, or power or FREF is removed and re-applied. After the fourth try, FAULT goes high. (See Figure 2)

(4) Reverse shutdown speed. During active braking (START = 0) the HALL sensor's phasing is changed to apply a reverse torque to the motor until the motor speed drops below the reverse shutdown speed at which time the drivers turn off to deny power to the motor and FAULT goes high. (See Figure 3)

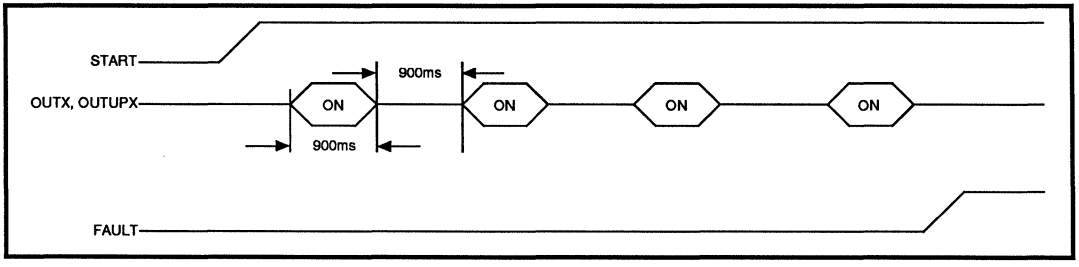


FIGURE 2: Jammed Platter Sequence

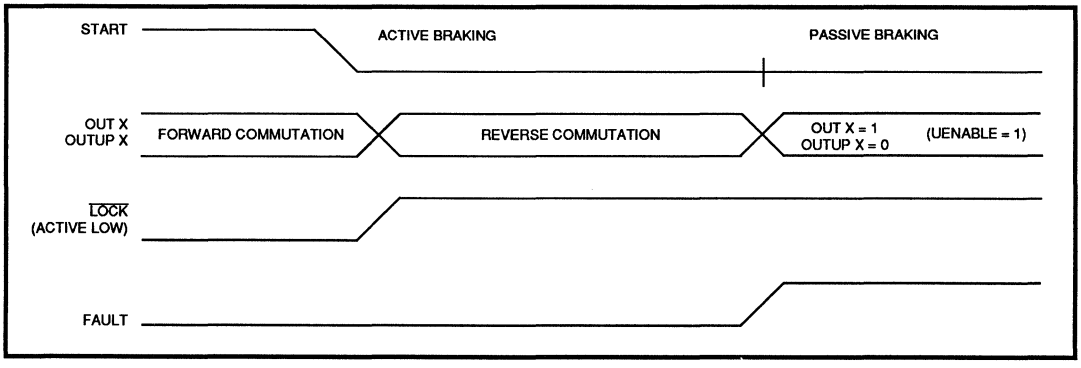


FIGURE 3: Active Braking Sequence

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VDD	I	+12V Power Supply
GND	I	Ground
FREF	I	The reference clock input used to set motor speed and operate circuit blocks.
START	I	Spin start is enabled by applying a logic "one" to the START pin. It may be connected to VDD in systems that do not require active braking. Active braking is enabled by applying a logic "zero" to the START pin. During active braking the commutation is changed to apply a reverse torque to the motor until the motor velocity drops below 281 rpm.
MODE	I	Mode Control. When tied high (to VDD) selects 8-pole operation where HALL1 signal is divided by four to generate an index signal. When left open, 4-pole operation is selected and HALL1 is divided by two.
FAULT	O	FAULT goes active high indicating low VDD, no FREF, a stalled motor, or motor velocity below the reverse shutdown speed.
$\overline{\text{LOCK}}$	O	$\overline{\text{LOCK}}$, open drain active low, goes active low when the motor frequency is within a specified lock range.
SENSE	I	Coil Current Sense Input. Senses the coil current and limits the sense voltage to the specified threshold by limiting the voltage from the lower drivers. (OUTX)
HALLOUT	O	Hall Sensor Bias Output. Provides a regulated bias voltage for the hall effect sensors.
HALL1, 2, 3	I	Hall Sensor inputs that determine commutation. The TTL open-collector type motor outputs drive these inputs, which have internal resistor pullups referenced to the HALLOUT bias voltage.
OUTUPA, B, C	O	Upper motor CMOS level outputs that drive either Darlingtons or PFETs.
OUTA, B, C	O	Lower Driver Outputs. These three driver outputs drive external Bipolar or NFET power transistors to control the motor current through the current setting resistor Re. During normal operation, the drive voltages are adjusted as necessary to maintain the proper motor speed and drive current.
DACIN	I	Reference voltage for motor current.
DACOUT	O	Summer Output (VDAC). The summation of integral and proportional channel voltages.

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

PARAMETER	RATING	UNIT
VDD Supply Voltage	-0.5 to +14V	V
Storage Temperature	-65 to +150	°C
Lead Temperature, PDIP (10 sec. soldering)	260	°C
Package Temperature, SO (20 sec. reflow)	215	°C
Input, Output pins	-0.3 to VDD +0.3	V
Inputs and outputs are protected from static charge using built-in ESD and Latchup protection devices.		

ELECTRICAL CHARACTERISTICS (Unless otherwise specified Vlvdt <VDD<13.2V.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VDD supply voltage		10.8	12	13.2	V
IDD supply current	includes output driver current	-	20	38	mA
PDD power dissipation	IoutA or B, or C = -10 mA IoutupA, or B, or C = 10 mA IHALLOUT = -10 mA	-	240	375	mW
FREF clock frequency		1.998	2	2.002	MHz
TA ambient temperature		0	-	70	°C
TTL Inputs START, FREF					
VIL Input Low Voltage	IIL ≤500 µA	-	-	0.8	V
VIH Input High Voltage	IIH ≤100 µA	2.0	-	-	V
MODE Input					
VIL Input Low Voltage		-	-	0.5	V
VIH Input High Voltage	IIH ≤500 µA	VDD-.5	-	-	V
HALLX Input					
VIL Input Low Voltage		-	-	1.0	V
VIH Input High Voltage	External pullup current ≤1.7 mA	3.0	-	-	V
Input Pullup-Pulldown Resistance					
Internal pullup resistance	START, FREF	40	-	-	KΩ
Internal pullup resistance	HALLX inputs	5	-	20	KΩ
Internal pulldown resistance	MODE input	40	-	-	KΩ
Input capacitance	All inputs	-	-	25	pF

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
SENSE Input						
SENSE voltage threshold		if exceeded, driver voltage is limited	0.9	1.0	1.1	V
Input current			-100	-	+100	µA
Open Drain Outputs $\overline{LOCK}$, FAULT						
VOL Output Low Voltage		IOL = 2 mA	-	-	0.5	V
Typical external pullup resistor			-	10	-	KΩ
FAULT Indication						
Vlvdt, low voltage			8.0	-	9.5	V
Fmin, loss of FREF			-	-	100	Hz
Stuck motor, start pulses		drivers on, drivers off	-	0.90	-	sec
Number of start pulses			-	4	-	-
Reverse shutdown speed		START = 0	-	281	-	rpm
$\overline{LOCK}$ Indication						
Lock range		FREF = 2 MHz	3594	3600	3607	rpm
Speed error		10.8 < VDD < 13.2	-0.037		+0.037	%
HALL Sensor Interface						
HALLOUT bias voltage		10.8 < VDD < 13.2, Iload = -5 mA	5.0		6.8	V
		10.8 < VDD < 13.2, Iload = -10 mA	5.0			V
Driver Outputs (FHALLX ≥ 100 Hz, Vlvdt < VDD ≤ 13.2, CL ≤ 500 pF unless otherwise specified.)						
Slew rate		All driver outputs	150	-	400	V/msec
OUTX	VOH	Iload = -7.5 mA	3.75	-	-	V
	VOH	Iload = -100 µA, 10.8 ≤ VDD ≤ 13.2	8.0	-	-	V
	VOL off state	Iload = 3.4mA, 5.0 ≤ VDD ≤ 13.2	-	-	0.5	V
OUTUPX	VOL	Iload = 10 mA	-	-	3.0	V
	VOH off state	Iload = -5 mA	VDD-0.5	-	-	V
	VOH off state	Iload = -2 mA, 5.0 ≤ VDD ≤ Vlvdt	VDD-0.5	-	-	V

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APPLICATION INFORMATION

PARAMETER	RECOMMENDED	MIN	NOM	MAX	UNIT
Power Transistors					
Power Darlington Vbe	Typical device: TIP 125, TIP 120	0.8	-	1.8	V
Power FET Vth	Typical device: IRFT 001	2	-	6	V
Power FET Rds (on)		-	-	0.4	Ω
Power FET BVds		30	-	-	V

R1, R2

R1/(R1 + R2)		0.02	0.2	1.0	
R1 + R2		20	50	200	KΩ

$$I\,running = \frac{R1}{R1+R2} \times \frac{VDAC}{Re}$$

Where $VDAC = Kp * \Delta f + Ki * \int \Delta f * \Delta t$

Kp = Proportional constant = .213 V/rad/sec

Ki = Integral constant = 1.33 V/rad

Δf = Frequency error

Motor Parameters

The SSI 32M594 MSC is optimized for use with a wide range of Winchester motors including 3 1/2" motors. Torque Constant Range (KT) of 0.01 to 0.02 Nt - m/A and an Inertia Range (J) from 0.5 to 6.5 x 10^{-4} $Nt - m - sec^2$. The choice of R1, R2 and Re will be affected by motor parameters, so some care in their selection is recommended.

Control Loop Parameters

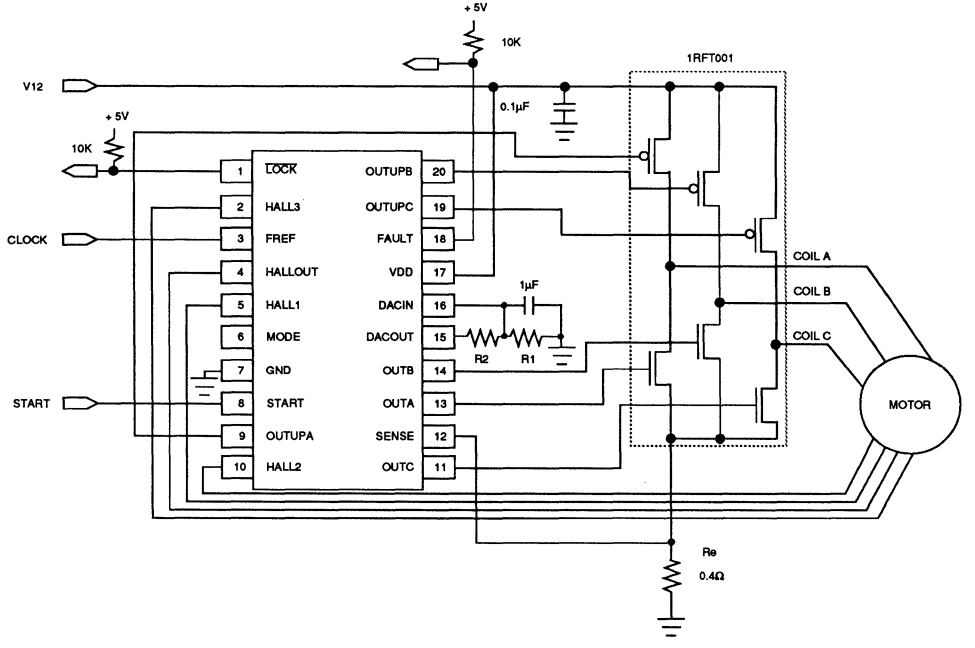
The motor control loop consists of counter, logic, and digital-to-analog converters that provide loop time constants. The continuous time transfer function of the on-chip control can be modeled as follows:

$$H(s) = \frac{Vc(s)}{Fm(s)} = \frac{Ki}{s} + Kp$$

Vc(s) is the voltage applied to the external sense resistor (Re) by the modulator. By adjusting the value of Re, the gain the motor sees can be adjusted as can the starting current.

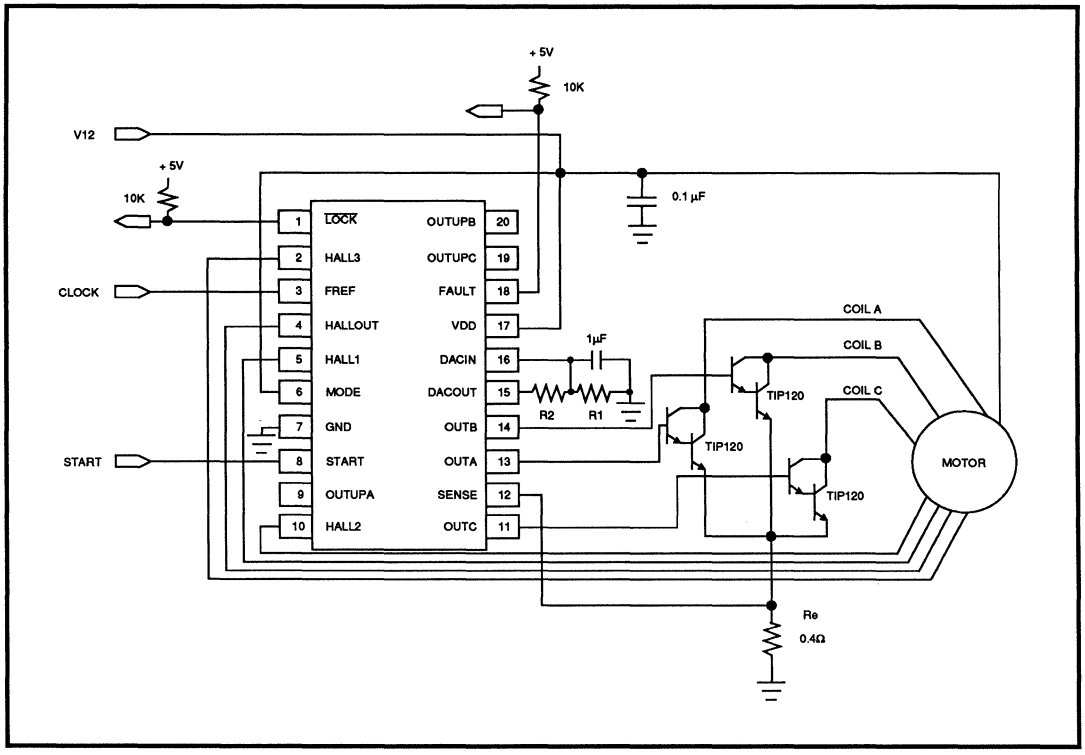
Control Loop Parameters (Continued)

PARAMETER	RECOMMENDED	MIN	NOM	MAX	UNIT
Loop Bandwidth	Nominal motor, Re = 0.4Ω		2		Hz
Loop Zero	Ki/Kp		1.0		Hz
Kp, Proportional Channel Gain		0.198	0.213	0.227	V/rad/s
Ki, Integral Channel Gain		1.23	1.33	1.42	V/rad
Start current		1.0	2.0	3.0	Amps
Running current		0.1	0.2	0.3	Amps



NOTE: In cases where motor coil voltages are noisy with complex transients, stability can be improved by snubber (filter) circuits on each coil. A series RC filter to ground is suggested with the following values: (R = 10Ω, C = 4.7 µF).

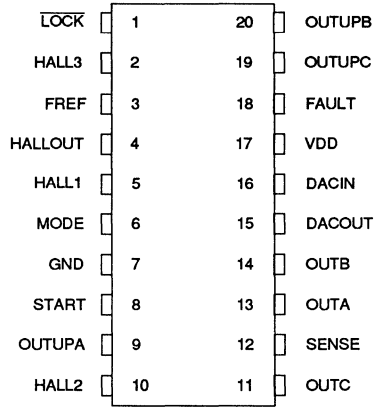
**Typical Three-Phase, 4-Pole, Bipolar,
Non-Center Tapped Motor using a Power FET Module**



**Typical Three-Phase, 8-Pole, Unipolar,
Center Tapped Motor using a Power Darlington.**

PACKAGE PIN DESIGNATIONS
(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.



20-Pin PDIP or SOL

5

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32M594 Three-Phase Delta Motor Speed Controller		
20-Pin SOL	SSI 32M594-CL	SSI 32M594-CL
20-PIN PDIP	SSI 32M594-CP	SSI 32M594-CP

Silicon Systems™
Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

NOTES:

Section

HDD CONTROLLER/ INTERFACE

6

SSI 32B450A
SCSI Controller

silicon systems™
INNOVATORS IN INTEGRATION

August, 1988

DESCRIPTION

The SSI 32B450A is a SCSI bus control IC that handles all arbitration, (re)selection, and data transfer functions for the SCSI bus interface portion of an intelligent peripheral controller or host controller in accordance with ANSI Standard X3.131-1986.

The SSI 32B450A is optimized for use with the SSI 32C452 Storage Controller, the SSI 32C453 Dual-Port Buffer Controller, and an 8-bit multiplexed address/data bus microprocessor such as the 8051 to implement complete SCSI controller functions for high performance data storage devices. Each IC in the set is highly integrated and utilizes a bus oriented design structure that implements high performance and requires minimal board space and software overhead.

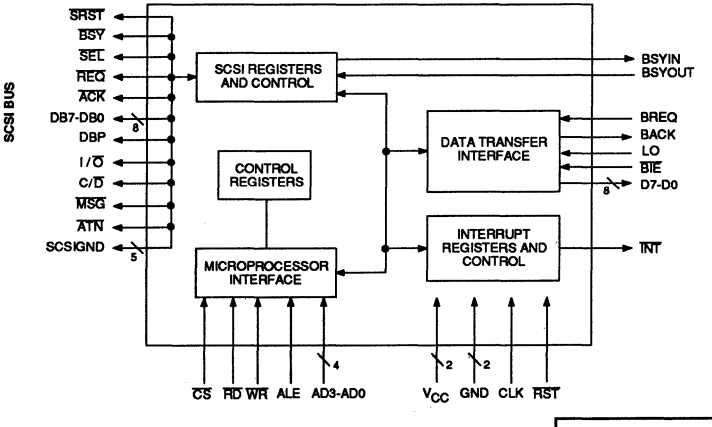
Functionally, the SSI 32B450A performs all SCSI bus control and interface functions and the DMA handshake to work with the buffer controller to ensure efficient data transfer. It supports both target and initiator modes, and carries out SCSI arbitration, (re)selection and data transfer functions without microprocessor intervention. It has eight programmable interrupts which eliminate the need for polling from the microprocessor to detect process completion or error conditions.

FEATURES

- **Single-chip SCSI bus control; no external circuitry required for bus-interface functions**
- **Optimized for use with SSI 32C452 Storage Controller IC and SSI 32C453 Dual-Port Buffer Controller IC**
- **Async SCSI data rate up to 4 Mbytes**
- **Operation conforms to ANSI Standard X3.131–1986**
- **Supports both Target and Initiator modes**
- **Software programmable SCSI ID for all modes**
- **High current drivers / receivers for direct SCSI bus connection**
- **Parity generation and check for SCSI data**
- **High performance, low-power CMOS design; single +5V power supply**
- **Available in 52-pin surface mount PLCC**

6

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

0888

FUNCTIONAL DESCRIPTION

The SSI 32B450A performs all the necessary tasks to control communication with the SCSI bus in both target and initiator roles, without assistance from the microprocessor, according to ANSI Standard X3.131-1986. Because the SSI 32B450A can operate in both the target and initiator roles it is suitable for use in both host and peripheral designs. A basic understanding of the physical and logical characteristics described in the ANSI specification is helpful. For more information refer to the Applications Information section at the end of this data sheet.

When directed the SSI 32B450A will arbitrate for the SCSI bus and (re)select another SCSI device automatically upon successful completion of arbitration. A programmable interrupt signal flags operation completion, arbitration lost, or error conditions so the microprocessor does not have to poll the SCSI Controller. The microprocessor can identify the cause of the interrupt by reading the interrupt status registers. Once a valid SCSI bus connection is made the SSI 32B450A works with the local DMA logic, such as the SSI 32C453 Buffer RAM Controller, without microprocessor intervention, to transfer data efficiently to and from the SCSI bus. The microprocessor controls the operation and obtains status from the SSI 32B450A by accessing the internal registers.

The functional sections of the SSI 32B450A are shown in the Block Diagram.

The **SCSI register and control** section executes the SCSI bus interface operations in accordance with ANSI Standard X3.131-1986. The arbitration and (re)selection operations are initiated by writing to the registers and the status is obtained by reading from them. Once arbitration is initiated by setting the ARB bit in the COMMAND register or asserting the BSYOUT pin, the SSI 32B450A executes the arbitration process and upon winning the SCSI bus proceeds directly into the (re)selection process. Whether it is the selection or reselection process is determined by the state of the ITAR bit in the TRGTID register, which directs whether the SSI 32B450A operates as an initiator or target. The SID2-SID0 (self ID) bits and TID2-TID0 (target ID) bits are automatically converted from binary code as they are written in the SELFID and TRGTID registers, and the proper data bus (DB) signal(s) driven onto the SCSI bus. During arbitration the SSI 32B450A compares the self ID with the other ID's on the bus to discern whether it has won the arbitration. The SSI 32B450A can be programmed to assert the INT (interrupt) line when the processes are complete or an error occurs.

The BSYIN pin indicates to the buffer control logic that the SCSI bus signal BSY is asserted and the bus is currently in use.

Upon being directed to initiate the arbitration phase, the SSI 32B450A checks for bus-free phase (BSY and SEL deasserted continuously for minimum of bus–settle delay and bus-free delay), then asserts the BSY signal and drives the SELFID onto the SCSI bus. After waiting an arbitration delay, it examines the data bus. If a higher SCSI ID is present on the bus, the SSI 32B450A has lost the arbitration. The SSI 32B450A releases the BSY and ID lines and waits for the bus-free phase to reoccur, and then begins the arbitration process again. The continuous arbitration retrying can be stopped by resetting the ARB bit and negating the BSYOUT signal. If arbitration is lost and the LOSE bit in the INTEN0 register is set, the INT line will be asserted and the LOST bit in the INTSTS0 register set. If arbitration is won, the SSI 32B450A asserts SEL. If the WIN bit in the INTEN0 register is set, upon winning arbitration the INT signal will be asserted and the WON bit in the INTSTS0 register will be set.

After a bus-clear plus bus-settle delay time with both BSY and SEL asserted, the arbitration phase is complete and the selection phase begins. The device becomes the initiator by leaving I/O negated, and driving both the self and target ID's onto the SCSI bus. The SSI 32B450A waits two deskew delays, negates BSY, then waits a bus-settle delay before looking for a response from the target. If there are no problems the target responds by asserting BSY within a bus-settle delay. BSY must stay asserted for a minimum of 100 nanoseconds from the end of the bus-settle delay waiting period to be recognized by the SSI 32B450A. There are two waiting periods: selection-abort time and timeout delay, which due to their long length are not monitored by the SSI 32B450A and are left to firmware implementation.

The arbitration and reselection phases occur in the same manner as arbitration and selection with the exception that the device which arbitrated asserts the I/O at the end of arbitration indicating it is a target. The winner (target) then asserts self and target ID's on to

the SCSI bus. When the SSI 32B450A is the target the target ID is located in the SID2-SID0 bits in the SELFID register.

Once arbitration and (re)selection phases are complete the information transfer phases can be entered. The microprocessor maintains the I/O, C/D, and MSG signals to control the interpretation of the commands during the message, command and status phases. These signals are asserted by setting and interrogated by reading the I/O, C/D, or MSG bits in the SCSI1 register. The SSI 32B450A monitors the state of these signals on the SCSI bus and compares them with the expected state from the contents of the SCSI registers (which are controlled by the microprocessor) to check for phase errors. If a difference is detected, a byte of data transferred across the SCSI bus, and the PHERREN bit in the INTEN1 register is set, the INT line will be asserted and the PHERRINT bit in the INTSTS1 register set to indicate that a phase error has occurred. During the message phase, when the SSI 32B450A is the initiator, the ATN signal can be asserted by setting the ATN bit in the SCSI2 register to indicate to the target that it has a message ready to transmit. Once the data transfer phase is entered the SSI 32B450A controls the SCSI bus signals necessary for data transfer.

Selection of the SSI 32B450A as a target by a host: The SSI 32B450A will respond only if RESELN or SELEN bits in CMD register are set. The SSI 32B450A determines that it is selected when SEL and its SCSI ID is asserted and BSY and I/O are deasserted continuously for minimum of bus-settle delay. Once it determines that it is selected the SSI 32B450A will assert BSY. If SLCTEN in INTEN0 register is set, the corresponding INT status bit will be set and INT line will be driven low to indicate a successful selection of the chip via the initiator.

Reselection of the SSI 32B450A as a host by a target: The SSI 32B450A will respond only if RESELN bit in CMD register is set. The SSI 32B450A determines it is reselected when SEL, I/O and SCSI ID are asserted and BSY is continuously free for minimum of bus-settle delay. Once it determines that it is reselected, the SSI 32B450A will assert BSY and deasserts BSY when it detects a deasserted SEL. If SLCTEN in INTEN0 register is set, the corresponding interrupt status bit will be set and INT line will be driven low to indicate successful reselection of the chip via the target. Also, if parity is supported and bad parity is found, or more than two IDs are on the bus, the SSI 32B450A will disregard the reselect attempt by the target.

The SSI 32B450A will assert the SRST signal on to the SCSI bus when the SRST bit in the SCSI2 register is set. The SRST signal is also received by the SSI 450A when it is asserted by another SCSI device on the bus. When it is received by the SSI 32B450A and the SRSTEN bit in the INTEN1 register is set, the INT signal will be asserted upon detection of SRST true and the SRSTINT bit in the INTSTS1 register set. This indicates that an SCSI reset was the cause of the interrupt. The SSI 32B450A will not be affected in any other way by assertion of SRST.

The **data transfer interface** logic coordinates the transfer of data between the data transfer logic and the SCSI bus. Standard two-wire DMA handshaking is supported by the BREQ and BACK signals. This section is organized to connect directly with the SSI 32C453.

The SSI 32B450A is easily connected to any DMA controller such as 8237 through a single PLA such as 16L8 and LS245 bidirectional octal buffer. In such case, the SSI 32B450A will support both initiator and target modes while the PLA and the octal buffer will replace the SSI 32C453.

Before DMA controlled information transfer can begin, a valid connection must exist to the SCSI bus with BSY active and no phase error. The direction of information flow is automatically determined by the SSI 32B450A from the ITAR bit of the TRGTID register and the I/O signal. There are four information flow states, initiator in and out, and target in and out. Initiator or target refers to the mode of the SSI 32B450A, and in or out refers to the direction of data flow with regard to the initiator. Once a valid SCSI bus connection is established, the transfer is initiated by the target and data transfer control logic asserting REQ and BREQ.

In the target-in state, the data is being transferred from the data transfer control logic to the initiator at the initiation of the data transfer control logic and the SSI 32B450A. Once valid data is present on D7-D0, LO is asserted, latching data into the SSI 32B450A. The data transfer control logic asserts BREQ, indicating to the SSI 32B450A that valid data is in the internal

latch ready to be transferred over the SCSI bus. The SSI 32B450A asserts REQ and places the data on the SCSI bus. The initiator asserts ACK indicating acceptance of the data and completion of the SCSI data transfer cycle. The SSI 32B450A asserts BACK to the data transfer control logic indicating completion of that cycle.

The handshaking of BREQ, BACK and LO is automatically controlled via the SSI 32C453. In non SSI 32C453 environment, it can be easily generated and controlled by the PLA and generic DMA controller, i.e. 8237.

In the target-out state data is being transferred from the initiator to the buffer at the initiation of the data transfer control logic and the SSI 32B450A. The data transfer control logic asserts BREQ requesting transfer of a byte of data from the initiator. The SSI 32B450A asserts REQ and the initiator responds by driving the SCSI data bus and asserting ACK which latches data into the SSI 32B450A. BACK is asserted indicating to the data transfer control logic that the byte has been transferred and is ready at the SSI 32B450A. The data transfer control logic then asserts BIE to enable output of the data onto D(7:0). When the data transfer control logic has completed transferring the data it negates BIE and BREQ indicating to the SSI 32B450A that the cycle is complete.

For an initiator-in transfer, data is moved to the SSI 32B450A from the SCSI target selected by the SSI 32B450A. The data is then moved from the SSI 32B450A to the data transfer control logic. The target initiates the transfer by asserting REQ and driving the SCSI data bus. The SSI 32B450A will not respond until it has been alerted to the pending transfer by the assertion of BREQ by the data transfer control logic. This insures the data transfer control logic is available to receive data and is not servicing a higher priority data transfer function such as synchronous transfer from the hard disk. The SSI 32B450A asserts ACK to latch data into the internal latch and tell the target the SCSI transfer is complete. The data transfer control logic then asserts BIE to enable data to the D7-D0 lines. The SSI 32B450A asserts BACK to indicate completion of transfer from the SCSI bus.

An initiator-out transfer moves data from the data transfer control logic, through the SSI 32B450A in the initiator role to the target SCSI device. The transfer is initiated by the target asserting REQ, but the SSI 32B450A must have already set up for the impending transfer by the data transfer control logic. Valid data must be present on D7-D0, and is then latched into the SSI 32B450A by asserting LO, and asserting BREQ to begin the data transfer cycle. The SSI 32B450A then drives the SCSI data bus and waits for two deskew delays and asserts ACK which the target uses to latch the data from the SCSI bus. Upon negation of REQ the SSI 32B450A asserts BACK indicating to the data transfer control logic that the transfer is complete.

A feature of the SSI 32B450A which allows for faster data transfer is that BREQ can be negated before the SSI 32B450A asserts BACK, allowing the data transfer control logic to begin preparing for another transfer cycle without having to wait for the current one to complete. BREQ must have a minimum pulse width of 30 nanoseconds. The SSI 32B450A will not recognize more than one BREQ assertion until it cycles BACK. The SSI 32B450A controls the interface to the SCSI bus so that it is transparent to the rest of the controller allowing other processes to continue.

During the command, status and message phases the ONEXFER bit in the SCSI2 register is provided for transfer of commands to the microprocessor. When it is set, a byte of data is transferred across the SCSI bus. When the transfer is complete the bit is reset. The direction of the data transfer is determined by the state of I/O and the ITAR bit in the TRGTID register. For outgoing transfers, the data transferred is that present in the internal data latch.

Parity is always generated when there is a transfer of data on the SCSI bus. Whether or not a parity error causes an interrupt to occur is controlled by the PERREN bit in the INTEN1 register. The PERREN bit also serves as a mask for the (re)selection process. If the parity interrupt is enabled, and bad parity occurs during the (re)selection procedure, the SSI 32B450A will not be (re)selected. If parity interrupt is disabled, the SSI 32B450A will be (re)selected regardless of the parity state. A phase error can be detected during a data transfer phase. Phase error detection is enabled by setting the PHERREN bit in the INTEN1 register, and causes the INT signal to be asserted and the PHERRINT bit in the INTSTS1 register to be set.

The **control registers** allow programmable control of the prescaling factor for the internal clock and soft reset of the SSI 32B450A. The internal clock synchronizes

internal functions such as SCSI bus control signals and data transfer, and clocks the state machines which control these functions. The prescaling factor allows use of available clocks to create the necessary internal clock rate of 3.34 to 5.0 MHz. For maximum speed of operation of the SCSI bus, a 5.0 MHz clock is required. A write to the RESET register causes the SSI 32B450A to be reset as though the RST pin were asserted. The details of the effects on the registers are described in the Register Description section of this data sheet.

The **interrupt registers and control** section controls the INT output and allows the microprocessor to obtain status once an interrupt has occurred. The INT signal can be programmed to be asserted for any of eight reasons by setting the appropriate bit in the INTEN0 or INTEN1 registers. These are winning or losing arbitration, (re)selection complete and (re)selected complete, loss of BSY (SCSI busy) true, a phase or parity error, and/or assertion of SRST (SCSI reset) signal on the SCSI bus. By not setting any of the bits the INT signal may be masked out completely. Once the INT signal has been asserted, the microprocessor can determine the cause(s) of the interrupt by reading from the INTSTS0 and INTSTS1 registers.

The **microprocessor interface** section decodes microprocessor read and write requests and provides access to all the registers. Since both data and address are carried on the multiplexed address/data lines, AD3-AD0, address information is latched from the bus on the falling edge of the ALE (address latch enable) input. When CS (chip select) is asserted with either RD (read) or WR (write), the register whose address was previously latched is selected and data moved as directed by the RD and WR signals.

PIN DESCRIPTION

NAME	NUMBER	TYPE	DESCRIPTION
GENERAL			
VCC	23,44		POWER SUPPLY - +5 volts
GND	29,41		GROUND - Device system ground.
$\overline{RST}$	39	I	RESET - This signal is active low.When asserted the SSI 32B450A goes to an idle mode and the contents of some registers are reset. In the idle mode no activity will take place until further inputs are given. See Register Description for exact details.
CLK	40	I	MASTER CLOCK - Synchronous internal functions are controlled by this signal. It is prescaled by the value in the CLKPRSC register.
SCSI BUS SIGNALS			
All signals connecting to the SCSI bus are designed to have a controlled rise and fall time to minimize the noise injected into the system.			
SGND	3,8,13, 9,49		SCSI GROUND - These are the ground signals for the SCSI bus interface. These pins should be connected to a good system ground, capable of handling the large transient and static SCSI bus current levels.
DB0-DB7	1,2,4-7, 51,52	I/O	SCSI DATA BUS - Buffered data bus signals to interface to the SCSI bus. Schmidt trigger input and high current open drain drivers allow direct connection to the SCSI bus.

SCSI BUS SIGNALS (Continued)

NAME	NUMBER	TYPE	DESCRIPTION
DBP	50	O	DATA BUS PARITY - Parity bit for the SCSI DATA BUS signals. This signal has the same electrical attributes as the DB0-DB7 signals. It is always generated when data is transferred on the SCSI bus. It can be ignored on reception of data from the SCSI bus by resetting the PERREN bit in the INTEN1 register.
$\overline{SRST}$	12	I/O	SCSI RESET - This signal can be asserted by any of the SCSI devices on the bus. When it is an input, and the SRSTEN bit in the INTEN1 register is set, the $\overline{INT}$ signal will be asserted upon detection of an asserted $\overline{SRST}$ signal on the SCSI bus. This causes the SRSTINT bit in the INTSTS1 register to be set by the SSI 32B450A, indicating to the microprocessor that the $\overline{INT}$ assertion was caused by the $\overline{SRST}$ signal being asserted. As an output it is asserted by setting the SRST bit in the SCSI1 register.
$\overline{BSY}$	10	I/O	BUSY - An active low signal which indicates that the SCSI bus is being used. It can be asserted by any of the devices on the SCSI bus. As an output it can be asserted by setting the BUSY bit in the SCSI0 register, or in the course of executing the SCSI bus control routines internal to the SSI 32B450A.
$\overline{SEL}$	15	I/O	SELECT - An active low signal which is asserted by the SSI 32B450A to (re)select a target (initiator).
$\overline{REQ}$	17	I/O	REQUEST - An active low signal. When the SSI 32B450A is the initiator it is an input which indicates that the target is requesting transfer of a byte of data on the bus. When the SSI 32B450A is the target the signal is an output which requests the initiator to transfer a byte of data over the bus. The status of $\overline{REQ}$ can be read in REQ bit in SCSI0.
$\overline{ACK}$	11	I/O	ACKNOWLEDGE - An active low signal. When the SSI 32B450A is the initiator the signal is an output which is asserted in response to the $\overline{REQ}$ input signal, indicates that there is valid data on the bus, and completes the handshaking for asynchronous data transfer. When the SSI 32B450A is the target, this signal is an input from the initiator in response to the SSI 32B450A's $\overline{REQ}$, and indicates valid data on the SCSI bus. The status on $\overline{ACK}$ can be read in ACK bit in SCSI0.

SCSI BUS SIGNALS (Continued)

NAME	NUMBER	TYPE	DESCRIPTION
I/$\overline{O}$	18	I/O	INPUT/$\overline{OUTPUT}$ - This signal controls the direction of the data transfer across the SCSI bus relative to the initiator. When it is asserted it indicates that data is being input to the initiator. When it is not asserted it indicates that data is being output from the initiator. This signal is only driven when the SSI 32B450A is in the target role. During reselection of an initiator by the SSI 32B450A this line will be driven low.
C/$\overline{D}$	16	I/O	CONTROL/$\overline{DATA}$ - This signal is driven when in the target mode to indicate whether control or data information is on the DB0 - DB7, and DBP lines. When the signal is asserted, control information is on the bus, and when it is inactive, it indicates that data is on the bus.
$\overline{MSG}$	14	I/O	$\overline{MESSAGE}$ - An active low signal. When the SSI 32B450A is in the target mode, it is asserted to indicate that the SCSI communication is in the message portion of the information transfer phase.
$\overline{ATN}$	9	I/O	$\overline{ATTENTION}$ - An active low signal. When the SSI 32B450A is in the initiator mode, this signal is an output which indicates that a message is ready to be transmitted.
BSYIN	34	O	BUSY IN - Reflects the state of the $\overline{BSY}$ signal from the SCSI bus.
BSYOUT	35	I	BUSY OUT - When asserted this signal causes the SSI 32B450A to initiate arbitration for the SCSI bus. Asserting this signal affects the SSI 32B450A in the same way as setting the ARB bit in the COMMAND register. The ARB bit will not be set by assertion of this signal.

DATA TRANSFER INTERFACE

BREQ	30	I	DATA TRANSFER REQUEST - When asserted, this signal indicates that the peripheral device data transfer control logic is requesting to transfer of a byte of data, and causes the SSI 32B450A to cycle for a transfer of data.
BACK	31	O	DATA TRANSFER ACKNOWLEDGE - When asserted indicates that the transfer of data is complete.
LO	32	I	LATCH OUTPUT - Latches data into the SSI 32B450A. It is named LATCH OUTPUT because it is latching data out onto the SCSI bus. It is valid only when data is going out to the SCSI bus, the target-in and initiator-out modes.

DATA TRANSFER INTERFACE (Continued)

NAME	NUMBER	TYPE	DESCRIPTION
$\overline{BIE}$	33	I	BUS INPUT ENABLE - This signal is active low. It is a strobe from the data transfer control logic which indicates it is transferring data from the SCSI bus to the peripheral device or local buffer. It enables the output drivers for D7-D0 of the SSI 32B450A so that data present in the internal latch is output.
D0-D7	20-22 24-28	I/O	DATA BUS - Data bus for transfer of data on local (usually peripheral controller and buffer) bus.

INTERRUPT CONTROL

$\overline{INT}$	36	O	INTERRUPT - This is an open drain, active low signal. When asserted it indicates that an interrupt condition has occurred as defined in the INT0EN and INT1EN registers. The status of the interrupt can be read from the INT0STS and INT1STS registers. The signal is negated when interrupt status is read.

MICROPROCESSOR INTERFACE

$\overline{CS}$	37	I	CHIP SELECT - This is an active low signal. When asserted it indicates that the microprocessor is selecting the device and it is enabled to respond to the microprocessor.
$\overline{RD}$	42	I	READ - This signal is active low. When asserted it indicates that the microprocessor wants to read from the device. The AD0-AD3 signals become an output. This signal is gated internally with $\overline{CS}$.
$\overline{WR}$	43	I	WRITE - This signal is active low. When asserted it indicates that the microprocessor wants to write to the device. The AD0-AD3 signals are written to the register pointed to by the address register. This signal is gated internally with $\overline{CS}$.
AD0-AD3	45-48	I/O	ADDRESS and DATA BUS - Bus which carries device register address information and bi-directional data. Whether it is carrying address or data is governed by the state of ALE.
ALE	38	I	ADDRESS LATCH ENABLE - The falling edge of this signal latches the register address form the AD0-AD3 pins into the internal address latch.

REGISTER DESCRIPTIONS

The SSI 32B450A has twelve four-bit registers which control the device and provide status for the microprocessor. They are broken into three functional groups; SCSI control, interrupt control, and general control. Register bits which are Read only are unaffected during writing.

REGISTER	ADDRESS	D3	D2	D1	D0	ACCESS
SELFID	0H	0	SID2	SID1	SID0	R/W
TRGTID	1H	ITAR	TID2	TID1	TID0	R/W
COMMAND	2H	RESELEN	SELEN	ARB	unused	R/W
INTEN0	4H	WIN	LOSE	SLCTEN	ENDSLEN	R/W
INTSTS0	5H	WON	LOST	SELED	ENDSEL	R
INTEN1	6H	LSBSYEN	PHERREN	SRSTEN	PERREN	R/W
INTSTS1	7H	LSBSYINT	PHERRINT	SRSTINT	PERRINT	R
SCSI0	8H	REQ	ACK	BSY	SEL	R/W
SCSI1	9H	SRST	I/O	C/D	MSG	R/W
SCSI2	AH	ONEXFER	reserved	ATNEN	ATN	R/W
CLKPRSC	EH	X	PRSC2	PRSC1	PRSC0	W
RESET	FH	X	X	X	X	W

SSI 32B450A REGISTER BIT MAP

REGISTER DESCRIPTIONS

SCSI BUS CONTROL AND STATUS REGISTERS - BIT DESCRIPTION

SELFID **0H** **READ/WRITE**

Self ID number - Contains the binary equivalent of its own SCSI ID.

BIT	NAME	DESCRIPTION
3	reserved	Must always be written as reset, always reads as reset.
2-0	SID2-SID0	SELF ID - Binary equivalent of device's SCSI ID. SID2 is the most significant bit.

The SELFID register is not affected by assertion of $\overline{RST}$.

TRGTID **1H** **READ/WRITE**

Target ID number - Contains the binary equivalent of the connecting SCSI device's ID in TID2-TID0.

BIT	NAME	DESCRIPTION
3	ITAR	INITIATOR/TARGET ROLE - When set indicates the device is in the initiator role and will select the target defined by the TID after arbitration has been won. When reset indicates the device is in the target role and will reselect an initiator defined by TID. This bit must be defined prior to beginning arbitration. When the device is selected by another SCSI device this bit is cleared and when reselected it is set.
2-0	TID2-TID0	TARGET ID NUMBER - These bits are the binary equivalent of the connecting device's SCSI ID. TID2 is the most significant bit.

The TRGTID register is not affected by assertion of $\overline{RST}$.

SCSI BUS CONTROL AND STATUS REGISTERS - BIT DESCRIPTION (Continued)

COMMAND 2H READ/WRITE

Command - Controls whether the SSI 32B450A will respond to selection, reselection, and initiation of arbitration.

BIT	NAME	DESCRIPTION
3	RESELEN	RESELECT ENABLE - When set, the SSI 32B450A will respond to a reselect or select request from another SCSI device.
2	SELEN	SELECT ENABLE - When set, the SSI 32B450A will only respond to a select request from another SCSI device.
1	ARB	ARBITRATE - When set, causes the SSI 32B450A to begin arbitration for the SCSI bus (re)select a target (initiator).
0	unused	Read only, always set.

The COMMAND register is reset (except bit 0) on assertion of $\overline{RST}$.

SCSI0 8H READ/WRITE

SCSI 0 - SCSI control and status register 0.

BIT	NAME	DESCRIPTION
3	REQ	REQUEST - This read only bit reflects the state of the $\overline{REQ}$ pin.
2	ACK	ACKNOWLEDGE - This read only bit reflects the state of the $\overline{ACK}$ pin.
1	BSY	BUSY - The $\overline{BSY}$ signal is asserted when this bit is set and negated when it is reset. When this register is read, this bit reflects the state of the $\overline{BSY}$ pin.
0	SEL	SELECT - This read only pin reflects the state of the $\overline{SEL}$ pin.

The BSY bit of the SCSI0 register is reset on assertion of $\overline{RST}$. All other bits remain unaffected.

SCSI BUS CONTROL AND STATUS REGISTERS - BIT DESCRIPTION (Continued)

SCSI1 **9H** **READ/WRITE**

SCSI 1 - SCSI control and status register 1.		
BIT	**NAME**	**DESCRIPTION**
3	SRST	SCSI RESET - The $\overline{SRST}$ signal is asserted when this bit is set and negated when this bit is reset. When this register is read, this bit reflects the state of the $\overline{SRST}$ pin.
2	I/$\overline{O}$	INPUT/$\overline{OUTPUT}$ - The I/$\overline{O}$ signal is asserted when this bit is set, the ITAR bit of the TRGTID register is reset, and the $\overline{BSY}$ signal is asserted. It is negated when this bit is reset. when this register is read, this bit reflects the state of the I/$\overline{O}$ pin.
1	C/$\overline{D}$	CONTROL/$\overline{DATA}$ - The C/$\overline{D}$ signal is asserted when this bit is set, the ITAR bit in the TRGTID register is reset, and the $\overline{BSY}$ signal is asserted. It is negated when this bit is reset. When this register is read, this bit reflects the state of the C/$\overline{D}$ pin.
0	MSG	MESSAGE - The $\overline{MSG}$ signal is asserted when this bit is set, the ITAR bit in the TRGTID register is reset and the $\overline{BSY}$ signal is asserted. It is negated when this bit is reset. When this register is read, this bit reflects the state of the $\overline{MSG}$ pin.
The SCSI1 register is reset on assertion of $\overline{RST}$.		

SCSI2 **AH** **READ/WRITE**

SCSI 2 - SCSI control and status register 2.		
BIT	**NAME**	**DESCRIPTION**
3	ONEXFER	ONE TRANSFER, R/W - When set a byte of information is transferred from the internal data latch across the SCSI bus. Upon completion of the transfer the bit will automatically be reset, and therefore reflects the status of the data transfer.
2	reserved	Must always be written as reset, always reads as reset.
1	ATNEN	$\overline{ATN}$ ENABLE, R/W - When set it enables the $\overline{ATN}$ signal to be asserted by the SSI 32B450A at the end of arbitration plus the bus settle and clear delay times when it is reselecting the initiator. The ATN bit (SCSI2 bit 0) is set when selecting a target and ATNEN bit is set.
0	ATN	ATTENTION - The $\overline{ATN}$ signal is asserted when this bit is set and negated when it is reset. When this register is read it reflects the state of the $\overline{ATN}$ pin.
The SCSI2 register is reset on assertion of the $\overline{SRST}$.		

INTERRUPT CONTROL AND STATUS REGISTERS - BIT DESCRIPTION

INTEN0 **4H** **READ/WRITE**

Interrupt Enable 0 - Controls interrupt mode enable.

BIT	NAME	DESCRIPTION
3	WIN	WIN ENABLE - When set enables the $\overline{INT}$ signal to be asserted when SCSI arbitration is won.
2	LOSE	LOSE ENABLE - When set enables the $\overline{INT}$ signal to be asserted when SCSI arbitration is lost.
1	SLCTEN	SELECTED ENABLE - When set enables the $\overline{INT}$ signal to be asserted when the SSI 32B450A has been selected or reselected by another SCSI device.
0	ENDSLEN	END SELECT ENABLE - When set enables the $\overline{INT}$ signal to be asserted at the end of the SSI 32B450A's selection process. This indicates that the SCSI device being (re)selected has responded properly.

The INTEN0 register is reset on assertion of $\overline{RST}$.

INTSTS0 **5H** **READ ONLY**

Interrupt status 0 - Provides information on cause of assertion of $\overline{INT}$ signal.

BIT	NAME	DESCRIPTION
3	WON	WON ARBITRATION - The SSI 32B450A has won arbitration and $\overline{SEL}$ is not active on the SCSI bus at the end of the arbitration phase. Indicates that no higher priority SCSI device was arbitrating for the SCSI bus.
2	LOST	LOST ARBITRATION - The SSI 32B450A has lost arbitration. This means that a device with a higher ID is on the bus or that $\overline{SEL}$ is (has become) active during arbitration time.
1	SELED	SELECTED - The SSI 32B450A has been (re)selected by another SCSI device. The ID of the other device is in the TRGTID register.
0	ENDSEL	END SELECT - The SSI 32B450A has completed (re)connection to the SCSI target (initiator) device with ID in the TRGTID register.

The INTSTS0 register is reset on assertion of $\overline{RST}$ or on read of this register.

INTERRUPT CONTROL AND STATUS REGISTERS - BIT DESCRIPTION (Continued)

INTEN1 **6H** **READ/WRITE**

Interrupt enable 1 - Controls interrupt mode enable.

BIT	NAME	DESCRIPTION
3	LSBSYEN	LOST BUSY ENABLE - When set enables the INT signal to be asserted when the $\overline{BSY}$ signal on the SCSI bus has been negated.
2	PHERREN	PHASE ERROR ENABLE - When set enables the $\overline{INT}$ signal to be asserted when a phase error has been detected by the SSI 32B450A during an information or data transfer phase.
1	SRSTEN	SCSI RESET ENABLE - When set enables the $\overline{INT}$ signal to be asserted when the $\overline{SRST}$ signal has been asserted on the SCSI bus.
0	PERREN	PARITY ERROR ENABLE - When set enables the $\overline{INT}$ signal to be asserted when a parity error is detected by the SSI 32B450A parity check circuitry.

The INTEN1 register is reset on assertion of $\overline{RST}$.

INTSTS1 **7H** **READ ONLY**

Interrupt Status 1 - Provides information on cause of assertion of $\overline{INT}$ signal.

BIT	NAME	DESCRIPTION
3	LSBSYINT	LOST BUSY - The $\overline{BSY}$ signal on the SCSI bus is no longer active.
2	PHERRINT	PHASE ERROR - A phase error was detected by the SSI 32B450A during the information or data transfer phase.
1	SRSTINT	SCSI RESET - The $\overline{SRST}$ signal is active on the SCSI bus.
0	PERRINT	PARITY ERROR - A parity error occurred during information or data transfer phase.

The INTSTS1 register is reset on assertion of $\overline{RST}$, or on Read of this register.

GENERAL CONTROL REGISTERS

CLKPRSC **EH** **WRITE ONLY**

CLOCK PRESCALE - Value to prescale the internal clock from the CLK input.

BIT	NAME	DESCRIPTION
3	x	don't care
2	PRSC2	CLOCK PRESCALE 2
1	PRSC1	CLOCK PRESCALE 1
0	PRSC0	CLOCK PRESCALE 0 - Clock input frequency is divided as follows:

PRSC2	PRSC1	PRSC0	DIVISOR
0	0	0	1
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

The CLKPRSC register is not affected by $\overline{RST}$.

RESET **FH** **WRITE ONLY**

RESET - Software reset for the device.

BIT	NAME	DESCRIPTION
3-0	x	Don't care - A write to this register of any value will cause a software reset to occur in the same way as asserting the $\overline{RST}$ pin.

Register locations 3H, BH, CH, and DH are reserved for future definition.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Ambient Temperature Under Bias	0 to 70	° C
Storage Temperature	-65 to 150	° C
Voltage With Respect to Ground - SCSI Bus Signals	-0.5 to 10.0	V
Voltage With Respect to Ground - All Other Pins	-0.5 to 7.0	V
Maximum Current Injection	± 20	mA

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
VCC Supply Voltage		4.75	5.00	5.25	V
TA Operating Free Air Temperature		0		70	° C

D.C. CHARACTERISTICS

TA = 0 °C to 70 °C; VCC = +5V ±5% Recommended operating range unless otherwise specified.

SCSI BUS SIGNALS

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNIT
VIH	Input High Voltage		1.5		2.0	V
VIL	Input Low Voltage		0.8		1.3	V
IIH	Input High Current	VIN = 5.0 V	-50		+50	µA
IIL	Input Low Current	VIN = 0.5 V	-50		+50	µA
VOL	Output Low Voltage	IOL = 48.0 mA			0.5	V
IOL	Output Low Current	VOL = 0.5 V	48.0			mA
H	Hysterisis	VCC = 5.0V Ta = 25°C		0.4		V
Power Dissipation					0.600	mW

DATA BUS SIGNALS: D7 - D0

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNIT
VIH	Input High Voltage		1.5		2.0	V
VIL	Input Low Voltage		0.8		1.3	V
H	Hysterisis		0.4			V
IIH	Input High Current	Vin = 2.4 V	-20		+20	µA
IIL	Input Low Current	Vin = 0.5 V	-20		+20	µA
VOL	Output Low Voltage	IOL = 8.0 mA			0.5	V
IOL	Output Low Current	VOL = 0.5 V	4.0			mA
VOH	Output High Voltage	IOH = -4.0 mA	2.4			V
IOH	Output High Current		-4.0			mA

ALL OTHER SIGNALS

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNIT
VIH	Input High Voltage		2.0			V
VIL	Input Low Voltage				0.6	V
IIH	Input High Current	Vin = 2.4 V	-20		+20	µA
IIL	Input Low Current	Vin = 0.5 V	-20		+20	µA
VOL	Output Low Voltage	IOL = 2.0 mA			0.5	V
IOL	Output Low Current	VOL = 0.5 V	2.0			mA
VOH	Output High Voltage	IOH = -500 µA	2.4			V
IOH	Output High Current				-500	µA

ELECTRICAL SPECIFICATIONS (Continued)

CLOCK (CLK) TIMING (See Figure 1)

PARAMETERS	MIN	NOM	MAX	UNIT
T_{ICLK} ICLK width	200		340	ns
$T_{ICLK/2}$ ICLK half-cycle	100		170	ns
NOTE: ICLK (internal clock) is the signal internal to the SSI 32B450A based on the CLK input. It will have a 50% duty cycle if the prescale factor programmed in the CLKPRSC register is greater than one.				

DATA TRANSFER INTERFACE TIMING - INITIATOR IN (See Figure 2)

PARAMETERS	MIN	NOM	MAX	UNIT
T_{ARH} $\overline{ACK}\downarrow$ to $\overline{REQ}\uparrow$	0			ns
T_{RAS} $\overline{REQ}\downarrow$ to $\overline{ACK}\downarrow$ ①	5		80	ns
T_{RAH} $\overline{REQ}\uparrow$ to $\overline{ACK}\uparrow$	5		100	ns
T_{BRA} $\overline{BREQ}\uparrow$ to $\overline{ACK}\downarrow$ ①	5		80	ns
T_{ADBH} $\overline{ACK}\downarrow$ to DB7-DB0, DBP invalid	30			ns
T_{DBR} DB7-DB0, DBP valid to $\overline{REQ}\downarrow$	0			ns
T_{BIDS} $\overline{BIE}\downarrow$ to D7-DO valid			35	ns
T_{BIDH} $\overline{BIE}\uparrow$ to D7-DO invalid	30			ns
T_{RBI} $\overline{REQ}\downarrow$ to $\overline{BIE}\downarrow$	40			ns
T_{BIW} $\overline{BIE}$ width	60			ns
T_{BRW} BREQ width	30			ns
T_{RBA} $\overline{REQ}\downarrow$ to BACK $\uparrow$ ②			60	ns
T_{BRBA} BREQ $\uparrow$ to BACK $\uparrow$ ②			70	ns
T_{RBAH} $\overline{REQ}\uparrow$ to BACK $\downarrow$ ③			60	ns

ELECTRICAL SPECIFICATIONS (Continued)

DATA TRANSFER INTERFACE TIMING - INITIATOR IN (Continued)

PARAMETERS	MIN	NOM	MAX	UNIT
T_{BRBAH} BREQ ↓ to BACK ↓ ③			45	ns
T_{BRI} BREQ ↑ to $\overline{INT}$ ↓			80	ns
T_{RI} $\overline{REQ}$ ↓ to $\overline{INT}$ ↓			70	ns
① NOTE: $\overline{ACK}$ ↓ is triggered by $\overline{REQ}$ ↓ or BREQ ↑ whichever occurs later.				
② NOTE: BACK ↑ is triggered by $\overline{REQ}$ ↓ or BREQ ↑ whichever occurs later.				
③ NOTE: BACK ↓ is triggered by $\overline{REQ}$ ↑ or BREQ ↓ whichever occurs later.				

DATA TRANSFER INTERFACE TIMING - INITIATOR OUT (See Figure 3)

PARAMETERS	MIN	NOM	MAX	UNIT
T_{LOW} LO width	30			ns
T_{DS} D7-DO valid to LO ↓	20			ns
T_{DH} LO ↓ to D7-DO invalid	20			ns
T_{LBR} LO ↓ to BREQ ↑	5			ns
T_{BRBAH} BREQ ↓ to BACK ↓ ①			45	ns
T_{RBAH} $\overline{REQ}$ ↑ to BACK ↓ ①			60	ns
T_{BRW} BREQ width	30			ns
T_{BRBAS} BREQ ↑ to BACK ↑ ②			80	ns
T_{RBA} $\overline{REQ}$ ↓ to BACK ↑ ②			70	ns
T_{RDB} $\overline{REQ}$ ↓ to DB7-DBO, DBP valid ③	5		80	ns
T_{BRDB} BREQ ↑ to DB7-DB0, DBP valid ③	5		80	ns

ELECTRICAL SPECIFICATIONS (Continued)

DATA TRANSFER INTERFACE TIMING - INITIATOR OUT (Continued)

PARAMETERS	MIN	NOM	MAX	UNIT
T_{RAS} $\overline{REQ}$ ↓ to $\overline{ACK}$ ↓ ④	$\frac{T_{ICLK}}{2}+5$		$T_{ICLK}+80$	ns
T_{BRA} BREQ ↑ to $\overline{ACK}$ ↓ ④	$\frac{T_{ICLK}}{2}+5$		$T_{ICLK}+80$	ns
T_{DBAS} DB7-DB0, DBP valid to $\overline{ACK}$ ↓	55			ns
T_{ARH} $\overline{ACK}$ ↓ to $\overline{REQ}$ ↑	0			ns
T_{RAH} $\overline{REQ}$ ↑ to $\overline{ACK}$ ↑	5		100	ns
T_{RDBH} $\overline{REQ}$ ↑ to DB7-DB0, DBP invalid	5		50	ns

① NOTE: BACK ↓ is triggered by BREQ ↓ or $\overline{REQ}$ ↑ whichever occurs later.

② NOTE: BACK ↑ is triggered by BREQ ↑ or $\overline{REQ}$ ↓ whichever occurs later.

③ NOTE: DB7-DB0, DBP valid are triggered by $\overline{REQ}$ ↓ or BREQ ↑ whichever occurs later.

④ NOTE: $\overline{ACK}$ ↓ is triggered by BREQ ↑ or $\overline{REQ}$ ↓ whichever occurs later.

DATA TRANSFER INTERFACE TIMING - TARGET IN (See Figure 4)

PARAMETERS	MIN	NOM	MAX	UNIT
T_{LOW} LO width	30			ns
T_{DS} D7-DO valid to LO ↓	20			ns
T_{DH} LO ↓ to D7-D0 invalid	20			ns
T_{LBR} LO ↓ to BREQ ↑	0			ns
T_{BRW} BREQ width	30			ns
T_{BRR} BREQ ↑ to $\overline{REQ}$ ↓	$\frac{T_{ICLK}}{2}+5$		$T_{ICLK}+80$	ns

ELECTRICAL SPECIFICATIONS (Continued)

DATA TRANSFER INTERFACE TIMING - TARGET IN (Continued)

PARAMETERS	MIN	NOM	MAX	UNIT
T_{BRDB} BREQ ↑ to DB7-DBO, DBP valid	5		80	ns
T_{DBR} DB7-DB0, DBP valid to $\overline{REQ}$ ↓	55			ns
T_{RAS} $\overline{REQ}$ ↓ to $\overline{ACK}$ ↓	0			ns
T_{BRBAH} BREQ ↓ to BACK ↓ ①			45	ns
T_{ABAH} $\overline{ACK}$ ↑ to BACK ↓ ①			60	ns
T_{ABAS} $\overline{ACK}$ ↓ to BACK ↑	5		60	ns
T_{ARH} $\overline{ACK}$ ↓ to $_{REQ}$ ↑	5		50	ns
T_{AW} $\overline{ACK}$ width	20			ns
T_{RAH} $\overline{REQ}$ ↑ to ACK ↑	0			ns
T_{ADBH} $\overline{ACK}$ ↑ to DB7-DB0, DBP invalid	5		50	ns
T_{ALO} $\overline{ACK}$ ↑ to LO ↑	0			ns
① NOTE: BACK ↓ is triggered by BREQ ↓ or $\overline{ACK}$ ↑ whichever occurs later.				

DATA TRANSFER INTERFACE TIMING - TARGET OUT (See Figure 5)

PARAMETERS	MIN	NOM	MAX	UNIT
T_{BRW} BREQ width	30			ns
T_{BRR} BREQ ↑ to $\overline{REQ}$ ↓	5		80	ns
T_{RAS} $\overline{REQ}$ ↓ to $\overline{ACK}$ ↓	0			ns
T_{ABA} $\overline{ACK}$ ↓ to BACK ↑	5		60	ns
T_{ABI} $\overline{ACK}$ ↓ to $\overline{BIE}$ ↓	40			ns

ELECTRICAL SPECIFICATIONS (Continued)

DATA TRANSFER INTERFACE TIMING - TARGET OUT (Continued)

PARAMETERS	MIN	NOM	MAX	UNIT
T_{AW} $\overline{ACK}$ width	20			ns
T_{DBAS} DB7-DB0, DBP valid to $\overline{ACK}$ ↓, set-up	0			ns
T_{ADBH} $\overline{ACK}$ ↓ to DB7-DB0, DBP invalid, hold	30			ns
T_{AI} $\overline{ACK}$ ↓ to $\overline{INT}$ ↓			70	ns
T_{ARS} $\overline{ACK}$ ↓ to $\overline{REQ}$ ↑	5		50	ns
T_{RAH} $\overline{REQ}$ ↑ to $\overline{ACK}$ ↑	0			ns
T_{BID} $\overline{BIE}$ ↓ to D7-D0 valid	30			ns
T_{BIDH} $\overline{BIE}$ ↑ to D7-D0 invalid	30			ns
T_{BIW} $\overline{BIE}$ width	60			ns
T_{ABAH} $\overline{ACK}$ ↑ to BACK ↓ ①			60	ns
T_{BRBA} BREQ to BACK ↓ ①			45	ns
T_{BIBR} $\overline{BIE}$ to BREQ ↑ ②	0			ns
T_{BABR} BACK ↓ to BREQ ↑ ②	15			ns

BSYIN AND BSYOUT TIMING (See Figures 6 & 7)

PARAMETERS	MIN	NOM	MAX	UNIT
T_{BNW} $\overline{BSY}$ invalid width	6 x T_{ICLK}		(7 x T_{ICLK}) + 100	µs
T_{BBS} $\overline{BSY}$ change to BSYIN change	0		100	ns
T_{SNW} $\overline{SEL}$ invalid before arbitration delay	6 x T_{ICLK}		(7 x T_{ICLK}) + 100	µs

ELECTRICAL SPECIFICATIONS (Continued)

BSYIN AND BSYOUT TIMING (Continued)

PARAMETERS	MIN	NOM	MAX	UNIT
T_{AD} arbitration delay	4 x T_{ICLK}		(5 x T_{ICLK}) + 100	µs
T_{BOS} BSYOUT to end of arbitration delay	100			ns

MICROPROCESSOR INTERFACE TIMING (See Figure 8)

PARAMETERS	MIN	NOM	MAX	UNIT
T_A ALE width	45			ns
T_{CA} $\overline{CS}$ ↓ to ALE ↓	7.5			ns
T_{AR} ALE ↓ to $\overline{RD}$ ↓	25			
T_R $\overline{RD}$ width	125			ns
T_{AS} AD3-AD0 valid to ALE ↓	7.5			ns
T_{AH} ALE ↓ to AD3-ADO invalid	20			ns
T_{RDS} $\overline{RD}$ ↓ to AD3-ADO valid			65	ns
T_{RDH} $\overline{RD}$ ↑ to AD3-ADO invalid			50	ns
T_{WDS} AD3-AD0 valid to $\overline{WR}$ ↑	40			ns
T_{WDH} $\overline{WR}$ ↑ to AD3 to AD0 invalid	10			ns
T_W $\overline{WR}$ width	125			ns
T_{IR} $\overline{RD}$ ↓ to $\overline{INT}$ ↑			65	ns
T_{RC} $\overline{RD}$ ↑ to $\overline{CS}$ ↑	0			ns
(T_{WC}) ① $\overline{WR}$ ↑ to $\overline{CS}$ ↑	0			ns
T_{AP} ALE period	250			ns

① NOTE: not shown in timing diagram

ELECTRICAL SPECIFICATIONS (Continued)

ARBITRATION AND (RE)SELECTION TIMING - SSI 32B450A INITIATED (See Figure 9)

PARAMETERS	MIN	NOM	MAX	UNIT
T_{BOB} BSYOUT ↑ to $\overline{BSY}$ ↓ ①	0		100	ns
T_{BNW} $\overline{BSY}$ invalid width ①	6 x T_{ICLK}		(7 x T_{ICLK}) +100	ns
T_{SNW} $\overline{SEL}$ invalid width	6 x T_{ICLK}		(7 x T_{ICLK}) +100	ns
T_{BS} $\overline{BSY}$ ↓ to $\overline{SEL}$ ↓	11 x T_{ICLK}		(12 x T_{ICLK}) +100	ns
T_{BOID} BSYOUT ↑ to SELF ID valid	0		100	ns
T_{IL} $\overline{SEL}$ ↓ to INT ↓ - Lost arbitration	5		120	ns
T_{SID} $\overline{SEL}$ ↓ to SELF and TARGET ID valid	6 x T_{ICLK}		(6 x T_{ICLK}) + 100	ns
T_{DS} DESKEW DELAY from VALID ID to $\overline{BSY}$ ↑	$T_{ICLK/2}$		$T_{ICLK/2}$	ns
T_{IES1} $\overline{BSY}$ ↑ to $\overline{INT}$ ↓ ②	(2 x T_{ICLK}) + 20		(2 x T_{ICLK}) + 20	ns
T_{IES2} $\overline{SEL}$ ↑ to $\overline{INT}$ ↓ ②	0		100	ns
T_{ES} $\overline{BSY}$ ↓ to $\overline{SEL}$ ↑	100		300	ns
T_{IDH} $\overline{SEL}$ ↑ to ID invalid	0			ns
T_{SBO} $\overline{SEL}$ ↑ to BSYOUT ↓	0			ns
T_{BBI} $\overline{BSY}$ ↓ to BSYIN ↓	0		100	ns
T_{SBI} $\overline{SEL}$ ↓ to BSYIN ↓	0		100	ns
T_{SA} $\overline{SEL}$ ↓ to $\overline{ATN}$ ↓	6 x T_{ICLK}		(6 x T_{ICLK}) + 100	ns
T_{SIO} $\overline{SEL}$ ↓ to I/$\overline{O}$ ↓	6 x T_{ICLK}		(6 x T_{ICLK}) + 100	ns

ELECTRICAL SPECIFICATIONS (Continued)

ARBITRATION AND (RE)SELECTION TIMING - SSI 32B450A INITIATED (Continued)

① NOTE: $\overline{BSY}$ ↓ will occur only after a minimum invalid period. If BSYOUT ↑ occurs more than T_{BOB} maximum before the end of the invalid period, then $\overline{BSY}$ ↓ will occur at the end, otherwise it will occur according to T_{BOB}. This is also true for SELF ID assertion. BSYOUT ↑ has the same effect as setting the ARB bit in the COMMAND register.

② NOTE: $\overline{INT}$ ↓ is triggered by $\overline{BSY}$ ↑ or $\overline{SEL}$ ↑ whichever occurs later.

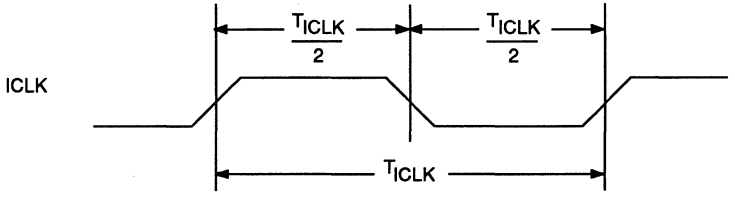


FIGURE 1: INTERNAL CLOCK

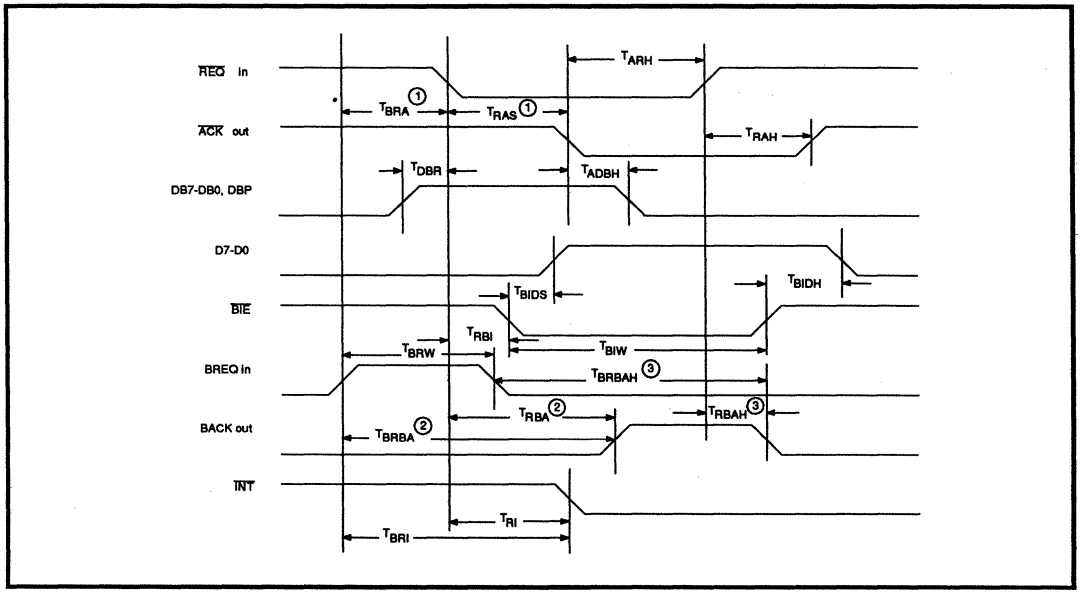


FIGURE 2: DATA TRANSFER INTERFACE TIMING - INITIATOR IN

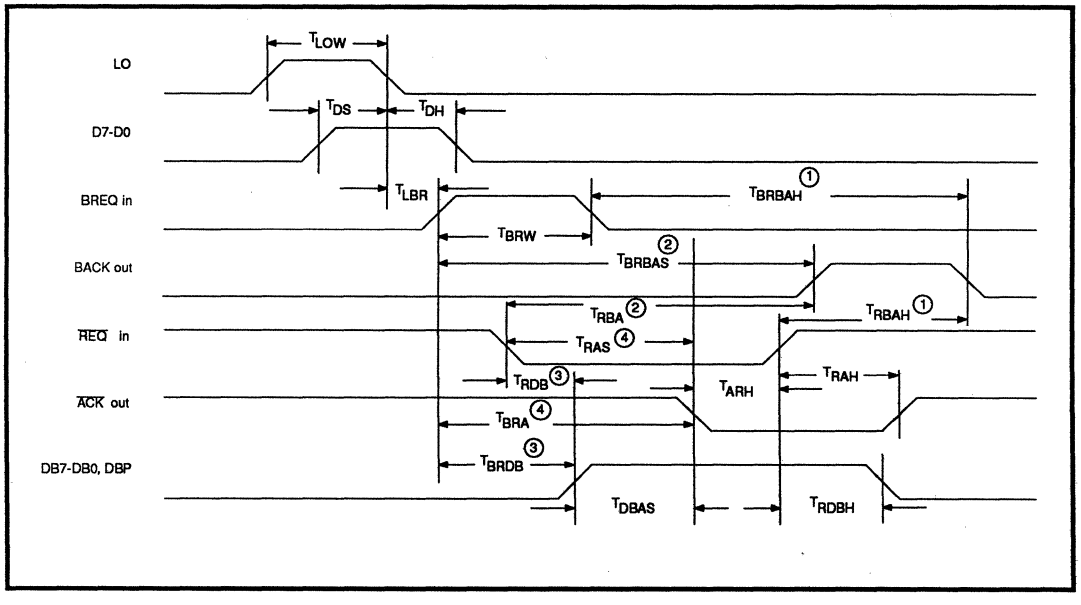


FIGURE 3: DATA TRANSFER INTERFACE TIMING - INITIATOR OUT

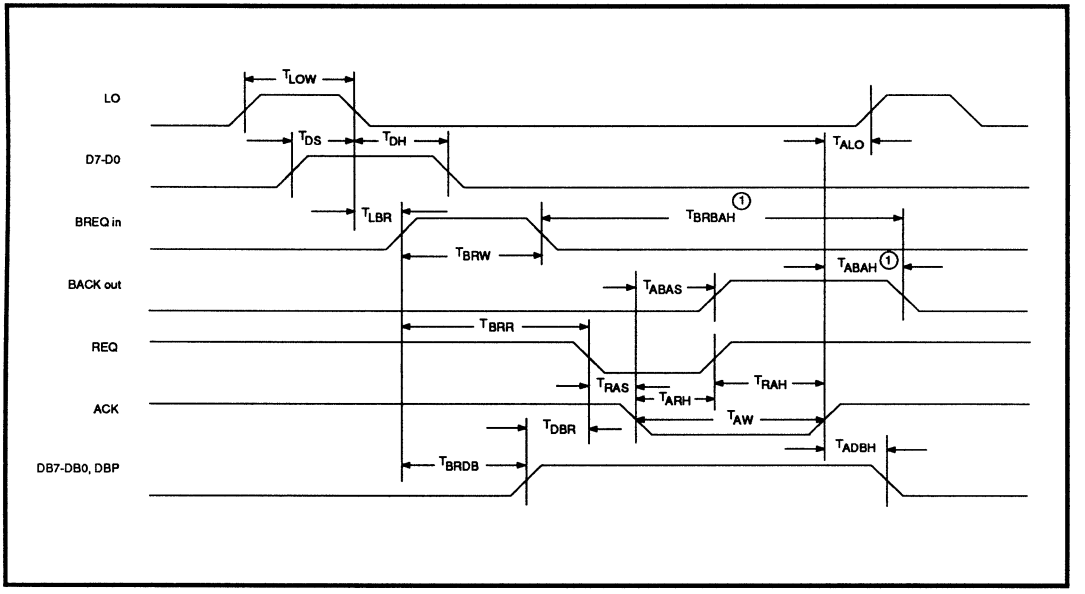


FIGURE 4: DATA TRANSFER INTERFACE TIMING - TARGET IN

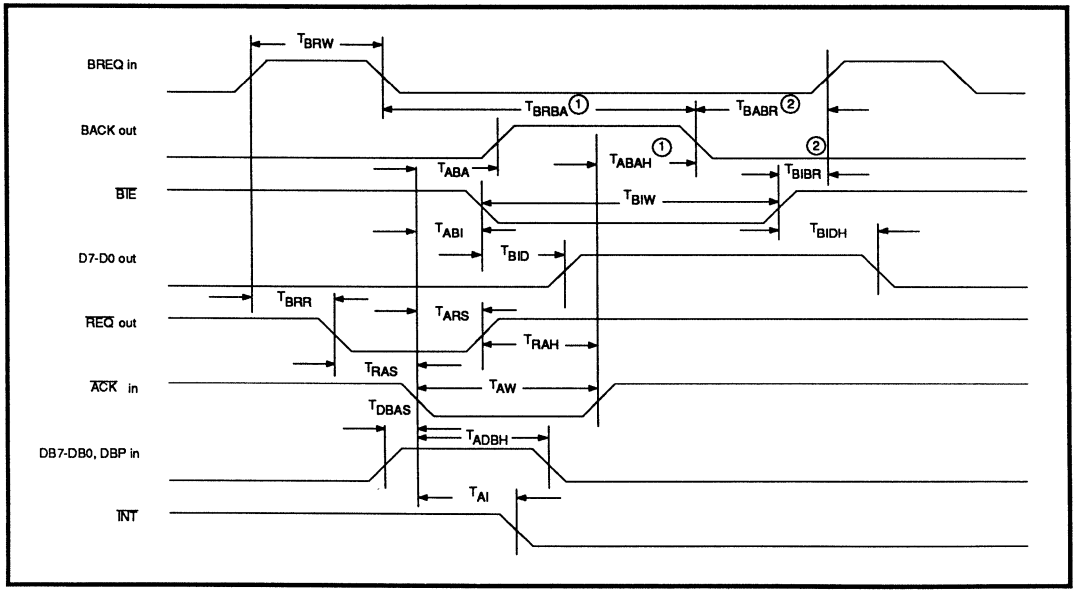


FIGURE 5: DATA TRANSFER INTERFACE TIMING - TARGET OUT

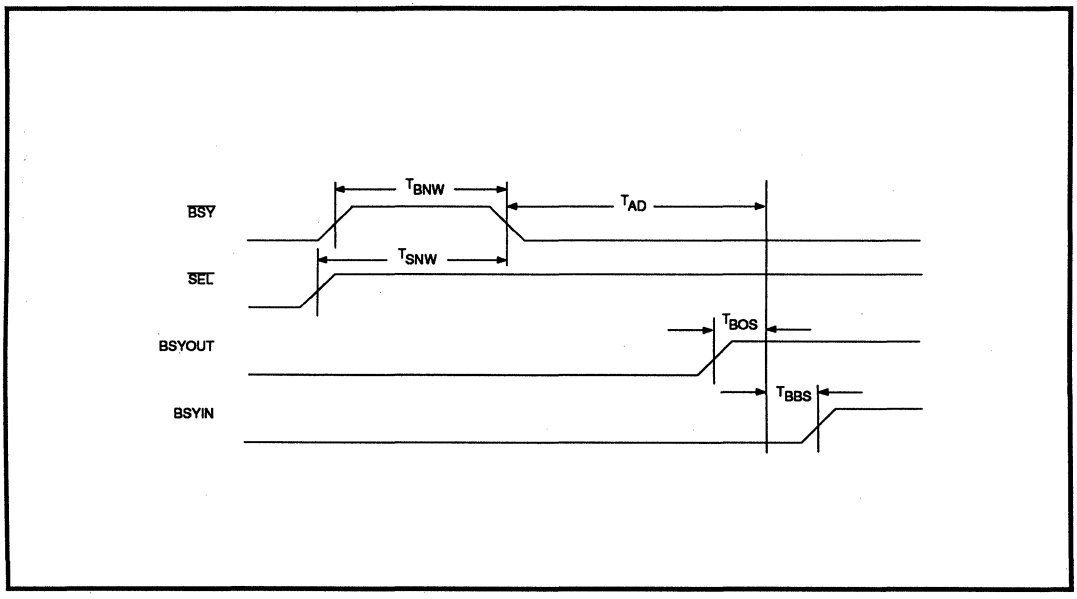


FIGURE 6: BSYIN AND BSYOUT TIMING - SSI 32B450A AND OTHER SCSI DEVICES ARBITRATING

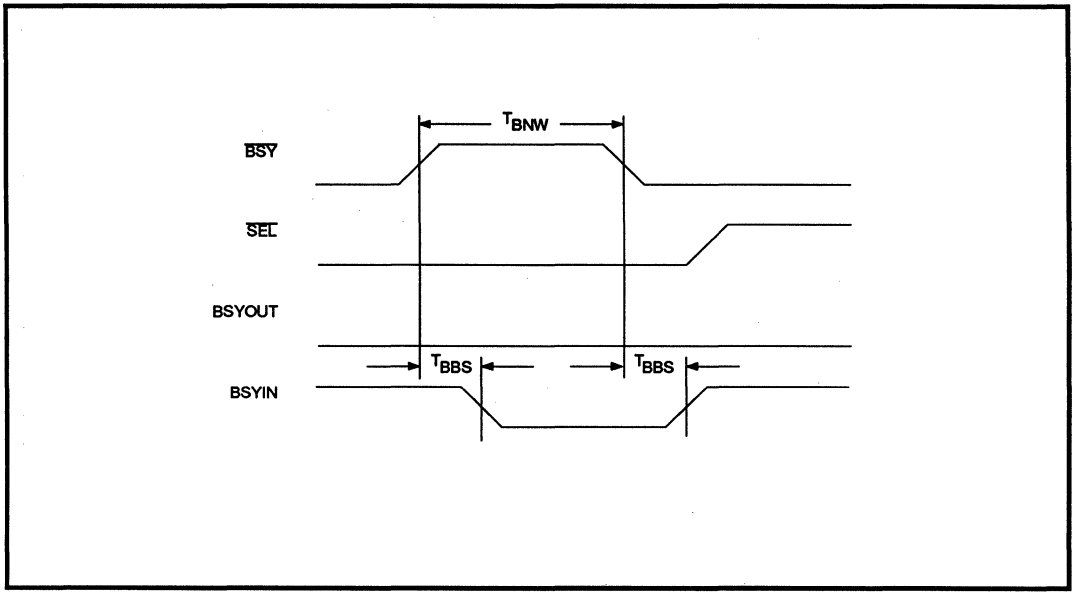


FIGURE 7: BSYIN AND BSYOUT TIMING - SSI 32B450A NOT ARBITRATING

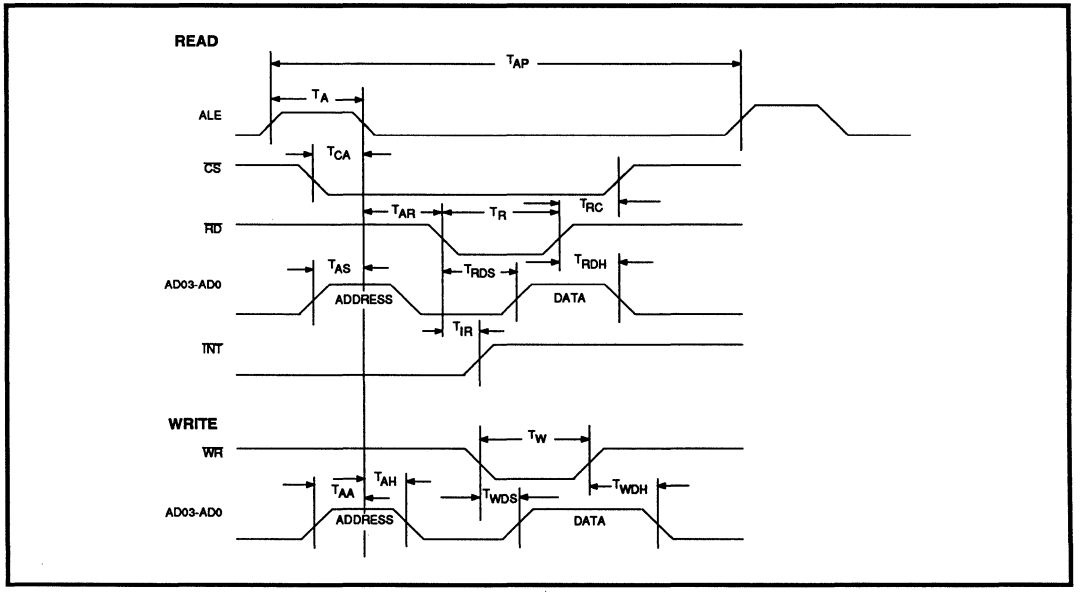


FIGURE 8: MICROPROCESSOR INTERFACE TIMING

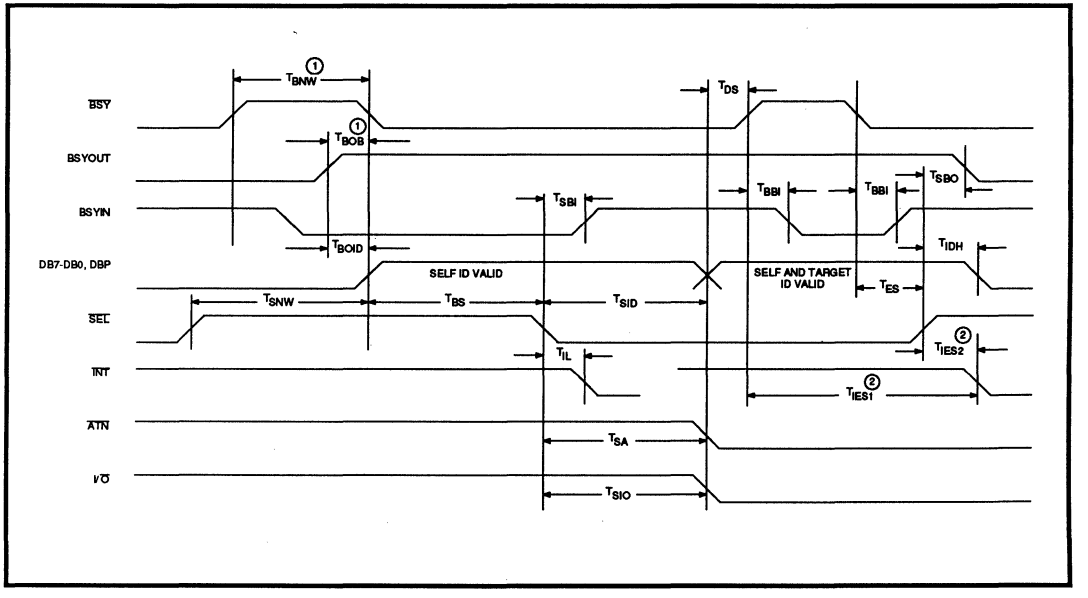


FIGURE 9: ARBITRATION AND (RE)SELECTION TIMING - SSI 32B450A INITIATED

APPLICATIONS INFORMATION

The SSI 32B450A is designed to be controlled by a multiplexed data/address bus microprocessor like the 8051. Before initiating any SCSI bus operations, the microprocessor should program the SSI 32B450A registers with self and target ID's, the conditions which will cause an interrupt, and response to bus operations by programming the registers.

The SCSI bus interface circuitry of the SSI 32B450A executes the interface processes in accordance with ANSI specification X3.131-1986. An overview of a typical SCSI signal sequence is shown in Figure 10. A definition of the delay times and signal states for the phases called out in this description is given at the end of the Applications Information section. The bus-free phase begins when both $\overline{SEL}$ and $\overline{BSY}$ are continuously false for a bus-settle delay (400 nsec). At the end of the bus-settle delay, plus bus-free time (800 nsec) the arbitration phase can begin.

The SCSI devices wishing to arbitrate for the bus-wait at least one bus-free delay (800 nsec.) but no longer than a bus-settle delay (1.8 µsec.) from the end of the bus-free phase, and assert $\overline{BSY}$ and their SCSI ID on to the bus. If at any time during arbitration delay, SEL becomes active, all arbitrating devices must relinquish the bus within the bus clear delay. After an arbitration delay (2.2 µsec) the arbitrators examine the bus and determine whether higher priority SCSI devices are also arbitrating. The winner asserts $\overline{SEL}$. The other devices must release $\overline{BSY}$ and their ID within a bus clear delay (800 nsec). The winner waits at least bus-clear plus bus-settle delays and then asserts both its ID and the target ID onto the bus. After two deskew delays it releases $\overline{BSY}$. The target determines that has been selected when $\overline{SEL}$ and its ID have been valid on the bus, and $\overline{BSY}$ and I/$\overline{O}$ have not been asserted, for a bus-settle delay. The target should assert $\overline{BSY}$ within a selection abort time (200 µsec). It is not required to assert $\overline{BSY}$ within a selection abort time but it must guarantee that it will not assert $\overline{BSY}$ after a selection abort time has passed and the initiator aborts the selection process. The initiator waits two deskew (45 nsec. each) delays after detecting $\overline{BSY}$ true to change the SCSI bus and move to other cycles.

The SSI 32B450A handles the processes described above without intervention from the microprocessor. When the arbitration process is initiated the SSI 32B450A will arbitrate for the bus. If it loses, the SSI 32B450A will continue to monitor for the bus- free phase and arbitrate again unless the BSYOUT signal is negated and/or the ARB bit in the COMMAND register is reset. If arbitration is initiated by asserting BSYOUT then it must be terminated by negating BSYOUT. If it is initiated by setting ARB, then it must be terminated by resetting ARB. When being selected or reselected the SSI 32B450A will assert the proper signals, including its ID onto the SCSI bus. When the registers are set up to do so $\overline{INT}$ will be asserted upon completion of (re)selection, when the SSI 32B450A has been (re)selected, in the case of an error or $\overline{SRST}$ being asserted.

There are two arbitration/selection timing parameters which have not been implemented by the SSI 32B450A due to their length. They are selection-abort time and selection-timeout delay. It is suggested that the microprocessor implement a timing sequence beginning when the $\overline{INT}$ signal is asserted to indicate arbitration won. The microprocessor reads the SSI 32B450A status at the end of each of the two time periods unless an interrupt has occurred to indicate successful (re)selection making the time-outs unnecessary. If (re)selection is not completed within the time-outs then the microprocessor must initiate a timeout procedure as described in the ANSI specification.

After successful completion of the (re)selection phase, the SCSI devices usually enter the command phase. The target asserts C/$\overline{D}$ and keeps I/$\overline{O}$ and $\overline{MSG}$ negated for this phase. The target is in control of information transfer which moves from initiator to target under direction of the target. The target asserts $\overline{REQ}$ requesting a command byte from the initiator. As in the data transfer phase, the initiator drives D7-D0 with valid information and asserts $\overline{ACK}$ to inform the target that valid information is present. This phase is distinguished from the data transfer phase by C/$\overline{D}$ being true. The target reads the information and negates $\overline{REQ}$ indicating to the initiator that it may release $\overline{ACK}$ and the data bus. The target requests transfer of command information until it has received the number of bytes contained in the group code of the first command byte. The target then asserts I/$\overline{O}$ and negates C/$\overline{D}$ and $\overline{MSG}$ to enter the data transfer phase. When using the SSI 32B450A the C/$\overline{D}$, I/$\overline{O}$ and $\overline{MSG}$ signals are asserted by setting the corresponding bits in the SCSI1 register. The byte of command data transferred is read or put into buffer memory by the microprocessor

using the ONEXFER bit in the SCSI2 register. Upon completion of the command phase, the microprocessor sets the proper bits in the SSI 32B450A to enter the data transfer phase and can continue to transfer data in a programmed I/O mode as it has the commands, or can turn control over to the data transfer control logic or SSI 32C453.

The SSI 32B450A and SSI 32C453 were designed to work directly with one another and timing of the data transfer signals is completely coordinated. No external logic is required to connect the two devices.

The data transfer phase is handled automatically by the SSI 32B450A and SSI 32C453 or data transfer control logic and is described in detail in the Functional Description section of this data sheet. The microprocessor ascertains that data transfer is complete by polling the DMADONE bit in the DMACON register of the SSI 32C453. The microprocessor then causes the SSI 32B450A to enter the status phase by setting the C/D and I/O bits in the SCSI1 register causing the C/$\overline{D}$ and I/$\overline{O}$ signals to be asserted onto the SCSI bus. The MSG signal remains negated during the status phase. This is the same as the command phase except that information transfer is from the target to the initiator which is indicated by the I/$\overline{O}$ signal being true. The purpose is to provide status to the initiator about the data transfer. The cycle is completed with the target requesting to send a command complete message to the initiator. This is the message-in phase which is the same as the status phase except that the MSG signal is asserted. There are other phases described in the ANSI specification which are not described in detail here.

When the SSI 32B450A is used with the SSI 32C452 and SSI 32C453 the command read and write can be handled in the following manner. The SSI 32C452 and SSI 32C453 have an external register feature. These registers are at locations 50H, and 51H. When the microprocessor writes or reads to or from these locations, the D7-D0 bus of the SSI 32C452 will be connected internally with the AD7-AD0 bus allowing data to pass from the data bus to or from the microprocessor in the proper direction. A microprocessor read from these locations will cause the SSI 32C453 to assert $\overline{BIE}$ and set the $\overline{BIE}$ bit in the INTCON register. Assertion of $\overline{BIE}$ enables output from D7-D0 from the SSI 32B450A (or any latch) so that the command can pass through the SSI 32C452. A microprocessor write to these locations will cause the SSI 32C453 to assert LO and $\overline{BOE}$. Asserting LO will strobe the data into the SSI 32B450A (or any latch). Setting the ONEXFER bit in the SCSI2 register of the SSI 32B450A will cause that data to be transferred on the SCSI bus. Register 50H access is for single byte transfer, and register 51H access is for the second byte of a double byte access if a 16 bit command word is used.

SCSI SPECIFICATION INFORMATION

This information from the ANSI Standard for the Small Systems Computer Interface is provided to assist in implementing a SCSI based controller with the SSI 32B450A.

	SIGNALS				
Bus Phase	**$\overline{BSY}$**	**$\overline{SEL}$**	**C/$\overline{D}$, I/$\overline{O}$, $\overline{MSG}$, $\overline{REQ}$**	**ACK/ATN**	**DB7-0**
Bus Free	None	None	None	None	None
Arbitration	All	Winner	None	None	SCSI ID
Selection	I & T	Initiator	None	Initiator	Initiator
Reselection	I & T	Target	Target	Initiator	Target
Command	Target	None	Target	Initiator	Initiator
Data In Target	Target	None	Target	Initiator	Target
Data Out	Target	None	Target	Initiator	Initiator
Status Target	Target	None	Target	Initiator	Target
Message In	Target	None	Target	Initiator	Target
Message	Target	None	Target	Initiator	Initiator

TABLE 1: BUS PHASE SIGNAL SOURCES

DEFINITIONS FOR TABLE

All: The signal is driven by all SCSI devices which are actively arbitrating.

SCSI ID: The SCSI ID is a unique data bit (DB) for each of the SCSI devices in the system and is driven onto the SCSI bus by each device that is actively arbitrating. The other seven data bits shall not be driven by the SCSI device. The parity bit may be asserted or undriven during arbitration but can't be driven false.

I&T: This signal is driven by the initiator, target or both as specified in the selection or reselection phase.

Initiator: If this signal is driven is can be driven only by the active initiator.

None: The signal is released, meaning it is not driven by any SCSI device.

Winner: The signal shall be driven by the one SCSI device that wins arbitration.

Target: If the signal is driven it can be driven only by the active target.

SIGNAL				
$\overline{MSG}$	C/$\overline{D}$	I/$\overline{O}$	Phase Name	Direction of Transfer
1	1	1	Data Out	Initiator to Target
1	1	0	Data In	Initiator from Target
1	0	1	Command	Initiator to Target
1	0	0	Status	Initiator from Target
0	1	1	#	
0	1	0	#	
0	0	1	Messsage Out	Initiator to Target
0	0	0	Messsage In	Initiator from Target
# = Reserved for future standardization				

TABLE 2: SIGNAL STATUS; INFORMATION TRANSFER PHASES

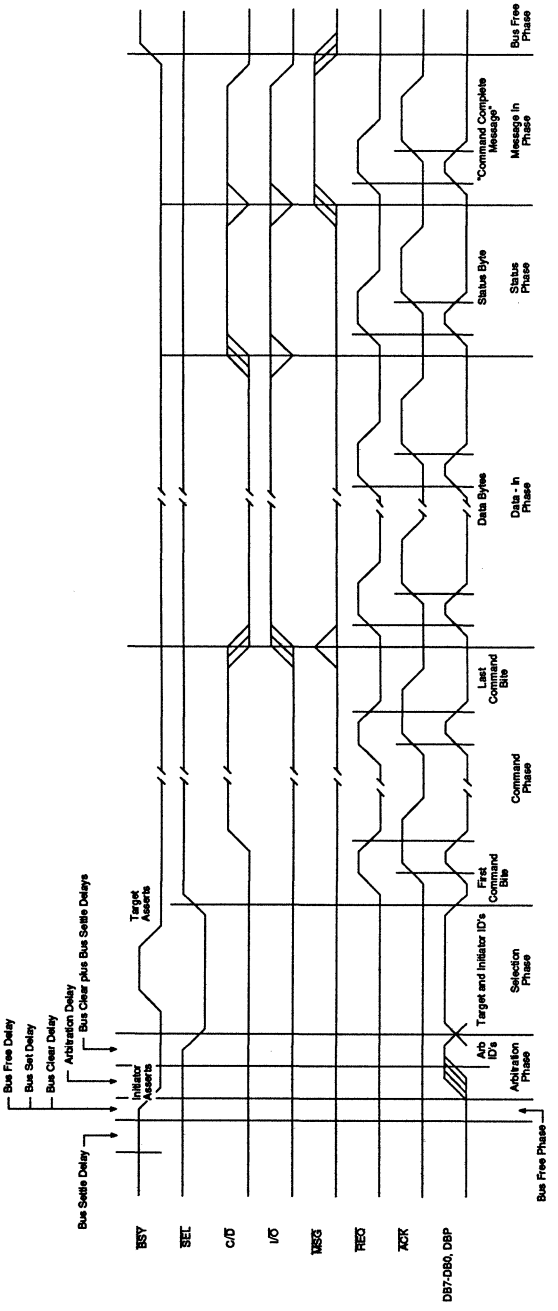
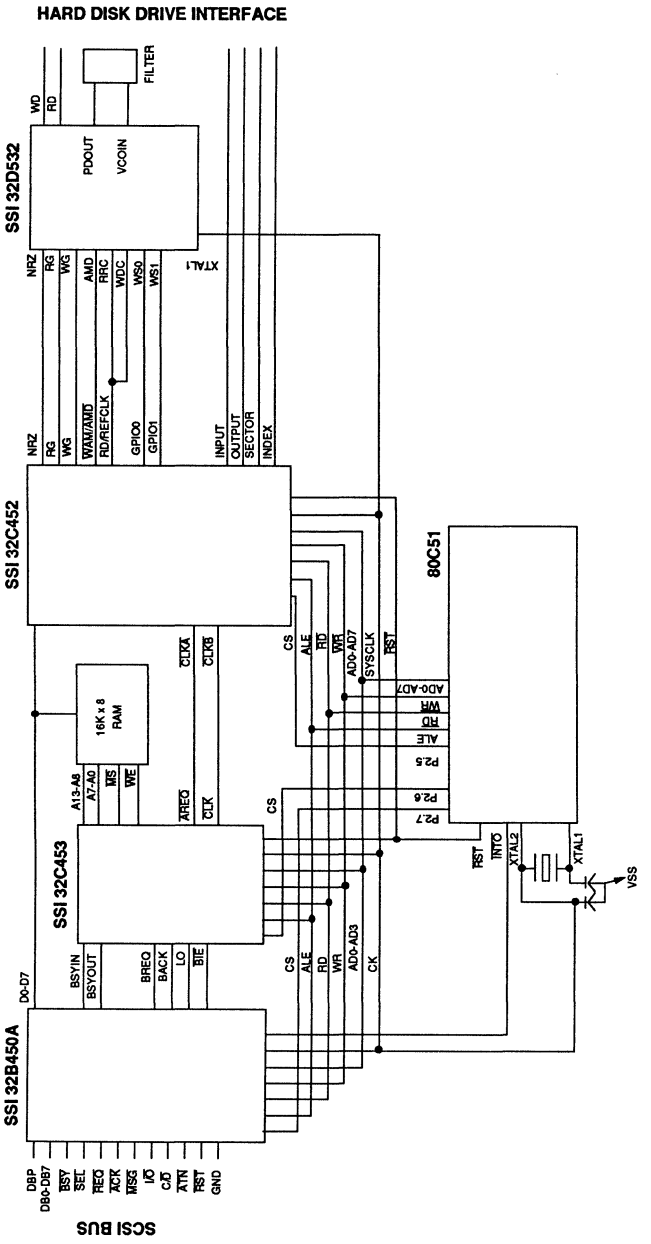


FIGURE 10: SCSI SIGNAL SEQUENCE EXAMPLE



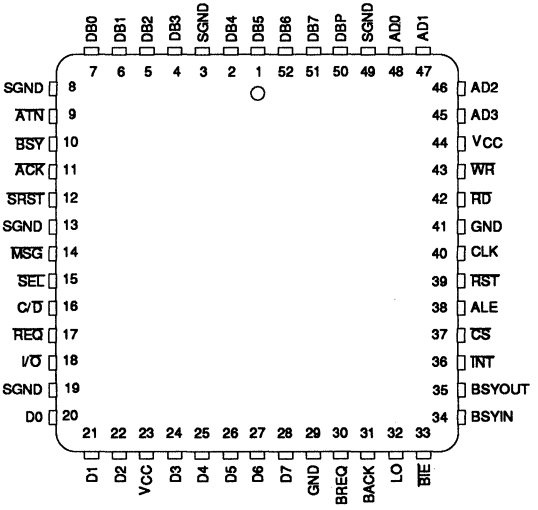
SCSI PERIPERAL CONTROLLER CHIP SET

6

SSI 32B450A
SCSI Controller

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32B450A SCSI Controller 52-Pin PLCC	SSI 32B450A-CH	32B450A-CH

silicon systems™

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

SSI 32B451
SCSI Controller

August, 1988

DESCRIPTION

The SSI 32B451 SCSI bus interface device is designed to adapt a peripheral controller (target) system to a small computer system interface (SCSI) bus.

As a target adapter, the SSI 32B451 contains circuitry to complement the logic of the SSI 32C453 Dual Port Buffer Controller for SCSI arbitration; SCSI REQ/ACK handshake; and parity generation and checking. In its role as a target SCSI adapter, the circuitry on the device maximizes SCSI bus performance in all phases and ensures conformance with the SCSI specification.

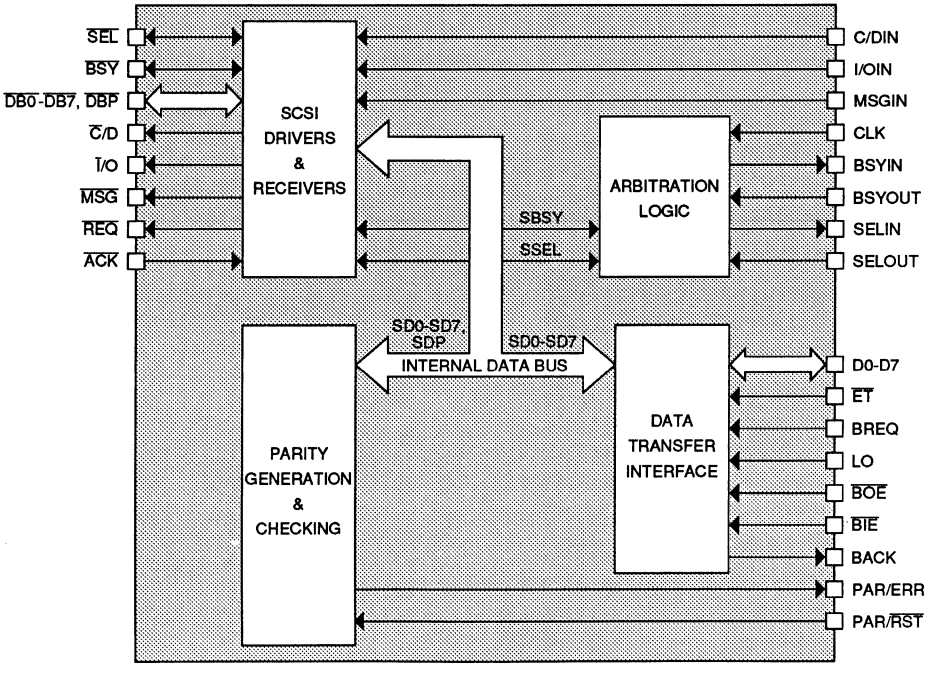
The SSI 32B451 includes high current drivers and Schmitt trigger receivers which allow for direct connection to the SCSI bus for the single ended interfacing option. The SSI 32B451 is intended for use in designs based around the SSI 32C452 storage controller and the SSI 32C453 Dual Port Buffer Controller.

FEATURES

- **Supports asynchronous data transfer up to 1.5 Mbytes/sec**
- **Supports target role in SCSI applications**
- **Includes high current drivers and Schmitt trigger receivers for direct connection to the SCSI bus**
- **Full hardware compliance to ANSI X3T9.2 Rev. 17B specification as a target peripheral adapter**
- **Contains circuitry to support SCSI arbitration, (re)selection and parity features**
- **Complements the SSI 32C453 Buffer controller**
- **Plug compatible with AIC 500L**
- **Available in 44 pin PLCC**
- **Single +5V supply**
- **Fabricated in 2 micron CMOS technology**

6

BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

The purpose of the SSI 32B451 is to fulfill a support role within a hardware design. The device contains four circuit functions which interact within the overall design. The partial schematic in Figure 10 illustrates this interaction. This section describes each of the functional circuits.

DATA TRANSFER INTERFACE

The data transfer interface logic coordinates the transfer of data between the data transfer logic and the SCSI bus. Standard two-wire DMA handshaking is supported by the BREQ and BACK signals. This section is organized to connect directly with the SSI 32C453, Dual Port Buffer Controller, but is easily connected to any other data transfer control device. Before DMA controlled information transfer can begin, a valid connection must exist to the SCSI bus with BSY active and no phase error. The direction of information flow is controlled by the I/O In signal from the storage controller or a latch.

The device complements the buffer controller handshake timing by latching the SCSI data before transferring into the controller buffer. This speeds the data transfer across the bus by reducing the $\overline{REQ}/\overline{ACK}$ timing restraints for the SCSI bus transfers.

In the target-in state (read operation), the data is being transferred from the peripheral controller to the initiator or the host. The buffer controller device controls when the buffer is accessed to pass on to the device. Once valid data is present on D0-D7 of the buffer data, LO is asserted, latching data into the device. The buffer controller then asserts BREQ, indicating to the device that valid data is in the internal latch ready to be transferred over the SCSI bus. The device then places data on the SCSI bus and then asserts $\overline{REQ}$. The data setup time required by SCSI specification is dictated primarily by the buffer controller. The host (initiator) asserts $\overline{ACK}$ indicating acceptance of the SCSI data transfer cycle. The device asserts BACK to the buffer controller logic indicating completion of that cycle. Refer to Read Operation timing diagram (Figure 4) for an illustration of this handshake.

In the target-out state (write operation), the data is being transferred from the initiator to the buffer upon the control of the buffer controller. The buffer controller asserts BREQ requesting transfer of a byte of data from the initiator. The device, in turn, asserts $\overline{REQ}$ and the initiator responds by driving the SCSI data bus and asserting $\overline{ACK}$ which latches data into the device. BACK is asserted by the device indicating that the byte is latched inside the device and is available to be transferred to the buffer RAM. The buffer controller then asserts $\overline{BIE}$ to enable output of the data to the RAM. When the buffer controller has completed transferring the data it negates $\overline{BIE}$ and BREQ indicating to the device that the cycle is complete. Refer to Write Operation timing diagram (Figure 3) for an illustration of this handshake.

ARBITRATION

The purpose of this block is to complement the logic in the SSI 32C453, buffer controller device, for SCSI bus arbitration during selection of the target controller or reselection of the initiator phases. The device simply passes along the $\overline{SEL}$ and $\overline{BSY}$ signals as SEL IN and BSY IN, respectively. It also monitors the control line BSYOUT received from the buffer controller chip for a minimum of three clock periods and a maximum of four clock periods (Bus-Free Delay) after which time it outputs $\overline{BSY}$.

Once the device has performed these functions it leaves the actual arbitration activity to the local microcontroller and the buffer controller. Refer to the SSI 32C453 specification for details of this activity.

The SCSI signals $\overline{SEL}$, SELOUT, $\overline{BSY}$ and BSYOUT received from the buffer controller are internally inverted and become SELIN, $\overline{SEL}$, BSYIN and $\overline{BSY}$, respectively. The actual monitoring of these lines for SCSI timing specification is accomplished by the buffer controller. The actual arbitration activity for the SCSI bus is performed by the buffer controller device and the local microcontroller. Refer to the SSI 32C453 specification for the timing of this activity.

PARITY GENERATION

Parity functions as 'Odd' parity only. For incoming data, the SSI 32B451 checks parity or computes and passes the computed bit to the buffer RAM depending upon the condition of PAR/$\overline{RST}$ line. For outgoing data, the device always computes parity on the data and presents to the SCSI bus.

For the incoming SCSI data, the device generates parity internally and compares it against the parity bit received if the PAR/$\overline{RST}$ line is high. The result of this comparison is latched at the PAR/ERR output signal. An error is indicated by a high signal at this output. To clear the error condition, the PAR/$\overline{RST}$ line must be driven to a low level.

Alternatively, if PAR/$\overline{RST}$ is held low, the device computes parity on incoming SCSI data and presents this parity bit at the PAR/ERR output. This value can be stored in the buffer RAM for parity checking at a later time.

For outgoing data, parity is always generated and presented for the SCSI bus on the $\overline{DBP}$ line by the device.

NOTE: Parity, as a function of SCSI, is optional. However, the SSI 32B451 ignores this and works parity continuously. The surrounding design has responsibility of either monitoring parity or ignoring it.

SCSI INTERFACE

Drivers and receivers are provided internally to the SSI 32B451 for direct connection to the SCSI bus. The only components necessary outside of the chip are the pull-up and pull-down resistors for the interface and receivers for SCSI Attention and Reset signals. The data and parity signals received from the SCSI bus are passed along to the Data Transfer Interface and parity circuits described above. The data and parity bits to be sent over to the SCSI bus are buffered by this circuit.

PIN DESCRIPTION

This section describes the names of pins, their symbols, their functions and their active states. The signals are grouped in four categories according to their interface to other components on the board. The four categories area:

* SCSI Bus Interface
* Buffer Controller/Buffer RAM Interface
* Storage Controller Interface
* Others

SCSI BUS INTERFACE

The following group of signals interface directly to the SCSI bus. All output and bi-directional lines have 48 mA sinking current capability. All input buffers are Schmitt trigger inputs and all outputs have high current open drain buffers to allow direct connection to the SCSI bus.

NAME	PIN #	TYPE	I/O	DESCRIPTION
$\overline{DB0}$-$\overline{DB7}$	13-17 19-21	SCSI	I/O	Data Bus. Buffered data bus signals interface directly to SCSI bus.
$\overline{DBP}$	10	SCSI	I/O	Data Bus Parity. Parity bit for the SCSI data bus signals. It is always generated when data is transferred on the SCSI bus. It can be ignored on reception. Active low.
$\overline{ACK}$	7	SCSI	I	Acknowledge. This signal is an input from the initiator in response to the SSI 32B451's $\overline{REQ}$, and indicates valid data on the SCSI bus. Active low.
$\overline{SEL}$	23	SCSI	I/O	Select. Active low signal used by an initiator (the host) to select a target or by a target to reselect an initiator.

SCSI BUS INTERFACE (Continued)

NAME	PIN #	TYPE	I/O	DESCRIPTION
$\overline{BSY}$	25	SCSI	I/O	Busy. Active low. An "OR-tied" signal that indicates the bus is being used.
$\overline{MSG}$	11	SCSI	O	Message. Open drain SCSI signal. Signal driven by the device to indicate that the SCSI communication is in the message phase. Active low.
$\overline{C}$/D	27	SCSI	O	Command/Data. Open drain SCSI signal driven by the device that indicates control or data information is on the data bus.
$\overline{REQ}$	22	SCSI	O	Request. Active low true signal driven to request data byte transfers. Also, used to "Acknowledge" at completion of transfer.
$\overline{I}$/O	26	SCSI	O	Input/Output. SCSI signal that controls the direction of data movement on the SCSI bus with respect to the initiator.

BUFFER CONTROLLER/BUFFER RAM INTERFACE

The following group of signals are associated with buffer data and control. All signals except the buffer data signals interface to the SSI 32C453, Dual Port Buffer Controller.

NAME	PIN #	TYPE	I/O	DESCRIPTION
BREQ	35	TTL	I	Buffer Request. When asserted, this signal indicates that the peripheral buffer controller is requesting to transfer a byte of data. Active high input.
BACK	6	TTL	O	Buffer Acknowledge. When asserted this signal indicates acceptance of data transfer. Active high output.
LO	38	TTL	I	Latch Out. Latches data into the device to be presented to the SCSI bus. Active high.
$\overline{BIE}$	39	TTL	I	Bus In Enable. Active low. A strobe from the data transfer control logic which indicates it is transferring data from the SCSI bus to the local buffer.
$\overline{BOE}$	5	TTL	I	Bus Out Enable. Active low. A strobe from the data transfer control logic which indicates it is transferring data from the local buffer to the SCSI bus.
$\overline{ET}$	8	TTL	I	Target Enable. Active low. A signal connected to the SSI 32C453. When this signal is active it provides microcode and hardware control to enable all drivers except Busy on the SCSI bus.

BUFFER CONTROLLER/BUFFER RAM INTERFACE (Continued)

NAME	PIN #	TYPE	I/O	DESCRIPTION
SEL IN	29	TTL	O	Select In. Active high. Used to pass the select line from the SCSI bus to the buffer controller.
SEL OUT	28	TTL	I	Select Out. Active high. Used as an input from the buffer controller to indicate when to drive the select line on the SCSI bus.
BSY IN	31	TTL	O	Busy In. Active high. Used to pass busy from the SCSI bus to the buffer controller. Indicates other devices are actively accessing the bus.
BSY OUT	32	TTL	I	Busy Out. Active high. Used as an input from the buffer controller to indicate when to drive the busy line on the SCSI bus.
D0-D7	2-4 40-44	TTL	I/O	Buffer Data. These lines connect to buffer RAM data pins.

STORAGE CONTROLLER INTERFACE

The following group of pins interface with the SSI 32C452, Storage Controller. These lines may also be connected to an output port of a microcontroller or a latch.

NAME	PIN #	TYPE	I/O	DESCRIPTION
MSG IN	9	TTL	I	Message In. Active high signal from the storage controller drives the SCSI $\overline{MSG}$ signal low.
I/O IN	33	TTL	I	I/O In. A high signal from the storage controller drives the SCSI $\overline{I/O}$ signal low.
C/D IN	30	TTL	I	C/D In. A high signal from the storage controller drives the SCSI $\overline{C/D}$ signal low.

OTHERS

The following group of lines are the miscellaneous signals.

NAME	PIN #	TYPE	I/O	DESCRIPTION
CLK	34	TTL	I	Clock. Used for clock input between 2.5 MHz and 5 MHz. This signal is used internally during the arbitration phase only.
PAR/ERR	37	TTL	O	Parity/Error. Logic 1 indicates a parity error detected on the SCSI bus when PAR/$\overline{RST}$ is held high. When the PAR/$\overline{RST}$ line is held low, parity will be passed to the controller buffer by using the PAR/ERR line as the parity bit for each byte.

OTHERS (Continued)

NAME	PIN #	TYPE	I/O	DESCRIPTION
PAR/$\overline{RST}$	36	TTL	I	Parity/Reset. When held high, the device checks SCSI bus parity error by setting logic 1 (high) on the PAR/ERR pin. When held low, parity is passed through the device to the controller buffer with the PAR/ERR line being the parity bit.
GND	12, 18, 24			Ground. Device system ground.
VCC	1			Power Supply. +5V input for power to the device.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.)

PARAMETER	RATING	UNIT
VCC with respect to VSS (GND)	+7	V
Max. voltage on any pin with respect to VSS	-0.5 to +7	V
Operating temperature	0 to 70	°C
Storage temperature	-55 to +125	°C

DC OPERATING CHARACTERISTICS

(Ta = 0 to 70°C, VCC = +5V ± 5%, VSS = 0V)

PARAMETER		CONDITION	MIN	MAX	UNITS
IIL	Input Leakage ($\overline{BREQ}$, LO, $\overline{BOE}$, $\overline{BIE}$, $\overline{ET}$ SELOUT, BSYOUT, $\overline{CDIN}$, I/OIN, $\overline{MSGIN}$, PAR/$\overline{RST}$, CLK, $\overline{ACK}$)	0 < Vin < VCC	-10	+10	µA
IOL	SCSI Output Leakage ($\overline{SEL}$, $\overline{BSY}$, $\overline{DB0}$-$\overline{DB7}$, $\overline{DBP}$, $\overline{MSG}$, $\overline{C}$/D, $\overline{I}$/O)	0.5 < Vout < VCC	-50	+50	µA
IOL	D0-D7	0.45 < Vout < VCC	-10	+10	µA
VIL	Input Low Voltage		0	0.8	V

DC OPERATING CHARACTERISTICS (Continued)

PARAMETER		CONDITION	MIN	MAX	UNITS
VIH	Input High Voltage		2.0		V
VOH	Output High Voltage	IOH = -400 µA	2.4		V
VOL	SCSI Output Low Voltage	IOL = 48 mA		0.5	V
VOL	All others	IOL = 2 mA		0.4	V
	Power Dissipation			500	mW
Vhsy	Hysteresis Voltage (all SCSI signals)		200		mV
Iccs	Standby Current	Ta = 70°C		600	µA
Icc	Supply Current	Ta = 70°C		30	mA
Cin	Input Capacitance			15	pF

AC CHARACTERISTICS

The following sections list the timing characteristics necessary for the proper operation of the device. Unless otherwise specified, all timing parameters pertain to input clock frequency (2.5 MHz min. to 5.0 MHz max.).

Note: AC timing is measured at Voh = 2.0V, Vol = 0.8V, Cin = 50 pF. Timing characteristics are valid over the entire operating temperature, 0 to 70°C, and voltage range, 4.75 to 5.25 volts.

CLOCK AND PARITY TIMING (See Figures 1 & 2)

SYMBOL	PARAMETER	MIN	MAX	UNITS
TICLK/2	Input Clock Half-Cycle	100	200	ns
TICLK	Input Clock Width	200	400	ns
DPV	Data Valid to Parity Detect		100	ns

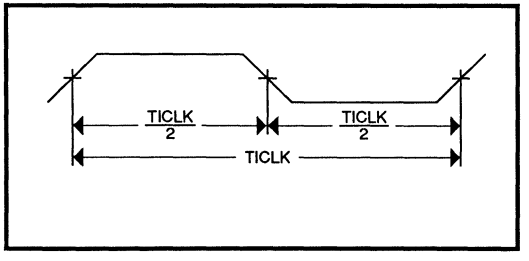


FIGURE 1: Input Clock Timing

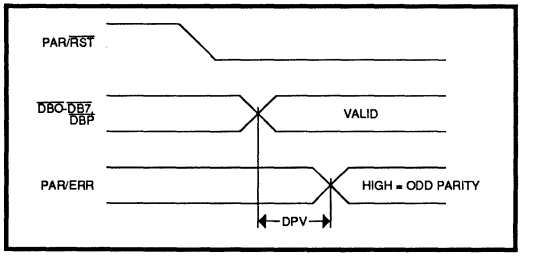
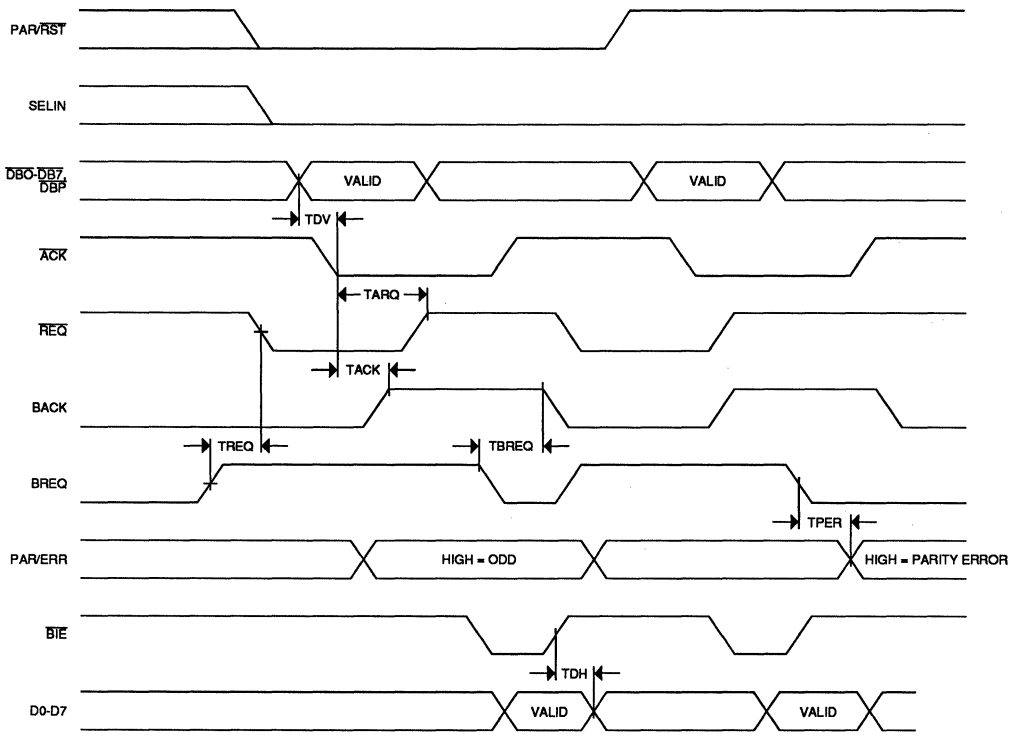


FIGURE 2: SCSI Bus Parity Timing

WRITE OPERATION TIMING (See Figure 3)

SYMBOL	PARAMETER	MIN	MAX	UNITS
TREQ	BREQ ↑ to $\overline{REQ}$ ↓		21	ns
TARQ	$\overline{ACK}$ ↓ to $\overline{REQ}$ ↑		55	ns
TACK	$\overline{ACK}$ ↓ to BACK ↑		50	ns
TBREQ	BREQ ↓ to BACK ↓		25	ns
TDH	$\overline{BIE}$ ↑ to Data Invalid		40	ns
TDV	SCSI Data Valid to $\overline{ACK}$ ↓	55		ns
TPER	BREQ ↓ to Parity Error Valid		45	ns

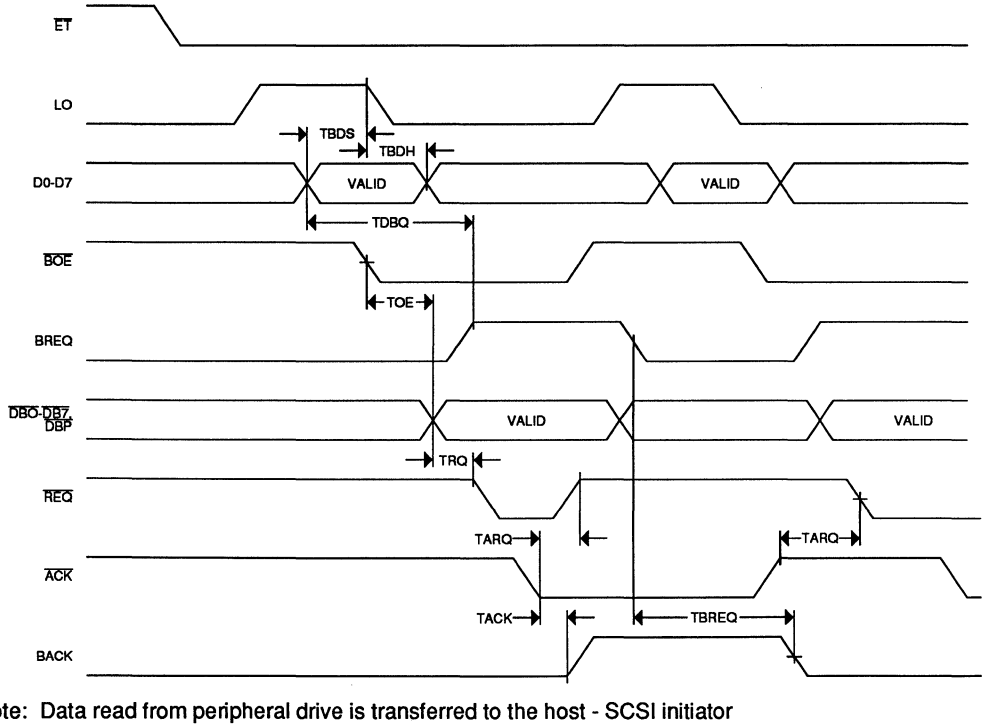


Note: Data from host - SCSI initiator - is transferred to buffer RAM.

FIGURE 3: Write Operation Timing

READ OPERATION TIMING (See Figure 4)

SYMBOL	PARAMETER	MIN	MAX	UNITS
TBDS	Buffer Data Valid to LO ↓	0		ns
TBDH	LO ↓ to Buffer Data Invalid	25		ns
TDBQ	Buffer Data Valid to BREQ ↑	90		ns
TRQ	SCSI Bus Data Valid to $\overline{REQ}$ ↓	55		ns
TARQ	$\overline{ACK}$ ↓ to $\overline{REQ}$ ↑		55	ns
TACK	$\overline{ACK}$ ↓ to BACK ↑		55	ns
TARQ	$\overline{ACK}$ ↑ to $\overline{REQ}$ ↓		55	ns
TBREQ	BREQ ↓ to BACK ↓		25	ns
TOE	$\overline{BOE}$ to SCSI Data Valid		35	ns



Note: Data read from peripheral drive is transferred to the host - SCSI initiator

FIGURE 4: Read Operation Timing

ARBITRATION AND CONTROL SIGNAL TIMING (See Figures 5 & 6)

SYMBOL	PARAMETER	MIN	MAX	UNITS
TSELO	SELOUT ↑ or ↓ to $\overline{SEL}$ ↓ or ↑		35	ns
TBOT	BSYOUT ↑ or ↓ to $\overline{BSY}$ ↓ or ↑	3 x TICLK	4 x TICLK + 40	ns
TCNT	MSGIN, I/OIN, CDIN to $\overline{MSG}$, $\overline{I}$/O, $\overline{C}$/D		35	ns

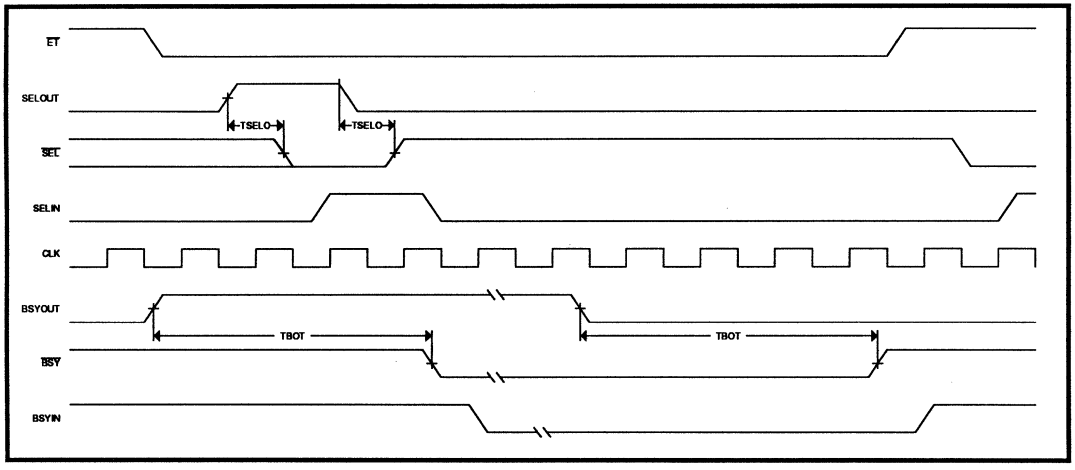


FIGURE 5: Arbitration Signals Timing

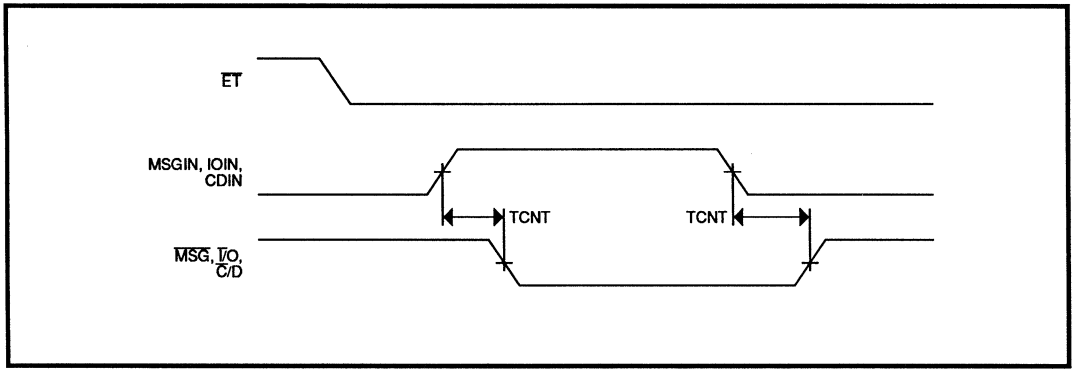


FIGURE 6: SCSI Control Signal Timing

APPLICATION NOTES

The SSI 32B451 supports the SSI 32C453 and the local microprocessor in performing all the SCSI target controller functions. For successful SCSI bus operation, the target controller must follow all the requirements of the SCSI protocol defined by ANSI specification X3T9.2 Rev. 17B. An overview of a typical SCSI signal sequence is shown in Figure 7.

Before any SCSI operations can begin, the local microprocessor polls the $\overline{BSY}$ line through the SSI 32C453 (BSYIN signal). When this signal is asserted, the microprocessor checks the arbitration I.D. asserted by the initiator.

Following the Arbitration phase, the SCSI bus enters the Selection phase. SSI 32B451 assists the Arbitration and Selection phases by passing the two control signals, BSY and SEL, and the SCSI I.D. to the SSI 32C453 and the local buffer, respectively. Other phases following Arbitration and Selection are command, data in, data out, status, message in and message out. Table 1 shows the various phases and their sources.

Table 2 shows the various control signal status during different SCSI phases. Being a target device, the SSI 32B451 drives these control lines out on the SCSI bus.

The SSI 32B451 requires local microprocessor supervision for successful operation over the SCSI bus. Firmware support for the local microprocessor consists of various routines. Flow charts for these routines are shown in Figures 8 and 9.

SCSI SPECIFIC INFORMATION

This information from the ANSI Standard for the Small Systems Computer Interface is provided to assist in implementing a SCSI based controller with the SSI 32B451.

TABLE 1: Bus Phase Signal Sources

BUS PHASE	SIGNALS				
	$\overline{BSY}$	$\overline{SEL}$	$\overline{C/D}$, $\overline{I/O}$, $\overline{MSG}$, REQ	ACK/ATN	DB7-DB0
Bus Free	None	None	None	None	None
Arbitration	All	Winner	None	None	SCSI ID
Selection	I & T	Initiator	None	Initiator	Initiator
Reselection	I & T	Target	Target	Initiator	Target
Command	Target	None	Target	Initiator	Initiator
Data In Target	Target	None	Target	Initiator	Target
Data Out	Target	None	Target	Initiator	Initiator
Status Target	Target	None	Target	Initiator	Target
Message In	Target	None	Target	Initiator	Target
Message	Target	None	Target	Initiator	Initiator

DEFINITIONS FOR TABLE 1

All: The signal is driven by all SCSI devices which are actively arbitrating.

SCSI ID: The SCSI ID is a unique data bit (DB) for each of the SCSI devices in the system and is driven onto the SCSI bus by each device that is actively arbitrating. The other seven data bits shall not be driven by the SCSI device. The parity bit may be asserted or undriven during arbitration but can't be driven false.

I & T: This signal is driven by the initiator, target or both as specified in the selection or reselection phase.

Initiator: If this signal is driven it can be driven only by the active initiator.

None: The signal is released meaning it is not driven by any SCSI device.

Winner: The signal shall be driven by the one SCSI device that wins arbitration.

Target: If the signal is driven it can be driven only by the active target.

TABLE 2: Signal Status, Information Transfer Phases

SIGNALS			PHASE NAME	DIRECTION OF TRANSFER
$\overline{MSG}$	$\overline{C}$/D,	$\overline{I}$/O		
1	1	1	Data Out	Initiator to Target
1	1	0	Data In	Initiator from Target
1	0	1	Command	Initiator to Target
1	0	0	Status	Initiator from Target
0	1	1	#	
0	1	0	#	
0	0	1	Message Out	Initiator to Target
0	0	0	Message In	Initiator from Target
# = Reserved for future standardization				

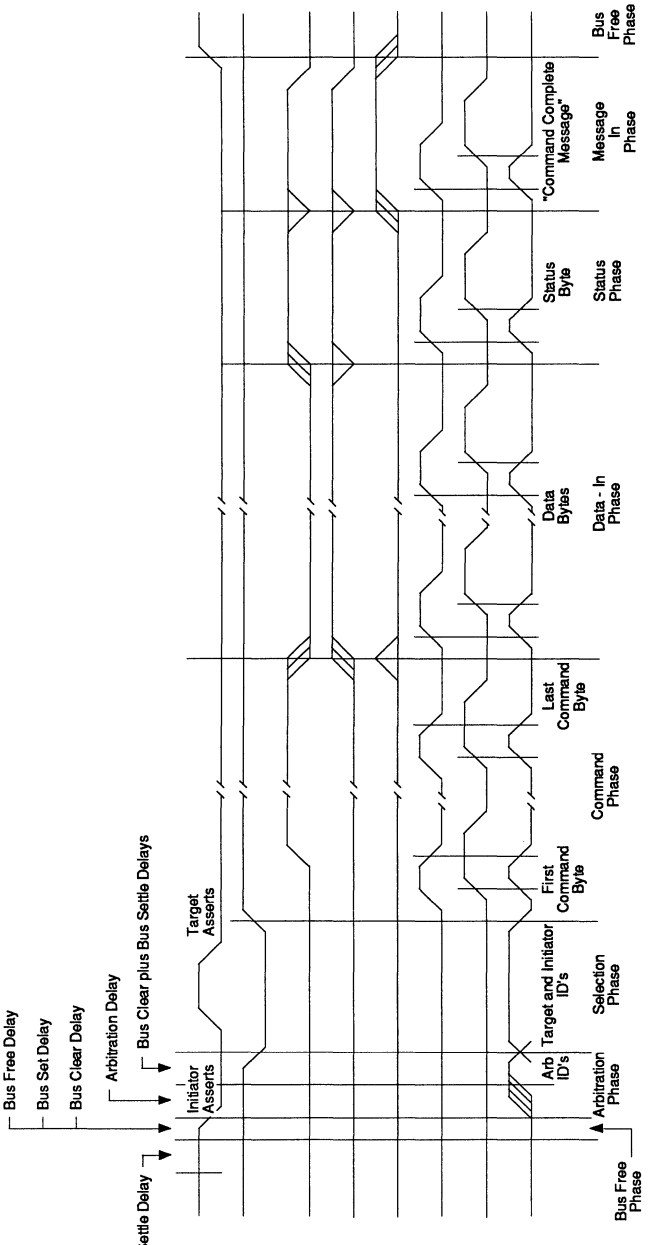


FIGURE 7: SCSI Signal Sequence Example

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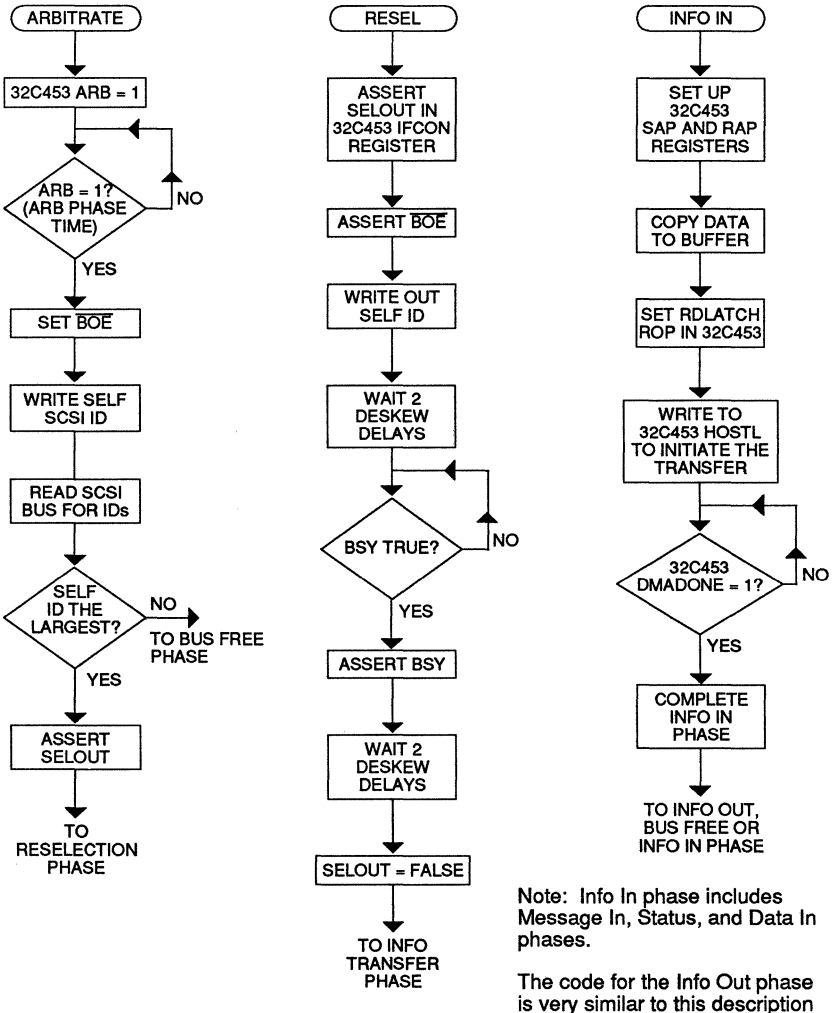


FIGURE 8: Flow Charts for Various SSI 32B451 Routines

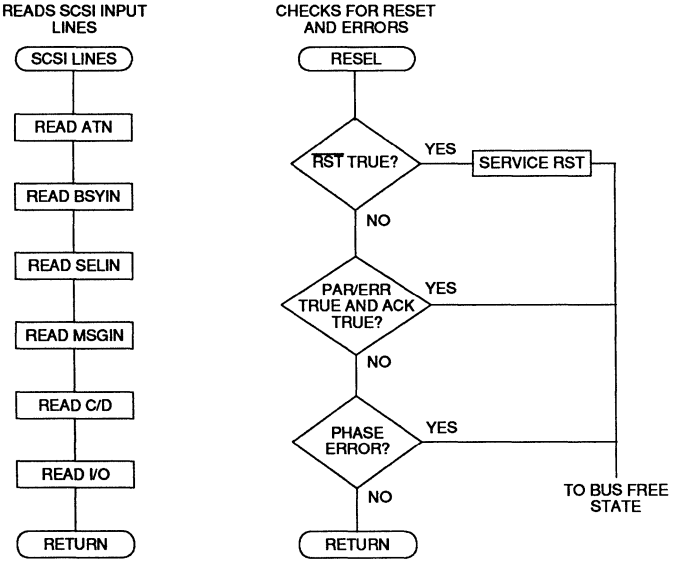


FIGURE 9: SCSI Background Routines Using SSI 32B451

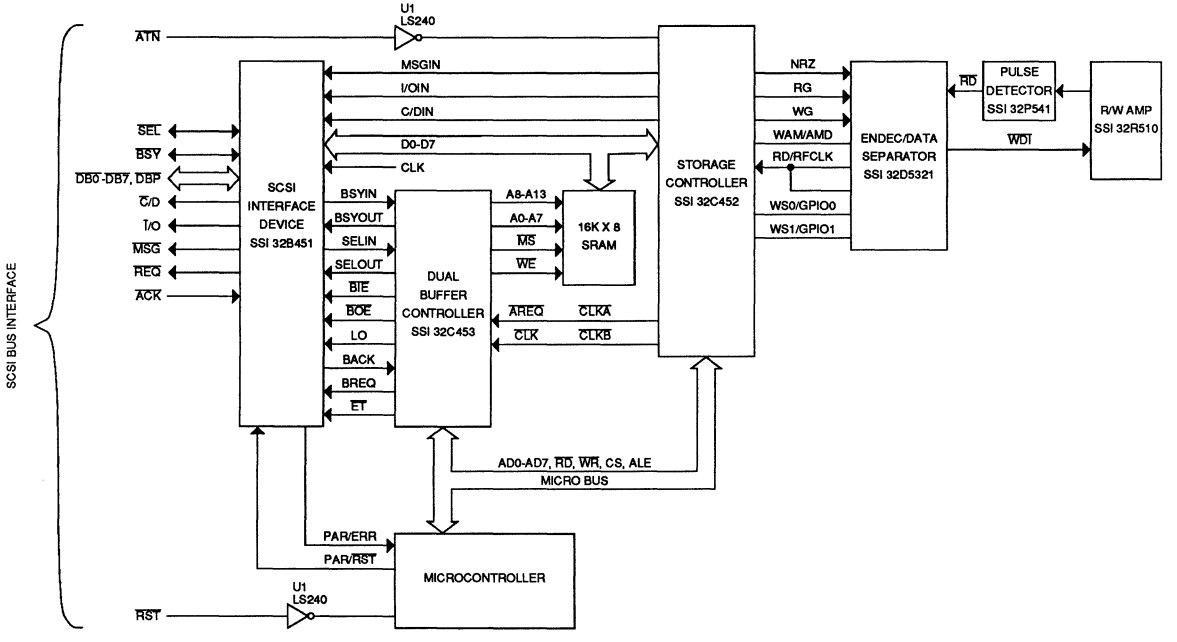
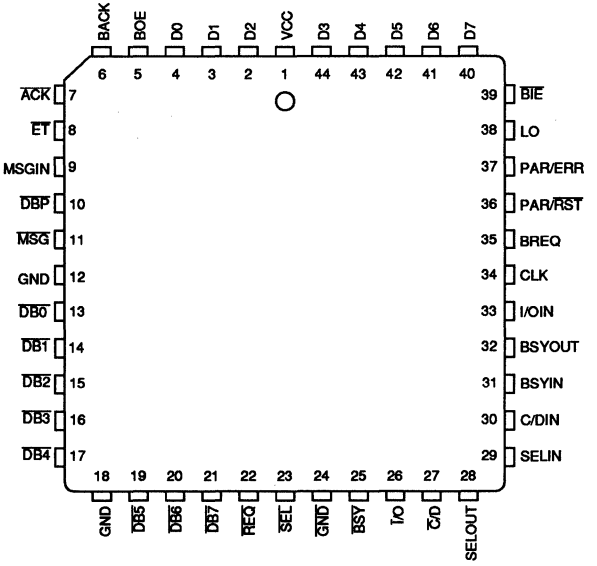


FIGURE 10: Partial Schematic for SCSI Implementation with Arbitration Support Using SSI 32B451

SSI 32B451
SCSI Controller

PACKAGE PIN DESIGNATIONS
(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.



44-pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32B451 44-pin PLCC	SSI 32B451-CH	32B451-CH

silicon systems™

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, TWX 910-595-2809

SSI 32C452
Storage Controller

August, 1988

DESCRIPTION

The SSI 32C452 Storage Controller is a CMOS device that provides the basis for an intelligent Winchester disk drive controller capable of non-interleaved data transfers at rates up to 20Mbps. When combined with a microprocessor, memory and a buffer management device such as the SSI 32C453, the SSI 32C452 implements a powerful and cost-efficient peripheral controller solution. It also has the flexibility to be used in SCSI systems.

The SSI 32C452 includes a control sequencer with a writeable control store, and configuration/status registers which can be programmed to support standard and custom interface protocols for storage controllers. Access to the control store and registers is accomplished through the microprocessor interface which is optimized for 8 bit, multiplexed address/data bus processors such as the 8085 . It also has the flexibility to interface with most standard 8-bit microprocessors. This organization allows the controller firmware to be stored in an EPROM or the host and down-loaded to the SSI 32C452, and means wide flexibility of the control functions performed by the device.

(Continued)

FEATURES

- **Supports ST506/412, ST412HP, SA100, SMD, ESDI and custom interfaces**
- **Operates with 16 MHz microprocessors**
- **Internal RAM-based control sequencer**
- **Internal user programmable ECC to 32 bits**
- **Non-interleaved data transfer to 20 Mbits/s**
- **Hard or soft sector formats**
- **Programmable sector lengths up to a full track**
- **High performance, low power CMOS device**
- **Plug and software compatible with AIC-010F Storage Controller**
- **Single 5 volt supply**
- **Available in 44-pin PLCC or 40-pin DIP package**

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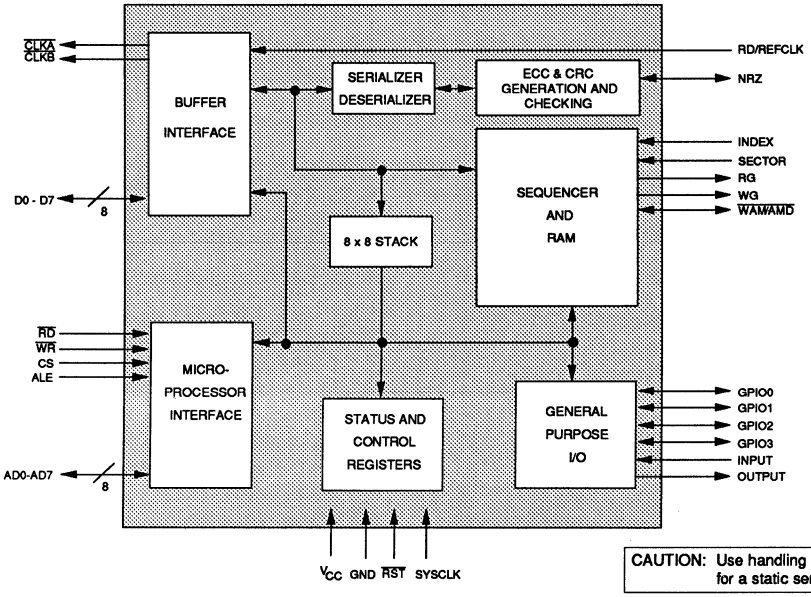
BLOCK DIAGRAM



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CAUTION: Use handling procedures necessary for a static sensitive components

DESCRIPTION (Continued)

The SSI 32C452 performs all the controller functions for the peripheral device, such as serialization/deserialization, ECC generation and checking on the data stream. It also handles overhead information such as address marks, gaps and sector ID fields. If an ECC error is detected during a read, the syndrome is saved so that defects can be corrected. The ECC polynomial and register length can be programmed or bypassed entirely so that external ECC hardware can be used.

FUNCTIONAL DESCRIPTION

The major functional elements and data paths of the SSI 32C452 are shown in the block diagram.

The SSI 32C452 performs the functions to interface a serial data storage device such as a Winchester disk drive, to a parallel bus interface for data processing on a byte wide basis. The functions necessary to accurately make this conversion are serialization/deserialization, error detection and correction, and data path control. The SSI 32C452 also has general purpose interface lines to further facilitate control of the data storage device or parallel interface. An eight byte stack allows data to be saved and reviewed by the microprocessor for error handling purposes. The internal sequencer performs most of the operations in conjunction with the control and status registers. The sequencer program is contained in internal sequencer RAM, which is easily (re)programmed providing almost infinite flexibility in communcations protocols and control features. A microprocessor effects both initialization and control of the SSI 32C452 by writing to and reading from the internal registers, sequencer RAM, stack and general purpose I/O circuitry. The microprocessor interface block of the SSI 32C452 provides the communication and control for the SSI 32C452 to the microprocessor.

The **buffer interface** includes a bidirectional data bus that exchanges data bytes between an external buffer memory and the serializer/deserializer. It generates two clocks, $\overline{\text{CLKA}}$ and $\overline{\text{CLKB}}$ which control all accesses to the buffer memory. All buffer memory cycles must be synchronous with $\overline{\text{CLKA}}$, which is derived from the RD/REFCLK input during data transfers and from SYSCLK otherwise. The internal register CLKCON contains control bits which define the relationship between these source clocks and $\overline{\text{CLKA}}$. The $\overline{\text{CLKB}}$ signal is asserted whenever a new data byte must be transferred (ie. when the serializer/deserializer is full during a read operation or empty during a write operation). The direction of the transfer is determined from the state of the read gate (RG) and write gate (WG) lines. A $\overline{\text{CLKB}}$ cycle is used to force the buffer control device (eg. an SSI 32C453) to reserve the next buffer memory access for the SSI 32C452, since peripheral transfers take precedence over the asynchronous host transfers. In order to allow host transfers to keep up with peripheral transfers, the $\overline{\text{CLKA}}$ rate selected should be at least twice the word transfer rate of the peripheral.

The **microprocessor interface** decodes microprocessor read and write requests and provides access to the appropriate register or internal memory location. Since both data and address information are carried on the multiplexed bus lines AD0-AD7, address information is latched from the bus on the falling edge of the microprocessor signal ALE (address latch enable). When $\overline{\text{CS}}$ is asserted along with either $\overline{\text{RD}}$ or $\overline{\text{WR}}$, the register whose address was previously latched is selected. The addresses and names of all the accessible registers are shown in the Register Address Map, Figure 1. The microprocessor should not read or write the sequencer RAM while the sequencer is running, since there is no circuitry to resolve conflicting accesses and incorrect sequencer operation will result.

The **status and control registers** make status information available to the microprocessor and allow the device to be configured for a wide variety of peripheral control applications. The microprocessor can monitor the status of transfers in progress and control the ECC register operation, the ECC polynomial, the clock generation hardware and the sequencer program execution. The microprocessor also has access to the sequencer's microprogram RAM so that it loads the microcode for all controller operations.

The **serializer/deserializer** circuit interfaces the parallel buffer memory bus to the serial NRZ data stream of the peripheral device. Byte synchronism is maintained with a bit ring, which is an 8 bit recirculating shift register clocked by the peripheral bit clock. During a sector write, the bit ring is initialized explicitly with a sequencer instruction. The bit ring continues to operate until the end of the field (ECC written or read) and causes $\overline{\text{CLKB}}$ to be asserted once for each data byte to be transferred. During write operations, the

sequencer may cause address marks and sync patterns to be loaded into the serializer instead of data bytes. These special patterns are contained in a sequencer instruction and are transferred to the serializer over an internal byte wide data path. During read operations, bytes of overhead information may be routed to the stack or sequencer for comparison against target values. This process is controlled by the control field (SEQCONF) in each sequencer instruction.

The eight byte recirculating **stack** may be used to capture read data for later examination by the microprocessor. Data is pushed onto the stack under sequencer control. The control bit STACKEN in the sequencer instruction field SEQCONF directly controls the stack. If more than 8 bytes are written to the stack, only the last 8 will be saved. When a data byte is read from the top of the stack by the microprocessor via the STACK register, the data is recirculated to the bottom of the stack, allowing the stack contents to be examined more than once without the use of temporary storage in the microprocessor or buffer.

Serial peripheral data is passed through a variable length shift register with programmable exclusive OR feedback that performs **ECC generation and checking**. The feedback taps for the desired ECC polynomial are selected in the four registers POLY0 - POLY24 and the polynomial length is determined by the LEN bits in ECCCON. In addition, the ECC register may be operated either under sequencer or microprocessor control. During read operations, the contents of the ECC register are compared to the actual ECC field read from the peripheral. If there is a mismatch, the error syndrome is available for error correction. The ECC polynomial may be reversed to allow hardware computation of the error location, relieving the microprocessor of the burden of this lengthy calculation. During writes to the peripheral, the computed ECC word can be appended to each data or address field. The sequencer data type field (SEQDATF) indicates when ECC bytes are to be written or checked during a peripheral transfer.

The **sequencer** controls the time critical operations of the SSI 32C452. It executes programs stored in the 28

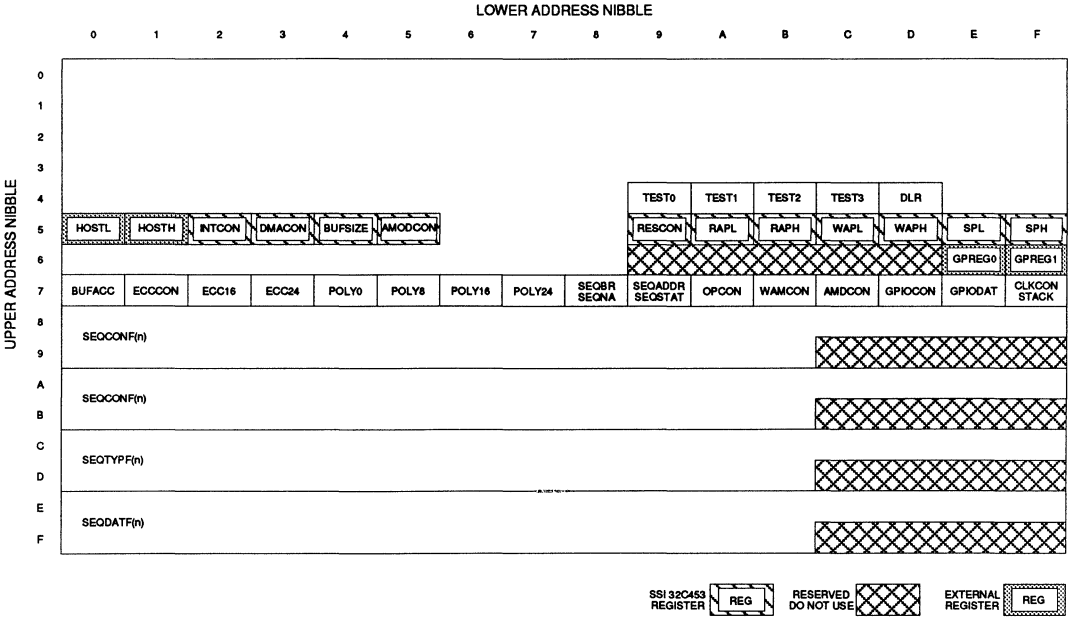


FIGURE 1: REGISTER ADDRESS MAP

FUNCTIONAL DESCRIPTION (continued)

word by 32 bit sequencer RAM, and can be programmed to support hard and soft sectored read, write, search and verify operations for a wide variety of Winchester disk drives and other peripherals. The sequencer RAM is loaded by writing to the sequencer instruction registers as outlined in the Sequencer Instructions section of this data sheet. Each instruction is comprised of four bytes. Each of the four bytes represents a function of the sequencer operation. They are address field, control field, data type field, and data field. The organization of these fields is shown in the Register Bit Map, Figure 2. The Sequencer Registers provide control from and status to the microprocessor and sequencer. They contain branch, next and start addresses, and sequencer status information. The SEQUENCER STATUS register provides informaton on the sequencer state such as whether an ECC error occurred, a compare equal or low occurred, if the branch condition or address mark is active, or whether the sequencer is halted.

The **general purpose I/O** section has four general purpose I/O lines GPIO0 - GPIO3, and the INPUT pin which are accessible through the internal general purpose input/output registers. They are available for user defined functions such as Winchester disk or host interface control. The functionality of the GPIO0 - GPIO3 pins is programmed in the GPIOCON and GPIODAT registers. They can act as I/O's asserted or read through the GPIODAT register, or they can be programmed to decode microprocessor access to addresses 6EH and 6FH eliminating the need for external decode. The INPUT signal can be programmed in the SEQADRF RAM (registers) to affect sequencer operation and the state of the pin read from the GPIODAT register. The other general purpose line, OUTPUT is controlled directly by the sequencer to synchronize it with external circuitry. The OUT bit of the GPIODAT register reflects the state of the output pin.

PIN DESCRIPTION

GENERAL

NAME	DIP	PLCC	TYPE	DESCRIPTION
VCC	40	1		POWER SUPPLY +5 volts
GND	20-21	22		GROUND
$\overline{RST}$	12	13	I	RESET - Active low signal halts the sequencer, sets output pins RG, WG, $\overline{WAM}$ and NRZ low, forces the GPIO pins into a high impedance state and resets a number of the registers as described below.
SYSCLK	13	14	I	SYSTEM CLOCK - Clock input in the range of 1.5 MHz to 16 MHz

MICROPROCESSOR INTERFACE

ALE	1	2	I	ADDRESS LATCH ENABLE - Falling edge latches register address from AD0-7 pins.
CS	29	33	I	CHIP SELECT- Active high signal enables device to respond to microprocessor read or write.

PIN DESCRIPTION (continued)

NAME	DIP	PLCC	TYPE	DESCRIPTION
$\overline{WR}$	30	34	I	WRITE STROBE - Active low signal causes the data on the address/data bus to be written to the addressed register if CS is also active.
$\overline{RD}$	31	35	I	READ STROBE - Active low signal causes the contents of the addressed register to be placed on the address/ data bus if CS is also active.
AD0-AD7	39-32	43-36	I/O	ADDRESS/DATA BUS - 8 bit bus which carries register address information and bi-directional data. These pins are high impedance when not in use.
GENERAL PURPOSE I/O				
GPIO0-3	4-7	5-8	I/O	GENERAL PURPOSE I/O LINES - These lines can be programmed as an inputs or outputs which are accessed though the GPIODAT register. They may also be programmed to serve as active low outputs which decode microprocessor accesses to the following locations: I/O pin — Alternate output decode GPIO0 — Write to 6EH GPIO1 — Read from 6EH GPIO2 — Write to 6FH GPIO3 — Read from 6FH
INPUT	8	9	I	INPUT PIN - This dedicated input line may be read through the GPIODAT register or tested directly by the control sequencer.
OUTPUT	9	10	O	OUTPUT PIN - Dedicated output line which is derived directly from the control sequencer instruction field.
DISK DRIVE INTERFACE				
INDEX	10	11	I	INDEX PULSE - Active high disk drive index pulse input, must be at least one byte time long.
SECTOR	11	12	I	SECTOR PULSE - Active high sector pulse input from disk drives that are hard sectored, must be at least one byte time long.
RG	14	15	O	READ GATE - Active high output from control sequencer enables external phase-locked loop (PLL) to synchronize to read data stream from the storage device.

PIN DESCRIPTION (continued)

DISK DRIVE INTERFACE (continued)

NAME	DIP	PLCC	TYPE	DESCRIPTION
WG	15	16	O	WRITE GATE - Active high output from control sequencer indicates valid write data to the storage device.
RD/REFCLK	26	30	I	READ/REFERENCE CLOCK - This input must be externally multiplexed to provide the PLL clock when read gate is active and the write oscillator clock at all other times. This pin must always be driven with a clock signal, even when $\overline{RST}$ is active.
NRZ	27	31	I/O	NRZ DATA - This bi-directional pin provides write data when WG is active, and must be driven with read data when RG is active. Data must be in the NRZ format.
$\overline{WAM}/\overline{AMD}$	28	32	I/O	WRITE ADDRESS MARK/ADDRESS MARK DETECT - This bi-directional pin is used to write and detect address marks. When WG is active, a low level output of one bit time on this pin indicates that an address mark must be written. When RG is active, the peripheral must provide an active low input to indicate the detection of an address mark.

BUFFER INTERFACE

$\overline{CLKA}$	2	3	O	CLOCK A - Clock signal which initiates host or controller accesses to the buffer memory on its falling edge. When either RG or WG is active, this output is derived from RD/REFCLK. At all other times it is derived from SYSCLK. The clock source is divided by 2 or 4 as programmed in the CLKCON register.
$\overline{CLKB}$	3	4	O	CLOCK B - This clock is used to reserve $\overline{CLKA}$ cycles for SSI 32C452 data transfers. An active low pulse spanning a falling edge of $\overline{CLKA}$ indicates that the next falling edge on $\overline{CLKA}$ will be used by the SSI 32C452 to access the buffer memory.
D0-D7	16-19 22-25	18-21 25-28	I/O	BUFFER DATA BUS - Bi-directional data bus that carries data to and from the buffer memory. Bus cycles are controlled by $\overline{CLKA}$ and $\overline{CLKB}$. Direction of the transfer is determined by RG and WG. Note: refer to pin diagram for exact ordering of the pins.
No connects on PLCC package: 17, 23, 24, 29, 44				

REGISTER	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0	READ/ WRITE
TEST0	49H	SEQUENCER NEXT ADDRESS FIELD								R
TEST1	4AH	SEQUENCER CONTROL FIELD								R
TEST2	4BH	SEQUENCER COUNT/DATA TYPE FIELD								R
TEST3	4CH	SEQUENCER DATA FIELD								R
DLR	4DH	DATA LATCH REGISTER								R
BUFACC	70H	BUFFER MEMORY BYTE								R/W
ECCCON	71H	LEN1	LEN0	RESET	SECTBR	CLRECC	FEEDINH	ECCSHIFT	ECCIN	R/W
ECC16	72H	ECC23	ECC22	ECC21	ECC20	ECC19	ECC18	ECC17	ECC0/16	R
ECC24	73H	ECC31	ECC30	ECC29	ECC28	ECC27	ECC26	ECC25	ECC24	R
POLY0	74H	F7	F6	F5	F4	F3	F2	F1	F0	R/W
POLY8	75H	F15	F14	F13	F12	F11	F10	F9	F8	R/W
POLY16	76H	F23	F22	F21	F20	F19	F18	F17	F16	R/W
POLY24	77H	UNUSED	F30	F29	F28	F27	F26	F25	F24	R/W
SEQBR	78H	UNUSED			BRADR4	BRADR3	BRADR2	BRADR1	BRADR0	W
SEQNA	78H	TEST POINTS			NADR4	NADR3	NADR2	NADR1	NADR0	R
SEQADDR	79H	UNUSED			STADR4	STADR3	STADR2	STADR1	STADR0	W
SEQSTAT	79H	AMACTIVE	DATATRANS	BRACTIVE	STOPPED	UNUSED	ECCERR	COMPLO	COMPEQ	R
OPCON	7AH	CARRYINH	UNUSED	TRANSINH	SEARCHOP	SYNDET	NRZDAT	SECTORP	INDEXP	R/W
WAMCON	7BH	AM7 - AM0								R/W
AMDCON	7CH	AMD7 - AMD0								R/W
GPIOCON	7DH	RGFSEL	WGFSEL	RGESEL	WGESEL	GPDIR3	GPDIR2	GPDIR1	GPDIR0	R/W
GPIODAT	7EH	UNUSED		OUT	INP	GP3	GP2	GP1	GP0	R/W
CLKCON	7FH	CLKF2	CLKF1	UNUSED	CLKFO	CLKINH	SYN2	SYN1	SYN0	W
STACK	7FH	TOP OF STACK								R
SEQADDRF	80H	BRCON2	BRCON1	BRCON0	NEXT4	NEXT3	NEXT2	NEXT1	NEXT0	R/W
	9BH									
SEQCONF	A0H	SETWG	SETRG	RESWG	STACKEN	NRZINH	OUTPIN	COMPEN	DATEN	R/W
	BBH									
SEQTYPF	C0H	CNT7/ DTYP2	CNT6/ DTYP1	CNT5/ DTYP0	CNT4	CNT3	CNT2	CNT1	CNTO	R/W
	DBH									
SEQDATF		DATA FIELD								R/W

FIGURE 2: REGISTER BIT MAP

REGISTER DESCRIPTION

The microprocessor which controls the system has access to all the SSI 32C452 registers and sequencer RAM through its external memory address space. The SSI 32C452 and its companion device, the SSI 32C453 Dual Port Buffer Controller, are designed to occupy a single 256 byte page. The 8 bit page address is latched from pins AD0-AD7 on a falling edge of ALE and remains valid until the next ALE falling edge.

The external registers described at the end of this section are not implemented in either the SSI 32C452 or SSI 32C453, and are assumed to be implemented in external hardware. These external registers are not required for use with the SSI 32C452, but are included as applications information.

ECC REGISTERS

The core of the ECC circuit is a 32 bit shift register whose effective length may be programmed to be 16, 24 or 32 bits. This is accomplished in hardware by directing the input data to stage 16, 8 or 0 of the ECC shift registers, ECC16 and ECC24, while its output is always bit 31, which is bit ECC31 of register ECC24.

The ECC polynomial to be implemented is programmed by the user into the ECC feedback registers, POLY0, POLY8, POLY16 and POLY24. Each bit in these registers enables or disables exlusive OR feedback to the output of the corresponding shift register stage. The feedback signal is the exclusive OR of the serial data stream with the output of shift register stage 31. An override bit in ECCCON forces normal shift register operation, regardless of the settings of the feedback control bits.

When WG or RG are active, the ECC shift register input is the serial read or write data and the shift clock is RD/REFCLK. When an ECC word is being written, feedback is disabled and the shift register output is substituted for the data stream. At other times the microprocessor may set the ECCIN bit explicitly and cause a single shift register clocking to occur. For further information on implementing an ECC polynomial see the Applications Information Section at the end of this data sheet.

ECCCON **71H** **Read/Write**

ECC CONTROL WORD		
BIT	**NAME**	**DESCRIPTION**
0	ECCIN	ECC SERIAL INPUT - When both RG and WG are inactive, this bit becomes the input bit for the ECC shift register. The RD/REFCLK must always be active for correct operation of the device.
1	ECCSHIFT	ECC SHIFT CONTROL - When both RG and WG are inactive, a single shift of the ECC register will occur when this bit is set. It is automatically cleared again when the shift is complete.
2	FEEDINH	ECC FEEDBACK INHIBIT - When this bit is set all feedback is inhibited and the ECC register functions as a simple shift register of the selected length.
3	CLRECC	CLEAR ECC - If this bit is set when either RG or WG are active, the ECC syndrome will be cleared at the end of the read/write operation. If both are inactive, the syndrome will be cleared immediately.
4	SECTBR	ENABLE SECTOR BRANCH - If the sequencer "branch on index or sector" instruction is executed and SECTBR is set, the sequencer will recognize the branch condition as true if either the INDEX or the SECTOR pin is active. If SECTBR is cleared, then the sequencer will only recognize the branch condition if the INDEX pin is active.

ECC REGISTERS (continued)

BIT	NAME	DESCRIPTION
5	RESET	CHIP RESET - When this bit is set, the SSI 32C452 will be held in its reset state. This bit is set when $\overline{RST}$ is true.
6-7	LEN0-LEN1	ECC REGISTER LENGTH - These two bits select the ECC register length as follows: LEN1 LEN0 0 0 16 bit register 0 1 24 bit register 1 0 illegal combination 1 1 32 bit register
Reset State: ECCCON= 20H (ie. RESET=1)		

ECC16 **72H** **Read only**

ECC DATA		
BIT	**NAME**	**DESCRIPTION**
0	ECC0/16	ECC REGISTER LEADING BITS - This bit reflects the OR of all the ECC register bits from the input stage through bit 16. For 16 bit operation, this is bit 16. For 24 bit operation this is bit 8 + bit 9 + .. + bit 16. For 32 bit operation, this is bit 0 + bit 1 + ... + bit 16.
1-7	ECC17-ECC23	ECC REGISTER BITS - These bits reflect the output of ECC shift register stages 17 to 23.
Reset State: Unknown		

ECC24 **73H** **Read only**

ECC DATA		
BIT	**NAME**	**DESCRIPTION**
0-7	ECC24-ECC31	ECC REGISTER BITS - These bits reflect the output of ECC shift register stages 24 to 31.
Reset State: Unknown		

ECC REGISTERS (continued)

POLY0 **74H** **Read/Write**

ECC POLYNOMIAL		
BIT	**NAME**	**DESCRIPTION**
0-7	F0-F7	ECC POLYNOMIAL FEEDBACK - These bits enable or disable exclusive OR feedback of both the shift register output (bit 31) and the serial input to the output of shift register stages 0 to 7. These settings may be overriden by the FEEDINH bit in ECCCON. For ECC register lengths of 16 or 24 bits, F0-F7 are irrelevant.
Reset State: POLY0=00H		

POLY8 **75H** **Read/Write**

ECC POLYNOMIAL		
BIT	**NAME**	**DESCRIPTION**
0-7	F8-F15	ECC POLYNOMIAL FEEDBACK - These bits enable or disable exclusive OR feedback to the output of shift register stages 8 to 15. For register lengths of 16 bits, F8-F15 are irrelevant.
Reset State: POLY8=00H		

POLY16 **76H** **Read/Write**

ECC POLYNOMIAL		
BIT	**NAME**	**DESCRIPTION**
0-7	F16-F23	ECC POLYNOMIAL FEEDBACK - These bits enable or disable exclusive OR feedback to the output of shift register stages 16 to 23.
Reset State: POLY16=00H		

POLY24 **77H** **Read/Write**

ECC POLYNOMIAL		
BIT	**NAME**	**DESCRIPTION**
0-6	F24-F30	ECC POLYNOMIAL FEEDBACK - These bits enable or disable exclusive OR feedback to the output of shift register stages 24 to 30.
7	unused	
Reset State: POLY24=00H		

SEQUENCER STATUS AND CONTROL REGISTERS

The sequencer controls all the time-critical interactions with the peripheral storage device being controlled by the SSI 32C452. The instructions directly control disk drive interface lines, provide data for writing or comparison, determine the number of bytes handled and control the sequence of instruction execution. It is programmed by the user for maximum capability and variability. There are 28 instructions which are 32 bits wide. They are divided in to 4 byte wide fields. These fields are sequencer address, control, data type and data fields. These may be further divided into subfields as described in detail below. Examples are shown in the Applications Information section at the end of this data sheet.

The next address field of the sequencer instruction contains address and branching information. Each instruction is executed for the duration of the number of byte times specified in its count field. The specified count is loaded into a down counter which clocks every 8 bit times. When the counter underflows execution of that instruction is terminated. A carry inhibit feature allows the counter to wrap around to a full count for fields which are more than 256 bytes long. Execution is passed to the instruction at the specified next address, unless a branch condition is specifed in the instruction (eg. ECC error or successful data comparison). In that case, execution passes to the address specified in the SEQBR register. Sequencer operation may also be conditionally stopped. The sequencer will always stop if execution passes to address 1FH, which is outside of the 28 word instruction control store.

The control field of the sequencer instruction is used to specify the state of RG and WG, to move data to the stack and to select data transfer or data comparison operations. The count field sets the duration of each instruction in byte times and is also used to select the type of data written, such as address marks or ECC bytes.

SEQBR 78H Write only

SEQUENCER BRANCH ADDRESS		
BIT	**NAME**	**DESCRIPTION**
0-4	BRADR0 - BRADR4	BRANCH ADDRESS BITS - When a sequencer instruction with a branch condition is finished (ie. the specified number of byte times have elapsed) and the specified condition did occur, execution will resume at this 5 bit address.
5-7	unused	
Reset State: Unknown		

SEQNA 78H Read only

SEQUENCER NEXT ADDRESS		
BIT	**NAME**	**DESCRIPTION**
0-4	NADR0 - NADR4	NEXT ADDRESS BITS- This reflects the 5 bit next address field of the sequencer instruction currently being executed. After the specified byte count, execution will proceed at this address provided no branch conditions occur.
5-7		Internal test points
Reset State: Unknown		

SEQUENCER STATUS AND CONTROL REGISTERS (continued)

SEQADDR 79H Write only

SEQUENCER START ADDRESS		
BIT	**NAME**	**DESCRIPTION**
0-4	STADR0 - STADR4	SEQUENCER START ADDRESS BITS - If the sequencer is currently halted, writing this register with an address in the range 00H to 1BH will cause sequencer execution to commence at that address. If this register is written with 1FH , the sequencer will halt.
5-7	unused	
Reset State: 00H		

SEQSTAT 79H Read only

SEQUENCER STATUS		
BIT	**NAME**	**DESCRIPTION**
0	COMPEQ	COMPARE EQUAL - When a sequencer instruction enables the comparison operation, this bit reflects the result of all the byte comparisons performed (ie. if it is set then all bytes compared so far have been equal.) If RG is enabled, the comparisons occur between the instruction's data field and the data bytes being read (or buffer memory if the SEARCHOP bit in OPCON is true as well).
1	COMPLO	COMPARE LOW - Similar to COMPEQ, except that it indicates that in all comparisons the data field was smaller than the compared byte.
2	ECCERR	ECC ERROR - This bit is set during RG active, upon reading the last ECC bit, if there was an error in the data read. The error syndrome will be stored in the ECC registers.
3	not used	
4	STOPPED	SEQUENCER STOPPED - This bit is set when the sequencer is stopped and its instruction address is 1FH.
5	BRACTIVE	BRANCH ACTIVE - This is set when the branch condition specified in the current instruction has been satisfied. This means that the next address used will be taken from the SEQBR register. This bit is reset when the microprocessor reads this register.
6	DATATRANS	DATA TRANSFER - This bit is set when the current sequencer instruction is causing data to be transferred between the buffer memory and the peripheral device. This distinguishes the activity from a search or verification operation.
7	AMACTIVE	ADDRESS MARK ACTIVE - This bit is set when the controller reads or writes an address mark or sync byte. It is reset after the ECC bytes are read or written, or when the sequencer is halted.
Reset State: 00H		

SEQUENCER INSTRUCTION REGISTERS

The 4 fields of 8 bits comprising a single sequencer instruction are detailed below. They are presented as arrays of 28 bytes each, corresponding to the 28 instructions at sequencer addresses 0 to 1BH.

SEQADRF(n) 80H-9BH Read/Write

SEQUENCER ADDRESS FIELD ARRAY			
BIT	**NAME**	**DESCRIPTION**	
0-4	NEXT0-NEXT4	NEXT ADDRESS FIELD - This 5 bit field specifies the address of the next instruction to be executed when the current instruction has continued for the specified number of bytes.	
5-7	BRCON0 -BRCON2	BRANCH CONTROL FIELD - This 3 bit field specifies the branch condition for the current instruction. When a branch condition is satisfied, execution of the current instruction is not curtailed. It continues to execute for the full byte count specifed, and then the sequencer proceeds with execution of the address specified in SEQBR. The branch condition used depends on the state of RG and data type field (see SEQTYPF). If RG is true and ECC bytes are being read, the following branch conditions apply:	
		BRCON2/1/0=	000 No branch
			001 Stop on ECC error
			010 Stop on comparison error
			011 Stop on ECC or comparison error
			100 Branch on good ECC and comparison
			101 Branch on ECC error
			110 Branch on comparison error
			111 Branch on ECC or comparison error
		Otherwise, the branch conditions are:	
		BRCON2/1/0=	000 No branch
			001 Stop if INPUT pin active
			010 Stop if INDEX or SECTOR pin active (see SECTBR bit of register ECCCON).
			011 Stop if comparison error
			100 Branch on carry (from byte counter).
			101 Branch on ECC error
			110 Branch if INDEX or SECTOR pin active (see SECTBR bit of register ECCCON).
			111 Branch on comparison error
Reset State: The contents of the sequencer RAM are unchanged.			

SEQUENCER INSTRUCTION REGISTERS (continued)

SEQCONF(n) A0H-BBH Read/Write

SEQUENCER CONTROL FIELD ARRAY		
BIT	**NAME**	**DESCRIPTION**
0	DATEN	DATA TRANSFER ENABLE - When this bit is set, the SSI 32C452 will generate $\overline{CLKB}$ requests to transfer data bytes to or from buffer memory, depending on whether WG or RG is active.
1	COMPEN	COMPARE ENABLE - When this bit is set and RG is active, read data bytes from the peripheral will be compared with the instruction data field (SEARCHOP reset in the OPCON register) or the buffer memory data (SEARCHOP set). The results of the comparisons are OR'ed together for the duration of the instruction and can be used for a branch condition or tested by the microprocessor.
2	OUTPIN	OUPUT PIN CONTROL - This bit appears on the OUTPUT pin and may be used to synchronize external circuitry to the sequencer.
3	NRZINH	NRZ DATA INHIBIT - When RG is active and this bit is set, the NRZ data input will be ignored. This is useful while external data recovery circuits start up.
4	STACKEN	STACK WRITE ENABLE - While this bit is set, bytes of NRZ data are pushed onto the recirculating stack.
5	RESWG	RESET WRITE GATE - This bit causes the WG line to go inactive 4 bit times after the current instruction is finished (byte counter reaches 0).
6	SETRG	SET READ GATE - Provided WG is inactive, this bit sets RG, which will remain active until the ECC information is read or the sequencer is halted.
7	SETWG	SET WRITE GATE - When this bit is set and an instruction executed, the WG line will be activated after a delay of 4 bit times. WG will remain active until cleared by the RESWG bit or the sequencer is halted. WG will not be activated if RG is already active.
Reset State: The contents of the sequencer RAM are unchanged.		

SEQTYPF(n) C0H-DBH Read/Write

SEQUENCER DATA TYPE FIELD ARRAY		
BIT	**NAME**	**DESCRIPTION**
0-4	CNT0-CNT4	COUNT FIELD - The current sequencer instruction is executed for the number of byte times specified by the count field. If the DATEN bit is set, the count is specified as an 8 bit quantity (CNT0-CNT7). If DATEN is reset, the count is specified as a 5 bit quantity (CNT0-CNT4), and the upper three bits of this instruction field are interpreted as data type bits, described below.

SEQUENCER INSTRUCTION REGISTERS (continued)

BIT	NAME	DESCRIPTION
5	CNT5/DTYP0	COUNT BIT 5 OR DATA TYPE 0 - When this bit is interpreted as a data type bit, it is used to initialize the bit ring with a single 1. This will occur at the next $\overline{CLKA}$ cycle. This starts $\overline{CLKB}$ so that write data bytes will be fetched from buffer memory. The bit ring will be cleared after the ECC is written.
6	CNT6/DTYP1	COUNT BIT 6 OR DATA TYPE BIT 1 - When this bit is interpreted as a data type bit, it indicates that ECC information is being read or written.
7	CNT7/DTYP2	COUNT BIT 7 OR DATA TYPE BIT 2 - When this bit is being interpreted as a data type bit it indicates that an address mark is being written.
Note: When DATEN is reset, and CNT5/DTYP0, CNT6/DTYP1 and CNT7/DTYP2 are being interpreted as data type select bits, the upper 3 bits of the byte counter are forced to 0 regardless of the settings of the data type bits. When all 3 data type bits are 0, the data field is interpreted as normal binary data.		
Reset State: The contents of the sequencer RAM are unchanged		

SEQDATF E0H-FBH Read/Write

SEQUENCER DATA FIELD ARRAY		
BIT	**NAME**	**DESCRIPTION**
0-7	DAT0-DAT7	DATA FIELD - When RG is active, the byte in this field is used for comparison operations. If WG is active, DATATRANS is set and TRANSINH (Transfer Inhibit bit in OPCON register) is set, the write data will come from this field. This allows the sequencer to generate the necessary overhead bytes while writing a sector.
Reset State: The contents of the sequencer RAM are unchanged.		

DISK DRIVE INTERFACE REGISTERS

The disk drive interface registers provide control and status for the interface of the SSI 32C452 to the disk drive (peripheral device), and for data transfer to the buffer or host.

OPCON 7AH Read/Write

OPERATION CONTROL WORD		
BIT	**NAME**	**DESCRIPTION**
0	INDEXP	INDEX PULSE DETECTED - This bit is set when an index pulse is encountered and reset each time the register is read. The bit will be reset even if the INDEX pin is true during the access.
1	SECTORP	SECTOR PULSE DETECTED - This bit is set when a sector pulse is encountered and cleared each time the register is read. The bit will be cleared even if the SECTOR pin is true during the read access. This bit is only used with hard-sectored disk drives.

DISK DRIVE INTERFACE REGISTERS (continued)

BIT	NAME	DESCRIPTION
2	NRZDAT	NRZ DATA IN - This bit is set when a rising edge is detected on the NRZ pin and RG is active. It is reset when the register is read.
3	SYNDET	SERIAL DATA SYNCHRONIZATION DETECT - Indicates that the bit ring is synchronized on byte boundaries, following detection of an address mark.
4	SEARCHOP	SEARCH OPERATION - Setting this bit will cause comparisons to occur between the contents of the buffer memory and the read data bytes from the peripheral. If SEARCHOP is reset, then read data bytes will be compared to the sequencer instruction data field.
5	TRANSINH	DATA TRANSFER INHIBIT - If WG is active and this bit is set, then the write data will come from the sequencer instruction data field instead of the buffer memory. If RG is active and this bit is set, then the read data bytes are used for comparisons only and are not written to buffer memory. Setting this bit will suppress $\overline{\text{CLKB}}$ so that no buffer memory transfers occur.
6	Unused	
7	CARRYINH	SEQUENCER COUNTER CARRY INHIBIT - When this bit is set, the sequencer will not detect a carry (underflow) in its byte counter. This bit is reset when a carry occurs.
Reset State: Unknown		

WAMCON 7BH Read/Write

WRITE ADDRESS MARK CONTROL		
BIT	**NAME**	**DESCRIPTION**
0-7	AM0-AM7	ADDRESS MARK BITS - When WG is active and the sequencer instruction specifies that an address mark is to be written (DATATRANS is reset, DTYP2 is set) the bits AM0-AM7 will be shifted out on the $\overline{\text{WAM}}/\overline{\text{AMD}}$ pin. The pattern is delayed by two bit times to compensate for the encoder delay.
Reset State: Unknown		

AMDCON 7CH Read/Write

ADDRESS MARK DETECT CONTROL		
BIT	**NAME**	**DESCRIPTION**
0-7	AMD0-AMD7	ADDRESS MARK DETECT CONTROL - When RG and the $\overline{\text{WAM}}/\overline{\text{AMD}}$ input are active, the NRZ data stream is compared to the contents of this register. Byte synchronization is established when a match occurs. The number of bits used in the comparison is determined in the CLKCON register.
Reset State: Unknown		

DISK DRIVE INTERFACE REGISTERS (continued)

CLKCON 7FH Write only

CLOCK CONTROL			
BIT	**NAME**	**DESCRIPTION**	
0-2	SYN0-SYN2	SYNC COMPARE CONTROL - These 3 bits determine which bits in register AMDCON are used when looking for the sync byte, as follows:	
		SYN2/1/0 =	000 Bit 7 used
			001 Bits 7,6 used
			010 Bits 7,6,5 used
			011 Bits 7,6,5,4 used
			100 Bits 7,6,5,4,3 used
			101 Bits 7,6,5,4,3,2 used
			110 Bits 7,6,5,4,3,2,1 used
			111 All bits used
3	CLKINH	CLOCK INHIBIT - When this bit is set, $\overline{CLKA}$ and $\overline{CLKB}$ are forced to a high impedance state.	
4	CLKF0	CLOCK FREQUENCY SELECT - This bit sets the relationship between $\overline{CLKA}$ and RD/REFCLK when data transfers are in progress. When it is set, $\overline{CLKA}$ will be 1/4 the RD/REFCLK frequency and when it is reset, $\overline{CLKA}$ will be 1/2 the RD/REFCLK frequency.	
5	Unused		
6-7	CLKF1-CLKF2	CLOCK FREQUENCY SELECT - These bits determine the relationship between the frequency of $\overline{CLKA}$ and SYSCLK when no data transfers are in progress, as follows:	
		CLKF2/CLKF1=	00 1/4 frequency
			01 1/2 frequency
			10 same frequency
			11 illegal combination
Reset State: Unknown			

STACK 7FH Read only

TOP OF STACK
This register provides the microprocessor read access to the top of the 8 byte stack. Each read operation causes the stack data to recirculate, with the top of the stack moving to the bottom. When the sequencer writes data to the stack, the byte on the bottom of the stack is lost.

GENERAL PURPOSE INPUT/OUTPUT REGISTERS

GPIOCON 7DH Read/Write

GENERAL PURPOSE I/O CONTROL		
BIT	**NAME**	**DESCRIPTION**
0-3	GPDIR0 -GPDIR3	GENERAL PURPOSE I/O LINE DIRECTION- These bits program the direction of lines GPIO0 to GPIO3. The direction bits are set for outputs and reset for inputs.
4	W6ESEL	$\overline{W6E}$ SELECT - If this bit is set along with GPDIR0, the GPIO0 pin becomes an active low output signal decoding a microprocessor write to location 6EH.
5	R6ESEL	$\overline{R6E}$ SELECT - If this bit is set along with GPDIR1, the GPIO1 pin becomes an active low output signal decoding a microprocessor read from location 6EH.
6	W6FSEL	$\overline{W6F}$ SELECT - If this bit is set along with GPDIR2, the GPIO2 pin becomes an active low output signal decoding a microprocessor write to location 6FH.
7	R6FSEL	$\overline{R6F}$ SELECT - If this bit is set along with GPDIR3, the GPIO3 pin becomes an active low output signal decoding a microprocessor read from location 6FH.
Reset State: Unknown		

GPIODAT 7EH Read/Write

GENERAL PURPOSE I/O DATA		
BIT	**NAME**	**DESCRIPTION**
0-3	GP0-GP3	GENERAL PURPOSE I/O PIN STATUS - These bits represent the state or output data for the GPIO0 to GPIO3 pins, depending on the direction programmed in the GPIOCON register.
4	INPUT	INPUT PIN STATUS - This bit reflects the data on the INPUT pin.
5	OUT	OUTPUT PIN STATUS - This bit reflects the data on the OUTPUT pin. The OUTPUT pin is actually written to by the sequencer.
6-7	Unused	
Note: The GPIOCON register must be initialized before GPIODAT is accessed.		
Reset State: Unknown		

MICROPROCESSOR INTERFACE REGISTERS

DLR **4DH** **Read only**

DATA LATCH REGISTER
When a microprocessor read from location 70H is detected, the data on the buffer memory bus (D0-D7) is latched by the SSI 32C452 into the DATA LATCH REGISTER. When the microprocessor accesses DLR this data is placed on the address/data bus (AD0-AD7).

SPECIAL ADDRESS DECODES 50H-51H **Read/Write**

Special decodes
Microprocessor accesses to these locations will cause the address/data bus (AD0-AD7) and the buffer data bus (D0-D7) to be bridged together internally (see external register description).

BUFACC **70H** **Read/Write**

BUFFER ACCESS
Microprocessor accesses to this location cause the address/data bus (AD0-AD7) and the buffer data bus (D0-D7) to be bridged together internally. If a read cycle is performed, the data present will be latched into register DLR as well.

TEST REGISTERS
These registers may not be accessed while the sequencer is running.

TEST0 **49H** **Read only**

TEST REGISTER 0
Access to the Next Address field of the current sequencer instruction.

TEST1 **4AH** **Read only**

TEST REGISTER 1
Access to the Control field of the current sequencer instruction.

TEST2 **4BH** **Read only**

TEST REGISTER 2
Access to the Count/Data Type field of the current sequencer instruction.

TEST3 **4CH** **Read only**

TEST REGISTER 3
Access to the Data field of the current sequencer instruction.

EXTERNAL REGISTERS (for reference only)

HOSTL **50H** **Read/Write**

HOST BUS (LOWER BYTE)
External hardware may be used to connect the lower byte of the host bus to the buffer memory when this address is accessed.

HOSTH **51H** **Read/Write**

HOST BUS (UPPER BYTE)
External hardware may be used to connect the upper byte of the host bus to the buffer memory when this address is accessed.

GPREG0 **6EH** **Read/Write**

GENERAL PURPOSE REGISTER 0
Systems which need extra I/O on the microprocessor data bus may take advantage of the strobes available on pins GPIO0 (write) and GPIO1 (read) to add an expansion port at this address.

GPREG1 **6FH** **Read/Write**

GENERAL PURPOSE REGISTER 1
Systems which need extra I/O on the microprocessor data bus may take advantage of the strobes available on pins GPIO2 (write) and GPIO3 (read) to add an expansion port at this address.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Ambient Temperature Under Bias	0 to 70	° C
Storage Temperature	-65 to 150	° C
Voltage On Any Pin With Respect To Ground	GND -0.5 or VCC + 0.5	V
Power Supply Voltage	7.0	V
Max Current Injection	25	mA

NOTE: Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC Supply Voltage		4.75		5.25	V
TA Operating Free Air Temp.		0		70	° C
Input Low Voltage		0		0.4	V
Input High Voltage		2.4		VCC	V

D. C. CHARACTERISTICS

TA = 0°C to 70°C, VCC = 5V ± 5%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VIL Input Low Voltage		-0.5		0.8	V
VIH Input High Voltage		2.0		VCC + .5	V
VOL Output Low Voltage	IOL = 4mA for			0.45	V
	IOL = 2mA all others				
VOH Output High Voltage	IOH = 400mA			2.4	V
ICCS Supply Current Standby	Inputs at GND or VCC			25	mA
ICC Supply Current				85	mA
Power Dissipation				500	mW

D. C. CHARACTERISTICS (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
IL	Input Leakage	0V < Vin < VCC	-10		10	µA
IOL	Output Leakage	0.45V < Vout < VCC	-10		10	µA
Cin	Input Capacitance				10	pF
Cout	Output Capacitance				10	pF

A. C. TIMING CHARACTERISTICS

TA = 0°C to 70°C, VCC = 5v ± 5%, unless otherwise specified.
Load conditions for all pins - 30pF. Timing measurements are made at 50% of rising or falling edge.
Note: ↓ indicates falling edge; ↑ indicates rising edge.

MICROPROCESSOR INTERFACE TIMING (See Figure 3)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
S	SYSCLK Period		50			ns
S/2	SYSCLK Assert to De-assert		18			ns
S/2	SYSCLK Rise and fall	Sr = Sf, S = 60 ns			5	ns
Ta	ALE Width		45			ns
Taw	ALE ↓ to $\overline{WR}$ ↓		25			ns
Tar	ALE ↓ to $\overline{RD}$ ↓		25			ns
Tw	$\overline{WR}$ Width		200			ns
Tr	$\overline{RD}$ Width		200			ns
As	AD0 - AD7 in Valid to ALE ↓		7.5			ns
Ah	ALE ↓ to AD0 - AD7 in Invalid		20			ns
Cs	CS ↑ to ALE ↓		7.5			ns
Ch	$\overline{RD}$ ↑ or $\overline{WR}$ ↑ to CS ↓		0			ns
Wds	AD0 - AD7 in Valid to $\overline{WR}$ ↑		70			ns
Wdh	$\overline{WR}$ ↑ to AD0 - AD7 in Invalid		10			ns
Tda	$\overline{RD}$ ↓ to AD0 - AD7 out Valid				145	ns
Tdh	$\overline{RD}$ ↑ to AD0 - AD7 out Invalid				50	ns

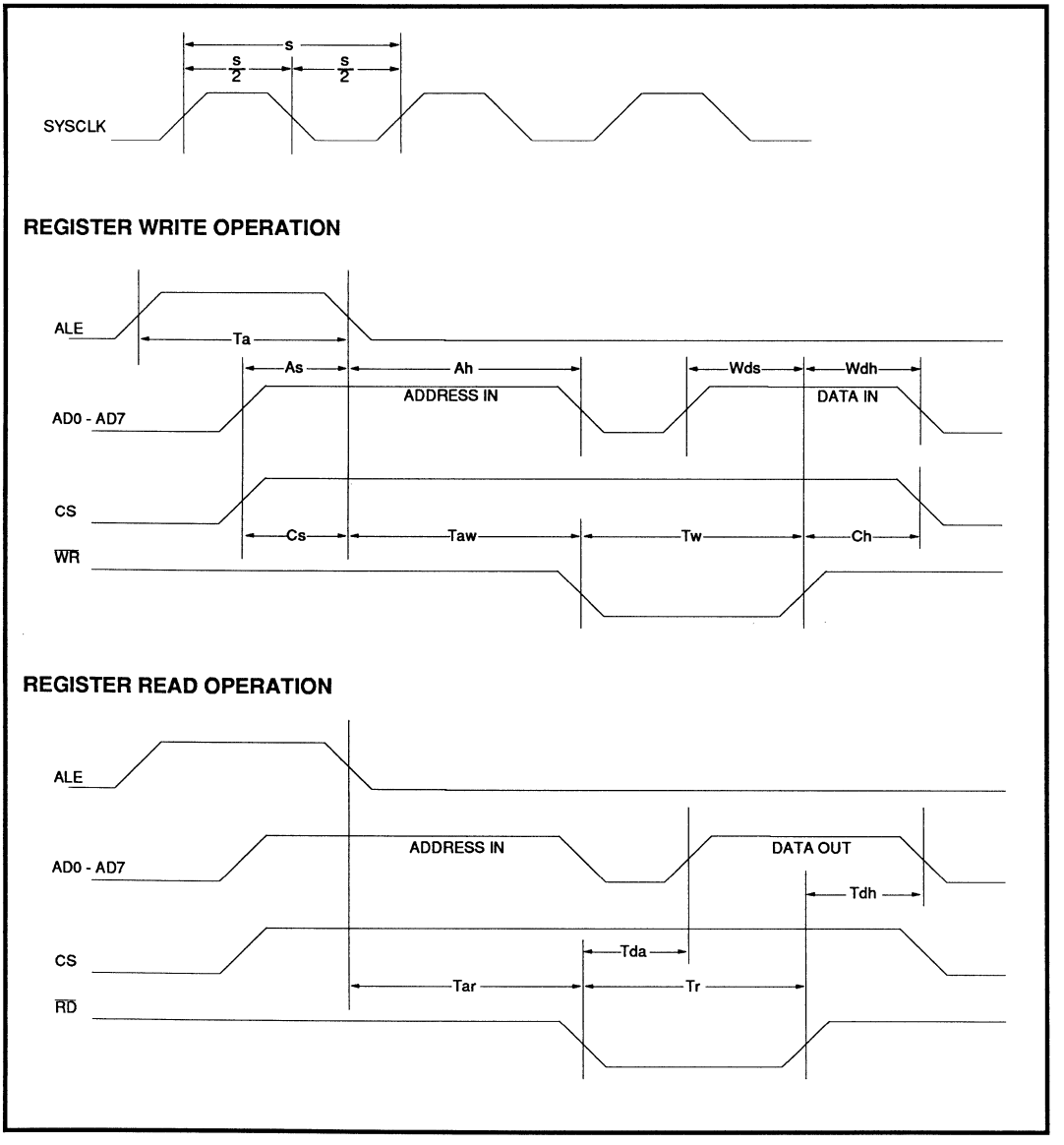


FIGURE 3: MICROPROCESSOR INTERFACE TIMING

A. C. TIMING CHARACTERISTICS (continued)

PERIPHERAL DEVICE INTERFACE TIMING (See Figure 4)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
T	RD/REFCLK Period		50			ns
T/2	RD/REFCLK Assert to De-assert		18			ns
Tr	RD/REFCLK Rise Time	T = 62.5 ns			5	ns
Tf	RD/REFCLK Fall Time	T = 62.5 ns			5	ns
Ds	NRZ in Valid to RD/REFCLK ↑	Set-up time	10			ns
Dh	RD/REFCLK ↑ to NRZ in Invalid	Hold time	7			ns
As	$\overline{AMD}$ ↓ to RD/REFCLK ↑	Set-up time	10			ns
Dv	RD/REFCLK ↑ to NRZ out		10		40	ns
Wv	RD/REFCLK ↑ to $\overline{WAM}$ ↓		10		40	ns
Wvr	RD/REFCLK ↑ to $\overline{WAM}$ ↑		10		40	ns

BUFFER INTERFACE TIMING (See Figure 5)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
T	$\overline{CLKA}$ Period		100			ns
T/2	$\overline{CLKA}$ Assert to De-assert		40			ns
Tba	$\overline{CLKB}$ ↓ to $\overline{CLKA}$ ↓		40			ns
Tab	$\overline{CLKA}$ ↓ to $\overline{CLKB}$ ↑		40			ns
Dov	$\overline{CLKA}$ ↑ to D0 - D7 out Valid		10		50	ns
Doh	$\overline{CLKA}$ ↑ to D0 - D7 out Invalid		0		50	ns
Dis	D0 - D7 in Valid to $\overline{CLKA}$ ↓		25			ns
Dih	$\overline{CLKA}$ ↓ to D0 - D7 in Invalid		10			ns

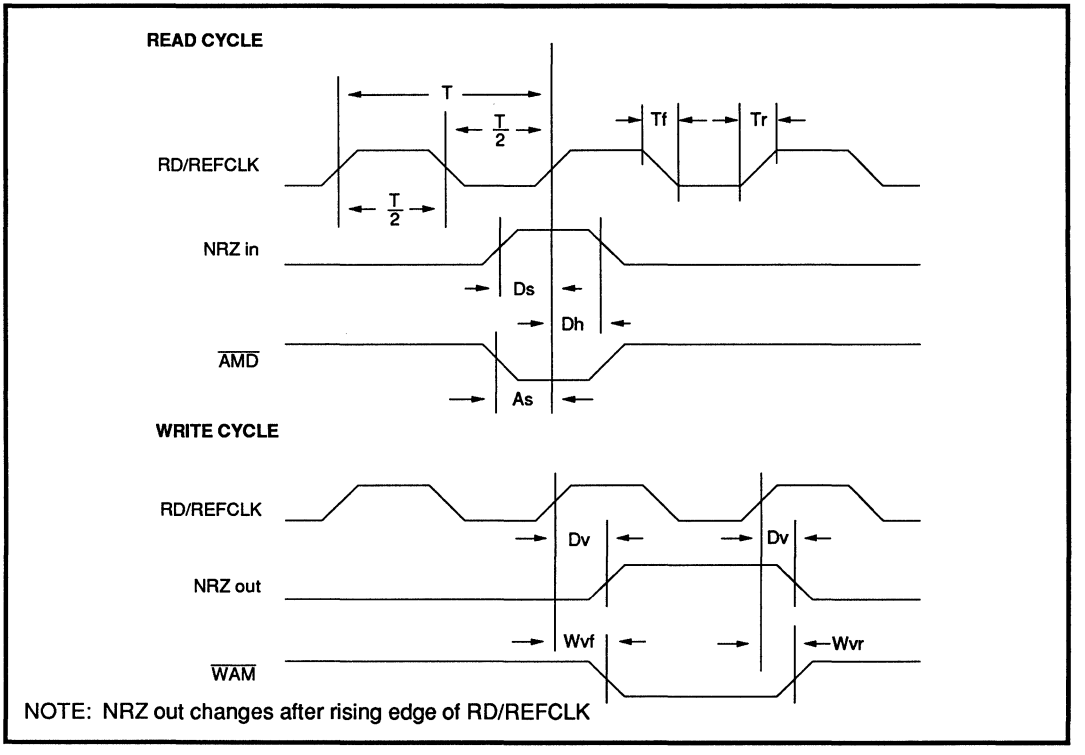


FIGURE 4: PERIPHERAL DEVICE INTERFACE TIMING

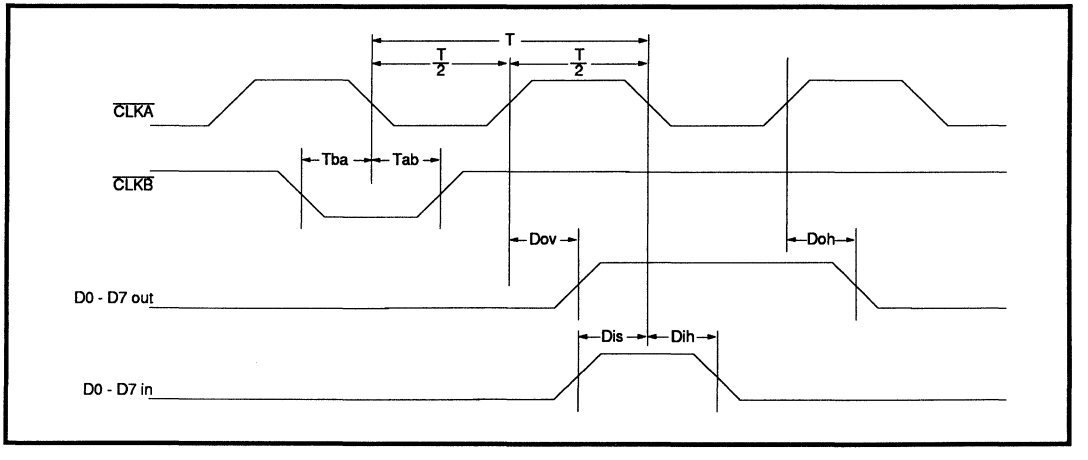


FIGURE 5: BUFFER INTERFACE TIMING

A. C. TIMING CHARACTERISTICS (continued)

EXTERNAL REGISTER TIMING (See Figure 6)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Tda	D0 - D7 in Valid to AD0 - AD7 out Valid				55	ns
Tra	$\overline{RD}$ ↓ to AD0 -AD7 out Valid	D0-D7 setup before $\overline{RD}$ ↓			60	ns
Trh	$\overline{RD}$ ↑ to AD0 - AD7 out Invalid				50	ns
Tad	AD0 - AD7 in Valid to D0 - D7 out Valid				55	ns
Twd	$\overline{WR}$ ↓ to D0 - D7 out Valid	AD0-AD7 setup before $\overline{WR}$ ↓			60	ns
Twh	$\overline{WR}$ ↑ to D0 - D7 out Invalid		50			ns

ADDRESS DECODE 6E AND 6F TIMING (See Figure 7)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Tdf	$\overline{RD}$ or $\overline{WR}$ ↓ to Strobe ↓				40	ns
Tdr	$\overline{RD}$ or $\overline{WR}$ ↑ to Strobe ↑				40	ns

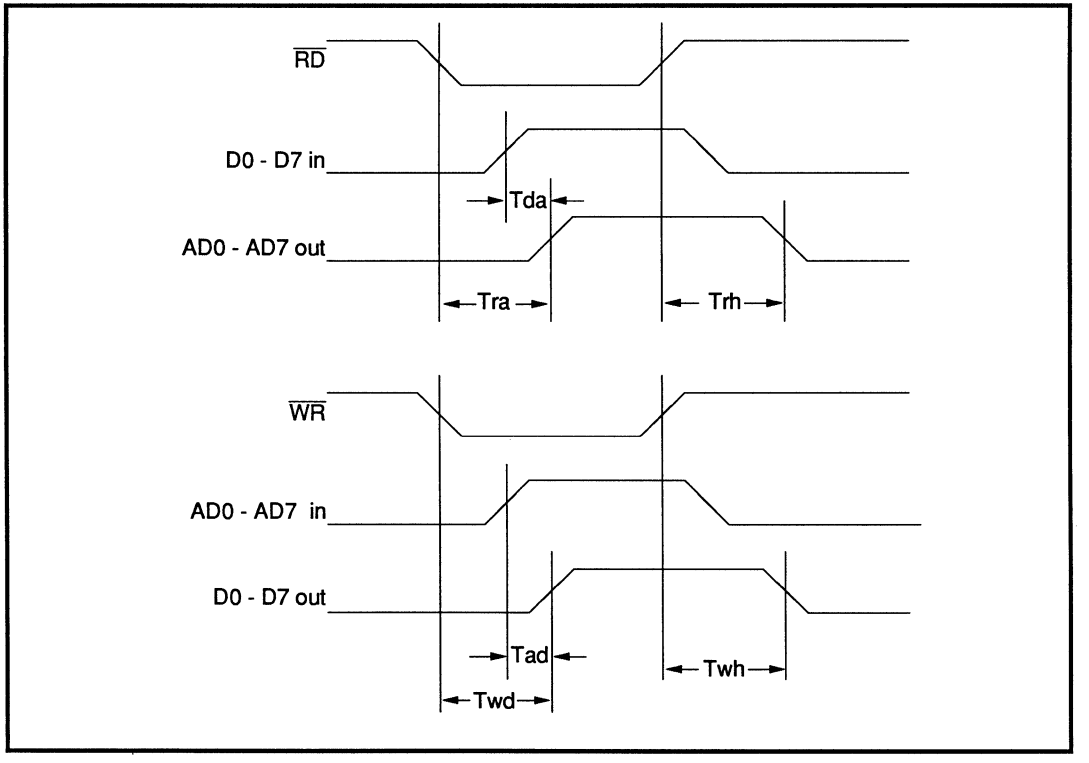


FIGURE 6: EXTERNAL REGISTER TIMING

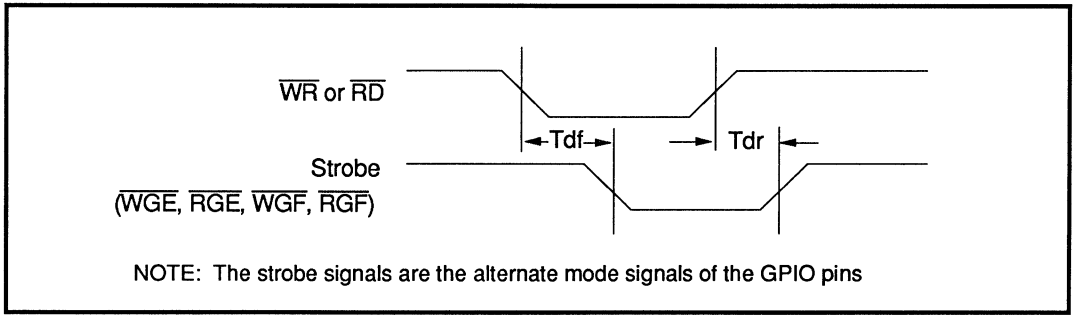


FIGURE 7: ADDRESS DECODE 6E AND 6F TIMING

APPLICATIONS INFORMATION

SEQUENCER PROGRAMMING EXAMPLES

This section describes how specific controller functions are implemented with the SSI 32C452. Sequencer programming examples for the specific case of an ST-506 Winchester disk drive are given. For convenience, all the code samples start at sequencer address 00H. In an actual implementation, the sequencer intructions would be distributed throughout the sequencer RAM, with common portions reused, so that the code for all operations would be resident simultaneously. All example values are hex quantities.

SECTOR ID

There are two types of Sector ID operation. In the first, the Sector ID field is read and saved by the controller for examination by the microprocessor. The 8 byte internal stack is used for this type of operation and read data is pushed to the stack under the control of the sequencer. In the second, the sector ID field is compared to a desired value in preparation for some other operation, such as sector read or sector write. In this case, the ID field parameters are compared to the data field of the controller instructions. A sequencer branch instruction is used to test for a positive field ID comparison and no ECC error before the rest of the operation proceeds. The microprocessor must program the SEQBR register with the address of the code for the following operation.

The controller establishes byte synchronism by searching for an address mark after RG is asserted. The data pattern of the address mark is specified in the AMDCON register and the number of bits actually used in the pattern is selected by the bits SYN2/1/0.

ADDR INSTRUCTION (SEQADRF SEQCONF SEQTYPF SEQDATF)

```
                                ; ST-506 Sector Identification example. Assumes AMDCON=A1H, SYN2/1/
                                  0=7
00    60 00 00 00               ; Loop here until Index Pulse (SEQBR=01H)
01    02 40 00 00               ; Turn on RG
02    03 02 80 A1               ; Look for address mark ( A1H in ST-506 format)COMPEN=1DTYP2=1
                                  (Address Mark - Data Separator will detect deliberate coding violations and
                                  assert WAM/AMD pin).
03    04 02 00 FE               ; Look for 2nd byte of address mark (FEH - written as normal data - no coding
                                  violations) COMPEN=1
05    06 12 00 NCYL             ; Compare cylinder number (NCYL) and save too.COMPEN=1, STACKEN=1
06    07 12 00 NHEAD            ; Compare head number (NHEAD) and save too.COMPEN=1, STACKEN=1
07    08 12 00 NSECT            ; Compare sector number (NSECT) and save too.COMPEN=1, STACKEN=1
08    89 10 41 00               ; Check ID field ECC and save ECC bytes.Branch to read or write operation
                                  if positive comparison on field ID and if ECC was good (SECTBR indicates
                                  condition for desired sector operation).DTYP1=1 (ECC byte),
                                  STACKEN=1COUNT=1
0A                              ; Here if sector ID did not match target. Actual ID field and ECC bytes are
                                  available on the stack for microprocessor check.
```

SECTOR READ

Once the sector ID field has been verified, the data field may be read. Detection of the address mark for the data portion of the sector proceeds as for ID field address mark, and causes the serializer/deserializer to be correctly synchronized with the incoming data bytes. At the end of a sector read, the microprocessor may check the ECC result to determine if a reread or error correction computation is required.

```
ADDR  INSTRUCTION  (SEQADRF SEQCONF SEQTYPF SEQDATF)

                                ; ST-506 Sector Read example assumes that sector ID field verification has
                                  been performed.
00    01 40 00 00               ; Turn on RG
01    02 02 A0 A1               ; Look for data field Address Mark (A1H)COMPEN=1DTYP2=1 (AM byte),
                                  DTYP0=1, enable CLKB when synchronization occurs.
02    E3 02 00 F8               ; Check second byte of AM. Must be F8H for ST-506 data field. Branch if AM
                                  bytes bad.COMPEN=1
03    04 01 FF 00               ; Transfer 256 data bytes DATEN=1COUNT=FFH
04    A5 00 41 00               ; Read ECC bytes, branch on error DTYP1=1 (ECC)COUNT=1
05                              ; Here if read was error free.
```

SECTOR WRITE

Sector writes proceed in a similar fashion to reads. Once the sector ID field has been verified, the sequencer writes a short gap (the 'write splice') and then the sector data, followed by ECC bytes and another gap.

```
ADDR  INSTRUCTION  (SEQADRF SEQCONF SEQTYPF SEQDATF)

                                ; ST-506 Sector Write exampleAssumes that sector ID field verification has
                                  been performed.
00    01 00 02 00               ; Skip 3 bytes
01    02 80 0C 00               ; Turn on WG and write 13 bytes of 00HCOUNT=0CHSETWG=1
02    03 00 A0 A1               ; Write first data AM byte (A1H)DTYP2=1 (AM), DTYP0=1 (Start CLKB*)
03    04 00 00 F8               ; Write second data AM byte (F8H)DTYP2=0 since this byte is written as
                                  normal data (no coding violations).
04    05 01 FF 00               ; Write 256 data bytes DATEN=1 (transfer enabled, data comes from buffer
                                  memory)COUNT=FFH
05    06 00 41 00               ; Write 2 ECC bytes COUNT=1DTYP1=1 (ECC)
06    07 00 02 00               ; Write three bytes of 00HCOUNT=2
07    08 20 00 00               ; Turn WG off RESWG=1
08                              ; Here when sector write is finished
```

OPERATIONAL INFORMATION

Sector formatting is similar to sector writing, except that the sector ID field is written in addition to the data field. The data field is also written with a fixed value instead of data transferred from buffer memory. Examples of sequencer code to write specific data are given under sector write. When an entire track is to be written, the microprocessor may update ID field information in the sequencer RAM to reflect the next sector while the sequencer is writing the current data field. This allows an entire track to be formatted in one continuous write operation. Formatting begins after the sequencer detects an index pulse.

A **data search** operation can be implemented by a simple modification to the sequencer programming for sector read operations. When the COMPEN bit of the sequencer control field is enabled, incoming data will be compared to buffer data instead of being stored. This allows the sector to be searched for specific data. (The SEARCHOP bit in the OPCON register must also be set for searches).

Data verification can be performed during a sector read if the TRANSINH bit (data transfer inhibit) of OPCON is enabled, because no data will be written to the buffer. However, ECC checking will continue so that at the end of the sector, the ECC result can be verified.

The controller can support **extended sector sizes** of greater than 256 bytes. One simple way to achieve larger sector sizes is to use several sequencer data transfer instructions in a row. The size of the data block that results will be the sum of the counts for each transfer instruction. Large sectors may also be implemented with a single sequencer instruction by using

the CARRYINH bit in OPCON. Sequencer instructions terminate when the carry caused by an underflow of the byte counter is detected. When CARRYINH is set, this carry will not be recognized, so the counter (which is initially loaded with the value specified in each instruction's count field) will wrap around to a full count (FFH). The CARRYINH bit is cleared by an underflow, so that if it is not set again by the microprocessor, the sequencer instruction will terminate after an additional 256 bytes. This permits the sector length to be extended in multiples of 256 bytes.

Multi-sector reads and writes are accomplished in a similar manner to full track formatting. The sequencer is programmed as for a single sector operation. However, when the microprocessor detects that the DATATRANS bit in the SEQSTAT register is set (implying that a data transfer is in progress), it alters the ID field information in the sequencer's instruction RAM. When the data transfer for a particular sector is completed, the sequencer is looped back to the same sector ID routine. It will then start a new sector operation using the ID information just loaded by the microprocessor. This type of operation may proceed for an entire track.

ECC IMPLEMENTATION

The ECC hardware may be used for error correction as well as checksum generation. An algorithm for locating and correcting read errors is described below. The algorithm assumes the use of a 32 bit ECC polynomial capable of correcting a single burst of up to 8 bit errors. Longer bursts or multiple bursts may be incorrectable.

1. If an ECC error is detected (ECCERR is set in SEQSTAT) and error correction is needed (ie. multiple reads from the same sector have failed) the error syndrome must be read from the ECC shift register and reloaded in bit-reversed order, as follows:
   - 1.1 Set FEEDINH in ECCCON
   - 1.2 Read and save top 8 bits of shift register from ECC24
   - 1.3 Set ECCSHIFT in ECCCON 8 times
   - 1.4 Repeat 1.2 and 1.3 until all 4 bytes of the syndrome are RAM
   - 1.5 Copy each syndrome bit, starting with the least significant, to ECCIN and set ECCSHIFT after each copy. After 32 such operations the ECC shift register will contain the bit reversed polynomial.
2. The reverse ECC generator polynomial must be written to the ECC generator.
   - 2.1 Configure the bit-reversed polynomial in the 4 feedback registers, POLY0, POLY8, POLY16 and POLY24. This step is not equivalent to bit reversing the feedback register contents, since the coefficients for x^0 and x^{32} are fixed in hardware. The reverse polynomial is generated by subtracting the exponents from 32. The following is a numerical example to illustrate the programming of forward and reverse polynomials for the 32 bit computer-generated code:
     forward:
     $x^0+x^4+x^6+x^{13}+x^{15}+x^{22}+x^{26}+x^{30}+x^{32}$;
     reverse:
     $x^{32}+x^{28}+x^{26}+x^{19}+x^{17}+x^{10}+x^6+x^2+x^0$;

	Forward	Reverse
POLY0	28H	22H
POLY8	50H	02H
POLY16	20H	05H
POLY24	22H	0AH
   - 2.2 Reset FEEDINH and ECCIN in the ECCCON register.
3. The ECC shift register is operated until either the number of shifts exceeds the number of bits in the read block or the 24 least significant bits of the ECC register are zero.
   - 3.1 Compute block length in bits, including ECC and overhead bits.
   - 3.2 Initialize a shift counter to zero.
   - 3.3 Set ECCSHIFT to shift the ECC registers by one, and increment the shift counter.
   - 3.4 If the shift counter exceeds the block length, stop the computation as this means the errors are uncorrectable. Otherwise, if register ECC16 is non-zero, repeat step 3.3.
4. At this point, ECC24 contains the bit-reversed error pattern and the shift counter indicates its displacement from the end of the block. The pattern must be mirrored and aligned to byte boundaries so that the errors in the buffer storage may be corrected.
   - 4.1 Subtract 7 from the shift counter, to compensate for a hardware offset internal to the SSI 32C452.
   - 4.2 Subtract 32 from the shift counter. (This is the number of the ECC bits). If the result is less than zero then no further action is required, since the errors occurred in the ECC portion of the block.
   - 4.3 Read the contents of ECC24 into RAM and bit-reverse this 8 bit quantity.

4.4 Form a 16 bit word with the reversed error pattern as its lower byte and zero as its upper byte.

4.5 If the lowest three bits of the shift counter are non-zero, left shift the 16 bit word and decrement the shift counter.

4.6 Repeat 4.5 until the shift counter's three least significant bits are zero.

4.7 Divide the shift counter by 8, to convert bits into bytes.

5. The position and nature of the errors are now known, so they may be corrected as follows:

5.1 Exclusive OR the lower byte of the error word with the data byte whose offset from the end of the data block is given by the value of the shift counter.

5.2 Exclusive OR the upper byte of the error word with the data byte whose offset from the end of the data block is one more than the value of the shift counter.

The above procedure will correct a single burst of errors, provided that the degree of the error is within the capability of the chosen code. The code whose polynomial is illustrated above is capable of correcting a single burst of up to 8 error bits.

Since the error correction process is time consuming and ties up the ECC hardware, blocks with errors should be re-read to ensure that the errors observed are in fact hard errors.

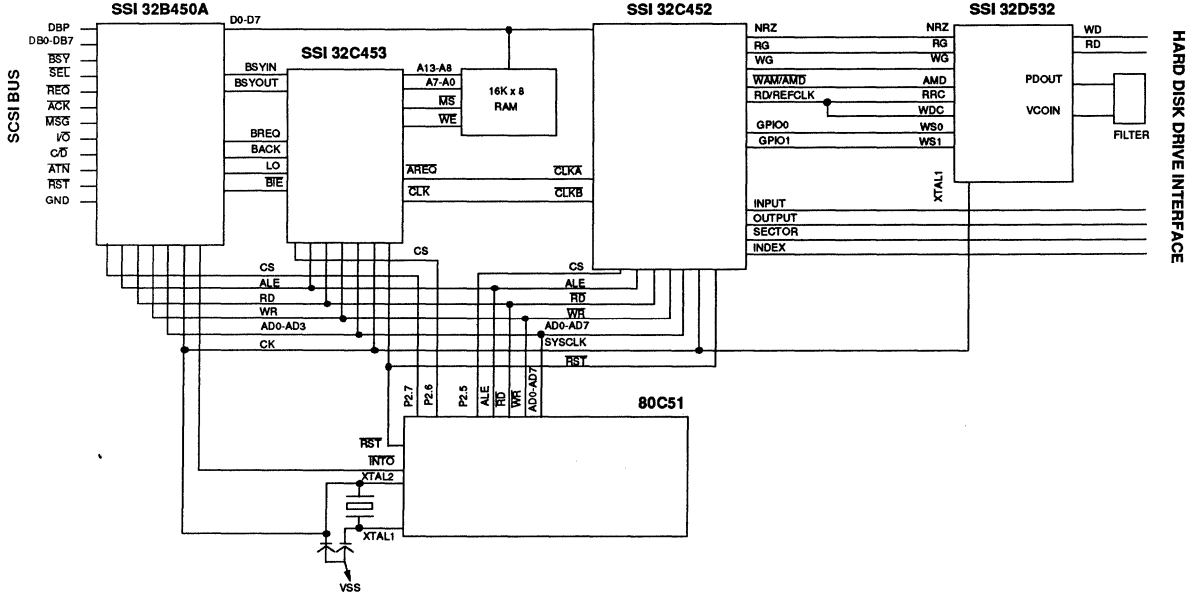
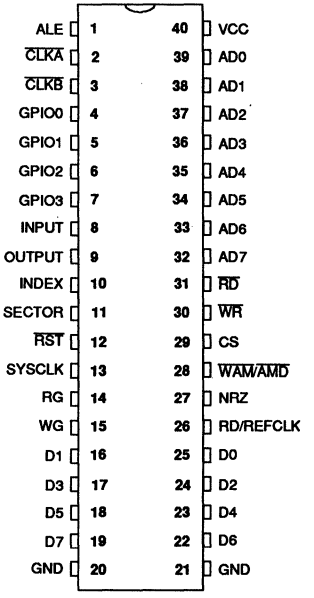


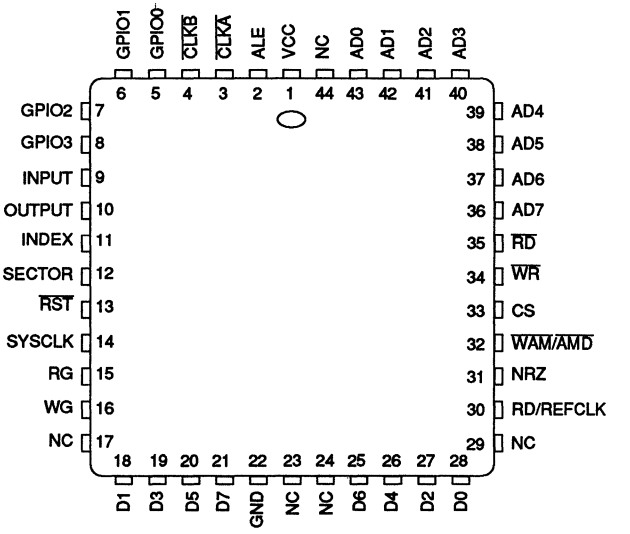
FIGURE 8: SCSI PERIPHERAL CONTROLLER CHIP SET

SSI 32C452
Storage Controller

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



DIP



PLCC

ORDERING INFORMATION

PART DESCRIPTION		ORDER NO.	PKG. MARK
SSI 32C452 Storage Controller	40 Pin DIP	SSI 32C452-CP	32C452-CP
	44 Pin PLCC	SSI 32C452-CH	32C452-CH

silicon systems™
Silicon Systems, Inc.,14351 Myford Road, Tustin CA 92680, (714) 731-7110, TWX 910-595-2809

silicon systems™
INNOVATORS IN INTEGRATION

SSI 32C452A
Storage Controller

August, 1988

DESCRIPTION

The SSI 32C452A Storage Controller is a CMOS device that provides the basis for an intelligent Winchester disk drive controller capable of non-interleaved data transfers at rates up to 20 Mbps. When combined with a microprocessor, memory and a buffer management device such as the SSI 32C453, the SSI 32C452A implements a powerful and cost-efficient peripheral controller solution. It also has the flexibility to be used in SCSI systems.

The SSI 32C452A includes a control sequencer with a writeable control store, and configuration/status registers which can be programmed to support standard and custom interface protocols for storage controllers. Access to the control store and registers is accomplished through the microprocessor interface which is optimized for 8 bit, multiplexed address/data bus processors such as the 8085 . It also has the flexibility to interface with most standard 8-bit microprocessors. This organization allows the controller firmware to be stored in an EPROM or the host and down-loaded to the SSI 32C452A, and means wide flexibility of the control functions performed by the device.

(Continued)

FEATURES

- **Supports all serial data storage interfaces**
- **Operates with 16 MHz microprocessors**
- **Internal RAM-based control sequencer**
- **Internal user programmable ECC to 64 bits**
- **Internal 16 bit CRC**
- **Non-interleaved data transfer to 15 Mbps**
- **Hard or soft sector formats**
- **Programmable sector lengths up to a full track**
- **High performance, low power CMOS device**
- **Functionally compatible with AIC-011**
- **Single 5 volt supply**
- **Available in 44-pin PLCC or 40-pin DIP package**

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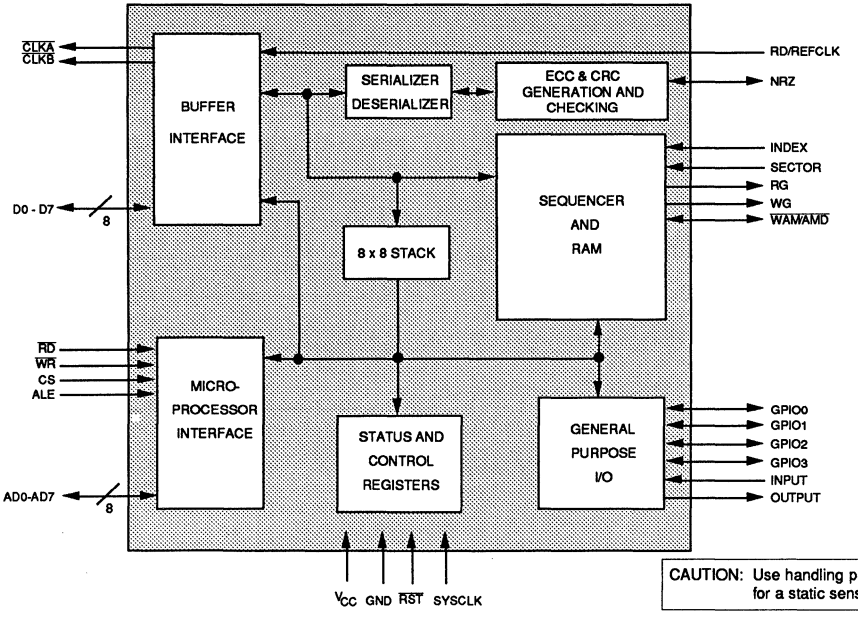
BLOCK DIAGRAM



0888

CAUTION: Use handling procedures necessary for a static sensitive device.

DESCRIPTION (Continued)

The SSI 32C452A performs all the controller functions for the peripheral device, such as serialization/deserialization, ECC generation and checking on the data stream, and CRC generation and checking on the header or data stream. It also handles overhead information such as address marks, gaps and sector ID fields. If an ECC error is detected during a read, the syndrome is saved so that defects can be corrected. The ECC polynomial and register length can be programmed or bypassed entirely so that external ECC hardware can be used.

FUNCTIONAL DESCRIPTION

The major functional elements and data paths of the SSI 32C452A are shown in the block diagram.

The SSI 32C452A performs the functions to interface a serial data storage device such as a Winchester disk drive, to a parallel bus interface for data processing on a byte wide basis. The functions necessary to accurately make this conversion are serialization/deserialization, error detection and correction for both the header information and data stream, and data path control. The SSI 32C452A also has general purpose interface lines to further facilitate control of the data storage device or parallel interface. An eight byte stack allows data to be saved and reviewed by the microprocessor for error handling purposes. The internal sequencer performs most of the operations in conjunction with the control and status registers. The sequencer program is contained in internal sequencer RAM, which is easily (re)programmed providing almost infinite flexibility in communcations protocols and control features. A microprocessor effects both initialization and control of the SSI 32C452A by writing to and reading from the internal registers, sequencer RAM, stack and general purpose I/O circuitry. The microprocessor interface block of the SSI 32C452A provides the communication and control for the SSI 32C452A interface to the microprocessor.

The **buffer interface** includes a bidirectional data bus that exchanges data bytes between an external buffer memory and the serializer/deserializer. It generates two clocks, $\overline{CLKA}$ and $\overline{CLKB}$ which control all accesses to the buffer memory. All buffer memory cycles must be synchronous with $\overline{CLKA}$, which is derived from the RD/REFCLK input during data transfers and from SYSCLK otherwise. The internal register CLKCON contains control bits which define the relationship between these source clocks and $\overline{CLKA}$. The $\overline{CLKB}$ signal is asserted whenever a new data byte must be transferred (ie. when the serializer/deserializer is full during a read operation or empty during a write operation). The direction of the transfer is determined from the state of the read gate (RG) and write gate (WG) lines. A $\overline{CLKB}$ cycle is used to force the buffer control device (eg. an SSI 32C453) to reserve the next buffer memory access for the SSI 32C452A, since peripheral transfers are synchronous they take precedence over the asynchronous host transfers. In order to allow host transfers to keep up with peripheral transfers, the $\overline{CLKA}$ rate selected should be at least twice the word transfer rate of the peripheral.

The **microprocessor interface** decodes microprocessor read and write requests and provides access to the appropriate register or internal memory location. Since both data and address information are carried on the multiplexed bus lines AD0-AD7, address information is latched from the bus on the falling edge of the microprocessor signal ALE (address latch enable). When $\overline{CS}$ is asserted along with either $\overline{RD}$ or $\overline{WR}$, the register whose address was previously latched is selected. The addresses and names of all the accessible registers are shown in the Register Address Map, Figure 1. The microprocessor should not read or write the sequencer RAM while the sequencer is running, since there is no circuitry to resolve conflicting accesses and incorrect sequencer operation will result.

The **status and control registers** make status information available to the microprocessor and allow the device to be configured for a wide variety of peripheral control applications. The microprocessor can monitor the status of transfers in progress and control the ECC register operation, the ECC polynomial, the clock generation hardware and the sequencer program execution. The microprocessor also has access to the sequencer's microprogram RAM so that it loads the microcode for all controller operations.

The **serializer/deserializer** circuit interfaces the parallel buffer memory bus to the serial NRZ data stream of the peripheral device. Byte synchronism is maintained with a bit ring, which is an 8 bit recirculating shift register clocked by the peripheral bit clock. During a sector write, the bit ring is initialized explicitly with a

sequencer instruction. The bit ring continues to operate until the end of the field (ECC or CRC written or read) and causes $\overline{CLKB}$ to be asserted once for each data byte to be transferred. During write operations, the sequencer may cause address marks and sync patterns to be loaded into the serializer instead of data bytes. These special patterns are contained in a sequencer instruction and are transferred to the serializer over an internal byte wide data path. During read operations, bytes of overhead information may be routed to the stack or sequencer for comparison against target values. This process is controlled by the control field (SEQCONF) in each sequencer instruction.

The eight byte recirculating **stack** may be used to capture read data for later examination by the microprocessor. Data is pushed onto the stack under sequencer control. The control bit STACKEN in the sequencer instruction field SEQCONF directly controls the stack. If more than 8 bytes are written to the stack, only the last 8 will be saved. When a data byte is read from the top of the stack by the microprocessor via the STACK register, the data is recirculated to the bottom of the stack, allowing the stack contents to be examined more than once without the use of temporary storage in the microprocessor or buffer.

Serial peripheral data is passed through a variable length shift register with programmable exclusive OR feedback that performs **ECC generation and checking**. The feedback taps for the desired ECC polynomial are selected in the eight registers POLY0 - POLY56 and the polynomial length is determined by the LEN bits in ECCCON as well as the LEN bits in EXT. In addition, the ECC register may be operated either under sequencer or microprocessor control. During read operations, the contents of the ECC register are compared to the actual ECC field read from the peripheral. If there is a mismatch, the error syndrome is available for error correction. The ECC polynomial may be reversed to allow hardware computation of the error location, relieving the microprocessor of the burden of this lengthy calculation. During writes to the peripheral, the computed ECC word can be appended to each data or address field. The sequencer data type field (SEQDATF) indicates when ECC bytes are to be written or checked during a peripheral transfer.

6

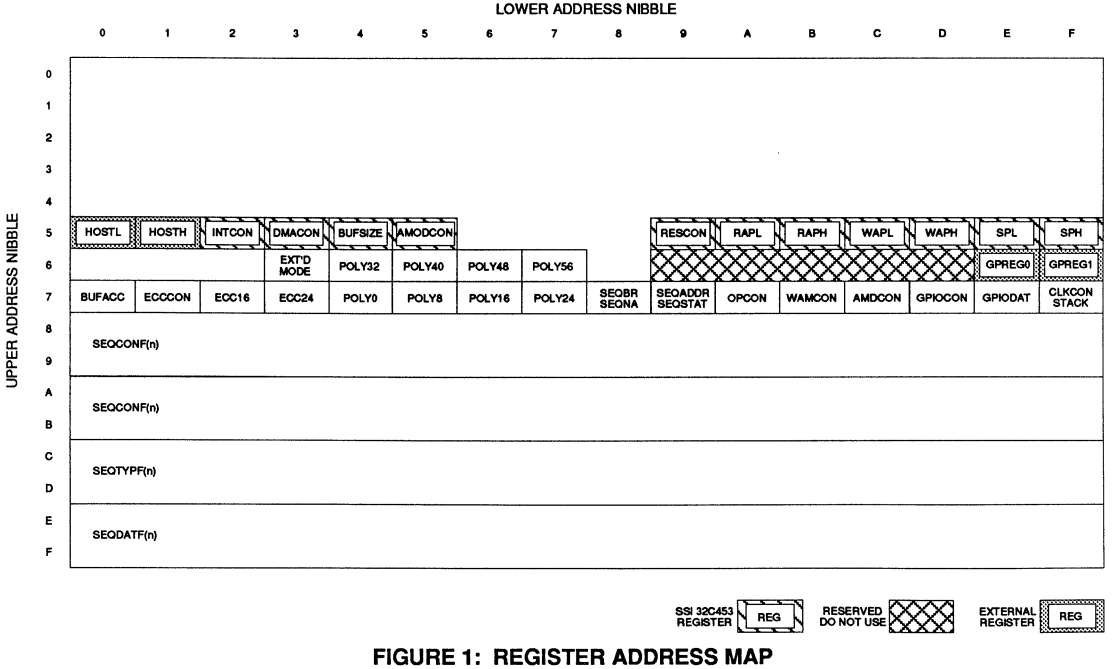


FIGURE 1: REGISTER ADDRESS MAP

FUNCTIONAL DESCRIPTION (continued)

The **sequencer** controls the time critical operations of the SSI 32C452A. It executes programs stored in the 31 word by 32 bit sequencer RAM, and can be programmed to support hard and soft sectored read, write, search and verify operations for a wide variety of Winchester disk drives and other peripherals. The sequencer RAM is loaded by writing to the sequencer instruction registers as outlined in the Sequencer Instructions section of this data sheet. Each instruction is comprised of four bytes. Each of the four bytes represents a function of the sequencer operation. They are address field, control field, data type field, and data field. The organization of these fields is shown in the Register Bit Map, Figure 2. The Sequencer Registers provide control from and status to the microprocessor and sequencer. They contain branch, next and start addresses, and sequencer status information. The SEQUENCER STATUS register provides informaton on the sequencer state such as whether an ECC error occurred, a compare equal or low occurred, if the branch condition or address mark is active, or whether the sequencer is halted.

The **general purpose I/O** section has four general purpose I/O lines GPIO0 - GPIO3, and the INPUT pin which are accessible through the internal general purpose input/output registers. They are available for user defined functions such as Winchester disk or host interface control. The functionality of the GPIO0 - GPIO3 pins is programmed in the GPIOCON and GPIODAT registers. They can act as I/O's asserted or read through the GPIODAT register, or they can be programmed to decode microprocessor access to addresses 6EH and 6FH eliminating the need for external decode. The INPUT signal can be programmed in the SEQADRF RAM (registers) to affect sequencer operation and the state of the pin read from the GPIODAT register. The other general purpose line, OUTPUT is controlled directly by the sequencer to synchronize it with external circuitry. The OUT bit of the GPIODAT register reflects the state of the output pin.

PIN DESCRIPTION

GENERAL

NAME	DIP	PLCC	TYPE	DESCRIPTION
VCC	40	1		POWER SUPPLY +5 volts
GND	20-21	22		GROUND
$\overline{RST}$	12	13	I	RESET - Active low signal halts the sequencer, sets output pins RG, WG, $\overline{WAM}$ and NRZ low, forces the GPIO pins into a high impedance state and resets a number of the registers as described below.
SYSCLK	13	14	I	SYSTEM CLOCK - Clock input in the range of 1.5 MHz to 16 MHz

MICROPROCESSOR INTERFACE

ALE	1	2	I	ADDRESS LATCH ENABLE - Falling edge latches register address from AD0-7 pins.
CS	29	33	I	CHIP SELECT- Active high signal enables device to respond to microprocessor read or write.

PIN DESCRIPTION (Continued)

NAME	DIP	PLCC	TYPE	DESCRIPTION
$\overline{WR}$	30	34	I	WRITE STROBE - Active low signal causes the data on the address/data bus to be written to the addressed register if CS is also active.
$\overline{RD}$	31	35	I	READ STROBE - Active low signal causes the contents of the addressed register to be placed on the address/ data bus if CS is also active.
AD0-AD7	39-32	43-36	I/O	ADDRESS/DATA BUS - 8 bit bus which carries register address information and bi-directional data. These pins are high impedance when not in use.

GENERAL PURPOSE I/O

GPIO0-3	4-7	5-8	I/O	GENERAL PURPOSE I/O LINES - These lines can be programmed as an inputs or outputs which are accessed though the GPIODAT register. They may also be programmed to serve as active low outputs which decode microprocessor accesses to the following locations: I/O pin — Alternate output decode GPIO0 — Write to 6EH GPIO1 — Read from 6EH GPIO2 — Write to 6FH GPIO3 — Read from 6FH
INPUT	8	9	I	INPUT PIN - This dedicated input line may be read through the GPIODAT register or tested directly by the control sequencer.
OUTPUT	9	10	O	OUTPUT PIN - Dedicated output line which is derived directly from the control sequencer instruction field.

DISK DRIVE INTERFACE

INDEX	10	11	I	INDEX PULSE - Active high disk drive index pulse input, must be at least one byte time long.
SECTOR	11	12	I	SECTOR PULSE - Active high sector pulse input from disk drives that are hard sectored, must be at least one byte time long.
RG	14	15	O	READ GATE - Active high output from control sequencer enables external phase-locked loop (PLL) to synchronize to read data stream from the storage device.

PIN DESCRIPTION (continued)

DISK DRIVE INTERFACE (continued)

NAME	DIP	PLCC	TYPE	DESCRIPTION
WG	15	16	O	WRITE GATE - Active high output from control sequencer indicates valid write data to the storage device.
RD/REFCLK	26	30	I	READ/REFERENCE CLOCK - This input must be externally multiplexed to provide the PLL clock when read gate is active and the write oscillator clock at all other times. This pin must always be driven with a clock signal, even when $\overline{RST}$ is active.
NRZ	27	31	I/O	NRZ DATA - This bi-directional pin provides write data when WG is active, and must be driven with read data when RG is active. Data must be in the NRZ format.
$\overline{WAM}/\overline{AMD}$	28	32	I/O	WRITE ADDRESS MARK/ADDRESS MARK DETECT - This bi-directional pin is used to write and detect address marks. When WG is active, a low level output of one bit time on this pin indicates that an address mark must be written. When RG is active, the peripheral must provide an active low input to indicate the detection of an address mark.

BUFFER INTERFACE

$\overline{CLKA}$	2	3	O	CLOCK A - Clock signal which initiates host or controller accesses to the buffer memory on its falling edge. When either RG or WG is active, this output is derived from RD/REFCLK. At all other times it is derived from SYSCLK. The clock source is divided by 2 or 4 as programmed in the CLKCON register.
$\overline{CLKB}$	3	4	O	CLOCK B - This clock is used to reserve $\overline{CLKA}$ cycles for SSI 32C452 data transfers. An active low pulse spanning a falling edge of $\overline{CLKA}$ indicates that the next falling edge on $\overline{CLKA}$ will be used by the SSI 32C452 to access the buffer memory.
D0-D7	16-19 22-25	18-21 25-28	I/O	BUFFER DATA BUS - Bi-directional data bus that carries data to and from the buffer memory. Bus cycles are controlled by $\overline{CLKA}$ and $\overline{CLKB}$. Direction of the transfer is determined by RG and WG. Note: refer to pin diagram for exact ordering of the pins.
No connects on PLCC package: 17, 23, 24, 29, 44				

REGISTER	ADDRESS	7	6	5	4	3	2	1	0	READ/ WRITE
BUFACC	70H	BUFFER MEMORY BYTE								R/W
ECCCON	71H	LEN1	LEN0	RESET	SECTBR	CLRECC	FEEDINH	ECCSHIFT	ECCIN	W
ECC16	72H	ECC23	ECC22	ECC21	ECC20	ECC19	ECC18	ECC17	ECC0/16	R
ECC24	73H	ECC31	ECC30	ECC29	ECC28	ECC27	ECC26	ECC25	ECC24	R
POLY32	74H	F39	F38	F37	F36	F35	F34	F33	F32	W
POLY40	75H	F47	F46	F45	F44	F43	F42	F41	F40	W
POLY48	76H	F55	F54	F53	F52	F51	F50	F49	F48	W
POLY56	77H	UNUSED	F62	F61	F60	F59	F58	F57	F56	W
SEQBR	78H	UNUSED			BRADR4	BRADR3	BRADR2	BRADR1	BRADR0	R/W
SEQADDR	79H	UNUSED			STADR4	STADR3	STADR2	STADR1	STADR0	W
SEQSTAT	79H	AMACTIVE	DATATRANS	BRACTIVE	STOPPED	UNUSED	ECCERR	COMPLO	COMPEQ	R
OPCON	7AH	CARRYINH	UNUSED	TRANSINH	SEARCHOP	UNUSED	NRZDAT	SECTORP	INDEXP	R/W
WAMCON	7BH	AM7 - AM0								W
AMDCON	7CH	AMD7 - AMD0								W
GPIOCON	7DH	RGFSEL	WGFSEL	RGESEL	WGESEL	GPDIR3	GPDIR2	GPDIR1	GPDIR0	R/W
GPIODAT	7EH	UNUSED		OUT	INP	GP3	GP2	GP1	GP0	R/W
CLKCON	7FH	CLKF2	CLKF1	UNUSED	CLKFO	CLKINH	SYN2	SYN1	SYN0	W
STACK	7FH	TOP OF STACK								R
SEQADDRF	80H	BRCON2	BRCON1	BRCON0	NEXT4	NEXT3	NEXT2	NEXT1	NEXT0	R/W
	9EH									
SEQCONF	A0H	SETWG	SETRG	RESWG	STACKEN	NRZINH	OUTPIN	COMPEN	DATEN	R/W
	BEH									
SEQTYPF	C0H	CNT7/ DTYP2	CNT6/ DTYP1	CNT5/ DTYP0	CNT4	CNT3	CNT2	CNT1	CNTO	R/W
	DEH									
SEQDATF	E0H	DATA FIELD								R/W
	FEH									
EXT	63H	LEN2	LEN3	UNUSED	MODE1	UNUSED				W
POLY0	64H	F7	F6	F5	F4	F3	F2	F1	F0	W
POLY8	65H	F15	F14	F13	F12	F11	F10	F9	F8	W
POLY16	66H	F23	F22	F21	F20	F19	F18	F17	F16	W
POLY24	67H	F31	F30	F29	F28	F27	F26	F25	F24	W

FIGURE 2: REGISTER BIT MAP

REGISTER DESCRIPTION

The microprocessor which controls the system has access to all the SSI 32C452A registers and sequencer RAM through its external memory address space. The SSI 32C452A and its companion device, the SSI 32C453 Dual Port Buffer Controller, are designed to occupy a single 256 byte page. The 8 bit page address is latched from pins AD0-AD7 on a falling edge of ALE and remains valid until the next ALE falling edge.

The external registers described at the end of this section are not implemented in either the SSI 32C452A or SSI 32C453, and are assumed to be implemented in external hardware. These external registers are not required for use with the SSI 32C452A, but are included as applications information.

ECC REGISTERS

The core of the ECC circuit is a 64 bit shift register whose effective length may be programmed to be 16, 24, 32, 48, 56 or 64 bits. This is accomplished in hardware by directing the input data to stage 48, 40, 32, 16, 8 or 0 of the ECC shift registers while its output is always bit 63, which is bit ECC63 of register ECC56.

The ECC polynomial to be implemented is programmed by the user into the ECC feedback registers, POLY0, POLY8, POLY16, POLY24, POLY32, POLY40, POLY48 and POLY56. Each bit in these registers enables or disables exlusive OR feedback to the output of the corresponding shift register stage. The feedback signal is the exclusive OR of the serial data stream with the output of shift register stage 63. An override bit in ECCCON forces normal shift register operation, regardless of the settings of the feedback control bits.

When WG or RG are active, the ECC shift register input is the serial read or write data and the shift clock is RD/REFCLK. When an ECC word is being written, feedback is disabled and the shift register output is substituted for the data stream. At other times the microprocessor may set the ECCIN bit explicitly and cause a single shift register clocking to occur. For further information on implementing an ECC polynomial see the Applications Information Section at the end of this data sheet.

ECCCON 71H Read/Write

ECC CONTROL WORD		
BIT	**NAME**	**DESCRIPTION**
0	ECCIN	ECC SERIAL INPUT - When both RG and WG are inactive, this bit becomes the input bit for the ECC shift register. The RD/REFCLK must always be active for correct operation of the device.
1	ECCSHIFT	ECC SHIFT CONTROL - When both RG and WG are inactive, a single shift of the ECC register will occur when this bit is set. It is automatically cleared again when the shift is complete.
2	FEEDINH	ECC FEEDBACK INHIBIT - When this bit is set all feedback is inhibited and the ECC register functions as a simple shift register of the selected length.
3	CLRECC	CLEAR ECC - If this bit is set when either RG or WG are active, the ECC syndrome will be cleared at the end of the read/write operation. If both are inactive, the syndrome will be cleared immediately.
4	SECTBR	ENABLE SECTOR BRANCH - If the sequencer 'branch on index or sector' instruction is executed and SECTBR is set, the sequencer will recognize the branch condition as true if either the INDEX or the SECTOR pin is active. If SECTBR is cleared, then the sequencer will only recognize the branch condition if the INDEX pin is active.

ECC REGISTERS (continued)

BIT	NAME	DESCRIPTION
5	RESET	CHIP RESET - When this bit is set, the SSI 32C452A will be held in its reset state. This bit is set when $\overline{RST}$ is true.
6-7	LEN0-LEN1	ECC REGISTER LENGTH - These two bits, together with bits 6 and 7 of Register 63 (LEN2 & LEN3), select ECC register length as follows: LEN0 LEN1 LEN2 LEN3 0 0 X X 16 bit register 1 0 X X 24 bit register 1 1 X X 32 bit register 0 1 0 0 illegal combination 0 1 1 0 48 bit register 0 1 1 1 56 bit register 0 1 0 1 64 bit register
Reset State: ECCCON= 20H (ie. RESET=1)		

ECC16 **72H** **Read Only**

ECC DATA		
BIT	**NAME**	**DESCRIPTION**
0	ECC0/48	ECC REGISTER LEADING BITS - This bit reflects the OR of all the ECC register bits from the input stage through bit 48. For 16 bit operation, this is bit 48. For 24 bit operation this is bit 40 + bit 41 + .. + bit 48. For 64 bit operation, this is bit 0 + bit 1 + ... + bit 48.
1-7	ECC49-ECC55	ECC REGISTER BITS - These bits reflect the output of ECC shift register stages 49 to 55.
Reset State: Unknown		

ECC24 **73H** **Read Only**

ECC DATA		
BIT	**NAME**	**DESCRIPTION**
0-7	ECC56-ECC63	ECC REGISTER BITS - These bits reflect the output of ECC shift register stages 56 to 63.
Reset State: Unknown		

ECC REGISTERS (continued)

POLY0 **64H** **Write Only**

ECC POLYNOMIAL		
BIT	**NAME**	**DESCRIPTION**
0-7	F0-F7	ECC POLYNOMIAL FEEDBACK - These bits enable or disable exclusive OR feedback of both the shift register output (bit 31) and the serial input to the output of shift register stages 0 to 7. These settings may be overriden by the FEEDINH bit in ECCCON. For ECC register lengths other than 64 bits, F0-F7 are irrelevant.
Reset State: POLY0 = 00H		

POLY8 **65H** **Write Only**

ECC POLYNOMIAL		
BIT	**NAME**	**DESCRIPTION**
0-7	F8-F15	ECC POLYNOMIAL FEEDBACK - These bits enable or disable exclusive OR feedback to the output of shift register stages 8 to 15. For register lengths other than 56 or 64 bits, F8-F15 are irrelevant.
Reset State: POLY8 = 00H		

POLY16 **66H** **Write Only**

ECC POLYNOMIAL		
BIT	**NAME**	**DESCRIPTION**
0-7	F16-F23	ECC POLYNOMIAL FEEDBACK - These bits enable or disable exclusive OR feedback to the output of shift register stages 16 to 23. For ECC register lengths other than 56 or 64 bits, F16-F23 are irrelevant.
Reset State: POLY16 = 00H		

ECC REGISTERS (continued)

POLY24 67H Write Only

ECC POLYNOMIAL		
BIT	**NAME**	**DESCRIPTION**
0-6	F24-F30	ECC POLYNOMIAL FEEDBACK - These bits enable or disable exclusive OR feedback to the output of shift register stages 24 to 30. For ECC register lengths of 16, 24 or 32 bits, F24-F30 are irrelevant.
7	unused	
Reset State: POLY24 = 00H		

POLY32 74H Write Only

ECC POLYNOMIAL		
BIT	**NAME**	**DESCRIPTION**
0-7	F32-F39	ECC POLYNOMIAL FEEDBACK - These bits enable or disable exclusive OR feedback of both the shift register output (bit 63) and the serial input to the output of shift register stages 32 to 39. These settings may be overriden by the FEEDINH bit in ECCCON. For ECC register lengths of 16 or 24 bits, F32-F39 are irrelevant.
Reset State: POLY32 = 00H		

POLY40 75H Write Only

ECC POLYNOMIAL		
BIT	**NAME**	**DESCRIPTION**
0-7	F40-F47	ECC POLYNOMIAL FEEDBACK - These bits enable or disable exclusive OR feedback to the output of shift register stages 40 to 47. For register lengths of 16 bits, F40-F47 are irrelevant.
Reset State: POLY40 = 00H		

ECC REGISTERS (continued)

POLY48 **76H** **Write Only**

ECC POLYNOMIAL		
BIT	**NAME**	**DESCRIPTION**
0-7	F48-F55	ECC POLYNOMIAL FEEDBACK - These bits enable or disable exclusive OR feedback to the output of shift register stages 48 to 55.
Reset State: POLY48 = 00H		

POLY56 **77H** **Write Only**

ECC POLYNOMIAL		
BIT	**NAME**	**DESCRIPTION**
0-6	F56-F62	ECC POLYNOMIAL FEEDBACK - These bits enable or disable exclusive OR feedback to the output of shift register stages 56 to 62.
7	unused	
Reset State: POLY56 = 00H		

EXTENSION REGISTERS

EXT **63H** **Write Only**

BIT	NAME	DESCRIPTION
0-1	LEN2-LEN3	Used to select ECC register length. Please see ECCCON description for detail. Only in effect if LEN0 & LEN1 of ECCCON are 01 pattern.
4	MODE1	If LEN0 & LEN1 of ECCCON are 01 pattern, this bit selects Mode 1 if it is set. Otherwise, Mode 0 is selected. When in Mode 1, a 16-bit CRC is enabled, and the sequencer RAM control field has a different control arrangement. Please see description of SEQCONF (A0H-BFH).

SEQUENCER STATUS AND CONTROL REGISTERS

The sequencer controls all the time-critical interactions with the peripheral storage device being controlled by the SSI 32C452A. The instructions directly control disk drive interface lines, provide data for writing or comparison, determine the number of bytes handled and control the sequence of instruction execution. It is programmed by the user for maximum capability and variability. There are 31 instructions which are 32 bits wide. They are divided in to 4 byte wide fields. These fields are sequencer address, control, data type and data fields. These may be further divided into subfields as described in detail below. Examples are shown in the Applications Information section at the end of this data sheet.

The next address field of the sequencer instruction contains address and branching information. Each instruction is executed for the duration of the number of byte times specified in its count field. The specified count is loaded into a down counter which clocks every 8 bit times. When the counter underflows execution of that instruction is terminated. A carry inhibit feature allows the counter to wrap around to a full count for fields which are more than 256 bytes long. Execution is passed to the instruction at the specified next address, unless a branch condition is specifed in the instruction (eg. ECC error or successful data comparison). In that case, execution passes to the address specified in the SEQBR register. Sequencer operation may also be conditionally stopped. The sequencer will always stop if execution passes to address 1FH, which is outside of the 28 word instruction control store.

The control field of the sequencer instruction is used to specify the state of RG and WG, to move data to the stack and to select data transfer or data comparison operations. The count field sets the duration of each instruction in byte times and is also used to select the type of data written, such as address marks or ECC bytes.

SEQBR 78H **Read/Write**

SEQUENCER BRANCH ADDRESS		
BIT	**NAME**	**DESCRIPTION**
0-4	BRADR0 - BRADR4	BRANCH ADDRESS BITS - When a sequencer instruction with a branch condition is finished (ie. the specified number of byte times have elapsed) and the specified condition did occur, execution will resume at this 5 bit address.
5-7	unused	
Reset State: Unknown		

SEQADDR 79H **Write Only**

SEQUENCER START ADDRESS		
BIT	**NAME**	**DESCRIPTION**
0-4	STADR0 - STADR4	SEQUENCER START ADDRESS BITS - If the sequencer is currently halted, (Bit 4 of Register 79, SEQSTAT, is set) writing this register with an address in the range 00H to 1EH will cause sequencer execution to commence at that address. If this register is written with 1FH , the sequencer will halt.
5-7	unused	
Reset State: Unknown		

SEQSTAT 79H Read Only

SEQUENCER STATUS		
BIT	**NAME**	**DESCRIPTION**
0	COMPEQ	COMPARE EQUAL - When a sequencer instruction enables the comparison operation, this bit reflects the result of all the byte comparisons performed (ie. if it is set then all bytes compared so far have been equal.) If RG is enabled, the comparisons occur between the instruction's data field and the data bytes being read (or buffer memory if the SEARCHOP bit in OPCON is true as well).
1	COMPLO	COMPARE LOW - Similar to COMPEQ, except that it indicates that in all comparisons the data field was smaller than the compared byte.
2	ECCERR	ECC ERROR - This bit is set during RG active, upon reading the last ECC bit, if there was an error in the data read. The error syndrome will be stored in the ECC registers.
3	not used	
4	STOPPED	SEQUENCER STOPPED - This bit is set when the sequencer is stopped and its instruction address is 1FH.
5	BRACTIVE	BRANCH ACTIVE - This is set when the branch condition specified in the current instruction has been satisfied. This means that the next address used will be taken from the SEQBR register. This bit is reset when the microprocessor reads this register.
6	DATATRANS	DATA TRANSFER - This bit is set when the current sequencer instruction is causing data to be transferred between the buffer memory and the peripheral device. This distinguishes the activity from a search or verification operation.
7	AMACTIVE	ADDRESS MARK ACTIVE - This bit is set when the controller reads or writes an address mark or sync byte. It is reset after the ECC bytes are read or written, or when the sequencer is halted.
Reset State: 00H		

SEQUENCER INSTRUCTION REGISTERS

The 4 fields of 8 bits comprising a single sequencer instruction are detailed below. They are presented as arrays of 31 bytes each, corresponding to the 31 instructions at sequencer addresses 0 to 1EH.

SEQADRF(n) 80H-9EH Read/Write

SEQUENCER ADDRESS FIELD ARRAY			
BIT	**NAME**	**DESCRIPTION**	
0-4	NEXT0-NEXT4	NEXT ADDRESS FIELD - This 5 bit field specifies the address of the next instruction to be executed when the current instruction has continued for the specified number of bytes.	
5-7	BRCON0 -BRCON2	BRANCH CONTROL FIELD - This 3 bit field specifies the branch condition for the current instruction. When a branch condition is satisfied, execution of the current instruction is not curtailed. It continues to execute for the full byte count specifed, and then the sequencer proceeds with execution of the address specified in SEQBR. The branch condition used depends on the state of RG and data type field (see SEQTYPF). If RG is true and ECC bytes are being read, the following branch conditions apply:	
		BRCON2/1/0=	000 No branch
			001 Stop on ECC error
			010 Stop on comparison error
			011 Stop on ECC or comparison error
			100 Branch on good ECC and comparison
			101 Branch on ECC error
			110 Branch on comparison error
			111 Branch on ECC or comparison error
		Otherwise, the branch conditions are:	
		BRCON2/1/0=	000 No branch
			001 Stop if INPUT pin active
			010 Stop if INDEX or SECTOR pin active (see SECTBR bit of register ECCCON).
			011 Stop if comparison error
			100 Branch on carry (from byte counter).
			101 Branch on ECC error
			110 Branch if INDEX or SECTOR pin active (see SECTBR bit of register ECCCON).
			111 Branch on comparison error
Reset State: The contents of the sequencer RAM are unchanged.			

SEQUENCER INSTRUCTION REGISTERS (continued)

SEQCONF(n) A0H-BEH Read/Write

SEQUENCER CONTROL FIELD ARRAY		
BIT	**NAME**	**DESCRIPTION**
0	DATEN	DATA TRANSFER ENABLE - When this bit is set, the SSI 32C452A will generate $\overline{CLKB}$ requests to transfer data bytes to or from buffer memory, depending on whether WG or RG is active.
1	COMPEN	COMPARE ENABLE - When this bit is set and RG is active, read data bytes from the peripheral will be compared with the instruction data field (SEARCHOP reset in the OPCON register) or the buffer memory data (SEARCHOP set). The results of the comparisons are OR'ed together for the duration of the instruction and can be used for a branch condition or tested by the microprocessor.
2	OUTPIN	OUPUT PIN CONTROL - This bit appears on the OUTPUT pin and may be used to synchronize external circuitry to the sequencer.
3	NRZINH	NRZ DATA INHIBIT - When RG is active and this bit is set, the NRZ data input will be ignored. This is useful while external data recovery circuits start up.
4	STACKEN	STACK WRITE ENABLE - While this bit is set, bytes of NRZ data are pushed onto the recirculating stack.
5	RESWG	RESET WRITE GATE MODE 0 - Used to turn off WG signal. WG latch will be cleared at carry and bit ring 4 time when the sequencer word with this bit set is executed. WG latch is also reset when the sequencer comes to the stop state. Note: RG latch is always reset at the end of ECC.
		MODE 1 - CRC Select: 1 = ECC generates or checks a fixed 16-bit CRC. 0 = Normal ECC function. This bit must stay on or off from the time RG or WG is turned on until they are turned off.
6	SETRG	SET READ GATE MODE 0 - RG signal will be set when the sequencer word with this bit set is executed. The RG latch will be reset at the end of ECC or when the sequencer goes to the stopped state. RG latch will not be set if WG is already on. The output of RG latch is connected to the RG pin.
7	SETWG	SET WRITE GATE MODE 0 - WG signal will be set when the sequencer word with this bit set is executed. The WG latch will be set at bit ring 4 time. After this is set, WG control will be reset by executing a sequencer word with RESET WG bit set or when the sequencer goes to the stopped state. WG latch will not be set if RG is already set. The output of the WG latch is connected to the WG pin.

SEQUENCERS INSTRUCTION REGISTERS (continued)

BIT	NAME	DESCRIPTION
6, 7	SETRG, SETWG	MODE 1 - Bit 7 = 0, Bit 6 = 0 - No Operation.
		MODE 1 - Bit 7 = 0, Bit 6 = 1 - Set Read Gate: RG signal will be turned on when the sequencer word with this bit pattern is executed. This pattern is equivalent to setting bit 6 in mode 0. Please refer to the paragraph describing Bit 6 in Mode 0 for functional details.
		MODE 1 - Bit 7 = 1, Bit 6 = 0 - Set Write Gate: WG signal will be set when the sequencer word with this bit pattern is executed. This pattern is equivalent to setting bit 7 in mode 0. Please refer to the paragraph describing Bit 7 in Mode 0 for functional details.
		MODE 1 - Bit 7 = 1, Bit 6 = 1 - Reset Write Gate: This is equivalent to setting bit 5 in mode 0. The WG signal will be turned off when the sequencer word with this pattern is executed. Please refer to the paragraph describing Bit 5 in Mode 0 for functional details.
Note: Mode 0 - Bit 4 of register 63 is 0, the default. Mode 1 - Bit 4 of register 63 is 1.		
Reset State: The contents of the sequencer RAM are unchanged.		

SEQTYPF(n) C0H-DEH Read/Write

SEQUENCER DATA TYPE FIELD ARRAY		
BIT	**NAME**	**DESCRIPTION**
0-4	CNT0-CNT4	COUNT FIELD - The current sequencer instruction is executed for the number of byte times specified by the count field. If the DATEN bit is set, the count is specified as an 8 bit quantity (CNT0-CNT7). If DATEN is reset, the count is specified as a 5 bit quantity (CNT0-CNT4), and the upper three bits of this instruction field are interpreted as data type bits, described below.
5	CNT5/DTYP0	COUNT BIT 5 OR DATA TYPE 0 - When this bit is interpreted as a data type bit, it is used to initialize the bit ring with a single 1. This will occur at the next $\overline{\text{CLKA}}$ cycle. This starts $\overline{\text{CLKB}}$ so that write data bytes will be fetched from buffer memory. The bit ring will be cleared after the ECC is written.
6	CNT6/DTYP1	COUNT BIT 6 OR DATA TYPE BIT 1 - When this bit is interpreted as a data type bit, it indicates that ECC information is being read or written.
7	CNT7/DTYP2	COUNT BIT 7 OR DATA TYPE BIT 2 - When this bit is being interpreted as a data type bit it indicates that an address mark is being written.
Note: When DATEN is reset, and CNT5/DTYP0, CNT6/DTYP1 and CNT7/DTYP2 are being interpreted as data type select bits, the upper 3 bits of the byte counter are forced to 0 regardless of the settings of the data type bits. When all 3 data type bits are 0, the data field is interpreted as normal binary data.		
Reset State: The contents of the sequencer RAM are unchanged		

SEQUENCER INSTRUCTION REGISTERS (continued)

SEQDATF E0H-FEH Read/Write

SEQUENCER DATA FIELD ARRAY		
BIT	**NAME**	**DESCRIPTION**
0-7	DAT0-DAT7	DATA FIELD - When RG is active, the byte in this field is used for comparison operations. If WG is active, DATATRANS is set and TRANSINH (Transfer Inhibit bit in OPCON register) is set, the write data will come from this field. This allows the sequencer to generate the necessary overhead bytes while writing a sector.
Reset State: The contents of the sequencer RAM are unchanged.		

DISK DRIVE INTERFACE REGISTERS

The disk drive interface registers provide control and status for the interface of the SSI 32C452A to the disk drive (peripheral device), and for data transfer to the buffer or host.

OPCON 7AH Read/Write

OPERATION CONTROL WORD		
BIT	**NAME**	**DESCRIPTION**
0	INDEXP	INDEX PULSE DETECTED - This bit is set when an index pulse is encountered and reset each time the register is read. The bit will be reset even if the INDEX pin is true during the access.
1	SECTORP	SECTOR PULSE DETECTED - This bit is set when a sector pulse is encountered and cleared each time the register is read. The bit will be cleared even if the SECTOR pin is true during the read access. This bit is only used with hard-sectored disk drives.
2	NRZDAT	NRZ DATA IN - This bit is set when a rising edge is detected on the NRZ pin and RG is active. It is reset when the register is read.
3	UNUSED	
4	SEARCHOP	SEARCH OPERATION - Setting this bit will cause comparisons to occur between the contents of the buffer memory and the read data bytes from the peripheral. If SEARCHOP is reset, then read data bytes will be compared to the sequencer instruction data field.

DISK DRIVE INTERFACE REGISTERS (continued)

BIT	NAME	DESCRIPTION
5	TRANSINH	DATA TRANSFER INHIBIT - If WG is active and this bit is set, then the write data will come from the sequencer instruction data field instead of the buffer memory. If RG is active and this bit is set, then the read data bytes are used for comparisons only and are not written to buffer memory. Setting this bit will suppress $\overline{\text{CLKB}}$ so that no buffer memory transfers occur.
6	Unused	
7	CARRYINH	SEQUENCER COUNTER CARRY INHIBIT - When this bit is set, the sequencer will not detect a carry (underflow) in its byte counter. This bit is reset when a carry occurs.
Reset State: Bits 7, 5, 4, 2-0 are reset to 0; Bits 6, 3 are unknown		

WAMCON 7BH Write Only

WRITE ADDRESS MARK CONTROL		
BIT	**NAME**	**DESCRIPTION**
0-7	AM0-AM7	ADDRESS MARK BITS - When WG is active and the sequencer instruction specifies that an address mark is to be written (DATATRANS is reset, DTYP2 is set) the bits AM0-AM7 will be shifted out on the $\overline{\text{WAM/AMD}}$ pin. The pattern is delayed by two bit times to compensate for the encoder delay.
Reset State: Unknown		

AMDCON 7CH Write Only

ADDRESS MARK DETECT CONTROL		
BIT	**NAME**	**DESCRIPTION**
0-7	AMD0-AMD7	ADDRESS MARK DETECT CONTROL - When RG and the $\overline{\text{WAM/AMD}}$ input are active, the NRZ data stream is compared to the contents of this register. Byte synchronization is established when a match occurs. The number of bits used in the comparison is determined in the CLKCON register.
Reset State: Unknown		

DISK DRIVE INTERFACE REGISTERS (continued)

CLKCON 7FH Write Only

CLOCK CONTROL			
BIT	**NAME**	**DESCRIPTION**	
0-2	SYN0-SYN2	SYNC COMPARE CONTROL - These 3 bits determine which bits in register AMDCON are used when looking for the sync byte, as follows:	
		SYN2/1/0 =	000 Bit 7 used
			001 Bits 7,6 used
			010 Bits 7,6,5 used
			011 Bits 7,6,5,4 used
			100 Bits 7,6,5,4,3 used
			101 Bits 7,6,5,4,3,2 used
			110 Bits 7,6,5,4,3,2,1 used
			111 All bits used
3	CLKINH	CLOCK INHIBIT - When this bit is set, $\overline{CLKA}$ and $\overline{CLKB}$ are forced to a high impedance state.	
4	CLKF0	CLOCK FREQUENCY SELECT - This bit sets the relationship between $\overline{CLKA}$ and RD/REFCLK when data transfers are in progress. When it is set, $\overline{CLKA}$ will be 1/4 the RD/REFCLK frequency and when it is reset, $\overline{CLKA}$ will be 1/2 the RD/REFCLK frequency.	
5	Unused		
6-7	CLKF1-CLKF2	CLOCK FREQUENCY SELECT - These bits determine the relationship between the frequency of $\overline{CLKA}$ and SYSCLK when no data transfers are in progress, as follows:	
		CLKF2/CLKF1=	00 1/4 frequency
			01 1/2 frequency
			10 same frequency
			11 illegal combination
Reset State: Bits 7, 6, 4, 3 are reset to 0; Bits 2-0 are unknown			

STACK 7FH Read Only

TOP OF STACK
This register provides the microprocessor read access to the top of the 8 byte stack. Each read operation causes the stack data to recirculate, with the top of the stack moving to the bottom. When the sequencer writes data to the stack, the byte on the bottom of the stack is lost.

GENERAL PURPOSE INPUT/OUTPUT REGISTERS

GPIOCON 7DH Read/Write

GENERAL PURPOSE I/O CONTROL		
BIT	**NAME**	**DESCRIPTION**
0-3	GPDIR0 -GPDIR3	GENERAL PURPOSE I/O LINE DIRECTION- These bits program the direction of lines GPIO0 to GPIO3. The direction bits are set for outputs and reset for inputs.
4	W6ESEL	$\overline{W6E}$ SELECT - If this bit is set along with GPDIR0, the GPIO0 pin becomes an active low output signal decoding a microprocessor write to location 6EH.
5	R6ESEL	$\overline{R6E}$ SELECT - If this bit is set along with GPDIR1, the GPIO1 pin becomes an active low output signal decoding a microprocessor read from location 6EH.
6	W6FSEL	$\overline{W6F}$ SELECT - If this bit is set along with GPDIR2, the GPIO2 pin becomes an active low output signal decoding a microprocessor write to location 6FH.
7	R6FSEL	$\overline{R6F}$ SELECT - If this bit is set along with GPDIR3, the GPIO3 pin becomes an active low output signal decoding a microprocessor read from location 6FH.
Reset State: Bits 3-0 are reset to 0; Bits 7, 5 are unknown		

GPIODAT 7EH Read/Write

GENERAL PURPOSE I/O DATA		
BIT	**NAME**	**DESCRIPTION**
0-3	GP0-GP3	GENERAL PURPOSE I/O PIN STATUS - These bits represent the state or output data for the GPIO0 to GPIO3 pins, depending on the direction programmed in the GPIOCON register.
4	INPUT	INPUT PIN STATUS - This bit reflects the data on the INPUT pin.
5	OUT	OUTPUT PIN STATUS - This bit reflects the data on the OUTPUT pin. The OUTPUT pin is actually written to by the sequencer.
6-7	Unused	
Note: The GPIOCON register must be initialized before GPIODAT is accessed.		
Reset State: Bits 3-0 are reset to 0 in the output direction and are not reset in the input direction		

MICROPROCESSOR INTERFACE REGISTERS

SPECIAL ADDRESS DECODES 50H-51H Read/Write

Special decodes
Microprocessor accesses to these locations will cause the address/data bus (AD0-AD7) and the buffer data bus (D0-D7) to be bridged together internally (see external register description).

BUFACC 70H Read/Write

BUFFER ACCESS
Microprocessor accesses to this location cause the address/data bus (AD0-AD7) and the buffer data bus (D0-D7) to be bridged together internally. If a read cycle is performed, the data present will be latched into register DLR as well.

EXTERNAL REGISTERS (for reference only)

HOSTL 50H Read/Write

HOST BUS (LOWER BYTE)
External hardware may be used to connect the lower byte of the host bus to the buffer memory when this address is accessed.

HOSTH 51H Read/Write

HOST BUS (UPPER BYTE)
External hardware may be used to connect the upper byte of the host bus to the buffer memory when this address is accessed.

GPREG0 6EH Read/Write

GENERAL PURPOSE REGISTER 0
Systems which need extra I/O on the microprocessor data bus may take advantage of the strobes available on pins GPIO0 (write) and GPIO1 (read) to add an expansion port at this address.

GPREG1 6FH Read/Write

GENERAL PURPOSE REGISTER 1
Systems which need extra I/O on the microprocessor data bus may take advantage of the strobes available on pins GPIO2 (write) and GPIO3 (read) to add an expansion port at this address.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Ambient Temperature Under Bias	0 to 70	° C
Storage Temperature	-65 to 150	° C
Voltage On Any Pin With Respect To Ground	GND -0.5 or VCC + 0.5	V
Power Supply Voltage	7.0	V
Max Current Injection	25	mA

NOTE: Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC Supply Voltage		4.75		5.25	V
TA Operating Free Air Temp.		0		70	° C
Input Low Voltage		0		0.4	V
Input High Voltage		2.4		VCC	V

D. C. CHARACTERISTICS

TA = 0°C to 70°C, VCC = 5V ± 5%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VIL Input Low Voltage		-0.5		0.8	V
VIH Input High Voltage		2.0		VCC + .5	V
VOL Output Low Voltage (WG, RG)	IOL = 4 mA			0.45	V
VOL All Others	IOL = 2 mA			0.45	V
VOH Output High Voltage	IOH = 400 mA			2.4	V
ICCS Supply Current Standby	Inputs at GND or VCC			25	mA
ICC Supply Current				85	mA
Power Dissipation				500	mW

D. C. CHARACTERISTICS (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
IL	Input Leakage	0V < Vin < VCC	-10		10	µA
IOL	Output Leakage	0.45V < Vout < VCC	-10		10	µA
Cin	Input Capacitance				10	pF
Cout	Output Capacitance				10	pF

A. C. TIMING CHARACTERISTICS
TA = 0°C to 70°C, VCC = 5v ± 5%, unless otherwise specified.
Load conditions for all pins is - 30pF. Timing measurements are made at 50% of rising or falling edge.
Note: ↓ indicates falling edge; ↑ indicates rising edge.

MICROPROCESSOR INTERFACE TIMING (See Figure 3.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
S	SYSCLK Period		50			ns
S/2	SYSCLK Assert to De-assert		18			ns
S/2	SYSCLK Rise and Fall	Sr = Sf, S = 60 ns			5	ns
Ta	ALE Width		45			ns
Taw	ALE ↓ to $\overline{WR}$ ↓		25			ns
Tar	ALE ↓ to $\overline{RD}$ ↓		25			ns
Tw	$\overline{WR}$ Width		200			ns
Tr	$\overline{RD}$ Width		200			ns
As	AD0 - AD7 in Valid to ALE ↓		7.5			ns
Ah	ALE ↓ to AD0 - AD7 in Invalid		20			ns
Cs	CS ↑ to ALE ↓		7.5			ns
Ch	$\overline{RD}$ ↑ or $\overline{WR}$ ↑ to CS ↓		0			ns
Wds	AD0 - AD7 in Valid to $\overline{WR}$ ↑		70			ns
Wdh	$\overline{WR}$ ↑ to AD0 - AD7 in Invalid		10			ns
Tda	$\overline{RD}$ ↓ to AD0 - AD7 out Valid				145	ns
Tdh	$\overline{RD}$ ↑ to AD0 - AD7 out Invalid				50	ns

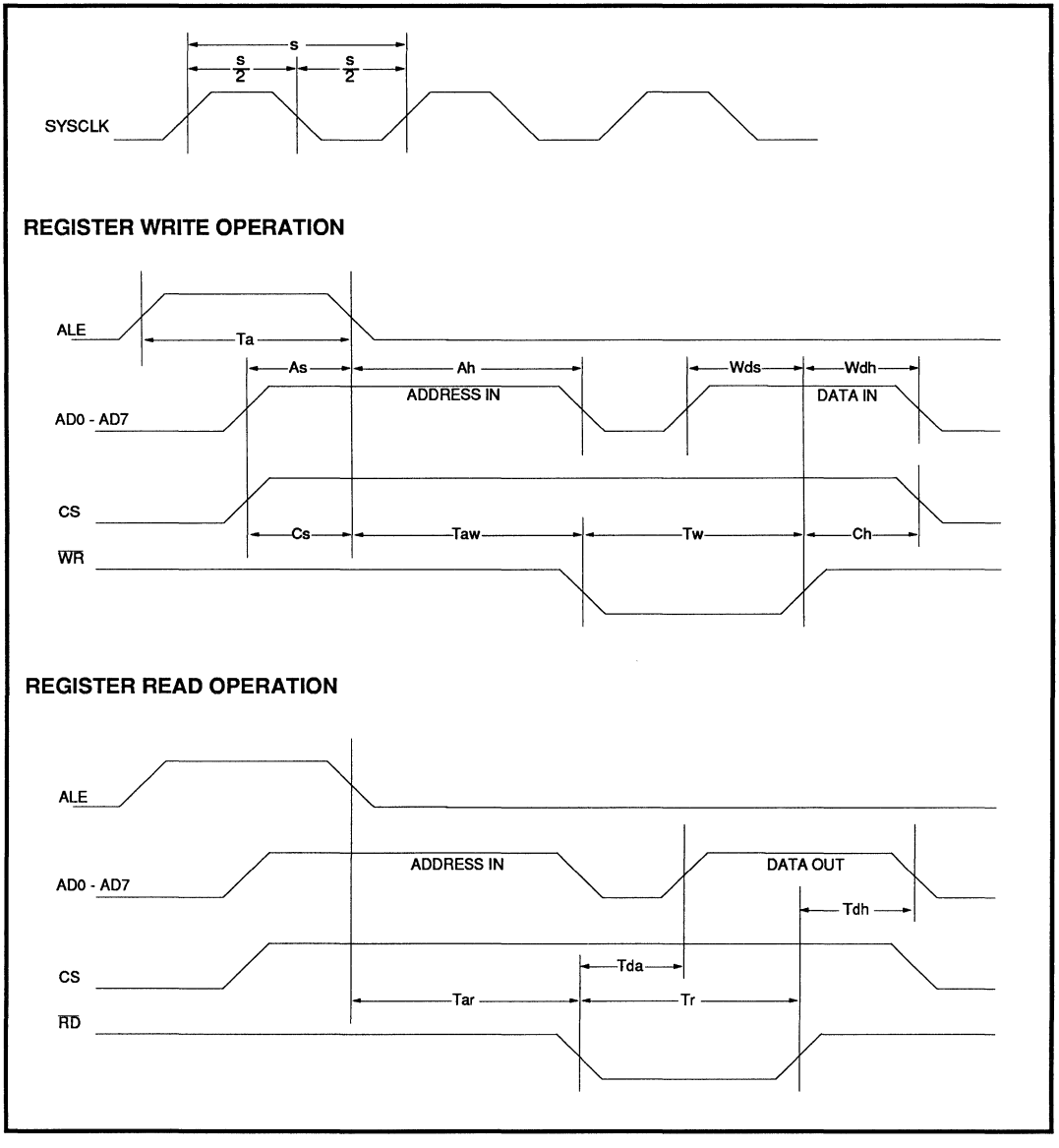


FIGURE 3: MICROPROCESSOR INTERFACE TIMING

A. C. TIMING CHARACTERISTICS (continued)

PERIPHERAL DEVICE INTERFACE TIMING (See Figure 4.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
T	RD/REFCLK Period		50			ns
T/2	RD/REFCLK Assert to De-assert		18			ns
Tr	RD/REFCLK Rise Time	T = 62.5 ns			5	ns
Tf	RD/REFCLK Fall Time	T = 62.5 ns			5	ns
Ds	NRZ in Valid to RD/REFCLK ↑	Set-up time	10			ns
Dh	RD/REFCLK ↑ to NRZ in Invalid	Hold time	7			ns
As	$\overline{AMD}$ ↓ to RD/REFCLK ↑	Set-up time	10			ns
Dv	RD/REFCLK ↑ to NRZ out		7		40	ns
Wv	RD/REFCLK ↑ to $\overline{WAM}$ ↓		7		40	ns
Wvr	RD/REFCLK ↑ to $\overline{WAM}$ ↑		7		40	ns

BUFFER INTERFACE TIMING (See Figure 5.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
T	$\overline{CLKA}$ Period		100			ns
T/2	$\overline{CLKA}$ Assert to De-assert		40			ns
Tba	$\overline{CLKB}$ ↓ to $\overline{CLKA}$ ↓		40			ns
Tab	$\overline{CLKA}$ ↓ to $\overline{CLKB}$ ↑		40			ns
Dov	$\overline{CLKA}$ ↑ to D0 - D7 out Valid		10		50	ns
Doh	$\overline{CLKA}$ ↑ to D0 - D7 out Invalid		0		50	ns
Dis	D0 - D7 in Valid to $\overline{CLKA}$ ↓		25			ns
Dih	$\overline{CLKA}$ ↓ to D0 - D7 in Invalid		10			ns

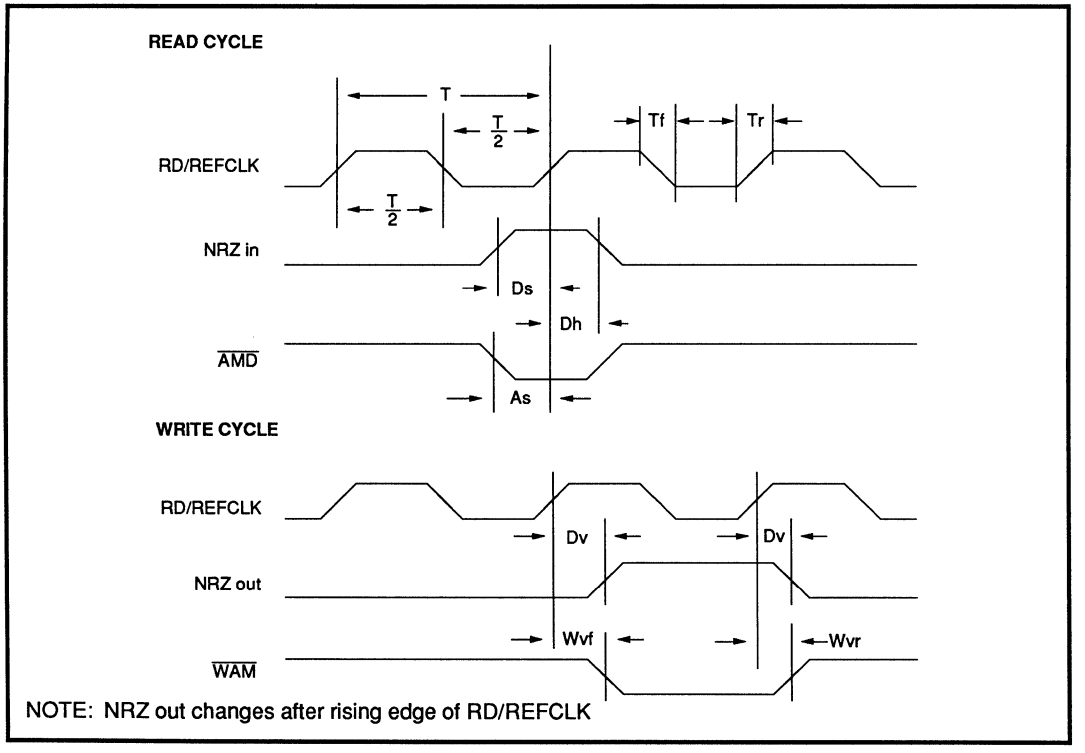


FIGURE 4: PERIPHERAL DEVICE INTERFACE TIMING

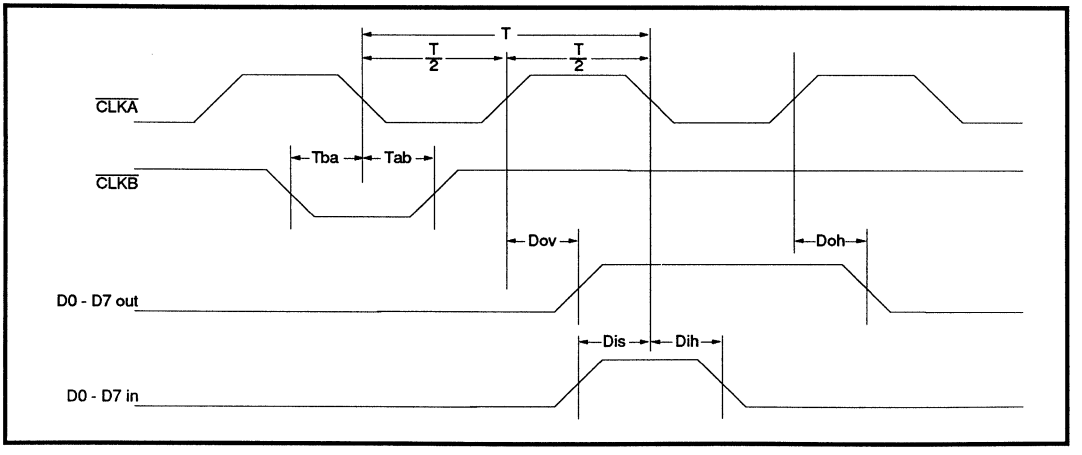


FIGURE 5: BUFFER INTERFACE TIMING

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A. C. TIMING CHARACTERISTICS (continued)

EXTERNAL REGISTER TIMING (See Figure 6.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Tda	D0 - D7 in Valid to AD0 - AD7 out Valid				55	ns
Tra	$\overline{RD}$ ↓ to D0 - D7 in Valid	D0-D7 stable before $\overline{RD}$ ↓			60	ns
Trh	$\overline{RD}$ ↑ to AD0 - AD7 out Invalid				50	ns
Tad	AD0 - AD7 in Valid to D0 - D7 out Valid				55	ns
Twd	$\overline{WR}$ ↓ to D0 - D7 out Valid	AD0-AD7 stable before $\overline{WR}$ ↓			60	ns
Twh	$\overline{WR}$ ↑ to D0 - D7 out Invalid		50			ns

ADDRESS DECODE 6E AND 6F TIMING (See Figure 7.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Tdf	$\overline{RD}$ or $\overline{WR}$ ↓ to Strobe ↓				40	ns
Tdr	$\overline{RD}$ or $\overline{WR}$ ↑ to Strobe ↑				40	ns

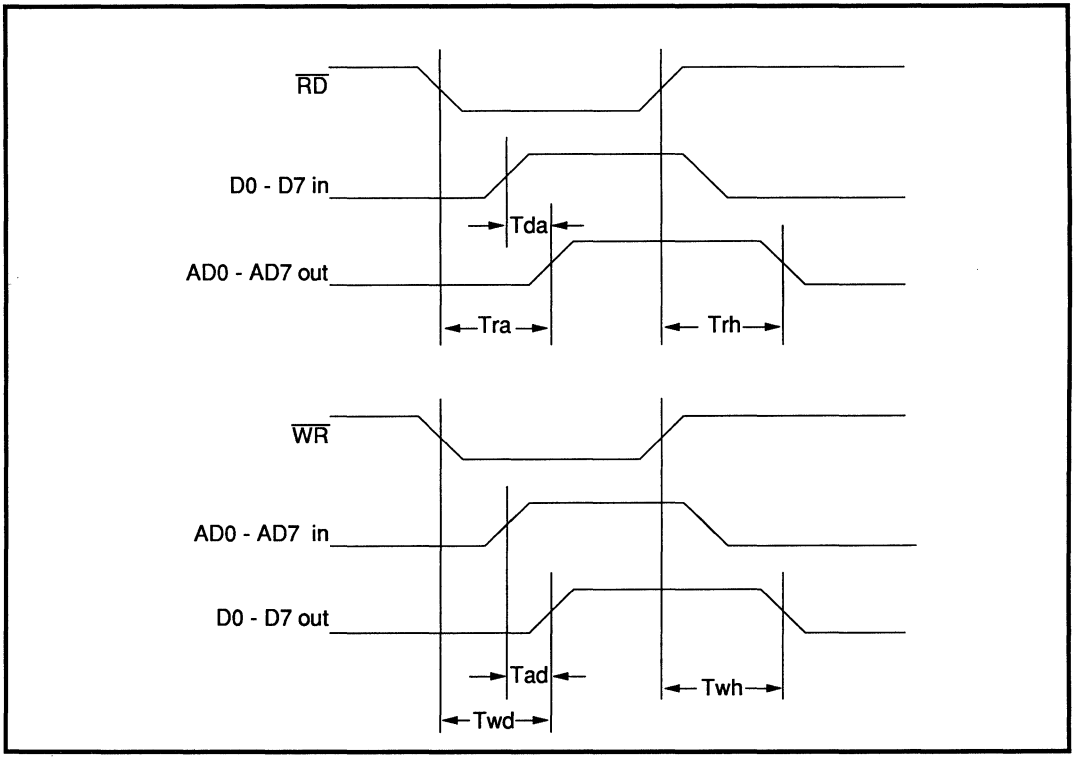


FIGURE 6: EXTERNAL REGISTER TIMING

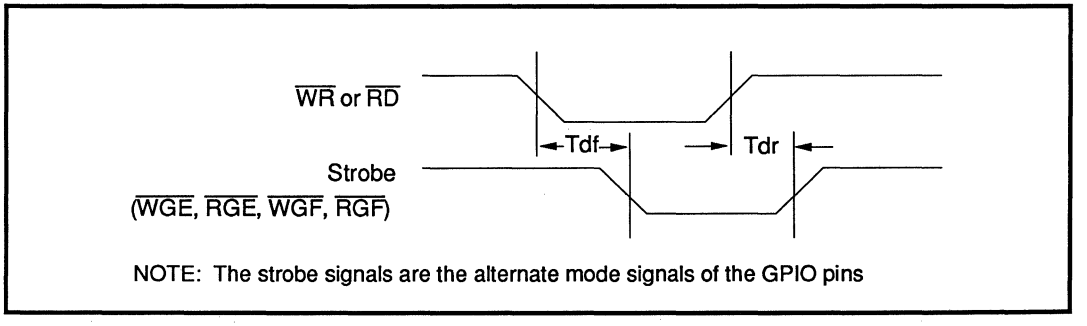


FIGURE 7: ADDRESS DECODE 6E AND 6F TIMING

APPLICATIONS INFORMATION

SEQUENCER PROGRAMMING EXAMPLES

This section describes how specific controller functions are implemented with the SSI 32C452A. Sequencer programming examples for the specific case of an ST-506 Winchester disk drive are given. For convenience, all the code samples start at sequencer address 00H. In an actual implementation, the sequencer intructions would be distributed throughout the sequencer RAM, with common portions reused, so that the code for all operations would be resident simultaneously. All example values are hex quantities.

SECTOR ID

There are two types of Sector ID operation. In the first, the Sector ID field is read and saved by the controller for examination by the microprocessor. The 8 byte internal stack is used for this type of operation and read data is pushed to the stack under the control of the sequencer. In the second, the sector ID field is compared to a desired value in preparation for some other operation, such as sector read or sector write. In this case, the ID field parameters are compared to the data field of the controller instructions. A sequencer branch instruction is used to test for a positive field ID comparison and no ECC error before the rest of the operation proceeds. The microprocessor must program the SEQBR register with the address of the code for the following operation.

The controller establishes byte synchronism by searching for an address mark after RG is asserted. The data pattern of the address mark is specified in the AMDCON register and the number of bits actually used in the pattern is selected by the bits SYN2/1/0.

ADDR INSTRUCTION (SEQADRF SEQCONF SEQTYPF SEQDATF)

```
                                ; ST-506 Sector Identification example. Assumes AMDCON=A1H, SYN2/1/
                                  0=7
00    60 00 00 00               ; Loop here until Index Pulse (SEQBR=01H)
01    02 40 00 00               ; Turn on RG
02    03 02 80 A1               ; Look for address mark ( A1H in ST-506 format)COMPEN=1DTYP2=1
                                  (Address Mark - Data Separator will detect deliberate coding violations and
                                  assert WAM/AMD pin).
03    04 02 00 FE               ; Look for 2nd byte of address mark (FEH - written as normal data - no coding
                                  violations) COMPEN=1
05    06 12 00 NCYL             ; Compare cylinder number (NCYL) and save too. COMPEN=1, STACKEN=1
06    07 12 00 NHEAD            ; Compare head number (NHEAD) and save too. COMPEN=1, STACKEN=1
```

APPLICATIONS INFORMATION (cont.)

SECTOR ID (cont.)

```
ADDR  INSTRUCTION (SEQADRF SEQCONF SEQTYPF SEQDATF)

07    08 12 00 NSECT   ; Compare sector number (NSECT) and save too. COMPEN=1, STACKEN=1

08    89 10 41 00      ; Check ID field ECC and save ECC bytes.Branch to read or write operation
                         if positive comparison on field ID and if ECC was good (SECTBR indicates
                         condition for desired sector operation). DTYP1=1 (ECC byte),
                         STACKEN=1, COUNT=1

0A                     ; Here if sector ID did not match target. Actual ID field and ECC bytes are
                         available on the stack for microprocessor check.
```

SECTOR READ

Once the sector ID field has been verified, the data field may be read. Detection of the address mark for the data portion of the sector proceeds as for ID field address mark, and causes the serializer/deserializer to be correctly synchronized with the incoming data bytes. At the end of a sector read, the microprocessor may check the ECC result to determine if a reread or error correction computation is required.

```
ADDR  INSTRUCTION (SEQADRF SEQCONF SEQTYPF SEQDATF)

                       ; ST-506 Sector Read example assumes that sector ID field verification has
                         been performed.

00    01 40 00 00      ; Turn on RG

01    02 02 A0 A1      ; Look for data field Address Mark (A1H)COMPEN=1DTYP2=1 (AM byte),
                         DTYP0=1, enable CLKB when synchronization occurs.

02    E3 02 00 F8      ; Check second byte of AM. Must be F8H for ST-506 data field. Branch if AM
                         bytes bad.COMPEN=1

03    04 01 FF 00      ; Transfer 256 data bytesDATEN=1COUNT=FFH

04    A5 00 41 00      ; Read ECC bytes, branch on errorDTYP1=1 (ECC)COUNT=1

05                     ; Here if read was error free.
```

APPLICATIONS INFORMATION (cont.)

SECTOR WRITE

Sector writes proceed in a similar fashion to reads. Once the sector ID field has been verified, the sequencer writes a short gap (the 'write splice') and then the sector data, followed by ECC bytes and another gap.

ADDR INSTRUCTION (SEQADRF SEQCONF SEQTYPF SEQDATF)

```
                              ; ST-506 Sector Write exampleAssumes that sector ID field verification has
                                been performed.
00    01 00 02 00             ; Skip 3 bytes
01    02 80 0C 00             ; Turn on WG and write 13 bytes of 00HCOUNT=0CHSETWG=1
02    03 00 A0 A1             ; Write first data AM byte (A1H)DTYP2=1 (AM), DTYP0=1 (Start CLKB*)
03    04 00 00 F8             ; Write second data AM byte (F8H)DTYP2=0 since this byte is written as nor-
                                mal data (no coding violations).
04    05 01 FF 00             ; Write 256 data bytesDATEN=1 (transfer enabled, data comes from buffer
                                memory)COUNT=FFH
05    06 00 41 00             ; Write 2 ECC bytesCOUNT=1DTYP1=1 (ECC)
06    07 00 02 00             ; Write three bytes of 00HCOUNT=2
07    08 20 00 00             ; Turn WG off RESWG=1
08                            ; Here when sector write is finished
```

OPERATIONAL INFORMATION

Sector formatting is similar to sector writing, except that the sector ID field is written in addition to the data field. The data field is also written with a fixed value instead of data transferred from buffer memory. Examples of sequencer code to write specific data are given under sector write. When an entire track is to be written, the microprocessor may update ID field information in the sequencer RAM to reflect the next sector while the sequencer is writing the current data field. This allows an entire track to be formatted in one continuous write operation. Formatting begins after the sequencer detects an index pulse.

A **data search** operation can be implemented by a simple modification to the sequencer programming for sector read operations. When the COMPEN bit of the sequencer control field is enabled, incoming data will be compared to buffer data instead of being stored. This allows the sector to be searched for specific data. (The SEARCHOP bit in the OPCON register must also be set for searches).

Data verification can be performed during a sector read if the TRANSINH bit (data transfer inhibit) of OPCON is enabled, because no data will be written to the buffer. However, ECC checking will continue so that at the end of the sector, the ECC result can be verified.

The controller can support **extended sector sizes** of greater than 256 bytes. One simple way to achieve larger sector sizes is to use several sequencer data transfer instructions in a row. The size of the data block that results will be the sum of the counts for each transfer instruction. Large sectors may also be implemented with a single sequencer instruction by using the CARRYINH bit in OPCON. Sequencer instructions terminate when the carry caused by an underflow of the byte counter is detected. When CARRYINH is set, this carry will not be recognized, so the counter (which is initially loaded with the value specified in each instruction's count field) will wrap around to a full count (FFH). The CARRYINH bit is cleared by an underflow, so that if it is not set again by the microprocessor, the sequencer instruction will terminate after an additional 256 bytes. This permits the sector length to be extended in multiples of 256 bytes.

Multi-sector reads and writes are accomplished in a similar manner to full track formatting. The sequencer is programmed as for a single sector operation. However, when the microprocessor detects that the DATA-TRANS bit in the SEQSTAT register is set (implying that a data transfer is in progress), it alters the ID field information in the sequencer's instruction RAM. When the data transfer for a particular sector is completed, the sequencer is looped back to the same sector ID routine. It will then start a new sector operation using the ID information just loaded by the microprocessor. This type of operation may proceed for an entire track.

ECC IMPLEMENTATION

The ECC hardware may be used for error correction as well as checksum generation. An algorithm for locating and correcting read errors is described below. The algorithm assumes the use of a 32 bit ECC polynomial capable of correcting a single burst of up to 8 bit errors. Longer bursts or multiple bursts may be incorrectable.

1. If an ECC error is detected (ECCERR is set in SEQSTAT) and error correction is needed (ie. multiple reads from the same sector have failed) the error syndrome must be read from the ECC shift register and reloaded in bit-reversed order, as follows:
   1.1 Set FEEDINH in ECCCON.
   1.2 Read and save top 8 bits of shift register from ECC56.
   1.3 Set ECCSHIFT in ECCCON 8 times.
   1.4 Repeat 1.2 and 1.3 until all 4 bytes of the syndrome are RAM.
   1.5 Copy each syndrome bit, starting with the least significant, to ECCIN and set ECCSHIFT after each copy. After 32 such operations the ECC shift register will contain the bit reversed polynomial.
2. The reverse ECC generator polynomial must be written to the ECC generator.
   2.1 Configure the bit-reversed polynomial in the 4 feedback registers, POLY32, POLY40, POLY48 and POLY56. This step is not equivalent to bit reversing the feedback register contents, since the coefficients for x^0 and x^{32} are fixed in hardware. The reverse polynomial is generated by subtracting the exponents from 32. The following is a numerical example to illustrate the programming of forward and reverse polynomials for the 32 bit computer-generated code:

   forward:
   $x^0+x^4+x^6+x^{13}+x^{15}+x^{22}+x^{26}+x^{30}+x^{32}$;

   reverse:
   $x^{32}+x^{28}+x^{26}+x^{19}+x^{17}+x^{10}+x^6+x^2+x^0$;

	Forward	Reverse
POLY32	28H	22H
POLY40	50H	02H
POLY48	20H	05H
POLY56	22H	0AH

   2.2 Reset FEEDINH and ECCIN in the ECCCON register.

ECC IMPLEMENTATION (cont.)

3. The ECC shift register is operated until either the number of shifts exceeds the number of bits in the read block or the 24 least significant bits of the ECC register are zero.

   3.1 Compute block length in bits, including ECC and overhead bits.

   3.2 Initialize a shift counter to zero.

   3.3 Set ECCSHIFT to shift the ECC registers by one, and increment the shift counter.

   3.4 If the shift counter exceeds the block length, stop the computation as this means the errors are uncorrectable. Otherwise, if register ECC48 is non-zero, repeat step 3.3.

4. At this point, ECC56 contains the bit-reversed error pattern and the shift counter indicates its displacement from the end of the block. The pattern must be mirrored and aligned to byte boundaries so that the errors in the buffer storage may be corrected.

   4.1 Subtract 7 from the shift counter, to compensate for a hardware offset internal to the SSI 32C452A.

   4.2 Subtract 32 from the shift counter. (This is the number of the ECC bits). If the result is less than zero then no further action is required, since the errors occurred in the ECC portion of the block.

   4.3 Read the contents of ECC56 into RAM and bit-reverse this 8 bit quantity.

   4.4 Form a 16 bit word with the reversed error pattern as its lower byte and zero as its upper byte.

   4.5 If the lowest three bits of the shift counter are non-zero, left shift the 16 bit word and decrement the shift counter.

   4.6 Repeat 4.5 until the shift counter's three least significant bits are zero.

   4.7 Divide the shift counter by 8, to convert bits into bytes.

5. The position and nature of the errors are now known, so they may be corrected as follows:

   5.1 Exclusive OR the lower byte of the error word with the data byte whose offset from the end of the data block is given by the value of the shift counter.

   5.2 Exclusive OR the upper byte of the error word with the data byte whose offset from the end of the data block is one more than the value of the shift counter.

The above procedure will correct a single burst of errors, provided that the degree of the error is within the capability of the chosen code. The code whose polynomial is illustrated above is capable of correcting a single burst of up to 8 error bits.

Since the error correction process is time consuming and ties up the ECC hardware, blocks with errors should be re-read to ensure that the errors observed are in fact hard errors.

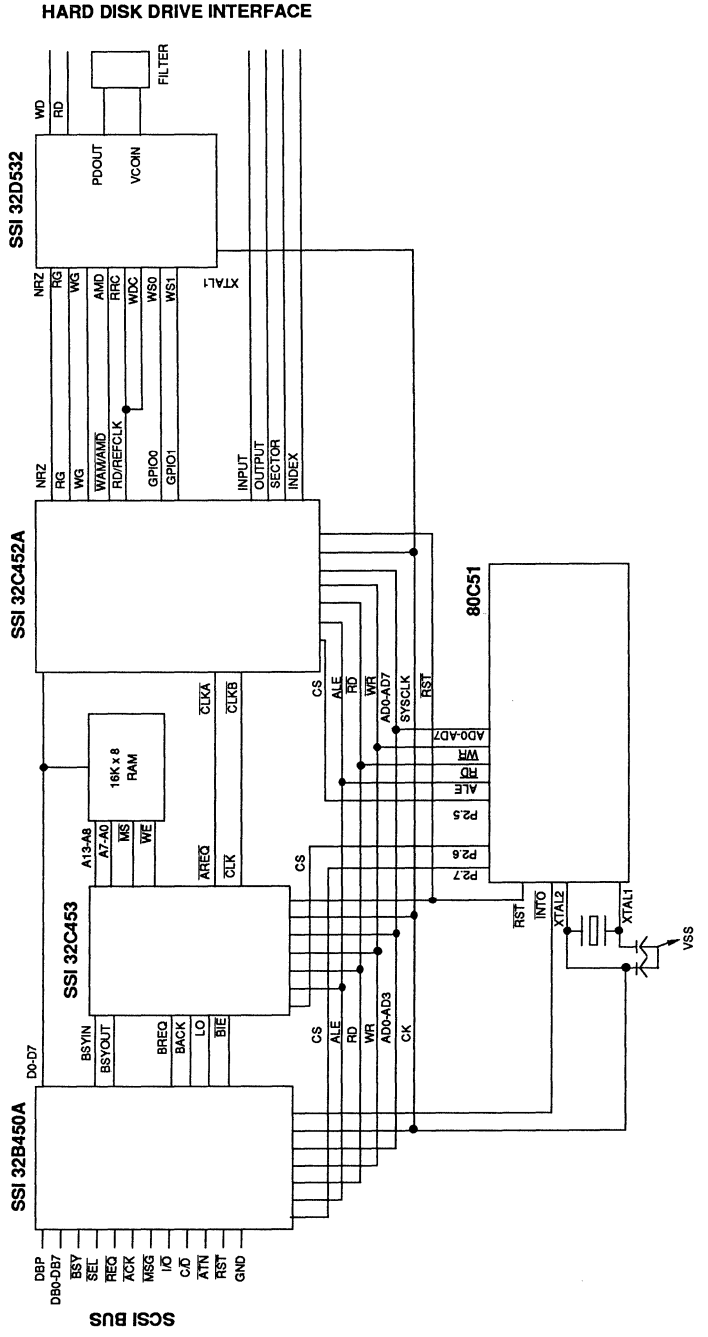
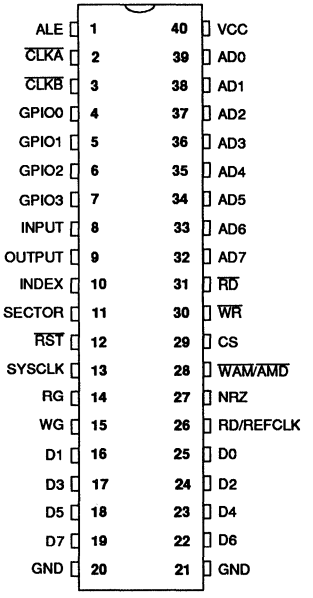


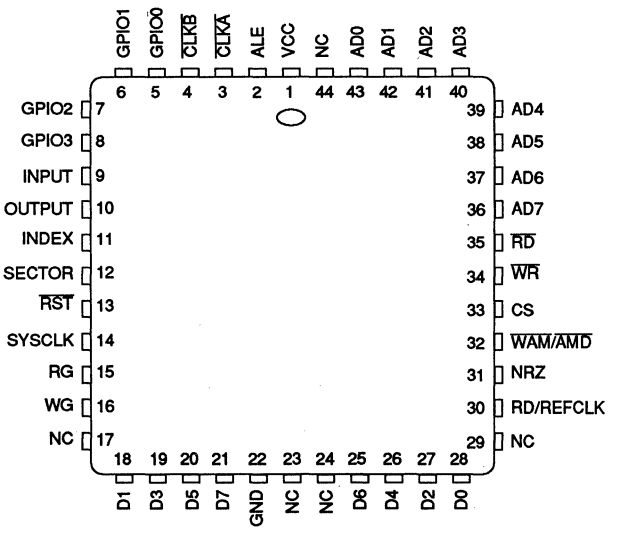
FIGURE 8: SCSI PERIPHERAL CONTROLLER CHIP SET

SSI 32C452A
Storage Controller

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



DIP



PLCC

ORDERING INFORMATION

PART DESCRIPTION		ORDER NO.	PKG. MARK
SSI 32C452A Storage Controller	40 Pin DIP	SSI 32C452A-CP	32C452A-CP
	44 Pin PLCC	SSI 32C452A-CH	32C452A-CH

silicon systems™
Silicon Systems, Inc.,14351 Myford Road, Tustin CA 92680, (714) 731-7110, TWX 910-595-2809

silicon systems™
INNOVATORS IN INTEGRATION

SSI 32C453
Dual Port Buffer Controller

August, 1988

DESCRIPTION

The SSI 32C453 Dual Port Buffer Controller is a CMOS device that allows low speed RAM to be configured as a dual port circular FIFO buffer. It generates all the buffer memory addressing required and manages two ports: Port A, a synchronous peripheral device interface and Port B, an asynchronous host interface. The SSI 32C453 has arbitration logic to support the SCSI protocol, host DMA transfers and uninterruptible peripheral block transfers.

On-chip counters generate the addresses needed to access the external RAM. In extended addressing mode, 16 bits of address are multiplexed onto 8 lines and the necessary strobes are provided. Direct addressing mode may be used for 10 bit addresses (DIP package) or 14 bit addresses (PLCC package) without multiplexing.

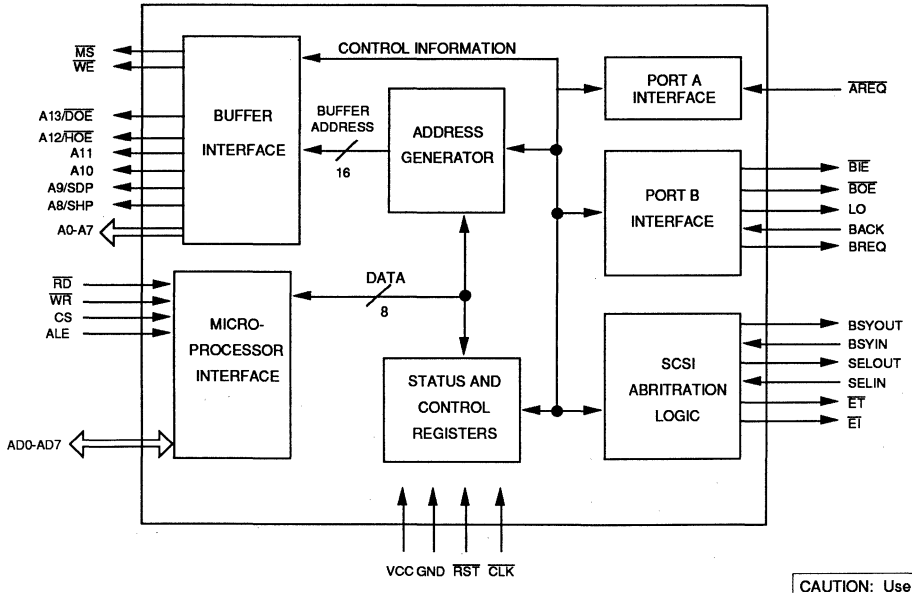
The SSI 32C453 is intended for use in intelligent controllers and includes a set of configuration/status registers which are accessed through the microprocessor interface. It is optimized for 8 bit, multiplexed address/

FEATURES

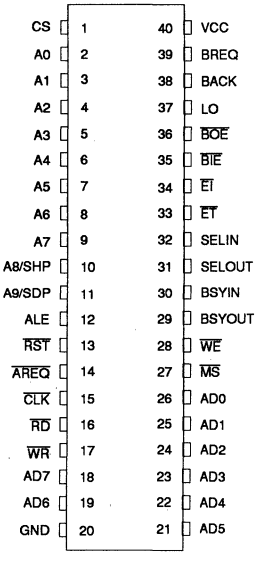
- **Dual port circular FIFO buffer controller**
- **SCSI bus arbitration control**
- **DMA handshake control**
- **Multiplexed mode buffer addressing up to 64 Kbytes**
- **Direct mode buffer addressing up to 1 Kbyte (DIP) or 16 Kbytes (PLCC)**
- **High speed CMOS device has 16 MHz microprocessor interface**
- **Compatible with SSI 32C452 Storage Controller**
- **Plug and software compatible with AIC-300 buffer controller**
- **Single 5V supply**
- **Available in 44-pin PLCC or 40-pin DIP package**

6

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

data bus processors such as the 8085 or 8051, and will also interface easily to most 8 bit microprocessors. The registers allow the designer to select buffer RAM sizes, manipulate the internal address pointers and sense impending overruns of the buffer.

The SSI 453 provides a cost-effective buffer memory and SCSI port control solution, and when used in conjunction with an 8 bit microprocessor and a peripheral controller device, such as the SSI 452, it forms the basis for an intelligent, high performance Winchester disk drive control system.

FUNCTIONAL DESCRIPTION

The major functional elements and data paths of the SSI 453 are shown in the block diagram. Data transfers are requested through two ports, Port A and Port B. The direction of and number of bytes to be transferred are determined by the setting of the status and control register. All buffer memory transfers are synchronous with the $\overline{CLK}$ signal.

The **Port A interface** communicates with the peripheral device controller. The $\overline{AREQ}$ signal is monitored by the SSI 453 and when asserted begins the Port A data transfer. The SSI 453 then generates the necessary address and control signal to coordinate data transfer between buffer and peripheral device.

The **Port B interface** communicates with the host bus. It supports a two wire request/acknowledge protocol for transferring data asynchronously, and generates the necessary strobes, LO and $\overline{BOE}$, for controlling and external latch and three-state drivers for host bus access.

Since peripheral data transfers occur synchronously and in blocks, Port A requests are alway honored over Port B requests. If the speed of the data transfer from the peripheral device allows, the SSI 453 has the capability to alternate Port A and Port B data transfers so that time is not lost waiting on the peripheral device.

The **buffer interface** generates buffer memory read and write cycles during data transfers and presents either the Port A or Port B address to the memory. Its memory address lines can be operated in one of two user selectable modes, supporting buffer sizes from 256 bytes to 64 Kbytes. In direct addressing mode, the buffer address is available on either 10 lines (A0-A9) or 14 lines (A0-A13), depending on the chosen buffer size. If larger buffer sizes are required, extended addressing mode supports up to 16 address lines multiplexed onto pins A0-A7. Two external 8 bit three-state latches must be provided to hold the upper 8 bits of the Port A and Port B addresses. The buffer interface provides the signals SDP and SHP for clocking the latches, and $\overline{DOE}$ and $\overline{HOE}$ for enabling the latch outputs at the appropriate times.

The **address generator** contains two 16 bit pointers, the read address pointer (RAP) and the write address pointer (WAP), which indicate where in the external buffer RAM data is to be read or written. During data transfers, these pointers are automatically incremented as the RAM is accessed. The pointers wrap around to 0 when the programmed buffer size is exceeded. To prevent host overruns of the buffer (caused by one of the pointers overtaking the other), the address generator includes a 16 bit stop pointer (SP). The microprocessor loads SP with the last address in buffer memory to be accessed during a host DMA transfer. When the port B address (RAP during an upload to the host or WAP during a download to the peripheral) reaches the value in SP, the DMA transfer is automatically suspended.

The SSI 453 includes the necessary logic to request a **SCSI arbitration** phase. When the microprocessor enables the SCSI logic, it will wait for a 'bus free' condition and then request arbitration. The microprocessor must generate the device address and determine whether the arbitration was favorable or not. Two output pins $\overline{EI}$ and $\overline{ET}$, are provided to allow the SSI 453 to be identified as either a target or an initiator.

The **microprocessor interface** decodes microprocessor read and write requests and provides access to the appropriate status or control register location. Since both data and address information are carried on the bus lines AD0-AD7, the microprocessor signal ALE (address latch enable) is used to indicate the presence of a valid address on the bus.

The **status and control registers** contain operational status for, and control information from, the microprocessor. They include data transfer and port status and information such as transfer complete or current address. The control registers configure the SSI 453 with parameters such as buffer size, read and write pointers and stop pointer.

PIN DESCRIPTION

GENERAL

NAME	DIP	PLCC	TYPE	DESCRIPTION
VCC	40	1		POWER SUPPLY +5 volts
GND	20-21	22		GROUND
$\overline{RST}$	13	14	I	RESET - Active low signal sets reset bit in RESCON and resets all other registers.
$\overline{CLK}$	15	16	I	MASTER CLOCK - All buffer memory transfers occur on a falling edge of $\overline{CLK}$. There should be at least two $\overline{CLK}$ cycles per byte transferred to allow the host and peripheral to remain in step.

MICROPROCESSOR INTERFACE

CS	1	2	I	CHIP SELECT- Active high signal enables device to respond to microprocessor read or write.
ALE	12	13	I	ADDRESS LATCH ENABLE - Falling edge latches register address from AD0-AD7 pins.
$\overline{RD}$	16	18	I	READ STROBE - Active low signal causes the contents of the addressed register to be placed on the address/databus if CS is also active.
$\overline{WR}$	17	19	I	WRITE STROBE - Active low signal causes the data on the address/ data bus to be written to the addressed register if CS is also active.
AD0-AD7	18-19 21-26	20-21 23-28	I/O	ADDRESS/DATABUS - 8 bit bus which carries register address information and bi-directional data.

BUFFER MEMORY INTERFACE

A0-A7	2-9	3-10	O	BUFFER ADDRESS BITS - In direct addressing mode, these are buffer address bits 0 to 7. In extended addressing mode, these lines are multiplexed between low and high order address bytes.
A8/SHP	10	11	O	A8/PORT B (HOST) ADDRESS STROBE - In direct addressing mode, this pin is buffer address bit 8. In extended addressing mode, this pin is an address strobe whose rising edge is used to clock the contents of pins A0-7 into an external latch, for the upper address byte for Port B transfers.

PIN DESCRIPTION (Continued)

BUFFER MEMORY INTERFACE (Continued)

NAME	DIP	PLCC	TYPE	DESCRIPTION
A9/SDP	11	12	O	A9/PORT A (DEVICE) ADDRESS STROBE - In direct addressing mode, this pin is buffer address bit 9. In extended addressing mode,this pin is an address strobe whose rising edge is used to clock the contents of pins A0-7 into an external latch, containing the upper address byte for Port A transfers.
A10-11		17,29	O	Buffer address bits - They are valid in both addressing modes. (PLCC version only)
A12/$\overline{HOE}$		30	O	A12/PORT B (HOST) ADDRESS ENABLE - In direct addressing mode this pin is buffer address bit 12. In extended addressing mode this pin is an active low signal used to enable an external three-state latch which holds the upper address byte for Port B transfers. (PLCC version only)
A13/$\overline{DOE}$		31	O	A13/PORT A (DEVICE) ADDRESS ENABLE - In direct addressing mode this pin is buffer address bit 13. In extended addressing mode this pin is an active low signal used to enable an external three-state latch which holds the upper address byte for Port A transfers. (PLCC version only)
$\overline{MS}$	27	32	O	MEMORY SELECT - This active low output is used to enable the buffer RAM for read or write access.
$\overline{WE}$	28	33	O	WRITE ENABLE - This active low output enables a write to the buffer RAM, in conjunction with $\overline{MS}$. If $\overline{MS}$ is active while $\overline{WE}$ is inactive, the buffer access will be a read operation.

PORT A INTERFACE

$\overline{AREQ}$	14	15	I	PORT A REQUEST - This active low input is sampled on each falling edge of $\overline{CLK}$. If it is low, a Port A transfer will occur on the next falling edge of $\overline{CLK}$.

PORT B INTERFACE

$\overline{BIE}$	35	40	O	PORT B INPUT ENABLE - Active low signal used to enable output of an external three-state driver which presents host bus data to the buffer RAM. This line is asserted either under microprocessor control or as a result of a Port B DMA transfer request (BREQ). Microprocessor control of this line permits direct host to microprocessor transfers.

PIN DESCRIPTION (Continued)

PORT B INTERFACE (Continued)

NAME	DIP	PLCC	TYPE	DESCRIPTION
$\overline{BOE}$	36	41	O	PORT B OUTPUT ENABLE - Active low signal used to enable output of an external three-state driver which holds buffer RAM output and presents it to the host data bus. This line is asserted either under microprocessor control or as a result of a Port B DMA transfer request (BREQ). Microprocessor control of this line permits direct microprocessor to host transfers.
LO	37	42	O	PORT B OUTPUT LATCH - Active high signal controls an external latch which holds buffer RAM output during Port B read operations.
BACK	38	43	I	PORT B ACKNOWLEDGE - Active high input signal from the host indicates that a Port B transfer request has been accepted and that the host bus is available.
BREQ	39	44	O	PORT B REQUEST - Active high output that requests the host to accept a Port B data transfer.

SCSI BUS ARBITRATION

BSYOUT	29	34	O	BUSY OUT - Active high output that is set either by the microprocessor or the arbitration logic and indicates that the SSI 32C453 is requesting control of the SCSI bus.
BSYIN	30	35	I	BUSY IN - Active high input which indicates that another device has control of the bus.
SELOUT	31	36	O	SELECT OUT - Active high output under microprocessor control which is asserted when bus access is granted to the peripheral controller.
SELIN	32	37	I	SELECT IN - Active high input which indicates that another device has been granted access to the bus.
$\overline{ET}$	33	38	O	ENABLE TARGET MODE - Active low output which allows the microprocessor to identify the peripheral controller as a SCSI Target device.
$\overline{EI}$	34	39	O	ENABLE INITIATOR MODE - Active low output which allows the microprocessor to identify the peripheral controller as a SCSI Initiator device.

REGISTER DESCRIPTION

The microprocessor which controls the system has access to all the SSI 32C453 registers through its external memory address space. The SSI 32C453 and its companion device, the SSI 32C452 storage controller, are designed to occupy a single 256 byte page. The 8 bit page address is latched into the SSI 32C453 from pins AD0-AD7 on a falling edge of ALE and remains valid until the next ALE falling edge.

The external registers are described at the end of this section. They are not implemented in either the SSI 32C453 or SSI 32C452, and are assumed to be implemented in external hardware. They are included as an applications suggestion for a 'standard' peripheral controller design.

SSI 32C453 REGISTER BIT MAP

REGISTER	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0	ACCESS
IFCON	52H	BSYOUT	SELOUT	BSYIN	SELIN	BOE	BIE	unused	ARB	R/W
DMACON	53H	TARGET	INIT	DMADONE	ROP/$\overline{WOP}$	RDLATCH	WRLATCH	BACK	unused	R/W
BUFSIZE	54H	BUFFER SIZE								R/W
AMODCON	55H	reserved							AMOD	W
RESCON	59H	unused							RESET	W
RAPL	5AH	READ ADDRESS POINTER (0-7)								R/W
RAPH	5BH	READ ADDRESS POINTER (8-15)								R/W
WAPL	5CH	WRITE ADDRESS POINTER (0-7)								R/W
WAPH	5DH	WRITE ADDRESS POINTER (8-15)								R/W
SPL	5EH	STOP POINTER (0-7)								R/W
SPH	5FH	STOP POINTER (8-15)								R/W

INTERNAL REGISTER DESCRIPTION

IFCON 52H READ/WRITE

INTERFACE CONTROL WORD - Controls and monitors host bus interface and SCSI bus arbitration.		
BIT	**NAME**	**DESCRIPTION**
0	ARB	ARBITRATION - This bit controls the SCSI bus arbitration and returns its status. When it is set, the SSI 32C453 will look for a 'bus free' condition (both SELIN and BSYIN false) and then assert BSYOUT and $\overline{BOE}$, so that the device address may be sent to the host. When ARB is reset, the arbitration activity ceases. When the ARB bit is read it indicates that a SCSI arbitration phase has been recognized if it is set, or not if it is reset.
1	-	unused
2	$\overline{BIE}$	BUS INPUT ENABLE - While this bit is set, the $\overline{BIE}$ output pin will be asserted if the microprocessor reads locations 50H or 51H (see external registers), enabling an external driver to pass host data to the buffer memory. (Note that the $\overline{BIE}$ pin may also be asserted automatically during DMA operations).
3	$\overline{BOE}$	BUS OUTPUT ENABLE - While this bit is set, the $\overline{BOE}$ output pin will be asserted if the microprocessor writes locations 50H or 51H (see external registers), enabling an external three-state latch to drive buffer data onto the host data bus. (Note that the $\overline{BOE}$ pin may also be asserted automatically during DMA operations).
4	SELIN	SELECT IN - This bit reflects the status of the SELIN pin and is read only.
5	BSYIN	BUSY IN - This bit reflects the status of the BSYIN pin and is read only.
6	SELOUT	SELECT OUT - This bit directly controls the SELOUT pin.
7	BSYOUT	BUSY OUT - This bit directly controls the BSYOUT pin.
Reset State: IFCON= 00H		

INTERNAL REGISTER DESCRIPTION (Continued)

DMACON 53H READ/WRITE

DMA CONTROL WORD - Used to initiate and control DMA transfers .		
BIT	**NAME**	**DESCRIPTION**
0	-	unused
1	BACK	PORT B ACKNOWLEDGE - This read only bit reflects the status of the BACK pin, which is set when the host acknowledges a Port B DMA transfer request from the SSI 32C453.
2	WRLATCH	WRITE LATCH - When this bit is set, a host bus to buffer RAM DMA transfer will be initiated. The transfer continues until the address pointer in WAPL/WAPH is equal to the stop value in SPL/SPH. The ROP/$\overline{WOP}$ bit in this register must be cleared. Until WRLATCH is reset, transfers will resume each time the stop pointer is changed.
3	RDLATCH	READ LATCH - When this bit is set, a buffer RAM to host bus DMA transfer will be initiated. The transfer continues until the address pointer in RAPL/RAPH is equal to the stop value in SPL/SPH. The ROP/$\overline{WOP}$ bit in this register must be set. Until RDLATCH is reset, transfers will resume each time the stop pointer is changed.
4	ROP/$\overline{WOP}$	READ/WRITE OPERATION SELECT - This bit determines the direction of DMA to buffer transfer.
5	DMADONE	DMA DONE - This read only bit is set when a DMA transfer is completed (read or write address pointer reaches stop pointer value) and both BREQ and BACK are inactive. It is cleared when the stop pointer is updated.
6	INIT	ENABLE INITIATOR MODE - The value written to this bit is inverted and presented on the $\overline{EI}$ output pin.
7	TARGET	ENABLE TARGET MODE - The value written to this bit is inverted and presented on the $\overline{ET}$ output pin.
Reset State: DMACON=00H		

BUFSIZE 54 READ/WRITE

BUFFER SIZE CONTROL - Used to select buffer size ranging from 256 bytes to 64K bytes. This register contains an 8 bit unsigned value which sets the buffer size as follows: Buffer Size = 256.(BUFSIZE+1) bytes In conjunction with the AMODCON register, this allows buffer sizes from 256 bytes to 64K bytes to be selected in 256 byte increments.
Reset State: BUFSIZE=00H

INTERNAL REGISTER DESCRIPTION (Continued)

AMODCON 55H WRITE ONLY

ADDRESS MODE CONTROL - Used in direct addressing mode (non-multiplexed address lines) to select the number of active address lines (10 or 14).

BIT	NAME	DESCRIPTION
0	AMOD	ADDRESSING MODE - In direct addressing mode, this bit determines the number of address lines supported. If AMOD=1, then 14 lines are supported (A0-A13), and if cleared then 10 lines are supported (A0-A9) .
1-7	-	reserved

The AMOD bit and the value chosen for buffer size (BUFSIZE) together determine the addressing mode used, as follows:

AMOD	BUFSIZE	Addressing Mode	Maximum Buffer Size
0	0-3	Direct (10 lines)	1 Kb
0	4-255	Extended (16 lines multiplexed)	64 Kb
1	0-63	Direct (14 lines - PLCC version only)	16 Kb
1	64-255	Extended (16 lines multiplexed)	64 Kb

Reset State: AMODCON=00H

RESCON 59H WRITE ONLY

RESET CONTROL - Used to return all device registers to a known condition.

BIT	NAME	DESCRIPTION
0	RESET	RESET CONTROL - When this bit is set, all the registers are forced to their reset state. It must be cleared by the microprocessor. It is set either by the microprocessor or by hardware, when $\overline{RST}$ is asserted. When not set, a write to it will reset WAP, RAP and SP.
1-7	-	unused

Reset State: RESCON=01H

INTERNAL REGISTER DESCRIPTION (Continued)

RAPL 5AH READ/WRITE

READ ADDRESS POINTER (LOW BYTE) - Lower 8 bits of address where next data byte will be read from buffer memory during DMA operations. When ROP/$\overline{WOP}$ is set, peripheral data will be read from the buffer RAM at this address and transferred to the host data bus, following a Port B DMA request (BREQ). When ROP/$\overline{WOP}$ is reset, host data will be read from the buffer RAM at this address and transferred to the peripheral, following Port A transfer requests ($\overline{AREQ}$).

RAPH 5BH READ/WRITE

READ ADDRESS POINTER (HIGH BYTE) - Upper 8 bits of address where next data byte will be read from buffer memory.

WAPL 5CH READ/WRITE

WRITE ADDRESS POINTER (LOW BYTE) - Lower 8 bits of address where next data byte will be written to buffer memory. When ROP/$\overline{WOP}$ is set, peripheral data will be written to the buffer RAM at this address, following a Port A transfer request ($\overline{AREQ}$). When ROP/$\overline{WOP}$ is reset, host data will be written to the buffer RAM at this address, following a Port B DMA transfer request (BREQ).

WAPH 5DH READ/WRITE

WRITE ADDRESS POINTER (HIGH BYTE) - Upper 8 bits of address where next data byte will be written to buffer memory.

SPL 5EH READ/WRITE

STOP ADDRESS POINTER (LOW BYTE) - During DMA the stop pointer is compared to RAP, for a peripheral to host transfer (ROP/$\overline{WOP}$ is set), or WAP, for a host to peripheral transfer (ROP/$\overline{WOP}$ is reset). Whenever the two pointers are equal, DMA is halted. DMA only resumes when the stop pointer is changed. SPL contains the lower byte of the 16 bit address.

SPH 5FH READ/WRITE

STOP ADDRESS POINTER (HIGH BYTE) - Upper 8 bits of the stop pointer.

EXTERNAL REGISTERS

HOSTL 50H Read/Write

Special decode - Microprocessor reads from this location will cause the $\overline{BIE}$ signal to be asserted if the $\overline{BIE}$ bit in INTCON is set. The $\overline{BIE}$ signal causes an external three-state driver to present host data to the buffer RAM. Microprocessor writes to this location will cause LO and $\overline{BOE}$ to be asserted in succession, if the $\overline{BOE}$ bit in INTCON is set. This allows buffer data to be latched and driven onto the host data bus.

HOSTH 51H Read/Write

Special decode - Same function as for external register HOSTL (50H). In systems with 16 bit hosts, external hardware may be used to distinguish between accesses to locations 50H and 51H, allowing separate access to the lower and upper bytes of the host bus.

BUFACC 70H Read/Write

BUFFER ACCESS - Microprocessor accesses to this location cause $\overline{MS}$ to be asserted. If the access is a write operation, $\overline{WE}$ will be asserted as well. This is intended to allow the microprocessor access to the currently addressed buffer RAM location, without altering the pointer value.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Ambient Temperature Under Bias	0 to 70	°C
Storage Temperature	-65 to 150	°C
Voltage on any Pin with respect to Ground	-0.5 to 7	V
Power Dissipation	0.475	W
Maximum Current Injection	±20	mA

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
VCC, Supply Voltage		4.75		5.25	V
TA, Operating Free Air Temperature		0		70	°C
Input Low Voltage		0		0.4	V
Input High Voltage		2.4		VCC	V

D.C. CHARACTERISTICS (TA = 0°C to 70° C, VCC = recommended range unless otherwise specified.)

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNIT
VIL	Input Low Voltage		-0.5		0.8	V
VIH	Input High Voltage		2.0		VCC+0.5	V
VOL	Output Low Voltage	IOL = 2 mA			0.4	V
VOH	Output High Voltage	IOH = 400 µA	2.4			V
ICC	Supply Current				85	mA
IL	Input Leakage	0V<VIN<VCC	-10		10	µA
IOL	Output Leakage	0.45V<VOUT<VCC	-10		10	µA
CIN	Input Capacitance				10	pF
COUT	Output Capacitance				10	pF

A. C. TIMING CHARACTERISTICS

TA = 0°C to 70°C, VCC = recommended range unless otherwise specified.
Load condition for all pins - 30 pF. Timing measurements are valid at 50% of rising or falling edge.
NOTE: ↓ indicates falling edge. ↑ indicates rising edge.

PERIPHERAL DEVICE TO BUFFER INTERFACE TIMING (see Figure 1)

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNIT
T/2	$\overline{CLK}$ half cycle		100			ns
Bs	$\overline{AREQ}$ ↓ to $\overline{CLK}$ ↓ setup time		30			ns
Bh	$\overline{CLK}$ ↓ to $\overline{AREQ}$ ↑ hold time		30			ns
Av	$\overline{CLK}$ ↓ to Address stable and $\overline{HOE}$ / $\overline{DOE}$ ↓				100	ns
Mv	$\overline{CLK}$ ↑ to $\overline{MS}$ ↓				40	ns
Mh	$\overline{CLK}$ ↓ to $\overline{MS}$ ↑		15		90	ns
Wv	$\overline{CLK}$ ↑ to $\overline{WE}$ ↓				40	ns
Wh	$\overline{CLK}$ ↓ to $\overline{WE}$ ↑				36	ns
Ah	$\overline{CLK}$ ↓ to Address stable and $\overline{HOE}$ / $\overline{DOE}$ ↑ hold time	Reading from RAM	15		90	ns
Dwe	$\overline{WE}$ ↑ to Address stable and $\overline{HOE}$ / $\overline{DOE}$ ↑ hold time	Writing to RAM	10		60	ns
Sv	$\overline{CLK}$ ↑ to SHP / SDP ↑				40	ns
Sh	$\overline{CLK}$ ↓ to SHP / SDP ↓				40	ns
Auh	Address, $\overline{HOE}$ / $\overline{DOE}$ stable to SHP/SDP ↑				40	ns

NOTE: In the multiplexed addressing mode, the higher order byte of the address and the control signals are provided for the external latch(es) when RAPH and WAPH are initialized by the microprocessor. When transferring data, the counter will overflow to indicate a need to update the external latch(es). The SSI 32C453 will then provide the correct address and control signals to update the external latches. When this occurs a Port B cycle is stolen to update the latch. The Port A and Port B cycles then occur normally.

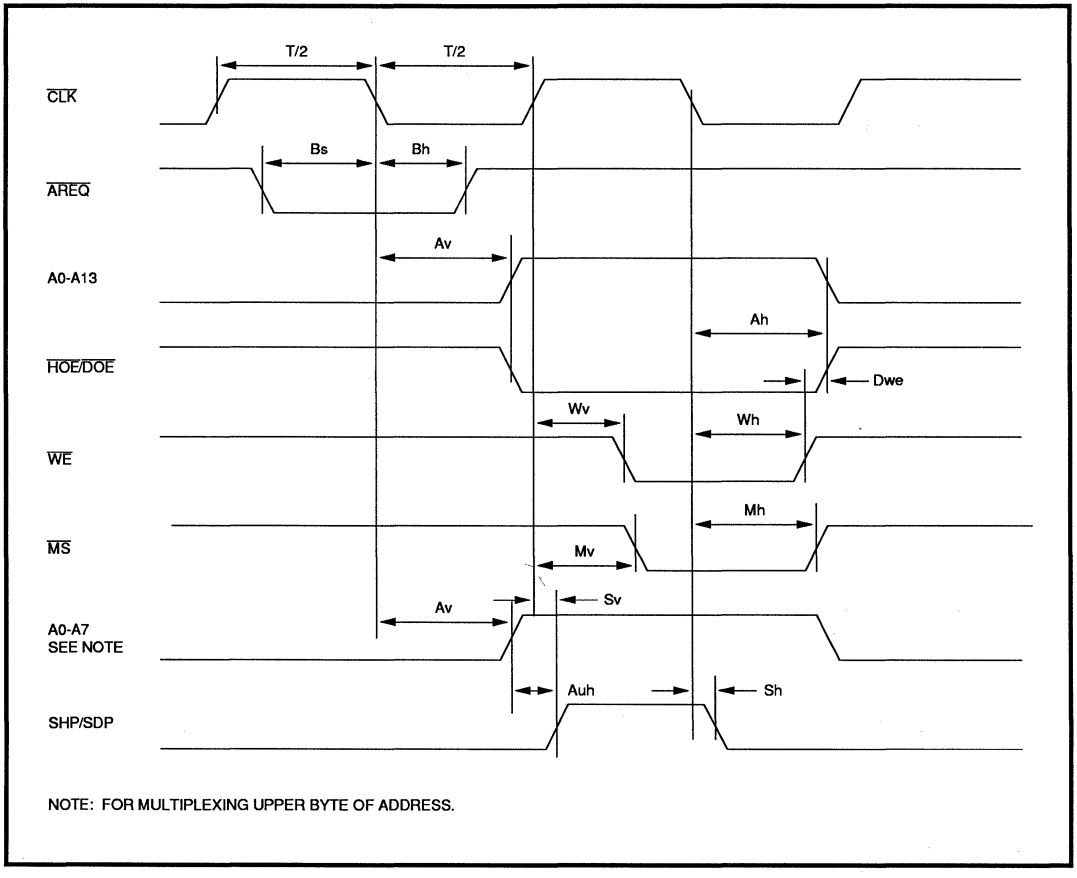


FIGURE 1: Peripheral Device to Buffer Interface Timing

BUFFER TO HOST INTERFACE TIMING (see Figure 2)

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNIT
Av	CLK ↓ to A0-A13 stable				100	ns
Dla	LO ↓ to A0-A13 hold		10		60	ns
Mv	CLK ↑ to MS ↓				40	ns
Dlm	LO ↓ to MS ↑		10		60	ns
Lv	CLK ↑ to LO ↑				40	ns
Lh	CLK ↓ to LO ↓				36	ns
Bv	CLK ↓ to BOE ↓				40	ns
Ba	CLK ↑ to BREQ ↑				40	ns
Br	BOE ↓ to BREQ ↑		70			ns
Ac	BACK ↑ to CLK ↑ set up		40			ns
Ar	BACK ↑ to BREQ ↓				40	ns
Acc	BACK ↓ to CLK ↓		10			ns

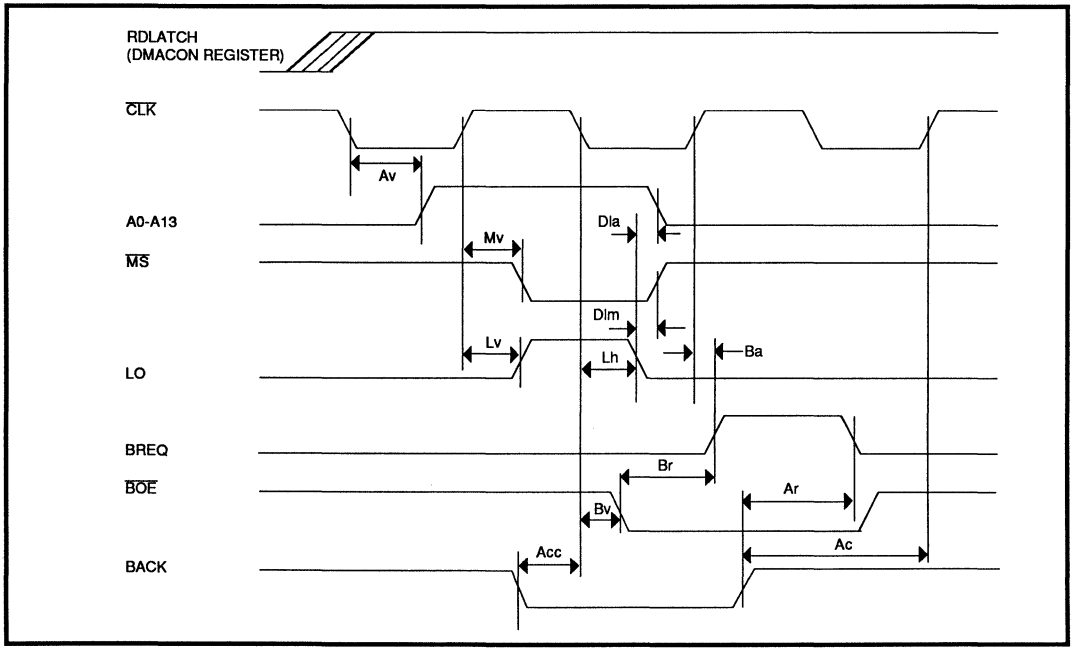


FIGURE 2: Buffer toHost Interface Timing

HOST TO BUFFER INTERFACE TIMING (see Figure 3)

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNIT
Bi	$\overline{CLK}$ ↑ to $\overline{BIE}$ ↓				40	ns
Dwg	$\overline{WE}$ ↑ to BREQ ↓		10		60	ns
Bs	BACK ↑ to $\overline{CLK}$ ↑		40			ns
Av	$\overline{CLK}$ ↓ to A0-A13 stable				100	ns
Dwa	$\overline{WE}$ ↑ to A0-A13 hold time		10		60	ns
Mv	$\overline{CLK}$ ↑ to $\overline{MS}$ ↓				40	ns
Mh	$\overline{CLK}$ ↓ to $\overline{MS}$ ↑				40	ns
Wv	$\overline{CLK}$ ↑ to $\overline{WE}$ ↓				40	ns
Wh	$\overline{CLK}$ ↓ to $\overline{WE}$ ↑				36	ns
Ab	BACK↓ to BREQ ↑				60	ns
Dwi	$\overline{WE}$ ↑ to $\overline{BIE}$ ↑		10		60	ns

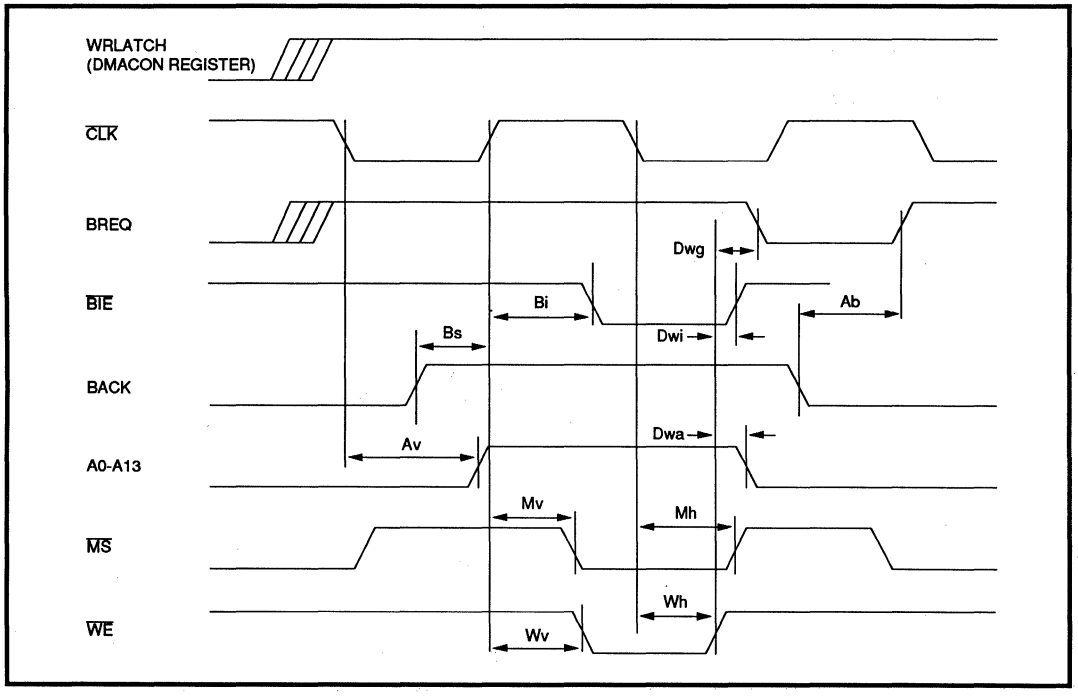


FIGURE 3: Host to Buffer Interface

MICROPROCESSOR INTERFACE TIMING (see Figure 4)

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNIT
Ta	ALE width		45			ns
Taw	ALE ↓ to $\overline{WR}$ ↓		25			ns
Tar	ALE ↓ to $\overline{RD}$ ↓		25			ns
Tw	$\overline{WR}$ width		200			ns
Tr	$\overline{RD}$ width		200			ns
As	AD0-AD7 set-up time		7.5			ns
Ah	AD0-AD7 hold time		20			ns
Cs	CS set-up time		7.5			ns
Ch	CS hold time		0			ns
Wds	Write data set-up time		70			ns
Wdh	Write data hold time		10			ns
Rts	$\overline{RD}$ ↓ to AD0-AD7 active		0			ns
Rda	$\overline{RD}$ ↓ to AD0-AD7 valid				145	ns
Rdh	AD0-AD7 hold from $\overline{RD}$ ↑				50	ns

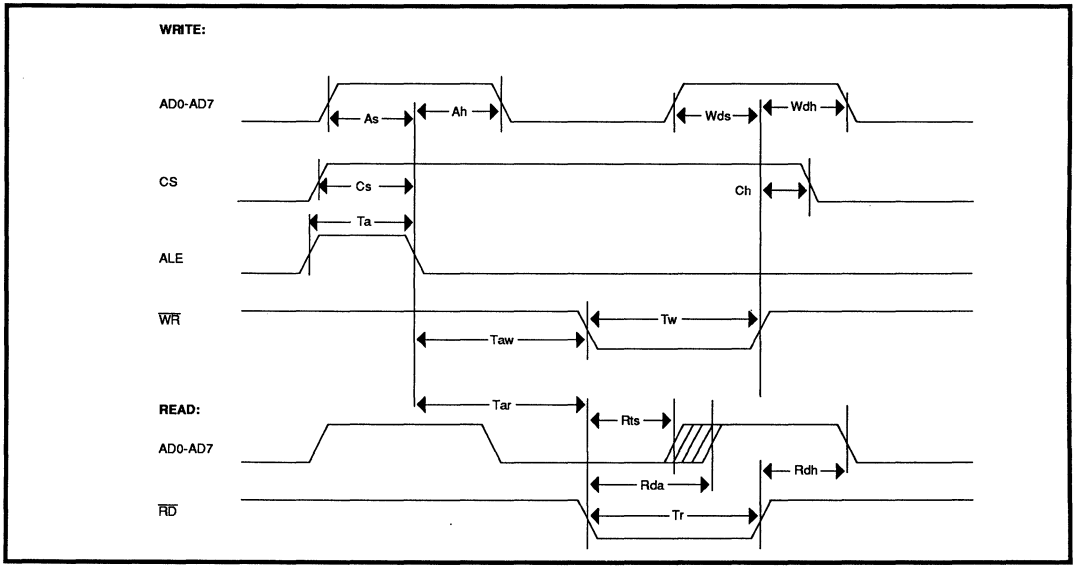


FIGURE 4: Microprocessor Interface

REGISTER 70 TIMING (see Figure 5)

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNIT
Mcl	$\overline{WR}\downarrow$ or $\overline{RD}\downarrow$ to $\overline{MS}\downarrow$		0		40	ns
Mch	$\overline{WR}\uparrow$ or $\overline{RD}\uparrow$ to $\overline{MS}\uparrow$		0		40	ns
Wwl	$\overline{WR}\downarrow$ to $\overline{WE}\downarrow$		0		40	ns
Wwh	$\overline{WR}\uparrow$ to $\overline{WE}\uparrow$		0		40	ns

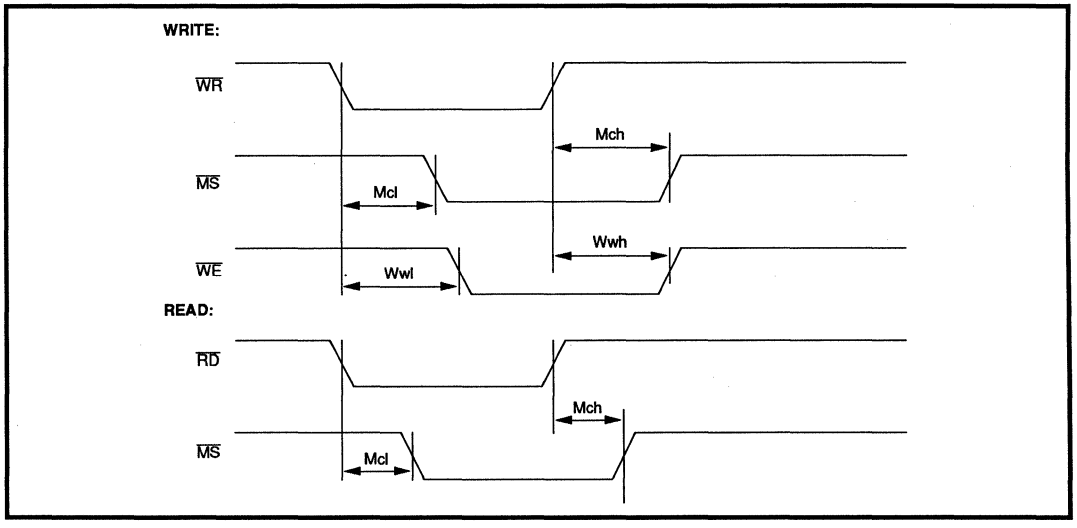


FIGURE 5: REGISTER 70 TIMING

SCSI ARBITRATION

The internal SSI 32C453 SCSI arbitration logic is shown in Figure 6. When the ARB bit in register IFCON is set, the SSI 32C453 is enabled to recognize SCSI "bus free" condition. When both the BSYIN and SELIN signals have been inactive for three $\overline{CLK}$ cycles this condition is held in a set/reset latch. After a further four $\overline{CLK}$ cycles, with BSYIN and SELIN remaining inactive ARB will be read as true. This indicates that a SCSI bus arbitration phase is underway. The ARB bit will be cleared if SELIN is active and the microprocessor asserts SELOUT, by setting the SELOUT bit in the IFCON register indicating that the arbitration was successful and the selection phase has begun. Figure 7 shows an overview of the SSI 32C453 SCSI interface timing for system considerations. An example of interfacing these signals to the SCSI bus is shown in Figure 12.

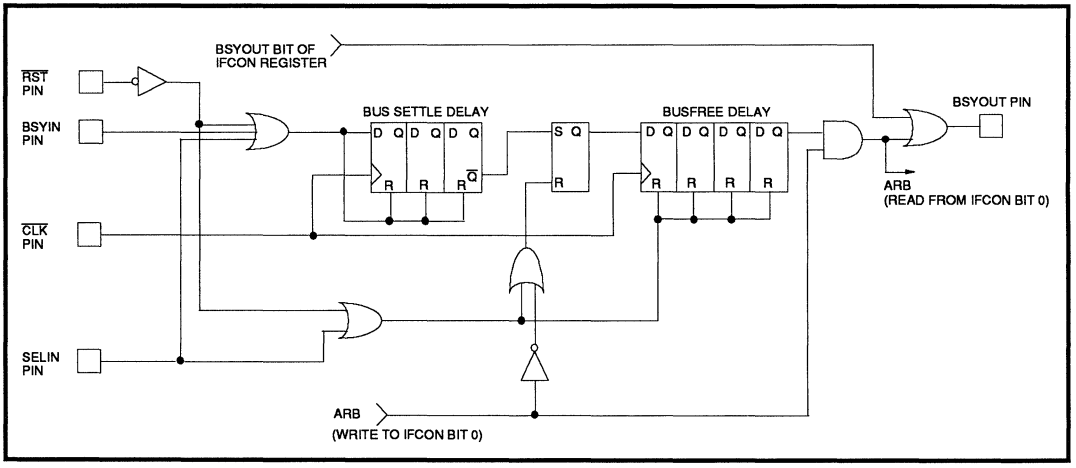


FIGURE 6: SSI 32C453 SCSI Arbitration Logic

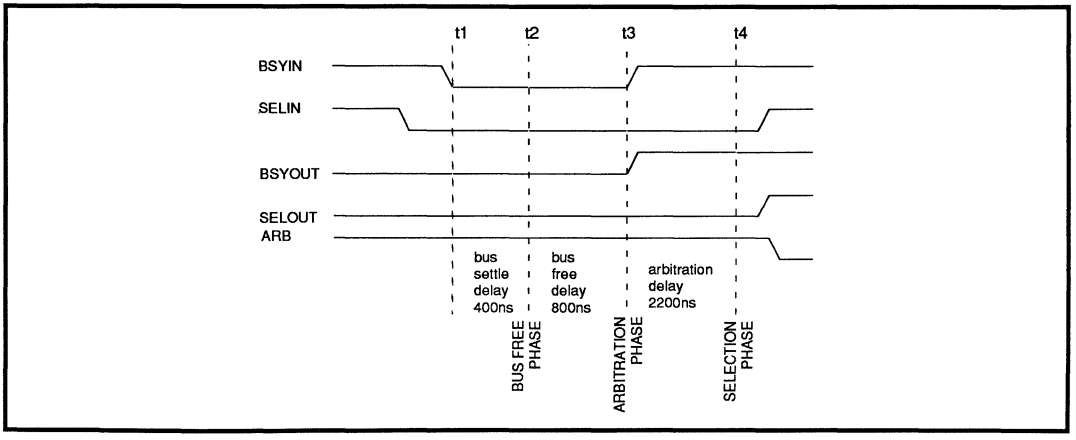


FIGURE 7: SSI 32C453 SCSI Arbitration Logic Timing

APPLICATIONS INFORMATION

EXTERNAL HARDWARE

As described previously, the SSI 32C453 provides a number of strobe outputs to control external interface hardware. Three different addressing configurations are illustrated in figures 8 to 11. Because of pin limitations, the DIP version of the SSI 32C453 does not provide either $\overline{HOE}$ or $\overline{DOE}$. These signals may be recreated with an external D flip-flop as shown in Figure 11. In extended addressing mode, the external Port A and Port B address latches must be initialized with explicit writes to the RAPH and WAPH registers, since only internal registers are initialized upon reset. To avoid interfering with data transfers, these registers should only be accessed when both ports are inactive.The ROP/$\overline{WOP}$ bit must be set correctly before these registers are written to in extended addressing mode, since this control bit can change which pointer is associated with which port. An example of interfacing the SSI 32C453 to the SCSI bus is shown in Figure 12.

A rule of thumb to use when selecting RAM for the buffer is:

$$\text{Buffer cycle time} = \frac{8\ \text{bits/byte}}{3 * \text{bit rate}}$$

SINGLE BLOCK READ

The following steps must be taken to effect the transfer of a single block of data from the peripheral to the host:

1. Initialize SSI 32C453 using RESET bit, and select desired buffer size and addressing mode.
2. Select read operation by setting ROP/$\overline{WOP}$.
3. Clear RAPH, WAPH explicitly when in extended addressing mode.
4. Instruct peripheral controller to commence peripheral read.
5. Wait for end of block. (Will be detected by controller or by observing value of WAP, which increments automatically).
6. Load stop pointer (SP) with the value (WAP-1), since WAP points to the location after the last entry in the FIFO buffer.
7. Set the RDLATCH bit so that the DMA request/ acknowledge cycles commence.
8. Wait for DMADONE to be set. (Occurs when RAP=SP).

SINGLE BLOCK WRITE

The following steps must be taken to effect the transfer of a single block of data from the host to the peripheral:

1. Initialize SSI 32C453 using RESET bit, and select desired buffer size and addressing mode. (This will clear ROP/$\overline{WOP}$.)
2. Clear RAPH, WAPH explicitly when in extended addressing mode.
3. Set SP to be equal to the length of the data block to be transferred.
4. Set the WRLATCH bit so that the DMA request/acknowledge cycles commence.
5. Wait for DMADONE to be set. (Occurs when WAP=SP).
6. Instruct peripheral controller to commence peripheral read.
7. Wait for end of block. (Will be detected by controller or by observing value of RAP, which increments automatically).

MUTLIPLE BLOCK READ

The initial steps in a multiple block read are similar to those of a single block read. However, once the DMA transfer of the first block to the host is underway, the next peripheral block read can occur, provided that the buffer is sufficiently large to accomodate the next block of data. (The microprocessor can either check the value of RAP, or maintain its own count of the number of blocks currently stored in the buffer, in order to prevent buffer overruns caused by the peripheral.) When the next peripheral block transfer has been initiated, the microprocessor waits for DMADONE to be set. When the host is ready for a new DMA transfer, the value of SP may be changed and a new transfer started (provided there is sufficient data in the buffer to prevent an overrun).

MULTIPLE BLOCK WRITE

As in the case of multiple block reads, the microprocessor starts by causing a single block of host data to be transferred to the buffer memory. Thereafter, host and peripheral transfers may be initiated simultaneously, provided the microprocessor ensures that a buffer overrun does not occur.

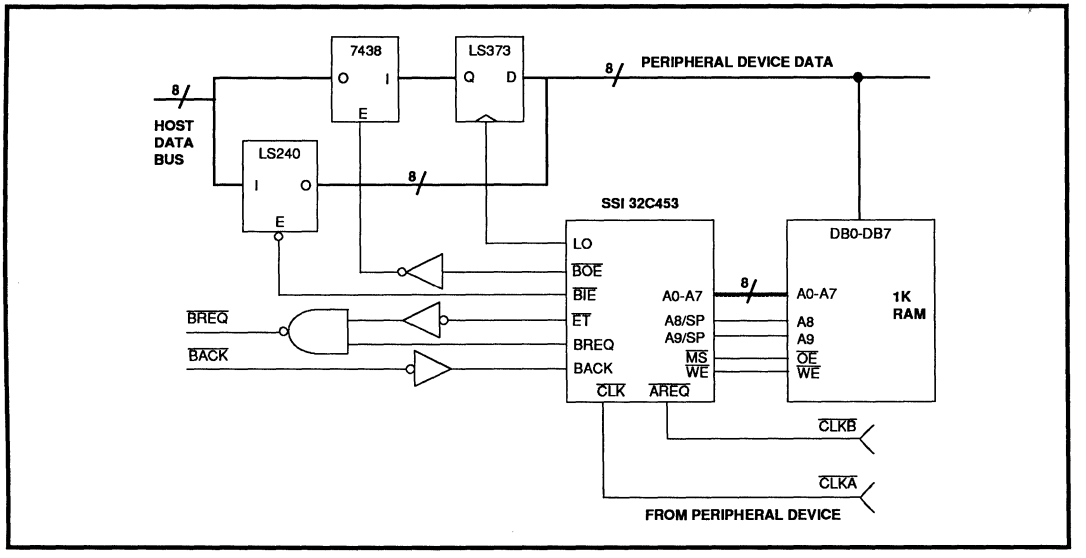


FIGURE 8: Direct Address Mode Example - 10 Address Lines

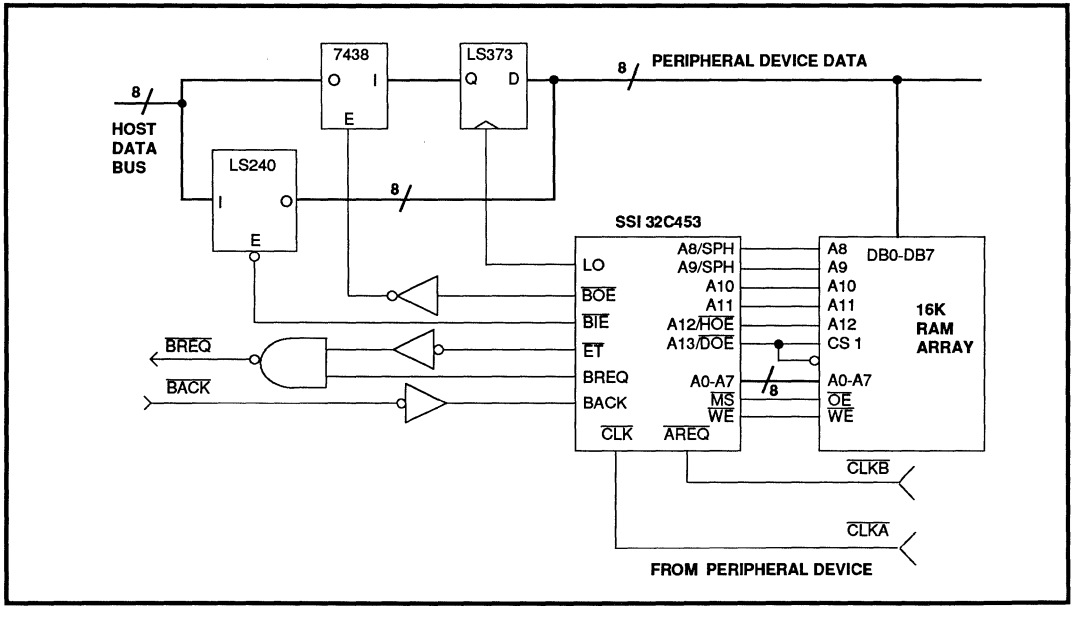


FIGURE 9: Direct Addressing Mode Example - 14 Address Lines (SSI 32C453 PLCC Version Only)

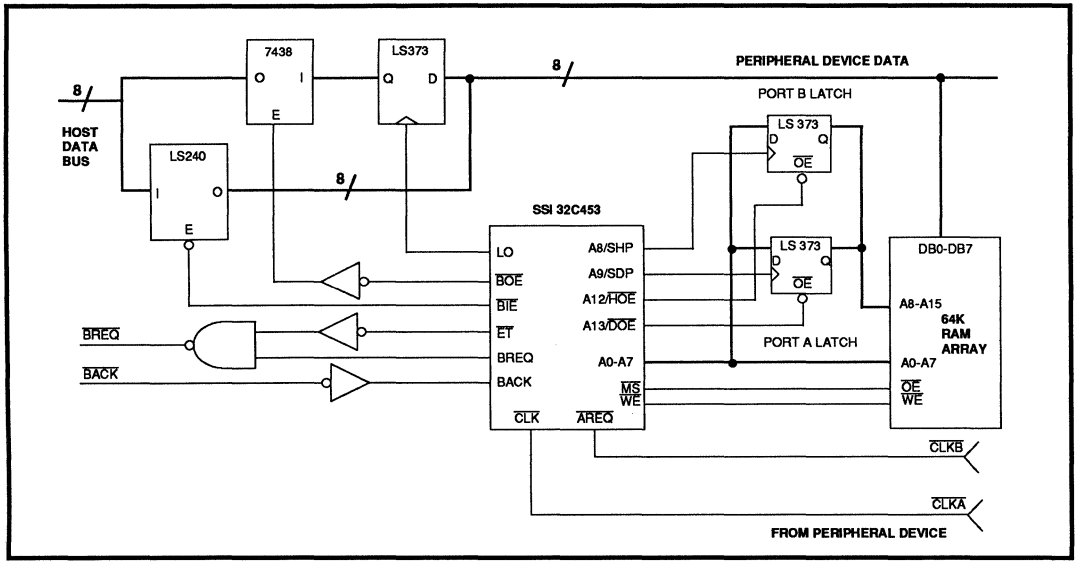


FIGURE 10: Extended Addressing Mode Example

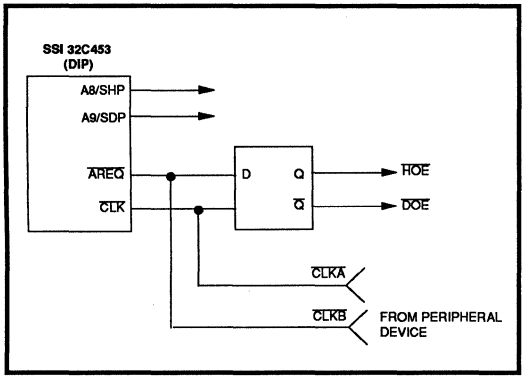


FIGURE 11: Extended Mode Address Strobes for DIP Package

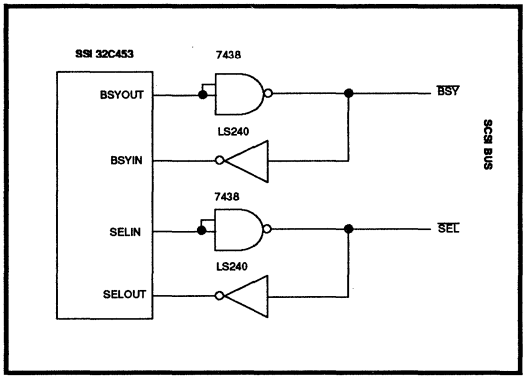


FIGURE 12: SCSI Bus Interface Example

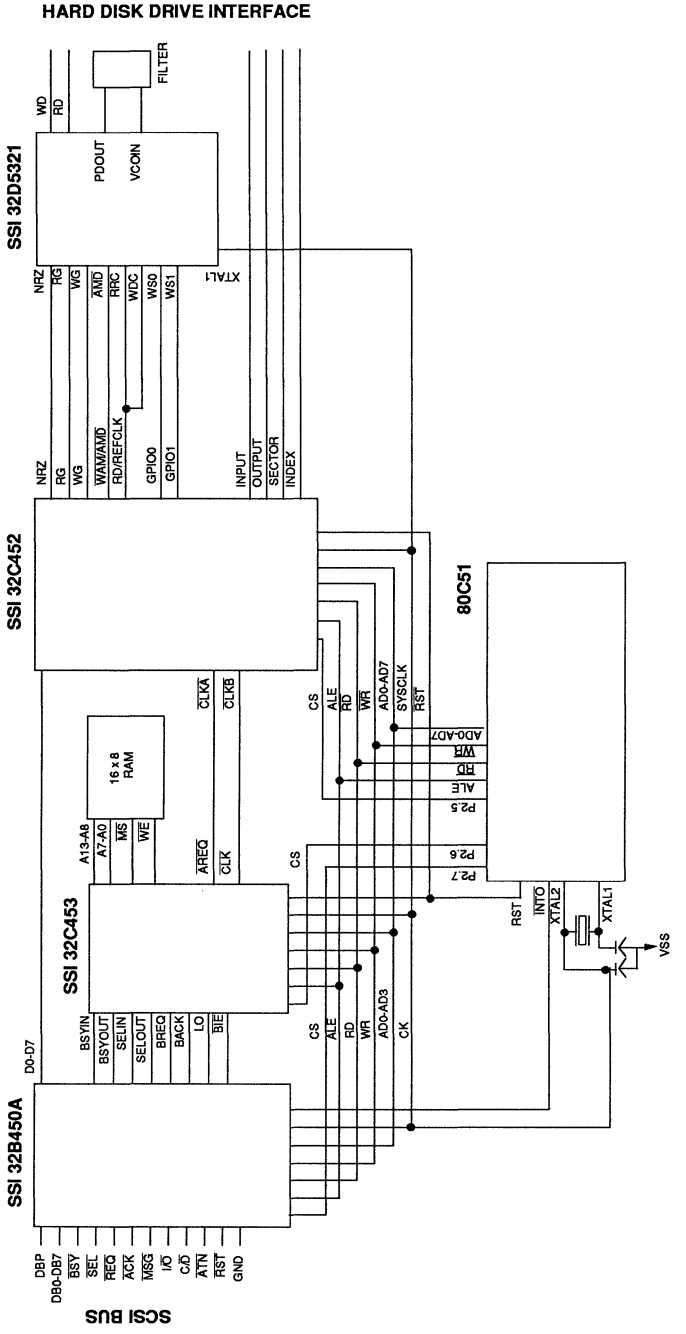
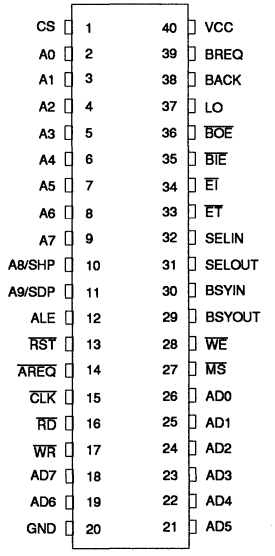


FIGURE 13: SCSI Peripheral Controller Chip Set

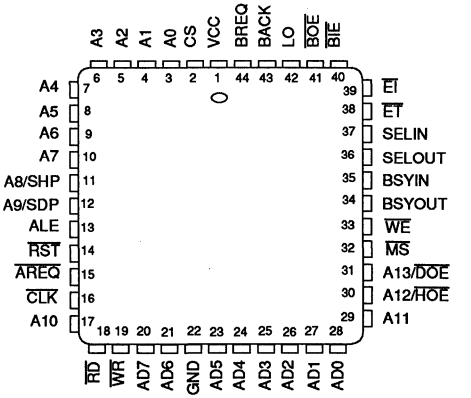
SSI 32C453
Dual Port
Buffer Controller

PACKAGE PIN DESIGNATIONS

(Top View)



40-Pin DIP



44-Lead PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32C453 Dual Port Buffer Controller		
40 Pin DIP	SSI 32C453-CP	SSI 32C453-CP
44-Pin PLCC	SSI 32C453-CH	SSI 32C453-CH

silicon systems™

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 CA 92680, (714) 731-7110, TWX 910-595-2809

SSI 32B545
Winchester Disk Drive Support Logic

August, 1988

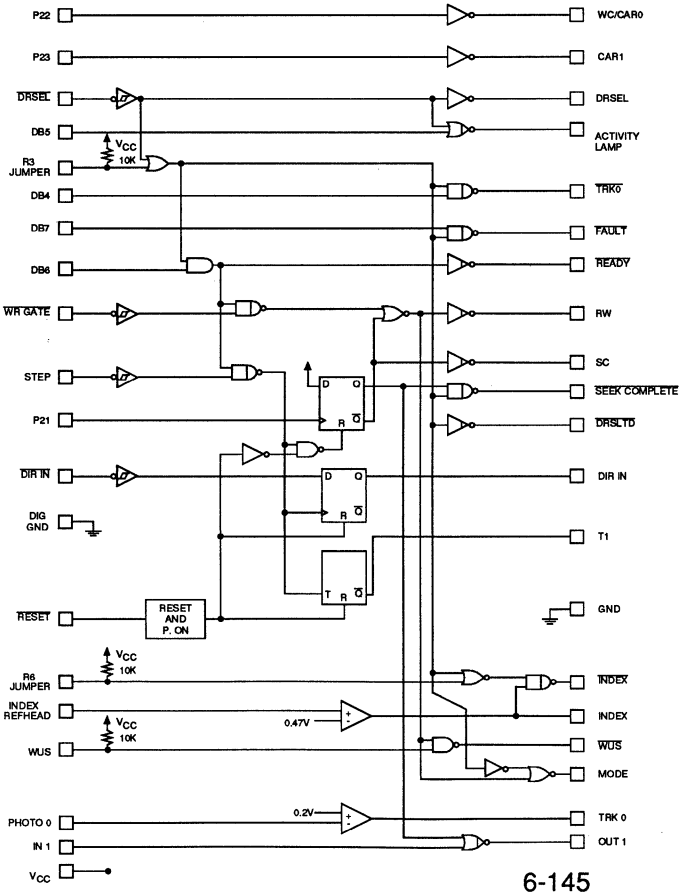
DESCRIPTION

The SSI 32B545 is an integrated circuit which consolidates functions in a Winchester Disk Drive normally performed by a variety of LSTTL SSI and MSI devices. Various gates, comparators and flip-flops are used to format signals compatible with the ST 506 interface requirements. All ST 506 connections have the necessary output drive or input hysteresis consistent with bus signal needs. The SSI 32B545 uses a single +5 volt supply and is available in 40 pin DIP and 44 pin PLCC packages.

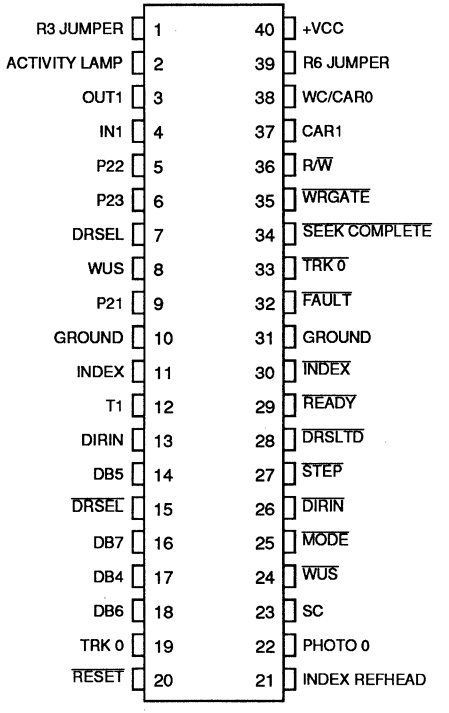
FEATURES

- **Reduces package count in 51/4" and smaller Winchester Disk Drives**
- **Replaces bus interface and combinatorial logic devices between the ST 506 bus and on board processor and mechanical interfaces**
- **Surface mount package available for further real estate reduction**

LOGIC DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

PIN DESCRIPTIONS

PIN NUMBER		I/O TYPE	PIN NAME	PIN NUMBER		I/O TYPE	PIN NAME
40 PIN DIP	44 PIN PLCC			40 PIN DIP	44 PIN PLCCΔ		
1	1	I3	R3 JUMPER	21	23	*	INDEX REF HEAD
2	2	O3	ACTIVITY LAMP	22	24	*	PHOTO0
3	3	O1	OUT1	23	25	O2	SC
4	4	I1	IN1	24	26	O2	$\overline{\text{WUS}}$
5	5	I1	P22	25	27		MODE
6	7	I1	P23	26	29	I2	$\overline{\text{DIRIN}}$
7	8	O2	DRSEL	27	30	I2	$\overline{\text{STEP}}$
8	9	I3	WUS	28	31	O4	$\overline{\text{DR SLTD}}$
9	10	I1	P21	29	32	O4	$\overline{\text{READY}}$
10	11		GROUND	30	33	O4	$\overline{\text{INDEX}}$
11	12	O2	INDEX	31	34		GROUND
12	13	O2	T1	32	35	O4	$\overline{\text{FAULT}}$
13	14	O2	DIRIN	33	36	O4	$\overline{\text{TRK 0}}$
14	15	I1	DB5	34	37	O4	$\overline{\text{SEEK COMPLETE}}$
15	16	I2	$\overline{\text{DRSEL}}$	35	38	I2	$\overline{\text{WRGATE}}$
16	18	I1	DB7	36	40	O1	R/$\overline{\text{W}}$
17	19	I1	DB4	37	41	O1	CAR1
18	20	I1	DB6	38	42	O1	WC/CAR0
19	21	O2	TRK 0	39	43	I3	R6 JUMPER
20	22	I1	$\overline{\text{RESET}}$	40	44		+VCC

Δ Pins 6,17, 28, and 39 are not connected in the 44 Pin QUAD package
*COMPARATOR

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified: 4.5 < Vcc < 5.5; 0 °C < Ta < 70 °C.)

ABSOLUTE MAXIMUM RATINGS

(Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	RATING	UNIT
VCC supply voltage	7	volts
Storage temperature	-65 to + 150	°C
Ambient operating temperature	0 to + 70	°C
Logic input voltage	-0.5 to 7.0	VDC
Lead temperature (soldering 10 sec)	260	°C

LOGIC OUTPUTS (Refer to Pin Descriptions for output type, pin number cross reference.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TYPE O1 (OPEN COLLECTOR) OUTPUTS					
Output High Current	VOH =5.5V			250	µA
Output Low Voltage	IOL = 16 mA			0.5	V
TYPE O2 (TOTEM POLE) OUTPUTS					
Output High Voltage	IOH = -400 µA	2.5			V
Output Low Voltage	IOL = 8 mA			0.5	V
Short Circuit Current				-100	mA
TYPE O3 (OPEN COLLECTOR) OUTPUTS					
Output High Current	VOH = VCC			50	µA
Output Low Voltage	IOL = 30 mA			0.8	V
TYPE O4 (OPEN COLLECTOR) OUTPUTS					
Output High Current	VOH = 5.5V			250	µA
Output Low Voltage	IOL = 48 mA			0.5	V

LOGIC INPUTS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TYPE I1 INPUTS					
Input High Voltage		2.0			V
Input Low Voltage				0.8	V
Input Low Current	VIL = 0.5V			-0.8	mA
Input High Current	VIH = 2.4V			400	µA

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TYPE I2 (SCHMIDT TRIGGER) INPUTS					
Threshold Voltage	Positive going, VCC = 5V	1.3		2.0	V
	Negative going, VCC = 5V	0.6		1.1	V
Hysteresis	VCC = 5V	0.4			V
Input High Current	VIH = 2.4V			40	µA
Input Low Current	VIL = 0.5V			-0.8	mA
TYPE I3 (INTERNAL PULLUP) INPUTS					
Input High Voltage		2.0			V
Input Low Voltage				0.8	V
Input Low Current	VIL = 0.5V			-1.2	V

COMPARATOR INPUTS

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
Threshold Voltage	Index Ref	Positive going			580	mV
		Negative going	370			mV
	Photo 0	Positive going			280	mV
		Negative going	120			mV
Hysteresis				30		mV
Input Resistance	VCC = 5.0V, 0<Vin<VCC		10			KΩ

TIMING CHARACTERISTICS (Ta = 25°C, CL = 25 pF)

Propagation Delay Time, Input to Output	P22 to WC/CAR0			40	ns
	P23 to CAR0			40	ns
	DB5 to ACTIVITY LAMP			40	ns
	DB4 to $\overline{\text{TRCK0}}$			40	ns
	DB7 to $\overline{\text{FAULT}}$			40	ns
	$\overline{\text{DRSEL}}$ to DRSEL			55	ns
	$\overline{\text{DRSEL}}$ to ACTIVITY LAMP			55	ns
	WUS to $\overline{\text{WUS}}$			55	ns
	DB6 to $\overline{\text{READY}}$			55	ns
	$\overline{\text{WRGATE}}$ to R/$\overline{\text{W}}$			60	ns
	$\overline{\text{STEP}}$ to SC, DIR IN, to T1			100	ns

TIMING CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Propagation Delay Time, Input to Output	P21 to SC			100	ns
	P21 to R/$\overline{W}$			120	ns
Data Setup Time	$\overline{DIRIN}$ reference to STEP			50	ns
Data Hold Time	$\overline{DIRIN}$ to STEP			5	ns
Delay Time	INDEX REF HEAD to INDEX, with 500 mV input step			250	ns
	PHOTO 0 to TRK0 with 500 mV input step			250	ns

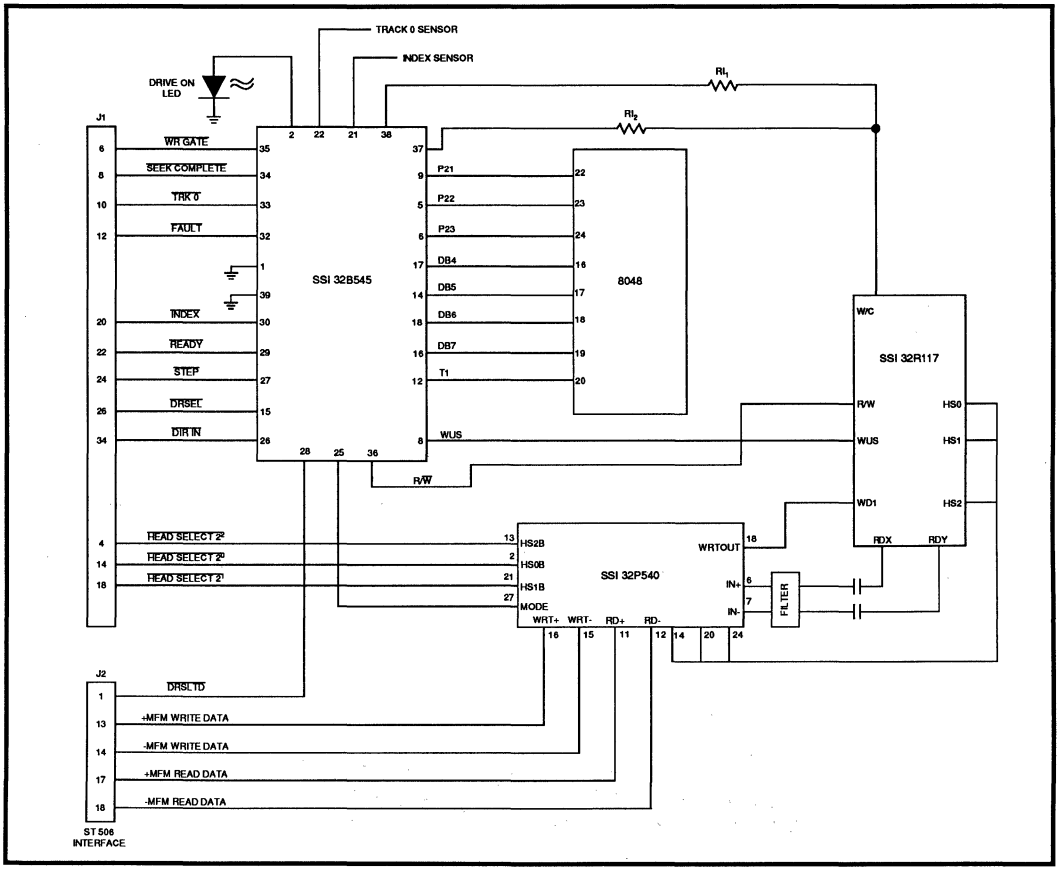
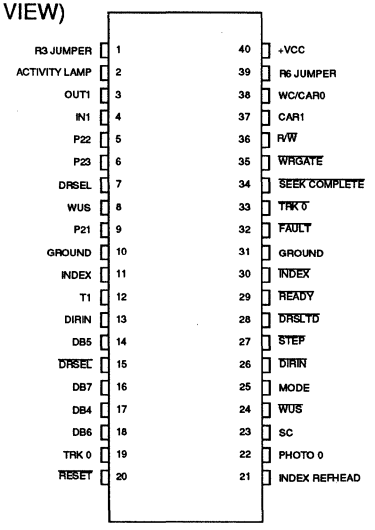


FIGURE 1: TYPICAL APPLICATION

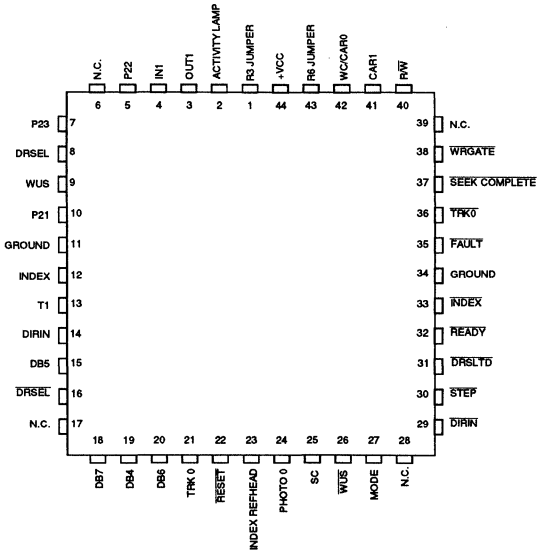
SSI 32B545
Winchester Disk Drive Support Logic

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



40-Pin DIP



44-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32B545-CH 44-Pin PLCC	SSI 32B545-CH	32B545-CH
SSI 32B545 40-Pin DIP	SSI 32B545-CP	32B545-CP

silicon systems™
14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

0888

Section 7

FLOPPY DISK DRIVE CIRCUITS

SSI 34D441

Data Synchronizer & Write Precompensator Device

August, 1988

DESCRIPTION

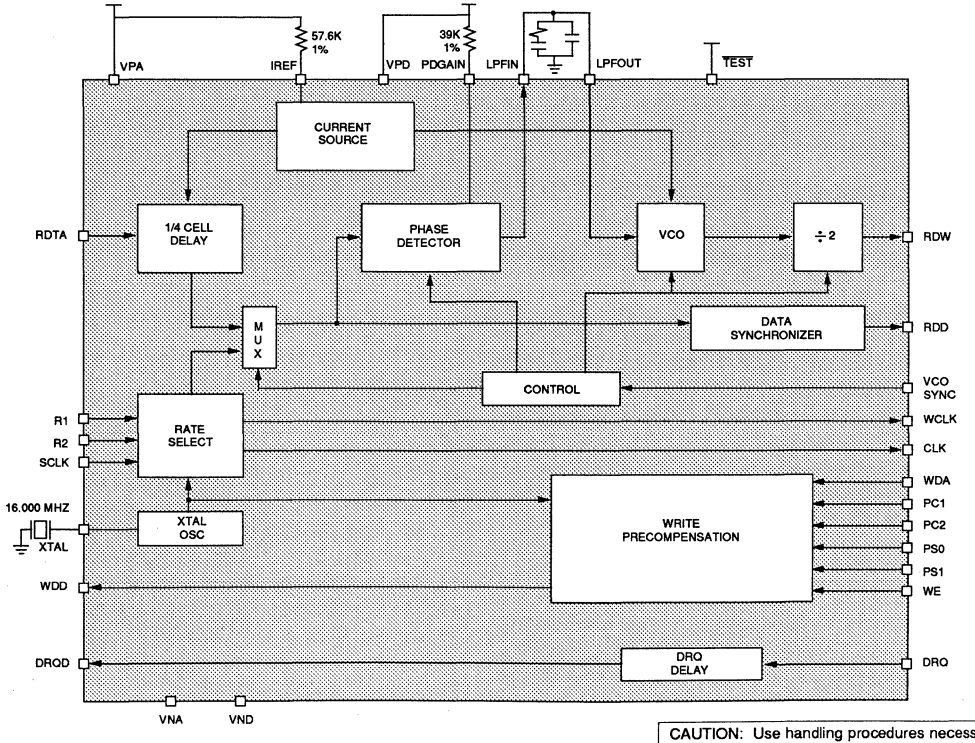
The SSI 34D441 floppy disk data synchronizer/write precompensator performs read-data synchronization and write data precompensation of MFM encoded data for high performance floppy disk drive systems. The SSI 34D441 is optimized for use with the NEC μPD765A/μPD7265 controller family.

The SSI 34D441 contains an analog phase-lock-loop for read data synchronization, a crystal controlled reference oscillator, write precompensation circuitry, and a delay function for the DRQ signal. It employs silicon gate CMOS technology for low power consumption. The SSI 34D441 requires a +5V power supply and is available in 28-pin PDIP and 28-pin PLCC packages.

FEATURES

- **Ideal for operation with NEC μPD765A/μPD7265**
- **Fast acquisition analog PLL for precise read data synchronization**
- **No adjustments or trims needed to external components**
- **Programmable data rate, up to 1 Mbits/s**
- **Internal crystal controlled oscillator**
- **Selectable write precompensation intervals**
- **Programmable write clock**
- **DRQ (Data DMA Request) delay function**
- **Low power CMOS, +5V operation**
- **28-pin PDIP and 28-pin PLCC**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 34D441
Data Synchronizer & Write Precompensator Device

FUNCTIONAL DESCRIPTION

CRYSTAL OSCILLATOR

The crystal controlled oscillator uses a 16.000 MHz crystal cut for fundamental series mode resonance. Its frequency is divided down and used throughout the 34D441. The device requires only one pin for the crystal input; the other crystal pin is connected to digital ground. An external source (TTL level) can also be used to drive the chip via this pin, if desired.

RATE-SELECT

The rate-select section generates the various write-data frequencies (WCLK), and one of the two alternative clock rates (CLK), as shown in Table 1. In addition, this section provides a time base for the read-data circuitry. The CLK and WCLK signals have their rising edges synchronized. The WCLK signal has a pulse width of 250 ns.

TABLE 1: WRITE-DATA CLOCK FREQUENCIES

R2	R1	WCLK	DATA RATE	SCLK	CLK
1	0	250 KHz	125 KHz	1	8 MHz
0	0	500 KHz	250 KHz	0	4 MHz
0	1	1 MHz	500 KHz		
1	1	2 MHz	1 MHz		

DRQ DELAY

This circuit is used to delay the leading edge of the DRQ signal, which is generated by the NEC 765 before it is sent to the DMA controller. The output pulse appearing at DRQD has its leading edge delayed by six to eight CLK pulses. The DRQ pulse is at least nine CLK pulses wide. The falling edge of the input clears the DRQD pulse.

DATA SEPARATOR

This circuit consists of several blocks, which include the one-shot, VCO, IREF, and the read-path circuitry. Read-data synchronization is accomplished with a fast acquisition phase-lock-loop (PLL). The input data from the disk drive, RDTA, is phase locked with the VCO. The synchronized read data and the VCO (divided by two) are available for external data extraction at the RDD and RDW pins, respectively.

Changing the state of VCOSYNC causes the VCO to be stopped and restarted in phase with the PLL reference, which can be either the internal crystal oscillator or the RDTA input data. Restarting the VCO in phase with the input prevents the PLL from locking to harmonics and insures short lock times. (See Figure 1.)

The one-shot is used to shape the input read data. The IREF block provides reference currents to both the VCO and the One-Shot circuits. Current for the current source block is set by an external resistor connected to the IREF pin. The rate pins R1 and R2 are used to select between various frequencies. The Read-Path circuitry includes the phase detector, charge pump, data synchronizer and control logic circuitry.

The data synchronizer separates the data and clock pulses using windows derived from the VCO output. Using a VCO running at twice the expected input data frequency allows accurate centering of these windows about the expected bit positions. The phase detector controls the charge pump which causes current pulses to flow in or out of the phase-lock-loop filter. The amount of current to be sourced or sunk by the charge pump is controlled by an external resistor connected to the PDGAIN pin. This feature can be used to change the phase detector gain, KPD, which is given by:

$I_{PDGAIN}/2\pi$ [A/rad]

The output read data pulse, RDD, is at least 62.5 nsec wide.

WRITE PATH

The WDD output is a re-synchronized version of the input MFM write data (WDA) which has been time shifted, if needed, to reduce interbit interference. The amount of precompensation, as well as the direction of the pulse shifting, is controlled by the external signals PC1, PC2, PS0 and PS1. Table 2 describes the precompensation signals. The output buffer for the precompensated write data (WDD) is capable of sinking 24 mA. The write path circuitry is also used to multiplex the output of the one-shot to the WDD pin for test purposes.

TABLE 2: PRECOMPENSATION DESCRIPTION

PC2	PC1	PRECOMPENSATION INTERNAL	PS0	PS1	SHIFT
0	0	±62.5 ns	0	1	Normal (no shift)
1	0	±125 ns	0	1	Late (delay)
0	1	±187.5 ns	1	0	Early (advance)
1	1	±250 ns	1	1	Invalid (no Shift)

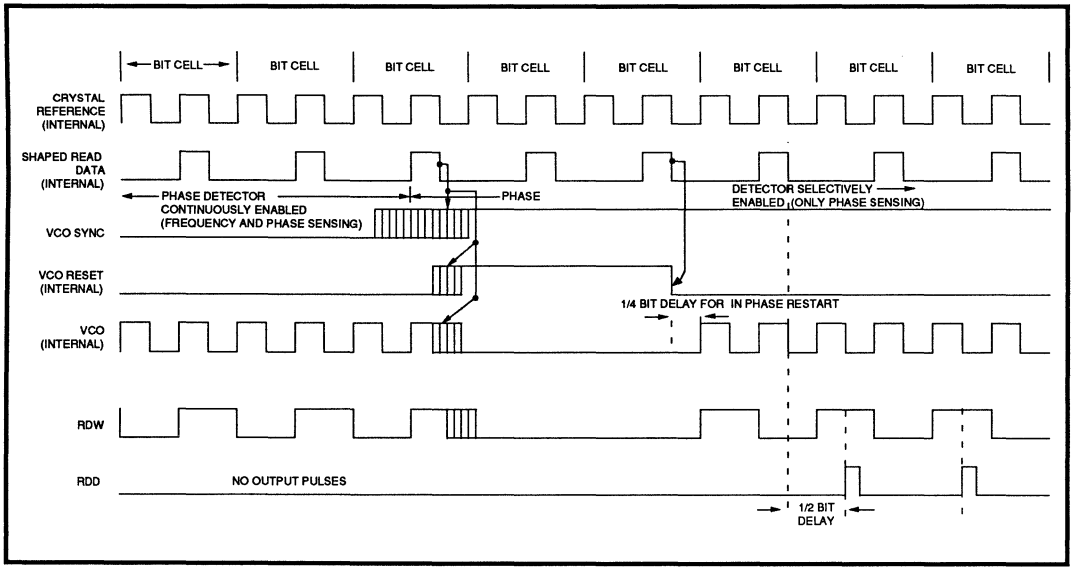


FIGURE 1: PLL Locking Sequence

PIN DESCRIPTIONS

<table>
<tr><th>NAME</th><th>PIN NO.</th><th>DESCRIPTION</th></tr>
<tr><td>R1, R2</td><td>3, 4</td><td>Used to set the following conditions: write data clock rate (WCLK), one-shot output pulse width, and the (VCO) voltage - controlled oscillator frequency.
<table>
<tr><th>R2</th><th>R1</th><th>DATA RATE</th><th>NOMINAL WCLK</th><th>VCO FREQ</th></tr>
<tr><td>1</td><td>0</td><td>125 KHz</td><td>250 KHz</td><td>250 KHz</td></tr>
<tr><td>0</td><td>0</td><td>250 KHz</td><td>500 KHz</td><td>500 KHz</td></tr>
<tr><td>0</td><td>1</td><td>500 KHz</td><td>1 MHz</td><td>1 MHz</td></tr>
<tr><td>1</td><td>1</td><td>1 MHz</td><td>2 MHz</td><td>2 MHz</td></tr>
</table></td></tr>
<tr><td>SCLK</td><td>5</td><td>This pin sets the clock frequency CLK
<table>
<tr><th>SCLK</th><th>CLK</th></tr>
<tr><td>0</td><td>4 MHz</td></tr>
<tr><td>1</td><td>8 MHz</td></tr>
</table></td></tr>
<tr><td>PC2, PC1</td><td>6, 7</td><td>Used to set the amount of write-data precompensation.
<table>
<tr><th>PC1</th><th>PC2</th><th>PRECOMPENSATION INTERVAL (ns)</th></tr>
<tr><td>0</td><td>0</td><td>±62.5</td></tr>
<tr><td>0</td><td>1</td><td>±125</td></tr>
<tr><td>1</td><td>0</td><td>±187.5</td></tr>
<tr><td>1</td><td>1</td><td>±250</td></tr>
</table></td></tr>
<tr><td>DRQ</td><td>8</td><td>Accepts DRQ signal from NEC 765 controller to delay it.</td></tr>
<tr><td>$\overline{\text{TEST}}$</td><td>10</td><td>Should be a logic high for normal operation. When $\overline{\text{TEST}}$ is low, the WDD pin outputs the one-shot pulse.</td></tr>
<tr><td>RDTA</td><td>11</td><td>Accepts the MFM encoded read data pulses from the read amplifier circuits.</td></tr>
<tr><td>VCOSYNC</td><td>18</td><td>Selects the reference input to the PLL. Selects a reference frequency equal to WCLK when low, and the incoming read data (RDTA), when high.</td></tr>
<tr><td>WDA</td><td>25</td><td>Accepts write data from the controller. This data is resynchronized and precompensated before being sent to the drive.</td></tr>
</table>

PIN DESCRIPTIONS (Continued)

<table>
<tr><th>NAME</th><th>PIN NO.</th><th>DESCRIPTION</th></tr>
<tr><td>PS0, PS1</td><td>26, 27</td><td>Pins to determine whether to precompensate write data pulses, and to advance or delay the leading edge of pulses.
<table>
<tr><th>PS0</th><th>PS1</th><th>SHIFT</th></tr>
<tr><td>0</td><td>1</td><td>Normal (no shift)</td></tr>
<tr><td>0</td><td>1</td><td>Late (delay)</td></tr>
<tr><td>1</td><td>0</td><td>Early (advance)</td></tr>
<tr><td>1</td><td>1</td><td>Invalid (no shift)</td></tr>
</table></td></tr>
<tr><td>WE</td><td>28</td><td>When high, causes data to be output at the WDD pin. When WE is low, write data (WDD) is low.</td></tr>
<tr><td>VPD</td><td>2</td><td>+5V Digital supply</td></tr>
<tr><td>VND</td><td>24</td><td>Digital ground for chip</td></tr>
<tr><td>VPA</td><td>12</td><td>+5V analog supply (isolated +5V source having very little noise).</td></tr>
<tr><td>VNA</td><td>13</td><td>Analog ground</td></tr>
<tr><td>DRQD</td><td>9</td><td>Output for the delayed DRQ signal from the NEC 765. Only the leading edge of the input signal is delayed.</td></tr>
<tr><td>RDW</td><td>19</td><td>This is a square wave output generated by the VCO which provides a read data window to be used by the NEC 765 controller to separate the read-data and read-clock transitions. RDW has the same frequency as the nominal data rate.</td></tr>
<tr><td>RDD</td><td>20</td><td>This signal consists of pulses that indicate flux reversals present on the floppy disk that could indicate either clock or data information. The leading edge of each RDD pulse will appear in the center of window defined by the RDW signal.</td></tr>
<tr><td>WCLK</td><td>21</td><td>This signal is the write clock for the controller device. All write signals output by the NEC 765 controller, are related to WCLK.</td></tr>
<tr><td>CLK</td><td>22</td><td>This signal is used by the NEC 765 controller and associated devices. The CLK signal has a 50% duty cycle and the rate is set by SCLK.</td></tr>
<tr><td>WDD</td><td>23</td><td>This open-drain output provides re-synchronized and precompensated write data in accordance with settings on PC1,PC2, and PS0, PS1 pins. The leading edge of WDD shall be used to define data. When $\overline{\text{TEST}}$ is low, this pin will output the one-shot pulses.</td></tr>
<tr><td>XTAL</td><td>1</td><td>Single input pin for the 16 MHz crystal oscillator. Other side of crystal to go to digital ground. Option of providing an external 16MHz signal with TTL compatible logic levels and a 40% to 60% duty cycle.</td></tr>
<tr><td>IREF</td><td>14</td><td>Used to set the internal reference current generated for the one-shot and VCO. Desired current shall be derived from a 1% tolerance 57.6 KΩ resistor connected between the analog 5 volt supply and this pin.</td></tr>
</table>

PIN DESCRIPTIONS (Continued)

<table>
<tr><th>NAME</th><th>PIN NO.</th><th>DESCRIPTION</th></tr>
<tr><td>LPFOUT</td><td>15</td><td>Control voltage input of the VCO, and also for the connection of loop-filter output. Control voltage shall range approximately from 0.7 to 4.5 volts.</td></tr>
<tr><td>LPFIN</td><td>16</td><td>Output pin for the current pulses from charge pump that the were converted from voltage pulses generated by phase detector. This pin is typically connected to LPFOUT, and an RC low pass loop filter network connected to the analog ground.</td></tr>
<tr><td>PDGAIN</td><td>17</td><td>Used to set the current level to be sunk or sourced by the charge-pump. A 39K ohm resistor connected between this pin and the digital 5 volt supply VPD, shall provide a 100 µA current to the charge-pump. Some other resistor values and their corresponding currents are given below:
<table>
<tr><th>RPDGAIN</th><th>IPDGAIN</th></tr>
<tr><td>15K</td><td>225 µA</td></tr>
<tr><td>22K</td><td>160 µA</td></tr>
<tr><td>30K</td><td>120 µA</td></tr>
<tr><td>46K</td><td>80 µA</td></tr>
</table></td></tr>
</table>

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Storage Temperature	-40 to +120	°C
Ambient Operating Temperature, TA	0 to +70	°C
Supply Voltages, VPD, VPA	-0.5 to +7.0	VDC
Voltage Applied to Logic inputs	-0.5 to +7.0	VDC
Voltage Supplied to Logic Outputs	-0.5 to +5.5	VDC
Maximum Power Dissipation	750	mW

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Ambient Temperature, TA		0		70	°C
Power Supply Voltage, VPD, VPA		4.75	5	5.25	VDC
High Level Input Voltage, VIH	Power supply = 4.75V	2.0			V
Input Current High, IIH	Power supply =4.75V VIH = 2.4V			20	µA
Low Level Input Voltage, VIL	Power supply = 4.75V			0.8	V
Input Current Low, IIH	Power supply = 5.25V VIL = 0.4V			-20	µA
High Level Output Voltage, VOH	Power supply = 4.75V IOH=4 mA	2.4			V
Low Level Output Voltage All others, VOL	Power supply = 4.75V IOL = 8 mA			0.4	V
Short Circuit Output Current WDD only IOS (to positive supply)	Power supply = 5.25V	20		150	mA

DC CHARACTERISTICS (Unless otherwise specified, power supplies = 4.75V to 5.25V, TA = 0 to 70°C, R_{IREF} = 57.6 KΩ ± 1%, R_{PDGAIN} = 39 KΩ ± 5%, XTAL = 16 MHz crystal in series resonance.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Current Analog, IVPA	Power supply = 5.25V 51 MHz data rate			10	mA
Supply Current Digital, IVPD	Power supply = 5.25V 1 MHz data rate			6	mA
Short Circuit Output Current (to ground) All others, IOS	Power supply = 5.25V	30		100	mA

DYNAMIC CHARACTERISTICS AND TIMING (Load Capacitance = 50 pF)

DATA DETECTION CHARACTERISTICS (See Figure 2)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TRDDW RDTA pulse width		25			ns
TRDWP RDW period	R1 = 0, R2 = 1		8		µsec
	R1 = 0, R2 = 0		4		µsec
	R1 = 1, R2 = 0		2		µsec
	R1 = 1, R2 = 1		1		µsec

DATA DETECTION CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TRDWW	RDW pulse width high or low	Same R1, R2 as above		TRDWP / 2		µs
TRDW	RDD pulse width		62.5		187.5	ns
TRDDD	Propagation Delay from RDW transition to RDD positive edge	Same R1, R2 as above	0.025	TRDWP / 4		µs

DRQ CHARACTERISTICS (See Figure 2)

TDLY	Propagation delay from DRQ positive edge to DRQD positive edge	SCLK = 1	0.75		1.0	µs
		SCLK = 0	1.50		2.0	µs
TDRLL	Propagation delay from DRQ negative edge to DRQD negative edge				50	ns

CRYSTAL CHARACTERISTICS

TXTALP	Crystal oscillator frequency period			62.5		ns

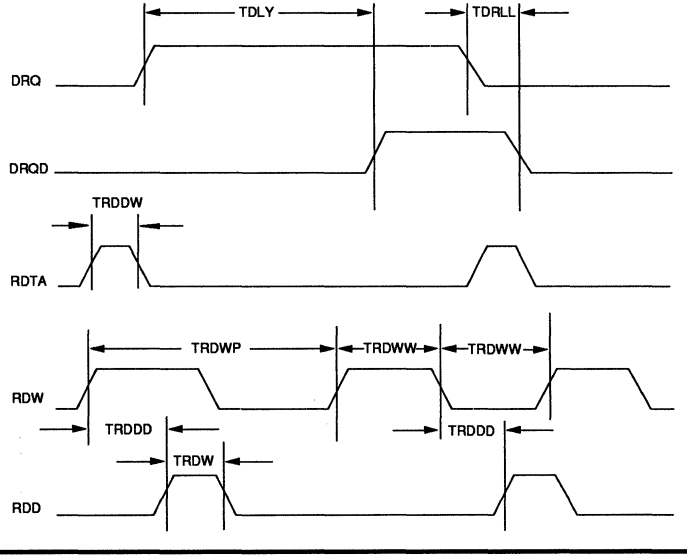


FIGURE 2: Timing Diagram

PHASE-LOCK-LOOP CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCO frequency range	Nominal frequency set by R1, R2, see Table 1	±20		±40	%
KVCO VCO gain	R2=1, R1=0		$0.5x10^6$		rad/s/V
	R2=0, R1=0		$0.96x10^6$		rad/s/V
	R2=0, R1=1		$1.75x10^6$		rad/s/V
	R2=1, R1=1		$2.98x10^6$		rad/s/V
KPD phase detector gain	RPDGAIN = 39KΩ ± 1%		15.9		µA/rad
VCO phase reset error				±0.2	rad
Number of RDW periods delay from RDTA to RDD			0.5		
Number of RDW periods VCO may be disabled during reference switching				3	

REFERENCE CLOCK (See Figure 3)

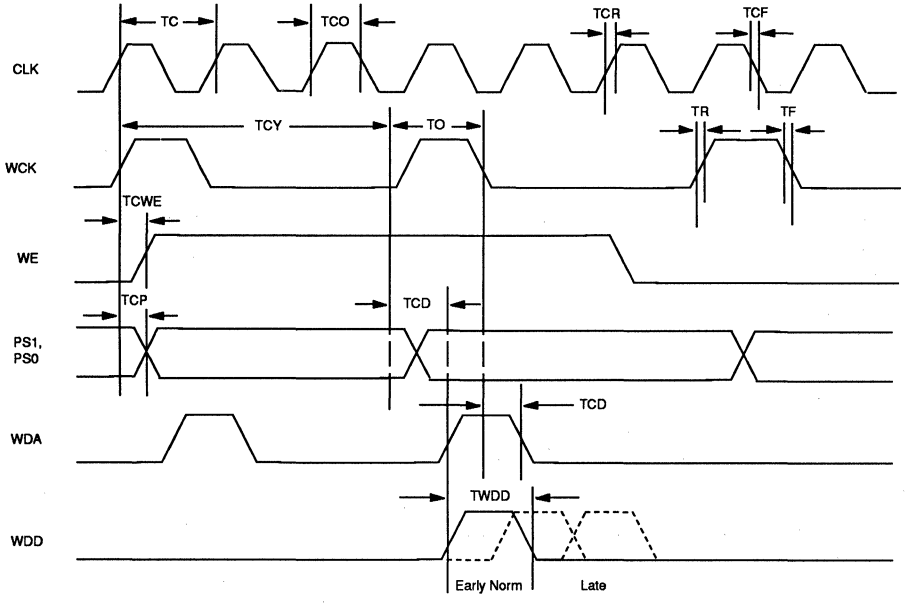
PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TC CLK period	SCLK = 1		125		ns
	SCLK = 0		250		ns
TCO CLK pulse width low or high			TC/2		ns
TCR CLK rise time				15	ns
TCF CLK fall time				15	ns

WRITE PRECOMPENSATION SWITCHING CHARACTERISTICS (See Figure 3)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TCY WCLK period	R1 = 0, R2 = 1		4		µs
	R1 = 0, R2 = 0		2		µs
	R1 = 1, R2 = 0		1		µs
	R1 = 1, R2 = 1		0.5		µs
TO WCLK pulse width	All combinations of R1, R2		250		ns
TR WCLK rise time				15	ns
TF WCLK fall time				15	ns

WRITE PRECOMPENSATION SWITCHING CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TCWE Propagation delay from WCLK positive edge to WE positive edge		10		100	ns
TCP Propagation delay from WCLK positive edge to PS0, PS1 transition		10		100	ns
TCD Propagation delay from WCLK positive edge to WDA negative edge		10		100	ns
TWDD WDD pusle width		62.5			ns



Note 1: Not to scale.
Note 2: Read data waveforms do not show delay between RDIA and RDW.
Note 3: Write data waveforms do not show WDD precompensation by exact amounts specified.
Note 4: WCLK and CLK have their rising edges synchronized.

FIGURE 3: Switching Characteristics

APPLICATION

LOOP FILTER

The element in the phase lock loop which controls the loop dynamics is known as the loop filter. Acquisition time, data margin, and data tracking can be optimized by the loop filter selection. One possible loop filter configuration is shown in Figure 4, where the function of C_1 is as an integrating element. The larger the capacitance of C_1, the longer will be the lock time. If the capacitance is too small, the loop will tend to track high frequency jitter. The role of the resistor R is to reduce the phase shift induced by C_1. This is necessary since the loop will oscillate at the frequency where the gain is unity. The capacitor C_2 will suppress high frequency transients when switching occurs. This capacitor will have a minimal effect of the loop response if it is small compared to C_1 (typically, $C_2 = C_1/19$).

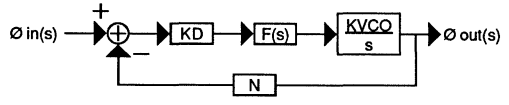
The loop filter transfer function is:

$$F(s) = \frac{Vout}{Iin} = \frac{1 + sRC_1}{sC_1\left(1 + sC_2R + \frac{C_2}{C_1}\right)}$$

if $C_2 < C_1$
then,

$$F(s) = \frac{Vout}{Iin} = \frac{1 + sRC_1}{sC_1}$$

The phase lock loop can be described as:



where,

KD = phase detector gain [A/rad]
F(s) = Filter impedance [V/A]
$\frac{KVCO}{s}$ = oscillator transfer function [rad/volt - sec]
N = ratio of reference input frequency vs. VCO output frequency.

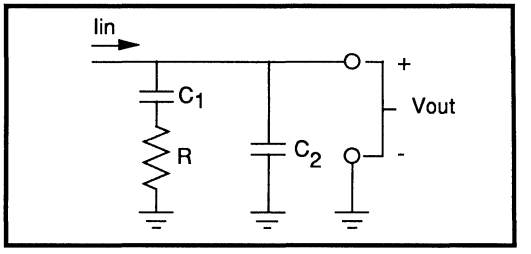


FIGURE 4: Loop Filter

Therefore, the closed loop transfer function is now:

$$T(s) = \frac{Ø\ out(s)}{Ø\ in(s)} = \frac{G(s)}{1 + G(s)H(s)} =$$

$$\frac{KD \times KVCO\left(\frac{1 + sRC_1}{C_1}\right)}{s^2 + s(N \times KD \times KVCO \times R) + \frac{N \times KD \times KVCO}{C_1}}$$

now we can put the characteristic equation (denominator) in the form:

$$s^2 + 2s\zeta\omega_n + \omega_n^2$$

$$\therefore \omega_n^2 = \frac{N \times KD \times KVCO}{C_1} \text{ and } \zeta = \frac{N \times KD \times KVCO \times R}{2\omega_n}$$

which results in:

$$C_1 = \frac{N \times KD \times KVCO}{\omega_n^2}$$

$$R = \frac{2\zeta\omega_n}{N \times KD \times KVCO} \text{ and } C_2 = \frac{C_1}{19}$$

For a $\zeta = 0.8$, the relationship between ω_n and lock time is:

$$\omega_n = \frac{4.5}{\text{lock time}}$$

Therefore, the loop filter components C_1, C_2, and R can be evaluated for a required lock time and coding scheme (N) frequency relationship to the VCO frequency.

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LOOP FILTER (Continued)

For data rates of 250 Kbits/s, the bit cell is 4 µs long. A lock time of 3 bytes translates into:

lock time = 3 x 8 x 4 = 96 µs

Therefore:

$$\omega_n = \frac{4.5}{96\,\mu s} = 47\,Krad/s$$

$$C_1 = \frac{15.9 \times 10^{-6} \times 0.96 \times 10^{6}}{2 \times (47 \times 10^{3})^2} = 3500\,pF$$

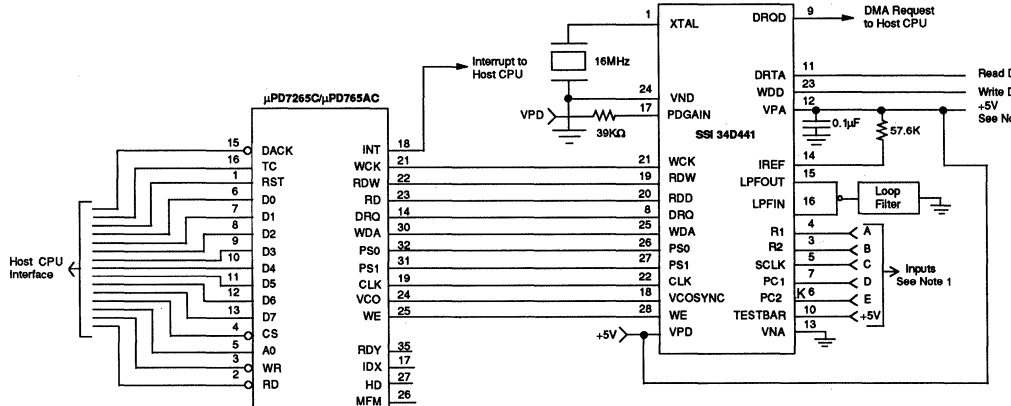
$$R = \frac{2 \times 0.8}{47 \times 10^{3} \times 3.5 \times 10^{-9}} = 9.8\,K\Omega$$

$$C_2 = \frac{C_1}{19} = 184\,pF$$

Table 3 lists suggested loop filter component values for various data rates. These values represent only a starting point for the design of the filter and they may be changed to meet the performance requirements of the system.

TABLE 3:

DATA RATE	LOCK TIME	LOOP FILTER
125 KHz	192 µs	R = 10 KΩ, C_1 = 6800 pF C2 = 360 pF
250 KHz	96 µs	R = 10 KΩ, C_1 = 3300 pF C_2 = 180 pF
500 KHz	46 µs	R = 11 KΩ, C_1 = 1500 pF C_2 = 82 pF
1 MHz	24 µs	R = 13 KΩ, C_1 = 680 pF C_2 = 39 pF



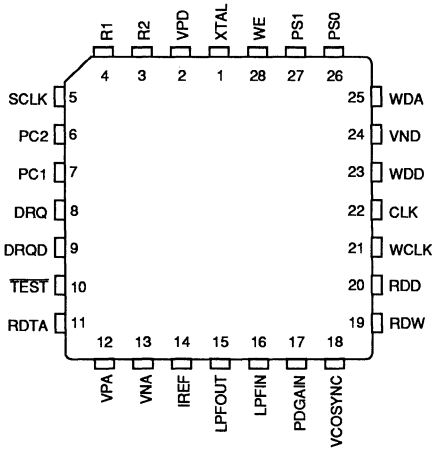
Note 1: Inputs A, B, C, D, and E may either be hardwired to desired control states, or may be programmable if controlled externally.

Note 2: A single voltage regulated +5V power supply should be used for VPA and VPD with appropriate bypassing capacitor.

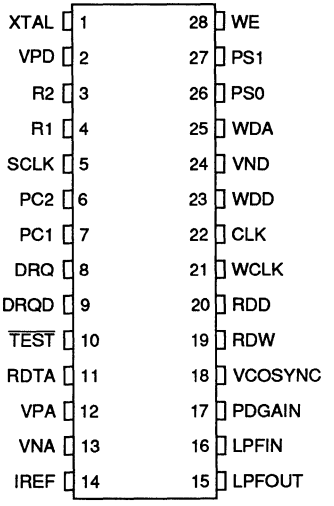
FIGURE 5: Application Diagram

PACKAGE PIN DESIGNATIONS

(Top View)



28-lead PLCC
PLCC pinouts are the same as the 28-pin DIP



600-mil
28-pin DIP

THERMAL CHARACTERISTICS: θja

28-lead PLCC	55°C/W
28-pin PDIP	65°C/W

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ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 34D441 28-pin PDIP	SSI 34D441-CP	34D441-CP
SSI 34D441 28-pin PLCC	SSI 34D441-CH	34D441-CH

Silicon Systems™
Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, TWX 910-595-2809

NOTES:

SSI 34P570
2-Channel Floppy Disk Read/Write Circuit

August, 1988

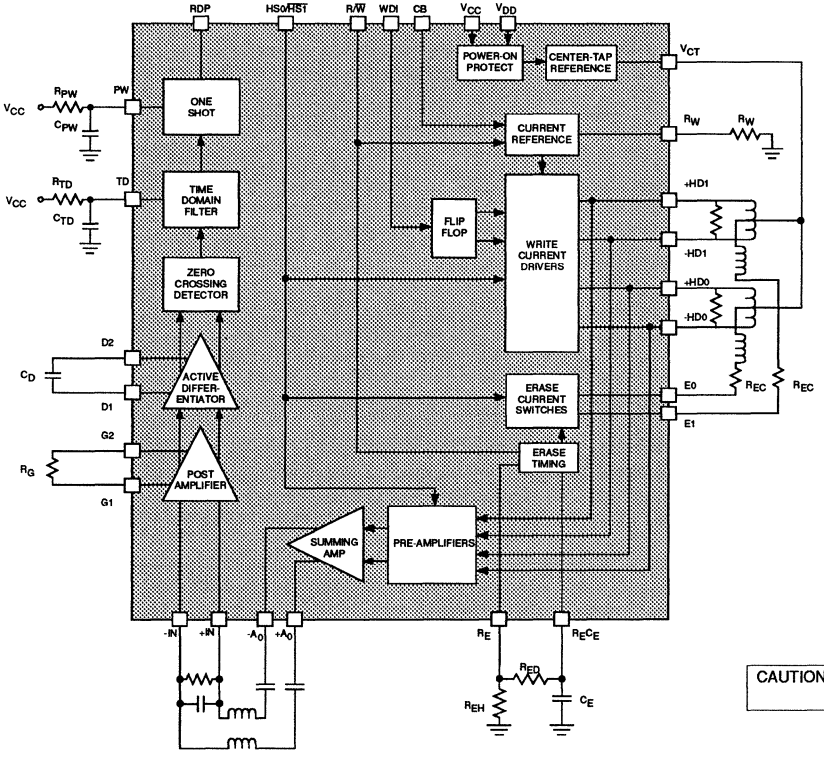
DESCRIPTION

The SSI 34P570 is an integrated circuit which performs the functions of generating write signals, amplifying and processing read signals required for a double-sided floppy disk drive. The write data circuitry includes switching differential current drivers and the erase head drive with programmable delay and hold times. The read data circuitry includes low noise amplifiers for each channel as well as a programmable gain stage and necessary equalization and filtering capability using external passive components. All logic inputs and outputs are TTL compatible and all timing is externally programmable for maximum design flexibility. The circuit operates on +12 volt and +5 volt power supplies and is available in 28-pin plastic DIP and PLCC packages.

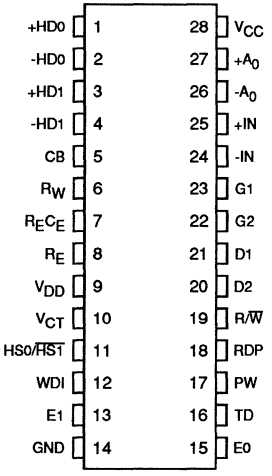
FEATURES

- **Single-chip read/write amplifier and read data processing function**
- **Compatible with 8", 5 1/4" and 3 1/2" drives**
- **Internal write and erase current sources, externally set**
- **Control signals are TTL compatible**
- **Schmitt trigger inputs for higher noise immunity on bussed control signals**
- **TTL selectable write current boost**
- **Operates on +12 volt and +5 volt power supplies**
- **High gain, low noise, low peak shift (0.3% typical) read processing circuits**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

0888

SSI 34P570
2-Channel Floppy Disk Read/Write Circuit

FUNCTIONAL DESCRIPTION

WRITE MODE CIRCUITRY

In Write Mode (R/$\overline{W}$ low), the circuit provides controlled write and erase currents to either of two magnetic heads. The write-erase circuitry consists of two differential write current drivers, a center tap voltage reference, two erase current switches and control circuits for head selection and erase timing.

Write current is toggled between opposing sides of the head on each negative transition of the write data input (WDI) and is set externally by a single resistor, Rw connected between the Rw terminal and ground. Since driver output impedance is large, proper damping resistors must be provided across each head. A signal at the CB terminal provides write current boost.

Erase current is also set externally through resistors REC connected in series with each erase coil. Erase can be activated by, but delayed from, selection of the write mode, and is held active after mode deselection. The turn-on delay is determined by the charging of CE through RED, while the hold time is determined by the discharge of CE through the series combination of RED and REH(see connection diagram). The RECE node may be driven directly by a logic gate, with external resistors per Figure 4, if the erase period is to be controlled separately from the write mode selection. For applications where no delays are required, CE is omitted.

The Center Tap Voltage Reference supplies both write and erase currents. A power turn-on protection circuit prevents undesired writing or erasure by holding the voltage reference off until the supply voltages are within their operating ranges.

READ MODE CIRCUITRY

In the Read Mode (R/$\overline{W}$ high), the circuit performs the functions of amplifying and detecting the selected head output pulses which correspond to magnetic transitions in the media. The read circuitry consists of two differential preamplifiers, a summing amplifier, a postamplifier, an active differentiator, a zero-crossing detector, a time domain filter, and an output one-shot.

The selected preamplifier drives the summing amplifier whose outputs are AC coupled to the postamplifier through an external filter network. The postamplifier adjusts signal amplitudes prior to application of signals to the active differentiator. Postamplifier gain is set as required by connecting a resistor across the gain terminals, G1 and G2. If desired, an additional frequency/phase compensation network may also be connected across these gain terminals.

The differentiator, driven by the postamplifier, provides zero-crossing output voltages in response to input signal peaks. Differentiator response characteristics are set by an external capacitor or more complex series network connected between the D1 and D2 terminals.

The zero-crossing detector provides a unipolar output for each positive or negative zero-crossing of the differentiator output. To enhance signal peak detection the time domain filter inhibits the detection of zero-crossings if they are not sufficiently separated in time. The filter period is set by an external RC network connected to the TD pin.

The time domain filter drives the output one-shot which generates uniform output data pulses. The pulse width is set by an external RC network connected to the PW pin. The output one-shot is inhibited while in the write mode.

ELECTRICAL CHARACTERISTIC Unless otherwise specified, 4.75 V ≤V_{CC} ≤5.25 V; 11.4 V ≤V_{DD}≤12.6; 0°C≤T_A≤70°C; R_W = 430 Ω; R_{ED} = 62 KΩ; C_E = 0.012 µF; R_{EH} = 62 KΩ; R_{EC} = 220 Ω

ABSOLUTE MAXIMUM RATINGS (Operating above absolute maximum ratings may damage the device.)

PARAMETER	RATING	UNIT
5 V Supply Voltage, V_{CC}	7	V
12 V Supply Voltage, V_{DD}	14	V
Storage Temperature	65 to +130	°C
Junction Operating Temperature	130	°C
Logic Input Voltage	-0.5 V to 7.0 V	dc
Lead Temperature (Soldering, 10 sec.)	260	°C
Power Dissipation	800	mW

POWER SUPPLY CURRENTS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
I_{CC} - 5 V Supply Current	Read Mode			35	mA
	Write Mode			38	mA
I_{DD} - 12 V Supply Current	Read Mode			26	mA
	Write Mode (excluding Write & Erase currents)			24	mA

LOGIC SIGNALS - READ/$\overline{\text{WRITE}}$ (R/$\overline{\text{W}}$), CURRENT BOOST (CB)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Low Voltage (V_{IL})				0.8	V
Input Low Current (I_{IL})	V_{IL} = 0.4 V			-0.4	mA
Input High Voltage (V_{IH})		2.0			V
Input High Current (I_{IH})	V_{IH} = 2.4 V			20	µA

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LOGIC SIGNALS - WRITE DATA INPUT (WDI), HEAD SELECT (HSO/$\overline{HS1}$)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Threshold Voltage, V_T + Positive - going		1.4		1.9	V
Threshold Voltage, V_T - Negative - going		0.6		1.1	V
Hysteresis, V_T + to V_T-		0.4			V
Input High Current, I_{IH}	V_{IH} = 2.4V			20	µA
Input Low Current, I_{IL}	V_{IL} = 0.4V			-0.4	mA

CENTER TAP VOLTAGE REFERENCE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Output Voltage (V_{CT})	I_{WC} + I_E = 3 mA to 60 mA	V_{DD} -1.5		V_{DD} - .5	V
V_{CC} Turn-Off Threshold	(See Note 1)	4.0			V
V_{DD} Turn-Off Threshold	(See Note 1)	9.6			V
V_{CT} Disabled Voltage				1.0	V

NOTE1: Voltage below which center tap voltage reference is disabled.

ERASE OUTPUTS (E1,E0)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Unselected Head Leakage	V_{E0}, V_{E1} = 12.6 V			100	µA
Output on Voltage (V_{E1}, V_{E0})	I_E = 50 mA			0.5	V

WRITE CURRENT

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Unselected Head Leakage	V_{E1}, V_{E0} = 12.6 V			25	µA
Write Current Range	Rw = 820 Ω to 180 Ω	3		10	mA
Current Reference Accuracy	I_{WC} = 2.3/Rw V_{CB}(current boost) = 0.5 V	-5		+5	%
Write Current Unbalance	I_{WC} = 3 mA to 10 mA			1.0	%
Differential Head Voltage Swing	Δ I_{WC} ≤ 5%	12.8			Vpk
Current Boost	V_{CB} = 2.4 V	1.25 I_{WC}		1.35 I_{WC}	

ERASE TIMING

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Erase Delay Range	R_{ED} = 39 KΩ to 82 KΩ C_E= 0.0015 µF to 0.043 µF	0.1		1.0	msec
Erase Delay Accuracy $\frac{\Delta T_{ED}}{T_{ED}} \times 100\%$	$T_{ED} = 0.69\ R_{ED}\ C_E$ R_{ED} = 39 KΩ to 82 KΩ; C_E = 0.0015 µF to 0.043 µF	-15		+15	%
Erase Hold Range	$R_{EH} + R_{ED}$ =78 KΩ to164 KΩ; C_E = 0.0015 µF to 0.043 µF	0.2		2.0	msec
Erase Hold Accuracy $\frac{\Delta T_{EH}}{T_{EH}} \times 100\%$	T_{EH}= 0.69 ($R_{EH} + R_{ED}$) C_E $R_{EH} + R_{ED}$ = 78 KΩ to 164 KΩ; C_E= 0.0015 µF to 0.043 µF	-15		+15	%

ELECTRICAL CHARACTERISTICS (Unless otherwise specified: V_{IN} (Preamplifier) = 10 mVp-p sine wave, dc coupled to center tap. (See Figure 1.) Summing Amplifier Load = 2 KΩ line-line, ac coupled. V_{IN} (Postamplifier) = 0.2 Vp-p sine wave, ac coupled; R_G = open; Data Pulse Load = 1 KΩ to Vcc; C_D = 240 pF; C_{TD} = 100 pF; R_{TD} = 7.5 KΩ ; C_{PW} = 47 pF; R_{PW}= 7.5 KΩ.)

READ MODE

PREAMPLIFIER - SUMMING AMPLIFIER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Voltage Gain	Freq. = 250 KHz	85		115	V/V
Bandwidth (-3 dB)		3			MHz
Gain Flatness	Freq. = dc to 1.5 MHz			±1.0	dB
Differential Input Impedance	Freq. = 250 KHz	20			KΩ
Max Differential Output Voltage Swing	V_{IN} = 250 KHz sine wave, THD ≤ 5%	2.5			Vp-p
Small Signal Differential Output Resistance	I_O ≤ 1.0 mAp-p			75	Ω
Common Mode Rejection Ratio	V_{IN} = 300 mVp-p @ 500 KHz Inputs Shorted	50			dB
Power Supply Rejection Ratio	Δ V_{DD} = 300 mVp-p @500 KHz Inputs shorted to V_{CT}.	50			dB
Channel Isolation	Unselected Channel V_{IN} 100mVp-p @ 500 KHz Selected channel input connected to V_{CT}	40			dB

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PREAMPLIFIER - SUMMING AMPLIFIER (cont'd.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Equivalent Input Noise	Power BW = 10 KHz to 1 MHz Inputs shorted to VCT.			10	µVrms
Center Tap Voltage, V_{CT}			1.5		V

POSTAMPLIFIER - ACTIVE DIFFERENTIATOR

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Ao, Differential Voltage Gain + IN, -IN to D1, D2	Freq. = 250 KHz (See Figure 2)	8.5		11.5	V/V
Bandwidth (-3 dB) + IN< -IN to D1, D2	C_D = 0.1 µF, R_D = 2.5 KΩ	3			MHz
Gain Flatness + IN, -IN to D1, D2	Freq. = dc to 1.5 MHz C_D = 0.1 µF, R_D = 2.5 KΩ			±1.0	dB
Max Differential Output Voltage Swing	V_{IN} = 250 KHz sine wave, ac coupled. ≤ 5% THD in voltage across C_D. (See Figure 2)	5.0			Vp-p
Max Differential Input Voltage	V_{IN} = 250 KHz sine wave, ac coupled. ≤ 5% THD in voltage across C_D. R_G = 1.5 KΩ	2.5			2.5 Vp-p
Differential Input Impedance		10			KΩ
Gain Control Accuracy $\frac{\Delta A_R}{A_R} \times 100\%$	$A_R = A_O R_G/(8 \times 10^3 + R_G)$ R_G = 2 KΩ	-25		+25	%
Threshold Differential Input Voltage. (See Note 2)	Min differential input voltage at post amp that results in a change of state at RDP V_{IN} = 250 KHz square wave, C_D = 0.1 µF, R_D = 500 Ω, T_R, TF ≤0.2 µsec No overshoot; Data Pulse from each V_{IN} . transition. (See Figure 3)			3.7	mVp-p
Peak Differentiator Network Current		1.0			mA

NOTE 2: Threshold Differential Input Voltage can be related to peak shift by the following formula:

$$\text{Peak Shift} = \frac{3.7\,mv}{\pi Vin} \times 100\%$$

where Vin = peak to peak input voltage at post amplifier. Note that this formula demonstrates an inverse relationship between the input amplitude and the Peak Shift.

TIME DOMAIN FILTER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Delay Accuracy $\frac{\Delta T_{TD}}{T_{TD}} \times 100\%$	T_{TD} = 0.58 R_{TD} x (C_{TD} + 10^{-11}) +50 nsec, R_{TD} = 5 KΩ, to 10 KΩ $C_{TD} \geq$ 56 pF. V_{IN} = 50m Vpp @ 250 KHz square wave, T_R, $T_F \leq$ 20 nsec, ac coupled. Delay measured from 50% input amplitude to1.5 V Data Pulse	-15		+15	%
Delay Range	T_{TD} = 0.58 R_{TD} x (C_{TD} + 10^{-11}) + 50 nsec, R_{TD} = 5 KΩ to 10 KΩ, C_{TD} = 56 pF to 240 pF	240		2370	ns

DATA PULSE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Width Accuracy $\frac{\Delta T_{PW}}{T_{PW}} \times 100\%$	T_{PW} = 0.58 R_{PW} x (C_{PW} +8 x 10^{-12}) + 20 nsec. R_{PW} = 5 KΩ to 10 KΩ C_{PW} = ≥36 pF width measured at 1.5V amplitudes	-20		+20	%
Active Level Output Voltage	I_{OH} = 400 µA	2.7			V
Inactive Level Output Leakage	I_{OL} =4 mA			0.5	V
Pulse Width	T_{PW} = 0.58 R_{PW} x (C_{PW} +8 x10-12) + 20 nsec. R_{PW} = 5 KΩ to 10 KΩ C_{PW} = 36 pF to 200 pF	145		1225	ns

TEST SCHEMATICS

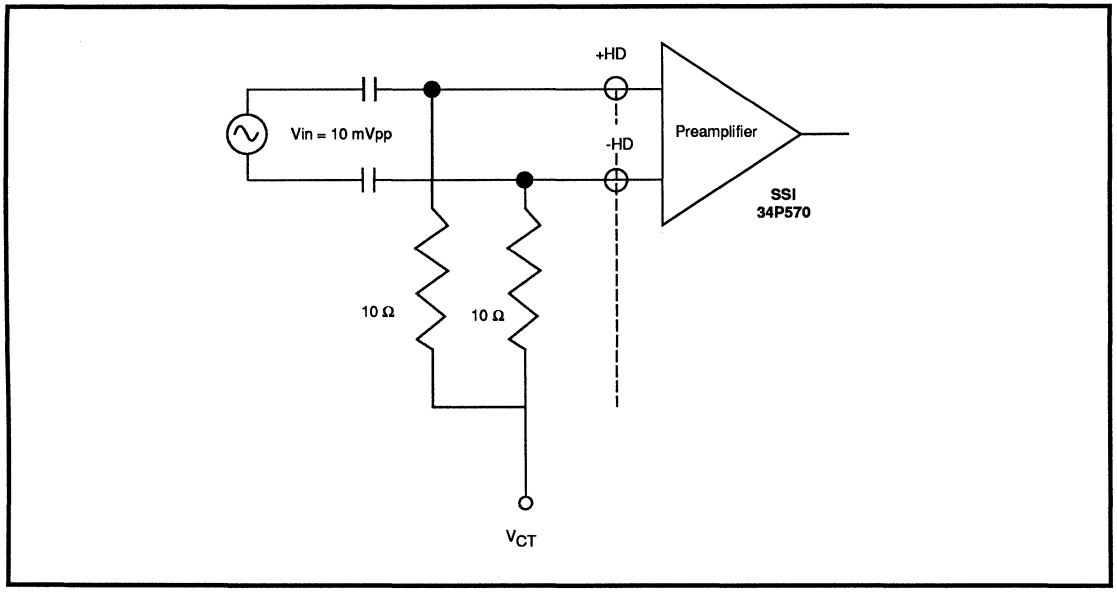

FIGURE 1: PREAMPLIFIER CHARACTERISTICS

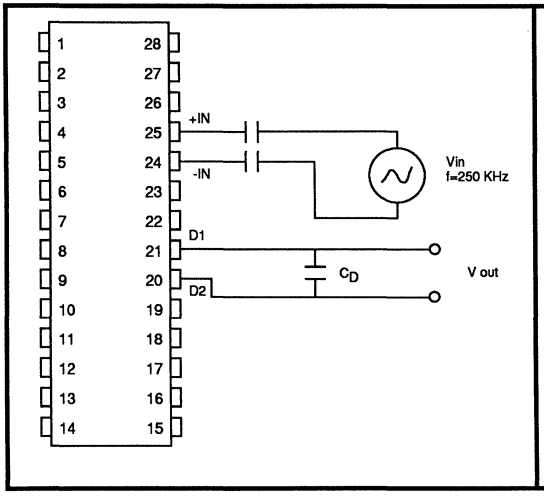

FIGURE 2:
POSTAMPLIFIER DIFFERENTIAL OUTPUT VOLTAGE SWING AND VOLTAGE GAIN

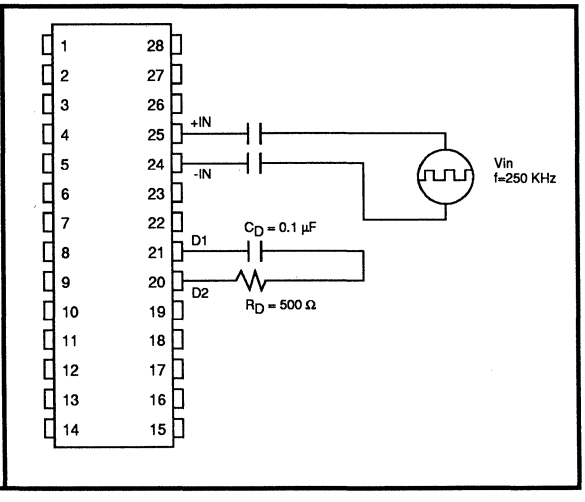

FIGURE 3:
POSTAMPLIFIER THRESHOLD DIFFERENTIAL INPUT VOLTAGE

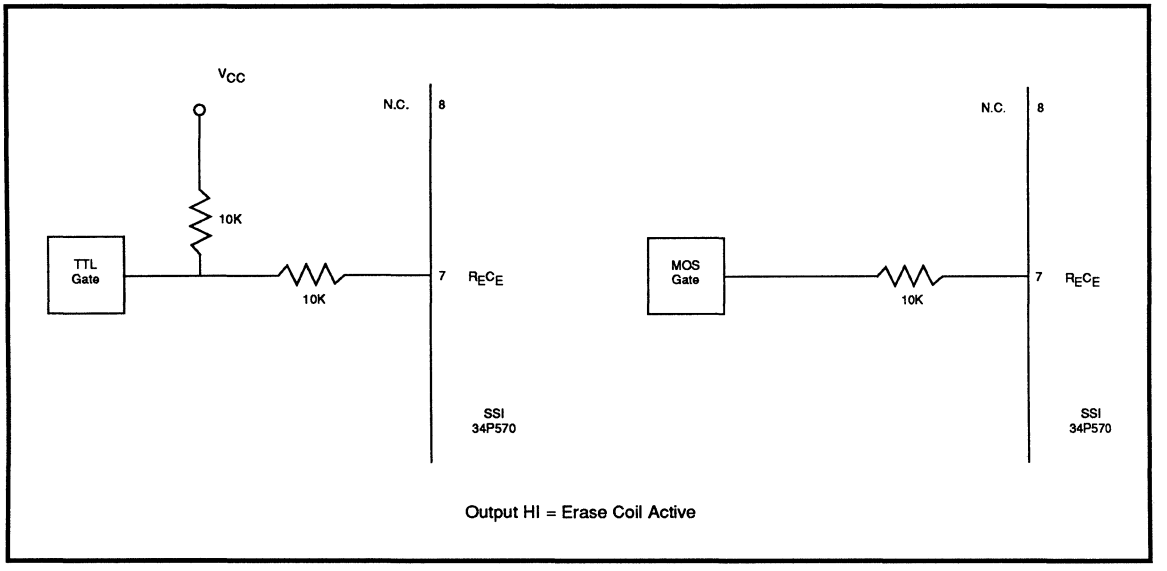

FIGURE 4 : EXTERNAL ERASE CONTROL CONNECTIONS

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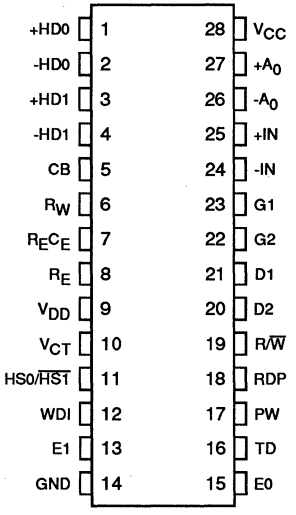
SSI 34P570
2-Channel Floppy Disk Read/Write Circuit

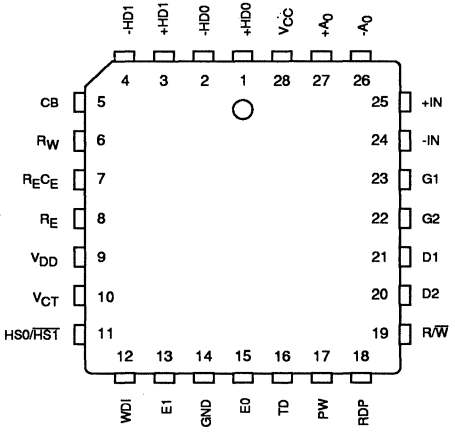
PACKAGE PIN DESIGNATIONS
(TOP VIEW)



28-Pin DIP

THERMAL CHARACTERISTICS: Ø ja

28-Pin	DIP	55°C/W
28-Pin	PLCC	65°C/W



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 34P570 28-Pin DIP	SSI 34P570-CP	34P570-CP
SSI 34P570 28-Pin PLCC	SSI 34P570-CH	34P570-CH

silicon systems™
14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

SSI 34R575
2 or 4-Channel Floppy Disk Read/Write Circuit

August, 1988

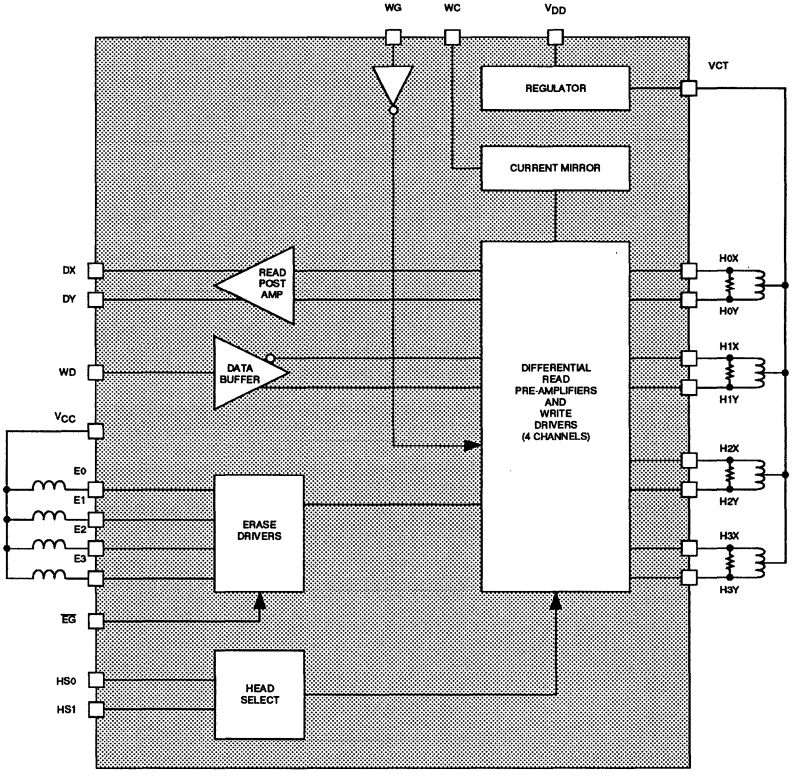
DESCRIPTION

The SSI 34R575 device is a bipolar monolithic integrated circuit used in floppy disk systems for head control and write, erase, and read select functions. The device has either two or four discrete read, write, and erase channels. Channel select inputs are TTL compatible. The SSI 34R575 device requires +5 V and +12 V power supplies and is available in 18-pin (2-channel version) or 24-pin (4-channel version) dual inline packages.

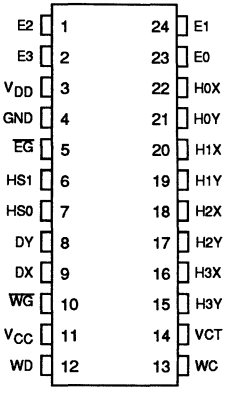
FEATURES

- **Operates on +5 V, +12 V power supplies**
- **Two or four channel capability**
- **TTL compatible control inputs**
- **Read/Write functions on one-chip**
- **Internal center tap voltage source**
- **Supports all disk sizes**
- **Applicable to tape systems**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 34R575
2 or 4-Channel Floppy Disk Read/Write Circuit

FUNCTIONAL DESCRIPTION

The SSI 34R575 functions as a write and erase driver or as a read amplifier for the selected head. Two TTL compatible inputs are decoded to select the desired read/write and erase heads. Head select logic is indicated in Table 1. Both the erase gate ($\overline{EG}$) and write gate ($\overline{WG}$) lines have internal pull up resistors to prevent an accidental write or erase condition.

MODE SELECTION

The read or write mode is determined by the write gate ($\overline{WG}$) line. The input is open collector TTL compatible. With the input low, the circuit is in the write mode. With the input high (open), the circuit is in the read mode. In the read mode, or with the +5 V supply off, the circuit will not pass write current.

ERASE

The erase operation is controlled by an open collector TTL compatible input. With erase gate ($\overline{EG}$) input high (open) or the +5 V supply off, the circuit will not pass erase current. With $\overline{EG}$ low, the selected open collector erase output will be low and current will be pulled through the erase heads.

READ MODE

With the $\overline{WG}$ line high, the read mode is enabled. In the read mode the circuit functions as a differential amplifier. The state of the head select input determines which amplifier is active. When the mode or head is switched, the read output will have a voltage level shift. External reactive elements must be allowed to recover before proper reading can commence. A current diverting circuit prevents any possible write current from appearing on a head line.

WRITE MODE

With the $\overline{WG}$ line low, externally generated write current is mirrored to the selected head and is switched between head windings by the state of the write data (WD) signal.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
V_{CC}		+5 V
V_{DD}		+12 V
H0X-H3X H0Y-H3X		X, Y head connections
DX, DY		X, Y Read Data: Differential read signal out
WG		Write gate: sets write mode of operation
WC		Write current: current mirror used to drive floppy disk heads
WD		Write data line
EG		Erase gate: allows erasure by selected head
E0-E3		Erase head driver connections
HS0-HS1		Head select inputs
GND		Ground
VCT		Center Tap Voltage Source

TABLE 1: HEAD SELECT LOGIC

4 - CHANNELS		
HS1	HS0	HEAD
0	0	0
0	1	1
1	0	2
1	1	3

2 - CHANNELS	
HS1	HEAD
0	0
1	1

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(Operating above absolute maximum ratings may damage the device.)

PARAMETER		RATING	UNIT
DC Supply Voltage:	Vcc	6.0	V
	Vdd	14.0	V
Write Current		10	mA
Head Port Voltage		18.0	V
Digital Input Voltages:	DX, DY, HS0, HS1, WD	-0.3 to + 10	V
	$\overline{EG}$, $\overline{WG}$	-0.3 to V_{cc} + 0.3	V
DX, DY Output Current		-5	mA
VCT Output Current		-10	mA
Storage Temperature Range		-65 to + 150	°C
Junction Temperature		125	°C
Lead Temperature (Soldering, 10 sec.)		260	°C

RECOMMENDED OPERATING CONDITIONS (0°C<Ta<50°C, 4.7 V<Vcc<5.3 V, 11 V<V_{DD}<13 V)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Vcc Supply Current					
Read mode	Vcc MAX			15	mA
Write mode	Vcc MAX			35	mA
V_{DD} Supply Current					
Read mode	V_{DD} MAX			25	mA
Write mode	V_{DD} MAX			15	mA
Write Current			5.5		mA

ERASE OUTPUT

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Erase On Voltage	IE = 80 mA	0.7		1.3	VDC
Erase Off Leakage				100	µA

LOGIC SIGNALS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Head Select (HS0, HS1) and Write Data (WD)					
Low Level Voltage		-0.3		0.8	VDC
High Level Voltage		2.0		6.0	VDC
Low Level Current	V_{IN} = 0 volts	-1.6			mA
High Level Current	V_{IN} = 2.7 volts			40	µA
$\overline{\text{WRITE GATE}}$ ($\overline{\text{WG}}$) and $\overline{\text{ERASE GATE}}$ ($\overline{\text{EG}}$)					
Low Level Voltage		-0.3		0.81	VDC
High Level Input Current		-300			µA
Low Level Current	V_{IN} = 0 volts	-2.0			mA

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Gain	f = 100 KHz, Vin = 5 mV Rms RL = 10 KΩ	80	100	120	V/V
Bandwidth	Vin = 5 m W Rms RL = 10 K CL = 15pF	9			MHz
Input Voltage Range for 95% Linearity	f = 100 KHz, RL = 10 K	25			mVpp
Differential Input Resistance	f = 1 MHz	100			KΩ
Differential Input Capacitance	f = 1 MHz			10	pF
Input Bias Current				25	μA
Input Offset Voltage				12	mV
Output Voltage, Common Mode			8		VDC
Output Resistance				35	Ω
Output Current Sink		2			mA
Output Current Source		3			mA
Common Mode Rejection Ratio	f = 1 MHz (input referred)	50			dB
Power Supply Rejection Ratio	f = 1 MHz (input referred)	50			dB
Channel Separation	f = 1 MHz (input referred)	50			dB
Input Noise	BW = 100 Hz to 1 MHz, Z Source = 0		7		μV RMS

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Write Current Gain	IW = 5.5 mA	.97		1.05	A/A
Write Current Voltage Level	IW = 5.5 mA	1.2		2.1	VDC
Differential Head Voltage	IW = 5.5 mA	12.5			VDC
Unselected Head Current	IW = 5.5 mA DC Condition			0.1	mA
Write Current Unbalance	IW = 5.5 mA			1	%
Write Current Time Symmetry	IW = 5.5 mA			±10	ns
Read Amplifier Output Level			10.5		VDC
Center Tap Voltage	(Read and Write Modes)		8.5		VDC

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Write and Erase Gate Switching Delay	Delay to 90% of Write Current			1	µsec
Head Select Switching Delay				1	µsec
Head Current Switching Delay	T1 in Fig. 1		10		nsec
Head Current Switching Time	IW = 5.5 mA Shorted Head		10	30	nsec
Write to Read Recovery Time				2	µsec

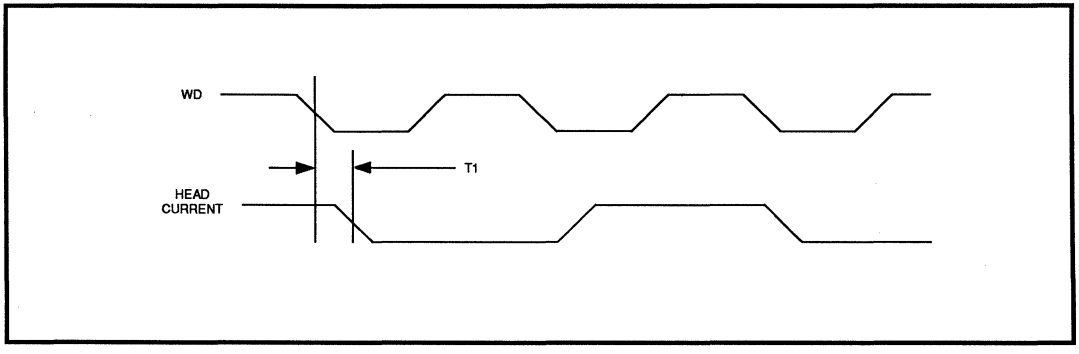
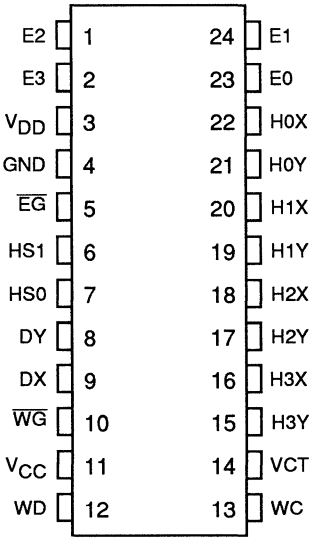


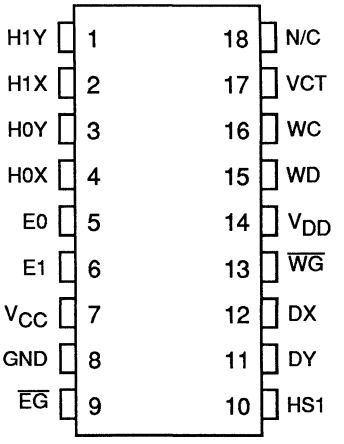
FIGURE 1: HEAD CURRENT SWITCHING DELAY

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



24-Pin DIP



18-Pin DIP

7

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 34R575 24-Pin DIP	SSI 34R575-4CP	34R575-4CP
SSI 34R575 18-Pin DIP	SSI 34R575-2CP	34R575-2CP

silicon systems™
14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

NOTES:

SSI 34B580
Port Expander
Floppy Disk Drive

August, 1988

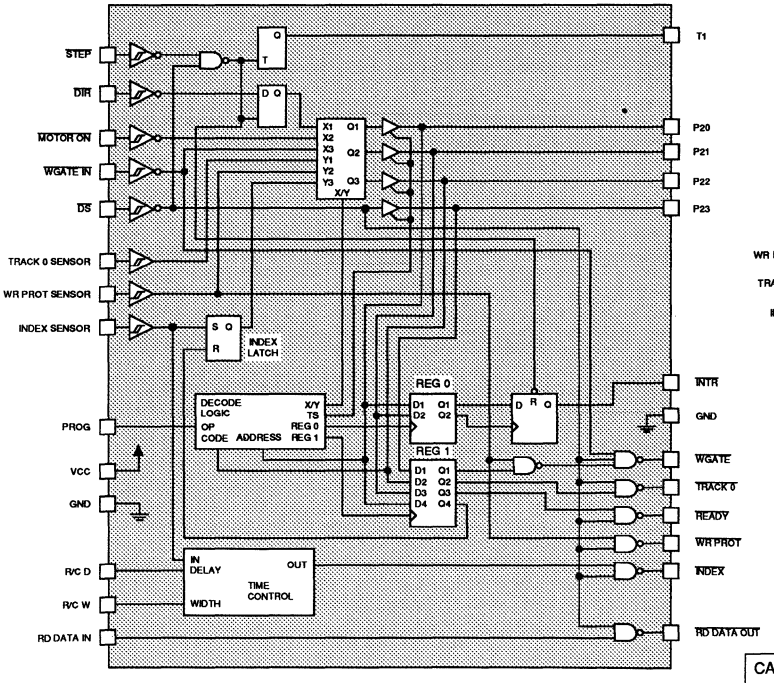
DESCRIPTION

The SSI 34B580 device is a bipolar integrated circuit that serves as an input/output port expander for an 8084 type microprocessor based floppy disk drive system. The device consolidates functions normally performed by a variety of LSTTL, SSI, AND MSI devices. The combination of an SSI 34P570 (read, write, and erase device), an 8048 type microprocessor, and the SSI 34B580 provides the majority of electronics required for a SA400 type floppy disk drive system, including host interface bus driver and receiver. In addition to its port expansion function, the SSI 34B580 processes system data and provides both pulse width and delay control (adjustable by external elements) for the INDEX SENSOR input. The device requires a single +5 V power supply and is available in a 28-pin package.

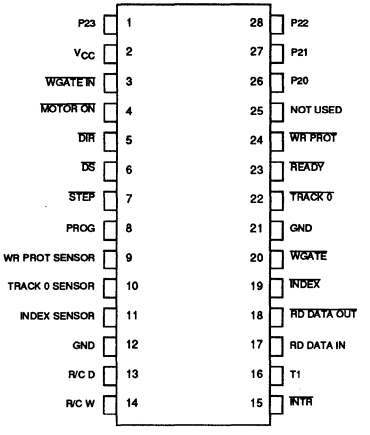
FEATURES

- **Reduces package count in flexible disk drive systems**
- **Replaces bus interface and combinational logic devices between the SSI 34P570, on board microprocessor and mechanical interfaces**
- **Surface mount available for further real estate reduction**
- **Provides drive capability for mechanical and system interfaces**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

7

FUNCTIONAL DESCRIPTION

PORTS

The SSI 34B580 has two 4-bit input ports, Port A and Port B. Port A receives data from the host interface bus for conveyance to the drive's read/write circuitry and to the microprocessor. Three sensors report the status of the drive to the 34B580 via Port B. Common to both ports is a drive select ($\overline{DS}$) signal from the host interface bus. This allows the host to address separate disk drives. There is also a 4-bit bidirectional port on the SSI 34B580. This is port 2 and it can be used by the microprocessor to write to or read from the SSI 34B580.

READ MODE

Ports A and B can be read by a microprocessor via Port 2. This allows the microprocessor to obtain data from the host interface bus and the status sensors. The PROG signal from the microprocessor provides the timing for the operation. First an OP code and a port address must be placed on Port 2 (see Table 1), then latched in on the falling edge of PROG. When the OP code and addresses have been decoded, the desired input port is selected and output on Port 2. The operation is terminated by the rising edge PROG, which returns Port 2 to the input mode.

WRITE MODE

In the write mode the microprocessor passes system parameters to the SSI 34B580 for logic processing and outputting. Table 2 shows how each bit of Port 2 affects the SSI 34B580. A logic one on the zero bit of Port 2 will reset the index latch. P21, qualified by the $\overline{DS}$ signal, sends a "this drive ready" signal from the microprocessor the the host interface bus. Similarly P22 is $\overline{DS}$ qualified and sent to the host as a signal that the head is positioned over track 0. P23 is used in the logic that sends a R/$\overline{W}$ signal to the drive's read/write circuitry. The write mode occurs when the proper OP code and address is placed on Port 2 and latched in on the falling edge of PROG (see Table 2). The microprocessor writes in the data on PROG's rising edge.

INDEX PULSE

An optical sensor connected to the INDEX SENSOR pin detects the diskette's index marker. The state of the index sensor is latched into the SSI 34B580 and is available to be read by the microprocessor on P22. The latch may be reset by writing a one to P20 from the microprocessor. The pulse received from the sensor also drives the host interface signal $\overline{INDEX}$, the width and delay of which can be controlled by external R/C circuits. The time constant attached to the R/C D pin determines the delay from the INDEX SENSOR input to the $\overline{INDEX}$ signal on the host interface bus. The equation for the delay is Td = 0.59Rd x Cd (seconds). The width of the $\overline{INDEX}$ signal is determined by the circuit attached to the R/C W pin and the equation Tw = 0.59Rw x Cw (seconds).

INTERRUPT

The $\overline{INTR}$ signal is asserted every time a step command is issued to the drive on the host interface bus. Thus when $\overline{INTR}$ is tied to the interrupt pin of 8048 type microprocessor, an interrupt service routine will be executed on each step command. This routine typically obtains information on the direction the heads should move and the status of the track 0 sensor to use for generating the stepper motor control signals. The interrupt signal is cleared (set high) by first placing the the proper OP code and address on Port 2 (seeTable 2). This is latched in on the falling edge of PROG, then on its rising edge logic ones on P20 and P21 will be latched in to set $\overline{INTR}$ back to a high state. Note that an indeterminate operation will result from holding the INDEX SENSOR latch reset (holding P20 high).

T1 PIN

This signal changes state with the $\overline{STEP}$ command of the host interface bus when the drive is selected. It drives the T1 pin on an 8048 type microprocessor which is an input to a counter. The 8048 can use this count and the DIR signal read from Port 2 of the SSI 34B580 to monitor the head position and issue a CB (current boost) command to the SSI 34P570 when a specific track is reached.

INPUT TO PORT2		READ FROM PORT 2				4-BIT
OP Code P22	Addr. P20	P23	P22	P21	P20	Input Port
0	0	$\overline{DS}$	Index Sensor Latch	WR Sensor	Track 0 Sensor	B
0	1	$\overline{DS}$	$\overline{WGATEIN}$	$\overline{MOTORON}$	$\overline{DIR}$	A

TABLE 1: READ MODE

INPUT TO PORT2		DATA PROCESSED FROM PORT 2				
OP Code P22	Addr. P20	$\overline{WGATE}$	$\overline{TRACK0}$	$\overline{READY}$	$\overline{INTR}$	Index Latch Reset
1	0	Z	$\overline{(P22 \cdot DS)}$	$\overline{(P21 \cdot DS)}$		P20
1	1				See Text	
Where Z = (P23 • WR PROT SENSOR) + $\overline{(DS \cdot WGATEIN)}$						

TABLE 2: WRITE MODE

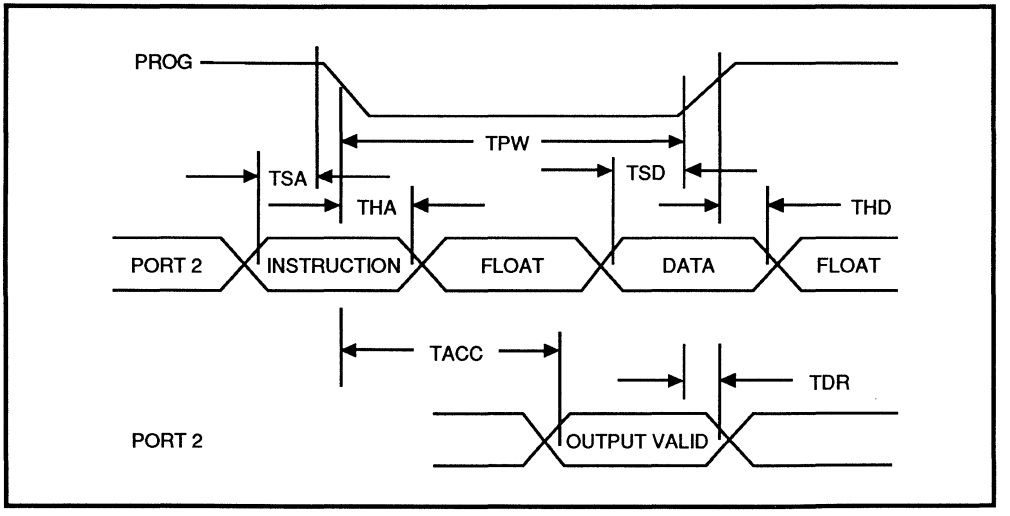


FIGURE 1: TIMING DIAGRAM

PIN DESCRIPTIONS

NAME	TYPE	DESCRIPTION
P20 - P23	I/O	4-bit bidirectional port, referred to as Port 2.
$\overline{\text{WGATE IN}}$	I	This input command to write is asserted by the host interface bus.
$\overline{\text{MOTOR ON}}$	I	This input command to turn on the spindle motor comes from the host interface bus.
$\overline{\text{DIR}}$	I	Input from the host interface bus selecting the direction in which the stepper motor should move the head.
$\overline{\text{DS}}$	I	Drive Select
INDEX SENSOR	I	Input from the photodiode that indicates the index marker in the diskette.
WR PROT SENSOR	I	Input from the photodiode that indicates if the diskette is write protected.
TRACK 0 SENSOR	I	Input from the photodiode that detects when the head is positioned over track 0.
$\overline{\text{STEP}}$	I	Input from the host interface bus indicating that the head should be moved.
T1	O	This pin changes state when a $\overline{\text{STEP}}$ command is received from the host interface bus.
RD DATA IN and $\overline{\text{RD DATA OUT}}$	I/O	Read data path
$\overline{\text{WGATE}}$	O	Output to the disk drive's read/write circuitry.
$\overline{\text{INDEX}}$	O	Output to the host interface bus indicating index sensor status.
$\overline{\text{TRACK 0}}$	O	Output to the host interface bus indicating track 0 sensor status.
$\overline{\text{READY}}$	O	Output to the host interface bus indicating track 0 sensor status.
$\overline{\text{WR PROT}}$	O	Output to the host interface bus indicating write protect sensor status.
PROG	I	Input from the 8048 microprocessor for I/O control of the SSI 34B580.
$\overline{\text{INTR}}$	O	Output to the interrupt pin of the 8048 microprocessor.
R/C D and R/C W		The external resistor and capacitor networks tied to these pins determine the delay and width of the output pulse to the $\overline{\text{INDEX}}$ pin.
Vcc		+5 V supply
GND		Ground

ABSOLUTE MAXIMUM RATINGS (All voltages referred to GND)

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
DC Supply	+ 7	VDC
Voltage Range (any pin to GND)	-0.4 to + 7	VDC
Power Dissipation	700	mW
Storage Temperature	-40 to + 125	°C
Lead Temperature (10 sec soldering)	260	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, 4.75 ≤ Vcc ≤ 5.25 VDC; 0°C < Ta < 70°C)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Totem pole outputs (P20 - P23, $\overline{\text{INTR}}$, T1)					
Output High Voltage	IOH = -400 A	2.5			V
Output Low Voltage	IOL = 2 mA			0.5	V
Open collector outputs ($\overline{\text{RD DATA OUT}}$, $\overline{\text{INDEX}}$, $\overline{\text{WGATE}}$, $\overline{\text{TRACK0}}$,$\overline{\text{READY}}$, $\overline{\text{WR PROT}}$)					
Output High Current	VOH = 5.25 V			250	µA
Output Low Voltage	IOL = 48 mA			0.5 V	V
Inputs (P20 - P23, PROG, RD DATA IN)					
Input High Voltage		2.0			V
Input Low Voltage				0.8	V
Input Low Current	VIL = 0.5 V			-0.8	mA
Input High Current	VIH = 2.4 V			40	µA
Input Current	Vin = 7.0 V			0.1	mA
Schmitt - Trigger Inputs ($\overline{\text{WGATE IN}}$, $\overline{\text{MOTOR ON}}$, $\overline{\text{DIR}}$, $\overline{\text{DS}}$, $\overline{\text{STEP}}$)					
Threshold Voltage	Positive Going, Vcc = 5.0 V	1.3		2.0	V
	Negative Going, Vcc = 5.0 V	0.6		1.1	V
Hysteresis	Vcc = 5.0 V	0.4			V
Input High Current	VIH = 2.4 V			40	µA
Input Low Current	VIL = 0.5 V			-0.4	mA
Input Current	VIN = 7.0 V			0.1	mA

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High Impedance Inputs with Hysteresis (WR PROT SENSOR, TRACK 0 SENSOR, INDEX SENSOR)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input High Voltage				2.0	V
Input Low Voltage		0.8			V
Hysteresis		0.2			V
Input Current	Vin = 0 to Vcc			-0.25	mA

TIMING CHARACTERISTICS (Unless otherwise specified; Ta = 25°C; 4.75V ≤ Vcc≤ 5.25V; CL = 15 pf.)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Propagation Delay Time	RD DATA IN to $\overline{\text{RD DATA OUT}}$			35	ns
	$\overline{\text{DS}}$ to $\overline{\text{WGATE}}$, $\overline{\text{TRACK 0}}$ $\overline{\text{READY}}$ $\overline{\text{WR PROT}}$,$\overline{\text{RD DATA}}$, $\overline{\text{INDEX}}$			80	ns
	PROG to $\overline{\text{INTR}}$, $\overline{\text{WGATE}}$, $\overline{\text{TRACK 0}}$ (Rising edge) $\overline{\text{READY}}$, $\overline{\text{WR PROT}}$			100	ns
	$\overline{\text{WR PROT}}$ to $\overline{\text{WGATE}}$, $\overline{\text{WR PROT SENSOR}}$			250	ns
	$\overline{\text{WGATE}}$ IN to $\overline{\text{WGATE}}$			80	ns
	$\overline{\text{STEP}}$ to T1, P20			80	ns
	TRACK 0 SENSOR WR PROT SENSOR to Port 2 INDEX SENSOR			250	ns
	$\overline{\text{MOTOR ON}}$ $\overline{\text{WGATE IN}}$ to Port 2 $\overline{\text{DS}}$			80	ns
Data Setup Time	$\overline{\text{DIR}}$ to $\overline{\text{STEP}}$	50			ns
Data Hold Time	$\overline{\text{DIR}}$ to $\overline{\text{STEP}}$	0			ns
Delay Accuracy (Pin 13)	Td = 0.59 Rd x Cd R_D = 3.9 K to 10 K C_D = 75 pF to 300 pF	0.8TD		1.2TD	sec
Pulse Width Accuracy (Pin 14)	Tw = 0.59 Rw x Cw Rw = 3.9 K to 10 K Cw = 75 pF to 300 pF	0.8Tw		1.2Tw	sec

PORT 2 (P20 - P23) TIMING (Timing Referenced to PROG signal, Figure 1.)

SYMBOL	DESCRIPTION	MIN	NOM	MAX	UNIT
TSA	Addr. setup time	100			ns
THA	Addr. hold time	80			ns
TSD	Data-in setup time	100			ns
THD	Data-in hold time	80			ns
TACC	Data-out access time			700	ns
TDR	Data-out release time			200	ns
TPW	PROG pulse width	1500			ns

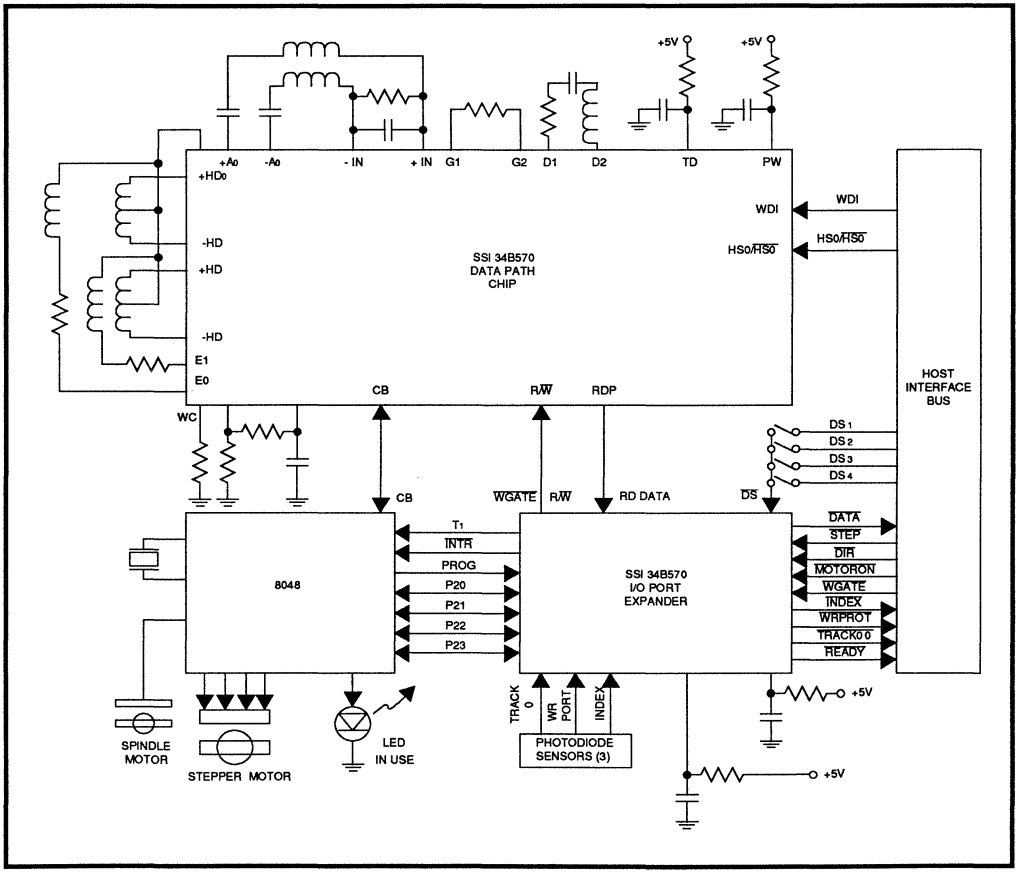
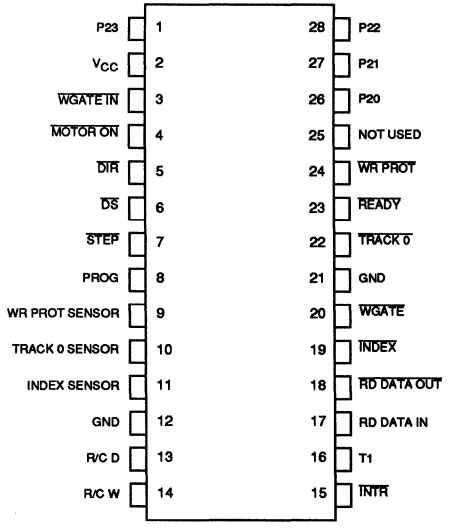


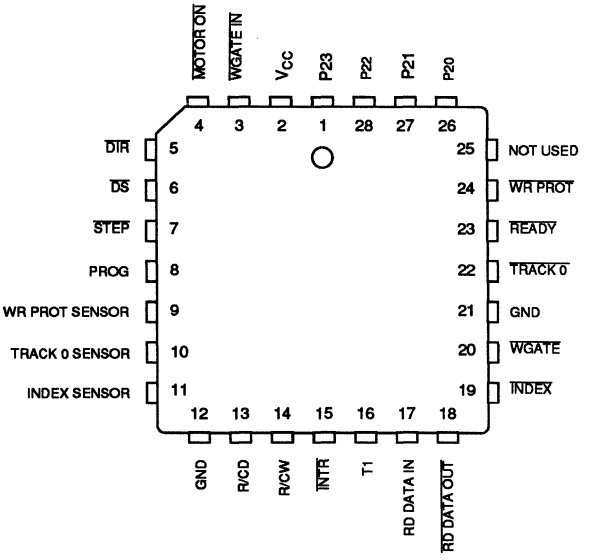
FIGURE 2: TYPICAL APPLICATION

SSI 34B580
Port Expander
Floppy Disk Drive

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 34B580 28-Pin DIP	SSI 34B580-CP	34B580-CP
SSI 34B580 28-Pin PLCC	SSI 34B580-CH	34B580-CH

silicon systems™
14351 Myford Road, Tustin, CA 92680 (714) 731-7110, TWX 910-595-2809

Section 8

TAPE DRIVE CIRCUITS

SSI 35P550
4-Channel Magnetic Tape Read Circuit

August, 1988

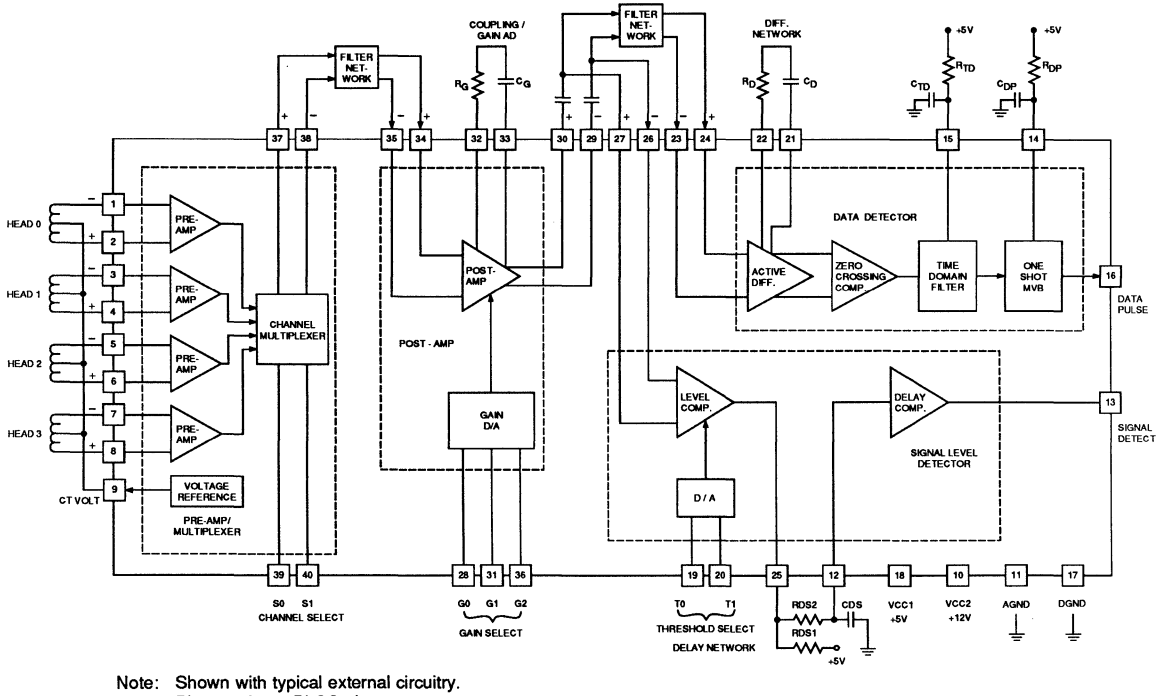
DESCRIPTION

Silicon Systems' SSI 35P550 combines magnetic tape head read signal amplification and processing onto a single integrated circuit. The device accepts up to 4 center-tapped magnetic read heads connected directly to the head inputs; head center tap voltage is provided by an on-chip reference. The device architecture permits system design flexibility by providing the external connections between the Preamplifier/Multiplexer, Postamplifier, Signal Level Detector, and Data Detector; this allows the implementation of many suitable filtering combinations. Low noise amplifiers are used throughout the device. The SSI 35P550 operates on +5 and +12 Volt supplies and has TTL compatible control signals.

FEATURES

- **4-Channel Multiplexer with differential-input Preamplifiers**
- **Postamplifier has component-adjustable and programmable gain**
- **On-chip Signal Level Detector with programmable threshold and adjustable delay**
- **Data Detection Circuit includes spurious signal rejection (adjustable time domain filter) and provides an adjustable uniform Data Pulse output**
- **Available in 40-pin DIP or 44-pin PLCC plastic packages**

BLOCK DIAGRAM



Note: Shown with typical external circuitry.
Pin #s refer to PLCC pinout.

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

4-CHANNEL PREAMPLIFIER AND MULTIPLEXER

The device contains four low level differential-input Preamplifiers. The differential output of a single Preamplifier is selectively connected to the Preamplifier output terminals by means of two logical CHANNEL SELECT signals, S0 and S1. The selected Preamplifier number is the binary value of the logical SELECT signals for active high voltage levels.

The Preamplifier inputs are intended for connection to center-tapped magnetic read heads. An appropriate Preamplifier input bias voltage level is obtained by connecting the head center taps to the circuit C.T. VOLT terminal.

The C.T. VOLT terminal is the output of a voltage reference which has a value to center the Preamplifier inputs within their operating range.

POSTAMPLIFIER

The Postamplifier is a differential-input, differential-output circuit which has two means of gain adjustment. A continuously-variable gain adjustment is obtained by use of an external resistor or potentiometer. Discrete values of gain setting are additionally obtained by applying combinations of logical signal levels to the three GAIN SELECT terminals, G0, G1, and G2.

The Postamplifier receives the output signals of the Preamplifier after frequency selection by an external filter network. The input characteristics of the Postamplifier are such that the inputs may have DC coupling to the Preamplifier output, or may be AC coupled with proper bias of 3V nom.

A suitable coupling capacitor must be connected between the GAIN1, GAIN2 terminals independent of the use of a gain setting resistor.

SIGNAL LEVEL DETECT CIRCUITS

The Signal Level Detect circuits consist of detector circuits which compare the amplitude of the signal envelope of the Postamplifier output with a selectable threshold and provide a logical output level which indicates the presence of Postamplifier signal greater than the threshold. AC coupling is required between the Postamplifier output and the Signal Level Detect circuits input. The Signal Level Detect input has internal bias connections so that no external bias network is required.

The threshold to which the Postamplifier signals are compared is selected by means of two THRESHOLD SELECT logical inputs T0 and T1. The result of the comparison is delayed from appearing at the circuit SIGNAL DETECT output terminal by means of a delay circuit which is adjustable by means of external components. The delay associated with signal detection is set by combinations of capacitor CDS and resistor RDS1. The delay associated with signal loss is set by combinations of CDS and resistors RDS1 plus RDS2.

DATA DETECTION CIRCUITS

The Data Detection circuits are AC coupled to the Postamplifier outputs through an (optional) external filter network and provide logical output pulse signals in response to positive and negative input signal amplitude peaks. This function is performed by differentiating input signals to obtain zero-crossing voltages at points of inflection and detecting these crossings to provide output signals.

To enhance the signal peak detection, spurious inflection points which occur in pairs between true signal peaks are suppressed by means of the Time Domain Filter. The filter inhibits the propagation of detected zero-crossings if they are not sufficiently separated in time. This time period is set by external capacitor CTD and resistor RTD.

Uniform DATA PULSE output signals are provided by the One-Shot Multivibrator which is triggered by outputs of the Time Domain Filter. The time duration of the DATA PULSE signals is set by external capacitor CDP and RDP.

DC paths through the external filter network to the Signal Level Detect circuits inputs are required to properly bias the Data Detection circuits. The resistance of each path is not critical and may be as large as 10 KΩ.

PIN DESCRIPTION

NAME	40-PIN	44-PIN	DESCRIPTION
IN0 -	1	1	Channel 0 (-) input
IN0 +	2	2	Channel 0 (+) input
IN1 -	3	3	Channel 1 (-) input
IN1 +	4	4	Channel 1 (+) input
IN2 -	5	5	Channel 2 (-) input
N/C		6	No internal connection
IN2 +	6	7	Channel 2 (+) input
IN3 -	7	8	Channel 3 (-) input
IN3 +	8	9	(+) input
CT VOLT	9	10	Center tap voltage
VCC2	10	11	+ 12 Volt supply connection
AGND	11	12	Analog signal ground
DEL IN	12	13	Input to delay comparator
SIGNAL DETECT	13	14	Output of delay comparator
DPN	14	15	External RC for output pulse width
TDF	15	16	External RC for time-domain delay
N/C		17	No internal connection
DATA PULSE	16	18	Output of time-domain filter
DGND	17	19	Ground
VCC1	18	20	+5 Volt supply
T0	19	21	Threshold select signal (1 of 2)
T1	20	22	Threshold select signal (1 of 2)
CAP1	21	23	External differentiating capacitor connection
CAP2	22	24	
DIF -	23	25	Inputs to active differentiator
DIF +	24	26	
LEV OUT	25	27	Output to level detector
N/C		28	No internal connection
LEV -	26	29	Inputs to level detector
LEV +	27	30	
G0	28	31	Postamp gain select (1 of 3)

PIN DESCRIPTION (Continued)

NAME	40-PIN	44-PIN	DESCRIPTION
PSTOUT -	29	32	Outputs of Postamplifier
PSTOUT +	30	33	
G1	31	34	Postamp gain select (1 of 3)
GAIN 1	32	35	External Postamplifier gain adjusting RC terminals
GAIN 2	33	36	
PSTIN +	34	37	Inputs to Postamplifier
PSTIN -	35	38	
N/C		39	No internal connection
G2	36	40	Postamp gain select (1 of 3)
PREOUT +	37	41	(+) Output of Preamplifier
PREOUT -	38	42	(-) Output of Preamplifier
S0	39	43	Input channel select (1 of 2)
S1	40	44	Input channel select (1 of 2)

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
Storage Temperature	-65 to +150	°C
Junction Operating Temperature	0 to 130	°C
Supply Voltage, VCC1	-0.5 to +6.0	VDC
Supply Voltage, VCC2	-0.5 to +14.0	VDC
Voltage Applied to Logic Inputs	-0.5 to VCC1 +0.5	VDC
Voltage Applied to OFF Logic Outputs	-0.5 to VCC1 +0.5	VDC
Current Into ON Logic Outputs	5.0	mA
Lead Temperature (soldering, 10 sec)	+260	°C

DC CHARACTERISTICS
(Unless otherwise specified, VCC1 = 4.75V to 5.25V, VCC2 = 11.4V to 12.6V, Ta = 0 to 70 °C.)

CHARACTERISTICS	CONDITIONS	MIN	NOM	MAX	UNITS
Input Current Logical Inputs HIGH	Vih = VCC1			100	µA
Input Current Logical Inputs LOW	Vil = 0V			-400	µA
Output Voltage Delay Comparator OFF	Ioh = -400 µA	2.4			V
Output Voltage Delay Comparator ON	Iol = 2.0 mA			0.5	V
Data Pulse Inactive Level Output Voltage	Ioh = -400 µA	2.4			V
Data Pulse Active Level Output Voltage	Iol = 2.0 mA			0.5	V
VCC1 Power Supply Current	No Head Inputs			30	mA
VCC2 Power Supply Current	No Head Inputs			62	mA
NOTE: Characteristic applies to Inputs S0, S1, G0, G1, G2, T0, T1					

PREAMPLIFIER AND MULTIPLEXER CHARACTERISTICS
Output Load = 2 KΩ line-line, Channel Select Signals (S0,S1): VON = 2V Min., VOFF = 0.8V Max.

CHARACTERISTICS	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain	Vin = 4 mV p-p @ 100 KHz ref. to CT VOLT	80		120	V/V
Gain Flatness	Vin = 4 mV p-p DC to 0.5 MHz ref. to CT VOLT	±0.5			dB
Bandwidth, -1 dB	Vin = 4 mV p-p	1.5			MHz
Bandwidth, -3 dB	Vin = 4 mV p-p	3.0			MHz
Differential Input Impedance	Vin = 4 mV p-p @ 100 KHz ref to CT VOLT	10			KΩ
Common-Mode Rejection Ratio	Vin = 300 mV p-p @ 500 KHz Inputs shorted to CT VOLT	50			dB
Power Supply Rejection Ratio	Δ VCC = 300 mV p-p @ 500 KHz Inputs shorted to CT VOLT	50			dB
Channel Isolation	Unselected Vin = 100 mV p-p @ 2 MHz. Selected Channel inputs connected to CT VOLT	60			dB

PREAMPLIFIER AND MULTIPLEXER CHARACTERISTICS (Continued)

CHARACTERISTICS	CONDITIONS	MIN	NOM	MAX	UNITS
Total Harmonic Distortion	Vin = 0.5 to 6.0 mV p-p @ 500 KHz			2	%
Equivalent Input Noise	Power BW = 10 KHz to 1MHz Inputs shorted to CT VOLT			10	μVrms
Small Signal Single-Ended Output Res.	Io = 1 mA p-p @ 100 KHz			35	Ω
Maximum Diff. Output Voltage	Freq = 100 KHz THD < 5%	3			Vp-p
Output Offset Voltage	Inputs shorted to CT VOLT Volt Load = Open Circuit			±1.0	V
Common-Mode Output Voltage	Inputs shorted to CT VOLT Volt Load = Open Circuit	2.68		3.5	V
Center Tap Voltage, CT VOLT			3.0		V

DATA DETECTION CIRCUIT CHARACTERISTICS

Vin = 1.0V p-p diff. square wave, Tr, Tf < 20 nsec, dc-coupled (for biasing).
RD = 2.5 KΩ; CD = 0.1 μF; RTD = 7.8 KΩ; CTD = 200 pF; RDP = 3.9 KΩ;
CDP = 100 pF. Data Pulse load = 2.5 KΩ to VCC1 plus 20 pF or less to PWR GND.

CHARACTERISTICS	CONDITIONS	MIN	NOM	MAX	UNITS
Differentiator Maximum Differential Input Voltage	Vin = 100 KHz sine wave, dc-coupled. < 5% THD in voltage across CD. CD = 620 pF RD = 0	5.0			Vp-p
Differentiator Input Impedance	Vin = 4V p-p diff., 100 KHz sine wave. CD = 620 pF RD = 0	10			KΩ
Differentiator Threshold Differential Input Voltage	Vin = 100 KHz square wave, Tr, Tf , 0.4 μsec, no overshoot. Data Pulse from each Vin transition.			300	mVp-p
Data Pulse Width Accuracy	TDP = .59 RDP X CDP, RDP = .85 TDP 3.9 KΩ to10 KΩ, CDP = 75 pF to 300 pF. Width measured at 1.5V amplitude	.85TDP		1.15TDP	sec

DATA DETECTION CIRCUIT CHARACTERISTICS

CHARACTERISTICS	CONDITIONS	MIN	NOM	MAX	UNITS
Time Domain Filter Delay Accuracy	TTD = 0.59 RTD X CTD + 50 nsec, RTD = 3.9KΩ to 10 KΩ, CTD =100pF to 750 pF Delay measured from 50% input amplitude to 1.5V Data Pulse amplitude	.85TTD		1.15TTD	sec
Data Pulse Width Drift from + 25 °C value	Width measure from 1.5V amplitude			±5.0	%
Time Domain Filter Delay Drift from +25 °C value	Delay measured from 50% Input amplitude to 1.5V Data Pulse amplitude			±5.0	%
Note: Differentiating network impedance should be chosen such that 1 mA peak current flows at maximum signal level and frequency.					

SIGNAL LEVEL DETECT CIRCUITS CHARACTERISTICS

Level Comparator Inputs connected in parallel with Differentiator Inputs. Vin (Level Comp) = 100 KHz sine wave, ac-coupled. RDS1 = 5 KΩ; RDS2, CDS = open

CHARACTERISTICS	CONDITIONS	MIN	NOM	MAX	UNITS
Level Comparator Input Thresholds, Single-Ended, Each Input	T0 VT0 = 0.8V VT1 = 0.8V Vo pulse value < 0.5V at MAX LIMIT, >VCC1 - 0.5V at MIN LIMIT	30		70	mV pk
	T1 VT0 = 2.0V VT1 = 0.8V Vo pulse Value <0.5V at MAX LIMIT, >VCC1 - 0.5V at MIN LIMIT	97		153	mV pk
	T2 VT0 = 0.8V VT1 = 2.0V Vo pulse value <0.5V at MAX LIMIT, >VCC1 - 0.5V at MIN LIMIT	138		202	mV pk
	T3 VT0 = 2.0V VT1 = 2.0V Vo pulse value <0.5V at MAX LIMIT, >VCC1 - 0.5V at MIN LIMIT	210		290	mV pk
Level Comparator Diff. Input Resistance	Vin = 5 Vp-p @ 100 KHz	5			KΩ
Level Comparator Off Output Leakage	Vo = VCC1			25	µA

SIGNAL LEVEL DETECT CIRCUITS CHARACTERISTICS (Continued)

CHARACTERISTICS	CONDITIONS	MIN	NOM	MAX	UNITS
Level Comparator ON Output Voltage	VT0 = 0.8V VT1 = 0.8V Vin = ±140 mV diff. dc Io = 2.0 mA			0.25	V
Delay Comparator Upper Threshold Voltage	Vo > 2.4V	.65VCC1		.75VCC1	V
Delay Comparator Lower Threshold Voltage	Vo < 0.5V	.25VCC1		.35VCC1	V
Delay Comparator Input Current	0V < Vin < VCC1			25	µA

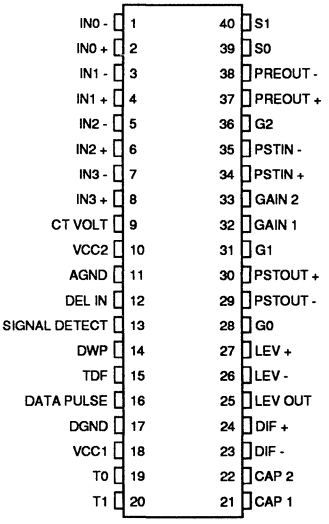
POSTAMPLIFIER CHARACTERISTICS

Output Load = 2.5 KΩ + 0.1 µF line-line, Vin = 100 mV p-p, 100 KHz sine wave, dc-coupled (to provide proper biasing). CG = 0.1 µF, RG = 0.

CHARACTERISTICS	CONDITIONS	MIN	MAX	UNITS
Differential Voltage Gain	A0 VG0 = 0.8V VG1 = 0.8V VG2 = 0.8V A1 VG0 = 2.0V VG1 = 0.8V VG2 = 0.8V A2 VG0 = 0.8V VG1 = 2.0V VG2 = 0.8V A3 VG0 = 2.0V VG1 = 2.0V VG2 = 0.8V A4 VG0 = 0.8V VG1 = 0.8V VG2 = 2.0V A5 VG0 = 2.0V VG1 = 0.8V VG2 = 2.0V A6 VG0 = 0.8V VG1 = 2.0V VG2 = 2.0V A7 VG0 = 2.0V VG1 = 2.0V VG2 = 2.0V ARG VG0 = 2.0V VG1 = 2.0V VG2 = 2.0V when RG = 2.5 KΩ	A7 - 14.75 A7 - 12.75 A7 - 10.75 A7 - 8.75 A7 - 6.75 A7 - 4.75 A7 - 2.75 32 A7 - 7.5	A7 - 13.25 A7 - 11.25 A7 - 9.25 A7 - 7.25 A7 - 5.25 A7 - 3.25 A7 - 1.25 36 A7 - 4.5	dB dB dB dB dB dB dB dB dB
Differential Input Impedance	VG0 = 2.0V VG1 = 2.0V VG2 = 2.0V	10		KΩ
Bandwidth, 1dB	VG0 = 2.0V VG1 = 2.0V VG2 = 2.0V	1.5		MHz
Bandwidth, 3dB	VG0 = 2.0V VG1 = 2.0V VG2 = 2.0V	3.0		MHz
Maximum Diff. Output Voltage	VG0 = 0.8V VG1 - 0.8V VG2 = 0.8V VIN = 100 KHz sine wave THD < 5%	5		Vp-p
Small Signal Single-Ended Output Res	VG0 = 2.0V VG1 = 2.0V VG2 = 2.0V VIN = 0V Io = 1 mA p-p, 100 KHz		35	Ω
Input Bias Offset Voltage Range	VG0 = 0.8V VG1 = 0.8V VG2 = 0.8V THD < 2.0%		±1.0	V
Input Bias Common-Mode Voltage Range	VG0 = 0.8V VG1 = 0.8V VG2 = 0.8V THD < 2.0%	2.68	3.5	V

SSI 35P550
4-Channel Magnetic Tape Read Circuit

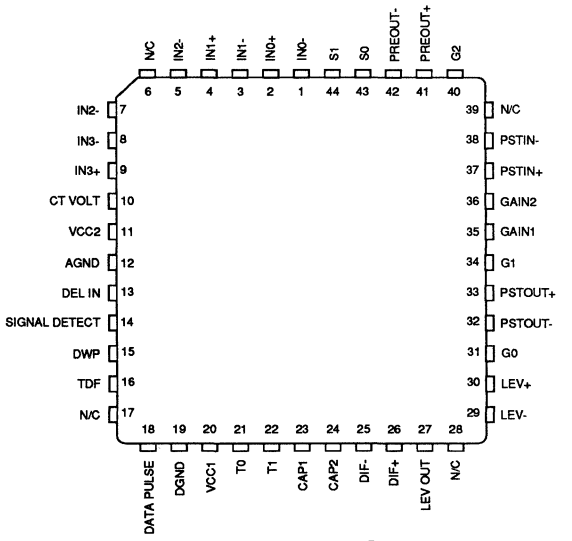
PACKAGE PIN DESIGNATIONS
(TOP VIEW)



40-Pin DIP

THERMAL CHARACTERISTICS: θja

40-pin PDIP	45°C/W
44-pin PLCC	60°C/W



44-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 35P550		
44-Pin PLCC	SSI 35P550-CH	35P550-CH
40-Pin DIP	SSI 35P550-CP	35P550-CP

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NOTES:

Section 9

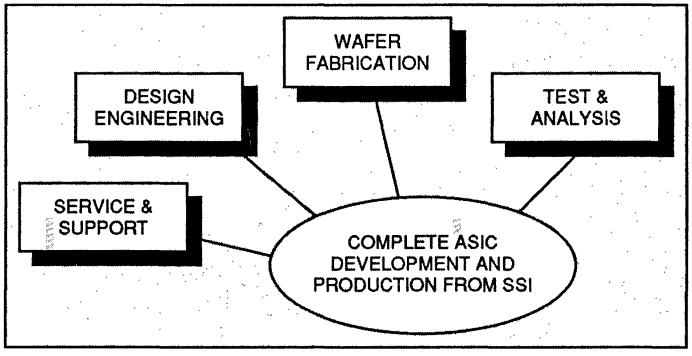
CUSTOM/SEMICUSTOM CAPABILITIES

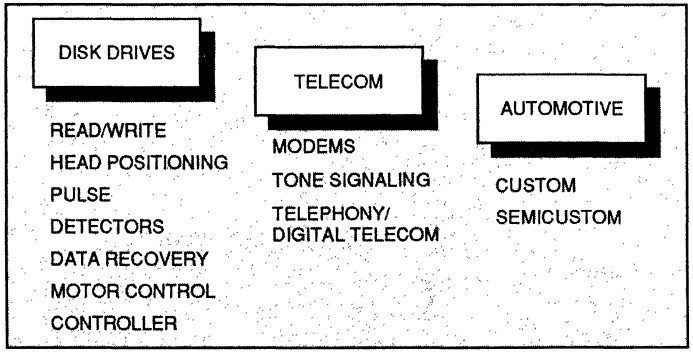
SILICON SYSTEMS LEADS THE WAY DEVELOPING MIXED-SIGNAL CUSTOM/SEMICUSTOM PRODUCTS

Silicon Systems is committed to leadership in the development of high-performance, mixed-signal custom/semicustom application-specific integrated circuits (ASICs).

Silicon Systems offers innovative designs for digital, analog, and mixed analog/digital ICs; a versatile range of CMOS and bipolar processes; quick-turn design methodologies supported by advanced and integrated design automation tools; specialized manufacturing facilities; comprehensive test, quality assurance, and prototype assembly programs; and, of course, greater than 15 years of IC design experience. SSi's efforts pay off by dramatically reducing the time (and cost) it takes to deliver the most optimized custom/semicustom ICs available.

Whether a customer's application falls in SSi's specialty areas of communications, microperipherals, automotive, or other areas, SSi's technical capabilities turn designs around faster and minimize a product's time to market for the competitive advantage.





BROAD RANGE OF ANALOG AND DIGITAL DESIGN EXPERIENCE

With a broad base of experience, systems knowledge, and applications expertise, SSi's designers provide creative IC solutions in both CMOS and bipolar process technologies for analog, digital, and mixed-signal applications.

In CMOS, SSi has designed digital products ranging from FIFOs to complex hard-disk drive controllers. Combined analog/digital products range from cross-point switches to complete, single-chip 2400 BPS modems.

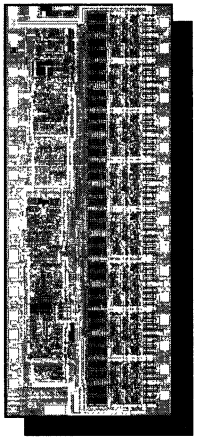
In bipolar, SSi's design expertise focuses on applications requiring high-speed ECL logic combined with high-performance analog circuitry. Bipolar products range from low-noise amps to very sophisticated data separators that employ patented phase locked loops.

TECHNIQUE	APPLICATION	SSi-DESIGNED EXAMPLES
CMOS Signal Processing	For analog continuous time and sampled data (switched-capacitor implementation) and Digital Signal Processing (DSP) applications. Low-power capability also allows inclusion of ROMs, RAMs, and other analog/digital subsystems.	-K224 complete single-chip 2400 BPS modem -C301 single-chip telephone headset amplifier -14.4 KBit modem -Direct-broadcast satellite descrambler -Motor controllers -Hi-resolution analog data acquisition
Bipolar Signal Processing	For high-performance, low noise, wideband signal acquisition and processing applications. Offers TTL and/or ECL logic interfaces with high current drive.	-Sub 1 nV/$\sqrt{Hz}$ HDD R/W amplifiers -AGC, pulse detection amplifiers -High-speed data separators -Wideband transceivers -PLLs (Phase Locked Loops) -Optical signal processing
Digital CMOS	For ASIC controllers, sequencers and data path applications with on-board ROM, RAM, and PLA sub-systems. Offers standard TTL and/or CMOS logic interfaces.	-Hard disk drive controllers -SCSI interface controllers -UARTs -Protocol controllers -Digital signal processors
Digital Bipolar	High-speed logic and interface circuitry. Offers standard logic or custom interfaces.	-Encoders and decoders -High-speed digital transceivers

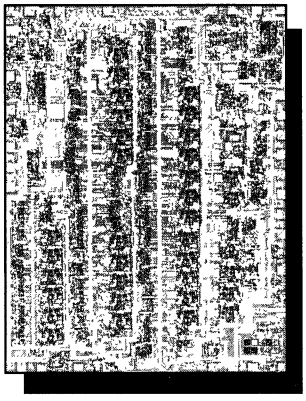
FULL ANALOG AND DIGITAL INTEGRATION ON THE SAME CHIP

Silicon Systems leads its competition in the design of complete systems on a chip which combine complex analog and digital functions. The total system solution approach allows designers to satisfy their application, cost, and performance objectives.

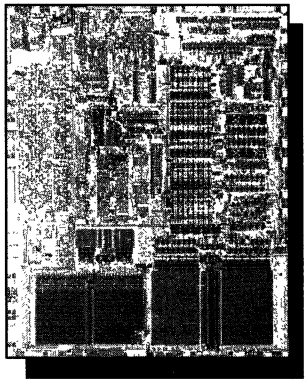
Custom mixed-signal Bipolar low-noise read/write IC



Standard Bipolar mixed-signal, high-performance data separator



Standard product single-chip 2400 BPS modem with switched capacitor filters and RISC DSP



"DESIGN-FOR-TESTABILITY" AND TEST SUPPORT

SSi employs design-for-testability methodologies, such as built-in test modes that allow direct testing of internal subsystems. SSi uses highly specialized equipment, test programs and test procedures for combined analog/digital designs to ensure delivery of high-quality product. To determine product reliability under extreme conditions, products are tested in-house by a wide variety of advanced analog or digital testers including:

- LTX (TS88/DX90) testers
- Eagle (LSI-4) testers
- Sentry 7 and Sentry 20 digital test systems

These testers are supported by:

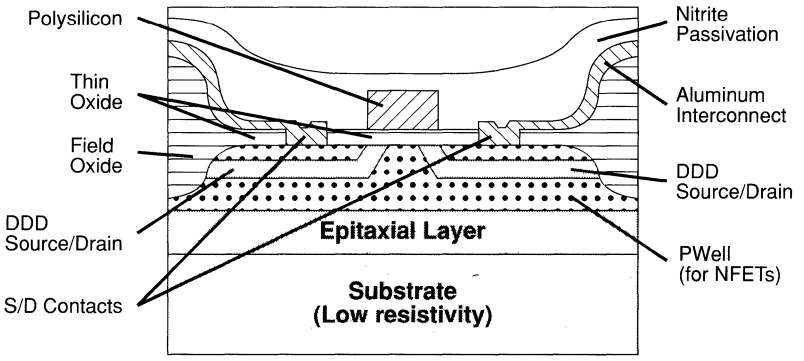
- Automatic handlers (Trigon PLCC, Symtek SOIC, and MCT and Daymarc handlers)
- Burn-in sockets, temperature chambers, Aehr burn-in ovens, and Highly Accelerated Stress Test (HAST)

CMOS TECHNOLOGIES...

SSi's state-of-the-art CMOS processes have allowed the company to become the leading supplier of systems-oriented, mixed analog/digital ASICs.

The "CH" process features a unique source/drain structure for higher voltage (12–volt) applications. Poly-poly capacitors support filtering and data conversion (A/D and D/A) applications. An epitaxial substrate provides latch-up protection for ASICs subject to adverse environments (such as motor control applications). And special poly resistors allow continuous time filters (for anti-aliasing functions) to be combined with sampled data, switched-capacitor filters, increasing the level of ASIC integration and lowering overall system manufacturing costs.

CH CMOS PROCESS TRANSISTOR



CMOS PROCESS CHART

PROCESS	TYPE/FEATURES	PRODUCTION	NEW DESIGNS	GATE SIZE (microns)	DIGITAL	ANALOG	INTERCONNECT LAYERS: PITCH (microns)	APPLICATION VOLTAGE
CB	High Voltage Metal Gate	Yes	No	7.2	Yes	Yes	Metal 1 (12.5)	18V
CF	Supports SSi 6600 Array Family only	Yes	No	4.0	Yes	Yes	Metal 1 (10.0) Poly 1 (8.0)	7V
CE	Digital CMOS, Supports Controller Group	Yes	Yes	2.0	Yes	No	Metal 1 (4.6) Metal 2 (6.0) Poly 1 (4.8)	5V
CD	Silicon Gate CMOS, High ohms/square Poly Option, Epi Substrate Available	Yes	Yes	3.5	Yes	Yes	Metal 1 (8.8) Poly 1 (5.8) Poly 2 (6.4)	12V
CH	Silicon Gate CMOS, Same Features as CD Plus Plasma (Dry) Metal Etch	Yes	Yes	3.5	Yes	Yes	Metal 1 (6.4) Poly 1 (5.8) Poly 2 (6.4)	12V
CG	Dual Poly, Dual Metal Silicon Gate	Development	Yes	1.5	Yes	Yes	Metal 1 (5.0) Metal 2 (7.6) Poly 1 (3.6) Poly 2 (5.0)	5V

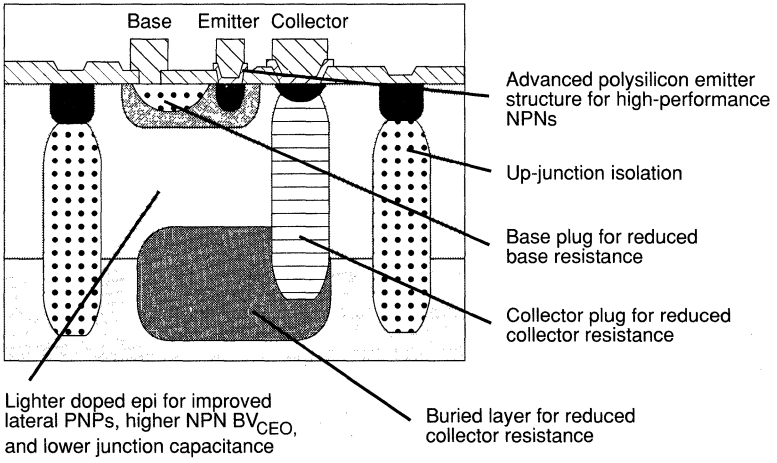
The "CG" process addresses 5-volt applications and features 1.5-micron gates and two layers of metal interconnect for high-performance digital circuitry, along with the dual poly layers required for analog circuitry. In addition to full-custom standard and customer-proprietary designs, both the "CH" and "CG" processes support a family of combined analog/digital CMOS arrays.

AND BIPOLAR TECHNOLOGIES

SSi's leading analog/digital bipolar technology is "BK," which supports the development of a wide variety of high-performance, combined analog/digital ASICs. In addition to full-custom standard and customer-proprietary designs, the "BK" process supports a family of advanced bipolar analog/digital arrays.

"BK" features a high-performance NPN (3 GHz F_T) with an operating capability of 12 BV_{CEO}. This process utilizes an advanced polysilicon emitter structure as well as base and collector plugs to reduce parasitic resistances for high-performance applications. Other key features include metal-nitride-poly capacitors, aluminum Schottky diodes, and improved lateral PNPs through the use of lighter doped epi.

BK BIPOLAR PROCESS NPN TRANSISTOR



BIPOLAR PROCESS CHART

PROCESS	TYPE/FEATURES	PRODUCTION	NEW DESIGNS	Emitter SIZE (microns)	DIGITAL	ANALOG	NPN F_T	INTERCONNECT LAYERS: PITCH (microns)	BV_{CEO} (volts)
BC	"Standard" Cut Emitter Process	Yes	No	6.0	Yes	Yes	1 GHZ	Metal 1 (14.0) Metal 2 (24.0)	12
BJ	High-Performance Polysilicon Emitter Structure	Yes	Yes	3.0	Yes	Yes	3 GHZ	Metal 1 (9.0) Metal 2 (14.0)	9
BK	Base and Collector Plugs, Improved Lateral PNPs	Yes	Yes	2.5	Yes	Yes	3 GHZ	Metal 1 (9.0) Metal 2 (14.0)	12

INTEGRATED DESIGN METHODOLOGY—THE IDM™ ADVANTAGE

Silicon Systems has spent almost 10 years developing its Integrated Design Methodology (IDM™). IDM consists of an interlocking set of design methods supported by a single Computer-Aided Engineering (CAE) and Computer-Aided Design (CAD) system. As IDM supports analog and digital designs in any of SSi's CMOS and bipolar technologies, it offers the tremendous advantage of flexibility.

COMPARE FULL-CUSTOM TO SEMICUSTOM DESIGN

IDM is based on two major design approaches: full-custom and semicustom.

Full-custom design is a "handcrafted" approach used to produce the most compact, high-performance design possible. Two approaches for full-custom physical design are possible: either composite or symbolic. In composite design, every process mask layer is drawn down to the process minimums. This yields the densest, highest-performance designs but is the most time-consuming approach. Symbolic design utilizes correct-by-construction, stick-like, process symbols, such as resistors, capacitors, and wires. Symbolic design is significantly more productive than composite and supports a higher level of circuit verification for greater design accuracy.

Semicustom design is an "automated" approach used to produce the most timely and cost-efficient designs possible. Two approaches are possible: either automatically placed-and-routed library components, including standard cells, or prefabricated array components.

SSi's analog and digital standard cells are pre-characterized, library-maintained circuits that are automatically placed and routed to generate a layout. The automatic place-and-route software also utilizes macro cell assemblers to route full-custom circuitry. The standard cell approach requires minimal layout effort, leading to lower development cost and a higher first article success rate.

SSi's mixed-signal arrays are bipolar and CMOS families of integrated circuits which are ninety percent prefabricated. The base arrays utilize a three-tile, three-segment structure each of which is targeted for a specific design application, i.e., analog, digital, and reference. The three segments forming the array core are separated by interconnect "highways" capable of handling both analog and digital signal busses. The core, in turn, is enclosed by a periphery of predefined I/O functions.

Array customization is achieved by the definition and interconnection of metal and poly-Si layers. SSi mixed-signal arrays provide a systems designer with fast prototype cycle times, lower integration costs, and the ability to migrate to either standard cell or custom integration with a minimum perturbation in design production.

CHOOSE THE OPTIMUM DESIGN APPROACH BASED ON TRADE-OFFS

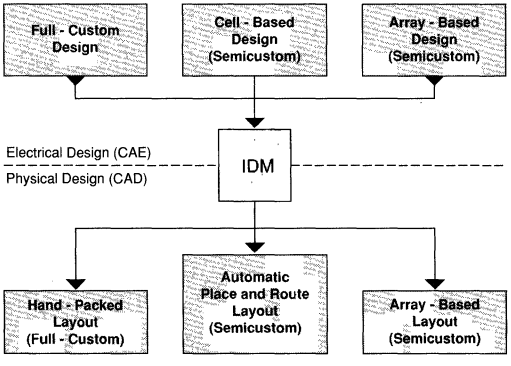
Each IDM design approach offers unique cost, time, and performance tradeoffs.

CUSTOM/SEMICUSTOM TRADE - OFFS				
	Full - Custom		Semicustom	
	Composite Design	Symbolic Design	Cell - Based Design	Array - Based Design
Design Parameters				
Cost (Non-Recurring Expense)	1.0	.50 - .80	.40 - .70	.20 - .40
Time (Schedule)	1.0	.50 - .70	.40 - .60	.20 - .40
Production Parameters				
Piece Price (Production Cost)	1.0	1.2 - 1.4	1.5 - 2.0	2.0 - 2.5
Die Size (Silicon Area)	1.0	1.1 - 1.2	1.3 - 1.6	1.6 - 2.0

NOTE: All comparisons are normalized to a composite-level design.

MIX FULL-CUSTOM AND SEMICUSTOM DESIGN ON A SINGLE CHIP

Due to the interlocking nature of SSi's design approaches, full-custom and semicustom design can be mixed on the electrical and/or physical design of any given IC.

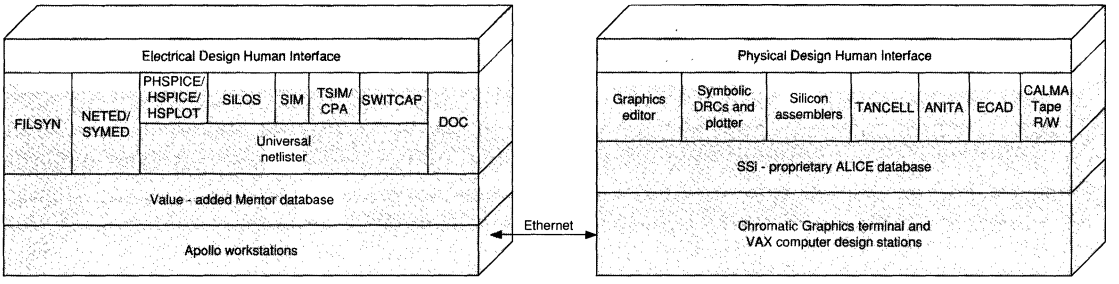


CONVERT SEMI-CUSTOM DESIGN INTO FULL-CUSTOM DESIGN

With its unique integrated design automation system, SSi can easily convert a semicustom design into full-custom circuitry. This capability allows SSi's customers to reduce production costs by converting an area-inefficient semicustom design into a high-performance full-custom design.

SOPHISTICATED DESIGN AUTOMATION TOOLS

The IDM™ design automation system, with proprietary and SSi-enhanced vendor software, addresses both the electrical and physical phases of design.



FILSYN: Filter circuit synthesizer
NETED/SYMED: Schematic editors
PHSPICE: HSPICE pre-processor
HSPICE: A/D circuit
HSPLOT: HSPICE graphic plotter
SILOS: Logic and fault simulator
SIM: Digital logic simulator
TSIM: Timing simulation preprocessor

CPA: Circuit path analyzer
SWITCAP: Switched-capacitor simulator
DOC: Document editor
TANCELL: Automatic placer and router
ANITA: Automated network intertrace algorithm
ECAD: Design rules checks and pattern generation
ALICE: Automated layout for IC engineering

ELECTRICAL DESIGN

Electrical design is done on Mentor Graphics/Apollo engineering workstations with SSi-enhanced software that provides schematic capture, simulation, synthesis, and documentation tools. This software is supported by libraries of pre-designed cells and components. Due to our integrated CAE environment, there is no distinction between any schematic capture, simulation, or synthesis capabilities for full- or semicustom design approaches.

ANALOG AND DIGITAL SIMULATION

Simulation ensures that we meet the customer's performance specification before converting the design into silicon. Circuit simulation, an important key to SSi's design methodology, allows us to accurately simulate the performance numbers of our technologies. For circuit simulation, we use Meta-Software's HSPICE™ with a proprietary analog CMOS model that accurately predicts output impedance and other analog parameters over a wide range of operating conditions and device sizes. The HSPICE environment includes a fully hierarchical netlister, a preprocessor called PHSPICE, and a Meta-Software graphic plotter called HSPLOT™. For the analog simulation of switched capacitors, we use Columbia University's SWITCAP™.

For digital simulation, we use a proprietary version of SimuCad's SILOS™ that performs gate and switch-level, zero-delay, functional logic and fault simulation. To analyze delays with a timing-based logic simulation, we use a combination of TSIM™ (developed on Meta-Software's Circuit Path Finder™) and SILOS.

DEVICE MODELING AND CHARACTERIZATION LABORATORY

Highly-accurate circuit simulation models and parameters are developed in SSi's state-of-the-art Device Modeling and Characterization (DMC) laboratory. With capabilities including precision AC measurement, RS1 statistical analysis, and worst-case modeling, the DMC lab provides complete device model data for our processes.

PHYSICAL DESIGN

Physical design is done on Chromatics Graphics terminal/VAX computer design stations. Our proprietary, VAX-based program called ALICE™ (Automated Layout for Integrated Circuit Engineering) with other SSi-enhanced vendor software is used for graphical editing, digitizing, design rules checking (DRC), circuit tracing, and pattern generation (PG).

AUTOMATIC PLACE AND ROUTE SOFTWARE

SSi's cell-based automatic place-and-route capability, which is based on Tangent's TANCELL™, performs physical design far more rapidly than can be done by hand. Extensive proprietary software, developed to complement TANCELL, supports hierarchical routing, parameter passing, library creation and maintenance, and CMOS switched-capacitor analog macro generation directly from full-custom design. A random-logic digital macro assembler is in develooment. This flexible place-and-route environment supports floorplanning, automatic chip construction, and the mix and match of custom cells, standard cells, and compiled cells—all of which are used to reduce design development time.

AUTOMATIC CIRCUIT TRACE AND VERIFICATION SOFTWARE

Using a proprietary circuit-trace program called ANITA™, we compare the completed IC layout database automatically to the Mentor schematic database to ensure that the layout implementation matches the schematic design exactly. When this trace program is applied to CMOS and bipolar mixed analog/digital designs, it performs a more detailed trace than is available through commercial layout-versus-schematic (LVS) packages. ANITA allows SSi to dramatically reduce design errors and minimize the time to product introduction.

DESIGN AUTOMATION BENEFITS

The proprietary IDM Design Automation system gives Silicon Systems the flexibility to create increasingly complex ASIC designs for our customers while dramatically reducing design schedules, costs, and errors.

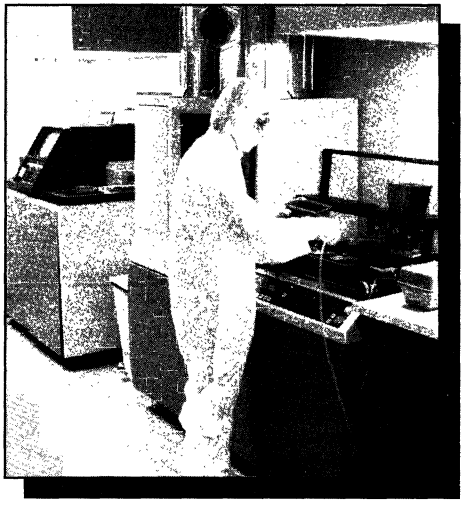
MANUFACTURING SUPPORTS BOTH CMOS AND BIPOLAR TECHNOLOGIES

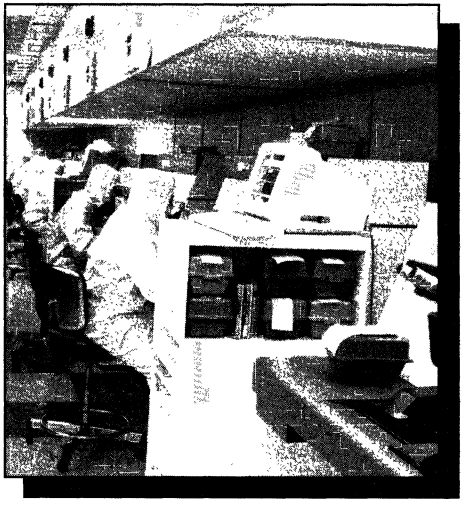
Silicon Systems is known in the ASIC industry for its commitment to producing standard and custom ASICs using a broad range of CMOS and bipolar process technologies.

SSi continually invests in quality and capacity improvements to ensure that the company's wafer fabrication, test, and assembly capabilities meet the latest manufacturing requirements. For special functional capabilities (i.e., increased speed, bandwidths, response times, etc.), SSi's 4-inch wafer fabrication facilities use sophisticated process techniques such as:

- Stepper and projection photolithography for high resolution.
- Positive resist and dry plasma etch for smaller feature size and minimal undercutting.
- And high-current ion implantation and automated sputtering, which are used to improve productivity.

SSi can also meet a wide spectrum of assembly and packaging needs. Quick-turn, low-volume assembly for prototypes is done in SSi's Tustin facility. High-volume production of plastic packages in any of DIP, PLCC, or SO configurations is done in Silicon Systems' Singapore Technology Center.





COMPUTER-AIDED MANUFACTURING WITH PROMIS ™ *FOR RAPID DELIVERY OF RELIABLE ICs*

Committed to Computer-Aided Manufacturing (CAM), Silicon Systems has invested in extensive computer resources. To handle the vast amounts of data required for manufacturing, monitoring, and statistical process control, SSi uses the Process and Management Information System (PROMIS™). The PROMIS system:

- manages inventory information,
- tracks wafers in process,
- monitors the clean room environment, and
- performs statistical process control.

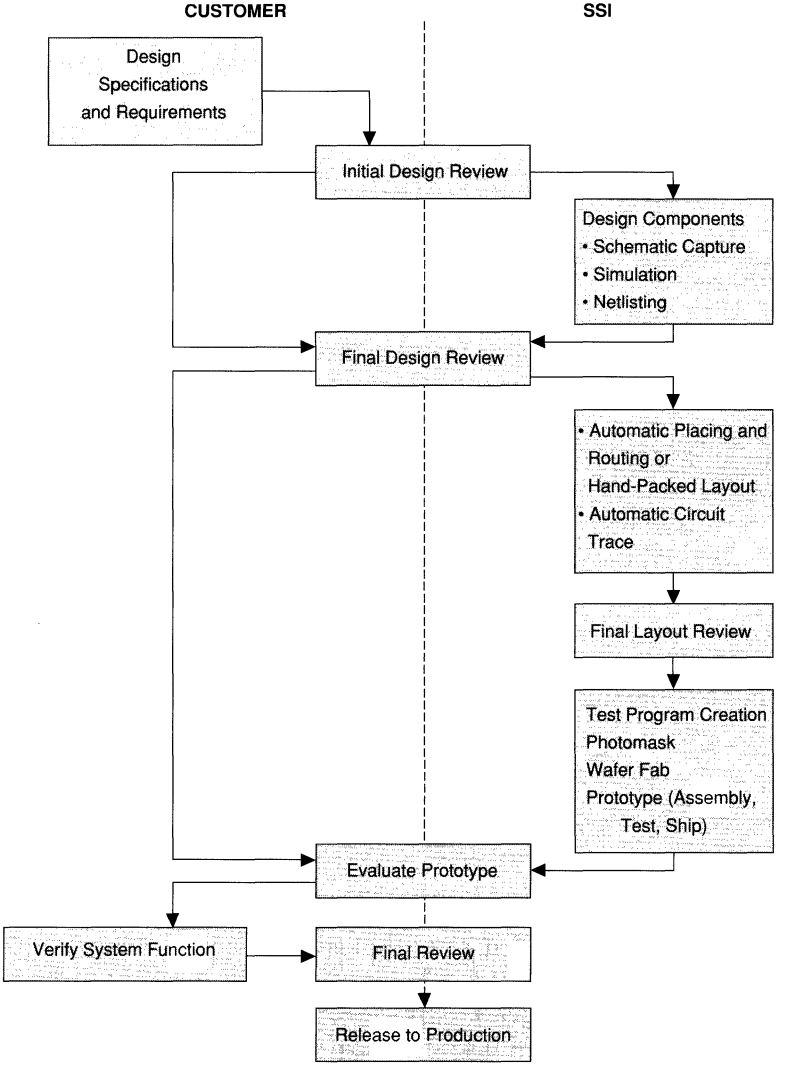
PROMIS provides computer-controlled (i.e., paperless) facilities, which reduces sources of contamination in the wafer fab clean rooms. SSi's wafer fab is a class "50" environment with class "10" work surfaces. Cleanliness is maintained through the service chase approach, which channels a minimum of 5 air exchanges per minute.

PROMIS allows Silicon Systems to deliver reliable ICs rapidly, thus allowing customers to introduce products to the marketplace on schedule and within budget.

SSi WORKS WITH CUSTOMERS TO CREATE THE BEST IC SOLUTION

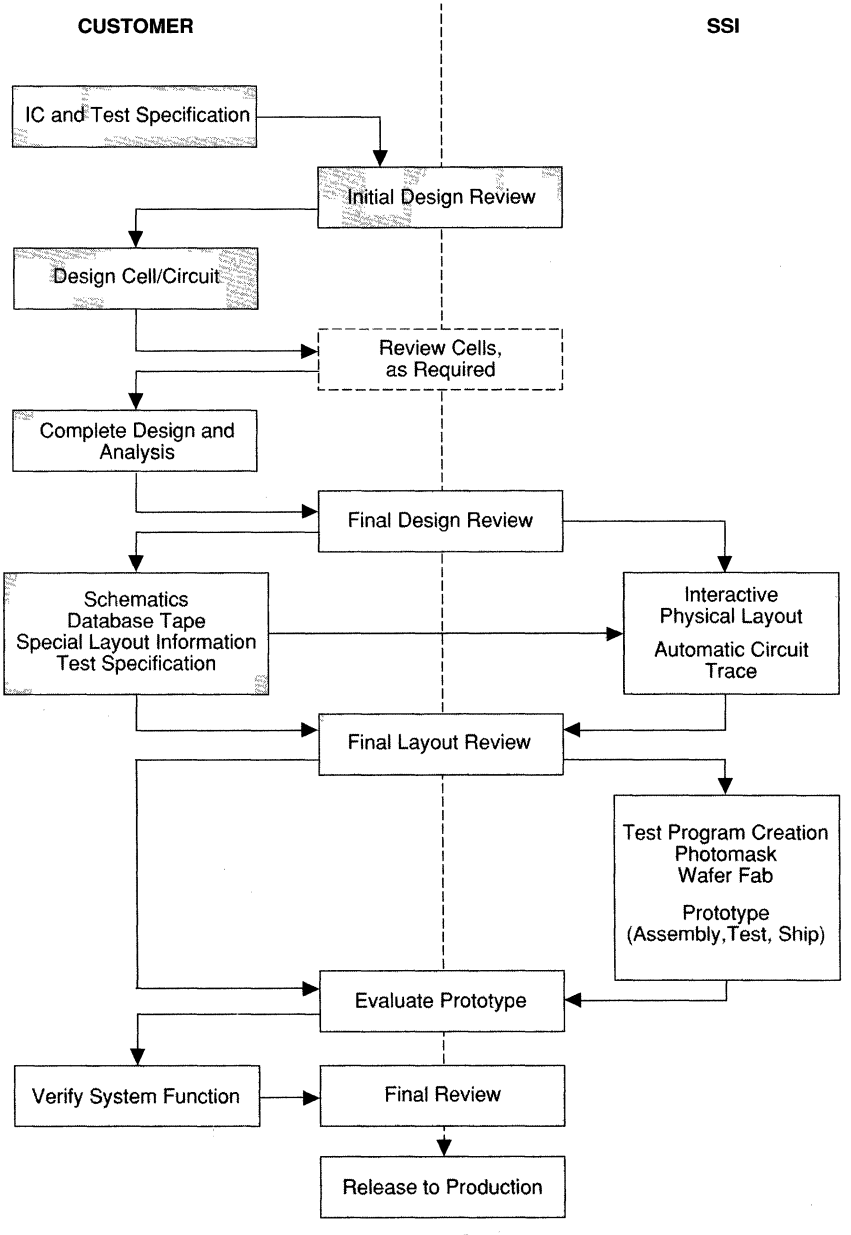
SSi has three IC design centers located in Tustin, California; Grass Valley, California; and Singapore. An additional center in Silicon Valley will open by late 1988. Any of these design centers can accept a functional specification and complete the entire design task using either a full-custom or a cell-based approach.

CUSTOMER INTERFACE FOR FULL-CUSTOM AND CELL-BASED DESIGNS



Or, a customer can complete most of the design, using array technology, and utilize SSi's expertise for physical layout.

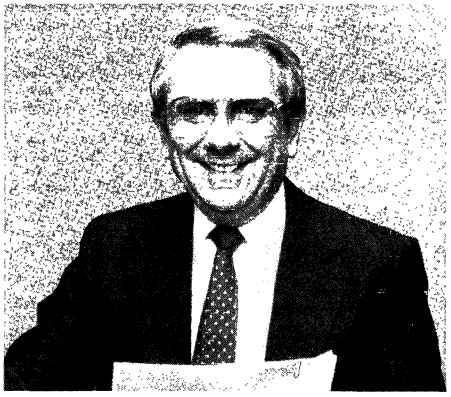
CUSTOMER INTERFACE FOR ARRAY-BASED DESIGNS



Section 10

QUALITY ASSURANCE AND RELIABILITY

TABLE OF CONTENTS



CARMELO J. SANTORO
Chairman, President & CEO

SECTION 1

A MESSAGE FROM SILICON SYSTEMS' PRESIDENT AND CEO

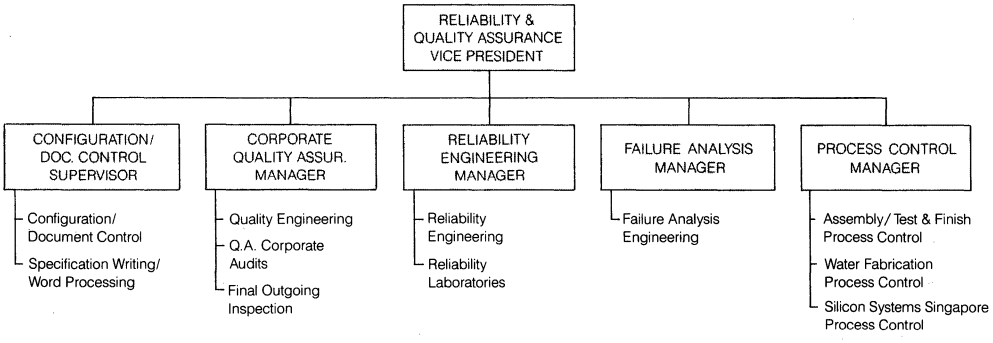
Quality is the secret to long term success. It literally overshadows the short term emphasis on price, delivery, or any other measure of performance.

At Silicon Systems, we have based our quality philosophy on the development of a "state of mind" in each employee, related to job performance and to its reflection in the overall level of quality and reliability of our product.

You won't hear very many cliches about quality in our environment. But we do strive for "zero defects" for "just in time service" and for "doing it right the first time." We think constant reminders of tired phrases can serve more as an irritant than a stimulant. Our quality ethic is based on setting examples for others and by intuitive "high quality" job performance propagating the quality ethic throughout the organization to each employee.

To be sure, we have programs related to quality and reliability. They are the subject of this brochure. We are dedicated to process control, overall product reliability and outstanding outgoing quality. Rapid analysis of failures and returns providing responsive service to our customers also generates quick solutions to our own problems. We believe that the high levels which we achieve in quality, reliability and

FIGURE 1.1 ORGANIZATION CHART



service are directly attributable to belief in the basic tenets of quality within our corporate culture.

1.1 INTRODUCTION

This brochure presents the basic quality and reliability philosophy used by Silicon Systems.

Silicon Systems' management philosophy is the manufacture of a quality product consistent with company policy and customer requirements. It is the goal of the Quality Assurance and Reliability departments to ensure that these requirements are met.

Included in this brochure is Silicon Systems' ongoing program for controlling and improving the quality of devices manufactured.

The data clearly illustrates that Silicon Systems is working diligently to maintain its position as a leader in the industry. The use of highly specialized equipment, test programs and test procedures allows us to determine product reliability under extreme conditions.

Quality is built into Silicon Systems' parts from rigid incoming inspection of piece parts and materials to stringent outgoing quality verification. The assembly process flow is encompassed by an elaborate system of test and inspection gates and in-line monitors. These gates and monitors ensure a step-by-step adherence to prescribed procedure.

In addition, Silicon Systems is also incorporating statistical process control into our manufacturing operations. This approach of studying and improving the quality of processes, products and services by the use of statistical problem solving techniques, analytical controls and quantitative methods ensures that Silicon Systems' products maintain a high level of quality and reliability. Our quality organization is committed to working closely with you to provide continuously improved incoming quality levels.

1.2 QUALITY ASSURANCE AND RELIABILITY

The quality of a semiconductor device is defined by its conformance to specification; the reliability of a semiconductor device is defined by how well it continues to conform to specification over time while under stress. This relationship between quality and reliabiiity requires a program that encompasses both. Included in this brochure are outlines of our process control program and our PPM (parts-per-million) program. These programs assure conformance to specification throughout the manufacturing process.

1.2.1 Organization Philosophy

To facilitate the close cooperation and coordination required of the Quality and Reliability functions, a combined organization has been established. This organization must have access to and support from the top of the organization. The R. & Q.A. organization is shown in Figure 1.1.

SECTION 2 QUALITY ASSURANCE

2.1 QUALITY PROGRAM

Quality Assurance has the ultimate responsiblity for the reliable performance of our products. This is accomplished through the administration of formal systems which assure that our products meet the requirements of customer purchase orders, and specifications for design, from raw materials through finished product.

Quality Assurance supports formal qualifications of suppliers, materials, processes, and products; administration of system and production monitors to assure that our products do meet the desired specifications; and the liaison between Silicon Systems and the customer for all product-related problems.

It is the practice of Silicon Systems to have the Quality and Reliability Program encompass all of its activities, starting with a strong commitment of support for the program from the corporate level, and continuing with customer support after the product has been shipped.

Silicon Systems firmly believes that quality must be "built into" all of its products by ensuring that employees are trained in the quality philosophy of the company. Some of the features built into Silicon Systems' Quality Program include:

1. Structured training programs directed at Wafer Fabrication, Test, and Process Control personnel.
2. Stringent in-process inspection gates and monitors.
3. Total evaluation of designs, materials, and processing procedures.
4. Stringent electrical testing (100% and redundant QA AQL testing).
5. Ongoing reliability monitors and process verifications.
6. Real time use of statistical process control methodology.
7. Corporate level audits of manufacturing, subcontractors, and suppliers.

These structured quality methods result in products which deliver superior performance in the field.

2.1.1 Lot Acceptance Testing

At Silicon Systems, all sampling for Lot Acceptance Testing is based upon MIL-STD-105D.

1. Commercial Testing includes resistance to solvents, Solution A, plus external Visual Inspection to strict SSi standards.

2. Industrial Testing includes hermetic-only Destructive Physical Analysis (DPA), as well as Resistance to Solvents, Solutions A and B, plus Solderability, Electrical @ 25°C, and external Visual Inspection to SSi standards.

3. Extended Reliability covers hermetic-only DPA and Burn-in, as well as Resistance to Solvents, Solutions A, B, and C, plus Solderability, Fine and Gross Leak Hermeticity, Electrical @ 25°C, and external Visual Inspection to SSi standards.

4. High Reliability includes Destructive Physical Analysis and Burn-in, as well as Resistance to Solvents, Solutions A, B, C, and D, plus Solderability, Fine and Gross Leak Hermeticity, Electrical @ max/min temperature limits as well as 25°C, and external Visual Inspection to SSi standards.

2.2 PROCESS CONTROL

Silicon Systems' process control program is designed to provide continuous visibility of the performance of manufacturing processes and ensures that corrective action is taken before problems develop.

The principal areas of process control which assess the quality of processed product against quality standards are incoming materials inspection and process control monitoring.

2.2.1 Incoming Inspections

Incoming inspection plays a very important role in Silicon Systems' quality program. Small deviations from material specifications can transverse the entire production cycle before being detected by outgoing quality control. By paying strict attention to quality at this early stage, the possibility of failures occurring further down the line is greatly minimized.

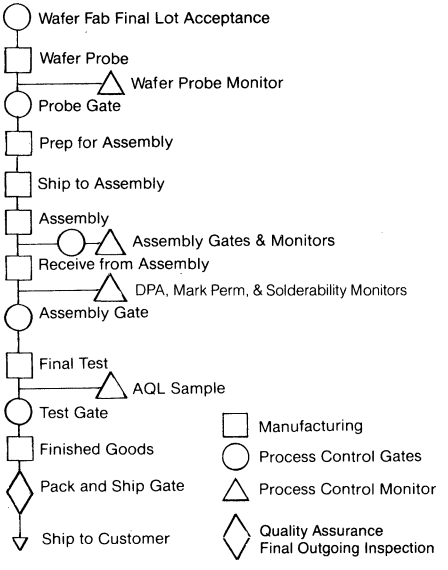
2.2.2 In-Process Inspections

Every major manufacturing step is followed by an appropriate in-process quality control inspection gate. Silicon Systems has established inspection gates in areas such as Wafer Fabrication, Wafer Probe, Assembly, and Final Test areas.

In addition to these established gates, Silicon Systems also has established monitors during various stages in the manufacturing process. It is this built-in quality that ensures failure-free shipment of Silicon Systems' products.

Quality control monitors have been placed throughout the manufacturing flow, so that data may be collected and analyzed to verify the results of intermediate manufacturing steps. This data is used to determine quality trends or long term changes in the quality of specific operations. A general description of the product flow and QC inspection points are shown in Figure 2.1.

FIGURE 2.1
PROCESS CONTROL GATES AND MONITORS



2.3 PPM PROGRAM

The main purpose of employing a PPM program is to eliminate defects. The action portion of this program is accomplished in three stages:

1. Identify all defects by failure mode.
2. Identify defect causes and initiate corrective action.
3. Measure results and set improved goals.

The data generated from an established PPM program is statistically compiled as a ratio of units rejected/tested. This ratio is then expressed in terms of parts per million (PPM) with a confidence

limit attached. The eventual reported PPM result therefore allows proper significance to be attached to every defect found. The final aim or goal is to achieve and maintain zero defects.

Based on significantly large volumes of PPM data and an established five-year strategic plan identifying industry-wide competitive PPM goals, Silicon Systems has progressively achieved excellent quality standards and will continue to measure the results and, therefore, improve on PPM standards as set by the industry.

2.4 COMPUTER AIDED MANUFACTURING CONTROL

Computer Aided Manufacturing (CAM) requires the identification, control, collection and dissemination of vast amounts of data for logistics control. Silicon Systems uses this type of computerized system for statistical process control and manufacturing monitoring.

PROMIS (Process Management and Information System) displays document control-released recipes, processes, and procedures, tracks work-in-process, contains accurate inventory information, allows continuous recording of facilities data, contains performance analysis capabilities, and much more. PROMIS allows for a paperless facility, which assists in keeping contamination out of the wafer fab clean room.

The configuration of PROMIS has been tailored to meet the requirements of Silicon Systems.

SECTION 3 RELIABILITY

3.1 RELIABILITY PROGRAM

Silicon Systems has defined various programs that will continuously characterize product reliability levels. These programs are categorically described as:

1. Qualifications
2. Production monitors
3. Evaluations
4. Failure analysis
5. Data collection and presentation for improvement projects

3.2 QUALIFICATIONS

The application of this program ensures that all new product designs, processes, and packaging meet the absolute maximum rated design and worst case end use criteria. The large data base generated by means of the accelerated stress testing results in a maximum confidence for determining the final use in the production environment.

3.3 PRODUCTION MONITORS

This program has been established to randomly select from production a statistically significant sample and subject it to the maximum stress test levels to determine useful life of the product in a field use environment.

The following pages show reliability methods that are in use at Silicon Systems. The importance of production monitors at Silicon Systems does, in effect, assure continued reliability.

3.4 EVALUATIONS

The evaluation program at Silicon Systems is an ongoing program that will continue defining standards which cover the reliability assessment of the circuit portion, process parameters, and packaging of a new product. This program continuously provides performance characteristics of the products that are part of the improvement projects at Silicon Systems.

3.5 FAILURE ANALYSIS

The failure analysis program is an integral part of the Reliability Department at Silicon Systems. Being aware of the low defect density requirements in the industry along with the needed competitive edge, Silicon Systems has formed a highly technical and sophisticated failure analysis laboratory. This laboratory provides visual analysis, electrical reject mode analysis, and both destructive and non-destructive data to aid the engineers in their corrective action for improvement programs, and to help our customers implement improved field use designs. This may include metallurgical, optical, chemical, electrical and SEM with X-ray dispersive analysis as needed.

Conclusively, this in-house testing and analysis allows Silicon Systems to monitor all aspects of manufacturing to ensure that a product of highest quality is shipped to our customers.

3.6 DATA COLLECTION & PRESENTATION FOR IMPROVEMENT PROJECTS

Data is collected from each of the above programs and summarized for ease of understanding among all engineering disciplines in the company. This data facilitates improvement and provides our customers an opportunity to review our product performance.

3.7 RELIABILITY METHODS

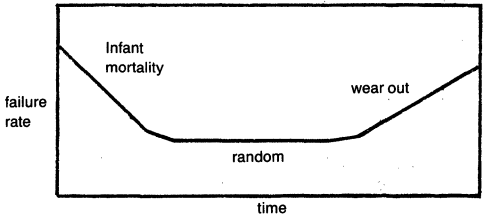
The Reliability Program utilizes various stress tests that are presently being used to define performance levels of our products. Many of these stress tests are per MIL-STD. 883C as shown on following page.

TABLE 3.1 RELIABILITY STRESS TESTS

TEST	CONDITIONS	PURPOSE OF EVALUATION
Biased temperature/humidity	85°C/85°%RH	Resistance to high humidity with bias
High temperature operating life	Mil 883C Method 1005	Resistance to electrical and thermal stress
Highly accelerated stress test	SSi Method	Evaluates package integrity
Steam pressure	121°C/15PSI	Resistance to high humidity
Temperature cycling	Mil 883C Method 1010	Resistance to thermal excursion (air)
Thermal shock	Mil 883C Method 1011	Resistance to thermal excursion (liquid)
Salt atmosphere	Mil 883C Method 1009	Resistance to corrosive environment
Constant acceleration	Mil 883C Method 2001	Resistance to constant acceleration
Mechanical shock	Mil 883C Method 2002	Resistance to mechanical shocks
Solderability	Mil 883C Method 2003	Evaluates solderability of leads
Lead integrity	Mil 883C Method 2004	Evaluates lead integrity before board assembly
Vibration, variable frequency	Mil 883C Method 2007	Resistance to vibration
Thermal resistance	Method—SSi	Evaluates thermal dissipation
Electrostatic damage	Method 3015	Evaluates ESD susceptibility
Latch-up	SSi Method	Evaluates latch-up susceptibility
Seal fine and gross leak	Mil Std 883C Method 1014	Evaluates hermeticity of sealed packages

3.8 RELIABILITY PREDICTION METHODOLOGY

It has been known in reliability engineering principles that the failure rate of a group of devices as a function of time will follow a life curve as shown below:



The bath tub curve above, implies that the useful life of the product extends until some basic design limitation is experienced. At SSi the Arrhenius Model is used to extrapolate a failure rate at an accelerated temperature test condition to a normal use temperature condition.

The model basically states $R = A\, e^{-Ea/KT}$

where R = Reaction rate

A = Constant

E_a = Activation energy (eV)

K = Boltzmann's constant 8.63×10^{-5} eV/°K

T = Absolute temperature (°K)

SECTION 4 ELECTROSTATIC DISCHARGE PROGRAM

4.1 ESD PREVENTION

Silicon Systems recognizes that procedures for the protection of Electrostatic Discharge (ESD) sensitive devices from damage by electrical transients and static electricity must be incorporated throughout all operations which come in contact with these devices.

Silicon Systems' quality program incorporates various protection measures for the control of ESD. Some of these preventive measures include handling of parts at static safe-guarded work stations; the wearing of wrist straps during all handling operations; the use of conductive lab coats in all test areas and areas which handle parts; and the packaging of components in conductive and anti-static containers.

Section 11

PACKAGING/ ORDERING INFORMATION

SSi PACKAGING INDEX

*SON is a 150 mil width package.
**SOL is a 300 mil width package.
***SOW is a 400 mil width package.

SSi PACKAGING MATRIX

Package Type	8	10	14	16	18	20	22	24	28	32	34	40	44	52	68
Plastic DIP															
300 mil	X		X	X	X	X		S							
400 mil							X								
600 mil								X	X	X		X			
Cerdip															
300 mil	X		X	X	X	X									
400 mil							X								
600 mil								X	X			X			
Side Braze															
300 mil	X		X	X	X	X		S							
400 mil							X								
600 mil								X	X			X			
Small Outline															
150 mil	X		X	X											
300 mil				X		X		X	X		X				
400 mil										X					
Flatpack		X	X					X	X	X					
Chip Carrier				X		X			X						
Plastic Quad									X				X	X	X
Ceramic Quad									X				X		X

MICROPERIPHERAL PRODUCTS PACKAGE TYPES

DEVICE TYPE	PACKAGE TYPE			
	P Plastic	F Flatpack	H PLCC	N L W Small Outline
SSI 32B450A			52	
SSI 32B451			44	
SSI 32B545	40		44	
SSI 32C452	40		44	
SSI 32C452A	40		44	
SSI 32C453	40		44	
SSI 32D531	24		28	
SSI 32D5321	28		28	
SSI 32D534	28		28	
SSI 32D535	32			32W
SSI 32D536	28		28	
SSI 32H101A/1012A	8			8N
SSI 32H116/1162	8	10		8N
SSI 32H523R				14N
SSI 32H566R				14N
SSI 32H567	28		28	
SSI 32H568	32		44	
SSI 32H569	20			20L
SSI 32M5901	8			
SSI 32M5902	14			16L
SSI 32M591	16			16L
SSI 32M593	20			20L
SSI 32M594	20			20L
SSI 32P540	28		28	
SSI 32P541	24		28	24L
SSI 32P544			44	
SSI 32P546				32W
SSI 32R104C		24		24L
SSI 32R104CL		24		
SSI 32R104CM				24L
SSI 32R108	24			
SSI 32R114		24		
SSI 32R115-2	18			
SSI 32R115-4	22			
SSI 32R115-5	24	24	28	24L
SSI 32R117/117R-2	18			
SSI 32R117/117R-4	22	24		24L
SSI 32R117/117R-6	28	28	28	28L

(Continued)

MICROPERIPHERAL PRODUCTS PACKAGE TYPES (Cont.)

DEVICE TYPE	PACKAGE TYPE			
	P Plastic	F Flatpack	H PLCC	N L W Small Outline
SSI 32R117A/117AR-2	18			
SSI 32R117A/117AR-4	22	24		24L
SSI 32R117A/117AR-6	28	28	28	28L
SSI 32R122	22			
SSI 32R188		24		
SSI 32R501/501R-4				24L
SSI 32R501/501R-6	28	28	28	28L
SSI 32R501/501R-8	40	32	44	32W
SSI 32R510A/510AR-2	18			20L
SSI 32R510A/510AR-4	22	24		24L
SSI 32R510A/510AR-6	28	28	28	28L
SSI 32R511/511R-4				24L
SSI 32R511/511R-6			28	28L
SSI 32R511/511R-8	40	32	44	32W
SSI 32R511M/511RM-6				28L
SSI 32R511M/511RM-8				32W
SSI 32R512/512R-8				32W
SSI 32R512/512R-9				34L
SSI 32R512M/512RM-8				32W
SSI 32R512M/512RM-9				34L
SSI 32R514/514R-2				18L
SSI 32R514/514R-4				24L
SSI 32R514/514R-6			28	28L
SSI 32R515/515R-9				34L
SSI 32R515/515R-10			44	
SSI 32R515M/515RM-9				34L
SSI 32R520/520R		24		
SSI 32R521/521R		28	28	28L
SSI 32R522/522R-4		24		
SSI 32R522/522R-6			28	28L
SSI 32R524R/524RM				32W, 34L
SSI 32R525R		24		24L
SSI 34B580	28		28	
SSI 34D441	28		28	
SSI 34P570	28		28	
SSI 34R575-2	18			
SSI 34R575-4	24			
SSI 35P550	40		44	

STANDARD PRODUCT MARKETING NUMBER DEFINITION

NNA NNNN A AA - N A A

(R) = REQUIRED
(O) = OPTIONAL

PRODUCT CATEGORY (R)

32B	HDD INTERFACE
32C	HDD CONTROLLER
32D	HDD DATA RECOVERY
32H	HDD HEAD POSITIONING
32M	HDD MOTOR SPEED CONTROLLER
32P	HDD PULSE DETECTION
32R	HDD READ/WRITE AMP
34B	FDD INTERFACE
34D	FDD DATA RECOVERY
34P	FDD PULSE DETECTION
34R	FDD READ/WRITE AMP
35P	TAPE DRIVE PULSE DETECTION
73D	MODEM DEVICE SET
73K	K-SERIES MODEM
73M	MODEM/MODEM SUPPORT
75T	TONE SIGNALING
78P	DIGITAL TELECOM
78A	ANALOG TELECOM

DEVICE TYPE (R)
3 OR 4 DIGITS

RELEASE LEVEL (0)
(REVISION)
A THROUGH E

NUMBER OF CHANNELS (0)

MODIFIERS (O)

J	BURN - IN (168 HOURS)
K	BURN - IN (48 HOURS)
LJ	LOW NOISE BURN - IN (168 HOURS)
L	LOW POWER
LN	LOW NOISE
LQ	LOW NOISE, RESISTOR, MIRROR IMAGE
LR	LOW NOISE, RESISTOR
M	MIRROR IMAGE
S	SERIAL VERSION
SL	LOW POWER SERIAL
R	DAMPING RESISTOR
RM	RESISTOR, MIRROR IMAGE
U	ON - CHIP UART

CANNOT USE A THROUGH E IN LEFT POSITION

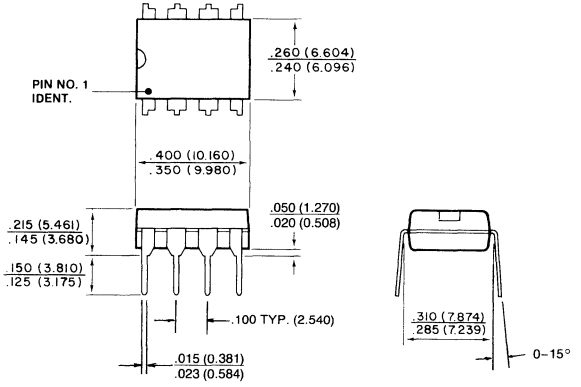
PACKAGE TYPE (R)

C	SIDE-BRAZED CERAMIC
D	CERAMIC DIP
F	FLAT PACK
H	PLCC
P	PLASTIC DIP
T	METAL CAN
S	PLASTIC, SKINNY DIP
N	SMALL OUTLINE, NARROW (150 MIL.)
L	SMALL OUTLINE, LARGE (300 MIL.)
W	SMALL OUTLINE, WIDE (400 MIL.)

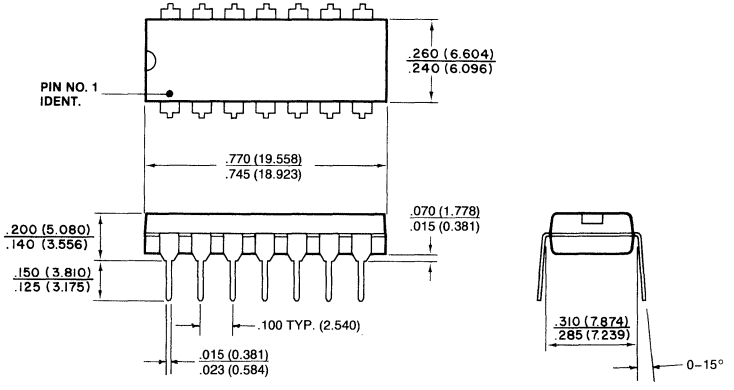
TEMPERATURE RANGE (O)

C	COMMERCIAL (0 °C to +70 °C)
I	INDUSTRIAL (-40 °C to +85 °C)
M	MILITARY (-55 °C to 125 °C)

PLASTIC DIP
8 Pins

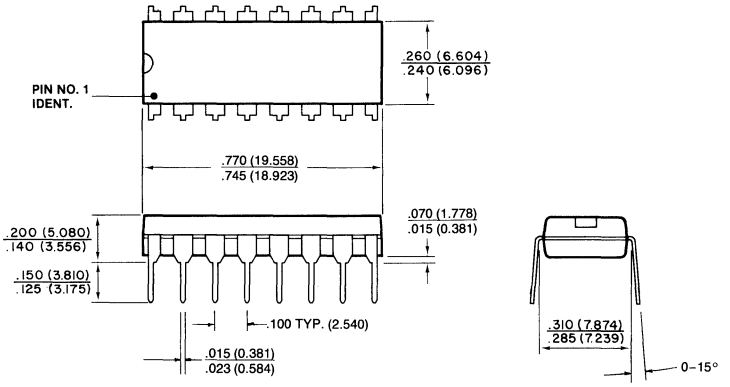


PLASTIC DIP
14 Pins

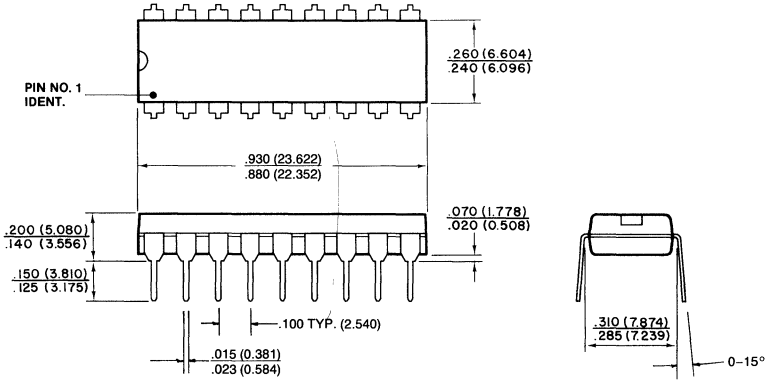


11

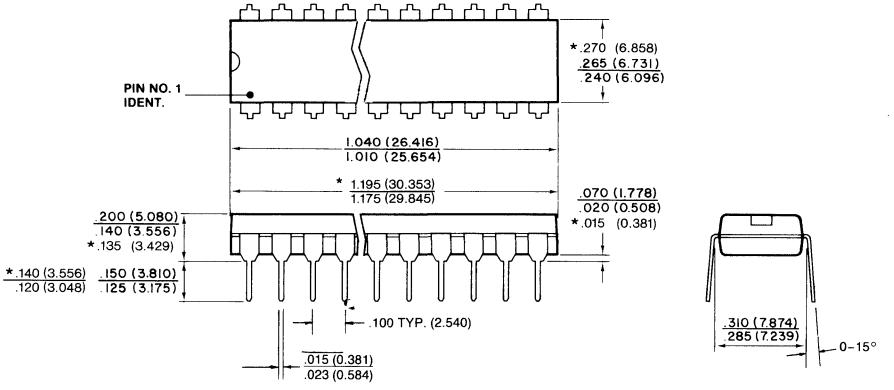
PLASTIC DIP
16 Pins



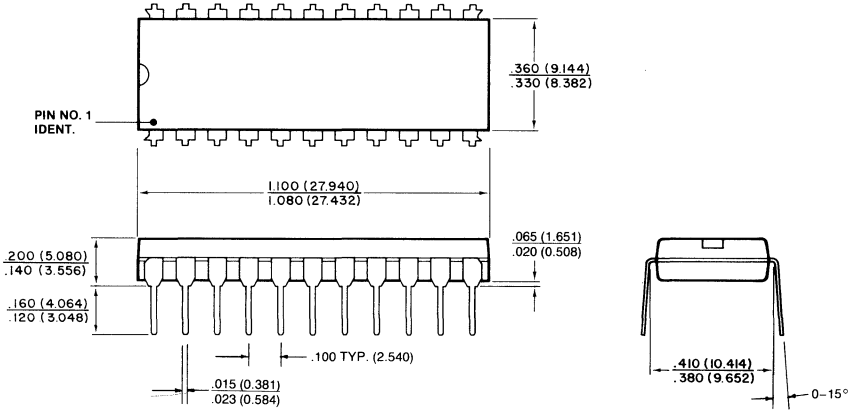
PLASTIC DIP
18 Pins



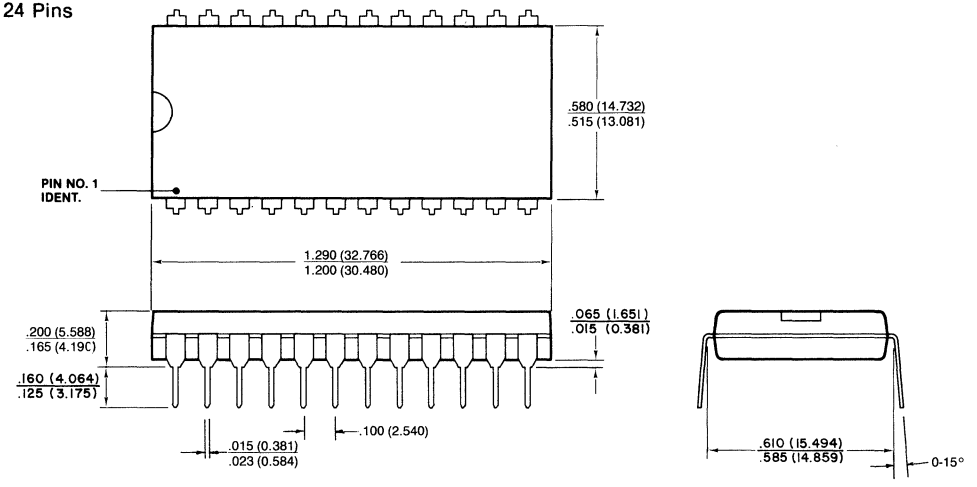
PLASTIC DIP
20 Pins
24 Pins*



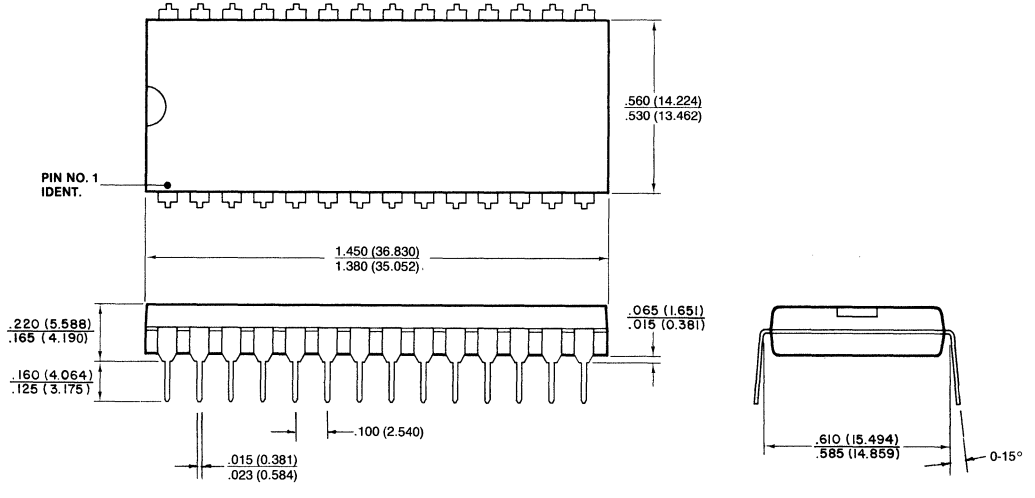
PLASTIC DIP
22 Pins



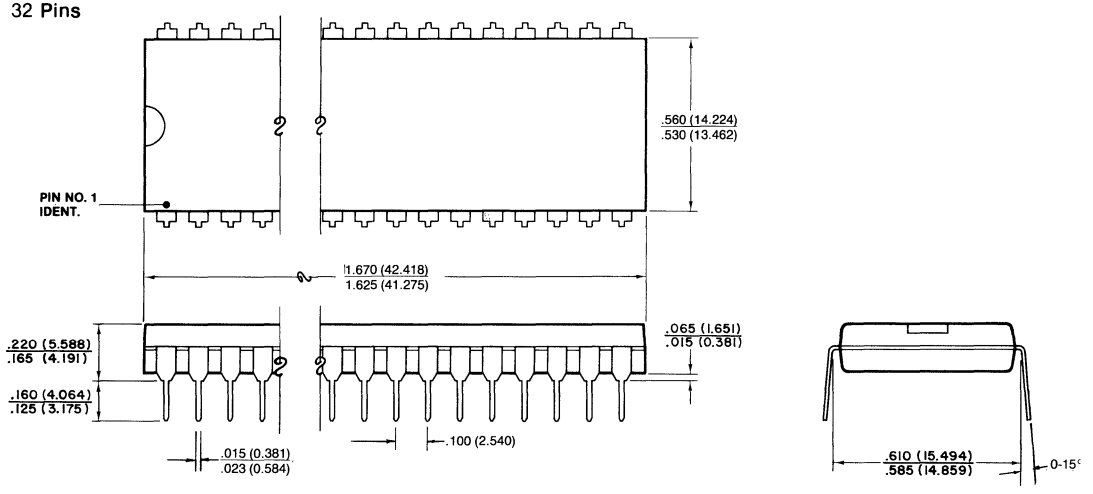
PLASTIC DIP
24 Pins



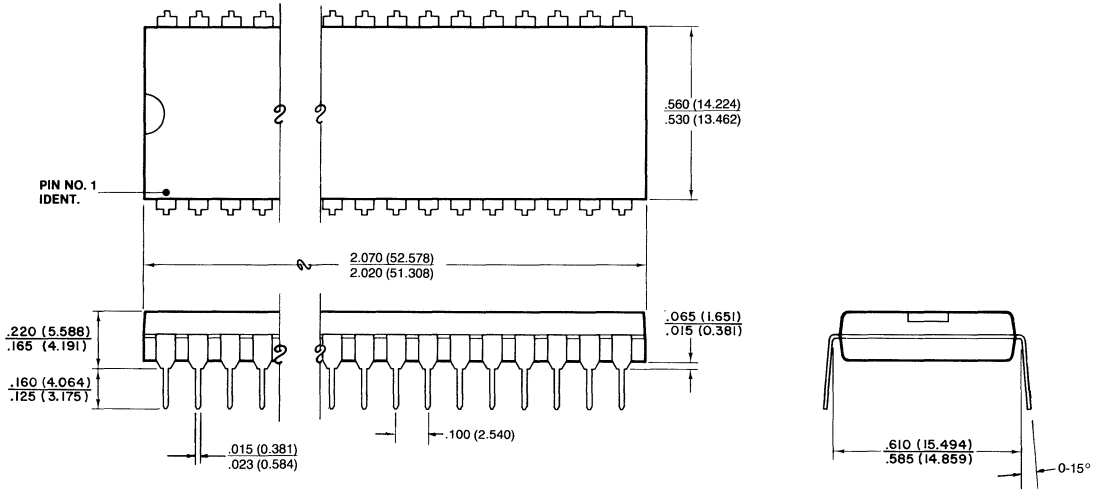
PLASTIC DIP
28 Pins



PLASTIC DIP
32 Pins

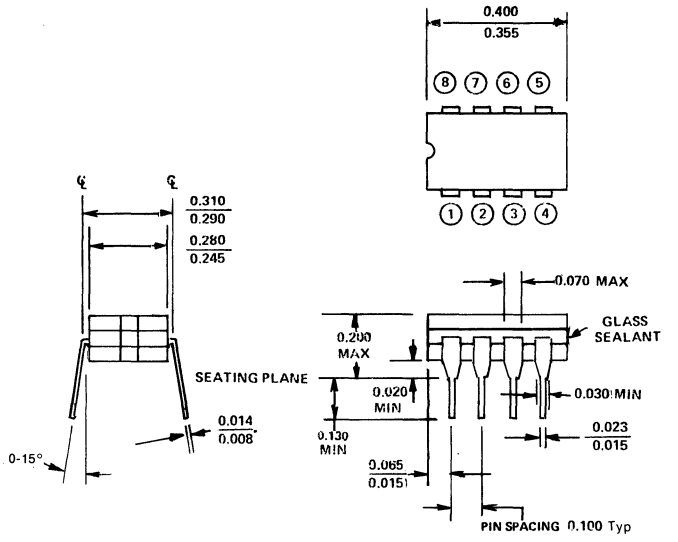


PLASTIC DIP
40 Pins

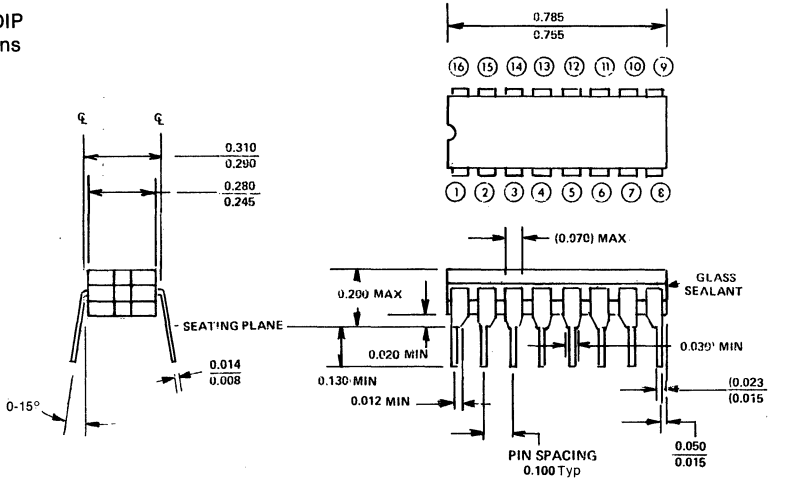


11

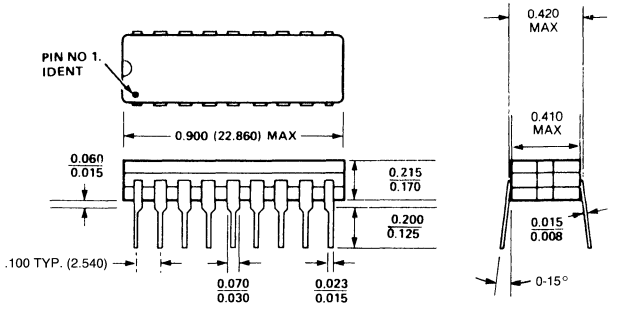
CERDIP
8 Pins



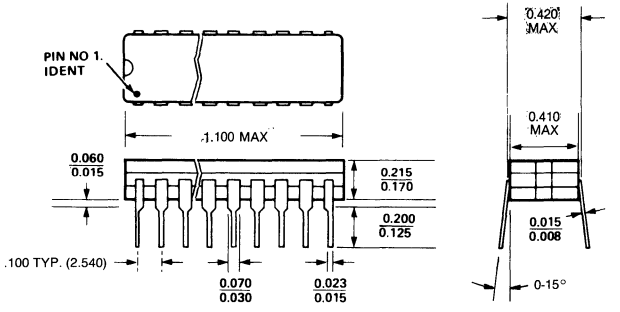
CERDIP
16 Pins



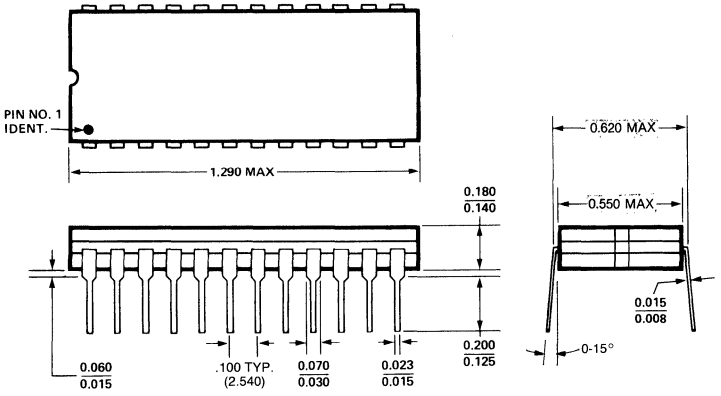
CERDIP
18 Pins



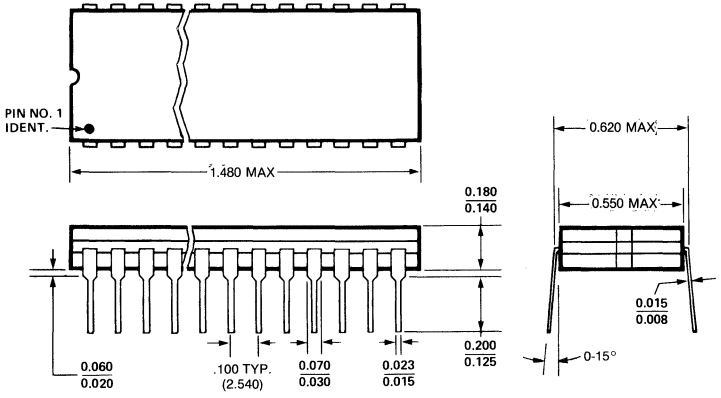
CERDIP
22 Pins



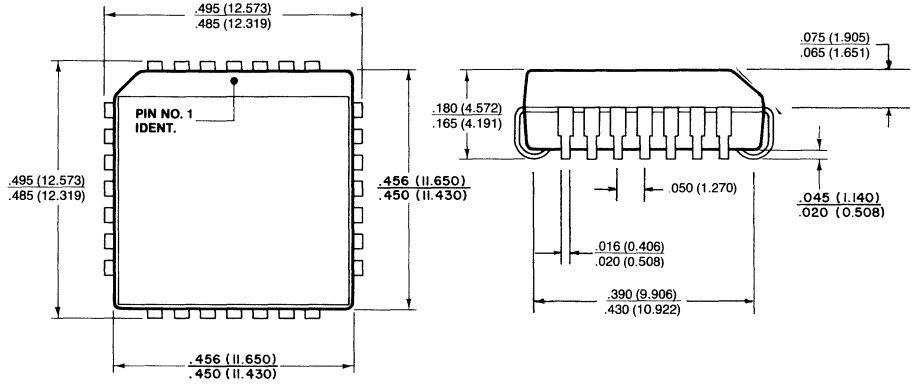
CERDIP
24 Pins



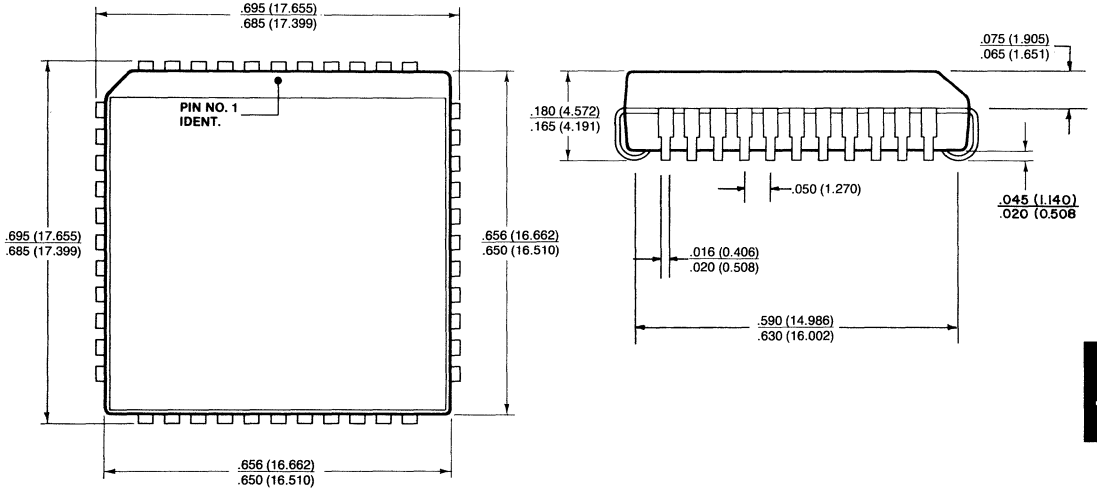
CERDIP
28 Pins



SURFACE MOUNTED
QUAD (PLCC)
28 Leads

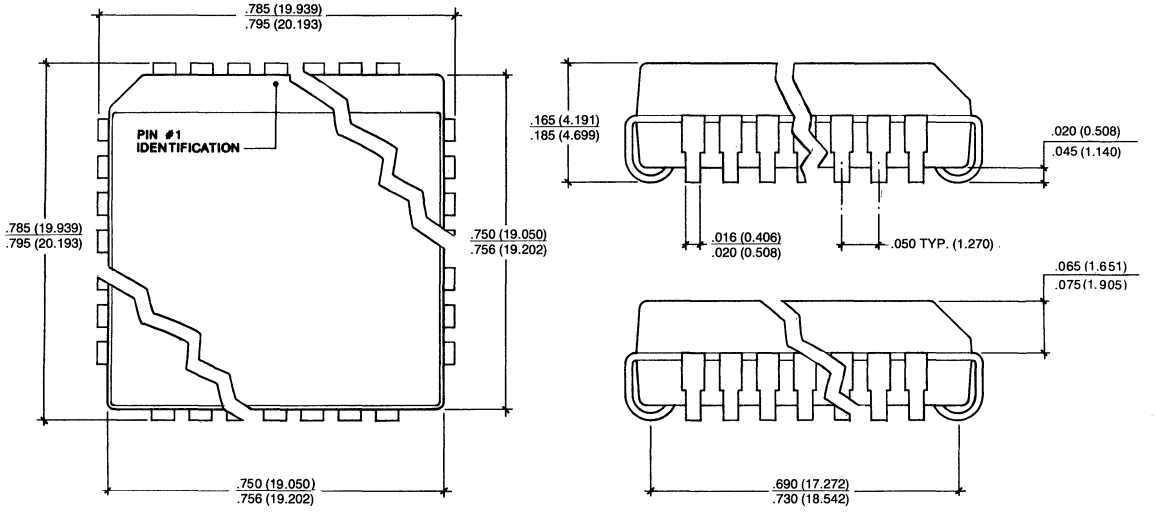


SURFACE MOUNTED
QUAD (PLCC)
44 Leads

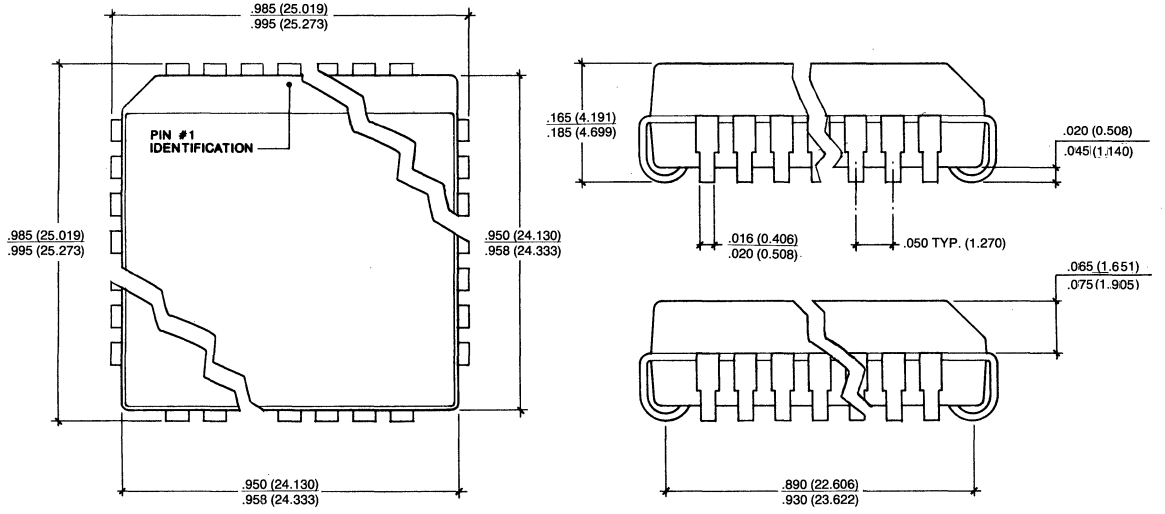


11

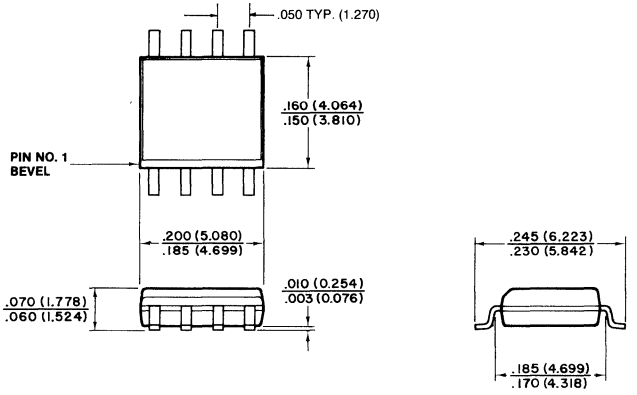
SURFACE MOUNTED
QUAD (PLCC)
52 Leads



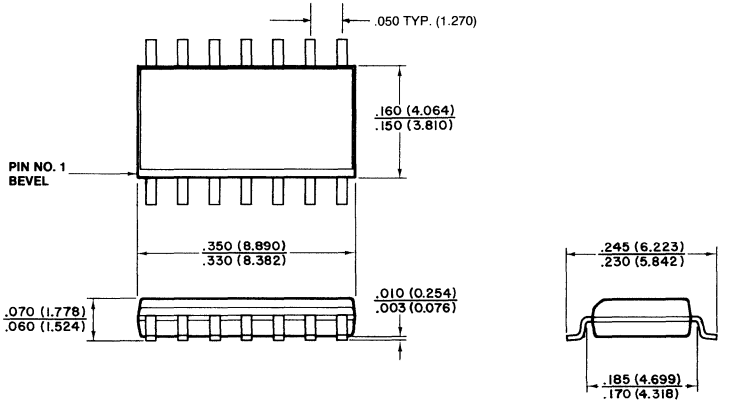
SURFACE MOUNTED
QUAD (PLCC)
68 Leads



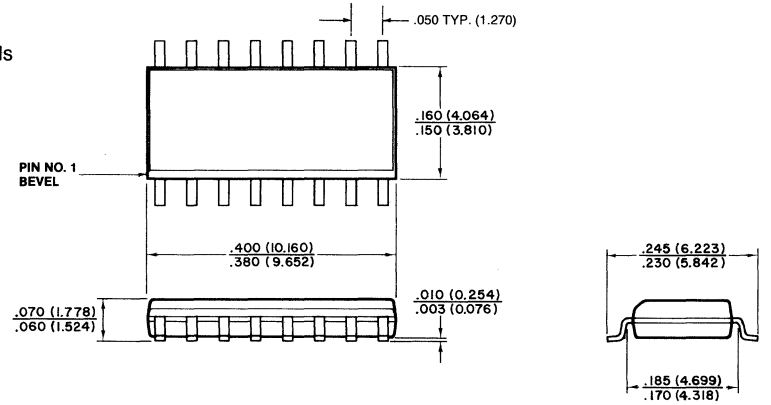
SON
8 Leads



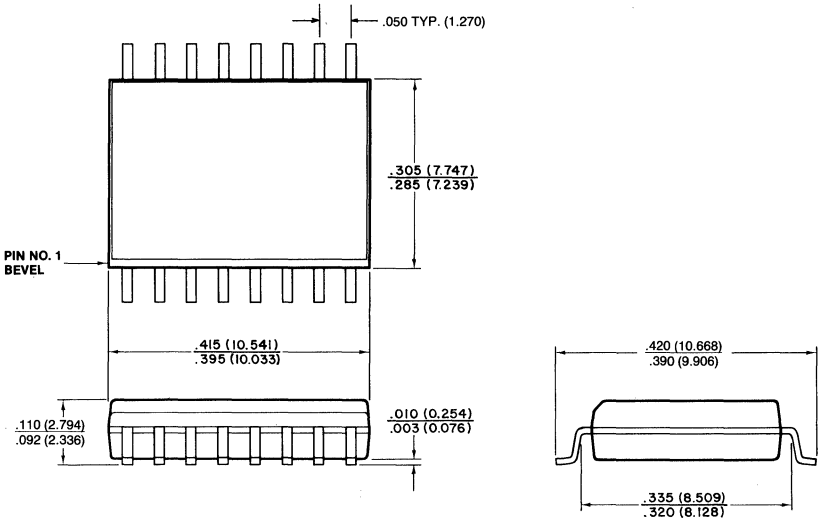
SON
14 Leads



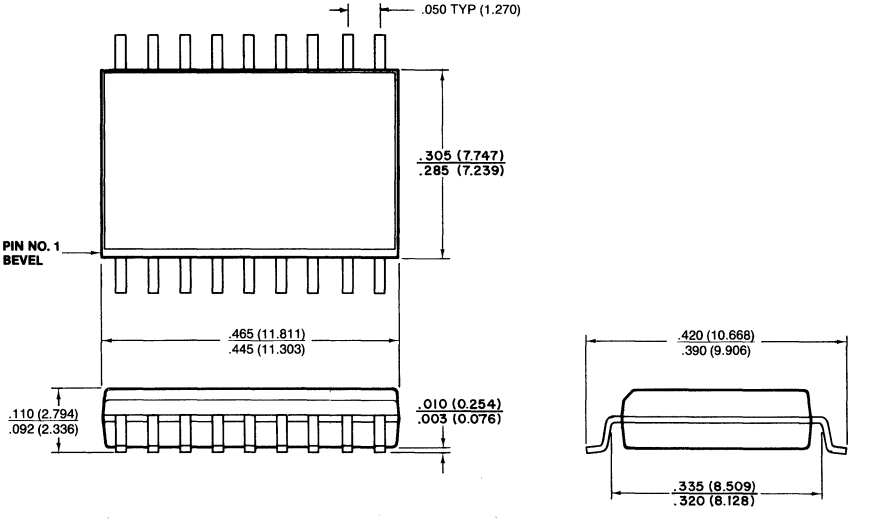
SON
16 Leads



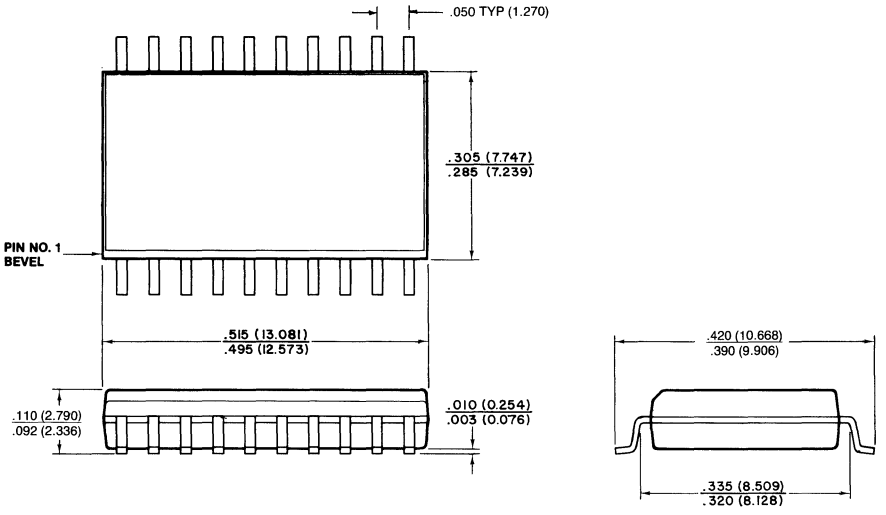
SOL
16 Leads



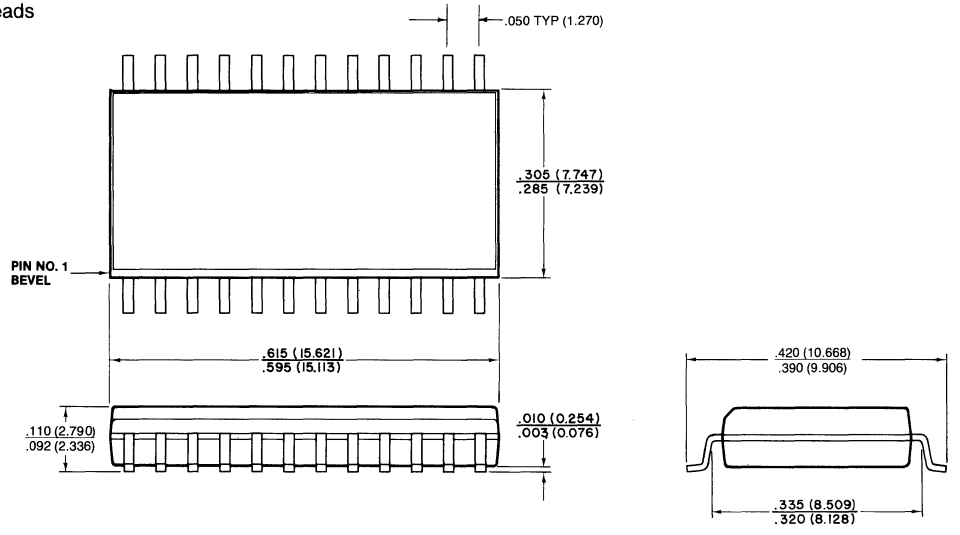
SOL
18 Leads



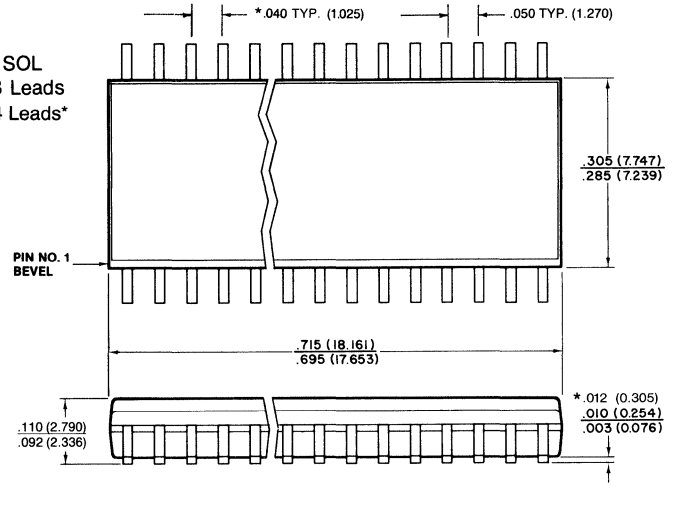
SOL
20 Leads

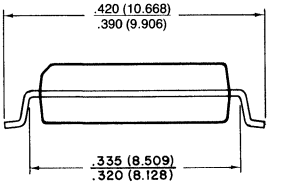


SOL
24 Leads

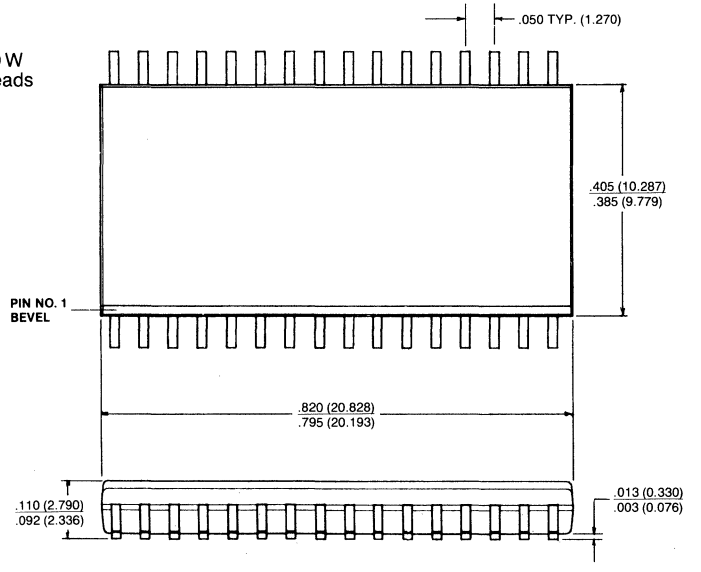


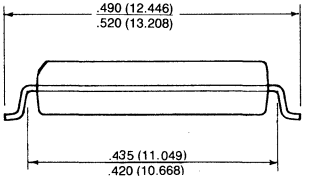
SOL
28 Leads
34 Leads*



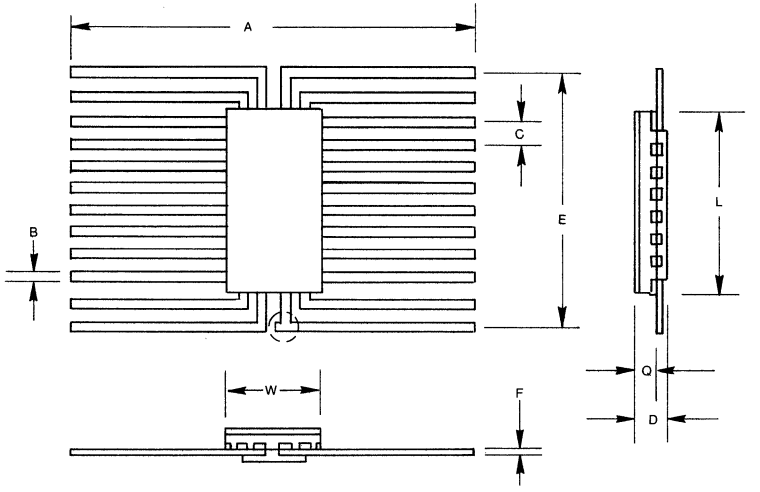


SOW
32 Leads

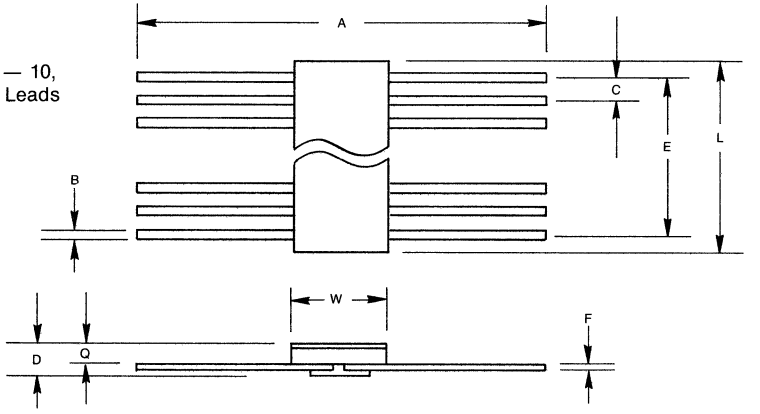




FLAT PACK
24 Leads



FLAT PACK — 10,
28 and 32 Leads



Pkg. Type	Lead Cnt.	A	B	C	D	E	F	L	Q	W
F	10	.900	.015 .019	.045 .055	.090 max	.200 typ	.004 .007	.250 .260	.074 typ	.250 .260
F	24	.900	.015 .019	.050 typ	.087 max	.567 typ	.004 .007	.391 .405	.075 typ	.264 .276
F	28	1.150	.015 .019	.045 .055	.092 max	.645 .655	.004 .007	.712 .728	.085 .078	.492 .508
F	32	1.150	.015 .019	.045 .055	.092 max	.745 .755	.004 .007	.812 .828	.085 .078	.492 .508

Section 12

SALES OFFICES/ DISTRIBUTORS

silicon systems™
INNOVATORS IN INTEGRATION

World Wide
Field Sales Network

North American

Regional Offices & Sales Representatives

NORTHWEST

SSI REGIONAL
Jon Tammel, RM
Silicon Systems, Inc.
2700 Augustine Dr.
Suite 219
Santa Clara, CA 95054
Ph: 408/980-9771
TLX: 171-200
FAX: 408/748-9488

CALIFORNIA
Magna Sales
Santa Clara
Ph: 408/727-8753
TLX: 171-200
FAX: 408/727-8573

CANADA
Enerlec
Surrey, BC
Ph: 604/888-1667
TLX: 04-365-634
FAX: 604/888-3381

COLORADO
Lange Sales
Littleton
Ph: 303/795-3600
TLX: 450-017
FAX: 303/795-0373

OREGON
Western Technical Sales
Beaverton
Ph: 503/644-8860
FAX: 503/644-8200

UTAH
Lange Sales
Salt Lake City
Ph: 801/487-0843
FAX: 801/484-5408

WASHINGTON
Western Technical Sales
Bellevue
Ph: 206/641-3900
FAX: 206/641-5829

Western Technical Sales
Spokane
Ph: 509/922-7600
FAX: 509/922-7603

SOUTHWEST

SSI REGIONAL
Silicon Systems, Inc.
14351 Myford Road
Tustin, CA 92680
Ph: 714/731-7110
TWX: 472-2133
FAX: 714/669-8814
714/731-5457

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(L.A. District)
454 Carson Plaza Drive
Suite 209
Carson, CA 90745
Ph: 213/532-1524,3499
FAX: 213/532-4571

ARIZONA
Western High Tech
Marketing, Inc.
Scottsdale
Ph: 602/860-2702
FAX: 602/860-2712

CALIFORNIA
Hadden Associates
San Diego
Ph: 619/565-9444
FAX: 619/565-1802

SC Cubed
Thousand Oaks
Ph: 805/496-7307
FAX: 805/495-3601

SC Cubed
Tustin
Ph: 714/731-9206
FAX: 714/731-7801

NEW MEXICO
Western High Tech
Marketing Inc.
Albuquerque
Ph: 505/884-2256
FAX: 505/884-2258

CENTRAL

SSI REGIONAL
Silicon Systems, Inc.
Tom George, RM
2201 N. Central Express-
way
Suite 132
Richardson, TX 75080
Ph: 214/669-3381
FAX: 214/669-3495

ILLINOIS
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Office
Ph: 214/669-3381

INDIANA
Technology Marketing
Corporation (TMC)
Carmel
Ph: 317/844-8462
FAX: 317/573-5472

Fort Wayne
Ph: 219/432-5553
FAX: 219/432-5555

KANSAS
B. C. Electronics
Kansas City
Ph: 913/342-1211
FAX: 314/524-8906

Wichita
Ph: 316/722-0104

KENTUCKY
Technology Marketing
Corporation (TMC)
Louisville
Ph: 502/893-1377
FAX: 502/896-6679

MICHIGAN
A.P. Associates
Brighton
Ph: 313/229-6550
TLX: 816/287-310
FAX: 313/229-9356

MINNESOTA
Com-Tek
Eden Prairie
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TWX: 310/431-0122
FAX: 612/941-4322

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FAX: 513/871-2524

Columbus
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FAX: 513/871-2524

Solon
Ph: 216/248-7370
FAX: 513/871-2524

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OM Assoc., Inc.
Austin
Ph: 512/388-1151
FAX: 512/244-9505

Richardson
Ph: 214/690-6746
TWX: 910-860-5368
FAX: 214/690-8721

Houston
Ph: 713/789-4426
TLX: 791-363
FAX: 713/789-4825

WISCONSIN
Please call Regional Office
Ph: 214/669-3381

EAST

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53 Stiles Road
Salem, NH 03079
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603/898-6721
603/898-6722
FAX: 603/898-9538

CONNECTICUT
NRG, Ltd.
Fairfield
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FAX: 203/335-2127

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Har-Tech
Downsview
Ph: 416/665-7773
FAX: 416/665-7290

Nepean
Ph: 613/726-9410
FAX: 613/726-8834

CANADA - Quebec
Har-Tech
Pointe Claire
Ph: 514/694-6110
FAX: 514/694-8501

MASSACHUSETTS
Mill-Bern Associates
Woburn
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TWX: 710-332-0077
FAX: 617/932-0511

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FAX: 201/692-8367

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FAX: 716/427-0614

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TLX: 82-1721
FAX: 315/437-8283

Technical Marketing Group
Melville
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FAX: 516/351-8667

PENNSYLVANIA
Omni Sales
Erdenheim
Ph: 215/233-4600
FAX: 215/233-4702

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Technology Marketing Associates (TMA)
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Ph: 205/883-7893
TWX: 510-600-4721
FAX: 205/882-6162

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TWX: 510-600-4721
FAX: 404/843-8705

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TWX: 510-600-4721
FAX: 407/857-6412

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TWX: 510-600-4721
FAX: 305/977-9044

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TWX: 510-600-4721
FAX: 813/545-8617

Melbourne
Ph: 407/676-3776
TWX: 510-600-4721
FAX: 407/676-4231

MARYLAND
Burgin-Kreh Associates
Baltimore
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FAX: 301/265-8536

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Technology Marketing Associates (TMA)
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FAX: 919/870-1085
TWX: 510-600-4721

VIRGINIA
Burgin-Kreh Associates
Lynchburg
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FAX: 804/239-1333

International
Sales Representatives / Distributors

EUROPE

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The Common
West Chiltington
Pulborough RH20 2PL
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TLX: 878411
FAX: 44/7983-2117

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D & D Electronics BVBA
Antwerp
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FAX: (32) 3-828-7254
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C-88
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Ilford, Essex
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FAX: (44) 1-518-3222
TLX: (851) 895-4213

FINLAND
Komdel Oy
Espoo
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TLX: (857) 121926
FAX: (358) 0-885-327

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Datadis, S. A.
Boulogne
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FAX: (33) 1-69-20-49-00
TLX: (842) 201-905

GERMANY
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FAX: (49) 89-857-3702
TWX: 521-511

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(30) 1-362-3614
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Milano
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TLX: 314543

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FAX: (31) 10-458-6482
TLX: 26160

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FAX: (47) 2-846020

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FAX: (27) 11-787-0831

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FAX: 34-1-456-7159

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FAX: (46) 8-732-7058
TLX: 13888 BEXTE S

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TWX: 822-542
FAX: 011-41-1-700-2071

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TLX: (790) 33288
FAX: (61) 3-288-9168

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FAX: (852) 5-285764
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TLX: 11-2633
FAX: 91-22-494-3459

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Internix
Tokyo
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TLX: (781) 26733
FAX: (81) 3-366-8566

KOREA
Hanaro Corporation
Seoul
Ph: 82-2-784-1144, 1145, 1146
TLX: (787) 26878
FAX: 82-2-784-0157

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Dynamar International
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TLX: (786) 26283
FAX: (65) 747-2648

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Ph: 55 (11) 531-9355
TLX: (391) 11-53288 HTHB BR
FAX: 55-240-2650

MEXICO
Panamtek
Mexico City
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TLX: 1173470
FAX: 011-754-6480

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FAX: 52-36-30-3115

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Toronto
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Vancouver
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