SONY CXD1185AQ

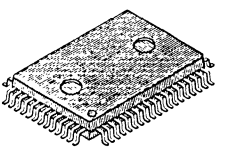
SCSI Controller LSI — Preliminary

Description

The CXD1185AQ is a high performance CMOS SCSI controller LSI that conforms to ANSIX3. 131-1986 standards. The CXD1185AQ is capable of operating in both initiator and target modes. It satisfies all standard SCSI bus features, such as arbitration, selection and parity generation/check functions. A 24-bit data transfer byte counter and 16-byte FIFO are built into the hardware. Two separate buses for data and processor makes high speed data transfer possible. 48 mA (sinking) port is built-in to achieve reduction in the number of external components.

The chip offers a set of high level commands at SCSI phase level. It is also possible to read/write all individual SCSI signals. The combination of the above two makes programs simpler and at the same time improves programability.

64pin QFP (Plastic)



Features

- Satisfies all SCSI bus features, including arbitration, selection, parity generation/check and synchronous data transfer mode.
- Maximum synchronous data transfer rate of 4.0MB/sec and maximum asynchronous data transfer rate of 2.5 MB/sec.
- Provides two separate parts for the data bus and the CPU bus.
- Built-in user-programmable timer for selection/reselection timeout operation.
- Supports 8-bit microcomputer bus.
- Supports programmed I/O and DMA transfer modes.
- Built-in 48mA (sinking) SCSI port. The SCSI port can be used as either single-ended port or differential port.
- Built-in 24-bit data transfer counter.
- Built-in 16-byte FIFO.
- Supports SCSI phase commands.
- All SCSI control signals are software controllable.
- All interrupt conditions are software maskable.
- Built-in 4-bit general-use I/O port.
- Programmable SCSI $\overline{RST}$ drive time.
- Programmable interrupt pin (IRQ) active logic level.
- 64-pin QFP.

Application

SCSI controller

Structure

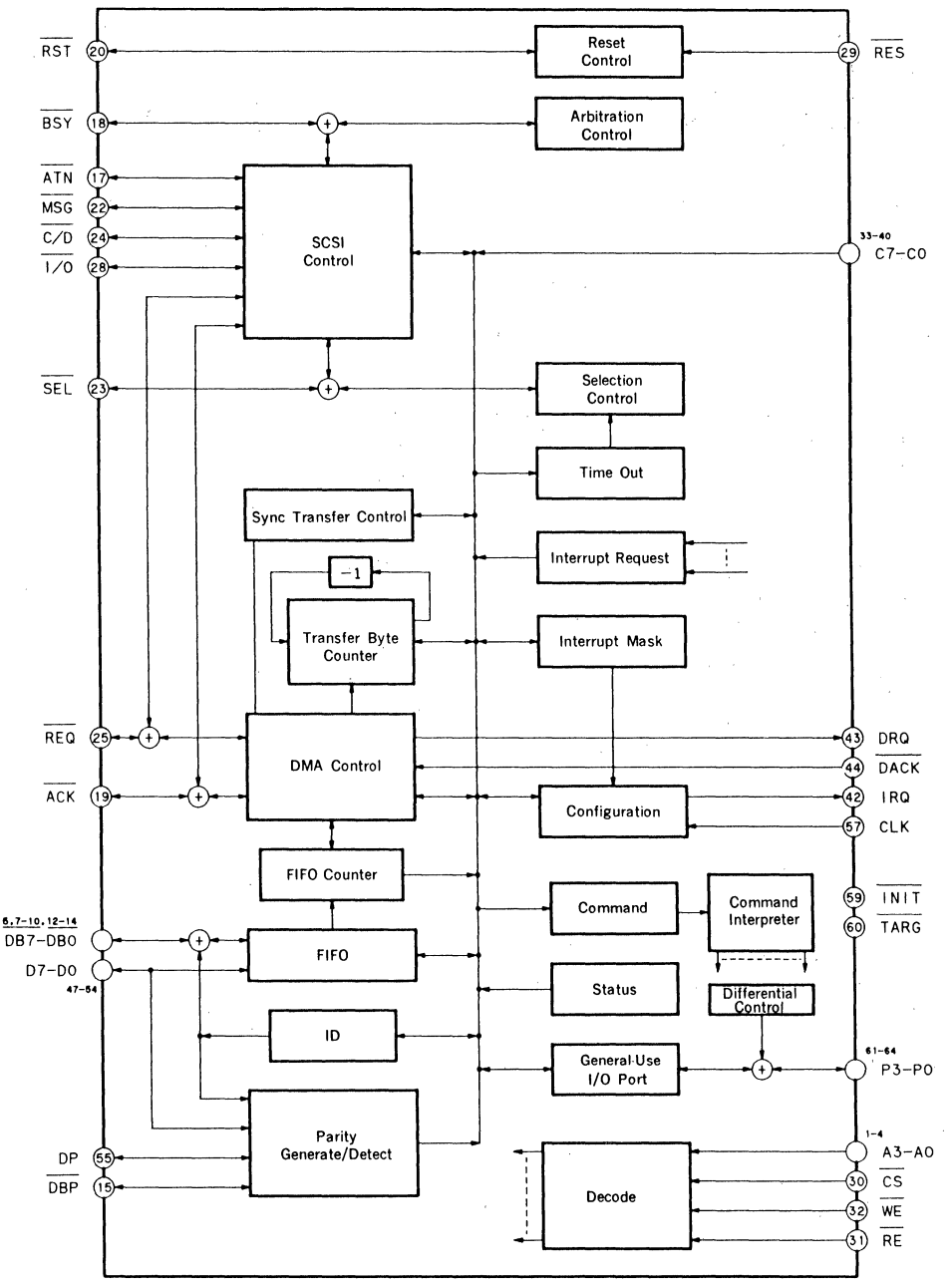
CMOS process

Absolute Maximum Ratings (Ta=25°C, V_{SS}=0V)

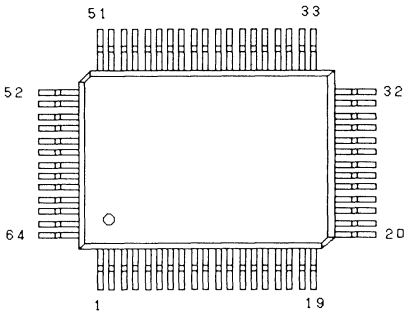
• Supply voltage	V_{DD}	$V_{SS}-0.5$ to $+7.0$	V
• Input voltage	V_I	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
• Output voltage	V_O	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
• Operating temperature	T_{opr}	-20 to $+75$	°C
• Storage temperature	T_{stg}	-55 to $+150$	°C

PE90271-HP

Block Diagram



Pin Configuration



Pin Description

Pin no.	Symbol	I/O	Description
1	A3	I	Register select signal bit 3
2	A2	I	Register select signal bit 2
3	A1	I	Register select signal bit 1
4	A0	I	Register select signal bit 0
5	$\overline{DB0}$	I/O	SCSI bus $\overline{DB0}$ signal
6	V_{SS}		GND ⟨note 1⟩
7	$\overline{DB1}$	I/O	SCSI bus $\overline{DB1}$ signal
8	$\overline{DB2}$	I/O	SCSI bus $\overline{DB2}$ signal
9	$\overline{DB3}$	I/O	SCSI bus $\overline{DB3}$ signal
10	$\overline{DB4}$	I/O	SCSI bus $\overline{DB4}$ signal
11	V_{SS}		GND ⟨note 1⟩
12	$\overline{DB5}$	I/O	SCSI bus $\overline{DB5}$ signal
13	$\overline{DB6}$	I/O	SCSI bus $\overline{DB6}$ signal
14	$\overline{DB7}$	I/O	SCSI bus $\overline{DB7}$ signal
15	$\overline{DBP}$	I/O	SCSI bus $\overline{DBP}$ signal, odd parity
16	V_{SS}		GND ⟨note 1⟩
17	$\overline{ATN}$	I/O	SCSI bus $\overline{ATN}$ signal
18	$\overline{BSY}$	I/O	SCSI bus $\overline{BSY}$ signal
19	$\overline{ACK}$	I/O	SCSI bus $\overline{ACK}$ signal
20	$\overline{RST}$	I/O	SCSI bus $\overline{RST}$ signal
21	V_{SS}		GND ⟨note 1⟩
22	$\overline{MSG}$	I/O	SCSI bus $\overline{MSG}$ signal
23	$\overline{SEL}$	I/O	SCSI bus $\overline{SEL}$ signal
24	$\overline{C/D}$	I/O	SCSI bus $\overline{C/D}$ signal
25	$\overline{REQ}$	I/O	SCSI bus $\overline{REQ}$ signal
26	V_{DD}		+5 V ⟨note 1⟩
27	V_{SS}		GND ⟨note 1⟩
28	$\overline{I/O}$	I/O	SCSI bus $\overline{I/O}$ signal

Pin no.	Symbol	I/O	Description
29	$\overline{RES}$	I	Reset all registers, negative logic
30	$\overline{CS}$	I	Chip select signal, negative logic
31	$\overline{RE}$	I	Internal register read signal, negative logic
32	$\overline{WE}$	I	Internal register write signal, negative logic
33	C7	I/O	CPU bus bit 7
34	C6	I/O	CPU bus bit 6
35	C5	I/O	CPU bus bit 5
36	C4	I/O	CPU bus bit 4
37	C3	I/O	CPU bus bit 3
38	C2	I/O	CPU bus bit 2
39	C1	I/O	CPU bus bit 1
40	C0	I/O	CPU bus bit 0
41	V_{SS}		GND 〈note 1〉
42	IRQ	O	Interrupt request signal
43	DRQ	O	DMA request signal
44	$\overline{DACK}$	I	DMA acknowledge signal, negative logic
45	$\overline{WED}$	I	Data bus write signal, negative logic 〈note 3〉
46	$\overline{RED}$	I	Data bus read signal, negative logic 〈note 3〉
47	D0	I/O	Data bus bit 0 〈note 3〉
48	D1	I/O	Data bus bit 1 〈note 3〉
49	D2	I/O	Data bus bit 2 〈note 3〉
50	D3	I/O	Data bus bit 3 〈note 3〉
51	D4	I/O	Data bus bit 4 〈note 3〉
52	D5	I/O	Data bus bit 5 〈note 3〉
53	D6	I/O	Data bus bit 6 〈note 3〉
54	D7	I/O	Data bus bit 7 〈note 3〉
55	DP	I/O	Data bus parity signal 〈note 4〉
56	V_{SS}		GND 〈note 1〉
57	CLK	I	Clock input,5 - 16MHz
58	V_{DD}		+5 V 〈note 1〉
59	$\overline{INIT}$	O	Initiator operation indicator signal
60	$\overline{TARG}$	O	Target operation indicator signal
61	P0 (DOE)	I/O	General-use port bit 0 (SCSI data output authorization) 〈note 2〉
62	P1 (ARB)	I/O	General-use port bit 1 (arbitration in progress) 〈note 2〉
63	P2 (BSYO)	I/O	General-use port bit 2 (SCSI $\overline{BSY}$ output) 〈note 2〉
64	P3 (SELO)	I/O	General-use port bit 3 (SCSI $\overline{SEL}$ output) 〈note 2〉

〈Note 1〉 All V_{DD} and V_{SS} pins should be connected to the power supply and ground, respectively.

〈Note 2〉 Items in parentheses ( ) indicate the meaning of the signal when operating in the SCSI differential mode.

〈Note 3〉 In systems where the CPU and data buses are not separate , connect the $\overline{WED}$ and $\overline{RED}$ pins to $\overline{WE}$ and $\overline{RE}$, respectively, and Pins D7-D0 to Pins C7-C0.

〈Note 4〉 If the data bus parity signal is not used, pull up the DP pin using a resistor.

Electrical Characteristics

DC characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
High level input voltage	V_{IHT}		2.2			V
Low level input voltage	V_{ILT}				0.8	V
SCSI bus pin input voltage hysteresis	V_{T+}-V_{T-}		0.2			V
High level output voltage	V_{OH}	$I_{OH}=-2mA$	$V_{DD}-0.5$			V
Low level output voltage	V_{OL}	$I_{OL}=4mA$			0.4	V
SCSI bus pin output voltage	V_{OLS}	$I_{OL}=48mA$			0.5	V
Input leak current	I_{LI1}		−10		10	μA
Input leak current (double-way pin)	I_{LI2}		−40		40	μA

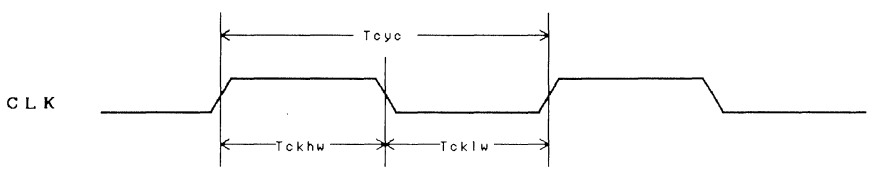
I/O Capacitance

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin	C_{IN}			9	pF
Output pin	C_{OUT}			11	pF
Input/Output pin	$C_{I/O}$			11	pF

AC characteristics (Ta = −20 to +75°C, V_{DD} = 5V ± 10%)

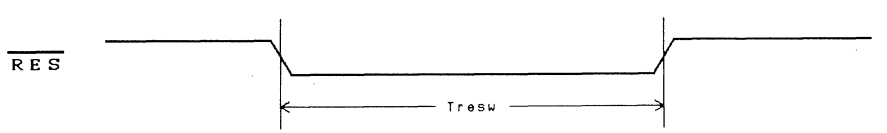
The following capacitances are assumed : input, output pins : 65pF, input /output pins : 125pF.

Clock input



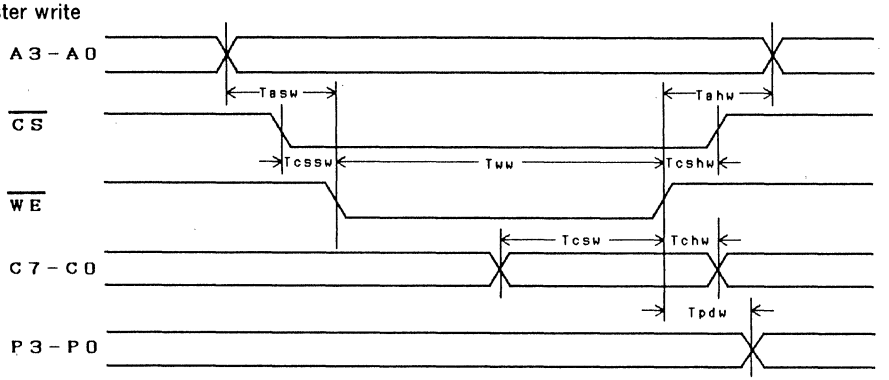
Item	Symbol	Min.	Typ.	Max.	Unit
Clock period	T_{cyc}	5		16	MHz
Clock pulse high level width (period: 16MHz)	T_{ckhw}	31		33	ns
Clock pulse low level width (period: 16MHz)	T_{cklw}	31		33	ns

Reset input



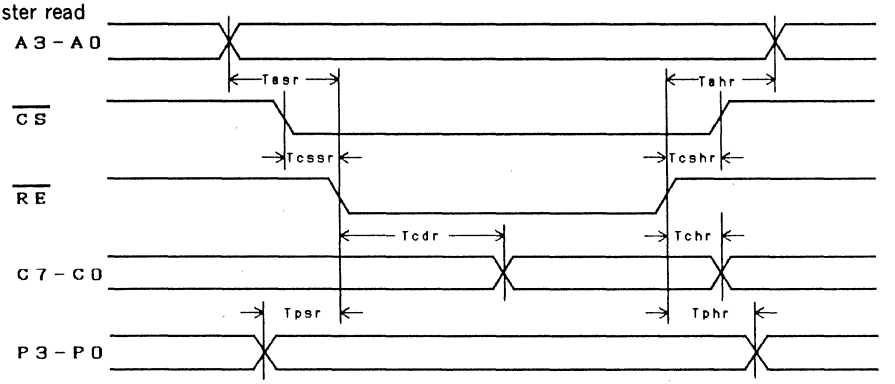
Item	Symbol	Min.	Typ.	Max.	Unit
Reset pulse width	T_{resw}	100			ns

Register write



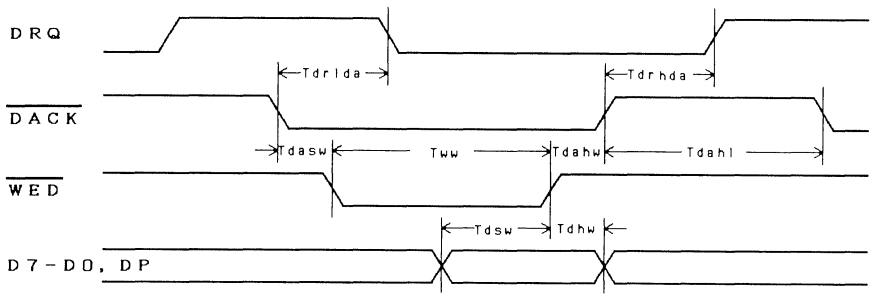
Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (vs. $\overline{WE}$ ↓)	Tasw	0			ns
$\overline{CS}$ setup time (vs. $\overline{WE}$ ↓)	Tcssw	0			ns
$\overline{WE}$ pulse width	Tww	70			ns
Date setup time (vs. $\overline{WE}$ ↑)	Tcsw	30			ns
Address hold time (vs. $\overline{WE}$ ↑)	Tahw	0			ns
$\overline{CS}$ hold time (vs. $\overline{WE}$ ↑)	Tcshw	0			ns
Data hold time (vs.$\overline{WE}$ ↑)	Tchw	10			ns
Port delay time (vs. $\overline{WE}$ ↑)	Tpdw			100	ns

Register read



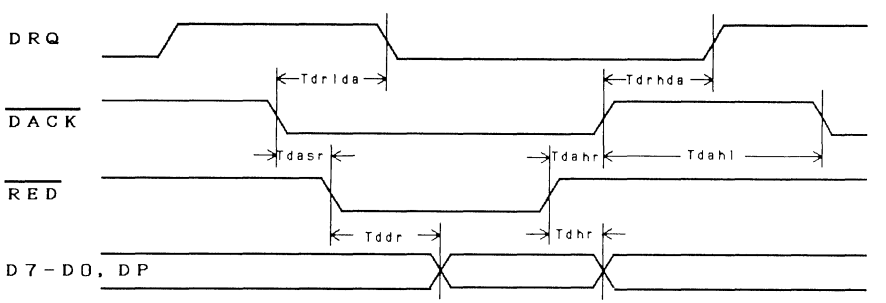
Item	Symbol	Min.	Typ.	Max.	Unit
Address setup time (vs. $\overline{RE}$ ↓)	Tasr	0			ns
$\overline{CS}$ setup time (vs. $\overline{RE}$ ↓)	Tcssr	0			ns
Data delay time (vs.$\overline{RE}$ ↓)	Tcdr			130	ns
Address hold time (vs. $\overline{RE}$ ↑)	Tahr	0			ns
$\overline{CS}$ hold time (vs. $\overline{RE}$ ↑)	Tcshr	0			ns
Date hold time (vs. $\overline{RE}$ ↑)	Tchr	5		25	ns
Port setup time (vs. $\overline{RE}$ ↓)	Tpsr	0			ns
Port hold time (vs.$\overline{RE}$ ↑)	Tphr			0	ns

DMA write



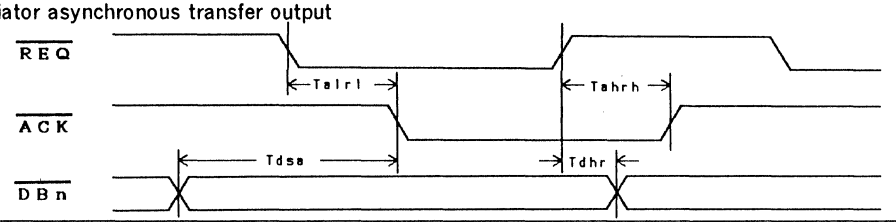
Item	Symbol	Min.	Typ.	Max.	Unit
DRQ fall time (vs. $\overline{\text{DACK}}$ ↓)	Tdrlda			70	ns
$\overline{\text{DACK}}$ setup time (vs. $\overline{\text{WED}}$ ↓)	Tdasw	0			ns
$\overline{\text{WED}}$ pulse width	Tww	50			ns
Data setup time (vs. $\overline{\text{WED}}$ ↑)	Tdsw	20			ns
$\overline{\text{DACK}}$ hold time (vs. $\overline{\text{WED}}$ ↑)	Tdahw	10			ns
Data hold time (vs. $\overline{\text{WED}}$ ↑)	Tdhw	10			ns
DRQ rise time (vs. $\overline{\text{DACK}}$ ↑)	Tdrhda			110	ns
$\overline{\text{DACK}}$ fall time (vs. $\overline{\text{DACK}}$ ↑)	Tdahl	50			ns

DMA read



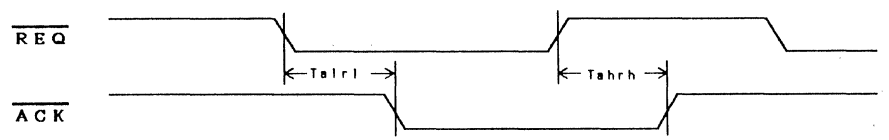
Item	Symbol	Min.	Typ.	Max.	Unit
DRQ fall time (vs. $\overline{\text{DACK}}$ ↓)	Tdrlda			70	ns
$\overline{\text{DACK}}$ setup time (vs. $\overline{\text{RED}}$ ↓)	Tdasr	0			ns
Data delay time (vs. $\overline{\text{RED}}$ ↓)	Tddr			90	ns
$\overline{\text{DACK}}$ hold time (vs. $\overline{\text{RED}}$ ↑)	Tdahr	10			ns
Data hold time (vs. $\overline{\text{RED}}$ ↑)	Tdhr	5		25	ns
DRQ rise time (vs. $\overline{\text{DACK}}$ ↑)	Tdrhda			110	ns
$\overline{\text{DACK}}$ fall time (vs. $\overline{\text{DACK}}$ ↑)	Tdahl	50			ns

Initiator asynchronous transfer output



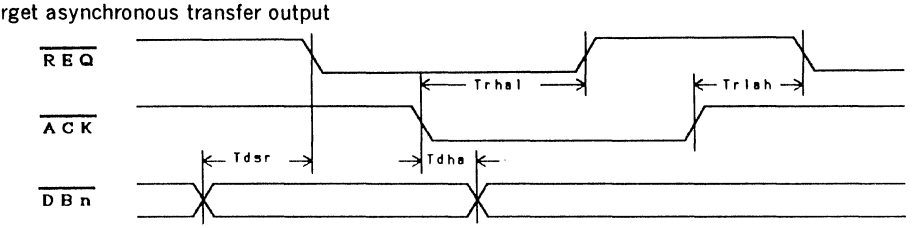
Item	Symbol	Min.	Typ.	Max.	Unit
$\overline{ACK}$ fall time (vs. $\overline{REQ}$ ↓)	Talrl			120	ns
Data setup time (vs. $\overline{ACK}$ ↓)	Tdsa	55			ns
$\overline{ACK}$ rise time (vs. $\overline{REQ}$ ↑)	Tahrh			90	ns
Data hold time (vs. $\overline{REQ}$ ↑)	Tdhr			195	ns

Initiator asynchronous transfer input



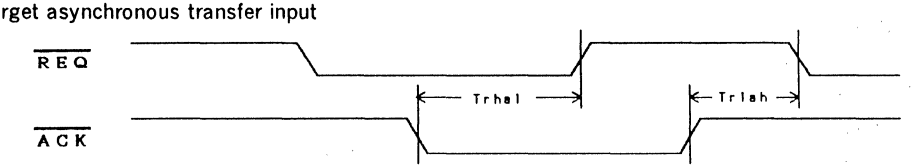
Item	Symbol	Min.	Typ.	Max.	Unit
$\overline{ACK}$ fall time (vs. $\overline{REQ}$ ↓)	Talrl			120	ns
$\overline{ACK}$ rise time (vs. $\overline{REQ}$ ↑)	Tahrh			90	ns

Target asynchronous transfer output



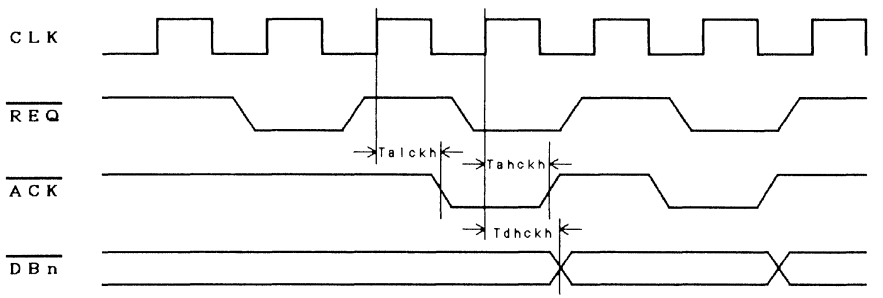
Item	Symbol	Min.	Typ.	Max.	Unit
Data setup time (vs. $\overline{REQ}$ ↓)	Tdsr	55			ns
$\overline{REQ}$ rise time (vs. $\overline{ACK}$ ↓)	Trhal			90	ns
Data hold time (vs. $\overline{ACK}$ ↓)	Tdha			195	ns
$\overline{REQ}$ fall time (vs. $\overline{ACK}$ ↑)	Trlah			120	ns

Target asynchronous transfer input



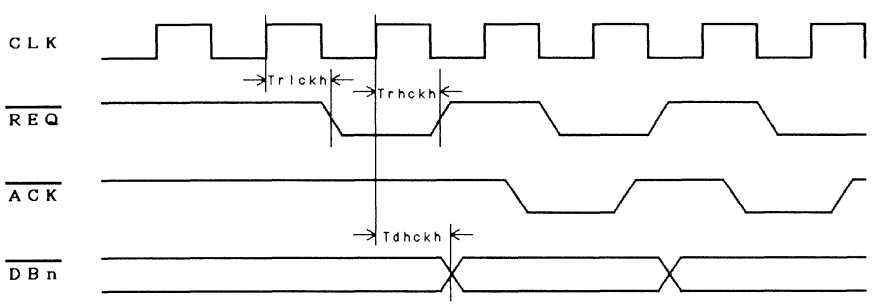
Item	Symbol	Min.	Typ.	Max.	Unit
$\overline{REQ}$ rise time (vs. $\overline{ACK}$ ↓)	Trhal			90	ns
$\overline{REQ}$ fall time (vs. $\overline{ACK}$ ↑)	Trlah			120	ns

Initiator synchronous transfer output



Item	Symbol	Min.	Typ.	Max.	Unit
$\overline{ACK}$ fall time (vs. CLK ↑)	Talckh			130	ns
$\overline{ACK}$ rise time (vs. CLK ↑)	Tahckh			100	ns
Data hold time (vs. CLK ↑)	Tdhckh			170	ns

Target synchronous transfer output



Item	Symbol	Min.	Typ.	Max.	Unit
$\overline{REQ}$ fall time (vs. CLK ↑)	Trlckh			130	ns
$\overline{REQ}$ rise time (vs. CLK ↑)	Trhckh			100	ns
Data hold time (vs. CLK ↑)	Tdhckh			170	ns

Description of Functions

1. Internal registers

CXD1185AQ possesses 16 internal registers. The CPU can control CXD1185AQ by reading and writing these registers.

A summary of the registers is provided below.

Address	Read	Write
0	Status	Command
1	SCSI data	←
2	Interrupt request 1	〈 * 〉
3	Interrupt request 2	Environment setting
4	SCSI control monitor	Selection/reset timer
5	FIFO status	〈 * 〉
6	SCSI ID	←
7	Transfer byte counter (low)	←
8	Transfer byte counter (middle)	←
9	Transfer byte counter (high)	←
A	Interrupt authorization 1	←
B	Interrupt authorization 2	←
C	Mode	←
D	Sync transfer control	←
E	SCSI bus control	←
F	I/O port	←

〈*〉 No register assigned to this address.

1-1. Status register (R0 : R)

This register is used to monitor the status of CXD1185AQ.

7	6	5	4	3	2	1	0
MRST	MDBP		INIT	TARG	TRBZ	MIRQ	CIP

MRST : Monitors the SCSI bus $\overline{RST}$ signal, positive logic.

MDBP : Monitors the SCSI bus $\overline{DBP}$ signal, positive logic.

INIT : "1" when CXD1185AQ is in initiator status.
When this bit is set to "1", all commands except ones which are valid in target status and in disconnected status are accepted.

TARG : "1" when CXD1185AQ is in target status.
When this bit is set to "1", all commands except ones which are valid in initiator status and in disconnected status are accepted.

TRBZ : When this bit is set to "1", it indicates that the transfer byte counter count is zero.

MIRQ : Monitors the interrupt request signal (IRQ signal).
This bit is set whenever interrupt request occurs and cleared once interrupt request 1 register and interrupt 2 register are read. This bit is not affected by the content of the interrupt authorization register. The logic level of this bit is not affected by the SIRM bit in the environment setting register.

CIP : Indicates that a chip command is being executed.
While this bit is "1", no new commands can be written to the command register, with the exception of the "Reset Chip" command.

1-2. Command register (R0 : W)

This is the register to which CXD1185AQ commands are written.

When a command is written to this register, status register bit 0 (CIP) is set. When the command is executed and terminated, interrupt request register bit 7 (FNC) is set, and the CIP bit and command register are cleared.

7	6	5	4	3	2	1	0
CAT1	CAT0	DMA	TRBE	CMD3	CMD2	CMD1	CMD0

CAT1, CAT0 :

Sets the category code given to CXD1185AQ.

CXD1185AQ commands are divided into the following four categories :

CAT1	CAT0	Mode
0	0	Commands which are valid in any status
0	1	Commands which are valid in disconnected status
1	0	Commands which are valid in target status
1	1	Comannds which are valid in initiator status

If the current status of CXD1185AQ does not match with the category code in the command received, the CIP and command registers are cleared. No interrupt is generated in this case.

DMA : DMA mode

When this bit is set to "1" and a transfer command is executed, DMA transfer takes place via the data bus (D7-D0). During the DMA transfer, any attempts by the CPU to read/write SCSI data register via CPU bus is ignored.

TRBE : Activates the transfer byte counter.

When this bit is set to "1" and a transfer command is executed, the transfer byte counter value is decremented each time a byte of data is transferred.

When the counter reaches "0" the next data request is stopped. At this point, if the data transfer mode is output to SCSI or in DMA mode, CXD1185AQ will continue to transfer any data remaining in FIFO until it is empty. If a transfer command is executed when this bit is set to "0", 1 byte of data will be transferred regardless of the value of the transfer byte counter. In this case the transfer byte counter is not decremented. When DMA bit is set, TRBE bit must also be set. These two bits can be set simultaneously during command write.

CMD3, CMD2, CMD1, CMD0 :

Indicates the command code.

CXD1185AQ responds to the following commands. See the command description section for detailed information.

Category	DMA	TRBE	Command code	Command
0 0	0	0	0 0 0 0	No Operation
	0	0	0 0 0 1	Reset Chip
	0	0	0 0 1 0	Assert $\overline{RST}$
	0	0	0 0 1 1	Flush FIFO
	0	0	0 1 0 0	Assert SCSI Control
	0	0	0 1 0 1	Deassert SCSI Control
	0	0	0 1 1 0	Assert SCSI Data
	0	0	0 1 1 1	Deassert SCSI Data
0 1	0	0	0 0 0 0	Reselect
	0	0	0 0 0 1	Select without $\overline{ATN}$
	0	0	0 0 1 0	Select with $\overline{ATN}$
	0	0	0 0 1 1	Enable Selection/Reselection
	0	0	0 1 0 0	Disable Selection/Reselection
1 0	*	*	0 0 0 0	Send Message
	*	*	0 0 0 1	Send Status
	*	*	0 0 1 0	Send Data
	0	0	0 0 1 1	Disconnect
	*	*	0 1 0 0	Receive Message Out
	*	*	0 1 0 1	Receive Command
	*	*	0 1 1 0	Receive Data
1 1	*	*	0 0 0 0	Transfer Information
	*	*	0 0 0 1	Transfer Pad
	0	0	0 0 1 0	Deassert $\overline{ACK}$
	0	0	0 0 1 1	Assert $\overline{ATN}$
	0	0	0 1 0 0	Deassert $\overline{ATN}$

〈*〉 Don't care, except that if DMA bit is set to "1", TRBE bit must be set to "1".

1-3. SCSI data register (R1 : R/W)

This register is used when transferring data between the SCSI bus and the CPU bus.

When data is output to the SCSI bus via the CPU bus, data can be written to this register if the FIFO status register bit 4 (FIF) is "0".

When data is input from SCSI bus, data can be read from this register if the FIFO status register bit 7 (FIE) is "0".

When "Assert SCSI data" is executed the 16 byte FIFO becomes a 1 byte FIFO. Any value written to the register will be on the SCSI bus instantly and a read operation will return the current SCSI data bus value.

When a DMA transfer is performed via the data bus, reads and writes to the SCSI data register are performed using the $\overline{WED}$, $\overline{RED}$ and $\overline{DACK}$ signals.

1-4. Interrupt request registers 1 and 2

These registers show the cause of the interrupt.

When an interrupt authorized by interrupt authorization registers 1 or 2 is generated, the IRQ pin is set immediately.

Bits in the interrupt request registers 1 and 2 are cleared once the registers are read by the CPU. When all interrupt bits are cleared, MIRQ bit (in the status register) and the IRQ pin are cleared.

Note that interrupt bits in these registers are set regardless of the values in the interrupt authorization registers. If interrupt requests are software polled, interrupt request registers 1 and 2 should only be read

when the MIRQ bit, in the status register, is "1".

1-4-1. Interrupt request register 1 (R2 : R)

This register's interrupt conditions can be masked in the interrupt authorization register 1.

When one of the bits in this register is set, MIRQ bit in the status register is set. If the interrupt bit is authorized in the interrupt authorization register 1, the IRQ pin is activated simultaneously.

7	6	5	4	3	2	1	0
			STO	RSL	SWA	SWOA	ARBF

STO : Selection Time Over
Indicates a time out error during selection. Also, indicates that the SCSI bus $\overline{RST}$ signal has been driven for the time set in the selection/reset timer if the mode register bit 4 (TMSL) is set to "1". The selection time out time and SCSI bus $\overline{RST}$ signal drive time are determined by the value of the selection/reset timer register.

RSL : Reselected
Indicates that reselection has taken place. FNC bit in the interrupt register 2 is set after reselection. The CPU may not write new commands to the command register until the FNC bit is set. This bit is not set unless the "Enable Selection/ Reselection" command is executed.

SWA : Selection With ATN
Indicates that selection has taken place with the SCSI bus $\overline{ATN}$ signal driven. FNC bit in the interrupt register 2 is set after selection. The CPU may not write new commands to the command register until the FNC bit is set. This bit is not set unless the " Enable Selection/Reselection" command is executed.

SWOA : Selection Without ATN
Indicates that selection has taken place. FNC bit in the interrupt register 2 is set after selection. The CPU may not write new commands to the command register until the FNC bit is set. This bit is not set unless the "Enable Selection/Reselection" command is executed.

ARBF : Arbitration Fail
Indicates that CXD1185AQ lost in the arbitration for the right to use the SCSI bus. This bit is set when, after receiving a selection/reselection command, the chip waited for bus free and entered arbitration only to be encountered by another device with higher priority. As soon as this bit is set the selection/reselection command is terminated. To participate in another arbitration a new selection/reselection command must be written to the command register.

1-4-2. Interrupt request register 2 (R3 : R)

This register's interrupt conditions can be masked in the interrupt authorization register 2.

When one of the bits in this register is set, MIRQ bit in the status register is set. If the interrupt bit is authorised in the interrupt authorization register 2, the IRQ pin is activated simultaneously.

7	6	5	4	3	2	1	0
FNC	DCNT	SRST	PHC	DATN	DPE	SPE	RMSG

FNC : Function Complete
Indicates that the received command was executed and terminated.

DCNT : Disconnected
Indicates that a disconnect has taken place in the initiator mode.

SRST : SCSI Reset
Indicates that the SCSI bus $\overline{RST}$ pin was driven. This bit is also set when the "Assert $\overline{RST}$" command is executed.

PHC : Phase Change
Indicates that the SCSI phase has been changed. This bit is set if CXD1185AQ is operating in the initiator mode and the target has changed the SCSI phase ($\overline{MSG}$, $\overline{I/O}$, $\overline{C/D}$ signal), and drove $\overline{REQ}$.

DATN : Drive ATN
Indicates that the SCSI bus $\overline{ATN}$ signal has been driven. This bit is set if the CXD1185AQ is operating in the target mode and the initiator has driven the $\overline{ATN}$ signal.

DPE : Data bus Parity Error
Indicates a parity error on the data bus. This bit is only set if environment setting register bit 5 (DPEN) is set to "1". In initial status odd parity (environment register bit 6 set to "0") is selected.

SPE : SCSI bus Parity Error
Indicates a parity error on the SCSI bus. Parity check takes place during the selection phase and data transfer phases.

RMSG : $\overline{REQ}$ in Message Phase
Indicates that the $\overline{REQ}$ signal has been driven during the message phase when the CXD1185AQ is in initiator mode. This bit is used when two different batches of message data have been received during the message phase or if the target requests that a message be resent.

1-5. Environment setting register (R3: W)
This register is used to set the operating mode of the CXD1185AQ.
Normally, some value must be written to this register immediately after a hardware reset from the CPU.

7	6	5	4	3	2	1	0
DIFE	SDPM	DPEN	SIRM			FS1	FS0

DIFE : Selects the differential mode.
When this bit is set to "1", general-use I/O port Pins P3-P0 are assigned for differential mode bits.

SDPM : Selects the data bus parity condition.
This bit is set to "0" for odd parity and to "1" for even parity. However, its value is irrelevant if the DPEN bit is set to "0".

DPEN : Enables parity generation/check for the data bus.
If this bit is set to "1", data bus parity signal is input/output via the DP pin.

SIRM : Selects the IRQ signal logic level.
After a hardware reset is performed, the IRQ signal output is positive logic. To change the IRQ signal to negative logic. "1" must be set in this bit.

FS1, FS0 :
Used to select the CXD1185AQ clock division ratio.
The appropriate values, as shown in the table below, must be written into these bits to match the external clock frequency applied to the CXD1185AQ:

Input frequency (MHz)	FS1	FS0	Clock division ratio
16-13	0	0	4
12-9	0	1	3
8-5	1	*	2

For the changes made to these bits to be effective, "Chip Reset" command must be executed.
Bits FS1 and FS0 are set for a clock division ratio of "4" after a hardware reset.

1-6. SCSI control monitor register (R4 : R)

Current status of all SCSI control signals can be read directly from this register.

7	6	5	4	3	2	1	0
MBSY	MSEL	MMSG	MCD	MIO	MREQ	MACK	MATN

MBSY : Monitors the SCSI bus $\overline{BSY}$ signal. Positive logic.
MSEL : Monitors the SCSI bus $\overline{SEL}$ signal. Positive logic.
MMSG : Monitors the SCSI bus $\overline{MSG}$ siganl. Positive logic.
MCD : Monitors the SCSI bus $\overline{C/D}$ signal. Positive logic.
MIO : Monitors the SCSI bus $\overline{I/O}$ signal. Positive logic.
MREQ : Monitors the SCSI bus $\overline{REQ}$ signal. Positive logic.
MACK : Monitors the SCSI bus $\overline{ACK}$ signal. Positive logic.
MATN : Monitors the SCSI bus $\overline{ATN}$ signal. Positive logic.

1-7. Selection/reset timer register (R4 : W)

This register is used to set the selection time out time or the SCSI bus $\overline{RST}$ drive time.
The real selection time out time can be calculated by the following equation :

$$\text{TIME } (\mu s)=\frac{Div}{f_{cyc}}\times(VAL+1)\times 8{,}192$$

f_{cyc} : Input frequency (MHz)
Div : Clock division ratio (See section on Environment setting register)
VAL : Value written to the selection/reset timer register

Generally the selection time out time is set to 250ms.
When the selection/reset timer register is used to set the drive time for the $\overline{RST}$ signal a "1" must be written to mode register bit 4 (TMSL).
The real $\overline{RST}$ signal drive time can be calculated by the following equation :

$$\text{TIME}(\mu s) = \frac{Div}{f_{cyc}}\times(32\times VAL+38)$$

f_{cyc} : Input frequency (MHz)
Div : Clock division ratio (See section on Environment setting register)
VAL : Value written to the selection/reset timer register

1-8. FIFO status register (R5 : R)

This register is for monitoring the FIFO status.

7	6	5	4	3	2	1	0
FIE			FIF	FC3	FC2	FC1	FC0

FIE : FIFO Empty
Indicates that the FIFO is empty.
FIF : FIFO Full
Indicates that the FIFO is full.
FC3, FC2, FC1, FC0 :
Indicate the number of bytes of data stored in the FIFO.

1-9. SCSI ID register (R6 : R/W)

This register is used to set the SCSI owner ID and the target ID for selection.

The upper three bits in this register have different meanings during reads and writes.

7	6	5	4	3	2	1	0	
SID2	SID1	SID0			OID2	OID1	OID0	(Read)

7	6	5	4	3	2	1	0	
TID2	TID1	TID0			OID2	OID1	OID0	(Write)

SID2, SID1, SID0 :

Indicates which device last selected/reselected the CXD1185AQ.

TID2, TID1, TID0 :

The target ID is written to these bits prior to selection.

OID2, OID1, OID0 :

The owner ID is written to these bits.

1-10. Transfer byte counter (high, middle, low) (R9, R8, R7 : R/W)

The 24-bit counter calculates the number of remaining bytes of transfer data during data transfer between SCSI bus and the CPU bus or data bus. To activate the transfer byte counter, command register bit 4 (TRBE) must be set when writing to the command register.

When data is output to the SCSI bus, the transfer byte counter is decremented at each rise of the $\overline{WE}$ or $\overline{WED}$ signal. When data is input from the SCSI bus, is decremented at each fall of the $\overline{ACK}$ signal when in the initiator mode and at each fall of the $\overline{REQ}$ signal when in the target mode.

1-11. Interrupt authorization registers 1 and 2 (RA, RB : R/W)

These registers are used to determine on which interrupt the IRQ pin should be activated.

The bit positions in these two registers correspond to the bit positions in the interrupt request registers. The IRQ pin will be activated if an interrupt bit becomes "1" and the corresponding bit in the interrupt authorization register is also set to "1".

1-12. Mode register (RC : R/W)

This register is used for setting the modes of CXD1185AQ.

7	6	5	4	3	2	1	0
HDPE	HSPE	HATN	TMSL	SPHI			BDMA

HDPE : When this bit is set to "1", data transfer will be terminated if a parity error is detected on the data bus during a data transfer. However, this bit is irrelevant if environment setting register bit 5 (DPEN) is set to "0".

HSPE : When this bit is set to "1", data transfer will be terminated if a parity error is detected on the SCSI bus during a data transfer.

HATN : When this bit is "1" in target mode, data transfer will be terminated if an $\overline{ATN}$ signal is driven on the SCSI bus.

TMSL : When this bit is set to "1", the selection/reset timer register is used to set the duration of the SCSI bus $\overline{RST}$ signal.

This bit must not be overwritten with a new value if status register bit 0 (CIP) is set to "1". If it is required to drive $\overline{RST}$ signal when the CIP bit is "1", first execute "Reset Chip" command, then overwrite this bit.

SPHI : When this bit is set to "0", if target changes the phase signal during the execution of a transfer command and the $\overline{REQ}$ pin is active, interrupt request register 2 bit 4 (PHC) is set immediately. If this bit is set to "1", in the mode in which data is input from the SCSI bus, the PHC bit is not set until all the FIFO contents are transferred to the CPU bus or the DMA bus.

BDMA : Burst DMA mode. When this bit is set to "1", the DRQ pin be "1" for the whole of the DMA transfer.

1-13. Synchronous transfer control register (RD : R/W)

This register is used to set the transfer period and the offset for synchronous transfers.

7	6	5	4	3	2	1	0
TPD3	TPD2	TPD1	TPD0	TOF3	TOF2	TOF1	TOF0

TPD3, TPD2, TPD1, TPD0 :

Bits used to set the transfer period for synchronous transfers.
The transfer period is designated according to the following equation :

$$RATE\ (\mu s)=\frac{Div}{f_{cyc}\times 2}\times(VAL+1)$$

fcyc : Input frequency (MHz)

Div : Clock division ratio (see section on Environment setting register)

VAL : Value written to TPD3-0

TOF3, TOF2, TOF1, TOF0 :

Bits used to set the offset for synchronous transfers.
The asynchronous transfer mode is selected by writing "0" to all of these bits.

1-14. SCSI bus control register (RE : R/W)

This register is used to control the control signals used by the SCSI bus.
Reading this register consists simply of reading the value which was written there previously. However, if the "Assert SCSI Control" command is executed, "0"s will be read out. The "Assert SCSI Control" command must be executed in order to output this register's value to the SCSI bus.

7	6	5	4	3	2	1	0
ABSY	ASEL	AMSG	ACD	AIO	AREQ	AACK	AATN

ABSY : When this bit is set to "1", the SCSI bus $\overline{BSY}$ signal is driven.

ASEL : When this bit is set to "1", the SCSI bus $\overline{SEL}$ signal is driven.

AMSG : When this bit is set to "1", the SCSI bus $\overline{MSG}$ signal is driven.
However, it is not driven unless CXD1185AQ is in the target mode.

ACD : When this bit is set to "1", the SCSI bus $\overline{C/D}$ signal is driven.
However, it is not driven unless CXD1185AQ is in the target mode.

AIO : When this bit is set to "1", the SCSI bus $\overline{I/O}$ signal is driven.
However, it is not driven unless CXD1185AQ is in the target mode.

AREQ : When this bit is set to "1", the SCSI bus $\overline{REQ}$ signal is driven.
However, it is not driven unless CXD1185AQ is in the target mode.

AACK : When this bit is set to "1", the SCSI bus $\overline{ACK}$ signal is driven.
However, it is not driven unless CXD1185AQ is in the initiator mode.

AATN : When this bit is set to "1", the SCSI bus $\overline{ATN}$ signal is driven.
However, it is not driven unless CXD1185AQ is in the initiator mode.

1-15. I/O port (RF : R/W)

This register is used for input/output switching of the general-use 4-bit port and for reading/writing the contents of the port.

7	6	5	4	3	2	1	0
PCN3	PCN2	PCN1	PCN0	PRT3	PRT2	PRT1	PRT0

PCN3, PCN2, PCN1, PCN0 :

These bits are used for input/output switching of individual bits when Pins P3-P0 are used as a general-use port. When a "1" is written to any of these bits, the corresponding port is set to the output mode.

All these bits are cleared when a hardware reset is performed. Note that first "0" must be written to all these bits before writing a "1" to environment setting register bit 7 (DIFE).

PRT3, PRT2, PRT1, PRT0 :

This is the 4-bit I/O port.

The values written to whichever of these four bits have been set to output mode by PCN3-PCN0 are output via Pins P3-P0. By reading these bits it is possible to monitor the values of Pins P3-P0 directly.

2. Command Description

This section gives description of all the commands supported by the CXD1185AQ.

With the exception of "Reset Chip", the following commands can only be written to the command register when the CIP bit in the status register (bit 0) is "0".

2-1. Commands valid in any status

The following commands can be issued when the CXD1185AQ is in any of its three statuses : disconnected, initiator or target.

The chip is, at any given time, in one of the three status disconnected, initiator or target. This section is divided into following subsections.

- Commands valid in any status
- Commands valid in disconnected state
- Commands valid in initiator mode
- Commands valid in target mode

- No Operation

  This command has no effect on the CXD1185AQ.

  However, the FNC bit is set when the command is completed.

- Reset Chip

  This command initializes the CXD1185AQ.

  Except for the environment setting register, all registers of the CXD1185AQ are cleared. If the clock division ratio is changed in the environment setting register, this command must be executed.

  This command can be executed regardless of the value of the CIP bit.

- Assert $\overline{RST}$

  This command drives the SCSI bus $\overline{RST}$ pin.

  When this command is executed, interrupt request register 2 bit 5 (SRST) is set and an interrupt is generated. The SCSI $\overline{RST}$ signal is active for 25 μs. However, if the $\overline{RST}$ signal drive duration needs to be changed, it is necessary to set mode register bit 4 (TMSL) to "1" and write the drive duration to the selection/reset timer register before executing this command.

- Flush FIFO

  Initializes FIFO.

- Assert SCSI Control
  Outputs the value of the SCSI bus control register to the SCSI bus.
  In initiator mode $\overline{ACK}$ and $\overline{ATN}$ signals can be asserted.
  In target mode $\overline{REQ}$, $\overline{MSG}$, $\overline{C/D}$ and $\overline{I/O}$ signals can be asserted.
  This instruction is only needed in program I/O transfer.
  On program I/O, see 5-1.

- Deassert SCSI Control
  Prohibits the content of the SCSI bus control register from being output to the SCSI bus.
  Once the "Assert SCSI Control" command is executed, some of the SCSI bus control signals are output from the SCSI bus control register until this command is executed.

- Assert SCSI Data
  Outputs the value of the SCSI data register to the SCSI bus.
  However, data is not output in the following circumstances :

  i) A phase change interrupt (PHC) is generated in initiator mode.
  ii) In initiator receive mode (SCSI bus $\overline{I/O}$ signal is high).
  iii) In target receive mode (SCSI bus $\overline{I/O}$ signal is low).
  iv) The mode is neither initiator nor target.

  This instruction is only needed in program I/O transfer.
  On program I/O, see 5-1.

- Deassert SCSI Data
  Prohibits the value of the SCSI data register from being output to the SCSI bus.
  Once the "Assert SCSI Data" command is executed, the SCSI bus data signals are output from the SCSI data register until this command is executed.

2-2. Commands valid in disconnected status

The following commands are valid only in disconnected status. If any of these commands are issued in any other state, the CIP bit and the content of the command register are cleared immediately.

- Reselect
  This command executes arbitration/reselection from disconnected status.
  When this command is executed, the CXD1185AQ switches to the target mode.
  Before issuing this command, the owner ID (OID2-0) and target ID (TID 2-0) values must be written in the SCSI ID register.

- Select without $\overline{ATN}$
  This command executes arbitration/selection from disconnected status.
  When this command is executed, the CXD1185AQ switches to the initiator mode. Before issuing this command, the owner ID (OID2-0) and target ID (TID2 -0) values must be written in the SCSI ID register.

- Select with $\overline{ATN}$
  This command executes arbitration/selection from disconnected status.
  During selection the $\overline{ATN}$ signal is driven on the SCSI bus.
  When this command is executed, the CXD1185AQ switches to the initiator mode. Before issuing this command, the owner ID (OID2-0) and target ID (TID2-0) values must be set in the SCSI ID register. If, after this command is executed, message-out phase is to be terminated, the "Deassert $\overline{ATN}$" command must be executed prior to the transfer of the last message byte.

• Enable Selection/Reselection
Activates selection/reselection interrupts.
When this command is executed, the FNC bit is set immediately and the contents of the CIP bit and command register are cleared. Once this command is executed, RSL/SWA/SWOA interrupts (in interrupt request 1 register) are set during selection/reselection phase. When one of the selection/reselection is executed this will occur before the FNC interrupt.

Selection/reselection is also enabled after the following events.
- ○ Hardware reset
- ○ Execution of "Reset Chip"
- ○ Assertion of SCSI bus $\overline{RST}$ signal
- ○ Disconnect in initiator mode

• Disable Selection/Reselection
Prohibits any response to selection/reselection.
Once this command is executed, the RSL/SWOA/SWA interrupts in interrupt request register 1 will not be generated.

2-3. Commands valid in target status
The following commands are valid only in target status.
If any of these commands are issued in any other state, the CIP bit and the Content of the command register are cleared immediately.
In the case of data send commands, the transfer data must not be written before the command is written in the command register and the necessary SCSI phase change is confirmed by software. In target mode, handshaking on the SCSI bus is terminated under the following conditions :

1. The $\overline{REQ}$ signal is in any state and if :
   - ○ a hardware reset is performed.
   - ○ the "Reset Chip" command is executed.
   - ○ the SCSI bus $\overline{RST}$ pin is driven.

2. The command completes with $\overline{REQ}$ inactive if :
   - ○ a parity error is generated on the SCSI bus or the data bus. (However, this is not the case if the mode register HDPE and HSPE bits are set to "0".)
   - ○ the SCSI bus $\overline{ATN}$ signal is driven. (However, this is not the case if the mode register HATN bit is set to "0".)
   - ○ while the transfer byte counter is in use :
     the DMA bit is set to "1", the status register TRBZ bit is set to "1" and the FIFO status register FIE bit is set to 1, or in receive mode, the DMA bit is set to "0" and the status register TRBZ bit is set to "1".
   - ○ While executing a single byte transfer :
     the mode is send and the FIE bit is set to "1",
     or the mode is receive and FIFO status register bits FC3-FC0 are all set to "1".

3. Handshaking is temporarily interrupted with $\overline{REQ}$ inactive if :
   - ○ while the transfer byte counter is in use :
     the mode is send and the FIFO status register FIE bit is set to "1",
     or the mode is receive and the FIFO status register FIF bit is set to "1".
   - ○ during synchronous transfer, the difference in the number of $\overline{REQ}$s and $\overline{ACK}$s reaches the offset specified in the synchronous transfer register.
   - ○ the mode is receive, during synchronous transfer, the number of FIFO bytes remaining is fewer than the offset specified in the synchronous transfer register.

- Send Message
  The CXD1185AQ changes the phase to Message In by making the SCSI bus $\overline{MSG}$ and $\overline{I/O}$ signals active and the $\overline{C/D}$ signal inactive. The message bytes are then sent.
  If there is more than one message byte or if the message must be sent all at once, the transfer byte counter must be used.

- Send Status
  The CXD1185AQ changes the phase to Status and sends the status byte to the initiator.
  It makes the SCSI bus $\overline{I/O}$ and $\overline{C/D}$ signals active and the $\overline{MSG}$ signal inactive.

- Send Data
  The CXD1185AQ changes the phase to Data In and sends the data bytes to the initiator.
  It makes the SCSI bus $\overline{I/O}$ signal active and $\overline{MSG}$ and $\overline{C/D}$ signals inactive.
  If more than one data byte must be sent all at once, the transfer byte counter must be used.

- Disconnect
  Makes all SCSI signals inactive, except for the $\overline{RST}$ signal.

- Receive Message Out
  The CXD1185AQ changes the phase to Message In and receives the message bytes from the initiator.
  It makes the SCSI bus $\overline{MSG}$ signal active and the $\overline{I/O}$ and $\overline{C/D}$ signals inactive.
  If there is more than one message byte or if the message must be received all at once, the transfer byte counter must be used.

- Receive Command
  The CXD1185AQ changes the phase to Command and receives the command bytes from the initiator.
  It makes the SCSI bus $\overline{C/D}$ signal active and the $\overline{MSG}$ and $\overline{I/O}$ signals inactive.
  If the command bytes must be received all at once, the transfer byte counter must be used.

- Receive Data
  The CXD1185AQ changes the phase to Data Out and receives the data bytes from the initiator.
  It makes the SCSI bus $\overline{MSG}$, $\overline{C/D}$ and $\overline{I/O}$ signals inactive and received the data bytes.
  If more than one data byte must be received all at once, the transfer byte counter must be used.

2-4. Commands valid in initiator status

The following commands are valid only in initiator status.
If any of these commands are issued in any other state, the CIP bit and the content of the command register are cleared immediately.
In the case of data send commands, the transfer data must not be written before the command is written in the command register.
Once the execution of a transfer command is commenced in initiator mode, handshaking on the SCSI bus is terminated under the following conditions:

1. The $\overline{ACK}$ signal is in any status and if :
   - ○ a hardware reset is performed.
   - ○ the "Reset Chip" command is executed.
   - ○ the SCSI bus $\overline{RST}$ pin is driven.

2. The command completes with $\overline{ACK}$ inactive if :
   - ○ phase change occurs and PHC bit in interrupt request register 2 is set to "1".
     If this is the case and the DMA bit is set to "1", the DRQ signal also remains inactive.
   - ○ while the transfer byte counter is in use :
     the DMA bit is set to "1", the status register TRBZ bit is set to "1" and the FIFO status register FIE

bit is set to 1, or in receive mode, the DMA bit is set to"0" and the status register TRBZ bit is set to "1".

- ○ while executing a single byte transfer :
  the mode is send and the FIE bit is set to 1,
  or the mode is receive, FIFO status register FIE bits FC3-FC0 are all set to "1".

3. The command completes with $\overline{ACK}$ active if :
   - ○ the mode is receive and a parity error occurs on the SCSI bus. (However, this is not the case if the mode register HSPE bit is set to "0".)
   - ○ status is message-in phase, the TRBE bit is set to "0", the $\overline{REQ}$ signal is active and a 1-byte message is received.

   Note that in the above two cases the "Deassert $\overline{ACK}$" command must be executed afterwards.

4. Handshaking is temporarily interrupted with $\overline{ACK}$ inactive if :
   - ○ while the transfer byte counter is in use :
     the mode is send and the FIFO status register FIE bit is set to "1".
   - ○ during synchronous transfer , the difference in the number of $\overline{REQ}$s and $\overline{ACK}$s reaches the offset specified in the synchronous transfer register.
   - ○ during synchronous transfer, the number of FIFO bytes remaining is fewer than the offset specified in the synchronous transfer register.

5. Handshaking is temporarily interrupted with $\overline{ACK}$ active if :
   - ○ while the transfer byte counter is in use :
     the mode is receive and the FIFO status register FIF bit is set to "1".

- Transfer Information
  In the initiator mode, causes data transfer to take place.

- Transfer Pad
  In the initiator mode, causes data transfer to take place.
  Note that unlike "Transfer Information", the data output by the CXD1185AQ are all "0"s and parity generation is not performed.
  In addition, no parity check is performed on any data input to the CXD1185AQ.
  Except for these two exceptions, this command is identical to the "Transfer Information" command.

- Deassert $\overline{ACK}$
  Makes the SCSI $\overline{ACK}$ signal inactive.

- Assert $\overline{ATN}$
  Makes the SCSI $\overline{ATN}$ signal active.

- Deassert $\overline{ATN}$
  Makes the SCSI $\overline{ATN}$ signal inactive. After executing the "Select with $\overline{ATN}$" or "Assert $\overline{ATN}$" command, the SCSI bus $\overline{ATN}$ signal remains active until this command is executed.

3. Reset Operation

There are four initializing methods for the CXD1185AQ:

- hardware reset
- execution of the "Reset Chip" command
- assertion of $\overline{RST}$ signal on the SCSI bus
- disconnection

3-1. Hardware reset

This returns the CXD1185AQ to its initial status.
However, environment setting register bit 1 (FS1) is set to "1", making the initial clock division ratio to "4".
All of the internal circuits are also initialized.

3-2. Execution of the "Reset Chip" command

CXD1185AQ can be initialized by "Reset Chip" command (command code "01"). This command is effective regardless of the CIP bit in the status register.
This command resets all registers with the exception of the environment setting register.
All read only registers except for bits 7 and 6 of the status register and the SCSI control monitor register are cleared.
Since the "Reset Chip" command clears all write registers, any SCSI bus signal it used to drive will also be cleared.

3-3. Assertion of $\overline{RST}$ signal on the SCSI bus

When the SCSI bus $\overline{RST}$ signal is active, signals on the SCSI bus being driven by the CXD1185AQ are made inactive with the exception of the $\overline{RST}$ pin.
Bits 4 and 3 (INIT and TARG bits) are also cleared.

3-4. Disconnection

If the CXD1185AQ is operating in initiator mode and a disconnect interrupt is generated, a reset identical to the one in 3-3 takes place.

4. Interrupt Operation

In this section various interrupts, generated by the CXD1185AQ, are discussed in greater detail. If the internal interrupt conditions of the CXD1185AQ are satisfied, "1"s are written to the appropriate bits in interrupt request registers 1 and 2 and the MIRQ bit in the status register. IRQ pin becomes active only if the interrupt is authorised in the interrupt authorization registers.

4-1. Arbitration interrupts

When a selection command is executed, the CXD1185AQ waits for bus free. Once bus free is detected it outputs the $\overline{BSY}$ signal and the owner ID to the SCSI bus and enters arbitration. If, during arbitration, another device with higher priority enters arbitration or if the $\overline{SEL}$ signal is driven on the SCSI bus, arbitration fails and ARBF is set to "1". The FNC bit is also set a while later. If arbitration is successful it enters selection phase.

4-2. Interrupts when selected/reselected

After "Enable Selection /Reselection" is executed, if the owner ID and the $\overline{SEL}$ signal appear on the SCSI bus, SWOA bit is set to "1". If $\overline{ATN}$ signal also appear at the same time, SWA bit is set instead. If $\overline{I/O}$ signal appears instead of $\overline{ATN}$ signal, then, RSL is set.

4-3. Interrupts when selection/reselection command is executing

CXD1185AQ enters arbitration and after obtaining the right to use the SCSI bus it enters selection/reselection phase by sending the target ID, the owner ID and $\overline{SEL}$ signal onto the bus. At this point, the value of the selection/reset timer register is loaded into the hardware timer (not user accessible) and decrementing begins. Note that TMSL bit in the mode register must be "1" for the loading to take place. If there is no response from the target device by the time the hardware timer reaches "0", selection time over occurs and the STO bit is set to "1" and, afterward, the FNC bit is set to "1".

4-4. Data transfer phase interrupts

- The RMSG and PHC bits are valid interrupts only when INIT bit (status register bit 4) is set to "1". Also, the DATN bit is valid only when the TARG bit (status register bit 3) is set to "1". The SPE and DPE bits are valid both in initiator and target modes.
- The RMSG bit is set to "1", if, in initiator mode, the target device activates $\overline{REQ}$ after changing the SCSI bus phase to either Message-In or Message-Out. If the message is of multiple byte, it is set each time $\overline{REQ}$ is activated.
- The PHC bit is set to "1", if, in initiator mode, the target device activates $\overline{REQ}$ after changing the SCSI bus phase. If the new phase is either Message-In or Message-Out, RMSG bit is also set to "1".
- The DATN bit is set to "1", if, in target mode, the initiator asserts $\overline{ATN}$ on the SCSI bus. Once the interrupt request register 2 is read by the CPU the bit is cleared even if $\overline{ATN}$ continues to be active.
- The SPE bit is set when a parity error is detected on the SCSI bus during receive mode data transfer in both initiator and target mode. In initiator mode, it is set on receiving the $\overline{REQ}$. In target mode it is set on receiving the $\overline{ACK}$. The SPE bit is also set if parity error is detected during selection/reselection.
- DPE bit is set when a parity error is detected on the data bus while writing data into FIFO. It is set at the rise of the FIFO write signal, $\overline{WED}$. This bit is valid only if the DPEN bit in the environment setting register is set to "1". If the SDPM bit in the environment register is "1", even parity check is carried out. Otherwise odd parity check is carried out.

4-5. Other interrupts

- The SRST bit is set to "1" when the SCSI bus $\overline{RST}$ signal becomes active. It is also set if the "Assert $\overline{RST}$" command is executed and the CXD1185AQ drives the $\overline{RST}$ pin.
- The DCNT bit is set to "1" if the CXD1185AQ is operating in the initiator mode and the target device makes the $\overline{BSY}$ signal on the SCSI bus inactive. Normally, in initiator mode, this bit is set at the end of a series of SCSI operation when the SCSI bus phase becomes bus free.

5. Data Transfer

In this section procedures for transferring data to and from the CXD1185AQ is described. Data can be transferred between the CPU and the CXD1185AQ in the following three ways:

1. Program I/O transfer
2. CPU I/O transfer
3. DMA transfer

5-1. Program I/O transfer

This method is used to transfer data between the CPU bus and the CXD1185AQ. The CPU manages SCSI handshaking entirely through software. By issuing the "Assert SCSI Control" and "Assert SCSI Data" commands, all of the SCSI bus bits can be software controlled. After the above two commands are issued, values can be written to the SCSI bus control register and the SCSI data register to carry out the SCSI handshake.

When the "Assert SCSI Data" command is issued, the CXD1185AQ internal FIFO counter is fixed at "0". As a result, only one byte of data can be received by the data register. Reading the SCSI data register results in reading the SCSI data bus directly. If the CXD1185AQ is in neither initiator nor target mode (status register bits 4 and 3 both set to "0"), none of the bits in the SCSI bus control register can be output to the SCSI bus except ABSY and ASEL. If the CXD1185AQ is in initiator mode, the AACK and AATN bits are output to the SCSI bus. In the target mode, the AMSG, ACD, AIO and AREQ bits are output.

When phase change (PHC) interrupt occur in initiator mode, output to the SCSI data bus is inhibited. In such case, read the SCSI control monitor register and watch the phase in the SCSI control register with that of the SCSI bus. When "Assert SCSI Control" instruction is executed in target mode, pins on the SCSI bus, except $\overline{BSY}$, are released.

The phase can be controlled by setting appropriate values to the SCSI bus control register. The contents of the SCSI control register and/or SCSI data register are output continually after "Assert SCSI Control" and/or "Assert SCSI data". Therefore, when program I/O transfer is completed the "Deassert SCSI Control "or" Deassert SCSI Data" command must be written to the command register.

5-2. CPU I/O transfer

This method is used to transfer data between the CPU bus and the CXD1185AQ without using DMA. Transfer commands can be issued when the CPU is in either the initiator or the target mode. When issuing these commands, command register bit 5 (DMA) must be set to "0".

- Outputting data to the SCSI bus
  During the transfer, the CPU must monitor the FIFO status and make sure that it does not attempt to write to the FIFO when it is full (FIFO is full when FIF bit in the FIFO status register is "1") (*). In target mode, after issuing the transfer command, the CPU must check that the SCSI bus phase is changed to the appropriate phase, by software, before any transfer data is written.

  (*) Before writing a value to the data register a transfer command must be written to the command register.

- Reading data from the SCSI bus
  After a transfer command is written to the command register, the CPU must monitor the FIE bit in the FIFO status register so as to make sure that it does not attempt to read an empty FIFO. The CPU must monitor the FNC bit in the status register to detect the end of transfer. The CPU, at the end of the transfer, must continue to read any remaining data in the FIFO.

5-3. DMA transfer

This method is used to transfer data between the Data bus and the CXD1185AQ. Transfer commands can be issued when the CPU is in either the initiator or the target mode. When issuing commands command register bits 5 (DMA) and 4 (TRBE) must be set to "1". When a transfer is initiated the DRQ pin (Pin 43) becomes active. Then, when the $\overline{\text{DACK}}$ pin (Pin 44) becomes active, the DRQ pin becomes inactive (when mode register bit 0 (BDMA) is set to "0") and one byte of data is either written to or read from the FIFO. If the environment setting register bit 5 (DPEN) is set to "1", the data bus parity is calculated from the DP pin (Pin 55). During reads the parity bit is generated, and during writes parity bit check takes place. During DMA transfer, the CPU bus and data register are cut off. Hence, data register reads/writes from the CPU are ignored.

6. Programming Overview

The CXD1185AQ supports SCSI phase level commands. As a result, when it is operating it is possible to perform programming without imposing a burden on the software. In this section actual methods for programming CXD1185AQ are introduced along with an explanation of all SCSI phases, assuming that the CXD1185AQ is in the initiator mode.

〈 Initial settings 〉

The CXD1185AQ is completely initialized when the power is turned on or after a hardware reset. Therefore, the following initial settings must be performed.

① Environment setting register initialization
The enviroment setting register is set to an initial value and initial clock division ratio of "4". Therefore, a new appropriate value must be written to match the external clock frequency as described in section 1-5. If required, "1"s must be written to the other bits at the same time.

② "Reset Chip" command execution

The new clock division ratio becomes valid only after executing the "Reset Chip" command. (The other bits are valid as soon as they are written.) Therefore, if the clock division ratio is to be changed, the "Reset Chip" command must be executed after changing the FSI and FSO bits in the environment setting register.

〈 Arbitration/selection execution 〉

③ SCSI ID setting

The owner ID and target ID must be written to the SCSI ID register to prepare for selection.

④ Arbitration/selection

Write "1"s to some of the bits of interrupt authorization registers 1 and 2 (ARBF, STO, FNC, etc.) as required. Write "Select with $\overline{ATN}$" command into the command register. If message-out phase is not necessary after selection, instead, write "Select without $\overline{ATN}$" command. In this example "Select with $\overline{ATN}$" is assumed. Wait for the CIP bit in the status register to become "1" and read the interrupt request registers.

If arbitration failed and ARBF bit is "1", repeat ④. Normally, if selection time over occurs and STO bit set to "1", "Assert $\overline{RST}$" command is executed.

〈 Message-out phase execution 〉

⑤ Switching to the message-out phase

Wait until the target device switches the SCSI bus to the message-out phase (PHC bit set to "1").

⑥ Halting $\overline{ATN}$ signal drive

Execute "De-assert $\overline{ATN}$" command to inactivate the $\overline{ATN}$ signal on the SCSI bus.

⑦ Sending message byte

Confirm that the CIP bit is "0" in the status register. Write "Transfer Information" command to the command register (DMA bit and TRBE bit are set to "0"s for a single byte message). Write the message byte into the SCSI data register. After confirming that the CIP bit is to "0", read interrupt request registers 1 and 2.

〈 Command phase execution 〉

⑧ Switching to the command phase

Wait until the target device switches the SCSI bus to the command phase (PHC bit set to "1").

⑨ Command send

Set the number of command bytes in the transfer byte counter. Write "Transfer Information" command into the command register. (this time set the TRBE bit to "1" and DMA bit to "0"). Write the command bytes into the SCSI data register. After confirming that the CIP bit is set to "0", read interrupt request registers 1 and 2.

〈 Data-in phase execution 〉

⑩ Switching to the data-in phase
Wait until the target device switches the SCSI bus to the data-in phase (PHC bit set to "1").

⑪ Data receive
Set the number of transfer data bytes in the transfer byte counter. Write "Transfer Information" command into the command register (with both DMA bit and TRBE bit set to "1"). Note that programming of DMA controller is also required before starting DMA transfer. After confirming that the CIP bit is set to "0", read interrupt request registers 1 and 2.

〈 Status phase execution 〉

⑫ Switching to the status phase
Wait until the target device switches the SCSI bus to the status phase (PHC bit set to "1").

⑬ Status receive
Write "Transfer Information" command in the command register (both DMA bit and TRBE bit are "0"). After confirming that the CIP bit is set to "0", read interrupt request registers 1 and 2.
The status byte is read from the data register.

〈 Message-in phase execution 〉

⑭ Switching to the message-in phase
Wait until the target device switches the SCSI bus to the message-in phase (PHC bit set to "1").

⑮ Message receive
Write "Transfer Information" command in the command register (both DMA bit and TRBE bit are "0"). After confirming that the CIP bit is set to "0", read interrupt request registers 1 and 2. The message byte is read from the data register.

⑯ Halting $\overline{\text{ACK}}$ signal drive
Message-In is exceptional in that after the message byte is read, $\overline{\text{ACK}}$ is not inactivated automatically. "Deassert $\overline{\text{ACK}}$" command must be executed to inactivate $\overline{\text{ACK}}$ signal.
Write " Deassert $\overline{\text{ACK}}$" command in the command register. After confirming that the CIP bit is "0", read the interrupt request registers.

〈 Disconnect 〉

⑰ Wait until the DCNT bit is set to "1".
All SCSI phases are covered in ① - ⑰ above. If a disconnect message is sent from the target device when in the data phase, the status phase is skipped and processing continues with the message in phase. When reselection is performed from the target device (RSL bit set to "1"), it is necessary to wait until the FNC bit is set to "1". Then read the monitor SCSI control register and perform the processing appropriate for the current SCSI phase.

Appendix A

Register Summary

READ

	7	6	5	4	3	2	1	0	Register
R0	MRST	MDBP		INIT	TARG	TRBZ	MIRQ	CIP	Status register
R1									Data register
R2				STO	RSL	SWA	SWOA	ARBF	Interrupt request register 1
R3	FNC	DCNT	SRST	PHC	DATN	DPE	SPE	RMSG	Interrupt request register 2
R4	MBSY	MSEL	MMSG	MCD	MIO	MREQ	MACK	MATN	SCSI control monitor register
R5	FIE			FIF	FC3	FC2	FC1	FC0	FIFO status register
R6	TID2	TID1	TID0			OID2	OID1	OID0	SCSI ID register
R7									Transfer byte counter (low)
R8									Transfer byte counter (middle)
R9									Transfer byte counter (high)
RA				STO	RSL	SWA	SWOA	ARBF	Interrupt authorization register 1
RB	FNC	DCNT	SRST	PHC	DATN	DPE	SPE	RMSG	Interrupt authorization register 2
RC	HDPE	HSPE	HATN	TMSL	SPHI			BDMA	Mode register
RD	TPD3	TPD2	TPD1	TPD0	TOF3	TOF2	TOF1	TOF0	Synchronous transfer register
RE	ABSY	ASEL	AMSG	ACD	AIO	AREQ	AACK	AATN	SCSI bus control register
RF	PCN3	PCN2	PCN1	PCN0	PRT3	PRT2	PRT1	PRT0	I/O port register

WRITE

	7	6	5	4	3	2	1	0	Register
R0	CAT1	CAT0	DMA	TRBE	CMD3	CMD2	CMD1	CMD0	Command register
R1									Data register
R2									⟨ * ⟩
R3	DIFE	SDPM	DPEN	SIRM			FS1	FS0	Environment setting register
R4									Selection/reset timer register
R5									⟨ * ⟩
R6	SID2	SID1	SID0			OID2	OID1	OID0	SCSI ID register
R7									Transfer byte counter (low)
R8									Transfer byte counter (middle)
R9									Transfer byte counter (high)
RA				STO	RSL	SWA	SWOA	ARBF	Interrupt authorization register 1
RB	FNC	DCNT	SRST	PHC	DATN	DPE	SPE	RMSG	Interrupt authorization register 2
RC	HDPE	HSPE	HATN	TMSL	SPHI			BDMA	Mode register
RD	TPD3	TPD2	TPD1	TPD0	TOF3	TOF2	TOF1	TOF0	Synchronous transfer register
RE	ABSY	ASEL	AMSG	ACD	AIO	AREQ	AACK	AATN	SCSI bus control register
RF	PCN3	PCN2	PCN1	PCN0	PRT3	PRT2	PRT1	PRT0	I/O port register

⟨ * ⟩ No register assigned to this address.

Appendix B

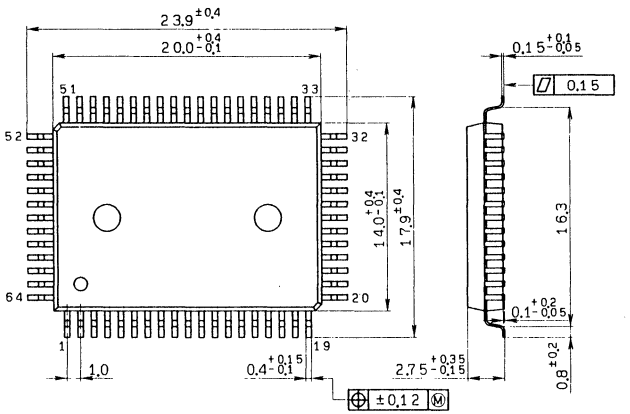
Command Summary

Category	DMA	TRBE	Command code	Command
0 0	0	0	0 0 0 0	No Operation
	0	0	0 0 0 1	Reset Chip
	0	0	0 0 1 0	Assert $\overline{RST}$
	0	0	0 0 1 1	Flush FIFO
	0	0	0 1 0 0	Assert SCSI Control
	0	0	0 1 0 1	Deassert SCSI Control
	0	0	0 1 1 0	Assert SCSI Data
	0	0	0 1 1 1	Deassert SCSI Data
0 1	0	0	0 0 0 0	Reselect
	0	0	0 0 0 1	Select without $\overline{ATN}$
	0	0	0 0 1 0	Select with $\overline{ATN}$
	0	0	0 0 1 1	Enable Selection/Reselection
	0	0	0 1 0 0	Disable Selection/Reselection
1 0	*	*	0 0 0 0	Send Message
	*	*	0 0 0 1	Send Status
	*	*	0 0 1 0	Send Data
	0	0	0 0 1 1	Disconnect
	*	*	0 1 0 0	Receive Message Out
	*	*	0 1 0 1	Receive Command
	*	*	0 1 1 0	Receive Data
1 1	*	*	0 0 0 0	Transfer Information
	*	*	0 0 0 1	Transfer Pad
	0	0	0 0 1 0	Deassert $\overline{ACK}$
	0	0	0 0 1 1	Assert $\overline{ATN}$
	0	0	0 1 0 0	Deassert $\overline{ATN}$

〈 * 〉 Don't care.
However, if the DMA bit is set to "1", the TRBE bit is always also set to "1".

Package Outline Unit: mm

64pin QFP (Plastic) 1.5g



SONY NAME	QFP-64P-L01
EIAJ NAME	*QFP064-P-1420-A
JEDEC CODE	