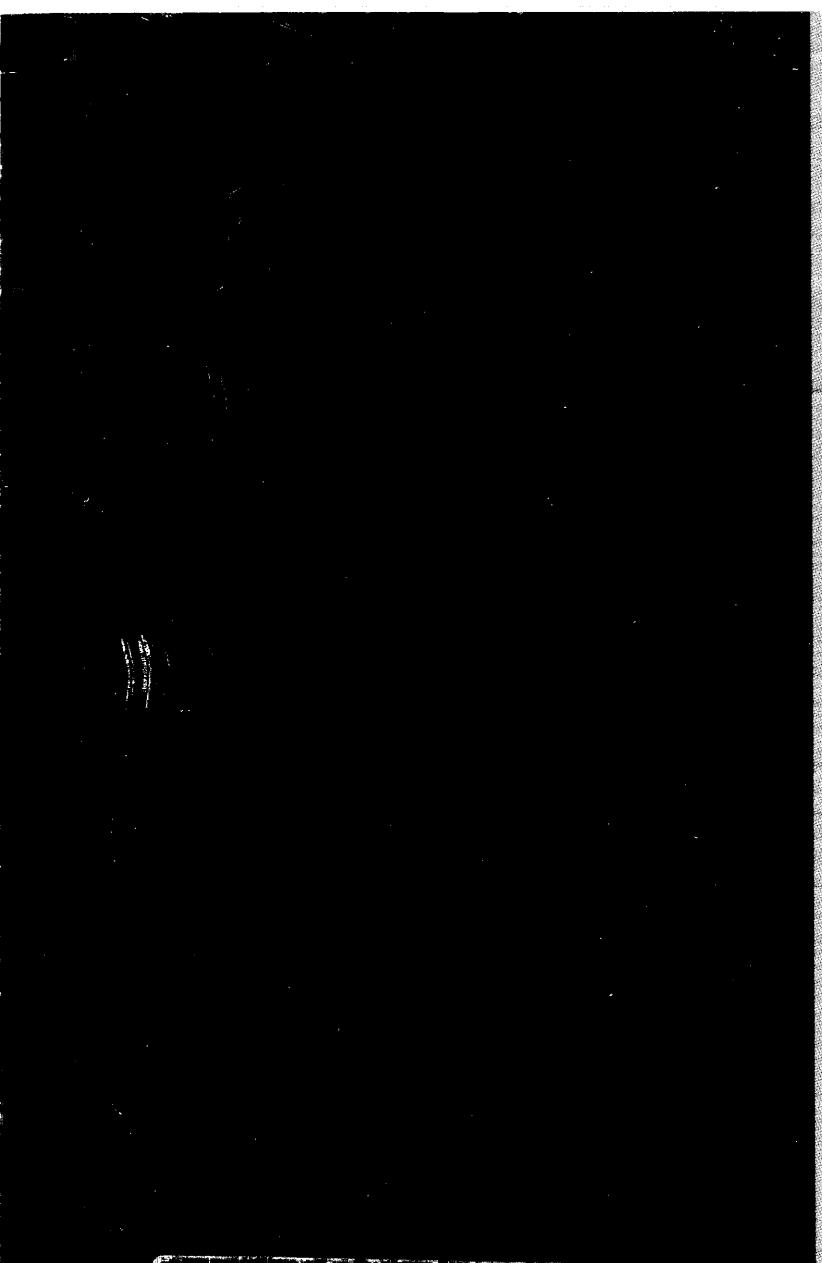
STANDARD MICROSYSTEMS CORPORATION

DATA CATALOG 1983



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PART NUMBER INDEX

FUNCTIONAL INDEX

Data Communication Products

Part Number	Name	Description	Max Baud Rate	Power Supplies	Package	Page
COM 1553A	MIL-STD-1553A UART	MIL-STD-1553 (Manchester) Interface Controller	1 MB	+5	40 DIP	27-42
COM 1553B	MIL-STD-1553B UART	MIL-STD-1553B (Manchester) Interface Controller	1 MB	+5	40 DIP	43-58
COM 1671	ASTRO	Asynchronous/Synchronous Transmitter/Receiver, Full Duplex, 5-8 data bit, 1X or 32X clock	1 MB	+5, −5, +12	40 DIP	59-74
COM 1863	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit, enhanced distortion margin	62.5 KB	+5	40 DIP	75-82
COM 2017	UART	Universal Asynchronous Receiver Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit	25 KB	+5, −12	40 DIP	83-90
COM 2017H	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit	40 KB	+5, −12	40 DIP	83-90
COM 2449	RS449-USART	RS 449 Compatible Universal Synchronous/Asynchronous Receiver/Transmitter	1 MB	+5	40 DIP	91-106
COM 2502	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 2 stop bit	25 KB	+5, −12	40 DIP	83-90
COM 2502H	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 2 stop bit	40 KB	+5, −12	40 DIP	83-90
COM 2601	USRT	Universal Synchronous Receiver/ Transmitter, STR, BSC, Bi-sync compatible	250 KB	+5, −12	40 DIP	107-114
COM 2651	USART/PCI	Universal Synchronous/Asynchronous Receiver/Transmitter, Full Duplex, 5-8 data bits; 1, 1½, 2 stop bit, 1X, 16X, 64X clock	1 MB	+5	28 DIP	115-126
COM 2661	USART/EPCI	Universal Synchronous/Asynchronous Receiver/Transmitter, Full Duplex, 5-8 data bits; 1, 1½, 2 stop bit, 1X, 16X, 64X clock	1 MB	+5	28 DIP	127-138
COM 5025	Multi-Protocol USYNRT	SDLC, HDLC, ADCCP, Bi-sync, DDCMP compatible, automatic bit stuffing/ stripping, frame detection/generation, CRC generation/checking, sync detection	1.5 MB	+5, +12	40 DIP	139-150
COM 7210	GPIB Interface Controller	Intelligent Interface Controller for GPIB (IEEE-488-1978)	8 MHz	+5	40 DIP	151-152
COM 8004	32 Bit CRC Generator/ Checker	Companion device to COM 5025 for 32 bit CRC	2.0 MB	+5	20 DIP	153-158
COM 8017	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit	40 KB	+5	40 DIP	159-166
COM 8018	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit, enhanced distortion margin	62.5 KB	+5	40 DIP	75-82
COM 8251A	USART	Universal Synchronous/Asynchronous Receiver/Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit	64 KB (sync) 9.6 KB (async)	+5	28 DIP	167-182
COM 8502	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 2 stop bit	40 KB	+5	40 DIP	159-166
COM 9004	IBM 3274 Receiver/ Transmitter	IBM 3274 Compatible receiver/ transmitter	2.36 MB	+5, ±12	40 DIP	183-190
COM 9026	LANC	Local Area Network Controller for token pass systems	2.5 MB	+5	40 DIP	191-206

Baud Rate Generator

All Baud Rate Generators are programmable dividers capable of providing 16 output frequencies* for UARTs or USARTs from either an on-chip crystal oscillator or an external frequency input. "T" versions utilize an external frequency input only. Dual Baud Rate Generators provide two output frequencies simultaneously for full duplex communications.

Baud Rate Generators providing all standard baud rates from various popular crystal frequencies are available. In addition the baud rate generator may be custom mask programmed for other divisors.

*except as noted

Part Number	Description	Features	Power Supplies	Package	Page
COM 5016	Dual Baud Rate Generator	On-chip oscillator or external frequency input	+5, +12	18 DIP	209-210
COM 5016T(1)	Dual Baud Rate Generator	External frequency input	+5, +12	18 DIP	209-210
COM 5026	Single Baud Rate Generator	On-chip oscillator or external frequency input	+5, +12	14 DIP	211-212
COM 5026T(1)	Single Baud Rate Generator	External frequency input	+5, +12	14 DIP	211-212
COM 5036	Dual Baud Rate Generator	COM 5016 with additional output of input frequency ÷ 4	+5, +12	18 DIP	213-214
COM 5036T(1)	Dual Baud Rate Generator	COM 5016T with additional output of input frequency ÷ 4	+5, +12	18 DIP	213-214
COM 5046	Single Baud Rate Generator	COM 5026 with additional output of input frequency ÷ 4	+5, +12	14 DIP	215-220
COM 5046T(1)	Single Baud Rate Generator	COM 5026T with additional output of input frequency ÷ 4	+5, +12	14 DIP	215-220
COM 8046	Single Baud Rate Generator	32 baud rates; 1X, 16X, 32X clock outputs; single +5 volt supply	+5	16 DIP	221-222
COM 8046T(1)	Single Baud Rate Generator	COM 8046 with external frequency input only	+5	16 DIP	221-222
COM 8116	Dual Baud Rate Generator	Single +5 volt version of COM 5016	+5	18 DIP	223-224
COM 8116T(1)	Dual Baud Rate Generator	Single +5 volt version of COM 5016T	+5	18 DIP	223-224
COM 8126	Single Baud Rate Generator	Single +5 volt version of COM 5026	+5	14 DIP	225-226
COM 8126T(1)	Single Baud Rate Generator	Single +5 volt version of COM 5026T	+5	14 DIP	225-226
COM 8136	Dual Baud Rate Generator	Single +5 volt version of COM 5036	+5	18 DIP	227-228
COM 8136T(1)	Dual Baud Rate Generator	Single +5 volt version of COM 5036T	+5	18 DIP	227-228
COM 8146	Single Baud Rate Generator	Single +5 volt version of COM 5046	+5	14 DIP	229-232
COM 8146T(1)	Single Baud Rate Generator	Single +5 volt version of COM 5046T	+5	14 DIP	229-232

Keyboard Encoder

Part Number	No. of Keys	Modes	Features	Standard Fonts Suffix	Standard Fonts Description	Power Supplies	Package	Page
KR-2376 XX(1)	88	3	2 Key Rollover	-ST	ASCII	+5, −12	40 DIP	429-432
KR-3600 XX(1)	90	4	2 Key or N Key Rollover	-ST -STD -PRO	ASCII ASCII Binary Sequential	+5, −12	40 DIP	433-440

(1)May be custom mask programmed

Printer

CHARACTER GENERATOR

Part Number	Description	Scan	Max Access Time	Power Supplies	Package	Page
CG 4103[1]	5 x 7 x 64	Column	1.2 μsec	+5, −12 or ±12	28 DIP	415-418

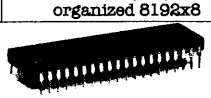
SHIFT REGISTER

Part Number	Description	Feature	Max Clock Freq.	Power Supply	Package	Page
SR 5015-XX[1]	Quad Static Shift Register Mask Programmable Length	Load, Recirculate, Shift Controls,	1 MHz	+5	16 DIP	419-422
SR 5015-80	Quad 80 Bit Static					
SR 5015-81	Quad 81 Bit Static					
SR 5015-133	Quad 133 Bit Static					
SR 5017	Quad 81 Bit	Shift Left/Shift Right, Recirculate Controls, Asynchronous clear	1 MHz	+5	16 DIP	423-426
SR 5018	Quad 133 Bit					

Microprocessor Peripheral

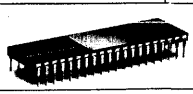
ROM

Part Number	Description	Access Time	Power Supply	Package	Page
ROM 4732[1]	32K ROM; 32,768 bits organized 4096x8	450 nsec	+5	24 DIP	405-408
ROM 36000[1][2]	64K ROM; 65,536 bits organized 8192x8	250 nsec	+5	24 DIP	409-412



FLOPPY DISK/HARD DISK

Part Number	Description	Sector/ Format	Density	Data Bus	Side Select Output	Power Supplies	Package	Page
FDC765	Floppy Disk Controller/ Formatter	Soft	Double	True	Yes	+5	40 DIP	341-342
FDC1761	Floppy Disk Controller/ Formatter (mini-floppy only)	Soft	Double	Inverted	No	+5, +12	40 DIP	343-358
FDC1763	Floppy Disk Controller/ Formatter (mini-floppy only)	Soft	Double	True	No	+5, +12	40 DIP	343-358
FDC1765	Floppy Disk Controller/ Formatter (mini-floppy only)	Soft	Double	Inverted	Yes	+5, +12	40 DIP	343-358
FDC1767	Floppy Disk Controller/ Formatter (mini-floppy only)	Soft	Double	True	Yes	+5, +12	40 DIP	343-358
FDC1791	Floppy Disk Controller/ Formatter	Soft	Double	Inverted	No	+5, +12	40 DIP	359-374
FDC1792	Floppy Disk Controller/ Formatter	Soft	Single	Inverted	No	+5, +12	40 DIP	359-374
FDC1793	Floppy Disk Controller/ Formatter	Soft	Double	True	No	+5, +12	40 DIP	359-374
FDC1794	Floppy Disk Controller/ Formatter	Soft	Single	True	No	+5, +12	40 DIP	359-374
FDC1795	Floppy Disk Controller/ Formatter	Soft	Double	Inverted	Yes	+5, +12	40 DIP	359-374
FDC1797	Floppy Disk Controller/ Formatter	Soft	Double	True	Yes	+5, +12	40 DIP	359-374
FDC3400	Floppy Disk Data Handler	Hard	NA	True	NA	+5, −12	40 DIP	389-396
FDC9216/B	Floppy Disk Data Separator	Soft/Hard	Double	NA	NA	+5	8 DIP	375-378
FDC9229/B	Floppy Disk Data Separator, Head Load Timer, write precompensation generator	Soft/Hard	Double	NA	NA	+5	20 DIP	379-386
HDC7261	Hard Disk Controller	Soft/Hard	Double	True	Yes	+5	40 DIP	387-388



CASSETTE/CARTRIDGE

Part Number	Description	Max Data Rate	Features	Power Supply	Package	Page
CCC 3500	Cassette/Cartridge Data Handler	250K bps	Sync byte detection, Read While Write	+5, −12	40 DIP	397-404

[1]May be custom mask programmed [2] For future release

CRT Display

TIMING CONTROLLERS

Part Number	Description	Features	Display Format	Max Clock	Power Supplies	Package	Page
CRT 5027	provides all of the timing and control for interlaced and non-interlaced CRT display		programmable	4 MHz	+5, +12	40 DIP	239-246
CRT 5037		balanced beam interlace	programmable	4 MHz	+5, +12	40 DIP	239-246
CRT 5047 (1)		fixed format	80 column 24 row	4 MHz	+5, +12	40 DIP	247-248
CRT 5057		line-lock	programmable	4 MHz	+5, +12	40 DIP	239-246
CRT 7220, −1, −2	Graphics Display Controller	Intelligent graphics display controller	1024 x 1024 Pixel	4/5/5.5 MHz	+5	40 DIP	249-251
CRT 9007	CRT video processor and controller	sequential or row-table driven memory	programmable	4 MHz	+5	40 DIP	251-270
CRT 96364A/B	complete CRT proccessor	on-chip cursor and write control	64 column 16 row	1.6 MHz	+5	28 DIP	271-278

VDAC™ DISPLAY CONTROLLERS

Part Number	Description	Display	Attributes	Max Clock	Power Supply	Package	Page
CRT 8002H	Provides complete display and attributes control for alphanumeric and graphics display. Consists of 7 x 11 x 128 character generator, video shift register, latches, graphics and attributes circuits.	7 x 11 dot matrix, wide graphics, thin graphics, on-chip cursor	reverse video blank blink underline strike-thru	25 MHz	+5	28 DIP	293-300
CRT 8002A (1,3)				20 MHz			279-288
CRT 8002B (1,3)				15 MHz			279-288
CRT 8002C (1,3)				10 MHz			279-288

CHARACTER GENERATORS

Part Number	Description	Max Frequency	Power Supply	Package	Page
CRT 7004A (1,4)	7 x 11 x 128 character generator, latches, video shift register	20 MHz	+5	24 DIP	301-306
CRT 7004B (1,4)		15 MHz			
CRT 7004C (1,4)		10 MHz			

ROW BUFFER

Part Number	Description	Max Row Length	Power Supply	Package	Page
CRT 9006-83	8 bit wide serial cascadable single row buffer memory for CRT or printer	83 characters	+5	24 DIP	307-312
CRT 9006-135		135 characters			
CRT 9212	8 bit wide serial cascadable double row buffer memory for CRT or printer	135 characters	+5	28 DIP	313-318

VIDEO ATTRIBUTES CONTROLLERS

Part Number	Description	Display	Attributes	Max Clock	Power Supply	Package	Page
CRT 8021	Provides attributes and graphics control for CRT video displays	Alphanumeric, wide graphics, thin graphics, on-chip cursor	Reverse video, blank, blink, underline, strike-thru	20 MHz	+5	28 DIP	319-326
CRT 9021B	Provides attributes and graphics control for CRT video displays	Alphanumeric, wide graphics, thin graphics, on-chip cursor, double height, double width	Reverse video, blank, blink, underline, intensity	28.5 MHz	+5	28 DIP	327-338

(1) May be custom mask programmed
(2) For future release
(3) Also available as CRT 8002A,B,C — 001 Katakana CRT 8002A,B,C — 003 5X7 dot matrix
(4) Also available as CRT 7004A,B,C — 003 5X7 dot matrix

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SMC CROSS

Description	SMC Part #	AMI	Fairchild	General Instrument	Harris	Intel	Intersil
UART (1½ SB)**	COM 2017	S1883	—	AY 5-1013A	—	—	—
UART (1, 2 SB)**	COM 2502	—	—	AY 5-1013	—	—	—
UART (n-Channel)**	COM 8017	S6850*	—	AY 3-1015	HM6402	—	IM6402
UART (n-Channel)**	COM 8502	—	—	AY 3-1015	HM6403*	8251*	IM6403*
UART (n-Channel)*	COM 1863	S1602	—	—	—	—	—
USRT	COM 2601	S2350*	—	—	—	—	—
ASTRO	COM 1671	—	—	—	—	—	—
PCI	COM 2651	—	—	—	—	—	—
EPCI	COM 2661	—	—	—	—	—	—
USART	COM 8251A	—	—	—	—	8251A	—
Multi-Protocc USYNRT	COM 5025	—	F3846* F6856*	—	—	—	—
USYRT	COM 7210	—	—	—	—	—	—
Dual Baud Rate Gen.	COM 5016/36 COM 8116/36	—	—	—	—	—	—
Single Baud Rate Gen.	COM 5026/46 COM 8126/46	—	F4702*	—	HD4702* HD6405*	—	—
88 Key KB Encoder	KR 2376	—	—	AY 5-2376	—	—	—
90 Key KB Encoder	KR 3600	—	—	AY 5-3600	—	—	—
CRT Controller	CRT 5037	—	—	—	—	8275*	—
Character Generator	CRT 7004	S8564*	—	—	—	—	—
Character Generator	CRT 8002	—	—	—	—	—	—
Graphics Controller	CRT 7220	—	—	—	—	—	—
Character Generator	CG 4100	S8499	—	RO 5-2240S*	—	—	—
Hard Disk Controller	HDC 7261	—	—	—	—	—	—
Shift Register	SR 5015	S2182/3/5	—	—	—	—	—
Microcomputer	MPU 3870	—	F3870-2	—	—	—	—

*Functional Equivalent

**Most UART's are interchangeable; consult the factory

REFERENCE GUIDE

Commodore (MOS Technology)	Mostek	Motorola	National	NEC	Signetics	Solid State Scientific	Synertec	Texas Instruments	Western Digital
—	—	—	MM5303*	μPD369*	—	—	—	TMS6011	TR1602
—	—	—	—	—	2536	—	—	—	TR1402
—	—	MC6850*	—	—	—	SCR1854	—	—	—
—	—	—	—	—	—	—	—	—	TR1983*
—	—	—	—	—	—	—	—	—	TR1863
—	—	—	—	—	—	—	—	—	—
—	—	—	INS1671	—	—	—	—	—	UC1671
—	—	—	INS2651	—	2651	—	—	—	—
—	—	—	—	—	2661	—	SY2661	—	—
—	—	—	INS8251	μPD8251A	—	—	—	—	—
—	—	—	—	μPD379*	2652	SND5025	—	—	SD1933*
—	—	—	—	μPD7210	—	—	—	—	—
—	—	—	—	—	—	—	—	—	BR1941L
—	—	MC14411*	MM5307*	—	—	—	—	—	—
—	—	—	—	—	—	—	—	—	—
MCS1009*	—	—	MM5740*	μPD364*	—	—	—	TMS5001	—
—	MK3807	MC6845*	DP8350*	—	—	SND5027 SND5037	6545*	TMS9927	—
—	—	MCM66700* MC6570*	DM8678*	—	2609*	—	—	—	—
—	—	—	—	—	—	SND8002	—	—	—
—	—	—	—	μPD7220	—	—	—	—	—
MCS1004* MCS2027*	MK2002	MC1132*	M5240	—	—	—	—	TMS4103	—
—	—	—	—	μPD 7261	—	—	—	—	—
—	MK1007*	—	5054*	—	2532*	—	—	TMS3113* TMS3114*	—
—	MK3870/20	—	—	—	—	—	—	—	—

for detailed information on interchangeability.

For Floppy Disk Controllers–See Next Page

FLOPPY DISK CONTROLLERS

Description	SMC Part #	Fujitsu	NEC	Synertec	Western Digital	Intel
Floppy Disk Controller	FDC 1791-02	MB8876	—	SY1791-02	FD 1791-02	—
Floppy Disk Controller	FDC 1792-02	—	—	—	FD 1792-02	—
Floppy Disk Controller	FDC 1793-02	M8877	—	SY1793-02	FD 1793-02	—
Floppy Disk Controller	FDC 1794-02	—	—	—	FD 1794-02	—
Floppy Disk Controller	FDC 1795-02	—	—	—	FD 1795-02	—
Floppy Disk Controller	FDC 1797-02	—	—	—	FD 1797-02	—
Floppy Disk Controller	FDC 1761-02	—	—	—	FD 1761-02	—
Floppy Disk Controller	FDC 1763-02	—	—	—	FD 1763-02	—
Floppy Disk Controller	FDC 1765-02	—	—	—	FD 1765-02	—
Floppy Disk Controller	FDC 1767-02	—	—	—	FD 1767-02	—
Floppy Disk Data Separator	FDC 9216	—	—	—	FD 1691*	—
Floppy Disk Controller	FDC765	—	HPD765	—	—	8272

*Functional Equivalent

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Innovation in microelectronic technology is the key to growth at Standard Microsystems.

Since its inception, Standard Microsystems has been a leader in creating new technology for metal oxide semiconductor large scale integrated (MOS/LSI) circuits.

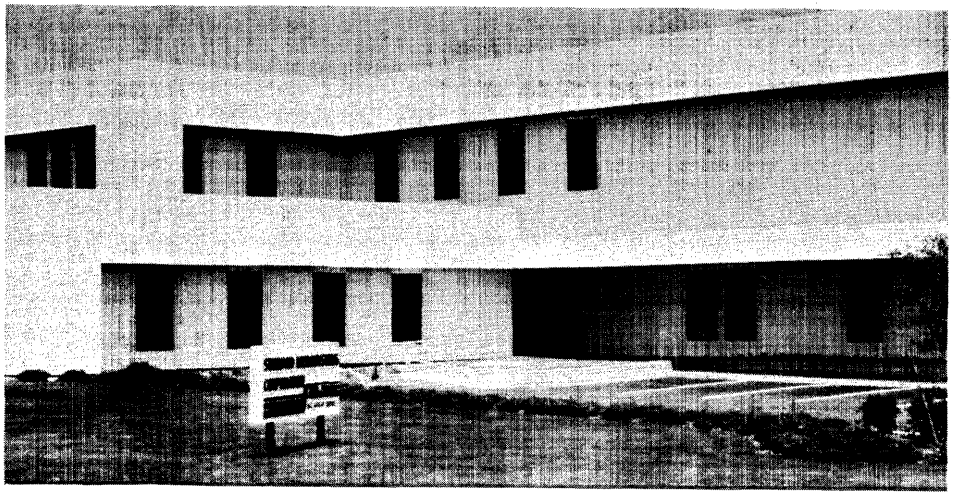
For example, while the first MOS/LSI processes were p-channel, it was recognized very early that an n-channel process would greatly improve switching speeds and circuit density. However, the fundamental problem of parasitic currents needed to be solved. The research and development staff at Standard Microsystems recognized this problem and directed its energy toward the development of its now-famous COPLAMOS® technology. COPLAMOS® defines a self-aligned, field-doped, locally oxidized structure which produces high-speed, high-density n-channel IC's.

In addition, on-chip generation of substrate bias, also pioneered by Standard Microsystems, when added to the COPLAMOS® technology, results in the ability to design dense, high-speed, low-power n-channel MOS integrated circuits through the use of one external power supply voltage.

Again recognizing a need and utilizing its staff of qualified process experts, Standard Microsystems developed the CLASP® process. The need was for fast turnaround, easily programmable semi-custom LSI technology. The development was CLASP®, a process that utilizes ion implantation to define either an active or passive device which allows for the presence of a logical 1 or 0 in the matrix of a memory or logic array. This step is accomplished after all wafer manufacturing steps are performed including metalization and final passiviation layer formation. Thus, the wafer can be tested and stored until customer needs dictate the application, a huge saving in turnaround time and inventory costs.

These innovations in both process and circuit technology have received widespread industry recognition. In fact, many of the world's most prominent semiconductor companies have been granted patent and patent/technology licenses covering various aspects of these technologies. The companies include Texas Instruments, IBM, General Motors, ITT, Western Electric, Mostek, Hitachi and Fujitsu.

Over the past few years, scientists and engineers at Standard Microsystems have been developing a technology to significantly reduce the sheet resistivity of polycrystalline silicon and thereby dramatically decrease internal time constants in MOS devices. Their work has culminated in the successful completion of a program to replace polycrystalline silicon in n-channel MOS devices with an alternate material, titanium disilicide. This has enabled Standard Microsystems to become the first semiconductor manufacturer to market and sell MOS/VLSI circuits which employ a metal silicide to replace the conventional doped polycrystalline silicon layer.



Our engineering staff follows the principle that "necessity is the mother of invention."

This philosophy led Standard Microsystems Corporation to COPLAMOS®, CLASP®, and Titanium Disilicide gate technology, as well as other innovative developments. It also brings companies to us to solve tough problems that other suppliers can't.

But it's a philosophy that involves more than just developing the next generation of MOS/LSI devices.

Such exploration, for example, helped Standard Microsystems recognize the need for communication controllers to handle the latest data communication protocols. As a result, Standard Microsystems was the first to introduce a one-chip LSI controller for HDLC protocols—the COM 5025.

The COM 5025 is so versatile it can actually provide the receiver/transmitter functions for all the standard bit and byte oriented synchronous protocols, including SDLC, HDLC, ADCCP, bi-sync and DDCMP.

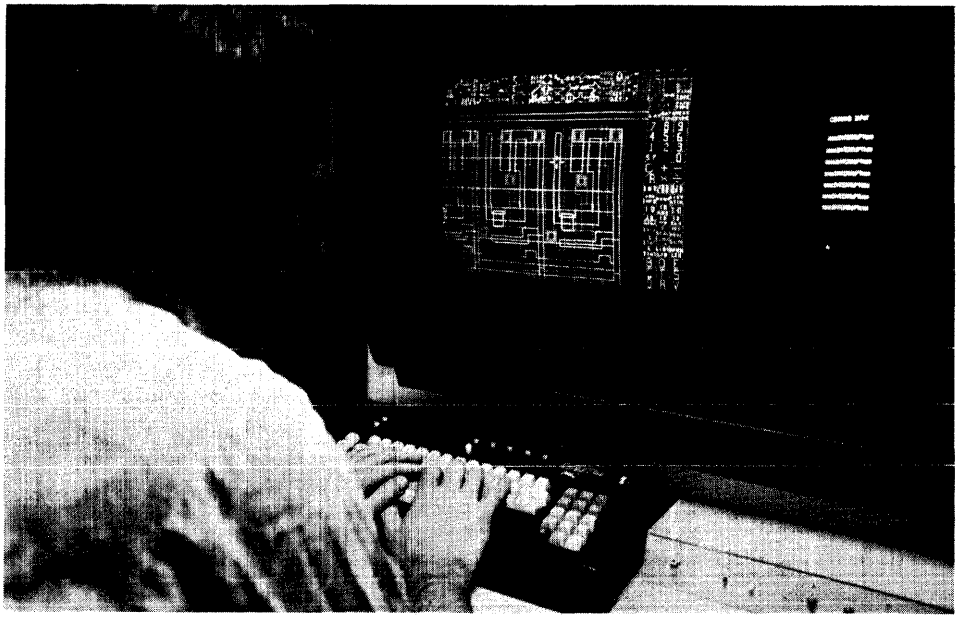
In another area, CRT display systems have traditionally required a great deal of support circuitry for the complex timing, refresh and control functions.

This need led the engineers at Standard Microsystems to develop the CRT 5027 Video Timer and Controller (VTAC®) that provides all these functions on a single chip. This left the display, graphics and attributes control spread over another 20 or 30 SSI, MSI and LSI devices. Standard Microsystems combined all these functions in the CRT 8002 Video Display Attributes Controller (VDAC™). The COPLAMOS® pro ccess was used to achieve a 20 MHz video shift register, and CLASP® was used for fast turnaround of character font changes through its last stage programmability.

So from 60 to 80 integrated circuits, Standard Microsystems reduced display and timing to 2 devices, drastically reducing the cost and size of today's CRT terminals.

Another major achievement was the development of the "next generation" Video Processor And Controller (VPAC™), the CRT 9007. This chip replaces up to 80 SSI and MSI TTL devices as well as providing a hardware solution to many of the software problems of CRT Video Controller design.

Achievements like these help keep Standard Microsystems custom and standard products in the forefront of technology with increased speeds and densities, and a lower cost per function.



Improvements in processing and manufacturing keep pace with advances in semiconductors.

With the phenomenal growth of the electronics industry, innovation is, of course, highly desirable. But if the products are to perform as designed, they also have to be reliable.

That's why at Standard Microsystems we take every means to insure the utmost quality and dependability. Consequently, "state-of-the-art" applies not only to our products, but to the way we manufacture them.

In wafer fabrication, the latest equipment and techniques are employed. In addition to conventional processing equipment, we use ion implantation technology extensively. We also use plasma reactors for much of our etching and stripping operations to maintain tight tolerances on process parameters.

To make plastic packaging immune to moisture, we use a process that deposits a protective (passivating) layer of silicon nitride on the device surface.

Standard Microsystems processes include high and low voltage p-channel metal gate, n-channel silicon gate (COPLAMOS®), high-speed n-channel silicon gate with depletion mode devices, CLASP® and titanium disilicide gate. In general, these processes have been engineered so that they are also compatible with most industry standard processes.

One obvious advantage our total capability gives customers, is that they can bring us their project at any stage in the development process. For instance, they may already have gone through system definition. Or they may have gone all the way to prototype masks, and only want production runs.

It makes no difference to Standard Microsystems. We can enter the process at any level.

Our full service capability lets us make full use of the technologies we develop. We can produce any quantity of semiconductors customers may require. And we can offer them one of the fastest turnaround times in the industry.

Standard Microsystems' Custom Capability.

Custom MOS. A Small Revolution with a Large Impact.

Remarkable advances in semiconductor technology, combined with the availability of quality, low-cost electronics, continue to open new markets for products incorporating microelectronic components.

Today, metal-oxide semiconductor/large scale integrated (MOS/LSI) circuits are integral components in computers and computer peripherals, automobiles, televisions, electrical appliances, electronic toys and games, bank terminals, telephones and a host of other significant applications.

With further applications for large scale integrated and very large scale integrated (VLSI) circuits being discovered every day, one thing is certain. They will have a profound effect on our lifestyle.

Custom Commitment

Standard Microsystems is organized into two separate Product Lines; Custom Products and Standard Products. Custom Products has its own management, marketing, and engineering team that is fully dedicated to developing and producing custom products.

Custom MOS/LSI is a major portion of our business. Fully one-third of all our revenue is a direct result of our custom MOS/LSI projects.

Over the years, Standard Microsystems has developed custom circuits for a wide variety of applications: Computers and computer peripherals, telecommunications and data communications, garage door openers and burglar alarms, electronic toys and games, musical instruments and more. Both over-the-air and cable T.V. systems have made use of our custom circuits. One company's line of word processing equipment makes almost exclusive use of our custom LSI.

As a company committed to serve the custom marketplace, Standard Microsystems has developed the resources and established procedures for MOS/LSI circuit development that enables the company to respond rapidly to growing customer needs.

System Design—The Alternatives

The electronic system designer can select from several alternatives in the implementation of the system. The optimum selection for any system will depend upon the relative significance of the following factors—

- Costs—developmental, production and maintenance;
- Performance—speed, power dissipation;
- Form factor—system size and weight;
- Uniqueness—proprietary features;
- Development time—product introduction;
- Reliability—mean time between failures (MTBF).

No single alternative is best for all cases—each represents a combination of advantages and disadvantages to be evaluated for the system under consideration. The major alternatives available are listed below.

Standard Circuits

The use of "off the shelf" small scale (SSI), medium scale (MSI), or large scale (LSI) integrated circuits is appropriate whenever development costs and time must be kept to a minimum, and system performance requirements can be met by interconnecting numbers of such standard components. Standard Microsystems is a recognized industry leader in standard LSI components for the data communications and computer peripheral markets.

Microprocessors

These programmable LSI standard circuits can be the elements of choice for certain classes of systems where there is a good fit between the microprocessor capability and the system performance requirements. The system parts count is reduced at the expense of a longer (software) development time.

Gate Arrays

A gate array is a semi-custom circuit containing a pattern of elements which can be selectively interconnected to form the desired logic. The interconnections are typically accomplished by a customized metal pattern.

For low to medium volume production, these "hardware programmable" circuits can reduce parts count and offer some degree of uniqueness, at modest development cost and time.

The Custom Option

FOR HIGH VOLUME PRODUCTION, WHERE THE DEVELOPMENT INVESTMENT CAN BE MADE, THE CLEAR CHOICE IS THE FULLY-CRAFTED CUSTOM CIRCUIT. A custom circuit implementation will provide—

Lowest Overall Cost

The overall cost savings realized with custom LSI can be substantial, especially when high-volume production is encountered.

Savings are effected in several ways. Because custom designed circuits contain only necessary components, the cost of unused circuitry on standard microprocessors or integrated circuits is eliminated. Costs for troubleshooting, repair and warranty claims are reduced. In addition, custom MOS can be more economical over SSI and MSI when purchase, inventory and assembly costs are considered. Also, when a system contains a large amount of SSI and MSI, its custom counterpart can significantly reduce power consumption.

Lowest Parts Count

There are many applications where a single-package custom LSI circuit can out-perform a microprocessor and its ROM and RAM circuits while reducing costs. A custom LSI unit can rapidly execute repetitive functions using high speed logic. A microprocessor needs time-consuming algorithms to do the same thing.

Highest Reliability

Higher reliability is achieved, especially when replacing circuits that contain significant amounts of SSI and MSI. Fewer parts and solder points reduce the failure rate and raise the reliability. This means low MTTR (mean time to repair), which translates into lower maintenance costs and higher customer satisfaction.

Minimum Size, Weight, Power Dissipation

The size and complexity of printed circuit boards are greatly reduced when using a custom circuit. The custom circuit results in a most compact package, specifically designed to perform only the necessary tasks utilizing minimum power and space.

Unique Proprietary Features

Proprietary design is another major benefit. It protects your design from would-be copiers because it makes testing and support difficult. This, coupled with the complexity of custom semiconductor fabrication, makes duplicating your custom circuit far less probable.

The Full Design Custom Program

Typically in a custom program where Standard Microsystems performs all of the operations—from design through to finished product—the following sequence applies:

Evaluation

The customer's system characteristics are carefully evaluated from the information provided to determine the feasibility of the custom approach, considering such factors as system partitioning, functional performance, operational environment, operating speed, power requirements, process selection, packaging and testing.

If the conclusion is positive, Standard Microsystems will quickly provide a Quotation to the potential customer, which will include—

- a firm development schedule
- the non-recurring engineering charge (NRE)
- a production price schedule

System Definition

Once the design is authorized, a thorough specification review takes place between Standard Microsystems' engineers and the customer's engineers. In this critical phase, Standard Microsystems' years of successful design experience are applied as an extension of the customer's design resource in a close working relationship.

Circuit Design

Required functions are converted to detailed MOS logic. The logic is verified via advanced logic simulation routines, utilizing our in-house computers (VAX, Eclipse, PDP-11), and/or breadboard emulators. Circuit simulation is done using SPICE, MOSAID, and Standard Microsystems written software.

Artwork Generation

At Standard Microsystems, device layout is a blend of custom "hand-crafting" and sophisticated CAD, using our Calma GDS I and GDS II color graphics systems, to achieve the optimum composite drawing in terms of size and schedule. Check plots are obtained on our Xynetics and Versatec plotters, and advanced design rule checks (DRC) and electrical rule checks (ERC) provide comprehensive artwork verification.

Mask Fabrication

Production tooling is obtained from qualified mask vendors to Standard Microsystems' exact-

ing, above-industry standards. Colored overlays of each mask layer are typically used as a final check point.

Wafer Fabrication

Standard Microsystems offers a variety of processes, including a mature p-channel metal gate process, and a range of n-channel silicon gate processes. We will determine the appropriate process to satisfy each customer's cost/performance requirements.

All wafer processing is done in our facilities, utilizing state-of-the-art equipment. Standard Microsystems has made substantial investments in direct-step-on-wafer equipment, and advanced ion-implantation, sputtering, deposition and plasma etch equipment.

Assembly

Standard Microsystems can provide a wide variety of industry-standard packages, including ceramic, plastic and CERDIP dual-in-line types, flat-packs and chip carriers. The latest in automated equipment, such as our automatic wire bonders, insure high quality and high volume throughput.

SMC PROCESS CHARACTERISTICS

PROCESS	MASK LEVELS	TYPICAL SUPPLY VOLTAGES	MAX. FREQ. (MHz)	FEATURES/COMMENTS
3000	5	+5, −12	1 to 3	p-channel metal gate. Enhancement mode, most mature process, low performance.
5000	5	+5, +12 −3 (or pump)	3 to 7	n-channel si-gate. Enhancement mode, most mature n-channel process, moderate performance. Substrate bias required.
6000	6	+5, +12, −3 (or pump)	3 to 7	Same as 5000 process with buried contacts.
7000	7	+5	6 to 15	n-channel si-gate. Enhancement/depletion mode, buried contacts, moderate to high performance. No substrate bias required.
8000	6	+5	6 to 15	Same as 7000 process without buried contacts.
9000	7	+5 +12 (optional) −3 (or pump)	9 to 25	Very high performance n-channel si-gate. Enhancement/depletion mode. Substrate bias required.

Customer Owned Tooling

An area of continuing interest to Standard Microsystems is that of Customer Owned Tooling (COT) or Customer Supplied Tooling (CST). In contrast to a full custom design program where Standard Microsystems is responsible for the MOS design, a COT/CST program is one in which the design function will be completed by the customer or an outside design house.

Many customers find it desirable to develop an in-house LSI design capability, for their internal circuit requirements. Standard Microsystems can provide valuable assistance in achieving this goal.

The customer then provides Standard Microsystems with either a completed composite drawing, a data base tape (in suitable format), or an actual processing mask set. Whatever the entry level, Standard Microsystems is prepared to carry the program through to completion.

If the design is in the formative stages, the requirements will be studied and the most suitable set of design rules will be provided.

If the design is already completed, Standard Microsystems will examine the design rules used and recommend which of our processes is most compatible. If small variations to our "standard" processing are required, they can usually be accommodated at little or no expense.

Standard Microsystems has developed comprehensive test sites that are incorporated into our masks for the purpose of parametric and quality assurance measurements. Automated equipment collects and stores measurements from these test sites. If a customer purchases wafers from us, these measurements are provided with the wafers. If a customer chooses to have masks fabricated himself, our test site can be provided for incorporation into the masks.

Standard Microsystems is also prepared to work with customers in establishing a suitable test interface which will enable us to provide the wafer probe and final test operations. Of course, packaging and burn-in are also available.

Whichever approach is taken, Standard Microsystems wants to partcipate in a partnership that makes best use of our respective areas of expertise. We'll work together to bring the project to completion; on time and on budget.

Customer Interface

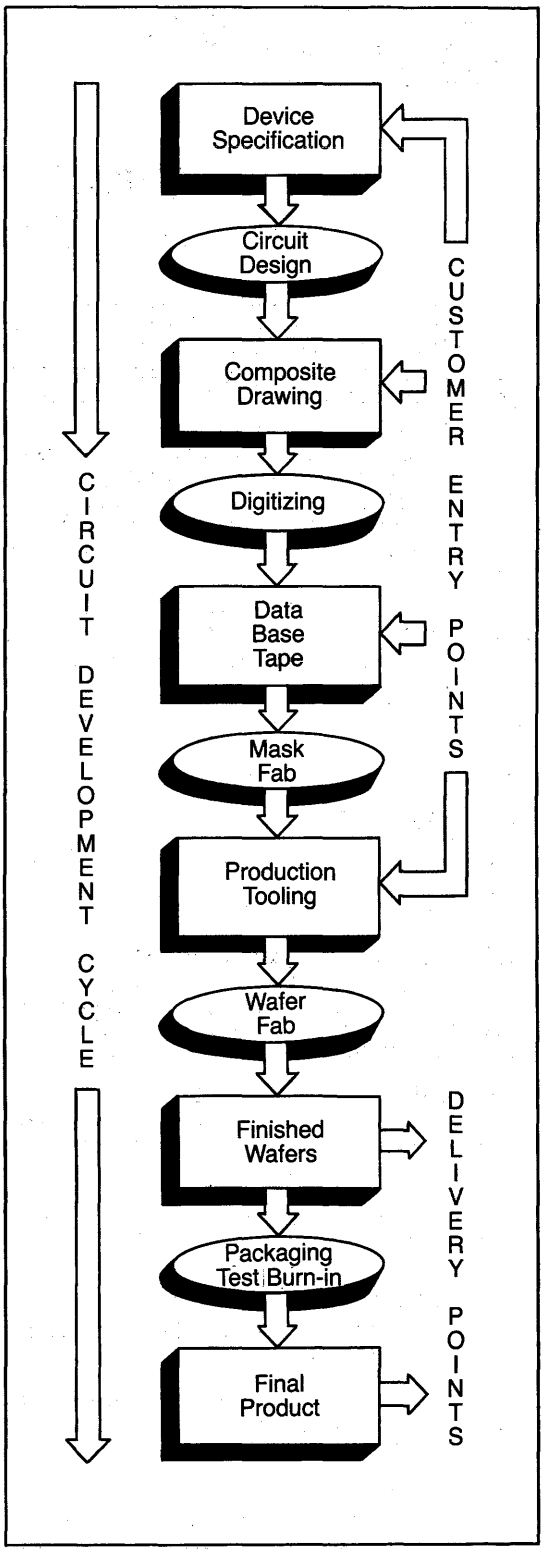
Standard Microsystems is a "full capability" company. We have the resources—an experienced staff and state-of-the-art equipment—to design, process, package and test our Custom MOS circuits.

Our customers are becoming increasingly aware of the benefits of custom circuits in their product lines. They know their products and markets best. Some have developed the technical expertise to perform or participate in the early design phases of a custom program. For this reason, Standard Microsystems offers a variety of customer interface possibilities to serve the broadest possible market.

Communications: The Key to Custom Development

On every Custom program, we establish communications with our customers that last throughout the development and production phases.

Our engineers work in an environment that stimulates creativity while encouraging adherence to pragmatic objectives. The status of each program is closely monitored. Strict scheduling, thorough program management and frequent customer contact have become the hallmark of a Standard Microsystems Custom program. Numerous testimonials from satisfied customers give evidence of our ability to perform—to specification and on time.



STANDARD MICROSYSTEMS CORPORATION

Quality Assurance and Quality Control

Volume manufacturing of quality products requires a rigorous commitment on behalf of STANDARD MICROSYSTEMS and all of its employees. Each phase of the operation from design to shipping must adhere stringently to documented procedures which have produced a product of proven reliability.

The design of a reliable product is assured by adherence to tested and proven design rules. Any change in design rules must be evaluated using a design-rule test vehicle. Each new product is evaluated first by prototype wafer runs and thorough preliminary production and device characterization.

Manufacturing flow is monitored by Quality Control to insure that parameters meet specifications on incoming material, within the line and at outgoing inspection. Clean room standards, calibration and work methods are also monitored. Quality Circles operate within the manufacturing organization to reduce the cost of quality and improve the product.

The Quality Assurance Department is the customer representative with the primary responsibility of evaluating product to current industry standards and related responsibilities of evaluating developmental processes, product and the standards themselves.

The following is a more detailed description of the types of screening performed and how SMC is organized to produce quality products.

1.0 Scope

The measures taken by SMC to produce reliable integrated circuits and the assembly/screening options available to the customer are given in this section.

2.0 Approach

Factors relating to quality and reliability are discussed in the following order: package options, screening, process control, test and characterization, quality conformance/reliability testing, and failure analysis.

3.0 Applicable Documentation

SMC internal specifications define every phase of production and must be approved by the designated representatives of Engineering, Manufacturing, Processing, Quality Control and Quality Assurance departments.

3.1 Design Rules (DR-XXXX)

3.1.1 Geometric design rules define layout considerations, alignment structures, critical-dimension targets, and input-protection networks.

3.1.2 Electrical design rules define performance criteria, measurement methods, device parameters, and process parameters.

3.2 Purchase Specifications (PS-XX)

All critical material is purchased to SMC specifications from qualified vendors.

3.3 Process Specifications (WX-XX, AX-XX)

3.3.1 The procedures used for wafer processing and assembly of microcircuits are fully documented.

3.4 Quality Control Procedures (QC-XX)

QC procedures define the sampling techniques, accept/reject criteria and test methods used in quality audits.

3.5 Quality Assurance Procedures (QA-XX)

QA procedures define methods for product/process qualification, reliability testing and failure analysis.

4.0 Military Standards and Specifications

MIL-C-45662	Calibration System Requirements
MIL-M-38510	General Specification for Microcircuits
MIL-M-55565	Packaging of Microcircuits
MIL-Q-9858	Quality System Requirement
MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
MIL-STD-883	Test Methods and Procedures for Microelectronics
MIL-STD-976	Certification Requirements for JAN Microcircuits
MIL-STD-1331	Microelectronics Terms and Definitions

5.0 Package Options, Features

5.1 Ceramic (no suffix)

50μ inches gold plating on external leads and die cavity, gold eutectic die attach.

5.2 Tin-Plated Ceramic (Suffix "TC")

Over 200μ inches tin plating on external leads, gold on die cavity, gold eutectic die attach.

5.3 Cerdip (Suffix "CD")

Meets MIL-STD-883 internal moisture content requirements of Method 5005. Substrate connections are made through jumper chips, gold eutectic die attach.

5.4 Plastic (Suffix "P")

The plastic used is a B-type epoxy or an approved advanced type having better resistance to a humid environment. Gold eutectic die attach and gold bond wires

are used. Lead material is MIL-M-38510 para 3.5.6 type B (42 Alloy) with a solder lead finish.

6.0 Screening Options

6.1 High-Reliability Screening

The routing is as defined in MIL-STD-883 Method 5004 for Class B product. Periodic Quality Conformance data (para. 10.2) is taken on generically similar parts. A sample flow chart for ceramic product is given on page 6.

6.1.1 Internal Visual

Both Die and Preseal Visual inspections are to the criteria of Method 2010, Condition B of MIL-STD-883. An AQL audit is performed on each lot by Quality Control.

6.1.2 Stabilization Bake

All parts are placed in 150°C storage for 24 hours per Method 1008, Condition C of MIL-STD-883.

6.1.3 Temperature Cycling

All parts are subjected to 10 cycles of −65°C to +150°C per Method 1010, Condition C of MIL-STD-883.

6.1.4 Constant Acceleration

All parts are subjected to a 30,000 g force in the Y1 orientation per Method 2001, Condition E.

6.1.5 Seal

Hermeticity testing is performed to conditions A and C of MIL-STD-883 Method 1014.

6.1.6 Pre burn-in Electrical Test

Ordinarily this is the same as final electrical test.

6.1.7 Burn-in

Condition A and Condition D of MIL-STD-883, Method 1015 are available. The stress is applied for 168 hours at 125°C or at other temperatures according to the time-temperature regression.

6.1.8 Final Electrical Test

Verifies functional and parametric performance to the device specifications.

6.1.9 Final Visual Inspection

All parts are inspected to Method 2009 of MIL-STD-883.

6.2 Standard Screening

Standard Screening is designed for the industrial-commercial customer and is available in all package types. For hermetic packages, temperature cycling, centrifuge and hermeticity are specified as well as die, preseal, and final visual inspection.

6.2.1 Standard Die and Preseal Visual Inspections (AC-04, AC-08)

These inspections were developed from Method 2010 of MIL-STD-883.The inspection criteria are specific to SMC's pMOS and nMOS COPLAMOS® technologies.

6.2.2 Temperature Cycling (AC-15, AD-13)

Temperature cycling is performed to the MIL-STD-883, equivalent of Method 1010, Condition C, −65°C/+150°C, ten cycles.

6.2.3 Constant Acceleration (centrifuge) (AC-16, AD-14)

Constant Acceleration is performed to the MIL-STD-883, equivalent of Method 2001, Condition E, 30,000 g in the Y1 orientation.

6.2.4 Hermeticity (AC-11, AD-15)

Includes fine and gross leak testing to SMC equivalent of MIL-STD-883 Method 1014 Conditions A and C.

6.2.5 Final Electrical Test

Verifies functional and parametric performance to the device specifications.

6.3 Custom Screening

Certain applications require special screening which can be arranged upon request.

7.0 Electrical Test

7.1 Probe and Final Test

SMC test programs are developed by the Test Engineering Department and verified by device characterization. An approval procedure is required for the transfer of a new test program or a revised test program from engineering to production.

7.2 Characterization/correlation

Characterization of parts and correlation of test results with customer incoming testing performed on SMC test equipment, including Megatest and Sentry™ test systems.

7.3 Product Engineering

SMC product engineers characterize parts to improve processing target parameters and test correlation with customers.

8.0 Purchased Material

All manufacturing materials are purchased from qualified vendors to SMC procurement specification.

9.0 Quality Control

The Quality Control Department reports at the same level as the manufacturing, test and process engineering departments. QC is responsible for incoming inspection, in-process audits, out-going inspection, document control, processing returned material and certification of compliance to specification.

9.1 Incoming Inspection

Inspectors verify critical parameters on all material used in manufacturing. The department maintains an approved vendor list and interfaces directly with vendor QC departments.

9.2 In-process Audits

QC performs an on-going monitoring of wafer processing, test and assembly functions.

9.3 Outgoing Inspection

QC inspectors verify proper documentation and perform an external mechanical/visual inspection on each lot prior to shipment.

9.4 Document Control

All procedures for design, wafer processing, assembly, quality control and quality assurance are maintained by document control.

9.5 Returned Material Processing

Returned material, whether for device performance or clerical reasons, is processed through visual and electrical testing.

9.6 Certificates of Compliance

Certificates of Compliance are available for specified screening and/or for products ordered under a customer part number/specification.

10.0 Quality Assurance

The Quality Assurance Department is the customer's

representative and is independent of the product line and manufacturing organizations. Quality Assurance is responsible for reliability assessment of new and existing processes, material analysis, failure analysis, and development of evaluation methods.

10.1 Process Qualification

All new processes and process revisions must equal or exceed the reliability of existing processes on applicable sections of the SMC Quality Conformance Test.

10.2 Quality Conformance Test

Samples of finished product are tested periodically to the criteria of QA-01 (see table 2). This test sequence provides historical data which is also used for qualification of new products and processes. The various subgroups contain tests referenced in Method 5005 of MIL-STD-883 as well as tests designed around industry requirements not yet incorporated in military standards.

10.3 Analysis

10.3.1 The analytical facilities include a scanning electron microscope (SEM), an infrared microscope, optical microscopes, an X-ray unit and electronic test instruments.

10.3.2 Scanning electron microscopy is used in the periodic evaluation of workmanship in wafer processing and assembly, to support engineering efforts at process development and improvement, and in failure analysis.

10.3.3 Failure Analysis is performed upon request by sales, marketing or manufacturing organizations and is also performed on reliability test failures. The failure analysis procedures support the development of new product, process improvements, and the evaluation of screening methods.

10.3.4 Material analysis is performed on layers of the integrated circuit and on packaging to support the engineering development. This characterization is performed on in-house facilities. Independent outside analytical laboratories are used to supplement SMC facilities if and when required.

11.0 Lot Traceability

SMC maintains full lot traceability on all product types in all packaging options (including plastic). The information available includes:

11.1 Wafer Processing Records

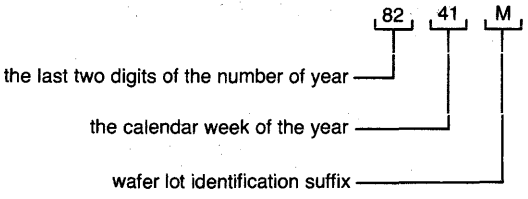
Sign-off and date on all operations, critical measurements and inspection records.

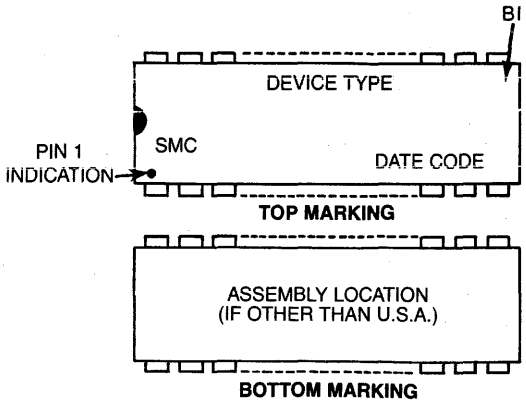
TABLE 1

WAFER LOT ACCEPTANCE

TEST	LIMIT	SAMPLING PLAN
wafer thickness	minimum thickness 0.010 in. exceeds MIL-M-38510 minimum of .006 in.	LTPD = 10 (Incoming)
metallization thickness	17,500 Å ± 2,500 Å	one wafer per metallization run
stability	$\Delta V_{FB} \leq 0.5$ volts	test piece each tube change, each week, and each wafer lot
device parameters	V_{th} enhancement, depletion as applicable K′ enhancement, depletion as applicable ρs polysilicon ρs mesa (n^-) dielectric strength (BV_{ox}) n+ diode breakdown (BV_n+)	each wafer
SEM	Mil-Std 883 Method 2018	each week on each process
Glassivation	3,000 Å minimum Silicon Nitride 5,000 Å minimum Silicon Dioxide	one test piece per deposition run

DATE CODE INTERPRETATION





11.2 Wafer Lot Acceptance (Mapping) (see table 1)

Device parameters are recorded using a precision parametric interface to a Digital Equipment Corporation PDP 11/23 computer. The data base at wafer map includes probe, final test and wafer processing records (run sheets).

11.3 Wafer Probe and Final Test Data

These are correlated with mapping results to develop optimized process targets and yield improvement.

11.4 Assembly Records

Inspection results and screening throughput is recorded with date and sign-off for each lot.

TABLE 2—QA-01 QUALITY CONFORMANCE

GROUP B TESTS

Test	SMC Test Method	Mil Std 883 Method	Condition	Quantity/ accept no. or LTPD	Frequency
Subgroup 1 Physical dimensions	QC-22	2016		2 devices (no failures)	every package lot
Subgroup 2 Resistance to solvents	QC-21	2015	Marking Permanence	4 devices (no failures)	every shipment
Subgroup 3 Solderability		2003	Soldering temperature of 260 ± 10°C	15	periodic conformance
Subgroup 4 Internal visual and mechanical		2014	Failure criteria from design and construction requirements of applicable procurement document	1 device (no failures)	periodic conformance
Subgroup 5 Bond strength (1) Thermocompression (2)Ultrasonic or wedge Die shear strength	QC-12 QC-13	2011 2019	 (1) Test condition C or D (2) Test condition C or D 	15	periodic conformance
Subgroup 6 Internal water-vapor content		1018	5,000 ppm maximum water content at 100°C	3 devices (no failures) or 5 devices (1 failure)	periodic conformance
Subgroup 7 Seal (a) Fine (b) Gross		1014	As applicable	5	periodic conformance
Subgroup 8 Electrical parameters Electrostatic discharge sensitivity Electrical parameters		3015	Group A, subgroup 1 Test condition A or B Group A, subgroup 1	15	new device types

GROUP C TESTS—DIE RELATED

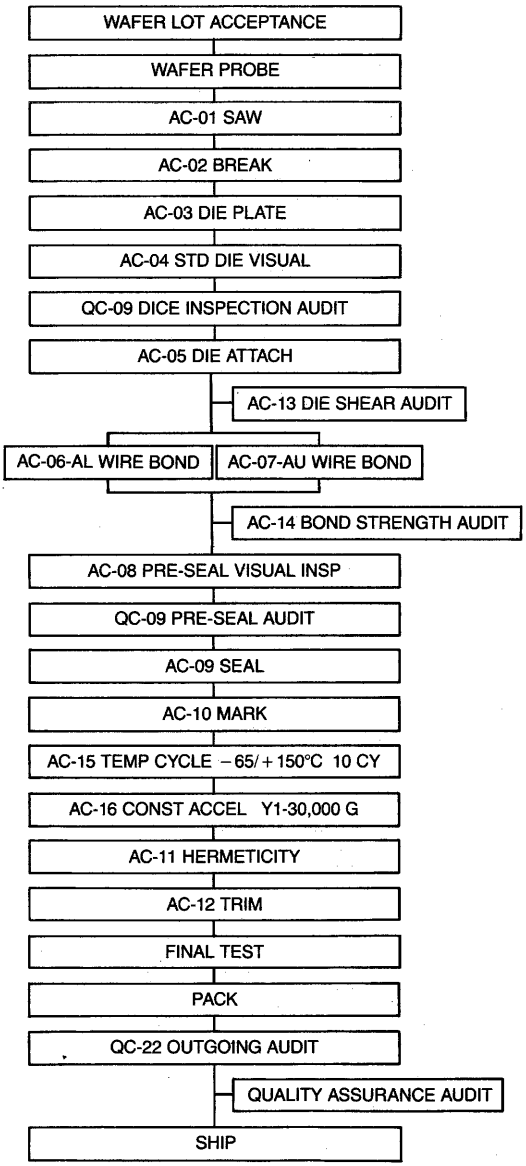
Test	SMC Test Method	Mil Std 883 Method	Condition	Quantity/ accept no. or LTPD	Package Type
Subgroup 1 Steady state life test End-point electrical parameters	QA-02 Final test	1005	Test condition to be specified (1,000 hours at 125°C) As specified in the applicable device specification	5	all
Subgroup 2 Temperature cycling Constant acceleration Seal (a) Fine (b) Gross Visual examination End-point electrical parameters	 Final test	 1010 2001 1014	 Test condition C Test condition E min. Y_1 orientation only As applicable As specified in the applicable device specification	15	all hermetic

GROUP D—PACKAGE RELATED

Test	SMC Test Method	Mil Std 883 Method	Condition	Quantity/ accept no. or LTPD	Package Type
Subgroup 1					
Physical dimensions	QC-22	2016		15	all
Subgroup 2					
Lead integrity	QC-19	2004	Test condition B2 (lead fatigue	15	all
Seal	AC-11	1014	As applicable		all
(a) Fine					hermetic
(b) Gross					
Lid torque		2024	As applicable		cerdip only
Subgroup 3					
Thermal shock		1011	Test condition B, 15 cycles	15	all
Temperature cycling		1010	Test condition C, 100 cycles		hermetic*
Moisture resistance	QA-03	1004			
Seal		1014	As applicable		
(a) Fine					
(b) Gross					
Visual examination			Per visual criteria of Method 1004 and 1010		
End-point electrical parameters			As specified in the applicable device specification		
Subgroup 4					
Mechanical shock		2002	Test condition B minimum	15	all
Vibration, variable frequency		2007	Test condition A minimum		hermetic
Constant acceleration		2001	Test condition E minimum, Y_1 orientation		
Seal		1014	As applicable		
(a) Fine					
(b) Gross					
Visual examination					
End-point electrical parameters			As specified in the applicable device specification		
Subgroup 5					
Salt atmosphere		1009	Test condition A minimum	15	all
Seal		1014	As applicable		hermetic*
(a) Fine					
(b) Gross					
Visual examination			Per visual criteria of Method 1009		
Subgroup 6					
Internal water-vapor content		1018	5,000 ppm maximum water content at 100°C	3 devices (no failures) or 5 devices (1 failure)	all hermetic
Subgroup 7					
Adhesion of lead finish		2025		15	all
Subgroup 8					
Humid Environment	QA-04		1000 hours 85°C/85% Relative Humidity	15	plastic
End-point electrical parameters	Final test				
Subgroup 9					
Autoclave (Pressure Cooker)	QA-05		24 hours at 2 atm 121°C	15	plastic
End-point electrical parameters	Final test				

*packages having gold plating thicknesses of 50 microinches or less are not required to pass subgroups 3 and 5.

CERAMIC



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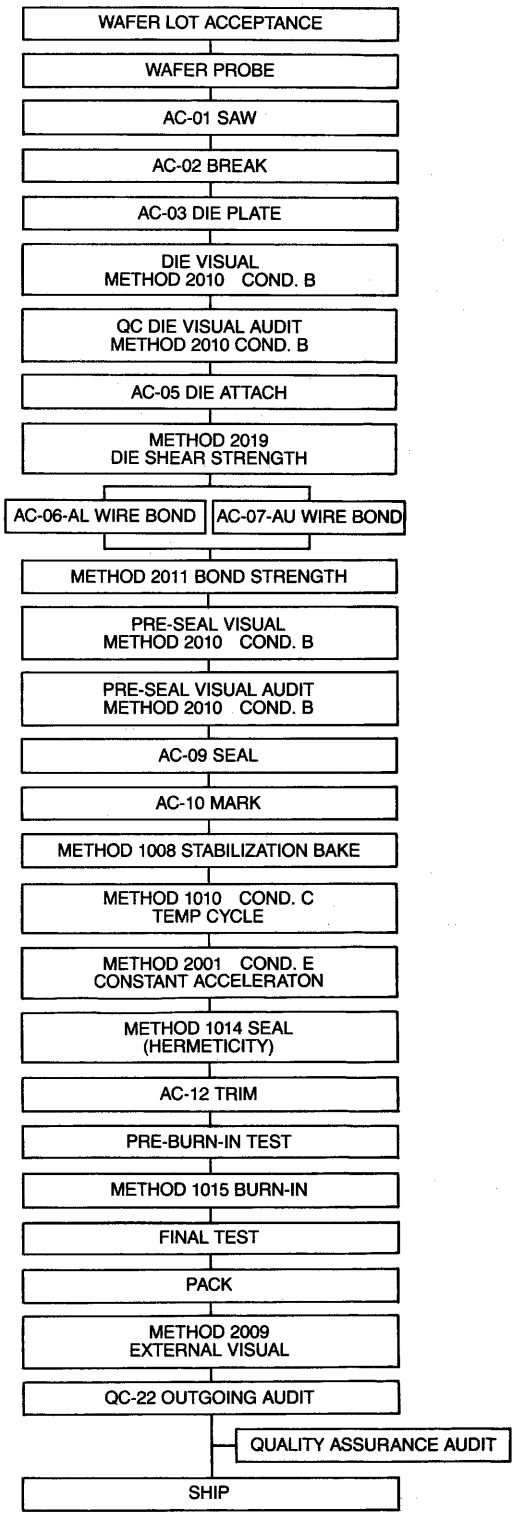
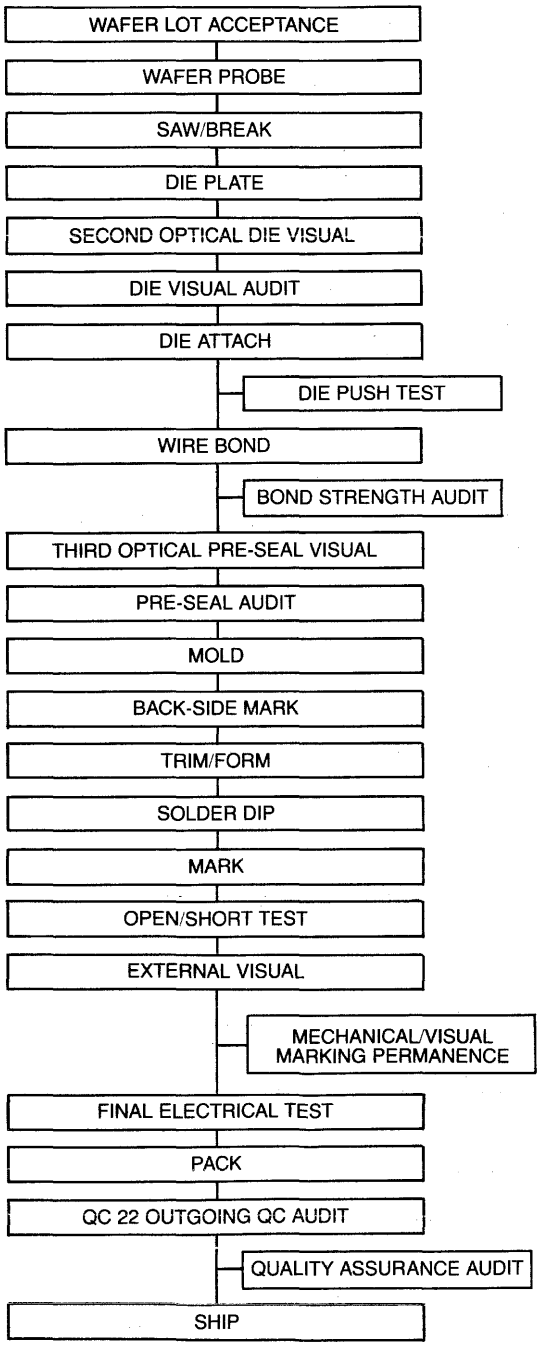
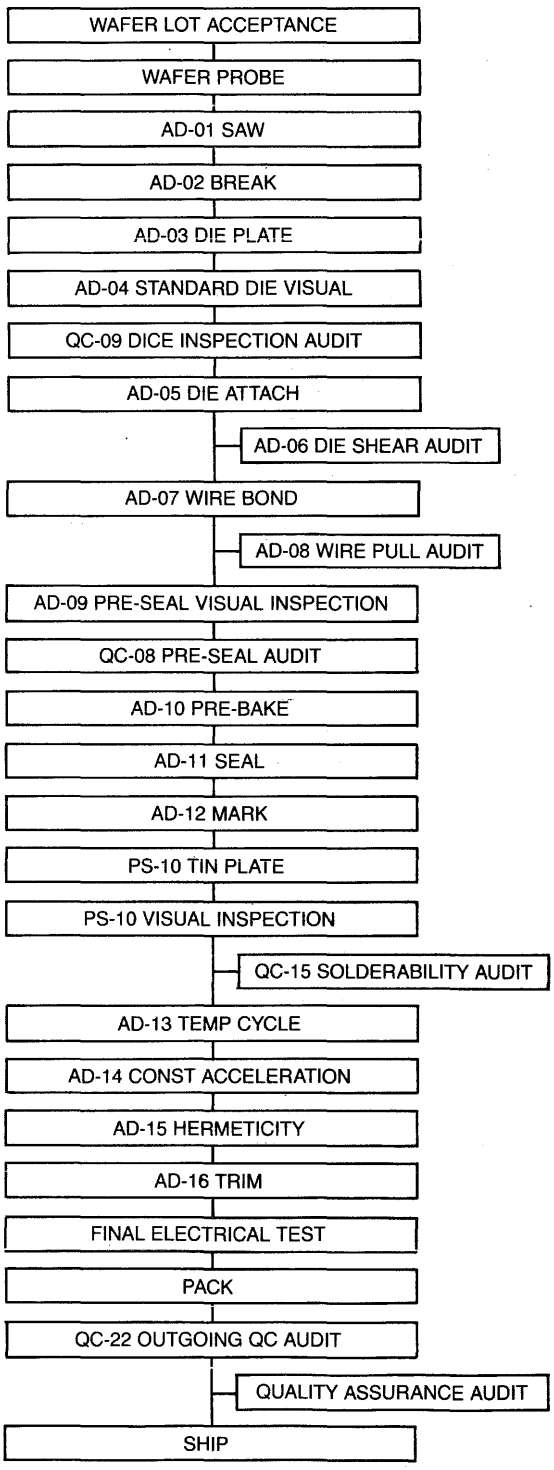


*This High Reliability flow chart applies to ceramic product. Similar flow charts exist for cerdip and TC packaging. All ACXX, QCXX procedures are under SMC Document Control. All Method XXXX procedures are MIL-STD-883 Test Methods.

PLASTIC (NOTE 1)



CERDIP



Note 1—Plastic assembly is sub-contracted. Assembly operations are controlled by SMC approved sub-contractor specifications.

Data Communication Products

Part Number	Name	Description	Max Baud Rate	Power Supplies	Package	Page
COM 1553A	MIL-STD-1553A UART	MIL-STD-1553 (Manchester) Interface Controller	1 MB	+5	40 DIP	27-42
COM 1553B	MIL-STD-1553B UART	MIL-STD-1553B (Manchester) Interface Controller	1 MB	+5	40 DIP	43-58
COM 1671	ASTRO	Asynchronous/Synchronous Transmitter/Receiver, Full Duplex, 5-8 data bit, 1X or 32X clock	1 MB	+5, −5, +12	40 DIP	59-74
COM 1863	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit, enhanced distortion margin	62.5 KB	+5	40 DIP	75-82
COM 2017	UART	Universal Asynchronous Receiver Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit	25 KB	+5, −12	40 DIP	83-90
COM 2017H	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit	40 KB	+5, −12	40 DIP	83-90
COM 2449	RS449-USART	RS 449 Compatible Universal Synchronous/Asynchronous Receiver/Transmitter	1 MB	+5	40 DIP	91-106
COM 2502	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 2 stop bit	25 KB	+5, −12	40 DIP	83-90
COM 2502H	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 2 stop bit	40 KB	+5, −12	40 DIP	83-90
COM 2601	USRT	Universal Synchronous Receiver/ Transmitter, STR, BSC, Bi-sync compatible	250 KB	+5, −12	40 DIP	107-114
COM 2651	USART/PCI	Universal Synchronous/Asynchronous Receiver/Transmitter, Full Duplex, 5-8 data bits; 1, 1½, 2 stop bit, 1X, 16X, 64X clock	1 MB	+5	28 DIP	115-126
COM 2661	USART/EPCI	Universal Synchronous/Asynchronous Receiver/Transmitter, Full Duplex, 5-8 data bits; 1, 1½, 2 stop bit, 1X, 16X, 64X clock	1 MB	+5	28 DIP	127-138
COM 5025	Multi-Protocol USYNRT	SDLC, HDLC, ADCCP, Bi-sync, DDCMP compatible, automatic bit stuffing/ stripping, frame detection/generation, CRC generation/checking, sync detection	1.5 MB	+5, +12	40 DIP	139-150
COM 7210	GPIB Interface Controller	Intelligent Interface Controller for GPIB (IEEE-488-1978)	8 MHz	+5	40 DIP	151-152
COM 8004	32 Bit CRC Generator/ Checker	Companion device to COM 5025 for 32 bit CRC	2.0 MB	+5	20 DIP	153-158
COM 8017	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit	40 KB	+5	40 DIP	159-166
COM 8018	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit, enhanced distortion margin	62.5 KB	+5	40 DIP	75-82
COM 8251A	USART	Universal Synchronous/Asynchronous Receiver/Transmitter, Full Duplex, 5-8 data bit, 1, 1½, 2 stop bit	64 KB (sync) 9.6 KB (async)	+5	28 DIP	167-182
COM 8502	UART	Universal Asynchronous Receiver/ Transmitter, Full Duplex, 5-8 data bit, 1, 2 stop bit	40 KB	+5	40 DIP	159-166
COM 9004	IBM 3274 Receiver/ Transmitter	IBM 3274 Compatible receiver/ transmitter	2.36 MB	+5, ±12	40 DIP	183-190
COM 9026	LANC	Local Area Network Controller for token pass systems	2.5 MB	+5	40 DIP	191-206

STANDARD MICROSYSTEMS CORPORATION

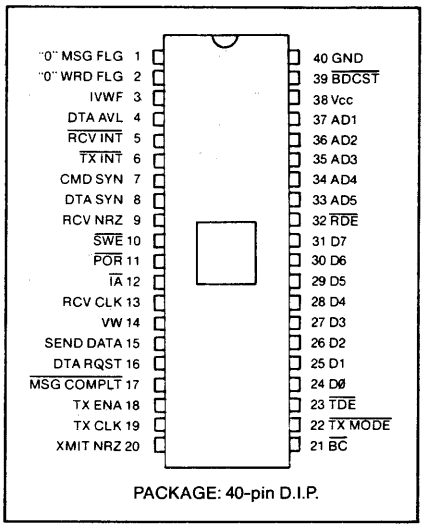
COM 1553A
μPC FAMILY

MIL-STD-1553A "SMART®"

FEATURES

- ☐ Support of MIL-STD-1553A
- ☐ Operates as a: Remote Terminal Responding
  Bus Controller Initiating
- ☐ Performs Parallel to Serial Conversion when Transmitting
- ☐ Performs Serial to Parallel Conversion when Receiving
- ☐ Compatible with HD-15531 Manchester Encoder/Decoder
- ☐ All Inputs and Outputs are TTL Compatible
- ☐ Single +5 Volt Supply
- ☐ COPLAMOS® N Channel MOS Technology
- ☐ Available in PC Board Form from Grumman Aerospace Corporation

PIN CONFIGURATION



PACKAGE: 40-pin D.I.P.

GENERAL DESCRIPTION

The COM 1553A SMART® (Synchronous Mode Avionics Receiver/Transmitter) is a special purpose COPLAMOS N-Channel MOS/LSI device designed to provide the interface between a parallel 8-bit bus and a MIL-STD-1553A serial bit stream.

The COM 1553A is a double buffered serial/parallel and parallel/serial converter providing all of the "hand shaking" required between a Manchester decoder/encoder and a microprocessor as well as the protocol handling for both a MIL-STD-1553 bus controller and remote terminal.

The COM 1553A performs the following functions in response to a 16 bit Command Word. It provides address detection for the first five bits of the serial data input. If all 1's appear in the address field, a broadcast signal is generated. The sixth bit is decoded as mode: transmit or receive. The next five bits are decoded for zero message flag and special flags in the subaddress/mode field. The last five bits (word-count field) are decoded determining the number of words to be received or transmitted.

When receiving data sync the COM 1553A performs a serial to parallel conversion, buffers the 16 bit message word, and formats it into two parallel (8 bit) bytes for presentation to the I/O bus under processor or hard wired logic control.

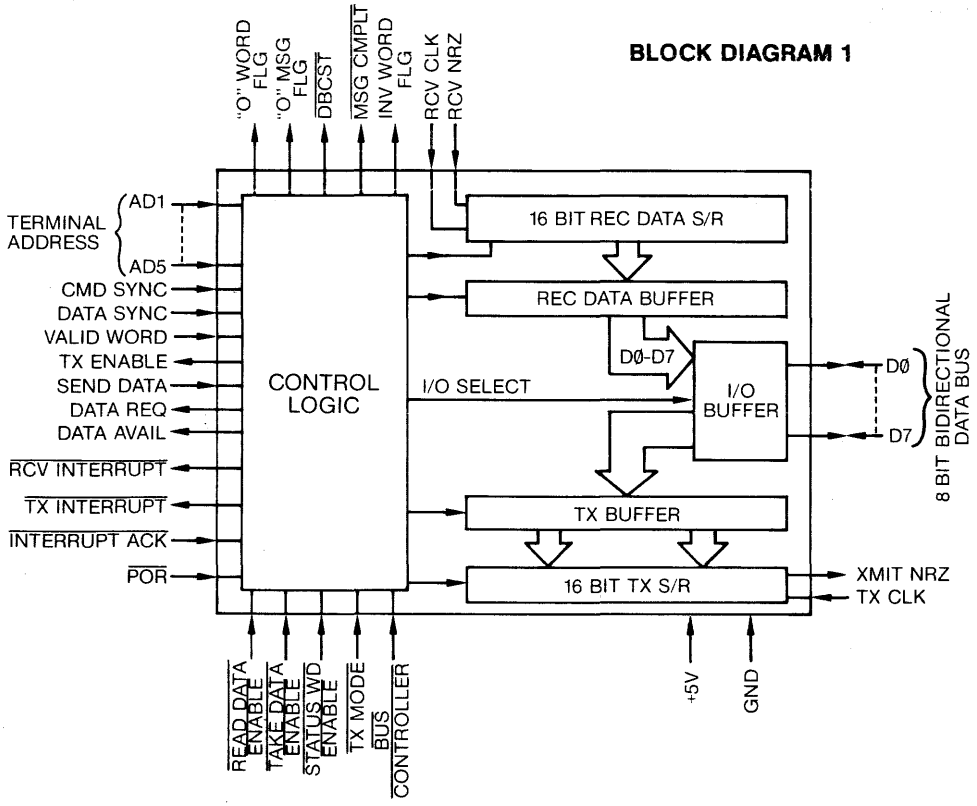
In the transmit mode the COM 1553A takes two parallel 8 bit data words from the I/O bus and serially transmits the resultant 16 bit word to the Manchester encoder. This is done under the control of Send Data. To facilitate data transfer the COM 1553A provides all necessary buffering and storage for transmitted and received data. It also provides all necessary hand shaking, control flags and interrupts to a processor or hard wired logic terminal. See block diagram 1.

The COM 1553A can be set up as either a remote terminal or a bus controller interface.

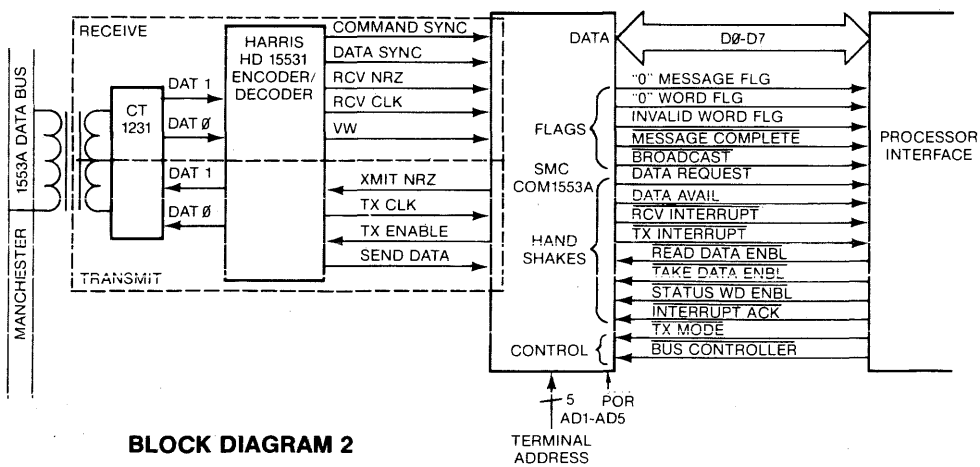
The COM 1553A is compatible with Harris' HD-15531 CMOS Manchester Encoder-Decoder chip and interfaces directly with it. A 3 device kit consisting of: SMC's COM 1553A, Harris' HD-15531 and Circuit Technology's CT1231 forms a complete system interface for the message structure of MIL-STD-1553A. See block diagram 2.

Note: All terminology utilized in this data sheet is consistent with MIL-STD-1553.

BLOCK DIAGRAM 1



BLOCK DIAGRAM 2



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	"Ø" MESSAGE FLAG	ØMF	The ZERO MESSAGE FLAG output is set when the 7th through 11th bits of the NRZ serial input data in a command envelope (see figure 1) are zero. ØMF is an open drain output.
2	"Ø" WORD FLAG	ØWF	The ZERO WORD FLAG output is set when the 12th through 16th bits of the NRZ serial input data in a command envelope (see figure 1) are zero. ØWF is an open drain output.
3	INVALID WORD FLAG	IVWF	The INVALID WORD FLAG output is set when the word just received has an invalid parity bit or invalid format. IVWF is an open drain output.
4	DATA AVAILABLE	DTA AVL	DATA AVAILABLE is set when a word received is ready to be read. When the COM 1553A is the bus controller, DTA AVL occurs on command, status or data words. When the COM 1553A is a remote terminal, DTA AVL is set only on data words. DTA AVL is an open drain output.
5	$\overline{\text{RECEIVE INTERRUPT}}$	$\overline{\text{RCV INT}}$	$\overline{\text{RECEIVE INTERRUPT}}$ is set to zero when the 6th bit following a command sync is a zero and the first 5 bits match AD1-AD5. $\overline{\text{RCV INT}}$ is reset to one by $\overline{\text{IA}}$ or $\overline{\text{POR}}$, or if the line is not active for 32 receive clocks.
6	$\overline{\text{TRANSMIT INTERRUPT}}$	$\overline{\text{TX INT}}$	$\overline{\text{TRANSMIT INTERRUPT}}$ is set to zero when the 6th bit following a command sync is a one, and the first 5 bits match AD1-AD5. $\overline{\text{TXINT}}$ is reset to one by $\overline{\text{IA}}$ or $\overline{\text{POR}}$.
7	COMMAND SYNC	CMD SYN	COMMAND SYNC is an input from the Manchester decoder and must be high for 16 receive clocks enveloping the receive NRZ data of a command word.
8	DATA SYNC	DTA SYN	DATA SYNC is an input from the Manchester decoder and must be high for 16 receive clocks enveloping the receive NRZ data of a data word.
9	RECEIVER NRZ	RCV NRZ	Receiver serial input from Manchester decoder. Data must be stable during the rising edge of the receive clock.
10	$\overline{\text{STATUS WORD ENABLE}}$	$\overline{\text{SWE}}$	$\overline{\text{SWE}}$ is the output enable for the following open drain outputs: ØMF ØWF IVWF DTA AVL $\overline{\text{DTA RQ}}$ $\overline{\text{MSG CPLT}}$
11	$\overline{\text{POWER ON RESET}}$	$\overline{\text{POR}}$	$\overline{\text{POWER ON RESET}}$. Active low for reset.
12	$\overline{\text{INTERRUPT ACKNOWLEDGE}}$	$\overline{\text{IA}}$	$\overline{\text{IA}}$ resets $\overline{\text{TX INT}}$, $\overline{\text{REC INT}}$, ØMF, ØWF and $\overline{\text{BRD CST}}$. $\overline{\text{IA}}$ may occur between the trailing edges of receive clocks 6 and 10, or between the leading edge of receive clock 12 and the falling edge of receive clock 15, or after the falling edge of clock 17.
13	RECEIVE CLOCK	RCV CLK	The RECEIVE CLOCK is synchronous with the Receiver NRZ input during the command sync or data sync envelopes.
14	VALID WORD	VW	This input is driven by the VALID WORD output of the Manchester Decoder. VW should occur immediately after the rise of the first RCV CLK following the fall DATA SYNC or COMMAND SYNC.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
15	SEND DATA	SD	SEND DATA is a "handshake" signal received from the Manchester encoder indicating that the encoder is ready for the COM 1553A to transmit data. SD will bracket 16 transmit data clocks. The contents of the transmitter buffer will be transferred into the transmit register when SD is low.
16	DATA REQUEST	DTA RQST	DATA REQUEST is an open drain output which is set high when the transmitter holding register is ready to accept more data.
17	$\overline{\text{MESSAGE COMPLETE}}$	$\overline{\text{MSG CMPLT}}$	In the receive mode the $\overline{\text{MESSAGE COMPLETE}}$ output is set low when the appropriate number of data words have been received. In the transmit mode, $\overline{\text{MSG CMPLT}}$ indicates that the appropriate number of command, status or data words have been transmitted. When the COM 1553A is a bus controller, $\overline{\text{MSG CMPLT}}$ will be asserted low when 33 command status or data words have been transmitted. $\overline{\text{MSG CMPLT}}$ is an open drain output.
18	TRANSMIT ENABLE	TXENA	A TRANSMIT ENABLE signal will be sent to the Manchester Encoder to initiate transmission of a word. TXENA is generated under the following conditions: 1) COM 1553A is a bus controller: A $\overline{\text{TXMODE}}$ pulse will set TXENA. A second $\overline{\text{TXMODE}}$ pulse will reset TXENA. 2) COM 1553A is a remote terminal. A Transmit Command from the Controller will cause a $\overline{\text{TRANSMIT INTERRUPT}}$ (see pin 6). When this is acknowledged by a TXMODE pulse from the system, TXENA will be set. TXENA will then be reset by either A) Send Data Command associated with the last data word. B) a second $\overline{\text{TXMODE}}$ pulse. 3) COM 1553A is a remote terminal. The falling edge of a DATA SYNC associated with the last data word of a message while in the receive mode. TXENA will be reset during the next SEND DATA envelope.
19	TRANSMIT CLOCK	TXCLK	Transmitter shift clock.
20	TRANSMIT NRZ	XMIT NRZ	Serial data output to the Manchester Encoder.
21	$\overline{\text{BUS CONTROLLER}}$	$\overline{\text{BC}}$	$\overline{\text{BC}}$ determines whether the COM 1553A is acting as bus controller ($\overline{\text{BC}} = 0$) or as a remote terminal ($\overline{\text{BC}} = 1$).
22	$\overline{\text{TRANSMIT MODE}}$	$\overline{\text{TXMODE}}$	$\overline{\text{TXMODE}}$ is a system input controlling transmission. See TXENA (pin 18).
23	$\overline{\text{TAKE DATA ENABLE}}$	$\overline{\text{TDE}}$	$\overline{\text{TDE}}$ is an input from the system initiating transmission. Two $\overline{\text{TDE}}$ pulses are required for each 16 bit data word, one for each 8 data bits placed on DØ-D7.
24-31	DATA BUS	DØ-D7	Bidirectional 8 bit Data Bus to the system. DØ is the LSB. DØ-D7 present open drain outputs.
32	$\overline{\text{READ DATA ENABLE}}$	$\overline{\text{RDE}}$	$\overline{\text{RDE}}$ is an input from the system instructing the COM 1553A to place the received data onto DØ-D7. Two $\overline{\text{RDE}}$ pulses are required per 16 bit data word, one for each 8 bits.
33-37	ADDRESS	AD5-AD1	AD1-AD5 provide addressing to the COM 1553A. Each input has a pull-up resister allowing simple switching to ground to select the user address.
38	POWER SUPPLY	VCC	+5 Volt supply.
39	$\overline{\text{BROADCAST}}$	$\overline{\text{BDCST}}$	$\overline{\text{BDCST}}$ is set low when a "broadcast" command word (the address bits all set to "one") is being received. $\overline{\text{BDCST}}$ is reset by $\overline{\text{IA}}$.
40	GROUND	GND	Ground

OPERATION...RECEIVE MODE

The COM 1553A is considered in the receive mode when TXENA = 0. The most significant bit of both command and data words is received first.

Message reception is initiated when CMD SYN goes high. The next 16 receive clocks are used to shift serial data into RCV NRZ.

The first 5 bits of a command word designate a remote terminal address. These 5 bits are compared with AD1-5. Should the address bits compare, the sixth bit is examined. If it is a zero, a $\overline{\text{RECEIVE INTERRUPT}}$ is generated. If it is a one, a $\overline{\text{TRANSMIT INTERRUPT}}$ is generated.

Bit fields 7-11 and 12-16 are examined for all zeros. All zeros in bit field 7-11 denotes a "ZERO MESSAGE" and all zeros in bit field 12-16 denotes a "ZERO WORD."

Receipt of a data word is indicated when DTA SYN goes high.

When DTA SYN or CMD SYN goes low, the contents of the 16 bit receive register are loaded into the receive buffer. The buffer is organized into two groups of 8 bits each. The most significant 8 bits (byte 1) will be enabled onto the 8 bit data bus on receipt of the first $\overline{\text{RDE}}$ pulse ($\overline{\text{RDE1}}$). The second byte will be enabled on receipt of the second $\overline{\text{RDE}}$ pulse ($\overline{\text{RDE2}}$).

A DATA AVAILABLE is generated for data words only. However, data will be available on DØ-D7 for both command and data words.

If 32 clocks are received after the rising edge of CMD SYN or DTA SYN an "Idle Line Reset" condition exists. This implies that a new CMD SYN or DTA SYN has not yet been received within 16 clocks of the fall of the previous sync signal. The "Idle Line Reset" will reset the following signals:

$\overline{\text{REC INT}}$	"0" MSG FLG
$\overline{\text{TX INT}}$	"0" WRD FLG
$\overline{\text{BRD CST}}$	

When the commanded number of data words have been received, a $\overline{\text{MESSAGE COMPLETE}}$ signal is generated.

As the transmitter and receiver registers operate independently, the COM 1553A will receive its own transmission. The following signals are inhibited during transmission:

$\overline{\text{BC}} = 0$	$\overline{\text{BC}} = 1$
$\overline{\text{REC INT}}$	DAT AVL
$\overline{\text{XMT INT}}$	IVWF
$\overline{\text{BRD CST}}$	$\overline{\text{REC INT}}$
ØWF	$\overline{\text{XMT INT}}$
ØMF	ØMG
JAM MESSAGE ERROR*	ØWF
	$\overline{\text{BRD CST}}$
	JAM MESSAGE ERROR*

*JAM MESSAGE ERROR is an internal signal. See OPERATION...TRANSMIT MODE.

OPERATION...TRANSMIT MODE

The COM 1553A is considered in the transmit mode when TXENA = 1. This is caused by a $\overline{\text{TXMODE}}$ pulse (see description of pin functions, pin 18). The $\overline{\text{TXMODE}}$ pulse in turn is a system response to a transmit command from the receiver.

When the Manchester Encoder receives TXENA = 1, it will respond with SEND DATA = 1. The COM 1553A will then send the system a DATA REQUEST.

Data is loaded into the transmitter data buffer from the 8 bit data bus by pulsing $\overline{\text{TDE}}$. The 8 most significant bits are loaded in by the first $\overline{\text{TDE}}$ pulse ($\overline{\text{TDE1}}$), the 8 least significant bits by the second $\overline{\text{TDE}}$ pulse ($\overline{\text{TDE2}}$).

When SEND DATA (pin 15) is low, the transmitter shift register inputs will follow either the transmit buffer output, JAM ADDRESS or JAM MESSAGE ERROR signals. When SEND DATA is high, the shift register parallel inputs are disabled and the shift register contents are shifted out in NRZ form using the 16 negative edges in the send data envelope.

To facilitate transmission of the status word from a remote terminal, the COM 1553A will "jam" the first (most significant) 6 bits of the status word into the transmit register when $\overline{\text{BC}}$ is high. These bits will automatically be sent at the first SEND DATA pulse. In general for MIL-STD-1553A the remaining 10 bits will normally be all zeros and will automatically be sent out as such. If it is desired to send additional status information (for MIL-STD-1553B), a $\overline{\text{TDE1}}$ pulse will load the least significant 2 bits of the first 8 bit byte, and a $\overline{\text{TDE2}}$ will load all 8 bits of the second byte. Note that these TDE pulses must be sent (and data presented) before the first SD = 1 response from the Manchester Encoder.

A JAM ADDRESS occurs when 1) a transmit command is addressed to the COM 1553A 2) A $\overline{\text{TXMODE}}$ pulse is received and 3) a valid word signal is received. Upon a JAM ADDRESS the COM 1553A will load its address into the first 5 bits of the transmit register.

Alternatively, a JAM ADDRESS will also occur at the fall of the last data sync after valid receive command has been detected.

The JAM ADDRESS function will be inhibited if a "0" word and "0" message condition exists in the command word. The JAM ADDRESS will be reset by the leading edge of SEND DATA.

The JAM MESSAGE ERROR function occurs when, in the receive mode, a data word is not followed by a VALID WORD signal. JAM MESSAGE ERROR consists of loading a one in the sixth bit location of the transmit shift register (the message error location).

JAM MESSAGE ERROR is inhibited when the transmit command word contains "0" Message and "0" Word fields.

When the commanded number of data words has been transmitted a $\overline{\text{MESSAGE COMPLETE}}$ signal will be generated.

GENERAL OPERATION NOTES

1. $\overline{\text{BUS CONTROLLER}}$. When $\overline{BC} = 0$, signifying that the COM 1553A is the bus controller the following is true:
   A. DTA AVL is generated on the rising edge of the 17th receive clock following a Command Sync or Data Sync. This allows the bus controller to receive command, status or data words regardless of their address.
   B. TXENA is contingent only on $\overline{\text{TXMODE}}$. A bus controller can therefore transmit whenever it desires.
   C. The jam functions are inhibited.

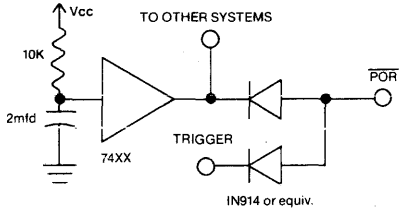
2. INVALID WORD FLAG. When $\overline{BC} = 0$, IVWF will be set if the Valid Word input (from the Manchester decorder) does not go high following receipt of all words. This includes words received from the same device's transmitter. (This provides a validity test of the controller transmission).
   When $\overline{BC} = 1$, IVWF will be set if Valid Word does not go high following receipt of all command and address words addressed to the terminal.
   IVWF will be set for the following conditions:

Message type	*Word*	*Terminal is*	*IVWF generated*
Transit Group	Transmit command	receiving	yes
	Status word	transmitting	no
	Data word	transmitting	no
Receive Group	Receive command	receiving	yes
	Data word	receiving	yes
	Status word	transmitting	no
Receive/Transmit Group (this terminal addressed to receive)	Receive command	receiving	yes
	Transmit command	receiving	no
	Status word	receiving	no
	Data word	receiving	yes
	Status word	transmitting	no
Receive/Transmit group (this terminal addressed to transmit)	Receive command	receiving	no
	Transmit command	receiving	yes
	Status word	transmitting	no
	Data word	transmitting	no
	Status word	receiving	no

3. $\overline{\text{POWER ON RESET}}$. During power-up, $\overline{\text{POR}}$ is a low to high exponential with a minimum low time, after the supply is within specified limits, of 10 microseconds. $\overline{\text{POR}}$ may also occur asynchronously anytime after power has stabilized.
   $\overline{\text{POR}}$ initializes the following outputs:

ØMG	$\overline{\text{REC INT}}$	$\overline{\text{TDE}}$
ØWF	$\overline{\text{MSG CMPLT}}$	DTA AVL
$\overline{\text{BRD CST}}$	IVW	TXENA
$\overline{\text{XMT INT}}$	$\overline{\text{RDE}}$	DTA RQ

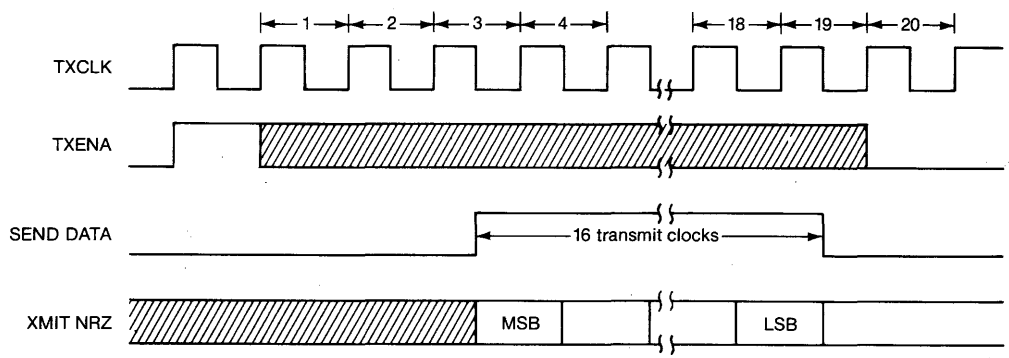
   The following circuit may be used to implement $\overline{\text{POR}}$.



4. WORD COUNT: Word count is decoded as follows:

D1	*D2*	*D3*	*D4*	*D5*	*Word Count*
0	0	0	0	1	1
0	0	0	1	0	2
1	1	1	1	1	31
0	0	0	0	0	32

TRANSMIT TIMING FIGURE 1



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... -0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

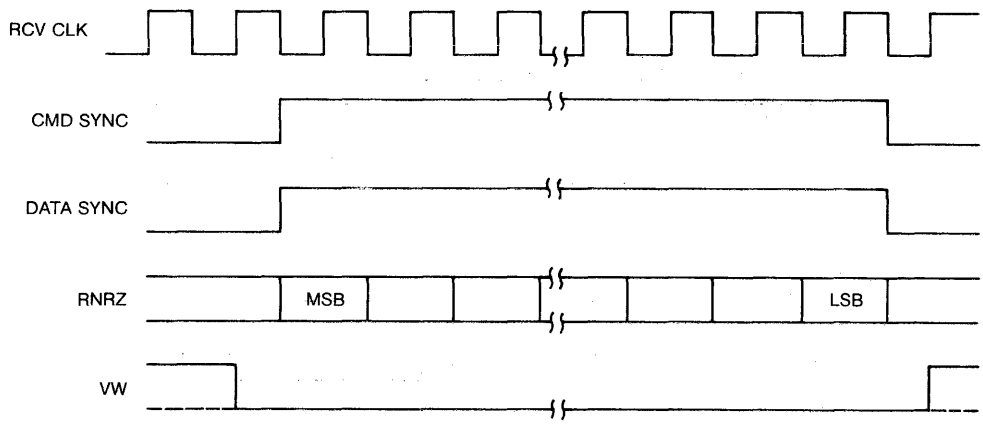
NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A = -55°C to 125°C, V_{CC} = +5 ±5%, unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
Input Voltage Levels					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	3.0			V	
Output Voltage Levels					
Low Level V_{OL}			0.4	V	I_{OL} = -1.6 mA, except open drain
High Level V_{OH}	3.0	4.0		V	I_{OH} = 100 μA, except open drain
Low Level V_{OL}			0.4	V	I_{OL} = -1.6 mA, open drain output
Output Leakage, I_{LO}			10	μA	
Input Current, AD1-AD5		60		μA	V_{IN} = 0V
Output Capacitance		5	10	pf	
Input Capacitance		10	25	pf	
Power Dissipation			500	mW	

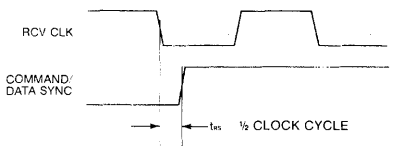
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
AC CHARACTERISTICS						
Clock Frequency	f_T, f_R	980	1000	1020	KHz	
Clock Duty Cycle		45	50	55	%	
Rise and fall times, $\overline{IA}$, $\overline{TDE}$ $\overline{TX\ MODE}$, $\overline{SWE}$, $\overline{RDE}$	tr, tf			20	ns	
rise and fall times, all other inputs	tr, tf			50	ns	
receiver clock-NRZ	t_{RN}			65	ns	figure 3B
receiver clock-sync delay	t_{SR}			85	ns	figure 3B
receiver clock-VW delay	t_{RV}			100	ns	figure 3B
VW reset delay	t_{VS}			500	ns	figure 3C
transmit clock-TX ENA delay	t_{TX}	25			ns	figure 4A
TX ENA pulse width	t_{XW}	60			ns	figure 4A
transmit clock-send data set-up	t_{TS}			40	ns	figure 4B
transmit clock-send data hold time	t_{ST}			140	ns	figure 4C
transmit clock fall to NRZ	t_{TN}	0			ns	figure 4B
transmit clock rise to NRZ	t_{NT}	95			ns	figure 4B
$\overline{TX\ MODE}$ pulse width	t_{MW}	150			ns	figure 5A
$\overline{TX\ MODE}$ to TX ENA delay	t_{MX}			750	ns	figure 5B
VALID word to TX ENA delay	t_{VX}			750	ns	figure 5B
Data sync to TX ENA delay	t_{DX}			750	ns	figure 5C
TX ENA reset delay	t_{SX}			750	ns	figure 5C
DATA SET-up time	t_{D1}	100			ns	figure 6A
$\overline{TDE}$ pulse width	t_{D2}	150			ns	figure 6A
Data Hold time	t_{D3}	100			ns	figure 6A
Cycle time	t_{D4}	450		16000	ns	figure 6A
DTA RQST Delay	t_{D5}	450			ns	figure 6A
Output Enable time	t_{D6}	100			ns	figure 6B
$\overline{RDE}$ Pulse width	t_{D7}	150			ns	figure 6B
receive cycle time	t_{D8}	450		17000	ns	figure 6B
Flag delay time	t_{D9}	450			ns	figure 6B
Output disable time	t_{D10}	100			ns	figure 6B
SEND DATA delay	t_{D11}	2.5		3.5	μs	figure 6C
$\overline{TDE}$ off delay	t_{D12}	1.5			μs	figure 6C
$\overline{TDE1}$ delay	t_{D13}	500			ns	figure 6C
SYN to $\overline{RDE}$	t_{D14}	500			ns	figure 6D
RDE to SYN	t_{D15}			2.5	μs	figure 6D
Status word Enable	t_{SE}			100	ns	figure 8A
Status word Disable	t_{SD}			100	ns	figure 8A
Flag delay time	t_{CF}			1	μs	figure 8B
VW delay time	t_{CV}			90	ns	figure 8B
IVWF delay time	t_{CI}			450	ns	figure 8B
DTA AVL delay time	t_{CD}			500	ns	figure 8B
DTA RQST delay time	t_{SR}			450	ns	figure 8C
$\overline{BRD\ CST}$ delay time	t_{RB}			2	μs	figure 8C
$\overline{BRD\ CST}$ pulse width	t_{BW}	1			μs	figure 8D
flag reset delay	t_{IB}			750	ns	figure 8D, 8E
interrupt delay	t_{RI}			1.5	μs	figure 8D
IA pulse width	t_{IA}	150			ns	figure 8D
Interrupt pulse width	t_{IW}	1			μs	figure 8D
Flag reset time	t_{FR}			450	ns	figure 8F
DTA AVL reset delay	t_{RD}			750	ns	figure 8F
IVWF reset delay	t_{RV}			750	ns	figure 8F
$\overline{MSG\ CMPLT}$ turn-on delay	t_{MR}			1.5	μs	figure 9A, 9B
$\overline{MSG\ CMPLT}$ turn-on delay	t_{MF}			1.5	μs	figure 9A, 9C

RECEIVE TIMING FIGURE 2

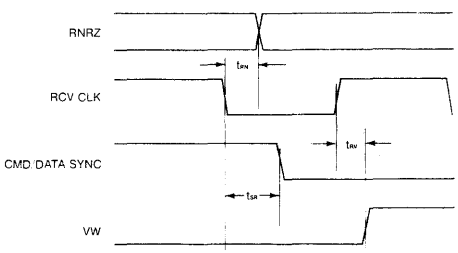


RECEIVER INPUT TIMING FIGURE 3

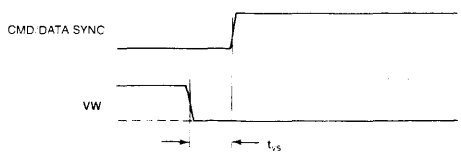
3A



3B

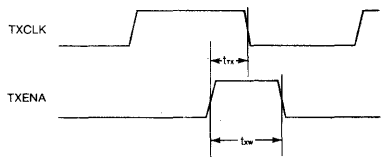


3C

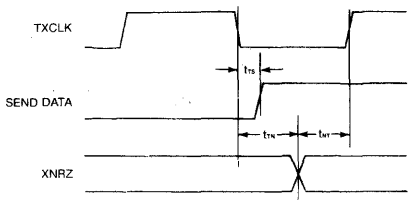


TRANSMITTER TIMING FIGURE 4

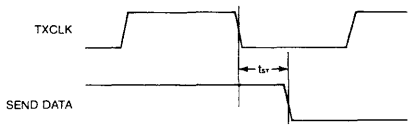
4A



4B

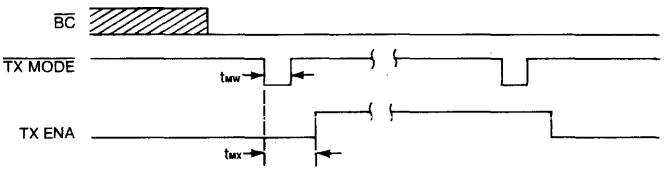


4C

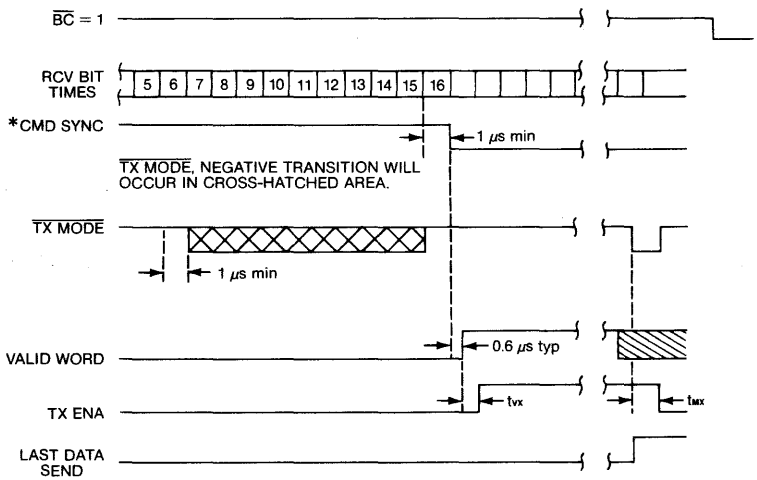


TRANSMIT ENABLE (TX ENA) TIMING FIGURE 5

5A

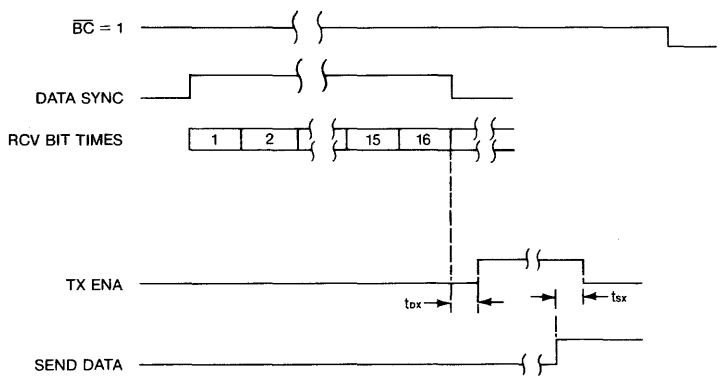


5B*



*THIS IS A CMD WORD BEING RECEIVED, IT IS ADDRESSED TO THIS BUFFER AND THE T/R BIT = 1. TX ENA IS RESET BY 2ND $\overline{TX\ MODE}$ NEGATIVE TRANSITION OR BY LAST SEND DATA (MESSAGE COMPLETE FUNCTION).

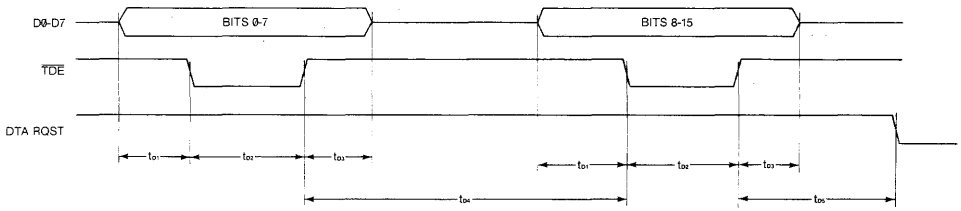
5C**



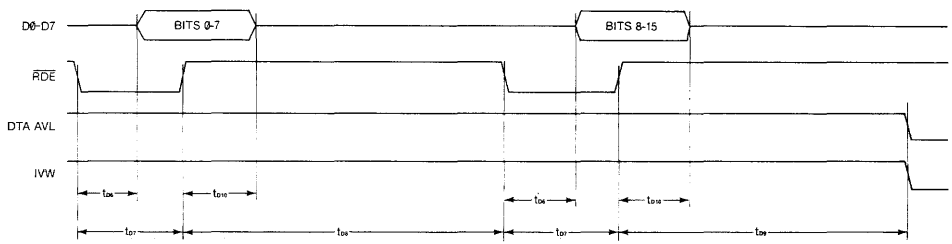
**THIS IS THE LAST DATA WORD BRING RECEIVED. THIS TERMINAL PREVIOUSLY HAD RECEIVED A REC CMD WORD WITH OUR ADDRESS AND A REC/XMIT BIT = 0 DURING THIS MESSAGE SEQUENCE. TX ENABLE IS SET BY $\overline{MSG\ CMPLT}$ FUNCTION AND RESET BY RECEIPT OF SEND DATA.

DATA BUS TIMING FIGURE 6

6A

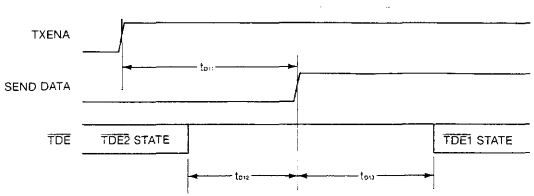


6B



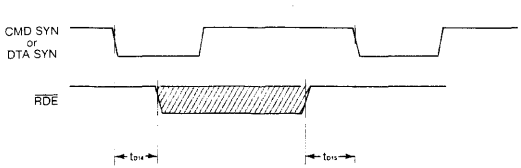
DATA BUS TIMING FIGURE 6

6C

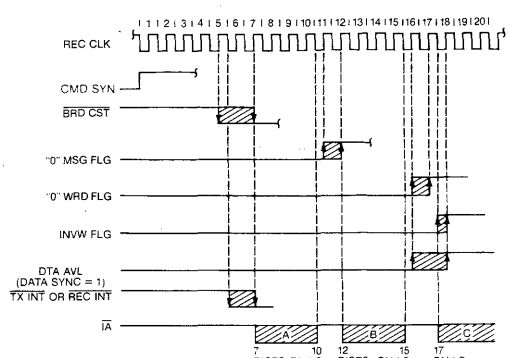


NOTE: SEND DATA RISING EDGE INITIALIZES $\overline{TDE}$ TO $\overline{TDE1}$ STATE

6D



$\overline{IA}$ RESETS FIGURE 7



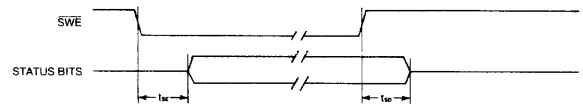
$\overline{IA}$ OCCURRING DURING ZONE A RESETS: BRD CST. TX INT. REC INT.

$\overline{IA}$ OCCURRING DURING ZONE B RESETS: BRD CST. TX INT. REC INT. "0" MSG FLG.

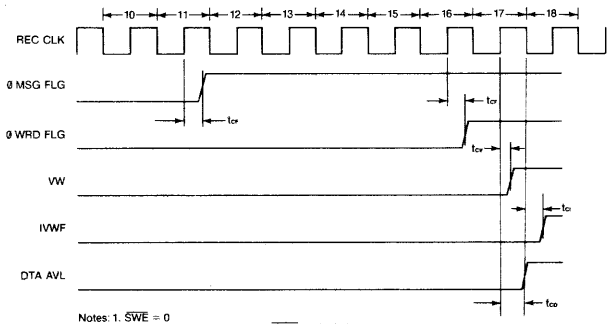
$\overline{IA}$ OCCURRING DURING ZONE C RESETS: BRD CST. TX INT. REC INT. "0" MSG FLG. "0" WRD FLG.

STATUS FLAGS FIGURE 8

8A

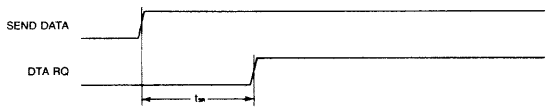


8B

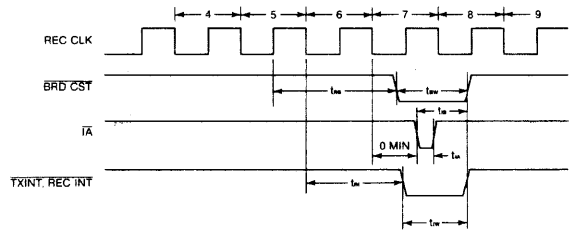


Notes: 1. $\overline{SWE}$ = 0
2. IVWF and DTA AVL reset by $\overline{RDE2}$ or REC CLK 14 of the next word

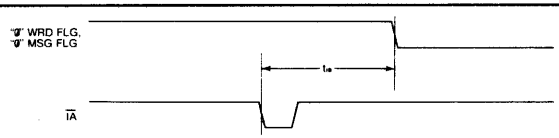
8C



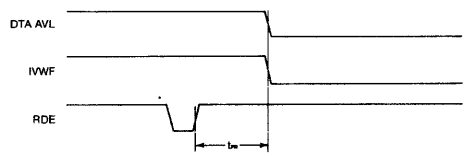
8D



8E

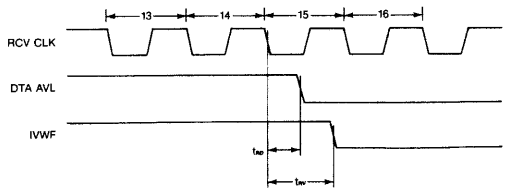


8F



*RDE 2

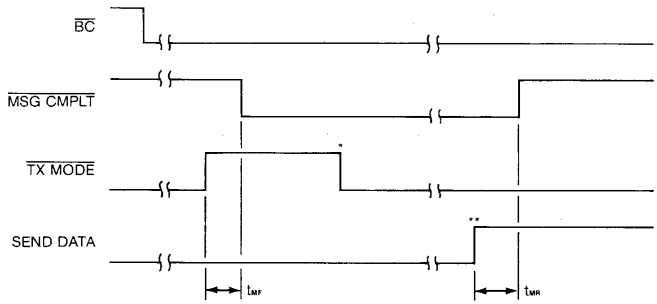
If RDE is not used to reset IVWF and RDE, then they are reset by RCV CLK 14 as shown below.



MESSAGE COMPLETE FIGURE 9

BUS CONTROLLER MODE

9A

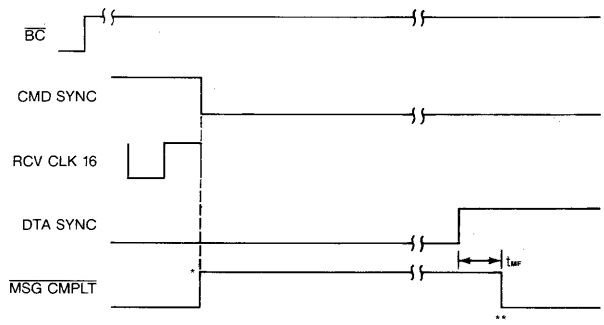


*WORD COUNTER IS PRESET TO 33

**MSG CMPLT SET t_{MR} MAX AFTER RISE OF 33RD SEND DATA PULSE

REMOTE TERMINAL, RECEIVE COMMAND RECEIVED

9B

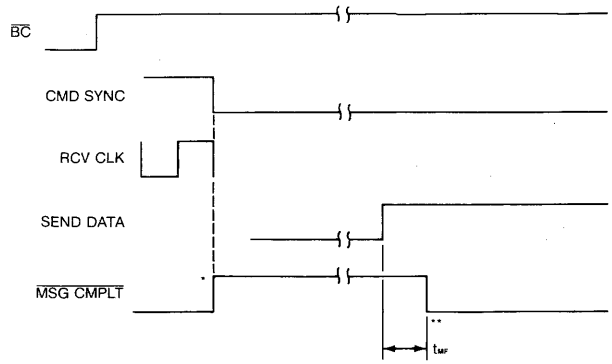


*WORD COUNTER PRESET TO COUNT IN COMMAND WORD

**MSG CMPLT GENERATED BY LAST DATA SYNC OF THE MESSAGE GROUP

REMOTE TERMINAL, TRANSMIT COMMAND RECEIVED

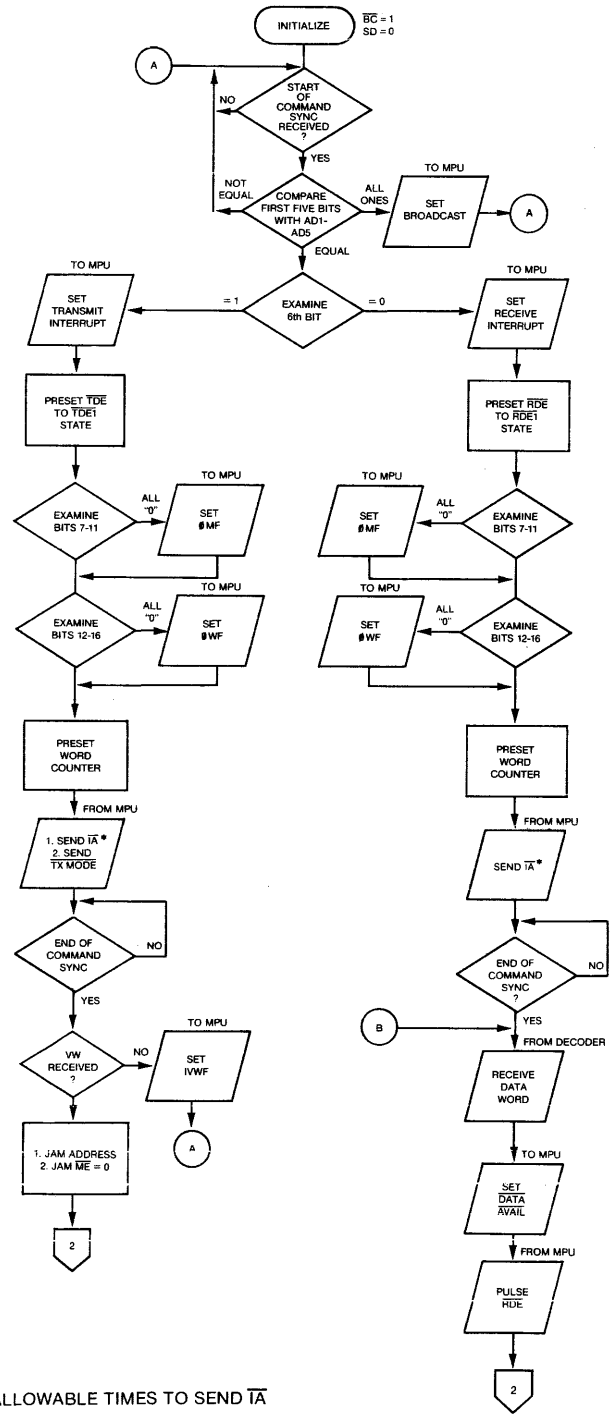
9C



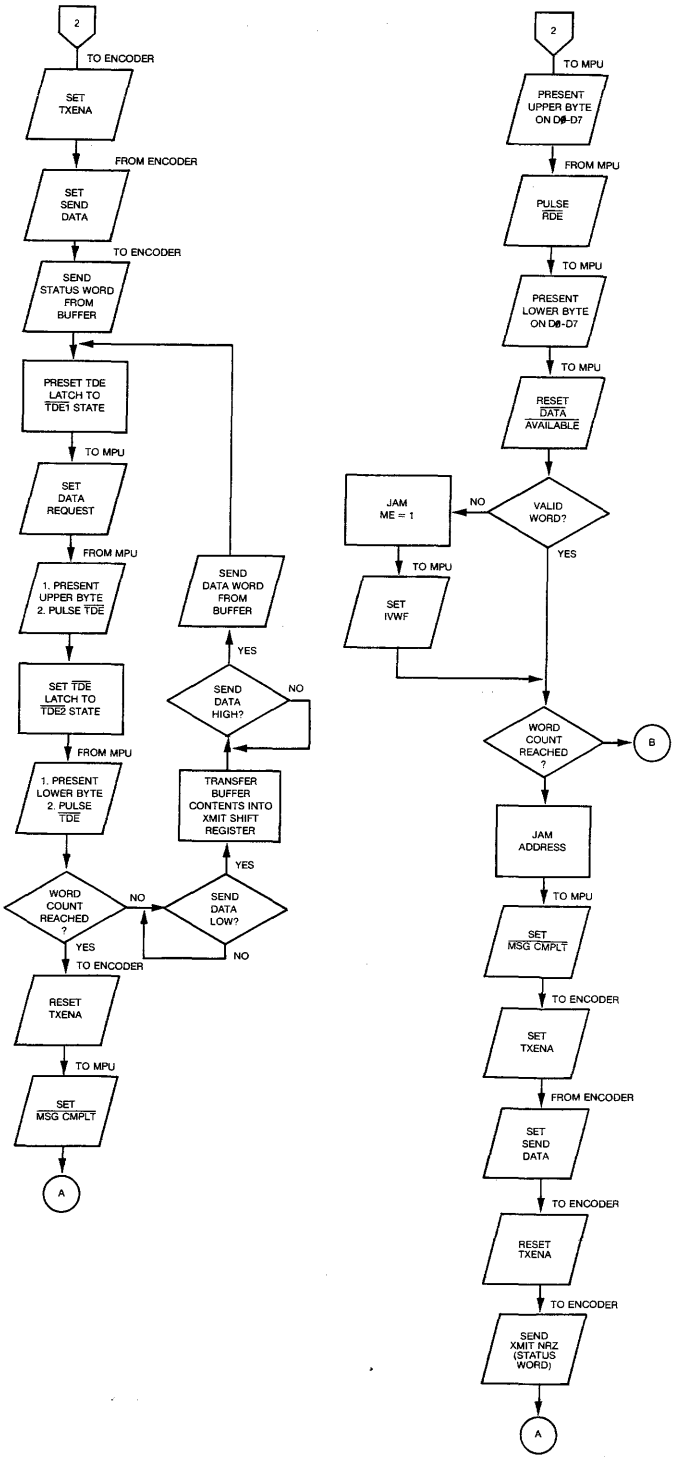
*WORD COUNTER PRESET TO TRANSMIT COMMAND WORD FIELD PLUS 1. THIS ALLOWS FOR THE STATUS WORD.

**MSG CMPLT GENERATED BY THE LAST SEND DATA OF THE TRANSMIT MESSAGE GROUP.

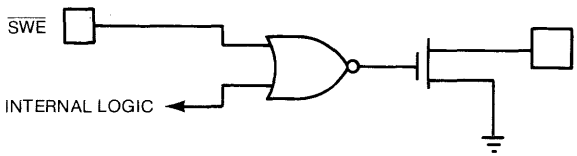
TYPICAL SYSTEM OPERATION



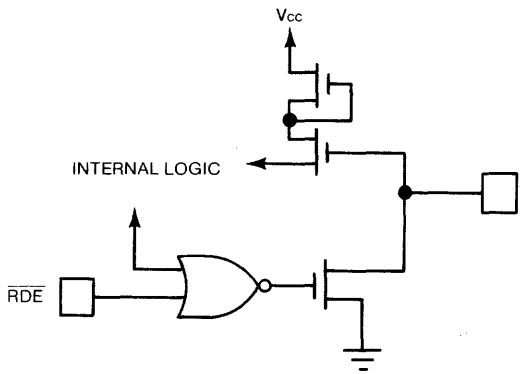
*SEE FIGURE 7 FOR ALLOWABLE TIMES TO SEND $\overline{IA}$


2
TO ENCODER
SET TXENA
FROM ENCODER
SET SEND DATA
TO ENCODER
SEND STATUS WORD FROM BUFFER
PRESET TDE LATCH TO TDE1 STATE
TO MPU
SET DATA REQUEST
FROM MPU
1. PRESENT UPPER BYTE 2. PULSE TDE
SET TDE LATCH TO TDE2 STATE
FROM MPU
1. PRESENT LOWER BYTE 2. PULSE TDE
WORD COUNT REACHED ?
NO
YES
TO ENCODER
RESET TXENA
TO MPU
SET MSG CMPLT
A
SEND DATA LOW?
NO
YES
TRANSFER BUFFER CONTENTS INTO XMIT SHIFT REGISTER
SEND DATA HIGH?
NO
YES
SEND DATA WORD FROM BUFFER
2
TO MPU
PRESENT UPPER BYTE ON D8-D7
FROM MPU
PULSE RDE
TO MPU
PRESENT LOWER BYTE ON D8-D7
TO MPU
RESET DATA AVAILABLE
VALID WORD?
NO
YES
JAM ME = 1
TO MPU
SET IVWF
WORD COUNT REACHED ?
B
JAM ADDRESS
TO MPU
SET MSG CMPLT
TO ENCODER
SET TXENA
FROM ENCODER
SET SEND DATA
TO ENCODER
RESET TXENA
TO ENCODER
SEND XMIT NRZ (STATUS WORD)
A

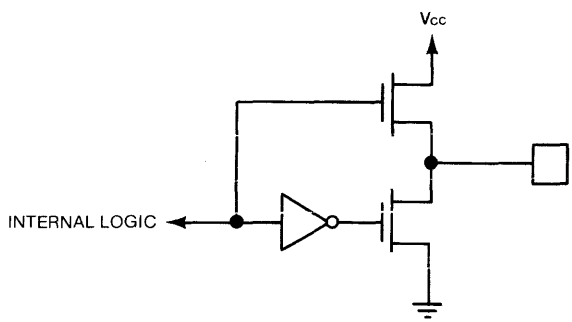
OPEN DRAIN OUTPUT
FIGURE 10



DØ-D7 INPUT/OUTPUT
FIGURE 11



OTHER OUTPUTS
FIGURE 12

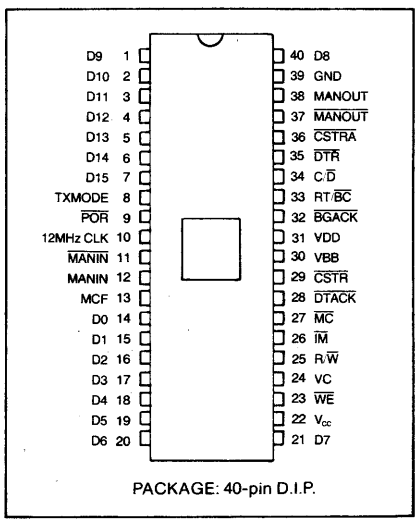


MIL-STD-1553B "SMART®"

FEATURES

- ☐ Support of MIL-STD-1553B
- ☐ Operates as both Remote Terminal and Bus Controller
- ☐ Manchester II Serial Biphase Input/Output
- ☐ 16 bit Microprocessor compatible
- ☐ Command/Data Sync Detection/Identification
- ☐ Automatic Command Response Generation
- ☐ On-Chip Address Recognition
- ☐ Error Detection For:
  - Sync Errors
  - Parity Errors
  - Word Count Errors
  - Bit Count Errors
  - Invalid Manchester Code
  - Incorrect Address
  - Incorrect Bus Response Time
- ☐ TTL Compatible
- ☐ Recognizes Mode Codes and Broadcast Commands
- ☐ Provides DMA handshaking signals
- ☐ COMPLAMOS® n-Channel MOS Technology

PIN CONFIGURATION



PACKAGE: 40-pin D.I.P.

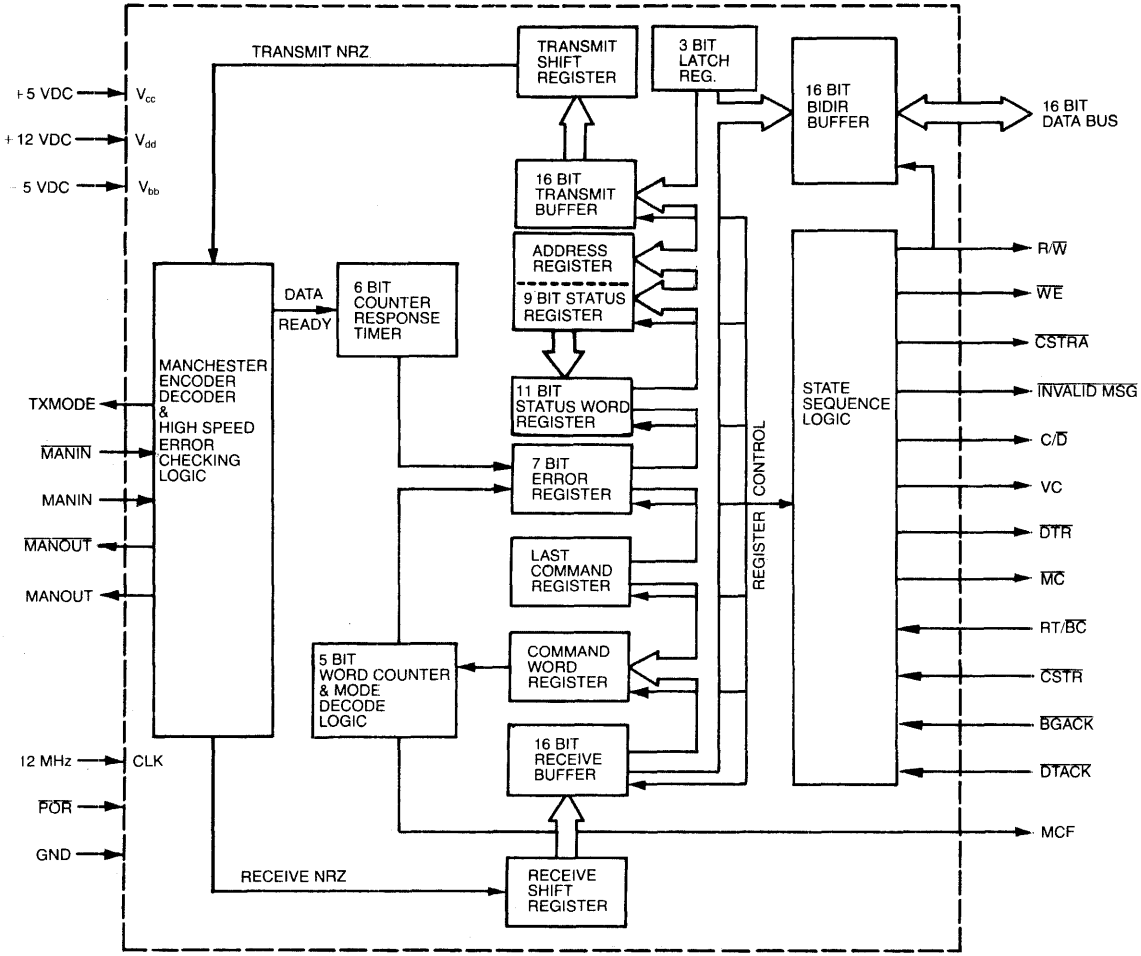
GENERAL DESCRIPTION

The COM1553B SMART® (Synchronous Mode Avionic Receiver-Transmitter) is a 40-pin COPLAMOS® n-Channel MOS/VLSI circuit designed to simplify the interface of a microprocessor or buffer to the serial MIL-STD-1553B data bus.

The COM1553B is a double buffered serial to parallel, parallel to serial converter. It receives serial Manchester II biphase encoded data from a 1553B bus receiver and converts it to 16 bit parallel data. When receiving Manchester II data, the COM1553B detects and identifies sync polarity, reconstructs the clock, detects zero crossing, checks for the proper number of bits and performs a parity check on the incoming data. In addition to parity check, the COM1553B also checks for sync errors, invalid Manchester code, improper word count, incorrect address and incorrect bus response time. The transmitter in turn, accepts 16 bits parallel data and serially transmits it as Manchester II data, appending the appropriate sync and parity.

The COM1553B recognizes protocol commands, and automatically generates the proper response, thereby offloading what otherwise would be microprocessor tasks. This feature eliminates critical software timing requirements.

The COM1553B is designed to work both as a Bus Controller and Remote Terminal, making it universal within the MIL-STD-1553B environment. The COM1553B automatically loads and recognizes its own address. It determines the type of transfer required in both the Bus Controller and Remote-Terminal modes and generates the proper control signals to complete the transfer. It automatically transmits the status word and detects message errors and mode commands. Furthermore, it generates the control signals for DMA operation, therefore eliminating processor intervention.



FUNCTIONAL BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1-7, 14-21, 40	16-bit Data Bus	D0-D15	Three-state bidirectional data lines used to transfer Command, Data, Error and Status Words between the COM1553B and external memory.
8	Transmit Mode	TXMODE	This output signal when high indicates that the COM1553B is transmitting information on the 1553B bus.
9	Power On Reset	$\overline{\text{POR}}$	Input signal used to initialize or reset the Error registers. The RT address must be reloaded after POR is issued.
10	12 MHz Clock	12 MHz CLK	12 MHz clock input.
11	Complementary Manchester In	$\overline{\text{MANIN}}$	This input is low when there is no data on the bus. A high level indicates that the data is in its negative state (Refer to receive waveform, figure 3).
12	Manchester In	MANIN	This input is low when there is no data on the bus. A high level indicates that the data is in its positive state (Refer to receive waveform, figure 3).
13	Mode Code Flag	MCF	Output signal that is active high when a mode command (all 1's or all 0's in subaddress) has been detected.
22	Power Supply	VCC	+5 volts DC supply.
23	Write Enable	$\overline{\text{WE}}$	Output signal. When low, $\overline{\text{WE}}$ indicates that the data on the 16 bit data bus is stable and can be written into the external memory.
24	Valid Command	VC	Output signal that is pulsed high to signify the reception of a valid command.
25	Read/Write	R/$\overline{\text{W}}$	Output signal that indicates whether a DMA transaction is a COM1553B read (when high) or a write (when low) operation.
26	Invalid Message	$\overline{\text{IM}}$	Output signal which is pulsed low at the same time as MC to indicate that a message error has occurred. IM is also pulsed low while MC remains high if there are errors in the Command word with matching address.
27	Message Complete	$\overline{\text{MC}}$	Output signal used as either an interrupt or flag to the processor whenever a COM1553B transaction has been completed.
28	Data Transfer Acknowledge	$\overline{\text{DTACK}}$	This input signal when low indicates that the Data Transfer Request ($\overline{\text{DTR}}$) and $\overline{\text{BGACK}}$ has been acknowledged and data is on the data bus.
29	Command Strobe	$\overline{\text{CSTR}}$	This input signal when low is used to inform the COM1553B that a Command Control Code is available in external memory. When the COM1553B is ready, it issues a Command Strobe Acknowledge and initiates a memory read cycle to load the Command Control Code bits CB2-CB0.
30	Power Supply	VBB	−5 volts DC supply voltage.
31	Power Supply	VDD	+12 volts DC supply.
32	Bus Grant Acknowledge	$\overline{\text{BGACK}}$	This input signal, when low, indicates that the processor has acknowledged $\overline{\text{DTR}}$ and relinquished the data bus.
33	Remote Terminal/Bus Controller	RT/$\overline{\text{BC}}$	When this input is high the COM1553B operates as a Remote Terminal. When RT/$\overline{\text{BC}}$ is low, the COM1553B operates as a Bus Controller.
34	Command/Data	C/$\overline{\text{D}}$	This output signal during memory write operations indicates either a Command or Data Word transfer. A low level indicates that the COM1553B is writing a Data Word, Status Word, the contents of the Error Register, or the contents of the Last Command Register into external memory. A high level indicates that the transferred word is a Command Word. During memory read operations this output is low. It goes high to indicate that data has been latched internally and the read operation is completed.
35	Data Transfer Request	$\overline{\text{DTR}}$	Output signal that initiates a DMA transfer with the processor.
36	Command Strobe Acknowledge	$\overline{\text{CSTRA}}$	This output pulse acknowledges the receipt of the command strobe and initiates the Command Control Code (CB2-CB0) transfer.
37	Complementary Manchester Output	$\overline{\text{MANOUT}}$	This output signal is high when the COM1553B is not transmitting. A low level indicates that output data is in a positive state (refer to driver waveform, figure 4).
38	Manchester	MANOUT	This output signal is high when the COM1553B is not transmitting. A low level indicates that output data is in a negative state (refer to driver waveform, figure 4).
39	Ground	GND	Ground

FUNCTIONAL DESCRIPTION

The COM1553B is organized into the following five sections:

Manchester Encoder/Decoder

This section performs the manchester encoder and decoder functions and code error check. The receiver continuously monitors the MANIN and the $\overline{\text{MANIN}}$ input lines for a valid sync. After the reception of the 3 bit sync, the receiver is in full synchronization. It then checks for transition errors and correct (odd) parity. If an error is detected in the Command Word the receiver resets itself, pulses IM and waits for another valid sync. If any errors are detected in Data and Status Words, the appropriate error bits in the Status and Error register are set.

The transmitter section encodes the NRZ data from the data bus into Manchester II and appends, depending on word type, the proper sync and parity.

State Sequencer Logic

The State Sequencer section generates the appropriate signals to various internal sections to control the overall device operation.

Inputs to the State Sequencer which establish its operational modes are as follows:

Remote Terminal/Bus Controller (RT/$\overline{\text{BC}}$)

Determines whether the data terminal is operating as a Remote Terminal or as a Bus Controller. As a result of Dynamic Bus Allocation, any terminal shall be capable of performing either function at different times.

Command Control Code bits D2-D0 (CB2-CB0)

These Command Control Code bits determine the type of memory operation the COM1553B will execute. Transfer of these commands to the COM1553B are initiated by asserting Strobe Command ($\overline{\text{CSTR}}$) low. This informs the COM1553B that a command is available in external memory. When the COM1553B acknowledges the $\overline{\text{CSTR}}$ signal, it sets the $\overline{\text{CSTRA}}$ output low. The $\overline{\text{CSTR}}$ must be reset within 1.5 μs. The COM1553B then initiates a memory read cycle by setting R/$\overline{\text{W}}$ high, C/$\overline{\text{D}}$ low, and DATA TRANSFER REQUEST ($\overline{\text{DTR}}$) low. When the Command Control Code bits are valid on the bidirectional data bus (D2-D0), $\overline{\text{DTACK}}$ and $\overline{\text{BGACK}}$ are generated by the processor and these bits are loaded into the COM1553B 3-bit latch decode register. The command is then decoded in accordance with Table A. Timing associated with loading these control bits into the COM1553B is shown in Figure 1.

Transmit Last Command

Allows the State Sequencer to bypass a memory read cycle to external memory and transmit the Last Command from the TRLC register following the Status Word transmission.

Broadcast

When the address field of the Command Word is all ones (11111), the State Sequencer is informed that a Bus Controller or a Remote Terminal is transmitting a Broadcast Command.

Word Count Zero

Input from the 5-bit counter and count decode logic informing the State Sequencer that all Data Word memory cycles are complete.

Sync Input

Indicates the type of sync word just strobed into the receive register.

Address Compare

When programmed as a Remote Terminal, the COM1553B compares the contents of the address register with the address field of the received Command Word. If the addresses compare, the State Sequencer will respond to the received command.

Any Error

This input to the State Sequencer indicates that one of the seven possible errors have been set in the error register at the end of a message (Refer to Error register).

Contiguous Word

Set if there is a transition 2 μs. after the parity transition of the last word, this signifies that a contiguous word follows the word presently in the receive register (Refer to figure 5).

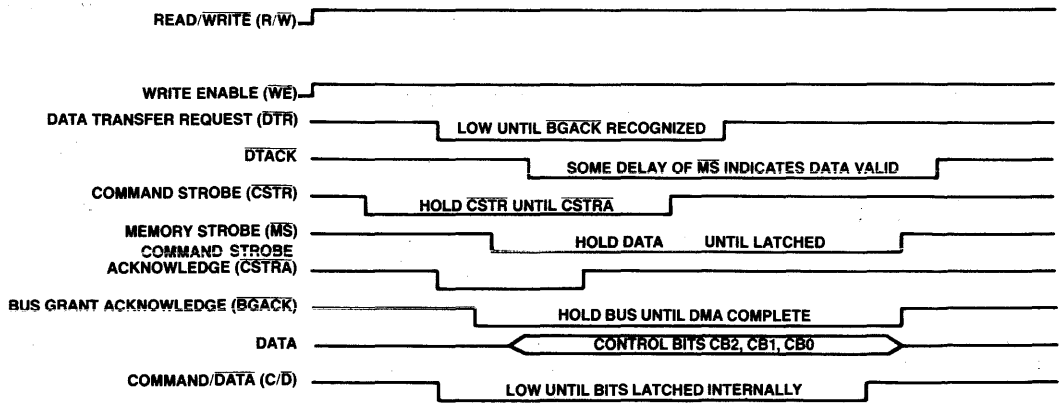


FIGURE 1:
BUS CONTROLLER TIMING SEQUENCE

Loading the Command Control Code Bits into the COM1553B prior to transmitting a Command or initiating a Diagnostic Sequence.

Error Detection Logic

The error detection logic of the COM1553B detects the following errors:

Improper Sync

One or more words have been received with incorrect sync polarity (For example a Status Word with Data Sync).

Invalid Manchester II Code

One or more words have been received with a missing transition during the 17 μs. data and parity bit time.

Information Field Greater Than 16 Bits

The decoder has detected a transition within one bit time (1 μs.) following the parity bit in one or more words.

Odd Parity Error

One or more words have been received with a parity error.

Improper Word Count

An improper word count error occurs when the number of Data Words received is not equal to the number of words indicated in the word count field of the Command Word. In the case of a Mode Code without data, no Data Words should follow the Mode command. Mode Codes with data should consist of only one Data Word. If the contents of the word counter are not zero, and there is no contiguous Data Word, then the receive message is considered incomplete (e.g., fewer words were received than indicated by the word count in the Command word). If the contents of the word counter are zero and there is a transition detected 2 μs. after the parity transition of the last Data Word, then this also will cause an improper word count. In either case, the Message Error bit of the Status Word is set and not transmitted and the invalid message ($\overline{IM}$) output pin pulsed at the same time as the message complete ($\overline{MC}$) signal output.

Response Time

The amount of time between the end of transmission of a Command or Data Word and the Status Word reply by a Remote Terminal should be less than 14 μs. If the response is greater than 14 μs. the response error bit is set in the error register.

Address Mismatch

An address mismatch occurs when a Bus Controller detects a mismatch between the address of the Status Word reply from a Remote Terminal and the Remote Terminal address of the Command.

Internal Register Description

Remote Terminal Address And Status Code Register

This register is loaded when the processor issues a load Remote Terminal Address (RTA) command. The word that is loaded in this register consists of 9 bits of status information (D0-D8) and the 5-bit address (D11-D15). The Remote Terminal Address may be checked any time by reading out the Error register. The RTA and Status Code register must be loaded before the COM1553B may respond as a Remote Terminal.

Table 1 defines the data bus bits which correspond to the Remote Terminal Address and Status Code register and Status Word that transmitted. Bits D0, D2, D3 and D8 are double buffered to allow the RT to retain this information after the Status Code register is updated. For all legal commands, other than Transmit Last Status and Transmit Last Command Mode command, the Status Word register is updated with these four bits, Any Error and the Broadcast flag. The Dynamic Bus Control and Terminal Flag bits are modified by the appropriate Mode Code commands whereas, the Broadcast Flag and Any Error bits are set by the COM1553B internal logic. The Reserved Bits and the RT address bits are transferred directly into the Status Word register during the RTA and Status Code command.

Bits D0, D2, D3, and D5-D9 are cleared after transmission for all commands except Transmit Last Status and Transmit Last Command Mode Code.

TABLE A:
COMMAND CONTROL CODE BIT DEFINITION

	DATA BITS													CONTROL BITS CB2-CB0			
RT/$\overline{BC}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	FUNCTION
X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	X	READ DATA REGISTER
X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	X	LOAD RT ADDRESS REGISTER AND STATUS CODE REGISTER
X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	READ LAST CMD
X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	1	READ ERROR AND REMOTE TERMINAL ADDRESS REGISTERS
0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	0	BUS CONTROLLER TRANSMISSION
0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	1	BUS CONTROLLER RT TO RT TRANSFER

X—DON'T CARE

TABLE 1

Data Bus Bit	RTA and Status Code Reg. Bits	Internal Logic Signals	Status Word Transmitted
D15 (MSB)	RTA Bit 4 (MSB)	—	RTA Bit 4 (MSB)
D14	RTA Bit 3	—	RTA Bit 3
D13	RTA Bit 2	—	RTA Bit 2
D12	RTA Bit 1	—	RTA Bit 1
D11	RTA Bit 0 (LSB)	—	RTA Bit 0 (LSB)
D10	Not used	Any Error	Message Error
D9	Instrumentation Bit	—	Instrumentation
D8	Service Request Bit	—	Service Request
D7	Reserved	—	Reserved
D6	Reserved	—	Reserved
D5	Reserved	—	Reserved
D4	Not Used	Broadcast Flag	Broadcast Flag
D3	Busy	—	Busy
D2	Subsystem Flag Bit	—	Subsystem Flag
D1	Dynamic Bus Control Acceptance Enable Bit (See Note)	Dynamic Bus Mode Code command	Dynamic Bus Control Bit
D0 (LSB)	Terminal Flag Enable Bit (See Note)	Inhibit Terminal Flag (set) or Override Terminal Flag (reset) Mode Code command	Terminal Flag

Note: When the Dynamic Bus Control Acceptance Enable bit is set, the RT will accept a Dynamic Bus Mode code request. If this bit is reset the RT will reject a Dynamic Bus Mode Code command request. The Terminal Flag Bit (if enabled) is only set high if no Inhibit Terminal Mode Code command has been received, or if an Override Inhibit Terminal bit command is received.

Last Command Word Register

The last valid Command Word received by a Remote Terminal is stored in an internal 16 bit Last Command Register. This makes it readily available for transmission onto the data bus whenever the Remote Terminal receives a Mode Command to transmit the last Command Word. The Last Command Register contents are automatically written into external memory following a receive or a transmit message.

As a bus controller (BC), the Last Command Register is used to hold the command transmitted before the present command. In RT-RT transfers this register of the BC holds the receive command while the transmit command is being transmitted.

The processor has the option of reading the Last Command Register of either a bus controller or remote terminal, by issuing a Read Last Command Register command code.

Error Register And RTA Register (Error Register)

A 7-bit error register is provided in the COM1553B to hold any errors associated with the previous message. If one or more of the 7 error types exists, the COM1553B asserts the Invalid Message output pin ($\overline{IM}$) at the same time that Message Complete (MC) is asserted, cueing either a Remote Terminal or a Bus Controller that an error occurred in the previous message. If desired, the processor may read out the 16-bit error word by issuing a read error register command code. When operating as a Remote Terminal, the COM1553B will write the Receive register, Error register and Last Command register automatically into external memory at the end of each command message because these registers may change before the processor has determined the necessity of reading them. The Error register may be read anytime during a message except during message transfers.

TABLE 2

The 16-bit error word is defined as follows:

DATA BUS LINE	ERROR BIT DEFINITION
D15	RT Address Bit 4
D14	RT Address Bit 3
D13	RT Address Bit 2
D12	RT Address Bit 1
D11	RT Address Bit 0
D10	Unused
D9	Improper Sync
D8	Address Mismatch Error
D7	Improper Word Count
D6	Response Time Error
D5	Information Field > 16 Bits
D4	Unused
D3	Invalid Manchester II
D2	Parity Error
D1	Unused
D0	Unused

*Unused bits are set high.

Mode Detection Logic

Both receive and transmit Command Words for a Remote Terminal and Bus Controller are decoded by the Mode Detection Logic. The Mode Detection Logic examines the following Command Word field to establish the correct operating mode for the COM1553B (Refer to TABLE B).

Subaddress/Mode Code Field (D5-D9) and Data Word Count/Mode Code (D0-D4)

This field Determines if the command is a normal command or a Mode command. A subaddress field of 00000 or 11111 implies a Mode command. All other codes are interpreted as a subaddress. Once a Mode Command is detected the most significant bit of the Data Word Count/Mode Code field is decoded. A most significant bit of "zero" implies no associated data with the Code Command. A "one" in this position implies that a Data Word will follow.

The COM1553B recognizes five Mode Code commands (Refer to TABLE B). Transmit Last Command or Transmit Last Status word Mode Code commands, when received by the COM1553B, will automatically transfer the contents of the Transmit Last Command or Transmit Last Status register onto the 1553B serial bus.

The Override/Inhibit Terminal Flag and Dynamic Bus Control Mode Code commands, when received by the COM1553B, may change the state of the Terminal Flag and Dynamic Bus Control bits of the Status Word register. The Inhibit Terminal Flag Bit Mode Code command resets the Terminal Flag bit.

The Override Inhibit Terminal Flag Mode Code command enables the Terminal Flag bit if it was previously disabled. Finally, Dynamic Bus Control Mode Code command sets the Dynamic Bus Control bit in the Status Word if the Dynamic Bus Control Enable bit is high. If the enable bit is low, the Dynamic Bus Control bit in the Status Word remains low when a Dynamic Bus Control Mode Code command is received.

Broadcast Mode Code

Broadcast Mode Code Commands are acknowledged if the T/$\overline{R}$ bit is low. If the T/$\overline{R}$ bit is high all Broadcast Mode Code commands without associated Data words are acknowledged except Dynamic Bus Control and Transmit Last Status Word.

Illegal Broadcast Commands are not acknowledged; the IM output pin is, however, pulsed low.

TABLE B
MODE CODE DEFINITION

FUNCTION	DETECT CONDITION	DETECTED BY	SPECIAL CONDITIONS	COMMENTS
Broadcast	All ones in RT address field of CMD WD	Broadcast Decode Logic	Status word is written into Memory but not transmitted	Address compare must recognize all ones as Broadcast
Mode Codes	All zeros or ones in sub-address field of CMD WD	Mode Code Decode Logic	MSB of Word Count 0 = No data Word 1 = With Data Word	Word Count is Decoded as mode code
(1) Dynamic Bus Control			Word Count Field = 00000	Dynamic Bus Accept Bit of Status word enabled for transmission
(2) Transmit Last Status Word			Word Count Field = 00010	Status Word remains unchanged
(3) Inhibit Terminal Flag Bit			Word Count Field = 00110	Terminal Flag Bit of Status word inhibited until overriden
(4) Override Inhibit Terminal Flag Bit			Word Count Field = 00111	Removes Inhibit from Terminal Flag Bit of Status Word
(5) Transmit Last Command			Word Count Field = 10010	Status Word Transmitted followed by Last Command Register. Status Word remains unchanged.

OPERATION

When operating as either a Bus Controller or Remote Terminal, the COM1553B decodes the Command Word and determines the type of message transfer. Having determined the type of message transfer, the COM1553B generates the proper control and timing signals to complete the transfer (refer to Figure 2). The types of messages are listed below:

1) Bus Controller to Remote Terminal
2) Remote Terminal to Bus Controller
3) Remote Terminal to Remote Terminal
4) Mode Code without Data Word
5) Mode Code with Data Word (transmit)
6) Mode Code with Data Word (receive)
7) Broadcast Bus Controller to Remote Terminal
8) Broadcast Remote Terminal to Remote Terminal
9) Broadcast Mode Code without data
10) Broadcast Mode Code with data

Bus Controller Transaction (RT/$\overline{BC}$ of the COM1553B set low)

The following section describes each 1553B information transfer format from the Bus Controller viewpoint. A table showing external memory operation is also provided for each message format.

Note that all MIL-STD-1553B serial bus activity is initiated by the Bus Controller.

Bus Controller-to-Remote Terminal Transfer (BC to RT)

This message format covers transactions where the Bus Controller transmits a receive Command and Data Words to a Remote Terminal. Initializing the COM1553B is accomplished by the processor loading an external memory address counter with the starting address of the COM1553B memory control block (address where the Command Control Code CB2-CB0 resides). The Bus Controller processor next issues a Command Strobe ($\overline{CSTR}$) and holds it low until the COM1553B issues a Command Strobe Acknowledge ($\overline{CSTRA}$). The COM1553B then responds with a Data Transfer Request ($\overline{DTR}$) which initiates a normal memory cycle.

Refer to figure 1 for timing associated with loading the Command Control Codes (CB2-CB0) into the COM1553B prior to transmitting the Command Word.

The first memory cycle loads the Command Control Code bits CB2-CB0 from external memory into the COM1553B functioning as Bus Controller (BC). The BC decodes this command to determine the type of memory transaction to perform (refer to TABLE A). The next read cycle loads the Command Word into the BC command register and then transmits it onto the 1553B bus. This Command Word, while in the command register, determines the BC mode of operation. The BC then completes this BC to RT transaction by issuing a predetermined number of read cycles (determined by the value in the word count field of the Command Word) and transmitting the data onto the 1553B bus. After transmission of the last Data word, the BC initializes its response timer, expecting a Status Word from the remote terminal within 14 μs.

After the reception of the Status Word, the BC initiates a memory write cycle which writes the Status Word into the external memory. If the BC doesn't receive the Status Word within the allowed response time the message error bit is set.

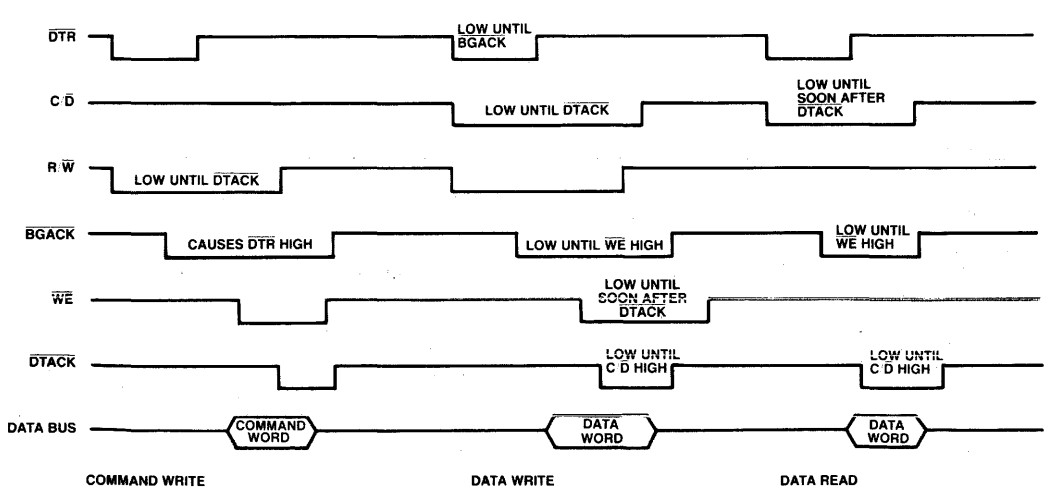


FIGURE 2

TABLE 3
BC to RT (The BC transmits a receive command to the RT)

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX2_H$	READ*
2	RECEIVE COMMAND	READ
3	DATA	READ
•	DATA	READ
•	DATA	READ
32	DATA	READ
	**	
33	STATUS	WRITE

*reads command control code bits CB2-CB0
** response time
X = don't care

Remote Terminal Transfer to Bus Controller

This message format covers transactions where the Bus Controller sends a transmit command to a Remote Terminal and requests data from it. Initialization of the BC for normal memory cycles is the same as the previous transfer. The difference between this transfer and the previous transfer is that after the Command Word is transmitted, the BC waits 14 μs for the Status Word and the requested number of Data Words. The Status and Data Words are written into external memory via write cycles as they are received by the BC.

TABLE 4
BC to RT (The BC transmits a Transmit Command to an RT)

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX2_H$	READ*
2	TRANSMIT COMMAND	READ
	**	
3	STATUS	WRITE
4	DATA	WRITE
•	DATA	WRITE
•	DATA	WRITE
36	DATA	WRITE

*reads command control code bits CB2-CB0
** response time
X = don't care

RT-to-RT Transfer

In this message format, the Bus Controller first issues a receive Command Word to the receiving Remote Terminal, followed by a transmit Command Word to the transmitting terminal. Next, the transmitting RT responds with a Status Word and the requested number of Data Words to both the receiving RT and BC. The receiving RT at the end of the message sends a Status Word to the BC. As Status and Data Words are received by the BC they are written into external memory.

TABLE 5
RT to RT

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX3_H$	READ*
2	RECEIVE COMMAND	READ
3	TRANSMIT COMMAND	READ
4	STATUS (transmitting RT)	WRITE
5	DATA	WRITE
•	DATA	WRITE
•	DATA	WRITE
36	WRITE	
	**	
37	STATUS (receiving RT)	WRITE

*reads command control code bits CB2-CB0
** response time
X = don't care

Mode Code Command without Data

The Bus Controller transmits a specific Mode Command and expects a Status Word back from the addressed Remote Terminal.

TABLE 6

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX2_H$	READ*
2	COMMAND	READ
	**	
3	STATUS	WRITE

*reads command control code bits CB2-CB0
** response time
X = don't care

Mode Command with Data
(BC receives a single word)

In this mode the Bus Controller issues a transmit Mode Command to an RT. The addressed Terminal responds to the Bus Controller with a Status Word and a single Data Word.

TABLE 7

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX2_H$	READ*
2	COMMAND	READ
	**	
3	STATUS	WRITE
4	DATA	WRITE

*reads command control code bits CB2-CB0
** response time
X = don't care

Mode Command with Data
(BC transmits a single word)

The Bus Controller issues a receive Mode Command and one Data Word to a Remote Terminal. A Status Word is returned by the Remote Terminal to the Bus Controller.

TABLE 8

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX2_H$	READ*
2	COMMAND	READ
3	DATA	READ
	**	
4	STATUS	WRITE

*reads command control code bits CB2-CB0
** response time
X = don't care

Bus Controller (Broadcast) to Remote Terminal Transfer

In this mode the Bus Controller issues a Broadcast Command followed by a number of Data Words. In all Broadcast Command transfers a BC will not expect to receive a Status Word back.

TABLE 9

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX2_H$	READ*
2	RECEIVE COMMAND	READ
3	DATA	READ
•	DATA	READ
•	DATA	READ
34	DATA	READ

*reads command control code bits CB2-CB0
** response time
X = don't care

RT to RT Transfer (Broadcast)

This transfer is similar to the normal RT to RT transfer with the exception that the Status Word is not returned by the receiving RT.

TABLE 10

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX3_H$	READ*
2	RECEIVE COMMAND	READ
3	TRANSMIT COMMAND	READ
	**	
4	STATUS	WRITE
5	DATA	WRITE
•	DATA	WRITE
•	DATA	WRITE
36	DATA	WRITE

*reads command control code bits CB2-CB0
** response time
X = don't care

Remote Terminal Transaction (RT/$\overline{BC}$ input of the COM1553B set high)

The following section addresses each COM1553B information transfer format from the Remote Terminal viewpoint.

Bus Controller to Remote Terminal Transfer
(BC to RT, where RT receives data)

In this transfer the COM1553B designated as the RT receives a command to receive data. As the Command Word is completely shifted into the receive shift register, the RT compares the Command Word address field with the preloaded Remote Terminal address. This determines if the message is addressed to the receiving RT. If the Command Word is valid, the RT issues a Data Transfer Request ($\overline{DTR}$) to initiate a memory cycle. Once the processor relinquishes control of the data bus, during the Bus Acknowledge ($\overline{BGACK}$) time, the Command Word is placed on the data bus.

The Subaddress field is thereafter decoded by external logic and the Command word is written into external memory. The RT then receives a predetermined number of Data Words (specified by the word count field). As each Data Word is received it is written into external memory. After the reception of the last Data Word the RT transmits the Status Word, the Message Error, Broadcast Flag, Terminal Flag, Subsystem Flag, Busy, and Service Request bits are updated for all commands except for the Transmit Status Word and Transmit Last Command Code commands. While transmitting the Status, the RT writes it into memory. The RT also writes the Last Command Register, Error Register and Receive Register into memory and then asserts Message complete.

Note that the receive register of the RT will contain the transmitted Status Word.

TABLE 11
BC TO RT (RT receives a data from BC)

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND	WRITE
2	DATA	WRITE
3	DATA	WRITE
•	•	WRITE
•	•	WRITE
32	DATA	WRITE
	**	
33	STATUS	WRITE
34	LAST COMMAND	WRITE
35	ERROR REGISTER	WRITE
36	RECEIVE REGISTER	WRITE

Remote Terminal-to-Bus Controller Transfer (RT transmits data to BC)

The Remote Terminal receives a Transmit Command Word from the Bus Controller. The RT will then proceed to decode the Command Word, as in the previous case and within the response time transmits the Status Word.

While the Status Word is being transmitted the RT issues a write memory cycle to write the Status Word into external memory. Thereafter, the Data words are read from memory and transmitted. After the last word is transmitted the RT writes the contents of the Last Command Register, Error Register and the Receive Register into memory.

TABLE 12
Remote Terminal to Bus Controller (RT Transmits Data to BC)

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND	WRITE
	**	
2	STATUS	WRITE
3	DATA	READ
•	DATA	READ
•	DATA	READ
32	DATA	READ
33	LAST COMMAND	WRITE
34	ERROR REGISTER	WRITE
35	RECEIVE REGISTER	WRITE

** response time

Remote Terminal-to-Remote Terminal Transfers

From the Remote Terminal viewpoint, RT-to-RT transfers are similar to the RT to BC receive or transmit data transfers. The only exception is that the receiving terminal waits for the first Data Word from the transmitting terminal. This satisfies the protocol requirement that the transmitting terminal first send its status to the controller before it transmits the data to the receiving terminal.

Mode Command with Data (RT receives a Mode Code Command to transmit)

In this transfer, after the Transmit Mode Command is received, the RT transmits the Status and one Data Word.

TABLE 13

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND	WRITE
	**	
2	STATUS	WRITE
3	DATA	READ*
4	LAST COMMAND	WRITE
5	ERROR REGISTER	WRITE
6	RECEIVE REGISTER	WRITE

*For a Transmit Last command Mode Code, Data is not read from memory but transmitted from the internal Last Command register.

** response time

Mode Code Command with Data (RT receives a Mode Command to receive)

This transfer is similar to a Receive Command having only one Data Word.

TABLE 14

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND	WRITE
2	DATA	WRITE
	**	
3	STATUS	WRITE
4	LAST COMMAND	WRITE
5	ERROR REGISTER	WRITE
6	RECEIVE REGISTER	WRITE

** response time

Bus Controller Broadcast Transfer to RT

The RT receives a Broadcast Command to receive data. If data received during a broadcast message is invalid, the COM1553B will set the message error bit.

TABLE 15
RT RECEIVE

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND	WRITE
2	DATA	WRITE
•	DATA	WRITE
•	DATA	WRITE
32	DATA	WRITE
33	STATUS	WRITE*
34	LAST COMMAND	WRITE
35	ERROR REGISTER	WRITE

*In all broadcast transfers, a memory cycle is shown for the Status Word but the RT does not transmit it on the 1553B bus.

Broadcast Mode Code Command with Data

This Broadcast Mode Code command is detected if the MSB of the word count field is a logical high.

Transmission of the Status Word is suppressed as in the previous case but is loaded into external memory.

TABLE 16
RT RECEIVE

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND	WRITE
2	DATA	WRITE
3	STATUS	WRITE*
4	LAST COMMAND	WRITE
5	ERROR REGISTER	WRITE

*In all broadcast transfers, a memory cycle is shown for the Status Word but the RT does not transmit it on the 1553B bus.

Broadcast Mode Code Command Without Data

This Mode Code command is detected if the MSB of the word count field is zero. This transaction is the same as the previous transfer except that there is no Data Word transfer.

TABLE 17

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND	WRITE
2	STATUS	WRITE*
3	LAST COMMAND	WRITE
4	ERROR REGISTER	WRITE

*In all broadcast transfers, a memory cycle is shown for the Status Word but the RT does not transmit it on the 1553B bus.

Broadcast RT to RT Transfer

For this message transfer a Broadcast Command to receive is issued by the Bus Controller. This is followed by a normal Transmit Command to the transmitting Remote Terminal. The Remote Terminal responds with a normal transmit message format of Status Word and Data Word(s). The receiving terminals do not transmit a Status Word after receiving the data. However, they do go through a memory cycle to load the Status Word into their respective memories.

For the Remote Terminal receive transfer refer to Table 15. The only difference in this transfer is that there is a gap time between the Command and Data word.

For the Remote Terminal transmit transfer refer to Table 12. The only difference in this transfer is that the Receive Register is not written into memory.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... −55 to +125°C
Storage Temperature Range ..... −55 to +150°C
Lead Temperature (soldering, 10 seconds) ..... +325°C
Positive Voltage on any pin ..... +15V
Negative Voltage on any pin except VBB, with respect to ground ..... −.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS $T_A = -55$ to 125°C, $V_{CC} = 5.0V \pm 5\%$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
V_{IL}	Input Low Voltage	−0.3		0.8	V	
V_{IH}	Input High Voltage	3		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = -3.2$ mA
V_{OH}	Output High Voltage	2.4	4	5	V	$I_{OH} = .8$ mA
I_L	Input Leakage Current			10	µA	
C_{IN}	Input Capacitance		10	25	pf	
C_o	Output Capacitance		10	15	pf	
C_L	Load Capacitance		100	150	pf	
P_W	Power Dissipation		0.8		W	$T_A = 25$°C

AC ELECTRICAL CHARACTERISTICS

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
clk	clock frequency		12		MHz	50% duty cycle
t_r	Clk, rise time		6		ns	
t_f	Clk, fall time		6		ns	
t_1	$\overline{DTR}$ and $\overline{WE}$	0.5	0.6	1	µs	
t_2	$\overline{BGACK}$ to $\overline{DTR}$	0.8	1.3	2	µs	
t_3	$\overline{WE}$ to DATA		100		ns	
t_4	$\overline{DTACK}$ to $\overline{WE}$		1.5	2	µs	
t_5	$\overline{DTACK}$ to R/$\overline{W}$		1	1.5	µs	
t_6	$\overline{DTACK}$ to C/$\overline{D}$		1.5	2.5	µs	
t_7	$\overline{CSTR}$ to $\overline{CSTRA}$			673	µs	µs
t_8	$\overline{CSTRA}$ to $\overline{CSTR}$			1.5	ns	
t_9	$\overline{CSTRA}$ width		500		ns	
t_{10}	C/$\overline{D}$ to DATA	0				

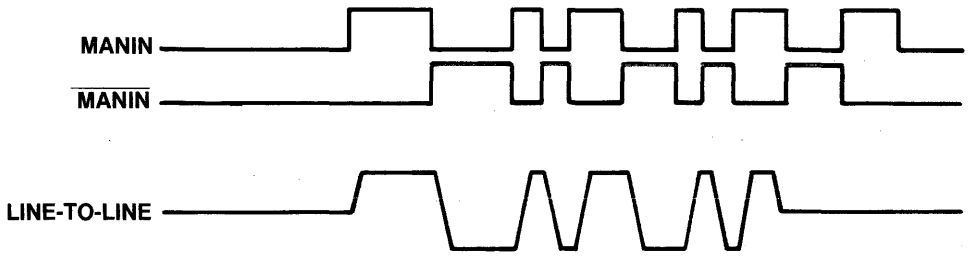


FIGURE 3:
RECEIVER LOGIC WAVEFORMS

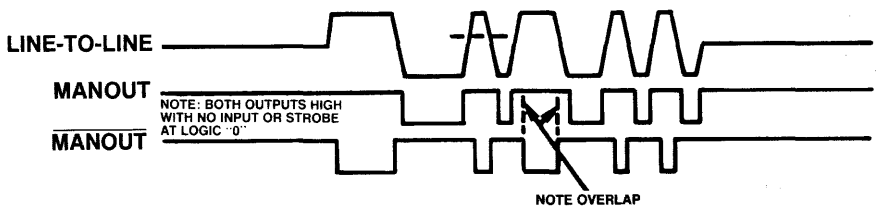


FIGURE 4:
DRIVER LOGIC WAVEFORMS

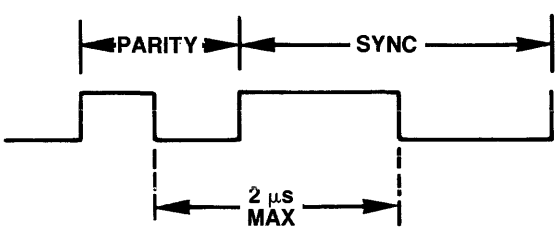
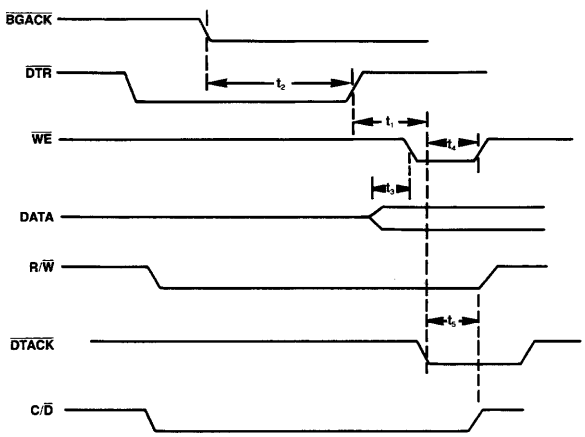
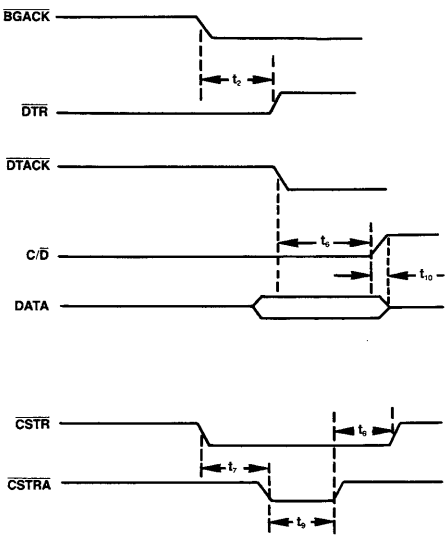


FIGURE 5:
CONTIGUOUS WORD

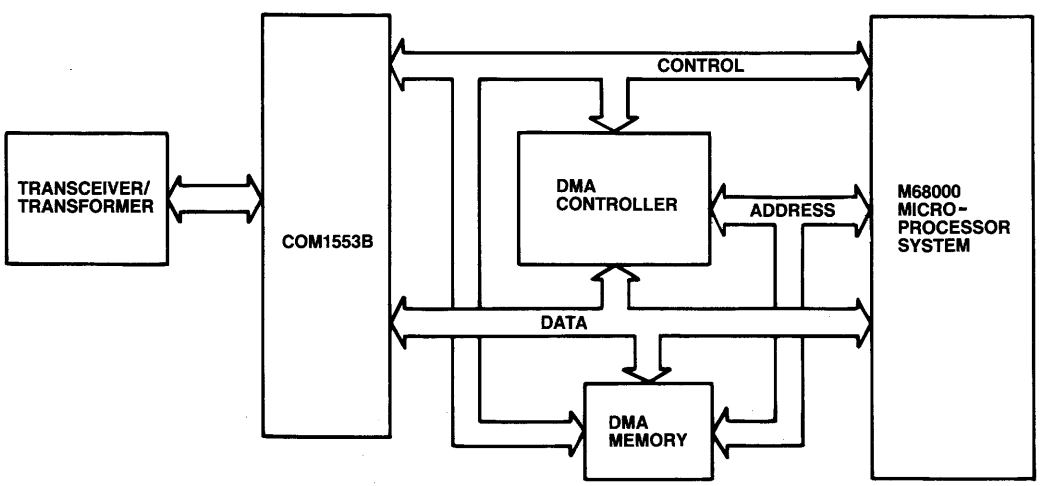
AC CHARACTERISTICS



WRITE CYCLE



READ CYCLE



TYPICAL SYSTEM IMPLEMENTATION

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • TWX-510-227-8898

STANDARD MICROSYSTEMS CORPORATION

COM1671
μPC FAMILY

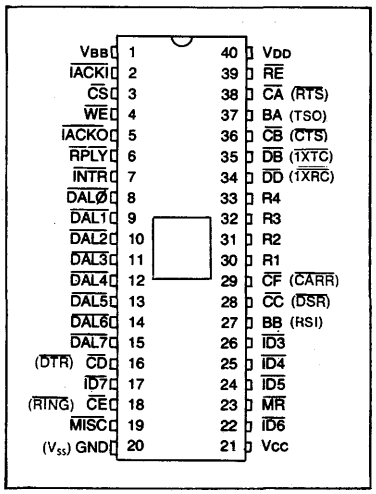
Asynchronous/Synchronous Transmitter-Receiver

ASTRO

FEATURES

- ☐ SYNCHRONOUS AND ASYNCHRONOUS
  - Full Duplex Operations
- ☐ SYNCHRONOUS MODE
  - Selectable 5-8 Bit Characters
  - Two Successive SYN Characters Sets Synchronization
  - Programmable SYN and DLE Character Stripping
  - Programmable SYN and DLE-SYN Fill
- ☐ ASYNCHRONOUS MODE
  - Selectable 5-8 Bit Characters
  - Line Break Detection and Generation
  - 1-, 1½-, or 2-Stop Bit Selection
  - Start Bit Verification
  - Automatic Serial Echo Mode
- ☐ BAUD RATE—DC TO 1M BAUD
- ☐ 8 SELECTABLE CLOCK RATES
  - Accepts 1X Clock and Up To 4 Different 32X Baud Rate Clock Inputs
  - Up to 47% Distortion Allowance With 32X Clock
- ☐ SYSTEM COMPATIBILITY
  - Double Buffering of Data
  - 8-Bit Bi-Directional Bus For Data, Status, and Control Words
  - All Inputs and Outputs TTL Compatible
  - Up To 32 ASTROS Can Be Addressed On Bus
  - On-Line Diagnostic Capability
- ☐ ERROR DETECTION
  - Parity, Overrun and Framing

PIN CONFIGURATION



- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ Pin for Pin replacement for Western Digital UC1671 and National INS 1671
- ☐ Baud Rate Clocks Generated by COM5036 @ 1X and COM5016-6 @ 32X

APPLICATIONS

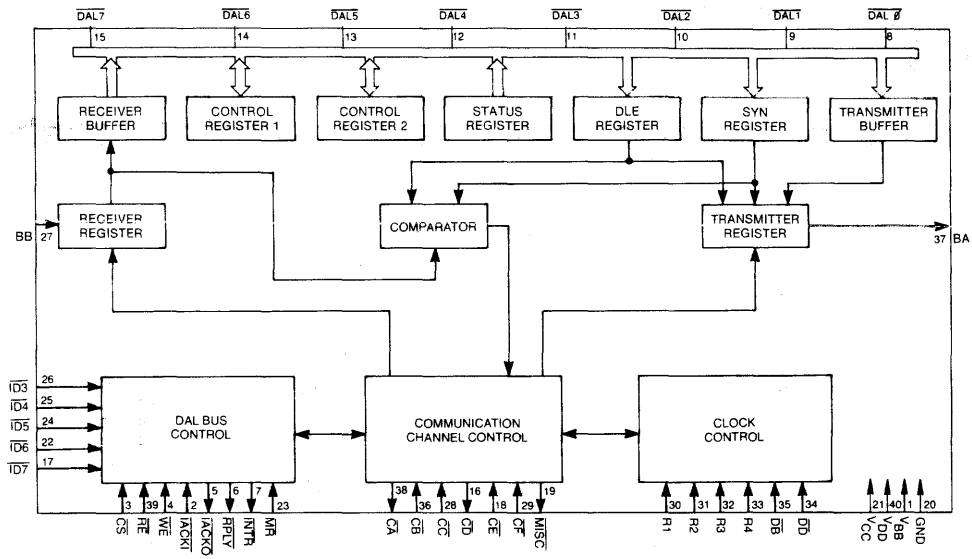
Synchronous Communications
Asynchronous Communications
Serial/Parallel Communications

General Description

The COM1671 (ASTRO) is a MOS/LSI device which performs the functions of interfacing a serial data communication channel to a parallel digital system. The device is capable of full duplex communications (receiving and transmitting) with synchronous or asynchronous systems. The ASTRO is designed to operate on a multiplexed bus with other bus-oriented devices. Its operation is programmed by a processor or controller via the bus and all parallel data transfers with these machines are accomplished over the bus lines.

The ASTRO contains several "handshaking" signals to insure easy interfacing with modems or other peripheral devices such as display terminals. In addition, a programmable diagnostic mode allows the selection of an internal looping feature which allows the device to be internally connected for processor testing.

The COM1671 provides the system communication designer with a software responsive device capable of handling complex communication formats in a variety of system applications.



Organization

Data Access Lines — The DAL bus is an 8-bit bi-directional port over which all address, data, control, and status transfers occur. In addition to transferring data and control words the DAL bus also transfers information related to addressing of the device, reading and writing requests, and interrupting information.

Receiver Buffer — This 8-bit parallel register presents assembled received characters to the DAL bus when requested through a Read operation.

Receiver Register — This 8-bit shift register inputs the received data at a clock rate determined by Control Register 2. The incoming data is assembled to the selected character length and then transferred to the Receiver Buffer with logic zeroes filling out any unused high-order bit positions.

Syn Register — This 8-bit register is loaded from the DAL bus by a Write operation and holds the synchronization code used for receiver character synchronization. It serves as a fill character when no new data is available in the Transmitter Buffer during transmission. This register cannot be read onto the DAL bus. It must be loaded with logic zeroes in all unused high-order bits.

Comparator — The 8-bit comparator is used in the Synchronous mode to compare the assembled contents of the Receiver Register and the SYN register or the DLE register. A match between the registers sets up stripping of the received character, when programmed, by preventing the data from being loaded into the Receiver Buffer. A bit in the Status Register is set when stripping is effected. The comparator output also enables character synchronization of the Receiver on two successive matches with the SYN register.

DLE Register — This 8-bit register is loaded from the DAL bus by a Write operation and holds the DLE character used in the Transparent mode of operation in which an idle transmit period is filled with the combination DLE-SYN pair of characters rather than a single SYN character. In addition the ASTRO may be programmed to force a single DLE character prior to any data character transmission while in the transmitter transparent mode.

Status Register — This 8-bit register holds information on communication errors, interface data register status, match character conditions, and communication equipment status. This register may be read onto the DAL bus by a Read operation.

Control Registers — There are two 8-bit Control Registers which hold device programming signals such as mode selection, clock selection, interface signal control, and data format. Each of the Control Registers can be loaded from the DAL bus by a Write operation or read onto the DAL bus by a Read operation. The registers are cleared by a Master Reset.

Transmitter Buffer — This 8-bit parallel register holds data transferred from the DAL bus by a Write operation. This data is transferred to the Transmitter Register when the transmitter section is enabled and the Transmitter Register is ready to send new data.

Transmitter Register — This 8-bit shift register is loaded from the Transmitter Buffer, SYN register, or DLE register. The purpose of this register is to serialize data and present it to the serial data output.

Astro Operation

Asynchronous Mode

Framing of asynchronous characters is provided by a Start bit (logic 0) at the beginning of a character and a Stop bit(s) (logic 1) at the end of a character. Reception of a character is initiated on recognition of the first Start bit by a positive transition of the receiver clock, after a preceding Stop bit(s). The Start and Stop bits are stripped off while assembling the serial input into a parallel character.

The character assembly is completed by the reception of the Stop bit(s) after reception of the last character bit (including the parity bit, if selected). If the Stop bit(s) is a logic 1, the character is determined to have correct framing and the ASTRO is prepared to receive the next character. If the Stop bit(s) is a logic 0, the Framing Error Status flag is set and the Receiver assumes this bit to be the Start bit of the next character. Character assembly continues from this point if the input is still a logic 0 when sampled at the theoretical center of the assumed Start bit. As long as the Receiver input is spacing, all zero characters are assembled and error flags and data received interrupts are generated so that line breaks can be determined. After a character of all zeroes is assembled along with a zero in the Stop bit(s) location, the first sampled logic one is determined as a Stop bit and this resets the Receiver circuit to a Ready state for assembly of the next character.

In the Asynchronous mode the character transmission occurs when information contained in the Transmitter Buffer is transferred to the Transmitter Register. Transmission is initiated by the insertion of a Start bit, followed by the serial output of the character (including the parity bit, if selected), then the insertion of a 1, 1.5, or 2 bit length Stop condition. If the Transmitter Buffer is full, the next character transmission starts after the transmission of the Stop bit(s) of the present character in the Transmitter Register. Otherwise, the Mark (logic 1) condition is continually transmitted until the Transmitter Buffer is loaded.

Synchronous Mode

Framing of characters is carried out by a special Synchronization Character Code (SYN) transmitted at the beginning of a block of characters. The Receiver, when enabled, searches for two contiguous characters matching the bit pattern contained in the SYN register. During the time the Receiver is searching, data is not transferred to the Receiver Buffer, status bits are not updated, and the Receiver interrupt is not activated. After the detection of the first SYN character, the Receiver assembles subsequent bits into characters whose length is determined by the contents of Control Register 2. If, after the first SYN character detection, a second SYN character is present, the Receiver enters the Synchronization mode until the Receiver Enable Bit is turned off. If a second successive SYN character is not found, the Receiver reverts back to the Search mode.

In the Synchronous mode a continuous stream of characters are transmitted once the Transmitter is enabled. If the Transmitter Buffer is not loaded at the time the Transmitter Register has completed transmission of a character, this idle time will be filled by a transmission of the character contained in the SYN register in the Non-transparent mode, or the characters contained in the DLE and SYN registers respectively while in the Transparent mode of operation.

Astro Operation

Receiver

The Receiver Data input is clocked into the Receiver Register by a 1X Receiver Clock from a modem Data Set, or by a local 32X bit rate clock selected from one of four externally supplied clock inputs. When using the 1X clock, the Receiver Data is sampled on the positive transition of the clock in both the Asynchronous and Synchronous modes. When using a 32X clock in the Asynchronous mode, the Receiver Sampling Clock is phased to the Mark-To-Space transition of the Received Data Start bit and defines, through clock counts, the center of each received Data bit with +0%, −3% at the positive transition 16 clock periods later.

In the Synchronous mode the Sampling Clock is phased to all Mark-To-Space transitions of the Received Data inputs when using a 32X clock. Each transition of the data causes an incremental correction of the Sampling Check by 1/32nd of a bit period. The Sampling clock can be immediately phased to every Mark-To-Space Data transition by setting Bit 4 of Control Register 1 to a logic one, while the Receiver is disabled.

When the complete character has been shifted into the Receiver Register it is transferred to the Receiver Buffer; the unused, higher order bits are filled with logic zero's. At this time the Receiver Status bits (Framing Error/Sync Detect, Parity Error/DLE Detect, Overrun Error, and Data Received) are updated in the Status Register and the Data Received interrupt is activated. Parity Error is set, if encountered while the Receiver parity check is enabled in the Control Registers. Overrun Error is set if the Data Received status bit is not cleared through a Read operation by an external device when a new character is transferred to the Receiver Buffer. This error flag indicates that a character has been lost; new data is lost while the old data and its status flags are saved.

The characters assembled in the Receiver Register that match the content of the SYN or the DLE register are not loaded into the Receiver Buffer, and the DR interrupt is not generated, if Bit 3 of Control Register 2 (CR23) or Bit 4 of Control Register 1 (CR14) are set respectively, and SYN Detect and DLE Detect are set with the next non SYN or non DLE character. When both CR23 and CR14 are set (Transparent mode), the DLE-SYN combination is stripped. The SYN comparison occurs only with the character received after the DLE character. If two successive DLE characters are received only the first DLE character is stripped. No parity check is made while in this mode.

Transmitter

Information is transferred to the Transmitter Buffer by a Write operation. Information can be loaded into this register at any time, even when the Transmitter is not enabled. Transmission of data occurs only when the Request to Send bit is set to a logic 1 in Control Register 1 and the Clear To Send input is logic 0. Information is normally transferred from the Transmitter Buffer to the Transmitter Register when the latter has completed transmission of a character. However, information in the DLE register may be transferred prior to the information contained in the Transmitter Buffer if the Force DLE signal condition is enabled (Bits 5 and 6 of Control Register 1 set to a logic 1). The control bit CR15 must be set prior to loading of a new character in the Transmitter Buffer to insure forcing the DLE character prior to transmission of the data character. The Transmitter Register output passes through a flip-flop which delays the output by one clock period. When using the 1X clock generated by the Modem Data Set, the output data changes state on the negative clock transition and the delay is one bit period. When using a local 32X clock the the transmitter section selects one of the four selected rate inputs and divides the clock down to the baud rate. This clock is phased to the Transmitter Buffer Empty Flag such that transmission of characters occurs within two clock times of the loading of the Transmitter Buffer, when the Transmitter Register is empty.

When the Transmitter is enabled, a Transmitter interrupt is generated each time the Transmitter Buffer is empty. If the Transmitter Buffer is empty, when the Transmitter Register is ready for a new character, the Transmitter enters an idle state. During this idle time a logic 1 will be presented to the Transmitted Data output in the Asynchronous mode or the contents of the SYN register will be presented in the Synchronous Non-transparent mode (CR16 = 0). in the Synchronous Transmit Transparent mode (CR16 = 1), the idle state will be filled by DLE-SYN character transmission in that order. When entering the Transparent mode DLE must precede the contents of the Transmitter Buffer. This is accomplished by setting of Bit 5 of Control Register 1.

If the transmitter section is disabled by a reset of the Request to Send, any partially transmitted character is completed before the transmitter section of the ASTRO is disabled. As soon as the Clear To Send goes high the transmitted data output will go high.

When the Transmitter parity is enabled, the selected Odd or Even parity bit is inserted into the last data bit of the character in place of the last bit of the Transmitter Register. This limits transfer of character information to a maximum of seven bits plus parity or eight bits without parity. Parity cannot be enabled in the Synchronous Transparency mode.

Input/Output Operations

All Data, Control, and Status words are transferred over the Data Access Lines (DAL 0-7). Additional input lines provide controls for addressing a particular ASTRO, and regulating all input and output operations. Other lines provide interrupt capability to indicate to a Controller that an input operation is requested by the ASTRO. All input/output terminology below is referenced to the Controller so that a Read or input takes data from the ASTRO and places it on the DAL bus, while a Write or Output places data from the DAL bus into the ASTRO.

A Read or Write operation is initiated by the placement of an eight-bit address on the DAL bus by the Controller. When the Chip Select signal goes to a logic 0 state, the ASTRO compares Bits 7-3 of the DAL bus with its hard-wired ID code (Pins 17, 22, 24, 25, and 26) and becomes selected on a Match condition. The ASTRO then sets its $\overline{\text{RPLY}}$ line low to acknowledge its readiness to transfer data. Bit 0 must be a logic O in Read or Write operation. A setup time must exist between $\overline{\text{CS}}$ and the $\overline{\text{RE}}$ or $\overline{\text{WE}}$ signals to allow chip selection prior to read/write operations.

Read

Bits 2-0 of the address are used to select ASTRO registers to read from as follows:

Bits 2-0	Selected Register
000	Control Register 1
010	Control Register 2
100	Status Register
110	Receiver Buffer

When the Read Enable ($\overline{\text{RE}}$) line is set to a logic 0 condition by the Controller the ASTRO gates the contents of the addressed register onto the DAL bus. The Read operation terminates, and the device becomes unselected, when both the Chip Select and Read Enable return to a logic 1 condition. Reading of the Receiver Buffer clears the Data Received Status bit. The data is removed from the DAL bus when the $\overline{\text{RE}}$ signal returns to the logic high state.

Write

Bits 2-0 of the address are used to select ASTRO registers to be written into as follows:

Bits 2-0	Selected Register
000	Control Register 1
010	Control Register 2
100	SYN and DLE Register
110	Transmitter Buffer

When the Write Enable ($\overline{\text{WE}}$) line is set to a logic 0 condition by the Controller the ASTRO gates the data from the DAL bus into the addressed register. If data is written into the Transmitter Buffer, the TBMT Status bit is cleared to a logic zero.

The 100 address loads both the SYN and DLE registers. After writing into the SYN register the device is conditioned to write into the DLE if followed by another Write pulse with the 100 address. Any intervening Read or Write operation with other addresses or other ASTROs resets this condition such that the next 100 will address the SYN register.

Interrupts

The following conditions generate interrupts:

Data Received (DR)
Indicates transfer of a new character to the Receiver Buffer while the Receiver is enabled.

Transmitter Buffer Empty (TBMT)
Indicates that the Transmitter Buffer is empty while the Transmitter is enabled. The first interrupt occurs when the Transmitter becomes enabled if there is an empty Transmitter Buffer, or after the character is transferred to the Transmitter Register making the Transmitter Buffer empty.

Carrier On
Indicates Carrier Detector input goes low and the Data Terminal Ready (DTR) bit (CR10) is high.

Carrier Off
Indicates Carrier Detector input goes high and the Data Terminal Ready (DTR) bit (CR10) is high.

Data Set Ready On
Indicates the Data Set Ready input goes low and the Data Terminal Ready (DTR) bit (CR10) is high.

Data Set Ready Off
Indicates the Data Set Ready input goes high and the Data Terminal Ready (DTR) bit (CR10) is high.

Ring On
Indicates the Ring Indicator input goes low and the Data Terminal Ready (DTR) bit (CR10) is low.

Each time an interrupt condition exists the $\overline{\text{INTR}}$ output from the ASTRO is made a logic low. The following interrupt procedure is then carried out even if the interrupt condition is removed.

The Controller acknowledges the Interrupt request by setting the Chip Select ($\overline{\text{CS}}$) and the Interrupt Acknowledge Input (IACKI) to the ASTRO to a low state. On this transition all non-interrupting devices receiving the IACKI signal set their Interrupt Acknowledge Output (IACKO) low, enabling lower priority daisy-chained devices to respond to the interrupt request. The highest priority device that is interrupting will then set its $\overline{\text{RPLY}}$ line low. This device will place its ID code on Bit Positions 7-3 of the DAL bus when a low $\overline{\text{RE}}$ signal is received. The data is removed from the DAL bus when the Read Enable ($\overline{\text{RE}}$) signal returns to the logic one state. To reset the Interrupt condition ($\overline{\text{INTR}}$) Chip Select ($\overline{\text{CS}}$) and IACKI must be received by the ASTRO.

Description of Pin Functions

Pin No.	Symbol	Pin Name	I/O	Function
1	V_{BB}	POWER SUPPLY	PS	− 5 Volts
21	V_{CC}	POWER SUPPLY	PS	+ 5 Volts
40	V_{DD}	POWER SUPPLY	PS	+ 12 Volts
20	V_{SS}	GROUND	GND	Ground
23	$\overline{MR}$	$\overline{MASTER\ RESET}$	I	The Control and Status Registers and other controls are cleared when this input is low.
8-15	$\overline{DAL0}$-$\overline{DAL7}$	$\overline{DATA\ ACCESS\ LINES}$	I/O	Eight-bit bi-directional bus used for transfer of data, control status, and address information.
17	$\overline{ID7}$	$\overline{SELECT\ CODE}$	I	Five input pins which when hard-wired assign the device a unique identification code used to select the device when addressing and used as an identification when responding to interrupts.
22	$\overline{ID6}$		I	
24	$\overline{ID5}$		I	
25	$\overline{ID4}$		I	
26	$\overline{ID3}$		I	
3	$\overline{CS}$	$\overline{CHIP\ SELECT}$	I	The low logic transition of $\overline{CS}$ identifies a valid address on the DAL bus during Read and Write operations.
39	$\overline{RE}$	$\overline{READ\ ENABLE}$	I	This input, when low, gates the contents of the addressed register from a selected ASTRO onto the DAL bus.
4	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	I	This input, when low, gates the contents of the DAL bus into the addressed register of a selected ASTRO.
7	$\overline{INTR}$	$\overline{INTERRUPT}$	O	This open drain output, to facilitate WIRE-ORing, goes low when any interrupt conditions occur.
2	$\overline{IACKI}$	$\overline{INTERRUPT\ ACKNOWLEDGE\ IN}$	I	When the Controller (determining the interrupting ASTRO) makes this input low, the ASTRO places its ID code on the DAL bus and sets reply low if it is interrupting, otherwise it makes $\overline{IACKO}$ a low.
5	$\overline{IACKO}$	$\overline{INTERRUPT\ ACKNOWLEDGE\ OUT}$	O	This output goes low in response to a low $\overline{IACKI}$ if the ASTRO is not the interrupting device.
6	$\overline{RPLY}$	$\overline{REPLY}$	O	This open drain output, to facilitate WIRE-ORing, goes low when the ASTRO is responding to being selected by an address on the DAL bus or in affirming that it is the interrupting source.

Description of Pin Functions

Pin No.	Symbol	Pin Name	I/O	Function
30 31 32 33	R1 R2 R3 R4	CLOCK RATES	I I I I	These four inputs accept four different local 32X data rate Transmit and Receive clocks. The input on R4 may be divided down into a 32X clock from a 32X, 64X, 128X, or 256X clock input. The clock used in the ASTRO is selected by bits 0-2 of Control Register 2.
37	BA	TRANSMITTED DATA	O	This output is the transmitted serial data from the ASTRO. This output is held in a Marking condition when the transmitter section is not enabled.
27	BB	RECEIVED DATA	I	This input receives serial data into the ASTRO.
38	$\overline{CA}$	$\overline{\text{REQUEST TO SEND}}$	O	This output is enabled by bit 1 of Control Register 1 and remains in a low state during transmitted data from the ASTRO.
36	$\overline{CB}$	$\overline{\text{CLEAR TO SEND}}$	I	This input, when low, enables the transmitter section of the ASTRO.
28	$\overline{CC}$	$\overline{\text{DATA SET READY}}$	I	This input generates an interrupt when going ON or OFF while the Data Terminal Ready signal is ON. It appears as bit 6 in the Status Register.
16	$\overline{CD}$	$\overline{\text{DATA TERMINAL READY}}$	O	This output is generated by bit 0 in Control Register 1 and indicates Controller readiness.
18	$\overline{CE}$	$\overline{\text{RING INDICATOR}}$	I	This input from the Data Set generates an interrupt when made low with Data Terminal Ready in the OFF condition.
29	$\overline{CF}$	$\overline{\text{CARRIER DETECTOR}}$	I	This input from the Data Set generates an interrupt when going ON or OFF if Data Terminal Ready is ON. It appears as bit 5 in the Status Register.
35	$\overline{DB}$	$\overline{\text{TRANSMITTER TIMING}}$	I	This input is the Transmitter 1X Data Rate Clock. Its use is selected by bits 0-2 of Control Register 2. The transmitted data changes on the negative transition of this signal.
34	$\overline{DD}$	$\overline{\text{RECEIVER TIMING}}$	I	This input is the Receiver 1X Data Rate Clock. Its use is selected by bits 0-2 of Control Register 2. The Received Data is sampled by the ASTRO on the positive transition of this signal.
19	$\overline{MISC}$	$\overline{\text{MISCELLANEOUS}}$	O	This output is controlled by bits 4 and 5 of Control Register 1 and is used as an extra programmable signal.

Device Programming

The two 8-bit Control Registers of the ASTRO determine the operative conditions of the ASTRO chip.

Control Register 1

BIT 7	6	5	4	3	2	1	0
SYNC/ASYNC 0 – LOOP MODE 1 – NORMAL MODE	ASYNC 0 – NONBREAK MODE 1 – BREAK MODE TX SYNC 0 – TRANSMITTER NON TRANSPARENT MODE 1 – TRANSMITTER TRANSPARENT MODE	ASYNC (TRANS. ENABLED) 0 – 1½ or 2 STOP BIT SELECTION 1 – SINGLE STOP BIT SELECTION ASYNC (TRANS. DISABLED) 0 – $\overline{\text{MISC}}$ OUT = 1 1 – $\overline{\text{MISC}}$ OUT = 0 SYNC (CR16 = 0) 0 – NO PARITY GENERATED 1 – TRANSMIT PARITY ENABLED SYNC (CR16 = 1) 0 – NO FORCE DLE 1 – FORCE DLE	ASYNC 0 – NON ECHO MODE 1 – AUTO ECHO MODE SYNC (CR12 = 1) 0 – DLE STRIPPING NOT ENABLED 1 – DLE STRIPPING ENABLED SYNC (CR12 = 0) 0 – $\overline{\text{MISC}}$ OUT = 1 1 – $\overline{\text{MISC}}$ OUT = 0	ASYNC 0 – NO PARITY ENABLED 1 – PARITY CHECK ENABLED ON RECEIVER AND PARITY GENERATION ENABLED ON TRANSMITTER SYNC 0 – RECEIVER PARITY CHECK IS DISABLED 1 – RECEIVER PARITY CHECK IS ENABLED	SYNC/ASYNC 0 – RECEIVER DISABLED 1 – RECEIVER ENABLED	SYNC/ASYNC 0 – SETS $\overline{\text{RTS}}$ OUT = 1 1 – SETS $\overline{\text{RTS}}$ OUT = 0	SYNC/ASYNC 0 – SETS $\overline{\text{DTR}}$ OUT = 1 1 – SETS $\overline{\text{DTR}}$ OUT = 0

Bit 0

Controls the $\overline{\text{Data Terminal Ready}}$ output on Pin 16 to control the CD circuit of the Data Set. A logic 1 enables the Carrier and Data Set Ready interrupts. A logic 0 enables only the telephone line Ring interrupt. The $\overline{\text{DTR}}$ output is inverted from the state of CR10.

Bit 1

Controls the $\overline{\text{Request to Send}}$ output on Pin 38 to control the CA circuit of the Data Set. The $\overline{\text{RTS}}$ output is inverted from the state of CR11. A logic 1 combined with a low logic $\overline{\text{Clear to Send}}$ input enables the Transmitter and allows TBMT interrupts to be generated. A logic 0 disables the Transmitter and turns off the external $\overline{\text{Request to Send}}$ signal. Any character in the Transmitter Register will be completely transmitted before the Transmitter is turned off. The $\overline{\text{Request to Send}}$ output may be used for other functions such as Make Busy on 103 Data Sets.

Bit 2

A logic 1 enables the ASTRO to receive data into the Receiver Buffer, update Receiver Status Bits 1, 2, 3, and 4, and to generate Data Received interrupts. A logic 0 disables the Receiver and clears the Receiver Status bits.

Bit 3

Asynchronous Mode

A logic 1 enables check of parity on received characters and generation of parity for transmitted characters.

Synchronous Mode

A logic 1 bit enables check of parity on received characters only. Note: Transmitter parity enable is controlled by CR15.

Bit 4

Asynchronous Mode

A logic 1 enables the Automatic Echo mode when the receiver section is enabled. In this mode the clocked regenerated data is presented to the Transmitter Data output in place of normal transmission through the Transmitter Register. This serial method of echoing does not present any abnormal restrictions on the transmit speed of the terminal. Only the first character of a Break condition of all zeroes (null character) is echoed when a Line Break condition is detected. For all subsequent null characters, with logic zero Stop bits, a steady Marking condition is transmitted until normal character reception resumes. Echoing does not start until a character has been received and the Transmitter is idle. The Transmitter does not have to be enabled during the Echo mode.

Synchronous Mode

A logic 1, with the Receiver enabled does not allow assembled Receiver data matching the DLE register contents to be transferred to the Receiver Buffer; also, parity checking is disabled.

When the Receiver is not enabled this bit controls the Miscellaneous output on Pin 19, which may be used for New Sync on a 201 Data Set. When operating with a 32X clock and a disabled Receiver, a logic 1 on this bit also causes the Receiver timing to synchronize on Mark-To-Space transitions.

Bit 5

Asynchronous Mode

A logic 1, with the Transmitter enabled, causes a single Stop bit to be transmitted. A logic 0 causes transmission of 2 stop bits for character lengths of 6, 7, or 8 bits and one-and-a-half Stop bits for a character length of 5 bits.

With the Transmitter disabled this bit controls the Miscellaneous output on Pin 19, which may be used for Make Busy on 103 Data Sets, Secondary Transmit on 202 Data Sets, or dialing on CBS Data Couplers.

Synchronous Mode

A logic 1 combined with a logic 0 on Bit 6 of Control Register 1 enables Transmit parity; if CR15=0 or CR16=1 no parity is generated. When set to a logic 1 with Bit 6 also a logic 1, the contents of the DLE register are transmitted prior to the next character loaded in the Transmitter Buffer as part of the Transmitter Transparent mode.

Bit 6

Asynchronous Mode

A logic 1 holds the Transmitted Data output in a Spacing (Logic 0) condition, starting at the end of any current transmitted character, when the Transmitter is enabled. Normal Transmitter timing continues so that this Break condition can be timed out after the loading of new characters into the Transmitter Buffer.

Synchronous Mode

A logic 1 conditions the Transmitter to a transparent transmission which implies that idle transmitter time will be filled by DLE-SYN character transmission and a DLE character can be forced ahead of any character in the Transmitter Buffer (Bit 5 above). When forcing DLE transmission, Bit 5 should be set to a logic 1 prior to loading the Transmitter Buffer, otherwise the character in the latter register may be transferred to the Transmitter Register prior to sending the DLE character.

Bit 7

A logic 0 configures the ASTRO into an Internal Data and Control Loop mode and disables the Ring interrupt. In this diagnostic mode the following loops are connected internally:

a. The Transmit Data is connected to the Receive Data with the BA pin held in a Mark condition and the input to the BB pin disregarded.

b. With a 1X clock selected, the Transmitter Clock also becomes the Receive Clock.

c. The Data Terminal Ready (DTR) Control bit is connected to the $\overline{\text{Data Set Ready (DSR)}}$ input, with the $\overline{\text{Data Terminal Ready (DSR)}}$ output pin held in an OFF condition (logic high), and the $\overline{\text{DSR}}$ input pin is disregarded.

d. The Request to Send Control bit is connected to the $\overline{\text{Clear To Send (CTS)}}$ and $\overline{\text{Carrier Detector (CF)}}$ inputs, with the $\overline{\text{Request To Send (RTS)}}$ output pin held in an OFF condition (logic high), and the $\overline{\text{CTS}}$ and $\overline{\text{Carrier Detector}}$ input pins are disregarded.

e. The $\overline{\text{Miscellaneous}}$ pin is held in an OFF (logic high) condition.

A logic 1 on Bit 7 enables the Ring interrupt and returns the ASTRO to the normal full duplex configuration.

Control Register 2

Control Register 2, unlike Control Register 1, cannot be changed at any time. This register should be changed only while both the receiver and transmitter sections of the ASTRO are in the idle state.

BIT 7 6	5	4	3	2 1 0
SYNC/ASYNC CHARACTER LENGTH SELECT 00 = 8 BITS 01 = 7 BITS 10 = 6 BITS 11 = 5 BITS	MODE SELECT 0 – ASYNCHRONOUS MODE 1 – SYNCHRONOUS MODE	SYNC/ASYNC 0 – EVEN PARITY SELECT 1 – ODD PARITY SELECT	ASYNC 0 – RECEIVER CLK = RATE 1 1 – RECEIVER CLOCK DETERMINED BY BITS 2-0 SYNC (CR16 = 0) 0 – NO SYN STRIP 1 – SYN STRIP SYNC (CR16 = 1) 0 – NO DLE-SYN STRIP 1 – DLE-SYN STRIP	SYNC/ASYNC CLOCK SELECT 000 – 1X CLOCK 001 – RATE 1 CLOCK 010 – RATE 2 CLOCK 011 – RATE 3 CLOCK 100 – RATE 4 CLOCK 101 – RATE 4 CLOCK ÷ 2 110 – RATE 4 CLOCK ÷ 4 111 – RATE 4 CLOCK ÷ 8

Bits 0-2
These bits select the Transmit and Receive clocks.

Bits	Clock Source	
2 1 0	Tx	Rx
0 0 0	1X Clock (Pin 35)	1X Clock (Pin 34)
0 0 1	Rate 1 32X clock (Pin 30)	
0 1 0	Rate 2 32X clock (Pin 31) *	
0 1 1	Rate 3 32X clock (Pin 32) *	
1 0 0	Rate 4 32X clock (Pin 33) *	
1 0 1	Rate 4 32X clock (Pin 33) (÷ 2) *†	
1 1 0	Rate 4 32X clock (Pin 33) (÷ 4) *†	
1 1 1	Rate 4 32X clock (Pin 33) (÷ 8) *†	

NOTES:
*Rx clock is modified by bit 3 in the asynchronous mode.
†Rate 4 is internally dividable so that the required 32X clock may be derived from an applied 64X, 128X, or 256X clock which may be available.

Bits 3

Asynchronous Mode

A logic 0 selects the Rate 1 32X clock input (Pin 30) as the Receiver clock rate and a logic 1 selects the same clock rate for the Receiver as selected by Bits 2-0 for the Transmitter. This bit must be a logic 1 for the 1X clock selection by Bits 2-0.

Synchronous Mode

A logic 1 causes all DLE-SYN combination characters in the Transparent mode when DLE strip (CR14) is a logic 1, or all SYN characters in the Non-transparent mode to be stripped out and no Data Received interrupt to be generated. The SYN Detect status bit is set with reception of the next assembled character as is transferred to the Receiver Buffer.

Bit 4
A logic 1 selects odd parity and a logic 0 selects even parity, when parity is enabled by CR13 and/or CR15.

Bit 5
A logic 1 selects the Synchronous Character mode. A logic 0 selects the Asynchronous Character mode.

Bits 6-7
These bits select the full character length (including parity, if selected) as shown above. When parity is enabled it must be considered as a bit when making character length selection (5 bits plus parity = 6 bits).

Status Register

The data contained in the Status Register define Receiver and Transmitter data conditions and status of the Data Set.

7	6	5	4	3	2	1	0
• Data Set Change	• Data Set Ready (DSR)	• Carrier Detector	• Framing Error • Syn Detect	• DLE Detect • Parity Error	• Overrun Error	• Data Received (DR)	• Transmitter Buffer Empty (TBMT)

Bit 0
A logic 1 indicates that the Transmitter Buffer may be loaded with new data. It is set to a logic 1 when the contents of the Transmitter Buffer is transferred to the Transmitter Register. It is cleared when the Transmitter Buffer is loaded from the DAL bus, or when the Transmitter is disabled.

Bit 1
A logic 1 indicates that an entire character has been received and transferred into the Receiver Buffer. It is cleared when the Receiver Buffer is read onto the DAL bus, or the Receiver is disabled.

Bit 2
A logic 1 indicates an Overrun error which occurs if the previous character in the Receiver Buffer has not been read and Data Received is not reset, at the time a new character is to be transferred to the Receiver Buffer. This bit is cleared when no Overrun condition is detected (the next character transfer time) or when the Receiver is disabled.

Bit 3
When the DLE Strip is enabled (CR14) the Receiver parity check is disabled and this bit is set to a logic 1 if the previous character to the presently assembled character matched the contents of the DLE register; otherwise it is cleared. The DLE DET remains for one character time and is reset on the next character transfer or on a Status Register Read. If DLE Strip is not enabled this bit is set to a logic 1 when the Receiver is enabled, Receiver parity (CR13) is also enabled, and the last received character has a Parity error. A logic 0 on this bit indicates correct parity. This bit is cleared in both modes when the Receiver is disabled.

Bit 4

Asynchronous Mode

A logic 1 indicates that the received data did not have a valid stop bit, while the Receiver was enabled, which indicates a Framing error. This bit is set to a logic 0 if the stop bit (logic 1) was detected.

Synchronous Mode

A logic 1 indicates that the contents of the Receiver Register matches the contents of the SYN Register. The condition of this bit remains for a full character assembly time. If SYN strip (CR23) is enabled this status bit is updated with the character received after the SYN character.

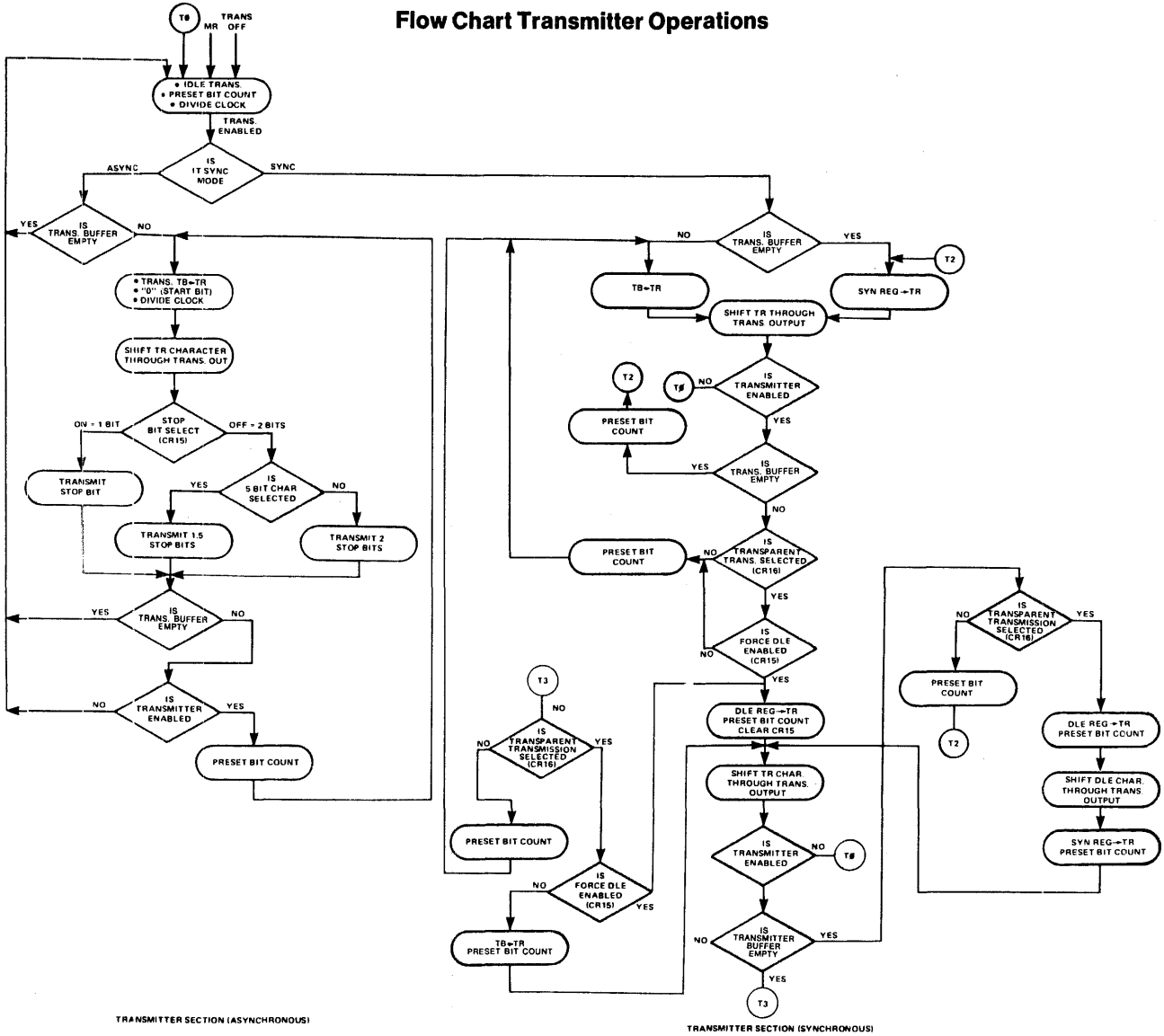
In both modes the bit is cleared when the Receiver is disabled.

Bit 5
This bit is the logic complement of the $\overline{\text{Carrier Detector}}$ input on Pin 29.

Bit 6
This bit is the logic complement of the $\overline{\text{Data Set Ready}}$ input on Pin 28. With 202-type Data Sets it can be used for Secondary Receive.

Bit 7
This bit is set to a logic 1 whenever there is a change in state of the $\overline{\text{Data Set Ready}}$ or $\overline{\text{Carrier Detector}}$ inputs while Data Terminal Ready (CR10) is a logic 1 or the $\overline{\text{Ring Indicator}}$ is turned ON, with DTR a logic 0. This bit is cleared when the Status Register is read onto the DAL bus.

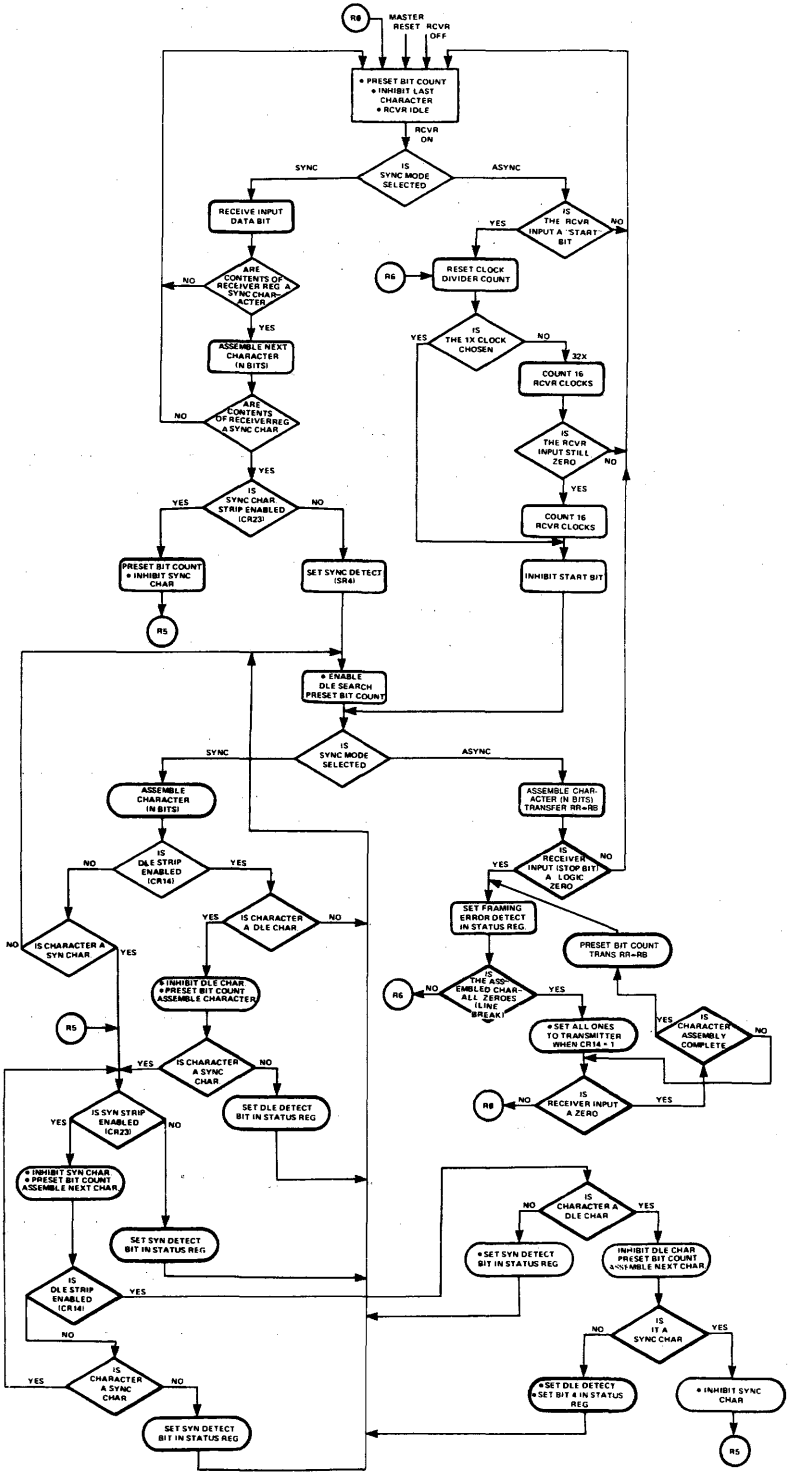
Flow Chart Transmitter Operations



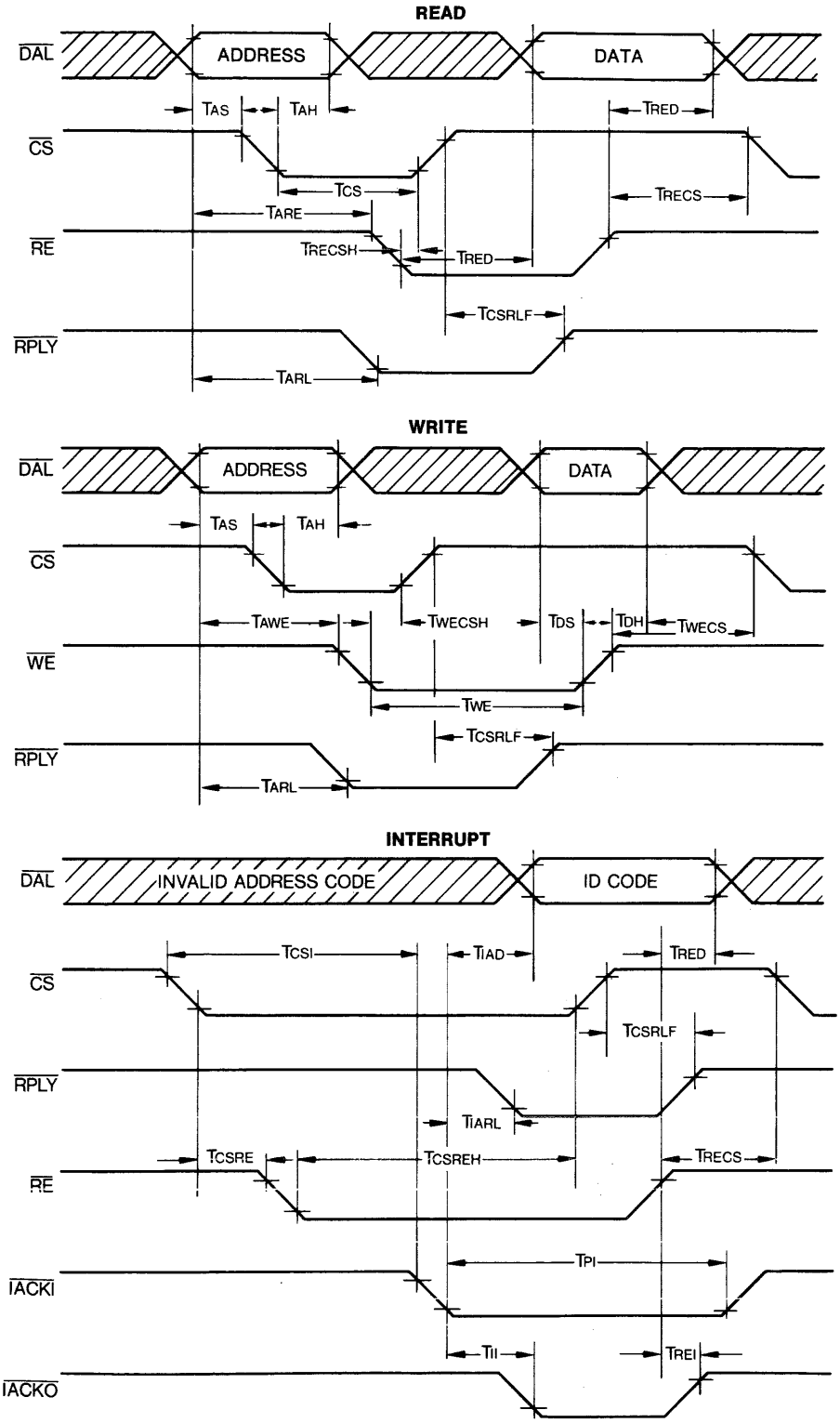
TRANSMITTER SECTION (ASYNCHRONOUS)

TRANSMITTER SECTION (SYNCHRONOUS)

Flow Chart Receiver Operations



RECEIVER SECTION


READ
DAL
ADDRESS
DATA
TAS
TAH
TRED
CS
TCS
TRECS
TARE
RE
TRECSH
TRED
TCSRLF
RPLY
TARL
WRITE
DAL
ADDRESS
DATA
TAS
TAH
CS
TAWE
TWECSH
TDS
TDH
TWECS
WE
TWE
TCSRLF
RPLY
TARL
INTERRUPT
DAL
INVALID ADDRESS CODE
ID CODE
TCSI
TIAD
TRED
CS
TCSRLF
RPLY
TIARL
TCSRE
TCSREH
TRECS
RE
TPI
IACKI
TII
TREI
IACKO

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS

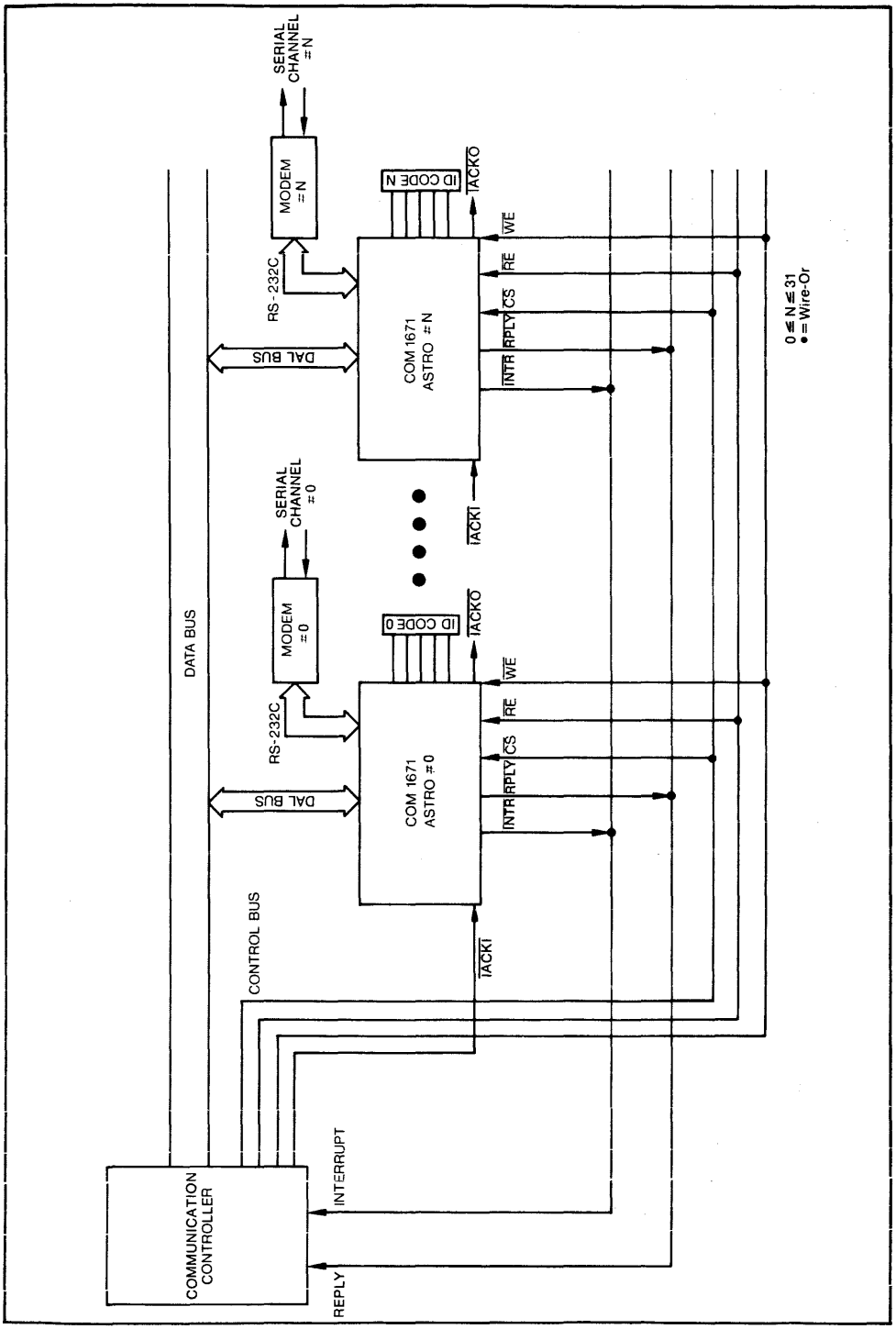
(T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V, unless otherwise noted)

Parameter		Min	Typ.	Max.	Unit	Comments
D.C. Characteristics						
INPUT VOLTAGE LEVELS						
Low Level, V_{IL}				0.8	V	
High Level, V_{IH}		2.4			V	
OUTPUT VOLTAGE LEVELS						
Low Level, V_{OL}			0.4		V	I_{OL} = 1.6ma
High Level, V_{OH}		2.4				I_{OH} = 100 μa
INPUT LEAKAGE						
Data Bus			5.0	10.0	μa	0 ≤ V_{IN} ≤ 5 v
All others			5.0	10.0	μa	V_{IN} = +12v
POWER SUPPLY CURRENT						
I_{CC}				80.0	ma	
I_{DD}				10.0	ma	
I_{BB}				1.0	ma	
A.C. Characteristics						T_A = 25°C
CLOCK-RCP, TCP						
frequency			1.0		MHz	
DAL Bus						
T_{AS}	Address Set-Up Time	0			ns	
T_{AH}	Address Hold Time	150			ns	
T_{ARL}	Address to $\overline{RPLY}$ Delay			400	ns	
T_{CS}	$\overline{CS}$ Width	250			ns	
T_{CSRLF}	$\overline{CS}$ to Reply OFF Relay	0		250	ns	R_L = 2.7 KΩ
Read						
T_{ARE}	Address and $\overline{RE}$ Spacing	250			ns	
T_{RECSH}	$\overline{RE}$ and $\overline{CS}$ Overlap	20			ns	
T_{RECS}	$\overline{RE}$ to $\overline{CS}$ Spacing	250			ns	
T_{RED}	$\overline{RE}$ to Data Out Delay			180	ns	C_L = 20 pf
Write						
T_{AWE}	Address to $\overline{WE}$ Spacing	250			ns	
T_{WECSH}	$\overline{WE}$ and $\overline{CS}$ Overlap	20			ns	
T_{WE}	$\overline{WE}$ Width	200		1000	ns	
T_{DS}	Data Set-Up Time	150			ns	
T_{DH}	Data Hold Time	100			ns	
T_{WECS}	$\overline{WE}$ to $\overline{CS}$ Spacing	250			ns	
Interrupt						
T_{CSI}	$\overline{CS}$ to $\overline{IACKI}$ Delay	0			ns	
T_{CSRE}	$\overline{CS}$ to $\overline{RE}$ Delay	250			ns	
T_{CSREH}	$\overline{CS}$ and $\overline{RE}$ Overlap	20			ns	
T_{RECS}	$\overline{RE}$ to $\overline{CS}$ Spacing	250			ns	
T_{PI}	$\overline{IACKI}$ Pulse Width	200			ns	
T_{IAD}	$\overline{IACKI}$ to Valid ID Code Delay			250	ns	See Note 1.
T_{RED}	$\overline{RE}$ OFF to $\overline{DAL}$ Open Delay			180	ns	
T_{IARL}	$\overline{IACKI}$ to $\overline{RPLY}$ Delay			250	ns	See Note 1.
T_{CSRLF}	$\overline{CS}$ to $\overline{RPLY}$ OFF Delay	0		250	ns	R_L = 2.7 KΩ
T_{II}	$\overline{IACKI}$ to $\overline{IACKO}$ Delay			200	ns	
T_{REI}	$\overline{RE}$ OFF to $\overline{IACKO}$ OFF Delay			250	ns	

Note 1: If $\overline{RE}$ goes low after $\overline{IACKI}$ goes low, the delay will be from the falling edge of $\overline{RE}$.

SECTION III

Multiple ASTRO System in Daisy-Chain Configuration



STANDARD MICROSYSTEMS CORPORATION

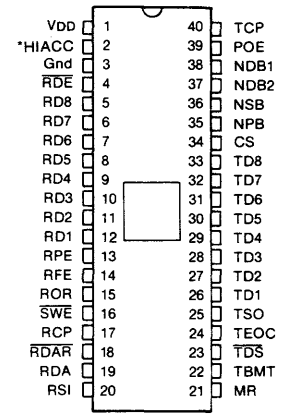
COM 1863
COM 8018
μPC FAMILY

Universal Asynchronous Receiver/Transmitter UART

FEATURES

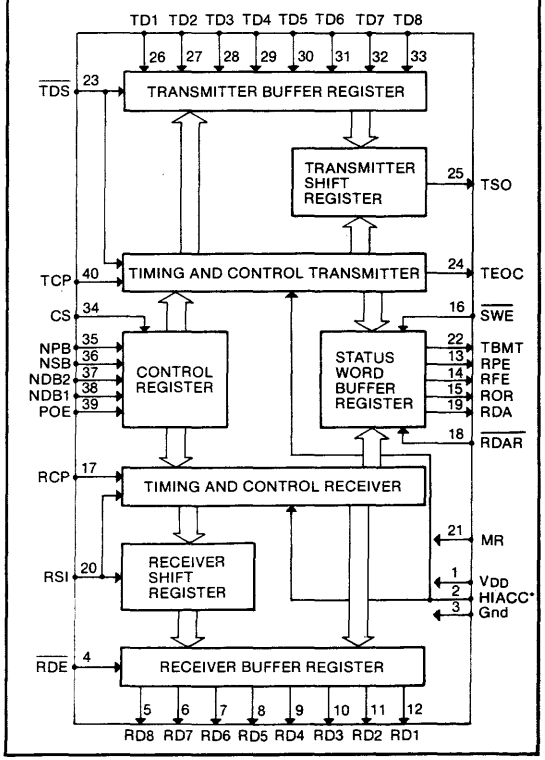
- ☐ Compatible with TR1863 timing
- ☐ High accuracy 32X clock mode: 48.4375% Receiver Distortion Immunity and improved RDA/ROR operation (COM 8018 only)
- ☐ High Speed Operation—62.5K baud, 200ns strobes
- ☐ Single +5V Power Supply
- ☐ Direct TTL Compatibility—no interfacing circuits required
- ☐ Input pull-up options: COM 8018 has low current pull-up resistors; COM 1863 has no pull up resistors
- ☐ Full or Half Duplex Operation—can receive and transmit simultaneously at different baud rates
- ☐ Fully Double Buffered—eliminates need for precise external timing
- ☐ Improved Start Bit Verification—decreases error rate
- ☐ 46.875% Receiver Distortion Immunity
- ☐ Fully Programmable—data word length; parity mode; number of stop bits: one, one and one-half, or two
- ☐ Master Reset—Resets all status outputs and Receiver Buffer Register
- ☐ Three State Outputs—bus structure oriented
- ☐ Low Power—minimum power requirements
- ☐ Input Protected—eliminates handling problems
- ☐ Ceramic or Plastic DIP Package—easy board insertion
- ☐ Baud Rates available from SMC's COM 8046, COM 8116, COM 8126, COM 8136, COM 8146 baud rate generators

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The Universal Asynchronous Receiver/Transmitter is an MOS/LSI monolithic circuit that performs all the receiving and transmitting functions associated with asynchronous data communications. This circuit is fabricated using SMC's patented COPLAMOS® technology and employs depletion mode loads, allowing operation from a single +5V supply. The duplex mode, baud rate, data word length, parity mode, and number of stop bits are independently programmable through the use of external controls. There may be 5, 6, 7, or 8 data bits, odd/even or no parity, and 1 or 2 stop bits or 1.5 stop bits when utilizing a 5-bit code. These programmable features provide the user with the ability to interface with all asynchronous peripherals.

*If pin 2 is taken to a logic 1 the COM 8018 will operate in a high accuracy mode. If pin 2 is connected to – 12V, GND, a valid logic zero, or left unconnected, the high accuracy feature is disabled, and the UART will operate in a 16X clock mode. Pin 2 is not connected on the COM 1863.

DESCRIPTION OF OPERATION— TRANSMITTER

At start-up the power is turned on, a clock whose frequency is 16 or 32 times the desired baud rate is applied, and master reset is pulsed. Under these conditions TBMT, TEOC, and TSO are all at a high level (the line is marking).

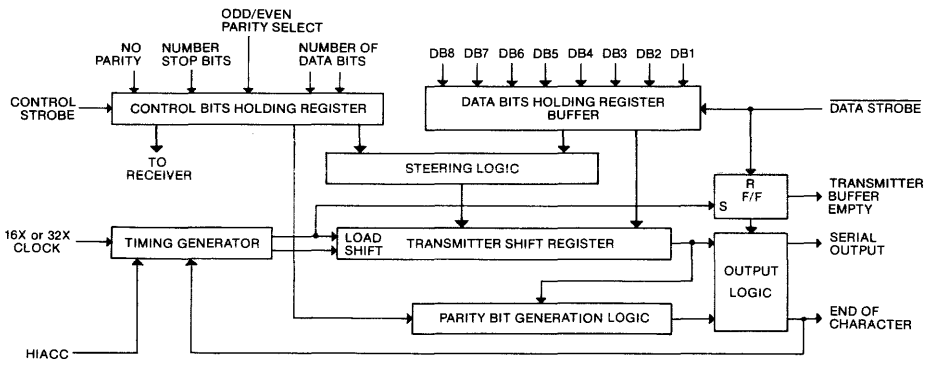
When TBMT and TEOC are high, the control bits may be set. After this has been done the data bits may be set. Normally, the control bits are strobed into the transmitter prior to the data bits. However, as long as minimum pulse width specifications are not violated, $\overline{TDS}$ and CS may occur simultaneously. Once the data strobe ($\overline{TDS}$) has been pulsed, the TBMT signal goes low, indicating that the data bits buffer register is full and unavailable to receive new data.

If the transmitter shift register is transmitting previously loaded data the TBMT signal remains low. If the transmitter shift register is empty, or when it is through transmitting the previous character, the data in the buffer register is loaded immediately into the transmitter shift register and data transmission commences. TEOC goes low, TSO goes low (the start bit), and TBMT goes high indicating that the data in the data bits buffer register has been loaded into the transmitter shift register and that the data bits buffer register is available to be loaded with new data.

If new data is loaded into the data bits buffer register at this time, TBMT goes low and remains in this state until the present transmission is completed. One full character time is available for loading the next character with no loss in speed of transmission. This is an advantage of double buffering.

Data transmission proceeds in an orderly manner: start bit, data bits, parity bit (if selected), and the stop bit(s). When the last stop bit has been on the line for one bit time TEOC goes high. If TBMT is low, transmission begins immediately. If TBMT is high the transmitter is completely at rest and, if desired, new control bits may be loaded prior to the next data transmission.

TRANSMITTER BLOCK DIAGRAM



DESCRIPTION OF OPERATION—RECEIVER

At start-up the power is turned on, a clock whose frequency is 16 or 32 times the desired baud rate is applied and master reset is pulsed. The data available (RDA) signal is now low. There is one set of control bits for both the receiver and transmitter.

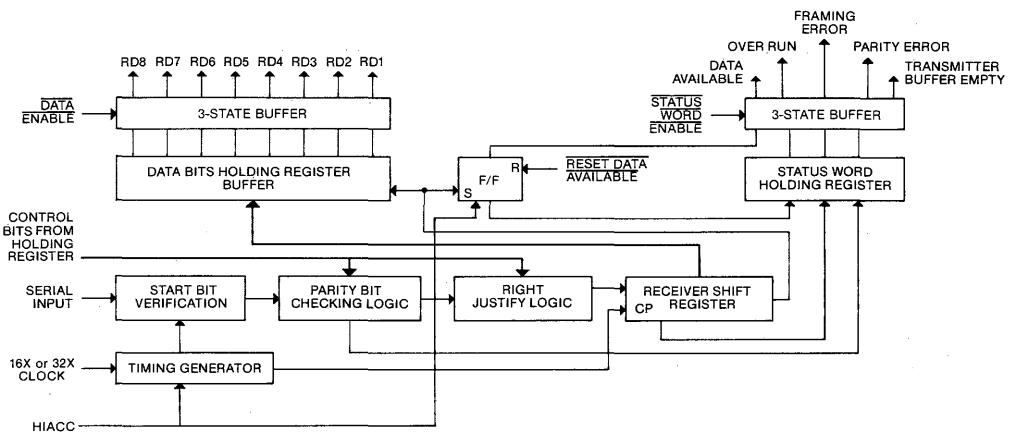
Data reception begins when the serial input line transitions for mark (high) to space (low). If the RSI line remains spacing for 15/32 to 17/32 bit times (in the 16X mode, HIACC = 0) or 31/64 to 33/64 bit times (in the 32X mode, HIACC = 1), a genuine start bit is verified. Should the line return to a marking condition prior to a 1/2 bit time, the start bit verification process begins again. A mark to space transition must occur in order to initiate start bit verification. Once a start bit has been verified, data reception proceeds in an orderly manner: start bit verified and received, data bits received, parity bit received (if selected) and the stop bit(s) received.

If the received parity bit is incorrect, the parity error flip-flop of the status word buffer register is set high, indicating a parity error. However, if the no parity mode is selected, the parity error flip-flop is unconditionally held low, inhibiting a parity error indication. If a stop bit is not received, the framing error flip-flop is set high, indicating a framing error.

On the negative RCP edge preceding the stop-bit center sample, internal logic looks at the data available (RDA) signal. If, at this instant, the RDA signal is high, or the $\overline{RDAR}$ signal is low, the receiver assumes that the previously received character has not been read out and the over-run flip-flop is set high. The only way the receiver is aware that data has been read out is by having the data available reset low.

Subsequently the RDA output goes high indicating that all outputs are available to be examined. The receiver shift register is now available to begin receiving the next character. Due to the double buffered receiver, a full character time is available to remove the received character.

RECEIVER BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
1	V_{DD}	Power Supply	+5 volt Supply
2	HIACC	High Accuracy Mode	Enables 32X clock and improved RDA/ROR operation. See NOTE on high accuracy mode.
3	GND	Ground	Ground
4	$\overline{RDE}$	Received Data Enable	A low-level input enables the outputs (RD8-RD1) of the receiver buffer register.
5-12	RD8-RD1	Receiver Data Outputs	These are the eight 3-state data outputs enabled by $\overline{RDE}$. Unused data output lines, as selected by NDB1 and NDB2, have a low-level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output.
13	RPE	Receiver Parity Error	This 3-state output (enabled by $\overline{SWE}$) is at a high-level if the received character parity bit does not agree with the selected parity.
14	RFE	Receiver Framing Error	This 3-state output (enabled by $\overline{SWE}$) is at a high-level if the received character has no valid stop bit.

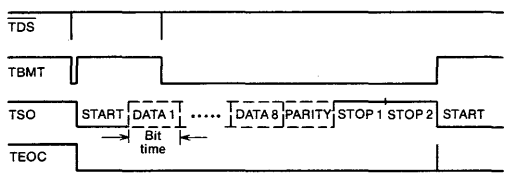
DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
15	ROR	Receiver Over Run	This 3-state output (enabled by $\overline{SWE}$) is at a high-level if the previously received character is not read (RDA output reset not completed) before the present character is transferred into the receiver buffer register.
16	$\overline{SWE}$	Status Word Enable	A low-level input enables the outputs (RPE, RFE, ROR, RDA, and TBMT) of the status word buffer register.
17	RCP	Receiver Clock	This input is a clock whose frequency is 16 times (16X) or 32 times (32X) the desired receiver baud rate.
18	$\overline{RDAR}$	Receiver Data Available Reset	A low-level input resets the RDA output to a low-level. $\overline{RDAR}$ must have gone low and come high again before ROR is sampled to avoid overrun indication.
19	RDA	Receiver Data Available	This 3-state output (enabled by $\overline{SWE}$) is at a high-level when an entire character has been received and transferred into the receiver buffer register.
20	RSI	Receiver Serial Input	This input accepts the serial bit input stream. A high-level (mark) to low-level (space) transition is required to initiate data reception.
21	MR	Master Reset	This input should be pulsed to a high-level after power turn-on. This sets TSO, TEOC, and TBMT to a high-level and resets RDA, RPE, RFE, ROR and RD1-RD8 to a low-level.
22	TBMT	Transmitter Buffer Empty	This 3-state output (enabled by $\overline{SWE}$) is at a high-level when the transmitter buffer register may be loaded with new data.
23	$\overline{TDS}$	Transmitter Data Strobe	A low-level input strobe enters the data bits into the transmitter buffer register.
24	TEOC	Transmitter End of Character	This output appears as a high-level during the last half clock cycle of the last stop bit. It remains at this level until the start of transmission of the next character or for one-half of a TCP period in the case of continuous transmission.
25	TSO	Transmitter Serial Output	This output serially provides the entire transmitted character. TSO remains at a high-level when no data is being transmitted.
26-33	TD1-TD8	Transmitter Data Inputs	There are 8 data input lines (strobed by $\overline{TDS}$) available. Unused data input lines, as selected by NDB1 and NDB2, may be in either logic state. The LSB should always be placed on TD1.
34	CS	Control Strobe	A high-level input enters the control bits (NDB1, NDB2, NSB, POE and NPB) into the control bits holding register. This line may be strobed or hard wired to a high-level.
35	NPB	No Parity Bit	A high-level input eliminates the parity bit from being transmitted: the stop bit(s) immediately follow the last data bit. In addition, the receiver requires the stop bit(s) to follow immediately after the last data bit. Also, the RPE output is forced to a low-level. See pin 39, POE.

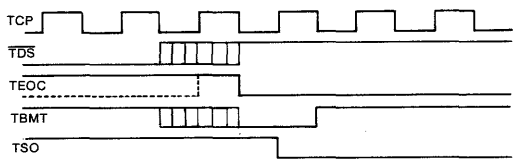
DESCRIPTION OF PIN FUNCTION

PIN NO.	SYMBOL	NAME	FUNCTION
36	NSB	Number of Stop Bits	This input selects the number of stop bits. A low-level input selects 1 stop bit; a high-level input selects 2 stop bits. Selection of two stop bits when programming a 5 data bit word generates 1.5 stop bits.
37-38	NDB2, NDB1	Number of Data Bits/Character	These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table: NDB2 NDB1 data bits/character L L 5 L H 6 H L 7 H H 8
39	POE	Odd/Even Parity Select	The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the receiver and transmitter, as per the following truth table: NPB POE MODE L L odd parity L H even parity H X no parity X = don't care
40	TCP	Transmitter Clock	This input is a clock whose frequency is 16 times (16X) or 32 times (32X) the desired transmitter baud rate.

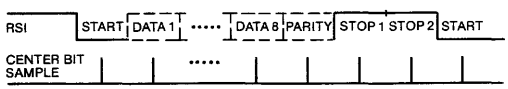
TRANSMITTER TIMING— 8 BIT, PARITY, 2 STOP BITS



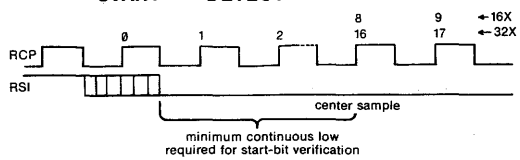
TRANSMITTER START-UP



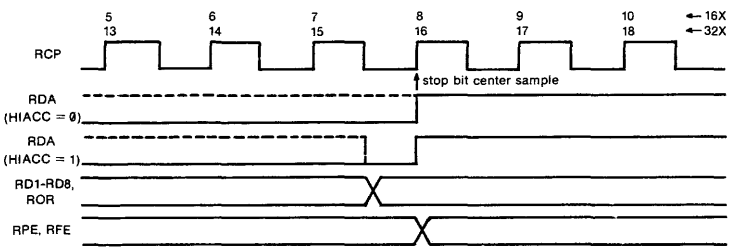
RECEIVER TIMING— 8 BIT, PARITY, 2 STOP BITS



START BIT DETECT AND VERIFY



RECEIVER TIMING DETAIL



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin (except Pin 2), with respect to ground ..... −0.3V
Negative Voltage on Pin 2, with respect to ground ..... −13.2V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that at clamp circuit be used.

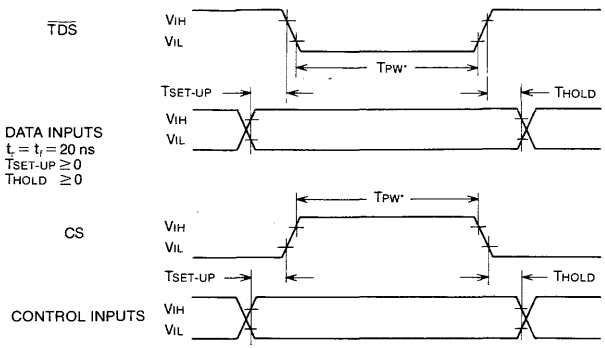
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $70°C$, $V_{DD} = +5V \pm 5\%$, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	
High-level, V_{IH}	2.0			V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	$I_{OL} = 1.6mA$
High-level, V_{OH}	2.4			V	$I_{OH} = -100\mu A$
INPUT CURRENT					
Low-level, I_{IL}			300	μA	V_{IN} = GND, COM 8018 only
INPUT LEAKAGE			±10	μA	COM 1863 only
OUTPUT CURRENT					
Leakage, I_{LO}			±10	μA	$\overline{SWE} = \overline{RDE} = V_{IH}$, $0 \leq V_{OUT} \leq +5V$
Short circuit, I_{OS}**			40	mA	$V_{OUT} = 0V$
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pf	$\overline{SWE} = \overline{RDE} = V_{IH}$
POWER SUPPLY CURRENT					
I_{CC}			25	mA	All outputs = V_{OH}, All inputs = V_{DD}
A.C. CHARACTERISTICS					$T_A = +25°C$, See Timing Diagrams
CLOCK FREQUENCY	DC		1.0	MHz	RCP, TCP
PULSE WIDTH					
Clock	0.45			μs	RCP, TCP
Master reset	500			ns	MR
Control strobe	200			ns	$\overline{CS}$
Transmitter data strobe	200			ns	$\overline{TDS}$
Receiver data available reset	200			ns	$\overline{RDAR}$
INPUT SET-UP TIME					
Data bits	0			ns	TD1-TD8
Control bits	0			ns	NPB, NSB, NDB2, NDB1, POE
INPUT HOLD TIME					
Data bits	0			ns	TD1-TD8
Control bits	0			ns	NPB, NSB, NDB2, NDB1, POE
ENABLE TO OUTPUT DELAY					Load = 20pf +1 TTL input
Receive data enable			250	ns	$\overline{RDE}$: T_{PD1}, T_{PD0}
Status word enable			250	ns	$\overline{SWE}$: T_{PD1}, T_{PD0}
OUTPUT DISABLE DELAY			250	ns	$\overline{RDE}$, $\overline{SWE}$

**Not more than one output should be shorted at a time.

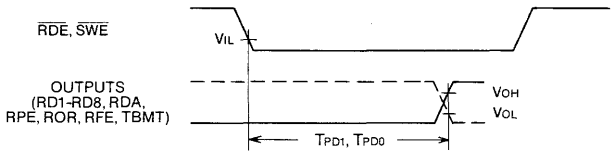
NOTES: 1. If the transmitter is inactive (TEOC and TBMT are at a high-level) the start bit will appear on the TSO line within 1½ clock period (TCP) after the trailing edge of $\overline{TDS}$.
2. The start bit (mark to space transition) will always be detected within one RCP clock period, guaranteeing a maximum start bit slippage of ±1/32 or ±1/64 of a bit time.
3. The 3-state output has 3 states: 1) low impedance to V_{DD} 2) low impedance to GND 3) high impedance OFF ≅ 10M ohms The "OFF" state is controlled by the $\overline{SWE}$ and $\overline{RDE}$ inputs.

DATA/CONTROL TIMING DIAGRAM



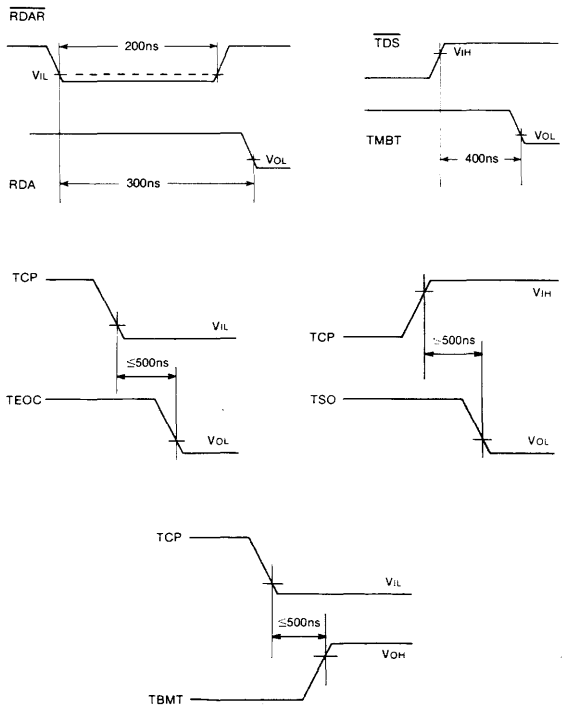
*Input information (Data/Control) need only be valid during the last TPW, min time of the input strobes (TDS, CS).

OUTPUT TIMING DIAGRAM



NOTE: Waveform drawings not to scale for clarity.

ADDITIONAL TIMING INFORMATION



NOTES ON COM 8018 AND COM 1863 HIGH-ACCURACY AND IMPROVED RDA/ROR MODE

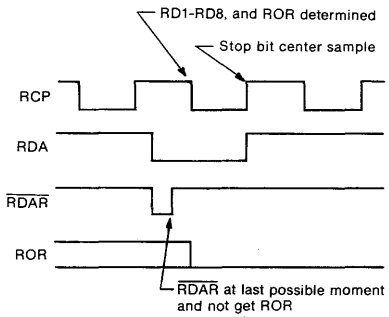
The HIACC mode is enabled by applying a logic "one" to pin 2. If this pin is left unconnected, or connected to GND, −12V, or a logic "zero," the HIACC mode is disabled. The HIACC input has an internal pull-down resistor.

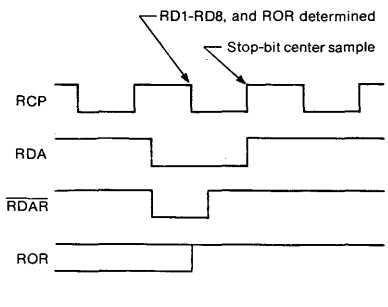
When the HIACC mode is selected, the TX and RX halves both operate on 32X instead of 16X clocks. Also, RDA is notched during the one half receiver clock cycle preceding the stop bit center sample when RD1-RD8 and ROR are changing.

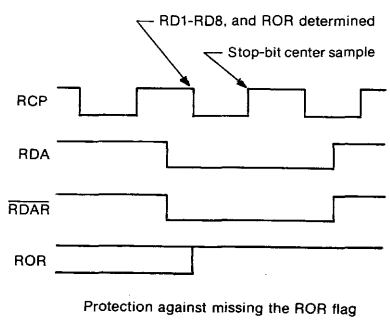
Whether or not the HIACC mode is selected, RDA must be low and $\overline{RDAR}$ must have returned high to avoid setting ROR. If $\overline{RDAR}$ is held low past the stop-bit center sample, RDA will go high after $\overline{RDAR}$ returns high.

The maximum current HIACC will supply if connected to −13.2V is 3.5mA.

IMPROVED RDA/ROR OPERATION TIMING DIAGRAMS

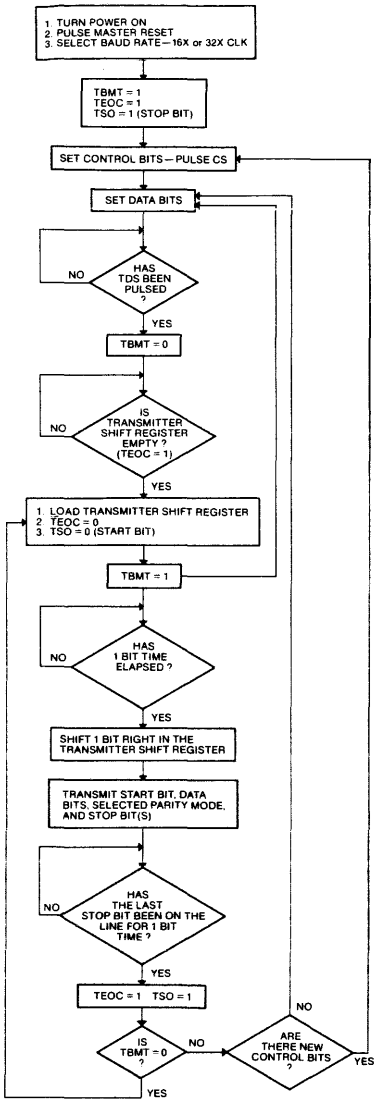




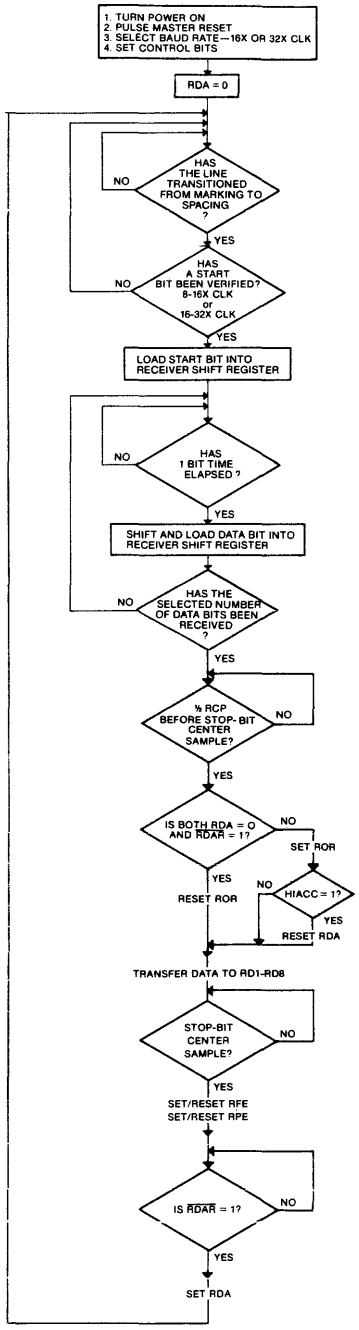


Protection against missing the ROR flag

FLOW CHART—TRANSMITTER



FLOW CHART—RECEIVER



STANDARD MICROSYSTEMS CORPORATION

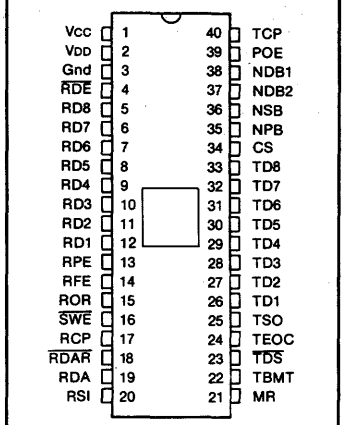
COM2502
COM2017
COM2502/H
COM2017/H

Universal Asynchronous Receiver/Transmitter
UART

FEATURES

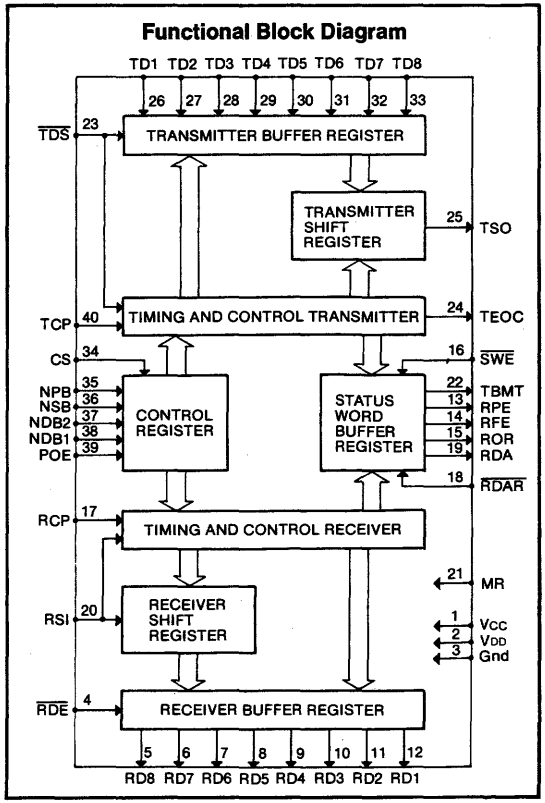
- ☐ Direct TTL Compatibility — no interfacing circuits required
- ☐ Full or Half Duplex Operation — can receive and transmit simultaneously at different baud rates
- ☐ Fully Double Buffered — eliminates need for precise external timing
- ☐ Start Bit Verification — decreases error rate
- ☐ Fully Programmable — data word length, parity mode, number of stop bits; one, one and one-half, or two
- ☐ High Speed Operation — 40K baud, 200ns strobes
- ☐ Master Reset — Resets all status outputs
- ☐ Tri-State Outputs — bus structure oriented
- ☐ Low Power — minimum power requirements
- ☐ Input Protected — eliminates handling problems
- ☐ Ceramic or Plastic Dip Package — easy board insertion

Pin Configuration



PACKAGE: 40-Pin D.I.P.

Functional Block Diagram



GENERAL DESCRIPTION

The Universal Asynchronous Receiver/Transmitter is an MOS/LSI monolothic circuit that performs all the receiving and transmitting functions associated with asynchronous data communications. This circuit is fabricated using SMC's P-channel low voltage oxide-nitride technology. The duplex mode, baud rate, data word length, parity mode, and number of stop bits are independently programmable through the use of external controls. There may be 5, 6, 7 or 8 data bits, odd/even or no parity, and 1, or 2 stop bits or 1.5 stop bits when utilizing a 5-bit code from the COM 2017 or COM 2017/H. The UART can operate in either the full or half duplex mode. These programmable features provide the user with the ability to interface with all asynchronous peripherals.

DESCRIPTION OF OPERATION— TRANSMITTER

At start-up the power is turned on, a clock whose frequency is 16 times the desired baud rate is applied and master reset is pulsed. Under these conditions TBMT, TEOC, and TSO are all at a high level (the line is marking).

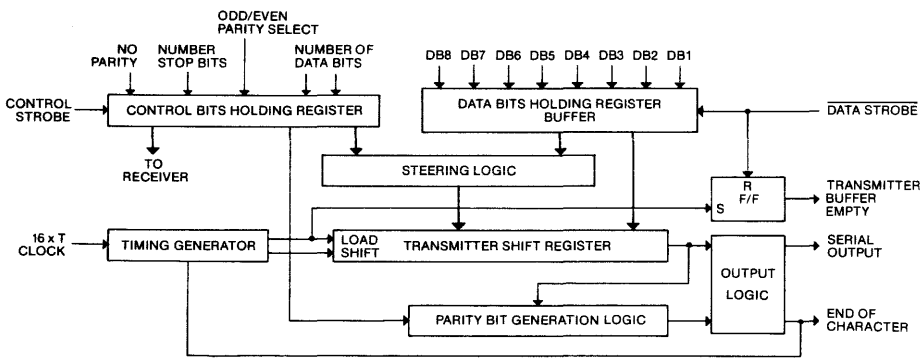
When TBMT and TEOC are high, the control bits may be set. After this has been done the data bits may be set. Normally, the control bits are strobed into the transmitter prior to the data bits. However, as long as minimum pulse width specifications are not violated, $\overline{TDS}$ and CS may occur simultaneously. Once the date strobe ($\overline{TDS}$) has been pulsed the TBMT signal goes low, indicating that the data bits buffer register is full and unavailable to receive new data.

If the transmitter shift register is transmitting previously loaded data the $\overline{TBMT}$ signal remains low. If the transmitter shift register is empty, or when it is through transmitting the previous character, the data in the buffer register is loaded immediately into the transmitter shift register and data transmission commences. TSO goes low (the start bit), TEOC goes low, the TBMT goes high indicating that the data in the data bits buffer register has been loaded into the transmitter shift register and that the data bits buffer register is available to be loaded with new data.

If new data is loaded into the data bits buffer register at this time, TBMT goes low and remains in this state until the present transmission is completed. One full character time is available for loading the next character with no loss in speed of transmission. This is an advantage of double buffering.

Data transmission proceeds in an orderly manner: start bit, data bits, parity bit (if selected), and the stop bit(s). When the last stop bit has been on the line for one bit time TEOC goes high. If TBMT is low, transmission begins immediately. If TBMT is high the transmitter is completely at rest and, if desired, new control bits may be loaded prior to the next data transmission.

TRANSMITTER BLOCK DIAGRAM



DESCRIPTION OF OPERATION—RECEIVER

At start-up the power is turned on, a clock whose frequency is 16 times the desired baud rate is applied and master reset is pulsed. The data available (RDA) signal is now low. There is one set of control bits for both the receiver and transmitter.

Data reception begins when the serial input line transitions from mark (high) to space (low). If the RSI line remains spacing for a 1/2 bit time, a genuine start bit is verified. Should the line return to a marking condition prior to a 1/2 bit time, the start bit verification process begins again. A mark to space transition must occur in order to initiate start bit verification. Once a start bit has been verified, data reception proceeds in an orderly manner: start bit verified and received, data bits received, parity bit received (if selected) and the stop bit(s) received.

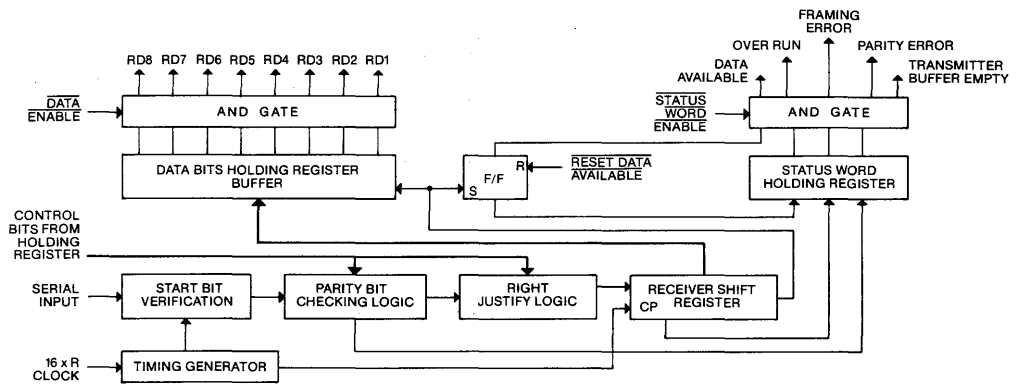
If the transmitted parity bit does not agree with the received parity bit, the parity error flip-flop of the

status word buffer register is set high, indicating a parity error. However, if the no parity mode is selected, the parity error flip-flop is unconditionally held low, inhibiting a parity error indication. If a stop bit is not received, due to an improperly framed character, the framing error flip-flop is set high, indicating a framing error.

Once a full character has been received internal logic looks at the data available (RDA) signal. If, at this instant, the RDA signal is high the receiver assumes that the previously received character has not been read out and the over-run flip-flop is set high. The only way the receiver is aware that data has been read out is by having the data available reset low.

At this time the RDA output goes high indicating that all outputs are available to be examined. The receiver shift register is now available to begin receiving the next character. Due to the double buffered receiver, a full character time is available to remove the received character.

RECEIVER BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
1	V_{CC}	Power Supply	+5 volt Supply
2	V_{DD}	Power Supply	−12 volt Supply
3	GND	Ground	Ground
4	$\overline{RDE}$	Received Data Enable	A low-level input enables the outputs (RD8-RD1) of the receiver buffer register.
5-12	RD8-RD1	Receiver Data Outputs	These are the 8 tri-state data outputs enabled by $\overline{RDE}$. Unused data output lines, as selected by NDB1 and NDB2, have a low-level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output.
13	RPE	Receiver Parity Error	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the received character parity bit does not agree with the selected parity.
14	RFE	Receiver Framing Error	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the received character has no valid stop bit.

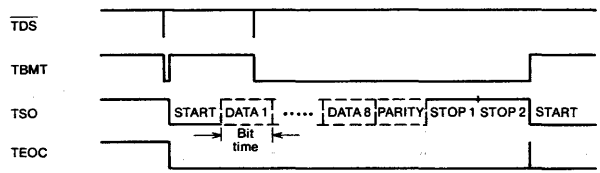
DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
15	ROR	Receiver Over Run	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the previously received character is not read (RDA output not reset) before the present character is transferred into the receiver buffer register.
16	$\overline{SWE}$	Status Word Enable	A low-level input enables the outputs (RPE, RFE, ROR, RDA, and TBMT) of the status word buffer register.
17	RCP	Receiver Clock	This input is a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	$\overline{RDAR}$	Receiver Data Available Reset	A low-level input resets the RDA output to a low-level.
19	RDA	Receiver Data Available	This tri-state output (enabled by $\overline{SWE}$) is at a high-level when an entire character has been received and transferred into the receiver buffer register.
20	RSI	Receiver Serial Input	This input accepts the serial bit input stream. A high-level (mark) to low-level (space) transition is required to initiate data reception.
21	MR	Master Reset	This input should be pulsed to a high-level after power turn-on. This sets TSO, TEOC, and TBMT to a high-level and resets RDA, RPE, RFE and ROR to a low-level.
22	TBMT	Transmitter Buffer Empty	This tri-state output (enabled by $\overline{SWE}$) is at a high-level when the transmitter buffer register may be loaded with new data.
23	$\overline{TDS}$	Transmitter Data Strobe	A low-level input strobe enters the data bits into the transmitter buffer register.
24	TEOC	Transmitter End of Character	This output appears as a high-level each time a full character is transmitted. It remains at this level until the start of transmission of the next character or for one-half of a TCP period in the case of continuous transmission.
25	TSO	Transmitter Serial Output	This output serially provides the entire transmitted character. TSO remains at a high-level when no data is being transmitted.
26-33	TD1-TD8	Transmitter Data Inputs	There are 8 data input lines (strobed by $\overline{TDS}$) available. Unused data input lines, as selected by NDB1 and NDB2, may be in either logic state. The LSB should always be placed on TD1.
34	CS	Control Strobe	A high-level input enters the control bits (NDB1, NDB2, NSB, POE and NPB) into the control bits holding register. This line may be strobed or hard wired to a high-level.
35	NPB	No Parity Bit	A high-level input eliminates the parity bit from being transmitted; the stop bit(s) immediately follow the last data bit. In addition, the receiver requires the stop bit(s) to follow immediately after the last data bit. Also, the RPE output is forced to a low-level. See pin 39, POE.

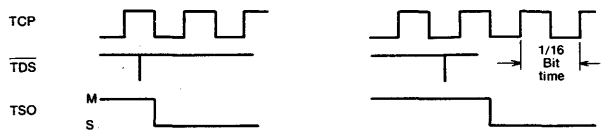
DESCRIPTION OF PIN FUNCTION

PIN NO.	SYMBOL	NAME	FUNCTION
36	NSB	Number of Stop Bits	This input selects the number of stop bits. A low-level input selects 1 stop bit; a high-level input selects 2 stop bits. Selection of 2 stop bits when programming a 5 data bit word generates 1.5 stop bits from the COM 2017 or COM 2017/H.
37-38	NDB2, NDB1	Number of Data Bits/Character	These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table: NDB2 NDB1 data bits/character L L 5 L H 6 H L 7 H H 8
39	POE	Odd/Even Parity Select	The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the receiver and transmitter, as per the following truth table: NPB POE MODE L L odd parity L H even parity H X no parity X = don't care
40	TCP	Transmitter Clock	This input is a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

TRANSMITTER TIMING—8 BIT, PARITY, 2 STOP BITS

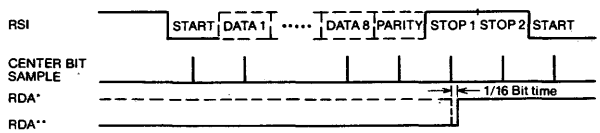


TRANSMITTER START-UP



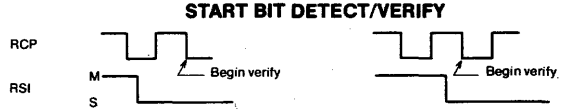
Upon data transmission initiation, or when not transmitting at 100% line utilization, the start bit will be placed on the TSO line at the high to low transition of the TCP clock following the trailing edge of TDS.

RECEIVER TIMING—8 BIT, PARITY, 2 STOP BITS



*The RDA line was previously not reset (ROR = high-level).
**The RDA line was previously reset (ROR = low-level).

START BIT DETECT/VERIFY



If the RSI line remains spacing for a 1/2 bit time, a genuine start bit is verified. Should the line return to a marking condition prior to a 1/2 bit time, the start bit verification process begins again.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, V_{CC} ..... +0.3V
Negative Voltage on any Pin, V_{CC} ..... −25V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0° C to 70° C, V_{CC} = +5V ±5%, V_{DD} = −12V ±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Conditions
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}	V_{DD}		0.8	V	
High-level, V_{IH}	V_{CC}-1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}		0.2	0.4	V	I_{OL} = 1.6mA
High-level, V_{OH}	2.4	4.0		V	I_{OH} = 100μA
INPUT CURRENT					
Low-level, I_{IL}			1.6	mA	see note 4
OUTPUT CURRENT					
Leakage, I_{LO}			−1	μA	$\overline{SWE}$ = $\overline{RDE}$ = V_{IH}, 0 ≤ V_{OUT} ≤ +5V
Short circuit, I_{OS}**			10	mA	V_{OUT} = 0V
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	V_{IN} = V_{CC}, f = 1MHz
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pf	$\overline{SWE}$ = $\overline{RDE}$ = V_{IH}, f = 1MHz
POWER SUPPLY CURRENT					
I_{CC}			28	mA	All outputs = V_{OH}, All inputs = V_{CC}
I_{DD}			28	mA	
A.C. CHARACTERISTICS					T_A = +25° C
CLOCK FREQUENCY					
(COM2502, COM2017)	DC		400	KHz	RCP, TCP
(COM2502H, COM2017H)	DC		640	KHz	RCP, TCP
PULSE WIDTH					
Clock	1			μs	RCP, TCP
Master reset	500			ns	MR
Control strobe	200			ns	$\overline{CS}$
Transmitter data strobe	200			ns	$\overline{TDS}$
Receiver data available reset	200			ns	$\overline{RDAR}$
INPUT SET-UP TIME					
Data bits	≥0			ns	TD1-TD8
Control bits	≥0			ns	NPB, NSB, NDB2, NDB1, POE
INPUT HOLD TIME					
Data bits	≥0			ns	TD1-TD8
Control bits	≥0			ns	NPB, NSB, NDB2, NDB1, POE
STROBE TO OUTPUT DELAY					Load = 20pf +1 TTL input
Receive data enable			350	ns	$\overline{RDE}$: T_{PD1}, T_{PD0}
Status word enable			350	ns	$\overline{SWE}$: T_{PD1}, T_{PD0}
OUTPUT DISABLE DELAY			350	ns	$\overline{RDE}$, $\overline{SWE}$

**Not more than one output should be shorted at a time.

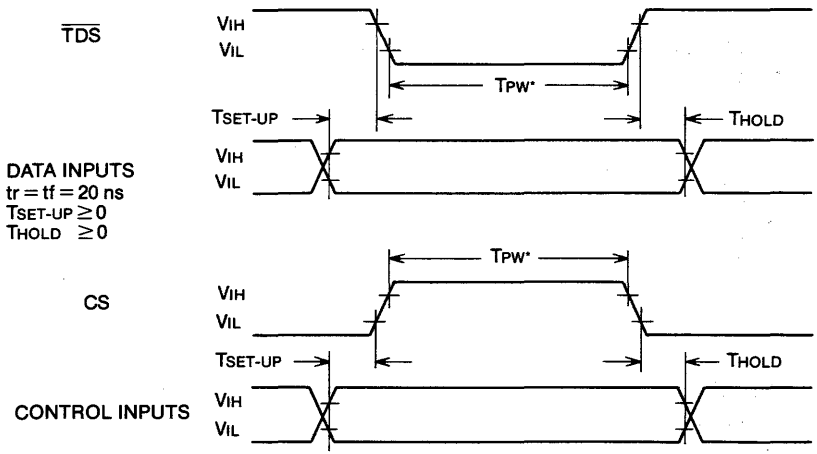
NOTES: 1. If the transmitter is inactive (TEOC and TBMT are at a high-level) the start bit will appear on the TSO line within one clock period (TCP) after the trailing edge of $\overline{TDS}$.

2. The start bit (mark to space transition) will always be detected within one clock period of RCP, guaranteeing a maximum start bit slippage of 1/16th of a bit time.

3. The tri-state output has 3 states: 1) low impedance to V_{CC} 2) low impedance to GND 3) high impedance OFF ≅ 10M ohms. The "OFF" state is controlled by the $\overline{SWE}$ and $\overline{RDE}$ inputs.

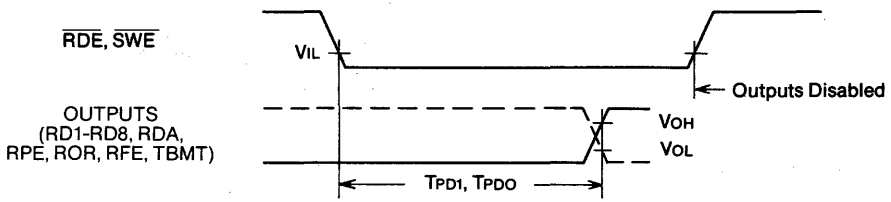
4. Under steady state conditions no current flows for TTL or MOS interfacing. (COM 2502 or COM 2502/H)

DATA/CONTROL TIMING DIAGRAM

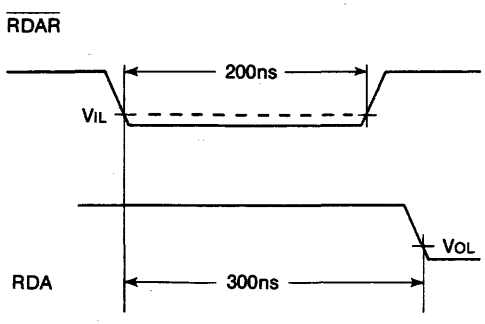


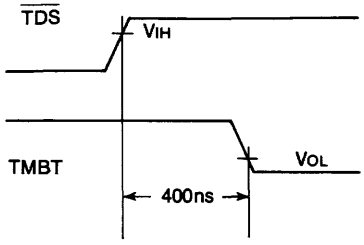
*Input information (Data/Control) need only be valid during the last TPW, min time of the input strobes (TDS, CS).

OUTPUT TIMING DIAGRAM

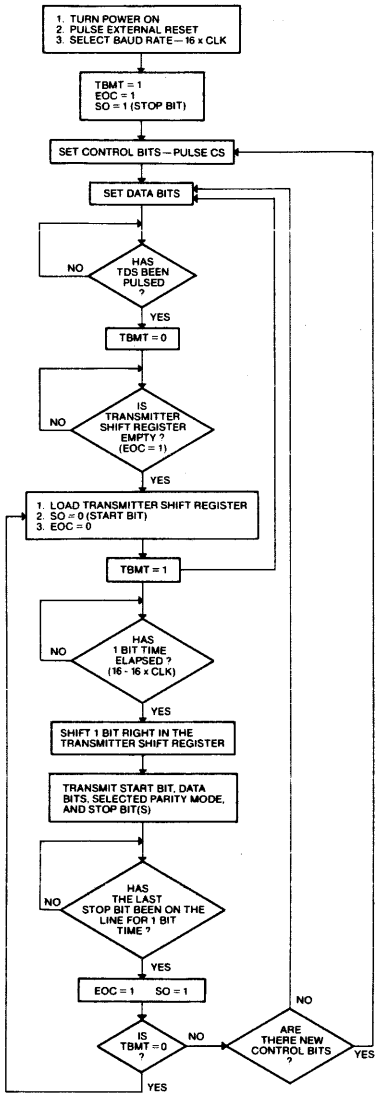


NOTE: Waveform drawings not to scale for clarity.

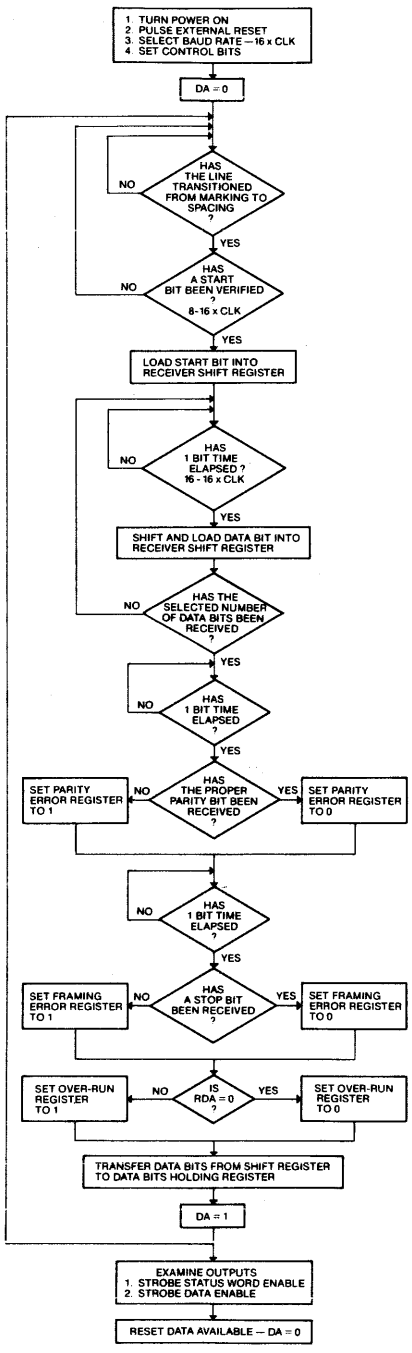




FLOW CHART—TRANSMITTER



FLOW CHART—RECEIVER



STANDARD MICROSYSTEMS CORPORATION

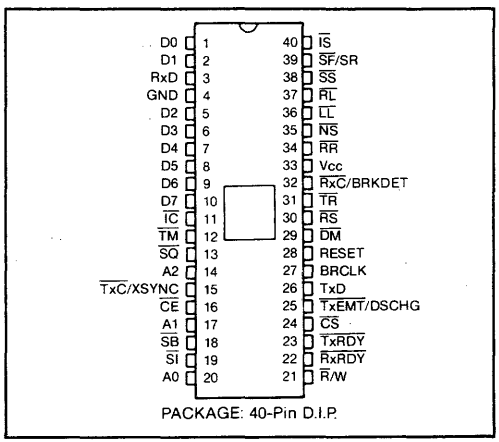
COM 2449-1
COM 2449-2
COM 2449-3
μPC FAMILY

RS-449 Programmable Communications Interface

FEATURES

- ☐ RS-449 compatible inputs and outputs
- ☐ Maskable Interrupts for RS-449 inputs
- ☐ Synchronous and Asynchronous Full Duplex or Half Duplex Operations
- ☐ Re-programmable ROM on-chip baud rate generator
- ☐ Synchronous Mode Capabilities
  - —Selectable 5 to 8-Bit Characters
  - —Selectable 1 or 2 SYNC Characters
  - —Internal or External Character Synchronization
  - —Transparent or Non-Transparent Mode
  - —Transparent mode DLE stuffing (Tx) and detection (Rx)
  - —Automatic SYNC or DLE-SYNC Insertion
  - —SYNC, DLE and DLE-SYNC stripping
  - —Odd, Even, or No Parity
  - —Local or remote maintenance loop back mode
- ☐ Asynchronous Mode Capabilities
  - —Selectable 5 to 8-Bit Characters plus parity
  - —3 Selectable Clock Rates (1X, 16X, 64X the Baud Rate)
  - —Line Break Detection and Generation
  - —1, 1½, or 2-Stop Bit Detection and Generation
  - —False Start Bit Detection
  - —Odd, Even, or No Parity
  - —Parity, Overrun, and framing error detect
  - —Local or remote maintenance loop back mode
  - —Automatic serial echo mode (echoplex)
- ☐ Baud Rates
  - —DC to 1.0M Baud (Synchronous)
  - —DC to 1.0M Baud (1X, Asynchronous)
  - —DC to 62.5K Baud (16X, Asynchronous)
  - —DC to 15.625K Baud (64X, Asynchronous)
- ☐ Double Buffering of Data
- ☐ RxC and TxC pins are short circuit protected
- ☐ Internal or External Baud Rate Clock
- ☐ 3 baud rate sets (2449-1, -2, -3)
- ☐ 16 internal rates for each version
- ☐ Single +5 volt Power Supply
- ☐ TTL Compatible
- ☐ No System Clock Required

PIN CONFIGURATION

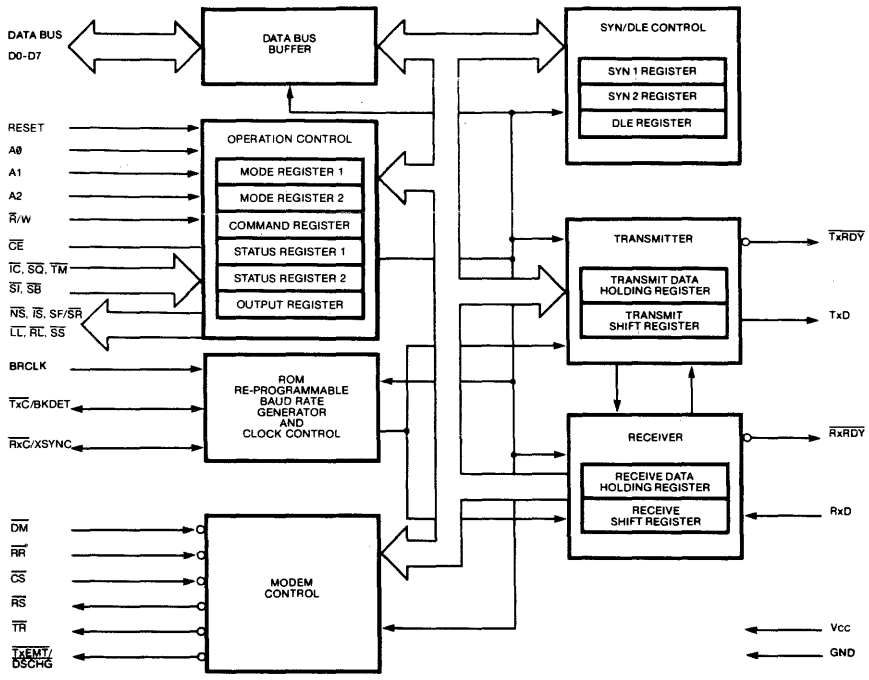


PACKAGE: 40-Pin D.I.P.

GENERAL DESCRIPTION

The COM 2449 is an MOS/LSI device fabricated using SMC's patented COPLAMOS® technology. It is equivalent to the COM 2661 with the additional features required to create the interface to an RS-449 compatible modem. Six new outputs are added to implement the RS-449 signals sent to the Data Communications Equipment (DCE) and five new signals are added to receive the RS-449 status signals from the DCE. A second status register and an output register have been added to allow a processor full control of the additional I/O pins. The COM 2449 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. Each version of the COM 2449 (-1, -2, -3) has a different set of baud rates. Custom baud rates can be ROM reprogrammed to accommodate different baud rates and different starting frequencies.

The COM 2449 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for microcomputer system data communications. The USART is used as a peripheral and is programmed by the processor to communicate in commonly used asynchronous and synchronous serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status including data format errors and control signals is available to the processor at any time.



COM 2449 ORGANIZATION

The COM 2449 is organized into 6 major sections. Communication between each section is achieved via an internal data and control bus. The data bus buffer allows a processor access to all internal registers on the COM 2449. The COM 2449 is a COM 2661 with 5 new inputs (readable by the processor from STATUS REGISTER 2) and 6 new outputs (written by the processor via the OUTPUT REGISTER). Each of the 5 new inputs can cause an interrupt condition on the COM 2449. The ability to enable these conditions for interrupt handling is provided. Table 1 outlines the differences between the COM 2661 and the COM 2449. It should be noted that the COM 2449 can be viewed as a general purpose communications interface device with general purpose I/O pins to allow setting output controls and interrogation of input status. This additional I/O capability, although added to allow RS-449 compatibility, can ease the interface to any communications discipline.

Operation Control

This functional block stores configuration and operation commands from the processor and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with a processor via the data bus and contains Mode Registers 1 and 2, the Command Register, the two Status Registers, and the Output Register. Details of register addressing and protocol are presented in the COM 2449 programming section of this specification.

Timing

The COM 2449 contains a Baud Rate Generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full duplex operation. Tables 2a, b, and c illustrate all available baud rates.

Receiver

The Receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and stores the "assembled" character in the receive data holding register until read by the processor.

Transmitter

The Transmitter accepts parallel data from the processor, converts it to a serial bit stream. inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Modem Control

The modem control provides three output signals and accepts three input signals used for "handshaking" and status indication between the COM 2449 and a modem. Five signals to and from the modem control are given names that are in accordance with the RS-449 specification. The signals, however, have an identical function to the corresponding COM 2661 RS-232 compatible signals and this correspondence is shown in Table 1.

SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the processor. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

Interface Signals

The COM 2449 interface signals can be grouped into two types: the processor-related signals (shown in Table 3) which interface the COM 2449 to the processor, and the device-related signals (shown in Table 4), which are used to interface to the communications equipment.

DESCRIPTION OF PIN FUNCTIONS

TABLE 3—PROCESSOR RELATED SIGNALS

PIN NO.	NAME	SYMBOL	FUNCTION
1,2,5,6, 7,8,9,10	Data	D7-D0	Bidirectional; 8 bit, three state data bus used to transfer commands, data and status between the COM 2449 and a processor. D0 is the least significant bit; D7 is the most significant bit.
14,17,20	Address	A2, A1, A0	Input; Address lines used to select COM 2449 registers.
16	Chip Enable	$\overline{CE}$	Input; when this signal is low, the operation specified by the $\overline{R}$/W, A2, A1 and A0 will be performed. When this input is high, D7-0 are in the high impedance state.
21	Read/Write	$\overline{R}$/W	Input; Processor read/write direction control. This signal defines the direction of the data bus D7-0 when the COM 2449 is selected. D7-0 drives out (read) when this signal is low and accepts data input when this signal is high. The input only has meaning when the $\overline{CE}$ input is active.
22	Receiver Ready	$\overline{RxRDY}$	Output; This signal is the complement of Status Register 1, bit 1 (SR11). When low, it indicates that the Receive Data Holding Register (RHR) has a character ready for input to the processor. It goes high when the RHR is read by the processor, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the processor.
23	Transmitter Ready	$\overline{TxRDY}$	Output; This signal is the complement of Status Register 1, bit 0 (SR10). When low, it indicates that the Transmit Data Holding Register (THR) is ready to accept a data character from the processor. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the processor.
25	Transmitter empty/data set change	$\overline{TxEMT}$/ $\overline{DSCHG}$	Output; This signal is the complement of Status Register 1, bit 2 (SR12). When low, it indicates that the transmitter has completed serialization of the last character loaded by the processor, or that a change of state of the $\overline{DM}$ or $\overline{RR}$ inputs has occurred. This signal also goes low if the $\overline{SI}$, $\overline{SB}$, $\overline{SQ}$, $\overline{TM}$ or $\overline{IC}$ experience a change of state if the corresponding input is enable for interrupt. Interrupt enable bits are located in the 3 most significant bits of Status Register 2 (SR2). This output goes high when Status Register 1 is read by the processor, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the processor for this line to go high. It is an open drain output which can be used as an interrupt to the processor.
28	Reset	RESET	Input; A high on this input performs a master reset on the COM 2449. This signal asynchronously terminates any device activity and clears the Mode, Command and Status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.
33	Supply Voltage	V_{CC}	+5 volt supply.
4	Ground	GND	Ground.

TABLE 4—DEVICE RELATED SIGNALS

PIN NO.	NAME	SYMBOL	FUNCTION
3	Receive Data	RxD	Input: Serial data to the receiver. "Mark" is high, "space" is low.
11	Incoming Call	$\overline{IC}$	Input: This general purpose signal can be used for "incoming call" status from the DCE. Its complement appears in Status Register 2 bit 0 (SR20). When this input is enabled for interrupt via Status Register 2 bit 5 (SR25), a change in its state will cause a low output on $\overline{TxEMT/DSCHG}$.
12	Test Mode	$\overline{TM}$	Input: This general purpose signal can be used for "test mode" status from the DCE. Its complement appears in Status Register 2 bit 1 (SR21). When this input is enabled for interrupt via Status Register 2, bit 6 (SR26) a change in its state will cause a low output on $\overline{TxEMT/DSCHG}$.
13	Signal Quality	$\overline{SQ}$	Input: This general purpose signal can be used for "signal quality" status from the DCE. Its complement appears in Status Register 2 bit 2 (SR22). When this input is enabled for interrupt via Status Register 2 bit 7 (SR27) a change in its state will cause a low output on $\overline{TxEMT/DSCHG}$.

TABLE 4—DEVICE RELATED SIGNALS (Cont'd)

PIN NO.	NAME	SYMBOL	FUNCTION
15	Transmitter Clock/External Sync	$\overline{TxC}$/ XSYNC	Input or Output: If the external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X, or 64X the baud rate as programmed by mode Register 1. The transmitted data changes on the falling edge of the clock. If the internal transmitter clock is programmed, this pin can be a 1X/16X clock output or an external jam synchronization input.
18	Standby Indicator	$\overline{SB}$	Input: This general purpose signal can be used for "standby indicator" status from the DCE. Its complement appears in Status Register 2 bit 3 (SR23). When this input is enabled for interrupt via Status Register 2 bit 7 (SR27), a change in its state will cause a low output on $\overline{TxEMT/DSCHG}$.
19	Signalling Rate Indicator	$\overline{SI}$	Input: This general purpose signal can be used for "signalling rate indicator" status from the DCE. Its complement appears in Status Register 2 bit 4 (SR24). When this input is enabled for interrupt via Status Register 2 bit 7 (SR27), a change in its state will cause a low output on $\overline{TxEMT/DSCHG}$.
24	Clear to Send	$\overline{CS}$	Input: This signal must be low in order for the transmitter to function. If it goes high during transmission, the character in the Transmit Shift Register will be transmitted before termination.
26	Transmit Data	TxD	Output: Serial data from the transmitter. "Mark" is high, "Space" is low. This signal is held in the "Mark" condition when the transmitter is disabled.
27	Baud Rate Clock	BRCLK	Input: Clock input to the internal baud rate generator (See Tables 2a, b, and c); not required if the external receiver and transmitter clocks are used.
29	Data Mode	$\overline{DM}$	Input: This general purpose signal can be used for Data Mode, Data Set Ready or Ring Indicator condition. Its complement appears as Status Register 1 bit 7 (SR17). DM causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes if CR2 or CR0=1.
30	Request to Send	$\overline{RS}$	Output: This general purpose signal is the complement of the Command Register bit 5 (CR5). It is normally used to indicate Request to Send. If the Transmit Shift Register is not empty when CR5 is reset (1 to 0), then $\overline{RS}$ will go high on TxC time after the last serial bit is transmitted.
31	Terminal Ready	$\overline{TR}$	Output: This general purpose signal is the complement of the Command Register bit 1 (CR1). It is normally used to indicate Terminal Ready.
32	Receive Clock/ Break Detect	$\overline{RxC}$/ BKDET	Input or Output: If the external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X, or 64X the Baud rate as programmed by Mode Register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin can be a 1X/16X clock or a break detect output.
34	Receiver Ready	$\overline{RR}$	Input: This signal must be low in order for the receiver to function. The complement appears in Status Register 1 bit 6 (SR16). $\overline{RR}$ causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes if CR2 or CR0=1. If $\overline{RR}$ goes high while receiving, the RxC is internally inhibited.
35	New Signal	$\overline{NS}$	Output: This signal is used to tell the DCE that a new line signal at the DTE has occurred. This output will go to its low active state when the Output Register, bit 0 (OR0) is set to a logic 1. This output will go to its high inactive state when the Output Register bit 0 (OR0) is set to a logic 0 and the $\overline{RR}$ input goes high.
36	Local Loopback	$\overline{LL}$	Output: This general purpose signal can be used to inform the DCE of a "local loopback" test condition. It is the complement of Output Register bit 1 (OR1) which has direct control over the state of this output.
37	Remote Loopback	$\overline{RL}$	Output: This general purpose signal can be used to inform the DCE of a "remote loopback" test condition. It is the complement of Output Register bit 2 (OR2) which has direct control over the state of this output.
38	Select Standby	$\overline{SS}$	Output: This general purpose signal can be used to select the normal or standby communication facilities of the DCE. It is the complement of Output Register bit 3 (OR3) which has direct control over the state of this output.
39	Select Frequency/ Signal Rate Select	$\overline{SF/SR}$	Output: This general purpose signal can be used as a combined "Select Frequency" and "Signal Rate Select". It is the complement of Output Register bit 4 (OR4) which has direct control over the state of this output.
40	Terminal in Service	$\overline{IS}$	Output: This general purpose signal can be used to inform the DCE of a "Terminal in Service" condition. It is the complement of Output Register bit 5 (OR5) which has direct control over the state of this output.

Table 1 COM 2449 vs. COM 2661

NEW INPUTS		NEW OUTPUTS		I/O SIGNAL NAME EQUIVALENTS	
Symbol	Name	Symbol	Name	COM 2449	COM 2661
$\overline{IC}$	incoming call	$\overline{NS}$	new signal	DM	DSR
$\overline{SQ}$	signal quality	$\overline{IS}$	terminal in service	RR	DCD
$\overline{TM}$	test mode	$\overline{SF}$/SR	select frequency/ signal rate select	CS	CTS
$\overline{SI}$	signaling rate indicator	$\overline{LL}$	local loopback	TR	DTR
$\overline{SB}$	standby select	$\overline{RL}$	remote loopback	RS	RTS
		$\overline{SS}$	standby select		

Table 2a BAUD RATE GENERATOR CHARACTERISTICS 2449-1 (BRCLK=4.9152MHz)

MR23-20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	—	6144
0001	75	1.2	—	4096
0010	110	1.7598	−0.01	2793
0011	134.5	2.152	—	2284
0100	150	2.4	—	2048
0101	200	3.2	—	1536
0110	300	4.8	—	1024
0111	600	9.6	—	512
1000	1050	16.8329	0.196	292
1001	1200	19.2	—	256
1010	1800	28.7438	−0.19	171
1011	2000	31.9168	−0.26	154
1100	2400	38.4	—	128
1101	4800	76.8	—	64
1110	9600	153.6	—	32
1111	19200	307.2	—	16

Table 2b BAUD RATE GENERATOR CHARACTERISTICS 2449-2 (BRCLK=4.9152MHz)

MR23-20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	45.5	0.7279kHz	0.005	6752
0001	50	0.8	—	6144
0010	75	1.2	—	4096
0011	110	1.7598	−0.01	2793
0100	134.5	2.152	—	2284
0101	150	2.4	—	2048
0110	300	4.8	—	1024
0111	600	9.6	—	512
1000	1200	19.2	—	256
1001	1800	28.7438	−0.19	171
1010	2000	31.9168	−0.26	154
1011	2400	38.4	—	128
1100	4800	76.8	—	64
1101	9600	153.6	—	32
1110	19200	307.2	—	16
1111	38400	614.4	—	8

Table 2c BAUD RATE CHARACTERISTICS 2449-3 (BRCLK=5.0688MHz)

MR23-20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	—	6336
0001	75	1.2	—	4224
0010	110	1.76	—	2880
0011	134.5	2.1523	0.016	2355
0100	150	2.4	—	2112
0101	300	4.8	—	1056
0110	600	9.6	—	528
0111	1200	19.2	—	264
1000	1800	28.8	—	176
1001	2000	32.081	0.253	158
1010	2400	38.4	—	132
1011	3600	57.6	—	88
1100	4800	76.8	—	66
1101	7200	115.2	—	44
1110	9600	153.6	—	33
1111	19200	316.8	3.125	16

NOTE:
16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X and BRG can be used only for TxC.

COM 2449 OPERATION

The functional operation of the COM 2449 is programmed by a set of control words supplied by the processor. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the COM 2449 Programming section of this data sheet.

After programming, the COM 2449 is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the processor to a serial bit stream. These actions are accomplished within the framework specified by the control words.

Receiver

The COM 2449 is conditioned to receive data when the $\overline{RR}$ input is low and the RxEN bit in the command register is true. In the asynchronous mode, the receiver looks for a high to low (mark to space) transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and one stop bit have been assembled. The data is then transferred to the

COM 2449 INITIALIZATION FLOW CHART

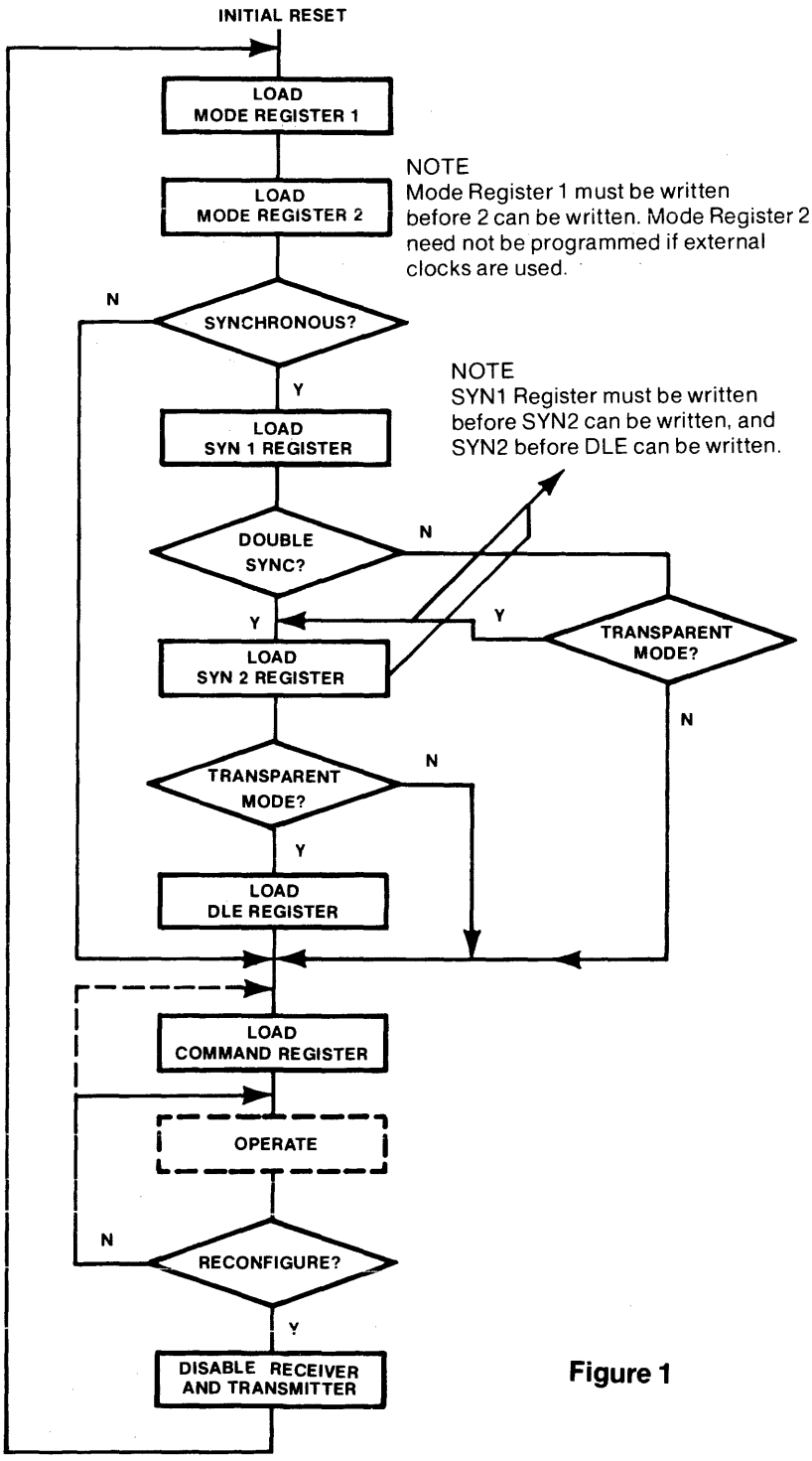


Figure 1

Receive Data Holding Register, the RxRDY bit in the status register is set, and the RxRDY output is asserted. If the character length is less than 8 bits, the high order unused bits in the Holding Register are set to zero. The Parity Error, Framing Error, and Overrun Error status bits are strobed into the status register on the positive going edge of RxC corresponding to the received character boundary. If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space as a start bit if it persists into the next bit time interval. If a break condition is detected (RxD is low for the entire character as well as the stop bit), only one character consisting of all zeros (with the Framing error status bit set) will be transferred to the Holding Register. The RxD input must return to a high condition before a search for the next start bit begins.

Pin 25 can be programmed to be a break detect output by appropriate setting of MR27-MR24. If so, a detected break will cause that pin to go high. When RxD returns to mark for one RxC time, pin 25 will go low. Refer to the break detection timing diagram.

When the COM 2449 is initialized into the synchronous mode, the receiver first enters the hunt mode on a 0 to 1 transition of RxEN (CR2). In this mode, as data is shifted into the Receiver Shift Register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly begins. If the single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the COM 2449 returns to the hunt mode. (Note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization). When synchronization has been achieved, the COM 2449 continues to assemble characters and transfers them to the Holding Register. The RxRDY status bit is set and the RxRDY output is asserted each time a character is assembled and transferred to the Holding Register. The Overrun error (OE) and Parity error (PE) status bits are set as appropriate. Further receipt of the proper SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the Holding Register. Note that the SYN characters used to establish initial synchronization are not transferred to the Holding Register in any case.

External jam synchronization can be achieved via pin 15 by appropriate setting of MR27-MR24. When pin 15 is an XSYNC input, the internal SYN1, SYN1-SYN2, and DLE-SYN1 detection is disabled. Each positive going signal on XSYNC will cause the receiver to establish synchronization on the rising edge of the next RxC pulse. Character assembly will start with the RxD input at this edge. XSYNC may be lowered on the next rising edge of RxC. This external synchronization will cause the SYN DETECT status bit to be set until the status register is read. Refer to XSYNC timing diagram.

Transmitter

The COM 2449 is conditioned to transmit data when the CS input is low and the TxEN command register bit is set. The COM 2449 indicates to the processor that it can accept a character for transmission by setting the TxRDY status bit and asserting the TxRDY output. When the processor writes a character into the Transmit Data Holding Register, the TxRDY status bit is reset and the TxRDY output is returned to a high (false) state. Data is transferred from the Holding Register to the Transmit Shift Register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the Transmit Holding Register, the TxD output remains in the marking (high) condition and the TxEMT/DSCHG output and its corresponding status bit are asserted. Transmission resumes when the processor loads a new character into the Holding Register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the Send Break command bit high.

In the synchronous mode, when the COM 2449 is initially conditioned to transmit, the TxD output remains high and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the processor. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity, if commanded) are generated by the COM 2449 unless the processor fails to send a new character to the COM 2449 by the time the transmitter has completed sending the previous character. Since synchronous communication does not allow gaps between characters, the COM 2449 asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, SYN1-SYN2 doublets, or DLE-SYN1 doublets, depending on the state of MR16 and MR17. Normal transmission of the message resumes when a new character is available in the Transmit Data Holding Register. If the SEND DLE bit in the command register is true, the DLE character is automatically transmitted prior to transmission of the message character in the transmit holding register.

COM 2449 PROGRAMMING

Prior to initiating data communications, the COM 2449 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The COM 2449 can be reconfigured at any time during program execution. A flow chart of the initialization process appears in Figure 1.

The internal registers of the COM 2449 are accessed by applying specific signals to the CE, R/W, A2, A1 and A0 inputs. The conditions necessary to address each register are shown in Table 5.

TABLE 5—COM 2449 REGISTER ADDRESSING

CE	A2	A1	A0	R/W	FUNCTION
1	X	X	X	X	Tri-state data bus
0	0	0	0	0	Read receive holding register
0	0	0	0	1	Write transmit holding register
0	0	0	1	0	Read status register 1
0	0	0	1	1	Write SYN1/SYN2/DLE registers
0	0	1	0	0	Read mode registers 1 and 2
0	0	1	0	1	Write mode registers 1 and 2
0	0	1	1	0	Read command register
0	0	1	1	1	Write command register
0	1	0	0	0	Read output register
0	1	0	0	1	Write output register
0	1	0	1	0	Read status register 2
					Write status register 2

NOTE
See AC Characteristics section for timing requirements.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions A2=0, A1=0, A0=1, and R/W=1. The first operation loads the SYN1 register. The next loads the SYN2 register, and the third loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses Mode Register 1, and a subsequent operation addresses Mode Register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 Register and Mode Register 1 by a RESET input or by performing a "Read Command Register" operation, but are unaffected by any other read or write operation.

The COM 2449 register formats are summarized in Tables 6, 7, 8, 9, 10 and 11. Mode Registers 1 and 2 define the general operational characteristics of the COM 2449, while the Command Register controls the operation within this basic framework. The COM 2449 indicates its status in the two Status Registers. The status registers are cleared when a RESET input is applied.

MODE REGISTER 1 (MR1)

Table 6 illustrates Mode Register 1. Bits MR11 and MR10 select the communication format and Baud rate multiplier. 00 specifies synchronous mode and 1X multiplier. 1X, 16X, and 64X multipliers are programmable for asynchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7, or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14.

In asynchronous mode, MR17 and MR16 select character framing of 1, 1.5, or 2 stop bits (if 1X baud rate is programmed, 1.5, stop bits defaults to 1 stop bits on transmit). In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17=1, and SYN1-SYN2 is used when MR17=0. If the transparent mode is specified by MR16, DLE-SYN1 is used for character fill and SYN Detect, but the normal synchronization sequence is used. When transmitting, a DLE character in the transmit holding register will cause a second DLE character to be transmitted. This DLE stuffing eliminates the software DLE compare and stuff on each transparent mode data character. If the send DLE command (CR3) is active when a DLE is loaded into THR, only one additional DLE will be transmitted. Also DLE stripping and DLE Detect (with MR14=0) are enabled.

TABLE 6—MODE REGISTER 1 (MR1)

MR17 MR16	MR15	MR14	MR13 MR12	MR11 MR10
Sync/Async	**Parity Type**	**Parity Control**	**Character Length**	**Mode and Baud Rate Factor**
ASYNCH: STOP BIT LENGTH 00=INVALID 01=1 STOP BIT 10=1½ STOP BITS 11=2 STOP BITS	0=ODD 1=EVEN	0=DISABLED 1=ENABLED	00=5 BITS 01=6 BITS 10=7 BITS 11=8 BITS	00=SYNCHRONOUS 1X RATE 01=ASYNCHRONOUS 1X RATE 10=ASYNCHRONOUS 16X RATE 11=ASYNCHRONOUS 64X RATE
SYNCH: NUMBER OF SYN CHAR 0=DOUBLE SYN 1=SINGLE SYN	**SYNCH: TRANSPARENCY CONTROL** 0=NORMAL 1=TRANSPARENT			

NOTE Baud rate factor in asynchronous applies only if external clock is selected. Factor is 15X if internal clock is selected. Mode must be selected (MR11, MR10) in any case.

MODE REGISTER 2 (MR2)

Table 7 illustrates mode register 2 (MR23, MR22, MR21 and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable for each COM 2449 version (-1, -2, -3). Version 1 and 2 specify a 4.9152 MHz TTL input at BRCLK (pin 20); version 3 specifies a 5.0688 MHz input which is identical to the COM 2651 and COM 2661-3. MR23-20 are don't cares if external clocks are selected (MR25-24=0). The individual rates are given in table 2a, b and c.

MR24-MR27 select the receive and transmit clock source (either the BRG or an external input) and the function at pins 15 and 32. Refer to table 7.

TABLE 7—MODE REGISTER 2 (MR2)

MR-27-MR24											MR23-MR20
	TxC	RxC	Pin 15	Pin 32		TxC	RxC	Pin 15	Pin 32	Mode	Baud Rate Selection
0000	E	E	TxC	RxC	1000	E	E	XSYNC[1]	RxC/TxC	sync	
0001	E	I	TxC	1X	1001	E	I	TxC	BKDET	async	
0010	I	E	1X	RxC	1010	I	E	XSYNC[1]	RxC	sync	
0011	I	I	1X	1X	1011	I	I	1X	BKDET	async	See baud rates in table 2
0100	E	E	TxC	RxC	1100	E	E	XSYNC[1]	RxC/TxC	sync	
0101	E	I	TxC	16X	1101	E	I	TxC	BKDET	async	
0110	I	E	16X	RxC	1110	I	E	XSYNC[1]	RxC	sync	
0111	I	I	16X	16X	1111	I	I	16X	BKDET	async	

NOTES
1. When pin 15 is programmed as XSYNC input, SYN1, SYN1-SYN2, and DLE-SYN1 detection is disabled.

E=External clock
I=Internal clock (BRG)
1X and 16X are clock outputs

COMMAND REGISTER (CR)

Table 8 illustrates the Command Register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. A 0 to 1 transition of CR2 forces start bit search (async mode) or hunt mode (sync mode) on the second RxC rising edge. Disabling the receiver causes RxRDY to go high (inactive). If the transmitter is disabled, it will complete the transmission of the character in the Transmit Shift Register (if any) prior to terminating operation. The TxD output will then remain in the marking state (high while the TxRDY and TxEMT will go high (inactive). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected. Bits CR1 (TR) and CR5 (RS) control the TR and RS outputs. Data at the outputs are the logical complement of the register data.

In asynchronous mode, setting CR3 will force and hold the TxD output low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go high for at least one bit time before beginning transmission of the next character in the Transmit Data Holding Register. In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the Transmit Data Holding Register. Since this is a one time command, CR3 does not have to be reset by software. CR3 should be set when entering and exiting transparent mode and for all DLE—non-DLE character sequences.

Setting CR4 causes the error flags in the Status Register 1 (SR13, SR14, and SR15) to be cleared. This is a one time command. There is no internal latch for this bit. When CR5 (RS) is set, the RS pin is forced low and the transmit serial logic is enabled. A 1 to 0 transition of CR5 will cause RS to go high (inactive) one TxC time after the last serial bit has been transmitted (if the transmit shift register was not empty).

The COM 2449 can operate in one of four sub-modes within each major mode (synchronous or asynchronous). The operational sub-mode is determined by CR7 and CR6. CR7-CR6=00 is the normal mode, with the transmitter and receiver operating independently in accordance with the Mode and Status Register instructions.

In asynchronous mode, CR7-CR6=01 places the COM 2449 in the Automatic Echo mode. Clocked, regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2=1), but the transmitter need not be enabled. Processor to receiver communications continue normally, but the processor to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in Automatic Echo mode:

1. Data assembled by the receiver are automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. TxRDY output=1.
4. The TxEMT/DSCHG pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In synchronous mode, CR7-CR6=01 places the COM 2449 in the Automatic SYN/DLE Stripping mode. The exact action taken depends on the setting of bits MR17 and MR16:

1. In the non-transparent, single SYN mode (MR17-MR16=10), characters in the data stream matching SYN1 are not transferred to the Receive Data Holding Register (RHR).
2. In the non-transparent, double SYN mode (MR17-MR16=00), characters in the data stream matching SYN1, or SYN2 if immediately preceded by SYN1, are not transferred to the RHR.
3. In transparent mode (MR16=1), characters in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However, only the first DLE of a DLE-DLE pair is stripped.

Note that Automatic Stripping mode does not affect the setting of the DLE Detect and SYN Detect status bits (SR13 and SR15).

Two diagnostic sub-modes can also be configured. In Local Loop Back mode (CR7-CR6=10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.
2. TR is connected to RR and RS is connected to CS.
3. The receiver is clocked by the transmit clock.
4. The TR, RS and TxD outputs are held high.
5. The CS, RR, DM and RxD inputs are ignored.

Additional requirements to operate in the Local Loop Back mode are that CR0 (TxEN), CR1 (TR), and CR5 (RS) must be set to 1. CR2 (RxEN) is ignored by the COM 2449.

The second diagnostic mode is the Remote Loop Back mode (CR7-CR6=11). In this mode:

1. Data assembled by the receiver is automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. No data are sent to the local processor, but the error status conditions (PE, OE, FE) are set.
4. The RxRDY, TxRDY, and TxEMT/DSCHG outputs are held high.
5. CR1 (TxEN) is ignored.
6. All other signals operate normally.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode		Request to Send	Reset Error	Sync/Async	Receive Control (RxEN)	Terminal Ready	Transmit Control (TxEN)
00=NORMAL OPERATION 01=ASYNCH: AUTOMATIC ECHO MODE SYNCH: SYN AND/OR DLE STRIPPING MODE 10=LOCAL LOOP BACK REMOTE LOOP BACK		0=FORCE RS OUTPUT HIGH ONE CLOCK TIME AFTER TxSR SERIALIZATION 1=FORCE RS OUTPUT LOW	0=NORMAL 1=RESET ERROR FLAG IN STATUS (FE, OE, PE/DLE DETECT)	ASYNCH: FORCE BREAK 0=NORMAL 1=FORCE BREAK SYNCH: SEND DLE 0=NORMAL 1=SEND DLE	0=DISABLE 1=ENABLE	0=FORCE TR OUTPUT HIGH 1=FORCE TR OUTPUT LOW	0=DISABLE 1=ENABLE

TABLE 8—COMMAND REGISTER (CR)

STATUS REGISTER 1 (SR1)

The data contained in the Status Register 1 (as shown in Table 9) indicate receiver and transmitter conditions and modem/data set status.

SR10 is the Transmitter Ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to 0, it indicates that the Transmit Data Holding Register has been loaded by the processor and the data has not been transferred to the Transmit Shift Register. If set equal to 1, it indicates that the Holding Register is ready to accept data from the processor. This bit is initially set when the Transmitter is enabled by CR0, unless a character has previously been loaded into the Holding Register. It is not set when the Automatic Echo or Remote Loop Back modes are programmed. When this bit is set, the $\overline{\text{TxRDY}}$ output pin is low. In the Automatic Echo and Remote Loop Back modes, the output is held high.

SR11, the Receiver Ready (RxRDY) status bit, indicates the condition of the Receive Data Holding Register. If set,it indicates that a character has been loaded into the Holding Register from the Receive Shift Register and is ready to be read by the processor. If equal to zero, there is no new character in the Holding Register. This bit is cleared when the processor reads the Receive Data Holding Register or when the receiver is disabled by CR2. When set, the $\overline{\text{RxRDY}}$ output is low.

The TxEMT/DSCHG bit, SR12, when set, indicates a change of state of the $\overline{\text{DM}}$ or $\overline{\text{RR}}$ inputs (when CR2 or CR0 = 1), the $\overline{\text{SI}}$, $\overline{\text{SB}}$, $\overline{\text{SQ}}$, $\overline{\text{TM}}$ or $\overline{\text{IC}}$ inputs (when SR25, SR26, or SR27=1) or that the Transmit Shift Register has completed transmission of a character and no new character has been loaded into the Transmit Data Holding Register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. TxEMT will not go active until at least one character has been transmitted. It is cleared by loading the Transmit Data Holding Register. The DSCHG condition is enabled when TxEN=1 or RxEN=1. It is cleared when status register 1 is read by the processor. If status register 1 is read twice and SR12=1 while SR16 and SR17 remain unchanged, then a TxEMT condition exists. When SR12 is set, the $\overline{\text{TxEMT/DSCHG}}$ output is low.

SR13, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16=1), with parity disabled, it indicates that a character matching the DLE Register has been received, and the present character is neither SYN1 nor DLE. This bit is cleared when the next character following the above sequence is loaded into the Receive Data Holding Register, when the receiver is disabled, or by a reset error command, CR4.

The Overrun Error status bit, SR14, indicates that the previous character loaded into the Receive Holding Register was not read by the processor at the time a new received character was transferred into it. This bit is cleared when the receiver is disabled and by the Reset Error command, CR4.

In asynchronous mode, bit SR15 signifies that the received character was not framed by a stop bit, i.e., only the first stop bit is checked. If the RHR contains all 0's when SR15=1, a break condition is present. In synchronous non-transparent mode (MR16=0), it indicates receipt of the SYN1 character in single SYN mode or the SYN1-SYN2 pair in double SYN mode. In synchronous transparent mode (MR16=1), this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1-SYN2) and, after synchronization has been achieved, when a DLE-SYN1 pair is received. The bit is reset when the receiver is disabled, when the Reset Error command is given in asynchronous mode, or when Status Register 1 is read by the processor in the synchronous mode.

SR16 and SR17 reflect the conditions of the $\overline{\text{RR}}$ and $\overline{\text{DM}}$ inputs respectively. A low input sets the corresponding status bit and a high input clears it.

SR17	SR16	SR15	SR14	SR13	SR12	SR11	SR10
Data Mode	**Receiver Ready**	**FE/SYN Detect**	**Overrun**	**PE/DLE Detect**	**TxEMT/DSCHG**	**RxRDY**	**TxRDY**
0=$\overline{\text{DM}}$ INPUT IS HIGH 1=$\overline{\text{DM}}$ INPUT IS LOW	0=$\overline{\text{RR}}$ INPUT IS HIGH 1=$\overline{\text{RR}}$ INPUT IS LOW	**ASYNCH:** 0=NORMAL 1=FRAMING ERROR **SYNCH:** 0=NORMAL 1=SYN CHAR DETECTED	0=NORMAL 1=OVERRUN ERROR	**ASYNCH:** 0=NORMAL 1=PARITY ERROR **SYNCH:** 0=NORMAL 1=PARITY ERROR OR DLE CHAR RECEIVED	0=NORMAL 1=CHANGE IN $\overline{\text{DSR}}$ OR $\overline{\text{DCD}}$, OR TRANSMIT SHIFT REGISTER IS EMPTY	0=RECEIVE HOLDING REG EMPTY 1=RECEIVE HOLDING REG HAS DATA	0=TRANSMIT HOLDING REG BUSY 1=TRANSMIT HOLDING REG EMPTY

TABLE 9—STATUS REGISTER 1 (SR1)

STATUS REGISTER 2 (SR2)

The Data contained in the 5 least significant bits (SR20 to SR24) reflect the conditions of the $\overline{IC}$, $\overline{TM}$, $\overline{SQ}$, $\overline{SB}$ and $\overline{SI}$ inputs respectively. A low input sets the corresponding status bit high and a high input clears the corresponding status bit low. These 5 bits or read only.

The three most significant bits (SR25 to SR27) allow interrupts to be enabled on the 5 inputs reflected in SR20 to SR24.

Setting SR25 enables an interrupt to occur when the $\overline{IC}$ input signal experiences a change of state. Setting SR26 enables an interrupt to occur when the $\overline{TM}$ input signal experiences a change of state. Setting SR27 enables an interrupt to occur when the $\overline{SQ}$, $\overline{SI}$, or $\overline{SB}$ input signals experience a change of state. All interrupts enabled in these 3 bits will be reflected in the $\overline{DSCHG/TxEMT}$ output signal and its corresponding status bit (SR12). These 3 bits can be read as well as written according to Table 5. Table 10 illustrates bit assignments of Status Register 2.

SR27 Interrupt Enable 1	SR26 Interrupt Enable 2	SR25 Interrupt Enable 3	SR24 Signal Rate Indication	SR23 Standby Indicator	SR22 Signal Quality	SR21 Test Mode	SR20 Incoming Call
1=INTERRUPT ON SQ, SI, SB STATE CHANGE	1=INTERRUPT ON TM STATE CHANGE	1=INTERRUPT ON IC STATE CHANGE	0=$\overline{SI}$ INPUT IS HIGH 1=$\overline{SI}$ INPUT IS LOW	0=$\overline{SB}$ INPUT IS HIGH 1=$\overline{SB}$ INPUT IS LOW	0=$\overline{SQ}$ INPUT IS HIGH 1=$\overline{SQ}$ INPUT IS LOW	0=$\overline{TM}$ INPUT IS HIGH 1=$\overline{TM}$ INPUT IS LOW	0=$\overline{IC}$ INPUT IS HIGH 1=$\overline{IC}$ INPUT IS LOW

TABLE 10—STATUS REGISTER 2 (SR2)

OUTPUT REGISTER (OR)

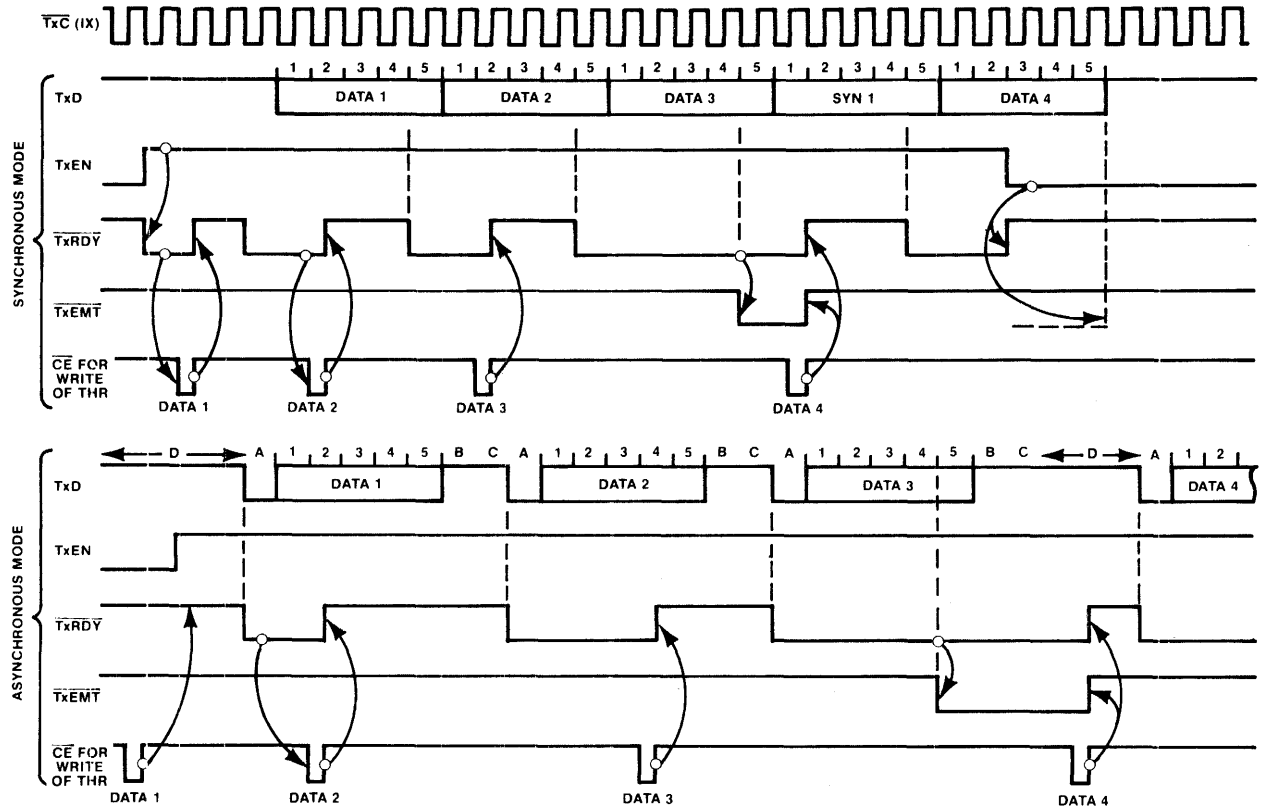
This 6 bit read write register (OR5-OR0) controls the 6 new output signals added to the COM2449. OR5-1 directly control the state of the $\overline{IS}$, $\overline{SF}$/SR, $\overline{SS}$, $\overline{RL}$, and $\overline{LL}$ respectively.

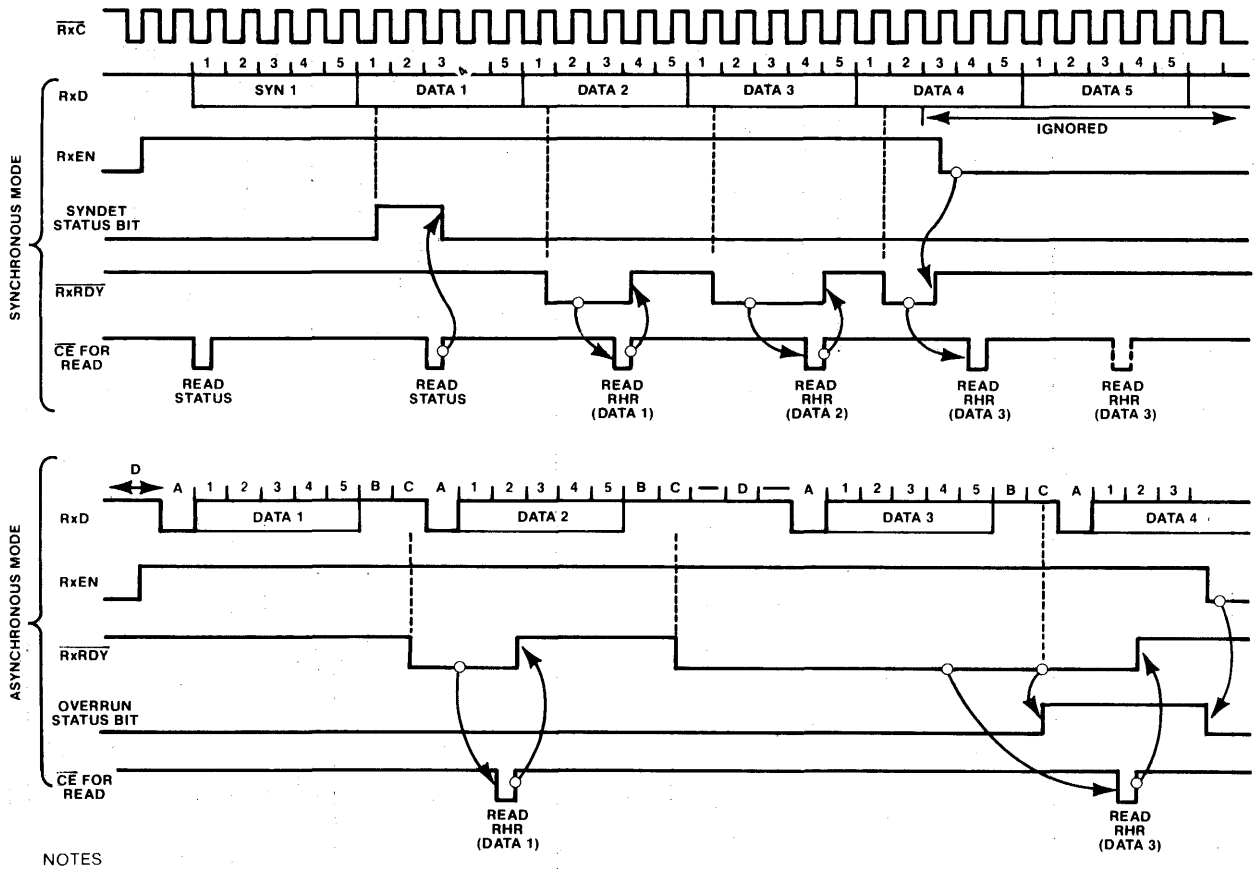
OR0 when set to a logic 1 will cause the $\overline{NS}$ output to become low. When OR0 is set to a logic 0 the $\overline{NS}$ output will not change until the $\overline{RR}$ input goes high.

Table 11 illustrates bit positions of the Output Register.

OR7	OR6	OR5	OR4	OR3	OR2	OR1	OR0
		Terminal in service	Select Frequency/ Signal rate select	Select Standby	Remote Loopback	Local Loopback	New Signal
DON'T CARE	DON'T CARE	0=$\overline{IS}$ OUTPUT GOES HIGH 1=$\overline{IS}$ OUTPUT GOES LOW	0=$\overline{SF}$/SR OUTPUT HIGH 1=$\overline{SF}$/SR OUTPUT LOW	0=$\overline{SS}$ OUTPUT HIGH 1=$\overline{SS}$ OUTPUT LOW	0=$\overline{RL}$ OUTPUT GOES HIGH 1=$\overline{RL}$ OUTPUT GOES LOW	0=$\overline{LL}$ OUTPUT GOES HIGH 1=$\overline{LL}$ OUTPUT GOES LOW	0=$\overline{NS}$ OUTPUT GOES HIGH ONLY WHEN $\overline{RR}$ INPUT GOES HIGH 1=$\overline{NS}$ OUTPUT GOES LOW

TABLE 11—OUTPUT REGISTER (OR)


TxC (IX)
SYNCHRONOUS MODE
TxD
TxEN
TxRDY
TxEMT
CE FOR WRITE OF THR
DATA 1
DATA 2
DATA 3
SYN 1
DATA 4
ASYNCHRONOUS MODE
D
A
B
C



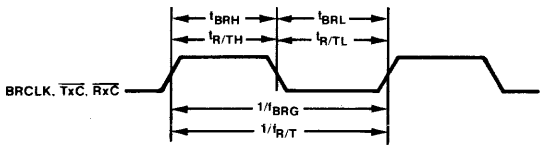
NOTES

A Start bit
B Stop bit 1
C Stop bit 2
D TxD marking condition

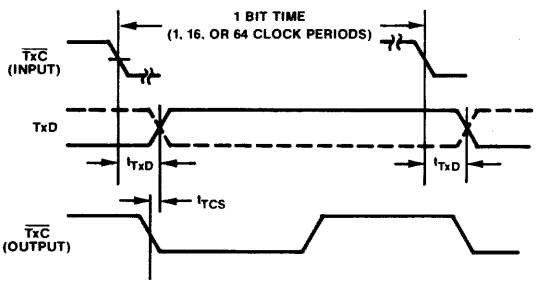
TIMING DIAGRAMS (Cont'd)

RESET

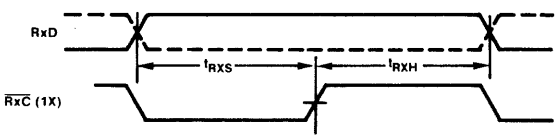
CLOCK



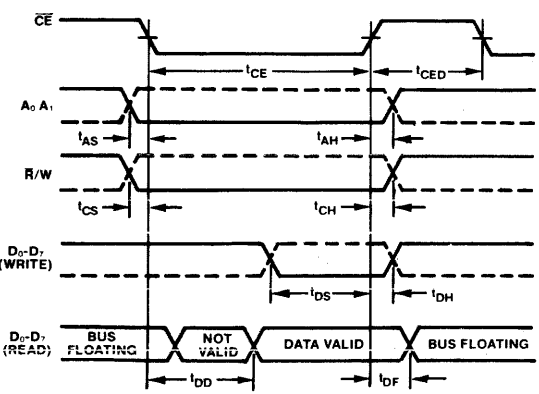
TRANSMIT



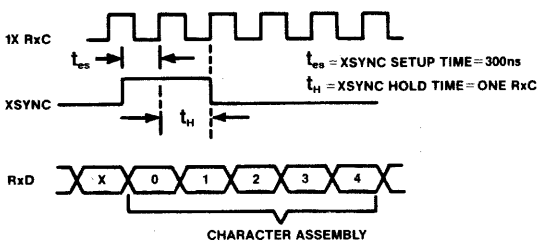
RECEIVE



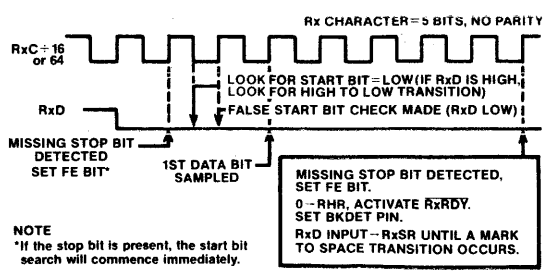
READ AND WRITE



EXTERNAL SYNCHRONIZATION WITH XSYNC



BREAK DETECTION TIMING



NOTE
*If the stop bit is present, the start bit search will commence immediately.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS T_A=0°C to +70°C, V_{CC}=5.0V±5%

	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
	Input voltage					
V_{IL}	Low			0.8	V	
V_{IH}	High	2.0				
	Output voltage					
V_{OL}	Low			0.4	V	I_{OL}=2.2mA
V_{OH}	High	2.4				I_{OH}=−400μA
I_{IL}	Input leakage current			10	μA	V_{IN}=0 to 5.5V
	Output leakage current					
I_{LH}	Data bus high			10	μA	V_O=4.0V
I_{LL}	Data bus low			10	μA	V_O=0.45V
I_{CC}	Power supply current			150	mA	
	Capacitance					
C_{IN}	Input			20	pF	fc=1MHz
C_{OUT}	Output			20	pF	Unmeasured pins tied
$C_{I/O}$	Input/Output			20	pF	to ground

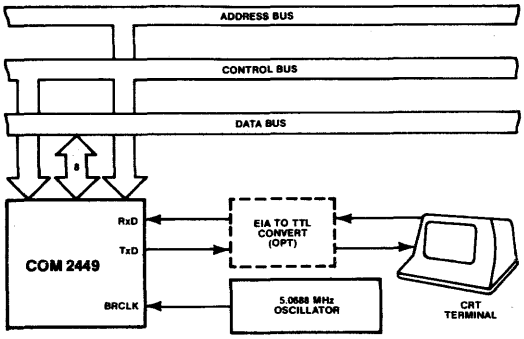
AC ELECTRICAL CHARACTERISTICS T_A=0°C to +70°C, V_{CC}=5.0V±5%

	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
	Pulse width					
t_{RES}	Reset	1000			ns	
t_{CE}	Chip enable	250			ns	
	Setup and hold time					
t_{AS}	Address setup	10			ns	
t_{AH}	Address hold	10			ns	
t_{CS}	R/W control setup	10			ns	
t_{CH}	R/W control hold	10			ns	
t_{DS}	Data setup for write	150			ns	
t_{DH}	Data hold for write	0			ns	
t_{RXS}	Rx data setup	300			ns	
t_{RXH}	Rx data hold	350			ns	
t_{DD}	Data delay time for read			200	ns	C_L=150pF
t_{DF}	Data bus floating time for read			100	ns	C_L=150pF
t_{CED}	CE to CE delay	600			ns	
	Input clock frequency					
f_{BRG}	Baud rate generator (2449-1, -2)	1.0	4.9152	4.9202	MHz	
f_{BRG}	Baud rate generator (2449-3)	1.0	5.0688	5.0738	MHz	
$f_{R,T}$[1]	TxC or RxC	dc		1.0	MHz	
	Clock width					
t_{BRH}	Baud rate high (2449-1, -2)	75				f_{BRG}=4.915MHz; measured at V_{IH}
t_{BRH}	Baud rate high (2449-3)	70				f_{BRG}=5.0688MHz; measured at V_{IH}
t_{BRL}	Baud rate low (2449-1, -2)	75				f_{BRG}=4.915MHz; measured at V_{IL}
t_{BRL}	Baud rate low (2449-3)	70				f_{BRG}=5.0688MHz; measured at V_{IL}
$t_{R,TH1}$	TxC or RxC high	480			ns	
$t_{R,TL}$	TxC or RxC low	480			ns	
t_{TXD}	TxD delay from falling edge of TxC			650	ns	C_L=150pF
t_{TCS}	Skew between TxD changing and falling edge of TxC output		0		ns	C_L=150pF

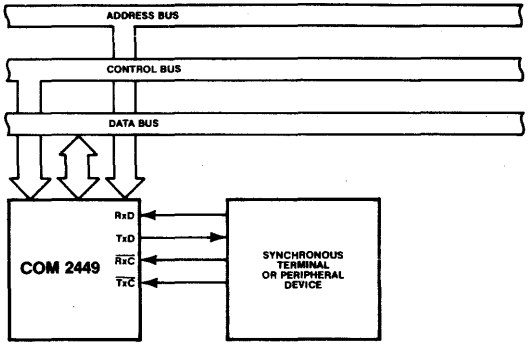
NOTE:
1. $f_{R,T}$ and $t_{R,TL}$ shown all modes except Local Loopback. For Local Loopback mode $f_{R,T}$=0.7MHz and $t_{R/TL}$=700ns min.

TYPICAL APPLICATIONS

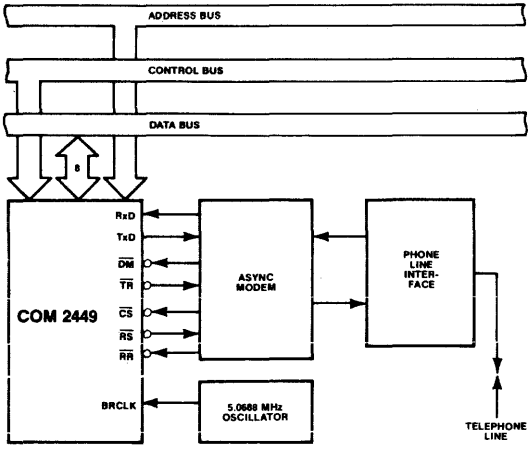
ASYNCHRONOUS INTERFACE TO CRT TERMINAL



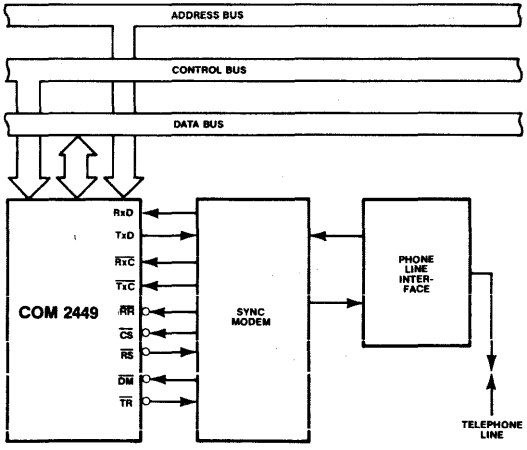
SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



ASYNCHRONOUS INTERFACE TO TELEPHONE LINES



SYNCHRONOUS INTERFACE TO TELEPHONE LINES



STANDARD MICROSYSTEMS CORPORATION

COM2601

Universal Synchronous Receiver/Transmitter USRT

FEATURES

- ☐ STR, BSC — Bi-sync and interleaved bi-sync modes of operation
- ☐ Fully Programmable — data word length, parity mode, receiver sync character, transmitter sync character
- ☐ Full or Half Duplex Operation — can receive and transmit simultaneously at different baud rates
- ☐ Fully Double Buffered — eliminates need for precise external timing
- ☐ Directly TTL Compatible — no interface components required
- ☐ Tri-State Data Outputs — bus structure oriented
- ☐ IBM Compatible — internally generated SCR and SCT signals
- ☐ High Speed Operation — 250K baud, 200ns strobes
- ☐ Low Power — 300mW
- ☐ Input Protected — eliminates handling problems
- ☐ Dip Package — easy board insertion

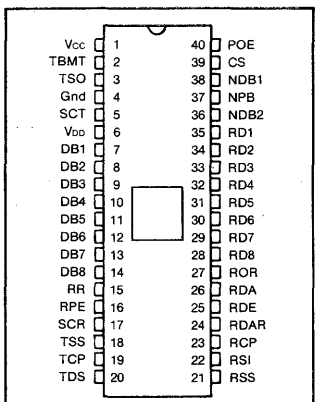
APPLICATIONS

- ☐ Bi-Sync Communications
- ☐ Cassette I/O
- ☐ Floppy Disk I/O

GENERAL DESCRIPTION

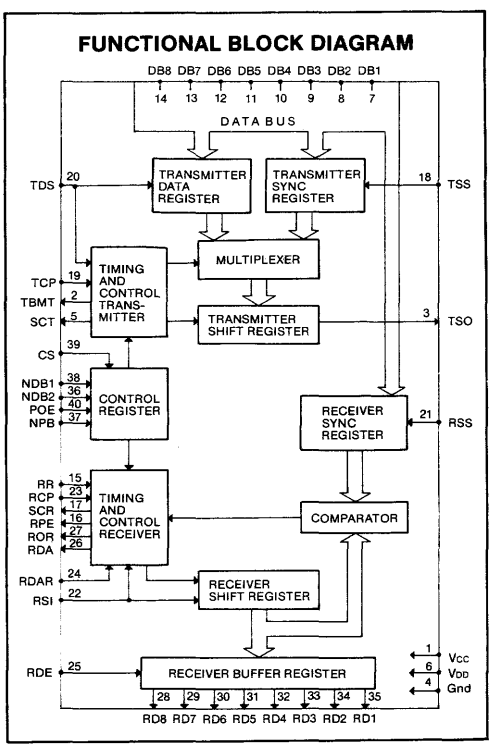
The Universal Synchronous Receiver/Transmitter is an MOS/LSI monolithic circuit that performs all the receiving and transmitting functions associated with synchronous (STR, BSC, Bi-sync, and interleaved bi-sync) data communications. This circuit is fabricated using SMC's P-channel low voltage oxide-nitride technology, allowing all inputs and outputs to be directly TTL compatible. The duplex mode, baud rate, data word length, parity mode, receiver sync character, and transmitter sync character are independently programmable through the use of external controls. The USR/T is fully double buffered and internally generates the sync character received and sync character transmitted signals. These programmable features provide the user with the ability to interface with all synchronous peripherals.

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
1	V_{CC}	Power Supply	+5 volt Supply
2	TBMT	Transmitter Buffer Empty	This output is at a high-level when the transmitter data buffer register may be loaded with new data.
3	TSO	Transmitter Serial Output	This output serially provides the entire transmitted character. This character is extracted from the transmitter data buffer register provided that a TDS pulse occurs during the presently transmitted character. If TDS is not pulsed, the next transmitted character will be extracted from the transmitter sync register.
4	GND	Ground	Ground
5	SCT	Sync Character Transmitted	This output is set high when the character loaded into the transmitter shift register is extracted from the transmitter sync register, indicating that the TDS was not pulsed during the previously transmitted character. This output is reset low when the character to be transmitted is extracted from the transmitter data buffer register. This can only occur if TDS is pulsed.
6	V_{DD}	Power Supply	−12 volt Supply
7-14	DB1-DB8	Data Bus Inputs	This 8 bit bus inputs information into the receiver sync register under control of the RSS strobe, into the transmitter sync register under control of the TSS strobe, and into the transmitter data buffer register under control of the TDS strobe. The strobes operate independently of each other. Unused bus inputs may be in either logic state. The LSB should always be placed on DB1.
15	RR	Receiver Reset	This input should be pulsed to a high-level after power turn-on. This resets the RDA, SCR, ROR, and RPE outputs to a low-level. The transition of the RR input from a high-level to a low-level sets the receiver into the search mode (bit phase). In the search mode the serially received data bit stream is examined on a bit by bit basis until a sync character is found. A sync character is found, by definition, when the contents of the receiver sync register and the receiver shift register are identical. When this occurs the SCR output is set high. This character is then loaded into the receiver buffer register and the receiver is set into the character mode. In this mode each character received is loaded into the receiver buffer register.
16	RPE	Receiver Parity Error	This output is a high-level if the received character parity bit does not agree with the selected parity.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
17	SCR	Sync Character Received	This output is set high each time the character loaded into the receiver buffer register is identical to the character in the receiver sync register. This output is reset low the next time the receiver buffer register is loaded with a character which is not a sync character.
18	TSS	Transmitter Sync Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the transmitter sync register.
19	TCP	Transmitter Clock	The positive going edge of this clock shifts data out of the transmitter shift register, at a baud rate equal to the TCP clock frequency.
20	TDS	Transmitter Data Buffer Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the transmitter data buffer register.
21	RSS	Receiver Sync Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the receiver sync register.
22	RSI	Receiver Serial Input	This input accepts the serial bit input stream.
23	RCP	Receiver Clock	The negative-going edge of this clock shifts data into the receiver shift register, at a baud rate equal to the RCP clock frequency.
24	RDAR	Receiver Data Available Reset	A high-level input resets the RDA output to a low-level.
25	RDE	Received Data Enable	A high-level input enables the outputs (RD8-RD1) of the receiver buffer register
26	RDA	Receiver Data Available	This output is at a high-level when an entire character has been received and transferred into the receiver buffer register.
27	ROR	Receiver Over-Run	This output is at a high-level if the previously received character is not read (RDA not reset) before the present character is transferred into the receiver buffer register.
28-35	RD8-RD1	Receiver Data Output	These are the 8 tri-state data outputs enabled by RDE. Unused data output lines, as selected by NDB1 and NDB2, have a low level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output.
36, 38	NDB2, NDB1	Number of Data Bits	These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table: NDB2 NDB1 data bits/character L L 5 L H 6 H L 7 H H 8

DESCRIPTION OF PIN FUNCTIONS

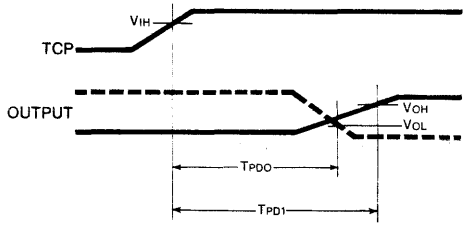
PIN NO.	SYMBOL	NAME	FUNCTION
37	NPB	No Parity Bit	A high-level input eliminates the parity bit from being transmitted. In addition, it is necessary that the received character contain no parity bit. Also, the RPE output is forced to a low-level. See pin 40, POE.
39	CS	Control Strobe	A high-level input enters the control bits (NDB1, NDB2, POE, and NPB) into the control bits register. This line may be strobed or hard wired to a high-level.
40	POE	Odd/Even Parity Select	The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the reciever and transmitter, as per the following table:

NPB	POE	MODE
L	L	odd parity
L	H	even parity
H	X	no parity

X = don't care

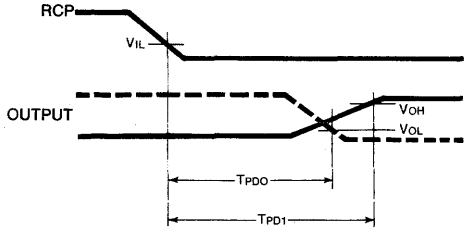
ADDITIONAL TIMING INFORMATION
(Typical Propagation Delays)

Transmitter

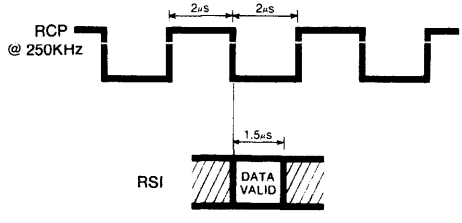


OUTPUT	TPDO	TPD1	UNITS
TBMT	NA	2.0	μs
SCT	1.0	1.5	μs
TSO	1.0	1.0	μs

Receiver



OUTPUT	TPDO	TPD1	UNITS
RDA	NA	1.0	μs
ROR	2.0	2.5	μs
RPE	2.0	2.5	μs
SCR	2.0	2.5	μs
RD1-RD8	2.5	2.5	μs



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, V_{CC} ..... +0.3V
Negative Voltage on any Pin, V_{CC} ..... −25 V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0° C to 70° C, V_{CC} = +5V ±5%, V_{DD} = −12V ±5%, unless otherwise noted)

Parameter	Min	Typ	Max	Unit	Conditions
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}	V_{DD}		0.8	V	
High-level, V_{IH}	V_{CC}-1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}		0.2	0.4	V	I_{OL} = 1.6mA
High-level, V_{OH}	2.4	4.0		V	I_{OH} = −100μA
INPUT CURRENT					
Low-level, I_{IL}			1.6	mA	see note 1
OUTPUT CURRENT					
Leakage, I_{LO}			−1	μA	RDE = V_{IL}, O ≤ V_{OUT} ≤ +5V
Short circuit, I_{OS}**			10	mA	V_{OUT} = 0V
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	V_{IN} = V_{CC}, f = 1MHz
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pf	R_{DE} = V_{IL}, f = 1MHz
POWER SUPPLY CURRENT					
I_{CC}			28	mA	All outputs = V_{OH}
I_{DD}			28	mA	All outputs = V_{OH}
A.C. CHARACTERISTICS					T_A = +25°C
CLOCK FREQUENCY	DC		250	KHz	RCP, TCP
PULSE WIDTH					
Clock	1			μs	RCP, TCP
Receiver reset	1			μs	RR
Control strobe	200			ns	CS
Transmitter data strobe	200			ns	TDS
Transmitter sync strobe	200			ns	TSS
Receiver sync strobe	200			ns	RSS
Receiver data available reset	200			ns	RDAR
INPUT SET-UP TIME					
Data bits	>0			ns	DB1-DB8
Control bits	>0			ns	NPB, NDB2, NDB1, POE
INPUT HOLD TIME					
Data bits	>0			ns	DB1-DB8
Control bits	>0			ns	NPB, NDB2, NDB1, POE
STROBE TO OUTPUT DELAY					Load = 20pf +1 TTL input
Receive data enable		180	250	ns	RDE: T_{PD1}, T_{PD0}
OUTPUT DISABLE DELAY		100	250	ns	RDE

**Not more than one output should be shorted at a time.

NOTES:
1. Under steady state condition no current flows for TTL or MOS interfacing. A switching current of 1.6 mA maximum flows during a transition of the input.
2. The three-state output has 3 states:
   1) low impedance to V_{CC}
   2) low impedance to GND
   3) high impedance OFF ≅ 10M ohms
   The OFF state is controlled by the RDE input.

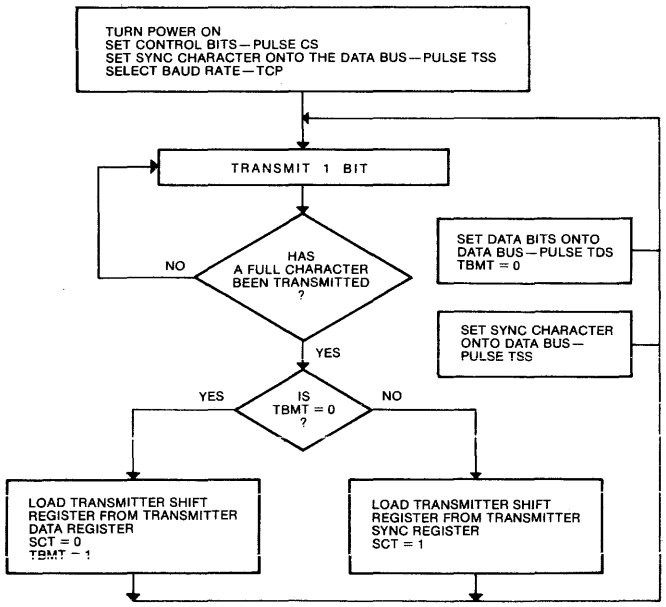
DESCRIPTION OF OPERATION—RECEIVER/TRANSMITTER

The input clock frequency for the receiver is set at the desired receiver baud rate and the desired receiver sync character (synchronous idle character) is loaded into the receiver sync register. When the Receiver Reset input transitions from a high-level to a low-level the receiver is set into the search mode (bit phase). In the search mode the serially received data bit stream is examined on a bit by bit basis until a sync character is found. A sync character is found, by definition, when the contents of the receiver sync register and the receiver shift register are identical. When this occurs the Sync Character Received output is set high. This character is then loaded into the receiver buffer register and the receiver is set into the character mode. In this mode each character received is loaded into the receiver buffer register. The receiver provides flags for Receiver Data Available, Receiver Over Run, Receiver Parity Error, and Sync Character Received. Full double buffering eliminates the need for precise external timing by allowing one full character time for received data to be read out.

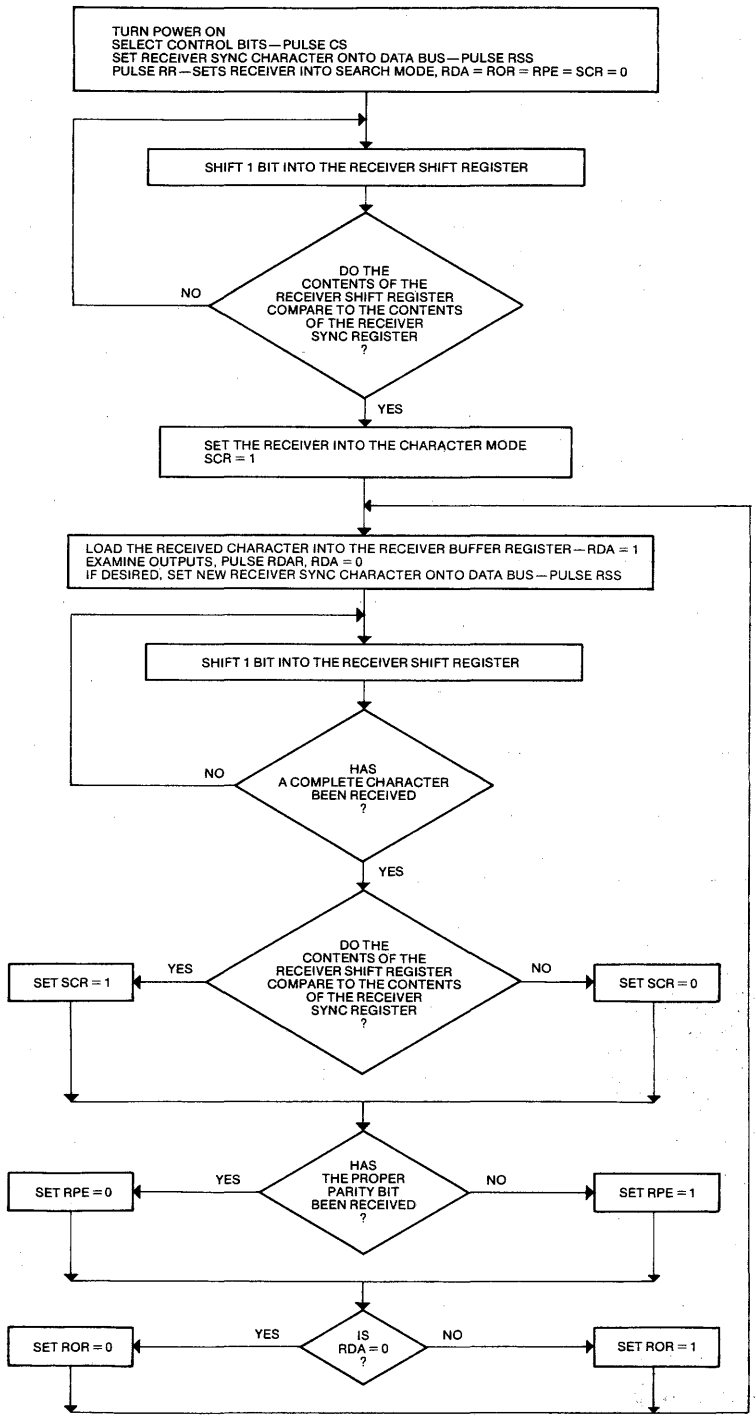
The input clock frequency for the transmitter is set at the desired baud rate and the desired transmitter sync character is loaded into the transmitter sync register. Internal logic decides if the character to be transmitted out of the transmitter shift register is extracted from the transmitter data register or the transmitter sync register. The next character transmitted is extracted from the transmitter data register provided that a Transmitter Data Strobe pulse occurs during the presently transmitted character. If the Transmitter Data Strobe is not pulsed, the next transmitted character is extracted from the transmitter sync register and the Sync Character Transmitted output is set to a high level. Full double buffering eliminates the need for precise external timing by allowing one full character time to load the next character to be transmitted.

There may be 5, 6, 7, or 8 data bits and odd/even or no parity bit. All inputs and outputs are directly TTL compatible. Tri-state data output levels are provided for the bus structure oriented signals. Input strobe widths of 200ns, output propagation delays of 250ns, and receiver/transmitter rates of 250K baud are achieved.

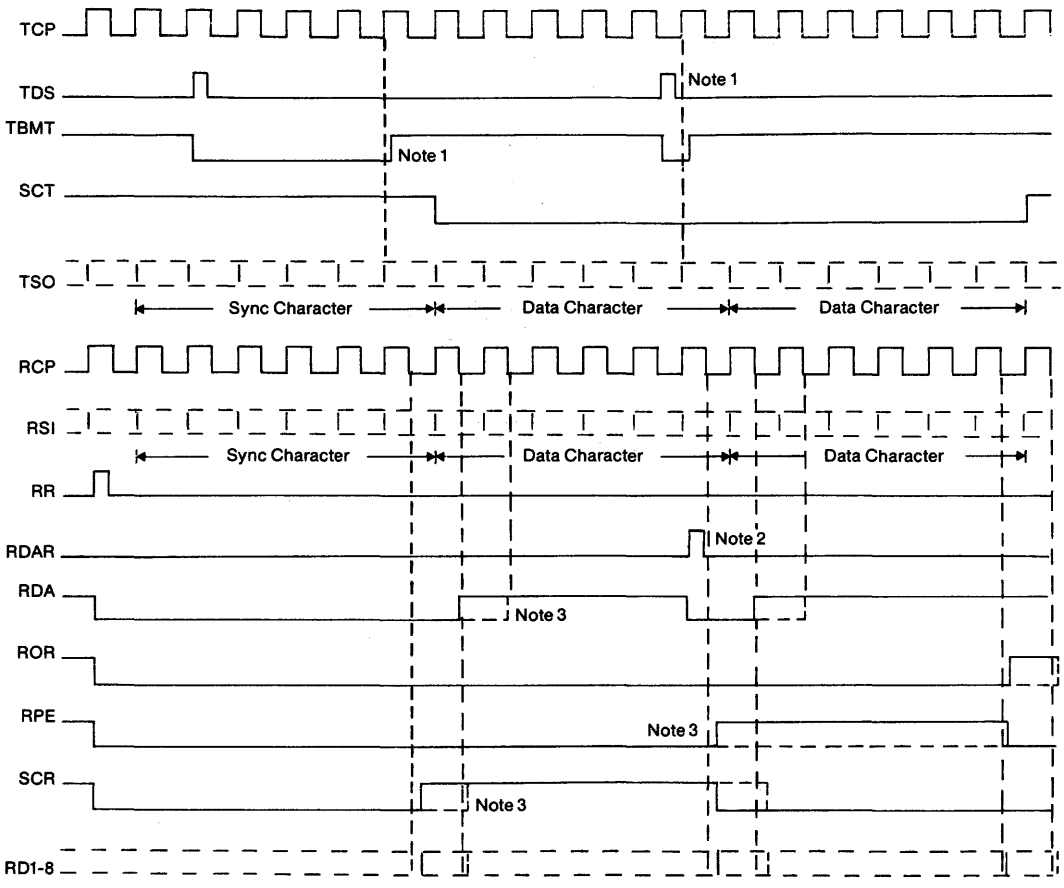
FLOW CHART—TRANSMITTER



FLOW CHART—RECEIVER



USRT TIMING DIAGRAM



NOTE 1
The transmitter shift register is loaded with the next character at the positive clock transition corresponding to the leading edge of the last bit of the current character on the TSO output. TBMT is set high approximately two microseconds after this clock transition. If it is desired that the next character be extracted from the transmitter data register the leading edge of the TDS should occur at least one microsecond prior to this clock transition.

NOTE 2
In order to avoid an ROR indication the leading edge of the RDAR pulse should occur at least one microsecond prior to the negative clock transition corresponding to the center of the first bit after the last data bit on the RSI input.

NOTE 3
The ROR, RPE, SCR and RD1-RD8 outputs are set to their correct levels approximately two microseconds after the negative clock transition corresponding to the center of the first bit after the last data bit on the RSI input. The RDA output is set high at the next negative clock transition.

The solid waveforms correspond to a control register setting of 5 data bits and a parity bit. The dashed waveforms are for a setting of 6 data bits and no parity bit.

STANDARD MICROSYSTEMS CORPORATION

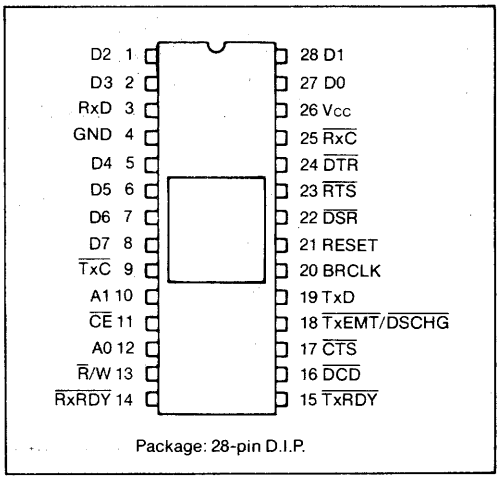
COM 2651
μPC FAMILY

Programmable Communication Interface PCI

FEATURES

- ☐ Synchronous and Asynchronous Full Duplex or Half Duplex Operations
- ☐ Re-programmable ROM on-chip baud rate generator
- ☐ Synchronous Mode Capabilities
  - —Selectable 5 to 8-Bit Characters
  - —Selectable 1 or 2 SYNC Characters
  - —Internal Character Synchronization
  - —Transparent or Non-Transparent Mode
  - —Automatic SYNC or DLE-SYNC Insertion
  - —SYNC or DLE Stripping
  - —Odd, Even, or No Parity
  - —Local or remote maintenance loop back mode
- ☐ Asynchronous Mode Capabilities
  - —Selectable 5 to 8-Bit Characters
  - —3 Selectable Clock Rates (1X, 16X, 64X the Baud Rate)
  - —Line Break Detection and Generation
  - —1, 1½, or 2-Stop Bit Detection and Generation
  - —False Start Bit Detection
  - —Odd, Even, or No Parity
  - —Parity, Overrun, and framing error detect
  - —Local or remote maintenance loop back mode
  - —Automatic serial echo mode
- ☐ Baud Rates
  - —DC to 1.0M Baud (Synchronous)
  - —DC to 1.0M Baud (1X, Asynchronous)
  - —DC to 62.5K Baud (16X, Asynchronous)
  - —DC to 15.625K Baud (64X, Asynchronous)
- ☐ Double Buffering of Data

PIN CONFIGURATION



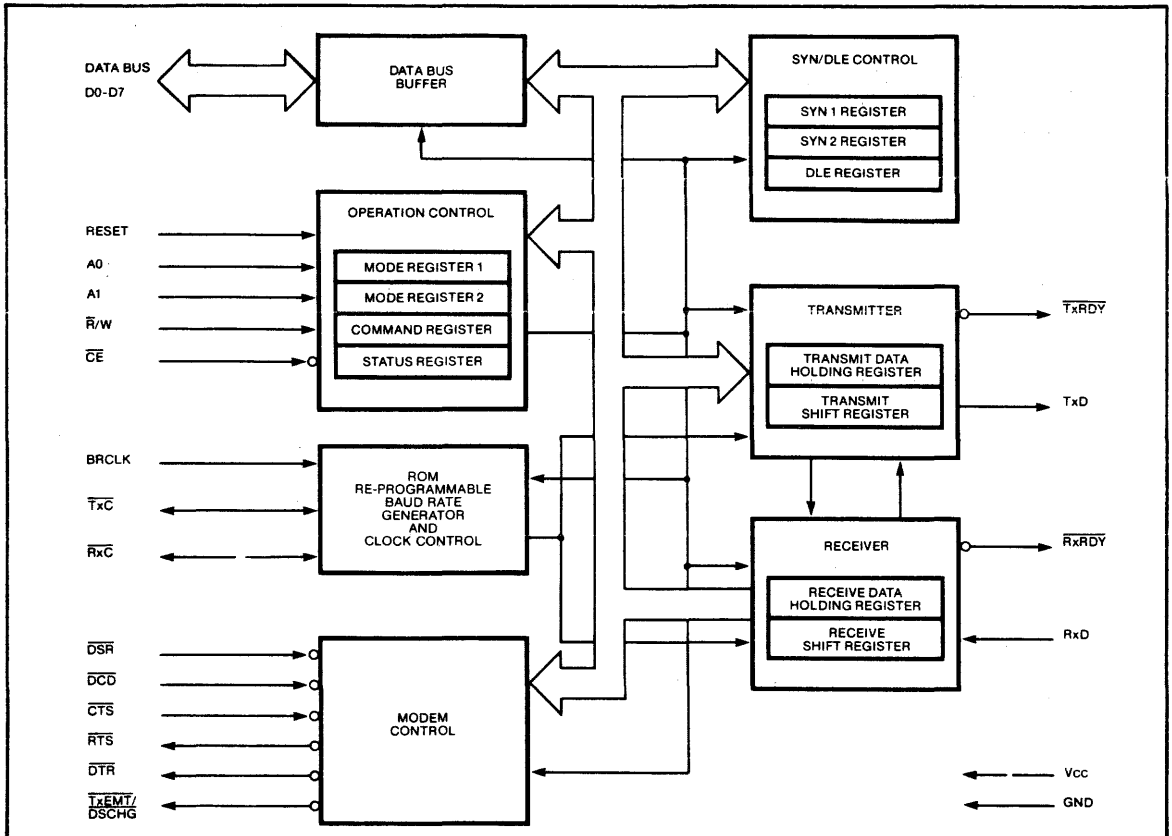
Package: 28-pin D.I.P.

- ☐ Internal or External Baud Rate Clock
  - —16 Internal Rates:50 to 19,200 Baud
- ☐ Single +5 volt Power Supply
- ☐ TTL Compatible
- ☐ No System Clock Required
- ☐ Compatible with 2651, INS2651

GENERAL DESCRIPTION

The COM 2651 is an MOS/LSI device fabricated using SMC's patented COPLAMOS® technology that meets the majority of asynchronous and synchronous data communication requirements, by interfacing parallel digital systems to asynchronous and synchronous data communication channels while requiring a minimum of processor overhead. The COM 2651 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. The on-chip baud rate generator can be ROM reprogrammed to accommodate different baud rates and different starting frequencies.

The COM 2651 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for microcomputer system data communications. The USART is used as a peripheral and is programmed by the processor to communicate in commonly used asynchronous and synchronous serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status including data format errors and control signals is available to the processor at any time.



COM 2651 ORGANIZATION

The COM 2651 is organized into 6 major sections. Communication between each section is achieved via an internal data and control bus. The data bus buffer allows a processor access to all internal registers on the COM 2651.

Operation Control

This functional block stores configuration and operation commands from the processor and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with a processor via the data bus and contains Mode Registers 1 and 2, the Command Register, and the Status Register. Details of register addressing and protocol are presented in the COM 2651 programming section of this specification.

Timing

The COM 2651 contains a Baud Rate Generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full duplex operation. Table 6 illustrates all available baud rates.

Receiver

The Receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and stores the "assembled" character in the receive data holding register until read by the processor.

Transmitter

The Transmitter accepts parallel data from the processor, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Modem Control

The modem control provides three output signals and accepts three input signals used for "handshaking" and status indication between the COM 2651 and a modem.

SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the processor. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

Interface Signals

The COM 2651 interface signals can be grouped into two types: the processor-related signals (shown in Table 2) which interface the COM 2651 to the processor, and the device-related signals (shown in Table 3), which are used to interface to the communications equipment.

TABLE 2—PROCESSOR RELATED SIGNALS

PIN NO.	NAME	SYMBOL	FUNCTION
1,2,5,6, 7,8,27,28	Data	D7-DØ	Bidirectional; 8 bit, three state data bus used to transfer commands, data and status between the COM 2651 and a processor. DØ is the least significant bit; D7 is the most significant bit.
10,12	Address	A1, AØ	Input; Address lines used to select COM 2651 registers.
11	Chip Enable	$\overline{CE}$	Input; when this signal is low, the operation specified by the $\overline{R}$/W, A1 and AØ will be performed. When this input is high, D7-Ø are in the high impedance state.
13	Read/Write	$\overline{R}$/W	Input; Processor read/write direction control. This signal defines the direction of the data bus D7-Ø when the COM 2651 is selected. D7-Ø drives out (read) when this signal is low and accepts data input when this signal is high. The input only has meaning when the chip enable input is active.
14	Receiver Ready	$\overline{RxRDY}$	Output; This signal is the complement of Status Register bit 1 (SR1). When low, it indicates that the Receive Data Holding Register (RHR) has a character ready for input to the processor. It goes high when the RHR is read by the processor, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the processor.
15	Transmitter Ready	$\overline{TxRDY}$	Output; This signal is the complement of Status Register bit 0 (SR0). When low, it indicates that the Transmit Data Holding Register (THR) is ready to accept a data character from the processor. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the processor.
18	Transmitter empty/data set change	$\overline{TxEMT}$/ $\overline{DSCHG}$	Output; This signal is the complement of Status Register bit 2 (SR2). When low, it indicates that the transmitter has completed serialization of the last character loaded by the processor, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This output goes high when the Status Register is read by the processor, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the processor for this line to go high. It is an open drain output which can be used as an interrupt to the processor.
21	Reset	Reset	Input; A high on this input performs a master reset on the COM 2651. This signal asynchronously terminates any device activity and clears the Mode, Command and Status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.
26	Supply Voltage	V_{CC}	+5 volts supply.
4	Ground	GND	Ground.

TABLE 3—DEVICE RELATED SIGNALS

PIN NO.	NAME	SYMBOL	FUNCTION
3	Receive Data	RxD	Input; Serial data to the receiver. "Mark" is high "space" is low.
9	Transmitter Clock	$\overline{TxC}$	Input or Output; If the external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X, the Baud rate as programmed by Mode Register 1. The transmitted data changes on the falling edge of the clock. If the internal transmitter clock is programmed, this pin becomes an output at 1X the programmed Baud rate.
16	Data Carrier Detect	$\overline{DCD}$	Input; This signal must be low in order for the receiver to function. The complement appears in the Status Register bit 6 (SR6). When this input changes state a low output on $\overline{TxEMT/DSCHG}$ occurs.
17	Clear to Send	$\overline{CTS}$	Input; This signal must be low in order for the transmitter to function. If it goes high during transmission, the character in the Transmit Shift Register will be transmitted before termination.
19	Transmit Data	TxD	Output; Serial data from the transmitter. "Mark" is high, "Space" is low. This signal is held in the "Mark" condition when the transmitter is disabled.
20	Baud Rate Clock	BRCLK	Input; The standard device requires a 5.0688MHz clock to the internal Baud rate generator allowing for Baud rate shown in Table 6. The reprogrammable ROM on chip allows for user specificed Baud rates and input frequency. Consult the factory for details. This input is not required if external receive and transmit clocks are used.
22	Data Set Ready	$\overline{DSR}$	Input; This general purpose signal can be used for Data Set Ready or Ring Indicator condition. Its complement appears as Status Register bit 7 (SR7). When this input changes state, a low output on $\overline{TxEMT/DSCHG}$ occurs.
23	Request to Send	$\overline{RTS}$	Output; This general purpose signal is the complement of the Command Register bit 5 (CR5). It is normally used to indicate Request to Send.

TABLE 3—DEVICE RELATED SIGNALS

PIN NO.	NAME	SYMBOL	FUNCTION
24	Data Terminal	$\overline{DTR}$	Output; This general purpose signal is the complement of the Command Register bit 1 (CR1). It is normally used to indicate Data Terminal Ready.
25	Receive Clock	$\overline{RxC}$	Input or Output; If the external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X, or 64X the Baud rate, as programmed by Mode Register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin becomes an output at 1X the programmed Baud rate.

COM 2651 OPERATION

The functional operation of the COM2651 is programmed by a set of control words supplied by the processor. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the COM 2651 Programming section of this data sheet.

After programming, the COM 2651 is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the processor to a serial bit stream. These actions are accomplished within the framework specificed by the control words.

Receiver

The COM 2651 is conditioned to receive data when the $\overline{DCD}$ input is low and the RxEN bit in the command register is true. In the asynchronous mode, the receiver looks for a high to low transition on the RxD input line indicating the start bit. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and the stop bit(s) have been assembled. The data is then transferred to the Receive Data Holding Register, the RxRDY bit in the status register is set, and the $\overline{RxRDY}$ output is asserted. If the character length is less than 8 bits, the high order unused bits in the Holding Register are set to zero. The Parity Error, Framing Error, and Overrun Error status bits are strobed into the status register on the positive going edge of $\overline{RxC}$ corresponding to the received character boundary. If a break condition is detected (RxD is low for the entire character as well as the stop bit[s]), only one character consisting of all zeros (with the Framing error status bit set) will be transferred to the Holding Register. The RxD input must return to a high condition before a search for the next start bit begins.

When the COM 2651 is initialized into the synchronous mode, the receiver first enters the hunt mode on a 0 to 1 transition of RxEN (CR2). In this mode, as data is shifted into the Reciver Shift Register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly begins. If the single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the COM 2651 returns to the hunt mode. (Note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization). When synchronization has been achieved, the COM 2651 continues to assemble characters and transfers them to the Holding Register. The RxRDY status bit is set and the $\overline{RxRDY}$ output is asserted each time a character is assembled and transferred to the Holding Register. The Overrun error (OE) and Parity error (PE) status bits are set as appropriate. Further receipt of the proper SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the Holding Register. Note that the SYN characters used to establish initial synchronization are not transferred to the Holding Register in any case.

Transmitter

The COM 2651 is conditioned to transmit data when the $\overline{CTS}$ input is low and the TxEN command register bit is set. The COM 2651 indicates to the processor that it can accept a character for transmission by setting the TxRDY status bit and asserting the $\overline{TxRDY}$ output. When the processor writes a character into the Transmit Data Holding Register, the TxRDY status bit is reset and the $\overline{TxRDY}$ output is returned to a high (false) state. Data is transferred from the Holding Register to the Transmit Shift Register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the Transmit Holding Register, the TxD output remains in the marking (high) condition and the $\overline{TxEMT/DSCHG}$ output and its corresponding status bit are asserted. Transmission resumes when the processor loads a new character into the Holding Register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the Send Break command bit high.

In the synchronous mode, when the COM 2651 is initially conditioned to transmit, the TxD output remains high and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the processor. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity, if commanded) are generated by the COM 2651 unless the processor fails to send a new character to the COM 2651 by the time the transmitter has completed sending the previous character. Since synchronous communication does not allow gaps between characters, the COM 2651

asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, SYN1-SYN2 doublets, or DLE-SYN1 doublets, depending on the state of MR16 and MR17. Normal transmission of the message resumes when a new character is available in the Transmit Data Holding Register. If the SEND DLE bit in the command register is true, the DLE character is automatically transmitted prior to transmission of the message character in the transmit holding register.

COM 2651 PROGRAMMING

Prior to initiating data communications, the COM 2651 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The COM 2651 can be reconfigured at any time during program execution. However, if the change has an effect on the reception of a character the receiver should be disabled. Alternatively if the change is made 1½ $\overline{RxC}$ periods after RxRDY goes active it will affect the next character assembly. A flowchart of the initialization process appears in Figure 1.

The internal registers of the COM 2651 are accessed by applying specific signals to the $\overline{CE}$, $\overline{R}/W$, A1 and A0 inputs. The conditions necessary to address each register are shown in Table 4.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions A1=0, A0=1, and $\overline{R}/W$=1. The first operation loads the SYN1 register. The next loads the SYN2 register, and the third loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses Mode Register 1, and a subsequent operation addresses Mode Register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 Register and Mode Register 1 by a RESET input or by performing a "Read Command Register" operation, but are unaffected by any other read or write operation.

The COM 2651 register formats are summarized in Tables 5, 6, 7 and 8. Mode Registers 1 and 2 define the general operational characteristics of the COM 2651, while the Command Register controls the operation within this basic framework. The COM 2651 indicates its status in the Status Register. These registers are cleared when a RESET input is applied.

COM 2651 INITIALIZATION FLOW CHART

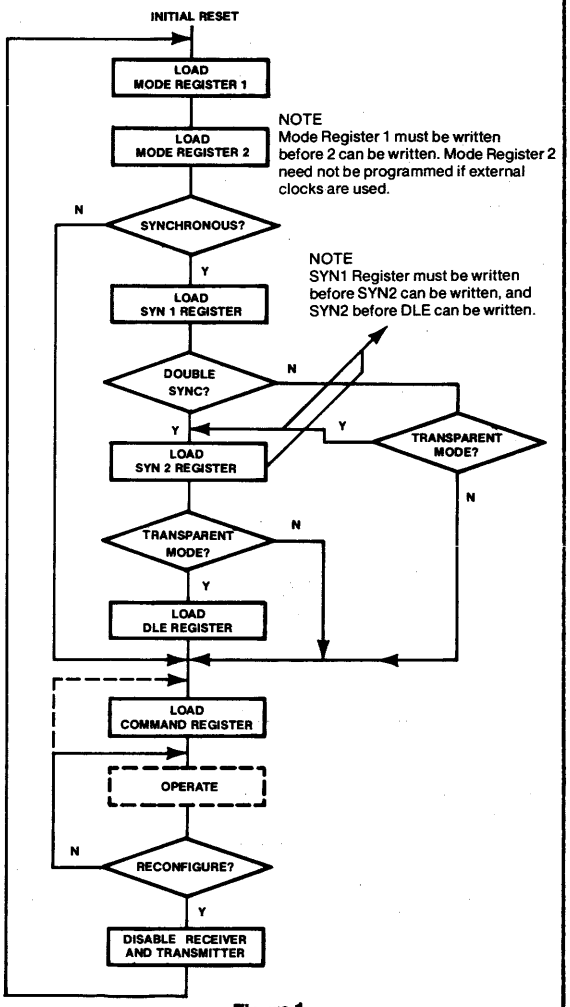


Figure 1

$\overline{CE}$	A1	A0	$\overline{R}/W$	FUNCTION
1	X	X	X	Tri-state data bus
0	0	0	0	Read receive holding register
0	0	0	1	Write transmit holding register
0	0	1	0	Read status register
0	0	1	1	Write SYN1/SYN2/DLE registers
0	1	0	0	Read mode registers 1 and 2
0	1	0	1	Write mode registers 1 and 2
0	1	1	0	Read command register
0	1	1	1	Write command register

NOTE
See AC Characteristics section for timing requirements.

Table 4—COM 2651 REGISTER ADDRESSING

MODE REGISTER 1 (MR1)

Table 5 illustrates Mode Register 1. Bits MR11 and MR10 select the communication format and Baud rate multiplier. 00 specifies synchronous mode and 1X multiplier. 1X, 16X, and 64X multipliers are programmable for asynchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7, or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14.

In asychronous mode, MR17 and MR16 select character framing of 1, 1.5, or 2 stop bits. (if 1X baud rate is programmed, 1.5, stop bits defaults to 1 stop bits on transmit). In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17=1, and SYN1-SYN2 is used when MR17=0. If the transparent mode is specified by MR16, DLE-SYN1 is used for character fill and SYN Detect, but the normal synchronization sequence is used. Also DLE stripping and DLE Detect (with MR14=0) are enabled.

MR17	MR16	MR15	MR14	MR13	MR12	MR11	MR10
Sync/Async		Parity Type	Parity Control	Character Length		Mode and Baud Rate Factor	
ASYNCH: STOP BIT LENGTH 00=INVALID 01=1 STOP BIT 10=1½ STOP BITS 11=2 STOP BITS		0=ODD 1=EVEN	0=DISABLED 1=ENABLED	00=5 BITS 01=6 BITS 10=7 BITS 11=8 BITS		00=SYNCHRONOUS 1X RATE 01=ASYNCHRONOUS 1X RATE 10=ASYNCHRONOUS 16X RATE 11=ASYNCHRONOUS 64X RATE	
SYNCH: NUMBER OF SYN CHAR 0=DOUBLE SYN 1=SINGLE SYN	**SYNCH: TRANSPARENCY CONTROL** 0=NORMAL 1=TRANSPARENT						

NOTE Baud rate factor in asynchronous applies only if external clock is selected. Factor is 16X if internal clock is selected. Mode must be selected (MR11, MR10) in any case.

TABLE 5—MODE REGISTER 1 (MR1)

MODE REGISTER 2 (MR2)

Table 6 illustrates Mode Register 2. MR23, MR22, MR21, and MR20 control the frequency of the internal Baud rate generator (BRG). Sixteen rates are selectable. When driven by a 5.0688 MHz input at the BRCLK input (pin 20), the BRG output has zero error except at 134.5, 2000, and 19,200 Baud, which have errors of +0.016% +0.253%, and +3.125% respectively.

MR25 and MR24 select either the BRG or the external inputs $\overline{TxC}$ and $\overline{RxC}$ as the clock source for the transmitter and receiver, respectively. If the BRG clock is selected, the Baud rate factor in asynchronous mode is 16X regardless of the factor selected by MR11 and MR10. In addition, the corresponding clock pin provides an output at 1X the Baud rate. Custom Baud rates other than the ones provided by the standard part are available. Contact the factory for details.

MR27	MR26	MR25	MR24	MR23-MR20					
		Transmitter Clock	Receiver Clock	Code	Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Divisor
NOT USED		0=EXTERNAL 1=INTERNAL	0=EXTERNAL 1=INTERNAL	0000	50	0.8 KHz	0.8 KHz	—	6336
				0001	75	1.2	1.2	—	4224
				0010	110	1.76	1.76	—	2880
				0011	134.5	2.152	2.1523	0.016	2355
				0100	150	2.4	2.4	—	2112
				0101	300	4.8	4.8	—	1056
				0110	600	9.6	9.6	—	528
				0111	1200	19.2	19.2	—	264
				1000	1800	28.8	28.8	—	176
				1001	2000	32.0	32.081	0.253	158
				1010	2400	38.4	38.4	—	132
				1011	3600	57.6	57.6	—	88
				1100	4800	76.8	76.8	—	66
				1101	7200	115.2	115.2	—	44
				1110	9600	153.6	153.6	—	33
				1111	19200*	307.2	316.8	3.125	16

NOTE *Error at 19200 can be reduced to zero by using crystal frequency 4.9152MHz
16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X.
Baud rates are valid for crystal frequency = 5.0688MHz

TABLE 6—MODE REGISTER 2 (MR2)

COMMAND REGISTER (CR)

Table 7 illustrates the Command Register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. A 0 to 1 transition of CR2 forces start bit search (async mode) or hunt mode (sync mode) on the second $\overline{RxC}$ rising edge. Disabling the receiver causes $\overline{RxRDY}$ to go high (inactive). If the transmitter is disabled, it will complete the transmission of the character in the Transmit Shift Register (if any) prior to terminating operation. The TxD output will then remain in the marking state (high) while the $\overline{TxRDY}$ and $\overline{TxEMT}$ will go high (inactive). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected.

In asynchronous mode, setting CR3 will force and hold the TxD output low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go high for at least one bit time before beginning transmission of the next character in the Transmit Data Holding Register. In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the Transmit Data Holding Register. CR3 should be reset in response to the next TxRDY.

Setting CR4 causes the error flags in the Status Register (SR3, SR4, and SR5) to be cleared. This is a one time command. There is no internal latch for this bit.

The COM 2651 can operate in one of four sub-modes within each major mode (synchronous or asynchronous). The operational sub-mode is determined by CR7 and CR6. CR7-CR6=00 is the normal mode, with the transmitter and receiver operating independently in accordance with the Mode and Status Register instructions.

In asynchronous mode, CR7-CR6=01 places the COM 2651 in the Automatic Echo mode. Clocked, regenerated received data is automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2=1), but the transmitter need not be enabled. Processor to receiver communications continues normally, but the processor to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in Automatic Echo mode:

1. Data assembled by the receiver are automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. $\overline{TxRDY}$ output=1.
4. The $\overline{TxEMT/DSCHG}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In synchronous mode, CR7-CR6=01 places the COM 2651 in the Automatic SYN/DLE Stripping mode. The exact action taken depends on the setting of bits MR17 and MR16:

1. In the non-transparent, single SYN mode (MR17-MR16=10), characters in the data stream matching SYN1 are not transferred to the Receive Data Holding Register (RHR).
2. In the non-transparent, double SYN mode (MR17-MR16=00), characters in the data stream matching, SYN1, or SYN2 if immediately preceded by SYN1, are not transferred to the RHR. However, only the first SYN1 of an SYN1-SYN1 pair is stripped.
3. In transparent mode (MR16=1), characters in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However, only the first DLE of a DLE-DLE pair is stripped.

Note that Automatic Stripping mode does not affect the setting of the DLE Detect and SYN Detect status bits (SR3 and SR5).

Two diagnostic sub-modes can also be configured. In Local Loop Back mode (CR7-CR6=10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.
2. $\overline{DTR}$ is connected to $\overline{DCD}$ and $\overline{RTS}$ is connected to $\overline{CTS}$.
3. The receiver is clocked by the transmit clock.
4. The $\overline{DTR}$, $\overline{RTS}$ and $\overline{TxD}$ outputs are held high.
5. The $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ and RxD inputs are ignored.

Additional requirements to operate in the Local Loop Back mode are that CR0 (TxEN), CR1 (DTR), and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the COM 2651.

The second diagnostic mode is the Remote Loop Back mode (CR7-CR6=11). In this mode:

1. Data assembled by the receiver is automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. No data are sent to the local processor, but the error status conditions (PE, OE, FE) are set.
4. The $\overline{RxRDY}$, $\overline{TxRDY}$, and $\overline{TxEMT/DSCHG}$ outputs are held high.
5. CR0 (TxEN) is ignored.
6. All other signals operate normally.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode		Request to Send	Reset Error	Sync/Async	Receive Control (RxEN)	Data Terminal Ready	Transmit Control (TxEN)
00=NORMAL OPERATION 01=ASYNCH: AUTOMATIC ECHO MODE SYNCH: SYN AND/OR DLE STRIPPING MODE 10=LOCAL LOOP BACK 11=REMOTE LOOP BACK		0=FORCE $\overline{RTS}$ OUTPUT HIGH 1=FORCE $\overline{RTS}$ OUTPUT LOW	0=NORMAL 1=RESET ERROR FLAG IN STATUS (FE, OE, PE/DLE DETECT)	**ASYNCH: FORCE BREAK** 0=NORMAL 1=FORCE BREAK **SYNCH: SEND DLE** 0=NORMAL 1=SEND DLE	0=DISABLE 1=ENABLE	0=FORCE $\overline{DTR}$ OUTPUT HIGH 1=FORCE $\overline{DTR}$ OUTPUT LOW	0=DISABLE 1=ENABLE

TABLE 7—COMMAND REGISTER (CR)

STATUS REGISTER (SR)

The data contained in the Status Register (as shown in Table 8) indicate receiver and transmitter conditions and modem/data set status.

SR0 is the Transmitter Ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to 0, it indicates that the Transmit Data Holding Register has been loaded by the processor and the data has not been transferred to the Transmit Shift Register. If set equal to 1, it indicates that the Holding Register is ready to accept data from the processor. This bit is initially set when the Transmitter is enabled by CR0, unless a character has previously been loaded into the Holding Register. It is not set when the Automatic Echo or Remote Loop Back modes are programmed. When this bit is set, the $\overline{\text{TxRDY}}$ output pin is low. In the Automatic Echo and Remote Loop Back modes, the output is held high.

SR1, the Receiver Ready (RxRDY) status bit, indicates the condition of the Receive Data Holding Register. If set, it indicates that a character has been loaded into the Holding Register from the Receive Shift Register and is ready to be read by the processor. If equal to zero. there is no new character in the Holding Register. This bit is cleared when the processor reads the Receive Data Holding Register or when the receiver is disabled by CR2. When set, the $\overline{\text{RxRDY}}$ output is low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{\text{DSR}}$ or $\overline{\text{DCD}}$ inputs or that the Transmit Shift Register has completed transmission of a character and no new character has been loaded into the Transmit Data Holding Register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. TxEMT will not go active until at least one character has been transmitted. It is cleared by loading the Transmit Data Holding Register. The DSCHG condition is enabled when TxEN = 1 or RxEN = 1. It is cleared when the Status Register is read by the processor. When SR2 is set, the TxEMT/DSCHG output is low.

SR3, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16=1), with parity disabled, it indicates that a character matching the DLE Register has been received. However, only the first DLE of two successive DLEs will set SR3. This bit is cleared when the receiver is disabled and by the Reset Error command, CR4.

The Overrun Error status bit, SR4, indicates that the previous character loaded into the Receive Holding Register was not read by the processor at the time a new received character was transferred into it. This bit is cleared when the receiver is disabled and by the Reset Error command, CR4.

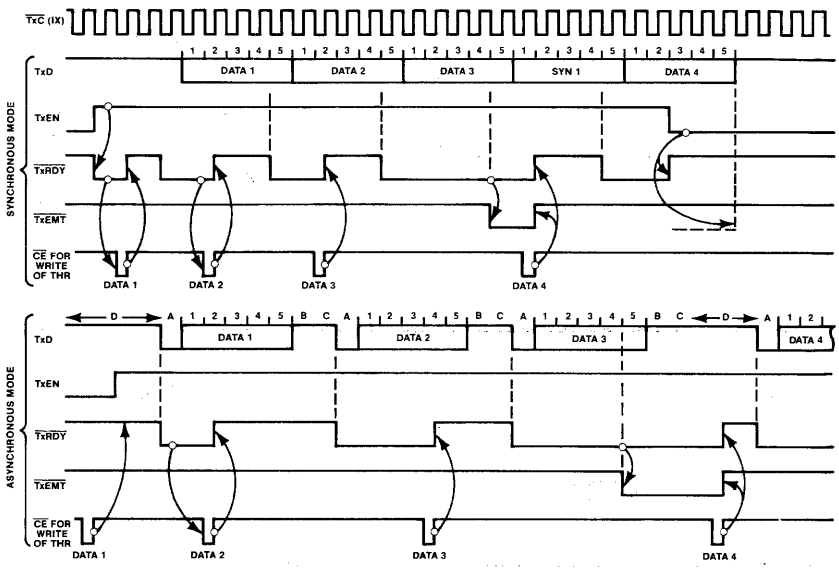
In asynchronous mode, bit SR5 signifies that the received character was not framed by the programmed number of stop bits. (if 1.5 stop bits are programmed, only the first stop bit is checked.) If the RHR contains all 0's when SR5=1, a break condition is present. In synchronous non-transparent mode (MR16=0), it indicates receipt of the SYN1 character in single SYN mode or the SYN1-SYN2 pair in double SYN mode. In synchronous transparent mode (MR16=1), this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1-SYN2) and, after synchronization has been achieved, when a DLE-SYN1 pair is received. The bit is reset when the receiver is disabled, when the Reset Error command is given in asynchronous mode, or when the Status Register is read by the processor in the synchronous mode.

SR6 and SR7 reflect the conditions of the $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ inputs respectively. A low input sets the corresponding status bit and a high input clears it.

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
Data Set Ready	**Data Carrier Detect**	**FE/SYN Detect**	**Overrun**	**PE/DLE Detect**	**TxEMT/DSCHG**	**RxRDY**	**TxRDY**
0=$\overline{\text{DSR}}$ INPUT IS HIGH 1=$\overline{\text{DSR}}$ INPUT IS LOW	0=$\overline{\text{DCD}}$ INPUT IS HIGH 1=$\overline{\text{DCD}}$ INPUT IS LOW	**ASYNCH:** 0=NORMAL 1=FRAMING ERROR **SYNCH:** 0=NORMAL 1=SYN CHAR DETECTED	0=NORMAL 1=OVERRUN ERROR	**ASYNCH:** 0=NORMAL 1=PARITY ERROR **SYNCH:** 0=NORMAL 1=PARITY ERROR OR DLE CHAR RECEIVED	0=NORMAL 1=CHANGE IN $\overline{\text{DSR}}$ OR $\overline{\text{DCD}}$, OR TRANSMIT SHIFT REGISTER IS EMPTY	0=RECEIVE HOLDING REG EMPTY 1=RECEIVE HOLDING REG HAS DATA	0=TRANSMIT HOLDING REG BUSY 1=TRANSMIT HOLDING REG EMPTY

TABLE 8—STATUS REGISTER (SR)

TxRDY, TxEMT (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])

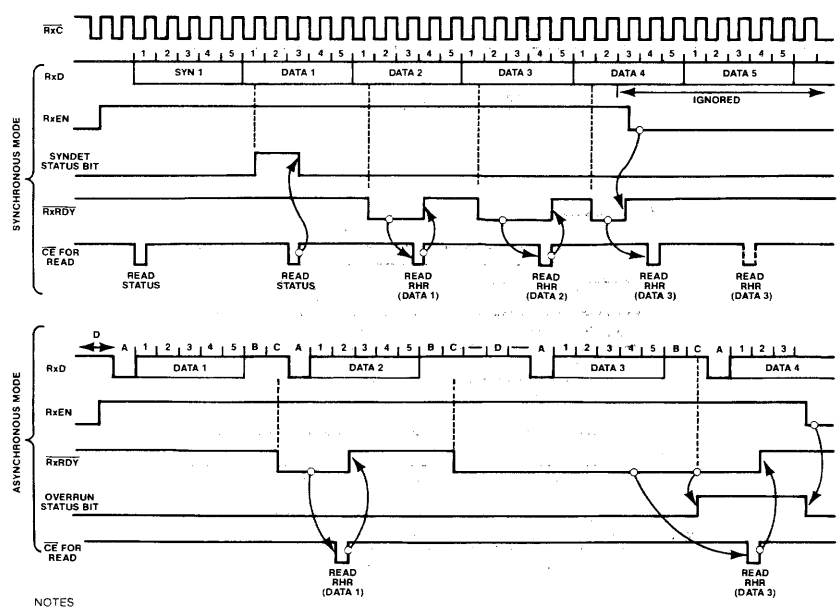


NOTES

A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition

TxEMT goes low at the beginning of the last data bit, or, if parity is enabled, at the beginning of the parity bit.

RxRDY (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])

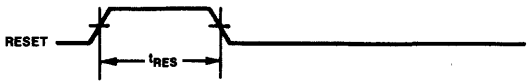


NOTES

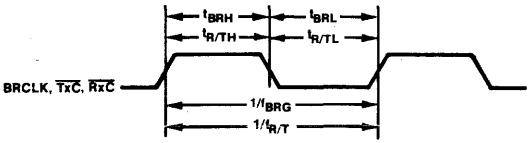
A Start bit
B Stop bit 1
C Stop bit 2
D TxD marking condition

TIMING DIAGRAMS (Cont'd)

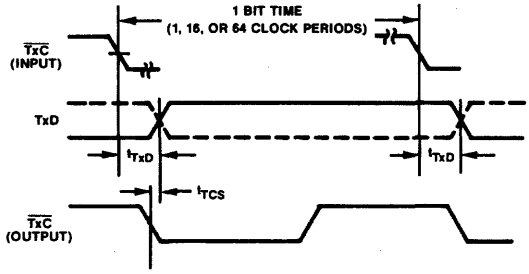
RESET



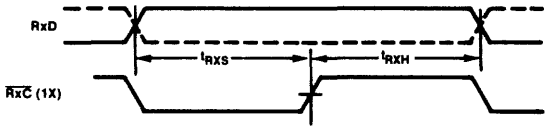
CLOCK



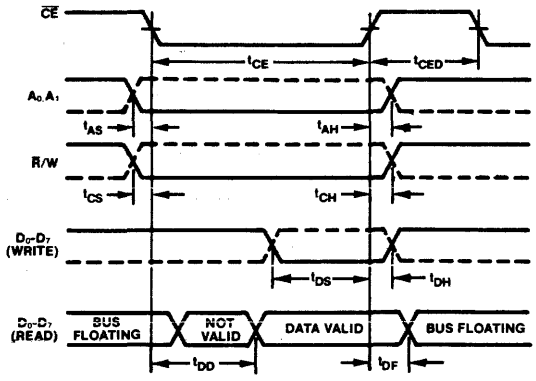
TRANSMIT



RECEIVE



READ AND WRITE



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, with respect to ground	+18.0V
Negative Voltage on any Pin, with respect to ground	−0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it it important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS T_A=0°C to +70°C, V_{CC}=5.0V ±5%

	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
	Input voltage					
V_{IL}	Low			0.8	V	
V_{IH}	High	2.0				
	Output voltage					
V_{OL}	Low			0.4	V	I_{OL}=1.6mA
V_{OH}	High	2.4				I_{OH}=−100μA
I_{IL}	Input leakage current			10	μA	V_{IN}=0 to 5.25V
	Output leakage current					
I_{LH}	Data bus high			10	μA	V_O=4.0V
I_{LL}	Data bus low			10	μA	V_O=0.45V
I_{CC}	Power supply current			150	mA	
	Capacitance					
C_{IN}	Input			20	pF	fc=1MHz
C_{OUT}	Output			20	pF	Unmeasured pins tied to ground
$C_{I/O}$	Input/Output			20	pF	

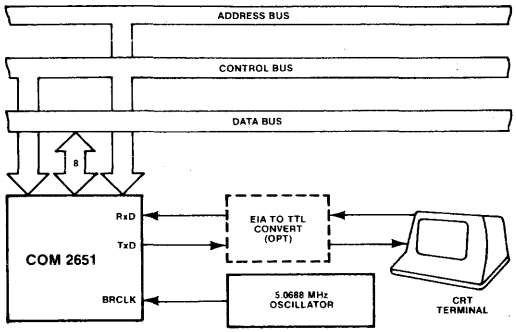
AC ELECTRICAL CHARACTERISTICS T_A=0°C to +70°C, V_{CC}=5.0V ±5%

	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
	Pulse width					
t_{RES}	Reset	1000			ns	
t_{CE}	Chip enable	300			ns	
	Setup and hold time					
t_{AS}	Address setup	20			ns	
t_{AH}	Address hold	20			ns	
t_{CS}	R/W control setup	20			ns	
t_{CH}	R/W control hold	20			ns	
t_{DS}	Data setup for write	225			ns	
t_{DH}	Data hold for write	0			ns	
t_{RXS}	Rx data setup	300			ns	
t_{RXH}	Rx data hold	350			ns	
t_{DD}	Data delay time for read			250	ns	C_L=100pF
t_{DF}	Data bus floating time for read			150	ns	C_L=100pF
t_{CED}	CE to CE delay	700			ns	
	Input clock frequency					
f_{BRG}	Baud rate generator	1.0	5.0688	5.0738	MHz	
$f_{R/T}$[1]	TxC or RxC	dc		1.0	MHz	
	Clock width					
t_{BRH}	Baud rate high	70			ns	f_{BRG}=5.0688MHz
t_{BRL}	Baud rate low	70			ns	f_{BRG}=5.0688MHz
$t_{R/TH}$[1]	TxC or RxC high	500			ns	
$t_{R/TL}$[1]	TxC or RxC low	500			ns	
t_{TXD}	TxD delay from falling edge of TxC			650	ns	C_L=100pF
t_{TCS}	Skew between TxD changing and falling edge of TxC output		0		ns	C_L=100pF

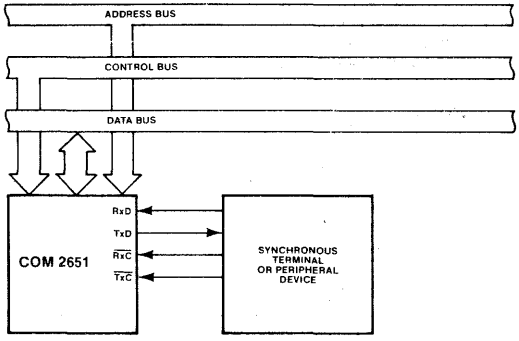
NOTE:
1. $f_{R/T}$ and $t_{R/TL}$ shown for all modes except Local Loopback. For Local Loopback mode $f_{R/T}$=0.7 MHz and $t_{R/TL}$=700ns min.

TYPICAL APPLICATIONS

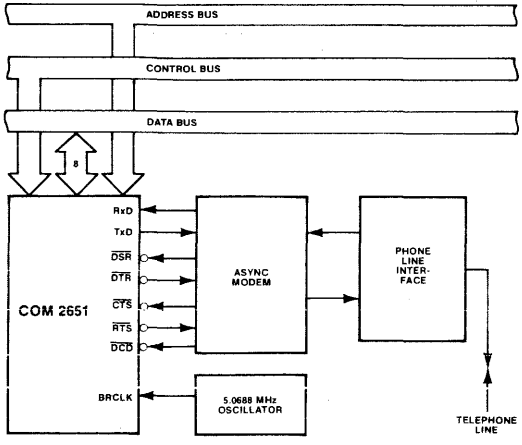
ASYNCHRONOUS INTERFACE TO CRT TERMINAL



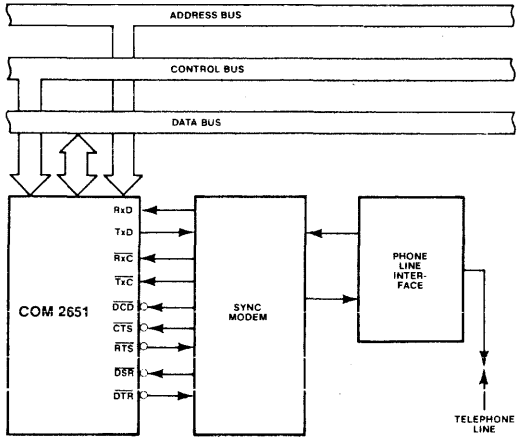
SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



ASYNCHRONOUS INTERFACE TO TELEPHONE LINES



SYNCHRONOUS INTERFACE TO TELEPHONE LINES



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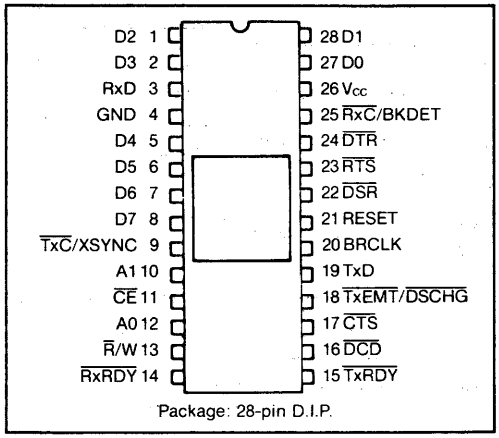
COM 2661-1
COM 2661-2
COM 2661-3
μPC FAMILY

Enhanced Programmable Communication Interface EPCI

FEATURES

- ☐ Synchronous and Asynchronous Full Duplex or Half Duplex Operations
- ☐ Re-programmable ROM on-chip baud rate generator
- ☐ Synchronous Mode Capabilities
  - —Selectable 5 to 8-Bit Characters
  - —Selectable 1 or 2 SYNC Characters
  - —Internal or External Character Synchronization
  - —Transparent or Non-Transparent Mode
  - —Transparent mode DLE stuffing (Tx) and detection (Rx)
  - —Automatic SYNC or DLE-SYNC Insertion
  - —SYNC, DLE and DLE-SYNC stripping
  - —Odd, Even, or No Parity
  - —Local or remote maintenance loop back mode
- ☐ Asynchronous Mode Capabilities
  - —Selectable 5 to 8-Bit Characters plus parity
  - —3 Selectable Clock Rates (1X, 16X, 64X the Baud Rate)
  - —Line Break Detection and Generation
  - —1, 1½, or 2-Stop Bit Detection and Generation
  - —False Start Bit Detection
  - —Odd, Even, or No Parity
  - —Parity, Overrun, and framing error detect
  - —Local or remote maintenance loop back mode
  - —Automatic serial echo mode (echoplex)
- ☐ Baud Rates
  - —DC to 1.0M Baud (Synchronous)
  - —DC to 1.0M Baud (1X, Asynchronous)
  - —DC to 62.5K Baud (16X, Asynchronous)
  - —DC to 15.625K Baud (64X, Asynchronous)

PIN CONFIGURATION



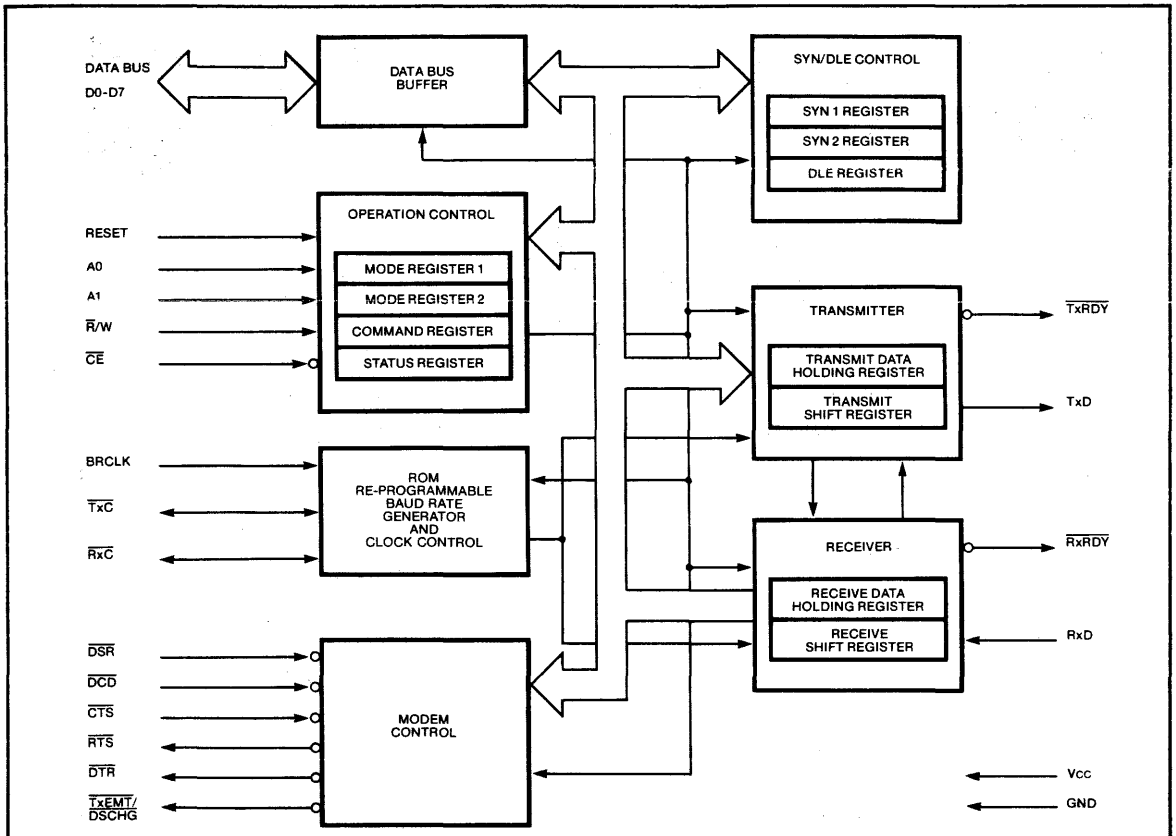
Package: 28-pin D.I.P.

- ☐ Double Buffering of Data
- ☐ RxC and TxC pins are short circuit protected
- ☐ Internal or External Baud Rate Clock
- ☐ 3 baud rate sets (2661-1, -2, -3)
- ☐ 16 internal rates for each version
- ☐ Single +5 volt Power Supply
- ☐ TTL Compatible
- ☐ No System Clock Required
- ☐ Compatible with EPCI 2661

GENERAL DESCRIPTION

The COM 2661 is an MOS/LSI device fabricated using SMC's patented COPLAMOS® technology. It is an enhanced pin and register compatible version of the COM 2651 that meets the majority of asynchronous and synchronous data communication requirements, by interfacing parallel digital systems to asynchronous and synchronous data communication channels while requiring a minimum of processor overhead. The COM2661 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. Each version of the COM 2661 (-1, -2, -3) has a different set of baud rates. Custom baud rates can be ROM reprogrammed to accommodate different baud rates and different starting frequencies.

The COM 2661 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for microcomputer system data communications. The USART is used as a peripheral and is programmed by the processor to communicate in commonly used asynchronous and synchronous serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status including data format errors and control signals is available to the processor at any time.



COM 2661 ORGANIZATION

The COM 2661 is organized into 6 major sections. Communication between each section is achieved via an internal data and control bus. The data bus buffer allows a processor access to all internal registers on the COM 2661. The differences between the COM 2661 and COM 2651 are outlined in table 1.

Operation Control

This functional block stores configuration and operation commands from the processor and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with a processor via the data bus and contains Mode Registers 1 and 2, the Command Register, and the Status Register. Details of register addressing and protocol are presented in the COM 2661 programming section of this specification.

Timing

The COM 2661 contains a Baud Rate Generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full duplex operation. Tables 2a, b, and c illustrate all available baud rates.

Receiver

The Receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and stores the "assembled" character in the receive data holding register until read by the processor.

Transmitter

The Transmitter accepts parallel data from the processor, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Modem Control

The modem control provides three output signals and accepts three input signals used for "handshaking" and status indication between the COM 2661 and a modem.

SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the processor. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

Interface Signals

The COM 2661 interface signals can be grouped into two types: the processor-related signals (shown in Table 3) which interface the COM 2661 to the processor, and the device-related signals (shown in Table 4), which are used to interface to the communications equipment.

TABLE 3—PROCESSOR RELATED SIGNALS

PIN NO.	NAME	SYMBOL	FUNCTION
1,2,5,6, 7,8,27,28	Data	D7-DØ	Bidirectional; 8 bit, three state data bus used to transfer commands, data and status between the COM 2661 and a processor. DØ is the least significant bit; D7 is the most significant bit.
10, 12	Address	A1, AØ	Input; Address lines used to select COM 2661 registers.
11	Chip Enable	$\overline{CE}$	Input; when this signal is low, the operation specified by the $\overline{R}$/W, A1 and AØ will be performed. When this input is high, D7-Ø are in the high impedance state.
13	Read/Write	$\overline{R}$/W	Input; Processor read/write direction control. This signal defines the direction of the data bus D7-0 when the COM 2661 is selected. D7-Ø drives out (read) when this signal is low and accepts data input when this signal is high. The input only has meaning when the $\overline{CE}$ input is active.
14	Receiver Ready	$\overline{RxRDY}$	Output; This signal is the complement of Status Register bit 1 (SR1). When low, it indicates that the Receive Data Holding Register (RHR) has a character ready for input to the processor. It goes high when the RHR is read by the processor, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the processor.
15	Transmitter Ready	$\overline{TxRDY}$	Output; This signal is the complement of Status Register bit 0 (SR0). When low, it indicates that the Transmit Data Holding Register (THR) is ready to accept a data character from the processor. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the processor.
18	Transmitter empty/data set change	$\overline{TxEMT}$/ $\overline{DSCHG}$	Output; This signal is the complement of Status Register bit 2 (SR2). When low, it indicates that the transmitter has completed serialization of the last character loaded by the processor, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This output goes high when the Status Register is read by the processor, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the processor for this line to go high. It is an open drain output which can be used as an interrupt to the processor.
21	Reset	Reset	Input; A high on this input performs a master reset on the COM 2661. This signal asynchronously terminates any device activity and clears the Mode, Command and Status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.
26	Supply Voltage	V_{CC}	+5 volts supply.
4	Ground	GND	Ground.

TABLE 4—DEVICE RELATED SIGNALS

PIN NO.	NAME	SYMBOL	FUNCTION
3	Receive Date	RxD	Input; Serial data to the receiver. "Mark" is high "space" is low.
9	Transmitter Clock/External Sync	$\overline{TxC}$/ XSYNC	Input or Output; If the external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X, the Baud rate as programmed by Mode Register 1. The transmitted data changes on the falling edge of the clock. If the internal transmitter clock is programmed, this pin can be a 1X/16X clock output or an external jam synchronization input.
16	Data Carrier Detect	$\overline{DCD}$	Input; This signal must be low in order for the receiver to function. The complement appears in the Status Register bit 6 (SR6). $\overline{DCD}$ causes a low output on $\overline{TxEMT}$/$\overline{DSCHG}$ when its state changes if CR2 or CR0=1. If $\overline{DCD}$ goes high while receiving, the RxC is internally inhibited.
17	Clear to Send	$\overline{CTS}$	Input; This signal must be low in order for the transmitter to function. If it goes high during transmission, the character in the Transmit Shift Register will be transmitted before termination.
19	Transmit Data	TxD	Output; Serial data from the transmitter. "Mark" is high, "Space" is low. This signal is held in the "Mark" condition when the transmitter is disabled.
20	Baud Rate Clock	BRCLK	Input; Clock input to the internal baud rate generator (See Tables 2a, b and c); not required if the external receiver and transmitter clocks are used.
22	Data Set Ready	$\overline{DSR}$	Input; This general purpose signal can be used for Data Set Ready or Ring Indicator condition. Its complement appears as Status Register bit 7 (SR7). $\overline{DSR}$ causes a low output on $\overline{TxEMT}$/$\overline{DSCHG}$ when its state changes if CR2 or CR0=1.
23	Request to Send	$\overline{RTS}$	Output; This general purpose signal is the complement of the Command Register bit 5 (CR5). It is normally used to indicate Request to Send. If the Transmit Shift Register is not empty when CR5 is reset (1 to 0), then $\overline{RTS}$ will go high on TxC time after the last serial bit is transmitted.
24	Data Terminal Ready	$\overline{DTR}$	Output; This general purpose signal is the complement of the Command Register bit 1 (CR1). It is normally used to indicate Data Terminal Ready.
25	Receive Clock/ Break Detect	$\overline{RxC}$/ BKDET	Input or Output; If the external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X, or 64X the Baud rate, as programmed by Mode Register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin can be a 1X/16X clock or a break detect output.

Table 1 COM 2661 vs. COM 2651

FEATURE	EPCI	PCI
1. MR2 Bit 6, 7	Control pin 9, 25	Not used
2. DLE detect-SR3	SR3=0 for DLE-DLE, DLE-SYNC1	SR3=1 for DLE-DLE, DLE-SYNC1
3. Reset of SR3, DLE detect	Second character after DLE; or receiver disable, or CR4=1	Receiver disable, or CR4=1
4. Send DLE-CR3	One time command	Reset via CR3 on next TxRDY
5. DLE stuffing in transparent mode	Automatic DLE stuffing when DLE is loaded except if CR3=1	None
6. SYNC1 stripping in double sync non-transparent mode	All SYNC1	First SYNC1 of pair
7. Baud rate versions	Three	One
8. Terminate ASYNC transmission (drop RTS)	Reset CR5 in response to TxRDY changing from 0 to 1	Reset CR0 when TxEMT goes from 1 to 0. Then reset CR5 when TxEMT goes from 0 to 1
9. Break detect	Pin 25[1]	FE and null character
10. Stop bit searched	One	Two
11. External jam sync	Pin 9[2]	No
12. Data bus timing	Improved over 2651	—
13. Data bus drivers	Sink 2.2mA Source 400μA	Sink 1.6mA Source 100μA

NOTES
1. Internal BRG used for RxC.
2. Internal BRG used for TxC.

Table 2a BAUD RATE GENERATOR CHARACTERISTICS 2661-1 (BRCLK=4.9152MHz)

MR23-20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	—	6144
0001	75	1.2	—	4096
0010	110	1.7598	−0.01	2793
0011	134.5	2.152	—	2284
0100	150	2.4	—	2048
0101	200	3.2	—	1536
0110	300	4.8	—	1024
0111	600	9.6	—	512
1000	1050	16.8329	0.196	292
1001	1200	19.2	—	256
1010	1800	28.7436	−0.19	171
1011	2000	31.9168	−0.26	154
1100	2400	38.4	—	128
1101	4800	76.8	—	64
1110	9600	153.6	—	32
1111	19200	307.2	—	16

Table 2b BAUD RATE GENERATOR CHARACTERISTICS 2661-2 (BRCLK=4.9152MHz)

MR23-20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	45.5	0.7279kHz	0.005	6752
0001	50	0.8	—	6144
0010	75	1.2	—	4096
0011	110	1.7598	−0.01	2793
0100	134.5	2.152	—	2284
0101	150	2.4	—	2048
0110	300	4.8	—	1024
0111	600	9.6	—	512
1000	1200	19.2	—	256
1001	1800	28.7438	−0.19	171
1010	2000	31.9168	−0.26	154
1011	2400	38.4	—	128
1100	4800	76.8	—	64
1101	9600	153.6	—	32
1110	19200	307.2	—	16
1111	38400	614.4	—	8

Table 2c BAUD RATE CHARACTERISTICS 2661-3 (BRCLK=5.0688MHz)

MR23-20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	—	6336
0001	75	1.2	—	4224
0010	110	1.76	—	2880
0011	134.5	2.1523	0.016	2355
0100	150	2.4	—	2112
0101	300	4.8	—	1056
0110	600	9.6	—	528
0111	1200	19.2	—	264
1000	1800	28.8	—	176
1001	2000	32.081	0.253	158
1010	2400	38.4	—	132
1011	3600	57.6	—	88
1100	4800	76.8	—	66
1101	7200	115.2	—	44
1110	9600	153.6	—	33
1111	19200	316.8	3.125	16

NOTE
16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X and BRG can be used only for TxC.

COM 2661 OPERATION

The functional operation of the COM 2661 is programmed by a set of control words supplied by the processor. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the COM 2661 Programming section of this data sheet.

After programming, the COM 2661 is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the processor to a serial bit stream. These actions are accomplished within the framework specified by the control words.

Receiver

The COM 2661 is conditioned to receive data when the $\overline{DCD}$ input is low and the RxEN bit in the command register is true. In the asynchronous mode, the receiver looks for a high to low (mark to space) transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and one stop bit have been assembled. The data is then transferred to the Receive Data Holding Register, the RxRDY bit in the status register is set, and the $\overline{RxRDY}$ output is asserted. If the character length is less than 8 bits, the high order unused bits in the Holding Register are set to zero. The Parity Error, Framing Error, and Overrun Error status bits are strobed into the status register on the positive going edge of $\overline{RxC}$ corresponding to the received character boundary. If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space as a start bit if it persists into the next bit time interval. If a break condition is detected (RxD is low for the entire character as well as the stop bit), only one character consisting of all zeros (with the Framing error status bit set) will be transferred to the Holding Register. The RxD input must return to a high condition before a search for the next start bit begins.

Pin 25 can be programmed to be a break detect output by appropriate setting of MR27-MR24. If so, a detected break will cause that pin to go high. When RxD returns to mark for one RxC time, pin 25 will go low. Refer to the break detection timing diagram.

When the COM 2661 is initialized into the synchronous mode, the receiver first enters the hunt mode on a 0 to 1 transition of RxEN (CR2). In this mode, as data is shifted into the Receiver Shift Register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly begins. If the single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the COM 2661 returns to the hunt mode. (Note that the sequence SYN1-SYN1-

SYN2 will not achieve synchronization). When synchronization has been achieved, the COM 2661 continues to assemble characters and transfers them to the Holding Register. The RxRDY status bit is set and the RxRDY output is asserted each time a character is assembled and transferred to the Holding Register. The Overrun error (OE) and Parity error (PE) status bits are set as appropriate. Further receipt of the proper SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the Holding Register. Note that the SYN characters used to establish initial synchronization are not transferred to the Holding Register in any case.

External jam synchronization can be achieved via pin 9 by appropriate setting of MR27-MR24. When pin 9 is an XSYNC input, the internal SYN1, SYN1-SYN2, and DLE-SYN1 detection is disabled. Each positive going signal on XSYNC will cause the receiver to establish synchronization on the rising edge of the next RxC pulse. Character assembly will start with the RxD input at this edge. XSYNC may be lowered on the next rising edge of RxC. This external synchronization will cause the SYN DETECT status bit to be set until the status register is read. Refer to XSYNC timing diagram.

Transmitter

The COM 2661 is conditioned to transmit data when the CTS input is low and the TxEN command register bit is set. The COM 2661 indicates to the processor that it can accept a character for transmission by setting the TxRDY status bit and asserting the TxRDY output. When the processor writes a character into the Transmit Data Holding Register, the TxRDY status bit is reset and the TxRDY output is returned to a high (false) state. Data is transferred from the Holding Register to the Transmit Shift Register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the Transmit Holding Register, the TxD output remains in the marking (high) condition and the TxEMT/DSCHG output and its corresponding status bit are asserted. Transmission resumes when the processor loads a new character into the Holding Register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the Send Break command bit high.

In the synchronous mode, when the COM 2661 is initially conditioned to transmit, the TxD output remains high and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the processor. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity, if commanded) are generated by the COM 2661 unless the processor fails to send a new character to the COM 2661 by the time the transmitter has completed sending the previous character. Since synchronous communication does not allow gaps between characters, the COM 2661 asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, SYN1-SYN2 doublets, or DLE-SYN1 doublets, depending on the state of MR16 and MR17. Normal transmission of the message resumes when a new character is available in the Transmit Data Holding Register. If the SEND DLE bit in the command register is true, the DLE character is automatically transmitted prior to transmission of the message character in the transmit holding register.

COM 2661 PROGRAMMING

Prior to initiating data communications, the COM 2661 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The COM 2661 can be reconfigured at any time during program execution. A flow chart of the initialization process appears in Figure 1.

The internal registers of the COM 2661 are accessed by applying specific signals to the CE, R/W, A1 and A0 inputs. The conditions necessary to address each register are shown in Table 5.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions A1=0, A0=1, and R/W=1. The first operation loads the SYN1 register. The next loads the SYN2 register, and the third loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses Mode Register 1, and a subsequent operation addresses Mode Register 2. If more

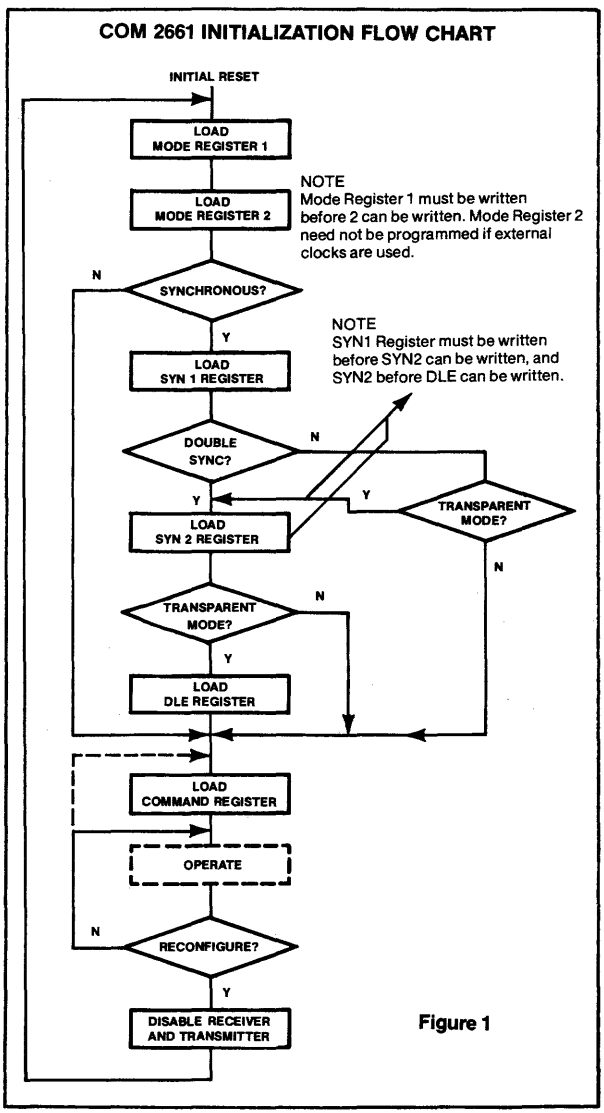


Figure 1

than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 Register and Mode Register 1 by a RESET input or by performing a "Read Command Register" operation, but are unaffected by any other read or write operation.

The COM 2661 register formats are summarized in Tables 6, 7, 8 and 9. Mode Registers 1 and 2 define the general operational characteristics of the COM 2661, while the Command Register controls the operation within this basic framework. The COM 2661 indicates its status in the Status Register. These registers are cleared when a RESET input is applied.

$\overline{CE}$	A1	A0	$\overline{R/W}$	FUNCTION
1	X	X	X	Tri-state data bus
0	0	0	0	Read receive holding register
0	0	0	1	Write transmit holding register
0	0	1	0	Read status register
0	0	1	1	Write SYN1/SYN2/DLE registers
0	1	0	0	Read mode registers 1 and 2
0	1	0	1	Write mode registers 1 and 2
0	1	1	0	Read command register
0	1	1	1	Write command register

NOTE
See AC Characteristics section for timing requirements.

Table 5—COM 2661 REGISTER ADDRESSING

MODE REGISTER 1 (MR1)

Table 6 illustrates Mode Register 1. Bits MR11 and MR10 select the communication format and Baud rate multiplier. 00 specifies synchronous mode and 1X multiplier. 1X, 16X, and 64X multipliers are programmable for asynchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7, or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14.

In asynchronous mode, MR17 and MR16 select character framing of 1, 1.5, or 2 stop bits (if 1X baud rate is programmed, 1.5, stop bits defaults to 1 stop bits on transmit). In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17=1, and SYN1-SYN2 is used when MR17=0. If the transparent mode is specified by MR16, DLE-SYN1 is used for character fill and SYN Detect, but the normal synchronization sequence is used. When transmitting, a DLE character in the transmit holding register will cause a second DLE character to be transmitted. This DLE stuffing eliminates the software DLE compare and stuff on each transparent mode data character. If the send DLE command (CR3) is active when a DLE is loaded into THR, only one additional DLE will be transmitted. Also DLE stripping and DLE Detect (with MR14=0) are enabled.

MR17	MR16	MR15	MR14	MR13	MR12	MR11	MR10
Sync/Async		Parity Type	Parity Control	Character Length		Mode and Baud Rate Factor	
ASYNCH: STOP BIT LENGTH 00=INVALID 01=1 STOP BIT 10=1⅛ STOP BITS 11=2 STOP BITS		0=ODD 1=EVEN	0=DISABLED 1=ENABLED	00=5 BITS 01=6 BITS 10=7 BITS 11=8 BITS		00=SYNCHRONOUS 1X RATE 01=ASYNCHRONOUS 1X RATE 10=ASYNCHRONOUS 16X RATE 11=ASYNCHRONOUS 64X RATE	
SYNCH: NUMBER OF SYN CHAR 0=DOUBLE SYN 1=SINGLE SYN	SYNCH: TRANSPARENCY CONTROL 0=NORMAL 1=TRANSPARENT						

NOTE Baud rate factor in asynchronous applies only if external clock is selected. Factor is 16X if internal clock is selected. Mode must be selected (MR11, MR10) in any case.

TABLE 6—MODE REGISTER 1 (MR1)

MODE REGISTER 2 (MR2)

Table 7 illustrates mode register 2 (MR23, MR22, MR21 and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable for each COM 2661 version (-1, -2, -3). Version 1 and 2 specify a 4.9152 MHz TTL input at BRCLK (pin 20); version 3 specifies a 5.0688 MHz input which is identical to the COM 2651. MR23-20 are don't cares if external clocks are selected (MR25-24=0). The individual rates are given in table 2a, b and c.

MR24-MR27 select the receive and transmit clock source (either the BRG or an external input) and the function at pins 9 and 25. Refer to table 7.

MR-27-MR24											MR23-MR20
	TxC	RxC	Pin 9	Pin 25		TxC	RxC	Pin 9	Pin 25	Mode	Baud Rate Selection
0000	E	E	TxC	RxC	1000	E	E	XSYNC'	RxC/TxC	sync	
0001	E	I	TxC	1X	1001	E	I	TxC	BKDET	async	
0010	I	E	1X	RxC	1010	I	E	XSYNC'	RxC	sync	
0011	I	I	1X	1X	1011	I	I	1X	BKDET	async	See baud rates in table 2
0100	E	E	TxC	RxC	1100	E	E	XSYNC'	RxC/TxC	sync	
0101	E	I	TxC	16X	1101	E	I	TxC	BKDET	async	
0110	I	E	16X	RxC	1110	I	E	XSYNC'	RxC	sync	
0111	I	I	16X	16X	1111	I	I	16X	BKDET	async	

NOTES
1. When pin 9 is programmed as XSYNC input, SYN1, SYN1-SYN2, and DLE-SYN1 detection is disabled.

E=External clock I=Internal clock (BRG)
1X and 16X are clock outputs

TABLE 7—MODE REGISTER 2 (MR2)

COMMAND REGISTER (CR)

Table 8 illustrates the Command Register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. A 0 to 1 transition of CR2 forces start bit search (async mode) or hunt mode (sync mode) on the second RxC rising edge. Disabling the receiver causes RxRDY to go high (inactive). If the transmitter is disabled, it will complete the transmission of the character in the Transmit Shift Register (if any) prior to terminating operation. The TxD output will then remain in the marking state (high while the TxRDY and TxEMT will go high (inactive). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected. Bits CR1 (DTR) and CR5 (RTS) control the DTR and RTS outputs. Data at the outputs are the logical complement of the register data.

In asynchronous mode, setting CR3 will force and hold the TxD output low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go high for at least one bit time before beginning transmission of the next character in the Transmit Data Holding Register. In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the Transmit Data Holding Register. Since this is a one time command, CR3 does not have to be reset by software. CR3 should be set when entering and exiting transparent mode and for all DLE—non-DLE character sequences.

Setting CR4 causes the error flags in the Status Register (SR3, SR4, and SR5) to be cleared. This is a one time command. There is no internal latch for this bit. When CR5 (RTS) is set, the RTS pin is forced low and the transmit serial logic is enabled. A 1 to 0 transition of CR5 will cause RTS to go high (inactive) one TxC time after the last serial bit has been transmitted (if the transmit shift register was not empty).

The COM 2661 can operate in one of four sub-modes within each major mode (synchronous or asynchronous). The operational sub-mode is determined by CR7 and CR6. CR7-CR6=00 is the normal mode, with the transmitter and receiver operating independently in accordance with the Mode and Status Register instructions.

In asynchronous mode, CR7-CR6=01 places the COM 2661 in the Automatic Echo mode. Clocked, regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2=1), but the transmitter need not be enabled. Processor to receiver communications continue normally, but the processor to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in Automatic Echo mode:

1. Data assembled by the receiver are automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. TxRDY output=1.
4. The TxEMT/DSCHG pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In synchronous mode, CR7-CR6=01 places the COM 2661 in the Automatic SYN/DLE Stripping mode. The exact action taken depends on the setting of bits MR17 and MR16:

1. In the non-transparent, single SYN mode (MR17-MR16=10), characters in the data stream matching SYN1 are not transferred to the Receive Data Holding Register (RHR).
2. In the non-transparent, double SYN mode (MR17-MR16=00), characters in the data stream matching SYN1, or SYN2 if immediately preceded by SYN1, are not transferred to the RHR.
3. In transparent mode (MR16=1), characters in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However, only the first DLE of a DLE-DLE pair is stripped.

Note that Automatic Stripping mode does not affect the setting of the DLE Detect and SYN Detect status bits (SR3 and SR5).

Two diagnostic sub-modes can also be configured. In Local Loop Back mode (CR7-CR6=10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.
2. DTR is connected to DCD and RTS is connected to CTS.
3. The receiver is clocked by the transmit clock.
4. The DTR, RTS and TxD outputs are held high.
5. The CTS, DCD, DSR and RxD inputs are ignored.

Additional requirements to operate in the Local Loop Back mode are that CR0 (TxEN), CR1 (DTR), and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the COM 2661.

The second diagnostic mode is the Remote Loop Back mode (CR7-CR6=11). In this mode:

1. Data assembled by the receiver is automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. No data are sent to the local processor, but the error status conditions (PE, OE, FE) are set.
4. The RxRDY, TxRDY, and TxEMT/DSCHG outputs are held high.
5. CR1 (TxEN) is ignored.
6. All other signals operate normally.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode		Request to Send	Reset Error	Sync/Async	Receive Control (RxEN)	Data Terminal Ready	Transmit Control (TxEN)
00=NORMAL OPERATION 01=ASYNCH: AUTOMATIC ECHO MODE SYNCH: SYN AND/OR DLE STRIPPING MODE 10=LOCAL LOOP BACK 11=REMOTE LOOP BACK		0 FORCE RTS OUTPUT HIGH ONE CLOCK TIME AFTER TxSR SERIALIZATION 1 FORCE RTS OUTPUT LOW	0=NORMAL 1=RESET ERROR FLAG IN STATUS (FE, OE, PE/DLE DETECT)	**ASYNCH: FORCE BREAK** 0=NORMAL 1=FORCE BREAK **SYNCH: SEND DLE** 0=NORMAL 1=SEND DLE	0=DISABLE 1=ENABLE	0=FORCE DTR OUTPUT HIGH 1=FORCE DTR OUTPUT LOW	0=DISABLE 1=ENABLE

TABLE 8—COMMAND REGISTER (CR)

STATUS REGISTER (SR)

The data contained in the Status Register (as shown in Table 9) indicate receiver and transmitter conditions and modem/data set status.

SR0 is the Transmitter Ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to 0, it indicates that the Transmit Data Holding Register has been loaded by the processor and the data has not been transferred to the Transmit Shift Register. If set equal to 1, it indicates that the Holding Register is ready to accept data from the processor. This bit is initially set when the Transmitter is enabled by CR0, unless a character has previously been loaded into the Holding Register. It is not set when the Automatic Echo or Remote Loop Back modes are programmed. When this bit is set, the $\overline{\text{TxRDY}}$ output pin is low. In the Automatic Echo and Remote Loop Back modes, the output is held high.

SR1, the Receiver Ready (RxRDY) status bit, indicates the condition of the Receive Data Holding Register. If set,it indicates that a character has been loaded into the Holding Register from the Receive Shift Register and is ready to be read by the processor. If equal to zero, there is no new character in the Holding Register. This bit is cleared when the processor reads the Receive Data Holding Register or when the receiver is disabled by CR2. When set, the $\overline{\text{RxRDY}}$ output is low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{\text{DSR}}$ or $\overline{\text{DCD}}$ inputs (when CR2 or CR0=1) or that the Transmit Shift Register has completed transmission of a character and no new character has been loaded into the Transmit Data Holding Register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. TxEMT will not go active until at least one character has been transmitted. It is cleared by loading the Transmit Data Holding Register. The DSCHG condition is enabled when TxEN=1 or RxEN=1. It is cleared when the status register is read by the processor. If the status register is read twice and SR2=1 while SR6 and SR7 remain unchanged, then a TxEMT condition exists. When SR2 is set, the $\overline{\text{TxEMT/DSCHG}}$ output is low.

SR3, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16=1), with parity disabled, it indicates that a character matching the DLE Register has been received, and the present character is neither SYN1 nor DLE. This bit is cleared when the next character following the above sequence is loaded into the Receive Data Holding Register, when the receiver is disabled, or by a reset error command, CR4.

The Overrun Error status bit, SR4, indicates that the previous character loaded into the Receive Holding Register was not read by the processor at the time a new received character was transferred into it. This bit is cleared when the receiver is disabled and by the Reset Error command, CR4.

In asynchronous mode, bit SR5 signifies that the received character was not framed by a stop bit, i.e., only the first stop bit is checked. If the RHR contains all 0's when SR5=1, a break condition is present. In synchronous non-transparent mode (MR16=0), it indicates receipt of the SYN1 character in single SYN mode or the SYN1-SYN2 pair in double SYN mode. In synchronous transparent mode (MR16=1), this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1-SYN2) and, after synchronization has been achieved, when a DLE-SYN1 pair is received. The bit is reset when the receiver is disabled, when the Reset Error command is given in asynchronous mode, or when the Status Register is read by the processor in the synchronous mode.

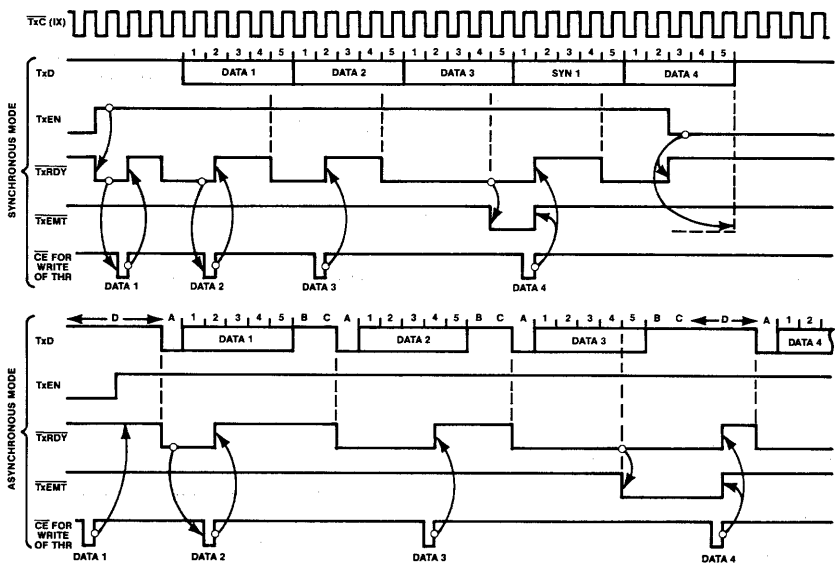
SR6 and SR7 reflect the conditions of the $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ inputs respectively. A low input sets the corresponding status bit and a high input clears it.

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
Data Set Ready	**Data Carrier Detect**	**FE/SYN Detect**	**Overrun**	**PE/DLE Detect**	**TxEMT/DSCHG**	**RxRDY**	**TxRDY**
0=$\overline{\text{DSR}}$ INPUT IS HIGH 1=$\overline{\text{DSR}}$ INPUT IS LOW	0=$\overline{\text{DCD}}$ INPUT IS HIGH 1=$\overline{\text{DCD}}$ INPUT IS LOW	**ASYNCH:** 0=NORMAL 1=FRAMING ERROR **SYNCH:** 0=NORMAL 1=SYN CHAR DETECTED	0=NORMAL 1=OVERRUN ERROR	**ASYNCH:** 0=NORMAL 1=PARITY ERROR **SYNCH:** 0=NORMAL 1=PARITY ERROR OR DLE CHAR RECEIVED	0=NORMAL 1=CHANGE IN $\overline{\text{DSR}}$ OR $\overline{\text{DCD}}$, OR TRANSMIT SHIFT REGISTER IS EMPTY	0=RECEIVE HOLDING REG EMPTY 1=RECEIVE HOLDING REG HAS DATA	0=TRANSMIT HOLDING REG BUSY 1=TRANSMIT HOLDING REG EMPTY

TABLE 9—STATUS REGISTER (SR)

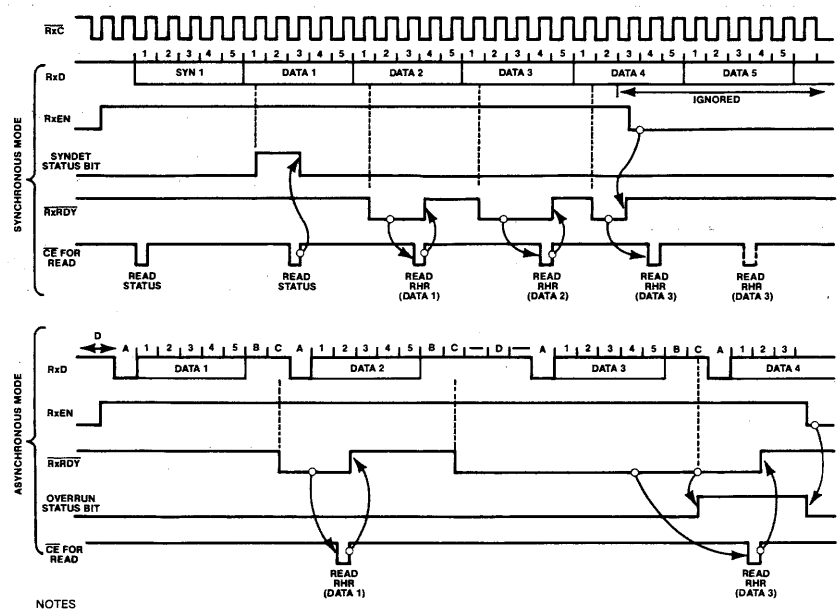
TIMING DIAGRAMS

TxRDY, TxEMT (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



NOTES
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
TxEMT goes low at the beginning of the last data bit, or, if parity is enabled, at the beginning of the parity bit.

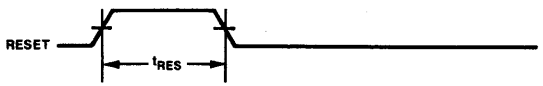
RxRDY (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



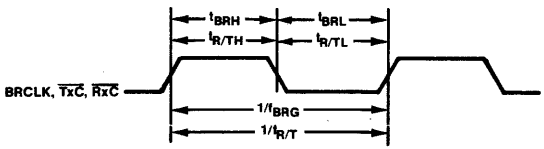
NOTES
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition

TIMING DIAGRAMS (Cont'd)

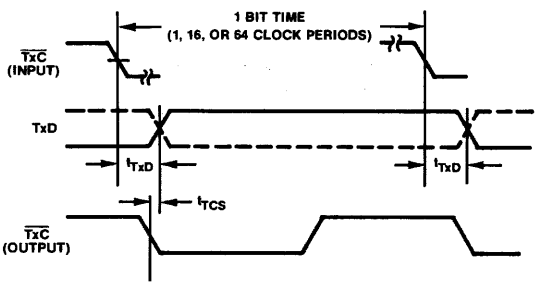
RESET



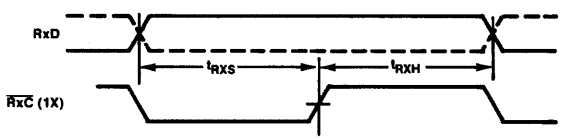
CLOCK



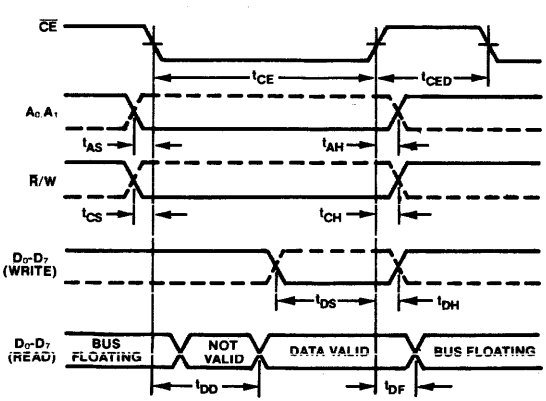
TRANSMIT



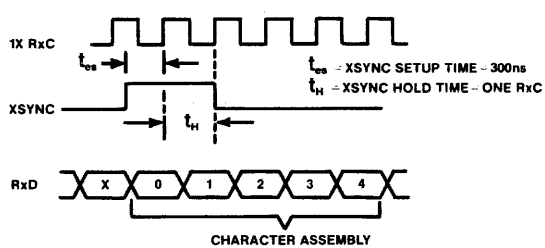
RECEIVE



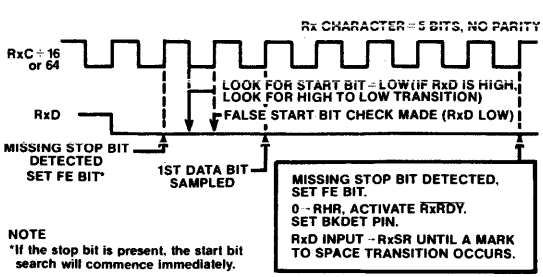
READ AND WRITE



EXTERNAL SYNCHRONIZATION WITH XSYNC



BREAK DETECTION TIMING



NOTE
*If the stop bit is present, the start bit search will commence immediately.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it it important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS T_A=0°C to +70°C, V_{CC}=5.0V±5%

	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
	Input voltage					
V_{IL}	Low			0.8	V	
V_{IH}	High	2.0				
	Output voltage					
V_{OL}	Low			0.4	V	I_{OL}=2.2mA
V_{OH}	High	2.4				I_{OH}=−400μA
I_{IL}	Input leakage current			10	μA	V_{IN}=0 to 5.5V
	Output leakage current					
I_{LH}	Data bus high			10	μA	V_O=4.0V
I_{LL}	Data bus low			10	μA	V_O=0.45V
I_{CC}	Power supply current			150	mA	
	Capacitance					
C_{IN}	Input			20	pF	fc=1MHz
C_{OUT}	Output			20	pF	Unmeasured pins tied
$C_{I/O}$	Input/Output			20	pF	to ground

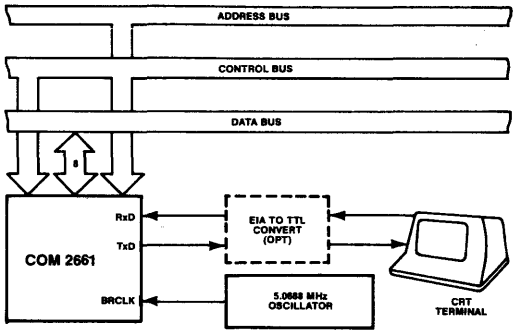
AC ELECTRICAL CHARACTERISTICS T_A=0°C to +70°C, V_{CC}=5.0V±5%

	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
	Pulse width					
t_{RES}	Reset	1000			ns	
t_{CE}	Chip enable	250			ns	
	Setup and hold time					
t_{AS}	Address setup	10			ns	
t_{AH}	Address hold	10			ns	
t_{CS}	R/$\overline{W}$ control setup	10			ns	
t_{CH}	R/$\overline{W}$ control hold	10			ns	
t_{DS}	Data setup for write	150			ns	
t_{DH}	Data hold for write	0			ns	
t_{RXS}	Rx data setup	300			ns	
t_{RXH}	Rx data hold	350			ns	
t_{DD}	Data delay time for read			200	ns	C_L=150pF
t_{DF}	Data bus floating time for read			100	ns	C_L=150pF
t_{CED}	$\overline{CE}$ to $\overline{CE}$ delay	600			ns	
	Input clock frequency					
f_{BRG}	Baud rate generator (2661-1, -2)	1.0	4.9152	4.9202	MHz	
f_{BRG}	Baud rate generator (2661-3)	1.0	5.0688	5.0738	MHz	
f_{RT}[1]	$\overline{TxC}$ or $\overline{RxC}$	dc		1.0	MHz	
	Clock width					
t_{BRH}	Baud rate high (2661-1, -2)	75			ns	f_{BRG}=4.915MHz; measured at V_{IH}
t_{BRH}	Baud rate high (2661-3)	70			ns	f_{BRG}=5.0688MHz; measured at V_{IH}
t_{BRL}	Baud rate low (2661-1, -2)	75			ns	f_{BRG}=4.915MHz; measured at V_{IL}
t_{BRL}	Baud rate low (2661-3)	70			ns	f_{BRG}=5.0688MHz; measured at V_{IL}
t_{RTH}	$\overline{TxC}$ or $\overline{RxC}$ high	480			ns	
t_{RTL}	$\overline{TxC}$ or $\overline{RxC}$ low	480			ns	
t_{TXD}	TxD delay from falling edge of $\overline{TxC}$			650	ns	C_L=150pF
t_{TCS}	Skew between TxD changing and falling edge of $\overline{TxC}$ output		0		ns	C_L=150pF

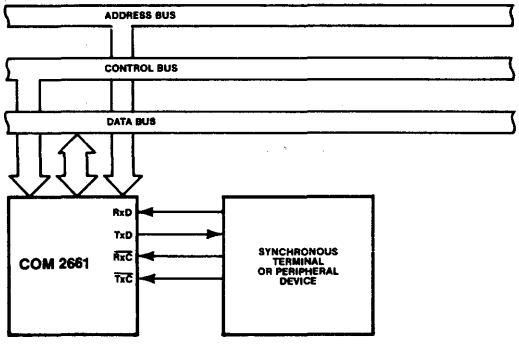
NOTE:
1. f_{RT} and t_{RTL} shown all modes except Local Loopback. For Local Loopback mode f_{RT}=0.7MHz and t_{RTL}=700ns min.

TYPICAL APPLICATIONS

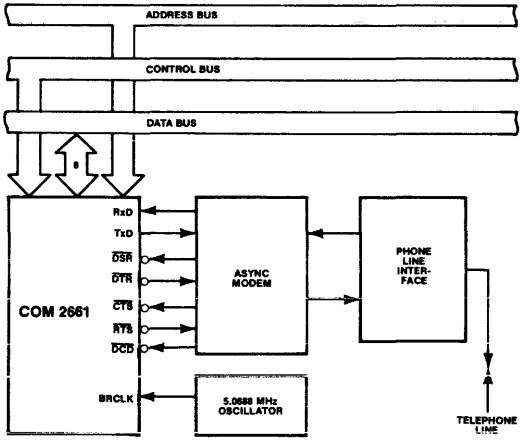
ASYNCHRONOUS INTERFACE TO CRT TERMINAL



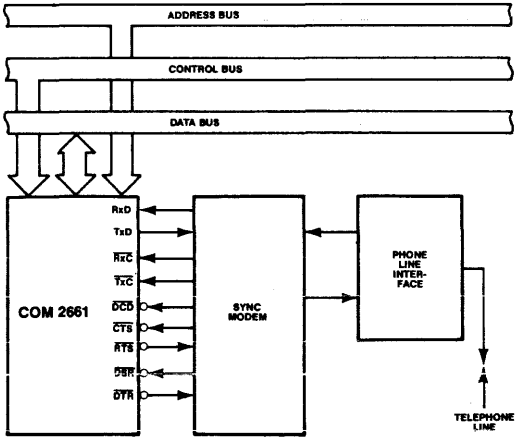
SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



ASYNCHRONOUS INTERFACE TO TELEPHONE LINES



SYNCHRONOUS INTERFACE TO TELEPHONE LINES



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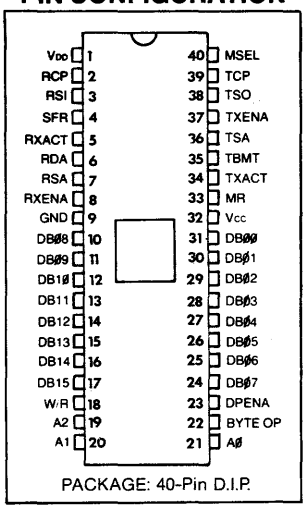
COM 5025
μPC FAMILY

Multi-Protocol Universal Synchronous Receiver/Transmitter
USYNR/T

FEATURES

- ☐ Selectable Protocol—Bit or Byte oriented
- ☐ Direct TTL Compatibility
- ☐ Three-state Input/Output BUS
- ☐ Processor Compatible—8 or 16 bit
- ☐ High Speed Operation—1.5 M Baud—typical
- ☐ Fully Double Buffered—Data, Status, and Control Registers
- ☐ Full or Half Duplex Operation—independent Transmitter and Receiver Clocks
  —individually selectable data length for Receiver and Transmitter
- ☐ Master Reset—resets all Data, Status, and Control Registers
- ☐ Maintenance Select—built-in self checking

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

BIT ORIENTED PROTOCOLS—SDLC, HDLC, ADCCP
- ☐ Automatic bit stuffing and stripping
- ☐ Automatic frame character detection and generation
- ☐ Valid message protection—a valid received message is protected from overrun
- ☐ Residue Handling—for messages which terminate with a partial data byte, the number of valid data bits is available

SELECTABLE OPTIONS:
- ☐ Variable Length Data—1 to 8 bit bytes
- ☐ Error Checking—CRC (CRC16, CCITT-0, or CCITT-1)
  —None
- ☐ Primary or Secondary Station Address Mode
- ☐ All Parties Address—APA
- ☐ Extendable Address Field—to any number of bytes
- ☐ Extendable Control Field—to 2 bytes
- ☐ Idle Mode—idle FLAG characters or MARK the line
- ☐ Point to Point, Multi-drop, or Loop Configuration

BYTE ORIENTED PROTOCOLS—BiSync, DDCMP
- ☐ Automatic detection and generation of SYNC characters

SELECTABLE OPTIONS:
- ☐ Variable Length Data—1 to 8 bit bytes
- ☐ Variable SYNC character—5, 6, 7, or 8 bits
- ☐ Error Checking—CRC (CRC16, CCITT-0, or CCITT-1)
  —VRC (odd/even parity)
  —None
- ☐ Strip Sync—deletion of leading SYNC characters after synchronization
- ☐ Idle Mode—idle SYNC characters or MARK the line

APPLICATIONS

- ☐ Intelligent Terminals
- ☐ Line Controllers
- ☐ Network Processors
- ☐ Front End Communications
- ☐ Remote Data Concentractors
- ☐ Communication Test Equipment
- ☐ Computer to Computer Links
- ☐ Hard Disk Data Handler

General Description

The COM 5025 is a COPLAMOS® n channel silicon gate MOS/LSI device that meets the majority of synchronous communications requirements, by interfacing parallel digital systems to synchronous serial data communication channels while requiring a minimum of controller overhead.

The COM 5025 is well suited for applications such as computer to modem interfaces, computer to computer serial links and in terminal applications. Since higher level decisions and responses are made or initiated by the controller, some degree of intelligence in each controller of the device is necessary.

Newly emerging protocols such as SDLC, HDLC, and ADCCP will be able to utilize the COM 5025 with a high degree of efficiency as zero insertion for transmission and zero deletion for reception are done automatically. These protocols will be referred to as Bit Oriented Protocols (BOP). Any differences between them will be discussed in their respective sections. Conventional synchronous protocols that are control character oriented such as BISYNC can also utilize this device. Control Character oriented protocols will be referred to as CCP protocols. Other types of protocols that operate on a byte or character count basis can also utilize the COM 5025 with a high degree of efficiency in most cases. These protocols, such as DDCMP will also be referred to as CCP protocols.

The COM 5025 is designed to operate in a synchronous communications system where some external source is expected to provide the necessary received serial data, and all clock signals properly synchronized according to EIA standard RS334. The external controller of the chip will provide the necessary control signals, intelligence in interpreting control signals from the device and data to be transmitted in accord with RS334.

The receiver and transmitter are as symmetrical as possible without loss of efficiency. The controller of the device will be responsible for all higher level decisions and interpretation of some fields within message frames. The degree to which this occurs is dependent on the protocol being implemented. The receiver and transmitter logic operate as two totally independent sections with a minimum of common logic.

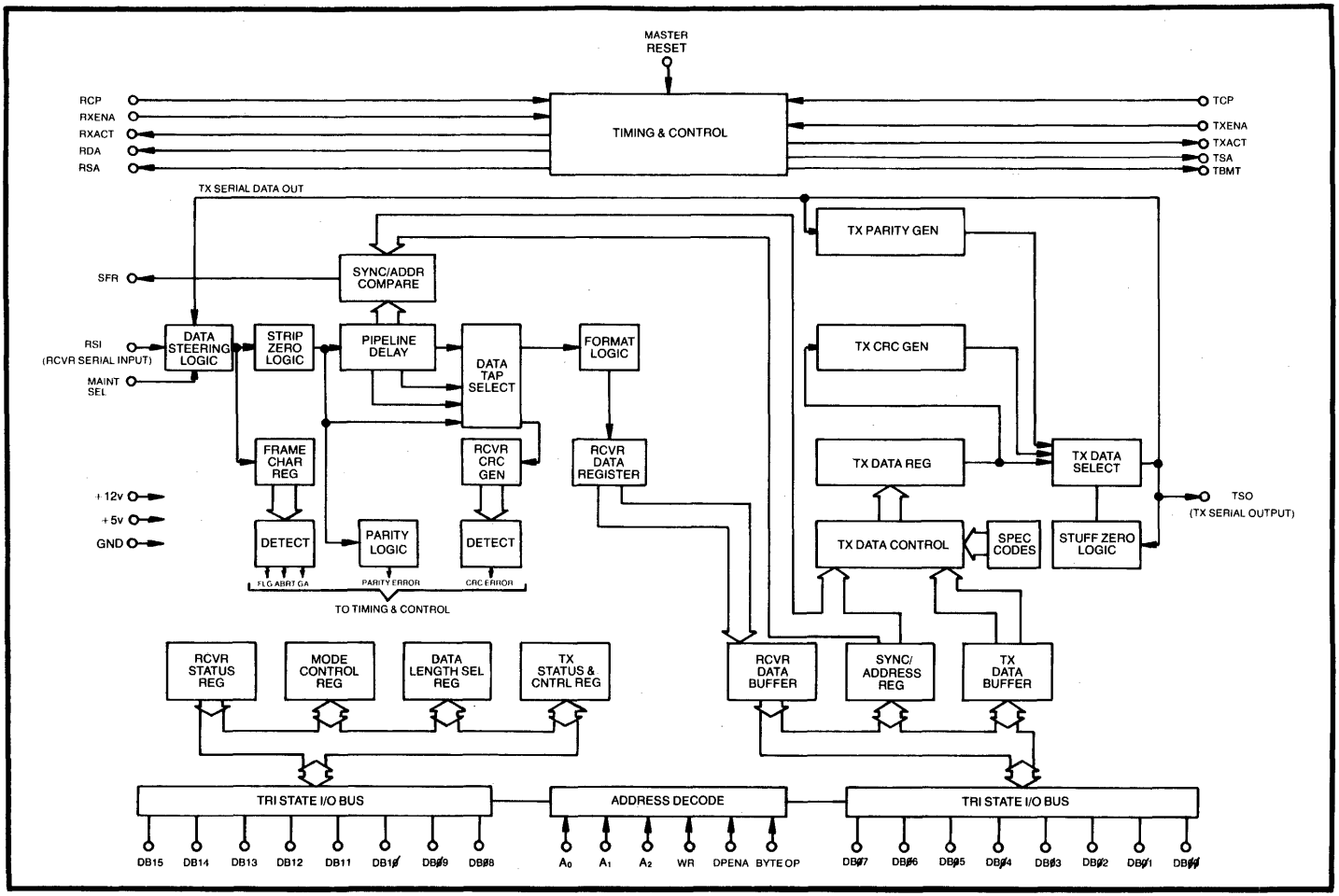
References:

1. ANSI—American National Standards Institute
   X353, XS34/589
   202-466-2299
2. CCITT—Consultative Committee for International Telephone and Telegraph
   X.25
   202-632-1007
3. EIA—Electronic Industries Association
   TR30, RS334
   202-659-2200
4. IBM
   General Information Brochure, GA27-3093
   Loop Interface—OEM Information, GA27-3098
   System Journal—Vol. 15, No. 1, 1976; G321-0044

Terminology

Term	Definition	Term	Definition
BOP	Bit Oriented Protocols: SDLC, HDLC, ADCCP	GA	01111111 (0 (LSB) followed by 7-1's)
CCP	Control Character Protocols: BiSync, DDCMP	LSB	First transmitted bit, First received bit
TDB	Transmitter Data Buffer	MSB	Last transmitted bit, Last received bit
RDB	Receiver Data Buffer	RDP	Receiver Data Path
TDSR	Transmitter Data Shift Register	TDP	Transmitter Data Path
FLAG	01111110	LM	Loop Mode
ABORT	11111111 (7 or more contiguous 1's)		

BLOCK DIAGRAM



Description of Pin Functions

Pin No.	Symbol	Name	I/O	Function
1	V_{DD}	Power Supply	PS	+12 volt Power Supply.
2	RCP	Receiver Clock	I	The positive-going edge of this clock shifts data into the receiver shift register.
3	RSI	Receiver Serial Input	I	This input accepts the serial bit input stream.
4	SFR	Sync/Flag Received	O	This output is set high, for 1 clock time of the RCP, each time a sync or flag character is received.
5	RXACT	Receiver Active	O	This output is asserted when the RDP presents the first data character of the message to the controller. In the BOP mode the first data character is the first non-flag character (address byte). In the CCP mode: 1. if strip-sync is set; the first non-sync character is the first data character 2. if strip-sync is not set; the first data character is the character following the second sync. In the BOP mode the trailing (next) FLAG resets RXACT. In the CCP mode RXACT is never reset, it can be cleared via RXENA.
6	RDA	Receiver Data Available	O	This output is set high when the RDP has assembled an entire character and transferred it into the RDB. This output is reset by reading the RDB.
7	RSA	Receiver Status Available	O	This output is set high: 1. CCP—in the event of receiver over run (ROR) or parity error (if selected), 2. BOP—in the event of ROR, CRC error (if selected) receiving REOM or RAB/GA. This output is reset by reading the receiver status register or dropping of RXENA.
8	RXENA	Receiver Enable	I	A high level input allows the processing of RSI data. A low level disables the RDP and resets RDA, RSA and RXACT.
9	GND	Ground	GND	Ground
10	DBØ8	Data Bus	I/O	Bidirectional Data Bus.
11	DBØ9	Data Bus	I/O	Bidirectional Data Bus.
12	DB1Ø	Data Bus	I/O	Bidirectional Data Bus.
13	DB11	Data Bus	I/O	Bidirectional Data Bus.
14	DB12	Data Bus	I/O	Bidirectional Data Bus.
15	DB13	Data Bus	I/O	Bidirectional Data Bus.
16	DB14	Data Bus	I/O	Bidirectional Data Bus.
17	DB15	Data Bus	I/O	Bidirectional Data Bus.
18	W/R	Write/Read	I	Controls direction of data port. W/R=1, Write. W/R=0, Read.
19	A2	Address 2	I	Address input—MSB.
20	A1	Address 1	I	Address input.
21	AØ	Address 0	I	Address input—LSB.
22	BYTE OP	Byte Operation	I	If asserted, byte operation (data port is 8 bits wide) is selected. If BYTE OP=0, data port is 16 bits wide.
23	DPENA	Data Port Enable	I	Strobe for data port. After address, byte op, W/R and data are set-up DPENA may be strobed. If reading the port, DPENA may reset (depending on register selected by address) RDA or RSA. If writing into the port, DPENA may reset (depending on register selected by address) TBMT.
24	DBØ7	Data Bus	I/O	Bidirectional Data Bus—MSB.
25	DBØ6	Data Bus	I/O	Bidirectional Data Bus.
26	DBØ5	Data Bus	I/O	Bidirectional Data Bus.
27	DBØ4	Data Bus	I/O	Bidirectional Data Bus.
28	DBØ3	Data Bus	I/O	Bidirectional Data Bus.
29	DBØ2	Data Bus	I/O	Bidirectional Data Bus.
30	DBØ1	Data Bus	I/O	Bidirectional Data Bus.
31	DBØØ	Data Bus	I/O	Bidirectional Data Bus—LSB.
32	V_{CC}	Power Supply	PS	+5 volt Power Supply.
33	MR	Master Reset	I	This input should be pulsed high after power turn on. This will: clear all flags, and status conditions, set TBMT=1, TSO=1 and place the device in the primary BOP mode with 8 bit TX/RX data length, CRC CCITT initialized to all 1's.
34	TXACT	Transmitter Active	O	This output indicates the status of the TDP. TXACT will go high after asserting TXENA and TSOM coinsidently with the first TSO bit. This output will reset one half clock after the byte during which TXENA is dropped.
35	TBMT	Transmitter Buffer Empty	O	This output is at a high level when the TDB or the TX Status and Control Register may be loaded with the new data. TBMT=0 on any write access to TDB or TX Status and Control Register. TBMT returns high when the TDSR is loaded.
36	TSA	Transmitter Status Available	O	TERR bit, indicating transmitter underflow. Reset by MR or assertion of TSOM.
37	TXENA	Transmitter Enable	I	A high level input allows the processing of transmitter data.
38	TSO	Transmitter Serial Output	O	This output is the transmitted character.
39	TCP	Transmitter Clock	I	The positive going edge of this clock shifts data out of the transmitter shift register.
40	MSEL	Maintenance Select	I	Internally RSI becomes TSO and RCP becomes $\overline{TCP}$. Externally RSI is disabled and TSO=1.

Wire "OR" with DBØØ-DBØ7 For 8 bit data bus

Definition of Terms
Register Bit Assignment Chart 1 and 2

Data Bus	Term	Definition
DBØ8	RSOM	Receiver Start of Message—read only bit. In BOP mode only, goes high when first non-flag (address byte) character loaded into RDB. It is cleared when the second byte is loaded into the RDB.
DBØ9	REOM	Receiver End of Message—read only bit. In BOP mode only, set high when last byte of data loaded into RDB, or when an ABORT character is received. It is cleared on reading of Receiver Status Register or dropping of RXENA.
DB1Ø	RAB/GA	Received ABORT or GO AHEAD character, read only bit. In BOP mode only, if LM=0 this bit is set on receiving an ABORT character; if LM=1 this bit is set on receiving a GO AHEAD character. This is cleared on reading of Receiver Status Register or dropping of RXENA.
DB11	ROR	Receiver Over Run—read only bit. Set high when received data transferred into RDB and previous data has not been read, indicating failure to service RDA within one character time. Cleared on reading of Receiver Status Register or dropping of RXENA.
DB12-14	A, B, C	Assembled Bit Count—read only bits. In BOP mode only, examine when REOM=1. ABC=0, message terminated on stated boundary. ABC=XXX, message terminated (by FLAG or GA) on unstated boundary, binary value of ABC = number of valid bits available in RDB (right hand justified).
DB15	ERR CHK	Error Check—read only bit. In BOP set high if CRC selected and received in error, examine when REOM=1. In CCP mode: 1. set high if parity selected and received in error, 2. if CRC selected (tested at end of each byte) ERR CHK = 1 if CRC GOOD, ERR CHK = 0 if CRC NOT GOOD. Controller must determine the last byte of the message.

Receiver Status Register

DB8	TSOM	Transmitter Start of Message—W/R bit. Provided TXENA=1, TSOM initiates start of message. In BOP, TSOM=1 generates FLAG and continues to send FLAG's until TSOM=0, then begin data. In CCP: 1. IDLE=0, transmit out of SYNC register, continue until TSOM=0, then begin data. 2. IDLE=1 transmit out of TDB. In BOP mode there is also a Special Space Sequence of 16-0's initiated by TSOM=1 and TEOM=1. SSS is followed by FLAG.
DB9	TEOM	Transmit End of Message—W/R bit. Used to terminate a message. In BOP mode, TEOM=1 sends CRC, then FLAG; if TXENA=1 and TEOM=1 continue to send FLAG's, if TXENA=0 and TEOM=1 MARK line. In CCP: 1. IDLE=0, TEOM=1 send SYNC, if TXENA=1 and TEOM=1 continue to send SYNC's, if TXENA=0 and TEOM=1 MARK line. 2. IDLE=1, TEOM=1, MARK line.
DB1Ø	TXAB	Transmitter Abort—W/R bit. In BOP mode only, TXAB=1 finish present character then: 1. IDLE=0, transmit ABORT 2. IDLE=1, transmit FLAG.
DB11	TXGA	Transmit Go Ahead—W/R bit. In BOP mode only, modifies character called for by TEOM. GA sent in place of FLAG. Allows loop termination—GA character.
DB15	TERR	Transmitter Error—read only bit. Underflow, set high when TDB not loaded in time to maintain continuous transmission. In BOP automatically transmit: 1. IDLE=0, ABORT 2. IDLE=1, FLAG. In CCP automatically transmit: 1. IDLE=0, SYNC 2. IDLE=1, MARK. Cleared by TSOM.

Transmitter Status and Control Register

DB8-1Ø	X,Y,Z	Z	Y	X	—W/R bits. These are the error control bits.
		0	0	0	$X^{16}+X^{12}+X^5+1$ CCITT—Initialize to "1"
		0	0	1	$X^{16}+X^{12}+X^5+1$ CCITT—Initialize to "0"
		0	1	0	Not used
		0	1	1	$X^{16}+X^{15}+X^2+1$—CRC16
		1	0	0	Odd Parity—CCP Only
		1	0	1	Even Parity—CCP Only
		1	1	0	Not Used
		1	1	1	Inhibit all error detection and transmission

Note: Do not modify XYZ until both data paths are idle

DB11	IDLE	IDLE mode select—W/R bit. Affects transmitter only. In BOP—control the type of character sent when TXAB asserted or in the event of data underflow. In CCP—controls the method of initial SYNC character transmission and underflow, "1" = transmit SYNC from TDB, "0"=transmit SYNC from SYNC/ADDRESS register.
DB12	SEC ADD	Secondary Address Mode—W/R bit. In BOP mode only—after FLAG looks for address match prior to activating RDP, if no match found, begin FLAG search again. SEC ADD bit should not be set if EXADD=1 or EXCON=1.
DB13	STRIP SYNC/LOOP	Strip Sync or Loop Mode—W/R bit. Effects receiver only. In BOP mode—allows recognition of a GA character. In CCP—after second SYNC, strip SYNC; when first data character detected, set RXACT=1, stop stripping.
DB14	PROTOCOL	PROTOCOL—W/R bit. BOP=0, CCP=1
DB15	*APA	All Parties Address—W/R bit. If selected, modifies secondary mode so that the secondary address or 8-1's will activate the RDP.

Mode Control Register

DB13-15 TXDL — Transmitter Data Length—W/R bits.

TXDL3	TXDL2	TXDL1	LENGTH
0	0	0	Eight bits per character
1	1	1	Seven bits per character
1	1	0	Six bits per character
1	0	1	Five bits per character
1	0	0	Four bits per character*
0	1	1	Three bits per character*
0	1	0	Two bits per character*
0	0	1	One bit per character*

*For data length only, not to be used for SYNC character (CCP mode).

DB8-1Ø RXDL — Receiver Data Length—W/R bits.

RXDL3	RXDL2	RXDL1	LENGTH
0	0	0	Eight bits per character
1	1	1	Seven bits per character
1	1	0	Six bits per character
1	0	1	Five bits per character
1	0	0	Four bits per character
0	1	1	Three bits per character
0	1	0	Two bits per character
0	0	1	One bit per character

Data Length Select Register

DB11	EXCON	Extended Control Field—W/R bit. In receiver only; if set, will receive control field as two 8-bit bytes. Excon bit should not be set if SEC ADD =1.
DB12	EXADD	Extended Address Field—W/R bit. In receiver only; LSB of address byte tested for a "1". If NO—continue receiving address bytes, if YES go into control field. EXADD bit should not be set if SEC ADD =1.

*Note: Product manufactured before 1Q79 may not have this feature.

Register Bit Assignment Chart 1

REGISTER	DPØ7	DPØ6	DPØ5	DPØ4	DPØ3	DPØ2	DPØ1	DPØØ
Receiver Data Buffer (Read Only- Right Justified- Unused Bits=0)	RD7 MSB	RD6	RD5	RD4	RD3	RD2	RD1	RDØ LSB
Transmitter Data Register (Read/Write- Unused Inputs=X)	TD7 MSB	TD6	TD5	TD4	TD3	TD2	TD1	TDØ LSB
Sync/Secondary Address (Read/Write- Right Justified- Unused Inputs=X)	SSA7 MSB	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSAØ LSB

Register Bit Assignment Chart 2

REGISTER	DP15	DP14	DP13	DP12	DP11	DP1Ø	DPØ9	DPØ8
Receiver Status (Read Only)	ERR CHK	C	B	A	ROR	RAB/GA	REOM	RSOM
TX Status and Control (Read/Write)	TERR (Read Only)	0	0	0	TXGA	TXAB	TEOM	TSOM
Mode Control (Read/Write)	*APA	PROTOCOL	STRIP SYNC/ LOOP	SEC ADD	IDLE	Z	Y	X
Data Length Select (Read/Write)	TXDL3	TXDL2	TXDL1	EXADD	EXCON	RXDL3	RXDL2	RXDL1

* Note: Product manufactured before 1Q79 may not have this feature.

Register Address Selection

1) BYTE OP = 0, data port 16 bits wide

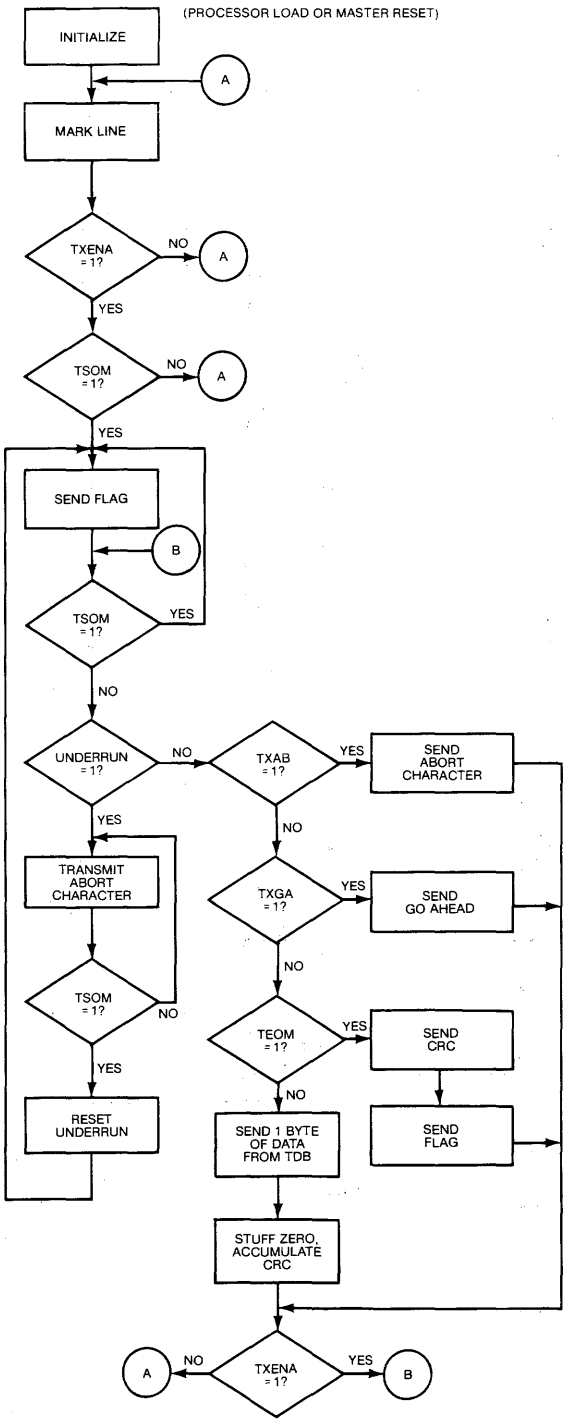
A2	A1	AØ	Register
0	0	X	Receiver Status Register and Receiver Data Buffer
0	1	X	Transmitter Status and Control Register and Transmitter Data Buffer
1	0	X	Mode Control Register and SYNC/Address Register
1	1	X	Data Length Select Register

X = don't care

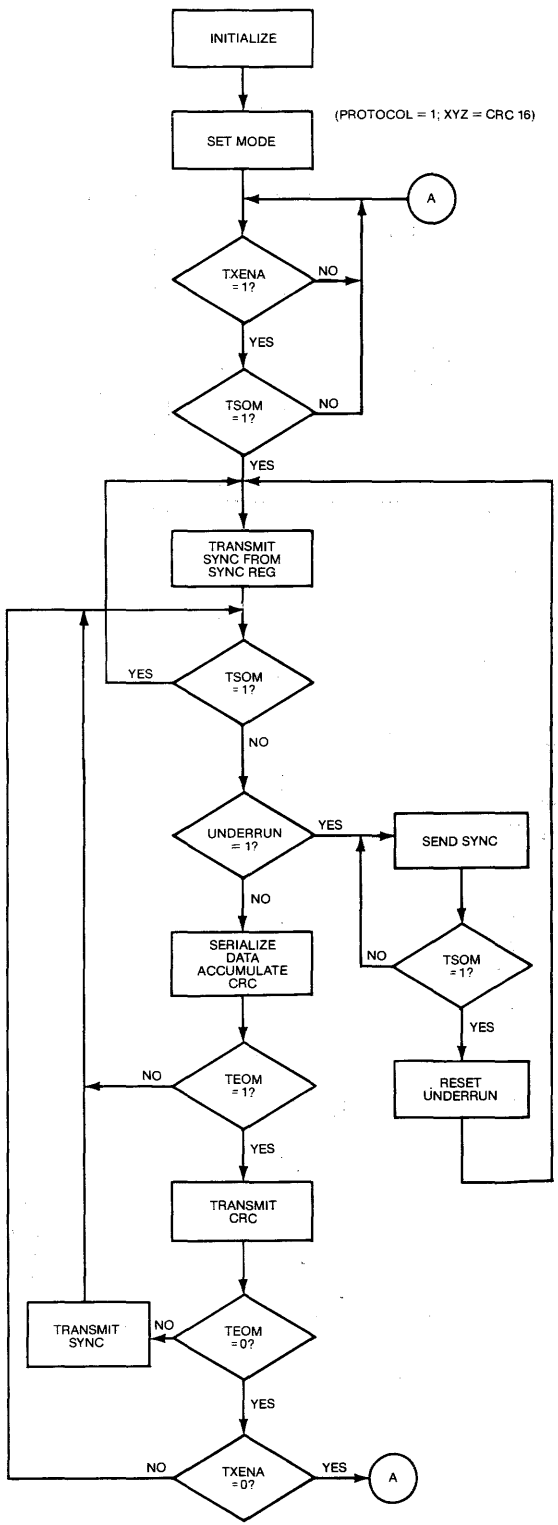
2) BYTE OP = 1, data port 8 bits wide

A2	A1	AØ	Register
0	0	0	Receiver Data Buffer
0	0	1	Receiver Status Register
0	1	0	Transmitter Data Buffer
0	1	1	Transmitter Status and Control Register
1	0	0	SYNC/Address Register
1	0	1	Mode Control Register
1	1	0	———————
1	1	1	Data Length Select Register

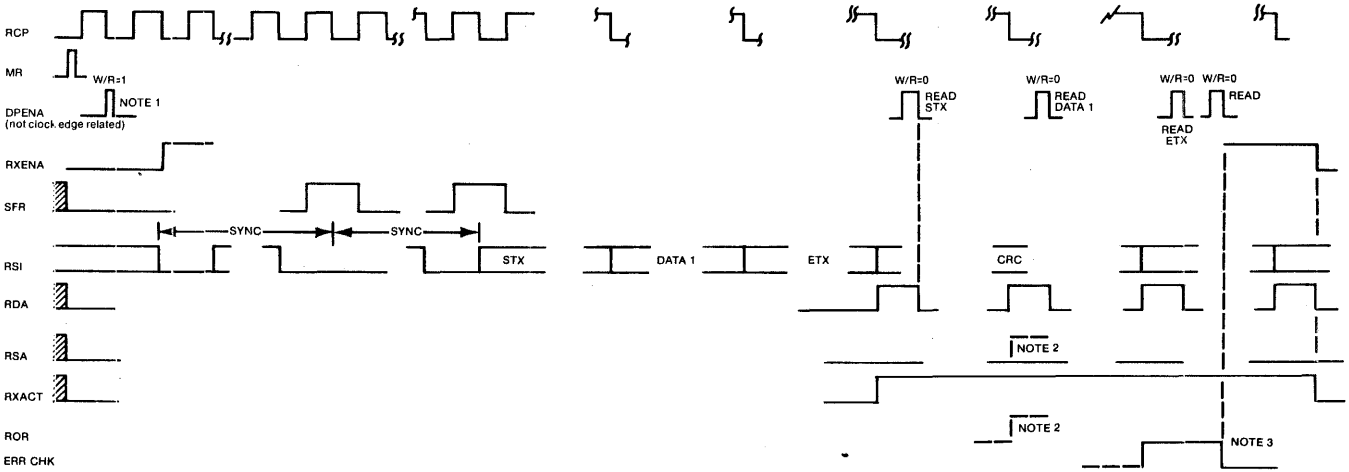
BOP TRANSMITTER OPERATION



CCP TRANSMITTER OPERATION

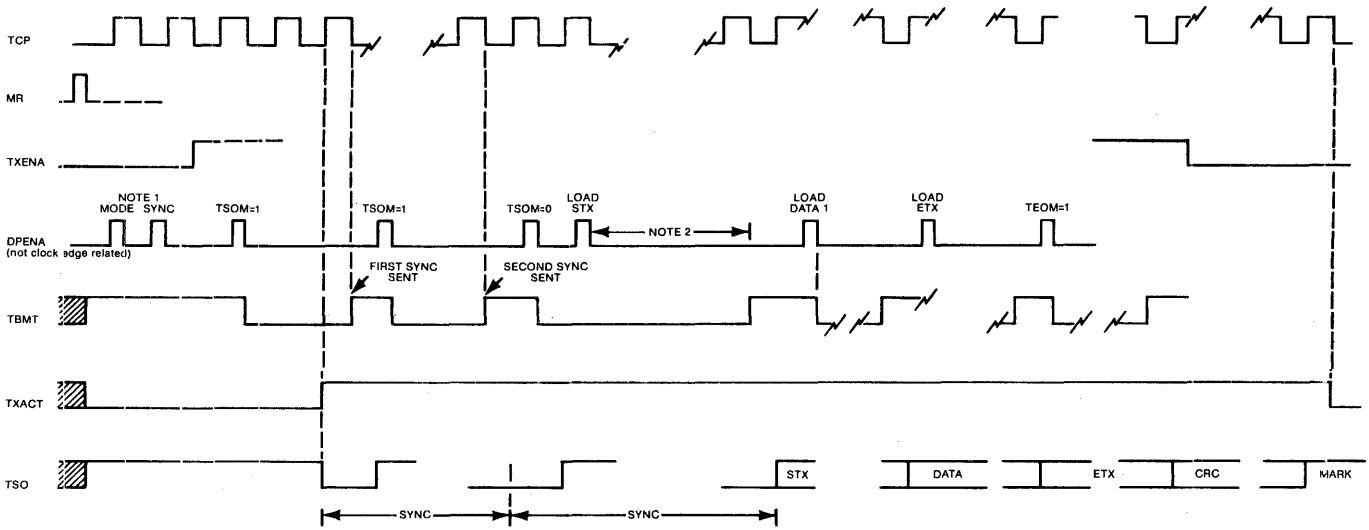


CCP RECEIVER TIMING



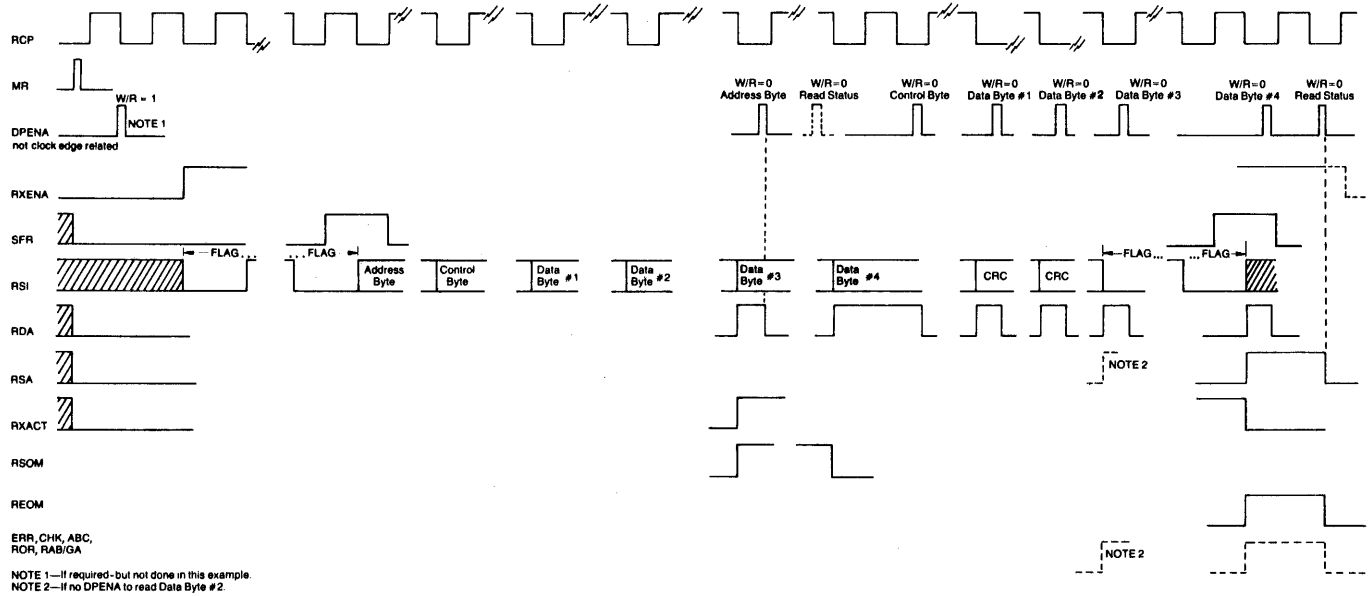
NOTE 1— Mode set for CCP with CRC selected
NOTE 2— If overrun had occured — no READ STX
NOTE 3— ERR CHK must be sampled before next byte or before RXENA brought low

CCP TRANSMITTER OPERATION



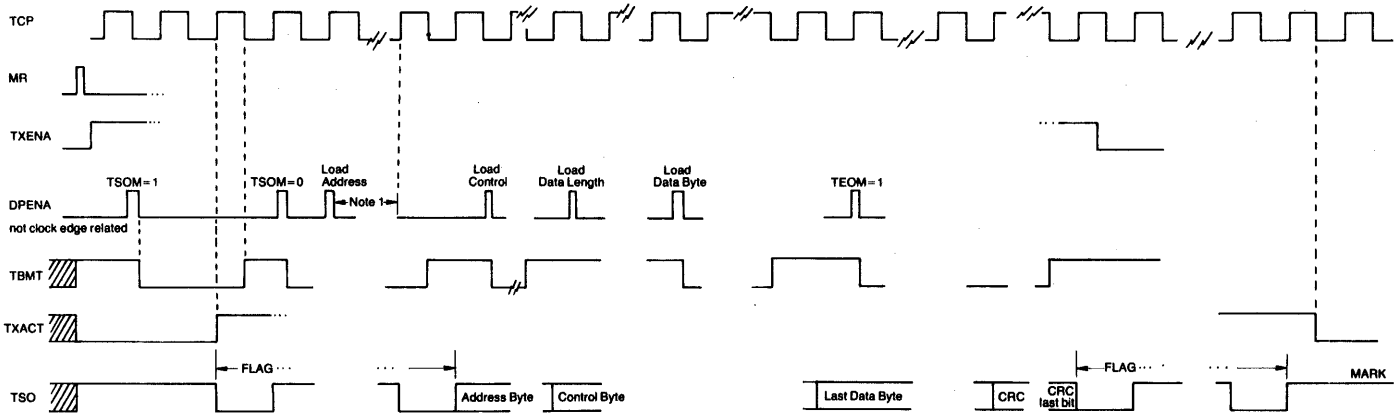
NOTE 1—Mode is CCP with CRC selected
NOTE 2—Trailing edge of DPENA must occur at least one-half clock pulse prior to TBMT=1 to avoid underrun

BOP RECEIVER TIMING



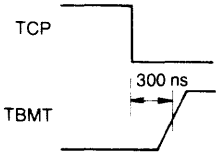
NOTE 1—If required - but not done in this example.
NOTE 2—If no DPENA to read Data Byte #2.

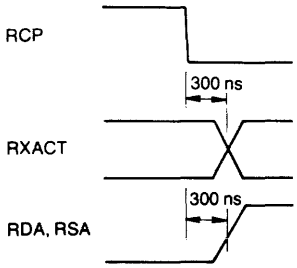
BOP TRANSMITTER OPERATION

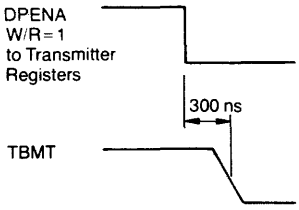


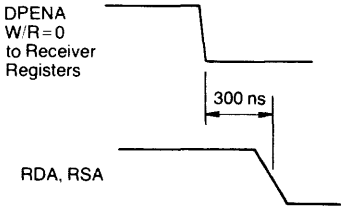
Note 1—Trailing edge of DPENA must occur at least one-half clock pulse prior to TBMT = 1. To avoid underrun.

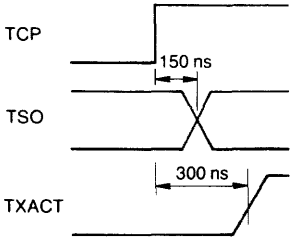
AC TIMING DIAGRAMS







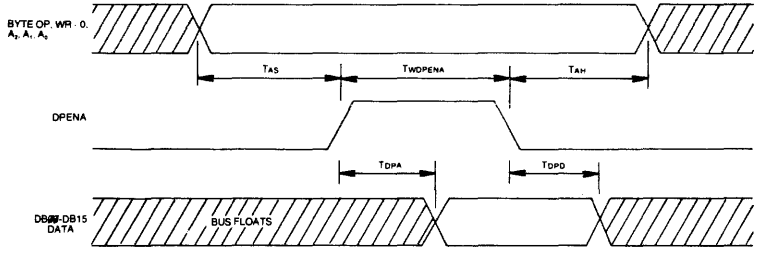




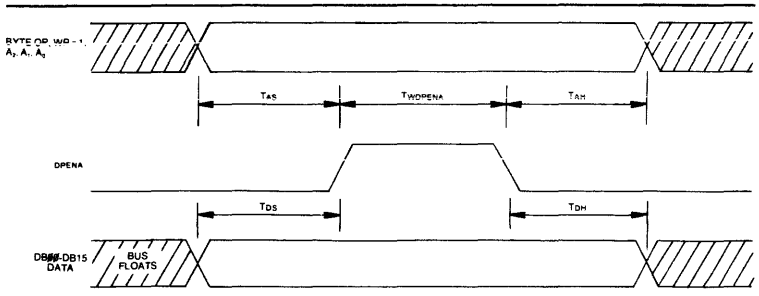
Resets: RDP-RDA, RSA, RXACT, receiver into search mode (for FLAG)

Note: Unless otherwise specified all times are maximum.

Data Port Timing



READ FROM USYNR/T



WRITE TO USYNR/T

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

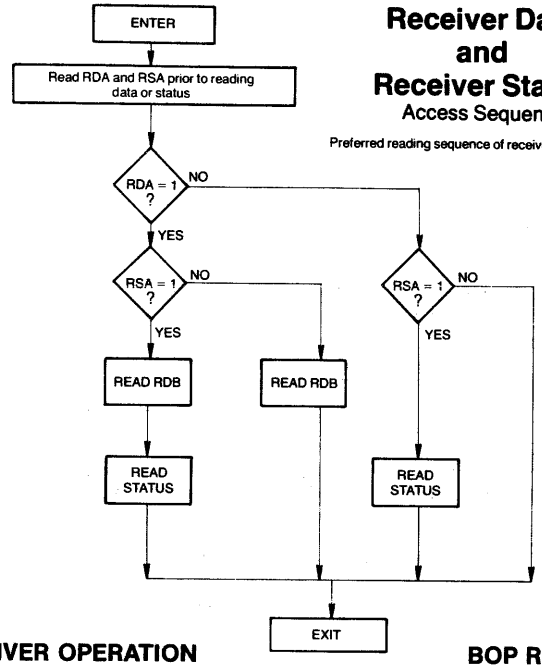
ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, V_{DD}=+12V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. Characteristics					
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	2.0		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low Level, V_{OL}			0.4	V	I_{OL}=1.6ma
High Level, V_{OH}	2.4				I_{OH}=40μa
INPUT LEAKAGE					
Data Bus		5.0	50.0	μa	0≤V_{IN}≤5v, DPENA=0 or W/R=I
All others				μa	V_{IN}=+5v
INPUT CAPACITANCE					
Data Bus, C_{IN}				pf	
Address Bus, C_{IN}				pf	
Clock, C_{IN}				pf	
All other, C_{IN}				pf	
POWER SUPPLY CURRENT					
I_{CC}			70	ma	
I_{DD}			90	ma	
A.C. Characteristics					T_A=25°C
CLOCK-RCP, TCP					
frequency	DC		1.5	MHz	
PW_H	325			ns	
PW_L	325			ns	
t_r, t_f		10		ns	
DPENA, T_{WDPENA}	250		50 μs	ns	
Set-up Time, T_{AS}	0			ns	
Byte Op, W/R					
A_2, A_1, A_0					
Hold Time, T_{AH}	0			ns	
Byte Op, WIR,					
A_2, A_1, A_0					
DATA BUS ACCESS, T_{DPA}			150	ns	
DATA BUS DISABLE DELAY, T_{DPD}			100	ns	
DATA BUS SET-UP TIME, T_{DBS}	0			ns	
DATA BUS HOLD TIME, T_{DBH}	100			ns	
MASTER RESET, MR	350			ns	

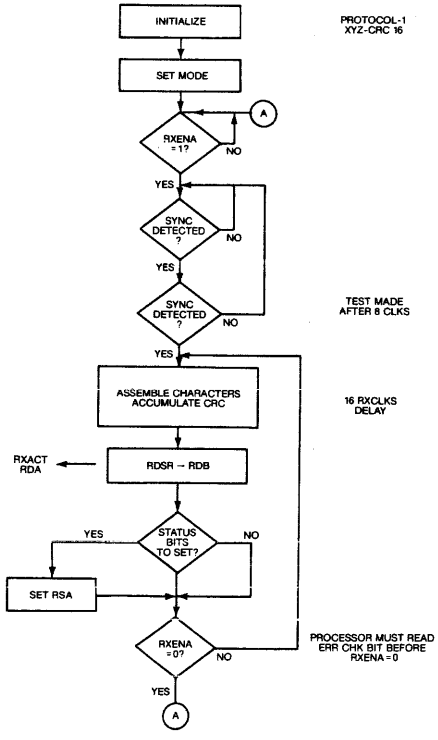
Receiver Data and Receiver Status

Access Sequence

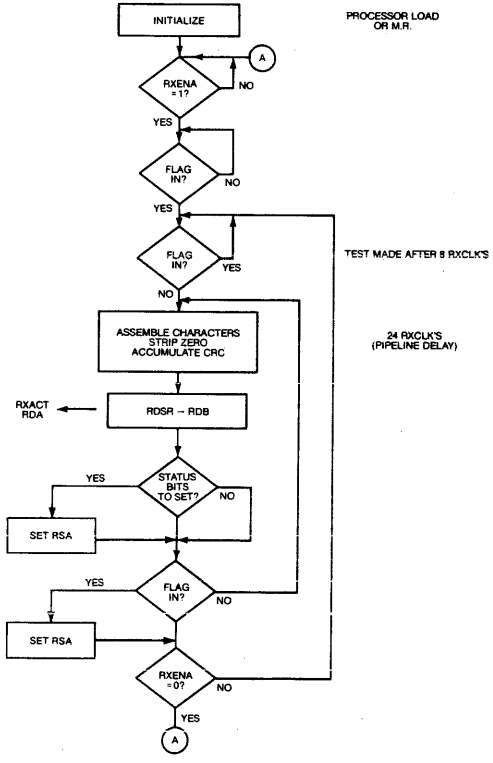
Preferred reading sequence of receiver RDA and RSA.



CCP RECEIVER OPERATION



BOP RECEIVER OPERATION



STANDARD MICROSYSTEMS CORPORATION

COM 7210

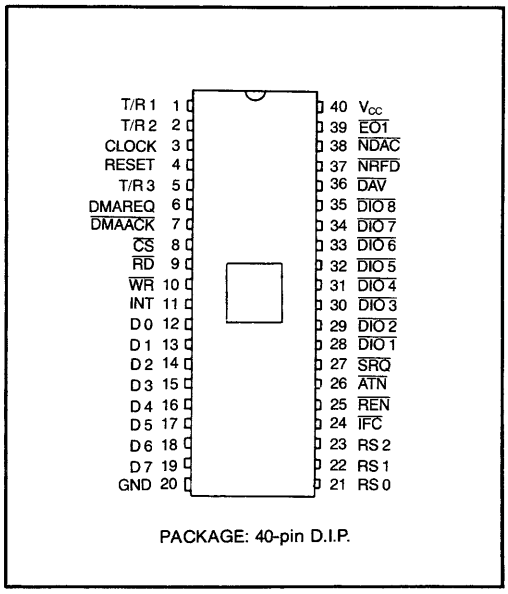
PRELIMINARY

Intelligent GPIB Interface Controller

FEATURES

- ☐ All Functional Interface Capability Meeting IEEE Standard 488-1978
  - —SH1 (Source Handshake)
  - —AH1 (Acceptor Handshake)
  - —T5 or TE5 (Talker or Extended Talker)
  - —L3 or LE3 (Listener or Extended Listener)
  - —SR1 (Service Request)
  - —RL1 (Remote Local)
  - —PP1 or PP2 (Parallel Poll) (Remote or Local Configuration)
  - —DC1 (Device Clear)
  - —DT1 (Device Trigger)
  - —C1-5 ((Controller) (All Functions))
- ☐ Programmable Data Transfer Rate
- ☐ 16 MPU Accessible Registers—8 Read/8 Write
- ☐ 2 Address Registers
  - —Detection of MTA, MLA, MSA (My Talk/Listen/ Secondary Address)
  - —2 Device Addresses
- ☐ EOS Message Automatic Detection
- ☐ Command (IEEE Standard 488-78) Automatic Processing and Undefined Command Read Capability
- ☐ DMA Capability
- ☐ Programmable Bus Transceiver I/O Specification (Works with T.I./Motorola/Intel)
- ☐ 1 to 8 MHz Clock Range
- ☐ TTL Compatible

PIN CONFIGURATION



PACKAGE: 40-pin D.I.P.

- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ +5V Single Power Supply
- ☐ 40-Pin DIP
- ☐ 8080/85/86 Compatible

GENERAL DESCRIPTION

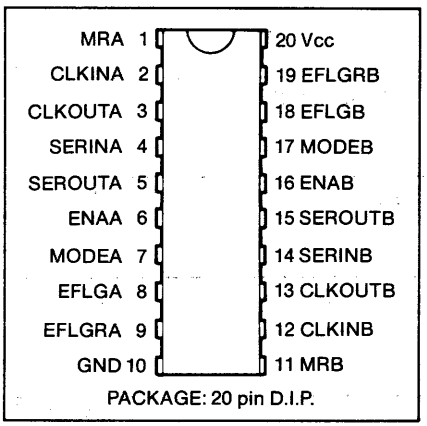
The COM7210 TLC is an intelligent GPIB Interface Controller designed to meet all of the functional requirements for Talkers, Listeners, and Controllers as specified by the IEEE Standard 488-1978. Connected between a processor bus and the GPIB, the TLC provides high level management of the GPIB to unburden the processor and to simplify both hardware and software design. Fully compatible with most processor architectures, Bus Driver/Receivers are the only additional components required to implement any type of GPIB interface.

Dual 32 Bit CRC SDLC Generator/Checker CRC-32

FEATURES

- ☐ SDLC 32 bit CRC
- ☐ COM 5025 USYNRT Companion
- ☐ Data Rate—2MHz typical
- ☐ All Inputs and Outputs are TTL Compatible
- ☐ Single +5 Volt Supply
- ☐ COPLAMOS® N-Channel MOS Technology

PIN CONFIGURATION



PACKAGE: 20 pin D.I.P.

GENERAL DESCRIPTION

SMC's COM 8004 is a dual 32-bit CRC Generator/Checker for use with SDLC protocols. It is a companion device to SMC's COM 5025 USYNRT. It operates at bit rates from DC to 2.0 MHz from a single +5v supply and is housed in a 20 lead x 0.3 inch DIP. All inputs and outputs are TTL compatible with full noise immunity.

The COM 8004 is comprised of two independent halves, and each half may be operated in the check or generate mode. The polynominal used in computations is:
$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$.

The CRC register is initialized to all ones and the result is inverted before being appended to the message. The expected remainder is:
$X^{31} + X^{30} + X^{26} + X^{25} + X^{24} + X^{18} + X^{15} + X^{14} + X^{12} + X^{11} + X^{10} + X^8 + X^6 + X^5 + X^4 + X^3 + X + 1$.

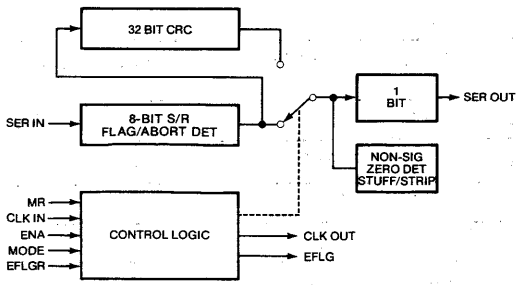
Each half has a nine-bit serial data shift register. Data moves on the positive edge of the clock, and all clocked inputs are designed for zero-hold-time (e.g. 7474). A "clock out" pin provides gated clocks to the accompanying USYNRT (COM 5025).

In the generate mode, computation is initiated upon detection of a flag character in the serial bit stream. CRC computation proceeds upon the serial data until a second flag is detected. CLK OUT to the SDLC transmitter is then halted, and the 32-bit CRC is passed out; CLK OUT is then resumed, and the flag character is passed out. Nonsignificant zeros are automatically stripped and stuffed, and shared flags are supported. If the data between flags is less than two full bytes, the CRC is discarded and the serial data stream remains unaltered.

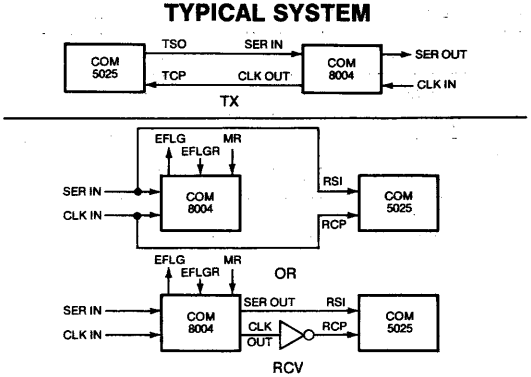
In the check mode, computation is similarly initiated upon detection of a flag. Detection of a second flag causes the conditional setting of the error flag. A separate reset pin is provided for the error flag. No error is flagged on messages of less than two full bytes between flags. Detection of an abort character (7 consecutive ones) in either mode causes computation to be reset and a search for an opening flag resumed.

BLOCK DIAGRAM

FOR ONE-HALF OF THE COM 8004



TYPICAL SYSTEM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	MASTER RESET-A	MRA	MRA presets the CRC calculation in Section A of the COM 8004 to all ones and forces the "pipeline" (8 shift register bits and the output flip-flop) to a logic "1" (Mark). The COM 8004 will only exit the reset state when MRA has been released and all 8 bits of a FLAG (01111110) have been received.
2	CLOCK INPUT-A	CLKINA	Baud Rate Clock for Section A.
3	CLOCK OUTPUT-A	CKLOUTA	Clock output from Section A. This is used to provide the clock for the USYNRT. CLKOUTA will normally track CLKINA. In the generate mode, when the last flag bit has been shifted into the shift register of the COM 8004, CLKOUTA will be held high until the CRC check character has been sent out. After the last bit of the CRC character is transmitted, CLKOUTA will resume tracking CLKINA.
4	SERIAL INPUT-A	SERINA	Serial input to the COM 8004 Section A. For transmission, SERINA is connected to the transmitter serial output of the USYNRT. For receiving, SERINA is connected to the received data output of the modem.
5	SERIAL OUTPUT-A	SEROUTA	Serial output from Section A of the COM 8004. For transmission, SEROUTA is connected to the transmit data input of the modem. For receiving, SEROUTA may be connected to the serial data input of the USYNRT.
6	ENABLE-A	ENAA	When ENAA is low, section A of the COM 8004 will pass data from SERINA to SEROUTA after a nine bit delay without alteration and without checking or generating CRC. If ENAA is high, CRC generation or checking will be enabled. ENAA is gated into the COM 8004 by the rising edge of CLKINA.
7	MODE SELECT-A	MODEA	MODEA determines whether Section A of the COM 8004 is in the receive (CRC check) Mode or transmit (CRC generate) Mode. Logic "1" selects CRC check. Logic "0" selects CRC generate.
8	ERROR FLAG-A	EFLGA	EFLGA will go high if, when in the CRC check mode, section A of the COM 8004 has detected an error. EFLGA can only be reset by a MASTER RESET (MRA) or by ERROR FLAG RESET (EFLGRA).
9	ERROR FLAG RESET-A	EFLGRA	A logic "1" on EFLGRA will reset EFLGA. If EFLGRA is kept at a logic "1," it will inhibit the setting of EFLGA.
10	GROUND	GND	Ground.
11	MASTER RESET-B	MRB	Master reset for Section B. See MRA for description.
12	CLOCK IN-B	CLKINB	Clock input for Section B. See CLKINA for description.
13	CLOCK OUT-B	CLKOUTB	Clock output for Section B. See CLKOUTA for description.
14	SERIAL INPUT-B	SERINB	Serial input for Section B. See SERINA for description.
15	SERIAL OUTPUT-B	SEROUTB	Serial output for Section B. See SEROUTA for description.
16	ENABLE-B	ENAB	CRC enable for Section B. See ENAA for description.
17	MODE SELECT-B	MODEB	Mode select for Section B. See MODEA for description.
18	ERROR FLAG-B	EFLGB	Error Flag for Section B. See EFLGA for description.
19	ERROR FLAG RESET-B	EFLGRB	Error flag reset for Section B. See EFLGRA for description.
20	POWER SUPPLY	V_{CC}	+5 volt power supply input.

OPERATION

The COM 8004 has 3 modes of operation, as selected by the ENABLE and MODE SELECT inputs. They are:

ENABLE	MODE SELECT	
0	0	CRC Disabled. Data is shifted from SERIN to SEROUT with no computation performed. Serial delay is 9 bit times.
0	1	Same as above.
1	0	CRC generation mode.
1	1	CRC check mode.

In the CRC generation and check modes, calculations begin upon receipt of the first data character after an opening FLAG. "Stuffed zeroes" are stripped for the purpose of the CRC calculation. CRC calculation will continue until either a MASTER RESET occurs, ENABLE is brought to logic zero, an ABORT character is received, or a closing FLAG is received.

CRC Generation

Upon detection of a closing FLAG character, CLKOUT is left high (stopping USYNRT activity), and the CRC accumulation is shifted out by CLKIN. CLKOUT then resumes clocking, and the FLAG (which has been stored in the shift register) is shifted out. The CRC check data is inverted before this data is transmitted. Zero-stuffing is performed on the inverted CRC check data.

During the time CKLOUT is forced high and CRC check data is being shifted out, data on SERIN will be ignored.

If an ABORT character is received, CRC calculation will cease after the last "1" bit of the ABORT character is shifted into the shift register. Data will pass through the COM 8004 without effect until a FLAG is received.

CRC Check (Reception)

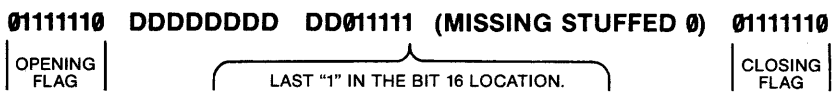
When the last bit of a closing flag enters the shift register, ERRCHK will go high on the following positive CLKIN transition if a CRC error is detected.

SECTION III

Operation Notes

Note 1: The minimum message size is sixteen significant bits following an opening flag. A stuffed zero is not considered a significant bit. If the message is less than 16 bits, the data will pass through the COM 8004 without being affected.

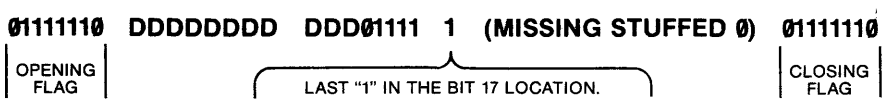
If the sixteenth received bit is the fifth consecutive one, but is not followed by a stuffed zero before a FLAG, the COM 8004 will detect the FLAG but the minimum message will not have occurred. CRC calculation will begin anew after this FLAG is detected.



Note 2: If the seventeenth bit of a message followed by a FLAG is the fifth consecutive one, but the stuffed zero is missing, the following will occur:

A) CRC Generate Mode: The last "one" bit, bit 17, will not be calculated into the CRC, but will appear at the serial output. The first bit of the CRC character will be forced to a zero, therefore looking like a stuffed zero.

B) CRC Check Mode: The last "one" bit, bit 17, will not be calculated into the CRC.



Note 3: If a stuffed zero is missing in the middle or end of a message, the reaction will depend on the next bit. If it is a one, a FLAG or ABORT may be detected. If an ABORT is detected, the message and the CRC checking is aborted. If a FLAG is detected, a CRC error will be detected.

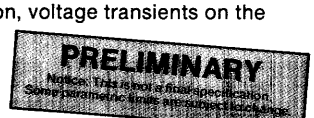
If the missing zero is followed by a zero, the CRC computation will continue, but the zero bit will be stripped, causing a CRC error.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... -0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.



ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5 Volts ±5%, unless otherwise noted)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS						
Input Voltage Levels						
Low Level	V_{IL}			0.8	V	
High Level	V_{IH}	2.0			V	
Output Voltage Levels						
Low Level	V_{OL}			0.4	V	I_{OL} = 1.6 mA
High Level	V_{OH}	2.4			V	I_{OH} = -100 μA
Input Capacitance	C_{IN}		10	25	pf	
Power Supply Current	I_{CC}			100	mA	
AC CHARACTERISTICS						T_A = 25°C
Clock Frequency	f_{IN}			2	MHz	
Clock Pulse Width—High	t_{CLKH}	350			ns	Figure 1
Input Set-Up Time	t_{DC}	100			ns	Figure 1
Input Hold Time	t_{CD}	0			ns	Figure 1
Master Reset Pulse Width	t_{PW}	250			ns	Figure 2
Reset Delay	t_{MR}			250	ns	Figure 2
Error Flag Delay	t_{FD}			300	ns	Figure 3
Error Flag Reset Delay	t_{FR}			100	ns	Figure 4
ERRST Pulse Width	t_{EW}	100			ns	Figure 4
Clock Propagation Delay	t_{PD}			150	ns	Figure 5
SEROUT Propagation Delay	t_{SD}			150	ns	Figure 5

Figure 1

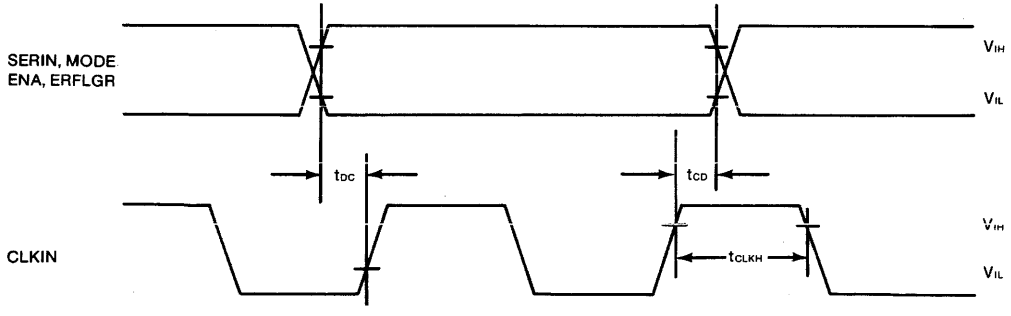


Figure 2

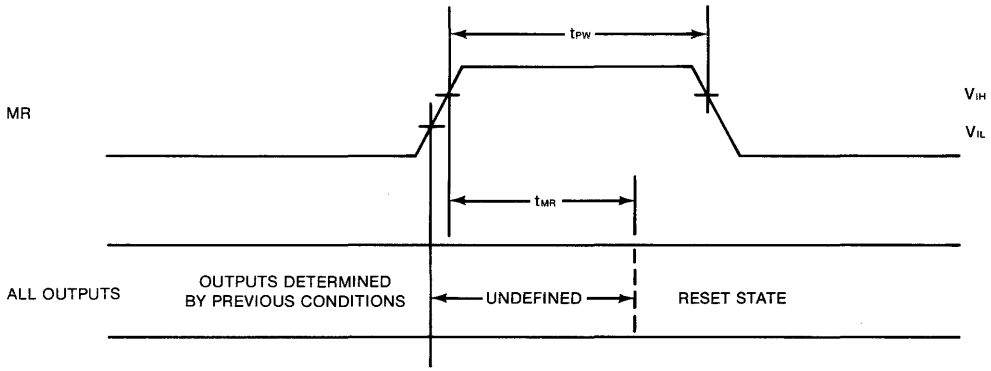


Figure 3

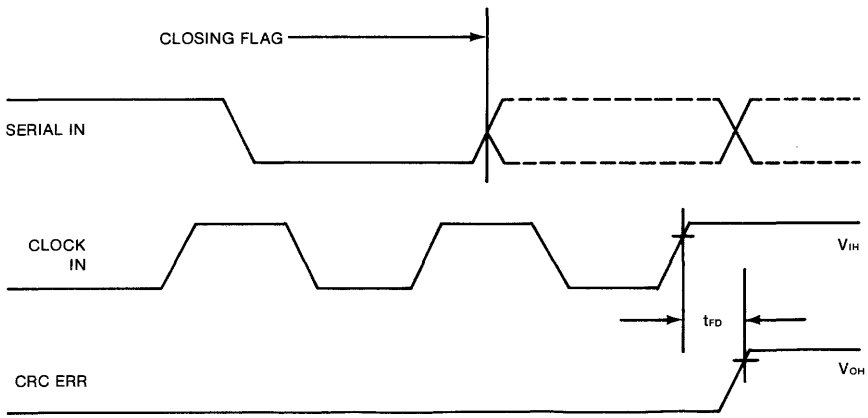


Figure 4

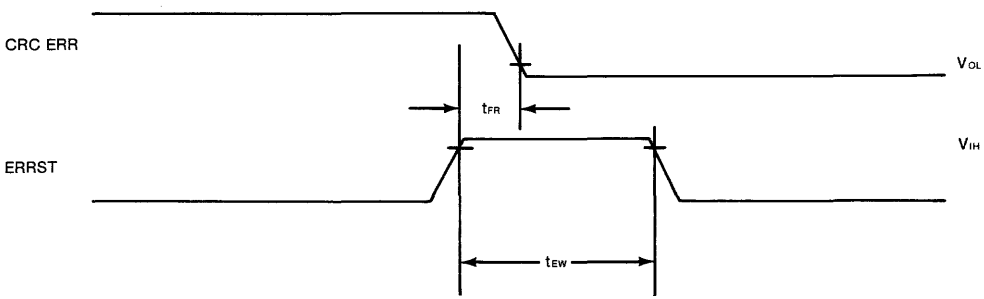
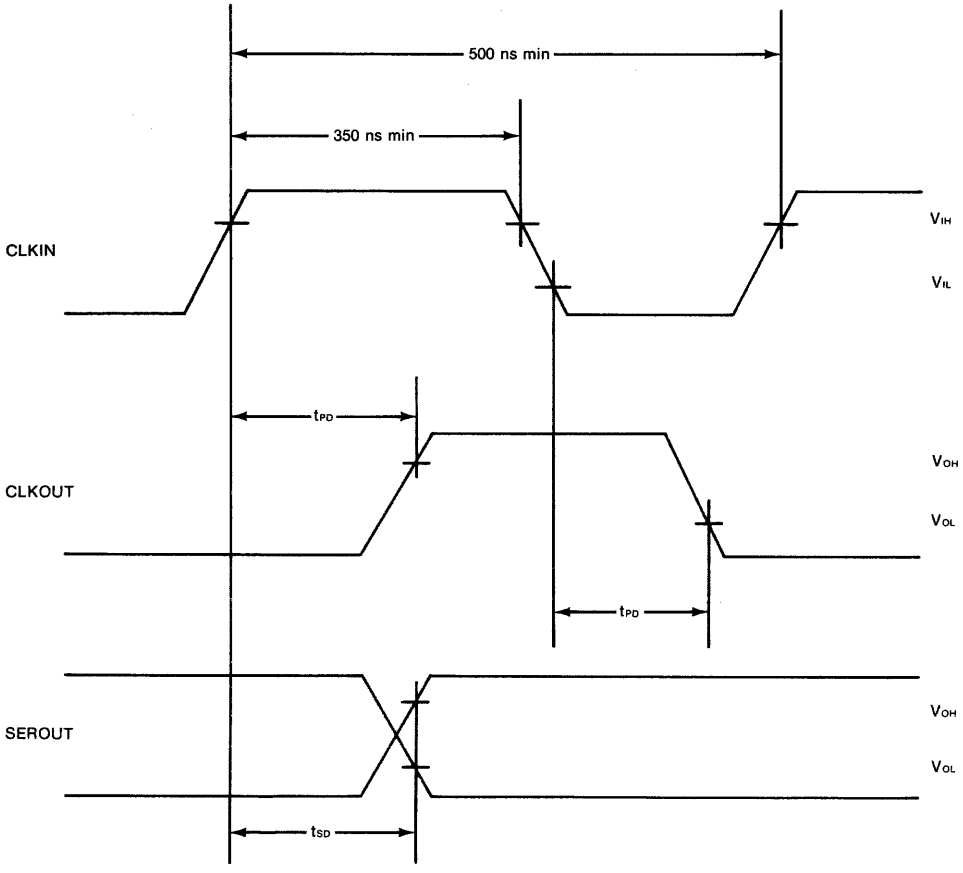


Figure 5



STANDARD MICROSYSTEMS CORPORATION

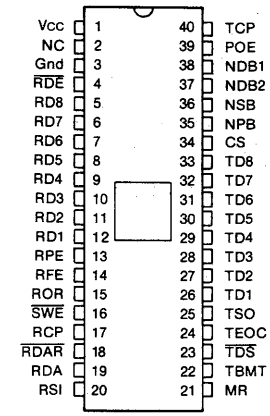
COM 8017
COM 8502

Universal Asynchronous Receiver/Transmitter
UART

FEATURES

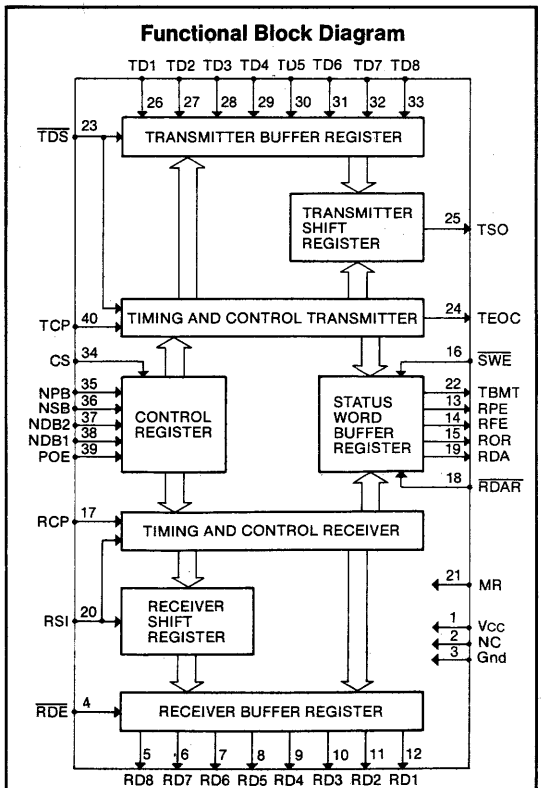
- ☐ Single +5V Power Supply
- ☐ Direct TTL Compatibility—no interfacing circuits required
- ☐ Full or Half Duplex Operation—can receive and transmit simultaneously at different baud rates
- ☐ Fully Double Buffered—eliminates need for precise external timing
- ☐ Start Bit Verification—decreases error rate
- ☐ Fully Programmable—data word length; parity mode; number of stop bits: one, one and one-half, or two
- ☐ High Speed Operation—40K baud, 200ns strobes
- ☐ Master Reset—Resets all status outputs
- ☐ Tri-State Outputs—bus structure oriented
- ☐ Low Power—minimum power requirements
- ☐ Input Protected—eliminates handling problems
- ☐ Ceramic or Plastic Dip Package—easy board insertion
- ☐ Compatible with COM 2017, COM 2502
- ☐ Compatible with COM 8116, COM 8126, COM 8136, COM 8146, COM 8046 Baud Rate Generators

Pin Configuration



PACKAGE: 40-Pin D.I.P.

Functional Block Diagram



GENERAL DESCRIPTION

The Universal Asynchronous Receiver/Transmitter is an MOS/LSI monolithic circuit that performs all the receiving and transmitting functions associated with asynchronous data communications. This circuit is fabricated using SMC's patented COPLAMOS® technology and employs depletion mode loads, allowing operation from a single +5V supply. The duplex mode, baud rate, data word length, parity mode, and number of stop bits are independently programmable through the use of external controls. There may be 5, 6, 7 or 8 data bits, odd/even or no parity, and 1, or 2 stop bits. In addition the COM 8017 will provide 1.5 stop bits when programmed for 5 data bits and 2 stop bits. The UART can operate in either the full or half duplex mode. These programmable features provide the user with the ability to interface with all asynchronous peripherals.

DESCRIPTION OF OPERATION— TRANSMITTER

At start-up the power is turned on, a clock whose frequency is 16 times the desired baud rate is applied and master reset is pulsed. Under these conditions TBMT, TEOC, and TSO are all at a high level (the line is marking).

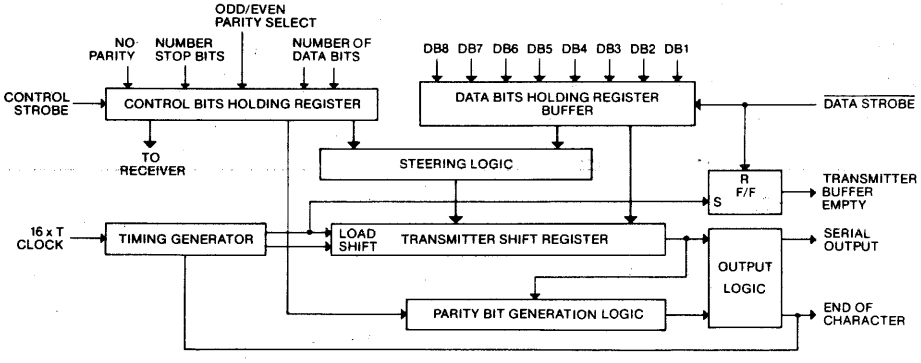
When TBMT and TEOC are high, the control bits may be set. After this has been done the data bits may be set. Normally, the control bits are strobed into the transmitter prior to the data bits. However, as long as minimum pulse width specifications are not violated, $\overline{TDS}$ and CS may occur simultaneously. Once the date strobe ($\overline{TDS}$) has been pulsed the TBMT signal goes low, indicating that the data bits buffer register is full and unavailable to receive new data.

If the transmitter shift register is transmitting previously loaded data the TBMT signal remains low. If the transmitter shift register is empty, or when it is through transmitting the previous character, the data in the buffer register is loaded immediately into the transmitter shift register and data transmission commences. TSO goes low (the start bit), TEOC goes low, the TBMT goes high indicating that the data in the data bits buffer register has been loaded into the transmitter shift register and that the data bits buffer register is available to be loaded with new data.

If new data is loaded into the data bits buffer register at this time, TBMT goes low and remains in this state until the present transmission is completed. One full character time is available for loading the next character with no loss in speed of transmission. This is an advantage of double buffering.

Data transmission proceeds in an orderly manner: start bit, data bits, parity bit (if selected), and the stop bit(s). When the last stop bit has been on the line for one bit time TEOC goes high. If TBMT is low, transmission begins immediately. If TBMT is high the transmitter is completely at rest and, if desired, new control bits may be loaded prior to the next data transmission.

TRANSMITTER BLOCK DIAGRAM



DESCRIPTION OF OPERATION—RECEIVER

At start-up the power is turned on, a clock whose frequency is 16 times the desired baud rate is applied and master reset is pulsed. The data available (RDA) signal is now low. There is one set of control bits for both the receiver and transmitter.

Data reception begins when the serial input line transitions from mark (high) to space (low). If the RSI line remains spacing for a 1/2 bit time, a genuine start bit is verified. Should the line return to a marking condition prior to a 1/2 bit time, the start bit verification process begins again. A mark to space transition must occur in order to initiate start bit verification. Once a start bit has been verified, data reception proceeds in an orderly manner: start bit verified and received, data bits received, parity bit received (if selected) and the stop bit(s) received.

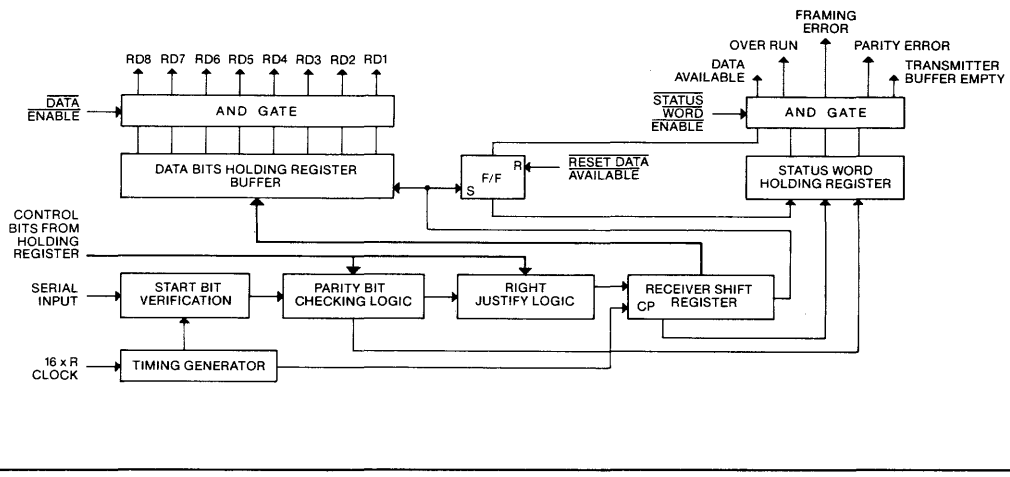
If the transmitted parity bit does not agree with the received parity bit, the parity error flip-flop of the

status word buffer register is set high, indicating a parity error. However, if the no parity mode is selected, the parity error flip-flop is unconditionally held low, inhibiting a parity error indication. If a stop bit is not received, due to an improperly framed character, the framing error flip-flop is set high, indicating a framing error.

Once a full character has been received internal logic looks at the data available (RDA) signal. If, at this instant, the RDA signal is high the receiver assumes that the previously received character has not been read out and the over-run flip-flop is set high. The only way the receiver is aware that data has been read out is by having the data available reset low.

At this time the RDA output goes high indicating that all outputs are available to be examined. The receiver shift register is now available to begin receiving the next character. Due to the double buffered receiver, a full character time is available to remove the received character.

RECEIVER BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
1	V_{CC}	Power Supply	+5 volt Supply
2	NC	No Connection	No Connection
3	GND	Ground	Ground
4	$\overline{RDE}$	Received Data Enable	A low-level input enables the outputs (RD8-RD1) of the receiver buffer register.
5-12	RD8-RD1	Receiver Data Outputs	These are the 8 tri-state data outputs enabled by $\overline{RDE}$. Unused data output lines, as selected by NDB1 and NDB2, have a low-level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output.
13	RPE	Receiver Parity Error	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the received character parity bit does not agree with the selected parity.
14	RFE	Receiver Framing Error	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the received character has no valid stop bit.

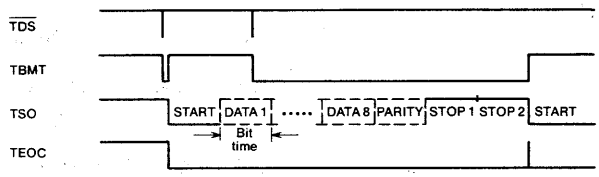
DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
15	ROR	Receiver Over Run	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the previously received character is not read (RDA output not reset) before the present character is transferred into the receiver buffer register.
16	$\overline{SWE}$	Status Word Enable	A low-level input enables the outputs (RPE, RFE, ROR, RDA, and TBMT) of the status word buffer register.
17	RCP	Receiver Clock	This input is a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	$\overline{RDAR}$	Receiver Data Available Reset	A low-level input resets the RDA output to a low-level.
19	RDA	Receiver Data Available	This tri-state output (enabled by $\overline{SWE}$) is at a high-level when an entire character has been received and transferred into the receiver buffer register.
20	RSI	Receiver Serial Input	This input accepts the serial bit input stream. A high-level (mark) to low-level (space) transition is required to initiate data reception.
21	MR	Master Reset	This input should be pulsed to a high-level after power turn-on. This sets TSO, TEOC, and TBMT to a high-level and resets RDA, RPE, RFE and ROR to a low-level.
22	TBMT	Transmitter Buffer Empty	This tri-state output (enabled by $\overline{SWE}$) is at a high-level when the transmitter buffer register may be loaded with new data.
23	$\overline{TDS}$	Transmitter Data Strobe	A low-level input strobe enters the data bits into the transmitter buffer register.
24	TEOC	Transmitter End of Character	This output appears as a high-level each time a full character is transmitted. It remains at this level until the start of transmission of the next character or for one-half of a TCP period in the case of continuous transmission.
25	TSO	Transmitter Serial Output	This output serially provides the entire transmitted character. TSO remains at a high-level when no data is being transmitted.
26-33	TD1-TD8	Transmitter Data Inputs	There are 8 data input lines (strobed by $\overline{TDS}$) available. Unused data input lines, as selected by NDB1 and NDB2, may be in either logic state. The LSB should always be placed on TD1.
34	CS	Control Strobe	A high-level input enters the control bits (NDB1, NDB2, NSB, POE and NPB) into the control bits holding register. This line may be strobed or hard wired to a high-level.
35	NPB	No Parity Bit	A high-level input eliminates the parity bit from being transmitted; the stop bit(s) immediately follow the last data bit. In addition, the receiver requires the stop bit(s) to follow immediately after the last data bit. Also, the RPE output is forced to a low-level. See pin 39, POE.

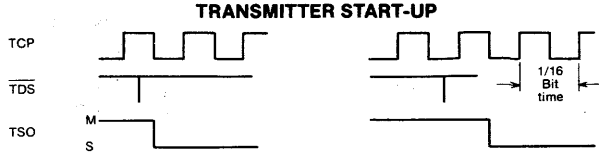
DESCRIPTION OF PIN FUNCTION

PIN NO.	SYMBOL	NAME	FUNCTION
36	NSB	Number of Stop Bits	This input selects the number of stop bits. A low-level input selects 1 stop bit; a high-level input selects 2 stop bits. Selection of 2 stop bits when programming a 5 data bit word generates 1.5 stop bits from the COM 8017 or COM 8017/H.
37-38	NDB2, NDB1	Number of Data Bits/Character	These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table: NDB2 NDB1 data bits/character L L 5 L H 6 H L 7 H H 8
39	POE	Odd/Even Parity Select	The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the receiver and transmitter, as per the following truth table: NPB POE MODE L L odd parity L H even parity H X no parity X = don't care
40	TCP	Transmitter Clock	This input is a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

TRANSMITTER TIMING—8 BIT, PARITY, 2 STOP BITS

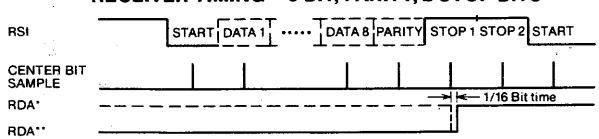


TRANSMITTER START-UP



Upon data transmission initiation, or when not transmitting at 100% line utilization, the start bit will be placed on the TSO line at the high to low transition of the TCP clock following the trailing edge of TDS.

RECEIVER TIMING—8 BIT, PARITY, 2 STOP BITS



*The RDA line was previously not reset (ROR = high-level).
**The RDA line was previously reset (ROR = low-level).

START BIT DETECT/VERIFY

If the RSI line remains spacing for a 1/2 bit time, a genuine start bit is verified. Should the line return to a marking condition prior to a 1/2 bit time, the start bit verification process begins again.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin. with respect to ground ..... −0.3V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that at clamp circuit be used.

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}	0		0.8	V	
High-level, V_{IH}	2.0		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	$I_{OL} = 1.6mA$
High-level, V_{OH}	2.4			V	$I_{OH} = -100\mu A$
INPUT CURRENT					
Low-level, I_{IL}			300	μA	$V_{IN} = G_{ND}$
OUTPUT CURRENT					
Leakage, I_{LO}			±10	μA	$\overline{SWE} = \overline{RDE} = V_{IH}$, $0 \leq V_{OUT} \leq +5V$
Short circuit, Ios**			30	mA	$V_{OUT} = 0V$
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pf	$\overline{SWE} = \overline{RDE} = V_{IH}$
POWER SUPPLY CURRENT					
I_{CC}			25	mA	All outputs = V_{OH}, All inputs = V_{CC}
A.C. CHARACTERISTICS					$T_A = +25°C$
CLOCK FREQUENCY					
COM8502, COM 8017	DC		640	KHz	RCP, TCP
PULSE WIDTH					
Clock	0.7			μs	RCP, TCP
Master reset	500			ns	MR
Control strobe	200			ns	$\overline{CS}$
Transmitter data strobe	200			ns	$\overline{TDS}$
Receiver data available reset	200			ns	$\overline{RDAR}$
INPUT SET-UP TIME					
Data bits	≥0			ns	TD1-TD8
Control bits	≥0			ns	NPB, NSB, NDB2, NDB1, POE
INPUT HOLD TIME					
Data bits	≥0			ns	TD1-TD8
Control bits	≥0			ns	NPB, NSB, NDB2, NDB1, POE
STROBE TO OUTPUT DELAY					Load = 20pf +1 TTL input
Receive data enable			350	ns	$\overline{RDE}$: T_{PD1}, T_{PD0}
Status word enable			350	ns	$\overline{SWE}$: T_{PD1}, T_{PD0}
OUTPUT DISABLE DELAY			350	ns	$\overline{RDE}$, $\overline{SWE}$

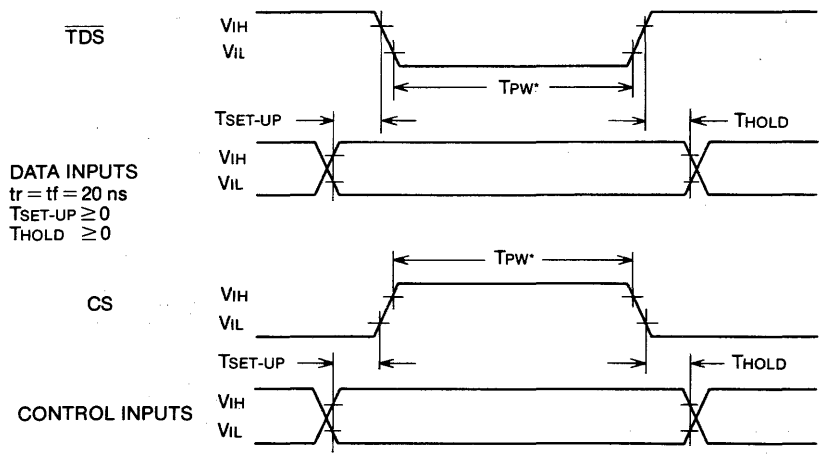
**Not more than one output should be shorted at a time.

NOTES: 1. If the transmitter is inactive (TEOC and TBMT are at a high-level) the start bit will appear on the TSO line within one clock period (TCP) after the trailing edge of $\overline{TDS}$.

2. The start bit (mark to space transition) will always be detected within one clock period of RCP, guaranteeing a maximum start bit slippage of 1/16th of a bit time.

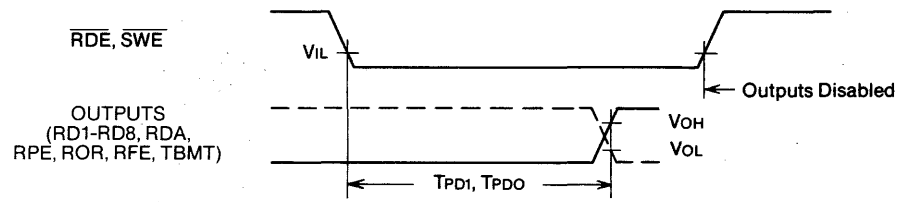
3. The tri-state output has 3 states: 1) low impedance to Vcc 2) low impedance to GND 3) high impedance OFF ≅ 10M ohms The "OFF" state is controlled by the $\overline{SWE}$ and $\overline{RDE}$ inputs.

DATA/CONTROL TIMING DIAGRAM

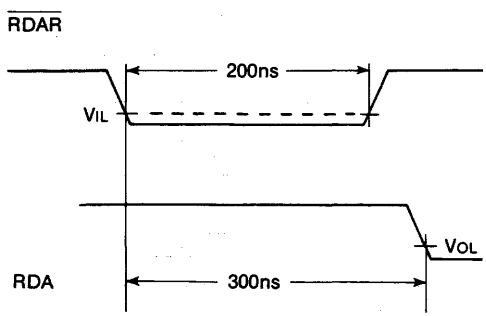


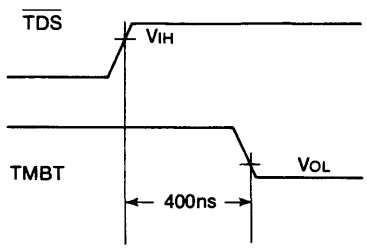
*Input information (Data/Control) need only be valid during the last TPW, min time of the input strobes (TDS, CS).

OUTPUT TIMING DIAGRAM

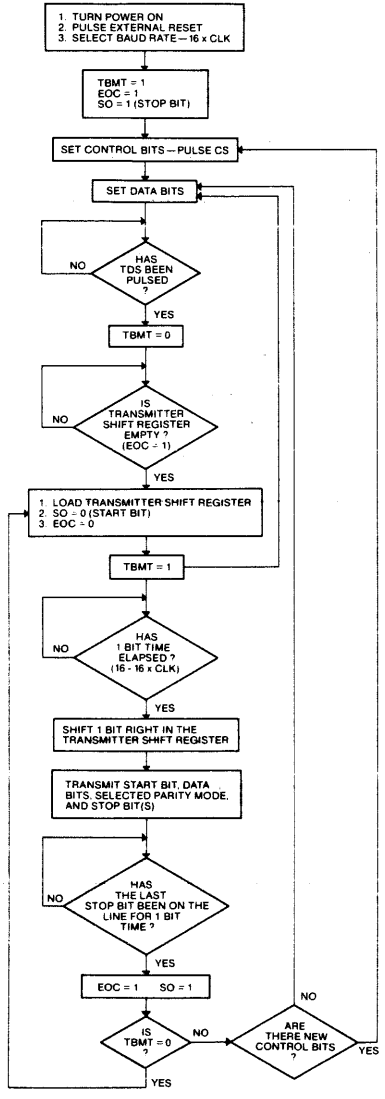


NOTE: Waveform drawings not to scale for clarity.

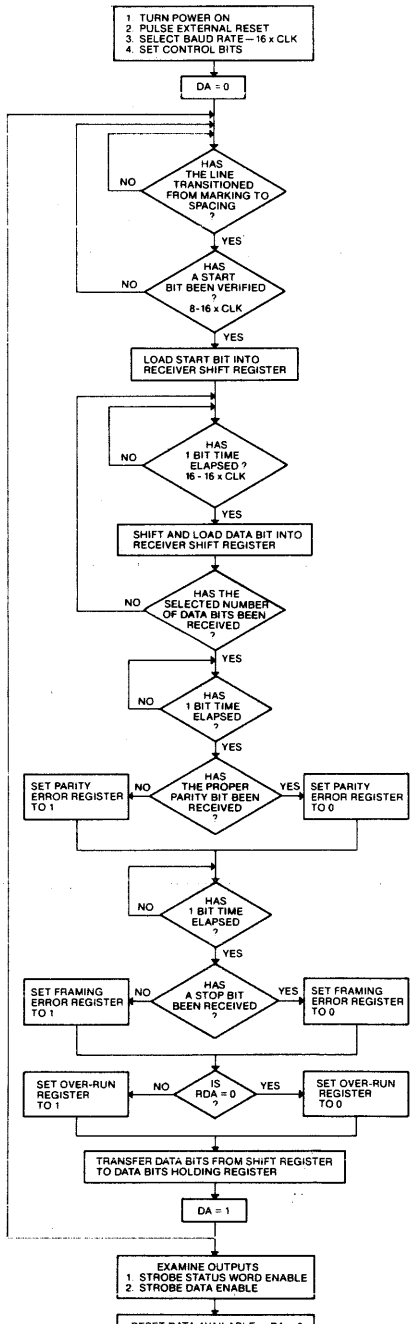




FLOW CHART—TRANSMITTER



FLOW CHART—RECEIVER



STANDARD MICROSYSTEMS CORPORATION

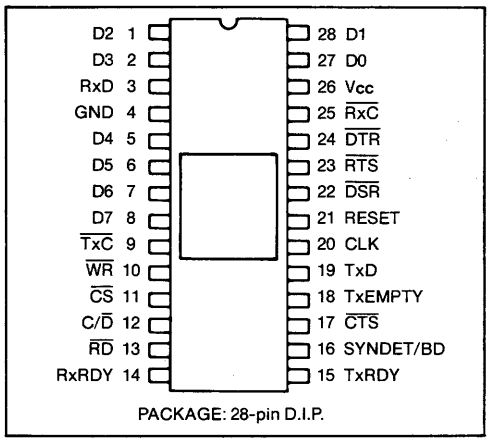
COM 8251A
μPC FAMILY

Universal Synchronous/Asynchronous Receiver/Transmitter USART

FEATURES

- ☐ Asynchronous or Synchronous Operation
  - —Asynchronous:
    - 5-8 Bit Characters
    - Clock Rate—1, 16 or 64 X Baud Rate
    - Break Character Generation
    - 1, 1½ or 2 Stop Bits
    - False Start Bit Detection
    - Automatic Break Detect and Handling
  - —Synchronous:
    - 5-8 Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
    - Single or Double Sync Characters
    - Programmable Sync Character(s)
- ☐ Baud Rate—Synchronous—DC to 64K Baud
  —Asynchronous—DC to 19.2K Baud
- ☐ Baud Rates available from SMC's COM 8116, COM 8126, COM 8136, COM 8146, and COM 8046
- ☐ Full Duplex, Double Buffered Transmitter and Receiver
- ☐ Odd parity, even parity or no parity bit
- ☐ Parity, Overrun and Framing Error Flags
- ☐ Modem Interface Controlled by Processor
- ☐ All Inputs and Outputs are TTL Compatible

PIN CONFIGURATION



PACKAGE: 28-pin D.I.P.

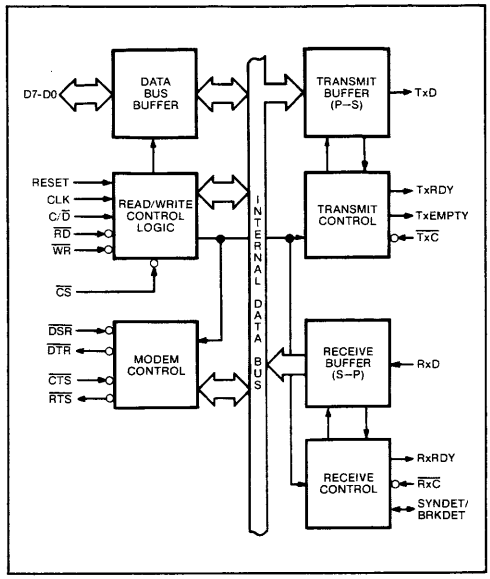
- ☐ Compatable with Intel 8251A, NEC μPD8251A
- ☐ Single +5 Volt Supply
- ☐ Separate Receive and Transmit TTL Clocks
- ☐ Enhanced version of 8251
- ☐ 28 Pin Plastic or Ceramic DIP Package
- ☐ COPLAMOS® N-Channel MOS Technology

GENERAL DESCRIPTION

The COM 8251A is an MOS/LSI device fabricated using SMC's patented COPLAMOS® technology that meets the majority of asynchronous and synchronous data communication requirements by interfacing parallel digital systems to asynchronous and synchronous data communication channels while requiring a minimum of processor overhead. The COM 8251A is an enhanced version of the 8251.

The COM 8251A is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for microcomputer system data communications. The USART is used as a peripheral and is programmed by the processor to communicate in commonly used asychronous and synchronous serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status, including data format errors and control signals such as TxE and SYNDET, is available to the processor at any time.

BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
1, 2, 27, 28, 5-8	D2, D3, D0, D1, D4-D7	DATA BUS	I/O	An 8-bit, 3-state bi-directional DATA BUS used to interface the COM 8251A to the processor data bus. Data is transmitted or received by the bus in response to input/output or Read/Write instructions from the processor. The DATA BUS also transfers Control words, Command words, and Status.
3	RxD	RECEIVER DATA	I	This input receives serial data into the USART.
4	GND	GROUND	GND	Ground
9	$\overline{TxC}$	$\overline{TRANSMITTER\ CLOCK}$	I	The $\overline{TRANSMITTER\ CLOCK}$ controls the serial character transmission rate. In the Asynchronous mode, the $\overline{TxC}$ frequency is a multiple of the actual Baud Rate. Two bits of the Mode Instruction select the multiple to be 1X, 16X, or 64X the Baud Rate. In the Synchronous mode, the $\overline{TxC}$ frequency is automatically selected to equal the actual Baud Rate. Note that for both Synchronous and Asynchronous modes, serial data is shifted out of the USART by the falling edge of $\overline{TxC}$.
10	$\overline{WR}$	$\overline{WRITE\ DATA}$	I	A "zero" on this input instructs the COM 8251A to accept the data or control word which the processor is writing out to the USART via the DATA BUS.
11	$\overline{CS}$	$\overline{CHIP\ SELECT}$	I	A "zero" on this input enables the USART for reading and writing to the processor. When $\overline{CS}$ is high, the DATA BUS is in the float state and $\overline{RD}$ and $\overline{WR}$ will have no effect on the chip.
12	C/$\overline{D}$	CONTROL/$\overline{DATA}$	I	The Control/$\overline{Data}$ input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the USART to accept or provide either a data character, control word or status information via the DATA BUS. 0 = Data; 1 = Control/Status
13	$\overline{RD}$	$\overline{READ\ DATA}$	I	A "zero" on this input instructs the COM 8251A to place the data or status information onto the DATA BUS for the processor to read.
14	RxRDY	RECEIVER READY	O	The RECEIVER READY output indicates that the Receiver Buffer is ready with an "assembled" character for input to the processor. For polled operation, the processor can check RxRDY using a Status Read or RxRDY can be connected to the processor interrupt structure. Note that reading the character to the processor automatically resets RxRDY.
15	TxRDY	TRANSMITTER READY	O	TRANSMITTER READY signals the processor that the transmitter is ready to accept a data character. TxRDY can be used as an interrupt or may be tested through the Status information polled operaton. TxRDY is automatically reset by the leading edge of $\overline{WR}$ when a data character is loaded from the processor.
16	SYNDET/ BRKDET	SYNC DETECT/ BREAK DETECT	I/O	The SYNDET feature is only used in the Synchronous mode. The USART may be programmed through the Mode Instruction to operate in either the internal or external Sync mode and SYNDET then functions as an output or input respectively. In the internal SYNC mode, the SYNDET output will go to a "one" when the COM 8251A has located the SYNC character in the Receive mode. If double SYNC character (bi-sync) operation has been programmed, SYNDET will go to "one" in the middle of the last bit of the second contiguously detected SYNC character. SYNDET is automatically reset to "zero" upon a Status Read or RESET. In the external SYNC mode, a "zero" to "one" transition on the SYNDET input is sampled during the negative half cycle of $\overline{RxC}$ and will cause the COM 8251A to start assembling data character on the next rising edge of $\overline{RxC}$. The length of the SYNDET input should be at least one $\overline{RxC}$ period, but may be removed once the COM 8251A is in SYNC. When external SYNC DETECT is programmed, the internal SYNC DETECT is disabled.

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
16 (cont.)				The SYNDET/BRKDET pin is used in both Synchronous and Asynchronous modes. When in SYNC mode the features for the SYNDET pin described above apply. When in Asynchronous mode, the BREAK DETECT output will go high when an all zero word of the programmed length is received. This word consists of: start bit, data bit, parity bit and one stop bit. Reset only occurs when Rx Data returns to a logic one state or upon chip RESET. The state of BREAK DETECT can also be read as a status bit.
17	$\overline{CTS}$	$\overline{CLEAR\ TO\ SEND}$	I	A "zero" on the $\overline{CLEAR\ TO\ SEND}$ input enables the USART to transmit serial data if the TxEN bit in the Command Instruction register is enabled (one). If either a TxEN off or $\overline{CTS}$ off condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART written prior to the Tx Disable command before shutting down.
18	TxE	TRANSMITTER EMPTY	O	The TRANSMITTER EMPTY output signals the processor that the USART has no further characters to transmit. TxE is automatically reset upon receiving a data character from the processor. In half-duplex, TxE can be used to signal end of a transmission and request the processor to "turn the line around". The TxEN bit in the command instruction does not effect TxE. In the Synchronous mode, a "one" on this output indicates that a SYNC character or characters are about to be automatically transmitted as "fillers" because the next data character has not been loaded; an underflow condition. If the USART is operating in the two SYNC character mode, both SYNC characters will be transmitted before the message can resume. TxE does not go low when the SYNC characters are being shifted out. TxE goes low upon the processor writing a character to the USART.
19	TxD	TRANSMITTER DATA	O	This output is the transmitted serial data from the USART. When a transmission is concluded the TxD line will always return to the marking state unless SBRK is programmed.
20	CLK	CLOCK PULSE	I	The CLK input provides for internal device timing. External inputs and outputs are not referenced to CLK, but the CLK frequency must be greater than 30 times the RECEIVER or TRANSMITTER CLOCKS in the 1X mode and greater than 4.5 times for the 16X and 64X modes.
21	RESET	RESET	I	A "one" on this input forces the USART into the "idle" mode where it will remain until reinitialized with a new set of control words. RESET causes: RxRDY = TxRDY = TxEmpty = SYNDET/BRKDET = 0; TxD = $\overline{DTR}$ = $\overline{RST}$ = 1. Minimum RESET pulse width is 6 t_{CY}, CLK must be running during RESET.
22	$\overline{DSR}$	$\overline{DATA\ SET\ READY}$	I	The $\overline{DATA\ SET\ READY}$ input can be tested by the processor via Status information. The $\overline{DSR}$ input is normally used to test Modem Data Set Ready condition.
23	$\overline{RTS}$	$\overline{REQUEST\ TO\ SEND}$	O	The $\overline{REQUEST\ TO\ SEND}$ output is controlled via the Command word. The $\overline{RTS}$ output is normally used to drive the Modem Request to Send line.
24	$\overline{DTR}$	$\overline{DATA\ TERMINAL\ READY}$	O	The $\overline{DATA\ TERMINAL\ READY}$ output is controlled via the Command word. The $\overline{DTR}$ output is normally used to drive Modem Data Terminal Ready or Rate Select lines.
25	$\overline{RxC}$	$\overline{RECEIVER\ CLOCK}$	I	The $\overline{RECEIVER\ CLOCK}$ is the rate at which the incoming character is received. In the Asynchronous mode, the $\overline{RxC}$ frequency may be 1, 16 or 64 times the actual Baud Rate but in the Synchronous mode the $\overline{RxC}$ frequency must equal the Baud Rate. Two bits in the mode instruction select Asynchronous at 1X, 16X or 64X or Synchronous operation at 1X the Baud Rate. Data is sampled into the USART on the rising edge of $\overline{RxC}$.
26	V_{CC}	V_{CC} SUPPLY VOLTAGE	PS	+5 volt supply

DESCRIPTION OF OPERATION—ASYNCHRONOUS

Transmission—

When a data character is written into the USART, it automatically adds a START bit (low level or "space") and the number of STOP bits (high level or "mark") specified by the Mode Instruction. If Parity has been enabled, an odd or even Parity bit is inserted just before the STOP bit(s), as specified by the Mode Instruction. Then, depending on $\overline{CTS}$ and TxEN, the character may be transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of $\overline{TxC}$ at a transmission rate of $\overline{TxC}$, $\overline{TxC}/16$ or $\overline{TxC}/64$, as defined by the Mode Instruction.

If no data characters have been loaded into the USART, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the START bit of the next character provided by the processor. TxD may be forced to send a BREAK (continuously low) by setting the correct bit in the Command Instruction.

Receive—

The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge (high to low transition) at RxD signals the possible beginning of a START bit and a new character. The receiver is thus prevented from starting in a "BREAK" state. The START bit is verified by testing for a "low" at its nominal center as specified by the BAUD RATE. If a "low" is detected, it is considered valid, and the bit assembling counter starts counting. The bit counter locates the approximate center of the data, parity (if specified), and STOP bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of $\overline{RxC}$. If a high is not detected for the STOP bit, which normally signals the end of an input character, a framing error (FE) will be set. After the STOP bit time, the input character is loaded into the paralled Data Bus Buffer of the USART and the RxRDY signal is raised to indicate to the processor that a character is ready to be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and overrun flag (OE) is set. All the error flags can be reset by setting a bit in the Command Instruction. Error flag conditions will not stop subsequent USART operation.

DESCRIPTION OF OPERATION—SYNCHRONOUS

Transmission—

As in Asynchronous transmission, the TxD output remains "high" (marking) until the USART receives the first character (usually a SYNC character) from the processor. After a Command Instruction has set TxEN and after Clear to Send ($\overline{CTS}$) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of $\overline{TxC}$ at the same rate as $\overline{TxC}$.

Once transmission has started, Synchronous Data Protocols require that the serial data stream at TxD continue at the $\overline{TxC}$ rate or SYNC will be lost. If a data character is not provided by the processor before the USART Transmit Buffer becomes empty, the SYNC character(s) loaded directly following the Mode Instruction will be automatically inserted in the TxD data stream. The SYNC character(s) are inserted to fill the line and maintain synchronization until the new data characters are available for transmission. If the USART becomes empty, and must send the SYNC character(s), the TxEMPTY output is raised to signal the processor that the Transmitter Buffer is empty and SYNC characters are being transmitted. TxEMPTY is automatically reset by the next character from the processor.

Receive—

In Synchronous receive, character synchronization can be either external or internal. If the internal SYNC mode has been selected, the ENTER HUNT (EH) bit has been set by a Command Instruction, the receiver goes into the HUNT mode.

Incoming data on the RxD input is sampled on the rising edge of $\overline{RxC}$, and the contents of the Receive Buffer are compared with the first SYNC character after each bit has been loaded until a match is found. If two SYNC characters have been programmed, the next received character is also compared. When the (two contiguous) SYNC character(s) programmed have been detected, the USART leaves the HUNT mode and is in character synchronization. At this time, the SYNDET (output) is set high. SYNDET is automatically reset by a STATUS READ.

If external SYNC has been specified in the Mode Instruction, a "one" applied to the SYNDET (input) for at least one $\overline{RxC}$ cycle will synchronize the USART.

Parity and Overrun Errors are treated the same in the Synchronous as in the Asynchronous Mode. If not in HUNT, parity will continue to be checked even if the receiver is not enabled. Framing errors do not appiy in the Synchronous format.

The processor may command the receiver to enter the HUNT mode with a Command Instruction which sets Enter HUNT (EH) if synchronization is lost. Under this condition the Rx register will be cleared to all "ones".

OPERATION AND PROGRAMMING

The microprocessor program controlling the COM 8251A performs these tasks:

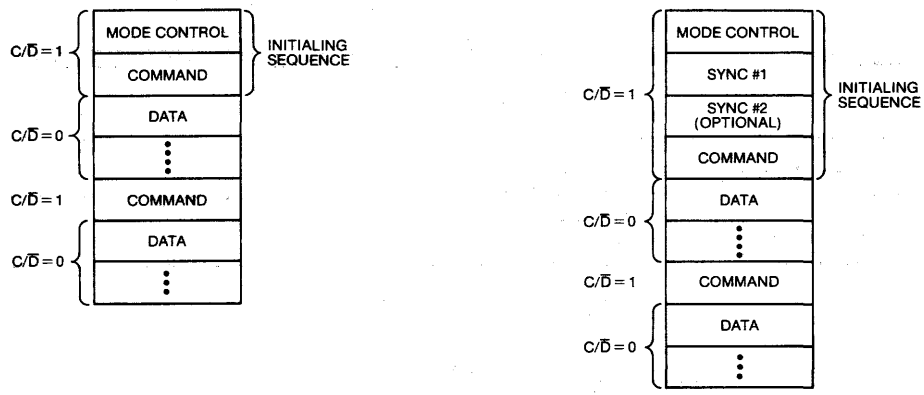
- Outputs control codes
- Inputs status
- Outputs data to be transmitted
- Inputs data which has been received

Control codes determine the mode in which the COM 8251A will operate and are used to set or reset control signals output by the COM 8251A.

The Status register contents will be read by the program monitoring this device's operation in order to determine error conditions, when and how to read data, write data or output control codes. Program logic may be based on reading status bit levels, or control signals may be used to request interrupts.

INITIALIZING THE COM 8251A

Figure 1. Control Word Sequences for Initialization



ASYNCHRONOUS OPERATION **SYNCHRONOUS OPERATION**

The COM 8251A may be initialized following a system RESET or prior to starting a new seral I/O sequence. The USART must be RESET (external or internal) following power up and subsequently may be reset at any time following completion of one activity and preceding a new set of operations. Following a reset, the COM 8251A enters an idle state in which it can neither transmit nor receive data.

The COM 8251A is initialized with two, three or four control words from the processor. Figure 1 shows the sequence of control words needed to initialize the COM 8251A, for synchronous or for asynchronous operation. Note that in asynchronous operation a mode control is output to the device followed by a command. For synchronous operation, the mode control is followed by one or two SYNC characters, and then a command.

Only a single address is set aside for mode control bytes, command bytes and SYNC character bytes. For this to be possible, logic internal to the chip directs control information to its proper destination based on the sequence in which it is received. Following a RESET (external or internal), the first control code output is interpreted as a mode control. If the mode control specifies synchronous operation, then the next one or two bytes (as determined by the mode byte) output as control codes will be interpreted as SYNC characters. For either asynchronous or synchronous operation, the next byte output as a control code is interpreted as a command. All subsequent bytes output as control codes are interpreted as commands. There are two ways in which control logic may return to anticipating a mode control input; following a RESET input or following an internal reset command. A reset operation (internal via IR or external via RESET) will cause the USART to interpret the next "control write", which should immediately follow the reset, as a Mode Instruction.

After receiving the control words the USART is ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. Concurrently, the USART is ready to receive serial data.

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	USART → Data Bus
0	1	0	0	Data Bus → USART
1	0	1	0	Status → Data Bus
1	1	0	0	Data Bus → Control
X	X	X	1	Data Bus → 3-State
X	1	1	0	

MODE CONTROL CODES

The COM 8251A interprets mode control codes as illustrated in Figures 2 and 3.

Control code bits 0 and 1 determine whether synchronous or asynchronous operation is specified. A non-zero value in bits 0 and 1 specifies asynchronous operation and defines the relationship between data transfer baud rate and receiver or transmitter clock rate. Asynchronous serial data may be received or transmitted on every clock pulse, on every 16th clock pulse, or on every 64th clock pulse, as programmed. A zero in both bits 0 and 1 defines the mode of operation as synchronous.

For synchronous and asynchronous modes, control bits 2 and 3 determine the number of data bits which will be present in each data character. In the case of a programmed character length of less than 8 bits, the least significant DATA BUS unused bits are "don't care" when writing data to the USART and will be "zeros" when reading data. Rx data will be right justified onto D0 and the LSB for Tx data is D0.

For synchronous and asynchronous modes, bits 4 and 5 determine whether there will be a parity bit in each character, and if so, whether odd or even parity will be adopted. Thus in synchronous mode a character will consist of five, six, seven or eight data bits, plus an optional parity bit. In asynchronous mode, the data unit will consist of five, six, seven or eight data bits, an optional parity bit, a preceeding start bit, plus 1, 1½ or 2 trailing stop bits. Interpretation of subsequent bits differs for synchronous or asynchronous modes.

Control code bits 6 and 7 in asynchronous mode determine how many stop bits will trail each data unit. 1½ stop bits can only be specified with a 16X or 64X baud rate factor. In these two cases, the half stop bit will be equivanlent to 8 or 32 clock pulses, respectively.

In synchronous mode, control bits 6 and 7 determine how character synchronization will be achieved. When SYNDET is an output, internal synchronization is specified; one or two SYNC characters, as specified by control bit 7, must be detected at the head of a data stream in order to establish synchronization.

COMMAND WORDS

Command words are used to initiate specific functions within the COM 8251A such as, "reset all error flags" or "start searching for sync". Consequently, Command Words may be issued by the processor to the COM 8251A at any time during the execution of a program in which specific functions are to be initialized within the communication circuit.

Figure 4 shows the format for the Command Word.

Figure 4. COM 8251A Control Command

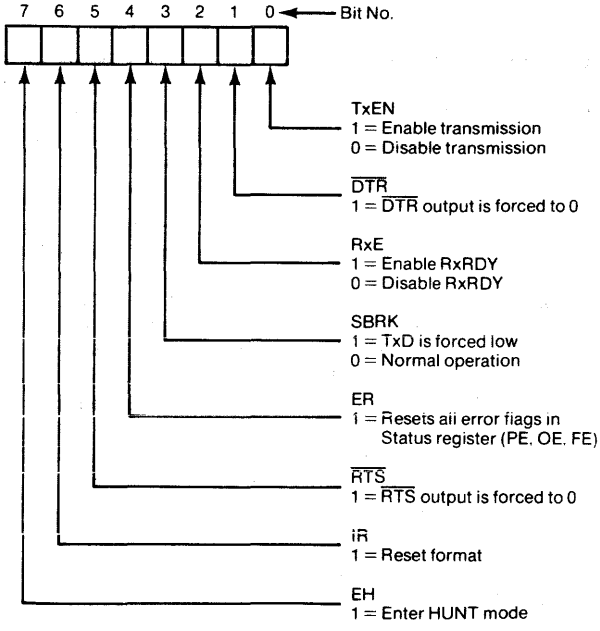


Figure 2. Synchronous Mode Control Code.

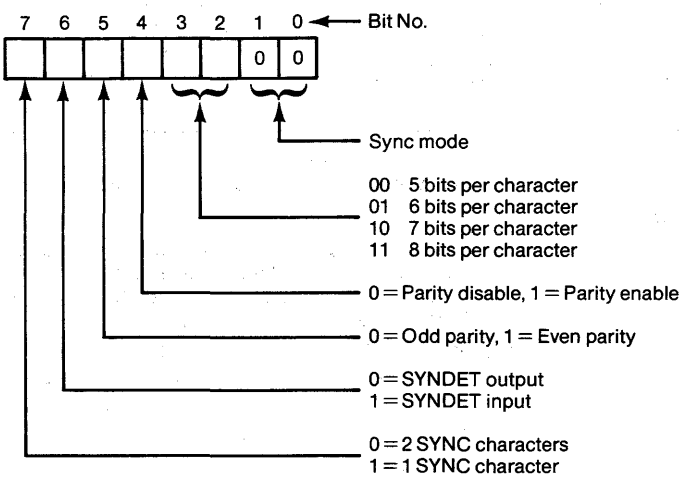
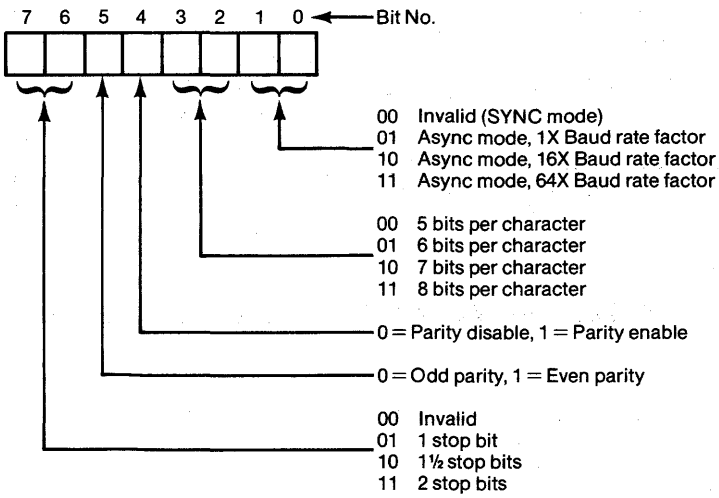


Figure 3. Asynchronous Mode Control Code.



Bit 0 of the Command Word is the Transmit Enable bit (TxEN). Data transmission for the COM 8251A cannot take place unless TxEN is set (assuming $\overline{CTS} = 0$) in the command register. The TX Disable command is prevented from halting transmission by the Tx Enable logic until all data previously written has been transmitted. Figure 5 defines the way in which TxEN, TxE and TxRDY combines to control transmitter operations.

Bit 1 is the Data Terminal Ready ($\overline{DTR}$) bit. When the $\overline{DTR}$ command bit is set, the $\overline{DTR}$ output connection is active (low). $\overline{DTR}$ is used to advise a modem that the data terminal is prepared to accept or transmit data.

Bit 2 is the Receiver Enable Command bit (RxE). RxE is used to enable the RxRDY output signal. RxE, when zero, prevents the RxRDY signal from being generated to notify the processor that a complete character is framed in the Receive Character Buffer. It does not inhibit the assembly of data characters at the input, however. Consequently, if communication circuits are active, characters will be assembled by the receiver and transferred to the Receiver Buffer. If RxE is disabled, the overrun error (OE) will probably be set; to insure proper operation, the overrun error is usually reset with the same command that enables RxE.

Figure 5.
Operation of the Transmitter Section as a Function of TxE, TxRDY and TxEN

TxEN	TxE	TxRDY	
1	1	1	Transmit Output Register and Transmit Character Buffer empty. TxD continues to mark if COM 8251A is in the asynchronous mode. TxD will send SYNC pattern if COM 8251A is in the Synchronous Mode. Data can be entered into Buffer.
1	0	1	Transmit Output Register is shifting a character. Transmit Character Buffer is available to receive a new byte from the processor.
1	1	0	Transmit Register has finished sending. A new character is waiting for transmission. This is a transient condition.
1	0	0	Transmit Register is currently sending and an additional character is stored in the Transmit Character Buffer for transmission.
0	0/1	0/1	Transmitter is disabled.

Bit 3 is the Send Break Command bit (SBRK). When SBRK is set, the transmitter output (TxD) is interrupted and a continuous binary "0" level, (spacing) is applied to the TxD output signal. The break will continue until a subsequent Command Word is sent to the COM 8251A to remove SBRK.

Bit 4 is the Error Reset bit (ER). When a Command Word is transferred with the ER bit set, all three error flags (PE, OE, FE) in the Status Register are reset. Error Reset occurs when the Command Word is loaded into the COM 8251A. No latch is provided in the Command Register to save the ER command bit.

Bit 5, the Request To Send Command bit ($\overline{RTS}$), sets a latch to reflect the $\overline{RTS}$ signal level. The output of this latch is created independently of other signals in the COM 8251A. As a result, data transfers may be made by the processor to the Transmit Register, and data may be actively transmitted to the communication line through TxD regardless of the status of $\overline{RTS}$.

Bit 6, the Internal Reset (IR), causes the COM 8251A to return to the Idle mode. All functions within the COM 8251A cease and no new operation can be resumed until the circuit is reinitialized. If the operating mode is to be altered during the execution of a processor program, the COM 8251A must first be reset. Either the RESET input can be activated, or the Internal Reset Command can be sent to the COM 8251A. Internal Reset is a momentary function performed only when the command is issued.

Bit 7 is the Enter Hunt command bit (EH). The Enter Hunt mode command is only effective for the COM 8251A when it is operating in the Synchronous mode. EH causes the receiver to stop assembling characters at the RxD input, clear the Rx register to all "ones", and start searching for the prescribed sync pattern. Once the "Enter Hunt" mode has been initiated, the search for the sync pattern will continue indefinitely until EH is reset when a subsequent Command Word is sent, when the IR command is sent to the COM 8251A, or when SYNC characters are recognized. Parity is not checked in the EH mode.

STATUS REGISTER

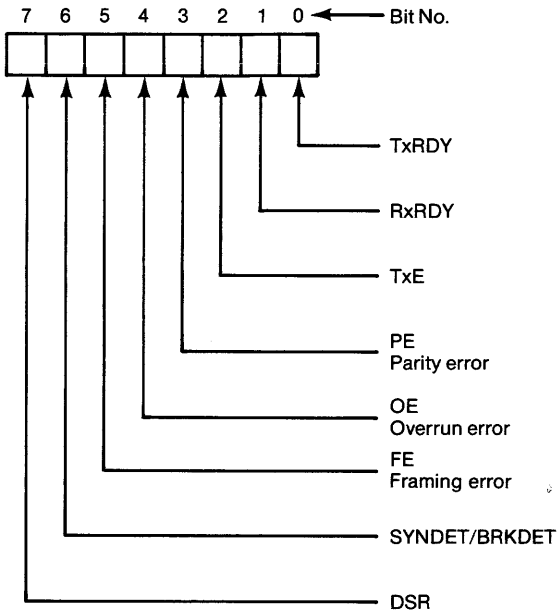
The Status Register maintains information about the current operational status of the COM 8251A. Status can be read at any time, however, the status update will be inhibited during status read. Figure 6 shows the format of the Status Register.

TxRDY signals the processor that the Transmit Character Buffer is empty and that the COM 8251A can accept a new character for transmission. The TxRDY status bit is not totally equivalent to the TxRDY output pin, the relationship is as follows:

TxRDY (status bit) = Tx Character Buffer Empty
TxRDY (pin 15) = Tx Character Buffer Empty • $\overline{CTS}$ • TxEN

RxRDY signals the processor that a completed character is holding in the Receive Character Buffer Register for transfer to the processor.

Figure 6. The COM 8251A Status Register



TxE signals the processor that the Transmit Register is empty.

PE is the Parity Error signal indicating to the CPU that the character stored in the Receive Character Buffer was received with an incorrect number of binary "1" bits. PE does not inhibit USART operation. PE is reset by the ER bit.

OE is the receiver Overrun Error. OE is set whenever a byte stored in the Receiver Character Register is overwritten with a new byte before being transferred to the processor. OE does not inhibit USART operation. OE is reset by the ER bit.

FE (Async only) is the character framing error which indicates that the asynchronous mode byte stored in the Receiver Character Buffer was received with incorrect bit format ("0" stop bit), as specified by the current mode. FE does not inhibit USART operaton. FE is reset by the ER bit.

SYNDET is the synchronous mode status bit associated with internal or external sync detection.

DSR is the status bit set by the external $\overline{\text{Data Set Ready}}$ signal to indicate that the communication Data Set is operational.

All status bits are set by the functions described for them. SYNDET is reset whenever the processor reads the Status Register. OE, FE, PE are reset by the error reset command or the internal reset command or the RESET input. OE, FE, or PE being set does not inhibit USART operation.

Many of the bits in the status register are copies of external pins. This dual status arrangement allows the USART to be used in both Polled and Interrupt driven environments. Status update can have a maximum delay of 16 t_{CY} periods.

Note:

1. While operating the receiver it is important to realize that the RxE bit of the Command Instruction only inhibits the assertion of RxRDY; it does not inhibit the actual reception of characters. As the receiver is constantly running, it is possible for it to contain extraneous data when it is enabled. To avoid problems this data should be read from the USART and discarded. This read should be done immediately following the setting of the RxE bit in the asynchronous mode, and following the setting of EH in the synchronous mode. It is not necessary to wait for RxRDY before executing the dummy read.
2. ER should be performed whenever RxE of EH are programmed. ER resets all error flags, even if RxE = 0.
3. The USART may provide faulty RxRDY for the first read after power-on or for the first read after the receiver is re-enabled by a command instruction (RxE). A dummy read is recommended to clear faulty RxRDY. This is not the case for the first read after hardware or software reset after the device opration has been established.
4. Internal Sync Detect is disabled when External Sync Detect is programmed. An External Sync Detect Status is provided through an internal flip-flop which clears itself, assuming the External Sync Detect assertion has removed, upon a status read. As long as External Sync Detect is asserted, External Sync Detect Status will remain high.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that as clamp circuit be used.

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
D.C. Characteristics					
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.2$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400\ \mu A$
I_{OFL}	Output Float Leakage		±10	μA	$V_{OUT} = V_{CC}$ TO 0.45V
I_{IL}	Input Leakage		±10	μA	$V_{IN} = V_{CC}$ TO 0.45V
I_{CC}	Power Supply Current		100	mA	All Outputs = High
Capacitance					$T_A = 25°C$, $V_{CC} = GND$
C_{IN}	Input Capacitance		10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to GND
A.C. Characteristics					
Bus Parameters (Note 1)					
Read Cycle:					
t_{AR}	Address Stable Before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	0		ns	Note 2
t_{RA}	Address Hold Time for $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	0		ns	Note 2
t_{RR}	$\overline{READ}$ Pulse Width	250		ns	
t_{RD}	Data Delay from $\overline{READ}$		200	ns	Note 3, $C_L = 150$ pF
t_{DF}	$\overline{READ}$ to Data Floating	10	100	ns	
Write Cycle:					
t_{AW}	Address Stable Before $\overline{WRITE}$	0		ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$	0		ns	
t_{WW}	$\overline{WRITE}$ Pulse Width	250		ns	
t_{DW}	Data Set Up Time for $\overline{WRITE}$	150		ns	
t_{WD}	Data Hold Time for $\overline{WRITE}$	0		ns	
t_{RV}	Recovery Time Between WRITES	6		t_{CY}	Note 4
Other Timings:					
t_{CY}	Clock Period	.320	1.35	μs	Notes 5, 6
t_{ϕ}	Clock High Pulse Width	120	$t_{CY}-90$	ns	
$t_{\overline{\phi}}$	Clock Low Pulse Width	90		ns	

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_R, t_F	Clock Rise and Fall Time	5	20	ns	
t_{DTx}	TxD Delay from Falling Edge of $\overline{TxC}$		1	μs	
t_{SRx}	Rx Data Set-Up Time to Sampling Pulse	2		μs	
t_{HRx}	Rx Data Hold Time to Sampling Pulse	2		μs	
f_{Tx}	Transmitter Input Clock Frequency				
	1X Baud Rate	DC	64	kHz	
	16X Baud Rate	DC	310	kHz	
	64X Baud Rate	DC	615	kHz	
t_{TPW}	Transmitter Input Clock Width				
	1X Baud Rate	12		t_{CY}	
	16X and 64X Baud Rate	1		t_{CY}	
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1X Baud Rate	15		t_{CY}	
	16X and 64X Baud Rate	3		t_{CY}	
f_{Rx}	Receiver Input Clock Frequency				
	1X Baud Rate	DC	64	kHz	
	16X Baud Rate	DC	310	kHz	
	64X Baud Rate	DC	615	kHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1X Baud Rate	12		t_{CY}	
	16X and 64X Baud Rate	1		t_{CY}	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1X Baud Rate	15		t_{CY}	
	16X and 64X Baud Rate	3		t_{CY}	
t_{TxRDY}	TxRDY Pin Delay from Center of last Bit		8	t_{CY}	Note 7
$t_{TxRDY\ CLEAR}$	TxRDY ↓ from Leading Edge of $\overline{WR}$		150	ns	Note 7
t_{RxRDY}	RxRDY Pin Delay from Center of last Bit		24	t_{CY}	Note 7
$t_{RxRDY\ CLEAR}$	RxRDY ↓ from Leading Edge of $\overline{RD}$		150	ns	Note 7
t_{IS}	Internal SYNDET Delay from Rising Edge of $\overline{RxC}$		24	t_{CY}	Note 7
t_{ES}	External SYNDET Set-Up Time Before Falling Edge of $\overline{RxC}$		16	t_{CY}	Note 7
$t_{TxEMPTY}$	TxEMPTY Delay from Center of Data Bit		20	t_{CY}	Note 7
t_{WC}	Control Delay from Rising Edge of WRITE (TxEn, $\overline{DTR}$, $\overline{RTS}$)		8	t_{CY}	Note 7
t_{CR}	Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)		20	t_{CY}	Note 7

NOTES: 1. AC timings measured $V_{OH} = 2.0$, $V_{OL} = 0.8$, and with load circuit of Figure 1.
2. Chip Select ($\overline{CS}$) and Command/$\overline{Data}$ ($C/\overline{D}$) are considered as Addresses.
3. Assumes that Address is valid before $R_{D}\downarrow$.
4. This recovery time is for RESET and Mode Initialization. Write Data is allowed only when TxRDY = 1. Recovery Time between Writes for Asynchronous Mode is 8 t_{CY} and for Synchronous Mode is 16 t_{CY}.
5. The TxC and RxC frequencies have the following limitations with respect to CLK.
   For 1X Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(30\ t_{CY})$
   For 16X and 64X Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(4.5\ t_{CY})$
6. Reset Pulse Width = 6 t_{CY} minimum; System Clock must be running during RESET.
7. Status update can have a maximum delay of 28 clock periods from the event affecting the status.

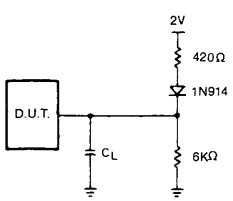
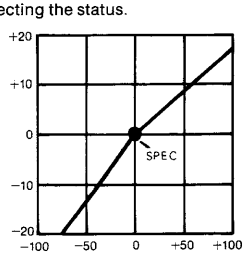


Figure 1.

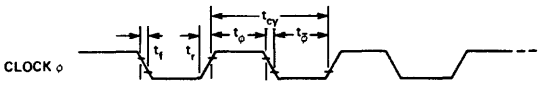
TEST LOAD CIRCUIT

Typical Δ Output Delay Versus Δ Capacitance (pF)

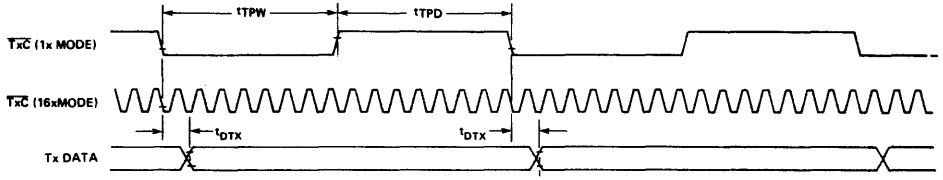


WAVEFORMS

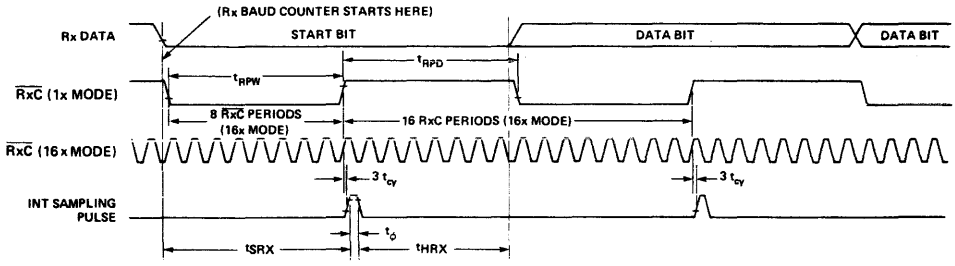
System Clock Input



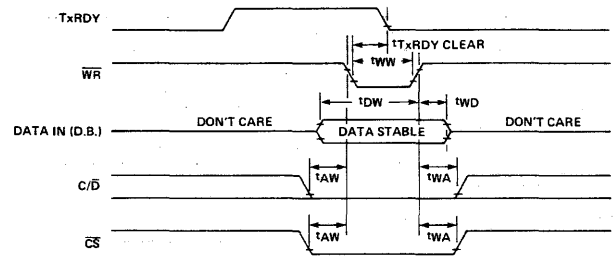
Transmitter Clock & Data



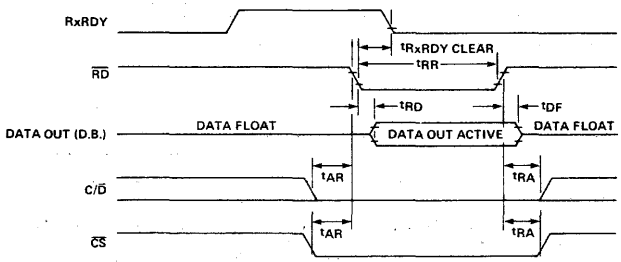
Receiver Clock & Data



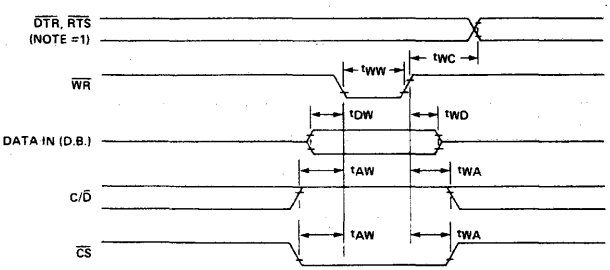
Write Data Cycle (CPU → USART)



Read Data Cycle (CPU ← USART)

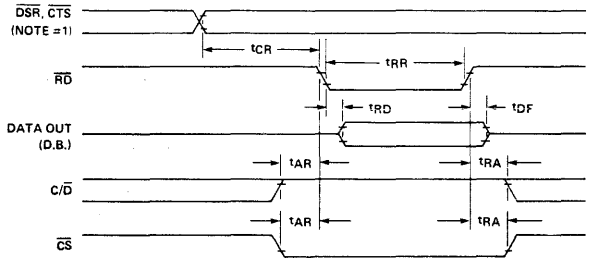


Write Control or Output Port Cycle (CPU → USART)



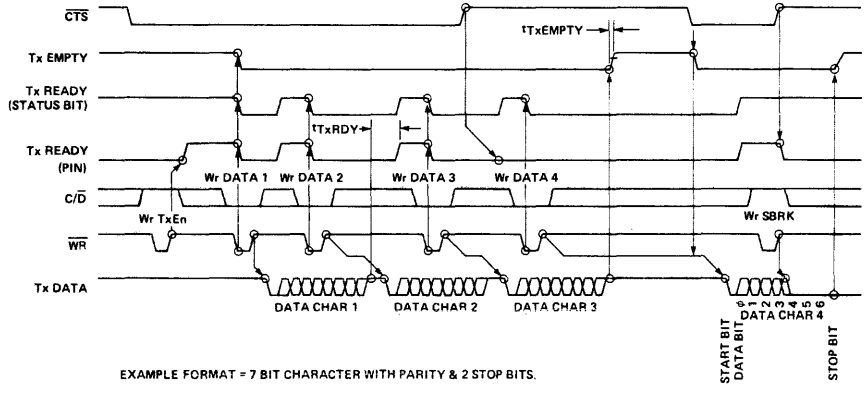
NOTE #1: T_{WC} INCLUDES THE RESPONSE TIMING OF A CONTROL BYTE.

Read Control or Input Port (CPU ← USART)



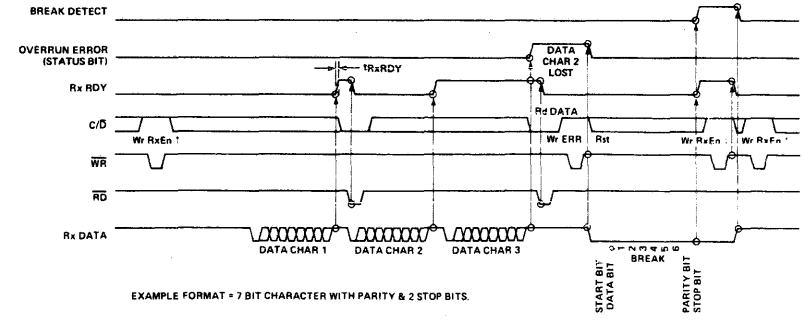
NOTE #1: T_{CR} INCLUDES THE EFFECT OF $\overline{CTS}$ ON THE TxENBL CIRCUITRY.

Transmitter Control & Flag Timing (ASYNC Mode)



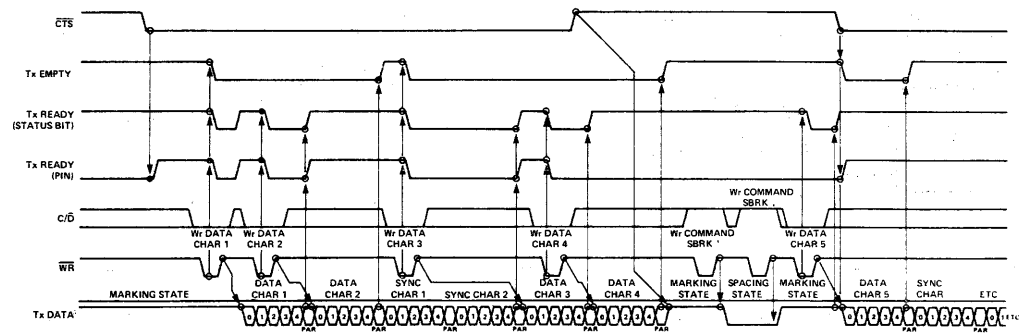
EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY & 2 STOP BITS.

Receiver Control & Flag Timing (ASYNC Mode)



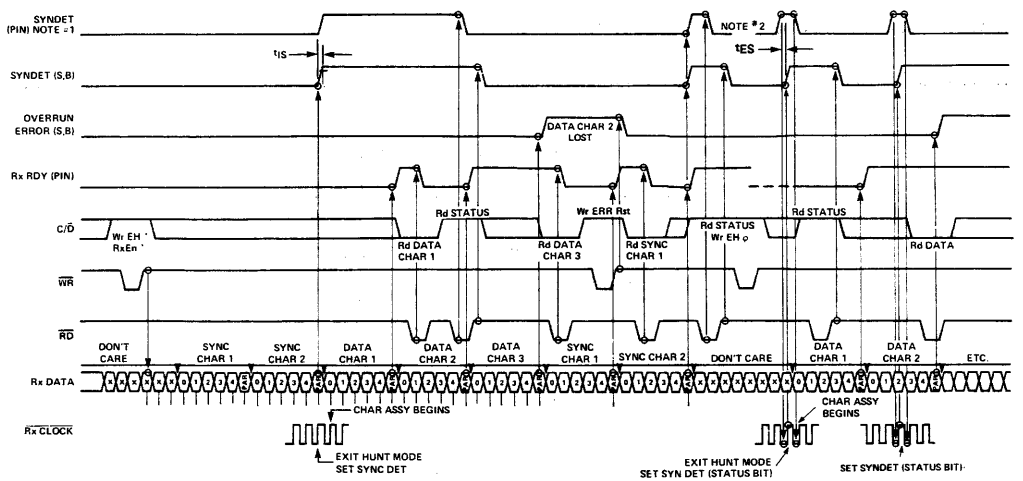
EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY & 2 STOP BITS.

Transmitter Control & Flag Timing (SYNC Mode)



EXAMPLE FORMAT = 5 BIT CHARACTER WITH PARITY, 2 SYNC CHARACTERS.

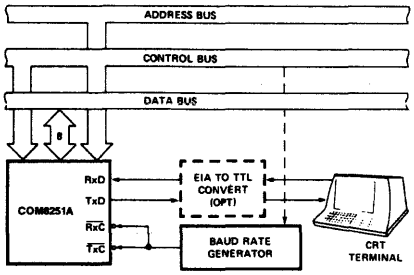
Receiver Control & Flag Timing (SYNC Mode)



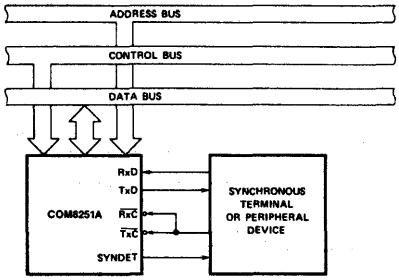
NOTE #1: INTERNAL SYNC, 2 SYNC CHARACTERS, 5 BITS, WITH PARITY
NOTE #2: EXTERNAL SYNC, 5 BITS, WITH PARITY

APPLICATION OF THE COM8251A

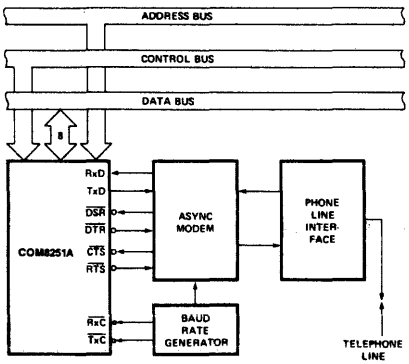
Asynchronous Serial Interface to CRT Terminal, DC to 9600 Baud



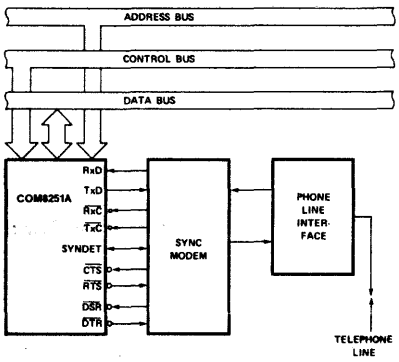
Synchronous Interface to Terminal or Peripheral Device



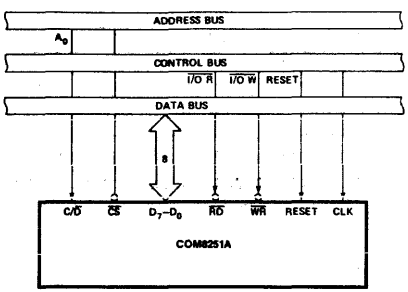
Asynchronous Interface to Telephone Lines



Synchronous Interface to Telephone Lines



COM8251A Interface to μP Standard System Bus

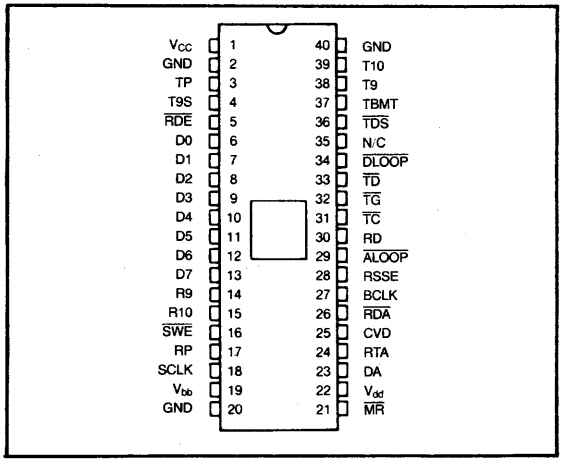


IBM 3274/3276 Compatible COAX Receiver/Transmitter

FEATURES

- ☐ Conforms to the IBM 3270 Interface Display System Standard
- ☐ Transmits and Receives Manchester II Code
- ☐ Detects and Generates Line Quiesce, Code Violation, Sync, Parity, and Ending Sequence (Mini Code Violation)
- ☐ Multi Byte or Single Byte Transfers
- ☐ Double Buffer Receiver and Transmitter
- ☐ Separate Data and Status Select
- ☐ Operates at 2.3587 MHz
- ☐ TTL Compatible Inputs and Outputs
- ☐ COPLAMOS® n-Channel Silicon Gate Technology

PIN CONFIGURATION

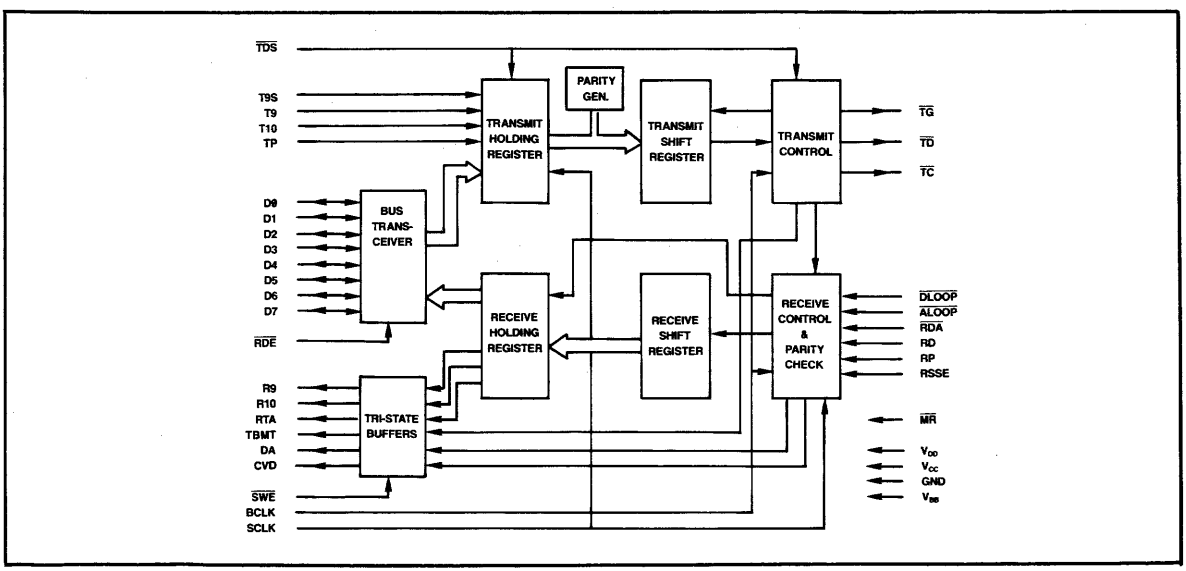


GENERAL DESCRIPTION

The COM 9004 is an MOS/LSI circuit which may be used to facilitate high speed data transmission. The COM 9004 is fabricated using SMC's patented COPLAMOS® technology and may be used to implement an interface between IBM 3274/3276 compatible control units and 3278/3287/3289 compatible terminal units. The receiver and transmitter sections of the COM 9004 are separate and may be used independently of each other.

The COM 9004 generates and detects the line quiesce, code violation, parity, and mini code violation bit patterns.

The on-chip parity logic is capable of generating and checking either even or odd parity for the entire 10 bit data word. In addition, parity may be generated for the least significant 8 bits of the data word (this parity bit would replace the ninth data bit).



ORGANIZATION

The COM 9004 is organized into 9 major sections. Communication between each section is achieved via internal data and control busses.

Transmitter Holding Register

The transmit holding register is a 12 bit latch. This latch is loaded with the transmit data and parity generation information from the system bus.

Tri-State Buffers

These buffers allow gating of the COM 9004's status word onto the system data bus.

Bus Transceiver

The bus transceiver allows bi-directional data transfer between the system data bus and the transmit and receive holding registers.

Parity Generator

This logic determines and generates the correct parity for the data in the transmitter holding register.

Transmitter Control

This logic generates signals required to enable external transmit circuitry. It also generates the Line Quiesce, Code Violation, sync bits and Mini Code Violation patterns.

Transmitter Shift Register

The transmitter shift register is an 11 bit parallel to serial shift register. It accepts data from the transmitter holding register and the parity generation logic and converts it into serial form for transmission.

Receive Control/Parity Check

This logic checks the received character for the specified parity and ensures that no Transmit Check conditions occurred. It also handles the self test mode and generates a strobe when the complete data word is received.

Receiver Shift Register

This logic is a serial to parallel shift register that converts the received information into a 10 bit data word and RTA status bit.

Receiver Holding Register

This register holds the assembled data word until it is read by the processor.

DESCRIPTION OF PIN FUNCTIONS
Processor Related Signals

PIN NO.	NAME	SYMBOL	FUNCTION
6-13	Transmit/ Receive Data Bits	D0-D7	Bidirectional: 8 bit, three state data port used to transfer data between the COM 9004 and the processor. D0 is the first bit transmitted.
4	Transmit Bit 9 Select	T9S	Input: A low level on this pin enables T9 to be transmitted as bit 9. A high level on this pin causes T9 to determine the type of parity bit generated for bits D0-D7.
38	Transmit Bit 9	T9	Input: If T9S is low, this supplies transmit bit 9. If T9S is high, then T9 low forces odd parity and T9 high forces even parity to be generated for D0-D7. In this case the parity bit generated is transmit bit 9.
39	Transmit Bit 10	T10	Input: This pin supplies transmit bit 10.
3	Transmit Parity	TP	Input: This input controls the parity bit for transmit bits 1-10. A low level on this pin causes odd parity and a high level on this pin causes even parity to be generated for bits 1-10. The parity bit generated is transmit bit 11.
18	System Clock	SCLK	Input: This signal is used to synchronize the COM 9004. The transmitter is loaded and started on the low to high transition of SCLK if TDS is low. DA is reset on the low to high transition of SCLK if RDA is low.
36	Transmitter Data Strobe	$\overline{TDS}$	Input: This input and SCLK are used to load the transmitter holding register and start the transmit sequence. Code Violation Detect (CVD) is reset at this time.
26	Reset Data Available	$\overline{RDA}$	Input: This input and SCLK are used to reset DA.
16	Status Word Enable	$\overline{SWE}$	Input: A low level at this pin enables the status word buffer outputs (DA, CVD, TBMT, R9, R10, and RTA). A high level on $\overline{SWE}$ places the status word buffer outputs in a high impedance state.
23	Receive Data Available	DA	This three-state output signal is at a high level when an entire word has been received and transferred into the receiver buffer register. It is only set if a Transmit Check Condition did not occur.
25	Code Violation Detected	CVD	This three-state output signal is at a high level if a valid Code Violation was detected at the receiver since the last time the transmitter was loaded. It is reset when the transmitter is loaded.
37	Transmit Buffer Empty	TBMT	This three-state output signal is at a high level when the transmit holding register may be loaded with new data.
14	Receive Bit 9	R9	This three-state output signal is receiver data bit 9.
15	Receive Bit 10	R10	This three-state output signal is receiver data bit 10.
24	Receiver Turn-around	RTA	This three-state output signal is set to a high level when a valid Mini Code Violation is detected. It is only set if a Transmit Check did not occur. It is reset when the transmitter is loaded.
5	Receive Data Enable	$\overline{RDE}$	Input: A low level enables the outputs of the receive data register D0-D7.
17	Receiver Parity	RP	Input: This input determines whether the entire received word will be checked for even or odd parity. A low at this pin will cause a check for odd parity and a high at this pin will cause a check for even parity. This input has an internal pull-up resistor.

DESCRIPTION OF PIN FUNCTIONS (cont.)

PIN NO.	NAME	SYMBOL	FUNCTION
29	Analog Loopback	$\overline{ALOOP}$	Input: A low level on this pin disables the receiver except when the transmitter is active. A high level on this pin and $\overline{DLOOP}$ will cause the receiver to be disabled while the transmitter is active. $\overline{ALOOP}$ is used to allow loop-back through the line drivers and receivers. This input has an internal pull-up resistor.
34	Digital Loopback	$\overline{DLOOP}$	Input: A low level on this pin disables the receiver except when the transmitter is active. $\overline{TG}$ is forced to a high level to disable the external coax driver. Data input to the receiver is internally wrapped from the transmitter data output. This input has an internal pull-up resistor.
21	Master Reset	$\overline{MR}$	Input: This input should be pulsed low after power-on. This signal resets DA to a low level and sets $\overline{TG}$ and TBMT to a high level. This input has an internal pull-up.
1	Supply Voltage	V_{cc}	+5 volt supply
22	Supply Voltage	V_{dd}	+12 volt supply
19	Supply Voltage	V_{bb}	−12 volt supply
2, 20, 40	Ground	GND	GROUND

Device Related Signals

PIN NO.	NAME	SYMBOL	FUNCTION
27	Baud Rate Clock	BCLK	This input is a clock whose frequency is 8 times the desired transmitter and receiver baud rate (typically 18.8696 MHz for 3274/3276 operation). This input is not TTL compatible.
33	Transmit Data	$\overline{TD}$	Output: Serial data from the transmitter. This signal is a biphase Manchester II encoded bit stream. This output is high when no data is being transmitted.
31	Transmit Clock	$\overline{TC}$	The Transmit Clock output is ½ the frequency of BCLK. It is synchronized with TD and used to provide external pre-distortion timing.
30	Receive Data	RD	Input: Accepts the serial biphase Manchester II encoded bit stream.
32	Transmit Gate	$\overline{TG}$	Output: This signal is low during the time that the transmit data is valid. TG is used to turn on the external transmit circuitry.
28	Receive Single Shot Enable	RSSE	Input: A high level on this pin enables an internal digital single shot on RD. This limits a high level on RD to 3 clock times. Also when high it will cause the receiver not to detect a valid Code Violation. A low level disables the single shot causing no reshaping of the RD input signal.

COM 9004 OPERATION

The COM 9004 consists of a receiver section that converts Manchester II phase encoded serial data to parallel data and a transmitter section that converts parallel data to Manchester II phase encoded serial data.

Receiver

Message transfers must conform to the IBM 3270 protocol in order for the COM 9004 to acknowledge them.

The received message is checked for the Code Violation sequence (start sequence) bit pattern, preceding the first data word, and Mini Code Violation (end sequence) following the last data word.

The data word consists of 10 data bits, a sync bit and a parity bit.

The data word along with the first bit of the next word or ending zero (bit 13) is shifted into a shift register. Once it is assembled it is transferred and held in the holding register until another data word is assembled. The 13th bit is inverted and presented to the bus or RTA (receiver turn-around). Therefore RTA is set high on the last word of a message and is reset when the transmitter is loaded with the response or on the rising edge of SCLK if RDA is held low.

Once the data word is in the holding register and parity is correct the data available (DA) status signal is set high.

The Code Violation Detect signal (CVD) goes active high after a line Quiesce, Code Violation and sync bit have been detected by the receiver. It is reset when the transmitter of the COM 9004 is asserted. By examining this signal, the processor can determine whether a timeout or Transmit Check condition caused a receiver error.

The receive input is sampled at 8 times the data rate. The receiver logic is brought into bit synchronization during the Line Quiesce pattern. Once the Code Violation following the Line Quiesce is detected, the receiver is brought into bit and word synchronization. The internal receiver clock is adjusted after each transition to compensate for jitter and distortion in the received data signal.

Transmitter

The transmitter section basically consists of a 12-bit holding register, parallel to serial shift register and a parity generator. The firmware initiates a transmit sequence by strobing $\overline{TDS}$ low. The data is loaded into the holding register on the rising edge of SCLK while TDS is low. Nine bits of data (D0-D7 and T10) are transferred without change to the transmit shift register. The logic level of T9S determines whether T9 will be transmitted as parity on the preceding eight bits, or as data.

After the processor loads the transmit holding register with data, status signal TBMT is driven inactive low until the COM 9004 transfers the data from the transmit holding register to the transmit shift register. After the transfer, TBMT is driven

high. The processor should not try to load data into the COM 9004 while TBMT is low. When initiating a data transmission, the COM 9004 automatically transmits a Line Quiesce pattern and a Code Violation. The data is then shifted out of the shift register with a sync bit (1) inserted before the data word, and a parity bit appended after the data word.

If a new word is loaded into the COM 9004 before the parity bit of the previous word has been transmitted, a sync bit (1) followed by the new data bits is transmitted. If not, after the COM 9004 transmits the last data word (no more transmit sequences are started), a sync bit (0) and a Mini Code Violation is appended to the end of the message.

Output $\overline{TG}$ goes active low one-half bit cell time before the first Line Quiesce character is output. It is made inactive (high) during the transmission of the Mini Code Violation.

Diagnostic Modes

NORMAL OPERATION ($\overline{ALOOP}$ AND $\overline{DLOOP}$ HIGH)
Internal read data signal follows the RD input as long as the COM 9004's transmitter is off. The receiver will be disabled while the transmitter is active.

ANALOG LOOPBACK ($\overline{ALOOP}$ LOW AND $\overline{DLOOP}$ HIGH)
The internal read data signal follows the RD input as long as the COM 9004's transmitter is active.

DIGITAL LOOPBACK $\overline{ALOOP}$ HIGH AND $\overline{DLOOP}$ LOW)
The internal read data signal follows an internally generated and latched valid transmit signal (only when the transmitter is active.) The output $\overline{TG}$ is disabled in digital loopback mode.

DISABLE RECEIVER ($\overline{ALOOP}$ AND $\overline{DLOOP}$ LOW)
The internal read data signal is held low and output $\overline{TG}$ is disabled.

MESSAGE FORMATS

Single Byte Transmission

COAX IDLE	LINE QUIESCE	CODE VIOLATION	SYNC BIT	DATA (10 BITS)	PARITY BIT	ENDING SEQUENCE	COAX IDLE

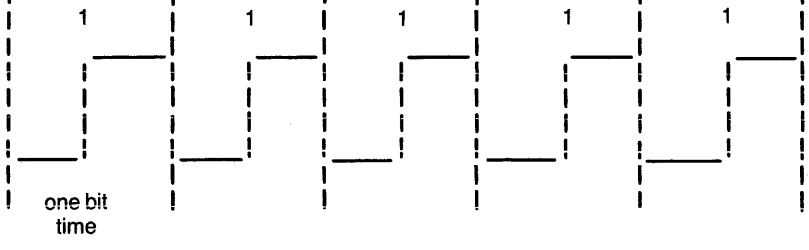
Multiple Byte Transmission

COAX IDLE	LINE QUIESCE	CODE VIOLATION	SYNC BIT	DATA 1 (10 BITS)	PARITY BIT	SYNC BIT	DATA 2 (10 BITS)

PARITY BIT	.....	SYNC BIT	DATA N (10 BITS)	PARITY BIT	ENDING SEQUENCE	COAX IDLE

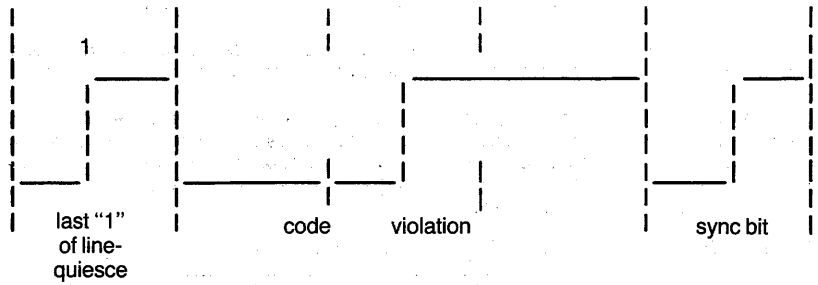
Bits on the coax appear as positive and negative going pulses. A positive pulse to negative pulse transition in the middle of the bit cell is interpreted as a logical '0'. A negative pulse to positive pulse transition in the middle of a bit cell is interpreted as a logical '1'. A predistortion pulse is generated for every pulse transition from an up to down level or a down to up level.

Line Quiesce Pattern



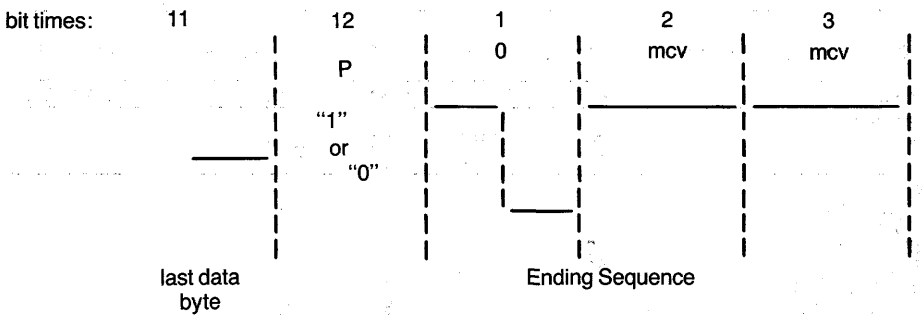
The Line Quiesce pattern consists of five contiguous logical ones. It establishes an equilibrium condition on the coax following line turnaround.

Code Violation Pattern



The Code Violation pattern is a bit sequence containing no mid-bit time level transition in two of its three bit cells. It is a unique pattern that violates the encoding rules and indicates the start of valid data.

Mini Code Violation Pattern



The Mini Code Violation (MCV) pattern is a bit sequence containing no mid-bit time level transition in either of its bit cells. It is a unique code that violates the encoding rules and indicates the end of valid transmit data.

Transmit Check

A Transmit Check is defined as follows:

1) A logical zero sync bit in the ending sequence not followed by a Mini Code Violation.
2) Loss of a level transition at the mid-bit time during other than a normal ending sequence.
3) A transmission parity error.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55° to +150°C
Lead Temperature (soldering, 10 sec.)	+300°C
Positive Voltage on any I/O Pin, with respect to ground	+18.0V
Negative Voltage on any I/O Pin, with respect to ground	−0.3V
Power Dissipation	0.75W

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

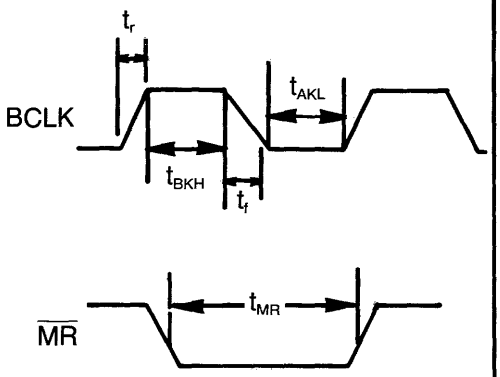
DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, V_{BB} = −12V ±5%)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE					
V_{IL} Low	−0.3		.8	V	
V_{IH} High	2.0		V_{CC}	V	(Except BCLK)
V_{IH} High	4.3		V_{CC}+.3	V	(BCLK only)
OUTPUT VOLTAGE					
V_{OL} Low			.4		I_{OL} = 2.0 mA
V_{OH} High	2.4				I_{OH} = −.25 mA
POWER SUPPLY CURRENT					
I_{CC}		70		mA	All outputs = V_{OH}
I_{DD}		16		mA	
I_{BB}		5		mA	
INPUT LEAKAGE CURRENT					
All input pins			.01	mA	V_{IN} = 0 to V_{CC}
CAPACITANCE					
C_{IN}			10	pf	(Except BCLK)
C_{IN}			35	pf	(BCLK only)

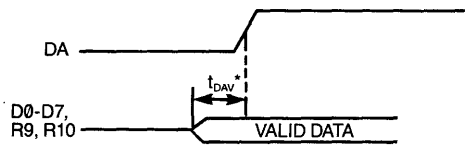
AC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, V_{BB} = −12V ±5%)

PARAMETER		MIN	TYP	MAX	UNIT	CONDITIONS
Clock Frequency						
B_{CLK}		7	18.8696	18.9	MHz	
S_{CLK}		DC	4.7474	5	MHz	
Clock Width						
t_{SKH}	SCLK High	80			ns	
t_{SKL}	SCLK Low	80			ns	
t_{BKH}	BCLK High	20			ns	
t_{BKH}	BCLK Low	20			ns	
t_r	BCLK rise time			6	ns	
t_F	BCLK fall time			6	ns	
t_{RDD}	$\overline{RDE}$ to Data Valid Delay			50	ns	
t_{SDD}	$\overline{SWE}$ to Data Valid Delay			50	ns	
t_{DF}	Data Read to Bus Float			50	ns	
t_{DS}	Data Setup Time	100			ns	
t_{DH}	Data Hold Time	0			ns	
t_{DAV}	DA to receive data valid delay	−100		100	ns	
t_{TC}	TC clock period		106		ns	
$t_{\overline{TGLD}}$	TC to TG low delay	−53		30	ns	
$t_{\overline{TGHD}}$	TC to TG high delay			30	ns	
t_{TDS}	Transmit data to TG setup time	10			ns	
t_{TDH}	Transmit data to TC hold time	20			ns	
t_D	TBMT active to de-active		200		ns	
t_{DDC}	TBMT cycle			3.2	µs	
t_{DD}	$\overline{TBMT}$ de-activated	1		2	µs	
t_{DSS}	$\overline{TDS}$ set up	100		200	ns	
t_{DSH}	$\overline{TDS}$ hold	0		100	ns	
t_{MR}	$\overline{MR}$ pulse width	300			ns	

MISC. TIMING

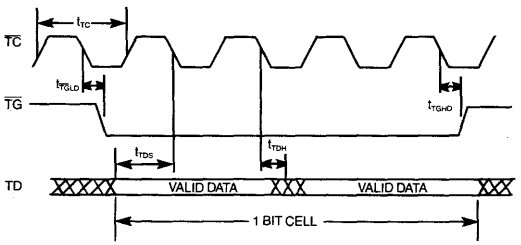


RECEIVE DATA TIMING

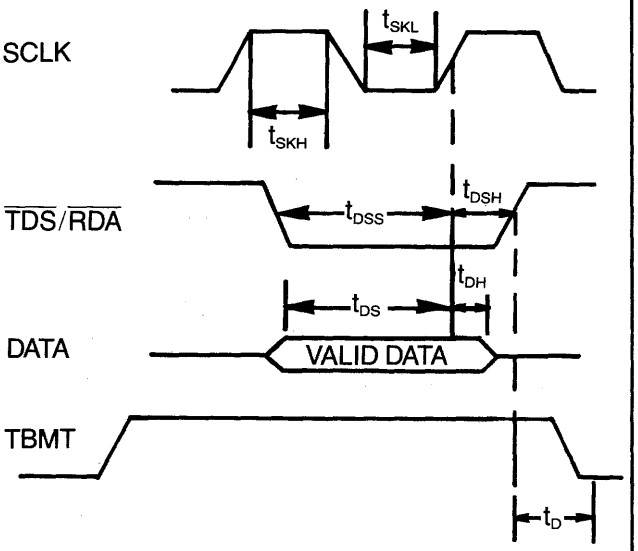


*DA may occur from 100 ns before to 100 ns after data is valid.

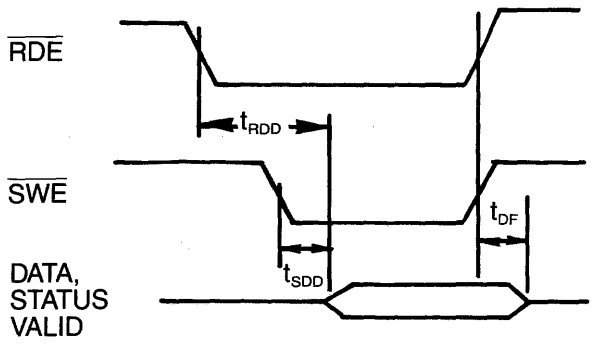
TRANSMITTER TIMING



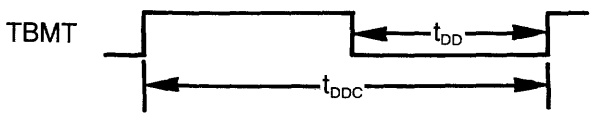
BUS INPUT TIMING

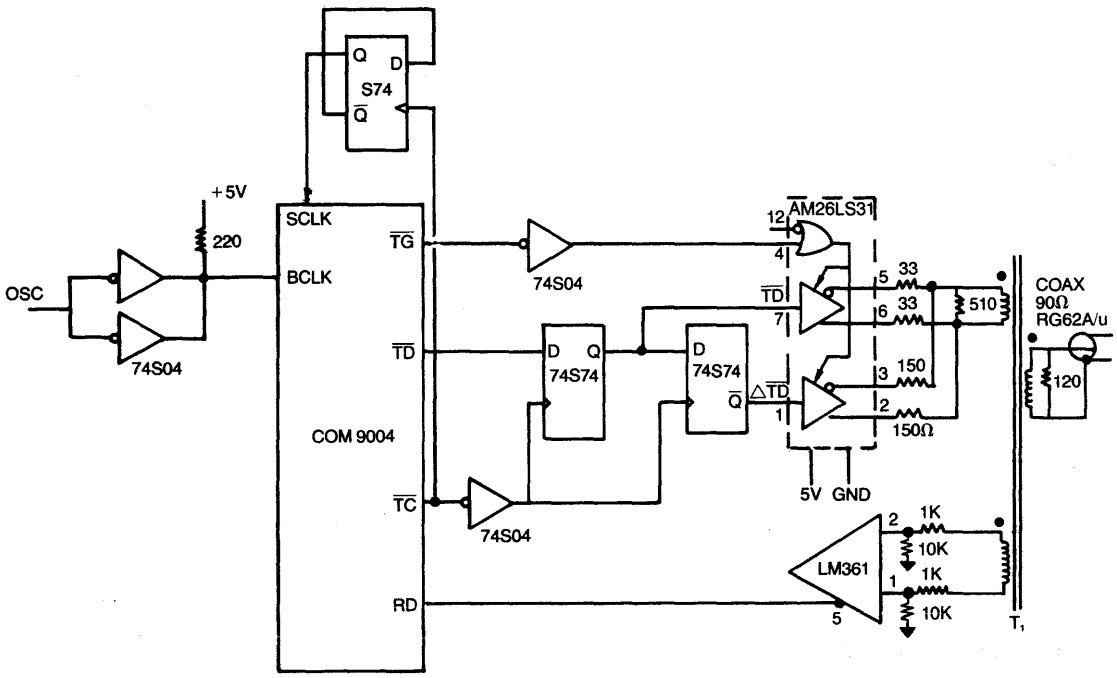


BUS OUTPUT TIMING



TBMT CYCLE





NOTE: 1. T1–1:1:1 PULSE TRANSFORMER (TECHNITROL PART NO. 11LHA OR EQUIV)
2. ALL RESISTOR IN OHMS

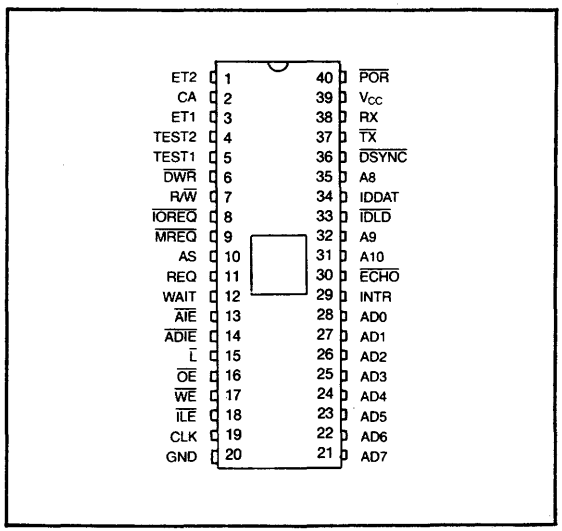
TYPICAL COAX INTERFACE

Local Area Network Controller LANC™

FEATURES

- ☐ 2.5 M bit data rate
- ☐ ARCNET* local area network controller
- ☐ Modified token passing protocol
- ☐ Self-reconfiguring as nodes are added or deleted from network
- ☐ Handles variable length data packets
- ☐ 16 bit CRC check and generation
- ☐ System efficiency increases with network loading
- ☐ Standard microprocessor interface
- ☐ Supports up to 255 nodes per network segment
- ☐ Ability to interrupt processor at conclusion of commands
- ☐ Interfaces to an external 1K or 2K RAM buffer
- ☐ Arbitrates buffer accesses between processor and COM 9026
- ☐ Replaces over 100 MSI/SSI parts
- ☐ Ability to transmit broadcast messages
- ☐ Compatible with broadband or baseband systems
- ☐ Compatible with any interconnect media (twisted pair, coax, etc.)

PIN CONFIGURATION



- ☐ Arbitrary network configurations can be used (star, tree, etc.)
- ☐ Single +5 volt supply

GENERAL DESCRIPTION

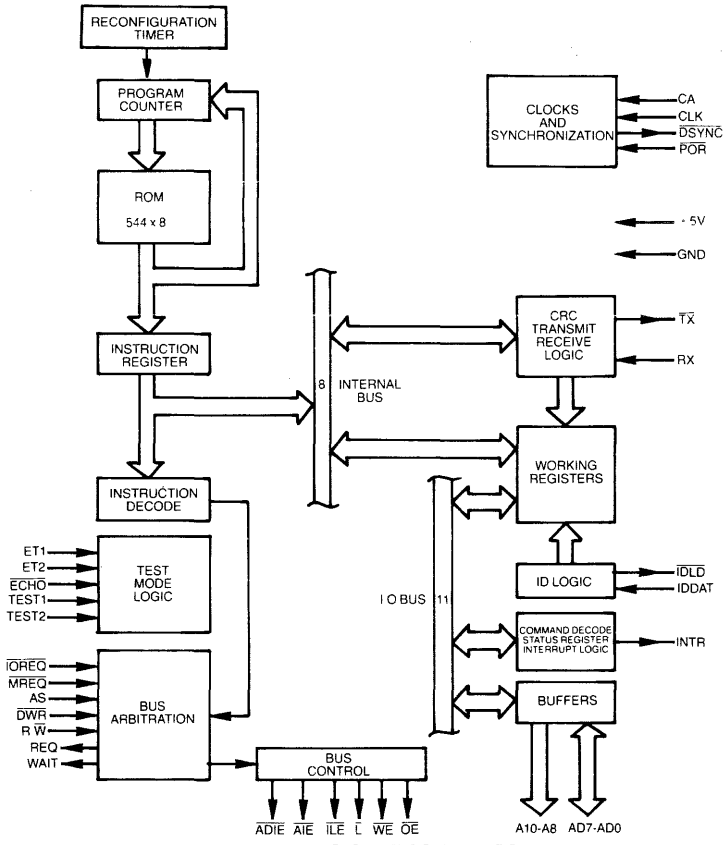
The COM 9026 is a special purpose communications adapter for interconnecting processors and intelligent peripherals using the ARCNET local area network. The ARCNET local area network is a self-polling "modified token passing" network operating at a 2.5 M bit data rate. A "modified token passing" scheme is one in which all token passes are acknowledged by the node accepting the token. The token passing network scheme avoids the fluctuating channel access times caused by data collisions in so-called CSMA/CD schemes such as Ethernet.

The COM 9026 circuit contains a microprogrammed sequencer and all the logic necessary to control the token passing mechanism on the network and send and receive data packets at the appropriate time. A maximum of 255 nodes may be connected to the network with each node being assigned a unique ID.

The COM 9026 establishes the network configuration, and automatically re-configures the network as new nodes are added or deleted from the network. The COM 9026 performs address decode, CRC checking and generation, and packet acknowledgement, as well as other network management functions. The COM 9026 interfaces directly to the host processor through a standard multiplexed address/data bus.

An external RAM buffer of up to 2K locations is used to hold up to four data packets with a maximum length of 508 bytes per message. The RAM buffer is accessed both by the processor and the COM 9026. The processor can write commands to the COM 9026 and also read COM 9026 status. The COM 9026 will provide all signals necessary to allow smooth arbitration of all RAM buffer operations.

*ARCNET is a registered trademark of the Datapoint Corporation.



COM 9026 BLOCK DIAGRAM

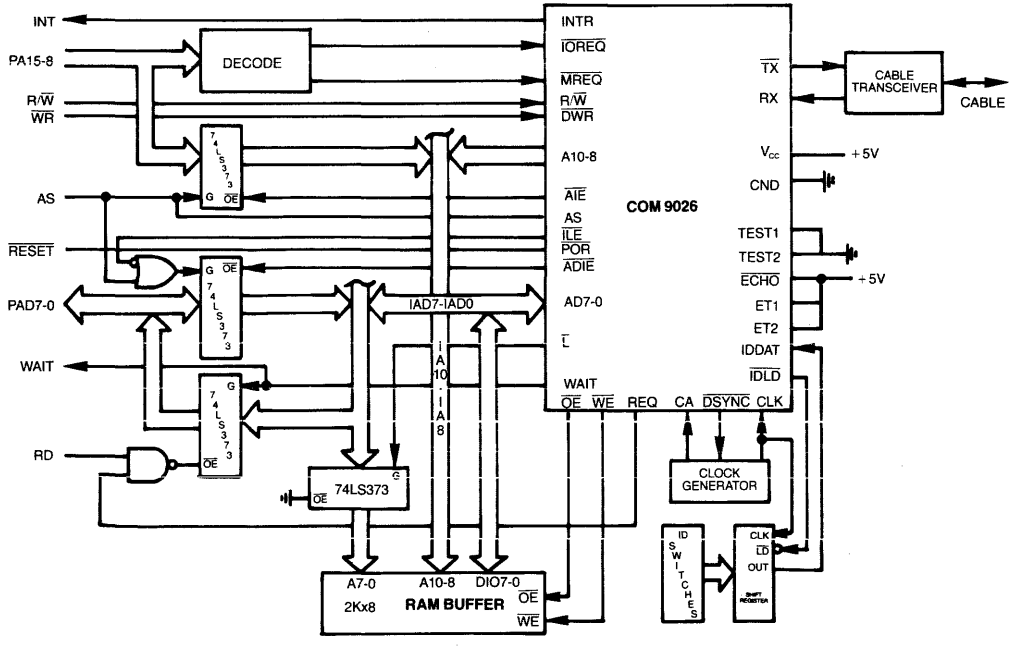


FIGURE 2—TYPICAL COM 9026 INTERFACE

DESCRIPTION OF PIN FUNCTIONS (refer to figure 2)

PIN NO.	NAME	SYMBOL	FUNCTION
31, 32, 35	ADDRESS 10, 9, 8	A10, A9, A8	These three output signals are the three most significant bits of the RAM buffer address. These signals are in their high impedance state except during COM 9026 access cycles to the RAM buffer. A10 and A9 will take on the value nn as specified in the ENABLE RECEIVE or ENABLE TRANSMIT commands to or from page nn and should be viewed as page select bits. For packets less than 256 bytes a 1K buffer can be used with A8 unconnected. For packets greater than 256 bytes, a 2K buffer is needed with A8 connected.
21, 22, 23, 24, 25, 26, 27, 28	ADDRESS/ DATA 7-0	AD7-AD0	These 8 bidirectional signals are the lower 8 bits of the RAM buffer address and the 8 bit data path in and out of the COM 9026. AD0 is also used for I/O command decoding of the processor control or status commands to the COM 9026.
8	I/O REQUEST	$\overline{\text{IOREQ}}$	This input signal indicates that the processor is requesting the use of the data bus to receive status information or to issue a command to the COM 9026. This signal is sampled internally on the falling edge of AS.
9	MEMORY REQUEST	$\overline{\text{MREQ}}$	This input signal indicates that the processor is requesting the use of the data bus to transfer data to or from the RAM buffer. This signal is sampled internally on the falling edge of AS.
7	READ/$\overline{\text{WRITE}}$	R/$\overline{\text{W}}$	A high level on this input signal indicates that the processor's access cycle to the COM 9026 or the RAM buffer will be a read cycle. A low level indicates that a write cycle will be performed to either the RAM buffer or the COM 9026. The write cycle will not be completed, however, until the $\overline{\text{DWR}}$ input is asserted. This signal is an internal transparent latch gated with AS.
10	ADDRESS STROBE	AS	This input signal is used by the COM 9026 to sample the state of the $\overline{\text{IOREQ}}$, $\overline{\text{MREQ}}$ and R/$\overline{\text{W}}$ inputs. The COM 9026 bus arbitration is initiated on the falling edge of this signal.
11	REQUEST	REQ	This output signal acknowledges the fact that the processor's I/O or memory cycle has been sampled. The signal is equal to $\overline{\text{MREQ}}$ or $\overline{\text{IOREQ}}$ passed through an internal transparent latch gated with AS.
12	WAIT	WAIT	This output signal is asserted by the COM 9026 at the start of a processor access cycle to indicate that it is not ready to transfer data. WAIT returns to its inactive state when the COM 9026 is ready for the processor to complete its cycle.
6	DELAYED WRITE	$\overline{\text{DWR}}$	This input signal informs the COM 9026 that valid data is present on the processor's data bus for write cycles. The COM 9026 will remain in the WAIT state until this signal is asserted. $\overline{\text{DWR}}$ has no effect on read cycles. If the processor is able to satisfy the write data setup time, it is recommended that this signal be grounded.
29	INTERRUPT REQUEST	INTR	This output signal is asserted when an enabled interrupt condition has occured. INTR returns to its inactive state by resetting the interrupting status condition or the corresponding interrupt mask bit.
18	INTERFACE LATCH ENABLE	$\overline{\text{ILE}}$	This output signal, in conjunction with $\overline{\text{ADIE}}$, gates the processor's address/data bus (PAD7-PAD0) onto the interface address/data bus (IAD7-IAD0) during the data valid portion of a Processor Write RAM or Processor Write COM 9026 operation.
14	ADDRESS/ DATA INPUT ENABLE	$\overline{\text{ADIE}}$	This output signal enables the processor's address/data bus (PAD7-PAD0) captured by AS or $\overline{\text{ILE}}$ onto the interface address/data bus (IAD7-IAD0).
13	ADDRESS INPUT ENABLE	$\overline{\text{AIE}}$	This output signal enables the processor's upper 3 address bits (PA10-PA8) onto the interface address bus (IA10-IA8).
15	LATCH	$\overline{\text{L}}$	This output signal latches the interface address/data bus (IAD7-IAD0) into a latch which feeds the lower 8 address bits of the RAM buffer during address valid time of all RAM buffer access cycles.
17	WRITE ENABLE	$\overline{\text{WE}}$	This output signal is used as a write pulse to the external RAM buffer. Data is referenced to the trailing edge of $\overline{\text{WE}}$.
16	OUTPUT ENABLE	$\overline{\text{OE}}$	This output signal enables the RAM buffer output data onto the interface address/data bus (IAD7-IAD0) during the data valid portion of all RAM buffer read operations.
33	ID LOAD	$\overline{\text{IDLD}}$	This output signal synchronously loads the value selected by the ID switches into an external shift register in preparation for shifting the ID into the COM 9026. The shift register is clocked with the same signal that feeds the COM 9026 on pin 19 (CLK). The timing associated with this signal and IDDAT (pin 34) is illustrated in figure 19.
34	ID DATA IN	IDDAT	This input signal is the serialized output from the external ID shift register. The ID is shifted in most significant bit first. A high level is defined as a logic "1".
1, 3	EXTENDED TIMEOUT FUNCTION 2, 1	ET2, ET1	The levels on these two input pins specify the timeout durations used by the COM 9026 in its network protocol. Refer to the section entitled "Extended Timeout Function" for details.
37	TRANSMIT DATA	$\overline{\text{TX}}$	This output signal contains the serial transmit data to the CABLE TRANSCEIVER.
38	RECEIVE DATA	RX	This input signal contains the serial receive data from the CABLE TRANSCEIVER.

DESCRIPTION OF PIN FUNCTIONS (Continued)

PIN NO.	NAME	SYMBOL	FUNCTION
4, 5	TEST PIN 2 TEST PIN 1	TEST2 TEST1	These input pins are grounded for normal chip operation. These pins are used in conjunction with ET2 and ET1 to enable various internal diagnostic functions when performing chip level testing.
30	ECHO DIAGNOSTIC ENABLE	$\overline{ECHO}$	When this input signal is low, the COM 9026 will re-transmit all messages of length less than 254 bytes. This input should be tied high for normal chip operation and is only utilized when performing chip level testing.
19	CLOCK	CLK	A continuous 5 MHz clock input used for timing of the COM 9026 bus cycles, bus arbitration, serial ID input, and the internal timers.
2	CA	CA	This input signal is a 5 MHz clock used to control the operation of the COM 9026 microcoded sequencer. This input is periodically halted in the high state by the $\overline{DSYNC}$ output.
36	DELAYED SYNC	$\overline{DSYNC}$	This output signal is asserted by the COM 9026 to cause the external clock generator logic to halt the CA clock. Refer to figure 9.
40	POWER ON RESET	$\overline{POR}$	This input signal clears the COM 9026 microcoded sequencer program counter to zero and initializes various internal control flags and status bits. The POR status bit is also set which causes the INTR output to be asserted. Repeated assertion of this signal will degrade the performance of the network.
39	+5 VOLT SUPPLY	V_{CC}	Power Supply
20	GROUND	GND	Ground

PROTOCOL DESCRIPTION

LINE PROTOCOL DESCRIPTION

The line protocol can be described as isochronous because each byte is preceded by a start interval and ended with a stop interval. Unlike asynchronous protocols, there is a constant amount of time separating each data byte. Each byte will take up exactly 11 clock intervals with a single clock interval being 400 nanoseconds in duration. As a result, 1 byte is transmitted every 4.4 microseconds and the time to transmit a message can be exactly determined. The line idles in a spacing (logic 0) condition. A logic '0' is defined as no line activity and a logic 1 is defined as a pulse of 200 nanoseconds duration. A transmission starts with an ALERT BURST consisting of 6 unit intervals of mark (logic 1). Eight bit data characters are then sent with each character preceded by 2 unit intervals of mark and one unit interval of space. Five types of transmission can be sent as described below:

Invitations To Transmit

An ALERT BURST followed by three characters; an EOT (end of transmission—ASCII code 04 HEX) and two (repeated) DID (Destination IDentification) characters. This message is used to pass the token from one node to another.

Free Buffer Enquiries

An ALERT BURST followed by three characters; an ENQ (ENQuiry—ASCII code 05 HEX) and two (repeated) DID (Destination IDentification) characters. This message is used to ask another node if it is able to accept a packet of data.

Data Packets

An ALERT BURST followed by the following characters:

- — an SOH (start of header-ASCII code 01 HEX)
- —a SID (Source IDentification) character
- —two (repeated) DID (destination IDentification) characters.
- —a single COUNT character which is the 2's complement of the number of data bytes to follow if a "short packet" is being sent or 00 HEX followed by a COUNT character which is the 2's complement of the number of data bytes to follow if a "long packet" is being sent.
- —N data bytes where COUNT = 256-N (512-N for a "long packet")
- —two CRC (Cyclic Redundancy Check) characters. The CRC polynomial used is $X^{16} + X^{15} + X^2 + 1$.

Acknowledgements

An ALERT BURST followed by one character; an ACK (ACKnowledgement—ASCII code 06 HEX) character. This message is used to acknowledge reception of a packet or as an affirmative response to FREE BUFFER ENQUIRIES.

Negative Acknowledgements

An ALERT BURST followed by one character; a NAK (Negative AcKnowledgement—ASCII code 15 HEX). This message is used as a negative response to FREE BUFFER ENQUIRIES.

NETWORK PROTOCOL DESCRIPTION

Communication on the network is based on a "modified token passing" protocol. A "modified token passing" scheme is one in which all token passes are acknowledged by the node receiving the token. Establishment of the network configuration and management of the network protocol are handled entirely by the COM 9026's internal microcoded sequencer. A processor or intelligent peripheral transmits data by simply loading a data packet and its destination ID into the RAM buffer, and issuing a command to enable the transmitter. When the COM 9026 next receives the token, it verifies that the receiving node is ready by first transmitting a FREE BUFFER ENQUIRY message. If the receiving node transmits an ACKnowledge message, the data packet is transmitted followed by a 16 bit CRC. If the receiving node cannot accept the packet (typically its receiver is inhibited), it transmits a Negative AcKnowledge message and the transmitter passes the token. Once it has been established that the receiving node can accept the packet and transmission is complete, the receiving node will verify the packet.

If the packet is received successfully, the receiving node transmits an acknowledge message (or nothing if it is received unsuccessfully) allowing the transmitter to set the appropriate status bits to indicating successful or unsuccessful delivery of the packet. An interrupt mask permits the COM 9026 to generate an interrupt to the processor when selected status bits become true. Figure 3 is a flow chart illustrating the internal operation of the COM 9026.

NETWORK RECONFIGURATION

A significant advantage of the COM 9026 is its ability to adapt to changes on the network. Whenever a new node is activated or deactivated a NETWORK RECONFIGURATION is performed. When a new COM 9026 is turned on (creating a new active node on the network), or if the COM 9026 has not received an INVITATION TO TRANSMIT for 840 milliseconds, it causes a NETWORK RECONFIGURATION by sending a RECONFIGURE BURST consisting of eight marks and one space repeated 765 times. The purpose of this burst is to terminate all activity on the network. Since this burst is longer than any other type of transmission, the burst will interfere with the next INVITATION TO TRANSMIT, destroy the token and keep any other node from assuming control of the line. It also provides line activity which allows the COM 9026 sending the INVITATION TO TRANSMIT to release control of the line.

When any COM 9026 sees an idle line for greater than 78.2 microseconds, which will only occur when the token is lost, each COM 9026 starts an internal time out equal to 146 microseconds times the quantity 255 minus its own ID. It also sets the internally stored NID (next ID representing the next possible ID node) equal to its own ID. If the timeout expires with no line activity, the COM 9026 starts sending INVITATIONS TO TRANSMIT with the DID equal to the currently stored NID. Within a given network, only one COM 9026 will timeout (the one with the highest ID number). After sending the INVITATION TO TRANSMIT, the COM 9026 waits for activity on the line. If there is no activity for 74.7 microseconds, the COM 9026 increments the NID value and transmits another INVITATION TO TRANSMIT using the new NID equal to the DID. If activity appears before the 74.7 microsecond timeout expires, the COM 9026 releases control of the line. During NETWORK RECONFIGURATION, INVITATIONS TO TRANSMIT will be sent to all 256 possible ID's. Each COM 9026 on the network will finally have saved a NID value equal to the ID of the COM 9026 that assumed control from it. From then until the next NETWORK RECONFIGURATION, control is passed directly from one node to the next with no wasted INVITATIONS TO TRANSMIT sent to ID's not on the network. When a node is powered off, the previous node will attempt to pass it the token by issuing an INVITATION TO TRANSMIT. Since this node will not respond, the previous node will time out and transmit another INVITATION TO TRANSMIT to an incremented ID and eventually a response will be received.

The time required to do a NETWORK RECONFIGURATION depends on the number of nodes in the network, the propogation delay between nodes and the highest ID number on network but will be in the range of 24 to 61 milliseconds.

BROADCAST MESSAGES

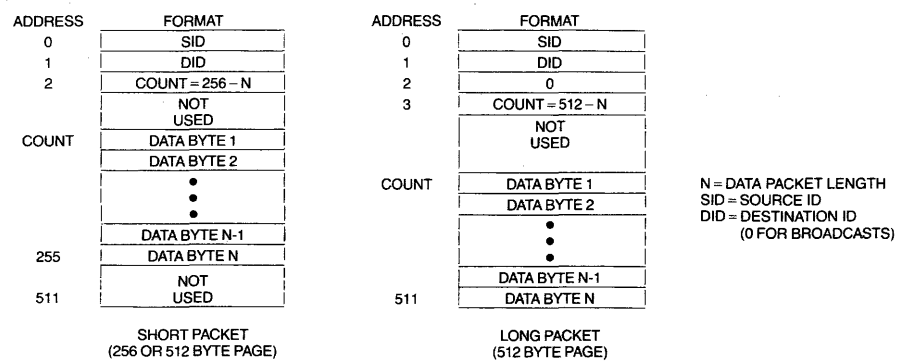
Broadcasting gives a particular node the ability to transmit a data packet to all nodes on the network simultaneously. ID zero is reserved for this feature and no node on the network can be assigned ID zero. To broadcast a message, the transmitting node's processor simply loads the RAM buffer with the data packet and sets the destination ID (DID) equal to zero. Figure 8 illustrates the position of each byte in the packet with the DID residing at address 01 HEX of the current page selected in the TRANSMIT command. Each individual node has the ability to ignore broadcast messages by setting the most signficant bit of the ENABLE RECEIVE TO PAGE nn command (see "WRITE COM 9026 COMMANDS") to a logic zero.

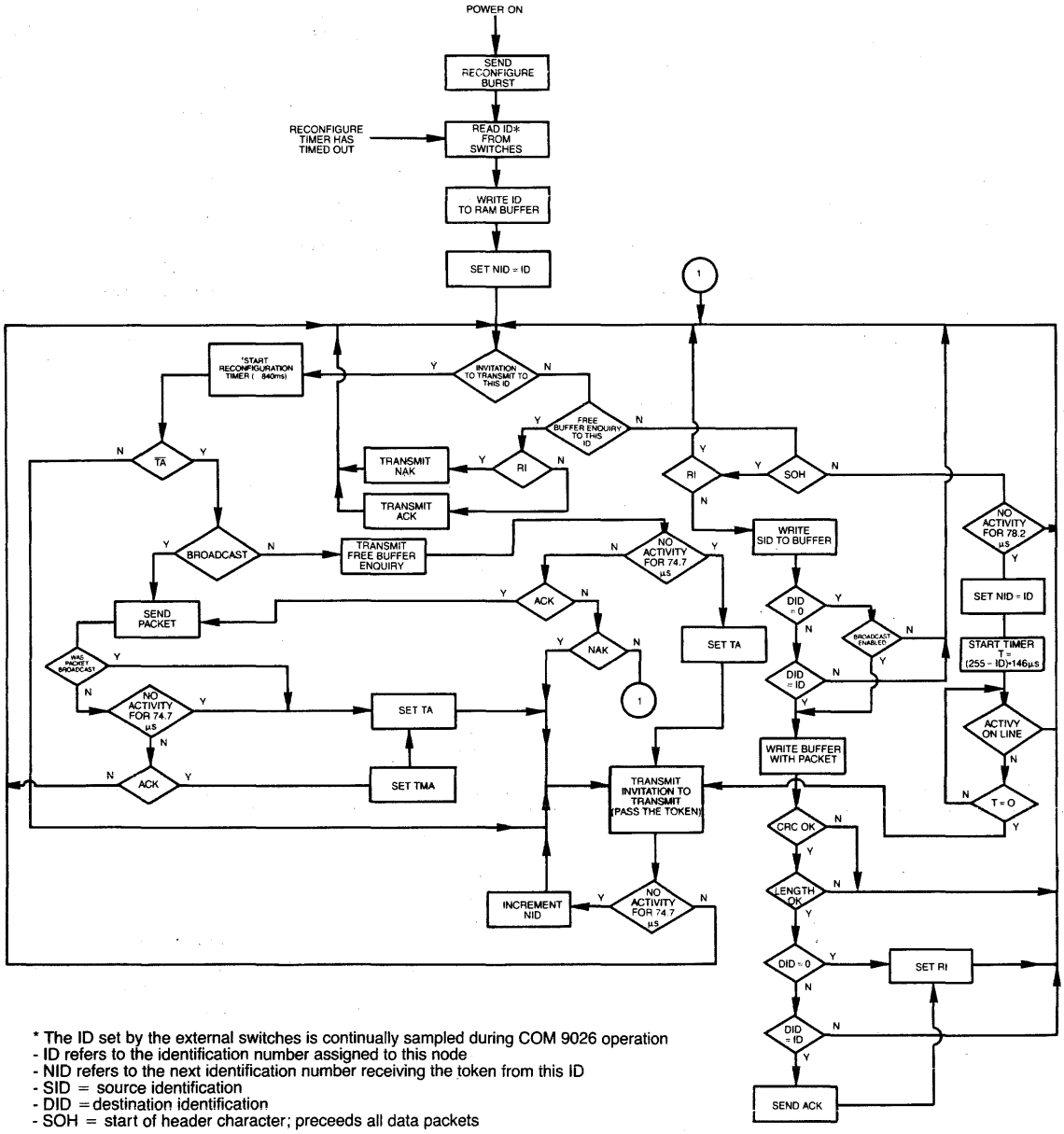
COM 9026 OPERATION

BUFFER CONFIGURATION

During a transmit sequence, the COM 9026 fetches data from the Transmit Buffer, a 256 (or 512) byte segment of the RAM buffer. The appropriate buffer size is specified in the DEFINE CONFIGURATION command. When long packets are enabled, the COM 9026 will interpret the packet as a long or short packet depending on whether the contents of buffer location 02 is zero or non zero. During a receive sequence, the COM 9026 stores data in the receive buffer, also a 256 (or 512) byte segment of the RAM buffer. The processor I/O command which enables either the COM 9026 receiver or the COM 9026 transmitter also initializes the respective buffer page register. The formats of the buffers (both 256 and 512 byte) are shown below.

FIGURE 8— RAM BUFFER PACKET CONFIGURATION





* The ID set by the external switches is continually sampled during COM 9026 operation
- ID refers to the identification number assigned to this node
- NID refers to the next identification number receiving the token from this ID
- SID = source identification
- DID = destination identification
- SOH = start of header character; preceeds all data packets

FIGURE 3—9026 OPERATION

PROCESSOR INTERFACE

Figure 2 illustrates a typical COM 9026 to processor interface. The signals on the left side of this figure represent typical processor signals with a 16 bit address bus and an 8 bit data bus with the data bus multiplexed onto the lower 8 address lines (PAD7-PAD0). The processor sees a network node (a node consists of a COM 9026, RAM buffer, cable transceiver, etc. as shown in figure 2) as 2K memory locations and 4 I/O locations within the COM 9026.

The RAM buffer is used to hold data packets temporarily prior to transmission on the network and as temporary storage of all received data packets directed to the particular node. The size of the buffer can be as large as 2K byte locations providing four pages at a maximum of 512 bytes per page. For packet lengths smaller than 256 bytes, a 1K RAM buffer can be used to provide four pages of storage. In this case address line IA8 (sourced from either the COM 9026 or the processor) should be left unconnected. Since four pages of RAM buffer are provided, both transmit and receive operations can be double buffered with respect to the processor. For instance, after one data packet has been loaded into a particular page within the RAM buffer and a transmit command for that page has been issued, the processor can start loading another page with the next message in a multimessage transmission sequence. Similarly, after one message is received and completely loaded into one page of the RAM buffer by the COM 9026, another receive command can be issued to allow reception of the next packet while the first packet is read by the processor. In general, the four pages in the RAM buffer can be used for transmit or receive in any combination. In addition, the processor will also use the interface bus (IA10-IA8, IAD7-IAD0) when performing I/O access cycles (status reads from the COM 9026 or command writes to the COM 9026).

To accomplish this double buffering scheme, the RAM buffer must behave as a dual port memory. To allow this RAM to be a standard component, arbitration and control on the interface bus (IA10-IA8, IAD7-IAD0) is required to permit both the COM 9026 and the processor access to the RAM buffer and, at the same time, permit all processor I/O operations to or from the COM 9026.

Processor access cycle requests begin on the trailing edge of AS if either $\overline{\text{IOREQ}}$ or $\overline{\text{MREQ}}$ is asserted. These access cycles run completely asynchronous with respect to the COM 9026. Because of this, upon processor access cycle requests, the COM 9026 immediately puts the processor into a wait state by asserting the WAIT output. This gives the COM 9026 the ability to synchronize and control the processor access cycle. When the processor access cycle is synchronized by the COM 9026, the WAIT signal is eventually removed allowing the processor to complete its cycle.

For processor RAM buffer access cycles, $\overline{\text{AIE}}$ and $\overline{\text{ADIE}}$ enable the processor address captured during AS time onto the interface address bus (IA10-IA8, IAD7-IAD0). The signal $\overline{\text{L}}$ will capture the 8 least significant bits of this address (appearing on IAD7-IAD0) before the data is multiplexed onto it. At the falling edge of L, a stable address is presented to the RAM buffer. For read cycles, $\overline{\text{OE}}$ allows the addressed RAM buffer data to source the interface address/data bus (IAD7-IAD0). In figure 2, this information is passed into a transparent latch gated with WAIT. At the falling edge of WAIT, the data accessed by the processor is captured

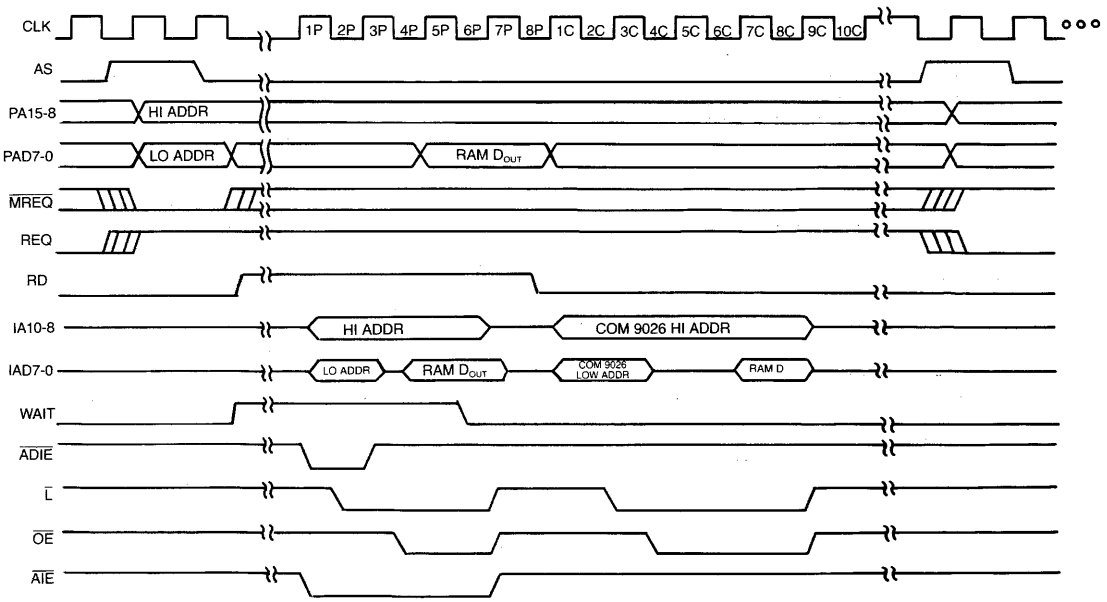


FIGURE 4—PROCESSOR READ RAM FOLLOWED BY COM 9026 READ RAM

and driven out via the logic function RD anded with REQ. For processor I/O read cycles from the COM 9026, ADIE and AIE are used to enable the processor address into the COM 9026. Data out of the COM 9026 is gated through the transparent latch and appears on the processor's data bus with the same control signals used for RAM read cycles.

For processor write cycles, after the falling edge of L, the COM 9026 produces a WE (write enable) output to the RAM buffer, and the ILE output from the COM 9026 allows the processor data to source the interface address/data bus (IAD7-IAD0). At this time the COM 9026 waits for DWR before concluding the cycle by removing the WAIT output. DWR should only be used if the processor cannot deliver the data to be written in enough time to satisfy the write setup time requirements of the RAM buffer. By delaying the activation of DWR, the period of the write cycle will be extended until the write data is valid. Since the architecture and operation of the COM 9026 requires periodic reading and writing of the RAM buffer in a timely manner, holding the DWR input off for a long period of time, or likewise by running the processor at a slow speed, can result in a data overflow condition. It is therefore recommended that if the processor write data setup time to the RAM buffer is met, then the DWR input should be grounded.

For processor I/O write cycles to the COM 9026, ADIE and AIE are used to enable the processor's address onto the interface data bus. ILE is used to enable the processor's write data into the COM 9026. Delaying the activation of DWR will hold up the COM 9026 cycle requiring the same precautions as stated for Processor RAM Write cycles.

As stated previously, processor requests occur at the falling edge of AS if either IOREQ or MREQ are active. COM 9026 requests occur when the transmitter or receiver need to read or write the RAM buffer in the course of executing the command. If the COM 9026 requests a bus cycle at the same time as the processor, or shortly after the processor, the COM 9026 cycle will follow immediately after the processor cycle. Figure 4 illustrates the timing relationship of a Processor RAM Read cycle followed by a COM 9026 RAM read cycle. Once the AS signal captures the processor address to the RAM buffer and requests a bus cycle, it takes 4 CLK periods for the processor cycle to end. Figure 4 breaks up these 4 CLK periods into 8 half clock interval labeled 1P through 8P. A COM 9026 access cycle will take 5 CLK periods to end. Figure 4 breaks up these 5 CLK periods into 10 half intervals labeled 1C through 10C.

If a processor cycle request occurs after a COM 9026 request has already been granted, the COM 9026 cycle will occur first, as shown in figure 5. Figure 5 illustrates the timing relationship of a COM 9026 RAM Write cycle followed by a Processor RAM Write cycle. Due to the asynchronous nature of the bus requests (AS and CLK), the transition from the end of the COM 9026 cycle to the beginning of the processor cycle might have some dead time. Refering to figure 5, if AS falling edge occurs after the start of half CLK interval 9C, no real contention exists and it will take between 200 and 500 nanoseconds before the processor cycle can start. The start of the processor cycle is defined as the time when the COM 9026 produces a leading edge on both ADIE and AIE. If the processor request occurs before the end of half

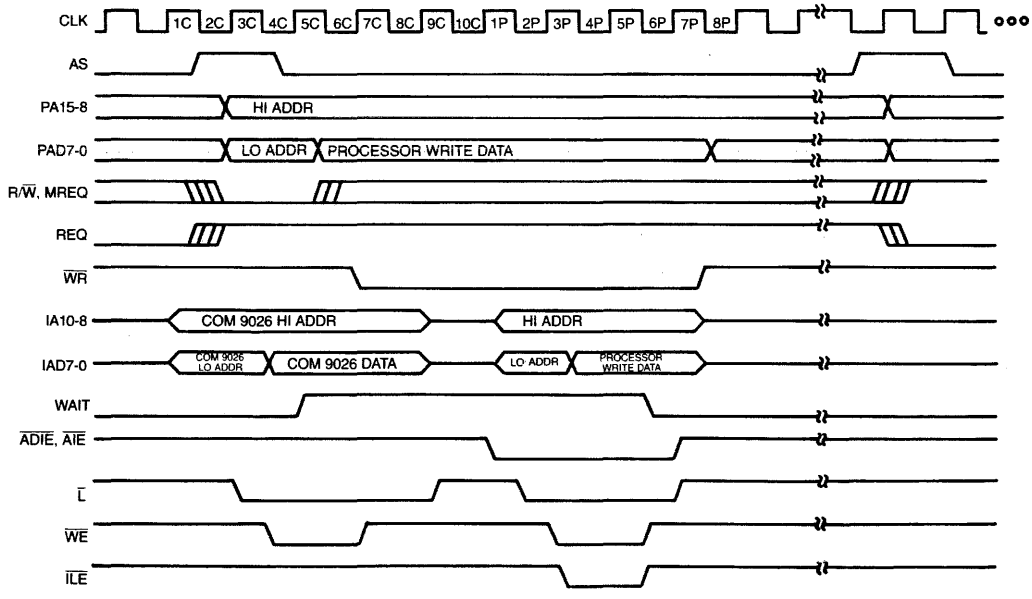


FIGURE 5—COM 9026 WRITE RAM FOLLOWED BY PROCESSOR WRITE RAM

CLK interval 5C (figure 5 illustrates this situation), then the processor cycle will always start at half CLK interval 1P. The uncertainty is introduced when the processor request occurs during half CLK intervals 6C, 7C or 8C. In this case, the processor cycle will start between 200 and 500 nanoseconds later depending on the particular timing relation between AS and CLK. The maximum time between processor request and processor cycle start, which occurs when the processor request comes just after a COM 9026 request, is 1300 nanoseconds. It should be noted that all times specified above assume a nominal CLK period of 200 nanoseconds.

Figures 6 and 7 illustrate timing for Processor Read COM 9026 and Processor Write COM 9026 respectively. These cycles are also shown divided into 8 half clock intervals (1P through 8P) and can be inserted within figures 4 and 5 if these processor cycles occur.

POWER UP AND INITIALIZATION

The COM has the following power up requirements:

1—The $\overline{\text{POR}}$ input must be active for at least 100 milliseconds.
2—The CLK input must run for at least 10 clock cycles before the $\overline{\text{POR}}$ input is removed.
3—While $\overline{\text{POR}}$ is asserted, the CA input may be running or held high. If the CA input is running, $\overline{\text{POR}}$ may be released asynchronously with respect to CA. If the CA input is held high, $\overline{\text{POR}}$ may be released before CA begins running.

During $\overline{\text{POR}}$ the status register will assume the following state:

BIT 7 (RI) set to a logic "1".
BIT 6 (ETS2) not affected
BIT 5 (ETS1) not affected
BIT 4 (POR) set to a logic "1".
BIT 3 (TEST) set to a logic "0".
BIT 2 (RECON) set to a logic "0".
BIT 1 (TMA) set to a logic "0".
BIT 0 (TA) set to a logic "1".

In addition the $\overline{\text{DSYNC}}$ output is reset inactive high and the interrupt mask register is reset (no maskable interrupts enabled). Page 00 is selected for both the receive and the transmit RAM buffer. After the $\overline{\text{POR}}$ signal is removed, the COM 9026 will generate an interrupt from the nonmaskable Power On Reset interrupt. The COM 9026 will start operation four CA clock cycles after the $\overline{\text{POR}}$ signal is removed. At this time, the COM 9026, after reading its ID from the external shift register, will execute two write cycles to the RAM buffer. Address 00 HEX will be written with the data D1 HEX and address 01 HEX will be written with the ID number as previously read from the external shift register. The processor may then read RAM buffer address 01 to determine the COM 9026 ID. It should be noted that the data pattern D1 written into the RAM has been chosen arbitrarily. Only if the D1 pattern appears in the RAM buffer can proper operation be assured.

CLOCK GENERATOR

The COM 9026 uses two separate clock inputs namely CA and CLK. The CLK input is a 5 MHz free running clock and the CA input is a start/stop clock periodically stopped and started to allow the COM 9026 to synchronize to the incoming data that appears on the RX input.

Figure 9 illustrates the timing of the CA clock generator and its relationship to the $\overline{\text{DSYNC}}$ output and the RX input. The $\overline{\text{DSYNC}}$ output is used to control the stopping of the CA clock. On the next rising edge of the CA input after $\overline{\text{DSYNC}}$ is asserted, CA will remain in the high state. The CA clock remains halted in the high state as long as the RX signal remains high. When the RX signal goes low, the CA clock is restarted and remains running until the next falling edge of $\overline{\text{DSYNC}}$. (See figure 20 for an implementation of this circuit.)

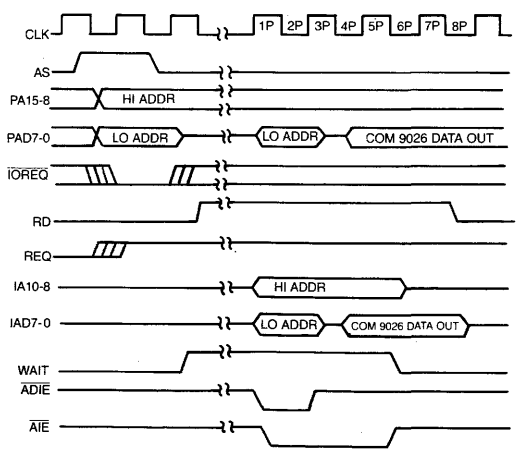


FIGURE 6—PROCESSOR READ COM 9026

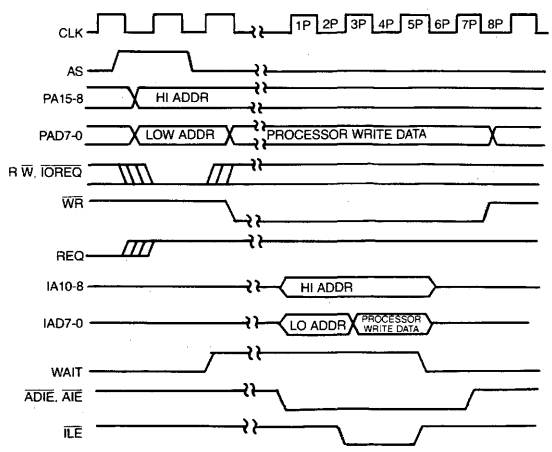


FIGURE 7—PROCESSOR WRITE COM 9026

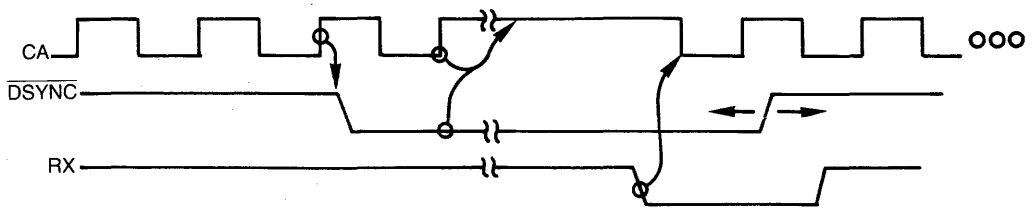


FIGURE 9—CA CLOCK GENERATOR TIMING

EXTENDED TIMEOUT FUNCTION

There are three timeouts associated with the COM 9026 operation.

Response Time

This timeout is equal to the round trip propagation delay between the 2 furthest nodes on the network plus the maximum turn around time (the time it takes a particular COM 9026 to start sending a message in response to a received message) which is known to be 12 microseconds. The round trip propagation delay is a function of the transmission media and network topology. For a typical system using RG62 coax in a baseband system, a one way cable propagation delay of 31 microseconds translates to a distance of about 4 miles. The flow chart in figure 3 uses a value of 74.7 microseconds (31 + 31 + 12 + margin) to determine if any node will respond.

Idle Time

This time is associated with a NETWORK RECONFIGURATION. Refering to figure 3, during a NETWORK RECONFIGURATION one node will continually transmit INVITATIONS TO TRANSMIT until it encounters an active node. Every other node on the network must distinguish between this operation and an entirely idle line. During NETWORK RECONFIGURATION, activity will appear on the line every 78 microseconds. This 78 microsecond is equal to the response time of 74.7 microseconds plus the time it takes the COM 9026 to retransmit another message (usually another INVITATION TO TRANSMIT). The actual timeout is set to 78.2 microseconds to allow for margin.

Reconfiguration Time

If any node does not receive the token within this time, the node will initiate a NETWORK RECONFIGURATION

The ET2 and ET1 inputs allow the network to operate over longer distances than the 4 miles stated earlier. DC levels on these inputs control the maximum distances over which the COM 9026 can operate by controlling the 3 timeout values described above. Table 1 illustrates the response time and reconfiguration time as a function of the ET2 and ET1 inputs. The idle time will always be equal to the response time plus 3.5 microseconds. It should be noted that for proper network operation, all COM 9026's connected to the same network must have the same response time, idle time and reconfiguration time.

ET2	ET1	RESPONSE TIME (μs)	RECONFIGURATION TIME (ms)
1	1	74.7	840
1	0	283.4	1680
0	1	561.8	1680
0	0	1118.6	1680

TABLE 1
COM 9026 INTERNAL PROGRAMMABLE TIMER VALUES

I/O COMMANDS

I/O commands are executed by activating the $\overline{\text{IOREQ}}$ input. The COM 9026 will interrogate the AD0 and the R/$\overline{\text{W}}$ inputs at the AS time to execute commands according to the following table:

$\overline{\text{IOREQ}}$	AD0	R/$\overline{\text{W}}$	FUNCTION
low	low	low	write interrupt mask
low	low	high	read status register
low	high	low	write COM 9026 command
low	high	high	reserved for future use

READ STATUS REGISTER

Execution of this command places the contents of the status register on the data bus (AD7-AD0) during the read portion of the processor's read cycle. The COM 9026 status register contents are defined as follows:

BIT 7—Receiver inhibited (RI)—This bit, if set high, indicates that a packet has been deposited into the RAM buffer page nn as specified by the last ENABLE RECEIVE TO PAGE nn command. The setting of this bit can cause an interrupt via INTR if enabled during a WRITE INTERRUPT MASK command. No messages will be received until an ENABLE RECEIVE TO PAGE nn command is issued. After any message is received, the receiver is automatically inhibited by setting this bit to a logic one.

BIT 6—Extended Timeout Status 2 (ETS2)—This bit reflects the current logic value tied to the ET2 input pin (pin 1).

BIT 5—Extended Timeout Status 1 (ETS1)—This bit reflects the current logic value tied to the ET1 input pin (pin 3).

BIT 4—Power On Reset (POR)—This bit, if set high, indicates that the COM 9026 has received an active signal on the POR input (pin 40). The setting of this bit will cause a nonmaskable interrupt via INTR.

BIT 3—Test (TEST)—This bit is intended for test and diagnostic purposes. It will be a logic zero under any normal operating conditions.

BIT 2—Reconfiguration (RECON)—This bit, if set high, indicates that the reconfiguration timer has timed out because the RX input was idle for 78.2 microseconds. The setting of this bit can cause an interrupt via INTR if enabled by the WRITE INTERRUPT MASK command. The bit is reset low during a CLEAR FLAGS command.

BIT 1—Transmit Message Acknowledged (TMA)—This bit, if set high, indicates that the packet transmitted as a result of an ENABLE TRANSMIT FROM PAGE nn command has been positively acknowledged. This bit should only be considered valid after the TA bit (bit 0) is set. Broadcast mesages are never acknowledged.

BIT 0—Transmitter Available (TA)—This bit, if set high, indicates that the transmitter is available for transmitting. This bit is set at the conclusion of a ENABLE TRANSMIT FROM PAGE nn command or upon the execution of a DISABLE TRANSMITTER command. The setting of this bit can cause an interrupt via INTR if enabled by the WRITE INTERRUPT MASK command.

WRITE INTERRUPT MASK

The COM 9026 is capable of generating an interrupt signal when certain status bits become true. A write to the MASK register specifies which status bits can generate the interrupt. The bit positions in the MASK register are in the same position as their corresponding status bits in the STATUS register with a logic one in a bit position enabling the corresponding interrupt. The setting of the TMA, EST1, and EST2 status bits will never cause an interrupt. The POR status bit will cause a non-maskable interrupt regardless of the value of the corresponding MASK register bit. The MASK register takes on the following bit definition:

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RECEIVE INHIBIT	XXX	XXX	XXX	XXX	RECON TIMER	XXX	TRANSMITTER AVAILABLE

The three maskable status bits are anded with their respective mask bits, and the results, along with the POR status bit, are or'ed to produce the processor interrupt signal INTR. This signal returns to its inactive low state when the interrupting status bit is reset to a logic "0" or when the corresponding bit in the MASK register is reset to a logic "0". To clear an interrupt generated as a result of a Power On Reset or Reconfiguration occurance, the CLEAR FLAGS command should be used. To clear an interrupt generated as a result of a completed transmission (TA) or a completed reception (RI), the corresponding masks bits should be reset to a logic zero.

WRITE COM 9026 COMMANDS

Execution of the following commands are initiated by performing a processor I/O write with the written data defining the following commands:

WRITTEN DATA	COMMAND
00000000	reserved for future use
00000001	DISABLE TRANSMITTER—This command will cancel any pending transmit command (transmission has not yet started) when the COM 9026 next receives the token. This command will set the TA (Transmitter Available) status bit when the token is received.
00000010	DISABLE RECEIVER—This command will cancel any pending receive command. If the COM 9026 is not yet receiving a packet, the RI (Receiver Inhibited) bit will be set the next time the token is received. If packet reception is already underway, reception will run to its normal conclusion.
000nn011	ENABLE TRANSMIT FROM PAGE nn—This command prepares the COM 9026 to begin a transmit sequence from RAM buffer page nn the next time it receives the token. When this command is loaded, the TA and TMA bits are set to a logic "0". The TA bit is set to a logic one upon completion of the transmit sequence. The TMA bit will have been set by this time if the COM 9026 has received an acknowledgement from the destination COM 9026. This acknowledgement is strictly hardware level which is sent by the receiving COM 9026 before its controlling processor is even aware of message reception. It is also possible for this acknowledgement to get lost due to line errors, etc. This implies that the TMA bit is not a guarantee of proper destination reception. Refer to figure 3 for details of the transmit sequence and its relation to the TA and TMA status bits.
b00nn100	ENABLE RECEIVE TO PAGE nn—This command allows the COM 9026 to receive data packets into RAM buffer page nn and sets the RI status bit to a logic zero. If "b" is a logic "1", the COM 9026 will also receive broadcast transmissions. A broadcast transmission is a transmission to ID zero. The RI status bit is set to a logic one upon successful reception of a message.
0000c101	DEFINE CONFIGURATION—If c is a logic "1", the COM 9026 will handle short as well as long packets. If c is a logic "0", the COM 9026 will only handle short packets (less than 254 bytes).
000rp110	CLEAR FLAGS—If p is a logic "1" the POR status flag is cleared. If r is a logic "1", the RECON status flag is cleared.

All other combinations of written data are not permitted and can result in incorrect chip and/or network operation.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0 to 70°C
Storage Temperature Range	−55 to 150°C
Lead Temperature (soldering, 10 seconds)	+325°C
Positive Voltage on any pin	+8V
Negative Voltage on any pin, with respect to ground	−0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $70°C$, $V_{CC} = 5.0V \pm 5\%$)

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
V_{IL}	input low voltage	−0.3		0.8	V	
V_{IH1}	input high voltage 1	2.2		V_{CC}	V	except CA and CLK
V_{IH2}	input high voltage 2	V_{CC}−0.5		6.5	V	for CA or CLK
V_{OL1}	output low voltage 1			0.4	V	$I_{OL} = 1.6$ ma
V_{OL2}	output low voltage 2			0.5	V	$I_{OL} = 2.0$ ma
V_{OH}	output high voltage (1)	2.4			V	
I_L	input leakage current			±10	μA	
C_{IN}	input capacitance			20	pf	
C_{DB}	data bus capacitance			50	pf	
C_L	all other capacitance			30	pf	
I_{CC}	power supply current			350	ma	

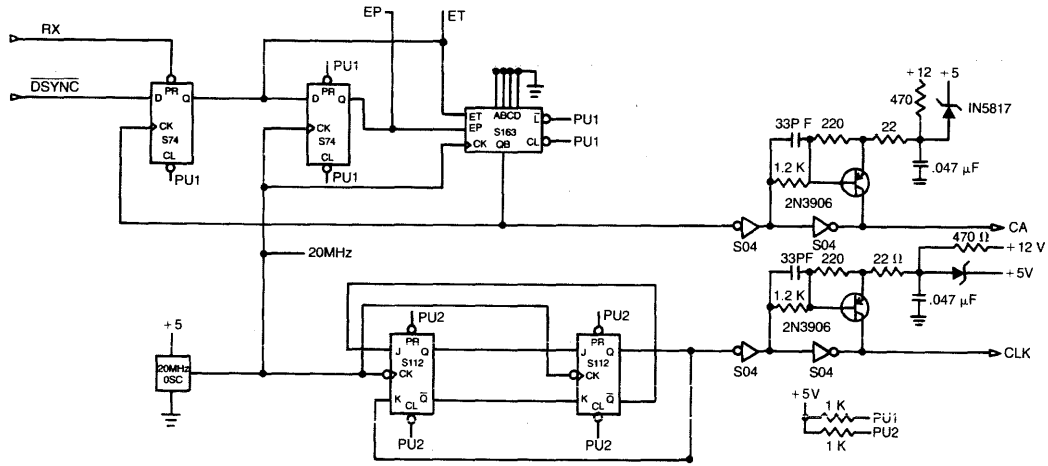


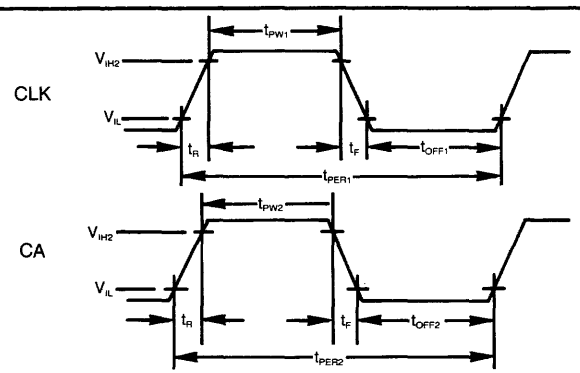
FIGURE 20—TYPICAL CLOCK GENERATOR CIRCUITRY

AC ELECTRICAL CHARACTERISTICS ($T_A = 0°$ to 70°C, $V_{CC} = 5.0V \pm 5\%$)

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
t_{PW1}	CLK pulse width	65			ns	
t_{PER1}	CLK period	190	200	600	ns	
t_{OFF1}	CLK off time	65			ns	
t_{PW2}	CA pulse width	60			ns	
t_{PER2}	CA period	190			ns	
t_{OFF2}	CA off time	60	100	300	ns	
t_R	CLK, CA rise time			20	ns	
t_F	CLK, CA fall time			20	ns	
t_1	width of addr. strobe	50			ns	
t_2	REQ output delay	0		100	ns	
t_3	WAIT assertion delay	0		200	ns	
t_4	delay to rising edge of processor cycle	t_P		$2t_P + 100$	ns	$t_P = t_{PER1}$
t_5	data hold into COM 9026	80			ns	
t_6	setup COM 9026 data out	60			ns	
t_7	$\overline{WE}$ delay from CLK	0		100	ns	
t_8	$\overline{TX}$ on delay from CA falling edge	10		150	ns	
t_9	$\overline{TX}$ off delay from CA rising edge	10		150	ns	
t_{10}	AS period	7/2 t_P			ns	$t_P = t_{PER2}$
t_{11}	$\overline{DSYNC}$ delay from CA rising edge	10		150	ns	
t_{12}	delay to wait off	20		100	ns	
t_{13}	$\overline{DWR}$ setup time	50			ns	
t_{14}	$\overline{ILE}$ delay from CLK	10		100	ns	
t_{15}	processor addr. setup from $\overline{ADIE}$,			50	ns	
t_{16}	processor command setup time	125			ns	
t_{17}	addr. enable setup time to $\overline{L}$	50			ns	
t_{18}	addr. hold time from $\overline{L}$	50			ns	
t_{19}	strobe and data hold for read	20			ns	
t_{20}	AD bus HI impedance to $\overline{OE}$s	0			ns	
t_{21}	delay of $\overline{IDLD}$ from CLK rising edge	0		120	ns	
t_{22}	delay of IDDAT from CLK rising edge	0		50	ns	
t_{23}	off delay from CLK rising edge	0		100	ns	
t_{24}	addr. to RAM data valid			300	ns	
t_{25}	$\overline{OE}$ setup to WAIT falling edge	140			ns	
t_{26}	strobe & data hold for write	50			ns	
t_{27}	addr. enable setup to WAIT	300			ns	
t_{28}	$\overline{ADIE}$ to $\overline{OE}$ delay	40			ns	
t_{29}	COM 9026 write data hold time	80			ns	
t_{30}	$\overline{OE}$ to RAM data valid	0		140	ns	
t_{31}	status setup to AS falling edge	50			ns	
t_{32}	status hold from AS falling edge	50			ns	
t_{33}	RX setup to CA rising edge	80			ns	
t_{34}	RX hold time from CA rising edge	30			ns	
t_{35}	$\overline{POR}$ active time	100			ms	after V_{cc} has been stable for time t_{35}, the minimum $\overline{POR}$ active time is 10 cycles of CLK.

The above timing information is valid for a worst case 40% to 60% duty cycle on CLK. All times are measured from the 50% point of the signals.

FIGURE 10— CLK, CA AC CHARACTERISTICS



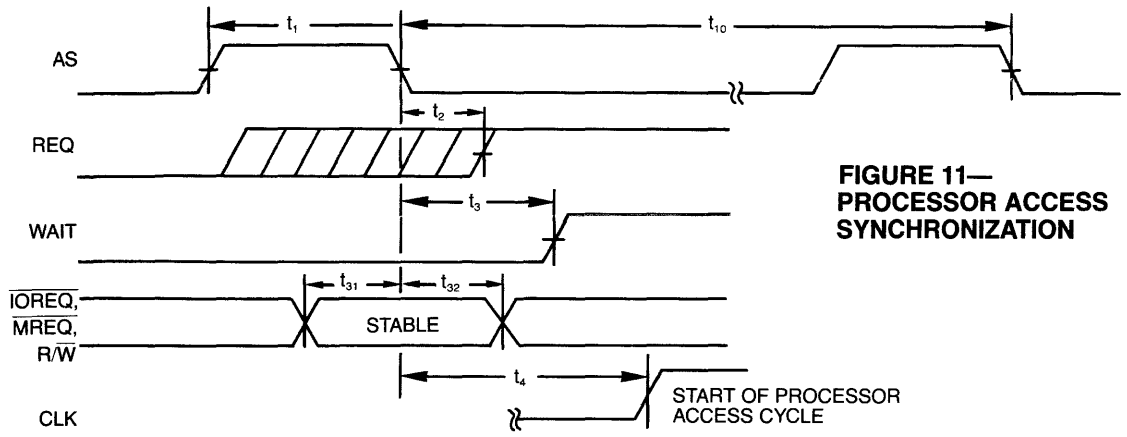


FIGURE 11—PROCESSOR ACCESS SYNCHRONIZATION

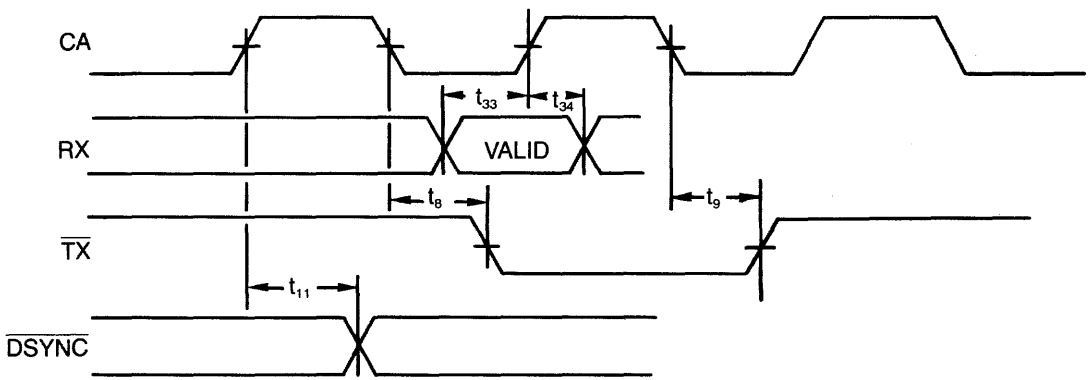


FIGURE 12—TRANSMIT AND RECEIVE TIMING

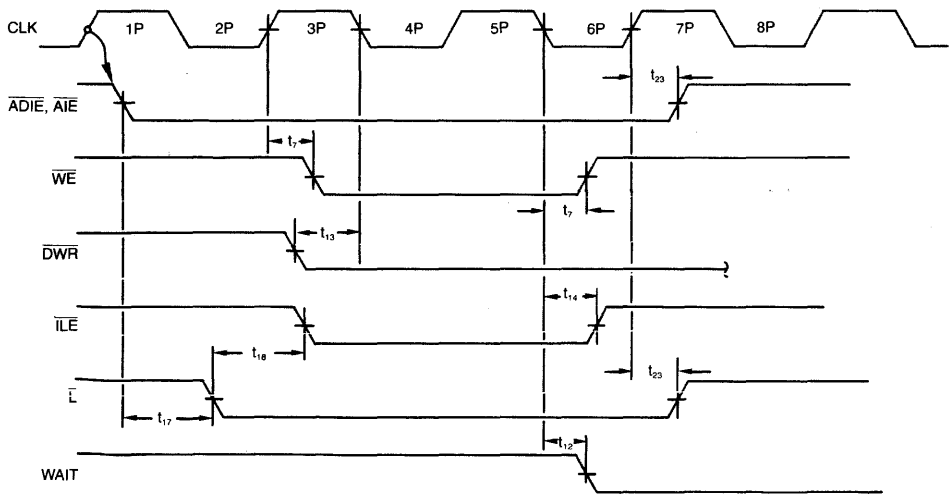


FIGURE 13—PROCESSOR WRITE RAM AC TIMING

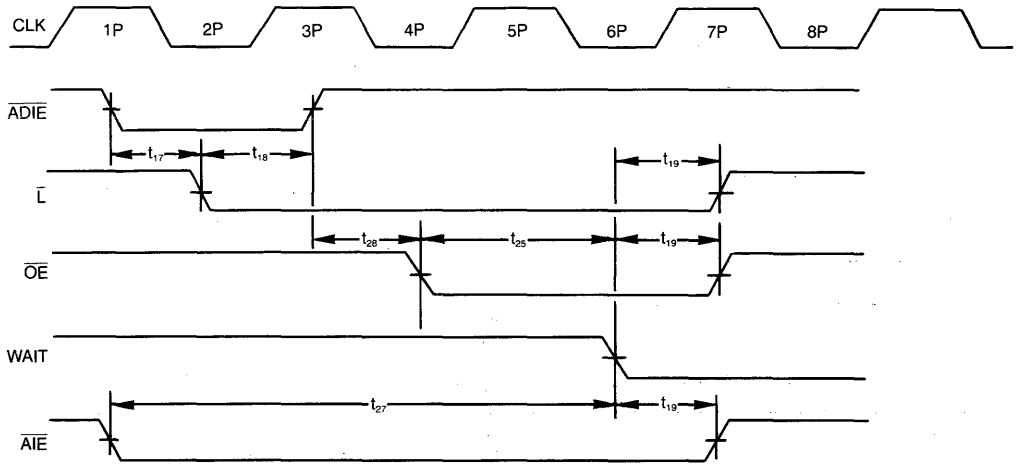


FIGURE 14—PROCESSOR READ RAM AC TIMING

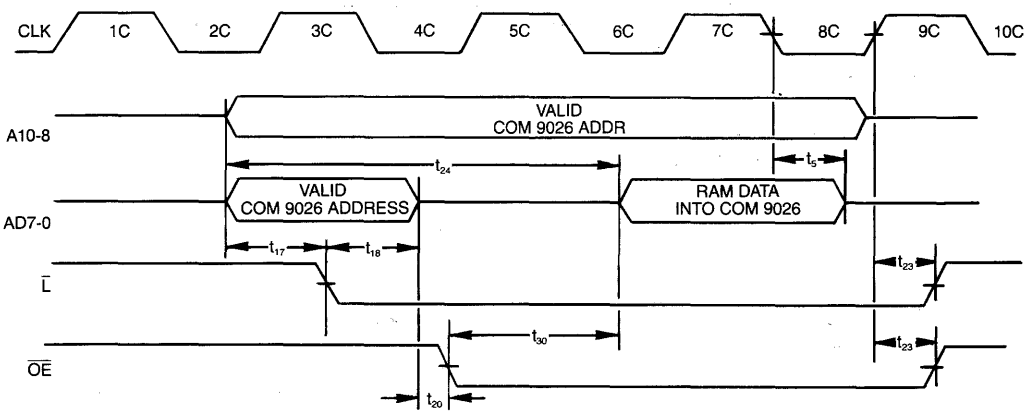


FIGURE 15—COM 9026 READ RAM AC TIMING

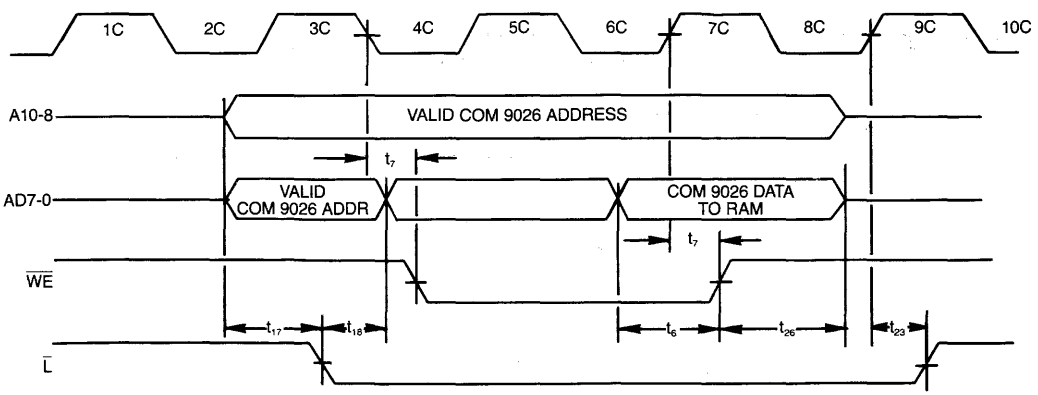


FIGURE 16—COM 9026 WRITE RAM AC TIMING

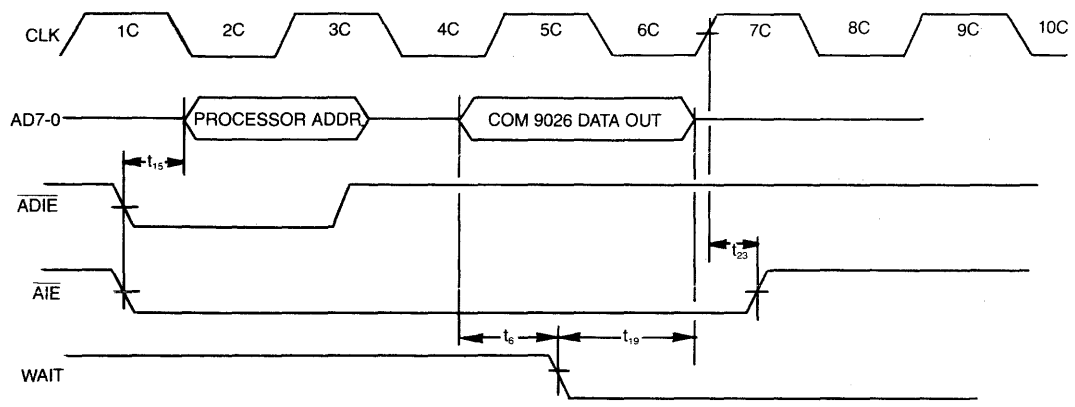


FIGURE 17—PROCESSOR READ COM 9026 AC TIMING

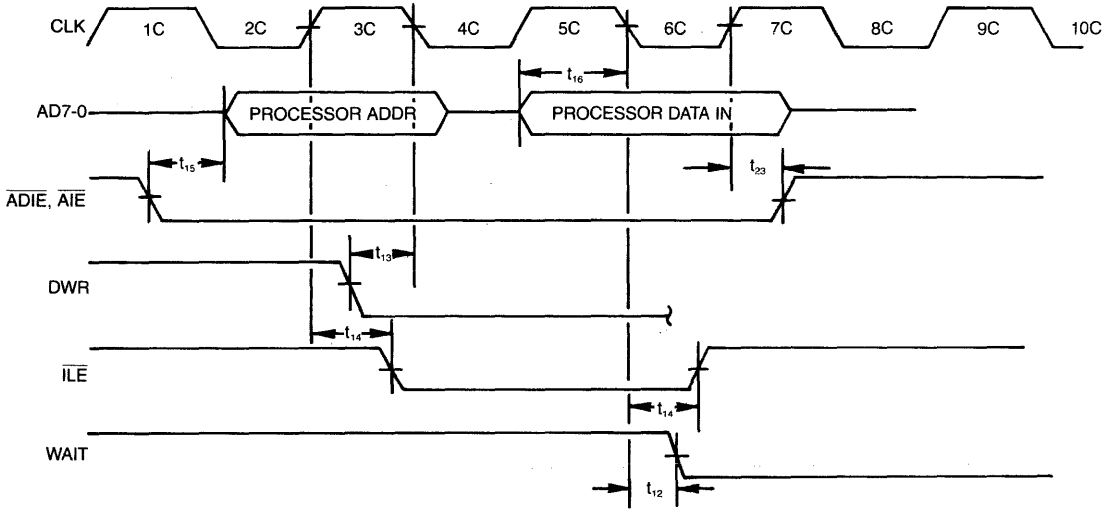


FIGURE 18—PROCESSOR WRITE COM 9026 AC TIMING

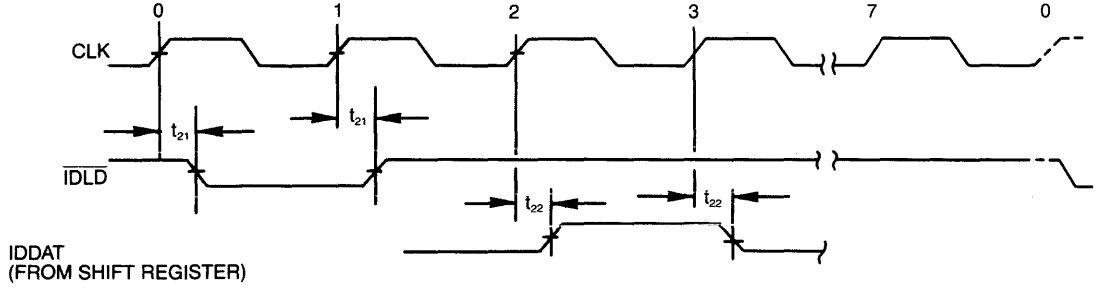


FIGURE 19—ID INPUT AC TIMING

Baud Rate Generator

All Baud Rate Generators are programmable dividers capable of providing 16 output frequencies* for UARTs or USARTs from either an on-chip crystal oscillator or an external frequency input. "T" versions utilize an external frequency input only. Dual Baud Rate Generators provide two output frequencies simultaneously for full duplex communications.

Baud Rate Generators providing all standard baud rates from various popular crystal frequencies are available. In addition the baud rate generator may be custom mask programmed for other divisors.

*except as noted

Part Number	Description	Features	Power Supplies	Package	Page
COM 5016	Dual Baud Rate Generator	On-chip oscillator or external frequency input	+5, +12	18 DIP	209-210
COM 5016T(1)	Dual Baud Rate Generator	External frequency input	+5, +12	18 DIP	209-210
COM 5026	Single Baud Rate Generator	On-chip oscillator or external frequency input	+5, +12	14 DIP	211-212
COM 5026T(1)	Single Baud Rate Generator	External frequency input	+5, +12	14 DIP	211-212
COM 5036	Dual Baud Rate Generator	COM 5016 with additional output of input frequency ÷ 4	+5, +12	18 DIP	213-214
COM 5036T(1)	Dual Baud Rate Generator	COM 5016T with additional output of input frequency ÷ 4	+5, +12	18 DIP	213-214
COM 5046	Single Baud Rate Generator	COM 5026 with additional output of input frequency ÷ 4	+5, +12	14 DIP	215-220
COM 5046T(1)	Single Baud Rate Generator	COM 5026T with additional output of input frequency ÷ 4	+5, +12	14 DIP	215-220
COM 8046	Single Baud Rate Generator	32 baud rates; 1X, 16X, 32X clock outputs; single +5 volt supply	+5	16 DIP	221-222
COM 8046T(1)	Single Baud Rate Generator	COM 8046 with external frequency input only	+5	16 DIP	221-222
COM 8116	Dual Baud Rate Generator	Single +5 volt version of COM 5016	+5	18 DIP	223-224
COM 8116T(1)	Dual Baud Rate Generator	Single +5 volt version of COM 5016T	+5	18 DIP	223-224
COM 8126	Single Baud Rate Generator	Single +5 volt version of COM 5026	+5	14 DIP	225-226
COM 8126T(1)	Single Baud Rate Generator	Single +5 volt version of COM 5026T	+5	14 DIP	225-226
COM 8136	Dual Baud Rate Generator	Single +5 volt version of COM 5036	+5	18 DIP	227-228
COM 8136T(1)	Dual Baud Rate Generator	Single +5 volt version of COM 5036T	+5	18 DIP	227-228
COM 8146	Single Baud Rate Generator	Single +5 volt version of COM 5046	+5	14 DIP	229-232
COM 8146T(1)	Single Baud Rate Generator	Single +5 volt version of COM 5046T	+5	14 DIP	229-232

(1)May be custom mask programmed

STANDARD MICROSYSTEMS CORPORATION

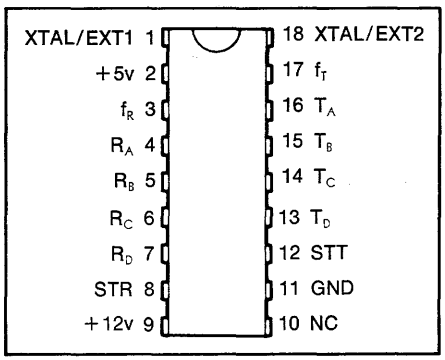
COM 5016
COM 5016T

Dual Baud Rate Generator
Programmable Divider

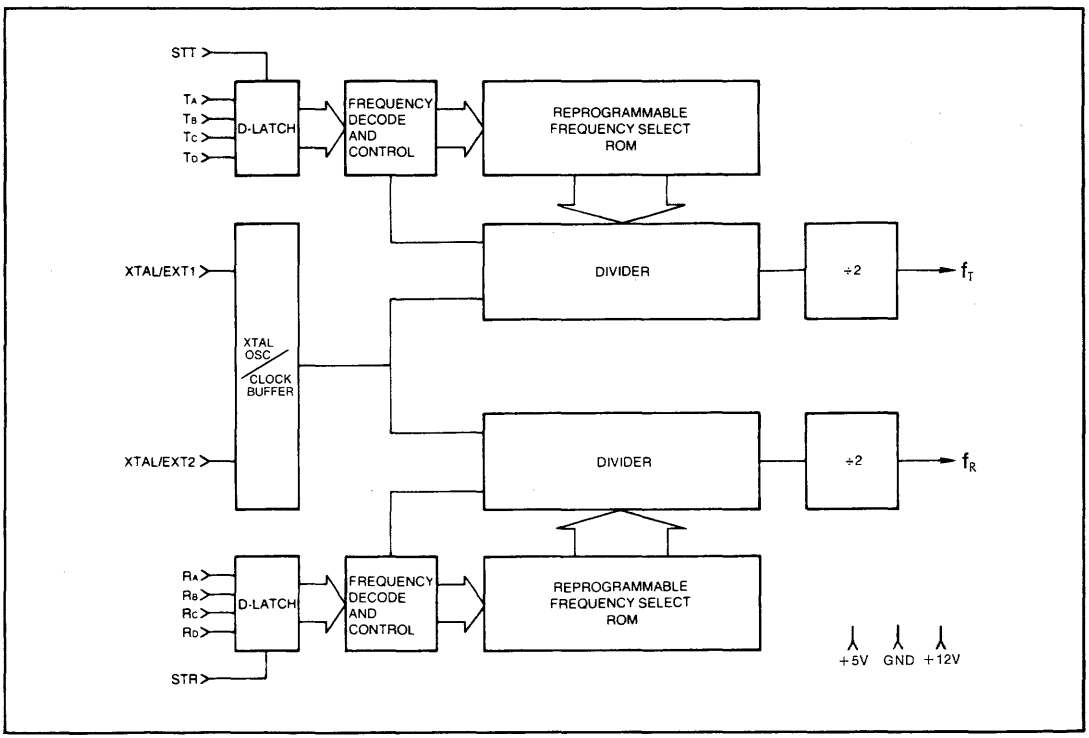
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Choice of 2 x 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Full duplex communication capability
- ☐ TTL, MOS compatibility

PIN CONFIGURATION



BLOCK DIAGRAM



General Description

The Standard Microsystems COM 5016 Dual Baud Rate Generator/Programmable Divider is an N-channel COPLAMOS® MOS/LSI device which, from a single crystal (on-chip oscillator) or input frequency is capable of generating 32 externally selectable frequencies.

The COM 5016 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies as shown in Table 1. One of the sixteen output frequencies is externally selected by four address inputs, on each of the independent dividers, as shown in Table 1.

Internal re-programmable ROM allows the generation of other frequencies from other crystal frequencies or input frequencies. The four address inputs on each divider section may be strobe (150ns) or DC loaded. As the COM 5016 is a dual baud rate generator, full duplex (independent receive and transmit frequencies) operation is possible.

The COM 5016 is basically a programmable 15-stage feedback shift register capable of dividing any modulo up to $(2^{15}-1)$.

By using one of the frequency outputs it is possible to generate additional divisions of the master clock frequency by cascading COM 5016's. The frequency output is fed into the XTAL/EXT input on a subsequent device. In this way one crystal or input frequency may be used to generate numerous output frequencies.

The COM 5016 can be driven by either an external crystal or TTL logic level inputs; COM 5016T is driven by TTL logic level inputs only.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+5 volt supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver divisor select data bits.
4-7	R_A, R_B, R_C, R_D	Receiver-Divisor Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver	A high level input strobe loads the receiver data (R_A, R_B, R_C, R_D) into the receiver divisor select register. This input may be strobed or hard-wired to a high level.
9	V_{DD}	Power Supply	+12 volt supply
10	NC	No Connection	
11	GND	Ground	Ground
12	STT	Strobe-Transmitter	A high level input strobe loads the transmitter data (T_A, T_B, T_C, T_D) into the transmitter divisor select register. This input may be strobed or hard-wired to a high level.
13-16	T_D, T_C, T_B, T_A	Transmitter-Divisor Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter divisor select data bits.
18	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.

For electrical characteristics, see page 217.

STANDARD MICROSYSTEMS CORPORATION

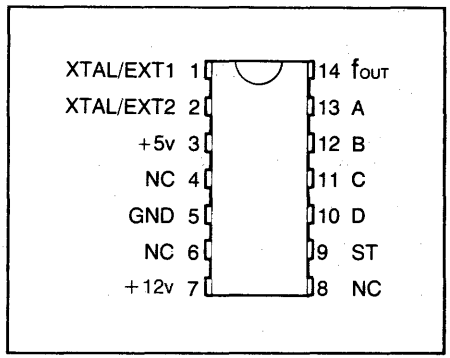
COM 5026
COM 5026T

Baud Rate Generator
Programmable Divider

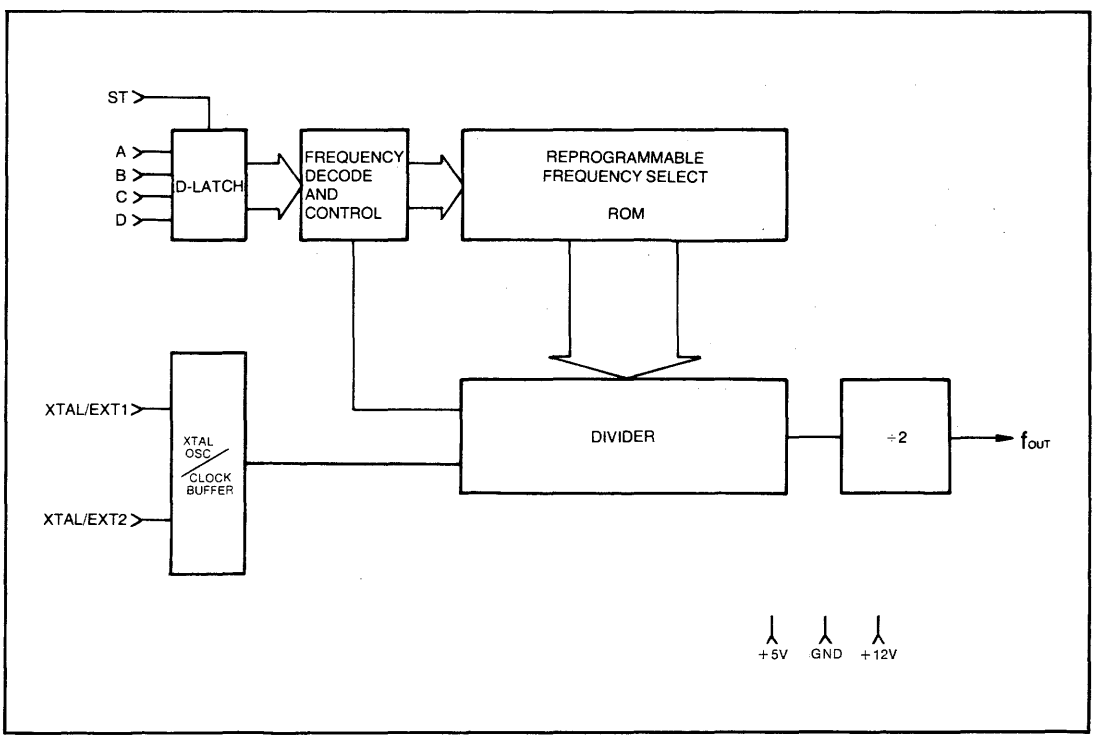
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Choice of 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ TTL, MOS compatibility

PIN CONFIGURATION



BLOCK DIAGRAM



SECTION IV

GENERAL DESCRIPTION

The Standard Microsystems COM 5026 Baud Rate Generator/Programmable Divider is an N-channel COPLAMOS® MOS/LSI device which, from a single crystal (on-chip oscillator) or input frequency is capable of generating 16 externally selectable frequencies.

The COM 5026 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies as shown in Table 1. One of the sixteen output frequencies is externally selected by four address inputs, as shown in Table 1.

Internal re-programmable ROM allows the generation of other frequencies from other crystal frequencies or input frequencies. The four address inputs may be strobe (150ns) or DC loaded.

The COM 5026 is basically a programmable 15-stage feedback shift register capable of dividing any modulo up to $(2^{15}-1)$.

By using the frequency output, it is possible to generate additional divisions of the master clock frequency by cascading COM 5026's. The frequency output is fed into the XTAL/EXT input on a subsequent device. In this way one crystal or input frequency may be used to generate numerous output frequencies.

The COM 5026 can be driven by either an external crystal or TTL logic level inputs; COM 5026T is driven by TTL logic level inputs only.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.
3	V_{CC}	Power Supply	+5 volt Supply
4,6,8	NC	No Connection	
5	GND	Ground	Ground
7	V_{DD}	Power Supply	+12 volt Supply
9	ST	Strobe	A high-level strobe loads the Input Address (A_A, A_B, A_C, A_D) into the Input Address register. This input may be strobed or hard wired to a high-level.
10-13	A_D, A_C, A_B, A_A	Input Address	The logic level on these inputs, as shown in Table 1, selects the output frequency.
14	f_{OUT}	Output Frequency	This output runs at a frequency as selected by the Input Address.

For electrical characteristics, see page 217.

STANDARD MICROSYSTEMS CORPORATION

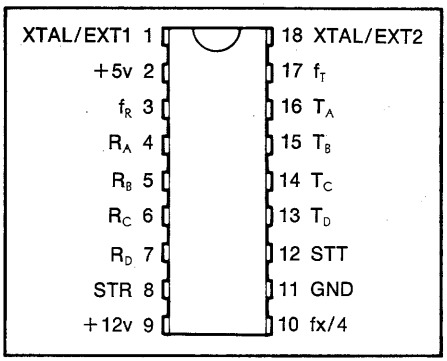
COM 5036
COM 5036T

Dual Baud Rate Generator
Programmable Divider

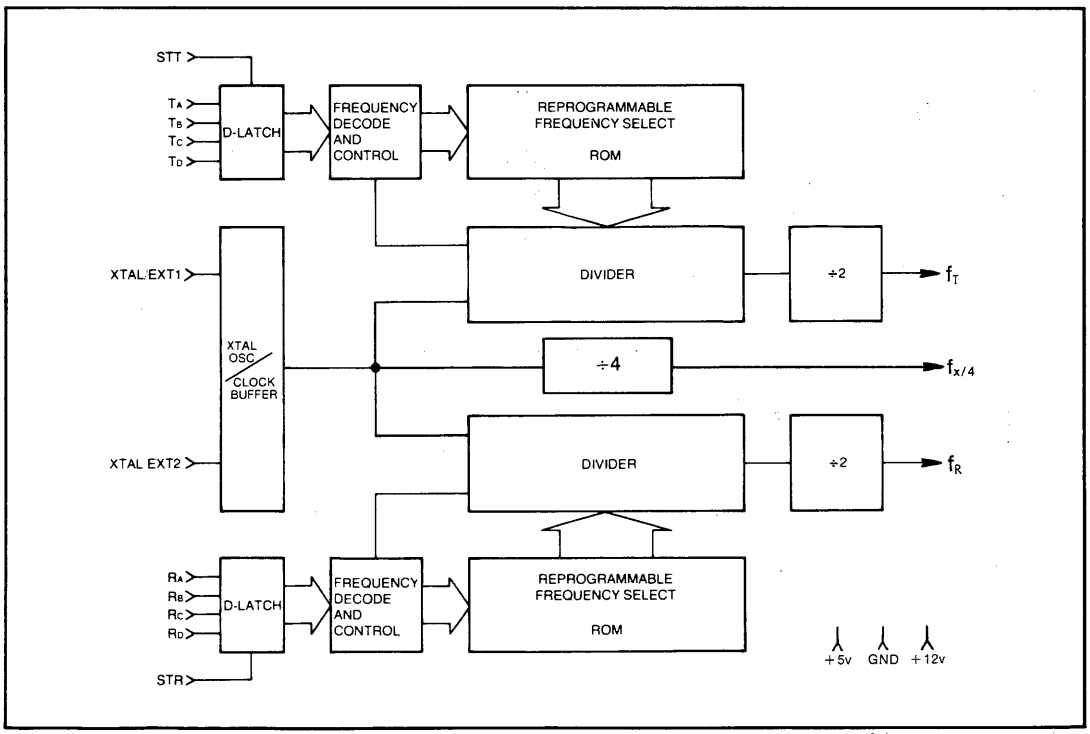
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Choice of 2 x 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Full duplex communication capability
- ☐ High frequency reference output
- ☐ TTL, MOS compatibility

PIN CONFIGURATION



BLOCK DIAGRAM



General Description

The Standard Microsystems COM 5036 Dual Baud Rate Generator/Programmable Divider is an N-channel COPLAMOS® MOS/LSI device which, from a single crystal (on-chip oscillator) or input frequency is capable of generating 32 externally selectable frequencies.

The COM 5036 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies as shown in Table 1. One of the sixteen output frequencies is externally selected by four address inputs, on each of the independent dividers, as shown in Table 1.

Internal re-programmable ROM allows the generation of other frequencies from other crystal frequencies or input frequencies. The four address inputs on each divider section may be strobe (150ns) or DC loaded. As the COM 5036 is a dual baud rate generator, full duplex (independent receive and transmit frequencies) operation is possible.

The COM 5036 is basically a programmable 15-stage feedback shift register capable of dividing any modulo up to $(2^{15}-1)$.

By using one of the frequency outputs it is possible to generate additional divisions of the master clock frequency by cascading COM 5036's. The frequency output is fed into the XTAL/EXT input on a subsequent device. In this way one crystal or input frequency may be used to generate numerous output frequencies.

The COM 5036 can be driven by either an external crystal or TTL logic level inputs; COM 5036T is driven by TTL logic level inputs only.

The COM 5036 provides a high frequency reference output at one-quarter (1/4) the XTAL/EXT input frequency.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+5 volt supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver divisor select data bits.
4-7	R_A, R_B, R_C, R_D	Receiver-Divisor Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver	A high level input strobe loads the receiver data (R_A, R_B, R_C, R_D) into the receiver divisor select register. This input may be strobed or hard-wired to a high level.
9	V_{DD}	Power Supply	+12 volt supply
10	$f_X/4$	$f_X/4$	¼ crystal/clock frequency reference output.
11	GND	Ground	Ground
12	STT	Strobe-Transmitter	A high level input strobe loads the transmitter data (T_A, T_B, T_C, T_D) into the transmitter divisor select register. This input may be strobed or hard-wired to a high level.
13-16	T_D, T_C, T_B, T_A	Transmitter-Divider Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter divisor select data bits.
18	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.

For electrical characteristics, see page 217.

STANDARD MICROSYSTEMS CORPORATION

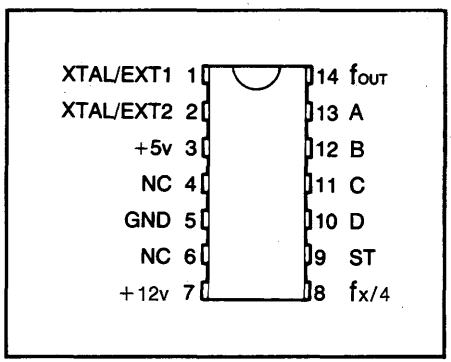
COM 5046
COM 5046T

Baud Rate Generator
Programmable Divider

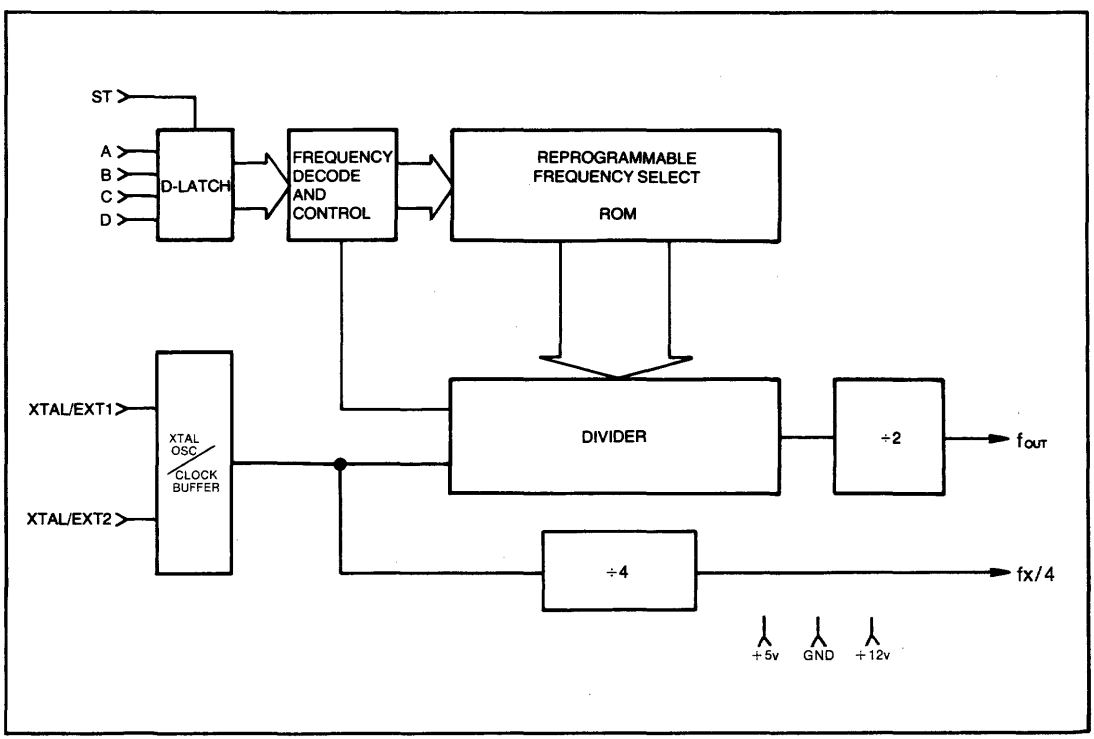
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Choice of 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ High frequency reference output
- ☐ TTL, MOS compatibility

PIN CONFIGURATION



BLOCK DIAGRAM



GENERAL DESCRIPTION

The Standard Microsystems COM 5046 Baud Rate Generator/Programmable Divider is an N-channel COPLAMOS® MOS/LSI device which, from a single crystal (on-chip oscillator) or input frequency is capable of generating 16 externally selectable frequencies.

The COM 5046 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies as shown in Table 1. One of the sixteen output frequencies is externally selected by four address inputs; as shown in Table 1.

Internal re-programmable ROM allows the generation of other frequencies from other crystal frequencies or input frequencies. The four address inputs may be strobe (150ns) or DC loaded.

The COM 5046 is basically a programmable 15-stage feedback shift register capable of dividing any modulo up to $(2^{15}-1)$.

By using the frequency output, it is possible to generate additional divisions of the master clock frequency by cascading COM 5046's. The frequency output is fed into the XTAL/EXT input on a subsequent device. In this way one crystal or input frequency may be used to generate numerous output frequencies.

The COM 5046 can be driven by either an external crystal or TTL logic level inputs; COM 5046T is driven by TTL logic level inputs only.

The COM 5046 provides a high frequency reference output at one-quarter (1/4) the XTAL/EXT input frequency.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.
3	V_{CC}	Power Supply	+5 volt Supply.
4,6	NC	No Connection	
5	GND	Ground	Ground
7	V_{DD}	Power Supply	+12 volt Supply.
8	$f_{X/4}$	Reference Frequency	High frequency reference output @ (1/4) f_{IN}
9	ST	Strobe	A high-level strobe loads the Input Address (A_A, A_B, A_C, A_D) into the input Address register. This input may be strobed or hard wired to a high-level,
10-13	A_D, A_C, A_B, A_A	Input Address	The logic level on these inputs, as shown in Table 1, selects the output frequency.
14	f_{OUT}	Output Frequency	This output runs at a frequency as selected by the Input Address.

For electrical characteristics, see page 217.

ELECTRICAL CHARACTERISTICS COM5016, COM5016T, COM5026, COM5026T, COM5036, COM5036T, COM5046, COM5046T

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

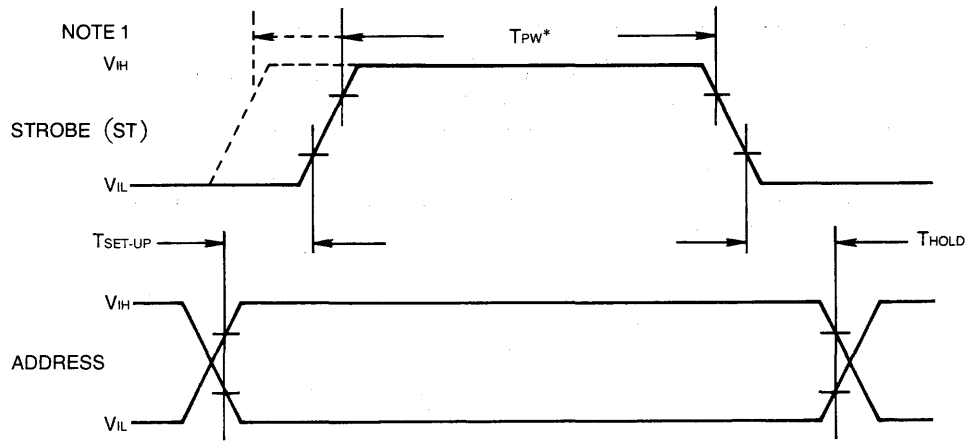
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, V_{DD}=+12V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	excluding XTAL inputs
High-level, V_{IH}	2.0		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL} = 1.6ma
			0.5	V	I_{OL} = 3.2ma
High-level, V_{OH}	V_{CC}−1.5	4.0		V	I_{OH} = 100μA
INPUT CURRENT					
Low-level, I_{IL}			0.3	mA	V_{IN} = GND, excluding XTAL inputs
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	V_{IN} = GND, excluding XTAL inputs
EXT INPUT LOAD		8	10		Series 7400 unit loads
POWER SUPPLY CURRENT					
I_{CC}		28	45	mA	
I_{DD}		12	22	mA	
A.C. CHARACTERISTICS					T_A = +25°C
CLOCK FREQUENCY		5.0688		MHz	XTAL, EXT
PULSE WIDTH					
Clock					50% Duty Cycle ±5%
Strobe	150		DC	ns	See Note 1.
INPUT SET-UP TIME					
Address	50			ns	See Note 1.
INPUT HOLD TIME					
Address	50			ns	
STROBE TO NEW FREQUENCY DELAY			3.5	μs	$=1/f_{IN}$ (18)

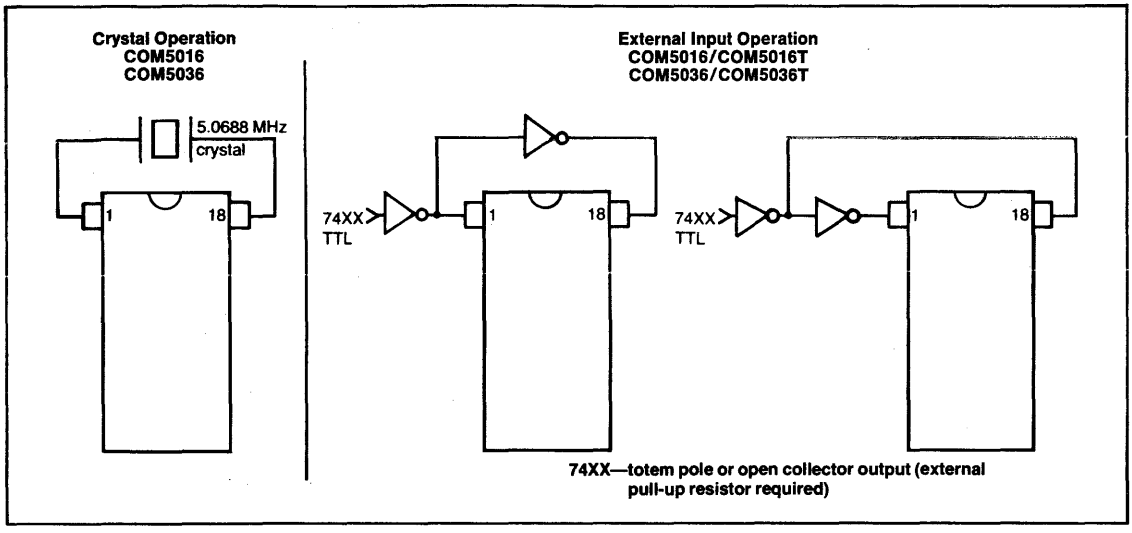
Note 1: Input set-up time can be decreased to ≥ 0ns by increasing the minimum strobe width by 50ns to a total of 200ns.

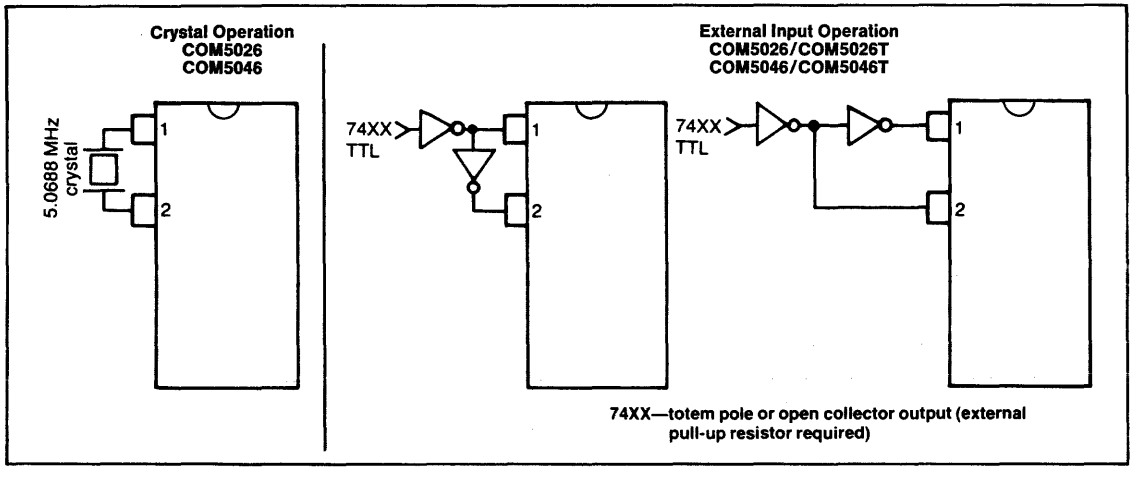
TIMING DIAGRAM



*Address need only be valid during the last T_{PW}, Min time of the input strobe.

SECTION IV





For ROM re-programming SMC has a computer program available whereby the customer need only supply the input frequency and the desired output frequencies. The ROM programming is automatically generated.

Crystal Specifications

User must specify termination (pin, wire, other)

Prefer: HC-18/U or HC-25/U

Frequency — 5.0688 MHz, AT cut

Temperature range 0°C to 70°C

Series resistance <50 Ω

Series Resonant

Overall tolerance ± .01%

or as required

Crystal manufacturers (Partial List)

Northern Engineering Laboratories
357 Beloit Street
Burlington, Wisconsin 53105
(414) 763-3591

Bulova Frequency Control Products
61-20 Woodside Avenue
Woodside, New York 11377
(212) 335-6000

CTS Knights Inc.
101 East Church Street
Sandwich, Illinois 60548
(815) 786-8411

Crystek Crystals Corporation
1000 Crystal Drive
Fort Myers, Florida 33901
(813) 936-2109

APPLICATIONS INFORMATION

Charge pump techniques using the +5 volt power supply can be used to generate the +12 volt power supply required. The +12 volt power supply of figure 1 will supply the 22 milli-amps that is typically required.

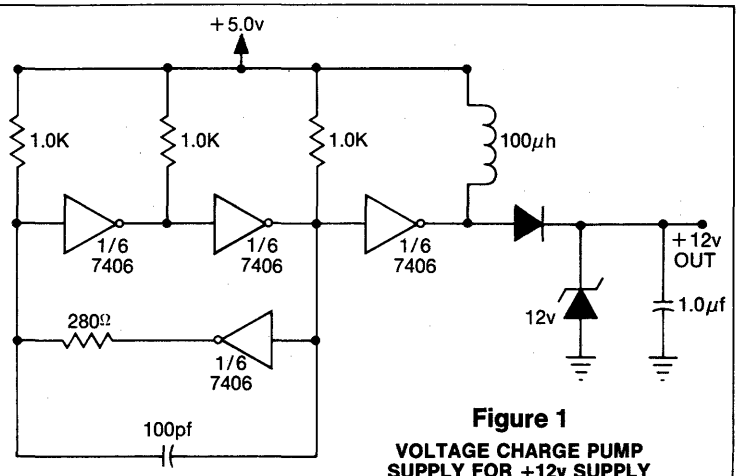


Figure 1
VOLTAGE CHARGE PUMP SUPPLY FOR +12v SUPPLY

When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that the clamp circuit of figure 2 or a Semtech* bi-polarity silicon transient suppressor such as the 1N6110 be used.

*SEMTECH CORPORATION
652 Mitchel Road
Newbury Park, California 91320
213-628-5392

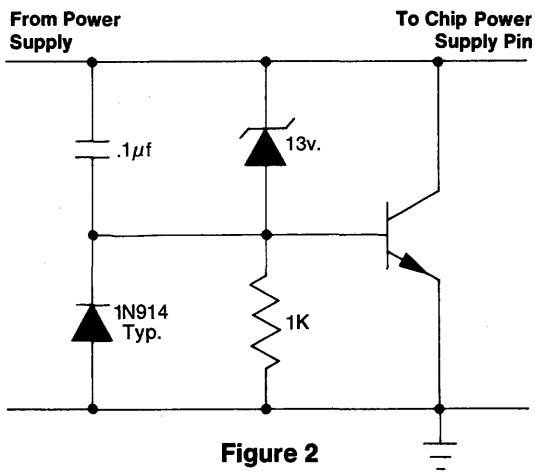


Figure 2
OVER-VOLTAGE PROTECTION CIRCUIT

Baud Rate Generator Output Frequency Options

Table 1. (16X clock)

CRYSTAL FREQUENCY = 5.0688 MHz

Tr'mit/Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	50	0.8 KHz	0.8 KHz	—	50/50	6336
0	0	0	1	75	1.2	1.2	—	50/50	4224
0	0	1	0	110	1.76	1.76	—	50/50	2880
0	0	1	1	134.5	2.152	2.1523	0.016	50/50	2355
0	1	0	0	150	2.4	2.4	—	50/50	2112
0	1	0	1	300	4.8	4.8	—	50/50	1056
0	1	1	0	600	9.6	9.6	—	50/50	528
0	1	1	1	1200	19.2	19.2	—	50/50	264
1	0	0	0	1800	28.8	28.8	—	50/50	176
1	0	0	1	2000	32.0	32.081	0.253	50/50	158
1	0	1	0	2400	38.4	38.4	—	50/50	132
1	0	1	1	3600	57.6	57.6	—	50/50	88
1	1	0	0	4800	76.8	76.8	—	50/50	66
1	1	0	1	7200	115.2	115.2	—	50/50	44
1	1	1	0	9600	153.6	153.6	—	48/52	33
1	1	1	1	19.200	307.2	316.8	3.125	50/50	16

Table 2. (16X clock)

CRYSTAL FREQUENCY = 4.9152 MHz

Tr'mit/Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	50	0.8 KHz	0.8 KHz	—	50/50	6144
0	0	0	1	75	1.2	1.2	—	50/50	4096
0	0	1	0	110	1.76	1.7589	−0.01	*	2793
0	0	1	1	134.5	2.152	2.152	—	50/50	2284
0	1	0	0	150	2.4	2.4	—	50/50	2048
0	1	0	1	300	4.8	4.8	—	50/50	1024
0	1	1	0	600	9.6	9.6	—	50/50	512
0	1	1	1	1200	19.2	19.2	—	50/50	256
1	0	0	0	1800	28.8	28.7438	−0.19	*	171
1	0	0	1	2000	32.0	31.9168	−0.26	50/50	154
1	0	1	0	2400	38.4	38.4	—	50/50	128
1	0	1	1	3600	57.6	57.8258	0.39	*	85
1	1	0	0	4800	76.8	76.8	—	50/50	64
1	1	0	1	7200	115.2	114.306	−0.77	*	43
1	1	1	0	9600	153.6	153.6	—	50/50	32
1	1	1	1	19,200	307.2	307.2	—	50/50	16

Table 3. (32X clock)

CRYSTAL FREQUENCY = 5.0688 MHz

Tr'mit/Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 32X Clock	Actual Frequency 32X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	50	1.6 KHz	1.6 KHz	—	50/50	3168
0	0	0	1	75	2.4	2.4	—	50/50	2112
0	0	1	0	110	3.52	3.52	—	50/50	1440
0	0	1	1	134.5	4.304	4.306	.06	*	1177
0	1	0	0	150	4.8	4.8	—	50/50	1056
0	1	0	1	200	6.4	6.4	—	50/50	792
0	1	1	0	300	9.6	9.6	—	50/50	528
0	1	1	1	600	19.2	19.2	—	50/50	264
1	0	0	0	1200	38.4	38.4	—	50/50	132
1	0	0	1	1800	57.6	57.6	—	50/50	88
1	0	1	0	2400	76.8	76.8	—	50/50	66
1	0	1	1	3600	115.2	115.2	—	50/50	44
1	1	0	0	4800	153.6	153.6	—	*	33
1	1	0	1	7200	230.4	230.4	—	50/50	22
1	1	1	0	9600	307.2	316.8	3.125	50/50	16
1	1	1	1	19,200	614.4	633.6	3.125	50/50	8

OUTPUT FREQUENCY OPTIONS

Part No.	Dash Number		
	Table 1	Table 2	Table 3
5016/5016T	STD	−5	−6
5026/5026T	STD	−5	−6
5036/5036T	STD	N/A	N/A
5046/5046T	STD	N/A	N/A

*When Duty Cycle is not exactly 50%, it is 50% ± 10%.

STANDARD MICROSYSTEMS CORPORATION

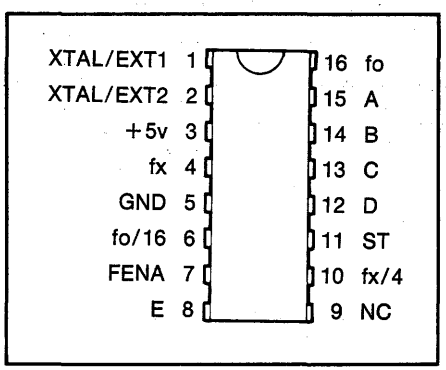
COM 8046
COM 8046T

Baud Rate Generator
Programmable Divider

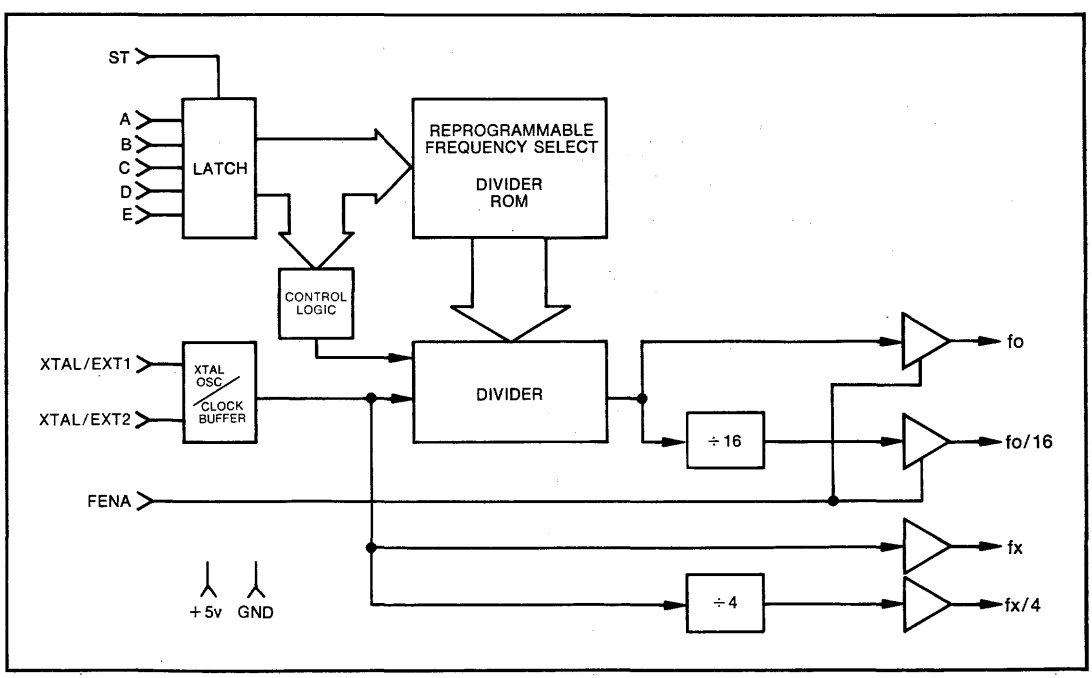
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Single +5v power supply
- ☐ Choice of 32 output frequencies
- ☐ 32 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Re-programmable ROM via CLASP® technology allows generation of other frequencies
- ☐ TTL, MOS compatible
- ☐ 1X Clock via fo/16 output
- ☐ Crystal frequency output via fx and fx/4 outputs
- ☐ Output disable via FENA

PIN CONFIGURATION



BLOCK DIAGRAM



General Description

The Standard Microsystems COM 8046 is an enhanced version of the COM 5046 Baud Rate Generator. It is fabricated using SMC's patented COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply.

The standard COM 8046 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 1X, 16X and 32X UART/USRT/ASTRO/USYNRT devices.

The COM 8046 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 2. Parts suitable for use only with an external TTL reference are marked COM 8046T. TTL outputs used to drive the COM 8046 or COM 8046T should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The reference frequency (fx) is used to provide two high frequency outputs: one at fx and the other at fx/4. The fx/4 output will drive one standard 7400 load, while the fx output will drive two 74LS loads.

The output of the oscillator/buffer is applied to the divider for generation of the output frequency f_O. The divider is capable of dividing by any integer from 6 to $2^{19} + 1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer than it is low by one fx clock period. The output of the divider is also divided internally by 16 and made available at the $f_O/16$ output pin. The $f_O/16$ output will drive one and the f_O output will drive two standard 7400 TTL loads. Both the f_O and $f_O/16$ outputs can be disabled by supplying a low logic level to the FENA input pin. Note that the FENA input has an internal pull-up which will cause the pin to rise to approximately V_{CC} if left unconnected.

The divisor ROM contains 32 divisors, each 19 bits wide, and is fabricated using SMC's unique CLASP® technology. This process permits reduction of turn-around-time for ROM patterns.

The five divisor select bits are held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is effected within 3.5μs of a change in any of the five divisor select bits; strobe activity is not required. This feature may be disabled through a CLASP® programming option causing new frequency initiation to be delayed until the end of the current f_O half-cycle All five data inputs have pull-ups identical to that of the FENA input, while the strobe input has no pull-up.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.
3	V_{CC}	Power Supply	+5 volt supply
4	f_X	f_X	Crystal/clock frequency reference output
5	GND	Ground	Ground
6	$f_O/16$	$f_O/16$	1X clock output
7	FENA	Enable	A low level at this input causes the f_O and $f_O/16$ outputs to be held high. An open or a high level at the FENA input enables the f_O and $f_O/16$ outputs.
8	E	E	Most significant divisor select data bit. An open at this input is equivalent to a logic high.
9	NC	NC	No connection
10	$f_X/4$	$f_X/4$	¼ crystal/clock frequency reference output.
11	ST	Strobe	Divisor select data strobe. Data is sampled when this input is high, preserved when this input is low.
12-15	D,C,B,A	D,C,B,A	Divisor select data bits. A=LSB. An open circuit at these inputs is equivalent to a logic high.
16	f_O	f_O	16X clock output

For electrical characteristics, see page 231.

STANDARD MICROSYSTEMS CORPORATION

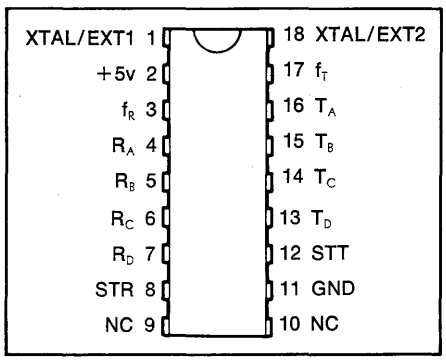
COM 8116
COM 8116T

Dual Baud Rate Generator
Programmable Divider

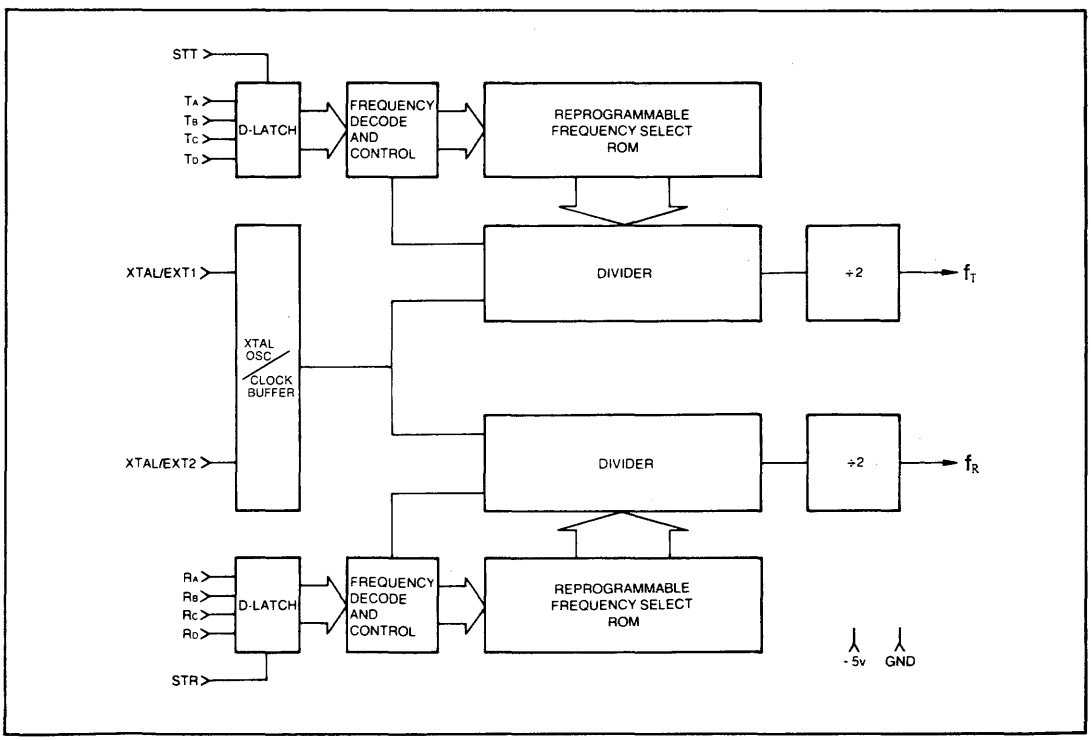
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Single +5v power supply
- ☐ Choice of 2 x 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Full duplex communication capability
- ☐ Re-programmable ROM via CLASP® technology allows generation of other frequencies
- ☐ TTL, MOS compatibility
- ☐ Compatible with COM 5016

PIN CONFIGURATION



BLOCK DIAGRAM



General Description

The Standard Microsystem's COM 8116 is an enhanced version of the COM 5016 Dual Baud Rate Generator. It is fabricated using SMC's patented COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply.

The standard COM 8116 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 16X UART/USRT devices. A large number of the frequencies available are also useful for 1X and 32X ASTRO/USYNRT devices.

The COM 8116 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 18. Parts suitable for use only with an external TTL reference are marked COM 8116T. TTL outputs used to drive the COM 8116 or COM 8116T XTAL/EXT inputs should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The output of the oscillator/buffer is applied to the dividers for generation of the output frequencies f_T, f_R. The dividers are capable of dividing by any integer from 6 to $2^{19} + 1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer than it is low by one fx clock period.

Each of the two divisor ROMs contains 16 divisors, each 19 bits wide, and is fabricated using SMC's unique CLASP® technology allowing up to 32 different divisors on custom parts. This process permits reduction of turn-around time for ROM patterns. Each group of four divisor select bits is held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is effected within 3.5μs of a change in any of the four divisor select bits (strobe activity is not required). The divisor select inputs have pull-up resistors; the strobe inputs do not.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+5 volt supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver divisor select data bits.
4-7	R_A, R_B, R_C, R_D	Receiver-Divisor Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver	A high level input strobe loads the receiver data (R_A, R_B, R_C, R_D) into the receiver divisor select register. This input may be strobed or hard-wired to a high level.
9	NC	No Connection	
10	NC	No Connection	
11	GND	Ground	Ground
12	STT	Strobe-Transmitter	A high level input strobe loads the transmitter data (T_A, T_B, T_C, T_D) into the transmitter divisor select register. This input may be strobed or hard-wired to a high level.
13-16	T_D, T_C, T_B, T_A	Transmitter-Divisor Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter divisor select data bits.
18	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.

For electrical characteristics, see page 231.

STANDARD MICROSYSTEMS CORPORATION

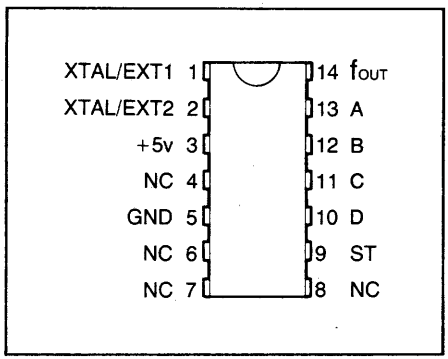
COM 8126
COM 8126T

Baud Rate Generator
Programmable Divider

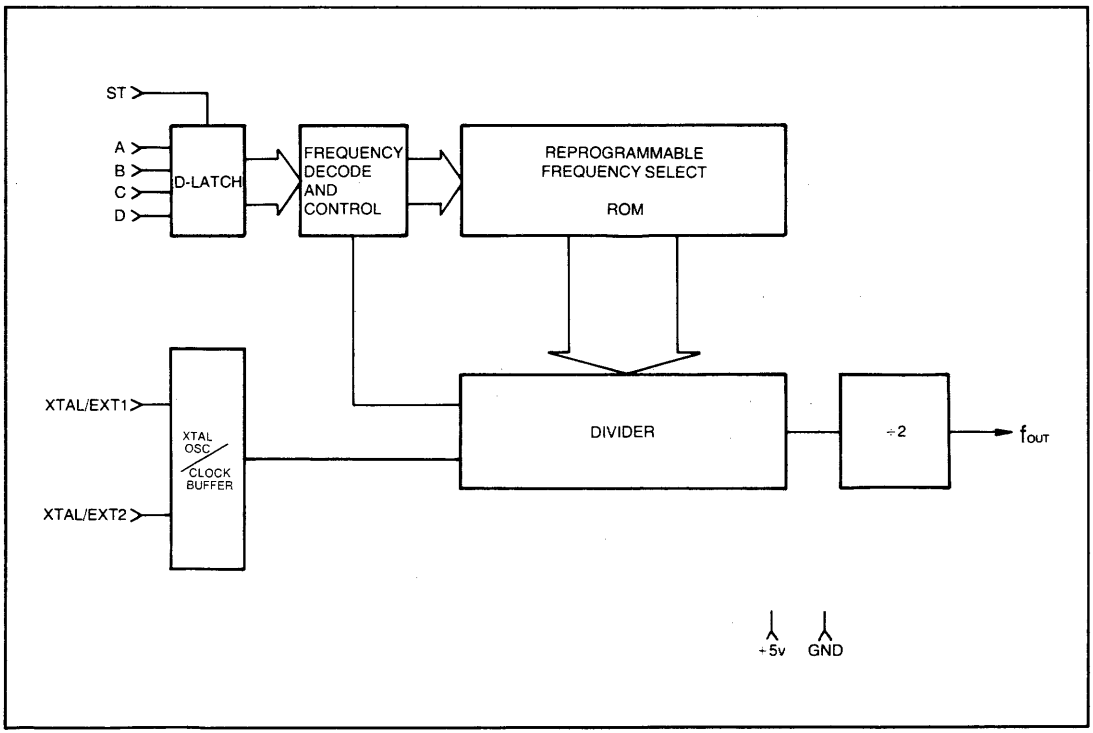
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Single +5v power supply
- ☐ Choice of 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Re-programmable ROM via CLASP® technology allows generation of other frequencies
- ☐ TTL, MOS compatibility
- ☐ Compatible with COM 5026

PIN CONFIGURATION



BLOCK DIAGRAM



General Description

The Standard Microsystem's COM 8126 is an enhanced version of the COM 5026 Baud Rate Generator. It is fabricated using SMC's patented COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply.

The standard COM 8126 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 16X UART/USRT devices. A large number of the frequencies available are also useful for 1X and 32X ASTRO/USYNRT devices.

The COM 8126 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 2. Parts suitable for use only with an external TTL reference are marked COM 8126T. TTL outputs used to drive the COM 8126 or COM 8126T XTAL/EXT inputs should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The output of the oscillator/buffer is applied to the divider for generation of the output frequency. The divider is capable of dividing by any integer from 6 to $2^{19} + 1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer than it is low by one fx clock period.

The divisor ROM contains 16 divisors, each 19 bits wide, and is fabricated using SMC's unique CLASP® technology. This process permits reduction of turn-around time for ROM patterns. The four divisor select bits are held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is effected within 3.5μs of a change in any of the four divisor select bits (strobe activity is not required). This feature may be disabled through a CLASP® programming option causing new frequency initiation to be delayed until the end of the current f_{OUT} half-cycle. The divisor select inputs have pull-up resistors; the strobe input does not.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.
3	V_{CC}	Power Supply	+5 volt supply
4,6,7,8	NC	No Connection	
5	GND	Ground	Ground
9	ST	Strobe	A high level strobe loads the input data (A, B, C, D) into the input divisor select register. This input may be strobed or hard-wired to a high level.
10-13	D,C, B, A	Divisor Select Data Bits	The logic level on these inputs as shown in Table 1, selects the output frequency.
14	f_{OUT}	Output Frequency	This output runs at a frequency selected by the divisor select data bits.

For electrical characteristics, see page 231.

STANDARD MICROSYSTEMS CORPORATION

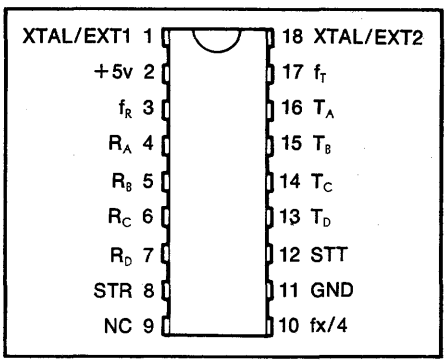
COM 8136
COM 8136T

Dual Baud Rate Generator
Programmable Divider

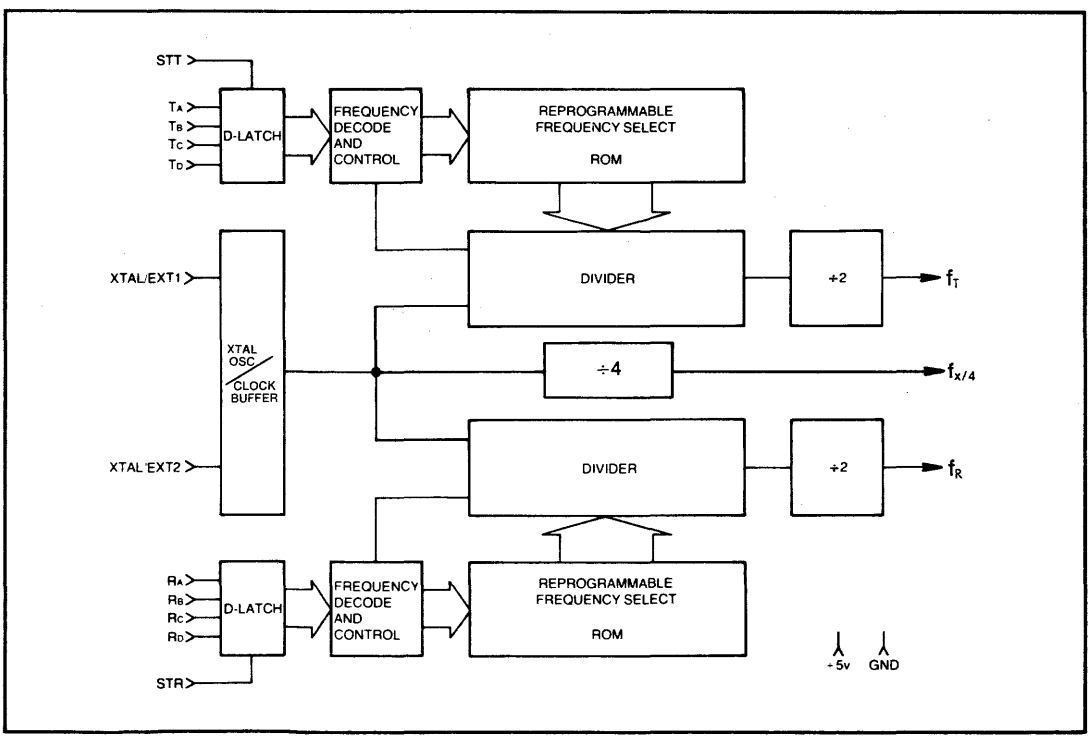
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Single +5v power supply
- ☐ Choice of 2 x 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Full duplex communication capability
- ☐ High frequency reference output
- ☐ Re-programmable ROM via CLASP® technology allows generation of other frequencies
- ☐ TTL, MOS compatibility
- ☐ Compatible with COM 5036

PIN CONFIGURATION



BLOCK DIAGRAM



General Description

The Standard Microsystem's COM 8136 is an enhanced version of the COM 5036 Dual Baud Rate Generator. It is fabricated using SMC's patented COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply.

The standard COM 8136 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 16X UART/USRT devices. A large number of the frequencies available are also useful for 1X and 32X ASTRO/USYNRT devices.

The COM 8136 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 18. Parts suitable for use only with an external TTL reference are marked COM 8136T. TTL outputs used to drive the COM 8136 or COM 8136T XTAL/EXT inputs should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The output of the oscillator/buffer is applied to the dividers for generation of the output frequencies f_T, f_R. The dividers are capable of dividing by any integer from 6 to $2^{19} + 1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer than it is low by one fx clock period.

The reference frequency (fx) is used to provide a high frequency output at fx/4.

Each of the two divisor ROMs contains 16 divisors, each 19 bits wide, and is fabricated using SMC's unique CLASP® technology allowing up to 32 different divisors on custom parts. This process permits reduction of turn-around time for ROM patterns. Each group of four divisor select bits is held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is effected within 3.5μs of a change in any of the four divisor select bits (strobe activity is not required). The divisor select inputs have pull-up resistors; the strobe inputs do not.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+5 volt supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver divisor select data bits.
4-7	R_A, R_B, R_C, R_D	Receiver-Divisor Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver	A high level input strobe loads the receiver data (R_A, R_B, R_C, R_D) into the receiver divisor select register. This input may be strobed or hard-wired to a high level.
9	NC	No Connection	
10	$f_X/4$	$f_X/4$	¼ crystal/clock frequency reference output.
11	GND	Ground	Ground
12	STT	Strobe-Transmitter	A high level input strobe loads the transmitter data (T_A, T_B, T_C, T_D) into the transmitter divisor select register. This input may be strobed or hard-wired to a high level.
13-16	T_D, T_C, T_B, T_A	Transmitter-Divider Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter divisor select data bits.
18	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.

For electrical characteristics, see page 231.

STANDARD MICROSYSTEMS CORPORATION

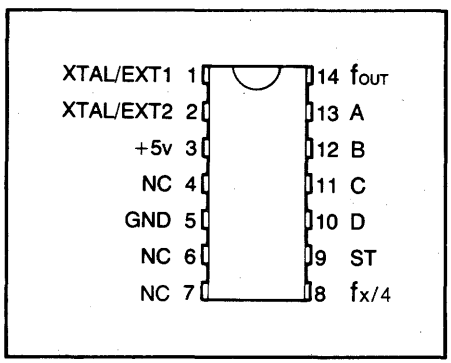
COM 8146
COM 8146T

Baud Rate Generator
Programmable Divider

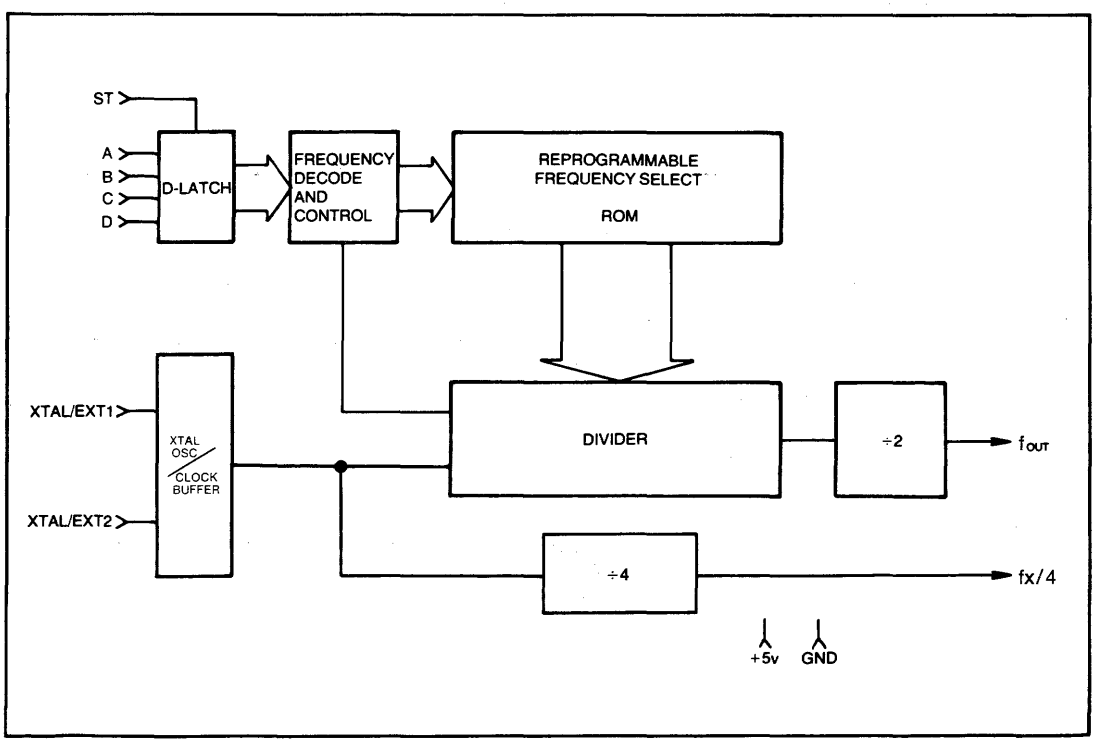
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Single +5v power supply
- ☐ Choice of 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ High frequency reference output
- ☐ Re-programmable ROM via CLASP® technology allows generation of other frequencies
- ☐ TTL, MOS compatibility
- ☐ Compatible with COM 5046

PIN CONFIGURATION



BLOCK DIAGRAM



General Description

The Standard Microsystem's COM 8146 is an enhanced version of the COM 5046 Baud Rate Generator. It is fabricated using SMC's patented COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply.

The standard COM 8146 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 16X UART/USRT devices. A large number of the frequencies available are also useful for 1X and 32X ASTRO/USYNRT devices.

The COM 8146 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 2. Parts suitable for use only with an external TTL reference are marked COM 8146T. TTL outputs used to drive the COM 8146 or COM 8146T XTAL/EXT inputs should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The output of the oscillator/buffer is applied to the divider for generation of the output frequency. The divider is capable of dividing by any integer from 6 to $2^{19} + 1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer than it is low by one fx clock period.

The reference frequency (fx) is used to provide a high frequency output at fx/4.

The divisor ROM contains 16 divisors, each 19 bits wide, and is fabricated using SMC's unique CLASP® technology. This process permits reduction of turnaround time for ROM patterns. The four divisor select bits are held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is effected within 3.5μs of a change in any of the four divisor select bits (strobe activity is not required). This feature may be disabled through a CLASP® programming option causing new frequency initiation to be delayed until the end of the current f_{OUT} half-cycle. The divisor select inputs have pull-up resistors; the strobe input does not.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.
3	V_{CC}	Power Supply	+5 volt supply
4,6,7	NC	No Connection	
5	GND	Ground	Ground
8	$f_X/4$	$f_X/4$	¼ crystal/clock frequency reference output.
9	ST	Strobe	A high level strobe loads the input data (A, B, C, D) into the input divisor select register. This input may be strobed or hard-wired to a high level.
10-13	D,C,B,A	Divisor Select Data Bits	The logic level on these inputs as shown in Table 1, selects the output frequency.
14	f_{OUT}	Output Frequency	This output runs at a frequency selected by the divisor select data bits.

For electrical characteristics, see page 231.

ELECTRICAL CHARACTERISTICS COM8046, COM8046T, COM8116, COM8116T, COM8126, COM8126T, COM8136, COM8136T, COM8146, COM8146T

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

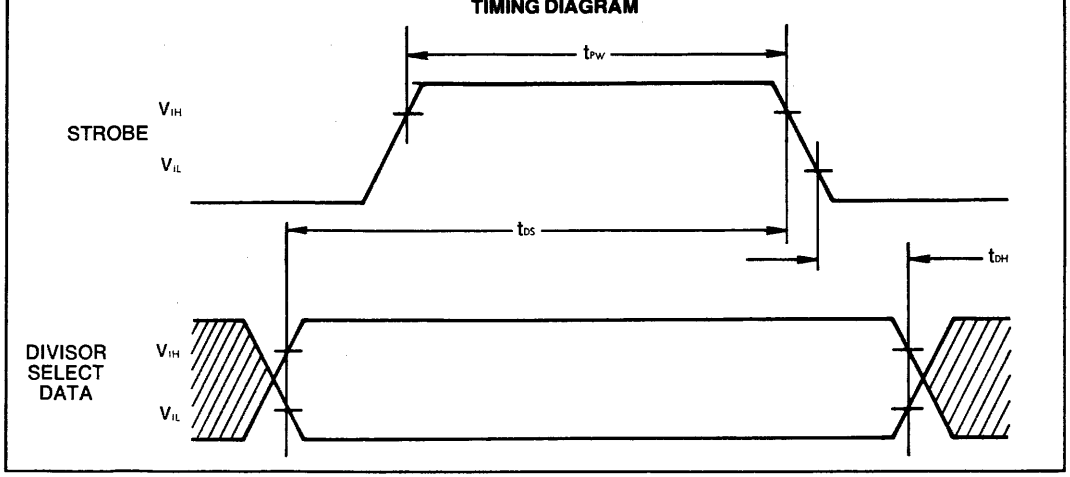
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

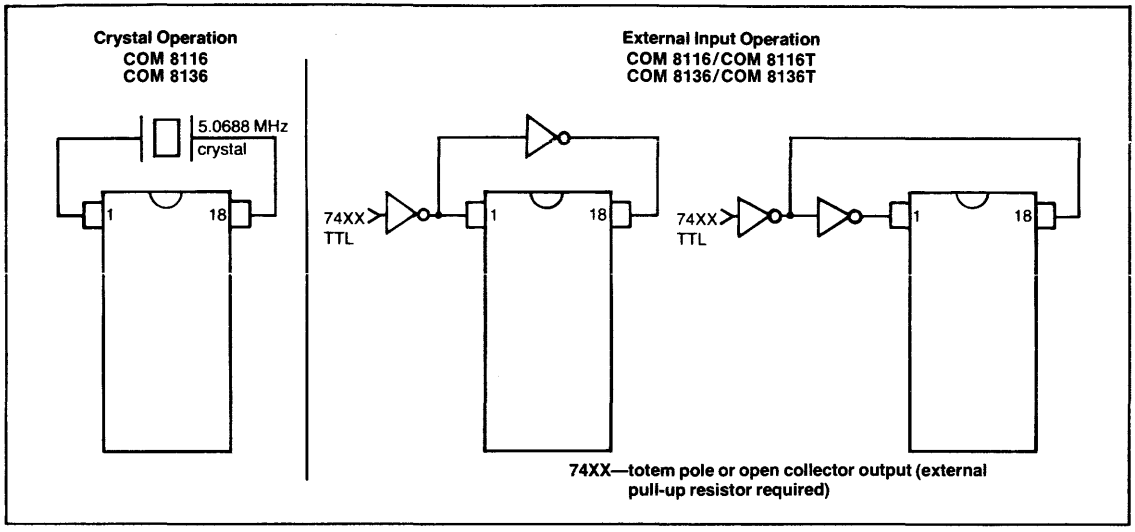
NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

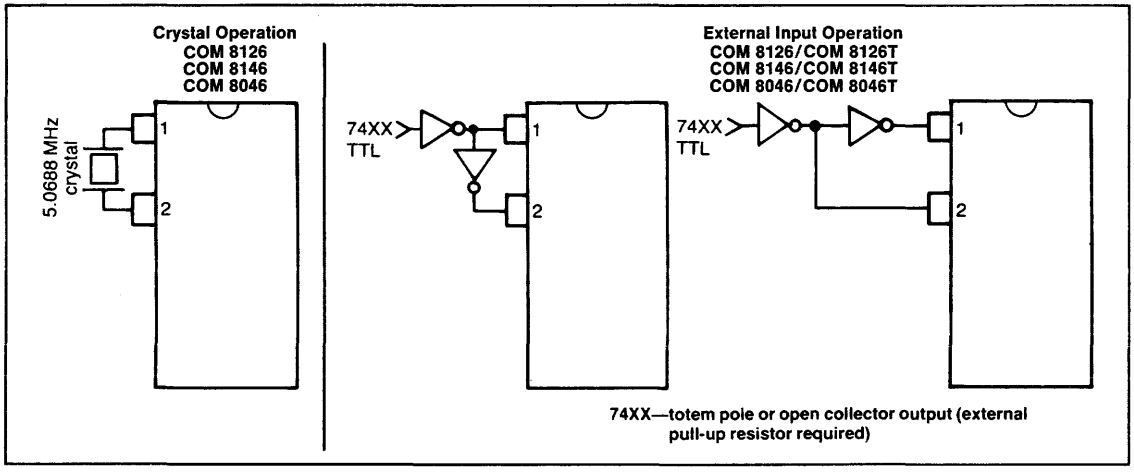
ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}= +5V ±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	
High-level, V_{IH}	2.0			V	excluding XTAL inputs
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL} = 1.6mA, for $f_X/4$, $f_O/16$
			0.4	V	I_{OL} = 3.2mA, for f_O, f_R, f_T
			0.4	V	I_{OL} = 0.8mA, for f_X
High-level, V_{OH}	3.5			V	I_{OH} = −100μA; for f_x, I_{OH} = −50μA
INPUT CURRENT					
Low-level, I_{IL}			-0.1	mA	V_{IN} = GND, excluding XTAL inputs
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pF	V_{IN} = GND, excluding XTAL inputs
EXT INPUT LOAD		8	10		Series 7400 equivalent loads
POWER SUPPLY CURRENT					
I_{CC}			50	mA	
A.C. CHARACTERISTICS					T_A = +25°C
CLOCK FREQUENCY, f_{IN}	0.01		7.0	MHz	XTAL/EXT, 50% Duty Cycle ±5% COM 8046, COM 8126, COM 8146
	0.01		5.1	MHz	XTAL/EXT, 50% Duty Cycle ±5% COM 8116, COM 8136
STROBE PULSE WIDTH, t_{PW}	150		DC	ns	
INPUT SET-UP TIME					
t_{DS}	200			ns	
INPUT HOLD TIME					
t_{DH}	50			ns	
STROBE TO NEW FREQUENCY DELAY			3.5	μs	@ f_x = 5.0 MHz

TIMING DIAGRAM







For ROM re-programming SMC has a computer program available whereby the customer need only supply the input frequency and the desired output frequencies. The ROM programming is automatically generated.

Crystal Specifications

User must specify termination (pin, wire, other)

Prefer: HC-18/U or HC-25/U

Frequency — 5.0688 MHz, AT cut

Temperature range 0°C to 70°C

Series resistance $<50\ \Omega$

Series Resonant

Overall tolerance ± .01%

or as required

Crystal manufacturers (Partial List)

Northern Engineering Laboratories
357 Beloit Street
Burlington, Wisconsin 53105
(414) 763-3591

Bulova Frequency Control Products
61-20 Woodside Avenue
Woodside, New York 11377
(212) 335-6000

CTS Knights Inc.
101 East Church Street
Sandwich, Illinois 60548
(815) 786-8411

Crystek Crystals Corporation
1000 Crystal Drive
Fort Myers, Florida 33901
(813) 936-2109

COM 8046
COM 8046T

Table 2

REFERENCE FREQUENCY = 5.068800MHz

Divisor Select EDCBA	Desired Baud Rate	Clock Factor	Desired Frequency (KHz)	Divisor	Actual Baud Rate	Actual Frequency (KHz)	Deviation
00000	50.00	32X	1.60000	3168	50.00	1.600000	0.0000%
00001	75.00	32X	2.40000	2112	75.00	2.400000	0.0000%
00010	110.00	32X	3.52000	1440	110.00	3.520000	0.0000%
00011	134.50	32X	4.30400	1177	134.58	4.306542	0.0591%
00100	150.00	32X	4.80000	1056	150.00	4.800000	0.0000%
00101	200.00	32X	6.40000	792	200.00	6.400000	0.0000%
00110	300.00	32X	9.60000	528	300.00	9.600000	0.0000%
00111	600.00	32X	19.20000	264	600.00	19.200000	0.0000%
01000	1200.00	32X	38.40000	132	1200.00	38.400000	0.0000%
01001	1800.00	32X	57.60000	88	1800.00	57.600000	0.0000%
01010	2400.00	32X	76.80000	66	2400.00	76.800000	0.0000%
01011	3600.00	32X	115.20000	44	3600.00	115.200000	0.0000%
01100	4800.00	32X	153.60000	33	4800.00	153.600000	0.0000%
01101	7200.00	32X	230.40000	22	7200.00	230.400000	0.0000%
01110	9600.00	32X	307.20000	16	9900.00	316.800000	3.1250%
01111	19200.00	32X	614.40000	8	19800.00	633.600000	3.1250%
10000	50.00	16X	0.80000	6336	50.00	0.800000	0.0000%
10001	75.00	16X	1.20000	4224	75.00	1.200000	0.0000%
10010	110.00	16X	1.76000	2880	110.00	1.760000	0.0000%
10011	134.50	16X	2.15200	2355	134.52	2.152357	0.0166%
10100	150.00	16X	2.40000	2112	150.00	2.400000	0.0000%
10101	300.00	16X	4.80000	1056	300.00	4.800000	0.0000%
10110	600.00	16X	9.60000	528	600.00	9.600000	0.0000%
10111	1200.00	16X	19.20000	264	1200.00	19.200000	0.0000%
11000	1800.00	16X	28.80000	176	1800.00	28.800000	0.0000%
11001	2000.00	16X	32.00000	158	2005.06	32.081013	0.2532%
11010	2400.00	16X	38.40000	132	2400.00	38.400000	0.0000%
11011	3600.00	16X	57.60000	88	3600.00	57.600000	0.0000%
11100	4800.00	16X	76.80000	66	4800.00	76.800000	0.0000%
11101	7200.00	16X	115.20000	44	7200.00	115.200000	0.0000%
11110	9600.00	16X	153.60000	33	9600.00	153.600000	0.0000%
11111	19200.00	16X	307.20000	16	19800.00	316.800000	3.1250%

Baud Rate Generator Output Frequency Options

Table 1. (16X clock)

CRYSTAL FREQUENCY = 5.0688 MHz

Tr'mit/Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	50	0.8 KHz	0.8 KHz	—	50/50	6336
0	0	0	1	75	1.2	1.2	—	50/50	4224
0	0	1	0	110	1.76	1.76	—	50/50	2880
0	0	1	1	134.5	2.152	2.1523	0.016	50/50	2355
0	1	0	0	150	2.4	2.4	—	50/50	2112
0	1	0	1	300	4.8	4.8	—	50/50	1056
0	1	1	0	600	9.6	9.6	—	50/50	528
0	1	1	1	1200	19.2	19.2	—	50/50	264
1	0	0	0	1800	28.8	28.8	—	50/50	176
1	0	0	1	2000	32.0	32.081	0.253	50/50	158
1	0	1	0	2400	38.4	38.4	—	50/50	132
1	0	1	1	3600	57.6	57.6	—	50/50	88
1	1	0	0	4800	76.8	76.8	—	50/50	66
1	1	0	1	7200	115.2	115.2	—	50/50	44
1	1	1	0	9600	153.6	153.6	—	48/52	33
1	1	1	1	19.200	307.2	316.8	3.125	50/50	16

Table 2. (16X clock)

CRYSTAL FREQUENCY = 4.9152 MHz

Tr'mit/Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	50	0.8 KHz	0.8 KHz	—	50/50	6144
0	0	0	1	75	1.2	1.2	—	50/50	4096
0	0	1	0	110	1.76	1.7589	−0.01	*	2793
0	0	1	1	134.5	2.152	2.152	—	50/50	2284
0	1	0	0	150	2.4	2.4	—	50/50	2048
0	1	0	1	300	4.8	4.8	—	50/50	1024
0	1	1	0	600	9.6	9.6	—	50/50	512
0	1	1	1	1200	19.2	19.2	—	50/50	256
1	0	0	0	1800	28.8	28.7438	−0.19	*	171
1	0	0	1	2000	32.0	31.9168	−0.26	50/50	154
1	0	1	0	2400	38.4	38.4	—	50/50	128
1	0	1	1	3600	57.6	57.8258	0.39	*	85
1	1	0	0	4800	76.8	76.8	—	50/50	64
1	1	0	1	7200	115.2	114.306	−0.77	*	43
1	1	1	0	9600	153.6	153.6	—	50/50	32
1	1	1	1	19,200	307.2	307.2	—	50/50	16

Table 3. (32X clock)

CRYSTAL FREQUENCY = 5.0688 MHz

Tr'mit/Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 32X Clock	Actual Frequency 32X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	50	1.6 KHz	1.6 KHz	—	50/50	3168
0	0	0	1	75	2.4	2.4	—	50/50	2112
0	0	1	0	110	3.52	3.52	—	50/50	1440
0	0	1	1	134.5	4.304	4.306	.06	*	1177
0	1	0	0	150	4.8	4.8	—	50/50	1056
0	1	0	1	200	6.4	6.4	—	50/50	792
0	1	1	0	300	9.6	9.6	—	50/50	528
0	1	1	1	600	19.2	19.2	—	50/50	264
1	0	0	0	1200	38.4	38.4	—	50/50	132
1	0	0	1	1800	57.6	57.6	—	50/50	88
1	0	1	0	2400	76.8	76.8	—	50/50	66
1	0	1	1	3600	115.2	115.2	—	50/50	44
1	1	0	0	4800	153.6	153.6	—	*	33
1	1	0	1	7200	230.4	230.4	—	50/50	22
1	1	1	0	9600	307.2	316.8	3.125	50/50	16
1	1	1	1	19,200	614.4	633.6	3.125	50/50	8

OUTPUT FREQUENCY OPTIONS

Dash Number		
Table 1	Table 2	Table 3
STD	−5	−6
STD	−5	−6
STD	N/A	N/A
STD	N/A	N/A

*When Duty Cycle is not exactly 50%, it is 50% ± 10%.

Baud Rate Generator Output Frequency Options

COM 8116T-013

CRYSTAL FREQUENCY = 2.76480 MHz

Transmit/ Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	50	0.8 KHz	0.8 KHz	0	50/50	3456
0	0	0	1	75	1.2	1.2	0	50/50	2304
0	0	1	0	110	1.76	1.76	−.006	50/50	1571
0	0	1	1	134.5	2.152	2.152	−.019	50/50	1285
0	1	0	0	150	2.4	2.4	0	50/50	1152
0	1	0	1	200	3.2	3.2	0	50/50	864
0	1	1	0	300	4.8	4.8	0	50/50	576
0	1	1	1	600	9.6	9.6	0	50/50	288
1	0	0	0	1200	19.2	19.2	0	50/50	144
1	0	0	1	1800	28.8	28.8	0	50/50	96
1	0	1	0	2000	32.0	32.149	+.465	50/50	86
1	0	1	1	2400	38.4	38.4	0	50/50	72
1	1	0	0	3600	57.6	57.6	0	50/50	48
1	1	0	1	4800	76.8	76.8	0	50/50	36
1	1	1	0	9600	153.6	153.6	0	50/50	18
1	1	1	1	19,200	307.2	307.2	0	44/56	9

COM 8116T-003

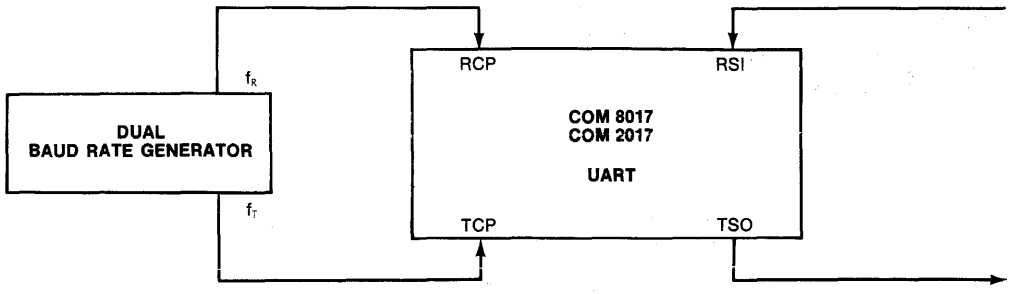
CRYSTAL FREQUENCIES = 6.01835 MHz

Transmit/ Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	50	0.8 KHz	799.9 Hz	0	50/50	7523
0	0	0	1	75	1.2	1200.0	0	50/50	5015
0	0	1	0	110	1.76	1759.7	0	50/50	3420
0	0	1	1	134.5	2.152	2151.7	0	50/50	2797
0	1	0	0	150	2.4	2399.6	0	50/50	2508
0	1	0	1	200	3.2	3199.5	0	50/50	1881
0	1	1	0	300	4.8	4799.3	0	50/50	1254
0	1	1	1	600	9.6	9598.6	0	50/50	627
1	0	0	0	1200	19.2	19227.9	+0.14	50/50	313
1	0	0	1	1800	28.8	28795.9	0	50/50	209
1	0	1	0	2000	32.0	32012.5	0	50/50	188
1	0	1	1	2400	38.4	38333.4	−0.17	50/50	157
1	1	0	0	3600	57.6	57868.7	+0.46	50/50	104
1	1	0	1	4800	76.8	77158.3	+0.46	50/50	78
1	1	1	0	9600	153.6	154316.6	+0.46	50/50	39
1	1	1	1	19,200	307.2	300917.5	2.04	50/50	20

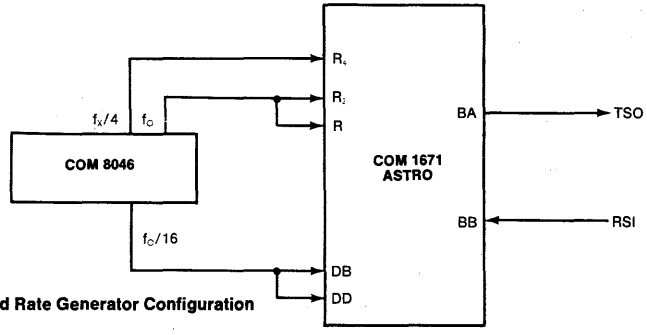
COM 8116T-013A

CRYSTAL FREQUENCY—5.52960 MHz

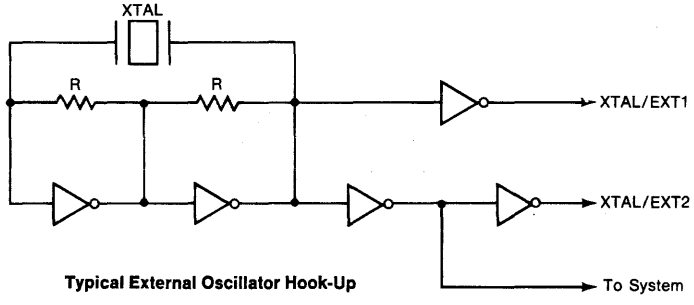
Transmit/ Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	100	1.6 KHz	1.6 KHz	0	50/50	3456
0	0	0	1	150	2.4	2.4	0	50/50	2304
0	0	1	0	220	3.52	3.5197	−.006	50/50	1571
0	0	1	1	269	4.304	4.3032	−.019	50/50	1285
0	1	0	0	300	4.8	4.8	0	50/50	1152
0	1	0	1	400	6.4	6.4	0	50/50	864
0	1	1	0	600	9.6	9.6	0	50/50	576
0	1	1	1	1200	19.2	19.2	0	50/50	288
1	0	0	0	2400	38.4	38.4	0	50/50	144
1	0	0	1	3600	57.6	57.6	0	50/50	96
1	0	1	0	4000	64.0	64.298	+.466	50/50	86
1	0	1	1	4800	76.8	76.8	0	50/50	72
1	1	0	0	7200	115.2	115.2	0	50/50	48
1	1	0	1	9600	153.6	153.6	0	50/50	36
1	1	1	0	19,200	307.2	307.2	0	50/50	18
1	1	1	1	38,400	614.8	614.8	0	44/56	9



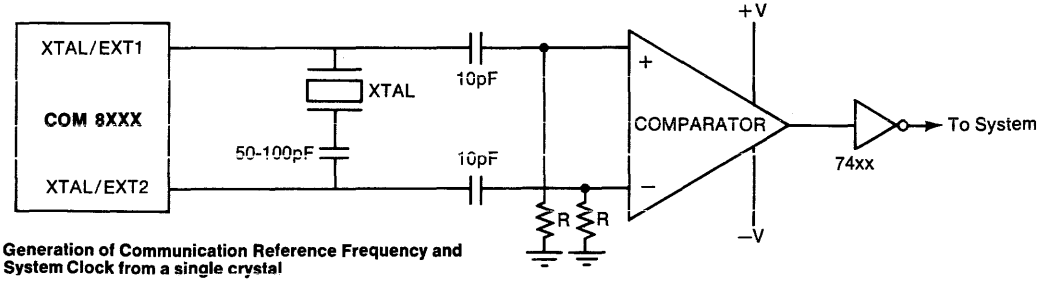
Typical UART—Dual Baud Rate Generator Configuration
Full Duplex—Split Speed



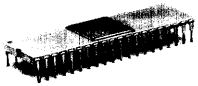
Typical ASTRO—Baud Rate Generator Configuration



Typical External Oscillator Hook-Up



Generation of Communication Reference Frequency and System Clock from a single crystal



CRT Display

TIMING CONTROLLERS

Part Number	Description	Features	Display Format	Max Clock	Power Supplies	Package	Page
CRT 5027	provides all of the timing and control for interlaced and non-interlaced CRT display		programmable	4 MHz	+5, +12	40 DIP	239-246
CRT 5037		balanced beam interlace	programmable	4 MHz	+5, +12	40 DIP	239-246
CRT 5047 (1)		fixed format	80 column 24 row	4 MHz	+5, +12	40 DIP	247-248
CRT 5067		line-lock	programmable	4 MHz	+5, +12	40 DIP	239-246
CRT 7220, −1, −2	Graphics Display Controller	Intelligent graphics display controller	1024 x 1024 Pixel	4/5/5.5 MHz	+5	40 DIP	249-251
CRT 9007	CRT video processor and controller	sequential or row-table driven memory	programmable	4 MHz	+5	40 DIP	251-270
CRT 96364A/B	complete CRT processor	on-chip cursor and write control	64 column 16 row	1.6 MHz	+5	28 DIP	271-278

VDAC™ DISPLAY CONTROLLERS

Part Number	Description	Display	Attributes	Max Clock	Power Supply	Package	Page
CRT 8002H	Provides complete display and attributes control for alphanumeric and graphics display. Consists of 7 x 11 x 128 character generator, video shift register, latches, graphics and attributes circuits.	7 x 11 dot matrix, wide graphics, thin graphics, on-chip cursor	reverse video blank blink underline strike-thru	25 MHz	+5	28 DIP	293-300
CRT 8002A (1,3)				20 MHz			279-288
CRT 8002B (1,3)				15 MHz			279-288
CRT 8002C (1,3)				10 MHz			279-288

CHARACTER GENERATORS

Part Number	Description	Max Frequency	Power Supply	Package	Page
CRT 7004A (1,4)	7 x 11 x 128 character generator, latches, video shift register	20 MHz	+5	24 DIP	301-306
CRT 7004B (1,4)		15 MHz			
CRT 7004C (1,4)		10 MHz			

ROW BUFFER

Part Number	Description	Max Row Length	Power Supply	Package	Page
CRT 9006-83	8 bit wide serial cascadable single row buffer memory for CRT or printer	83 characters	+5	24 DIP	307-312
CRT 9006-135		135 characters			
CRT 9212	8 bit wide serial cascadable double row buffer memory for CRT or printer	135 characters	+5	28 DIP	313-318

VIDEO ATTRIBUTES CONTROLLERS

Part Number	Description	Display	Attributes	Max Clock	Power Supply	Package	Page
CRT 8021	Provides attributes and graphics control for CRT video displays	Alphanumeric, wide graphics, thin graphics, on-chip cursor	Reverse video, blank, blink, underline, strike-thru	20 MHz	+5	28 DIP	319-326
CRT 9021B	Provides attributes and graphics control for CRT video displays	Alphanumeric, wide graphics, thin graphics, on-chip cursor, double height, double width	Reverse video, blank, blink, underline, intensity	28.5 MHz	+5	28 DIP	327-338

(1) May be custom mask programmed
(2) For future release
(3) Also available as CRT 8002A,B,C — 001 Katakana
CRT 8002A,B,C — 003 5X7 dot matrix
(4) Also available as CRT 7004A,B,C — 003 5X7 dot matrix

SECTION V

STANDARD MICROSYSTEMS CORPORATION

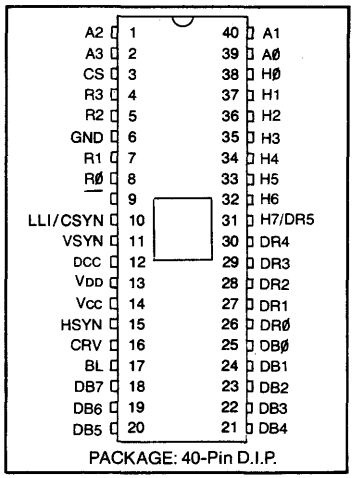
CRT 5027
CRT 5037
CRT 5057
μPC FAMILY

CRT Video Timer and Controller VTAC®

FEATURES

- ☐ Fully Programmable Display Format
  - Characters per data row (1-200)
  - Data rows per frame (1-64)
  - Raster scans per data row (1-16)
- ☐ Programmable Monitor Sync Format
  - Raster Scans/Frame (256-1023)
  - "Front Porch"
  - Sync Width
  - "Back Porch"
  - Interlace/Non-Interlace
  - Vertical Blanking
- ☐ Lock Line Input (CRT 5057)
- ☐ Direct Outputs to CRT Monitor
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync (CRT 5027, CRT 5037)
  - Blanking
  - Cursor coincidence
- ☐ Programmed via:
  - Processor data bus
  - External PROM
  - Mask Option ROM
- ☐ Standard or Non-Standard CRT Monitor Compatible
- ☐ Refresh Rate: 60Hz, 50Hz,...
- ☐ Scrolling
  - Single Line
  - Multi-Line
- ☐ Cursor Position Registers
- ☐ Character Format: 5x7, 7x9,...
- ☐ Programmable Vertical Data Positioning
- ☐ Balanced Beam Current Interlace (CRT 5037)
- ☐ Graphics Compatible

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

- ☐ Split-Screen Applications
  - Horizontal
  - Vertical
- ☐ Interlace or Non-Interlace operation
- ☐ TTL Compatibility
- ☐ BUS Oriented
- ☐ High Speed Operation
- ☐ COPLAMOS® N-Channel Silicon Gate Technology
- ☐ Compatible with CRT 8002 VDAC™
- ☐ Compatible with CRT 7004

GENERAL DESCRIPTION

The CRT Video Timer and Controller Chip (VTAC)® is a user programmable 40-pin COPLAMOS® n channel MOS/LSI device containing the logic functions required to generate all the timing signals for the presentation and formatting of interlaced and non-interlaced video data on a standard or non-standard CRT monitor.

With the exception of the dot counter, which may be clocked at a video frequency above 25 MHz and therefore not recommended for MOS implementation, all frame formatting, such as horizontal, vertical, and composite sync, characters per data row, data rows per frame, and raster scans per data row and per frame are totally user programmable. The data row counter has been designed to facilitate scrolling.

Programming is effected by loading seven 8 bit control registers directly off an 8 bit bidirectional data bus. Four register address lines and a chip select line provide complete microprocessor compatibility for program controlled set up. The device can be "self loaded" via an external PROM tied on the data bus as described in the OPERATION section. Formatting can also be programmed by a single mask option.

In addition to the seven control registers two additional registers are provided to store the cursor character and data row addresses for generation of the cursor video signal. The contents of these two registers can also be read out onto the bus for update by the program.

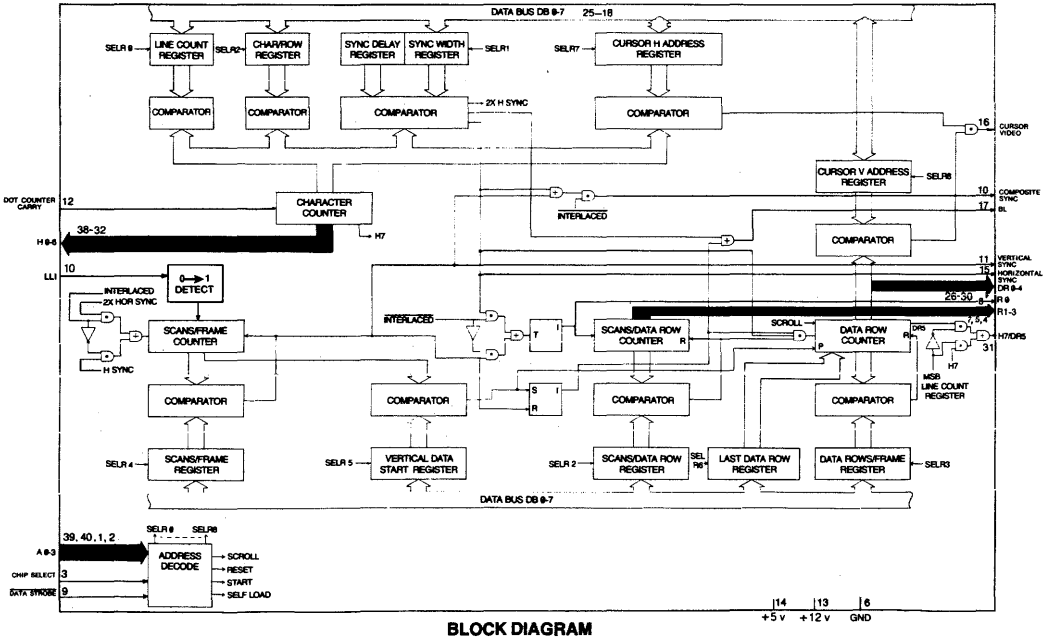
Three versions of the VTAC® are available. The CRT 5027 provides non-interlaced operation with an even or odd number of scan lines per data row, or interlaced operation with an even number of scan lines per data row. The CRT 5037 may be programmed for an odd or even number of scan lines per data row in both interlaced and non-interlaced modes. Programming the CRT 5037 for an odd number of scan lines per data row eliminates character distortion caused by the uneven beam current normally associated with odd field/even field interlacing of alphanumeric displays.

The CRT 5057 provides the ability to lock a CRT's vertical refresh rate, as controlled by the VTAC's® vertical sync pulse, to the 50 Hz or 60 Hz line frequency thereby eliminating the so called "swim" phenomenon. This is particularly well suited for European system requirements. The line frequency waveform, processed to conform to the VTAC's® specified logic levels, is applied to the line lock input. The VTAC® will inhibit generation of vertical sync until a zero to one transition on this input is detected. The vertical sync pulse is then initiated within one scan line after this transition rises above the logic threshold of the VTAC.®

To provide the pin required for the line lock input, the composite sync output is not provided in the CRT 5057.

Description of Pin Functions

Pin No.	Symbol	Name	Input/ Output	Function
25-18	DBØ–7	Data Bus	I/O	Data bus. Input bus for control words from microprocessor or PROM. Bidirectional bus for cursor address.
3	CS	Chip Select	I	Signals chip that it is being addressed
39, 40, 1, 2	AØ-3	Register Address	I	Register address bits for selecting one of seven control registers or either of the cursor address registers
9	$\overline{DS}$	Data Strobe	I	Strobes DBØ-7 into the appropriate register or outputs the cursor character address or cursor line address onto the data bus
12	DCC	DOT Counter Carry	I	Carry from off chip dot counter establishing basic character clock rate. Character clock.
38-32	HØ-6	Character Counter Outputs	O	Character counter outputs.
7, 5, 4	R1-3	Scan Counter Outputs	O	Three most significant bits of the Scan Counter; row select inputs to character generator.
31	H7/DR5	H7/DR5	O	Pin definition is user programmable. Output is MSB of Character Counter if horizontal line count (REG.Ø) is ≧128; otherwise output is MSB of Data Row Counter.
8	RØ	Scan Counter LSB	O	Least significant bit of the scan counter. In the interlaced mode with an even number of scans per data row, RØ will toggle at the field rate; for an odd number of scans per data row in the interlaced mode, RØ will toggle at the data row rate.
26-30	DRØ-4	Data Row Counter Outputs	O	Data Row counter outputs.
17	BL	Blank	O	Defines non active portion of horizontal and vertical scans.
15	HSYN	Horizontal Sync	O	Initiates horizontal retrace.
11	VSYN	Vertical Sync	O	Initiates vertical retrace.
10	CSYN/ LLI	Composite Sync Output/ Line Lock Input	O/I	Composite sync is provided on the CRT 5027 and CRT 5037. This output is active in non-interlaced mode only. Provides a true RS-170 composite sync wave form. For the CRT 5057, this pin is the Line Lock Input. The line frequency waveform, processed to conform to the VTAC's® specified logic levels, is applied to this pin.
16	CRV	Cursor Video	O	Defines cursor location in data field.
14	V_{CC}	Power Supply	PS	+5 volt Power Supply
13	V_{DD}	Power Supply	PS	+12 volt Power Supply



BLOCK DIAGRAM

Operation

The design philosophy employed was to allow the device to interface effectively with either a microprocessor based or hardwire logic system. The device is programmed by the user in one of two ways; via the processor data bus as part of the system initialization routine, or during power up via a PROM tied on the data bus and addressed directly by the Row Select outputs of the chip. (See figure 4). Seven 8 bit words are required to fully program the chip. Bit assignments for these words are shown in Table 1. The information contained in these seven words consists of the following:

Horizontal Formatting:

Characters/Data Row	A 3 bit code providing 8 mask programmable character lengths from 20 to 132. The standard device will be masked for the following character lengths; 20, 32, 40, 64, 72, 80, 96, and 132.
Horizontal Sync Delay	3 bits assigned providing up to 8 character times for generation of "front porch".
Horizontal Sync Width	4 bits assigned providing up to 15 character times for generation of horizontal sync width.
Horizontal Line Count	8 bits assigned providing up to 256 character times for total horizontal formatting.
Skew Bits	A 2 bit code providing from a 0 to 2 character skew (delay) between the horizontal address counter and the blank and sync (horizontal, vertical, composite) signals to allow for retiming of video data prior to generation of composite video signal. The Cursor Video signal is also skewed as a function of this code.

Vertical Formatting:

Interlaced/Non-interlaced	This bit provides for data presentation with odd/even field formatting for interlaced systems. It modifies the vertical timing counters as described below. A logic 1 establishes the interlace mode.
Scans/Frame	8 bits assigned, defined according to the following equations: Let X = value of 8 assigned bits. 1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields. Range = 513 to 1023 scans/frame, odd counts only. 2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011). Range = 256 to 766 scans/frame, even counts only. In either mode, vertical sync width is fixed at three horizontal scans (= 3H).
Vertical Data Start	8 bits defining the number of raster scans from the leading edge of vertical sync until the start of display data. At this raster scan the data row counter is set to the data row address at the top of the page.
Data Rows/Frame	6 bits assigned providing up to 64 data rows per frame.
Last Data Row	6 bits to allow up or down scrolling via a preload defining the count of the last displayed data row.
Scans/Data Row	4 bits assigned providing up to 16 scan lines per data row.

Additional Features

Device Initialization:

Under microprocessor control—The device can be reset under system or program control by presenting a 1Ø1Ø address on A3-Ø. The device will remain reset at the top of the even field page until a start command is executed by presenting a 111Ø address on A3-Ø.

Via "Self Loading"—In a non-processor environment, the self loading sequence is effected by presenting and holding the 1111 address on A3-Ø, and is initiated by the receipt of the strobe pulse ($\overline{DS}$). The 1111 address should be maintained long enough to insure that all seven registers have been loaded (in most applications under one millisecond). The timing sequence will begin one line scan after the 1111 address is removed. In processor based systems, self loading is initiated by presenting the Ø111 address to the device. Self loading is terminated by presenting the start command to the device which also initiates the timing chain.

Scrolling—In addition to the Register 6 storage of the last displayed data row a "scroll" command (address 1Ø11) presented to the device will increment the first displayed data row count to facilitate up scrolling in certain applications.

Control Registers Programming Chart

Horizontal Line Count: Total Characters/Line = N + 1, N = 0 to 255 (DB0 = LSB)

Characters/Data Row:

DB2	DB1	DB0		
0	0	0	= 20	Active Characters/Data Row
0	0	1	= 32	
0	1	0	= 40	
0	1	1	= 64	
1	0	0	= 72	
1	0	1	= 80	
1	1	0	= 96	
1	1	1	= 132	

Horizontal Sync Delay: = N, from 1 to 7 character times (DB0 = LSB) (N = 0 Disallowed)

Horizontal Sync Width: = N, from 1 to 15 character times (DB3 = LSB) (N = 0 Disallowed)

Skew Bits

DB7	DB6	Sync/Blank Delay (Character Times)	Cursor Delay (Character Times)
0	0	0	0
1	0	1	0
0	1	2	1
1	1	2	2

Scans/Frame 8 bits assigned, defined according to the following equations:
Let X = value of 8 assigned bits. (DB0 = LSB)

1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields.

Range = 513 to 1023 scans/frame, odd counts only.

2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011).

Range = 256 to 766 scans/frame, even counts only.

In either mode, vertical sync width is fixed at three horizontal scans (=3H).

Vertical Data Start: N = number of raster lines delay after leading edge of vertical sync of vertical start position. (DB0 = LSB)

Data Rows/Frame: Number of data rows = N + 1, N = 0 to 63 (DBO = LSB)

Last Data Row: N = Address of last dsplayed data row, N = 0 to 63, ie; for 24 data rows, program N = 23. (DB0 = LSB)

Mode: Register, 1, DB7 = 1 establishes Interlace.

Scans/Data Row:

Interlace Mode

CRT 5027: Scans per Data Row = N + 1 where N = programmed number of scans/data rows. N = 0 to 15. Scans per data row must be even counts only.

CRT 5037, CRT 5057: Scans per data Row = N + 2. N = 0 to 14, odd or even counts.

Non-Interlace Mode

CRT 5027, CRT 5037, CRT 5057: Scans per Data Row = N + 1, odd or even count. N = 0 to 15.

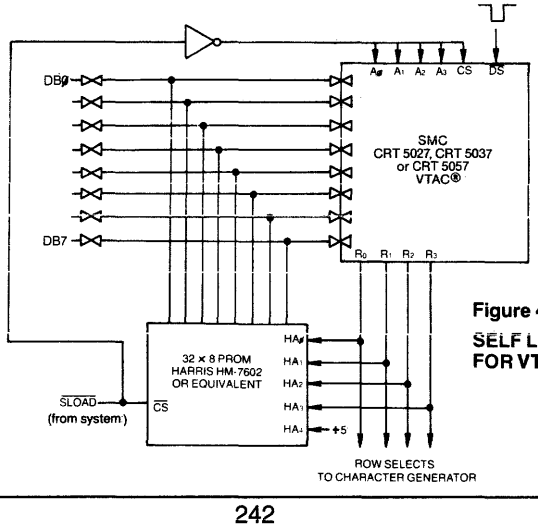


Figure 4.
SELF LOADING SCHEME FOR VTAC® SET-UP

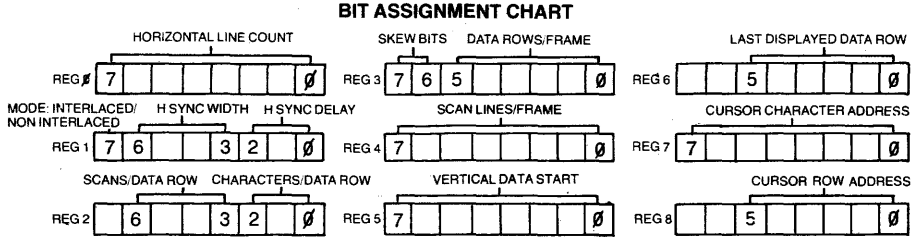
Register Selects/Command Codes

A3	A2	A1	AØ	Select/Command	Description
0	0	0	0	Load Control Register Ø	See Table 1
0	0	0	1	Load Control Register 1	
0	0	1	0	Load Control Register 2	
0	0	1	1	Load Control Register 3	
0	1	0	0	Load Control Register 4	
0	1	0	1	Load Control Register 5	
0	1	1	0	Load Control Register 6	
0	1	1	1	Processor Initiated Self Load	Command from processor instructing VTAC® to enter Self Load Mode (via external PROM)
1	0	0	0	Read Cursor Line Address	
1	0	0	1	Read Cursor Character Address	
1	0	1	0	Reset	Resets timing chain to top left of page. Reset is latched on chip by $\overline{DS}$ and counters are held until released by start command.
1	0	1	1	Up Scroll	Increments address of first displayed data row on page. ie; prior to receipt of scroll command—top line = 0, bottom line = 23. After receipt of Scroll Command—top line = 1, bottom line = 0.
1	1	0	0	Load Cursor Character Address*	
1	1	0	1	Load Cursor Line Address*	
1	1	1	0	Start Timing Chain	Receipt of this command after a Reset or Processor Self Load command will release the timing chain approximately one scan line later. In applications requiring synchronous operation of more than one CRT 5027 the dot counter carry should be held low during the $\overline{DS}$ for this command.
1	1	1	1	Non-Processor Self Load	Device will begin self load via PROM when $\overline{DS}$ goes low. The 1111 command should be maintained on A3-Ø long enough to guarantee self load. (Scan counter should cycle through at least once). Self load is automatically terminated and timing chain initiated when the all "1's" condition is removed, independent of $\overline{DS}$. For synchronous operation of more than one VTAC®, the Dot Counter Carry should be held low when the command is removed.

*NOTE: During Self-Load, the Cursor Character Address Register (REG 7) and the Cursor Row Address Register (REG 8) are enabled during states Ø111 and 1ØØØ of the R3-RØ Scan Counter outputs respectively. Therefore, Cursor data in the PROM should be stored at these addresses.

TABLE 1

BIT ASSIGNMENT CHART



AC TIMING DIAGRAMS

FIGURE 1 VIDEO TIMING

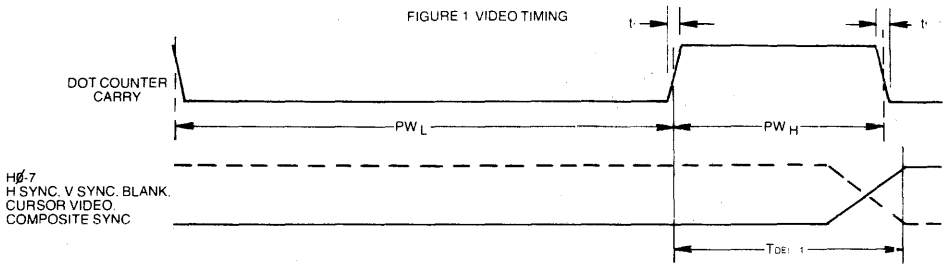


FIGURE 2 LOAD READ TIMING

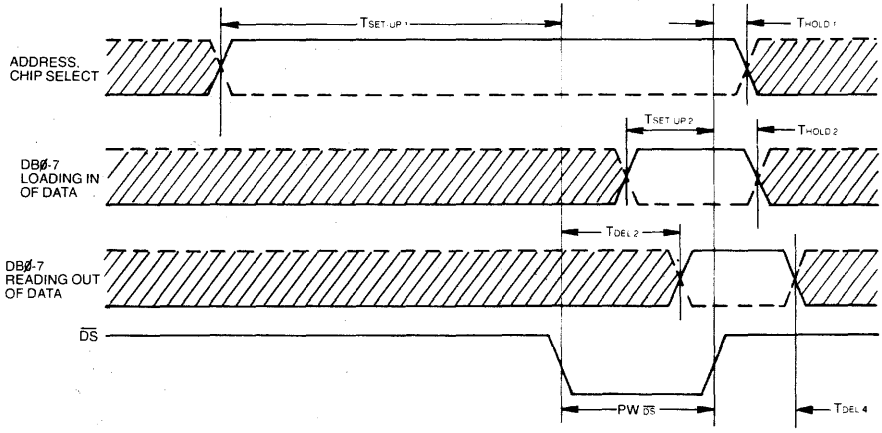
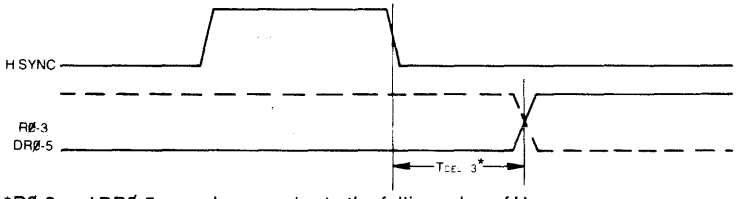
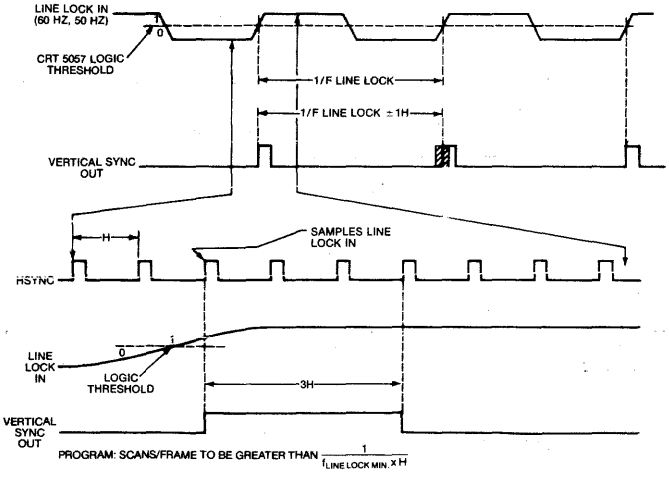


FIGURE 3 SCAN AND DATA ROW COUNTER TIMING



*RØ-3 and DRØ-5 may change prior to the falling edge of H sync

CRT 5057 LINE LOCK



Note: To ensure a stable display when using the line lock mode, the CRT 5057 should be used with DC coupled monitors only.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering, 10 sec.)	325°C
Positive Voltage on any Pin, with respect to ground	+18.0V
Negative Voltage on any Pin, with respect to ground	−0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, V_{DD}=+12V±5%, unless otherwise noted)

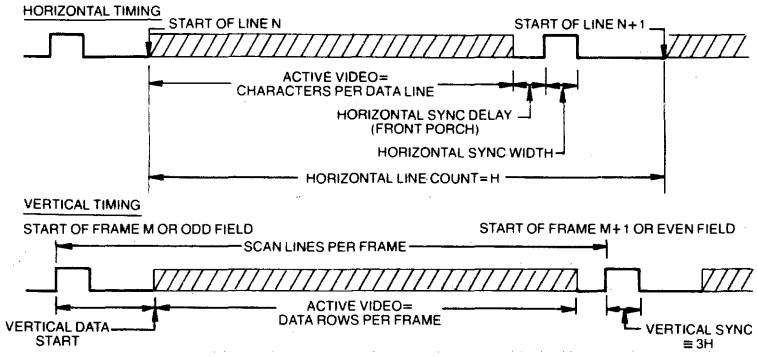
Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	V_{CC}−1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low Level—V_{OL} for RØ-3			0.4	V	I_{OL}=3.2ma
Low Level—V_{OL} all others			0.4	V	I_{OL}=1.6ma
High Level—V_{OH} for RØ-3, DBØ-7	2.4				I_{OH}=80μa
High Level—V_{OH} all others	2.4				I_{OH}=40μa
INPUT CURRENT					
Low Level, I_{IL} (Address, CS only)			250	μA	V_{IN}=0.4V
Leakage, I_{IL} (All Inputs except Address, CS)			10	μA	$0 \leq V_{IN} \leq V_{CC}$
INPUT CAPACITANCE					
Data Bus, C_{IN}		10	15	pF	
$\overline{DS}$, Clock, C_{IN}		25	40	pF	
All other, C_{IN}		10	15	pF	
DATA BUS LEAKAGE in INPUT MODE					
I_{DB}			10	μA	$0.4V \leq V_{IN} \leq 5.25V$
POWER SUPPLY CURRENT					
I_{CC}		80	100	mA	
I_{DD}		40	70	mA	
A.C. CHARACTERISTICS					T_A = 25°C
DOT COUNTER CARRY					
frequency	0.5		4.0	MHz	Figure 1
PW_H	35			ns	Figure 1
PW_L	215			ns	Figure 1
t_r, t_f		10	50	ns	Figure 1
DATA STROBE					
$PW_{\overline{DS}}$	150ns		10μs		Figure 2
ADDRESS, CHIP SELECT					
Set-up time	125			ns	Figure 2
Hold time	50			ns	Figure 2
DATA BUS—LOADING					
Set-up time	125			ns	Figure 2
Hold time	75			ns	Figure 2
DATA BUS—READING					
T_{DEL2}			125	ns	Figure 2, CL=50pF
T_{DEL4}	5		60	ns	Figure 2, CL=50pF
OUTPUTS: HØ-7, HS, VS, BL, CRV, CS-T_{DEL1}			125	ns	Figure 1, CL=20pF
OUTPUTS: RØ-3, DRØ-5					
T_{DEL3}	*		750	ns	Figure 3, CL=20pF

*RØ-3 and DRØ-5 may change prior to the falling edge of H sync

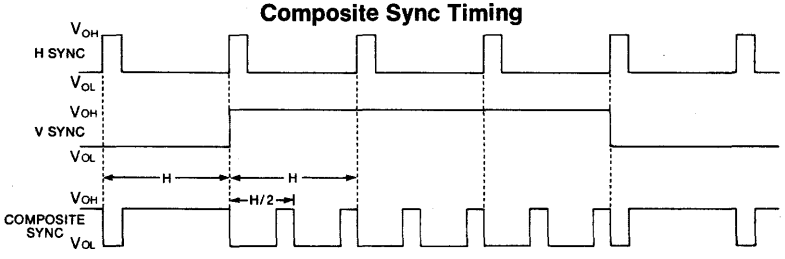
Restrictions

1. Only one pin is available for strobing data into the device via the data bus. The cursor X and Y coordinates are therefore loaded into the chip by presenting one set of addresses and outputed by presenting a different set of addresses. Therefore the standard WRITE and READ control signals from most microprocessors must be "NORed" externally to present a single strobe ($\overline{DS}$) signal to the device.
2. In interlaced mode the total number of character slots assigned to the horizontal scan must be even to insure that vertical sync occurs precisely between horizontal sync pulses.

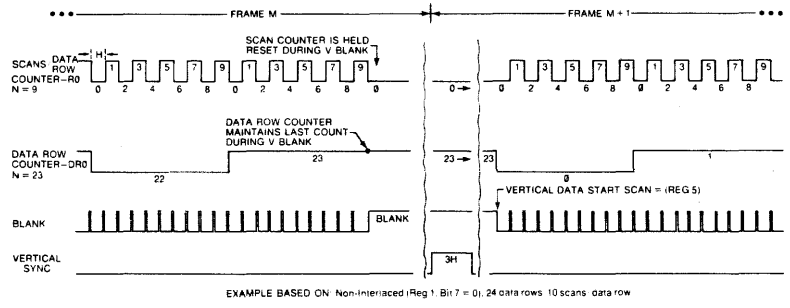
General Timing



Composite Sync Timing



Vertical Sync Timing



EXAMPLE BASED ON: Non-Interlaced (Reg 1, Bit 7 = 0), 24 data rows, 10 scans/data row

Start-up, CRT 5027

When employing microprocessor controlled loading of the CRT 5027's registers, the following sequence of instructions is necessary:

ADDRESS	COMMAND
1 1 1 0	Start Timing Chain
1 0 1 0	Reset
0 0 0 0	Load Register 0
.	.
.	.
.	.
0 1 1 0	Load Register 6
1 1 1 0	Start Timing Chain

The sequence of START RESET LOAD START is necessary to insure proper initialization of the registers.

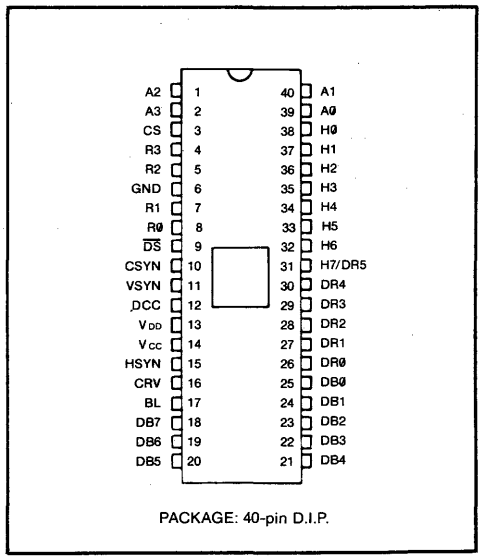
This sequence is not required if register loading is via either of the Self Load modes. This sequence is optional with the CRT 5037 or CRT 5057.

Preprogrammed CRT Video Timer and Controller VTAC®

FEATURES

- ☐ Preprogrammed (Mask-Programmed) Display Format
  - 80 Characters Per Data Row
  - 24 Data Rows Per Frame
  - 9 Scan Lines Per Data Row
- ☐ Preprogrammed Monitor Sync Format
  - 262 Scan Lines Per Frame
  - 6 Character Times for Horizontal Front Porch
  - 8 Character Times for Horizontal Sync Width
  - 6 Character Times for Horizontal Back Porch
  - 16 Scan Lines for Vertical Front Porch
  - 3 Scan Lines for Vertical Sync Width
  - 27 Scan Lines for Vertical Back Porch
  - Non-Interlace
  - 15.720KHz Horizontal Scan Rate
  - 60Hz Frame Refresh Rate
- ☐ Fixed Character Rate
  - 1.572MHz Character Rate (636.13ns/Character)
  - 11.004MHz Dot Rate (90.88ns/Dot) for 7 Dot Wide Character Block
- ☐ Character Format
  - 5 X 7 Character in a 7 X 9 Block
- ☐ Compatible with CRT 8002B-003 VDAC™
- ☐ Compatible with CRT 7004B-003
- ☐ May be mask-programmed with other display formats

PIN CONFIGURATION



PACKAGE: 40-pin D.I.P.

SECTION V

GENERAL DESCRIPTION

The two chip combination of SMC's CRT 5047 and CRT 8002B-003 effectively provide all of the video electronics for a CRT terminal. This chip set along with a μC form the basis for a minimum chip count CRT terminal.

The CRT 5047 Video Timer and Controller is a special version of the CRT 5037 VTAC® which has been ROM-programmed with a fixed format. It is especially effective for low-cost CRT terminals using an 80 X 24 display format with a 5 X 7 character matrix. The use of a fixed ROM program in the CRT 5047 eliminates the software overhead normally required to specify the display parameters and simplifies terminal software design.

The Cursor Character Address Register and the Cursor Row Address Register are the only two registers accessible by the processor. The CRT 5047 is easily initialized by the following sequence of commands:

Reset Load Control Register 6 Start Timing Chain

The parameters of the CRT 5047 have been selected to be compatible with most CRT monitors. The horizontal timing is programmed so that when the two character skew delay of the CRT 8002 VDAC™ is taken into account, the effective timing is: Horizontal Front Porch—four characters, and Horizontal Back Porch—eight characters.

Figure 1 shows the contents of the internal CRT 5047 registers. Other mask-programmed versions of the CRT 5037 are available. Consult SMC for more information.

VTAC® WORK SHEET

1. H CHARACTER MATRIX (No. of Dots): . 5
2. V CHARACTER MATRIX (No. of Horiz. Scan Lines): 7
3. H CHARACTER BLOCK (Step 1 + Desired Horiz. Spacing = No. in Dots): .. 7
4. V CHARACTER BLOCK (Step 2 + Desired Vertical Spacing = No. in Horiz. Scan Lines): 9
5. VERTICAL FRAME (REFRESH) RATE (Freq. in Hz): 60
6. DESIRED NO. OF DATA ROWS: 24
7. TOTAL NO. OF ACTIVE "VIDEO DISPLAY" SCAN LINES (Step 4 x Step 6 = No. in Horiz. Scan Lines): 216
8. VERT. SYNC DELAY (No. in Horiz. Scan Lines): 16
9. VERT. SYNC (No. in Horiz. Scan Lines; T= 190.8 μs*): 3
10. VERT. SCAN DELAY (No. in Horiz. Scan Lines; T= 1.718 ms*): 27
11. TOTAL VERTICAL FRAME (Add steps 7 thru 10 = No. in Horiz. Scan Lines): ... 262
12. HORIZONTAL SCAN LINE RATE (Step 5 x Step 11 = Freq. in KHz): 15.720
13. DESIRED NO. OF CHARACTERS PER HORIZ. ROW: 80
14. HORIZ. SYNC DELAY (No. in Character Time Units; T = 3.817 μs**): 6
15. HORIZ. SYNC (No. in Character Time Units; T = 5.090 μs**): 8
16. HORIZ. SCAN DELAY (No. in Character Time Units; T = 3.817 μs**): 6
17. TOTAL CHARACTER TIME UNITS IN (1) HORIZ. SCAN LINE (Add Steps 13 thru 16): 100
18. CHARACTER RATE (Step 12 x Step 17 = Freq. in MHz): 1.572
19. CLOCK (DOT) RATE (Step 3 x Step 18 = Freq. in MHz): 11.004

*Vertical Interval **Horizontal Interval

REG. #	ADDRESS A3 A0	FUNCTION	BIT ASSIGNMENT	HEX.	DEC.
0	0000	HORIZ. LINE COUNT 100	0 1 1 0 0 0 1 1	63	99
1	0001	INTERLACE 0 H SYNC WIDTH 8 H SYNC DELAY 6	0 1 0 0 0 1 1 0	46	70
2	0010	SCANS/DATA ROW 9 CHARACTERS/ROW 80	X 1 0 0 0 1 0 1	45	69
3	0011	SKEW CHARACTERS 0,0 DATA ROWS 24	0 0 0 1 0 1 1 1	17	23
4	0100	SCANS/FRAME 262 X = 3	0 0 0 0 0 0 1 1	03	03
5	0101	VERTICAL DATA START = 3 + VERTICAL SCAN DELAY: SCAN DELAY 27 DATA START 30	0 0 0 1 1 1 1 0	1E	30
6*	0110	LAST DISPLAYED DATA ROW (= DATA ROWS)	X X	–	–

*Register 6 has an initialization option. It is loaded with the data contained in Register 3 by a "Load Register 6" command. The "Up Scroll" command can be used to effect scrolling operations.

Figure 1: CRT 5047 Mask Programmed Registers

STANDARD MICROSYSTEMS CORPORATION

CRT 7220
CRT 7220-1
CRT 7220-2

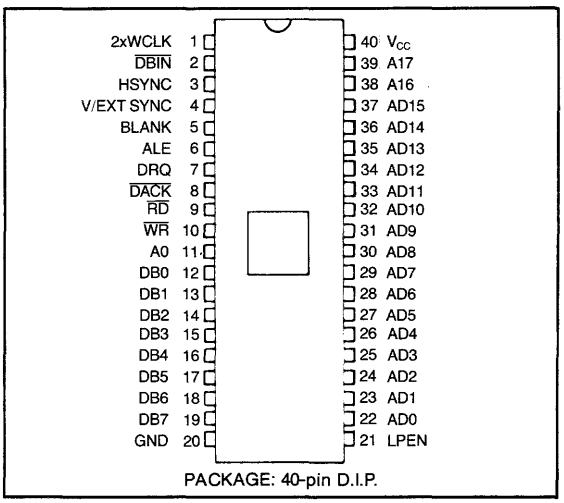
PRELIMINARY

Graphics Display Controller

FEATURES

- ☐ Microprocesser Interface
  - DMA transfers with 8257- or 8237-type controllers
  - FIFO Command Buffering
- ☐ Display Memory Interface
  - Up to 256K words of 16 bits
  - Read-Modify-Write (RMW) Display Memory cycles in under 800ns
  - Dynamic RAM refresh cycles for nonaccessed memory
- ☐ Light Pen Input
- ☐ External video synchronization mode
- ☐ Graphics Mode
  - Four megabit, bit-mapped display memory
- ☐ Character Mode
  - 8K character code and attributes display memory
- ☐ Mixed Graphics and Character Mode
  - 64K if all characters
  - 1 megapixel if all graphics
- ☐ Graphics Capabilities
  - Figure drawing of lines, arc/circles, rectangles, and graphics characters in 800ns per pixel
  - Display 1024-by-1024 pixels with 4 planes of color or grayscale
  - Two independently scrollable areas
- ☐ Character Capabilities
  - Auto cursor advance
  - Four independently scrollable areas
  - Programmable cursor height
  - Characters per row: up to 256
  - Character rows per screen: up to 100

PIN CONFIGURATION



PACKAGE: 40-pin D.I.P.

- ☐ Video Display Format
  - Zoom magnification factors of 1 to 16
  - Panning
  - Command-settable video raster parameters
- ☐ Technology
- ☐ Single +5 volt Power Supply
- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ DMA Capability
  - Bytes or word transfers
  - 4 clock periods per byte transferred

SECTION V

GENERAL DESCRIPTION

The CRT 7220 Graphics Display Controller (GDC) is an intelligent microprocessor peripheral designed to be the heart of a high-performance raster-scan computer graphics and character display system. Positioned between the video display memory and the microprocessor bus, the GDC performs the tasks needed to generate the raster display and manage the display memory. Processor software overhead is minimized by the GDC's sophisticated instruction set, graphics figure drawing, and DMA transfer capabilities. The display memory supported by the GDC can be configured in any number of formats and sizes up to 256K 16-bit words. The display can be zoomed and panned, while partitioned screen areas can be independently scrolled. With its light pen input and multiple controller capability, the GDC is ideal for advanced computer graphics applications.

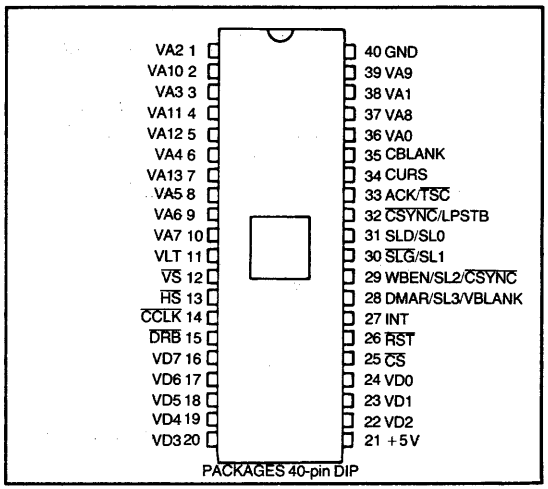
The GDC is designed to work with a general purpose microprocessor to implement a high-performance computer graphics system. Through the division of labor established by the GDC's design, each of the system components is used to the maximum extent through a six-level hierarchy of simultaneous tasks. At the lowest level, the GDC generates the basic video raster timing, including sync and blanking signals. Partitioned areas on the screen and zooming are also accomplished at this level. At the next level, video display memory is modified during the figure drawing operations and data moves. Third, display memory addresses are calculated pixel by pixel as drawing progresses. Outside the GDC at the next level, preliminary calculations are done to prepare drawing parameters. At the fifth level, the picture must be represented as a list of graphics figures drawable by the GDC. Finally, this representation must be manipulated, stored, and communicated. By handling the first three levels, the GDC takes care of the high-speed and repetitive tasks required to implement a graphics system.

CRT Video Processor and Controller
VPAC™

FEATURES

- ☐ Fully Programmable Display Format
  - Characters per Data Row (8-240)
  - Data Rows per Frame (2-256)
  - Raster Scans per Data Row (1-32)
- ☐ Programmable Monitor Sync Format
  - Raster Scans/Frame (4-2048)
  - Front Porch—Horizontal (Negative or Positive)
  - —Vertical
  - Sync Width—Horizontal (1-128 Character Times)
  - —Vertical (2-256 Scan Lines)
  - Back Porch—Horizontal
  - —Vertical
- ☐ Direct Outputs to CRT Monitor
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync
  - Composite Blanking
  - Cursor Coincidence
- ☐ Binary Addressing of Video Memory
- ☐ Row-Table Driven or Sequential Video Addressing Modes
- ☐ Programmable Status Row Position and Address Registers
- ☐ Bidirectional Partial or Full Page Smooth Scroll
- ☐ Attribute Assemble Mode
- ☐ Double Height Data Row Mode
- ☐ Double Width Data Row Mode
- ☐ Programmable DMA Burst Mode
- ☐ Configurable with a Variety of Memory Contention Arrangements
- ☐ Light Pen Register
- ☐ Cursor Horizontal and Vertical Position Registers
- ☐ Maskable Processor Interrupt Line
- ☐ Internal Status Register
- ☐ Three-state Video Memory Address Bus
- ☐ Partial or Full Page Blank Capability
- ☐ Two Interlace Modes: Enhanced Video and Alternate Scan Line

PIN CONFIGURATION



PACKAGES 40-pin DIP

- ☐ Ability to Delay Cursor and Blanking with respect to Active Video
- ☐ Programmable for Horizontal Split Screen Applications
- ☐ Graphics Compatible
- ☐ Ability to Externally Sync each Raster Line, each Field
- ☐ Single +5 Volt Power Supply
- ☐ TTL Compatible on All Inputs and Outputs
- ☐ VT-100 Compatible
- ☐ RS-170 Interlaced Composite Sync Available

SECTION V

GENERAL DESCRIPTION

The CRT 9007 VPAC™ is a next generation video processor/controller—an MOS LSI integrated circuit which supports either sequential or row-table driven memory addressing modes. As indicated by the features above, the VPAC™ provides the user with a wide range of programmable features permitting low cost implementation of high performance CRT systems. Its 14 address lines can directly address up to 16K of video memory. This is equivalent to eight pages of an 80 character by 24 line CRT display. Smooth or jump scroll operations may be performed anywhere within the addressable memory. In addition, status rows can be defined anywhere on the screen.

In the sequential video addressing mode, a Table Start Register points to the address of the first character of the first data row on the screen. It can be easily changed to produce a scrolling effect on the screen. By using this register in conjunction with two auxiliary address registers and two sequential break registers, a screen roll can be produced with a stable status row held at either the first or last data row position.

In the row-table driven video addressing mode, each row in the video display is designated by its own address. This provides the user with greater flexibility than sequential addressing since the rows of characters are linked by pointers instead of residing in sequential memory locations. Operations such as data row insertion, deletion, and replication are easily accomplished by manipulating pointers instead of entire lines. The row table itself can be stored in memory in a linked list or in a contiguous format.

The VPAC™ works with a variety of memory contention schemes including operation with a Single Row Buffer such as the CRT 9006, a Double Row Buffer such as the CRT 9212, or no buffer at all, in which case character addresses are output during each displayable scan line.

User accessable internal registers provide such features as light pen, interrupt enabling, cursor addressing, and VPAC™ status. Ten of these registers are used for screen formatting with the ability to define over 200 characters per data row and up to 256 data rows per frame. These 10 registers contain the "vital screen parameters".

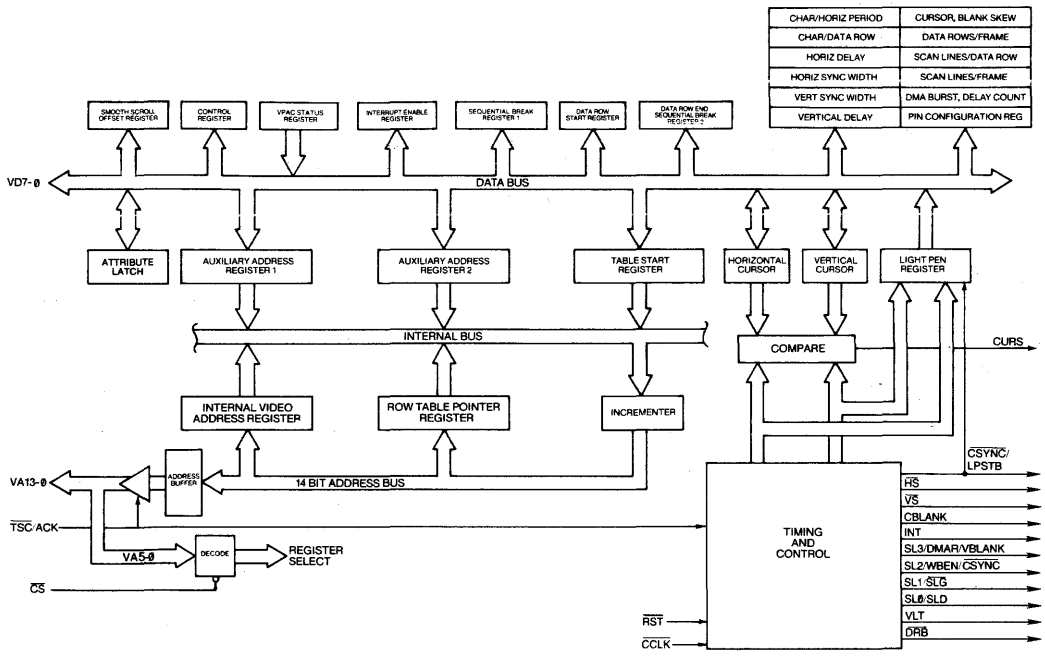


FIGURE 1: CRT 9007 BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PROCESSOR INTERFACE:

PIN NO.	NAME	SYMBOL	FUNCTION
7, 5, 4, 2, 39, 37, 10, 9, 8, 6, 3, 1, 38, 36	Video Address 13-0	VA13-VA0	These 14 signals are the binary address presented to the video memory by the CRT 9007. The function depends on the particular CRT 9007 mode of operation. VA13-6 are outputs only. VA5-0 are bidirectional. —Double Row Buffer Configuration: VA13-0 are active outputs for the DMA operations and are in their high impedance state at all other times. —Single Row Buffer Configuration: VA13-0 are active outputs during the first scan line of each data row and are in their high impedance state at all other times. —Repetitive Memory Addressing Configuration: VA13-0 are active outputs at all times except during horizontal and vertical retrace at which time they are in their high impedance state. If row table addressing is used for either single row buffer or repetitive memory addressing modes, VA13-0 are active outputs during the horizontal retrace at each data row boundary to allow the CRT 9007 to retrieve the row table address. For processor read/write operations VA5-0 are inputs that select the appropriate internal register.
16, 17, 18, 19, 20, 22, 23, 24	Video Data 7-0	VD7-VD0	Bidirectional video data bus: during processor Read/write operations data is transferred via VD7-VD0 when chip strobe ($\overline{CS}$) is active. These lines are in their high impedance state when $\overline{CS}$ is inactive. During CRT 9007 DMA operations, data from video memory is input via VD7-VD0 when a new row table address is being retrieved or when the attribute latch is being updated in the attribute assemble mode. VD7-VD0 are outputs when the external row buffer is updated with a new attribute in the attribute assemble mode.
25	Chip strobe	$\overline{CS}$	Input; this signal when active low, allows the processor to read or write internal CRT 9007 registers. When reading from an internal CRT 9007 register, the chip strobe ($\overline{CS}$) enables the output drivers. When writing to an internal CRT 9007 register, the trailing edge of this signal latches the incoming data. Figure 2 shows all processor read/write timing.
26	Reset	$\overline{RST}$	Input; this active low signal puts the CRT 9007 into a known, inactive state and insures that the horizontal sync ($\overline{HS}$) output is inactive. Activating this input has the same effect as a RESET command. After initialization, a START command causes normal CRT 9007 operation. See processor addressable registers section, Register 16 for the reset state definition.
27	Interrupt	INT	Output; an interrupt to the processor from the CRT 9007 occurs when this signal is active high. The interrupt returns to its inactive low state when the status register is read.

DESCRIPTION OF PIN FUNCTIONS CONT'D

CRT INTERFACE:

PIN NO.	NAME	SYMBOL	FUNCTION
11	Visible Line Time	VLT	Output; this signal is active high during all visible scan lines and during the horizontal trace times at vertical retrace. This signal can be used to gate the character clock ($\overline{CCLK}$) when supplying data to a character generator from a single or double row buffer.
12	Vertical Sync	$\overline{VS}$	Open drain output; this signal determines the vertical position of displayed text by initiating a vertical retrace. Its position and pulse width are user programmable. The open drain allows the vertical frame rate to be synchronized to the line frequency when using monitors with DC coupled vertical amplifiers. If the $\overline{VS}$ output is pulled active low externally before the CRT 9007 itself initiates a vertical sync, the CRT 9007 will start its own vertical sync at the next leading edge of horizontal sync ($\overline{HS}$).
13	Horizontal Sync	$\overline{HS}$	Open drain output; this signal determines the horizontal position of displayed text by initiating a horizontal retrace. Its position and pulse width are user programmable. During hardware and software reset, this signal is inactive high. The open drain allows the horizontal scan rate to be synchronized to an external source. If the $\overline{HS}$ output is pulled low externally before the CRT 9007 itself initiates a horizontal sync, the CRT 9007 will start its own horizontal sync on the next character clock ($\overline{CCLK}$).
14	Character Clock	$\overline{CCLK}$	Input; this signal defines the character rate of the screen and is used by the CRT 9007 for all internal timing. A minimum high voltage of 4.3V must be maintained for proper chip operation.
15	Data Row Boundary	$\overline{DRB}$	Output: this signal is active low for one full scan line (from VLT trailing edge to VLT trailing edge) at the top scan line of each new data row. This signal can be used to swap buffers in the double row buffer mode. It indicates the particular horizontal retrace time that the CRT 9007 outputs addresses (VA13-VA0) for single row buffer operation. There will always be one extra $\overline{DRB}$ signal which will become active during the first scan line of the vertical retrace interval.
34	Cursor	CURS	Output; this signal marks the cursor position on the screen as specified by the horizontal and vertical cursor registers. The signal is active for one character time at the particular character position for all scan lines within the data row. For double height or width characters, this signal is active for 2 consecutive $\overline{CCLK}$'s in every scan line within the data row. For double height characters, this signal can be programmed to be active at the proper position for 2 consecutive data rows. CURS is also used to signal either a double height or double width data row by becoming active during the horizontal retrace (CBLANK active) prior to a double height or double width scan line. The time of activation and deactivation is a function of the addressing mode, buffer configuration and the scan line number. See section of Double height/width for details.
35	Composite Blank	CBLANK	Output. This signal when active high, indicates that a retrace (either horizontal or vertical) will be performed. The signal remains active for the entire retrace interval as programmed. It is used to blank the video to a CRT.

USER SELECTABLE PINS: (see Tables 4 and 5)

PIN NO.	NAME	SYMBOL	FUNCTION
28, 29, 30, 31	Scan Line 3-Scan Line 0	SL3-SL0	Output; these 4 signals are the direct scan line counter outputs, in binary form, that indicate to the character generator the current scan line. These signals continue to be updated during the vertical retrace interval. SL3 and SLØ are the most and least significant bits respectively.
28	Direct Memory Access Request	DMAR	Output; this signal is the DMA request issued by the CRT 9007. It will only become active if the acknowledge (ACK) input is inactive. It remains active high throughout the entire DMA operation.
28	Vertical Blank	VBLANK	Output; this signal is active high only during the vertical retrace period.
29	Write Buffer Enable	WBEN	Output; this active high signal is used to gate the clock feeding the write buffer in a double row buffer configuration.
29 or 32	Composite Sync	$\overline{CSYNC}$	Output; this signal provides a true RS-170 composite sync waveform with equalization pulses and vertical serrations in both interlace and noninterlace formats. Figure 3 illustrates the $\overline{CSYNC}$ output in both interlaced and noninterlaced formats.
30	Scan Line Gate	$\overline{SLG}$	Output; this active low signal is used as a clock gate. It captures the correct 5 or 6 $\overline{CCLK}$'s and, in conjunction with $\overline{SLD}$ (pin 31), allows scan line information to be loaded serially into an external shift register.
31	Scan Line Data	SLD	Output; this signal allows one to load an external shift register with the current scan line count. The count is presented least significant to most significant bit during the 5 or 6 $\overline{CCLK}$'s framed by $\overline{SLG}$. With this form of scan line representation, it is possible to define up to 32 scan lines per data row. The external shift register must be at least 5 bits in length. Even though 6 shifts can occur one should only use the 5 last bits shifted to define the scan line count. The extra shift occurs in interlace or double height character mode to allow the scan line count to be adjusted to its proper value. Figures 4 and 5 illustrate the serial scan line timing.
32	Light Pen Strobe	LPSTB	Input; this signal strobes the current row/column position into the light pen register at its positive transition.
33	Acknowledge	ACK	Input; this active high signal acknowledges a DMA request. It indicates that the processor bus has entered its high impedance state and the CRT 9007 may access video memory. It is not recommended to deactivate this signal during a CRT 9007 DMA cycle because the CRT 9007 will not shut down in a predictable amount of time.
33	Three State Control	$\overline{TSC}$	Input; this signal, when active low, places VA13-VAØ in their high impedance state.

Single Row Buffer Operation

The CRT 9007 configured with a CRT 9006 Single Row Buffer is shown in figure 6. The use of the CRT 9006 Single Row Buffer requires that the buffer be loaded at the video painting rate during the top scan line of each data row. However, after the CRT 9006 is loaded, the CRT 9007 address lines enter their high impedance state for the remaining N-1 scan lines of the data row, thereby permitting full processor access to memory during these scan lines. The percentage of total memory cycles available to the processor is approximately $[(N-1)/N] \times 100$ where N is the total number of scan lines per data row. For a typical system with 12 scan lines per data row this percentage is 92%. Figure 7 illustrates typical timing for the CRT 9007 used with the CRT 9006 Single Row Buffer.

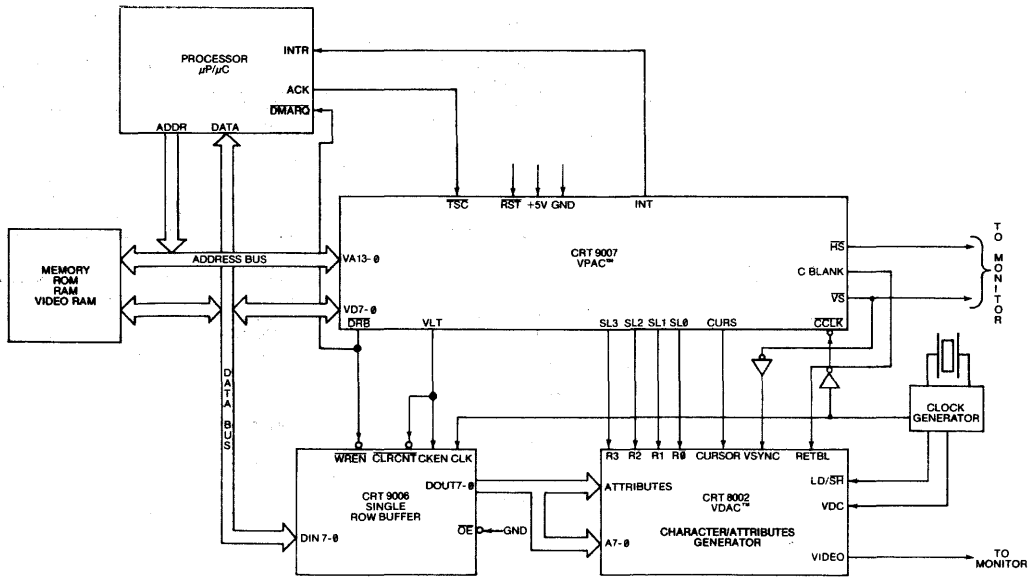


FIGURE 6: CRT 9007 CONFIGURATION WITH SINGLE ROW BUFFER

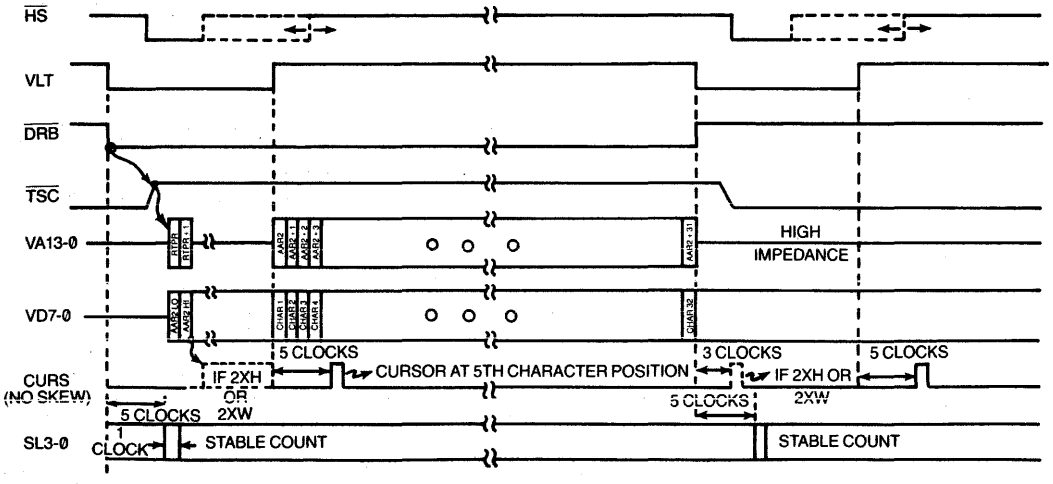


FIGURE 7: CRT 9007 SINGLE ROW BUFFER TIMING (32 CHARACTERS PER DATA ROW)

Double Row Buffer Operation

Figure 8 shows the CRT 9007 used in conjunction with a CRT 9212 Double Row Buffer. The Double Row Buffer has a read buffer which is read at the painting rate of the CRT during each scan line in the data row. While the read buffer is being read and supplying data to the character generator for the current displayed data row, the write buffer is being loaded with the next data row to be displayed. This arrangement allows for relaxed write timing to the write buffer as it may be filled in the time it takes for N scan lines on the CRT to be painted where N is the number of scan lines per data row. Used in this configuration, the CRT 9007 takes advantage of the relaxed write buffer timing by stealing memory cycles from the processor to fill the write buffer (Direct memory access operation). The CRT 9007 sends the DMAR (DMA request) signal, awaits an ACK (acknowledge) signal and then drives out on VA13-VA0 the address at which the next video data resides. The CRT 9007 then activates the WBEN (write buffer enable) signal to write the data into the buffer. If for example there are 80 characters per data row, the CRT 9007 performs 80 DMA operations. The user has the ability to program the number of DMA cycles performed during each DMAR-ACK sequence, as well as the delay between each DMAR-ACK sequence, via the DMA CONTROL REGISTER (RA). If 8 DMA operations are performed for each ACK received, 10 such DMAR-ACK sequences must be performed to completely fill the write buffer. The programmed delay allows the user to evenly distribute the DMA operations so as not to hold up the processor for an excessive length of time. This feature also permits other DMA devices to be used and allows the processor to respond to real time events. In addition, the user has the ability to disable the CRT 9007 DMA mechanism. Figure 9 illustrates typical timing for the CRT 9007 used with the CRT 9212 Double Row Buffer.

Since the CRT 9212 Double Row Buffer has separate inputs for read and write clocks (RCLK, WCLK), it is possible to display proportional character widths (variable number of dots per character) by reading out the buffer at a character clock rate determined by the particular character. The writing of the buffer can be clocked from a different and constant character clock. Figure 10 illustrates the CRT 9007 used with two double row buffers and a CRT 9021 Video Attributes Controller chip to provide proportional character display.

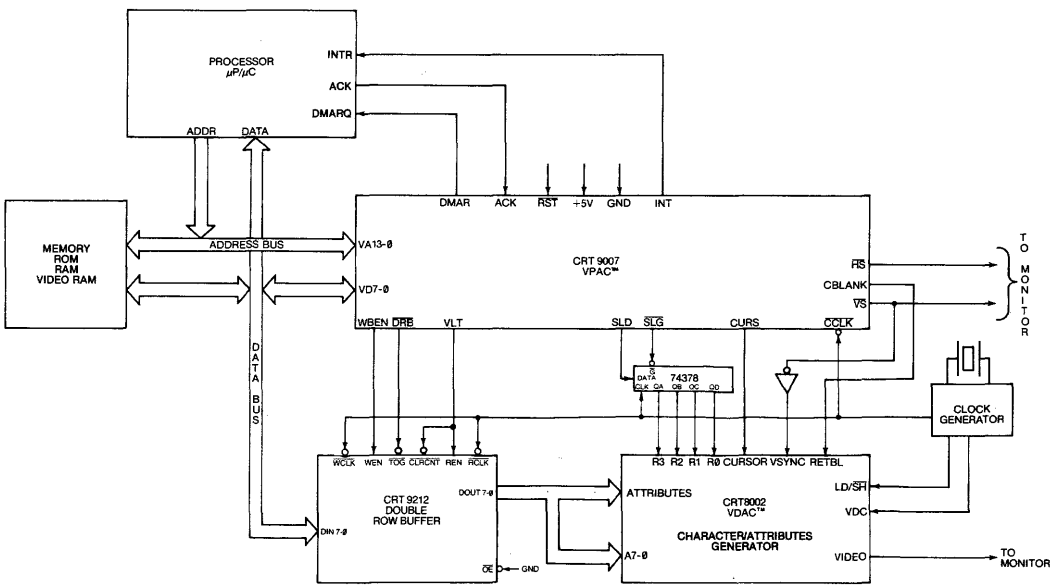


FIGURE 8: CRT 9007 CONFIGURATION WITH DOUBLE ROW BUFFER

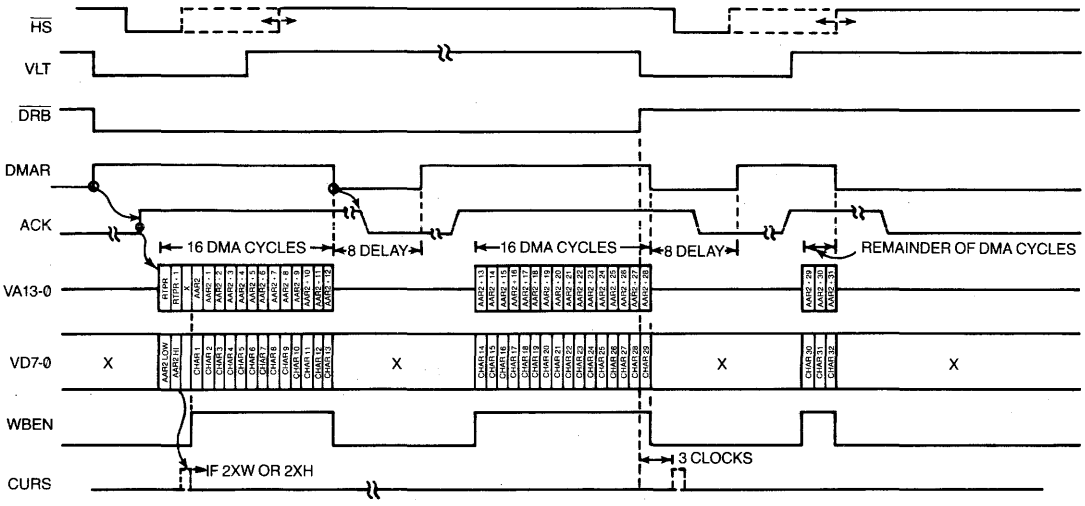


FIGURE 9: CRT 9007 DOUBLE ROW BUFFER TIMING (32 CHARACTERS PER DATA ROW)

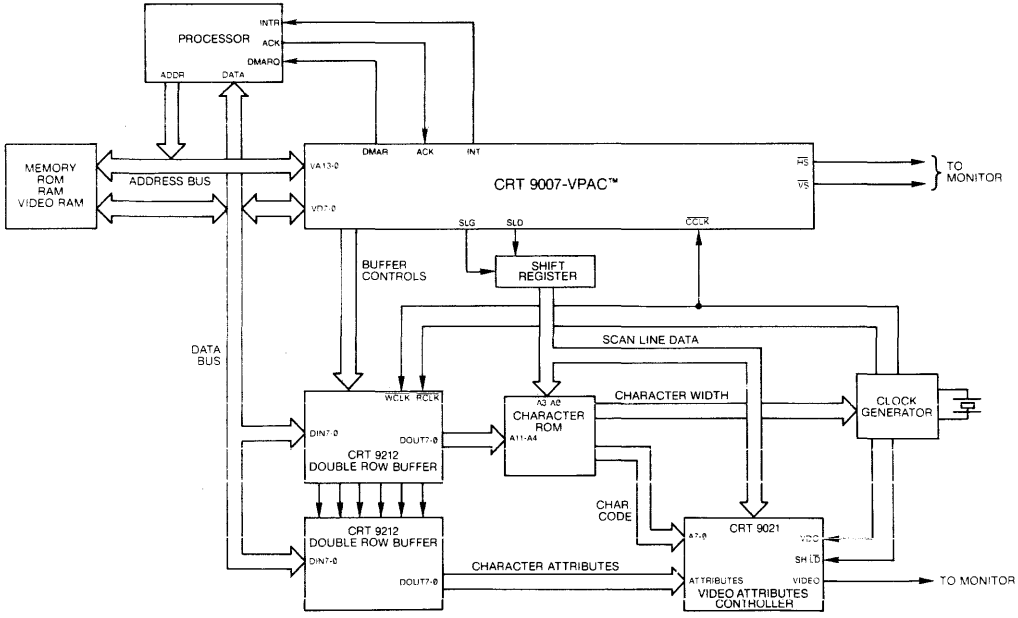


FIGURE 10: CRT 9007 CONFIGURATION FOR PROPORTIONAL CHARACTER DISPLAY

Repetitive Memory Addressing Operation

In this operation mode, the CRT 9007 will repeat the sequence of video addresses for every scan line of every data row. The CRT 9007 address bus will enter its high impedance state during all horizontal retrace intervals (except the retrace interval at a data row boundary if the CRT 9007 is configured in a row driven addressing mode). This arrangement allows for such low end contention schemes as retrace intervention (the processor is only allowed access to video memory during retrace intervals) and processor priority (the processor has an unlimited access to video memory). A high end contention scheme can be employed which uses a double speed memory such that in a single character period both the processor and the CRT 9007 are permitted access to video memory at predetermined time slots. Figure 11 illustrates the CRT 9007 configured with a double speed memory. Typical timing for this mode is illustrated in figure 12.

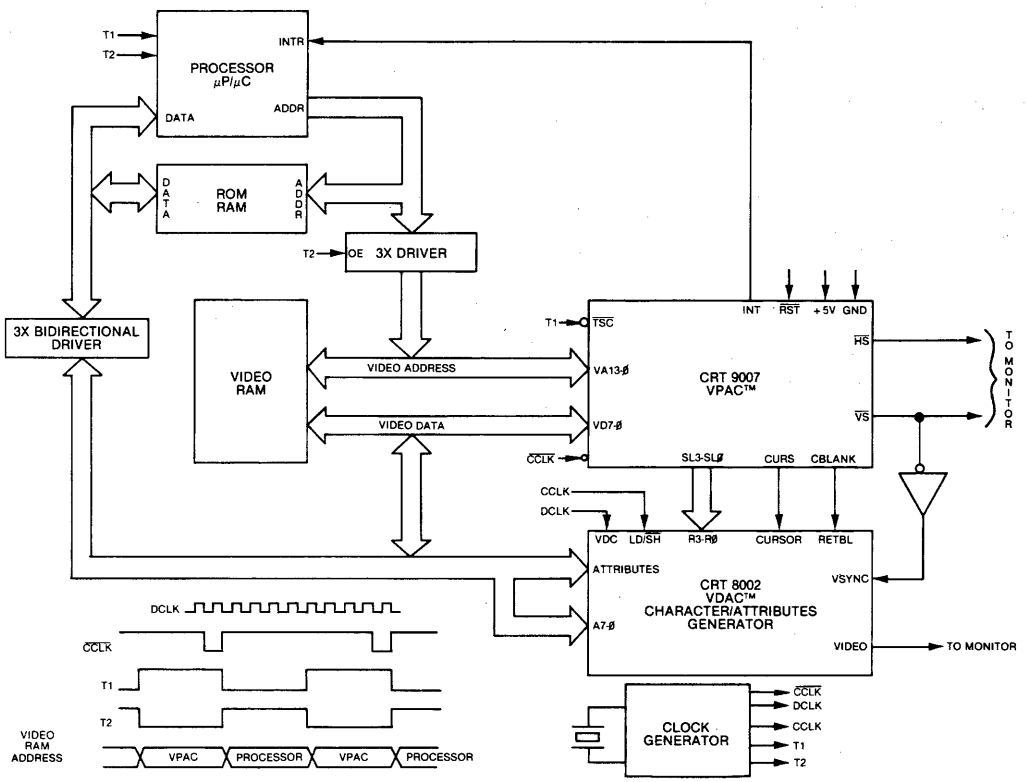


FIGURE 11: CRT 9007 CONFIGURATION WITH DOUBLE SPEED MEMORY

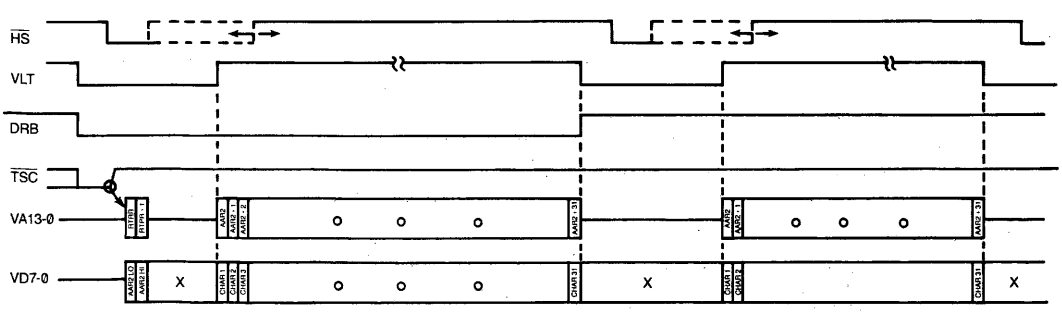


FIGURE 12: CRT 9007 REPETITIVE MEMORY ADDRESS TIMING (32 CHARACTERS PER DATA ROW)

Attribute Assemble Operation

This configuration allows the user to retain an 8 bit wide video memory in which attributes occupy memory locations but not positions on the CRT. This mode assumes that every other display position in video memory contains an attribute. During one clock cycle, attribute data is latched into the CRT 9007; during the next clock cycle a character location is addressed. The attribute data is driven out along with a WBEN signal allowing the character plus its associated attribute to be written simultaneously to two 8 bit double row buffers. Figure 13 illustrates the memory organization used for the Attribute Assemble mode. The first entry in each data row must begin with an attribute.

Figure 14 shows the CRT 9007 configured in the Attribute Assemble mode used with two CRT 9212 Double Row Buffers and 8, 16Kx1 dynamic RAMS. This mode, since it retains an 8 bit wide memory while providing all the advantages of a 16 bit wide memory, lends itself to some cost effective designs using dynamic RAMS. The CRT 9007 will refresh dynamic RAMS because twice the number of the programmed characters per data row are accessed sequentially for each data row.* Figure 15 illustrates typical timing of the CRT 9007 used in the Attribute Assemble mode.

Memory Address (typ)	Memory Data (8 bits)
0D00	Attribute 0
0D01	Character 0
0D02	Attribute 1
0D03	Character 1
0 0 0	0 0 0
2N	Attribute N
2N + 1	Character N

Figure 13: Attribute Assemble Memory Organization

*Note: For 50 Hz operation there usually is about 3 milliseconds extra vertical blanking where refreshing might fail. In this situation the CRT 9007 can be programmed with about 5 more "dummy" data rows while extending the vertical blank signal. This allows the CRT 9007 to start addressing video memory much earlier within the vertical blanking interval and hence provide refresh to the dynamic RAMS. When displaying double height or double width data rows, only half as many sequential locations are accessed each data row and dynamic RAM refresh might fail.

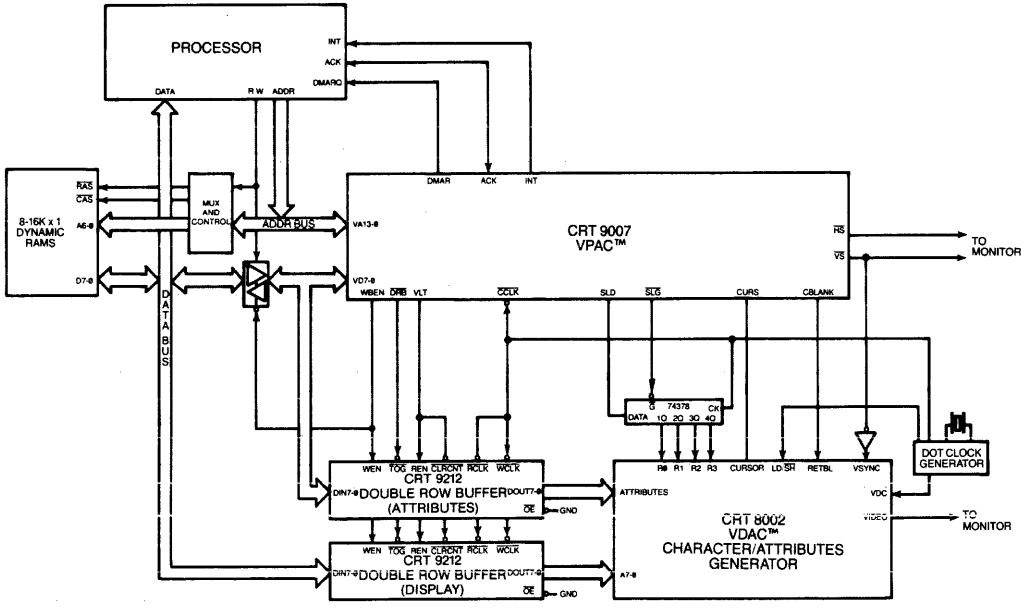
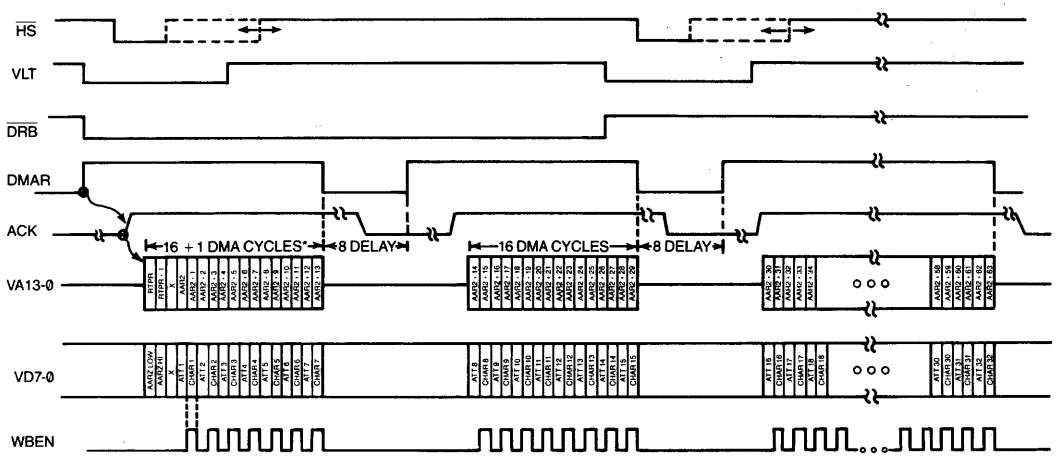


FIGURE 14: CRT 9007 CONFIGURATION FOR ATTRIBUTE ASSEMBLE MODE

Smooth Scroll Operation

Smooth scroll requires that all or a portion of the screen move up or down an integral number of scan lines at a time. 2 user programmable registers allow one to define the "start data row" and the "end data row" for the smooth scroll operation. A SMOOTH SCROLL OFFSET REGISTER (R17), when used in conjunction with a CRT 9007 vertically timed interrupt, allows the user to synchronize the update of the offset register to the vertical frame rate. The offset register causes the scan line counter outputs of the CRT 9007 to start at the programmed offset value rather than zero for the data row that starts the smooth scroll interval. To allow complete flexibility in smooth scroll direction and rate, one can update the offset register in the positive as well as negative direction and can also offset any number of scan lines each frame. Since a smooth scroll can momentarily result in a partial data row consisting of one scan line, the loading of the write buffer under DMA operations for the start and end data row of the smooth scroll operation is forced to occur in one scan line. This condition overrides the programmable DMA CONTROL REGISTER (RA).



*DMA cycles will always end at a character fetch

FIGURE 15: CRT 9007 ATTRIBUTE ASSEMBLE TIMING (32 CHARACTERS PER DATA ROW)

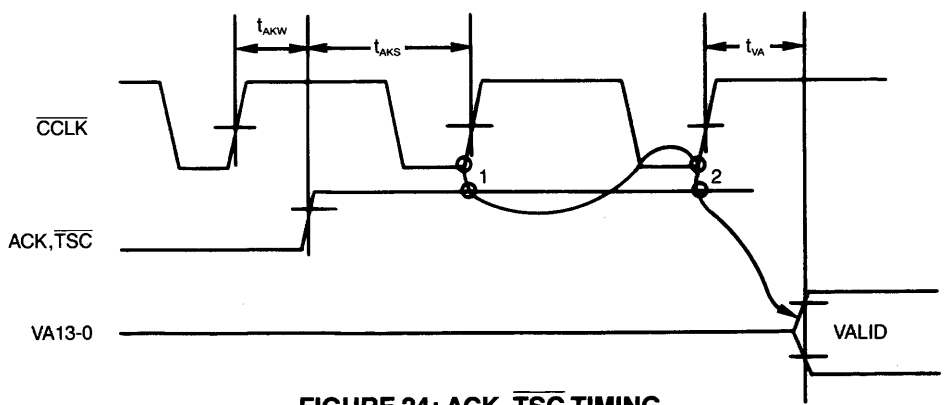


FIGURE 24: ACK, $\overline{TSC}$ TIMING

Row Table Addressing

In this addressing mode, each data row in video memory is designated by its own starting address. This provides greater flexibility with respect to screen operations than with other addressing schemes used by previous CRT controllers. The row table, which is a list of starting addresses for each data row, can be configured in one of 2 ways. The choice of row table format is highly dependent upon the particular application and the programmer's preference since each format allows full utilization of the CRT 9007 features.

Contiguous Row Table Format

In this format, the TABLE START REGISTER (RC and RD) points to the address where the row table begins. The contents of the first 2 locations define the starting address of the first data row. These 2 bytes define a 14 bit address where the first byte is the low order 8 bits and the second byte is the high order 6 bits. The 2 most significant bits of the second byte define double height/width characteristics to the current data row. The contents of the third and fourth locations define the address where the second data row begins. Figure 16 illustrates the contiguous row table organization in video memory.

Linked List Row Table Format

In this format the TABLE START REGISTER (RC and RD) points to the memory location which starts the entire addressing sequence into operation. The first byte read is the lower 8 bits and the second byte read is the upper 6 bits of the next data row's start address. The 2 most significant bits of the second byte define double height/width characteristics for the data row about to be read. The third, fourth, fifth, etc., bytes read are the first, second, third, etc., characters of the current data row. Figure 17 illustrates the linked list row table organization in video memory.

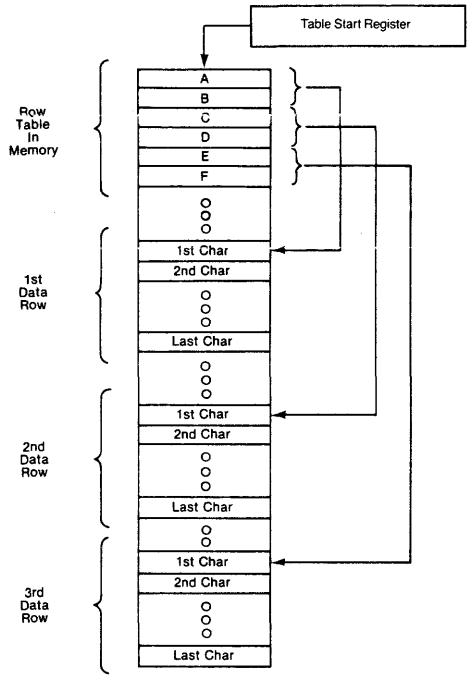


FIGURE 16: CONTIGUOUS ROW TABLE ADDRESS FORMAT

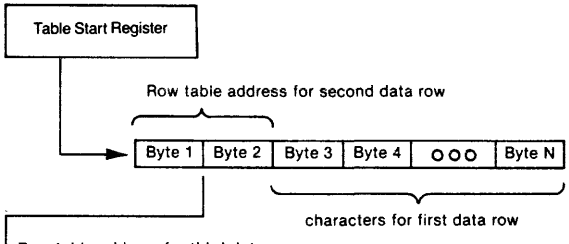


FIGURE 17: LINKED LIST ROW TABLE ADDRESS FORMAT

Sequential Addressing[1]

In this addressing mode, characters on the display screen are located in successive memory locations. The TABLE START REGISTER (RC and RD) points to the address of the first character of the first data row on the screen. In this mode the TABLE START REGISTER does not point to the start of a table but the start of the screen. As each character is read by the CRT 9007 for display refresh, the internal video address register is incremented by one to access the next character.

For more versatile systems operation in the sequential addressing mode, SEQUENTIAL BREAK REGISTER 1 (R10) and SEQUENTIAL BREAK REGISTER 2 (R12) may be used to define the data rows at which two additional

[1]SEQUENTIAL BREAK 2 is not functional in the repetitive memory addressing mode. It is fully functional in all other operation modes.

sequential display areas begin. Note that DATA ROW END REGISTER (R12) is defined as SEQUENTIAL BREAK REGISTER 2 (R12) for the sequential addressing mode only. The starting addresses for these two additional display areas are defined by AUXILIARY ADDRESS REGISTER 1 (RE and RF) and AUXILIARY ADDRESS REGISTER 2 (R13 and R14). When the raster begins painting a data row equal to the number programmed in one of the sequential break registers, the CRT 9007 addresses the video memory sequentially starting with the address specified by the corresponding auxiliary address register. Figure 18 illustrates a display with 80 characters per data row having sequential breaks at data rows 3 and 6.

Using the sequential addressing mode with 2 breaks, it is possible to roll a portion of the screen and keep the rest of the screen stable. Double height/width characteristics can be attached to the 2 sequentially addressed screens defined by SEQUENTIAL BREAK REGISTERS 1 and 2 by using the 2 most significant bits of AUXILIARY ADDRESS REGISTERS 1 and 2. See the description of these 2 registers for their bit definition.

TABLE START REGISTER = 1000
AUXILIARY ADDRESS REGISTER 1 = 2000
AUXILIARY ADDRESS REGISTER 2 = 0800
SEQUENTIAL BREAK REGISTER 1 = 3
SEQUENTIAL BREAK REGISTER 2 = 6

Data Row	Address range	
Ø	1000 to 104 F	
1	1050 to 109F	
2	10AØ to 10EF	
3	2000 to 204F	(Break 1)
4	2050 to 209F	
5	20AØ to 20EF	
6	0800 to 084F	(Break 2)
7	0850 to 089F	
8	08AØ to 08EF	
	O	
	O	
	O	

Figure 18: Sequential Addressing Example With Two Breaks

Double Height/Width Operation

When double height/width characters (2XH/2XW) are displayed, the following will occur:

1. the CRT 9007 will address half as many characters for each data row by incrementing its address every other character clock.
2. the high speed video shift register supplying serial video to the CRT must shift out dots at half frequency.
3. For double height, the scan line counter outputs (SL3-SL0 or $\overline{SLG}$, SLD) are incremented every other scan line.

The CRT 9007 is informed of the double height or double width display modes via the 2 most significant bits of the row table address or the 2 most significant bits of the AUXILIARY ADDRESS registers depending on the selected addressing mode. In any case, once the information is obtained by the CRT 9007, it must initiate the 3 tasks listed above. Tasks 1 and 3 are performed as appropriate and task 2 is performed using the CURS output of the CRT 9007 during CBLANK (horizontal retrace) to signal the external logic that a change in the dot shift frequency is required. The exact time of activation and deactivation of the CURS signal during horizontal retrace is a function of addressing mode, operation mode and actual scan line number to be painted. Tables 1 and 2 show the cursor activation and deactivation times as a function of the buffer configuration and addressing mode for the top scan line of a new data row. Tables 1 and 2 assume a cursor skew of zero. A cursor skew will effect the cursor position during trace as well as retrace time. For all subsequent scan lines, the CURS signal is activated 3 $\overline{CCLK}$'s after VLT trailing edge and stays active for exactly 1 $\overline{CCLK}$ assuming no cursor skew. When the cursor is placed on a double height or double width data row, it will become active for 2 $\overline{CCLK}$'s to allow the cursor to be displayed as double width. If the cursor position is programmed to reside in the top half of a double height data row, it may become active for all scan lines in both the current and next data row to allow the cursor to be displayed as double height.

For row driven addressing, a particular data row or pair of data rows can appear in one of the following ways as a function of the two most significant bits of the row table address (bits 15 and 14).

—Single height, single width (Row table address bits 15, 14 = 00). The CRT 9007 will display the particular data row as single height, single width.

—Single height, double width (Row table address bits 15, 14 = 01). The CRT 9007 will display the particular data row as single height double width by accessing half as many characters as appear in a single width data row. The CURS signal becomes active during horizontal retrace in the manner described previously.

—Double height, double width top half (Row table address bits 15, 14 = 10). In addition to providing the special timing associated with single height double width data rows, the scan line counter is started from zero and incremented every other scan line until N scan lines are painted (N is the number of scan lines per single height data row). In this way, new dot information appears every other scan line and the top half of the data row appears in N scan lines.

—Double Height, Double Width Bottom Half (Row table address bits 15, 14 = 11)—Same as Double Height, Double Width Top except the scan line counter is started from N/2 (or (N-1)/2 if N is odd), and incremented every other scan line until N scan lines are painted. In single row buffer operation, a double height bottom data row can only stand alone during a smooth scroll operation; otherwise it is assumed to follow a double height top data row.

OPERATION MODE	ADDRESSING MODE	
	Row Driven (linked list or contiguous)	Sequential
Repetitive Memory Addressing	1 CCLK after high byte of row table read	1 CCLK after TSC leading edge
Single row buffer	1 CCLK after high byte of row table read	1 CCLK after TSC leading edge
Double row buffer	1 CCLK after high byte of row table read	1 CCLK after ACK leading edge

Table 1: Double Height/Width CURS activation for top scan line of new data row.

OPERATION MODE	ADDRESSING MODE	
	Row driven (linked list or contiguous)	Sequential
Repetitive Memory Addressing	at the leading edge of VLT	at the leading edge of VLT
Single row buffer	at the leading edge of VLT	at the leading edge of VLT
Double row buffer	1 CCLK after leading edge of CURS	1 CCLK after leading edge of CURS

Table 2: Double Height/Width CURS deactivation for top scan line of new data row.

PROCESSOR ADDRESSABLE REGISTERS

All CRT 9007 registers are selected by specifying the address on VA5-0 and asserting $\overline{CS}$. All 14 bit registers are written or read as two consecutive 8 bit registers addressed low byte first. Only the VERTICAL CURSOR REGISTER and the HORIZONTAL CURSOR REGISTER are read/write registers with 2 different addresses for read or write operations. The register address assigned to each register represents the actual address in hexadecimal form that must appear on VA5-0. Figure 2 illustrates all processor to CRT 9007 register timing. Tables 3a, 3b, and 3c summarize all register bits and provide register addresses.

HORIZONTAL TIMING REGISTERS

The following 4 registers define the horizontal timing parameters. Figure 19 relates the horizontal timing to these registers.

CHARACTERS PER HORIZONTAL PERIOD (R0)

This 8 bit write only register, programmed in units of character times, represents the total number of characters in the horizontal period (trace plus retrace time). This register is programmed with the binary number N where N is the total characters in the horizontal period. The horizontal period should not be programmed for less than 12 characters.

CHARACTERS PER DATA ROW (R1)

This 8 bit write only register, programmed in units of character times, represents the number of displayable characters during the horizontal trace interval. The difference R0 minus R1 represents the number of character times reserved for horizontal retrace. This register is programmed with the binary number (N-1) where N is the displayable characters per data row.

HORIZONTAL DELAY (R2)

This 8 bit write only register, programmed in units of character times, represents the time between the leading edge of horizontal sync and leading edge of VLT. This register is programmed with N where N represents the time of horizontal delay. By programming this time greater than the horizontal blank interval, one can obtain negative front porch (horizontal sync begins before the horizontal blank interval).

HORIZONTAL SYNC WIDTH (R3)

This 8 bit write only register defines the horizontal sync width in units of character times. The start of the sync pulse is defined by the HORIZONTAL DELAY REGISTER and the end is independent of the start of the active display time. This register is programmed with N where N is the horizontal sync width. However this register must be programmed less than or equal to [(A/2)-1] where A is the programmed contents of REGISTER Ø rounded to the smallest even integer.

VERTICAL TIMING REGISTERS

The following 5 registers define the vertical timing parameters. Figure 20 relates the vertical timing to these registers.

VERTICAL SYNC WIDTH (R4)

This 8 bit write only register defines the vertical sync width in units of horizontal periods. The start of this signal is defined by the delay register (R5) and the end is independent of the start of the active display time. This register is programmed with N where N is the vertical SYNC width.

VERTICAL DELAY (R5)

This 8 bit write only register, programmed in units of horizontal periods, represents the time between the leading edge of vertical sync and the leading edge of the first VLT after the vertical retrace interval. This register is programmed with (N+1) where N represents the time of the vertical delay.

VISIBLE DATA ROWS PER FRAME (R7)

This 8 bit write only register defines the number of data rows displayed on the screen. This register is programmed with (N-1) where N is the number of data rows displayed.

SCAN LINES PER DATA ROW (R8)

The 5 LSBs of this write only register define the number of scan lines per data row. These 5 bits are programmed with (N-1) where N is the number of scan lines per data row. When programming for scan lines per data row greater than 16, only the serial scan line pin option (SLD, $\overline{SLG}$) can be used.

SCAN LINES PER VERTICAL PERIOD (R8; R9)

Registers R9 and the 3 most significant bits of R8 define the number of scan lines for the entire frame. R8 contains the 3 most significant bits of the 11 bit programmed value and R9 contains the 8 least significant bits of the 11 bit programmed value. The 11 bits are programmed with N where N is the number of scan lines per frame. In the 2 interlace modes, the programmed value represents the number of scan lines per field.

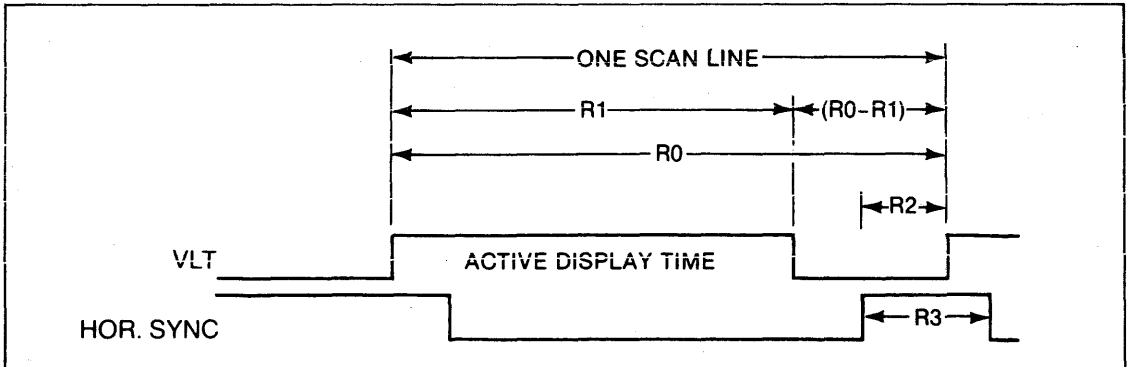


FIGURE 19: CRT 9007 HORIZONTAL TIMING

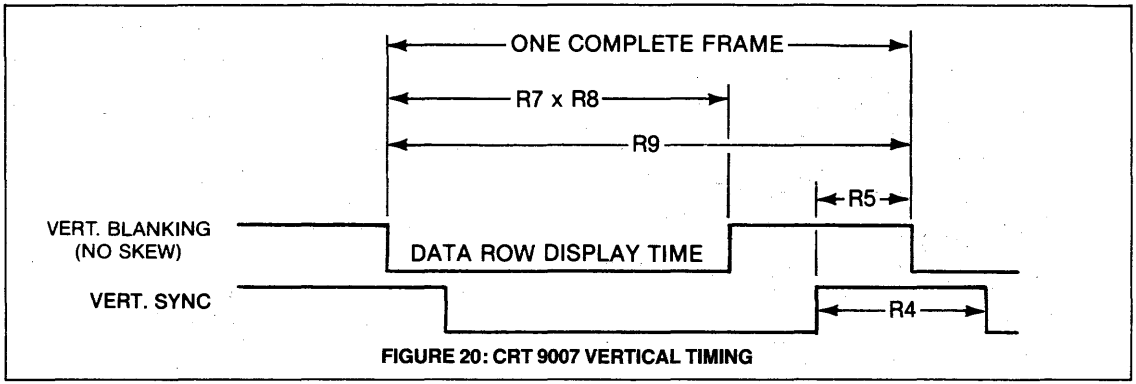


FIGURE 20: CRT 9007 VERTICAL TIMING

PIN CONFIGURATION/SKEW BITS REGISTER (R6)

This 8 bit write only register is used to select certain pin configurations and to skew (delay) the cursor and the blank signals independently with respect to the video signal sent to the monitor. The bits take on the following definition:

Bit 7, 6 (Pin Configuration)

These 2 bits, as illustrated in tables 4 and 5, define all pinout configurations as a function of double row buffer mode and non double row buffer mode. (The buffer mode is defined in the CONTROL REGISTER bits 3, 2, and 1.) The attribute assemble mode is assumed to be a double row buffer mode and obeys table 4.

Bits 5, 4, 3 (Cursor skew)

These three bits define the number of character clocks the cursor signal is skewed (delayed) from the VLT signal. The VLT signal is active for all characters within a data row and a non skewed cursor will always become active within the active VLT time at the designated position. The cursor can be skewed from 0 to 5 character clocks (Bits 5, 4 and 3 programmed from 000 to 101, bit 5 is the most significant bit; bit 3 is the least significant bit). For double height/width data rows, the cursor signal appearing during horizontal retrace is also skewed as programmed.

Bits 2, 1, 0 (Blank skew)

These three bits define the number of character clocks the horizontal blank component of the CBLANK signal is skewed (delayed) from the VLT signal. The edges of VLT will line up exactly with the edges of the horizontal component of the CBLANK signal if no skew is programmed. The CBLANK can be skewed from 0 to 5 character clocks (Bits 2, 1 and 0 programmed from 000 to 101, bit 2 is the most significant bit; bit 0 is the least significant bit).

REGISTER R6 BITS		CRT 9007 PIN NUMBER					
7	6	28	29	30	31	32	33
0	1	DMAR	WBEN	$\overline{SLG}$	SLD	$\overline{CSYNC}$	ACK
1	1	DMAR	WBEN	$\overline{SLG}$	SLD	LPSTB	ACK
0	0	NOT PERMITTED					
1	0	NOT PERMITTED					

Table 4: Pin configuration for double row buffer and attribute assemble modes.

REGISTER 6 BITS		CRT 9007 PIN NUMBER					
7	6	28	29	30	31	32	33
0	0	SL3	SL2	SL1	SL0	$\overline{CSYNC}$	$\overline{TSC}$
1	0	SL3	SL2	SL1	SL0	LPSTB	$\overline{TSC}$
1	1	VBLANK	$\overline{CSYNC}$	$\overline{SLG}$	SLD	LPSTB	$\overline{TSC}$
0	1	NOT PERMITTED					

Table 5: Pin configuration for Single Row Buffer and Repetitive Memory Addressing Modes.

DMA CONTROL REGISTER (RA)

This 8 bit write only register allows the user to set up a DMA burst count and delay as well as disable the DMA mechanism of the CRT 9007. The register bits have the following definition:

Bit 7 (DMA Disable)

A logic one will immediately force the CRT 9007 DMA request to the inactive level and the CRT 9007 address bus (VA13-VA0) will enter its high impedance state. After enabling the DMA mechanism by setting this bit to a logic zero, a start command must be issued (see START COMMAND, R15).

Bits 6, 5, 4 (DMA Burst Delay)

These 3 bits define the number of clock delays ($\overline{CCLK}$) between successive DMAR–ACK sequences. Bit 6 is the most and bit 4 is the least significant bit respectively. When programmed with a number N, the CRT 9007 will delay for 4 (N + 1) clock cycles before initiating another DMA request. If 111 is programmed, however, this will result in a zero delay allowing all characters to be retrieved from video RAM in one DMA burst regardless of the value programmed for the DMA burst count.

Bits 3, 2, 1, 0 (DMA Burst Count)

These 4 bits define the number of DMA operations in one DMAR-ACK sequence. Bit 3 is the most and bit 0 is the least significant bit respectively. When programmed with a number N, the CRT 9007 will produce 4 (N + 1) DMA cycles before relinquishing the bus. When programmed with 0000, the minimum DMA Burst will occur ($4 \times 1 = 4$) and when programmed with 1111 the maximum DMA Burst will occur ($4 \times 16 = 64$). When bits 6, 5, and 4 are programmed with 111, no DMA delay will occur and the Burst count will equal the number of programmed characters per data row as specified in R1. Refer to figures 9 and 15 which illustrate a DMA burst of 16 and a DMA delay of 8 for double row buffer and attribute assemble modes respectively. For single row buffer operation, no DMA delay is permitted and bits 6, 5, 4 must be programmed with 000.

CONTROL REGISTER (RB)

This 7 bit write only register controls certain frame operations as well as specifying the operation mode used. Internal to the CRT 9007, this register is double buffered. Changes in the register are reflected into the CRT 9007 at a particular time during vertical retrace. This allows the user to update the CONTROL REGISTER at any time without running the risk of destroying the frame or field currently being painted.

The bits take on the following definition:

Bit 6 (PB/$\overline{SS}$)

= 0; The smooth scroll mechanism is enabled permitting the SMOOTH SCROLL OFFSET REGISTER (R17) to be loaded in the scan line counter (SL3-0 or SLG, SLD signals) allowing for a scroll on the screen of a predetermined number of scan lines per frame or field. The starting and ending of the smooth scroll operation is defined by the DATA ROW START REGISTER (R11) and DATA ROW END REGISTER (R12) respectively.

= 1; The page blank mechanism is enabled. The CBLANK signal is made active high for a continuous period of time starting and ending at the data row defined by the DATA ROW START REGISTER (R11) and DATA ROW END REGISTER (R12) respectively.

Bits 5, 4 (Interlace)—these 2 bits define one of 3 displayed modes as illustrated in figure 21

= 00; Non interlaced display

= 10; Enhanced video interlace. This display mode will produce an interlaced frame with the same dot information painted in adjacent odd/even scan lines.

= 11; Normal video interlace. This display mode will produce an interlaced frame with odd scan lines of characters displayed in odd fields and even scan lines displayed in even fields. This mode can be used to allow the screen to show twice as many data rows at half the height since it effectively doubles the character density on the screen.

= 01; This combination is not permitted.

Bits 3, 2, 1 (Operation modes): These 3 bits define the various buffer configuration modes as follows:

= 000; (Repetitive memory addressing)—In this mode the address information (VA13-VA0) appears during every visible scan line and the address bus enters its high impedance state during all retrace intervals. When using a row driven addressing mode (linked list or contiguous), the address bus is in the high impedance state for all retrace intervals except the horizontal retrace interval prior to the top scan line of a new data row. This period can be distinguished from other retrace intervals because the $\overline{DRB}$ (data row boundary) signal is active.

= 001; (Double row buffer)—In this mode, the CRT 9007 will address a particular data row from video memory one data row prior to the time when it is displayed on the CRT. During vertical retrace, the first data row is retrieved and loaded into the double row buffer. At the next data row boundary (in this case at the end of vertical retrace), the first data row feeds the character generator while the second data row is retrieved from video memory. The address bus will enter its high impedance state in accordance with the DMA mechanism for address bus arbitration.

= 100; (Single row buffer)—In this mode, during the first scan line of each data row, the CRT 9007 will address video memory, load the buffer and feed the character generator at the painting rate of the CRT. If the CRT 9007 is used in a row driven addressing mode, it will drive the address bus during the retrace period prior to the first scan line of each data row in order to retrieve the row table address. It will automatically enter the high impedance state at the end of the first visible scan line of each data row. If the CRT 9007 is used in a sequential addressing mode, it will drive the address bus only during the visible line time of the first scan line of each data row.

= 111; (Attribute assemble)—In the attribute assemble mode, character data and attribute data are shared in consecutive alternating byte locations in memory. When the CRT 9007 reads an attribute byte, it loads it into its internal attribute latch. During the next memory access, a character byte is fetched. At this time the CRT 9007 isolates its bus from the main system bus and outputs the previously latched attribute. A WBEN signal is produced during every character byte fetch to allow the character and its associated attribute to be simultaneously latched into two double row buffers. This mode assumes that there exists twice as many byte locations as there are displayable character positions on the CRT. The first byte of every data row is assumed to be an attribute.

All other combinations of the CONTROL REGISTER bits 3, 2, 1 are not permitted.

Bit 0 ($\overline{2XC}$/1XC): This bit allows for either single or double height cursor display when the cursor is placed within a double height data row as follows:

= 1; (Single height cursor)—The CURS signal will appear during every scan line for single height data rows and will appear only during the top half or bottom half of a double height data row depending upon where the VERTICAL CURSOR REGISTER (R18, R38) defines the CURSOR data row.

= 0; (Double height cursor)—If the VERTICAL CURSOR REGISTER (R18, R38) places the cursor in the top half of a double height data row, the CURS signal will appear during every scan line of the top half (the current data row) and the bottom half (the next data row) of the double height data row. If the cursor is placed in the bottom half of a double height data row or if it is placed in a single height data row, the CURS signal will only appear during the one particular data row.

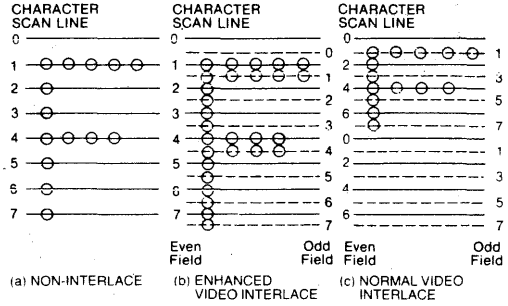


FIGURE 21: CRT 9007 INTERLACE MODES

TABLE START REGISTER (RC AND RD)

This 16 bit write only register contains a 14 bit address which is used in a variety of ways depending on the addressing mode chosen; the 2 remaining bits define the addressing mode. Register C contains the lower 8 bits of the 14 bit address. The 6 least significant bits of register D contain the upper 6 bits of the 14 bit address. The 2 most significant bits of register D define four addressing modes as follows:

Register D bits 7, 6:

= 00; (Sequential addressing mode)—The CRT 9007 will address video memory in a sequential fashion starting with the 14 bit address contained in REGISTER D bits 5-0 and REGISTER C bits 7-0. 2 sequential breaks are allowed as defined by SEQUENTIAL BREAK 1 (R10) using AUXILIARY ADDRESS REGISTER 1 (RE and RF) and SEQUENTIAL BREAK 2 (R12) using AUXILIARY ADDRESS REGISTER 2 (R13 and R14).

= 01; (Sequential roll addressing mode)—The CRT 9007 will address video memory in a sequential fashion starting with the 14 bit address contained in REGISTER D bits 5-0 and REGISTER C bits 7-0. SEQUENTIAL BREAK REGISTER 1 and AUXILIARY ADDRESS REGISTER 1 can be used to cause one sequential break as described in the sequential addressing mode. A second break in the sequential addressing can be defined by SEQUENTIAL BREAK REGISTER 2 (R12) and AUXILIARY ADDRESS REGISTER 2 (R13 and R14) permitting up to 3 separate sequentially addressed screens to be painted.

= 10; (Contiguous row table mode)—The CRT 9007 will address video memory according to the contiguous row table format. The 14 address bits contained in REGISTER D bits 5-0 and REGISTER C bits 7-0 define an address that points to the beginning of the contiguous row table.

= 11; (Linked list row table mode)—The CRT 9007 will address video memory according to the linked list row table format. The 14 address bits contained in REGISTER D bits 5-0 and REGISTER C bits 7-0 define the address at which the second row table entry and the first data row reside.

AUXILIARY ADDRESS REGISTER 1 (RE and RF)

This 16 bit write only register contains a 14 bit address. The 6 least significant bits of REGISTER F contain the upper order 6 bits of the 14 bit address and REGISTER E contains the 8 lower order bits of the 14 bit address. When the current data row equals the value programmed in SEQUENTIAL BREAK REGISTER 1 (R10) the remainder of the screen is addressed sequentially starting at the 14 bit address specified in this register. This sequential break overrides any row driven addressing mode used prior to the sequential break.

The 2 most significant bits of REGISTER F allow one to attach double height and/or double width characteristics to every data row in this sequentially addressed area in the following way:

For Double row buffer or attribute assemble mode REGISTER F Bits 7, 6

= 00; single height single width

= 01; single height double width

= 10; even data rows are double height double width top half odd data rows are double height double width bottom half

= 11; odd data rows are double height double width top half even data rows are double height double width bottom half

For Single row buffer or repetitive memory addressing mode REGISTER F Bits 7, 6

= 00; single height single width

= 01; single height double width

= 10; odd data rows are double height double width top half even data rows are double height double width bottom half

= 11; even data rows are double height double width top half
odd data rows are double height double width bottom half

SECTION V

SEQUENTIAL BREAK REGISTER 1 (R10)

This 8 bit write only register defines the data row number in which a new sequential video address begins as specified by AUXILIARY ADDRESS REGISTER 1 (RE and RF). To disable the use of this break, the register should be loaded with a data row count greater than the number of displayable data rows on the screen.

DATA ROW START REGISTER (R11)

This 8 bit write only register defines the first data row number at which a page blank or smooth scroll operation will begin. Bit 6 of the CONTROL REGISTER determines if a page blank or smooth scroll operation will occur.

DATA ROW END/SEQUENTIAL BREAK REGISTER 2 (R12)

This 8 bit write only register has a dual function depending on the addressing mode used. For row driven addressing (contiguous or linked list as specified by the 2 most significant bits of the TABLE START REGISTER) this register defines the data row number which ends either a page blank or smooth scroll operation. The row numerically one less than the row defined by this register is the last data row on which the page blank or smooth scroll will occur. To use the page blank feature to blank a portion of the screen that includes the last displayed data row, this register must be programmed to zero. For sequential addressing, this register can cause a break in the sequential addressing at the data row number specified and a new sequential addressing sequence begins at the address contained in AUXILIARY ADDRESS REGISTER 2.

AUXILIARY ADDRESS REGISTER 2 (R13 and R14)

This 16 bit write only register contains a 14 bit address. The 6 least significant bits of REGISTER 14 contain the upper order 6 bits of the 14 bit address and REGISTER 13 contains the 8 lower order bits of the 14 bit address. In the row driven addressing mode, this register is automatically loaded by the CRT 9007 with the current table address. The two most significant bits of REGISTER 14 specify one of four combinations of row attributes (for example double height

double width) on a row by row basis. Refer to the section entitled Double Height/Double Width operation for the meaning of these 2 bits. In the sequential addressing mode, this register can be loaded by the processor with a 14 bit address and a 2 bit row attributes field. The bit positions are identical for the row driven addressing mode. When the current data row equals the value programmed in DATA ROW END/SEQUENTIAL BREAK REGISTER 2 (R12), the remainder of the screen is addressed sequentially starting at the location specified by the programmed 14 bit address. The 2 most significant bits of register 14 allow one to attach double height and or double width characteristics to every data row in this sequentially addressed area. The bit definitions take on the same meaning as the 2 most significant bits of AUXILIARY ADDRESS REGISTER 1 and affect the display in an identical manner.

START COMMAND (R15)

After all vital screen parameters are loaded, a START command can be initiated by addressing this dummy register location within the CRT 9007. A START command must be issued after the DMA mechanism is enabled (DMA CONTROL REGISTER bit 7).

RESET COMMAND (R16)

The CRT 9007 can be reset via software by addressing this dummy location. Activation of the RST input pin or initiating this software command will effect the CRT 9007 in an identical manner. The reset state of the CRT 9007 is defined as follows:

CRT 9007 outputs	Reset state
VA13-0	High impedance
VD7-0	High impedance
HS	High
VS	High
CBLANK	High
CURS	Low
VLT	Low
DRB	High
INT	Low
Pin 28	Low
Pin 29	Low
Pin 30	Low
Pin 31	Low
Pin 32	Low

SMOOTH SCROLL OFFSET REGISTER (R17)

This register is loaded with the scan line offset number to allow a smooth scroll operation to occur. The offset register causes the scan line counter output of the CRT 9007 to start at the programmed value rather than zero for the data row that starts the smooth scroll interval. The start is specified in the DATA ROW START REGISTER (R11). Typically, this register is updated every frame and it ranges from zero (no offset) to a maximum of the programmed scan lines per data row (maximum offset). For example, if 12 scan lines per data row are programmed (scan line 0 to scan line 11) an offset of zero will cause an unscrolled display. An offset of one will cause a display starting at scan line 1 and ending at scan line 11 (eleven scan lines total). An offset of eleven will cause a display starting at scan line eleven.

The next scan line will be zero, starting the subsequent data row. To allow smooth scroll of double height rows, the programmed range of the register is from zero to twice the programmed scan lines per data row. Whenever the offset register if greater than the programmed scan lines per data row, bit 7 of the register must be set to a logic 1 (offset overflow). It must be set to a logic zero at all other times. The 6 bit offset value occupies bits 6 through 1. Bit 0 must always be programmed with a logic zero. By setting the offset overflow (bit 7) to a logic 1, it is possible to have the bottom half of a double height data row stand alone in Single Row Buffer Mode by programming the scrolled data row as double height top half and loading R17 with the proper value.

VERTICAL CURSOR REGISTER (R18 or R38)

This 8 bit read/write register specifies the data row in which the cursor appears. To write into this register it is addressed as R18 and to read from this register it is addressed as R38.

HORIZONTAL CURSOR REGISTER (R19 or R39)

This 8 bit read/write register specifies the character position in which the cursor appears. To write into this register it is addressed as R19 and to read from this register it is addressed as R39.

It should be noted that the vertical and horizontal cursor is programmed in an X-Y format with respect to the screen and not dependant upon a particular location in video memory. The cursor will remain stationary during all scroll operations.

INTERRUPT ENABLE REGISTER (R1A)

This 3 bit write only register allows each of the three CRT 9007 interrupt conditions to be individually enabled or disabled according to the following definition:

Bit 6 (Vertical retrace interrupt)—This bit, when set to a logic one, will cause the CRT 9007 to activate the INT signal when a vertical retrace (i.e., the start of the vertical blanking interval) begins.

Bit 5 (Light pen interrupt)—This bit, when set to a logic one, will cause the CRT 9007 to activate the INT signal when the LIGHT PEN REGISTER (R3B, R3C) captures an X-Y coordinate. This interrupt, which occurs at the beginning of vertical retrace, reflects the occurrence of a LPSTB input on the frame or field just painted. This interrupt need not be enabled when other CRT 9007 interrupt conditions are enabled since the STATUS REGISTER (R3A) will flag the occurance of a light pen update and servicing can be done off of other interrupts.

Bit 0 (Frame timer)—This bit, when set to a logic one, allows the CRT 9007 to activate the INT signal once every frame or field at a time when a potential smooth scroll update may occur. In this way the user can use the frame timer interrupt as both a real time clock and can service smooth scroll updates and other frame oriented operations by using the appropriate status bits. This interrupt will occur after the last row table entry is read by the CRT 9007. In single row buffer operation, this will occur one data row before the start of vertical retrace. In double row buffer operation, this will occur two data rows before the start of vertical retrace.

STATUS REGISTER (R3A)

This 5 bit register flags the various conditions that can potentially cause an interrupt regardless of whether the corresponding condition is enabled for interrupt. In this way some or all of the conditions can be reported to the processor via the STATUS REGISTER. If some of the conditions are enabled for interrupt, the processor, in response to an interrupt, simply has to read the STATUS REGISTER to determine the cause of the interrupt. The bit definition of the STATUS REGISTER is as follows:

Bit 7 (Interrupt Pending)—This bit will set when any other status bit, having its corresponding interrupt enabled, experiences a 0 to 1 transition. In this manner, when the processor services a potential CRT 9007 interrupt, it only has to test the interrupt pending bit to determine if the CRT 9007 caused the interrupt. If it did, the individual bits can then be tested to determine the details of the CRT 9007 interrupt. Any noninterruptable status change (corresponding interrupt enable bit reset to a logic 0) will not be reflected in the interrupt pending bit and must be polled by

the processor in order to provide service. The interrupt pending bit is reset when the status register is read. All other bits except Light Pen Update are reset to a logic 0 at the end of the vertical retrace interval. The light pen update bit is reset to a logic 0 when the HORIZONTAL LIGHT PEN REGISTER is read.

Bit 6 (Vertical Retrace)—A logic 1 indicates that a vertical retrace interval has begun.

Bit 5 (Light Pen Update)—A logic 1 indicates that a new coordinate has been strobed into the LIGHT PEN REGISTER. It is reset to a logic zero when the HORIZONTAL LIGHT PEN REGISTER is read. The light pen coordinates may have to be modified via software depending on light pen characteristics.

Bit 2 (odd/even)—For a normal video interlaced display, this bit is a logic 1 when the field about be painted is an odd field and is a logic zero when the field about be painted is an even field.

Bit 0 (Frame timer occurred)—This bit becomes a logic 1 either one or two data rows before the start of vertical retrace. Since this bit is set when the CRT has finished reading the row table for the frame or field just painted, it permits row table manipulation to start at the earliest possible time.

VERTICAL LIGHT PEN REGISTER (R3B)

This 8 bit read only register contains the vertical coordinate captured at the time the CRT 9007 received a light pen strobe signal (LPSTB).

HORIZONTAL LIGHT PEN REGISTER (R3C)

This 8 bit read only register contains the horizontal coordinate captured at the time the CRT 9007 received a light pen strobe signal. When a coordinate is captured, the appropriate status bit is set and further transitions on LPSTB are ignored until this register is read. The reading of this register will reset the light pen status bit in the STATUS REGISTER. The captured coordinate may have to be modified in software to allow for light pen response.

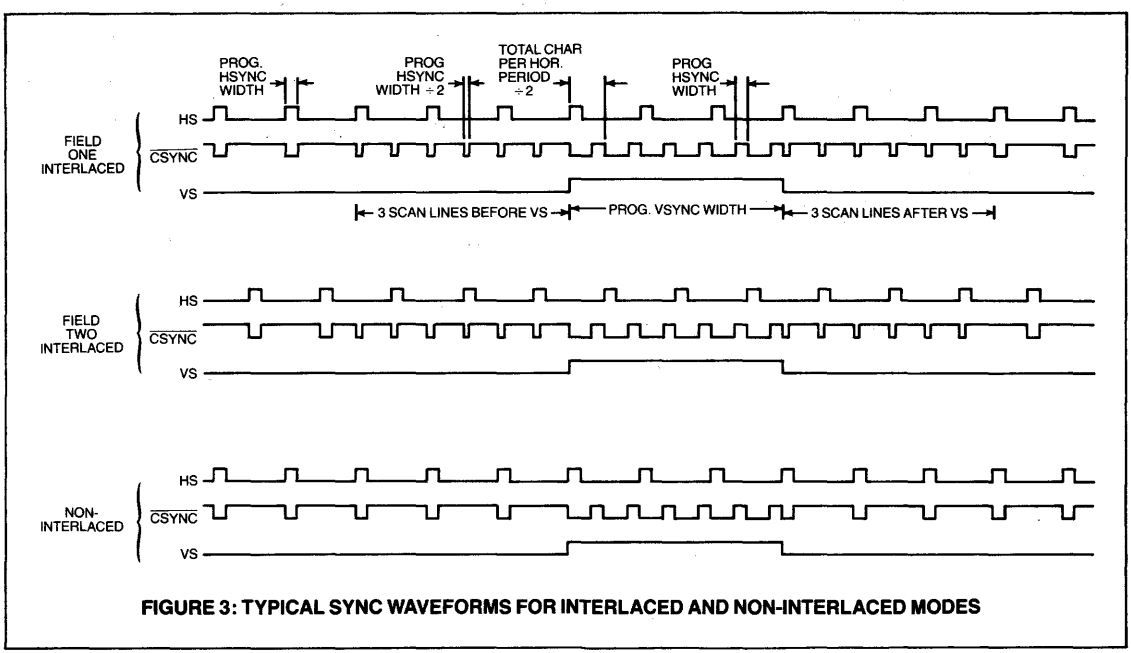


FIGURE 3: TYPICAL SYNC WAVEFORMS FOR INTERLACED AND NON-INTERLACED MODES

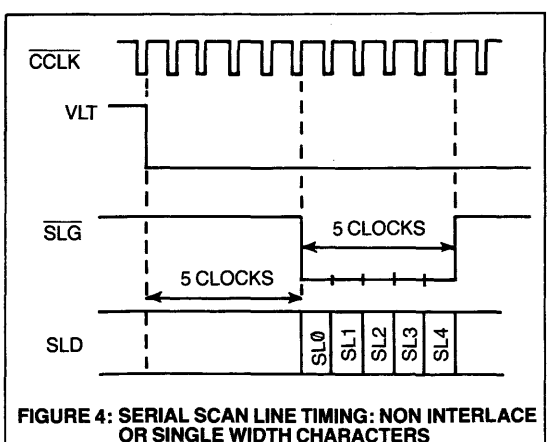


FIGURE 4: SERIAL SCAN LINE TIMING: NON INTERLACE OR SINGLE WIDTH CHARACTERS

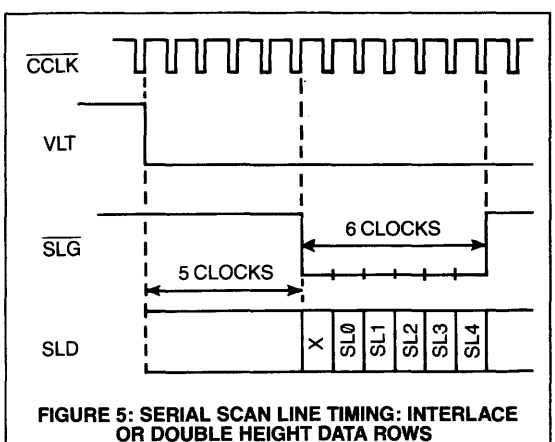


FIGURE 5: SERIAL SCAN LINE TIMING: INTERLACE OR DOUBLE HEIGHT DATA ROWS

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0° to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
	Input voltage					
V_{IL}	Low			0.8	V	
V_{IH1}	High	2.0			V	all inputs except $\overline{CCLK}$
V_{IH2}	High	4.3			V	$\overline{CCLK}$ input; see note 4
	Output voltage					
V_{OL}	Low			0.4	V	I_{OL} = 1.6 mA
V_{OH}	High	2.4			V	I_{OH} = 100μA
	Input leakage current					
I_{L1}				10	μA	$0 \leq V_{IN} \leq 3.5V$; excluding $\overline{CCLK}$
I_{L2}				50	μA	V_{IN} = 5V; for $\overline{CCLK}$
I_{L3}				−200	μA	V_{IN} = 0V; for $\overline{CCLK}$
	Input capacitance					
C_{IN1}			10	15	pF	all inputs except $\overline{CCLK}$ at 1 MHZ
C_{IN2}			25	50	pF	$\overline{CCLK}$ input at 1 MHZ
	Power supply current					
I_{CC}			100	170	mA	

AC ELECTRICAL CHARACTERISTICS[3] $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
	Clock					
t_{CY}	clock period	330		1200	ns	for double row buffer or attribute assemble
		300		1200	ns	for all other operation modes
t_{CKL}	clock low	90			ns	
t_{CKH}	clock high	150			ns	
t_{CKR}	clock rise time			15	ns	measured from 0.8V to 3.5V level
t_{CKF}	clock fall time			10	ns	measured from 90% to 10% points
	Output delay[1]					
t_{D1}				150	ns	
t_{D2}				150	ns	
t_{D3}				150	ns	
t_{D4}				150	ns	
t_{VA}		25		115	ns	measured to the 2.3V or 0.5V level on VA13-VA0
t_{DSL}				500	ns	
t_{D5}				185	ns	
t_{D6}				185	ns	
t_{DSY}				185	ns	
t_{VDS}		50			ns	valid for loading auxiliary address register 2 or the attribute latch
t_{VDH}		10			ns	
t_{VDO}				185	ns	c_L = 50pF
t_{SLG}				185	ns	
t_{SLD}				185	ns	
t_{D7}				240	ns	cursor skew of zero
t_{D7}				185	ns	cursor skew of one through five
t_{D8}				300	ns	
	Processor Read/write[2]					
t_{AS}		110			ns	
t_{AH}		0			ns	
t_{PW}		165			ns	
t_{CSH}		650			ns	
t_{PDS}		100			ns	
t_{PDH}		0			ns	
t_{PDA}				140	ns	
t_{PDO}		10		85	ns	
t_{IRR}				400	ns	
	Miscellaneous timing					
t_{ATS}		25		115	ns	measured from the 0.4V level of ACK or $\overline{TSC}$ falling edge
t_{RW}		$4t_{CY}$			ns	measured from the 0.4V level falling edge to 0.4V level rising edge
t_{AKW}		50			ns	see figure 24
t_{AKS}		50			ns	see figure 24

NOTE:
1. Timing measured from the 1.5V level of the rising edge of $\overline{CCLK}$ to the 2.4V (high) or 0.4V (low) voltage level of the ouput unless otherwise noted.
2. Reference points are 2.4V high and 0.4V low.
3. Loading on all outputs is 30 pF except where noted.
4. This level must be reached before the next falling edge of $\overline{CCLK}$.

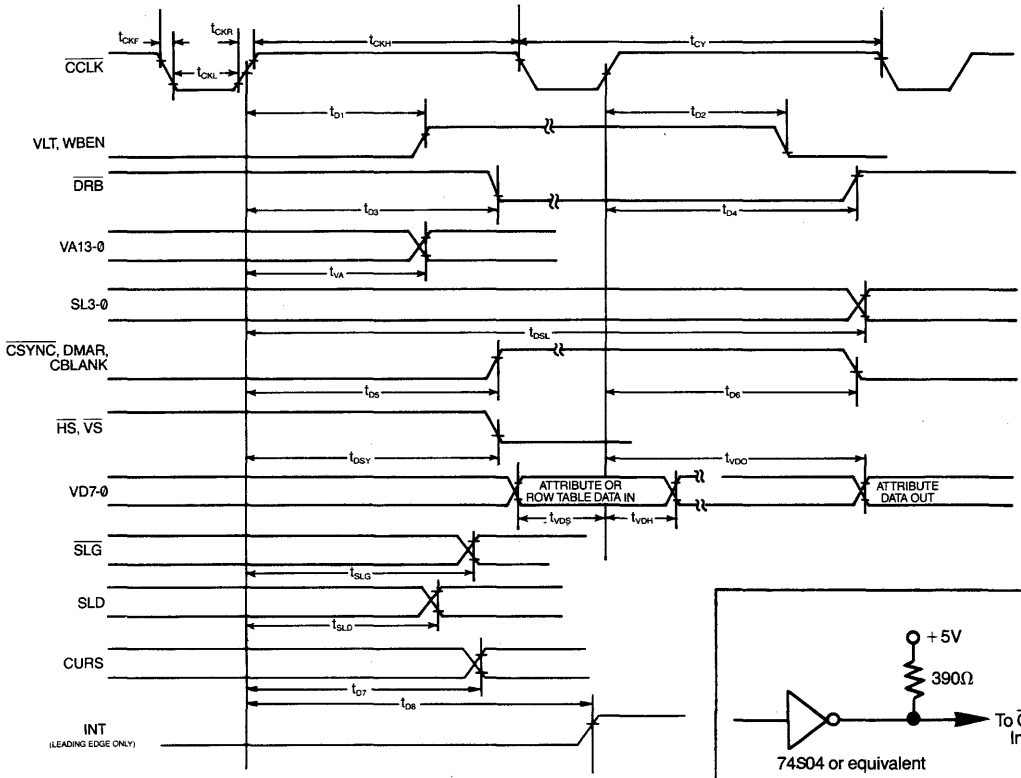


FIGURE 22: CRT 9007 TIMING PARAMETERS: OUTPUT SIGNALS

FIGURE 25: RECOMMENDED CCLK DRIVER CIRCUIT

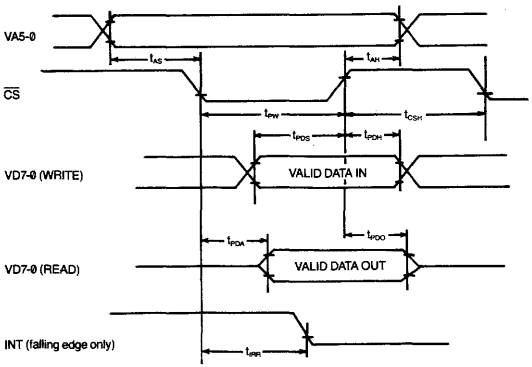
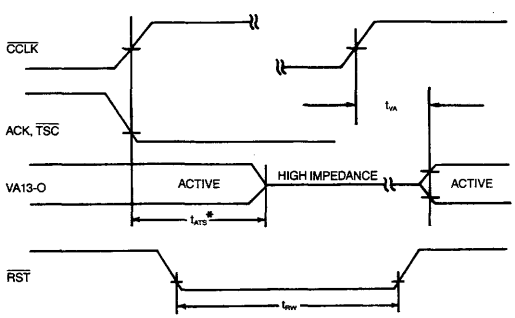


FIGURE 2: CRT 9007 PROCESSOR READ AND WRITE TIMING PARAMETERS



* t_{ATS} is controlled directly from ACK or $\overline{TSC}$ or from the particular $\overline{CCLK}$ that ends a DMA burst cycle.

FIGURE 23: CRT 9007 MISCELLANEOUS TIMING PARAMETERS

Register Type	ADDRESS DECODE VA5	VA4	VA3	VA2	VA1	VA0	BIT DEFINITION D7	D6	D5	D4	D3	D2	D1	D0	REGISTER NUMBER (HEX)
WRITE	0	0	0	0	0	0	MSB	CHARACTERS PER HORIZONTAL PERIOD						LSB	R0
WRITE	0	0	0	0	0	1	MSB	CHARACTERS PER DATA ROW						LSB	R1
WRITE	0	0	0	0	1	0	MSB	HORIZONTAL DELAY						LSB	R2
WRITE	0	0	0	0	1	1	MSB	HORIZONTAL SYNC WIDTH						LSB	R3
WRITE	0	0	0	1	0	0	MSB	VERTICAL SYNC WIDTH						LSB	R4
WRITE	0	0	0	1	0	1	MSB	VERTICAL DELAY						LSB	R5
WRITE	0	0	0	1	1	0	PIN CONFIG-URATION	CURSOR SKEW MSB			LSB	BLANK SKEW MSB		LSB	R6
WRITE	0	0	0	1	1	1	MSB	VISIBLE DATA ROWS PER FRAME						LSB	R7
WRITE	0	0	1	0	0	0	SCAN LINES/FRAME (B10))	(B8)	MSB	SCAN LINES PER DATA ROW				LSB	R8
WRITE	0	0	1	0	0	1	(B7)	SCAN LINES PER FRAME						LSB (B0)	R9

Table 3a: CRT 9007 Screen Format Registers

Register Type	ADDRESS DECODE VA5	VA4	VA3	VA2	VA1	VA0	BIT DEFINITION D7	D6	D5	D4	D3	D2	D1	D0	REGISTER NUMBER (HEX)
WRITE	0	0	1	0	1	0	DMA DIS-ABLE	DMA BURST DELAY MSBA		LSB	DMA BURST COUNT MSB			LSB	RA
WRITE	0	0	1	0	1	1	X	PB/SS	INTERLACE MODES		OPERATION MODES			2XC/1XC	RB
WRITE	0	0	1	1	0	0	MSB	TABLE START REGISTER (LS BYTE)						LSB	RC
WRITE	0	0	1	1	0	1	ADDRESS MODE	TABLE STRT REGISTER (MS BYTE) MSB						LSB	RD
WRITE	0	0	1	1	1	0	MSB	AUXILIARY ADDRESS REGISTER 1 (LS BYTE)						LSB	RE
WRITE	0	0	1	1	1	1	ROW ATTRIBUTES	AUXILIARY ADDRESS REGISTER 1 (MS BYTE) MSB						LSB	RF
WRITE	0	1	0	0	0	0	MSB	SEQUENTIAL BREAK REGISTER 1						LSB	R10
WRITE	0	1	0	0	0	1	MSB	DATA ROW START REGISTER						LSB	R11
WRITE	0	1	0	0	1	0	MSB	DATA ROW END/SEQUENTIAL BREAK REGISTER 2						LSB	R12
WRITE	0	1	0	0	1	1	MSB	AUXILIARY ADDRESS REGISTER 2 (LS BYTE)						LSB	R13
WRITE	0	1	0	1	0	0	ROW ATTRIBUTES	AUXILIARY ADDRESS REGISTER 2 (MS BYTE) MSB						LSB	R14

Table 3b: Control and Memory Address Registers

Register Type	ADDRESS DECODE VA5	VA4	VA3	VA2	VA1	VA0	BIT DEFINITION D7	D6	D5	D4	D3	D2	D1	D0	REGISTER NUMBER (HEX)
READ OR WRITE	0	1	0	1	0	1	START COMMAND								R15
READ OR WRITE	0	1	0	1	1	0	RESET COMMAND								R16
WRITE	0	1	0	1	1	1	OFFSET OVER-FLOW	OFFSET VALUE MSB					LSB	0	R17
WRITE	0	1	1	0	0	0	MSB	VERTICAL CURSOR REGISTER (ROW COORD.)						LSB	R18 or R38
READ	1	1	1	0	0	0									
WRITE	0	1	1	0	0	1	MSB	HORIZONTAL CURSOR REGISTER (COL. COORD.)						LSB	R19 or R39
READ	1	1	1	0	0	1									
WRITE	0	1	1	0	1	0	X	VER-TICAL RE-TRACE	INTERRUPT ENABLE REGISTER LIGHT PEN	X	X	X	X	FRAME TIMER	R1A
READ	1	1	1	0	1	0	INT PEND-ING	VER-TICAL RE-TRACE	LIGHT PEN	STATUS REGISTER			ODD/ EVEN	X FRAME TIMER	R3A
READ	1	1	1	0	1	1	MSB	VERTICAL LIGHT PEN REGISTER (ROW COORD.)						LSB	R3B
READ	1	1	1	1	0	0	MSB	HORIZONTAL LIGHT PEN REGISTER (COL. COORD.)						LSB	R3C

Table 3c: Cursor, Light Pen, Offset, and Status Registers

STANDARD MICROSYSTEMS CORPORATION

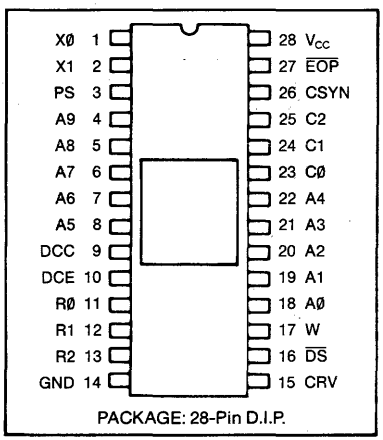
CRT 96364 A
CRT 96364 B
μPC FAMILY

CRT Controller

FEATURES

- ☐ Single +5v power supply
- ☐ 16 line x 64 character display
- ☐ On chip sync oscillator
- ☐ Complete cursor control
- ☐ Automatic scrolling
- ☐ Erase functions built in
- ☐ Performs character entry during horizontal sync
- ☐ Internal blinking cursor
- ☐ Page linking logic built in
- ☐ LS-TTL compatible
- ☐ Compatible with CRT 8002, CRT 7004

PIN CONFIGURATION



PACKAGE: 28-Pin D.I.P.

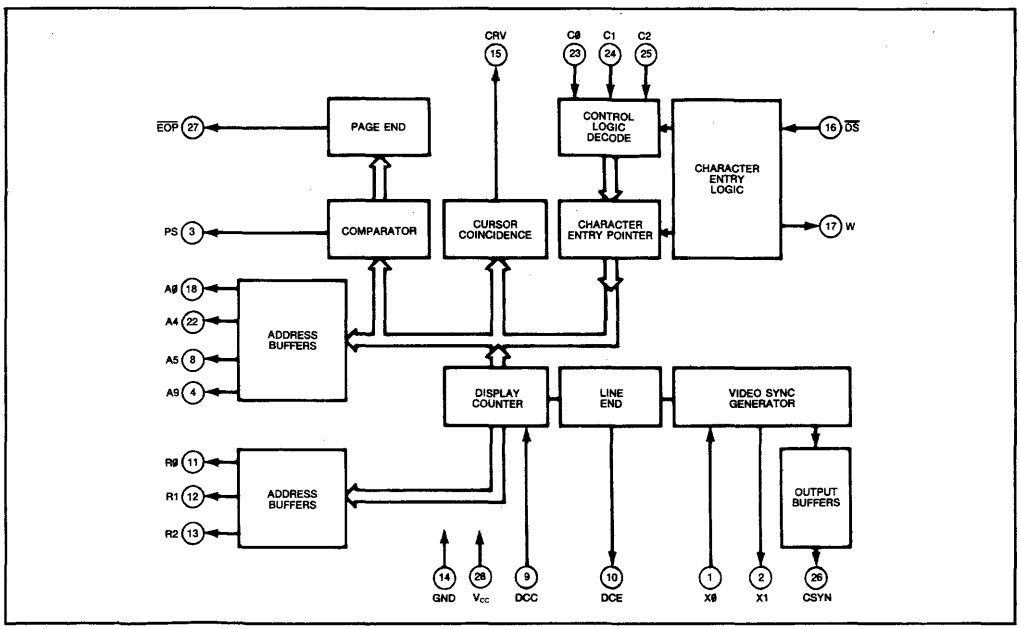
GENERAL DESCRIPTION

The CRT 96364 A/B is a CRT Controller which controls all of the functions associated with a 16 line x 64 character video display. Functions include CRT refresh, character entry, and cursor management.

The CRT 96364 A/B contains an internal oscillator which produces the composite sync output. The CRT 96364 B generates a 60 Hz vertical sync while the CRT 96364 A generates a 50 Hz vertical sync.

Standard functions such as ERASE PAGE, ERASE LINE, and ERASE TO END OF LINE make the CRT 96364 A/B easy to interface to any computer or microprocessor, or to use as a stand-alone video processor.

The CRT 96364 A/B requires only +5v power at less than 100 mA. It is manufactured in COPLAMOS® N channel silicon gate technology.



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1 2	Crystal in Crystal out	XØ X1	Pin one is the sync clock input. It may be driven directly from a TTL gate or from a parallel mode crystal connected between pins one and two. When a crystal is used, a 10 MΩ resistor should be connected in parallel. For standard 60 Hz line operation, a 1.018 MHz frequency source or crystal is required (with the CRT 96364B). For 50 Hz line operation, the CRT 96364A requires a 1.008 MHz crystal.
3	Page Select	PS	PS provides automatic page selection when two pages of memory are used. A "zero" output indicates selection of page 1; a logic "one" indicates page 2.
4-8	Memory Address	A9-A5	Upper order memory address lines; A6-A9 determine which lines of text are being refreshed or written. A5 along with AØ-A4 determine the character position.
9	Character Clock	DCC	Character clock input. Addresses are changed on the trailing edge of DCC.
10	Dot Clock Enable	DCE	A logic zero from DCE is used to inhibit oscillation of the dot clock for retrace blanking.
11-13	Row Address	RØ-R2	Character Generator row addresses. Blanks are generated by forcing RØ-R2 to "000". During character entry, R2 gates data into memory to control the erase function. Row addressing follows the sequence 0-1-2-3-4-5-6-7-0-0-0-0-increment text line-0-1-2-etc.
14	Ground	GND	Ground
15	Cursor	CRV	Cursor video output. Indicates cursor location by a 2 Hz blinking underline.
16	Data Strobe	$\overline{DS}$	The rising edge of $\overline{DS}$ strobes the appropriate CØ-C2 control word into the CRT 96364A/B.
17	Write	W	A positive going signal which indicates that the CRT 96364A/B is allowing a memory write. W is approximately 4 μs, and occurs during H sync. Memory address lines are latched at the cursor address during W.
18-22	Memory Address	AØ-A4	Lower order memory addresses. AØ-A4 plus A5 (pin 8) determine the character position.
23-25	Command Inputs	CØ-C2	Command inputs are strobed into the CRT 96364A/B by $\overline{DS}$. Functions are as follows: **Function** — C_2 C_1 C_0 Page erase and cursor home (top-left) — 0 0 0 Erase to end of line and return cursor (to left) — 0 0 1 Line feed (cursor down) — 0 1 0 No operation* — 0 1 1 Cursor left (one position) — 1 0 0 Erasure of cursor-line — 1 0 1 Cursor up (one position) — 1 1 0 Normal character. Write signal is generated and cursor position is incremented — 1 1 1 * In order to suppress non-displayed characters
26	Composite Sync	CSYN	Positive logic composite sync output. Horizontal sync is generated during VSYNC and $\overline{VSYNC}$ time. A vertical sync output may be generated by logically "ANDing" CSYN and DCE.
27	End of Page	$\overline{EOP}$	This output is used to increment an external page counter when using more than one page of memory.
28	Power Supply	V_{CC}	+ 5 volt supply.

OPERATION

The CRT 96364A/B provides all of the control functions required by a CRT display with a minimum of external circuitry.

The cursor and erase commands may be decoded from the data bus by a low cost 256 x 4 PROM. The CRT 96364A/B then provides the necessary cursor movement and gates the memory for writing or erasing. Erase is controlled by providing a write signal to RAM, and gating "zeros" to the RAM input bus. Use of an external PROM allows user selection of control words.

The RAM write command, "W", is generated during horizontal retrace. At this time, the RAM address is set to the cursor address. Immediately following the write command, the RAM addresses revert to refresh addressing and the cursor is shifted one character.

CURSOR

The cursor location is indicated by an alternating high on pin 15 (CRV) at row 7, and a low on pin 15 with RØ-R2 forced low at rows 0-6. These alternate at a 2 Hz rate. If CRV is used to force the display on, the result will be a blink of the cursor character position alternating with an underline at a 2 Hz rate.

CHARACTER ENTRY

When a Normal Character code (C2, C1, CØ = 1, 1, 1) and a Data Strobe are received, the write command will be generated during horizontal retrace. If, at the end of the horizontal retrace, the cursor is at the last position on a line, a carriage return and line feed will automatically occur. When the cursor is at the last position of the last line, a carriage return and up-scroll will automatically occur.

EXTRA FUNCTIONS

By using the fourth bit of the decoder PROM as a write enable signal, and properly programming the PROM, the additional commands of Home Cursor, Return Cursor, and Roll Screen may be generated. This is done by inhibiting the W signal to the page memory and inputting the control codes, respectively, of Page Erase and Home Cursor, Erase to end of line and Return Cursor, and Line Feed.

SCROLLING

Scrolling of the screen text will occur under any of the following characteristics:

1. Inputting a line feed command when the cursor is at the bottom line of the screen.
2. Inputting a character when the cursor is at the bottom right hand side of the screen.

Scrolling will result in the entire top line of the screen being erased and all of the remaining lines shifting up. Alternatively, a Roll (defined as all of the lines shifting up with the previous top line reappearing at the bottom of the screen) may be performed by inhibiting the write signal to the page memory as described in "Extra Functions."

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +7.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

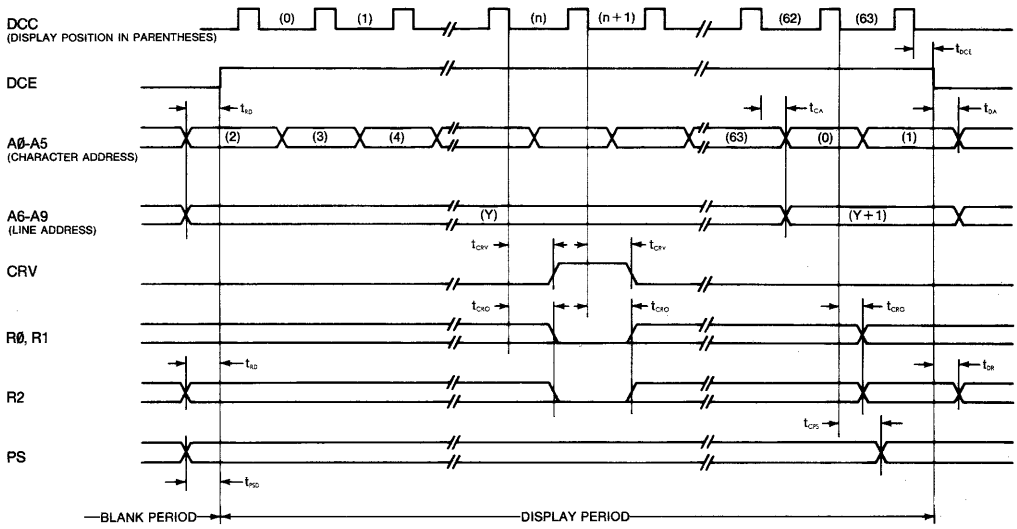
ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS (except DCC)					
Low-level, V_{IL}			0.65	V	excluding DCC
High-level, V_{IH}	2.2			V	excluding DCC
INPUT VOLTAGE LEVELS—DCC					
Low-level, V_{IL}			0.65	V	
High-level, V_{IH}	3.5			V	
OUTPUT VOLTAGE LEVELS (DCE Only)					
Low-level, V_{OL}			0.4	V	I_{OL}=1.9 mA
High-level, V_{OH}	2.2			V	I_{OH}=−100 μA
OUTPUT VOLTAGE LEVELS (except DCE)					
Low-level, V_{OL}			0.4	V	I_{OL}=0.36 mA
High-level, V_{OH}	2.2			V	I_{OH}=−100 μA
INPUT CURRENT					
Low-level, I_{IL}			10	μA	$0 \leq V_{IN} \leq +5V$
INPUT CAPACITANCE					
All inputs, C_{IN} (except DCE)		5		pF	V_{IN}=GND
C_{IN} (DCC Only)		25		pF	V_{IN}=GND
POWER SUPPLY CURRENT					
I_{CC}		100	120	mA	

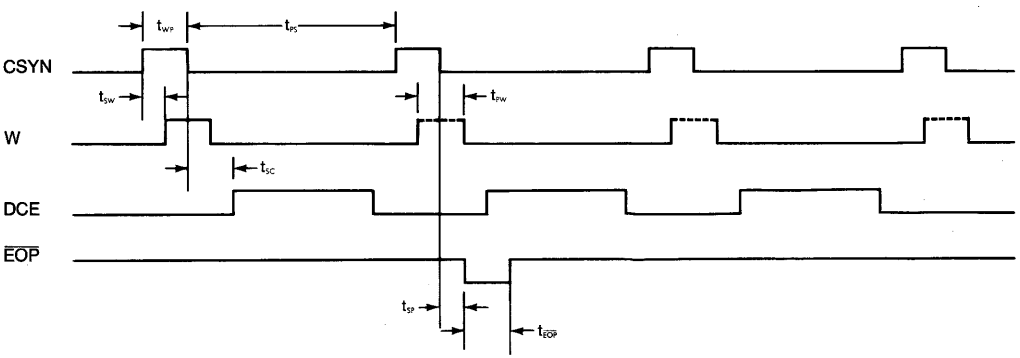
AC CHARACTERISTICS

PARAMETERS	SYMBOL	VALUES MIN.	VALUES TYP.	VALUES MAX.	UNIT
Frequency of control clock DCC	f_{DCC}		1.6		MHz
Crystal Frequency CRT 9364A	f_X		1.008		MHz
CRT 9364B	f_X		1.018		MHz
DCC pulse width	t_{DCC}	200			ns
Rise and fall times	t_r t_f		20	40	ns
Refresh memory address access time	t_{CA}		200	250	ns
Character memory address access time	t_{CRO}		200	250	ns
PS access time (read)	t_{CPS}		300	1000	ns
CRV access time	t_{CRV}		200	250	ns
DCE access time (high to low)	t_{DCE}		100		ns
SYNC period	t_{PS}		64		μs
SYNC pulse width	t_{WP}		4		μs
DCE access time (low to high level)	t_{SC}		11		μs
EOP access time (high to low level)	t_{SP}		1	1.5	μs
W access time (low to high)	t_{SW}		500	1000	ns
W pulse width	t_{PW}		4		μs
EOP pulse width	$t_{\overline{EOP}}$		10		μs
Address to rising edge of DCE delay	t_{AD}	0		2.1	μs
Falling edge of DCE to Address delay	t_{DA}	0		1	μs
Row to rising edge of DCE delay	t_{RD}	0		2.1	μs
Falling edge of DCE to row delay	t_{DR}	0		1	μs
PS to rising edge of DCE delay	t_{PSD}	0			μs

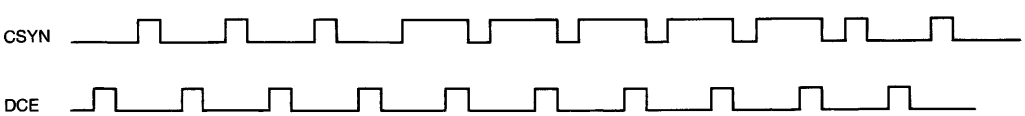
LINE TIMING



SYNC TIMING



FRAME TIMING



SECTION V

DATA INPUT TIMING

Asynchronous Operation

PARAMETER	SYMBOL	Value MIN	TYP	MAX	UNIT
DS Pulse Width	t_{PW}	0.5			μs
CØ-C2 Set Up Time	t_{CDS}	1			μs
CØ-C2 Hold Time	t_{DSC}	90			μs
Minimum Strobe Period (Operation Execution Time)	t_{DS}				

FUNCTION	C2	C1	CØ		
Page Erase & Cursor Home	0	0	0	132	ms
Erase to End of Line & Return Cursor	0	0	1	4.2	ms
Line Feed (Cursor Down)	0	1	0	130*	μs
No Operation	0	1	1	80	μs
Cursor Left	1	0	0	80	μs
Erasure of Cursor Line	1	0	1	8.3	ms
Cursor Up	1	1	0	80	μs
Normal Character	1	1	1	130*	μs

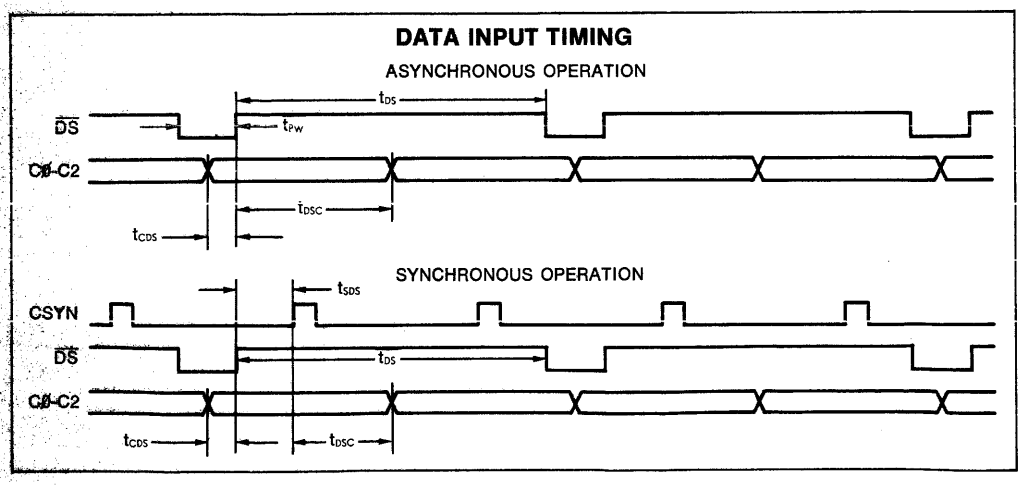
*Will increase to 8.3 ms when text scroll occurs. See "Scrolling" for conditions.

Synchronous Operation

PARAMETER	SYMBOL	Value MIN	TYP	MAX	UNIT
DS Pulse Width	t_{PW}	0.5			μs
C0-C2 Set-Up Time	t_{CDS}	1			μs
C0-C2 Hold Time	t_{DSC}	16			μs
DS Set Up Time	t_{SDS}	1			μs
Minimum Strobe Period (Operation Execution Time)	t_{DS}				

FUNCTION	C2	C1	CØ		
Page Erase & Cursor Home	0	0	0	132	ms
Erase to End of Line & Return Cursor	0	0	1	4.2	ms
Line Feed (Cursor Down)	0	1	0	64*	μs
No Operation	0	1	1	64	μs
Cursor Left	1	0	0	64	μs
Erasure of Cursor Line	1	0	1	8.3	ms
Cursor Up	1	1	0	64	μs
Normal Character	1	1	1	64*	μs

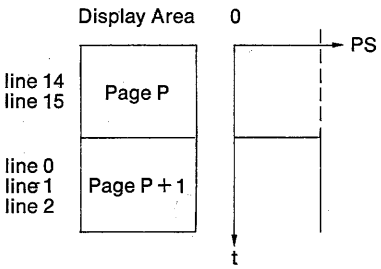
*Will increase to 8.3 ms when text scroll occurs. See "Scrolling" for conditions.



MULTIPLE PAGE DISPLAY

When linking two or more pages, the $\overline{EOP}$ and PS signals may be used to allow a "moving window" text display.

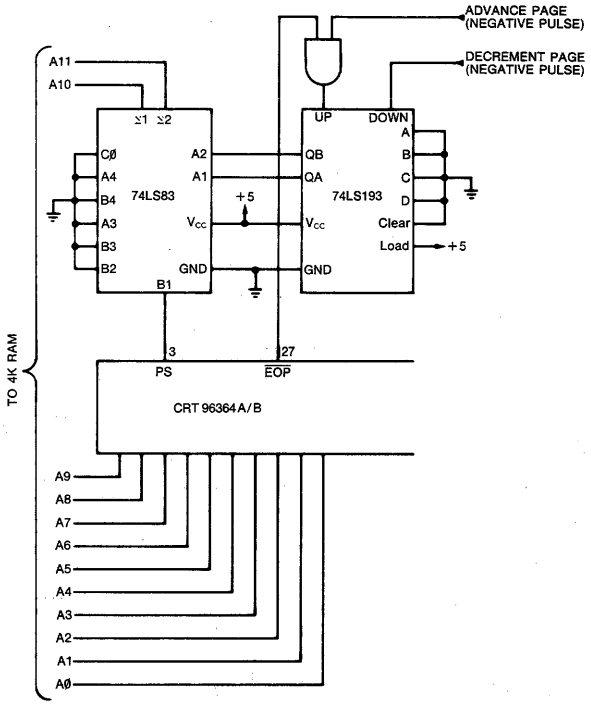
PS (Page Select) indicates the end of page location. If a scroll has occurred, PS will show the transition from the end of line 15 of page P and the beginning of line 0 of page P + 1.



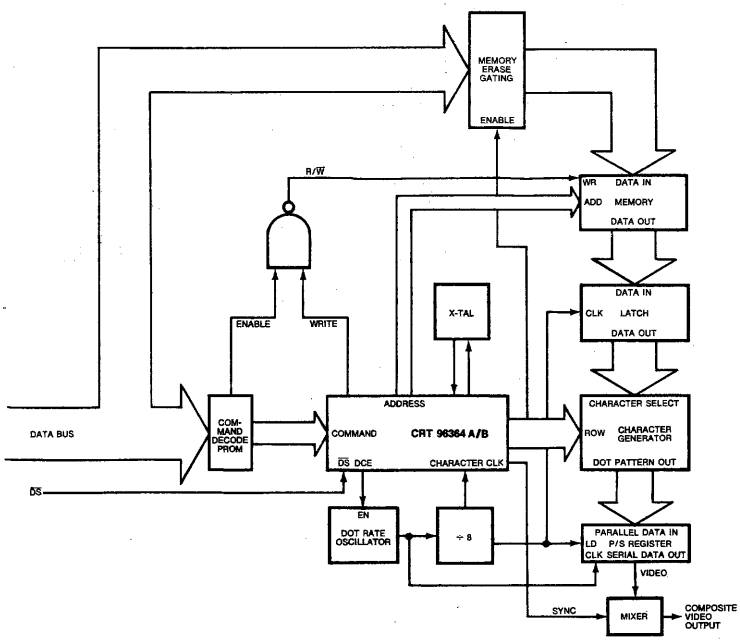
To properly maintain the memory address when displaying more than two pages, $\overline{EOP}$ pulses low at the point in time when page P is scrolled completely off the screen. At this time, PS will remain low for the entire frame since page P + 1 is now the only displayed page.

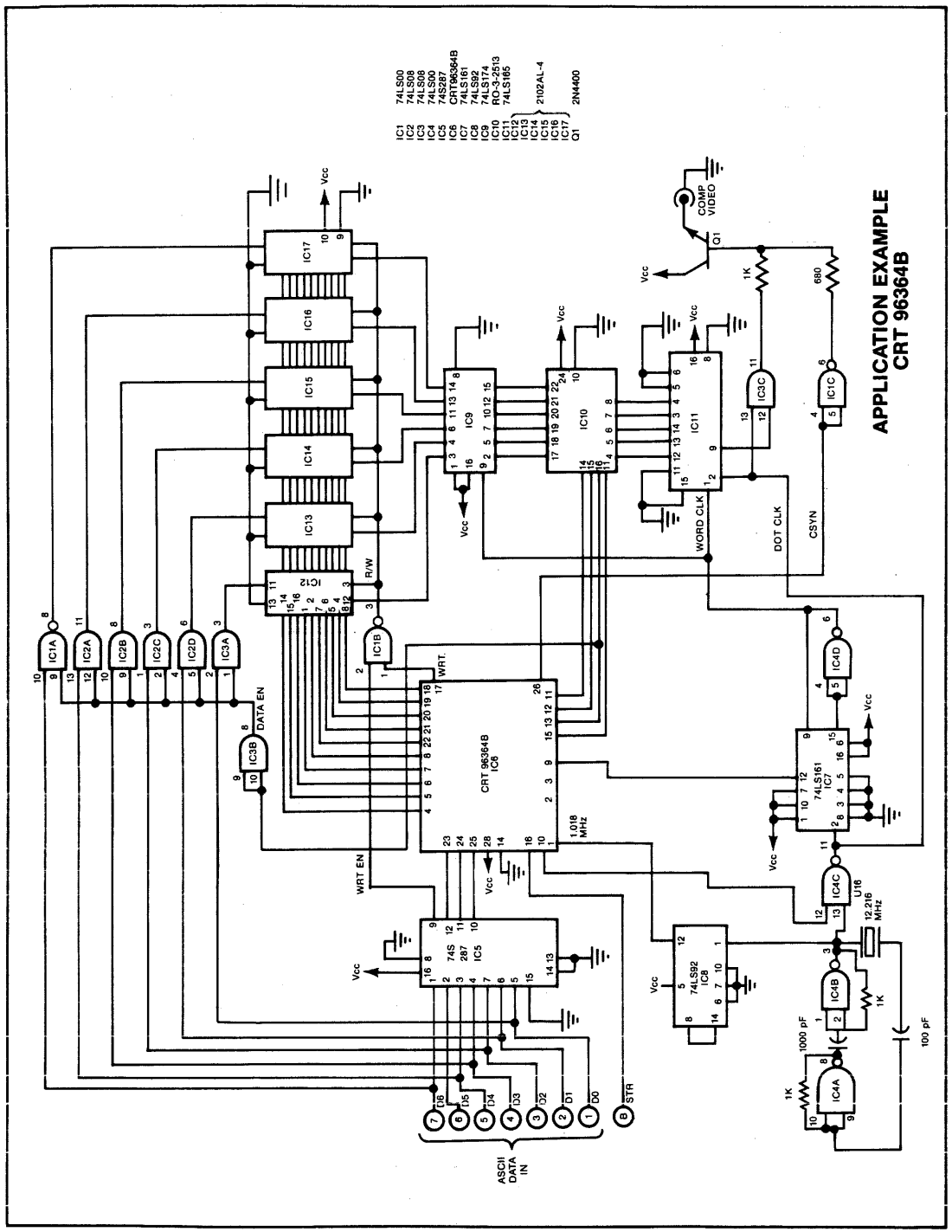
The circuit at the right will allow scrolling through 4 pages of memory.

4 PAGE DISPLAY



TYPICAL SYSTEM APPLICATION





STANDARD MICROSYSTEMS CORPORATION

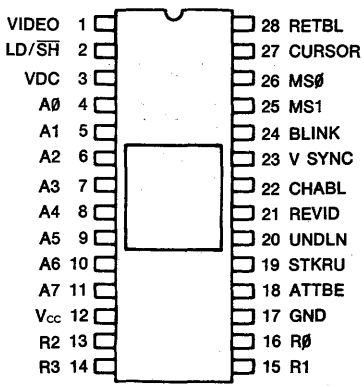
CRT 8002
μPC FAMILY

CRT Video Display Attributes Controller Video Generator VDAC™

FEATURES

- ☐ On chip character generator (mask programmable)
  - 128 Characters (alphanumeric and graphic)
  - 7 x 11 Dot matrix block
- ☐ On chip video shift register
  - Maximum shift register frequency
    - CRT 8002A 20MHz
    - CRT 8002B 15MHz
    - CRT 8002C 10MHz
    - Access time 400ns
- ☐ On chip horizontal and vertical retrace video blanking
- ☐ No descender circuitry required
- ☐ Four modes of operation (intermixable)
  - Internal character generator (ROM)
  - Wide graphics
  - Thin graphics
  - External inputs (fonts/dot graphics)
- ☐ On chip attribute logic—character, field
  - Reverse video
  - Character blank
  - Character blink
  - Underline
  - Strike-thru
- ☐ Four on chip cursor modes
  - Underline
  - Blinking underline
  - Reverse video
  - Blinking reverse video
- ☐ Programmable character blink rate
- ☐ Programmable cursor blink rate
- ☐ Subscriptable
- ☐ Expandable character set
  - External fonts
  - Alphanumeric and graphic
  - RAM, ROM, and PROM
- ☐ On chip address buffer
- ☐ On chip attribute buffer
- ☐ +5 volt operation
- ☐ TTL compatible
- ☐ MOS N-channel silicon-gate COPLAMOS® process
- ☐ CLASP® technology—ROM and options
- ☐ Compatible with CRT 5027 VTAC®

PIN CONFIGURATION



SECTION V

General Description

The SMC CRT 8002 Video Display Attributes Controller (VDAC) is an N-channel COPLAMOS® MOS/LSI device which utilizes CLASP® technology. It contains a 7X11X128 character generator ROM, a wide graphics mode, a thin graphics mode, an external input mode, character address/data latch, field and/or character attribute logic, attribute latch, four cursor modes, two programmable blink rates, and a high speed video shift register. The CRT 8002 VDAC is a companion chip to SMC's CRT 5027 VTAC®. Together these two chips comprise the circuitry required for the display portion of a CRT video terminal.

The CRT 8002 video output may be connected directly to a CRT monitor video input. The CRT 5027 blanking output can be connected directly to the CRT 8002 retrace blank input to provide both horizontal and vertical retrace blanking of the video output.

Four cursor modes are available on the CRT 8002. They are: underline, blinking underline, reverse video block, and blinking reverse video block. Any one of these can be mask programmed as the cursor function. There is a separate cursor blink rate which can be mask programmed to provide a 15 Hz to 2 Hz blink rate.

The CRT 8002 attributes include: reverse video, character blank, blink, underline, and strike-thru. The character blink rate is mask programmable from 7.5 Hz to 1.0 Hz and has a duty cycle of 75/25. The underline and strike-thru are similar but independently controlled functions and can be mask programmed to any number of raster lines at any position in the character block. These attributes are available in all modes.

In the wide graphic mode the CRT 8002 produces a graphic entity the size of the character block. The graphic entity contains 8 parts, each of which is associated with one bit of a graphic byte, thereby providing for 256 unique graphic symbols. Thus, the CRT 8002 can produce either an alphanumeric symbol or a graphic entity depending on the mode selected. The mode can be changed on a per character basis.

The thin graphic mode enables the user to create single line drawings and forms.

The external mode enables the user to extend the on-chip ROM character set and/or the on-chip graphics capabilities by inserting external symbols. These external symbols can come from either RAM, ROM or PROM.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

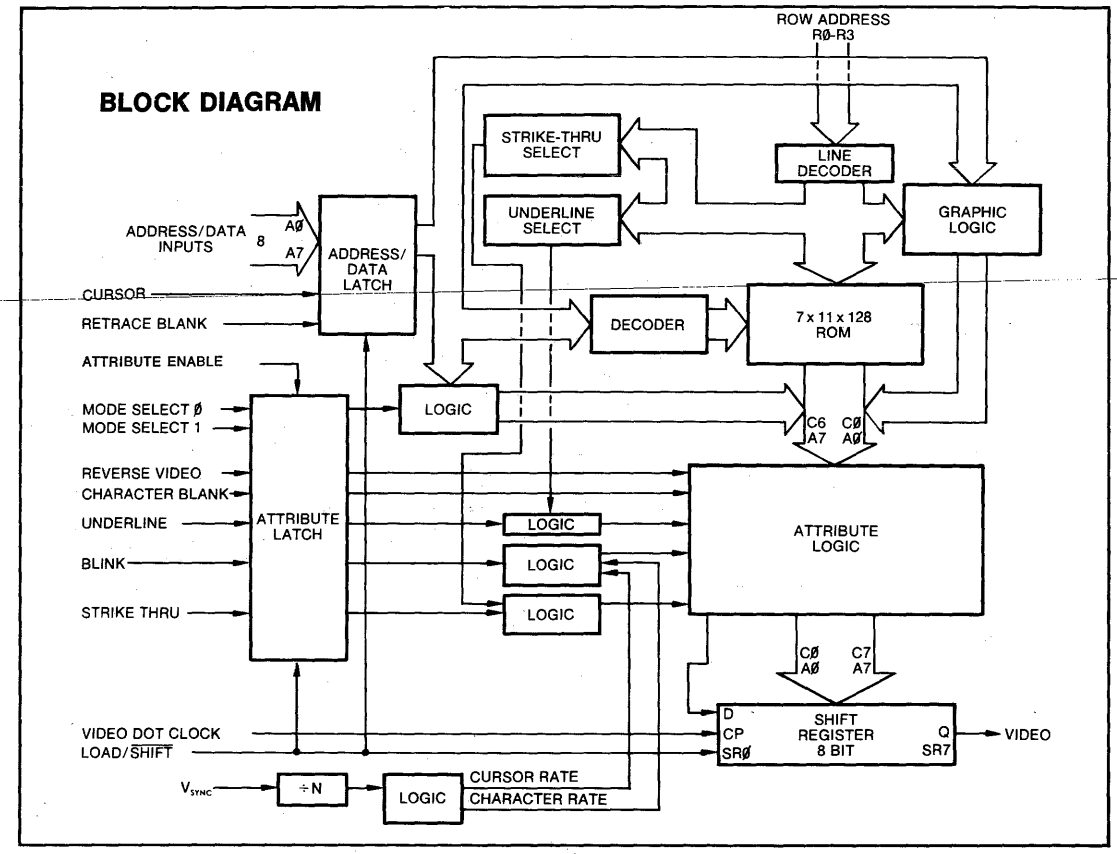
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}= +5V ±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	excluding VDC
High-level, V_{IH}	2.0			V	excluding VDC
INPUT VOLTAGE LEVELS-CLOCK					
Low-level, V_{IL}			0.8	V	
High-level, V_{IH}	4.3			V	See Figure 6
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL}=0.4 mA, 74LSXX load
High-level, V_{OH}	2.4			V	I_{OH}=−20μA
INPUT CURRENT					
Leakage, I_L (Except CLOCK)			10	μA	$0 \leq V_{IN} \leq V_{CC}$
Leakage, I_L (CLOCK Only)			50	μA	$0 \leq V_{IN} \leq V_{CC}$
INPUT CAPACITANCE					
Data		10		pF	@ 1 MHz
LD/$\overline{SH}$		20		pF	@ 1 MHz
CLOCK		25		pF	@ 1 MHz
POWER SUPPLY CURRENT					
I_{CC}		100		mA	
A.C. CHARACTERISTICS					
See Figure 6, 7					

SYMBOL	PARAMETER	CRT 8002A		CRT 8002B		CRT 8002C		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
VDC	Video Dot Clock Frequency	1.0	20	1.0	15	1.0	10	MHz
PW_H	VDC—High Time	15.0		23		40		ns
PW_L	VDC—Low Time	15.0		23		40		ns
t_{CY}	LD/$\overline{SH}$ cycle time	400		533		800		ns
t_r, t_f	Rise, fall time		10		10		10	ns
t_{SET-UP}	Input set-up time	≥0		≥0		≥0		ns
t_{HOLD}	Input hold time	15		15		15		ns
t_{PDI}, t_{PDO}	Output propagation delay	15	50	15	65	15	100	ns
t_1	LD/$\overline{SH}$ set-up time	10		15		20		ns
t_2	LD/$\overline{SH}$ hold time	5		5		5		ns



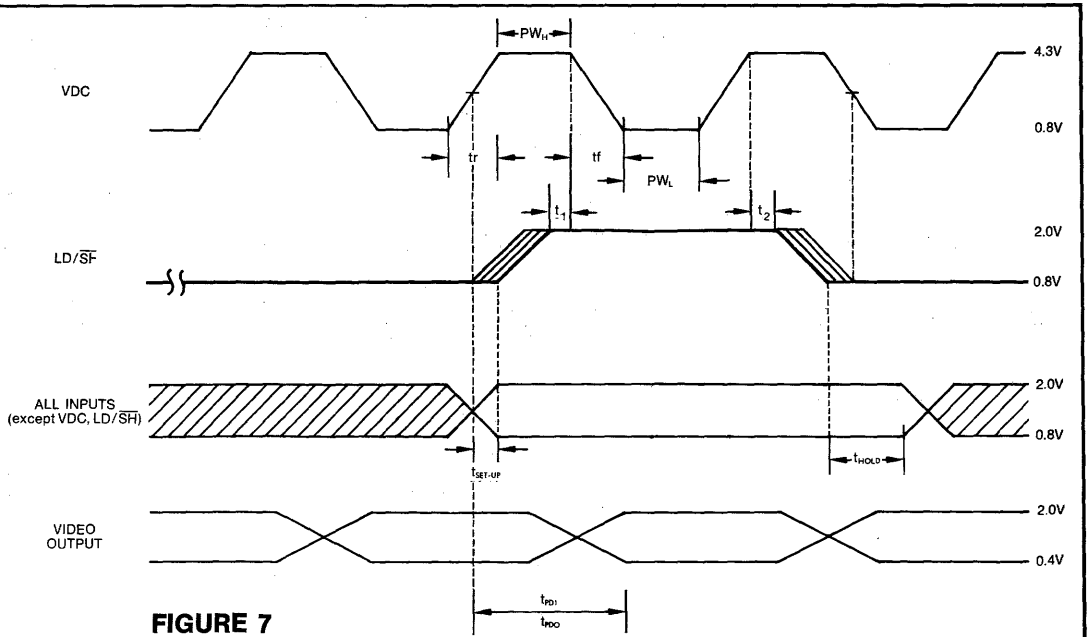


FIGURE 7
AC TIMING DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
1	VIDEO	Video Output	O	The video output contains the dot stream for the selected row of the alpha-numeric, wide graphic, thin graphic, or external character after processing by the attribute logic, and the retrace blank and cursor inputs. In the alphanumeric mode, the characters are ROM programmed into the 77 dots, (7X11) allocated for each of the 128 characters. See figure 5. The top row (RØ) and rows R12 to R15 are normally all zeros as is column C7. Thus, the character is defined in the box bounded by R1 to R11 and CØ to C6. When a row of the ROM, via the attribute logic, is parallel loaded into the 8-bit shift-register, the first bit serially shifted out is C7 (A zero; or a one in REVID). It is followed by C6, C5, through CØ. The timing of the Load/$\overline{\text{Shift}}$ pulse will determine the number of additional (— —, zero to N) backfill zeros (or ones if in REVID) shifted out. See figure 4. When the next Load/$\overline{\text{Shift}}$ pulse appears the next character's row of the ROM, via the attribute logic, is parallel loaded into the shift register and the cycle repeats.
2	LD/$\overline{\text{SH}}$	Load/$\overline{\text{Shift}}$	I	The 8 bit shift-register parallel-in load or serial-out shift modes are established by the Load/$\overline{\text{Shift}}$ input. When low, this input enables the shift register for serial shifting with each Video Dot Clock pulse. When high, the shift register parallel (broadside) data inputs are enabled and synchronous loading occurs on the next Video Dot Clock pulse. During parallel loading, serial data flow is inhibited. The Address/Data inputs (AØ-A7) are latched on the negative transition of the Load/$\overline{\text{Shift}}$ input. See timing diagram, figure 7.
3	VDC	Video Dot Clock	I	Frequency at which video is shifted.
4-11	AØ-A7	Address/Data	I	In the Alphanumeric Mode the 7 bits on inputs (AØ-A6) are internally decoded to address one of the 128 available characters (A7 = X). In the External Mode, AØ-A7 is used to insert an 8 bit word from a user defined external ROM, PROM or RAM into the on-chip Attribute logic. In the wide Graphic Modes AØ-A7 is used to define one of 256 graphic entities. In the thin Graphic Mode AØ-A2 is used to define the 3 line segments.
12	V_{CC}	Power Supply	PS	+5 volt power supply
13,14,15,16	R2,R3,R1,RØ	Row Address	I	These 4 binary inputs define the row address in the current character block.
17	GND	Ground	GND	Ground
18	ATTBE	Attribute Enable	I	A positive level on this input enables data from the Reverse Video, Character Blank, Underline, Strike-Thru, Blink, Mode Select Ø, and Mode Select 1 inputs to be strobed into the on-chip attribute latch at the negative transition of the Load/$\overline{\text{Shift}}$ pulse. The latch loading is disabled when this input is low. The latched attributes will remain fixed until this input becomes high again. To facilitate attribute latching on a character by character basis, tie ATTBE high. See timing diagram, figure 7.
19	STKRU	Strike-Thru	I	When this input is high and RETBL = 0, the parallel inputs to the shift register are forced high (SRØ-SR7), providing a solid line segment throughout the character block. The operation of strike-thru is modified by Reverse Video (see table 1). In addition, an on-chip ROM programmable decoder is available to decode the line count on which strike-thru is to be placed as well as to program the strike-thru to be 1 to N raster lines high. Actually, the strike-thru decoder (mask programmable) logic allows the strike-thru to be any number or arrangement of horizontal lines in the character block. The standard strike-thru will be a double line on rows R5 and R6.
20	UNDLN	Underline	I	When this input is high and RETBL = 0, the parallel inputs to the shift register are forced high (SRØ-SR7), providing a solid line segment throughout the character block. The operation of underline is modified by Reverse Video (see table 1). In addition, an on-chip ROM programmable decoder is available to decode the line count on which underline is to be placed as well as to program the underline to be 1 to N raster lines high. Actually, the underline decoder (mask programmable) logic allows the underline to be any number or arrangement of horizontal lines in the character block. The standard under-line will be a single line on R11.
21	REVID	Reverse Video	I	When this input is low and RETBL = 0, data into the Attribute Logic is presented directly to the shift register parallel inputs. When reverse video is high data into the Attribute Logic is inverted and then presented to the shift register parallel inputs. This operation reverses the data and field video. See table 1.
22	CHABL	Character Blank	I	When this input is high, the parallel inputs to the shift register are all set low, providing a blank character line segment. Character blank will override blink. The operation of Character Blank is modified by the Reverse Video input. See table 1.
23	V SYNC	V SYNC	I	This input is used as the clock input for the two on-chip mask programmable blink rate dividers. The cursor blink rate (50/50 duty cycle) will be twice the character blink rate (75/25 duty cycle). The divisors can be programmed from ÷ 4 to ÷ 30 for the cursor (÷ 8 to ÷ 60 for the character).
24	BLINK	Blink	I	When this input is high and RETBL = 0 and CHABL = 0, the character will blink at the programmed character blink rate. Blinking is accomplished by blanking the character block with the internal Character Blink clock. The standard character blink rate is 1.875 Hz.
25 26	MS1 MSØ	Mode Select 1 Mode Select Ø	I I	These 2 inputs define the four modes of operation of the CRT 8002 as follows: Alphanumeric Mode — In this mode addresses AØ-A6 (A7 = X) are internally decoded to address 1 of the 128 available ROM characters. The addressed character along with the decoded row will define a 7 bit output from the ROM to be loaded into the shift register via the attribute logic. Thin Graphics Mode — In this mode AØ-A2 (A3-A7 = X) will be loaded into the thin graphic logic along with the row addresses. This logic will define the segments of a graphic entity as defined in figure 2. The top of the entity will begin on row 0000 and will end on a mask programmable row.

MS1	MSØ	MODE
1	1	Alphanumeric
1	0	Thin Graphics
0	1	External Mode
0	0	Wide Graphics

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
25 26 (cont.)				External Mode – In this mode the inputs AØ-A7 go directly from the character latch into the shift register via the attribute logic. Thus the user may define external character fonts or graphic entities in an external PROM. ROM or RAM. See figure 3. Wide Graphics Mode—In this mode the inputs AØ-A7 will define a graphic entity as described in figure 1. Each line of the graphic entity is determined by the wide graphic logic in conjunction with the row inputs RØ to R3. In this mode each segment of the entity is defined by one of the bits of the 8 bit word. Therefore, the 8 bits can define any 1 of the 256 possible graphic entities. These entities can butt up against each other to form a contiguous pattern or can be interspaced with alphanumeric characters. Each of the entities occupies the space of 1 character block and thus requires 1 byte of memory. These 4 modes can be intermixed on a per character basis.
27	CURSOR	Cursor	I	When this input is enabled 1 of the 4 pre-programmed cursor modes will be activated. The cursor mode is on-chip mask programmable. The standard cursor will be a blinking (at 3.75Hz) reverse video block. The 4 cursor modes are: Underline—In this mode an underline (1 to N raster lines) at the programmed underline position occurs. Blinking Underline—In this mode the underline blinks at the cursor rate. Reverse Video Block—In this mode the Character Block is set to reverse video. Blinking Reverse Video Block—In this mode the Character Block is set to reverse video at the cursor blink rate. The Character Block will alternate between normal video and reverse video. The cursor functions are listed in table 1.
28	RETBL	Retrace Blank	I	When this input is latched high, the shift register parallel inputs are unconditionally cleared to all zeros and loaded into the shift register on the next Load/Shift pulse. This blanks the video, independent of all attributes, during horizontal and vertical retrace time.

TABLE 1

CURSOR	RETBL	REVID	CHABL	UNDLN*	FUNCTION
X	1	X	X	X	"0" S.R. All
0	0	0	0	0	D (S.R.) All
0	0	0	0	1	"1" (S.R.)*
					D (S.R.) All others
0	0	0	1	X	"0" (S.R.) All
0	0	1	0	0	D (S.R.) All
0	0	1	0	1	"0" (S.R.)*
					D (S.R.) All others
0	0	1	1	X	"1" (S.R.) All
Underline*	0	0	0	X	"1" (S.R.)*
					D (S.R.) All others
Underline*	0	0	1	X	"1" (S.R.)*
					"0" (S.R.) All others
Underline*	0	1	0	X	"0" (S.R.)*
					D (S.R.) All others
Underline*	0	1	1	X	"0" (S.R.)*
					"1" (S.R.) All others
Blinking** Underline*	0	0	0	X	"1" (S.R.)* Blinking
					D (S.R.) All others
Blinking** Underline*	0	0	1	X	"1" (S.R.)* Blinking
					"0" (S.R.) All others
Blinking** Underline*	0	1	0	X	"0" (S.R.)* Blinking
					D (S.R.) All others
Blinking** Underline*	0	1	1	X	"0" (S.R.)* Blinking
					"1" (S.R.) All others
REVID Block	0	0	0	0	D (S.R.) All
REVID Block	0	0	0	1	"0" (S.R.)*
					D (S.R.) All others
REVID Block	0	0	1	X	"1" (S.R.) All
REVID Block	0	0	0	1	"0" (S.R.)*
					D (S.R.) All others
REVID Block	0	1	0	0	D (S.R.) All
REVID Block	0	1	0	1	"1" (S.R.)*
					D (S.R.) All others
REVID Block	0	1	1	X	"0" (S.R.) All
Blink** REVID Block	0	0	0	0	Alternate Normal Video/REVID At Cursor Blink Rate
Blink** REVID Block	0	0	0	1	
Blink** REVID Block	0	0	1	X	
Blink** REVID Block	0	1	0	0	
Blink** REVID Block	0	1	0	1	
Blink** REVID Block	0	1	1	X	

*At Selected Row Decode **At Cursor Blink Rate

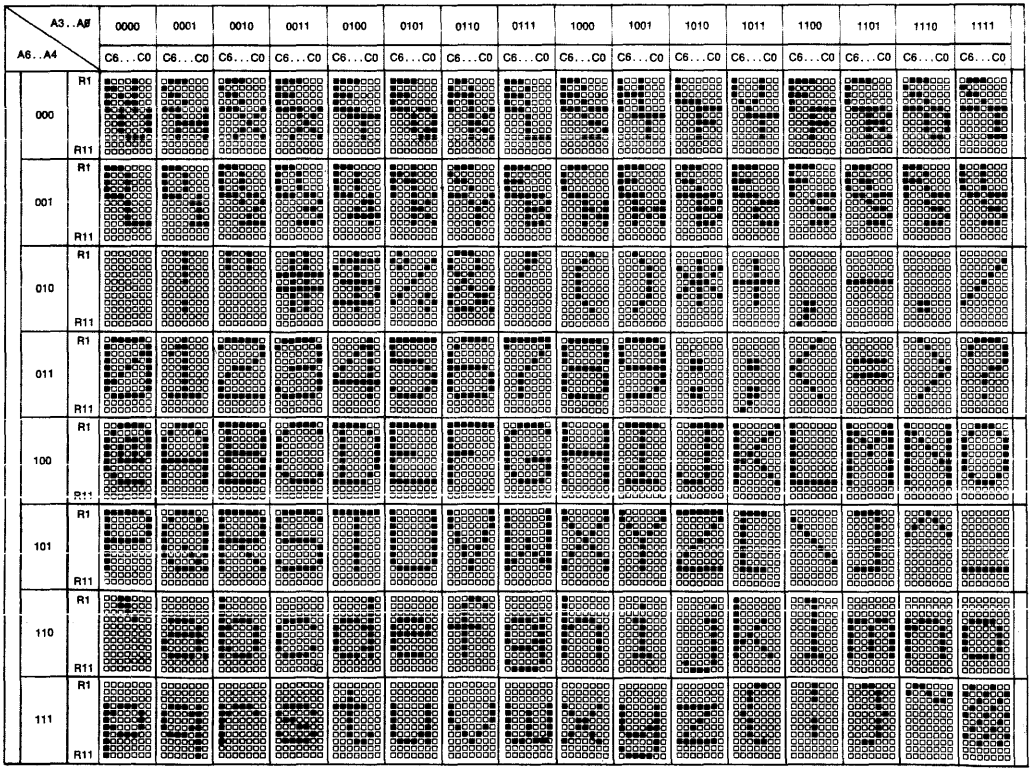
Note: If Character is Blinking at Character Rate, Cursor will change it to Cursor Blink Rate.

FIGURE 5
ROM CHARACTER BLOCK FORMAT

											ROWS	R3	R2	R1	RØ
(ALL ZEROS) →	0	0	0	0	0	0	0	0	—	—	RØ	0	0	0	0
	0	0	0	0	0	0	0	0	—	—	R1	0	0	0	1
	0	0	0	0	0	0	0	0	—	—	R2	0	0	1	0
	0	0	0	0	0	0	0	0	—	—	R3	0	0	1	1
	0	0	0	0	0	0	0	0	—	—	R4	0	1	0	0
	0	0	0	0	0	0	0	0	—	—	R5	0	1	0	1
77 BITS (7 x 11 ROM)	0	0	0	0	0	0	0	0	—	—	R6	0	1	1	0
	0	0	0	0	0	0	0	0	—	—	R7	0	1	1	1
	0	0	0	0	0	0	0	0	—	—	R8	1	0	0	0
	0	0	0	0	0	0	0	0	—	—	R9	1	0	0	1
	0	0	0	0	0	0	0	0	—	—	RIØ	1	0	1	0
	0	0	0	0	0	0	0	0	—	—	R11	1	0	1	1
	0	0	0	0	0	0	0	0	—	—	R12	1	1	0	0
	0	0	0	0	0	0	0	0	—	—	R13	1	1	0	1
(ALL ZEROS)	0	0	0	0	0	0	0	0	—	—	R14	1	1	1	0
	0	0	0	0	0	0	0	0	—	—	R15	1	1	1	1
	*C7	C6	C5	C4	C3	C2	C1	CØ	—	—					

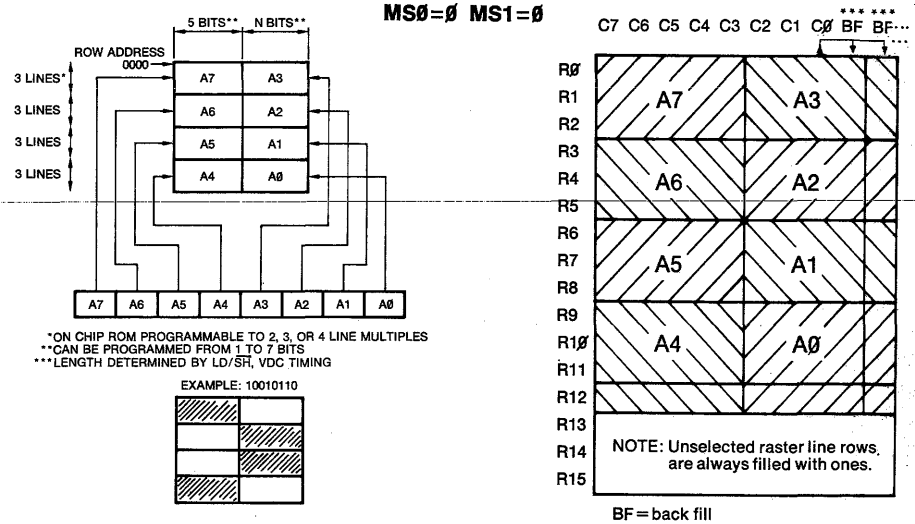
EXTENDED ZEROS (BACK FILL) FOR INTERCHARACTER SPACING (NUMBER CONTROLLED BY LD/SH, VDC TIMING)

*COLUMN 7 IS ALL ZEROS (REVID = 0)
COLUMN 7 IS SHIFTED OUT FIRST



CONSULT FACTORY FOR CUSTOM FONT AND OPTION PROGRAMMING FORMS.

FIGURE 1
WIDE GRAPHICS MODE
MSØ=Ø MS1=Ø

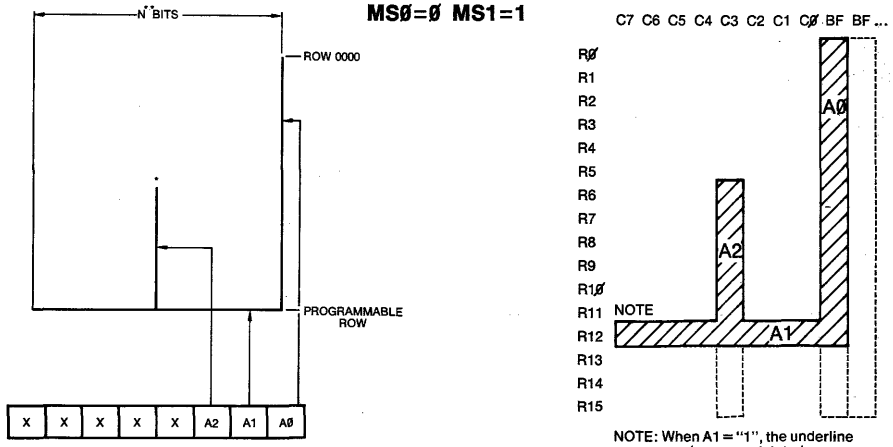


*ON CHIP ROM PROGRAMMABLE TO 2, 3, OR 4 LINE MULTIPLES
**CAN BE PROGRAMMED FROM 1 TO 7 BITS
***LENGTH DETERMINED BY LD/$\overline{SR}$, VDC TIMING

EXAMPLE: 10010110

BF = back fill

FIGURE 2
THIN GRAPHICS MODE
MSØ=Ø MS1=1



X = DON'T CARE
* THE INSIDE SEGMENT IS MASK PROGRAMMABLE TO ROW 0000
** LENGTH DETERMINED BY LD/$\overline{SR}$, VDC TIMING

NOTE: When A1 = "1", the underline row/rows are deleted.
When A1 = "0", the underline, if selected, will appear.

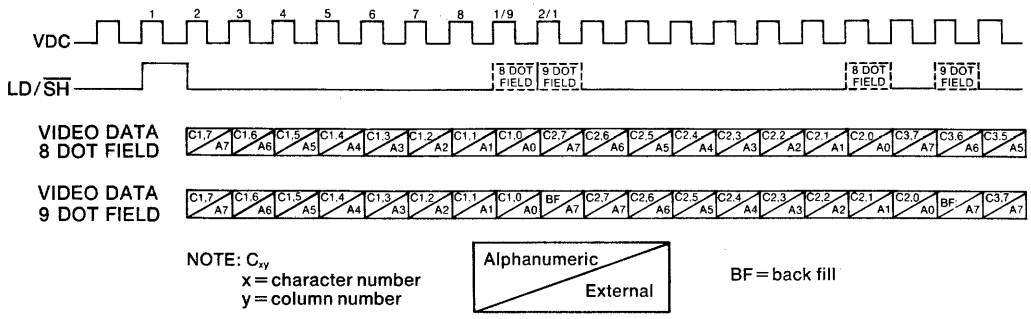
BF = back fill

FIGURE 3
EXTERNAL MODE
MSØ=1 MS1=Ø

	C7	C6	C5	C4	C3	C2	C1	CØ	BF	BF	···
RØ – R15	A7	A6	A5	A4	A3	A2	A1	AØ	A7	A7	···

BF = back fill

FIGURE 4 TYPICAL VIDEO OUTPUT



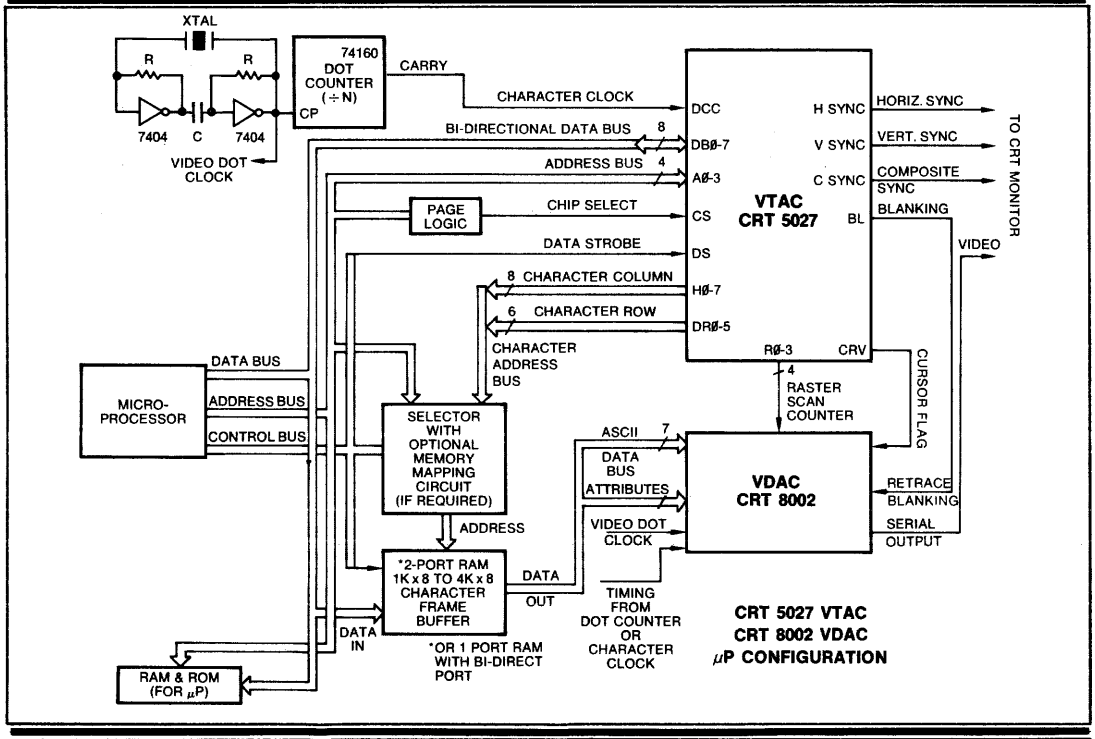
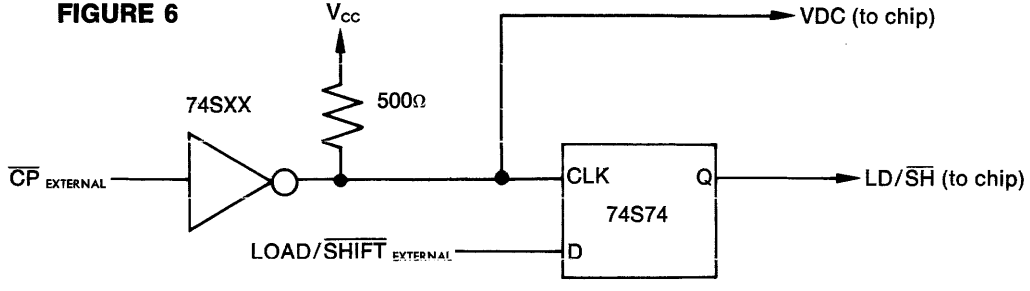


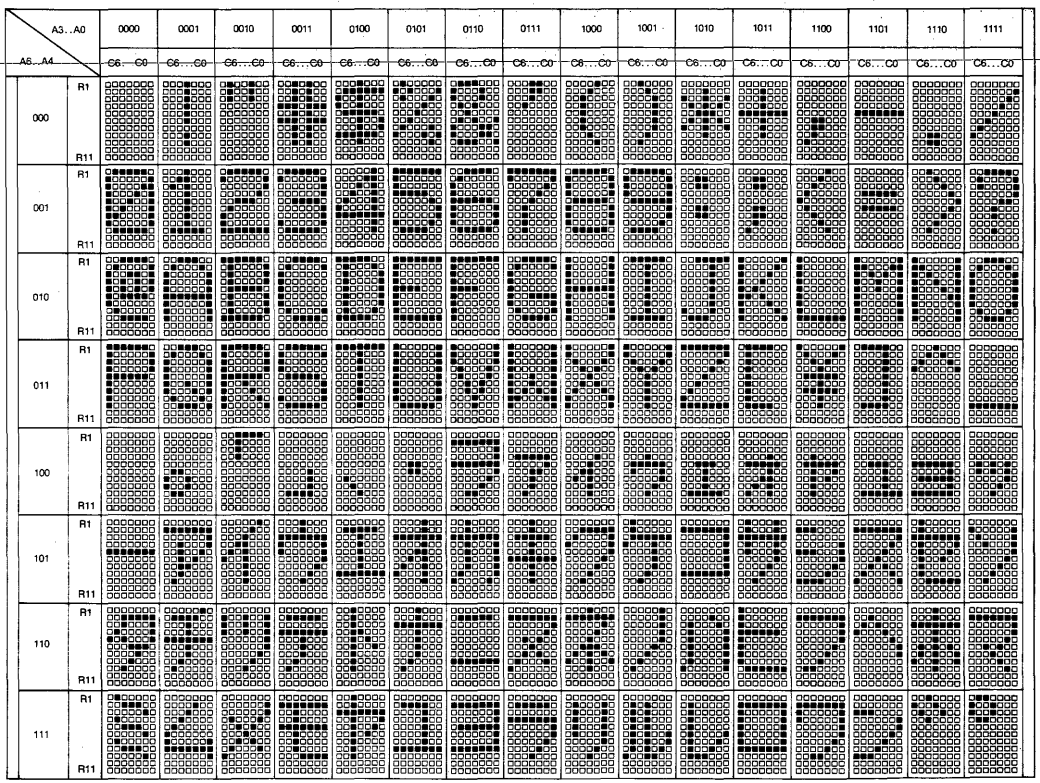
FIGURE 6

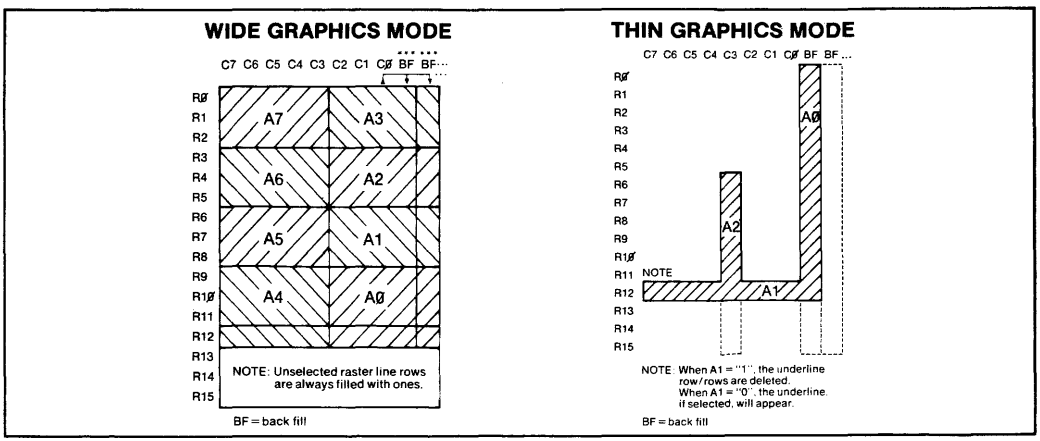


STANDARD MICROSYSTEMS CORPORATION

CRT 8002-001 (KATAKANA) CODING INFORMATION

CRT Video Display-Controller Video Generator VDAC™





ATTRIBUTES

Underline
Underline will be a single horizontal line at row R11

Cursor
Cursor will be a blinking reverse video block, blinking at 3.75 Hz

Blink Rate
The character blink rate will be 1.875 Hz

Strike-Thru
The strike-thru will be a double line at rows R5 and R6

SECTION V

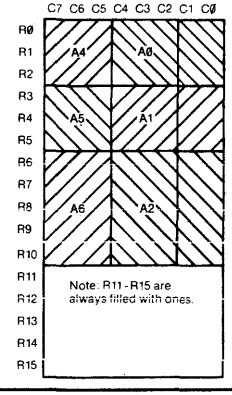
STANDARD MICROSYSTEMS CORPORATION

CRT 8002-003
(5 X 7 ASCII)
CODING INFORMATION

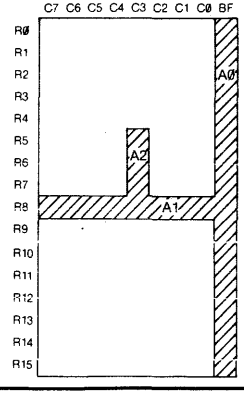
CRT Video Display-Controller Video Generator VDAC™

A6..A4 \ A3..A0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0	C6...C0
000	R1 ... R11															
001	R1 ... R11															
010	R1 ... R11															
011	R1 ... R11															
100	R1 ... R11															
101	R1 ... R11															
110	R1 ... R11															
111	R1 ... R11															

WIDE GRAPHICS MODE



THIN GRAPHICS MODE



ATTRIBUTES

Underline
Underline will be a single horizontal line at R8

Cursor
Cursor will be a blinking reverse video block, blinking at 3.75 Hz

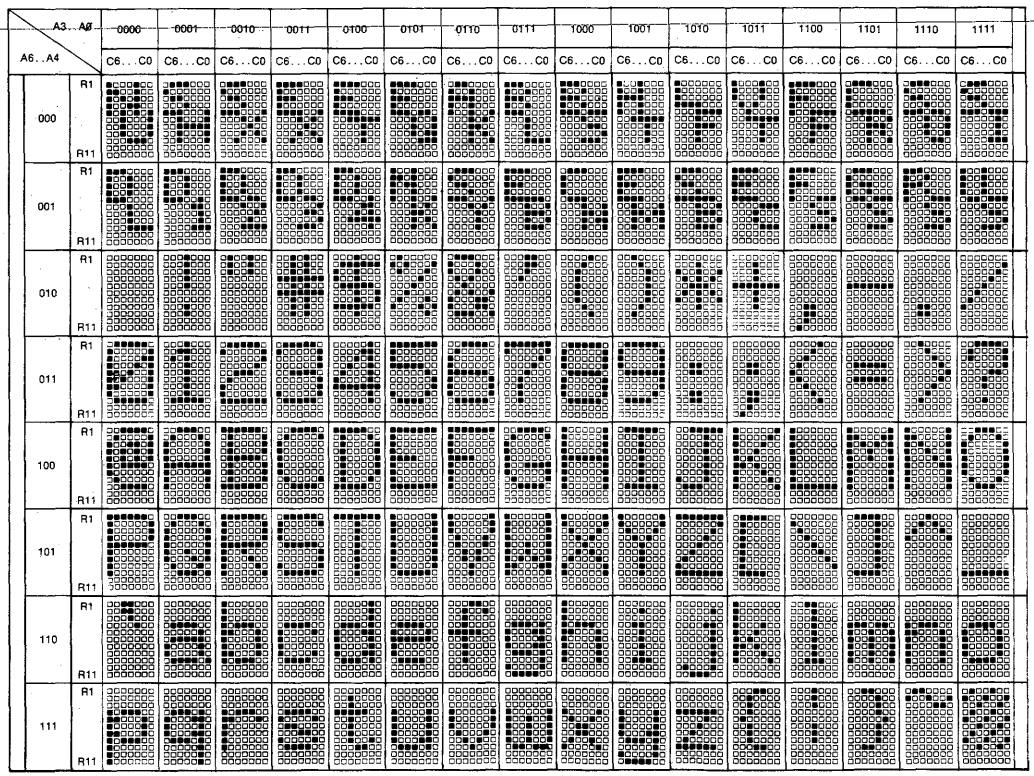
Blink Rate
The character blink rate is 1.875 Hz

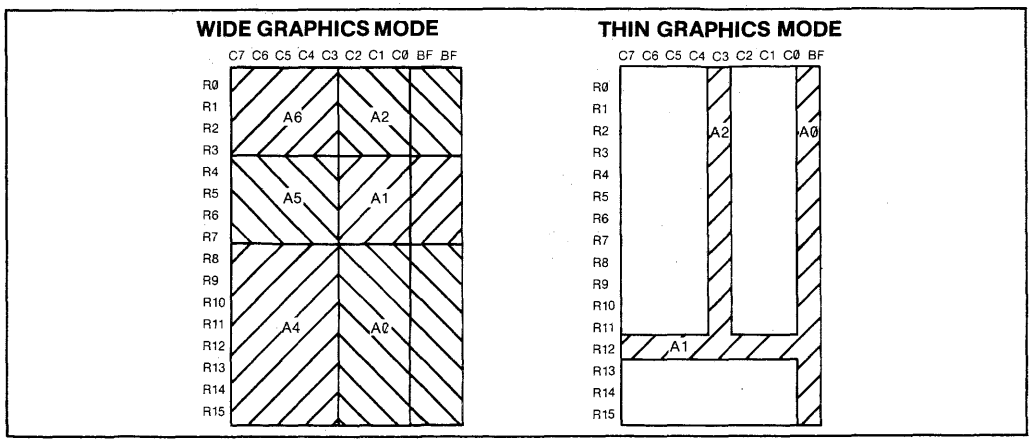
Strike-Thru
The strike-thru will be a single horizontal line at R4

STANDARD MICROSYSTEMS CORPORATION

CRT 8002-005 (ASCII) CODING INFORMATION

CRT Video Display-Controller Video Generator VDAC™





ATTRIBUTES

Underline
Underline will be a single horizontal line at R12

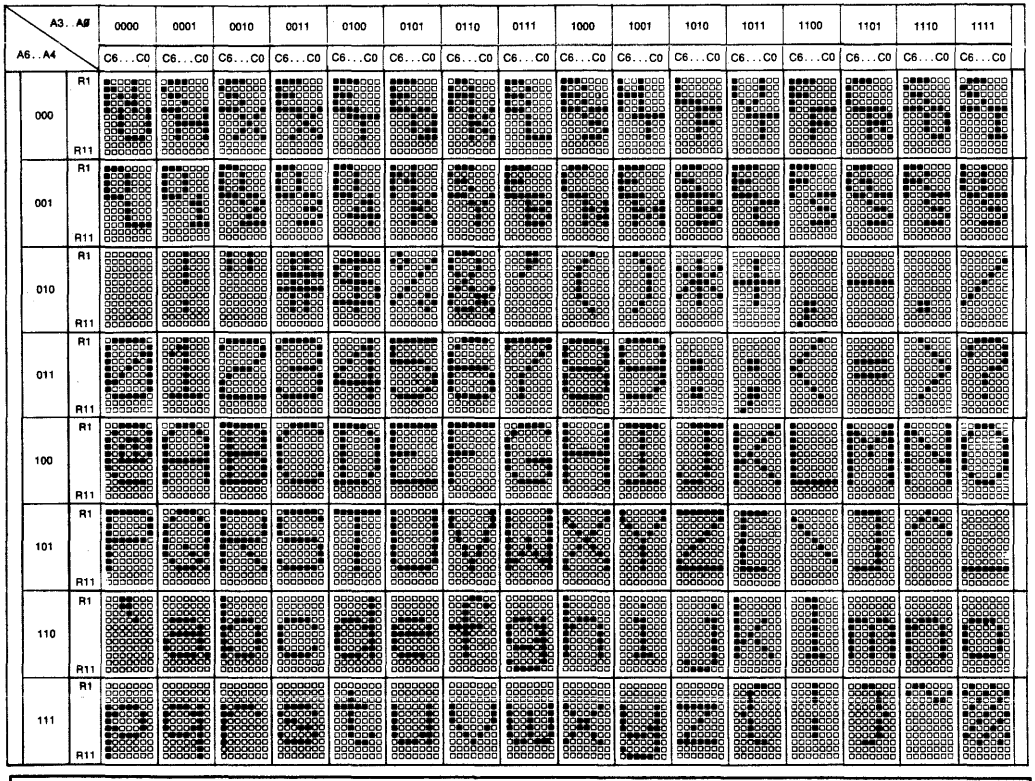
Cursor
Cursor will be a reverse video block

Blink Rate
The character blink rate is 1.875 Hz

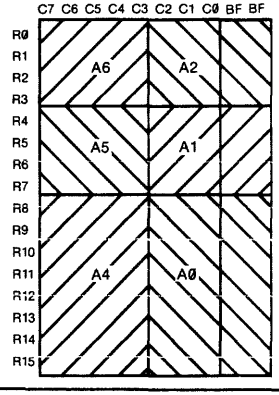
Strike-Thru
The strike-thru will be a double line at rows R5 and R6

CRT 8002-011
(ASCII)
CODING INFORMATION

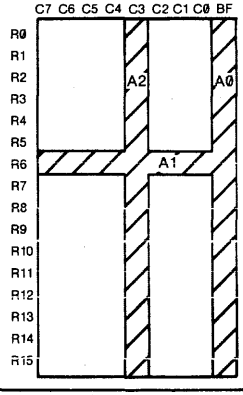
CRT Video Display-Controller Video Generator VDAC™



WIDE GRAPHICS MODE



THIN GRAPHICS MODE



ATTRIBUTES

Underline
Underline will be a single horizontal line at R11

Cursor
Cursor will be a blinking reverse video block, blinking at 3.75 Hz

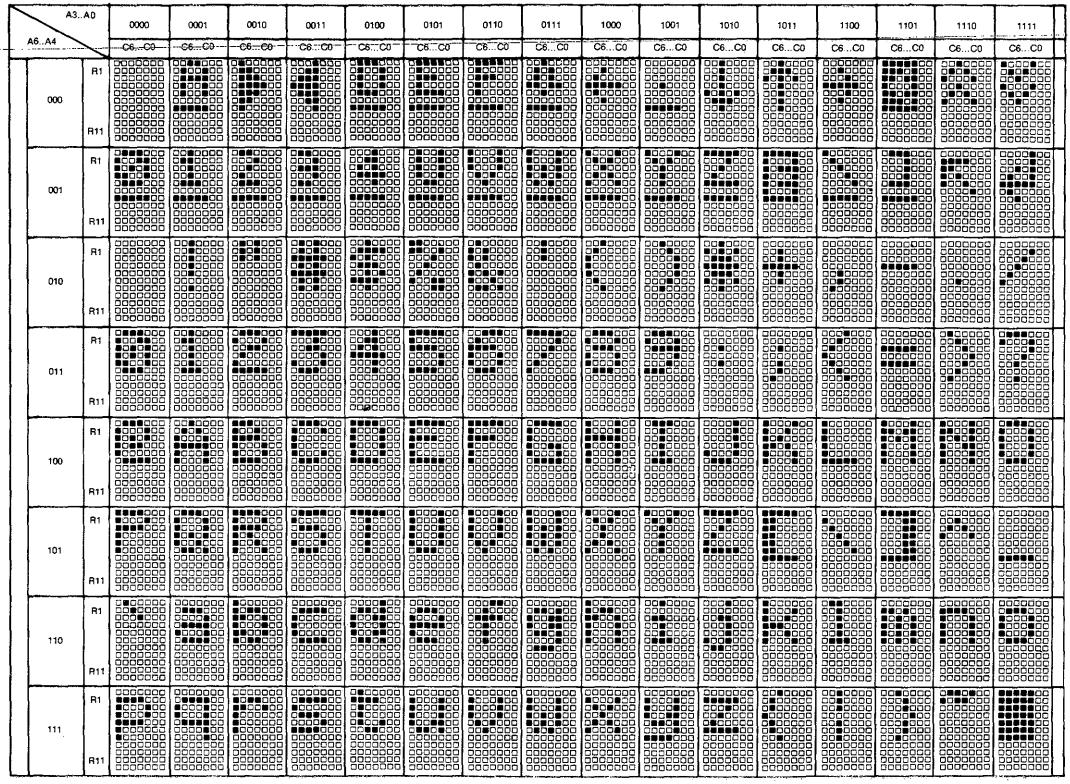
Blink Rate
The character blink rate is 1.875 Hz

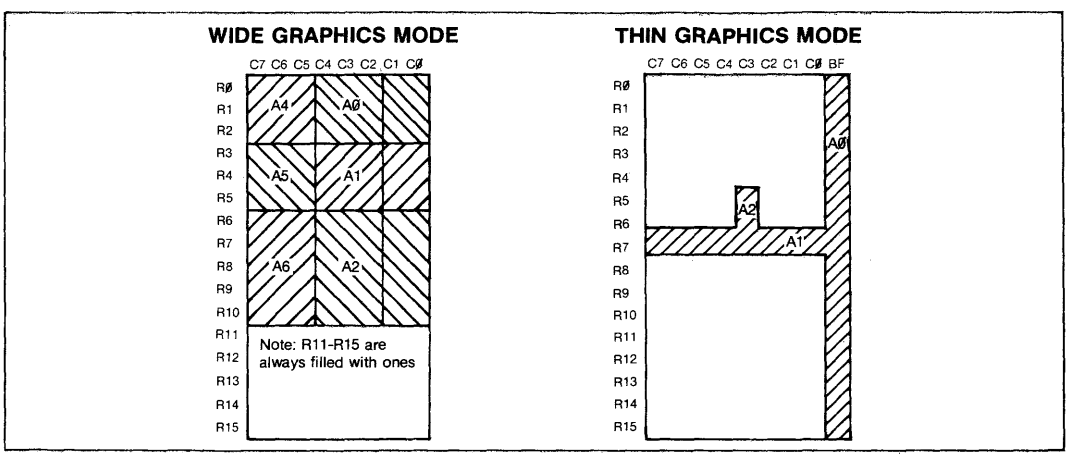
Strike-Thru
The strike-thru will be a double line at rows R5 and R6

STANDARD MICROSYSTEMS CORPORATION

CRT 8002-018
(5 X 7 ASCII)
CODING INFORMATION

CRT Video Display-Controller Video Generator VDAC™





ATTRIBUTES

Underline
Underline will be a double horizontal line at R7 and R8

Cursor
Cursor will be a reverse video block

Blink Rate
The character blink rate is 1.875 Hz

Strike-Thru
The strike-thru will be a single horizontal line at R4

STANDARD MICROSYSTEMS CORPORATION

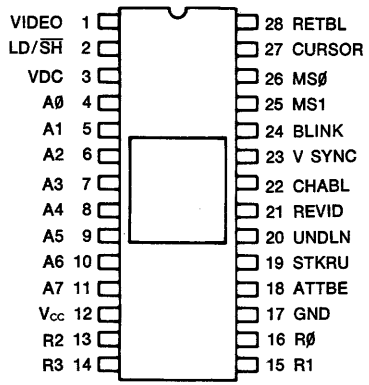
CRT 8002H
μPC FAMILY

CRT Video Display Attributes Controller Video Generator VDAC™

FEATURES

- ☐ On chip character generator (mask programmable)
  - 128 Characters (alphanumeric and graphic)
  - 7 x 11 Dot matrix block
- ☐ On chip video shift register
  - Maximum shift register frequency 25 MHz
- ☐ ROM Access time 310 ns
- ☐ On chip horizontal and vertical retrace video blanking
- ☐ No descender circuitry required
- ☐ Four modes of operation (intermixable)
  - Internal character generator (ROM)
  - Wide graphics
  - Thin graphics
  - External inputs (fonts/dot graphics)
- ☐ On chip attribute logic—character, field
  - Reverse video
  - Character blank
  - Character blink
  - Underline
  - Strike-thru
- ☐ On chip cursor
- ☐ Programmable character blink rate
- ☐ Programmable cursor blink rate
- ☐ Subscriptable
- ☐ Expandable character set
  - External fonts
  - Alphanumeric and graphic
  - RAM, ROM, and PROM

PIN CONFIGURATION



- ☐ On chip address buffer
- ☐ On chip attribute buffer
- ☐ +5 volt operation
- ☐ TTL compatible
- ☐ N-channel COPLAMOS® Titanium Disilicide Process
- ☐ Compatible with CRT 5027/37 VTAC®

SECTION V

General Description

The SMC CRT 8002H Video Display Attributes Controller (VDAC) is an n-channel COPLAMOS® MOS/LSI device. It contains a 7X11X128 character generator ROM, a wide graphics mode, a thin graphics mode, an external input mode, character address/data latch, field and/or character attribute logic, attribute latch, four cursor modes, two programmable blink rates, and a high speed video shift register. The CRT 8002H VDAC is a companion chip to SMC's CRT 5027/37 VTAC®. Together these two chips comprise the circuitry required for the display portion of a CRT video terminal.

The CRT 8002H video output may be connected directly to a CRT monitor video input. The CRT 5027/37 blanking output can be connected directly to the CRT 8002H retrace blank input to provide both horizontal and vertical retrace blanking of the video output.

The CRT 8002H attributes include: reverse video, character blank, blink, underline, and strike-thru. The character blink rate is mask programmable from 7.5 Hz to 1.0 Hz and has a duty cycle of 75/25. The underline and strike-thru are similar but independently controlled functions and can be mask programmed to any number of raster lines at any position in the character block. These attributes are available in all modes.

In the wide graphic mode the CRT 8002H produces a graphic entity the size of the character block. The graphic entity contains 8 parts, each of which is associated with one bit of a graphic byte, thereby providing for 256 unique graphic symbols. Thus, the CRT 8002H can produce either an alphanumeric symbol or a graphic entity depending on the mode selected. The mode can be changed on a per character basis.

The thin graphic mode enables the user to create single line drawings and forms.

The external mode enables the user to extend the on-chip ROM character set and/or the on-chip graphics capabilities by inserting external symbols. These external symbols can come from either RAM, ROM or PROM.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, with respect to ground	+8.0V
Negative Voltage on any Pin, with respect to ground	−0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, unless otherwise noted)

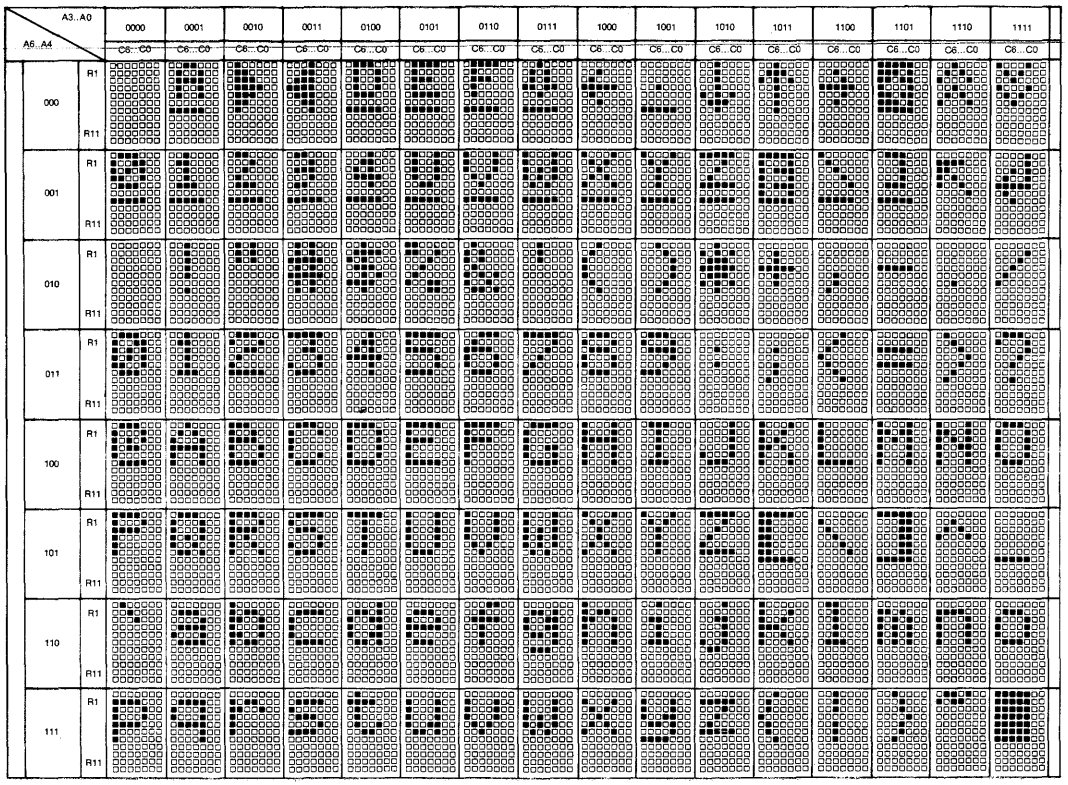
Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	excluding VDC
High-level, V_{IH}	2.0			V	excluding VDC
INPUT VOLTAGE LEVELS-CLOCK					
Low-level, V_{IL}			0.8	V	
High-level, V_{IH}	4.3			V	See Figure 6
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL}=0.4 mA, 74LSXX load
High-level, V_{OH}	2.4			V	I_{OH}=−20μA
INPUT CURRENT					
Leakage, I_L (Except CLOCK)			10	μA	$0 \leq V_{IN} \leq V_{CC}$
Leakage, I_L (CLOCK Only)			50	μA	$0 \leq V_{IN} \leq V_{CC}$
INPUT CAPACITANCE					
Data		10		pF	@ 1 MHz
LD/$\overline{SH}$		20		pF	@ 1 MHz
CLOCK		25		pF	@ 1 MHz
POWER SUPPLY CURRENT					
I_{CC}		100		mA	
A.C. CHARACTERISTICS					
See Figure 6, 7					

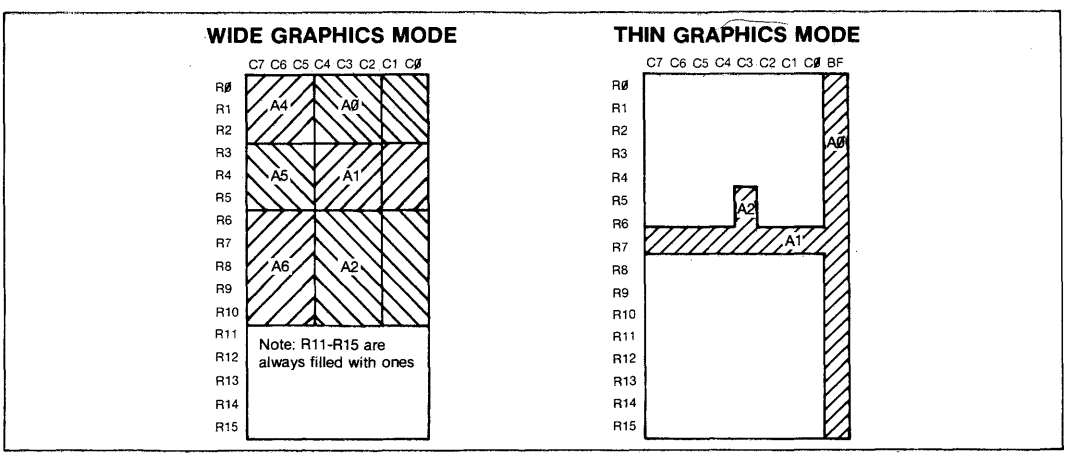
SYMBOL	PARAMETER	MIN.	MAX.	UNITS
VDC	Video Dot Clock Frequency	1.0	25	MHz
PW_H	VDC—High Time	11.0		ns
PW_L	VDC—Low Time	11.0		ns
t_{CY}	LD/SH cycle time	310		ns
t_r, t_f	Rise, fall time		9	ns
t_{SET-UP}	Input set-up time	≥0		ns
t_{HOLD}	Input hold time	15		ns
t_{PDI}, t_{PDO}	Output propagation delay	15	27	ns
t_1	LD/SH set-up time	5		ns
t_2	LD/SH hold time	5		ns

STANDARD MICROSYSTEMS CORPORATION

CRT 8002-018
(5 X 7 ASCII)
CODING INFORMATION

CRT Video Display-Controller Video Generator VDAC™





ATTRIBUTES

Underline
Underline will be a double horizontal line at R7 and R8

Cursor
Cursor will be a reverse video block

Blink Rate
The character blink rate is 1.875 Hz

Strike-Thru
The strike-thru will be a single horizontal line at R4

STANDARD MICROSYSTEMS CORPORATION

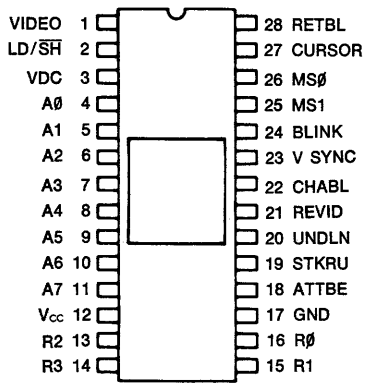
CRT 8002H
μPC FAMILY

CRT Video Display Attributes Controller Video Generator VDAC™

FEATURES

- ☐ On chip character generator (mask programmable)
  - 128 Characters (alphanumeric and graphic)
  - 7 x 11 Dot matrix block
- ☐ On chip video shift register
  - Maximum shift register frequency 25 MHz
- ☐ ROM Access time 310 ns
- ☐ On chip horizontal and vertical retrace video blanking
- ☐ No descender circuitry required
- ☐ Four modes of operation (intermixable)
  - Internal character generator (ROM)
  - Wide graphics
  - Thin graphics
  - External inputs (fonts/dot graphics)
- ☐ On chip attribute logic—character, field
  - Reverse video
  - Character blank
  - Character blink
  - Underline
  - Strike-thru
- ☐ On chip cursor
- ☐ Programmable character blink rate
- ☐ Programmable cursor blink rate
- ☐ Subscriptable
- ☐ Expandable character set
  - External fonts
  - Alphanumeric and graphic
  - RAM, ROM, and PROM

PIN CONFIGURATION



- ☐ On chip address buffer
- ☐ On chip attribute buffer
- ☐ +5 volt operation
- ☐ TTL compatible
- ☐ N-channel COPLAMOS® Titanium Disilicide Process
- ☐ Compatible with CRT 5027/37 VTAC®

SECTION V

General Description

The SMC CRT 8002H Video Display Attributes Controller (VDAC) is an n-channel COPLAMOS® MOS/LSI device. It contains a 7X11X128 character generator ROM, a wide graphics mode, a thin graphics mode, an external input mode, character address/data latch, field and/or character attribute logic, attribute latch, four cursor modes, two programmable blink rates, and a high speed video shift register. The CRT 8002H VDAC is a companion chip to SMC's CRT 5027/37 VTAC®. Together these two chips comprise the circuitry required for the display portion of a CRT video terminal.

The CRT 8002H video output may be connected directly to a CRT monitor video input. The CRT 5027/37 blanking output can be connected directly to the CRT 8002H retrace blank input to provide both horizontal and vertical retrace blanking of the video output.

The CRT 8002H attributes include: reverse video, character blank, blink, underline, and strike-thru. The character blink rate is mask programmable from 7.5 Hz to 1.0 Hz and has a duty cycle of 75/25. The underline and strike-thru are similar but independently controlled functions and can be mask programmed to any number of raster lines at any position in the character block. These attributes are available in all modes.

In the wide graphic mode the CRT 8002H produces a graphic entity the size of the character block. The graphic entity contains 8 parts, each of which is associated with one bit of a graphic byte, thereby providing for 256 unique graphic symbols. Thus, the CRT 8002H can produce either an alphanumeric symbol or a graphic entity depending on the mode selected. The mode can be changed on a per character basis.

The thin graphic mode enables the user to create single line drawings and forms.

The external mode enables the user to extend the on-chip ROM character set and/or the on-chip graphics capabilities by inserting external symbols. These external symbols can come from either RAM, ROM or PROM.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, with respect to ground	+8.0V
Negative Voltage on any Pin, with respect to ground	−0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

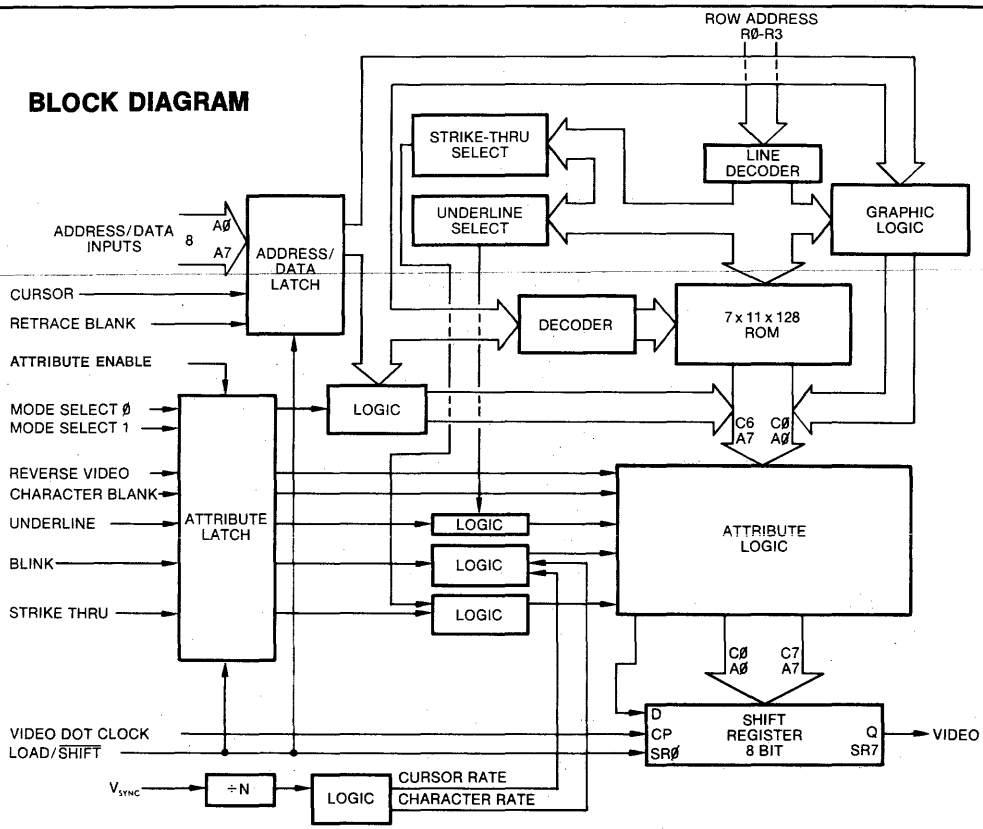
NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC} = +5V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	excluding VDC
High-level, V_{IH}	2.0			V	excluding VDC
INPUT VOLTAGE LEVELS-CLOCK					
Low-level, V_{IL}			0.8	V	
High-level, V_{IH}	4.3			V	See Figure 6
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL} = 0.4 mA, 74LSXX load
High-level, V_{OH}	2.4			V	I_{OH} = −20μA
INPUT CURRENT					
Leakage, I_L (Except CLOCK)			10	μA	$0 \leq V_{IN} \leq V_{CC}$
Leakage, I_L (CLOCK Only)			50	μA	$0 \leq V_{IN} \leq V_{CC}$
INPUT CAPACITANCE					
Data		10		pF	@ 1 MHz
LD/$\overline{SH}$		20		pF	@ 1 MHz
CLOCK		25		pF	@ 1 MHz
POWER SUPPLY CURRENT					
I_{CC}		100		mA	
A.C. CHARACTERISTICS					
See Figure 6, 7					

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
VDC	Video Dot Clock Frequency	1.0	25	MHz
PW_H	VDC—High Time	11.0		ns
PW_L	VDC—Low Time	11.0		ns
t_{CY}	LD/SH cycle time	310		ns
t_r, t_f	Rise, fall time		9	ns
t_{SET-UP}	Input set-up time	≥0		ns
t_{HOLD}	Input hold time	15		ns
t_{PDI}, t_{PDO}	Output propagation delay	15	27	ns
t_1	LD/SH set-up time	5		ns
t_2	LD/SH hold time	5		ns

BLOCK DIAGRAM



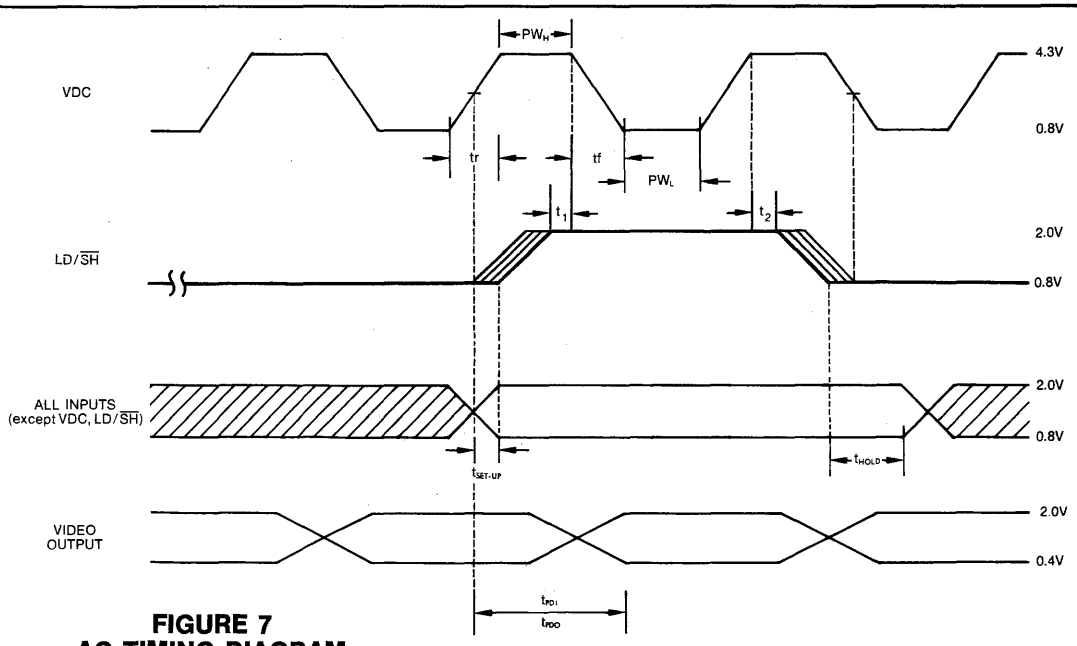


FIGURE 7
AC TIMING DIAGRAM

SECTION V

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
1	VIDEO	Video Output	0	The video output contains the dot stream for the selected row of the alphanumeric, wide graphic, thin graphic, or external character after processing by the attribute logic, and the retrace blank and cursor inputs. In the alphanumeric mode, the characters are ROM programmed into the 77 dots, (7X11) allocated for each of the 128 characters. See figure 5. The top row (RØ) and rows R12 to R15 are normally all zeros as is column C7. Thus, the character is defined in the box bounded by R1 to R11 and CØ to C6. When a row of the ROM, via the attribute logic, is parallel loaded into the 8-bit shift-register, the first bit serially shifted out is C7 (A zero; or a one in REVID). It is followed by C6, C5, through CØ. The timing of the Load/$\overline{\text{Shift}}$ pulse will determine the number of additional (— —, zero to N) backfill zeros (or ones if in REVID) shifted out. See figure 4. When the next Load/$\overline{\text{Shift}}$ pulse appears the next character's row of the ROM, via the attribute logic, is parallel loaded into the shift register and the cycle repeats.
2	LD/$\overline{\text{SH}}$	Load/$\overline{\text{Shift}}$	I	The 8 bit shift-register parallel-in load or serial-out shift modes are established by the Load/$\overline{\text{Shift}}$ input. When low, this input enables the shift register for serial shifting with each Video Dot Clock pulse. When high, the shift register parallel (broadside) data inputs are enabled and synchronous loading occurs on the next Video Dot Clock pulse. During parallel loading, serial data flow is inhibited. The Address/Data inputs (AØ-A7) are latched on the negative transition of the Load/$\overline{\text{Shift}}$ input. See timing diagram, figure 7.
3	VDC	Video Dot Clock	I	Frequency at which video is shifted.
4-11	AØ-A7	Address/Data	I	In the Alphanumeric Mode the 7 bits on inputs (AØ-A6) are internally decoded to address one of the 128 available characters (A7 = X). In the External Mode, AØ-A7 is used to insert an 8 bit word from a user defined external ROM, PROM or RAM into the on-chip Attribute logic. In the wide Graphic Modes AØ-A7 is used to define one of 256 graphic entities. In the thin Graphic Mode AØ-A2 is used to define the 3 line segments.
12	V_{CC}	Power Supply	PS	+5 volt power supply
13,14,15,16	R2,R3,R1,RØ	Row Address	I	These 4 binary inputs define the row address in the current character block.
17	GND	Ground	GND	Ground
18	ATTBE	Attribute Enable	I	A positive level on this input enables data from the Reverse Video, Character Blank, Underline, Strike-Thru, Blink, Mode Select Ø, and Mode Select 1 inputs to be strobed into the on-chip attribute latch at the negative transition of the Load/$\overline{\text{Shift}}$ pulse. The latch loading is disabled when this input is low. The latched attributes will remain fixed until this input becomes high again. To facilitate attribute latching on a character by character basis, tie ATTBE high. See timing diagram, figure 7.
19	STKRU	Strike-Thru	I	When this input is high and RETBL = 0, the parallel inputs to the shift register are forced high (SRØ-SR7), providing a solid line segment throughout the character block. The operation of strike-thru is modified by Reverse Video (see table 1). In addition, an on-chip ROM programmable decoder is available to decode the line count on which strike-thru is to be placed as well as to program the strike-thru to be 1 to N raster lines high. Actually, the strike-thru decoder (mask programmable) logic allows the strike-thru to be any number or arrangement of horizontal lines in the character block. The standard strike-thru will be a double line on rows R5 and R6.
20	UNDLN	Underline	I	When this input is high and RETBL = 0, the parallel inputs to the shift register are forced high (SRØ-SR7), providing a solid line segment throughout the character block. The operation of underline is modified by Reverse Video (see table 1). In addition, an on-chip ROM programmable decoder is available to decode the line count on which underline is to be placed as well as to program the underline to be 1 to N raster lines high. Actually, the underline decoder (mask programmable) logic allows the underline to be any number or arrangement of horizontal lines in the character block. The standard underline will be a single line on R11.
21	REVID	Reverse Video	I	When this input is low and RETBL = 0, data into the Attribute Logic is presented directly to the shift register parallel inputs. When reverse video is high data into the Attribute Logic is inverted and then presented to the shift register parallel inputs. This operation reverses the data and field video. See table 1.
22	CHABL	Character Blank	I	When this input is high, the parallel inputs to the shift register are all set low, providing a blank character line segment. Character blank will override blink. The operation of Character Blank is modified by the Reverse Video input. See table 1.
23	V SYNC	V SYNC	I	This input is used as the clock input for the two on-chip mask programmable blink rate dividers. The cursor blink rate (50/50 duty cycle) will be twice the character blink rate (75/25 duty cycle). The divisors can be programmed from ÷ 4 to ÷ 30 for the cursor (÷ 8 to ÷ 60 for the character).
24	BLINK	Blink	I	When this input is high and RETBL = 0 and CHABL = 0, the character will blink at the programmed character blink rate. Blinking is accomplished by blanking the character block with the internal Character Blink clock. The standard character blink rate is 1.875 Hz.
25 26	MS1 MSØ	Mode Select 1 Mode Select Ø	I I	These 2 inputs define the four modes of operation of the CRT 8002 as follows: Alphanumeric Mode — In this mode addresses AØ-A6 (A7 = X) are internally decoded to address 1 of the 128 available ROM characters. The addressed character along with the decoded row will define a 7 bit output from the ROM to be loaded into the shift register via the attribute logic. Thin Graphics Mode — In this mode AØ-A2 (A3-A7 = X) will be loaded into the thin graphic logic along with the row addresses. This logic will define the segments of a graphic entity as defined in figure 2. The top of the entity will begin on row 0000 and will end on a mask programmable row.

MS1	MSØ	MODE
1	1	Alphanumeric
1	0	Thin Graphics
0	1	External Mode
0	0	Wide Graphics

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
25 26 (cont.)				External Mode – In this mode the inputs AØ-A7 go directly from the character latch into the shift register via the attribute logic. Thus the user may define external character fonts or graphic entities in an external PROM, ROM or RAM. See figure 3. Wide Graphics Mode—In this mode the inputs AØ-A7 will define a graphic entity as described in figure 1. Each line of the graphic entity is determined by the wide graphic logic in conjunction with the row inputs RØ to R3. In this mode each segment of the entity is defined by one of the bits of the 8 bit word. Therefore, the 8 bits can define any 1 of the 256 possible graphic entities. These entities can butt up against each other to form a contiguous pattern or can be interspaced with alphanumeric characters. Each of the entities occupies the space of 1 character block and thus requires 1 byte of memory. These 4 modes can be intermixed on a per character basis.
27	CURSOR	Cursor	I	When this input is enabled 1 of the 4 pre-programmed cursor modes will be activated. The cursor mode is on-chip mask programmable. The standard cursor will be a blinking (at 3.75Hz) reverse video block. The 4 cursor modes are: Underline—In this mode an underline (1 to N raster lines) at the programmed underline position occurs. Blinking Underline—In this mode the underline blinks at the cursor rate. Reverse Video Block—In this mode the Character Block is set to reverse video. Blinking Reverse Video Block—In this mode the Character Block is set to reverse video at the cursor blink rate. The Character Block will alternate between normal video and reverse video. The cursor functions are listed in table 1.
28	RETBL	Retrace Blank	I	When this input is latched high, the shift register parallel inputs are unconditionally cleared to all zeros and loaded into the shift register on the next Load/$\overline{\text{Shift}}$ pulse. This blanks the video, independent of all attributes, during horizontal and vertical retrace time.

TABLE 1

CURSOR	RETBL	REVID	CHABL	UNDLN*	FUNCTION
X	1	X	X	X	"0" S.R. All
0	0	0	0	0	$\overline{D}$ (S.R.) All
0	0	0	0	1	"1" (S.R.)*
					$\overline{D}$ (S.R.) All others
0	0	0	1	X	"0" (S.R.) All
0	0	1	0	0	$\overline{D}$ (S.R.) All
0	0	1	0	1	"0" (S.R.)*
					$\overline{D}$ (S.R.) All others
0	0	1	1	X	"1" (S.R.) All
Underline*	0	0	0	X	"1" (S.R.)*
					$\overline{D}$ (S.R.) All others
Underline*	0	0	1	X	"1" (S.R.)*
					"0" (S.R.) All others
Underline*	0	1	0	X	"0" (S.R.)*
					$\overline{D}$ (S.R.) All others
Underline*	0	1	1	X	"0" (S.R.)*
					"1" (S.R.) All others
Blinking** Underline*	0	0	0	X	"1" (S.R.)* Blinking
					$\overline{D}$ (S.R.) All others
Blinking** Underline*	0	0	1	X	"1" (S.R.)* Blinking
					"0" (S.R.) All others
Blinking** Underline*	0	1	0	X	"0" (S.R.)* Blinking
					$\overline{D}$ (S.R.) All others
Blinking** Underline*	0	1	1	X	"0" (S.R.)* Blinking
					"1" (S.R.) All others
REVID Block	0	0	0	0	$\overline{D}$ (S.R.) All
REVID Block	0	0	0	1	"0" (S.R.)*
					$\overline{D}$ (S.R.) All others
REVID Block	0	0	1	X	"1" (S.R.) All
REVID Block	0	0	0	1	"0" (S.R.)*
					$\overline{D}$ (S.R.) All others
REVID Block	0	1	0	0	$\overline{D}$ (S.R.) All
REVID Block	0	1	0	1	"1" (S.R.)*
					$\overline{D}$ (S.R.) All others
REVID Block	0	1	1	X	"0" (S.R.) All
Blink** REVID Block	0	0	0	0	Alternate Normal Video/REVID At Cursor Blink Rate
Blink** REVID Block	0	0	0	1	
Blink** REVID Block	0	0	1	X	
Blink** REVID Block	0	1	0	0	
Blink** REVID Block	0	1	0	1	
Blink** REVID Block	0	1	1	X	

*At Selected Row Decode **At Cursor Blink Rate

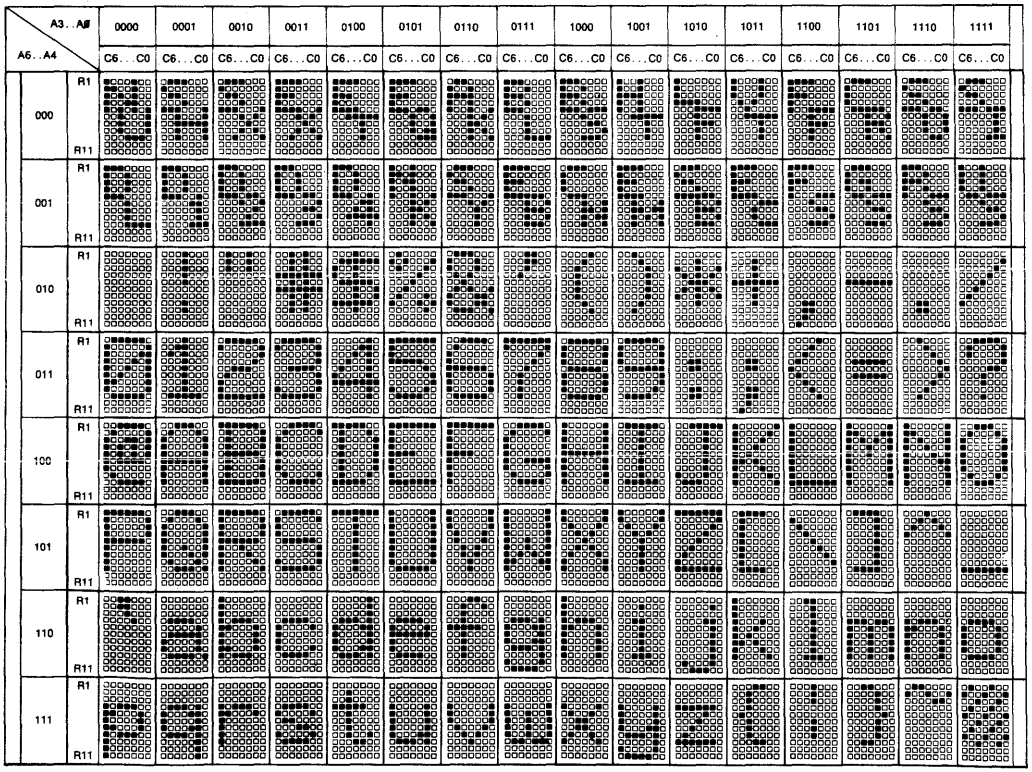
Note: If Character is Blinking at Character Rate, Cursor will change it to Cursor Blink Rate.

FIGURE 5
ROM CHARACTER BLOCK FORMAT

										ROWS	R3	R2	R1	RØ
(ALL ZEROS) →	0	0	0	0	0	0	0	—	—	RØ	0	0	0	0
	0	0	0	0	0	0	0	—	—	R1	0	0	0	1
	0	0	0	0	0	0	0	—	—	R2	0	0	1	0
	0	0	0	0	0	0	0	—	—	R3	0	0	1	1
	0	0	0	0	0	0	0	—	—	R4	0	1	0	0
	0	0	0	0	0	0	0	—	—	R5	0	1	0	1
77 BITS (7 x 11 ROM)	0	0	0	0	0	0	0	—	—	R6	0	1	1	0
	0	0	0	0	0	0	0	—	—	R7	0	1	1	1
	0	0	0	0	0	0	0	—	—	R8	1	0	0	0
	0	0	0	0	0	0	0	—	—	R9	1	0	0	1
	0	0	0	0	0	0	0	—	—	R1Ø	1	0	1	0
	0	0	0	0	0	0	0	—	—	R11	1	0	1	1
	0	0	0	0	0	0	0	—	—	R12	1	1	0	0
	0	0	0	0	0	0	0	—	—	R13	1	1	0	1
(ALL ZEROS)	0	0	0	0	0	0	0	—	—	R14	1	1	1	0
	0	0	0	0	0	0	0	—	—	R15	1	1	1	1
	*C7	C6	C5	C4	C3	C2	C1	CØ	—	—				

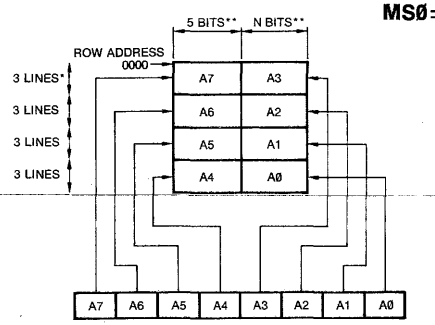
EXTENDED ZEROS (BACK FILL) FOR INTERCHARACTER SPACING (NUMBER CONTROLLED BY LD/$\overline{SH}$, VDC TIMING)

*COLUMN 7 IS ALL ZEROS (REVID = 0)
COLUMN 7 IS SHIFTED OUT FIRST



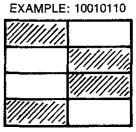
CONSULT FACTORY FOR CUSTOM FONT AND OPTION PROGRAMMING FORMS.

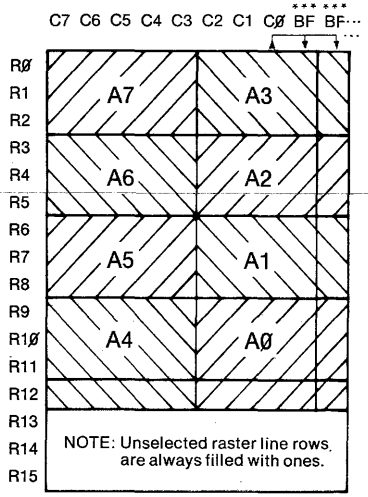
FIGURE 1
WIDE GRAPHICS MODE
MSØ=Ø MS1=Ø



*ON CHIP ROM PROGRAMMABLE TO 2, 3, OR 4 LINE MULTIPLES
**CAN BE PROGRAMMED FROM 1 TO 7 BITS
***LENGTH DETERMINED BY LD/$\overline{SR}$, VDC TIMING

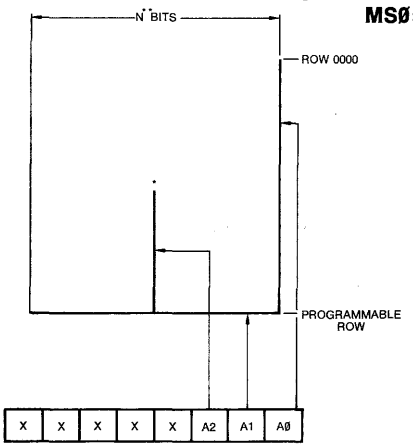
EXAMPLE: 10010110



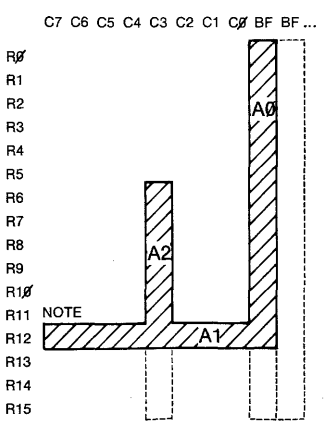


BF = back fill

FIGURE 2
THIN GRAPHICS MODE
MSØ=Ø MS1=1



X = DON'T CARE
* THE INSIDE SEGMENT IS MASK PROGRAMMABLE TO ROW 0000
** LENGTH DETERMINED BY LD/$\overline{SR}$, VDC TIMING



NOTE: When A1 = "1", the underline row/rows are deleted.
When A1 = "0", the underline, if selected, will appear.

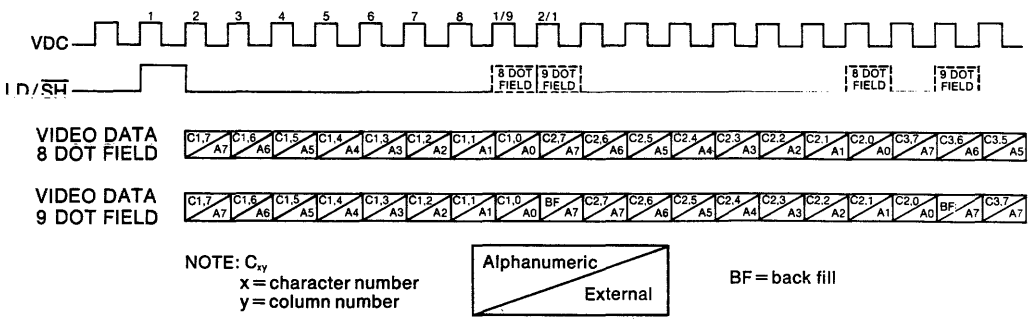
BF = back fill

FIGURE 3
EXTERNAL MODE
MSØ=1 MS1=Ø

	C7	C6	C5	C4	C3	C2	C1	CØ	BF	BF	···
RØ – R15	A7	A6	A5	A4	A3	A2	A1	AØ	A7	A7	···

BF = back fill

FIGURE 4 TYPICAL VIDEO OUTPUT



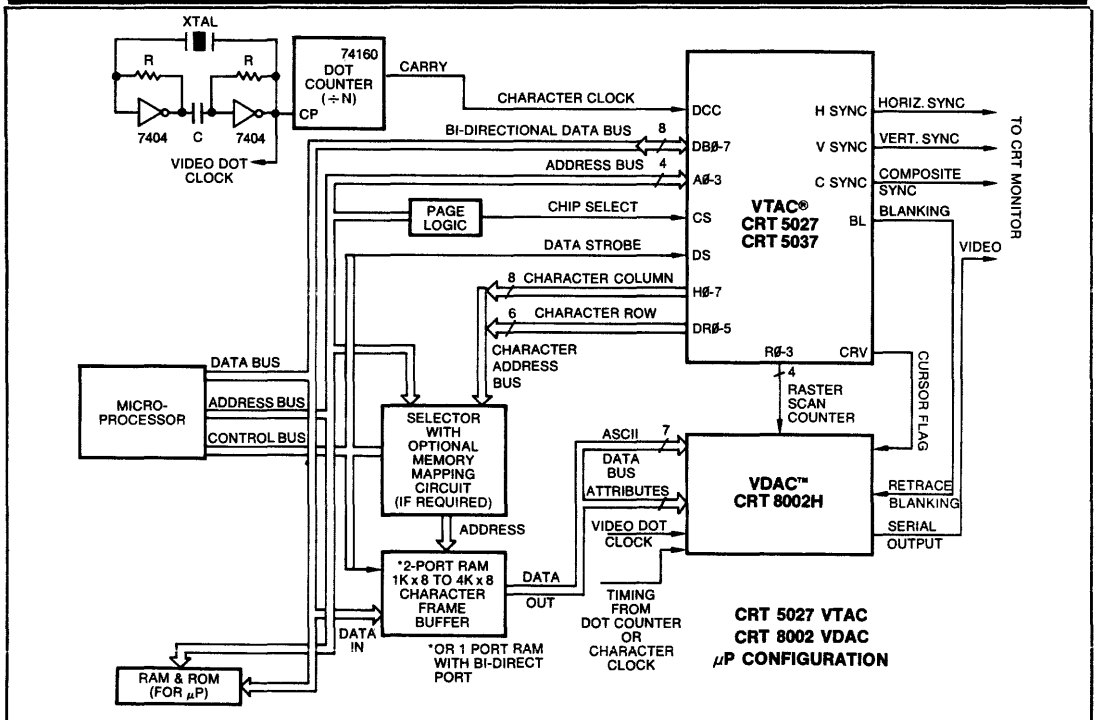
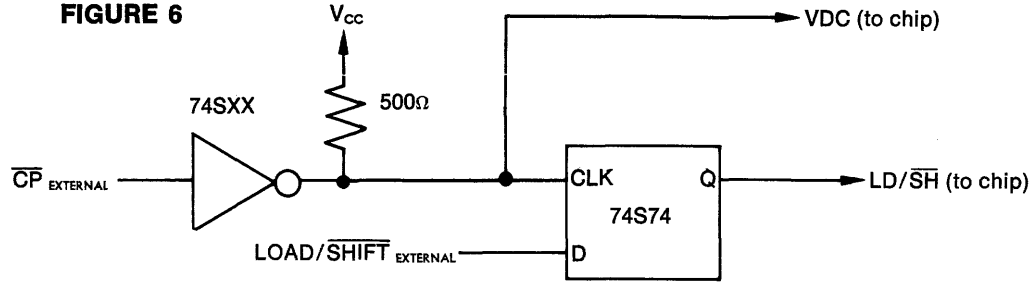


FIGURE 6



STANDARD MICROSYSTEMS CORPORATION

CRT 7004
μPC FAMILY

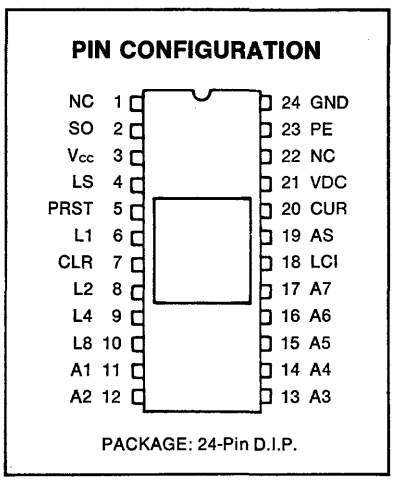
Dot Matrix Character Generator

128 Characters of 7 x 11 Bits

FEATURES

- ☐ On chip character generator (mask programmable)
  - 128 Characters
  - 7 x 11 Dot matrix block
- ☐ On chip video shift register
  - Maximum shift register frequency
    - CRT 7004A 20MHz
    - CRT 7004B 15MHz
    - CRT 7004C 10MHz
    - Access time 400ns
- ☐ No descender circuitry required
- ☐ On chip cursor
- ☐ On chip character address buffer
- ☐ On chip line address buffer
- ☐ Single +5 volt power supply
- ☐ TTL compatible
- ☐ MOS N-channel silicon-gate COPLAMOS® process
- ☐ CLASP® technology—ROM
- ☐ Compatible with CRT 5027 VTAC®
- ☐ Enhanced version of CG5004L-1

PIN CONFIGURATION



PACKAGE: 24-Pin D.I.P.

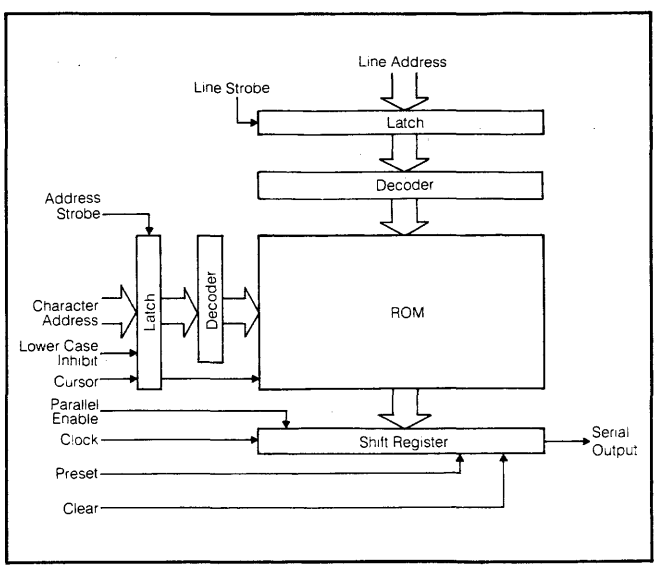
SECTION V

GENERAL DESCRIPTION

SMC's CRT 7004 is a high speed character generator with a high speed video shift register designed to display 128 characters in a 7 x 11 dot matrix. The CRT 7004 is an enhanced, pin for pin compatible, version of SMC's CG5004L-1. It is fabricated using SMC's patented COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply. This process permits reduction of turn-around time for ROM patterns.

The CRT 7004 is a companion chip to SMC's CRT 5027 VTAC®. Together these two chips comprise the circuitry required for the display portion of a CRT video terminal.

FUNCTIONAL BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

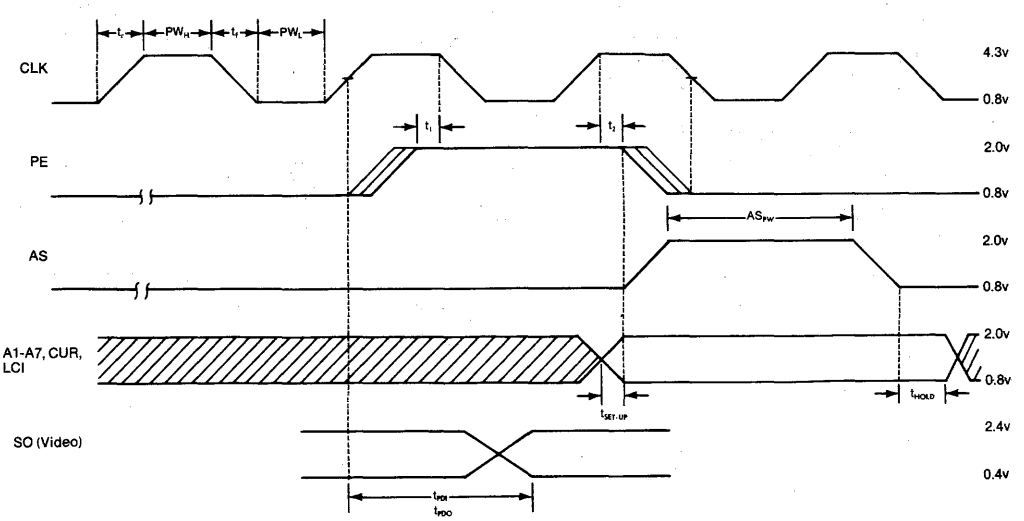
ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}= +5V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	excluding VDC
High-level, V_{IH}	2.0			V	excluding VDC
INPUT VOLTAGE LEVELS-CLOCK					
Low-level, V_{IL}			0.8	V	
High-level, V_{IH}	4.3			V	See AC Timing Diagram
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL}=0.4 mA, 74LSXX load
High-level, V_{OH}	2.4			V	I_{OH}=−20μA
INPUT CURRENT					
Leakage, I_L			100	μA	V_{IN} = O, LS, AS, A1-A7, Cursor LCI
			10	μA	$O \leq V_{IN} \leq V_{CC}$, All others
INPUT CAPACITANCE					
Data		10		pF	@ 1 MHz
PE		20		pF	@ 1 MHz
CLOCK		25		pF	@ 1 MHz
POWER SUPPLY CURRENT					
I_{CC}		100		mA	

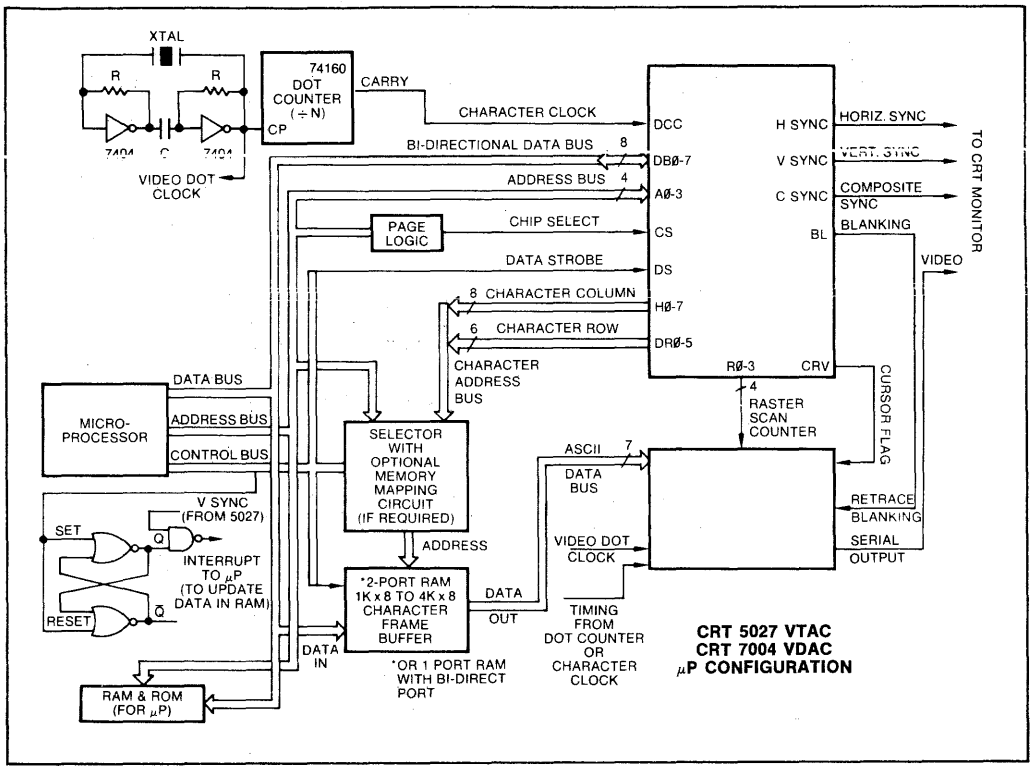
SYMBOL	PARAMETER	CRT 7004A		CRT 7004B		CRT 7004C		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
VDC	Video Dot Clock Frequency	1.0	20	1.0	15	1.0	10	MHz
PW_H	VDC — High Time	13.5		21		36		ns
PW_L	VDC — Low Time	13.5		21		36		ns
$t_{CY}AS$	Address strobe to PE high	400		533		800		ns
$t_{CY}LS$	Line strobe to PE high	1.0		1.0		1.0		μs
t_r, t_f	Rise, fall time		10		10		10	ns
t_1	PE set-up time	5		20		20		ns
t_2	PE hold time	15		15		15		ns
AS_{PW}	Address strobe pulse width	50		50		50		ns
LS_{PW}	Line strobe pulse width	50		50		50		ns
t_{SET-UP}	Input set-up time	≥0		≥0		≥0		ns
t_{HOLD}	Input hold time	15		15		15		ns
t_{Pd1}, t_{Pd0}	Output propagation delay		45		60		90	ns

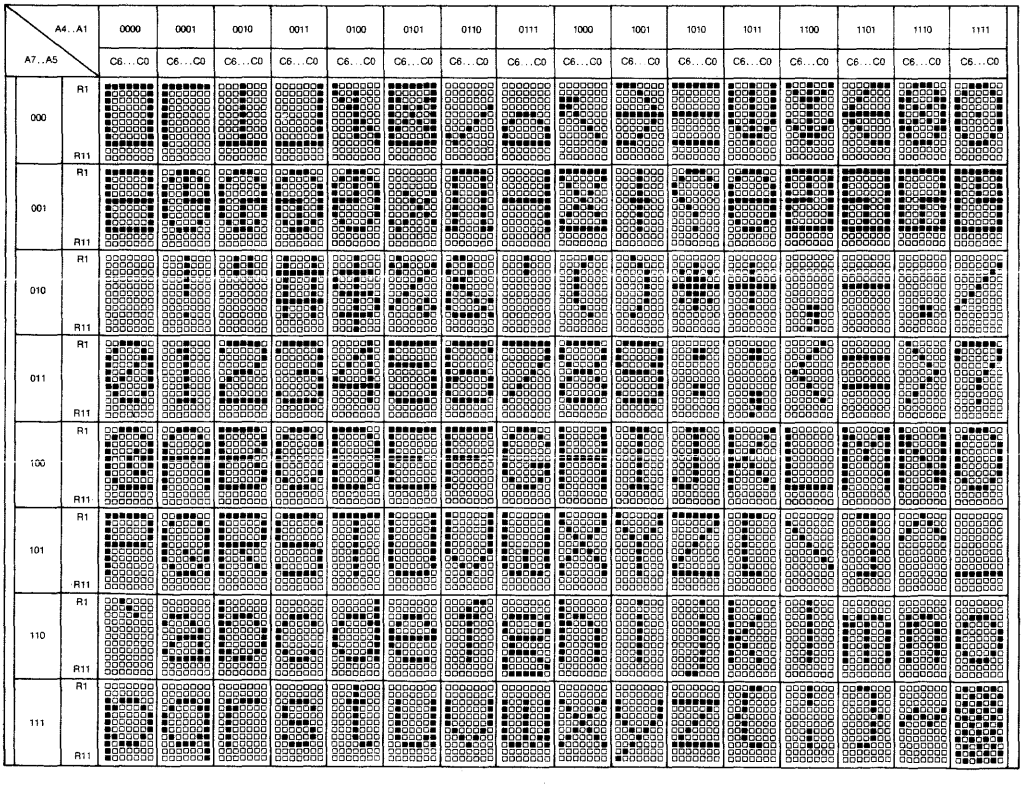
DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
1	NC	No Connection	
2	SO	Serial Output	The output of the dynamic shift register is clocked out on this pin. The serial input to this shift register is internally grounded; thus zeros are shifted in while data is shifted out.
3	V_{CC}	Power Supply	+5 volt supply
4	LS	Line Strobe	A positive pulse on this input enters data from the L1, L2, L4, L8 lines into the line address holding register. The LS input may be left open, in which case it is pulled up to V_{CC} by an internal resistor. Data on the L1 to L8 inputs is then entered directly into the register without any latching action.
5	PRST	Preset	A high level on this input forces the last stage of the shift register and the serial output to a logic high.
6,8,9,10	L1, L2, L4, L8	Line Address	A binary number N, on these four inputs address the Nth line of the character font for N = 1—11. If lines 0, 12, 13, 14 or 15 are addressed, the parallel inputs to the shift register are all forced low.
7	CLR	Clear	A high level on this input forces the last stage of the shift register and the serial output to a logic low and will be latched (for a character time) by PE. Clear overrides preset.
11-17	A1-A7	Character Address	The seven-bit word on these inputs is decoded internally to address one of the 128 available characters.
18	LCI	Lower Case Inhibit	A high level on this input transforms the address of a lower case character into that of the equivalent upper case character. This is internally achieved by forcing A6 low whenever A7 and LCI are high.
19	AS	Address Strobe	A positive pulse on this input enters data from the A1-A7, LCI and CUR inputs into the holding register. The AS input may be left open, in which case it is pulled up to V_{CC} by an internal resistor. The data on the A1-A7, LCI and CUR inputs is then entered directly into the register without any latching action.
20	CUR	Cursor*	A high level on this input causes the cursor pattern to be superimposed on the pattern of the character addressed, i.e., the two patterns are OR-ed to generate the parallel inputs to the shift register. The standard cursor is presented as a double underscore on rows 10 and 11.
21	CLK	Clock	Frequency at which video (SO) is shifted.
22	NC	No Connection	
23	PE	Parallel Enable	A high level on this input loads the word at the output of the ROM into the shift register. The PE input must then be brought low again to allow the shift register to clock out this word.
24	GND	Ground	Ground

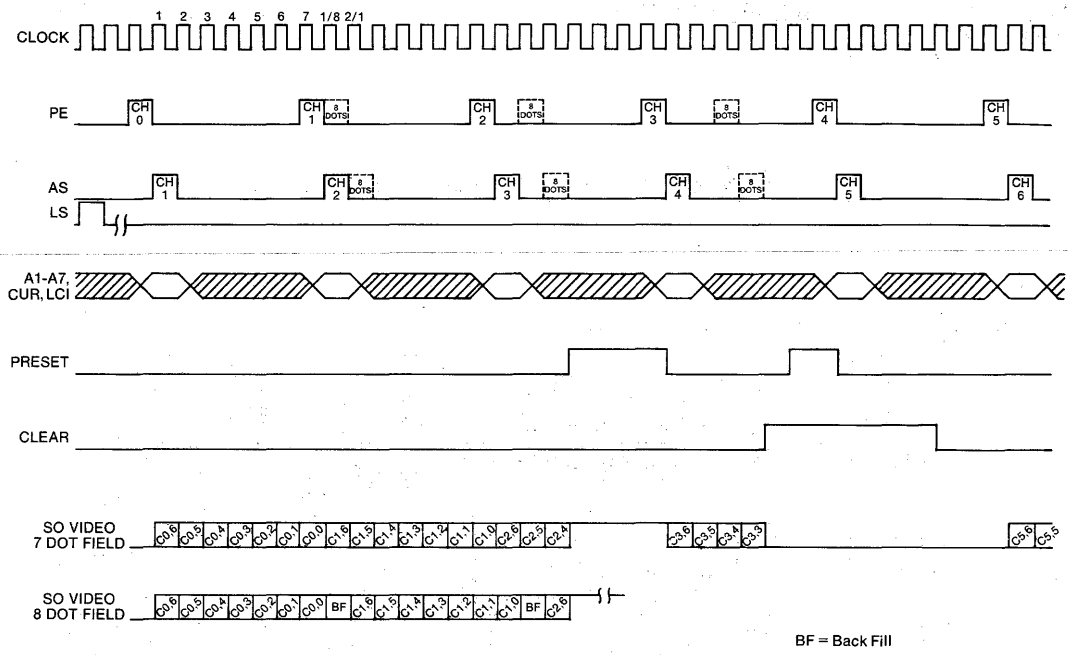


AC TIMING DIAGRAM

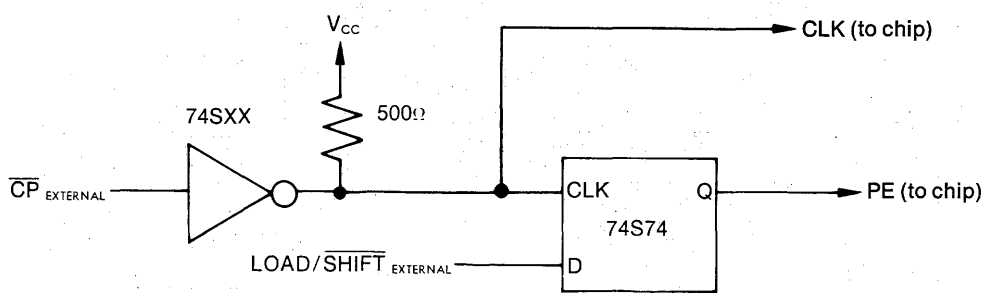




*CONSULT FACTORY FOR CUSTOM FONT AND CURSOR OPTION.



TYPICAL VIDEO OUTPUT

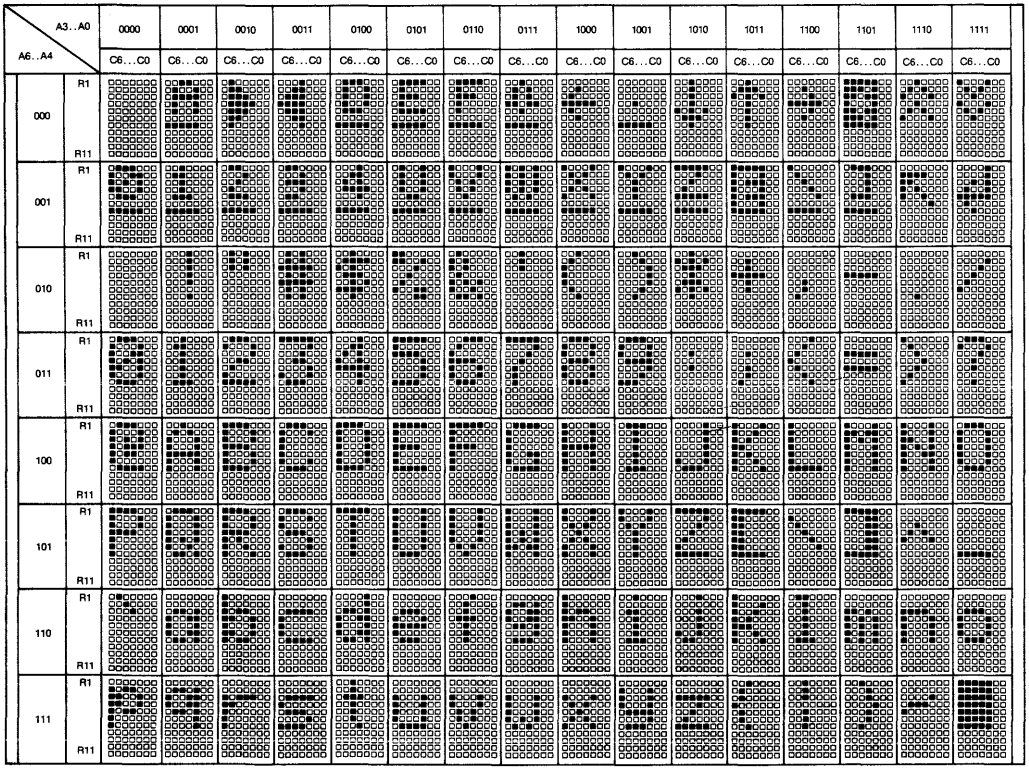


NOTE

The differences between the CRT 7004 and CG5004L-1 are detailed below:

CG5004L-1	CRT 7004
1. If both the Preset and Clear inputs are brought high simultaneously the Serial Output is disabled and may be wire-ORed.	1. Clear overrides Preset, no output disable is possible.
2. All Inputs $V_{IH} = V_{CC} - 1.5v$	2. All inputs (except CLK) $V_{IH} = 2.0v$, min. CLK $V_{IH} = 4.3v$, min.
3. SO $V_{OL} = 0.4v$ @ $I_{OL} = 0.2mA$	3. SO $V_{OL} = 0.4v$ @ $I_{OL} = 0.4mA$ 74LSXX load
4. Shift Register is static	4. Shift Register is dynamic
5. Clear—directly forces the output low; when released, the output is determined by the state of the shift register output.	5. Clear directly forces the output low and will be latched (for a character time) by PE.
6. General Timing Differences—See Timing Diagram	6. General Timing Differences—See Timing Diagram

Dot Matrix Character Generator



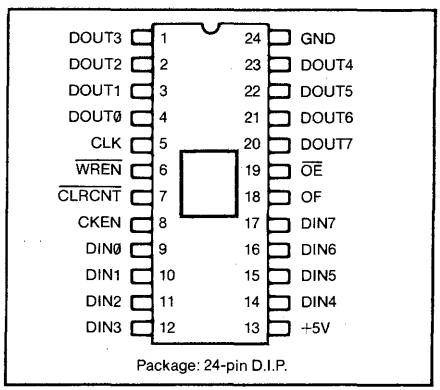
The Cursor for the CRT 7004-003 is presented as a double underscore on Rows 8 and 9.

Single Row Buffer
SRB

FEATURES:

- ☐ Low Cost Solution to CRT Memory Contention Problem
- ☐ Provides Enhanced Processor Throughput for CRT Display Systems
- ☐ Provides 8 Bit Wide Variable Length Serial Memory
- ☐ Permits Active Video on All Scan Lines of Data Row
- ☐ Dynamically Variable Number of Characters per Data Row — ...64, 80, 132,... up to a Maximum of 135
- ☐ Cascadable for Data Rows Greater than 135 Characters
- ☐ Stackable for Invisible Attributes or Character Widths of Greater than 8 Bits
- ☐ Three-State Outputs
- ☐ 3.3MHz Typical Read/Write Data Rate
- ☐ Static Operation
- ☐ Compatible with SMC CRT 5037, CRT 9007, and other CRT Controllers
- ☐ 24 Pin Dual In Line Package
- ☐ +5 Volt Only Power Supply
- ☐ TTL Compatible Inputs and Outputs
- ☐ Available in 135 Byte Maximum Length (CRT 9006-135) or 83 Byte Maximum Length (CRT 9006-83)

PIN CONFIGURATION



Package: 24-pin D.I.P.

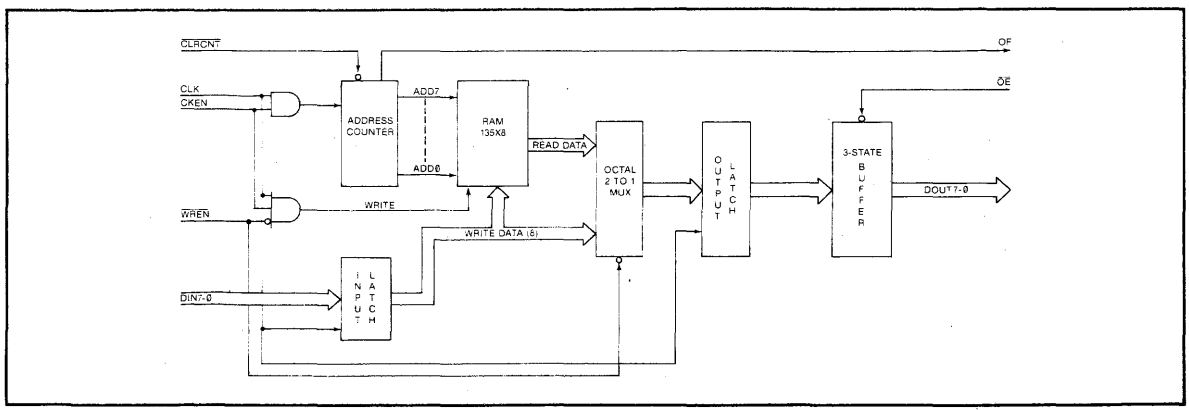
APPLICATIONS:

- ☐ CRT Data Row Buffer
- ☐ Block-Oriented Buffer
- ☐ Printer Buffer
- ☐ Synchronous Communications Buffer
- ☐ Floppy Disk Sector Buffer

SECTION V

GENERAL DESCRIPTION

The SMC Single Row Buffer (SRB) provides a low cost solution to memory contention between the system processor and CRT controller in video display systems.
The SRB is a RAM-based buffer which is loaded with character data from system memory during the first scan line of each data row. While data is being written into the RAM it is also being output through the multiplexer onto the Data Ouput (DOUT) Lines. During subsequent scan lines in the data row, the system will disable Write Enable (WREN) and cause data to be read out from the internal RAM for CRT screen refresh, thereby releasing the system memory for processor access for the remaining N-1 scan lines where N is the number of scan lines per data row. The SRB enhances processor throughput and permits a flicker-free display of data.



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1-4	DATA OUTPUTS	DOUT3-DOUTØ	Data Outputs from the internal output latch.
5	CLOCK	CLK	Character clock. The negative-going edge of CLK clocks the latches. When CKEN (pin 8) is high, CLK will increment the address counter.
6	WRITE ENABLE	$\overline{WREN}$	When $\overline{WREN}$ is low, data from the input latch is transferred directly to the output latch and simultaneously written into sequential locations in the RAM.
7	CLEAR COUNTER	$\overline{CLRCNT}$	A negative transition on $\overline{CLRCNT}$ clears the RAM address counter. $\overline{CLRCNT}$ is normally asserted low near the beginning of each scan line.
8	CLOCK ENABLE	CKEN	When CKEN is high, CLK will clock the address counter. The combination of CKEN high and WREN low will allow the writing of data into the RAM.
9-12	DATA INPUTS	DINØ-DIN3	Data Inputs from system memory.
13	POWER SUPPLY	V_{CC}	+5 Volt supply.
14-17	DATA INPUTS	DIN4-DIN7	Data Inputs from system memory.
18	OVERFLOW FLAG	OF	This output goes high when the RAM address counter reaches its maximum count. If cascaded operation of multiple CRT 9006's is desired for more than 135 bytes, OF may be used to drive the CKEN input of the second row buffer chip.
19	OUTPUT ENABLE	$\overline{OE}$	When $\overline{OE}$ is low, the data outputs DOUTØ-DOUT7 are enabled. When $\overline{OE}$ is high, DOUTØ-DOUT7 present a high impedance state.
20-23	DATA OUTPUTS	DOUT7-DOUT4	Data Outputs from the internal output latch.
24	GROUND	GND	Ground.

OPERATION

For CRT operation, the Write Enable ($\overline{WREN}$) signal is made active for the duration of the top scan line of each data row. Clear Counter ($\overline{CLRCNT}$) typically occurs at the beginning of each scan line (HSYNC may be used as input to $\overline{CLRCNT}$). Data is continually clocked into the input latch by CLK. When Clock Enable (CKEN) occurs, the data in the input latch (Write Data) is written into the first location of RAM. At the negative-going edge of the next clock, the address counter is incremented, the next input data is latched into the input latch, and the new data is then written into the RAM. Loading the RAM continues until one clock after CKEN goes inactive or until the RAM has been fully loaded (135 bytes). While data is being written into the RAM, it is also being output through the multiplexer onto the Data Output (DOUT) lines. Each byte is loaded into the output latch one clock time later than it is written into the RAM. Output of the data during the first scan line permits the Video Display Controller (such as the CRT 8002) to display video on the first scan line. During subsequent scan lines in the data row, the system will disable Write Enable ($\overline{WREN}$) and cause data to be read out from the internal RAM, thereby freeing the system memory for processor access for the remaining N-1 scan lines where N is the number of scan lines per data row.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0° C to + 70° C
Storage Temperature Range ..... -55° C to + 150° C
Lead Temperature (soldering, 10 sec.) ..... +325° C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... -0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS ($T_A = 0°$ C to 70° C, $V_{CC} = +5 \pm 5\%$, unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
DC CHARACTERISTICS					
Input Voltage Levels					
Low Level V_{IL}			0.8	V	
High Level V_{IH}	2.0			V	
Output Voltage Levels					
Low Level V_{OL}			0.4	V	$I_{OL} = 2mA$
High Level V_{OH}	2.4			V	$I_{OH} = -100\mu A$
Input Current Leakage, I_{IL}			10	μA	$0 \leq V_{IN} \leq V_{CC}$
Output '1' Leakage			10	μA	
Output '0' Leakage (Off State)			10	μA	
Input Capacitance					
CLK		30	45	pF	
All other inputs		10	15	pF	
Power Supply Current					
I_{CC} (SRB-135)			115	mA	
I_{CC} (SRB-83)			100	mA	
AC CHARACTERISTICS					
t_{CY}					
(SRB135)	300	250		ns	
(SRB83)	400	330		ns	
t_{CKL}					
(SRB135)	240	190	DC	ns	
(SRB83)	320	250	DC	ns	
t_{CKH}					
(SRB135)	28		5000	ns	
(SRB83)	34		5000	ns	
t_{CKR}					
(SRB135)			10	ns	$t_{CKH} = 28ns$
(SRB83)			10	ns	$t_{CKH} = 34ns$
t_{CKF}					
(SRB135)			10	ns	$t_{CKL} = 240ns$
(SRB83)			10	ns	$t_{CLK} = 320ns$
t_{DSET}	65			ns	
t_{DHOLD}	0			ns	
t_{ENCKP}	0			ns	
t_{ENCKN}					
(SRB135)	100			ns	
(SRB83)	125			ns	
t_{ENHOLD}	0			ns	
t_{WRCKN}					
(SRB135)	100			ns	
(SRB83)	125			ns	
t_{WENHLD}	0			ns	
t_{DOUT}			175	ns	$C_L = 50pF$
t_{TSON}			175	ns	
t_{TSOFF}			175	ns	
t_{OFON}			175	ns	$C_L = 30pF$
t_{CLRS}					
(SRB135)	100			ns	
(SRB83)	125			ns	
t_{CLRH}	0			ns	

FIGURE 1: AC CHARACTERISTICS

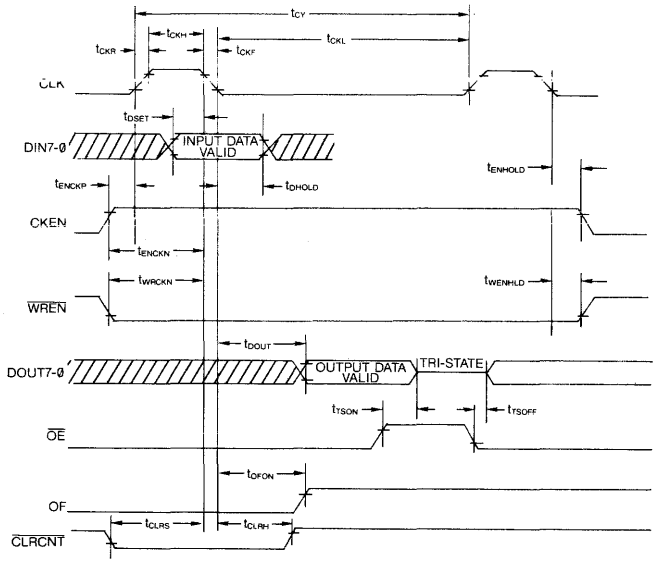


FIGURE 2: SINGLE ROW BUFFER READ TIMING

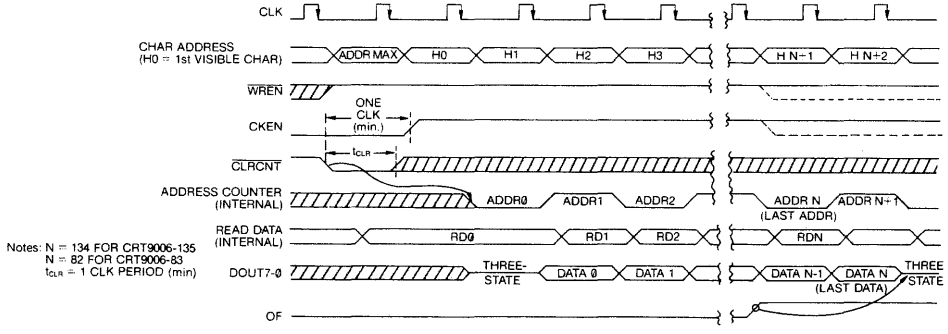
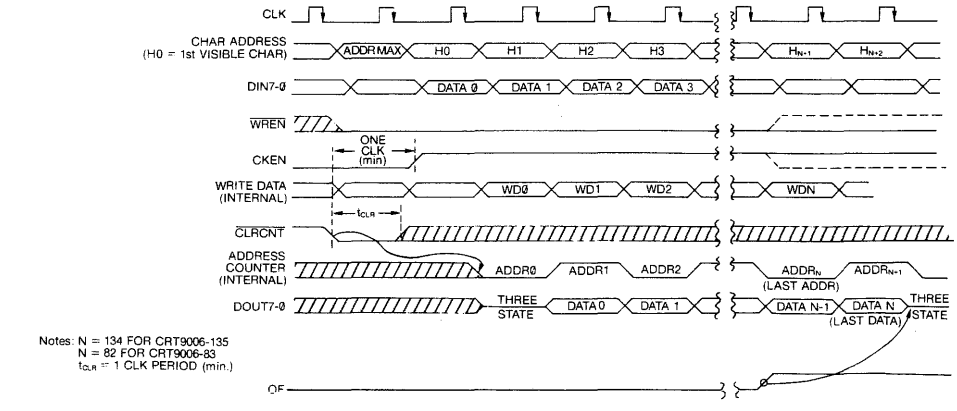


FIGURE 3: SINGLE ROW BUFFER WRITE TIMING



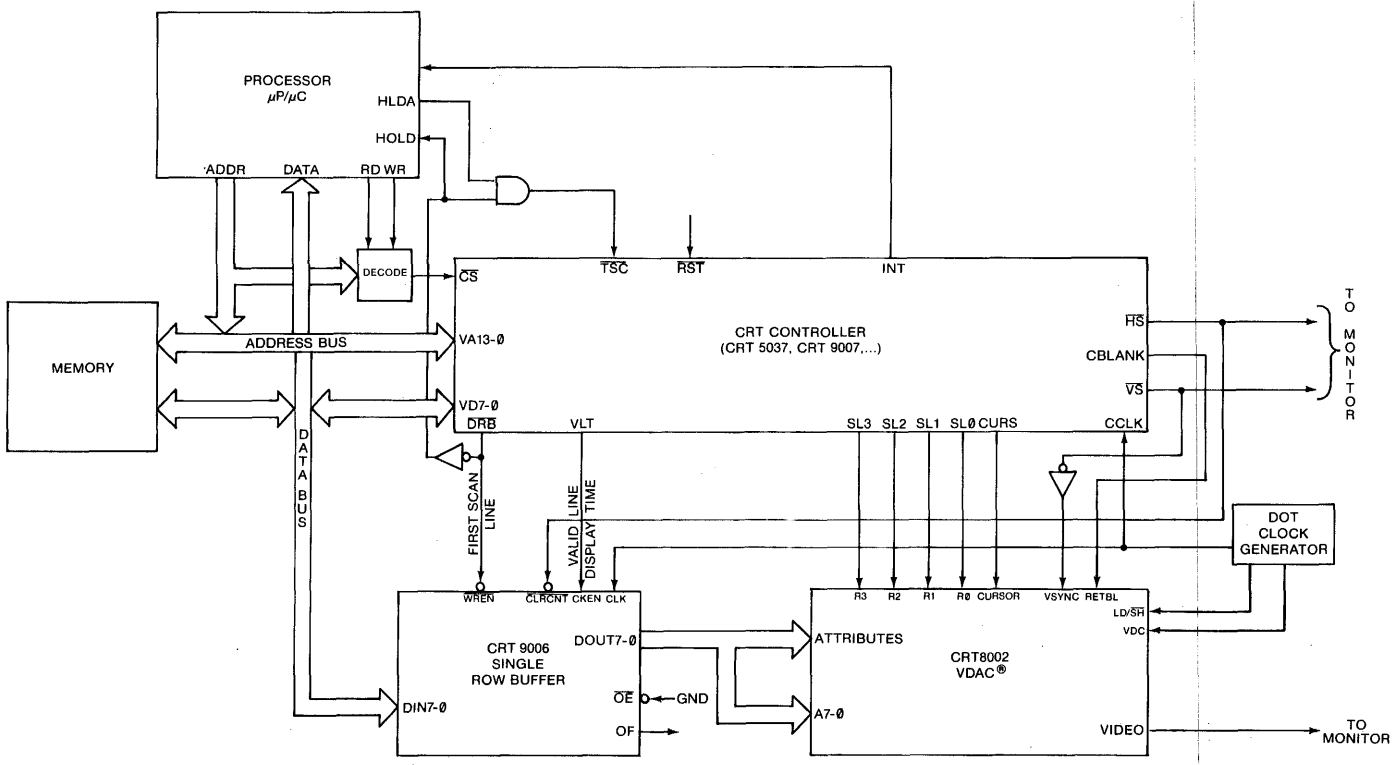
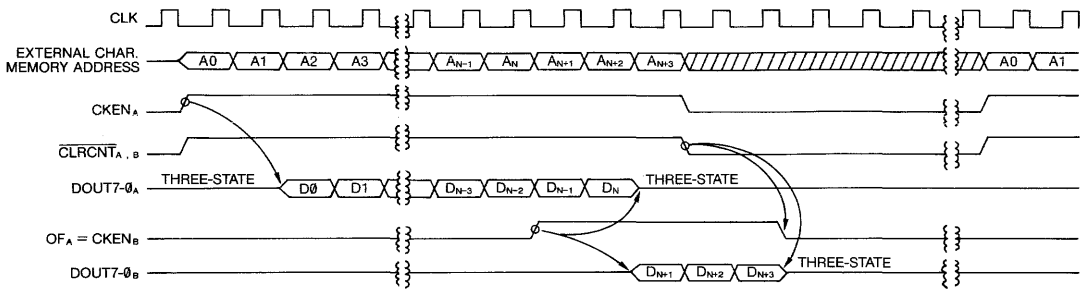


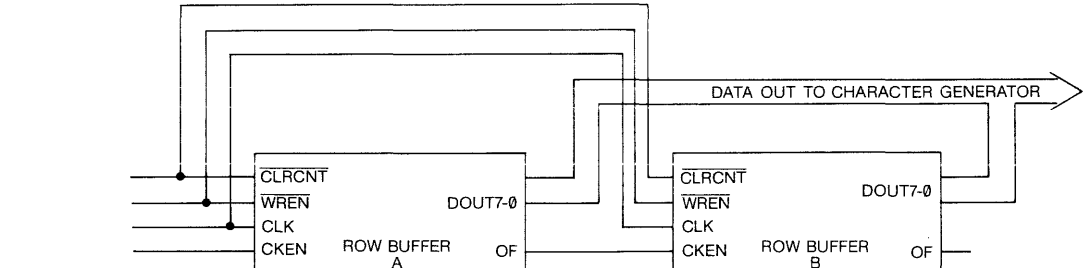
FIGURE 2: TYPICAL CRT CONTROLLER CONFIGURATION WITH SINGLE ROW BUFFER

FIGURE 4:
TYPICAL READ TIMING FOR SRB CASCADED CONFIGURATION



Notes: N = 134 FOR CRT9006-135
N = 82 FOR CRT9006-83
EXAMPLE IS FOR N+3 CHARACTERS TOTAL
A, B REFER TO DEVICES A&B IN FIGURE 5

FIGURE 5:
TYPICAL CASCADE OF SINGLE ROW BUFFERS—270 BYTES TOTAL



STANDARD MICROSYSTEMS CORPORATION

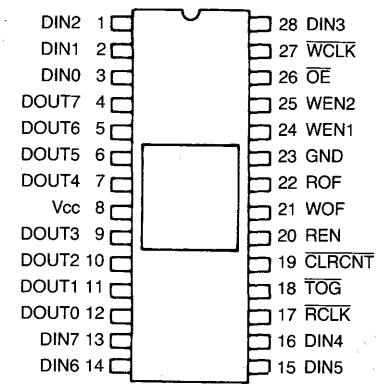
CRT 9212
μPC FAMILY

Double Row Buffer
DRB

FEATURES

- ☐ Low Cost Solution to CRT Memory Contention Problem
- ☐ Provides Enhanced Processor Throughput for CRT Display Systems
- ☐ Replaces Shift Registers or Several RAM and Counter IC's in CRT Display System
- ☐ Permits Display of One Data Row While Next Data Row is Being Loaded
- ☐ Data May be Written into Buffer at Less Than the Video Painting Rate
- ☐ Double Data Row Buffer Permits Second Data Row to be Loaded Anytime during the Display of the Preceding Data Row
- ☐ Permits Active Video on All Scan Lines of Data Row
- ☐ Dynamically Variable Number of Characters per Data Row—...64, 80, 132,...up to a Maximum of 135
- ☐ Cascadable for Data Rows Greater than 135 Characters
- ☐ Stackable for "Invisible Attributes" or Character Widths of Greater than 8 Bits

PIN CONFIGURATION



PACKAGE 28-pin D.I.P.

- ☐ Three-State Outputs
- ☐ Up to 4 MHz Read/Write Data Rate
- ☐ Compatible with SMC CRT 5037, CRT 9007, and other CRT Controllers
- ☐ 28 Pin Dual-In-Line Package
- ☐ +5 Volt Only Power Supply
- ☐ TTL Compatible

SECTION V

GENERAL DESCRIPTION

The CRT 9212 Double Row Buffer (DRB) provides a low cost solution to memory contention between the system processor and the CRT controller in video display systems.

The CRT 9212 DRB is a RAM-based buffer which provides two rows of buffering. It appears to the system as two octal shift registers of dynamically variable length (2-135 bytes) plus steering logic.

The CRT 9212 permits the loading of one data row while the previous data row is being displayed. The loading of data may take place during any of the scan line times of the data row. This relaxed time-constraint allows the processor to perform additional processing on the data or service other high priority interrupt conditions (such as a Floppy Disk DMA request) which may occur during a single video scan line. The result is enhanced processor throughput and flicker-free display of data.

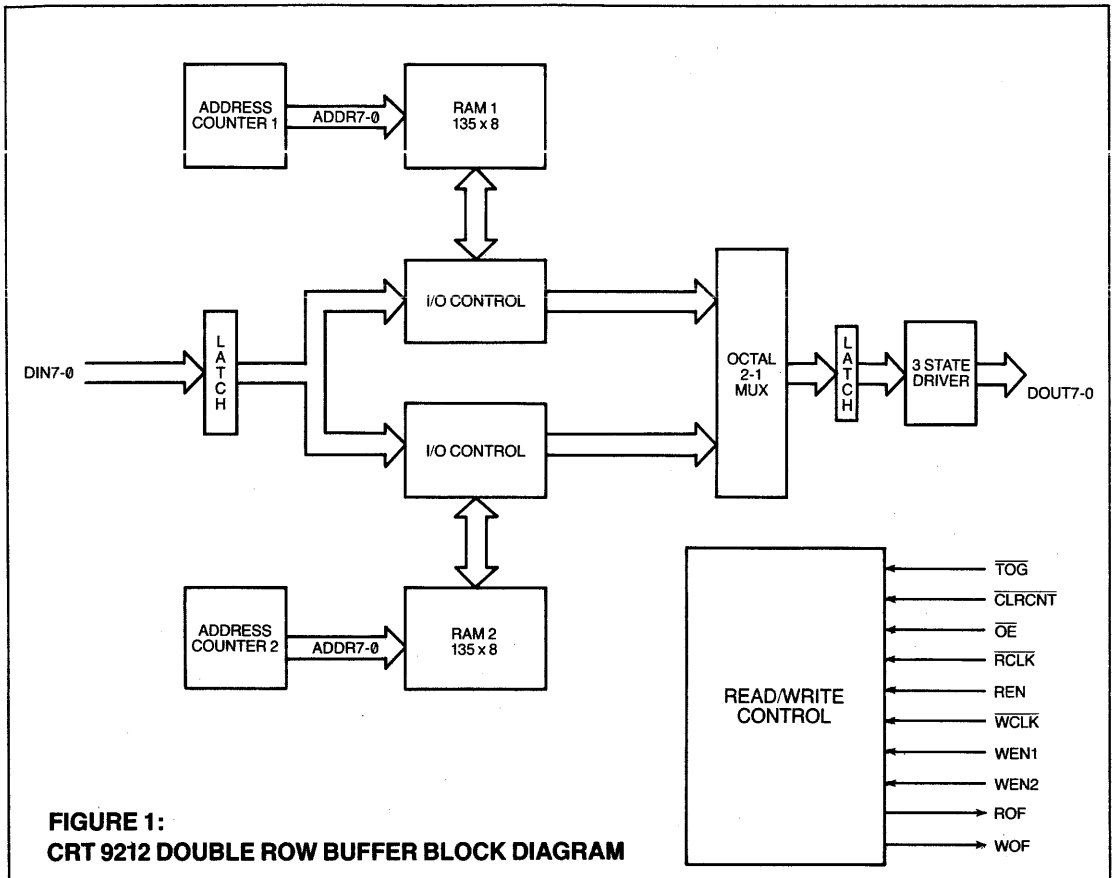


FIGURE 1:
CRT 9212 DOUBLE ROW BUFFER BLOCK DIAGRAM

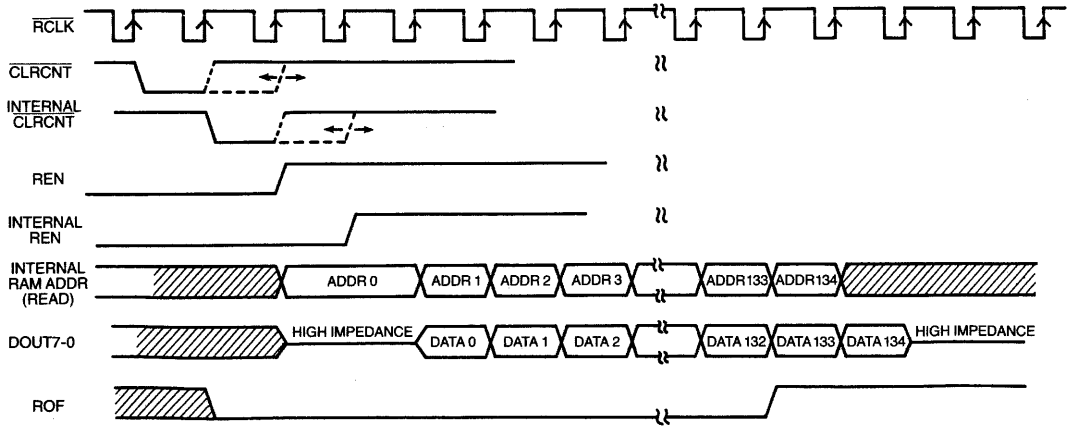


FIGURE 2: CRT 9212 DOUBLE ROW BUFFER READ TIMING

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
3-0, 28, 16-13	Data inputs	DIN0-DIN7	DIN0-DIN7 are the data inputs from the system memory.
12-9, 7-4	Data outputs	DOUT0-DOUT7	DOUT0-DOUT7 are the data outputs from the CRT 9212 internal data output latch. Valid information will appear on DOUT0-DOUT7 two $\overline{RCLK}$ periods after the rising edge of REN. This introduces two pipeline delays when supplying data to the character generator.
17	$\overline{Read\ Clock}$	$\overline{RCLK}$	$\overline{RCLK}$ increments the current "read" address register, clocks data through the "read" buffer and moves data through the internal pipeline at the trailing edge.
18	$\overline{Toggle\ Signal}$	$\overline{TOG}$	$\overline{TOG}$ alternates the function of each buffer between read and write. $\overline{TOG}$ normally occurs at every data row boundary. Switching of the buffers occurs when both $\overline{TOG}$ and $\overline{CLRCNT}$ are low.
19	$\overline{Clear\ Counter}$	$\overline{CLRCNT}$	$\overline{Clear\ Counter}$ clears the current "read" address counter at the next $\overline{RCLK}$ positive edge. $\overline{CLRCNT}$ is normally asserted low at the beginning of each horizontal retrace interval. $\overline{CLRCNT}$ clears the current "write" address counter when the $\overline{TOG}$ is active.
20	Read Enable	REN	REN enables the loading of data from the selected "read" buffer into the output latch. Data is loaded when $\overline{Read\ Clock}$ is active.
21	Write Overflow	WOF	WOF high indicates that data is being written into the last memory position (position 135). When WOF is high, further writing into the selected "write" buffer is disabled. WOF may be connected to the WEN1 or WEN2 inputs of a second CRT 9212 for cascaded operation where data row lengths of greater than 135 characters are desired. See figure 4.
22	Read Overflow	ROF	The Read Overflow output is high when data is being read from the last memory position (position 135). ROF high disables further reading from the selected "read" buffer. ROF may be connected to the REN input of a second CRT 9212 for cascaded operation where data row lengths of greater than 135 characters are desired. DOUT0-7 will switch into a high impedance state at the second positive transition of $\overline{RCLK}$ after ROF goes high. See figure 4.
24, 25	Write Enable	WEN1, WEN 2	WEN allows input data to be written into the selected "write" buffer during $\overline{WCLK}$ active. Both WEN1 and WEN 2 must be high to enable writing. WEN1 has an internal pullup resistor allowing it to assume a high if pin 24 is left open.
26	$\overline{Output\ Enable}$	$\overline{OE}$	When the $\overline{OE}$ input is low, the data outputs DOUT0-DOUT7 are enabled. When $\overline{OE}$ is high, DOUT0-DOUT7 present a high impedance state. $\overline{OE}$ has an internal pulldown resistor allowing it to assume a low if pin 26 is left open.
27	$\overline{Write\ Clock}$	$\overline{WCLK}$	$\overline{WCLK}$ clocks input data into the selected "write" buffer and increments the current "write" address register when WEN1 and WEN2 are high.
8	Power Supply	V_{CC}	+5 Volt supply
23	Ground	GND	Ground

OPERATION

Figure 1 illustrates the internal architecture of the CRT 9212. It contains 135 bytes of RAM in each of its two buffers. In normal operation, data is written into the input latch on the positive-going edge of Write Clock ($\overline{WCLK}$). When both Write Enable (WEN1, WEN 2) signals go high, the next $\overline{WCLK}$ causes data from the input latch to be written into the selected buffer (1 or 2) and the associated address counter to be incremented by one. Loading of the selected RAM buffer continues until WEN goes inactive or until the buffer has been fully loaded. At the next data row boundary, the $\overline{Toggle\ Signal}$ ($\overline{TOG}$) will go low. When $\overline{Clear\ Counter}$ ($\overline{CLRCNT}$) goes low, the next $\overline{Read\ Clock}$ ($\overline{RCLK}$) will begin to reset both buffer address counters to zero, switching the buffer just loaded from a "write buffer" to a "read buffer", permitting the next row of data to be written into the other buffer. Data from the current "read" buffer is read out of the buffer and to the output latch whenever Read Enable (REN) is high during a $\overline{Read\ Clock}$ ($\overline{RCLK}$). Each read-out from the buffer RAM causes the "read" address counter to be incremented. REN is normally high during the entire visible line time of each scan line of the data row. $\overline{CLRCNT}$ resets the present "read" address counter. The negative edge of $\overline{CLRCNT}$ is detected by the CRT 9212 and the internal "read" address counter is cleared independent of the $\overline{CLRCNT}$ pulse width. The $\overline{CLRCNT}$ input may be tied to the REN input for proper operation.

Figures 2 and 3 illustrate the functional timing for reading and writing the CRT 9212. It is possible to cascade two or more CRT 9212's to allow for data storage greater than 135 bytes by employing the read overflow (ROF) and write overflow (WOF) outputs. Figure 4 illustrates two CRT 9212's cascaded together.

The CRT 9212 is compatible with the CRT 9007 video processor and controller (VPAC™) and the CRT 8002 video display attributes controller (VDAC™). A typical video configuration employing the three parts is illustrated in figure 5.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%)

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low Level V_{IL}			0.8	V	
High Level V_{IH1}	2.0			V	excluding $\overline{RCLK}$; $\overline{WCLK}$
High Level V_{IH2}	4.2			V	$\overline{RCLK}$, $\overline{WCLK}$
OUTPUT VOLTAGE LEVELS					
Low Level V_{OL}			0.4	V	
High Level V_{OH}	2.4			V	
INPUT LEAKAGE CURRENT					
High Leakage I_{LH1}			10	µA	excluding $\overline{OE}$
Low Leakage I_{LL1}			10	µA	excluding WEN1
High Leakage I_{LH2}			400	µA	WEN1
Low Leakage I_{LL2}			400	µA	$\overline{OE}$
INPUT CAPACITANCE					
C_{IN1}		10		pF	excluding $\overline{RCLK}$, $\overline{WCLK}$
C_{IN2}		15		pF	$\overline{RCLK}$, $\overline{WCLK}$
POWER SUPPLY CURRENT					
I_{CC}		100		mA	

AC CHARACTERISTICS[1]

t_{CYW}	300			ns	Write clock period
t_{CYR}	300			ns	Read clock period
t_{CKH}	247		DC	ns	
t_{CKL}	33			ns	
t_{CKR}			10	ns	measured from 10% to 90% points
t_{CKF}			10	ns	measured from 90% to 10% points
t_{DS}	50			ns	referenced to $\overline{WCLK}$
t_{DH}	0			ns	referenced to $\overline{WCLK}$
t_{EN1}[2]	0			ns	
t_{EN2}[2]	100			ns	
t_{ENH}[2]	0			ns	
t_{DV}			175	ns	C_L = 50 pF; referenced from $\overline{RCLK}$
t_{DOFF}			175	ns	
t_{DON}			175	ns	
t_{OF}[3]			175	ns	C_L = 30 pF
t_{CS}	100			ns	
t_{CH}	0			ns	
t_{WT}[4]		$1t_{CYW}$			

1 - Reference points for all AC parameters are 2.4V high and 0.4V low.
2 - For REN, referenced from $\overline{RCLK}$; for WEN1 or WEN2 referenced to $\overline{WCLK}$.
3 - For ROF, referenced from $\overline{RCLK}$; for WOF referenced from $\overline{WCLK}$.
4 - At least 1 WCLK rising edge must occur between $\overline{CLRCNT}$ or $\overline{TOG}$ (whichever occurs last) and WEN (= WEN1-WEN2).

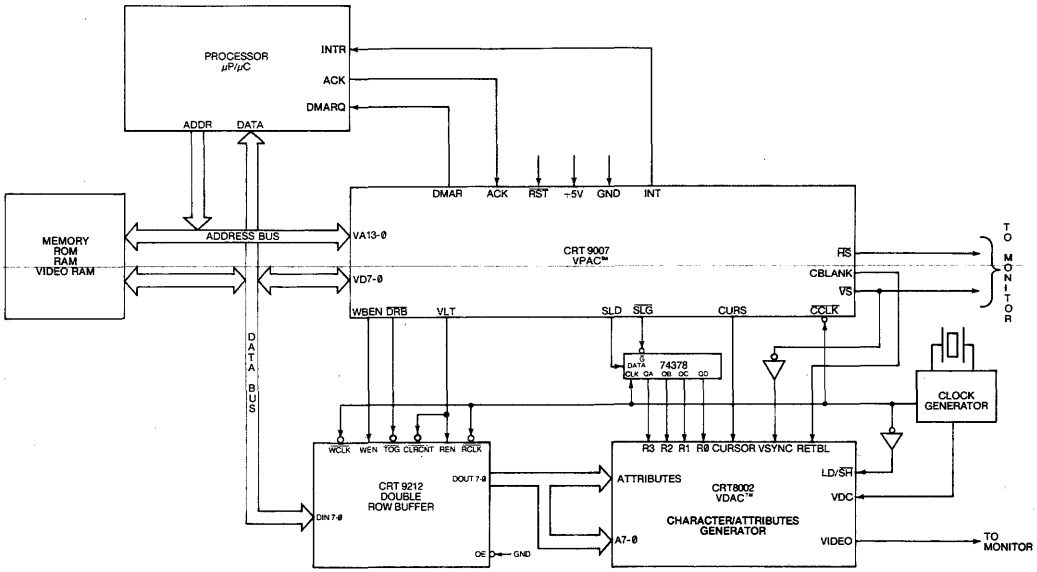


FIGURE 5: CRT 9212 CONFIGURED WITH THE CRT 9007 VPAC AND THE CRT 8002 VDAC™

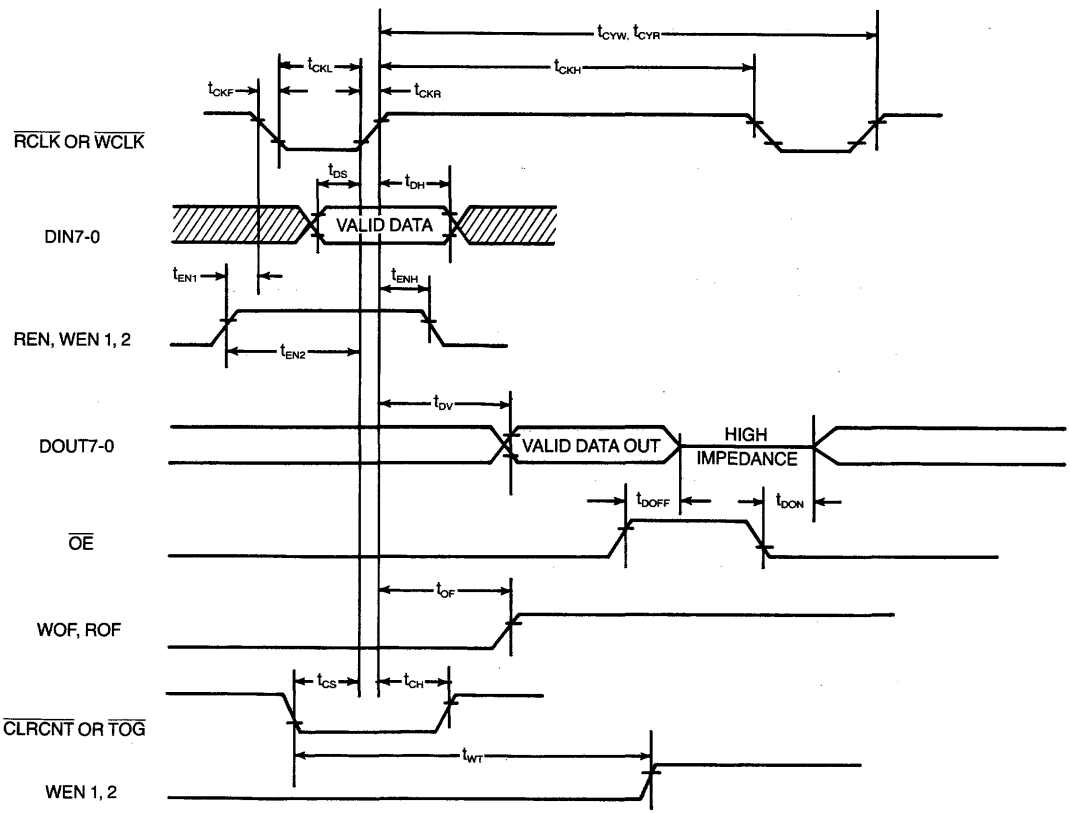
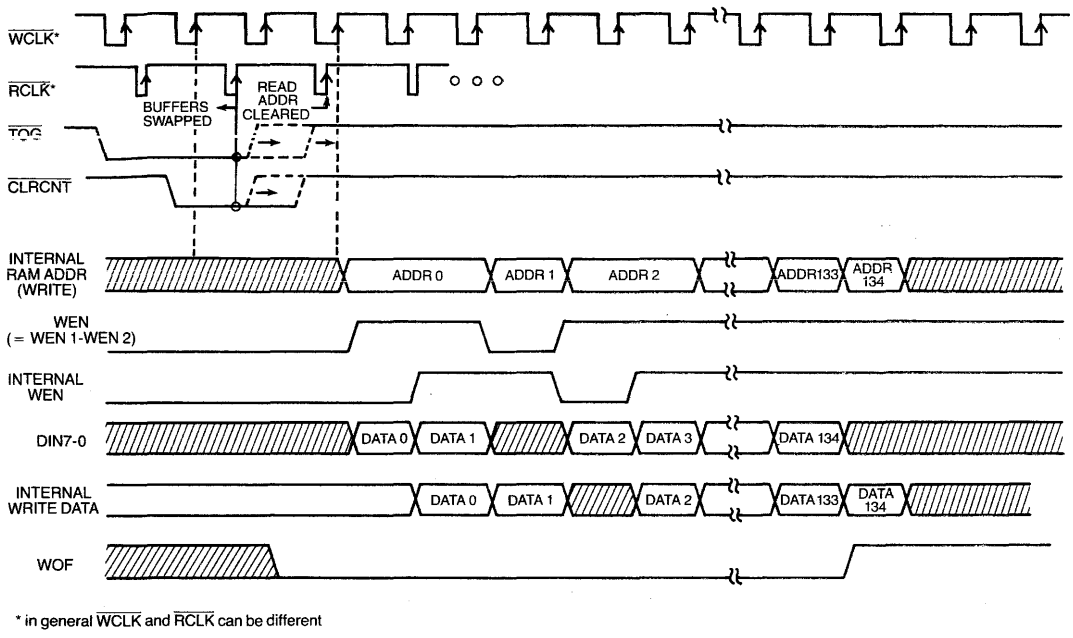


FIGURE 6: CRT 9212 I/O TIMING



* in general WCLK and RCLK can be different

FIGURE 3: CRT 9212 DOUBLE ROW BUFFER WRITE TIMING

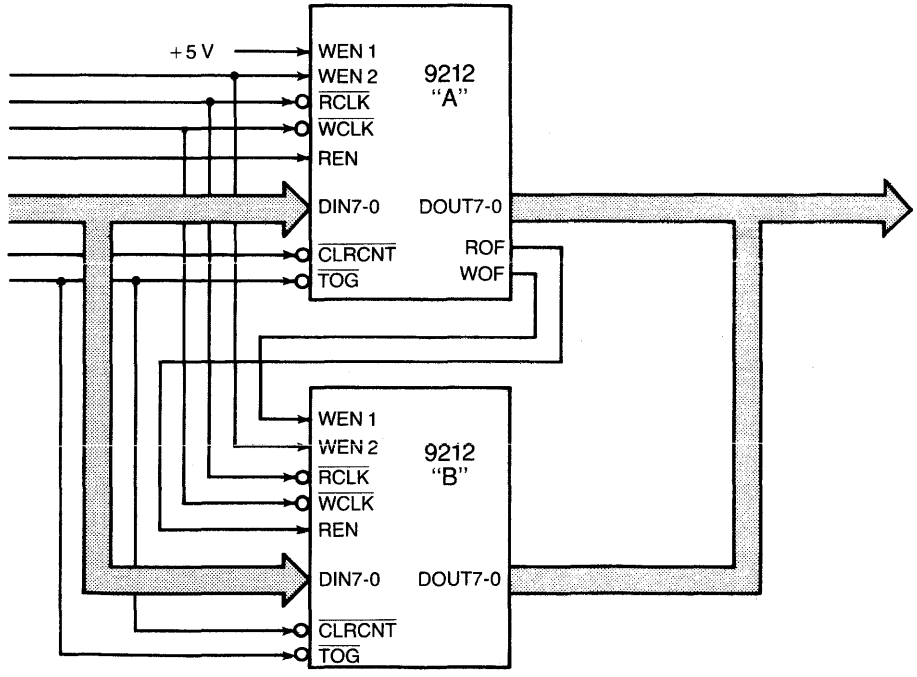


FIGURE 4: CRT 9212 CASCADED CONFIGURATION FOR DATA ROW LENGTHS UP TO 270 CHARACTERS

STANDARD MICROSYSTEMS CORPORATION

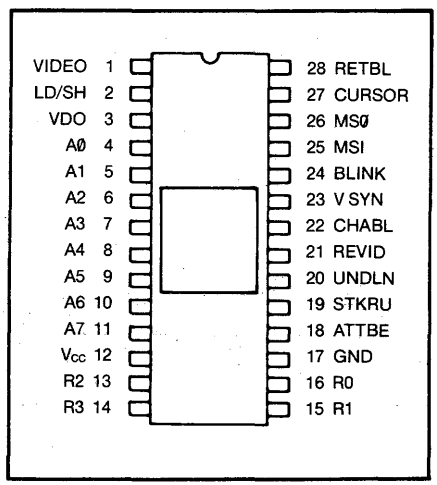
CRT 8021
CRT 8021-003
μPC FAMILY

CRT Video Attributes Controller
Video Generator
VAC

FEATURES

- ☐ ON CHIP VIDEO SHIFT REGISTER
  Maximum shift register frequency—20MHz
  Maximum character clock rate—2.5MHz
- ☐ ON CHIP HORIZONTAL AND VERTICAL RETRACE VIDEO BLANKING
- ☐ ON CHIP GRAPHICS GENERATION
- ☐ ON CHIP ATTRIBUTE LOGIC-CHARACTER, FIELD
  Reverse video
  Character blank
  Character blink
  Underline
  Strike-thru
- ☐ ON CHIP BLINKING CURSOR
- ☐ ON CHIP DATA BUFFER
- ☐ ON CHIP ATTRIBUTE BUFFER
- ☐ +5 VOLT OPERATION
- ☐ TTL COMPATIBLE
- ☐ MOS N-CHANNEL SILICON-GATE COPLAMOS® PROCESS

PIN CONFIGURATION



- ☐ COMPATIBLE WITH CRT 5027/37 VTAC® AND CRT 9007 VPAC

GENERAL DESCRIPTION

The SMC CRT 8021 Video Attributes Controller (VAC) is an n-channel COPLAMOS® MOS/LSI device. It contains wide and thin graphics logic, attributes logic, a data latch, field and character attribute latch, a blinking cursor, and a high speed video shift register. The CRT 8021 VAC is a companion to SMC's CRT 5027/37 VTAC® or CRT 9007 VPAC. The CRT 8021 and a character ROM combined with either a CRT 5027/37 or a CRT 9007 comprises the major circuitry required for the display portion of a CRT video terminal.

The CRT 8021 video output may be connected directly to a CRT monitor video input. The CRT 5027/37 or CRT 9007 blanking output can be connected directly to the CRT 8021 retrace blank input to provide both horizontal and vertical retrace blanking of the video output.

A blinking cursor is available on the CRT 8021. There is a separate cursor blink rate which is twice the character blink rate and has a duty cycle of 50/50.

The CRT 8021 attributes include: reverse video, character blank, blink, underline, and strike-thru. The character blink rate has a duty cycle of 75/25. The underline and strike-thru are similar but independently controlled functions. These attributes are available in all modes.

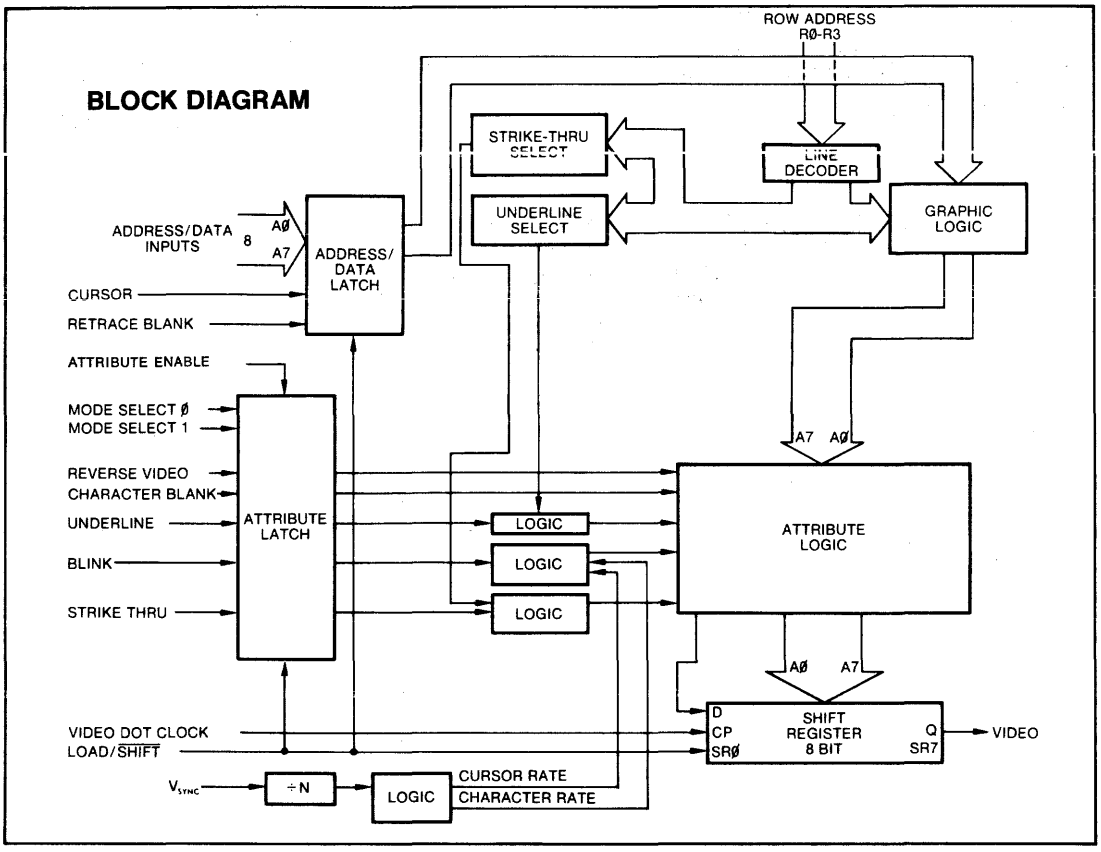
The thin graphic mode enables the user to create single line drawings and forms.

In the wide graphic mode the CRT 8021 produces a graphic entity the size of the character block. The graphic entity contains 8 parts, each of which is associated with one bit of a graphic byte, thereby providing 256 unique graphic symbols. Thus, the CRT 8021 can produce either alphanumeric symbols or various graphic entities depending on the mode selected. The mode can be changed on a per character basis.

The CRT 8021 is available in two versions. The CRT 8021 provides an eight-part graphic entity which fills the character block. The CRT 8021 is designed for seven dot wide, nine or eleven dot high characters in nine by twelve or ten by twelve character blocks.

The CRT 8021-003 provides a six part graphic entity for five by seven or five by nine characters in character blocks of up to seven by ten dots.

BLOCK DIAGRAM



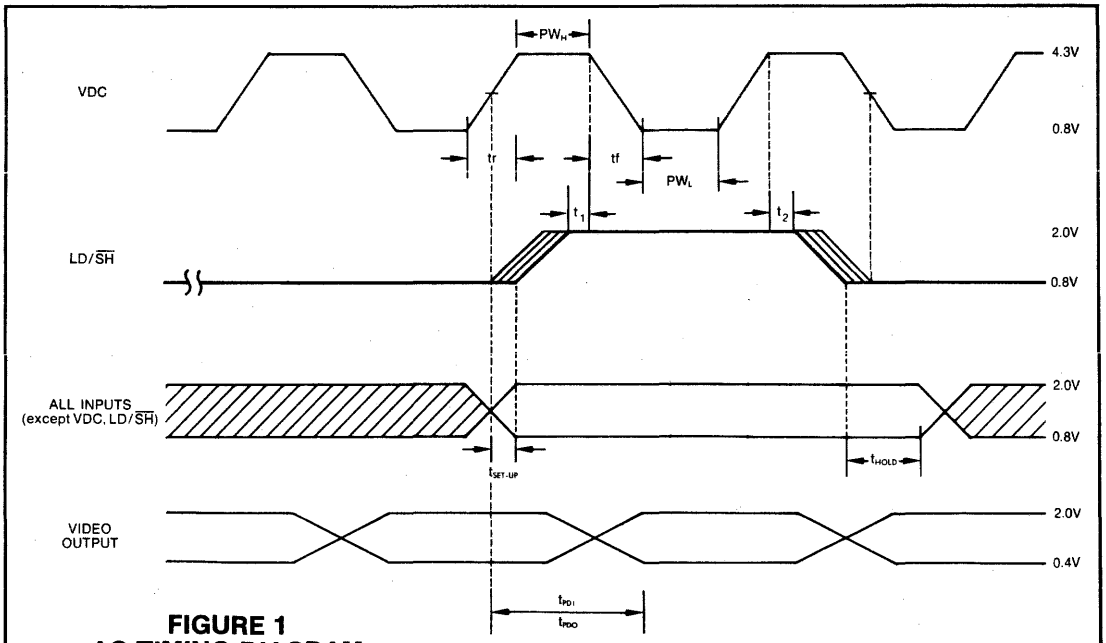


FIGURE 1
AC TIMING DIAGRAM

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	excluding VDC
High-level, V_{IH}	2.0			V	excluding VDC
INPUT VOLTAGE LEVELS-CLOCK					
Low-level, V_{IL}			0.8	V	
High-level, V_{IH}	4.3			V	See Figure 7
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	$I_{OL} = 0.4$ mA, 74LSXX load
High-level, V_{OH}	2.4			V	$I_{OH} = -20\ \mu A$
INPUT CURRENT					
Leakage, I_L (Except CLOCK)			10	μA	$0 \leq V_{IN} \leq V_{CC}$
Leakage, I_L (CLOCK Only)			50	μA	$0 \leq V_{IN} \leq V_{CC}$
INPUT CAPACITANCE					
Data		10		pF	@ 1 MHz
LD/$\overline{SH}$		20		pF	@ 1 MHz
CLOCK		25		pF	@ 1 MHz
POWER SUPPLY CURRENT					
I_{CC}		100		mA	
A.C. CHARACTERISTICS					
See Figure 6, 7					

SYMBOL	PARAMETER	CRT 8021		UNITS
		MIN.	MAX.	
VDC	Video Dot Clock Frequency	1.0	20	MHz
PW_H	VDC—High Time	15.0		ns
PW_L	VDC—Low Time	15.0		ns
t_{CY}	LD/$\overline{SH}$ cycle time	400		ns
t_r, t_f	Rise, fall time		10	ns
t_{SET-UP}	Input set-up time	≥0		ns
t_{HOLD}	Input hold time	15		ns
t_{PDI}, t_{PDO}	Output propagation delay	15	50	ns
t_1	LD/$\overline{SH}$ set-up time	10		ns
t_2	LD/$\overline{SH}$ hold time	5		ns

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
1	VIDEO	Video Output	O	The video output contains the dot stream for the selected row of the wide graphic, thin graphic, or external character after processing by the attribute logic, and the retrace blank and cursor inputs. The timing of the Load/$\overline{\text{Shift}}$ pulse will determine the number of additional (— —, zero to N) backfill zeros (or ones if in REVID) shifted out. See figure 4. When the next Load/$\overline{\text{Shift}}$ pulse appears the next character via the attribute logic, is parallel loaded into the shift register and the cycle repeats.
2	LD/$\overline{\text{SH}}$	Load/$\overline{\text{Shift}}$	I	The 8 bit shift-register parallel-in load or serial-out shift modes are established by the Load/$\overline{\text{Shift}}$ input. When low, this input enables the shift register for serial shifting with each Video Dot Clock pulse. When high, the shift register parallel (broadside) data inputs are enabled and synchronous loading occurs on the next Video Dot Clock pulse. During parallel loading, serial data flow is inhibited. The Address/Data inputs (AØ-A7) are latched on the negative transition of the Load/$\overline{\text{Shift}}$ input. See timing diagram, figure 1.
3	VDC	Video Dot Clock	I	Frequency at which video is shifted.
4-11	AØ-A7	Address/Data	I	In the External Mode, AØ-A7 is used to insert an 8 bit word from a user defined external ROM, PROM or RAM into the on-chip Attribute logic. In the wide Graphic Mode AØ-A7 is used to define one of 256 graphic entities. In the thin Graphic Mode AØ-A2 is used to define the 3 line segments.
12	V_{CC}	Power Supply	PS	+5 volt power supply.
13, 14, 15, 16	R2, R3, R1, RØ	Row Address	I	These 4 binary inputs define the row address in the current character block.
17	GND	Ground	GND	Ground
18	ATTBE	Attribute Enable	I	A positive level on this input enables data from the Reverse Video, Character Blank, Underline, Strike-Thru, Blink, Mode Select Ø, and Mode Select 1 inputs to be strobed into the on-chip attribute latch at the negative transition of the Load/$\overline{\text{Shift}}$ pulse. The latch loading is disabled when this input is low. The latched attributes will remain fixed until this input becomes high again. To facilitate attribute latching on a character by character basis, tie ATTBE high. See timing diagram, figure 1.
19	STKRU	Strike-Thru	I	When this input is high and RETBL = 0, the parallel inputs to the shift register are forced high (SRØ-SR7), providing a solid line segment throughout the character block. The operation of strike-thru is modified by Reverse Video (see table 1). The strike-thru is a double line on rows R5 and R6 for the CRT 8021 and a single line on row R4 for the CRT 8021-003.
20	UNDLN	Underline	I	When this input is high and RETBL = 0, the parallel inputs to the shift register are forced high (SRØ-SR7), providing a solid line segment throughout the character block. The operation of underline is modified by Reverse Video (see table 1). The underline is a single line of R11 for the CRT 8021 and a single line on R8 for the CRT 8021-003.
21	REVID	Reverse Video	I	When this input is low and RETBL = 0, data into the Attribute Logic is presented directly to the shift register parallel inputs. When reverse video is high data into the Attribute Logic is inverted and then presented to the shift register parallel inputs. This operation reverses the data and field video. See table 1.
22	CHABL	Character Blank	I	When this input is high, the parallel inputs to the shift register are all set low, providing a blank character line segment. Character blank will override blink. The operation of Character Blank is modified by the Reverse Video input. See table 1.
23	V SYNC	V SYNC	I	This input is used as the clock input for the two on-chip blink rate dividers. The cursor blink rate (50/50 duty cycle) will be twice the character blink rate (75/25 duty cycle).
24	BLINK	Blink	I	When this input is high and RETBL = 0 and CHABL = 0, the character will blink at the character blink rate. Blinking is accomplished by blanking the character block with the internal Character Blink clock. The character blink rate is 1.875 Hz when V SYNC = 60 Hz.
25 26	MS1 MSØ	Mode Select 1 Mode Select Ø	I I	These 2 inputs define the three modes of operation of the CRT 8002 as follows: Thin Graphics Mode — In this mode AØ-A2, (A3-A7 = X) will be loaded into the thin graphic logic along with the row addresses. This logic will define the segments of a graphic entity as defined in figure 6. Character Mode — In this mode the inputs AØ-A7 go directly from the character latch into the shift register via the attribute logic. Thus the user may define external character fonts or graphic entities in an external PROM, ROM or RAM. See figure 3. Wide Graphics Mode — In this mode the inputs AØ-A7 will define a graphic entity as described in figure 5. Each line of the graphic entity is determined by the wide graphic logic in conjunction with the row inputs RØ to R3. In this mode each segment of the entity is defined by one of the bits of the 8 bit word. Therefore, the 8 bits can define any 1 of the 256 possible graphic entities. These entities can butt up against each other to form a contiguous pattern or can be interspaced with alphanumeric characters. Each of the entities occupies the space of 1 character block and thus requires 1 byte of memory. These 3 modes can be intermixed on a per character basis.
27	CURSOR	Cursor	I	When this input is enabled the cursor will be activated. The cursor will be a blinking (at 3.75 Hz when V SYNC = 60 Hz) reverse video block. In this mode the Character Block is set to reverse video at the cursor blink rate. The Character Block will alternate between normal video and reverse video.
28	RETBL	Retrace Blank	I	When this input is latched high, the shift register parallel inputs are unconditionally cleared to all zeros and loaded into the shift register on the next Load/$\overline{\text{Shift}}$ pulse. This blanks the video, independent of all attributes, during horizontal and vertical retrace time.

MS1	MSØ	MODE
1	0	Thin Graphics
0	1	Character Mode
0	0	Wide Graphics

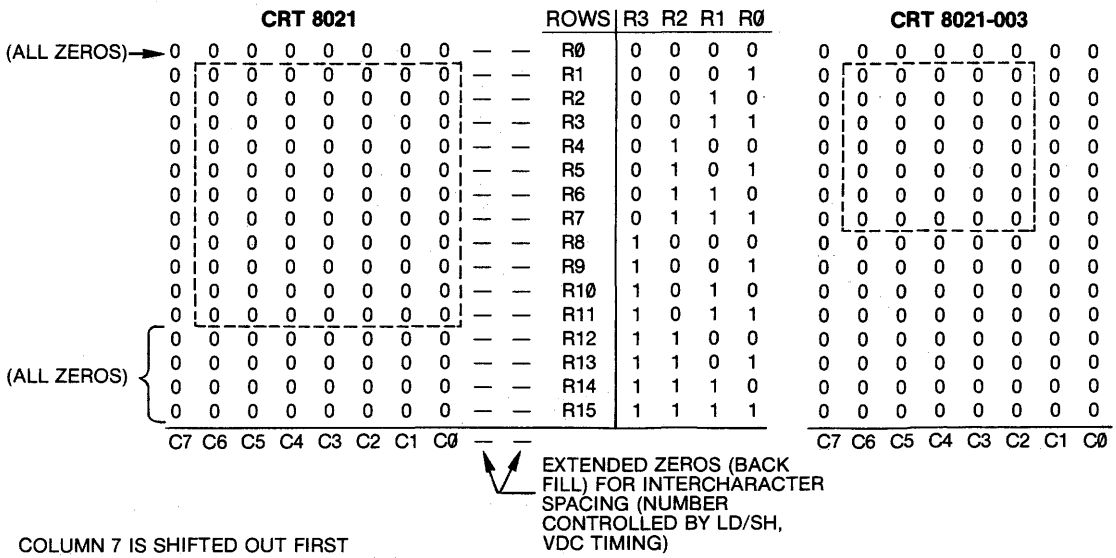
TABLE 1

CURSOR	RETBL	REVID	CHABL	UNDLN*	FUNCTION
X	1	X	X	X	"0" (S.R.) All
0	0	0	0	0	D (S.R.) All
0	0	0	0	1	"1" (S.R.)*
					D (S.R.) All others
0	0	0	1	X	"0" (S.R.) All
0	0	1	0	0	$\overline{D}$ (S.R.) All
0	0	1	0	1	"0" (S.R.)*
					$\overline{D}$ (S.R.) All others
0	0	1	1	X	"1" (S.R.) All
Blink** REVID Block	0	0	0	0	Alternate Normal Video/REVID At Cursor Blink Rate
Blink** REVID Block	0	0	0	1	
Blink** REVID Block	0	0	1	X	
Blink** REVID Block	0	1	0	0	
Blink** REVID Block	0	1	0	1	
Blink** REVID Block	0	1	1	X	

*At Selected Row Decode **At Cursor Blink Rate

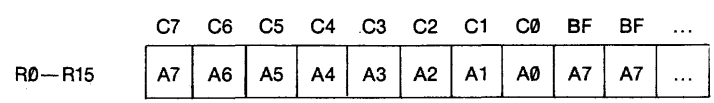
Note: If Character is Blinking at Character Rate, Cursor will change it to Cursor Blink Rate

FIGURE 2
TYPICAL CHARACTER MODE BLOCK FORMATS



Note: Dotted line shows typical character display area.

FIGURE 3
CHARACTER MODE
MSØ = 1 MS1= Ø



BF = back fill

FIGURE 4. TYPICAL VIDEO OUTPUT—CHARACTER MODE

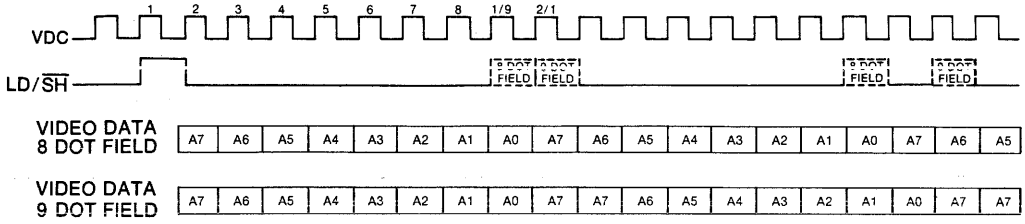
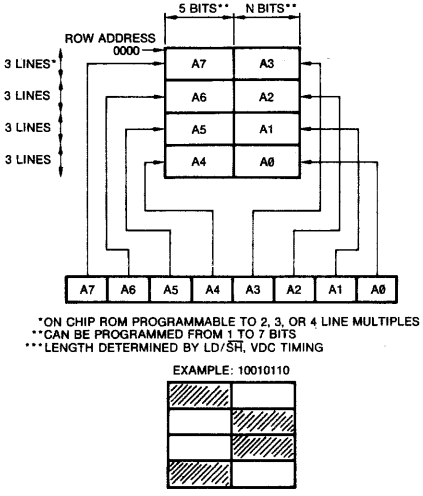


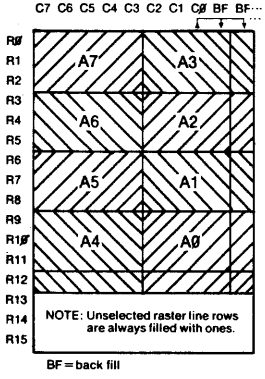
FIGURE 5
WIDE GRAPHICS MODE
MSØ = Ø MS1 = Ø



*ON CHIP ROM PROGRAMMABLE TO 2, 3, OR 4 LINE MULTIPLES
**CAN BE PROGRAMMED FROM 1 TO 7 BITS
***LENGTH DETERMINED BY LD/SH, VDC TIMING

EXAMPLE: 10010110

CRT 8021



BF = back fill

CRT 8021-003

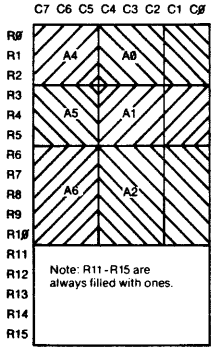
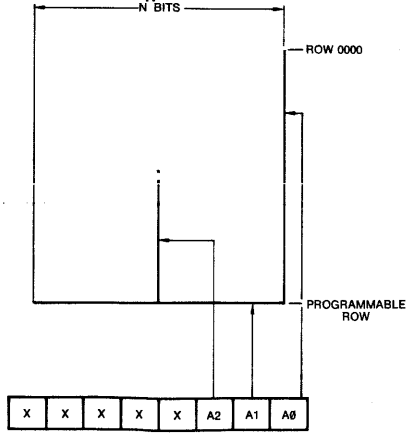
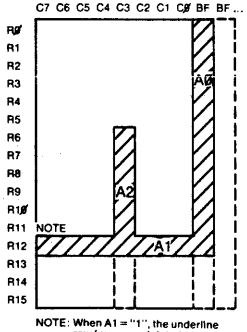


FIGURE 6
THIN GRAPHICS MODE
MSØ = Ø MS1 = 1



X = DON'T CARE
* THE INSIDE SEGMENT IS MASK PROGRAMMABLE TO ROW 0000
** LENGTH DETERMINED BY LD/SH, VDC TIMING

CRT 8021



NOTE: When A1 = "1", the underline row/rows are deleted.
When A1 = "0", the underline, if selected, will appear.

BF = back fill

CRT 8021-003

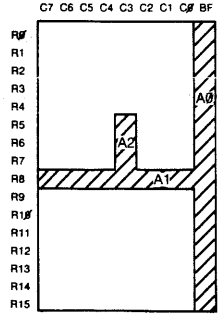


FIGURE 7

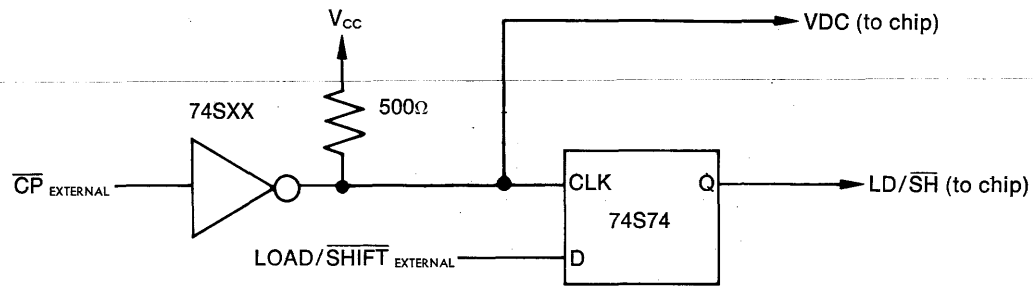
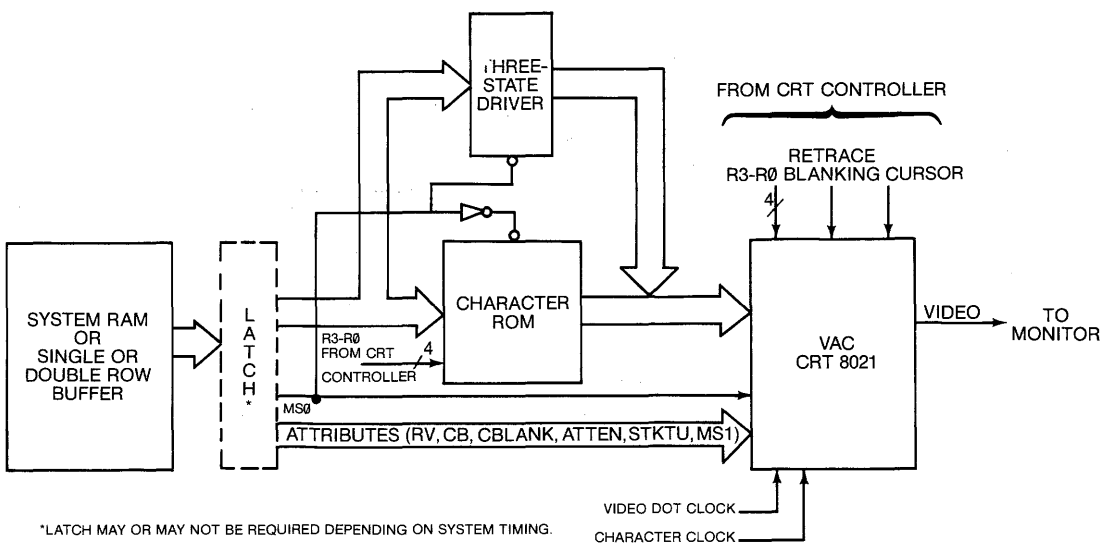
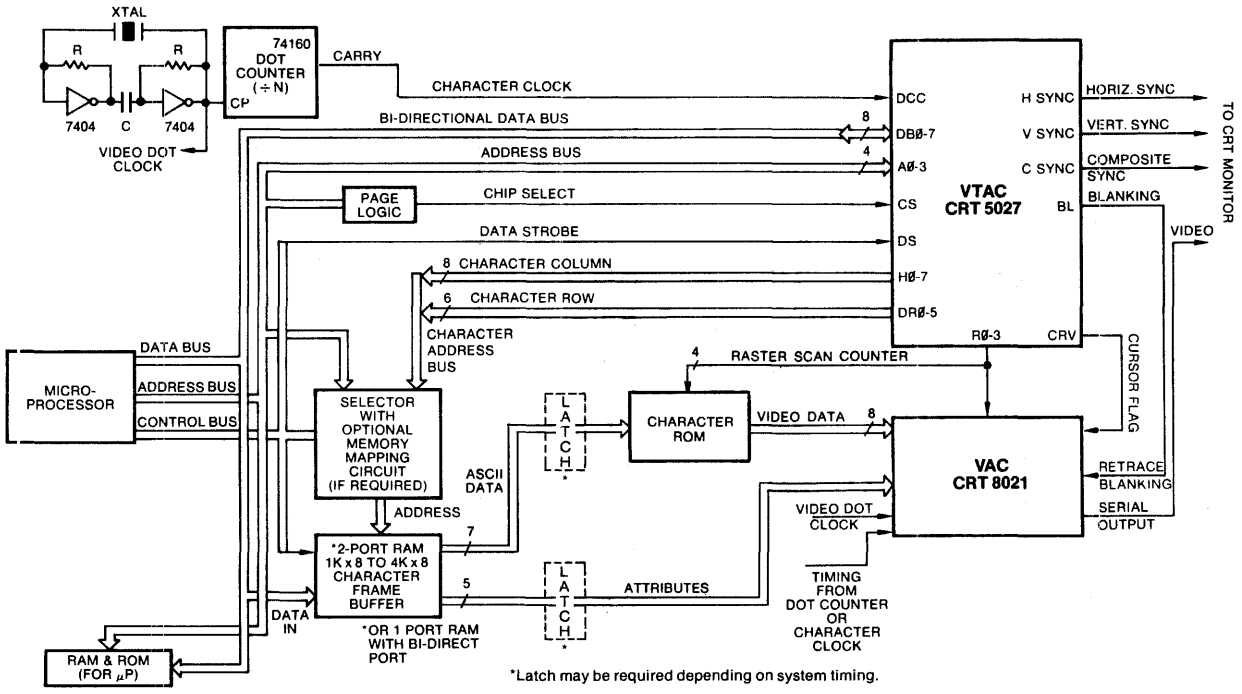


FIGURE 8
TYPICAL CRT 8021 CONFIGURATION FOR COMBINED CHARACTER AND GRAPHICS MODES



*LATCH MAY OR MAY NOT BE REQUIRED DEPENDING ON SYSTEM TIMING.



*Latch may be required depending on system timing.

FIGURE 9. CRT 8021 TYPICAL μP CONFIGURATION (CHARACTER MODE ONLY)

STANDARD MICROSYSTEMS CORPORATION

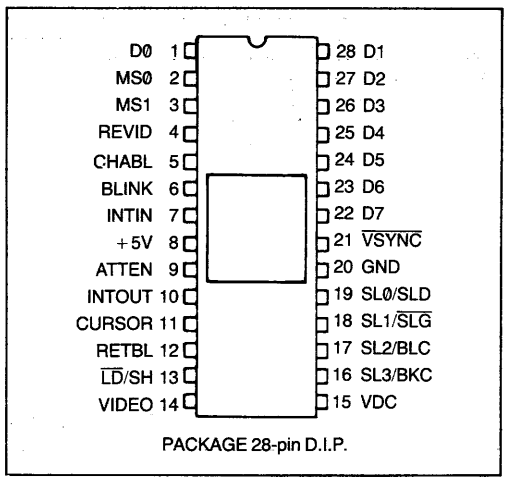
CRT 9021A
CRT 9021B
µPC FAMILY

CRT Video Attributes Controller VAC

FEATURES

- ☐ On chip video shift register
  Maximum shift register frequency
  CRT 9021A 30 MHz
  CRT 9021B 28.5 MHz
- ☐ On chip attributes logic
  Reverse video
  Character blank
  Character blink
  Underline
  Full/half intensity
- ☐ Four modes of operation
  Wide graphics
  Thin graphics
  Character mode without underline
  Character mode with underline
- ☐ On Chip logic for double height/double width characters
- ☐ Accepts scan line information in parallel or serial format
- ☐ Four cursor modes dynamically selectable via 2 input pins
  Underline
  Blinking underline
  Reverse video
  Blinking reverse video
- ☐ Programmable character blink rate

PIN CONFIGURATION



PACKAGE 28-pin D.I.P.

- ☐ Programmable cursor blink rate
- ☐ On chip data and attribute latches
- ☐ +5 volt operation
- ☐ TTL compatible
- ☐ MOS n-Channel silicon gate COPLAMOS® process
- ☐ Compatible with CRT 5037 VTAC®; CRT 9007 VPAC™

GENERAL DESCRIPTION

The SMC CRT 9021 Video Attributes Controller (VAC) is an n-channel COPLAMOS MOS/LSI device containing Graphics logic, attributes logic, data and attributes latches, cursor control, and a high speed video shift register. The CRT 9021, a character generator ROM and a CRT controller such as the CRT 9007 provide all of the major circuitry for the display portion of a CRT video terminal.

The CRT 9021 serial video output may be connected directly to a CRT monitor's video input. The maximum video shift register frequency of 28.5 MHz or 30 MHz allows for CRT displays of up to 132 characters per data row.

The CRT 9021 attributes include: reverse video, underline, character blank, character blink, and full/half intensity selection. In addition, when used in conjunction with the CRT 9007 VPAC,™ the CRT 9021 will provide double height or double width characters.

Four programmable cursor modes are provided on the CRT 9021. They are: underline, blinking underline, reverse video character block, and blinking reverse video character block. When used in the serial scan line input mode, the cursor mode may be selected via two input pins. When used in the parallel scan line input mode, the cursor mode is a mask program option and is fixed at the time of manufacture.

Two graphics modes are provided. In the wide graphics mode, the CRT 9021 produces a graphic entity the size of the character block. The graphic entity contains eight parts, each of which is associated with one bit of the input byte, thereby providing 256 unique graphic symbols. The thin graphics mode enables the user to create thin line drawings and forms.

In both graphics modes, continuous horizontal and vertical lines may be drawn. Additional flexibility is provided by allowing the mask programming of the placement and dimensions of the blocks or lines within a character block. In the thin graphics mode, mask programming allows serrated horizontal or vertical lines.

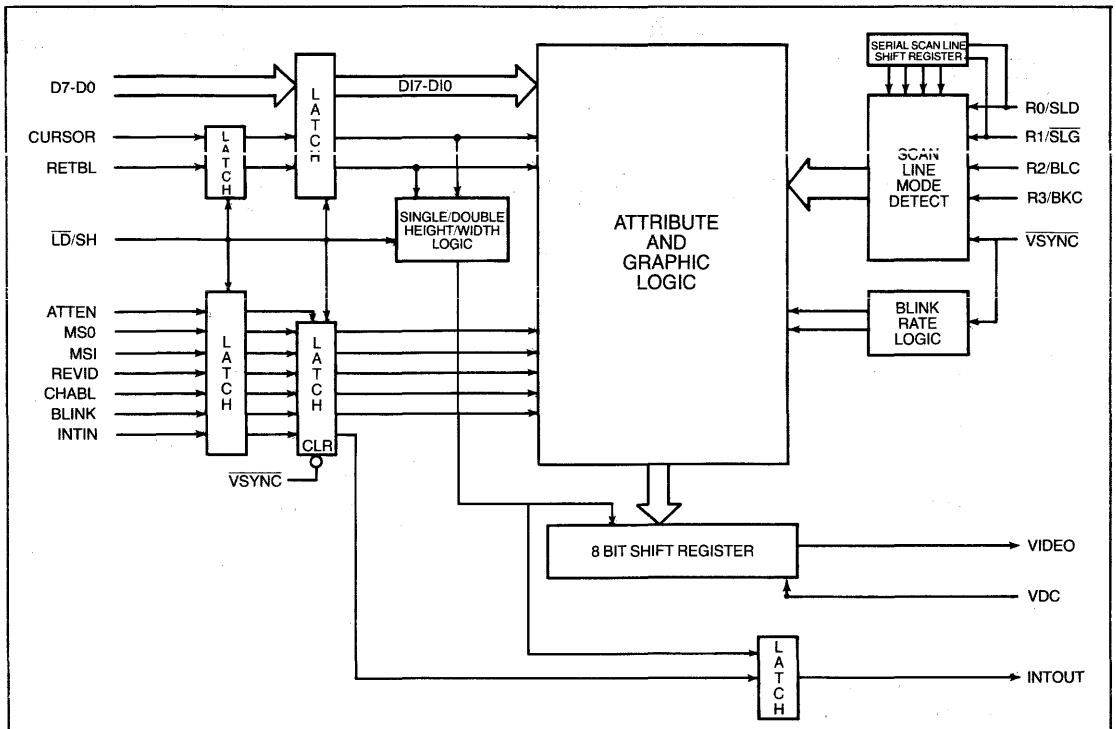


FIGURE 1: CRT 9021 BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1, 28, 27, 26, 25, 24, 23, 22	Data	D7-D0	In the character mode, the data on these inputs is passed through the Attributes logic into the 8 bit high speed video shift register. The binary information on D7 will be the first bit output after the LD/SH input goes low. In the thin or wide graphics mode these 8 inputs will individually control the on/off condition of the particular portion of the character block or line drawing. Figures 2 and 3 illustrate the wide and thin graphics modes respectively and their relationships to D7-D0
2 3	Mode Select 0 Mode Select 1	MS0 MS1	These 2 inputs define the four modes of operation of the CRT 9021 as follows: MS1, MS0 = 00; Wide graphics mode = 10; Thin graphics mode = 01; Character mode without underline = 11; Character mode with underline See section entitled Display Modes for details.
4	Reverse Video	REVID	When this input and Retrace Blank (RETBL) are both low, data from the Attributes and Graphics logic is presented directly to the video shift register. When this input is high and RETBL is low, the Attribute and Graphics logic will invert the data before presenting it to the video shift register.
5	Character blank	CHABL	When this input is high, the parallel inputs to the video shift register are all set low (or high depending on the state of REVID) thus providing a constant video level for the entire length of the character block.
6	Blink	BLINK	When this input is high and both the RETBL and CHABL inputs are low, the character will blink at the programmed character blink rate. Blinking is accomplished by causing the video to go to the background level during the "off" portion of the Character Blink cycle. This video level may be either the white or black level depending on state of REVID. The duty cycle for the character blink is 75/25 (on/off). This input is ignored if it coincides with the CURSOR input and the cursor is formatted to blink.
7	Intensity In	INTIN	The INTIN input along with the INTOUT output provides a user controlled general purpose attribute. Data input to INTIN will appear at INTOUT with the same delay as that from any other attribute input to the serial video output (VIDEO). By using an external mixing circuit, it is possible to raise or lower the voltage level of the video output to produce such attributes as "half intensity" or "intensity".

DESCRIPTION OF PIN FUNCTIONS CONT'D

PIN NO.	NAME	SYMBOL	FUNCTION
8	Supply Voltage	+5V	+5 volt power supply
9	Attribute Enable	ATTEN	When this input is high, the internal attribute latch is updated at the positive going edge of the LD/SH input with data appearing on the REVID, CHABL, MS1, MSØ, BLINK and INTIN inputs. By selectively bringing this input high, the user will update the attribute only at specific character times; all subsequent characters will carry with them the attributes last updated thus allowing "field" or "embedded" attributes. When using a wide video memory where attribute bits are attached to every character, the internal attribute latch may be updated at each character by tieing this input high (thus allowing for "invisible" attributes).
10	Intensity Out	INTOUT	This output is used in conjunction with the INTIN input to provide a three character pipeline delay to allow for general purpose attributes (such as intensity) to be implemented. See INTIN (pin 7).
11	Cursor	CURSOR	When this input is high and RETBL is low, the programmed cursor format will be displayed. When this input is high, and RETBL is high, the CRT 9021 enters the double width mode. See section entitled cursor formats for details.
12	Retrace Blank	RETBL	When this input is high, the parallel inputs to the video shift register are unconditionally cleared to all zeros and loaded on the next LD/SH pulse. This forces the VIDEO output to a low voltage level, independent of all attributes, for blanking the CRT during horizontal and vertical retrace time.
13	Load/Shift	LD/SH	The 8 bit video shift register parallel-in load or serial-out shift operation is established by the state of this input. When high, this input enables the shift register for serial shifting with each video dot clock pulse (VDC input). When low, the video shift register is parallel loaded on the next video dot clock pulse and all data and attributes are moved to the next position in the internal pipeline. In addition, input data and attributes are latched on the positive transition of LD/SH.
14	Video	VIDEO	The Video output provides the serial dot stream to the CRT. Video is shifted out on the rising edge of the video dot clock VDC. The timing of the LD/SH input will determine the number of backfill dots. See figure 5.
15	Video Dot Clock	VDC	This input clock controls the rate at which video is shifted out on the VIDEO output.
16	Scan line 3/Block Cursor	SL3/BKC	This input has two separate functions depending on the way scan line information is presented to the CRT 9021. *Parallel scan line mode*—This input is the most significant bit of the binary scan line row address. *Serial scan line mode*—This input controls the cursor's physical dimensions. If high the cursor will appear as a reverse video block (the entire character cell will be displayed in reverse video). If low, the cursor will appear as an underline on the scan line(s) programmed.
17	Scan line 2/Blink Cursor	SL2/BLC	This input has two separate functions depending on the way scan line information is presented to the CRT 9021. *Parallel scan line mode*—This input is the second most significant bit of the binary scan line row address. *Serial scan line mode*—This input if low, will cause the cursor to alternate between normal and reverse video at the programmed cursor blink rate. The duty cycle for the cursor blink is 50/50 (on/off). If this input is high, the cursor will be non-blinking.
18	Scan Line 1/Scan Line Gate	SL1/SLG	This input has two separate functions depending on the way scan line information is presented to the CRT 9021. *Parallel scan line mode*—This input is the next to the least significant bit of the binary scan line row address. *Serial scan line mode*—This input will be low for 5 or 6 LD/SH pulses to allow the scan line information to be serially shifted into the serial scan line shift register. If this signal is low for 7 or more LD/SH pulses, the CRT 9021 will assume the parallel input scan line row address mode.
19	Scan line 0/Scan Line data	SL0/SLD	This input has two separate functions depending on the way scan line information is presented to the CRT 9021. Refer to figure 6. *Parallel scan line mode*—This input is the least significant bit of the binary scan line row address. *Serial scan line mode*—This input will present the scan line information in serial form (least significant bit first) to the CRT 9021 and permits the proper scan line information to enter the serial scan line shift register during the LD/SH pulses framed by SLG (pin 18).
20	Ground	GND	Ground
21	Vertical Sync	VSYNC	This input is typically connected to the vertical sync output of the CRT controller and is used as the clock input for the two on-chip mask programmable blink rate dividers. The cursor blink rate (50/50 duty cycle) will always be twice the character blank rate (75/25 duty cycle). In addition, the internal attributes are reset when this input is low. The VSYNC input is also used to determine the scan line mode (parallel or serial) used. See the section "Scan Line Input Modes".

ATTRIBUTES FUNCTION

Retrace Blank —The RETBL input causes the VIDEO to go to the zero (black) level regardless of the state of all other inputs.

Reverse Video —The REVID input causes inverted data to be loaded into the video shift register.

Character Blank —The CHABL input forces the video to go to the current background level as defined by Reverse Video.

Underline —MS1, MSØ = 1, 1 forces the video to go to the inverse of the background level for the scan line(s) programmed for underline.

Blink —The BLINK input will cause characters to blink by forcing the video to the background level 25% of the time and allowing the normal video for 75% of the time. When the cursor is programmed to blink (not controlled by the BLINK input), the video alternates from normal to reverse video at 50% duty cycle. The cursor blink rate always overrides the character blink rate when they both appear at the same character position.

Intensity (Half Intensity) —The INTIN input and the INTOUT output allow an intensity (or half intensity) attribute to be carried through the pipeline of the CRT 9021. An external mixer can be used to combine VIDEO and INTOUT to create the desired video level. See figure 8.

Table 1 illustrates the effect of the REVID, CHABL, UNDLN attributes as a function of the cursor format and the CURSOR and RETBL inputs.

TABLE 1: CRT 9021 ATTRIBUTE COMBINATIONS

CURSOR FORMAT	CRT 9021 INPUTS					VIDEO SHIFT REGISTER LOADED WITH:	
	RETBL	CURSOR	REVID	CHABL	UNDLN		
X	1	X	X	X	X	all zero's	
	0	0	0	0	0	data	
	0	0	0	0	1	One's for selected scan line(s); Data for all other scan lines.	
	0	0	0	1	X	All zero's	
	0	0	1	0	0	$\overline{\text{data}}$	
	0	0	1	0	1	Zero's for selected scan line(s); $\overline{\text{data}}$ for all other scan lines.	
	0	0	1	1	X	One's for all scan lines.	
UNDERLINE[2]	0	1	0	0	X[1]	One's for selected scan line(s) for cursor; data for all other scan lines.	
	0	1	0	1	X[1]	One's for selected scan line(s) for cursor; zero's for all other scan lines.	
	0	1	1	0	X[1]	Zero's for selected scan line(s) for cursor; Data for all other scan lines.	
	0	1	1	1	X[1]	Zero's for selected scan line(s) for cursor; one's for all other scan lines.	
BLINKING[3] UNDERLINE[2]	0	1	0	0	X[1]	One's for selected scan line(s) blinking; Data for all other scan lines.	
	0	1	0	1	X[1]	One's for selected scan line(s) blinking; zero's for all other scan lines.	
	0	1	1	0	X[1]	Zero's for selected scan line(s) blinking; Data for all other scan lines.	
	0	1	1	1	X[1]	Zero's for selected scan line(s) blinking; one's for all other scan lines.	
REVID BLOCK	0	1	0	0	0	$\overline{\text{Data}}$ for all scan lines.	
	0	1	0	0	1	Zero's for selected scan line(s) for underline; data for all other scan lines.	
	0	1	0	1	X	One's for all scan lines.	
	0	1	1	0	0	Data for all scan lines	
	0	1	1	0	1	One's for selected scan line(s) for underline; data for all other scan lines.	
	0	1	1	1	X	Zero's for all scan lines.	
BLINKING[3] REVID BLOCK	0	1	0	0	0	On Data for all scan lines.	Off Data for all scan lines.
	0	1	0	0	1	Zero's for selected scan line(s) for underline; Data for all other scan lines.	One's for selected scan line(s) for underline; Data for all other scan lines.
	0	1	0	1	X	One's for all scan lines.	Zero's for all scan lines.
	0	1	1	0	0	Data for all scan lines.	$\overline{\text{Data}}$ for all scan lines.
	0	1	1	0	1	One's for selected scan line(s); Data for all other scan lines.	Zero's for selected scan line(s); Data for all other scan lines.
	0	1	1	1	X	Zero's for all scan lines.	One's for all scan lines.

1 - if the programmed scan line(s) for cursor and underline coincide, the cursor takes precedence; otherwise both are displayed.
2 - at programmed scan line(s) for underline
3 - at cursor blink rate
Note—cursor blink rate overrides character blink rate.

DISPLAY MODES

Inputs MS1 and MSØ select one of four display modes. All attributes except underline operate independent of the display mode used. Figures 8a and 8b illustrate a typical CRT 9021 configuration which operates in all display modes for both the parallel and serial scan line modes respectively.

MS1, MS0 = 00 —Wide Graphics Mode.
In this display mode, inputs D7-D0 define a graphics entity as illustrated in figure 2. Note that individual bits in D7-D0 will illuminate particular portions of the character block. Table 2 shows all programming ranges possible when defining the wide graphic boundaries. No underline is possible in this display mode.

MS1, MS0 = 10 —Thin Graphics Mode.
In this display mode, inputs D7-D0 define a graphic entity as illustrated in figure 3. Note that individual bits in D7-D0 will illuminate particular horizontal or vertical line segments within the character block. Table 3 shows all programming ranges possible when defining the thin graphics boundaries. No underline is possible in this display mode.

MS1, MS0 = 01 —Character Mode Without Underline.
In this display mode, inputs D7-D0 go directly from the input latch to the video shift register via the Attributes and Graphics logic. This mode requires either a bit mapped system RAM (1 bit in RAM equals 1 pixal on the CRT) or an external character generator as shown in figures 8a and 8b.

MS1, MS0 = 11 —Character Mode With Underline.
Same operation as MS1, MSØ = 01 with the underline attribute appearing on the scan line(s) mask programmed.

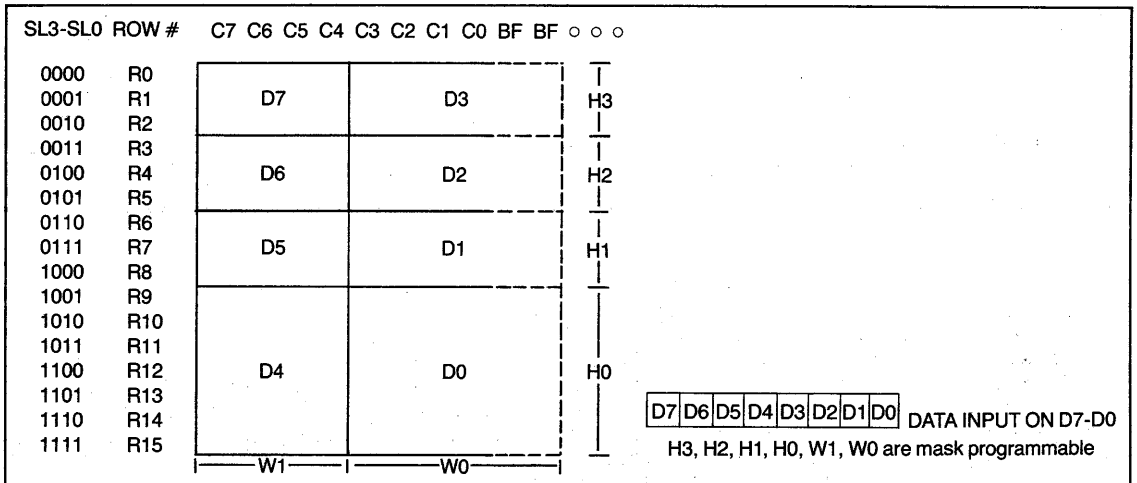


FIGURE 2: WIDE GRAPHICS MODE FOR STANDARD CRT 9021

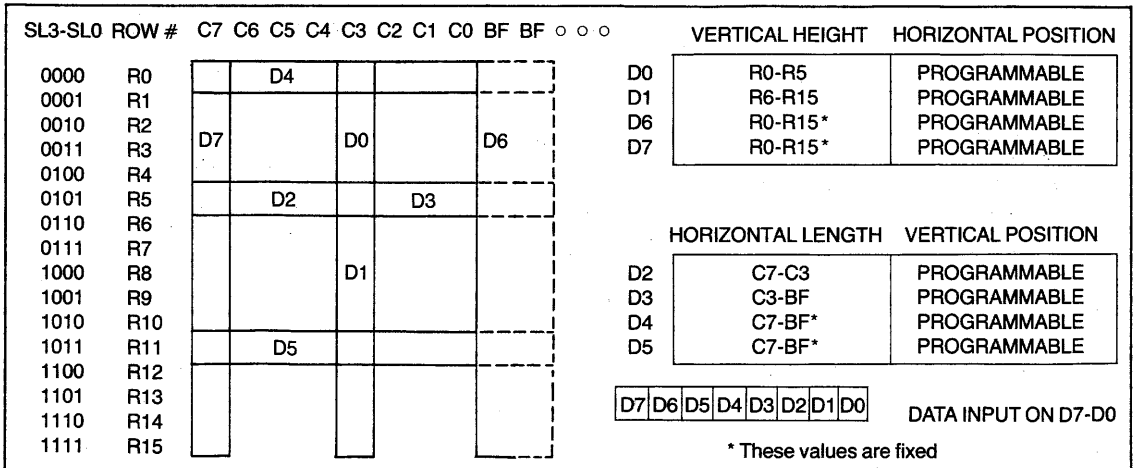


FIGURE 3: THIN GRAPHICS MODE FOR STANDARD CRT 9021

BACKFILL

Backfill is a mechanism that allows a character width of greater than 8 dots and provides dot information (usually blanks) for all dot positions beyond 8. The character width is defined by the period of the $\overline{LD}$/SH input. For the character modes, backfill is added to the tail end of the character by two methods which are mask programmable.

Method A — The backfill (BF) dots will be the same as the dot displayed in position C7.

Method B — The backfill (BF) dots will be the same as the dot displayed in position C0.

For the wide graphics mode, the backfill dots will always be the same as the dot displayed in position C0 (method B) with no programmable option.

CURSOR FORMATS

Four cursor formats are possible with the CRT 9021. If the parallel scan line input mode is used, one of four cursor formats may be selected as a mask programmed option. If the serial scan line input mode is used, the cursor format is selected via input pins 16 and 17 (SL3/BKC, SL2/BLC). See Table 5. The four cursor modes are as follows:

Underline — The cursor will appear as an underline. The position and width of the cursor underline is mask programmed.

Blinking Underline — The cursor will appear as an underline. The underline will alternate between normal and reverse video at the mask programmed cursor blink rate.

Reverse Video Block — The cursor will appear as a reverse video block (The entire character cell will be displayed in reverse video).

Blinking Reverse Video Block — The cursor will appear as a reverse video block and the entire block (character plus background) will alternate between normal and reverse video at the masked programmed cursor blink rate.

Scan Line Input Mode	Pin 17	Pin 16	Cursor Function
Serial	1	0	Underline
	1	1	Reverse Video Block
	0	0	Blinking Underline
	0	1	Blinking Reverse Video Block
Parallel	X	X	Mask programmable Only

TABLE 5: CURSOR FORMATS

DOUBLE WIDTH MODE

In order to display double width characters, video must be shifted out at half frequency and the video shift register must receive new information (parallel load) every other $\overline{LD}$/SH input pulse. In order to divide the video dot clock (VDC) and the $\overline{LD}$/SH pulse internally at the proper time, the cursor input should be pulsed during RETBL prior to the scan line to be displayed as double width. The CURSOR input must remain low for a minimum of 1 $\overline{LD}$/SH period from the leading edge of RETBL. The CURSOR input can stay high for the entire RETBL time but should not extend into active video. If it does, a cursor will be displayed. It is assumed that the CRT controller knows when a particular scan line should be double width and it should activate the CURSOR in the manner just described. Double height/double width characters can also be displayed if the scan line count is incremented by the CRT controller every other scan line. With respect to the CRT 9021, no distinction between double width and double height display is necessary. Figure 4 illustrated timing for both single and double width modes. The CRT 9007, which supports double height double width characters, will produce the CURSOR signal as required by the CRT 9021 with no additional hardware.

SCAN LINE INPUT MODES

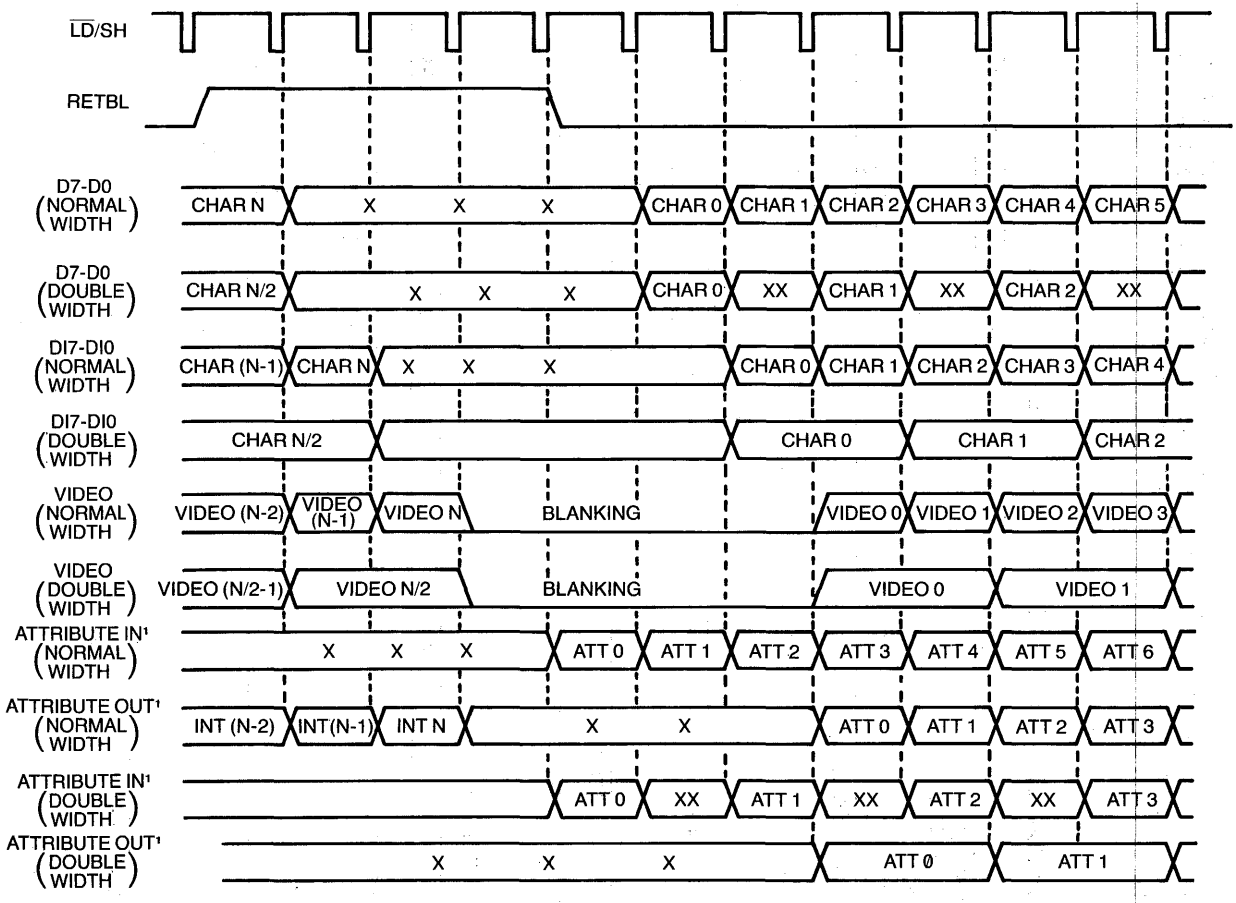
Scan line information can be introduced into the CRT 9021 in parallel format or serial format. Table 6 illustrates the pin definition as a function of the scan line input mode. The CRT 9021 will automatically recognize the proper scan line mode by observing the activity on pin 18. In parallel mode, this input will be stable for at least 1 scan line and in serial mode this input will remain low for about 5 or 6 $\overline{LD}$/SH periods. If pin 18 goes active low for less than seven but more than two continuous $\overline{LD}$/SH periods during the last scan line that has an active low on the $\overline{VSYNC}$ input, the serial mode will be locked in for the next field. The parallel scan line input mode will be selected for the next field if the following two conditions occur during $\overline{VSYNC}$ low time. First, at least one positive transition must occur on pin 18 and second, pin 18 must be low for seven or more $\overline{LD}$/SH periods. Refer to figure 7 for timing details.

Scan Line Input Mode	CRT 9021 Pin Number			
	19	18	17	16
Serial	SLD	$\overline{SLG}$	BLC	BKC
Parallel	SL0	SL1	SL2	SL3

TABLE 6: PIN DEFINITION FOR PARALLEL AND SERIAL SCAN LINE MODES

PROGRAM OPTIONS

The CRT 9021 has a variety of mask programmed options. Tables 2 and 3 illustrate the range of these options for the wide and thin graphics modes respectively. Table 4 illustrates the range of the miscellaneous mask programmed options. In addition, Tables 2, 3 and 4 show the mask programmed options for the standard CRT 9021.



1-Attributes include MS0 , MSI, BLINK, CHABL, INTENSITY, REVID

FIGURE 4: CRT 9021 FUNCTIONAL I/O TIMING

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... .15V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to 70°C, $V_{CC} = +5V \pm 5\%$, unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low Level V_{IL}			0.8	V	
High Level V_{IH1}	2.0			V	All inputs except VDC, $\overline{LD}$/SH
High Level V_{IH2}	4.3			V	For VDC, $\overline{LD}$/SH input
OUTPUT VOLTAGE LEVELS					
Low Level V_{OL}			0.4	V	$I_{OL} = 0.4$ mA
High Level V_{OH}	2.4			V	$I_{OH} = 100\mu A$
INPUT LEAKAGE CURRENT					
Leakage I_{L1}			10	μA	$0 \leq V_{IN} < V_{CC}$; excluding VDC, $\overline{LD}$/SH
Leakage I_{L2}			50	μA	$0 \leq V_{IN} \leq V_{CC}$; for VDC $\overline{LD}$/SH
INPUT CAPACITANCE					
C_{IN1}		10		pf	Excluding VDC, $\overline{LD}$/SH
C_{IN2}		20		pf	For $\overline{LD}$/SH
C_{IN3}		25		pf	For VDC
POWER SUPPLY CURRENT					
I_{CC}		50		mA	

AC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VDC[1]					
$1/t_{CY1}$ VDC frequency	1.0		30.0	MHZ	CRT 9021A; see note 1
	1.0		28.5	MHZ	CRT 9021B
1_{CKL} VDC low	10				
t_{CKH} VDC high	10			ns	
t_{CKR} VDC rise time	10		10	ns	Measured from 10% to 90% points
t_{CKF} VDC fall time			10	ns	Measured from 90% to 10% points
$\overline{LD}$/SH					
t_{CY2}	290			ns	CRT 9021A; see note 1
	315			ns	CRT 9021B
t_{S1}	7			ns	
t_{H1}	0			ns	
INPUT SETUP AND HOLD					
t_{S2}	35			ns	
t_{H2}	0			ns	
MISCELLANEOUS TIMING					
t_{PD}			35	ns	C_L = 15 pf
t_{DW}	t_{CY2}				

1-These parameters are Preliminary.

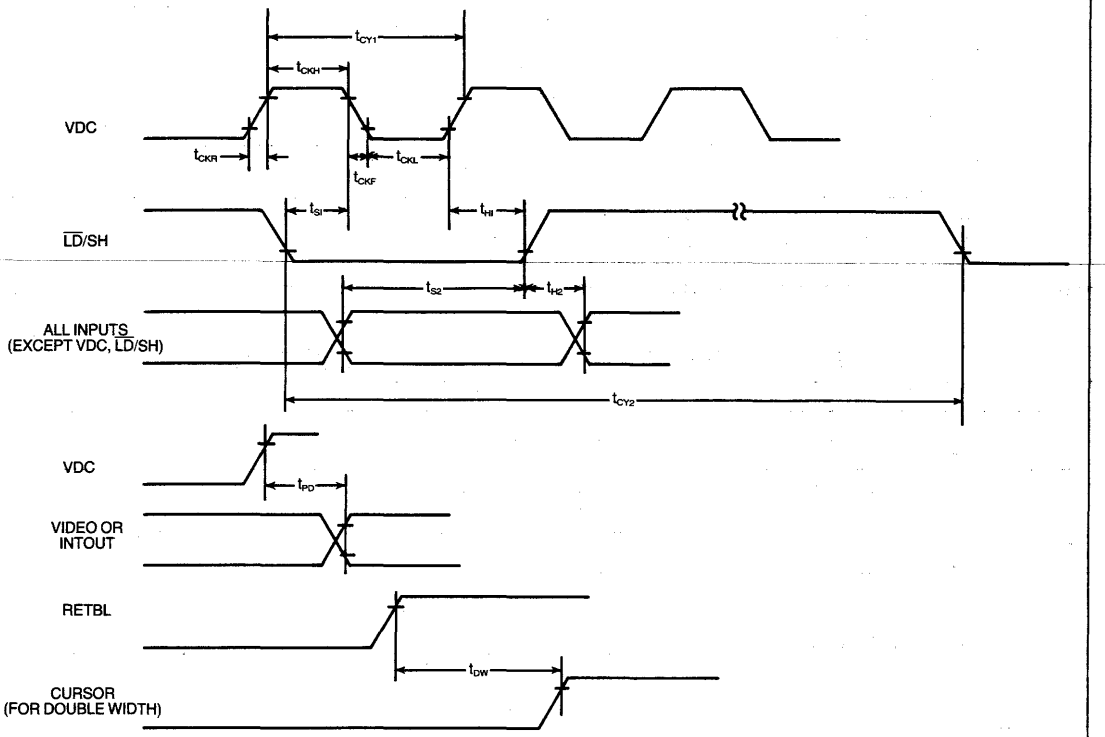


FIGURE 5: CRT 9021 INPUT/OUTPUT TIMING

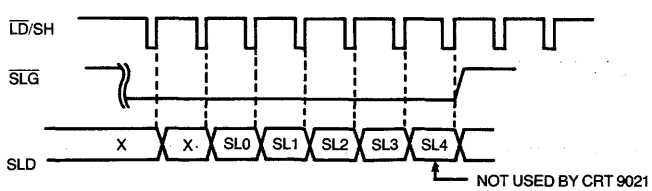


FIGURE 6: SERIAL SCAN LINE MODE TIMING

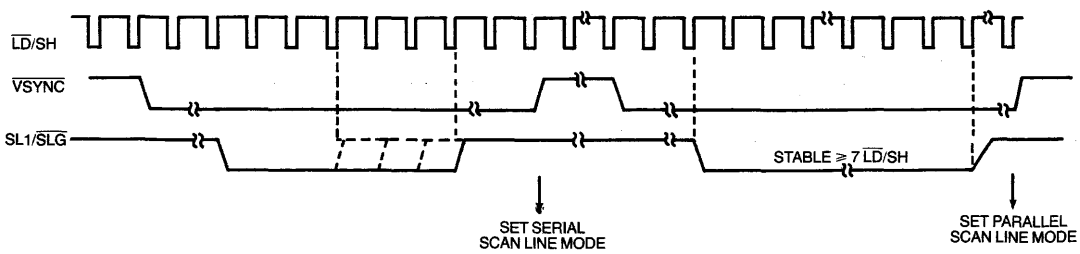


FIGURE 7: SERIAL/PARALLEL SCAN LINE MODE SELECTION TIMING

TABLE 2
WIDE GRAPHICS MASK PROGRAMMING OPTIONS

OPTION	CHOICES	STANDARD CRT 9021
Height of graphic block*		
D7 and D3	any scan line(s)	R0, R1, R2
D6 and D2	any scan line(s)	R3, R4, R5
D5 and D1	any scan line(s)	R6, R7, R8
D4 and D0	any scan line(s)	R9, R10, R11, R12, R13, R14, R15
Width of D7, D6, D5, D4**	any number of dots 0 to 8	C7, C6, C5, C4
Width of D3, D2, D1, D0**	any number of dots 0 to 8	C3, C2, C1, C0, BF

* Any graphic block pair can be removed by programming for zero scan lines.

** Total number of dots for both must be equal to the total dots per character with no overlap.

TABLE 3
THIN GRAPHICS MASK PROGRAMMING OPTIONS

OPTION	CHOICES	STANDARD CRT 9021
Backfill	C1 or C0	C0
Horizontal position for		
D2 and D3	any scan line(s) R0-R15	R5
D4	any scan line(s) R0-R15	R0
D5	any scan line(s) R0-R15	R11
Horizontal length for		
D2[2]	any continuous dots C7-C0, BF	C7-C3
D3[2]	all dots not covered by D2	C3-BF
Blanked dots for serrated horizontal lines		
D2	any dot(s) C7-C0, BF	none
D3	any dot(s) C7-C0, BF	none
D4 and D5	any dot(s) C7-C0, BF	none
Vertical position for		
D0 and D1	any dot(s) C7-C0, BF	C3
D6[1]	any dot(s) C6-C0, BF	BF
D7[1]	any dot(s) C7-C0	C7
Vertical length for		
D0	any scan line(s)	R0 to R5
D1	all scan lines not used by D0	R6 to R15
D6	no choice; always R0-R15	R0 to R15
D7	no choice; always R0-R15	R0 to R15

1-D7 must always come before D6 with no overlap; otherwise D6 is lost.
2-D2 and D3 must always overlap by one and only one dot.

TABLE 4
MISCELLANEOUS MASK PROGRAMMING OPTIONS

OPTION	CHOICES	STANDARD CRT 9021
Backfill in character mode	C7 or C0	C7
Character blink rate (division of $\overline{\text{VSYNC}}$ frequency)	8 to 60; divisible by 4 (7.5 Hz to 1 Hz)[1]	32 (1.875 Hz)[1]
Cursor blink rate[2]	Twice the character blink rate	16 (3.75 Hz)[1]
character underline position	any scan line(s) R0-R15	R11
cursor underline[3]	any scan line(s) R0-R15	not applicable
cursor format[4]	underline Blinking underline Reverse video block Blinking reverse video block	Blinking reverse video block

1 - Assumes $\overline{\text{VSYNC}}$ input frequency of 60 Hz.
2 - Valid only if the cursor is formatted to blink.
3 - Valid only if the cursor is formatted for underline.
4 - Valid for the parallel scan line mode only.

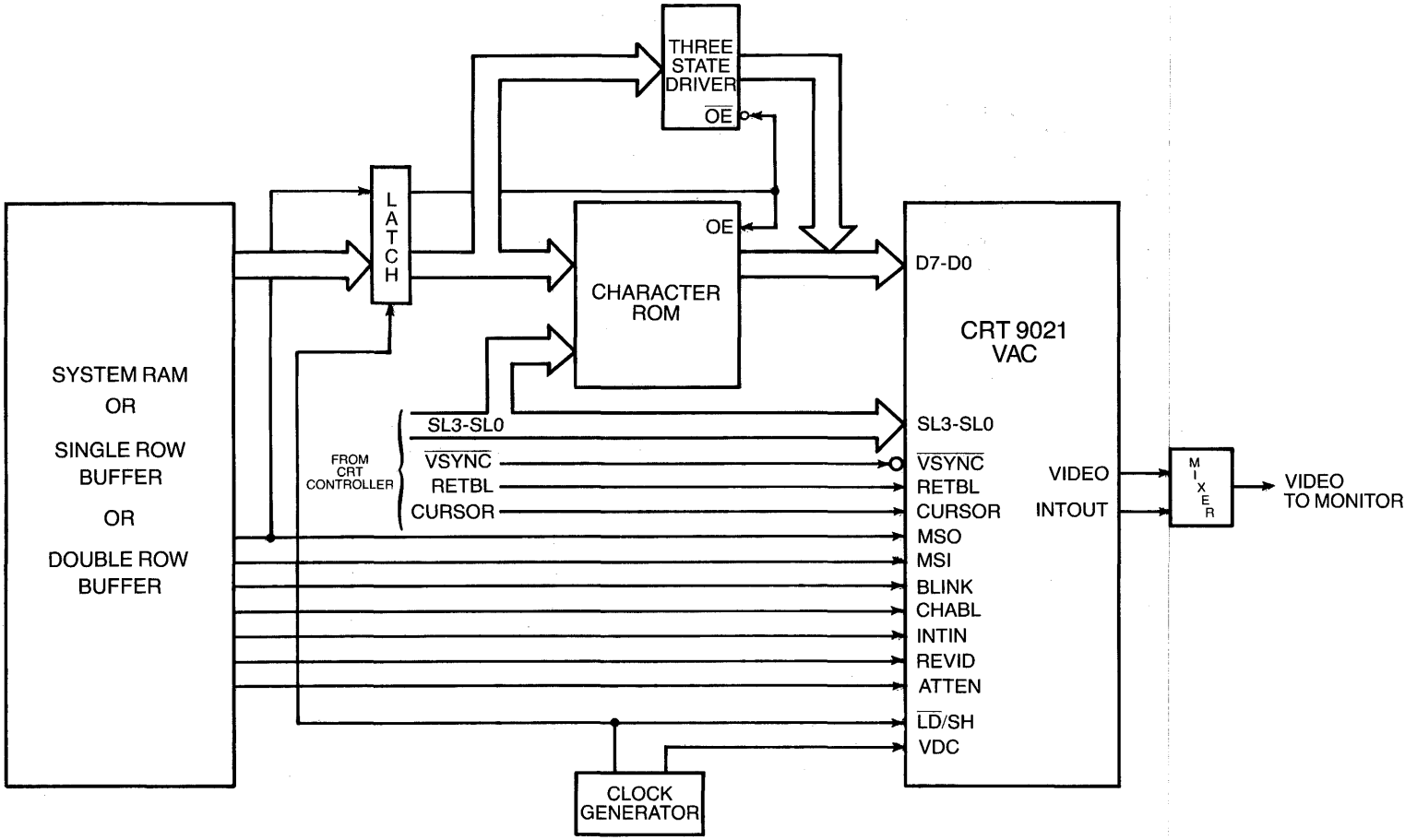


FIGURE 8a: CRT 9021 SYSTEM CONFIGURATION IN PARALLEL SCAN LINE MODE

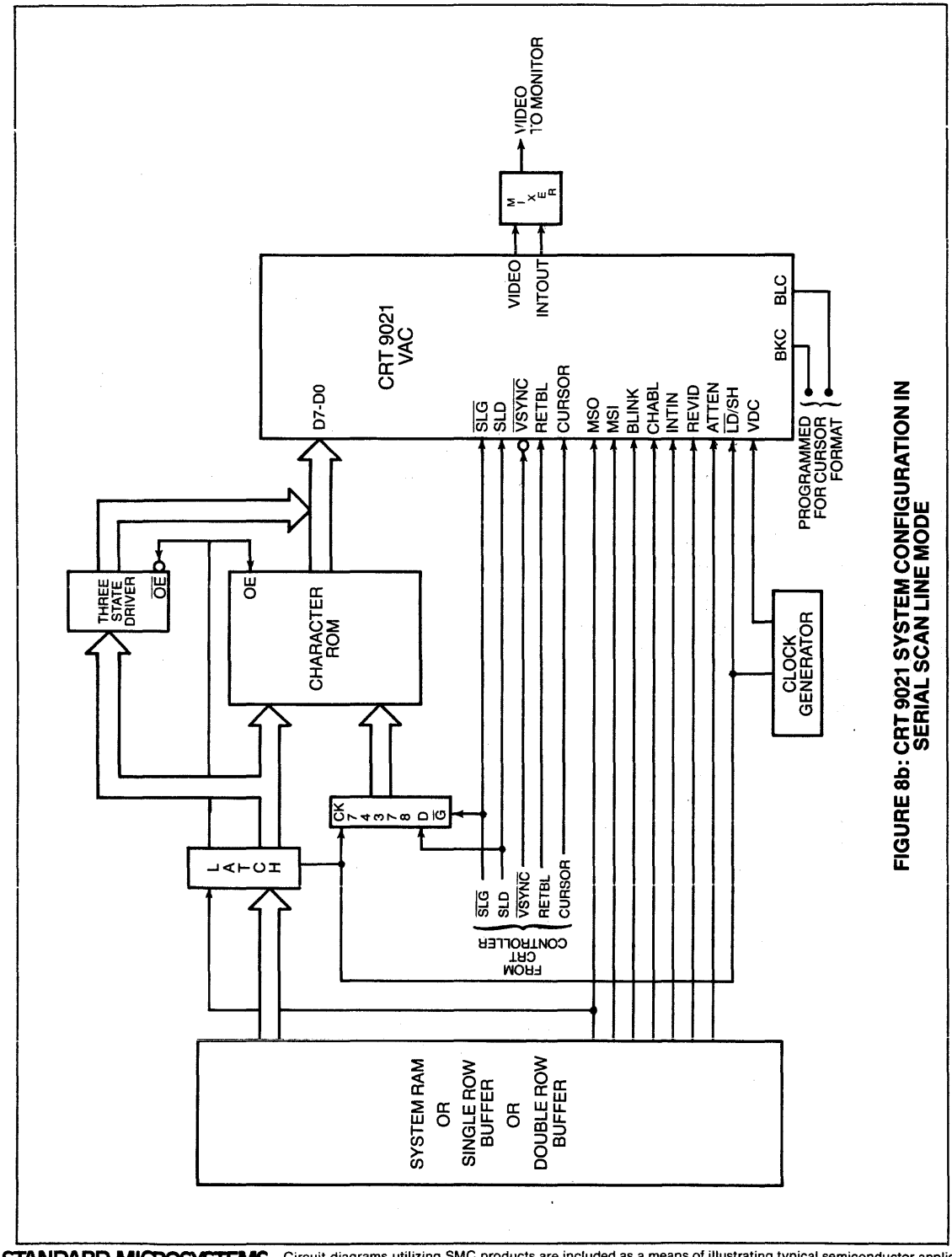


FIGURE 8b: CRT 9021 SYSTEM CONFIGURATION IN SERIAL SCAN LINE MODE

Microprocessor Peripheral

ROM

Part Number	Description	Access Time	Power Supply	Package	Page
ROM 4732 (1)	32K ROM; 32,768 bits organized 4096x8	450 nsec	+5	24 DIP	405-408
ROM 36000 (1)(2)	64K ROM; 65,536 bits organized 8192x8	250 nsec	+5	24 DIP	409-412

FLOPPY DISK/HARD DISK

Part Number	Description	Sector/ Format	Density	Data Bus	Side Select Output	Power Supplies	Package	Page
FDC765	Floppy Disk Controller/ Formatter	Soft	Double	True	Yes	+5	40 DIP	341-342
FDC1761	Floppy Disk Controller/ Formatter (mini-floppy only)	Soft	Double	Inverted	No	+5, +12	40 DIP	343-358
FDC1763	Floppy Disk Controller/ Formatter (mini-floppy only)	Soft	Double	True	No	+5, +12	40 DIP	343-358
FDC1765	Floppy Disk Controller/ Formatter (mini-floppy only)	Soft	Double	Inverted	Yes	+5, +12	40 DIP	343-358
FDC1767	Floppy Disk Controller/ Formatter (mini-floppy only)	Soft	Double	True	Yes	+5, +12	40 DIP	343-358
FDC1791	Floppy Disk Controller/ Formatter	Soft	Double	Inverted	No	+5, +12	40 DIP	359-374
FDC1792	Floppy Disk Controller/ Formatter	Soft	Single	Inverted	No	+5, +12	40 DIP	359-374
FDC1793	Floppy Disk Controller/ Formatter	Soft	Double	True	No	+5, +12	40 DIP	359-374
FDC1794	Floppy Disk Controller/ Formatter	Soft	Single	True	No	+5, +12	40 DIP	359-374
FDC1795	Floppy Disk Controller/ Formatter	Soft	Double	Inverted	Yes	+5, +12	40 DIP	359-374
FDC1797	Floppy Disk Controller/ Formatter	Soft	Double	True	Yes	+5, +12	40 DIP	359-374
FDC3400	Floppy Disk Data Handler	Hard	NA	True	NA	+5, −12	40 DIP	389-396
FDC9216/B	Floppy Disk Data Separator	Soft/Hard	Double	NA	NA	+5	8 DIP	375-378
FDC9229/B	Floppy Disk Data Separator, Head Load Timer, write precompensation generator	Soft/Hard	Double	NA	NA	+5	20 DIP	379-386
HDC7261	Hard Disk Controller	Soft/Hard	Double	True	Yes	+5	40 DIP	387-388

CASSETTE/CARTRIDGE

Part Number	Description	Max Data Rate	Features	Power Supply	Package	Page
CDC 3600	Cassette/Cartridge Data Handler	250K bps	Sync byte detection, Read While Write	+5, −12	40 DIP	397-404

(1) May be custom mask programmed

(2) For future release

STANDARD MICROSYSTEMS CORPORATION

FDC 765A

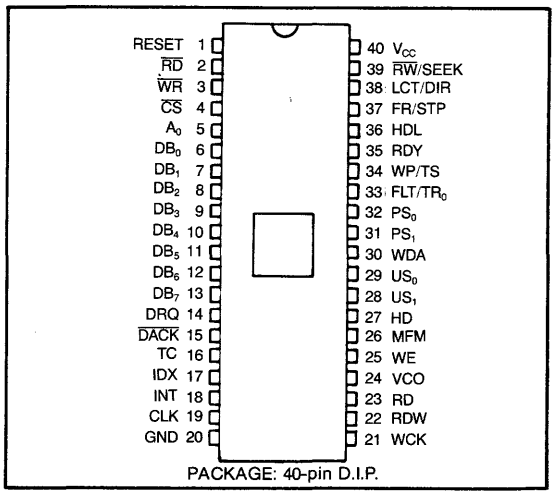
PRELIMINARY

Single/Double Density Floppy Disk Controller

FEATURES

- ☐ IBM Compatible in both Single and Double Density Recording Formats
- ☐ Programmable Data Record Lengths: 128, 256, 512, or 1024 Bytes/Sector
- ☐ Multi-Sector and Multi-Track Transfer Capability
- ☐ Drive Up to 4 Floppy Disks
- ☐ Data Scan Capability—will scan a Single Sector or an entire cylinder's worth of data fields, comparing on a Byte by Byte Basis, data in the Processor's Memory with data read from the Diskette
- ☐ Data Transfers in DMA or Non-DMA Mode
- ☐ Parallel Seek Operations on up to four drives
- ☐ Compatible with Most Microprocessors
- ☐ Single Phase 8 MHz Clock
- ☐ Single +5 Volt Power Supply
- ☐ COPLAMOS® n-Channel Silicon Gate Technology
- ☐ Available in 40-Pin Dual-in-Line Package

PIN CONFIGURATION



PACKAGE: 40-pin D.I.P.

SECTION V

GENERAL DESCRIPTION

The FDC765 is an LSI Floppy Disk Controller (FDC) Chip, which contains the circuitry and control functions for interfacing a processor to 4 Floppy Disk Drives. It is capable of supporting either IBM 3740 single density format (FM), or IBM System 34 Double Density format (MFM) including double sided recording. The FDC765 provides control signals which simplify the design of an external phase locked loop, and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a Floppy Disk Interface.

Hand-shaking signals are provided in the FDC765 which make DMA operation easy to incorporate with the aid of an external DMA Controller chip. The FDC will operate in either DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor every time a data byte is available. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the FDC765 and DMA controller.

There are 15 separate commands which the FDC765 will execute. Each of these commands require multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

Read Data	Write Data
Read ID	Format a Track
Read Deleted Data	Write Deleted Data
Read a Track	Seek
Scan Equal	Recalibrate (Restore to Track 0)
Scan High or Equal	Sense Interrupt Status
Scan Low or Equal	Sense Drive Status
Specify	

Address mark detection circuitry is internal to the FDC which simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time may be programmed by the user. The FDC765 offers many additional features such as multiple sector transfers in both read and write with a single command, and full IBM compatibility in both single and double density modes.

STANDARD MICROSYSTEMS CORPORATION

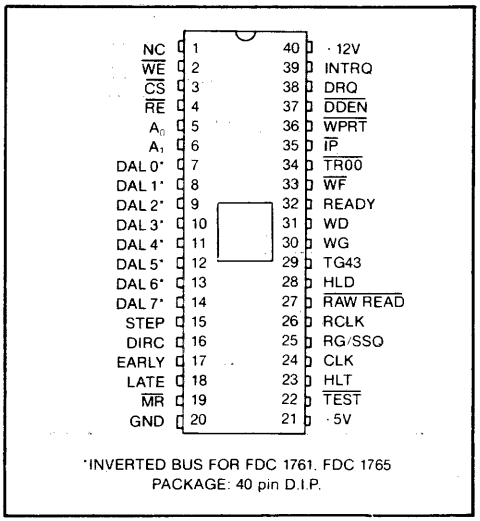
FDC 1761-02
FDC 1763-02
FDC 1765-02
FDC 1767-02
μPC FAMILY

Floppy Disk Controller/Formatter FDC

FEATURES

- ☐ 1 MHZ VERSION OF FDC 179X
- ☐ SOFT SECTOR FORMAT COMPATIBILITY
- ☐ AUTOMATIC TRACK SEEK WITH VERIFICATION
- ☐ ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
- ☐ READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128 Byte or Variable Length Record
- ☐ WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Initialization
- ☐ PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- ☐ SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-chip Track and Sector Registers/Comprehensive Status Information
- ☐ WRITE PRECOMPENSATION (MFM AND FM)
- ☐ SIDE SELECT LOGIC (FDC 1765, FDC 1767)
- ☐ WINDOW EXTENSION (IN MFM)

PIN CONFIGURATION



*INVERTED BUS FOR FDC 1761, FDC 1765
PACKAGE: 40 pin D.I.P.

- ☐ INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- ☐ COMPATIBLE WITH FD176X-02
- ☐ COPLAMOS® n-CHANNEL MOS TECHNOLOGY
- ☐ COMPATIBLE WITH THE FDC 9216 FLOPPY DISK DATA SEPARATOR

GENERAL DESCRIPTION

The FDC 176X is an MOS/LSI device which performs the functions of a Floppy Disk Controller/Formatter in a single chip implementation. The basic FDC 176X chip design has evolved into four specific parts: FDC 1761, FDC 1763, FDC 1765, and the FDC 1767. It is a 1MHz version of the FDC 179X family.

This FDC family performs all the functions necessary to read or write data to a floppy disk drive. 5¼" (mini-floppy) drives with single or double density storage capabilities are supported. These n-channel MOS/LSI devices will replace a large amount of discrete logic required for interfacing a host processor to a floppy disk.

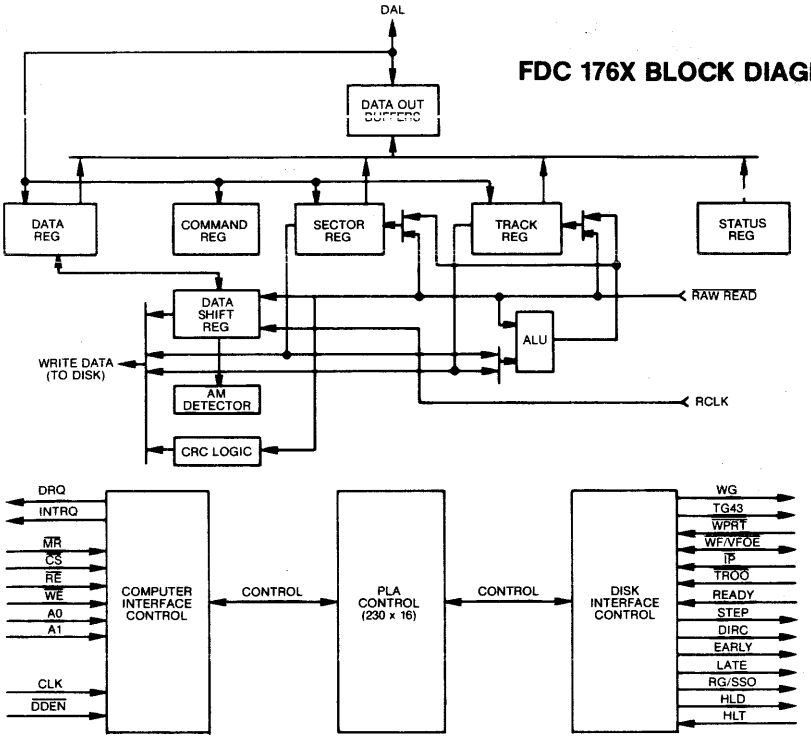
The FDC 176X is IBM 3740 compatible in single density mode (FM) and System 34 compatible in double density mode (MFM). The FDC 176X contains enhanced features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation.

The FDC 1763 is identical to the FDC 1761 except the DAL lines are TRUE for systems that utilize true data busses.

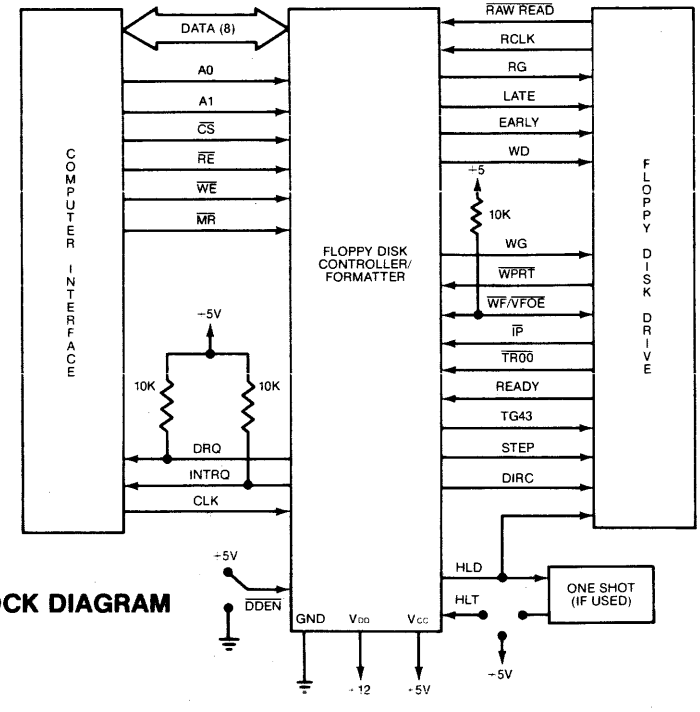
The FDC 1765 adds side select logic to the FDC 1761. The FDC 1767 adds the side select logic to the FDC 1763.

The processor interface consists of an 8 bit bidirectional bus for data, status, and control word transfers. This family of controllers is configured to operate on a multiplexed bus with other bus-oriented devices.

FDC 176X BLOCK DIAGRAM



SYSTEM BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	NO CONNECTION	NC	This pin is internally connected to the substrate bias generator and must be left open.
20	GROUND	V_{SS}	Ground
21	POWER SUPPLY	V_{CC}	+5V ±5%
40	POWER SUPPLY	V_{DD}	+12V ±5%
19	MASTER RESET	$\overline{MR}$	A logic low (50 microseconds min.) on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a Restore Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into the sector register.
COMPUTER INTERFACE:			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and the parallel data bus (DAL).
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on DALØ-DAL7 when $\overline{CS}$ is low.
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control:
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit Bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by $\overline{WE}$ or a transmitter enabled by $\overline{RE}$. The Data Bus is inverted on the FDC 1761, and FDC 1765. Each line will drive 1 standard TTL load.
24	CLOCK	CLK	This input requires a free-running square wave clock for internal timing reference of 1 MHz ±1% with a 50% duty cycle.
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use a 10K pull-up resistor to +5V.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register or the status register is read. Use a 10K pull-up resistor to +5V.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	Step and direction motor control. The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the write data pulse occurring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.
22	TEST	$\overline{TEST}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated motors.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged.

$\overline{CS}$	A1	A0	$\overline{RE}$	$\overline{WE}$
0	0	0	Status Reg	Command Reg
0	0	1	Track Reg	Track Reg
0	1	0	Sector Reg	Sector Reg
0	1	1	Data Reg	Data Reg

	NAME	SYMBOL	FUNCTION
25	READ GATE (1761/3)	RG	This output is used for synchronization of external data separators. The output goes high after two bytes of zeroes in single density, or four bytes of either zeroes or ones in double density operation.
25	SIDE SELECT OUTPUT (1765, 1767)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When S = 1, SSO is set to a logic 1. When S = 0, SSO is set to a logic 0. The SSO is compared with the side information in the sector I.D. field. If they do not compare, status bit 4 (RNF) is set. The side select output is only updated at the beginning of a type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signals directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	A 400 ns (MFM) or 1000 ns (FM) pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$/ $\overline{\text{VFO ENABLE}}$	$\overline{\text{WF/VFOE}}$	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG=1, Pin 33 functions as a $\overline{\text{WF}}$ input. If $\overline{\text{WF}}$=0, any write command will immediately be terminated. When WG=0, Pin 33 functions as a $\overline{\text{VFOE}}$ output. $\overline{\text{VFOE}}$ will go low during a read operation after the head has loaded and settled (HLT=1). On the 1765/7, it will remain low until the last bit of the second CRC byte in the ID field. $\overline{\text{VFOE}}$ will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1761/3, $\overline{\text{VFOE}}$ will remain low until the end of the Data Field.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FDC176X that the Read/Write head is positioned over Track 00.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	This input informs the FDC176X when the index hole is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	$\overline{\text{DOUBLE DENSITY}}$	$\overline{\text{DDEN}}$	This pin selects either single or double density operation. When $\overline{\text{DDEN}}$=0, double density is selected. When $\overline{\text{DDEN}}$=1, single density is selected.

FUNCTIONAL DESCRIPTION

The FDC 176X-02 major functional blocks are as follows:

Data Shift Register—This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register—This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Sector Register (SR)—This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR)—This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a Force Interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR)—This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic—This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x)=x^{16}+x^{12}+x^5+1$.

Track Register—This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU)—The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control—All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

AM Detector—The address mark detector detects ID, data and index address marks during ready and write operations.

OPERATION

The FDC 176X has two modes of operation, according to the state of $\overline{\text{DDEN}}$. When $\overline{\text{DDEN}}=0$, double density (MFM) is assumed. When $\overline{\text{DDEN}}=1$, single density (FM) is assumed. In either case the CLK input (Pin 24) is at 1MHz and stepping rates of 6, 12, 20 and 30ms can be obtained.

Disk Read Operation

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{\text{DDEN}}$ should be placed to logical "1." For MFM formats, $\overline{\text{DDEN}}$ should be placed to a logical "0." Sector lengths are determined at format time by a special byte in the "ID" field. If this Sector length byte in the ID field is zero, then the sector length is 128 bytes. If 01, then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes. For the FDC 1765/67 the sector length may be different according to the state of the b flag in the command word. Refer to Table 1; command summary. The number of sectors per track can be from 1 to 255 sectors. The number of tracks is from 0 to 255 tracks.

For read operations, the FDC 176X requires $\overline{\text{RAW READ}}$ Data (Pin 27) signal which is a 400 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not, it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) on 1761/63 which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FDC 176X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FDC 176X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FDC 176X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG=0), the $\overline{\text{VFOE}}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{\text{VFOE}}$ will go active when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 176X is inspecting data off the disk

If $\overline{\text{WF/VFOE}}$ is not used, this pin may be left open, as it has an internal pull up resistor.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit

is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

Disk Write Operation

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution against erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FDC 176X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The $\overline{\text{Write Fault}}$ input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FDC 176X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FDC176X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 1000 ns pulses in FM ($\overline{\text{DDEN}}$=1) and 400 ns pulses in MFM ($\overline{\text{DDEN}}$=0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FDC 176X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

COMMAND WORDS

The FDC 176X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

Table 1. Command Summary

		BITS							
COMMAND	TYPE	7	6	5	4	3	2	1	0
Restore	I	0	0	0	0	h	V	r_1	r_0
Seek	I	0	0	0	1	h	V	r_1	r_0
Step	I	0	0	1	u	h	V	r_1	r_0
Step In	I	0	1	0	u	h	V	r_1	r_0
Step Out	I	0	1	1	u	h	V	r_1	r_0
Read Sector	II	1	0	0	m	F_2	E	F_1	0
Write Sector	II	1	0	1	m	F_2	E	F_1	a_0
Read Address	III	1	1	0	0	0	E	F_1	0
Read Track	III	1	1	1	0	0	E	F_1	0
Write Track	III	1	1	1	1	0	E	F_1	0
Force Interrupt	IV	1	1	0	1	I_3	I_2	I_1	I_0

Type I Commands

The Type I Commands are Restore, Seek, Step, Step-In, and Step-Out. Each of the Type I Commands contains a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 2.

The Type I Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h=1, the head is loaded at the beginning of the command (HLD output is made active). If h=0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FDC 176X receives a command that specifically disengages the head. If the FDC 176X is idle (busy=0) for 15 revolutions of the disk, the head will be automatically disengaged (HLD made inactive).

The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V=1, a verification is performed, if V=0, no verification is performed.

During verification, the head is loaded and after an internal 30 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt

is generated, and Seek Error Status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after five revolutions of the disk, the FDC 176X terminates the operation and sends an interrupt (INTRQ).

The Step, Step-In, and Step-Out commands contain an Update flag (u). When u=1, the track register is updated by one for each step. When u=0, the track register is not updated.

On the FDC 1765/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.

Restore (Seek Track 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. if $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r_1r_0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FDC 176X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when MR goes from an active to an inactive state.

Seek

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FDC 176X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command. Note: When using multiple drives, the track register must be updated for the drive selected before seeks are issued.

Step

Upon receipt of this command, the FDC 176X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the u flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step-In

Upon receipt of this command, the FDC 176X issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step-Out

Upon receipt of this command, the FDC 176X issues one stepping pulse in the direction towards track 0. If the u flag is on, the Track Register is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of command. An interrupt is generated at the completion of the command.

Head Positioning

The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 30 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. If $\overline{TEST}$=0, there is zero settling time. There is also a 30 ms head settling time if the E flag is set in any Type II or III command.

The rates (shown in Table 2) can be applied to a Step-Direction Motor through the device interface.

Step—A 4 μs (MFM) or 8 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC)—The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 24 μs before the first stepping pulse is generated.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V=1) in the command word to a logic 1. The verification operation begins at the end of the 30 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The FDC 176X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated.

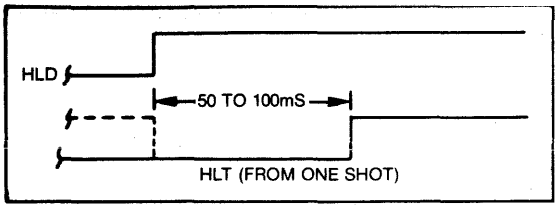
Table 2. Stepping Rates

$\overline{DDEN}$: r_1	r_0	0 $\overline{TEST}$=1	1 $\overline{TEST}$=1	X $\overline{TEST}$=0
0	0	6 ms	6 ms	368μs
0	1	12 ms	12 ms	380μs
1	0	20 ms	20 ms	396μs
1	1	30 ms	30 ms	416μs

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h=1), at the end of the Type I command if the verify flag (V=1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h=0 and V=0); or if the FDC 176X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load Timing (HLT) is an input to the FDC 176X which is used for the head engage time. When HLT=1, the FDC 176X assumes the head is completely engaged.

The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FDC 176X.



Head Load Timing

When both HLD and HLT are true, the FDC 176X will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

TYPE I COMMANDS FLAG SUMMARY
h=Head Load Flag (Bit 3)
h=1, Load head at beginning
h=0, Unload head at beginning
V=Verify flag (Bit 2)
V=1, Verify on destination track
V=0, No verify
r_1r_0=Stepping motor rate (Bits 1-0)
Refer to Table 2 for rate summary
u=Update flag (Bit 4)
u=1, Update Track register
u=0, No update

EXCEPTIONS
On the FDC 1765/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.

Type II Commands

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the system must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag=1 (this is the normal case) HLD is made active and HLT is sampled until true after a 30 msec delay. If the E flag is 0, HLD is made active and HLT is sampled with no delay until true. The ID field and Data Field format are shown below.

When an ID field is located on the disk, the FDC 176X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there is a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FDC 176X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m=0, a single sector is read or written and an interrupt is generated at the completion of the command. If m=1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FDC 176X will read or write multiple records starting with the sector presently in the sector register. The FDC 176X will continue to read or write multiple records and update the sector register in numerical ascending sequence until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

If the Sector Register exceeds the number of sectors on the track, the Record-Not-Found status bit will be set.

The Type II commands also contain side select compare flags. When C=0, no side comparison is made. When C=1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag. If the S flag compares with the side number recorded in the ID field, the 176X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The Type II and III commands for the FDC 1765/67 contain a side select flag (bit 1). When U = 0, SSO is updated to 0. Similarly, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not compare within 5 revolutions, the interrupt line is made active and the RNF status bit is set.

The FDC 1765/7 READ SECTOR and WRITE SECTOR commands include a 'b' flag. The 'b' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatibility, the 'b' flag should be set to a one. The 's' flag allows direct control over the SSO Line (Pin 25) and is set or reset at the beginning of the command, dependent upon the value of this flag.

Sector Length Table (1761/3 only)	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

Field Format

GAP III	ID AM	TRACK NUMBER	SIDE NUMBER	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP II	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD										DATA FIELD		

In MFM only, IDAM and DATA AM are preceded by three bytes of A1 with clock transition between bits 4 and 5 missing.

Read Sector

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record-Not-Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

Write Sector

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FDC 176X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The FDC 176X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing, the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated. For a 1 MHz clock, the INTRQ will set 16 or 24 μsec after the last CRC byte is written.

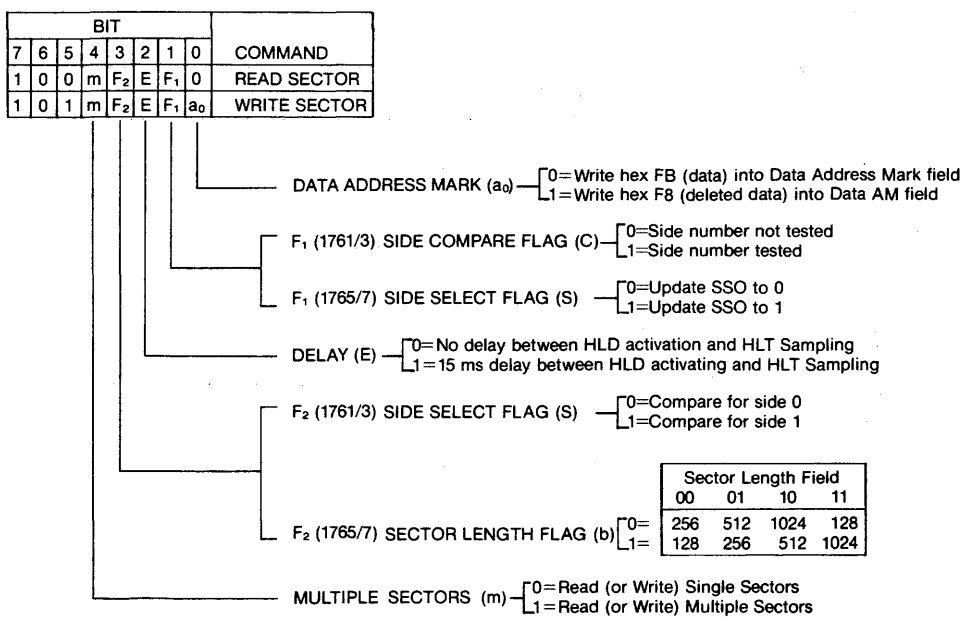


Figure 1. Type II and III Flag Summary

Type III Commands

There are three Type III Commands:

- READ ADDRESS—Read the next ID field (6 bytes) into the FDC.
- READ TRACK—Read all bytes of the entire track, including gaps.
- WRITE TRACK—Write all bytes to the entire track, including gaps.

Read Address

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FDC176X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

Read Track

Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated. RG is not activated during the Read Track Command. An internal side compare is not performed during a Read Track.

This command has several characteristics which make it suitable for diagnostic purposes. They are: the Read Gate is not activated during the command; no CRC checking is performed; gap information is included in the data stream; the internal side compare is not per-

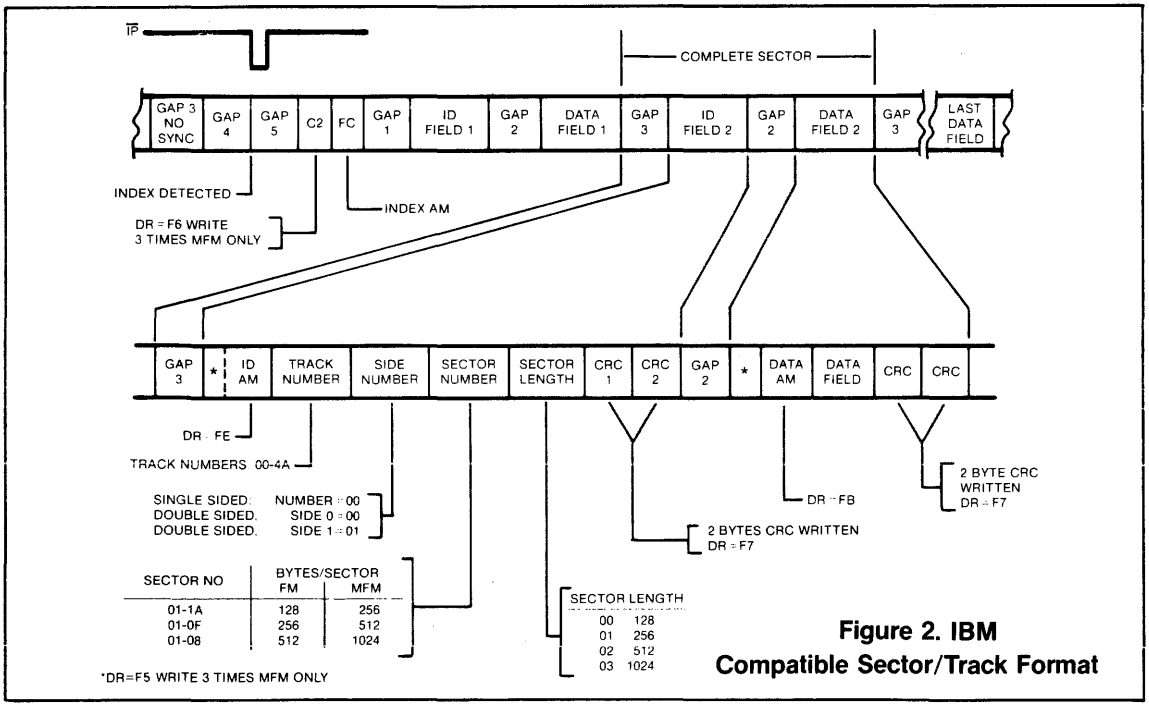


Figure 2. IBM Compatible Sector/Track Format

Table 3. Control Bytes For Initialization

DATA PATTERN IN DR (HEX)	FDC 176X INTERPRETATION IN FM (DDEN = 1)	FDC 176X INTERPRETATION IN MFM (DDEN = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Now Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5

**Missing clock transition between bits 3 and 4.

formed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule the Lost Data status flag is set. The ID A.M., ID field, ID CRC bytes, DAM, Data, and Data CRC Bytes for each sector will be correct. The Gap Bytes may be read incorrectly during write-splice time because of synchronization.

Write Track

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM.

Disk formatting (initialization) is accomplished by the Write Track command. Each byte for the entire track must be provided for proper formatting. This includes gap as well as data bytes.

The sequence required to format a diskette begins with positioning the Read/Write head at the desired track. Once this has been done, it is necessary to perform a Write Track command to store all the information on a track. The Write Track command uses DRQ to request each byte from the system MPU, starting with the byte at the beginning of the physical Index Pulse and ending with the last gap bytes at the end of the track. Figure 2 illustrates the IBM standard for track formatting.

Normally, each data byte stored on the diskette must be generated by the system MPU and passed into the FDC Data Register. However, there are exceptions to this rule. If a data byte of hex F5 through FE is entered into the Data Register, then the FDC recognizes this as an AM with missing clocks or CRC generation code. Consequently, F5 through FE must not be used in gaps, data fields, or ID fields, as this will disrupt normal operation of the FDC during formatting. Table 3 shows the definition of F5 through FE for disk intialization.

Type IV Commands

Force Interrupt is the only Type IV command. This command permits the MPU to terminate (abort) any command in progress. Figure 3 tabulates the Type IV command option bits.

The four bits, I_0-I_3, are used to select the condition of the interrupt occurrence. Regardless of which bit is set, any command currently being executed is immediately terminated and the Busy status bit is cleared, indicating "Not Busy". Then, when the condition is met, INTRQ goes high, causing the required interrupt.

If I_0-I_3 are all "0", no interrupt occurs, but any currently executing command is immediately terminated. If more than one condition is selected, then the interrupt occurs when any of the conditions is met.

To clear the interrupt, it is necessary to read the Status Register or to write the Command Register. An exception, however, is for I_3=1 (Immediate Interrupt). For this case, the interrupt is cleared with another Force Interrupt command with I_0-I_3 all low.

It is necessary to wait 16 microseconds (double density) or 32 microseconds (single density) before issuing a new command after issuing a force interrupt. Loading a new command sooner than this will nullify the forced interrupt.

Status Register

The Status Register permits the MPU to monitor a variety of conditions in the FDC. For each command, the individual status bits have their own meaning. When a command is initiated (except for the Force Interrupt command), the Busy status bit is set and the others are cleared or updated. If the Force Interrupt command is entered when another command is in progress, the Busy status bit is cleared, but the others remain unaffected. However, if the Force Interrupt command is initiated when there is *not* another command in progress, the other status bits are cleared or updated and represent the Type I Command status. Figure 4 illustrates the meaning of the status bits for each command.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are shown in Figure 3A.

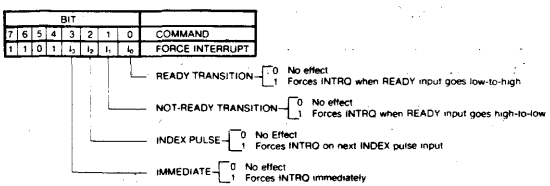


Figure 3.
Force Interrupt Command Flags

Operation	Next Operation	Delay Req'd. FM	Delay Req'd. MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	24 μs	12 μs
Write to Command Reg.	Read Status Bits 1-7	56 μs	28 μs
Write Any Register	Read From Diff. Register	0	0

Figure 3A.
Observed delay during programmed I/O

Figure 4A. Status Register Summary

COMMAND	STATUS BIT							
	7	6	5	4	3	2	1	0
ALL TYPE I	Not Ready	Write Protect	Head Loaded	Seek Error	CRC Error	Track 0	Index	Busy
READ SECTOR	Not Ready	0	Record Type	Rec not Found	CRC Error	Lost Data	DRQ	Busy
WRITE SECTOR	Not Ready	Write Protect	Write Fault	Rec not Found	CRC Error	Lost Data	DRQ	Busy
READ ADDRESS	Not Ready	0	0	Rec not Found	CRC Error	Lost Data	DRQ	Busy
READ TRACK	Not Ready	0	0	0	0	Lost Data	DRQ	Busy
WRITE TRACK	Not Ready	Write Protect	Write Fault	0	0	Lost Data	DRQ	Busy

Figure 4B. Status Description for Type I Commands

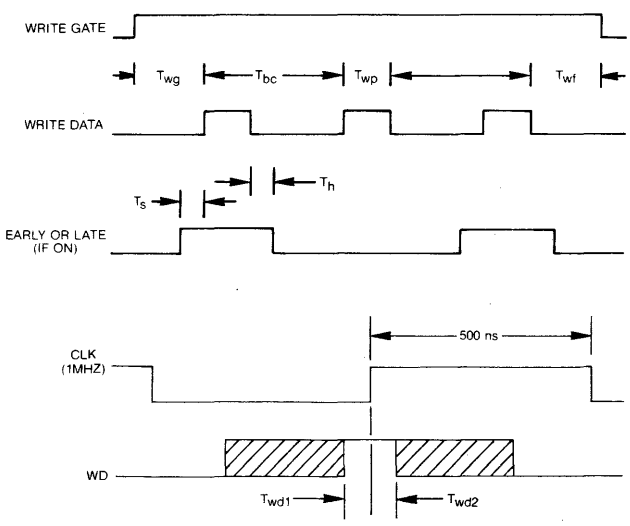
BIT	NAME	MEANING
S7	NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6	PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5	HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4	SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3	CRC ERROR	CRC encountered in ID field.
S2	TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TR00}}$ input.
S1	INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0	BUSY	When set command is in progress. When reset no command is in progress.

Figure 4C. Status Description for Type II and III Commands

BIT	NAME	MEANING
S7	NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6	WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5	RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1=Deleted Data Mark. 0=Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4	RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3	CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2	LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1	DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0	BUSY	When set, command is under execution. When reset, no command is under execution.

Write Data Timing:

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Write Data Pulse Width	T_{wp}	900	1000	550	nsec	FM
		300	500	250	nsec	MFM
Write Gate to Write Data	T_{wg}		4		μsec	FM
			2		μsec	MFM
Write data cycle Time	T_{bc}		4, 6, or 8		μsec	±CLK Error
Early (Late) to Write Data	T_s	250			nsec	MFM
Early (Late) From Write Data	T_h	250			nsec	MFM
Write Gate off from WD	T_{wf}		4		μsec	FM
			2		μsec	MFM
WD Valid to Clk	T_{wd1}	100			nsec	
WD Valid after Clk	T_{wd2}	100			nsec	



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +15V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, V_{DD}=+12V±5% unless otherwise noted)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS							
Input Voltage Levels							
Low Level, V_{IL}					0.8	V	
High Level, V_{IH}			2.6			V	
Output Voltage Levels							
Low Level V_{OL}					0.45	V	I_{OL} = 1.6 mA
High Level V_{OH}			2.8			V	I_{OH}=100 μA
Output Leakage, I_{LO}					10	μA	$V_{OUT}=V_{DD}$
Input Leakage, I_{IL}					10	μA	$V_{IN}=V_{DD}$
Output Capacitance				5		pf	
Input Capacitance				10		pf	
Power Dissipation					600	mW	
AC CHARACTERISTICS							
Processor Read Timing							
Address Setup Time		t_{SETR}	50			ns	Figure 5
Address Hold Time		t_{HLDR}	10			ns	Figure 5
RE Pulse Width (C_L=50pF)		t_{RE}	400			ns	Figure 5
DRQ Reset Time		t_{DRR}			500	ns	Figure 5
INTRQ Reset Time		t_{IRR}		1000	6000	ns	Figure 5
Data Delay Time (C_L=50pF)		t_{DACC}			350	ns	Figure 5
Data Hold Time (C_L=50pF)		t_{DOH}	50		150	ns	Figure 5
Microprocessor Write Timing							
Address Setup Time		t_{SETW}	50			ns	Figure 6
Address Hold Time		t_{HLDW}	10			ns	Figure 6
WE Pulse Width		t_{WE}	350			ns	Figure 6
DRQ Reset Time		t_{DRR}			500	ns	Figure 6
INTRQ Reset Time		t_{IRR}		1000	6000	ns	Figure 6
Data Setup Time		t_{DS}	250			ns	Figure 6
Data Hold Time		t_{DH}	70			ns	Figure 6
Disk Input Data Timing							
RAWREAD Pulse Width		t_{pw}	100	200		ns	Figure 7, See Note
Clock Setup Time		t_d	40			ns	Figure 7 See Note
Clock Hold Time for MFM		t_{cd}	40			ns	Figure 7
Clock Hold Time for FM		t_{cs}	40			ns	Figure 7
RAWREAD Cycle Time		t_{bc}	3000			ns	3600 at 70°C, Figure 7
RCLK High Pulse Width	MFM	t_a	1.6	2		μs	Figure 7
	FM		1.6	4		μs	Figure 7
RCLK Low Pulse Width	MFM	t_b	1.6	2		μs	Figure 7
	FM		1.6	4		μs	Figure 7
RCLK Cycle Time	MFM	t_c		4		μs	Figure 7
	FM			8		μs	Figure 7
Miscellaneous Timing							
CLK Low Pulse Width		t_{CD1}	460	500	20000	ns	Figure 8
CLK High Pulse Width		t_{CD2}	460	500	20000	ns	Figure 8
STEP Pulse Width	MFM	t_{STP}	4			μs	Figure 8
	FM		8			μs	Figure 8
DIRC Setup Time		t_{DIR}		24		μs	Figure 8
MR Pulse Width		t_{MR}	50			μs	Figure 8
IP Pulse Width		t_{IP}	10			μs	Figure 8
WF Pulse Width		t_{WF}	10			μs	Figure 8
CLK Cycle Time		t_{CYC}		1.0		μs	Figure 8

Figure 5. Microprocessor Read Timing

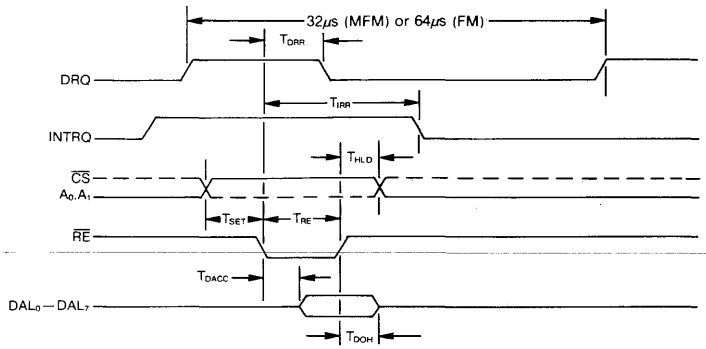


Figure 6. Microprocessor Write Timing

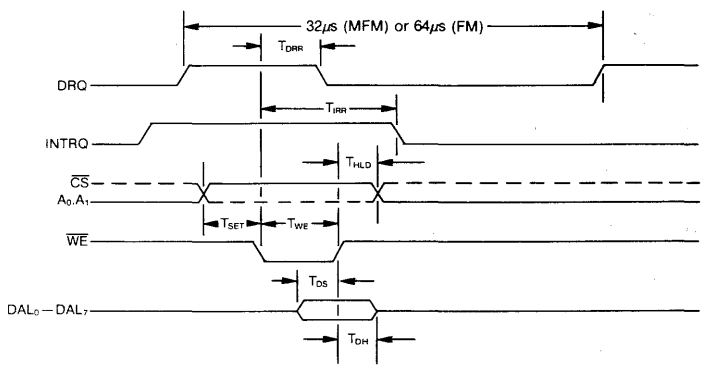
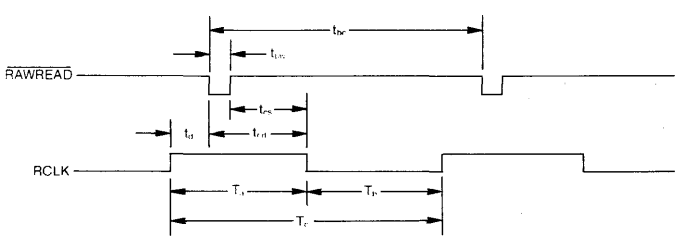
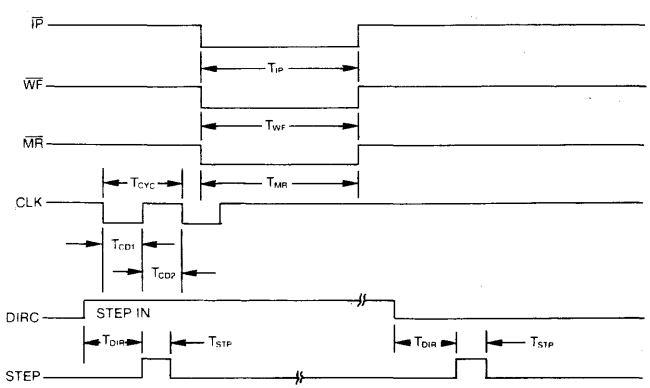


Figure 7. Disk Input Timing



Note: Pulse width on RAW READ (Pin 27) is normally 10-300 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 600 ns for MFM at CLK = 1 MHz and 1200 ns for FM at 1 MHz.

Figure 8. Miscellaneous Timing



Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

IBM 3740 Format
This single-density (FM) format utilizes 128 bytes/sector. The bytes to be generated by the system MPU for use in the execution of the Write Track command are shown in Figure 9.

IBM System 34 Format
This double-density (MFM) format utilizes 256 bytes/sector. The bytes to be generated by the system MPU for use in the execution of the Write Track command are shown in Figure 10.

Non-IBM Formats
Unique (non-IBM) formats are permissible providing the following restrictions are understood.

- Sector length may only be 128, 256, 512, or 1024 bytes.
- Gap sizes must conform to Figure 11.

In addition, the Index Address Mark is not required for operation by the FDC 176X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for FDC 176X operation, however PLL lock up time, motor speed variation, write-splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the appropriate format be used for highest system reliability.

	DATA BYTE (hex)	NO. OF BYTES	COMMENTS
	FF	40	Gap 5 (Post Index)
	00	6	
	FC	1	Index AM
	FF	26	Gap 1
	00	6	
	FE	1	ID AM
	XX	1	Track Number (00-4C)
	0X	1	Side Number (00 or 01)
	XX	1	Sector Number (01-1A)
	00	1	Sector Length (128 bytes)
ONE SECTOR ①	F7	1	Causes 2-Byte CRC to be Written
	FF	11	Gap 2 (ID Gap)
	00	6	
	FB	1	Data AM
	E5	128	Data Field
	F7	1	Causes 2-Byte CRC to be Written
	FF	27	Part of Gap 3 (Data Gap)
	FF	247 ②	Gap 4 (Pre Index)

Figure 9. Byte Sequence for IBM 3740 Formatting

NOTES: 1. THIS PATTERN MUST BE WRITTEN 26 TIMES PER TRACK.
2. CONTINUE WRITING HEX FF UNTIL FDC COMPLETES SEQUENCE AND GENERATES INTRQ INTERRUPT

	DATA BYTE (hex)	NO. OF BYTES	COMMENTS
	4E	80	Gap 5 (Post Index)
	00	12	
	F6	3	Writes C2
	FC	1	Index AM
	4E	50	
	00	12	Gap 1
	F5	3	Writes A1
	FE	1	ID AM
	XX	1	Track Number (00-4C)
ONE SECTOR ①	0X	1	Side Number (00 or 01)
	XX	1	Sector Number (01-1A)
	01	1	Sector Length (256 Bytes)
	F7	1	Causes 2-Byte CRC to be Written
	4E	22	Gap 2 (ID Gap)
	00	12	
	F5	3	Writes A1
	FB	1	Data AM
	40	256	Data Field
	F7	1	Causes 2-Byte CRC to be Written
	4E	54	Part of Gap 3 (Data Gap)
	4E	598 ②	Gap 4 (Pre Index)

Figure 10. Byte Sequence for IBM System-34 Formatting

NOTES: 1. THIS PATTERN MUST BE WRITTEN 26 TIMES PER TRACK.
2. CONTINUE WRITING HEX 4E UNTIL FDC COMPLETES SEQUENCE AND GENERATES INTRQ INTERRUPT.

GAP	SINGLE DENSITY (FM)	DOUBLE DENSITY (MFM)	NOTE
Gap 1	16 bytes FF	16 bytes 4E	2
Gap 2	11 bytes FF 6 bytes 00	22 bytes 4F 12 bytes 00 3 bytes A1	1
Gap 3	10 bytes FF 4 bytes 00	16 bytes 4E 8 bytes 00 3 bytes A1	2
Gap 4	16 bytes FF	16 bytes 4E	2

NOTES: 1. THESE BYTES COUNTS ARE EXACT.
2. THESE BYTES COUNTS ARE MINIMUM EXCEPT FOR 3 BYTES A1, WHICH IS EXACT.

Figure 11. Gap Size Limitations

STANDARD MICROSYSTEMS CORPORATION

FDC 1791-02
FDC 1792-02
FDC 1793-02
FDC 1794-02
FDC 1795-02
FDC 1797-02

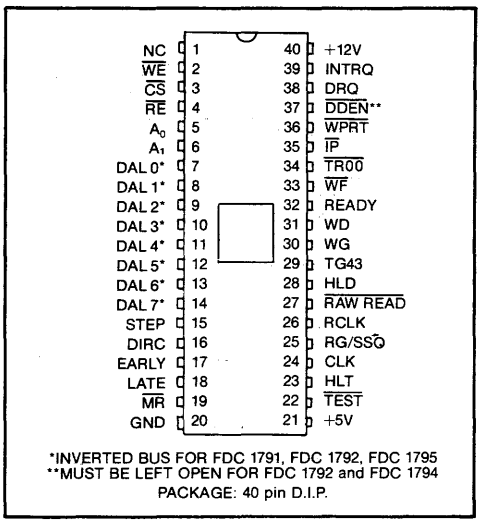
Floppy Disk Controller/Formatter FDC

μPC FAMILY

FEATURES

- ☐ SOFT SECTOR FORMAT COMPATIBILITY
- ☐ AUTOMATIC TRACK SEEK WITH VERIFICATION
- ☐ ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
- ☐ READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128 Byte or Variable Length Record
- ☐ WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Initialization
- ☐ PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- ☐ SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-chip Track and Sector Registers/Comprehensive Status Information
- ☐ WRITE PRECOMPENSATION (MFM AND FM)
- ☐ SIDE SELECT LOGIC (FDC 1795, FDC 1797)
- ☐ WINDOW EXTENSION (IN MFM)

PIN CONFIGURATION



*INVERTED BUS FOR FDC 1791, FDC 1792, FDC 1795
**MUST BE LEFT OPEN FOR FDC 1792 and FDC 1794
PACKAGE: 40 pin D.I.P.

- ☐ INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- ☐ COMPATIBLE WITH FD179X-02
- ☐ COPLAMOS® n-CHANNEL MOS TECHNOLOGY
- ☐ COMPATIBLE WITH THE FDC 9216 FLOPPY DISK DATA SEPARATOR

GENERAL DESCRIPTION

The FDC 179X is an MOS/LSI device which performs the functions of a Floppy Disk Controller/Formatter in a single chip implementation. The basic FDC 179X chip design has evolved into six specific parts: FDC 1791, FDC 1792, FDC 1793, FDC 1794, FDC 1795, and the FDC 1797.

This FDC family performs all the functions necessary to read or write data to any type of floppy disk drive. Both 8" and 5¼" (mini-floppy) drives with single or double density storage capabilities are supported. These n-channel MOS/LSI devices will replace a large amount of discrete logic required for interfacing a host processor to a floppy disk.

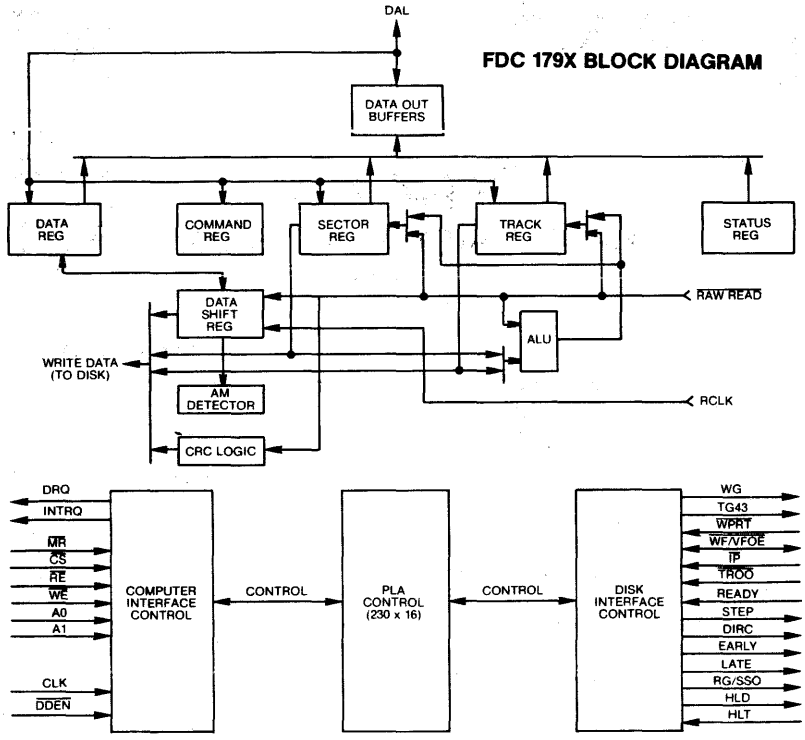
The FDC 1791 is IBM 3740 compatible in single density mode (FM) and System 34 compatible in double density mode (MFM). The FDC 1791 contains enhanced features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation.

The FDC 1793 is identical to the FDC 1791 except the DAL lines are TRUE for systems that utilize true data busses.

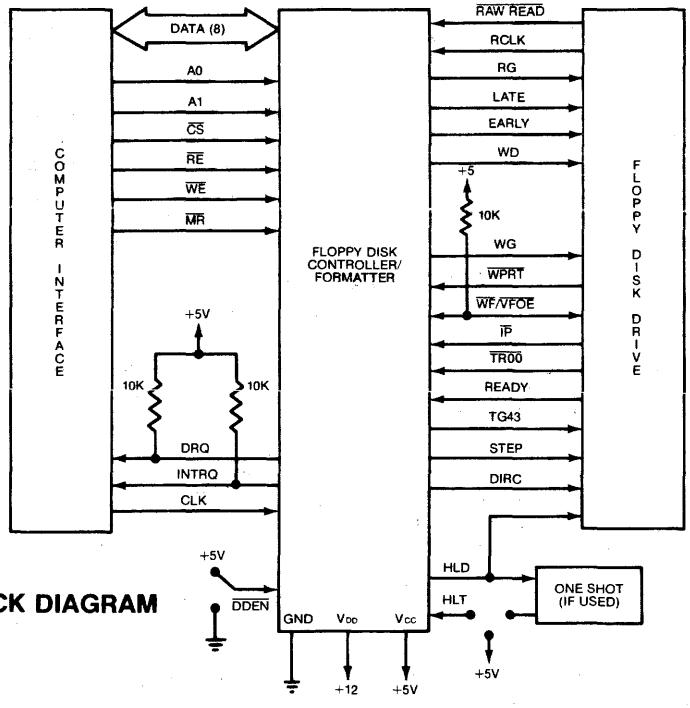
The FDC 1792 operates in the single density mode only. Pin 37 (DDEN) of the FDC 1792 must be left open for proper operation. The FDC 1794 is identical to the FDC 1792 except the DAL lines are TRUE for systems that utilize true data busses. The FDC 1795 adds side select logic to the FDC 1791. The FDC 1797 adds the side select logic to the FDC 1793.

The processor interface consists of an 8 bit bidirectional bus for data, status, and control word transfers. This family of controllers is configured to operate on multiplexed bus with other bus-oriented devices.

FDC 179X BLOCK DIAGRAM



SYSTEM BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	NO CONNECTION	NC	This pin is internally connected to the substrate bias generator and must be left open.
20	GROUND	V_{SS}	Ground
21	POWER SUPPLY	V_{CC}	+5V
40	POWER SUPPLY	V_{DD}	+12V
19	MASTER RESET	$\overline{MR}$	A logic low on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a Restore Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into the sector register.
COMPUTER INTERFACE:			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and the parallel data bus (DAL).
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on DALØ-DAL7 when $\overline{CS}$ is low.
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control:
7-14	DATA ACCESS LINES	DAL0-DAL7	Eight bit Bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by $\overline{WE}$ or a transmitter enabled by $\overline{RE}$. The Data Bus is inverted on the FDC 1791, FDC 1792 and FDC 1795.
24	CLOCK	CLK	This input requires a free-running square wave clock for internal timing reference, 2 MHz for 8" drives, 1 MHz for 5¼" drives.
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use a 10K pull-up resistor to +5V.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register or the status register is read. Use a 10K pull-up resistor to +5V.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	Step and direction motor control. The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the write data pulse occurring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.
22	TEST	$\overline{TEST}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated motors.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged.

A1	A0	$\overline{RE}$	$\overline{WE}$
0	0	Status Reg	Command Reg
0	1	Track Reg	Track Reg
1	0	Sector Reg	Sector Reg
1	1	Data Reg	Data Reg

PIN NO.	NAME	SYMBOL	FUNCTION
25	READ GATE (1791/3)	RG	A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered, and is used for synchronization.
25	SIDE SELECT OUTPUT (1795, 1797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When S=1, SSO is set to a logic 1. When S=0, SSO is set to a logic 0. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	A 250 ns (MFM) or 500 ns (FM) pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$/ $\overline{\text{VFO ENABLE}}$	$\overline{\text{WF/VFOE}}$	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG=1, Pin 33 functions as a $\overline{\text{WF}}$ input. If $\overline{\text{WF}}$=0, any write command will immediately be terminated. When WG=0, Pin 33 functions as a $\overline{\text{VFOE}}$ output. $\overline{\text{VFOE}}$ will go low during a read operation after the head has loaded and settled (HLT=1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. $\overline{\text{VFOE}}$ will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, $\overline{\text{VFOE}}$ will remain low until the end of the Data Field.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FDC179X that the Read/Write head is positioned over Track 00.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	This input informs the FDC179X when the index hole is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	$\overline{\text{DOUBLE DENSITY}}$	$\overline{\text{DDEN}}$	This pin selects either single or double density operation. When $\overline{\text{DDEN}}$=0, double density is selected. When $\overline{\text{DDEN}}$=1, single density is selected. This line must be left open on the 1792/4.

FUNCTIONAL DESCRIPTION

The FDC 179X-02 major functional blocks are as follows:

Data Shift Register—This 8-bit register assembles serial data from the Read Data input ($\overline{\text{RAW READ}}$) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register—This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Sector Register (SR)—This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR)—This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a Force Interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR)—This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic—This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x)=x^{16}+x^{12}+x^5+1$.

Track Register—This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU)—The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control—All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

AM Detector—The address mark detector detects ID, data and index address marks during ready and write operations.

OPERATION

FDC 1791, FDC 1793, FDC 1795 and FDC 1797 have two modes of operation according to the state of $\overline{\text{DDEN}}$ (Pin 37). When $\overline{\text{DDEN}}=1$, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled.

DDEN must be left open for the FDC 1792 and FDC 1794.

Disk Read Operation

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{\text{DDEN}}$ should be placed to logical "1." For MFM formats, $\overline{\text{DDEN}}$ should be placed to a logical "0." Sector lengths are determined at format time by a special byte in the "ID" field. If this Sector length byte in the ID field is zero, then the sector length is 128 bytes. If 01 then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes. The number of sectors per track can be from 1 to 255 sectors. The number of tracks is from 0 to 255 tracks.

For read operations, the FDC 179X requires $\overline{\text{RAW READ}}$ Data (Pin 27) signal which is a 250 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not, it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FDC179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FDC179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FDC179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG=0), the $\overline{\text{VFOE}}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{\text{VFOE}}$ will go active when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 179X is inspecting data off the disk

If $\overline{\text{WF/VFOE}}$ is not used, leave open or tie to a 10K resistor to +5.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is

transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

Disk Write Operation

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution against erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FDC179X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The $\overline{\text{Write Fault}}$ input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FDC179X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FDC179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{\text{DDEN}}$=1) and 250 ns pulses in MFM ($\overline{\text{DDEN}}$=0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FDC179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

COMMAND WORDS

The FDC179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 1.

Table 1. Command Summary

		BITS							
COMMAND	TYPE	7	6	5	4	3	2	1	0
Restore	I	0	0	0	0	h	V	r_1	r_0
Seek	I	0	0	0	1	h	V	r_1	r_0
Step	I	0	0	1	u	h	V	r_1	r_0
Step In	I	0	1	0	u	h	V	r_1	r_0
Step Out	I	0	1	1	u	h	V	r_1	r_0
Read Sector	II	1	0	0	m	F_2	E	F_1	0
Write Sector	II	1	0	1	m	F_2	E	F_1	a_0
Read Address	III	1	1	0	0	0	E	0	0
Read Track	III	1	1	1	0	0	E	0	0
Write Track	III	1	1	1	1	0	E	0	0
Force Interrupt	IV	1	1	0	1	i_3	i_2	i_1	i_0

Type I Commands

The Type I Commands are Restore, Seek, Step, Step-In, and Step-Out. Each of the Type I Commands contains a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 2.

The Type I Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h=1, the head is loaded at the beginning of the command (HLD output is made active). If h=0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FDC179X receives a command that specifically disengages the head. If the FDC179X is idle (busy=0) for 15 revolutions of the disk, the head will be automatically disengaged (HLD made inactive).

The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V=1, a verification is performed, if V=0, no verification is performed.

During verification, the head is loaded and after an internal 15 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field if read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt

is generated, and Seek Error Status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the FDC179X terminates the operation and sends an interrupt (INTRQ).

The Step, Step-In, and Step-Out commands contain an Update flag (u). When u=1, the track register is updated by one for each step. When u=0, the track register is not updated.

On the FDC 1795/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.

Restore (Seek Track 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. if $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r_1r_0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FDC179X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when MR goes from an active to an inactive state.

Seek

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FDC179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step

Upon receipt of this command, the FDC179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the u flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step-In

Upon receipt of this command, the FDC179X issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step-Out

Upon receipt of this command, the FDC179X issues one stepping pulse in the direction towards track 0. If the u flag is on, the Track Register is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of command. An interrupt is generated at the completion of the command.

Head Positioning

The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If $\overline{TEST}$=0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

The rates (shown in Table 2) can be applied to a Step-Direction Motor through the device interface.

Step—A 2 μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC)—The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V=1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The FDC179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated.

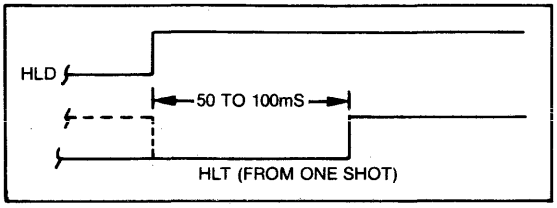
Table 2. Stepping Rates

CLK:		2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
$\overline{DDEN}$:		0	1	0	1	X	X
r_1	r_0	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=0	$\overline{TEST}$=0
0	0	3 ms	3 ms	6 ms	6 ms	184μs	368μs
0	1	6 ms	6 ms	12 ms	12 ms	190μs	380μs
1	0	10 ms	10 ms	20 ms	20 ms	198μs	396μs
1	1	15 ms	15 ms	30 ms	30 ms	208μs	416μs

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h=1), at the end of the Type I command if the verify flag (V=1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h=0 and V=0); or if the FDC179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load Timing (HLT) is an input to the FDC179X which is used for the head engage time. When HLT=1, the FDC179X assumes the head is completely engaged.

The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FDC179X.



Head Load Timing

When both HLD and HLT are true, the FDC179X will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

TYPE I COMMANDS FLAG SUMMARY
h=Head Load Flag (Bit 3)
h=1, Load head at beginning h=0, Unload head at beginning
V=Verify flag (Bit 2)
V=1, Verify on destination track V=0, No verify
r_1r_0=Stepping motor rate (Bits 1-0)
Refer to Table 2 for rate summary
u=Update flag (Bit 4)
u=1, Update Track register u=0, No update

Type II Commands

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the system must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag=1 (this is the normal case) HLD is made active and HLT is sampled until true after a 15 msec delay. If the E flag is 0, HLD is made active and HLT is sampled with no delay until true. The ID field and Data Field format are shown below.

When an ID field is located on the disk, the FDC179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there is a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FDC179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m=0, a single sector is read or written and an interrupt is generated at the completion of the command. If m=1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FDC179X will read or write multiple records starting with the sector presently in the sector register. The FDC179X will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

If the Sector Register exceeds the number of sectors on the track, the Record-Not-Found status bit will be set.

The Type II commands also contain side select compare flags. When C=0, no side comparison is made. When C=1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag. If the S flag compares with the side number recorded in the ID field, the 179X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The FDC1795/7 READ SECTOR and WRITE SECTOR commands include a 'b' flag. The 'b' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatability, the 'b' flag should be set to a one. The 's' flag allows direct control over the SSO Line (Pin 25) and is set or reset at the beginning of the command, dependent upon the value of this flag.

Sector Length Table (1791/2/3/4 only)	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

Field Format

GAP III	ID AM	TRACK NUMBER	SIDE NUMBER	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP II	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD										DATA FIELD		

In MFM only, IDAM and DATA AM are preceded by three bytes of A1 with clock transition between bits 4 and 5 missing.

Read Sector

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record-Not-Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

Write Sector

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FDC179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The FDC179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated.

BIT 7	6	5	4	3	2	1	0	COMMAND
1	0	0	m	F_2	E	F_1	0	READ SECTOR
1	0	1	m	F_2	E	F_1	a_0	WRITE SECTOR

DATA ADDRESS MARK (a_0) — 0=Write hex FB (data) into Data Address Mark field; 1=Write hex F8 (deleted data) into Data AM field

F_1 (1791/3) SIDE COMPARE FLAG (C) — 0=Side number not tested; 1=Side number tested

F_1 (1795/7) SIDE SELECT FLAG (S) — 0=Update SSO to 0; 1=Update SSO to 1

DELAY (E) — 0=No delay between HLD activation and HLT Sampling; 1=15 ms delay between HLD activating and HLT Sampling

F_2 (1791/3) SIDE SELECT FLAG (S) — 0=Compare for side 0; 1=Compare for side 1

F_2 (1795/7) SECTOR LENGTH FLAG (b)

Sector Length Field	00	01	10	11
0=	256	512	1024	128
1=	128	256	512	1024

MULTIPLE SECTORS (m) — 0=Read (or Write) Single Sectors; 1=Read (or Write) Multiple Sectors

Figure 1. Type II and III Flag Summary

Type III Commands

There are three Type III Commands:

- READ ADDRESS—Read the next ID field (6 bytes) into the FDC.
- READ TRACK—Read all bytes of the entire track, including gaps.
- WRITE TRACK—Write all bytes to the entire track, including gaps.

Read Address

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FDC179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

Read Track

Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated. RG is not activated during the Read Track Command. An internal side compare is not performed during a Read Track.

Write Track

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which

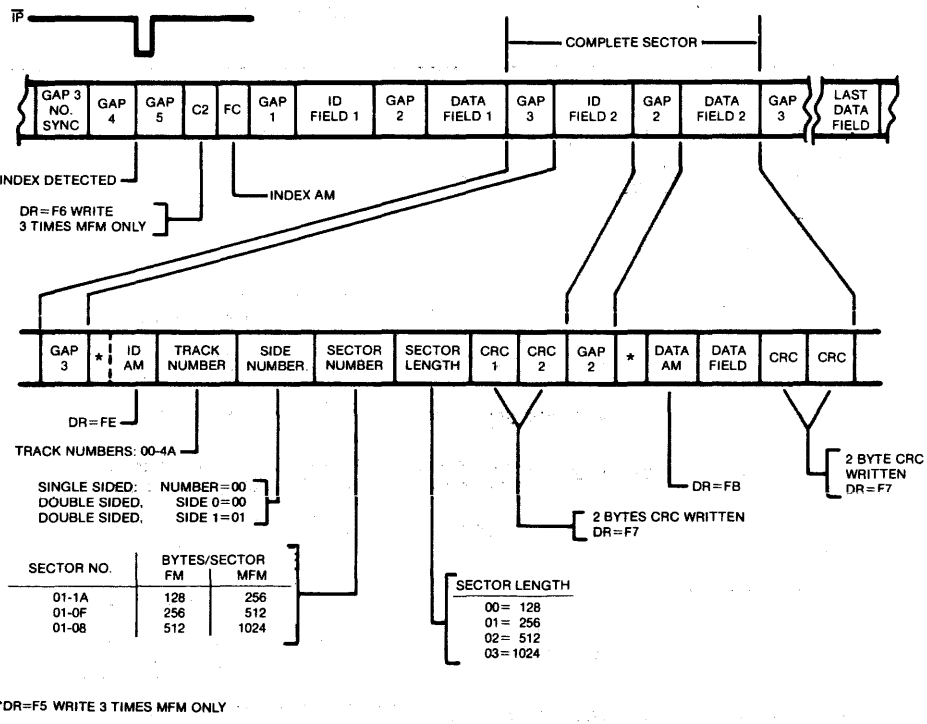


Figure 2. IBM Compatible Sector/Track Format

time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM.

Disk formatting (initialization) is accomplished by the Write Track command. Each byte for the entire track must be provided for proper formatting. This includes gap as well as data bytes.

The sequence required to format a diskette begins with positioning the Read/Write head at the desired track. Once this has been done, it is necessary to perform a Write Track command to store all the information on a track. The Write Track command uses DRQ to request each byte from the system MPU, starting with the byte at the beginning of the physical Index Pulse and ending with the last gap bytes at the end of the track. Figure 2 illustrates the IBM standard for track formatting.

Normally, each data byte stored on the diskette must be generated by the system MPU and passed into the FDC Data Register. However, there are exceptions to this rule. If a data byte of hex F5 through FE is entered into the Data Register, then the FDC recognizes this as an AM with missing clocks or CRC generation code. Consequently, F5 through FE must not be used in gaps, data fields, or ID fields, as this will disrupt normal operation of the FDC during formatting.

Type IV Commands

Force Interrupt is the only Type IV command. This command permits the MPU to terminate (abort) any command in progress. Figure 3 tabulates the Type IV command option bits.

The four bits, I_0-I_3, are used to select the condition of the interrupt occurrence. Regardless of which bit is set, any command currently being executed is immediately terminated and the Busy status bit is cleared, indicating "Not Busy". Then, when the condition is met, INTRQ goes high, causing the required interrupt.

If I_0-I_3 are all "0", no interrupt occurs, but any currently executing command is immediately terminated. If more than one condition is selected, then the interrupt occurs when any of the conditions is met.

To clear the interrupt, it is necessary to read the Status Register or to write the Command Register. An exception, however, is for $I_3=1$ (Immediate Interrupt). For this case, the interrupt is cleared with another Force Interrupt command with I_0-I_3 all low.

Status Register

The Status Register permits the MPU to monitor a variety of conditions in the FDC. For each command, the individual status bits have their own meaning. When a command is initiated (except for the Force Interrupt command), the Busy status bit is set and the others are cleared or updated. If the Force Interrupt command is entered when another command is in progress, the Busy status bit is cleared, but the others remain unaffected. However, if the Force Interrupt command is initiated when there is *not* another command in progress, the other status bits are cleared or updated and represent the Type I Command status. Figure 4 illustrates the meaning of the status bits for each command.

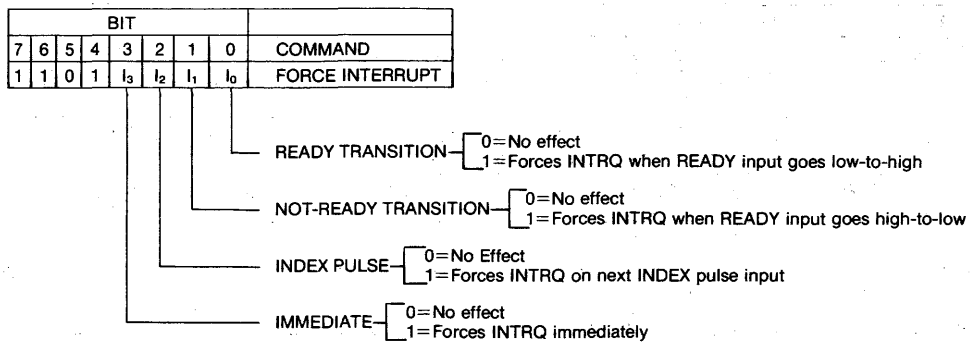


Figure 3. Force Interrupt Command Flags

Figure 4A. Status Register Summary

COMMAND	STATUS BIT							
	7	6	5	4	3	2	1	0
ALL TYPE I	Not Ready	Write Protect	Head Loaded	Seek Error	CRC Error	Track 0	Index	Busy
READ SECTOR	Not Ready	0	Record Type	Rec not Found	CRC Error	Lost Data	DRQ	Busy
WRITE SECTOR	Not Ready	Write Protect	Write Fault	Rec not Found	CRC Error	Lost Data	DRQ	Busy
READ ADDRESS	Not Ready	0	0	Rec not Found	CRC Error	Lost Data	DRQ	Busy
READ TRACK	Not Ready	0	0	0	0	Lost Data	DRQ	Busy
WRITE TRACK	Not Ready	Write Protect	Write Fault	0	0	Lost Data	DRQ	Busy

Figure 4B. Status Description for Type I Commands

BIT	NAME	MEANING
S7	NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6	PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{\text{WRPT}}$ input.
S5	HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4	SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3	CRC ERROR	CRC encountered in ID field.
S2	TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{\text{TR00}}$ input.
S1	INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0	BUSY	When set command is in progress. When reset no command is in progress.

Figure 4C. Status Description for Type II and III Commands

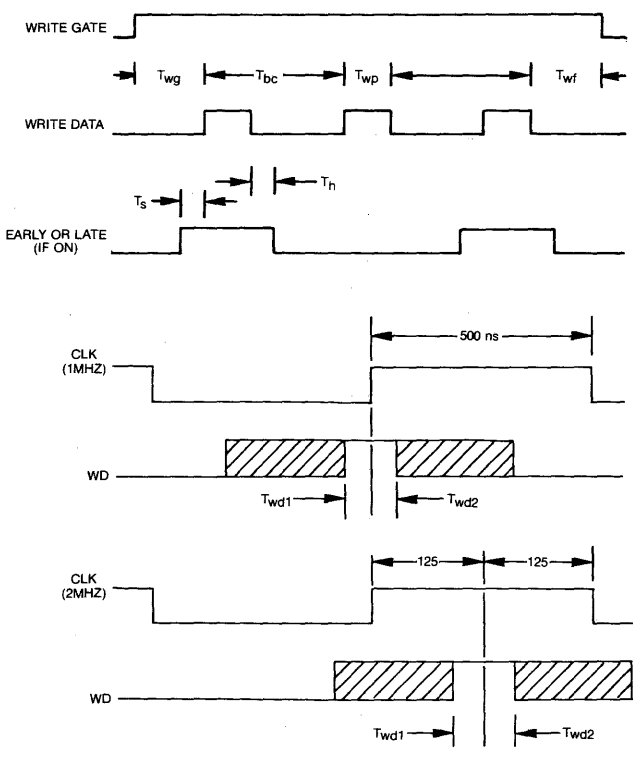
BIT	NAME	MEANING
S7	NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6	WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5	RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1=Deleted Data Mark. 0=Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4	RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3	CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2	LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1	DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0	BUSY	When set, command is under execution. When reset, no command is under execution.

Write Data Timing:

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Write Data Pulse Width	T_{wp}	450	500	550	nsec	FM
		150	200	250	nsec	MFM
Write Gate to Write Data	T_{wg}		2		μsec	FM
			1		μsec	MFM
Write data cyle Time	T_{bc}		2, 3, or 4		μsec	±CLK Error
Early (Late) to Write Data	T_s	125			nsec	MFM
Early (Late) From Write Data	T_h	125			nsec	MFM
Write Gate off from WD	T_{wf}		2		μsec	FM
			1		μsec	MFM
WD Valid to Clk	T_{wd1}	100			nsec	CLK=1 MHZ
		50			nsec	CLK=2 MHZ
WD Valid after Clk	T_{wd2}	100			nsec	CLK=1 MHZ
		30			nsec	CLK=2 MHZ

These values are doubled when CLK=1 MHz.

Write Data Timing



WRITE DATA/CLOCK RELATIONSHIP
($\overline{DDEN}$=0)

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +15V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, V_{DD}=+12V±5% unless otherwise noted)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS							
Input Voltage Levels							
Low Level, V_{IL}					0.8	V	
High Level, V_{IH}			2.6			V	
Output Voltage Levels							
Low Level V_{OL}					0.45	V	I_{OL}=1.6 mA
High Level V_{OH}			2.8			V	I_{OH}=100 μA
Output Leakage, I_{LO}					10	μA	$V_{OUT}=V_{DD}$
Input Leakage, I_{IL}					10	μA	$V_{IN}=V_{DD}$
Output Capacitance				5		pf	
Input Capacitance				10		pf	
Power Dissipation					500	mW	
AC CHARACTERISTICS							
Processor Read Timing							
Address Setup Time		t_{SETR}	50			ns	Figure 5
Address Hold Time		t_{HLDR}	10			ns	Figure 5
$\overline{RE}$ Pulse Width (C_L=50pF)		t_{RE}	400			ns	Figure 5
DRQ Reset Time		t_{DRR}			500	ns	Figure 5
INTRQ Reset Time		t_{IRR}		500*	3000*	ns	Figure 5
Data Delay Time (C_L=50pF)		t_{DACC}			350	ns	Figure 5
Data Hold Time (C_L=50pF)		t_{DOH}	50		150	ns	Figure 5
Microprocessor Write Timing							
Address Setup Time		t_{SETW}	50			ns	Figure 6
Address Hold Time		t_{HLDW}	10			ns	Figure 6
WE Pulse Width		t_{WE}	350			ns	Figure 6
DRQ Reset Time		t_{DRR}			500	ns	Figure 6
INTRQ Reset Time		t_{IRR}		500*	3000*	ns	Figure 6
Data Setup Time		t_{DS}	250			ns	Figure 6
Data Hold Time		t_{DH}	70			ns	Figure 6
Disk Input Data Timing							
RAWREAD Pulse Width		t_{pw}	100*	200		ns	Figure 7, See Note
Clock Setup Time		t_d	40			ns	Figure 7 See Note
Clock Hold Time for MFM		t_{cd}	40			ns	Figure 7
Clock Hold Time for FM		t_{cs}	40			ns	Figure 7
RAWREAD Cycle Time		t_{bc}	1500			ns	1800 at 70°C, Figure 7
RCLK High Pulse Width	MFM	t_a	0.8	1*		μs	Figure 7
	FM		0.8	2*		μs	Figure 7
RCLK Low Pulse Width	MFM	t_b	0.8	1*		μs	Figure 7
	FM		0.8	2*		μs	Figure 7
RCLK Cycle Time	MFM	t_c		2*		μs	Figure 7
	FM			4*		μs	Figure 7
Miscellaneous Timing							
CLK Low Pulse Width		t_{CD1}	230	250	20000	ns	Figure 8
CLK High Pulse Width		t_{CD2}	200	250	20000	ns	Figure 8
STEP Pulse Width	MFM	t_{STP}	2*			μs	Figure 8
	FM		4*			μs	Figure 8
DIRC Setup Time		t_{DIR}		12		μs	Figure 8
MR Pulse Width		t_{MR}	50*			μs	Figure 8
IP Pulse Width		t_{IP}	10*			μs	Figure 8
WF Pulse Width		t_{WF}	10*			μs	Figure 8
CLK Cycle Time		t_{CYC}		0.5*		μs	Figure 8

*: These Values are doubled when CLK=1 MHz.

Figure 5. Microprocessor Read Timing

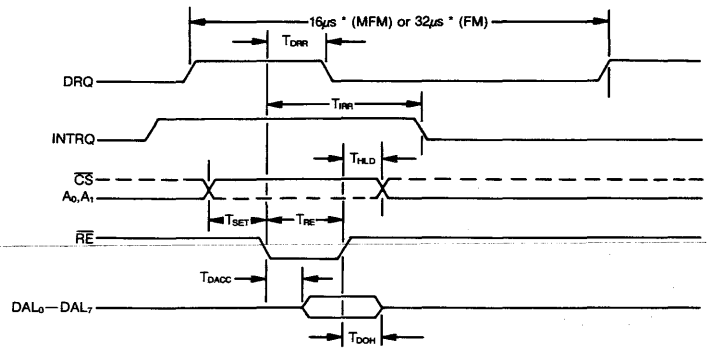


Figure 6. Microprocessor Write Timing

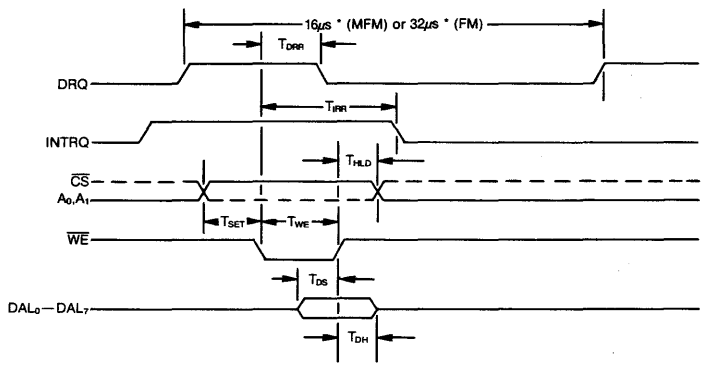
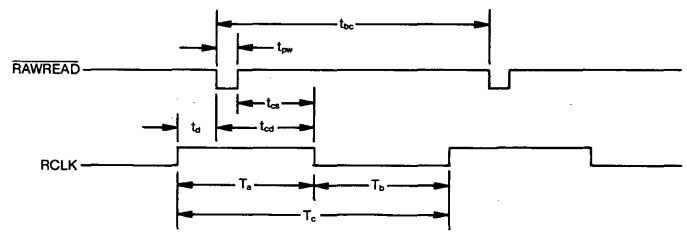
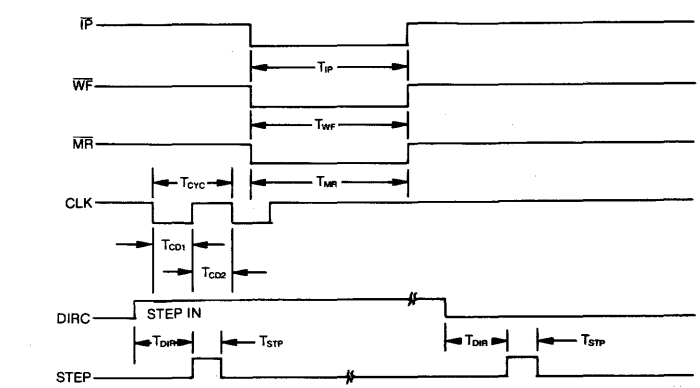


Figure 7. Disk Input Timing



Note: Pulse width on RAW READ (Pin 27) is normally 10-300 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.

Figure 8. Miscellaneous Timing



Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

IBM 3740 Format

This single-density (FM) format utilizes 128 bytes/sector. The bytes to be generated by the system MPU for use in the execution of the Write Track command are shown in Figure 9.

IBM System 34 Format

This double-density (MFM) format utilizes 256 bytes/sector. The bytes to be generated by the system MPU for use in the execution of the Write Track command are shown in Figure 10.

Non-IBM Formats

Unique (non-IBM) formats are permissible providing the following restrictions are understood.

- Sector length may only be 128, 256, 512, or 1024 bytes.
- Gap sizes must conform to Figure 11.

	DATA BYTE (hex)	NO. OF BYTES	COMMENTS
	FF	40	Gap 5 (Post Index)
	00	6	
	FC	1	Index AM
	FF	26	Gap 1
	00	6	
ONE SECTOR ①	FE	1	ID AM
	XX	1	Track Number (00-4C)
	0X	1	Side Number (00 or 01)
	XX	1	Sector Number (01-1A)
	00	1	Sector Length (128 bytes)
	F7	1	Causes 2-Byte CRC to be Written
	FF	11	Gap 2 (ID Gap)
	00	6	
	FB	1	Data AM
	E5	128	Data Field
	F7	1	Causes 2-Byte CRC to be Written
	FF	27	Part of Gap 3 (Data Gap)
	FF	247 ②	Gap 4 (Pre Index)

NOTES: 1. THIS PATTERN MUST BE WRITTEN 26 TIMES PER TRACK.
2. CONTINUE WRITING HEX FF UNTIL FDC COMPLETES SEQUENCE AND GENERATES INTRQ INTERRUPT

Figure 9. Byte Sequence for IBM 3740 Formatting

	DATA BYTE (hex)	NO. OF BYTES	COMMENTS
	4E	80	Gap 5 (Post Index)
	00	12	
	F6	3	Writes C2
	FC	1	Index AM
	4E	50	
	00	12	Gap 1
	F5	3	Writes A1
	FE	1	ID AM
	XX	1	Track Number (00-4C)
ONE SECTOR ①	0X	1	Side Number (00 or 01)
	XX	1	Sector Number (01-1A)
	01	1	Sector Length (256 Bytes)
	F7	1	Causes 2-Byte CRC to be Written
	4E	22	Gap 2 (ID Gap)
	00	12	
	F5	3	Writes A1
	FB	1	Data AM
	40	256	Data Field
	F7	1	Causes 2-Byte CRC to be Written
	4E	54	Part of Gap 3 (Data Gap)
	4E	598 ②	Gap 4 (Pre Index)

NOTES: 1. THIS PATTERN MUST BE WRITTEN 26 TIMES PER TRACK.
2. CONTINUE WRITING HEX 4E UNTIL FDC COMPLETES SEQUENCE AND GENERATES INTRQ INTERRUPT.

Figure 10. Byte Sequence for IBM System-34 Formatting

GAP	SINGLE DENSITY (FM)	DOUBLE DENSITY (MFM)	NOTE
Gap 1	16 bytes FF	16 bytes 4E	2
Gap 2	11 bytes FF 6 bytes 00	22 bytes 4F 12 bytes 00 3 bytes A1	1
Gap 3	10 bytes FF 4 bytes 00	16 bytes 4E 8 bytes 00 3 bytes A1	2
Gap 4	16 bytes FF	16 bytes 4E	2

NOTES: 1. THESE BYTES COUNTS ARE EXACT.
2. THESE BYTES COUNTS ARE MINIMUM EXCEPT FOR 3 BYTES A1, WHICH IS EXACT.

Figure 11. Gap Size Limitations

STANDARD MICROSYSTEMS CORPORATION

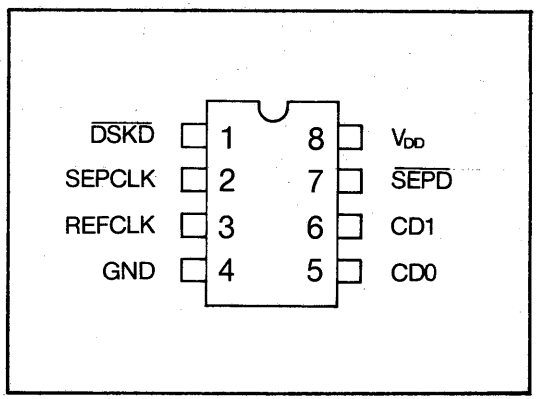
FDC 9216
FDC 9216B
μPC FAMILY

Floppy Disk Data Separator
FDDS

FEATURES

- ☐ PERFORMS COMPLETE DATA SEPARATION FUNCTION FOR FLOPPY DISK DRIVES
- ☐ SEPARATES FM OR MFM ENCODED DATA FROM ANY MAGNETIC MEDIA
- ☐ ELIMINATES SEVERAL SSI AND MSI DEVICES NORMALLY USED FOR DATA SEPARATION
- ☐ NO CRITICAL ADJUSTMENTS REQUIRED
- ☐ COMPATIBLE WITH STANDARD MICROSYSTEMS' FDC 1791, FDC 1793 AND OTHER FLOPPY DISK CONTROLLERS
- ☐ SMALL 8-PIN DUAL-IN-LINE PACKAGE
- ☐ +5 VOLT ONLY POWER SUPPLY
- ☐ TTL COMPATIBLE INPUTS AND OUTPUTS

PIN CONFIGURATION



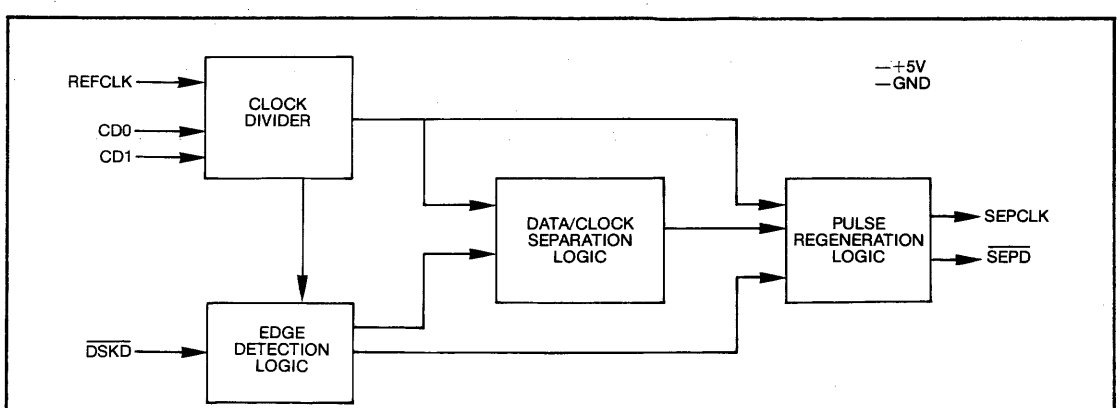
SECTION V

GENERAL DESCRIPTION

The Floppy Disk Data Separator provides a low cost solution to the problem of converting a single stream of pulses from a floppy disk drive into separate Clock and Data inputs for a Floppy Disk Controller.

The FDDS consists primarily of a clock divider, a long-term timing corrector, a short-term timing corrector, and reclocking circuitry. Supplied in an 8-pin Dual-In-Line package to save board real estate, the FDDS operates on +5 volts only and is TTL compatible on all inputs and outputs.

The FDC 9216 is available in two versions; the FDC 9216, which is intended for 5¼" disks and the FDC 9216B for 5¼" and 8" disks.

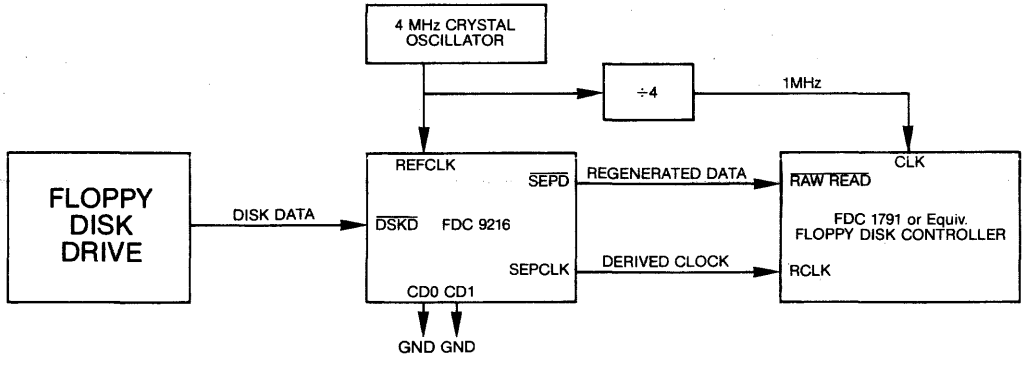


FLOPPY DISK DATA SEPARATOR BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	$\overline{\text{Disk Data}}$	$\overline{\text{DSKD}}$	Data input signal direct from disk drive. Contains combined clock and data waveform.
2	Separated Clock	SEPCLK	Clock signal output from the FDDS derived from floppy disk drive serial bit stream.
3	Reference Clock	REFCLK	Reference clock input
4	Ground	GND	Ground
5, 6	Clock Divisor	CD0, CD1	CD0 and CD1 control the internal clock divider circuit. The internal clock is a submultiple of the REFCLK according to the following table: CD1 CD0 Divisor 0 0 1 0 1 2 1 0 4 1 1 8
7	$\overline{\text{Separated Data}}$	$\overline{\text{SEPD}}$	SEPD is the data output of the FDDS
8	Power Supply	V_{DD}	+5 volt power supply

FIGURE 1
TYPICAL SYSTEM CONFIGURATION
(5¼" Drive, Double Density)



OPERATION

A reference clock (REFCLK) of between 2 and 8 MHz is divided by the FDDS to provide an internal clock. The division ratio is selected by inputs CD0 and CD1. The reference clock and division ratio should be chosen per table 1.

The FDDS detects the leading edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPARATED CLOCK output.

Separate short and long term timing correctors assure accurate clock separation.

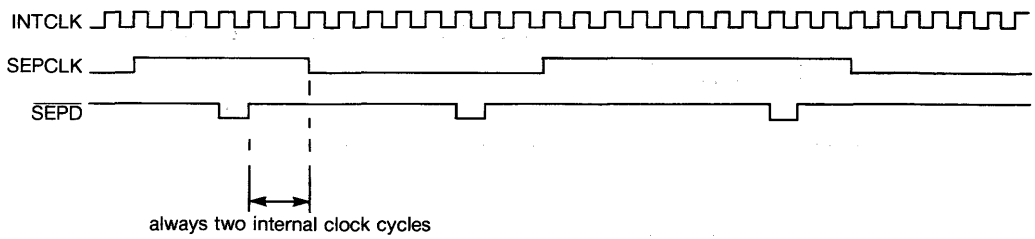
The internal clock frequency is nominally 16 times the SEPCLK frequency. Depending on the internal timing correction, the internal clock may be a minimum of 12 times to a maximum of 22 times the SEPCLK frequency.

The reference clock (REFCLK) is divided to provide the internal clock according to pins CD0 and CD1.

TABLE 1:
CLOCK DIVIDER SELECTION TABLE

DRIVE (8" or 5¼")	DENSITY (DD or SD)	REFCLK MHz	CD1	CD0	REMARKS
8	DD	8	0	0	
8	SD	8	0	1	Select either one
8	SD	4	0	0	
5¼	DD	8	0	1	Select either one
5¼	DD	4	0	0	
5¼	SD	8	1	0	
5¼	SD	4	0	1	Select any one
5¼	SD	2	0	0	

FIGURE 2



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

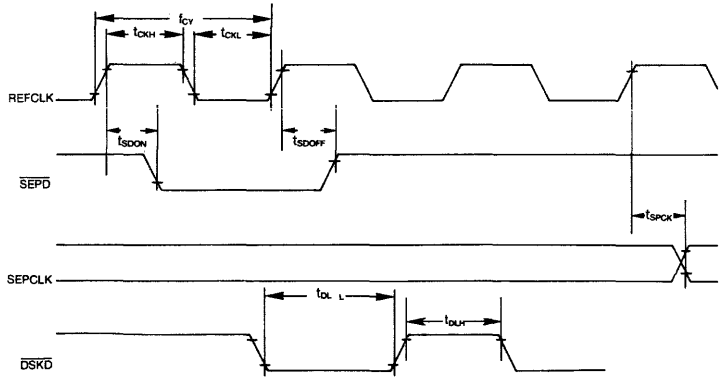
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A =0°C to 70°C, V_{DD}=+5V±5%, unless otherwise noted)

Parameter		Min.	Typ.	Max.	Units	Comments
D.C. CHARACTERISTICS						
INPUT VOLTAGE LEVELS						
Low Level V_{IL}				0.8	V	
High Level V_{IH}		2.0			V	
OUTPUT VOLTAGE LEVELS						
Low Level V_{OL}				0.4	V	I_{OL}=1.6mA
High Level V_{OH}		2.4			V	I_{OH}=−100 μA
INPUT CURRENT						
Leakage I_{IL}				10	μA	$O \le V_{IN} \le V_{DD}$
INPUT CAPACITANCE						
All Inputs				10	pF	
POWER SUPPLY CURRENT						
I_{DD}				60	mA	
A.C. CHARACTERISTICS						
Symbol						
f_{cy}	REFCLK Frequency	0.2		4.3	MHz	FDC 9216
f_{cy}	REFCLK Frequency	0.2		8.3	MHz	FDC 9216B
t_{CKH}	REFCLK High Time	50		2500	ns	
t_{CKL}	REFCLK Low Time	50		2500	ns	
t_{SDON}	REFCLK to $\overline{SEPD}$ "ON" Delay		100		ns	
t_{SDOFF}	REFCLK to $\overline{SEPD}$ "OFF" Delay		100		ns	
t_{SPCK}	REFCLK to SEPCLK Delay	100			ns	
t_{DLL}	DSKD Active Low Time	0.1		100	μs	
t_{DLH}	DSKD Active High Time	0.2		100	μs	

FIGURE 3: AC CHARACTERISTICS



STANDARD MICROSYSTEMS CORPORATION

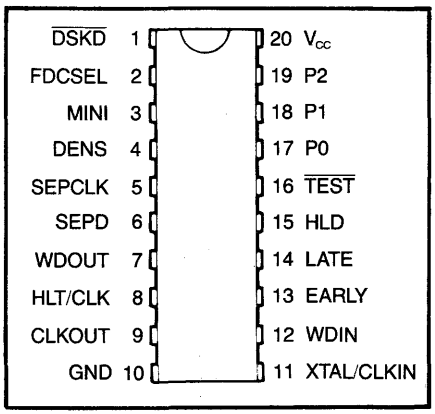
FDC 9229
FDC 9229B
FDC 9229T
FDC 9229BT

FLOPPY DISK INTERFACE CIRCUIT

FEATURES

- ☐ Digital Data Separator
  - Performs complete data separation function for floppy disk drives
  - Separates FM and MFM encoded data
  - No critical adjustments necessary
  - 5¼" and 8" compatible
- ☐ Variable Write Precompensation
- ☐ Internal Crystal Oscillator Circuit
- ☐ Track-Selectable Write Precompensation
- ☐ Retriggerable Head-Load Timer
- ☐ Compatible with the FDC 179X, 765, and other standard Floppy Disk Controllers
- ☐ COPLAMOS® n-channel MOS Technology
- ☐ Single +5 Volt Supply
- ☐ TTL Compatible

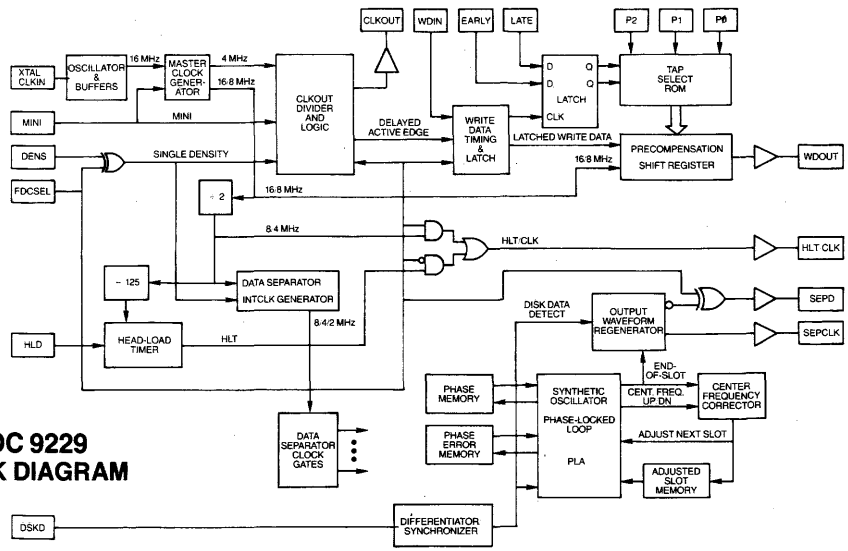
PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

The FDC 9229/B is an MOS integrated circuit designed to complement either the 179X or 765 (8272) type of floppy disk controller chip. It incorporates a digital data separator, write precompensation logic, and a head-load timer in one 0.3-inch wide 20-pin package. A single pin will configure the chip to work with either the 179X or 765 type of controller. The FDC 9229/B provides a number of different dynamically selected precompensation values so that different values may be used when writing to the inner and outer tracks of the floppy disk drive. The FDC 9229/B operates from a +5V supply and simply requires that a 16 or 8 MHz crystal or TTL-level clock be connected to the XTAL/CLKIN pin. All inputs and outputs are TTL compatible.

The FDC 9229 is available in four versions: The FDC 9229/T are intended for 5¼" disks and the FDC 9229B/T for 5¼" and 8" disks. The FDC 9229/B have an internal crystal oscillator circuit; the FDC 9229T/BT require an external clock.



FDC 9229 BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	I/O	DESCRIPTION
1	$\overline{\text{DSKD}}$	I	This input is the raw read data received from the drive. (This input is active low.)
2	FDCSEL	I	This input signal, when low, programs the FDC 9229/B for a 179X type of LSI controller. When FDCSEL is high, the FDC 9229/B is programmed for a 765 (8272) type of controller. (See fig. 4.)
3	MINI	I	The state of this input determines whether the FDC 9229/B is configured to support 8" or 5¼" floppy disk drive interfaces. It is used in conjunction with the DENS input to prescale the clock for the data separator. The state of this input also alters the CLKOUT frequency, the precompensation value, the head load delay time (when in 179X mode) and the HLT/CLK frequency (when in 765 mode). (See figs. 2, 3, and 4.)
4	DENS	I	The state of this input determines whether the FDC 9229/B is configured to support single density (FM) or double density (MFM) floppy disk drive interfaces. It is used in conjunction with the MINI input to prescale the clock for the data separator. The state of this input also alters the CLKOUT frequency when in the 765 mode. (See figs. 2, 3, and 4.)
5	SEPCLK	O	A square-wave window clock signal output derived from the $\overline{\text{DSKD}}$ input.
6	SEPD	O	This output is the regenerated data pulse derived from the raw data input ($\overline{\text{DSKD}}$). This signal may be either active low or active high as determined by FDCSEL (pin 2).
7	WDOUT	O	The precompensated WRITE DATA stream to the drive.
8	HLT/CLK	O	When in the 765 mode (FDCSEL high), this output is the master clock to the floppy disk controller. When in the 179X mode, this signal goes high after the head load delay has occured following the HLD input going high. This output is retriggerable. (See fig. 3.)
9	CLKOUT	O	This signal is the write clock to the floppy disk controller. Its frequency is determined by the state of the MINI, DENS, and FDCSEL input pins. (See fig. 3.)
10	GND		Ground
11	XTAL/CLKIN	I	This input is for direct connection to a 16 MHz or 8 MHz crystal (FDC 9229/B only). The other pin of the crystal is grounded. XTAL/CLKIN may alternatively be connected to a single-phase TTL-level clock. The FDC 9229T and BT require an external TTL-level clock.
12	WDIN	I	The write data stream from the floppy disk controller.
13	EARLY	I	When this input is high, the current WRITE DATA pulse will be written early to the disk.
14	LATE	I	When this input is high, the current WRITE DATA pulse will be written late to the disk. When both EARLY and LATE are low, the current WRITE DATA pulse will be written at the nominal position.
15	HLD	I	This input is only used in 179X mode. A high level at this input causes a high level on the HLT/CLK output after the specified head-load time delay has elapsed. The delay is selected by the state of the MINI output. (See fig. 3.)
16	$\overline{\text{TEST}}$	I	This input (when low) decreases the head-load time delay and initializes the data separator. This pin is for test purposes only. This input has an internal pull-up resistor and should be tied high or disconnected for normal operation.
17	P0	I	P2-P0 select the amount of precompensation applied to the write data. (See fig. 2.)
18	P1	I	
19	P2	I	
20	V_{CC}		+5 VOLT SUPPLY

Data Separator

The XTAL/CLKIN input clock is internally divided by the FDC 9229/B to provide an internal clock. The division ratio is selected by the FDCSEL, MINI and DENS inputs depending on the type of drive used. (See fig. 1.)

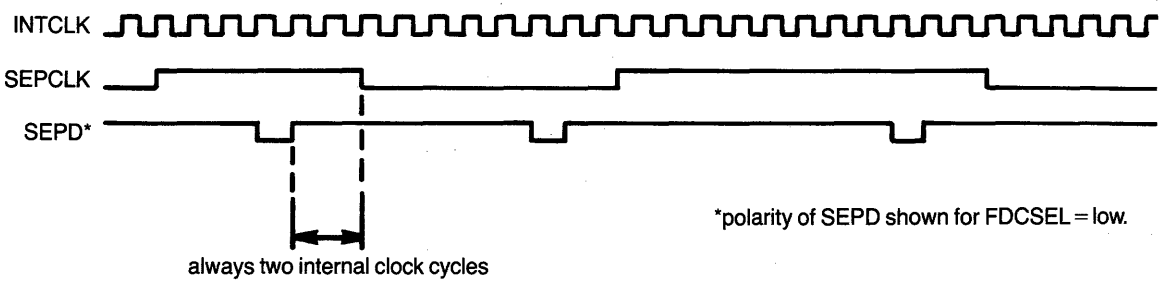
The FDC 9229/B detects the leading (negative) edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPCLK output.

Separate short- and long-term timing correctors assure accurate clock separation.

The SEPCLK frequency is nominally 1/16 the internal clock frequency. Depending on the internal timing correction, the duration of any SEPCLK half-cycle may vary from a nominal of 8 to a minimum of 6 and a maximum of 11 internal clock cycles.

INPUTS			DIVISOR
FDCSEL	DENS	MINI	f(XTAL/CLKIN)/f(INTCLK)
0	0	0	2
0	0	1	4
0	1	0	4
0	1	1	8
1	0	0	4
1	0	1	8
1	1	0	2
1	1	1	4

FIG. 1



Precompensation

The desired precompensation delay is determined by the state of the P0, P1 and P2 inputs of the FDC 9229/B as per fig. 2. Logic levels present on these pins may be changed dynamically as long as the inputs are stable during the time the floppy disk controller is writing to the drive and the inputs meet the minimum setup time with respect to the write data from the floppy disk controller.

MINI	P2	P1	P0	PRECOMP VALUE
0	0	0	0	0 ns
0	0	0	1	62.5 ns
0	0	1	0	125 ns
0	0	1	1	187.5 ns
0	1	0	0	250 ns
0	1	0	1	250 ns
0	1	1	0	312.5 ns
0	1	1	1	312.5 ns
1	0	0	0	0 ns
1	0	0	1	125 ns
1	0	1	0	250 ns
1	0	1	1	375 ns
1	1	0	0	500 ns
1	1	0	1	500 ns
1	1	1	0	625 ns
1	1	1	1	625 ns

NOTE: All values shown are obtained with a 16 MHz reference clock. Multiply pre-comp values by two for 8 MHz operation.

FIG. 2 WRITE PRECOMPENSATION VALUE SELECTION

Head Load Timer

The head load time delay is either 40 ms or 80 ms, depending on the state of MINI. (See fig. 3.) The purpose of this delay is to ensure that the head has enough time to engage properly. The head load timer is only used in the 179X mode; it is non-functional in the 765 mode.

The FDC 179X initiates the loading of the floppy disk drive head by setting HLD high. The controller then waits the programmed amount of time until the HLT signal from the FDC 9229/B goes high before starting a read or write operation.

INPUTS			OUTPUTS	
FDCSEL	DENS	MINI	CLKOUT	HLT/CLK
0	0	0	2 MHz	40 ms*
0	0	1	1 MHz	80 ms*
0	1	0	2 MHz	40 ms*
0	1	1	1 MHz	80 ms*
1	0	0	500 KHz	8 MHz
1	0	1	250 KHz	4 MHz
1	1	0	1 MHz	8 MHz
1	1	1	500 KHz	4 MHz

NOTE: All values shown are obtained with a 16 MHz reference clock. Divide all frequencies and multiply all periods by two for 8 MHz operation.

*May be mask programmed at factory to any value from 1 to 512 ms in 15.625 μs increments (MINI low) or 1 to 1024 ms in 31.25 μs increments (MINI high).

FIG. 3 CLOCK AND HEAD LOAD TIME DELAY SELECTION

INPUTS			FLOPPY DISK DRIVE TYPE	FLOPPY DISK DRIVE DENSITY	FLOPPY DISK CONTROLLER TYPE
FDCSEL	DENS	MINI			
0	0	0	8" DRIVE	DOUBLE	179X
0	0	1	5¼" DRIVE	DOUBLE	179X
0	1	0	8" DRIVE	SINGLE	179X
0	1	1	5¼" DRIVE	SINGLE	179X
1	0	0	8" DRIVE	SINGLE	765 (8272)
1	0	1	5¼" DRIVE	SINGLE	765 (8272)
1	1	0	8" DRIVE	DOUBLE	765 (8272)
1	1	1	5¼" DRIVE	DOUBLE	765 (8272)

FIG. 4 FLOPPY DISK DRIVE AND CONTROLLER SELECTION

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55° to +150°C
Lead Temperature (soldering, 10 sec.)	+300°C
Positive Voltage on any I/O Pin, with respect to ground	+8.0V
Negative Voltage on any I/O Pin, with respect to ground	−0.3V
Power Dissipation	0.75W

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ±5%)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
DC CHARACTERISTICS					
INPUT VOLTAGE					
Low Level V_{IL}	−0.3		0.8	V	Except XTAL/CLKIN
High Level V_{IH}	2.0		(V_{CC})	V	
XTAL/CLKIN INPUT VOLTAGE					
AC Amplitude	1.0			V_{P-P}	XTAL/CLKIN only; input is
Instantaneous voltage	−0.3		(V_{CC})	V	AC-coupled.
OUTPUT VOLTAGE					
Low Level V_{OL}			0.4	V	I_{OL} = 1.6 mA except HLT/CLK
					I_{OL} = 0.4 mA, HLT/CLK only
High Level V_{OH}	2.4			V	I_{OH} = −100 µA except HLT/CLK
					I_{OH} = −400 µA, HLT/CLK only
POWER SUPPLY CURRENT					
I_{CC}			100	mA	
INPUT LEAKAGE CURRENT					
I_{IL}			10	µA	V_{IN} = 0 to V_{CC}
INPUT CAPACITANCE			10	pF	Except CLKIN
C_{IN}			25	pF	CLKIN only

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ±5%

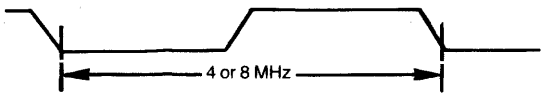
PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
AC ELECTRICAL CHARACTERISTICS	(All times assume XTAL/CLKIN = 16 MHz unless otherwise specified)				
XTAL/CLKIN frequency	3.95	16	16.2	MHz	FDC 9229B
	3.95	8	8.1	MHz	FDC 9229
XTAL/CLKIN DUTY CYCLE	25		75	%	
t_{clkoh}	465	500	515	ns	FDCSEL = low; MINI = high.
	215	250	265	ns	FDCSEL = low; MINI = low.
	90	125	140	ns	FDCSEL = high.
t_{wdo}	280	312.5	350	ns	
t_d	50		400	ns	
t_{dNEC}	0		400	ns	
t_{wdE}		562.5		ns	
t_{wdN}		precomp value			See fig. 2.
t_{wdL}		2 x precomp value			See fig. 2.
t_s	1.0			µs	

CRYSTAL SPECIFICATIONS

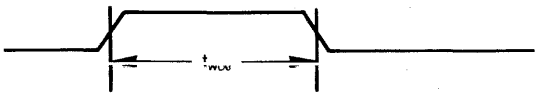
Frequency (8" Disk Drive) 16 MHz, at Cut
(5¼" Disk Drive) 8 MHz, at Cut
Holder Preferred HC − 18/V
Frequency and stability tolerance ± .05% from 0°C to 70°C
Series Resistance 50 ohm max

AC TIMING CHARACTERISTICS

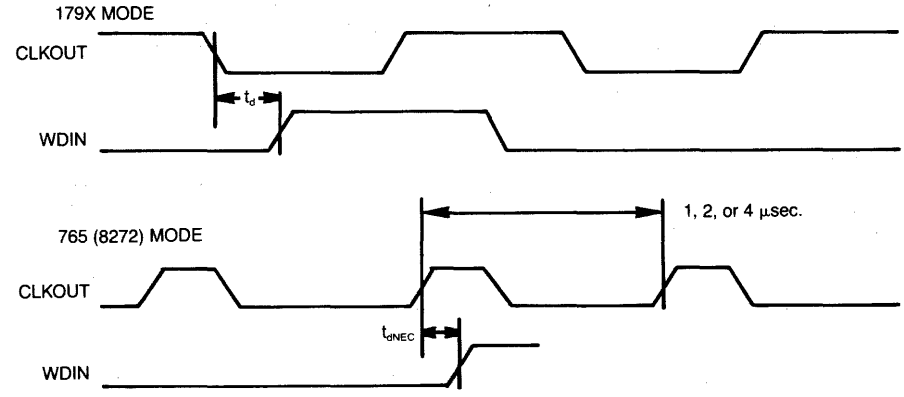
HLT/CLK (765 MODE)



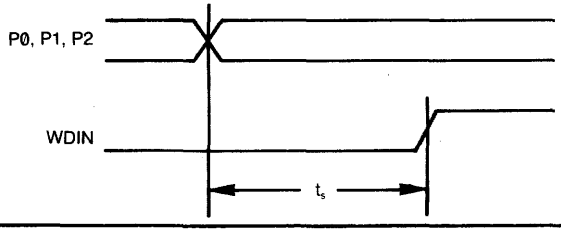
WDOUT PULSE WIDTH



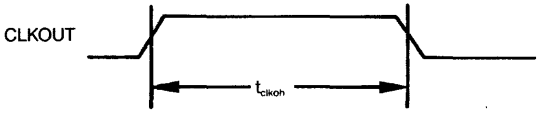
CLKOUT VS. WDIN TIMING



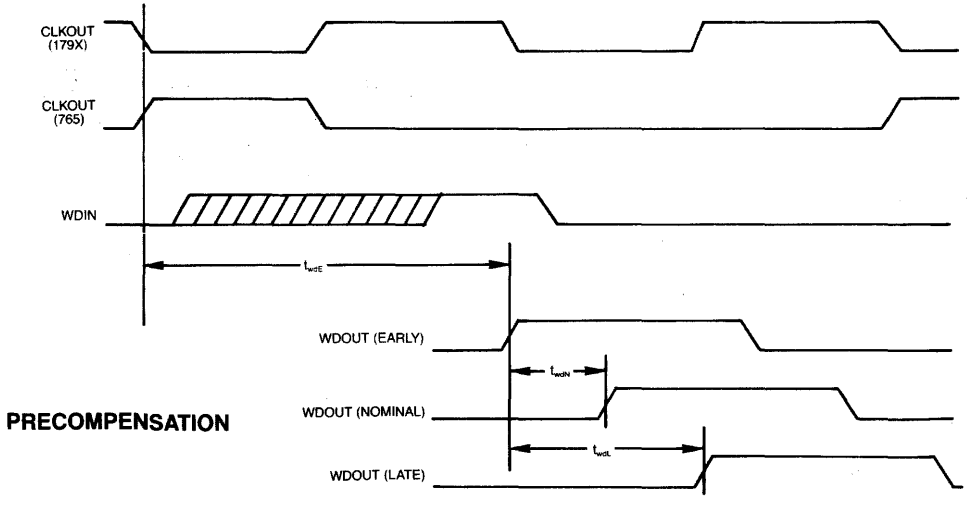
SET-UP TIME P0, P1 AND P2 TO WDIN



CLKOUT

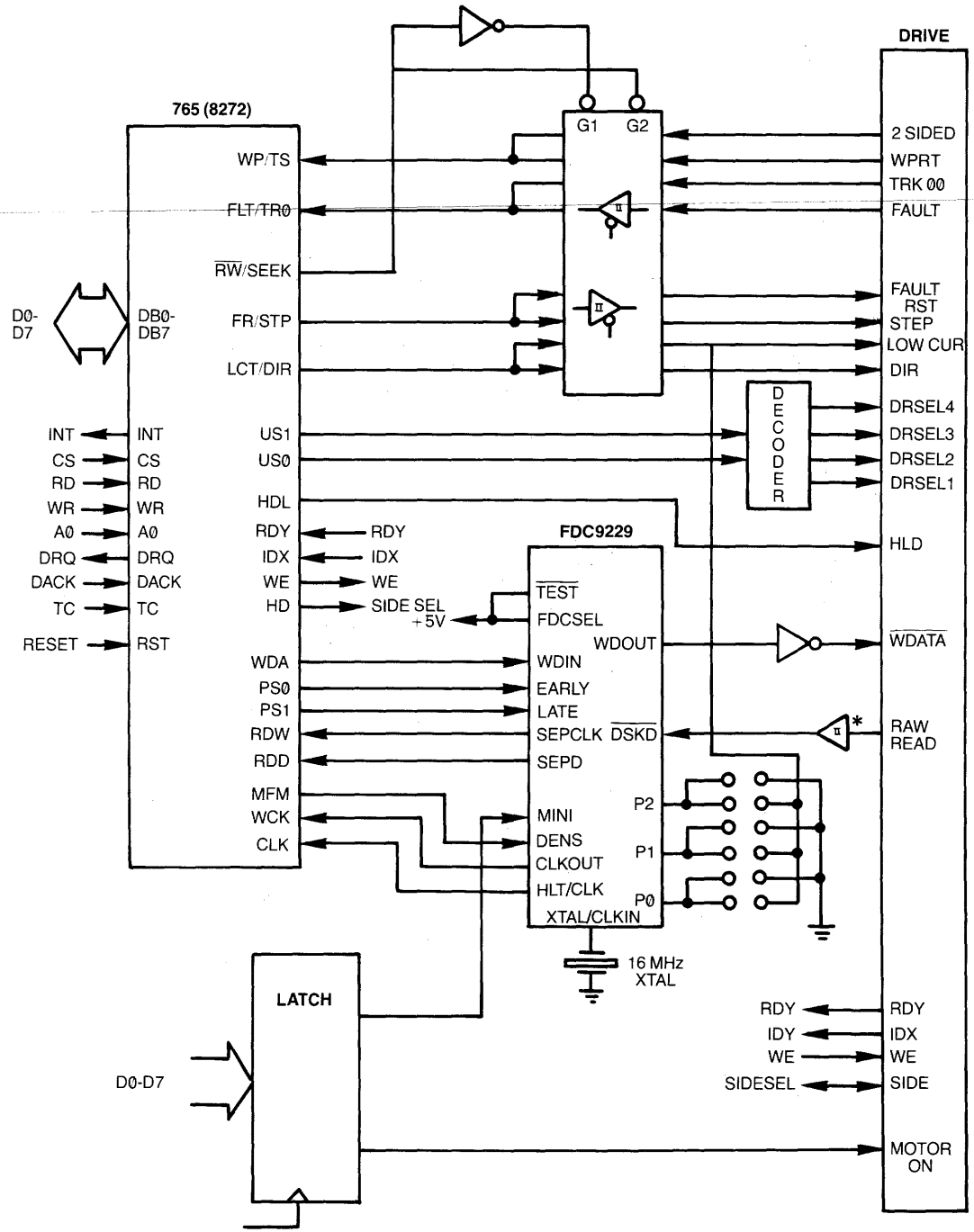


PRECOMPENSATION



Ref. to Fig. 2 for t_p (precompensation) value

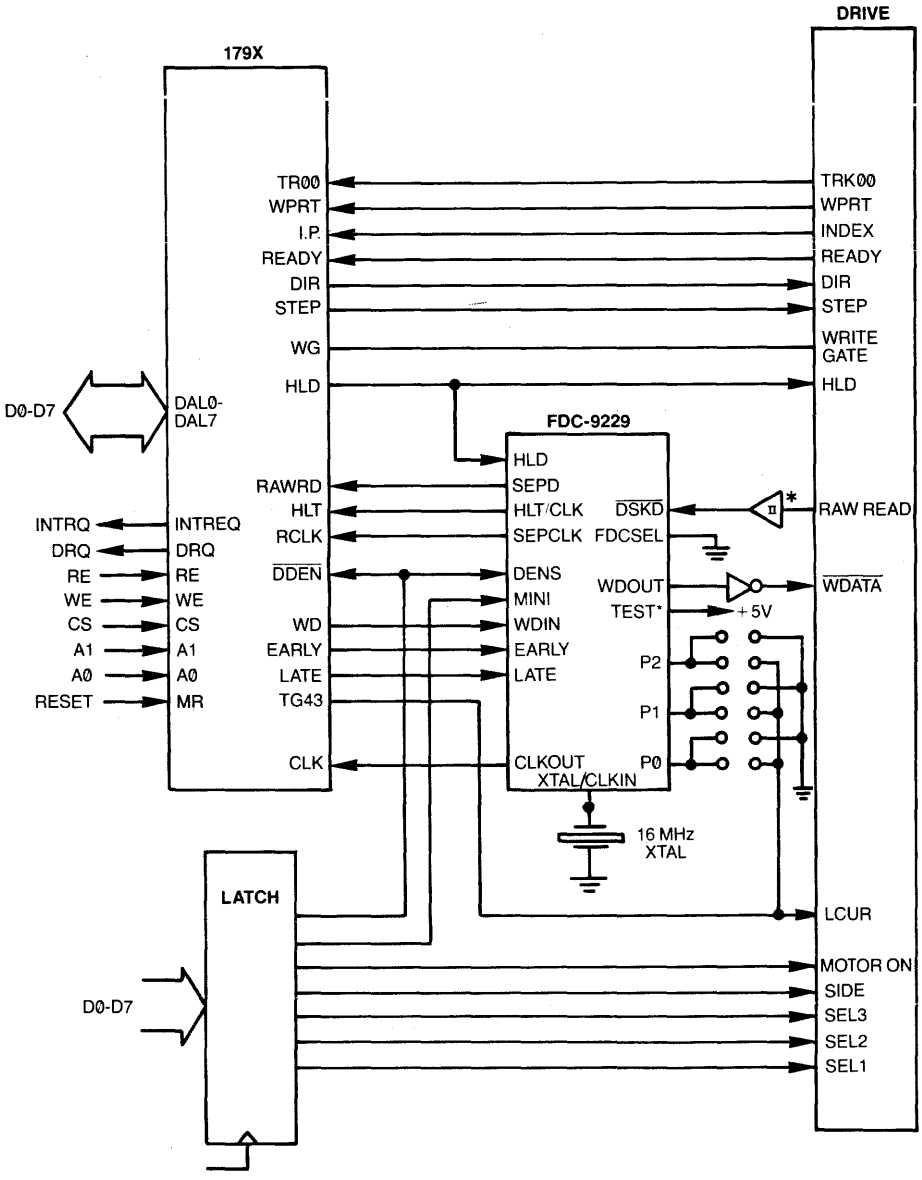
TYPICAL SYSTEM IMPLEMENTATION—765 (8272) FDC



*The FDC9229/B, as all other NMOS integrated circuits, presents a high impedance on all inputs.

To avoid soft errors caused by transmission line effects and noise where there is long cabling between the floppy disk drive and the controller board, the use of a (non-inverting) TTL schmidt-trigger input gate or bus transceiver is recommended at the DSKD input to the FDC9229/B.

TYPICAL SYSTEM IMPLEMENTATION—179X FDC



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To avoid soft errors caused by transmission line effects and noise where there is long cabling between the floppy disk drive and the controller board, the use of a (non-inverting) TTL schmidt-trigger input gate or bus transceiver is recommended at the DSKD input to the FDC9229/B.

STANDARD MICROSYSTEMS CORPORATION

HDC 7261D

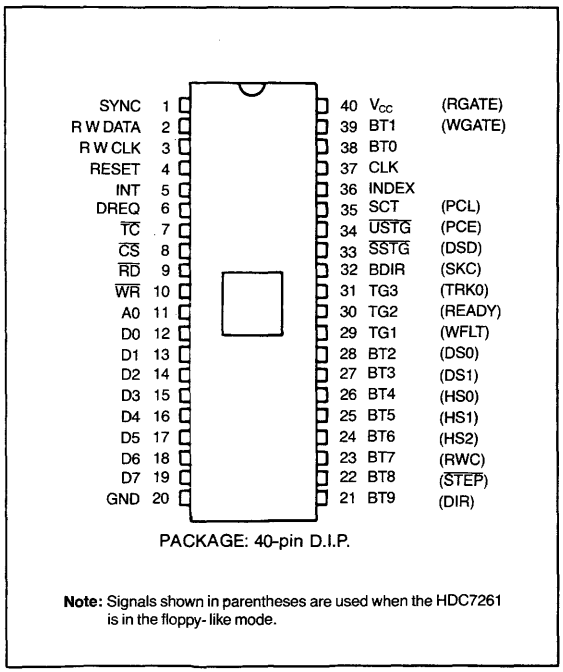
PRELIMINARY

Hard Disk Controller

FEATURES

- ☐ Flexible interface to various types of Hard Disk Drives
- ☐ Programmable Track Format
- ☐ Controls up to 8 Drives
- ☐ Parallel Seek Operation Capability
- ☐ Multi-sector and Multi-track Transfer Capability
- ☐ Data Scan and Data Verify Capability
- ☐ High Level Commands, Including:
  - READ DATA
  - READ ID
  - WRITE DATA
  - WRITE ID
  - SCAN DATA
  - VERIFY DATA
  - VERIFY ID
  - CHECK
  - SEEK (Normal or Buffered)
  - RECALIBRATE (Normal or Buffered)
  - READ DIAGNOSTIC (SMD Only)
  - SPECIFY
  - SENSE INTERRUPT STATUS
  - SENSE DRIVE STATUS
  - DETECT ERROR
- ☐ NRZ, FM, or MFM Data Format
- ☐ Maximum Data Transfer Rate: 12MHz
- ☐ Error Detection and Correction Capability
- ☐ Simple I/O Structure: Compatible with Most Microprocessors
- ☐ All Inputs and Outputs except Clock Pins are TTL-Compatible (Clock Pins Require Pull-up)
- ☐ Single +5V Power Supply
- ☐ 40-Pin Dual-in-line Package
- ☐ COPLAMOS® n-Channel Silicon Gate Technology

PIN CONFIGURATION



PACKAGE: 40-pin D.I.P.

Note: Signals shown in parentheses are used when the HDC7261 is in the floppy-like mode.

SECTION V

GENERAL DESCRIPTION

The HDC7261 Hard Disk Controller is an intelligent microprocessor peripheral designed to control a number of different types of disk drives. It is capable of supporting either hard-sector or soft-sector disks and provides all control signals that interface the controller with either SMD disk interfaces or Seagate floppy-like drives. Its sophisticated instruction set minimizes the software overhead for the host microprocessor. By using the DMA controller, the microprocessor needs only to load a few command bytes into the HDC7261 and all the data transfers associated with read, write, or format operations are done by the HDC7261 and the DMA controller. Extensive error reporting, verify commands, ECC, and CRC data error checking assure reliable controller operation. The HDC7261 provides internal address mark detection, ID verification, and CRC or ECC checking and verification. An eight-byte FIFO is used for loading command parameters and obtaining command results. This makes the structuring of software drivers a simple task. The FIFO is also used for buffering data during DMA read/write operations.

STANDARD MICROSYSTEMS CORPORATION

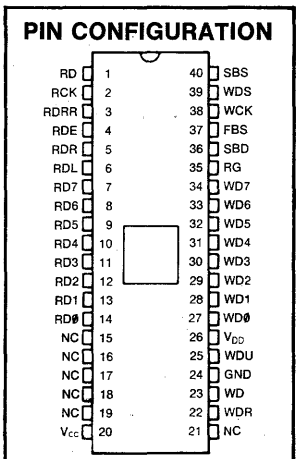
FDC3400
μPC FAMILY

Floppy Disk Hard Sector Data Handler HSDH

FEATURES

- ☐ Hard-Sectored Operation — performs all data operations
- ☐ Single or Double Density Operation — recording code independent
- ☐ Minifloppy or Standard Floppy compatible
- ☐ Programmable Sync Byte
- ☐ Internal Sync Byte Detection and Byte Framing
- ☐ Fully Double Buffered
- ☐ Data Overrun/Underrun Detection
- ☐ Dual Disk Operation — Write on one disk drive while simultaneously reading from another
- ☐ Tri-State Output Bus for processor compatibility
- ☐ TTL Compatible Inputs and Outputs

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

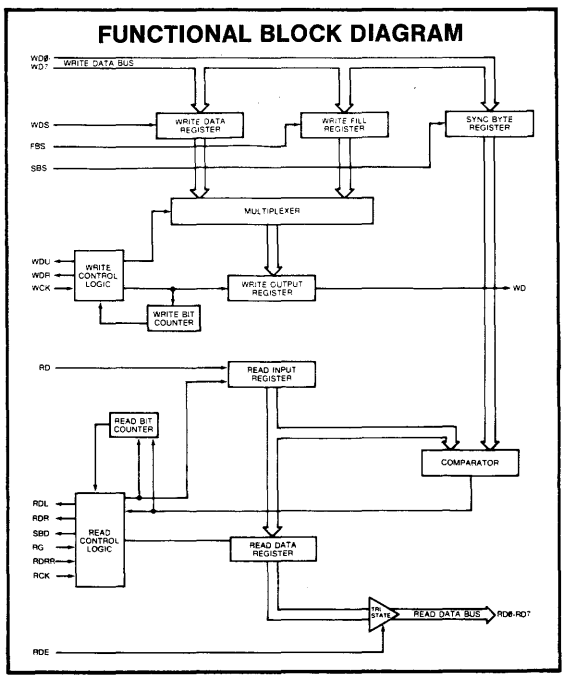
GENERAL DESCRIPTION

The FDC3400 is an MOS integrated circuit which simplifies the data interface between a processor and a floppy disk drive. During a write operation, the HSDH receives data from the processor and shifts it out bit-serially to the floppy disk data encoding logic. Similarly, during a read operation the HSDH receives a bit-serial stream of read data from the floppy disk data separator, establishes byte synchronization by detecting the sync byte, and transfers data on a byte by byte basis to the processor.

The HSDH detects data overrun and underrun conditions and indicates these conditions on its status lines. A data underrun causes write data to be written onto the disk from a special programmable fill register until new data is entered into the write data buffer or until the write operation is ended.

Separate read and write data registers permit simultaneous read and write operations on two different drives for enhanced system throughput. The HSDH is fully double buffered and all inputs and outputs are TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



SECTION VI

DESCRIPTION OF OPERATION

Prior to reading or writing on the disk, the read/write head must be positioned and loaded onto the desired track.

Write Operation

The Write Clock is set at the desired bit rate (usually 125, 250, or 500KHz), and the desired fill byte is written into the Write Fill Register. After the external logic makes the write enable to the drive active, the first byte to be written should be loaded into the Write Data Register. This byte is then loaded into the Write Output Register and shifted out bit serially to the external write encoding logic. The first bit shifted out of each byte is the LSB. Whenever a byte is transferred from the Write Data Register to the Write Output Register, Write Data Request becomes active and requests another byte from the processor. If new data is not loaded into the Write Data Register before the Write Output Register becomes empty, then the Write Output Register is loaded with data from the Write Fill Register and the Write Data Underrun status line is set. WDU is reset the next time WDS is pulsed. At the end of the write operation, the processor should return the external write enable line to an inactive state.

Read Operation

The Read Clock is set at the desired bit rate (usually 125, 250, or 500KHz) and the desired sync byte is loaded into the Sync Byte Register. When the processor wishes to read a sector of data it causes a transition on the Read Gate input to set the read logic into a sync byte search mode. In the search mode the serial read data bit stream is examined on a bit by bit basis until a sync byte is found. A sync byte is found, by definition, when the contents of the Sync Byte Register and the Read Input Register are identical. When this occurs the Sync Byte Detected output is set high. This byte is then loaded into the Read Data Register and the read logic is set into the byte mode. In this mode each byte read is loaded into the Read Data Register and Read Data Request is made active high for each byte. The processor responds to each Read Data Request by enabling the output bus with Read Data Enable, reading the data byte from the Read Data Register, and resetting Read Data Request by pulsing Read Data Request Reset. If the processor fails to respond to Read Data Request within one byte time, the Read Data Lost status line is set. When the processor has read the required amount of data it may reset Read Gate to an inactive-high level.

System Operation — Additional Features

Automatic Sector Fill

In some applications, such as the end of a logical file, the system buffer may contain less than a full sector of data. In this case the processor need supply only this data to the FDC3400. The FDC3400 will then underrun, setting the Write Data Underrun Status line and thereby causing the remainder of the sector to fill with bytes taken from the Write Fill Register. This operation continues until the processor returns the disk's write enable signal to an inactive level.

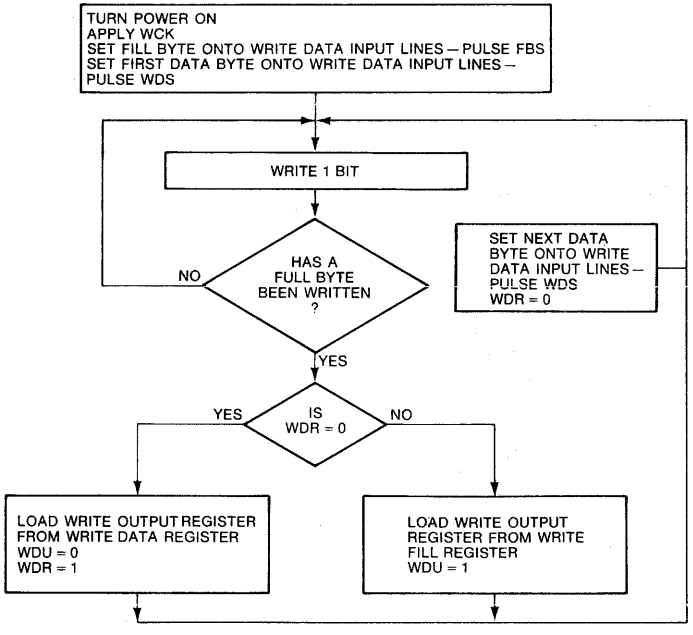
Byte Search

After byte synchronization has been established during a read operation, the processor may load a different byte into the Sync Byte Register. Whenever that byte occurs in the data being read, the Sync Byte Detected status line will go high. This feature permits the processor to search for the occurence of a specific byte while reading a sector.

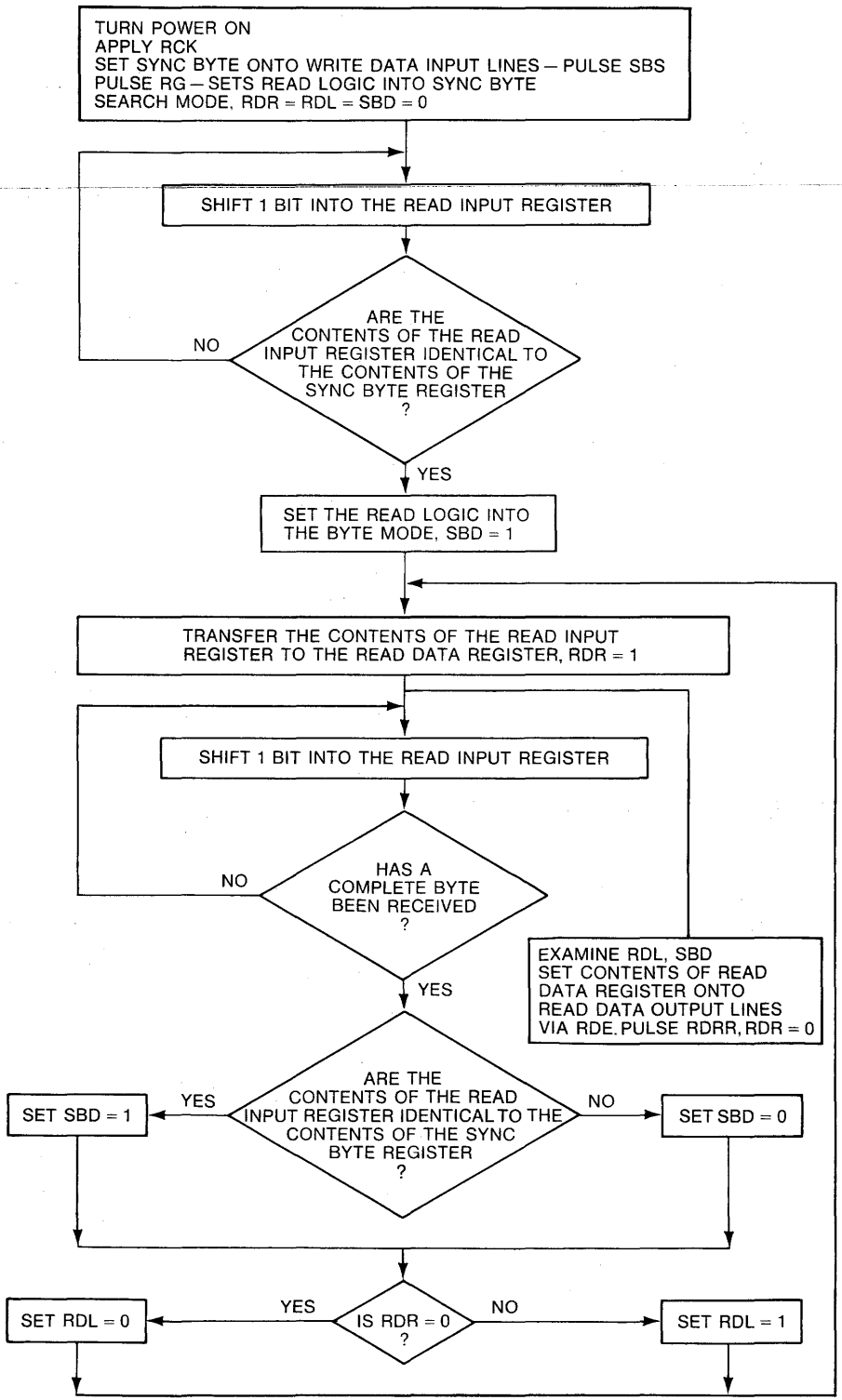
Multiple Byte Synchronization

Some systems use two or more contiguous sync bytes to establish byte synchronization. For these applications, the number of Read Data Requests received while Sync Byte Detected remains active-high may be counted by the processor to establish valid synchronization.

FLOW DIAGRAM — WRITE DATA



FLOW DIAGRAM — READ DATA



DESCRIPTION OF PIN FUNCTIONS

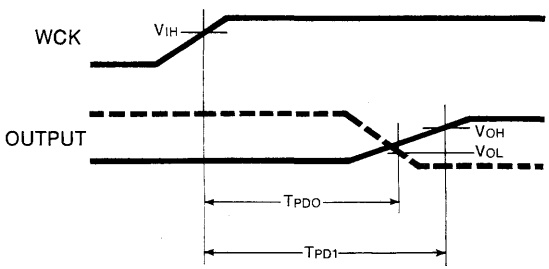
PIN NO.	SYMBOL	NAME	FUNCTION
1	RD	Read Data	The Read Data input accepts the serial data stream from the floppy disk data separator.
2	RCK	Read Clock	The negative-going edge of the Read Clock input shifts Read Data into the Read Input Register.
3	RDRR	Read Data Request Reset	An active-high pulse input on the Read Data Request Reset input resets the RDR output to a low level.
4	RDE	Read Data Enable	An active-high level on the Read Data Enable line gates the outputs of the Read Data Register onto the Read Data Output lines.
5	RDR	Read Data Request	The Read Data Request output is made active-high when an assembled byte is transferred from the Read Input Register to the Read Data Register.
6	RDL	Read Data Lost	The Read Data Lost output is made active-high, if the byte presently in the Read Data Register is not read (RDR not reset) by the processor before the next byte is loaded into the Read Data Register.
7-14	RD7-RDØ	Read Data Output	When enabled by RDE the tri-state Read Data Output lines present the data in the Read Data Register to the processor. When RDE is inactive-low the RD7-RDØ lines are held at a high-impedance state.
15-19	NC		Not Connected
20	V_{CC}	Power Supply	+5 volt supply
21	NC		Not Connected
22	WDR	Write Data Request	The Write Data Request output is made active-high when the Write Data Register becomes empty and requires a data byte. It is reset to a low level when WDS occurs to load the Write Data Register. If WDR is not serviced by the time the next byte is required by the Write Output Register, the byte stored in the Write Fill Register is written onto the disk and the WDU line is made active high.
23	WD	Write Data	The Write Data output presents the serial stream of data to the external write data encoder. Each byte is normally provided from the Write Data Register provided that a WDS pulse occurs during the presently written byte. If WDS is not pulsed, the next byte to be written will be extracted from the Write Fill Register.
24	GND	Ground	Ground
25	WDU	Write Data Underrun	The Write Data Underrun output is set active-high when the processor fails to respond to the WDR signal within one byte time. When WDU occurs the data written on the disk is extracted from the Write Fill Register. This line is reset when WDS is pulsed.
26	V_{DD}	Power Supply	−12 volt supply
27-34	WDØ-WD7	Write Data Input	The Write Data Input lines present information to the Write Data Register, the Write Fill Register, and the Sync Byte Register under control of their respective strobes. The strobes operate independently of each other. The LSB should always be placed on WDØ.
35	RG	Read Gate	This input should be pulsed to a high-level after power turn on to reset RDR, SBD, and RDL to an inactive-low level. The high-to-low transition of RG sets the read logic into the sync byte search mode. In this mode the serial Read Data stream is examined on a bit by bit basis until a sync byte is found. A sync byte is found by definition when the contents of the Sync Byte Register and the Read Input Register are identical. When this occurs the SBD output is set active-high. The sync byte just read is then transferred into the Read Data Register; RDR is set high, and the read logic is set into the byte mode. In this mode each byte read is transferred into the Read Data Register.
36	SBD	Sync Byte Detected	The Sync Byte Detected output is set active-high each time the byte loaded into the Read Data Register is identical to the byte in the Sync Byte Register. This output is reset low the next time the Read Data Register is loaded with a byte which is not a sync byte.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
37	FBS	Fill Byte Strobe	The Fill Byte Strobe is an active-high input strobe which loads the byte on the WDØ-WD7 lines into the Write Fill Register.
38	WCK	Write Clock	Each positive-going edge of this clock shifts one bit out of the Write Output Register onto WD.
39	WDS	Write Data Strobe	The Write Data Strobe is an active-high input strobe which loads the byte on the WDØ-WD7 lines into the Write Data Register.
40	SBS	Sync Byte Strobe	The Sync Byte Strobe is an active-high input strobe which loads the byte on the WDØ-WD7 lines into the Sync Byte Register.

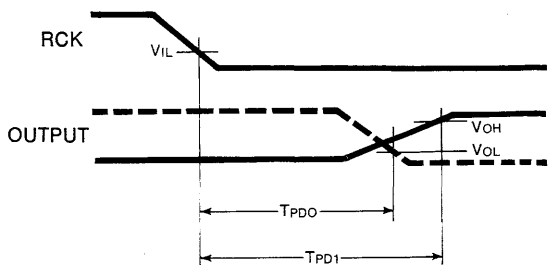
ADDITIONAL TIMING INFORMATION
(Typical Propagation Delays)

WRITE DATA

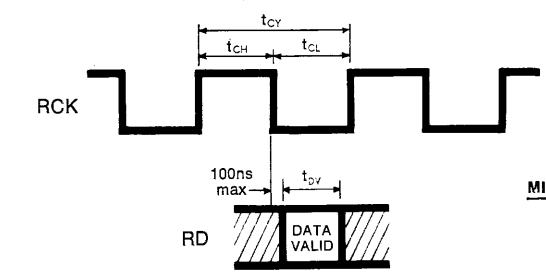


OUTPUT	T_{PDO}	T_{PD1}	UNITS
WDR	NA	2.0	µS
WDU	1.0	1.5	µS
WD	1.0	1.0	µS

READ DATA

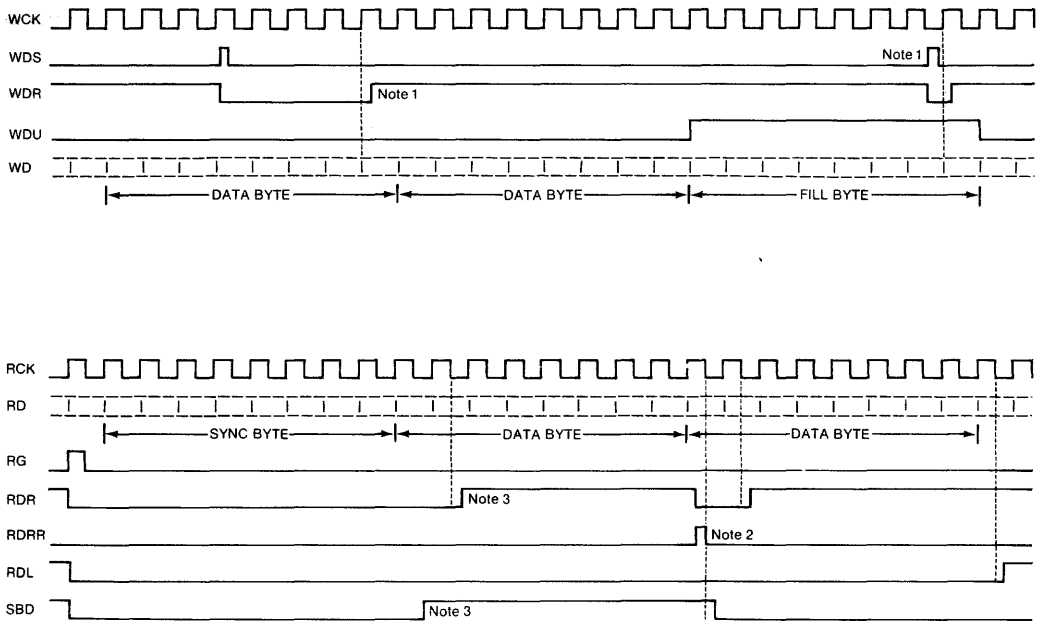


OUTPUT	T_{PDO}	T_{PD1}	UNITS
RDR	NA	1.5	µS
RDL	2.0	2.5	µS
SBD	2.0	2.5	µS
RDØ-RD7	2.5	2.5	µS



MIN. TIMING	FDC3400	FDC3400-1	UNITS
t_{CY}	4.0	2.0	µS
t_{CH}	1.0	0.5	µS
t_{CL}	2.0	1.0	µS
t_{DV}	1.4	0.9	µS

HSDH TIMING DIAGRAM



NOTE 1
The Write Output Register is loaded with the next byte at the positive clock transition corresponding to the leading edge of the last bit of the current byte on the WD output. WDR is set high approximately two microseconds after this clock transition. If it is desired that the next byte be extracted from the Write Data Register the leading edge of the WDS should occur at least one microsecond prior to this clock transition.

NOTE 2
In order to avoid an RDL indication the leading edge of the RDRR pulse should occur at least one microsecond prior to the negative clock transition corresponding to the center of the first bit after the last bit of the previous byte on the RD input.

NOTE 3
The RDL, SBD and RD0-RD7 output are set to their correct levels approximately two microseconds after the negative clock transition corresponding to the center of the first bit after the last bit of the previous byte on the RD input. The RDR output is set high at the next negative clock transition.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Load Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, V_{CC} ..... +0.3V
Negative Voltage on any Pin, V_{CC} ..... −25V

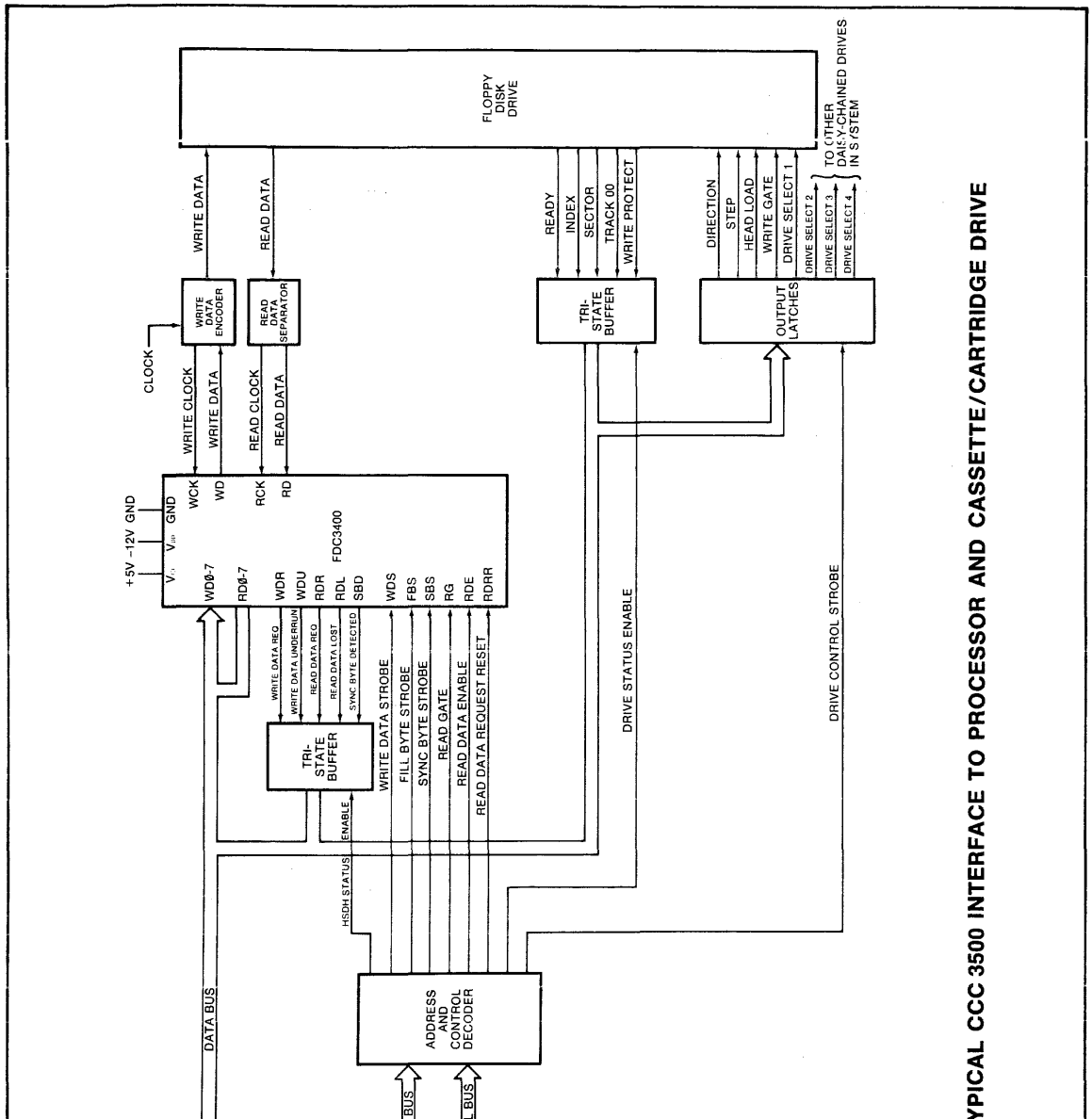
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±5% V_{DD} = −12V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Conditions
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}	V_{DD}		0.8	V	
High-level, V_{IH}	V_{CC}-1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}		0.2	0.4	V	I_{OL} = 1.6mA
High-level, V_{OH}	2.4	4.0		V	I_{OH} = −100μA
INPUT CURRENT					
Low-level, I_{IL}			1.6	mA	See note 1
OUTPUT CURRENT					
Leakage, I_{LO}			-1	μA	RDE = V_{IL}, 0 ≤ V_{OUT} ≤ +5V
Short circuit, I_{OS}**			10	mA	V_{OUT} = 0V
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pF	V_{IN} = V_{CC}, f = 1MHz
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pF	RDE = V_{IL}, f = 1MHz
POWER SUPPLY CURRENT					
I_{CC}			28	mA	All outputs = V_{OH}
I_{DD}			28	mA	
A.C. CHARACTERISTICS					T_A = +25°C
CLOCK FREQUENCY	DC		250	KHz	RCK, WCK
	DC		500	KHz	RCK, WCK, FDC3400-1
PULSE WIDTH					
Clock	1			μs	RCK, WCK
	0.5			μs	RCK, WCK, FDC3400-1
Read Gate	1			μs	RG
Write Data Strobe	200			ns	WDS
Fill Byte Strobe	200			ns	FBS
Sync Byte Strobe	200			ns	SBS
Read Data Request Reset	200			ns	RDRR
INPUT SET-UP TIME					
Write Data Inputs	0			ns	WDØ-WD7
INPUT HOLD TIME					
Write Data Inputs	0			ns	WDØ-WD7
STROBE TO OUTPUT DELAY					Load = 20pf + 1 TTL input
Read Data Enable		180	250	ns	RDE: T_{PD1}, T_{PD0}
OUTPUT DISABLE DELAY		100	250	ns	RDE

**Not more than one output should be shorted at a time.

NOTES:
1. Under steady state condition no current flows for TTL or MOS interfacing.
   A switching current of 1.6mA maximum flows during a high to low transition of the input.
2. The tri-state output has 3 states:
   1) low-impedance to V_{CC}
   2) low-impedance to GND
   3) high-impedance OFF ≅ 10M ohms
   The OFF state is controlled by the RDE input.



TYPICAL CCC 3500 INTERFACE TO PROCESSOR AND CASSETTE/CARTRIDGE DRIVE

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 TWX: 510-227-8898
We keep ahead of our competition so you can keep ahead of yours.

STANDARD MICROSYSTEMS CORPORATION

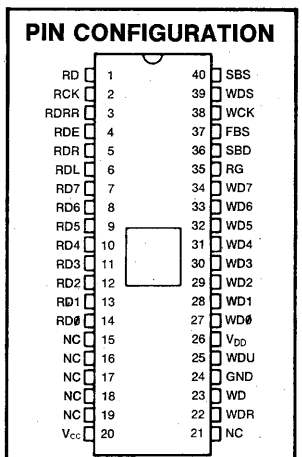
CCC 3500
μPC FAMILY

Cassette/Cartridge Data Handler CCDH

FEATURES

- ☐ Facilitates Magnetic Tape Cassette or Cartridge to Processor Interfacing
- ☐ Performs All Data Operations
- ☐ Up to 250K bps Data Transfer Rate
- ☐ Recording Code Independent
- ☐ Compatible with Standard and Mini Cassettes
- ☐ Compatible with Standard and Mini 3M-type Cartridges
- ☐ Read-While-Write Operation for Write Verification In Dual Gap Head Systems
- ☐ Programmable Sync Byte
- ☐ Internal Sync Byte Detection and Byte Framing
- ☐ Fully Double Buffered
- ☐ Data Overrun/Underrun Detection
- ☐ Tri-State Output Bus for Processor Compatibility
- ☐ TTL Compatible Inputs and Outputs

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

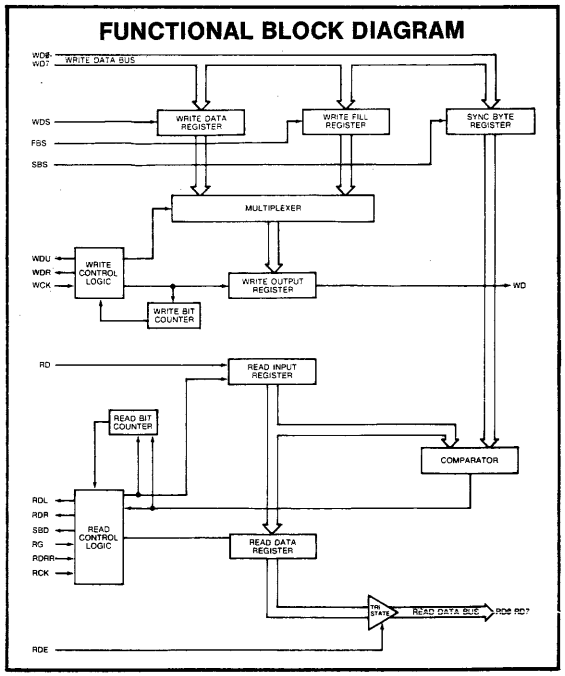
GENERAL DESCRIPTION

The CCC 3500 is an MOS integrated circuit which simplifies the data interface between a processor and a magnetic tape cassette or cartridge drive. During a write operation the CCDH receives data from the processor and shifts it out bit serially to the cassette/cartridge data encoding logic. Similarly during a read operation the CCDH receives a bit-serial stream of read data from the cassette/cartridge data recovery circuit, establishes byte synchronization by detecting the sync byte, and transfers data on a byte by byte basis to the processor.

The CCDH detects data overrun and underrun conditions and indicates these conditions on its status lines. A data underrun causes data from a special programmable fill register to be written onto the cassette/cartridge until new data is entered into the write data buffer or until the write operation is ended.

Separate read and write data registers permit simultaneous read and write operations. Drives with dual gap heads may utilize this read-while-write feature for write data verification thereby enhancing system throughput and reliability. The CCDH is fully double buffered and all inputs and outputs are TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



SECTION VI

DESCRIPTION OF OPERATION

Write Operation

After power-on, the Write Clock is set at the desired bit rate and the desired fill byte is written into the Write Fill Register. After the external control logic has caused the tape to come up to operating speed and activated the write enable signal, the first byte to be written should be loaded into the Write Data Register. This byte is then loaded into the Write Output Register and shifted out bit serially to the external write encoding logic. The first bit shifted out of each byte is the LSB. Whenever a byte is transferred from the Write Data Register to the Write Output Register, Write Data Request becomes active and requests another byte from the processor. If new data is not loaded into the Write Data Register before the Write Output Register becomes empty, then the Write Output Register is loaded with data from the Write Fill Register and the Write Data Underrun status line is set. WDU is reset the next time WDS is pulsed. At the end of the write operation, the processor should return the external write enable line to an inactive state.

Read Operation

After power-on, the desired sync byte is loaded into the Sync Byte Register. After the external control logic has initiated forward motion and the tape has come up to operating speed, the processor produces a positive-to-negative transition on the Read Gate input to set the read logic into the sync byte search mode. In the search mode the serial read data bit stream is examined on a bit by bit basis until a sync byte is found. A sync byte is found, by definition, when the contents of the Sync Byte Register and the Read Input Register are identical. When this occurs the Sync Byte Detected output is set high. This byte is then loaded into the Read Data Register and the read logic is set into the byte mode. In this mode each byte read is loaded into the Read Data Register and Read Data Request is made active high for each byte. The processor responds to each Read Data Request by enabling the output bus with Read Data Enable, reading the data byte from the Read Data Register, and resetting Read Data Request by pulsing Read Data Request Reset. If the processor fails to respond to Read Data Request within one byte time, the Read Data Lost status line is set. When the processor has read the required amount of data it may reset Read Gate to an inactive-high level and stop tape motion.

System Operation — Additional Features

Automatic Block Fill

In some applications, such as the end of a logical file, the system buffer may contain less than a full block of data. In this case the processor need supply only this data to the CCC 3500. The CCC 3500 will then underrun, setting the Write Data Underrun Status line and thereby causing the remainder of the block to fill with bytes taken from the Write Fill Register. This operation continues until the processor returns the drive's write enable signal to an inactive level.

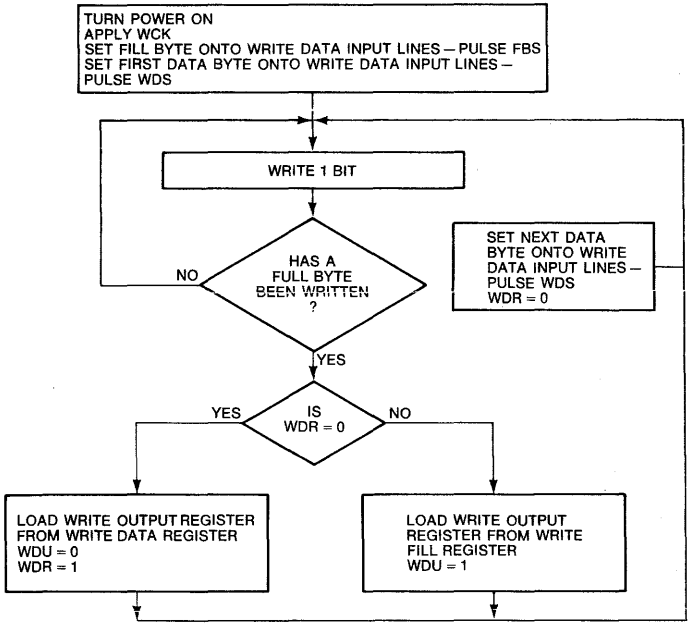
Byte Search

After byte synchronization has been established during a read operation, the processor may load a different byte into the Sync Byte Register. Whenever that byte occurs in the data being read, the Sync Byte Detected status line will go high. This feature permits the processor to search for the occurrence of a specific byte while reading a block.

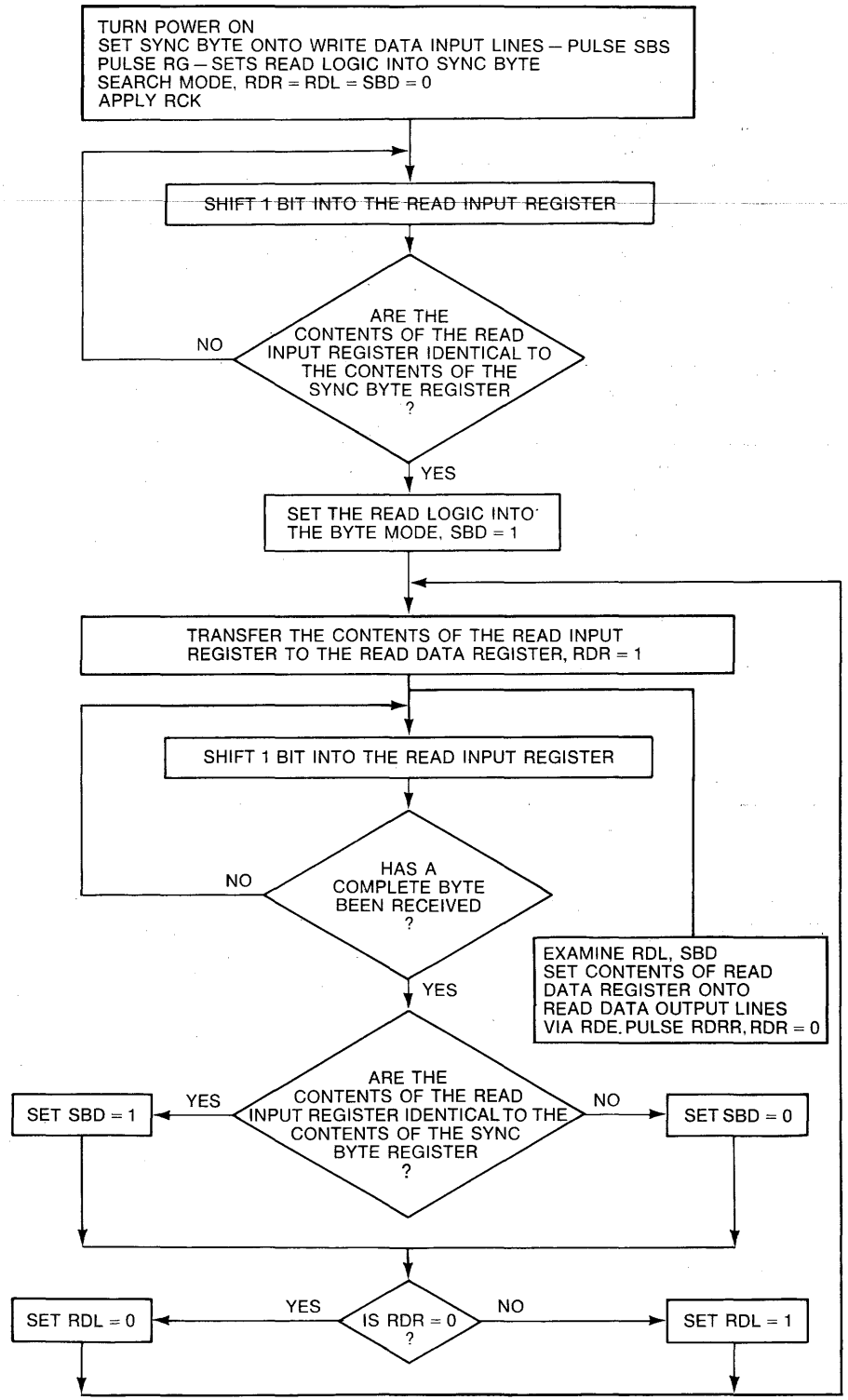
Multiple Byte Synchronization

Some systems use two or more contiguous sync bytes to establish byte synchronization. For these applications, the number of Read Data Requests received while Sync Byte Detected remains active-high may be counted by the processor to establish valid synchronization.

FLOW DIAGRAM — WRITE DATA



FLOW DIAGRAM — READ DATA



DESCRIPTION OF PIN FUNCTIONS

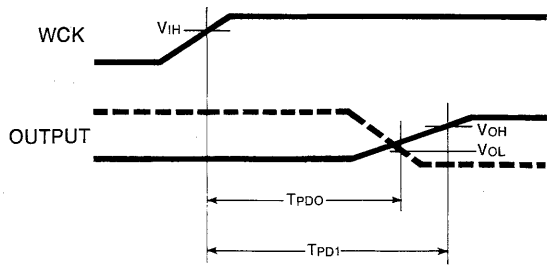
PIN NO.	SYMBOL	NAME	FUNCTION
1	RD	Read Data	The Read Data input accepts the serial data stream from the cassette/cartridge data recovery circuit.
2	RCK	Read Clock	The negative-going edge of the Read Clock input shifts Read Data into the Read Input Register.
3	RDRR	Read Data Request Reset	An active-high pulse input on the Read Data Request Reset input resets the RDR output to a low level.
4	RDE	Read Data Enable	An active-high level on the Read Data Enable line gates the outputs of the Read Data Register onto the Read Data Output lines.
5	RDR	Read Data Request	The Read Data Request output is made active-high when an assembled byte is transferred from the Read Input Register to the Read Data Register.
6	RDL	Read Data Lost	The Read Data Lost output is made active-high, if the byte presently in the Read Data Register is not read (RDR not reset) by the processor before the next byte is loaded into the Read Data Register.
7-14	RD7-RDØ	Read Data Output	When enabled by RDE the tri-state Read Data Output lines present the data in the Read Data Register to the processor. When RDE is inactive-low the RD7-RDØ lines are held at a high-impedance state.
15-19	NC		Not Connected
20	V_{CC}	Power Supply	+5 volt supply
21	NC		Not Connected
22	WDR	Write Data Request	The Write Data Request output is made active-high when the Write Data Register becomes empty and requires a data byte. It is reset to a low level when WDS occurs to load the Write Data Register. If WDR is not serviced by the time the next byte is required by the Write Output Register, the byte stored in the Write Fill Register is written onto the cassette/cartridge and the WDU line is made active high.
23	WD	Write Data	The Write Data output presents the serial stream of data to the external write data encoder. Each byte is normally provided from the Write Data Register provided that a WDS pulse occurs during the presently written byte. If WDS is not pulsed, the next byte to be written will be extracted from the Write Fill Register.
24	GND	Ground	Ground
25	WDU	Write Data Underrun	The Write Data Underrun output is set active-high when the processor fails to respond to the WDR signal within one byte time. When WDU occurs the data written on the disk is extracted from the Write Fill Register. This line is reset when WDS is pulsed.
26	V_{DD}	Power Supply	−12 volt supply
27-34	WDØ-WD7	Write Data Input	The Write Data Input lines present information to the Write Data Register, the Write Fill Register, and the Sync Byte Register under control of their respective strobes. The strobes operate independently of each other. The LSB should always be placed on WDØ.
35	RG	Read Gate	This input should be pulsed to a high-level after power turn on to reset RDR, SBD, and RDL to an inactive-low level. The high-to-low transition of RG sets the read logic into the sync byte search mode. In this mode the serial Read Data stream is examined on a bit by bit basis until a sync byte is found. A sync byte is found by definition when the contents of the Sync Byte Register and the Read Input Register are identical. When this occurs the SBD output is set active-high. The sync byte just read is then transferred into the Read Data Register; RDR is set high, and the read logic is set into the byte mode. In this mode each byte read is transferred into the Read Data Register.
36	SBD	Sync Byte Detected	The Sync Byte Detected output is set active-high each time the byte loaded into the Read Data Register is identical to the byte in the Sync Byte Register. This output is reset low the next time the Read Data Register is loaded with a byte which is not a sync byte.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	FUNCTION
37	FBS	Fill Byte Strobe	The Fill Byte Strobe is an active-high input strobe which loads the byte on the WDØ-WD7 lines into the Write Fill Register.
38	WCK	Write Clock	Each positive-going edge of this clock shifts one bit out of the Write Output Register onto WD.
39	WDS	Write Data Strobe	The Write Data Strobe is an active-high input strobe which loads the byte on the WDØ-WD7 lines into the Write Data Register.
40	SBS	Sync Byte Strobe	The Sync Byte Strobe is an active-high input strobe which loads the byte on the WDØ-WD7 lines into the Sync Byte Register.

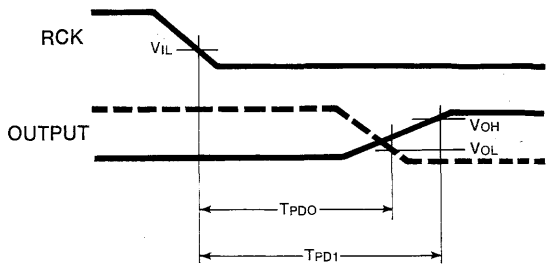
ADDITIONAL TIMING INFORMATION
(Typical Propagation Delays)

WRITE DATA

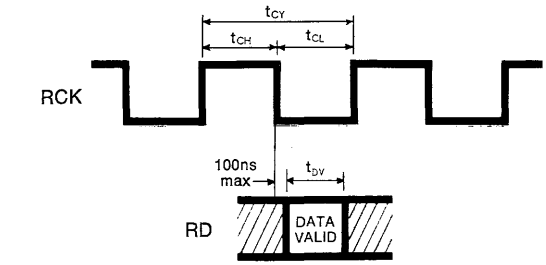


OUTPUT	T_{PDO}	T_{PD1}	UNITS
WDR	NA	2.0	µS
WDU	1.0	1.5	µS
WD	1.0	1.0	µS

READ DATA



OUTPUT	T_{PDO}	T_{PD1}	UNITS
RDR	NA	1.5	µS
RDL	2.0	2.5	µS
SBD	2.0	2.5	µS
RDØ-RD7	2.5	2.5	µS



MIN. TIMING	CCC 3500	UNITS
t_{CY}	4.0	µS
t_{CH}	1.0	µS
t_{CL}	2.0	µS
t_{DV}	1.4	µS

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Load Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, V_{CC} ..... +0.3V
Negative Voltage on any Pin, V_{CC} ..... −25V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

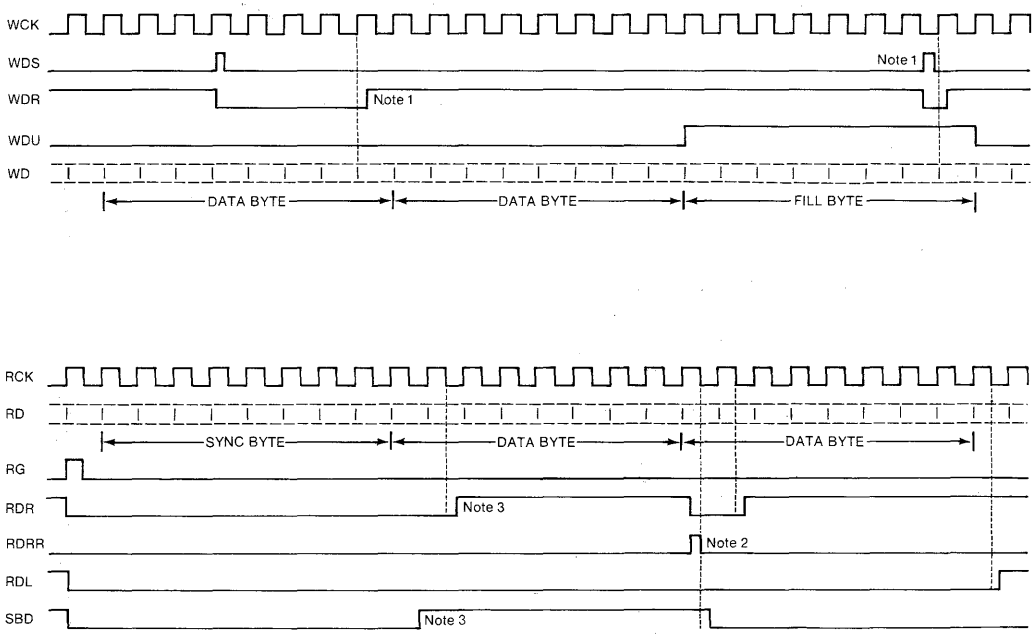
ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±5% V_{DD} = −12V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Conditions
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}	V_{DD}		0.8	V	
High-level, V_{IH}	V_{CC}-1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}		0.2	0.4	V	I_{OL} = 1.6mA
High-level, V_{OH}	2.4	4.0		V	I_{OH} = −100μA
INPUT CURRENT					
Low-level, I_{IL}			1.6	mA	See note 1
OUTPUT CURRENT					
Leakage, I_{LO}			-1	μA	RDE = V_{IL}, 0 ≤ V_{OUT} ≤ +5V
Short circuit, I_{OS}**			10	mA	V_{OUT} = 0V
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pF	V_{IN} = V_{CC}, f = 1MHz
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pF	RDE = V_{IL}, f = 1MHz
POWER SUPPLY CURRENT					
I_{CC}			28	mA	All outputs = V_{OH}
I_{DD}			28	mA	
A.C. CHARACTERISTICS					T_A = +25°C
CLOCK FREQUENCY	DC		250	KHz	RCK, WCK
PULSE WIDTH					
Clock	1			μs	RCK, WCK
Read Gate	1			μs	RG
Write Data Strobe	200			ns	WDS
Fill Byte Strobe	200			ns	FBS
Sync Byte Strobe	200			ns	SBS
Read Data Request Reset	200			ns	RDRR
INPUT SET-UP TIME					
Write Data Inputs	0			ns	WDØ-WD7
INPUT HOLD TIME					
Write Data Inputs	0			ns	WDØ-WD7
STROBE TO OUTPUT DELAY					Load = 20pf + 1 TTL input
Read Data Enable		180	250	ns	RDE: T_{PD1}, T_{PD0}
OUTPUT DISABLE DELAY		100	250	ns	RDE

**Not more than one output should be shorted at a time.

NOTES:
1. Under steady state condition no current flows for TTL or MOS interfacing.
   A switching current of 1.6mA maximum flows during a high to low transition of the input.
2. The tri-state output has 3 states:
   1) low-impedance to V_{CC}
   2) low-impedance to GND
   3) high-impedance OFF ≅ 10M ohms
   The OFF state is controlled by the RDE input.

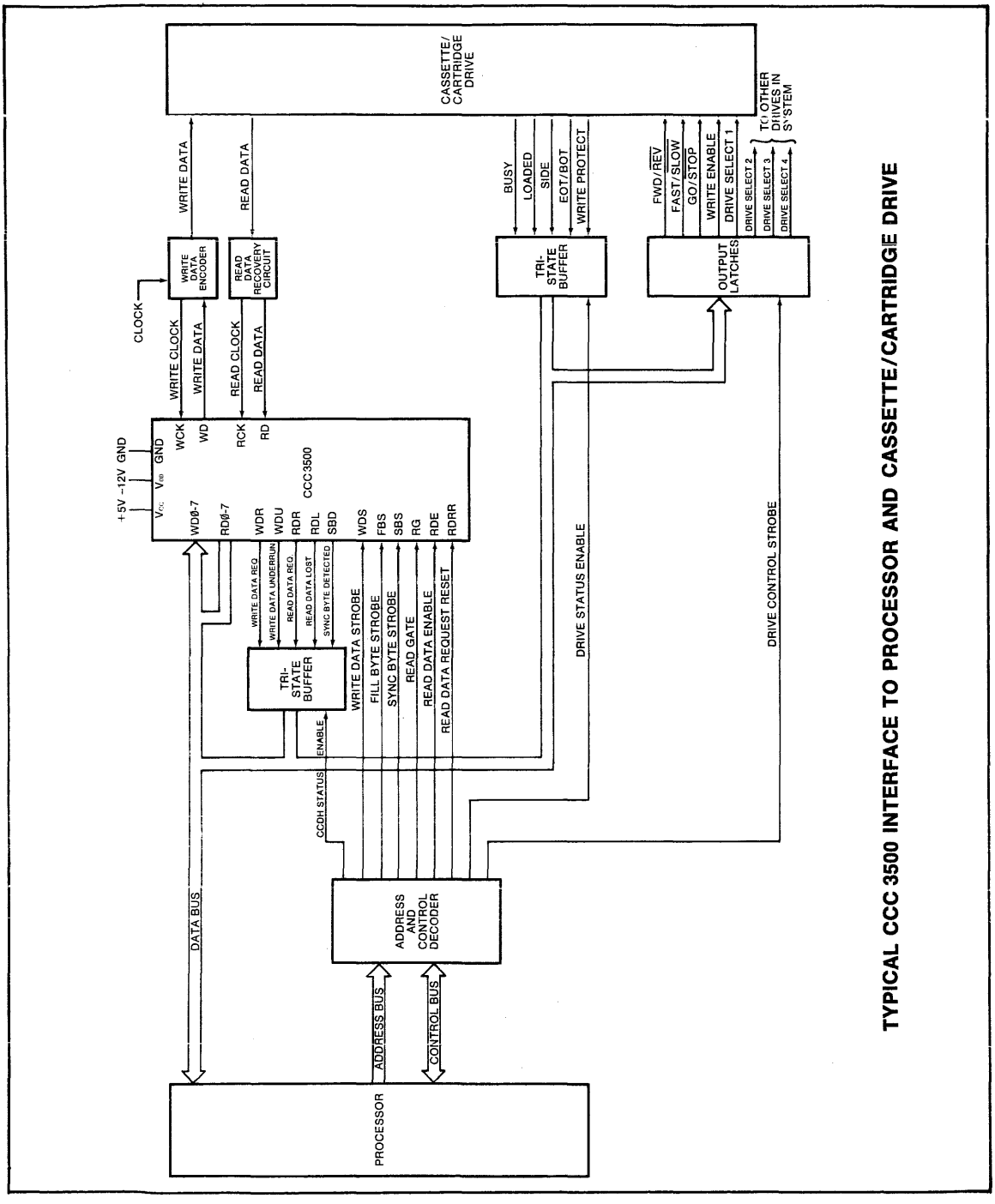
CCDH TIMING DIAGRAM



NOTE 1
The Write Output Register is loaded with the next byte at the positive clock transition corresponding to the leading edge of the last bit of the current byte on the WD output. WDR is set high approximately two microseconds after this clock transition. If it is desired that the next byte be extracted from the Write Data Register the leading edge of the WDS should occur at least one microsecond prior to this clock transition.

NOTE 2
In order to avoid an RDL indication the leading edge of the RDRR pulse should occur at least one microsecond prior to the negative clock transition corresponding to the center of the first bit after the last bit of the previous byte on the RD input.

NOTE 3
The RDL, SBD and RD0-RD7 output are set to their correct levels approximately two microseconds after the negative clock transition corresponding to the center of the first bit after the last bit of the previous byte on the RD input. The RDR output is set high at the next negative clock transition.



TYPICAL CCC 3500 INTERFACE TO PROCESSOR AND CASSETTE/CARTRIDGE DRIVE

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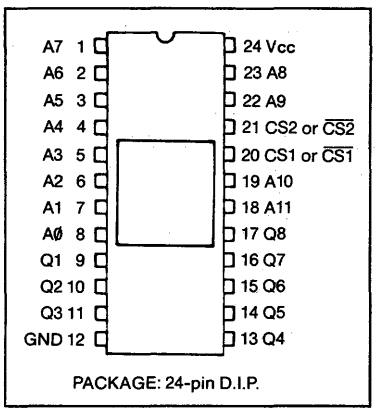
ROM 4732
μPC FAMILY

4096 X 8-Bit Static Read-Only Memory
32K ROM

FEATURES

- ☐ 4096 x 8 Organization
- ☐ All Inputs and Outputs TTL-Compatible
- ☐ Fully Static (No Clocks, No Refresh)
- ☐ Single +5v Power Supply
- ☐ Maximum Access Time...450ns
- ☐ Minimum Cycle Time...450ns
- ☐ Typical Power Dissipation...580mW
- ☐ Three-State Outputs for Wire-OR Expansion
- ☐ Industry Standard 24 pin DIP Pin Out
- ☐ Pin Compatible with TMS 4732, TMS 4700, TMS 2708 and Intel 2316E
- ☐ Two programmable chip select inputs for Chip Select Flexibility
- ☐ Automated Custom Programming—Formats—Media
- ☐ COPLAMOS® N-Channel MOS Technology

PIN CONFIGURATION



PACKAGE: 24-pin D.I.P.

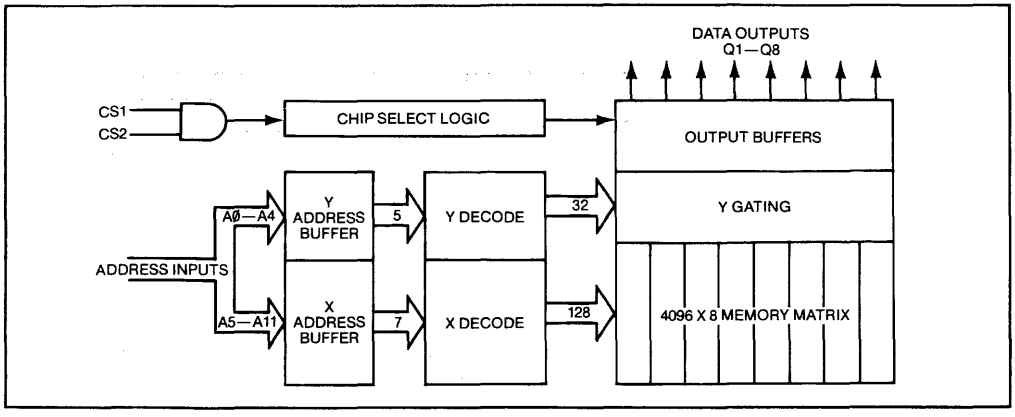
GENERAL DESCRIPTION

The ROM 4732 is a 32,768-bit read-only memory organized as 4096 words of 8-bit length. This makes the ROM 4732 ideal for microprocessor based systems. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with bipolar circuits.

All inputs can be driven directly by Series 74 TTL circuits without the use of any external pull-up resistor. Each output can drive one Series 74 or 74S load without external resistors. The data outputs are three-state for OR-tieing multiple devices on a common bus, facilitating easy memory expansion. Two chip select controls allow data to be read. These controls are programmable, providing additional system decode flexibility allowing four 32K ROMs to be OR-tied without external decoding. The data is always available, it is not dependent on external CE clocking.

The ROM 4732 is designed for high-density fixed-memory applications such as logic function generation and microprogramming. Systems utilizing 1024 x 8-bit ROMs or 1024 x 8-bit EPROMs can expand to the 4096 x 8-bit ROM 4732 with changes only to pins 18, 19, and 21. To upgrade from the 2316E, simply replace CS2 with A11 on pin 18.

BLOCK DIAGRAM



SECTION VI

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +7.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

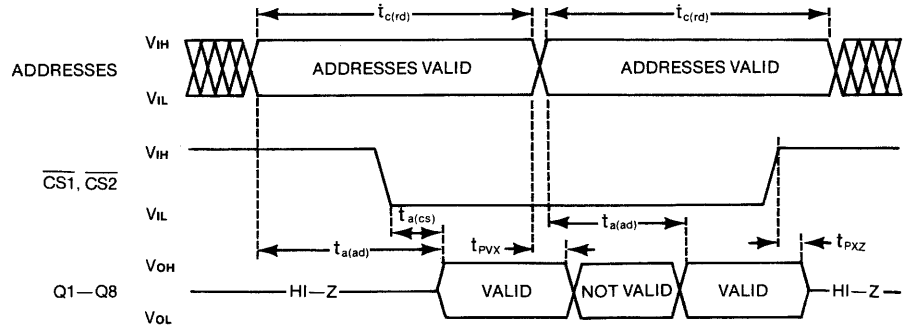
NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.65	V	
High-level, V_{IH}	2.0			V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL} = 2.0mA
High-level, V_{OH}	2.4			V	I_{OH} = −200μA
INPUT CURRENT					
Low-level, I_{IL}			10	μA	$0V \leq V_{IN} \leq V_{CC}$
OUTPUT CURRENT					
I_{OL}			±10	μA	Chip Deselected
INPUT CAPACITANCE					
All inputs, C_{IN}			7	pF	
OUTPUT CAPACITANCE					
All Outputs, C_{OUT}			10	pF	
POWER SUPPLY CURRENT					
I_{CC}			150	mA	
A.C. CHARACTERISTICS					1 Series 74 TTL load, C_L = 100 pF
Read cycle time, $t_{c(rd)}$	450			ns	
Access time from address, $t_{a(ad)}$			450	ns	
Access time from chip select, $t_{a(cs)}$			200	ns	
Previous output data valid after address change, t_{PVX}			450	ns	
Output disable time from chip select, t_{PXZ}			200	ns	

READ CYCLE TIMING



Description of Pin Functions

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 18, 19, 22, 23	A7, A6, A5, A4, A3, A2, A1, AØ, A11, A10, A9, A8	Addresses	I	The 12-bit positive-logic address is decoded on-chip to select one of 4096 words of 8-bit length in the memory array. AØ is the least significant bit and A11 the most significant bit of the word address. The address valid interval determines the device cycle time.
9, 10, 11, 13, 14, 15, 16, 17	Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8	Data Outputs	0	The eight outputs must be enabled by both chip select controls before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least significant bit, Q8 the most significant bit. The outputs will drive TTL circuits without external components.
12	GND	Ground	GND	Ground
20, 21	CS1, CS2	Chip Select	I	Each chip select control can be programmed during mask fabrication to be active with either a high or a low level input. When both chip select signals are active, all eight outputs are enabled and the eight-bit addressed word can be read. When either chip select is not active, all eight outputs are in a high-impedance state.
24	V_{CC}	Power Supply	PS	+5 volt power supply

PROGRAMMING DATA

PROGRAMMING REQUIREMENTS: The ROM 4732 is a fixed program memory in which the programming is performed via computer aided techniques by SMC at the factory during the manufacturing cycle to the specific customer inputs supplied in the punched computer card format below. The device is organized as 4096 8-bit words with address locations numbered Ø to 4095. The 8-bit words can be coded as a 2-digit hexadecimal number between ØØ and FF. All data words and addresses in the following format are coded in hexadecimal numbers. In coding, all binary words must be in positive logic before conversion to hexadecimal. Q1 is considered the least significant bit and Q8 the most significant bit. For addresses, AØ is least significant bit and A11 is the most significant bit.

Every card should include the SMC Custom Device Number in the form ROXXXX (4 digit number to be assigned by SMC) in column 75 through 80.

PROGRAMMABLE CHIP SELECTS: The chip select inputs shall be programmed according to the data punched in columns 73 and 74. Every card should include in column 73 a 1 if the output is to be enabled with a high level at CS2 or a Ø (zero) to enable the output with a low level at CS2. The column 74 entry is the same for programming CS1.

PROGRAMMED DATA FORMAT: The format for the cards to be supplied to SMC to specify that data to be programmed is provided below. The card deck for each device consists of 128 cards with each card containing data for 32 memory locations.

CARD COLUMN	HEXADECIMAL FORMAT
1 to 3	Hexadecimal address of first word on the card
4	Blank
5 to 68	Data. Each 8-bit memory byte is represented by two ASCII characters to represent a hexadecimal value of '00' or 'FF'.
69, 70	Checksum. The checksum is the negative of the sum of all 8-bit bytes in the record from column 1 to 68, evaluate modulo 256 (carry from high order bit ignored). (For purposes of calculating the checksum, the value of Column 4 is defined to be zero.) Adding together, modulo 256, all 8-bit bytes from Column 1 to 68 (Column 4 = 0), then adding the checksum, results in zero.
71, 72	Blank
73	One (1) or zero (Ø) for CS2
74	One (1) or zero (Ø) for CS1
75, 76	RO
77 to 80	XXXX (4 digit number assigned by SMC)

ALTERNATIVE INPUT MEDIA

In addition to the preferred 80 column "IBM Card," customers may submit their ROM bit patterns on 9-track 800-BPI mag tape, 8-channel perforated paper tape, EPROM, ROM, etc. Where one of several nationwide time sharing services is mutually available, arrangements may be made with the factory to communicate the ROM definition data directly through the service computer. Format requirements and other information required to use alternative input media may be obtained through SMC sales personnel.

ALTERNATIVE DATA FILE FORMATS

In addition to the standard SMC format, it is possible to furnish data to SMC in other formats if prearranged with the factory. Non-standard formats may be acceptable. Contact SMC sales personnel.

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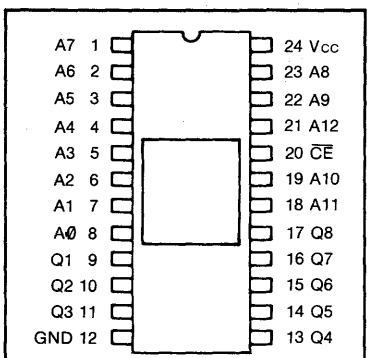
ROM 36000*
μPC FAMILY

8192 X 8-Bit Static Read-Only Memory
64K ROM

FEATURES

- ☐ 8192 X 8 Organization
- ☐ All Inputs and Outputs TTL-Compatible
- ☐ Edge Activated**
- ☐ Single +5V±10% Power Supply
- ☐ Maximum Access Time...250ns
- ☐ Minimum Cycle Time...375ns
- ☐ Low Power Consumption...220mW max active
- ☐ Low Standby Power Dissipation...35mW typical
- ☐ Three-State Outputs for Wire-OR Expansion
- ☐ Industry Standard 24 Pin DIP Pin Out
- ☐ Pin Compatible with MOSTEK MK36000-4
- ☐ On-Chip Address Latches
- ☐ Outputs drive 2 TTL loads and 100pf
- ☐ COPLAMOS® N-Channel MOS Technology

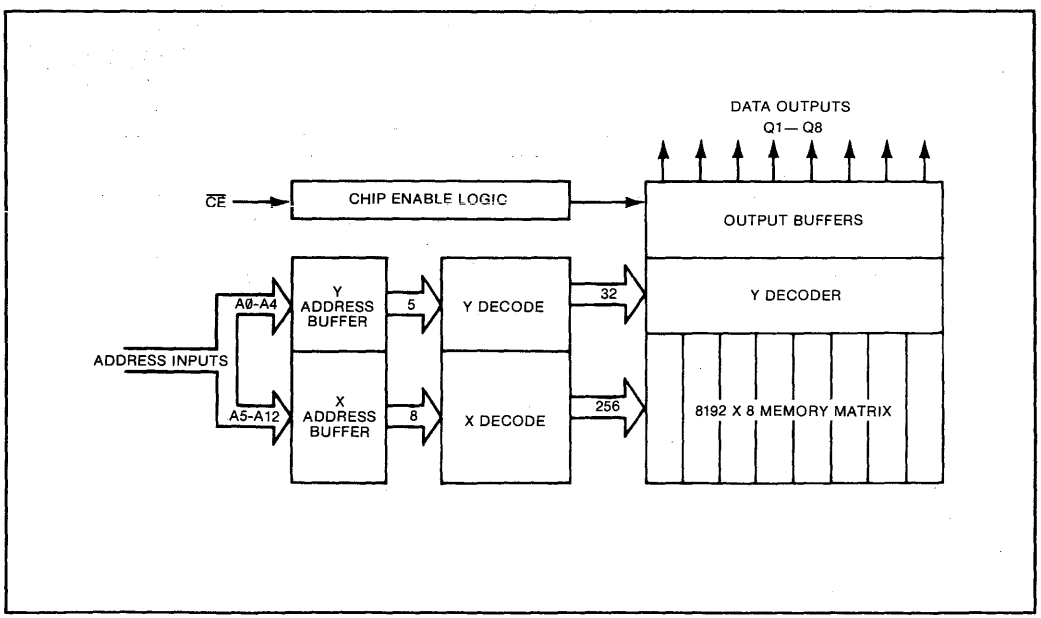
PIN CONFIGURATION



PACKAGE: 24-pin D.I.P.

SECTION VI

BLOCK DIAGRAM



*FOR FUTURE RELEASE

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GENERAL DESCRIPTION

The ROM 36000 is a new generation N-channel silicon gate MOS Read Only Memory, organized as 8192 words by 8 bits. As a state-of-the-art device, the ROM 36000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins.

The ROM 36000 utilizes what is fast becoming an industry standard method of device operation. Use of a static storage cell with clocked control periphery allows the circuit to be put into an automatic low power standby mode. This is accomplished by maintaining the chip enable ($\overline{CE}$) input at a TTL high level. In this mode, power dissipation is reduced to typically 35mW, as compared to unclocked devices which draw full power continuously. In system operation, a device is selected by the $\overline{CE}$ input, while all others are in a low power mode, reducing the overall system power. Lower power means reduced power supply cost, less heat to dissipate and an increase in device and system reliability.

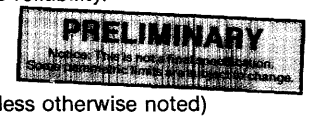
The edge activated chip enable also means greater system flexibility and an increase in system speed. The ROM 36000 features onboard address latches controlled by the $\overline{CE}$ input. Once the address hold time specification has been met, new address data can be applied in anticipation of the next cycle. Outputs can be wire- 'OR'ed together, and a specific device can be selected by utilizing the $\overline{CE}$ input with no bus conflict on the outputs. The $\overline{CE}$ input allows the fastest access times yet available in 5 volt only ROM's and imposes no loss in system operating flexibility over an unclocked device.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the $\overline{CE}$ input, will drive a minimum of 2 standard TTL loads. The ROM 36000 operates from a single +5 volt power supply with a wide ±10% tolerance, providing the widest operating margins available. The ROM 36000 is packaged in the industry standard 24 pin DIP.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS} ..... —0.5V to +7V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature—Ceramic (Ambient) ..... —65°C to +150°C
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±10%, unless otherwise noted)

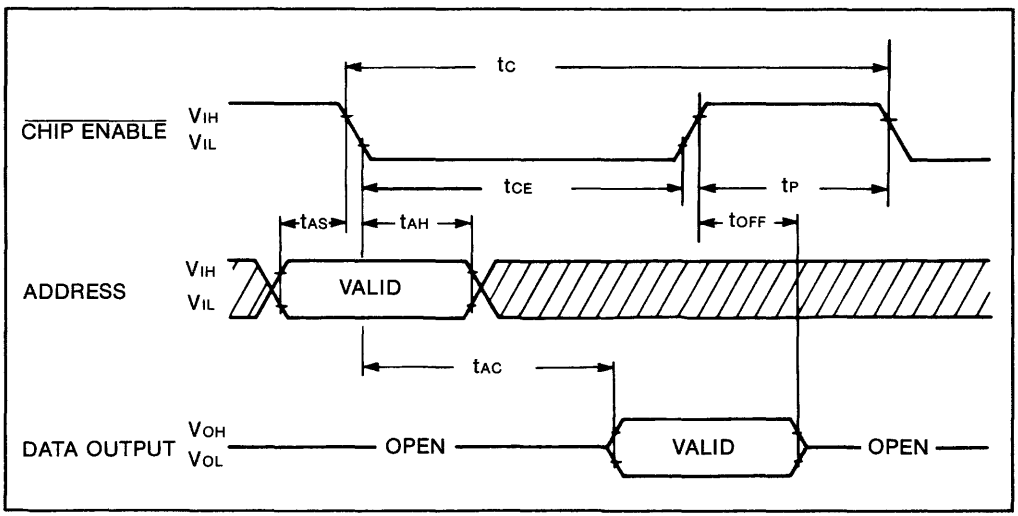
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	Volts	6
Input Logic 0 Voltage	V_{IL}	—0.5		0.8	Volts	
Input Logic 1 Voltage	V_{IH}	2.0		V_{CC}	Volts	
DC ELECTRICAL CHARACTERISTICS						
V_{CC} Power Supply Current (Active)	I_{CC1}			40	mA	1
V_{CC} Power Supply Current (Standby)	I_{CC2}		7		mA	7
Input Leakage Current	$I_{I(L)}$	—10		10	μA	2
Output Leakage Current	$I_{O(L)}$	—10		10	μA	3
Output Logic "0" Voltage @ I_{OUT} = 3.3mA	V_{OL}			0.4	Volts	
Output Logic "1" Voltage @ I_{OUT} = —220μA	V_{OH}	2.4			Volts	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
AC ELECTRICAL CHARACTERISTICS						
Cycle Time	tC	375			ns	4
$\overline{CE}$ Pulse Width	tCE	250				4
$\overline{CE}$ Access Time	tAC			250	ns	4
Output Turn Off Delay	tOFF			60	ns	4
Address Hold Time Referenced to $\overline{CE}$	tAH	60			ns	
Address Setup Time Referenced to $\overline{CE}$	tAS	0			ns	
CE Precharge Time	tP	125			ns	
CAPACITANCE						
Input Capacitance	CI		5		pF	5
Output Capacitance	CO		7		pF	5

NOTES:

1. Current is proportional to cycle rate. ICCI is measured at the specified minimum cycle time.
2. VIN = 0V to 5.5V.
3. Device unselected; VOUT = 0V to 5.5V.
4. Measured with 2 TTL loads and 100pF, transition times = 20ns.
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{\Delta Q}{\Delta V}$ with $\Delta V = 3$ volts
6. A minimum 100μs time delay is required after the application of VCC (+5) before proper device operation is achieved.
7. $\overline{CE}$ high.

TIMING DIAGRAM



OPERATION

The ROM 36000 is controlled by the chip enable ($\overline{CE}$) input. A negative going edge at the $\overline{CE}$ input will activate the device as well as strobe and latch the inputs into the onchip address registers. At access time the outputs will become active and contain the data read from the selected location. The outputs will remain latched and active until $\overline{CE}$ is returned to the inactive state.

PROGRAMMING

Standard Microsystems Corporation will accept data input in the form of 8K, 16K, 32K and 64K EPROMS and 8K, 16K, 32K and 64K ROMS. If other programming media is preferable, please consult the factory.

Printer

CHARACTER GENERATOR

Part Number	Description	Scan	Max Access Time	Power Supplies	Package	Page
CG 4103[1]	5 x 7 x 64	Column	1.2 μsec	+5, −12 or ±12	28 DIP	415-418

SHIFT REGISTER

Part Number	Description	Feature	Max Clock Freq.	Power Supply	Package	Page
SR 5015-XX[1]	Quad Static Shift Register Mask Programmable Length	Load, Recirculate, Shift Controls,	1 MHz	+5	16 DIP	419-422
SR 5015-80	Quad 80 Bit Static					
SR 5015-81	Quad 81 Bit Static					
SR 5015-133	Quad 133 Bit Static					
SR 5017	Quad 81 Bit	Shift Left/Shift Right, Recirculate Controls, Asynchronous clear	1 MHz	+5	16 DIP	423-426
SR 5018	Quad 133 Bit					

[1] May be custom mask programmed

STANDARD MICROSYSTEMS CORPORATION

4100 Series

CG4103

CHARACTER GENERATOR

2240-Bit Programmable (ROM) 64 Characters of 5 x 7 Bits

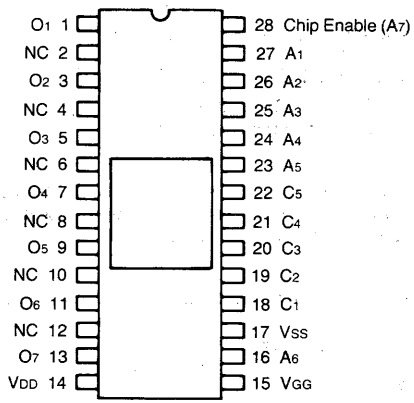
FEATURES

- ☐ Static Operation, no clocks required.
- ☐ 2240-Bit Capacity, fully decoded
- ☐ 64 Characters of 35 Bits (5 x 7)
- ☐ Column by Column Output—Column Scan
- ☐ TTL Compatible
- ☐ Wired "OR" Capability for memory expansion
- ☐ Power Supplies: +14v, −14v or +12v, −12v, or +5v, −12v
- ☐ Eliminates need for +12v power supply
- ☐ Single mask custom programming

APPLICATIONS

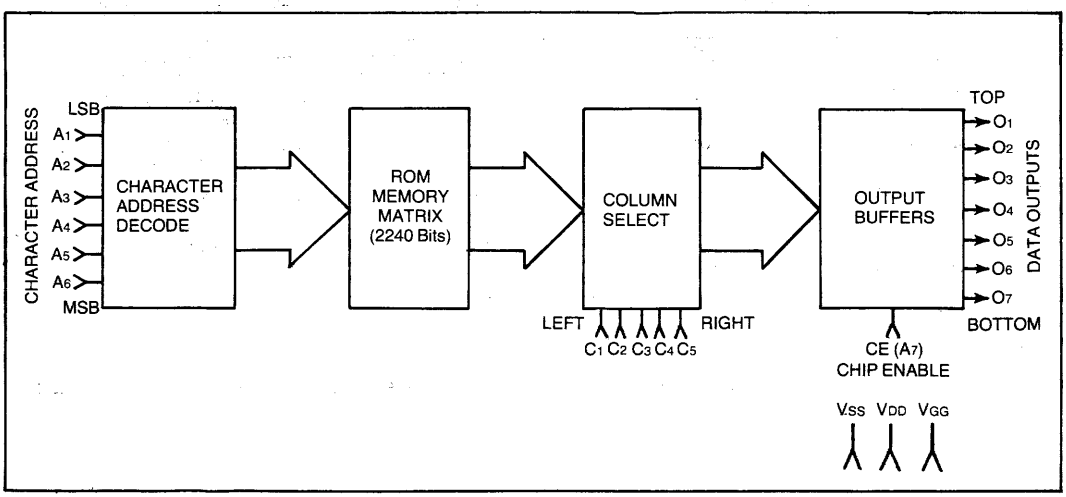
- ☐ Matrix Printers
- ☐ Vertical Scan Alphanumeric Displays
- ☐ Billboard and Stock Market Displays
- ☐ Strip Printer
- ☐ LED Matrix Arrays

PIN CONFIGURATION



NC = No Connection

BLOCK DIAGRAM



SECTION VII

General Description

The CG4100 Series MOS Read Only Memories (ROMs) are designed specifically for dot-matrix character generation where column by column output data is desired. Each ROM contains 2240 bits of programmable storage, organized as 64 characters, each having 5 columns of 7 bits.

The output word appears as a 5 word sequence on each of the output lines. Sequence is controlled by the 5 Column Select lines. By strobing the first select line, the first group of 7 bits (first column) is obtained at the output. By sequentially strobing C_1 through C_5 the font of the addressed character would be displayed. The character address may remain fixed while the column select changes.

Since only 6 address bits are required in order to decode the 64 stored characters, the seventh bit (A_7) may be used as a chip enable. The chip enable (CE) in conjunction with the single ended open drain output buffers allow for memory expansion through wired "OR" connection.

The CG4100 Series contains an USASCII character font. Custom memory patterns are provided through the use of customer provided encoding sheets, tapes, or card decks.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... −25°C to + 85°C
Storage Temperature Range ..... −55°C to +150°C
Voltage on any Pin, with respect to V_{SS} ..... +0.3V to −30V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

RECOMMENDED OPERATING CONDITIONS (−25°C≤T_A≤+85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Suppy Voltage	V_{SS}		0.0		V
Supply Voltage	V_{DD}	−12.0	−14.0	−16.0	V
Supply Voltage	V_{GG}	−24.0	−28.0	−29.0	V
Input Voltage, logic "O" Logic "O"=most positive level	V_{IH}	V_{SS} −1.5	V_{SS}		V
Input Voltage, logic "I" Logic "I"=most negative level	V_{IL}		V_{DD}	V_{SS}−11	V

Note: The design of the CG4100 permits a broad range of operation that allows the user to take advantage of readily available power supplies; e.g. +5V, −12V. See "Operational Interface—To/From TTL logic" diagram.

ELECTRICAL CHARACTERISTICS (V_{SS}=+14v, V_{GG}=−14v, V_{DD}=Ground, T_A=25°C, unless otherwise noted)

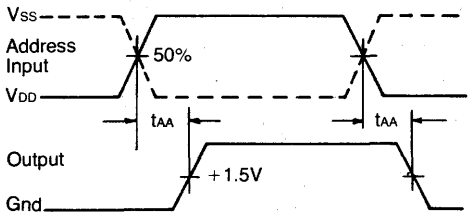
Parameter	Symbol	Min.	Typ.	Max.	Units	Comments
Output Blank Current	I_{OB}	—	—	10	μa	V_{DD} applied to output see Note 1.
Output Dot Current	I_{OD}	2.5	—	—	ma	V_{DD} applied to output see Note 1.
Input Leakage Current	I_{IN}	—	—	10	μa	V_{IN} = 0V
Output Voltage	V_O	—	2.0	—	V	Io=0.5ma
		—	5.0	—	V	Io=2.0ma
Address Access Time	t_{AA}	—	—	1200	ns	
Column Select Access Time	t_{CA}	—	—	600	ns	
Chip Enable Access Time	t_{CE}	—	—	400	ns	
Power Dissipation		—	—	400	mw	Output unconnected

Note 1: An output dot is defined as the ON state of the MOS output transmitter. An output blank is defined as the OFF state.

Description of Pin Functions

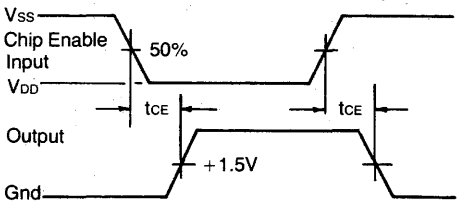
Pin No.	Symbol	Name	Function
1, 3, 5, 7 9, 11, 13	O_1, O_2, O_3, O_4 O_5, O_6, O_7	Outputs	7 Data Outputs
14	V_{DD}	V_{DD}	Usually connected to Ground
15	V_{GG}	V_{GG}	Negative power supply: −14v or −12v
16	A_6	Address	Bit 6 of the character address
17	V_{SS}	V_{SS}	Positive power supply: +14v or +12v or +5v
18-22	C_1-C_5	Column Select	Column Select inputs
23-27	A_5-A_1	Address	Bits 1 through 5 of the character address
28	CE(A_7)	Chip Enable	Chip Enable for memory expansion

ADDRESS ACCESS TIMING



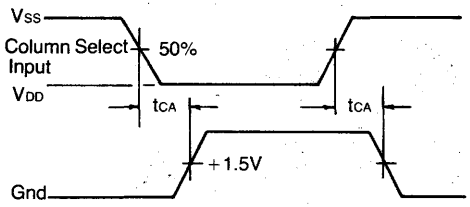
Only one of the five Column Select inputs is at logic "1."
Chip Enable input is at logic "1."

CHIP ENABLE ACCESS TIMING



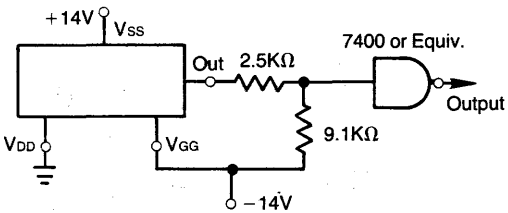
Only one of the five Column Select inputs is a logic "1."
Address inputs are set in a dc state.

COLUMN SELECT ACCESS TIMING



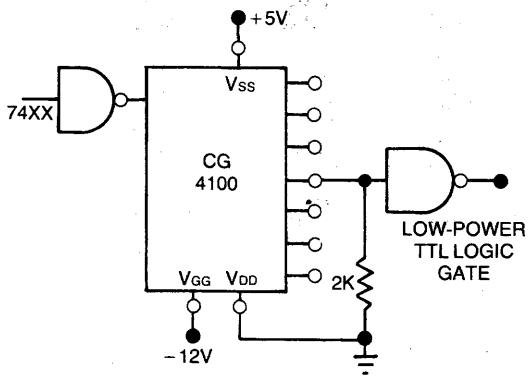
All Column Select inputs are at logic "0" except one under test.
Address inputs are set in a dc state.
Chip Enable input is at logic "1."

AC TEST CIRCUIT

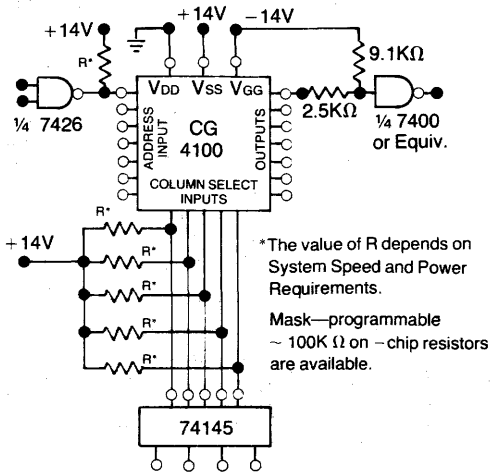


$t_r = t_f < 50$ ns for all timing diagram forcing functions.
All output waveforms are measured at the output of the 7400 TTL gate.

OPTIONAL INTERFACE TO/FROM TTL LOGIC

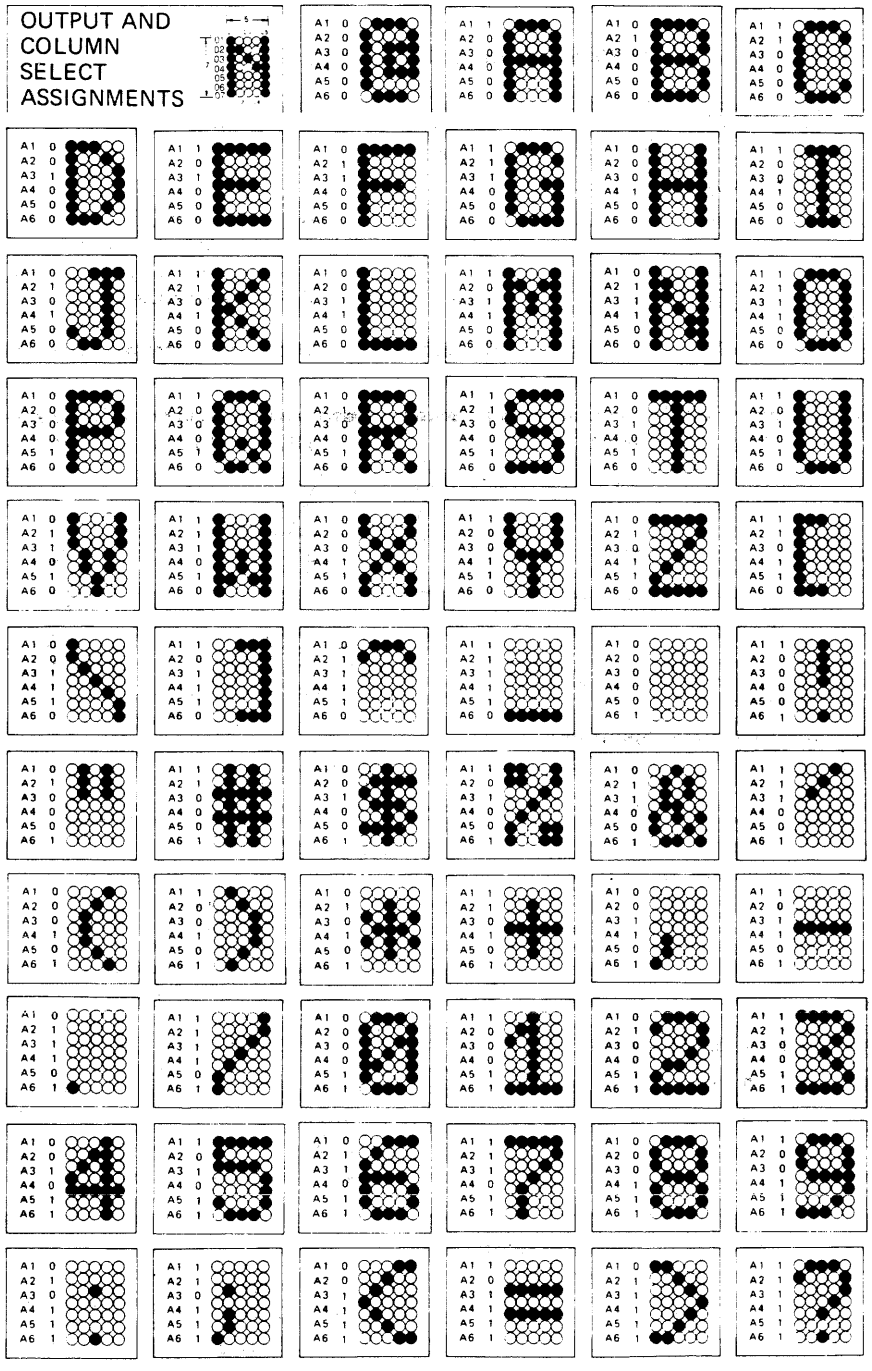


INTERFACE TO TTL LOGIC



*The value of R depends on System Speed and Power Requirements.

Mask—programmable ~ 100K Ω on −chip resistors are available.



Pin-for-Pin Equivalent for: TMS 4103 MK2002 S8499.

STANDARD MICROSYSTEMS CORPORATION
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STANDARD MICROSYSTEMS CORPORATION

SR 5015-XXX

SR 5015-80
SR 5015-81
SR 5015-133

Quad Static Shift Register

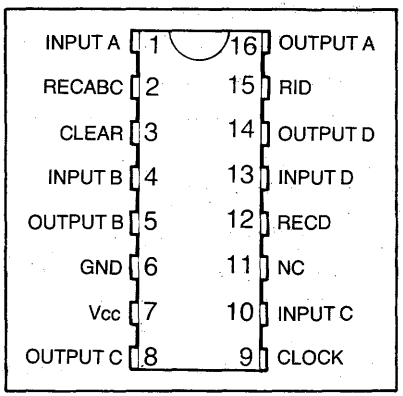
FEATURES

- ☐ COPLAMOS® N Channel Silicon Gate Technology
- ☐ Variable Length—Single Mask Programmable—1 to 134 bits
- ☐ Directly TTL-compatible on all inputs, outputs, and clock
- ☐ Clear function
- ☐ Operation guaranteed from DC to 1.0 MHz
- ☐ Recirculate logic on-chip
- ☐ Single +5.0V power supply
- ☐ Low clock input capacitance
- ☐ 16 pin ceramic DIP Package
- ☐ Pin for Pin replacement for AMI S2182, 83. 85

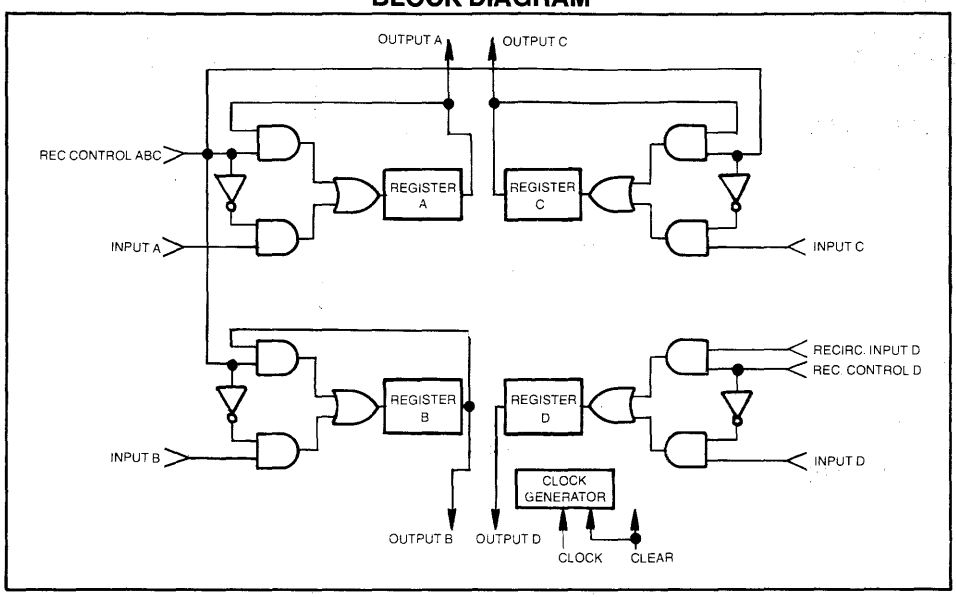
APPLICATIONS

- ☐ Memory Buffering
- ☐ Unique Buffering Lengths
- ☐ Terminals

PIN CONFIGURATION



BLOCK DIAGRAM



General Description

The SMC SR 5015-XXX is a quad static shift register family fabricated using SMC's COPLAMOS® N channel silicon gate process which provides a higher functional density and speed on a monolithic chip than conventional MOS technology. The COPLAMOS® process provides high speed operation, low power dissipation, low clock input capacitance, and single +5 volt power supply operation.

These shift registers can be driven by either T²L circuits or by MOS circuits and provide driving capability to MOS or T²L circuits. This device consists of four separate static shift registers with independent input and output terminals and logic for loading, recirculating or shifting information. The SR 5015-80, SR 5015-81, and SR 5015-133 are respectively 80, 81, and 133 bit quad shift registers.

The recirculate control pin is common for registers A, B, and C. Register D has an independent recirculate control pin as well as a recirculate input pin.

A clear pin has been provided that will cause the shift register to be cleared when the pin is at V_{CC}. A single T²L clock is required for operation.

The transfer of data into the register is accomplished on the low-to-high transition of the clock with the recirculate control low. For long term data storage the clock may be stopped and held in either logic state. Recirculate occurs when the recirculate control is high. Output data appears on the low-to-high transition of the clock pulse.

Bits 81 and 133 are available for flag storage.

This device has been designed to be used in high speed buffer storage systems and small recirculating memories.

Special custom configurations are achieved via single mask programming in lengths of 1 to 134 bits.

MAXIMUM GUARANTEED RATINGS*

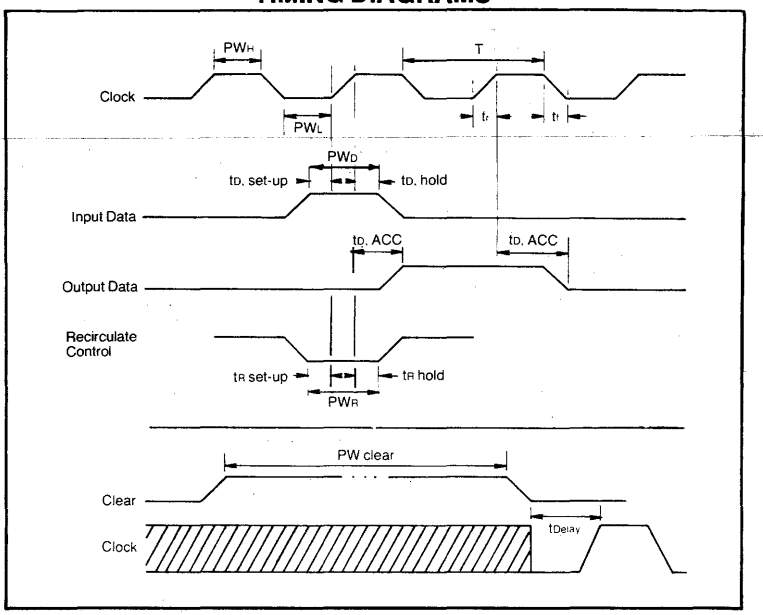
Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. Characteristics					
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	V_{CC}−1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low Level, V_{OL}			0.4	V	I_{OL}=1.6ma
High Level, V_{OH}	V_{CC}−1.5	4.0		V	I_{OH}=100μa
INPUT LEAKAGE CURRENT			1.0	μa	$V_{IN}=V_{CC}$
CLOCK, CLEAR			25	pf	
All Other			10	pf	
POWER SUPPLY CURRENT			80	ma	
A.C. Characteristics					T_A=+25°C
CLOCK					
PW_H	300			ns	
PW_L	600			ns	
Transition, t_r, t_f		0.02	1.0	μs	
Repetition Rate, 1/T	0		1.0	MHz	
t_{Delay}	300			ns	
INPUT DATA					
t_D, set-up	100			ns	
t_D, hold	200			ns	
PW_D	300			ns	
OUTPUT DATA					
t_D, ACC		200	350	ns	
RECIRCULATE CONTROL					
t_R, set-up	200			ns	
t_R, hold	300			ns	
PW_R	500			ns	
CLEAR					
PW_{CLEAR}	20			μs	

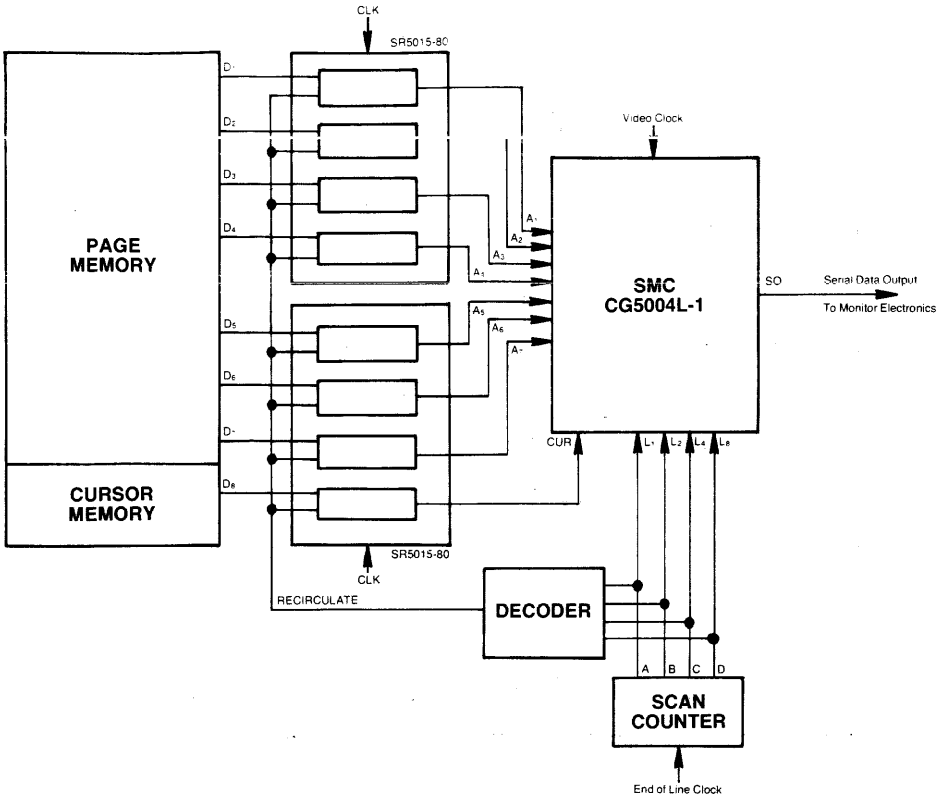
TIMING DIAGRAMS



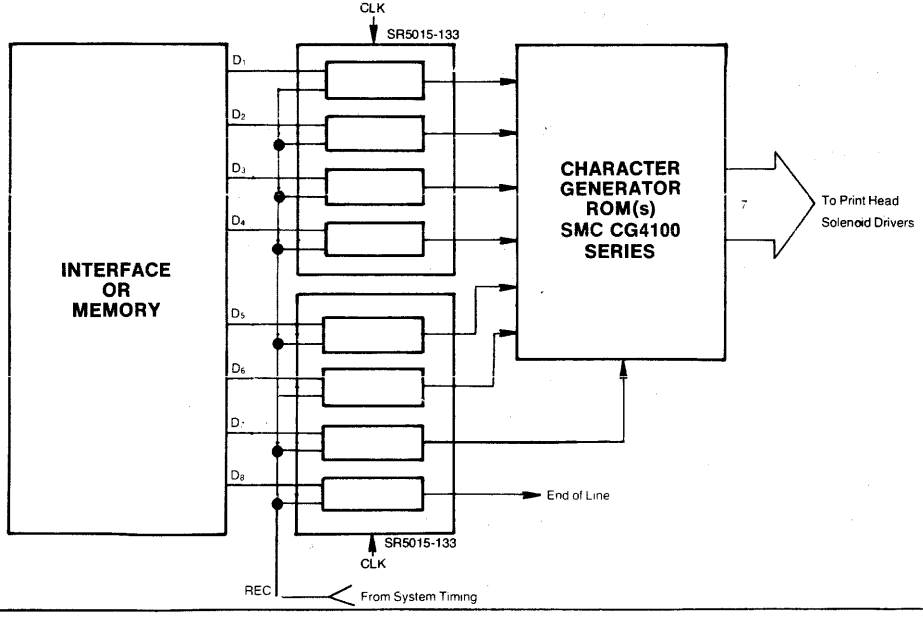
Description of Pin Functions

Pin No.	Symbol	Name	Function
1	A	Input A	Input signal which is either high or low depending on what word is to be loaded into shift register.
2	RECABC	Recirculate ABC	Input signal when high disconnects inputs from registers and connects outputs to inputs, thus recirculating data. Recirculates only A, B, C outputs.
3	CLR	Clear	Input signal when high forces outputs to a low state immediately and clears all the registers.
4	B	Input B	Input signal for B register.
5	O_B	Output B	Output signal for B register.
6	GND	GND	Power supply Ground.
7	V_{CC}	+5 Volt	5 volt power supply.
8	O_C	Output C	Output signal for C register.
9	CLK	Clock Input	Input signal which is normally low and pulses high to shift data into the registers. The data is clocked in on low to high edge of clock.
10	C	Input C	Input signal for C register.
11	NC	NC	
12	RECD	Recirculate Control D	Input signal which is normally low and, when goes high, disconnects Input D to register and connects Recirculate Input D to register.
13	D	Input D	Input signal for D register.
14	O_D	Output D	Output signal for D register.
15	RID	Recirculate Input D	Input signal which is the input to the D register when Recirculate Control D is high: RECD=1.
16	O_A	Output A	Output signal for A register.

Line Buffer for CRT Display . . . 80 Characters per line.



Line Buffer for Matrix Printer . . . 132 Characters per line.



STANDARD MICROSYSTEMS CORPORATION

SR 5017
SR 5018

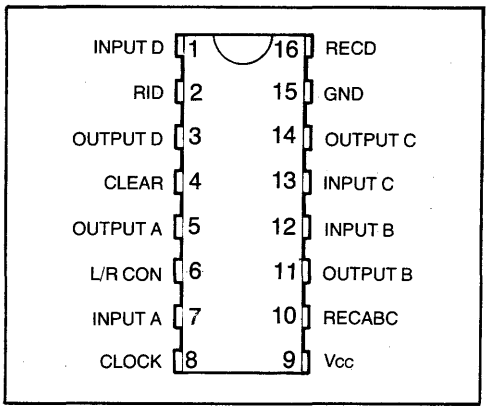
Quad Static Shift Right/Shift Left Shift Register

Last In First Out Buffer
LIFO

FEATURES

- ☐ COMPLAMOS® N-Channel Silicon Gate Technology.
- ☐ Quad 81 bit or Quad 133 bit
- ☐ Directly Compatible with T²L, MOS
- ☐ Operation Guaranteed from DC to 1.0MHz
- ☐ Recirculate logic on-chip
- ☐ Single +5.0V power supply
- ☐ Low clock input capacitance
- ☐ Single phase clock at T²L levels
- ☐ Clear function
- ☐ 16-pin Ceramic DIP Package

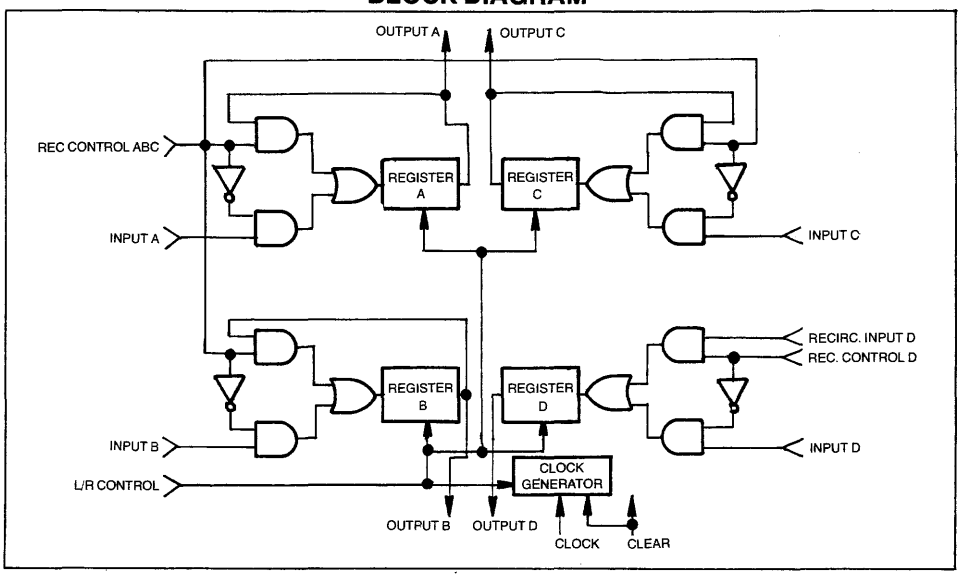
PIN CONFIGURATION



APPLICATIONS

- ☐ Bi-Directional Printer
- ☐ Computers—Push Down Stack—LIFO
- ☐ Buffer data storage—memory buffer
- ☐ Delay lines—delay line processing
- ☐ Digital filtering
- ☐ Telemetry Systems
- ☐ Terminals
- ☐ Peripheral Equipment

BLOCK DIAGRAM



SECTION VII

General Description

The SMC SR 5017 and SR 5018 are quad 133 (SR 5017) and quad 81 (SR 5018) bit static shift registers utilizing SMC's COPLAMOS® N channel silicon gate process. The COPLAMOS® process provides high speed operation, low power dissipation, low clock input capacitance, and requires only a single +5 volt power supply.

These shift registers can be driven by either T²L circuits or by MOS circuits and provide driving capability to MOS to T²L circuits.

This device consists of four separate static shift registers with independent input and output terminals and logic for loading, recirculating or shifting information right or left. This shift left/shift right (L/R Control) control input is common to all registers.

The recirculate control input is common for registers A, B, and C. Register D has an independent recirculate control input as well as a Recirculate Input.

A Clear input has been provided that will cause the shift register to be cleared when the input is at V_{CC}. A single T²L clock input is required for operation.

The transfer of data into the register is accomplished on the low-to-high transition of the clock with the recirculate control low. For long term data storage the clock may be stopped and held in either logic state. Recirculate occurs when the recirculate control is high. Output data appears on the low-to-high transition of the clock pulse.

Bits 81 or 133 are available for flag storage.

MAXIMUM GUARANTEED RATINGS*

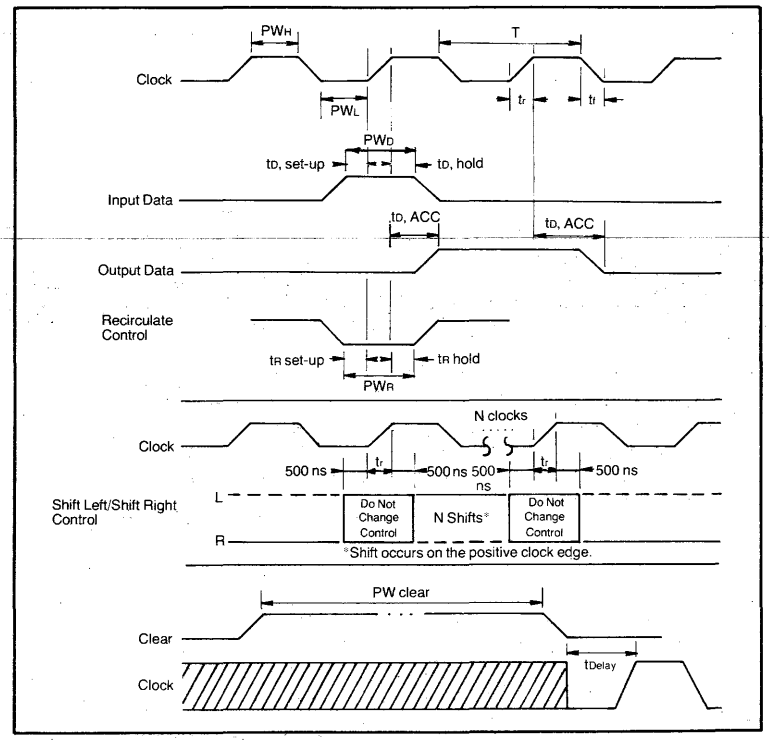
Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}= +5V±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. Characteristics					
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	V_{CC}—1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low Level, V_{OL}			0.4	V	I_{OL}=1.6ma
High Level, V_{OH}	V_{CC}—1.5	4.0		V	I_{OH}=100μa
INPUT LEAKAGE CURRENT			1.0	μa	V_{IN}=V_{CC}
CLOCK, CLEAR			25	pf	
All Other			10	pf	
POWER SUPPLY CURRENT			100	ma	
A.C. Characteristics					T_A=+25°C
CLOCK					
PW_H	300			ns	
PW_L	600			ns	
Transition, t_r, t_f		0.02	1.0	μs	
Repetition Rate, 1/T	0		1.0	MHz	
t_D Delay	500			ns	
INPUT DATA					
t_D, set-up	150			ns	
t_D, hold	150			ns	
PW_D	300			ns	
OUTPUT DATA					
t_D, ACC		200	350	ns	
RECIRCULATE CONTROL					
t_R, set-up	200			ns	
t_R, hold	300			ns	
PW_R	500			ns	
CLEAR					
PW_{CLEAR}	20			μs	

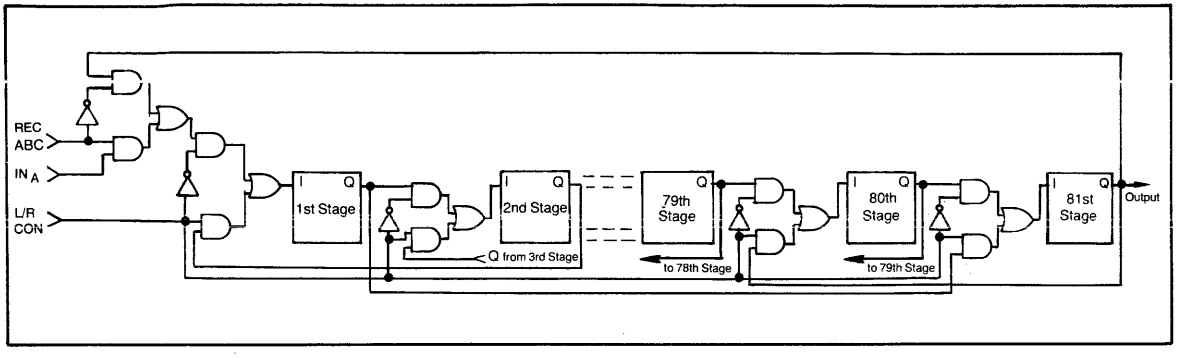
Timing Diagram



Description of Pin Functions

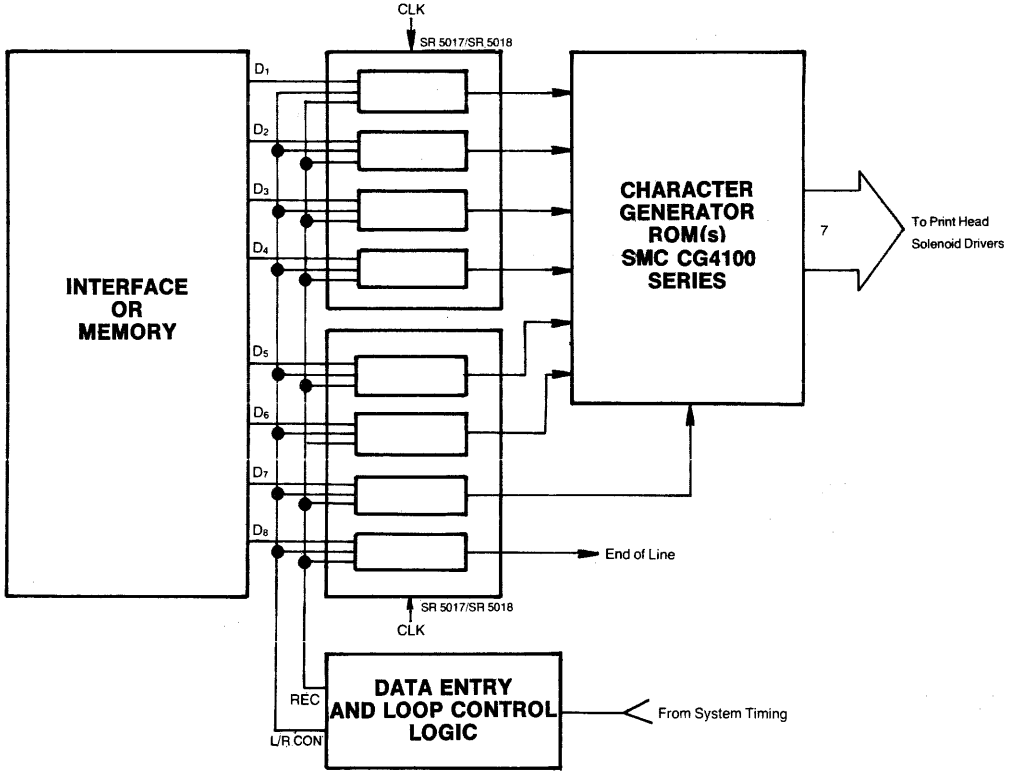
Symbol	Name	Pin	Function
D	Input D	1	Input signal for D register.
RID	Recirculate Input D	2	Input signal which is the input to the D register when recirculate control D is high: RECD = 1.
O_D	Output D	3	Output signal for D register.
CLR	Clear	4	Input signal when high forces outputs to a low state immediately and clears all the registers.
O_A	Output A	5	Output signal for A register.
L/R CON	Shift Left/Shift Right Control	6	Input signal which is low for loading data and for shifting right. When L/R CON is high, the register will shift left.
A	Input A	7	Input signal which is either high or low depending on what word is to be loaded into shift register.
CLK	Clock Input	8	Input signal which is normally low and pulses high to shift data into the registers. The data is clocked in on low to high edge of clock.
V_{CC}	5 Volt	9	5 volt power supply.
RECABC	Recirculate ABC	10	Input signal when high disconnects inputs from registers and connects outputs to inputs, thus recirculating data. Recirculates only A, B, C outputs.
O_B	Output B	11	Output signal for B register.
B	Input B	12	Input signal for B register.
C	Input C	13	Input signal for C register.
O_C	Output C	14	Output signal for C register.
GND	GND	15	Ground.
RECD	Recirculate Control D	16	Input signal which is normally low and, when goes high, disconnects Input D to register and connects RECIRCULATE INPUT D to register.

Logic Diagram



APPLICATION

Line Buffer for Bidirectional Matrix Printer . . . 80/132 characters per line



Keyboard Encoder

Part Number	No. of Keys	Modes	Features	Standard Fonts Suffix	Standard Fonts Description	Power Supplies	Package	Page
KR-2376 XX [1]	88	3	2 Key Rollover	-ST	ASCII	+5, −12	40 DIP	429-432
KR-3600 XX [1]	90	4	2 Key or N Key Rollover	-ST -STD -PRO	ASCII ASCII Binary Sequential	+5, −12	40 DIP	433-440

[1] May be custom mask programmed

STANDARD MICROSYSTEMS CORPORATION

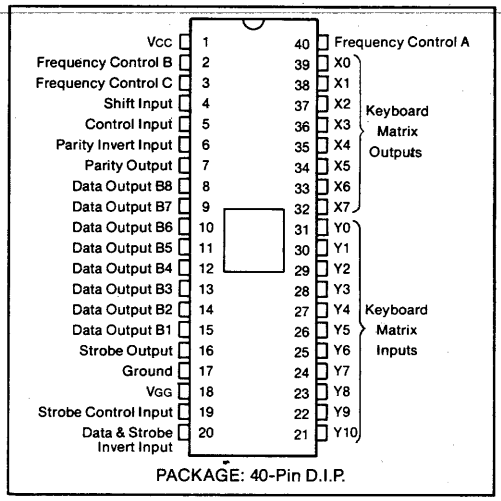
KR2376-XX

Keyboard Encoder Read Only Memory

FEATURES

- ☐ Outputs directly compatible with TTL/DTL or MOS logic arrays.
- ☐ External control provided for output polarity selection.
- ☐ External control provided for selection of odd or even parity.
- ☐ Two key roll-over operation.
- ☐ N-key lockout.
- ☐ Programmable coding with a single mask change.
- ☐ Self-contained oscillator circuit.
- ☐ Externally controlled delay network provided to eliminate the effect of contact bounce.
- ☐ One integrated circuit required for complete keyboard assembly.
- ☐ Static charge protection on all input and output terminals.
- ☐ Entire circuit protected by a layer of glass passivation.

PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

GENERAL DESCRIPTION

The SMC KR2376-XX is a 2376-bit Read Only Memory with all the logic necessary to encode single pole single throw keyboard closures into a usable 9-bit code. Data and strobe outputs are directly compatible with TTL/DTL or MOS logic arrays without the use of any special interface components.

The KR2376-XX is fabricated with low threshold, P-channel technology and contains 2942 P-channel enhancement mode transistors on a single monolithic chip, available in a 40 pin dual-in-line package.

TYPICAL CONNECTION OF KR2376-XX

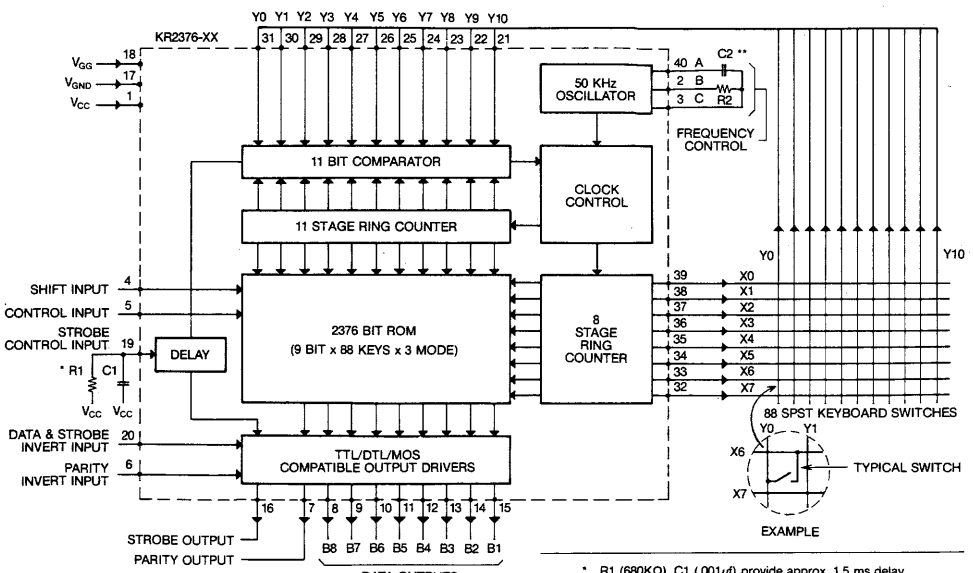


Fig. 1

* R1 (680KΩ), C1 (.001μf) provide approx. 1.5 ms delay (see figure 5)

** R2 (100KΩ), C2 (50pf) provide 50KHz clock frequency (see figure 6)

MAXIMUM GUARANTEED RATINGS†

Operating Temperature Range ..... 0° C to +70° C
Storage Temperature Range ..... −65° C to +150° C
GND and V_{GG}, with respect to V_{CC} ..... −20V to +0.3V
Logic Input Voltages, with respect to V_{CC} ..... −20V to +0.3V

† Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS

(T_A = 0° C to +70° C, V_{CC} = +5V ±0.5V, V_{GG} = −12V ±1.0V, unless otherwise noted)

Characteristics	Min	Typ	Max	Unit	Conditions
CLOCK	20	50	100	KHz	see fig.1 footnote (**) for typical R-C values
DATA INPUT					
Logic "0" Level			+0.8	V	
Logic "1" Level	V_{CC}-1.5			V	
Input Capacitance			10	pf	
INPUT CURRENT					
*Control, Shift & Y0 thru Y10	10	100	140	μA	V_{IN} = +5.0V
*Control, Shift & Y0 thru Y10	5	30	50	μA	V_{IN} = Ground
Data Invert, Parity Invert		.01	1	μA	V_{IN} = −5.0V to +5.0V
DATA OUTPUT & X OUTPUT					
Logic "0" Level			+0.4	V	I_{OL} = 1.6mA (see fig. 7)
Logic "1" Level	V_{CC}-1.0			V	I_{OH} = 100 μA
POWER CONSUMPTION		140	200	mW	Nom. Power Supp. Voltages (see fig. 8)
SWITCH CHARACTERISTICS					
Minimum Switch Closure	see timing diagram-fig. 2				
Contact Closure Resistance between X1 and Y1			300	Ohm	
Contact Open Resistance between X1 and Y1	1×10^7			Ohm	

*Inputs with Internal Resistor to V_{GG}

DESCRIPTION OF OPERATION

The KR2376-XX contains (see Fig. 1), a 2376-bit ROM, 8-stage and 11-stage ring counters, an 11-bit comparator, an oscillator circuit, an externally controllable delay network for eliminating the effect of contact bounce, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 264 by 9-bit memory arranged into three 88-word by 9-bit groups. The appropriate levels on the Shift and Control inputs selects one of the three 88-word groups; the 88-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control inputs with the two ring counters.

The external outputs of the 8-stage ring counter and the external inputs to the 11-bit comparator are wired to the keyboard to form an X-Y matrix with the 88-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM; the absence of a Strobe Output indicates that the Data Outputs are 'not valid' at this time.

When a key is depressed, a single path is completed between one output of the 8-stage ring counter (X0 thru X7) and one input of the 11-bit comparator (Y0-Y10). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 11-stage ring counter. When this occurs, the comparator generates a signal to the clock control and to the Strobe Output (via the delay network). The clock control stops the clocks to the ring counters and the Data Outputs (B1-B9) stabilize with the selected 9-bit code, indicated by a 'valid' signal on the Strobe Output. The Data Outputs remain stable until the key is released.

As an added feature two inputs are provided for external polarity control of the Data Outputs. Parity Invert (pin 6) provides polarity control of the Parity Output (pin 7) while the Data and Strobe Invert Input (pin 20) provides for polarity control of Data Outputs B1 thru B8 (pins 8 thru 15) and the Strobe Output (pin 16).

SPECIAL PATTERNS

Since the selected coding of each key is defined during the manufacture of the chip, the coding can be changed to fit any particular application of the keyboard. Up to 264 codes of up to 8 bits (plus one parity bit) can be programmed into the KR2376-XX ROM covering most popular codes such as ASC11, EBCD1C, Selectric, etc., as well as many specialized codes. The ASC11 code is available as a standard pattern. For special patterns, use Fig. 9.

TIMING DIAGRAM

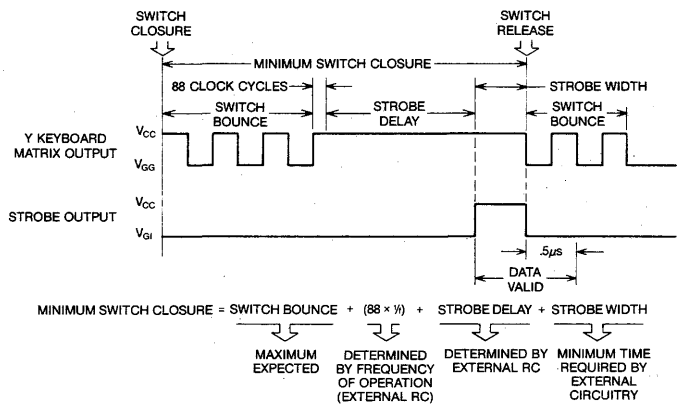
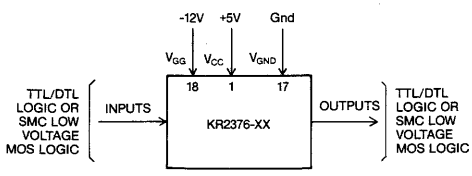


Fig. 2

POWER SUPPLY CONNECTIONS FOR TTL/DTL OPERATION



POWER SUPPLY CONNECTIONS FOR MOS OPERATION

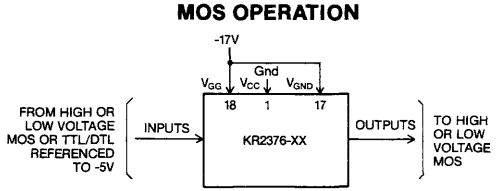
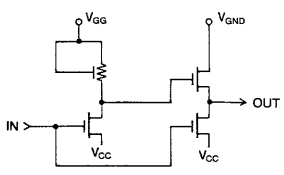


Fig. 3

OUTPUT DRIVER & "X" OUTPUT STAGE TO KEYBOARD



"Y" INPUT STAGE FROM KEYBOARD

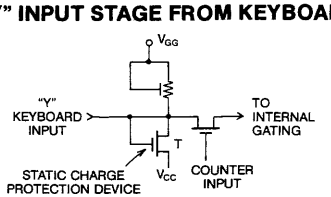


Fig. 4

STROBE DELAY VS. C_1

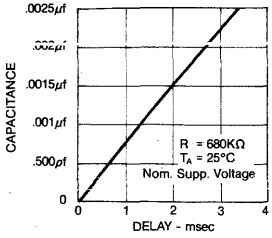


Fig. 5

OSCILLATOR FREQUENCY VS. C_2

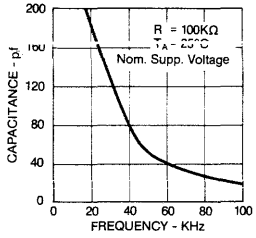


Fig. 6

TYP. OUTPUT ON RESISTANCE VS. GATE BIAS VOLTAGE

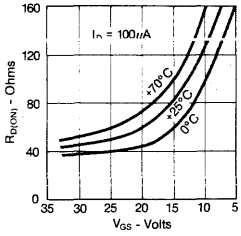


Fig. 7

TYP. POWER CONSUMPTION VS. TEMPERATURE

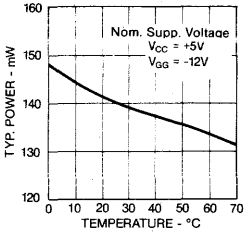


Fig. 8

CODE ASSIGNMENT CHART
KR2376-ST
8 Bit ASCII, odd parity

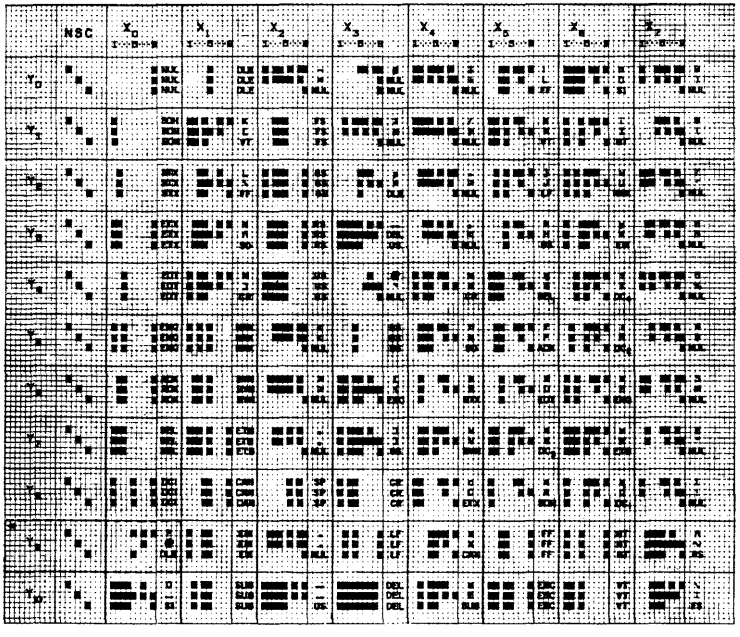


Fig. 9

(Code representative of key depression at location X0-Y9 and proper mode selection)

N = Normal Mode
S = Shift Mode
C = Control Mode
■ = Output Logic "1" (see data B1-B8)
Logic "1" = +5.0V
Logic "0" = Ground

DATA (B1-B8) INVERT TRUTH TABLE

DATA & STROBE INVERT INPUT (Pin 20)	CODE ASSIGNMENT CHART	DATA OUTPUTS (B1-B8)
1	1	0
0	1	1
1	0	1
0	0	0

STROBE INVERT TRUTH TABLE

DATA & STROBE INVERT INPUT (Pin 20)	INTERNAL STROBE	STROBE OUTPUT (Pin 16)
1	1	0
0	0	0
1	0	1
0	1	1

PARITY INVERT TRUTH TABLE

PARITY INVERT INPUT (Pin 6)	CODE ASSIGNMENT CHART	PARITY OUTPUT (Pin 7)
1	1	0
0	1	1
1	0	1
0	0	0

MODE SELECTION

$\overline{S}\,\overline{C}$ = N
S $\overline{C}$ = S
$\overline{S}$ C = C
S C = INVALID (SPURIOUS DATA)

STANDARD MICROSYSTEMS CORPORATION

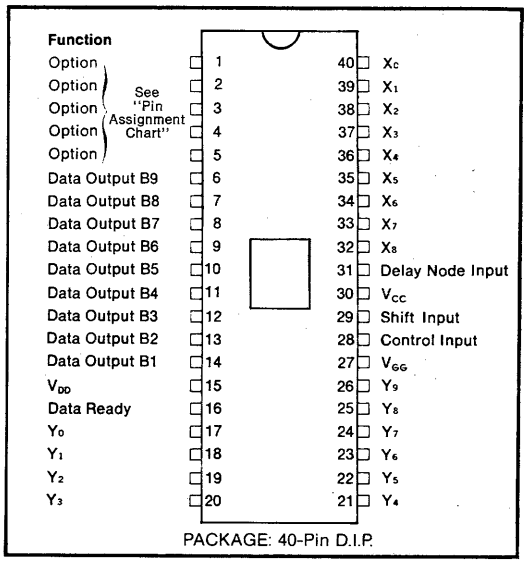
KR3600-XX
KR3600-ST
KR3600-STD
KR3600-PRO

Keyboard Encoder Read Only Memory

FEATURES

- Data output directly compatible with TTL
- N Key rollover or lockout operation
- Quad mode
- Lockout/rollover selection externally selected as option
- On chip-master/slave oscillator
- All 10 output bits available
- Fully buffered data outputs
- Output enable provided as option
- Data compliment control provided as option
- Pulse or level data ready output signal provided as an option
- Any key down output provided as an option
- Contact bounce circuit provided to eliminate contact bounce
- Static charge protection on all input/outputs
- Pin for Pin replacement for GI AY-5-3600

PIN CONFIGURATION



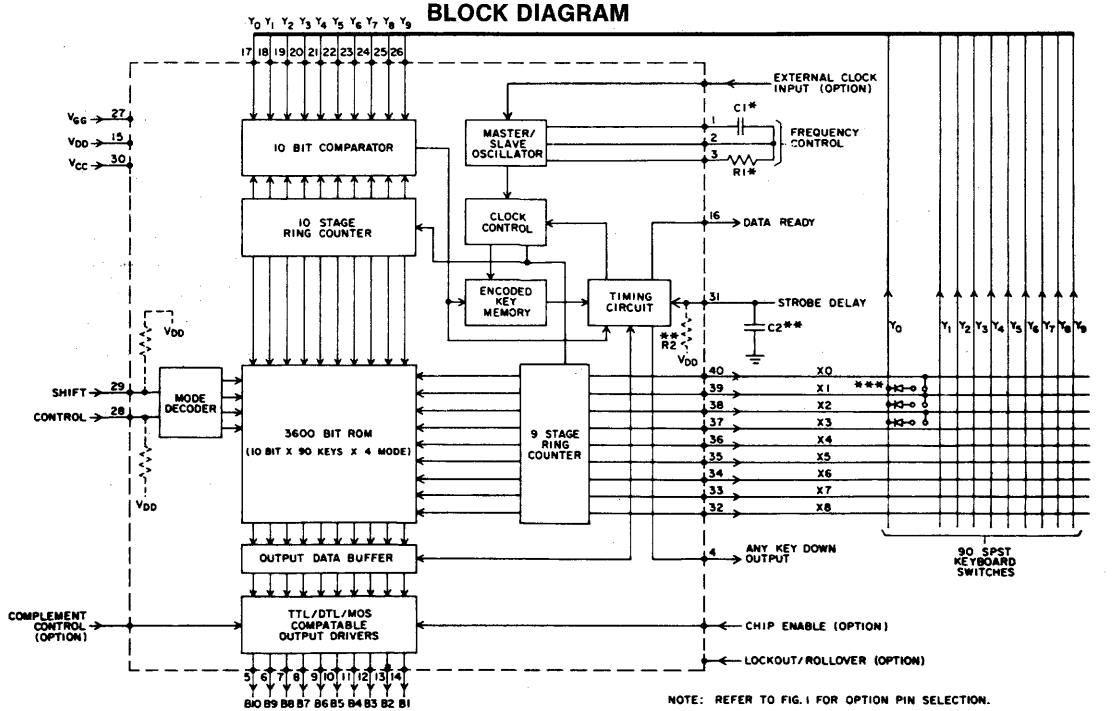
PACKAGE: 40-Pin D.I.P.

GENERAL DESCRIPTION

The SMC Microsystems KR3600-XX is a Keyboard Encoder containing a 3600 bit read only memory and all the logic necessary to encode single pole single throw keyboard closures into a 10 bit code.

The KR3600-XX is fabricated with a low voltage p channel technology and contains the equivalent of 5000 transistors on a monolithic chip in a 40 lead dip ceramic package.

BLOCK DIAGRAM



NOTE: REFER TO FIG. 1 FOR OPTION PIN SELECTION.
*R1 (100KΩ), C1 (45pF) PROVIDES APPROX. 50KHZ CLOCK FREQ.
**C2 (300nS DELAY/CPF) R2 SUPPLIED INTERNALLY.
***DIODES NECESSARY FOR COMPLETE nKEY ROLLOVER OPERATION.

DESCRIPTION OF OPERATION

The KR3600 contains a 3600 bit ROM, 9-stage and 10-stage ring counters, a 10 bit comparator, timing circuitry, a 90 bit memory to store the location of encoded keys for n key rollover operation, an externally controllable delay network for eliminating the effect of contact bounce, an output data buffer, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 360 by 10 bit memory arranged into four 90-word by 10-bit groups. The appropriate levels on the Shift and Control Inputs selects one of the four 90-word groups; the 90-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

The external outputs of the 9-stage ring counter and the external inputs to the 10-bit comparator are wired to the keyboard to form an X-Y matrix with the 90-keyboard switches as the crosspoints. In the standby conditions, when no key is depressed, the two ring counters are clocked and sequentially address the ROM, thereby scanning the key switches for key closures.

When a key is depressed, a single path is completed between one output of the 9-stage ring counter (X0 thru X8) and one input of the 10-bit comparator (Y_0-Y_9). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 10-stage ring counter.

N KEY ROLLOVER — When a match occurs, and the key has not been encoded, the switch bounce delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears, a one is stored in the encoded key memory and the scan sequence is resumed. If a match occurs at another key location, the sequence is repeated thus encoding the next key. If the match occurs for an already encoded key, the match is not recognized. The code of the last key encoded remains in the output data buffer.

N KEY LOCKOUT — When a match occurs, the delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears and the remaining keys are locked out by halting the scan sequence. The scan sequence is resumed upon key release. The output data buffer stores the code of the last key encoded.

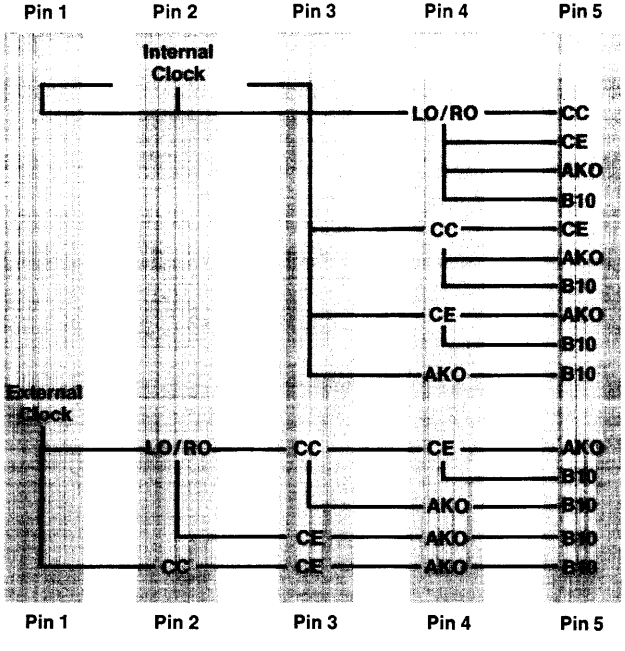
SPECIAL PATTERNS — Since the selected coding of each key and all the options are defined during the manufacture of the chip, the coding and options can be changed to fit any particular application of the keyboard. Up to 360 codes of up to 10 bits can be programmed into the KR3600 ROM covering most popular codes such as ASCII, EBCDIC, Selectric, etc., as well as many specialized codes.

CUSTOM CODING INFORMATION

The custom coding information for SMC's 3600 Bit Keyboard Encoder ROM should be transmitted to SMC. The Truth Table should be completed on the format supplied.

LEGEND

CC = Complement Control
AKO = Any Key Down Output
B10 = B10 (Data) Output
LO/RO = Lockout/Rollover
CE = Chip Enable
Internal Clock = Self Contained Oscillator
External Clock = External Frequency Source



OPTION SELECTION/PIN ASSIGNMENT

FIGURE 1

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, V_{CC}	+0.3 V
Negative Voltage on any Pin, V_{CC}	−25 V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS

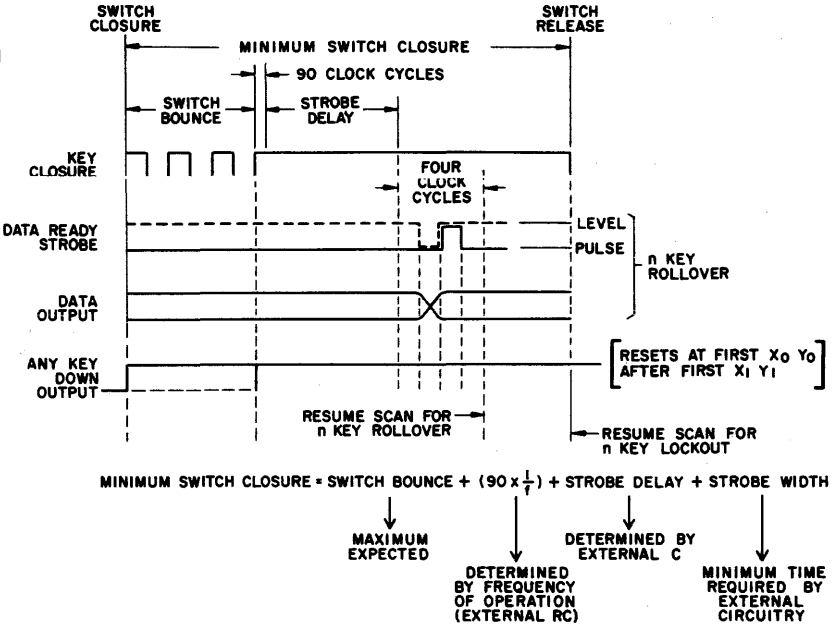
(T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{GG} = −12V ±1.0V, V_{DD} = GND, unless otherwise noted)

Characteristics	Min	Typ**	Max	Units	Conditions
Clock Frequency	10	50	100	KHz	See Block diagram footnote* for typical R-C values
External Clock Width	7	—	—	μs	
Data & Clock Input (Shift, Control, Compliment Control, Lockout/Rollover, Chip Enable & External Clock)					
Logic "0" Level	V_{GG}	—	+0.8	V	
Logic "1" Level	V_{CC}−1.5	—	V_{CC}+0.3	V	
Shift & Control Input Current	75	150	220	μA	V_{IN} = +5V
X Output (X_0-X_8)					
Logic "1" Output Current	40	250	500	μA	V_{OUT} = V_{CC} (See Note 2)
	600	1300	4000	μA	V_{OUT} = V_{CC}−1.3V
	900	2000	6500	μA	V_{OUT} = V_{CC}−2.0V
	1500	2000	14,000	μA	V_{OUT} = V_{CC}−5V
	3000	10,000	23,000	μA	V_{OUT} = V_{CC}−10V
Logic "0" Output Current	8	30	60	μA	V_{OUT} = V_{CC}
	6	25	50	μA	V_{OUT} = V_{CC}−1.3V
	5	20	45	μA	V_{OUT} = V_{CC}−2.0V
	2	10	30	μA	V_{OUT} = V_{CC}−5V
	—	0.5	5	μA	V_{OUT} = V_{CC}−10V
Y Input (Y_0-Y_9)					
Trip Level	V_{CC}−5	V_{CC}−3	V_{CC}−2	V	Y Input Going Positive (See Note 2)
Hysteresis	0.5	0.9	1.4	V	(See Note 1)
Selected Y Input Current	18	100	170	μA	V_{IN} = V_{CC}
	14	80	150	μA	V_{IN} = V_{CC}−1.3V
	13	50	130	μA	V_{IN} = V_{CC}−2.0V
	5	40	110	μA	V_{IN} = V_{CC}−4.0V
Unselected Y Input Current	9	40	80	μA	V_{IN} = V_{CC}
	7	30	70	μA	V_{IN} = V_{CC}−1.3V
	6	25	60	μA	V_{IN} = V_{CC}−2.0V
	3	15	40	μA	V_{IN} = V_{CC}−5V
	—	0.5	20	μA	V_{IN} = V_{CC}−10V
Input Capacitance	—	3	10	pF	at 0V (All Inputs)
Switch Characteristics					
Minimum Switch Closure	—	—	—	—	See Timing Diagram
Contact Closure Resistance	—	—	300	Ω	Z_{CC}
	1 x 10^7	—	—	Ω	Z_{CO}
Strobe Delay					
Trip Level (Pin 31)	V_{CC}−4	V_{CC}−3	V_{CC}−2	V	
Hysteresis	0.5	0.9	1.4	V	(See Note 1)
Quiescent Voltage (Pin 31)	−3	−5	−9	V	With Internal Switched Resistor
Data Output (B1-B10), Any Key Down Output, Data Ready					
Logic "0"	—	—	0.4	V	I_{OL} = 1.6m A
Logic "1"	V_{CC}−1	—	—	V	I_{OH} = 1.0m A
	V_{CC}−2	—	—	V	I_{OH} = 2.2m A
Power					
I_{CC}	—	12	25	mA	V_{CC} = +5V
I_{GG}	—	12	25	mA	V_{GG} = −12V

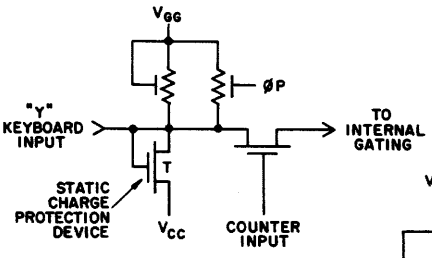
**Typical values are at +25°C and nominal voltages.

NOTE
1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Precharge of X outputs and Y inputs occurs during each scanned clock cycle.

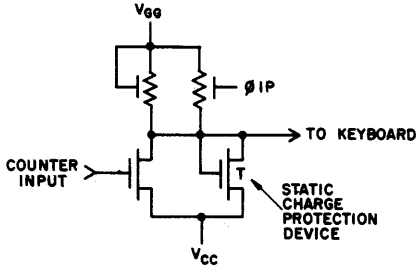
TIMING DIAGRAM



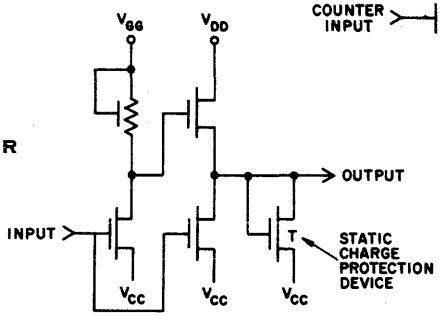
"Y" INPUT STAGE FROM KEYBOARD



"X" OUTPUT STAGE TO KEYBOARD

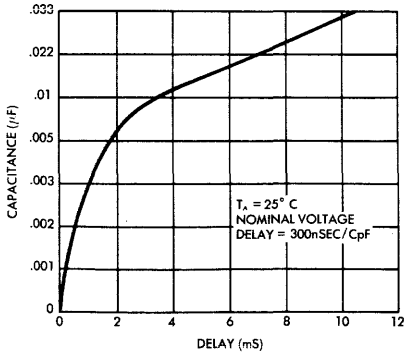


OUTPUT DRIVER

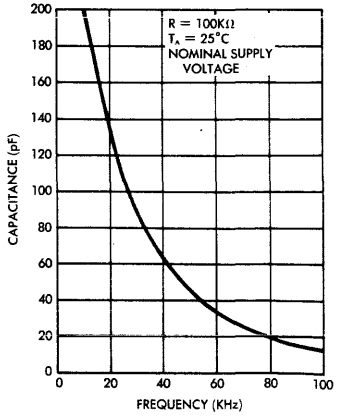


NOTE: Output driver capable of driving one TTL load with no external resistor. Capable of driving two TTL loads using an external 6.8KΩ resistor to V_{GG}

STROBE DELAY vs. C_2



OSCILLATOR FREQUENCY vs. C_1



KR3600-STD

XY	Normal B-12345678910	Shift B-12345678910	Control B-12345678910	Shift Control B-12345678910
00	1 1000111001	< 0011111001	1 1000111011	SUB 0101100001
01	q 1000110101	Q 1000100101	q 1000111111	DLE 0000100001
02	a 1000010101	A 1000000101	a 1000011111	@ 0000000101
03	z 0101110101	Z 0101100101	z 0101111111	P 0000100101
04	HT 1001000001	HT 1001000001	HT 1001000001	I 1001000101
05	H 0001000101	H 0001000101	H 0001000101	H 0001000111
06	+ 1101011001	+ 1101011001	+ 1101011001	+ 1101011011
07	SO 0111001001	> 0111111001	SO 0111000001	SO 0111000011
08	p 0000110101	@ 0000000101	NUL 0000000001	NUL 0000000001
09	1 1000111001	! 1000011001	SOH 1000000001	SOH 1000000001
10	2 0100111001	@ 0000000101	2 0100111011	ETB 1110100001
11	w 1110110101	W 1110100101	w 1110111111	A 0011100101
12	s 1100110101	S 1100100101	s 1100111111	A 1000000101
13	x 0001110101	X 0001100101	x 0001111111	Q 1000100101
14	RS 0111100001	RS 0111100001	RS 0111100001	FS 0011100001
15	% 1010011001	% 1010011001	% 1010011001	% 1010011011
16	m 1011010101	] 1011100101	CR 1011000001	CR 1011000001
17	SI 1111000001	SI 1111000001	SI 1111000001	SI 1111000011
18	n 0111010101	A 0111100101	SO 0111000001	SO 0111000001
19	2 0100111001	" 0100011001	STX 0100000001	STX 0100000001
20	3 1100111001	# 1100011001	3 1100111011	NAK 1010100001
21	e 1010010101	E 1010000101	e 1010011111	DC3 1100100001
22	d 0010010101	D 0010000101	d 0010011111	B 0100000101
23	c 1100010101	C 1100000101	c 1100011111	R 0100100101
24	— 1111100100	— 1111100100	— 1111100100	A 0111100100
25	$ 0010011001	$ 0010011001	$ 0010011001	$ 0010011011
26	L 0011000101	L 0011000101	L 0011000101	L 0011000111
27	US 1111100001	US 1111100001	US 1111100001	US 1111100011
28	6 0110111001	& 0110011001	ACK 0110000001	ACK 0110000001
29	k 1101010101	[1101100101	DEL 1111111101	DEL 1111111101
30	4 0010111001	$ 0010011001	4 0010111011	DC4 0010100001
31	r 0100110101	R 0100100101	r 0100111111	ENQ 1010000001
32	f 0110010101	F 0110000101	f 0110011111	C 1100000101
33	SP 0000011000	SP 0000011000	SP 0000011000	SP 0000011000
34	CAN 0001101000	(0001011000	CAN 0001100000	BS 0001000000
35	CR 1011000001	CR 1011000001	CR 1011000001	M 1011000101
36	[1101111101	[1101111101	[1101111111	K 1101000101
37	VT 1101000000	VT 1101000000	VT 1101000000	VT 1101000010
38	7 1110111001	' 1110011001	BEL 1110000001	BEL 1110000001
39	" 0100011001	" 0100011001	" 0100011001	" 0100011011
40	5 1010111001	% 1010011001	5 1010111011	STX 0100000001
41	t 0010110101	T 0010100101	t 0010111111	EOT 0010000001
42	g 1110010101	g 1110000101	G 1110011111	D 0010000101
43	v 0110110101	V 0110100101	v 0110111111	S 1100100101
44	ETX 1100000001	ETX 1100000001	ETX 1100000001	ETX 1100000001
45	] 1011111101	] 1011111101	] 1011111111	N 0111000101
46	? 1111111001	? 1111111001	? 1111111011	[1101100101
47	— 1011011001	— 1011111001	— 1011011001	— 1011011011
48	) 1001011001	) 1001011001	) 1001011001	) 1001011011
49	SP 0000011001	SP 0000011001	SP 0000011001	SP 0000011011
50	6 0110111001	> 0111111001	6 0110111011	SOH 1000000001
51	y 1001110101	Y 1001100101	y 1001111111	DC1 1000100001
52	h 0001010101	H 0001000101	h 0001011111	E 1010000101
53	b 0100010101	B 0100000101	b 0100011111	T 0010100101
54	: 0101111001	* 0101011001	: 0101111011	SYN 0110100001
55	> 0111111001	> 0111111001	> 0111111011	Z 0101100101
56	; 1101111001	+ 1101011001	; 1101111011	Y 1001100101
57	NUL 0000000001	NUL 0000000001	NUL 0000000001	NUL 0000000001
58	* 0101011001	* 0101011001	* 0101011001	* 0101011011
59	! 1000011001	! 1000011001	! 1000011001	! 1000011011
60	7 1110111001	& 0110011001	7 1110111011	ETX 1100000001
61	u 1010110101	U 1010100101	u 1010111111	BEL 1110000001
62	j 0101010101	J 0101000101	j 0101011111	F 0110000101
63	n 0111010101	N 0111000101	n 0111011111	U 1010100101
64	= 1011111000	= 1011111000	= 1011111010	~ 0111111100
65	< 0011111001	< 0011111001	< 0011111011	W 1110100101
66	p 0000110101	P 0000100101	p 0000111111	J 0101000101
67	0 0000111001	) 1001011001	0 0000111011	DC2 0100100001
68	& 0110011001	& 0110011001	& 0110011001	& 0110011011
69	# 1100011001	# 1100011001	# 1100011001	# 1100011011
70	8 0001111001	* 0101011001	8 0001111011	ESC 1101100001
71	i 1001010101	I 1001000101	i 1001011111	ACK 0110000001
72	k 1101010101	K 1101000101	k 1101011111	G 1110000101
73	m 1011010101	M 1011000101	m 1011011111	V 0110100101
74	/ 1111011001	? 1111111001	/ 1111011001	' 1110011001
75	' 1110011001	" 0100011001	' 1110011001	" 0100011001
76	LF 0101000000	LF 0101000000	LF 0101000000	GS 1011100000
77	= 1011111001	+ 1101011001	= 1011111001	+ 1101011001
78	FF 0011001001	< 0011111001	FF 0011000001	FF 0011000011
79	(0001011001	(0001011001	(0001011001	(0001011011
80	9 1001111001	(0001011001	9 1001111011	EM 1001100001
81	o 1111010101	O 1111000101	o 1111011111	] 1011100101
82	l 0011010101	L 0011000101	l 0011011111	X 0001100101
83	, 0011011001	, 0011011001	, 0011011001	, 0011011011
84	. 0111011001	. 0111011001	. 0111011001	. 0111011011
85	; 1101111001	: 0101111001	; 1101111001	: 0101111001
86	] 1011100101	[1101100101	] 1011100101	[1101100101
87	- 1011011001	— 1111100101	- 1011011001	— 1111100101
88	0 0000111001	0 0000111001	0 0000111001	0 0000111001
89	9 1001111001	) 1001011001	HT 1001000001	HT 1001000001

Options:

Internal oscillator (pins 1, 2, 3)
Any key down (pin 4) positive output
N key rollover only
Pulse data ready signal
Internal resistor to VDD on shift and control pins
KR3600-STD outputs provides ASC II bits 1-6 on B1-B6, and bit 7 on B8

KR 3600-ST

XY	Normal B-123456789	Shift B-123456789	Control B-123456789	Shift/Control B-123456789
00	\ 000001101	- 011111101	NUL 000000001	RS 011110001
01	= 101111010	+ 110101001	GS 101110001	VT 110100010
02	DC3 110010010	DC3 110010010	DC3 110010010	DC3 110010010
03	— 101101001	— 111110101	CR 101100010	US 111110010
04	BS 000100010	BS 000100010	BS 000100010	BS 000100010
05	0 000011001	0 000011001	0 000011001	0 000011001
06	• 011101001	• 011101001	• 011101001	• 011101001
07	000000000	000000000	000000000	000000000
08	000000000	000000000	000000000	000000000
09	000000000	000000000	000000000	000000000
10	/ 111101010	? 111111001	ST 111100001	US 111110010
11	• 011101001	> 011111010	SO 011100010	RS 011110001
12	? 001101010	< 001111001	FF 001100001	FS 001110010
13	m 101101110	M 101100101	CR 101100010	CR 101100010
14	n 011101110	N 011100101	SO 011100010	SO 011100010
15	b 010001110	B 010000101	STX 010000010	STX 010000010
16	v 011011110	V 011010101	SYN 011010010	SYN 011010010
17	c 110001101	C 110000110	ETX 110000001	ETX 110000001
18	x 000111101	X 000110110	CAN 000110001	CAN 000110001
19	z 010111110	Z 010110101	SUB 010110010	SUB 010110010
20	LF 010100001	LF 010100001	LF 010100001	LF 010100001
21	\ 001110101	¦ 001111110	FS 001110010	FS 001110010
22	DEL 111111110	DEL 111111110	DEL 111111110	DEL 111111110
23	[110110110	} 101110110	ESC 110110001	GS 101110001
24	7 111011010	7 111011010	7 111011010	7 111011010
25	8 000111010	8 000111010	8 000111010	8 000111010
26	9 100111001	9 100111001	9 100111001	9 100111001
27	000000000	000000000	000000000	000000000
28	000000000	000000000	000000000	000000000
29	000000000	000000000	000000000	000000000
30	; 110111010	: 010111001	ESC 110110001	SUB 010110010
31	l 001101101	L 001100110	FF 001100001	FF 001100001
32	k 110101110	K 110100101	VT 110100010	VT 110100010
33	j 010101101	J 010100110	LF 010100001	LF 010100001
34	h 000101110	H 000100101	BS 000100010	BS 000100010
35	g 111001110	G 111000101	BEL 111000010	BEL 111000010
36	f 011001101	F 011000110	ACK 011000001	ACK 011000001
37	d 001001110	D 001000101	EOT 001000010	EOT 001000010
38	s 110011110	S 110010101	DC3 110010010	DC3 110010010
39	a 100001110	A 100000101	SOH 100000010	SOH 100000010
40	000000000	000000000	000000000	000000000
41	{ 110111101	} 101111101	ESC 110110001	GS 101110001
42	GR 101100010	GR 101100010	GR 101100010	GR 101100010
43	' 111001001	" 010001001	BEL 111000010	STX 010000010
44	4 001011010	4 001011010	4 001011010	4 001011010
45	5 101011001	5 101011001	5 101011001	5 101011001
46	6 011011001	6 011011001	6 011011001	6 011011001
47	000000000	000000000	000000000	000000000
48	000000000	000000000	000000000	000000000
49	000000000	000000000	000000000	000000000
50	p 000011110	P 000010101	DEL 000010010	DEL 000010010
51	o 111101101	O 111100110	SI 111100001	SI 111100001
52	i 100101101	I 100100110	HT 100100001	HT 100100001
53	u 101011110	U 101010101	NAK 101010010	NAK 101010010
54	y 100111110	Y 100110101	EM 100110010	EM 100110010
55	t 001011101	T 001010110	DC4 001010001	DC4 001010001
56	r 010011101	R 010010110	DC2 010010001	DC2 010010001
57	e 101001101	E 101000110	ENQ 101000001	ENQ 101000001
58	w 111011101	W 111010110	ETB 111010001	ETB 111010001
59	q 100011101	Q 100010110	DC1 100010001	DC1 100010001
60	000000000	000000000	000000000	000000000
61	000000000	000000000	000000000	000000000
62	DC2 010010001	DC2 010010001	DC2 010010001	DC2 010010001
63	000000000	000000000	000000000	000000000
64	1 100011010	1 100011010	1 100011010	1 100011010
65	2 010011010	2 010011010	2 010011010	2 010011010
66	3 110011001	3 110011001	3 110011001	3 110011001
67	000000000	000000000	000000000	000000000
68	000000000	000000000	000000000	000000000
69	000000000	000000000	000000000	000000000
70	0 000011001	) 100101010	DLE 000010010	HT 100100001
71	9 100111001	(000101001	EM 100110010	BS 000100010
72	8 000111010	* 010101010	CAN 000110001	LF 010100001
73	7 111011010	& 011001010	ETB 111010001	ACK 011000001
74	6 011011001	Λ 011110110	SYN 011010010	RS 011110001
75	5 101011001	% 101001010	NAK 101010010	ENQ 101000001
76	4 001011010	$ 001001001	DC4 001010001	EOT 001000010
77	3 110011001	# 110001010	DC3 110010010	ETX 110000001
78	2 010011010	@ 000000110	DC2 010010001	NUL 000000001
79	1 100011010	! 100001001	DC1 100010001	SOH 100000010
80	000000000	000000000	000000000	000000000
81	000000000	000000000	000000000	000000000
82	000000000	000000000	000000000	000000000
83	000000000	000000000	000000000	000000000
84	000000000	000000000	000000000	000000000
85	SP 000001010	SP 000001010	NUL 000000001	NUL 000000001
86	000000000	000000000	000000000	000000000
87	DC1 100010001	DC1 100010001	DC1 100010001	DC1 100010001
88	HT 100100001	HT 100100001	HT 100100001	HT 100100001
89	ESC 110110001	ESC 110110001	ESC 110110001	ESC 110110001

Options: Pin 1, 2, 3—Internal oscillator
Pin 4—Lockout (logic 1), rollover (logic 0)
Pin 5—Any key down output

All outputs complemented
Level data ready

KR 3600-PRO

XY	Normal	Shift	Control	Shift/Control
00	000000000	001000000	010000000	011000000
01	000000001	001000001	010000001	011000001
02	000000010	001000010	010000010	011000010
03	000000011	001000011	010000011	011000011
04	000000100	001000100	010000100	011000100
05	000000101	001000101	010000101	011000101
06	000000110	001000110	010000110	011000110
07	000000111	001000111	010000111	011000111
08	000001000	001001000	010001000	011001000
09	000001001	001001001	010001001	011001001
10	000001010	001001010	010001010	011001010
11	000001011	001001011	010001011	011001011
12	000001100	001001100	010001100	011001100
13	000001101	001001101	010001101	011001101
14	000001110	001001110	010001110	011001110
15	000001111	001001111	010001111	011001111
16	000010000	001010000	010010000	011010000
17	000010001	001010001	010010001	011010001
18	000010010	001010010	010010010	011010010
19	000010011	001010011	010010011	011010011
20	000010100	001010100	010010100	011010100
21	000010101	001010101	010010101	011010101
22	000010110	001010110	010010110	011010110
23	000010111	001010111	010010111	011010111
24	000011000	001011000	010011000	011011000
25	000011001	001011001	010011001	011011001
26	000011010	001011010	010011010	011011010
27	000011011	001011011	010011011	011011011
28	000011100	001011100	010011100	011011100
29	000011101	001011101	010011101	011011101
30	000011110	001011110	010011110	011011110
31	000011111	001011111	010011111	011011111
32	000100000	001100000	010100000	011100000
33	000100001	001100001	010100001	011100001
34	000100010	001100010	010100010	011100010
35	000100011	001100011	010100011	011100011
36	000100100	001100100	010100100	011100100
37	000100101	001100101	010100101	011100101
38	000100110	001100110	010100110	011100110
39	000100111	001100111	010100111	011100111
40	000101000	001101000	010101000	011101000
41	000101001	001101001	010101001	011101001
42	000101010	001101010	010101010	011101010
43	000101011	001101011	010101011	011101011
44	000101100	001101100	010101100	011101100
45	000101101	001101101	010101101	011101101
46	000101110	001101110	010101110	011101110
47	000101111	001101111	010101111	011101111
48	000110000	001110000	010110000	011110000
49	000110001	001110001	010110001	011110001
50	000110010	001110010	010110010	011110010
51	000110011	001110011	010110011	011110011
52	000110100	001110100	010110100	011110100
53	000110101	001110101	010110101	011110101
54	000110110	001110110	010110110	011110110
55	000110111	001110111	010110111	011110111
56	000111000	001111000	010111000	011111000
57	000111001	001111001	010111001	011111001
58	000111010	001111010	010111010	011111010
59	000111011	001111011	010111011	011111011
60	000111100	001111100	010111100	011111100
61	000111101	001111101	010111101	011111101
62	000111110	001111110	010111110	011111110
63	000111111	001111111	010111111	011111111
64	100000000	101000000	110000000	111000000
65	100000001	101000001	110000001	111000001
66	100000010	101000010	110000010	111000010
67	100000011	101000011	110000011	111000011
68	100000100	101000100	110000100	111000100
69	100000101	101000101	110000101	111000101
70	100000110	101000110	110000110	111000110
71	100000111	101000111	110000111	111000111
72	100001000	101001000	110001000	111001000
73	100001001	101001001	110001001	111001001
74	100001010	101001010	110001010	111001010
75	100001011	101001011	110001011	111001011
76	100001100	101001100	110001100	111001100
77	100001101	101001101	110001101	111001101
78	100001110	101001110	110001110	111001110
79	100001111	101001111	110001111	111001111
80	100010000	101010000	110010000	111010000
81	100010001	101010001	110010001	111010001
82	100010010	101010010	110010010	111010010
83	100010011	101010011	110010011	111010011
84	100010100	101010100	110010100	111010100
85	100010101	101010101	110010101	111010101
86	100010110	101010110	110010110	111010110
87	100010111	101010111	110010111	111010111
88	100011000	101011000	110011000	111011000
89	100011001	101011001	110011001	111011001

Options:
Internal oscillator (pins 1, 2, 3)
Lockout/rollover (pin 4), with internal resistor to VDD
Lockout is logic 1
Any key down (pin 5), positive output
Pulse data ready
Internal resistor to VDD on shift & control pins

DESCRIPTION

The KR 3600 PRO is a MOS/LSI device intended to simplify the interface of a microprocessor to a keyboard matrix. Like the other KR 3600 parts, the KR 3600 PRO contains all of the logic to de-bounce and encode keyswitch closures, while providing either a 2-key or N-key rollover.

The output of the KR 3600 PRO is a simple binary code which may be converted to a standard information code by a PROM or directly by a microprocessor. This permits a user maximum flexibility of key layout with simple field programming.

The code in the KR 3600 is shown in Table I. The format is simple: output bits 9, 8, 7, 6, 5, 4 and 1 are a binary sequence. The count starts at X0, Y0 and increments through X0Y1, X0Y2...X8Y9. Bit 9 is the LSB; bit 1 is the MSB.

Bits 2 and 3 indicate the mode as follows:

Bit 2	Bit 3	
0	0	Normal
0	1	Shift
1	0	Control
1	1	Shift Control

For maximum ease of use and flexibility, an internal scanning oscillator is used, with pin selection of N-key lockout (also known as 2-key rollover) and N-key rollover. An "any-key-down" output is provided for such uses as repeat oscillator keying.

Figure 1 shows a PROM-encoded 64 key, 4 mode application, using a 256x8 PROM, and Figure 2 a full 90 key, 4 mode application, utilizing a 512x8 PROM.

If N-key rollover operation is desired, it is recommended that a diode be inserted in series with each switch as shown. This prevents "phantom" key closures from resulting if three or more keys are depressed simultaneously.

FIGURE 1
KR 3600 PRO TYPICAL APPLICATION
64 KEY, 4 MODE

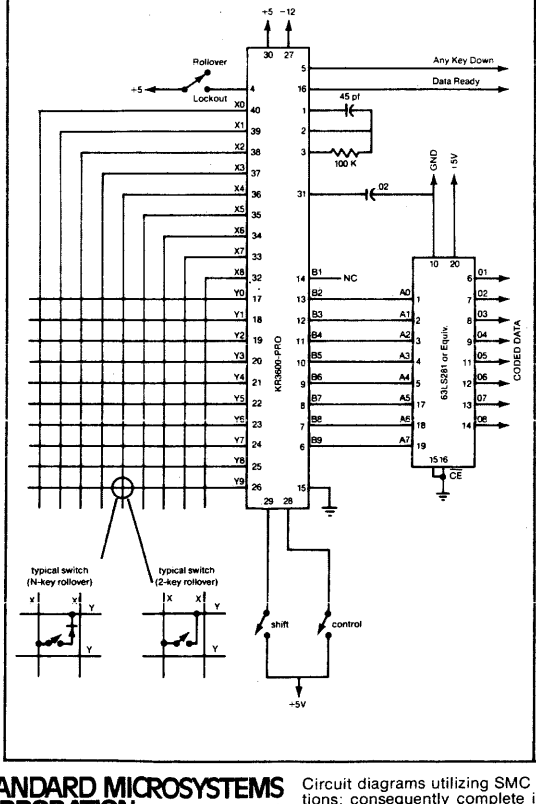
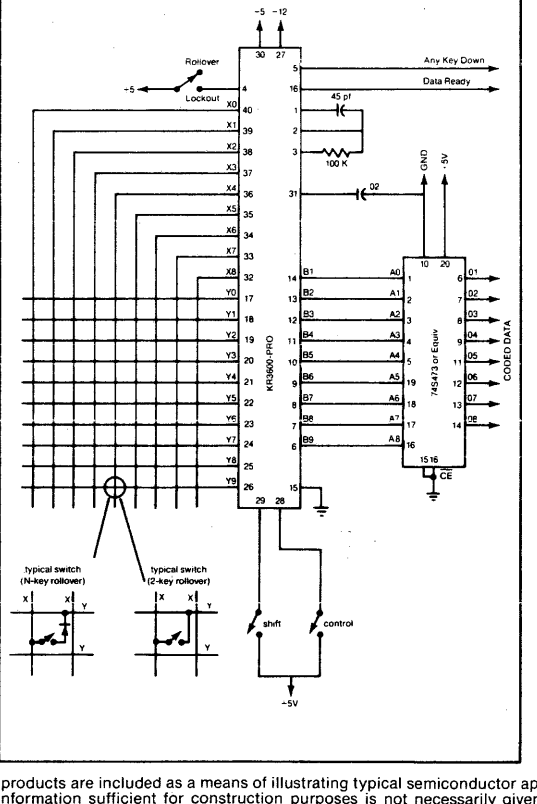


FIGURE 2
KR 3600 PRO TYPICAL APPLICATION
90 KEY, 4 MODE



STANDARD MICROSYSTEMS CORPORATION

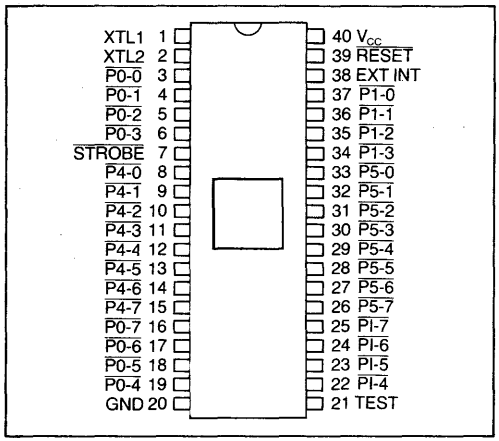
MPU 3870
μPC FAMILY

Single Chip 8-Bit Microcomputer

FEATURES

- ☐ 2K bytes of mask programmable ROM memory
- ☐ 64 bytes of scratch pad RAM
- ☐ 32 bits (4 ports) TTL compatible I/O
- ☐ Programmable binary timer
  - interval timer mode
  - pulse width measurement mode
  - event counter mode
- ☐ External Interrupt Input
- ☐ Crystal, LC, RC, or external time base options
- ☐ Low Power (275 mW typical)

PIN CONFIGURATION



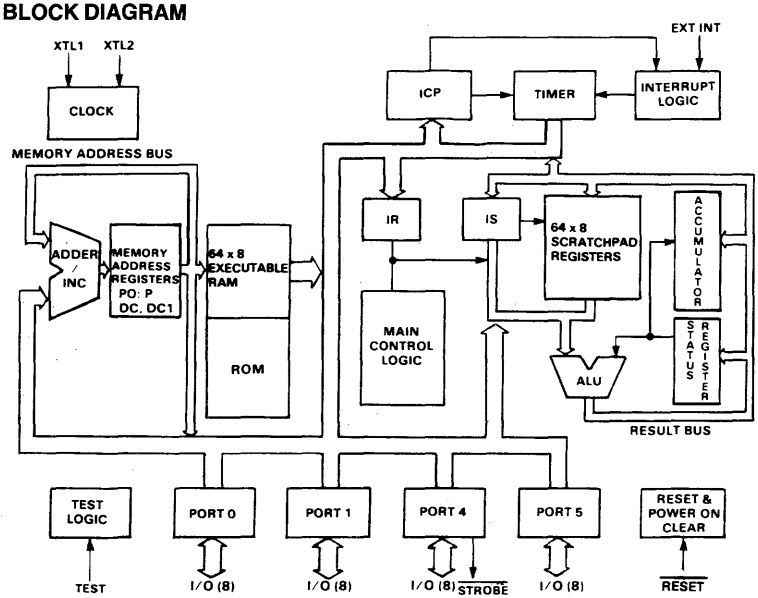
GENERAL DESCRIPTION

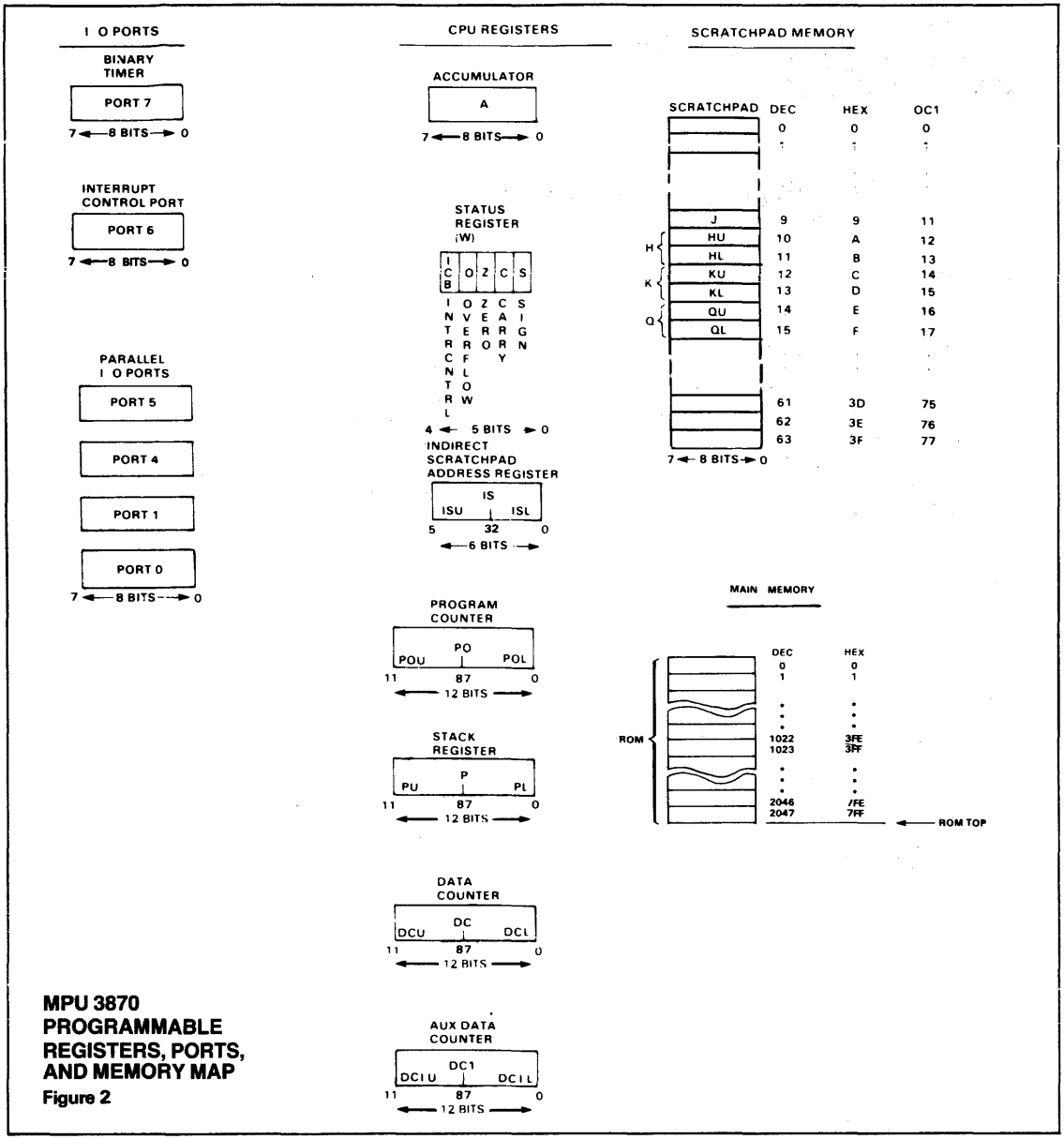
The MPU3870 is a complete 8-bit microcomputer on a single MOS integrated circuit. The MPU3870 can execute a set of more than 70 instructions. The MPU3870 features 2K bytes of ROM, 64 bytes of scratch pad RAM, a programmable binary timer, and 32 bits of I/O.

The programmable binary timer operates by itself in the interval timer mode or in conjunction with the external interrupt input in the pulse width measurement and the event counter modes of operation. Two sources of vectored, prioritized interrupt are provided with the binary timer and the external interrupt input. The user has the option of specifying one of four clock sources: crystal, LC, RC or external clock.

MPU3870 BLOCK DIAGRAM

Figure 1





MPU 3870 PROGRAMMABLE REGISTERS, PORTS, AND MEMORY MAP

Figure 2

MPU3870 MAIN MEMORY

There are four address registers used to access main memory. These are the Program Counter (PO), the Stack Register (P), the Data Counter (DC), and the Auxiliary Data Counter (DC1). The Program Counter is used to address instructions or immediate operands. The Stack Register is used to save the contents of the Program Counter during an interrupt or subroutine call. Thus, the Stack Register contains the return address at which processing is to resume upon completion of the subroutine or interrupt routine. The Data Counter is used to address data tables. The register is auto-incrementing. Of the two data counters, only Data Counter (DC), can access the ROM. However, the XDC instruction allows the Data Counter and Auxiliary Data Counter to be exchanged.

I/O PORTS

The MPU3870 provides four, 8 bit bidirectional Input/Output ports. These are ports 0, 1, 4, 5. In addition, the Interrupt Control Port is addressed as Port 6 and the binary timer is addressed as Port 7. The programming of Ports 6 and 7 and the bidirectional I/O pin are covered in the 3870 Technical Manual. The schematic of an I/O pin and available output drive options are shown in Figure 4.

An output ready strobe is associated with Port 4. This flag may be used to signal a peripheral device that the MPU3870 has just completed an output of new data to Port 4. The strobe provides a single low pulse shortly after the output operation is completely finished, so either edge may be used to signal the peripheral. STROBE may also be used as an input strobe to Port 4 after completing the input operation.

MPU3870 CLOCKS

The time base network used with the MPU3870 may be one of the four different types listed below.

Crystal
LC
RC
External Clock

The type of network which is to be used with the MPU3870 is to be specified at the time when mask ROM MPU3870 devices are ordered. The time base specifications for each of the four modes are covered in the 3870 Technical Manual.

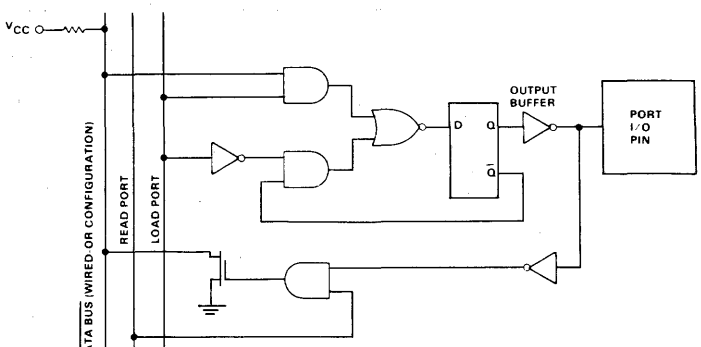
MPU3870 ARCHITECTURE

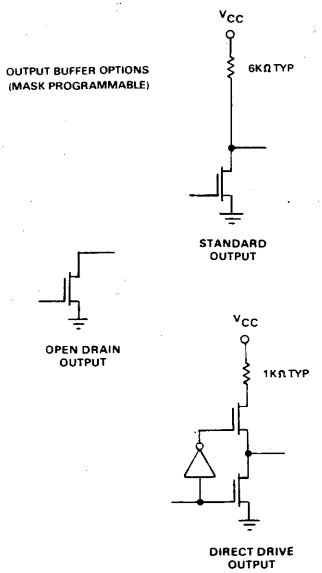
The basic functional elements of the MPU3870 are shown in Figure 1. A programming model is shown in Figure 2. The user is referred to the 3870 Technical Manual for a thorough discussion of the architecture, instruction set, and other features.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	DESCRIPTION	FUNCTION
3-6, 19-16 37-34, 22-25 8-15 33-26	$\overline{P0\text{-}0}$–$\overline{P0\text{-}7}$ $\overline{P1\text{-}0}$–$\overline{P1\text{-}7}$ $\overline{P4\text{-}0}$–$\overline{P4\text{-}7}$ $\overline{P5\text{-}0}$–$\overline{P5\text{-}7}$	I/O Port 0 I/O Port 1 I/O Port 4 I/O Port 5	$\overline{P0\text{-}0}$ through $\overline{P0\text{-}7}$, $\overline{P1\text{-}0}$ through $\overline{P1\text{-}7}$, $\overline{P4\text{-}0}$ through $\overline{P4\text{-}7}$, and $\overline{P5\text{-}0}$ through $\overline{P5\text{-}7}$ are 32 lines which can be individually used as either TTL compatible inputs or as latched outputs.
7	$\overline{\text{STROBE}}$	Ready Strobe	$\overline{\text{STROBE}}$ is a ready strobe associated with I/O Port 4. This output pin, which is normally high, provides a single low pulse after valid data is present on the $\overline{P4\text{-}0}$ through $\overline{P4\text{-}7}$ pins during an output instruction.
38	EXT INT	External Interrupt	EXT INT is the external interrupt input. Its active state is software programmable. This input is also used in conjunction with the timer for pulse width measurement and event counting.
39	$\overline{\text{RESET}}$	External Reset	$\overline{\text{RESET}}$ may be used to externally reset the MK3870. When pulled low the MK3870 will reset. When then allowed to go high the MK3870 will begin program execution at program location H '000'.
1, 2	XTL 1, XTL 2	Time Base	XTL 1 and XTL 2 are the time base inputs to which a crystal, LC network, RC network, or an external single-phase clock may be connected. The time base network must be specified when ordering a mask ROM MK3870. The MK38P70 will operate with any of the four configurations.
21	TEST	Test Line	TEST is an input, used only in testing the MK3870. For normal circuit functionality this pin may be left unconnected, but it is recommended that TEST be grounded.
40	V_{CC}	Power Supply	+5 volt supply pin
20	GND	Ground	Ground

I/O PIN CONCEPTUAL DIAGRAM WITH OUTPUT BUFFER OPTIONS





Ports 0 and 1 are Standard Output type only
Ports 4 and 5 may both be any of the three output options (mask programmable bit by bit)
The $\overline{\text{STROBE}}$ output is always configured similar to a Direct Drive Output except that it is capable of driving 3 TTL loads.
$\overline{\text{RESET}}$ and EXT INT may have standard 6K Ω (typical) pull-up or may have no pull-up (mask programmable).

OPERATING VOLTAGES AND TEMPERATURES

Dash Number Suffix	Operating Voltage V_{CC}	Operating Temperature T_A
—00	+5V ± 10%*	0°C-70°C
—05	+5V ± 5%	0°C-70°C
—10	+5V ± 10%*	−40°C-+85°C
—15	+5V ± 5%*	−40°C-+85°C

See Ordering Information for explanation of part numbers.

ABSOLUTE MAXIMUM RATINGS*

	−00, −05	−10, −15
Temperature Under Bias	−20°C to +85°C	−50°C to +100°C
Storage Temperature	−65°C to +150°C	−65°C to +150°C
Voltage on any Pin With Respect to Ground (Except open drain pins and TEST)	−1.0V to +7V	−1.0V to +7V
Voltage on TEST with Respect to Ground	−1.0V to +9V	−1.0V to +9V
Voltage on Open Drain Pins With Respect to Ground	−1.0V to +13.5V	−1.0V to +13.5V
Power Dissipation	1.5W	1.5W
Power Dissipation by any one I/O pin	60mW	60mW
Power Dissipation by all I/O pins	600mW	600mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC CHARCTERISTICS T_A, V_{CC} within specified operating range. I/O power dissipation ≤100mW (Note 2)

SIGNAL	SYM	PARAMETER	−00, −05 MIN	−00, −05 MAX	−10, −15 MIN	−10, −15 MAX	UNIT	NOTES
XTL1 XTL2	t_o	Timer Base Period, all clock modes	250	500	250	500	ns	4MHz-2MHz
	$t_{ex(H)}$	External clock pulse width high	90	400	100	390	ns	
	$t_{ex(L)}$	External clock pulse width low	100	400	110	390	ns	
Φ	t_Φ	Internal Φ clock	$2t_o$		$2t_o$			
WRITE	t_W	Internal WRITE Clock period	4tΦ 6tΦ		4tΦ 6tΦ			Short Cycle Long Cycle
I/O	$t_{dI/O}$	Output delay from internal WRITE clock	0	100	0	1200	ns	50pF plus one TTL load
	$t_{sI/O}$	Input setup time to intrenal WRITE clock	1000		1200		ns	
$\overline{\text{STROBE}}$	$t_{I/O-s}$	Output valid to $\overline{\text{STROBE}}$ delay	3tΦ −1000	3tΦ +250	3tΦ −1200	3tΦ +300	ns	I/O load = 50pF + 1 TTL load
	t_{sL}	$\overline{\text{STROBE}}$ low time	8tΦ −250	12tΦ +250	8tΦ −300	12tΦ +300	ns	$\overline{\text{STROBE}}$ load = 50pF + 3TTL loads
$\overline{\text{RESET}}$	t_{RH}	$\overline{\text{RESET}}$ hold time, low	6tΦ +750		6tΦ +1000		ns	
	t_{RPOC}	$\overline{\text{RESET}}$ hold time, low for power clear	power supply rise time −0.1		power supply rise time +15		ms	
EXT INT	t_{EH}	EXT INT hold time in active and inactive state	6tΦ +750		6tΦ +1000		ns	To trigger interrupt
			2tΦ		2tΦ		ns	To trigger timer

DC CHARACTERISTICS T_A, V_{CC} within specified operating range I/O power dissipation≤100mW (Note 2)

SYM	PARAMETER	−00, −05		−10, −15		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX		
V_{IHEX}	External Clock input high level	2.4	5.8	2.4	5.8	V	
V_{ILEX}	External Clock input low level	−.3	.6	−.3	.6	V	
I_{IHEX}	External Clock input high current		100		130	μA	$V_{IHEX} = V0_{CC}$
I_{ILEX}	External Clock input low current		−100		−130	μA	$V_{ILEX} = V_{SS}$
$V_{IHI/O}$	Input high level, I/O pins	2.0	5.8	2.0	5.8	V	Standard pull-up
		2.0	13.2	2.0	13.2	V	Open drain (1)
V_{IHR}	Input high level, RESET	2.0	5.8	2.2	5.8	V	Standard pull-up
		2.0	13.2	2.2	13.2	V	No Pull-up
V_{IHEI}	Input high level, EXT INT	2.0	5.8	2.2	5.8	V	Standard pull-up
		2.0	13.2	2.2	13.2	V	No Pull-up
V_{IL}	Input low level	−.3	.8	−.3	.7	V	(1)
I_{IL}	Input low current, all pins with standard pull-up resistor		−1.6		−1.9	mA	$V_{IN} = 0.4V$
I_L	Input leakage current, open drain pins, and inputs with no pull-up resistor		+10 −5		+18 −8	μA μA	$V_{IN} = 13.2V$ $V_{IN} = 0.0V$
I_{OH}	Output high current pins with standard pull-up resistor	−100 −30		−89 −25		μA μA	$V_{OH} = 2.4V$ $V_{OH} = 3.9V$
I_{OHDD}	Output high current, direct drive pins	−100 −1.5	 −8.5	−80 −1.3	 −11	μA mA mA	$V_{OH} = 2.4V$ $V_{OH} = 1.5V$ $V_{OH} = 0.7V$
I_{OHS}	STROBE Output High current	−300		−270		μA	$V_{OL} = 2.4V$
I_{OL}	Output low current	1.8		1.65		mA	$V_{OL} = 0.4V$
I_{OLS}	STROBE Output Low current	5.0		4.5		mA	$V_{OL} = o.4V$
I_{CC}	Average Power Supply Current		85		110	mA	MK3870/20 Outputs Open

TIMER AC CHARACTERISTICS

Definitions:
Error = Indicated time value − actual time value
tpsc = tΦ × Prescale Value

Interval Timer Mode:

Single interval error, free running (Note 3) ..... ±6tΦ
Cumulative interval error, free running (Note 3) 0
Error between two Timer reads (Note 2) ..... ±(tpsc+tΦ)
Start Timer to stop Timer error (Notes 1, 4) ..... +tΦ to − (tpsc+tΦ)
Start Timer to read Timer error (Notes 1, 2) ..... −5tΦ to − (tpsc+7tΦ)
Start Timer to interrupt request error (Notes 1, 3) ..... −2tΦ to −8tΦ
Load Timer to stop Timer error (Note 1) ..... +tΦ to − (tpsc+2tΦ)
Load Timer to read Timer error (Notes 1, 2) ..... −5tΦ ± to − (tpsc + 8tΦ)
Load Timer to interrupt request error (Notes 1, 3) ..... −2tΦ to −9tΦ

Pulse Width Measurement Mode:

Measurement accuracy (Note 4) ..... +tΦ to − (tpsc+2tΦ)
Minimum pulse width of EXT INT pin 2tΦ

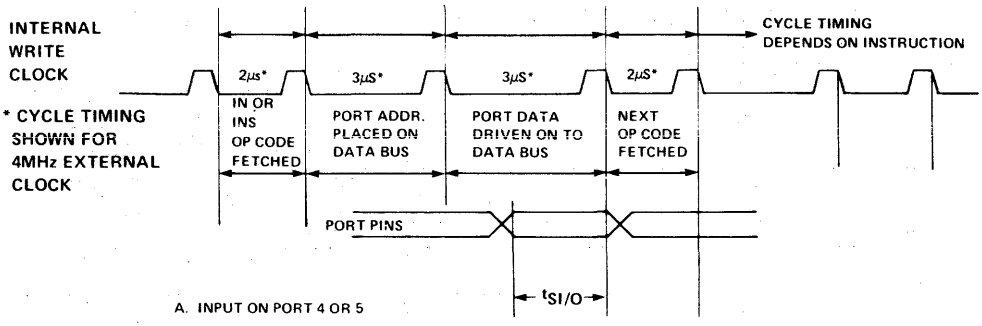
Event Counter Mode:

Minimum active time of EXT INT pin 2tΦ
Minimum inactive time of EXT INT pin 2tΦ

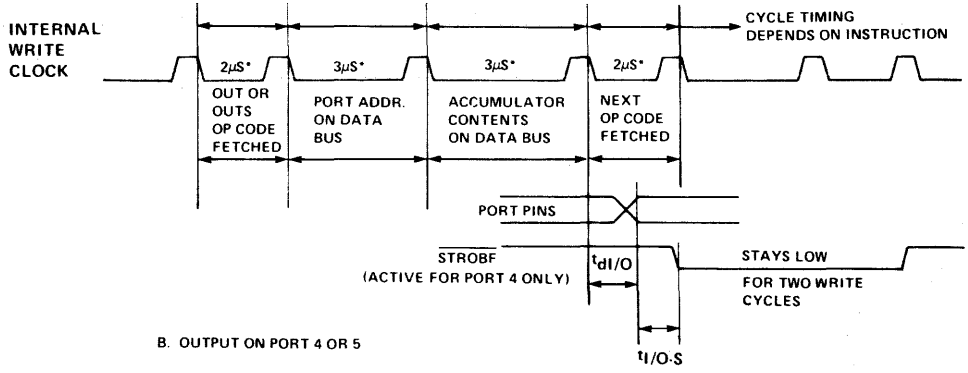
Notes:

1. All times which entail loading, starting, or stopping the Timer are referenced from the end of the last machine cycle of the OUT or OUTS instruction.
2. All times which entail reading the Timer are referenced from the end of the last machine cycle of the IN or INS instruction.
3. All times which entail the generation of an interrupt request are referenced from the start of the machine cycle in which the appropriate interrupt request latch is set. Additional time may elapse if the interrupt request occurs during a privileged or multicycle instruction.
4. Error may be cumulative if operation is repetitively performed.

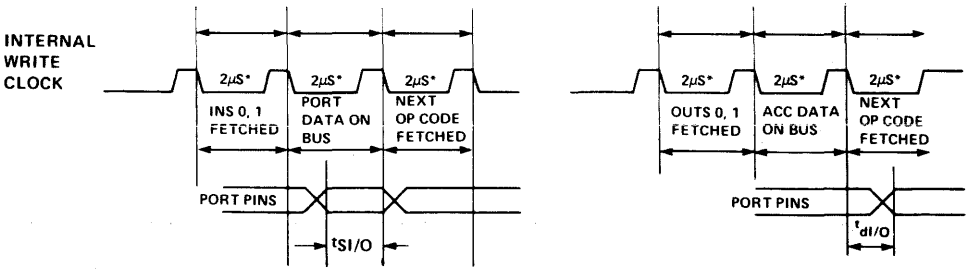
INPUT/OUTPUT AC TIMING



A. INPUT ON PORT 4 OR 5



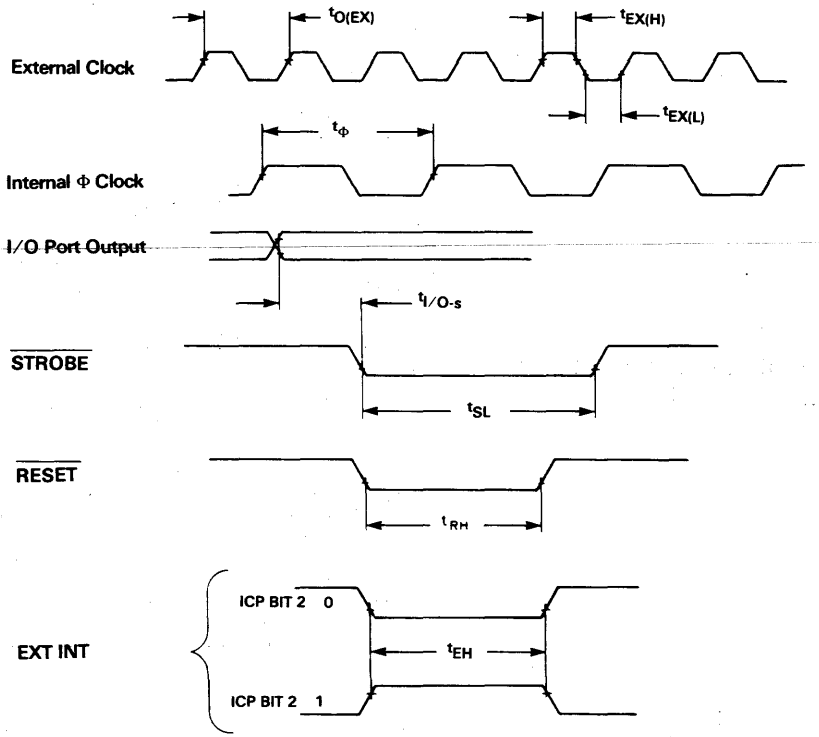
B. OUTPUT ON PORT 4 OR 5



C. INPUT ON PORT 0 OR 1

D. OUTPUT ON PORT 0, 1

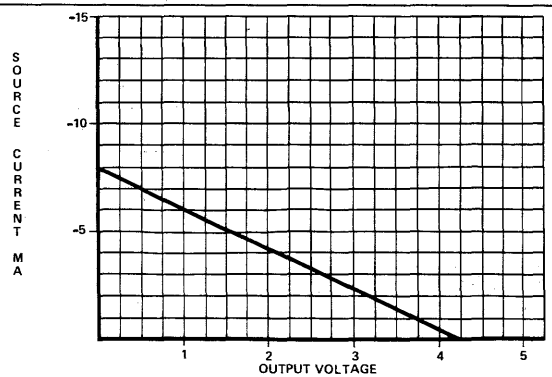
AC TIMING DIAGRAM



Note: All measurements are referenced to V_{IL} max., V_{IH} min., V_{OL} max., or V_{OH} min.

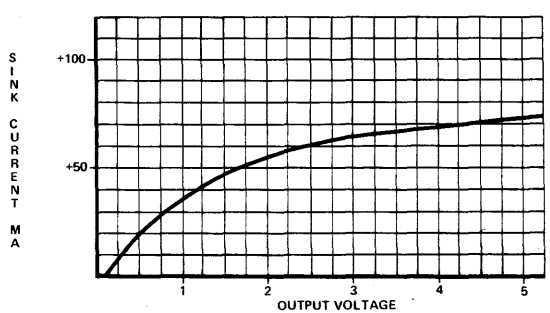
STROBE SOURCE CAPABILITY

(TYPICAL AT V_{CC} = 5V, T_A = 25°C)

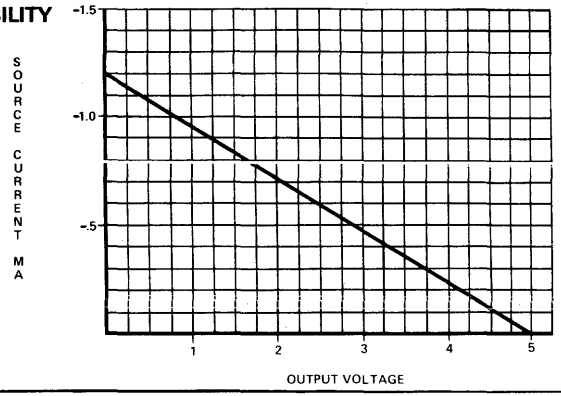


STROBE SINK CAPABILITY

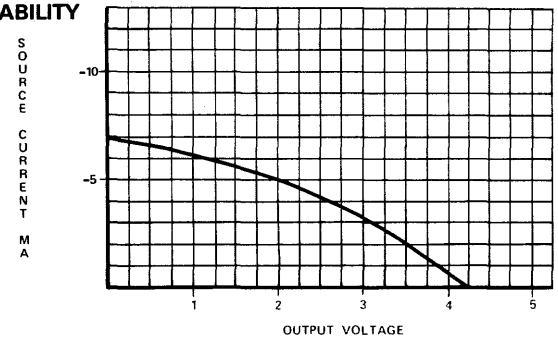
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)



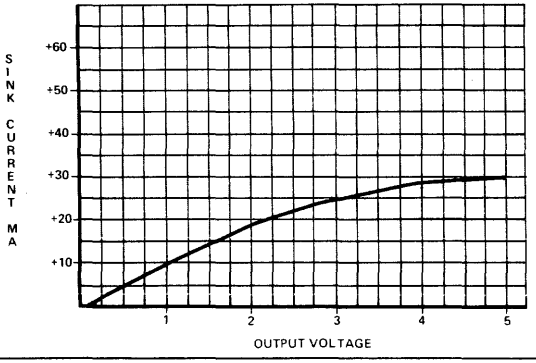
STANDARD I/O PORT SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)



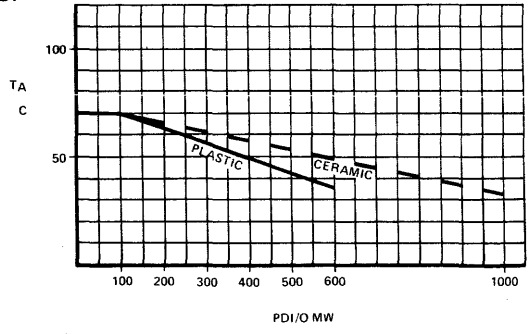
DIRECT DRIVE I/O PORT SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)



I/O PORT SINK CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)



MAXIMUM OPERATING TEMPERATURE VS. I/O POWER DISSIPATION



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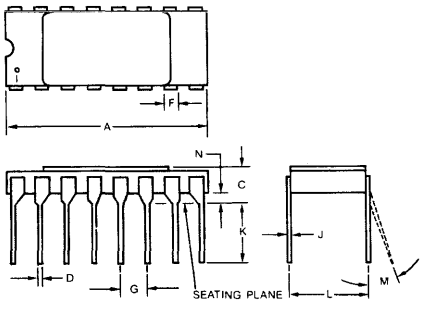
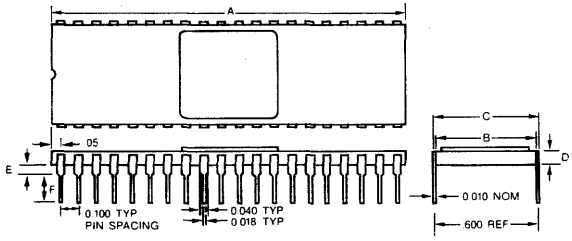
Package Outlines

14, 16, 18, 20 PIN HERMETIC PACKAGE

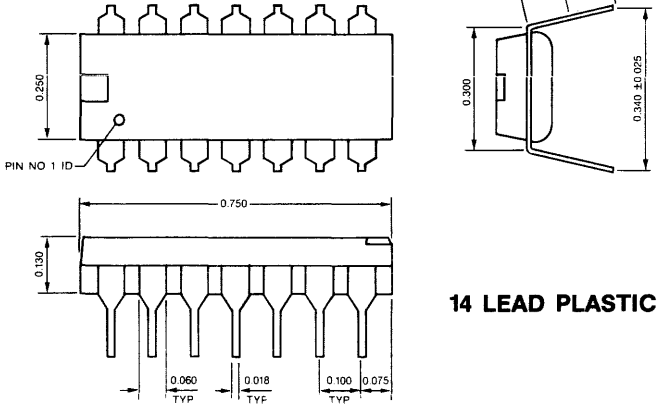


DIM	14 LEAD		16 LEAD		18 LEAD		20 LEAD	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.670	.760	.790	.810	.885	.915	.965	.995
C		.175		.175		.175		.175
D	.015	.021	.015	.021	.015	.021	.015	.021
F	.048	.060	.048	.060	.048	.060	.048	.060
G	.090	.110	.090	.110	.090	.110	.090	.110
J	.008	.012	.008	.012	.008	.012	.008	.012
K	.100		.100		.100		.100	
L	.295	.325	.295	.325	.295	.325	.295	.325
M		10°		10°		10°		10°
N	.025	.060	.025	.060	.025	.060	.025	.060

24, 28, 40 LEAD HERMETIC DIP



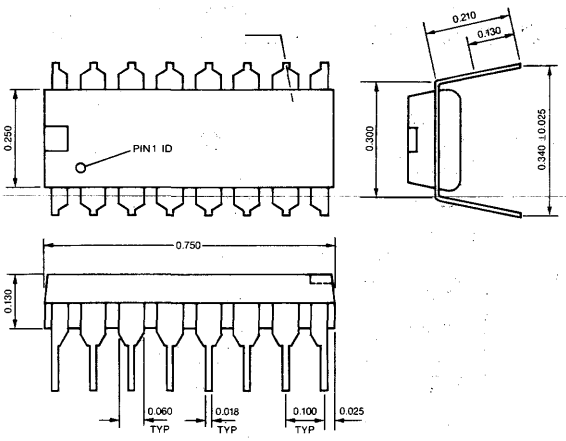
DIM	24 LEAD		28 LEAD		40 LEAD	
	MIN	MAX	MIN	MAX	MIN	MAX
A	1.188	1.212	1.386	1.414	1.980	2.020
B	.568	.598	.568	.598	.568	.598
C	.590	.610	.590	.610	.590	.610
D	.070	.090	.070	.090	.070	.090
E	.025	.060	.025	.060	.025	.060
F	.100		.100		.100	



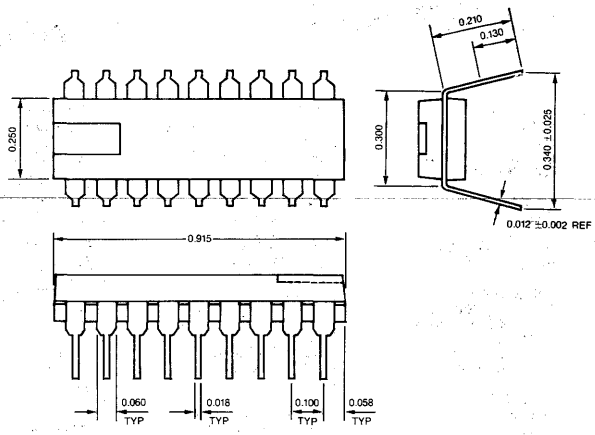
14 LEAD PLASTIC DIP

ALL UNITS INCHES UNLESS OTHERWISE SPECIFIED

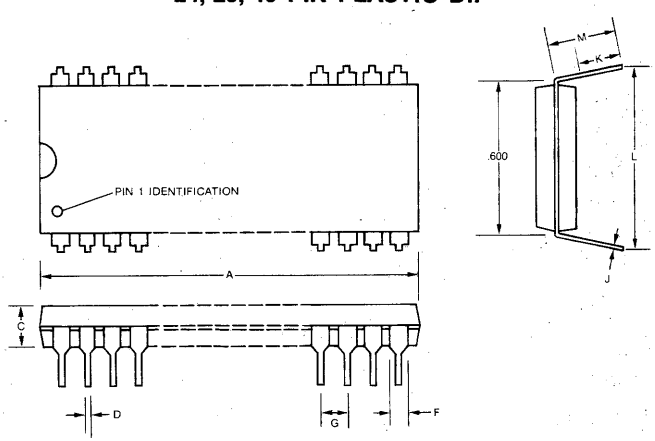
16 LEAD PLASTIC DIP



18 LEAD PLASTIC DIP



24, 28, 40 PIN PLASTIC DIP



DIM	24 LEAD		28 LEAD		40 LEAD	
	MIN	MAX	MIN	MAX	MIN	MAX
A	1.245	1.255	1.445	1.455	2.045	2.055
C	.145	.155	.145	.155	.145	.155
D	.018 TYP		.018 TYP		.018 TYP	
F	.060 TYP		.060 TYP		.060 TYP	
G	.099	.101	.099	.101	.099	.101
J	.010	.014	.010	.014	.010	.014
K	.120		.120		.120	
L	.645	.675	.645	.675	.645	.675
M	.210		.210		.210	

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Wescom Marketing, Inc.
7985 Vance Drive
Suite 102
Arvada, CO 80003
(303) 422-7619

VERMONT
Mill-Bern Assoc., Inc.
120 Cambridge St.
Suite 8
Burlington, MA 01803
(617) 273-1313

VIRGINIA
Robert Electronic Sales
Suite 103
7637 Hull St.
Richmond, VA 23235
(804) 276-3979

AREA SALES MANAGEMENT OFFICES

SMC International
35 Marcus Boulevard
Hauppauge, NY 11788
(516) 273-3100
TWX 510-227-8898
TELEX 221646

EASTERN AREA
35 Marcus Boulevard
Hauppauge, NY 11788
(516) 273-3100
TWX 510-227-8898
TELEX 221646

WESTERN AREA
Turk Enterprises
2172 Dupont Dr., Patio Bldg.
Irvine, Ca 92715
(714) 955-1575
TWX 910-595-2635

SOUTHERN AREA
Microsystems Sales
17070 Dallas Pkwy.
Suite 109
Dallas, TX 75248
(214) 931-5321
TWX 910-860-9269

NO. CENTRAL AREA
Standard Micro Sales, Inc.
P.O. Box 292497
3411 Office Park Drive
Suite 209B
Kettering, OH 45429
(513) 293-5393
TWX 810-459-1617

(West Virginia)
Thompson Associates
23715 Mercantile Rd.
Beachwood, OH 44122
(216) 831-6277
TXW 810 427-9453

WASHINGTON
SDR² Products & Sales Co.
14230 N.E. 8th Street
Bellevue, WA 98007
(206) 747-9424

WASHINGTON D.C.
Robert Electronic Sales
5525 Twin Knolls Rd.
Suite 331
Columbia, MD 21045
(301) 995-1900

WISCONSIN
(East)
Metcom Associates Corp.
237 S. Curtis Rd.
W. Allis, WI 53214
(414) 476-1300

(West)
Quantum Sales
10800 Normandale Blvd.
Bloomington, MN 55437
(612) 884-4700

WYOMING
SDR² Products & Sales Co.
14230 N.E. 8th Street
Bellevue, WA 98007
(206) 747-9424

PUERTO RICO
Mill-Bern Assoc., Inc.
G.P.O. Box 4543
San Juan, Puerto Rico 00936
(809) 792-1541

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AUSTRIA
O. Lackner
Elektron Bauelemente
und Gerate
A-1011 Wien
Singerstr. 2,
1010 Vienna
43-222-531185
TLX: 847111198

AUSTRALIA
Total Electronics
9 Harker St
Burwood, Victoria 3125
(03) 288 4044
TLX: AA 31261

BELGIUM
Auriema, S.A.
Rue Brogniezstraat 172-A
B-1070 Brussels, Belgium
32-2-523-6295
TLX: 84621646

BRAZIL
Filcres
Rua Aurora, 165
CEP 01209
Caixa Postal 18767
Sao Paulo
011-223-7388
TLX: 1131298

CANADA
(Ottawa)
R.F.Q. Ltd.
2249 Carling Ave.
Suite 416
Ottowa, Ontario
Canada K28 7E9
(613) 820-8445
(610) 562-1973

(Toronto)
R.F.Q. Ltd.
385 The West Mall
Suite 251
Etobicoke, Ontario
Canada, M9C 1E7
(416) 626-1445
TWX: (610) 492-2540

DENMARK
Tage Olsen A/S
Ballerup Byvej 222
275D Ballerup
Denmark
45-2-658111
TLX: 85535293

FINLAND
Havulinna
Vitikka 1
02630 ESP00 63
35805281
TLX: 124426

FRANCE
Teklec Airtronic
Cite Des Bruyeres
Rue Carle Vernet
BP2 92310 Sevres
33-1-534-7535
TLX: 204552F

GREAT BRITAIN
Manhattan (Skyline) Ltd.
57 Forlease Rd.
Maidenhead, Berks
United Kingdom 5L6 1RP
44-628-39735
TLX: 851847898

HOLLAND
Auriema Nederland BV
Doornakkersweg 26
5642MP Eindhoven
Nederland
Tel. 31-40-816565
TLX: 84451992

HONG KONG
Protech
Wah Sing St.
Wah Sing Ind. Bldg.
18F, Flat 1
Kwai Chung, N.T. Kowloon
Tel. 12-294721
TLX: 38396 PLTD HX

INDIA
FEGU, Inc.
Electronics Div.
3308 Middlefield Road
Palo Alto, CA 94306
(415) 493-1788
TWX: 345599

ISRAEL
Vectronics, Ltd.
60 Madinat Hayehudim St.
P.O. Box 2024
Herzl ia B46120
052-56070 TLX: 342579

ITALY
Dott. Ing. Guiseppe
De Mico S.P.A.
Viale Vittorio Veneto 8
20060 Cassina De Pecchi
Milano, Italy
02-95-20-551 TLX: 330869

JAPAN
Teijin Advanced Prod. Corp
1-1 Uchisaiwai-Cho
2 Chome, Chiyoda-Ku
Tokyo 100 Japan
506-4670-6 TLX: J23548

NORWAY
National Elektro A/S
Trade Division
Ulvenveien 75
P.O. Box 53, Oekern
N. Oslo, 5, Norway
02-644970 TLX: 71265

SOUTH AFRICA
Eagle Electric
31-41 Hout Street
Capetown 8000
Republic of South Africa
451421
TLX: 960570713

SOUTH KOREA
Kortronics Enterprise
Rm 201-202, 18-Dong,
C-Block
#604-1,Guro-Dong,Guro-Gu
Seoul
634-5497
TLX: MICROSK28484

SPAIN
Amitron S.A.
Loeches, 6
Madrid 8, Spain
34-1-2485863
TLX: 83145550

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FAR EAST
SMC International
6F-1, 323
Jing Ping Road
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Taipei, Taiwan
R.O.C.
02-946-9666
TLX: 31310 HSI SHEMG

SWEDEN
NAXAB
Box 4115
17104 Soina, Sweden
08-98-51-40 TLX: 17912

SWITZERLAND
Datacomp AG
Zurchestr 20
CH-8952 Schlieren, Zurich
41-1-7302165 TLX: 854553533

TAIWAN
Multitech Int'l Corp.
977 Min Shen E. Road
Taipei 105 Taiwan R.O.C.
02-769-1225 TLX: 23756

WEST GERMANY
Tekelec Airtronic Gmbh
Nussbaumstraße 4
8000 Munchen 2
89-594621 TLX: 05-22241

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ARIZONA
Cetec Moltronics
3617 N. 35th Ave.
Phoenix, AZ 85017
(602) 272-7951

Kachina Electronic Dist.
1425 N. 27th Lane
Phoenix, AZ 85009
(602) 269-6201

Kachina Electronic Dist.
920 W. Grant Road
Tucson, AZ 85705
(602) 792-2223

CALIFORNIA
Cetec Moltronics
5610 E. Imperial Hwy.
South Gate, CA 90280
(213) 773-6521
(714) 521-7412

Cetec Moltronics
721 Charcot Ave.
San Jose, CA 95121
(408) 263-7373

Cetec Moltronics
3940 Ruffin Rd.
San Diego, CA 92123
(714) 278-5020

Diplomat Electronics, Inc.
1283F Mt. View-Alviso Rd.
Sunnyvale, CA 94086
(408) 734-1900

Diplomat/Westates Elec.
3001 Redhill Ave.
Bldg. 3-108
Costa Mesa, CA 92626
(714) 549-8401

Diplomat/Westates Elec.
20151 Bahama St.
Chatsworth, CA 91311
(213) 341-4411

Diplomat/Westates Elec.
9787 Aero Drive
San Diego, CA 92123
(714) 292-5693

NESCO
P.O. Box 7840
Van Nuys, CA 91409
(800) 423-2664

NESCO
1651 E. Edinger Ave.
Suite 108
Santa Ana, CA 92705
(714) 541-6181

Western Micro Sales
10040 Bubb Road
Cupertino, CA 95014
(408) 725-1660

COLORADO
Bell Industries
Electronic Distributor Div.
8155 W. 48th Ave.
Wheatridge, CO 80033
(303) 424-1985

Diplomat Electronics, Inc.
96 Iverness Dr., East
Unit R
Englewood, CO 80112
(303) 740-8300

A.C.T.—Rocky Mountain
4016 Youngfield Street
Wheatridge, CO 80033
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Diplomat Electronics, Inc.
52 Federal Road
Danbury, CT 06810
(203) 797-9674

J.V. Electronics, Inc.
690 Main Street
East Haven, CT 06512
(203) 469-2321

Milgray/Connecticut
378 Boston Post Road
Orange, CT 06477
(203) 795-0711

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2120 Calumet St.
Clearwater, FL 33515
(813) 443-4514

Diplomat Electronics, Inc.
115 Palm Bay Road
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Palm Bay, FL 32905
(305) 725-4520

Milgray/Florida, Inc.
1850 Lee Rd., Suite 104
Winter Park, FL 32789
(305) 647-5747
(800) 327-5262

Components South
2500 N.W. 16th Lane
Pompano Beach, FL 33067
(305) 971-0350
(800) 432-4898

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6659 Peachtree Ind. Blvd.
Suite B
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(404) 449-4133

Milgray/Atlanta
17 Dunwoody Park,
Suite 102
Atlanta, GA 30338
(404) 393-9666
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ILLINOIS
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1071 Judson St.
Bensenville, IL 60106
(312) 595-1000

Mar-Con
4836 Main Street
Skokie, IL 60076
(312) 675-6450

Semiconductor Spec. Inc.
195 Spangler Ave.
Elmhurst Indus. Park
Elmhurst, IL 60126
(312) 279-1000

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6901 West 63rd St.
Overland Park, KS 66202
(913) 236-8800

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9150 Rumsey Rd., Suite A6
Columbia, MD 21045
(301) 995-1226

Milgray/Washington
11820 Parklawn Dr.
Rockville, MD 20852
(301) 468-6400
(800) 638-6656

Whitney Distributors, Inc.
6707 Whitestone Road
Baltimore, MD 21207
(301) 944-8080

Resco/Baltimore
1026 Cromwell Bridge Rd.
Baltimore, MD 21204
(301) 823-0070
TWX 710-232-1819

Resco/Washington
10523 Ewing Rd.
Beltsville, MD 20705
(301) 937-9100

MASSACHUSETTS
Diplomat Electronics, Inc.
Kuniholm Drive
Holliston, MA 01746
(617) 429-4120

JV Elec. of Boston Inc.
207A Cambridge St.
Burlington, MA 01803
(617) 273-4300

Milgray/New England
79 Terrace Hall Ave.
Burlington, MA 01803
(617) 272-6800

RC Components
10 Cornell Place
Wilmington, MA 01887
(617) 657-4310

MINNESOTA
The Joel Company
8836 7th Ave. North
Minneapolis, MN 55427
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Semiconductor Spec. Inc.
1701 E. 79th St.
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Bloomington, MN 55420
(612) 854-8841

MISSOURI
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3805 N. Oak Trafficway
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382 Franklin Ave.
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3002 Greentree
Executive Campus
Marlton, NJ 08053
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110 Marcus Dr.
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(516) 454-6400

Diplomat Electronics
4610 Wetzel Road
Liverpool, NY 13088
(315) 652-5000

Current Components
215 Marcus Blvd.
Hauppauge, NY 11788
(516) 273-2600

ADD Electronics
7 Adler Drive
E. Syracuse, NY 13057
(315) 437-0300

Milgray Electronics, Inc.
191 Hanse Ave.
Freeport, NY 11520
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57 Monroe Ave.
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435 Dayton St.
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(800) 321-0006
(800) 362-2808

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Quality Components
9934 E. 21st St.
Tulsa, OK 74129
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Salt Lake City, UT 84121
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SECTION X

STANDARD MICROSYSTEMS CORPORATION

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