



**1967-68**

**INTEGRATED  
CIRCUITS  
CATALOG**

**TEXAS INSTRUMENTS  
INCORPORATED**



## Notes on This First Edition

This first edition of TI's Integrated Circuits catalog contains currently published data sheets covering SOLID CIRCUIT® semiconductor networks. As new data sheets are published, they will be distributed for insertion in the appropriate sections of this basic Tightleaf® catalog.

**This catalog replaces** collections of loose integrated circuits data sheets. Many of the data sheets in this book have been revised, and therefore cancel and supersede earlier editions.

**Please give your present collection** to a co-worker who can make use of it; the largest part of the old data is still current.

**Note that certain large blocks of page numbers have intentionally been omitted,** to permit simplified numbering of insert pages.

**To insert pages: Turn to colored page, Page 1251.**

# 1967-8

## TEXAS INSTRUMENTS

### INTEGRATED CIRCUITS CATALOG

#### CONTENTS

	Page
How to Use the Indexes	2
<b>Table of Data Sheet Contents</b>	<b>3</b>
Integrated Circuits Selection Guides	4
Numeric Index	6
Data Sheets	1001
<b>How to Insert Pages</b>	<b>1251</b>
Interface Components	9501



**TEXAS INSTRUMENTS**  
INCORPORATED  
SEMICONDUCTOR-COMPONENTS DIVISION  
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

## HOW TO USE THE INDEXES

If you know only the **category of device**,  
look in the **Table of Data Sheet Contents**, page **3**.

If you know only the **device number**,  
look in the **Numeric Index**, page **6**.

**The first page of a data sheet is always a right-hand page.**

## INTEGRATED CIRCUIT SELECTION GUIDES

For assistance in selecting devices to meet your requirements,  
use the **Selection Guides**, pages **4** and **5**.

## SPECIAL INFORMATION

TI Field Sales Office Addresses	page 7
TI Authorized Distributor Addresses	page 8
TI Microlibrary Information	page 4512



# TABLE OF DATA SHEET CONTENTS

(Updated with each mailing of new data sheets)

## Full Military Temperature Range Digital Circuits

### Transistor-Transistor-Logic (TTL) -55°C to 125°C

	Page
<b>SERIES 54</b>	1001
SN5400	Quadruple 2-Input Positive NAND Gate 1005
SN5410	Triple 3-Input Positive NAND Gate 1006
SN5420	Dual 4-Input Positive NAND Gate 1007
SN5430	8-Input Positive NAND Gate 1008
SN5440	Dual 4-Input Positive NAND Buffer 1009
SN5450	Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate 1010
SN5451	Dual 2-Wide 2-Input AND-OR-INVERT Gate 1010
SN5453	Expandable 4-Wide 2-Input AND-OR-INVERT Gate 1012
SN5454	4-Wide 2-Input AND-OR-INVERT Gate 1012
SN5460	Dual 4-Input Expander 1014
SN5470	J-K Flip-Flop 1015
SN5472	J-K Master-Slave Flip-Flop 1018
SN5473	Dual J-K Master-Slave Flip-Flop 1021
SN5474	Dual D-Type Edge-Triggered Flip-Flop 1024
SN5480	Gated Full Adder 1027

<b>SERIES 54 930</b>	1501
SN54 930	Dual 4-Input Positive NAND Gate 1502
SN54 932	Dual 4-Input Positive NAND Buffer 1502
SN54 946	Quadruple 2-Input Positive NAND Gate 1502
SN54 948	Master-Slave Flip-Flop 1503
SN54 962	Triple 3-Input Positive NAND Gate 1502
SN54 965	8-Input Positive NAND Gate 1502
SN54 966	Dual 2-Wide 2-Input AND-OR-INVERT Gate 1502

### Modified Diode-Transistor Logic (Modified DTL) -55°C to 125°C

<b>SERIES 53</b>	2001
SN5300	J-K Flip-Flop With Preset 2005
SN5301	J-K Flip-Flop With Preset and Clear 2007
SN5302	Dual J-K Flip-Flop With Preset 2009
SN5304	Dual J-K Flip-Flop With Preset and Clear 2011
SN5310	5-Input Expandable NAND/NOR Gate 2013
SN5311	Dual 5-Input NAND/NOR Gate 2015
SN5315	10-Input Expandable NAND/NOR Gate 2016
SN5320	5-Input Expandable AND/OR Gate (Also Usable as 5-Input Expander) 2018
SN5330	Dual 3-Input NAND/NOR Gate 2020
SN5331	Triple 3-Input NAND/NOR Gate 2021
SN5340	Dual AND/OR Gate 2023
SN5350	Quadruple Inverter/Driver 2024
SN5360	Quadruple 2-Input NAND/NOR Gate 2025
SN5370	Dual AND-OR-INVERT Gate 2026
SN5380	ONE-SHOT Monostable Multivibrator 2027

### Diode-Transistor Logic (DTL) -55°C to 125°C

<b>SERIES 15 930</b>	3001
SN15 930	Dual 4-Input NAND/NOR Gate 3005
SN15 931	Flip-Flop With Set and Clear 3007
SN15 932	Dual 4-Input NAND/NOR Buffer 3009
SN15 933	Dual 4-Input Expander 3011
SN15 944	Dual 4-Input NAND/NOR Power Gate 3012
SN15 945	Flip-Flop With Set and Clear 3014
SN15 946	Quadruple 2-Input NAND/NOR Gate 3017
SN15 948	Flip-Flop With Set and Clear 3019
SN15 950	Pulse-Triggered Binary 3022
SN15 951	Monostable Multivibrator 3024
SN15 962	Triple 3-Input NAND/NOR Gate 3026

\*Operating free-air temperature range of -55°C to 70°C and operating case temperature range of -55°C to 100°C

†Operating free-air temperature range of -55°C to 100°C and operating case temperature range of -55°C to 125°C

## Full Military Temperature Range Linear Circuits

<b>SERIES 52 (-55°C to 125°C)</b>	4001
SN521A	General-Purpose Operational Amplifier 4001
SN522A	
SN523A	
SN5231L	General-Purpose Differential Amplifier 4009
SN524A	General-Purpose Operational Amplifier 4013
SN524AL	
SN525	General-Purpose Differential Amplifier 4017
SN526	General-Purpose Differential Amplifier 4023
<b>SERIES 55 (-55°C to 125°C)</b>	4501
SN5500	Sense Amplifier With One-Shot Output 4501
SN5510*	Wideband Video Amplifier 4505
SN5510L†	

## Industrial Temperature Range Digital Circuits

### Transistor-Transistor Logic (TTL) 0°C to 70°C

<b>SERIES 74</b>	5001
SN7400	Quadruple 2-Input Positive NAND Gate 5005
SN7410	Triple 3-Input Positive NAND Gate 5006
SN7420	Dual 4-Input Positive NAND Gate 5007
SN7430	8-Input Positive NAND Gate 5008
SN7440	Dual 4-Input Positive NAND Buffer 5009
SN7450	Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate 5010
SN7451	Dual 2-Wide 2-Input AND-OR-INVERT Gate 5010
SN7453	Expandable 4-Wide 2-Input AND-OR-INVERT Gate 5012
SN7454	4-Wide 2-Input AND-OR-INVERT Gate 5012
SN7460	Dual 4-Input Expander 5014
SN7470	J-K Flip-Flop 5015
SN7472	J-K Master-Slave Flip-Flop 5018
SN7473	Dual J-K Master-Slave Flip-Flop 5021
SN7474	Dual D-Type Edge-Triggered Flip-Flop 5024
SN7480	Gated Full Adder 5027

<b>SERIES 74 930</b>	5501
SN74 930	Dual 4-Input Positive NAND Gate 5502
SN74 932	Dual 4-Input Positive NAND Buffer 5502
SN74 946	Quadruple 2-Input Positive NAND Gate 5502
SN74 948	Master-Slave Flip-Flop 5503
SN74 962	Triple 3-Input Positive NAND Gate 5502
SN74 965	8-Input Positive NAND Gate 5502
SN74 966	Dual 2-Wide 2-Input AND-OR-INVERT Gate 5502

<b>SERIES 74N</b>	6001
SN7400N	Quadruple 2-Input Positive NAND Gate 6002
SN7410N	Triple 3-Input Positive NAND Gate 6002
SN7420N	Dual 4-Input Positive NAND Gate 6002
SN7430N	8-Input Positive NAND Gate 6002
SN7440N	Dual 4-Input Positive NAND Buffer 6003
SN7450N	Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate 6003
SN7451N	Dual 2-Wide 2-Input AND-OR-INVERT Gate 6003
SN7453N	Expandable 4-Wide 2-Input AND-OR-INVERT Gate 6003
SN7454N	4-Wide 2-Input AND-OR-INVERT Gate 6003
SN7460N	Dual 4-Input Expander 6003
SN7470N	J-K Flip-Flop 6004
SN7472N	J-K Master-Slave Flip-Flop 6004
SN7473N	Dual J-K Master-Slave Flip-Flop 6005
SN7474N	Dual D-Type Edge-Triggered Flip-Flop 6005
SN7480N	Gated Full Adder 6006

### Modified Diode-Transistor Logic (Modified DTL) 0°C to 70°C

<b>SERIES 73</b>	6501
SN7300	J-K Flip-Flop With Preset 6505
SN7301	J-K Flip-Flop With Preset and Clear 6507
SN7302	Dual J-K Flip-Flop With Preset 6509
SN7304	Dual J-K Flip-Flop With Preset and Clear 6511
SN7310	5-Input Expandable NAND/NOR Gate 6513

	Page
SN7311 Dual 5-Input NAND/NOR Gate	6515
SN7315 10-Input Expandable NAND/NOR Gate	6516
SN7320 5-Input Expander	6517
SN7330 Dual 3-Input NAND/NOR Gate	6518
SN7331 Triple 3-Input NAND/NOR Gate	6519
SN7350 Quadruple Inverter/Driver	6520
SN7360 Quadruple 2-Input NAND/NOR Gate	6521
SN7370 Dual AND-OR-INVERT Gate	6522
SN7380 ONE-SHOT Monostable Multivibrator	6523

### Diode-Transistor Logic (DTL) 0°C to 75°C

<b>SERIES 15 830</b>	7001
SN15 830 Dual 4-Input NAND/NOR Gate	7005
SN15 831 Flip-Flop With Set and Clear	7007
SN15 832 Dual 4-Input NAND/NOR Buffer	7009
SN15 833 Dual 4-Input Expander	7011
SN15 844 Dual 4-Input NAND/NOR Power Gate	7012
SN15 845 Flip-Flop With Set and Clear	7014
SN15 846 Quadruple 2-Input NAND/NOR Gate	7017
SN15 848 Flip-Flop With Set and Clear	7019
SN15 850 Pulse-Triggered Binary	7022
SN15 851 Monostable Multivibrator	7024
SN15 862 Triple 3-Input NAND/NOR Gate	7026
<b>SERIES 15 830N (0°C to 75°C)</b>	7501
SN15 830N Dual 4-Input NAND/NOR Gate	7503
SN15 831N Flip-Flop With Set and Clear	7502

SN15 832N Dual 4-Input NAND/NOR Buffer	7503
SN15 833N Dual 4-Input Expander	7503
SN15 844N Dual 4-Input NAND/NOR Power Gate	7503
SN15 845N Flip-Flop With Set and Clear	7502
SN15 846N Quadruple 2-Input NAND/NOR Gate	7503
SN15 848N Flip-Flop With Set and Clear	7502
SN15 850N Pulse-Triggered Binary	7502
SN15 851N Monostable Multivibrator	7504
SN15 862N Triple 3-Input NAND/NOR Gate	7503

### Industrial Temperature Range Linear Circuits

<b>SERIES 72 (0°C to 70°C)</b>	8001
SN723 General-Purpose Differential Amplifier	8001
SN7231L General-Purpose Differential Amplifier	8005
SN724 } General-Purpose Operational Amplifier	8009
SN724L }	
<b>SERIES 75 (0°C to 70°C)</b>	8501
SN7500 Sense Amplifier With One-Shot Output	8504
SN7501 Sense Amplifier With Flip-Flop Output	8506
SN7502 Sense Amplifier With One-Shot Output	8508
<b>Experimental Circuits</b>	<b>9001</b>
<b>SNX1304 Optoelectronic Pulse Amplifier</b>	<b>9001</b>
<b>Interface Components</b>	<b>9501</b>

## DIGITAL INTEGRATED CIRCUITS SELECTION GUIDE

TYPICAL CHARACTERISTICS			TEMPERATURE RANGE	TYPE OF LOGIC	LOGIC FAMILY	CATALOG PAGE
PROPAGATION DELAY TIME	POWER DISSIPATION (each gate)	NOISE IMMUNITY				
<b>HIGH SPEED — HIGH A-C AND D-C NOISE MARGINS</b>						
13 ns	10 mW	1000 mV	-55°C to 125°C	TTL	Series 54	1001
13 ns	10 mW	1000 mV	-55°C to 125°C	TTL	Series 54 930	1501
13 ns	10 mW	1000 mV	0°C to 70°C	TTL	Series 74	5001
13 ns	10 mW	1000 mV	0°C to 70°C	TTL	Series 74 930	5501
<b>MEDIUM SPEED — HIGH D-C NOISE MARGIN</b>						
25 ns	8 mW	750 mV	-55°C to 125°C	DTL	Series 15 930	3001
25 ns	8 mW	750 mV	0°C to 75°C	DTL	Series 15 830	7001
<b>ECONOMICAL PLUG-IN PACKAGE</b>						
13 ns	10 mW	1000 mV	0°C to 70°C	TTL	Series 74N	6001
25 ns	8 mW	750 mV	0°C to 75°C	DTL	Series 15 830N	7501
<b>MODIFIED DTL</b>						
30 ns	10 mW	300 mV	-55°C to 125°C	Modified DTL	Series 53	2001
30 ns	10 mW	300 mV	0°C to 70°C	Modified DTL	Series 73	6501

# LINEAR INTEGRATED CIRCUITS SELECTION GUIDE

## DIFFERENTIAL/OPERATIONAL AMPLIFIERS

PARAMETER	TYPE	SN521A	SN522A	SN523A	SN5231L	SN524A	SN524AL	SN525	SN526	SN5510	SN5510L	SN723	SN7231L	SN724	SN724L	UNIT
$A_{vs}$	Open-loop voltage gain	62	62	72	63	90	66	40	69	61						dB
BW	Bandwidth (−3 dB)	50	50	180	140	45	120	40,000	150	140						kHz
$Z_{in}$	Input impedance	—	—	15	1,000	140	1,000	6	10	800						k $\Omega$
$C_{in}$	Input capacitance	—	—	55	60	250	50	7	55	60						pF
$V_{DI}$	Differential-input offset voltage	1	1	2.2	12	1	3	3	4	15						mV
$I_{DI}$	Differential-input offset current	0.2	0.2	0.5	0.02	0.016	0.006	3	1	0.044						$\mu$ A
$\alpha_{VDI}$	Differential-input offset voltage temperature coefficient	8	8	9	25	5	10	10	10	30						$\mu$ V/deg
$V_{CMIM}$	Maximum common-mode input voltage range	$\pm 3$	$\pm 3$	$\pm 5$	$\pm 5$	$\pm 7$	$\pm 7$	$\pm 1$	$\pm 5$	$\pm 5$						V
$V_{CMO}$	Common-mode output offset voltage	0.5	0.5	0.5	—	0.25	0.22	3.1	0.6	—						V
$Z_{out}$	Output impedance	10,000	160	200	200	10,000	—	35	250	300						$\Omega$
$V_{OM}$	Maximum peak-to-peak output voltage	8.2	5.4	24	15	18	11.7	4.0	20	12						V
CMRR	Common-mode rejection ratio	60	60	90	55	100	77	85	80	55						dB
$P_T$	Total power dissipation	28	72	100	120	100	132	165	100	120						mW
$I_{in}$	Input current	2	2	5	0.08	0.45	0.05	40	6.5	0.11						$\mu$ A
	<b>CATALOG PAGE</b>	4001	4001	4005 4009	4013	4017	4023	4505	8001 8005	8009						

## SENSE AMPLIFIERS

PARAMETER	TYPE	SN5500	SN7500	SN7501	SN7502	UNIT
$V_T$	Differential-input threshold voltage	17	17	17	21	mV
$V_{CMF}$	Common-mode input firing voltage	2	2	2	2.5	V
$V_{out(1)}$	Logical 1 output voltage	3.2	3.2	3.2	3.2	V
$V_{out(0)}$	Logical 0 output voltage	0.2	0.2	0.2	0.2	V
$I_{in(1)}$	Logical 1 level input current (strobe or reset)	1.2	1.2	—	—	mA
$I_{in(0)}$	Logical 0 level input current (strobe or reset)	—	—	−1.1	−1.1	mA
$Z_{inD}$	Differential-input impedance	0.2	0.2	5	5	k $\Omega$
$I_{CC1}$	$V_{CC1}$ supply current	15	15	18	15	mA
$I_{CC2}$	$V_{CC2}$ supply current	−10	−10	−10	−8	mA
$I_{ref}$	$V_{ref}$ supply current	—	—	2.5	2.5	mA
$t_{cyc(min)}$	Minimum cycle time	1.5	1.5	0.7	1.5	$\mu$ s
	<b>CATALOG PAGE</b>	4501	8504	8506	8508	



# NUMERIC INDEX

(Updated with each mailing of new data sheets)

This index is presented for the user who is not familiar with the "series system" of designating integrated circuits. It is therefore arranged in strict ascending numerical order, disregarding letter prefixes and series relationships.

	page		page		page
Series 52	4001	<b>5500</b>		<b>15 800</b>	
Series 53	2001	SN5500	4501	Series 15 830	7001
Series 54	1001	SN5510	4505	Series 15 830N	7501
Series 55	4501	SN5510L	4505	SN15 830	7005
Series 72	8001			SN15 830N	7503
Series 73	6501	<b>7200</b>		SN15 831	7007
Series 74	5001	SN7231L	8005	SN15 831N	7502
Series 74N	6001	<b>7300</b>		SN15 832	7009
Series 75	8501	SN7300	6505	SN15 832N	7503
<b>500</b>		SN7301	6507	SN15 833	7011
SN521A	4003	SN7302	6509	SN15 833N	7503
SN522A	4003	SN7304	6511	SN15 844	7012
SN523A	4007	SN7310	6513	SN15 844N	7503
SN524A	4015	SN7311	6515	SN15 845	7014
SN524AL	4015	SN7315	6516	SN15 845N	7502
SN525	4019	SN7320	6517	SN15 846	7017
SN526	4025	SN7330	6518	SN15 846N	7503
<b>700</b>		SN7331	6519	SN15 848	7019
SN723	8001	SN7350	6520	SN15 848N	7502
SN724	8009	SN7360	6521	SN15 850	7022
SN724L	8009	SN7370	6522	SN15 850N	7502
<b>1300</b>		SN7380	6523	SN15 851	7024
SNX1304	9001	<b>7400</b>		SN15 851N	7504
<b>5200</b>		SN7400	5005	SN15 862	7026
SN5231L	4011	SN7400N	6002	SN15 862N	7503
<b>5300</b>		SN7410	5006		
SN5300	2005	SN7410N	6002	<b>15 900</b>	
SN5301	2007	SN7420	5007	Series 15 930	3001
SN5302	2009	SN7420N	6002	SN15 930	3005
SN5304	2011	SN7430	5008	SN15 931	3007
SN5310	2013	SN7430N	6002	SN15 932	3009
SN5311	2015	SN7440	5009	SN15 933	3011
SN5315	2016	SN7440N	6003	SN15 944	3012
SN5320	2018	SN7450	5010	SN15 945	3014
SN5330	2020	SN7450N	6003	SN15 946	3017
SN5331	2021	SN7451	5010	SN15 948	3019
SN5340	2023	SN7451N	6003	SN15 950	3022
SN5350	2024	SN7453	5012	SN15 951	3024
SN5360	2025	SN7453N	6003	SN15 962	3026
SN5370	2026	SN7454	5012	<b>54 900</b>	
SN5380	2027	SN7454N	6003	Series 54 930	1501
<b>5400</b>		SN7460	5014	SN54 930	1502
SN5400	1005	SN7460N	6003	SN54 932	1502
SN5410	1006	SN7470	5015	SN54 946	1502
SN5420	1007	SN7470N	6004	SN54 948	1503
SN5430	1008	SN7472	5018	SN54 962	1502
SN5440	1009	SN7472N	6004	SN54 965	1502
SN5450	1010	SN7473	5021	SN54 966	1502
SN5451	1010	SN7473N	6005	<b>74 900</b>	
SN5453	1012	SN7474	5024	Series 74 930	5501
SN5454	1012	SN7474N	6005	SN74 930	5502
SN5460	1014	SN7480	5027	SN74 932	5502
SN5470	1015	SN7480N	6006	SN74 946	5502
SN5472	1018	<b>7500</b>		SN74 948	5503
SN5473	1021	SN7500	8504	SN74 962	5503
SN5474	1024	SN7501	8506	SN74 962	5502
SN5480	1027	SN7502	8508	SN74 965	5502
				SN74 966	5502
				<b>Interface Components</b>	<b>9501</b>

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3240 Hillview Drive  
Stanford Industrial Park/DA 1-5373  
Palo Alto, California 94304

TI SUPPLY COMPANY  
1651 Tenth Street/393-6733  
Santa Monica, California 90404

### COLORADO

NEWARK-DENVER ELECTRONIC  
SUPPLY CORP.  
2170 South Grape Street/757-3351  
Denver, Colorado 80222

### FLORIDA

ELECTRONIC WHOLESALERS, INC.  
345 Graham Avenue/841-1550  
Orlando, Florida 32814  
9390 N.W. 27th Avenue/OX 6-1620  
Miami, Florida 33147

### GEORGIA

ACK SEMICONDUCTORS INC.  
554 Deering, N.W./873-5246  
Atlanta, Georgia 30309

### ILLINOIS

ALLIED ELECTRONICS CORPORATION  
100 North Western Avenue/TA 9-9100  
Chicago, Illinois 60680

MERQUIP ELECTRONICS, INC.  
4939 North Elston Avenue/AV 2-5400  
Chicago, Illinois 60630

NEWARK ELECTRONICS CORPORATION  
500 North Pulaski Road/638-4411  
Chicago, Illinois 60624

### INDIANA

RADIO DISTRIBUTING COMPANY  
812 North Senate Avenue/ME 7-5571  
Indianapolis, Indiana 46206

### IOWA

DEECO, INC.  
618 First Street, N.W./EM 5-7751  
Cedar Rapids, Iowa 72405

### LOUISIANA

ELECTRONIC PRODUCTS CORPORATION  
3622 Toulouse Street/HU 6-3777  
New Orleans, Louisiana 70119

### MARYLAND

ELECTRONIC WHOLESALERS, INC.  
3004 Wilkens Avenue/WI 5-3400  
Baltimore, Maryland 21223

MILGRAY/WASHINGTON  
5133 Lawrence Place/864-6330  
Hyattsville, Maryland 20781

### MASSACHUSETTS

DEMAMBRO ELECTRONICS  
1095 Commonwealth Avenue/783-1200  
Boston, Massachusetts 02215

TI SUPPLY COMPANY  
480 Neponset Road/828-5020  
Canton, Massachusetts 02021

LAFAYETTE INDUSTRIAL ELECTRONICS  
1400 Worcester Road/969-6100  
Natick, Massachusetts 01710

### MICHIGAN

NEWARK-DETROIT ELECTRONICS, INC.  
20700 Hubbell Avenue/UN 1-6700  
Detroit, Michigan 48237

NEWARK-INDUSTRIAL  
ELECTRONICS CORP.  
2114 South Division/CH 1-5695  
Grand Rapids, Michigan 49507

### MINNESOTA

STARK ELECTRONIC SUPPLY CO.  
112 Third Avenue N/FE 2-1325  
Minneapolis, Minnesota 55401

### MISSOURI

TI SUPPLY COMPANY  
1660 Broadway/HA 1-5670  
Kansas City, Missouri 64108

ELECTRONIC COMPONENTS FOR  
INDUSTRY  
2605 South Hanley Road/MI 7-5505  
St. Louis, Missouri 63144

### NEW JERSEY

GENERAL RADIO SUPPLY COMPANY, INC.  
600 Penn Street/WO 4-8560  
Camden, New Jersey 08102

TI SUPPLY COMPANY  
U. S. Highway #22  
Post Office Box 366/687-0213  
Union, New Jersey 07083

LAFAYETTE INDUSTRIAL ELECTRONICS  
24 Central Avenue/MI 3-6868  
Newark, New Jersey 07102

### NEW MEXICO

KIERULFF ELECTRONICS, INC.  
6405 Acoma Road, S.E./AM 8-3901  
Albuquerque, New Mexico 87108

### NEW YORK

GENESEE RADIO & PARTS CO., INC.  
2550 Delaware Avenue/TR 3-9661  
Buffalo, New York 14216

LAFAYETTE INDUSTRIAL ELECTRONICS  
165-08 Liberty Avenue/AX 1-7000  
Jamaica, New York 11431

MILGRAY/NEW YORK  
160 Varick Street/YU 9-1600  
New York, New York 10013

ROCHESTER RADIO SUPPLY CO., INC.  
140 West Main Street/454-7800  
Rochester, New York 14614

### NORTH CAROLINA

ELECTRONIC WHOLESALERS, INC.  
938 Burke Street/PA 5-8711  
Winston-Salem, North Carolina 27101

### OHIO

NEWARK-HERRLINGER  
ELECTRONICS CORP.  
112 East Liberty Street/GA 1-5282  
Cincinnati, Ohio 45210

SREPCO ELECTRONICS, INC.  
314 Leo Street/BA 4-3871  
Dayton, Ohio 45404

ESCO ELECTRONICS INC.  
3130 Valleywood Drive/298-0191  
Dayton, Ohio 45429

W. M. PATTISON SUPPLY CO.  
777 Rockwell Avenue/621-7320  
Cleveland, Ohio 44101

### OKLAHOMA

TI SUPPLY COMPANY  
1124 East 4th Street/LU 3-8121  
Tulsa, Oklahoma 74110

### PENNSYLVANIA

MILGRAY/DELAWARE VALLEY INC.  
2532 North Broad Street/BA 8-2000  
Philadelphia, Pennsylvania 19107

RADIO PARTS COMPANY, INC.  
6401 Penn Avenue/EM 1-4600  
Pittsburgh, Pennsylvania 15206

### TEXAS

TI SUPPLY COMPANY  
6000 Denton Drive/FL 7-6121  
Dallas, Texas 75235

5240 Elm Street/MO 6-2175  
Houston, Texas 77036

HARRISON EQUIPMENT COMPANY, INC.  
1422 San Jacinto Street/CA 4-9131  
Houston, Texas 77001

MIDLAND SPECIALTY COMPANY  
2235 Wyoming Avenue/KE 3-9555  
El Paso, Texas 79903

### UTAH

STANDARD SUPPLY COMPANY  
225 East Sixth South St./EL 5-2971  
Salt Lake City, Utah 84110

### WASHINGTON

ALMAC-STROUM ELECTRONICS  
621 South Michigan Street/723-7310  
Seattle, Washington 98108

### WASHINGTON, D.C.

ELECTRONIC WHOLESALERS, INC.  
2345 Sherman Avenue, N.W./HU 3-5200  
Washington, D.C. 20001

### CANADA

CANADIAN ELECTRONICS LTD.  
Calgary, Alberta  
Edmonton, Alberta  
Lethbridge, Alberta  
Medicine Hat, Alberta  
Vancouver, B.C.

CAM GARD SUPPLY LTD.  
Saskatoon, Saskatchewan  
Winnipeg, Manitoba

CESCO ELECTRONICS LTD.  
Montreal, Quebec  
Quebec, Quebec  
Ottawa, Ontario  
Toronto, Ontario

TI SUPPLY COMPANY  
Montreal, Quebec

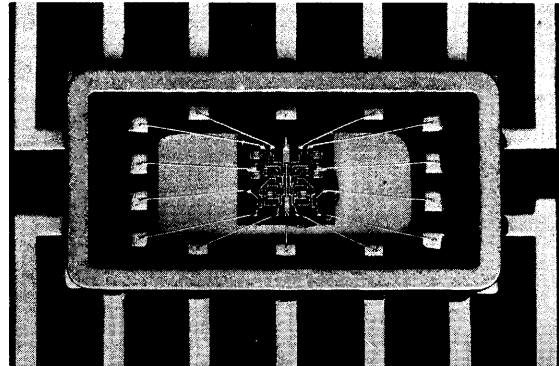




**HIGH-SPEED SATURATED TRANSISTOR-TRANSISTOR LOGIC CIRCUITS  
FOR GENERAL-PURPOSE DIGITAL SYSTEM APPLICATIONS**

**description**

Series 54 integrated circuits have been designed and characterized for high-speed, general-purpose digital applications where high d-c noise margin and relatively low power dissipation are important system considerations. Definitive specifications are provided for operating characteristics over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . This logic series includes the basic gates, flip-flop elements, and complex logic and storage elements needed to perform all functions of general-purpose digital systems.



**TYPE SN5400 PRIOR TO CAPPING**

**features**

**LOW SYSTEM COST**

- maximum number of circuits per package through use of 14-lead package

**OPTIMUM CIRCUIT PERFORMANCE**

- high speed — typical gate propagation delay time of 13 ns
- high d-c noise margin — typically one volt
- low output impedance provides low a-c noise susceptibility
- waveform integrity over full range of loading and temperature conditions
- low power dissipation — 10 mW per gate at 50% duty cycle
- full fan-out of 10

CONTENTS	Page
CIRCUIT DESIGN CHARACTERISTICS AND OPERATION . . . . .	1002
LOGIC DEFINITION AND SYMBOLS . . . . .	1003-1004
DEFINITIVE SPECIFICATIONS . . . . .	1005-1031
D-C TEST CIRCUITS . . . . .	1032-1043
SWITCHING TIME TEST CIRCUITS AND VOLTAGE WAVEFORMS . . . . .	1024-1052
TYPICAL CHARACTERISTICS . . . . .	1053-1055
MECHANICAL DATA . . . . .	1056

<sup>†</sup>Patented by Texas Instruments.

SERIES 54  
 BULLETIN NO. D.L.S. 669179, DECEMBER 1966  
 REPLACES BULLETINS NO. D.L.S. 657921, AUGUST 1965  
 AND D.L.S. 668579, NOVEMBER 1966

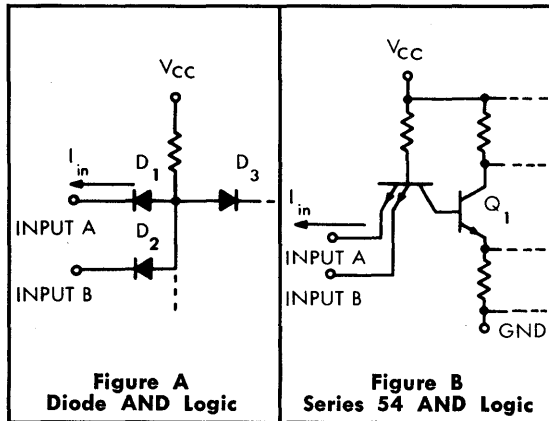


**design characteristics**

Series 54 digital integrated circuits effect an optimization between saturated logic circuitry and monolithic semiconductor technology yielding high performance at lowest cost. In discrete-component circuitry maximum use is made of lower cost components (diodes and resistors) instead of the higher priced transistors. However, in monolithic circuitry it costs no more to build transistors than diodes or resistors. Therefore, in Series 54, transistors are used to buffer the fluctuations in currents that occur as resistor values change. Also, the Series 54 multiple-emitter transistor can easily be built in a monolithic bar to eliminate the need for conventional input diodes.

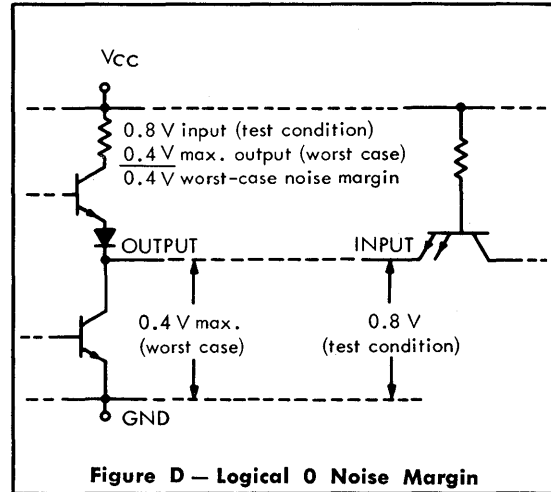
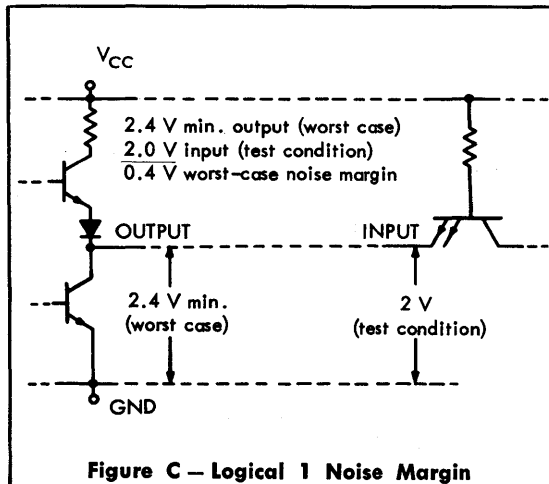
**circuit operation**

The transistor-transistor logic (TTL) used in Series 54 is analogous to diode-transistor logic (DTL) in certain respects. As shown in figure A, a low voltage at inputs A or B will allow current to flow through the diode associated with the low input, and no drive current will pass through diode  $D_3$ . If inputs A and B are raised to a high voltage, drive current will then pass through diode  $D_3$ .



In Series 54 TTL circuitry, the multiple-emitter transistor performs the same function as the diodes in DTL (see figure B). However, the transistor action of the multiple-emitter transistor causes transistor  $Q_1$  to turn-off more rapidly, thus providing an inherent switching-time advantage over the DTL circuit.

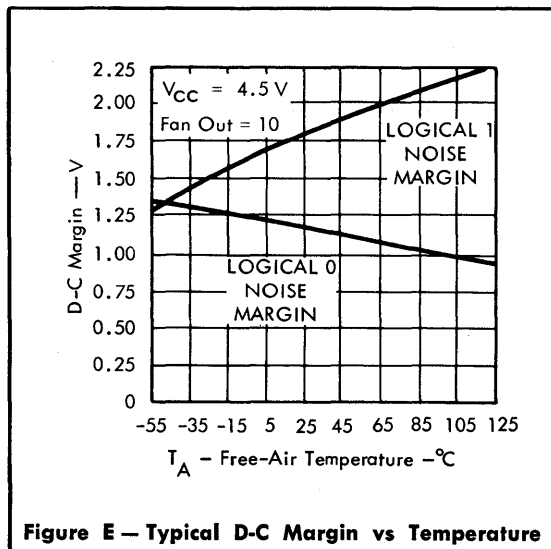
Although one-volt d-c noise margins are typical for Series 54 circuits, an absolute guarantee of 400 millivolts is assured for every unit. This is accomplished by testing each output and input as shown in figures C and D.



Each output is tested to ensure that the logical 1 output voltage will not fall below 2.4 volts. This is done with full fan-out, lowest  $V_{CC}$ , and 0.8 volt on the input — 400 mV more than the logical 0 maximum.

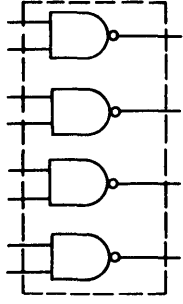
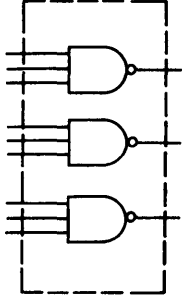
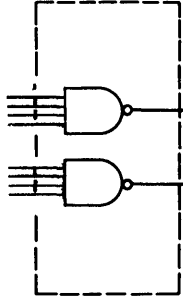
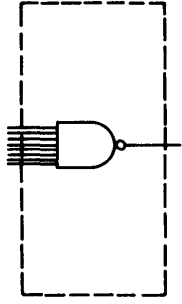
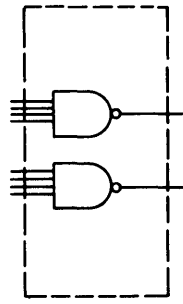
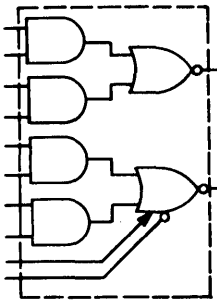
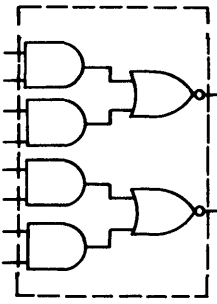
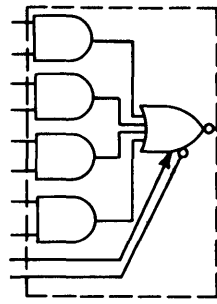
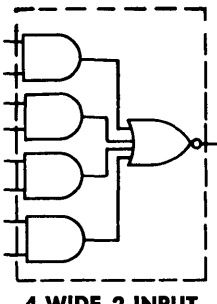
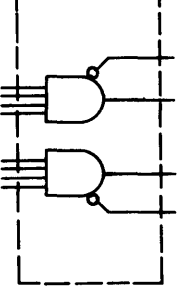
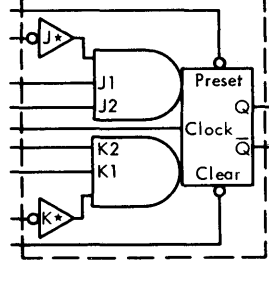
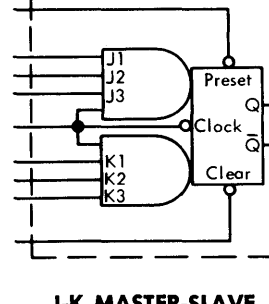
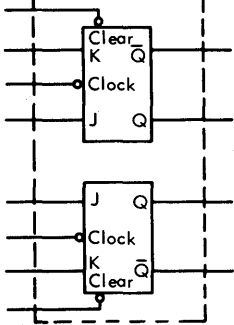
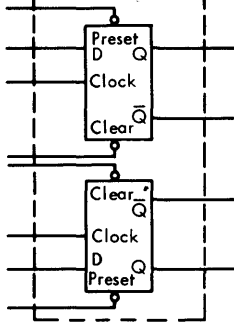
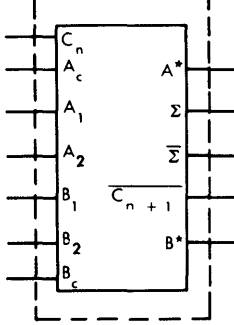
Each output is tested to ensure that the logical 0 output voltage will not exceed 0.4 volt. This is done with full fan-out, lowest  $V_{CC}$ , and 2 volts on the input — 400 mV less than the logical 1 minimum.

In actual system operation, the majority of circuits do not experience worst-case conditions of fan-out, supply voltage, temperature, and input voltage simultaneously. In addition, the threshold voltage of the Series 54 circuits is about 1.5 volts. These characteristics allow a larger voltage change on an input without false triggering. This typical noise margin is shown in figure E.



Another important feature of the design is the output configuration which both supplies current (in the logical 1 state) and sinks current (in the logical 0 state) from a low impedance. Typically, logical 0 output impedance is 12  $\Omega$  and logical 1 output impedance is 70  $\Omega$ . This low output impedance in either state rejects capacitively coupled a-c pulses and ensures small R-C time constants which preserve wave-shape integrity.

standard line summary

<p><b>SN5400</b> See page 1005</p>  <p><b>QUADRUPLE 2-INPUT POSITIVE NAND GATE</b></p>	<p><b>SN5410</b> See page 1006</p>  <p><b>TRIPLE 3-INPUT POSITIVE NAND GATE</b></p>	<p><b>SN5420</b> See page 1007</p>  <p><b>DUAL 4-INPUT POSITIVE NAND GATE</b></p>	<p><b>SN5430</b> See page 1008</p>  <p><b>8-INPUT POSITIVE NAND GATE</b></p>
<p><b>SN5440</b> See page 1009</p>  <p><b>DUAL 4-INPUT POSITIVE NAND BUFFER</b></p>	<p><b>SN5450</b> See page 1010</p>  <p><b>EXPANDABLE DUAL 4-WIDE 2-INPUT AND-OR-INVERT GATE</b></p>	<p><b>SN5451</b> See page 1010</p>  <p><b>DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE</b></p>	<p><b>SN5453</b> See page 1012</p>  <p><b>EXPANDABLE 4-WIDE 2-INPUT AND-OR-INVERT GATE</b></p>
<p><b>SN5454</b> See page 1012</p>  <p><b>4-WIDE 2-INPUT AND-OR-INVERT GATE</b></p>	<p><b>SN5460</b> See page 1014</p>  <p><b>DUAL 4-INPUT EXPANDER</b></p>	<p><b>SN5470</b> See page 1015</p>  <p><b>J-K FLIP-FLOP</b></p>	<p><b>SN5472</b> See page 1018</p>  <p><b>J-K MASTER-SLAVE FLIP-FLOP</b></p>
<p><b>SN5473</b> See page 1021</p>  <p><b>DUAL J-K MASTER-SLAVE FLIP-FLOP</b></p>	<p><b>SN5474</b> See page 1024</p>  <p><b>DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP</b></p>	<p><b>SN5480</b> See page 1027</p>  <p><b>GATED FULL ADDER</b></p>	



# SERIES 54

## **SOLID CIRCUIT**<sup>®</sup> SEMICONDUCTOR NETWORKS

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage $V_{CC}$ (See Note 1) . . . . .	7 V
Input Voltage $V_{in}$ (See Notes 1 and 2) . . . . .	5.5 V
Operating Free-Air Temperature Range . . . . .	-55°C to 125°C
Storage Temperature Range . . . . .	-65°C to 150°C

- NOTES: 1. Voltage values are with respect to network ground terminal.  
2. Input signals must be zero or positive with respect to network ground terminal.

### logic definition

Series 54 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

- LOW VOLTAGE = LOGICAL 0
- HIGH VOLTAGE = LOGICAL 1

### input-current requirements

Input-current requirements reflect worst-case conditions for  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$  and  $V_{CC} = 4.5\text{ V}$  to  $5.5\text{ V}$ . Each input of the multiple-emitter input transistor requires that no more than  $-1.6\text{ mA}$  flow out of the input at a logical 0 voltage level; therefore, one load ( $N = 1$ ) is  $-1.6\text{ mA}$  maximum. Each input requires current into the input at a logical 1 voltage level. This current is  $40\ \mu\text{A}$  maximum for each emitter input. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

### fan-out capability

Fan-out reflects the ability of an output to sink current from a number of loads ( $N$ ) at a logical 0 voltage level and to supply current at a logical 1 voltage level. Each standard output is capable of sinking current or supplying current to 10 loads ( $N = 10$ ). The buffer gate is capable of sinking current or supplying current to 30 loads ( $N = 30$ ). The carry output ( $C_{n+1}$ ) of the full adder is capable of driving 5 loads ( $N = 5$ ) and the  $A^*$  and  $B^*$  nodes may be used to drive 3 loads ( $N = 3$ ). Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuits indicate the actual direction of current flow.

### unused inputs

For optimum switching times, unused gate inputs should be tied to a positive voltage source of  $2.4\text{ V}$  to  $5.5\text{ V}$ . This eliminates the distributed capacitance associated with the floating input-transistor emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Supply voltage  $V_{CC}$ , if regulated to  $5.5\text{ V}$  maximum, may be used.

If the supply voltage  $V_{CC}$  cannot be limited to  $5.5\text{ V}$  the following alternatives are recommended:

- a. Connect unused gate inputs to an independent supply voltage source of  $2.4\text{ V}$  to  $5.5\text{ V}$ .
- b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded.

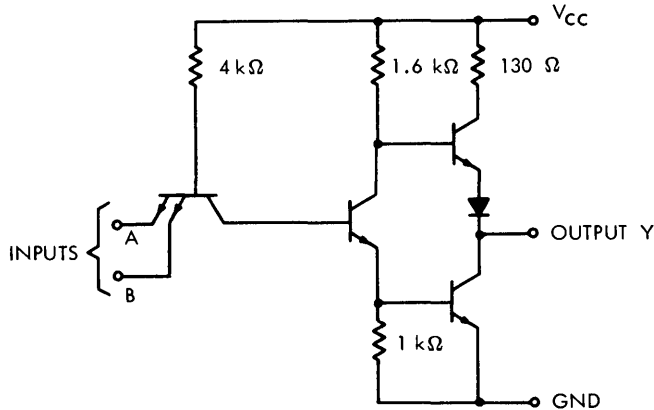
In all cases, unused  $J^*$  and  $K^*$  inputs of the SN5470 must be connected to ground.

Instructions for terminating unused inputs of the SN5480 are provided in the applications shown for that device.

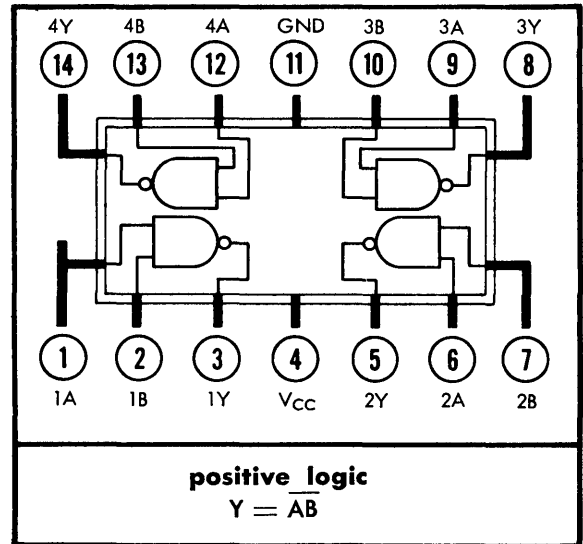
# TYPE SN5400

## QUADRUPLE 2-INPUT POSITIVE NAND GATE

### schematic (each gate)



Component values shown are nominal.



### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	4.5 V to 5.5 V
Fan-Out From Each Output, N . . . . .	1 to 10

### electrical characteristics, $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	$V_{CC} = 4.5 \text{ V}$ , $V_{out(0)} \leq 0.4 \text{ V}$	2			V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	$V_{CC} = 4.5 \text{ V}$ , $V_{out(1)} \geq 2.4 \text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	2	$V_{CC} = 4.5 \text{ V}$ , $I_{load} = -400 \mu\text{A}$ , $V_{in} = 0.8 \text{ V}$	2.4	3.3 $\ddagger$		V
$V_{out(0)}$ Logical 0 output voltage	1	$V_{CC} = 4.5 \text{ V}$ , $I_{sink} = 16 \text{ mA}$ , $V_{in} = 2 \text{ V}$		0.22 $\ddagger$	0.4	V
$I_{in(0)}$ Logical 0 level input current (each input)	3	$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 0.4 \text{ V}$			-1.6	mA
$I_{in(1)}$ Logical 1 level input current (each input)	4	$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 2.4 \text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 5.5 \text{ V}$			1	mA
$I_{OS}$ Short-circuit output current $\dagger$	5	$V_{CC} = 5.5 \text{ V}$	-20		-55	mA
$I_{CC(0)}$ Logical 0 level supply current (each gate)	6	$V_{CC} = 5 \text{ V}$ , $V_{in} = 5 \text{ V}$		3		mA
$I_{CC(1)}$ Logical 1 level supply current (each gate)	6	$V_{CC} = 5 \text{ V}$ , $V_{in} = 0$		1		mA

### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$ , N = 10

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$ Propagation delay time to logical 0 level	50	$C_1 = 15 \text{ pF}$		8	15	ns
$t_{pd1}$ Propagation delay time to logical 1 level	50	$C_1 = 15 \text{ pF}$		18	29	ns

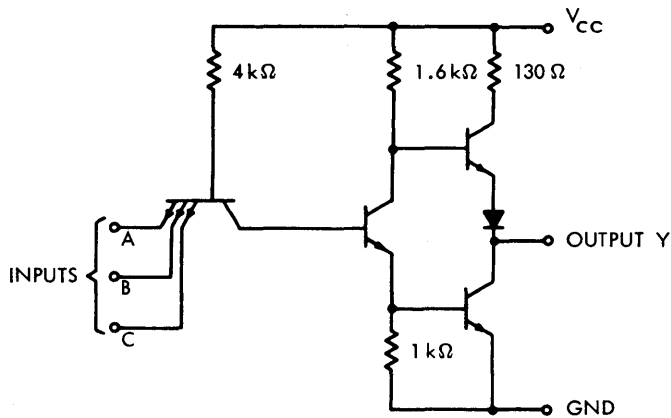
$\dagger$ Not more than one output should be shorted at a time.

$\ddagger$ These typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

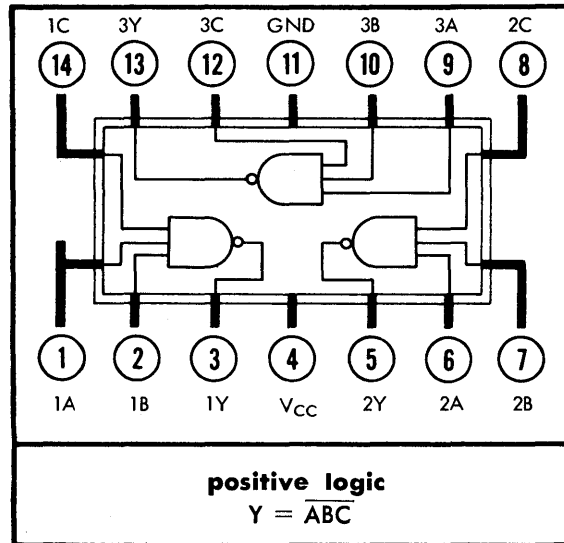
# TYPE SN5410

## TRIPLE 3-INPUT POSITIVE NAND GATE

schematic (each gate)



Component values shown are nominal.



positive logic  
 $Y = \overline{ABC}$

### recommended operating conditions

Supply Voltage $V_{CC}$	4.5 V to 5.5 V
Fan-Out From Output, N	1 to 10

### electrical characteristics, $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	$V_{CC} = 4.5 \text{ V}$ , $V_{out(0)} \leq 0.4 \text{ V}$	2			V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	$V_{CC} = 4.5 \text{ V}$ , $V_{out(1)} \geq 2.4 \text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	2	$V_{CC} = 4.5 \text{ V}$ , $V_{in} = 0.8 \text{ V}$ , $I_{load} = -400 \mu\text{A}$	2.4	3.3‡		V
$V_{out(0)}$ Logical 0 output voltage	1	$V_{CC} = 4.5 \text{ V}$ , $V_{in} = 2 \text{ V}$ , $I_{sink} = 16 \text{ mA}$		0.22‡	0.4	V
$I_{in(0)}$ Logical 0 level input current (each input)	3	$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 0.4 \text{ V}$			-1.6	mA
$I_{in(1)}$ Logical 1 level input current (each input)	4	$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 2.4 \text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 5.5 \text{ V}$			1	mA
$I_{OS}$ Short-circuit output current†	5	$V_{CC} = 5.5 \text{ V}$	-20		-55	mA
$I_{CC(0)}$ Logical 0 level supply current (each gate)	6	$V_{CC} = 5 \text{ V}$ , $V_{in} = 5 \text{ V}$		3		mA
$I_{CC(1)}$ Logical 1 level supply current (each gate)	6	$V_{CC} = 5 \text{ V}$ , $V_{in} = 0$		1		mA

### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$ , $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$ Propagation delay time to logical 0 level	50	$C_1 = 15 \text{ pF}$		8	15	ns
$t_{pd1}$ Propagation delay time to logical 1 level	50	$C_1 = 15 \text{ pF}$		18	29	ns

†Not more than one output should be shorted at a time.

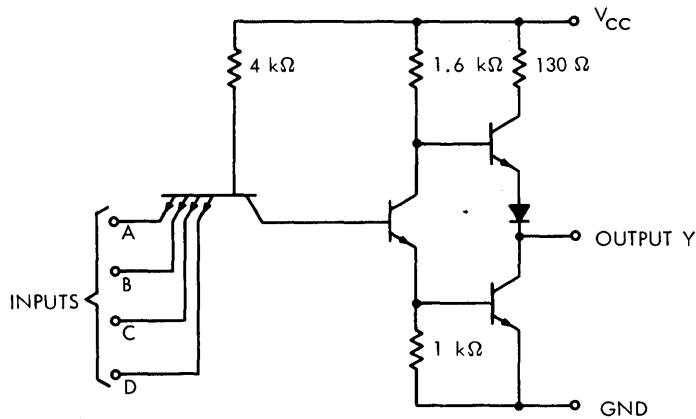
‡These typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .



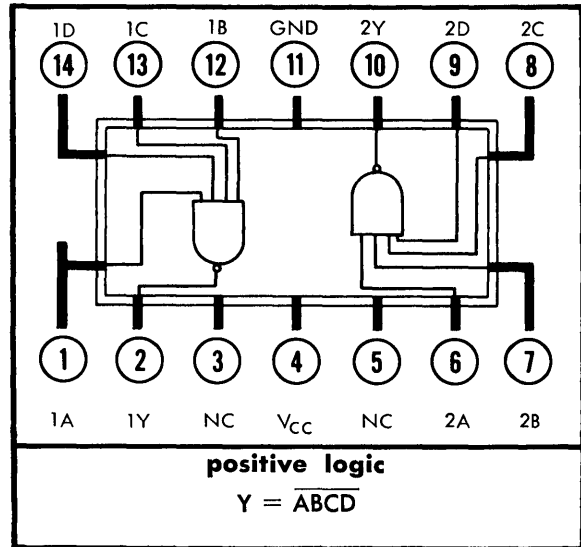
# TYPE SN5420

## DUAL 4-INPUT POSITIVE NAND GATE

### schematic (each gate)



Component values shown are nominal.



### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	4.5 V to 5.5 V
Fan-Out From Each Output, N . . . . .	1 to 10

### electrical characteristics, $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	$V_{CC} = 4.5\text{ V}$ , $V_{out(0)} \leq 0.4\text{ V}$	2			V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	$V_{CC} = 4.5\text{ V}$ , $V_{out(1)} \geq 2.4\text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	2	$V_{CC} = 4.5\text{ V}$ , $I_{load} = -400\ \mu\text{A}$ , $V_{in} = 0.8\text{ V}$	2.4	3.3‡		V
$V_{out(0)}$ Logical 0 output voltage	1	$V_{CC} = 4.5\text{ V}$ , $I_{sink} = 16\text{ mA}$ , $V_{in} = 2\text{ V}$		0.22‡	0.4	V
$I_{in(0)}$ Logical 0 level input current (each input)	3	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 0.4\text{ V}$			-1.6	mA
$I_{in(1)}$ Logical 1 level input current (each input)	4	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 2.4\text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}$ , $V_{in} = 5.5\text{ V}$			1	mA
$I_{OS}$ Short-circuit output current†	5	$V_{CC} = 5.5\text{ V}$	-20		-55	mA
$I_{CC(0)}$ Logical 0 level supply current (each gate)	6	$V_{CC} = 5\text{ V}$ , $V_{in} = 5\text{ V}$		3		mA
$I_{CC(1)}$ Logical 1 level supply current (each gate)	6	$V_{CC} = 5\text{ V}$ , $V_{in} = 0$		1		mA

### switching characteristics, $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ , $N = 10$

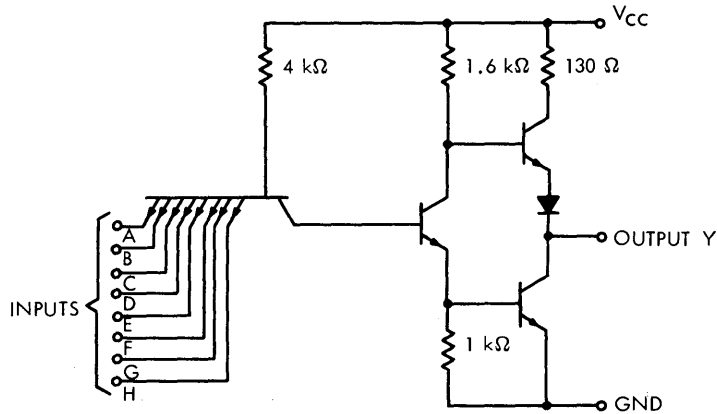
PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$ Propagation delay time to logical 0 level	50	$C_1 = 15\text{ pF}$		8	15	ns
$t_{pd1}$ Propagation delay time to logical 1 level	50	$C_1 = 15\text{ pF}$		18	29	ns

†Not more than one output should be shorted at a time.  
‡These typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

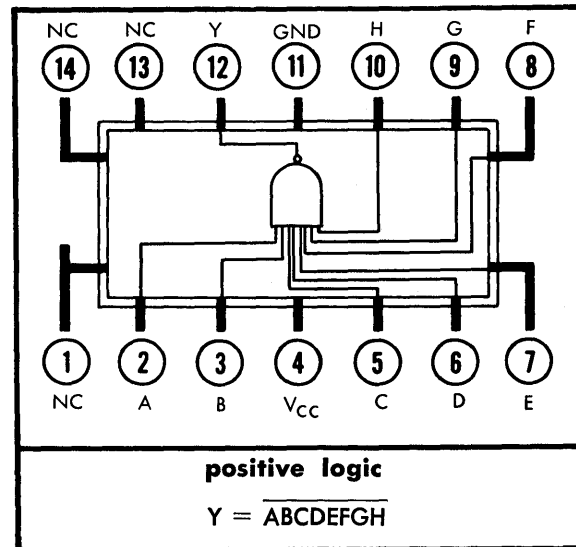
# TYPE SN5430

## 8-INPUT POSITIVE NAND GATE

### schematic



Component values shown are nominal.



### recommended operating conditions

Supply Voltage $V_{CC}$	4.5 V to 5.5 V
Fan-Out From Output, N	1 to 10

### electrical characteristics, $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	$V_{CC} = 4.5 \text{ V}$ , $V_{out(0)} \leq 0.4 \text{ V}$	2			V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	$V_{CC} = 4.5 \text{ V}$ , $V_{out(1)} \geq 2.4 \text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	2	$V_{CC} = 4.5 \text{ V}$ , $V_{in} = 0.8 \text{ V}$ , $I_{load} = -400 \mu\text{A}$	2.4	3.3‡		V
$V_{out(0)}$ Logical 0 output voltage	1	$V_{CC} = 4.5 \text{ V}$ , $I_{sink} = 16 \text{ mA}$ , $V_{in} = 2 \text{ V}$		0.22‡	0.4	V
$I_{in(0)}$ Logical 0 level input current (each input)	3	$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 0.4 \text{ V}$			-1.6	mA
$I_{in(1)}$ Logical 1 level input current (each input)	4	$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 2.4 \text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 5.5 \text{ V}$			1	mA
$I_{OS}$ Short-circuit output current	5	$V_{CC} = 5.5 \text{ V}$	-20		-55	mA
$I_{CC(0)}$ Logical 0 level supply current	6	$V_{CC} = 5 \text{ V}$ , $V_{in} = 5 \text{ V}$		3		mA
$I_{CC(1)}$ Logical 1 level supply current	6	$V_{CC} = 5 \text{ V}$ , $V_{in} = 0$		1		mA

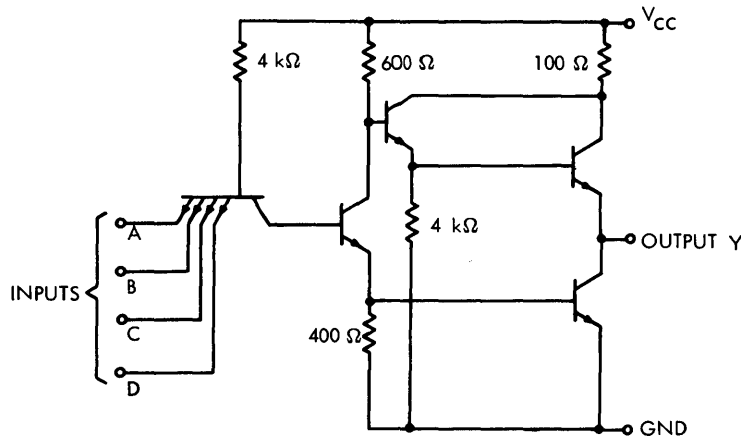
### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$ , $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$ Propagation delay time to logical 0 level	50	$C_1 = 15 \text{ pF}$		8	15	ns
$t_{pd1}$ Propagation delay time to logical 1 level	50	$C_1 = 15 \text{ pF}$		18	29	ns

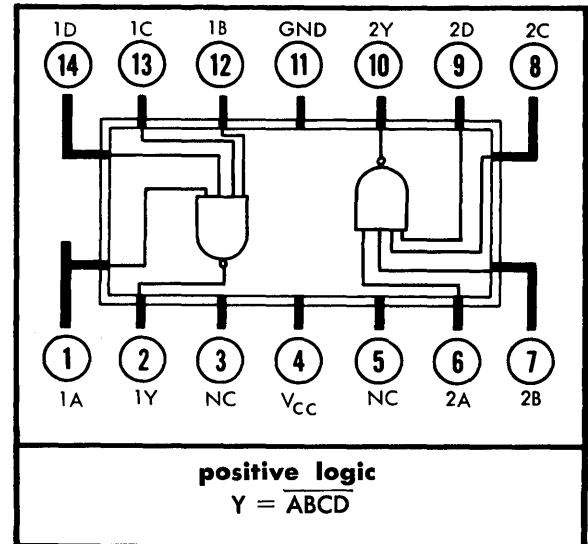
‡These typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

# TYPE SN5440 DUAL 4-INPUT POSITIVE NAND BUFFER

## schematic (each gate)



Component values shown are nominal.



## recommended operating conditions

Supply Voltage $V_{CC}$	4.5 V to 5.5 V
Fan-Out From Output, N	1 to 30

## electrical characteristics, $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	$V_{CC} = 4.5 \text{ V}$ , $V_{out(0)} \leq 0.4 \text{ V}$	2			V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	$V_{CC} = 4.5 \text{ V}$ , $V_{out(1)} \geq 2.4 \text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	2	$V_{CC} = 4.5 \text{ V}$ , $I_{load} = -1.2 \text{ mA}$ , $V_{in} = 0.8 \text{ V}$	2.4	3.3 $\ddagger$		V
$V_{out(0)}$ Logical 0 output voltage	1	$V_{CC} = 4.5 \text{ V}$ , $I_{sink} = 48 \text{ mA}$ , $V_{in} = 2 \text{ V}$	0.28 $\ddagger$	0.4		V
$I_{in(0)}$ Logical 0 level input current (each input)	3	$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 0.4 \text{ V}$			-1.6	mA
$I_{in(1)}$ Logical 1 level input current (each input)	4	$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 2.4 \text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 5.5 \text{ V}$			1	mA
$I_{OS}$ Short-circuit output current $\dagger$	5	$V_{CC} = 5.5 \text{ V}$	-20		-70	mA
$I_{CC(0)}$ Logical 0 level supply current (each gate)	6	$V_{CC} = 5 \text{ V}$ , $V_{in} = 5 \text{ V}$		8.6		mA
$I_{CC(1)}$ Logical 1 level supply current (each gate)	6	$V_{CC} = 5 \text{ V}$ , $V_{in} = 0$		2		mA

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$ , $N = 30$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$ Propagation delay time to logical 0 level	50	$C_1 = 15 \text{ pF}$		8	15	ns
$t_{pd1}$ Propagation delay time to logical 1 level	50	$C_1 = 15 \text{ pF}$		18	29	ns

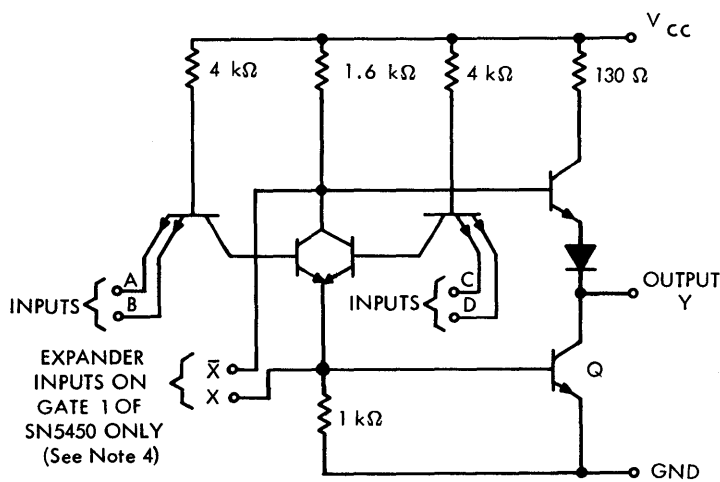
$\dagger$ Not more than one output should be shorted at a time.

$\ddagger$ These typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

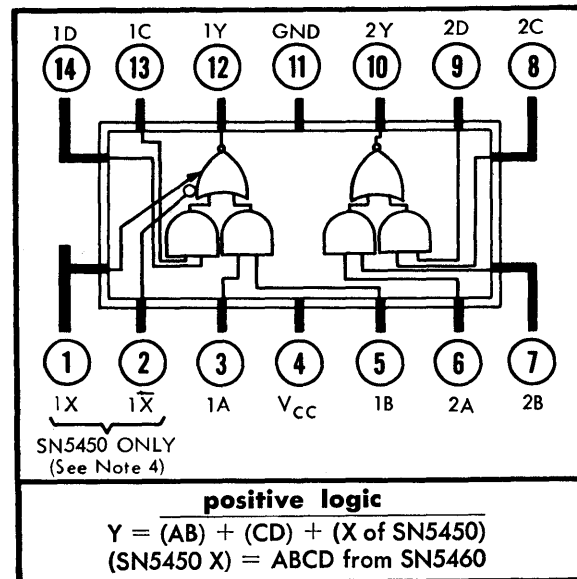
# TYPES SN5450, SN5451

## DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

schematic (each gate)



- NOTES:
- Component values shown are nominal.
  - Both SN5450 expander inputs are used simultaneously for expanding with the SN5460.
  - If expander is not used leave pins ① and ② open.
  - Make no external connection to pins ① and ② of the SN5451.
  - A total of four expander gates may be connected to the SN5450 expander inputs.



### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	4.5 V to 5.5 V
Fan-Out From Each Output, N . . . . .	1 to 10

### electrical characteristics, $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$ , pins ① and ② open

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	7	$V_{CC} = 4.5 \text{ V}, V_{out(0)} \leq 0.4 \text{ V}$	2			V
$V_{in(0)}$ Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	8	$V_{CC} = 4.5 \text{ V}, V_{out(1)} \geq 2.4 \text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	8	$V_{CC} = 4.5 \text{ V}, V_{in} = 0.8 \text{ V}, I_{load} = -400 \mu\text{A}$	2.4	3.3‡		V
$V_{out(0)}$ Logical 0 output voltage	7	$V_{CC} = 4.5 \text{ V}, V_{in} = 2 \text{ V}, I_{sink} = 16 \text{ mA}$		0.22‡	0.4	V
$I_{in(0)}$ Logical 0 level input current (each input)	9	$V_{CC} = 5.5 \text{ V}, V_{in} = 0$			-1.6	mA
$I_{in(1)}$ Logical 1 level input current (each input)	10	$V_{CC} = 5.5 \text{ V}, V_{in} = 2.4 \text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.5 \text{ V}, V_{in} = 5.5 \text{ V}$			1	mA
$I_{OS}$ Short-circuit output current†	11	$V_{CC} = 5.5 \text{ V}$	-20		-55	mA
$I_{CC(0)}$ Logical 0 level supply current (each gate)	12	$V_{CC} = 5 \text{ V}, V_{in} = 5 \text{ V}$		3.7		mA
$I_{CC(1)}$ Logical 1 level supply current (each gate)	13	$V_{CC} = 5 \text{ V}, V_{in} = 0$		2		mA

†Not more than one output should be shorted at a time.  
 ‡These typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

# TYPES SN5450, SN5451

## DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

electrical characteristics (SN5450 only) using expander inputs,  $T_A = -55^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_X$ Expander current	14	$V_{CC} = 4.5\text{ V}$ , $V_1 = 0.4\text{ V}$ , $I_{\text{sink}} = 16\text{ mA}$			2.9	mA
$V_{BE(Q)}$ Base-emitter voltage of output transistor (Q)	15	$V_{CC} = 4.5\text{ V}$ , $I_{\text{sink}} = 16\text{ mA}$ , $I_1 = 0.41\text{ mA}$ , $R_1 = 0$			1	V
$V_{\text{out}(1)}$ Logical 1 output voltage	16	$V_{CC} = 4.5\text{ V}$ , $I_{\text{load}} = -400\ \mu\text{A}$ , $I_1 = 0.15\text{ mA}$ , $I_2 = -0.15\text{ mA}$	2.4	$3.3\ddagger$		V
$V_{\text{out}(0)}$ Logical 0 output voltage	15	$V_{CC} = 4.5\text{ V}$ , $I_{\text{sink}} = 16\text{ mA}$ , $I_1 = 0.3\text{ mA}$ , $R_1 = 138\ \Omega$		$0.22\ddagger$	0.4	V

$\ddagger$ These typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

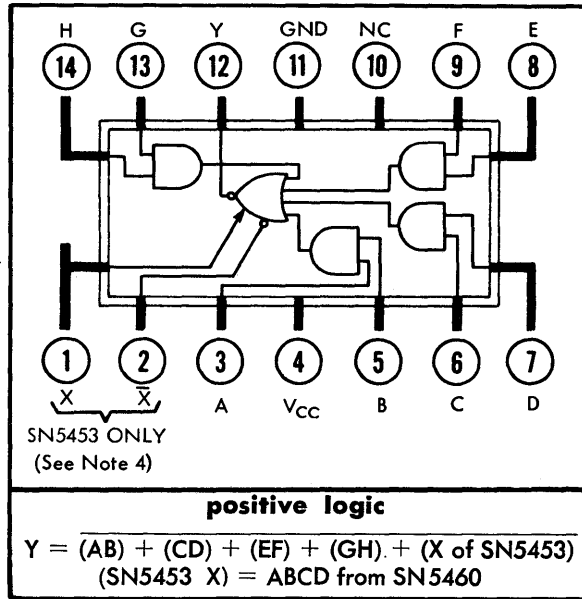
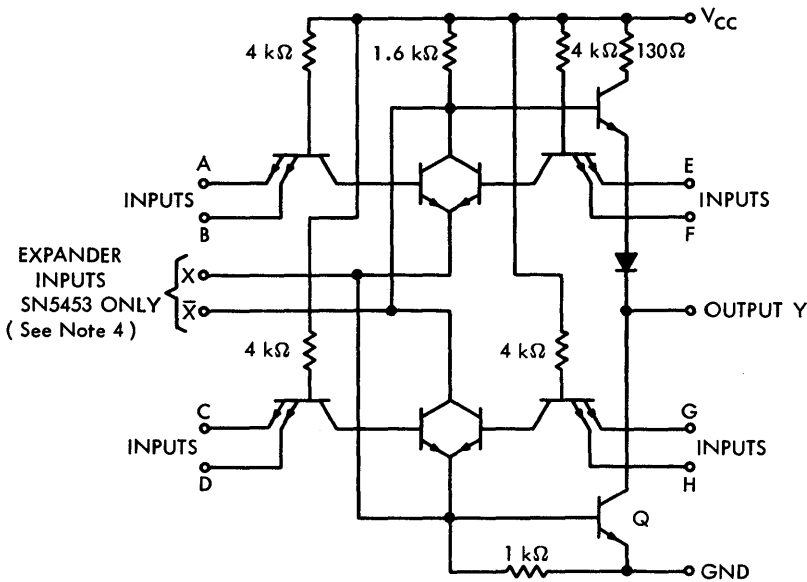
switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , pins (1) and (2) open,  $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\text{pd}0}$ Propagation delay time to logical 0 level	50	$C_1 = 15\text{ pF}$		8	15	ns
$t_{\text{pd}1}$ Propagation delay time to logical 1 level	50	$C_1 = 15\text{ pF}$		18	29	ns

# TYPES SN5453, SN5454

## 4-WIDE 2-INPUT AND-OR-INVERT GATES

### schematic



- NOTES: 1. Component values shown are nominal.
2. Both SN5453 expander inputs are used simultaneously for expanding with the SN5460.
3. If SN5453 expander is not used leave pins ① and ② open.
4. Make no external connection to pins ① and ② of the SN5454.
5. A total of four expander gates may be connected to the SN5453 expander inputs.

### recommended operating conditions

Supply Voltage $V_{CC}$	4.5 V to 5.5 V
Fan-Out From Each Output, N	1 to 10

### electrical characteristics, $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$ , pins ① and ② open

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	7	$V_{CC} = 4.5 \text{ V}, V_{out(0)} \leq 0.4 \text{ V}$	2			V
$V_{in(0)}$ Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	8	$V_{CC} = 4.5 \text{ V}, V_{out(1)} \geq 2.4 \text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	8	$V_{CC} = 4.5 \text{ V}, V_{in} = 0.8 \text{ V}, I_{load} = -400 \mu\text{A}$	2.4	3.3‡		V
$V_{out(0)}$ Logical 0 output voltage	7	$V_{CC} = 4.5 \text{ V}, V_{in} = 2 \text{ V}, I_{sink} = 16 \text{ mA}$		0.22‡	0.4	V
$I_{in(0)}$ Logical 0 level input current (each input)	9	$V_{CC} = 5.5 \text{ V}, V_{in} = 0$			-1.6	mA
$I_{in(1)}$ Logical 1 level input current (each input)	10	$V_{CC} = 5.5 \text{ V}, V_{in} = 2.4 \text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.5 \text{ V}, V_{in} = 5.5 \text{ V}$			1	mA
$I_{OS}$ Short-circuit output current†	11	$V_{CC} = 5.5 \text{ V}$	-20		-55	mA
$I_{CC(0)}$ Logical 0 level supply current	12	$V_{CC} = 5 \text{ V}, V_{in} = 5 \text{ V}$		5.1		mA
$I_{CC(1)}$ Logical 1 level supply current	13	$V_{CC} = 5 \text{ V}, V_{in} = 0$		4		mA

†Not more than one output should be shorted at a time.

‡These typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .



# TYPES SN5453, SN5454

## 4-WIDE 2-INPUT AND-OR-INVERT GATES

electrical characteristics (SN5453 only) using expander inputs,  $T_A = -55^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_X$ Expander current	14	$V_{CC} = 4.5\text{ V}$ , $V_1 = 0.4\text{ V}$ , $I_{\text{sink}} = 16\text{ mA}$			2.9	mA
$V_{BE(Q)}$ Base-emitter voltage of output transistor (Q)	15	$V_{CC} = 4.5\text{ V}$ , $I_{\text{sink}} = 16\text{ mA}$ , $I_1 = 0.41\text{ mA}$ , $R_1 = 0$			1	V
$V_{\text{out}(1)}$ Logical 1 output voltage	16	$V_{CC} = 4.5\text{ V}$ , $I_{\text{load}} = -400\text{ }\mu\text{A}$ , $I_1 = 0.15\text{ mA}$ , $I_2 = -0.15\text{ mA}$	2.4	3.3‡		V
$V_{\text{out}(0)}$ Logical 0 output voltage	15	$V_{CC} = 4.5\text{ V}$ , $I_{\text{sink}} = 16\text{ mA}$ , $I_1 = 0.3\text{ mA}$ , $R_1 = 138\text{ }\Omega$		0.22‡	0.4	V

‡These typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

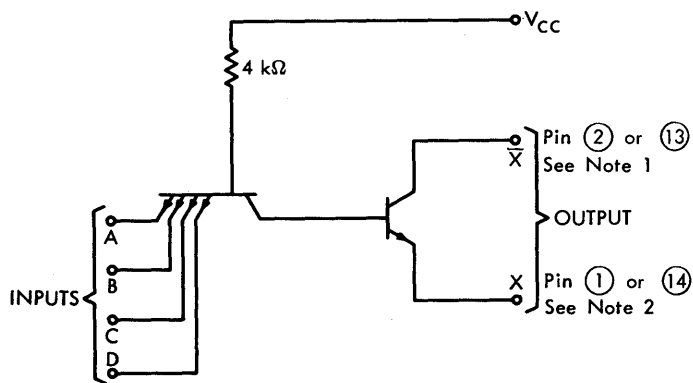
switching characteristics(SN5453 andSN5454),  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , pins ① and ② open,  $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$ Propagation delay time to logical 0 level	50	$C_1 = 15\text{ pF}$		8	15	ns
$t_{pd1}$ Propagation delay time to logical 1 level	50	$C_1 = 15\text{ pF}$		18	29	ns

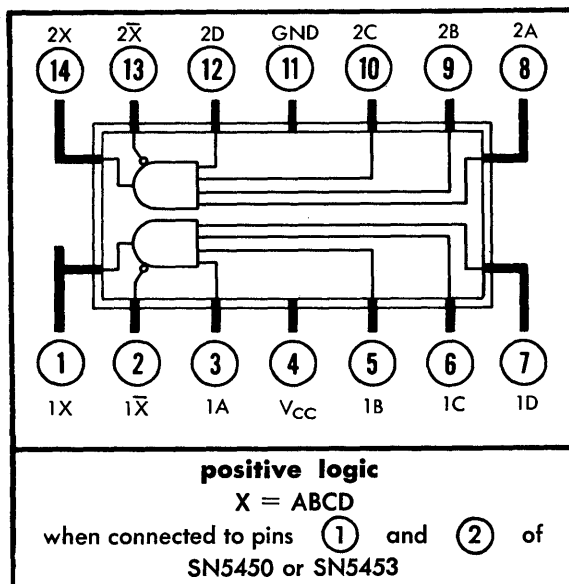
# TYPE SN5460

## DUAL 4-INPUT EXPANDER

### schematic



- NOTES: 1. Connect pin ② or ⑬ to pin ② of SN5450 or SN5453.  
 2. Connect pin ① or ⑭ to pin ① of SN5450 or SN5453.  
 3. Component values shown are nominal.



### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	4.5 V to 5.5 V
Maximum number of expanders that may be fanned-in to one SN5450 or one SN5453 . . . . .	4

### electrical characteristics (unless otherwise noted $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure output on level	17	$V_{CC} = 4.5 \text{ V}$ , $R = 1.1 \text{ k}\Omega$ , $V_1 = 1 \text{ V}$ , $T_A = -55^\circ\text{C}$ ,	2			V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure output off level current	18	$V_{CC} = 4.5 \text{ V}$ , $R = 1.2 \text{ k}\Omega$ , $T_A = -55^\circ\text{C}$ , $I_{off} = 0.15 \text{ mA}$ ,			0.8	V
$V_{on}$ Output voltage on level	17	$V_{CC} = 4.5 \text{ V}$ , $V_1 = 1 \text{ V}$ , $T_A = -55^\circ\text{C}$ , $V_{in} = 2 \text{ V}$ , $R = 1.1 \text{ k}\Omega$ ,			0.4	V
$I_{off}$ Output off level current	18	$V_{CC} = 4.5 \text{ V}$ , $V_1 = 4.5 \text{ V}$ , $T_A = -55^\circ\text{C}$ , $V_{in} = 0.8 \text{ V}$ , $R = 1.2 \text{ k}\Omega$ ,			150	$\mu\text{A}$
$I_{on}$ Output on level current	19	$V_{CC} = 4.5 \text{ V}$ , $V_1 = 1 \text{ V}$ , $T_A = -55^\circ\text{C}$ , $V_{in} = 2 \text{ V}$ , $T_A = -55^\circ\text{C}$	-0.3			mA
$I_{in(0)}$ Logical 0 level input current (each input)	18	$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 0.4 \text{ V}$ ,		-1.6		mA
$I_{in(1)}$ Logical 1 level input current (each input)	20	$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 2.4 \text{ V}$		40		$\mu\text{A}$
		$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 5.5 \text{ V}$		1		mA
$I_{CC(on)}$ On level supply current (each gate)	21	$V_{CC} = 5 \text{ V}$ , $V_1 = 0.85 \text{ V}$ , $V_{in} = 5 \text{ V}$ ,		0.6		mA
$I_{CC(off)}$ Off level supply current (each gate)	21	$V_{CC} = 5 \text{ V}$ , $V_1 = 0.85 \text{ V}$ , $V_{in} = 0$ ,		1		mA

### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$ , $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$ Propagation delay time to logical 0 level (through SN5450 or SN5453)	51	$C_1 = 15 \text{ pF}$		10	20	ns
$t_{pd1}$ Propagation delay time to logical 1 level (through SN5450 or SN5453)	51	$C_1 = 15 \text{ pF}$		20	34	ns

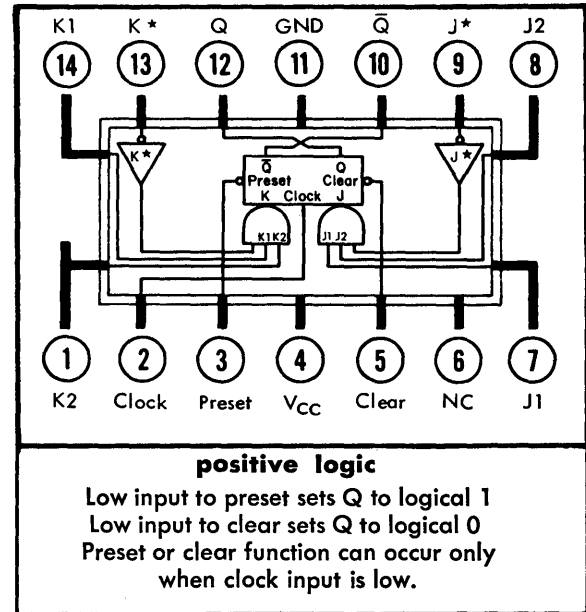
# TYPE SN5470

## J-K FLIP-FLOP

### logic

TRUTH TABLE		
J	$t_n$ K	$t_{n+1}$ Q
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\overline{Q}_n$

- NOTES: 1.  $J = J1 \cdot J2 \cdot \overline{J\star}$ .  
 2.  $K = K1 \cdot K2 \cdot \overline{K\star}$ .  
 3.  $t_n$  = Bit time before clock pulse.  
 4.  $t_{n+1}$  = Bit time after clock pulse.  
 5. If inputs  $J\star$  or  $K\star$  are not used they must be grounded.



### description

The SN5470 is a monolithic, edge-triggered J-K flip-flop featuring gated inputs, direct clear and preset inputs, and complementary Q and  $\overline{Q}$  outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse; and after the clock input threshold voltage has been passed, the gated inputs are locked out.

The SN5470 flip-flop is ideally suited for medium- to high-speed applications, and can be used for a significant saving in system power dissipation and package count where input gating is required.

### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	4.5 V to 5.5 V
Fan-Out From Each Output, N . . . . .	1 to 10
Clock Pulse Transition Time to Logical 1 Level, $t_{1(\text{clock})}$ (See Figure 53) . . . . .	5 to 150 ns
Width of Clock Pulse, $t_{p(\text{clock})}$ (See Figure 53) . . . . .	$\geq 20$ ns
Width of Preset Pulse, $t_{p(\text{preset})}$ (See Figure 52) . . . . .	$\geq 25$ ns
Width of Clear Pulse, $t_{p(\text{clear})}$ (See Figure 52) . . . . .	$\geq 25$ ns

# TYPE SN5470

## J-K FLIP-FLOP

electrical characteristics,  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal	22	$V_{CC} = 4.5\text{ V}$	2			V
$V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal	23	$V_{CC} = 4.5\text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	22	$V_{CC} = 4.5\text{ V}, I_{load} = -400\ \mu\text{A}$	2.4	3.5 $\ddagger$		V
$V_{out(0)}$ Logical 0 output voltage	23	$V_{CC} = 4.5\text{ V}, I_{sink} = 16\text{ mA}$	0.22 $\ddagger$		0.4	V
$I_{in(0)}$ Logical 0 level input current at J1, J2, J $\star$ , K1, K2, K $\star$ , or clock	24	$V_{CC} = 5.5\text{ V}, V_{in} = 0.4\text{ V}$			-1.6	mA
$I_{in(0)}$ Logical 0 level input current at preset or clear	24	$V_{CC} = 5.5\text{ V}, V_{in} = 0.4\text{ V}$			-3.2	mA
$I_{in(1)}$ Logical 1 level input current at J1, J2, J $\star$ , K1, K2, K $\star$ , or clock	25	$V_{CC} = 5.5\text{ V}, V_{in} = 2.4\text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}, V_{in} = 5.5\text{ V}$			1	mA
$I_{in(1)}$ Logical 1 level input current at preset or clear	25	$V_{CC} = 5.5\text{ V}, V_{in} = 2.4\text{ V}$			80	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}, V_{in} = 5.5\text{ V}$			1	mA
$I_{OS}$ Short-circuit output current $\dagger$	26	$V_{CC} = 5.5\text{ V}, V_{in} = 0$	-20		-57	mA
$I_{CC}$ Supply current	25	$V_{CC} = 5\text{ V}, V_{in} = 5\text{ V}$		13		mA

$\dagger$ Not more than one output should be shorted at a time.

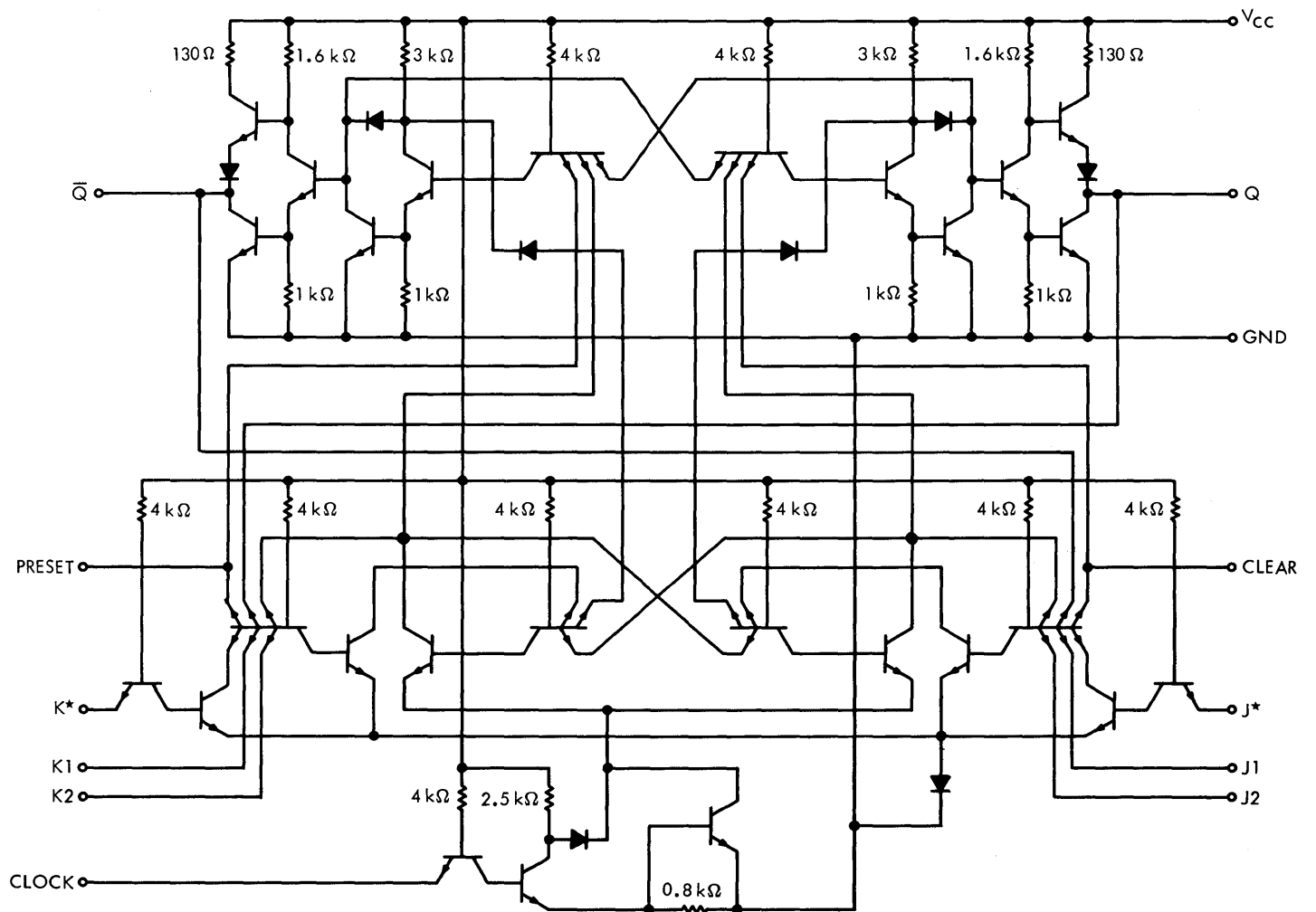
$\ddagger$ These typical values are at  $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$ .

switching characteristics,  $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}, N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{clock}$ Maximum clock frequency	53	$C_1 = 15\text{ pF}$	20	35		MHz
$t_{setup}$ Minimum input setup time	53	$C_1 = 15\text{ pF}$		10	20	ns
$t_{hold}$ Minimum input hold time	53	$C_1 = 15\text{ pF}$		0	5	ns
$t_{pd1}$ Propagation delay time to logical 1 level from clear or preset to output	52	$C_1 = 15\text{ pF}$			50	ns
$t_{pd0}$ Propagation delay time to logical 0 level from clear or preset to output	52	$C_1 = 15\text{ pF}$			50	ns
$t_{pd1}$ Propagation delay time to logical 1 level from clock to output	53	$C_1 = 15\text{ pF}$	10	27	50	ns
$t_{pd0}$ Propagation delay time to logical 0 level from clock to output	53	$C_1 = 15\text{ pF}$	10	18	50	ns

# TYPE SN5470 J-K FLIP-FLOP

## schematic



Component values shown are nominal.

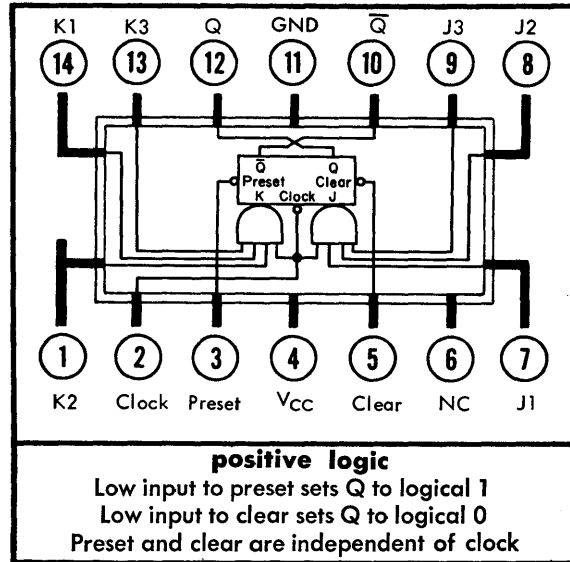
# TYPE SN5472

## J-K MASTER-SLAVE FLIP-FLOP

### logic

TRUTH TABLE		
$t_n$		$t_{n+1}$
J	K	Q
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\overline{Q_n}$

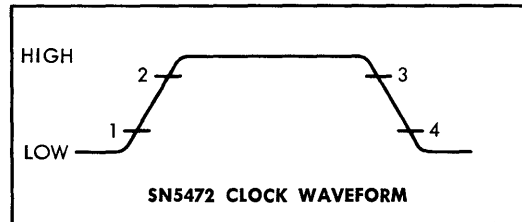
- NOTES: 1.  $J = J1 \cdot J2 \cdot J3$   
 2.  $K = K1 \cdot K2 \cdot K3$   
 3.  $t_n =$  Bit time before clock pulse.  
 4.  $t_{n+1} =$  Bit time after clock pulse.



### description

The SN5472 J-K flip-flop is based on the master-slave principle. This device has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.



### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	4.5 V to 5.5 V
Fan-Out From Each Output, N . . . . .	1 to 10
Width of Clock Pulse, $t_{p(\text{clock})}$ (See Figure 54) . . . . .	$\geq 20$ ns
Width of Preset Pulse, $t_{p(\text{preset})}$ (See Figure 55) . . . . .	$\geq 25$ ns
Width of Clear Pulse, $t_{p(\text{clear})}$ (See Figure 55) . . . . .	$\geq 25$ ns
Input Setup Time, $t_{\text{setup}}$ (See Figure 54) . . . . .	$\geq$ Applied Clock Pulse Width
Input Hold Time, $t_{\text{hold}}$ . . . . .	$\geq 0$



# TYPE SN5472 J-K MASTER-SLAVE FLIP-FLOP

## electrical characteristics, $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal	27	$V_{CC} = 4.5\text{ V}$	2			V
$V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal	27	$V_{CC} = 4.5\text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	27	$V_{CC} = 4.5\text{ V}, I_{load} = -400\ \mu\text{A}$	2.4	3.5 $\ddagger$		V
$V_{out(0)}$ Logical 0 output voltage	28	$V_{CC} = 4.5\text{ V}, I_{sink} = 16\text{ mA}$	0.22 $\ddagger$	0.4		V
$I_{in(0)}$ Logical 0 level input current at J1, J2, J3, K1, K2, or K3	29	$V_{CC} = 5.5\text{ V}, V_{in} = 0.4\text{ V}$			-1.6	mA
$I_{in(0)}$ Logical 0 level input current at preset, clear, or clock	29	$V_{CC} = 5.5\text{ V}, V_{in} = 0.4\text{ V}$			-3.2	mA
$I_{in(1)}$ Logical 1 level input current at J1, J2, J3, K1, K2, or K3	30	$V_{CC} = 5.5\text{ V}, V_{in} = 2.4\text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}, V_{in} = 5.5\text{ V}$			1	mA
$I_{in(1)}$ Logical 1 level input current at preset, clear, or clock	30	$V_{CC} = 5.5\text{ V}, V_{in} = 2.4\text{ V}$			80	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}, V_{in} = 5.5\text{ V}$			1	mA
$I_{OS}$ Short-circuit output current $\dagger$	31	$V_{CC} = 5.5\text{ V}, V_{in} = 0$	-20		-57	mA
$I_{CC}$ Supply current	30	$V_{CC} = 5\text{ V}, V_{in} = 5\text{ V}$			8	mA

$\dagger$ Not more than one output should be shorted at a time.

$\ddagger$ These typical values are at  $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$ .

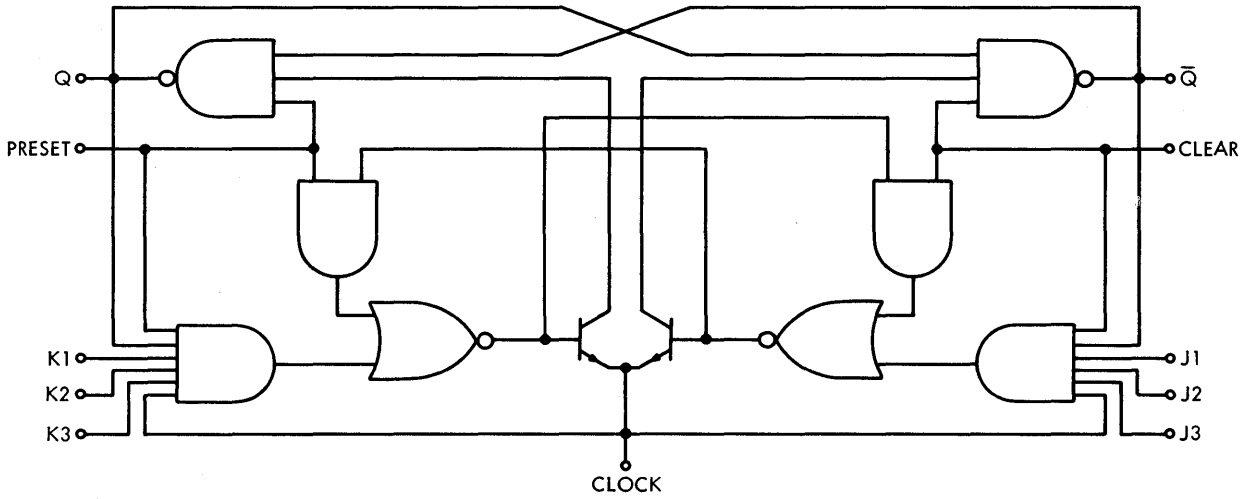
## switching characteristics, $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}, N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{clock}$ Maximum clock frequency	54	$C_1 = 15\text{ pF}$	10	15		MHz
$t_{pd1}$ Propagation delay time to logical 1 level from clear or preset to output	55	$C_1 = 15\text{ pF}$		26	50	ns
$t_{pd0}$ Propagation delay time to logical 0 level from clear or preset to output	55	$C_1 = 15\text{ pF}$		34	50	ns
$t_{pd1}$ Propagation delay time to logical 1 level from clock to output	54	$C_1 = 15\text{ pF}$	10	26	50	ns
$t_{pd0}$ Propagation delay time to logical 0 level from clock to output	54	$C_1 = 15\text{ pF}$	10	34	50	ns

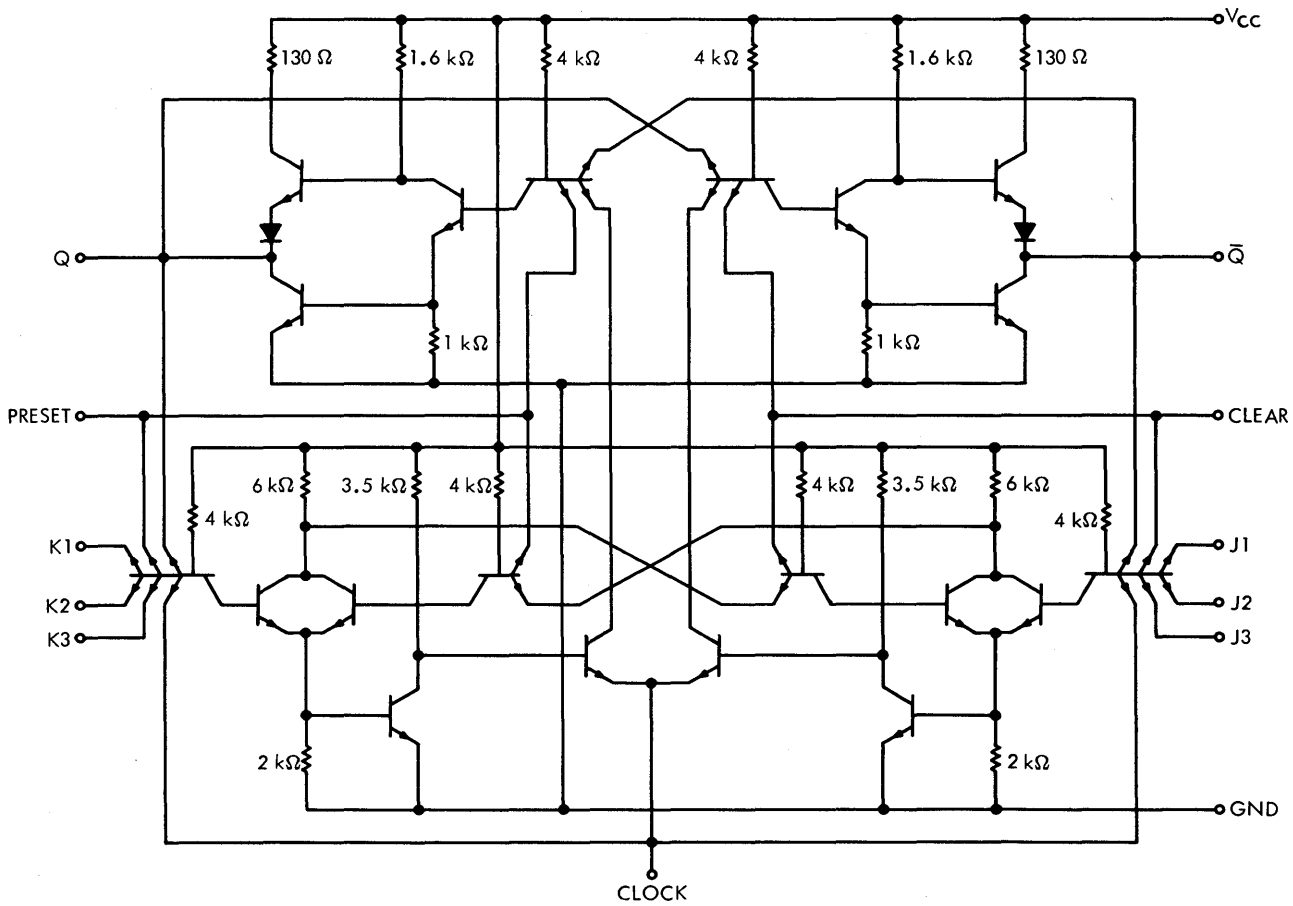
# TYPE SN5472

## J-K MASTER-SLAVE FLIP-FLOP

functional block diagram



schematic



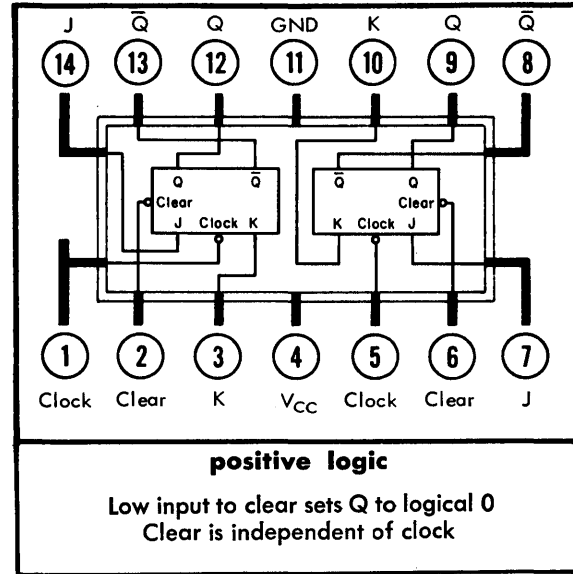
Component values shown are nominal.

# TYPE SN5473 DUAL J-K MASTER-SLAVE FLIP-FLOP

## logic

TRUTH TABLE (Each Flip-Flop)		
$t_n$		$t_{n+1}$
J	K	Q
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\bar{Q}_n$

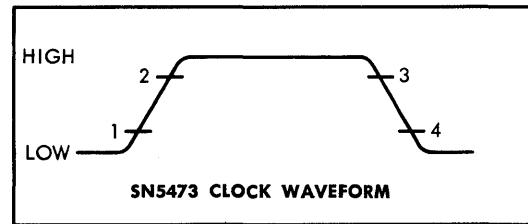
NOTES: 1.  $t_n$  = Bit time before clock pulse.  
2.  $t_{n+1}$  = Bit time after clock pulse.



## description

The SN5473 J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.



## recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	4.5 V to 5.5 V
Fan-Out From Each Output, N . . . . .	1 to 10
Width of Clock Pulse, $t_{p(\text{clock})}$ (See Figure 54) . . . . .	$\geq 20$ ns
Width of Clear Pulse, $t_{p(\text{clear})}$ (See Figure 55) . . . . .	$\geq 25$ ns
Input Setup Time, $t_{\text{setup}}$ (See Figure 54) . . . . .	$\geq$ Applied Clock Pulse Width
Input Hold Time, $t_{\text{hold}}$ . . . . .	$\geq 0$

# TYPE SN5473

## DUAL J-K MASTER-SLAVE FLIP-FLOP

electrical characteristics,  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal	32	$V_{CC} = 4.5\text{ V}$	2			V
$V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal	32	$V_{CC} = 4.5\text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	32	$V_{CC} = 4.5\text{ V}$ , $I_{load} = -400\ \mu\text{A}$	2.4	3.5 $\ddagger$		V
$V_{out(0)}$ Logical 0 output voltage	33	$V_{CC} = 4.5\text{ V}$ , $I_{sink} = 16\text{ mA}$		0.22 $\ddagger$	0.4	V
$I_{in(0)}$ Logical 0 level input current at J or K	34	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 0.4\text{ V}$			-1.6	mA
$I_{in(0)}$ Logical 0 level input current at clear or clock	34	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 0.4\text{ V}$			-3.2	mA
$I_{in(1)}$ Logical 1 level input current at J or K	35	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 2.4\text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}$ , $V_{in} = 5.5\text{ V}$			1	mA
$I_{in(1)}$ Logical 1 level input current at clear or clock	35	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 2.4\text{ V}$			80	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}$ , $V_{in} = 5.5\text{ V}$			1	mA
$I_{OS}$ Short-circuit output current $\dagger$	36	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 0$	-20		-57	mA
$I_{CC}$ Supply current (each flip-flop)	35	$V_{CC} = 5\text{ V}$ , $V_{in} = 5\text{ V}$		8		mA

$\dagger$ Not more than one output should be shorted at a time.

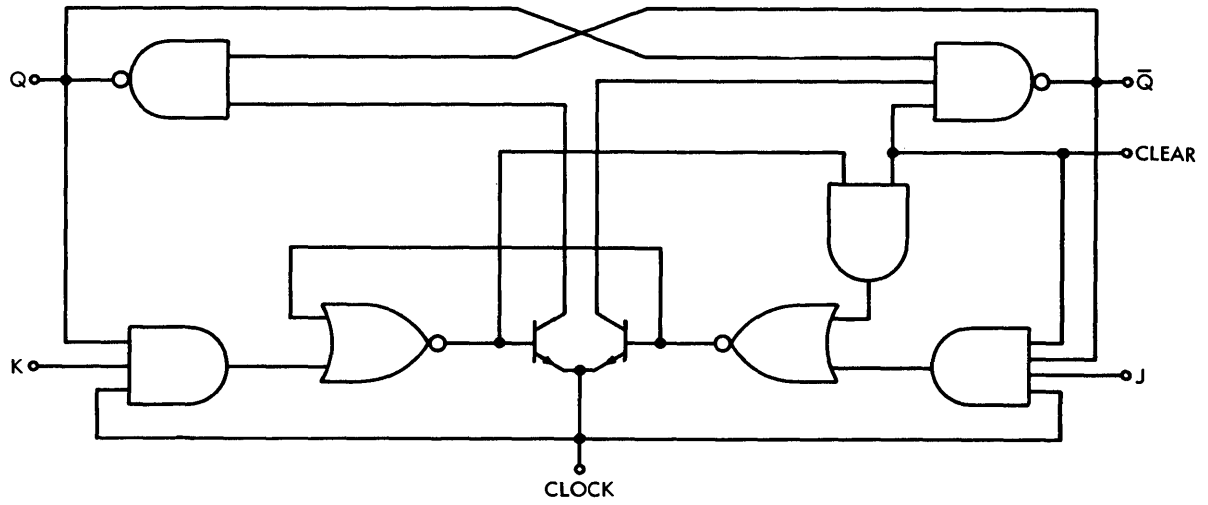
$\ddagger$ These typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $N = 10$

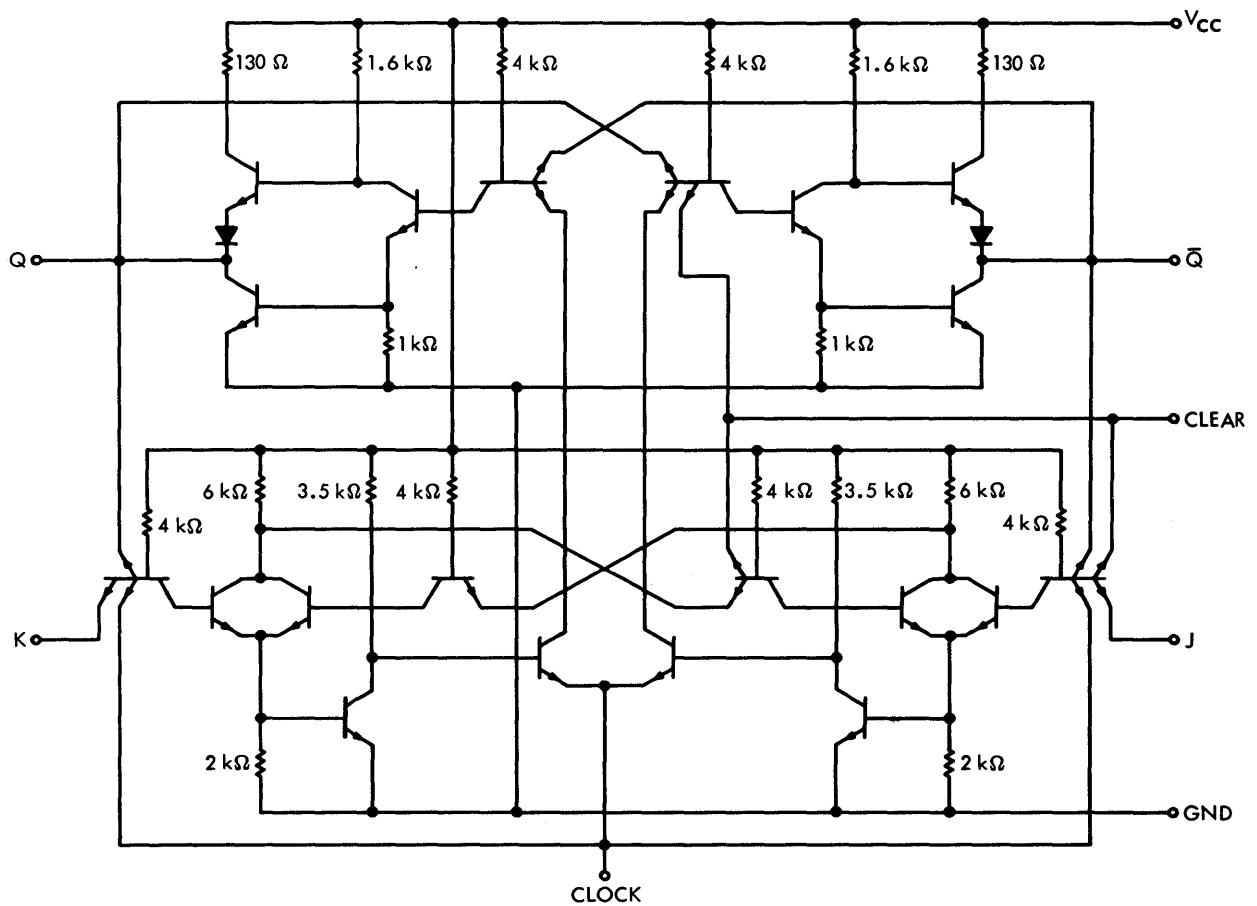
PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{clock}$ Maximum clock frequency	54	$C_1 = 15\text{ pF}$	10	15		MHz
$t_{pd1}$ Propagation delay time to logical 1 level from clear to output	55	$C_1 = 15\text{ pF}$		26	50	ns
$t_{pd0}$ Propagation delay time to logical 0 level from clear to output	55	$C_1 = 15\text{ pF}$		34	50	ns
$t_{pd1}$ Propagation delay time to logical 1 level from clock to output	54	$C_1 = 15\text{ pF}$	10	26	50	ns
$t_{pd0}$ Propagation delay time to logical 0 level from clock to output	54	$C_1 = 15\text{ pF}$	10	34	50	ns

# TYPE SN5473 DUAL J-K MASTER-SLAVE FLIP-FLOP

functional block diagram (each flip-flop)



schematic (each flip-flop)



Component values shown are nominal.

# TYPE SN5474

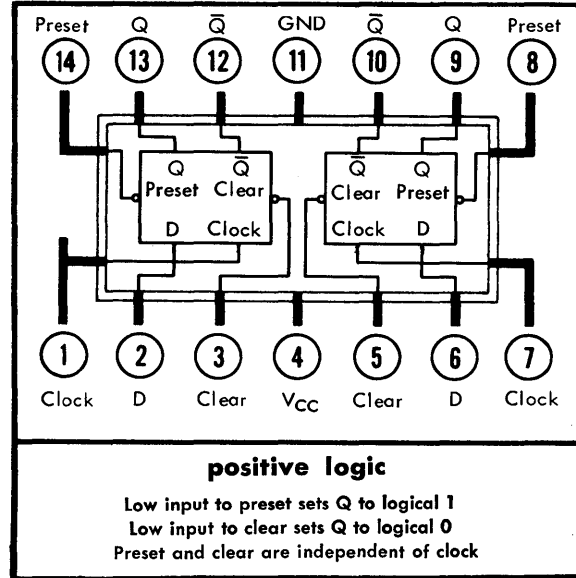
## DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP

### logic

TRUTH TABLE (Each Flip-Flop)

$t_n$	$t_{n+1}$	
INPUT D	OUTPUT Q	OUTPUT $\bar{Q}$
0	0	1
1	1	0

- NOTES: 1.  $t_n$  = bit time before clock pulse.  
 2.  $t_{n+1}$  = bit time after clock pulse.



### description

The SN5474 is a monolithic, dual, D-type, edge-triggered flip-flop featuring direct clear and preset inputs and complementary Q and  $\bar{Q}$  outputs. Input information is transferred to the Q output on the positive edge of the clock pulse.

Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed the data input (D) is locked out.

The SN5474 dual flip-flop has the same clocking characteristics as the SN5470 gated (edge-triggered) flip-flop and both are ideally suited for medium-to-high-speed applications. The SN5474 can be used at a significant saving in system power dissipation and package count in applications where input gating is not required.

### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	4.5 V to 5.5 V
Fan-Out From Each Output, N . . . . .	1 to 10
Width of Clock Pulse, $t_{p(\text{clock})}$ (See Figure 56) . . . . .	$\geq 30$ ns
Width of Preset Pulse, $t_{p(\text{preset})}$ (See Figure 53) . . . . .	$\geq 30$ ns
Width of Clear Pulse, $t_{p(\text{clear})}$ (See Figure 53) . . . . .	$\geq 30$ ns



# TYPE SN5474

## DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP

electrical characteristics,  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal	37	$V_{CC} = 4.5\text{ V}$	2			V
$V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal	37	$V_{CC} = 4.5\text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	37	$V_{CC} = 4.5\text{ V}$ , $I_{load} = -400\ \mu\text{A}$	2.4	3.5 ‡		V
$V_{out(0)}$ Logical 0 output voltage	38	$V_{CC} = 4.5\text{ V}$ , $I_{sink} = 16\text{ mA}$		0.22 ‡	0.4	V
$I_{in(0)}$ Logical 0 level input current at preset or D	39	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 0.4\text{ V}$			-1.6	mA
$I_{in(0)}$ Logical 0 level input current at clear or clock	39	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 0.4\text{ V}$			-3.2	mA
$I_{in(1)}$ Logical 1 level input current at D	40	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 2.4\text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}$ , $V_{in} = 5.5\text{ V}$			1	mA
$I_{in(1)}$ Logical 1 level input current at preset or clock	40	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 2.4\text{ V}$			80	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}$ , $V_{in} = 5.5\text{ V}$			1	mA
$I_{in(1)}$ Logical 1 level input current at clear	40	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 2.4\text{ V}$			120	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}$ , $V_{in} = 5.5\text{ V}$			1	mA
$I_{OS}$ Short-circuit output current †	41	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 0$	-20		-57	mA
$I_{CC}$ Supply current (each flip-flop)	40	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 5\text{ V}$		8.5		mA

†Not more than one output should be shorted at a time.

‡These typical values are at  $V_{CC} = 5\text{ V}$ .

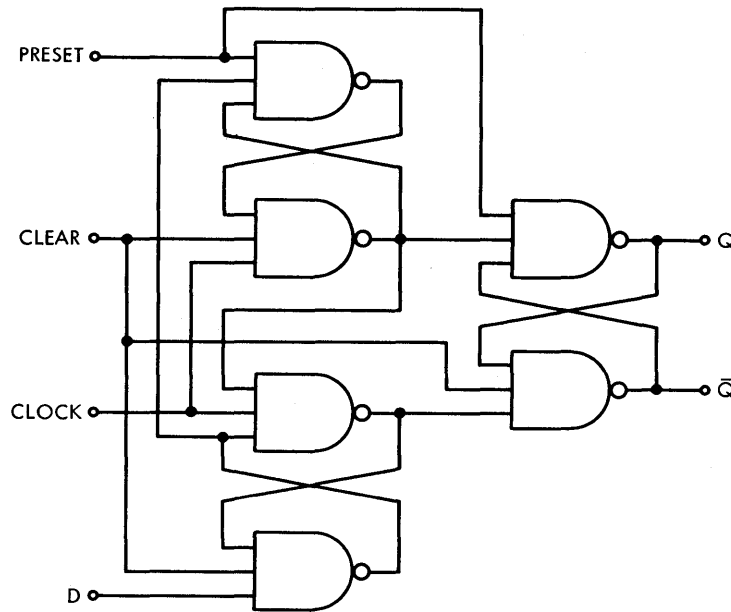
switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{clock}$ Maximum clock frequency	56	$C_1 = 15\text{ pF}$	15	25		MHz
$t_{setup}$ Minimum input setup time	56	$C_1 = 15\text{ pF}$		15	20	ns
$t_{hold}$ Minimum input hold time	56	$C_1 = 15\text{ pF}$		2	5	ns
$t_{pd1}$ Propagation delay time to logical 1 level from clear or preset to output	53	$C_1 = 15\text{ pF}$			25	ns
$t_{pd0}$ Propagation delay time to logical 0 level from clear or preset to output	53	$C_1 = 15\text{ pF}$			40	ns
$t_{pd1}$ Propagation delay time to logical 1 level from clock to output	56	$C_1 = 15\text{ pF}$	10	28	35	ns
$t_{pd0}$ Propagation delay time to logical 0 level from clock to output	56	$C_1 = 15\text{ pF}$	10	20	50	ns

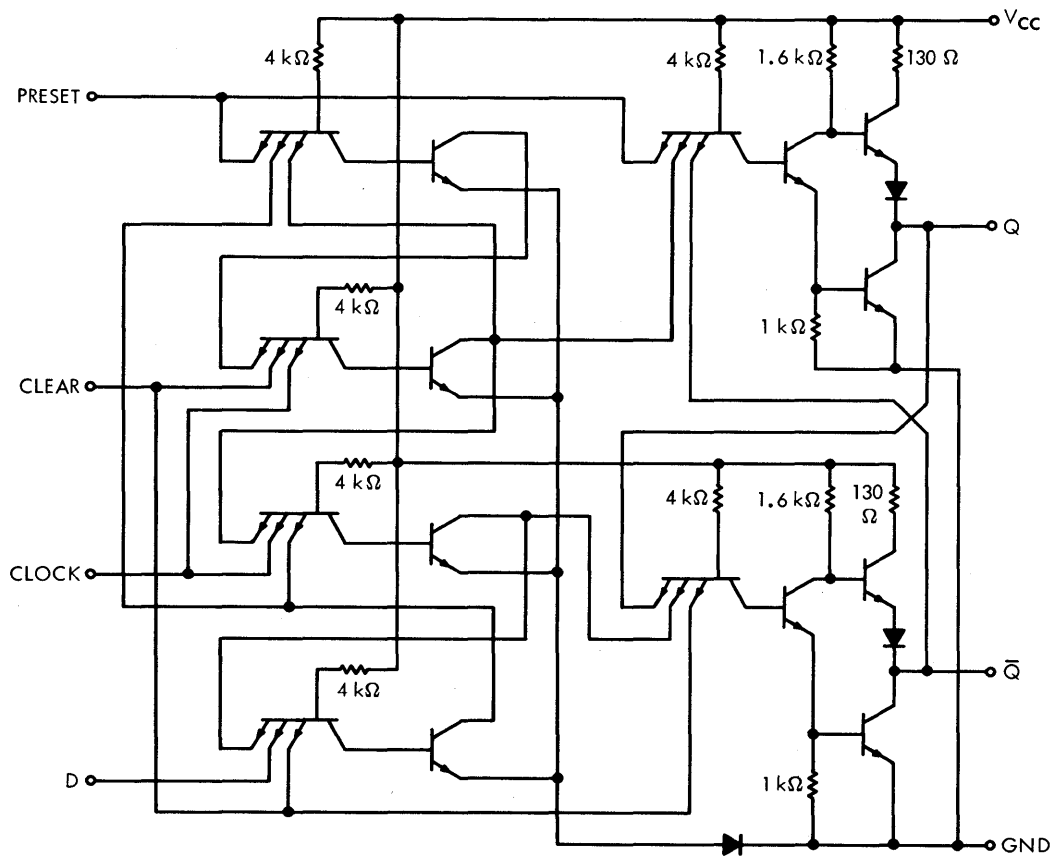
# TYPE SN5474

## DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP

functional block diagram (each flip-flop)



schematic (each flip-flop)



Component values shown are nominal.

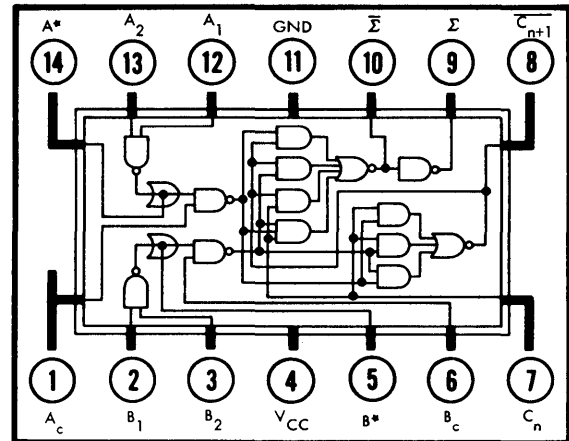
# TYPE SN5480 GATED FULL ADDER

## logic

TRUTH TABLE (See Notes 1, 2, and 3)

$C_n$	B	A	$\overline{C_{n+1}}$	$\overline{\Sigma}$	$\Sigma$
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

- NOTES: 1.  $A = A^* \cdot A_c$ ,  $B = B^* \cdot B_c$   
 where  $A^* = A_1 \cdot A_2$ ,  $B^* = B_1 \cdot B_2$   
 2. When  $A^*$  or  $B^*$  are used as inputs,  $A_1$  and  $A_2$  or  $B_1$  and  $B_2$  respectively must be connected to GND.  
 3. When  $A_1$  and  $A_2$  or  $B_1$  and  $B_2$  are used as inputs,  $A^*$  or  $B^*$  respectively must be open or used to perform Dot-OR logic.



## description

The SN5480 is a single-bit, high-speed, binary full adder with gated complementary inputs, complementary sum ( $\Sigma$  and  $\overline{\Sigma}$ ) outputs and inverted carry output. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit (see schematic diagram) utilizes diode-transistor logic (DTL) for the gated inputs, and high-speed, high-fan-out transistor-transistor logic (TTL) for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform full-adder functions.

## recommended operating conditions

Supply Voltage $V_{CC}$	4.5 V to 5.5 V
Maximum Allowable Fan-Out From Outputs:	
$C_{n+1}$ , N	1 to 5
$\Sigma$ or $\overline{\Sigma}$ , N	1 to 10
$A^*$ or $B^*$ , N	1 to 3

# TYPE SN5480

## GATED FULL ADDER

electrical characteristics,  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage	42 and 43	$V_{CC} = 4.5\text{ V}$ , $V_{in(0)} = 0.8\text{ V}$ , $V_{out(1)} \geq 2.4\text{ V}$ , $V_{out(0)} \leq 0.4\text{ V}$	2			V
$V_{in(0)}$ Logical 0 input voltage	42 and 43	$V_{CC} = 4.5\text{ V}$ , $V_{in(1)} = 2\text{ V}$ , $V_{out(1)} \geq 2.4\text{ V}$ , $V_{out(0)} \leq 0.4\text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	43	$V_{CC} = 4.5\text{ V}$	2.4	3.5 ‡		V
$V_{out(0)}$ Logical 0 output voltage	42	$V_{CC} = 4.5\text{ V}$		0.22 ‡	0.4	V
$I_{in(0)}$ Logical 0 level input current at $A_1$ , $A_2$ , $B_1$ , $B_2$ , $A_C$ or $B_C$	44	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 0.4\text{ V}$			-1.6	mA
$I_{in(0)}$ Logical 0 level input current at $A^*$ or $B^*$	45	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 0.4\text{ V}$			-2.6	mA
$I_{in(0)}$ Logical 0 level input current at $C_n$	45	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 0.4\text{ V}$ (all inputs and outputs open)			-8	mA
$I_{in(1)}$ Logical 1 level input current at $A_1$ , $A_2$ , $B_1$ , $B_2$ , $A_C$ or $B_C$	46	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 2.4\text{ V}$			15	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}$ , $V_{in} = 5.5\text{ V}$			1	mA
$I_{in(1)}$ Logical 1 level input current at $C_n$	47	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 2.4\text{ V}$			200	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}$ , $V_{in} = 5.5\text{ V}$			1	mA
$I_{OS}$ Short-circuit output current at $\Sigma$ or $\Sigma^\dagger$	48	$V_{CC} = 5.5\text{ V}$	-20		-57	mA
$I_{OS}$ Short-circuit output current at $C_{n+1}^\dagger$	48	$V_{CC} = 5.5\text{ V}$	-20		-70	mA
$I_{CC}$ Supply Current	49	$V_{CC} = 5\text{ V}$		21		mA

† Not more than one output should be shorted at a time.

‡ These typical values are at  $V_{CC} = 5\text{ V}$ .

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER ¶	FROM INPUT	TO OUTPUT	FIGURE 57 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd1}$	$C_n$	$C_{n+1}$	1	$N = 5$		13	17	ns
$t_{pd0}$			2	$N = 5$		3	7	ns
$t_{pd1}$	$B_C$	$C_{n+1}$	3	$N = 5$		18	25	ns
$t_{pd0}$			4	$N = 5$		38	55	ns
$t_{pd1}$	$A_C$	$\Sigma$	5	$N = 10$		52	70	ns
$t_{pd0}$			6	$N = 10$		62	80	ns
$t_{pd1}$	$B_C$	$\Sigma$	7	$N = 10$		38	55	ns
$t_{pd0}$			8	$N = 10$		56	75	ns
$t_{pd1}$	$A_1$	$A^*$	9	$C_L = 15\text{ pF}$		48	65	ns
$t_{pd0}$			10	$C_L = 15\text{ pF}$		17	25	ns
$t_{pd1}$	$B_1$	$B^*$	11	$C_L = 15\text{ pF}$		48	65	ns
$t_{pd0}$			12	$C_L = 15\text{ pF}$		17	25	ns

¶  $t_{pd1}$  is propagation delay time to logical 1 level.  $t_{pd0}$  is propagation delay time to logical 0 level.

# TYPE SN5480 GATED FULL ADDER

## TYPICAL APPLICATIONS

### n-bit binary adder or subtractor (see figures F and G)

The SN5480 is designed specifically for N-bit adder or subtractor operations without external gates or inverters. In both applications, the sum or difference functions are generated in parallel while the carry functions are obtained serially. When the number of stages is small, the add or subtract time determines the maximum system clock rate. However, as the number of bits increases, the time required for the carry function to ripple through each bit becomes the limiting factor. Normally the ripple time of adders built with standard integrated circuits is excessive, and the resulting system speed is so slow that other more complex methods are required to perform these functions.

In the SN5480, two methods are used to reduce the carry delay. The carry circuit employs a high-speed Darlington output, and the logic gating has only one inversion between the  $C_n$  input and the  $\bar{C}_{n+1}$  output. This logic configuration results in an inverted carry output, and consequently an inverted carry input to the succeeding stage. To counteract this inverted input without sacrificing propagation time through the carry, gates are provided within the circuit to invert the A and B inputs and the resulting sum or difference output. This

interconnection method is illustrated by bit 2 and bit 4 of the adder (figure F). The inverted carry output is a true carry from bit 2 and bit 4, enabling the use of noninverted A and B inputs for the odd-numbered bits.

When performing subtraction (figure G) the  $C_n$  input to bit 1 is connected to a logical 1 and input bits and input control functions for the subtrahend (memory or register B) are effectively inverted.

The input control is used to disable the A and B inputs when memory or register information is being shifted. A logical 0 applied to this line will bring each sum or difference output to a logical 0 condition and maintain this level regardless of the state of the input information into each bit. For the adder (figure F), input control is applied to  $A_2$  and  $B_2$  of odd-numbered bits and to  $A_c$  and  $B_c$  of even-numbered bits. For the subtractor (figure G), input control is applied to  $A_2$  and  $B_c$  of the odd-numbered bits and to  $A_c$  and  $B_2$  of the even-numbered bits. These alternating patterns are necessary to complement the varying input sequence which they control.

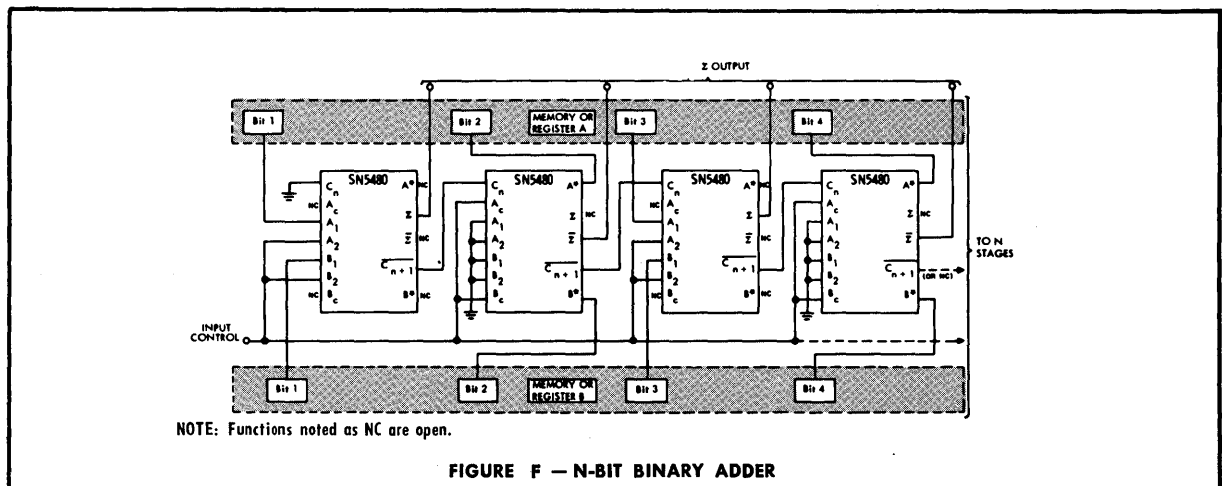


FIGURE F — N-BIT BINARY ADDER

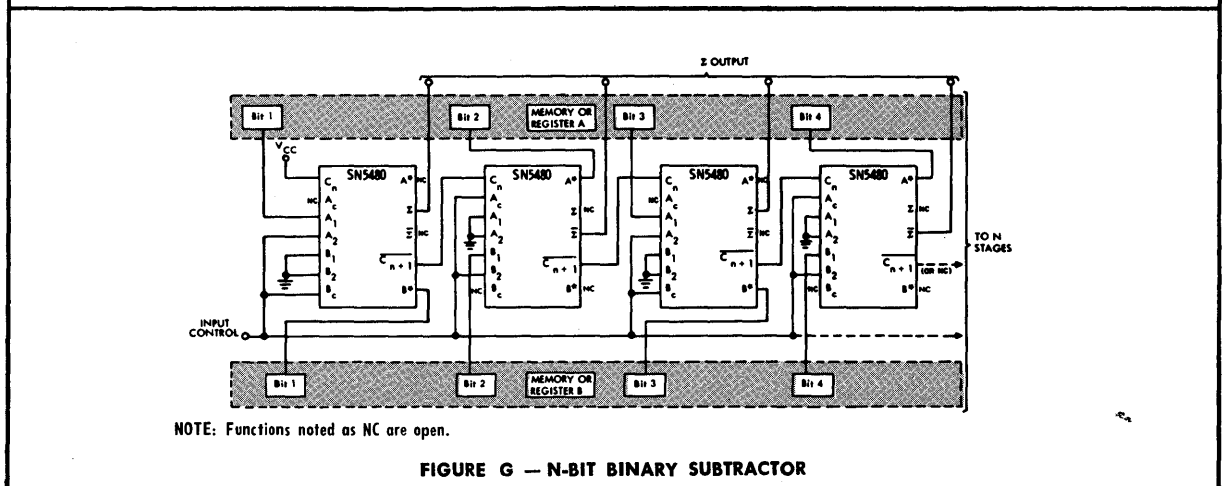


FIGURE G — N-BIT BINARY SUBTRACTOR

# TYPE SN5480 GATED FULL ADDER

## TYPICAL APPLICATIONS

### n-bit binary adder with register selection (see figure H)

This application fully utilizes the flexibility of the input gating available within the SN5480. Two "A" registers and two "B" registers drive a single adder for each bit required. Register selection is performed internally for registers A<sub>1</sub> and B<sub>1</sub> and externally by a type SN15 946 DTL gate for registers A<sub>2</sub> and B<sub>2</sub>. Dot-OR logic is performed at the A\* and B\* nodes within the adder when the register selection is made.

Operation is as follows: To add the contents of Register A<sub>1</sub> to Register B<sub>1</sub>, A<sub>2</sub> and B<sub>2</sub> control lines are brought to the logical 0 state. (If the input to these lines is from a logic gate, fan-out rules should be observed.) In similar fashion, the contents of register A<sub>1</sub> are added to register B<sub>2</sub> by holding A<sub>2</sub> and B<sub>1</sub> control lines at a logical 0. Four register combinations may be used. Even-numbered input bits from each register must be inverted since the A\* and B\* inputs are being used to perform Dot-OR logic. This is not a configuration restriction for flip-flop type registers and memories, but may require additional logic elements if other storage configurations are used as inputs.

The input control function is available as in the previous application and is implemented by bringing all four register control lines and the input control line to a logical 0 level. This condition ensures a logical 0 at each Σ output regardless of "A" and "B" register logic levels.

Up to four "A" registers and four "B" registers may be implemented in a fashion analogous to that shown in figure H. Inputs from the register-control gates (SN15 946) of the additional registers would be Dot-OR connected with A<sub>2</sub> and B<sub>2</sub> registers at the A\* and B\* inputs.

To perform N-bit subtraction, the C<sub>n</sub> input at bit 1 is connected to a logical 1 and bit inputs from each register or memory used as a subtrahend must consist of the complement of bit inputs shown for the adder addend. Input control remains the same.

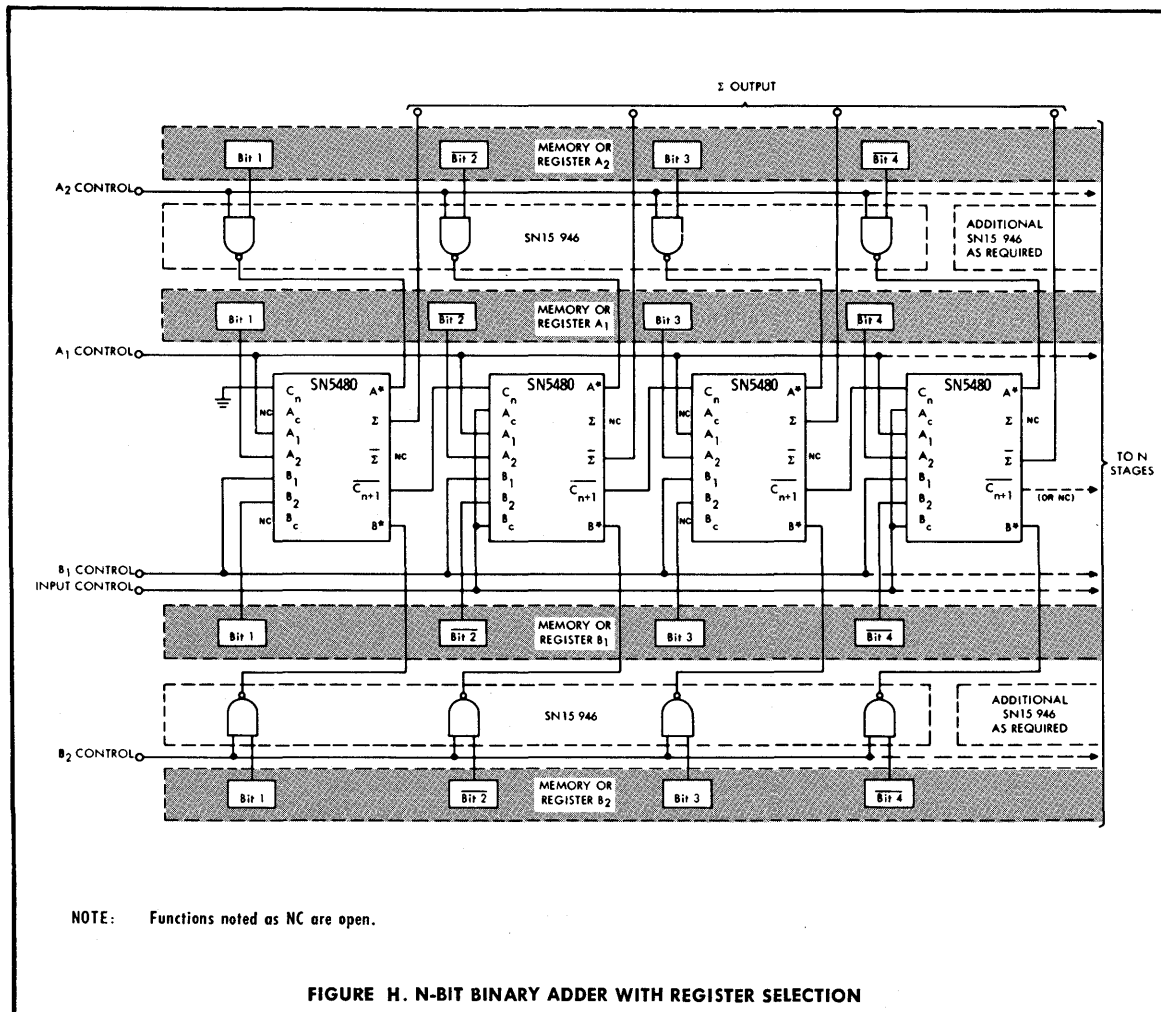
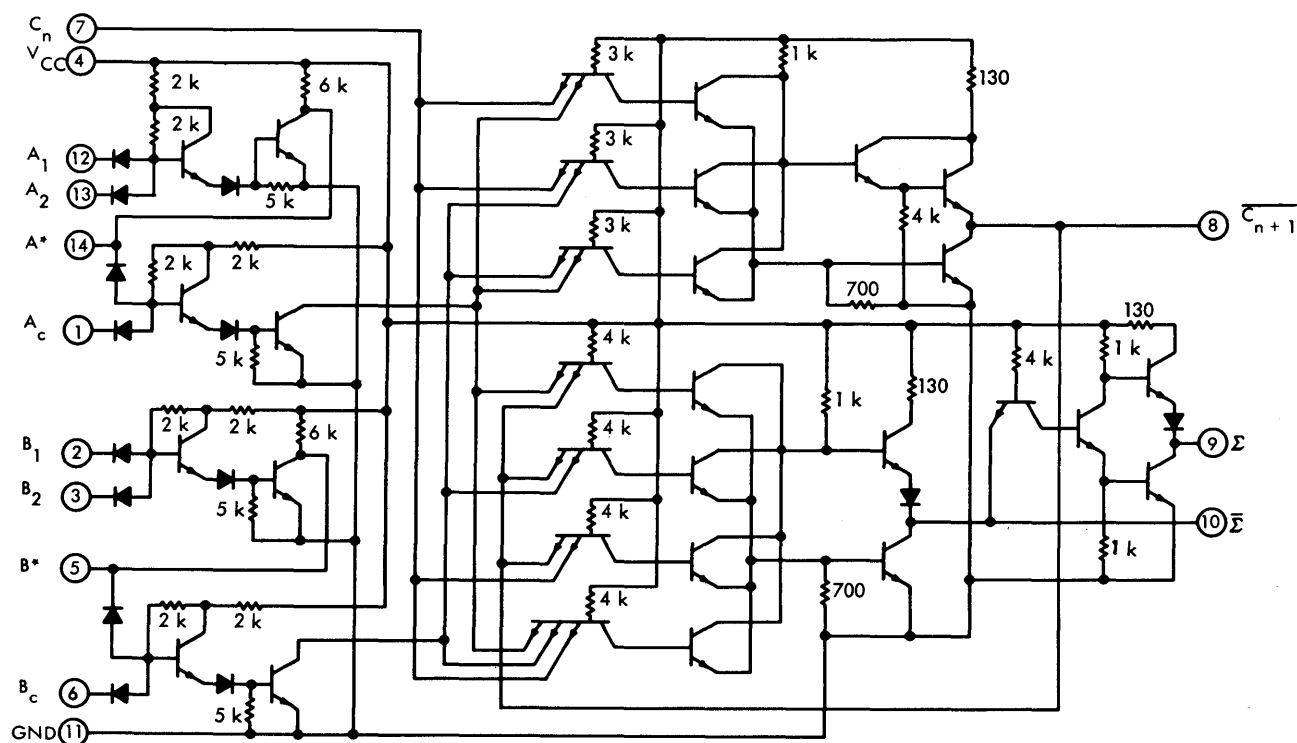


FIGURE H. N-BIT BINARY ADDER WITH REGISTER SELECTION

# TYPE SN5480 GATED FULL ADDER

schematic diagram

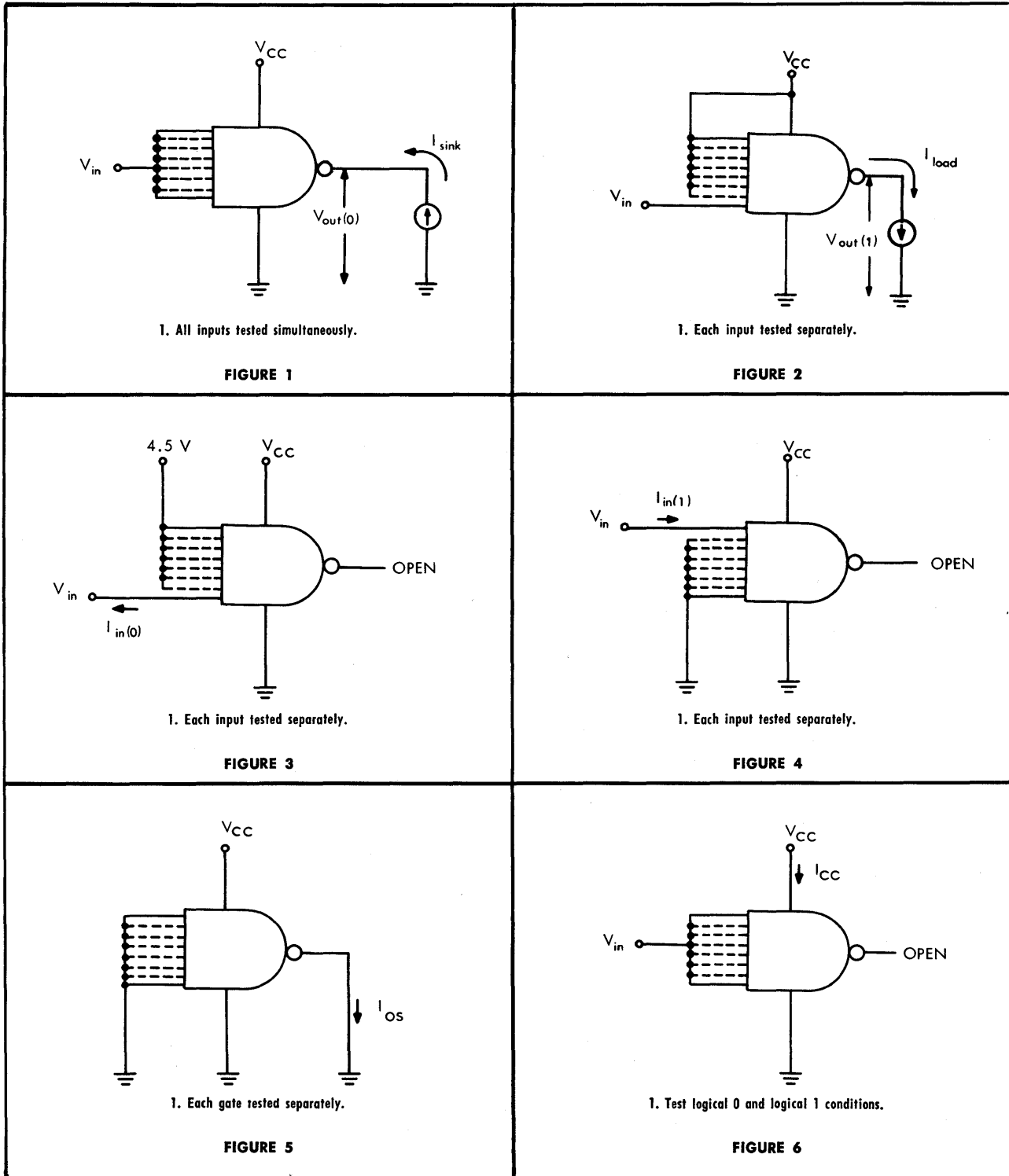


Component values shown are nominal.  
Resistor values are in ohms.



PARAMETER MEASUREMENT INFORMATION

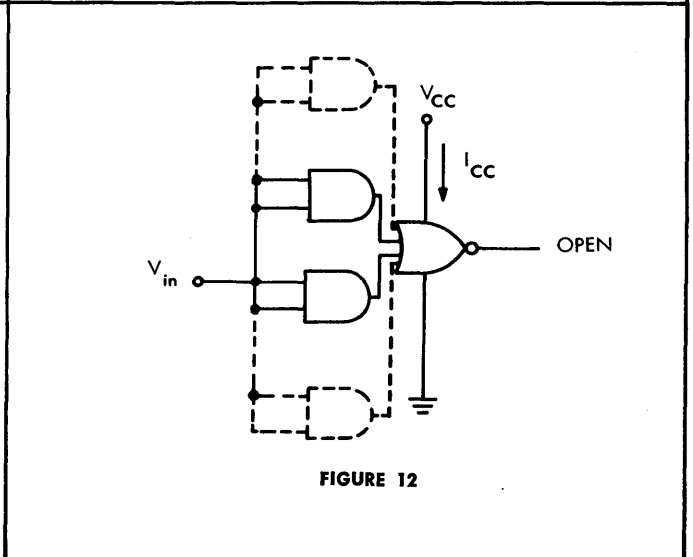
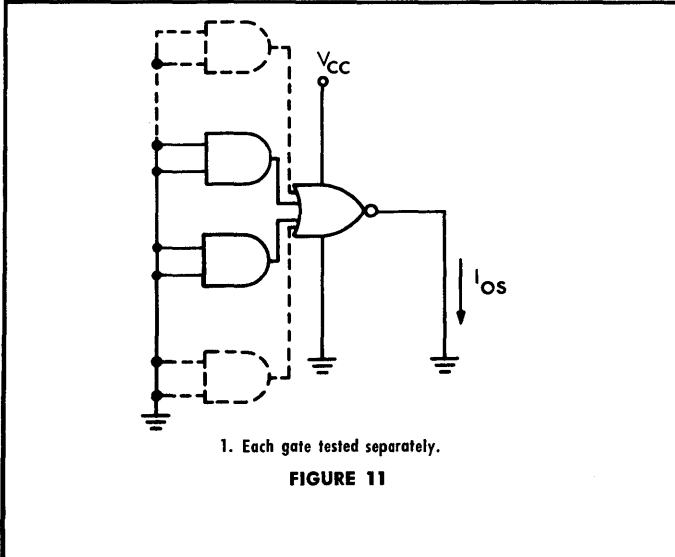
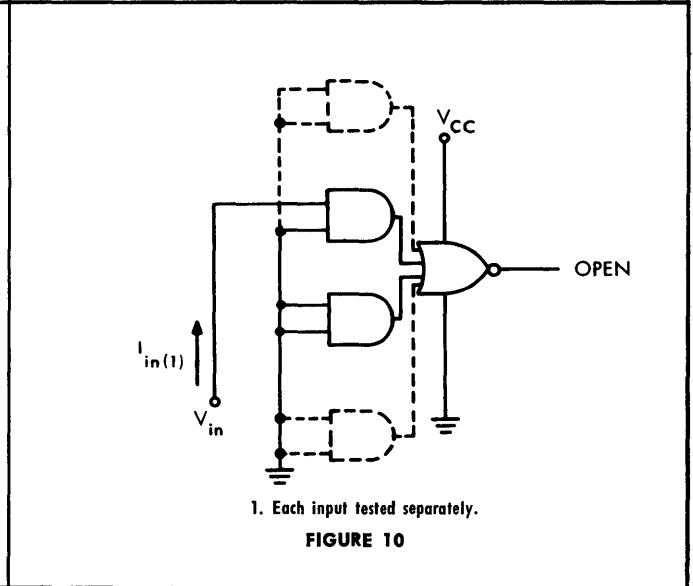
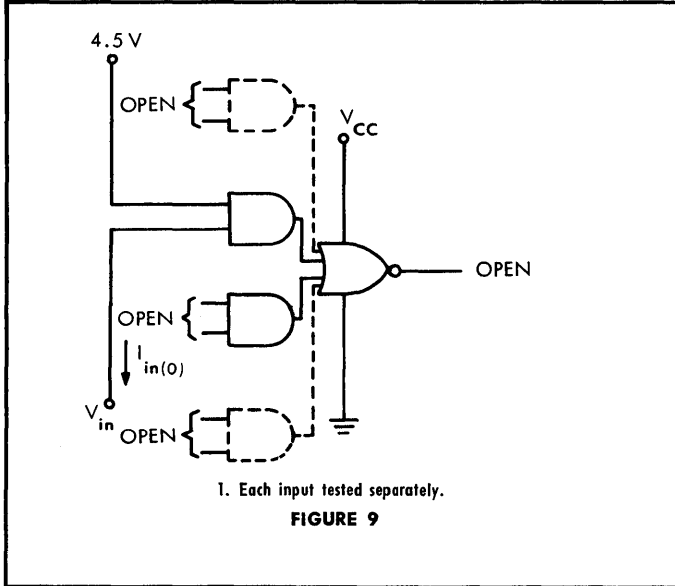
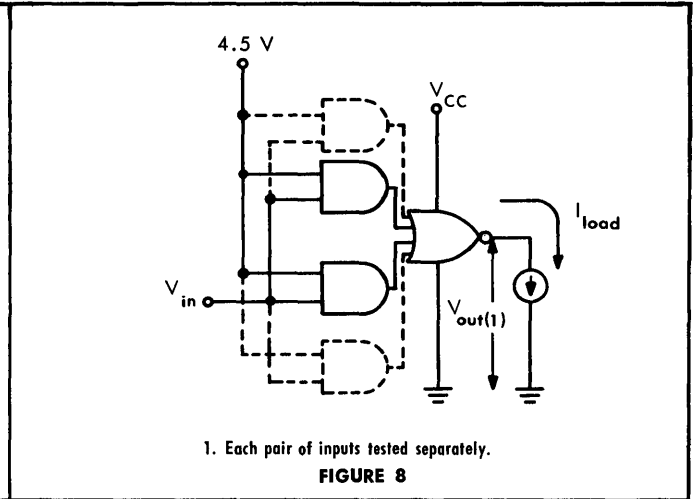
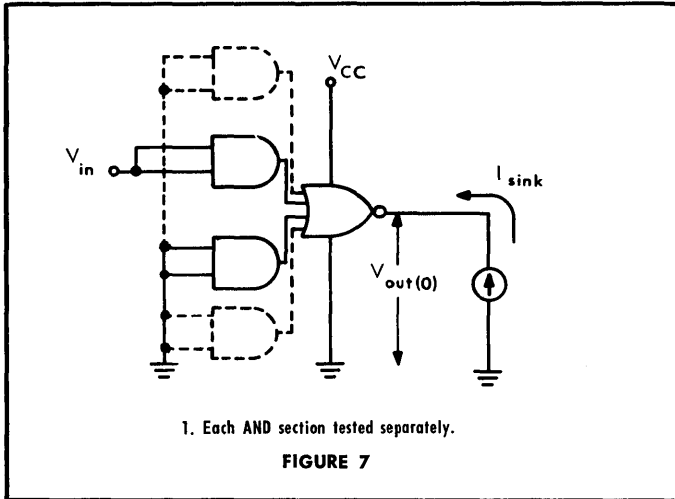
d-c test circuits§



§Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

d-c test circuits § (continued)



§ Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

d-c test circuits<sup>§</sup> (continued)

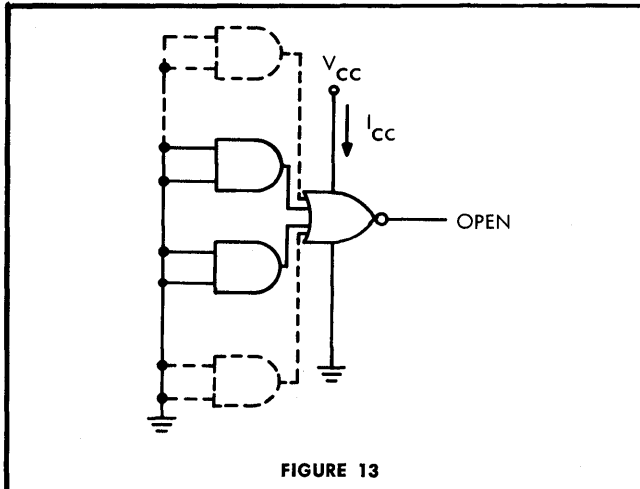


FIGURE 13

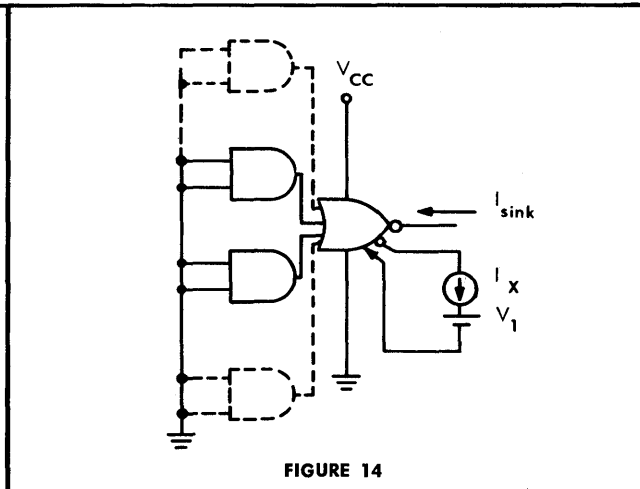


FIGURE 14

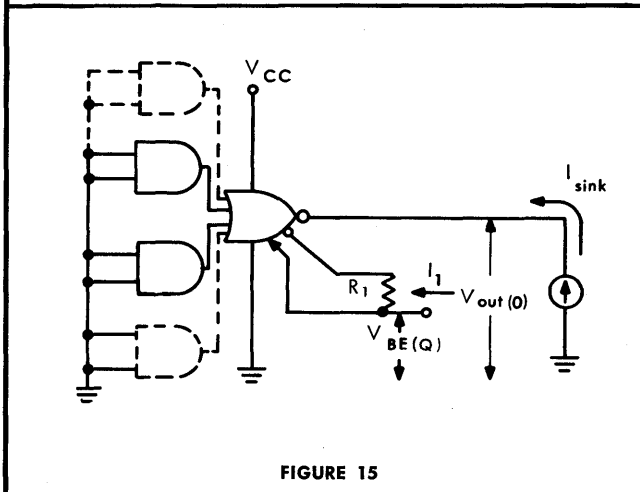


FIGURE 15

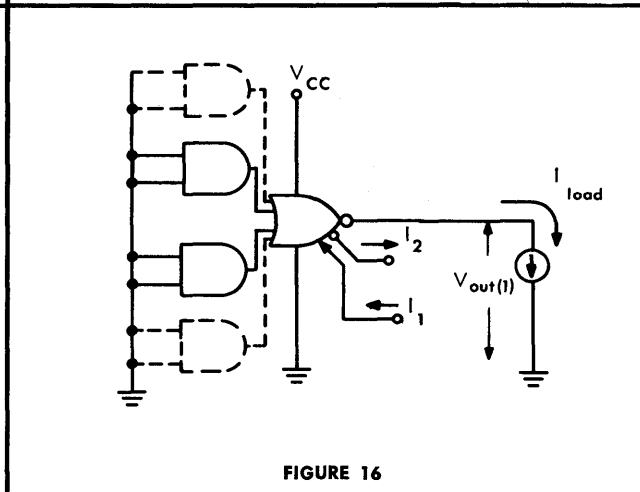


FIGURE 16

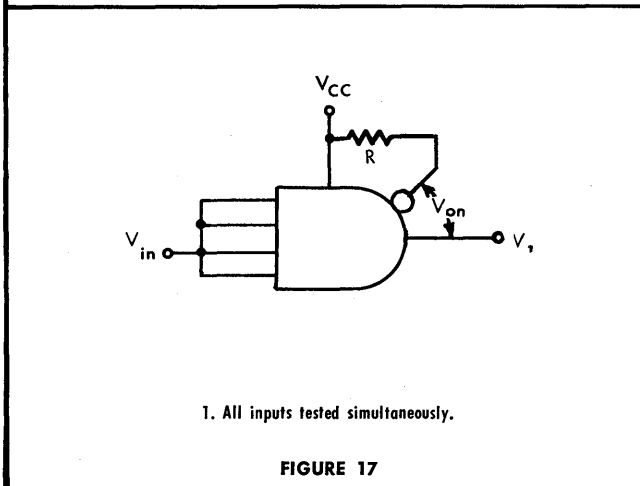


FIGURE 17

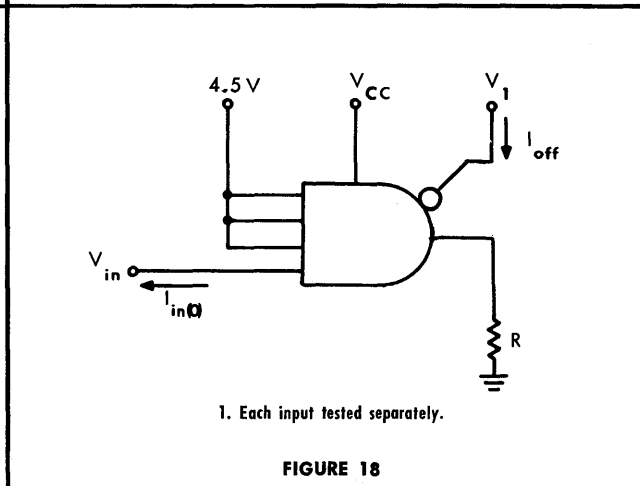
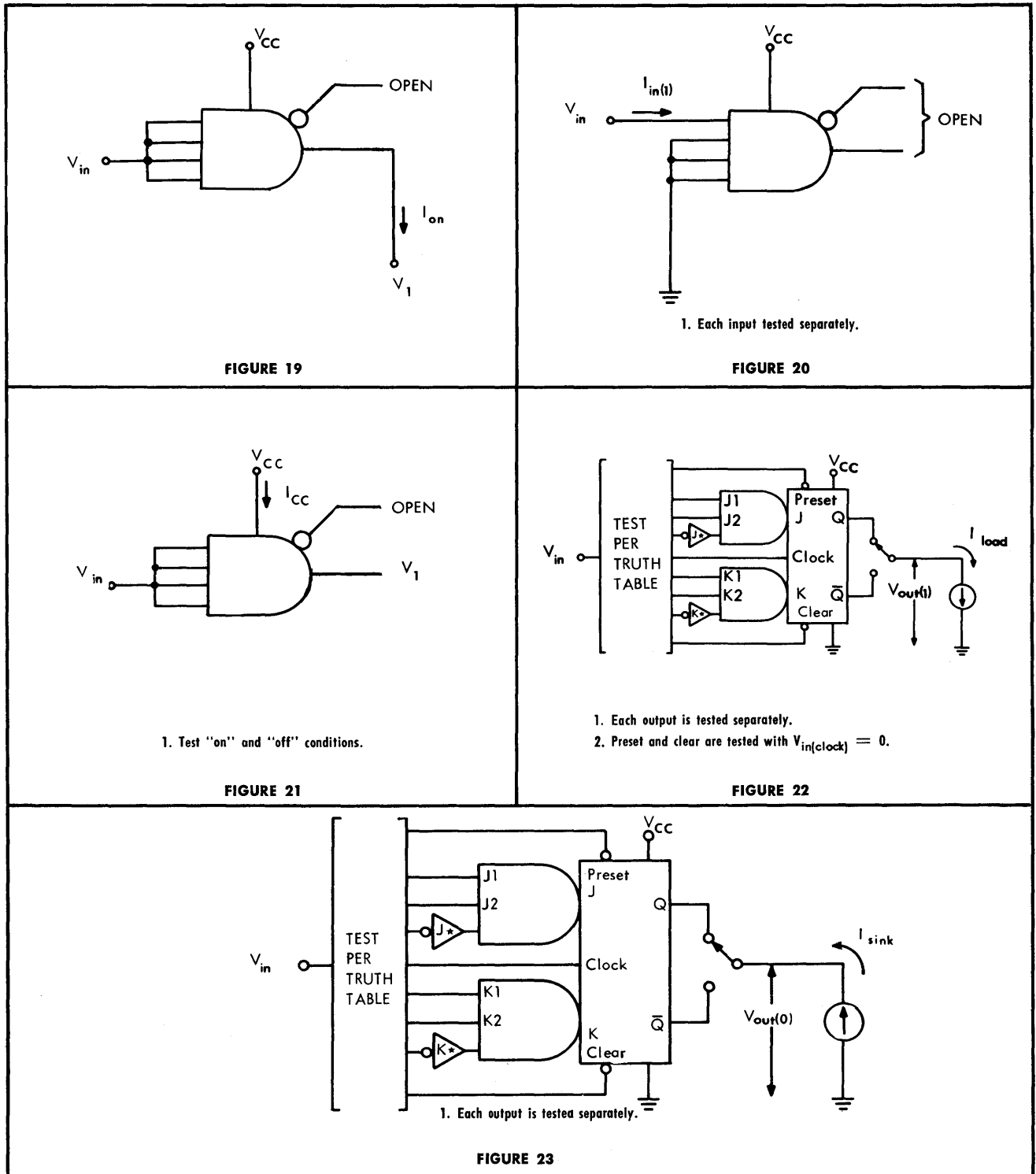


FIGURE 18

<sup>§</sup>Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

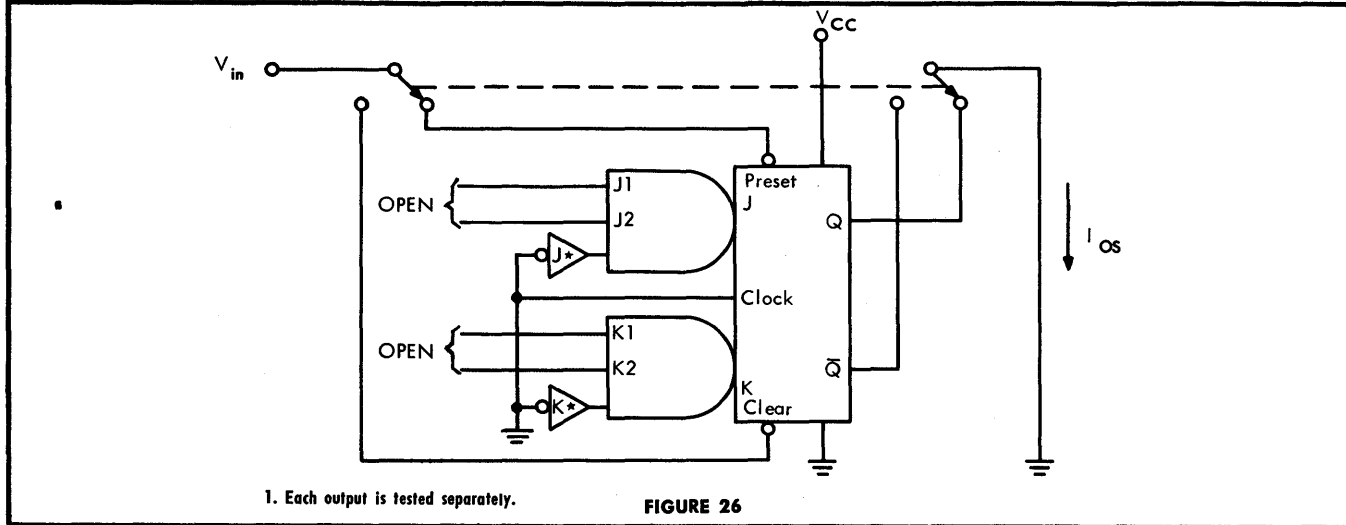
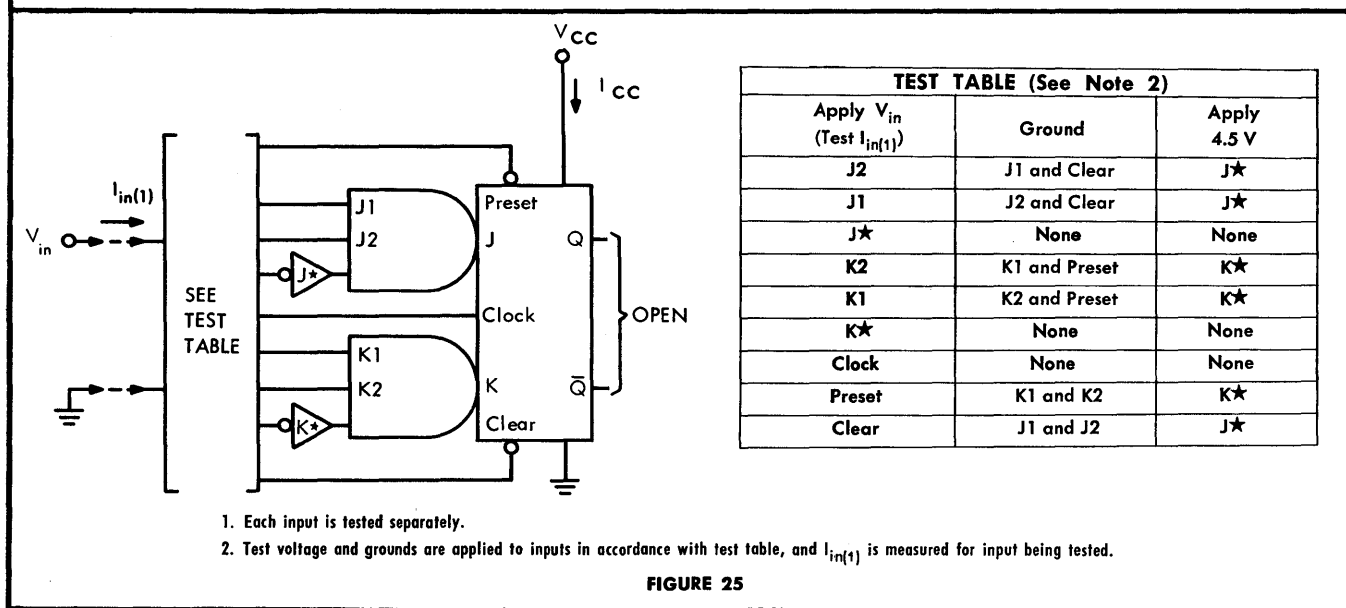
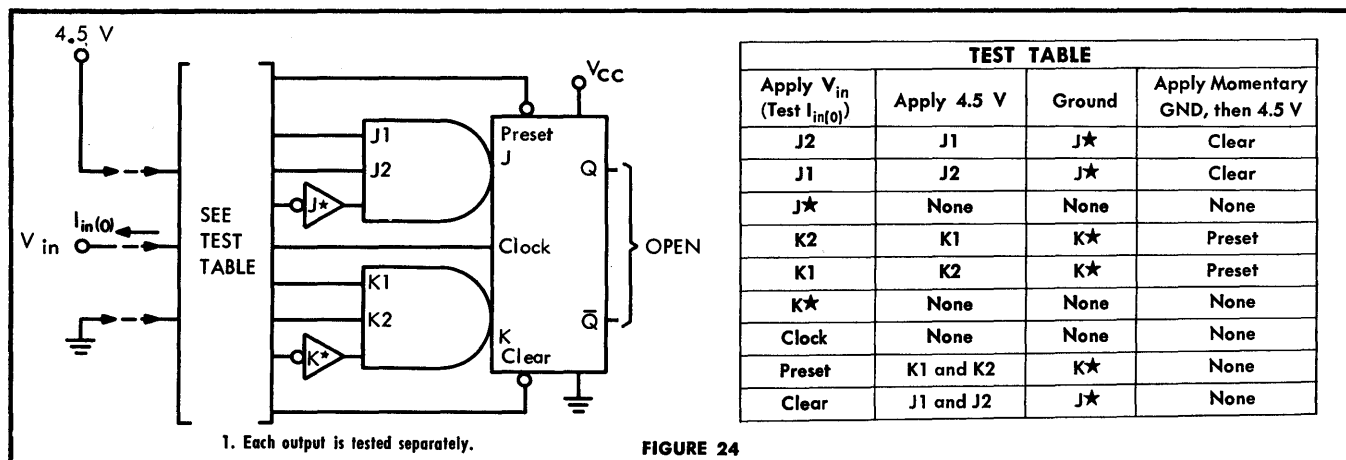
d-c test circuits§ (continued)



§ Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

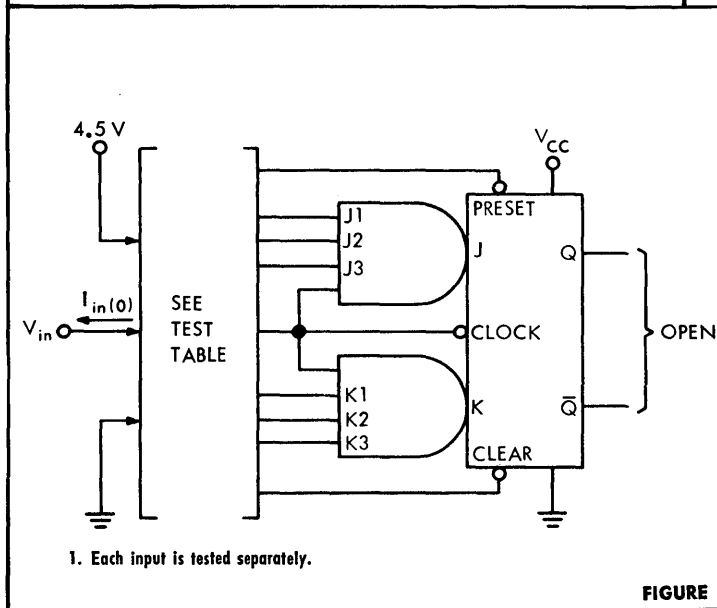
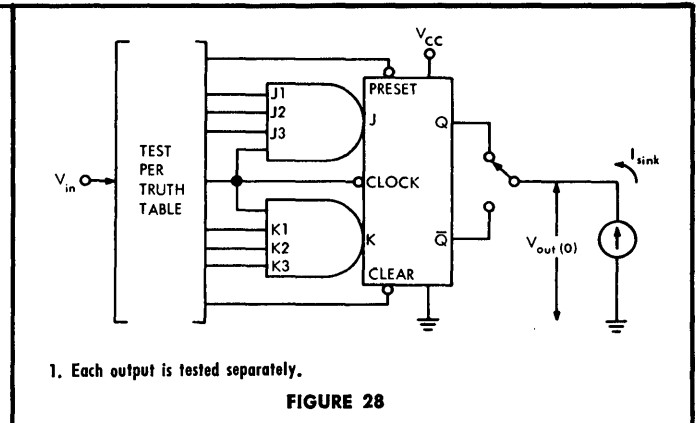
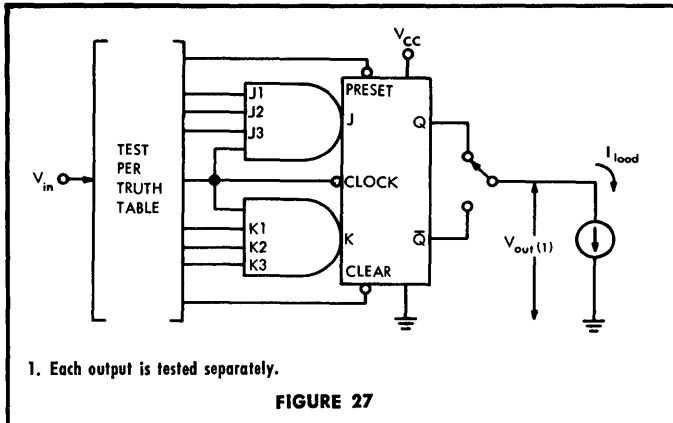
**d-c test circuits§ (continued)**



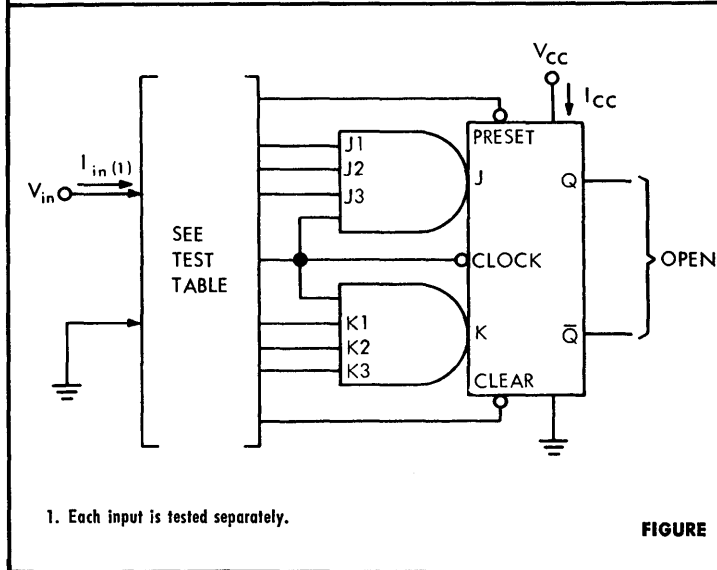
§ Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

d-c test circuits§ (continued)



TEST TABLE		
Apply $V_{in}$ (Test <sub>in(0)</sub> )	Apply Momentary GND, then 4.5 V	Apply 4.5 V
Clock	Preset	J1, J2, J3, K1, K2, and K3
Clock	Clear	J1, J2, J3, K1, K2, and K3
Preset	None	J1, J2, J3, K1, K2, and K3
Clear	None	J1, J2, J3, K1, K2, and K3
J1	Clear	Clock, J2, and J3
J2	Clear	Clock, J1, and J3
J3	Clear	Clock, J1, and J2
K1	Preset	Clock, K2, and K3
K2	Preset	Clock, K1, and K3
K3	Preset	Clock, K1, and K2

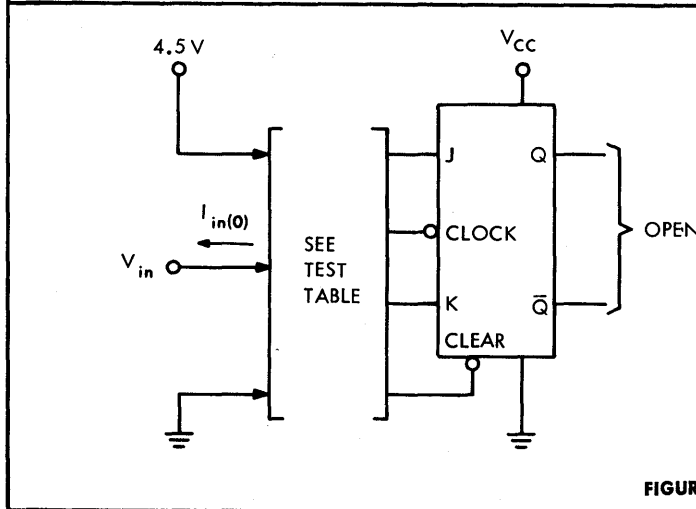
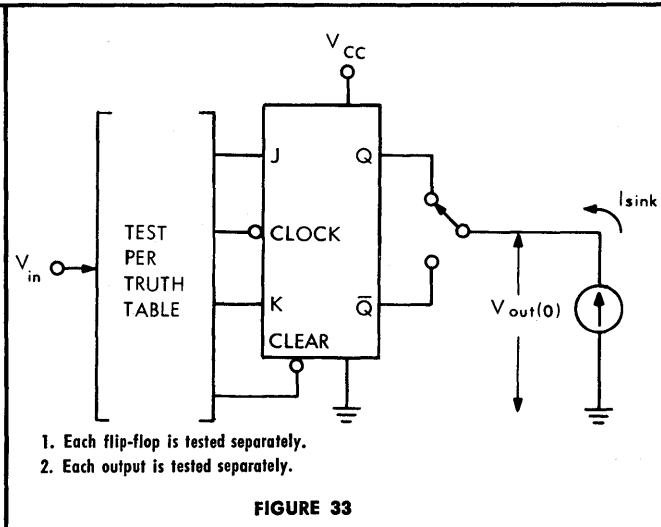
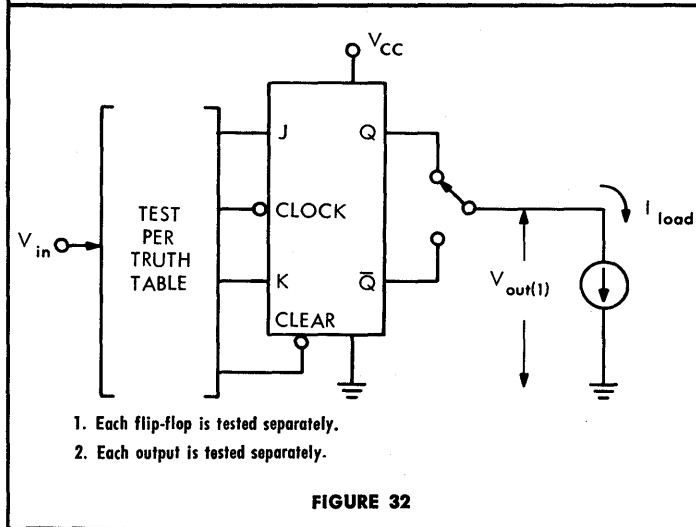
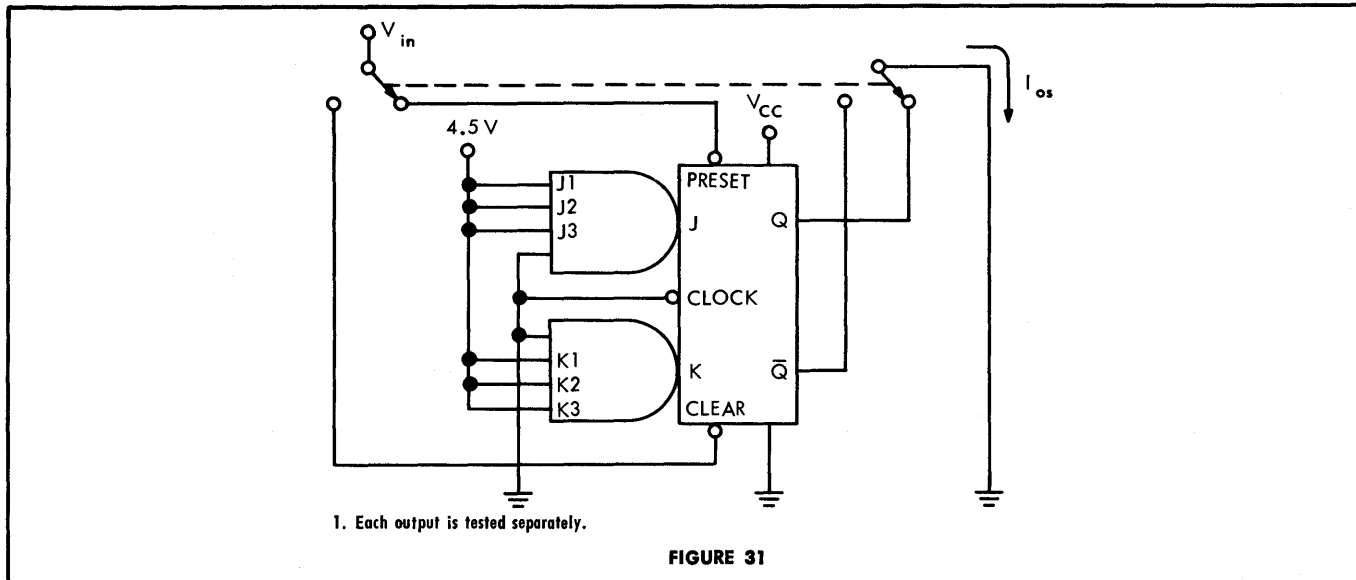


TEST TABLE	
Apply $V_{in}$ (Test <sub>in(1)</sub> )	Ground
Clock	Preset, Clear, J1, J2, J3, K1, K2, and K3
Preset	Clock, K1, K2, and K3
Clear	Clock, J1, J2, and J3
J1	Clock, Clear, J2, and J3
J2	Clock, Clear, J1, and J3
J3	Clock, Clear, J1, and J2
K1	Clock, Preset, K2, and K3
K2	Clock, Preset, K1, and K3
K3	Clock, Preset, K1, and K2

§Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

**d-c test circuits § (continued)**



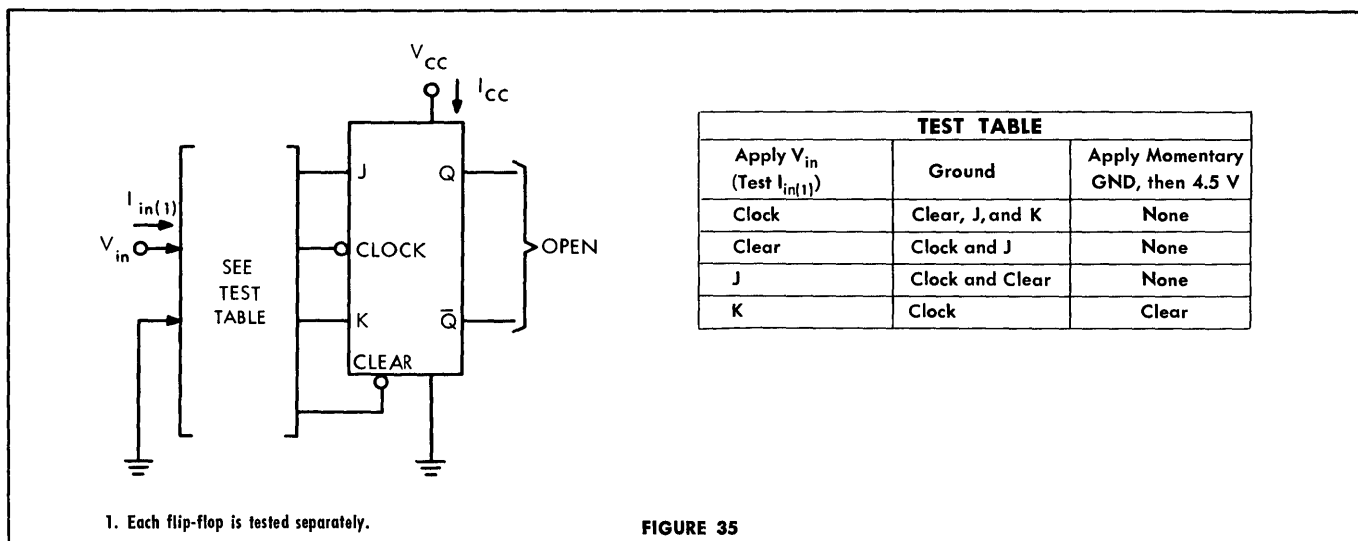
TEST TABLE		
Apply $V_{in}$ (Test $I_{in(0)}$ )	Apply Momentary GND	Apply 4.5 V
Clock	Clear (See Note 2)	J and K
Clear	None	Clock and J
J	Q (See Note 3)	Clock and Clear
K	$\bar{Q}$ (See Note 3)	Clock and Clear

1. Each flip-flop is tested separately.
2. Apply momentary ground, then 4.5 V.
3. After application of momentary ground, Q and  $\bar{Q}$  are left floating.
4. Ground all inputs of the unused flip-flop.

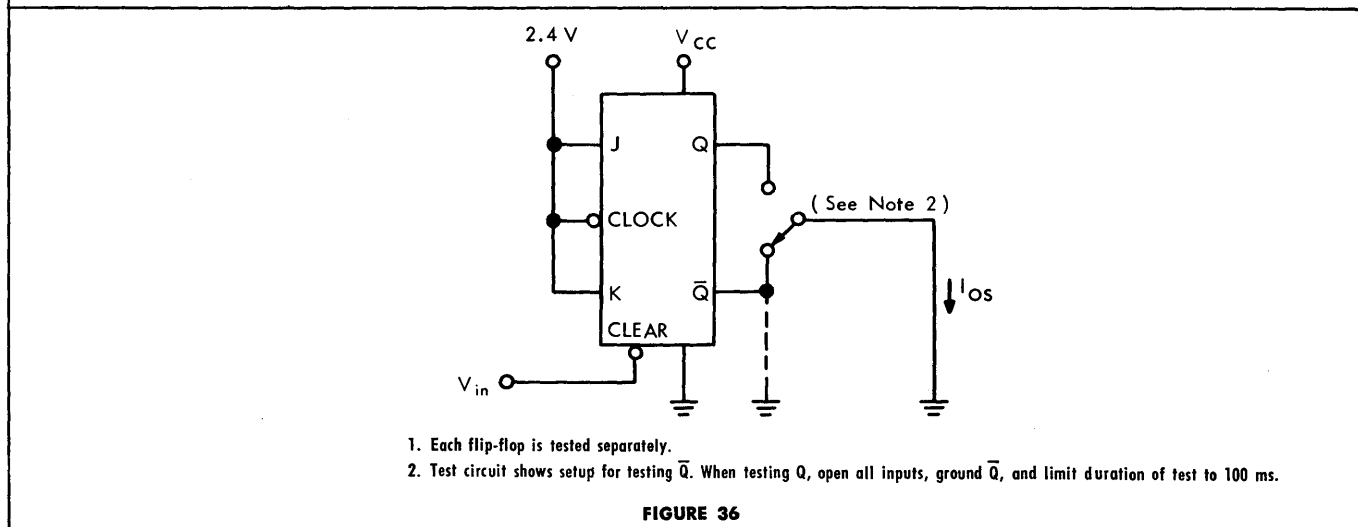
§ Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

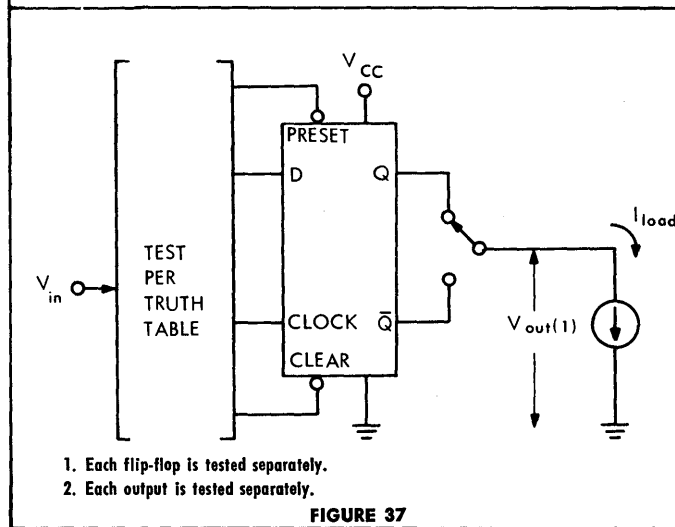
d-c test circuits § (continued)



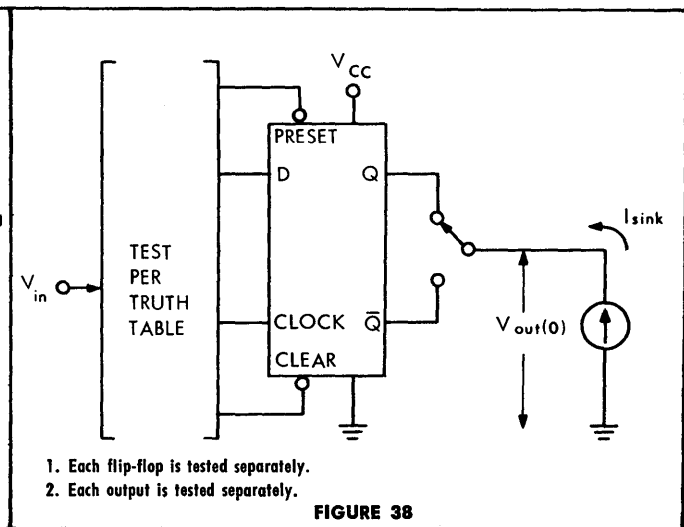
**FIGURE 35**



**FIGURE 36**



**FIGURE 37**



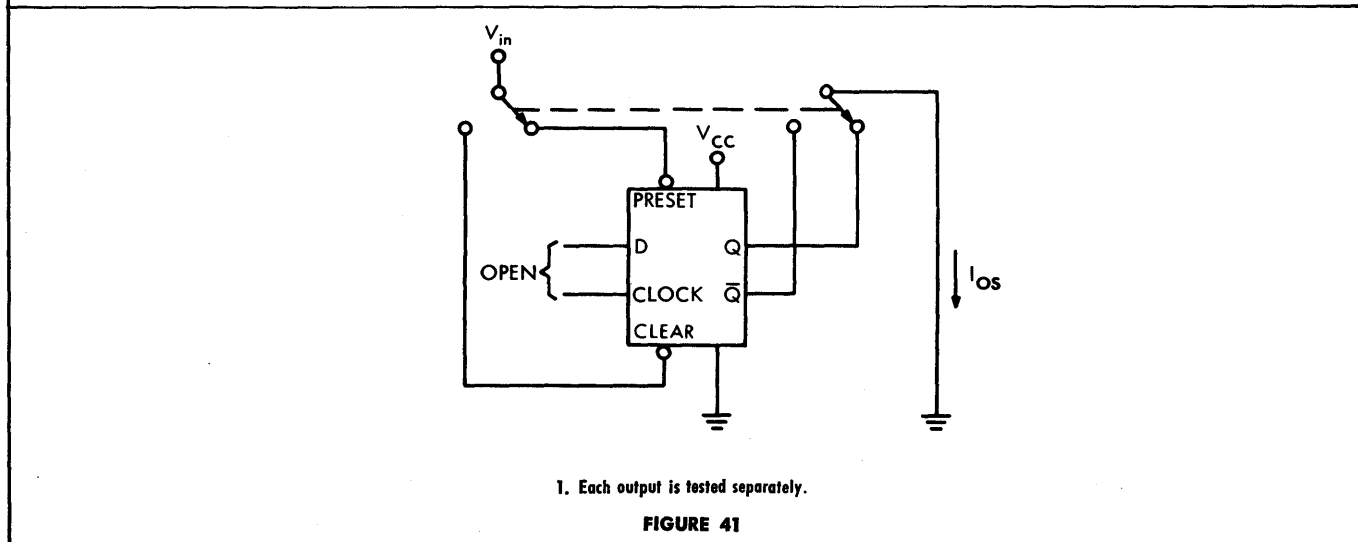
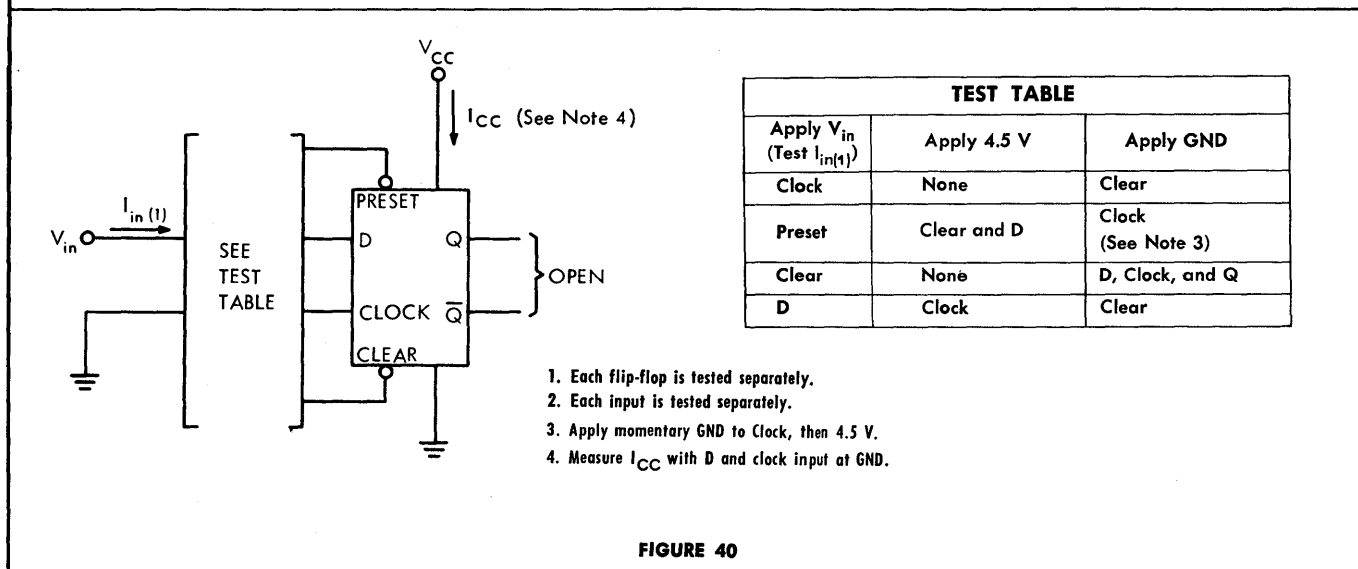
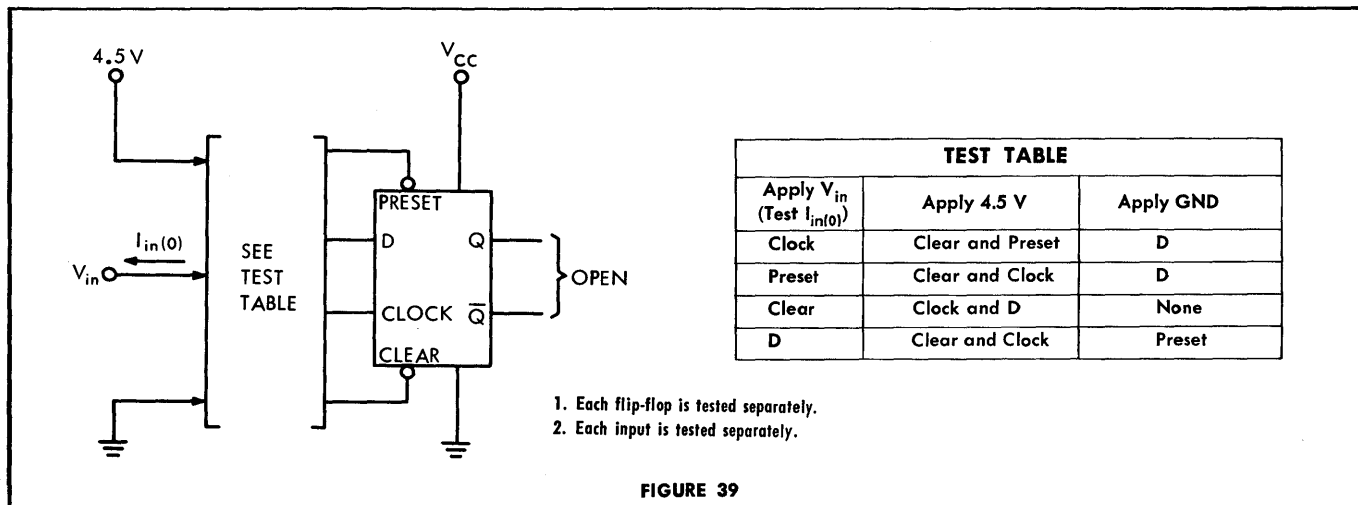
**FIGURE 38**

§Arrows indicate actual direction of current flow.



PARAMETER MEASUREMENT INFORMATION

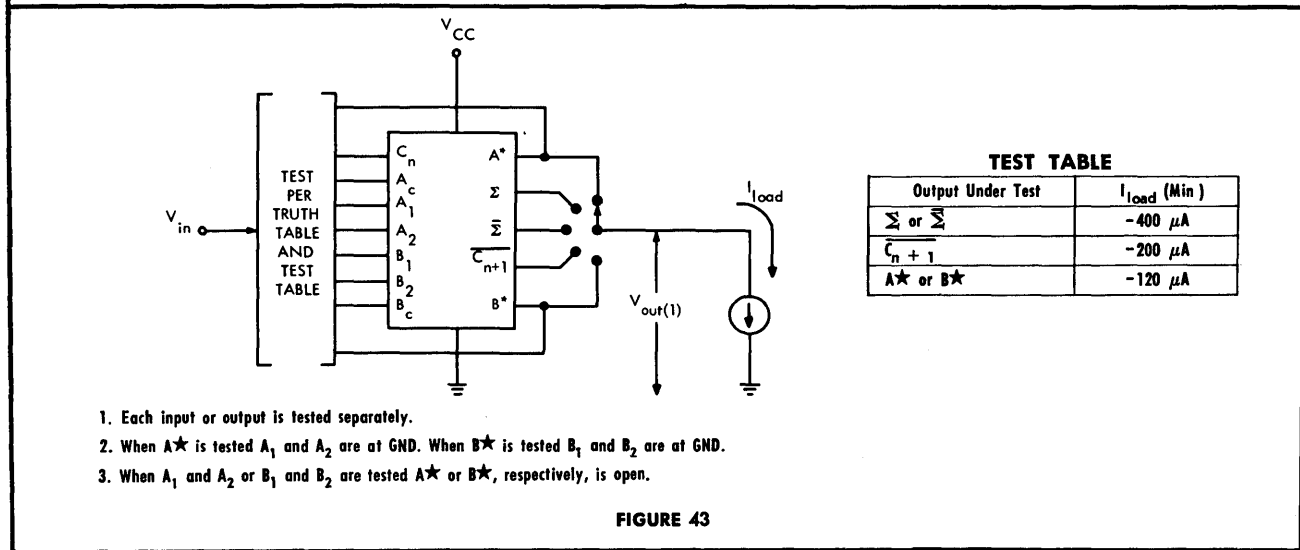
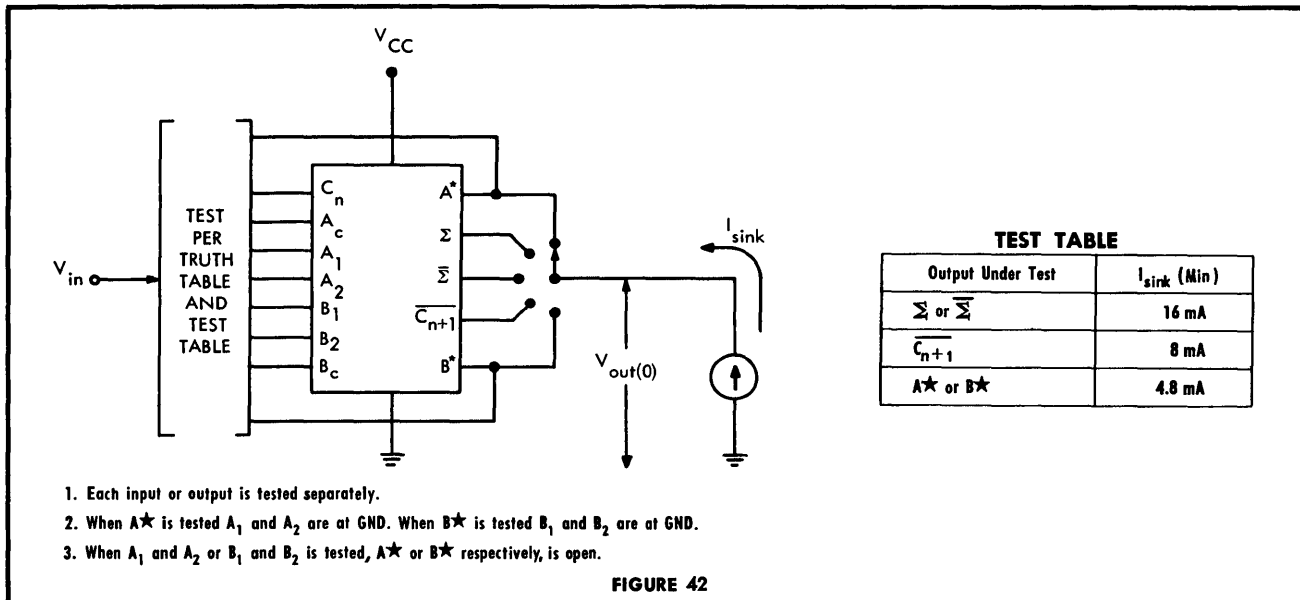
d-c test circuits § (continued)



§Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

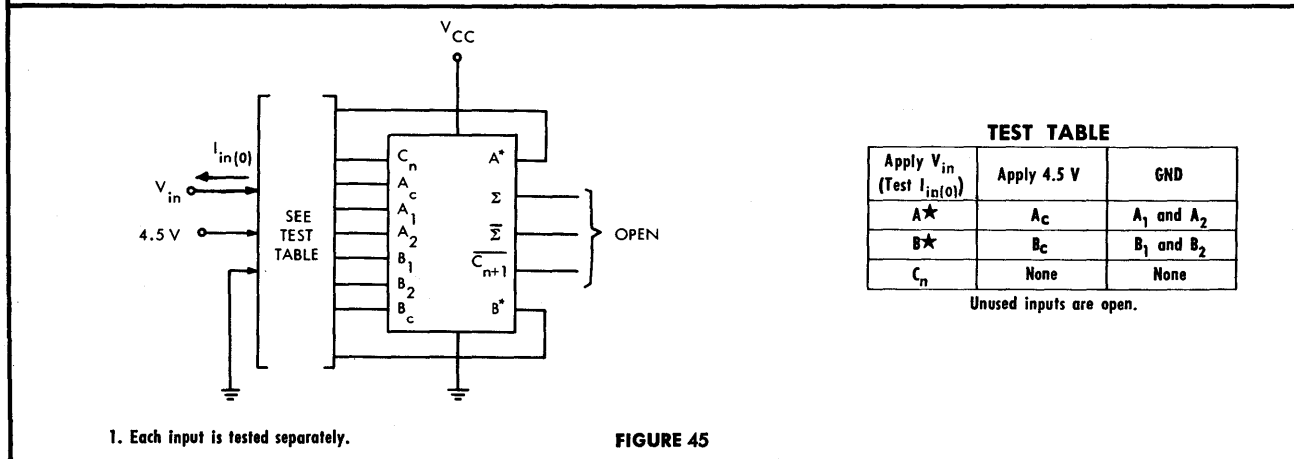
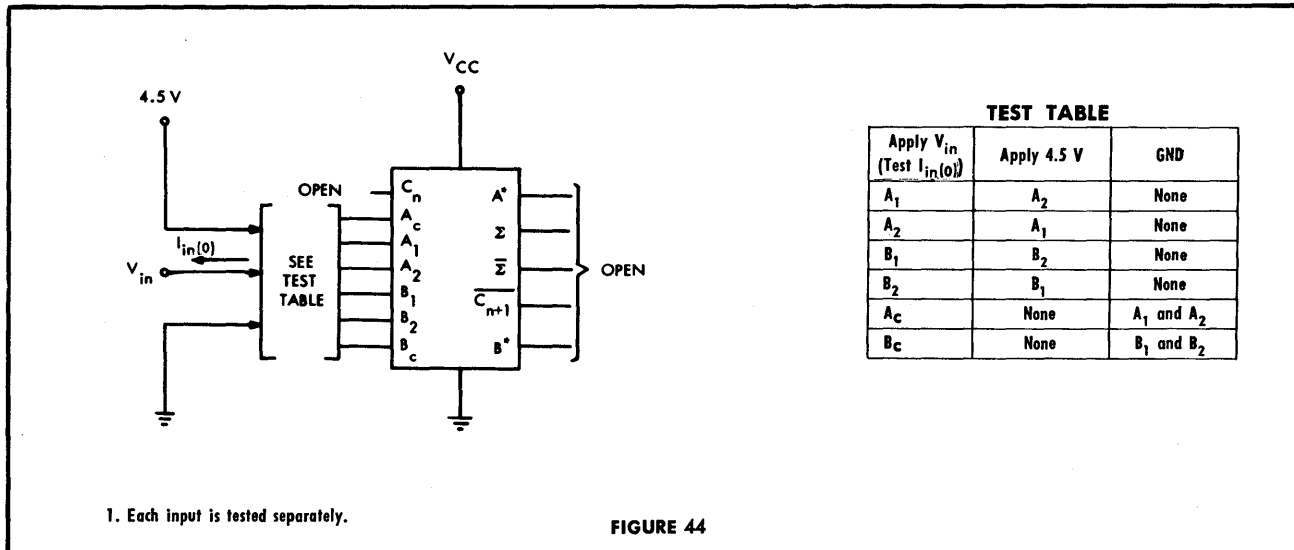
**d-c test circuits § (continued)**



§Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

d-c test circuits (continued)



§ Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

**d-c test circuits§(continued)**

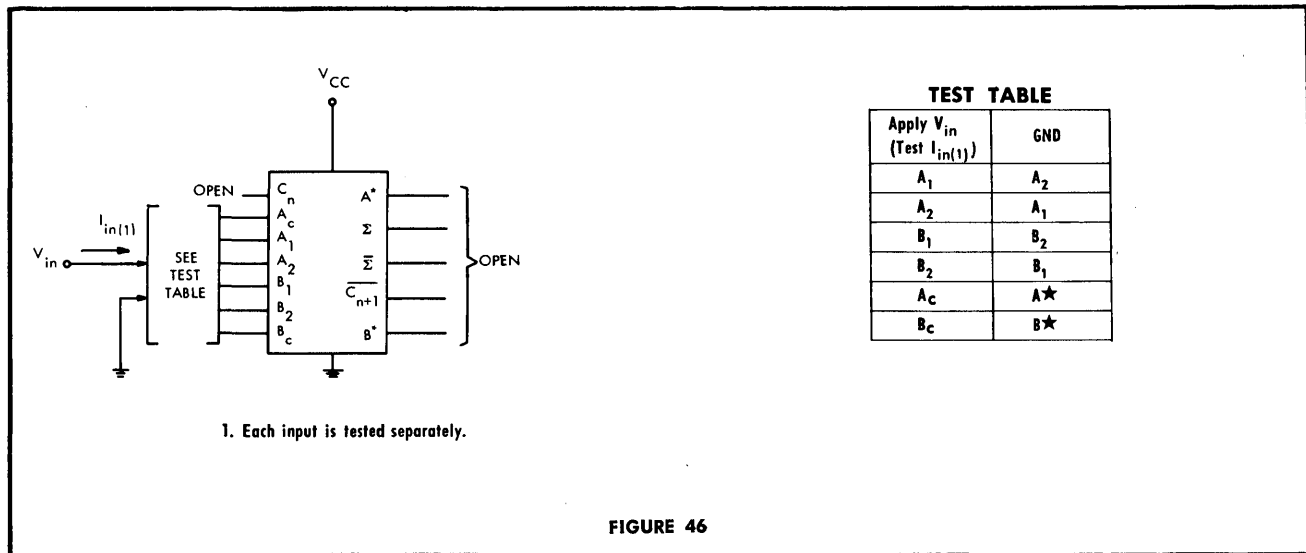


FIGURE 46

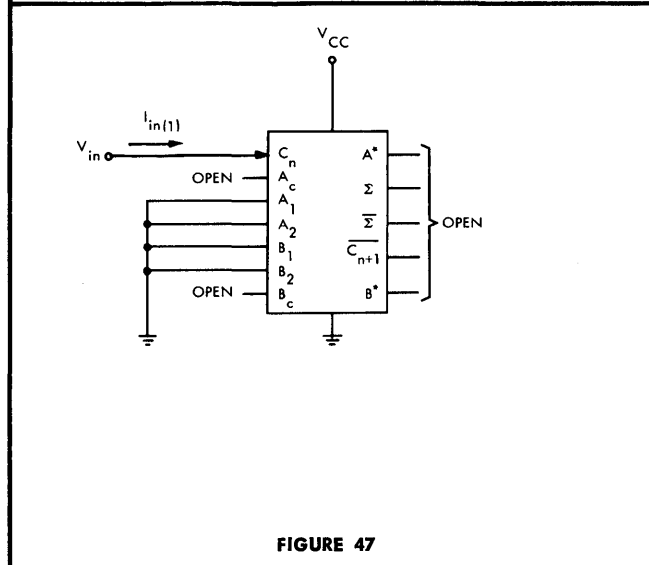


FIGURE 47

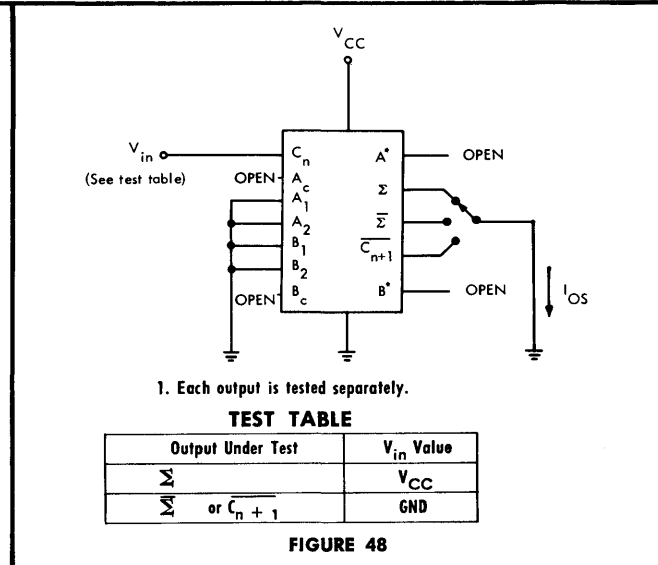


FIGURE 48

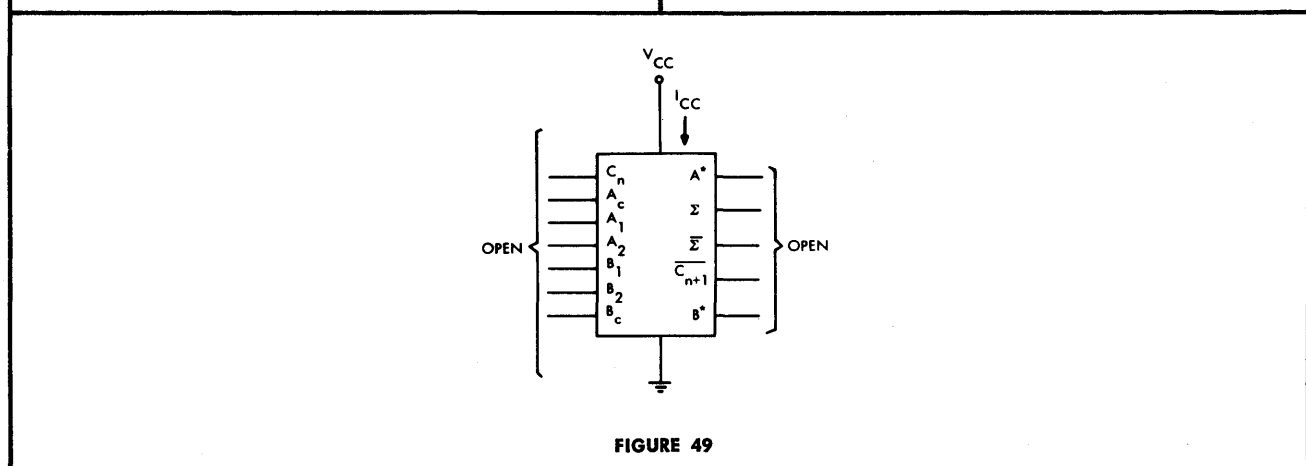
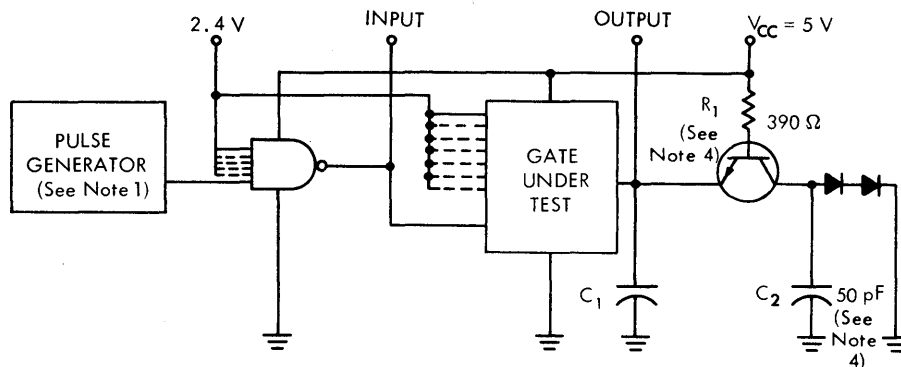


FIGURE 49

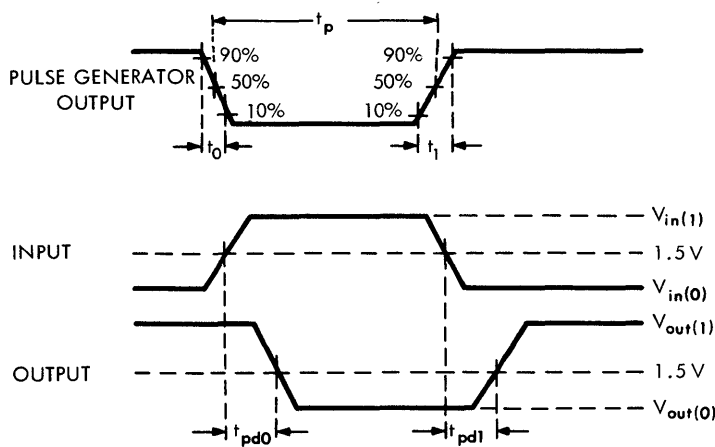
§ Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

switching characteristics



**TEST CIRCUIT**



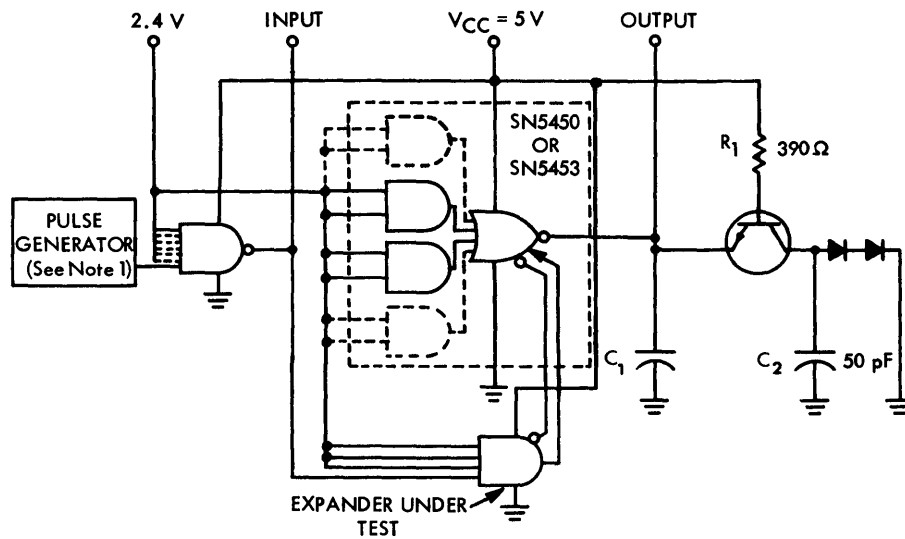
**VOLTAGE WAVEFORMS**

- NOTES: 1. The generator has the following characteristics:  $t_0 = t_1 \leq 15 \text{ ns}$ ,  $t_p = 0.5 \mu\text{s}$ ,  $\text{PRR} = 1 \text{ MHz}$ ,  $Z_{\text{out}} \approx 50 \Omega$ .  
 2. All transistors are 2N2368.  
 3. All diodes are 1N916.  
 4. Test SN5440 with  $R_1 = 130 \Omega$ ,  $C_2 = 150 \text{ pF}$ .  
 5.  $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$   
 6.  $C_1$  includes probe and jig capacitance.

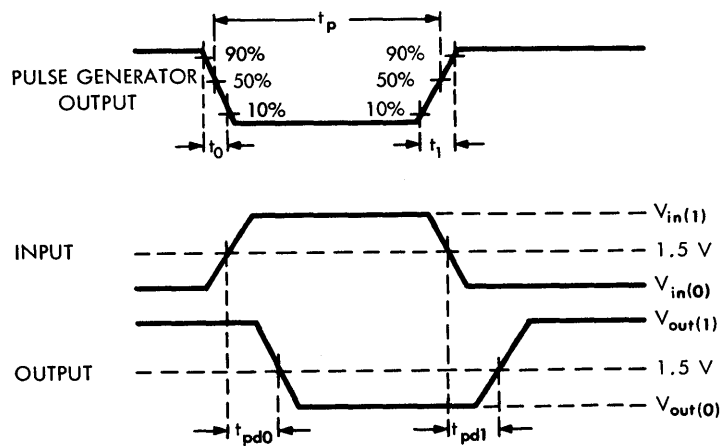
**FIGURE 50 — GATE PROPAGATION DELAY TIMES**

**PARAMETER MEASUREMENT INFORMATION**

**switching characteristics (continued)**



**TEST CIRCUIT**



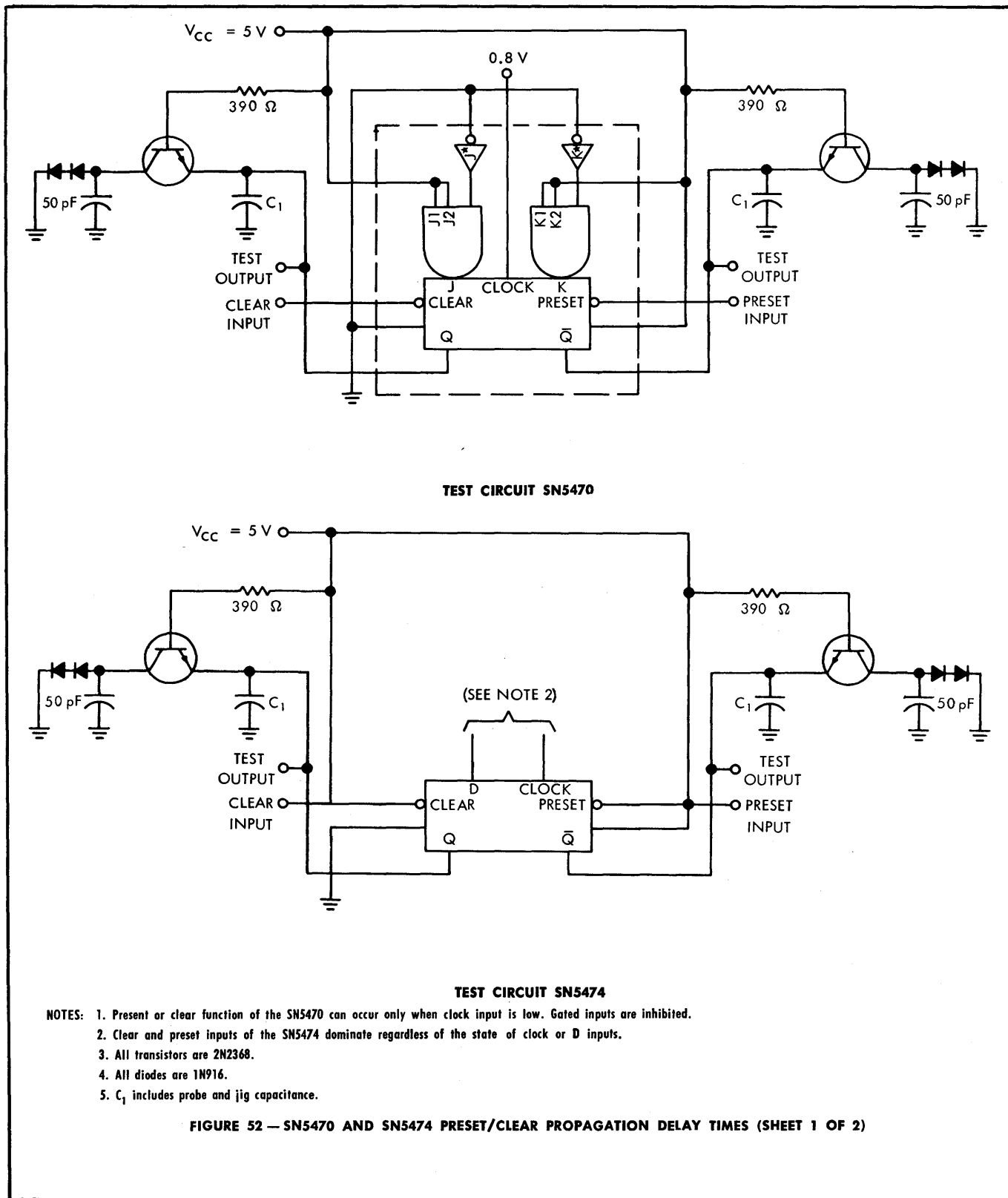
**VOLTAGE WAVEFORMS**

- NOTES:**
1. The generator has the following characteristics:  $t_0 = t_1 \leq 15 \text{ ns}$ ,  $t_p = 0.5 \mu\text{s}$ ,  $\text{PRR} = 1 \text{ MHz}$ ,  $Z_{\text{out}} \approx 50 \Omega$ .
  2. All transistors are 2N2368.
  3. All diodes are 1N916.
  4.  $t_{\text{pd}} = \frac{t_{\text{pd0}} + t_{\text{pd1}}}{2}$
  5.  $C_1$  includes probe and jig capacitance.

**FIGURE 51 — EXPANDER PROPAGATION DELAY TIMES**

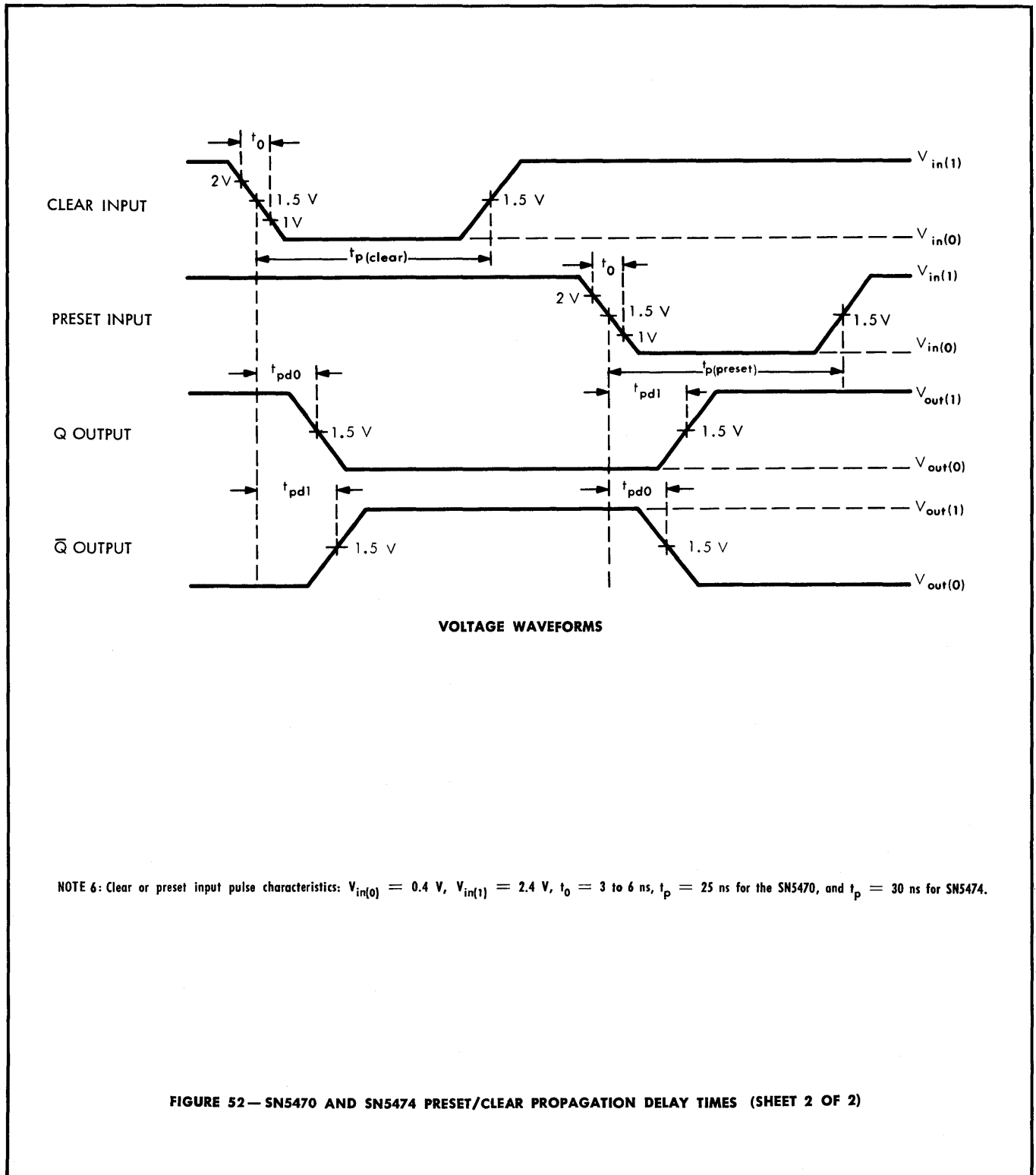
**PARAMETER MEASUREMENT INFORMATION**

switching characteristics (continued)



**PARAMETER MEASUREMENT INFORMATION**

switching characteristics (continued)

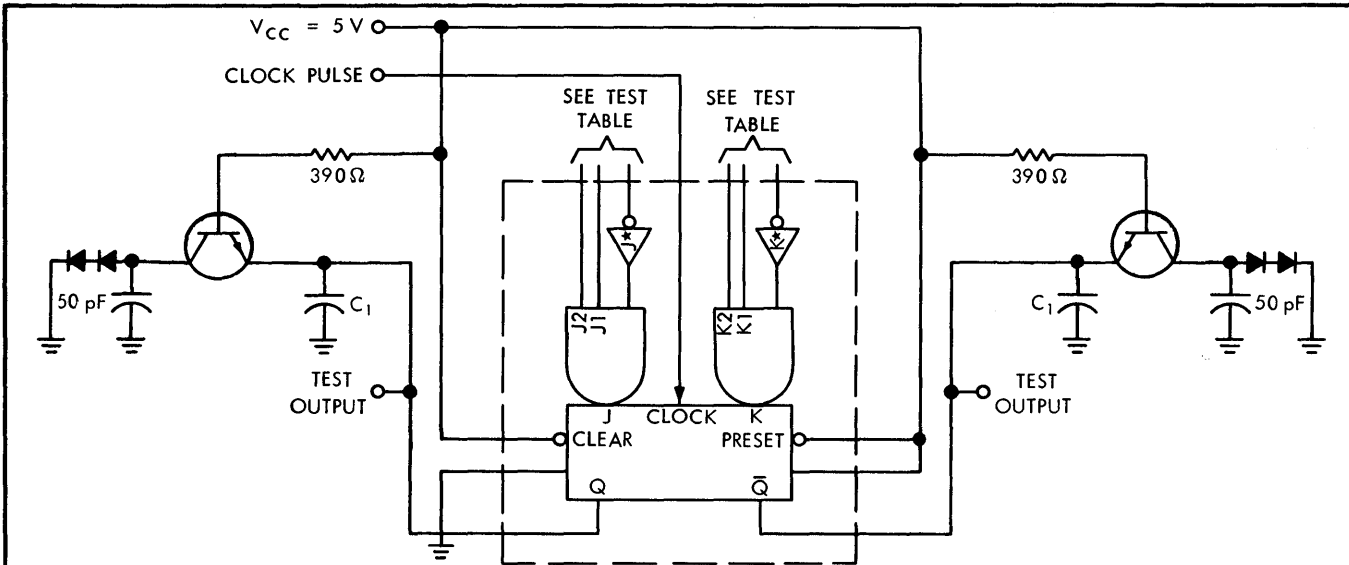


**FIGURE 52—SN5470 AND SN5474 PRESET/CLEAR PROPAGATION DELAY TIMES (SHEET 2 OF 2)**



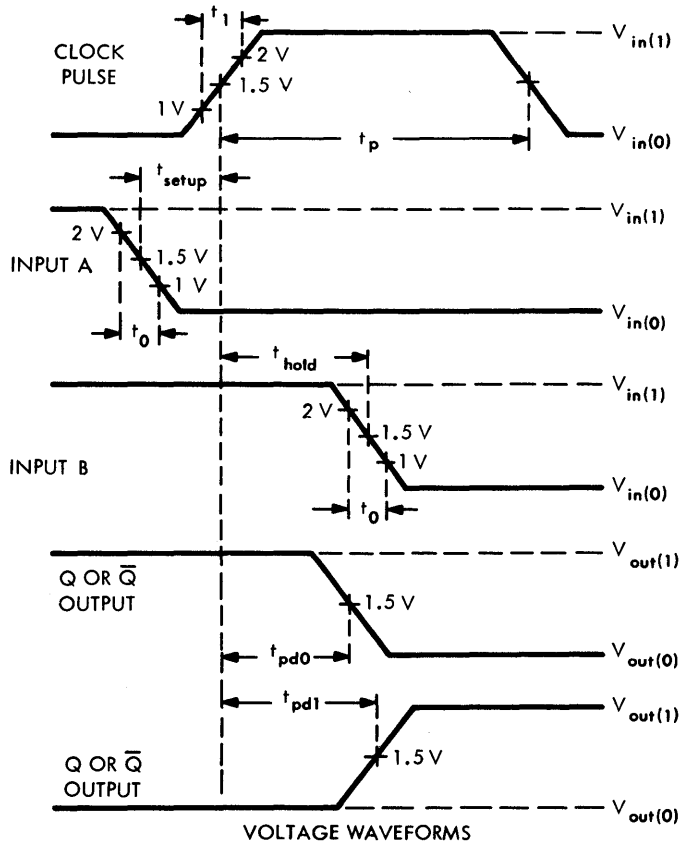
**PARAMETER MEASUREMENT INFORMATION**

**switching characteristics (continued)**



TEST TABLE					
TEST NO.	TEST	INPUT A	INPUT B	APPLY + 2.4 V	GND
1	$t_{\text{setup}}$ at J★	J★	None	J1, J2, K1, K2	K★
2	$t_{\text{hold}}$ at J1, J2	None	J1, J2	K1, K2	J★ and K★
3	$t_{\text{setup}}$ at K★	K★	None	J1, J2, K1, K2	J★
4	$t_{\text{hold}}$ at K1, K2	None	K1, K2	J1, J2	J★ and K★

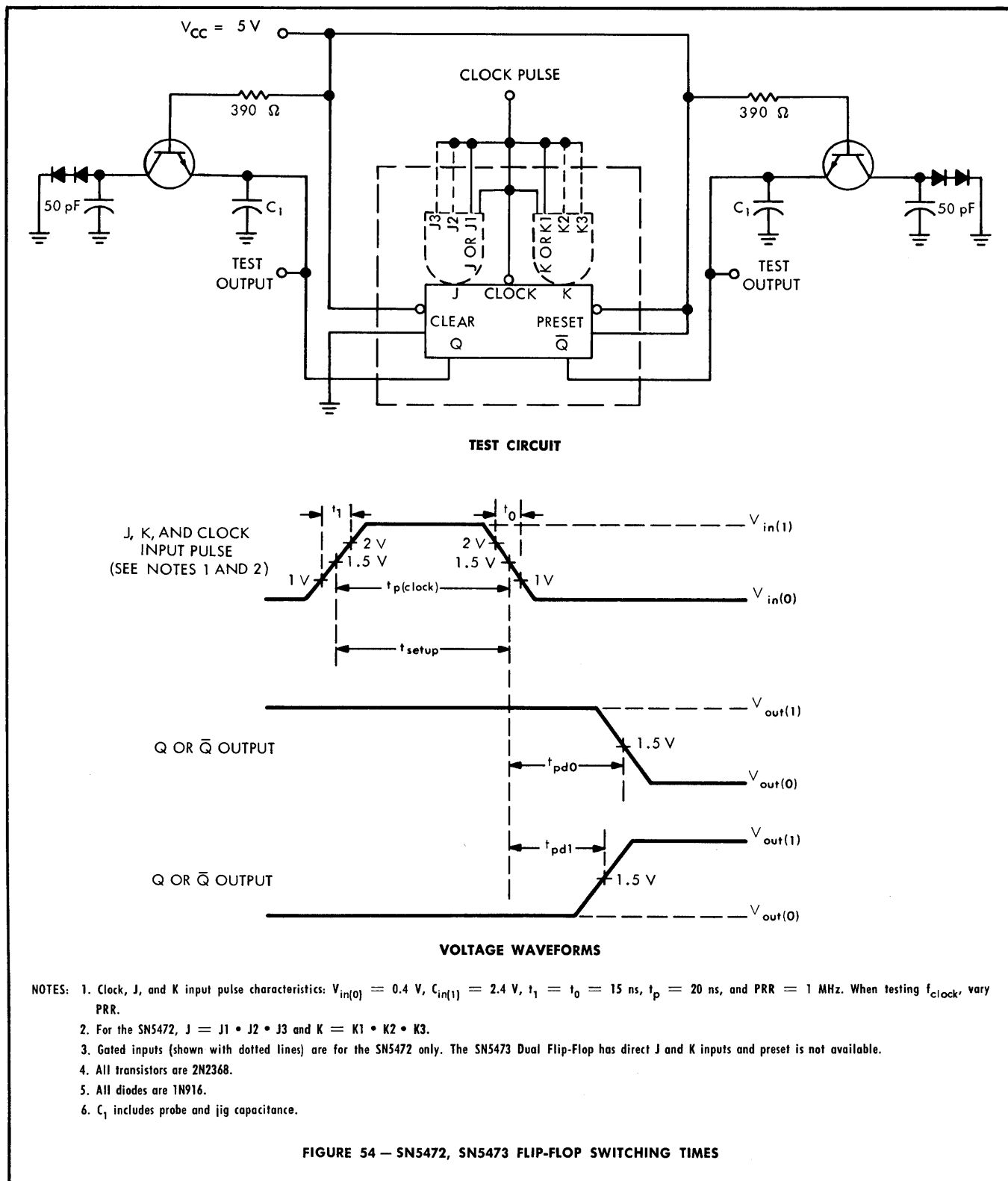
- NOTES: 1. Clock pulse (see note 3), input A, and input B are used to measure  $t_{\text{setup}}$  and  $t_{\text{hold}}$ .
2. Clock frequency,  $t_{\text{pd1}}$ , and  $t_{\text{pd0}}$  (from clock to output) are measured in the toggle mode. Hold J = K = logical 1 per truth table and apply clock pulse (see note 3).
3. Clock pulse characteristics:  $V_{\text{in}(0)} = 0.4 \text{ V}$ ,  $V_{\text{in}(1)} = 2.4 \text{ V}$ ,  $t_1 = 15 \text{ ns}$ ,  $t_p = 20 \text{ ns}$ , and  $\text{PRR} = 1 \text{ MHz}$ . When testing  $f_{\text{clock}}$ , vary PRR.
4. Input pulse characteristics:  $V_{\text{in}(0)} = 0.4 \text{ V}$ ,  $V_{\text{in}(1)} = 2.4 \text{ V}$ ,  $t_0 = 3 \text{ to } 6 \text{ ns}$ .
5. All transistors are 2N2368.
6. All diodes are 1N916.
7.  $C_1$  includes probe and jig capacitance.



**FIGURE 53 — SN5470 FLIP-FLOP SWITCHING TIMES**

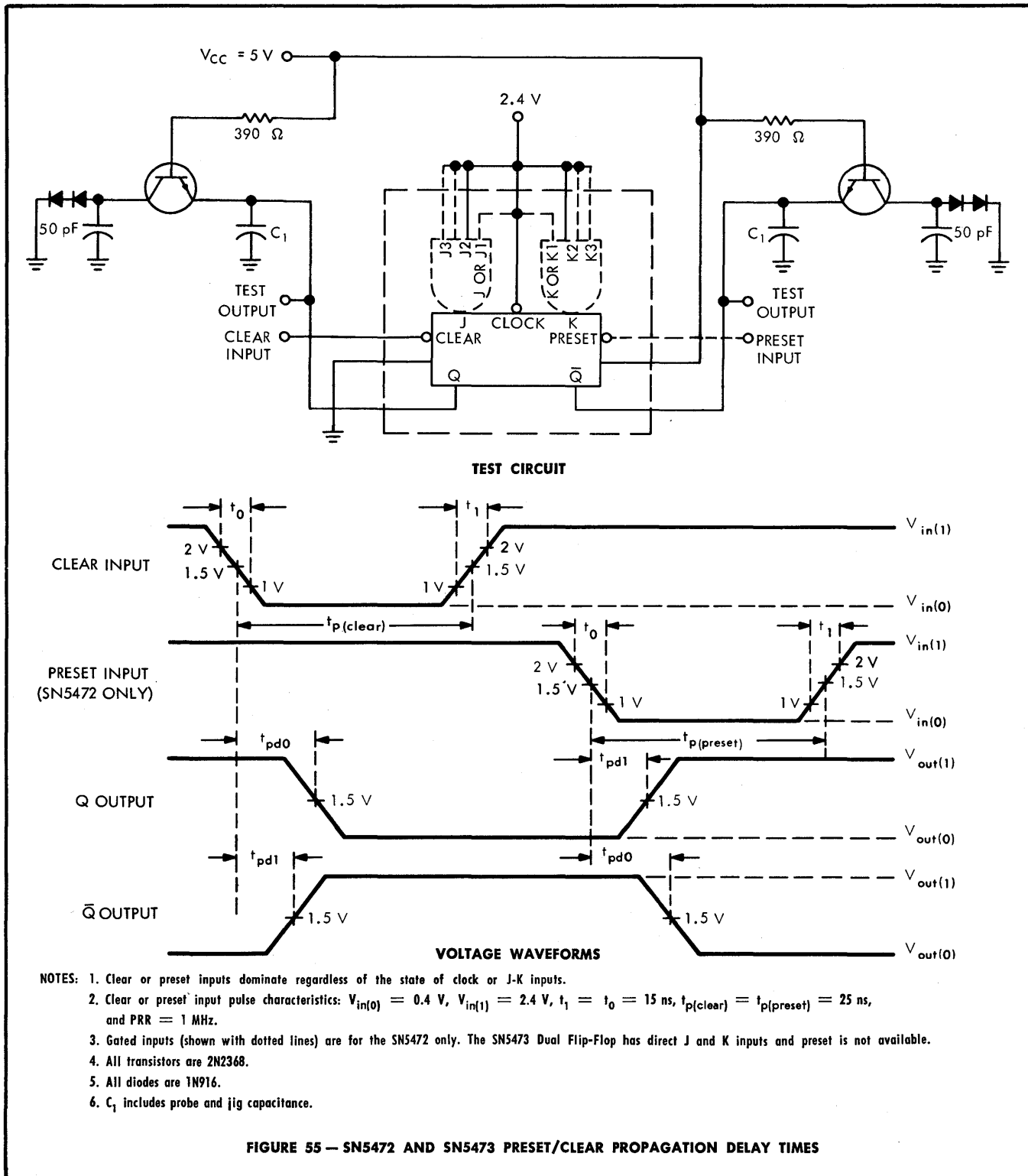
**PARAMETER MEASUREMENT INFORMATION**

**switching characteristics (continued)**



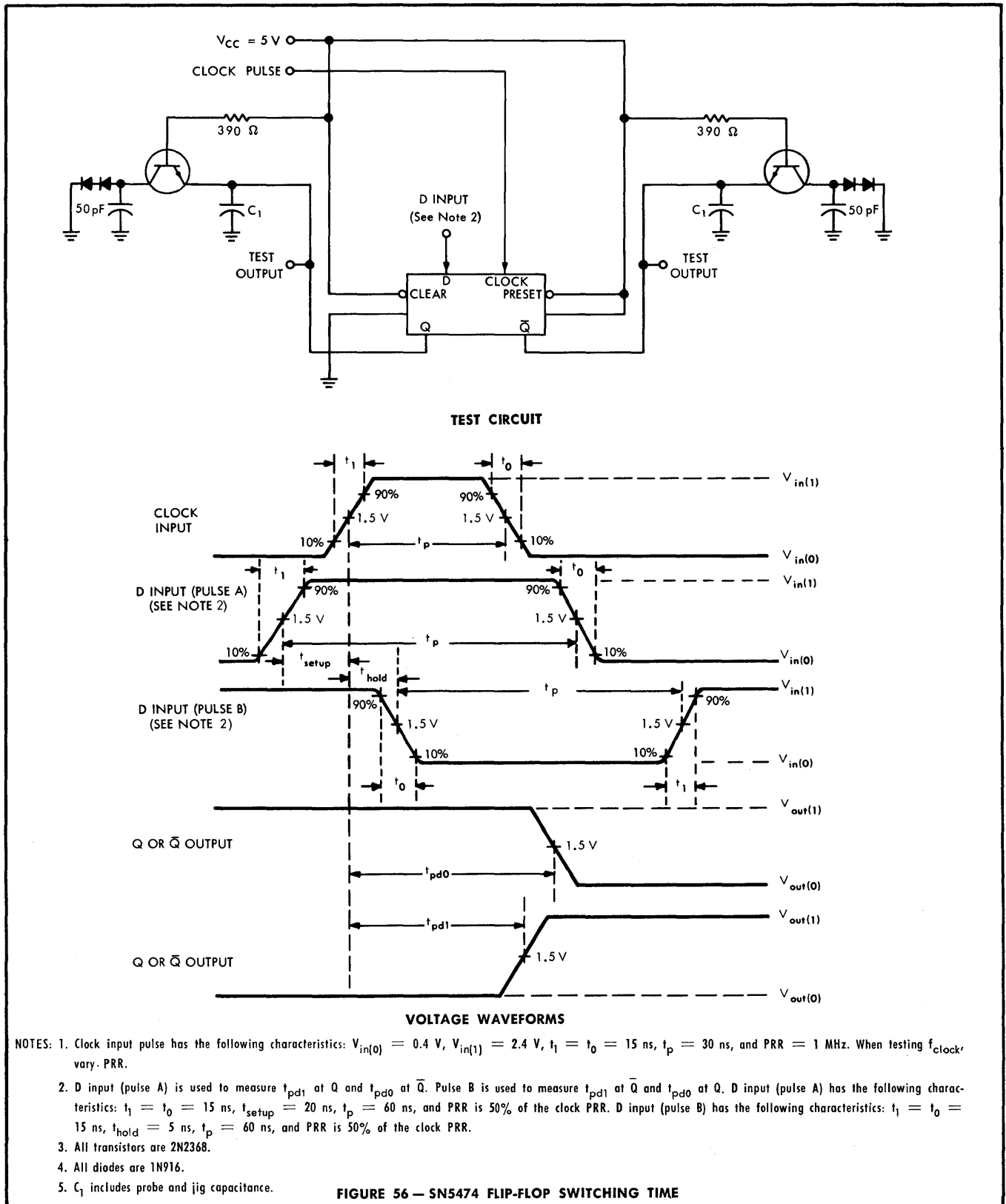
**PARAMETER MEASUREMENT INFORMATION**

**switching characteristics (continued)**



**PARAMETER MEASUREMENT INFORMATION**

**switching characteristics (continued)**



**PARAMETER MEASUREMENT INFORMATION**

**switching characteristics (continued)**

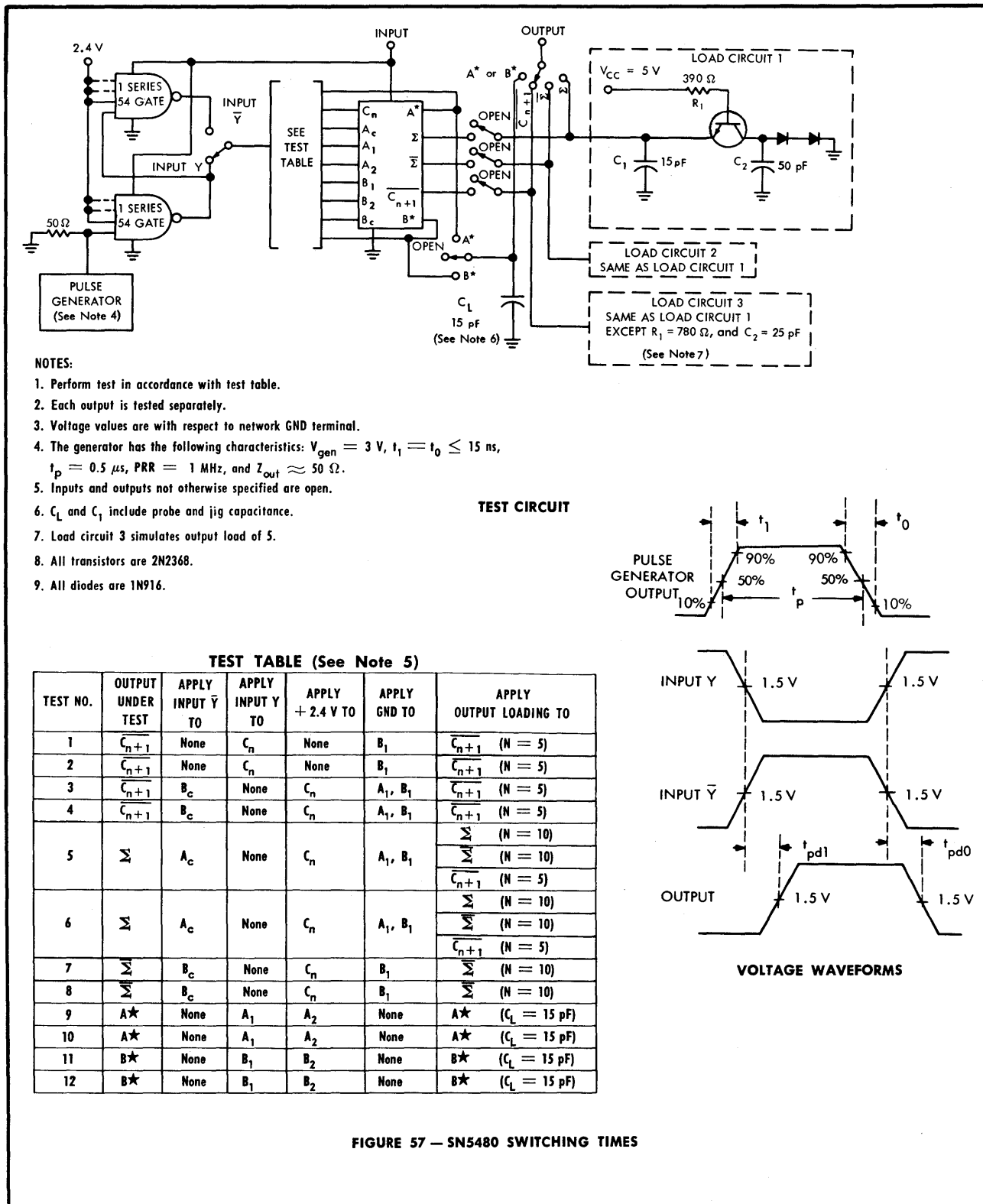


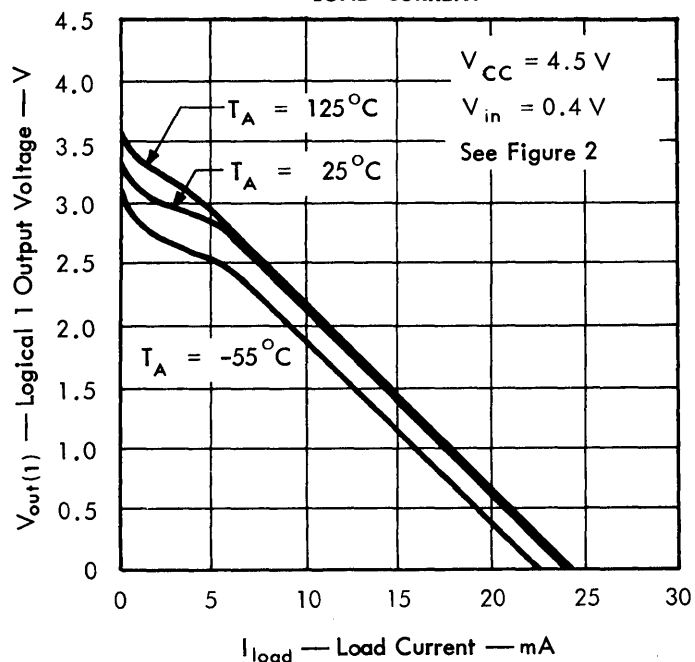
FIGURE 57 — SN5480 SWITCHING TIMES

**TYPICAL CHARACTERISTICS §**

LOGICAL 1 OUTPUT VOLTAGE

vs

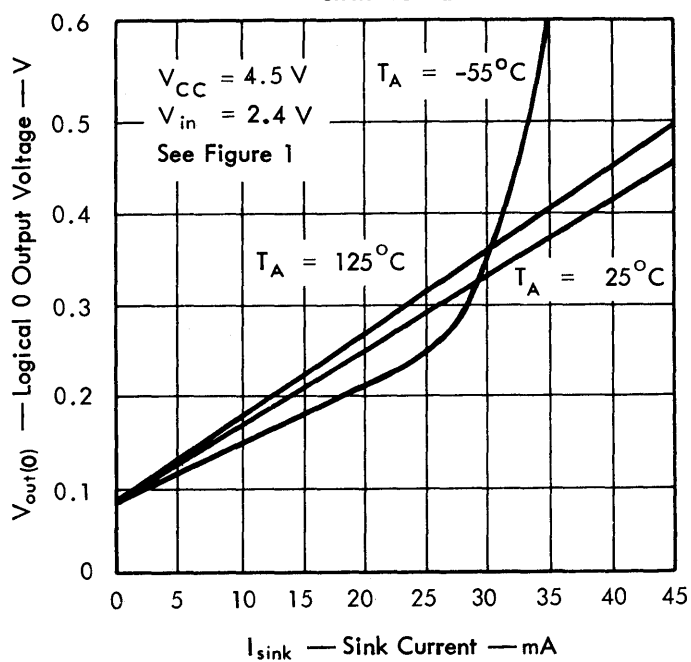
LOAD CURRENT



LOGICAL 0 OUTPUT VOLTAGE

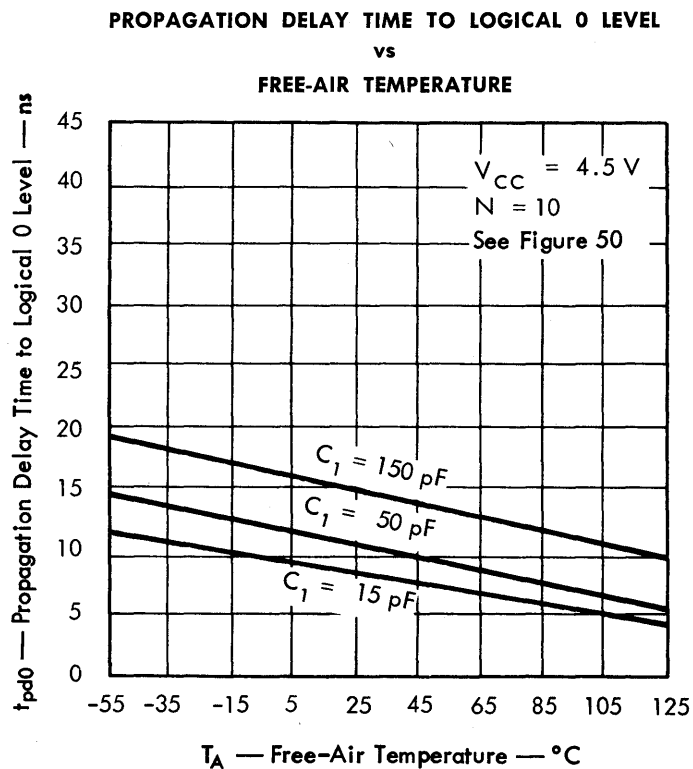
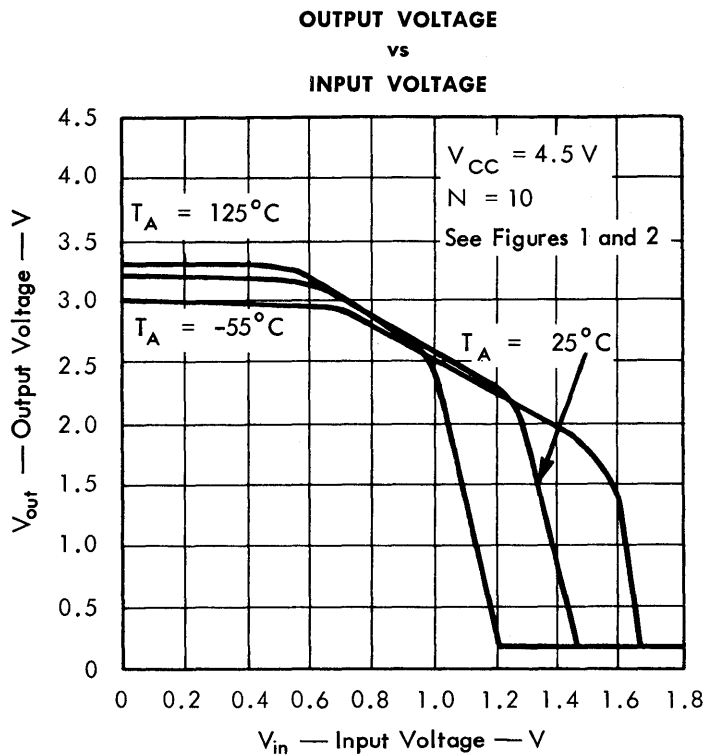
vs

SINK CURRENT



§ Unless otherwise noted, data as shown is applicable for SN5400, SN5410, SN5420, SN5430, SN5450, SN5451, SN5453, and SN5454.

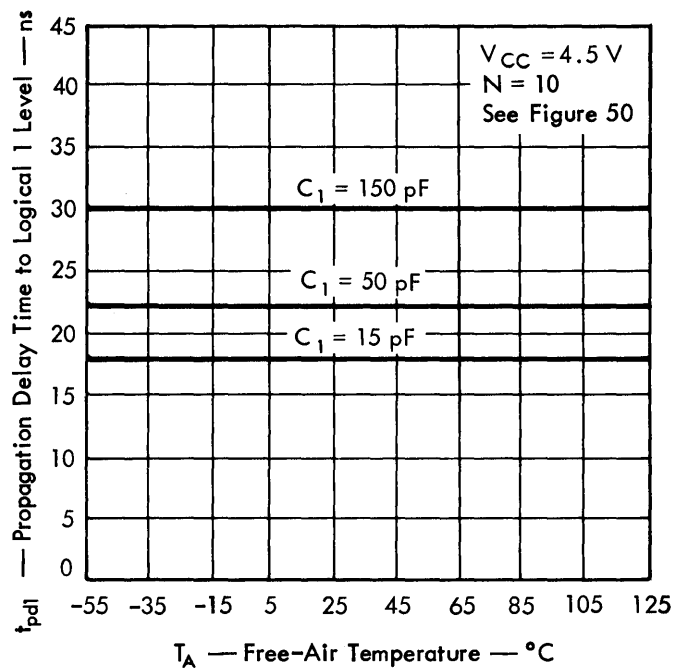
**TYPICAL CHARACTERISTICS §**



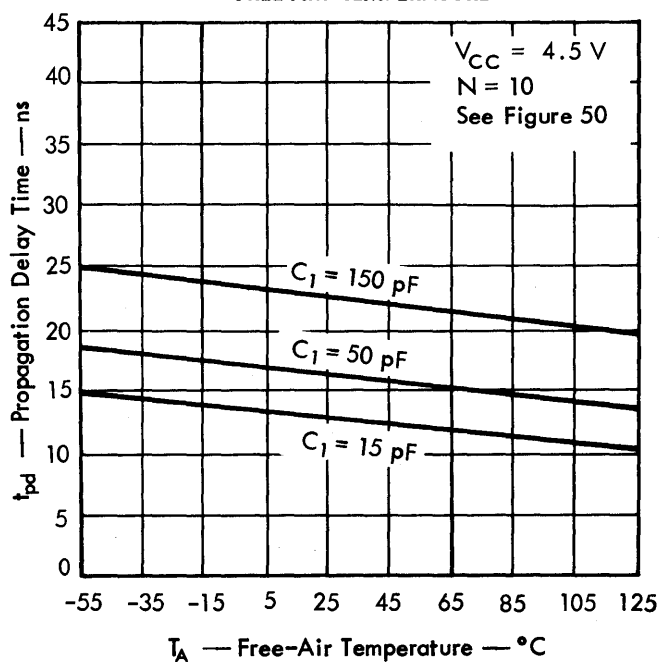
§ Unless otherwise noted, data as shown is applicable for SN5400, SN5410, SN5420, SN5430, SN5450, SN5451, SN5453, and SN5454.

**TYPICAL CHARACTERISTICS §**

**PROPAGATION DELAY TIME TO LOGICAL 1 LEVEL  
vs  
FREE-AIR TEMPERATURE**



**PROPAGATION DELAY TIME  
vs  
FREE-AIR TEMPERATURE**



§ Unless otherwise noted, data as shown is applicable for SN5400, SN5410, SN5420, SN5430, SN5450, SN5451, SN5453, and SN5454.



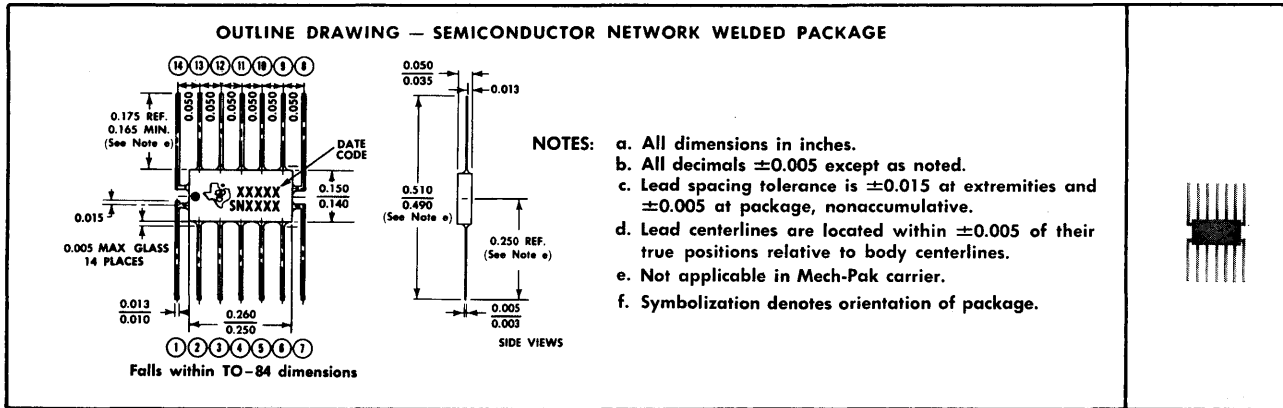
# SERIES 54 SOLID CIRCUIT<sup>®</sup> SEMICONDUCTOR NETWORKS<sup>†</sup>

## MECHANICAL DATA

### general

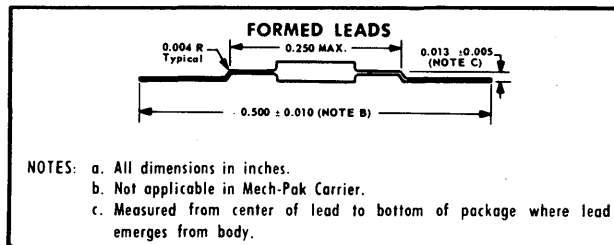
Series 54 semiconductor networks are mounted in glass-to-metal hermetically sealed, welded packages. Package body and leads are gold-plated F-15<sup>‡</sup> glass-sealing alloy. Approximate weight is

0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. All Series 54 networks are available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier.



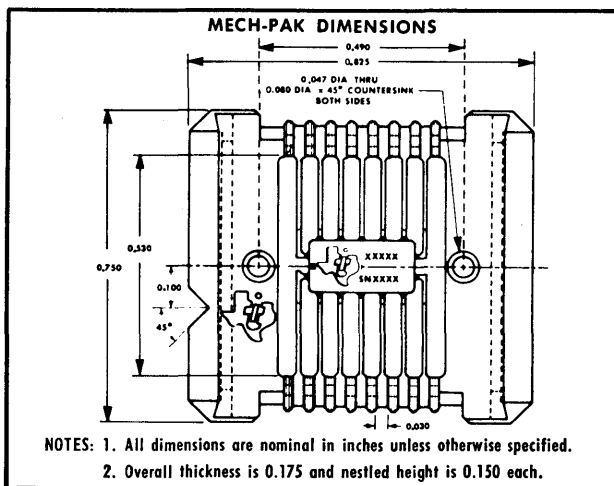
### leads

Gold-plated F-15<sup>‡</sup> leads require no additional cleaning or processing when used in soldered or welded assembly. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Standard lead length is 0.175 inch. Networks can be removed from Mech-Pak carriers with lead lengths up to 0.175 inch.



### insulator

An insulator, secured to the back surface of the package, permits mounting networks on circuit boards which have conductors passing beneath the package. The insulator is 0.0025 inch thick and has an insulation resistance of greater than 10 megohms at 25°C.



### mech-pak carrier

The Mech-Pak carrier facilitates handling the network, and is compatible with automatic equipment used for testing and assembly. The carrier is particularly appropriate for mechanized assembly operations and will withstand temperatures of 125°C for indefinite periods.

### ordering instructions

Variations in mechanical configuration of semiconductor networks are identified by suffix numbers shown in a table at the right.

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5

<sup>†</sup>Patented by Texas Instruments

<sup>‡</sup>F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

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TI cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

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## How to Insert Pages

1. Place pile of insert pages at right of book.
2. Grasp plastic tabs and pull all three straps out of book.
3. Work from back of book to front, placing insert sheets in numerical order by page number\*, aligning their holes with holes in book.
4. After *all* insert sheets are in place, with left hand slip long ends of *all three straps* into right-hand holes.
5. With right hand, slip short ends of straps into left-hand holes. The book is now re-bound.

*To delete pages*, tear them out one at a time as you would tear sheets from a tablet.

**\*Certain large blocks of page numbers have intentionally been omitted** from the bound book. These numbers are reserved for insert pages.

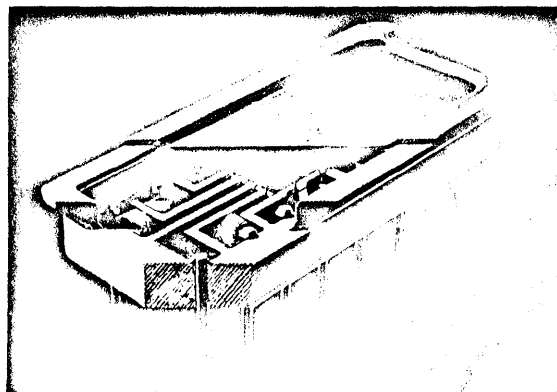
DIGITAL SEMICONDUCTOR NETWORKS  
IN A PLUG-IN FLAT PACKAGE

Description

Series 74P consists of Series 74 general-purpose digital circuits mounted in 16-pin hermetically sealed plug-in flat packages.

Package features

- plug-in pin configuration ideal for economical flow-soldering techniques
- pins on 100-mil grid spacings for industrial-type circuit-boards
- economical package construction
- sturdy pins for easy insertion
- welded hermetic seal
- low profile for space savings

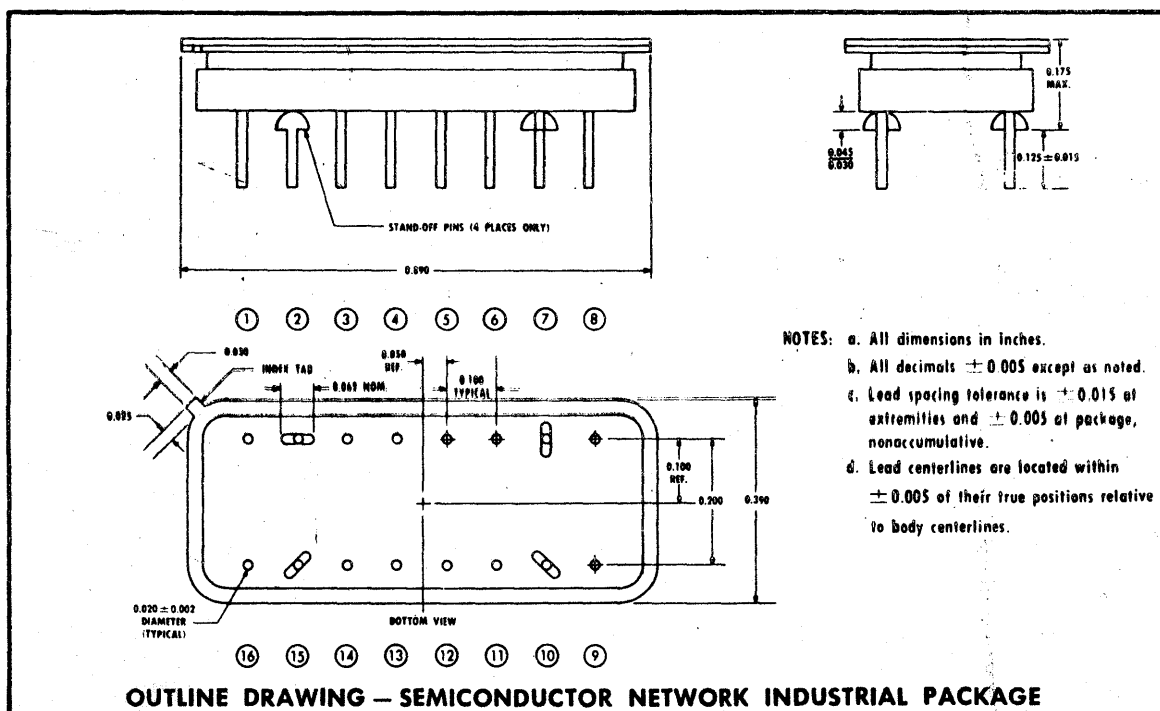


INDUSTRIAL 16-PIN PLUG-IN FLAT PACKAGE

This inexpensive plug-in package is adaptable to conventional low-cost assembly and design techniques, including high-volume manual or automatic insertion, flow- or wave-soldering, and the use of economical circuit boards designed with 100-mil grid spacings. The package has two rows of firm pins out the bottom with the rows spaced 200 mils apart. A flange tab is provided for indexing, simplifying both manual and automatic insertion. The package has a rugged ceramic-fo-metal construction and a welded-metal hermetic seal, assuring the highest degree of network rigidity and reliability.

Mechanical data

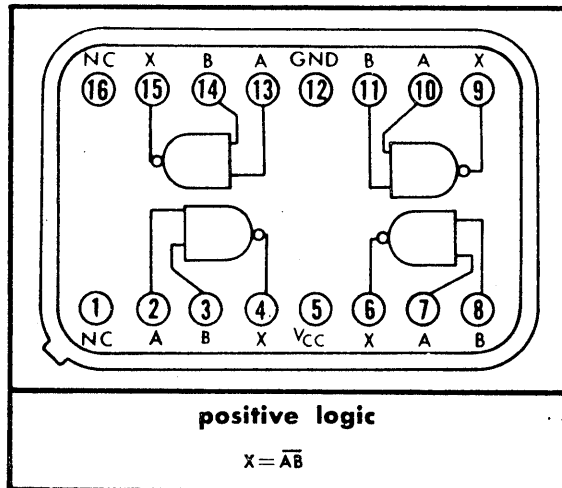
Series 74P networks are mounted in a ceramic-fo-metal, hermetically sealed, plug-in package. The circuit and leads are insulated from the package. Leads require no additional cleaning or processing prior to soldering.



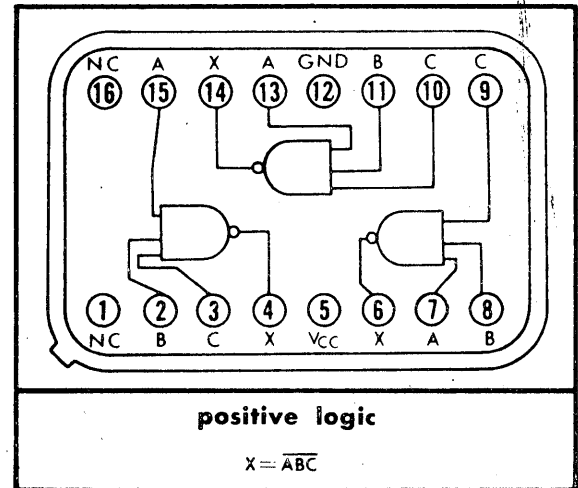
Specifications, logic symbols, and pin numbers

Schematic diagrams, fan-out rules and specifications for all Series 74P networks are identical to those of the corresponding Series 74 network. Logic symbols for all Series 74P networks are shown here to provide external circuit pin connections. The absence of internal connections to a package is indicated by NC.

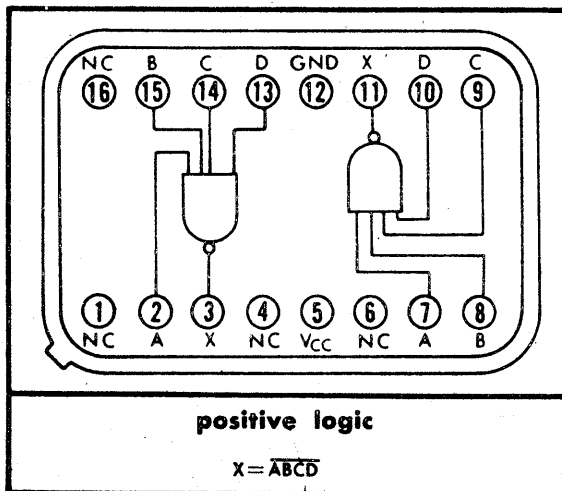
**TYPE SN7400P**  
**QUADRUPLE 2-INPUT POSITIVE NAND GATE**



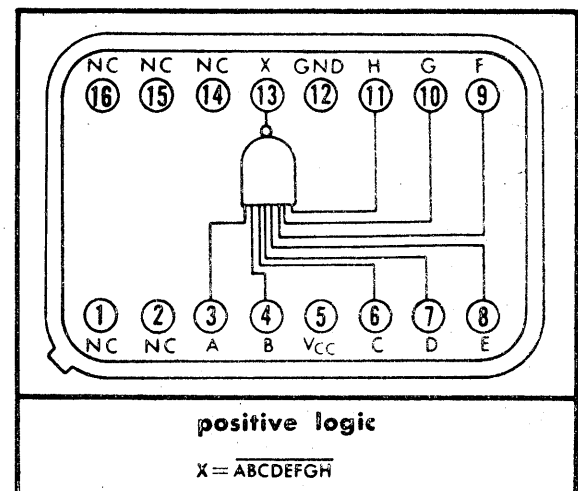
**TYPE SN7410P**  
**TRIPLE 3-INPUT POSITIVE NAND GATE**



**TYPE SN7420P**  
**DUAL 4-INPUT POSITIVE NAND GATE**



**TYPE SN7430P**  
**8-INPUT POSITIVE NAND GATE**



Manufacturer.

Texas Instruments, Inc., Semiconductor Components Division, P.O. Box 5012,  
 Dallas, Texas.

TEXAS INSTRUMENTS

SERIES 74P SEMICONDUCTOR NETWORKS (Contd)

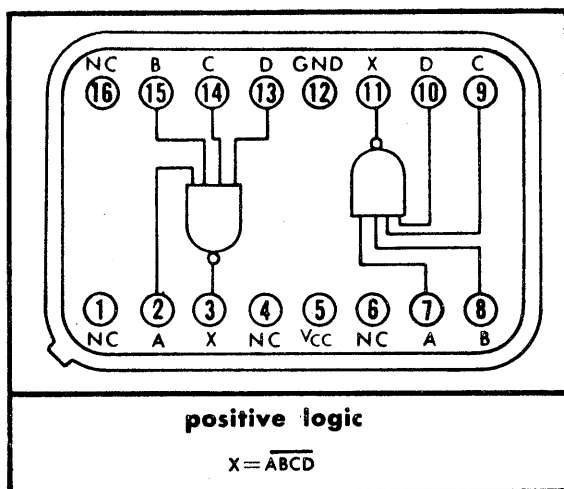
logic definition

Series 74P logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE=LOGICAL 0

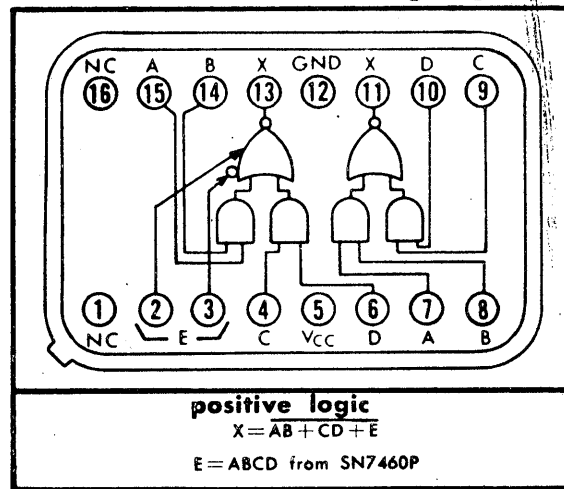
HIGH VOLTAGE=LOGICAL 1

**TYPE SN7440P**  
**DUAL 4-INPUT POSITIVE NAND "POWER" GATE**



**TYPE SN7450P**  
**EXPANDABLE DUAL EXCLUSIVE-OR GATE**

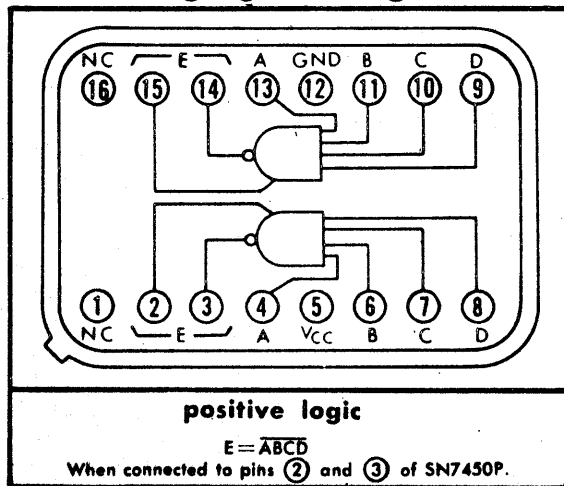
Both expander inputs are used simultaneously for expanding with the SN7460P. If expander is not used leave pins ② and ③ open



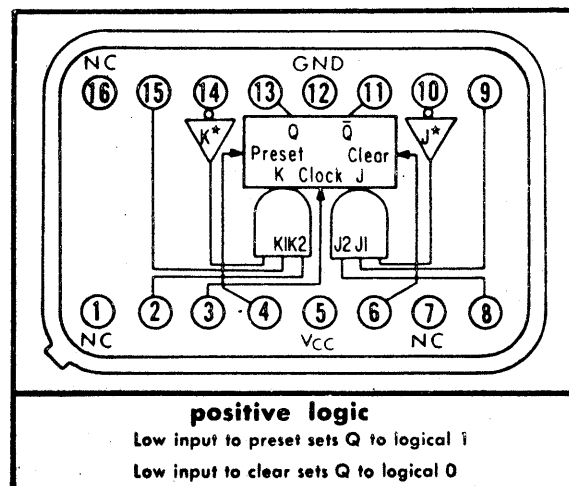
**TYPE SN7460P**  
**DUAL 4-INPUT EXPANDER FOR SN7450P**

Connect pin ③ or ⑭ (collector) to pin ③ of SN7450P.

Connect pin ② or ⑮ (emitter) to pin ② of SN7450P.



**TYPE SN7470P**  
**J-K FLIP-FLOP**





**HIGH-SPEED TTL DIGITAL SEMICONDUCTOR NETWORKS  
IN  
DTL PIN CONFIGURATIONS**

**description**

Series 54 930 consists of Texas Instruments high-speed TTL circuits with pin configurations and logic functions that make them electrically compatible and mechanically interchangeable with Series 15 930 DTL circuits. In addition to five interchangeable networks, an 8-input NAND gate and a dual AND-OR-INVERT gate are available.

**comparative features**

	SERIES 15 930 DTL	SERIES 54 930 TTL
Gate propagation delay time (typically)	25 ns	13 ns
Fan-out capability (DTL can drive 8 DTL or 5 TTL loads, TTL can drive 10 TTL or 10 DTL loads)	8	10
Noise immunity (guaranteed)	350 mV	400 mV

**standard line summary**

FUNCTION	TYPES	SIMILAR DTL CIRCUIT
Dual 4-Input Positive NAND Gate	SN54 930	SN15 930
Dual 4-Input Positive NAND Buffer	SN54 932	SN15 932
Quadruple 2-Input Positive NAND Gate	SN54 946	SN15 946
Triple 3-Input Positive NAND Gate	SN54 962	SN15 962
8-Input Positive NAND Gate	SN54 965	None
Dual 2-Wide 2-Input AND-OR-INVERT Gate	SN54 966	None
Master-Slave Flip-Flop	SN54 948	SN15 931/SN15 945/SN15 948

**specifications**

Schematic diagrams, fan-out rules, maximum ratings, temperature ranges, and electrical characteristics are identical to those of the corresponding Series 54 type number.

SERIES 54 930 TYPE	CORRESPONDING SERIES 54 TYPE
SN54 930	SN5420
SN54 932	SN5440
SN54 946	SN5400
SN54 948	See Note 1
SN54 962	SN5410
SN54 965	SN5430
SN54 966	SN5451

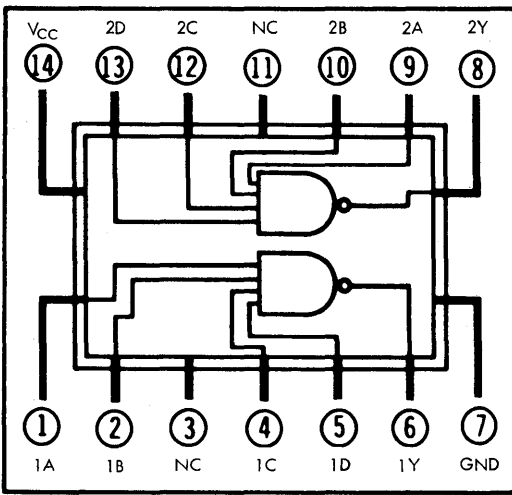
NOTE 1: The SN54 948 has no corresponding Series 54 type. Electrical and switching characteristics are included in this data sheet.

<sup>†</sup>Patented by Texas Instruments

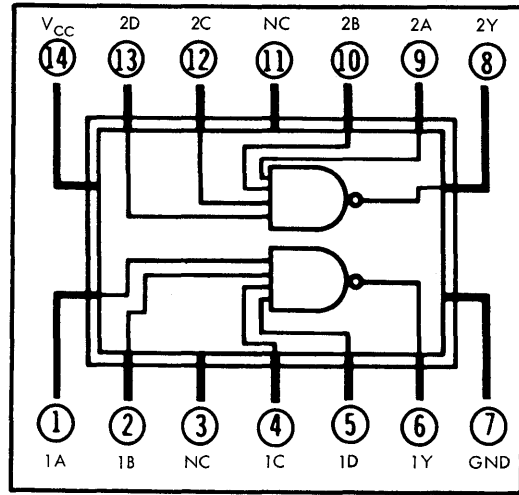


**PIN CONFIGURATIONS**

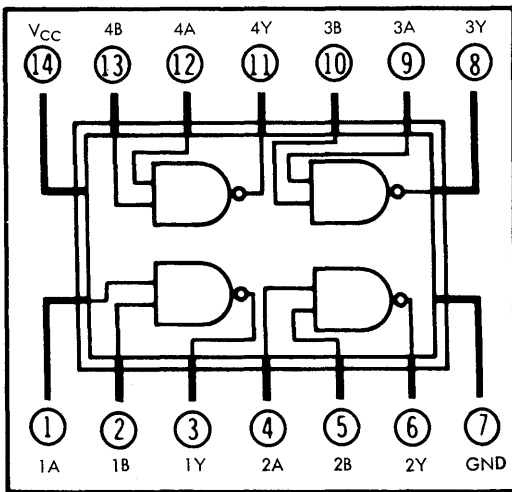
SN54 930  
DUAL 4-INPUT POSITIVE NAND GATE



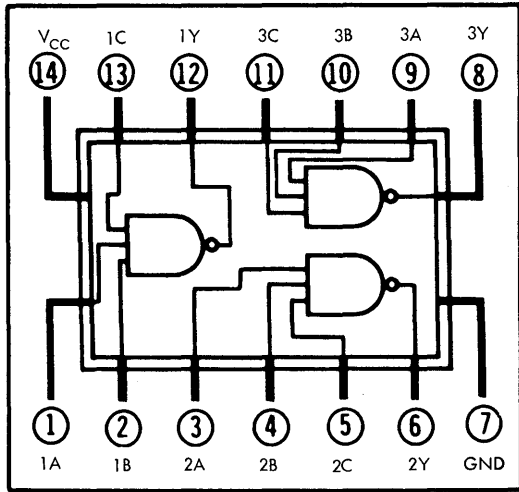
SN54 932  
DUAL 4-INPUT POSITIVE NAND BUFFER



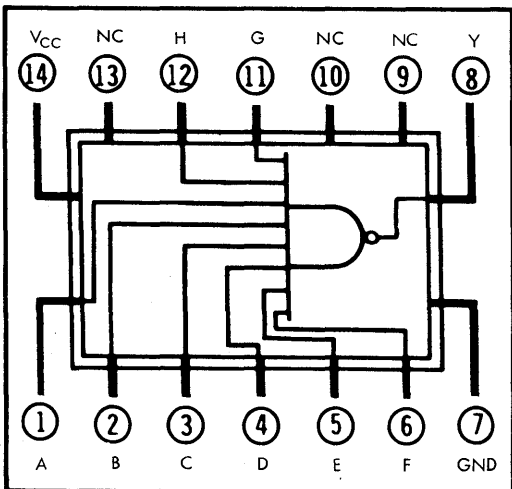
SN54 946  
QUADRUPLE 2-INPUT POSITIVE NAND GATE



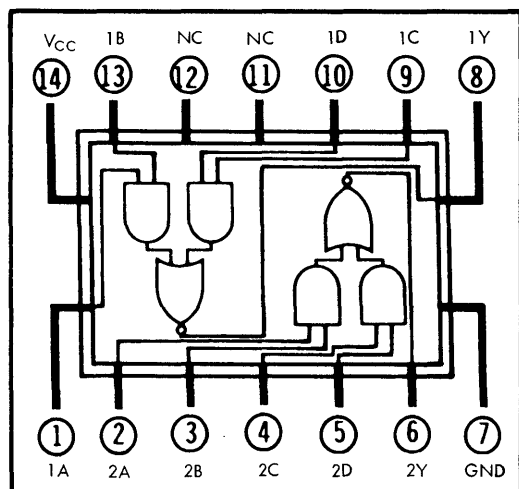
SN54 962  
TRIPLE 3-INPUT POSITIVE NAND GATE



SN54 965  
8-INPUT POSITIVE NAND GATE



SN54 966  
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE



# TYPE SN54 948 MASTER-SLAVE FLIP-FLOP

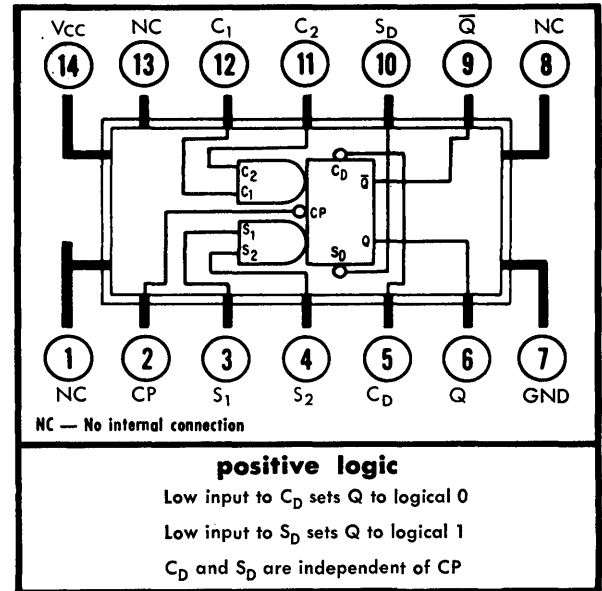
## logic

### TRUTH TABLES

R-S MODE				
$t_n$				$t_{n+1}$
$S_1$	$S_2$	$C_1$	$C_2$	Q
0	X	0	X	$Q_n$
0	X	X	0	$Q_n$
X	0	0	X	$Q_n$
X	0	X	0	$Q_n$
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	Indeterminate

J-K MODE		
$t_n$	$t_{n+1}$	
$S_1$	$C_1$	Q
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\bar{Q}_n$

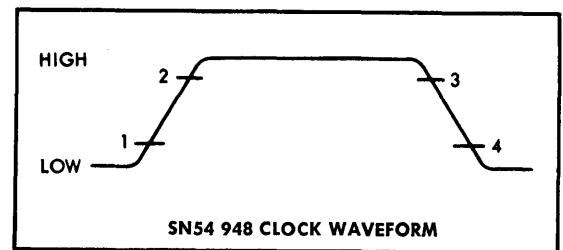
- NOTES:
1.  $t_n$  = bit time before clock pulse.
  2.  $t_{n+1}$  = bit time after clock pulse.
  3. X indicates that either a logical 1 or a logical 0 may be present.
  4. Logical 1 is more positive than logical 0.
  5. For operation in the J-K mode connect  $S_2$  to  $\bar{Q}$  and  $C_2$  to Q.



## description

The SN54 948 flip-flop is based on the master-slave principle. This device has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master.
2. Enter information from AND gate inputs to master.
3. Disable AND gate inputs.
4. Transfer information from master to slave.



## recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	4.5 V to 5.5 V
Fan-Out From Each Output, N . . . . .	1 to 10
Width of Clock Pulse, $t_{p(\text{clock})}$ (See Figure 6) . . . . .	$\geq 20$ ns
Width of Direct Set Pulse, $t_{p(SD)}$ (See Figure 7) . . . . .	$\geq 25$ ns
Width of Direct Clear Pulse, $t_{p(CD)}$ (See Figure 7) . . . . .	$\geq 25$ ns
Input Setup Time, $t_{\text{setup}}$ (See Figure 6) . . . . .	applied clock pulse width
Input Hold Time, $t_{\text{hold}}$ . . . . .	$\geq 0$



# TYPE SN54 948

## MASTER-SLAVE FLIP-FLOP

electrical characteristics,  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage	1	$V_{CC} = 4.5\text{ V}$	2			V
$V_{in(0)}$ Logical 0 input voltage	1	$V_{CC} = 4.5\text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	1	$V_{CC} = 4.5\text{ V}, I_{load} = -400\ \mu\text{A}$	2.4	3.5‡		V
$V_{out(0)}$ Logical 0 output voltage	2	$V_{CC} = 4.5\text{ V}, I_{sink} = 16\text{ mA}$		0.22‡	0.4	V
$I_{in(0)}$ Logical 0 level input current at $C_1, C_2, S_1,$ or $S_2$	3	$V_{CC} = 5.5\text{ V}, V_{in} = 0.4\text{ V}$			-1.6	mA
$I_{in(0)}$ Logical 0 level input current at $C_D$ or $S_D$	3	$V_{CC} = 5.5\text{ V}, V_{in} = 0.4\text{ V}$			-3.2	mA
$I_{in(0)}$ Logical 0 level input current at CP	3	$V_{CC} = 5.5\text{ V}, V_{in} = 0.4\text{ V}$			-4.8	mA
$I_{in(1)}$ Logical 1 level input current at $C_1, C_2, S_1,$ or $S_2$	4	$V_{CC} = 5.5\text{ V}, V_{in} = 2.4\text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}, V_{in} = 5.5\text{ V}$			1	mA
$I_{in(1)}$ Logical 1 level input current at $C_D$ or $S_D$	4	$V_{CC} = 5.5\text{ V}, V_{in} = 2.4\text{ V}$			80	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}, V_{in} = 5.5\text{ V}$			1	mA
$I_{in(1)}$ Logical 1 level input current at CP	4	$V_{CC} = 5.5\text{ V}, V_{in} = 2.4\text{ V}$			120	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}, V_{in} = 5.5\text{ V}$			1	mA
$I_{OS}$ Short-circuit output current †	5	$V_{CC} = 5.5\text{ V}, V_{in} = 0$	-20		-57	mA
$I_{CC}$ Supply current	4	$V_{CC} = 5\text{ V}, V_{in} = 5\text{ V}$		8		mA

† Not more than one output should be shorted at a time.

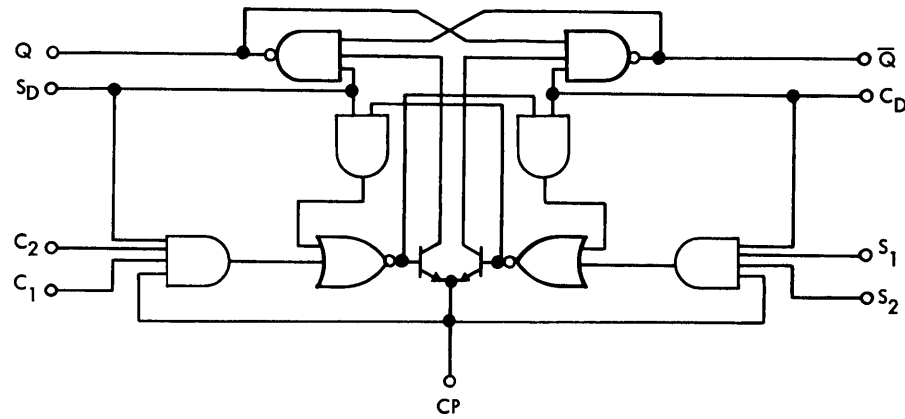
‡ These typical values are at  $V_{CC} = 5\text{ V}$ .

switching characteristics,  $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}, N = 10$

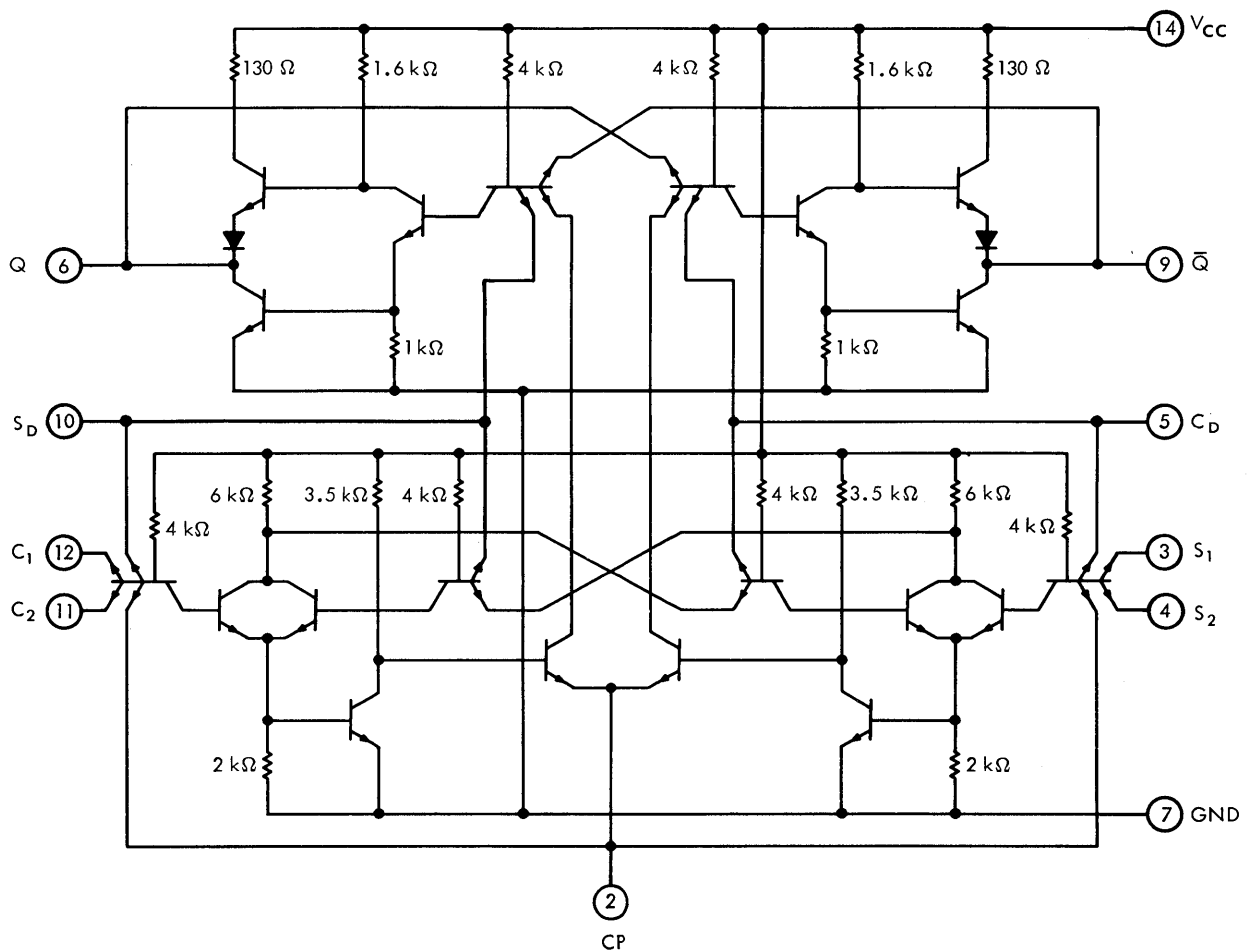
PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{clock}$ Maximum clock frequency	6		10	15		MHz
$t_{pd1}$ Propagation delay time to logical 1 level from $C_D$ or $S_D$ to output	7			26	50	ns
$t_{pd0}$ Propagation delay time to logical 0 level from $C_D$ or $S_D$ to output	7			34	50	ns
$t_{pd1}$ Propagation delay time to logical 1 level from $C_1, C_2, S_1,$ or $S_2$ to output	6		10	26	50	ns
$t_{pd0}$ Propagation delay time to logical 0 level from $C_1, C_2, S_1,$ or $S_2$ to output	6		10	34	50	ns

# TYPE SN54 948 MASTER-SLAVE FLIP-FLOP

functional block diagram



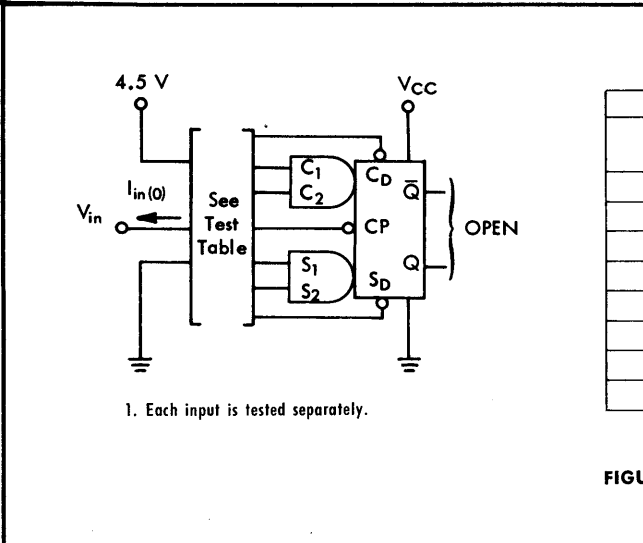
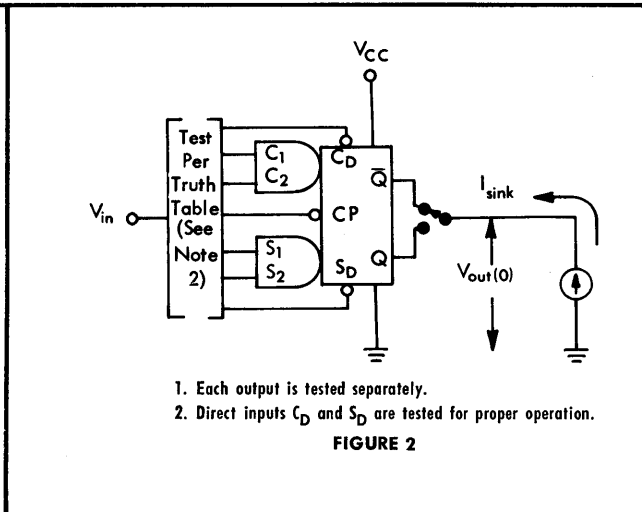
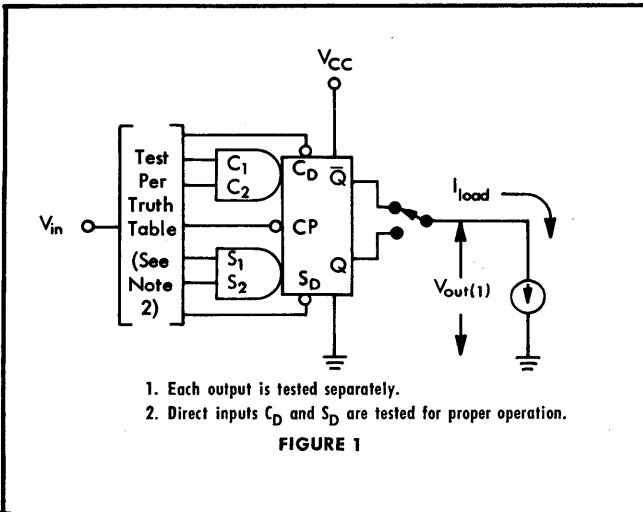
schematic



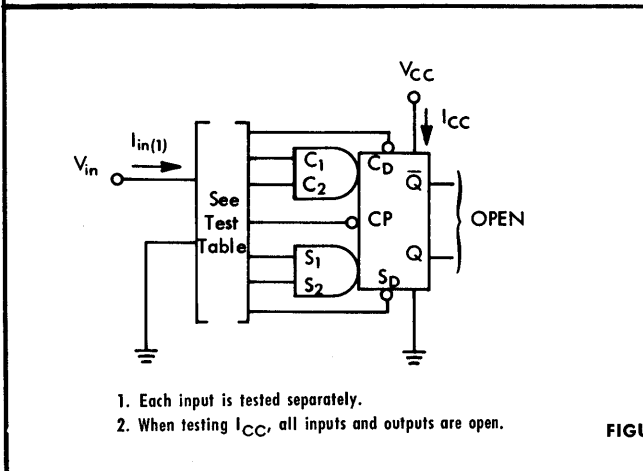
# TYPE SN54 948 MASTER-SLAVE FLIP-FLOP

## PARAMETER MEASUREMENT INFORMATION

### d-c test circuits†



TEST TABLE		
Apply $V_{in}$ (Test $I_{in}$ )	Apply Momentary GND, Then 4.5 V	Apply 4.5 V
CP	$C_D$	$C_1, C_2, S_1, S_2,$ and $S_D$
CP	$S_D$	$C_1, C_2, S_1, S_2,$ and $C_D$
$C_D$	None	$S_1, S_2,$ and CP
$S_D$	None	$C_1, C_2,$ and CP
$C_1$	None	$C_2, S_D,$ and CP
$C_2$	None	$C_1, S_D,$ and CP
$S_1$	None	$S_2, C_D,$ and CP
$S_2$	None	$S_1, C_D,$ and CP



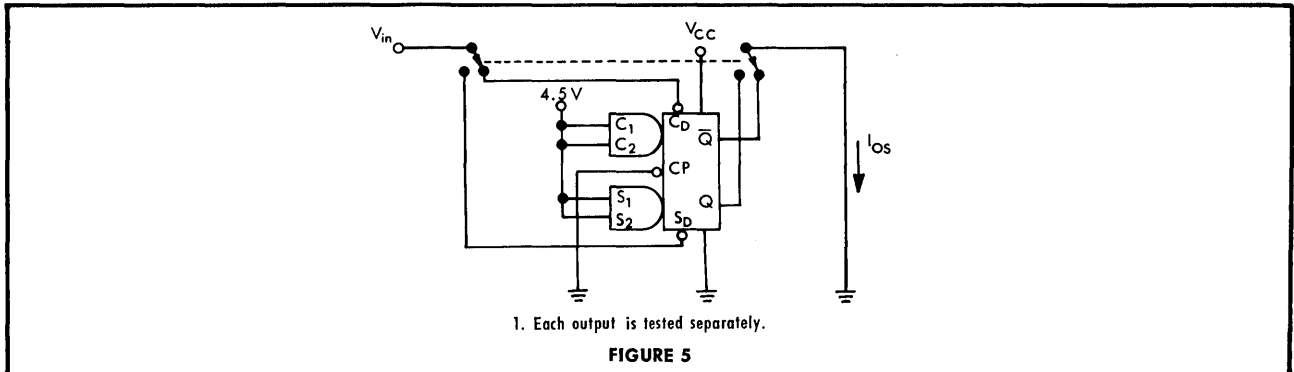
TEST TABLE	
Apply $V_{in}$ (Test $I_{in}$ )	Ground
CP	$C_D, S_D, C_1, C_2, S_1,$ and $S_2$
$C_D$	CP, $S_1,$ and $S_2$
$S_D$	CP, $C_1,$ and $C_2$
$C_1$	CP, $S_D,$ and $C_2$
$C_2$	CP, $S_D,$ and $C_1$
$S_1$	CP, $C_D,$ and $S_2$
$S_2$	CP, $C_D,$ and $S_1$

†Arrows indicate actual direction of current flow.

# TYPE SN54 948 MASTER-SLAVE FLIP-FLOP

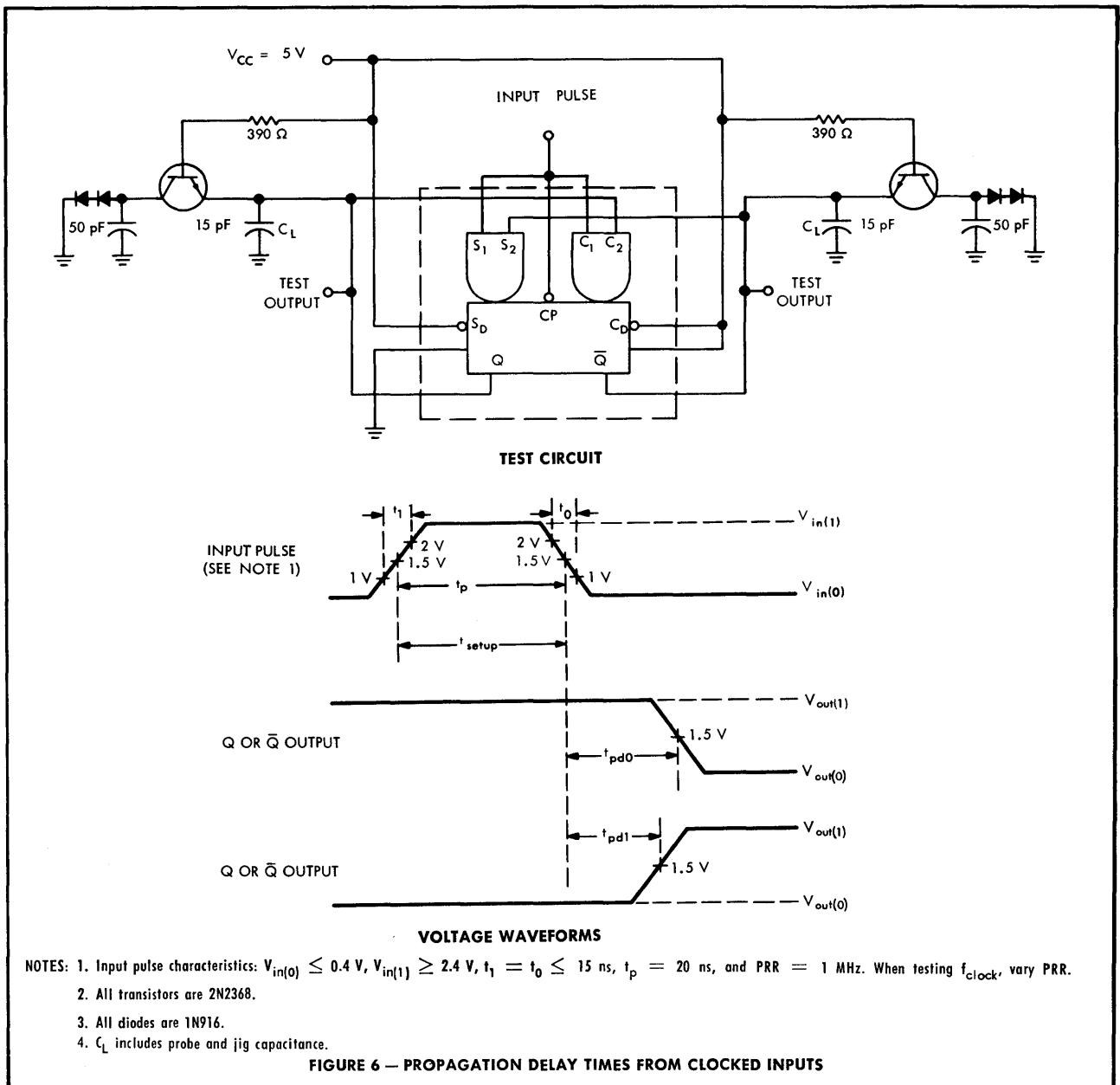
## PARAMETER MEASUREMENT INFORMATION

### d-c test circuits† (continued)



†Arrows indicate actual direction of current flow.

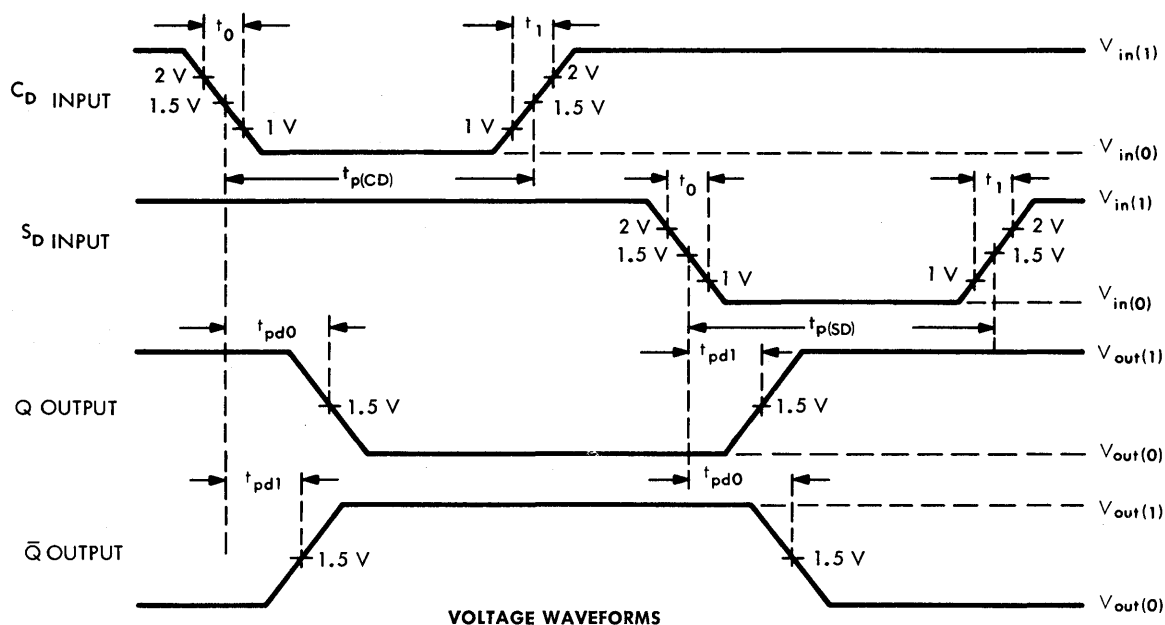
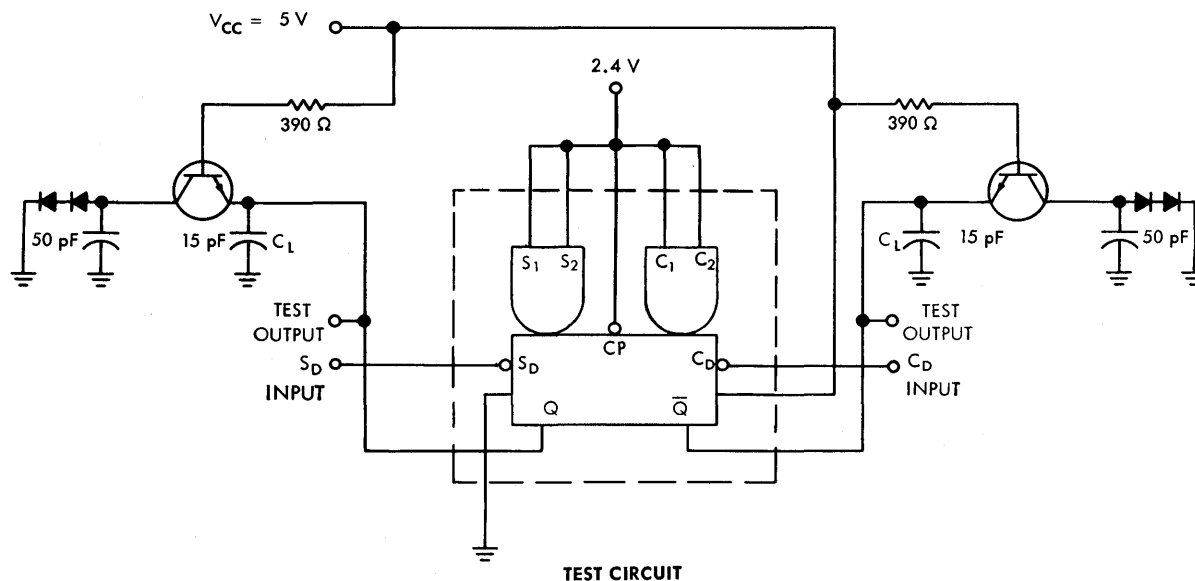
### switching characteristics



# TYPE SN54 948 MASTER-SLAVE FLIP-FLOP

## PARAMETER MEASUREMENT INFORMATION

### switching characteristics (continued)



- NOTES: 1.  $C_D$  or  $S_D$  inputs dominate regardless of the state of clock,  $C_1$ ,  $C_2$  or  $S_1$ ,  $S_2$  inputs.  
 2.  $C_D$  or  $S_D$  input pulse characteristics:  $V_{in(0)} \leq 0.4$  V,  $V_{in(1)} \geq 2.4$  V,  $t_1 = t_0 \leq 15$  ns,  $t_{p(CD)} = t_{p(SD)} = 25$  ns, and  $PRR = 1$  MHz.  
 3. All transistors are 2N2368.  
 4. All diodes are 1N916.  
 5.  $C_L$  includes probe and jig capacitance.

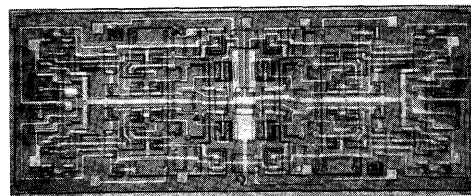
FIGURE 7 —  $C_D$  AND  $S_D$  PROPAGATION DELAY TIMES



**DIGITAL SEMICONDUCTOR NETWORKS  
FOR GENERAL PURPOSE SYSTEM APPLICATIONS**

**application**

Series 53 semiconductor networks are ideally suited for general-purpose digital applications, including computer, data handling, and control systems. Series 53 is designed and characterized for use over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .



**DUAL J-K FLIP-FLOP BAR**

**features**

**LOW SYSTEM COST**

- multifunction devices offering lowest cost per logic function

**ADVANCED PERFORMANCE**

- attractive speed/power ratio
- high a-c noise rejection from low output impedance
- waveshape integrity maintained over rated temperature and loading conditions by double-ended output stage

**EASE OF DESIGN**

- complete family available — 15 networks
- modified DTL circuitry simplifies system design
- fan-out of 10 from each double-ended output

**description**

Series 53 is a compatible line of digital semiconductor networks capable of performing all basic and some special logic functions. All basic logic functions are offered as multifunction networks. Utilization of this complete line of compatible networks reduces systems engineering design time, while the use of multifunction networks reduces system cost per logic function.

Series 53 logic employs a modified form of diode-transistor logic (DTL) where transistors replace conventional diodes in order to improve circuit performance. Input transistors reduce drive requirements while offset transistors improve switching speed. The Series 53 low-impedance output stage maintains symmetrical waveshapes over wide ranges of d-c fan-out, capacitive loads, and operating temperatures. The low-impedance output also provides a high degree of protection against capacitively coupled noise transients on system information lines.

CONTENTS	Page
DESIGN CHARACTERISTICS AND LOGIC SYMBOLS . . . . .	2002-2003
LOADING TABLES AND PIN IDENTIFICATION . . . . .	2004
DEFINITIVE SPECIFICATIONS . . . . .	2005-2028
D-C TEST CIRCUITS . . . . .	2029-2032
SWITCHING TIME TEST CIRCUITS AND VOLTAGE WAVEFORMS . . . . .	2032-2035
MECHANICAL DATA . . . . .	2036

<sup>†</sup>Patented by Texas Instruments

SERIES 53  
 BULLETIN NO. DL-S 668907, NOVEMBER 1966  
 REPLACES BULLETINS NOS. 634187 THROUGH 634192, DECEMBER 1963;  
 NOS. 657751 THROUGH 657758, AUGUST 1965; AND NO. 7446, MARCH 1965



typical operating characteristics,  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ , supply voltage  $V_{CC} = 3\text{ V}$  to  $4\text{ V}$

Speed: Gate Propagation Delay . . . . .	35 ns
Flip-flop Toggle Rate . . . . .	4 MHz
Fan-Out Capability (Double-ended Outputs) . . . . .	10
Fan-In With Expanders . . . . .	25 max
Output Impedance . . . . .	< 50 $\Omega$
Average Power Dissipation: Per Gate . . . . .	12 mW
Per Flip-flop . . . . .	40 mW

**design characteristics**

Series 53 is a compatible line of digital semiconductor integrated circuits built and characterized for medium-speed applications (up to 4 MHz) over the full military temperature range. The networks are fabricated from triple-diffused planar silicon, and employ a modified form of diode-transistor logic selected to take advantage of inherent integrated-circuit characteristics.

As in conventional diode logic (Figure A), logic is performed at node A of a Series 53 gate (Figure B).

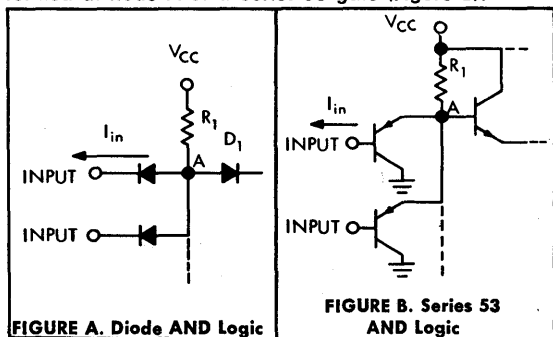


FIGURE A. Diode AND Logic

FIGURE B. Series 53 AND Logic

The gain of the p-n-p transistors replacing the input diodes increases the effective drive capability of the preceding stage. The voltage at node A is now a function of  $I_{in}$ ,  $R_1$ , and the p-n-p transistor gain, rather than only  $I_{in}$  and  $R_1$  as in diode logic. The effect of the transistor gain is to minimize the importance of the resistor value in the circuit's performance. Since silicon resistors have inherently wide production tolerances and high temperature coefficients, the transistor gain makes fabrication of Series 53 networks more economical while assuring greater stability over the full military temperature range.

The n-p-n transistor which replaces the offset diode  $D_1$  also has gain, increasing the circuit drive capability and improving the waveshapes at node A.

This basic AND logic configuration is coupled with an inverting double-ended output stage (Figure C) in each Series 53 NAND/NOR gate and each flip-flop.

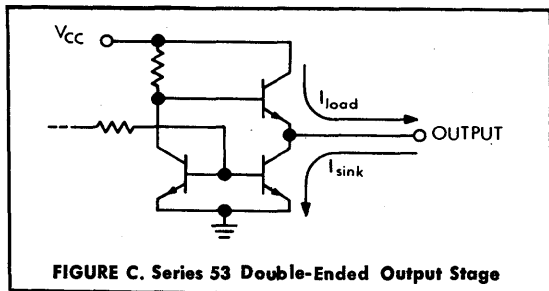


FIGURE C. Series 53 Double-Ended Output Stage

The most important feature of the Series 53 NAND/NOR gate or flip-flop output stage is its ability to supply load and sink current with low output impedance. This provides high d-c fan-out to both types of loads and simplifies interface design. Low output impedance in either state ensures that turn-on and turn-off waveshapes will remain sharp and symmetrical over a wide range of d-c and capacitive loadings throughout the temperature range. The low output impedance of these outputs ensure that every information line will have a low-impedance termination, providing valuable protection against a-c coupled noise transients.

All Series 53 networks are fabricated using a 4-step planar diffusion process. First, an n-type diffusion is made in the p-type substrate, forming the n-p-n collectors only. A second n-type diffusion is made forming the base area of the p-n-p transistors, isolation region of the resistors, one section of the capacitors, and further forming the n-p-n collectors. This sequence reduces the n-p-n transistor  $r_{CE(sat)}$  to approximately 30 ohms, while keeping the p-n-p base width narrow and the gain high (typically 12). The next step is a p-type diffusion which forms the p-n-p emitters, n-p-n bases, resistors, and another portion of the capacitors. The final diffusion is an n-type, forming the n-p-n emitters and completing the capacitors.

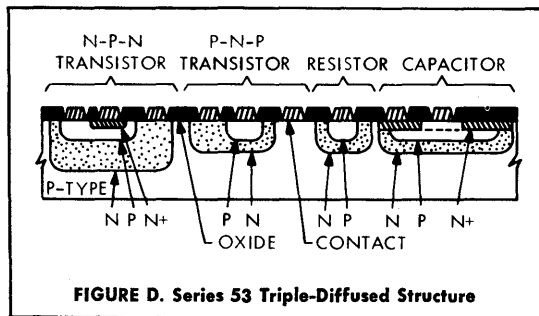


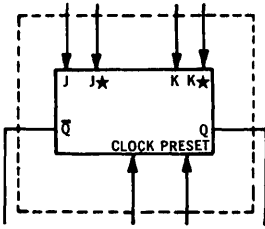
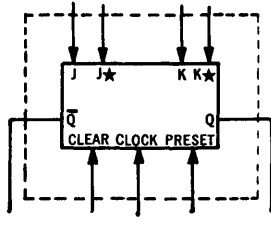
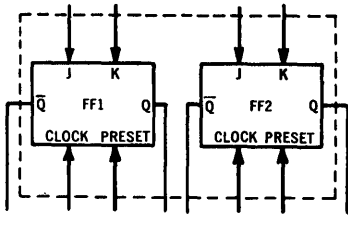
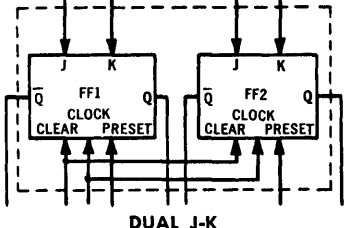
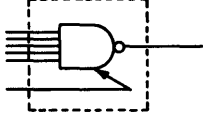
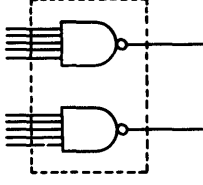
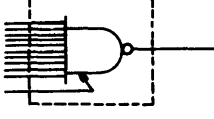
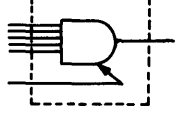
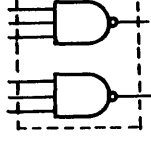
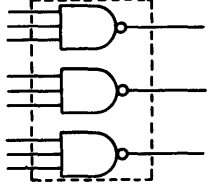
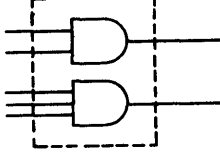
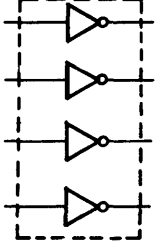
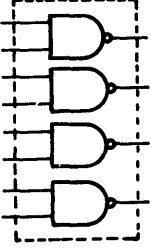
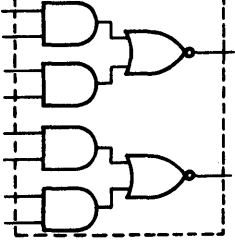
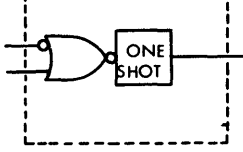
FIGURE D. Series 53 Triple-Diffused Structure

Two AND/OR gates, the SN5320 and SN5340, provide additional flexibility for the logic designer. These gates may be used in applications where noninverted signals and/or reduced propagation delay times are necessary and high fan-out is not a requirement. Characteristics of the AND/OR gates limit the number which may be cascaded (connected in series) between any Series 53 circuit and Series 53 flip-flops or inverter/drivers.

SERIES 53 AND/OR GATE CASCADING CAPABILITY

Minimum $V_{CC}$	3.2 V	3.6 V	4.0 V
Maximum number of AND/OR gates which may be cascaded	1	2	3

standard line summary

<p><b>SN5300</b> See Page 2005</p>  <p><b>J-K FLIP-FLOP WITH PRESET</b></p>	<p><b>SN5301</b> See Page 2007</p>  <p><b>J-K FLIP-FLOP WITH PRESET AND CLEAR</b></p>	<p><b>SN5302</b> See Page 2009</p>  <p><b>DUAL J-K FLIP-FLOP WITH PRESET</b></p>
<p><b>SN5304</b> See Page 2011</p>  <p><b>DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR</b></p>	<p><b>SN5310</b> See Page 2013</p>  <p><b>5-INPUT EXPANDABLE NAND/NOR GATE</b></p>	<p><b>SN5311</b> See Page 2015</p>  <p><b>DUAL 5-INPUT NAND/NOR GATE</b></p>
<p><b>SN5315</b> See Page 2016</p>  <p><b>10-INPUT EXPANDABLE NAND/NOR GATE</b></p>	<p><b>SN5320</b> See Page 2018</p>  <p><b>5-INPUT EXPANDABLE AND/OR GATE (ALSO USABLE AS 5-INPUT EXPANDER)</b></p>	<p><b>SN5330</b> See Page 2020</p>  <p><b>DUAL 3-INPUT NAND/NOR GATE</b></p>
<p><b>SN5331</b> See Page 2021</p>  <p><b>TRIPLE 3-INPUT NAND/NOR GATE</b></p>	<p><b>SN5340</b> See Page 2022</p>  <p><b>DUAL AND/OR GATE</b></p>	<p><b>SN5350</b> See Page 2024</p>  <p><b>QUADRUPLE INVERTER/DRIVER</b></p>
<p><b>SN5360</b> See Page 2025</p>  <p><b>QUADRUPLE 2-INPUT NAND/NOR GATE</b></p>	<p><b>SN5370</b> See Page 2026</p>  <p><b>DUAL EXCLUSIVE-OR GATE</b></p>	<p><b>SN5380</b> See Page 2027</p>  <p><b>ONE-SHOT MONOSTABLE MULTIVIBRATOR</b></p>



# SERIES 53

## SOLID CIRCUIT<sup>®</sup> SEMICONDUCTOR NETWORKS

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage $V_{CC}$ (See Note 1) . . . . .	+7 V
Supply Voltage $V_{EE}$ With Respect to $V_{CC}$ (SN5320 and SN5340) . . . . .	-7 V
Input Voltage $V_{in}$ (See Notes 1 and 2) . . . . .	$V_{CC}$
Operating Free-Air Temperature Range . . . . .	-55°C to 125°C
Storage Temperature Range . . . . .	-65°C to 150°C

NOTES: 1. Voltage values (with the exception of the  $V_{EE}$  rating above) are with respect to network ground terminal.  
 2. Input signals must be zero or positive with respect to network ground terminal.

### logic definition

Series 53 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE = LOGICAL 0

HIGH VOLTAGE = LOGICAL 1

### input current requirements

Weighted values of input current requirements reflect worst-case conditions for  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$  and  $V_{CC} = 3\text{ V}$  to  $4\text{ V}$ . One positive load ( $N+ = 1$ ) requires current into the input at a logical 1 voltage level (0.5 mA at  $V_{CC} = 3\text{ V}$  or  $V_{CC} = 4\text{ V}$ ). One negative load ( $N- = 1$ ) requires current out of the input at a logical 0 voltage level (0.25 mA at  $T_A = -55^\circ\text{C}$ , or 0.19 mA at  $T_A = 125^\circ\text{C}$ ). Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

WEIGHTED VALUES OF INPUT CURRENT REQUIREMENTS				
NETWORK	TYPE	INPUT	N+ LOADS	N- LOADS
FLIP-FLOPS	5300, 5301 5302	J, J*, K, K*, Preset, Clear	1	0
		Clock	2.5	2.5
	5304	J, K, Preset	1	0
		Clear Clock	2 5	0 5
GATES AND EXPANDER	5310, 5311, 5315, 5320, 5330, 5331, 5340, 5360, 5370	Each Input	0	1
ONE-SHOT	5380	T, T*	1	0
INVERTER	5350	Each Input	2	0

### output drive capability

Weighted values of fan-out reflect the ability of an output to drive current to  $N+$  loads and sink current from  $N-$  loads under worst-case conditions. Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuits indicate the actual direction of current flow.

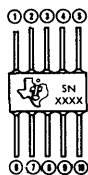
WEIGHTED VALUES OF FAN-OUT			
NETWORK	OUTPUT	N+ LOADS	N- LOADS
FLIP-FLOPS, NAND/NOR GATES, AND ONE-SHOT	Each Output	10	10
INVERTER (SN5350)	Each Output	10	10
	4 Inverters in parallel	40	40
AND/OR GATES SN5320 and SN5340	Each Output	4	4

### pin identification

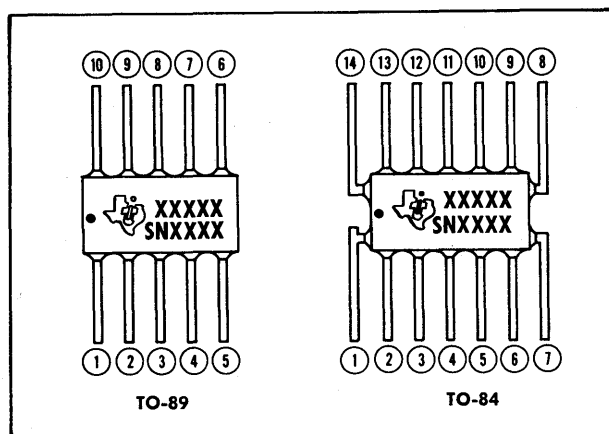
Pin identification for Series 53 networks is shown in the illustration at the right. Symbolization on package denotes orientation. For dimensions see mechanical data.

#### CAUTION:

Pin numbers of the 10-pin package have been renumbered in accordance with TO-89. The electrical functions are in the same physical location as shown on all previous data. Former pin numbers of 10-pin package are shown for reference.



FORMER  
PIN NOS.



# TYPE SN5300

## J-K FLIP-FLOP WITH PRESET

**logic**

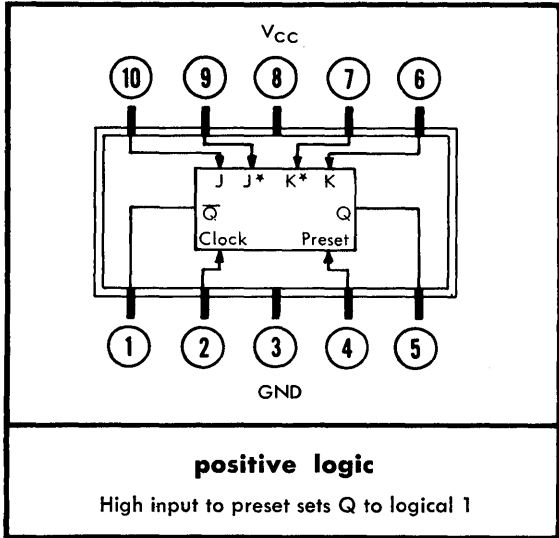
**TRUTH TABLES**

J★=K★=1		
$t_n$		$t_{n+1}$
J	K	Q
0	0	$\overline{Q_n}$
0	1	0
1	0	1
1	1	$\overline{Q_n}$

J=K=0		
$t_n$		$t_{n+1}$
J★	K★	Q
0	0	$\overline{Q_n}$
0	1	1
1	0	0
1	1	$\overline{Q_n}$

ADDITIONAL INPUT LOGIC COMBINATIONS				
$t_n$				$t_{n+1}$
J	K	J★	K★	Q
0	1	0	0	$\overline{Q_n}$
1	0	0	0	$\overline{Q_n}$
1	1	0	0	$\overline{Q_n}$
0	1	0	1	$\overline{Q_n}$
1	1	0	1	$\overline{Q_n}$
1	0	1	0	$\overline{Q_n}$
1	1	1	0	$\overline{Q_n}$
1	0	0	1	1
0	1	1	0	0

$t_n$  = Bit time before clock pulse  
 $t_{n+1}$  = Bit time after clock pulse



**recommended operating conditions**

Supply Voltage $V_{CC}$	3 V to 4 V
Maximum Fan-out From Each Output Into Positive Loads, $N+$	10
Maximum Fan-out From Each Output Into Negative Loads, $N-$	10
Fall Time of Clock Pulse $t_{f(\text{clock})}$	20 to 150 ns
Minimum Width of Clock Pulse $t_{p(\text{clock})}$	50 ns
Rise Time of Clock Pulse $t_{r(\text{clock})}$	10 to 500 ns

**electrical characteristics (unless otherwise noted,  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 3\text{ V}$  to  $4\text{ V}$ )**

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at J, K, J★, K★, preset, and clock	1, 2	$V_{CC} = 3\text{ V}$	1.5		3	V
		$V_{CC} = 4\text{ V}$	1.5		4	V
$V_{in(0)}$ Input voltage required to ensure logical 0 at J, K, J★, K★, preset, and clock	1, 2		0		0.3	V
$V_{out(1)}$ Logical 1 output voltage (off level)	3	$V_{CC} = 3\text{ V}, N+ = 10 (I_{load} = -5\text{ mA})$	1.7		3	V
		$V_{CC} = 4\text{ V}, N+ = 10 (I_{load} = -5\text{ mA})$	2.7		4	V
$V_{out(0)}$ Logical 0 output voltage (on level)	3	$N- = 10 (I_{sink} = 2.5\text{ mA}), T_A = -55^\circ\text{C}$	0		0.3	V
		$N- = 10 (I_{sink} = 1.9\text{ mA}), T_A = 125^\circ\text{C}$	0		0.3	V
$I_{in}$ J, K, J★, K★, or preset input current	3	$V_{in} = 2.7\text{ V}$	0		0.5	mA
		$V_{in} = 2\text{ V}$	0		1.25	mA
$I_{in}$ Clock input current	3	$V_{in} = 0.3\text{ V}, T_A = -55^\circ\text{C}$			-0.625	mA
		$V_{in} = 0.3\text{ V}, T_A = 125^\circ\text{C}$			-0.475	mA
$I_{CC(av)}$ Average supply current	4	$V_{CC} = 3\text{ V}, N+ = N- = 0, \text{Toggle} = 1\text{ MHz}, T_A = 25^\circ\text{C}$		9		mA
		$V_{CC} = 4\text{ V}, N+ = N- = 0, \text{Toggle} = 1\text{ MHz}, T_A = 25^\circ\text{C}$		13		mA

**CAUTION:**

This device was formerly TYPE SN530. Pin numbers of the SN5300 have been renumbered in accordance with TO-89. The electrical functions of the SN530 and the SN5300 are in the same physical location. See pin identification, page 2004, for SN530 pin numbers.

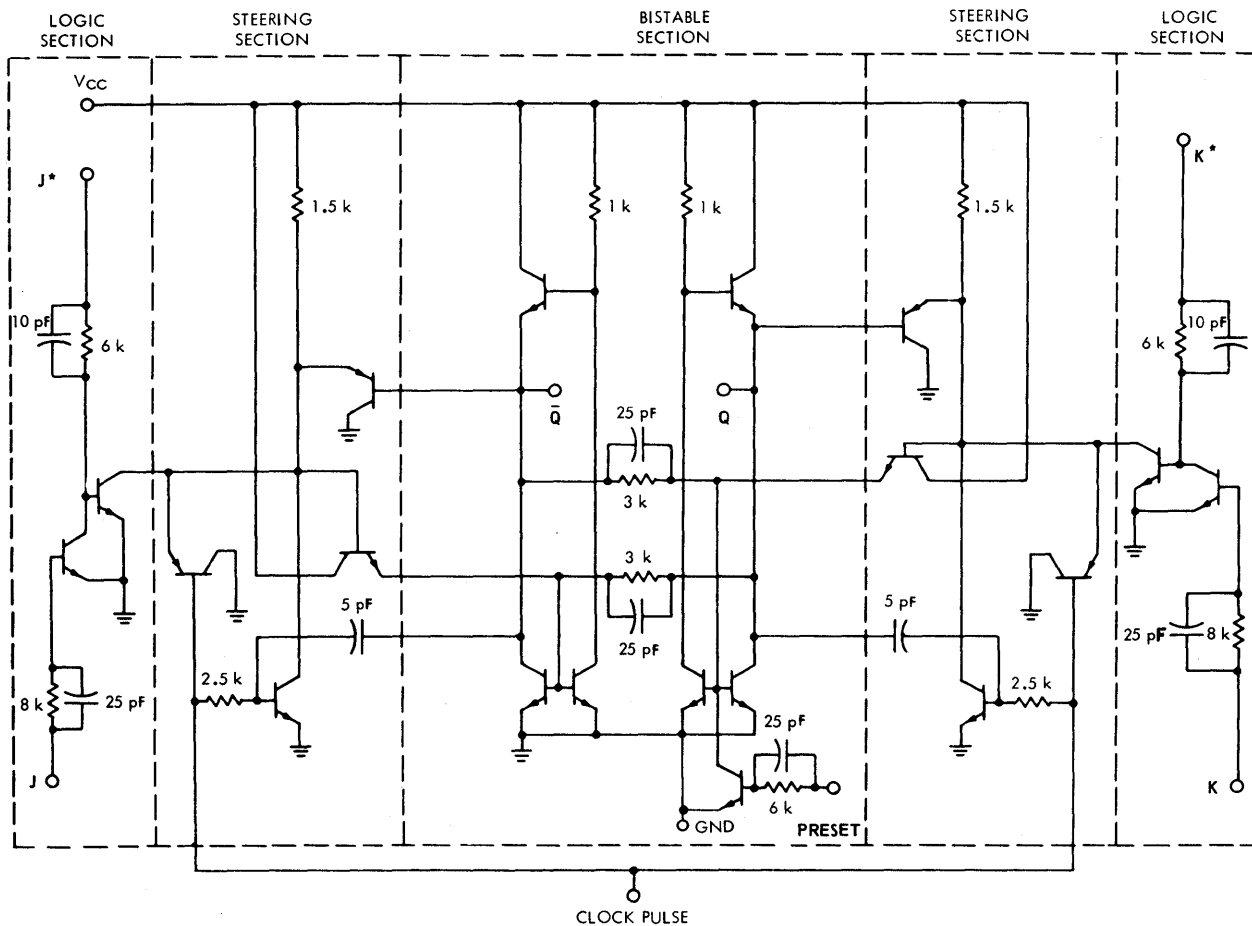
# TYPE SN5300

## J-K FLIP-FLOP WITH PRESET

switching characteristics,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ V}$ ,  $N + = N - = 0$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$ Delay Time	22	Clock Input: $V_{in} = 2.5\text{ V}$ , $t_f = 20\text{ ns}$ , $t_p = 500\text{ ns}$ , $f = 1\text{ MHz}$ J, J*, K and K* Input: $V_{in} = V_{CC}$ Preset Input: $V_{in} = 0$	20	30	ns
$t_r$ Rise Time			20	45	ns
$t_s$ Storage Time			40	60	ns
$t_f$ Fall Time			25	40	ns
Time to Set a Logical 1: J or K J* or K*	23	Clock Input: $V_{in} = 2.5\text{ V}$ , $t_f = 20\text{ ns}$ , $t_p = 500\text{ ns}$ , $f = 1\text{ MHz}$ J, J*, K or K* Input: $V_{in(1)} = 2.5\text{ V}$ , $V_{in(0)} = 0$ , $t_r = t_f = 50\text{ ns}$	50		ns
Time to Set a Logical 0: J or K J* or K*			35		ns
$t_{set(1)}$			40		ns
$t_{set(0)}$			40		ns
$t_{preset}$ Preset Time	24	Clock Input: $V_{in} = 0$ Preset Input: $V_{in} = 2.5\text{ V}$ , $t_f = 50\text{ ns}$	55		ns

### schematic



NOTES: a. Component values shown are nominal.  
b. Resistor values are in ohms.

# TYPE SN5301

## J-K FLIP-FLOP WITH PRESET AND CLEAR

logic

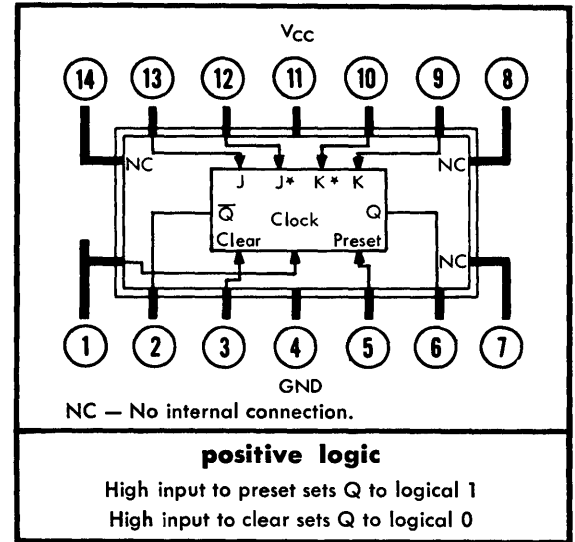
TRUTH TABLES

J★ = K★ = 1		
J	K	Q <sub>n+1</sub>
0	0	Q <sub>n</sub>
0	1	0
1	0	1
1	1	$\overline{Q}_n$

J = K = 0		
J★	K★	Q
0	0	$\overline{Q}_n$
0	1	1
1	0	0
1	1	Q <sub>n</sub>

ADDITIONAL INPUT LOGIC COMBINATIONS				
J	K	J★	K★	Q
0	1	0	0	$\overline{Q}_n$
1	0	0	0	$\overline{Q}_n$
1	1	0	0	$\overline{Q}_n$
0	1	0	1	$\overline{Q}_n$
1	1	0	1	$\overline{Q}_n$
1	0	1	0	$\overline{Q}_n$
1	1	1	0	$\overline{Q}_n$
1	0	0	1	1
0	1	1	0	0

t<sub>n</sub> = Bit time before clock pulse  
t<sub>n+1</sub> = Bit time after clock pulse



### recommended operating conditions

Supply Voltage V <sub>CC</sub>	3 V to 4 V
Maximum Fan-out From Each Output Into Positive Loads, N <sup>+</sup>	10
Maximum Fan-out From Each Output Into Negative Loads, N <sup>-</sup>	10
Fall Time of Clock Pulse t <sub>f(clock)</sub>	20 to 150 ns
Minimum Width of Clock Pulse t <sub>p(clock)</sub>	50 ns
Rise Time of Clock Pulse t <sub>r(clock)</sub>	10 to 500 ns

### electrical characteristics (unless otherwise noted, T<sub>A</sub> = -55°C to 125°C, V<sub>CC</sub> = 3 V to 4 V)

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>in(1)</sub>	1, 2	V <sub>CC</sub> = 3 V	1.5		3	V
		V <sub>CC</sub> = 4 V	1.5		4	V
V <sub>in(0)</sub>	1, 2		0		0.3	V
V <sub>out(1)</sub>	3	V <sub>CC</sub> = 3 V, N <sup>+</sup> = 10 (I <sub>load</sub> = -5 mA)	1.7		3	V
		V <sub>CC</sub> = 4 V, N <sup>+</sup> = 10 (I <sub>load</sub> = -5 mA)	2.7		4	V
V <sub>out(0)</sub>	3	N <sup>-</sup> = 10 (I <sub>sink</sub> = 2.5 mA), T <sub>A</sub> = -55°C	0		0.3	V
		N <sup>-</sup> = 10 (I <sub>sink</sub> = 1.9 mA), T <sub>A</sub> = 125°C	0		0.3	V
I <sub>in</sub>	3	V <sub>in</sub> = 2.7 V	0		0.5	mA
I <sub>in</sub>	3	V <sub>in</sub> = 2 V	0		1.25	mA
		V <sub>in</sub> = 0.3 V, T <sub>A</sub> = -55°C			-0.625	mA
		V <sub>in</sub> = 0.3 V, T <sub>A</sub> = 125°C			-0.475	mA
I <sub>CC(av)</sub>	4	V <sub>CC</sub> = 3 V, N <sup>+</sup> = N <sup>-</sup> = 0, Toggle = 1 MHz, T <sub>A</sub> = 25°C		9		mA
		V <sub>CC</sub> = 4 V, N <sup>+</sup> = N <sup>-</sup> = 0, Toggle = 1 MHz, T <sub>A</sub> = 25°C		13		mA

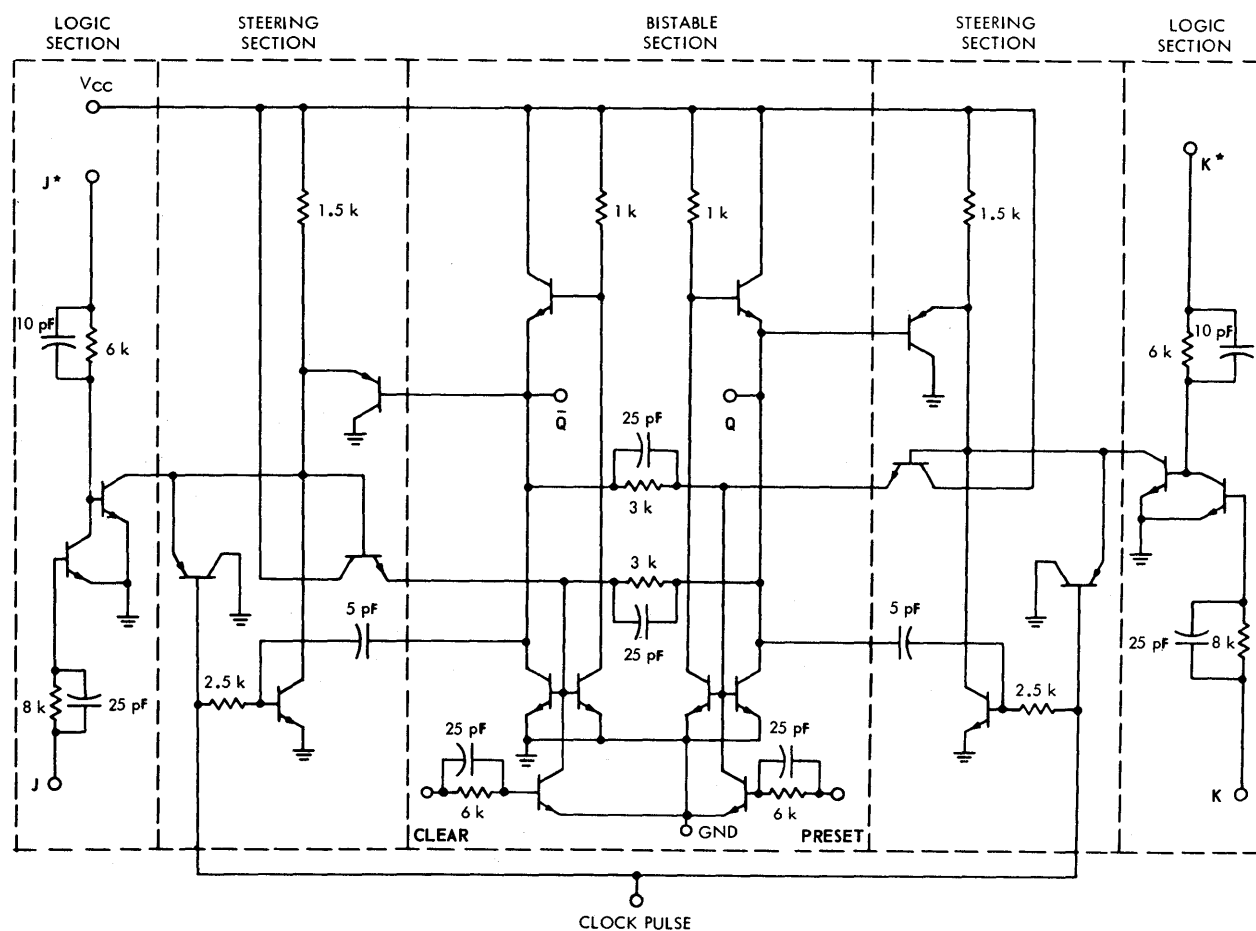
# TYPE SN5301

## J-K FLIP-FLOP WITH PRESET AND CLEAR

switching characteristics,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ V}$ ,  $N_+ = N_- = 0$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$ Delay Time	22	Clock Input: $V_{in} = 2.5\text{ V}$ , $t_f = 20\text{ ns}$ , $t_p = 500\text{ ns}$ , $f = 1\text{ MHz}$ J, J*, K and K* Input: $V_{in} = V_{CC}$ Preset Input: $V_{in} = 0$ Clear Input: $V_{in} = 0$	20	30	ns
$t_r$ Rise Time			20	45	ns
$t_s$ Storage Time			40	60	ns
$t_f$ Fall Time			25	40	ns
$t_{set\{1\}}$ Time to Set a Logical 1: J or K J* or K*	23	Clock Input: $V_{in} = 2.5\text{ V}$ , $t_f = 20\text{ ns}$ , $t_p = 500\text{ ns}$ , $f = 1\text{ MHz}$ J, J*, K and K* Input: $V_{in\{1\}} = 2.5\text{ V}$ , $V_{in\{0\}} = 0$ , $t_r = t_f = 50\text{ ns}$	50		ns
$t_{set\{0\}}$ Time to Set a Logical 0: J or K J* or K*			35		ns
$t_{preset}$ Preset Time	24	Clock Input: $V_{in} = 0$ Preset Input: $V_{in} = 2.5\text{ V}$ , $t_f = 50\text{ ns}$	55		ns
$t_{clear}$ Clear Time	24	Clock Input: $V_{in} = 0$ Clear Input: $V_{in} = 2.5\text{ V}$ , $t_f = 50\text{ ns}$	75		ns

### schematic



NOTES: a. Component values shown are nominal.  
b. Resistor values are in ohms.

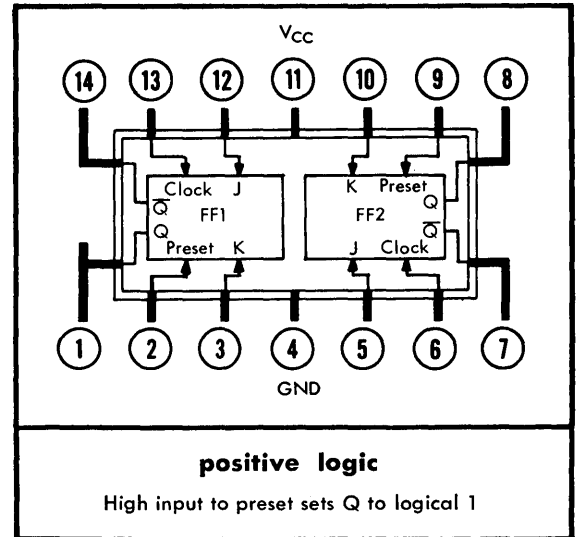
# TYPE SN5302 DUAL J-K FLIP-FLOP WITH PRESET

## logic

TRUTH TABLE  
EACH FLIP-FLOP

$t_n$		$t_{n+1}$
J	K	Q
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\bar{Q}_n$

$t_n$  = Bit time before clock pulse  
 $t_{n+1}$  = Bit time after clock pulse



## recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	3 V to 4 V
Maximum Fan-out From Each Output Into Positive Loads, $N^+$ . . . . .	10
Maximum Fan-out From Each Output Into Negative Loads, $N^-$ . . . . .	10
Fall Time of Clock Pulse $t_{f(\text{clock})}$ . . . . .	20 to 150 ns
Minimum Width of Clock Pulse $t_{p(\text{clock})}$ . . . . .	. 50 ns
Rise Time of Clock Pulse $t_{r(\text{clock})}$ . . . . .	10 to 500 ns

## electrical characteristics (unless otherwise noted, $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$ , $V_{CC} = 3\text{ V}$ to $4\text{ V}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at J, K, preset, and clock	1, 2	$V_{CC} = 3\text{ V}$	1.5		3	V
		$V_{CC} = 4\text{ V}$	1.5		4	V
$V_{in(0)}$ Input voltage required to ensure logical 0 at J, K, preset, and clock	1, 2		0		0.3	V
$V_{out(1)}$ Logical 1 output voltage (off level)	3	$V_{CC} = 3\text{ V}$ , $N^+ = 10$ ( $I_{load} = -5\text{ mA}$ )	1.7		3	V
		$V_{CC} = 4\text{ V}$ , $N^+ = 10$ ( $I_{load} = -5\text{ mA}$ )	2.7		4	V
$V_{out(0)}$ Logical 0 output voltage (on level)	3	$N^- = 10$ ( $I_{sink} = 2.5\text{ mA}$ ), $T_A = -55^\circ\text{C}$	0		0.3	V
		$N^- = 10$ ( $I_{sink} = 1.9\text{ mA}$ ), $T_A = 125^\circ\text{C}$	0		0.3	V
$I_{in}$ J, K, or preset input current	3	$V_{in} = 2.7\text{ V}$	0		0.5	mA
		$V_{in} = 2\text{ V}$	0		1.25	mA
$I_{in}$ Clock input current	3	$V_{in} = 0.3\text{ V}$ , $T_A = -55^\circ\text{C}$			-0.625	mA
		$V_{in} = 0.3\text{ V}$ , $T_A = 125^\circ\text{C}$			-0.475	mA
$I_{CC(av)}$ Average supply current (each flip-flop)	4	$V_{CC} = 3\text{ V}$ , $N^+ = N^- = 0$ , Toggle = 1 MHz, $T_A = 25^\circ\text{C}$		9		mA
		$V_{CC} = 4\text{ V}$ , $N^+ = N^- = 0$ , Toggle = 1 MHz, $T_A = 25^\circ\text{C}$		13		mA

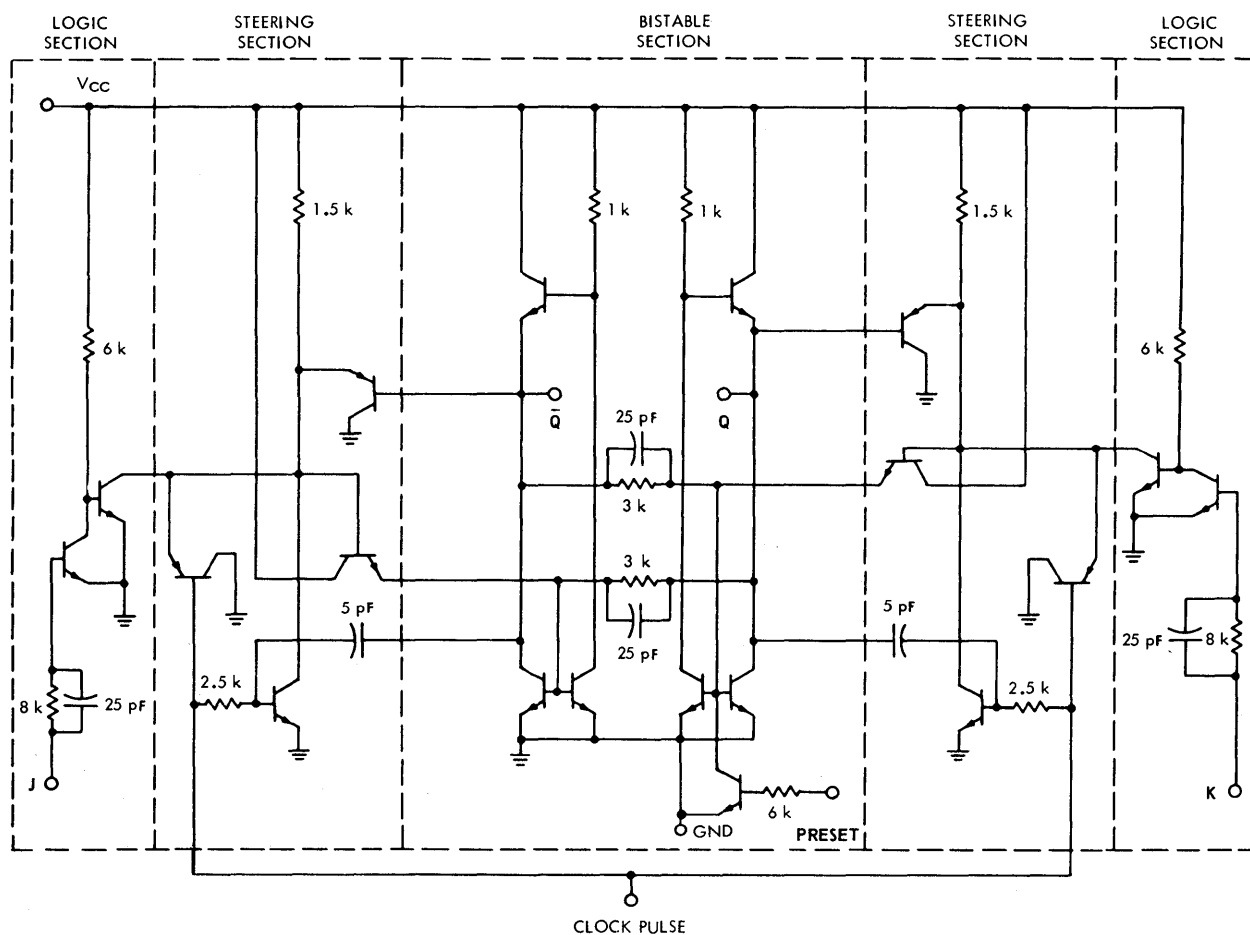
# TYPE SN5302

## DUAL J-K FLIP-FLOP WITH PRESET

switching characteristics,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ V}$ ,  $N + = N - = 0$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$ Delay Time	22	Clock Input: $V_{in} = 2.5\text{ V}$ , $t_f = 20\text{ ns}$ , $t_p = 500\text{ ns}$ , $f = 1\text{ MHz}$	20	30	ns
$t_r$ Rise Time		J and K Input: $V_{in} = V_{CC}$	20	45	ns
$t_s$ Storage Time		Preset Input: $V_{in} = 0$	40	60	ns
$t_f$ Fall Time			25	40	ns
$t_{set(1)}$ Time to Set a Logical 1: J or K	23	Clock Input: $V_{in} = 2.5\text{ V}$ , $t_f = 20\text{ ns}$ , $t_p = 500\text{ ns}$ , $f = 1\text{ MHz}$	50		ns
$t_{set(0)}$ Time to Set a Logical 0: J or K		J and K Input: $V_{in(1)} = 2.5\text{ V}$ , $V_{in(0)} = 0$ , $t_r = t_f = 50\text{ ns}$	40		ns
$t_{preset}$ Preset Time	24	Clock Input: $V_{in} = 0$ Preset Input: $V_{in} = 2.5\text{ V}$ , $t_f = 50\text{ ns}$	75		ns

### schematic (each flip-flop)



NOTES: a. Component values shown are nominal.  
b. Resistor values are in ohms.

# TYPE SN5304

## DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR

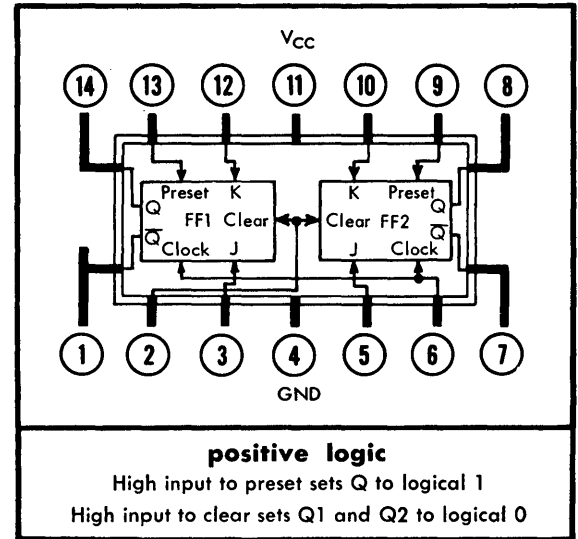
logic

TRUTH TABLE  
EACH FLIP-FLOP

$t_n$		$t_{n+1}$
J	K	Q
0	0	$\overline{Q}_n$
0	1	0
1	0	1
1	1	$\overline{Q}_n$

$t_n$  = Bit time before clock pulse

$t_{n+1}$  = Bit time after clock pulse



### recommended operating conditions

Supply Voltage $V_{CC}$	3 V to 4 V
Maximum Fan-out From Each Output Into Positive Loads, $N+$	10
Maximum Fan-out From Each Output Into Negative Loads, $N-$	10
Fall Time of Clock Pulse $t_{f(\text{clock})}$	20 to 150 ns
Minimum Width of Clock Pulse $t_{p(\text{clock})}$	50 ns
Rise Time of Clock Pulse $t_{r(\text{clock})}$	10 to 500 ns

### electrical characteristics (unless otherwise noted, $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$ , $V_{CC} = 3\text{ V}$ to $4\text{ V}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at J, K, preset, clock and clear	1, 2	$V_{CC} = 3\text{ V}$	1.5		3	V
		$V_{CC} = 4\text{ V}$	1.5		4	V
$V_{in(0)}$ Input voltage required to ensure logical 0 at J, K, preset, clock and clear	1, 2		0		0.3	V
$V_{out(1)}$ Logical 1 output voltage (off level)	3	$V_{CC} = 3\text{ V}, N+ = 10$ ( $I_{load} = -5\text{ mA}$ )	1.7		3	V
		$V_{CC} = 4\text{ V}, N+ = 10$ ( $I_{load} = -5\text{ mA}$ )	2.7		4	V
$V_{out(0)}$ Logical 0 output voltage (on level)	3	$N- = 10$ ( $I_{sink} = 2.5\text{ mA}$ ), $T_A = -55^\circ\text{C}$	0		0.3	V
		$N- = 10$ ( $I_{sink} = 1.9\text{ mA}$ ), $T_A = 125^\circ\text{C}$	0		0.3	V
$I_{in}$ J, K, or preset input current	3	$V_{in} = 2.7\text{ V}$	0		0.5	mA
		$V_{in} = 2\text{ V}$	0		2.5	mA
$I_{in}$ Clock input current	3	$V_{in} = 0.3\text{ V}$ , $T_A = -55^\circ\text{C}$			-1.25	mA
		$V_{in} = 0.3\text{ V}$ , $T_A = 125^\circ\text{C}$			-0.95	mA
		$V_{in} = 2.7\text{ V}$	0		1	mA
$I_{CC(av)}$ Average supply current (each flip-flop)	4	$V_{CC} = 3\text{ V}$ , $N+ = N- = 0$ , Toggle = 1 MHz, $T_A = 25^\circ\text{C}$		9		mA
		$V_{CC} = 4\text{ V}$ , $N+ = N- = 0$ , Toggle = 1 MHz, $T_A = 25^\circ\text{C}$		13		mA



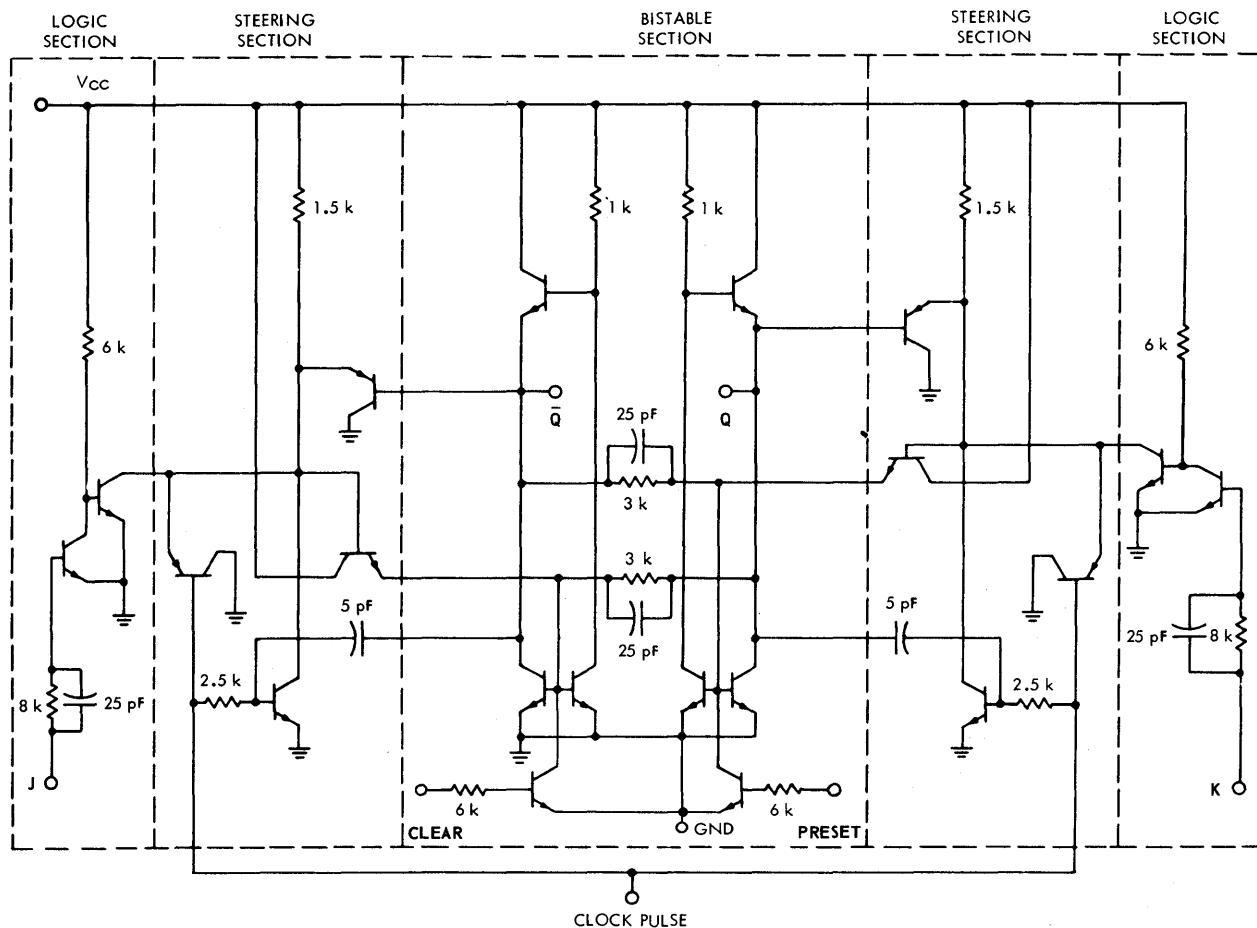
# TYPE SN5304

## DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR

switching characteristics,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ V}$ ,  $N + = N - = 0$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$ Delay Time	22	Clock Input: $V_{in} = 2.5\text{ V}$ , $t_f = 20\text{ ns}$ , $t_p = 500\text{ ns}$ , $f = 1\text{ MHz}$ J and K Input: $V_{in} = V_{CC}$ Preset Input: $V_{in} = 0$ Clear Input: $V_{in} = 0$	20	30	ns
$t_r$ Rise Time			20	45	ns
$t_s$ Storage Time			40	60	ns
$t_f$ Fall Time			25	40	ns
$t_{set(1)}$ Time to Set a Logical 1: J or K	23	Clock Input: $V_{in} = 2.5\text{ V}$ , $t_f = 20\text{ ns}$ , $t_p = 500\text{ ns}$ , $f = 1\text{ MHz}$ J or K Input: $V_{in(1)} = 2.5\text{ V}$ , $V_{in(0)} = 0$ , $t_r = t_f = 50\text{ ns}$	50		ns
$t_{set(0)}$ Time to Set a Logical 0: J or K			40		ns
$t_{preset}$ Preset Time	24	Clock Input: $V_{in} = 0$ Preset Input: $V_{in} = 2.5\text{ V}$ , $t_f = 50\text{ ns}$	75		ns
$t_{clear}$ Clear Time	24	Clock Input: $V_{in} = 0$ Clear Input: $V_{in} = 2.5\text{ V}$ , $t_f = 50\text{ ns}$	100		ns

### schematic (each flip-flop)

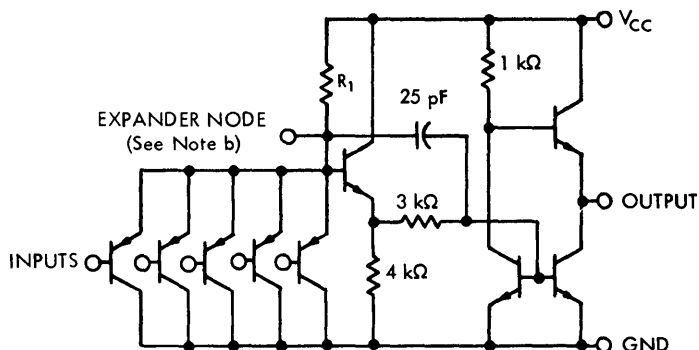


NOTES: a. Component values shown are nominal.  
b. Resistor values are in ohms.

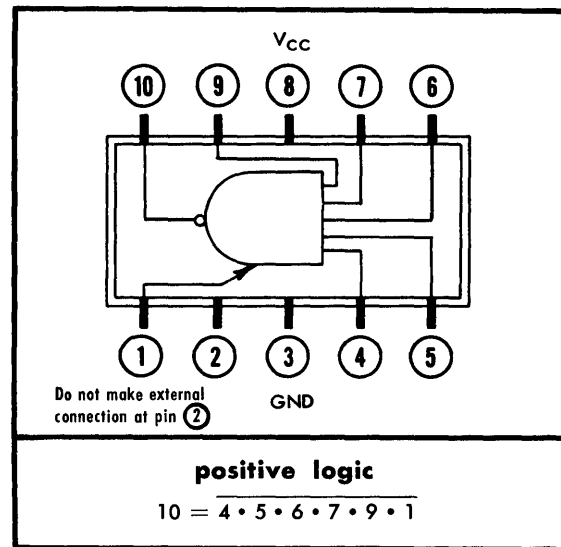
# TYPE SN5310

## 5-INPUT EXPANDABLE NAND/NOR GATE

### schematic



- NOTES: a. Component values shown are nominal.
- b. Four SN5320 expanders may be fanned into one SN5310 to provide a total fan-in of 25. If expander is not used, leave pin ① open.



### recommended operating conditions

Supply Voltage $V_{CC}$	3 V to 4 V
Maximum Fan-out Into Positive Loads, $N^+$	10
Maximum Fan-out Into Negative Loads, $N^-$	10

### electrical characteristics (unless otherwise noted $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$ , $V_{CC} = 3\text{ V}$ to $4\text{ V}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 0 (on level) at output	5	$V_{CC} = 3\text{ V}$	1.7		3	V
		$V_{CC} = 4\text{ V}$	2.5		4	V
$V_{in(1)X}$ Input voltage required at expander node (pin ①) to ensure logical 0 (on level) at output	6	$V_{CC} = 3\text{ V}, T_A = -55^\circ\text{C}$	2.35		3	V
		$V_{CC} = 3\text{ V}, T_A = 125^\circ\text{C}$	1.9		3	V
		$V_{CC} = 4\text{ V}, T_A = -55^\circ\text{C}$	3.15		4	V
		$V_{CC} = 4\text{ V}, T_A = 125^\circ\text{C}$	2.7		4	V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 (off level) at output	7		0		0.3	V
$V_{in(0)X}$ Input voltage required at expander node (pin ①) to ensure logical 1 (off level) at output	8	$T_A = -55^\circ\text{C}$	0		1.5	V
		$T_A = 125^\circ\text{C}$	0		0.95	V

### CAUTION:

This device was formerly TYPE SN531. Pin numbers of the SN5310 have been renumbered in accordance with TO-89. The electrical functions of the SN531 and the SN5310 are in the same physical location. See pin identification, page 2004, for SN531 pin numbers.

# TYPE SN5310

## 5-INPUT EXPANDABLE NAND/NOR GATE

### electrical characteristics (continued)

(unless otherwise noted,  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 3\text{ V}$  to  $4\text{ V}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{out(1)}$ Logical 1 output voltage (off level)	7	$V_{CC} = 3\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = 10$ ( $I_{load} = -5\text{ mA}$ )	1.7		3	V
		$V_{CC} = 4\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = 10$ ( $I_{load} = -5\text{ mA}$ )	2.7		4	V
$V_{out(0)}$ Logical 0 output voltage (on level)	5	$V_{CC} = 3\text{ V}$ , $V_{in} = 1.7\text{ V}$ , $N- = 10$ ( $I_{sink} = 2.5\text{ mA}$ ), $T_A = -55^\circ\text{C}$			0.3	V
		$V_{CC} = 3\text{ V}$ , $V_{in} = 1.7\text{ V}$ , $N- = 10$ ( $I_{sink} = 1.9\text{ mA}$ ), $T_A = 125^\circ\text{C}$	0		0.3	V
$I_{in}$ Input current (each input)	7	$V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = -55^\circ\text{C}$			-0.25	mA
		$V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = 125^\circ\text{C}$			-0.19	mA
$I_{CC(on)}$ On level supply current (each gate)	9	$V_{CC} = V_{in} = 3\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		3.3		mA
		$V_{CC} = V_{in} = 4\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		4.5		mA
$I_{CC(off)}$ Off level supply current (each gate)	9	$V_{CC} = 3\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		1.2		mA
		$V_{CC} = 4\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		1.6		mA
$R_1$ Resistance value of $R_1$	10	$T_A = -55^\circ\text{C}$	1.24		2.6	k $\Omega$
		$T_A = 125^\circ\text{C}$	1.7		3.25	k $\Omega$

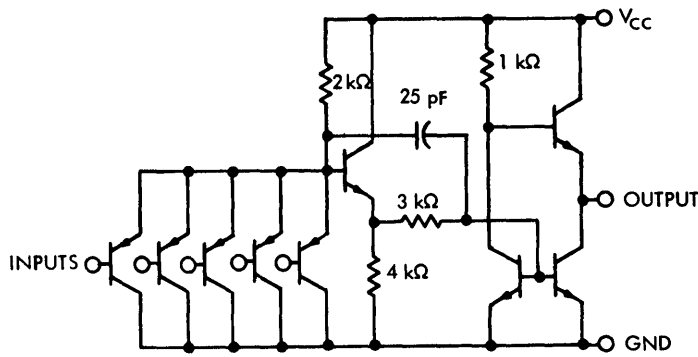
### switching characteristics, $T_A = 25^\circ\text{C}$ , $V_{CC} = 3.5\text{ V}$ , $N- = 1$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$ Delay Time	25	Input: $V_{in} = 2.5\text{ V}$ , $f = 1\text{ MHz}$ , $t_p = 500\text{ ns}$ , $t_r = t_f = 20\text{ ns}$	35	45	ns
$t_r$ Rise Time			40	50	ns
$t_s$ Storage Time			25	45	ns
$t_f$ Fall Time			30	40	ns
$t_{pd}$ Propagation Delay Time	26		30		ns

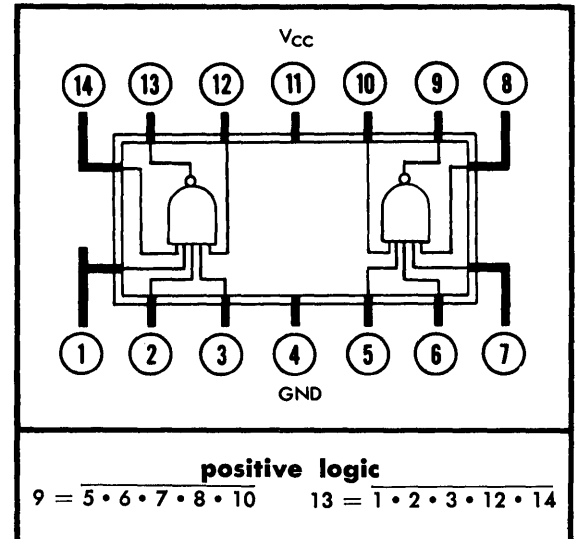
# TYPE SN5311

## DUAL 5-INPUT NAND/NOR GATE

### schematic (each gate)



Component values shown are nominal



### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	3 V to 4 V
Maximum Fan-out From Each Output Into Positive Loads, $N+$ . . . . .	10
Maximum Fan-out From Each Output Into Negative Loads, $N-$ . . . . .	10

### electrical characteristics (unless otherwise noted, $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$ , $V_{CC} = 3\text{ V}$ to $4\text{ V}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 0 (on level) at output	5	$V_{CC} = 3\text{ V}$	1.7		3	V
		$V_{CC} = 4\text{ V}$	2.5		4	V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 (off level) at output	7		0		0.3	V
$V_{out(1)}$ Logical 1 output voltage (off level)	7	$V_{CC} = 3\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = 10$ ( $I_{load} = -5\text{ mA}$ )	1.7		3	V
		$V_{CC} = 4\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = 10$ ( $I_{load} = -5\text{ mA}$ )	2.7		4	V
$V_{out(0)}$ Logical 0 output voltage (on level)	5	$V_{CC} = 3\text{ V}$ , $V_{in} = 1.7\text{ V}$ , $N- = 10$ ( $I_{sink} = 2.5\text{ mA}$ ), $T_A = -55^\circ\text{C}$	0		0.3	V
		$V_{CC} = 3\text{ V}$ , $V_{in} = 1.7\text{ V}$ , $N- = 10$ ( $I_{sink} = 1.9\text{ mA}$ ), $T_A = 125^\circ\text{C}$	0		0.3	V
$I_{in}$ Input current (each input)	7	$V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = -55^\circ\text{C}$			-0.25	mA
		$V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = 125^\circ\text{C}$			-0.19	mA
$I_{CC(on)}$ On level supply current (each gate)	9	$V_{CC} = V_{in} = 3\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		3.3		mA
		$V_{CC} = V_{in} = 4\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		4.5		mA
$I_{CC(off)}$ Off level supply current (each gate)	9	$V_{CC} = 3\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		1.2		mA
		$V_{CC} = 4\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		1.6		mA

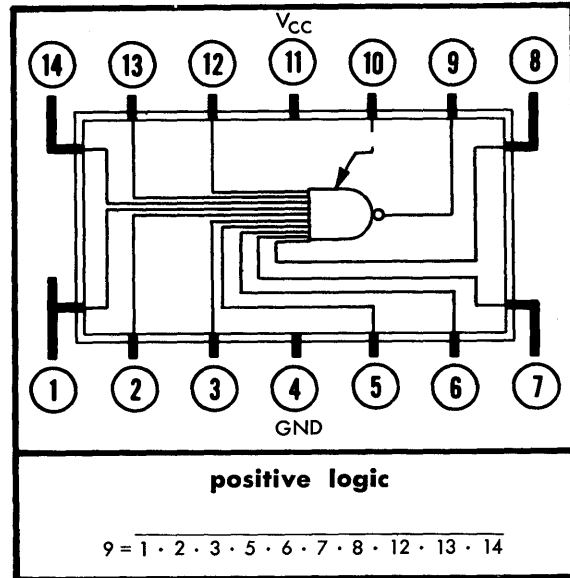
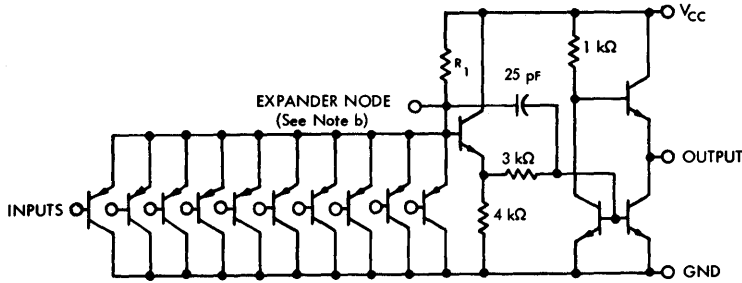
### switching characteristics, $T_A = 25^\circ\text{C}$ , $V_{CC} = 3.5\text{ V}$ , $N- = 1$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$ Delay Time	25	$Input: V_{in} = 2.5\text{ V}$ , $f = 1\text{ MHz}$ , $t_p = 500\text{ ns}$ , $t_r = t_f = 20\text{ ns}$	20	30	ns
$t_r$ Rise Time			25	45	ns
$t_s$ Storage Time			25	45	ns
$t_f$ Fall Time			25	40	ns
$t_{pd}$ Propagation Delay Time	26		25		ns

# TYPE SN5315

## 10-INPUT EXPANDABLE NAND/NOR GATE

### schematic



- NOTES: a. Component values shown are nominal.  
 b. Three SN5320 expanders may be fanned into one SN5315 to provide a total fan-in of 25. If expander is not used leave pin 10 open.

### recommended operating conditions

Supply Voltage $V_{CC}$	3 V to 4 V
Maximum Fan-out Into Positive Loads, $N+$	10
Maximum Fan-out Into Negative Loads, $N-$	10

### electrical characteristics (unless otherwise noted, $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$ , $V_{CC} = 3\text{ V}$ to $4\text{ V}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 0 (on level) at output	5	$V_{CC} = 3\text{ V}$	1.7		3	V
		$V_{CC} = 4\text{ V}$	2.5		4	V
$V_{in(1)X}$ Input voltage required at expander node (pin 10) to ensure logical 0 (on level) at output	6	$V_{CC} = 3\text{ V}, T_A = -55^\circ\text{C}$	2.35		3	V
		$V_{CC} = 3\text{ V}, T_A = 125^\circ\text{C}$	1.9		3	V
		$V_{CC} = 4\text{ V}, T_A = -55^\circ\text{C}$	3.15		4	V
		$V_{CC} = 4\text{ V}, T_A = 125^\circ\text{C}$	2.7		4	V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 (off level) at output	7		0		0.3	V
$V_{in(0)X}$ Input voltage required at expander node pin (pin 10) to ensure logical 1 (off level) at output	8	$T_A = -55^\circ\text{C}$	0		1.5	V
		$T_A = 125^\circ\text{C}$	0		0.95	V

# TYPE SN5315

## 10-INPUT EXPANDABLE NAND/NOR GATE

### electrical characteristics (continued)

(unless otherwise noted,  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 3\text{ V}$  to  $4\text{ V}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{out(1)}$ Logical 1 output voltage (off level)	7	$V_{CC} = 3\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = 10$ ( $I_{load} = -5\text{ mA}$ )	1.7		3	V
		$V_{CC} = 4\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = 10$ ( $I_{load} = -5\text{ mA}$ )	2.7		4	V
$V_{out(0)}$ Logical 0 output voltage (on level)	5	$V_{CC} = 3\text{ V}$ , $V_{in} = 1.7\text{ V}$ , $N- = 10$ ( $I_{sink} = 2.5\text{ mA}$ ), $T_A = -55^\circ\text{C}$	0		0.3	V
		$V_{CC} = 3\text{ V}$ , $V_{in} = 1.7\text{ V}$ , $N- = 10$ ( $I_{sink} = 1.9\text{ mA}$ ), $T_A = 125^\circ\text{C}$	0		0.3	V
$I_{in}$ Input current (each input)	7	$V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = -55^\circ\text{C}$			-0.25	mA
		$V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = 125^\circ\text{C}$			-0.19	mA
$I_{CC(on)}$ On level supply current	9	$V_{CC} = V_{in} = 3\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		3.3		mA
		$V_{CC} = V_{in} = 4\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		4.5		mA
$I_{CC(off)}$ Off level supply current	9	$V_{CC} = 3\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		1.2		mA
		$V_{CC} = 4\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		1.6		mA
$R_1$ Resistance value of $R_1$	10	$T_A = -55^\circ\text{C}$	1.24		2.6	k $\Omega$
		$T_A = 125^\circ\text{C}$	1.7		3.25	k $\Omega$

### switching characteristics, $T_A = 25^\circ\text{C}$ , $V_{CC} = 3.5\text{ V}$ , $N- = 1$

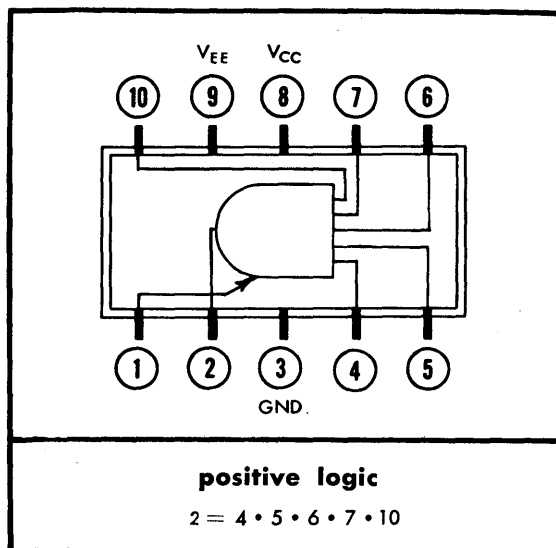
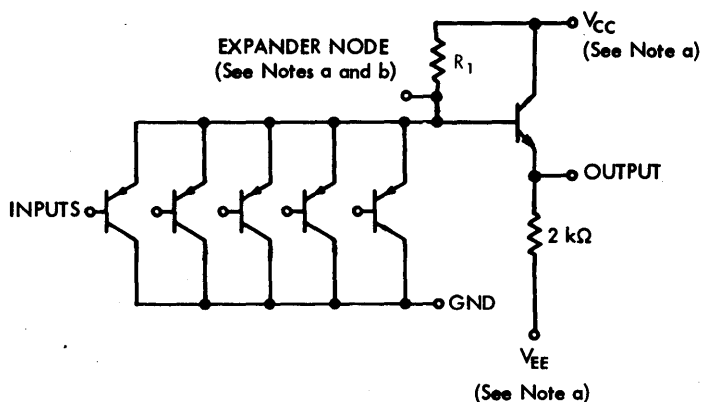
PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$ Delay Time	25	<i>Input:</i> $V_{in} = 2.5\text{ V}$ , $f = 1\text{ MHz}$ , $t_p = 500\text{ ns}$ , $t_r = t_f = 20\text{ ns}$	35	45	ns
$t_r$ Rise Time			40	50	ns
$t_s$ Storage Time			25	45	ns
$t_f$ Full Time			30	40	ns
$t_{pd}$ Propagation Delay Time	26		30		ns

# TYPE SN5320

## 5-INPUT EXPANDABLE AND/OR GATE

ALSO USABLE AS 5-INPUT EXPANDER

### schematic



- NOTES: a. When used as an expander for the SN5310, SN5315 or another SN5320, leave  $V_{CC}$  and  $V_{EE}$  terminals open.  
 b. Three expanders may be fanned into one SN5315 or 4 expanders may be fanned into one SN5310 or SN5320 to provide a total fan-in of 25.  
 c. Component values shown are nominal.

### recommended operating conditions

Supply Voltage $V_{CC}$	3 V to 4 V
Supply Voltage $V_{EE}$	-3 V
Maximum Fan-out Into Positive Loads, $N^+$	4
Maximum Fan-out Into Negative Loads, $N^-$	4

NOTE: For cascading capabilities see design characteristics, page 2.

### electrical characteristics

(unless otherwise noted,  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 3\text{ V}$  to  $4\text{ V}$ ,  $V_{EE} = -3\text{ V}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure off level at output	11	$V_{CC} = 3\text{ V}$	1.7		3	V
		$V_{CC} = 4\text{ V}$	2.5		4	V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 0 (on level) at output	12		0		0.3	V
$V_{out(0)}$ Logical 0 output voltage (on level)	12	$V_{CC} = 3\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N^- = 4$ ( $I_{sink} = 1\text{ mA}$ ), $T_A = -55^\circ\text{C}$	0		0.3	V
		$V_{CC} = 3\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N^- = 4$ ( $I_{sink} = 0.76\text{ mA}$ ), $T_A = 125^\circ\text{C}$	0		0.3	V
$V_{out(0)X}$ Expander node output voltage (off level) with logical 0 at any input	13	$V_{CC} = 4\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $T_A = -55^\circ\text{C}$			1.5	V
		$V_{CC} = 4\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $T_A = 125^\circ\text{C}$			0.95	V
$V_{out(1)X}$ Expander node output voltage (on level) with logical 1 at all inputs	14	$V_{CC} = 3\text{ V}$ , $V_{in} = 1.7\text{ V}$ , $T_A = -55^\circ\text{C}$	2.35			V
		$V_{CC} = 3\text{ V}$ , $V_{in} = 1.7\text{ V}$ , $T_A = 125^\circ\text{C}$	1.9			V
		$V_{CC} = 4\text{ V}$ , $V_{in} = 2.5\text{ V}$ , $T_A = -55^\circ\text{C}$	3.15			V
		$V_{CC} = 4\text{ V}$ , $V_{in} = 2.5\text{ V}$ , $T_A = 125^\circ\text{C}$	2.7			V

### CAUTION:

This device was formerly TYPE SN532. Pin numbers of the SN5320 have been renumbered in accordance with TO-89. The electrical functions of the SN532 and the SN5320 are in the same physical location. See pin identification, page 2004, for SN532 pin numbers.

# TYPE SN5320

## 5-INPUT EXPANDABLE AND/OR GATE

### electrical characteristics, continued

(unless otherwise noted,  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 3\text{ V}$  to  $4\text{ V}$ ,  $V_{EE} = -3\text{ V}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{(1)}$ Voltage difference from input to output when logical 1 level is applied to all inputs	11	$V_{CC} = 3\text{ V}$ , $V_{in} = 1.7\text{ V}$ , $N+ = 4$ ( $I_{load} = -2\text{ mA}$ )			0.4	V
		$V_{CC} = 4\text{ V}$ , $V_{in} = 2.5\text{ V}$ , $N+ = 4$ ( $I_{load} = -2\text{ mA}$ )			0.4	V
$I_{in}$ Input current (each input)	12	$V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = -55^\circ\text{C}$			-0.25	mA
		$V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = 125^\circ\text{C}$			-0.19	mA
$I_{CC(on)}$ On level $V_{CC}$ supply current (each gate)	15	$V_{CC} = 3\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		2.60		mA
		$V_{CC} = 4\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		3.1		mA
$I_{EE(on)}$ On level $V_{EE}$ supply current (each gate)	15	$V_{CC} = 3\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		1.7		mA
		$V_{CC} = 4\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		1.7		mA
$I_{CC(off)}$ Off level $V_{CC}$ supply current (each gate)	15	$V_{CC} = V_{in} = 3\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		2.6		mA
		$V_{CC} = V_{in} = 4\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		3.05		mA
$I_{EE(off)}$ Off level $V_{EE}$ supply current (each gate)	15	$V_{CC} = V_{in} = 3\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		2.6		mA
		$V_{CC} = V_{in} = 4\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		3.05		mA
$R_1$ Resistance value of $R_1$	15	$T_A = -55^\circ\text{C}$	1.24		2.6	k $\Omega$
		$T_A = 125^\circ\text{C}$	1.7		3.25	k $\Omega$

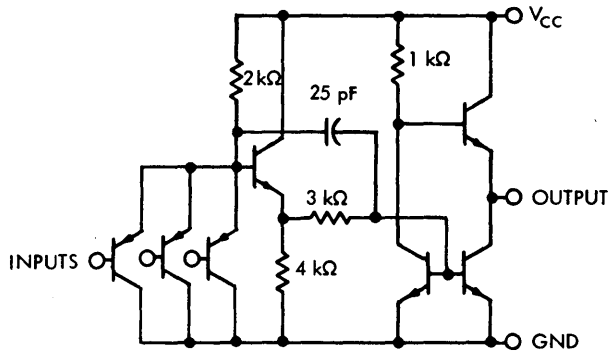
### switching characteristics, $T_A = 25^\circ\text{C}$ , $V_{CC} = 3.5\text{ V}$ , $V_{EE} = -3\text{ V}$ , $N- = 1$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_{d1}$ Delay Time 1	27	<i>Input:</i> $V_{in} = 2.5\text{ V}$ , $f = 1\text{ MHz}$ , $t_p = 500\text{ ns}$ , $t_r = t_f = 20\text{ ns}$	5	10	ns
$t_r$ Rise Time			40	200	ns
$t_{d2}$ Delay Time 2			5	10	ns
$t_f$ Fall Time			75	100	ns
$t_{pd}$ Propagation Delay Time	26		5		ns

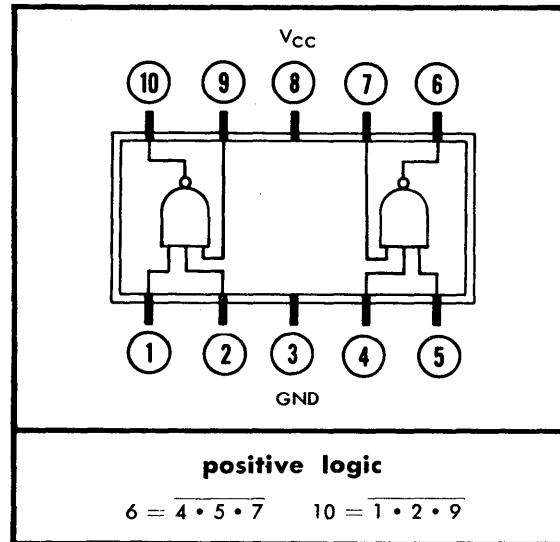


DUAL 3-INPUT NAND/NOR GATE

schematic (each gate)



Component values shown are nominal



recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	3 V to 4 V
Maximum Fan-out From Each Output Into Positive Loads, $N+$ . . . . .	10
Maximum Fan-out From Each Output Into Negative Loads, $N-$ . . . . .	10

electrical characteristics (unless otherwise noted,  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 3\text{ V}$  to  $4\text{ V}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals that will ensure logical 0 (on level) at output	5	$V_{CC} = 3\text{ V}$	1.7		3	V
		$V_{CC} = 4\text{ V}$	2.5		4	V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal that will ensure logical 1 (off level) at output	7		0		0.3	V
$V_{out(1)}$ Logical 1 output voltage (off level)	7	$V_{CC} = 3\text{ V}, V_{in} = 0.3\text{ V}, N+ = 10 (I_{load} = -5\text{ mA})$	1.7		3	V
		$V_{CC} = 4\text{ V}, V_{in} = 0.3\text{ V}, N+ = 10 (I_{load} = -5\text{ mA})$	2.7		4	V
$V_{out(0)}$ Logical 0 output voltage (on level)	5	$V_{CC} = 3\text{ V}, V_{in} = 1.7\text{ V}, N- = 10 (I_{sink} = 2.5\text{ mA}), T_A = -55^\circ\text{C}$	0		0.3	V
		$V_{CC} = 3\text{ V}, V_{in} = 1.7\text{ V}, N- = 10 (I_{sink} = 1.9\text{ mA}), T_A = 125^\circ\text{C}$	0		0.3	V
$I_{in}$ Input current (each input)	7	$V_{in} = 0.3\text{ V}, N+ = N- = 0, T_A = -55^\circ\text{C}$			-0.25	mA
		$V_{in} = 0.3\text{ V}, N+ = N- = 0, T_A = 125^\circ\text{C}$			-0.19	mA
$I_{CC(on)}$ On level supply current (each gate)	9	$V_{CC} = V_{in} = 3\text{ V}, N+ = N- = 0, T_A = 25^\circ\text{C}$		3.3		mA
		$V_{CC} = V_{in} = 4\text{ V}, N+ = N- = 0, T_A = 25^\circ\text{C}$		4.5		mA
$I_{CC(off)}$ Off level supply current (each gate)	9	$V_{CC} = 3\text{ V}, V_{in} = 0.3\text{ V}, N+ = N- = 0, T_A = 25^\circ\text{C}$		1.2		mA
		$V_{CC} = 4\text{ V}, V_{in} = 0.3\text{ V}, N+ = N- = 0, T_A = 25^\circ\text{C}$		1.6		mA

switching characteristics,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ V}$ ,  $N- = 1$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$ Delay Time	25	Input: $V_{in} = 2.5\text{ V}, f = 1\text{ MHz}, t_p = 500\text{ ns}, t_r = t_f = 20\text{ ns}$	20	30	ns
$t_r$ Rise Time			25	45	ns
$t_s$ Storage Time			25	45	ns
$t_f$ Fall Time			25	40	ns
$t_{pd}$ Propagation Delay Time	26		25		ns

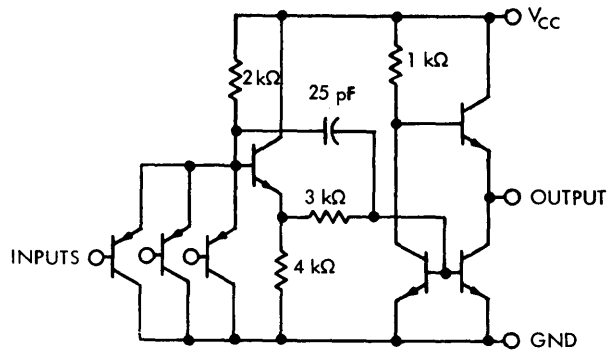
CAUTION:

This device was formerly TYPE SN533. Pin numbers of the SN5330 have been renumbered in accordance with TO-89. The electrical functions of the SN533 and the SN5330 are in the same physical location. See pin identification, page 2004, for SN533 pin numbers.

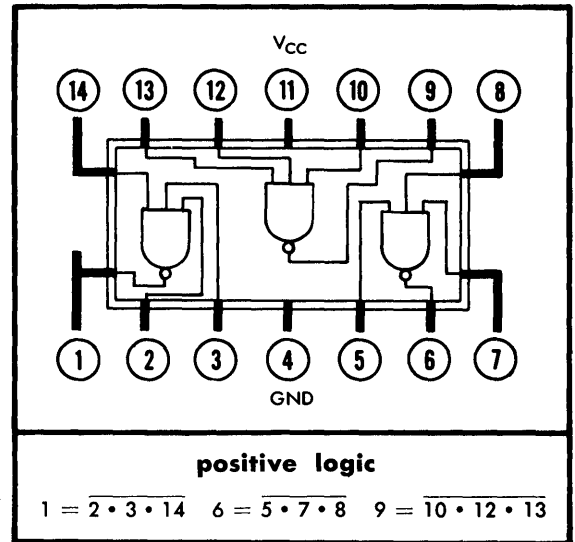
# TYPE SN5331

## TRIPLE 3-INPUT NAND/NOR GATE

schematic (each gate)



Component values shown are nominal.



### recommended operating conditions

Supply Voltage $V_{CC}$	3 V to 4 V
Maximum Fan-out From Each Output Into Positive Loads, $N+$	10
Maximum Fan-out From Each Output Into Negative Loads, $N-$	10

### electrical characteristics (unless otherwise noted, $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$ , $V_{CC} = 3\text{ V}$ to $4\text{ V}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 0 (on level) at output	5	$V_{CC} = 3\text{ V}$	1.7		3	V
		$V_{CC} = 4\text{ V}$	2.5		4	V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 (off level) at output	7		0		0.3	V
$V_{out(1)}$ Logical 1 output voltage (off level)	7	$V_{CC} = 3\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = 10$ ( $I_{load} = -5\text{ mA}$ )	1.7		3	V
		$V_{CC} = 4\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = 10$ ( $I_{load} = -5\text{ mA}$ )	2.7		4	V
$V_{out(0)}$ Logical 0 output voltage (on level)	5	$V_{CC} = 3\text{ V}$ , $V_{in} = 1.7\text{ V}$ , $N- = 10$ ( $I_{sink} = 2.5\text{ mA}$ ), $T_A = -55^\circ\text{C}$	0		0.3	V
		$V_{CC} = 3\text{ V}$ , $V_{in} = 1.7\text{ V}$ , $N- = 10$ ( $I_{sink} = 1.9\text{ mA}$ ), $T_A = 125^\circ\text{C}$	0		0.3	V
$I_{in}$ Input current (each input)	7	$V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = -55^\circ\text{C}$			-0.25	mA
		$V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = 125^\circ\text{C}$			-0.19	mA
$I_{CC(on)}$ On level supply current (each gate)	9	$V_{CC} = V_{in} = 3\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		3.3		mA
		$V_{CC} = V_{in} = 4\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		4.5		mA
$I_{CC(off)}$ Off level supply current (each gate)	9	$V_{CC} = 3\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		1.2		mA
		$V_{CC} = 4\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		1.6		mA

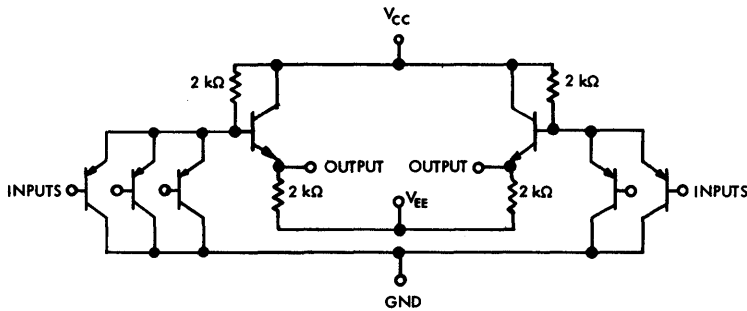
### switching characteristics, $T_A = 25^\circ\text{C}$ , $V_{CC} = 3.5\text{ V}$ , $N- = 1$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$ Delay Time	25	$Input: V_{in} = 2.5\text{ V}$ , $f = 1\text{ MHz}$ , $t_p = 500\text{ ns}$ , $t_r = t_f = 20\text{ ns}$	20	30	ns
$t_r$ Rise Time			25	45	ns
$t_s$ Storage Time			25	45	ns
$t_f$ Fall Time			25	40	ns
$t_{pd}$ Propagation Delay Time	26		25		ns

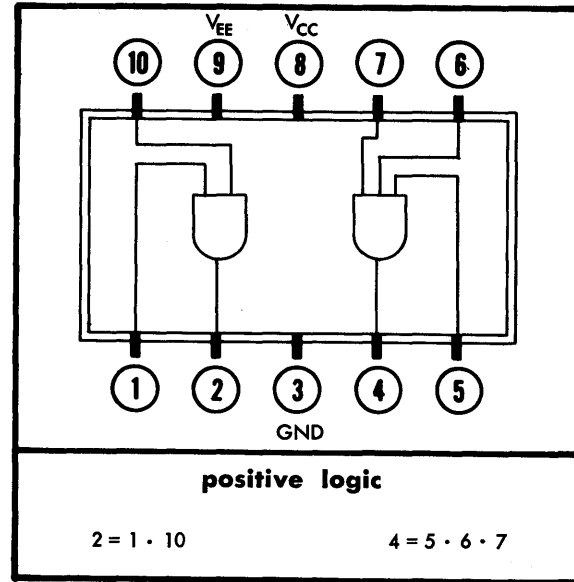
# TYPE SN5340

## DUAL AND/OR GATE

### schematic



- NOTES: a. Component values shown are nominal.  
 b. Do not connect pins (2) and (4) together.



### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	3 V to 4 V
Supply Voltage $V_{EE}$ . . . . .	-3 V
Maximum Fan-out From Each Output Into Positive Loads, $N^+$ . . . . .	4
Maximum Fan-out From Each Output Into Negative Loads, $N^-$ . . . . .	4

NOTE: For cascading capabilities see design characteristics, page 2.

### electrical characteristics

(unless otherwise noted,  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 3\text{ V}$  to  $4\text{ V}$ ,  $V_{EE} = -3\text{ V}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 1 (off level) at output	11	$V_{CC} = 3\text{ V}$	1.7	3	V
		$V_{CC} = 4\text{ V}$	2.5	4	V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 0 (on level) at output	12		0	0.3	V
$\Delta V_{(1)}$ Voltage difference from input to output when logical 1 level is applied to all inputs	11	$V_{CC} = 3\text{ V}$ , $V_{in} = 1.7\text{ V}$ , $N^+ = 4$ ( $I_{load} = -2\text{ mA}$ )		0.4	V
		$V_{CC} = 4\text{ V}$ , $V_{in} = 2.5\text{ V}$ , $N^+ = 4$ ( $I_{load} = -2\text{ mA}$ )		0.4	V
$V_{out(0)}$ Logical 0 output voltage (on level)	12	$V_{CC} = 3\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N^- = 4$ ( $I_{sink} = 1\text{ mA}$ ), $T_A = -55^\circ\text{C}$	0	0.3	V
		$V_{CC} = 3\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N^- = 4$ ( $I_{sink} = 0.76\text{ mA}$ ), $T_A = 125^\circ\text{C}$	0	0.3	V

### CAUTION:

This device was formerly TYPE SN534. Pin numbers of the SN5340 have been renumbered in accordance with TO-89. The electrical functions of the SN534 and the SN5340 are in the same physical location. See pin identification, page 2004, for SN534 pin numbers.

# TYPE SN5340 DUAL AND/OR GATE

## electrical characteristics, continued

(unless otherwise noted  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 3\text{ V}$  to  $4\text{ V}$ ,  $V_{EE} = -3\text{ V}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in}$ Input current (each input)	12	$V_{in} = 0.3\text{ V}, N+ = N- = 0, T_A = -55^\circ\text{C}$		-0.25		mA
		$V_{in} = 0.3\text{ V}, N+ = N- = 0, T_A = 125^\circ\text{C}$		-0.19		mA
$I_{CC(on)}$ On level $V_{CC}$ supply current (each gate)	15	$V_{CC} = 3\text{ V}, V_{in} = 0.3\text{ V}, N+ = N- = 0, T_A = 25^\circ\text{C}$		2.6		mA
		$V_{CC} = 4\text{ V}, V_{in} = 0.3\text{ V}, N+ = N- = 0, T_A = 25^\circ\text{C}$		3.1		mA
$I_{EE(on)}$ On level $V_{EE}$ supply current (each gate)	15	$V_{CC} = 3\text{ V}, V_{in} = 0.3\text{ V}, N+ = N- = 0, T_A = 25^\circ\text{C}$		1.7		mA
		$V_{CC} = 4\text{ V}, V_{in} = 0.3\text{ V}, N+ = N- = 0, T_A = 25^\circ\text{C}$		1.7		mA
$I_{CC(off)}$ Off level $V_{CC}$ supply current (each gate)	15	$V_{CC} = V_{in} = 3\text{ V}, N+ = N- = 0, T_A = 25^\circ\text{C}$		2.6		mA
		$V_{CC} = V_{in} = 4\text{ V}, N+ = N- = 0, T_A = 25^\circ\text{C}$		3.05		mA
$I_{EE(off)}$ Off level $V_{EE}$ supply current (each gate)	15	$V_{CC} = V_{in} = 3\text{ V}, N+ = N- = 0, T_A = 25^\circ\text{C}$		2.6		mA
		$V_{CC} = V_{in} = 4\text{ V}, N+ = N- = 0, T_A = 25^\circ\text{C}$		3.05		mA

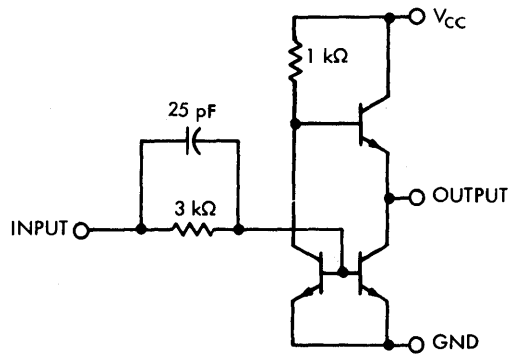
## switching characteristics, $T_A = 25^\circ\text{C}$ , $V_{CC} = 3.5\text{ V}$ , $N- = 1$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_{d1}$ Delay Time 1	27	<i>Input:</i> $V_{in} = 2.5\text{ V}, f = 1\text{ MHz}, t_p = 500\text{ ns}, t_r = t_f = 20\text{ ns}$	5	10	ns
$t_r$ Rise Time			40	200	ns
$t_{d2}$ Delay Time 2			5	10	ns
$t_f$ Fall Time			75	100	ns
$t_{pd}$ Propagation Delay Time	26		5		ns

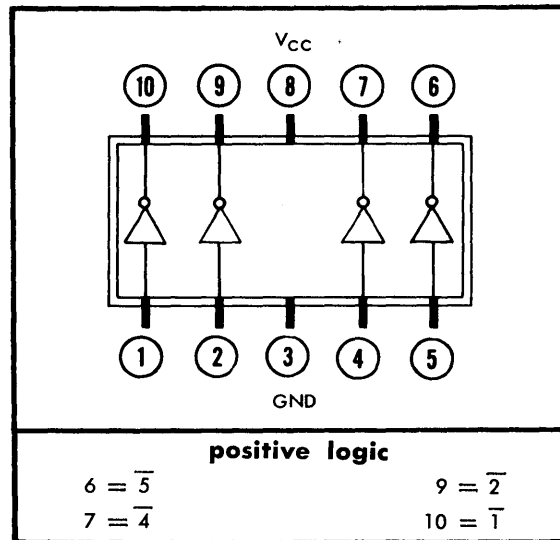
# TYPE SN5350

## QUADRUPLE INVERTER/DRIVER

schematic (each inverter)



Component values shown are nominal



### recommended operating conditions

Supply Voltage $V_{CC}$	3 V to 4 V
Maximum Fan-out From Each Output Into Positive Loads, $N+$	10
Maximum Fan-out From Each Output Into Negative Loads, $N-$	10

electrical characteristics (unless otherwise noted,  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 3\text{ V}$  to  $4\text{ V}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required to ensure logical 0 (on level) at output	16	$V_{CC} = 3\text{ V}$	1.5		3	V
		$V_{CC} = 4\text{ V}$	1.5		4	V
$V_{in(0)}$ Logical 0 input voltage required to ensure logical 1 (off level) at output	16		0		0.3	V
$V_{out(1)}$ Logical 1 output voltage (off level)	16	$V_{CC} = 3\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = 10$ ( $I_{load} = -5\text{ mA}$ )	1.7		3	V
		$V_{CC} = 4\text{ V}$ , $V_{in} = 0.3\text{ V}$ , $N+ = 10$ ( $I_{load} = -5\text{ mA}$ )	2.7		4	V
$V_{out(0)}$ Logical 0 output voltage (on level)	16	$V_{CC} = 3\text{ V}$ , $V_{in} = 1.7\text{ V}$ , $N- = 10$ ( $I_{sink} = 2.5\text{ mA}$ ), $T_A = -55^\circ\text{C}$	0		0.3	V
		$V_{CC} = 3\text{ V}$ , $V_{in} = 1.7\text{ V}$ , $N- = 10$ ( $I_{sink} = 1.9\text{ mA}$ ), $T_A = 125^\circ\text{C}$	0		0.3	V
$I_{in}$ Input current	16	$V_{CC} = 4\text{ V}$ , $V_{in} = 2.7\text{ V}$ , $N+ = N- = 0$			1	mA
$I_{CC(on)}$ On level supply current (each inverter)	16	$V_{CC} = V_{in} = 3\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		3.3		mA
		$V_{CC} = V_{in} = 4\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		4.5		mA

switching characteristics,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ V}$ ,  $N- = 1$

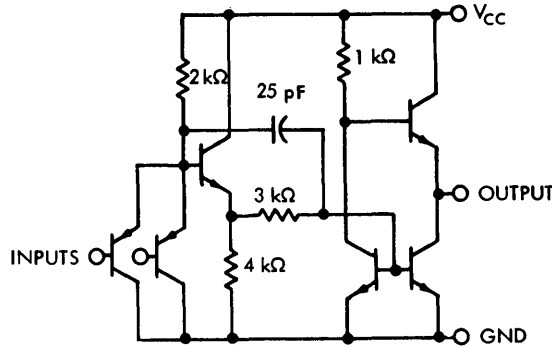
PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$ Delay Time	25	Input: $V_{in} = 2.5\text{ V}$ , $f = 1\text{ MHz}$ , $t_p = 500\text{ ns}$ , $t_r = t_f = 20\text{ ns}$	20	30	ns
$t_r$ Rise Time			25	45	ns
$t_s$ Storage Time			25	45	ns
$t_f$ Fall Time			25	40	ns
$t_{pd}$ Propagation Delay Time	26		25		ns

### CAUTION:

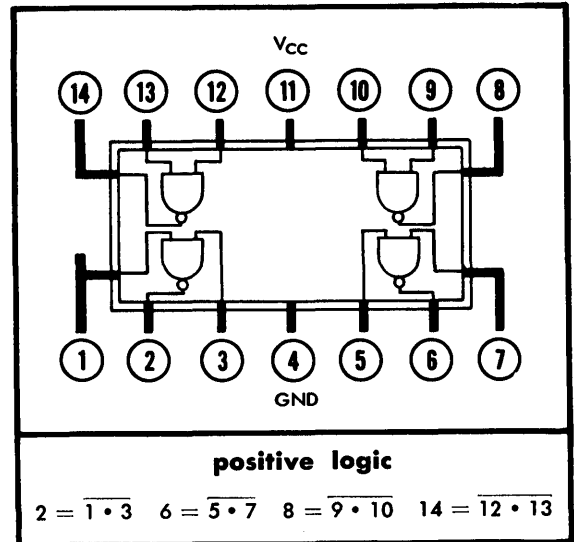
This device was formerly TYPE SN535. Pin numbers of the SN5350 have been renumbered in accordance with TO-89. The electrical functions of the SN535 and the SN5350 are in the same physical location. See pin identification, page 2004, for SN535 pin numbers.

# TYPE SN5360 QUADRUPLE 2-INPUT NAND/NOR GATE

schematic (each gate)



Component values shown are nominal



**recommended operating conditions**

- Supply Voltage  $V_{CC}$  . . . . . 3 V to 4 V
- Maximum Fan-out From Each Output Into Positive Loads,  $N+$  . . . . . 10
- Maximum Fan-out From Each Output Into Negative Loads,  $N-$  . . . . . 10

**electrical characteristics (unless otherwise noted,  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{CC} = 3 \text{ V}$  to  $4 \text{ V}$ )**

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 0 (on level) at output	5	$V_{CC} = 3 \text{ V}$	1.7		3	V
		$V_{CC} = 4 \text{ V}$	2.5		4	V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 (off level) at output	7		0		0.3	V
$V_{out(1)}$ Logical 1 output voltage (off level)	7	$V_{CC} = 3 \text{ V}, V_{in} = 0.3 \text{ V}, N+ = 10 (I_{load} = -5 \text{ mA})$	1.7		3	V
		$V_{CC} = 4 \text{ V}, V_{in} = 0.3 \text{ V}, N+ = 10 (I_{load} = -5 \text{ mA})$	2.7		4	V
$V_{out(0)}$ Logical 0 output voltage (on level)	5	$V_{CC} = 3 \text{ V}, V_{in} = 1.7 \text{ V}, N- = 10, (I_{sink} = 2.5 \text{ mA}), T_A = -55^\circ\text{C}$	0		0.3	V
		$V_{CC} = 3 \text{ V}, V_{in} = 1.7 \text{ V}, N- = 10, (I_{sink} = 1.9 \text{ mA}), T_A = -125^\circ\text{C}$	0		0.3	V
$I_{in}$ Input current (each input)	7	$V_{in} = 0.3 \text{ V}, N+ = N- = 0, T_A = -55^\circ\text{C}$			-0.25	mA
		$V_{in} = 0.3 \text{ V}, N+ = N- = 0, T_A = 125^\circ\text{C}$			-0.19	mA
$I_{CC(on)}$ On level supply current (each gate)	9	$V_{CC} = V_{in} = 3 \text{ V}, N+ = N- = 0, T_A = 25^\circ\text{C}$		3.3		mA
		$V_{CC} = V_{in} = 4 \text{ V}, N+ = N- = 0, T_A = 25^\circ\text{C}$		4.5		mA
$I_{CC(off)}$ Off level supply current (each gate)	9	$V_{CC} = 3 \text{ V}, V_{in} = 0.3 \text{ V}, N+ = N- = 0, T_A = 25^\circ\text{C}$		1.2		mA
		$V_{CC} = 4 \text{ V}, V_{in} = 0.3 \text{ V}, N+ = N- = 0, T_A = 25^\circ\text{C}$		1.6		mA

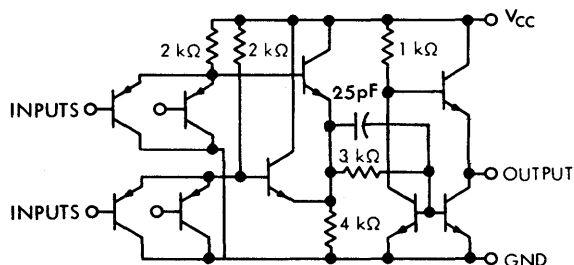
**switching characteristics,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.5 \text{ V}$ ,  $N- = 1$**

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_d$ Delay Time	25	Input: $V_{in} = 2.5 \text{ V}, f = 1 \text{ MHz}, t_p = 500 \text{ ns}, t_r = t_f = 20 \text{ ns}$		20	30	ns
$t_r$ Rise Time			25	45	ns	
$t_s$ Storage Time			25	45	ns	
$t_f$ Fall Time			25	40	ns	
$t_{pd}$ Propagation Delay Time	26			25		ns

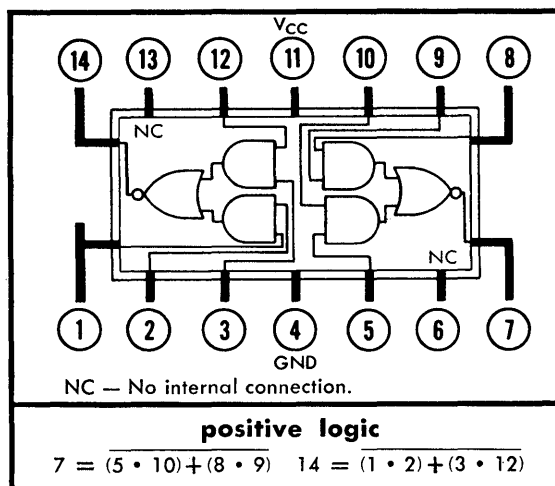
# TYPE SN5370

## DUAL EXCLUSIVE-OR GATE

schematic (each gate)



Component values shown are nominal



### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	3 V to 4 V
Maximum Fan-out From Each Output Into Positive Loads, $N+$ . . . . .	10
Maximum Fan-out From Each Output Into Negative Loads, $N-$ . . . . .	10

### electrical characteristics (unless otherwise noted, $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$ , $V_{CC} = 3\text{ V}$ to $4\text{ V}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 (on level) at output	17	$V_{CC} = 3\text{ V}$	1.7		3	V
		$V_{CC} = 4\text{ V}$	2.5		4	V
$V_{in(0)}$ Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 (off level) at output	18		0		0.3	V
$V_{out(1)}$ Logical 1 output voltage (off level)	18	$V_{CC} = 3\text{ V}$ , $N+ = 10$ ( $I_{load} = -5\text{ mA}$ ) $V_{in} = 0.3\text{ V}$ ,	1.7		3	V
		$V_{CC} = 4\text{ V}$ , $N+ = 10$ ( $I_{load} = -5\text{ mA}$ ) $V_{in} = 0.3\text{ V}$ ,	2.7		4	V
$V_{out(0)}$ Logical 0 output voltage (on level)	17	$V_{CC} = 3\text{ V}$ , $N- = 10$ ( $I_{sink} = 2.5\text{ mA}$ ), $V_{in} = 1.7\text{ V}$ , $T_A = -55^\circ\text{C}$	0		0.3	V
		$V_{CC} = 3\text{ V}$ , $N- = 10$ ( $I_{sink} = 1.9\text{ mA}$ ), $V_{in} = 1.7\text{ V}$ , $T_A = 125^\circ\text{C}$	0		0.3	V
$I_{in}$ Input current (each input)	18	$V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = -55^\circ\text{C}$			-0.25	mA
		$V_{in} = 0.3\text{ V}$ , $N+ = N- = 0$ , $T_A = 125^\circ\text{C}$			-0.19	mA
$I_{CC(on)}$ On level supply current (each gate)	17	$V_{CC} = V_{in} = 3\text{ V}$ , $T_A = 25^\circ\text{C}$ , $N+ = N- = 0$ ,		3.3		mA
		$V_{CC} = V_{in} = 4\text{ V}$ , $T_A = 25^\circ\text{C}$ , $N+ = N- = 0$ ,		4.5		mA
$I_{CC(off)}$ Off level supply current (each gate)	18	$V_{CC} = 3\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		1.2		mA
		$V_{CC} = 4\text{ V}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		1.6		mA

### switching characteristics, $T_A = 25^\circ\text{C}$ , $V_{CC} = 3.5\text{ V}$ , $N- = 1$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$ Delay Time	25	Input: $V_{in} = 2.5\text{ V}$ , $t_p = 500\text{ ns}$ , $f = 1\text{ MHz}$ , $t_r = t_f = 20\text{ ns}$	30	60	ns
$t_r$ Rise Time			30	60	ns
$t_s$ Storage Time			100	200	ns
$t_f$ Fall Time			100	200	ns
$t_{pd}$ Propagation Delay Time	26		65		ns

# TYPE SN5380

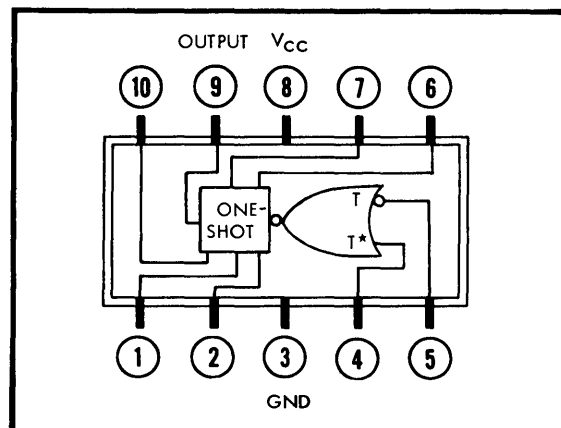
## ONE-SHOT MONOSTABLE MULTIVIBRATOR

logic

TRUTH TABLE

positive logic				
T		T*		OUTPUT
$t_n$	$t_{n+1}$	$t_n$	$t_{n+1}$	
1	1	..	..	INHIBITED (logical 1)
..	..	0	0	INHIBITED (logical 1)
0	0	1	0	ONE-SHOT (logical 0 for $t_{p\ ns}$ )
0	1	1	1	ONE-SHOT (logical 0 for $t_{p\ ns}$ )

$t_n$  = bit time before change in input levels  
 $t_{n+1}$  = bit time after change in input levels



### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	3 V to 4 V
Maximum Fan-out Into Positive Loads, $N+$ . . . . .	10
Maximum Fan-out Into Negative Loads, $N-$ . . . . .	10
Minimum Set-Up Time, $t_{set-up}^\dagger$ . . . . .	400 ns

### electrical characteristics (unless otherwise noted, $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$ , $V_{CC} = 3\text{ V}$ to $4\text{ V}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at T or T* input terminal	19	$V_{CC} = 3\text{ V}$	1.7		3	V
		$V_{CC} = 4\text{ V}$	2.5		4	V
$V_{in(0)}$ Input voltage required to ensure logical 0 at T or T* terminal	19		0		0.3	V
$V_{out(1)}$ Logical 1 output voltage (off level)	20	$V_{CC} = 3\text{ V}$ , $N+ = 10$ ( $I_{load} = -5\text{ mA}$ )	1.7		3	V
		$V_{CC} = 4\text{ V}$ , $N+ = 10$ ( $I_{load} = -5\text{ mA}$ )	2.7		4	V
$V_{out(0)}$ Logical 0 output voltage (on level)	20	$V_{CC} = 3\text{ V}$ , $V_{\odot} = 0.3\text{ V}$ , pin (10) open $N- = 10$ ( $I_{sink} = 2.5\text{ mA}$ ), $T_A = -55^\circ\text{C}$	0		0.3	V
		$V_{CC} = 4\text{ V}$ , $V_{\odot} = 0.3\text{ V}$ , pin (10) open $N- = 10$ ( $I_{sink} = 1.9\text{ mA}$ ), $T_A = 125^\circ\text{C}$	0		0.3	V
$I_{in}$ Input current (each input)	19	$V_{in} = 2.7\text{ V}$ , $N+ = N- = 0$			0.5	mA
$I_{CC(av)}$ Average supply current	21	$V_{CC} = 3\text{ V}$ , $N+ = N- = 0$ Duty cycle = 50%, $T_A = 25^\circ\text{C}$		4.8		mA
		$V_{CC} = 4\text{ V}$ , $N+ = N- = 0$ , Duty cycle = 50%, $T_A = 25^\circ\text{C}$		6.3		mA

$^\dagger$ This is the minimum time necessary for the input signal to dwell before the triggering transition begins and applies when pin (6) is shorted to pin (7) and pin (2) is shorted to pin (10). Set-up time begins only after the occurrence of the 10% point of the output fall time.

$^\ddagger$ Pin (6) shorted to pin (7) and pin (2) shorted to pin (10) unless otherwise noted.

#### CAUTION:

Pin numbers of the SN5380 have been renumbered in accordance with TO-89. The electrical functions are in the same physical location. See pin identification, page 2004, for former pin numbers.



# TYPE SN5380

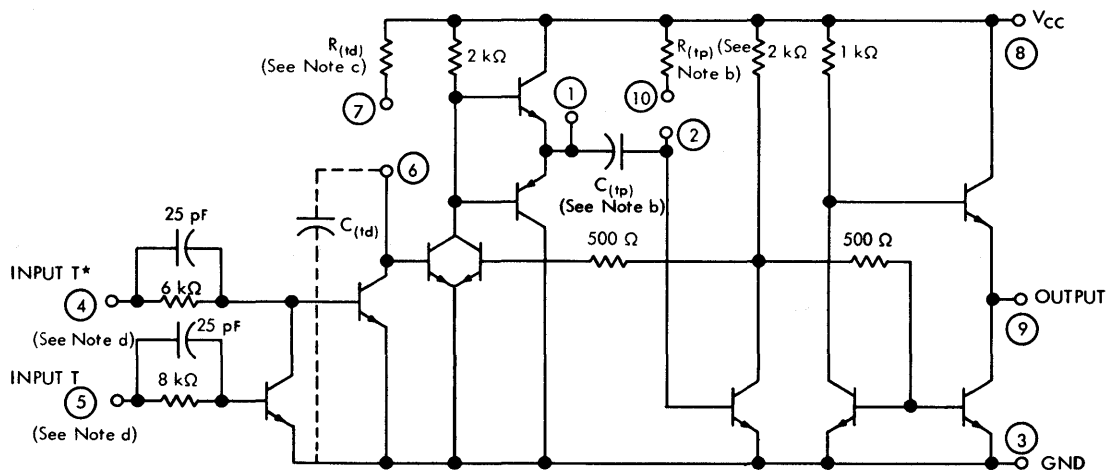
## ONE-SHOT MONOSTABLE MULTIVIBRATOR

switching times,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ V}$ , fan-out  $N = 1$

PARAMETER	TEST FIGURE	TEST CONDITIONS <sup>‡</sup>	MIN	TYP	MAX	UNIT
$t_{d1}$ Delay Time after Positive-going Transition at T (pin ⑤)	28	Input: $V_{in} = 2.5\text{ V}$ , $f = 1\text{ MHz}$ , $t_p = 400\text{ ns}$ , $t_r = t_f = 20\text{ ns}$		90	130	ns
$t_{d2}$ Delay Time after Negative-going Transition at T* (pin ④)				90	130	ns
$t_r$ Rise Time				35	60	ns
$t_f$ Fall Time				35	60	ns
$t_p$ Output Pulse Width	28	Input: $V_{in} = 2.5\text{ V}$ , $f = 1\text{ MHz}$ , $t_p = 400\text{ ns}$ , $t_r = t_f = 20\text{ ns}$	100	250	400	ns

<sup>‡</sup>Pin ⑥ shorted to pin ⑦ and pin ② shorted to pin ⑩ unless otherwise noted.

### schematic



NOTES: a. Component values shown are nominal.

b. Output pulse width  $t_p$  is proportional to  $R_{(tp)} C_{(tp)}$ . Output pulse width may be modified using pins ①, ②, ⑧, and ⑩ to change effective values of  $R_{(tp)}$  and  $C_{(tp)}$ . Nominal value of internal  $R_{(tp)}$  is 8 kΩ and  $C_{(tp)}$  is 25 pF. Value of modified  $R_{(tp)}$  should be maintained between 6 kΩ and 15 kΩ.

#### CAUTION:

When the effective value of  $C_{(tp)} \geq 0.1\ \mu\text{F}$ , a 560-Ω resistor must be connected in series with the external portion of  $C_{(tp)}$  (between pins ① and ②).

c. Delay time ( $t_d$ ) may be modified using pins ③, ⑥, ⑦, and ⑧ to change effective values of  $R_{(td)}$  and  $C_{(td)}$ . Nominal value of internal  $R_{(td)}$  is 2 kΩ. Value of modified  $R_{(td)}$  should be maintained between 2 kΩ and 10 kΩ.

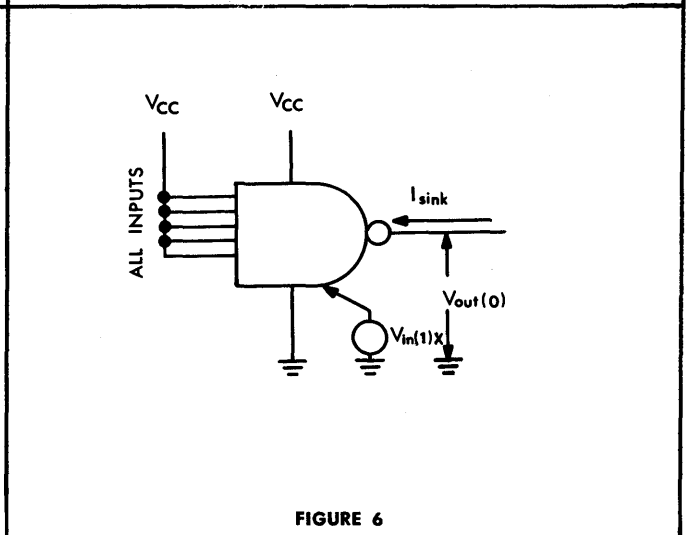
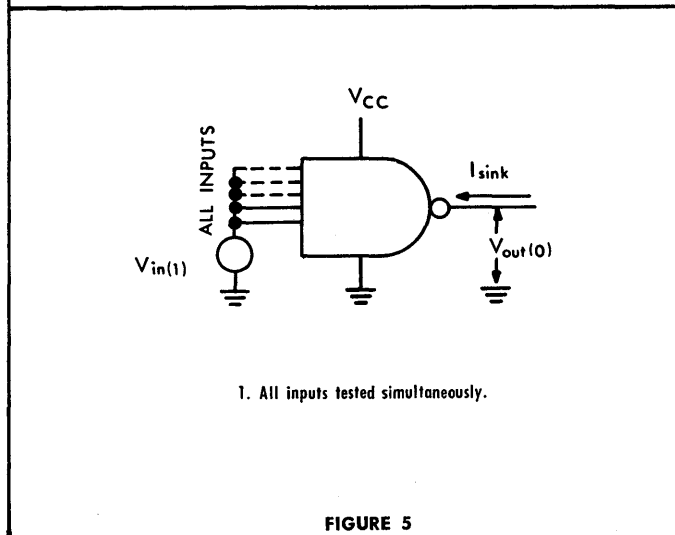
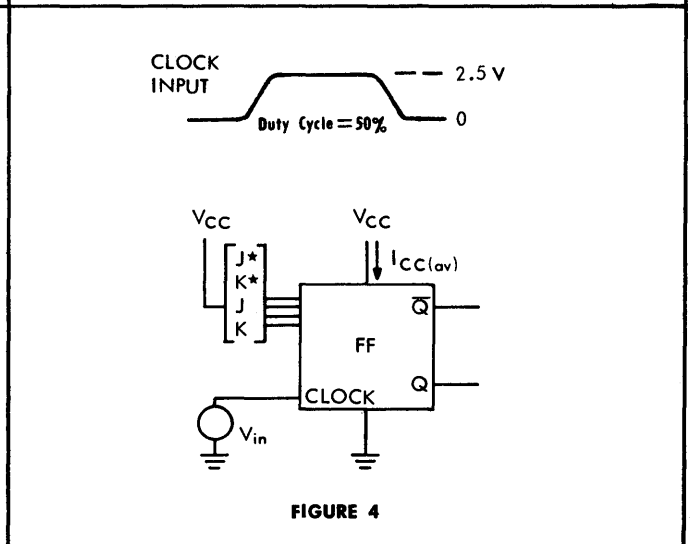
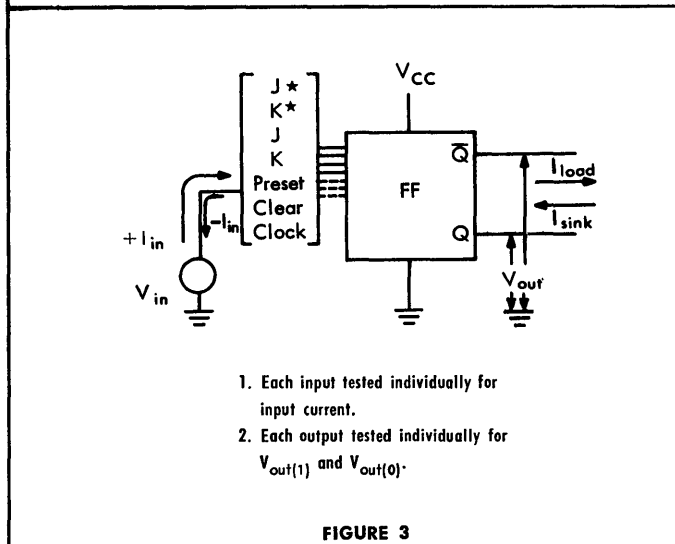
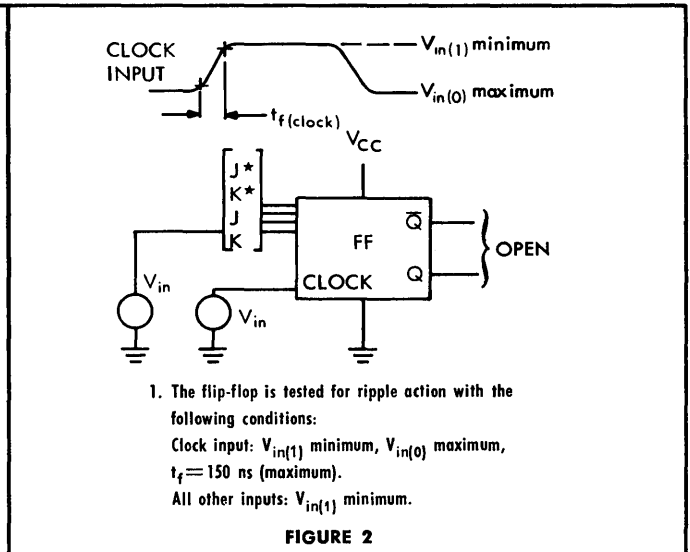
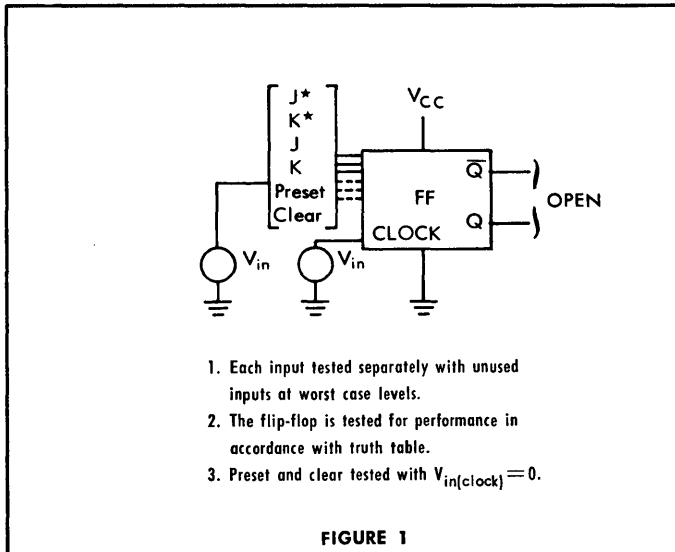
d. T triggers on a positive transition to logical 1 level, and T\* triggers on a negative transition to logical 0 level. When triggering with T input, hold T\* at logical 1. When triggering with T\* input, hold T at logical 0.

#### CAUTION:

Pin numbers of the SN5380 have been renumbered in accordance with TO-89. The electrical functions are in the same physical location. See pin identification, page 2004, for former pin numbers.

**PARAMETER MEASUREMENT INFORMATION**

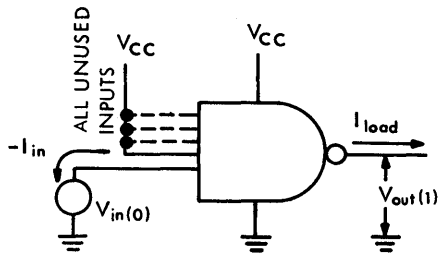
**d-c test circuits †**



†Arrows indicate actual direction of current flow.

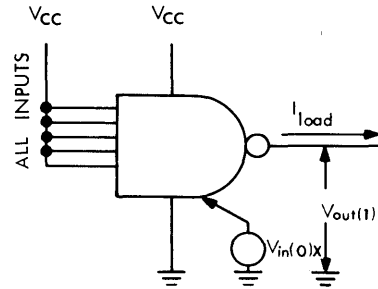
**PARAMETER MEASUREMENT INFORMATION**

**d-c test circuits†(continued)**

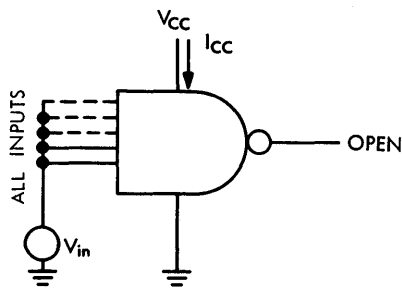


1. Each input tested separately.

**FIGURE 7**

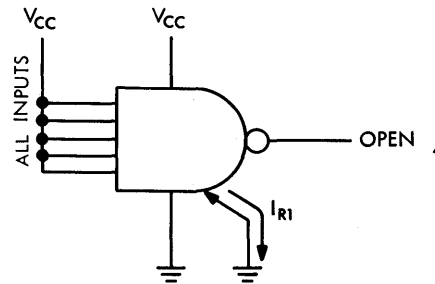


**FIGURE 8**



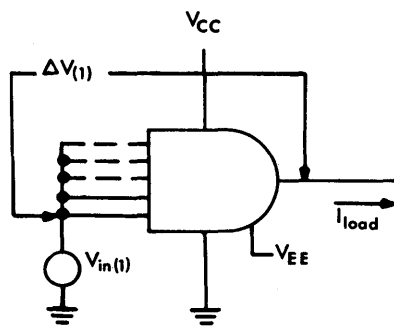
1. Test on-level and off-level currents.

**FIGURE 9**



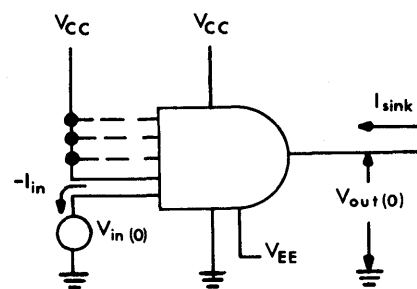
$$1. R_1 = \frac{V_{CC}}{I_{R1}}$$

**FIGURE 10**



1. All inputs tested simultaneously.  
 2. SN5320 expander node is open.

**FIGURE 11**



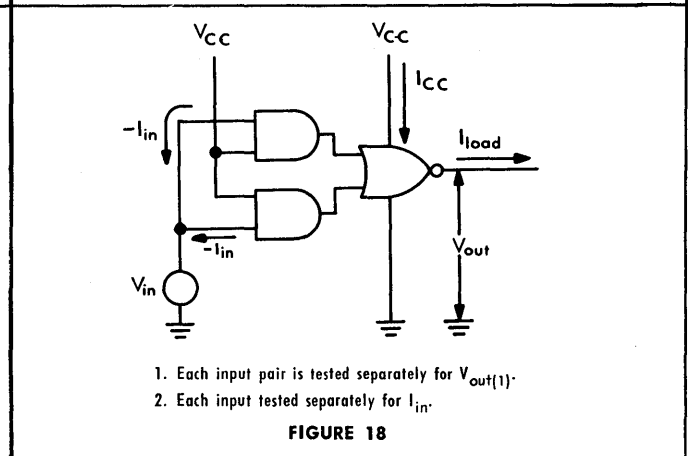
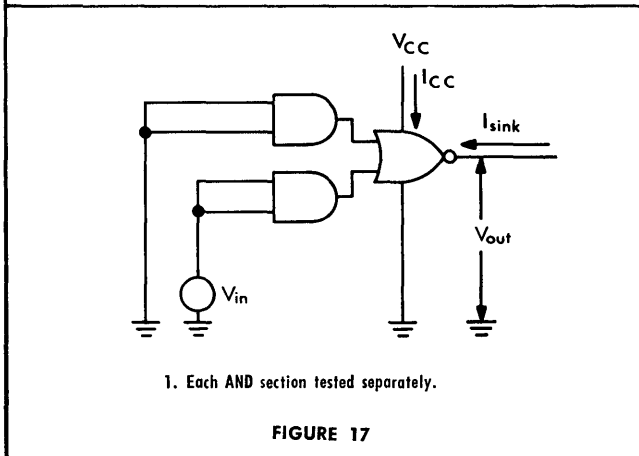
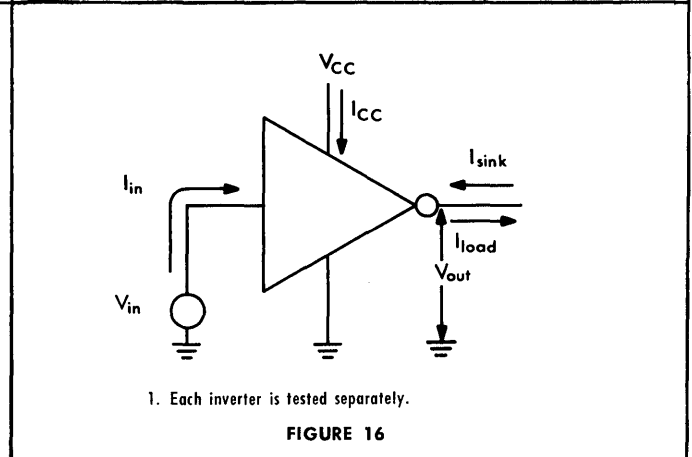
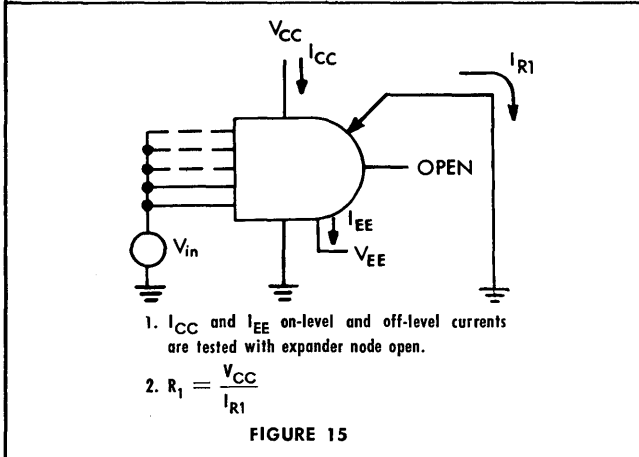
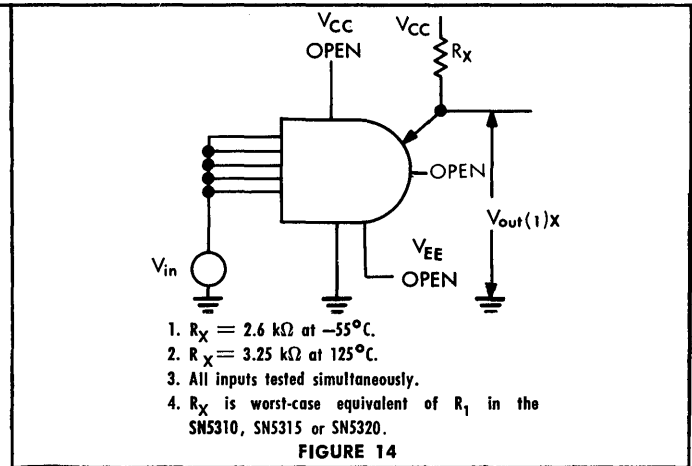
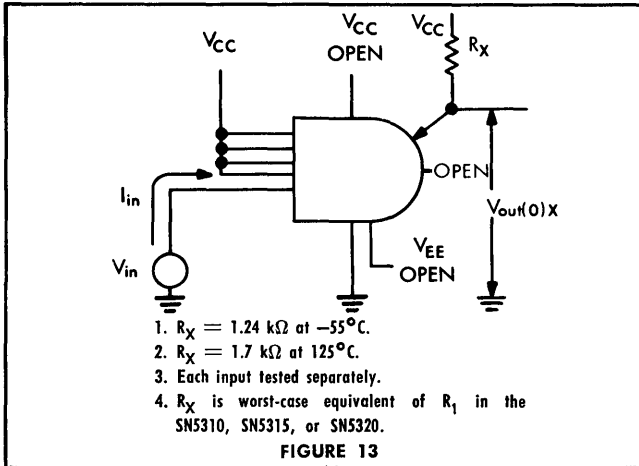
1. Each input tested separately.  
 2. SN5320 expander node is open.

**FIGURE 12**

† Arrows indicate actual direction of current flow

**PARAMETER MEASUREMENT INFORMATION**

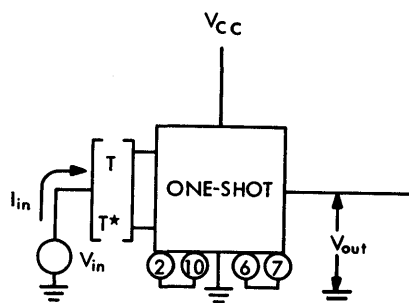
**d-c test circuits†(continued)**



† Arrows indicate actual direction of current flow

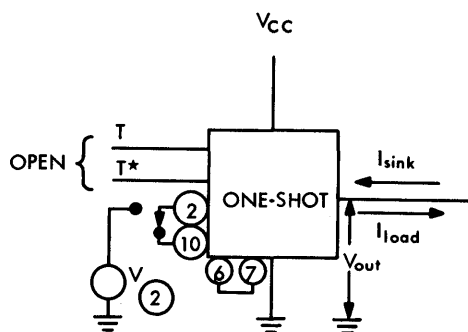
**PARAMETER MEASUREMENT INFORMATION**

**d-c test circuits†(continued)**

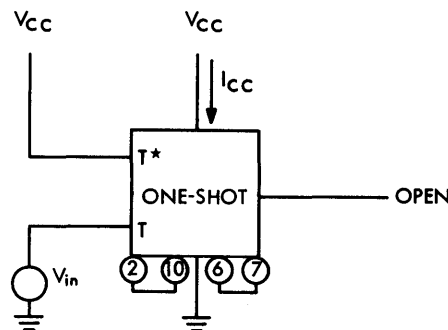


1. Each input tested separately.
2. With minimum  $V_{in(1)}$  and maximum  $V_{in(0)}$ , and the unused input at the worst-case level, the one-shot output is verified.

**FIGURE 19**



**FIGURE 20**



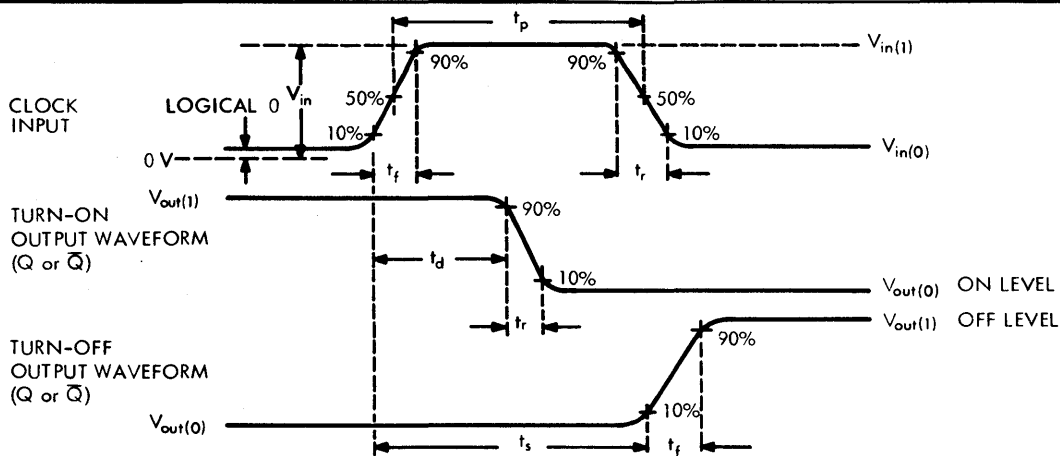
1.  $I_{CC}$  is measured with a 50% duty cycle.

**FIGURE 21**

**CAUTION:**

Pin numbers of the SN5380 have been renumbered in accordance with TO-89. The electrical functions are in the same physical location. See pin identification, page 2004, for former pin numbers.

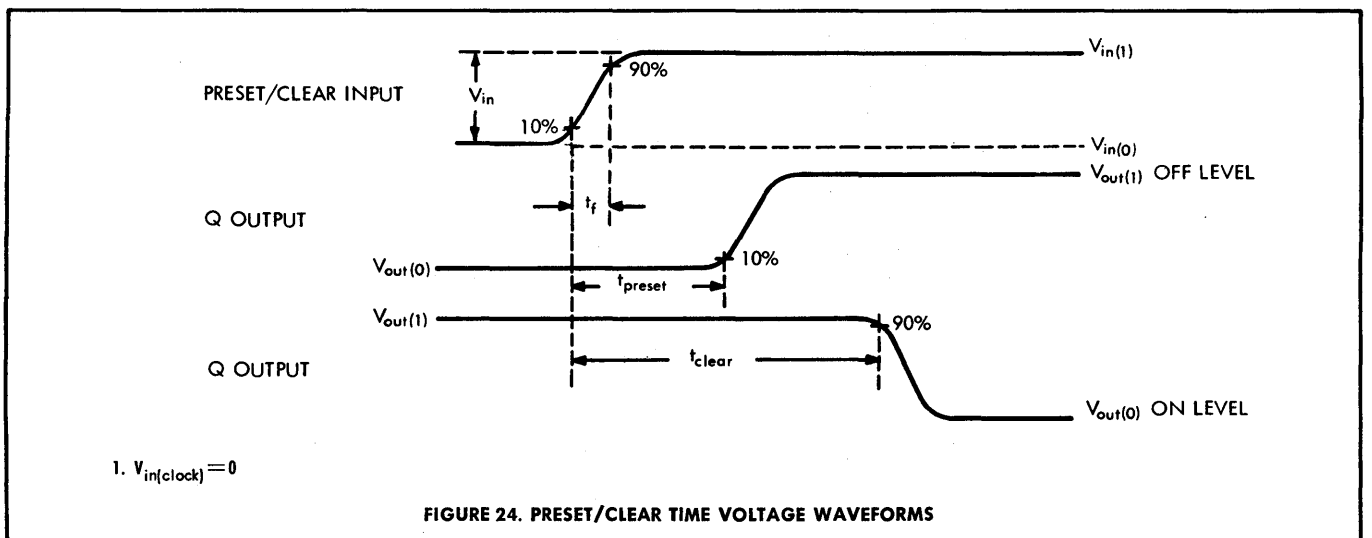
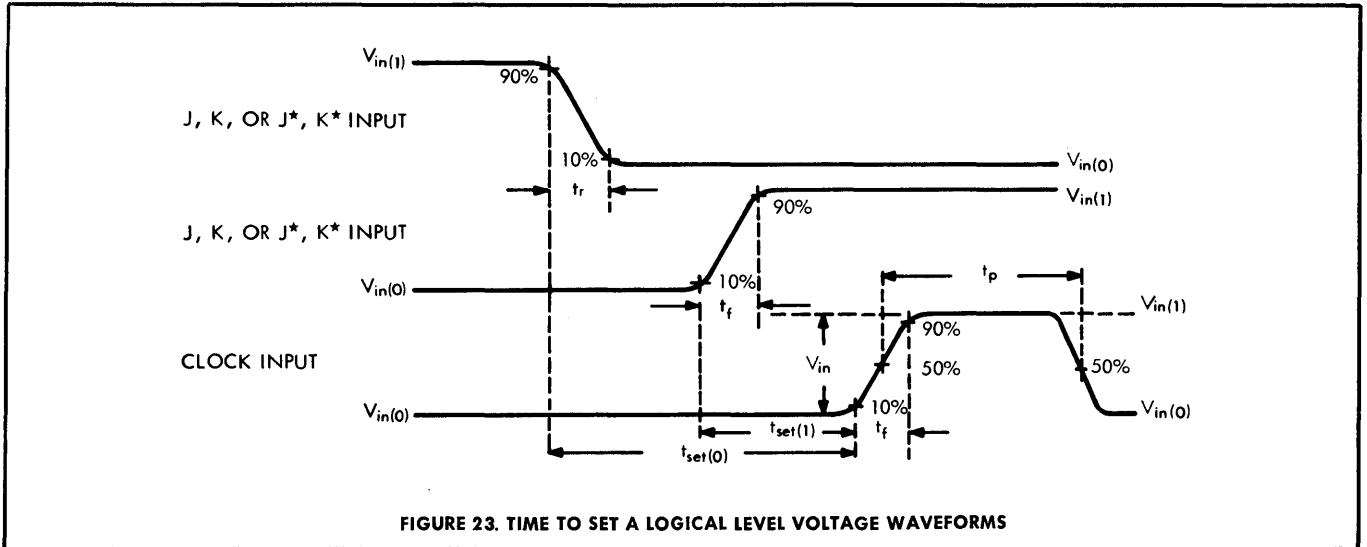
**switching characteristics**



**FIGURE 22. CLOCK PULSE AND OUTPUT VOLTAGE WAVEFORMS**

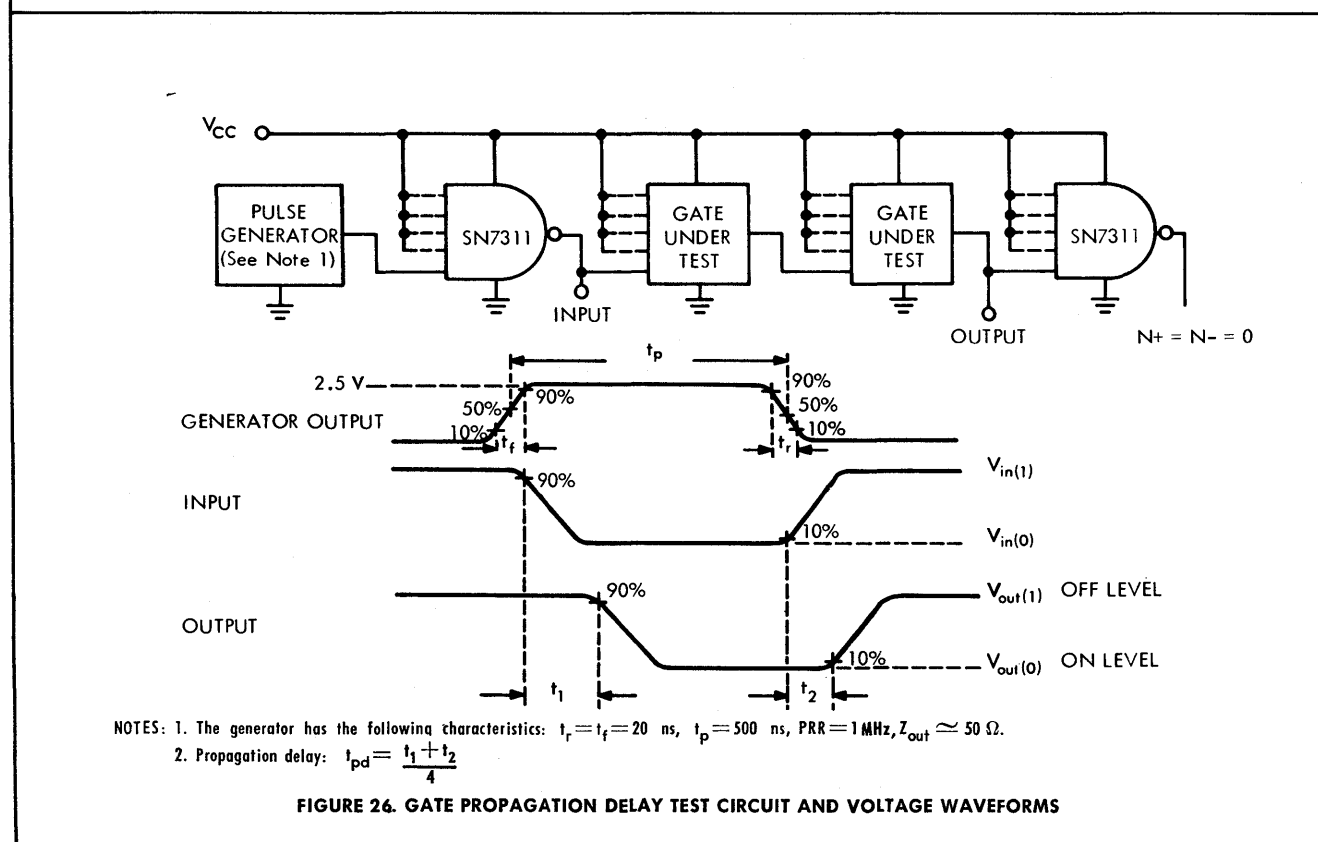
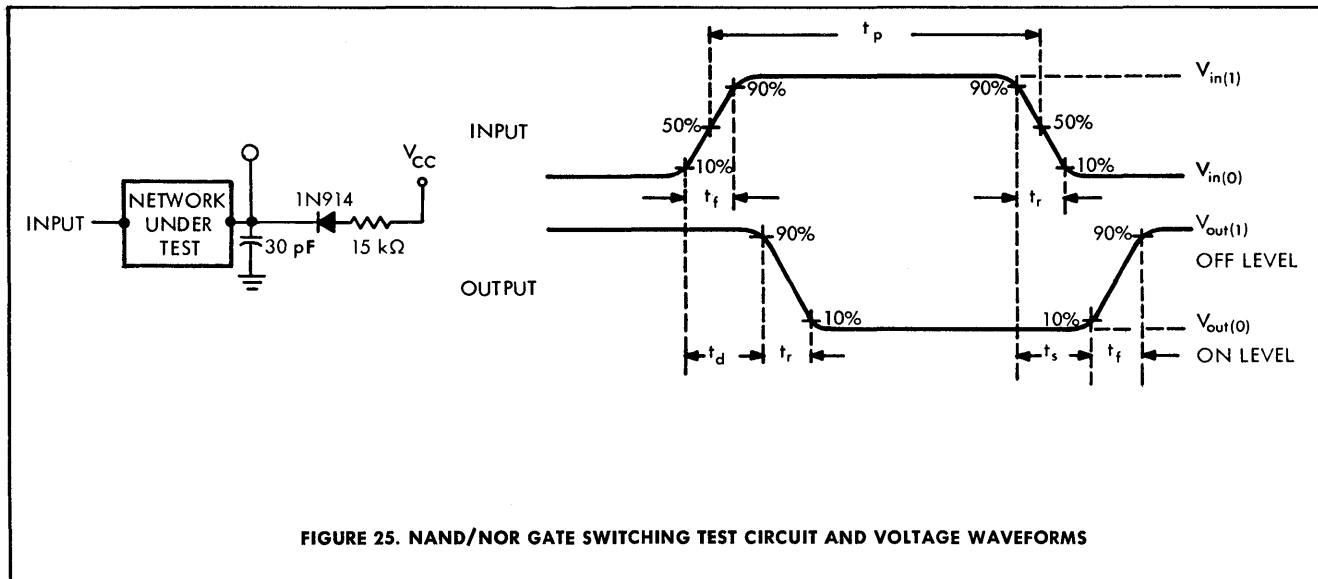
**PARAMETER MEASUREMENT INFORMATION**

switching characteristics (continued)



PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



**PARAMETER MEASUREMENT INFORMATION**

switching characteristics (continued)

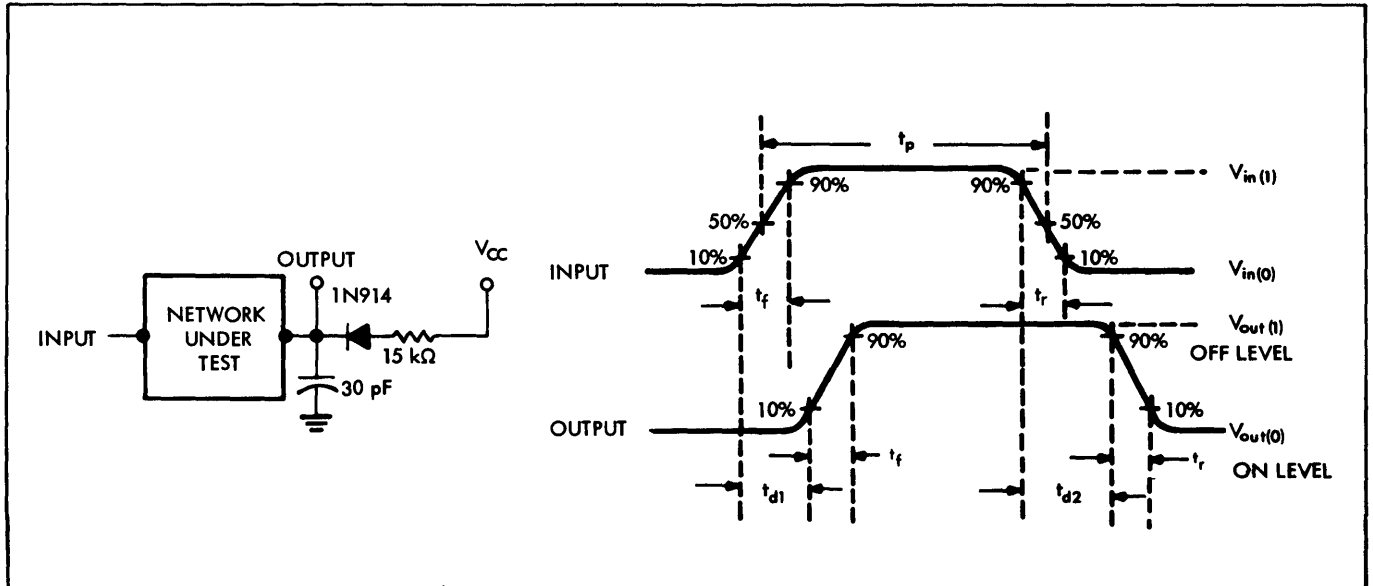


FIGURE 27. AND/OR GATE SWITCHING TEST CIRCUIT AND VOLTAGE WAVEFORMS

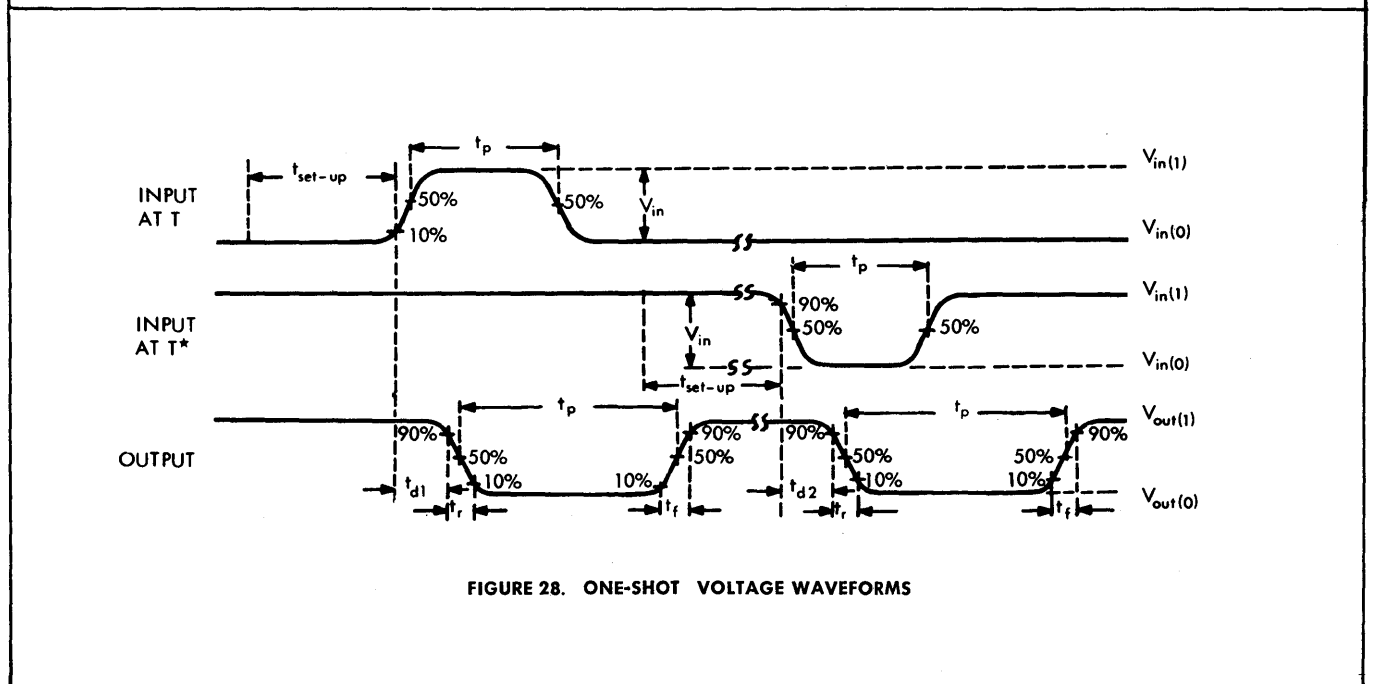


FIGURE 28. ONE-SHOT VOLTAGE WAVEFORMS

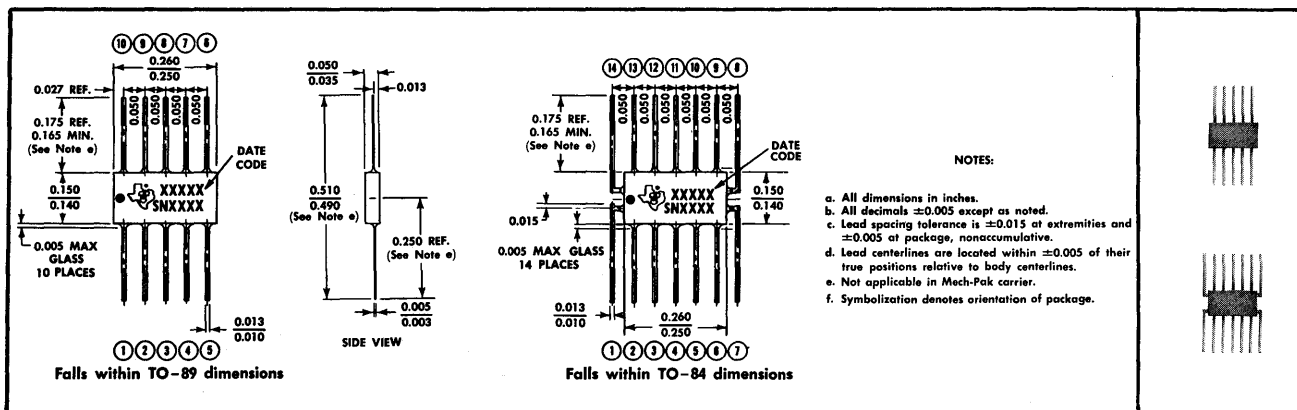


**MECHANICAL DATA**

**general**

Series 53 semiconductor networks are mounted in glass-to-metal hermetically sealed, welded packages. Package body and leads are gold-plated F-15<sup>‡</sup> glass-sealing alloy. Approximate weight is

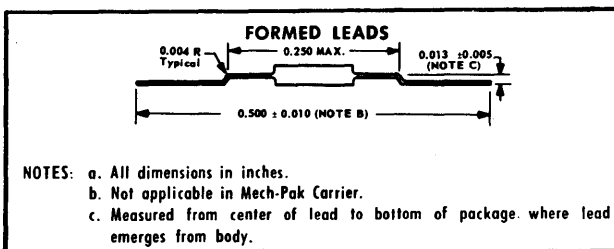
0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. All Series 53 networks are available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier.



- NOTES:
- a. All dimensions in inches.
  - b. All decimals  $\pm 0.005$  except as noted.
  - c. Lead spacing tolerance is  $\pm 0.015$  at extremities and  $\pm 0.005$  at package, nonaccumulative.
  - d. Lead centerlines are located within  $\pm 0.005$  of their true positions relative to body centerlines.
  - e. Not applicable in Mech-Pak carrier.
  - f. Symbolization denotes orientation of package.

**leads**

Gold-plated F-15<sup>‡</sup> leads require no additional cleaning or processing when used in soldered or welded assembly. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Standard lead length is 0.175 inch. Networks can be removed from Mech-Pak carriers with lead lengths up to 0.175 inch.



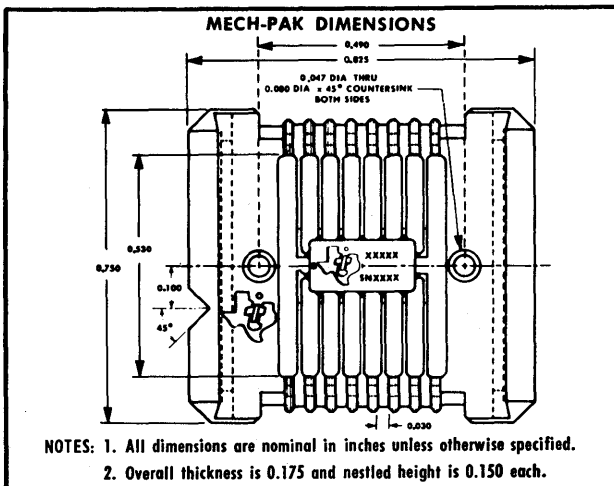
- NOTES:
- a. All dimensions in inches.
  - b. Not applicable in Mech-Pak Carrier.
  - c. Measured from center of lead to bottom of package where lead emerges from body.

**insulator**

An insulator, secured to the back surface of the package, permits mounting networks on circuit boards which have conductors passing beneath the package. The insulator is 0.0025 inch thick and has an insulation resistance of greater than 10 megohms at 25°C.

**mech-pak carrier**

The Mech-Pak carrier facilitates handling the network, and is compatible with automatic equipment used for testing and assembly. The carrier is particularly appropriate for mechanized assembly operations and will withstand temperatures of 125°C for indefinite periods.



- NOTES:
1. All dimensions are nominal in inches unless otherwise specified.
  2. Overall thickness is 0.175 and nestled height is 0.150 each.

**ordering instructions**

Variations in mechanical configuration of semiconductor networks are identified by suffix numbers shown in a table at the right.

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
	0.175 inch				Not Applicable			
Lead Length	No	No	Yes	Yes	No	No	Yes	Yes
Formed Leads	No	Yes	No	Yes	No	Yes	No	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5

<sup>†</sup>Patented by Texas Instruments

<sup>‡</sup>F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

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TEXAS INSTRUMENTS RESERVES THE RIGHT TO MAKE CHANGES AT ANY TIME IN ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.



**DIODE-TRANSISTOR LOGIC (DTL) NETWORKS  
FOR DIGITAL SYSTEMS**

SERIES 15 930  
BULLETIN NO. DL-S 668840, NOVEMBER, 1966  
REPLACES BULLETIN NO. DL-S 668129, FEBRUARY 1966

**application**

The series 15 930 networks are designed for use in medium to high-speed digital applications, including data handling, computer and control systems. Definitive specifications are provided for operating characteristics over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

**features**

**LOW SYSTEM COST**

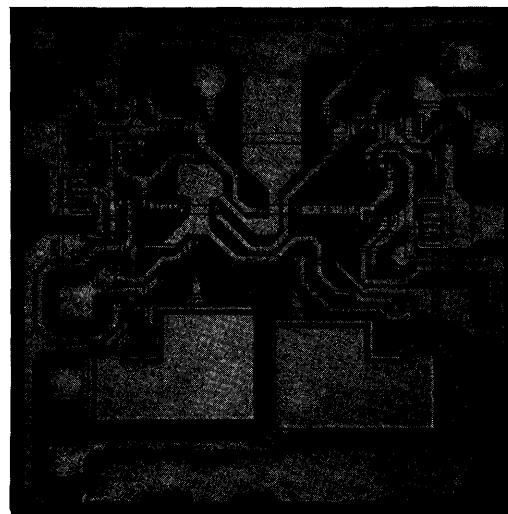
- multifunction gates offering low cost per logic function
- electrically designed specifically for monolithic integrated-circuit technology

**PERFORMANCE**

- high speed
- high d-c noise margins
- low power dissipation
- good fan-out capability

**EASE OF DESIGN**

- familiar logic configuration (DTL)
- single-ended output — dot-OR logic
- complete family for design flexibility
- single power supply



**TYPE SN15 950 PULSE-TRIGGERED BINARY BAR**

**description**

Series 15 930 is a complete family of diode-transistor logic (DTL) which is most attractive when high performance and low cost per function are necessities to system design.

The basic family consists of NAND gates, an expander, a buffer, a power gate, master-slave flip-flops, a pulse-triggered binary and a monostable multivibrator. Dual, triple, and quadruple multi-function gates are available to minimize system package count.

This line features a unique combination of high speed, high d-c noise margin, and low power dissipation. The single-ended output lends itself readily to performing dot-OR logic thus reducing the number of different type functional blocks in a system.

CONTENTS	Page
DESIGN CHARACTERISTICS AND LOGICAL SYMBOLS . . . . .	3002-3003
LOADING TABLES . . . . .	3004
DEFINITIVE SPECIFICATIONS . . . . .	3005-3027
D-C TEST CIRCUITS . . . . .	3028-3036
SWITCHING TIME CIRCUITS AND VOLTAGE WAVEFORMS . . . . .	3036-3039
MECHANICAL AND PACKAGING DATA . . . . .	3040

<sup>†</sup>Patented by Texas Instruments



# SERIES 15930

## SOLID CIRCUIT<sup>®</sup> SEMICONDUCTOR NETWORKS

typical operating characteristics,  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ , supply voltage  $V_{CC} = 4.5\text{ V}$  to  $5.5\text{ V}$

Speed: Gate Propagation Delay . . . . .	25 ns
Monostable Multivibrator Propagation Delay . . . . .	20 ns
Flip-Flop Clock Rate (SN15 931, SN15 945, SN15 948) . . . . .	7 MHz
Pulse-Triggered Binary Clock Rate . . . . .	20 MHz
Fan-Out Capability: Standard Gates (SN15 930, SN15 946, SN15 962) . . . . .	8
Buffer (SN15 932) . . . . .	25
Power Gate (SN15 944) . . . . .	27
Monostable Multivibrator (SN15 951) . . . . .	10
Flip-Flops: SN15 931 . . . . .	7
SN15 945 . . . . .	10
SN15 948 . . . . .	9
Pulse-Triggered Binary . . . . .	8
D-C Margin: At logical 1 . . . . .	500 mV
At logical 0 . . . . .	500 mV
Average Power Dissipation: Per Gate . . . . .	5 mW
Per Flip-Flop . . . . .	20 mW

### design characteristics

Series 15930 is a complete line of high-speed, high-noise-margin, low-power-dissipation, saturated DTL logic. The circuitry is a modification of the conventional DTL in that it utilizes only one power supply and provides a nonsaturating offset transistor in place of one of the offset diodes.

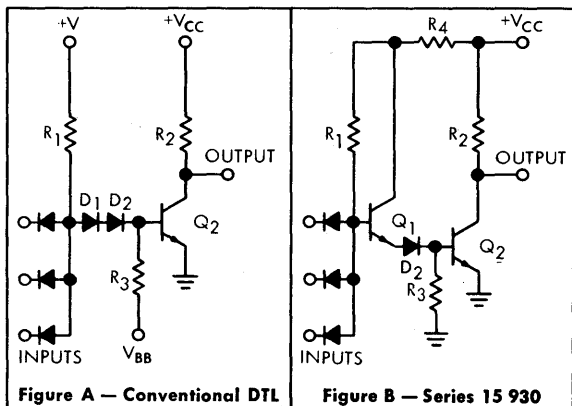


Figure A — Conventional DTL

Figure B — Series 15930

Replacing the offset diode  $D_1$  with transistor  $Q_1$  offers both the manufacturer and the customer a number of advantages:

1. Elimination of the  $V_{BB}$  power supply makes one more pin available for multifunction capability, which in turn reduces system package count.
2. Reduction of size of resistor  $R_3$  from  $20\text{ k}\Omega$  to  $5\text{ k}\Omega$  invites a substantial reduction in the overall size of the monolithic chip and improves yields. Both of these factors contribute heavily to reducing manufacturing costs.
3. Reduction of turn-off current transients on signal lines is accomplished because the stored charge on the output transistor  $Q_2$  is removed locally by  $R_3$  rather than through diodes  $D_1$  and  $D_2$  onto the input signal lines. These transients are also reduced during switching by the offset transistor  $Q_1$ , which operates in the unsaturated mode. This technique eliminates the necessity of producing low-speed, high-stored-charge diodes in the same monolithic bar with fast input diodes.

4. The offset transistor  $Q_1$  provides additional drive current to the output transistor  $Q_2$  without requiring high input currents when the input is in the low state. High input currents would limit fan-out of the driving gates. The additional drive to the output transistor invites the use of a smaller base resistor  $R_3$  and relaxes the  $h_{FE}$  requirement of the output transistor thus producing higher manufacturing yields.

In order to drive high-fan-out or high-capacity loads, a buffer is available which has a modified double-ended output. This output has a high-sink-current capability when in the ON state and a low-impedance emitter-follower output in the OFF state.

The master-slave flip-flops have AND gate inputs to the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows (see figure C):

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

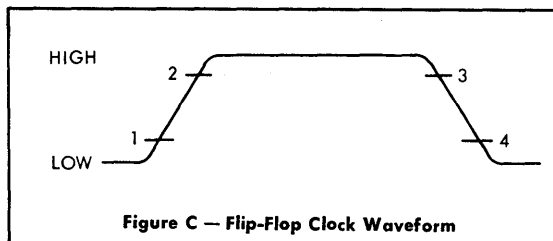
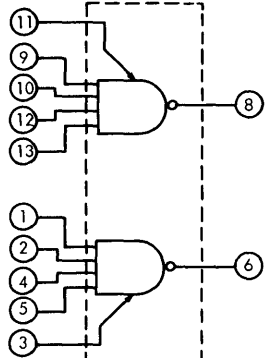
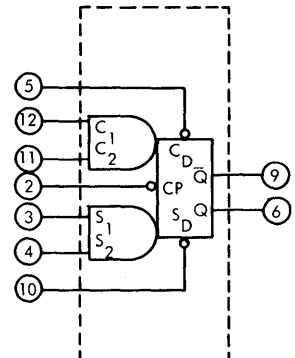
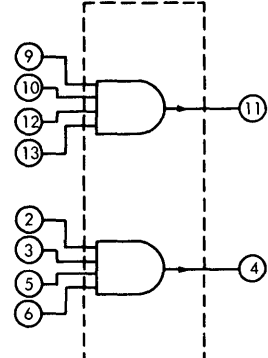
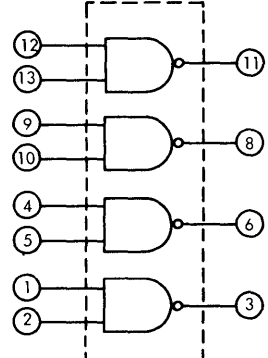
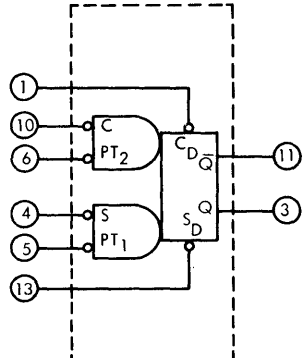
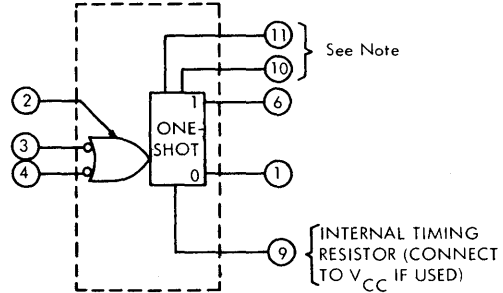
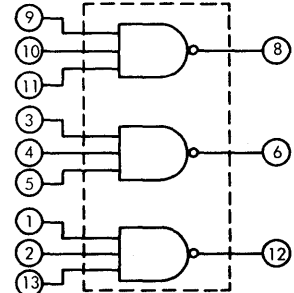


Figure C — Flip-Flop Clock Waveform

The pulse-triggered binary has two  $70\text{-pF}$  capacitors in the clock line which provide an input-differentiating network for high-speed clocking applications.

## standard line summary

Input and output pin numbers are shown for reference. For all networks shown  $V_{CC}$  is pin (14) (unless otherwise noted) and GND is pin (7). See referenced page for complete pin configuration.

<p><b>SN15 930</b> . . . . . See Page 3005  <b>SN15 932 (Buffer)</b> . . . . . See Page 3009  <b>SN15 944 (Power Gate)</b> . . . . . See Page 3012</p>  <p style="text-align: center;"><b>DUAL 4-INPUT NAND/NOR GATES</b></p>	<p><b>SN15 931</b> . . . . . See Page 3007  <b>SN15 945</b> . . . . . See Page 3014  <b>SN15 948</b> . . . . . See Page 3019</p>  <p style="text-align: center;"><b>FLIP-FLOPS WITH SET AND CLEAR</b></p>	
<p><b>SN15 933</b> . . . See Page 3011          (No <math>V_{CC}</math> Terminal)</p>  <p style="text-align: center;"><b>DUAL 4-INPUT EXPANDER</b></p>	<p><b>SN15 946</b> . . . See Page 3017</p>  <p style="text-align: center;"><b>QUADRUPLE 2-INPUT NAND/NOR GATE</b></p>	<p><b>SN15 950</b> . . . See Page 3022</p>  <p style="text-align: center;"><b>PULSE-TRIGGERED BINARY</b></p>
<p><b>SN15 951</b> . . . . . See Page 3024</p>  <p style="text-align: center;"><b>MONOSTABLE MULTIVIBRATOR</b></p> <p style="font-size: small;">NOTE: External capacitance is added between pins (10) and (11). External resistance bypasses internal timing resistor if connected from (10) to <math>V_{CC}</math>.</p>	<p><b>SN15 962</b> . . . . . See Page 3026</p>  <p style="text-align: center;"><b>TRIPLE 3-INPUT NAND/NOR GATE</b></p>	

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply Voltage $V_{CC}$ (See Note 1)	.. . . . .	+8 V
Continuous Output Sink Current (SN15 930, SN15 931, SN15 945, SN15 946, SN15 948, SN15 962)	.. . . . .	30 mA
Continuous Output Sink Current (SN15 950, SN15 951)	.. . . . .	50 mA
Continuous Output Sink Current (SN15 932, SN15 944)	.. . . . .	150 mA
Current Out of Input Terminal	.. . . . .	-10 mA
Current Into Input Terminal (except SN15 950 and SN15 951 pin (10))	.. . . . .	1 mA
Current Into Input Terminal (SN15 950 and SN15 951 pin (10))	.. . . . .	5 mA
Operating Free-Air Temperature Range (See Note 2)	.. . . . .	-55°C to 125°C
Storage Temperature Range	.. . . . .	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. This rating applies for networks operating at  $V_{CC} = 5.5$  V, all inputs† at 5.5 V, and the following output sink current:

SN15 930†, SN15 946, SN15 950, SN15 962	.. . . . .	12 mA
SN15 931	.. . . . .	10.6 mA
SN15 932†	.. . . . .	36 mA
SN15 944†	.. . . . .	40 mA
SN15 945	.. . . . .	15.2 mA
SN15 948	.. . . . .	13.6 mA
SN15 951	.. . . . .	15 mA

†Expander nodes open

**logic definition**

Series 15 930 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE = LOGICAL 0  
HIGH VOLTAGE = LOGICAL 1

**input current requirements**

Weighted values of input current requirements reflect worst-case conditions for  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$  and  $V_{CC} = 4.5$  V to 5.5 V. Each gate input requires that no more than -1.6 mA flow out of the input at a logical 0 input voltage level; therefore, one input load is -1.6 mA maximum. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

WEIGHTED VALUES OF INPUT CURRENT REQUIREMENTS			
NETWORK	TYPE	INPUT	NUMBER OF LOADS
GATES AND EXPANDER	SN15 930	Each Input	1
	SN15 932		
	SN15 933		
	SN15 944		
	SN15 946		
	SN15 962		
FLIP-FLOPS	SN15 931	Each Input (Synchronous or Asynchronous)	3/4
		Clock	2
	SN15 945 and SN15 948	Synchronous Inputs	3/4
		Asynchronous and Clock Inputs	2
PULSE-TRIGGERED BINARY	SN15 950	Synchronous or Asynchronous	1 1/2
MONOSTABLE MULTIVIBRATOR	SN15 951	Each Input	2

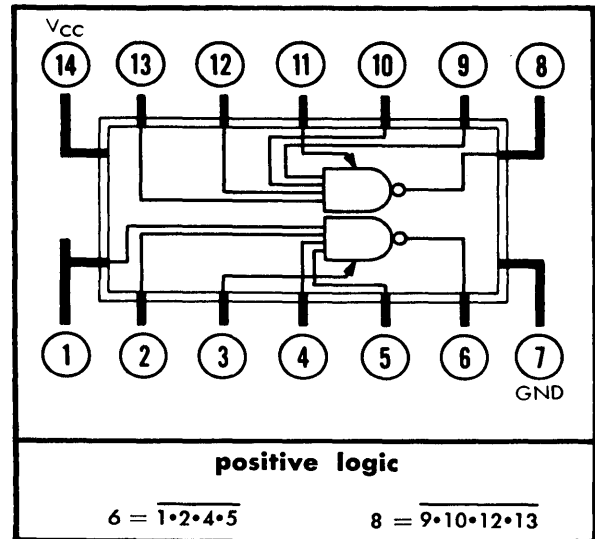
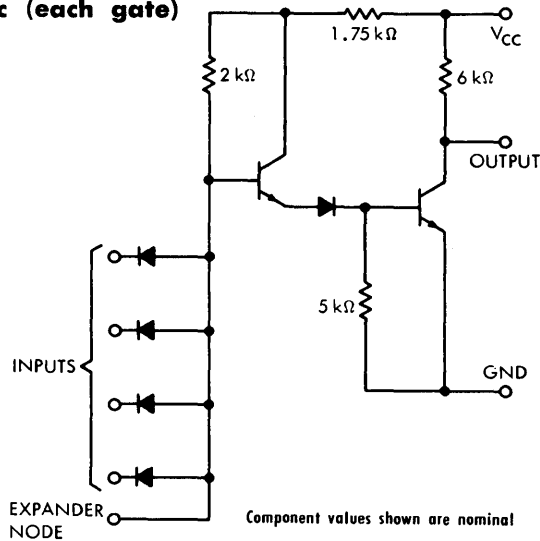
**output drive capability**

Weighted values of fan-out reflect the ability of an output to sink current (into the output terminal) under recommended operating conditions and are specified as positive values. Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuits indicate the actual direction of current flow.

WEIGHTED VALUES OF FAN-OUT			
NETWORK	TYPE	OUTPUT	LOADS
GATES	SN15 930	Each Output	8
	SN15 946		
	SN15 962		
BUFFER	SN15 932	Each Output	25
POWER GATE	SN15 944	Each Output	27
FLIP-FLOPS	SN15 931	Q or $\bar{Q}$	7
	SN15 945	Q or $\bar{Q}$	10
	SN15 948	Q or $\bar{Q}$	9
PULSE-TRIGGERED BINARY	SN15 950	Q or $\bar{Q}$	8
MONOSTABLE MULTIVIBRATOR	SN15 951	Each Output	10

# TYPE SN15 930 DUAL 4-INPUT NAND/NOR GATE

schematic (each gate)



### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	4.5 V to 5.5 V
Maximum Fan-Out From Each Output . . . . .	8

### electrical characteristics

PARAMETER	TEST FIGURE	TEST CONDITIONS †	MIN	MAX	UNIT
$V_{out(0)}$ Logical 0 output voltage (on level)	1	$V_{CC} = 4.5 \text{ V}, V_{in} = 1.9 \text{ V}, I_{sink} = 12 \text{ mA}, T_A = 25^\circ\text{C}$		0.4	V
		$V_{CC} = 4.5 \text{ V}, V_{in} = 2.1 \text{ V}, I_{sink} = 11.4 \text{ mA}, T_A = -55^\circ\text{C}$		0.4	V
		$V_{CC} = 4.5 \text{ V}, V_{in} = 1.7 \text{ V}, I_{sink} = 10.8 \text{ mA}, T_A = 125^\circ\text{C}$		0.45	V
$V_{out(1)}$ Logical 1 output voltage (off level)	2	$V_{CC} = 4.5 \text{ V}, V_{in} = 1.1 \text{ V}, I_{load} = -0.12 \text{ mA}, T_A = 25^\circ\text{C}$	2.6		V
		$V_{CC} = 4.5 \text{ V}, V_{in} = 1.4 \text{ V}, I_{load} = -0.12 \text{ mA}, T_A = -55^\circ\text{C}$	2.5		V
		$V_{CC} = 4.5 \text{ V}, V_{in} = 0.8 \text{ V}, I_{load} = -0.12 \text{ mA}, T_A = 125^\circ\text{C}$	2.5		V

† Expander nodes are open unless otherwise noted.

# TYPE SN15 930

## DUAL 4-INPUT NAND/NOR GATE

### electrical characteristics (continued)

PARAMETER	TEST FIGURE	TEST CONDITIONS †	MIN	MAX	UNIT
$V_{out(1)}$ Logical 1 output voltage (off level) with low voltage at expander input node, $V_{inX}$	3	$V_{CC} = 4.5\text{ V}$ , $V_{inX} = 1.8\text{ V}$ , $I_{load} = -0.12\text{ mA}$ , $T_A = 25^\circ\text{C}$	2.6		V
$I_{in(1)}$ Logical 1 level input current	4	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 4\text{ V}$ , $T_A = 25^\circ\text{C}$ and $-55^\circ\text{C}$		2	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}$ , $V_{in} = 4\text{ V}$ , $T_A = 125^\circ\text{C}$		5	$\mu\text{A}$
$I_{in(0)}$ Logical 0 level input current	5	$V_{CC} = 5.5\text{ V}$ , $V_{in} = 0$ , $V_R = 4\text{ V}$ , $T_A = 25^\circ\text{C}$ and $-55^\circ\text{C}$		-1.6	mA
		$V_{CC} = 5.5\text{ V}$ , $V_{in} = 0$ , $V_R = 4\text{ V}$ , $T_A = 125^\circ\text{C}$		-1.5	mA
$I_{out(1)}$ Output reverse current (off level)	6	$V_{CC} = V_{out} = 4.5\text{ V}$ , $T_A = 25^\circ\text{C}$		50	$\mu\text{A}$
$I_{os}$ Short-circuit output current	7	$V_{CC} = 5.5\text{ V}$ , $V_{out} = 0$ , $T_A = 25^\circ\text{C}$	-0.6	-1.34	mA
		$V_{CC} = 5.5\text{ V}$ , $V_{out} = 0$ , $T_A = -55^\circ\text{C}$		-1.34	mA
		$V_{CC} = 5.5\text{ V}$ , $V_{out} = 0$ , $T_A = 125^\circ\text{C}$		-1.3	mA
$I_{CC(0)}$ Logical 0 level supply current (both gates)	8	$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$		6.5	mA
$I_{CC(1)}$ Logical 1 level supply current at maximum $V_{CC}$ (both gates)	9	$V_{CC} = 8\text{ V}$ , $T_A = 25^\circ\text{C}$		5.5	mA

### switching characteristics, $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS †	MIN	MAX	UNIT
$t_{pd(0)}$ Propagation delay time to logical 0 level	51	$R_1 = 400\ \Omega$ , $C_L = 50\text{ pF}$	10	30	ns
$t_{pd(1)}$ Propagation delay time to logical 1 level		$R_1 = 3.9\text{ k}\Omega$ , $C_L = 30\text{ pF}$	25	80	ns

† Expander nodes are open unless otherwise noted.

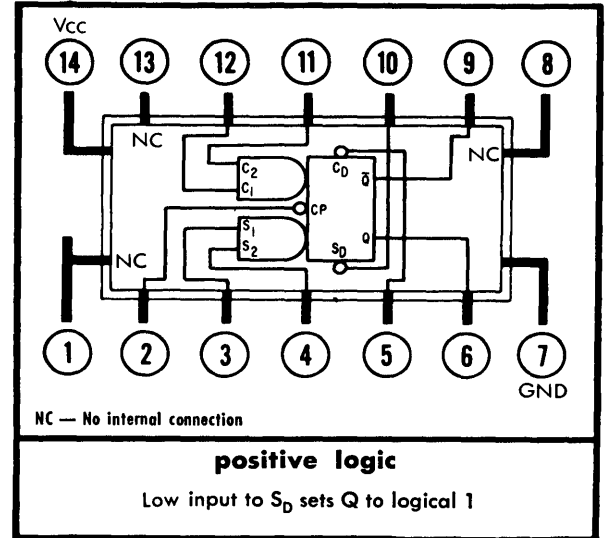
# TYPE SN15 931 FLIP-FLOP WITH SET AND CLEAR

## logic

**TRUTH TABLES**

R-S MODE						J-K MODE		
$t_n$				$t_{n+1}$		$t_n$		$t_{n+1}$
$S_1$	$S_2$	$C_1$	$C_2$	$Q$		$S_1$	$C_1$	$Q$
0	X	0	X	$Q_n$		0	0	$Q_n$
0	X	X	0	$Q_n$		0	1	0
X	0	0	X	$Q_n$		1	0	1
X	0	X	0	$Q_n$		1	1	$\bar{Q}_n$
0	X	1	1	0				
X	0	1	1	0				
1	1	0	X	1				
1	1	X	0	1				
1	1	1	1	Indeterminate				

- NOTES: 1.  $t_n$  = bit time before clock pulse.  
 2.  $t_{n+1}$  = bit time after clock pulse.  
 3. X indicates that either a logical 1 or a logical 0 may be present.  
 4. Logical 1 is more positive than logical 0.  
 5. For operation in the J-K mode connect  $S_2$  to  $\bar{Q}$  and  $C_2$  to  $Q$ .



## recommended operating conditions

Supply Voltage  $V_{CC}$  . . . . . 4.5 V to 5.5 V  
 Maximum Fan-Out From Each Output . . . . . 7

## electrical characteristics

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$ Logical 0 output voltage (on level) at $Q$ or $\bar{Q}$	10	$V_{CC} = 4.5 V, V_{CP(S)} = 0.95 V, I_{sink} = 10.6 mA, T_A = 25^\circ C$	0.4		V
		$V_{CC} = 4.5 V, V_{CP(S)} = 1.1 V, I_{sink} = 10 mA, T_A = -55^\circ C$	0.4		V
		$V_{CC} = 4.5 V, V_{CP(S)} = 0.75 V, I_{sink} = 9.5 mA, T_A = 125^\circ C$	0.45		V
$V_{out(1)}$ Logical 1 output voltage (off level) at $Q$ or $\bar{Q}$	11	$V_{CC} = 4.5 V, V_1 = 1.9 V, V_2 = 1.1 V, I_{load} = -0.12 mA, T_A = 25^\circ C$	2.6		V
		$V_{CC} = 4.5 V, V_1 = 2.1 V, V_2 = 1.4 V, I_{load} = -0.12 mA, T_A = -55^\circ C$	2.5		V
		$V_{CC} = 4.5 V, V_1 = 1.7 V, V_2 = 0.8 V, I_{load} = -0.12 mA, T_A = 125^\circ C$	2.5		V
$V_{out(1)}$ Logical 1 output voltage (off level) at $Q$ or $\bar{Q}$	12	$V_{CC} = 4.5 V, V_1 = 1.9 V, V_2 = 1.1 V, I_{load} = -0.12 mA, T_A = 25^\circ C$	2.6		V
		$V_{CC} = 4.5 V, V_1 = 2.1 V, V_2 = 1.4 V, I_{load} = -0.12 mA, T_A = -55^\circ C$	2.5		V
		$V_{CC} = 4.5 V, V_1 = 1.7 V, V_2 = 0.8 V, I_{load} = -0.12 mA, T_A = 125^\circ C$	2.5		V
$I_{CP(0)}$ Logical 0 level clock-input forward current	13	$V_{CC} = 5.5 V, V_{in} = 1.1 V, T_A = 25^\circ C$	-3.4		mA
		$V_{CC} = 5.5 V, V_{in} = 1.4 V, T_A = -55^\circ C$	-3.4		mA
		$V_{CC} = 5.5 V, V_{in} = 0.8 V, T_A = 125^\circ C$	-3		mA
$I_{CP(1)}$ Logical 1 level clock-input reverse current	14	$V_{CC} = 5.5 V, V_{CP} = 4 V, T_A = 25^\circ C \text{ and } -55^\circ C$	20		$\mu A$
		$V_{CC} = 5.5 V, V_{CP} = 4 V, T_A = 125^\circ C$	30		$\mu A$



# TYPE SN15 931 FLIP-FLOP WITH SET AND CLEAR

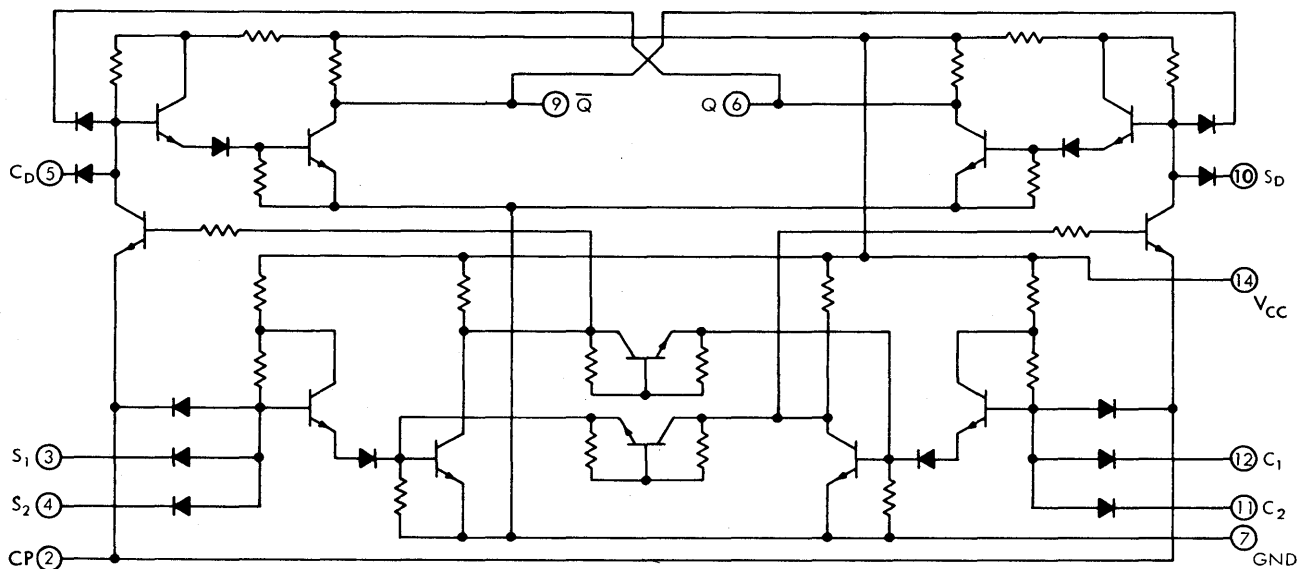
## electrical characteristics (continued)

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$ Logical 1 level synchronous-input current	15	$V_{CC} = 5.5\text{ V}, V_{in} = 4\text{ V}, T_A = 25^\circ\text{C and } -55^\circ\text{C}$		2	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}, V_{in} = 4\text{ V}, T_A = 125^\circ\text{C}$		5	$\mu\text{A}$
$I_{in(0)}$ Logical 0 level synchronous-input current	16	$V_{CC} = 5.5\text{ V}, V_{in} = 0, T_A = 25^\circ\text{C and } -55^\circ\text{C}$		-1.07	mA
		$V_{CC} = 5.5\text{ V}, V_{in} = 0, T_A = 125^\circ\text{C}$		-1	mA
$I_{in(1)}$ Logical 1 level asynchronous-input current	17	$V_{CC} = 5.5\text{ V}, V_{in} = 4\text{ V}, T_A = 25^\circ\text{C and } -55^\circ\text{C}$		2	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}, V_{in} = 4\text{ V}, T_A = 125^\circ\text{C}$		5	$\mu\text{A}$
$I_{in(0)}$ Logical 0 level asynchronous-input current	18	$V_{CC} = 5.5\text{ V}, V_{in} = 0, T_A = 25^\circ\text{C and } -55^\circ\text{C}$		-1.2	mA
		$V_{CC} = 5.5\text{ V}, V_{in} = 0, T_A = 125^\circ\text{C}$		-1.1	mA
$I_{CC(0)}$ Logical 0 level supply current	19	$V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$		11	mA
$I_{CC(1)}$ Logical 1 level supply current at maximum $V_{CC}$	20	$V_{CC} = 8\text{ V}, T_A = 25^\circ\text{C}$		14.5	mA

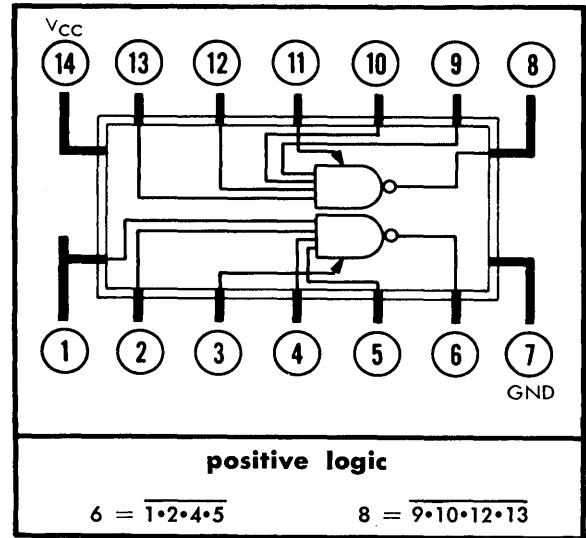
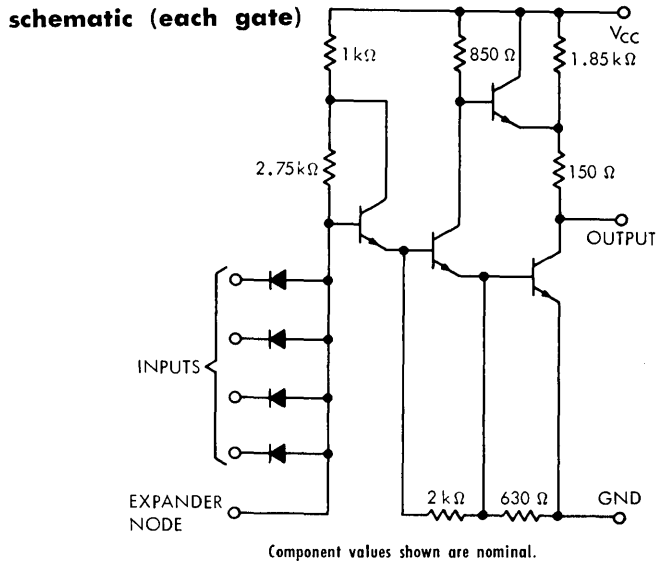
## switching characteristics, $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$ Propagation delay time to logical 0 level	52	$R_1 = 400\ \Omega, C_L = 50\ \text{pF}$	35	75	ns
$t_{pd(1)}$ Propagation delay time to logical 1 level		$R_1 = 3.9\ \text{k}\Omega, C_L = 30\ \text{pF}$	35	75	ns

## schematic



# TYPE SN15 932 DUAL 4-INPUT NAND/NOR BUFFER



### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	4.5 V to 5.5 V
Maximum Fan-Out From Each Output . . . . .	25

### electrical characteristics

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{out(0)}$ Logical 0 output voltage (on level)	1	$V_{CC} = 4.5 \text{ V}, V_{in} = 1.9 \text{ V}, I_{sink} = 36 \text{ mA}, T_A = 25^\circ\text{C}$		0.4	V
		$V_{CC} = 4.5 \text{ V}, V_{in} = 2.1 \text{ V}, I_{sink} = 34 \text{ mA}, T_A = -55^\circ\text{C}$		0.4	V
		$V_{CC} = 4.5 \text{ V}, V_{in} = 1.7 \text{ V}, I_{sink} = 32 \text{ mA}, T_A = 125^\circ\text{C}$		0.45	V
$V_{out(1)}$ Logical 1 output voltage (off level)	2	$V_{CC} = 4.5 \text{ V}, V_{in} = 1.1 \text{ V}, I_{load} = -2.5 \text{ mA}, T_A = 25^\circ\text{C}$	2.6		V
		$V_{CC} = 4.5 \text{ V}, V_{in} = 1.4 \text{ V}, I_{load} = -2 \text{ mA}, T_A = -55^\circ\text{C}$	2.5		V
		$V_{CC} = 4.5 \text{ V}, V_{in} = 0.8 \text{ V}, I_{load} = -4 \text{ mA}, T_A = 125^\circ\text{C}$	2.5		V

† Expander nodes are open unless otherwise noted.

# TYPE SN15 932

## DUAL 4-INPUT NAND/NOR BUFFER

### electrical characteristics (continued)

PARAMETER	TEST FIGURE	TEST CONDITIONS <sup>†</sup>	MIN	MAX	UNIT
$V_{out(1)}$ Logical 1 output voltage (off level) with low voltage input at expander node, $V_{inX}$	3	$V_{CC} = 4.5 \text{ V}$ , $V_{inX} = 1.8 \text{ V}$ , $I_{load} = -2.5 \text{ mA}$ , $T_A = 25^\circ\text{C}$	2.6		V
$I_{in(1)}$ Logical 1 level input current	4	$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 4 \text{ V}$ , $T_A = 25^\circ\text{C}$ and $-55^\circ\text{C}$		2	$\mu\text{A}$
		$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 4 \text{ V}$ , $T_A = 125^\circ\text{C}$		5	$\mu\text{A}$
$I_{in(0)}$ Logical 0 level input current	5	$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 0$ , $V_R = 4 \text{ V}$ , $T_A = 25^\circ\text{C}$ and $-55^\circ\text{C}$		-1.6	mA
		$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 0$ , $V_R = 4 \text{ V}$ , $T_A = 125^\circ\text{C}$		-1.5	mA
$I_{out(1)}$ Output reverse current (off level)	6	$V_{CC} = V_{out} = 4.5 \text{ V}$ , $T_A = 25^\circ\text{C}$		50	$\mu\text{A}$
$I_{os}$ Short-circuit output current	7	$V_{CC} = 5.5 \text{ V}$ , $V_{out} = 0$ , $T_A = 25^\circ\text{C}$		-18	mA
		$V_{CC} = 5.5 \text{ V}$ , $V_{out} = 0$ , $T_A = 125^\circ\text{C}$ and $-55^\circ\text{C}$		-16	mA
$I_{CC(0)}$ Logical 0 level supply current (both gates)	8	$V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$		26.6	mA
$I_{CC(1)}$ Logical 1 level supply current at maximum $V_{CC}$ (both gates)	9	$V_{CC} = 8 \text{ V}$ , $T_A = 25^\circ\text{C}$		6	mA

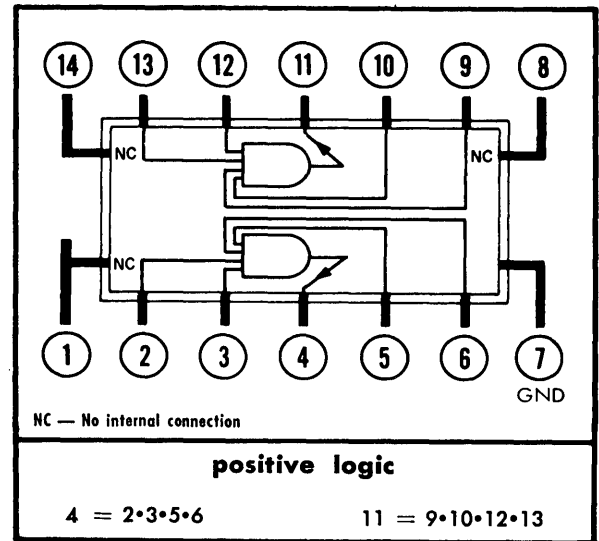
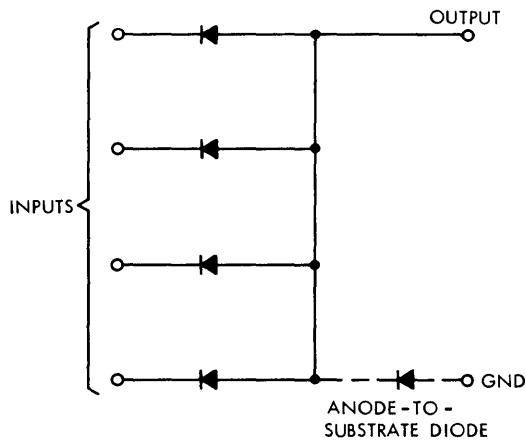
### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS <sup>†</sup>	MIN	MAX	UNIT
$t_{pd(0)}$ Propagation delay time to logical 0 level	51	$R_1 = 150 \Omega$ , $C_L = 500 \text{ pF}$	15	40	ns
$t_{pd(1)}$ Propagation delay time to logical 1 level		$R_1 = 510 \Omega$ , $C_L = 500 \text{ pF}$	25	80	ns

<sup>†</sup> Expander nodes are open unless otherwise noted.

# TYPE SN15 933 DUAL 4-INPUT EXPANDER

schematic (each expander)



## electrical characteristics

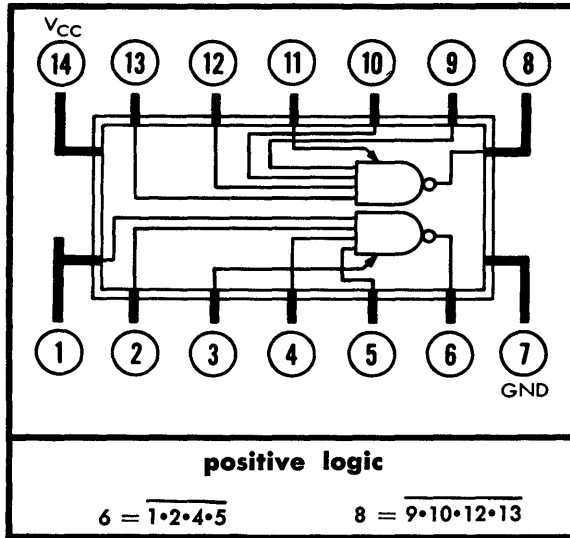
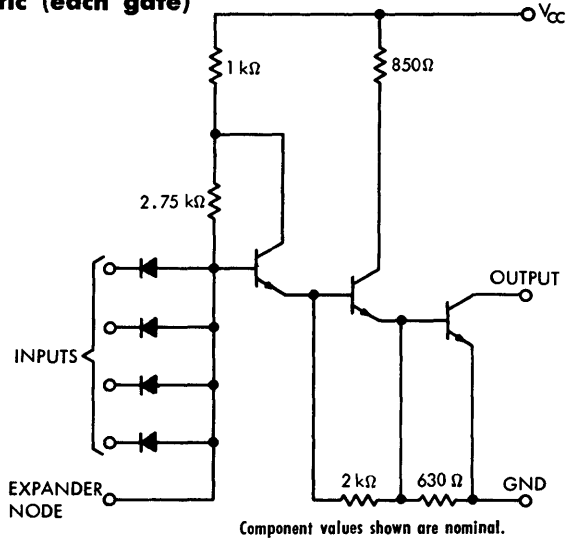
PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_F$ Input diode forward voltage	21	$I_{out} = 2 \text{ mA}, T_A = 25^\circ\text{C}$	0.7	0.82	V
		$I_{out} = 2 \text{ mA}, T_A = -55^\circ\text{C}$	0.85	0.98	V
		$I_{out} = 2 \text{ mA}, T_A = 125^\circ\text{C}$	0.5	0.65	V
$I_{inR}$ Input diode reverse current	22	$V_{in} = 4 \text{ V}, T_A = 25^\circ\text{C}$		2	$\mu\text{A}$
		$V_{in} = 4 \text{ V}, T_A = -55^\circ\text{C}$		2	$\mu\text{A}$
		$V_{in} = 4 \text{ V}, T_A = 125^\circ\text{C}$		5	$\mu\text{A}$
$I_{outR}$ Anode-to-substrate reverse current	23	$V_{out} = 4 \text{ V}, T_A = 25^\circ\text{C and } -55^\circ\text{C}$		10	$\mu\text{A}$
		$V_{out} = 4 \text{ V}, T_A = 125^\circ\text{C}$		25	$\mu\text{A}$

NOTE: A total of four expanders may be connected to an expandable gate to provide a fan-in of 20.

# TYPE SN15 944

## DUAL 4-INPUT NAND/NOR POWER GATE

schematic (each gate)



### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	4.5 V to 5.5 V
Maximum Fan-Out From Each Output . . . . .	27

### electrical characteristics

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{out(0)}$ Logical 0 output voltage (on level)	1	$V_{CC} = 4.5 \text{ V}, V_{in} = 1.9 \text{ V}, I_{sink} = 40 \text{ mA}, T_A = 25^\circ\text{C}$		0.4	V
		$V_{CC} = 4.5 \text{ V}, V_{in} = 2.1 \text{ V}, I_{sink} = 36 \text{ mA}, T_A = -55^\circ\text{C}$		0.4	V
		$V_{CC} = 4.5 \text{ V}, V_{in} = 1.7 \text{ V}, I_{sink} = 36 \text{ mA}, T_A = 125^\circ\text{C}$		0.45	V
$V_{out(1)}$ Logical 1 output voltage (off level)	24	$V_{CC} = 5.5 \text{ V}, I_{sink} = 5 \text{ mA}, T_A = 25^\circ\text{C}$	6		V
$I_{in(1)}$ Logical 1 level input current	4	$V_{CC} = 5.5 \text{ V}, V_{in} = 4 \text{ V}, T_A = 25^\circ\text{C}$ and $-55^\circ\text{C}$		2	$\mu\text{A}$
		$V_{CC} = 5.5 \text{ V}, V_{in} = 4 \text{ V}, T_A = 125^\circ\text{C}$		5	$\mu\text{A}$

† Expander nodes are open unless otherwise noted.

# TYPE SN15 944

## DUAL 4-INPUT NAND/NOR POWER GATE

### electrical characteristics (continued)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$I_{in(0)}$ Logical 0 level input current	5	$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 0$ , $V_R = 4 \text{ V}$ , $T_A = 25^\circ\text{C}$ and $-55^\circ\text{C}$		-1.6	mA
		$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 0$ , $V_R = 4 \text{ V}$ , $T_A = 125^\circ\text{C}$		-1.5	mA
$I_{out(1)}$ Output reverse current (off level, worst-case voltage at any input)	25	$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 1.1 \text{ V}$ , $V_{out} = 4.5 \text{ V}$ , $T_A = 25^\circ\text{C}$		100	$\mu\text{A}$
		$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 1.4 \text{ V}$ , $V_{out} = 4.5 \text{ V}$ , $T_A = -55^\circ\text{C}$		50	$\mu\text{A}$
		$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 0.8 \text{ V}$ , $V_{out} = 4.5 \text{ V}$ , $T_A = 125^\circ\text{C}$		200	$\mu\text{A}$
$I_{out(1)}$ Output reverse current (off level, worst-case voltage at expander input)	26	$V_{CC} = 5.5 \text{ V}$ , $V_{in x} = 1.8 \text{ V}$ , $V_{out} = 4.5 \text{ V}$ , $T_A = 25^\circ\text{C}$		100	$\mu\text{A}$
$I_{CC(0)}$ Logical 0 level supply current (both gates)	8	$V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$		20	mA
$I_{CC(1)}$ Logical 1 level supply current at maximum $V_{CC}$ (both gates)	9	$V_{CC} = 8 \text{ V}$ , $T_A = 25^\circ\text{C}$		6	mA

### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$t_{pd(0)}$ Propagation delay time to logical 0 level	51	$R_1 = 150 \Omega$ , $C_L = 100 \text{ pF}$	10	35	ns
$t_{pd(1)}$ Propagation delay time to logical 1 level		$R_1 = 510 \Omega$ , $C_L = 20 \text{ pF}$	15	50	ns

† Expander nodes are open unless otherwise noted.

# TYPE SN15 945

## FLIP-FLOP WITH SET AND CLEAR

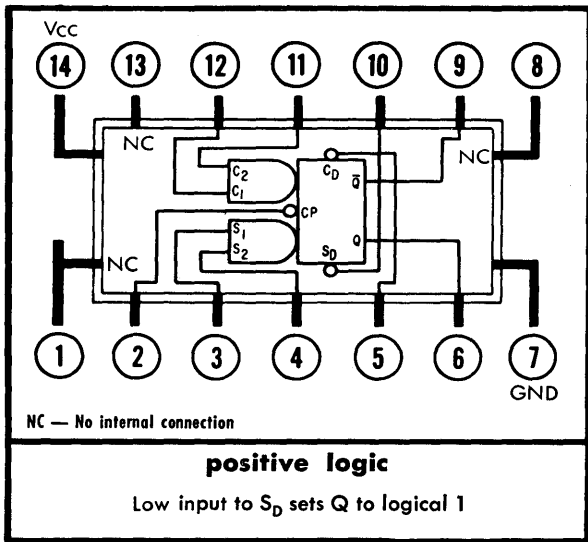
logic

TRUTH TABLES

R-S MODE				
$t_n$				$t_{n+1}$
$S_1$	$S_2$	$C_1$	$C_2$	Q
0	X	0	X	$Q_n$
0	X	X	0	$Q_n$
X	0	0	X	$Q_n$
X	0	X	0	$Q_n$
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	Indeterminate

J-K MODE		
$t_n$		$t_{n+1}$
$S_1$	$C_1$	Q
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\bar{Q}_n$

- NOTES: 1.  $t_n$  = bit time before clock pulse.  
 2.  $t_{n+1}$  = bit time after clock pulse.  
 3. X indicates that either a logical 1 or a logical 0 may be present.  
 4. Logical 1 is more positive than logical 0.  
 5. For operation in the J-K mode connect  $S_2$  to  $\bar{Q}$  and  $C_2$  to Q.



### recommended operating conditions

Supply Voltage  $V_{CC}$  . . . . . 4.5 V to 5.5 V  
 Maximum Fan-Out From Each Output . . . . . 10

### electrical characteristics

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$ Logical 0 output voltage (on level) at Q or $\bar{Q}$	27 and 28	$V_{CC} = 4.5 V, V_1 = 1.1 V, V_2 = 1.9 V, V_3 = 4.5 V, I_{sink} = 15.2 mA, T_A = 25^\circ C$	0.4		V
		$V_{CC} = 4.5 V, V_1 = 1.4 V, V_2 = 2.1 V, V_3 = 4.5 V, I_{sink} = 14.6 mA, T_A = -55^\circ C$	0.4		V
		$V_{CC} = 4.5 V, V_1 = 0.8 V, V_2 = 1.7 V, V_3 = 4.5 V, I_{sink} = 13.8 mA, T_A = 125^\circ C$	0.45		V
$V_{out(1)}$ Logical 1 output voltage (off level) at Q or $\bar{Q}$	12	$V_{CC} = 4.5 V, V_1 = 4.5 V, V_2 = 1.1 V, I_{load} = -0.12 mA, T_A = 25^\circ C$	2.6		V
		$V_{CC} = 4.5 V, V_1 = 4.5 V, V_2 = 1.4 V, I_{load} = -0.12 mA, T_A = -55^\circ C$	2.5		V
		$V_{CC} = 4.5 V, V_1 = 4.5 V, V_2 = 0.8 V, I_{load} = -0.12 mA, T_A = 125^\circ C$	2.5		V
$I_{CP(0)}$ Logical 0 level clock-input forward current	29	$V_{CC} = 5.5 V, V_{in} = 1.1 V, V_{CP} = 0, T_A = 25^\circ C$	-3.2		mA
		$V_{CC} = 5.5 V, V_{in} = 1.4 V, V_{CP} = 0, T_A = -55^\circ C$	-3.2		mA
		$V_{CC} = 5.5 V, V_{in} = 0.8 V, V_{CP} = 0, T_A = 125^\circ C$	-2.8		mA
$I_{CP(1)}$ Logical 1 level clock-input reverse current	30	$V_{CC} = 4 V, V_{CP} = 4 V, T_A = 25^\circ C \text{ and } -55^\circ C$	10		$\mu A$
		$V_{CC} = 4 V, V_{CP} = 4 V, T_A = 125^\circ C$	20		$\mu A$

# TYPE SN15 945 FLIP-FLOP WITH SET AND CLEAR

## electrical characteristics (continued)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$	Logical 1 level synchronous-input current	15	$V_{CC} = 5.5 \text{ V}, V_{in} = 4 \text{ V}, T_A = 25^\circ\text{C and } -55^\circ\text{C}$		2	$\mu\text{A}$
			$V_{CC} = 5.5 \text{ V}, V_{in} = 4 \text{ V}, T_A = 125^\circ\text{C}$		5	$\mu\text{A}$
$I_{in(0)}$	Logical 0 level synchronous-input current	31	$V_{CC} = 5.5 \text{ V}, V_{in} = 0, V_1 = 4 \text{ V}, V_{CP} = 4 \text{ V}, T_A = 25^\circ\text{C and } -55^\circ\text{C}$	-1.07		mA
			$V_{CC} = 5.5 \text{ V}, V_{in} = 0, V_1 = 4 \text{ V}, V_{CP} = 4 \text{ V}, T_A = 125^\circ\text{C}$	-1		mA
$I_{in(1)}$	Logical 1 level asynchronous-input current	32	$V_{CC} = 5.5 \text{ V}, V_{in} = 4 \text{ V}, V_1 = 5.5 \text{ V}, T_A = 25^\circ\text{C and } -55^\circ\text{C}$		2	$\mu\text{A}$
			$V_{CC} = 5.5 \text{ V}, V_{in} = 4 \text{ V}, V_1 = 5.5 \text{ V}, T_A = 125^\circ\text{C}$		5	$\mu\text{A}$
$I_{in(0)}$	Logical 0 level asynchronous-input current	33	$V_{CC} = 5.5 \text{ V}, V_{in} = 0, T_A = 25^\circ\text{C and } -55^\circ\text{C}$		-2.4	mA
			$V_{CC} = 5.5 \text{ V}, V_{in} = 0, T_A = 125^\circ\text{C}$		-2.1	mA
$I_{OS}$	Short-circuit output current	18	$V_{CC} = 5.5 \text{ V}, V_{in} = 5.5 \text{ V}, V_{out} = 0, T_A = 25^\circ\text{C and } -55^\circ\text{C}$	-0.7	-1.33	mA
			$V_{CC} = 5.5 \text{ V}, V_{in} = 5.5 \text{ V}, V_{out} = 0, T_A = 125^\circ\text{C}$	-0.625	-1.3	mA
$I_{CC(0)}$	Logical 0 level supply current	19	$V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$		14	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum $V_{CC}$	20	$V_{CC} = 8 \text{ V}, T_A = 25^\circ\text{C}$		16	mA

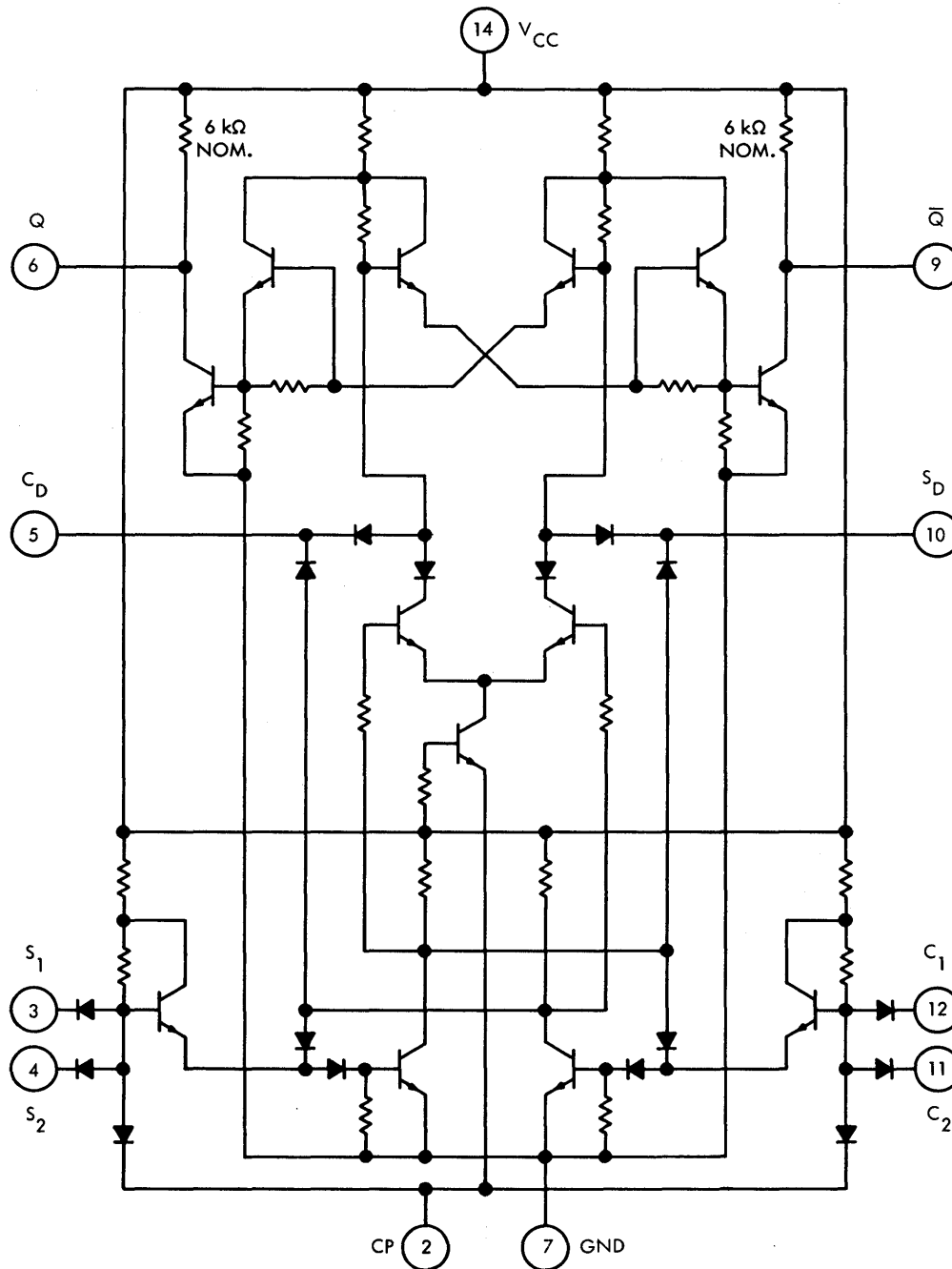
## switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	52	$R_1 = 330 \Omega, C_L = 50 \text{ pF}$		75	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level		$R_1 = 2 \text{ k}\Omega, C_L = 30 \text{ pF}$		75	ns



# TYPE SN15 945 FLIP-FLOP WITH SET AND CLEAR

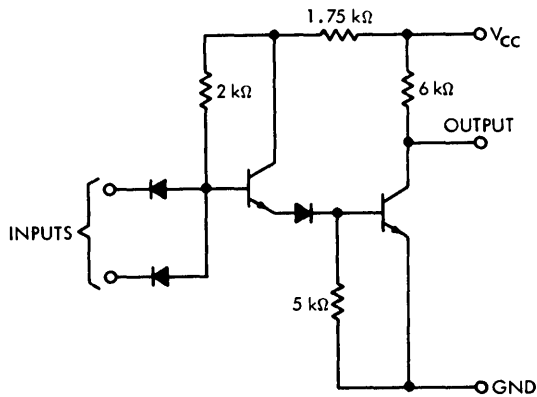
schematic



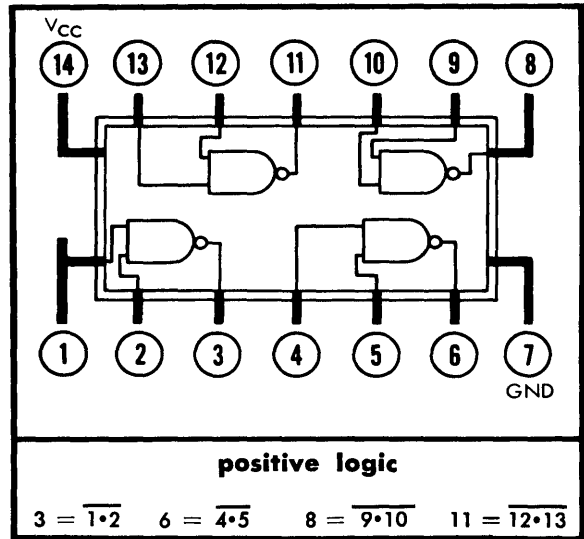
NOTE: Pins 1, 8, and 13 — no internal connection.

# TYPE SN15 946 QUADRUPLE 2-INPUT NAND/NOR GATE

schematic (each gate)



Component values shown are nominal.



### recommended operating conditions

Supply Voltage  $V_{CC}$  . . . . . 4.5 V to 5.5 V  
 Maximum Fan-Out From Each Output . . . . . 8

### electrical characteristics

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$ Logical 0 output voltage (on level)	1	$V_{CC} = 4.5 \text{ V}, V_{in} = 1.9 \text{ V}, I_{sink} = 12 \text{ mA}, T_A = 25^\circ\text{C}$		0.4	V
		$V_{CC} = 4.5 \text{ V}, V_{in} = 2.1 \text{ V}, I_{sink} = 11.4 \text{ mA}, T_A = -55^\circ\text{C}$		0.4	V
		$V_{CC} = 4.5 \text{ V}, V_{in} = 1.7 \text{ V}, I_{sink} = 10.8 \text{ mA}, T_A = 125^\circ\text{C}$		0.45	V
$V_{out(1)}$ Logical 1 output voltage (off level)	2	$V_{CC} = 4.5 \text{ V}, V_{in} = 1.1 \text{ V}, I_{load} = -0.12 \text{ mA}, T_A = 25^\circ\text{C}$	2.6		V
		$V_{CC} = 4.5 \text{ V}, V_{in} = 1.4 \text{ V}, I_{load} = -0.12 \text{ mA}, T_A = -55^\circ\text{C}$	2.5		V
		$V_{CC} = 4.5 \text{ V}, V_{in} = 0.8 \text{ V}, I_{load} = -0.12 \text{ mA}, T_A = 125^\circ\text{C}$	2.5		V

# TYPE SN15 946

## QUADRUPLE 2-INPUT NAND/NOR GATE

### electrical characteristics (continued)

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$ Logical 1 level input current	4	$V_{CC} = 5.5 \text{ V}, V_{in} = 4 \text{ V}, T_A = 25^\circ\text{C and } -55^\circ\text{C}$		2	$\mu\text{A}$
		$V_{CC} = 5.5 \text{ V}, V_{in} = 4 \text{ V}, T_A = 125^\circ\text{C}$		5	$\mu\text{A}$
$I_{in(0)}$ Logical 0 level input current	5	$V_{CC} = 5.5 \text{ V}, V_{in} = 0, V_R = 4 \text{ V}, T_A = 25^\circ\text{C and } -55^\circ\text{C}$		-1.6	mA
		$V_{CC} = 5.5 \text{ V}, V_{in} = 0, V_R = 4 \text{ V}, T_A = 125^\circ\text{C}$		-1.5	mA
$I_{out(1)}$ Output reverse current (off level)	6	$V_{CC} = V_{out} = 4.5 \text{ V}, T_A = 25^\circ\text{C}$		50	$\mu\text{A}$
$I_{OS}$ Short-circuit output current	7	$V_{CC} = 5.5 \text{ V}, V_{out} = 0, T_A = 25^\circ\text{C}$	-0.6	-1.34	mA
		$V_{CC} = 5.5 \text{ V}, V_{out} = 0, T_A = -55^\circ\text{C}$		-1.34	mA
		$V_{CC} = 5.5 \text{ V}, V_{out} = 0, T_A = 125^\circ\text{C}$		-1.3	mA
$I_{CC(0)}$ Logical 0 level supply current (all gates)	8	$V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$		13	mA
$I_{CC(1)}$ Logical 1 level supply current at maximum $V_{CC}$ (all gates)	9	$V_{CC} = 8 \text{ V}, T_A = 25^\circ\text{C}$		11	mA

### switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$ Propagation delay time to logical 0 level	51	$R_1 = 400 \Omega, C_L = 50 \text{ pF}$	10	30	ns
$t_{pd(1)}$ Propagation delay time to logical 1 level		$R_1 = 3.9 \text{ k}\Omega, C_L = 30 \text{ pF}$	25	80	ns

# TYPE SN15 948 FLIP-FLOP WITH SET AND CLEAR

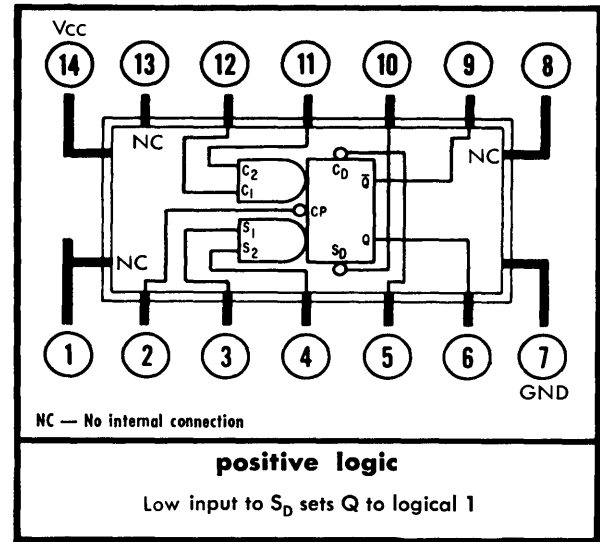
## logic

**TRUTH TABLES**

R-S MODE				
$t_n$				$t_{n+1}$
$S_1$	$S_2$	$C_1$	$C_2$	Q
0	X	0	X	$Q_n$
0	X	X	0	$Q_n$
X	0	0	X	$Q_n$
X	0	X	0	$Q_n$
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	Indeterminate

J-K MODE		
$t_n$		$t_{n+1}$
$S_1$	$C_1$	Q
0	0	$Q_n$
0	1	0
1	0	1
1	1	$Q_n$

- NOTES: 1.  $t_n$  = bit time before clock pulse.  
 2.  $t_{n+1}$  = bit time after clock pulse.  
 3. X indicates that either a logical 1 or a logical 0 may be present.  
 4. Logical 1 is more positive than logical 0.  
 5. For operation in the J-K mode connect  $S_2$  to  $\bar{Q}$  and  $C_2$  to Q.



## recommended operating conditions

Supply Voltage  $V_{CC}$  . . . . . 4.5 V to 5.5 V  
 Maximum Fan-Out From Each Output . . . . . 9

## electrical characteristics

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$ Logical 0 output voltage (on level) at Q or $\bar{Q}$	27 and 28	$V_{CC} = 4.5 V, V_1 = 1.1 V, V_2 = 1.9 V, V_3 = 4.5 V, I_{sink} = 13.6 mA, T_A = 25^\circ C$	0.4		V
		$V_{CC} = 4.5 V, V_1 = 1.4 V, V_2 = 2.1 V, V_3 = 4.5 V, I_{sink} = 13 mA, T_A = -55^\circ C$	0.4		V
		$V_{CC} = 4.5 V, V_1 = 0.8 V, V_2 = 1.7 V, V_3 = 4.5 V, I_{sink} = 12.3 mA, T_A = 125^\circ C$	0.45		V
$V_{out(1)}$ Logical 1 output voltage (off level) at Q or $\bar{Q}$	12	$V_{CC} = 4.5 V, V_1 = 4.5 V, V_2 = 1.1 V, I_{load} = -0.12 mA, T_A = 25^\circ C$	2.6		V
		$V_{CC} = 4.5 V, V_1 = 4.5 V, V_2 = 1.4 V, I_{load} = -0.12 mA, T_A = -55^\circ C$	2.5		V
		$V_{CC} = 4.5 V, V_1 = 4.5 V, V_2 = 0.8 V, I_{load} = -0.12 mA, T_A = 125^\circ C$	2.5		V
$I_{CP(0)}$ Logical 0 level clock-input forward current	29	$V_{CC} = 5.5 V, V_{in} = 1.1 V, V_{CP} = 0, T_A = 25^\circ C$	-2.56		mA
		$V_{CC} = 5.5 V, V_{in} = 1.4 V, V_{CP} = 0, T_A = -55^\circ C$	-2.56		mA
		$V_{CC} = 5.5 V, V_{in} = 0.8 V, V_{CP} = 0, T_A = 125^\circ C$	-2.2		mA
$I_{CP(1)}$ Logical 1 level clock-input reverse current	30	$V_{CC} = 4 V, V_{CP} = 4 V, T_A = 25^\circ C \text{ and } -55^\circ C$	10		$\mu A$
		$V_{CC} = 4 V, V_{CP} = 4 V, T_A = 125^\circ C$	20		$\mu A$

# TYPE SN15 948

## FLIP-FLOP WITH SET AND CLEAR

### electrical characteristics (continued)

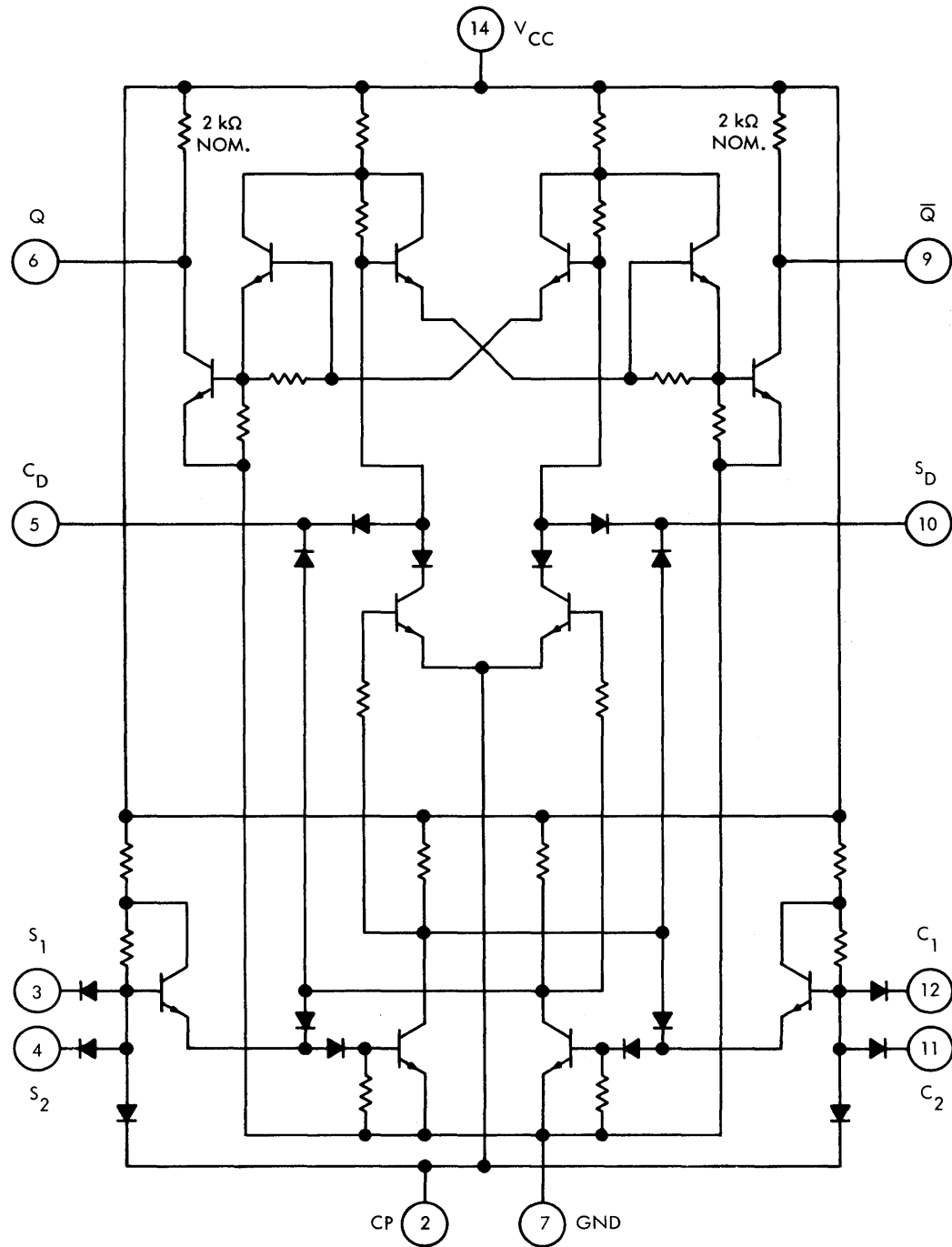
PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$ Logical 1 level synchronous-input current	15	$V_{CC} = 5.5 \text{ V}, V_{in} = 4 \text{ V}, T_A = 25^\circ\text{C and } -55^\circ\text{C}$		2	$\mu\text{A}$
		$V_{CC} = 5.5 \text{ V}, V_{in} = 4 \text{ V}, T_A = 125^\circ\text{C}$		5	$\mu\text{A}$
$I_{in(0)}$ Logical 0 level synchronous-input current	31	$V_{CC} = 5.5 \text{ V}, V_{in} = 0, V_1 = 4 \text{ V}, V_{CP} = 4 \text{ V}, T_A = 25^\circ\text{C and } -55^\circ\text{C}$		-1.07	mA
		$V_{CC} = 5.5 \text{ V}, V_{in} = 0, V_1 = 4 \text{ V}, V_{CP} = 4 \text{ V}, T_A = 125^\circ\text{C}$		-1	mA
$I_{in(1)}$ Logical 1 level asynchronous-input current	32	$V_{CC} = 5.5 \text{ V}, V_{in} = 4 \text{ V}, V_1 = 5.5 \text{ V}, T_A = 25^\circ\text{C and } -55^\circ\text{C}$		2	$\mu\text{A}$
		$V_{CC} = 5.5 \text{ V}, V_{in} = 4 \text{ V}, V_1 = 5.5 \text{ V}, T_A = 125^\circ\text{C}$		5	$\mu\text{A}$
$I_{in(0)}$ Logical 0 level asynchronous-input current	33	$V_{CC} = 5.5 \text{ V}, V_{in} = 0, T_A = 25^\circ\text{C and } -55^\circ\text{C}$		-2.4	mA
		$V_{CC} = 5.5 \text{ V}, V_{in} = 0, T_A = 125^\circ\text{C}$		-2.1	mA
$I_{OS}$ Short-circuit output current	18	$V_{CC} = 5.5 \text{ V}, V_{in} = 5.5 \text{ V}, V_{out} = 0, T_A = 25^\circ\text{C and } -55^\circ\text{C}$	-2.1	-3.96	mA
		$V_{CC} = 5.5 \text{ V}, V_{in} = 5.5 \text{ V}, V_{out} = 0, T_A = 125^\circ\text{C}$		-3.54	mA
$I_{CC(0)}$ Logical 0 level supply current	19	$V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$		16.2	mA
$I_{CC(1)}$ Logical 1 level supply current at maximum $V_{CC}$	20	$V_{CC} = 8 \text{ V}, T_A = 25^\circ\text{C}$		16	mA

### switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$ Propagation delay time to logical 0 level	52	$R_1 = 330 \Omega, C_L = 50 \text{ pF}$	5	65	ns
$t_{pd(1)}$ Propagation delay time to logical 1 level		$R_1 = 2 \text{ k}\Omega, C_L = 30 \text{ pF}$	5	75	ns

# TYPE SN15 948 FLIP-FLOP WITH SET AND CLEAR

schematic



NOTE: Pins 1, 8 and 13 no internal connection.

# TYPE SN15 950 PULSE-TRIGGERED BINARY

## logic

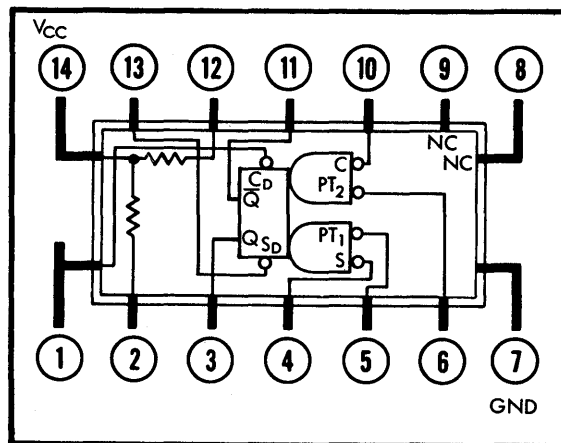
### TRUTH TABLES

SYNCHRONOUS					
$t_n$ PULSE INPUT				$t_{n+1}$ OUTPUT	
S	C	PT <sub>1</sub>	PT <sub>2</sub>	Q	$\bar{Q}$
1	X	X	1	Q <sub>n</sub>	Q <sub>n</sub>
X	1	1	X	Q <sub>n</sub>	Q <sub>n</sub>
0	1	0	X	1	0
0	X	0	1	1	0
1	0	X	0	0	1
X	0	1	0	0	1
0	0	0	0	Indeterminate	

ASYNCHRONOUS			
DIRECT INPUT		OUTPUT	
S <sub>D</sub>	C <sub>D</sub>	Q	$\bar{Q}$
1	1	Q <sub>n</sub>	Q <sub>n</sub>
0	1	0	1
1	0	1	0
0	0	1	1

#### NOTES:

1. X indicates that either a logical 1 or a logical 0 may be present.
2. Logical 1 is more positive than logical 0.
3. Logical states shown for pulse inputs PT<sub>1</sub> and PT<sub>2</sub> indicate that a transition to that state has just occurred.
4. Truth tables reflect individual conditions at the inputs. Either direct input may be used to inhibit its corresponding pulse input.



## recommended operating conditions

Supply Voltage V <sub>CC</sub> . . . . .	4.5 V to 5.5 V
Maximum Fan-Out From Each Output . . . . .	8

## electrical characteristics

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
V <sub>out(0)</sub> Logical 0 output voltage (on level) at Q or $\bar{Q}$	34	V <sub>CC</sub> = 4.5 V, V <sub>in</sub> = 1.9 V, I <sub>sink</sub> = 12 mA, T <sub>A</sub> = 25°C		0.4	V
		V <sub>CC</sub> = 4.5 V, V <sub>in</sub> = 2.1 V, I <sub>sink</sub> = 11.4 mA, T <sub>A</sub> = -55°C		0.4	V
		V <sub>CC</sub> = 4.5 V, V <sub>in</sub> = 1.7 V, I <sub>sink</sub> = 10.8 mA, T <sub>A</sub> = 125°C		0.45	V
V <sub>out(1)</sub> Logical 1 output voltage (off level) at Q or $\bar{Q}$	35	V <sub>CC</sub> = 4.5 V, V <sub>1</sub> = 1.1 V, V <sub>2</sub> = 1.9 V, V <sub>3</sub> = 4.5 V, I <sub>load</sub> = -1.5 mA, T <sub>A</sub> = 25°C	2.6		V
		V <sub>CC</sub> = 4.5 V, V <sub>1</sub> = 1.4 V, V <sub>2</sub> = 2.1 V, V <sub>3</sub> = 4.5 V, I <sub>load</sub> = -1.5 mA, T <sub>A</sub> = -55°C	2.5		V
		V <sub>CC</sub> = 4.5 V, V <sub>1</sub> = 0.8 V, V <sub>2</sub> = 1.7 V, V <sub>3</sub> = 4.5 V, I <sub>load</sub> = -1.5 mA, T <sub>A</sub> = 125°C	2.5		V
I <sub>inPT</sub> Pulse-triggered-input current	36	V <sub>CC</sub> = 5.5 V, V <sub>in</sub> = 8 V, T <sub>A</sub> = 25°C and -55°C		2	μA
		V <sub>CC</sub> = 5.5 V, V <sub>in</sub> = 8 V, T <sub>A</sub> = 125°C		5	μA
I <sub>in(0)</sub> Logical 0 level input current at C or S	37	V <sub>CC</sub> = 5.5 V, V <sub>in</sub> = 0, T <sub>A</sub> = 25°C and -55°C		-2.4	mA
		V <sub>CC</sub> = 5.5 V, V <sub>in</sub> = 0, T <sub>A</sub> = 125°C		-2.25	mA
I <sub>in(0)</sub> Logical 0 level input current at C <sub>D</sub> or S <sub>D</sub>	37	V <sub>CC</sub> = 5.5 V, V <sub>in</sub> = 0, T <sub>A</sub> = 25°C and -55°C		-1.82	mA
		V <sub>CC</sub> = 5.5 V, V <sub>in</sub> = 0, T <sub>A</sub> = 125°C		-1.62	mA

# TYPE SN15 950 PULSE-TRIGGERED BINARY

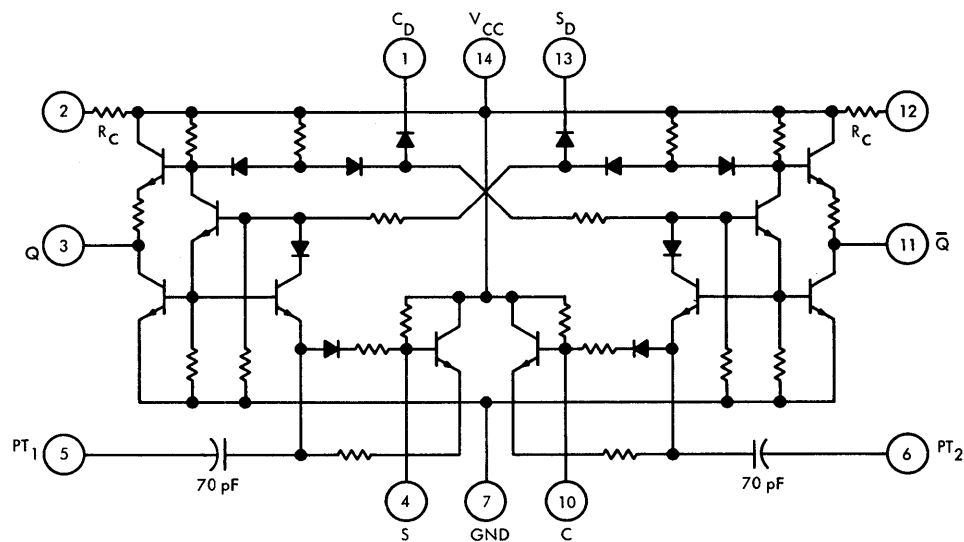
## electrical characteristics (continued)

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$ Logical 1 level input current at $C_D$ or $S_D$	38	$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 4 \text{ V}$ , $T_A = 25^\circ\text{C}$ and $-55^\circ\text{C}$		2	$\mu\text{A}$
		$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 4 \text{ V}$ , $T_A = 125^\circ\text{C}$		5	$\mu\text{A}$
$I_{RC}$ Current through resistor $R_C$	39	$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 0$ , $T_A = 25^\circ\text{C}$	-4.22	-7.35	mA
$I_{OS}$ Short-circuit output current	40	$V_{CC} = 5.5 \text{ V}$ , $V_{out} = 0$ , $T_A = 25^\circ\text{C}$ and $-55^\circ\text{C}$	-15.7	-27	mA
		$V_{CC} = 5.5 \text{ V}$ , $V_{out} = 0$ , $T_A = 125^\circ\text{C}$	-14.6	-26	mA
$I_{out(1)}$ Output reverse current (off level)	40	$V_{CC} = 4.5 \text{ V}$ , $V_{out} = 4.5 \text{ V}$ , $T_A = 25^\circ\text{C}$		50	$\mu\text{A}$
$I_{CC(0)}$ Logical 0 level supply current	41	$V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$		8.7	mA
$I_{CC(1)}$ Logical 1 level supply current at maximum $V_{CC}$	42	$V_{CC} = 8 \text{ V}$ , $T_A = 25^\circ\text{C}$		18.4	mA

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$ Propagation delay time to logical 0 level	53	$R_1 = 400 \Omega$ , $C_1 = 100 \text{ pF}$	5	32	ns
$t_{pd(1)}$ Propagation delay time to logical 1 level		$R_1 = 3.9 \text{ k}\Omega$ , $C_1 = 100 \text{ pF}$	5	25	ns

## schematic





# TYPE SN15 951

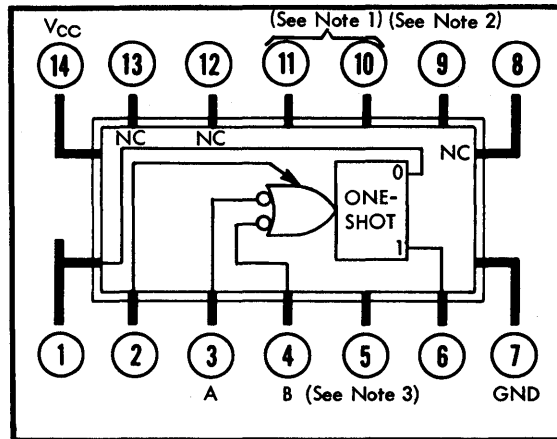
## MONOSTABLE MULTIVIBRATOR

logic

TRUTH TABLE

$t_n$ INPUT		$t_{n+1}$ INPUT		OUTPUT
A	B	A	B	
1	1	1	1	INHIBIT
1	1	1	0	ONE-SHOT
1	1	0	1	ONE-SHOT
1	1	0	0	ONE-SHOT
0	1	X	X	INHIBIT
1	0	X	X	INHIBIT
0	0	X	X	INHIBIT

NOTES: a.  $t_n$  = time before input transition.  
 b.  $t_{n+1}$  = time after input transition.  
 c. X indicates that either a logical 1 or a logical 0 may be present.



NOTES: 1. External resistor and capacitor may be used between pins (10), (11), and (14) to control one-shot pulse width.  
 2. To use the internal timing resistor, connect pin (9) to pin (14).  
 3. Input sensitivity can be decreased by adding a capacitor from pin (5) to ground.

### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	4.5 V to 5.5 V
Maximum Fan-Out From Each Output . . . . .	10
Input Pulse Characteristics:	
Minimum Negative-Going Transition . . . . .	1 V
Maximum Input Fall Time Per Volt . . . . .	25 ns/V
Maximum Duty Cycle . . . . .	40%

### electrical characteristics

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{out(0)}$ Logical 0 output voltage (on level)	43	$V_{CC} = 4.5 \text{ V}$ , $I_{sink} = 15 \text{ mA}$ , $T_A = 25^\circ\text{C}$ and $-55^\circ\text{C}$		0.4	V
		$V_{CC} = 4.5 \text{ V}$ , $I_{sink} = 14 \text{ mA}$ , $T_A = 125^\circ\text{C}$		0.45	V
$V_{out(1)}$ Logical 1 output voltage (off level)	44	$V_{CC} = 4.5 \text{ V}$ , $I_{load} = -0.18 \text{ mA}$ , $T_A = 25^\circ\text{C}$	2.6		V
		$V_{CC} = 4.5 \text{ V}$ , $I_{load} = -0.18 \text{ mA}$ , $T_A = 125^\circ\text{C}$ and $-55^\circ\text{C}$	2.5		V
$I_{in(1)}$ Logical 1 level input current	45	$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 4 \text{ V}$ , $T_A = 25^\circ\text{C}$ and $-55^\circ\text{C}$		2	$\mu\text{A}$
		$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 4 \text{ V}$ , $T_A = 125^\circ\text{C}$		5	$\mu\text{A}$
$I_{in(0)}$ Logical 0 level input current	46	$V_{CC} = 5.5 \text{ V}$ , $V_1 = 4 \text{ V}$ , $V_2 = 0$ , $T_A = 25^\circ\text{C}$ and $-55^\circ\text{C}$	-1.6	-3.1	mA
		$V_{CC} = 5.5 \text{ V}$ , $V_1 = 4 \text{ V}$ , $V_2 = 0$ , $T_A = 125^\circ\text{C}$	-1.4	-3	mA

†Expander node is open unless otherwise noted.

# TYPE SN15 951 MONOSTABLE MULTIVIBRATOR

## electrical characteristics (continued)

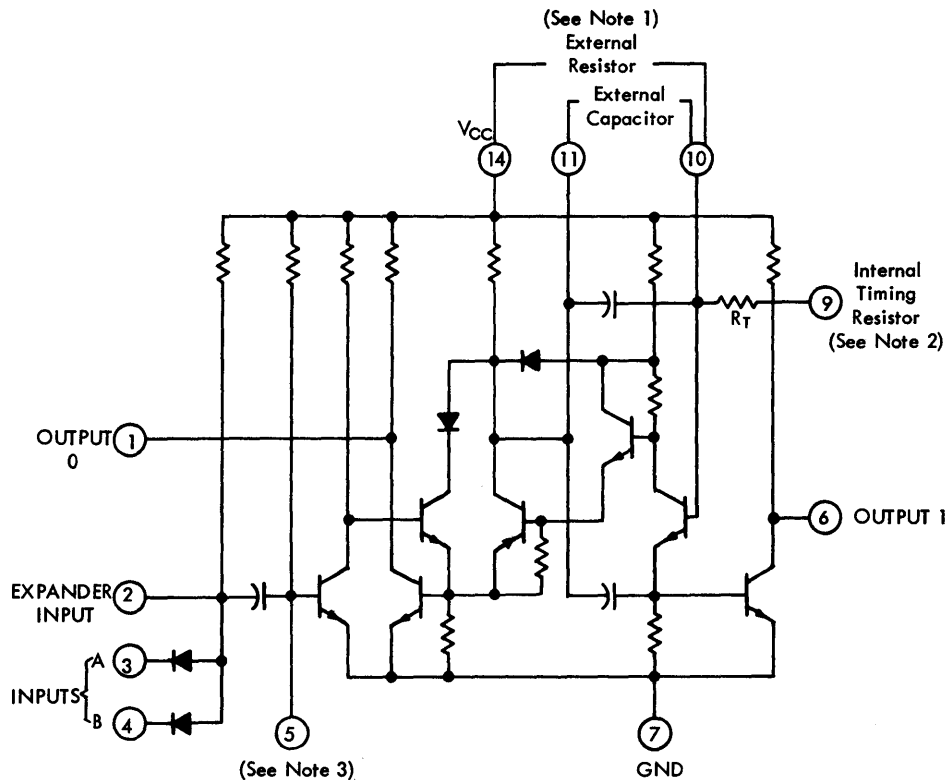
PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$I_{RT}$ Current through internal timing resistor $R_T$	47	$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 5.5 \text{ V}$ , $T_A = 25^\circ\text{C}$	0.5	0.75	mA
$I_{SC}$ Short-circuit current at expander node or pin (11)	48	$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 0$ , $T_A = 25^\circ\text{C}$ and $-55^\circ\text{C}$	-0.8		mA
		$V_{CC} = 5.5 \text{ V}$ , $V_{in} = 0$ , $T_A = 125^\circ\text{C}$	-0.75		mA
$I_{CC}$ Supply current	49	$V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$		9	mA
$I_{CC(max)}$ Supply current at maximum $V_{CC}$	50	$V_{CC} = 8 \text{ V}$ , $T_A = 25^\circ\text{C}$		20	mA

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$t_{pd(0)}$ Propagation delay time to logical 0 level	54	$R_T = 300 \Omega$ , $C_L = 50 \text{ pF}$		50	ns
$t_{pd(1)}$ Propagation delay time to logical 1 level				50	ns
$t_p$ Pulse width			90	160	ns

† Expander node is open unless otherwise noted.

## schematic

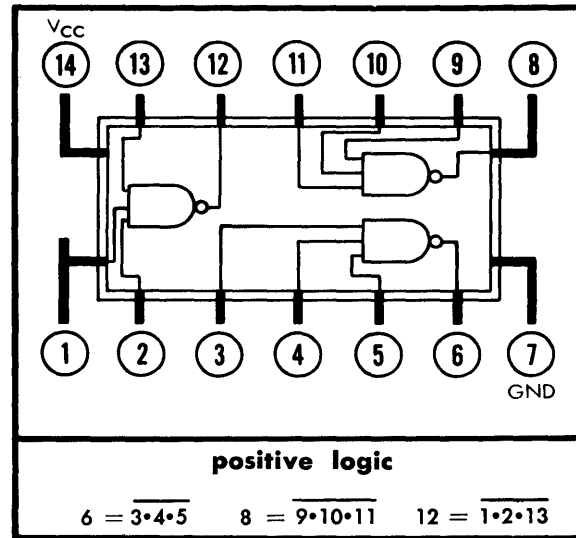
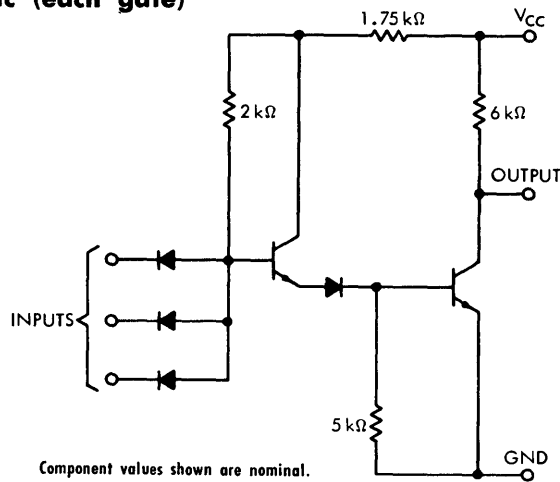


- NOTES: 1. External resistor and capacitor may be used (as indicated above) between pins (10), (11), and (14) to control one-shot pulse width.  
 2. To use the internal timing resistor, connect pin (9) to pin (14).  
 3. Input sensitivity can be decreased by adding a capacitor from pin (5) to ground.

# TYPE SN15 962

## TRIPLE 3-INPUT NAND/NOR GATE

schematic (each gate)



### recommended operating conditions

Supply Voltage  $V_{CC}$  . . . . . 4.5 V to 5.5 V  
 Maximum Fan-Out From Each Output . . . . . 8

### electrical characteristics

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$ Logical 0 output voltage (on level)	1	$V_{CC} = 4.5 \text{ V}, V_{in} = 1.9 \text{ V}, I_{sink} = 12 \text{ mA}, T_A = 25^\circ\text{C}$		0.4	V
		$V_{CC} = 4.5 \text{ V}, V_{in} = 2.1 \text{ V}, I_{sink} = 11.4 \text{ mA}, T_A = -55^\circ\text{C}$		0.4	V
		$V_{CC} = 4.5 \text{ V}, V_{in} = 1.7 \text{ V}, I_{sink} = 10.8 \text{ mA}, T_A = 125^\circ\text{C}$		0.45	V
$V_{out(1)}$ Logical 1 output voltage (off level)	2	$V_{CC} = 4.5 \text{ V}, V_{in} = 1.1 \text{ V}, I_{load} = -0.12 \text{ mA}, T_A = 25^\circ\text{C}$	2.6		V
		$V_{CC} = 4.5 \text{ V}, V_{in} = 1.4 \text{ V}, I_{load} = -0.12 \text{ mA}, T_A = -55^\circ\text{C}$	2.5		V
		$V_{CC} = 4.5 \text{ V}, V_{in} = 0.8 \text{ V}, I_{load} = -0.12 \text{ mA}, T_A = 125^\circ\text{C}$	2.5		V

# TYPE SN15 962 TRIPLE 3-INPUT NAND/NOR GATE

## electrical characteristics (continued)

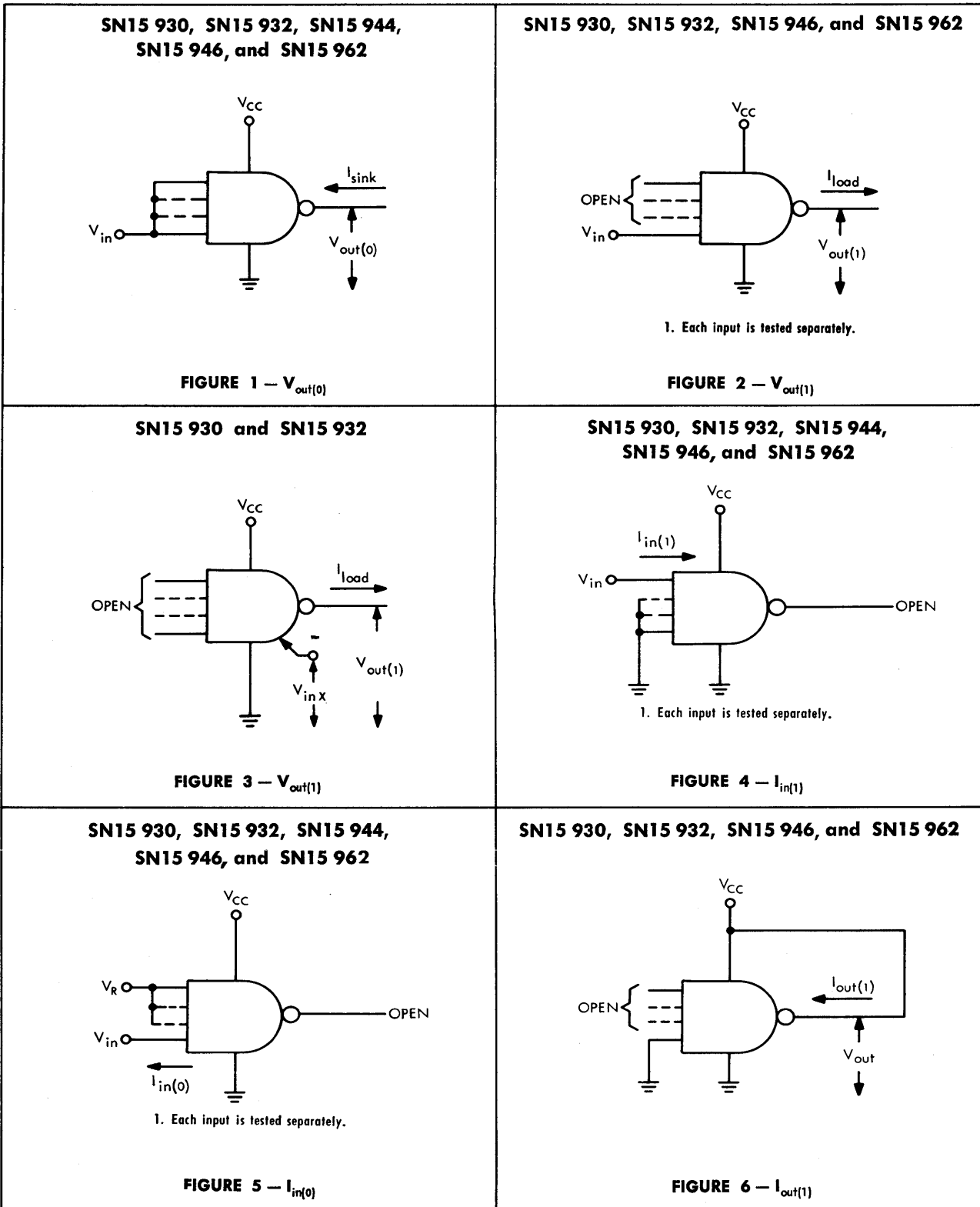
PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$ Logical 1 level input current	4	$V_{CC} = 5.5 \text{ V}, V_{in} = 4 \text{ V}, T_A = 25^\circ\text{C and } -55^\circ\text{C}$		2	$\mu\text{A}$
		$V_{CC} = 5.5 \text{ V}, V_{in} = 4 \text{ V}, T_A = 125^\circ\text{C}$		5	$\mu\text{A}$
$I_{in(0)}$ Logical 0 level input current	5	$V_{CC} = 5.5 \text{ V}, V_{in} = 0, V_R = 4 \text{ V}, T_A = 25^\circ\text{C and } -55^\circ\text{C}$		-1.6	mA
		$V_{CC} = 5.5 \text{ V}, V_{in} = 0, V_R = 4 \text{ V}, T_A = 125^\circ\text{C}$		-1.5	mA
$I_{out(1)}$ Output reverse current (off level)	6	$V_{CC} = V_{out} = 4.5 \text{ V}, T_A = 25^\circ\text{C}$		50	$\mu\text{A}$
$I_{OS}$ Short-circuit output current	7	$V_{CC} = 5.5 \text{ V}, V_{out} = 0, T_A = 25^\circ\text{C}$	-0.6	-1.34	mA
		$V_{CC} = 5.5 \text{ V}, V_{out} = 0, T_A = -55^\circ\text{C}$		-1.34	mA
		$V_{CC} = 5.5 \text{ V}, V_{out} = 0, T_A = 125^\circ\text{C}$		-1.3	mA
$I_{CC(0)}$ Logical 0 level supply current (all gates)	8	$V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$		9.75	mA
$I_{CC(1)}$ Logical 1 level supply current at maximum $V_{CC}$ (all gates)	9	$V_{CC} = 8 \text{ V}, T_A = 25^\circ\text{C}$		8.25	mA

## switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$ Propagation delay time to logical 0 level	51	$R_1 = 400 \Omega, C_L = 50 \text{ pF}$	10	30	ns
$t_{pd(1)}$ Propagation delay time to logical 1 level		$R_1 = 3.9 \text{ k}\Omega, C_L = 30 \text{ pF}$	25	80	ns

**PARAMETER MEASUREMENT INFORMATION**

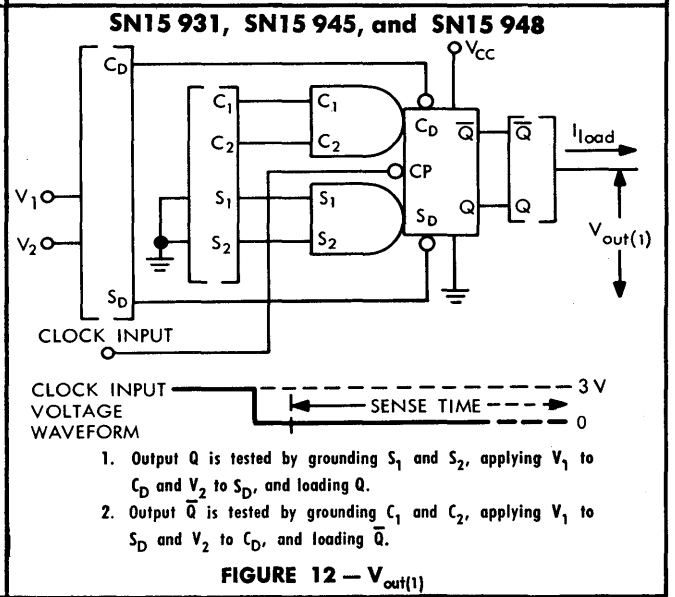
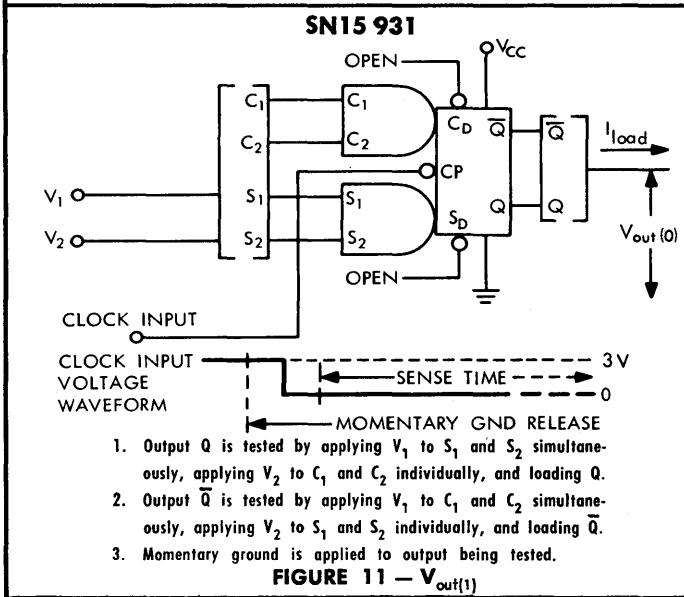
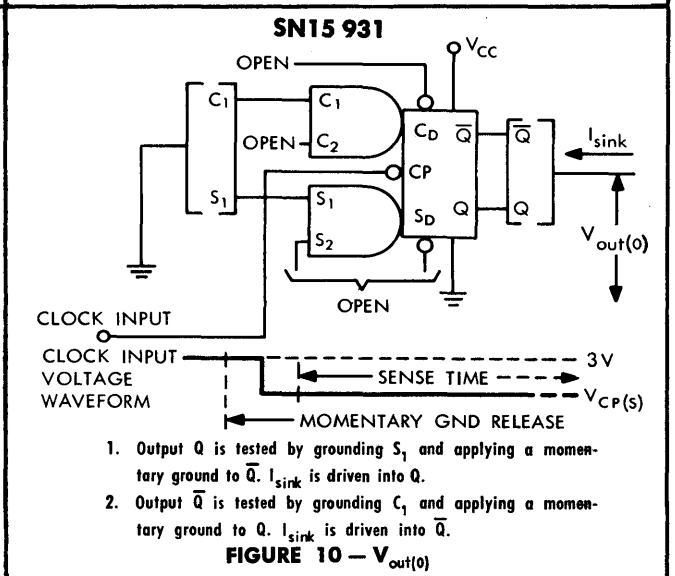
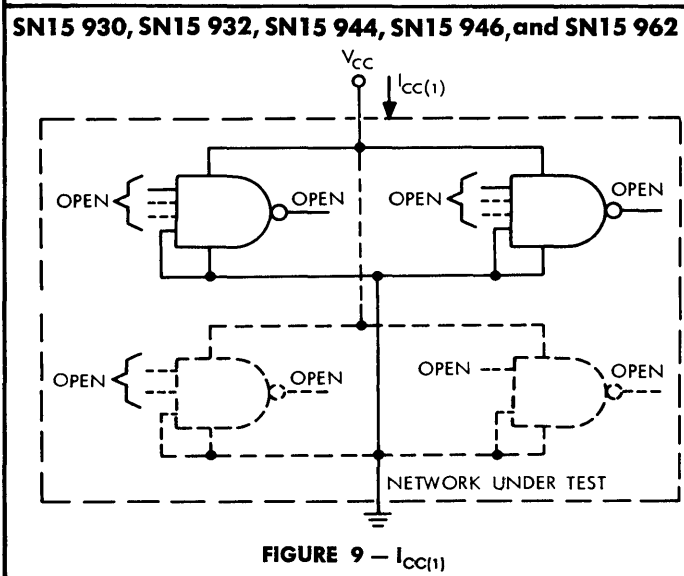
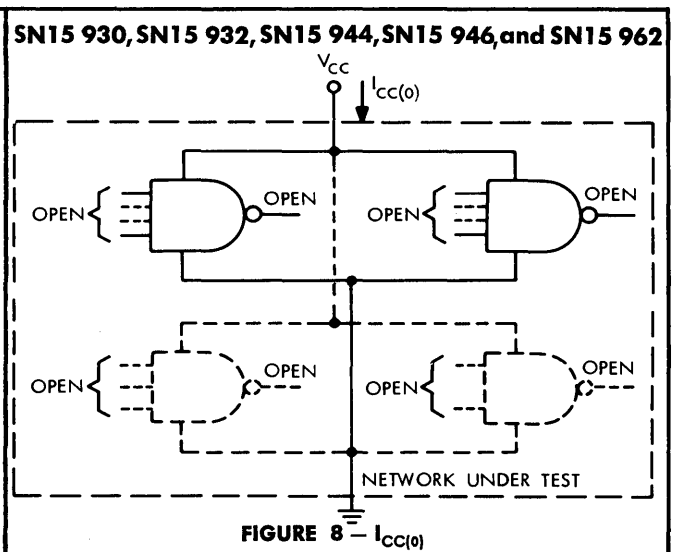
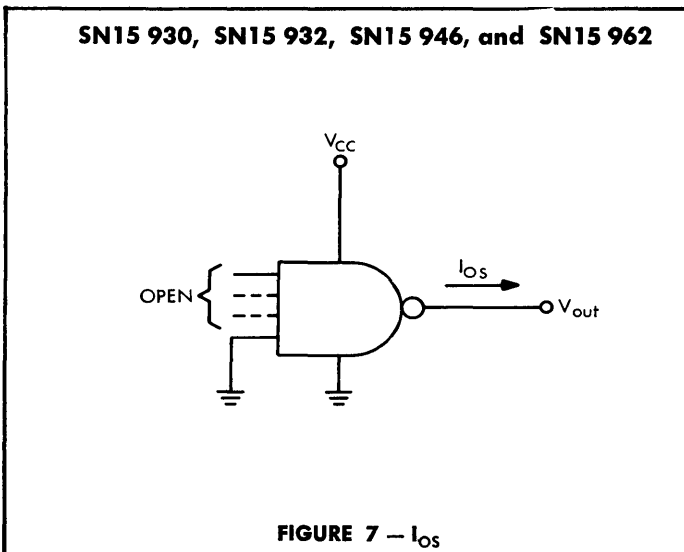
d-c test circuits †



† Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

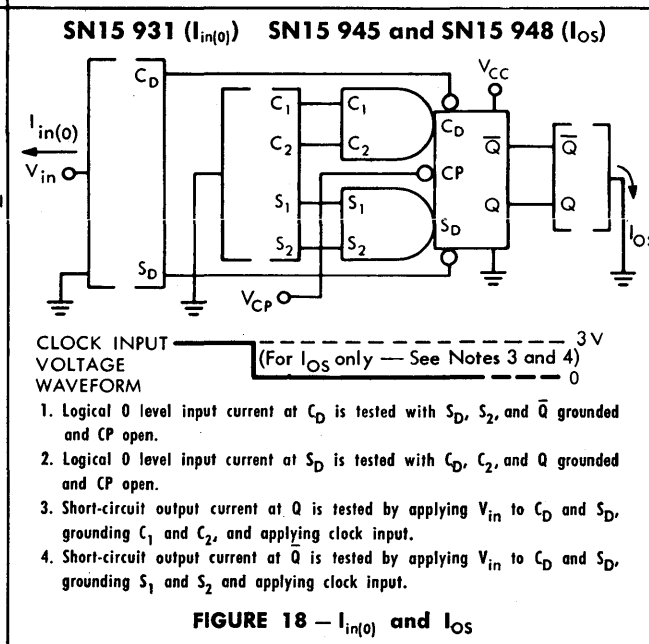
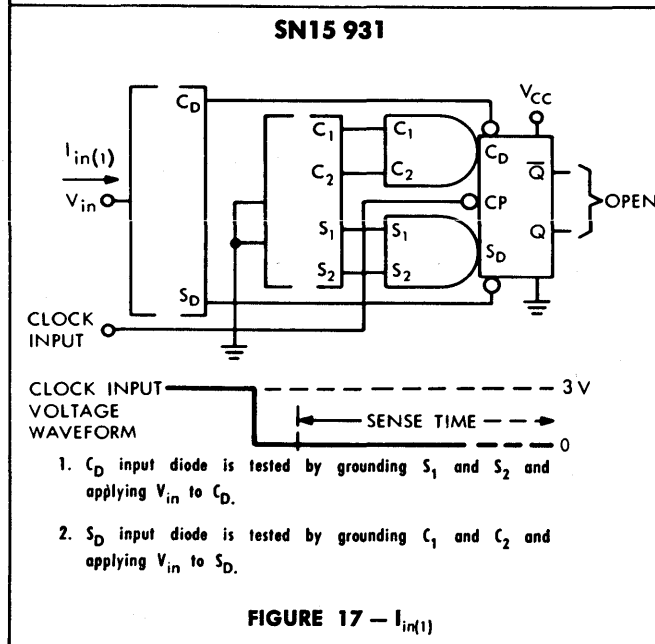
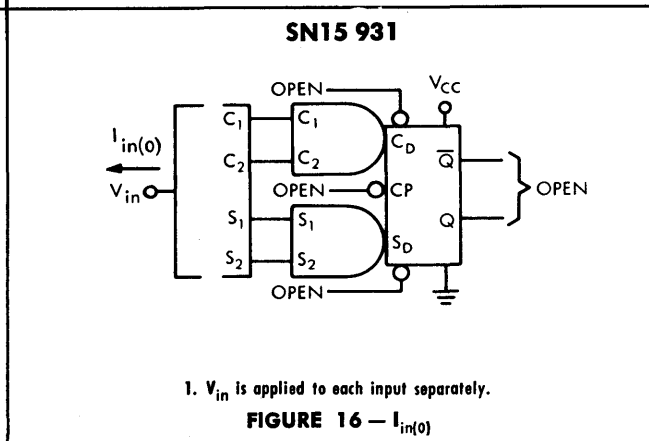
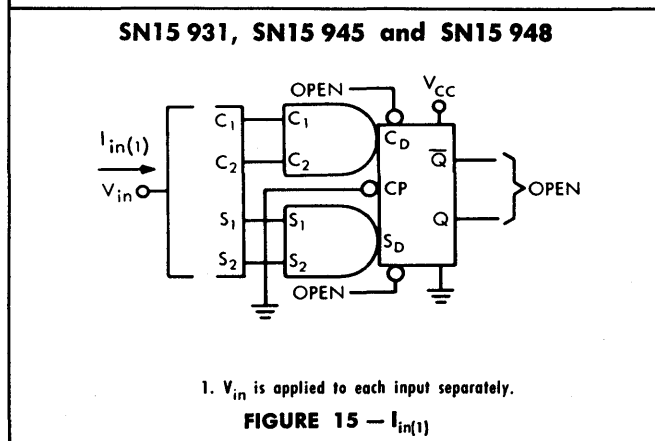
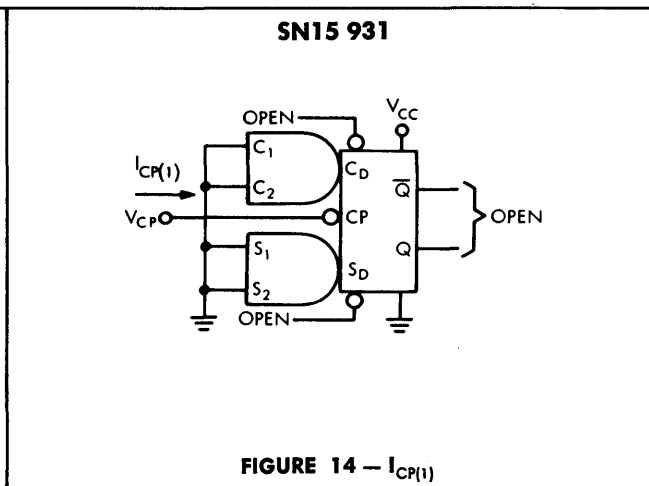
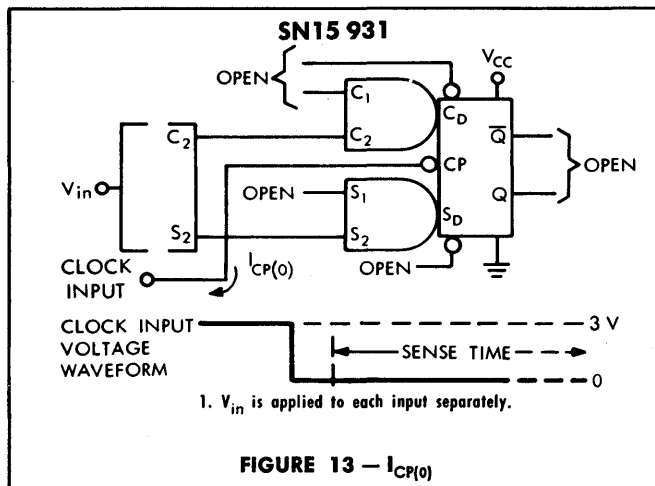
d-c test circuits<sup>†</sup> (continued)



<sup>†</sup> Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

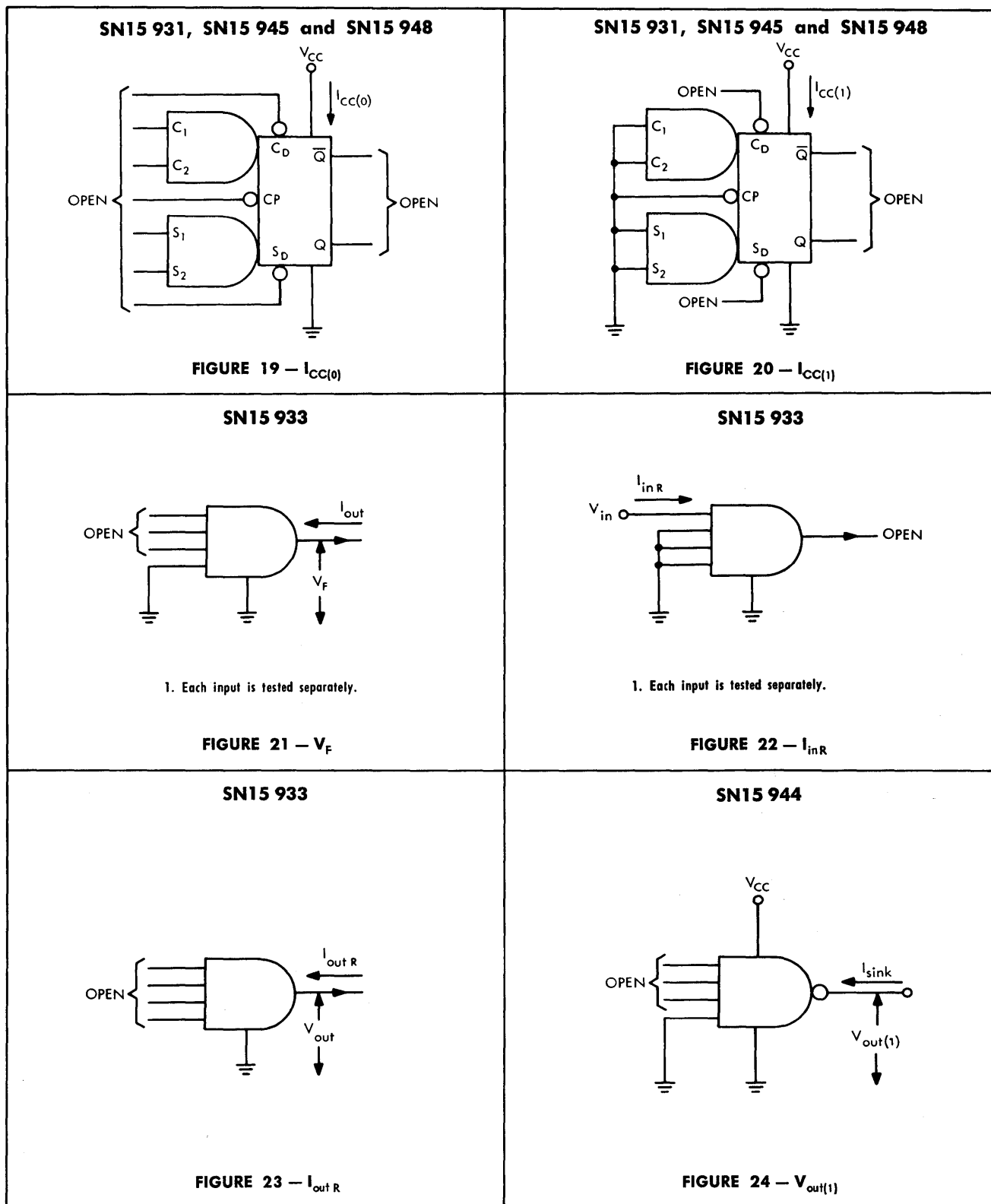
d-c test circuits<sup>†</sup> (continued)



<sup>†</sup> Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

d-c test circuits<sup>†</sup> (continued)

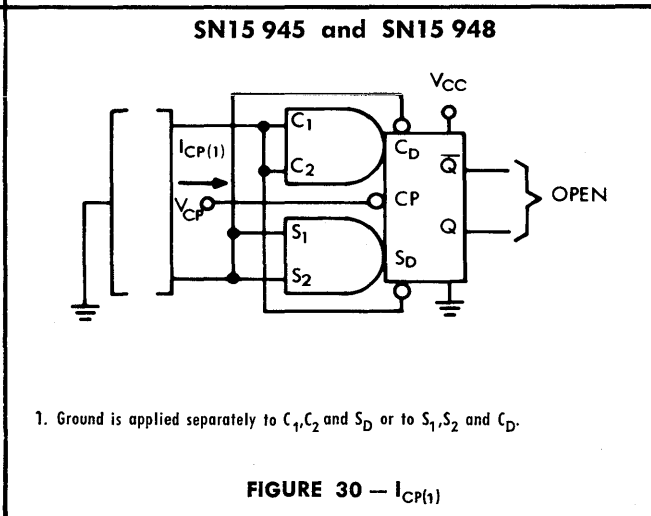
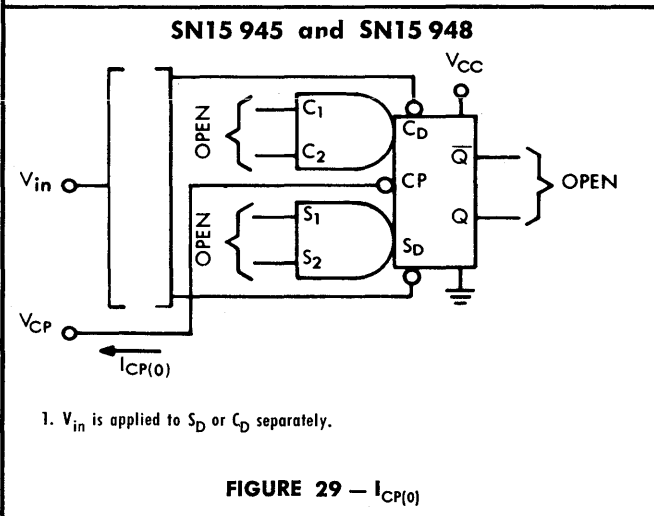
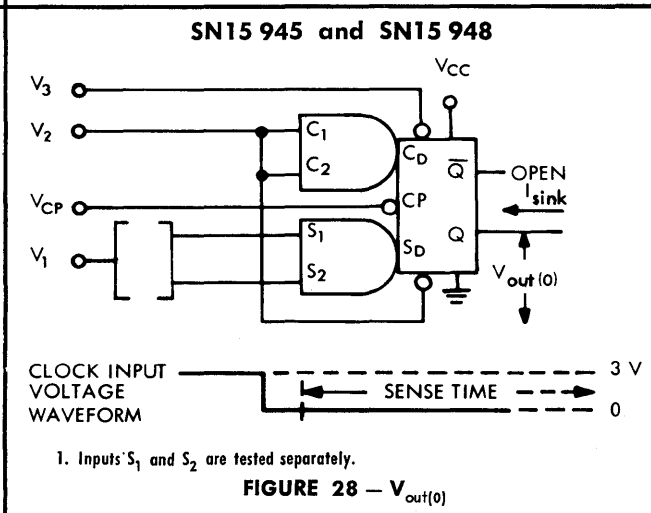
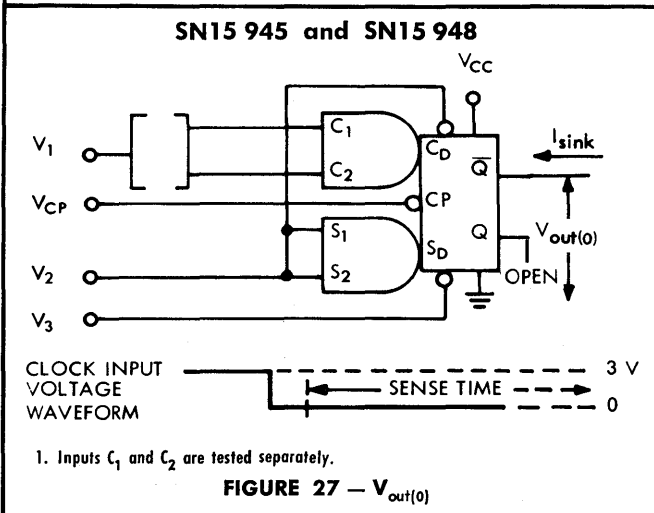
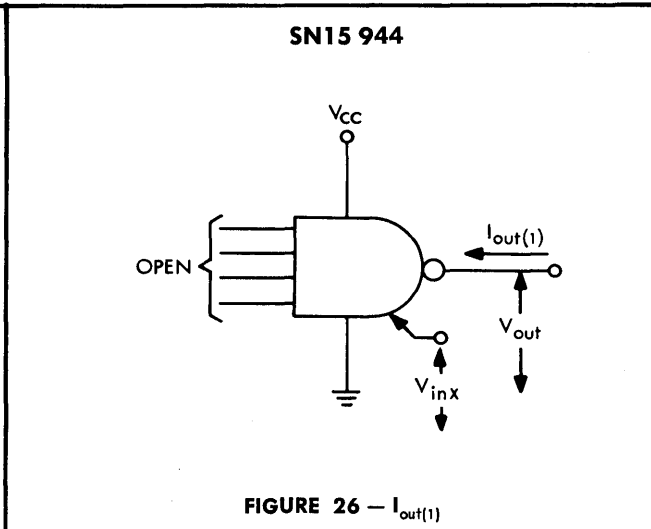
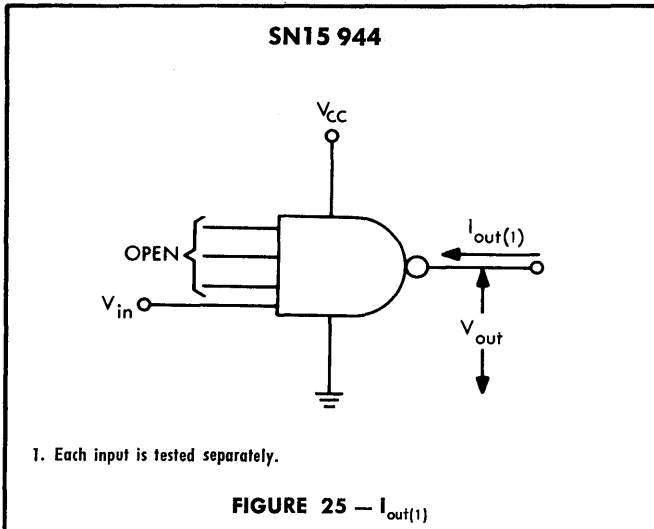


<sup>†</sup> Arrows indicate actual direction of current flow.



**PARAMETER MEASUREMENT INFORMATION**

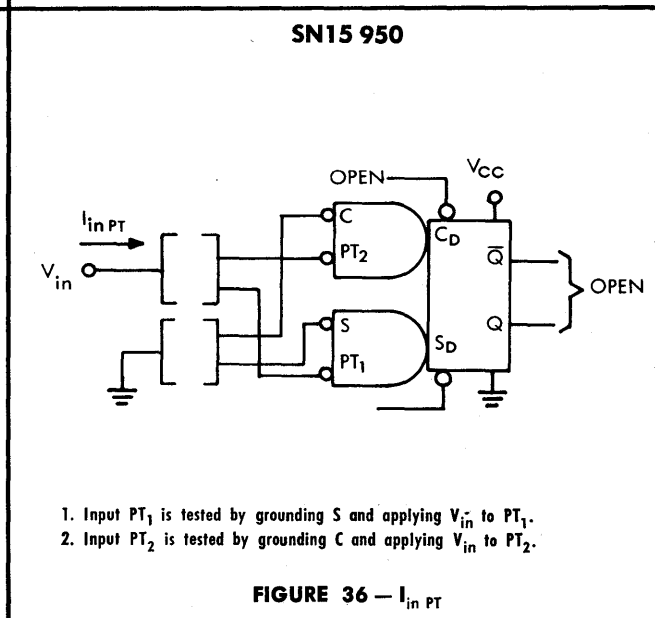
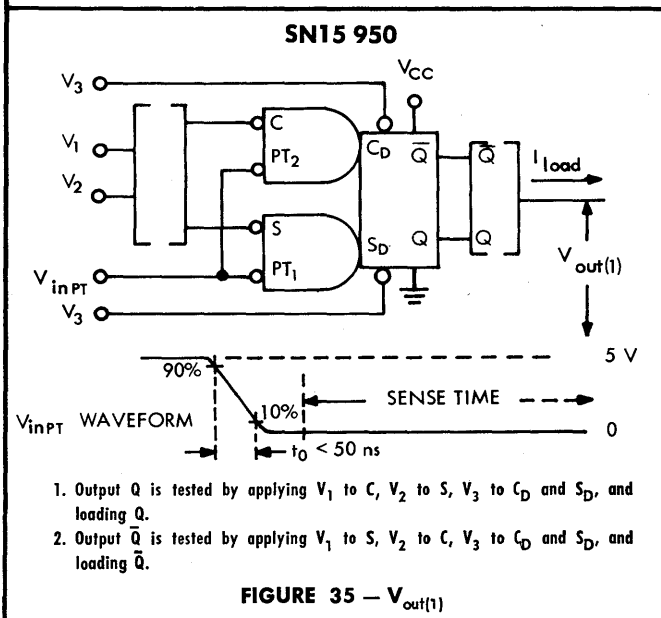
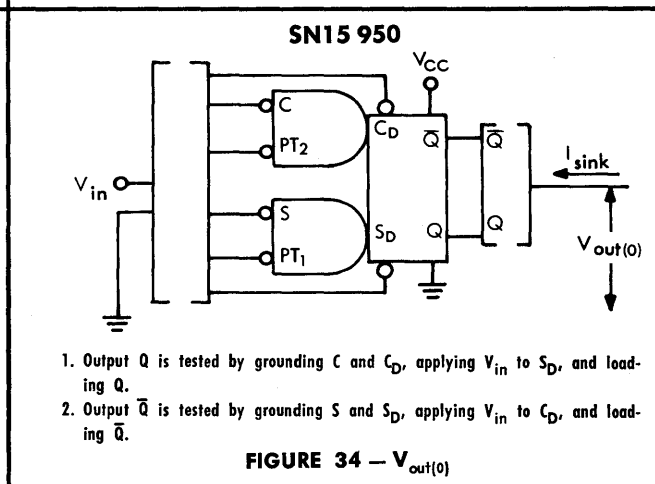
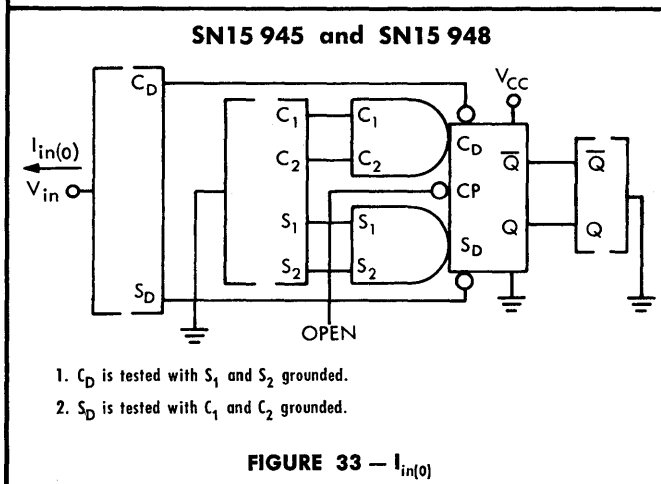
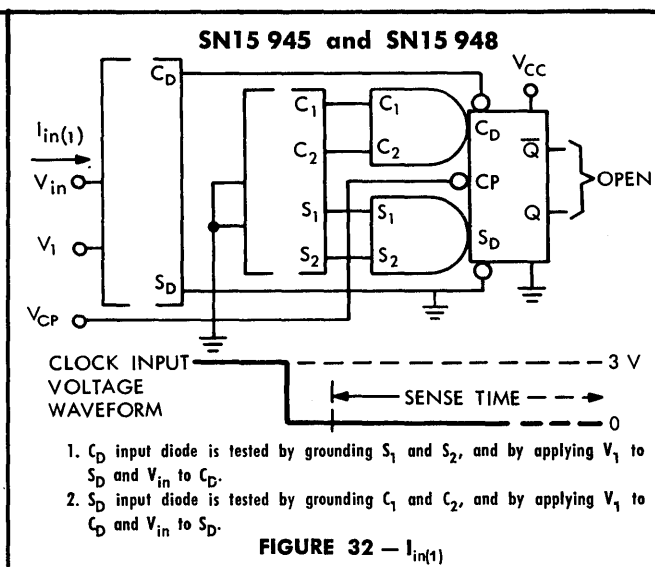
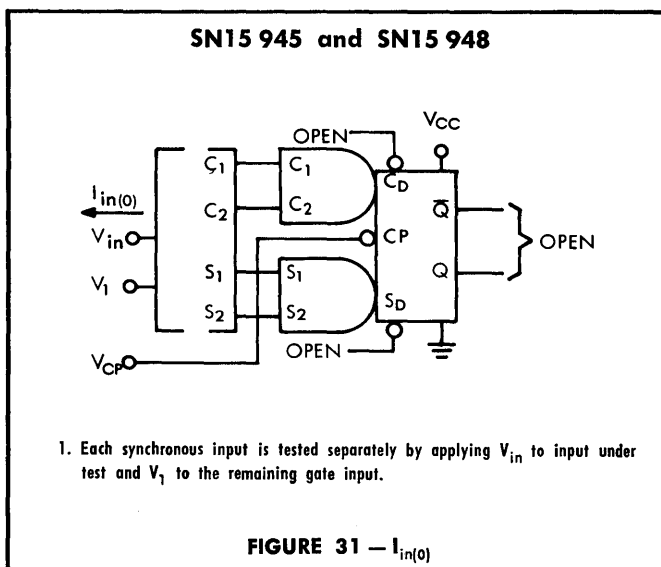
d-c test circuits † (continued)



†Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

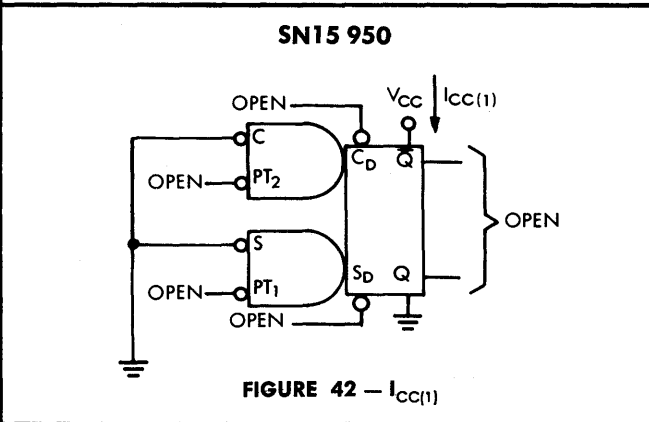
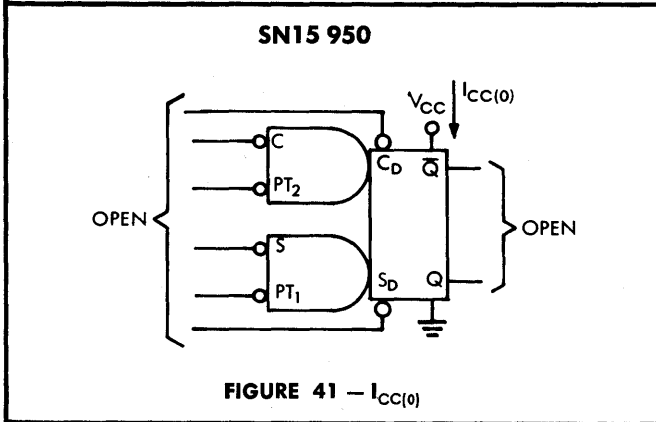
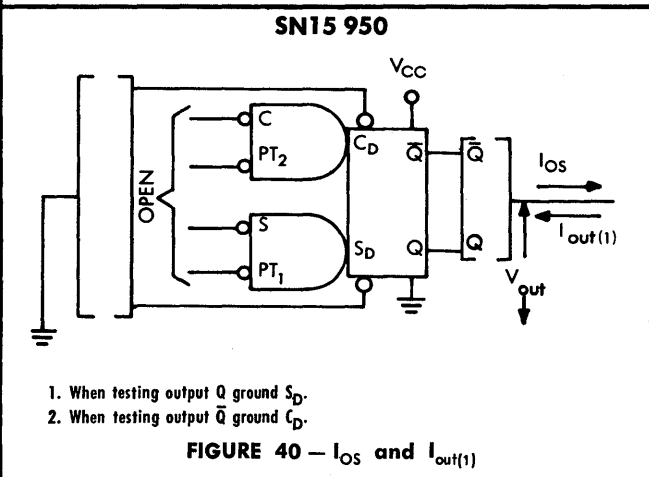
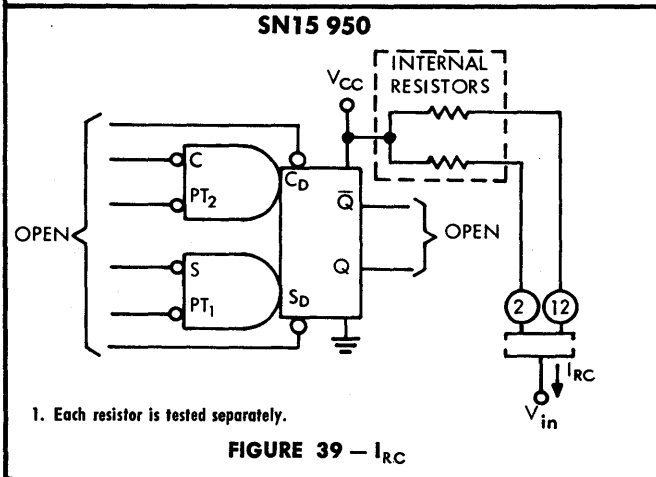
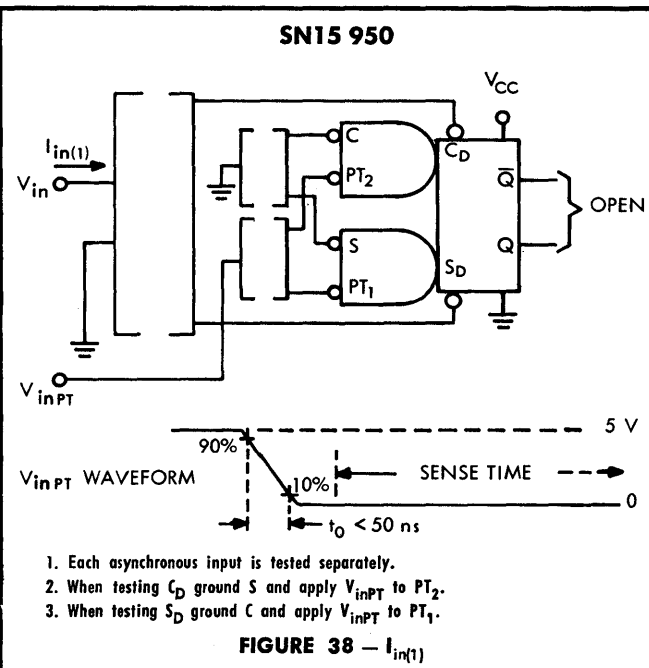
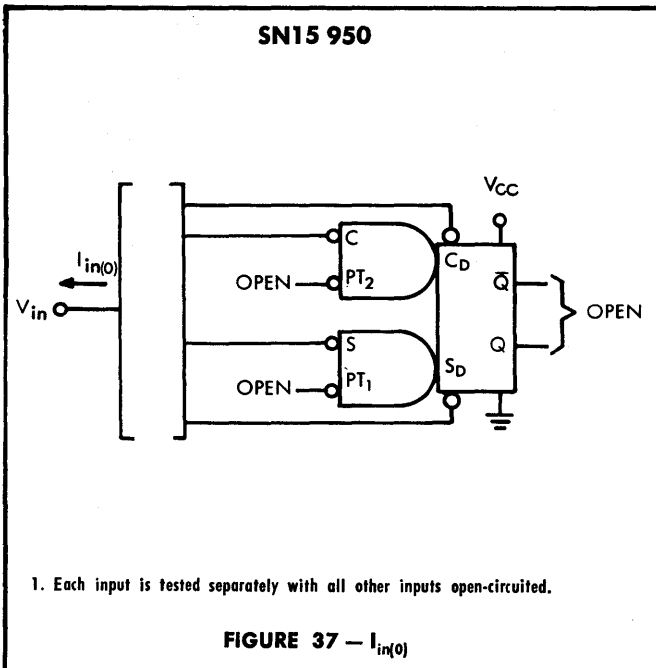
d-c test circuits<sup>†</sup> (continued)



<sup>†</sup>Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

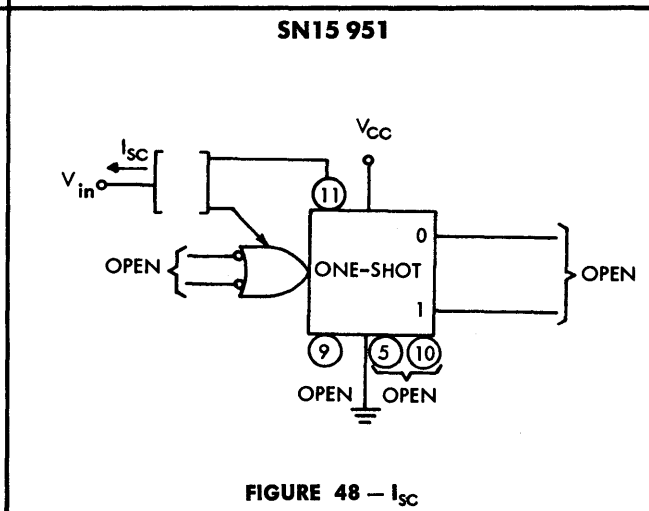
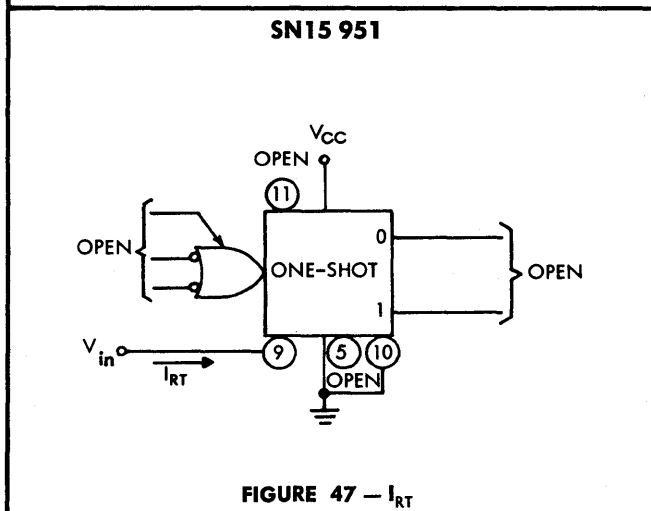
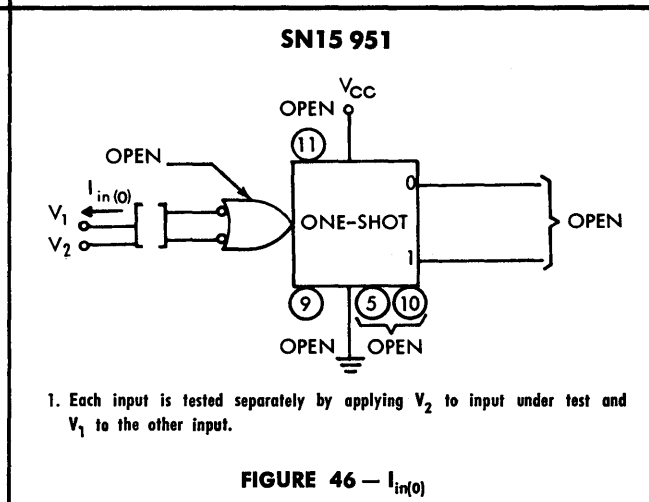
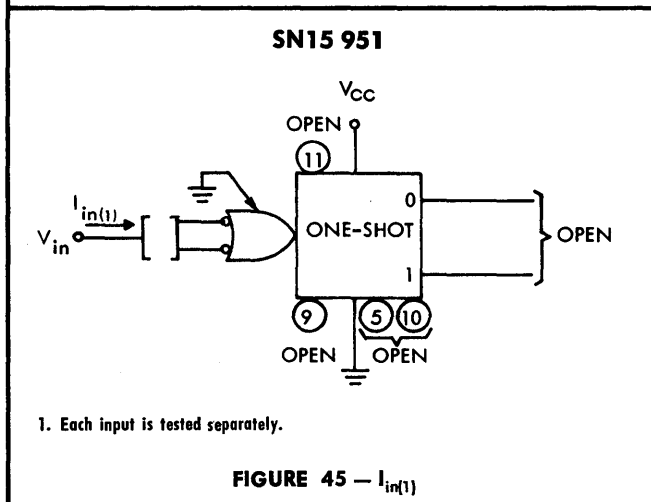
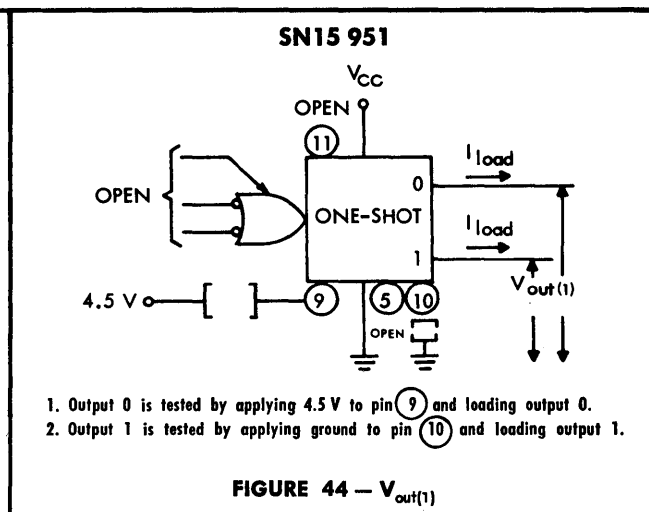
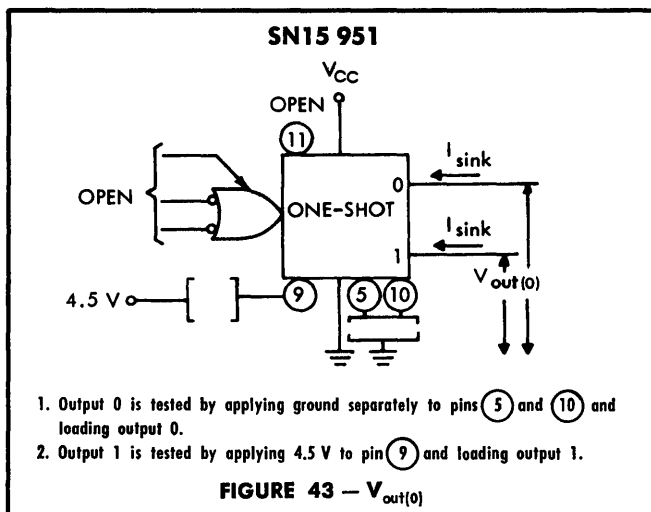
d-c test circuits<sup>†</sup> (continued)



<sup>†</sup>Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

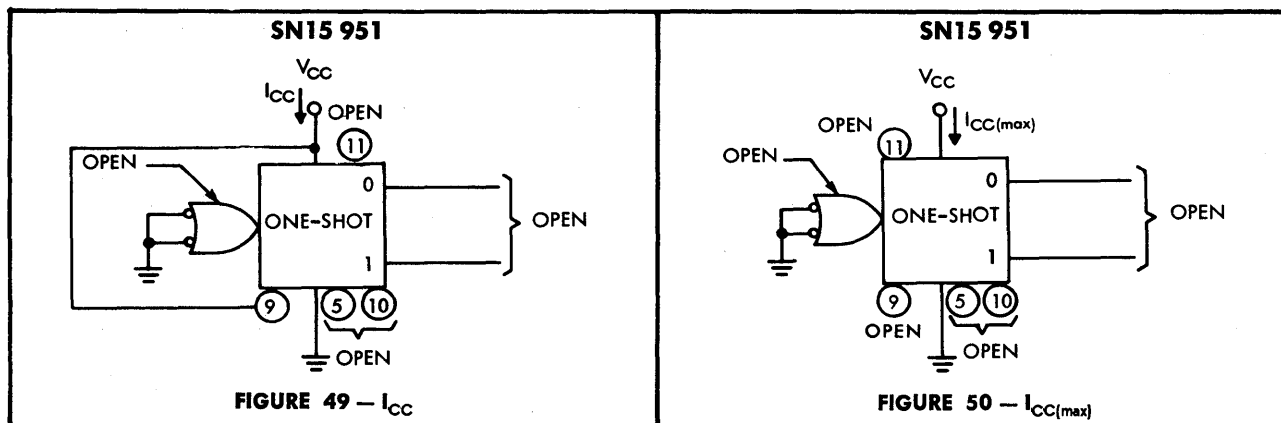
d-c test circuits<sup>†</sup> (continued)



<sup>†</sup>Arrows indicate actual direction of current flow.

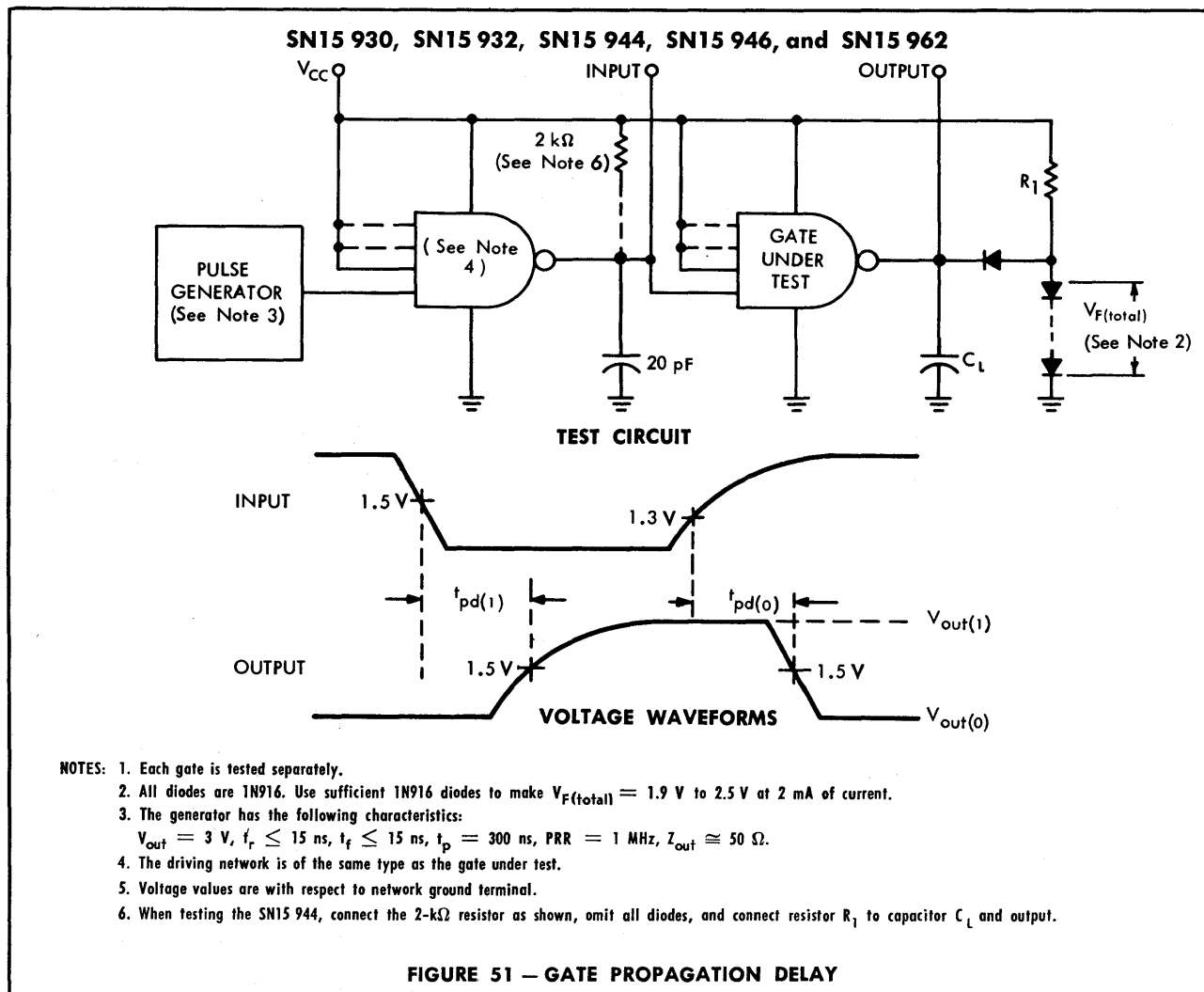
**PARAMETER MEASUREMENT INFORMATION**

d-c test circuits<sup>†</sup> (continued)



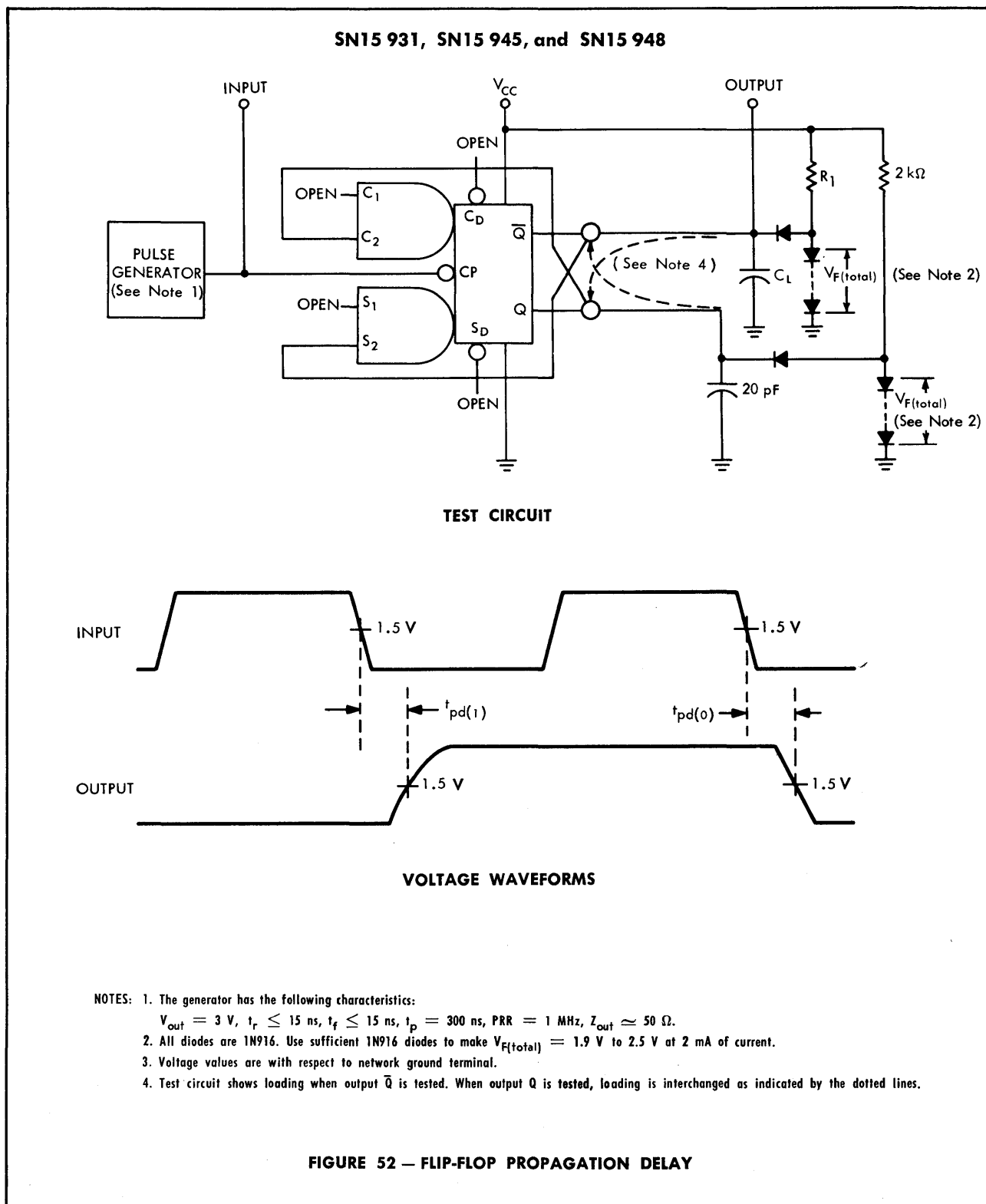
<sup>†</sup>Arrows indicate actual direction of current flow.

**switching characteristics**



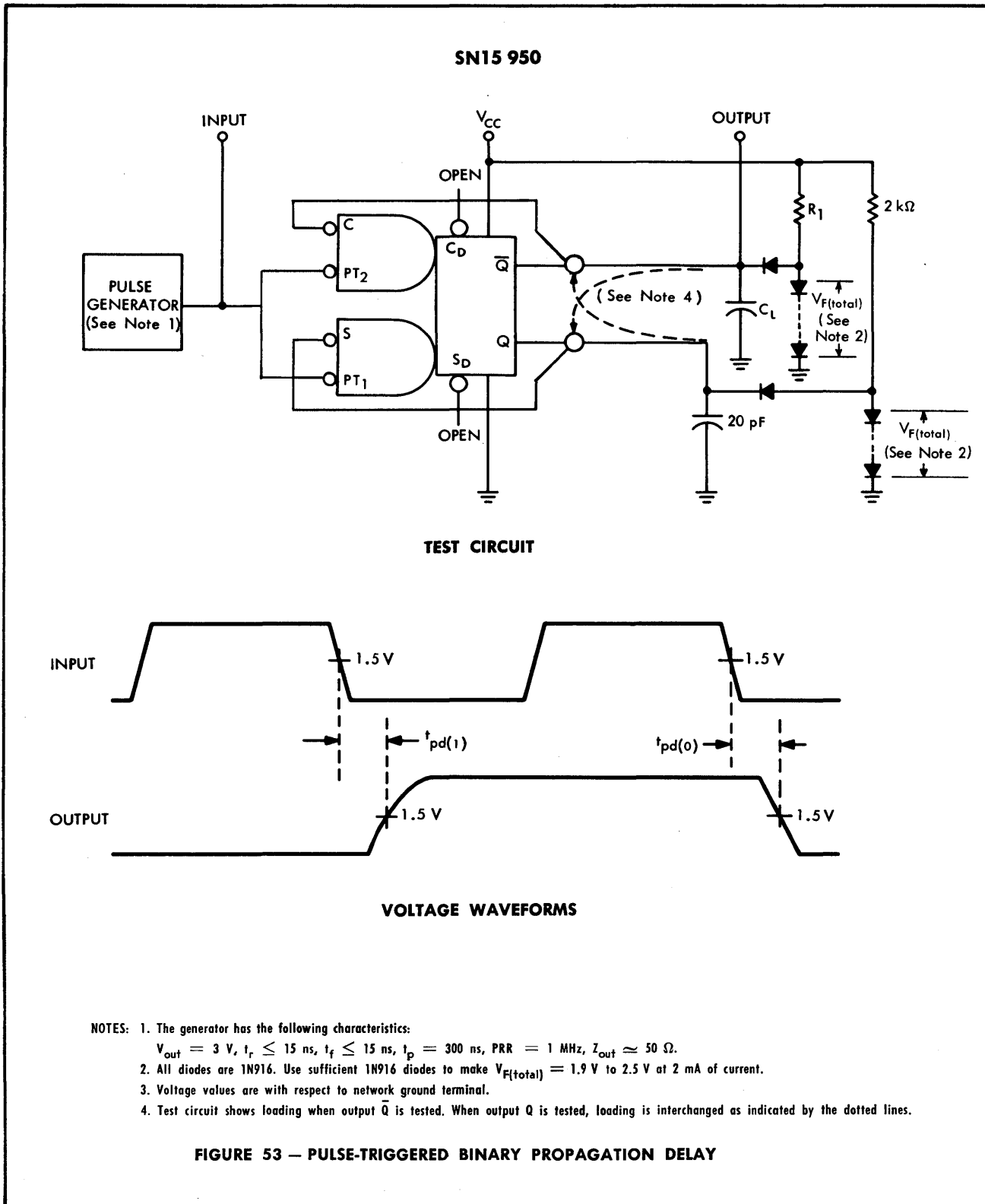
**PARAMETER MEASUREMENT INFORMATION**

switching characteristics (continued)

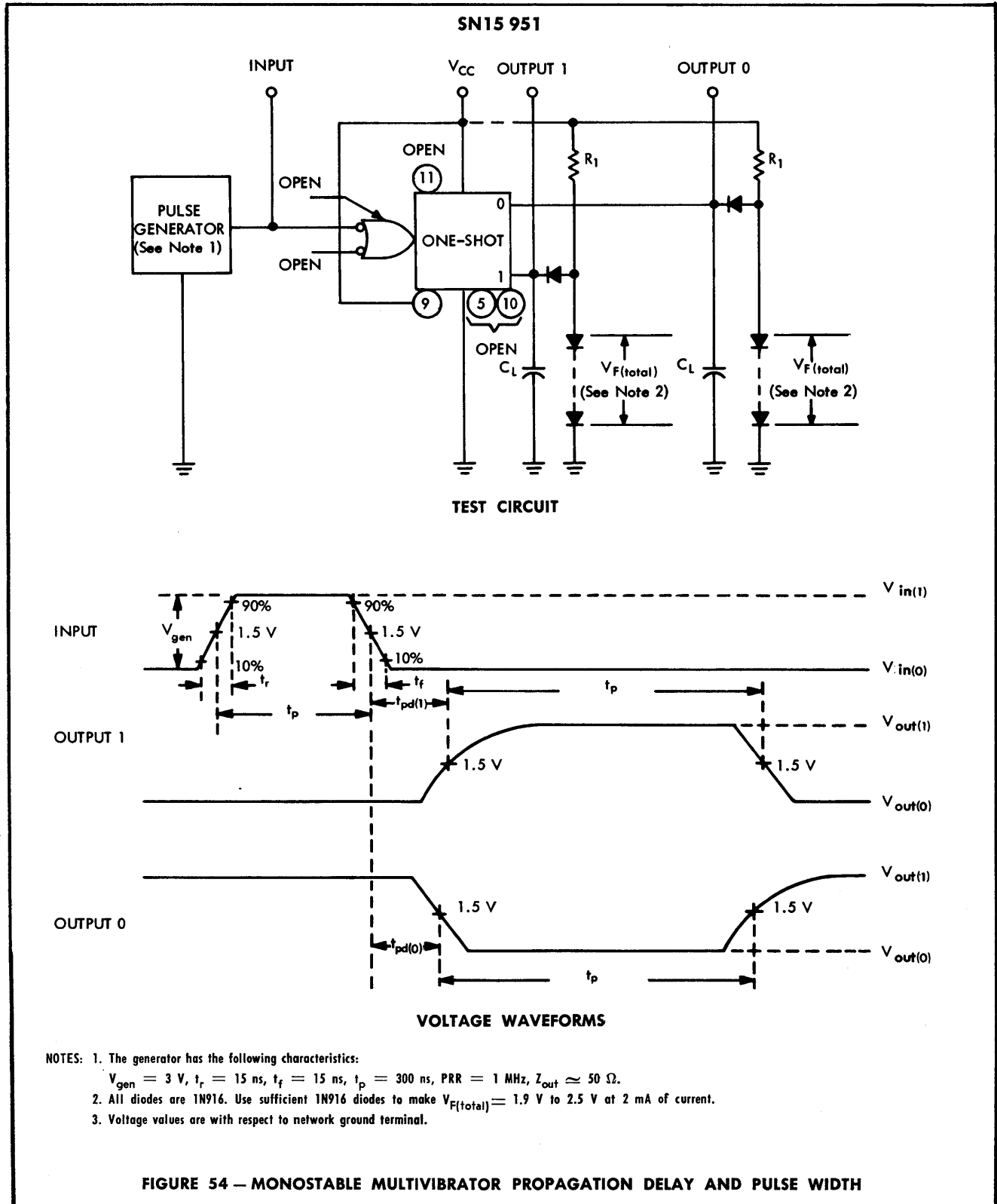


**SERIES 15930**  
**SOLID CIRCUIT<sup>®</sup> SEMICONDUCTOR NETWORKS**

**switching characteristics (continued)**



**switching characteristics (continued)**



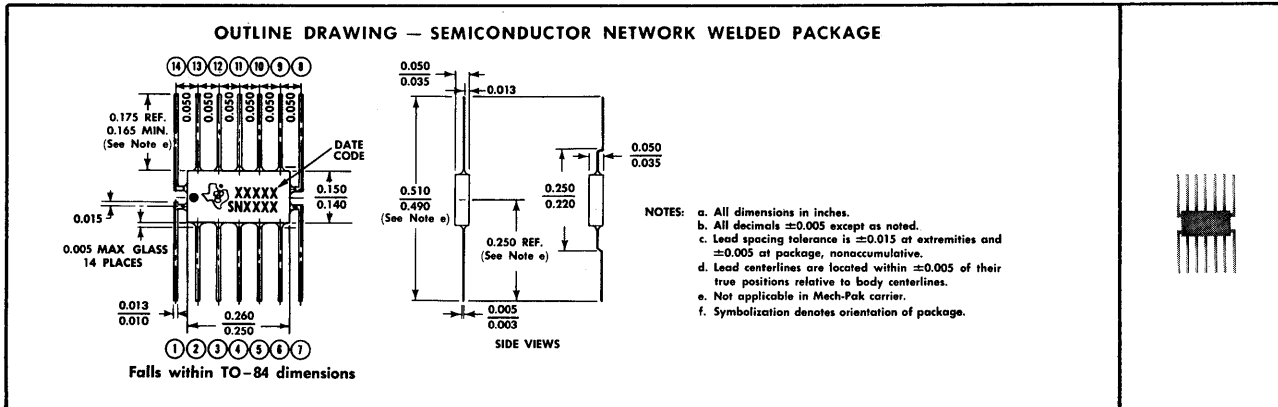


**MECHANICAL DATA**

**general**

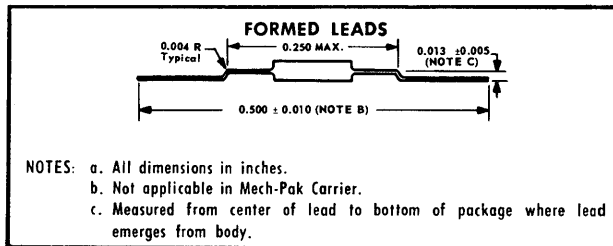
SOLID CIRCUIT semiconductor networks are mounted in a glass-to-metal hermetically sealed, welded package. Package body and leads are gold-plated F-15<sup>‡</sup> glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are

metallic and are insulated from leads and circuit. All Series 15 930 networks are available with formed leads, insulator attached, and/or mounted in a Mech-Pack carrier.



**leads**

Gold-plated F-15<sup>‡</sup> leads require no additional cleaning or processing when used in soldered or welded assembly. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Standard lead length is 0.175 inches. Networks can be removed from Mech-Pak carriers with lead lengths up to 0.175 inches.

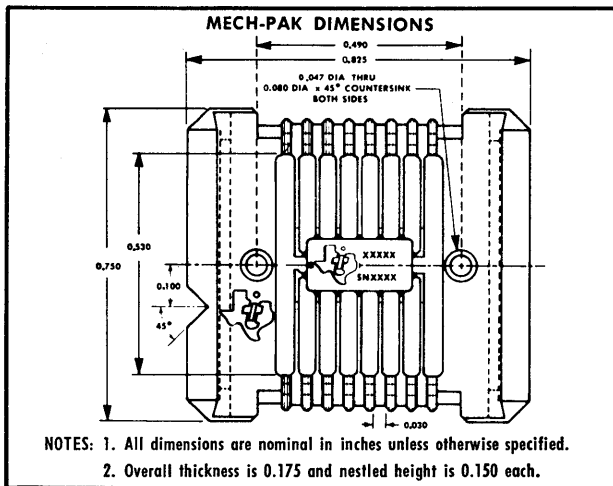


**insulator**

An insulator, secured to the back surface of the package, permits mounting networks on circuit boards which have conductors passing beneath the package. The insulator is 0.0025 inches thick and has an insulation resistance of greater than 10 megohms at 25°C.

**mech-pak carrier**

The Mech-Pak carrier facilitates handling the network, and is compatible with automatic equipment used for testing and assembly. The carrier is particularly appropriate for mechanized assembly operations and will withstand temperatures of 125°C for indefinite periods.



**ordering instructions**

Variations in mechanical configuration of semiconductor networks are identified by suffix numbers shown in a table at the right.

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5

<sup>†</sup>Patented by Texas Instruments

<sup>‡</sup>F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.



**SERIES 52 OPERATIONAL AMPLIFIERS**

*for application in*

**Military & Industrial Control Systems • Analog-to-Digital Convertors • Analog Computers**

**Improved Version of SN521 and SN522**

TYPES SN521A, SN522A  
BULLETIN NO. D.L.S. 639468, JANUARY 1963  
REVISED OCTOBER 1966

**description**

Each of these networks is a general-purpose operational amplifier. The SN521A single-ended amplifier has both inverting and noninverting inputs. The SN522A, in addition to both types of inputs, features a single-ended output with higher output current drive capability.

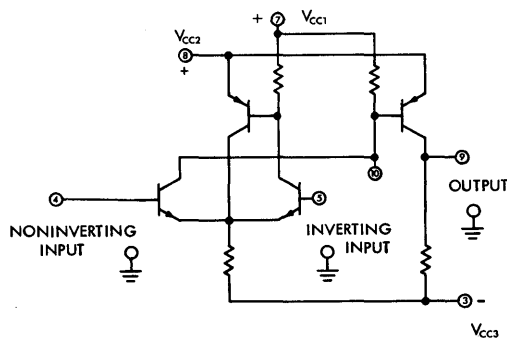
The SN521A and SN522A, two of Texas Instruments Series 52 catalog line integrated circuits, offer higher reliability, lower cost, smaller size, and lower weight than equivalent discrete component circuits. Each Series 52 device is a monolithic semiconductor structure comprising diffused resistors and both n-p-n and p-n-p transistors.

**typical operating characteristics and conditions**

Open-loop voltage gain . . . . .	62 db
Common-mode rejection . . . . .	60 db
Dynamic output voltage range . . . . .	±2.5 v
Frequency response . . . . .	DC to 50 kc
Operating ambient temperature range . . . . .	-55°C to 125°C
Supply voltages: V <sub>CC1</sub> . . . . .	+10 v
V <sub>CC2</sub> . . . . .	+6 v
V <sub>CC3</sub> . . . . .	-9 v

**circuit diagrams**

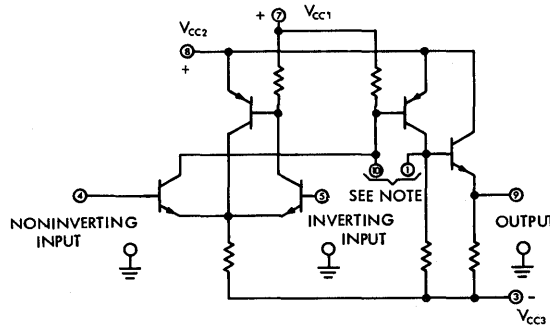
**CIRCUIT DIAGRAM SN521A**



NOTES: PIN ⑩ IS FOR FREQUENCY SHAPING  
PINS ①, ②, AND ③ — NO INTERNAL CONNECTION

†Patented by Texas Instruments

**CIRCUIT DIAGRAM SN522A**



NOTES: PINS ⑩ AND ① ARE FOR FREQUENCY SHAPING  
PINS ② AND ③ — NO INTERNAL CONNECTION



# TYPES SN521A, SN522A

## GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

### absolute maximum ratings

Supply Voltages: $V_{CC1}$ . . . . .	+15 v
$V_{CC2}$ . . . . .	+10 v
$V_{CC3}$ . . . . .	-15 v
Input Voltage (Common-Mode) . . . . .	$\pm 4$ v
Operating Ambient Temperature Range . . . . .	-55°C to 125°C
Storage Temperature Range . . . . .	-65°C to 150°C

### electrical characteristics over operating ambient temperature range (unless otherwise noted)

All measurements shown are with amplifier in the open-loop condition and with the following supply voltages:  $V_{CC1} = +10$  v  $\pm 0.2$  v;  $V_{CC2} = +6$  v  $\pm 0.2$  v;  $V_{CC3} = -9$  v  $\pm 0.2$  v.

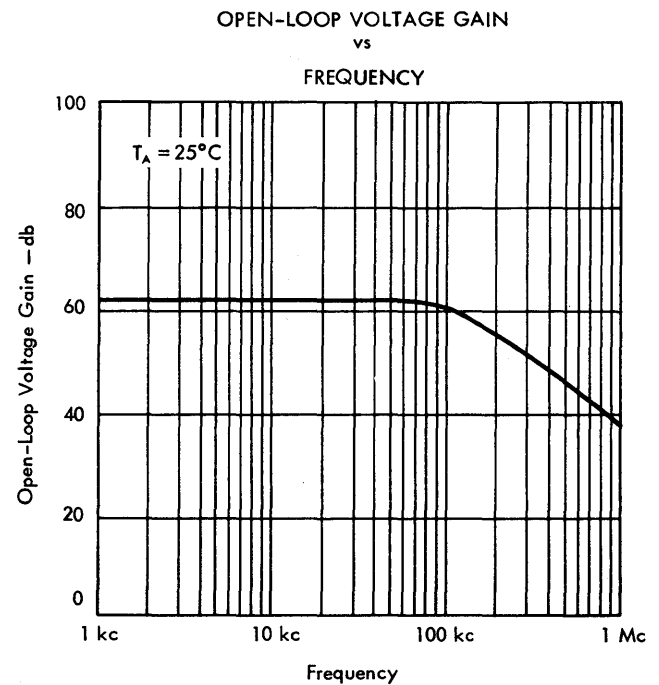
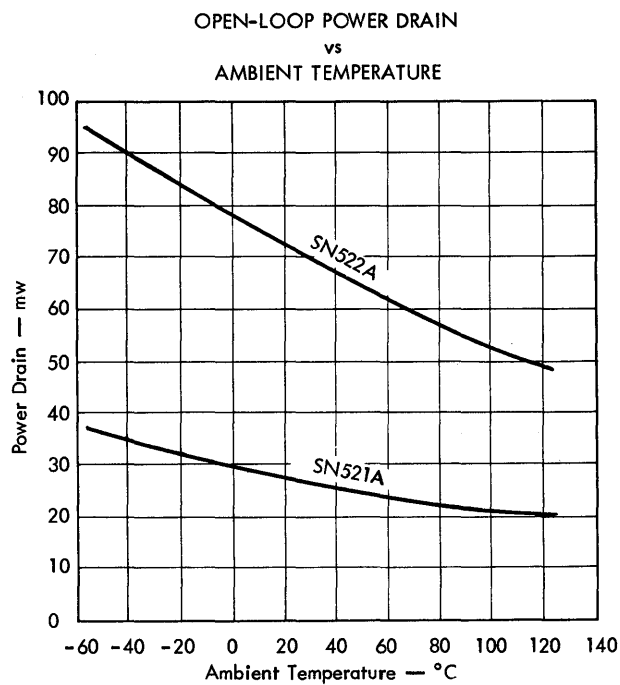
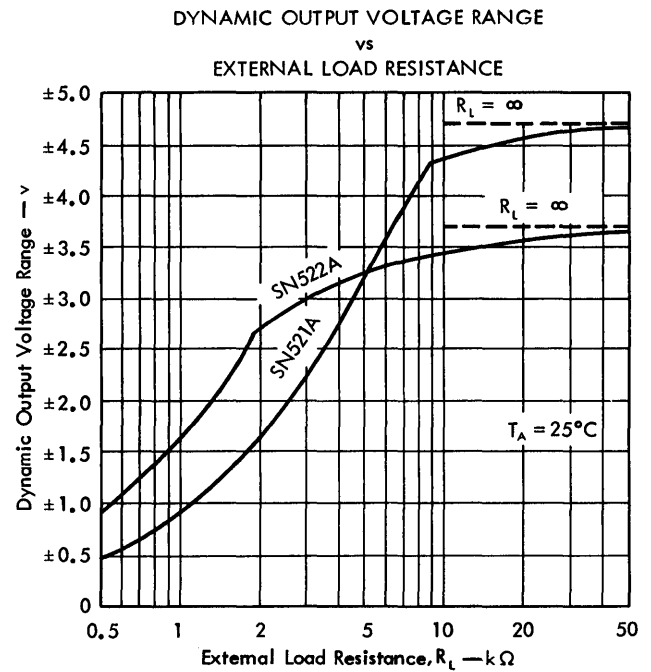
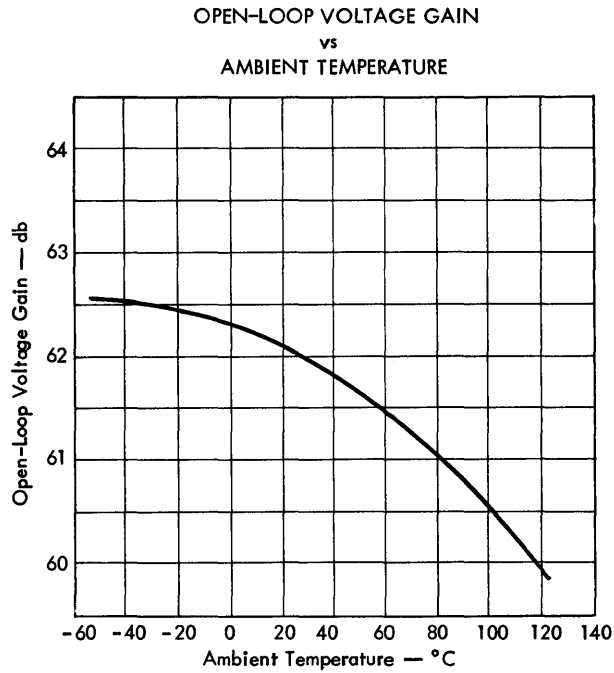
	SN521A			SN522A			
	Min	Typ	Max	Min	Typ	Max	Units
Voltage Gain, Open Loop Output Voltage, $E_o = 1$ v rms; $f = 1$ kc	54	62		54	62		db
Common Mode Rejection Output Voltage, $E_o = 1$ v rms; $f = 1$ kc	50	60		50	60		db
Dynamic (Linear) Output Voltage Range Peak or dc with output open-circuited (Note 1) $T_A = 25^\circ\text{C}$	$\pm 2.5$			$\pm 2.5$			v
Peak or dc with external load resistance of: (Important: See Note 2)							
$R_L = 2000 \Omega, T_A = 25^\circ\text{C}$					$\pm 2.7$		v
$R_L = 8000 \Omega, T_A = 25^\circ\text{C}$		$\pm 4.1$					v
Input Resistance							
Noninverting input; with inverting input shorted to ground, $T_A = 25^\circ\text{C}$	6	12		6	12		k $\Omega$
Inverting input; with noninverting input shorted to ground, $T_A = 25^\circ\text{C}$	30	100		30	100		k $\Omega$
Output Resistance; $T_A = 25^\circ\text{C}$	5	10			0.16	0.40	k $\Omega$
Input Current; either input; $T_A = 25^\circ\text{C}$		2			2		$\mu\text{a}$
Output Offset Voltage Both inputs with $510 \Omega \pm 1\%$ to ground; $T_A = 25^\circ\text{C}$		-0.5	$\pm 2$		-0.5	$\pm 2$	v
D-C Drift referred to Input Both inputs with $510 \Omega \pm 1\%$ to ground		8	25		8	25	$\mu\text{v}/\text{C}^\circ$
Frequency Response							
Half-Power Point (-3 db); $T_A = 25^\circ\text{C}$	30	50		30	50		kc
Unity Gain (0 db); $T_A = 25^\circ\text{C}$		10			10		Mc
Power Drain; no external load, $T_A = 25^\circ\text{C}$		28			72		mw

NOTES: 1. The open-circuit condition of the amplifier is defined as that condition in which the external load resistance applied between the output of the circuit and ground is equal to or greater than 200 k $\Omega$ .

2. Under no circumstances are either of these networks to be operated with an external load of less than 200  $\Omega$  between the output of the amplifier and ground. Permanent damage to the semiconductor network may occur if this rule is not followed.

# TYPES SN521A, SN522A GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

## TYPICAL CHARACTERISTICS



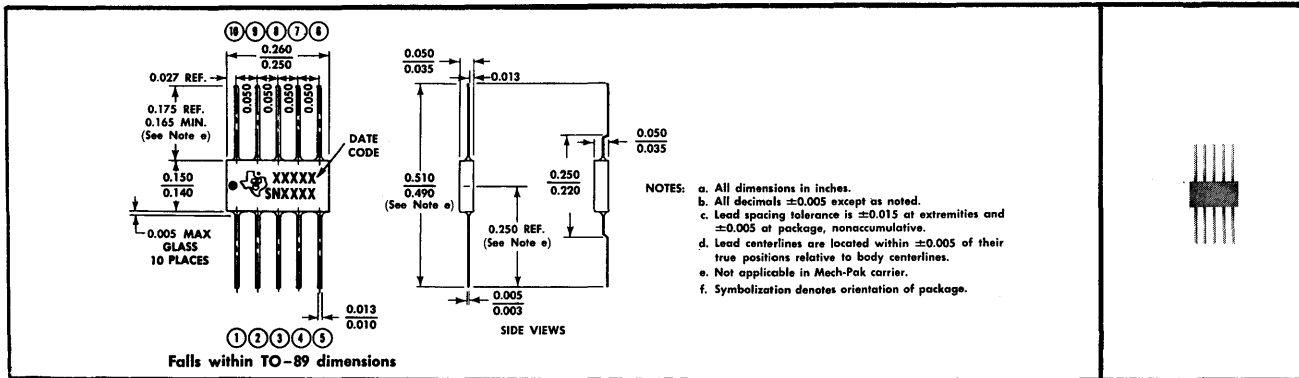
# TYPES SN521A, SN522A GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

## mechanical data

These operational amplifiers are mounted in glass-to-metal hermetically sealed welded packages meeting TO-89. Leads are gold-plated F-15 $\ddagger$  glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. Both are available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier. See Ordering Instructions.

## ORDERING INSTRUCTIONS

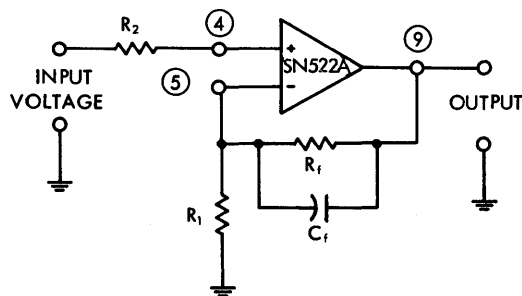
	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5



$\ddagger$ F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

## TYPICAL APPLICATION

### noninverting operational amplifier



TYPICAL FEEDBACK COMPONENTS AND ASSOCIATED CLOSED-LOOP GAIN

GAIN	$R_1$ , k $\Omega$	$R_2$ , k $\Omega$	$R_f$ , k $\Omega$	$C_f$ , pf
2	10.0	5.1	10.0	33
6	6.2	5.1	31.0	10
10	5.6	5.1	51.0	10

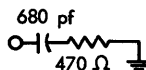
### conditions

Pin ⑦ ;  $V_{CC1} = +10$  v

Pin ⑧ ;  $V_{CC2} = +6$  v

Pin ③ ;  $V_{CC3} = -9$  v

Frequency Shaping Network; connect the network as shown between pin ① and ground.



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TI cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

TEXAS INSTRUMENTS RESERVES THE RIGHT TO MAKE CHANGES AT ANY TIME IN ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.



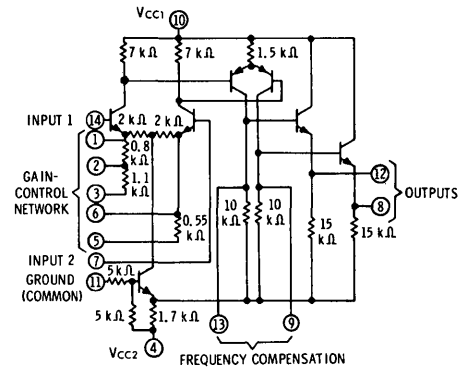
**SERIES 52 SEMICONDUCTOR-NETWORK GENERAL-PURPOSE AMPLIFIER**  
for application as

- Comparator
- Level Detector
- Differential Amplifier
- Voltage Regulator
- Military & Industrial Control Systems
- Analog-to-Digital Converters
- Analog Computers

**description**

The SN523A, offering differential inputs and differential emitter-follower outputs, incorporates a resistance network in the emitters of the input stage to facilitate gain adjustment. From the wide range of total resistance available, a particular value may be selected by connecting the resistor-network pins in a configuration which produces the desired gain. Maximum-gain configuration is with pin ① shorted to pin ⑥.

The SN523A, one of Texas Instruments Series 52 catalog line of linear integrated circuits, offers higher reliability, lower cost, smaller size, and lower weight than equivalent discrete-component circuits. Each Series 52 device is a monolithic semiconductor structure comprising diffused resistors and both n-p-n and p-n-p transistors.



NOTE: Component values shown are nominal.  
**SCHEMATIC DIAGRAM**

**mechanical data**

The SN523A is mounted in a glass-to-metal hermetically sealed welded package meeting TO-84. Leads are gold-plated F-15<sup>‡</sup> glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. The SN523A is available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier. See Ordering Instructions.

**ORDERING INSTRUCTIONS**

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 Inch				Not Applicable			
Formed Leads	No	Yes	No	Yes	No	Yes	No	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5

**OUTLINE DRAWING — SEMICONDUCTOR NETWORK WELDED PACKAGE**

**NOTES:**

- All dimensions in inches.
- All decimals  $\pm 0.005$  except as noted.
- Lead spacing tolerance is  $\pm 0.015$  at extremities and  $\pm 0.005$  at package, nonaccumulative.
- Lead centerlines are located within  $\pm 0.005$  of their true positions relative to body centerlines.
- Not applicable in Mech-Pak carrier.
- Symbolization denotes orientation of package.

<sup>†</sup>Patented by Texas Instruments

<sup>‡</sup>F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 24% nickel, and 17% cobalt.

TYPE SN523A  
BULLETIN NO. DLS-668494, MARCH 1966  
REPLACES ENGINEERING SPEC. DATED AUGUST 1964

# TYPE SN523A

## GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltages (See Note 1): $V_{CC1}$ . . . . .	+15 V
$V_{CC2}$ . . . . .	-15 V
Differential Input Voltage . . . . .	$\pm 6$ V
Input Voltage (Either Input, See Note 1) . . . . .	$\pm 10$ V
Duration of Short-Circuit Output Current . . . . .	5 s
Continuous Total Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 2) . . . . .	300 mW
Operating Free-Air Temperature Range . . . . .	-55°C to 125°C
Storage Temperature Range . . . . .	-65°C to 150°C

- NOTES: 1. These voltage values are with respect to network ground.  
 2. Derate linearly to 120 mW at 125°C free-air temperature at the rate of 1.8 mW/deg.

### electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>§</sup>	MIN	TYP	MAX	UNIT
$V_{DI}$ Differential-input offset voltage			2.2	12	mV
$\alpha_{VDI}$ Differential-input offset voltage temperature coefficient	$T_A = -55^\circ\text{C to } 125^\circ\text{C}$		9		$\mu\text{V/deg}$
$V_{CMO}$ Common-mode output offset voltage			500		mV
$I_{in}$ Input current			5		$\mu\text{A}$
$I_{DI}$ Differential-input offset current			0.5	2	$\mu\text{A}$
$V_{OM}$ Maximum peak-to-peak output voltage	Differential output, $f = 1$ kc/s		24		V
	Differential output, $f = 1$ kc/s, $T_A = -55^\circ\text{C to } 125^\circ\text{C}$	20			V
$V_{CMIM}$ Maximum common-mode input voltage			$\pm 5$		V
$A_{VD}$ Differential voltage gain	$f = 1$ kc/s		4000		
	$f = 1$ kc/s, $T_A = -55^\circ\text{C to } 125^\circ\text{C}$	2500			
	$f = 1$ kc/s, pins ① and ② open		135		
	$f = 1$ kc/s, pin ① shorted to pin ②, pin ③ open		830		
	$f = 1$ kc/s, pin ② shorted to pin ③, pins ① and ④ open		465		
	$f = 1$ kc/s, pin ③ shorted to pin ④, pins ① and ② open		325		
	$f = 1$ kc/s, pin ② shorted to pin ④, pin ① open		680		
CMRR Common-mode rejection ratio	$f = 1$ kc/s		90		dB
BW Bandwidth (-3 dB)		70	180		kc/s
$Z_{in}$ Input impedance	$f = 1$ kc/s	5	15		k $\Omega$
$Z_{out}$ Output impedance	$f = 1$ kc/s		200		$\Omega$
$P_T$ Total power dissipation			100		mW

<sup>§</sup>Unless otherwise noted, test conditions are:

$V_{CC1} = +12$  V,  $V_{CC2} = -12$  V,  $V_{DI}$  applied, no external loading; pin ① grounded, pin ② shorted to pin ③, and pins ④, ⑤, ⑥, ⑦, ⑧, ⑨ and ⑩ open.

### letter symbol and parameter definitions

- $V_{DI}$  That d-c voltage which must be applied between the input terminals to obtain zero-differential-output voltage. The application of this voltage balances the amplifier.
- $V_{CMO}$  That d-c voltage level which exists between either output terminal and ground when the outputs are balanced.
- $I_{in}$  The current into either input of the amplifier.
- $I_{DI}$  The difference in the currents into the two input terminals when the output is balanced.
- $V_{OM}$  The maximum peak-to-peak output voltage swing that can be obtained without clipping when the output is balanced.
- $V_{CMIM}$  The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.
- CMRR The ratio of the differential-mode voltage gain to the common-mode voltage gain.
- BW The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.
- $Z_{in}$  The impedance between either input terminal and ground with the other input terminal a-c grounded and the output balanced.
- $Z_{out}$  The impedance between the output terminal and ground when the output is balanced.

# TYPE SN523A GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

## TYPICAL CHARACTERISTICS§

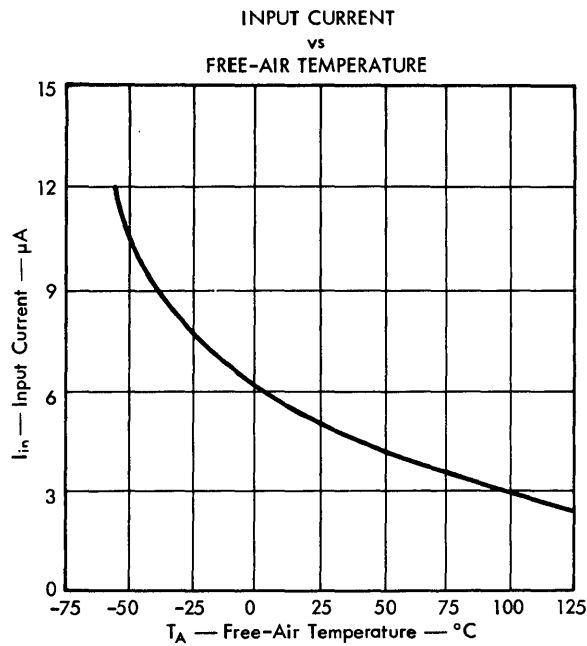


FIGURE 1

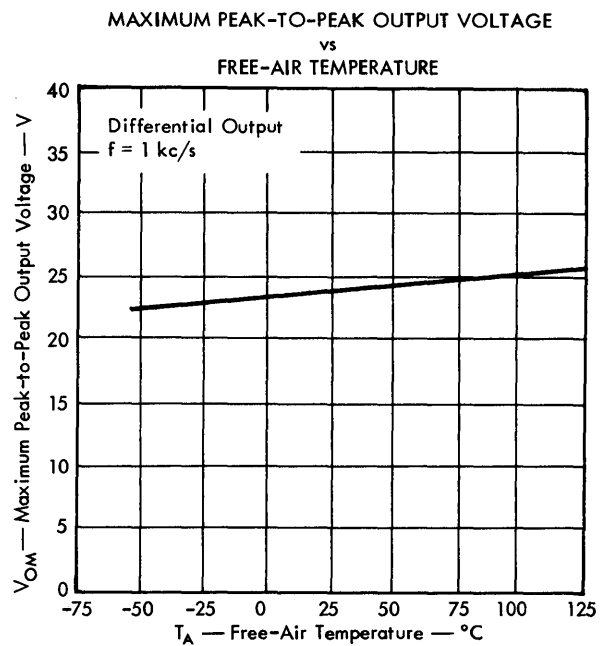


FIGURE 2

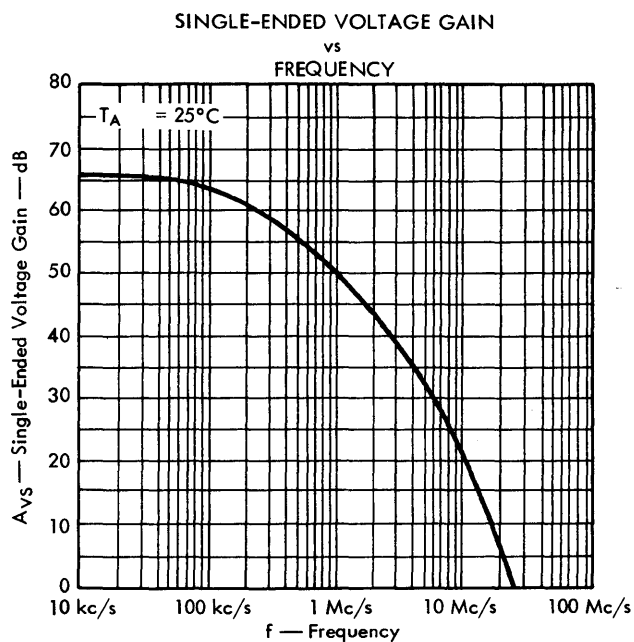


FIGURE 3

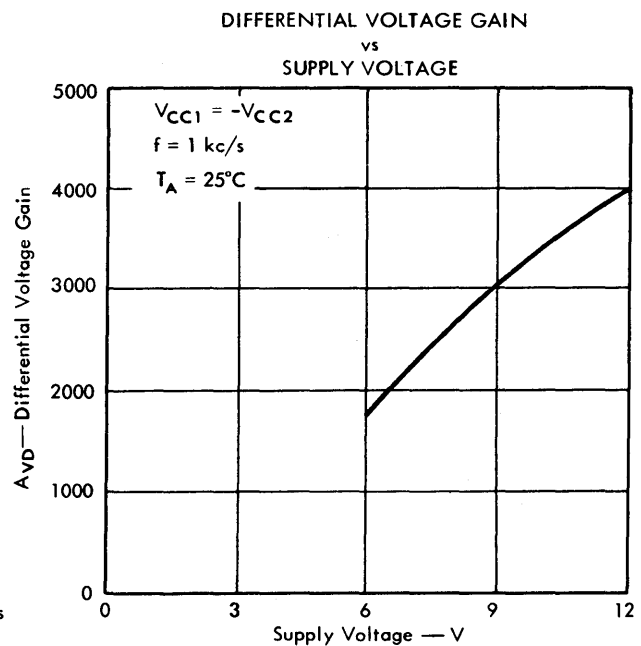


FIGURE 4

§Unless otherwise noted, test conditions are:

$V_{CC1} = +12\text{ V}$ ,  $V_{CC2} = -12\text{ V}$ ,  $V_{D1}$  applied, no external loading, pin ① grounded, pin ② shorted to pin ⑥, and pins ③, ④, ⑤, ⑧ and ⑩ open.



# TYPE SN523A GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

## TYPICAL CHARACTERISTICS§

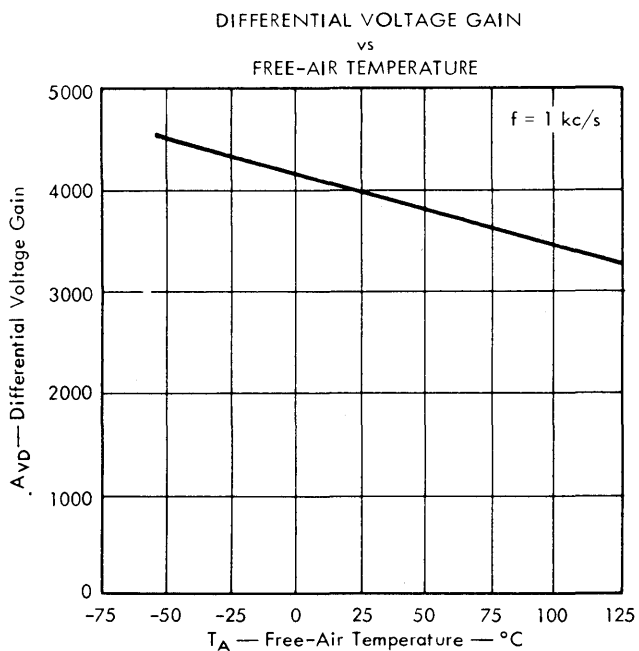


FIGURE 5

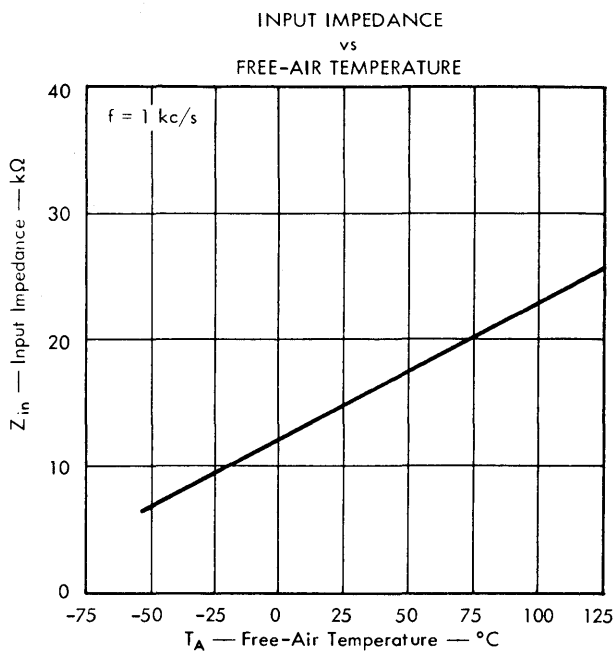


FIGURE 6

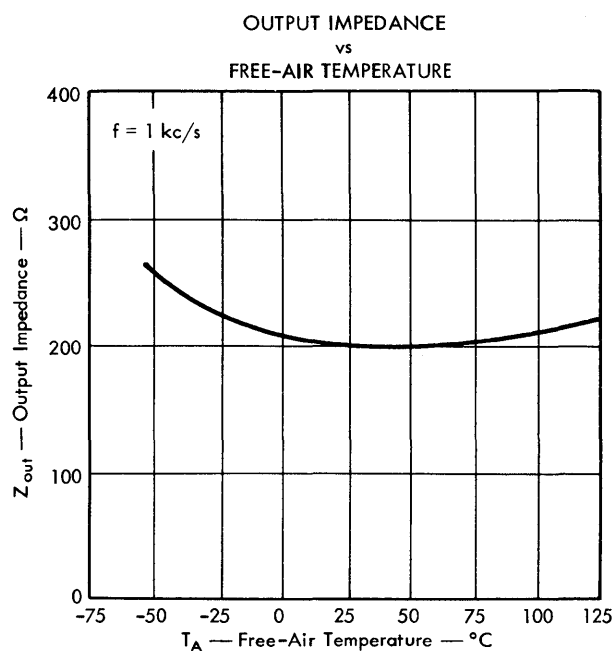


FIGURE 7

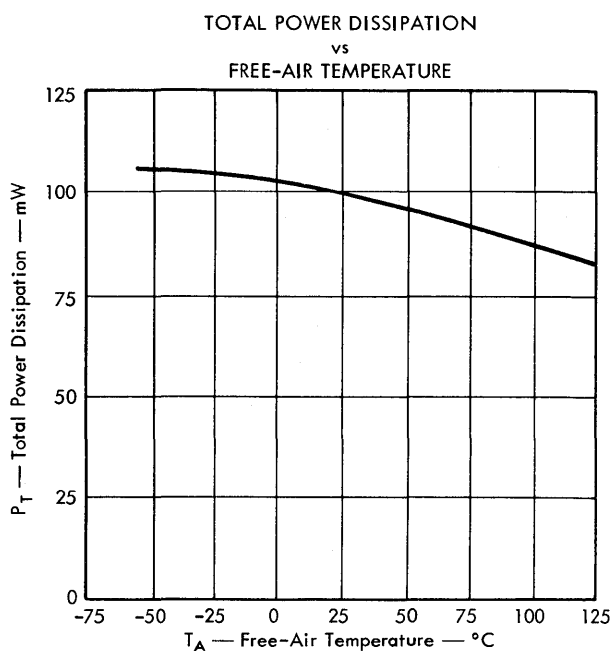


FIGURE 8

§Unless otherwise noted, test conditions are:

$V_{CC1} = +12\text{ V}$ ,  $V_{CC2} = -12\text{ V}$ ,  $V_{DI}$  applied, no external loading, pin ① grounded, pin ① shorted to pin ⑥, and pins ②, ③, ⑤, ⑨ and ⑬ open.

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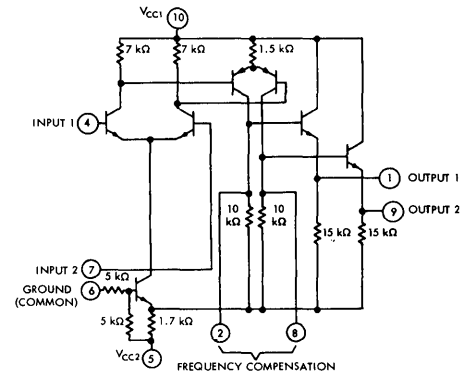
**SERIES 52 SEMICONDUCTOR-NETWORK GENERAL-PURPOSE AMPLIFIER**  
for application as

- Comparator
- Differential Amplifier
- Military & Industrial Control Systems
- Analog-to-Digital Converters
- Level Detector
- Voltage Regulator
- Analog Computers

**description**

The SN5231L offers differential inputs and differential emitter-follower outputs. Two stages of differential amplification are used to provide high gain at frequencies up to 1 MHz. A high degree of component matching, which assures stable operation over the temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , is achieved by the monolithic construction.

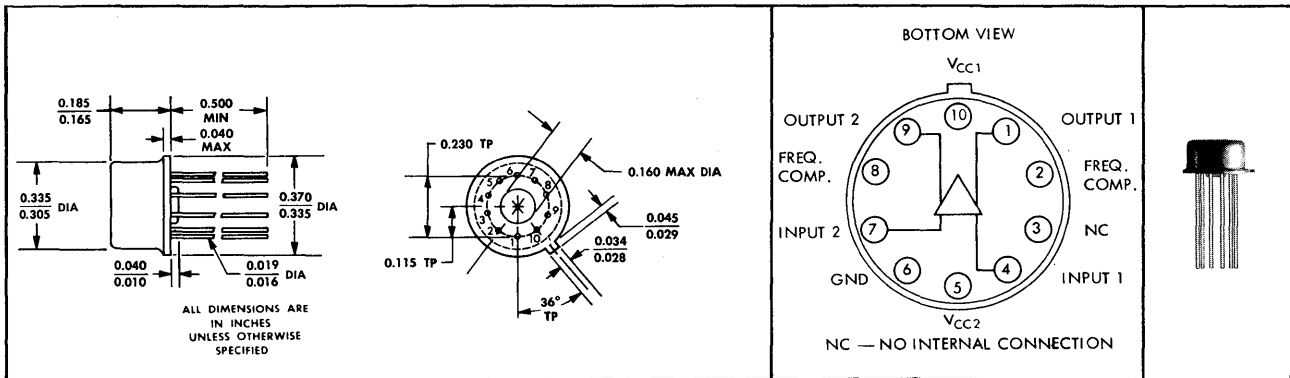
The SN5231L, one of Texas Instruments Series 52 catalog line of linear integrated circuits, offers higher reliability, lower cost, smaller size, and lower weight than equivalent discrete-component circuits. Each Series 52 device is a monolithic semiconductor structure comprising diffused resistors and both n-p-n and p-n-p transistors.



NOTE: Component values shown are nominal.  
**SCHEMATIC DIAGRAM**

**mechanical data**

The SN5231L package outline is same as JEDEC TO-100 except for diameter of standoff.



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply Voltages (See Note 1): $V_{CC1}$	.....	+15 V
$V_{CC2}$	.....	-15 V
Differential Input Voltage	.....	$\pm 6$ V
Input Voltage (Either Input, See Note 1)	.....	$\pm 10$ V
Duration of Short-Circuit Output Current	.....	5 s
Continuous Total Power Dissipation at (or below) $25^{\circ}\text{C}$ Free-Air Temperature (See Note 2)	.....	300 mW
Operating Free-Air Temperature Range	.....	$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$
Storage Temperature Range	.....	$-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$

NOTES: 1. These voltage values are with respect to network ground.  
2. Derate linearly to 120 mW at  $125^{\circ}\text{C}$  free-air temperature at the rate of 1.8 mW/deg.

<sup>†</sup>Patented by Texas Instruments

# TYPE SN5231L

## GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS§	MIN	TYP	MAX	UNIT
V <sub>DI</sub>	Differential-input offset voltage		2.2	12	mV
α <sub>VDI</sub>	Differential-input offset voltage temperature coefficient	T <sub>A(1)</sub> = 125°C, T <sub>A(2)</sub> = -55°C	9		μV/deg
V <sub>CMO</sub>	Common-mode output offset voltage		500		mV
I <sub>in</sub>	Input current		5		μA
I <sub>DI</sub>	Differential-input offset current		0.5	2	μA
V <sub>OM</sub>	Maximum peak-to-peak output voltage	Differential output, f = 1 kHz	24		V
		Differential output, f = 1 kHz, T <sub>A</sub> = -55°C to 125°C	20		V
V <sub>CMIM</sub>	Maximum common-mode input voltage		±5		V
A <sub>VD</sub>	Differential voltage gain	R <sub>S</sub> = 50 Ω, f = 1 kHz	4000		
		R <sub>S</sub> = 50 Ω, f = 1 kHz, T <sub>A</sub> = -55°C to 125°C	2500		
CMRR	Common-mode rejection ratio	R <sub>S</sub> = 50 Ω, f = 1 kHz	90		dB
BW	Bandwidth (-3 dB)		70	180	kHz
Z <sub>in</sub>	Input impedance	f = 1 kHz	5	15	kΩ
Z <sub>out</sub>	Output impedance	f = 1 kHz	200		Ω
P <sub>T</sub>	Total power dissipation		100		mW

§Unless otherwise noted, test conditions are: V<sub>CC1</sub> = +12 V, V<sub>CC2</sub> = -12 V, V<sub>DI</sub> applied, no external loading and pin 6 grounded.

### letter symbol and parameter definitions

- V<sub>DI</sub> That d-c voltage which must be applied between the input terminals to obtain zero-differential-output voltage. The application of this voltage balances the amplifier.
- α<sub>VDI</sub> Temperature coefficient averaged over the specified temperature range and defined by the equation:
- $$\alpha_{VDI} = \frac{(V_{DI} @ T_{A(1)}) - (V_{DI} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}}$$
- V<sub>CMO</sub> That d-c voltage level which exists between either output terminal and ground when the outputs are balanced.
- I<sub>in</sub> The current into either input of the amplifier.
- I<sub>DI</sub> The difference in the currents into the two input terminals when the output is balanced.
- V<sub>OM</sub> The maximum peak-to-peak output voltage swing that can be obtained without clipping when the output is balanced.
- V<sub>CMIM</sub> The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.
- CMRR The ratio of the differential-mode voltage gain to the common-mode voltage gain.
- BW The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.
- Z<sub>in</sub> The impedance between either input terminal and ground with the other input terminal a-c grounded and the output balanced.
- Z<sub>out</sub> The impedance between either output terminal and ground when the output is balanced.

# TYPE SN5231L

## GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

### TYPICAL CHARACTERISTICS§

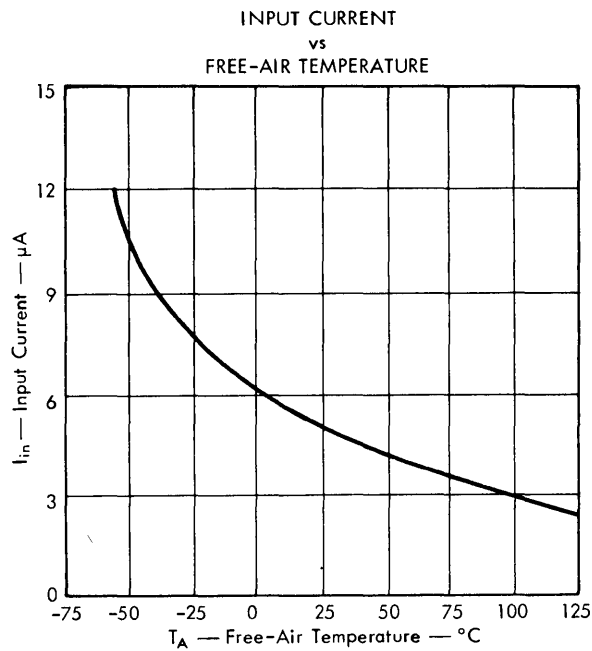


FIGURE 1

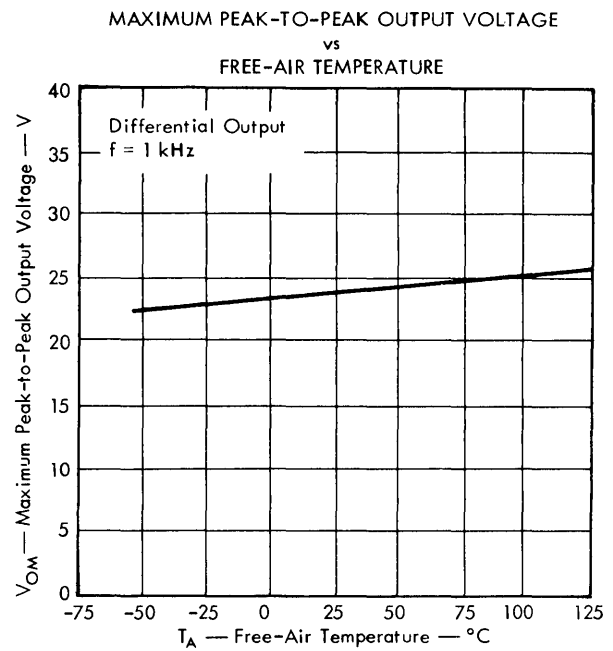


FIGURE 2

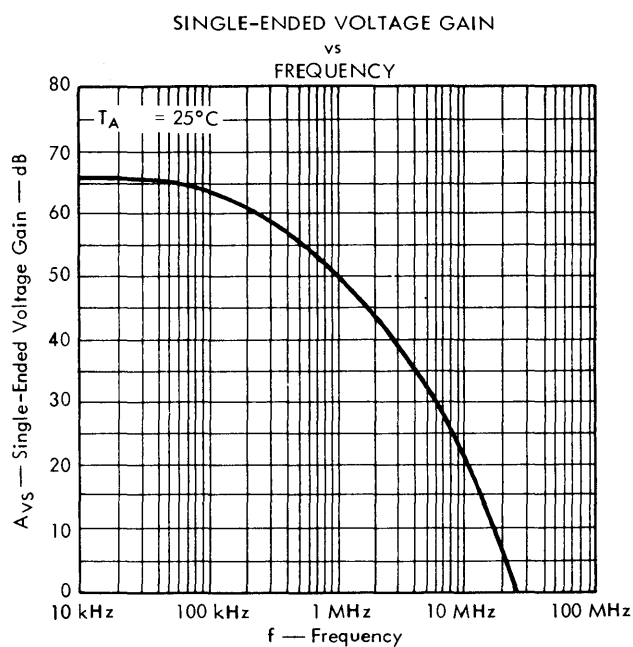


FIGURE 3

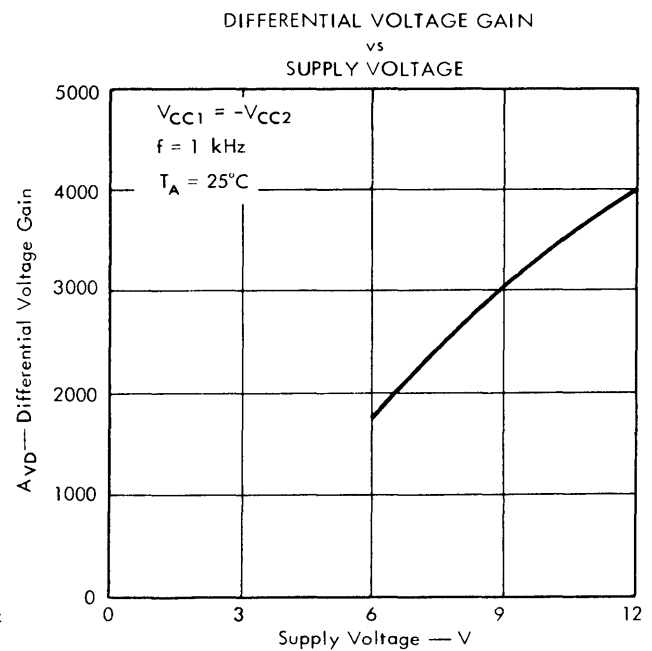


FIGURE 4

§Unless otherwise noted, test conditions are:  $V_{CC1} = +12\text{ V}$ ,  $V_{CC2} = -12\text{ V}$ ,  $V_{D1}$  applied, no external loading and pin ⑥ grounded.

# TYPE SN5231L GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

## TYPICAL CHARACTERISTICS §

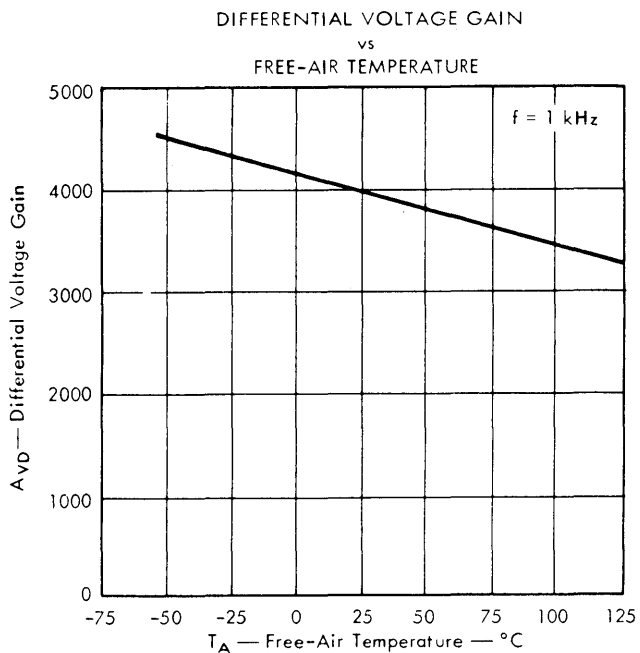


FIGURE 5

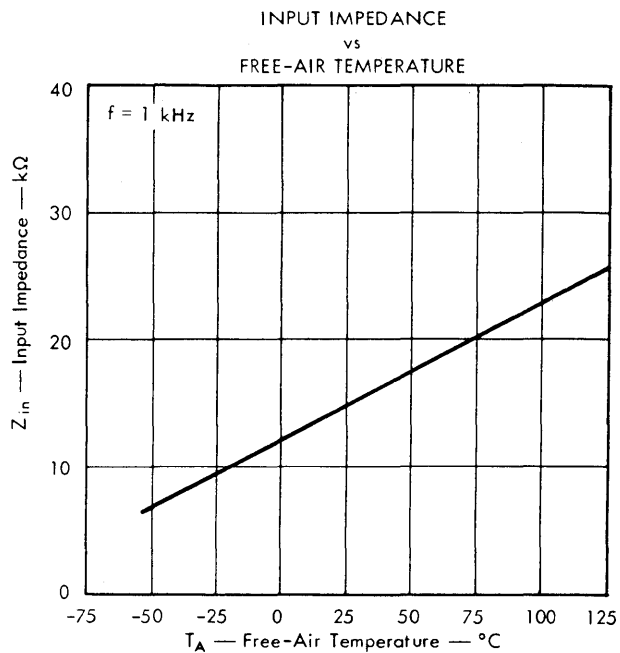


FIGURE 6

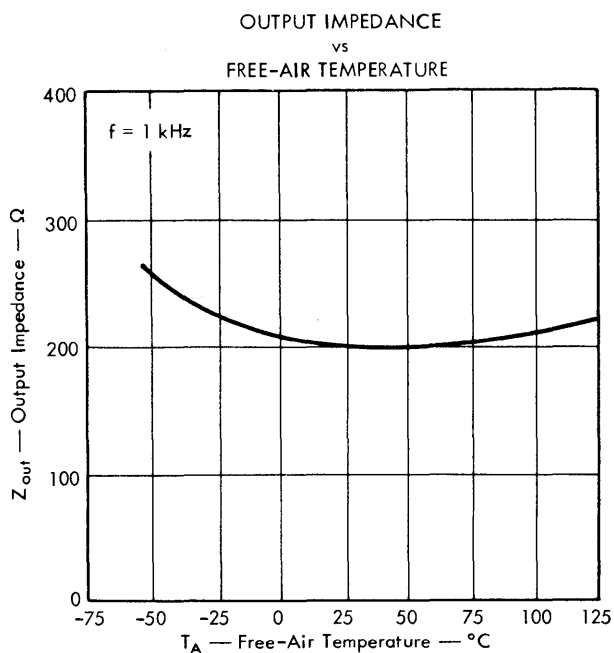


FIGURE 7

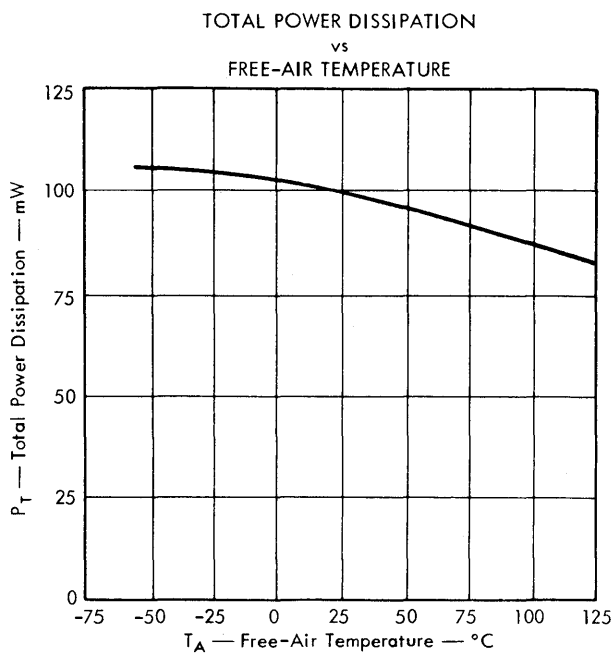


FIGURE 8

§Unless otherwise noted, test conditions are:  $V_{CC1} = +12\text{ V}$ ,  $V_{CC2} = -12\text{ V}$ ,  $V_{D1}$  applied, no external loading and pin 6 grounded.

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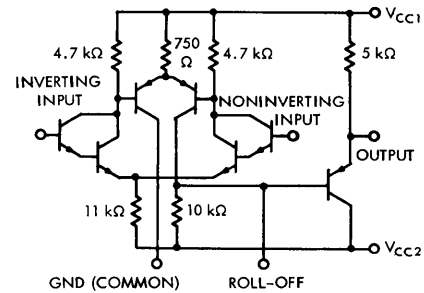
**SERIES 52 SEMICONDUCTOR-NETWORK GENERAL-PURPOSE AMPLIFIERS**  
for application as

- Buffer Amplifier**
- Differentiator**
- Integrator**
- Multivibrator**
- Level Detector**
- Summing Amplifier**

**description**

Each of these networks is a general-purpose operational amplifier consisting of two differential-gain stages and a single-ended emitter-follower output. The input stage utilizes Darlington-connected n-p-n transistors for high input impedance.

The SN524A and SN524AL, two of Texas Instruments Series 52 catalog line of linear integrated circuits, offers higher reliability, lower cost, smaller size, and lower weight than equivalent discrete component circuits. Each Series 52 device is a monolithic semiconductor structure comprising diffused resistors and both n-p-n and p-n-p transistors.



NOTE: Component values shown are nominal.

**SCHEMATIC DIAGRAM**

**mechanical data**

The SN524A operational amplifier is mounted in a glass-to-metal hermetically sealed welded package meeting TO-89. Leads are gold-plated F-15<sup>‡</sup> glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. The SN524A is available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier. See Ordering Instructions.

**SN524A ORDERING INSTRUCTIONS**

Lead Length	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5

**OUTLINE DRAWING — SN524A**

DATE CODE: XXXXX SNXXXX  
XXXXXX SNXXXX

NOTES:  
a. All dimensions in inches.  
b. All decimals  $\pm 0.005$  except as noted.  
c. Lead spacing tolerance is  $\pm 0.015$  at extremities and  $\pm 0.005$  at package, nonaccumulative.  
d. Lead centerlines are located within  $\pm 0.005$  of their true positions relative to body centerlines.  
e. Not applicable in Mech-Pak carrier.  
f. Symbolization denotes orientation of package.

Falls within TO-89 dimensions

**TOP VIEW**

NC — NO INTERNAL CONNECTION

The SN524AL package outline is same as JEDEC TO-76 except for case height.

**OUTLINE DRAWING — SN524AL**

DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED

**BOTTOM VIEW**

NC — NO INTERNAL CONNECTION

<sup>†</sup>Patented by Texas Instruments.

<sup>‡</sup>F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

TYPES SN524A, SN524AL  
 BULLETIN NO. DL-S 668375, MARCH 1966  
 REPLACES ENGINEERING SPEC. DATED AUGUST 1964

# TYPES SN524A, SN524AL

## GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltages (See Note 1): $V_{CC1}$ . . . . .	+15 V
$V_{CC2}$ . . . . .	-15 V
Differential Input Voltage . . . . .	12 V
Common-Mode Input Voltage . . . . .	$\pm 10$ V
Operating Free-Air Temperature Range . . . . .	-55°C to 125°C
Storage Temperature Range . . . . .	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground.

### electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS§	MIN	TYP	MAX	UNIT
$V_{DI}$	Differential-input offset voltage			12		mV
		$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$			40	mV
$\alpha_{VDI}$	Differential-input offset voltage temperature coefficient	$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$		25		$\mu\text{V}/\text{deg}$
$I_{in}$	Input Current			80	350	nA
$I_{DI}$	Differential-input offset current			20		nA
		$T_A = -55^\circ\text{C}$		60		nA
		$T_A = 125^\circ\text{C}$		6		nA
$V_{OM}$	Maximum peak-to-peak output voltage	$f = 1 \text{ kc/s}$ , $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	11			V
		$f = 1 \text{ kc/s}$		16		V
		10 k $\Omega$ load, $f = 1 \text{ kc/s}$ , $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	9			V
		10 k $\Omega$ load, $f = 1 \text{ kc/s}$		15		V
					$\pm 5$	
$V_{CMIM}$	Maximum common-mode input voltage			$\pm 5$		V
$A_V$	Voltage gain	$f = 1 \text{ kc/s}$ , $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	630			
		$f = 1 \text{ kc/s}$		1400		
CMRR	Common-mode rejection ratio	$f = 1 \text{ kc/s}$ , $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$		55		dB
BW	Bandwidth (-3 dB)		70	140		kc/s
$Z_{in}$	Input impedance	$f = 1 \text{ kc/s}$	350	1000		k $\Omega$
$Z_{out}$	Output impedance	$f = 1 \text{ kc/s}$		200		$\Omega$
$P_T$	Total power dissipation	No input signal, no external load		120		mW

§Unless otherwise noted test conditions are:  $V_{CC1} = +12 \text{ V}$ ,  $V_{CC2} = -12 \text{ V}$ , ground and  $V_{DI}$  applied; roll-off terminal open, no external loading. The unused input is grounded for all tests except when common-mode characteristics are under test.

### letter symbol and parameter definitions

$V_{DI}$	That d-c voltage which must be applied between the input terminals to obtain zero-output voltage referenced to ground. The application of this voltage balances the amplifier.
$I_{in}$	The current into either input of the amplifier.
$I_{DI}$	The difference in the currents into the two input terminals when the output is balanced.
$V_{OM}$	The maximum peak-to-peak output voltage swing that can be obtained without clipping when the output is balanced.
$V_{CMIM}$	The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.
CMRR	The ratio of the differential-mode voltage gain to the common-mode voltage gain.
BW	The range of frequencies within which the voltage gain is within 3 dB of the mid-frequency value.
$Z_{in}$	The impedance between either input terminal and ground with the other input terminal a-c grounded and the output balanced.
$Z_{out}$	The impedance between the output terminal and ground when the output is balanced.

# TYPES SN524A, SN524AL GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

## TYPICAL CHARACTERISTICS §

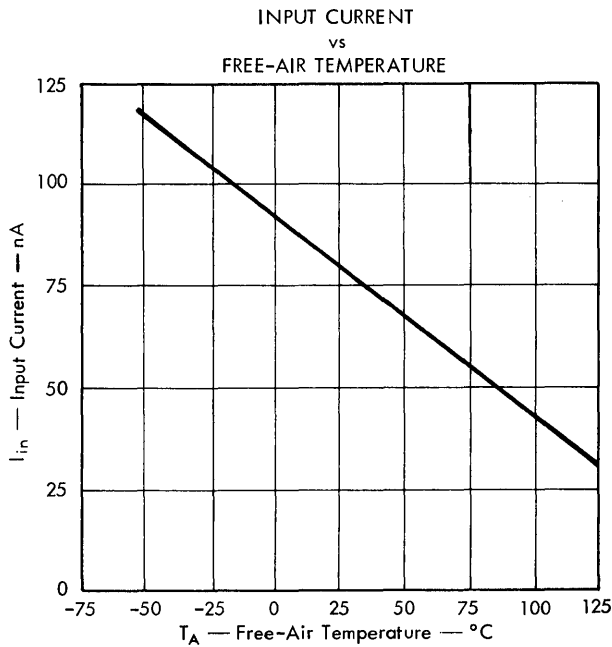


FIGURE 1

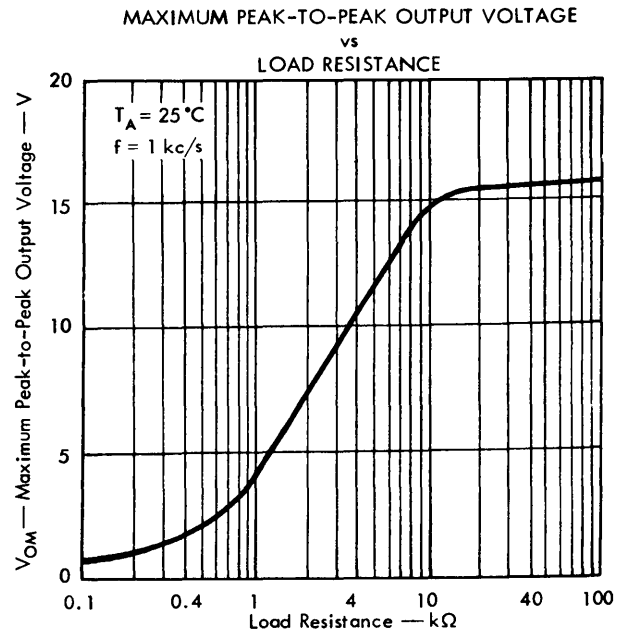


FIGURE 2

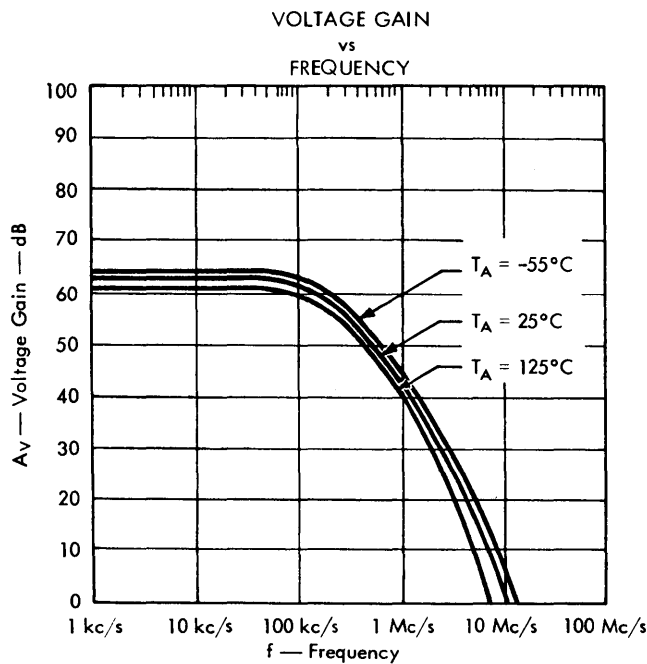


FIGURE 3

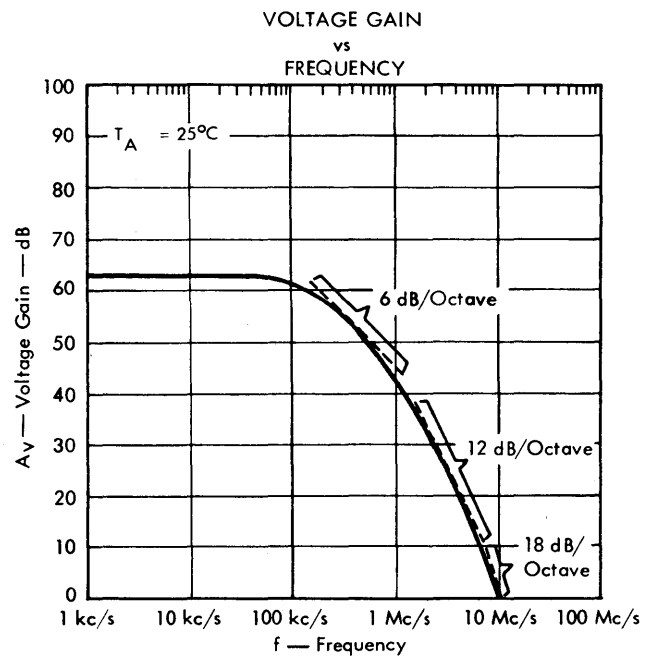


FIGURE 4

§Unless otherwise noted test conditions are:  $V_{CC1} = +12 \text{ V}$ ,  $V_{CC2} = -12 \text{ V}$ , ground and  $V_{D1}$  applied; roll-off terminal open, no external loading. The unused input is grounded for all tests except when common-mode characteristics are under test.



# TYPES SN524A, SN524AL

## GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

### TYPICAL CHARACTERISTICS §

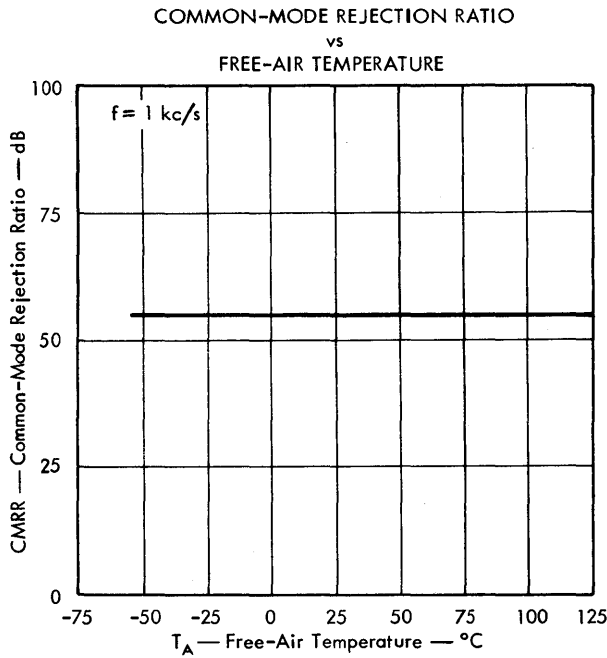


FIGURE 5

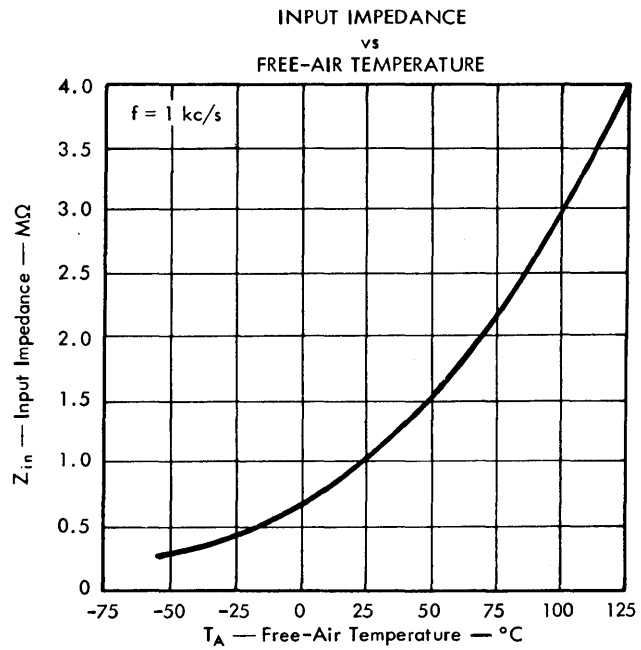


FIGURE 6

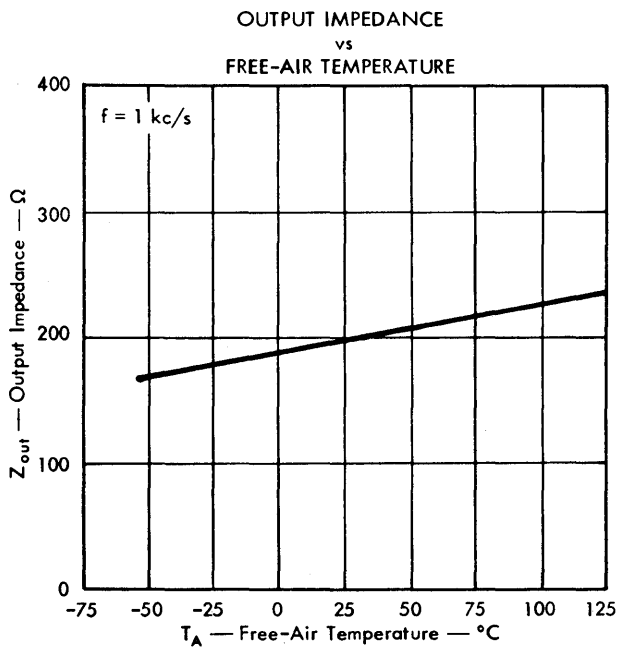


FIGURE 7

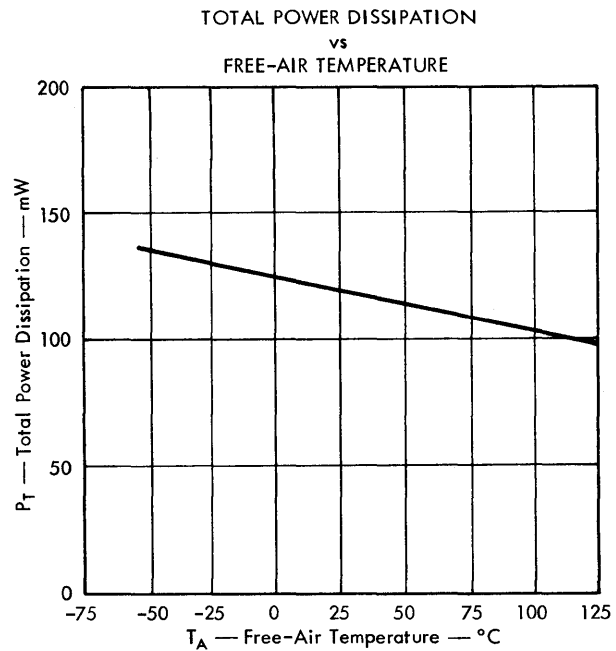


FIGURE 8

§Unless otherwise noted test conditions are:  $V_{CC1} = +12$  V,  $V_{CC2} = -12$  V, ground and  $V_{DI}$  applied; roll-off terminal open, no external loading. The unused input is grounded for all tests except when common-mode characteristics are under test.

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**A SERIES 52 AMPLIFIER**

featuring

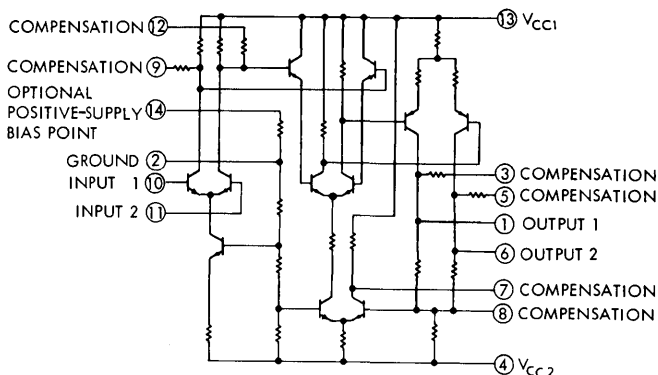
• Open-Loop Gain ... 90 dB

• Typical CMRR ... 100 dB

**description**

The SN525 is a high-performance amplifier featuring an open-loop gain of 90 dB, yet it is unconditionally stable when used with external capacitors in the frequency-response shaping circuit. A feedback loop provides high common-mode rejection. Both differential input and output terminals are available.

Texas Instruments Series 52 catalog line of linear integrated circuits offers higher reliability, lower cost, smaller size, and less weight than equivalent discrete component circuits. Each Series 52 device is a monolithic semiconductor structure comprising diffused resistors and both n-p-n and p-n-p transistors.



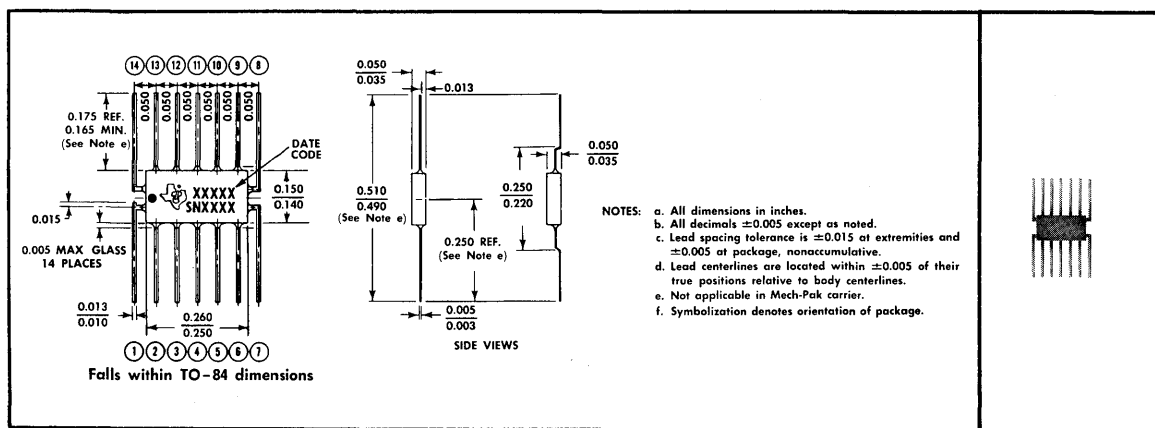
**SCHEMATIC**

**mechanical data**

The SN525 semiconductor network is mounted in a glass-to-metal hermetically sealed welded package. Leads are gold-plated F-15<sup>‡</sup> glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. The SN525 is available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier. See ordering instructions.

**ORDERING INSTRUCTIONS**

Lead Length	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5



- NOTES:
- a. All dimensions in inches.
  - b. All decimals  $\pm 0.005$  except as noted.
  - c. Lead spacing tolerance is  $\pm 0.015$  at extremities and  $\pm 0.005$  at package, nonaccumulative.
  - d. Lead centerlines are located within  $\pm 0.005$  of their true positions relative to body centerlines.
  - e. Not applicable in Mech-Pak carrier.
  - f. Symbolization denotes orientation of package.

<sup>†</sup>Patented by Texas Instruments

<sup>‡</sup>F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.



# TYPE SN525

## GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltages (See Note 1): $V_{CC1}$ . . . . .	+15 V
$V_{CC2}$ . . . . .	-15 V
Differential Input Voltage . . . . .	5 V
Common-Mode Input Voltage . . . . .	$\pm 12$ V
Operating Free-Air Temperature Range . . . . .	-55°C to 125°C
Storage Temperature Range . . . . .	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

### electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS §	MIN	TYP	MAX	UNIT
$V_{DI}$	Differential-input offset voltage			1	3	mV
		$T_A = -55^\circ\text{C to } 125^\circ\text{C}$			4	mV
$V_{CMO}$	Common-mode output offset voltage			250	1000	mV
$I_{in}$	Input current	$T_A = 125^\circ\text{C}$		270	700	nA
				450	900	nA
		$T_A = -55^\circ\text{C}$		750	1500	nA
$I_{DI}$	Differential-input offset current	$T_A = 125^\circ\text{C}$		12	200	nA
				16	200	nA
		$T_A = -55^\circ\text{C}$		38	550	nA
$V_{OM}$	Maximum peak-to-peak output voltage	Single-ended output, $f = 1$ kHz		18		V
		Single-ended output, $f = 1$ kHz, $T_A = -55^\circ\text{C to } 125^\circ\text{C}$	14			V
$V_{CMIM}$	Maximum common-mode input voltage			$\pm 7$		V
$A_{VS}$	Small-signal single-ended voltage gain	$f = 1$ kHz	20 000	32 000		
		$f = 1$ kHz, $T_A = -55^\circ\text{C to } 125^\circ\text{C}$	10 000			
$A_{VCM}$	Small-signal common-mode single-ended voltage gain	$f = 1$ kHz			0.9	
CMRR	Small-signal common-mode rejection ratio	$f = 1$ kHz		100		dB
BW	Bandwidth (-3 dB)			45		kHz
$z_{in}$	Input impedance	$f = 1$ kHz	50	140		$k\Omega$
$z_{out}$	Output impedance	$f = 1$ kHz		10		$k\Omega$
SVRR	Supply voltage rejection ratio	$\Delta V_{CC} \leq 0.5$ V		25		$\mu\text{V/V}$
$P_T$	Total power dissipation			100	135	mW

§ Unless otherwise noted, test conditions include:  $V_{CC1} = +12$  V,  $V_{CC2} = -12$  V, ground and  $V_{DI}$  applied, no external load, external 250-pF capacitor connected between pins (7) and (8), and other frequency-compensation pins open.

### letter symbol and parameter definitions

- $V_{DI}$  That d-c voltage which must be applied between the input terminals to obtain zero-differential-output voltage. The application of this voltage balances the amplifier.
- $V_{CMO}$  That d-c voltage level which exists between either output terminal and ground when the outputs are balanced.
- $I_{in}$  The current into either input of the amplifier.
- $I_{DI}$  The difference in the currents into the two input terminals when the output is balanced.
- $V_{OM}$  The maximum peak-to-peak output voltage swing that can be obtained without clipping when the output is balanced.
- $V_{CMIM}$  The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.
- CMRR The ratio of the differential-mode voltage gain to the common-mode voltage gain.
- BW The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.
- $z_{in}$  The impedance between either input terminal and ground with the other input terminal a-c grounded and the output balanced.
- $z_{out}$  The impedance between either output terminal and ground when the output is balanced.
- SVRR The ratio of the change in input offset voltage to the change in power supply voltage which produces the variation.

### compensation requirements

External capacitance must be connected between pins (7) and (8) to stabilize the amplifier if symmetrical compensation to ground is not used on pins (3) and (5) or pins (1) and (6).

# TYPE SN525 GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

## TYPICAL CHARACTERISTICS §

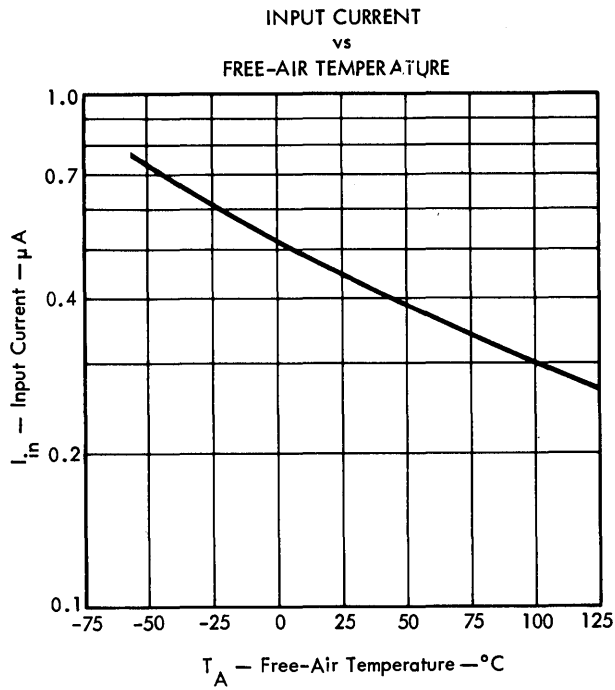


FIGURE 1

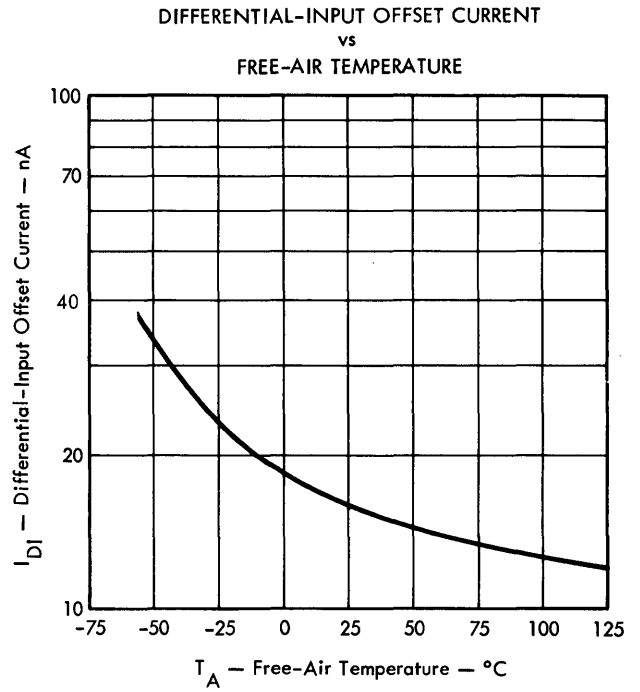


FIGURE 2

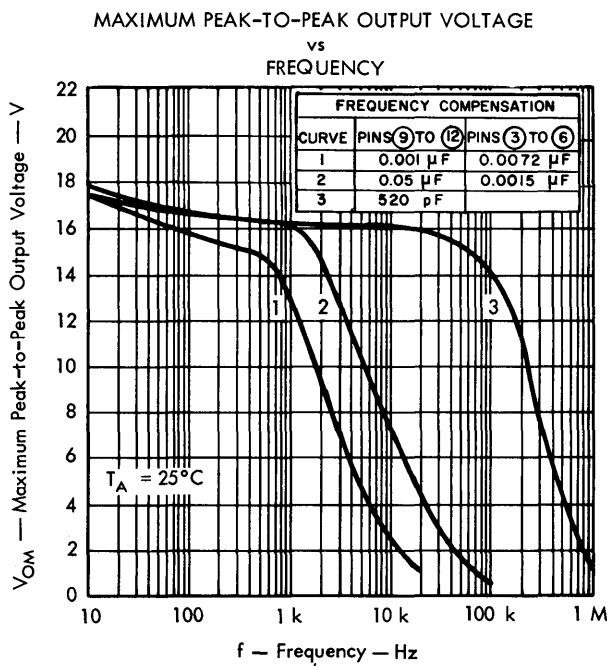


FIGURE 3

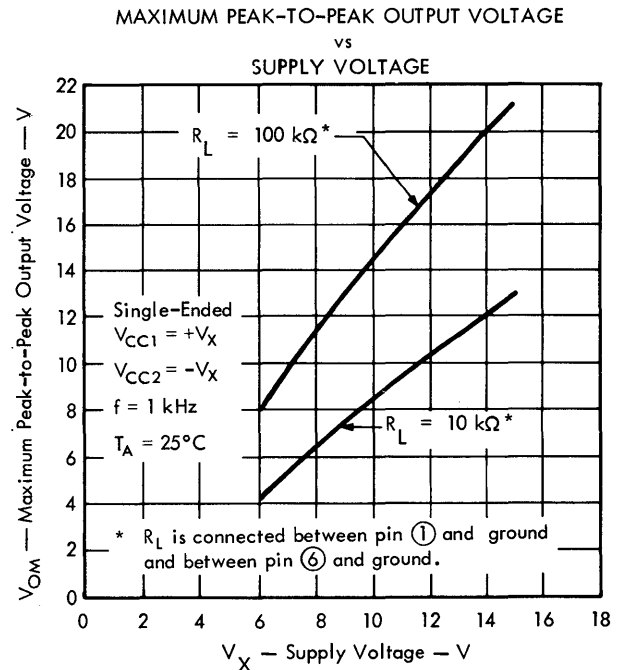


FIGURE 4

§ Unless otherwise noted, test conditions include:  $V_{CC1} = +12 V$ ,  $V_{CC2} = -12 V$ , ground and  $V_{DI}$  applied, no external load, external 250-pF capacitor connected between pins (7) and (8), and other frequency-compensation pins open.

# TYPE SN525 GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

## TYPICAL CHARACTERISTICS §

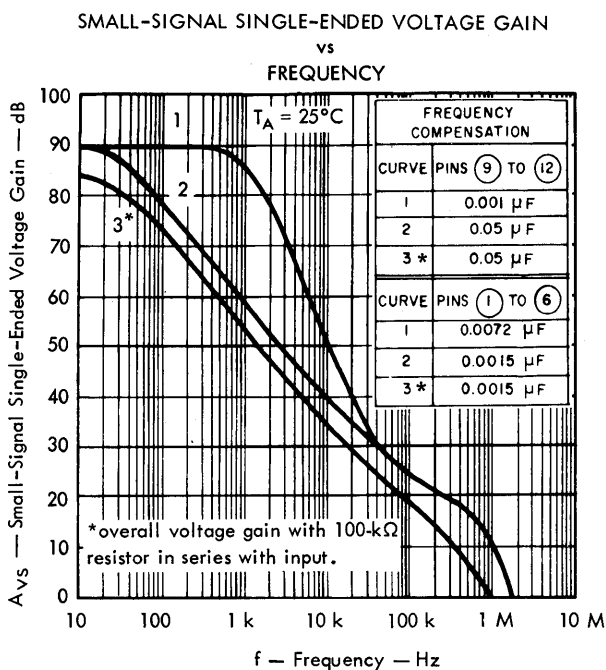


FIGURE 5

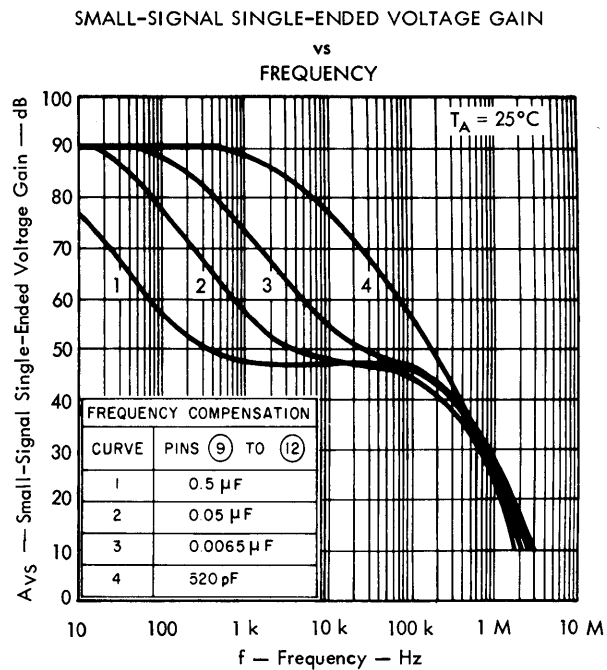


FIGURE 6

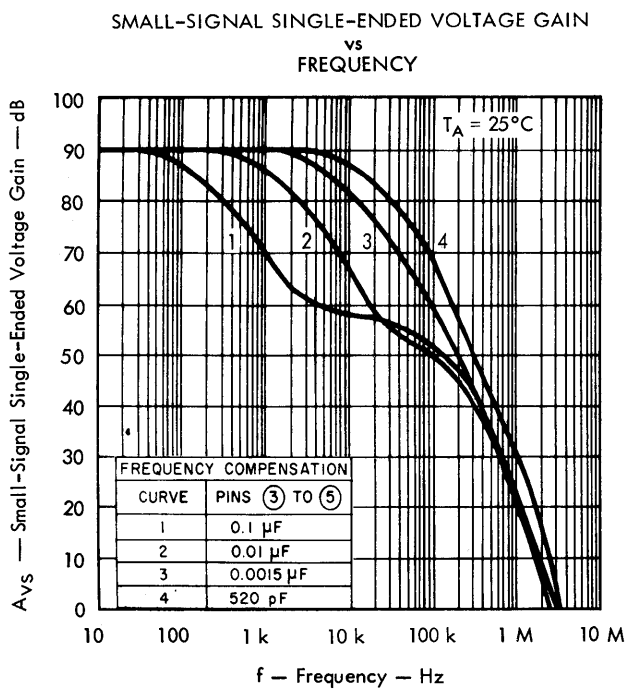


FIGURE 7

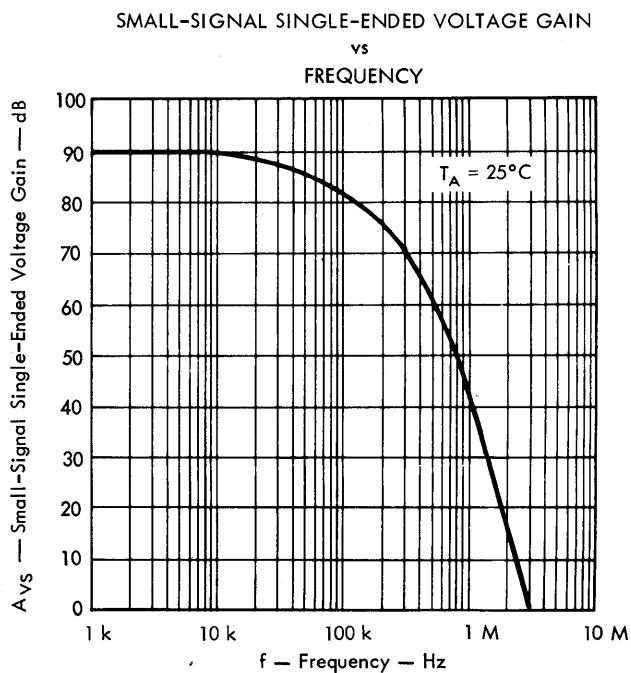


FIGURE 8

§ Unless otherwise noted, test conditions include:  $V_{CC1} = +12\text{ V}$ ,  $V_{CC2} = -12\text{ V}$ , ground and  $V_{D1}$  applied, no external load, external 250-pF capacitor connected between pins (7) and (8), and other frequency-compensation pins open.

# TYPE SN525 GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

## TYPICAL CHARACTERISTICS §

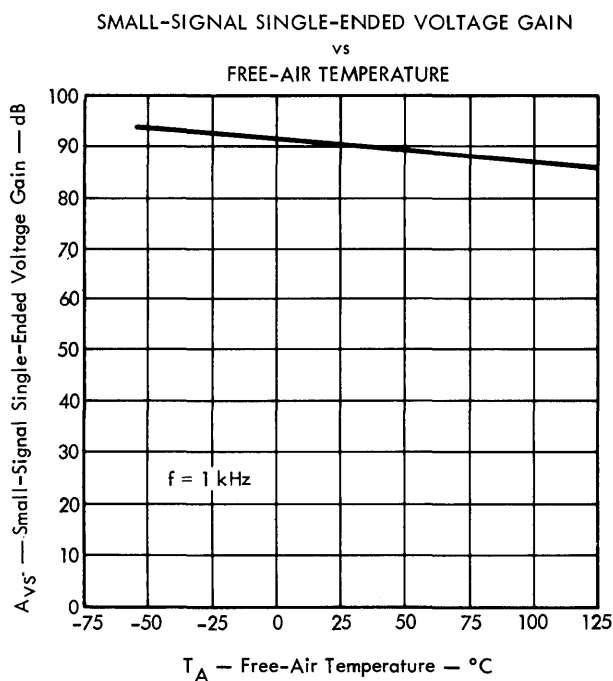


FIGURE 9

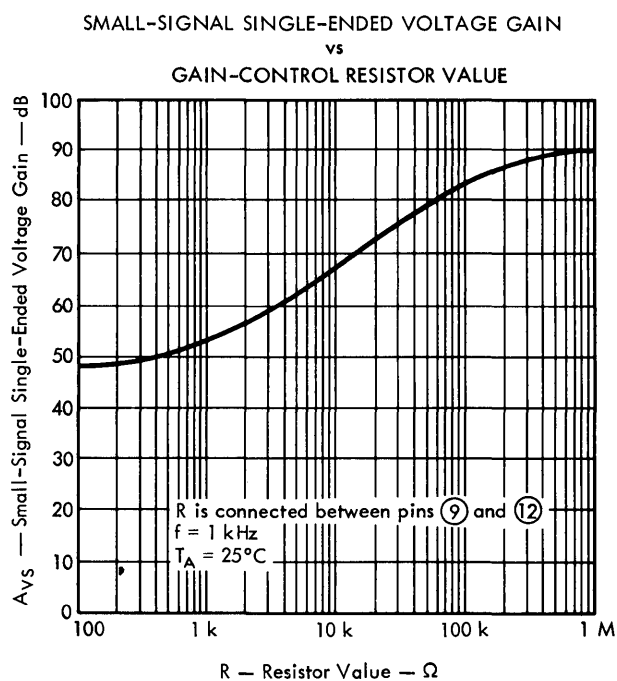


FIGURE 10

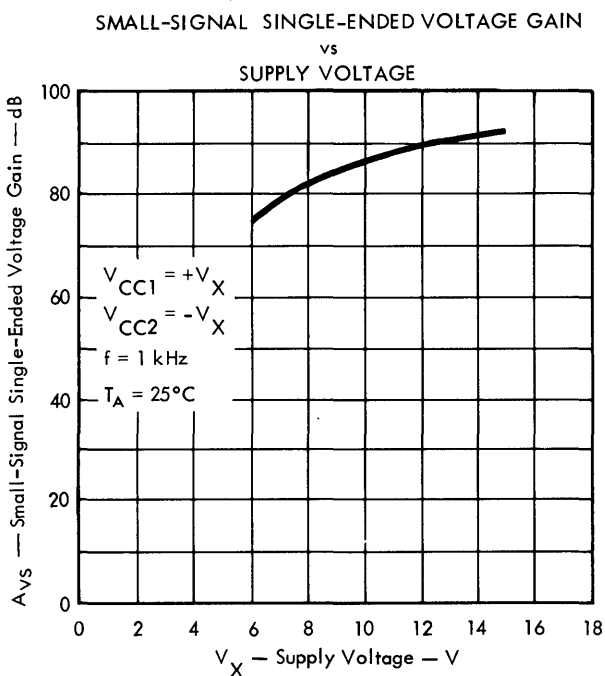


FIGURE 11

§ Unless otherwise noted, test conditions include:  $V_{CC1} = +12 \text{ V}$ ,  $V_{CC2} = -12 \text{ V}$ , ground and  $V_{DI}$  applied, no external load, external 250-pF capacitor connected between pins ⑦ and ⑧, and other frequency-compensation pins open.

# TYPE SN525 GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

## TYPICAL UNITY-GAIN CONFIGURATION

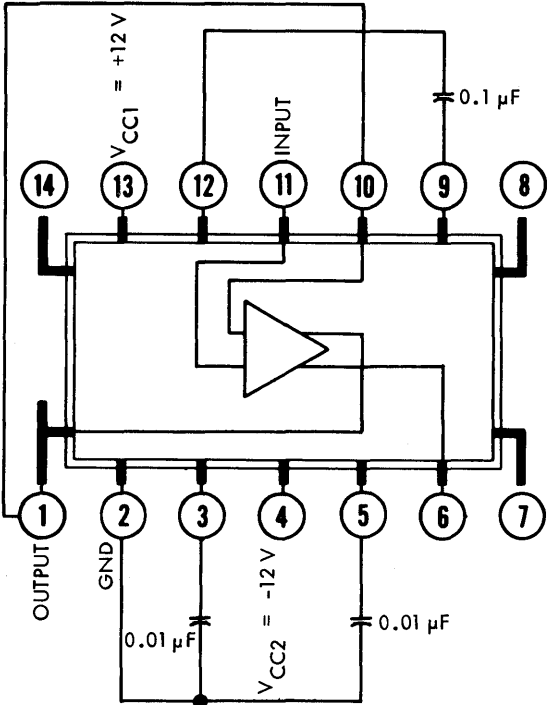


FIGURE 12



**A SERIES 52 AMPLIFIER**

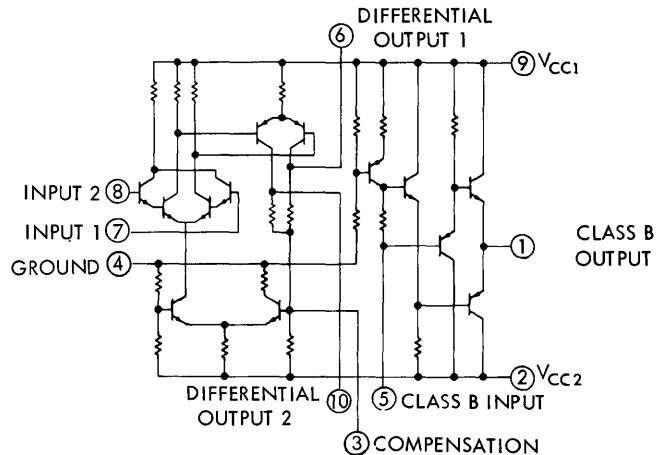
featuring

- Minimum  $Z_{in} \dots 350 \text{ k}\Omega$
- Differential or Class B Power Output

**description**

The SN526 semiconductor-network amplifier features Darlington high-impedance differential-input stages and a Class B output power amplifier with high-voltage- and current-range capabilities. Common-mode input signals are rejected by use of common-mode feedback to the input amplifier.

The SN526, one of Texas Instruments Series 52 catalog line of linear integrated circuits, offers higher reliability, lower cost, smaller size, and less weight than equivalent discrete-component circuits. Each Series 52 device is a monolithic semiconductor structure comprising diffused resistors and both n-p-n and p-n-p transistors.



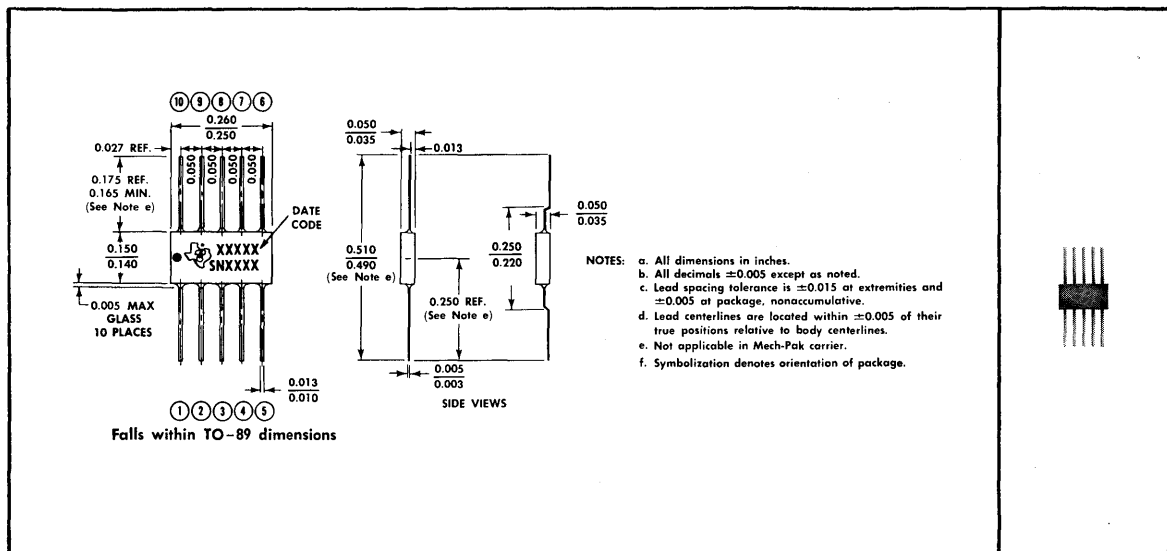
**SCHEMATIC**

**mechanical data**

The SN526 is mounted in a glass-to-metal hermetically sealed welded package. Leads are gold-plated F-15 † glass sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. The SN526 is available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier. See Ordering Instructions.

**ORDERING INSTRUCTIONS**

Lead Length	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5



- NOTES:
- All dimensions in inches.
  - All decimals  $\pm 0.005$  except as noted.
  - Lead spacing tolerance is  $\pm 0.015$  at extremities and  $\pm 0.005$  at package, nonaccumulative.
  - Lead centerlines are located within  $\pm 0.005$  of their true positions relative to body centerlines.
  - Not applicable in Mech-Pak carrier.
  - Symbolization denotes orientation of package.

† Patented by Texas Instruments.

‡ F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

TYPE SN526  
BULLETIN NO. DL-S 669273, NOVEMBER 1966





# TYPE SN526

## GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltages (See Note 1): $V_{CC1}$ . . . . .	+15 V
$V_{CC2}$ . . . . .	-15 V
Differential Input Voltage . . . . .	10 V
Common-Mode Input Voltage . . . . .	$\pm 12$ V
Continuous Total Power Dissipation at (or below) 100°C Case Temperature (See Note 2) . . . . .	250 mW
Operating Free-Air Temperature Range . . . . .	-55°C to 125°C
Storage Temperature Range . . . . .	-65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground.  
2. Derate linearly above 100°C case temperature at a rate of 5 mW/deg.

### electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS §	MIN	TYP	MAX	UNIT
$V_{DI}$ Differential-input offset voltage			3	17	mV
	$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$			20	mV
$V_{CMO}$ Common-mode output offset voltage			220	750	mV
$I_{in}$ Input current	$T_A = 125^\circ\text{C}$		9	100	nA
			50	300	nA
$I_{DI}$ Differential-input offset current	$T_A = -55^\circ\text{C}$		230	1000	nA
	$T_A = 125^\circ\text{C}$		1.5	50	nA
			6	100	nA
$V_{OM}$ Maximum peak-to-peak output voltage	Class B output (See Note 3) $R_L = 600 \Omega$ , $f = 1 \text{ kHz}$		11.7		V
	Class B output (See Note 3) $R_L = 600 \Omega$ , $f = 1 \text{ kHz}$ $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	10			V
$V_{CMIM}$ Maximum common-mode input voltage			$\pm 7$		V
$A_{VS}$ Small-signal single-ended voltage gain	$f = 1 \text{ kHz}$	800	1200		
	$f = 1 \text{ kHz}$ , $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	630			
$A_{V_{CMS}}$ Small-signal single-ended common-mode voltage gain	$f = 1 \text{ kHz}$		0.14	0.5	
CMRR Small-signal common-mode rejection ratio	$f = 1 \text{ kHz}$		77		dB
BW Bandwidth (-3 dB)			120		kHz
$z_{in}$ Input impedance	$f = 1 \text{ kHz}$	0.35	1		M $\Omega$
$P_T$ Total power dissipation			132	190	mW

§ Unless otherwise noted, test conditions include:  $V_{CC1} = +12 \text{ V}$ ,  $V_{CC2} = -12 \text{ V}$ , ground and  $V_{DI}$  applied, no external load, and a 0.05- $\mu\text{F}$  capacitor between pin (3) and ground. All parameters except  $V_{OM}$  are measured with pin (5) grounded and pin (1) open.

Note 3: Pin (5) is connected to pin (6) or pin (10).

### letter symbol and parameter definitions

$V_{DI}$	That d-c voltage which must be applied between the input terminals to obtain zero-differential-output voltage. The application of this voltage balances the amplifier.
$V_{CMO}$	That d-c voltage level which exists between either output terminal and ground when the outputs are balanced.
$I_{in}$	The current into either input of the amplifier.
$I_{DI}$	The difference in the currents into the two input terminals when the output is balanced.
$V_{OM}$	The maximum peak-to-peak output voltage swing that can be obtained without clipping when the output is balanced.
$V_{CMIM}$	The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.
CMRR	The ratio of the differential-mode voltage gain to the common-mode voltage gain.
BW	The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.
$z_{in}$	The impedance between either input terminal and ground with the other input terminal a-c grounded and the output balanced.
$z_{out}$	The impedance between either output terminal and ground when the output is balanced.

### compensation requirements

External capacitance must be connected between pin (3) and ground to stabilize the amplifier if symmetrical compensation is not used on pins (6) and (10).

# TYPE SN526 GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

## TYPICAL CHARACTERISTICS §

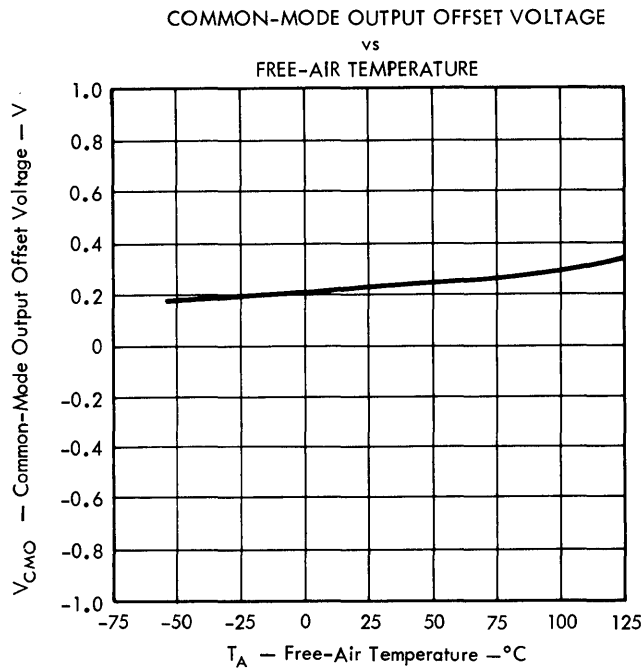


FIGURE 1

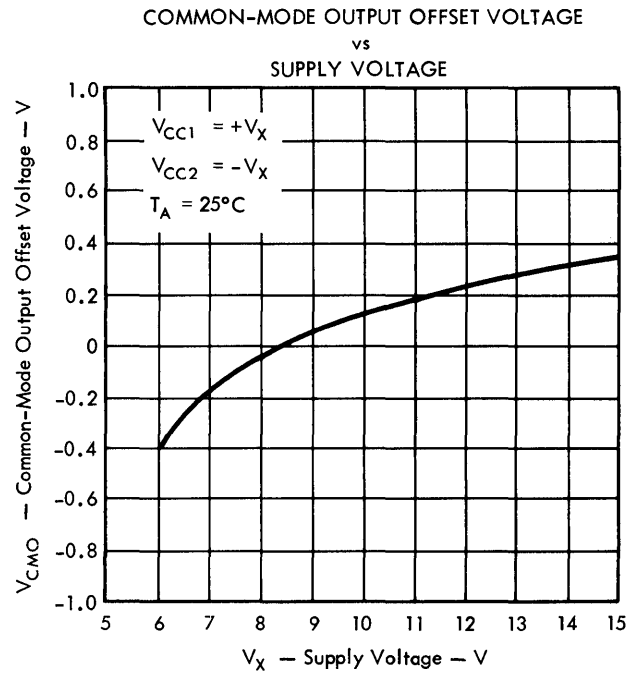


FIGURE 2

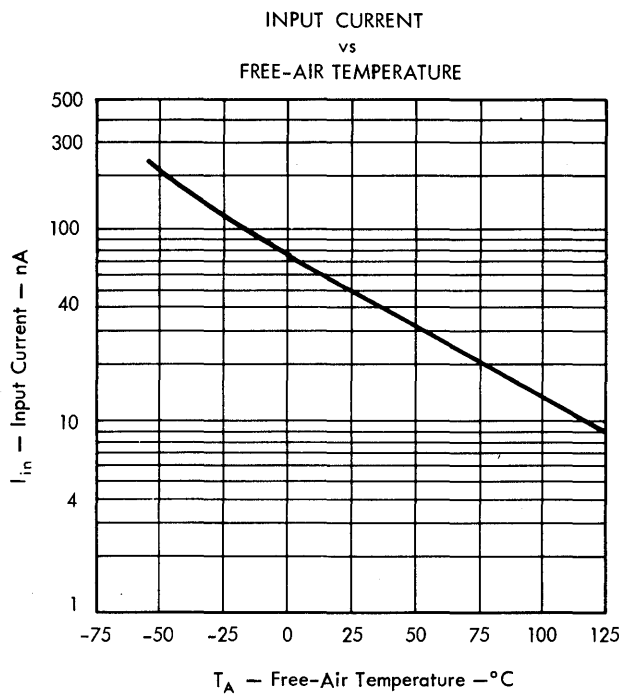


FIGURE 3

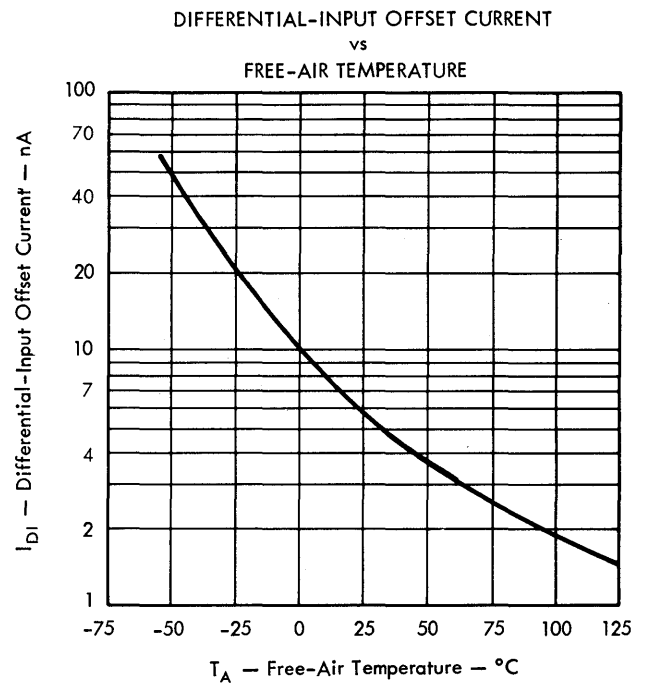


FIGURE 4

§ Unless otherwise noted, test conditions include:  $V_{CC1} = +12\text{ V}$ ,  $V_{CC2} = -12\text{ V}$ , ground and  $V_{DI}$  applied, no external load, and a  $0.05\text{-}\mu\text{F}$  capacitor between pin (3) and ground. All parameters except  $V_{OM}$  are measured with pin (5) grounded and pin (1) open.

# TYPE SN526 GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

## TYPICAL CHARACTERISTICS §

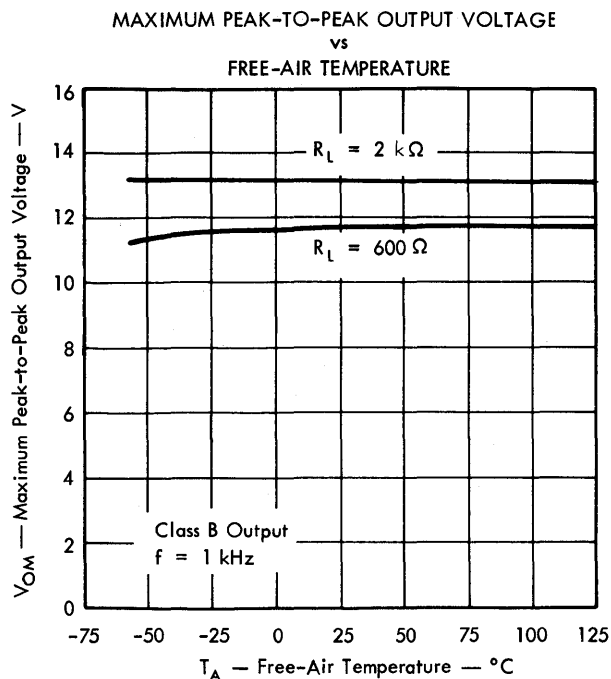


FIGURE 5

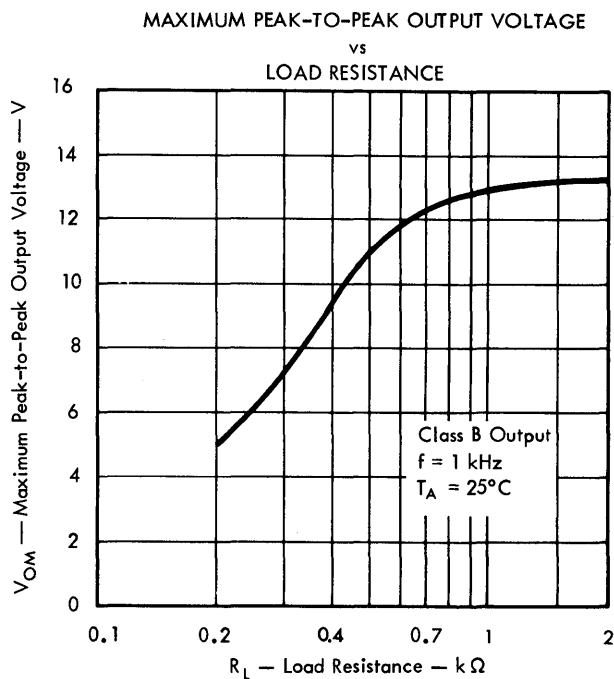


FIGURE 6

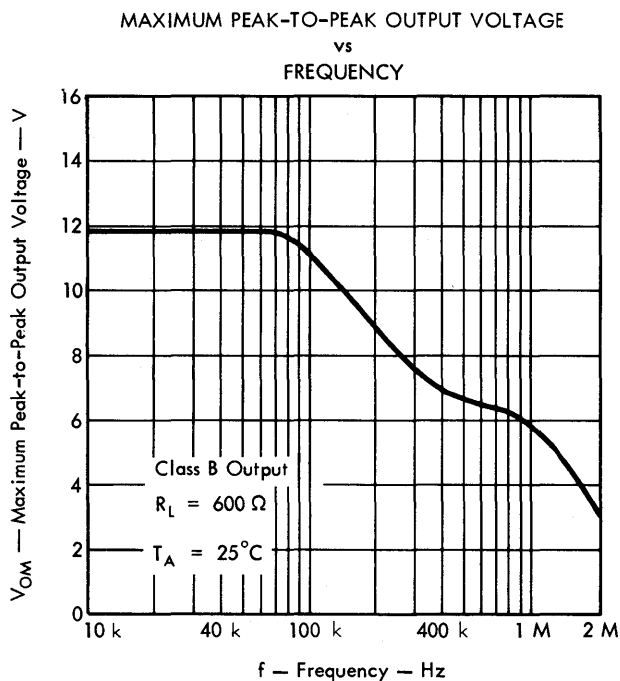
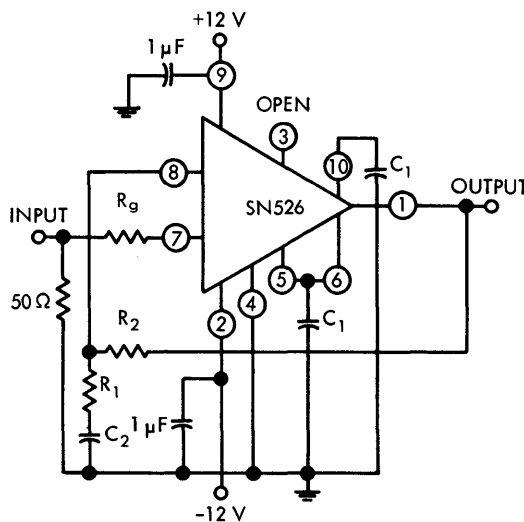


FIGURE 7



FREQUENCY RESPONSE TEST CIRCUIT

FIGURE 8

§ Unless otherwise noted, test conditions include:  $V_{CC1} = +12 \text{ V}$ ,  $V_{CC2} = -12 \text{ V}$ , ground and  $V_{DI}$  applied, no external load, and a  $0.05\text{-}\mu\text{F}$  capacitor between pin (3) and ground. All parameters except  $V_{OM}$  are measured with pin (5) grounded and pin (1) open.

# TYPE SN526 GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

## TYPICAL CHARACTERISTICS §

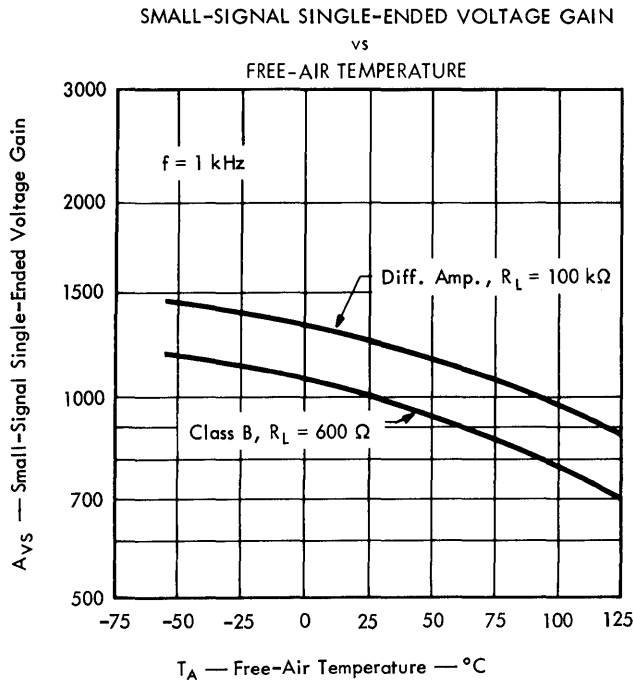


FIGURE 9

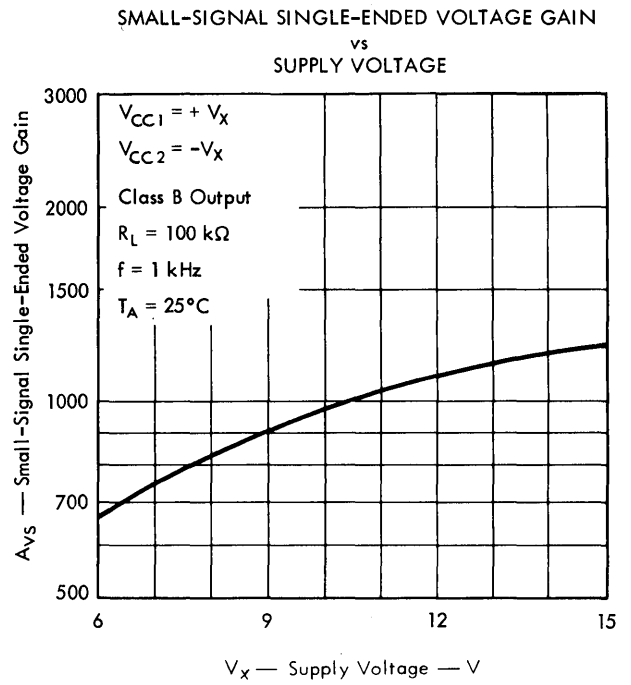


FIGURE 10

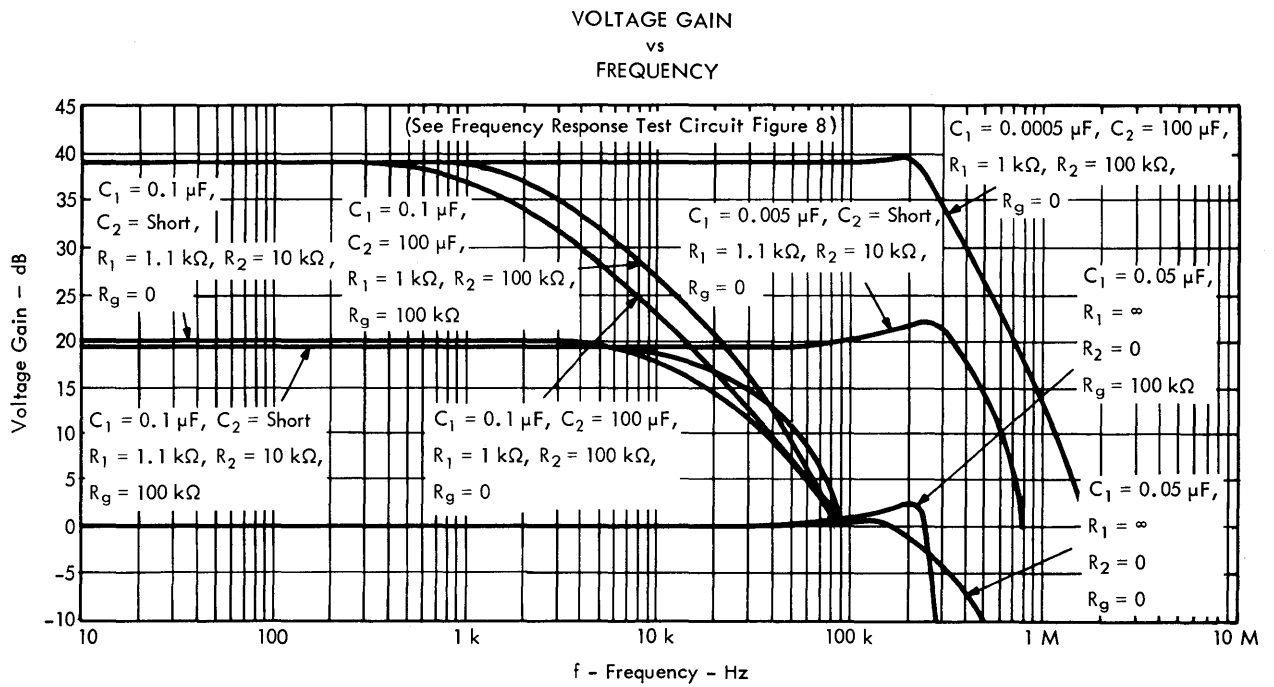


FIGURE 11

§ Unless otherwise noted, test conditions include:  $V_{CC1} = +12 \text{ V}$ ,  $V_{CC2} = -12 \text{ V}$ , ground and  $V_{D1}$  applied, no external load, and a  $0.05\text{-}\mu\text{F}$  capacitor between pin (3) and ground. All parameters except  $V_{OM}$  are measured with pin (5) grounded and pin (1) open.

# TYPE SN526

## GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

### TYPICAL CHARACTERISTICS §

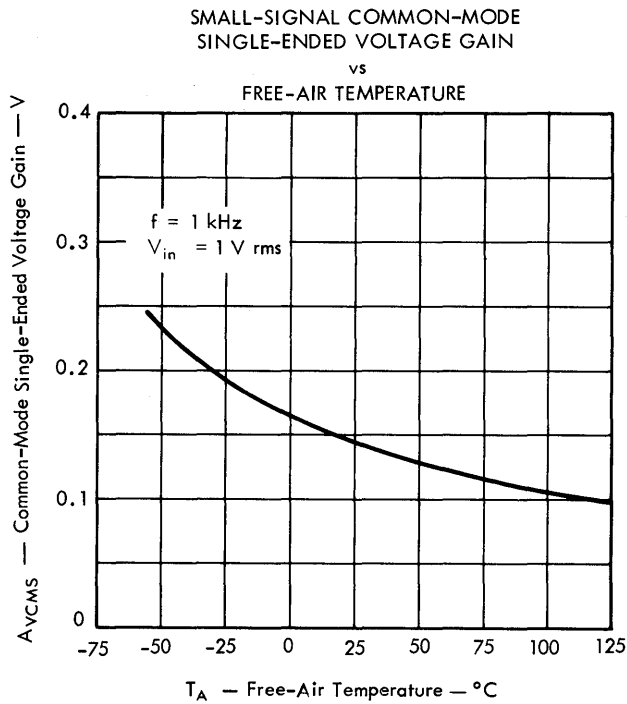


FIGURE 12

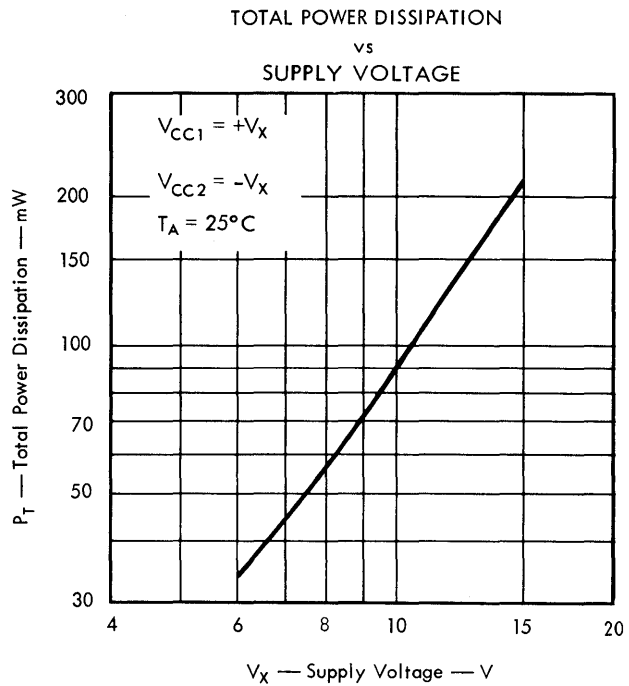


FIGURE 13

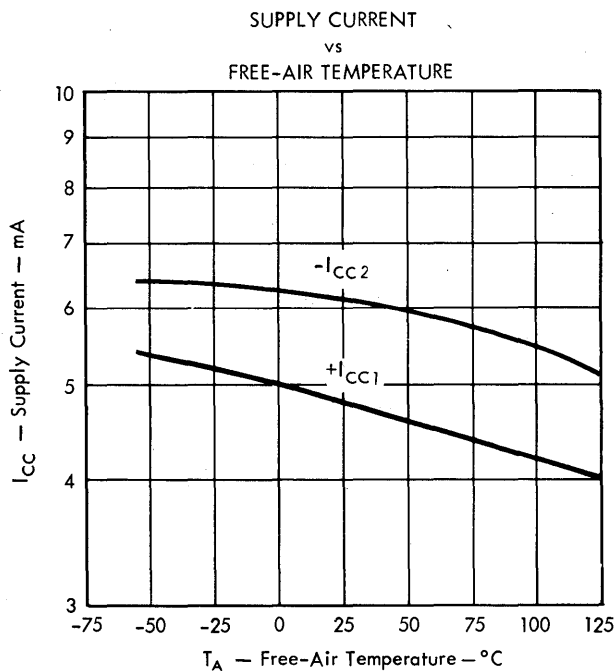


FIGURE 15

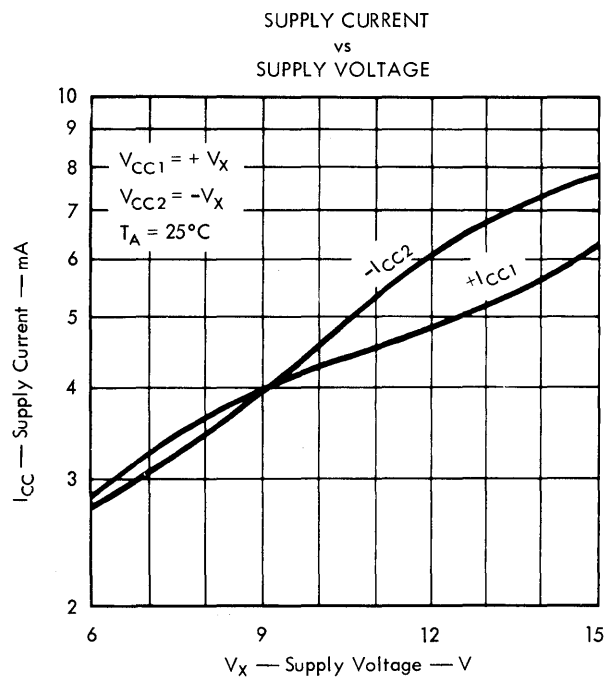


FIGURE 14

§ Unless otherwise noted, test conditions include:  $V_{CC1} = +12 \text{ V}$ ,  $V_{CC2} = -12 \text{ V}$ , ground and  $V_{DI}$  applied, no external load, and a  $0.05\text{-}\mu\text{F}$  capacitor between pin (3) and ground. All parameters except  $V_{OM}$  are measured with pin (5) grounded and pin (1) open.

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**A SERIES 55 HIGH-SPEED SEMICONDUCTOR NETWORK SENSE AMPLIFIER  
FOR APPLICATION IN  
MAGNETIC CORE MEMORIES FOR**  
• DIGITAL COMPUTER SYSTEMS • DATA HANDLING SYSTEMS • CONTROL SYSTEMS

TYPE SN5500  
BULLETIN NO. DI-S 657487, MARCH 1965  
REVISED AUGUST 1966

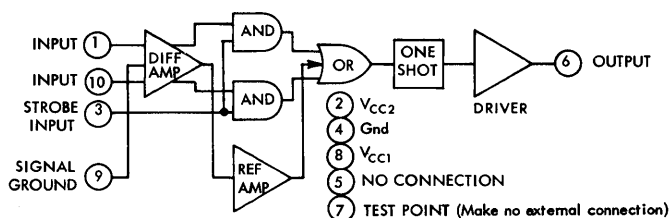
**description**

The SN5500 sense amplifier detects bipolar (positive or negative) differential-input signals from a magnetic core memory and provides the interface circuitry between the memory unit and the logic circuitry. In performing this function the sense amplifier accepts low-level pulses originating in the memory, discriminates between those representing logical 1 and those representing logical 0, and converts them to logic levels compatible with standard integrated logic circuitry.

The SN5500 is an amplitude-discriminating sense amplifier incorporating a threshold circuit with a narrow region of uncertainty. Signals of either polarity are accepted. A strobe input is provided so the threshold detector can be enabled when the signal-to-noise ratio is a maximum during the system read cycle and inhibited during the write cycle. It is recommended for core memory application with cycle times as low as two microseconds.

An internal one-shot pulse amplifier provides a standard-width negative-going output pulse when triggered by the threshold detector.

**FUNCTIONAL BLOCK DIAGRAM**



**PULSE TRUTH TABLE**

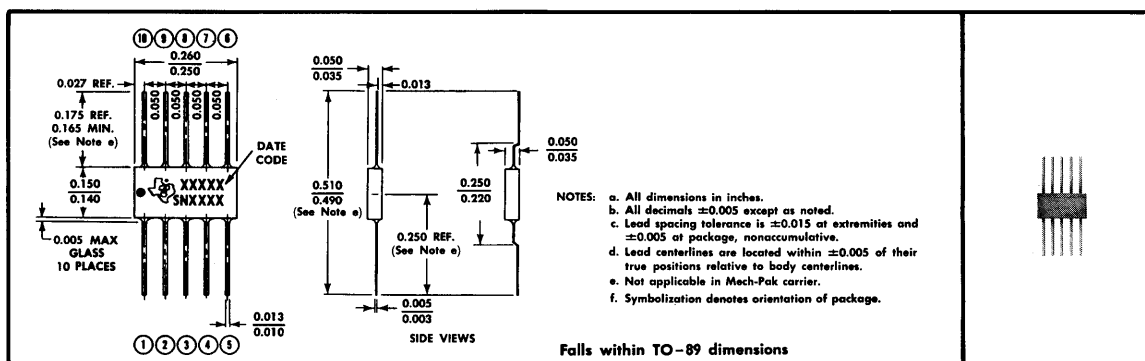
INPUT CONDITION		STROBE INPUT	OUTPUT
INPUT VOLTAGE MAGNITUDE			
$ V_{in}  < V_T$	Lo	$V_{off}$	
$ V_{in}  < V_T$	Hi	$V_{off}$	
$ V_{in}  > V_T$	Lo	$V_{off}$	
$ V_{in}  > V_T$	Hi	$V_{on}$	
$\pm V_{CMR}$	Lo	$V_{off}$	
$\pm V_{CMR}$	Hi	$V_{off}$	

**mechanical data**

The SN5500 Semiconductor Network is mounted in a glass-to-metal hermetically sealed welded package. Leads are gold-plated F-15<sup>‡</sup> glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. The SN5500 is available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier. See ordering instructions.

**ORDERING INSTRUCTIONS**

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
	0.175 inch				Not Applicable			
Lead Length	No	No	Yes	Yes	No	No	Yes	Yes
Formed Leads	No	Yes	No	Yes	No	Yes	No	Yes
Insulators	None	-6	-7	-1	-2	-3	-4	-5
Ordering Suffix								



<sup>†</sup>Patented by Texas Instruments

<sup>‡</sup>F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.



# TYPE SN5500

## SENSE AMPLIFIER WITH ONE-SHOT OUTPUT

### absolute maximum ratings over operating free-air temperature range

Supply Voltages: $V_{CC1}$ . . . . .	+6 v
$V_{CC2}$ . . . . .	-6 v
Strobe Input Voltage: $V_{strobe}$ . . . . .	+6 v
Operating Free-Air Temperature Range . . . . .	-55°C to 125°C
Storage Temperature Range . . . . .	-65°C to 150°C

### electrical characteristics, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT	
$V_T$ Input threshold voltage level		10	30	mv	
	$T_A = 25^\circ\text{C}$	15	19	mv	
$V_{TO}$ Input threshold offset voltage			4	mv	
$R_{in}$ Differential-input resistance	$V_{CC1} = +4.5\text{ v}, V_{CC2} = -4.5\text{ v},$ $V_{strobe} = +2.5\text{ v},$ $t_{p(strobe)} = 100\text{ nsec},$	150	300	$\Omega$	
$I_S$ Strobe input current			2.5	ma	
$V_{off}$ Off output level		$I_{load} = -3\text{ ma}$	2.5		v
$V_{on}$ On output level		$I_{sink} = 3\text{ ma}$		0.5	v
$V_{CMR}$ Common-mode rejection voltage		$t_r = t_f = 20\text{ nsec},$ $t_p = 100\text{ nsec}$	1		v
$P_T$ Total power dissipation				200	mw

### switching characteristics, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$t_{p(out)}$ Output pulse width	$V_{diff} = 50\text{ mv}$	200	800	nsec
$t_{pd}$ Propagation delay time	$V_{diff} = 50\text{ mv}$		125	nsec
$t_{od}$ Differential input overload recovery time	$V_{diff} = 250\text{ mv}$		100	nsec

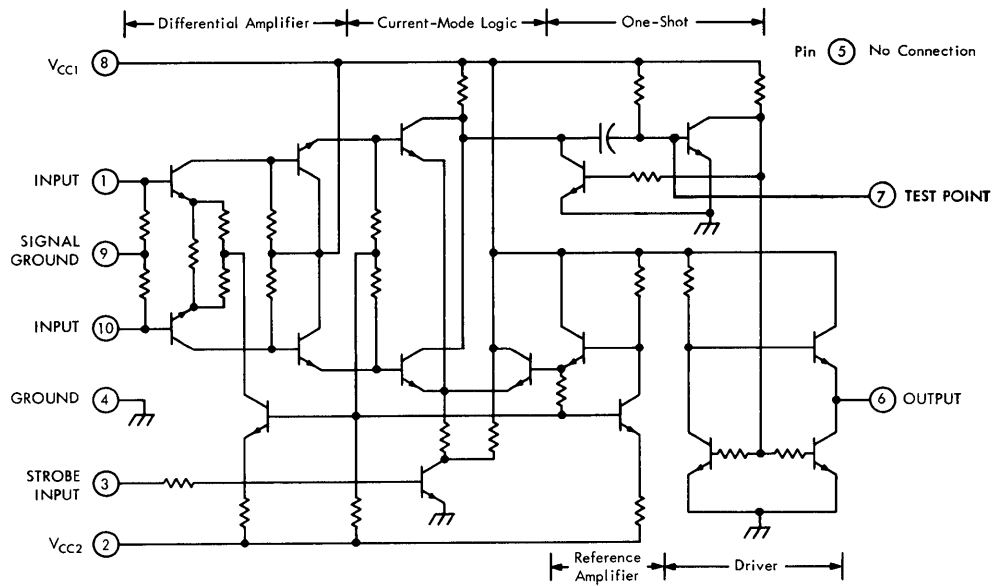
$V_{CC1} = +4.5\text{ v}, V_{CC2} = -4.5\text{ v},$   
 $V_{strobe} = +2.5\text{ v},$   
 $t_{p(strobe)} = 100\text{ nsec},$   
See Figure 4

### letter symbol and parameter definitions

- $V_T$  — Differential input signal level just sufficient to cause an output when coincident with a strobe signal. See Figure 2.
- $V_{TO}$  — Input threshold offset to opposite polarity input signals,  $|V_{T(1)} - V_{T(10)}|$ .
- $R_{in}$  — D-c resistance between input terminals.
- $I_S$  — Strobe input current.
- $V_{off}$  — High output-voltage level while supplying specified current.
- $V_{on}$  — Low output-voltage level while sinking specified current.
- $V_{CMR}$  — Common-mode signal that will not cause an output when a strobe signal is present.
- $t_{p(out)}$  — Output pulse width measured at 50-percent levels (see Figure 4).
- $V_{diff}$  — Differential voltage between input terminals.
- $t_{pd}$  — Propagation delay time from input leading edge to output leading edge measured at 50-percent levels with 50-mv input.
- $t_{od}$  — Strobe delay time after a specified differential overload noise signal required to inhibit an output.

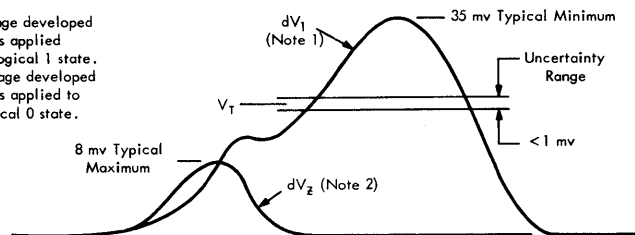
# TYPE SN5500

## SENSE AMPLIFIER WITH ONE-SHOT OUTPUT



**FIGURE 1 — CIRCUIT DIAGRAM**

- NOTES: 1.  $dV_1$  is the core output voltage developed when a read current pulse is applied to a core in the disturbed logical 1 state.  
 2.  $dV_2$  is the core output voltage developed when a read current pulse is applied to a core in the disturbed logical 0 state.



**FIGURE 2 — THRESHOLD CHARACTERISTICS**

(Referred to Typical Coincident-Current Memory Core  $dV_1$  and  $dV_2$  Output Voltage Waveforms)



# TYPE SN5500

## SENSE AMPLIFIER WITH ONE-SHOT OUTPUT

### PARAMETER MEASUREMENT INFORMATION

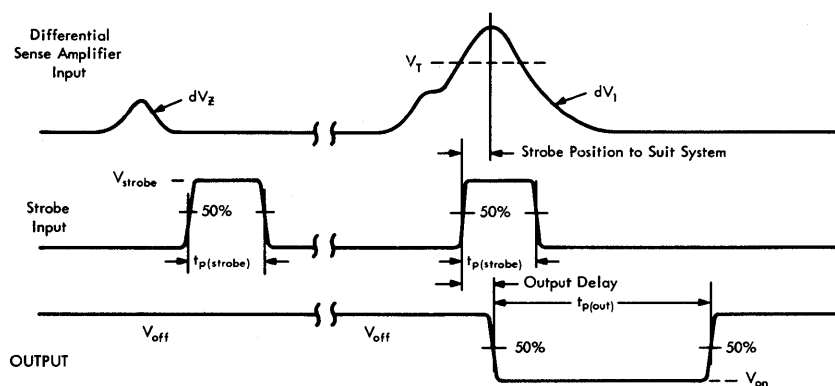


FIGURE 3 — TYPICAL SYSTEM TIMING DIAGRAM

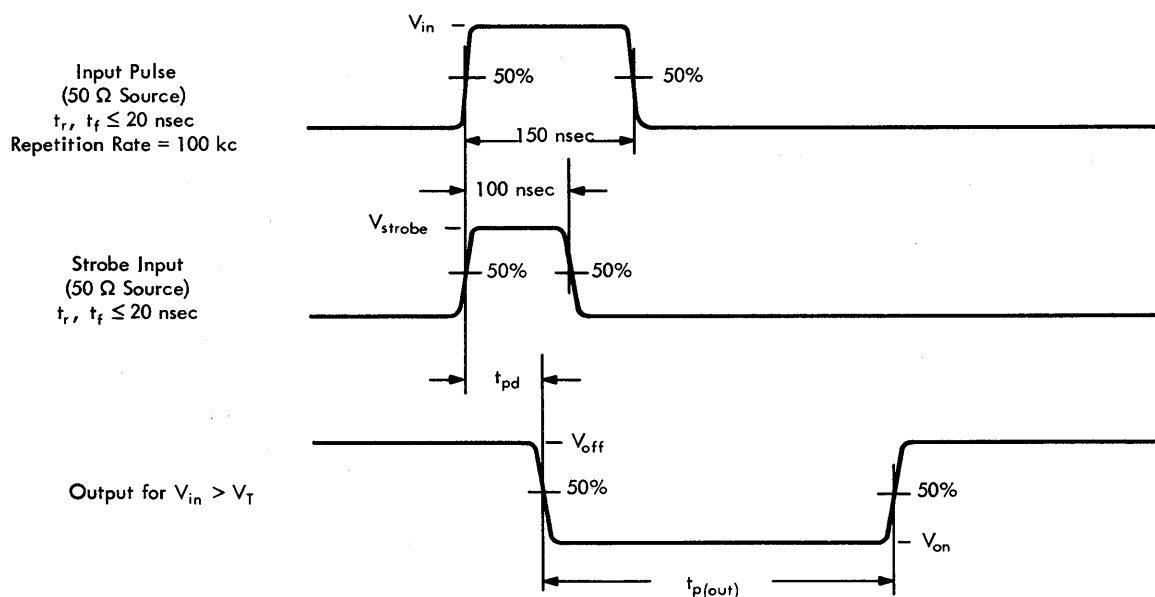


FIGURE 4 — TEST TIMING DIAGRAM FOR THRESHOLD AND SWITCHING CHARACTERISTICS



**SERIES 55 WIDE-BAND VIDEO AMPLIFIERS**

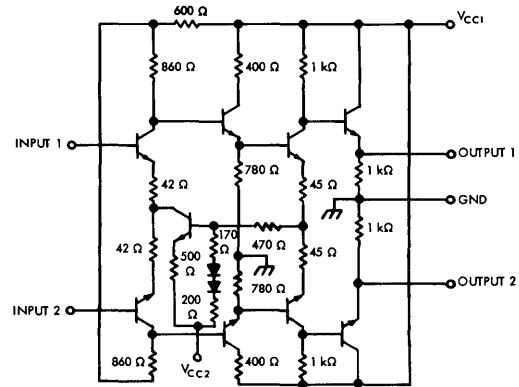
**FEATURING**

**Flat Frequency Response with Low Phase-Shift from DC to 40 MHz**

**description**

Each of these wide-band video amplifiers features a flat frequency response and low phase-shift from dc to 40 MHz. Differential inputs and outputs are provided which permit them to be used as high-frequency differential amplifiers.

Elements of the Series 55 video-amplifier bar include transistors with transition frequency as high as 1.2 GHz under low-current and low- $V_{CE}$  conditions. Circuit frequency response from dc to greater than 100 MHz is possible.



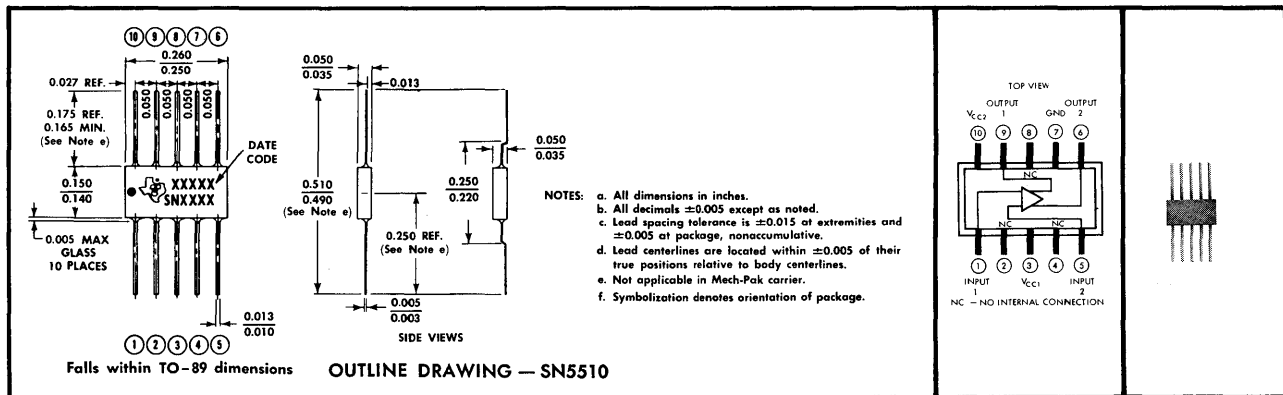
See logic symbols below for pin numbers

**mechanical data**

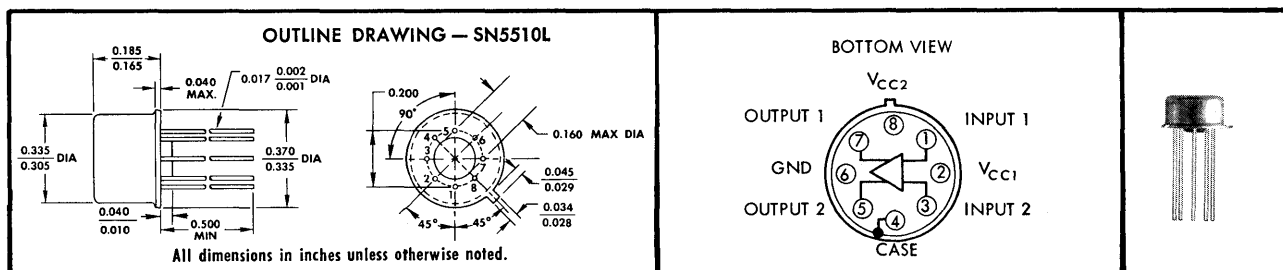
The SN5510 wide-band video amplifier is mounted in a glass-to-metal hermetically sealed welded package meeting TO-89. Leads are gold-plated F-15<sup>‡</sup> glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. The SN5510 is available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier. See Ordering Instructions.

**SN5510 ORDERING INSTRUCTIONS**

Lead Length	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5



The SN5510L package outline is same as JEDEC TO-99 except for diameter of standoff.



<sup>†</sup>Patented by Texas Instruments

<sup>‡</sup>F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.



# TYPES SN5510, SN5510L

## WIDE-BAND VIDEO AMPLIFIERS

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (See Note 1):	$V_{CC1}$	.....	+8 V
	$V_{CC2}$	.....	-8 V
Differential input voltage	.....	.....	5 V
Positive input voltage (See Note 1)	.....	.....	$V_{CC1}$
Negative input voltage (See Note 1)	.....	.....	$V_{CC2}$
Operating free-air temperature ranges:	SN5510	.....	-55°C to 70°C
	SN5510L	.....	-55°C to 100°C
Operating case temperature ranges:	SN5510	.....	-55°C to 100°C
	SN5510L	.....	-55°C to 125°C
Storage temperature range	.....	.....	-65°C to 150°C

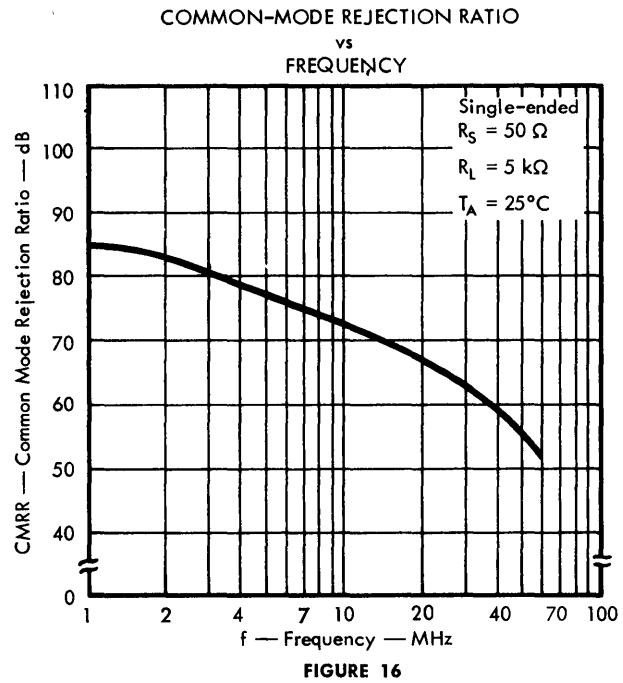
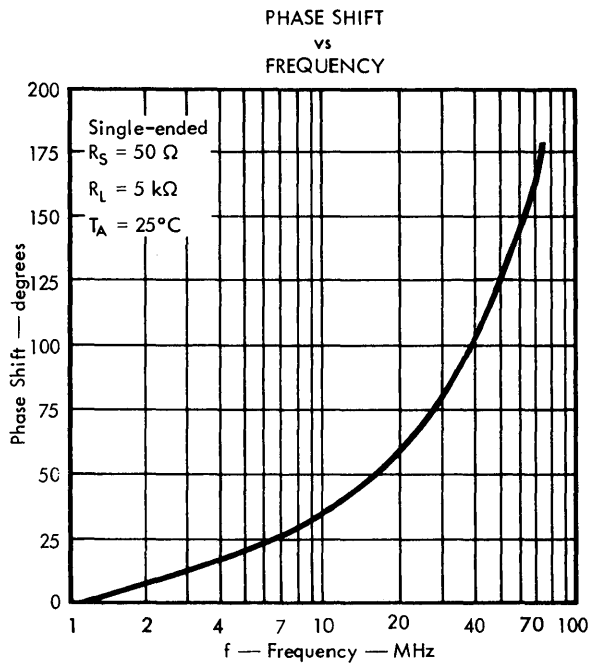
NOTE 1: These voltage values are with respect to network ground.

### electrical characteristics, $T_A = 25^\circ\text{C}$ , $V_{CC1} = +6\text{ V}$ , $V_{CC2} = -6\text{ V}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DO}$ Differential-output offset voltage	1			0.5	1.3	V
$V_{CMO(av)}$ Average common-mode output offset voltage	1		2.6	3.1	3.5	V
$I_{in}$ Input current	1			40	80	$\mu\text{A}$
$I_{DI}$ Differential-input offset current	1			3	20	$\mu\text{A}$
$D_S$ Single-ended output distortion	2	Load resistance = 5 k $\Omega$ , input distortion < 0.2%, $V_{out} = 1\text{ V rms}$ , $f = 10\text{ kHz}$		1.5	5	%
$V_{N(in)}$ Equivalent average input noise voltage	3	Single-ended, $R_S = 0$ , $f = 10\text{ Hz to } 500\text{ kHz}$		5		$\mu\text{V}$
$V_{CMIM}$ Maximum common-mode input voltage				$\pm 1$		V
$A_{vs}$ Small-signal voltage gain	2	Single-ended, load resistance = 5 k $\Omega$ , $f = 100\text{ kHz}$	75	93	110	
$A_{vcm}$ Common-mode-input voltage gain	4	Single-ended, load resistance = 5 k $\Omega$ , $V_{in} = 0.3\text{ V rms}$ , $f = 100\text{ kHz}$	-45		-30	dB
CMRR Common-mode rejection ratio	4	Load resistance = 5 k $\Omega$ , $f = 100\text{ kHz}$		85		dB
BW Bandwidth (-3 dB)	2			40		MHz
$r_{in}$ Input resistance	5	$f = 100\text{ kHz}$		6		k $\Omega$
$C_{in}$ Input capacitance	5	$f = 100\text{ kHz}$		7		pF
$z_{out}$ Output impedance	5	$f = 100\text{ kHz}$		35		$\Omega$
$P_T$ Total power dissipation	1	No input signal, no external load		165	220	mW
$t_r$ Rise time	6	Single-ended, $V_{in} = 5\text{ mV}$		9	12	ns
$t_f$ Fall time	6	Single-ended, $V_{in} = 5\text{ mV}$		9	12	ns

# TYPES SN5510, SN5510L WIDE-BAND VIDEO AMPLIFIERS

## TYPICAL CHARACTERISTICS §



$V_{CC1} = +6 \text{ V}$  and  $V_{CC2} = -6 \text{ V}$ .

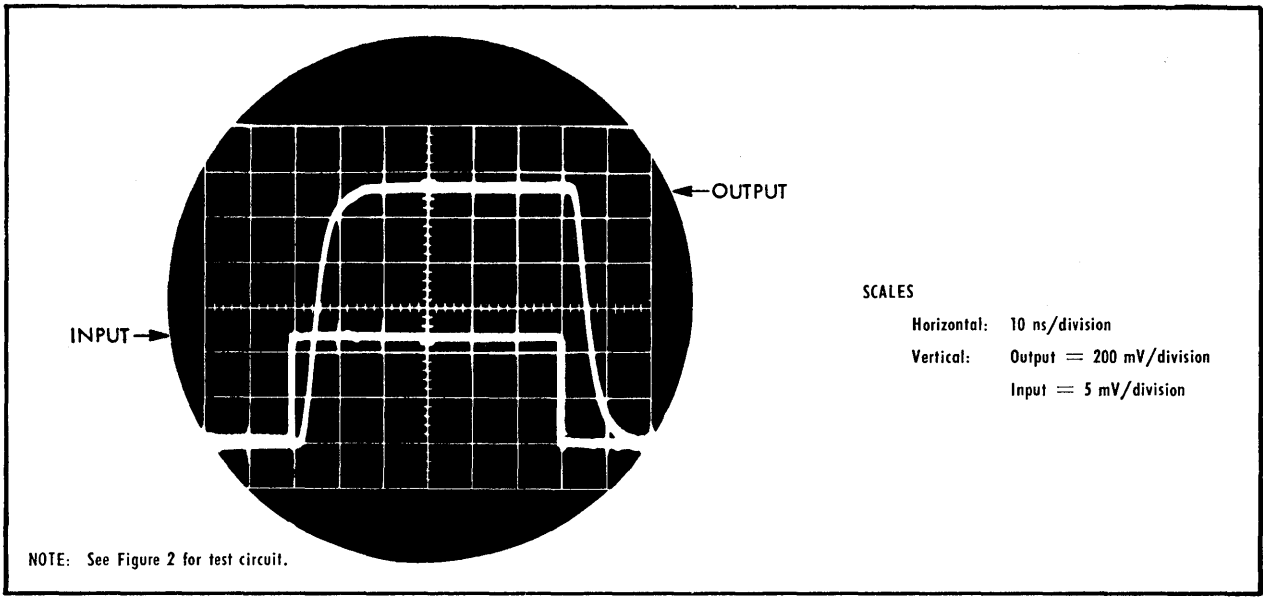


FIGURE 17 — OSCILLOSCOPE PRESENTATION OF PULSE RESPONSE

# TYPES SN5510, SN5510L

## WIDE-BAND VIDEO AMPLIFIERS

### TYPICAL CHARACTERISTICS §

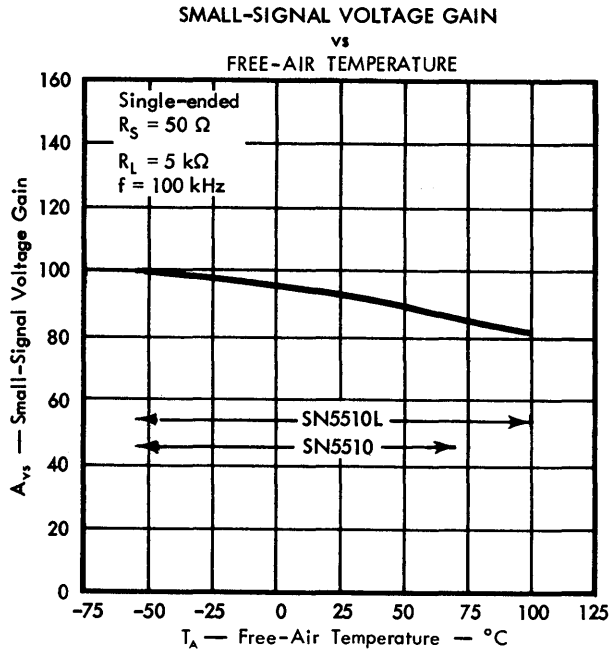


FIGURE 11

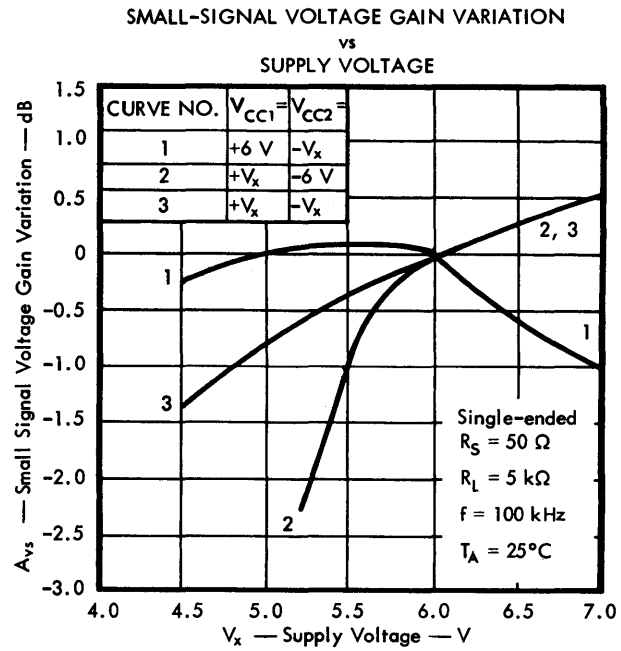


FIGURE 12

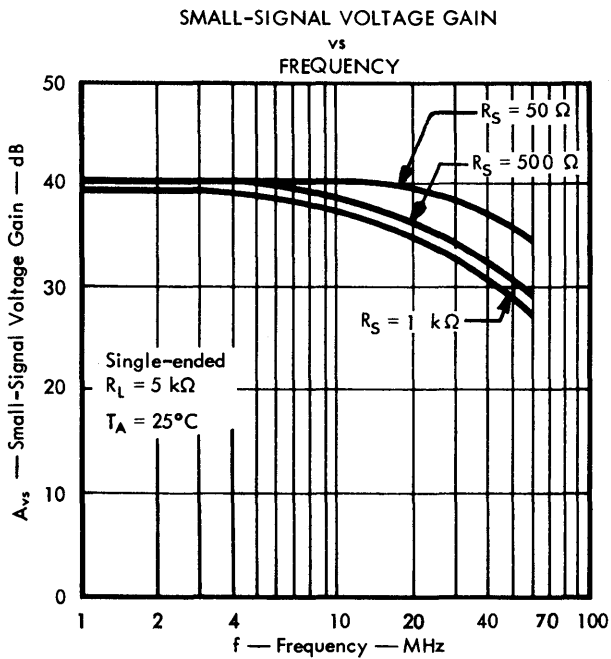


FIGURE 13

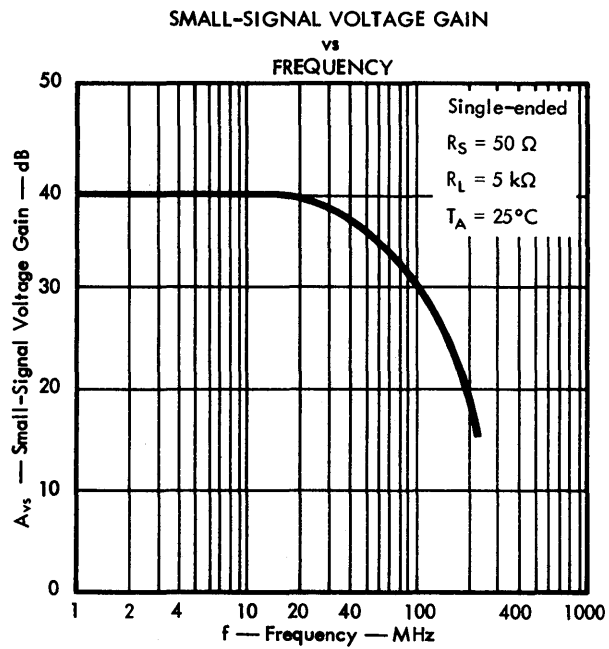


FIGURE 14

§Unless otherwise noted  $V_{CC1} = +6 \text{ V}$ ,  $V_{CC2} = -6 \text{ V}$ .

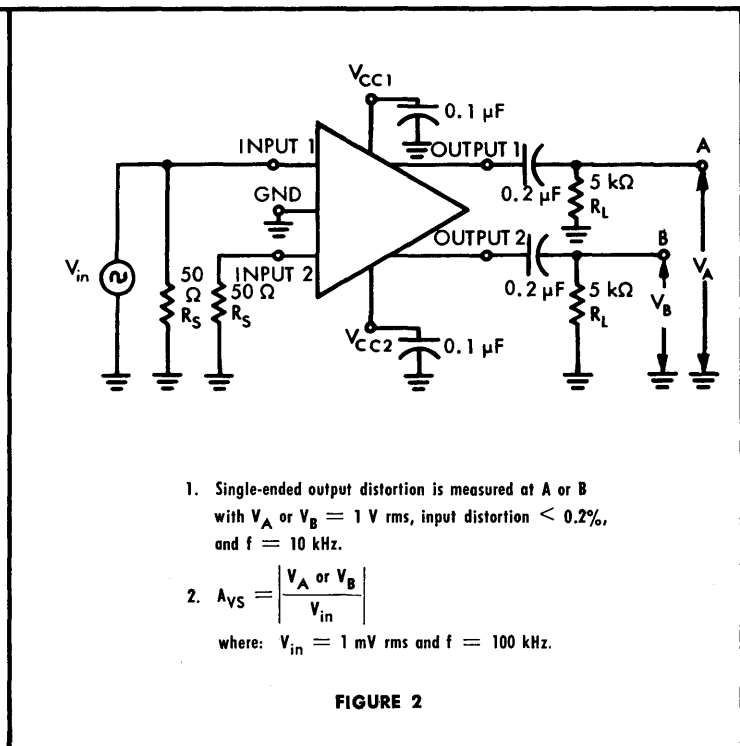
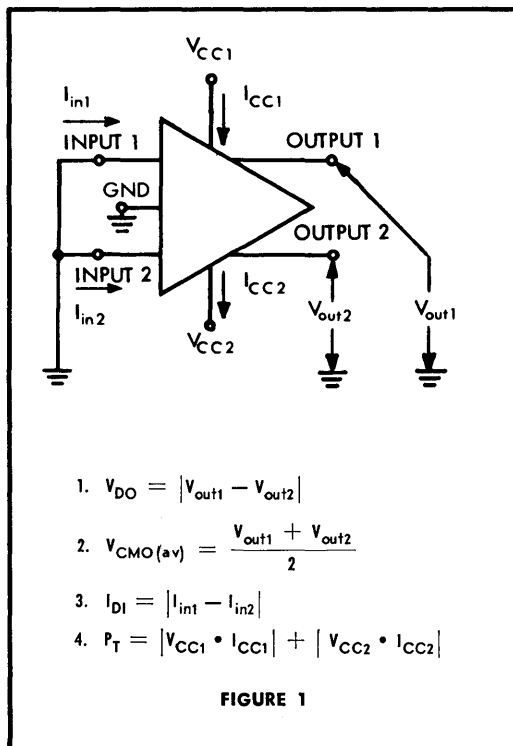
# TYPES SN5510, SN5510L WIDE-BAND VIDEO AMPLIFIERS

## letter symbol and parameter definitions

$V_{DO}$	The d-c differential voltage that exists between the output terminals when the input terminals are at ground.
$V_{CMO(av)}$	The average of the d-c output voltages with respect to ground when the input terminals are grounded.
$I_{DI}$	The difference in the currents into the two input terminals.
$V_{CMIM}$	The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.
CMRR	The ratio of the differential-mode voltage gain to the common-mode voltage gain.
BW	The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.

## PARAMETER MEASUREMENT INFORMATION

### test circuits



# TYPES SN5510, SN5510L

## WIDE-BAND VIDEO AMPLIFIERS

### PARAMETER MEASUREMENT INFORMATION

test circuits (continued)

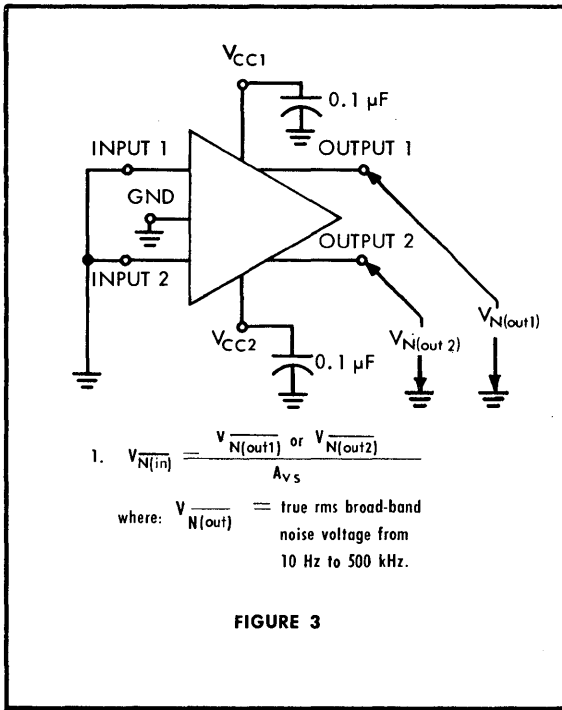


FIGURE 3

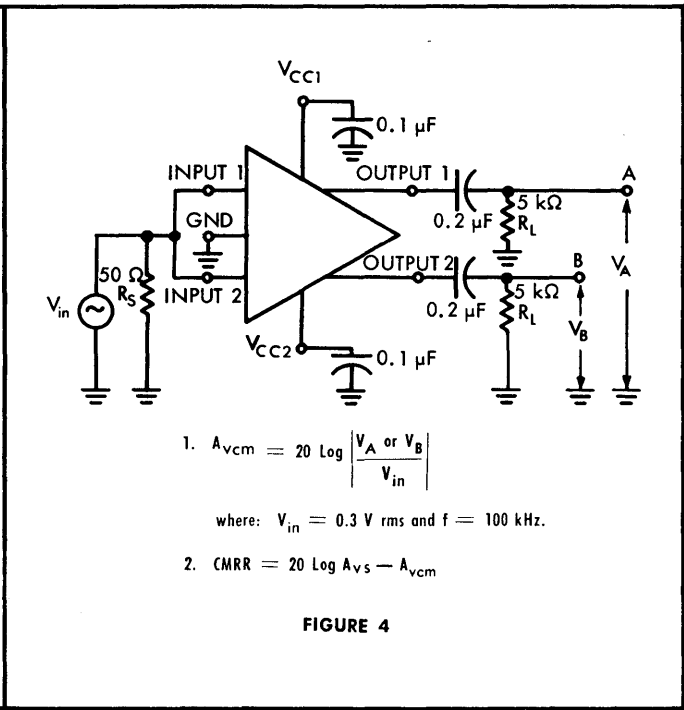


FIGURE 4

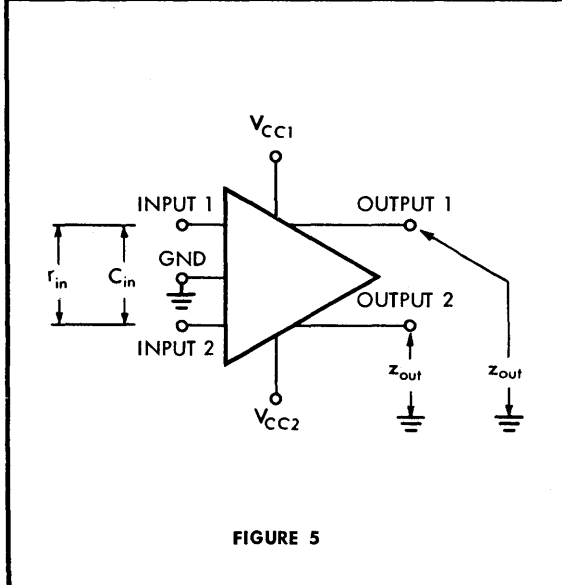


FIGURE 5

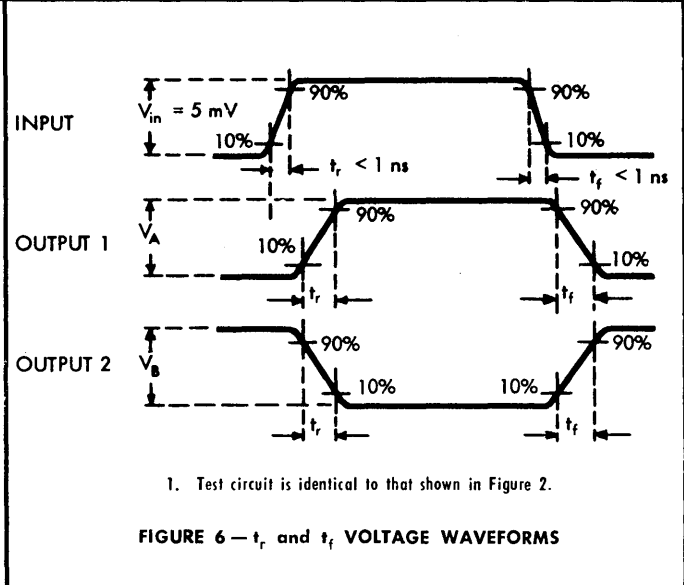


FIGURE 6 —  $t_r$  and  $t_f$  VOLTAGE WAVEFORMS

# TYPES SN5510, SN5510L MONOLITHIC WIDE-BAND VIDEO AMPLIFIERS

## TYPICAL CHARACTERISTICS §

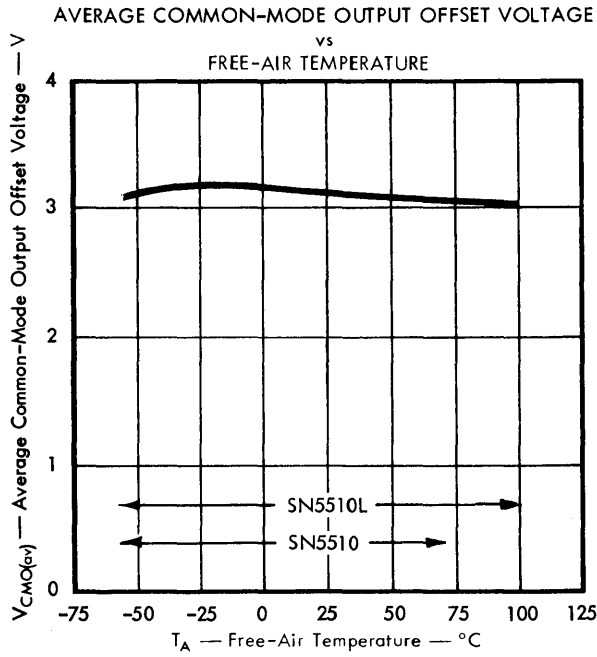


FIGURE 7

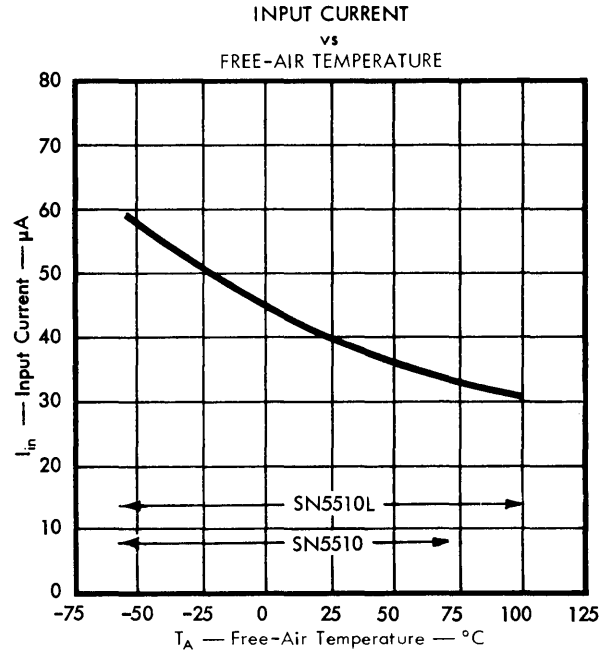


FIGURE 8

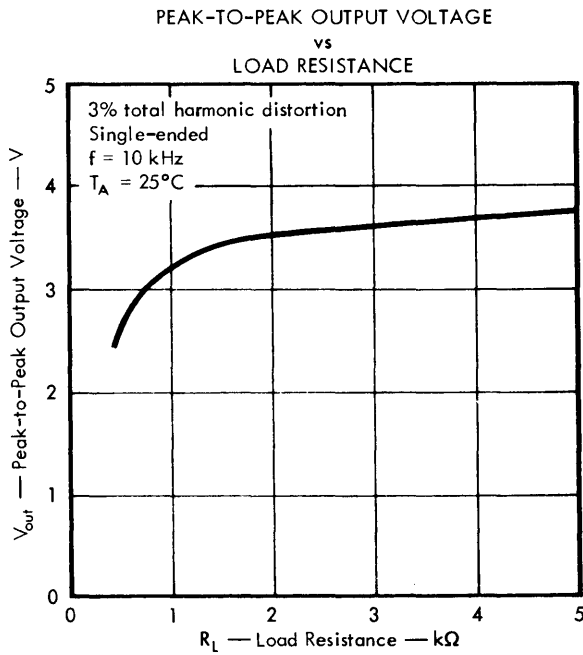


FIGURE 9

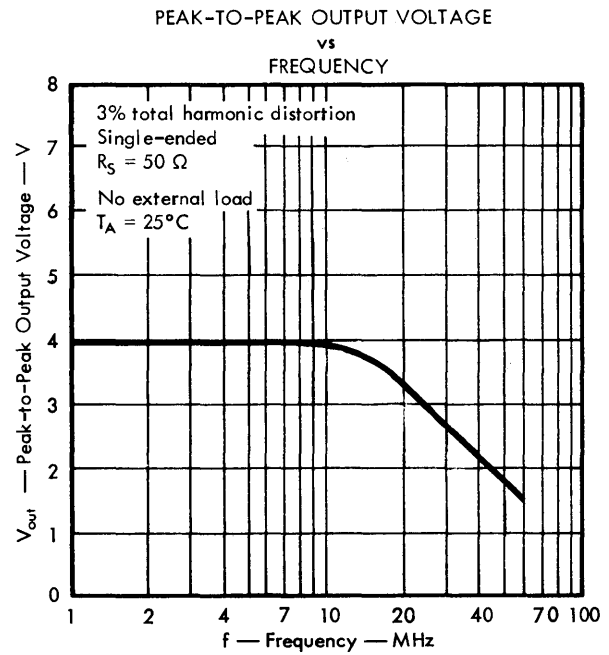


FIGURE 10

§Unless otherwise noted  $V_{CC1} = +6$  V,  $V_{CC2} = -6$  V.





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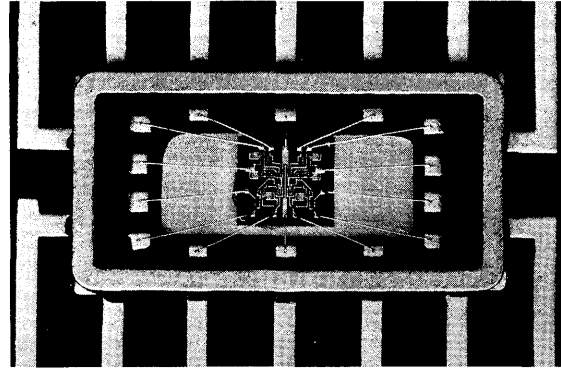
Texas Instruments Incorporated  
Post Office Box 5012  
Dallas, Texas 75222  
Attn: Jack Miller MS75



**HIGH-SPEED SATURATED TRANSISTOR-TRANSISTOR LOGIC CIRCUITS  
FOR GENERAL-PURPOSE DIGITAL SYSTEM APPLICATIONS**

**description**

Series 74 integrated circuits have been designed and characterized for high-speed, general-purpose digital applications where high d-c noise margin and relatively low power dissipation are important system considerations. Definitive specifications are provided for operating characteristics over the temperature range of 0°C to 70°C. This logic series includes the basic gates, flip-flop elements, and complex logic and storage elements needed to perform all functions required of general purpose industrial digital systems.



**TYPE SN7400 PRIOR TO CAPPING**

SERIES 74  
BULLETIN NO. D.L.S 669195, DECEMBER 1966  
REPLACES BULLETIN NO. D.L.S 657934, AUGUST 1965

**features**

**LOW SYSTEM COST**

- maximum number of circuits per package through use of 14-lead package

**OPTIMUM CIRCUIT PERFORMANCE**

- high speed — typical gate propagation delay time of 13 ns
- high d-c noise margin — typically one volt
- low output impedance provides low a-c noise susceptibility
- waveform integrity over full range of loading and temperature conditions
- low power dissipation — 10 mW per gate at 50% duty cycle
- full fan-out of 10

CONTENTS	Page
CIRCUIT DESIGN CHARACTERISTICS AND OPERATION . . . . .	5002
LOGIC DEFINITION AND SYMBOLS . . . . .	5003-5004
DEFINITIVE SPECIFICATIONS . . . . .	5005-5031
D-C TEST CIRCUITS . . . . .	5032-5043
SWITCHING TIME TEST CIRCUITS AND VOLTAGE WAVEFORMS . . . . .	5044-5052
TYPICAL CHARACTERISTICS . . . . .	5053-5055
MECHANICAL DATA . . . . .	5056

<sup>†</sup>Patented by Texas Instruments.

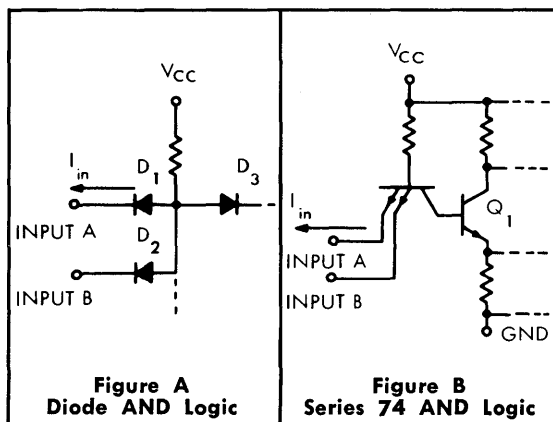


**design characteristics**

Series 74 digital integrated circuits effect an optimization between saturated logic circuitry and monolithic semiconductor technology yielding high performance at lowest cost. In discrete-component circuitry maximum use is made of lower cost components (diodes and resistors) instead of the higher priced transistors. However, in monolithic circuitry it costs no more to build transistors than diodes or resistors. Therefore, in Series 74, transistors are used to buffer the fluctuations in currents that occur as resistor values change. Also, the Series 74 multiple-emitter transistor can easily be built in a monolithic bar to eliminate the need for conventional input diodes.

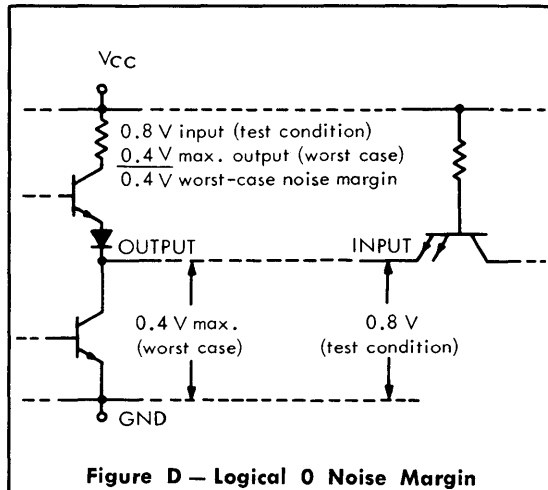
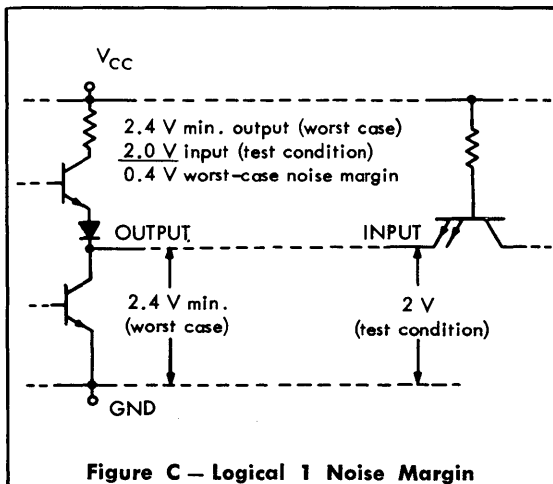
**circuit operation**

The transistor-transistor logic (TTL) used in Series 74 is analogous to diode-transistor logic (DTL) in certain respects. As shown in figure A, a low voltage at inputs A or B will allow current to flow through the diode associated with the low input, and no drive current will pass through diode  $D_3$ . If inputs A and B are raised to a high voltage, drive current will then pass through diode  $D_3$ .



In Series 74 TTL circuitry, the multiple-emitter transistor performs the same function as the diodes in DTL (see figure B). However, the transistor action of the multiple-emitter transistor causes transistor  $Q_1$  to turn-off more rapidly, thus providing an inherent switching-time advantage over the DTL circuit.

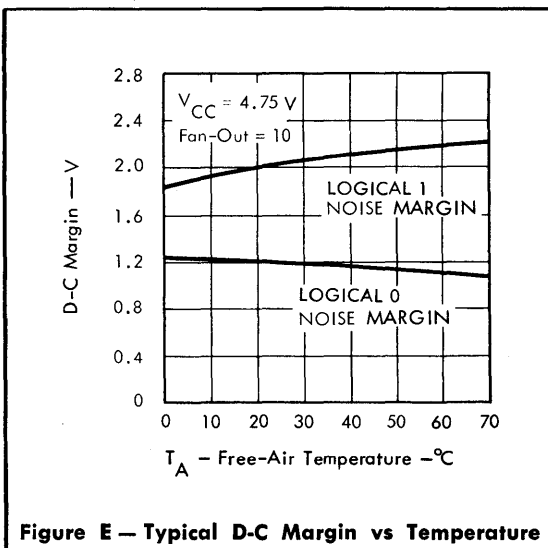
Although one-volt d-c noise margins are typical for Series 74 circuits, an absolute guarantee of 400 millivolts is assured for every unit. This is accomplished by testing each output and input as shown in figures C and D.



Each output is tested to ensure that the logical 1 output voltage will not fall below 2.4 volts. This is done with full fan-out, lowest  $V_{CC}$ , and 0.8 volt on the input — 400 mV more than the logical 0 maximum.

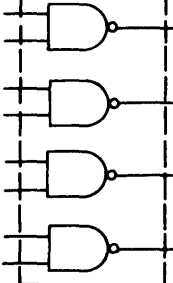
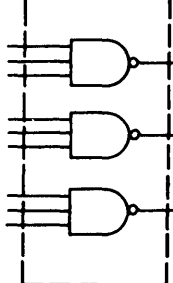
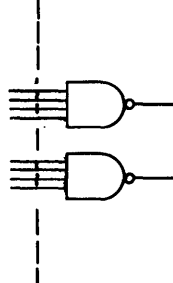
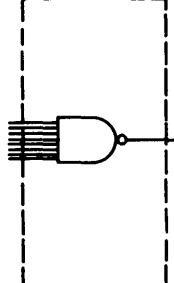
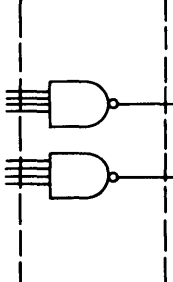
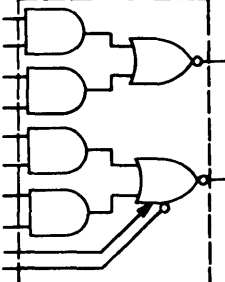
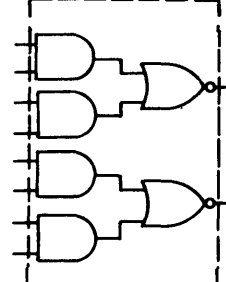
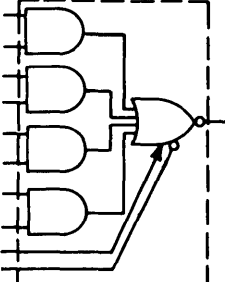
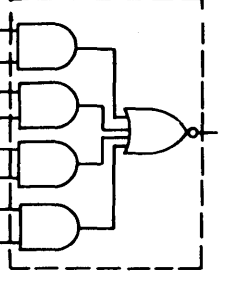
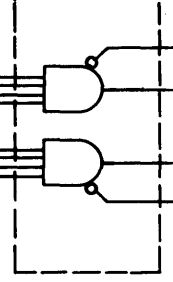
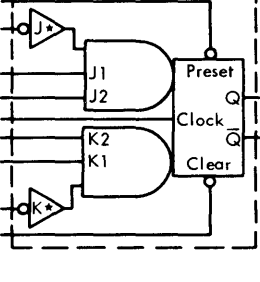
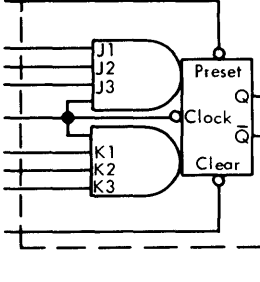
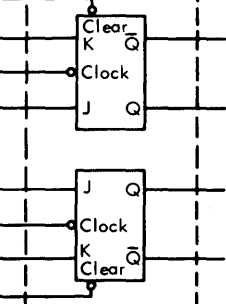
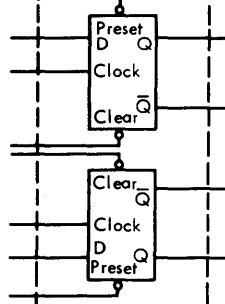
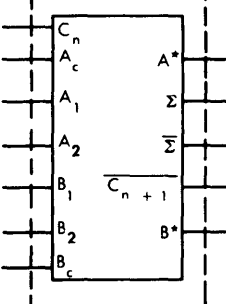
Each output is tested to ensure that the logical 0 output voltage will not exceed 0.4 volt. This is done with full fan-out, lowest  $V_{CC}$ , and 2 volts on the input — 400 mV less than the logical 1 minimum.

In actual system operation, the majority of circuits do not experience worst-case conditions of fan-out, supply voltage, temperature, and input voltage simultaneously. In addition, the threshold voltage of the Series 74 circuits is about 1.5 volts. These characteristics allow a larger voltage change on an input without false triggering. This typical noise margin is shown in figure E.



Another important feature of the design is the output configuration which both supplies current (in the logical 1 state) and sinks current (in the logical 0 state) from a low impedance. Typically, logical 0 output impedance is 12  $\Omega$  and logical 1 output impedance is 70  $\Omega$ . This low output impedance in either state rejects capacitively coupled a-c pulses and ensures small R-C time constants which preserve wave-shape integrity.

## standard line summary

<p><b>SN7400</b> See Page 5005</p>  <p style="text-align: center;"><b>QUADRUPLE 2-INPUT POSITIVE NAND GATE</b></p>	<p><b>SN7410</b> See Page 5006</p>  <p style="text-align: center;"><b>TRIPLE 3-INPUT POSITIVE NAND GATE</b></p>	<p><b>SN7420</b> See Page 5007</p>  <p style="text-align: center;"><b>DUAL 4-INPUT POSITIVE NAND GATE</b></p>	<p><b>SN7430</b> See Page 5008</p>  <p style="text-align: center;"><b>8-INPUT POSITIVE NAND GATE</b></p>
<p><b>SN7440</b> See Page 5009</p>  <p style="text-align: center;"><b>DUAL 4-INPUT POSITIVE NAND BUFFER</b></p>	<p><b>SN7450</b> See Page 5010</p>  <p style="text-align: center;"><b>EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE</b></p>	<p><b>SN7451</b> See Page 5010</p>  <p style="text-align: center;"><b>DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE</b></p>	<p><b>SN7453</b> See Page 5012</p>  <p style="text-align: center;"><b>EXPANDABLE 4-WIDE 2-INPUT AND-OR-INVERT GATE</b></p>
<p><b>SN7454</b> See Page 5012</p>  <p style="text-align: center;"><b>4-WIDE 2-INPUT AND-OR-INVERT GATE</b></p>	<p><b>SN7460</b> See Page 5014</p>  <p style="text-align: center;"><b>DUAL 4-INPUT EXPANDER</b></p>	<p><b>SN7470</b> See Page 5015</p>  <p style="text-align: center;"><b>J-K FLIP-FLOP</b></p>	<p><b>SN7472</b> See Page 5018</p>  <p style="text-align: center;"><b>J-K MASTER-SLAVE FLIP-FLOP</b></p>
<p><b>SN7473</b> See Page 5021</p>  <p style="text-align: center;"><b>DUAL J-K MASTER-SLAVE FLIP-FLOP</b></p>	<p><b>SN7474</b> See Page 5024</p>  <p style="text-align: center;"><b>DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP</b></p>	<p><b>SN7480</b> See Page 5027</p>  <p style="text-align: center;"><b>GATED FULL ADDER</b></p>	

# SERIES 74

## **SOLID CIRCUIT**<sup>®</sup> SEMICONDUCTOR NETWORKS

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage $V_{CC}$ (See Note 1) . . . . .	7 V
Input Voltage $V_{in}$ (See Notes 1 and 2) . . . . .	5.5 V
Operating Free-Air Temperature Range . . . . .	0°C to 70°C
Storage Temperature Range . . . . .	-65°C to 150°C

- NOTES: 1. Voltage values are with respect to network ground terminal.  
2. Input signals must be zero or positive with respect to network ground terminal.

### logic definition

Series 74 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE = LOGICAL 0  
HIGH VOLTAGE = LOGICAL 1

### input-current requirements

Input-current requirements reflect worst-case conditions for  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  and  $V_{CC} = 4.75\text{ V}$  to  $5.25\text{ V}$ . Each input of the multiple-emitter input transistor requires that no more than  $-1.6\text{ mA}$  flow out of the input at a logical 0 voltage level; therefore, one load ( $N = 1$ ) is  $-1.6\text{ mA}$  maximum. Each input requires current into the input at a logical 1 voltage level. This current is  $40\ \mu\text{A}$  maximum for each emitter input. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

### fan-out capability

Fan-out reflects the ability of an output to sink current from a number of loads ( $N$ ) at a logical 0 voltage level and to supply current at a logical 1 voltage level. Each standard output is capable of sinking current or supplying current to 10 loads ( $N = 10$ ). The buffer gate is capable of sinking current or supplying current to 30 loads ( $N = 30$ ). The carry output ( $C_{n+1}$ ) of the full adder is capable of driving 5 loads ( $N = 5$ ) and the  $A^*$  and  $B^*$  nodes may be used to drive 3 loads ( $N = 3$ ). Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuits indicate the actual direction of current flow.

### unused inputs

For optimum switching times, unused gate inputs should be tied to a positive voltage source of  $2.4\text{ V}$  to  $5.5\text{ V}$ . This eliminates the distributed capacitance associated with the floating input-transistor emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Supply voltage  $V_{CC}$ , if regulated to  $5.5\text{ V}$  maximum, may be used.

If the supply voltage  $V_{CC}$  cannot be limited to  $5.5\text{ V}$  the following alternatives are recommended:

- Connect unused gate inputs to an independent supply voltage source of  $2.4\text{ V}$  to  $5.5\text{ V}$ .
- Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded.

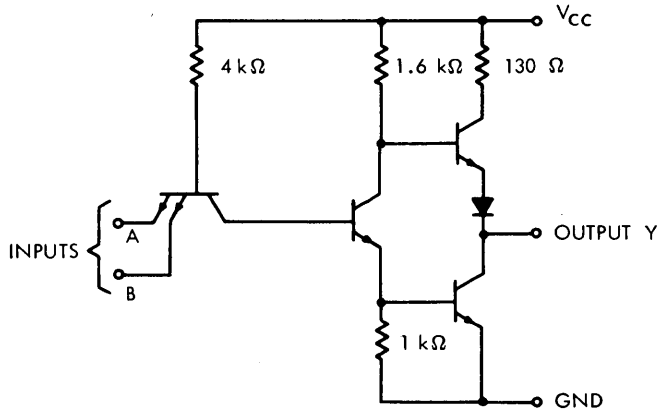
In all cases, unused  $J^*$  and  $K^*$  inputs of the SN7470 must be connected to ground.

Instructions for terminating unused inputs of the SN7480 are provided in the applications shown for that device.

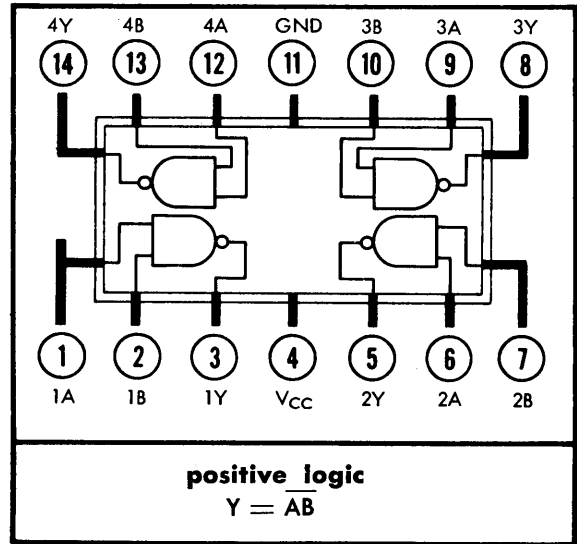
# TYPE SN7400

## QUADRUPLE 2-INPUT POSITIVE NAND GATE

schematic (each gate)



Component values shown are nominal.



### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	4.75 V to 5.25 V
Fan-Out From Each Output, N . . . . .	1 to 10

### electrical characteristics, $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	$V_{CC} = 4.75\text{ V}$ , $V_{out(0)} \leq 0.4\text{ V}$	2			V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	$V_{CC} = 4.75\text{ V}$ , $V_{out(1)} \geq 2.4\text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	2	$V_{CC} = 4.75\text{ V}$ , $I_{load} = -400\ \mu\text{A}$ , $V_{in} = 0.8\text{ V}$	2.4	3.3 $\ddagger$		V
$V_{out(0)}$ Logical 0 output voltage	1	$V_{CC} = 4.75\text{ V}$ , $I_{sink} = 16\text{ mA}$ , $V_{in} = 2\text{ V}$		0.22 $\ddagger$	0.4	V
$I_{in(0)}$ Logical 0 level input current (each input)	3	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 0.4\text{ V}$			-1.6	mA
$I_{in(1)}$ Logical 1 level input current (each input)	4	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 2.4\text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.25\text{ V}$ , $V_{in} = 5.5\text{ V}$			1	mA
$I_{OS}$ Short-circuit output current $\dagger$	5	$V_{CC} = 5.25\text{ V}$	-18		-55	mA
$I_{CC(0)}$ Logical 0 level supply current (each gate)	6	$V_{CC} = 5\text{ V}$ , $V_{in} = 5\text{ V}$		3 $\ddagger$		mA
$I_{CC(1)}$ Logical 1 level supply current (each gate)	6	$V_{CC} = 5\text{ V}$ , $V_{in} = 0$		1 $\ddagger$		mA

### switching characteristics, $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ , $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$ Propagation delay time to logical 0 level	50	$C_1 = 15\text{ pF}$		8	15	ns
$t_{pd1}$ Propagation delay time to logical 1 level	50	$C_1 = 15\text{ pF}$		18	29	ns

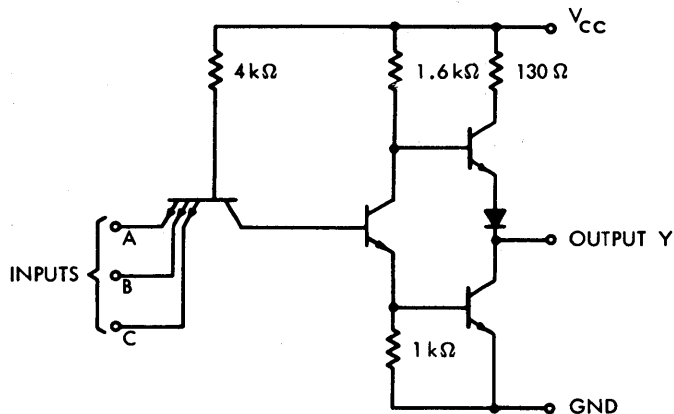
$\dagger$ Not more than one output should be shorted at a time.

$\ddagger$ These typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

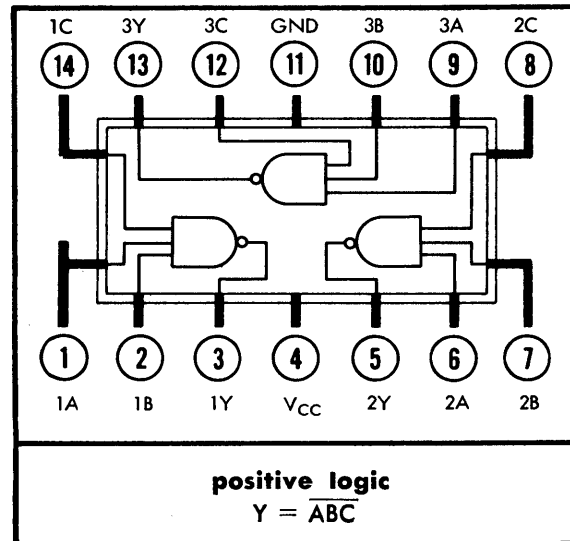
# TYPE SN7410

## TRIPLE 3-INPUT POSITIVE NAND GATE

schematic (each gate)



Component values shown are nominal.



### recommended operating conditions

Supply Voltage $V_{CC}$	4.75 V to 5.25 V
Fan-Out From Output, N	1 to 10

### electrical characteristics, $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	$V_{CC} = 4.75\text{ V}$ , $V_{out(0)} \leq 0.4\text{ V}$	2			V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	$V_{CC} = 4.75\text{ V}$ , $V_{out(1)} \geq 2.4\text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	2	$V_{CC} = 4.75\text{ V}$ , $I_{load} = -400\ \mu\text{A}$ , $V_{in} = 0.8\text{ V}$	2.4	3.3 $\ddagger$		V
$V_{out(0)}$ Logical 0 output voltage	1	$V_{CC} = 4.75\text{ V}$ , $I_{sink} = 16\text{ mA}$ , $V_{in} = 2\text{ V}$		0.22 $\ddagger$	0.4	V
$I_{in(0)}$ Logical 0 level input current (each input)	3	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 0.4\text{ V}$			-1.6	mA
$I_{in(1)}$ Logical 1 level input current (each input)	4	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 2.4\text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.25\text{ V}$ , $V_{in} = 5.5\text{ V}$			1	mA
$I_{OS}$ Short-circuit output current $\dagger$	5	$V_{CC} = 5.25\text{ V}$	-18		-55	mA
$I_{CC(0)}$ Logical 0 level supply current (each gate)	6	$V_{CC} = 5\text{ V}$ , $V_{in} = 5\text{ V}$		3 $\ddagger$		mA
$I_{CC(1)}$ Logical 1 level supply current (each gate)	6	$V_{CC} = 5\text{ V}$ , $V_{in} = 0$		1 $\ddagger$		mA

### switching characteristics, $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ , $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$ Propagation delay time to logical 0 level	50	$C_1 = 15\text{ pF}$		8	15	ns
$t_{pd1}$ Propagation delay time to logical 1 level	50	$C_1 = 15\text{ pF}$		18	29	ns

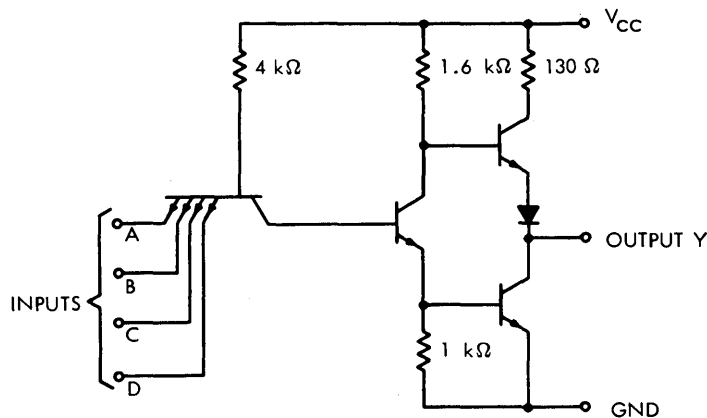
$\dagger$ Not more than one output should be shorted at a time.

$\ddagger$ These typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

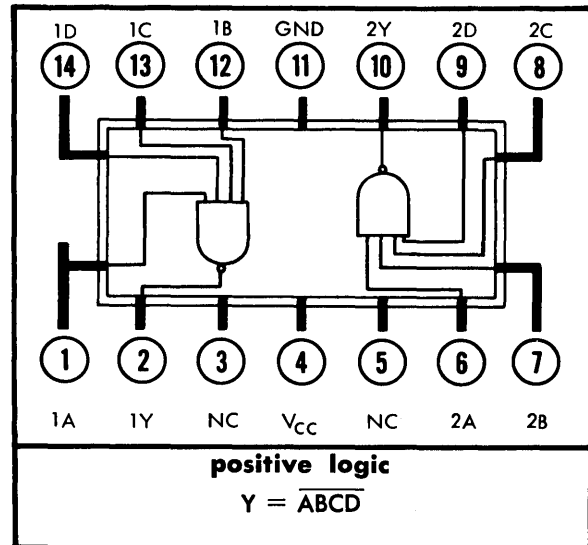
# TYPE SN7420

## DUAL 4-INPUT POSITIVE NAND GATE

schematic (each gate)



Component values shown are nominal.



### recommended operating conditions

Supply Voltage $V_{CC}$	4.75 V to 5.25 V
Fan-Out From Each Output, N	1 to 10

### electrical characteristics, $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	$V_{CC} = 4.75 \text{ V}$ , $V_{out(0)} \leq 0.4 \text{ V}$	2			V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	$V_{CC} = 4.75 \text{ V}$ , $V_{out(1)} \geq 2.4 \text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	2	$V_{CC} = 4.75 \text{ V}$ , $V_{in} = 0.8 \text{ V}$ , $I_{load} = -400 \mu\text{A}$	2.4	3.3‡		V
$V_{out(0)}$ Logical 0 output voltage	1	$V_{CC} = 4.75 \text{ V}$ , $V_{in} = 2 \text{ V}$ , $I_{sink} = 16 \text{ mA}$	0.22‡	0.4		V
$I_{in(0)}$ Logical 0 level input current (each input)	3	$V_{CC} = 5.25 \text{ V}$ , $V_{in} = 0.4 \text{ V}$			-1.6	mA
$I_{in(1)}$ Logical 1 level input current (each input)	4	$V_{CC} = 5.25 \text{ V}$ , $V_{in} = 2.4 \text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.25 \text{ V}$ , $V_{in} = 5.5 \text{ V}$			1	mA
$I_{OS}$ Short-circuit output current†	5	$V_{CC} = 5.25 \text{ V}$	-18		-55	mA
$I_{CC(0)}$ Logical 0 level supply current (each gate)	6	$V_{CC} = 5 \text{ V}$ , $V_{in} = 5 \text{ V}$		3‡		mA
$I_{CC(1)}$ Logical 1 level supply current (each gate)	6	$V_{CC} = 5 \text{ V}$ , $V_{in} = 0$		1‡		mA

### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$ , $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$ Propagation delay time to logical 0 level	50	$C_1 = 15 \text{ pF}$		8	15	ns
$t_{pd1}$ Propagation delay time to logical 1 level	50	$C_1 = 15 \text{ pF}$		18	29	ns

†Not more than one output should be shorted at a time.

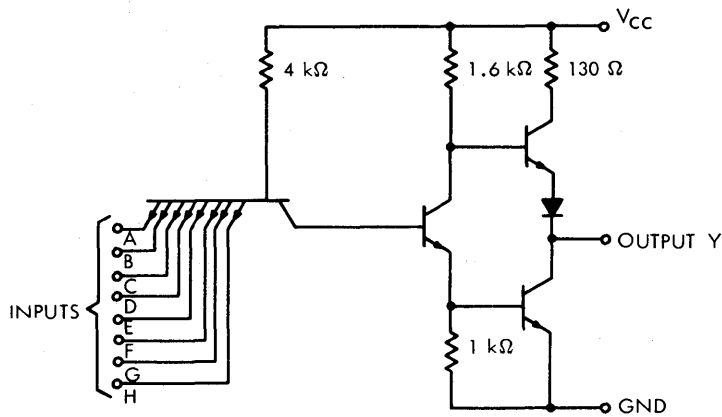
‡These typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .



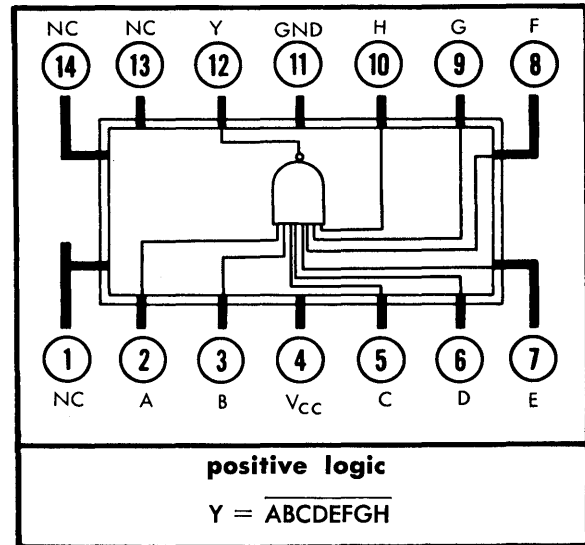
# TYPE SN7430

## 8-INPUT POSITIVE NAND GATE

### schematic



Component values shown are nominal.



### recommended operating conditions

Supply Voltage $V_{CC}$	.....	4.75 V to 5.25 V
Fan-Out From Output, N	.....	1 to 10

### electrical characteristics, $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	$V_{CC} = 4.75 \text{ V}$ , $V_{out(0)} \leq 0.4 \text{ V}$	2			V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	$V_{CC} = 4.75 \text{ V}$ , $V_{out(1)} \geq 2.4 \text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	2	$V_{CC} = 4.75 \text{ V}$ , $V_{in} = 0.8 \text{ V}$ , $I_{load} = -400 \mu\text{A}$	2.4	3.3‡		V
$V_{out(0)}$ Logical 0 output voltage	1	$V_{CC} = 4.75 \text{ V}$ , $V_{in} = 2 \text{ V}$ , $I_{sink} = 16 \text{ mA}$		0.22‡	0.4	V
$I_{in(0)}$ Logical 0 level input current (each input)	3	$V_{CC} = 5.25 \text{ V}$ , $V_{in} = 0.4 \text{ V}$			-1.6	mA
$I_{in(1)}$ Logical 1 level input current (each input)	4	$V_{CC} = 5.25 \text{ V}$ , $V_{in} = 2.4 \text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.25 \text{ V}$ , $V_{in} = 5.5 \text{ V}$			1	mA
$I_{OS}$ Short-circuit output current	5	$V_{CC} = 5.25 \text{ V}$	-18		-55	mA
$I_{CC(0)}$ Logical 0 level supply current	6	$V_{CC} = 5 \text{ V}$ , $V_{in} = 5 \text{ V}$		3‡		mA
$I_{CC(1)}$ Logical 1 level supply current	6	$V_{CC} = 5 \text{ V}$ , $V_{in} = 0$		1‡		mA

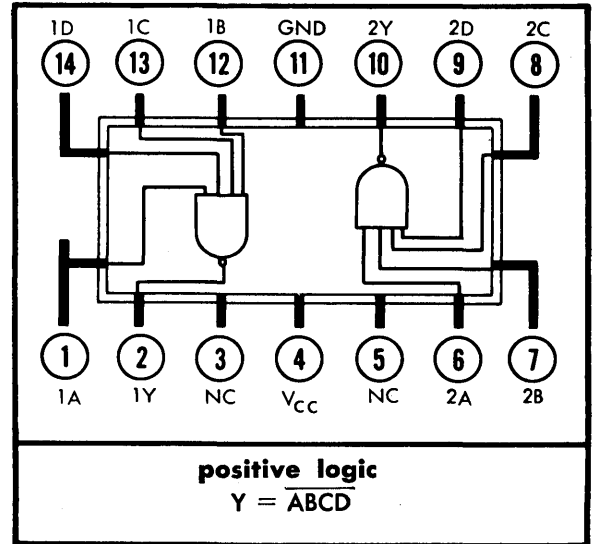
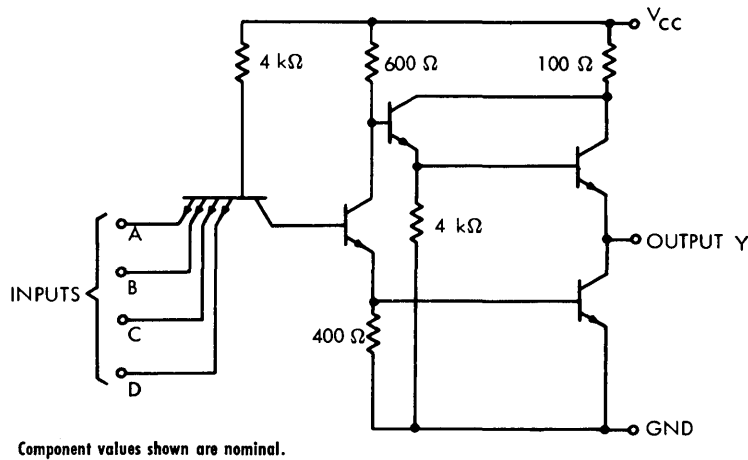
### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$ , $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$ Propagation delay time to logical 0 level	50	$C_1 = 15 \text{ pF}$		8	15	ns
$t_{pd1}$ Propagation delay time to logical 1 level	50	$C_1 = 15 \text{ pF}$		18	29	ns

‡These typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

# TYPE SN7440 DUAL 4-INPUT POSITIVE NAND BUFFER

## schematic (each gate)



## recommended operating conditions

Supply Voltage $V_{CC}$	4.75 V to 5.25 V
Fan-Out From Output, N	1 to 30

## electrical characteristics, $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	$V_{CC} = 4.75 \text{ V}$ , $V_{out(0)} \leq 0.4 \text{ V}$	2			V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	$V_{CC} = 4.75 \text{ V}$ , $V_{out(1)} \geq 2.4 \text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	2	$V_{CC} = 4.75 \text{ V}$ , $I_{load} = -1.2 \text{ mA}$ , $V_{in} = 0.8 \text{ V}$	2.4	3.3‡		V
$V_{out(0)}$ Logical 0 output voltage	1	$V_{CC} = 4.75 \text{ V}$ , $I_{sink} = 48 \text{ mA}$ , $V_{in} = 2 \text{ V}$		0.28‡	0.4	V
$I_{in(0)}$ Logical 0 level input current (each input)	3	$V_{CC} = 5.25 \text{ V}$ , $V_{in} = 0.4 \text{ V}$			-1.6	mA
$I_{in(1)}$ Logical 1 level input current (each input)	4	$V_{CC} = 5.25 \text{ V}$ , $V_{in} = 2.4 \text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.25 \text{ V}$ , $V_{in} = 5.5 \text{ V}$			1	mA
$I_{OS}$ Short-circuit output current†	5	$V_{CC} = 5.25 \text{ V}$	-18		-70	mA
$I_{CC(0)}$ Logical 0 level supply current (each gate)	6	$V_{CC} = 5 \text{ V}$ , $V_{in} = 5 \text{ V}$		8.6‡		mA
$I_{CC(1)}$ Logical 1 level supply current (each gate)	6	$V_{CC} = 5 \text{ V}$ , $V_{in} = 0$		2 ‡		mA

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$ , $N = 30$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$ Propagation delay time to logical 0 level	50	$C_1 = 15 \text{ pF}$		8	15	ns
$t_{pd1}$ Propagation delay time to logical 1 level	50	$C_1 = 15 \text{ pF}$		18	29	ns

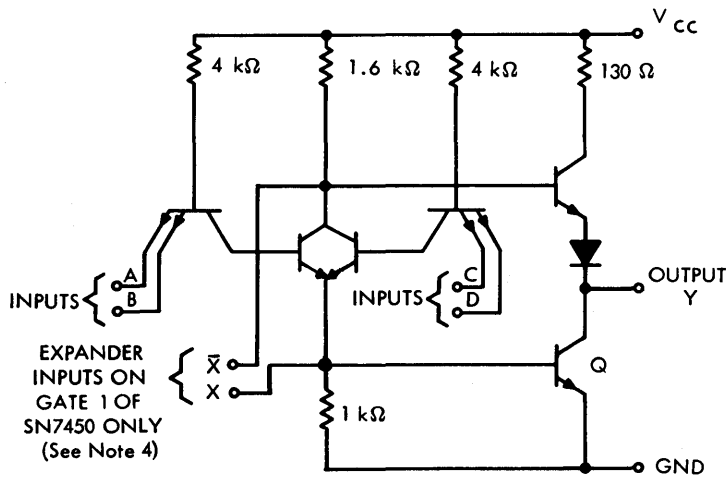
†Not more than one output should be shorted at a time.

‡These typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

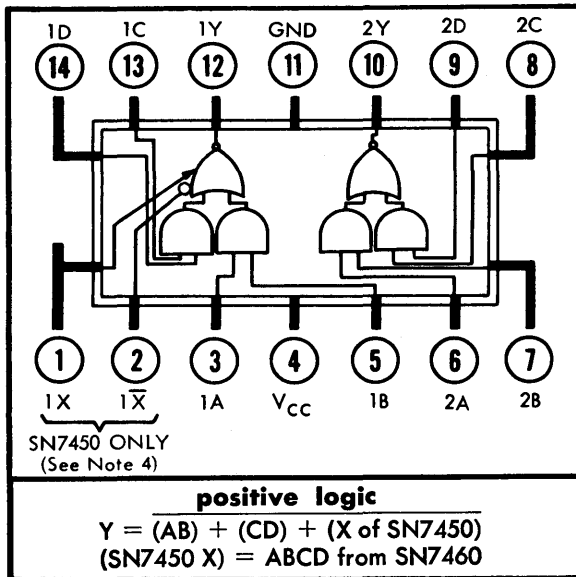
# TYPES SN7450, SN7451

## DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

schematic (each gate)



- NOTES: 1. Component values shown are nominal.  
 2. Both SN7450 expander inputs are used simultaneously for expanding with the SN7460.  
 3. If expander is not used leave pins ① and ② open.  
 4. Make no external connection to pins ① and ② of the SN7451.  
 5. A total of four expander gates may be connected to the SN7450 expander.



### recommended operating conditions

Supply Voltage V <sub>CC</sub> . . . . .	4.75 V to 5.25 V
Fan-Out From Each Output, N . . . . .	1 to 10

### electrical characteristics, T<sub>A</sub> = 0°C to 70°C, pins ① and ② open

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>in(1)</sub> Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	7	V <sub>CC</sub> = 4.75 V, V <sub>out(0)</sub> ≤ 0.4 V	2			V
V <sub>in(0)</sub> Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	8	V <sub>CC</sub> = 4.75 V, V <sub>out(1)</sub> ≥ 2.4 V			0.8	V
V <sub>out(1)</sub> Logical 1 output voltage	8	V <sub>CC</sub> = 4.75 V, V <sub>in</sub> = 0.8 V, I <sub>load</sub> = -400 μA	2.4	3.3‡		V
V <sub>out(0)</sub> Logical 0 output voltage	7	V <sub>CC</sub> = 4.75 V, V <sub>in</sub> = 2 V, I <sub>sink</sub> = 16 mA		0.22‡	0.4	V
I <sub>in(0)</sub> Logical 0 level input current (each input)	9	V <sub>CC</sub> = 5.25 V, V <sub>in</sub> = 0			-1.6	mA
I <sub>in(1)</sub> Logical 1 level input current (each input)	10	V <sub>CC</sub> = 5.25 V, V <sub>in</sub> = 2.4 V			40	μA
		V <sub>CC</sub> = 5.25 V, V <sub>in</sub> = 5.5 V			1	mA
I <sub>OS</sub> Short-circuit output current†	11	V <sub>CC</sub> = 5.25 V	-18		-55	mA
I <sub>CC(0)</sub> Logical 0 level supply current (each gate)	12	V <sub>CC</sub> = 5 V, V <sub>in</sub> = 5 V		3.7‡		mA
I <sub>CC(1)</sub> Logical 1 level supply current (each gate)	13	V <sub>CC</sub> = 5 V, V <sub>in</sub> = 0		2‡		mA

†Not more than one output should be shorted at a time.  
 ‡These typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

# TYPES SN7450, SN7451

## DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

**electrical characteristics (SN7450 only) using expander inputs,  $T_A = 0^\circ\text{C}$**

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_X$	Expander current	14	$V_{CC} = 4.75\text{ V}$ , $V_1 = 0.4\text{ V}$ , $I_{\text{sink}} = 16\text{ mA}$			3.1	mA
$V_{\text{BE}(Q)}$	Base-emitter voltage of output transistor (Q)	15	$V_{CC} = 4.75\text{ V}$ , $I_{\text{sink}} = 16\text{ mA}$ , $I_1 = 0.62\text{ mA}$ , $R_1 = 0$			1	V
$V_{\text{out}(1)}$	Logical 1 output voltage	16	$V_{CC} = 4.75\text{ V}$ , $I_{\text{load}} = -400\ \mu\text{A}$ , $I_1 = 0.15\text{ mA}$ , $I_2 = -0.15\text{ mA}$	2.4	3.3‡		V
$V_{\text{out}(0)}$	Logical 0 output voltage	15	$V_{CC} = 4.75\text{ V}$ , $I_{\text{sink}} = 16\text{ mA}$ , $I_1 = 0.43\text{ mA}$ , $R_1 = 130\ \Omega$		0.22‡	0.4	V

‡These typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

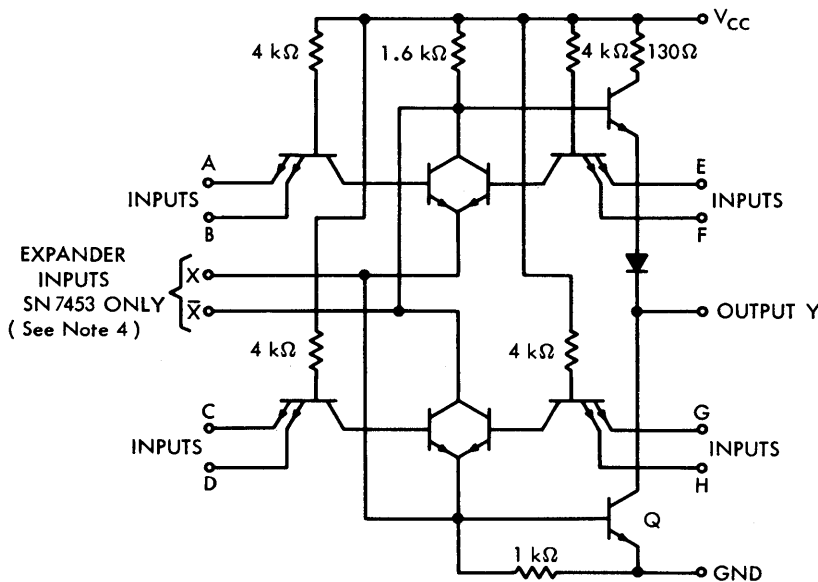
**switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , pins ① and ② open,  $N = 10$**

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\text{pd}0}$	Propagation delay time to logical 0 level	50	$C_1 = 15\text{ pF}$		8	15	ns
$t_{\text{pd}1}$	Propagation delay time to logical 1 level	50	$C_1 = 15\text{ pF}$		18	29	ns

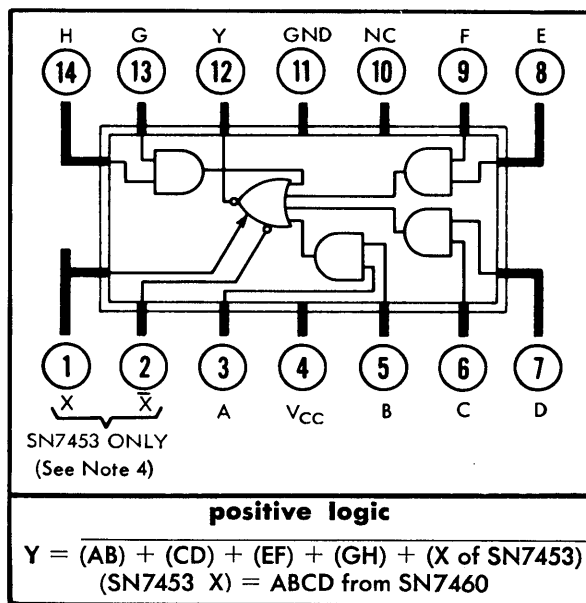
# TYPES SN7453, SN7454

## 4-WIDE 2-INPUT AND-OR-INVERT GATES

### schematic



- NOTES:
- Component values shown are nominal.
  - Both SN7453 expander inputs are used simultaneously for expanding with the SN7460.
  - If SN7453 expander is not used leave pins ① and ② open.
  - Make no external connection to pins ① and ② of the SN7454.
  - A total of four expander gates may be connected to the SN7453 expander inputs.



### recommended operating conditions

Supply Voltage  $V_{CC}$  . . . . . 4.75 V to 5.25 V  
 Fan-Out From Each Output, N . . . . . 1 to 10

### electrical characteristics, $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ , pins ① and ② open

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	7	$V_{CC} = 4.75 \text{ V}$ , $V_{out(0)} \leq 0.4 \text{ V}$	2			V
$V_{in(0)}$ Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	8	$V_{CC} = 4.75 \text{ V}$ , $V_{out(1)} \geq 2.4 \text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	8	$V_{CC} = 4.75 \text{ V}$ , $V_{in} = 0.8 \text{ V}$ , $I_{load} = -400 \mu\text{A}$	2.4	3.3‡		V
$V_{out(0)}$ Logical 0 output voltage	7	$V_{CC} = 4.75 \text{ V}$ , $V_{in} = 2 \text{ V}$ , $I_{sink} = 16 \text{ mA}$		0.22‡	0.4	V
$I_{in(0)}$ Logical 0 level input current (each input)	9	$V_{CC} = 5.25 \text{ V}$ , $V_{in} = 0$			-1.6	mA
$I_{in(1)}$ Logical 1 level input current (each input)	10	$V_{CC} = 5.25 \text{ V}$ , $V_{in} = 2.4 \text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.25 \text{ V}$ , $V_{in} = 5.5 \text{ V}$			1	mA
$I_{OS}$ Short-circuit output current†	11	$V_{CC} = 5.25 \text{ V}$	-18		-55	mA
$I_{CC(0)}$ Logical 0 level supply current	12	$V_{CC} = 5 \text{ V}$ , $V_{in} = 5 \text{ V}$		3.7 ‡		mA
$I_{CC(1)}$ Logical 1 level supply current	13	$V_{CC} = 5 \text{ V}$ , $V_{in} = 0$		2 ‡		mA

†Not more than one output should be shorted at a time.

‡These typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

# TYPES SN7453, SN7454

## 4-WIDE 2-INPUT AND-OR-INVERT GATES

electrical characteristics (SN7453 only) using expander inputs,  $T_A = 0^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_X$ Expander current	14	$V_{CC} = 4.75\text{ V}$ , $V_1 = 0.4\text{ V}$ , $I_{\text{sink}} = 16\text{ mA}$			3.1	mA
$V_{BE(Q)}$ Base-emitter voltage of output transistor (Q)	15	$V_{CC} = 4.75\text{ V}$ , $I_{\text{sink}} = 16\text{ mA}$ , $I_1 = 0.62\text{ mA}$ , $R_1 = 0$			1	V
$V_{\text{out}(1)}$ Logical 1 output voltage	16	$V_{CC} = 4.75\text{ V}$ , $I_{\text{load}} = -400\text{ }\mu\text{A}$ , $I_1 = 0.15\text{ mA}$ , $I_2 = -0.15\text{ mA}$	2.4	3.3‡		V
$V_{\text{out}(0)}$ Logical 0 output voltage	15	$V_{CC} = 4.75\text{ V}$ , $I_{\text{sink}} = 16\text{ mA}$ , $I_1 = 0.43\text{ mA}$ , $R_1 = 130\text{ }\Omega$		0.22‡	0.4	V

‡These typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

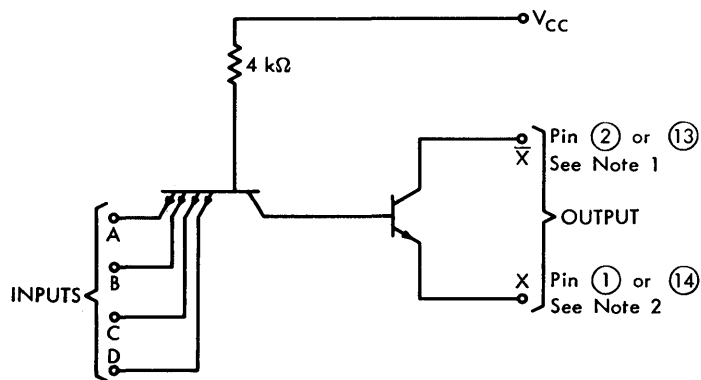
switching characteristics(SN7453 and SN7454),  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , pins ① and ② open,  $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$ Propagation delay time to logical 0 level	50	$C_1 = 15\text{ pF}$		8	15	ns
$t_{pd1}$ Propagation delay time to logical 1 level	50	$C_1 = 15\text{ pF}$		18	29	ns

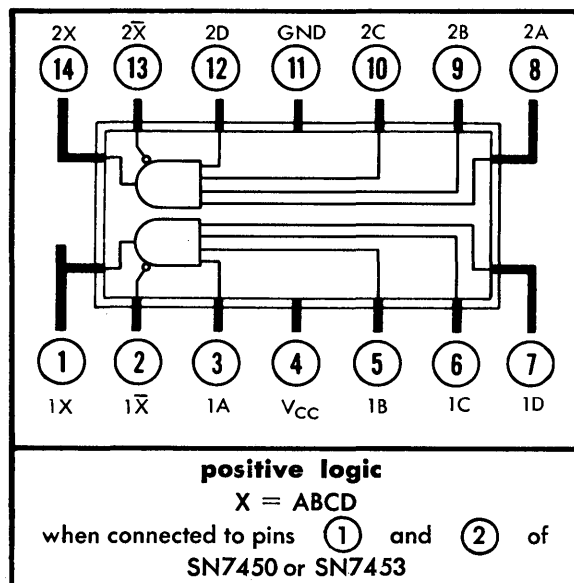
# TYPE SN7460

## DUAL 4-INPUT EXPANDER

### schematic



- NOTES: 1. Connect pin 2 or 13 to pin 2 of SN7450 or SN7453.  
 2. Connect pin 1 or 14 to pin 1 of SN7450 or SN7453.  
 3. Component values shown are nominal.



### recommended operating conditions

Supply Voltage  $V_{CC}$  . . . . . 4.75 V to 5.25 V  
 Maximum number of expanders that may be fanned-in to one SN7450 or one SN7453 . . . . . 4

### electrical characteristics (unless otherwise noted $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure output on level	17	$V_{CC} = 4.75\text{ V}$ , $V_1 = 1\text{ V}$ , $R = 1.1\text{ k}\Omega$ , $T_A = 0^\circ\text{C}$	2			V
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure output off level current	18	$V_{CC} = 4.75\text{ V}$ , $V_1 = 4.5\text{ V}$ , $R = 1.2\text{ k}\Omega$ , $I_{off} = 0.15\text{ mA}$ , $T_A = 0^\circ\text{C}$			0.8	V
$V_{on}$ Output voltage on level	17	$V_{CC} = 4.75\text{ V}$ , $V_{in} = 2\text{ V}$ , $V_1 = 1\text{ V}$ , $R = 1.1\text{ k}\Omega$ , $T_A = 0^\circ\text{C}$			0.4	V
$I_{off}$ Output off level current	18	$V_{CC} = 4.75\text{ V}$ , $V_{in} = 0.8\text{ V}$ , $V_1 = 4.5\text{ V}$ , $R = 1.2\text{ k}\Omega$ , $T_A = 0^\circ\text{C}$			270	$\mu\text{A}$
$I_{on}$ Output on level current	19	$V_{CC} = 4.75\text{ V}$ , $V_{in} = 2\text{ V}$ , $V_1 = 1\text{ V}$	-0.43			mA
$I_{in(0)}$ Logical 0 level input current (each input)	18	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 0.4\text{ V}$			-1.6	mA
$I_{in(1)}$ Logical 1 level input current (each input)	20	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 2.4\text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.25\text{ V}$ , $V_{in} = 5.5\text{ V}$			1	mA
$I_{CC(on)}$ On level supply current (each gate)	21	$V_{CC} = 5\text{ V}$ , $V_{in} = 5\text{ V}$ , $V_1 = 0.85\text{ V}$		0.6 ‡		mA
$I_{CC(off)}$ Off level supply current (each gate)	21	$V_{CC} = 5\text{ V}$ , $V_{in} = 0$ , $V_1 = 0.85\text{ V}$		1 ‡		mA

### switching characteristics, $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ , $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd0}$ Propagation delay time to logical 0 level (through SN7450 or SN7453)	51	$C_1 = 15\text{ pF}$		10	20	ns
$t_{pd1}$ Propagation delay time to logical 1 level (through SN7450 or SN7453)	51	$C_1 = 15\text{ pF}$		20	34	ns

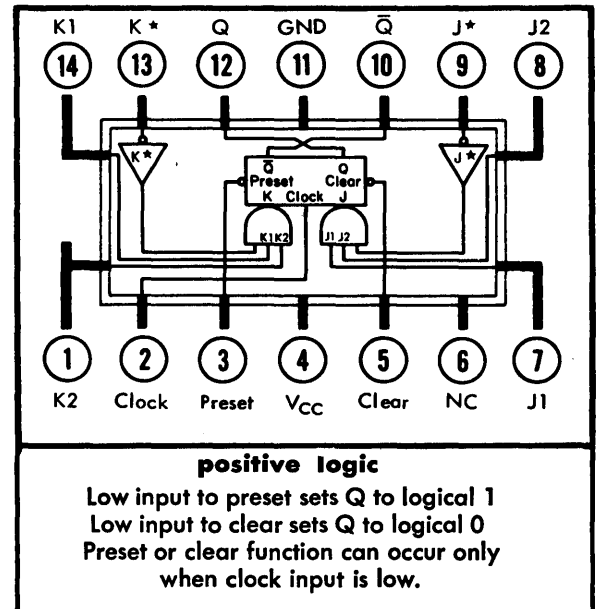
‡These typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

# TYPE SN7470 J-K FLIP-FLOP

## logic

TRUTH TABLE		
$t_n$		$t_{n+1}$
J	K	Q
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\overline{Q}_n$

- NOTES: 1.  $J = J1 \cdot J2 \cdot \overline{J\star}$ .  
 2.  $K = K1 \cdot K2 \cdot \overline{K\star}$ .  
 3.  $t_n$  = Bit time before clock pulse.  
 4.  $t_{n+1}$  = Bit time after clock pulse.  
 5. If inputs  $J\star$  or  $K\star$  are not used they must be grounded.



## description

The SN7470 is a monolithic, edge-triggered J-K flip-flop featuring gated inputs, direct clear and preset inputs, and complementary Q and  $\overline{Q}$  outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse; and after the clock input threshold voltage has been passed, the gated inputs are locked out.

The SN7470 flip-flop is ideally suited for medium-and-high-speed applications, and can be used for a significant saving in system power dissipation and package count where input gating is required.

## recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	4.75 V to 5.25 V
Fan-Out From Each Output, N . . . . .	1 to 10
Clock Pulse Transition Time to Logical 1 Level, $t_{f(\text{clock})}$ (See Figure 53) . . . . .	5 to 150 ns
Width of Clock Pulse, $t_{p(\text{clock})}$ (See Figure 53) . . . . .	$\geq 20$ ns
Width of Preset Pulse, $t_{p(\text{preset})}$ (See Figure 52) . . . . .	$\geq 25$ ns
Width of Clear Pulse, $t_{p(\text{clear})}$ (See Figure 52) . . . . .	$\geq 25$ ns



# TYPE SN7470

## J-K FLIP-FLOP

### electrical characteristics, $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal	22	$V_{CC} = 4.75\text{ V}$	2			V
$V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal	23	$V_{CC} = 4.75\text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	22	$V_{CC} = 4.75\text{ V}, I_{load} = -400\ \mu\text{A}$	2.4	3.5 $\ddagger$		V
$V_{out(0)}$ Logical 0 output voltage	23	$V_{CC} = 4.75\text{ V}, I_{sink} = 16\text{ mA}$		0.22 $\ddagger$	0.4	V
$I_{in(0)}$ Logical 0 level input current at J1, J2, J $\star$ , K1, K2, K $\star$ , or clock	24	$V_{CC} = 5.25\text{ V}, V_{in} = 0.4\text{ V}$			-1.6	mA
$I_{in(0)}$ Logical 0 level input current at preset or clear	24	$V_{CC} = 5.25\text{ V}, V_{in} = 0.4\text{ V}$			-3.2	mA
$I_{in(1)}$ Logical 1 level input current at J1, J2, J $\star$ , K1, K2, K $\star$ , or clock	25	$V_{CC} = 5.25\text{ V}, V_{in} = 2.4\text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.25\text{ V}, V_{in} = 5.5\text{ V}$			1	mA
$I_{in(1)}$ Logical 1 level input current at preset or clear	25	$V_{CC} = 5.25\text{ V}, V_{in} = 2.4\text{ V}$			80	$\mu\text{A}$
		$V_{CC} = 5.25\text{ V}, V_{in} = 5.5\text{ V}$			1	mA
$I_{OS}$ Short-circuit output current $\dagger$	26	$V_{CC} = 5.25\text{ V}, V_{in} = 0$	-18		-57	mA
$I_{CC}$ Supply current	25	$V_{CC} = 5\text{ V}, V_{in} = 5\text{ V}$		13 $\ddagger$		mA

$\dagger$ Not more than one output should be shorted at a time.

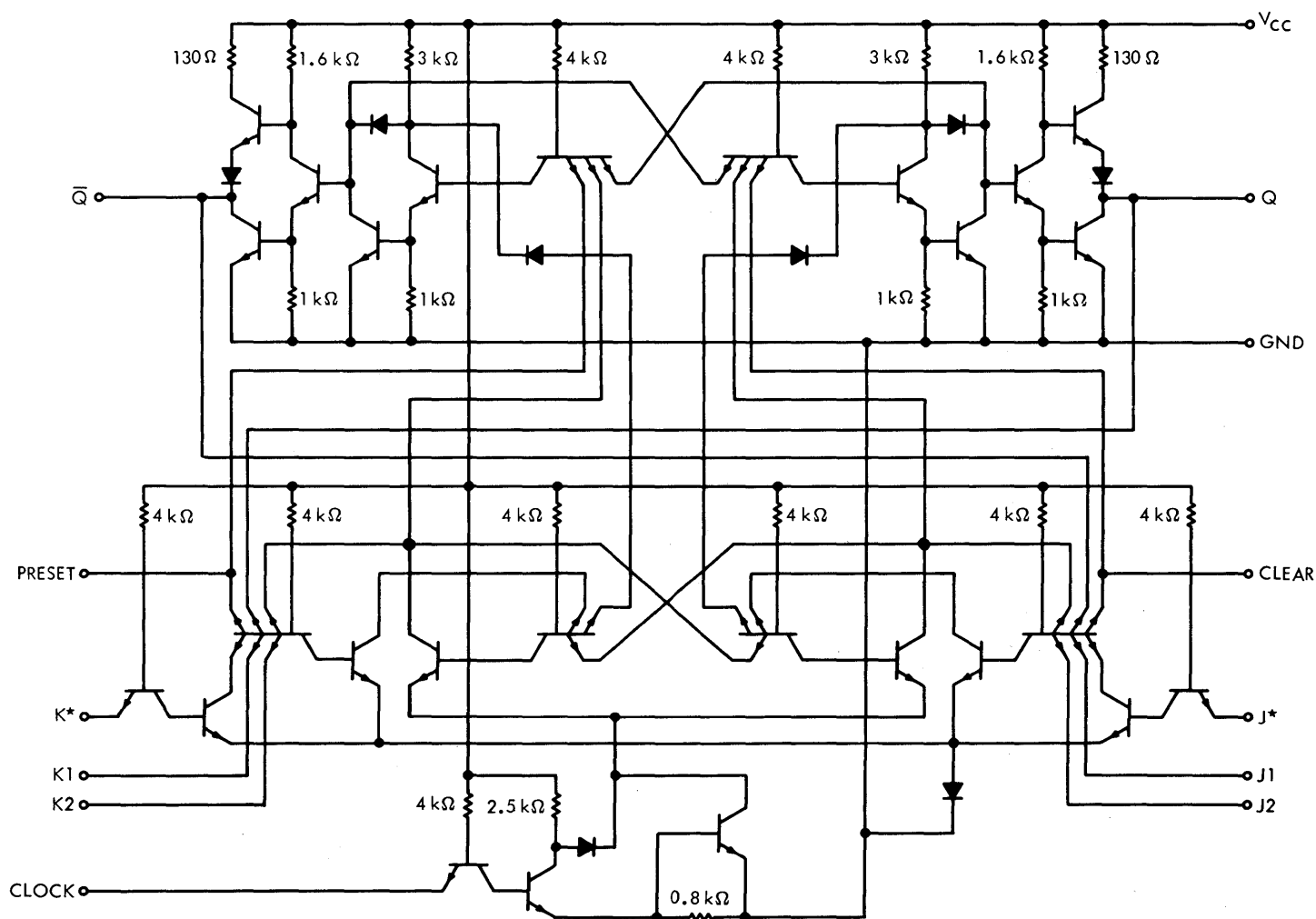
$\ddagger$ These typical values are at  $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$ .

### switching characteristics, $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}, N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{clock}$ Maximum clock frequency	53	$C_1 = 15\text{ pF}$	20	35		MHz
$t_{setup}$ Minimum input setup time	53	$C_1 = 15\text{ pF}$		10	20	ns
$t_{hold}$ Minimum input hold time	53	$C_1 = 15\text{ pF}$		0	5	ns
$t_{pd1}$ Propagation delay time to logical 1 level from clear or preset to output	52	$C_1 = 15\text{ pF}$			50	ns
$t_{pd0}$ Propagation delay time to logical 0 level from clear or preset to output	52	$C_1 = 15\text{ pF}$			50	ns
$t_{pd1}$ Propagation delay time to logical 1 level from clock to output	53	$C_1 = 15\text{ pF}$	10	27	50	ns
$t_{pd0}$ Propagation delay time to logical 0 level from clock to output	53	$C_1 = 15\text{ pF}$	10	18	50	ns

# TYPE SN7470 J-K FLIP-FLOP

## schematic



Component values shown are nominal.

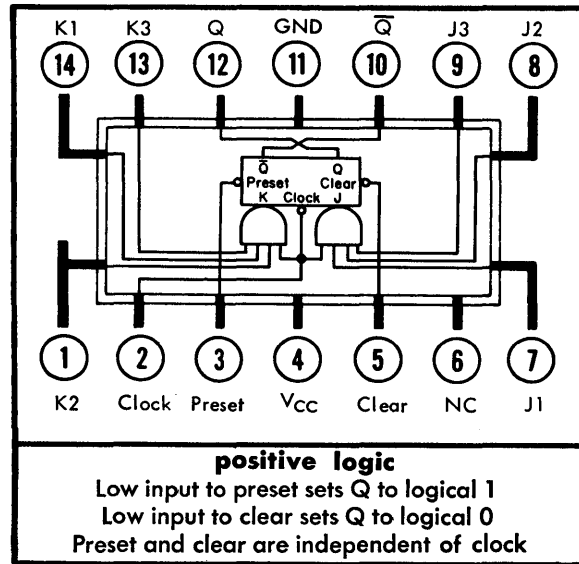
# TYPE SN7472

## J-K MASTER-SLAVE FLIP-FLOP

### logic

TRUTH TABLE		
$t_n$		$t_{n+1}$
J	K	Q
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\overline{Q}_n$

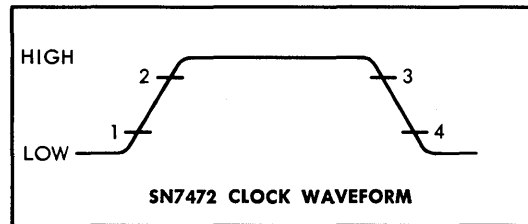
- NOTES: 1.  $J = J1 \cdot J2 \cdot J3$   
 2.  $K = K1 \cdot K2 \cdot K3$   
 3.  $t_n$  = Bit time before clock pulse.  
 4.  $t_{n+1}$  = Bit time after clock pulse.



### description

The SN7472 J-K flip-flop is based on the master-slave principle. This device has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.



### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	4.75 V to 5.25 V
Fan-Out From Each Output, N . . . . .	1 to 10
Width of Clock Pulse, $t_{p(\text{clock})}$ (See Figure 54) . . . . .	$\geq 20$ ns
Width of Preset Pulse, $t_{p(\text{preset})}$ (See Figure 55) . . . . .	$\geq 25$ ns
Width of Clear Pulse, $t_{p(\text{clear})}$ (See Figure 55) . . . . .	$\geq 25$ ns
Input Setup Time, $t_{\text{setup}}$ (See Figure 54) . . . . .	$\geq$ Applied Clock Pulse Width
Input Hold Time, $t_{\text{hold}}$ . . . . .	$\geq 0$

# TYPE SN7472

## J-K MASTER-SLAVE FLIP-FLOP

### electrical characteristics, $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal	27	$V_{CC} = 4.75\text{ V}$	2			V
$V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal	27	$V_{CC} = 4.75\text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	27	$V_{CC} = 4.75\text{ V}$ , $I_{load} = -400\ \mu\text{A}$	2.4	3.5‡		V
$V_{out(0)}$ Logical 0 output voltage	28	$V_{CC} = 4.75\text{ V}$ , $I_{sink} = 16\text{ mA}$	0.22‡		0.4	V
$I_{in(0)}$ Logical 0 level input current at J1, J2, J3, K1, K2, or K3	29	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 0.4\text{ V}$			-1.6	mA
$I_{in(0)}$ Logical 0 level input current at preset, clear, or clock	29	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 0.4\text{ V}$			-3.2	mA
$I_{in(1)}$ Logical 1 level input current at J1, J2, J3, K1, K2, or K3	30	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 2.4\text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.25\text{ V}$ , $V_{in} = 5.5\text{ V}$			1	mA
$I_{in(1)}$ Logical 1 level input current at preset, clear, or clock	30	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 2.4\text{ V}$			80	$\mu\text{A}$
		$V_{CC} = 5.25\text{ V}$ , $V_{in} = 5.5\text{ V}$			1	mA
$I_{OS}$ Short-circuit output current†	31	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 0$	-18		-57	mA
$I_{CC}$ Supply current	30	$V_{CC} = 5\text{ V}$ , $V_{in} = 5\text{ V}$			8‡	mA

†Not more than one output should be shorted at a time.

‡These typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

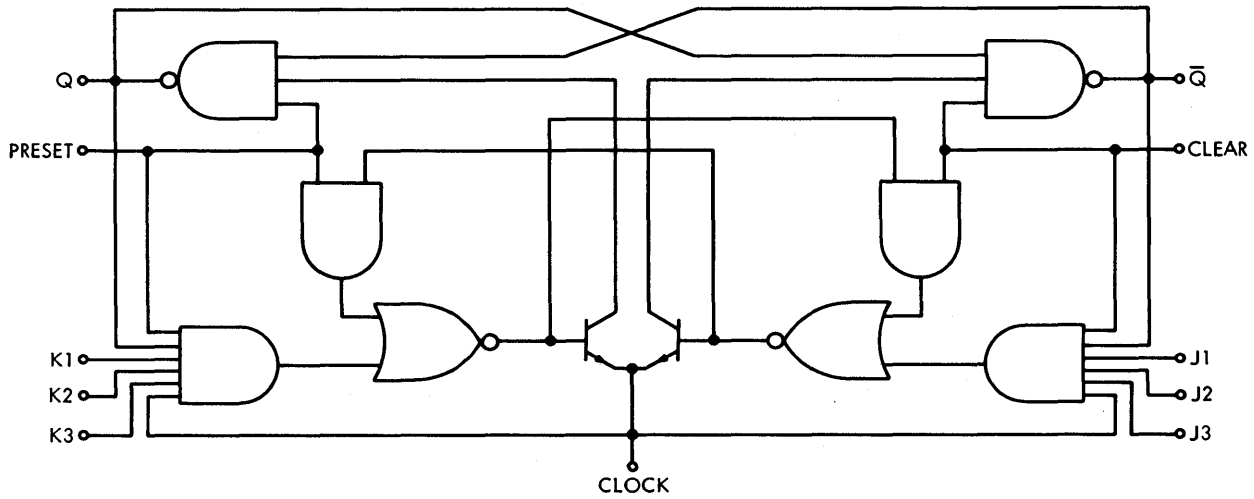
### switching characteristics, $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ , $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{clock}$ Maximum clock frequency	54	$C_1 = 15\text{ pF}$	10	15		MHz
$t_{pd1}$ Propagation delay time to logical 1 level from clear or preset to output	55	$C_1 = 15\text{ pF}$		26	50	ns
$t_{pd0}$ Propagation delay time to logical 0 level from clear or preset to output	55	$C_1 = 15\text{ pF}$		34	50	ns
$t_{pd1}$ Propagation delay time to logical 1 level from clock to output	54	$C_1 = 15\text{ pF}$	10	26	50	ns
$t_{pd0}$ Propagation delay time to logical 0 level from clock to output	54	$C_1 = 15\text{ pF}$	10	34	50	ns

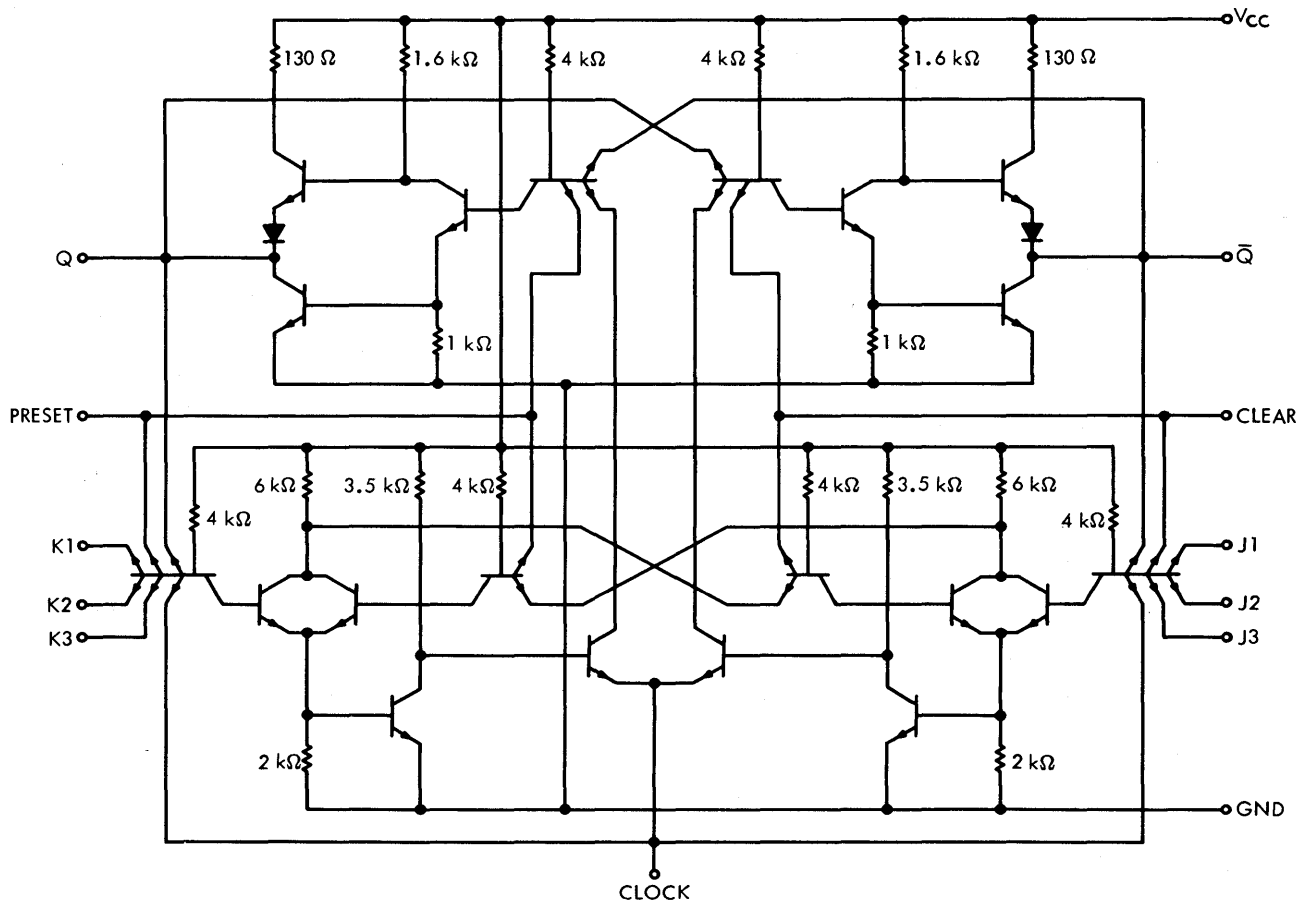
# TYPE SN7472

## J-K MASTER-SLAVE FLIP-FLOP

functional block diagram



schematic



Component values shown are nominal.

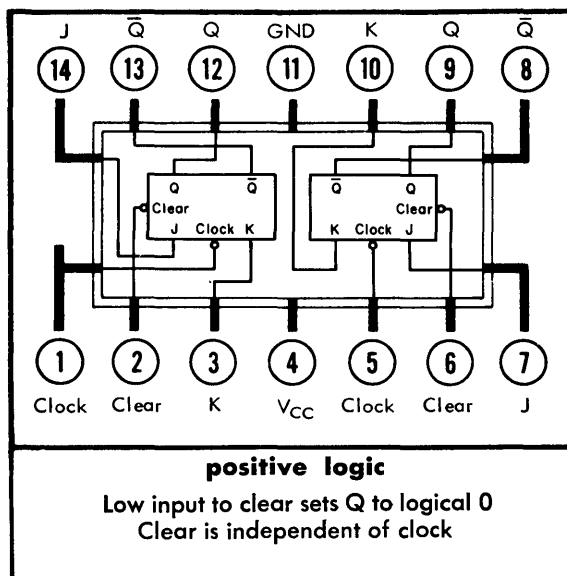
# TYPE SN7473

## DUAL J-K MASTER-SLAVE FLIP-FLOP

### logic

TRUTH TABLE (Each Flip-Flop)		
$t_n$		$t_{n+1}$
J	K	Q
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\bar{Q}_n$

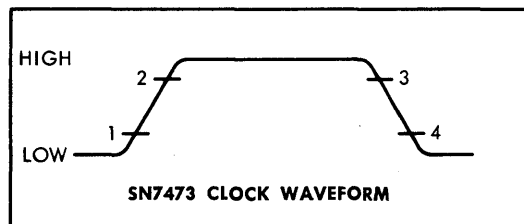
NOTES: 1.  $t_n$  = Bit time before clock pulse.  
 2.  $t_{n+1}$  = Bit time after clock pulse.



### description

The SN7473 J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.



### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	4.75 V to 5.25 V
Fan-Out From Each Output, N . . . . .	1 to 10
Width of Clock Pulse, $t_{p(\text{clock})}$ (See Figure 54) . . . . .	$\geq 20$ ns
Width of Clear Pulse, $t_{p(\text{clear})}$ (See Figure 55) . . . . .	$\geq 25$ ns
Input Setup Time, $t_{\text{setup}}$ (See Figure 54) . . . . .	$\geq$ Applied Clock Pulse Width
Input Hold Time, $t_{\text{hold}}$ . . . . .	$\geq 0$

# TYPE SN7473

## DUAL J-K MASTER-SLAVE FLIP-FLOP

### electrical characteristics, $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal	32	$V_{CC} = 4.75\text{ V}$	2			V
$V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal	32	$V_{CC} = 4.75\text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	32	$V_{CC} = 4.75\text{ V}$ , $I_{load} = -400\ \mu\text{A}$	2.4	3.5 ‡		V
$V_{out(0)}$ Logical 0 output voltage	33	$V_{CC} = 4.75\text{ V}$ , $I_{sink} = 16\text{ mA}$		0.22 ‡	0.4	V
$I_{in(0)}$ Logical 0 level input current at J or K	34	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 0.4\text{ V}$			-1.6	mA
$I_{in(0)}$ Logical 0 level input current at clear or clock	34	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 0.4\text{ V}$			-3.2	mA
$I_{in(1)}$ Logical 1 level input current at J or K	35	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 2.4\text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.25\text{ V}$ , $V_{in} = 5.5\text{ V}$			1	mA
$I_{in(1)}$ Logical 1 level input current at clear or clock	35	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 2.4\text{ V}$			80	$\mu\text{A}$
		$V_{CC} = 5.25\text{ V}$ , $V_{in} = 5.5\text{ V}$			1	mA
$I_{OS}$ Short-circuit output current†	36	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 0$	-18		-57	mA
$I_{CC}$ Supply current (each flip-flop)	35	$V_{CC} = 5\text{ V}$ , $V_{in} = 5\text{ V}$		8 ‡		mA

†Not more than one output should be shorted at a time.

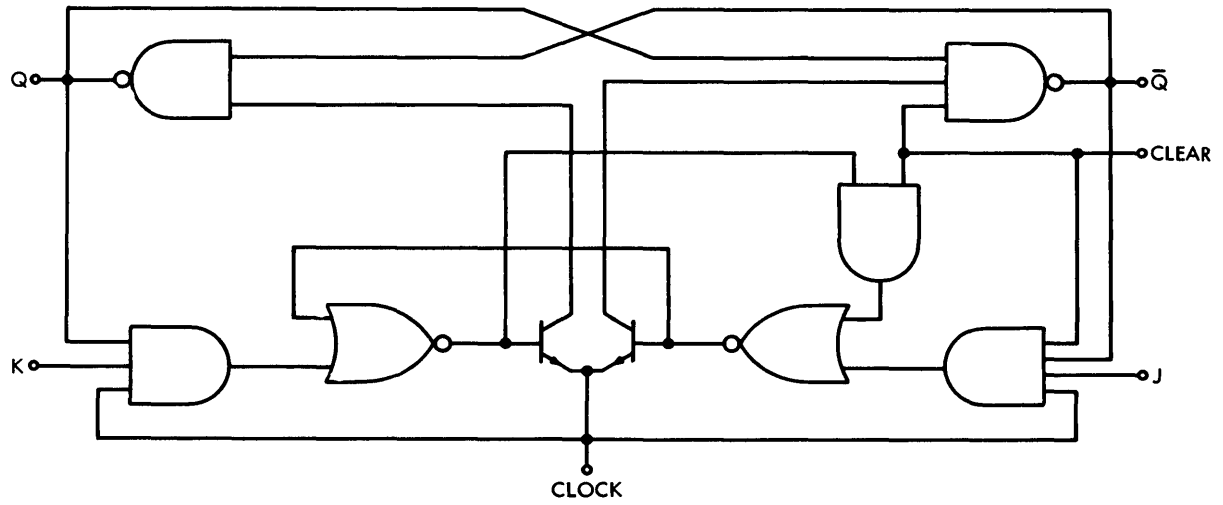
‡These typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

### switching characteristics, $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ , $N = 10$

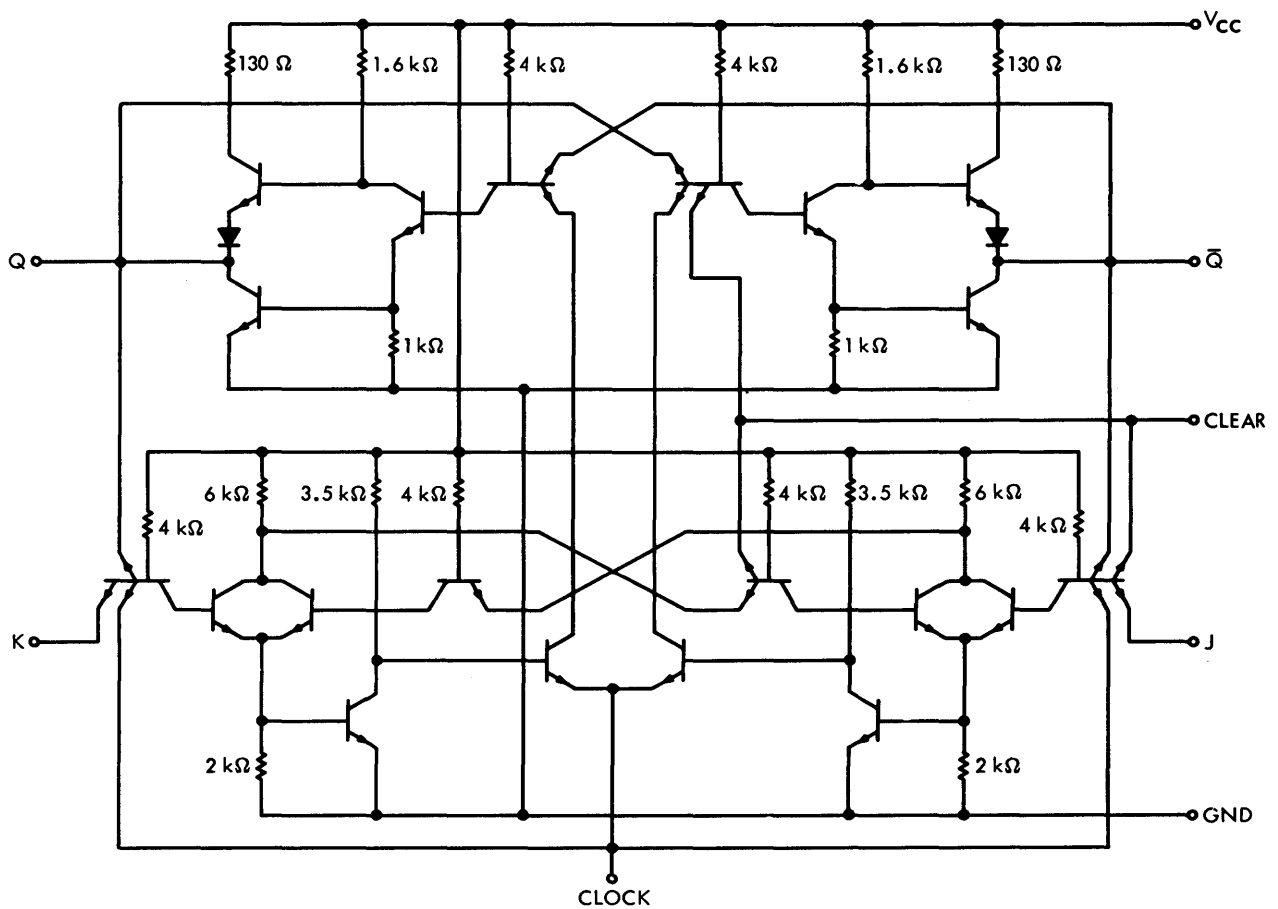
PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{clock}$ Maximum clock frequency	54	$C_1 = 15\text{ pF}$	10	15		MHz
$t_{pd1}$ Propagation delay time to logical 1 level from clear to output	55	$C_1 = 15\text{ pF}$		26	50	ns
$t_{pd0}$ Propagation delay time to logical 0 level from clear to output	55	$C_1 = 15\text{ pF}$		34	50	ns
$t_{pd1}$ Propagation delay time to logical 1 level from clock to output	54	$C_1 = 15\text{ pF}$	10	26	50	ns
$t_{pd0}$ Propagation delay time to logical 0 level from clock to output	54	$C_1 = 15\text{ pF}$	10	34	50	ns

# TYPE SN7473 DUAL J-K MASTER-SLAVE FLIP-FLOP

**functional block diagram (each flip-flop)**



**schematic (each flip-flop)**



Component values shown are nominal.



# TYPE SN7474

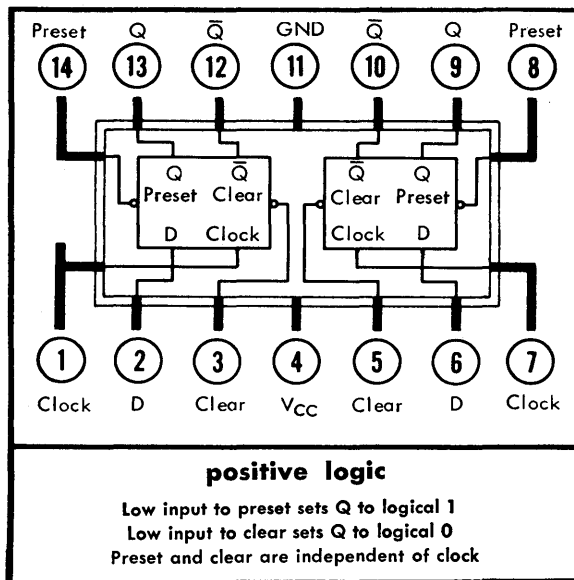
## DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP

### logic

TRUTH TABLE (Each Flip-Flop)

$t_n$	$t_{n+1}$	
INPUT D	OUTPUT Q	OUTPUT $\bar{Q}$
0	0	1
1	1	0

- NOTES: 1.  $t_n$  = bit time before clock pulse.  
 2.  $t_{n+1}$  = bit time after clock pulse.



### description

The SN7474 is a monolithic, dual, D-type, edge-triggered flip-flop featuring direct clear and preset inputs and complementary Q and  $\bar{Q}$  outputs. Input information is transferred to the Q output on the positive edge of the clock pulse.

Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed the data input (D) is locked out.

The SN7474 dual flip-flop has the same clocking characteristics as the SN7470 gated (edge-triggered) flip-flop and both are ideally suited for medium- and high-speed applications. The SN7474 can be used at a significant saving in system power dissipation and package count in applications where input gating is not required.

### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	4.75 V to 5.25 V
Fan-Out From Each Output, N . . . . .	1 to 10
Width of Clock Pulse, $t_{p(\text{clock})}$ (See Figure 56) . . . . .	$\geq 30$ ns
Width of Preset Pulse, $t_{p(\text{preset})}$ (See Figure 53) . . . . .	$\geq 30$ ns
Width of Clear Pulse, $t_{p(\text{clear})}$ (See Figure 53) . . . . .	$\geq 30$ ns

# TYPE SN7474

## DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP

electrical characteristics,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal	37	$V_{CC} = 4.75\text{ V}$	2			V
$V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal	37	$V_{CC} = 4.75\text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	37	$V_{CC} = 4.75\text{ V}$ , $I_{load} = -400\ \mu\text{A}$	2.4	3.5 ‡		V
$V_{out(0)}$ Logical 0 output voltage	38	$V_{CC} = 4.75\text{ V}$ , $I_{sink} = 16\text{ mA}$	0.22 ‡	0.4		V
$I_{in(0)}$ Logical 0 level input current at preset or D	39	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 0.4\text{ V}$			-1.6	mA
$I_{in(0)}$ Logical 0 level input current at clear or clock	39	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 0.4\text{ V}$			-3.2	mA
$I_{in(1)}$ Logical 1 level input current at D	40	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 4.5\text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.25\text{ V}$ , $V_{in} = 5.5\text{ V}$			1	mA
$I_{in(1)}$ Logical 1 level input current at preset or clock	40	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 2.4\text{ V}$			80	$\mu\text{A}$
		$V_{CC} = 5.25\text{ V}$ , $V_{in} = 5.5\text{ V}$			1	mA
$I_{in(1)}$ Logical 1 level input current at clear	40	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 2.4\text{ V}$			120	$\mu\text{A}$
		$V_{CC} = 5.25\text{ V}$ , $V_{in} = 5.5\text{ V}$			1	mA
$I_{OS}$ Short-circuit output current †	41	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 0$	-18		-57	mA
$I_{CC}$ Supply current (each flip-flop)	40	$V_{CC} = 5\text{ V}$ , $V_{in} = 5\text{ V}$		8.5 ‡		mA

†Not more than one output should be shorted at a time.

‡These typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

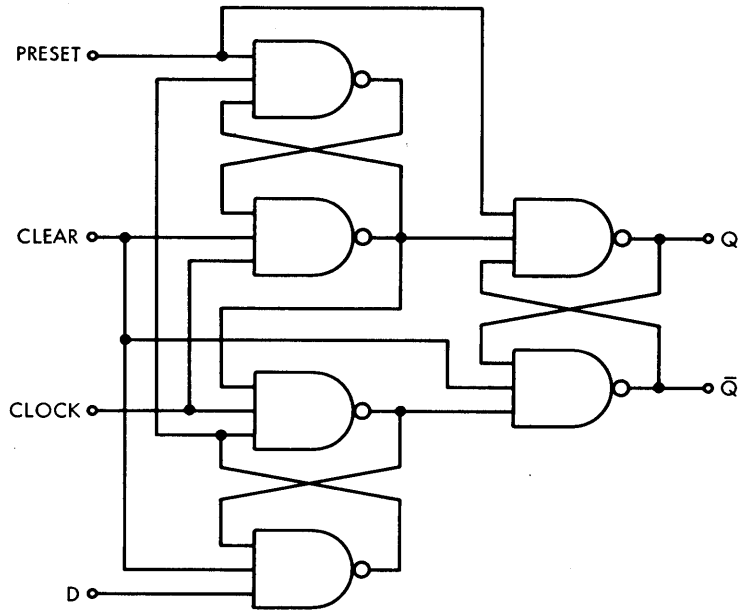
switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{clock}$ Maximum clock frequency	56	$C_1 = 15\text{ pF}$	15	25		MHz
$t_{setup}$ Minimum input setup time	56	$C_1 = 15\text{ pF}$		15	20	ns
$t_{hold}$ Minimum input hold time	56	$C_1 = 15\text{ pF}$		2	5	ns
$t_{pd1}$ Propagation delay time to logical 1 level from clear or preset to output	53	$C_1 = 15\text{ pF}$			25	ns
$t_{pd0}$ Propagation delay time to logical 0 level from clear or preset to output	53	$C_1 = 15\text{ pF}$			40	ns
$t_{pd1}$ Propagation delay time to logical 1 level from clock to output	56	$C_1 = 15\text{ pF}$	10	28	35	ns
$t_{pd0}$ Propagation delay time to logical 0 level from clock to output	56	$C_1 = 15\text{ pF}$	10	20	50	ns

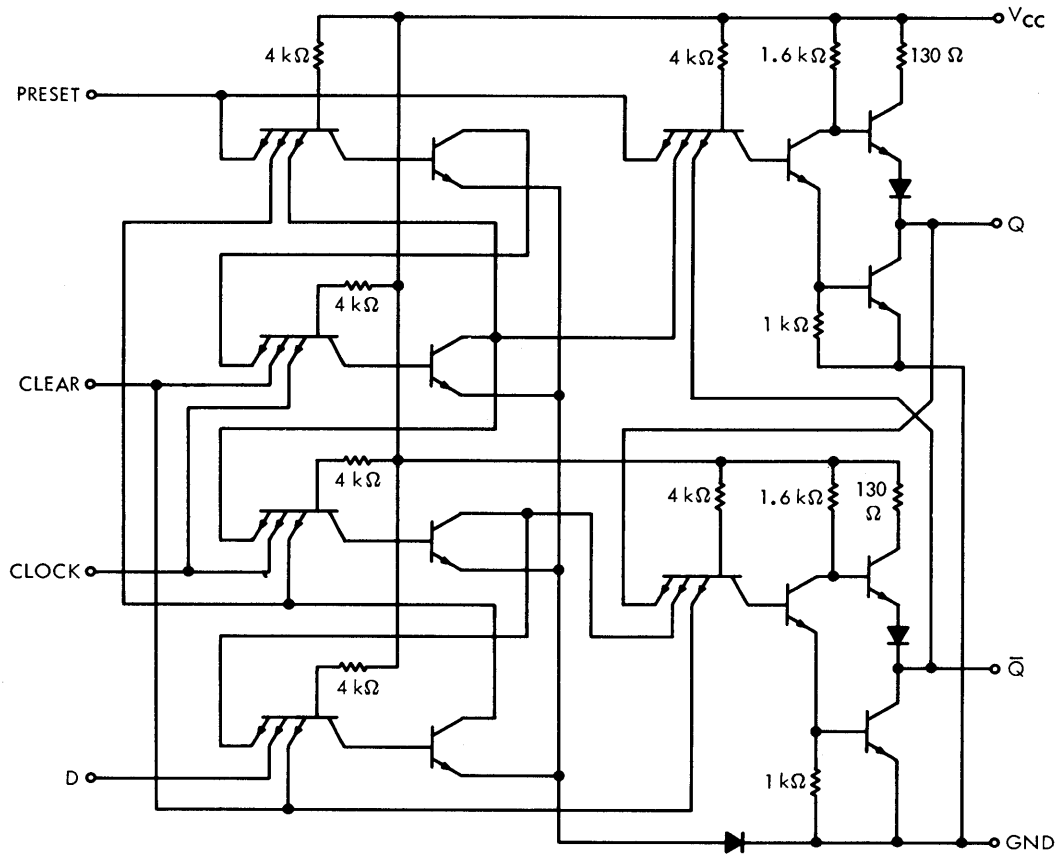
# TYPE SN7474

## DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP

functional block diagram (each flip-flop)



schematic (each flip-flop)



Component values shown are nominal.

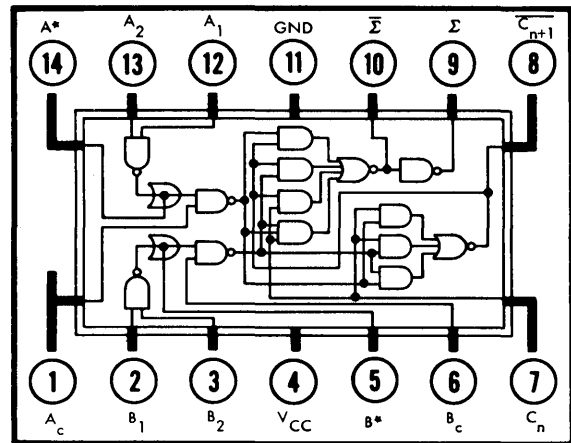
# TYPE SN7480 GATED FULL ADDER

## logic

TRUTH TABLE (See Notes 1, 2, and 3)

$C_n$	B	A	$\overline{C_{n+1}}$	$\overline{\Sigma}$	$\Sigma$
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

- NOTES: 1.  $A = A^* \cdot A_c$ ,  $B = B^* \cdot B_c$   
 where  $A^* = A_1 \cdot A_2$ ,  $B^* = B_1 \cdot B_2$   
 2. When  $A^*$  or  $B^*$  are used as inputs,  $A_1$  and  $A_2$  or  $B_1$  and  $B_2$  respectively must be connected to GND.  
 3. When  $A_1$  and  $A_2$  or  $B_1$  and  $B_2$  are used as inputs,  $A^*$  or  $B^*$  respectively must be open or used to perform Dot-OR logic.



## description

The SN7480 is a single-bit, high-speed, binary full adder with gated complementary inputs, complementary sum ( $\Sigma$  and  $\overline{\Sigma}$ ) outputs and inverted carry output. Designed for medium- and high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit (see schematic diagram) utilizes diode-transistor logic (DTL) for the gated inputs, and high-speed, high-fan-out transistor-transistor logic (TTL) for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform full-adder functions.

## recommended operating conditions

Supply Voltage $V_{CC}$	4.75 V to 5.25 V
Maximum Allowable Fan-Out From Outputs:	
$C_{n+1}$ , N	1 to 5
$\Sigma$ or $\overline{\Sigma}$ , N	1 to 10
$A^*$ or $B^*$ , N	1 to 3

# TYPE SN7480

## GATED FULL ADDER

electrical characteristics,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage	42 and 43	$V_{CC} = 4.75\text{ V}$ , $V_{in(0)} = 0.8\text{ V}$ , $V_{out(1)} \geq 2.4\text{ V}$ , $V_{out(0)} \leq 0.4\text{ V}$	2			V
$V_{in(0)}$	Logical 0 input voltage	42 and 43	$V_{CC} = 4.75\text{ V}$ , $V_{in(1)} = 2\text{ V}$ , $V_{out(1)} \geq 2.4\text{ V}$ , $V_{out(0)} \leq 0.4\text{ V}$			0.8	V
$V_{out(1)}$	Logical 1 output voltage	43	$V_{CC} = 4.75\text{ V}$	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	42	$V_{CC} = 4.75\text{ V}$		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at $A_1$ , $A_2$ , $B_1$ , $B_2$ , $A_C$ or $B_C$	44	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 0.4\text{ V}$			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at $A^*$ or $B^*$	45	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 0.4\text{ V}$			-2.6	mA
$I_{in(0)}$	Logical 0 level input current at $C_n$	45	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 0.4\text{ V}$			-8	mA
$I_{in(1)}$	Logical 1 level input current at $A_1$ , $A_2$ , $B_1$ , $B_2$ , $A_C$ or $B_C$	46	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 2.4\text{ V}$			15	$\mu\text{A}$
			$V_{CC} = 5.25\text{ V}$ , $V_{in} = 5.5\text{ V}$			1	mA
$I_{in(1)}$	Logical 1 level input current at $C_n$	47	$V_{CC} = 5.25\text{ V}$ , $V_{in} = 2.4\text{ V}$			200	$\mu\text{A}$
			$V_{CC} = 5.25\text{ V}$ , $V_{in} = 5.5\text{ V}$			1	mA
$I_{OS}$	Short-circuit output current at $\Sigma$ or $\Sigma^*$ †	48	$V_{CC} = 5.25\text{ V}$	-18		-57	mA
$I_{OS}$	Short-circuit output current at $\overline{C_{n+1}}$ †	48	$V_{CC} = 5.25\text{ V}$	-18		-70	mA
$I_{CC}$	Supply current	49	$V_{CC} = 5\text{ V}$		21‡		mA

†Not more than one output should be shorted at a time.

‡These typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER ¶	FROM INPUT	TO OUTPUT	FIGURE 57 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd1}$	$C_n$	$\overline{C_{n+1}}$	1	$N = 5$		13	17	ns
$t_{pd0}$			2	$N = 5$		3	7	ns
$t_{pd1}$	$B_C$	$\overline{C_{n+1}}$	3	$N = 5$		18	25	ns
$t_{pd0}$			4	$N = 5$		38	55	ns
$t_{pd1}$	$A_C$	$\Sigma$	5	$N = 10$		52	70	ns
$t_{pd0}$			6	$N = 10$		62	80	ns
$t_{pd1}$	$B_C$	$\overline{M}$	7	$N = 10$		38	55	ns
$t_{pd0}$			8	$N = 10$		56	75	ns
$t_{pd1}$	$A_1$	$A^*$	9	$C_L = 15\text{ pF}$		48	65	ns
$t_{pd0}$			10	$C_L = 15\text{ pF}$		17	25	ns
$t_{pd1}$	$B_1$	$B^*$	11	$C_L = 15\text{ pF}$		48	65	ns
$t_{pd0}$			12	$C_L = 15\text{ pF}$		17	25	ns

¶ $t_{pd1}$  is propagation delay time to logical 1 level.  $t_{pd0}$  is propagation delay time to logical 0 level.

## TYPICAL APPLICATIONS

### n-bit binary adder or subtractor (see figures F and G)

The SN7480 is designed specifically for N-bit adder or subtractor operations without external gates or inverters. In both applications, the sum or difference functions are generated in parallel while the carry functions are obtained serially. When the number of stages is small, the add or subtract time determines the maximum system clock rate. However, as the number of bits increases, the time required for the carry function to ripple through each bit becomes the limiting factor. Normally the ripple time of adders built with standard integrated circuits is excessive, and the resulting system speed is so slow that other more complex methods are required to perform these functions.

In the SN7480, two methods are used to reduce the carry delay. The carry circuit employs a high-speed Darlington output, and the logic gating has only one inversion between the  $C_n$  input and the  $\overline{C_{n+1}}$  output. This logic configuration results in an inverted carry output, and consequently an inverted carry input to the succeeding stage. To counteract this inverted input without sacrificing propagation time through the carry, gates are provided within the circuit to invert the A and B inputs and the resulting sum or difference output. This

interconnection method is illustrated by bit 2 and bit 4 of the adder (figure F). The inverted carry output is a true carry from bit 2 and bit 4, enabling the use of noninverted A and B inputs for the odd-numbered bits.

When performing subtraction (figure G) the  $C_n$  input to bit 1 is connected to a logical 1 and input bits and input control functions for the subtrahend (memory or register B) are effectively inverted.

The input control is used to disable the A and B inputs when memory or register information is being shifted. A logical 0 applied to this line will bring each sum or difference output to a logical 0 condition and maintain this level regardless of the state of the input information into each bit. For the adder (figure F), input control is applied to  $A_2$  and  $B_2$  of odd-numbered bits and to  $A_c$  and  $B_c$  of even-numbered bits. For the subtractor (figure G), input control is applied to  $A_2$  and  $B_c$  of the odd-numbered bits and to  $A_c$  and  $B_2$  of the even-numbered bits. These alternating patterns are necessary to complement the varying input sequence which they control.

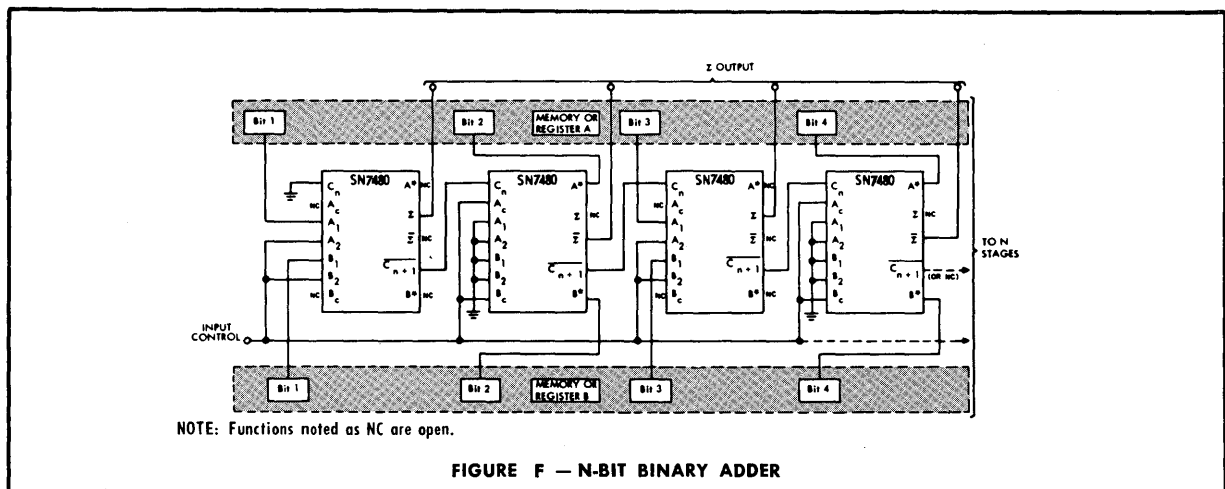


FIGURE F — N-BIT BINARY ADDER

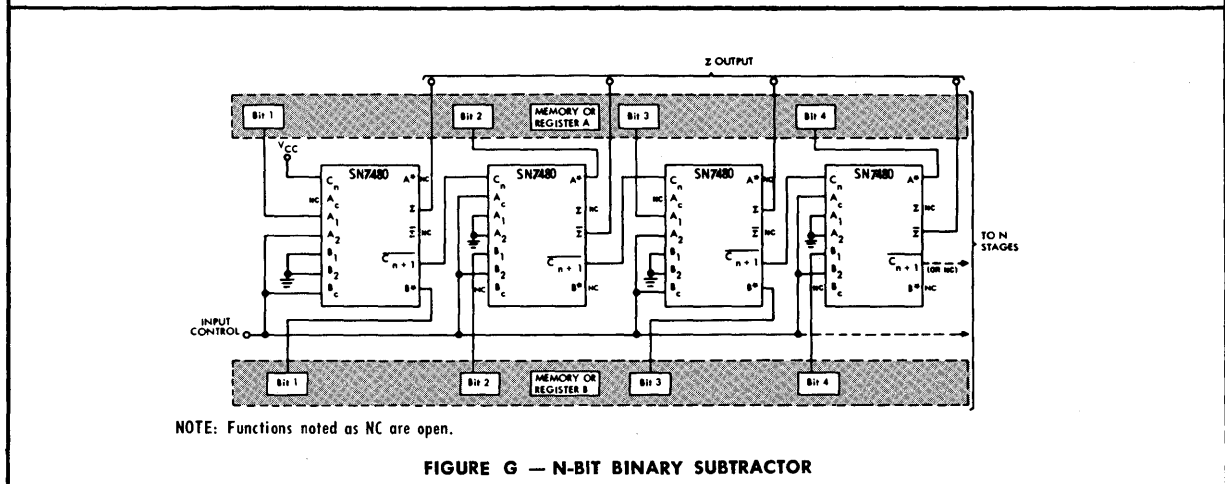


FIGURE G — N-BIT BINARY SUBTRACTOR

# TYPE SN7480

## GATED FULL ADDER

### TYPICAL APPLICATIONS

#### n-bit binary adder with register selection (see figure H)

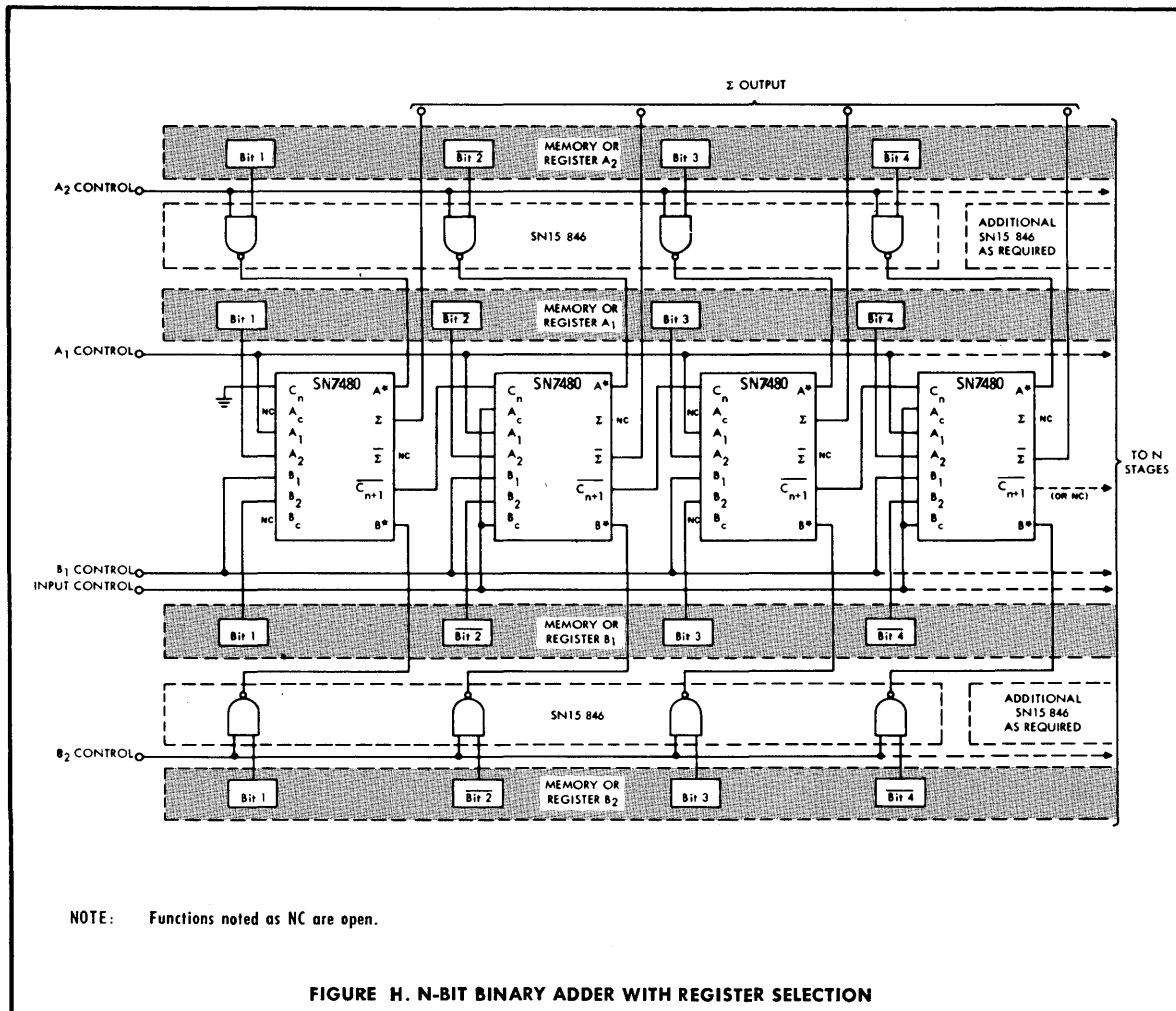
This application fully utilizes the flexibility of the input gating available within the SN7480. Two "A" registers and two "B" registers drive a single adder for each bit required. Register selection is performed internally for registers  $A_1$  and  $B_1$  and externally by a type SN15 846 DTL gate for registers  $A_2$  and  $B_2$ . Dot-OR logic is performed at the  $A^*$  and  $B^*$  nodes within the adder when the register selection is made.

Operation is as follows: To add the contents of Register  $A_1$  to Register  $B_1$ ,  $A_2$  and  $B_2$  control lines are brought to the logical 0 state. (If the input to these lines is from a logic gate, fan-out rules should be observed.) In similar fashion, the contents of register  $A_1$  are added to register  $B_2$  by holding  $A_2$  and  $B_1$  control lines at a logical 0. Four register combinations may be used. Even-numbered input bits from each register must be inverted since the  $A^*$  and  $B^*$  inputs are being used to perform Dot-OR logic. This is not a configuration restriction for flip-flop type registers and memories, but may require additional logic elements if other storage configurations are used as inputs.

The input control function is available as in the previous application and is implemented by bringing all four register control lines and the input control line to a logical 0 level. This condition ensures a logical 0 at each  $\Sigma$  output regardless of "A" and "B" register logic levels.

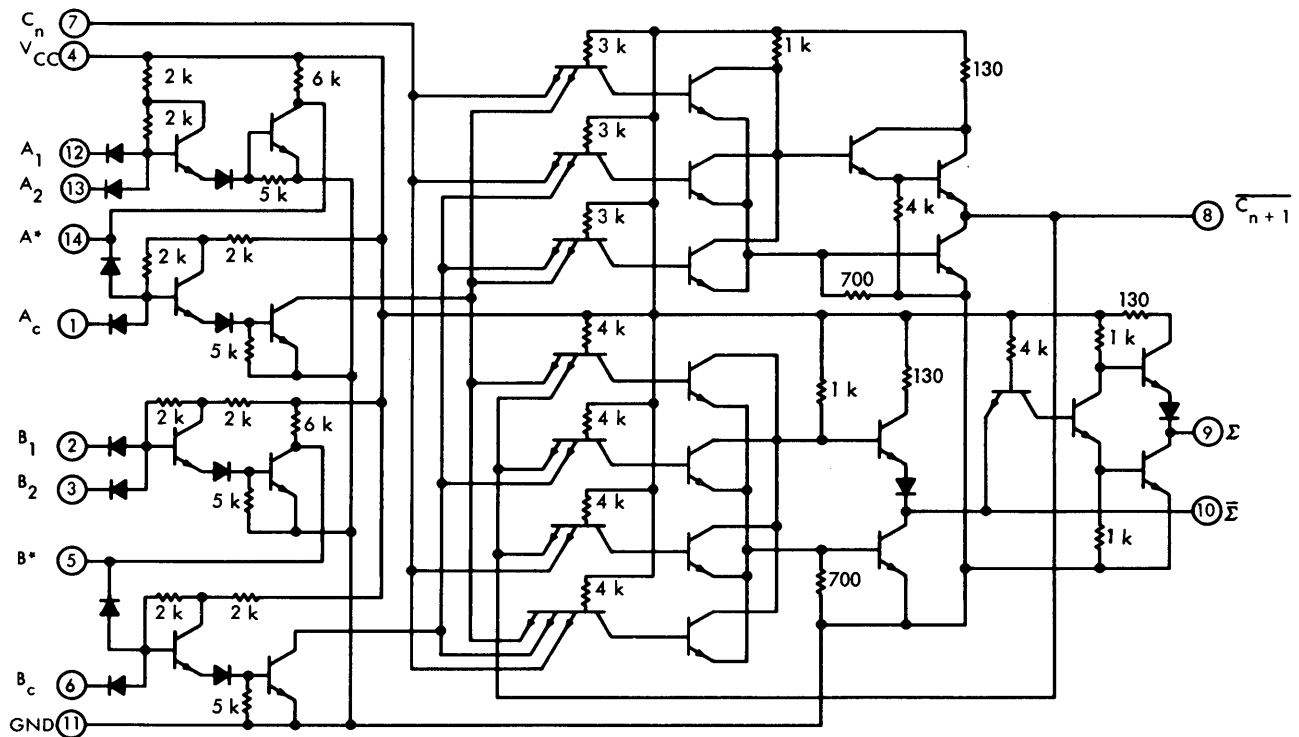
Up to four "A" registers and four "B" registers may be implemented in a fashion analogous to that shown in figure H. Inputs from the register-control gates (SN15 846) of the additional registers would be Dot-OR connected with  $A_2$  and  $B_2$  registers at the  $A^*$  and  $B^*$  inputs.

To perform N-bit subtraction, the  $C_n$  input at bit 1 is connected to a logical 1 and bit inputs from each register or memory used as a subtrahend must consist of the complement of bit inputs shown for the adder addend. Input control remains the same.



# TYPE SN7480 GATED FULL ADDER

schematic diagram

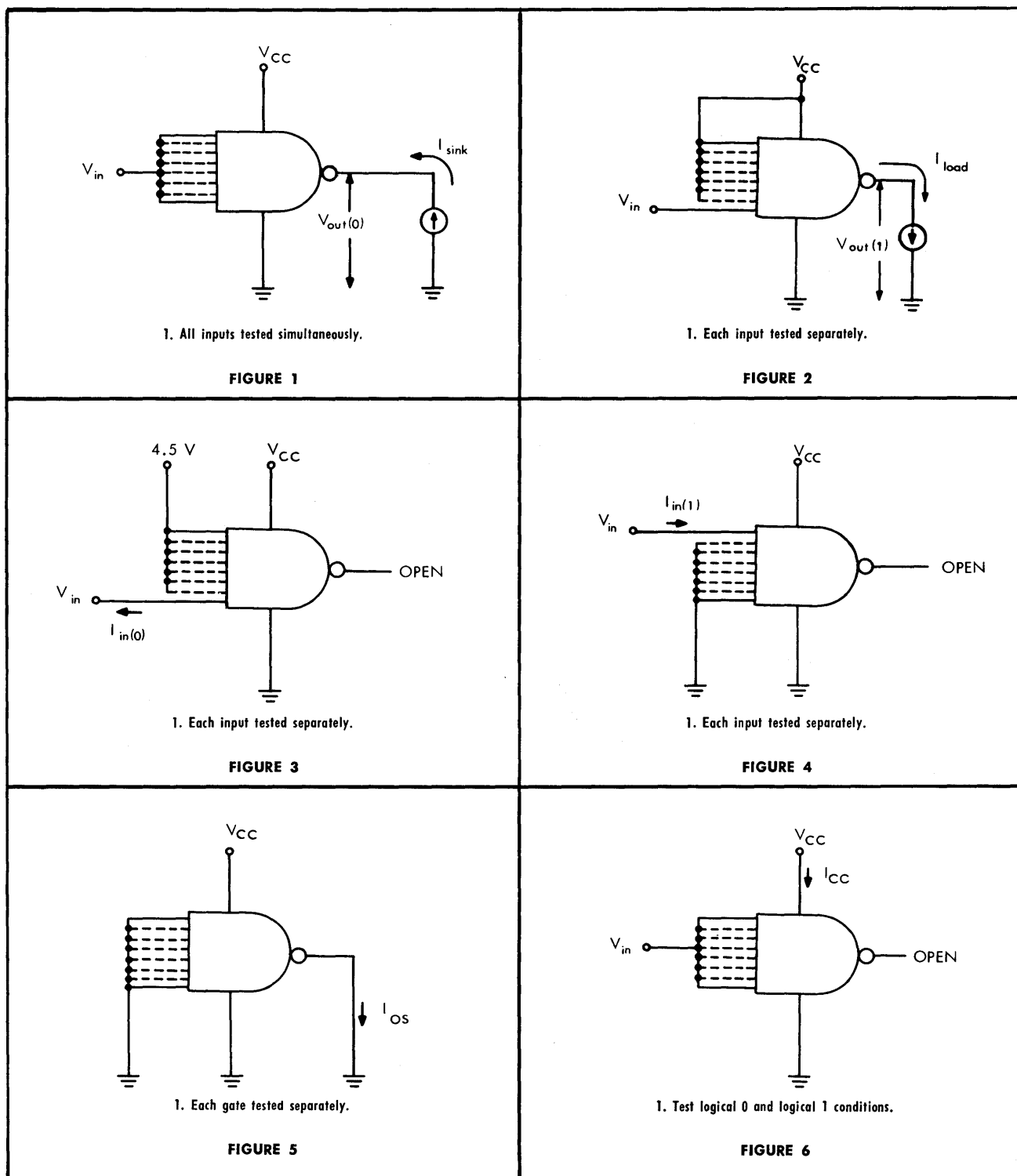


Component values shown are nominal.  
Resistor values are in ohms.



PARAMETER MEASUREMENT INFORMATION

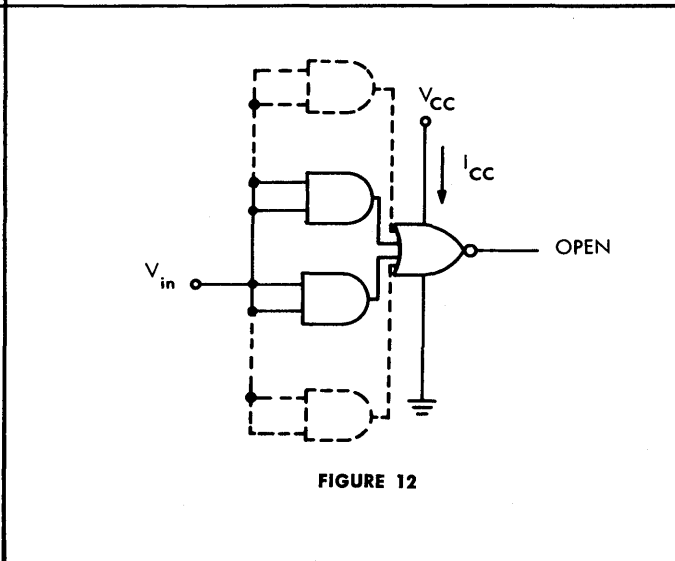
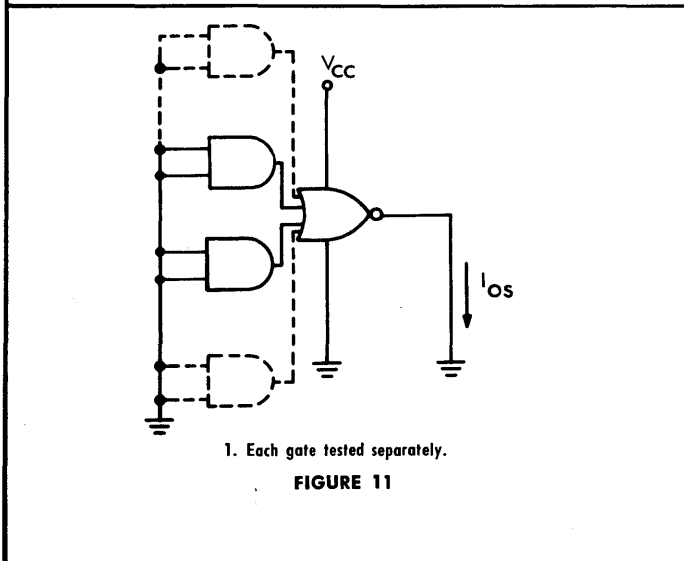
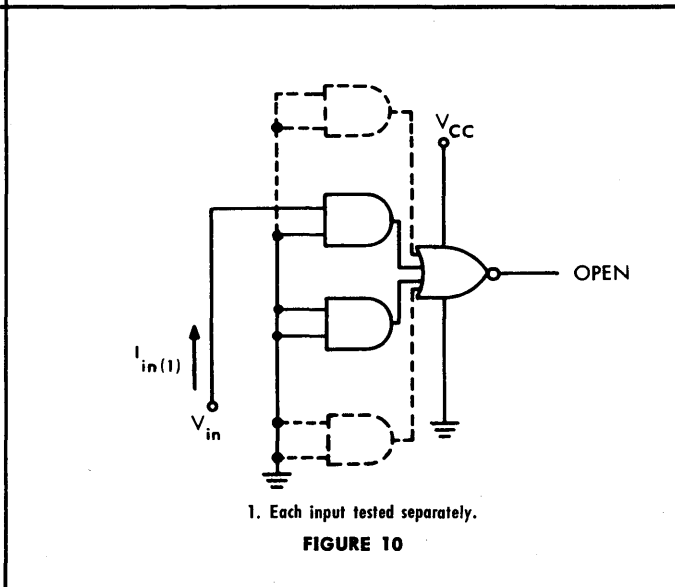
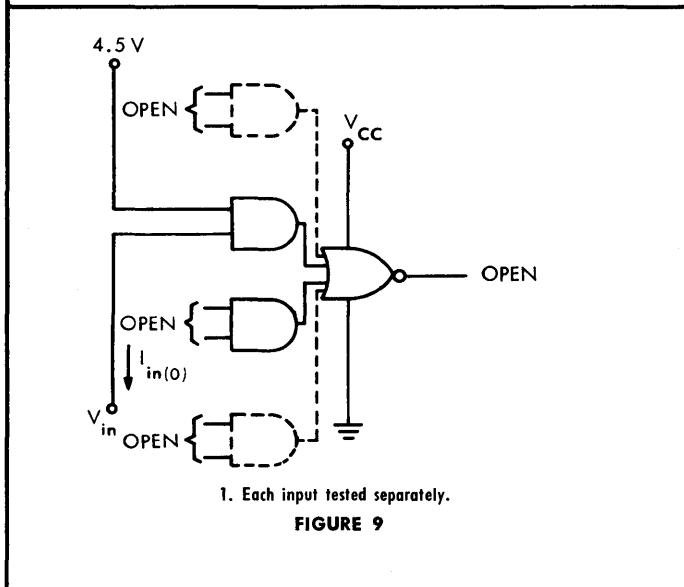
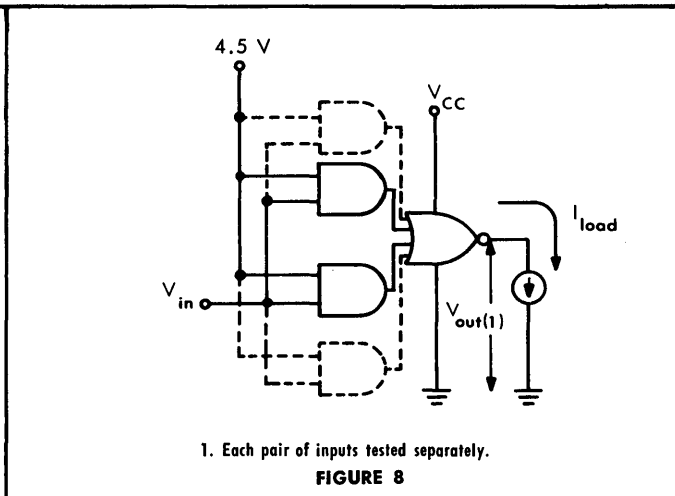
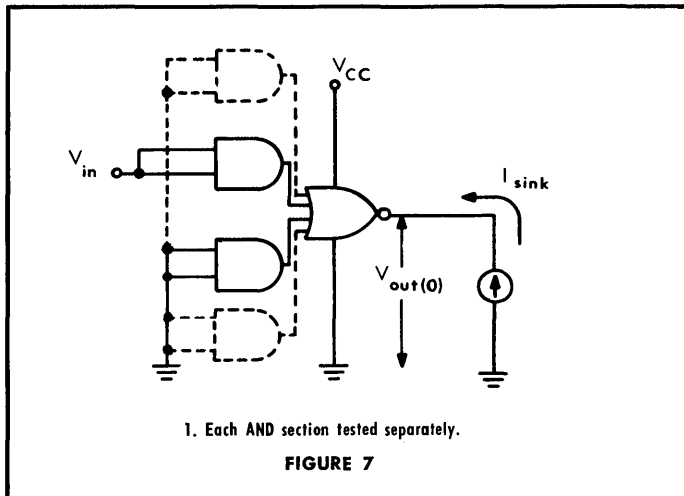
d-c test circuits§



§Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

**d-c test circuits § (continued)**



§ Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

d-c test circuits§ (continued)

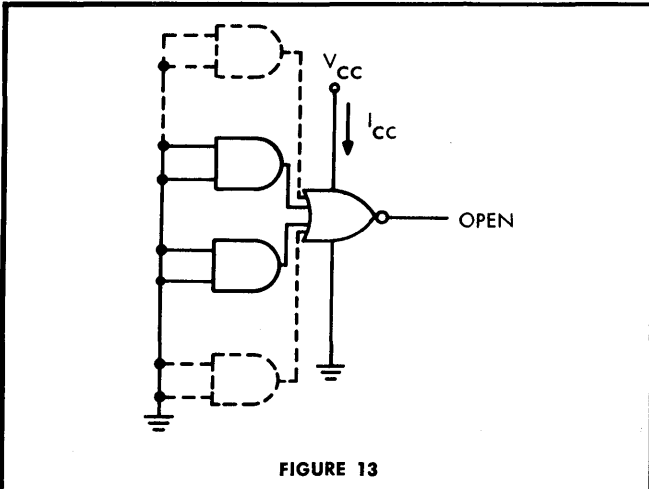


FIGURE 13

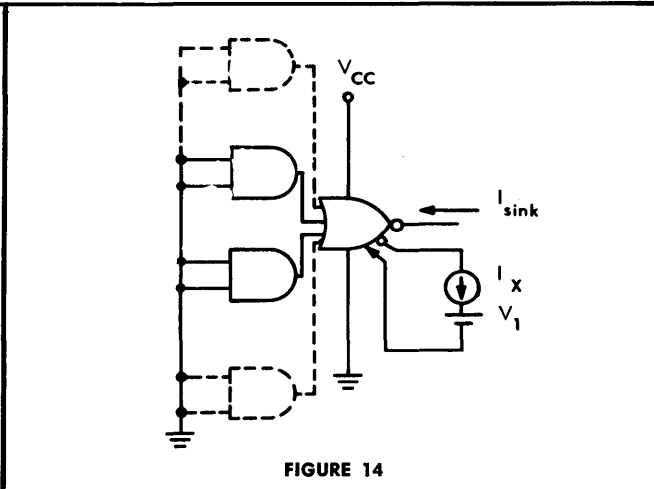


FIGURE 14

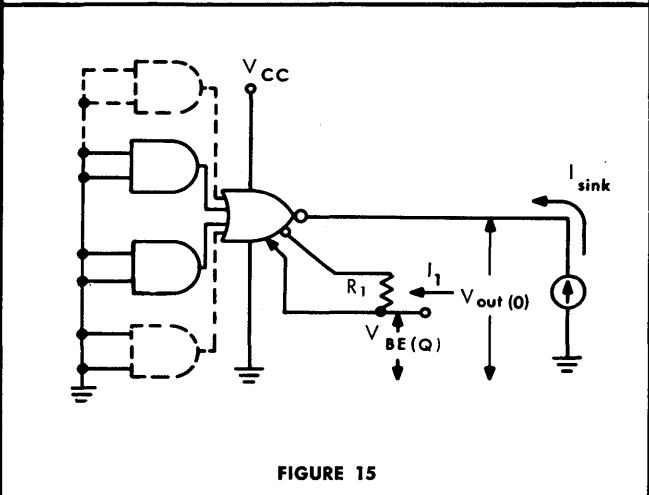


FIGURE 15

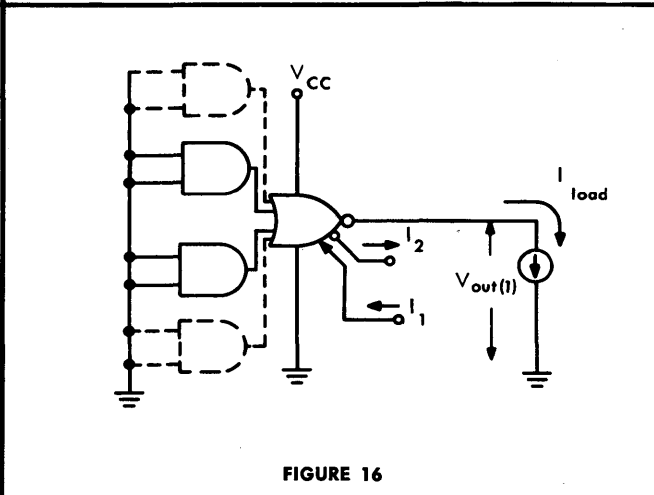


FIGURE 16

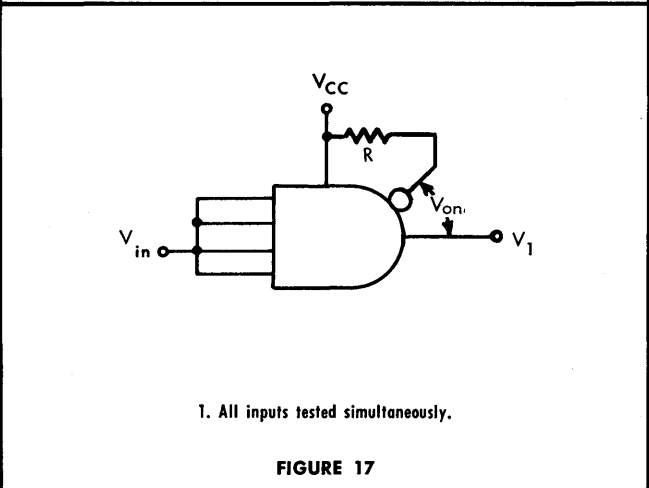


FIGURE 17

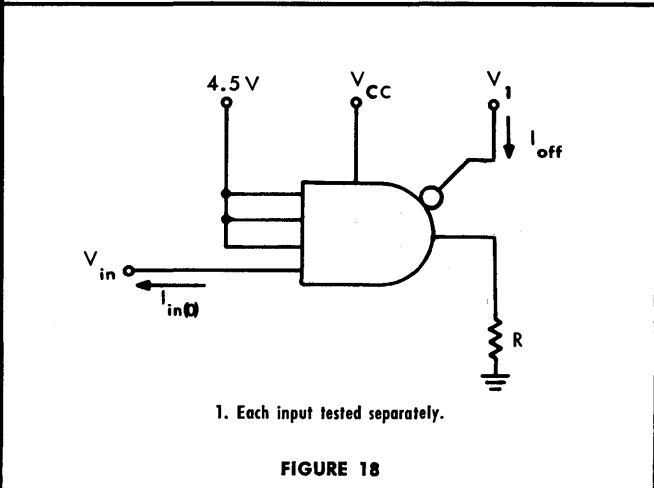
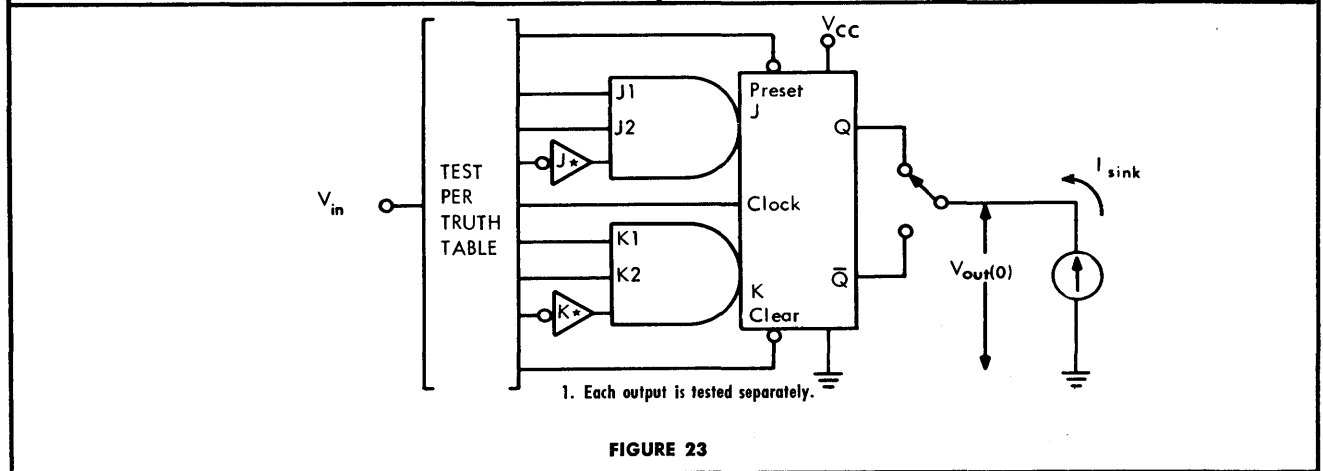
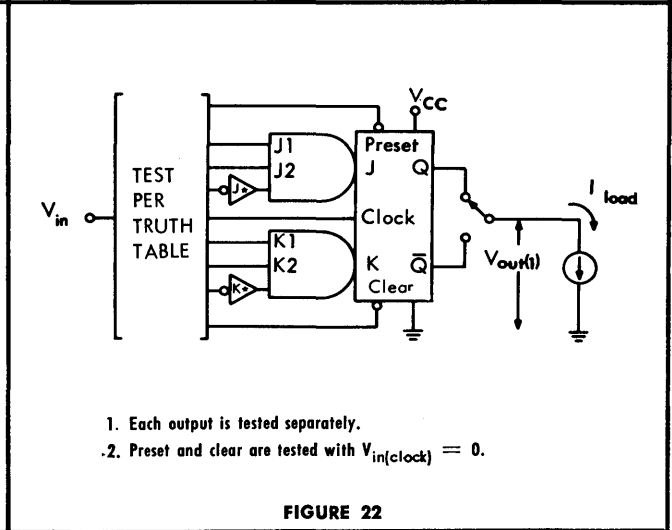
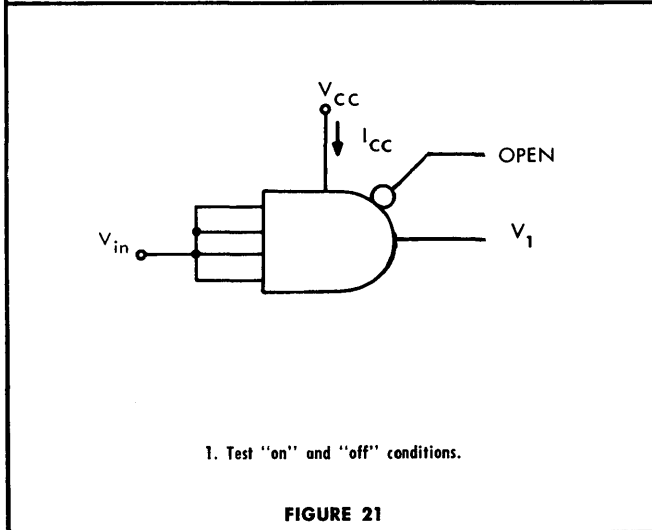
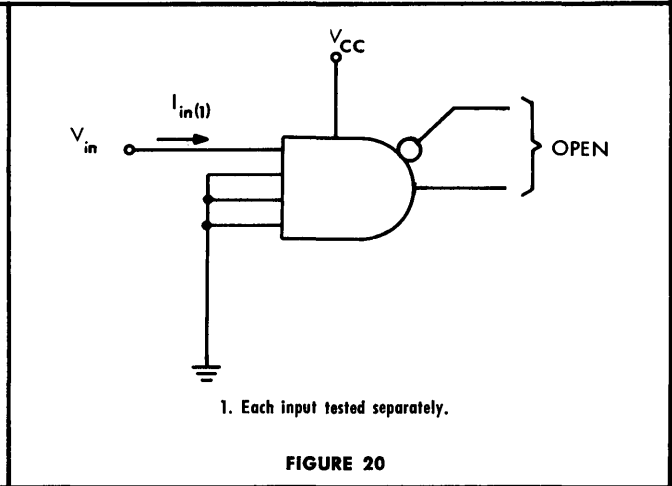
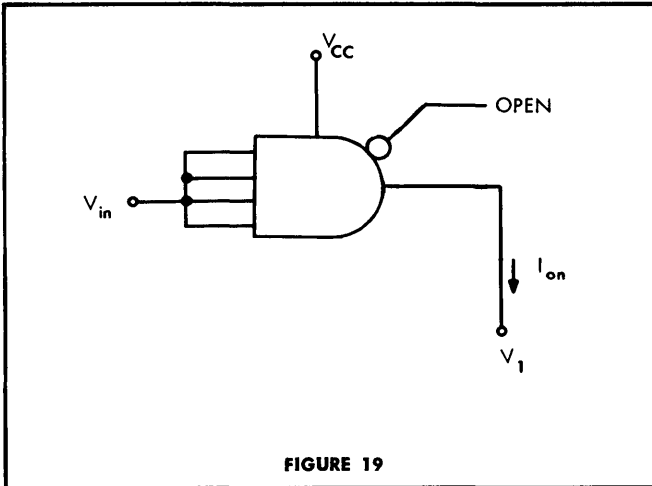


FIGURE 18

§Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

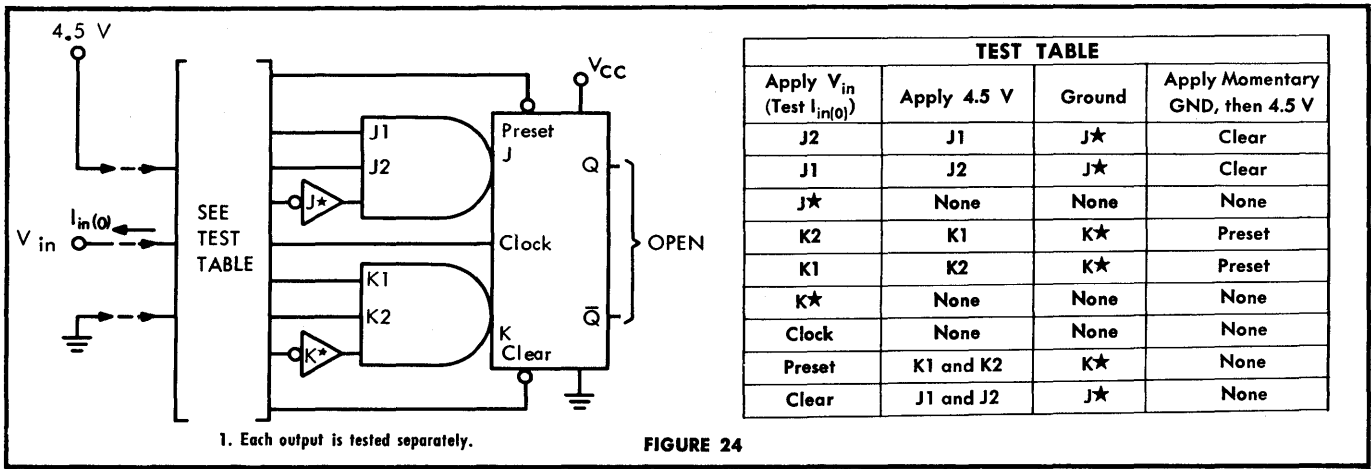
**d-c test circuits§ (continued)**



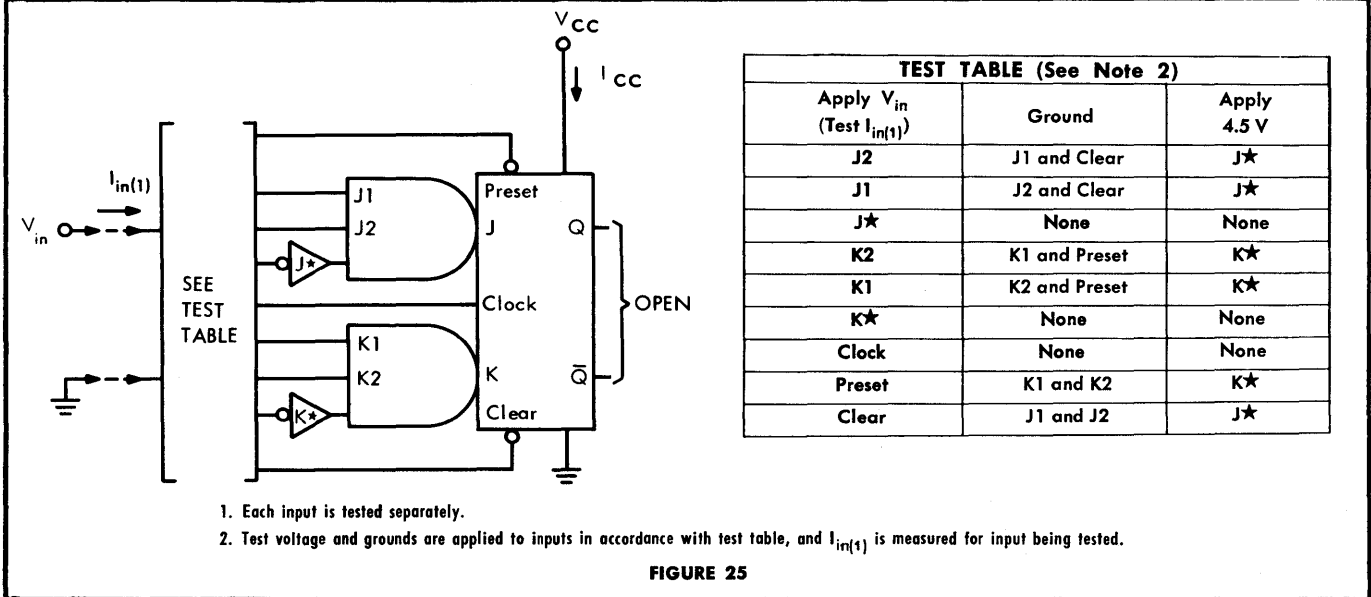
§Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

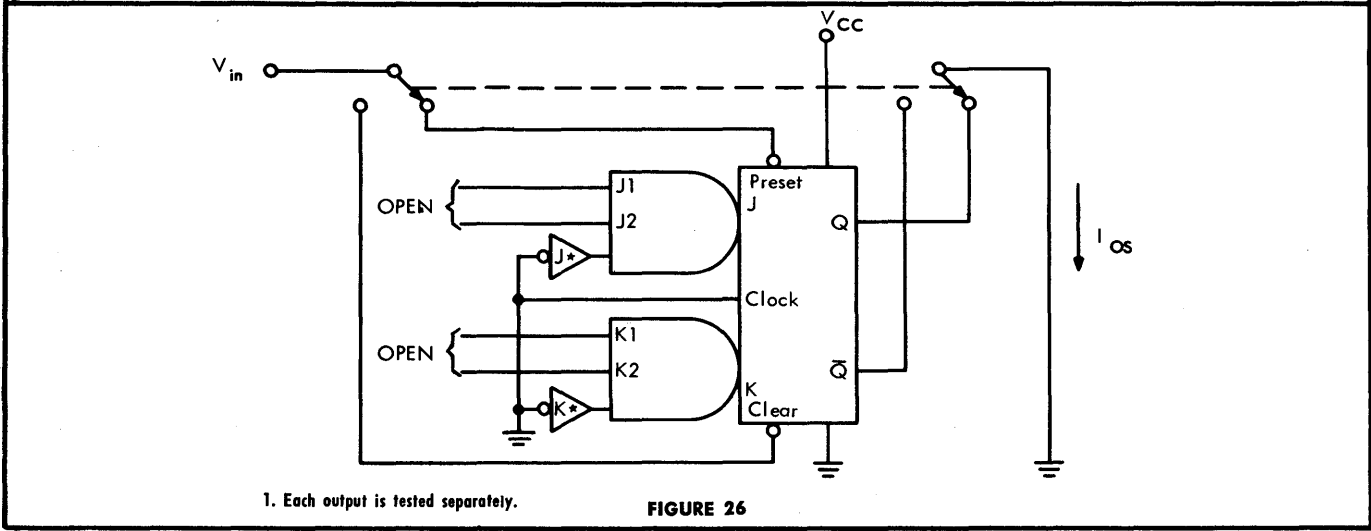
**d-c test circuits§ (continued)**



**FIGURE 24**



**FIGURE 25**

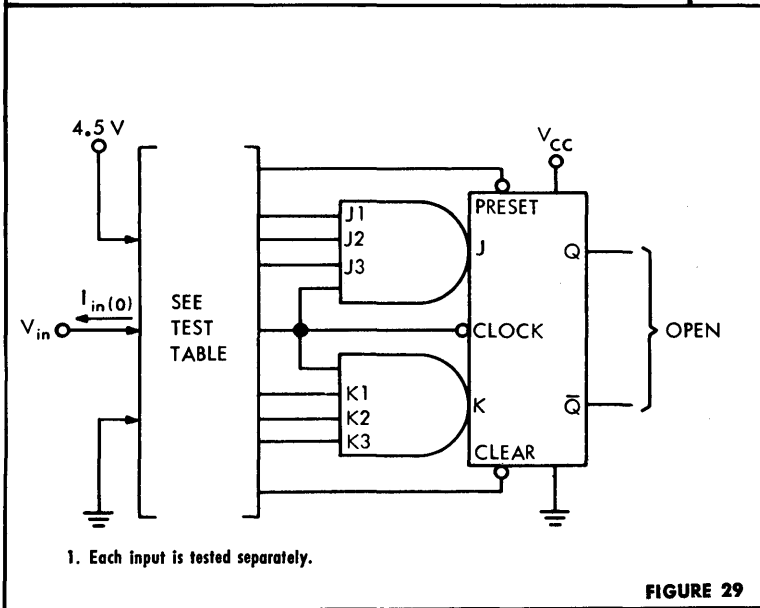
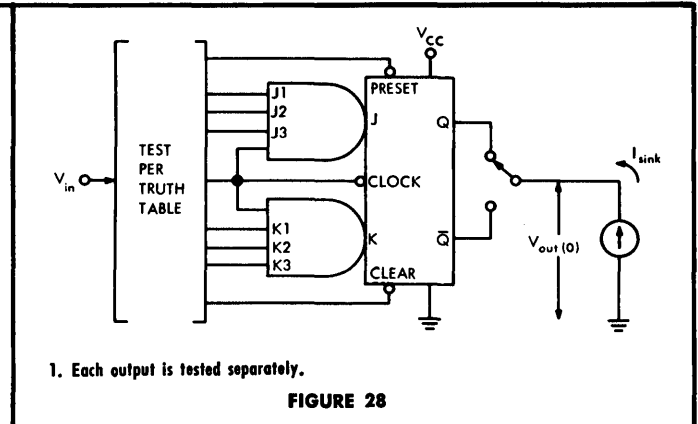
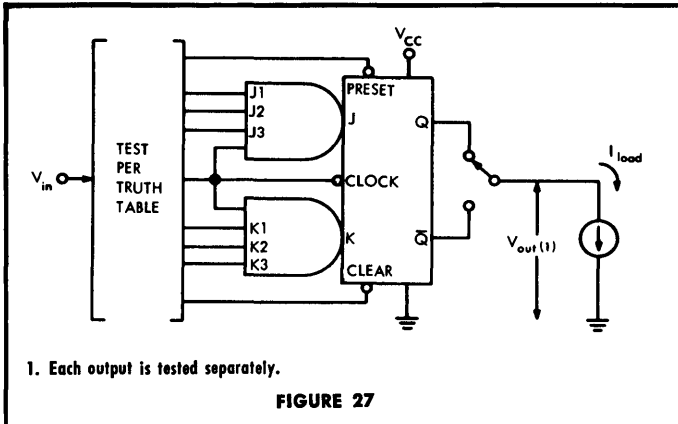


**FIGURE 26**

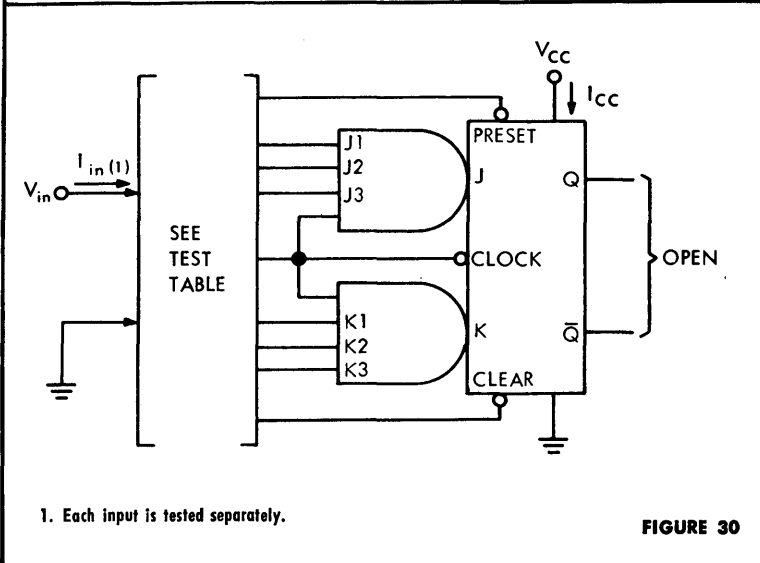
§ Arrows indicate actual direction of current flow.

## PARAMETER MEASUREMENT INFORMATION

### d-c test circuits§ (continued)



TEST TABLE		
Apply $V_{in}$ (Test $I_{in(0)}$ )	Apply Momentary GND, then 4.5 V	Apply 4.5 V
Clock	Preset	J1, J2, J3, K1, K2, and K3
Clock	Clear	J1, J2, J3, K1, K2, and K3
Preset	None	J1, J2, J3, K1, K2, and K3
Clear	None	J1, J2, J3, K1, K2, and K3
J1	Clear	Clock, J2, and J3
J2	Clear	Clock, J1, and J3
J3	Clear	Clock, J1, and J2
K1	Preset	Clock, K2, and K3
K2	Preset	Clock, K1, and K3
K3	Preset	Clock, K1, and K2

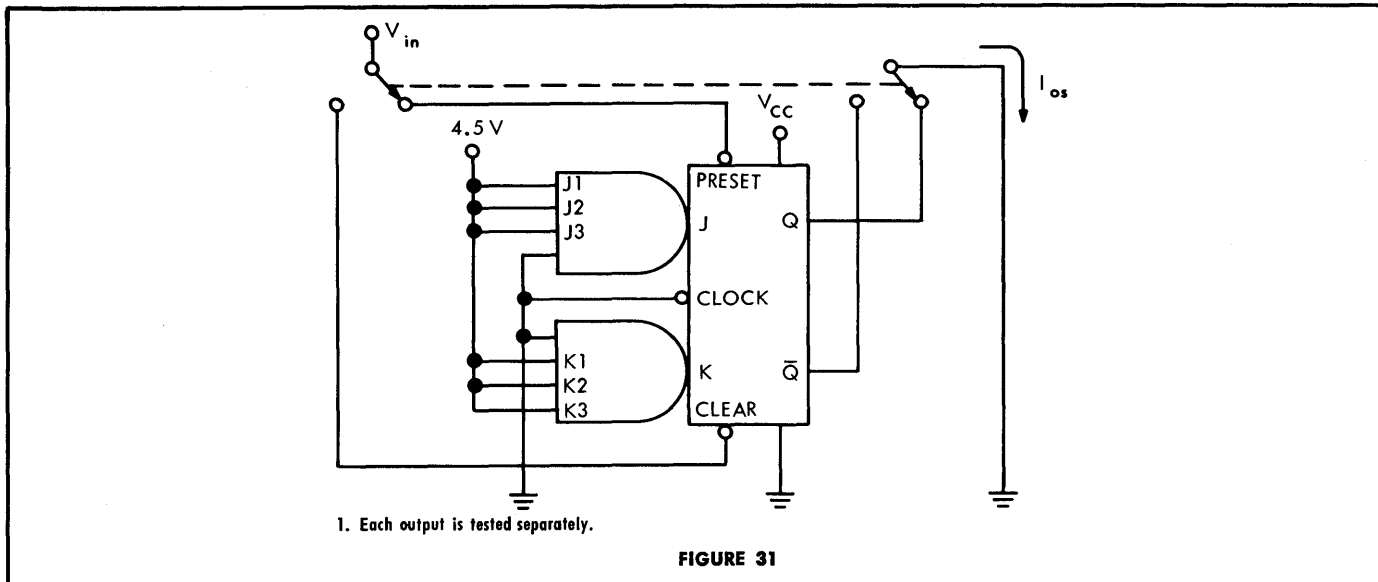


TEST TABLE	
Apply $V_{in}$ (Test $I_{in(1)}$ )	Ground
Clock	Preset, Clear, J1, J2, J3, K1, K2, and K3
Preset	Clock, K1, K2, and K3
Clear	Clock, J1, J2, and J3
J1	Clock, Clear, J2, and J3
J2	Clock, Clear, J1, and J3
J3	Clock, Clear, J1, and J2
K1	Clock, Preset, K2, and K3
K2	Clock, Preset, K1, and K3
K3	Clock, Preset, K1, and K2

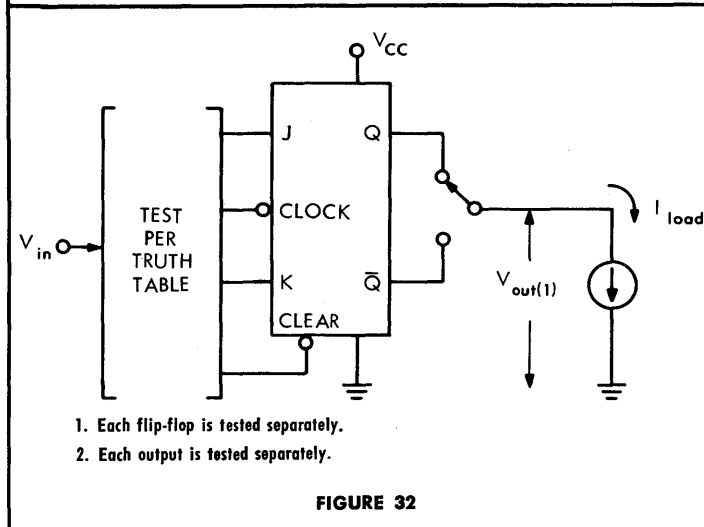
§Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

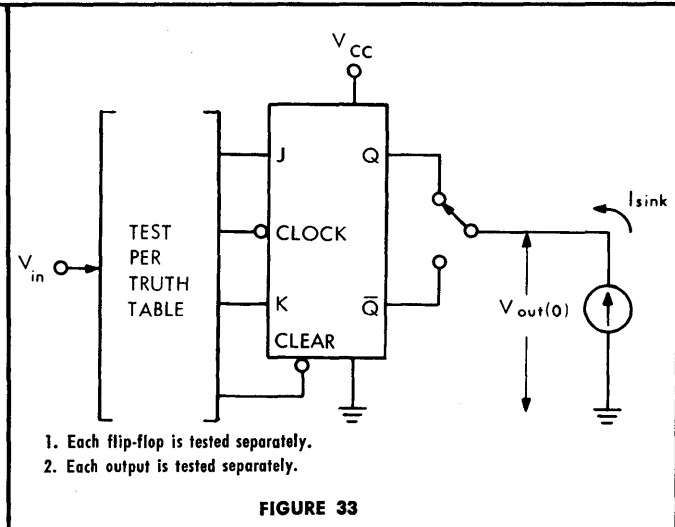
**d-c test circuits § (continued)**



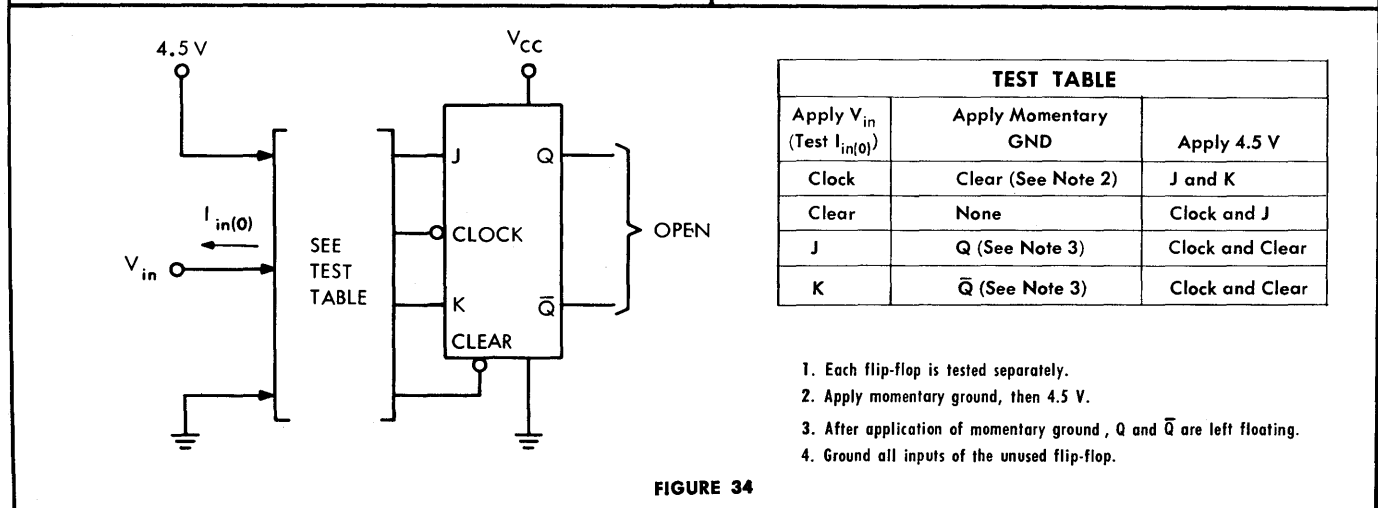
**FIGURE 31**



**FIGURE 32**



**FIGURE 33**



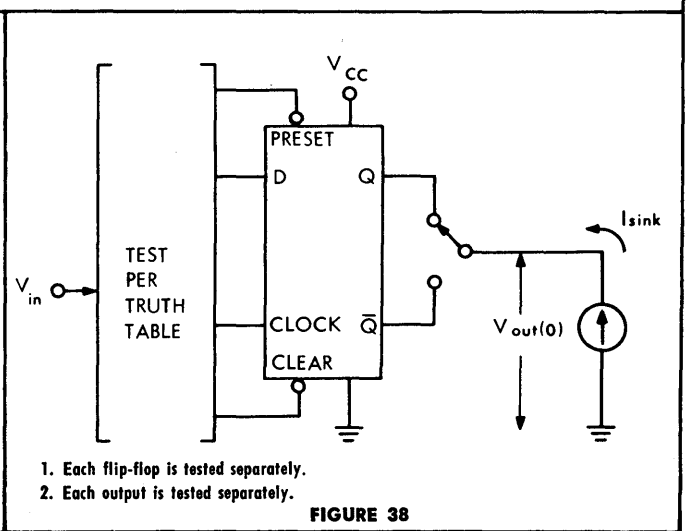
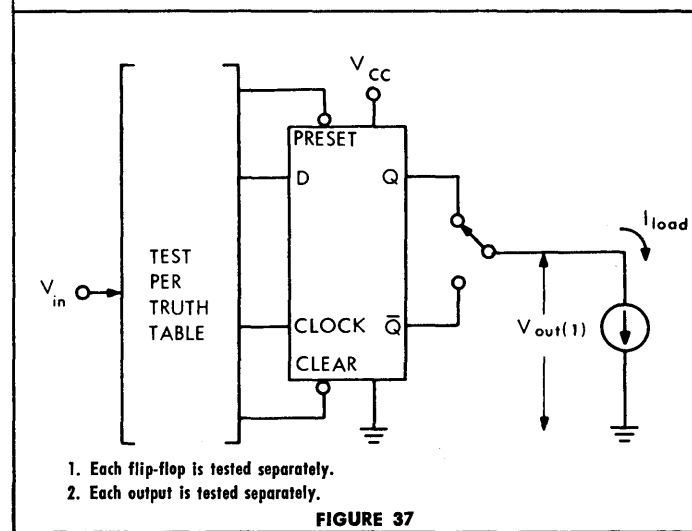
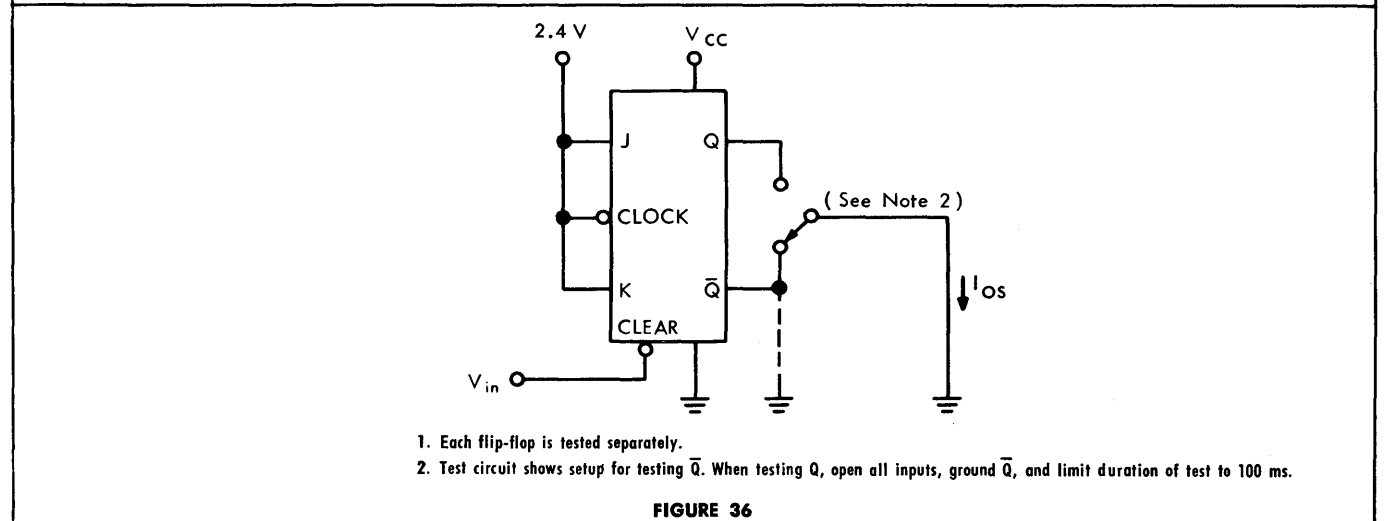
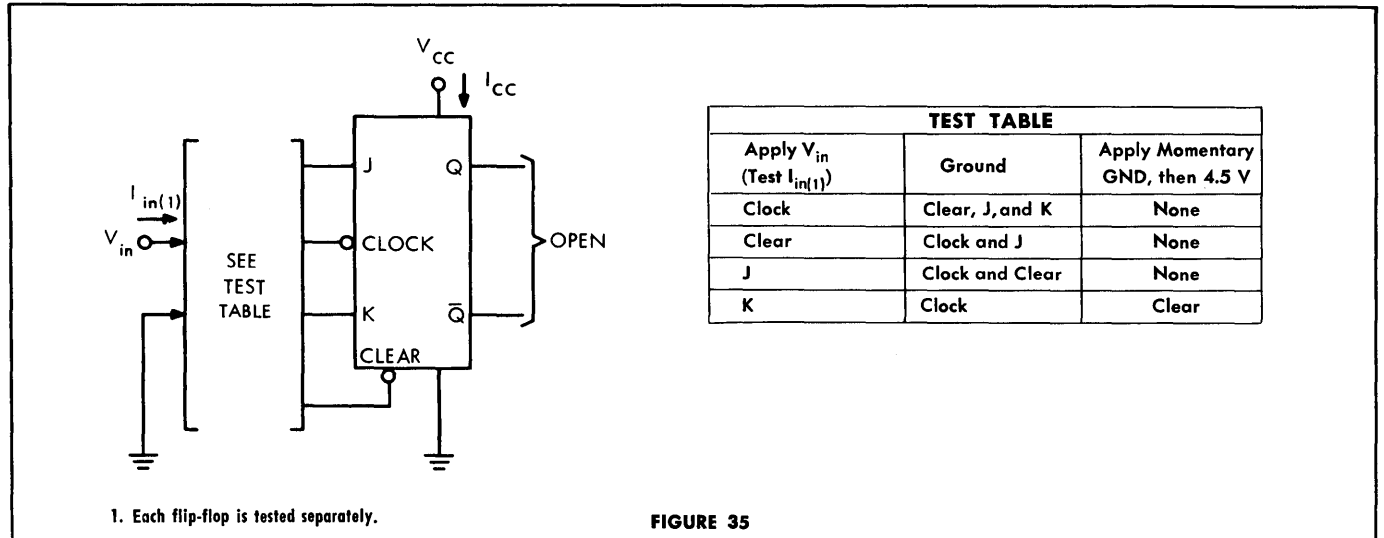
**FIGURE 34**

TEST TABLE		
Apply $V_{in}$ (Test $I_{in(0)}$ )	Apply Momentary GND	Apply 4.5 V
Clock	Clear (See Note 2)	J and K
Clear	None	Clock and J
J	Q (See Note 3)	Clock and Clear
K	$\bar{Q}$ (See Note 3)	Clock and Clear

§ Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

**d-c test circuits § (continued)**



§Arrows indicate actual direction of current flow.



PARAMETER MEASUREMENT INFORMATION

d-c test circuits § (continued)

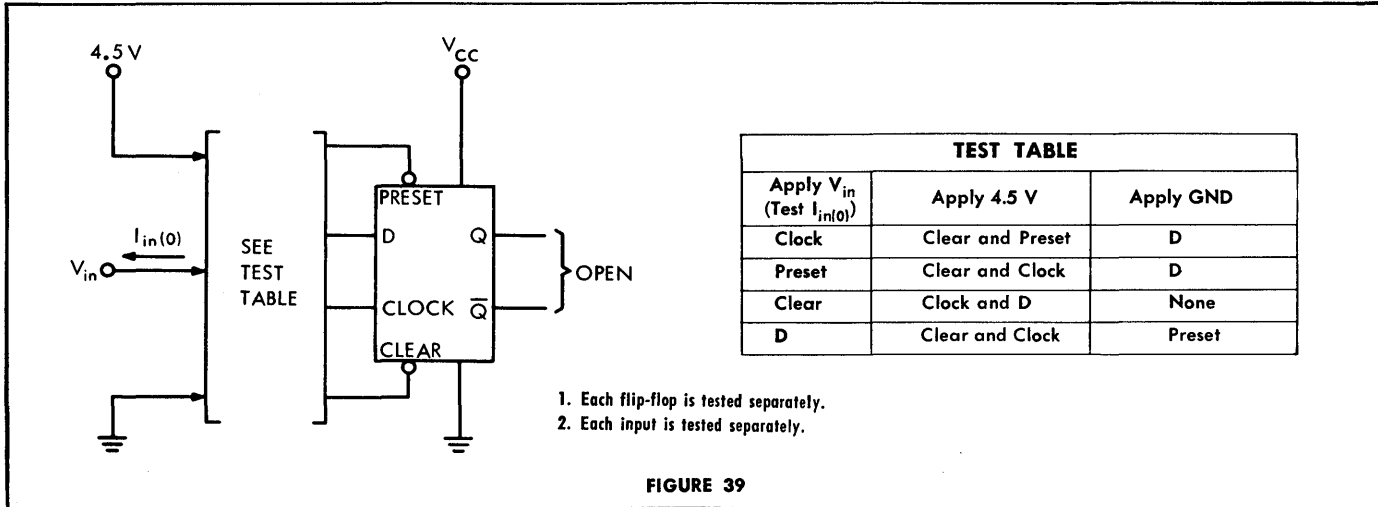


FIGURE 39

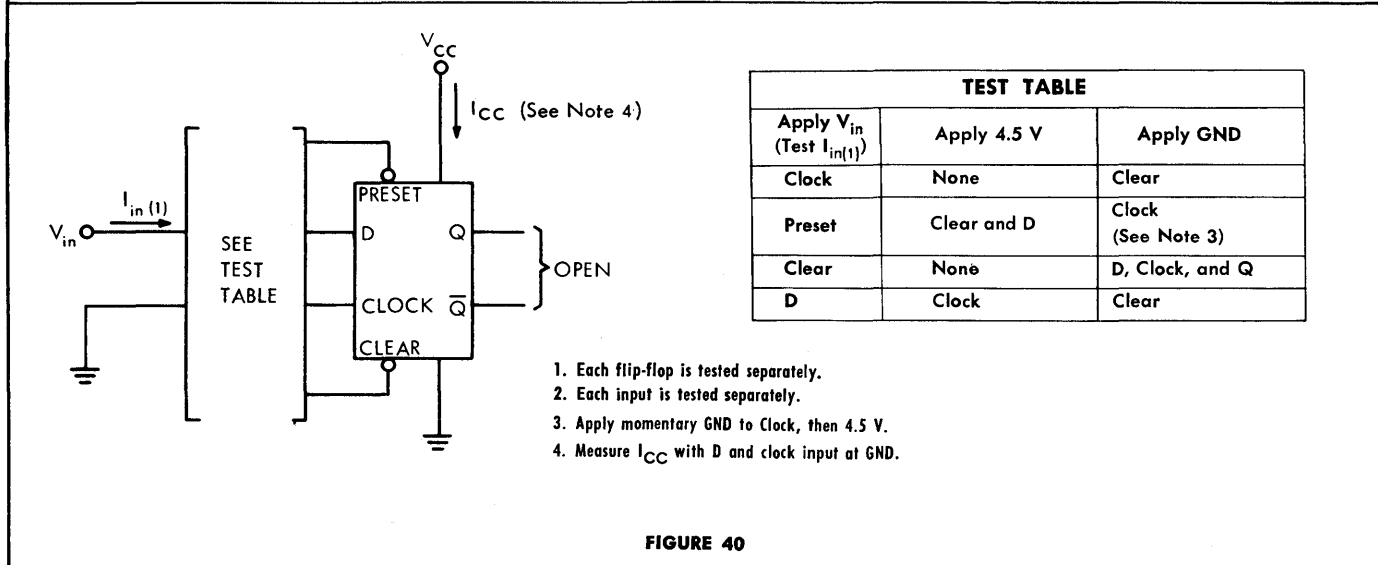


FIGURE 40

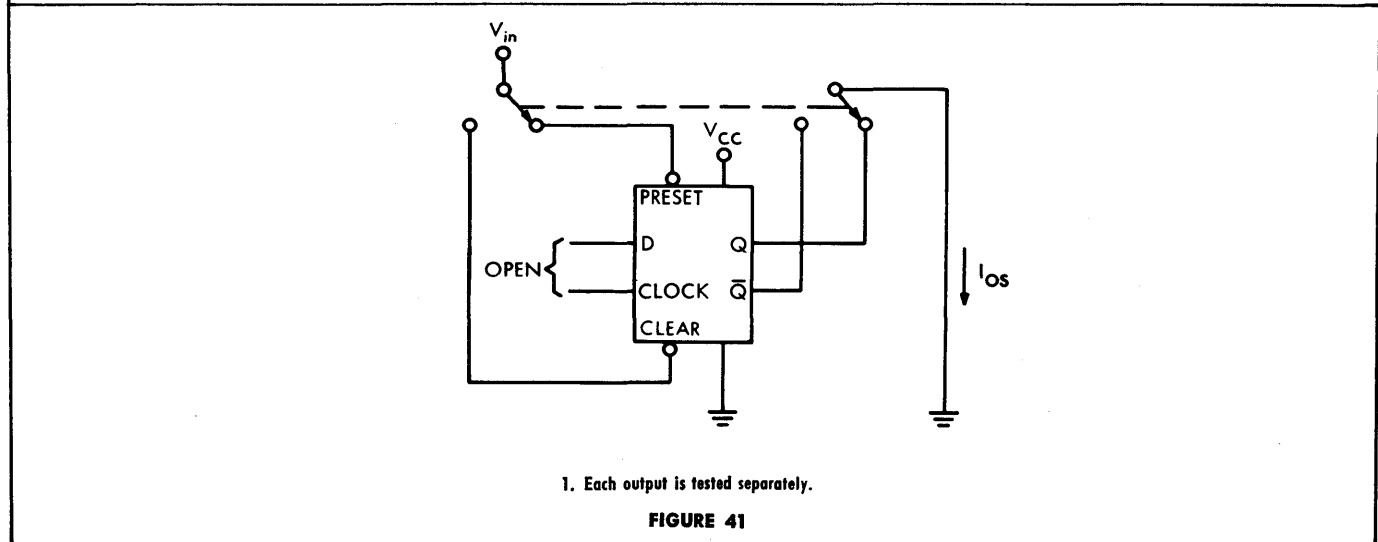
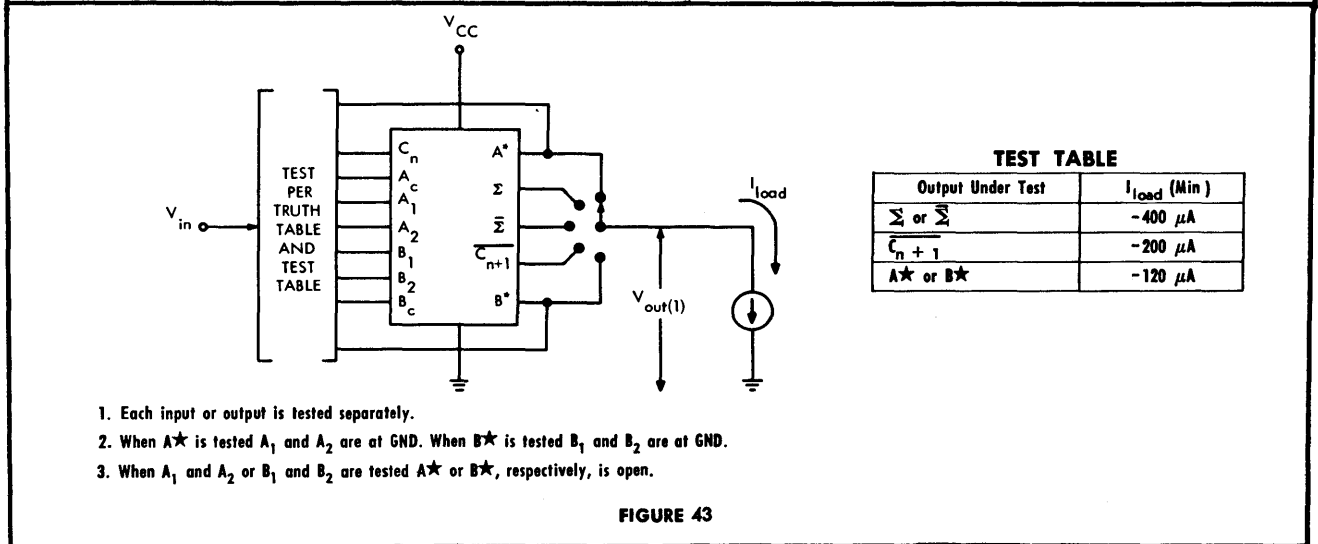
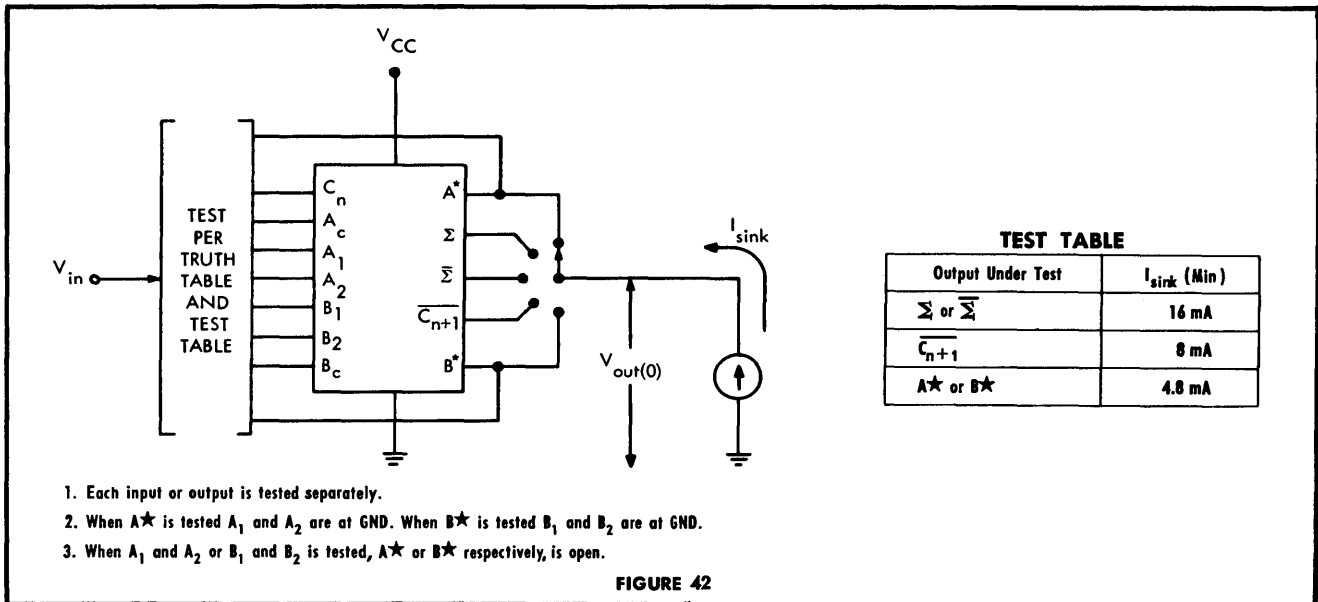


FIGURE 41

§Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

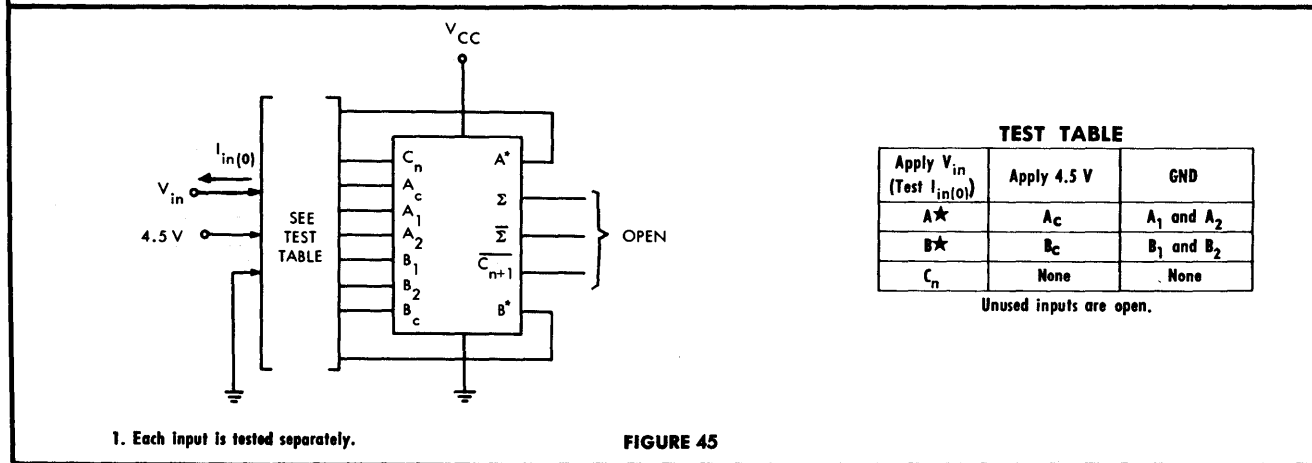
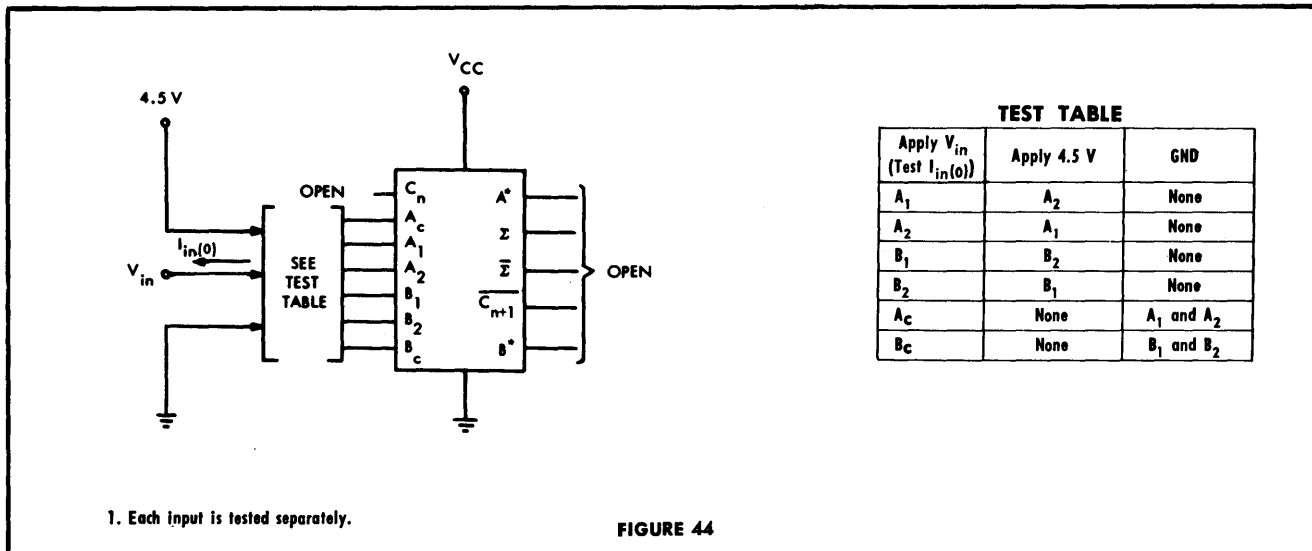
**d-c test circuits § (continued)**



§Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

**d-c test circuits (continued)**



Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

**d-c test circuits§(continued)**

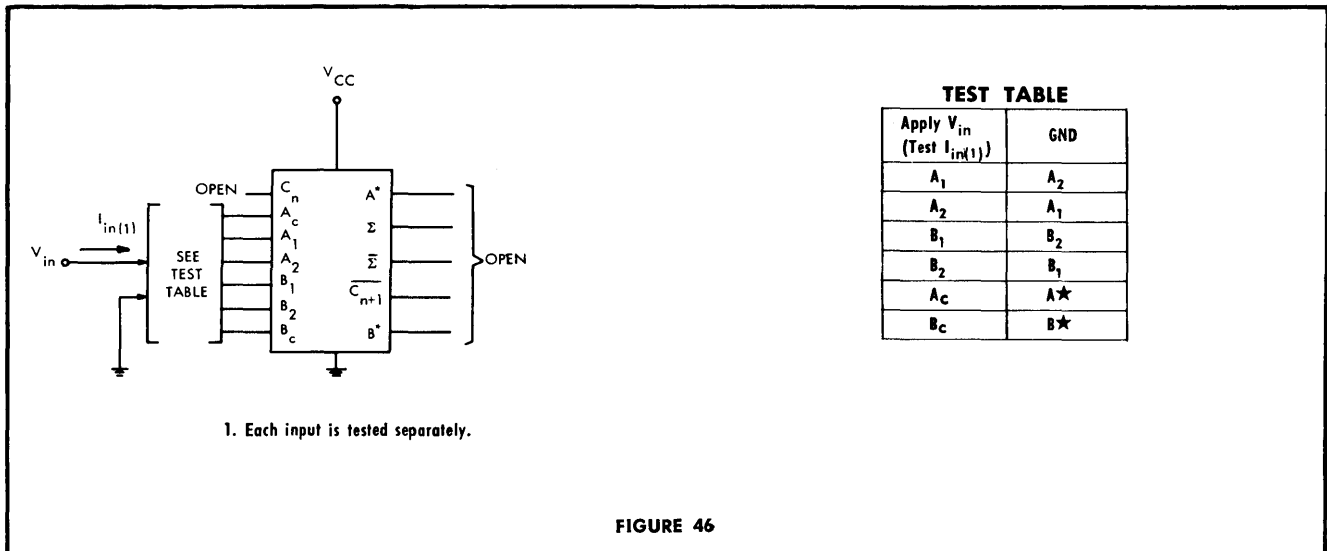


FIGURE 46

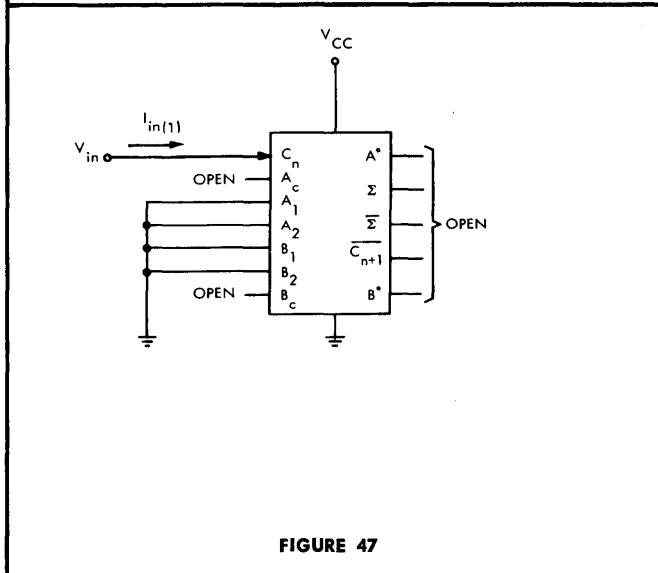


FIGURE 47

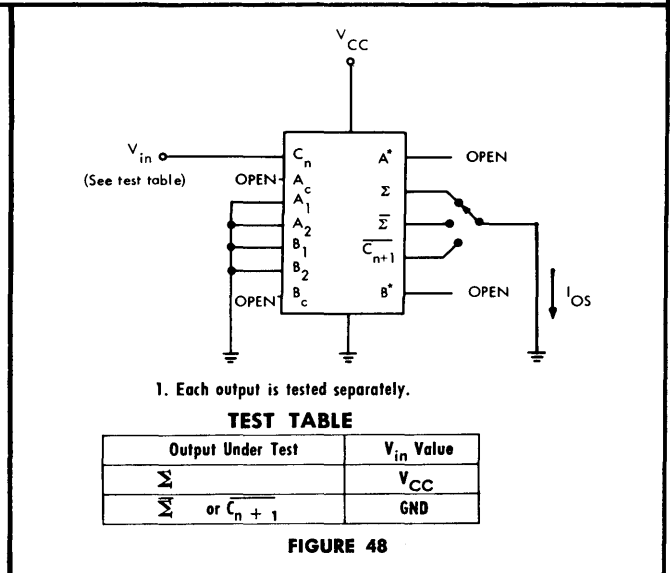


FIGURE 48

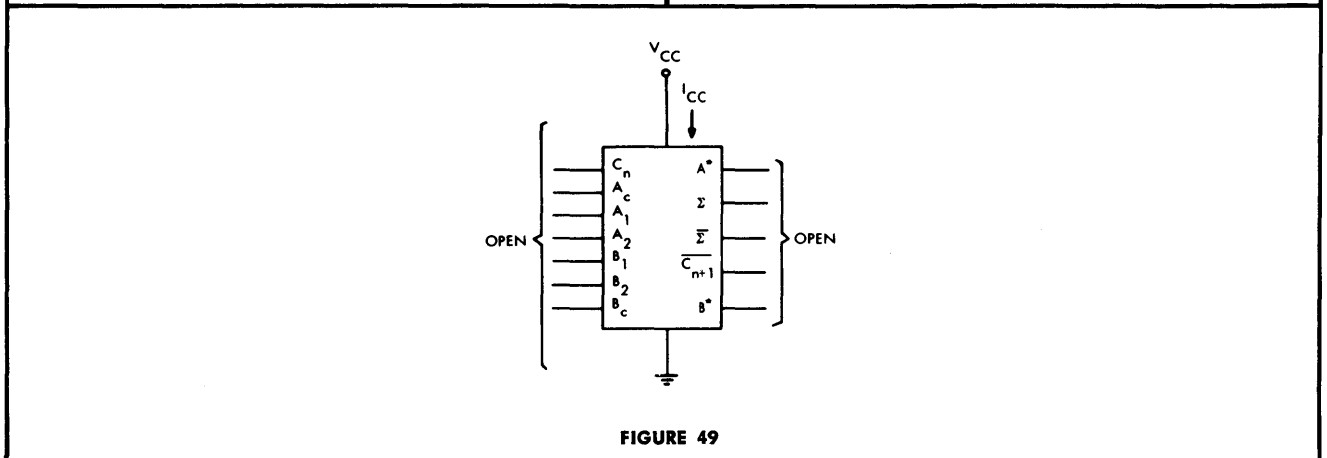
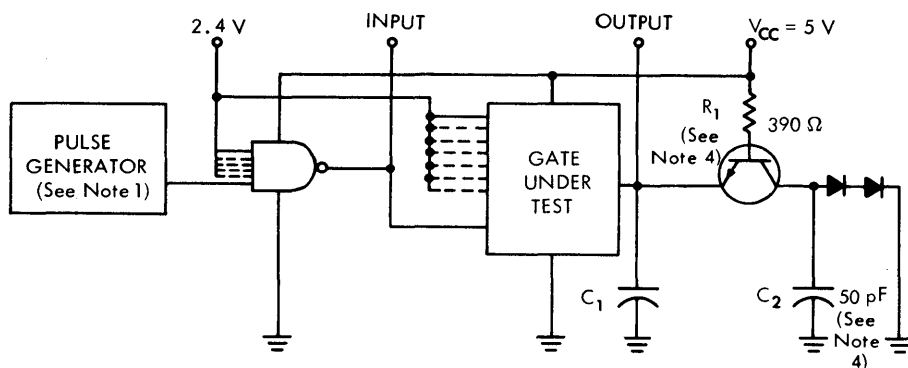


FIGURE 49

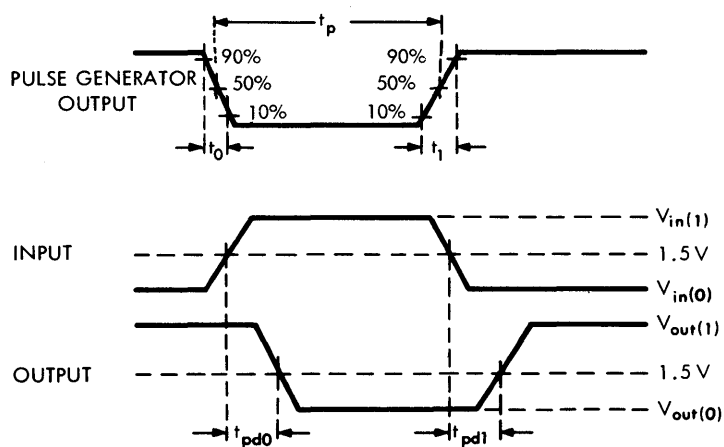
§ Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

**switching characteristics**



**TEST CIRCUIT**



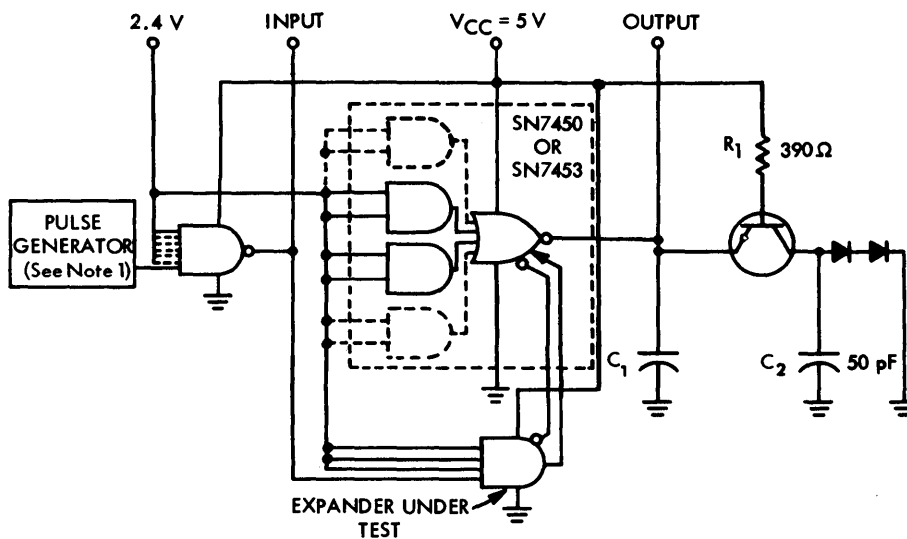
**VOLTAGE WAVEFORMS**

- NOTES: 1. The generator has the following characteristics:  $t_0 = t_1 \leq 15 \text{ ns}$ ,  $t_p = 0.5 \mu\text{s}$ ,  $\text{PRR} = 1 \text{ MHz}$ ,  $Z_{\text{out}} \approx 50 \Omega$ .  
 2. All transistors are 2N2368.  
 3. All diodes are 1N916.  
 4. Test SN7440 with  $R_1 = 130 \Omega$ ,  $C_2 = 150 \text{ pF}$ .  
 5.  $t_{\text{pd}} = \frac{t_{\text{pd0}} + t_{\text{pd1}}}{2}$   
 6.  $C_1$  includes probe and jig capacitance.

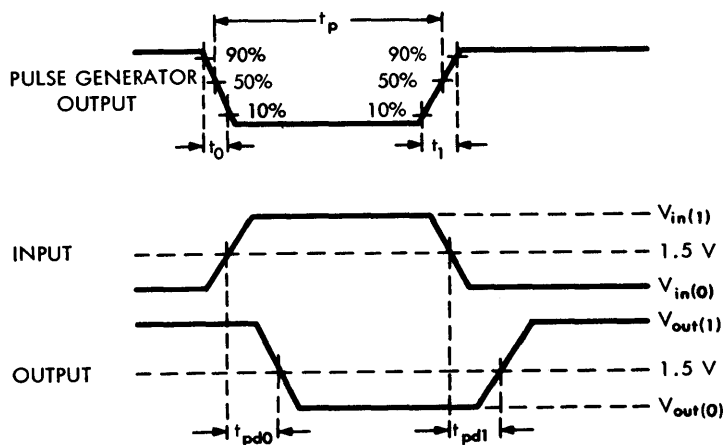
**FIGURE 50 — GATE PROPAGATION DELAY TIMES**

**PARAMETER MEASUREMENT INFORMATION**

switching characteristics (continued)



**TEST CIRCUIT**



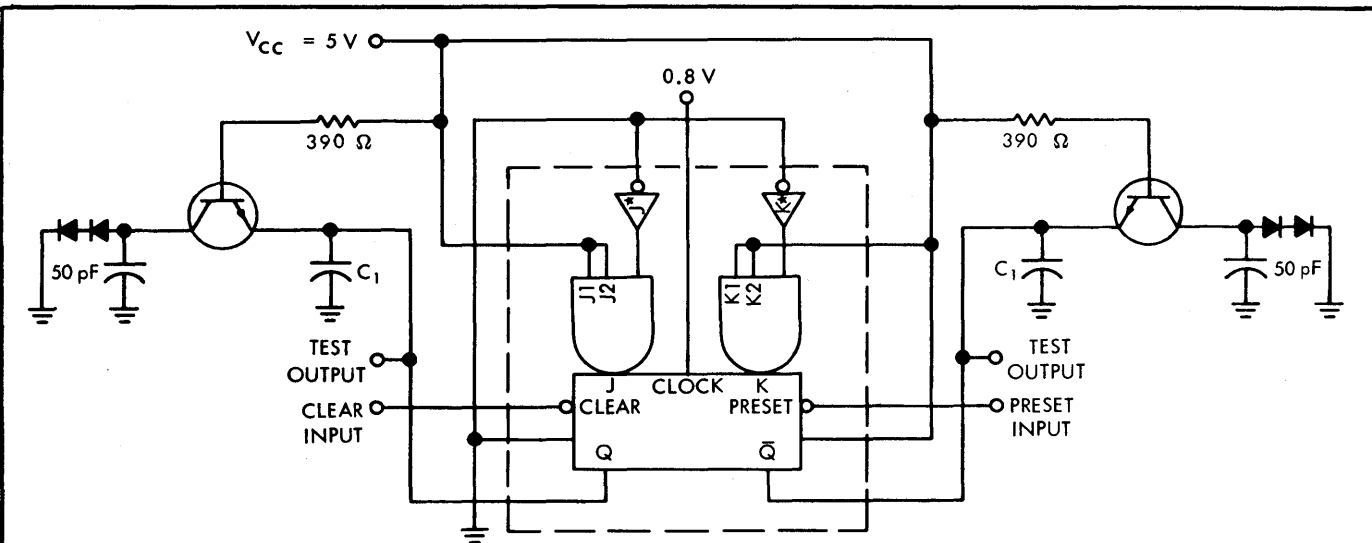
**VOLTAGE WAVEFORMS**

- NOTES:
1. The generator has the following characteristics:  $t_0 = t_1 \leq 15 \text{ ns}$ ,  $t_p = 0.5 \mu\text{s}$ ,  $\text{PRR} = 1 \text{ MHz}$ ,  $Z_{\text{out}} \approx 50 \Omega$ .
  2. All transistors are 2N2368.
  3. All diodes are 1N916.
  4.  $t_{\text{pd}} = \frac{t_{\text{pd0}} + t_{\text{pd1}}}{2}$
  5.  $C_1$  includes probe and jig capacitance.

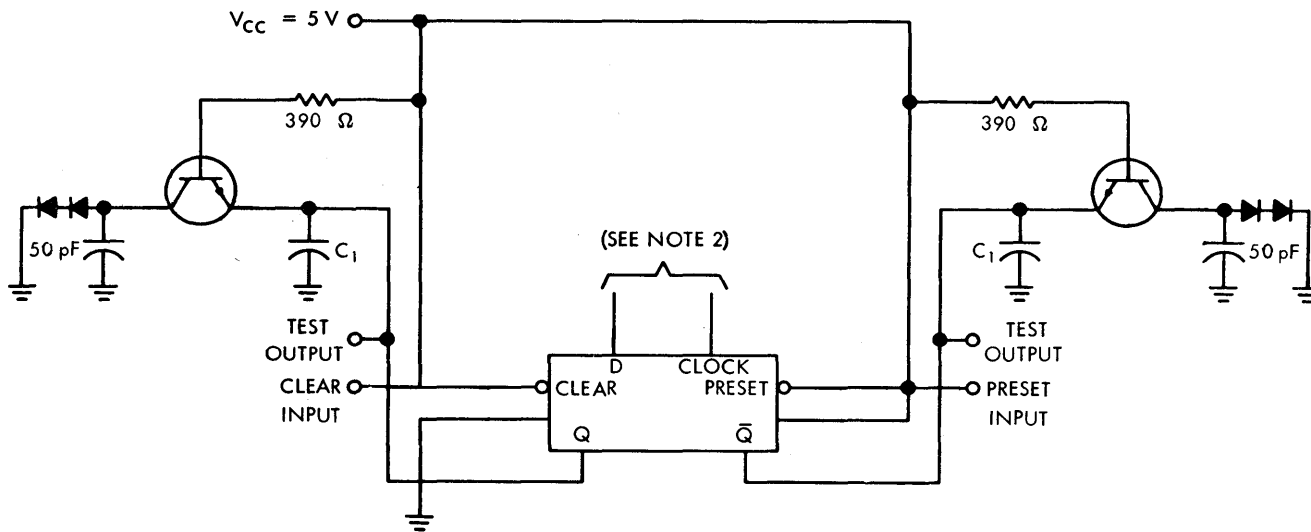
**FIGURE 51 — EXPANDER PROPAGATION DELAY TIMES**

**PARAMETER MEASUREMENT INFORMATION**

switching characteristics (continued)



TEST CIRCUIT SN7470



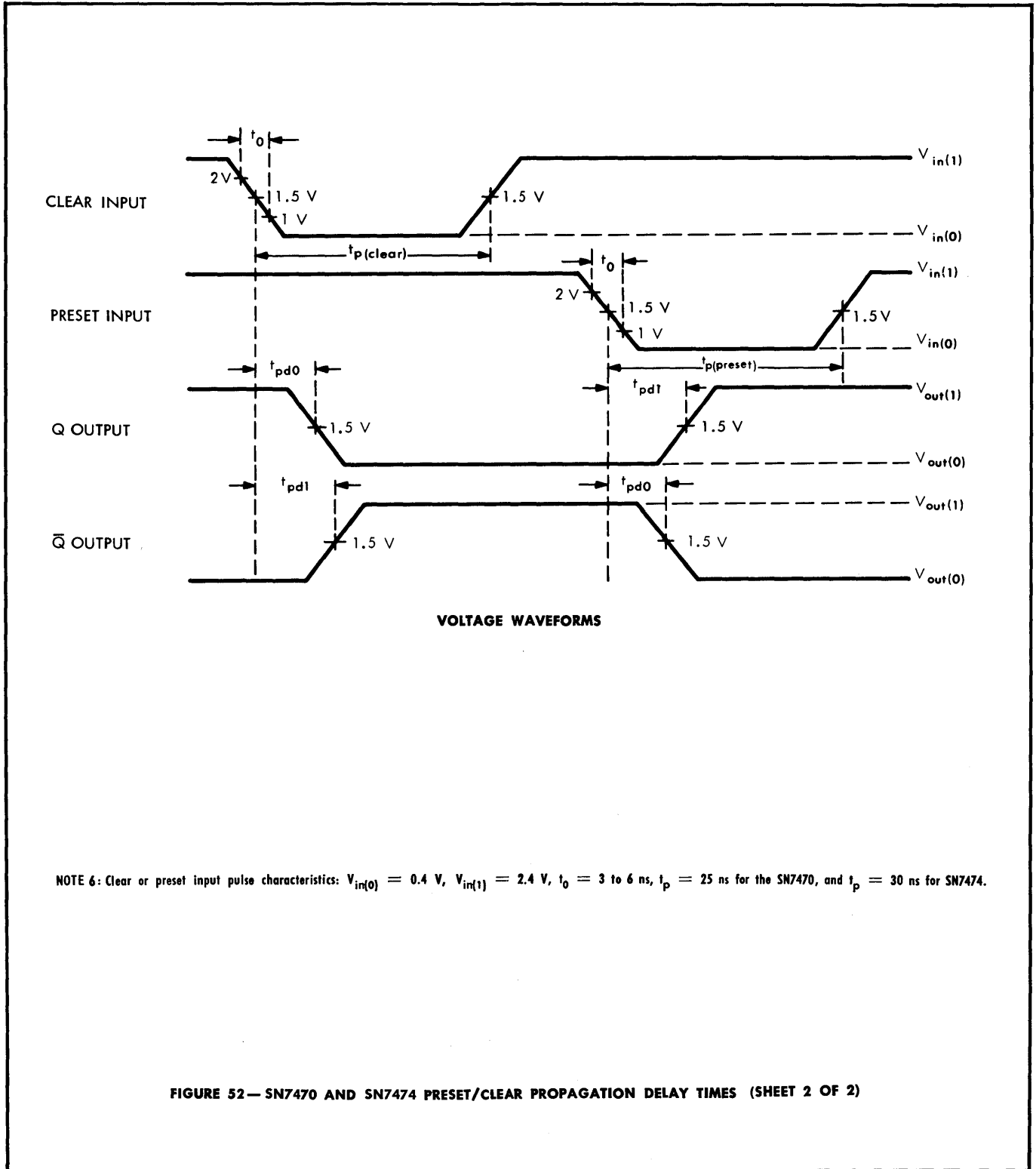
TEST CIRCUIT SN7474

- NOTES:
1. Present or clear function of the SN7470 can occur only when clock input is low. Gated inputs are inhibited.
  2. Clear and preset inputs of the SN7474 dominate regardless of the state of clock or D inputs.
  3. All transistors are 2N2368.
  4. All diodes are 1N916.
  5.  $C_1$  includes probe and jig capacitance.

FIGURE 52 — SN7470 AND SN7474 PRESET/CLEAR PROPAGATION DELAY TIMES (SHEET 1 OF 2)

**PARAMETER MEASUREMENT INFORMATION**

switching characteristics (continued)

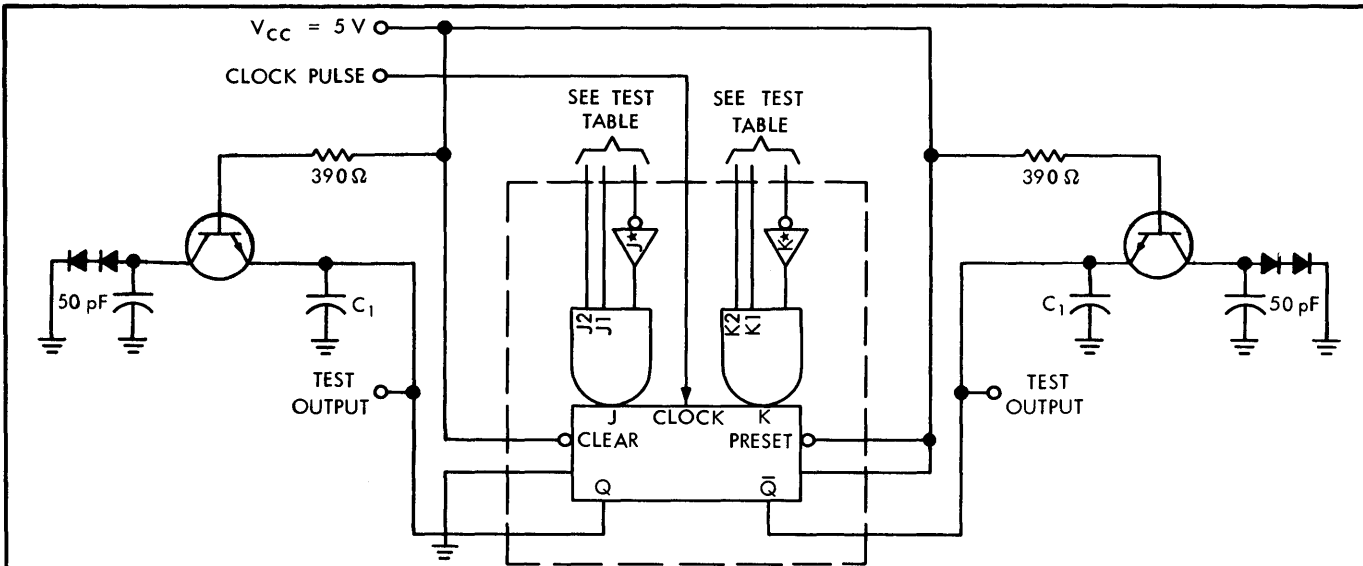


**FIGURE 52—SN7470 AND SN7474 PRESET/CLEAR PROPAGATION DELAY TIMES (SHEET 2 OF 2)**



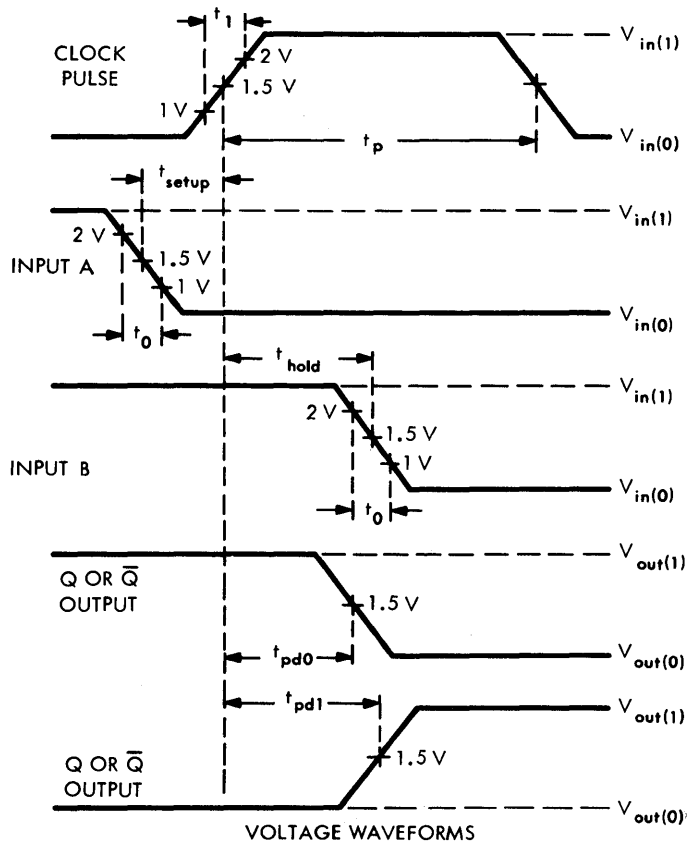
**PARAMETER MEASUREMENT INFORMATION**

**switching characteristics (continued)**



TEST TABLE					
TEST NO.	TEST	INPUT A	INPUT B	APPLY + 2.4 V	GND
1	$t_{\text{setup}}$ at J*	J*	None	J1, J2, K1, K2	K*
2	$t_{\text{hold}}$ at J1, J2	None	J1, J2	K1, K2	J* and K*
3	$t_{\text{setup}}$ at K*	K*	None	J1, J2, K1, K2	J*
4	$t_{\text{hold}}$ at K1, K2	None	K1, K2	J1, J2	J* and K*

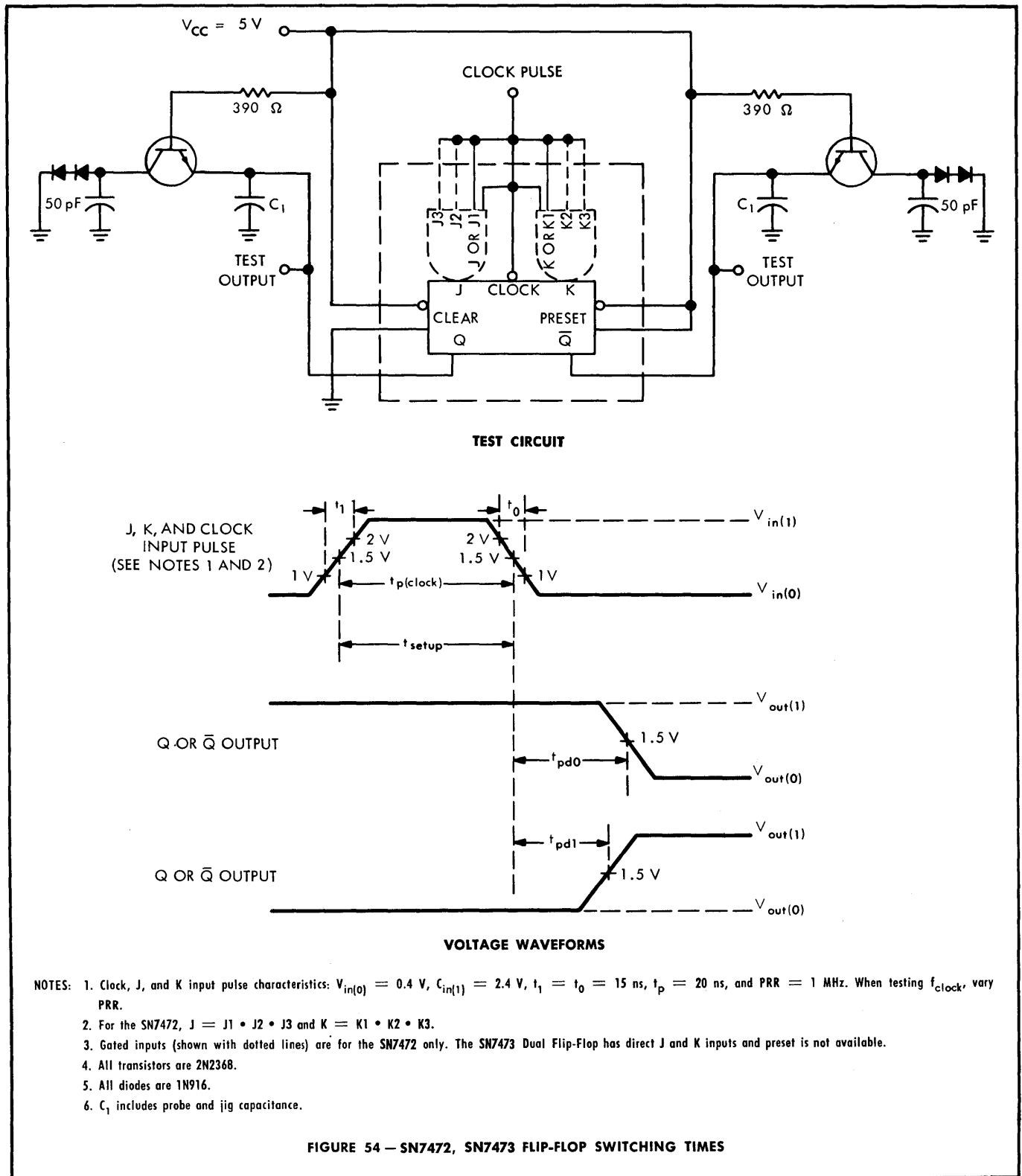
- NOTES: 1. Clock pulse (see note 3), input A, and input B are used to measure  $t_{\text{setup}}$  and  $t_{\text{hold}}$ .
2. Clock frequency,  $t_{\text{pd1}}$ , and  $t_{\text{pd0}}$  are measured in the toggle mode. Hold J = K = logical 1 per truth table and apply clock pulse (see note 3).
3. Clock pulse characteristics:  $V_{\text{in}(0)} = 0.4 \text{ V}$ ,  $V_{\text{in}(1)} = 2.4 \text{ V}$ ,  $t_1 = 15 \text{ ns}$ ,  $t_p = 20 \text{ ns}$ , and PRR = 1 MHz. When testing  $f_{\text{clock}}$ , vary PRR.
4. Input pulse characteristics:  $V_{\text{in}(0)} = 0.4 \text{ V}$ ,  $V_{\text{in}(1)} = 2.4 \text{ V}$ ,  $t_0 = 3 \text{ to } 6 \text{ ns}$ .
5. All transistors are 2N2368.
6. All diodes are 1N916.
7.  $C_1$  includes probe and jig capacitance.



**FIGURE 53 — SN7470 FLIP-FLOP SWITCHING TIMES**

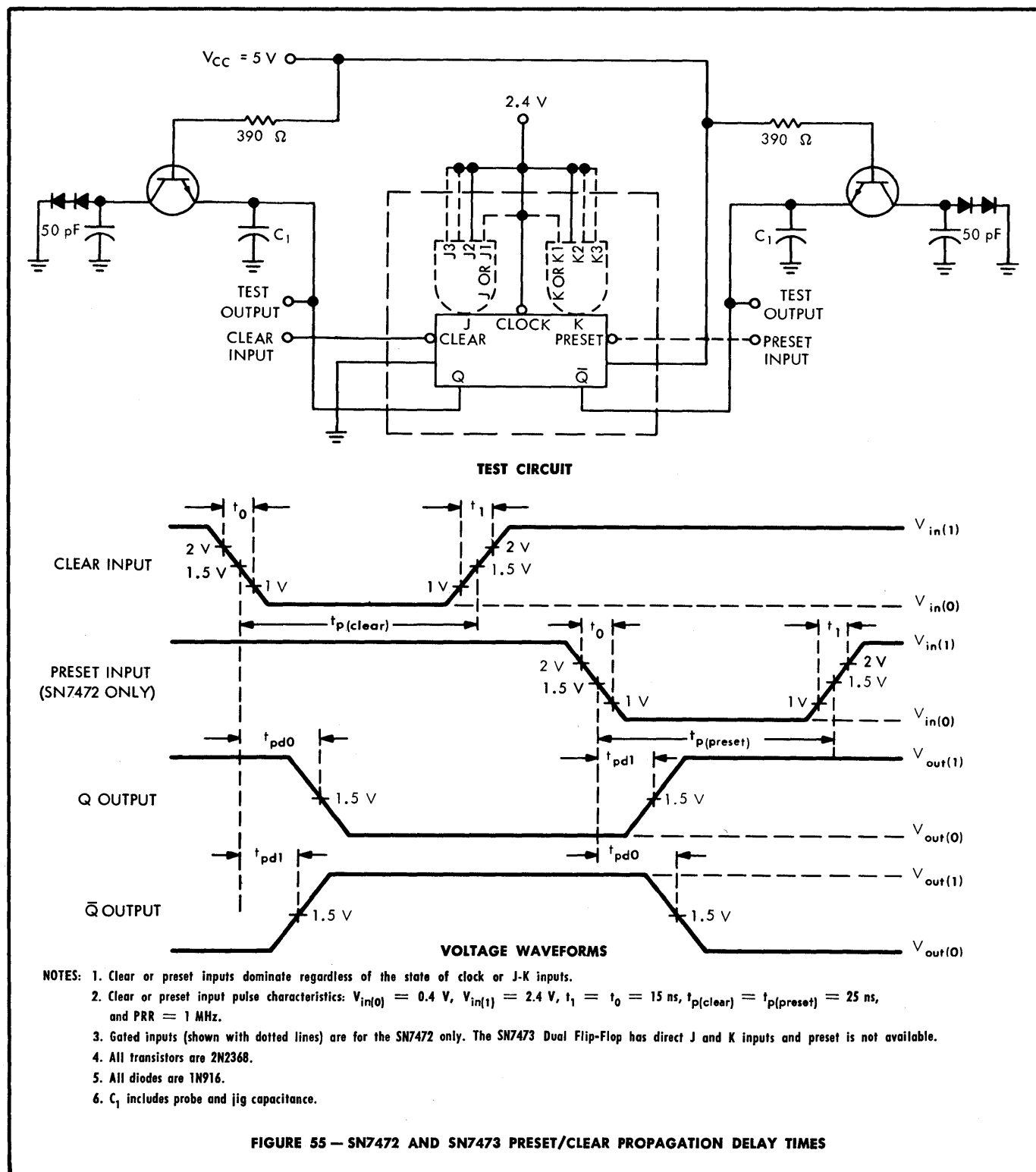
**PARAMETER MEASUREMENT INFORMATION**

**switching characteristics (continued)**



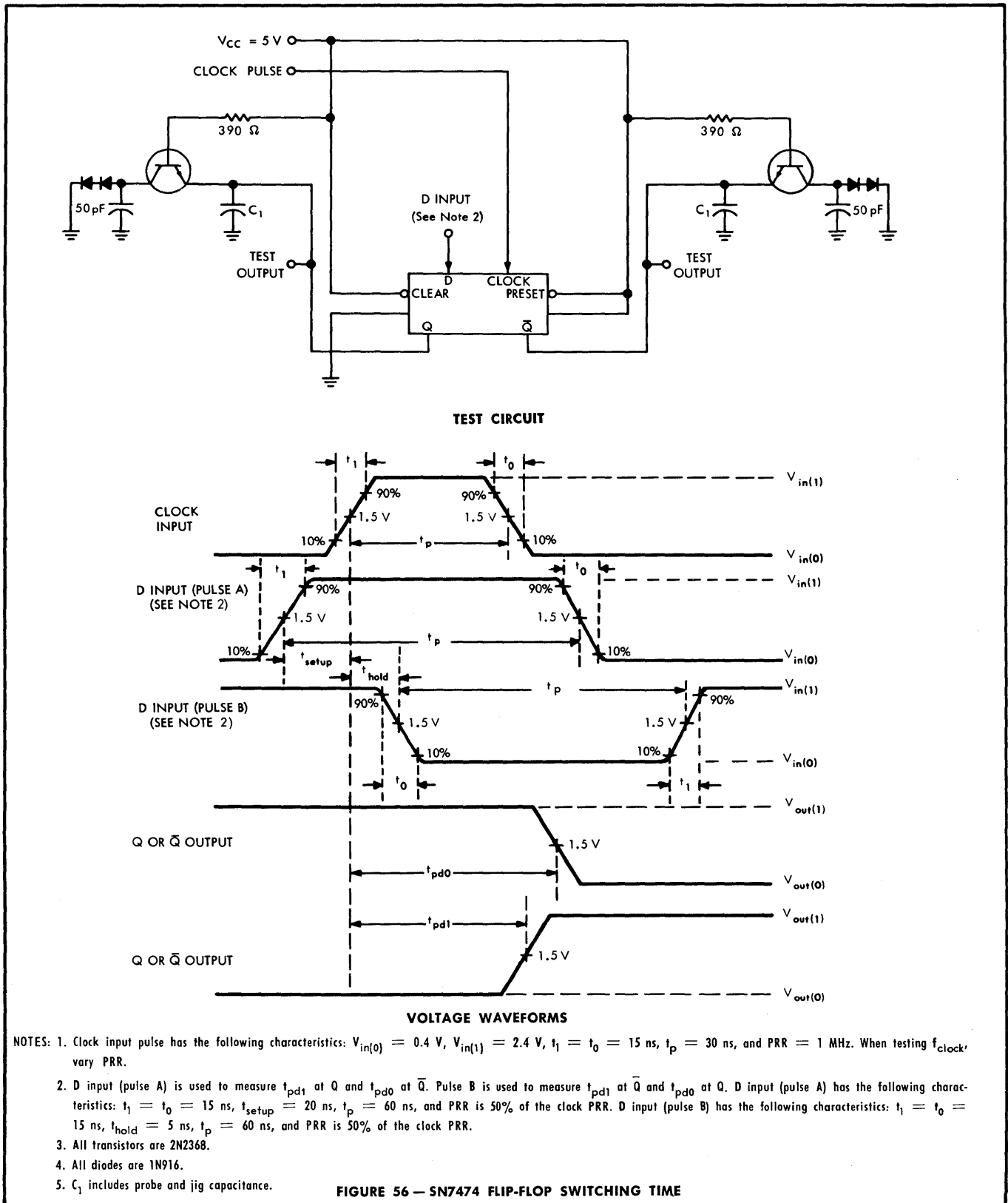
**PARAMETER MEASUREMENT INFORMATION**

**switching characteristics (continued)**



**PARAMETER MEASUREMENT INFORMATION**

**switching characteristics (continued)**



**PARAMETER MEASUREMENT INFORMATION**

**switching characteristics (continued)**

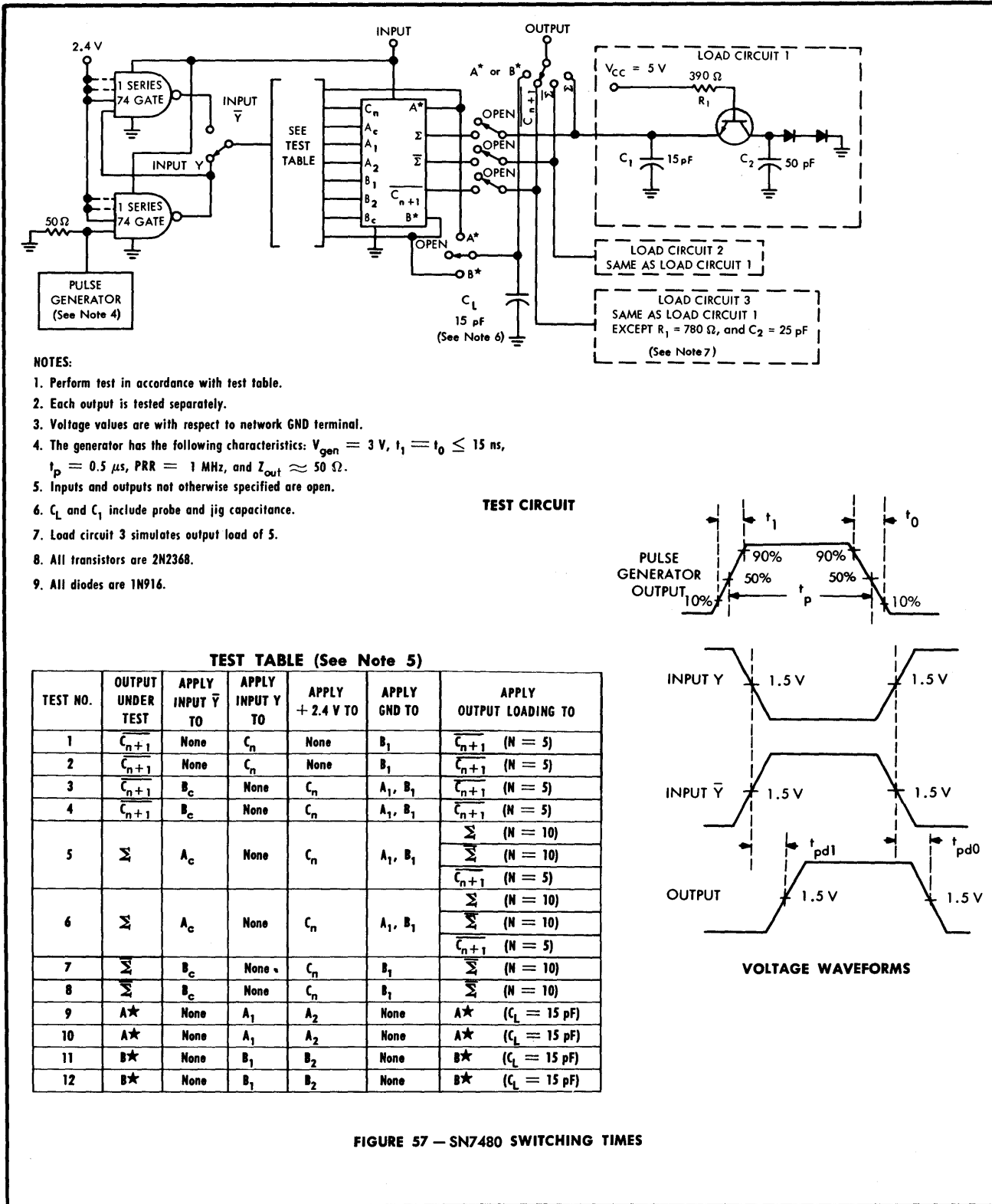


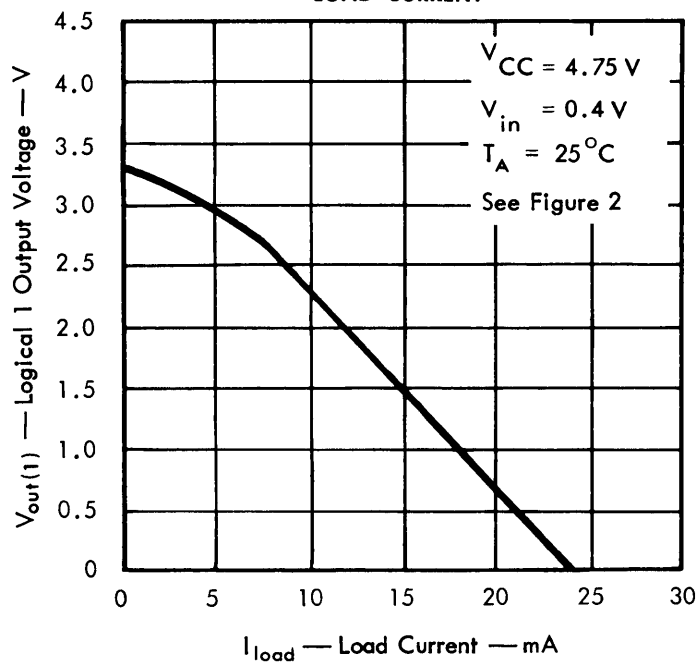
FIGURE 57 — SN7480 SWITCHING TIMES

**TYPICAL CHARACTERISTICS §**

LOGICAL 1 OUTPUT VOLTAGE

vs

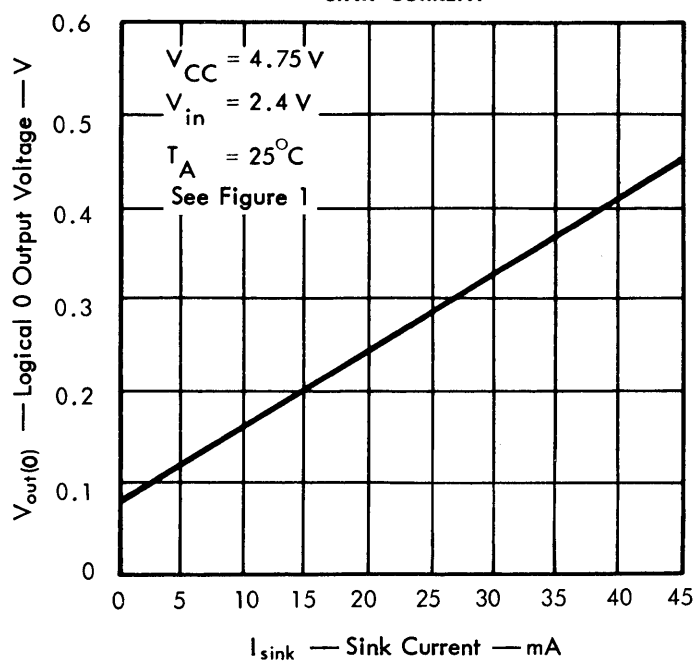
LOAD CURRENT



LOGICAL 0 OUTPUT VOLTAGE

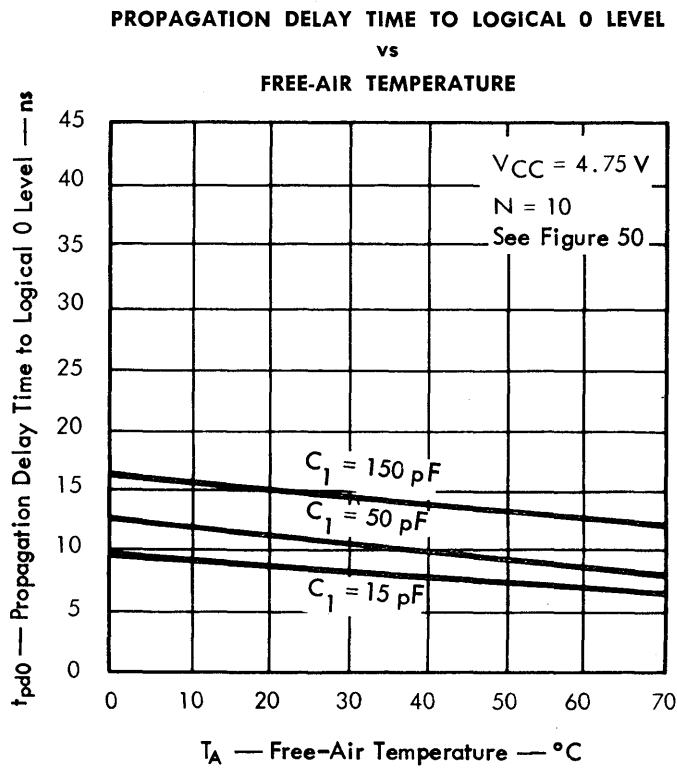
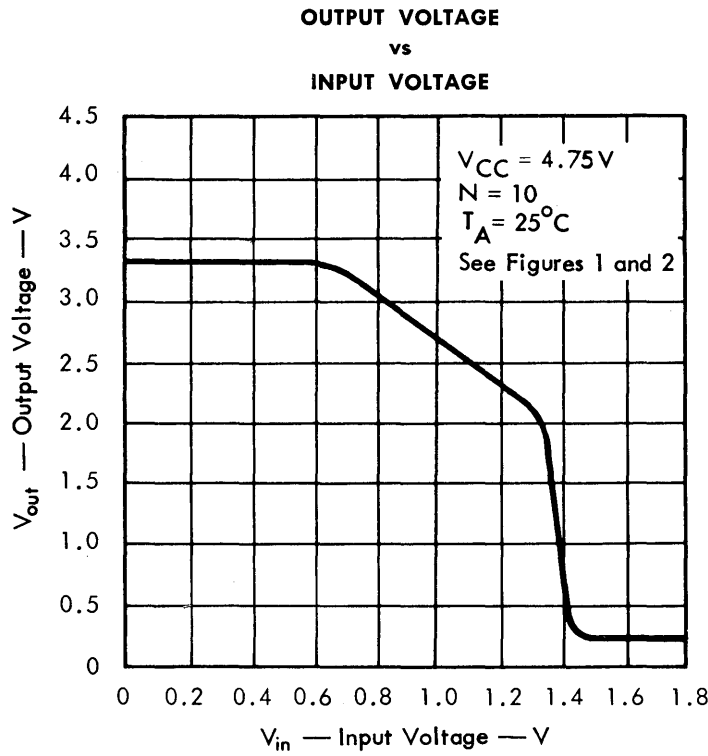
vs

SINK CURRENT



§ Unless otherwise noted, data as shown is applicable for SN7400, SN7410, SN7420, SN7430, SN7450, SN7451, SN7453, and SN7454.

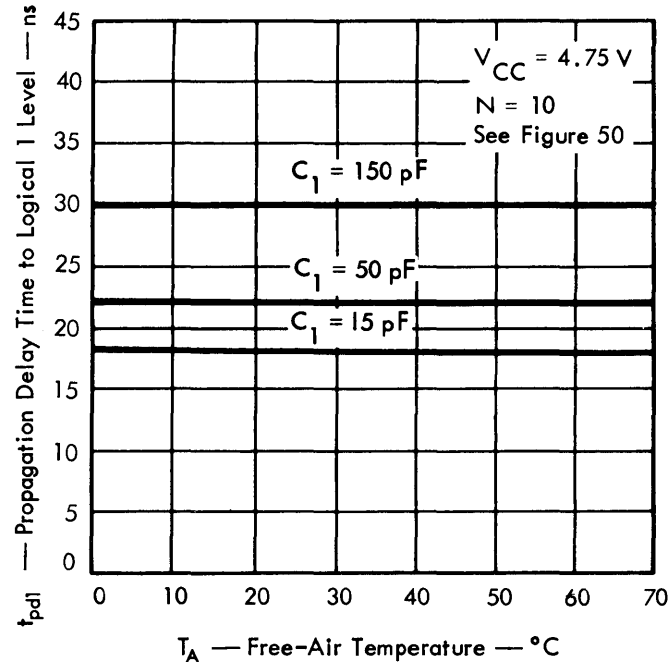
**TYPICAL CHARACTERISTICS §**



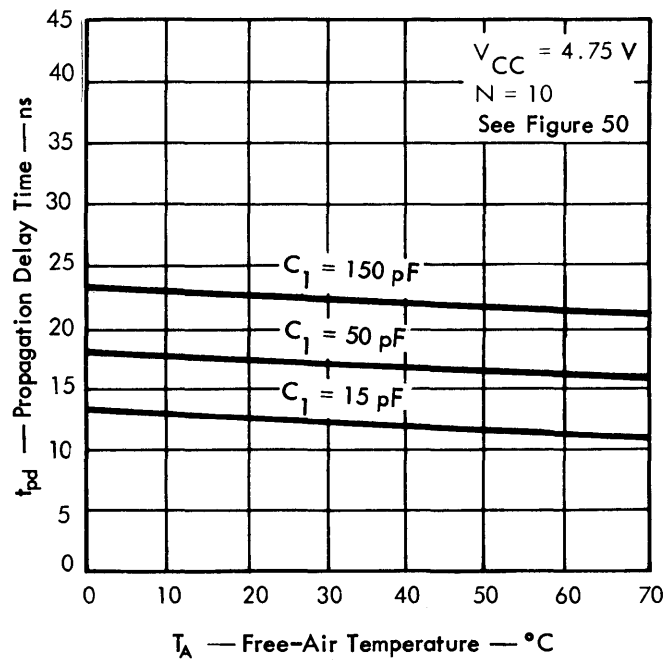
§ Unless otherwise noted, data as shown is applicable for SN7400, SN7410, SN7420, SN7430, SN7450, SN7451, SN7453, and SN7454.

**TYPICAL CHARACTERISTICS §**

**PROPAGATION DELAY TIME TO LOGICAL 1 LEVEL  
vs  
FREE-AIR TEMPERATURE**



**PROPAGATION DELAY TIME  
vs  
FREE-AIR TEMPERATURE**



§ Unless otherwise noted, data as shown is applicable for SN7400, SN7410, SN7420, SN7430, SN7450, SN7451, SN7453, and SN7454.



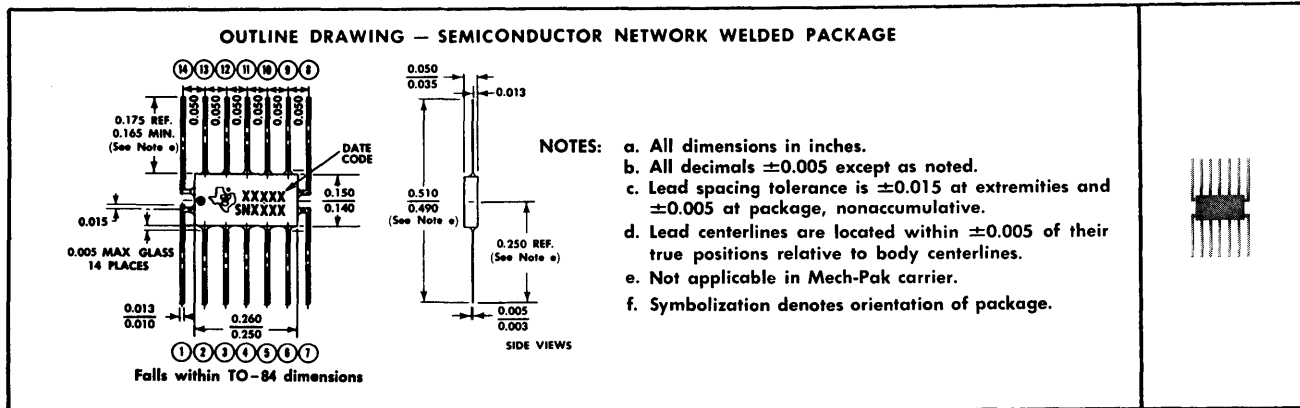
# SERIES 74 SOLID CIRCUIT<sup>®</sup> SEMICONDUCTOR NETWORKS<sup>†</sup>

## MECHANICAL DATA

### general

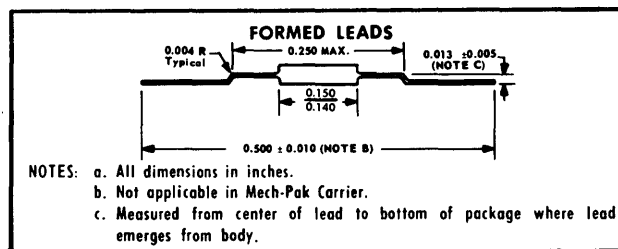
Series 74 semiconductor networks are mounted in glass-to-metal hermetically sealed, welded packages. Package body and leads are gold-plated F-15<sup>‡</sup> glass-sealing alloy. Approximate weight is

0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. All Series 74 networks are available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier.



### leads

Gold-plated F-15<sup>‡</sup> leads require no additional cleaning or processing when used in soldered or welded assembly. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Standard lead length is 0.175 inch. Networks can be removed from Mech-Pak carriers with lead lengths up to 0.175 inch.

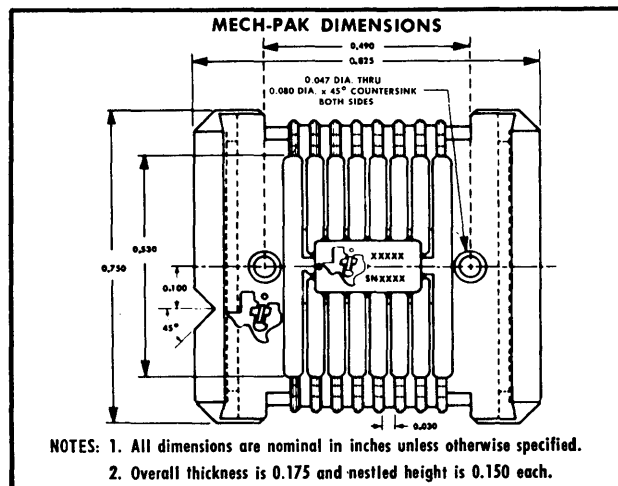


### insulator

An insulator, secured to the back surface of the package, permits mounting networks on circuit boards which have conductors passing beneath the package. The insulator is 0.0025 inch thick and has an insulation resistance of greater than 10 megohms at 25°C.

### mech-pak carrier

The Mech-Pak carrier facilitates handling the network, and is compatible with automatic equipment used for testing and assembly. The carrier is particularly appropriate for mechanized assembly operations and will withstand temperatures of 125°C for indefinite periods.



### ordering instructions

Variations in mechanical configuration of semiconductor networks are identified by suffix numbers shown in a table at the right.

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
	0.175 Inch				Not Applicable			
Lead Length	No	No	Yes	Yes	No	No	Yes	Yes
Formed Leads	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5

<sup>†</sup>Patented by Texas Instruments

<sup>‡</sup>F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.



**HIGH-SPEED TTL DIGITAL SEMICONDUCTOR NETWORKS  
IN  
DTL PIN CONFIGURATIONS**

SERIES 74 930  
BULLETIN NO. DL-S 669227, NOVEMBER 1966

**description**

Series 74 930 consists of Texas Instruments high-speed TTL circuits with pin configurations and logic functions that make them electrically compatible and mechanically interchangeable with Series 15 830 DTL circuits. In addition to five interchangeable networks, an 8-input NAND gate and a dual AND-OR-INVERT gate are available.

**comparative features**

	SERIES 15 830 DTL	SERIES 74 930 TTL
Gate propagation delay time (typically) . . . . .	25 ns	13 ns
Fan-out capability . . . . . (DTL can drive 8 DTL or 5 TTL loads, TTL can drive 10 TTL or 10 DTL loads)	8	10
Noise immunity (guaranteed) . . . . .	350 mV	400 mV

**standard line summary**

FUNCTION	TYPES	SIMILAR DTL CIRCUIT
Dual 4-Input Positive NAND Gate	SN74 930	SN15 830
Dual 4-Input Positive NAND Buffer	SN74 932	SN15 832
Quadruple 2-Input Positive NAND Gate	SN74 946	SN15 846
Triple 3-Input Positive NAND Gate	SN74 962	SN15 862
8-Input Positive NAND Gate	SN74 965	None
Dual 2-Wide 2-Input AND-OR-INVERT Gate	SN74 966	None
Master-Slave Flip-Flop	SN74 948	SN15 831/SN15 845/SN15 848

**specifications**

Schematic diagrams, fan-out rules, maximum ratings, temperature ranges, and electrical characteristics are identical to those of the corresponding Series 74 type number.

SERIES 74 930 TYPE	CORRESPONDING SERIES 74 TYPE
SN74 930	SN7420
SN74 932	SN7440
SN74 946	SN7400
SN74 948	See Note 1
SN74 962	SN7410
SN74 965	SN7430
SN74 966	SN7451

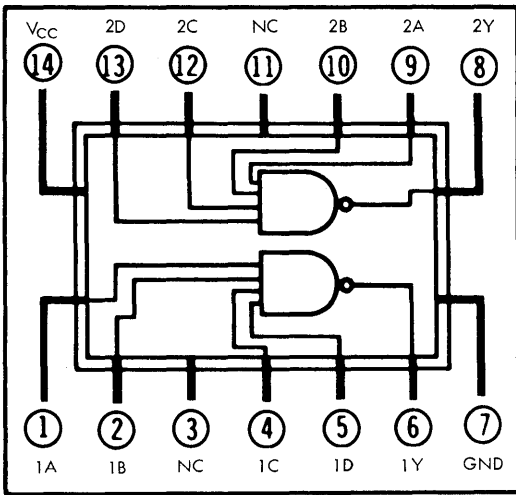
NOTE 1: The SN74 948 has no corresponding Series 74 type. Electrical and switching characteristics are included in this data sheet.

<sup>†</sup>Patented by Texas Instruments

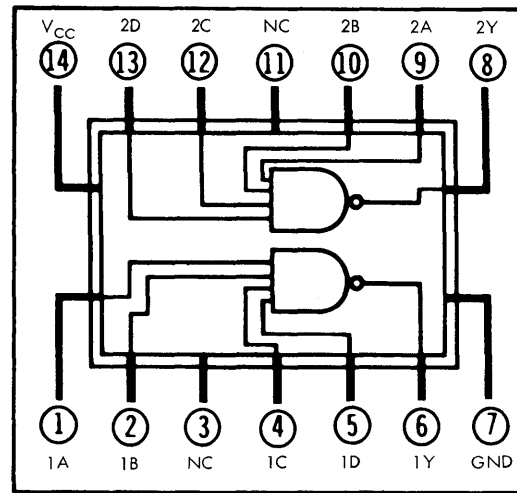


**PIN CONFIGURATIONS**

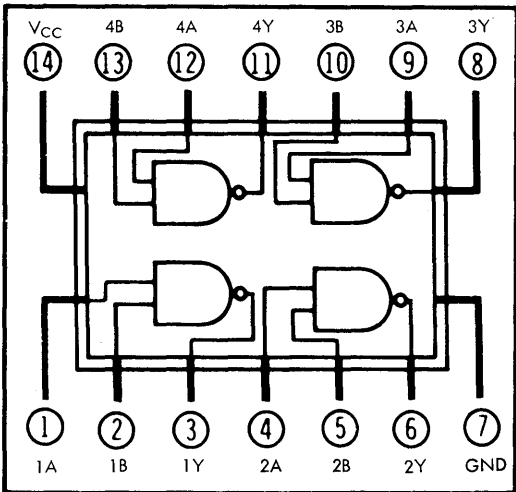
SN74 930  
DUAL 4-INPUT POSITIVE NAND GATE



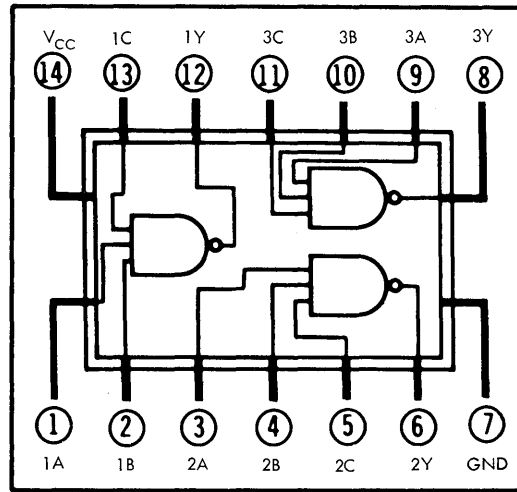
SN74 932  
DUAL 4-INPUT POSITIVE NAND BUFFER



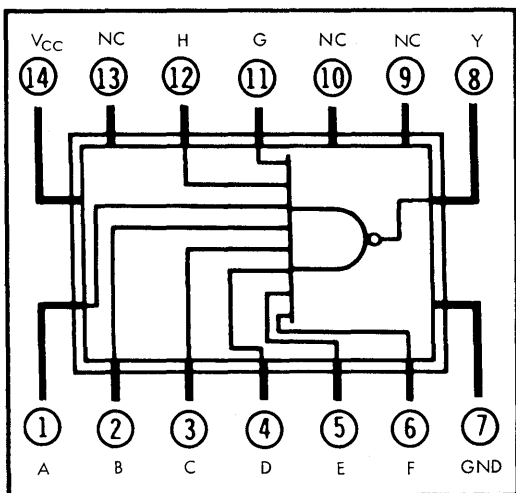
SN74 946  
QUADRUPLE 2-INPUT POSITIVE NAND GATE



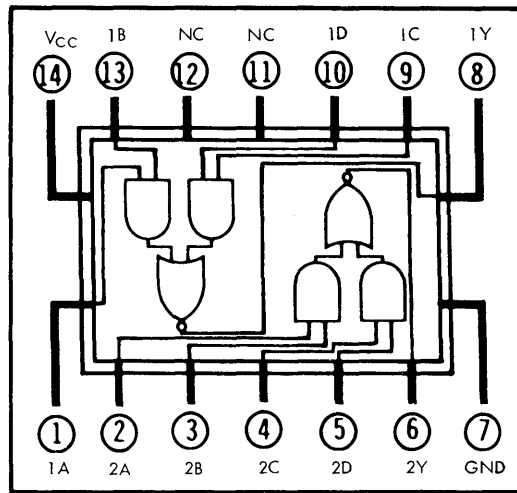
SN74 962  
TRIPLE 3-INPUT POSITIVE NAND GATE



SN74 965  
8-INPUT POSITIVE NAND GATE



SN74 966  
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE



# TYPE SN74 948

## MASTER-SLAVE FLIP-FLOP

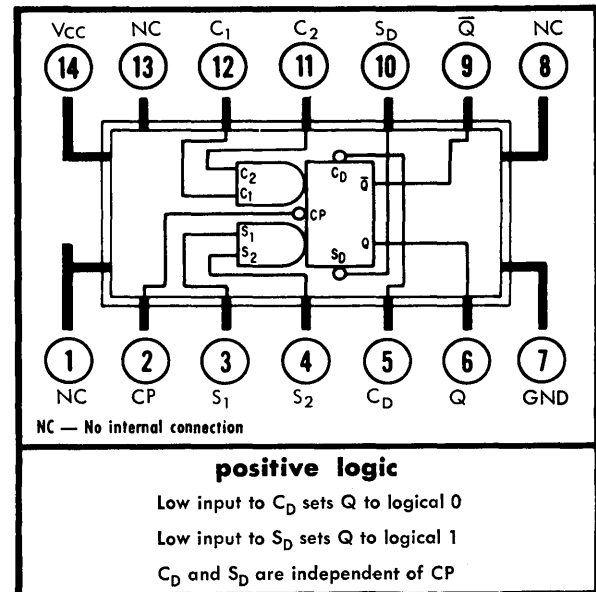
### logic

#### TRUTH TABLES

R-S MODE					
$t_n$				$t_{n+1}$	
$S_1$	$S_2$	$C_1$	$C_2$	Q	$\bar{Q}$
0	X	0	X	Qn	$\bar{Q}n$
0	X	X	0	Qn	$\bar{Q}n$
X	0	0	X	Qn	$\bar{Q}n$
X	0	X	0	Qn	$\bar{Q}n$
0	X	1	1	0	1
X	0	1	1	0	1
1	1	0	X	1	0
1	1	X	0	1	0
1	1	1	1	Indeterminate	Indeterminate

J-K MODE		
$t_n$	$t_{n+1}$	
$S_1$	$C_1$	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\bar{Q}n$

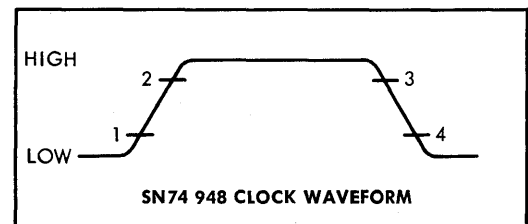
- NOTES: 1.  $t_n$  = bit time before clock pulse.  
 2.  $t_{n+1}$  = bit time after clock pulse.  
 3. X indicates that either a logical 1 or a logical 0 may be present.  
 4. Logical 1 is more positive than logical 0.  
 5. For operation in the J-K mode connect  $S_2$  to  $\bar{Q}$  and  $C_2$  to Q.



### description

The SN74 948 flip-flop is based on the master-slave principle. This device has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master.
2. Enter information from AND gate inputs to master.
3. Disable AND gate inputs.
4. Transfer information from master to slave.



### recommended operating conditions

Supply Voltage $V_{CC}$	4.75 V to 5.25 V
Fan-Out From Each Output, N	1 to 10
Width of Clock Pulse, $t_{p(\text{clock})}$ (See Figure 6)	$\geq 20$ ns
Width of Direct Set Pulse, $t_{p(\text{SD})}$ (See Figure 7)	$\geq 25$ ns
Width of Direct Clear Pulse, $t_{p(\text{CD})}$ (See Figure 7)	$\geq 25$ ns
Input Setup Time, $t_{\text{setup}}$ (See Figure 6)	applied clock pulse width
Input Hold Time, $t_{\text{hold}}$	$\geq 0$

# TYPE SN74 948

## MASTER-SLAVE FLIP-FLOP

electrical characteristics,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage	1	$V_{CC} = 4.75\text{ V}$	2			V
$V_{in(0)}$ Logical 0 input voltage	1	$V_{CC} = 4.75\text{ V}$			0.8	V
$V_{out(1)}$ Logical 1 output voltage	1	$V_{CC} = 4.75\text{ V}, I_{load} = -400\ \mu\text{A}$	2.4	3.5‡		V
$V_{out(0)}$ Logical 0 output voltage	2	$V_{CC} = 4.75\text{ V}, I_{sink} = 16\text{ mA}$		0.22‡	0.4	V
$I_{in(0)}$ Logical 0 level input current at $C_1, C_2, S_1,$ or $S_2$	3	$V_{CC} = 5.25\text{ V}, V_{in} = 0.4\text{ V}$			-1.6	mA
$I_{in(0)}$ Logical 0 level input current at $C_D$ or $S_D$	3	$V_{CC} = 5.25\text{ V}, V_{in} = 0.4\text{ V}$			-3.2	mA
$I_{in(0)}$ Logical 0 level input current at CP	3	$V_{CC} = 5.25\text{ V}, V_{in} = 0.4\text{ V}$			-4.8	mA
$I_{in(1)}$ Logical 1 level input current at $C_1, C_2, S_1,$ or $S_2$	4	$V_{CC} = 5.25\text{ V}, V_{in} = 2.4\text{ V}$			40	$\mu\text{A}$
		$V_{CC} = 5.25\text{ V}, V_{in} = 5.5\text{ V}$			1	mA
$I_{in(1)}$ Logical 1 level input current at $C_D$ or $S_D$	4	$V_{CC} = 5.25\text{ V}, V_{in} = 2.4\text{ V}$			80	$\mu\text{A}$
		$V_{CC} = 5.25\text{ V}, V_{in} = 5.5\text{ V}$			1	mA
$I_{in(1)}$ Logical 1 level input current at CP	4	$V_{CC} = 5.25\text{ V}, V_{in} = 2.4\text{ V}$			120	$\mu\text{A}$
		$V_{CC} = 5.25\text{ V}, V_{in} = 5.5\text{ V}$			1	mA
$I_{OS}$ Short-circuit output current †	5	$V_{CC} = 5.25\text{ V}, V_{in} = 0$	-18		-57	mA
$I_{CC}$ Supply current	4	$V_{CC} = 5\text{ V}, V_{in} = 5\text{ V}$		8		mA

† Not more than one output should be shorted at a time.

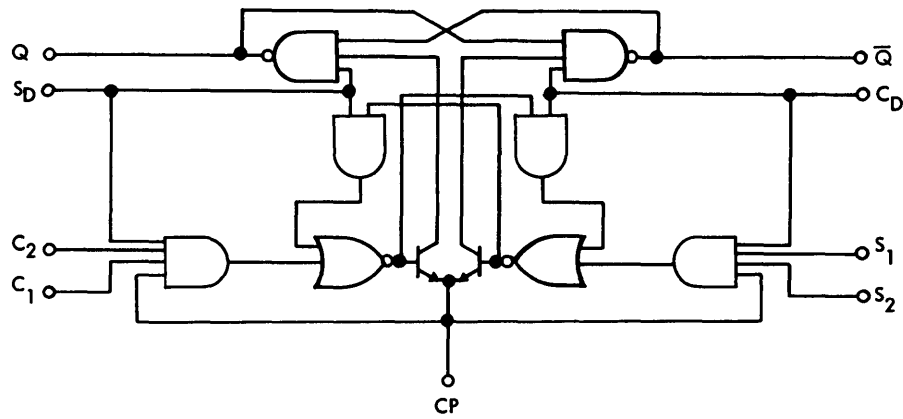
‡ These typical values are at  $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$ .

switching characteristics,  $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}, N = 10$

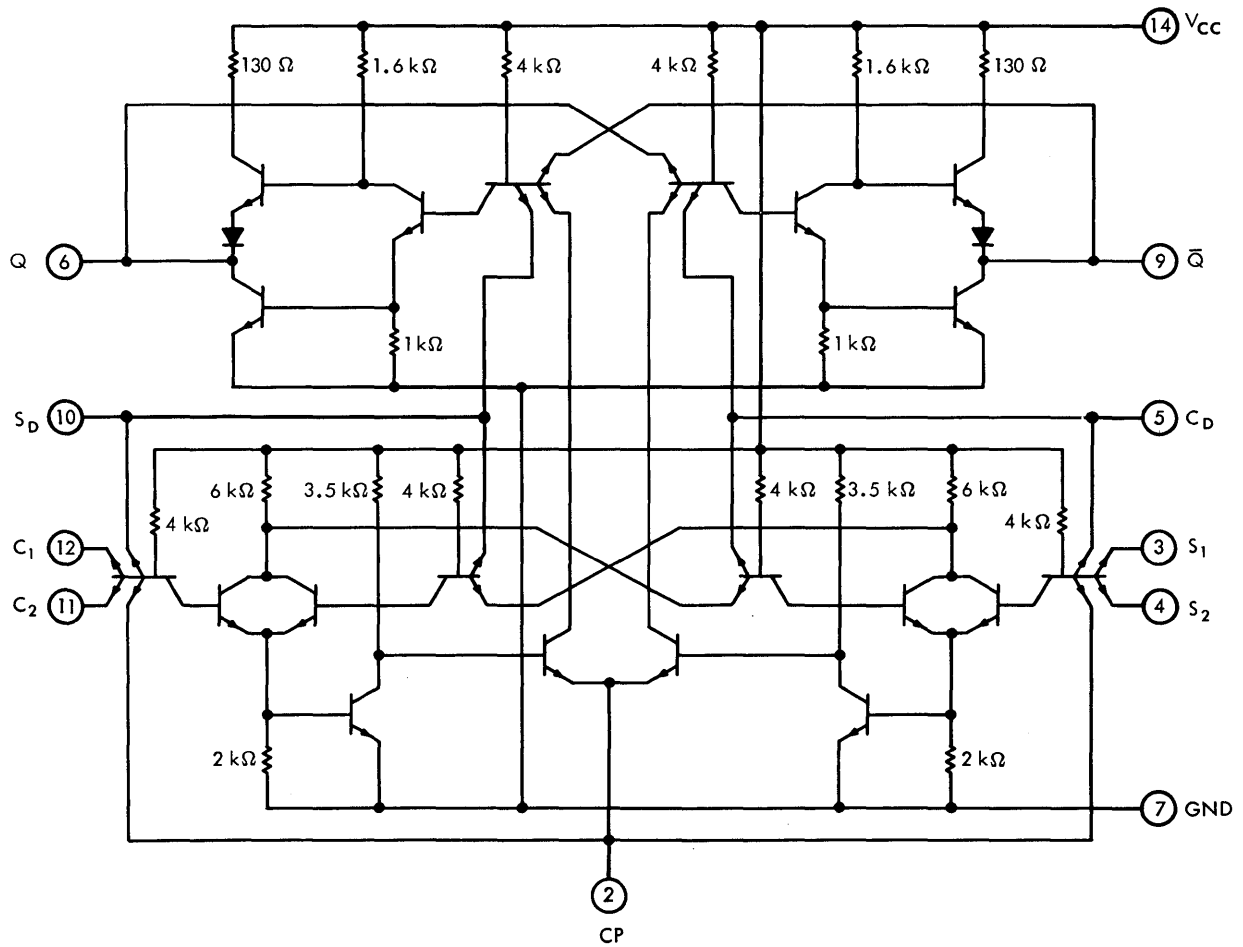
PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{clock}$ Maximum clock frequency	6		10	15		MHz
$t_{pd1}$ Propagation delay time to logical 1 level from $C_D$ or $S_D$ to output	7			26	50	ns
$t_{pd0}$ Propagation delay time to logical 0 level from $C_D$ or $S_D$ to output	7			34	50	ns
$t_{pd1}$ Propagation delay time to logical 1 level from $C_1, C_2, S_1,$ or $S_2$ to output	6		10	26	50	ns
$t_{pd0}$ Propagation delay time to logical 0 level from $C_1, C_2, S_1,$ or $S_2$ to output	6		10	34	50	ns

# TYPE SN74 948 MASTER-SLAVE FLIP-FLOP

functional block diagram



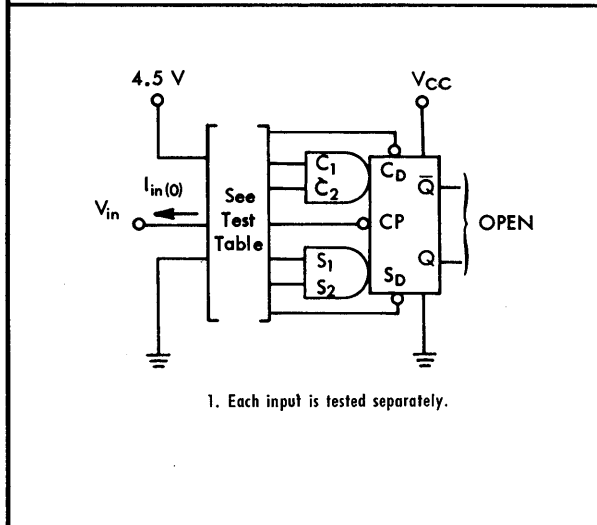
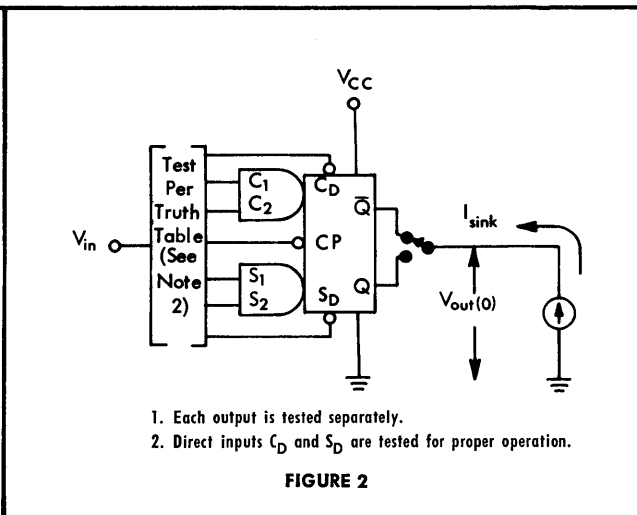
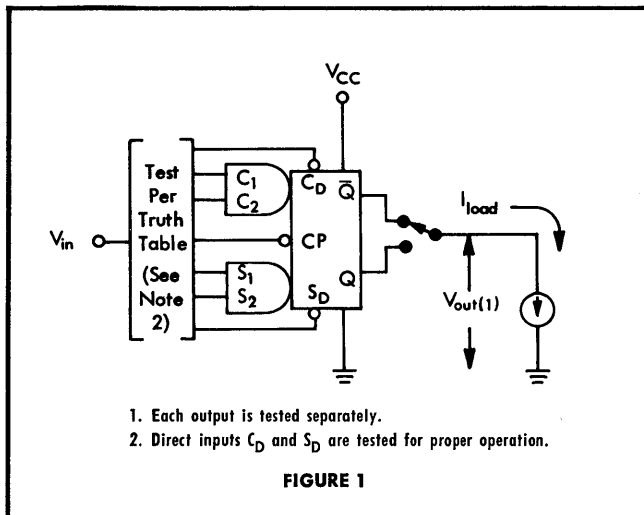
schematic



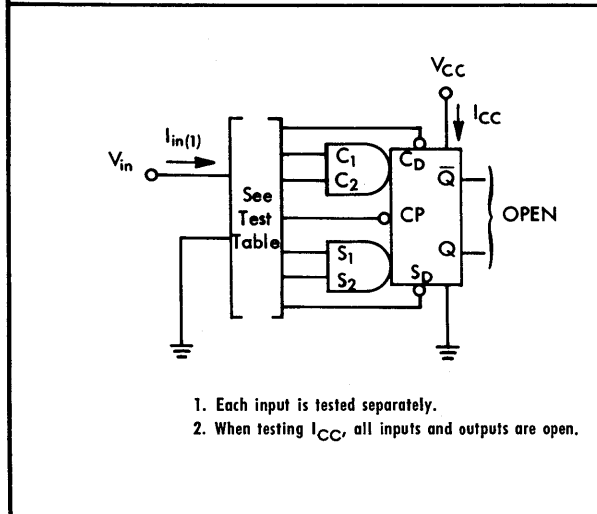
# TYPE SN74 948 MASTER-SLAVE FLIP-FLOP

## PARAMETER MEASUREMENT INFORMATION

### d-c test circuits†



TEST TABLE		
Apply $V_{in}$ (Test $I_{in}$ )	Apply Momentary GND, Then 4.5 V	Apply 4.5 V
CP	$C_D$	$C_1, C_2, S_1, S_2,$ and $S_D$
CP	$S_D$	$C_1, C_2, S_1, S_2,$ and $C_D$
$C_D$	None	$S_1, S_2,$ and CP
$S_D$	None	$C_1, C_2,$ and CP
$C_1$	None	$C_2, S_D,$ and CP
$C_2$	None	$C_1, S_D,$ and CP
$S_1$	None	$S_2, C_D,$ and CP
$S_2$	None	$S_1, C_D,$ and CP



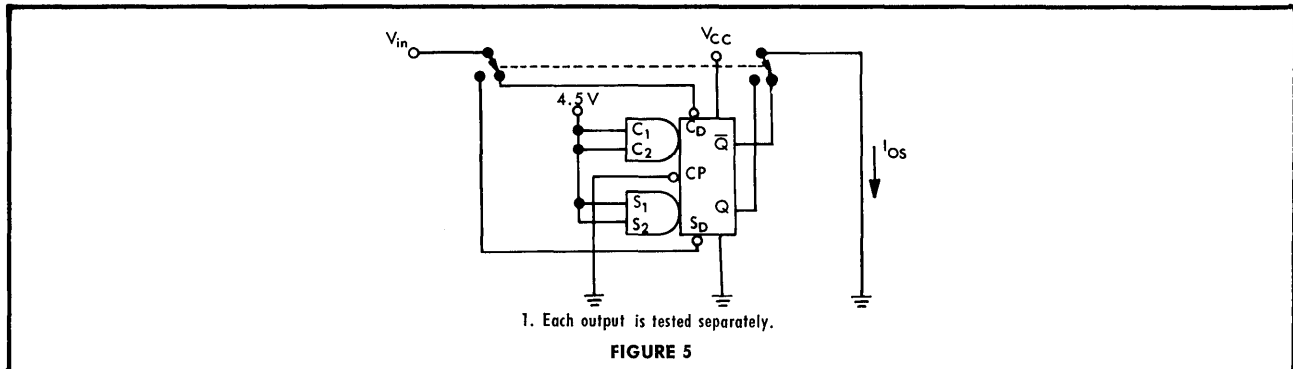
TEST TABLE	
Apply $V_{in}$ (Test $I_{in}$ )	Ground
CP	$C_D, S_D, C_1, C_2, S_1,$ and $S_2$
$C_D$	CP, $S_1,$ and $S_2$
$S_D$	CP, $C_1,$ and $C_2$
$C_1$	CP, $S_D,$ and $C_2$
$C_2$	CP, $S_D,$ and $C_1$
$S_1$	CP, $C_D,$ and $S_2$
$S_2$	CP, $C_D,$ and $S_1$

†Arrows indicate actual direction of current flow.

# TYPE SN74 948 MASTER-SLAVE FLIP-FLOP

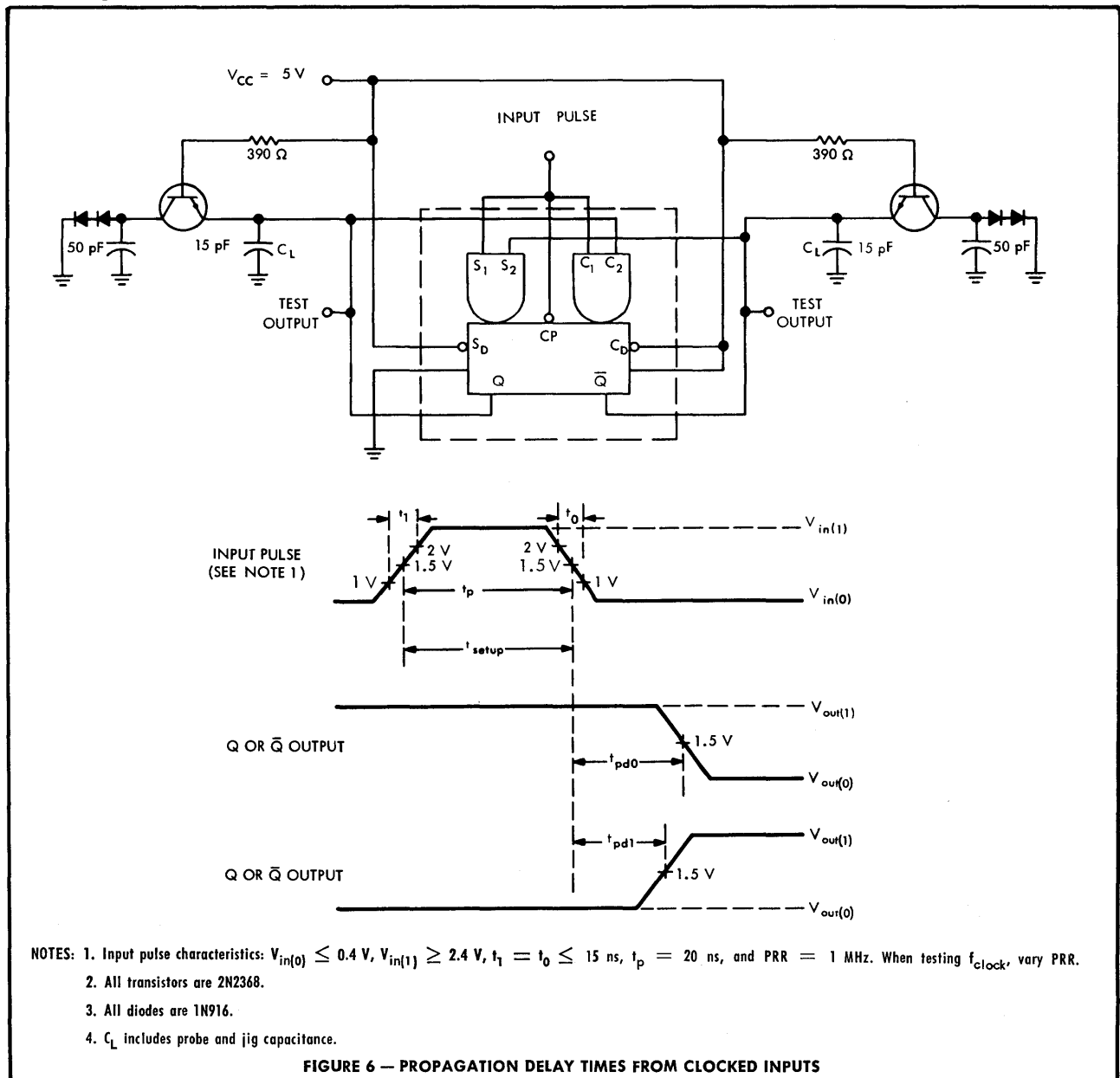
## PARAMETER MEASUREMENT INFORMATION

### d-c test circuits† (continued)



†Arrows indicate actual direction of current flow.

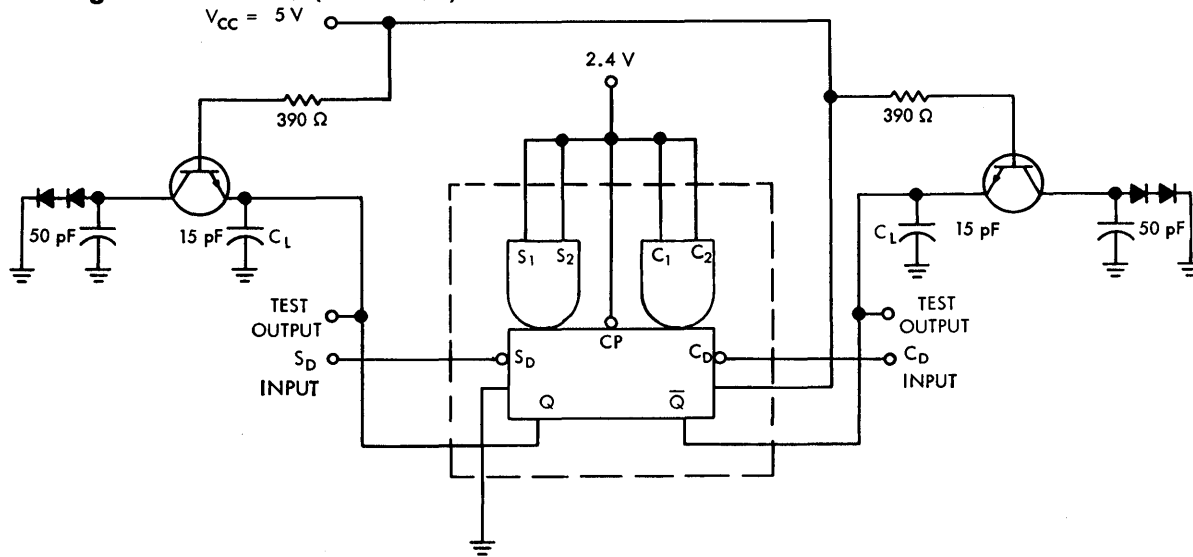
### switching characteristics



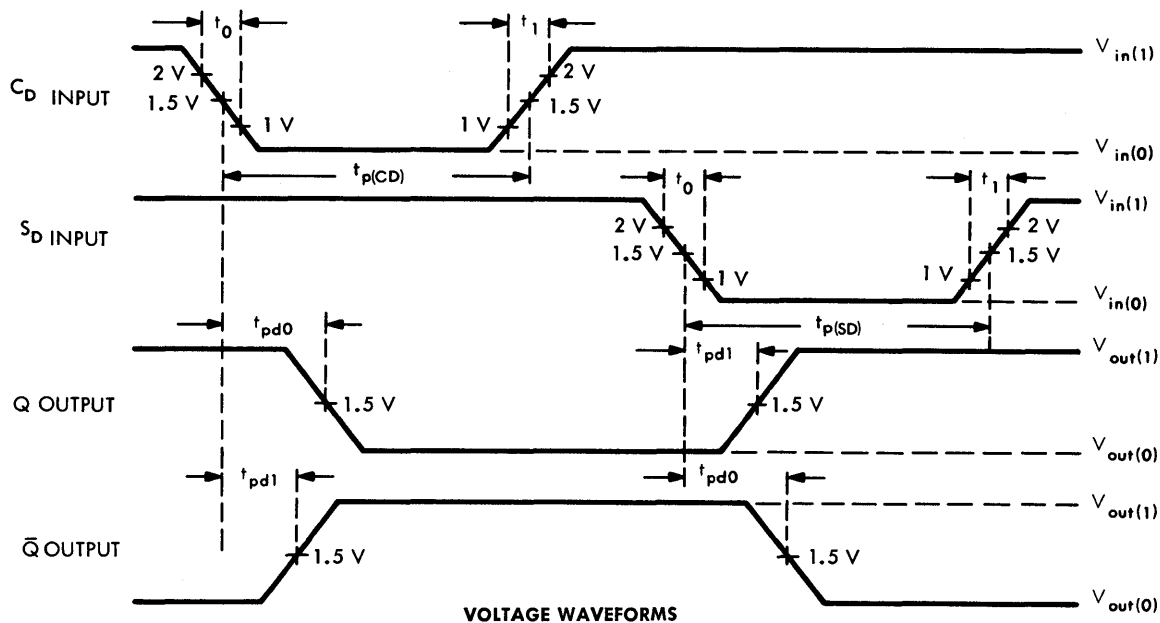


### PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: 1.  $C_D$  or  $S_D$  inputs dominate regardless of the state of clock,  $C_1$ ,  $C_2$  or  $S_1$ ,  $S_2$  inputs.  
 2.  $C_D$  or  $S_D$  input pulse characteristics:  $V_{in(0)} \leq 0.4 \text{ V}$ ,  $V_{in(1)} \geq 2.4 \text{ V}$ ,  $t_1 = t_0 \leq 15 \text{ ns}$ ,  $t_{p(CD)} = t_{p(SD)} = 25 \text{ ns}$ , and  $\text{PRR} = 1 \text{ MHz}$ .  
 3. All transistors are 2N2368.  
 4. All diodes are 1N916.  
 5.  $C_L$  includes probe and jig capacitance.

FIGURE 7 —  $C_D$  AND  $S_D$  PROPAGATION DELAY TIMES

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TI cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

TEXAS INSTRUMENTS RESERVES THE RIGHT TO MAKE CHANGES AT ANY TIME IN ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBLE.



**TRANSISTOR-TRANSISTOR-LOGIC SEMICONDUCTOR NETWORKS  
IN  
MOLDED PLUG-IN PACKAGES**

SERIES 74N  
BULLETIN NO. DL-S 668940, OCTOBER 1966

**description**

Series 74N consists of the Series 74 general-purpose TTL circuits mounted within a 14-pin plastic package and characterized for operation over the temperature range of 0°C to 70°C.

**features**

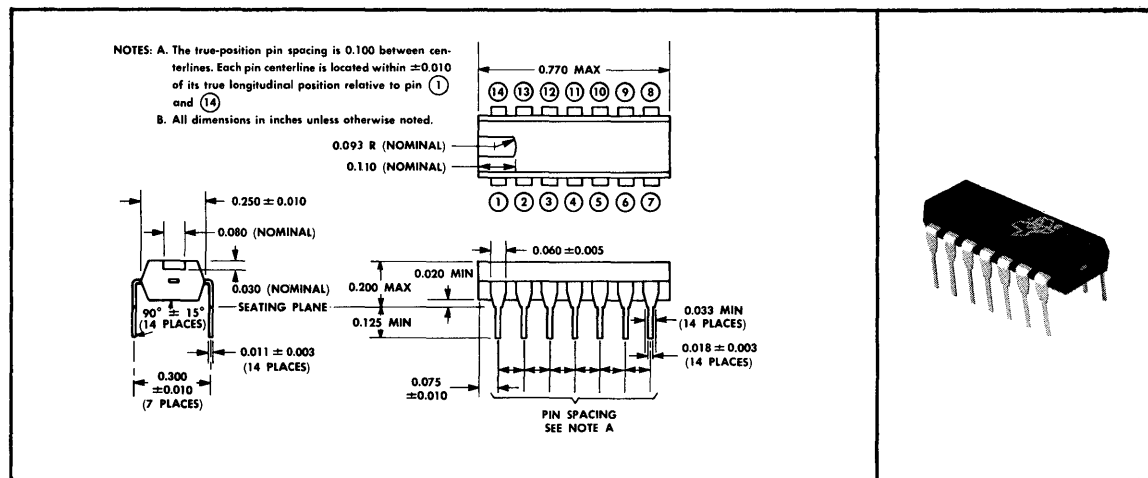
- high speed — typical gate propagation delay time of 13 ns
- high d-c noise margin — typically 1 V
- low power dissipation — 10 mW per gate at 50% duty cycle
- low output impedance — less than 100 Ω at logical 1 output state
- full fan-out of 10
- plug-in configuration ideal for flow-soldering techniques
- pins on 100-mil grid spacings for industrial-type circuit-boards

**specifications, logic symbols, and terminal designations**

Schematic diagrams, fan-out rules, maximum ratings, and electrical characteristics for Series 74N networks are identical to those of the corresponding Series 74 type number. Terminal designations for the Series 74N networks are shown in this data sheet.

**mechanical data**

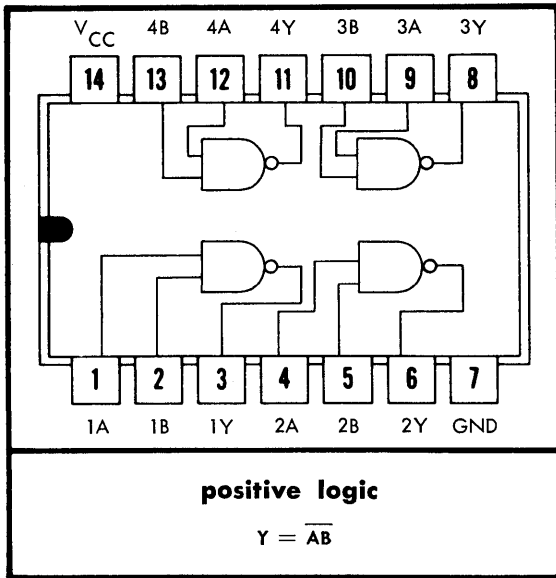
Series 74N networks are mounted on a 14-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions.



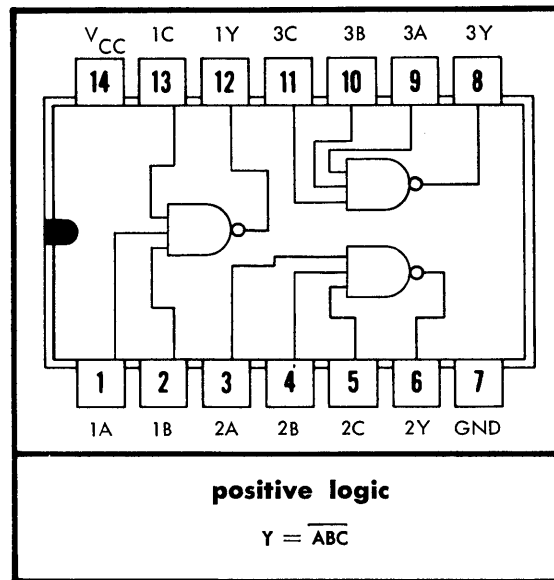
<sup>†</sup>Patented by Texas Instruments



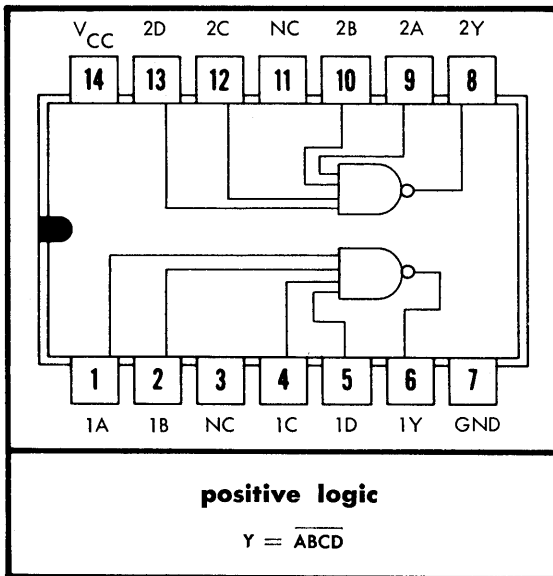
**SN7400N**  
QUADRUPLE 2-INPUT POSITIVE NAND GATE



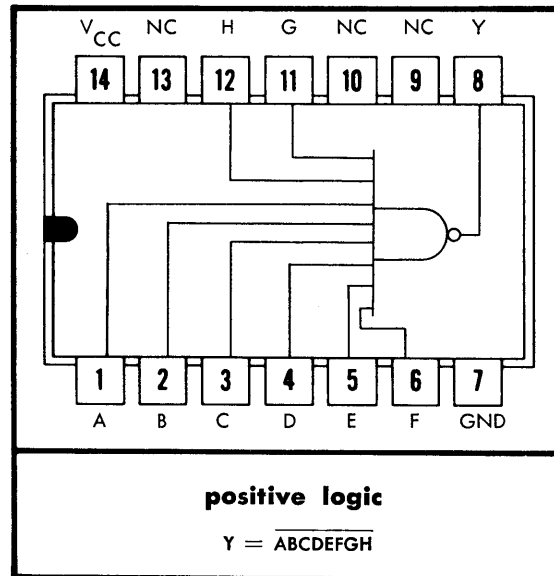
**SN7410N**  
TRIPLE 3-INPUT POSITIVE NAND GATE



**SN7420N**  
DUAL 4-INPUT POSITIVE NAND GATE

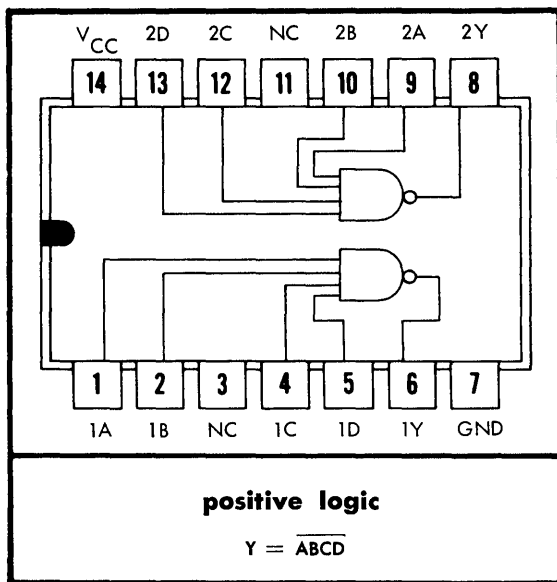


**SN7430N**  
8-INPUT POSITIVE NAND GATE

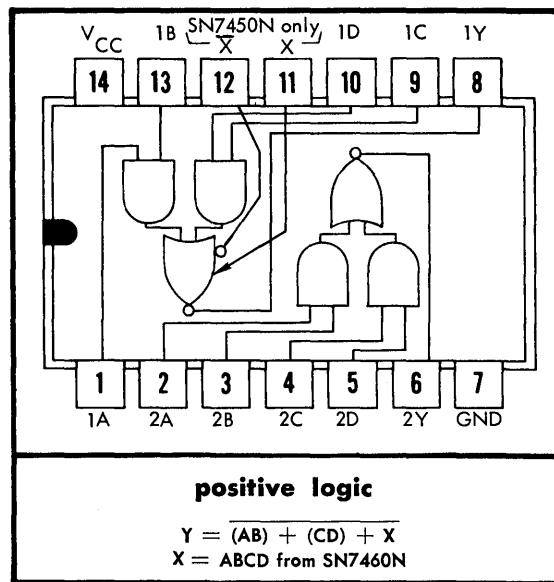


NC — No internal connection.  
†Patented by Texas Instruments

**SN7440N  
DUAL 4-INPUT POSITIVE NAND BUFFER**

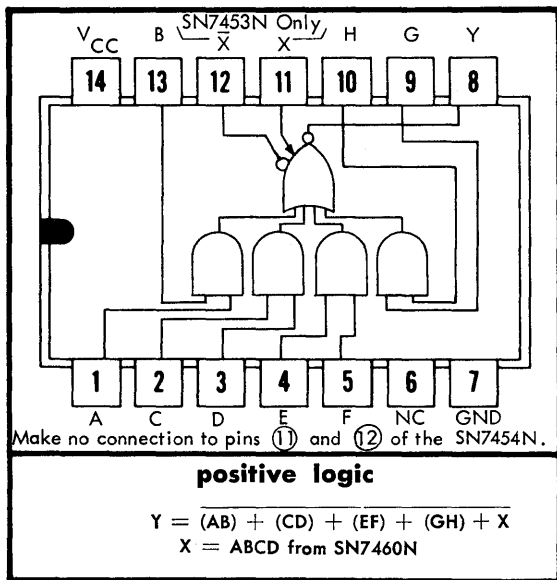


**SN7450N/SN7451N  
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES**



NOTE: Expander nodes X and  $\bar{X}$  are on the SN7450N only.  
Make no external connection to pins ⑪ and ⑫ of the SN7451N.

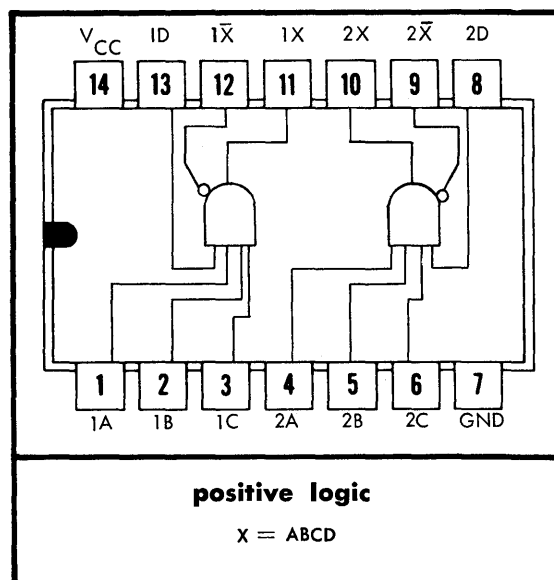
**SN7453N, SN7454N  
4-WIDE 2-INPUT AND-OR-INVERT GATES**



NOTE: Expander nodes X and  $\bar{X}$  are on the SN7453N only.

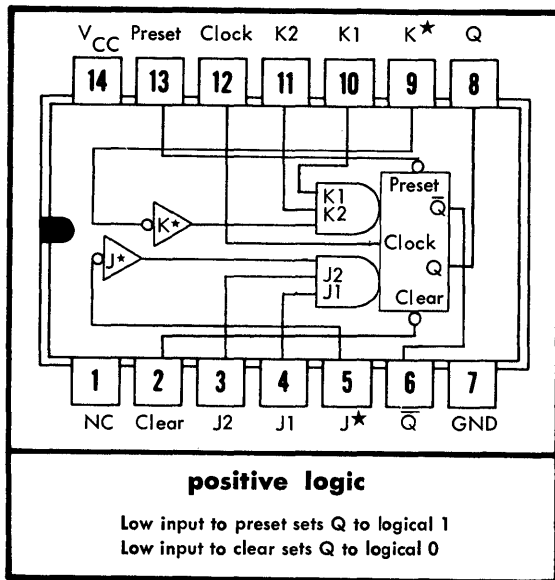
NC — No internal connection.  
†Patented by Texas Instruments

**SN7460N  
DUAL 4-INPUT EXPANDER**



NOTE: Connect pin ⑨ or ⑫ to pin ⑫ of SN7450N or SN7453N.  
Connect pin ⑩ or ⑪ to pin ⑪ of SN7450N or SN7453N.

**SN7470N  
J-K FLIP-FLOP**

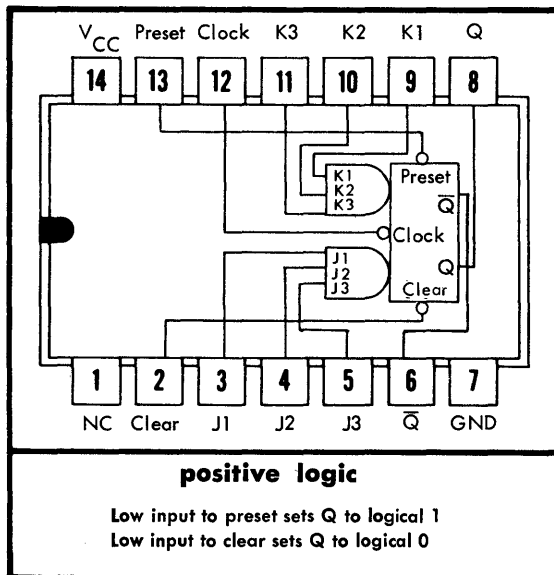


TRUTH TABLE		
$t_n$		$t_{n+1}$
J	K	Q
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\bar{Q}_n$

- NOTES: 1.  $J = J1 \cdot J2 \cdot J*$   
 2.  $K = K1 \cdot K2 \cdot K*$   
 3.  $t_n$  = bit time before clock pulse.  
 4.  $t_{n+1}$  = bit time after clock pulse.  
 5. If inputs  $J*$  or  $K*$  are not used they must be grounded.

NOTE: Clock must be at logical 0 prior to the application of preset or clear functions.

**SN7472N  
J-K MASTER-SLAVE FLIP-FLOP**

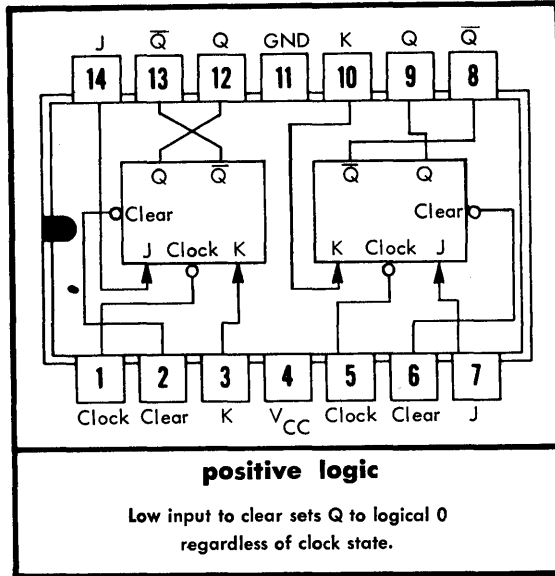


TRUTH TABLE		
$t_n$		$t_{n+1}$
J	K	Q
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\bar{Q}_n$

- NOTES: 1.  $J = J1 \cdot J2 \cdot J3$   
 2.  $K = K1 \cdot K2 \cdot K3$   
 3.  $t_n$  = bit time before clock pulse.  
 4.  $t_{n+1}$  = bit time after clock pulse.

NC — No internal connection.  
<sup>†</sup>Patented by Texas Instruments

**SN7473N**  
**DUAL J-K MASTER-SLAVE FLIP-FLOP**

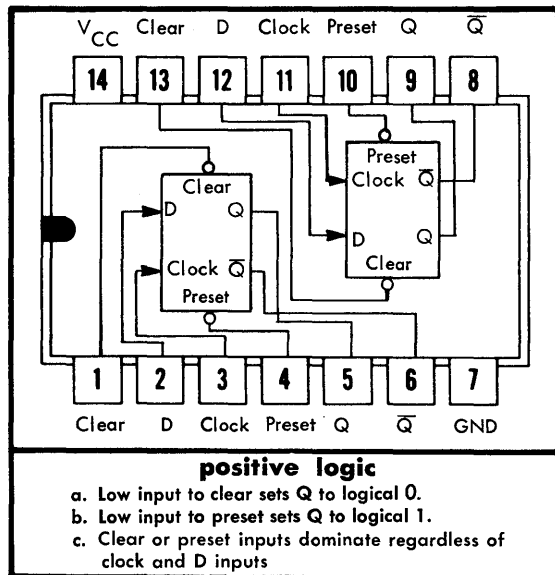


TRUTH TABLE (Each Flip-Flop)

$t_n$		$t_{n+1}$
J	K	Q
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1.  $t_n$  = bit time before clock pulse.  
2.  $t_{n+1}$  = bit time after clock pulse.

**SN7474N**  
**DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP**



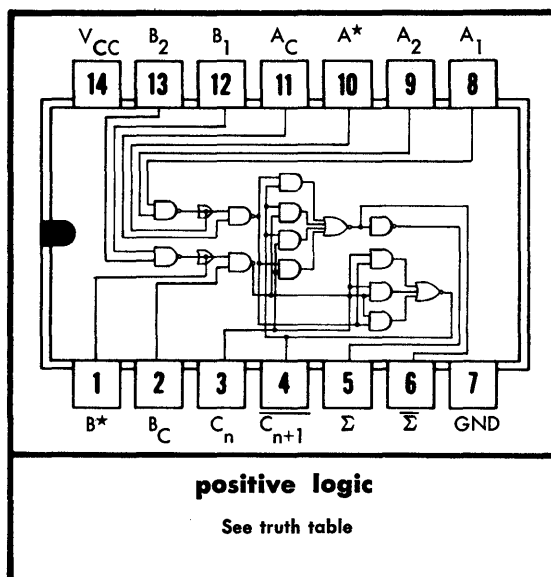
TRUTH TABLE (Each Flip-Flop)

$t_n$	$t_{n+1}$	
INPUT D	OUTPUT Q	OUTPUT $\bar{Q}$
0	0	1
1	1	0

NOTES: 1.  $t_n$  = bit time before clock pulse.  
2.  $t_{n+1}$  = bit time after clock pulse.

<sup>†</sup>Patented by Texas Instruments

**SN7480N**  
**GATED FULL ADDER**



**TRUTH TABLE**  
 (See Notes 1, 2, and 3)

$C_n$	B	A	$C_{n+1}$	$\Sigma$	$\bar{\Sigma}$
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

- NOTES: 1.  $A = \overline{A^* \cdot A_C}$ ,  $B = \overline{B^* \cdot B_C}$  where  $A^* = A_1 \cdot A_2$  and  $B^* = B_1 \cdot B_2$ .  
 2. When  $A^*$  or  $B^*$  are used as inputs,  $A_1$  and  $A_2$  or  $B_1$  and  $B_2$  respectively must be connected to GND.  
 3. When  $A_1$  and  $A_2$  or  $B_1$  and  $B_2$  are used as inputs,  $A^*$  or  $B^*$  respectively must be open, or used to perform Dot-OR logic.

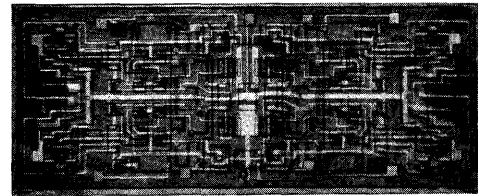
<sup>†</sup>Patented by Texas Instruments



### DIGITAL SEMICONDUCTOR NETWORKS FOR INDUSTRIAL APPLICATIONS

#### application

Series 73 semiconductor networks are ideally suited for general-purpose digital applications, including computer, data handling, and control systems. Series 73 is designed and characterized for use in environmental conditions found in industrial applications.



DUAL J-K FLIP-FLOP BAR

#### features

##### LOW SYSTEM COST

- multifunction devices offering lowest cost per logic function

##### ADVANCED PERFORMANCE

- optimum speed/power ratio for industrial applications
- guaranteed d-c margin
- high a-c noise rejection from low output impedance
- waveshape integrity maintained over rated temperature and loading conditions by double-ended output stage

##### EASE OF DESIGN

- most complete industrial family available — 14 networks
- modified DTL circuitry simplifies system design
- fan-out of 10 from each output

#### description

Series 73 is a compatible line of digital semiconductor networks capable of performing all basic and some special logic functions. All basic logic functions are offered as multi-function networks. Utilization of this complete line of compatible networks reduces systems engineering design time, while the use of multi-function networks reduces system cost per logic function.

Series 73 logic employs a modified form of diode-transistor logic (DTL) where transistors replace conventional diodes in order to improve circuit performance. Input transistors improve drive capability while offset transistors improve switching speed. The Series 73 low-impedance output stage maintains symmetrical waveshapes over wide ranges of d-c fan-out, capacitive loads, and operating temperatures. The low-impedance output also provides for a high degree of protection against capacitively coupled noise transients on system information lines.

CONTENTS	Page
DESIGN CHARACTERISTICS AND LOGIC SYMBOLS . . . . .	6502-6503
LOADING TABLES . . . . .	6504
DEFINITIVE SPECIFICATIONS . . . . .	6505-6524
D-C TEST CIRCUITS . . . . .	6525-6528
SWITCHING TIME TEST CIRCUITS AND VOLTAGE WAVEFORMS . . . . .	6529-6531
MECHANICAL AND PACKAGING DATA . . . . .	6532

<sup>†</sup>Patented by Texas Instruments

SERIES 73  
 BULLETIN NO. DL-S 669019, OCTOBER 1966  
 REPLACES BULLETIN NO. DL-S 657650, JULY 1965





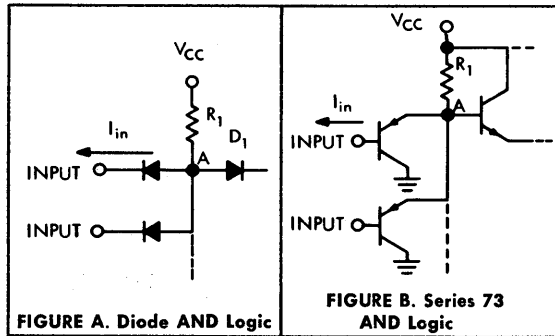
typical operating characteristics,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ , supply voltage  $V_{CC} = 3\text{ v}$  to  $4\text{ v}$

Speed: Gate Propagation Delay . . . . .	35 nsec
Flip-flop Toggle Rate . . . . .	4 Mc
Fan-Out Capability of Each Output . . . . .	10
Fan-In With Expanders . . . . .	25 max
D-C Margin: At Logical 1 . . . . .	300 mv
At Logical 0 . . . . .	200 mv
Output Impedance . . . . .	< 50 $\Omega$
Average Power Dissipation: Per Gate . . . . .	12 mw
Per Flip-flop . . . . .	40 mw

**design characteristics**

Series 73 is a compatible line of digital semiconductor integrated circuits built and characterized for medium-speed applications (up to 4 Mc) in industrial environments. The networks are fabricated from triple-diffused planar silicon, and employ a modified form of diode-transistor logic selected to take advantage of inherent integrated-circuit characteristics.

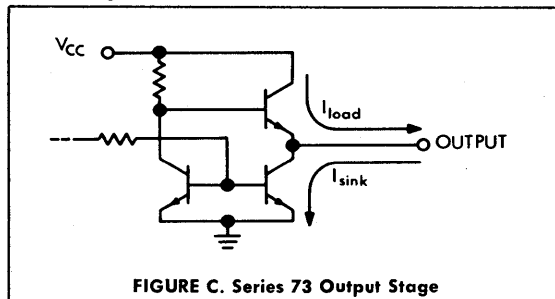
As in conventional diode logic (Figure A), logic is performed at node A of a Series 73 gate (Figure B).



The gain of the p-n-p transistors replacing the input diodes increases the effective drive capability of the preceding stage. The voltage at node A is now a function of  $I_{in}$ ,  $R_1$ , and the p-n-p transistor gain, rather than only  $I_{in}$  and  $R_1$  as in diode logic. The effect of the transistor gain is to minimize the importance of the resistor value in the circuit's performance. Since silicon resistors have inherently wide production tolerances and high temperature coefficients, the transistor gain makes fabrication of Series 73 networks more economical while assuring greater stability over the temperature range.

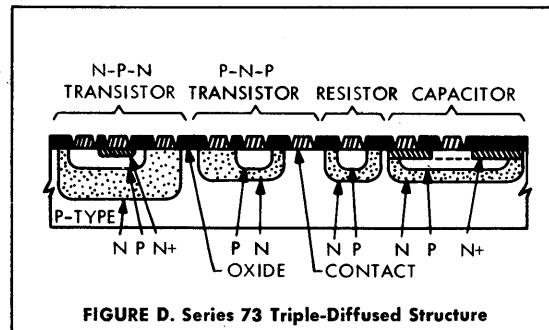
The n-p-n transistor which replaces the offset diode  $D_1$ , also has gain, increasing the circuit drive capability and improving the waveshapes at node A.

This basic AND logic configuration is coupled with an inverting double-ended output stage (Figure C) in each Series 73 gate.

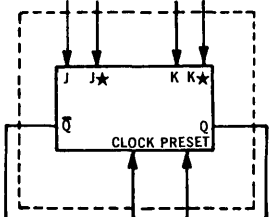
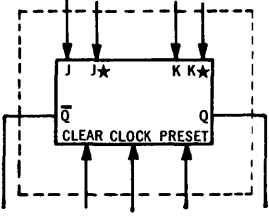
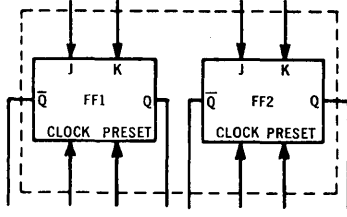
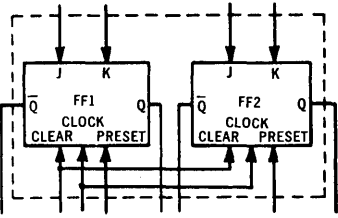
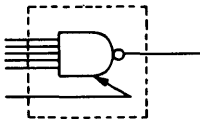
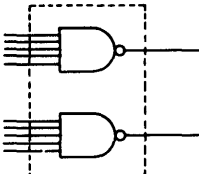
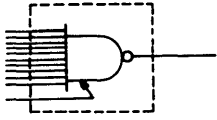
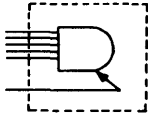
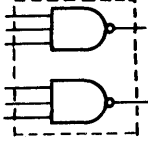
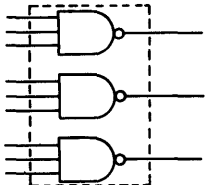
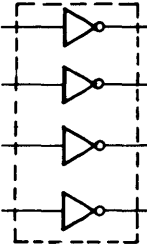
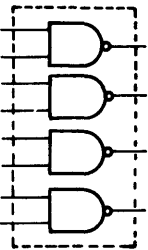
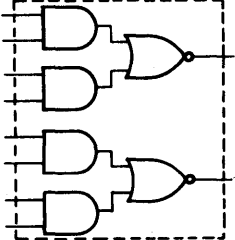
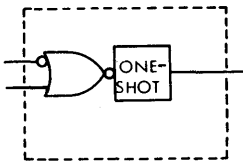


The most important feature of the Series 73 output stage is its ability to supply load and sink current with low output impedance. This provides high d-c fan-out to both types of loads and simplifies interface design. Low output impedance in either state ensures that turn-on and turn-off waveshapes will remain sharp and symmetrical over a wide range of d-c and capacitive loadings throughout the temperature range. The low output impedance of each output ensures that every information line will have a low-impedance termination, providing valuable protection against a-c coupled noise transients.

All Series 73 networks are fabricated using a 4-step planar diffusion process. First, an n-type diffusion is made in the p-type substrate, forming the n-p-n collectors only. A second n-type diffusion is made forming the base area of the p-n-p transistors, isolation region of the resistors, one section of the capacitors, and further forming the n-p-n collectors. This sequence reduces the n-p-n transistor  $r_{CE(sat)}$  to approximately 30 ohms, while keeping the p-n-p base width narrow and the gain high (typically 12). The next step is a p-type diffusion which forms the p-n-p emitters, n-p-n bases, resistors, and another portion of the capacitors. The final diffusion is an n-type, forming the n-p-n emitters and completing the capacitors.



standard line summary

<p><b>SN7300</b> See Page 6505</p>  <p><b>J-K FLIP-FLOP WITH PRESET</b></p>	<p><b>SN7301</b> See Page 6507</p>  <p><b>J-K FLIP-FLOP WITH PRESET AND CLEAR</b></p>	<p><b>SN7302</b> See Page 6509</p>  <p><b>DUAL J-K FLIP-FLOP WITH PRESET</b></p>
<p><b>SN7304</b> See Page 6511</p>  <p><b>DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR</b></p>	<p><b>SN7310</b> See Page 6513</p>  <p><b>5-INPUT EXPANDABLE NAND/NOR GATE</b></p>	<p><b>SN7311</b> See Page 6515</p>  <p><b>DUAL 5-INPUT NAND/NOR GATE</b></p>
<p><b>SN7315</b> See Page 6516</p>  <p><b>10-INPUT EXPANDABLE NAND/NOR GATE</b></p>	<p><b>SN7320</b> See Page 6517</p>  <p><b>5-INPUT EXPANDER</b></p>	<p><b>SN7330</b> See Page 6518</p>  <p><b>DUAL 3-INPUT NAND/NOR GATE</b></p>
<p><b>SN7331</b> See Page 6519</p>  <p><b>TRIPLE 3-INPUT NAND/NOR GATE</b></p>	<p><b>SN7350</b> See Page 6520</p>  <p><b>QUADRUPLE INVERTER/DRIVER</b></p>	<p><b>SN7360</b> See Page 6521</p>  <p><b>QUADRUPLE 2-INPUT NAND/NOR GATE</b></p>
<p><b>SN7370</b> See Page 6522</p>  <p><b>DUAL AND-OR-INVERT GATE</b></p>		<p><b>SN7380</b> See Page 6523</p>  <p><b>ONE-SHOT MONOSTABLE MULTIVIBRATOR</b></p>

# SERIES 73

# SOLID CIRCUIT<sup>®</sup> SEMICONDUCTOR NETWORKS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage, $V_{CC}$ (See Note 1) . . . . .	+7 v
Input Voltage, $V_{in}$ (See Notes 1 and 2) . . . . .	$V_{CC}$
Operating Free-Air Temperature Range . . . . .	0°C to 70°C
Storage Temperature Range . . . . .	-65°C to 125°C

- NOTES: 1. Voltage values are with respect to network ground terminal.  
 2. Input signals must be zero or positive with respect to network ground terminal.

### logic definition

Series 73 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE = LOGICAL 0  
 HIGH VOLTAGE = LOGICAL 1

### input current requirements

Weighted values of input current requirements reflect worst-case conditions for  $T_A = 0^\circ$  to  $70^\circ\text{C}$  and  $V_{CC} = 3$  to  $4$  v. One positive load ( $N+ = 1$ ) requires current into the input at a logical 1 voltage level (0.5 ma at  $V_{CC} = 3$  v, and 0.8 ma at  $V_{CC} = 4$  v). One negative load ( $N- = 1$ ) requires current out of the input at a logical 0 voltage level (-0.2 ma). Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

WEIGHTED VALUES OF INPUT CURRENT REQUIREMENTS				
NETWORK	TYPE	INPUT	N+ LOADS	N- LOADS
FLIP-FLOPS	7300, 7301 7302	J, J*, K, K*, Preset, Clear	1	0
		Clock	2.5	2.5
	7304	J, K, Preset	1	0
		Clear Clock	2 5	0 5
GATES AND EXPANDER	7310, 7311 7315, 7320 7330, 7331 7360, 7370	Each Input	0	1
ONE-SHOT	7380	T, T*	1	0
INVERTER	7350	Each Input	2	0

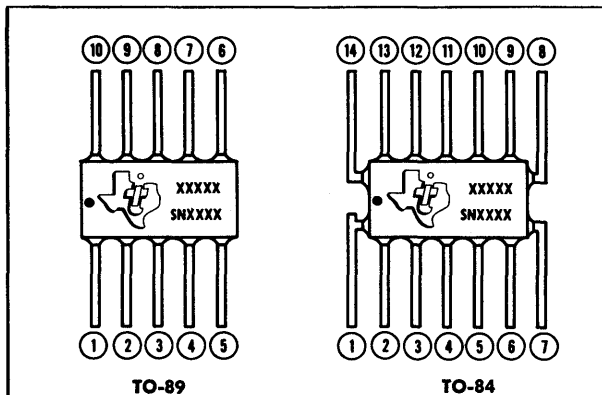
### output drive capability

Weighted values of fan-out reflect the ability of an output to drive current to  $N+$  loads and sink current from  $N-$  loads under worst-case conditions. Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuits indicate the actual direction of current flow.

WEIGHTED VALUES OF FAN-OUT			
NETWORK	OUTPUT	N+ LOADS	N- LOADS
FLIP-FLOPS, GATES, AND ONE-SHOT	Each Output	10	10
	Each Output	10	10
INVERTER (SN7350)	4 Inverters in parallel	40	40

### pin identification

Pin identification for Series 73 networks is shown in the illustration at the right. Symbolization on package denotes orientation. For dimensions see mechanical data.



# TYPE SN7300

## J-K FLIP-FLOP WITH PRESET

### logic

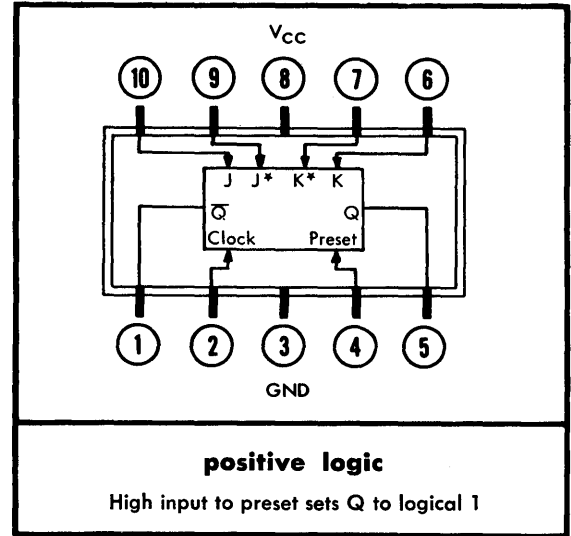
#### TRUTH TABLES

J★=K★=1		
$t_n$		$t_{n+1}$
J	K	Q
0	0	Q <sub>n</sub>
0	1	0
1	0	1
1	1	$\overline{Q}_n$

J=K=0		
$t_n$		$t_{n+1}$
J★	K★	Q
0	0	Q <sub>n</sub>
0	1	1
1	0	0
1	1	Q <sub>n</sub>

ADDITIONAL INPUT LOGIC COMBINATIONS				
$t_n$				$t_{n+1}$
J	K	J★	K★	Q
0	1	0	0	Q <sub>n</sub>
1	0	0	0	$\overline{Q}_n$
1	1	0	0	Q <sub>n</sub>
0	1	0	1	Q <sub>n</sub>
1	1	0	1	$\overline{Q}_n$
1	0	1	0	$\overline{Q}_n$
1	1	1	0	$\overline{Q}_n$
1	0	0	1	1
0	1	1	0	0

$t_n$  = Bit time before clock pulse  
 $t_{n+1}$  = Bit time after clock pulse



#### recommended operating conditions

Supply Voltage, $V_{CC}$	3 v to 4 v
Maximum Fan-out From Each Output Into Positive Loads, $N_+$	10
Maximum Fan-out From Each Output Into Negative Loads, $N_-$	10
Fall Time of Clock Pulse, $t_{f(\text{clock})}$	20 to 150 nsec
Minimum Width of Clock Pulse, $t_{p(\text{clock})}$	50 nsec

#### electrical characteristics (unless otherwise noted $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ , $V_{CC} = 3\text{ v}$ to $4\text{ v}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at J, K, J★, K★, and preset inputs	1	$V_{CC}=3\text{ v}$	1.7		3	v
		$V_{CC}=4\text{ v}$	2.4		4	v
$V_{in(1)}$ Input voltage required to ensure logical 1 at clock input	2	$V_{CC}=3\text{ v}$	1.5		3	v
		$V_{CC}=4\text{ v}$	2.2		4	v
$V_{in(0)}$ Input voltage required to ensure logical 0 at J, K, J★, K★, preset, and clock inputs	1, 2		0		0.4	v
$V_{out(1)}$ Logical 1 output voltage (off level)	3	$V_{CC}=3\text{ v}$ , $N_+=10$ ( $I_{load}=-5\text{ ma}$ )	1.7			v
		$V_{CC}=4\text{ v}$ , $N_+=10$ ( $I_{load}=-8\text{ ma}$ )	2.6			v
$V_{out(0)}$ Logical 0 output voltage (on level)	3	$V_{CC}=3\text{ v}$ , $N_-=10$ ( $I_{sink}=2\text{ ma}$ )			0.3	v
		$V_{CC}=4\text{ v}$ , $N_-=10$ ( $I_{sink}=2\text{ ma}$ )			0.3	v
$I_{in}$ J, K, J★, K★, and preset input current	3	$V_{in}=1.7\text{ v}$			0.5	ma
		$V_{in}=2.6\text{ v}$			0.8	ma
$I_{in}$ Clock input current	3	$V_{in}=1.7\text{ v}$			1.25	ma
		$V_{in}=2.4\text{ v}$			2	ma
		$V_{in}=0.3\text{ v}$			-0.5	ma
$I_{CC(av)}$ Average supply current	4	$V_{CC}=3\text{ v}$ , $N_+=N_-=0$ , Toggle=1 Mc, $T_A=25^\circ\text{C}$		9		ma
		$V_{CC}=4\text{ v}$ , $N_+=N_-=0$ , Toggle=1 Mc, $T_A=25^\circ\text{C}$		13		ma

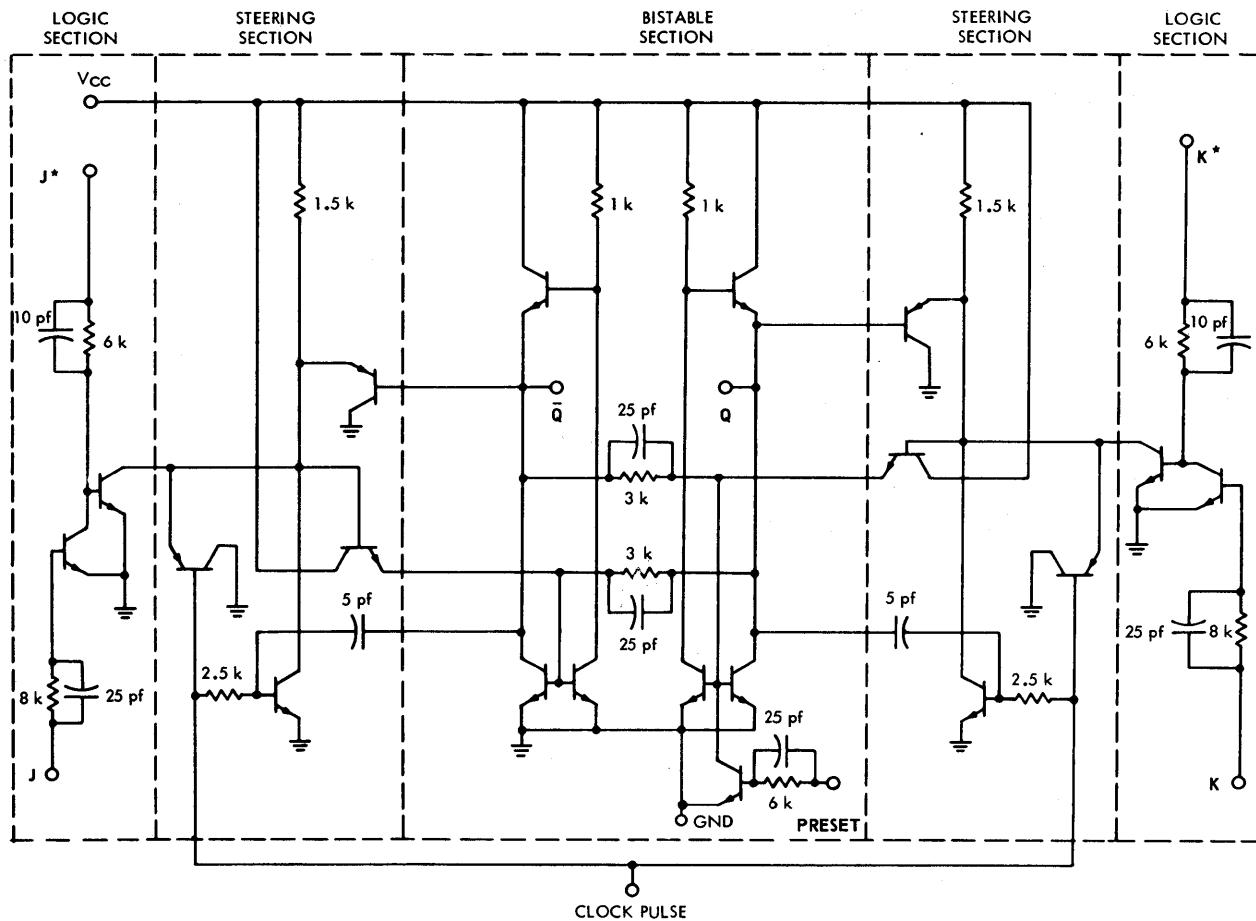
# TYPE SN7300

## J-K FLIP-FLOP WITH PRESET

switching characteristics,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ v}$ ,  $N+ = N- = 0$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$ Delay Time	19	Clock Input: $V_{in} = 2.5\text{ v}$ , $t_f = 20\text{ nsec}$ , $t_p = 500\text{ nsec}$ , $f = 1\text{ Mc}$ J, J*, K and K* Input: $V_{in} = V_{CC}$ Preset Input: $V_{in} = 0$	20	30	nsec
$t_r$ Rise Time			20	45	nsec
$t_s$ Storage Time			40	60	nsec
$t_f$ Fall Time			25	40	nsec
$t_{set(1)}$ Time to Set a Logical 1: J or K J* or K*	20	Clock Input: $V_{in} = 2.5\text{ v}$ , $t_f = 20\text{ nsec}$ , $t_p = 500\text{ nsec}$ , $f = 1\text{ Mc}$ J, J*, K or K* Input: $V_{in(1)} = 2.5\text{ v}$ , $V_{in(0)} = 0$ , $t_r = t_f = 50\text{ nsec}$	50		nsec
$t_{set(0)}$ Time to Set a Logical 0: J or K J* or K*			35		nsec
$t_{preset}$ Preset Time	21	Clock Input: $V_{in} = 0$ Preset Input: $V_{in} = 2.5\text{ v}$ , $t_f = 50\text{ nsec}$	55		nsec

### schematic



NOTES: a. Component values shown are nominal.  
b. Resistor values are in ohms.

# TYPE SN7301 J-K FLIP-FLOP WITH PRESET AND CLEAR

## logic

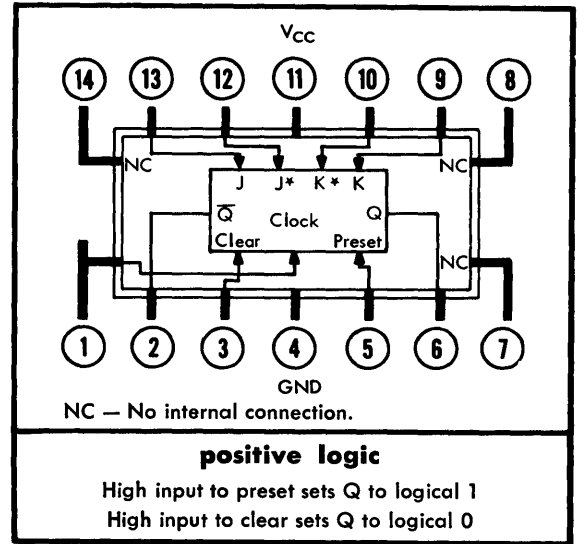
TRUTH TABLES

J★=K★=1		
J	K	Q
0	0	Q <sub>n</sub>
0	1	0
1	0	1
1	1	$\overline{Q}_n$

J=K=0		
J★	K★	Q
0	0	Q <sub>n</sub>
0	1	1
1	0	0
1	1	Q <sub>n</sub>

ADDITIONAL INPUT LOGIC COMBINATIONS				
J	K	J★	K★	Q
0	1	0	0	Q <sub>n</sub>
1	0	0	0	$\overline{Q}_n$
1	1	0	0	$\overline{Q}_n$
0	1	0	1	$\overline{Q}_n$
1	1	0	1	$\overline{Q}_n$
1	0	1	0	$\overline{Q}_n$
1	1	1	0	$\overline{Q}_n$
1	0	0	1	1
0	1	1	0	0

$t_n$  = Bit time before clock pulse  
 $t_{n+1}$  = Bit time after clock pulse



### recommended operating conditions

Supply Voltage, V <sub>CC</sub>	3 v to 4 v
Maximum Fan-out From Each Output Into Positive Loads, N <sup>+</sup>	10
Maximum Fan-out From Each Output Into Negative Loads, N <sup>-</sup>	10
Fall Time of Clock Pulse, $t_{f(\text{clock})}$	20 to 150 nsec
Minimum Width of Clock Pulse, $t_{p(\text{clock})}$	50 nsec

### electrical characteristics (unless otherwise noted T<sub>A</sub> = 0°C to 70°C, V<sub>CC</sub> = 3 v to 4 v)

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>in(1)</sub> Input voltage required to ensure logical 1 at J, K, J★, K★, preset, and clear inputs	1	V <sub>CC</sub> = 3 v	1.7		3	v
		V <sub>CC</sub> = 4 v	2.4		4	v
V <sub>in(1)</sub> Input voltage required to ensure logical 1 at clock input	2	V <sub>CC</sub> = 3 v	1.5		3	v
		V <sub>CC</sub> = 4 v	2.2		4	v
V <sub>in(0)</sub> Input voltage required to ensure logical 0 at J, K, J★, K★, preset, clock, and clear inputs	1, 2		0		0.4	v
V <sub>out(1)</sub> Logical 1 output voltage (off level)	3	V <sub>CC</sub> = 3 v, N <sup>+</sup> = 10 (I <sub>load</sub> = -5 ma)	1.7			v
		V <sub>CC</sub> = 4 v, N <sup>+</sup> = 10 (I <sub>load</sub> = -8 ma)	2.6			v
V <sub>out(0)</sub> Logical 0 output voltage (on level)	3	V <sub>CC</sub> = 3 v, N <sup>-</sup> = 10 (I <sub>sink</sub> = 2 ma)			0.3	v
		V <sub>CC</sub> = 4 v, N <sup>-</sup> = 10 (I <sub>sink</sub> = 2 ma)			0.3	v
I <sub>in</sub> J, K, J★, K★, preset, and clear input current	3	V <sub>in</sub> = 1.7 v			0.5	ma
		V <sub>in</sub> = 2.6 v			0.8	ma
I <sub>in</sub> Clock input current	3	V <sub>in</sub> = 1.7 v			1.25	ma
		V <sub>in</sub> = 2.4 v			2	ma
		V <sub>in</sub> = 0.3 v			-0.5	ma
I <sub>CC(av)</sub> Average supply current	4	V <sub>CC</sub> = 3 v, N <sup>+</sup> = N <sup>-</sup> = 0, Toggle = 1 Mc, T <sub>A</sub> = 25°C		9		ma
		V <sub>CC</sub> = 4 v, N <sup>+</sup> = N <sup>-</sup> = 0, Toggle = 1 Mc, T <sub>A</sub> = 25°C		13		ma

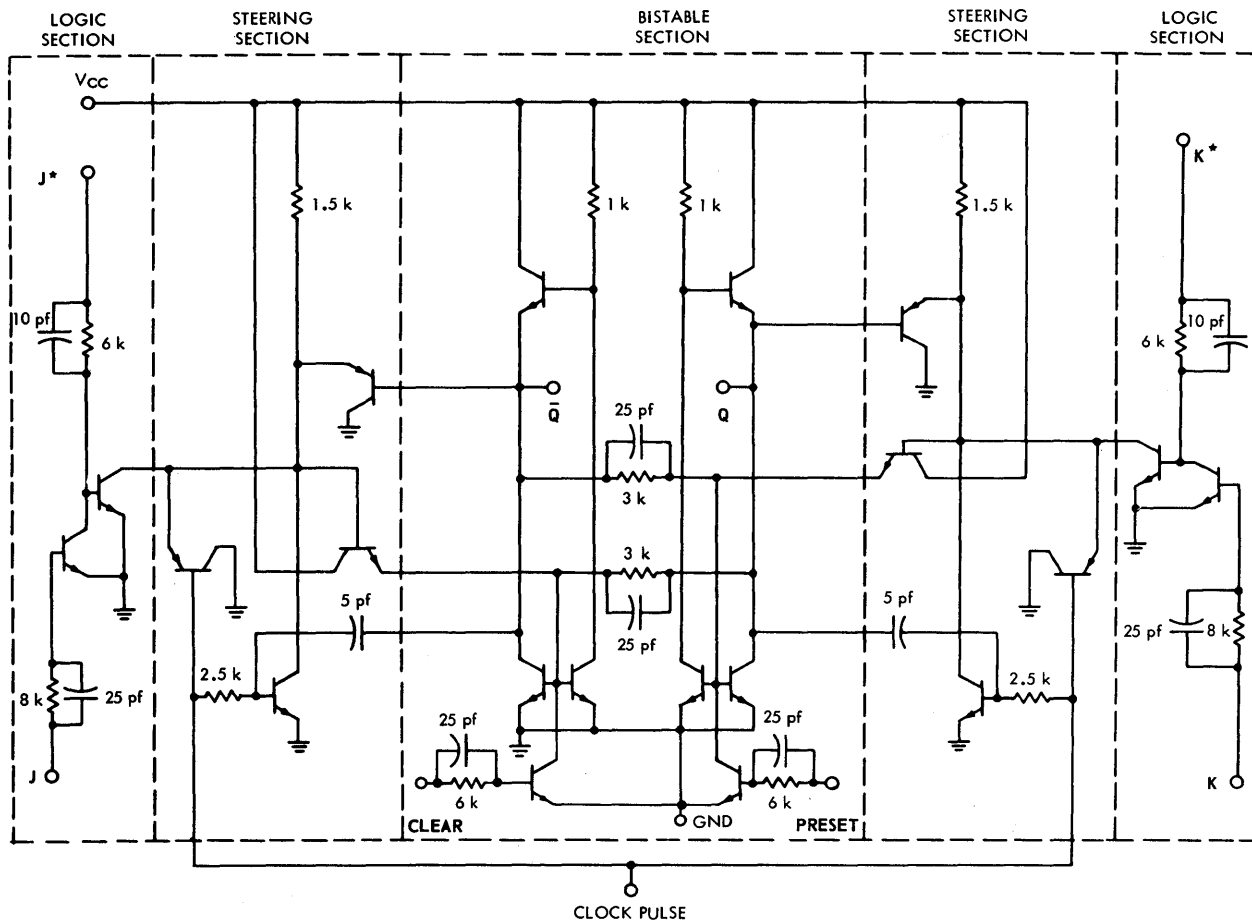
# TYPE SN7301

## J-K FLIP-FLOP WITH PRESET AND CLEAR

switching characteristics,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ v}$ ,  $N+ = N- = 0$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$ $t_r$ $t_s$ $t_f$	19	Clock Input: $V_{in} = 2.5\text{ v}$ , $t_f = 20\text{ nsec}$ , $t_p = 500\text{ nsec}$ , $f = 1\text{ Mc}$ J, J*, K and K* Input: $V_{in} = V_{CC}$ Preset Input: $V_{in} = 0$ Clear Input: $V_{in} = 0$	20 20 40 25	30 45 60 40	nsec nsec nsec nsec
$t_{set(1)}$	20	Clock Input: $V_{in} = 2.5\text{ v}$ , $t_f = 20\text{ nsec}$ , $t_p = 500\text{ nsec}$ , $f = 1\text{ Mc}$	50		nsec
$t_{set(0)}$		J, J*, K or K* Input: $V_{in(1)} = 2.5\text{ v}$ , $V_{in(0)} = 0$ , $t_r = t_f = 50\text{ nsec}$	35		nsec
$t_{preset}$	21	Clock Input: $V_{in} = 0$ Preset Input: $V_{in} = 2.5\text{ v}$ , $t_f = 50\text{ nsec}$	55		nsec
$t_{clear}$	21	Clock Input: $V_{in} = 0$ Clear Input: $V_{in} = 2.5\text{ v}$ , $t_f = 50\text{ nsec}$	75		nsec

### schematic



NOTES: a. Component values shown are nominal.  
b. Resistor values are in ohms.

# TYPE SN7302 DUAL J-K FLIP-FLOP WITH PRESET

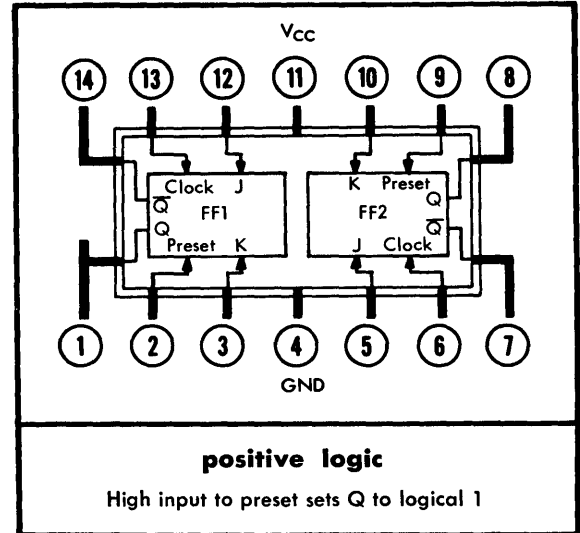
logic

TRUTH TABLE  
EACH FLIP-FLOP

$t_n$		$t_{n+1}$
J	K	Q
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\bar{Q}_n$

$t_n$  = Bit time before clock pulse

$t_{n+1}$  = Bit time after clock pulse



**recommended operating conditions**

Supply Voltage, $V_{CC}$ . . . . .	3 v to 4 v
Maximum Fan-out From Each Output Into Positive Loads, $N^+$ . . . . .	10
Maximum Fan-out From Each Output Into Negative Loads, $N^-$ . . . . .	10
Fall Time of Clock Pulse, $t_{f(\text{clock})}$ . . . . .	20 to 150 nsec
Minimum Width of Clock Pulse, $t_{p(\text{clock})}$ . . . . .	50 nsec

**electrical characteristics (unless otherwise noted  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 3\text{v}$  to  $4\text{v}$ )**

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at J, K, and preset inputs	1	$V_{CC} = 3\text{v}$	1.7		3	v
		$V_{CC} = 4\text{v}$	2.4		4	v
$V_{in(1)}$ Input voltage required to ensure logical 1 at clock input	2	$V_{CC} = 3\text{v}$	1.5		3	v
		$V_{CC} = 4\text{v}$	2.2		4	v
$V_{in(0)}$ Input voltage required to ensure logical 0 at J, K, preset, and clock inputs	1, 2		0		0.4	v
$V_{out(1)}$ Logical 1 output voltage (off level)	3	$V_{CC} = 3\text{v}$ , $N^+ = 10$ ( $I_{load} = -5\text{ma}$ )	1.7			v
		$V_{CC} = 4\text{v}$ , $N^+ = 10$ ( $I_{load} = -8\text{ma}$ )	2.6			v
$V_{out(0)}$ Logical 0 output voltage (on level)	3	$V_{CC} = 3\text{v}$ , $N^- = 10$ ( $I_{sink} = 2\text{ma}$ )			0.3	v
		$V_{CC} = 4\text{v}$ , $N^- = 10$ ( $I_{sink} = 2\text{ma}$ )			0.3	v
$I_{in}$ J, K, and preset input current	3	$V_{in} = 1.7\text{v}$			0.5	ma
		$V_{in} = 2.6\text{v}$			0.8	ma
$I_{in}$ Clock input current	3	$V_{in} = 1.7\text{v}$			1.25	ma
		$V_{in} = 2.4\text{v}$			2	ma
		$V_{in} = 0.3\text{v}$			-0.5	ma
$I_{CC(av)}$ Average supply current (each flip-flop)	4	$V_{CC} = 3\text{v}$ , $N^+ = N^- = 0$ , Toggle = 1 Mc, $T_A = 25^\circ\text{C}$		9		ma
		$V_{CC} = 4\text{v}$ , $N^+ = N^- = 0$ , Toggle = 1 Mc, $T_A = 25^\circ\text{C}$		13		ma



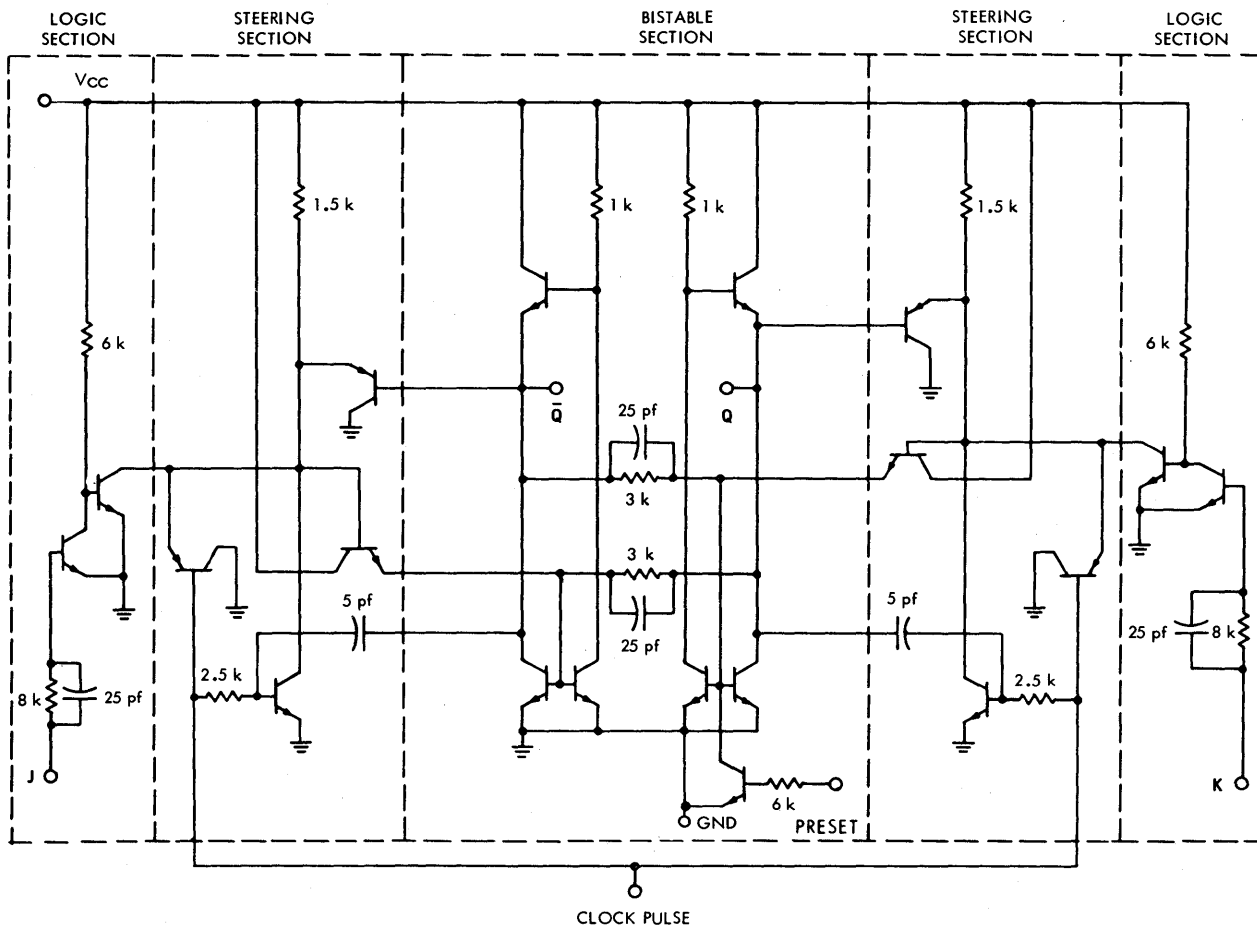
# TYPE SN7302

## DUAL J-K FLIP-FLOP WITH PRESET

switching characteristics,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ v}$ ,  $N+ = N- = 0$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$ Delay Time	19	Clock Input: $V_{in} = 2.5\text{ v}$ , $t_f = 20\text{ nsec}$ , $t_p = 500\text{ nsec}$ , $f = 1\text{ Mc}$ J and K Input: $V_{in} = V_{CC}$ Preset Input: $V_{in} = 0$	20	30	nsec
$t_r$ Rise Time			20	45	nsec
$t_s$ Storage Time			40	60	nsec
$t_f$ Fall Time			25	40	nsec
$t_{set(1)}$ Time to Set a Logical 1: J or K	20	Clock Input: $V_{in} = 2.5\text{ v}$ , $t_f = 20\text{ nsec}$ , $t_p = 500\text{ nsec}$ , $f = 1\text{ Mc}$ J or K Input: $V_{in(1)} = 2.5\text{ v}$ , $V_{in(0)} = 0$ , $t_r = t_f = 50\text{ nsec}$	50		nsec
$t_{set(0)}$ Time to Set a Logical 0: J or K			40		nsec
$t_{preset}$ Preset Time	21	Clock Input: $V_{in} = 0$ Preset Input: $V_{in} = 2.5\text{ v}$ , $t_f = 50\text{ nsec}$	75		nsec

### schematic (each flip-flop)



NOTES: a. Component values shown are nominal.  
b. Resistor values are in ohms.

# TYPE SN7304

## DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR

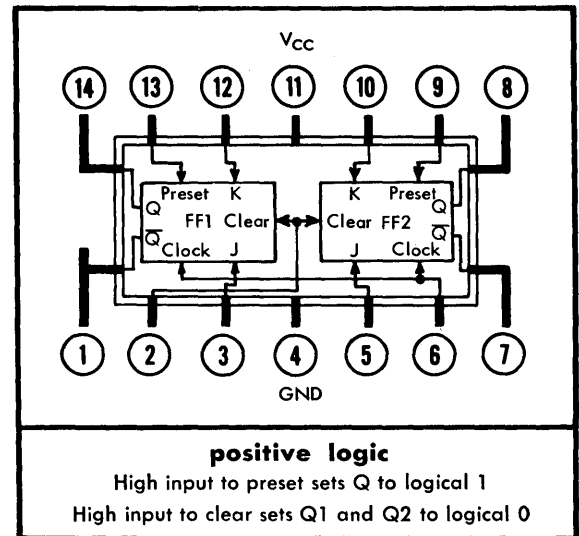
logic

TRUTH TABLE  
EACH FLIP-FLOP

$t_n$		$t_{n+1}$
J	K	Q
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\overline{Q_n}$

$t_n$  = Bit time before clock pulse

$t_{n+1}$  = Bit time after clock pulse



### recommended operating conditions

Supply Voltage, $V_{CC}$	3 v to 4 v
Maximum Fan-out From Each Output Into Positive Loads, $N^+$	10
Maximum Fan-out From Each Output Into Negative Loads, $N^-$	10
Fall Time of Clock Pulse, $t_{f(\text{clock})}$	20 to 150 nsec
Minimum Width of Clock Pulse, $t_{p(\text{clock})}$	50 nsec

### electrical characteristics (unless otherwise noted $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ , $V_{CC} = 3\text{ v}$ to $4\text{ v}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at J, K, preset, and clear inputs	1	$V_{CC} = 3\text{ v}$	1.7		3	v
		$V_{CC} = 4\text{ v}$	2.4		4	v
$V_{in(1)}$ Input voltage required to ensure logical 1 at clock input	2	$V_{CC} = 3\text{ v}$	1.5		3	v
		$V_{CC} = 4\text{ v}$	2.2		4	v
$V_{in(0)}$ Input voltage required to ensure logical 0 at J, K, preset, clear, and clock inputs	1, 2		0		0.4	v
$V_{out(1)}$ Logical 1 output voltage (off level)	3	$V_{CC} = 3\text{ v}$ , $N^+ = 10$ ( $I_{load} = -5\text{ ma}$ )	1.7			v
		$V_{CC} = 4\text{ v}$ , $N^+ = 10$ ( $I_{load} = -8\text{ ma}$ )	2.6			v
$V_{out(0)}$ Logical 0 output voltage (on level)	3	$V_{CC} = 3\text{ v}$ , $N^- = 10$ ( $I_{sink} = 2\text{ ma}$ )			0.3	v
		$V_{CC} = 4\text{ v}$ , $N^- = 10$ ( $I_{sink} = 2\text{ ma}$ )			0.3	v
$I_{in}$ J, K, and preset input current	3	$V_{in} = 1.7\text{ v}$			0.5	ma
		$V_{in} = 2.6\text{ v}$			0.8	ma
$I_{in}$ Clock input current	3	$V_{in} = 1.7\text{ v}$			2.5	ma
		$V_{in} = 2.4\text{ v}$			4	ma
		$V_{in} = 0.3\text{ v}$			-1	ma
$I_{in}$ Clear input current	3	$V_{in} = 1.7\text{ v}$			1	ma
		$V_{in} = 2.6\text{ v}$			1.6	ma
$I_{CC(av)}$ Average supply current (each flip-flop)	4	$V_{CC} = 3\text{ v}$ , $N^+ = N^- = 0$ , Toggle = 1 Mc, $T_A = 25^\circ\text{C}$		9		ma
		$V_{CC} = 4\text{ v}$ , $N^+ = N^- = 0$ , Toggle = 1 Mc, $T_A = 25^\circ\text{C}$		13		ma

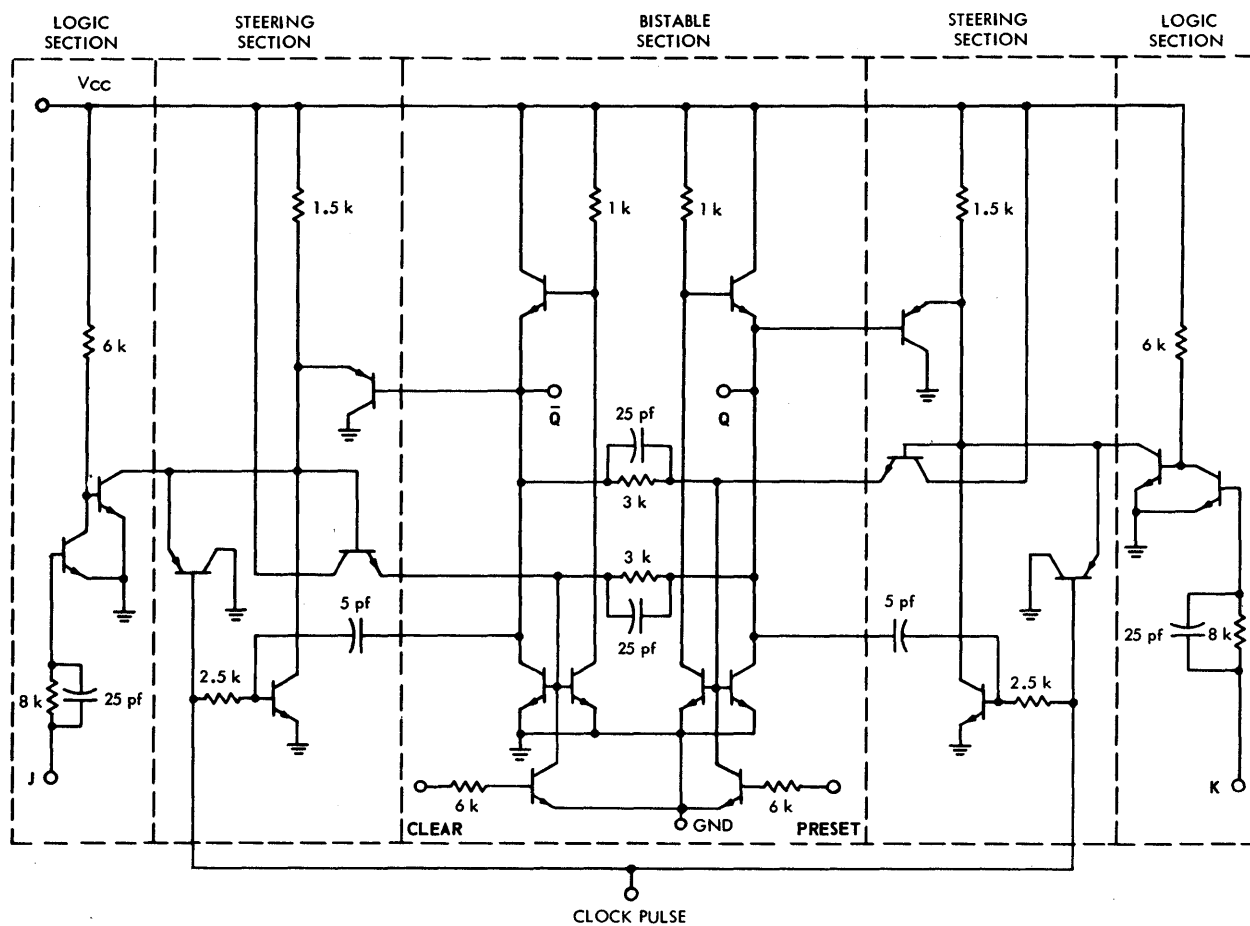
# TYPE SN7304

## DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR

switching characteristics,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ v}$ ,  $N+ = N- = 0$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$ Delay Time	19	Clock Input: $V_{in} = 2.5\text{ v}$ , $t_f = 20\text{ nsec}$ , $t_p = 500\text{ nsec}$ , $f = 1\text{ Mc}$ J and K Input: $V_{in} = V_{CC}$ Preset Input: $V_{in} = 0$ Clear Input: $V_{in} = 0$	20	30	nsec
$t_r$ Rise Time			20	45	nsec
$t_s$ Storage Time			40	60	nsec
$t_f$ Fall Time			25	40	nsec
$t_{set(1)}$ Time to Set a Logical 1: J or K	20	Clock Input: $V_{in} = 2.5\text{ v}$ , $t_f = 20\text{ nsec}$ , $t_p = 500\text{ nsec}$ , $f = 1\text{ Mc}$ J or K Input: $V_{in(1)} = 2.5\text{ v}$ , $V_{in(0)} = 0$ , $t_r = t_f = 50\text{ nsec}$	50		nsec
$t_{set(0)}$ Time to Set a Logical 0: J or K			40		nsec
$t_{preset}$ Preset Time	21	Clock Input: $V_{in} = 0$ Preset Input: $V_{in} = 2.5\text{ v}$ , $t_f = 50\text{ nsec}$	75		nsec
$t_{clear}$ Clear Time	21	Clock Input: $V_{in} = 0$ Clear Input: $V_{in} = 2.5\text{ v}$ , $t_f = 50\text{ nsec}$	100		nsec

### schematic (each flip-flop)

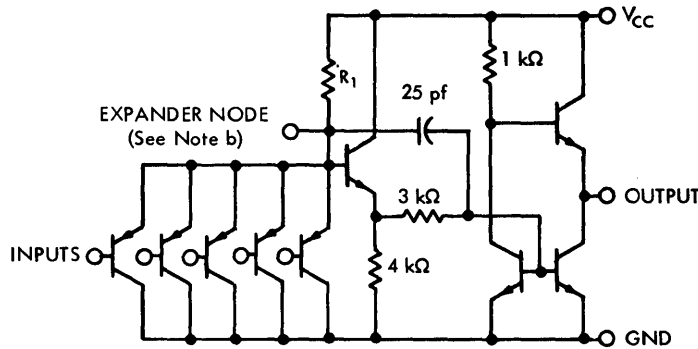


NOTES: a. Component values shown are nominal.  
b. Resistor values are in ohms.

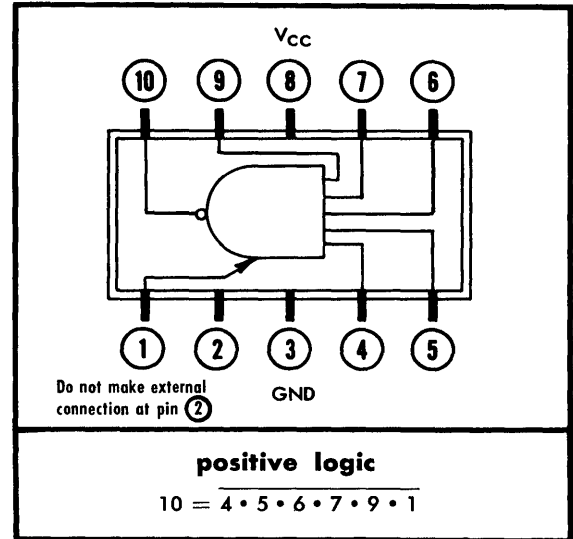
# TYPE SN7310

## 5-INPUT EXPANDABLE NAND/NOR GATE

### schematic



- NOTES: a. Component values shown are nominal
- b. Four SN7320 expanders may be fanned into one SN7310 to provide a total fan-in of 25. If expander is not used leave pin ① open.



### recommended operating conditions

Supply Voltage, $V_{CC}$	3 v to 4 v
Maximum Fan-out Into Positive Loads, $N+$	10
Maximum Fan-out Into Negative Loads, $N-$	10

### electrical characteristics (unless otherwise noted $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ , $V_{CC} = 3\text{ v}$ to $4\text{ v}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 0 (on level) at output.	5	$V_{CC} = 3\text{ v}$	1.7		3	v
		$V_{CC} = 4\text{ v}$	2.4		4	v
$V_{in(1)X}$ Input voltage required at expander node (pin ①) to ensure logical 0 (on level) at output	8	$V_{CC} = 3\text{ v}$	2.1		3	v
		$V_{CC} = 4\text{ v}$	2.9		4	v
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 (off level) at output	6		0		0.4	v
$V_{in(0)X}$ Input voltage required at expander node (pin ①) to ensure logical 1 (off level) at output	7	$T_A = 0^\circ\text{C}$	0		1.2	v
		$T_A = 70^\circ\text{C}$	0		1	v
$V_{out(1)}$ Logical 1 output voltage (off level)	6	$V_{CC} = 3\text{ v}$ , $V_{in} = 0.4\text{ v}$ , $N+ = 10$ ( $I_{load} = -5\text{ ma}$ )	1.7			v
		$V_{CC} = 4\text{ v}$ , $V_{in} = 0.4\text{ v}$ , $N+ = 10$ ( $I_{load} = -8\text{ ma}$ )	2.6			v
$V_{out(0)}$ Logical 0 output voltage (on level)	5	$V_{CC} = 3\text{ v}$ , $V_{in} = 1.7\text{ v}$ , $N- = 10$ ( $I_{sink} = 2\text{ ma}$ )			0.3	v
		$V_{CC} = 4\text{ v}$ , $V_{in} = 2.4\text{ v}$ , $N- = 10$ ( $I_{sink} = 2\text{ ma}$ )			0.3	v

Characteristics continued next page.

# TYPE SN7310

## 5-INPUT EXPANDABLE NAND/NOR GATE

### electrical characteristics continued

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in}$ Input current (each input)	6	$V_{in} = 0.3 \text{ v}$ , $N+ = N- = 0$			-0.2	ma
$I_{CC(on)}$ On level supply current	9	$V_{CC} = V_{in} = 3 \text{ v}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		3.3		ma
		$V_{CC} = V_{in} = 4 \text{ v}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		4.5		ma
$I_{CC(off)}$ Off level supply current	9	$V_{CC} = 3 \text{ v}$ , $V_{in} = 0.3 \text{ v}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		1.2		ma
		$V_{CC} = 4 \text{ v}$ , $V_{in} = 0.3 \text{ v}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		1.6		ma
$R_{1(eff)}$ $R_1$ Effective resistance	10	$T_A = 0^\circ\text{C}$	1.35		2.6	$k \Omega$
		$T_A = 70^\circ\text{C}$	1.5		2.8	$k \Omega$

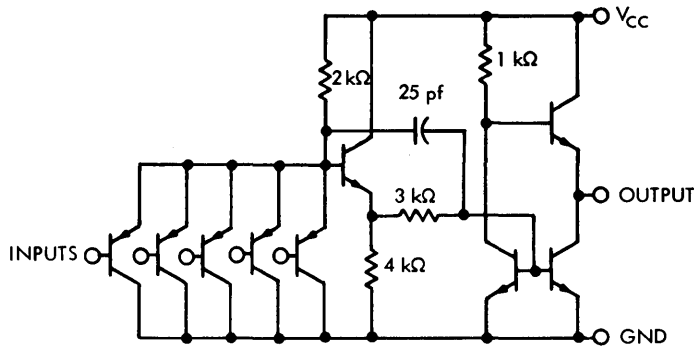
### switching characteristics, $T_A = 25^\circ\text{C}$ , $V_{CC} = 3.5 \text{ v}$ , $N- = 1$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$ Delay Time	22	<i>Input</i> : $V_{in} = 2.5 \text{ v}$ , $f = 1 \text{ Mc}$ , $t_p = 500 \text{ nsec}$ , $t_r = t_f = 20 \text{ nsec}$	35	45	nsec
$t_r$ Rise Time			40	50	nsec
$t_s$ Storage Time			25	45	nsec
$t_f$ Fall Time			30	40	nsec
$t_{pd}$ Propagation Delay Time	23		30		nsec

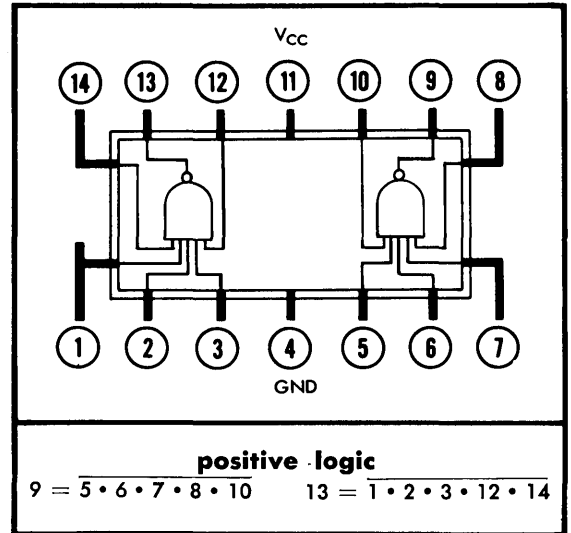
# TYPE SN7311

## DUAL 5-INPUT NAND/NOR GATE

schematic (each gate)



Component values shown are nominal



**recommended operating conditions**

Supply Voltage, $V_{CC}$ . . . . .	3 v to 4 v
Maximum Fan-out From Each Output Into Positive Loads, $N^+$ . . . . .	10
Maximum Fan-out From Each Output Into Negative Loads, $N^-$ . . . . .	10

**electrical characteristics (unless otherwise noted  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 3\text{ v}$  to  $4\text{ v}$ )**

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	5	$V_{CC} = 3\text{ v}$	1.7		3	v
		$V_{CC} = 4\text{ v}$	2.4		4	v
$V_{in(0)}$	6		0		0.4	v
$V_{out(1)}$	6	$V_{CC} = 3\text{ v}$ , $V_{in} = 0.4\text{ v}$ , $N^+ = 10$ ( $I_{load} = -5\text{ ma}$ )	1.7			v
		$V_{CC} = 4\text{ v}$ , $V_{in} = 0.4\text{ v}$ , $N^+ = 10$ ( $I_{load} = -8\text{ ma}$ )	2.6			v
$V_{out(0)}$	5	$V_{CC} = 3\text{ v}$ , $V_{in} = 1.7\text{ v}$ , $N^- = 10$ ( $I_{sink} = 2\text{ ma}$ )			0.3	v
		$V_{CC} = 4\text{ v}$ , $V_{in} = 2.4\text{ v}$ , $N^- = 10$ ( $I_{sink} = 2\text{ ma}$ )			0.3	v
$I_{in}$	6	$V_{in} = 0.3\text{ v}$ , $N^+ = N^- = 0$			-0.2	ma
$I_{CC(on)}$	9	$V_{CC} = V_{in} = 3\text{ v}$ , $N^+ = N^- = 0$ , $T_A = 25^\circ\text{C}$		3.3		ma
		$V_{CC} = V_{in} = 4\text{ v}$ , $N^+ = N^- = 0$ , $T_A = 25^\circ\text{C}$		4.5		ma
$I_{CC(off)}$	9	$V_{CC} = 3\text{ v}$ , $V_{in} = 0.3\text{ v}$ , $N^+ = N^- = 0$ , $T_A = 25^\circ\text{C}$		1.2		ma
		$V_{CC} = 4\text{ v}$ , $V_{in} = 0.3\text{ v}$ , $N^+ = N^- = 0$ , $T_A = 25^\circ\text{C}$		1.6		ma

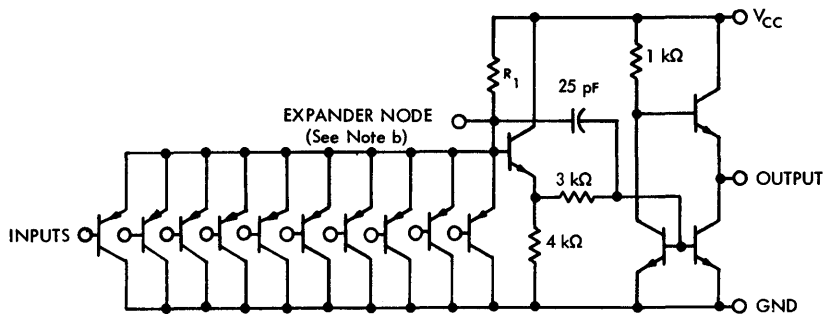
**switching characteristics,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ v}$ ,  $N^- = 1$**

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$	22	$Input: V_{in} = 2.5\text{ v}$ , $f = 1\text{ Mc}$ , $t_p = 500\text{ nsec}$ , $t_r = t_f = 20\text{ nsec}$	20	30	nsec
$t_r$			25	45	nsec
$t_s$			25	45	nsec
$t_f$			25	40	nsec
$t_{pd}$	23		25		nsec

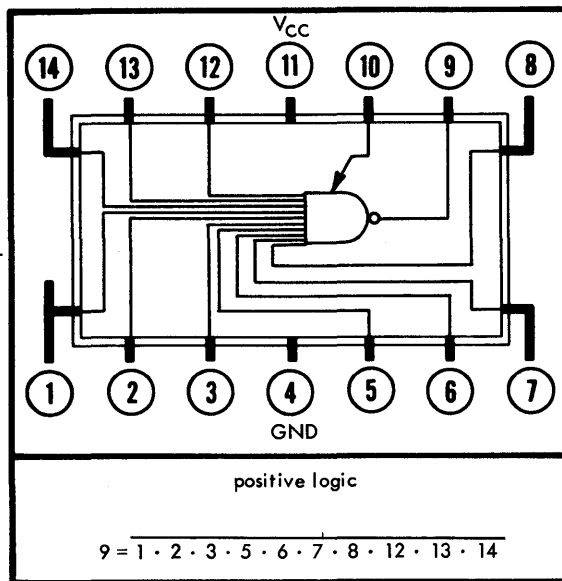
# TYPE SN7315

## 10-INPUT EXPANDABLE NAND/NOR GATE

### schematic



- NOTES: a. Component values shown are nominal.  
 b. Three SN7320 expanders may be fanned into one SN7315 to provide a total fan-in of 25. If expander is not used leave pin ⑩ open.



### recommended operating conditions

Supply Voltage, $V_{CC}$	3 v to 4 v
Maximum Fan-out Into Positive Loads, $N+$	10
Maximum Fan-out Into Negative Loads, $N-$	10

### electrical characteristics (unless otherwise noted $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ , $V_{CC} = 3\text{ v}$ to $4\text{ v}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 0 (on level) at output.	5	$V_{CC}=3\text{ v}$	1.7		3	v
		$V_{CC}=4\text{ v}$	2.4		4	v
$V_{in(1)X}$ Input voltage required at expander node (pin ⑩) to ensure logical 0 (on level) at output	8	$V_{CC}=3\text{ v}$	2.1		3	v
		$V_{CC}=4\text{ v}$	2.9		4	v
$V_{in(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 (off level) at output	6		0		0.4	v
$V_{in(0)X}$ Input voltage required at expander node (pin ⑩) to ensure logical 1 (off level) at output	7	$T_A=0^\circ\text{C}$	0		1.2	v
		$T_A=70^\circ\text{C}$	0		1	v
$V_{out(1)}$ Logical 1 output voltage (off level)	6	$V_{CC}=3\text{ v}$ , $V_{in}=0.4\text{ v}$ , $N+=10$ ( $I_{load}=-5\text{ ma}$ )	1.7			v
		$V_{CC}=4\text{ v}$ , $V_{in}=0.4\text{ v}$ , $N+=10$ ( $I_{load}=-8\text{ ma}$ )	2.6			v
$V_{out(0)}$ Logical 0 output voltage (on level)	5	$V_{CC}=3\text{ v}$ , $V_{in}=1.7\text{ v}$ , $N-=10$ ( $I_{sink}=2\text{ ma}$ )			0.3	v
		$V_{CC}=4\text{ v}$ , $V_{in}=2.4\text{ v}$ , $N-=10$ ( $I_{sink}=2\text{ ma}$ )			0.3	v
$I_{in}$ Input current (each input)	6	$V_{in}=0.3\text{ v}$ , $N+=N-=0$			-0.2	ma
$I_{CC(on)}$ On level supply current	9	$V_{CC}=V_{in}=3\text{ v}$ , $N+=N-=0$ , $T_A=25^\circ\text{C}$		3.3		ma
		$V_{CC}=V_{in}=4\text{ v}$ , $N+=N-=0$ , $T_A=25^\circ\text{C}$		4.5		ma

Characteristics continued next page.

# TYPE SN7315

## 10-INPUT EXPANDABLE NAND/NOR GATE

### electrical characteristics continued

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC(off)}$ Off level supply current	9	$V_{CC}=3\text{ v}, V_{in}=0.3\text{ v}, N+=N-=0, T_A=25^\circ\text{C}$		1.2		ma
		$V_{CC}=4\text{ v}, V_{in}=0.3\text{ v}, N+=N-=0, T_A=25^\circ\text{C}$		1.6		ma
$R_{1(off)}$ $R_1$ Effective resistance	10	$T_A=0^\circ\text{C}$	1.35		2.6	k $\Omega$
		$T_A=70^\circ\text{C}$	1.5		2.8	k $\Omega$

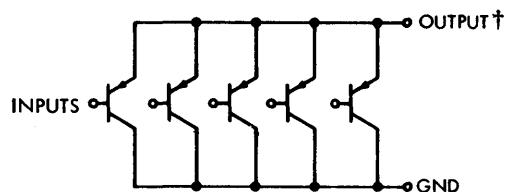
### switching characteristics, $T_A = 25^\circ\text{C}, V_{CC} = 3.5\text{ v}, N- = 1$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$ Delay Time	22	<i>Input</i> : $V_{in}=2.5\text{ v}, f=1\text{ Mc}, t_p=500\text{ nsec}, t_r=t_f=20\text{ nsec}$	35	45	nsec
$t_r$ Rise Time			40	50	nsec
$t_s$ Storage Time			25	45	nsec
$t_f$ Fall Time			30	40	nsec
$t_{pd}$ Propagation Delay Time	23		30		nsec

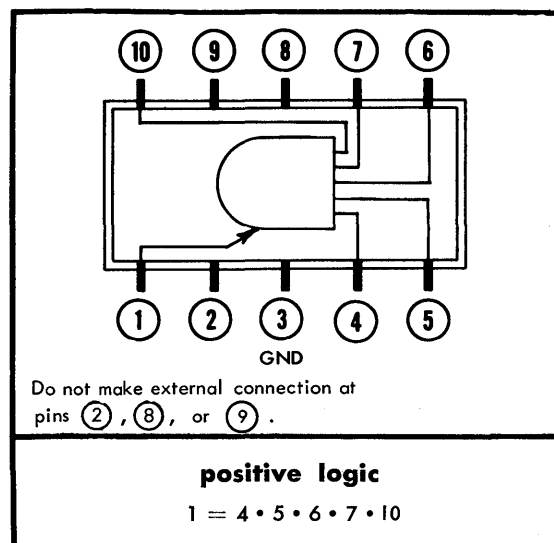
# TYPE SN7320

## 5-INPUT EXPANDER

### schematic



† Connect output to expander node of SN7310 (pin ①) or SN7315 (pin ⑩).



### electrical characteristics (unless otherwise noted $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}, V_{CC} = 3\text{ v}$ to $4\text{ v}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in}$ Input Current (each input)	11	$V_{in}=0.3\text{ v}$		-0.2	ma
$V_{out(0)X}$ Expander node output voltage (off level) with logical 0 at any input	11	$V_{CC}=4\text{ v}, V_{in}=0.3\text{ v}, T_A=0^\circ\text{C}$		1.2	v
		$V_{CC}=4\text{ v}, V_{in}=0.3\text{ v}, T_A=70^\circ\text{C}$		1	v
$V_{out(1)X}$ Expander node output voltage (on level) with logical 1 at all inputs	12	$V_{CC}=3\text{ v}, V_{in}=1.7\text{ v}$	2.1		v
		$V_{CC}=4\text{ v}, V_{in}=2.6\text{ v}$	2.9		v

NOTES: The SN7320  $V_{in(1)}$  and  $V_{in(0)}$  limits are the same as defined for the SN7310 and the SN7315.

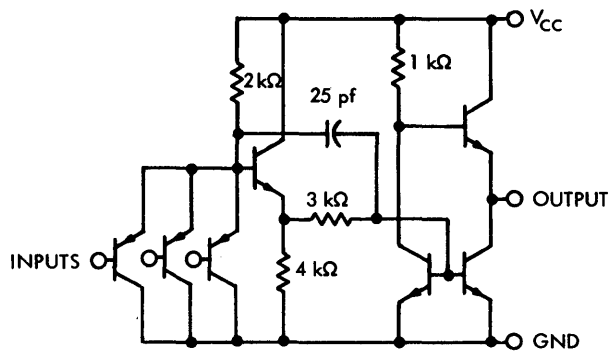
Four SN7320 expanders may be fanned into one SN7310 to provide a total fan-in of 25. Three SN7320 expanders may be fanned into one SN7315 to provide a total fan-in of 25.



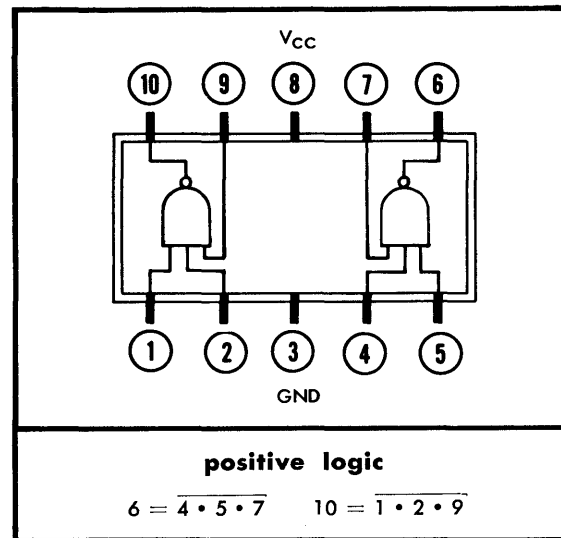
# TYPE SN7330

## DUAL 3-INPUT NAND/NOR GATE

schematic (each gate)



Component values shown are nominal



### recommended operating conditions

Supply Voltage, $V_{CC}$	3 v to 4 v
Maximum Fan-out From Each Output Into Positive Loads, $N+$	10
Maximum Fan-out From Each Output Into Negative Loads, $N-$	10

### electrical characteristics (unless otherwise noted $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ , $V_{CC} = 3\text{ v}$ to $4\text{ v}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	5	$V_{CC} = 3\text{ v}$	1.7		3	v
		$V_{CC} = 4\text{ v}$	2.4		4	v
$V_{in(0)}$	6		0		0.4	v
$V_{out(1)}$	6	$V_{CC} = 3\text{ v}$ , $V_{in} = 0.4\text{ v}$ , $N+ = 10$ ( $I_{load} = -5\text{ ma}$ )	1.7			v
		$V_{CC} = 4\text{ v}$ , $V_{in} = 0.4\text{ v}$ , $N+ = 10$ ( $I_{load} = -8\text{ ma}$ )	2.6			v
$V_{out(0)}$	5	$V_{CC} = 3\text{ v}$ , $V_{in} = 1.7\text{ v}$ , $N- = 10$ ( $I_{sink} = 2\text{ ma}$ )			0.3	v
		$V_{CC} = 4\text{ v}$ , $V_{in} = 2.4\text{ v}$ , $N- = 10$ ( $I_{sink} = 2\text{ ma}$ )			0.3	v
$I_{in}$	6	$V_{in} = 0.3\text{ v}$ , $N+ = N- = 0$			-0.2	ma
$I_{CC(on)}$	9	$V_{CC} = V_{in} = 3\text{ v}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		3.3		ma
		$V_{CC} = V_{in} = 4\text{ v}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		4.5		ma
$I_{CC(off)}$	9	$V_{CC} = 3\text{ v}$ , $V_{in} = 0.3\text{ v}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		1.2		ma
		$V_{CC} = 4\text{ v}$ , $V_{in} = 0.3\text{ v}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		1.6		ma

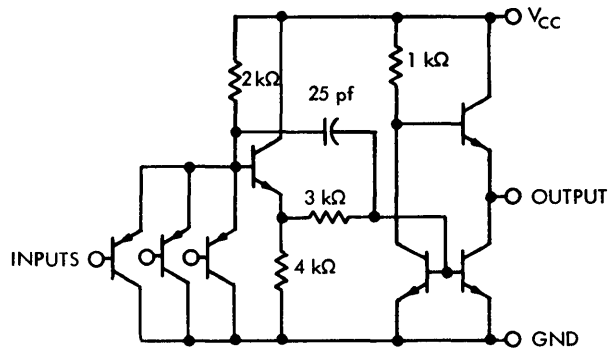
### switching characteristics, $T_A = 25^\circ\text{C}$ , $V_{CC} = 3.5\text{ v}$ , $N- = 1$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$	22	$Input: V_{in} = 2.5\text{ v}$ , $f = 1\text{ Mc}$ , $t_p = 500\text{ nsec}$ , $t_r = t_f = 20\text{ nsec}$	20	30	nsec
$t_r$			25	45	nsec
$t_s$			25	45	nsec
$t_f$			25	40	nsec
$t_{pd}$	23		25		nsec

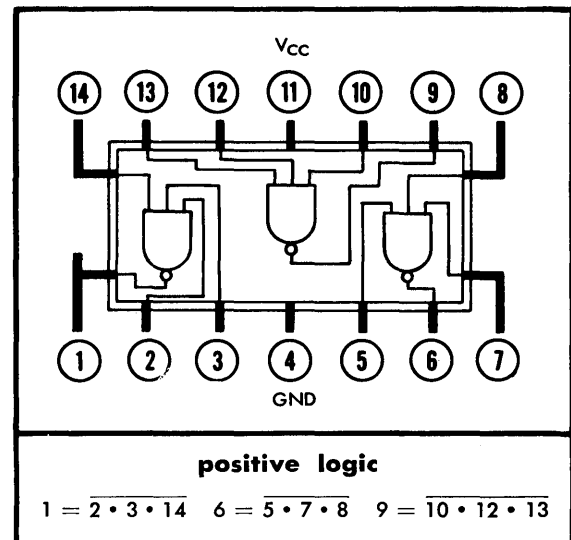
# TYPE SN7331

## TRIPLE 3-INPUT NAND/NOR GATE

### schematic (each gate)



Component values shown are nominal.



### recommended operating conditions

Supply Voltage, $V_{CC}$	3 v to 4 v
Maximum Fan-out From Each Output Into Positive Loads, $N+$	10
Maximum Fan-out From Each Output Into Negative Loads, $N-$	10

### electrical characteristics (unless otherwise noted $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ , $V_{CC} = 3\text{ v}$ to $4\text{ v}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	5	$V_{CC} = 3\text{ v}$	1.7		3	v
		$V_{CC} = 4\text{ v}$	2.4		4	v
$V_{in(0)}$	6		0		0.4	v
$V_{out(1)}$	6	$V_{CC} = 3\text{ v}$ , $V_{in} = 0.4\text{ v}$ , $N+ = 10$ ( $I_{load} = -5\text{ ma}$ )	1.7			v
		$V_{CC} = 4\text{ v}$ , $V_{in} = 0.4\text{ v}$ , $N+ = 10$ ( $I_{load} = -8\text{ ma}$ )	2.6			v
$V_{out(0)}$	5	$V_{CC} = 3\text{ v}$ , $V_{in} = 1.7\text{ v}$ , $N- = 10$ ( $I_{sink} = 2\text{ ma}$ )			0.3	v
		$V_{CC} = 4\text{ v}$ , $V_{in} = 2.4\text{ v}$ , $N- = 10$ ( $I_{sink} = 2\text{ ma}$ )			0.3	v
$I_{in}$	6	$V_{in} = 0.3\text{ v}$ , $N+ = N- = 0$			-0.2	ma
$I_{CC(on)}$	9	$V_{CC} = V_{in} = 3\text{ v}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		3.3		ma
		$V_{CC} = V_{in} = 4\text{ v}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		4.5		ma
$I_{CC(off)}$	9	$V_{CC} = 3\text{ v}$ , $V_{in} = 0.3\text{ v}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		1.2		ma
		$V_{CC} = 4\text{ v}$ , $V_{in} = 0.3\text{ v}$ , $N+ = N- = 0$ , $T_A = 25^\circ\text{C}$		1.6		ma

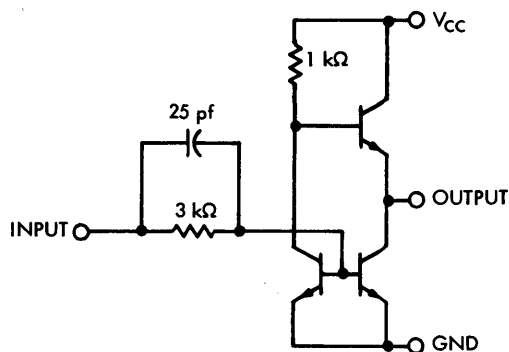
### switching characteristics, $T_A = 25^\circ\text{C}$ , $V_{CC} = 3.5\text{ v}$ , $N- = 1$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$	22	Input: $V_{in} = 2.5\text{ v}$ , $f = 1\text{ Mc}$ , $t_p = 500\text{ nsec}$ , $t_r = t_f = 20\text{ nsec}$	20	30	nsec
$t_r$			25	45	nsec
$t_s$			25	45	nsec
$t_f$			25	40	nsec
$t_{pd}$			23	25	nsec

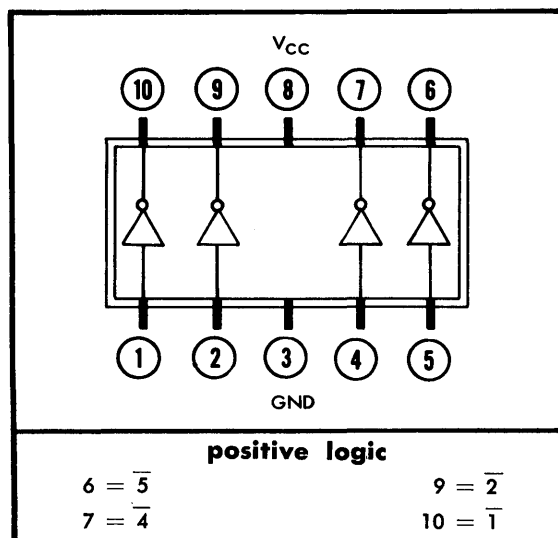
# TYPE SN7350

## QUADRUPLE INVERTER/DRIVER

schematic (each inverter)



Component values shown are nominal



### recommended operating conditions

Supply Voltage, $V_{CC}$	3 v to 4 v
Maximum Fan-out From Each Output Into Positive Loads, $N_+$	10
Maximum Fan-out From Each Output Into Negative Loads, $N_-$	10

### electrical characteristics (unless otherwise noted $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ , $V_{CC} = 3\text{ v}$ to $4\text{ v}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	13	$V_{CC} = 3\text{ v}$	1.7		3	v
		$V_{CC} = 4\text{ v}$	2.4		4	v
$V_{in(0)}$	13		0		0.4	v
$V_{out(1)}$	13	$V_{CC} = 3\text{ v}$ , $V_{in} = 0.4\text{ v}$ , $N_+ = 10$ ( $I_{load} = -5\text{ ma}$ )	1.7			v
		$V_{CC} = 4\text{ v}$ , $V_{in} = 0.4\text{ v}$ , $N_+ = 10$ ( $I_{load} = -8\text{ ma}$ )	2.6			v
$V_{out(0)}$	13	$V_{CC} = 3\text{ v}$ , $V_{in} = 1.7\text{ v}$ , $N_- = 10$ ( $I_{sink} = 2\text{ ma}$ )			0.3	v
		$V_{CC} = 4\text{ v}$ , $V_{in} = 2.4\text{ v}$ , $N_- = 10$ ( $I_{sink} = 2\text{ ma}$ )			0.3	v
$I_{in}$	13	$V_{CC} = 3\text{ v}$ , $V_{in} = 1.7\text{ v}$ , $N_+ = N_- = 0$			1	ma
		$V_{CC} = 4\text{ v}$ , $V_{in} = 2.6\text{ v}$ , $N_+ = N_- = 0$			1.6	ma
$I_{CC(on)}$	13	$V_{CC} = V_{in} = 3\text{ v}$ , $N_+ = N_- = 0$ , $T_A = 25^\circ\text{C}$		3.3		ma
		$V_{CC} = V_{in} = 4\text{ v}$ , $N_+ = N_- = 0$ , $T_A = 25^\circ\text{C}$		4.5		ma

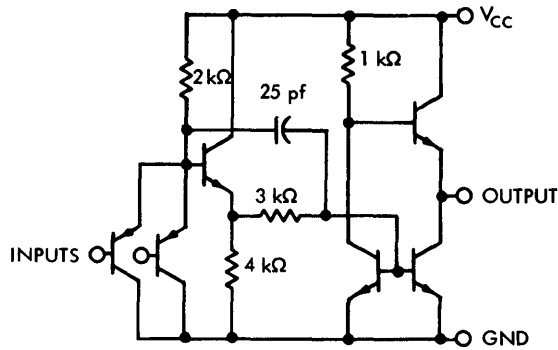
### switching characteristics, $T_A = 25^\circ\text{C}$ , $V_{CC} = 3.5\text{ v}$ , $N_- = 1$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$	22	Input: $V_{in} = 2.5\text{ v}$ , $f = 1\text{ Mc}$ , $t_p = 500\text{ nsec}$ , $t_r = t_f = 20\text{ nsec}$	20	30	nsec
$t_r$			25	45	nsec
$t_s$			25	45	nsec
$t_f$			25	40	nsec
$t_{pd}$	23		25		nsec

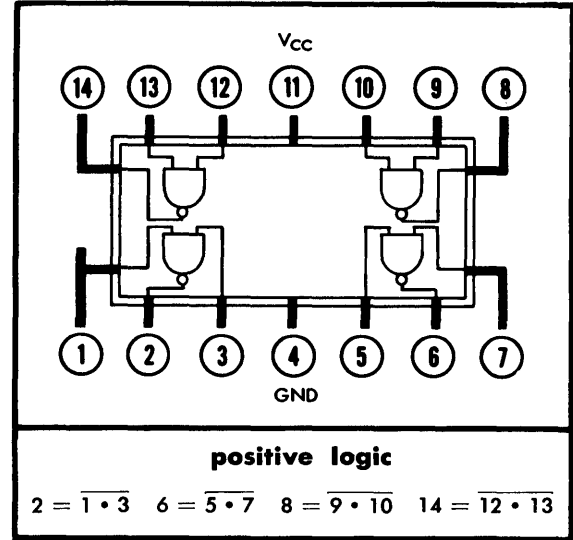
# TYPE SN7360

## QUADRUPLE 2-INPUT NAND/NOR GATE

### schematic (each gate)



Component values shown are nominal



### recommended operating conditions

Supply Voltage, $V_{CC}$	3 v to 4 v
Maximum Fan-out From Each Output Into Positive Loads, $N^+$	10
Maximum Fan-out From Each Output Into Negative Loads, $N^-$	10

### electrical characteristics (unless otherwise noted $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ , $V_{CC} = 3\text{ v}$ to $4\text{ v}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	5	$V_{CC} = 3\text{ v}$	1.7		3	v
		$V_{CC} = 4\text{ v}$	2.4		4	v
$V_{in(0)}$	6		0		0.4	v
$V_{out(1)}$	6	$V_{CC} = 3\text{ v}$ , $V_{in} = 0.4\text{ v}$ , $N^+ = 10$ ( $I_{load} = -5\text{ ma}$ )	1.7			v
		$V_{CC} = 4\text{ v}$ , $V_{in} = 0.4\text{ v}$ , $N^+ = 10$ ( $I_{load} = -8\text{ ma}$ )	2.6			v
$V_{out(0)}$	5	$V_{CC} = 3\text{ v}$ , $V_{in} = 1.7\text{ v}$ , $N^- = 10$ ( $I_{sink} = 2\text{ ma}$ )			0.3	v
		$V_{CC} = 4\text{ v}$ , $V_{in} = 2.4\text{ v}$ , $N^- = 10$ ( $I_{sink} = 2\text{ ma}$ )			0.3	v
$I_{in}$	6	$V_{in} = 0.3\text{ v}$ , $N^+ = N^- = 0$			-0.2	ma
$I_{CC(on)}$	9	$V_{CC} = V_{in} = 3\text{ v}$ , $N^+ = N^- = 0$ , $T_A = 25^\circ\text{C}$		3.3		ma
		$V_{CC} = V_{in} = 4\text{ v}$ , $N^+ = N^- = 0$ , $T_A = 25^\circ\text{C}$		4.5		ma
$I_{CC(off)}$	9	$V_{CC} = 3\text{ v}$ , $V_{in} = 0.3\text{ v}$ , $N^+ = N^- = 0$ , $T_A = 25^\circ\text{C}$		1.2		ma
		$V_{CC} = 4\text{ v}$ , $V_{in} = 0.3\text{ v}$ , $N^+ = N^- = 0$ , $T_A = 25^\circ\text{C}$		1.6		ma

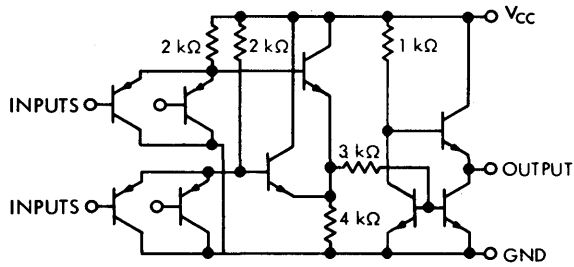
### switching characteristics, $T_A = 25^\circ\text{C}$ , $V_{CC} = 3.5\text{ v}$ , $N^- = 1$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$	22	$Input: V_{in} = 2.5\text{ v}$ , $f = 1\text{ Mc}$ , $t_p = 500\text{ nsec}$ , $t_r = t_f = 20\text{ nsec}$	20	30	nsec
$t_r$			25	45	nsec
$t_s$			25	45	nsec
$t_f$			25	40	nsec
$t_{pd}$	23		25		nsec

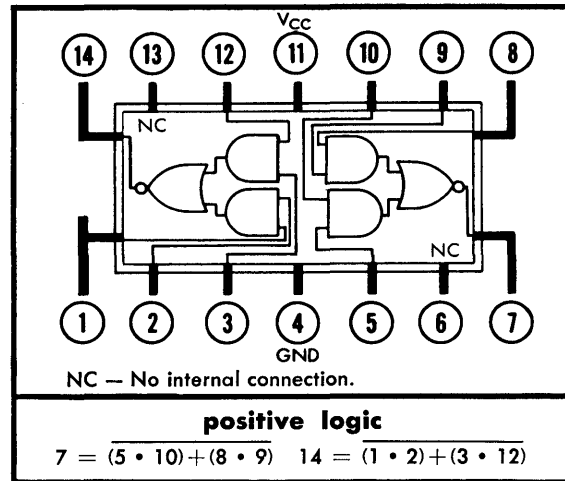
# TYPE SN7370

## DUAL AND-OR-INVERT GATE

schematic (each gate)



Component values shown are nominal.



### recommended operating conditions

Supply Voltage, $V_{CC}$	3 v to 4 v
Maximum Fan-out From Each Output Into Positive Loads, $N^+$	10
Maximum Fan-out From Each Output Into Negative Loads, $N^-$	10

### electrical characteristics (unless otherwise noted $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ , $V_{CC} = 3\text{ v}$ to $4\text{ v}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(0)}$ Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 (on level) at output	14	$V_{CC} = 3\text{ v}$	1.7		3	v
		$V_{CC} = 4\text{ v}$	2.4		4	v
$V_{in(1)}$ Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 (off level) at output	15		0		0.4	v
$V_{out(1)}$ Logical 1 output voltage (off level)	15	$V_{CC} = 3\text{ v}$ , $V_{in} = 0.4\text{ v}$ , $N^+ = 10$ ( $I_{load} = -5\text{ ma}$ )	1.7			v
		$V_{CC} = 4\text{ v}$ , $V_{in} = 0.4\text{ v}$ , $N^+ = 10$ ( $I_{load} = -8\text{ ma}$ )	2.6			v
$V_{out(0)}$ Logical 0 output voltage (on level)	14	$V_{CC} = 3\text{ v}$ , $V_{in} = 1.7\text{ v}$ , $N^- = 10$ ( $I_{sink} = 2\text{ ma}$ )			0.3	v
		$V_{CC} = 4\text{ v}$ , $V_{in} = 2.4\text{ v}$ , $N^- = 10$ ( $I_{sink} = 2\text{ ma}$ )			0.3	v
$I_{in}$ Input current (each input)	15	$V_{in} = 0.3\text{ v}$ , $N^+ = N^- = 0$			-0.2	ma
$I_{CC(on)}$ On level supply current (each gate)	14	$V_{CC} = V_{in} = 3\text{ v}$ , $N^+ = N^- = 0$ , $T_A = 25^\circ\text{C}$		3.3		ma
		$V_{CC} = V_{in} = 4\text{ v}$ , $N^+ = N^- = 0$ , $T_A = 25^\circ\text{C}$		4.5		ma
$I_{CC(off)}$ Off level supply current (each gate)	15	$V_{CC} = 3\text{ v}$ , $V_{in} = 0.3\text{ v}$ , $N^+ = N^- = 0$ , $T_A = 25^\circ\text{C}$		1.2		ma
		$V_{CC} = 4\text{ v}$ , $V_{in} = 0.3\text{ v}$ , $N^+ = N^- = 0$ , $T_A = 25^\circ\text{C}$		1.6		ma

### switching characteristics, $T_A = 25^\circ\text{C}$ , $V_{CC} = 3.5\text{ v}$ , $N^- = 1$

PARAMETER	TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
$t_d$ Delay Time	22	Input: $V_{in} = 2.5\text{ v}$ , $f = 1\text{ Mc}$ , $t_p = 500\text{ nsec}$ , $t_r = t_f = 20\text{ nsec}$	30	60	nsec
$t_r$ Rise Time			30	60	nsec
$t_s$ Storage Time			100	200	nsec
$t_f$ Fall Time			100	200	nsec
$t_{pd}$ Propagation Delay Time	23		65		nsec

# TYPE SN7380

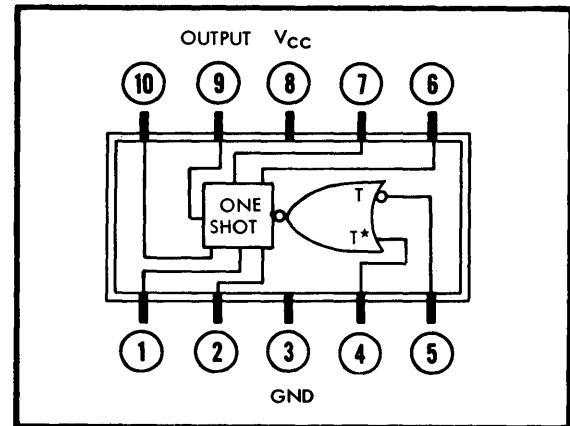
## ONE-SHOT MONOSTABLE MULTIVIBRATOR

logic

TRUTH TABLE  
positive logic

T		T*		OUTPUT
$t_n$	$t_{n+1}$	$t_n$	$t_{n+1}$	
1	1	..	..	INHIBITED (logical 1)
..	..	0	0	INHIBITED (logical 1)
0	0	1	0	ONE-SHOT (logical 0 for $t_p$ nsec)
0	1	1	1	ONE-SHOT (logical 0 for $t_p$ nsec)

$t_n$  = bit time before change in input levels  
 $t_{n+1}$  = bit time after change in input levels



### recommended operating conditions

Supply Voltage, $V_{CC}$	3 v to 4 v
Maximum Fan-out Into Positive Loads, $N^+$	10
Maximum Fan-out Into Negative Loads, $N^-$	10
Minimum Set-Up Time, $t_{set-up}^\dagger$	400 nsec

### electrical characteristics (unless otherwise noted $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ , $V_{CC} = 3\text{ v}$ to $4\text{ v}$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS <sup>‡</sup>	MIN	TYP	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at T or T* input	16	$V_{CC} = 3\text{ v}$	1.7		3	v
		$V_{CC} = 4\text{ v}$	2.4		4	v
$V_{in(0)}$ Input voltage required to ensure logical 0 at T or T* input	16		0		0.4	v
$V_{out(1)}$ Logical 1 output voltage (off level)	17	$V_{CC} = 3\text{ v}$ , $N^+ = 10$ ( $I_{load} = -5\text{ ma}$ )	1.7			v
		$V_{CC} = 4\text{ v}$ , $N^+ = 10$ ( $I_{load} = -8\text{ ma}$ )	2.6			v
$V_{out(0)}$ Logical 0 output voltage (on level)	17	$V_{CC} = 3\text{ v}$ , $V_{(2)} = 0.3\text{ v}$ , pin 10 open, $N^- = 10$ ( $I_{sink} = 2\text{ ma}$ )			0.3	v
		$V_{CC} = 4\text{ v}$ , $V_{(2)} = 0.3\text{ v}$ , pin 10 open, $N^- = 10$ ( $I_{sink} = 2\text{ ma}$ )			0.3	v
$I_{in}$ Input current (each input)	16	$V_{CC} = 3\text{ v}$ , $V_{in} = 1.7\text{ v}$ , $N^+ = N^- = 0$			0.5	ma
		$V_{CC} = 4\text{ v}$ , $V_{in} = 2.6\text{ v}$ , $N^+ = N^- = 0$			0.8	ma
$I_{CC(av)}$ Average supply current	18	$V_{CC} = 3\text{ v}$ , $N^+ = N^- = 0$ , Duty Cycle = 50%, $T_A = 25^\circ\text{C}$		4.8		ma
		$V_{CC} = 4\text{ v}$ , $N^+ = N^- = 0$ , Duty Cycle = 50%, $T_A = 25^\circ\text{C}$		6.3		ma

<sup>†</sup>This is the minimum time necessary for the input signal to dwell before the triggering transition begins and applies when pin 6 is shorted to pin 7 and pin 2 is shorted to pin 10. Set-up time begins only after the occurrence of the 10% point of the output fall time.

<sup>‡</sup>Pin 6 shorted to pin 7 and pin 2 shorted to pin 10 unless otherwise noted.

# TYPE SN7380

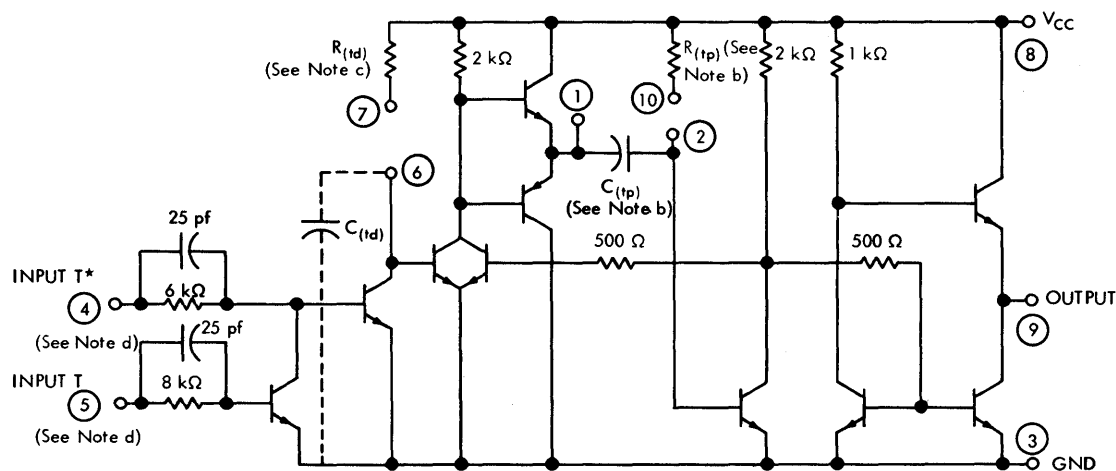
## ONE-SHOT MONOSTABLE MULTIVIBRATOR

switching times,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.5\text{ v}$ , fan-out  $N = 1$

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$t_{d1}$ Delay Time after Positive-going Transition at T (pin ⑤)	24	Input: $V_{in} = 2.5\text{ v}$ , $f = 1\text{ Mc}$ , $t_p = 400\text{ nsec}$ , $t_r = t_f = 20\text{ nsec}$		90	130	nsec
$t_{d2}$ Delay Time after Negative-going Transition at T* (pin ④)				90	130	nsec
$t_r$ Rise Time				35	60	nsec
$t_f$ Fall Time				35	60	nsec
$t_p$ Output Pulse Width	24	Input: $V_{in} = 2.5\text{ v}$ , $f = 1\text{ Mc}$ , $t_p = 400\text{ nsec}$ , $t_r = t_f = 20\text{ nsec}$	100	250	400	nsec

†Pin ⑥ shorted to pin ⑦ and pin ② shorted to pin ⑩ unless otherwise noted.

### schematic



NOTES: a. Component values shown are nominal.

b. Output pulse width  $t_p$  is proportional to  $R_{(tp)}C_{(tp)}$ . Output pulse width may be modified using pins ①, ②, ⑧, and ⑩ to change effective values of  $R_{(tp)}$  and  $C_{(tp)}$ . Nominal value of internal  $R_{(tp)}$  is  $8\text{ k}\Omega$  and  $C_{(tp)}$  is  $25\text{ pf}$ . Value of modified  $R_{(tp)}$  should be maintained between  $6\text{ k}\Omega$  and  $15\text{ k}\Omega$ .

#### CAUTION:

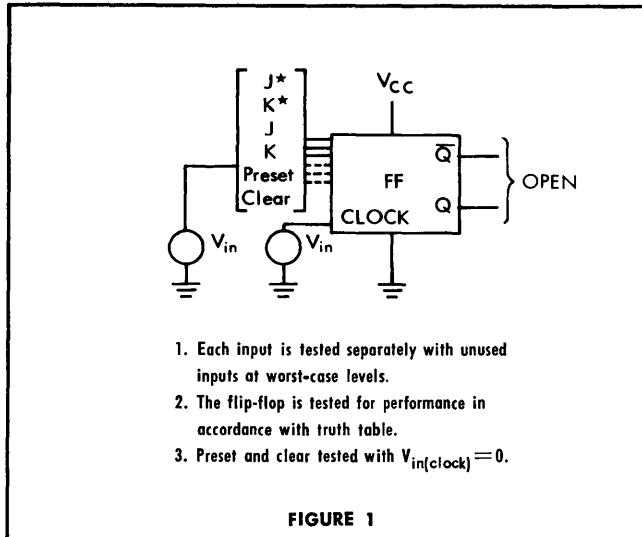
When the effective value of  $C_{(tp)} \geq 0.1\text{ }\mu\text{f}$ , a  $560\text{-}\Omega$  resistor must be connected in series with the external portion of  $C_{(tp)}$  (between pins ① and ②).

c. Delay time ( $t_d$ ) may be modified using pins ③, ④, ⑦, and ⑧ to change effective values of  $R_{(td)}$  and  $C_{(td)}$ . Nominal value of internal  $R_{(td)}$  is  $2\text{ k}\Omega$ . Value of modified  $R_{(td)}$  should be maintained between  $2\text{ k}\Omega$  and  $10\text{ k}\Omega$ .

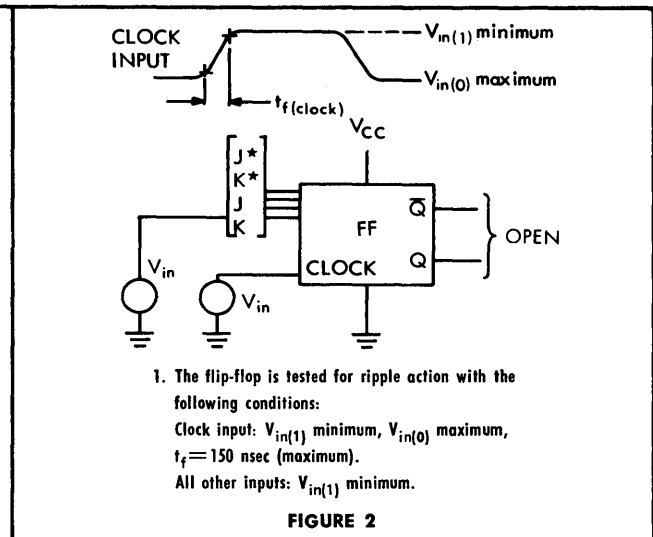
d. T triggers on a positive transition to logical 1 level, and T\* triggers on a negative transition to logical 0 level. When triggering with T input, hold T\* at logical 1. When triggering with T\* input, hold T at logical 0.

**PARAMETER MEASUREMENT INFORMATION §**

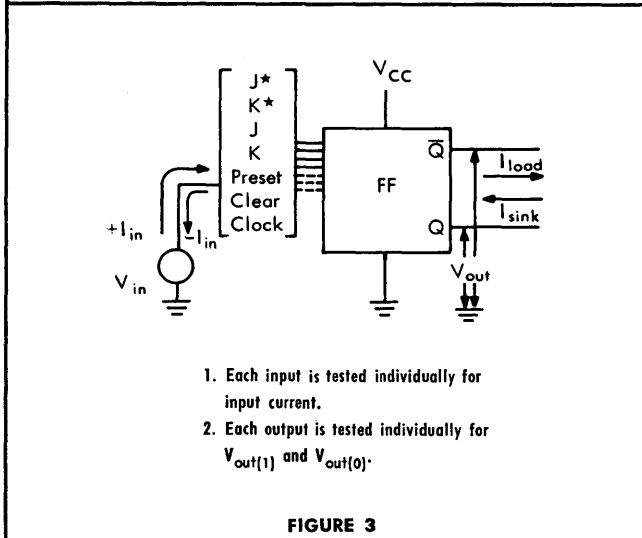
**d-c test circuits**



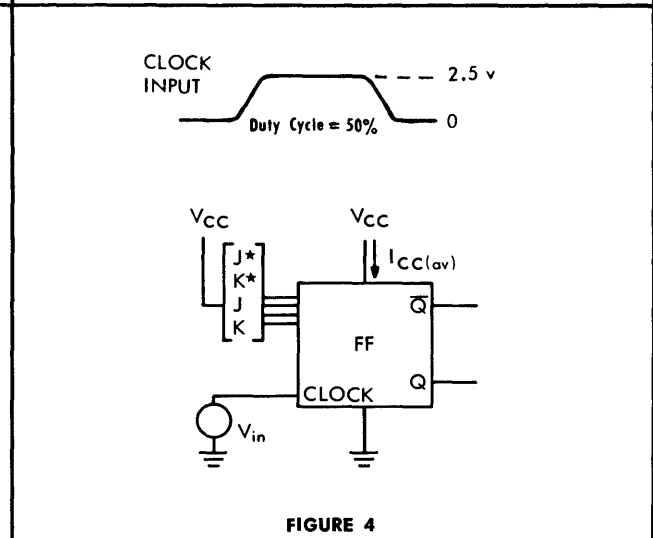
**FIGURE 1**



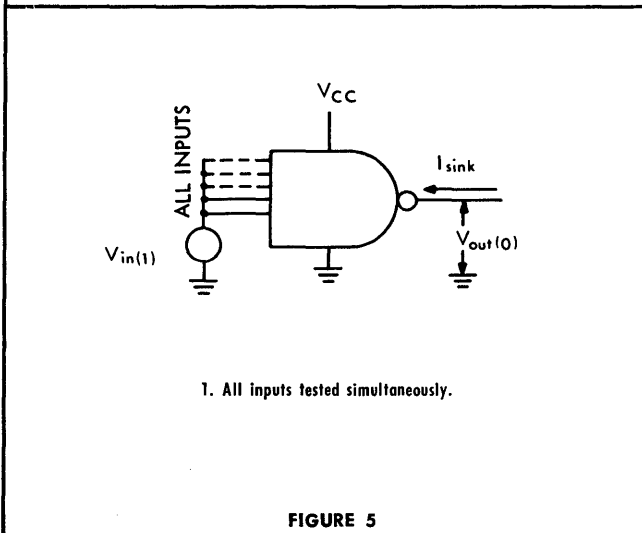
**FIGURE 2**



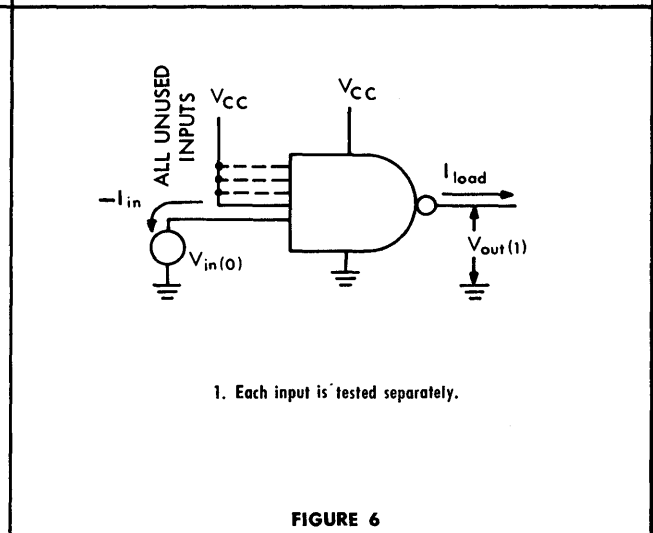
**FIGURE 3**



**FIGURE 4**



**FIGURE 5**



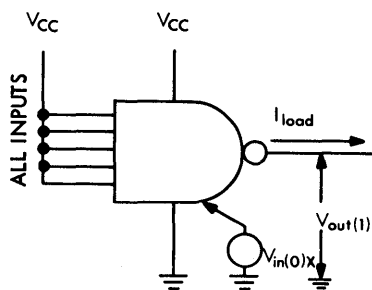
**FIGURE 6**

§ Arrows indicate actual direction of current flow.

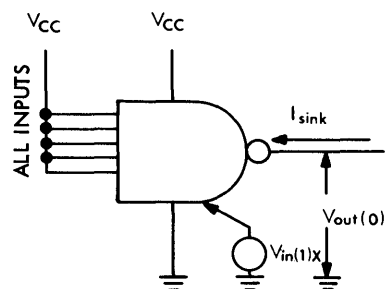


**PARAMETER MEASUREMENT INFORMATION§**

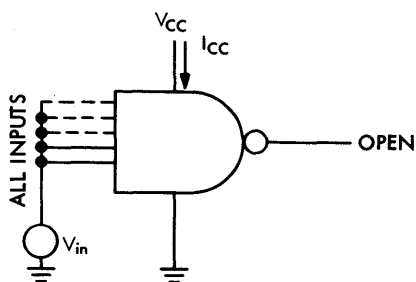
**d-c test circuits (continued)**



**FIGURE 7**

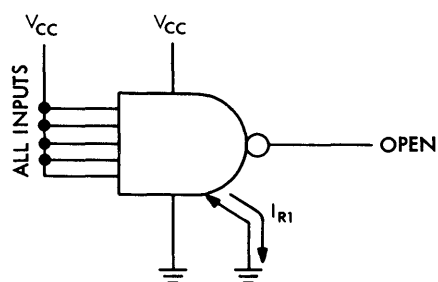


**FIGURE 8**



1. Test on-level and off-level current.

**FIGURE 9**



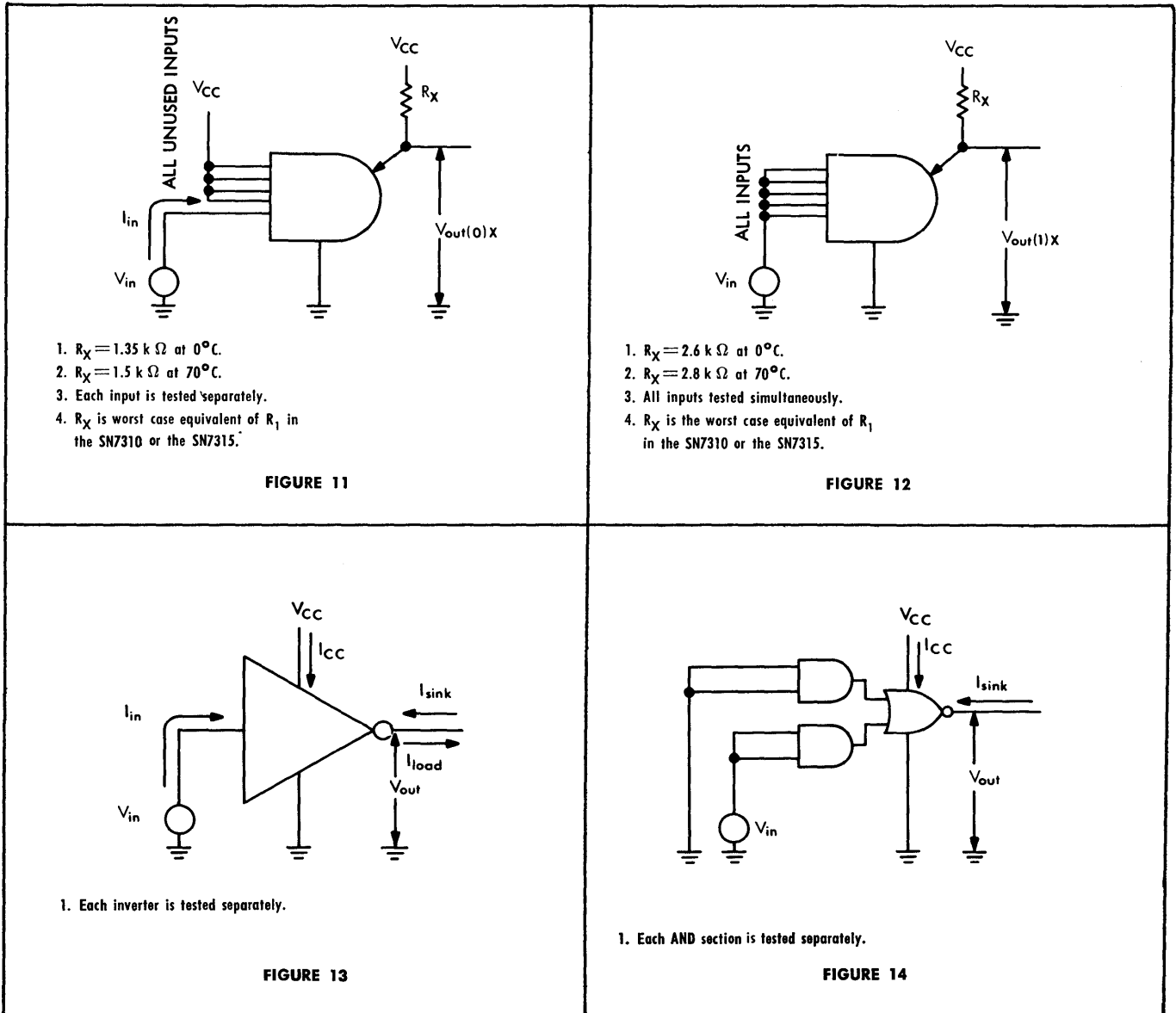
$$1. R_{1(off)} = \frac{V_{CC}}{I_{R1}}$$

**FIGURE 10**

§ Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION<sup>§</sup>**

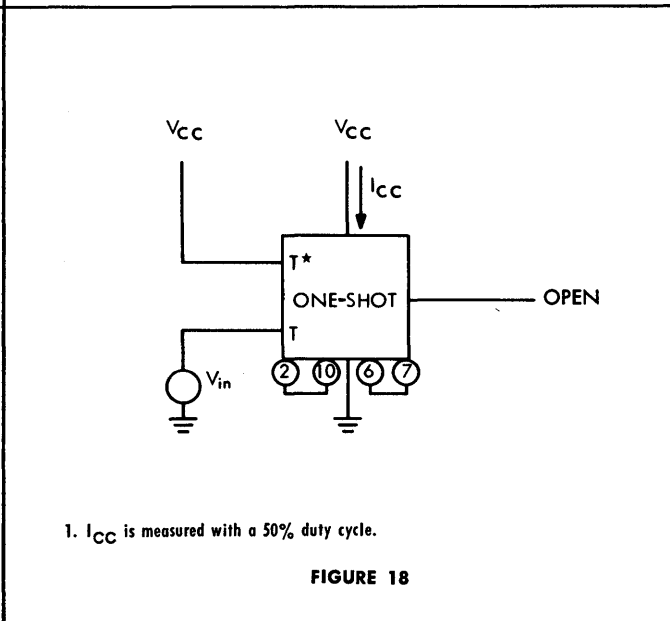
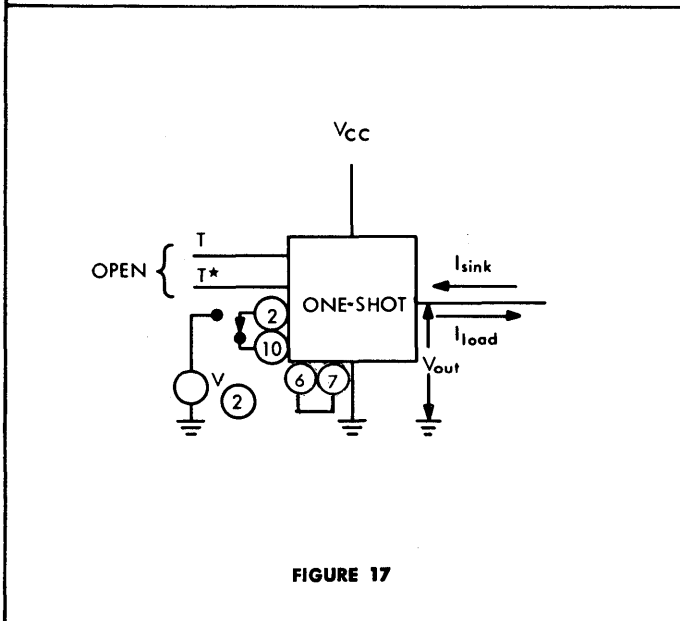
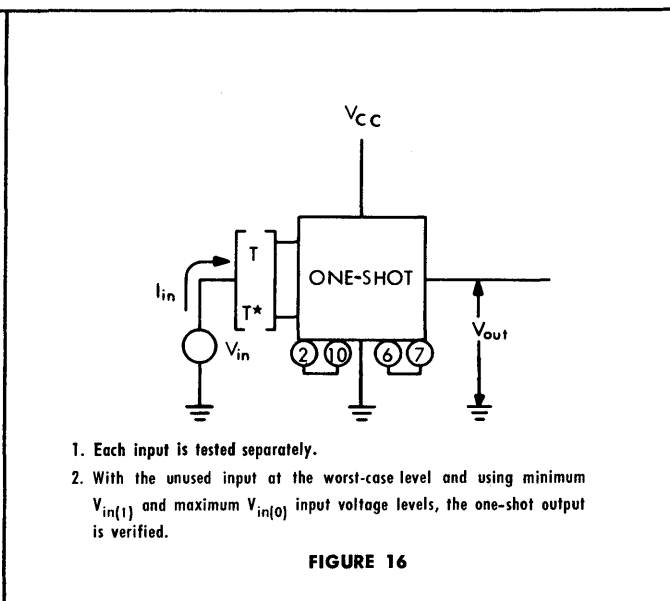
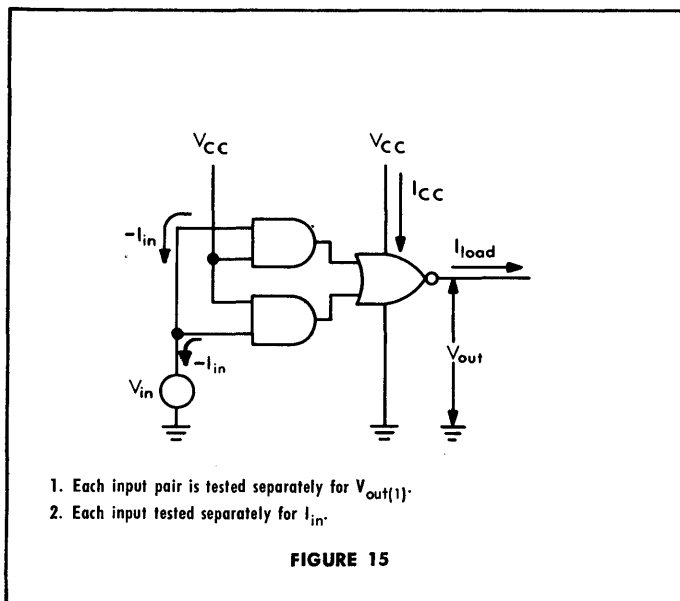
**d-c test circuits (continued)**



<sup>§</sup> Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION<sup>§</sup>

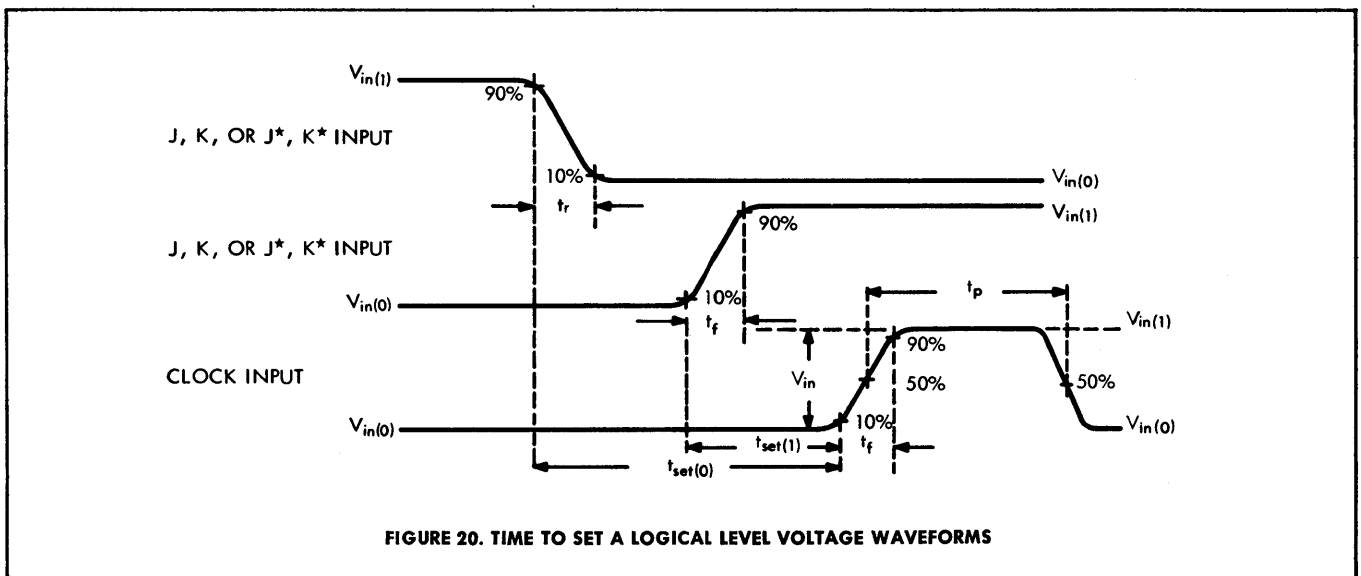
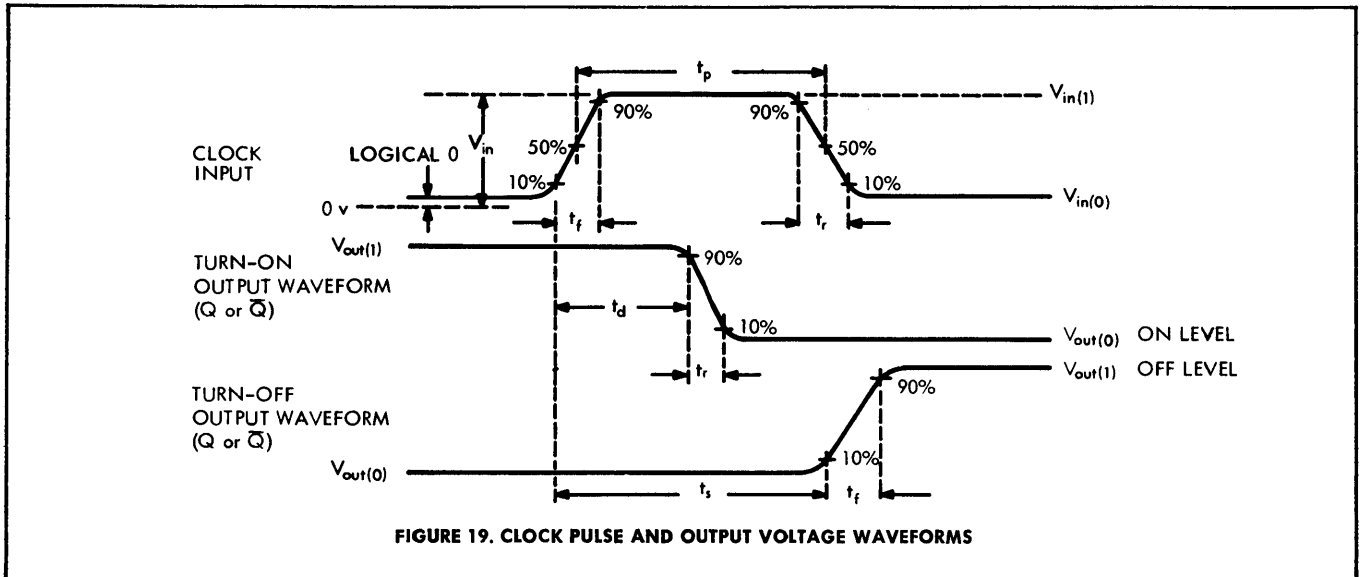
d-c test circuits (continued)



<sup>§</sup> Arrows indicate actual direction of current flow.

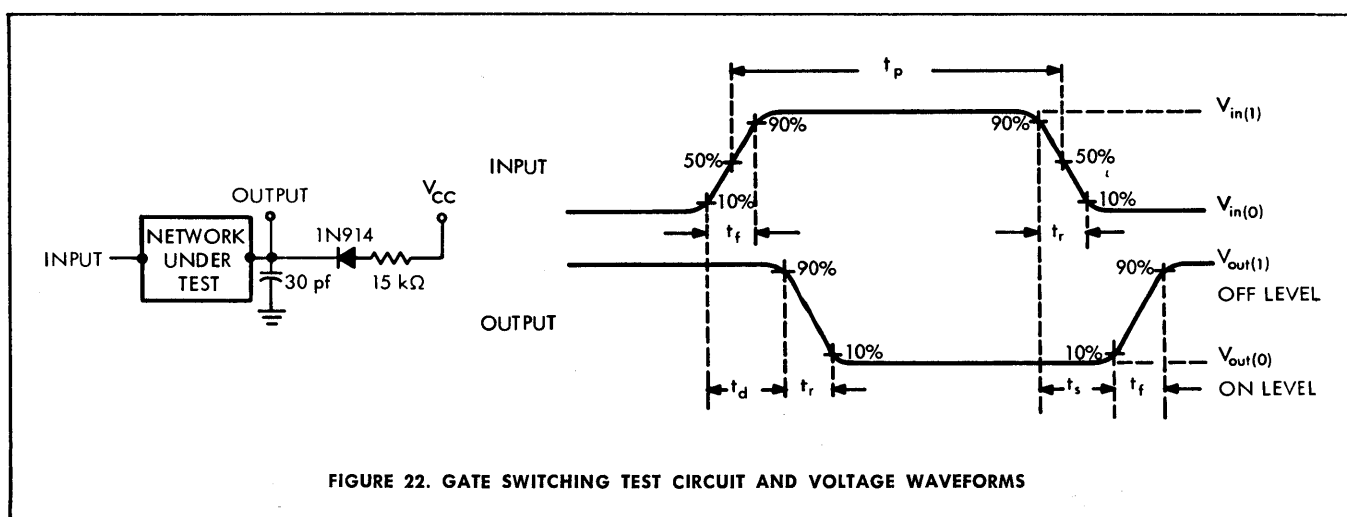
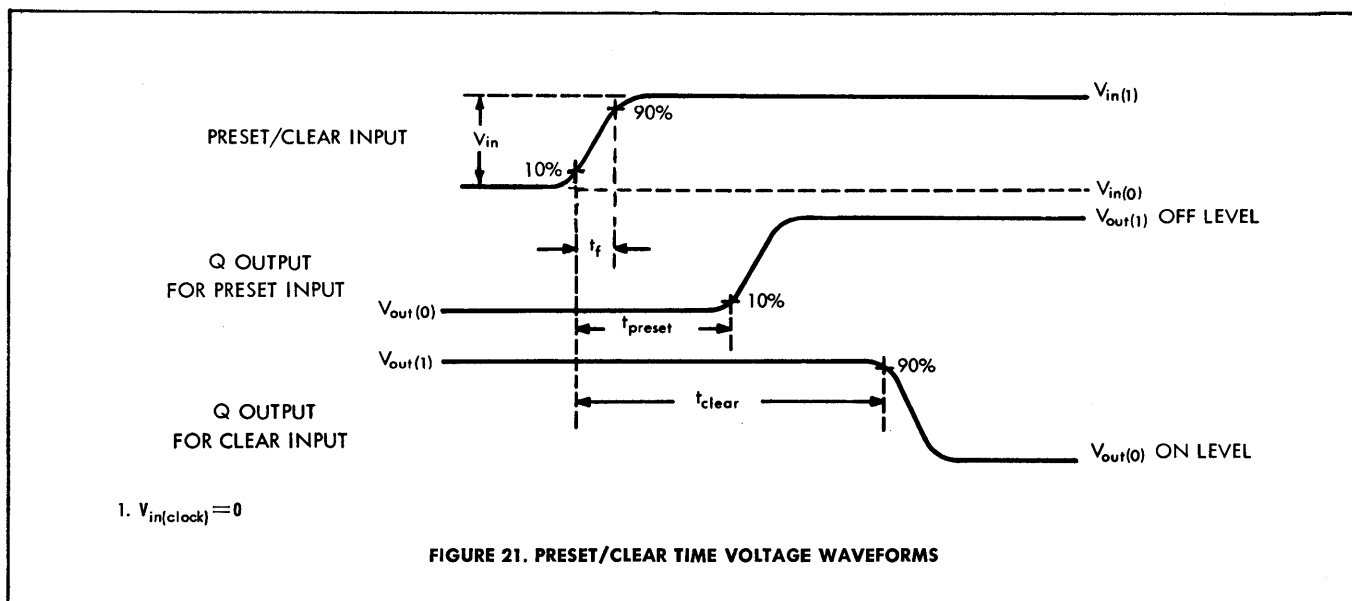
**PARAMETER MEASUREMENT INFORMATION**

**switching characteristics**



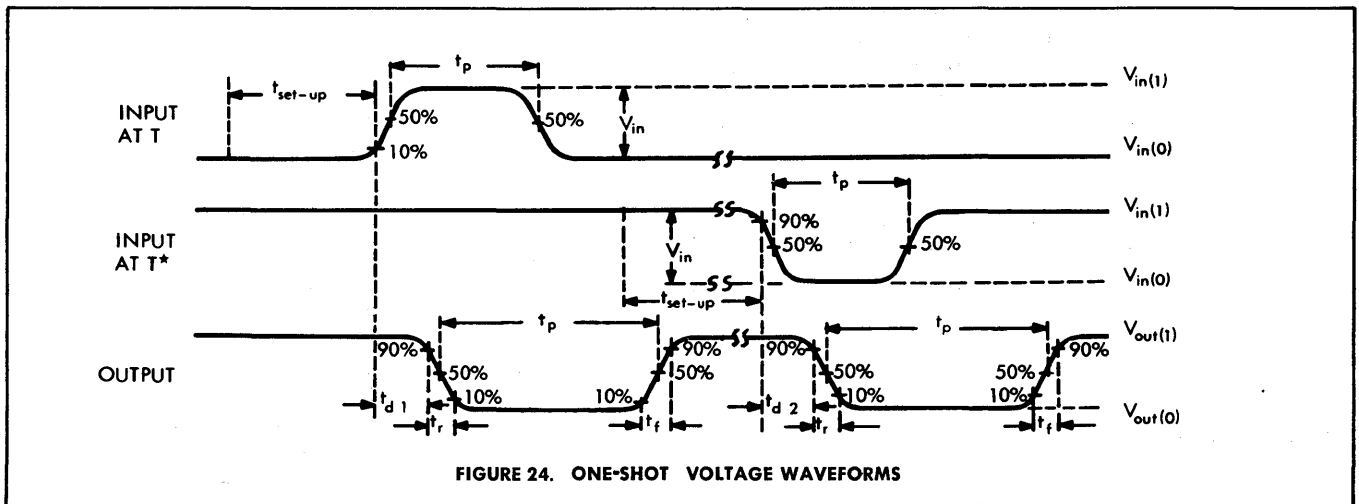
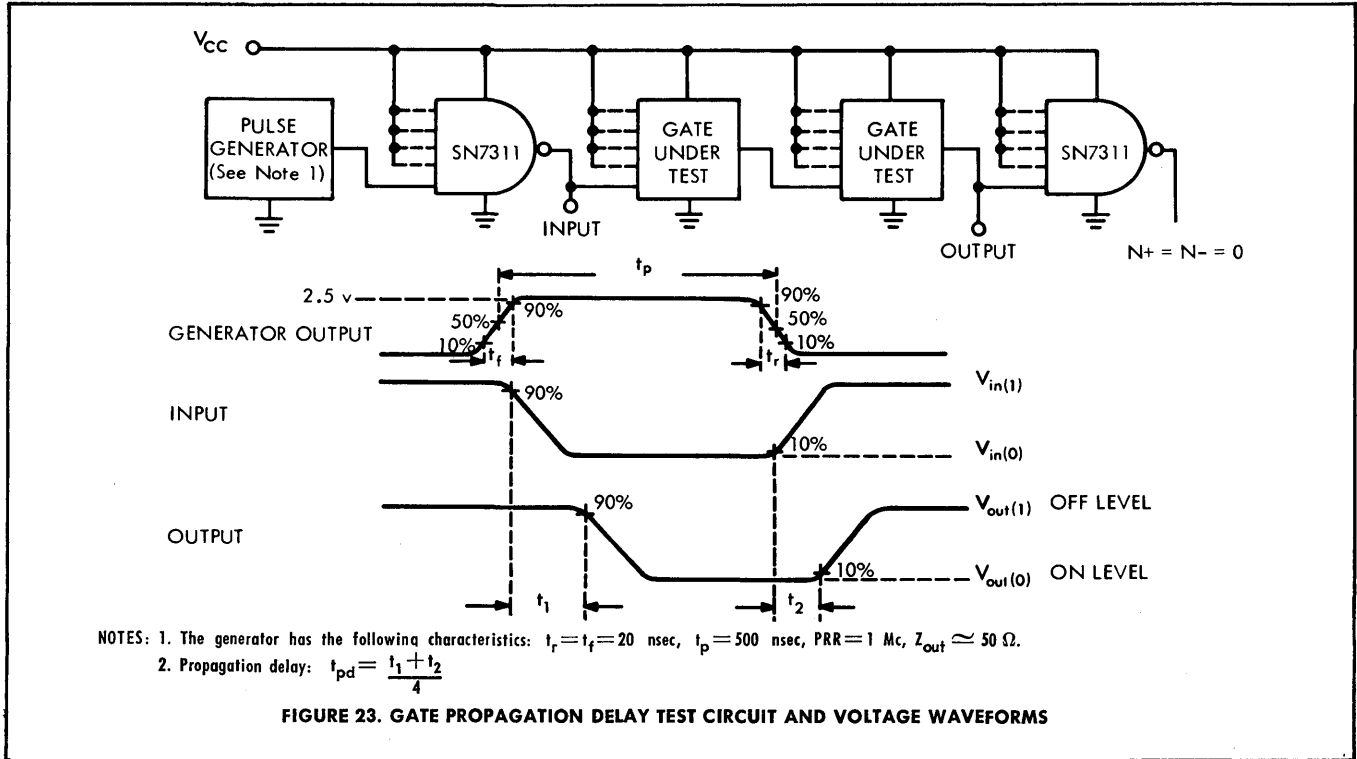
**PARAMETER MEASUREMENT INFORMATION**

**switching characteristics (continued)**



**PARAMETER MEASUREMENT INFORMATION**

**switching characteristics (continued)**



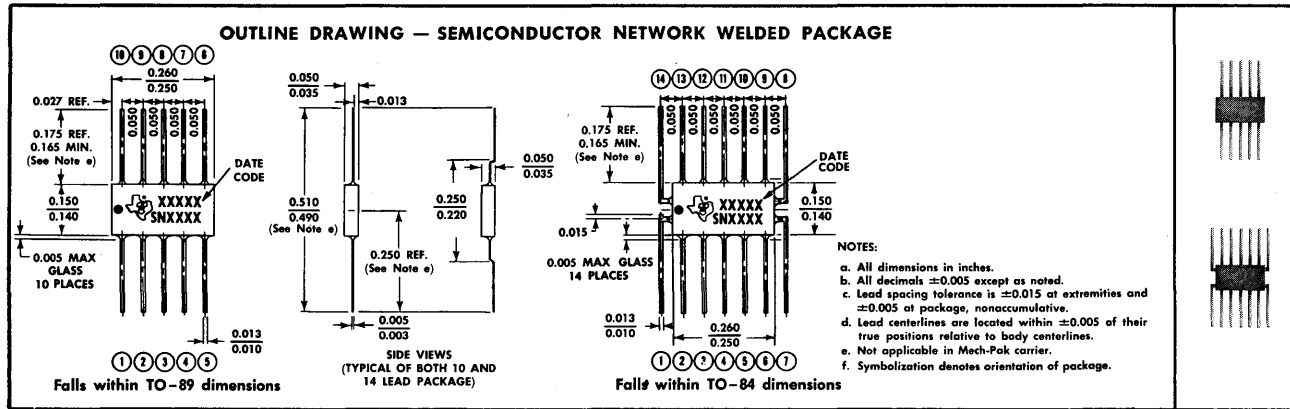
# SERIES 73 SOLID CIRCUIT<sup>®</sup> SEMICONDUCTOR NETWORKS<sup>†</sup>

## MECHANICAL DATA

### general

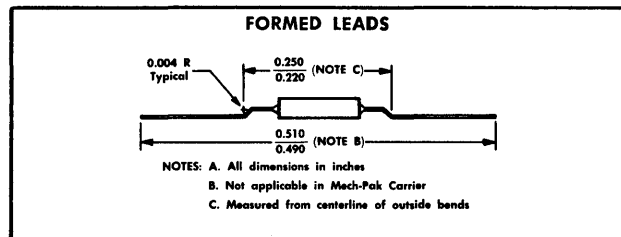
Series 73 semiconductor networks are mounted in glass-to-metal hermetically sealed, welded packages. Package body and leads are gold-plated F-15<sup>‡</sup> glass-sealing alloy. Approximate weight is

0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. All Series 73 networks are available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier.



### leads

Gold-plated F-15<sup>‡</sup> leads require no additional cleaning or processing when used in soldered or welded assembly. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Standard lead length is 0.175 inches. Networks can be removed from Mech-Pak carriers with lead lengths up to 0.175 inches.

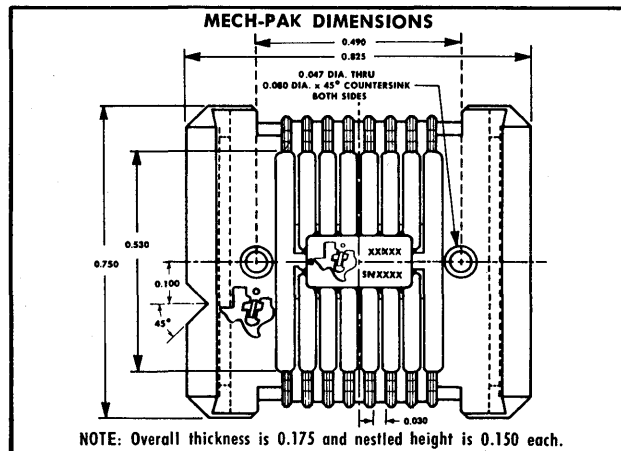


### insulator

An insulator, secured to the back surface of the package, permits mounting networks on circuit boards which have conductors passing beneath the package. The insulator is 0.0025 inch thick and has an insulation resistance of greater than 10 megohms at 25°C.

### mech-pak carrier

The Mech-Pak carrier facilitates handling the network, and is compatible with automatic equipment used for testing and assembly. The carrier is particularly appropriate for mechanized assembly operations and will withstand temperatures of 125°C for indefinite periods.



### ordering instructions

Variations in mechanical configuration of semiconductor networks are identified by suffix numbers shown in a table at the right.

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5

<sup>†</sup>Patented by Texas Instruments

<sup>‡</sup>F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.



**DIODE-TRANSISTOR LOGIC (DTL) NETWORKS  
FOR DIGITAL SYSTEMS**

**application**

The series 15 830 networks are designed for use in medium to high-speed digital applications, including data handling, computer and control systems. Definitive specifications are provided for operating characteristics over the temperature range of 0°C to 75°C.

**features**

**LOW SYSTEM COST**

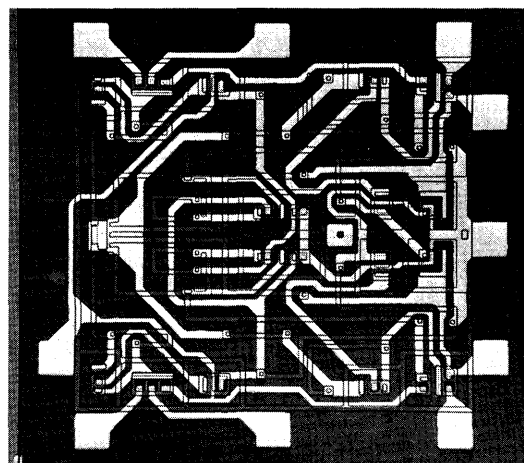
- multifunction gates offering low cost per logic function
- electrically designed specifically for monolithic integrated-circuit technology

**PERFORMANCE**

- high speed
- high d-c noise margins
- low power dissipation
- good fan-out capability

**EASE OF DESIGN**

- familiar logic configuration (DTL)
- single-ended output — dot-OR logic
- complete family for design flexibility
- single power supply



**TYPE SN15 850 PULSE-TRIGGERED BINARY BAR**

**description**

Series 15 830 is a complete family of diode-transistor logic (DTL) which is most attractive when high performance and low cost per function are necessities to system design.

The basic family consists of NAND gates, an expander, a buffer, a power gate, master-slave flip-flops, a pulse-triggered binary and a monostable multivibrator. Dual, triple, and quadruple multifunction gates are available to minimize system package count.

This line features a unique combination of high speed, high d-c noise margin, and low power dissipation. The single-ended output lends itself readily to performing dot-OR logic thus reducing the number of different type functional blocks in a system.

CONTENTS	Page
DESIGN CHARACTERISTICS AND LOGICAL SYMBOLS . . . . .	7002-7003
LOADING TABLES . . . . .	7004
DEFINITIVE SPECIFICATIONS . . . . .	7005-7027
D-C TEST CIRCUITS . . . . .	7028-7036
SWITCHING TIME CIRCUITS AND VOLTAGE WAVEFORMS . . . . .	7036-7039
MECHANICAL AND PACKAGING DATA . . . . .	7040

<sup>†</sup>Patented by Texas Instruments



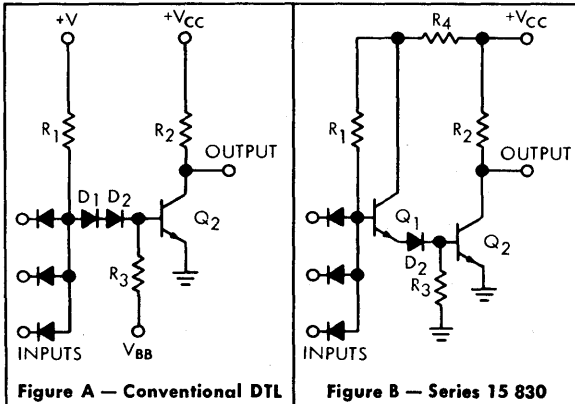


typical operating characteristics,  $T_A = 0^\circ\text{C}$  to  $75^\circ\text{C}$ , supply voltage  $V_{CC} = 5\text{ V}$

Speed: Gate Propagation Delay . . . . .	25 ns
Monostable Multivibrator Propagation Delay . . . . .	20 ns
Flip-Flop Clock Rate (SN15 831, SN15 845, SN15 848) . . . . .	7 MHz
Pulse-Triggered Binary Clock Rate . . . . .	20 MHz
Fan-Out Capability: Standard Gates (SN15 830, SN15 846, SN15 862) . . . . .	8
Buffer (SN15 832) . . . . .	25
Power Gate (SN15 844) . . . . .	27
Monostable Multivibrator (SN15 851) . . . . .	10
Flip-Flops: SN15 831 . . . . .	7
SN15 845 . . . . .	12
SN15 848 . . . . .	11
Pulse-Triggered Binary . . . . .	10
D-C Margin: At logical 1 . . . . .	500 mV
At logical 0 . . . . .	500 mV
Average Power Dissipation: Per Gate . . . . .	5 mW
Per Flip-Flop . . . . .	20 mW

**design characteristics**

Series 15 830 is a complete line of high-speed, high-noise-margin, low-power-dissipation, saturated DTL logic. The circuitry is a modification of the conventional DTL in that it utilizes only one power supply and provides a nonsaturating offset transistor in place of one of the offset diodes.



Replacing the offset diode  $D_1$  with transistor  $Q_1$  offers both the manufacturer and the customer a number of advantages:

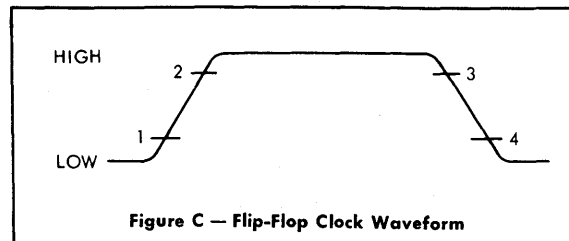
1. Elimination of the  $V_{BB}$  power supply makes one more pin available for multifunction capability, which in turn reduces system package count.
2. Reduction of size of resistor  $R_3$  from  $20\text{ k}\Omega$  to  $5\text{ k}\Omega$  produces a substantial reduction in the overall size of the monolithic chip and improves yields. Both of these factors contribute heavily to reducing manufacturing costs.
3. Reduction of turn-off current transients on signal lines is accomplished because the stored charge on the output transistor  $Q_2$  is removed locally by  $R_3$  rather than through diodes  $D_1$  and  $D_2$  onto the input signal lines. These transients are also reduced during switching by the offset transistor  $Q_1$  which operates in the unsaturated mode. This technique eliminates the necessity of producing low-speed, high-stored-charge diodes in the same monolithic bar with fast input diodes.

4. The offset transistor  $Q_1$  provides additional drive current to the output transistor  $Q_2$  without requiring high input currents when the input is in the low state. High input currents would limit fan-out of the driving gates. The additional drive to the output transistor permits the use of a smaller base resistor  $R_3$  and relaxes the  $h_{FE}$  requirement of the output transistor thus producing higher manufacturing yields.

In order to drive high-fan-out or high-capacity loads, a buffer is available which has a modified double-ended output. This output has a high-sink-current capability when in the ON state and a low-impedance emitter-follower output in the OFF state.

The master-slave flip-flops have AND gate inputs to the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows (see figure C):

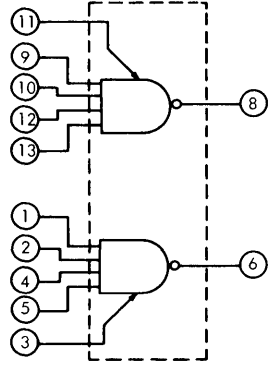
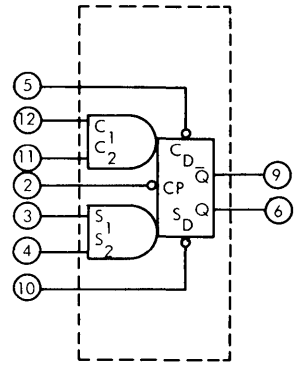
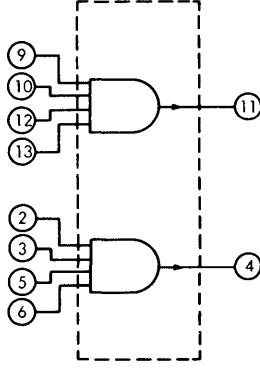
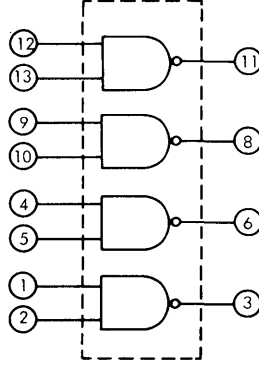
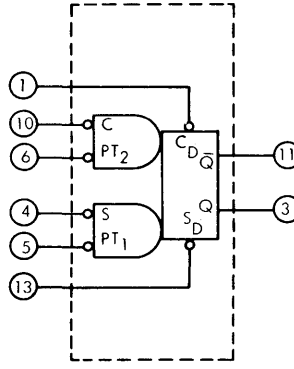
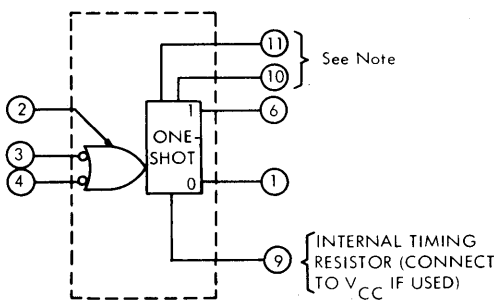
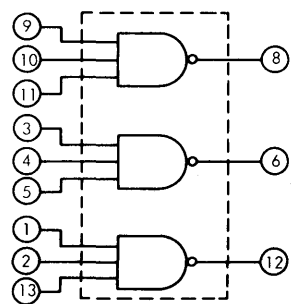
1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.



The pulse-triggered binary has two  $70\text{-pF}$  capacitors in the clock line which provide an input-differentiating network for high-speed clocking applications.

### standard line summary

Input and output pin numbers are shown for reference. For all networks shown,  $V_{CC}$  is pin (14) (unless otherwise noted) and GND is pin (7). See referenced page for complete pin configuration.

<p><b>SN15 830</b> . . . . . See Page 7005  <b>SN15 832 (Buffer)</b> . . . . . See Page 7009  <b>SN15 844 (Power Gate)</b>. . . . . See Page 7012</p>  <p style="text-align: center;"><b>DUAL 4-INPUT NAND/NOR GATES</b></p>	<p><b>SN15 831</b> . . . . . See Page 7007  <b>SN15 845</b> . . . . . See Page 7014  <b>SN15 848</b> . . . . . See Page 7019</p>  <p style="text-align: center;"><b>FLIP-FLOPS WITH SET AND CLEAR</b></p>	
<p><b>SN15 833</b> . . . See Page 7011          (No <math>V_{CC}</math> Terminal)</p>  <p style="text-align: center;"><b>DUAL 4-INPUT EXPANDER</b></p>	<p><b>SN15 846</b> . . . See Page 7017</p>  <p style="text-align: center;"><b>QUADRUPLE 2-INPUT NAND/NOR GATE</b></p>	<p><b>SN15 850</b> . . . See Page 7022</p>  <p style="text-align: center;"><b>PULSE-TRIGGERED BINARY</b></p>
<p><b>SN15 851</b> . . . . . See Page 7024</p>  <p style="text-align: center;"><b>MONOSTABLE MULTIVIBRATOR</b></p>	<p><b>SN15 862</b> . . . . . See Page 7026</p>  <p style="text-align: center;"><b>TRIPLE 3-INPUT NAND/NOR GATE</b></p>	

# SERIES 15 830

## SOLID CIRCUIT<sup>®</sup> SEMICONDUCTOR NETWORKS

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage $V_{CC}$ (See Note 1)	+8 V
Continuous Output Sink Current (SN15 830, SN15 831, SN15 845, SN15 846, SN15 848, SN15 862)	30 mA
Continuous Output Sink Current (SN15 850, SN15 851)	50 mA
Continuous Output Sink Current (SN15 832, SN15 844)	150 mA
Current Out of Input Terminal	-10 mA
Current Into Input Terminal (except SN15 850 and SN15 851 pin ⑩)	1 mA
Current Into Input Terminal (SN15 850 and SN15 851 pin ⑩)	5 mA
Operating Free-Air Temperature Range (See Note 2)	0°C to 75°C
Storage Temperature Range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. This rating applies for networks operating at  $V_{CC} = 5$  V, all inputs† at 5 V, and the following output sink current:

SN15 830†, SN15 846, SN15 850, SN15 862	12 mA
SN15 831	10.5 mA
SN15 832†	36 mA
SN15 844†	40 mA
SN15 845	16.8 mA
SN15 848	14.6 mA
SN15 851	15 mA

† Expander nodes open

### logic definition

Series 15 830 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE = LOGICAL 0  
HIGH VOLTAGE = LOGICAL 1

### input current requirements

Weighted values of input current requirements reflect worst case conditions for  $T_A = 0^\circ\text{C}$  to  $75^\circ\text{C}$  and  $V_{CC} = 5$  V. Each gate input requires that no more than -1.4 mA flow out of the input at a logical 0 input voltage level; therefore, one input load is -1.4 mA maximum. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

WEIGHTED VALUES OF INPUT CURRENT REQUIREMENTS			
NETWORK	TYPE	INPUT	NUMBER OF LOADS
GATES AND EXPANDER	SN15 830	Each Input	1
	SN15 832		
	SN15 833		
	SN15 844		
	SN15 846		
FLIP-FLOPS	SN15 831	Each Input (Synchronous or Asynchronous)	3/8
		Clock	2
	SN15 845 and SN15 848	Synchronous Inputs	3/8
		Asynchronous and Clock Inputs	2
PULSE-TRIGGERED BINARY	SN15 850	Synchronous or Asynchronous	11 1/2
MONOSTABLE MULTIVIBRATOR	SN15 851	Each Input	2

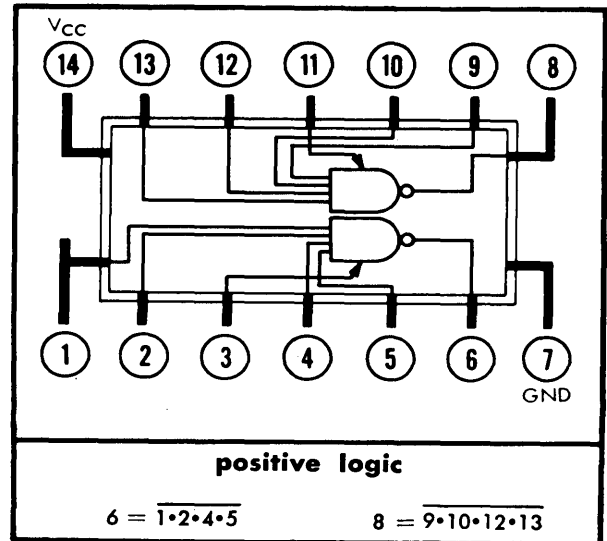
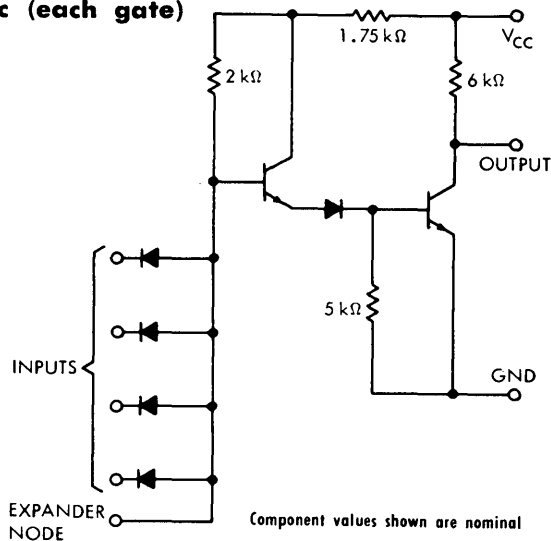
### output drive capability

Weighted values of fan-out reflect the ability of an output to sink current (into the output terminal) under recommended operating conditions and are specified as positive values. Load currents (out of the output terminal) are specified as negative values. Arrows on the d-c test circuits indicate the actual direction of current flow.

WEIGHTED VALUES OF FAN-OUT			
NETWORK	TYPE	OUTPUT	LOADS
GATES	SN15 830	Each Output	8
	SN15 846		
	SN15 862		
BUFFER	SN15 832	Each Output	25
POWER GATE	SN15 844	Each Output	27
FLIP-FLOPS	SN15 831	Q or $\bar{Q}$	7
	SN15 845	Q or $\bar{Q}$	12
	SN15 848	Q or $\bar{Q}$	11
PULSE-TRIGGERED BINARY	SN15 850	Q or $\bar{Q}$	8
MONOSTABLE MULTIVIBRATOR	SN15 851	Each Output	10

# TYPE SN15 830 DUAL 4-INPUT NAND/NOR GATE

schematic (each gate)



### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	5 V
Maximum Fan-Out From Each Output . . . . .	8

### electrical characteristics at $V_{CC} = 5 V$

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{out(0)}$ Logical 0 output voltage (on level)	1	$V_{in} = 1.9 V, I_{sink} = 12 mA,$ $T_A = 25^\circ C$		0.45	V
		$V_{in} = 2 V, I_{sink} = 12 mA,$ $T_A = 0^\circ C$		0.45	V
		$V_{in} = 1.8 V, I_{sink} = 11.4 mA,$ $T_A = 75^\circ C$		0.5	V
$V_{out(1)}$ Logical 1 output voltage (off level)	2	$V_{in} = 1.1 V, I_{load} = -0.12 mA,$ $T_A = 25^\circ C$	2.6		V
		$V_{in} = 1.2 V, I_{load} = -0.12 mA,$ $T_A = 0^\circ C$	2.6		V
		$V_{in} = 0.95 V, I_{load} = -0.12 mA,$ $T_A = 75^\circ C$	2.5		V

† Expander nodes are open unless otherwise noted.

# TYPE SN15 830

## DUAL 4-INPUT NAND/NOR GATE

electrical characteristics (continued) at  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{out(1)}$ Logical 1 output voltage (off level) with low voltage at expander input node, $V_{inX}$	3	$V_{inX} = 1.8\text{ V}$ , $I_{load} = -0.12\text{ mA}$ , $T_A = 25^\circ\text{C}$	2.6		V
$I_{in(1)}$ Logical 1 level input current	4	$V_{in} = 4\text{ V}$ , $T_A = 25^\circ\text{C}$ and $0^\circ\text{C}$		5	$\mu\text{A}$
		$V_{in} = 4\text{ V}$ , $T_A = 75^\circ\text{C}$		10	$\mu\text{A}$
$I_{in(0)}$ Logical 0 level input current	5	$V_{in} = 0.45\text{ V}$ , $V_R = 4\text{ V}$ , $T_A = 25^\circ\text{C}$ and $0^\circ\text{C}$		-1.4	mA
		$V_{in} = 0.5\text{ V}$ , $V_R = 4\text{ V}$ , $T_A = 75^\circ\text{C}$		-1.33	mA
$I_{out(1)}$ Output reverse current (off level)	6	$V_{out} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$		100	$\mu\text{A}$
$I_{OS}$ Short-circuit output current	7	$V_{out} = 0$ , $T_A = 25^\circ\text{C}$		-1.3	mA
		$V_{out} = 0$ , $T_A = 0^\circ\text{C}$		-1.3	mA
		$V_{out} = 0$ , $T_A = 75^\circ\text{C}$		-1.25	mA
$I_{CC(0)}$ Logical 0 level supply current (both gates)	8	$T_A = 25^\circ\text{C}$		8	mA
$I_{CC(1)}$ Logical 1 level supply current at maximum $V_{CC}$ (both gates)	9	$V_{CC} = 8\text{ V}$ , $T_A = 25^\circ\text{C}$		8	mA

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$t_{pd(0)}$ Propagation delay time to logical 0 level	51	$R_1 = 400\ \Omega$ , $C_L = 50\text{ pF}$	10	30	ns
$t_{pd(1)}$ Propagation delay time to logical 1 level		$R_1 = 3.9\text{ k}\Omega$ , $C_L = 30\text{ pF}$	25	80	ns

† Expander nodes are open unless otherwise noted.

# TYPE SN15 831 FLIP-FLOP WITH SET AND CLEAR

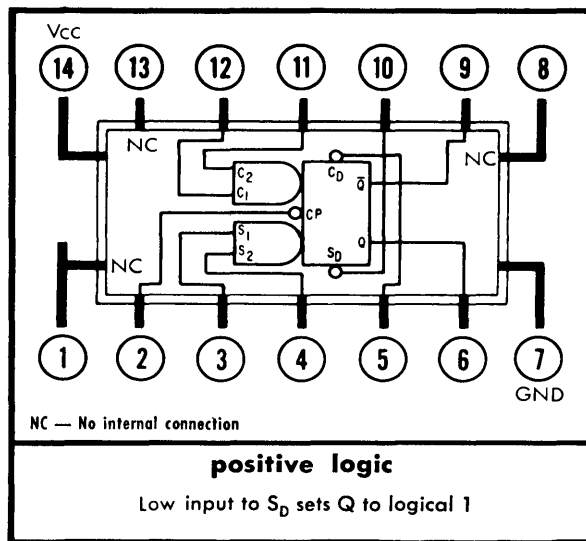
## logic

### TRUTH TABLES

R-S MODE					
$t_n$				$t_{n+1}$	
$S_1$	$S_2$	$C_1$	$C_2$	Q	
0	X	0	X	Q <sub>n</sub>	Q <sub>n</sub>
0	X	X	0	Q <sub>n</sub>	Q <sub>n</sub>
X	0	0	X	Q <sub>n</sub>	Q <sub>n</sub>
X	0	X	0	Q <sub>n</sub>	Q <sub>n</sub>
0	X	1	1	0	0
X	0	1	1	0	0
1	1	0	X	1	1
1	1	X	0	1	1
1	1	1	1	Indeterminate	

J-K MODE		
$t_n$		$t_{n+1}$
$S_1$	$C_1$	Q
0	0	Q <sub>n</sub>
0	1	0
1	0	1
1	1	$\bar{Q}_n$

- NOTES: 1.  $t_n$  = bit time before clock pulse.  
 2.  $t_{n+1}$  = bit time after clock pulse.  
 3. X indicates that either a logical 1 or a logical 0 may be present.  
 4. Logical 1 is more positive than logical 0.  
 5. For operation in the J-K mode connect  $S_2$  to  $\bar{Q}$  and  $C_2$  to Q.



### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	5 V
Maximum Fan-Out From Each Output . . . . .	7

### electrical characteristics at $V_{CC} = 5 V$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$ Logical 0 output voltage on level at Q or $\bar{Q}$	10	$V_{CP(S)} = 0.95 V, I_{sink} = 10.5 mA, T_A = 25^\circ C$		0.45	V
		$V_{CP(S)} = 1 V, I_{sink} = 10.5 mA, T_A = 0^\circ C$		0.45	V
		$V_{CP(S)} = 0.85 V, I_{sink} = 10.2 V, T_A = 75^\circ C$		0.5	V
$V_{out(1)}$ Logical 1 output voltage off level at Q or $\bar{Q}$	11	$V_1 = 1.9 V, V_2 = 1.1 V, I_{load} = -0.12 mA, T_A = 25^\circ C$	2.6		V
		$V_1 = 2 V, V_2 = 1.2 V, I_{load} = -0.12 mA, T_A = 0^\circ C$	2.6		V
		$V_1 = 1.8 V, V_2 = 0.95 V, I_{load} = -0.12 mA, T_A = 75^\circ C$	2.5		V
$V_{out(1)}$ Logical 1 output voltage off level at Q or $\bar{Q}$	12	$V_1 = 1.9 V, V_2 = 1.1 V, I_{load} = -0.12 mA, T_A = 25^\circ C$	2.6		V
		$V_1 = 2 V, V_2 = 1.2 V, I_{load} = -0.12 mA, T_A = 0^\circ C$	2.6		V
		$V_1 = 1.8 V, V_2 = 0.95 V, I_{load} = -0.12 mA, T_A = 75^\circ C$	2.5		V
$I_{CP(0)}$ Logical 0 level clock-input forward current	13	$V_{in} = 1.1 V, V_{CP(0)} = 0.45 V, T_A = 25^\circ C$		-2.8	mA
		$V_{in} = 1.2 V, V_{CP(0)} = 0.45 V, T_A = 0^\circ C$		-2.8	mA
		$V_{in} = 0.95 V, V_{CP(0)} = 0.5 V, T_A = 75^\circ C$		-2.67	mA
$I_{CP(1)}$ Logical 1 level clock-input reverse current	14	$V_{CP} = 4 V, T_A = 25^\circ C \text{ and } 0^\circ C$		30	$\mu A$
		$V_{CP} = 4 V, T_A = 75^\circ C$		40	$\mu A$

# TYPE SN15 831 FLIP-FLOP WITH SET AND CLEAR

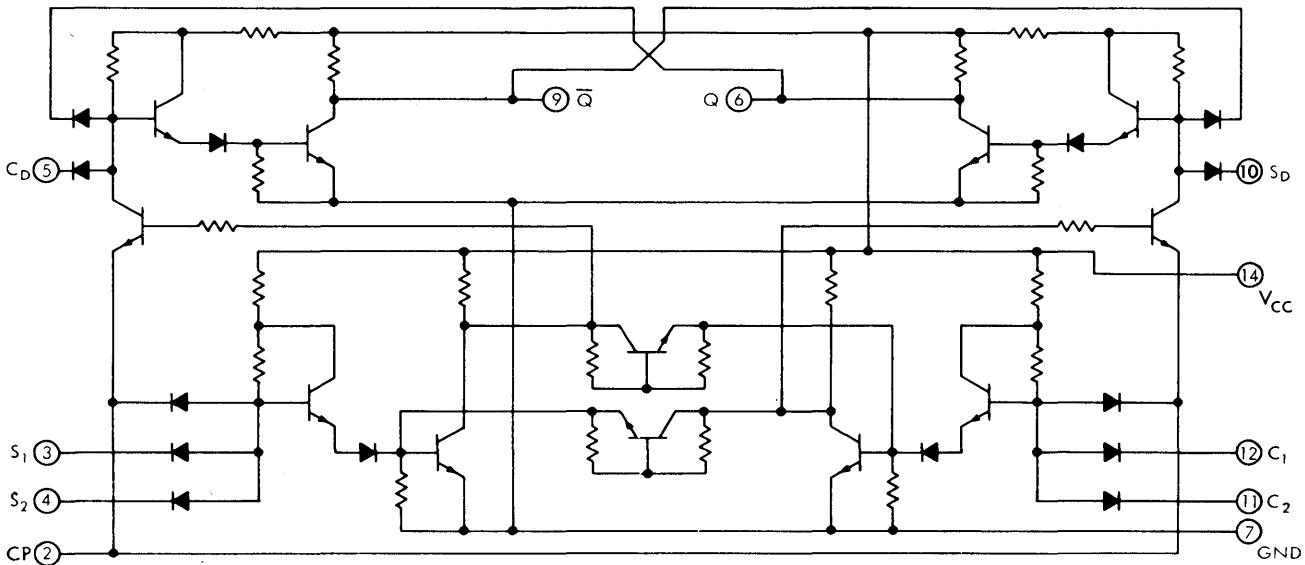
electrical characteristics (continued) at  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$ Logical 1 level synchronous-input current	15	$V_{in} = 4\text{ V}, T_A = 25^\circ\text{C and } 0^\circ\text{C}$		5	$\mu\text{A}$
		$V_{in} = 4\text{ V}, T_A = 75^\circ\text{C}$		10	$\mu\text{A}$
$I_{in(0)}$ Logical 0 level synchronous-input current	16	$V_{in} = 0.45\text{ V}, T_A = 25^\circ\text{C and } 0^\circ\text{C}$		-1.05	mA
		$V_{in} = 0.5\text{ V}, T_A = 75^\circ\text{C}$		-1	mA
$I_{in(1)}$ Logical 1 level asynchronous-input current	17	$V_{in} = 4\text{ V}, T_A = 25^\circ\text{C and } 0^\circ\text{C}$		5	$\mu\text{A}$
		$V_{in} = 4\text{ V}, T_A = 75^\circ\text{C}$		10	$\mu\text{A}$
$I_{in(0)}$ Logical 0 level asynchronous-input current	18	$V_{in} = 0.45\text{ V}, T_A = 25^\circ\text{C and } 0^\circ\text{C}$		-0.95	mA
		$V_{in} = 0.5\text{ V}, T_A = 125^\circ\text{C}$		-0.9	mA
$I_{CC(0)}$ Logical 0 level supply current	19	$T_A = 25^\circ\text{C}$		14	mA
$I_{CC(1)}$ Logical 1 level supply current at maximum $V_{CC}$	20	$V_{CC} = 8\text{ V}, T_A = 25^\circ\text{C}$		18	mA

switching characteristics,  $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$

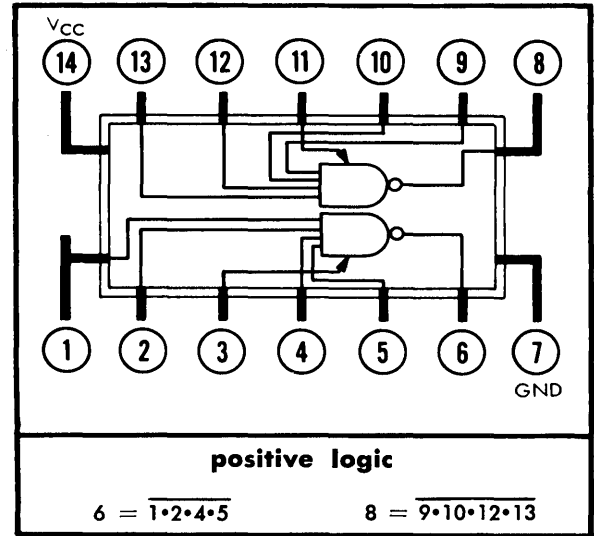
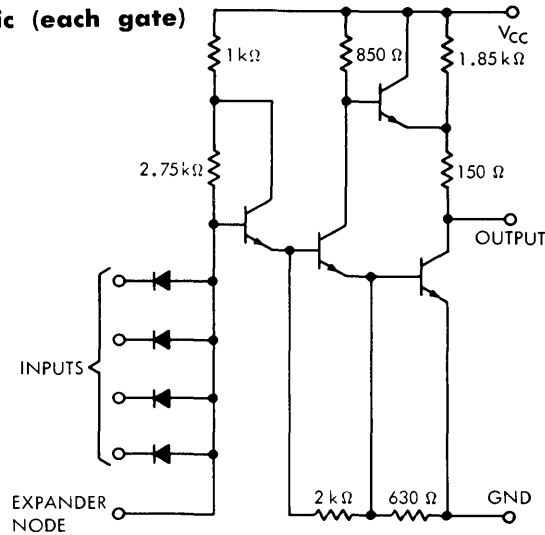
PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$ Propagation delay time to logical 0 level	52	$R_1 = 400\ \Omega, C_L = 50\text{ pF}$	5	75	ns
$t_{pd(1)}$ Propagation delay time to logical 1 level		$R_1 = 3.9\text{ k}\Omega, C_L = 30\text{ pF}$	5	75	ns

schematic



# TYPE SN15 832 DUAL 4-INPUT NAND/NOR BUFFER

schematic (each gate)



**recommended operating conditions**

Supply Voltage $V_{CC}$ . . . . .	5 V
Maximum Fan-Out From Each Output . . . . .	25

**electrical characteristics at  $V_{CC} = 5 V$**

PARAMETER	TEST FIGURE	TEST CONDITIONS †	MIN	MAX	UNIT
$V_{out(0)}$ Logical 0 output voltage (on level)	1	$V_{in} = 1.9 V, I_{sink} = 36 mA,$ $T_A = 25^\circ C$		0.45	V
		$V_{in} = 2 V, I_{sink} = 36 mA,$ $T_A = 0^\circ C$		0.45	V
		$V_{in} = 1.8 V, I_{sink} = 34 mA,$ $T_A = 75^\circ C$		0.5	V
$V_{out(1)}$ Logical 1 output voltage (off level)	2	$V_{in} = 1.1 V, I_{load} = -2.5 mA,$ $T_A = 25^\circ C$	2.6		V
		$V_{in} = 1.2 V, I_{load} = -2 mA,$ $T_A = 0^\circ C$	2.6		V
		$V_{in} = 0.95 V, I_{load} = -3 mA,$ $T_A = 75^\circ C$	2.5		V

† Expander nodes are open unless otherwise noted.



# TYPE SN15 832

## DUAL 4-INPUT NAND/NOR BUFFER

electrical characteristics (continued) at  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{out(1)}$ Logical 1 output voltage (off level) with low voltage input at expander node, $V_{inX}$	3	$V_{inX} = 1.8\text{ V}$ , $I_{load} = -2.5\text{ mA}$ , $T_A = 25^\circ\text{C}$	2.6		V
$I_{in(1)}$ Logical 1 level input current	4	$V_{in} = 4\text{ V}$ , $T_A = 25^\circ\text{C}$ and $0^\circ\text{C}$		5	$\mu\text{A}$
		$V_{in} = 4\text{ V}$ , $T_A = 75^\circ\text{C}$		10	$\mu\text{A}$
$I_{in(0)}$ Logical 0 level input current	5	$V_{in} = 0.45\text{ V}$ , $V_R = 4\text{ V}$ , $T_A = 25^\circ\text{C}$ and $0^\circ\text{C}$		-1.4	mA
		$V_{in} = 0.5\text{ V}$ , $V_R = 4\text{ V}$ , $T_A = 75^\circ\text{C}$		-1.33	mA
$I_{out(1)}$ Output reverse current (off level)	6	$V_{out} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$		100	$\mu\text{A}$
$I_{OS}$ Short-circuit output current	7	$V_{out} = 0$ , $T_A = 25^\circ\text{C}$		-16	mA
		$V_{out} = 0$ , $T_A = 0^\circ\text{C}$		-15	mA
		$V_{out} = 0$ , $T_A = 75^\circ\text{C}$		-14	mA
$I_{CC(0)}$ Logical 0 level supply current (both gates)	8	$T_A = 25^\circ\text{C}$		30	mA
$I_{CC(1)}$ Logical 1 level supply current at maximum $V_{CC}$ (both gates)	9	$V_{CC} = 8\text{ V}$ , $T_A = 25^\circ\text{C}$		8	mA

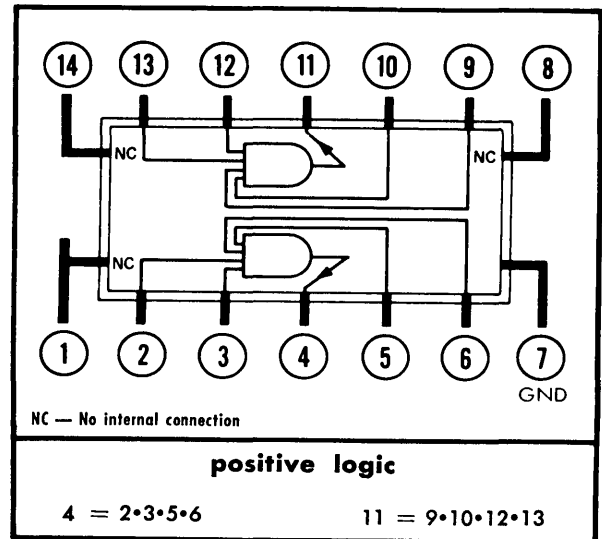
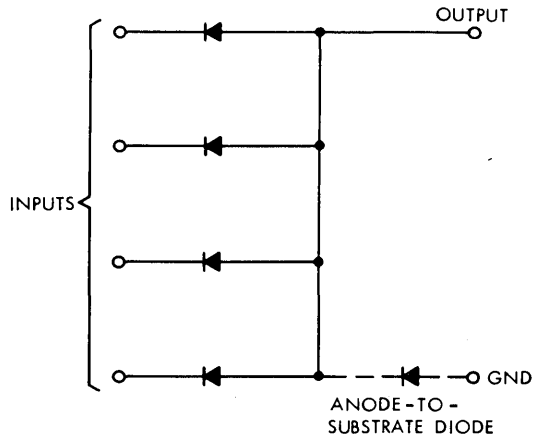
switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$t_{pd(0)}$ Propagation delay time to logical 0 level	51	$R_1 = 150\ \Omega$ , $C_L = 500\text{ pF}$	15	40	ns
$t_{pd(1)}$ Propagation delay time to logical 1 level		$R_1 = 510\ \Omega$ , $C_L = 500\text{ pF}$	25	80	ns

† Expander nodes are open unless otherwise noted.

# TYPE SN15 833 DUAL 4-INPUT EXPANDER

schematic (each expander)



## electrical characteristics

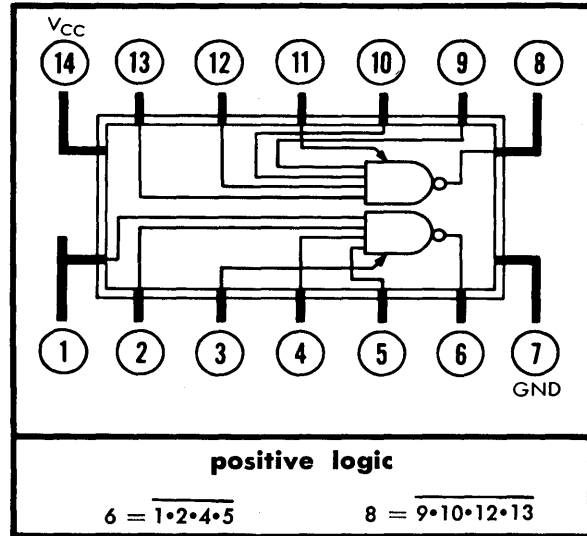
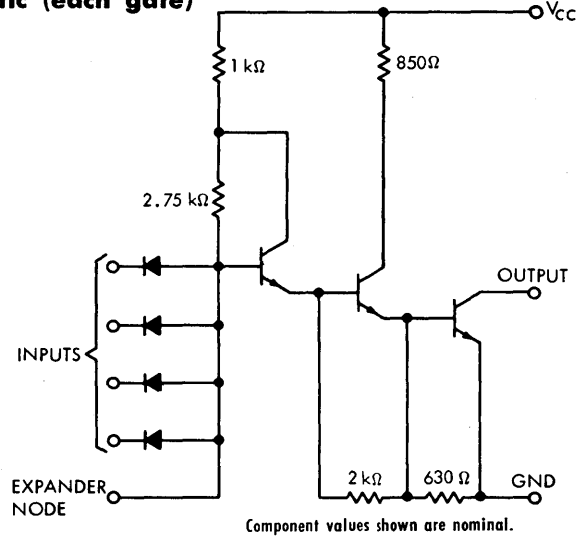
PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_F$ Input diode forward voltage	21	$I_{out} = 2 \text{ mA}, T_A = 25^\circ\text{C}$	0.68	0.82	V
		$I_{out} = 2 \text{ mA}, T_A = 0^\circ\text{C}$	0.75	0.9	V
		$I_{out} = 2 \text{ mA}, T_A = 75^\circ\text{C}$	0.6	0.75	V
$I_{in R}$ Input diode reverse current	22	$V_{in} = 4 \text{ V}, T_A = 25^\circ\text{C}$		5	$\mu\text{A}$
		$V_{in} = 4 \text{ V}, T_A = 0^\circ\text{C}$		5	$\mu\text{A}$
		$V_{in} = 4 \text{ V}, T_A = 75^\circ\text{C}$		10	$\mu\text{A}$
$I_{out R}$ Anode-to-substrate reverse current	23	$V_{out} = 4 \text{ V}, T_A = 25^\circ\text{C}$		10	$\mu\text{A}$

NOTE: A total of four expanders may be connected to an expandable gate to provide a fan-in of 20.

# TYPE SN15 844

## DUAL 4-INPUT NAND/NOR POWER GATE

schematic (each gate)



### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	5 V
Maximum Fan-Out From Each Output . . . . .	27

### electrical characteristics at $V_{CC} = 5 V$

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{out(0)}$ Logical 0 output voltage (on level)	1	$V_{in} = 1.9 V, I_{sink} = 40 mA, T_A = 25^\circ C$		0.45	V
		$V_{in} = 2 V, I_{sink} = 40 mA, T_A = 0^\circ C$		0.45	V
		$V_{in} = 1.8 V, I_{sink} = 36 mA, T_A = 75^\circ C$		0.5	V
$V_{out(1)}$ Logical 1 output voltage (off level)	24	$I_{sink} = 5 mA, T_A = 25^\circ C$	6		V
$I_{in(1)}$ Logical 1 level input current	4	$V_{in} = 4 V, T_A = 25^\circ C \text{ and } 0^\circ C$		5	$\mu A$
		$V_{in} = 4 V, T_A = 75^\circ C$		10	$\mu A$

† Expander nodes are open unless otherwise noted.

# TYPE SN15 844

## DUAL 4-INPUT NAND/NOR POWER GATE

electrical characteristics (continued) at  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$I_{in(0)}$ Logical 0 level input current	5	$V_{in} = 0.45\text{ V}$ , $V_R = 4\text{ V}$ , $T_A = 25^\circ\text{C}$ and $0^\circ\text{C}$		-1.4	mA
		$V_{in} = 0.5\text{ V}$ , $V_R = 4\text{ V}$ , $T_A = 75^\circ\text{C}$		-1.33	mA
$I_{out(1)}$ Output reverse current (off level, worst-case voltage at any input)	25	$V_{in} = 1.1\text{ V}$ , $V_{out} = 4.5\text{ V}$ , $T_A = 25^\circ\text{C}$		100	$\mu\text{A}$
		$V_{in} = 1.2\text{ V}$ , $V_{out} = 4.5\text{ V}$ , $T_A = 0^\circ\text{C}$		100	$\mu\text{A}$
		$V_{in} = 0.95\text{ V}$ , $V_{out} = 4.5\text{ V}$ , $T_A = 75^\circ\text{C}$		200	$\mu\text{A}$
$I_{out(1)}$ Output reverse current (off level, worst-case voltage at expander input)	26	$V_{inX} = 1.8\text{ V}$ , $V_{out} = 4.5\text{ V}$ , $T_A = 25^\circ\text{C}$		100	$\mu\text{A}$
$I_{CC(0)}$ Logical 0 level supply current (both gates)	8	$T_A = 25^\circ\text{C}$		24	mA
$I_{CC(1)}$ Logical 1 level supply current at maximum $V_{CC}$ (both gates)	9	$V_{CC} = 8\text{ V}$ $T_A = 25^\circ\text{C}$		8	mA

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$t_{pd(0)}$ Propagation delay time to logical 0 level	51	$R_1 = 150\ \Omega$ , $C_L = 100\text{ pF}$	10	35	ns
$t_{pd(1)}$ Propagation delay time to logical 1 level		$R_1 = 510\ \Omega$ , $C_L = 20\text{ pF}$	15	50	ns

† Expander nodes are open unless otherwise noted.

# TYPE SN15845 FLIP-FLOP WITH SET AND CLEAR

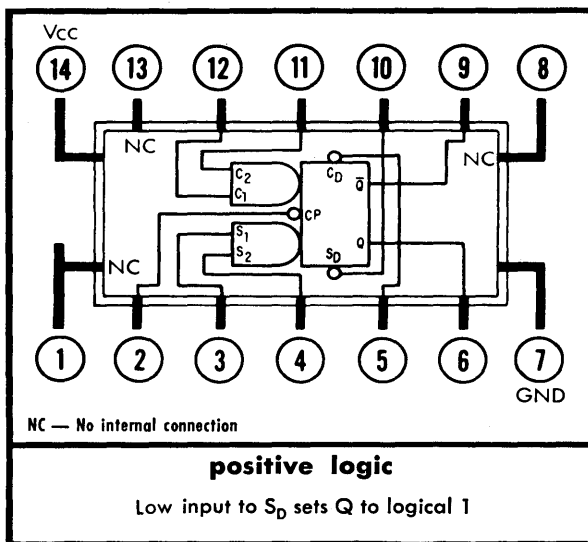
logic

TRUTH TABLES

R-S MODE				
$t_n$				$t_{n+1}$
$S_1$	$S_2$	$C_1$	$C_2$	Q
0	X	0	X	$Q_n$
0	X	X	0	$Q_n$
X	0	0	X	$Q_n$
X	0	X	0	$Q_n$
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	Indeterminate

J-K MODE		
$t_n$		$t_{n+1}$
$S_1$	$C_1$	Q
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\bar{Q}_n$

- NOTES: 1.  $t_n$  = bit time before clock pulse.  
 2.  $t_{n+1}$  = bit time after clock pulse.  
 3. X indicates that either a logical 1 or a logical 0 may be present.  
 4. Logical 1 is more positive than logical 0.  
 5. For operation in the J-K mode connect  $S_2$  to  $\bar{Q}$  and  $C_2$  to Q.



## recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	5 V
Maximum Fan-Out From Each Output . . . . .	12

## electrical characteristics at $V_{CC} = 5 V$ (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$ Logical 0 output voltage (on level) at Q or $\bar{Q}$	27 and 28	$V_1 = 1.1 V, V_2 = 1.9 V, V_3 = 5 V, I_{sink} = 16.8 mA, T_A = 25^\circ C$	0.45		V
		$V_1 = 1.2 V, V_2 = 2 V, V_3 = 5 V, I_{sink} = 16.8 mA, T_A = 0^\circ C$	0.45		V
		$V_1 = 0.95 V, V_2 = 1.8 V, V_3 = 5 V, I_{sink} = 16 mA, T_A = 75^\circ C$	0.5		V
$V_{out(1)}$ Logical 1 output voltage (off level) at Q or $\bar{Q}$	12	$V_1 = 5 V, V_2 = 1.1 V, I_{load} = -0.12 mA, T_A = 25^\circ C$	2.6		V
		$V_1 = 5 V, V_2 = 1.2 V, I_{load} = -0.12 mA, T_A = 0^\circ C$	2.6		V
		$V_1 = 5 V, V_2 = 0.95 V, I_{load} = -0.12 mA, T_A = 75^\circ C$	2.5		V
$I_{CP(0)}$ Logical 0 level clock-input forward current	29	$V_{in} = 1.1 V, V_{CP} = 0.45 V, T_A = 25^\circ C$		-2.8	mA
		$V_{in} = 1.2 V, V_{CP} = 0.45 V, T_A = 0^\circ C$		-2.8	mA
		$V_{in} = 0.95 V, V_{CP} = 0.5 V, T_A = 75^\circ C$		-2.67	mA
$I_{CP(1)}$ Logical 1 level clock-input reverse current	30	$V_{CC} = 4 V, V_{CP} = 4 V, T_A = 25^\circ C \text{ and } 0^\circ C$		20	$\mu A$
		$V_{CC} = 4 V, V_{CP} = 4 V, T_A = 75^\circ C$		30	$\mu A$

# TYPE SN15 845 FLIP-FLOP WITH SET AND CLEAR

electrical characteristics (continued) at  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

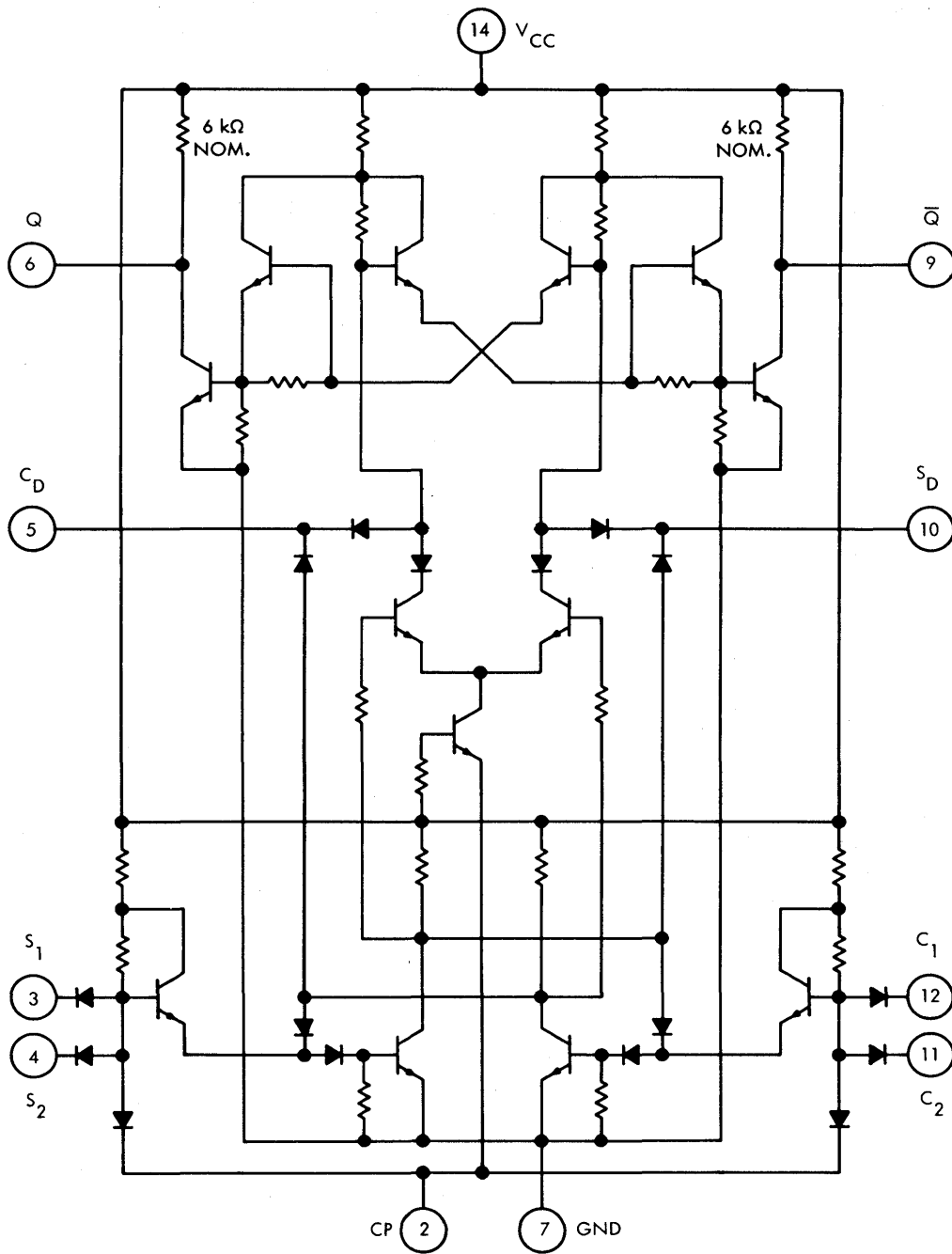
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$	Logical 1 level synchronous-input current	15	$V_{in} = 4\text{ V}, T_A = 25^\circ\text{C and } 0^\circ\text{C}$		5	$\mu\text{A}$
			$V_{in} = 4\text{ V}, T_A = 75^\circ\text{C}$		10	$\mu\text{A}$
$I_{in(0)}$	Logical 0 level synchronous-input current	31	$V_{in} = 0.45\text{ V}, V_1 = 4\text{ V}, V_{CP} = 4\text{ V}, T_A = 25^\circ\text{C and } 0^\circ\text{C}$		-0.95	mA
			$V_{in} = 0.5\text{ V}, V_1 = 4\text{ V}, V_{CP} = 4\text{ V}, T_A = 75^\circ\text{C}$		-0.9	mA
$I_{in(1)}$	Logical 1 level asynchronous-input current	32	$V_{in} = 4\text{ V}, V_1 = 5\text{ V}, T_A = 25^\circ\text{C and } 0^\circ\text{C}$		5	$\mu\text{A}$
			$V_{in} = 4\text{ V}, V_1 = 5\text{ V}, T_A = 75^\circ\text{C}$		10	$\mu\text{A}$
$I_{in(0)}$	Logical 0 level asynchronous-input current	33	$V_{in} = 0.45\text{ V}, T_A = 25^\circ\text{C and } 0^\circ\text{C}$		-2.1	mA
			$V_{in} = 0.5\text{ V}, T_A = 75^\circ\text{C}$		-2	mA
$I_{OS}$	Short-circuit output current	18	$V_{in} = 5\text{ V}, V_{out} = 0, T_A = 25^\circ\text{C and } 0^\circ\text{C}$	-0.59	-1.41	mA
			$V_{in} = 5\text{ V}, V_{out} = 0, T_A = 75^\circ\text{C}$	-0.55	-1.38	mA
$I_{CC(0)}$	Logical 0 level supply current	19	$T_A = 25^\circ\text{C}$		15	mA
$I_{CC(1)}$	Logical 1 level supply current at maximum $V_{CC}$	20	$V_{CC} = 8\text{ V}, T_A = 25^\circ\text{C}$		17	mA

switching characteristics,  $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$	Propagation delay time to logical 0 level	52	$R_1 = 330\ \Omega, C_L = 50\text{ pF}$	5	75	ns
			$R_1 = 2\text{ k}\Omega, C_L = 30\text{ pF}$	5	75	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level					

# TYPE SN15 845 FLIP-FLOP WITH SET AND CLEAR

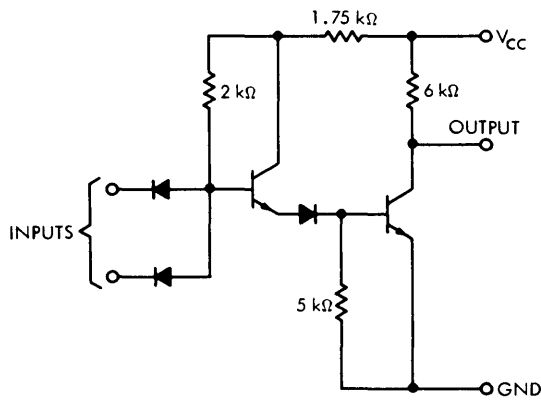
schematic



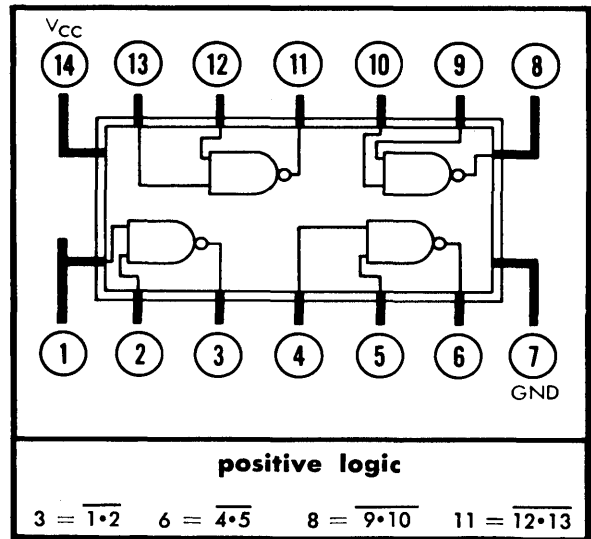
NOTE: Pins ①, ⑧, and ⑬ — no internal connection.

# TYPE SN15 846 QUADRUPLE 2-INPUT NAND/NOR GATE

schematic (each gate)



Component values shown are nominal.



**recommended operating conditions**

Supply Voltage  $V_{CC}$  . . . . . 5 V  
 Maximum Fan-Out From Each Output . . . . . 8

**electrical characteristics at  $V_{CC} = 5$  V**

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$ Logical 0 output voltage (on level)	1	$V_{in} = 1.9$ V, $I_{sink} = 12$ mA, $T_A = 25^\circ$ C	0.45		V
		$V_{in} = 2$ V, $I_{sink} = 12$ mA, $T_A = 0^\circ$ C	0.45		V
		$V_{in} = 1.8$ V, $I_{sink} = 11.4$ mA, $T_A = 75^\circ$ C	0.5		V
$V_{out(1)}$ Logical 1 output voltage (off level)	2	$V_{in} = 1.1$ V, $I_{load} = -0.12$ mA, $T_A = 25^\circ$ C	2.6		V
		$V_{in} = 1.2$ V, $I_{load} = -0.12$ mA, $T_A = 0^\circ$ C	2.6		V
		$V_{in} = 0.95$ V, $I_{load} = -0.12$ mA, $T_A = 75^\circ$ C	2.5		V



# TYPE SN15 846

## QUADRUPLE 2-INPUT NAND/NOR GATE

electrical characteristics (continued) at  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$ Logical 1 level input current	4	$V_{in} = 4\text{ V}, T_A = 25^\circ\text{C}$ and $0^\circ\text{C}$		5	$\mu\text{A}$
		$V_{in} = 4\text{ V}, T_A = 75^\circ\text{C}$		10	$\mu\text{A}$
$I_{in(0)}$ Logical 0 level input current	5	$V_{in} = 0.45\text{ V}, V_R = 4\text{ V}, T_A = 25^\circ\text{C}$ and $0^\circ\text{C}$		-1.4	$\text{mA}$
		$V_{in} = 0.5\text{ V}, V_R = 4\text{ V}, T_A = 75^\circ\text{C}$		-1.33	$\text{mA}$
$I_{out(1)}$ Output reverse current (off level)	6	$V_{out} = 5\text{ V}, T_A = 25^\circ\text{C}$		100	$\mu\text{A}$
$I_{OS}$ Short-circuit output current	7	$V_{out} = 0, T_A = 25^\circ\text{C}$		-1.3	$\text{mA}$
		$V_{out} = 0, T_A = 0^\circ\text{C}$		-1.3	$\text{mA}$
		$V_{out} = 0, T_A = 75^\circ\text{C}$		-1.25	$\text{mA}$
$I_{CC(0)}$ Logical 0 level supply current (all gates)	8	$T_A = 25^\circ\text{C}$		16	$\text{mA}$
$I_{CC(1)}$ Logical 1 level supply current at maximum $V_{CC}$ (all gates)	9	$V_{CC} = 8\text{ V}, T_A = 25^\circ\text{C}$		16	$\text{mA}$

switching characteristics,  $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$ Propagation delay time to logical 0 level	51	$R_1 = 400\ \Omega, C_L = 50\text{ pF}$	10	30	ns
$t_{pd(1)}$ Propagation delay time to logical 1 level		$R_1 = 3.9\text{ k}\Omega, C_L = 30\text{ pF}$	25	80	ns

# TYPE SN15 848 FLIP-FLOP WITH SET AND CLEAR

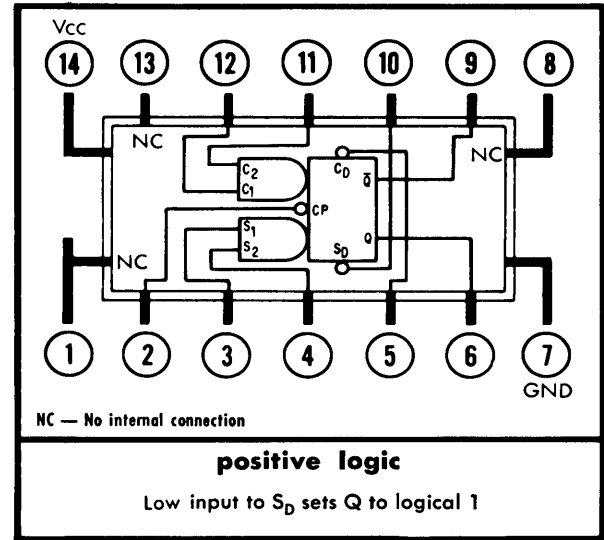
## Logic

### TRUTH TABLES

R-S MODE				
$t_n$				$t_{n+1}$
$S_1$	$S_2$	$C_1$	$C_2$	Q
0	X	0	X	$Q_n$
0	X	X	0	$Q_n$
X	0	0	X	$Q_n$
X	0	X	0	$Q_n$
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	Indeterminate

J-K MODE		
$t_n$		$t_{n+1}$
$S_1$	$C_1$	Q
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\bar{Q}_n$

- NOTES: 1.  $t_n$  = bit time before clock pulse.  
 2.  $t_{n+1}$  = bit time after clock pulse.  
 3. X indicates that either a logical 1 or a logical 0 may be present.  
 4. Logical 1 is more positive than logical 0.  
 5. For operation in the J-K mode connect  $S_2$  to  $\bar{Q}$  and  $C_2$  to Q.



### recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	5 V
Maximum Fan-Out From Each Output . . . . .	11

### electrical characteristics at $V_{CC} = 5 V$ (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$ Logical 0 output voltage (on level) at Q or $\bar{Q}$	27 and 28	$V_1 = 1.1 V, V_2 = 1.9 V, V_3 = 5 V, I_{sink} = 15.4 mA, T_A = 25^\circ C$	0.45		V
		$V_1 = 1.2 V, V_2 = 2 V, V_3 = 5 V, I_{sink} = 15.4 mA, T_A = 0^\circ C$	0.45		V
		$V_1 = 0.95 V, V_2 = 1.8 V, V_3 = 5 V, I_{sink} = 14.6 mA, T_A = 75^\circ C$	0.5		V
$V_{out(1)}$ Logical 1 output voltage (off level) at Q or $\bar{Q}$	12	$V_1 = 5 V, I_{load} = -0.12 mA, V_2 = 1.1 V, T_A = 25^\circ C$	2.6		V
		$V_1 = 5 V, I_{load} = -0.12 mA, V_2 = 1.2 V, T_A = 0^\circ C$	2.6		V
		$V_1 = 5 V, I_{load} = -0.12 mA, V_2 = 0.95 V, T_A = 75^\circ C$	2.5		V
$I_{CP(0)}$ Logical 0 level clock-input forward current	29	$V_{in} = 1.1 V, V_{CP} = 0.45 V, T_A = 25^\circ C$		-2.8	mA
		$V_{in} = 1.2 V, V_{CP} = 0.45 V, T_A = 0^\circ C$		-2.8	mA
		$V_{in} = 0.95 V, V_{CP} = 0.5 V, T_A = 75^\circ C$		-2.67	mA
$I_{CP(1)}$ Logical 1 level clock-input reverse current	30	$V_{CC} = 4 V, V_{CP} = 4 V, T_A = 25^\circ C \text{ and } 0^\circ C$		20	$\mu A$
		$V_{CC} = 4 V, V_{CP} = 4 V, T_A = 75^\circ C$		30	$\mu A$

# TYPE SN15 848

## FLIP-FLOP WITH SET AND CLEAR

electrical characteristics (continued) at  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

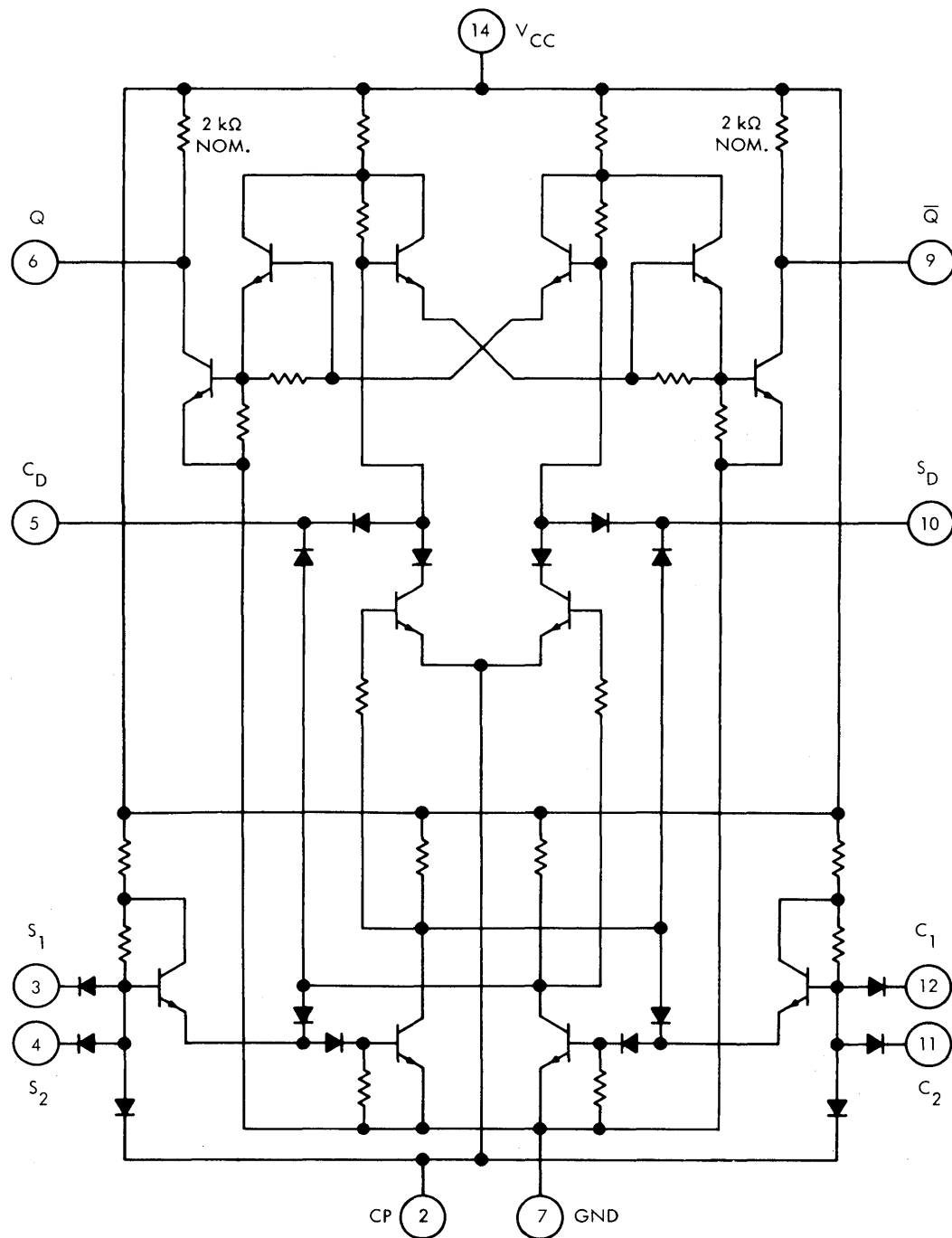
PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$ Logical 1 level synchronous-input current	15	$V_{in} = 4\text{ V}, T_A = 25^\circ\text{C and } 0^\circ\text{C}$		5	$\mu\text{A}$
		$V_{in} = 4\text{ V}, T_A = 75^\circ\text{C}$		10	$\mu\text{A}$
$I_{in(0)}$ Logical 0 level synchronous-input current	31	$V_{in} = 0.45\text{ V}, V_1 = 4\text{ V}, V_{CP} = 4\text{ V}, T_A = 25^\circ\text{C and } 0^\circ\text{C}$		-0.95	mA
		$V_{in} = 0.5\text{ V}, V_1 = 4\text{ V}, V_{CP} = 4\text{ V}, T_A = 75^\circ\text{C}$		-0.9	mA
$I_{in(1)}$ Logical 1 level asynchronous-input current	32	$V_{in} = 4\text{ V}, V_1 = 5\text{ V}, T_A = 25^\circ\text{C and } 0^\circ\text{C}$		5	$\mu\text{A}$
		$V_{in} = 4\text{ V}, V_1 = 5\text{ V}, T_A = 75^\circ\text{C}$		10	$\mu\text{A}$
$I_{in(0)}$ Logical 0 level asynchronous-input current	33	$V_{in} = 0.45\text{ V}, T_A = 25^\circ\text{C and } 0^\circ\text{C}$		-2.1	mA
		$V_{in} = 0.5\text{ V}, T_A = 75^\circ\text{C}$		-2	mA
$I_{OS}$ Short-circuit output current	18	$V_{in} = 5\text{ V}, V_{out} = 0, T_A = 25^\circ\text{C and } 0^\circ\text{C}$	-0.59	-1.41	mA
		$V_{in} = 5\text{ V}, V_{out} = 0, T_A = 75^\circ\text{C}$	-0.55	-1.38	mA
$I_{CC(0)}$ Logical 0 level supply current	19	$T_A = 25^\circ\text{C}$		15	mA
$I_{CC(1)}$ Logical 1 level supply current at maximum $V_{CC}$	20	$V_{CC} = 8\text{ V}, T_A = 25^\circ\text{C}$		17	mA

switching characteristics,  $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$ Propagation delay time to logical 0 level	52	$R_1 = 330\ \Omega, C_L = 50\text{ pF}$	5	65	ns
$t_{pd(1)}$ Propagation delay time to logical 1 level		$R_1 = 2\text{ k}\Omega, C_L = 30\text{ pF}$	5	75	ns

# TYPE SN15 848 FLIP-FLOP WITH SET AND CLEAR

schematic



NOTE: Pins 1, 8 and 13 —no internal connection.

# TYPE SN15850

## PULSE-TRIGGERED BINARY

logic

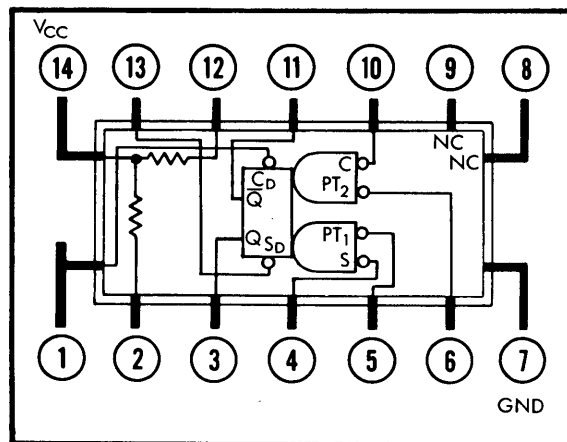
TRUTH TABLES

SYNCHRONOUS					
PULSE INPUT				OUTPUT	
S	C	PT <sub>1</sub>	PT <sub>2</sub>	Q	$\bar{Q}$
1	X	X	1	Q <sub>n</sub>	$\bar{Q}$ <sub>n</sub>
X	1	1	X	Q <sub>n</sub>	$\bar{Q}$ <sub>n</sub>
0	1	0	X	1	0
0	X	0	1	1	0
1	0	X	0	0	1
X	0	1	0	0	1
0	0	0	0	Indeterminate	

ASYNCHRONOUS			
DIRECT INPUT		OUTPUT	
S <sub>D</sub>	C <sub>D</sub>	Q	$\bar{Q}$
1	1	Q <sub>n</sub>	$\bar{Q}$ <sub>n</sub>
0	1	0	1
1	0	1	0
0	0	1	1

NOTES:

1. X indicates that either a logical 1 or a logical 0 may be present.
2. Logical 1 is more positive than logical 0.
3. Logical states shown for pulse inputs PT<sub>1</sub> and PT<sub>2</sub> indicate that a transition to that state has just occurred.
4. Truth tables reflect individual conditions at the inputs. Either direct input may be used to inhibit its corresponding pulse input.



### recommended operating conditions

Supply Voltage  $V_{CC}$  . . . . . 5 V  
 Maximum Fan-Out From Each Output . . . . . 8

### electrical characteristics at $V_{CC} = 5 V$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$ Logical 0 output voltage (on level) at Q or $\bar{Q}$	34	$V_{in} = 1.9 V, I_{sink} = 12 mA, T_A = 25^\circ C$		0.45	V
		$V_{in} = 2 V, I_{sink} = 12 mA, T_A = 0^\circ C$		0.45	V
		$V_{in} = 1.8 V, I_{sink} = 11.4 mA, T_A = 75^\circ C$		0.5	V
$V_{out(1)}$ Logical 1 output voltage (off level) at Q or $\bar{Q}$	35	$V_1 = 1.1 V, V_2 = 1.9 V, V_3 = 5 V, I_{load} = -1.5 mA, T_A = 25^\circ C$	2.6		V
		$V_1 = 1.2 V, V_2 = 2 V, V_3 = 5 V, I_{load} = -1.5 mA, T_A = 0^\circ C$	2.6		V
		$V_1 = 0.95 V, V_2 = 1.8 V, V_3 = 5 V, I_{load} = -1.5 mA, T_A = 75^\circ C$	2.5		V
$I_{inPT}$ Pulse-triggered-input current	36	$V_{in} = 8 V, T_A = 25^\circ C \text{ and } 0^\circ C$		5	$\mu A$
		$V_{in} = 8 V, T_A = 75^\circ C$		10	$\mu A$
$I_{in(0)}$ Logical 0 level-input current at C or S	37	$V_{in} = 0.45 V, T_A = 25^\circ C \text{ and } 0^\circ C$		-2.1	mA
		$V_{in} = 0.5 V, T_A = 75^\circ C$		-2	mA
$I_{in(0)}$ Logical 0 level at $C_D$ or $S_D$ input current	37	$V_{in} = 0.45 V, T_A = 25^\circ C \text{ and } 0^\circ C$		-1.6	mA
		$V_{in} = 0.5 V, T_A = 75^\circ C$		-1.52	mA

# TYPE SN15 850 PULSE-TRIGGERED BINARY

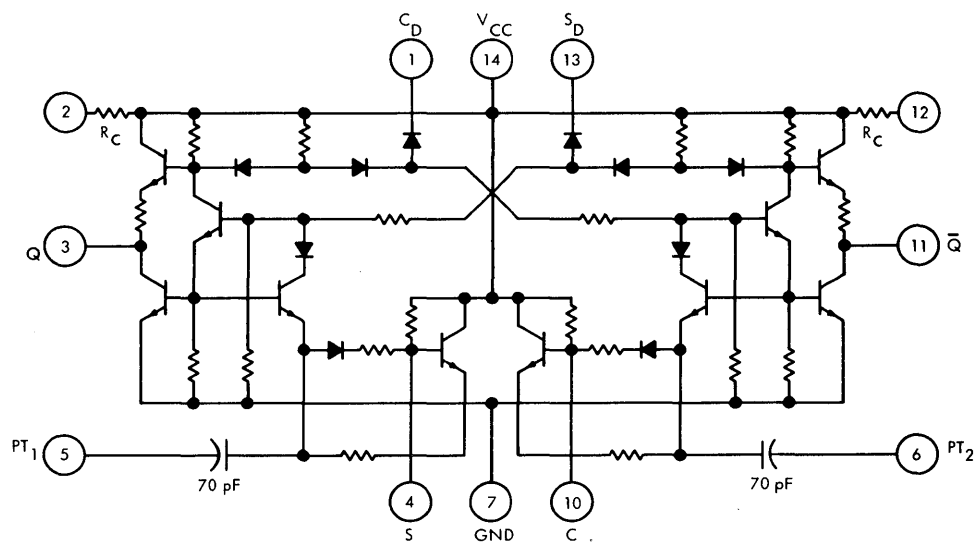
electrical characteristics (continued) at  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$ Logical 1 level input current at $C_D$ or $S_D$	38	$V_{in} = 4\text{ V}, T_A = 25^\circ\text{C and } 0^\circ\text{C}$		5	$\mu\text{A}$
		$V_{in} = 4\text{ V}, T_A = 75^\circ\text{C}$		10	$\mu\text{A}$
$I_{RC}$ Current through resistor $R_C$	39	$V_{in} = 0, T_A = 25^\circ\text{C}$	-3.3	-7.9	mA
$I_{OS}$ Short-circuit output current	40	$V_{out} = 0, T_A = 25^\circ\text{C and } 0^\circ\text{C}$	-13.7	-29	mA
		$V_{out} = 0, T_A = 75^\circ\text{C}$	-12.6	-28	mA
$I_{out(1)}$ Output reverse current (off level)	40	$V_{out} = 4.5\text{ V}, T_A = 25^\circ\text{C and } 0^\circ\text{C}$		150	$\mu\text{A}$
$I_{CC(0)}$ Logical 0 level supply current	41	$T_A = 25^\circ\text{C}$		9.3	mA
$I_{CC(1)}$ Logical 1 level supply current at maximum $V_{CC}$	42	$V_{CC} = 8\text{ V}, T_A = 25^\circ\text{C}$		19.6	mA

switching characteristics,  $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$ Propagation delay time to logical 0 level	53	$R_1 = 400\ \Omega, C_L = 100\text{ pF}$	5	32	ns
$t_{pd(1)}$ Propagation delay time to logical 1 level		$R_1 = 3.9\text{ k}\Omega, C_L = 100\text{ pF}$	5	25	ns

schematic



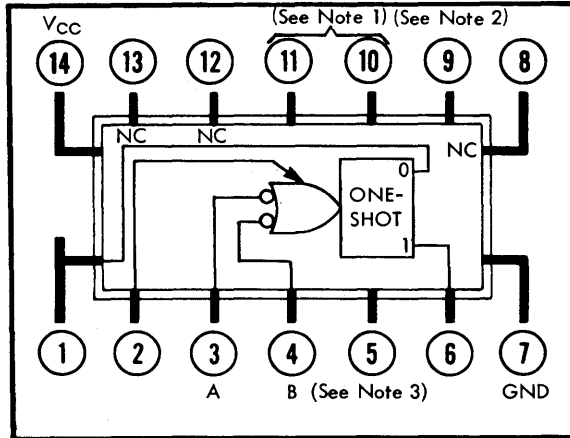
# TYPE SN15 851 MONOSTABLE MULTIVIBRATOR

logic

TRUTH TABLE

$t_n$ INPUT		$t_{n+1}$ INPUT		OUTPUT
A	B	A	B	
1	1	1	1	INHIBIT
1	1	1	0	ONE-SHOT
1	1	0	1	ONE-SHOT
1	1	0	0	ONE-SHOT
0	1	X	X	INHIBIT
1	0	X	X	INHIBIT
0	0	X	X	INHIBIT

NOTES: a.  $t_n$  = time before input transition.  
 b.  $t_{n+1}$  = time after input transition.  
 c. X indicates that either a logical 1 or a logical 0 may be present.



NOTES: 1. External resistor and capacitor may be used between pins (10), (11), and (14) to control one-shot pulse width.  
 2. To use the internal timing resistor, connect pin (9) to pin (14).  
 3. Input sensitivity can be decreased by adding a capacitor from pin (5) to ground.

## recommended operating conditions

Supply Voltage $V_{CC}$ . . . . .	5 V
Maximum Fan-Out From Each Output . . . . .	10
Input Pulse Characteristics:	
Minimum Negative-Going Transition . . . . .	1 V
Maximum Input Fall Time Per Volt . . . . .	25 ns/V
Maximum Duty Cycle . . . . .	40%

## electrical characteristics at $V_{CC} = 5 V$

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$V_{out(0)}$ Logical 0 output voltage (on level)	43	$I_{sink} = 15 \text{ mA}$ , $T_A = 25^\circ\text{C}$ and $0^\circ\text{C}$		0.45	V
		$I_{sink} = 14.5 \text{ mA}$ , $T_A = 75^\circ\text{C}$		0.5	V
$V_{out(1)}$ Logical 1 output voltage (off level)	44	$I_{load} = -0.18 \text{ mA}$ , $T_A = 25^\circ\text{C}$ and $0^\circ\text{C}$	2.6		V
		$I_{load} = -0.18 \text{ mA}$ , $T_A = 75^\circ\text{C}$	2.5		V
$I_{in(1)}$ Logical 1 level input current	45	$V_{in} = 4 \text{ V}$ , $T_A = 25^\circ\text{C}$ and $0^\circ\text{C}$		5	$\mu\text{A}$
		$V_{in} = 4 \text{ V}$ , $T_A = 75^\circ\text{C}$		10	$\mu\text{A}$
$I_{in(0)}$ Logical 0 level input current	46	$V_1 = 4 \text{ V}$ , $V_2 = 0.45 \text{ V}$ , $T_A = 25^\circ\text{C}$ and $0^\circ\text{C}$	-1.35	-2.8	mA
		$V_1 = 4 \text{ V}$ , $V_2 = 0.5 \text{ V}$ , $T_A = 75^\circ\text{C}$	-1.25	-2.63	mA

†Expander node is open unless otherwise noted.

# TYPE SN15 851 MONOSTABLE MULTIVIBRATOR

electrical characteristics (continued) at  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

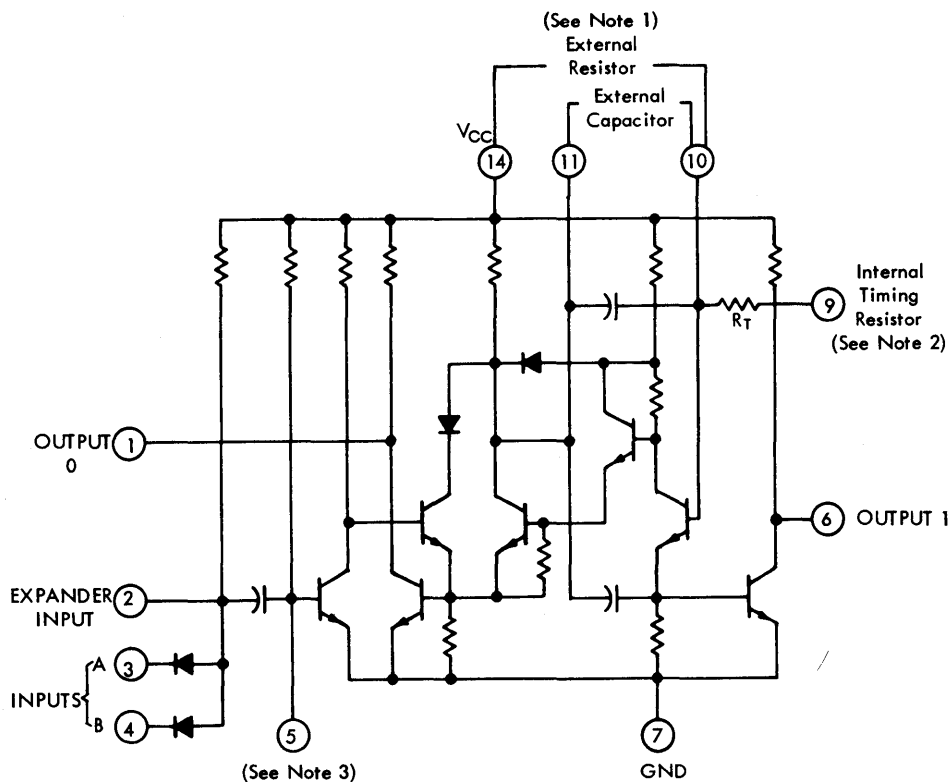
PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$I_{RT}$ Current through internal timing resistor $R_T$	47	$V_{in} = 5\text{ V}, T_A = 25^\circ\text{C}$	0.4	0.75	mA
$I_{SC}$ Short circuit current at expander node or pin (11)	48	$V_{in} = 0, T_A = 25^\circ\text{C}$ and $0^\circ\text{C}$	-0.8		mA
		$V_{in} = 0, T_A = 75^\circ\text{C}$	-0.75		mA
$I_{CC}$ Supply current	49	$T_A = 25^\circ\text{C}$		12	mA
$I_{CC(max)}$ Supply current at maximum $V_{CC}$	50	$V_{CC} = 8\text{ V}, T_A = 25^\circ\text{C}$		26.7	mA

switching characteristics,  $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
$t_{pd(0)}$ Propagation delay time to logical 0 level	54	$R_1 = 300\ \Omega, C_L = 50\ \text{pF}$		50	ns
$t_{pd(1)}$ Propagation delay time to logical 1 level				50	ns
$t_p$ Pulse width			50	175	ns

† Expander nodes are open unless otherwise noted.

## schematic



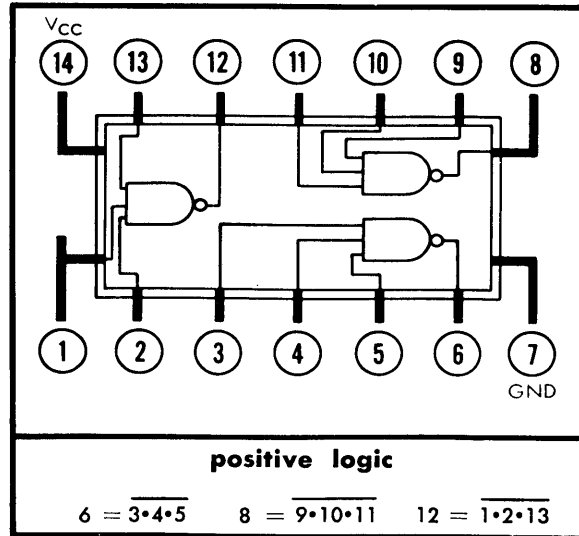
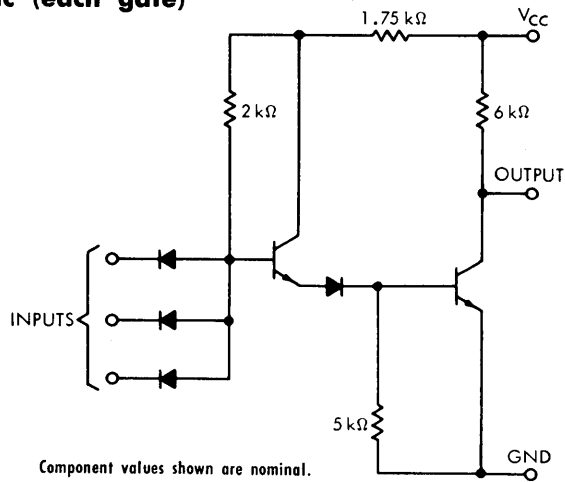
- NOTES: 1. External resistor and capacitor may be used (as indicated above) between pins (10), (11), and (14) to control one-shot pulse width.  
 2. To use the internal timing resistor, connect pin (9) to pin (14).  
 3. Input sensitivity can be decreased by adding a capacitor from pin (5) to ground.



# TYPE SN15 862

## TRIPLE 3-INPUT NAND/NOR GATE

schematic (each gate)



### recommended operating conditions

Supply Voltage  $V_{CC}$  . . . . . 5 V  
 Maximum Fan-Out From Each Output . . . . . 8

### electrical characteristics at $V_{CC} = 5$ V

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$V_{out(0)}$ Logical 0 output voltage (on level)	1	$V_{in} = 1.9$ V, $I_{sink} = 12$ mA, $T_A = 25^\circ$ C		0.45	V
		$V_{in} = 2$ V, $I_{sink} = 12$ mA, $T_A = 0^\circ$ C		0.45	V
		$V_{in} = 1.8$ V, $I_{sink} = 11.4$ mA, $T_A = 75^\circ$ C		0.5	V
$V_{out(1)}$ Logical 1 output voltage (off level)	2	$V_{in} = 1.1$ V, $I_{load} = -0.12$ mA, $T_A = 25^\circ$ C	2.6		V
		$V_{in} = 1.2$ V, $I_{load} = -0.12$ mA, $T_A = 0^\circ$ C	2.6		V
		$V_{in} = 0.95$ V, $I_{load} = -0.12$ mA, $T_A = 75^\circ$ C	2.5		V

# TYPE SN15 862 TRIPLE 3-INPUT NAND/NOR GATE

electrical characteristics (continued) at  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

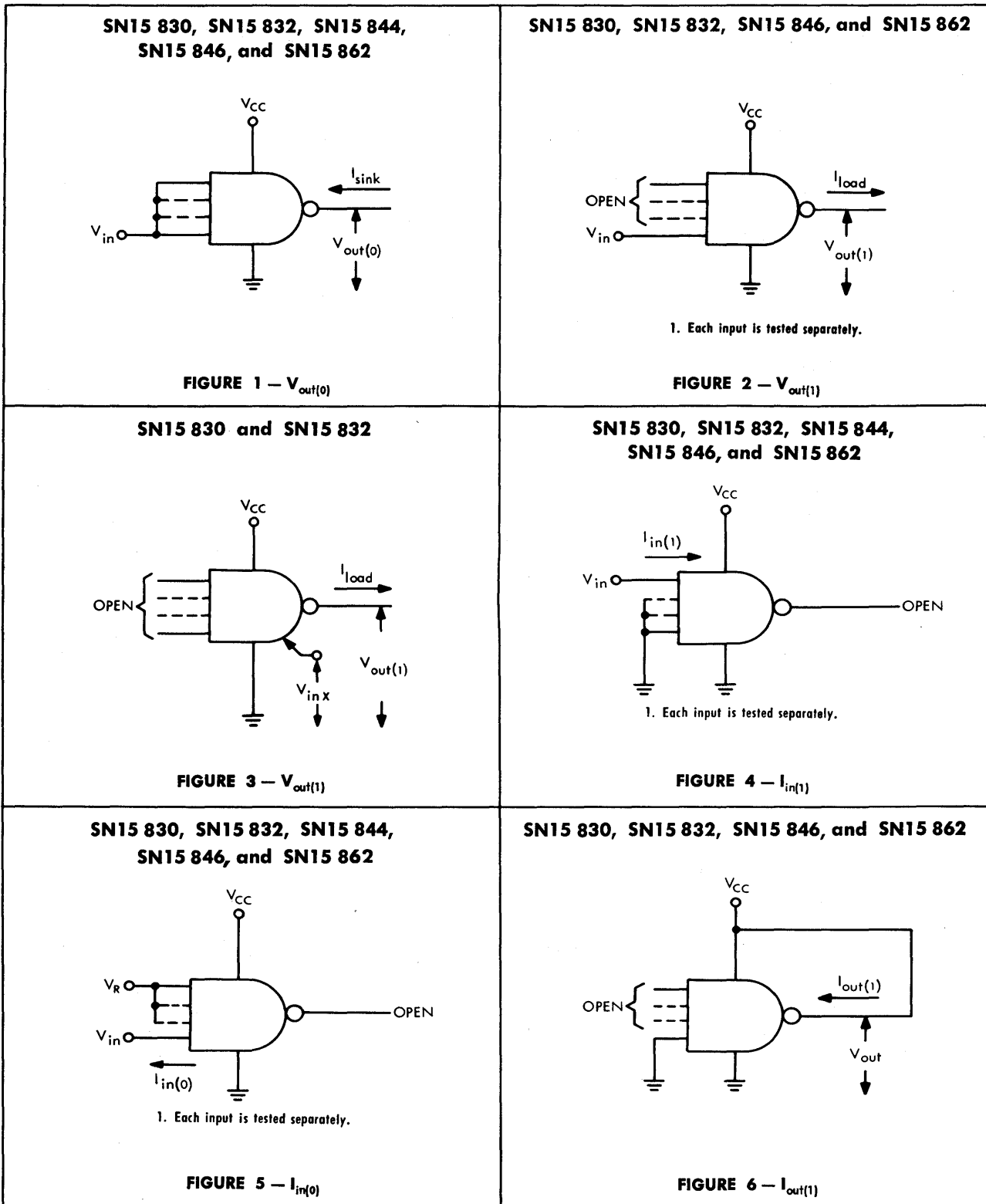
PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{in(1)}$ Logical 1 level input current	4	$V_{in} = 4\text{ V}, T_A = 25^\circ\text{C and } 0^\circ\text{C}$		5	$\mu\text{A}$
		$V_{in} = 4\text{ V}, T_A = 75^\circ\text{C}$		10	$\mu\text{A}$
$I_{in(0)}$ Logical 0 level input current	5	$V_{in} = 0.45\text{ V}, V_R = 4\text{ V}, T_A = 25^\circ\text{C and } 0^\circ\text{C}$		-1.4	mA
		$V_{in} = 0.5\text{ V}, V_R = 4\text{ V}, T_A = 75^\circ\text{C}$		-1.33	mA
$I_{out(1)}$ Output reverse current (off level)	6	$V_{out} = 5\text{ V}, T_A = 25^\circ\text{C}$		100	$\mu\text{A}$
$I_{OS}$ Short-circuit output current	7	$V_{out} = 0, T_A = 25^\circ\text{C}$		-1.3	mA
		$V_{out} = 0, T_A = 0^\circ\text{C}$		-1.3	mA
		$V_{out} = 0, T_A = 75^\circ\text{C}$		-1.25	mA
$I_{CC(0)}$ Logical 0 level supply current (all gates)	8	$T_A = 25^\circ\text{C}$		12	mA
$I_{CC(1)}$ Logical 1 level supply current at maximum $V_{CC}$ (all gates)	9	$V_{CC} = 8\text{ V}, T_A = 25^\circ\text{C}$		12	mA

switching characteristics,  $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$t_{pd(0)}$ Propagation delay time to logical 0 level	51	$R_1 = 400\ \Omega, C_L = 50\text{ pF}$	10	30	ns
$t_{pd(1)}$ Propagation delay time to logical 1 level		$R_1 = 3.9\text{ k}\Omega, C_L = 30\text{ pF}$	25	80	ns

**PARAMETER MEASUREMENT INFORMATION**

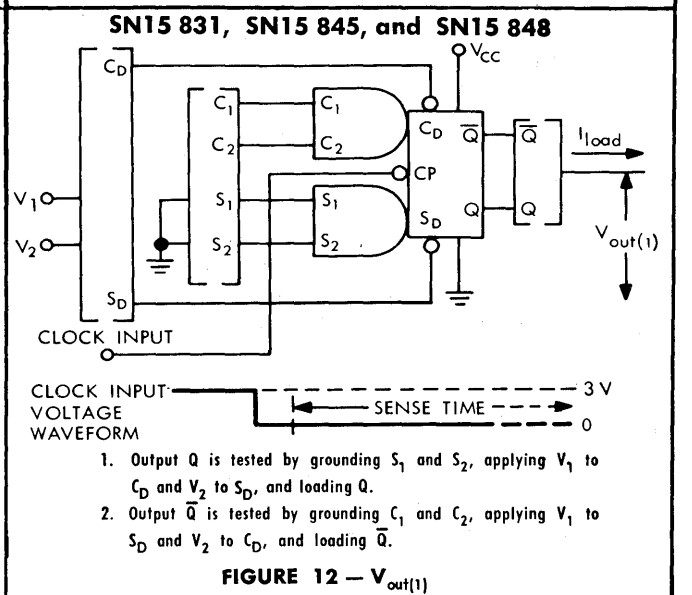
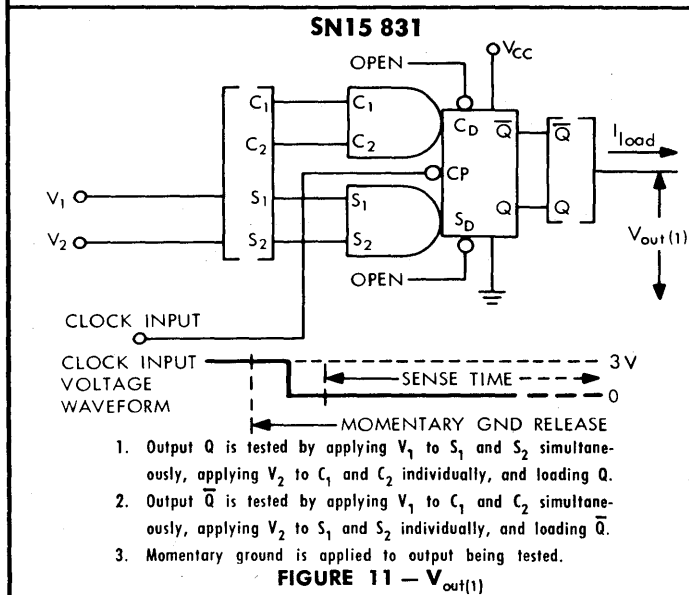
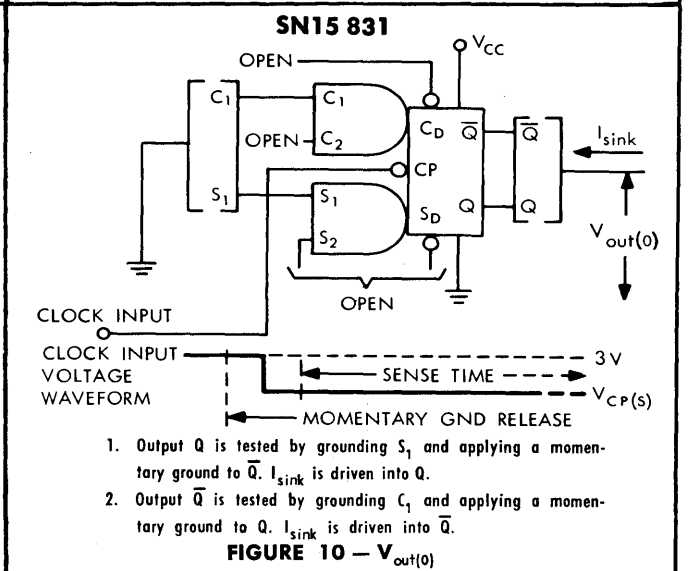
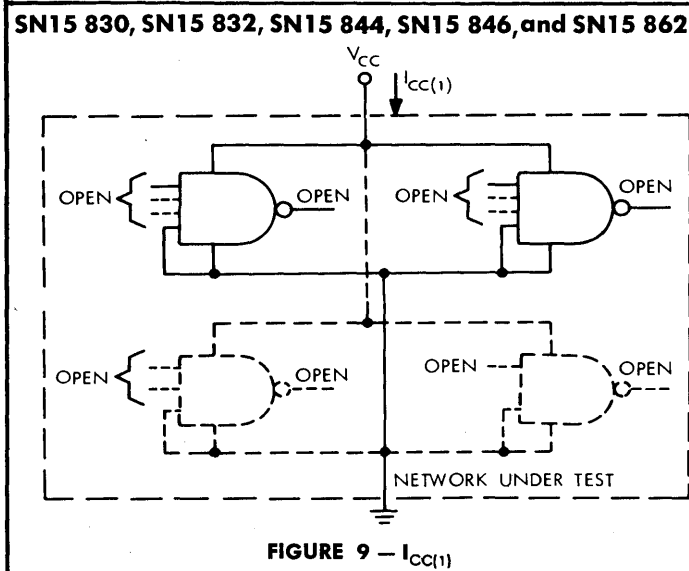
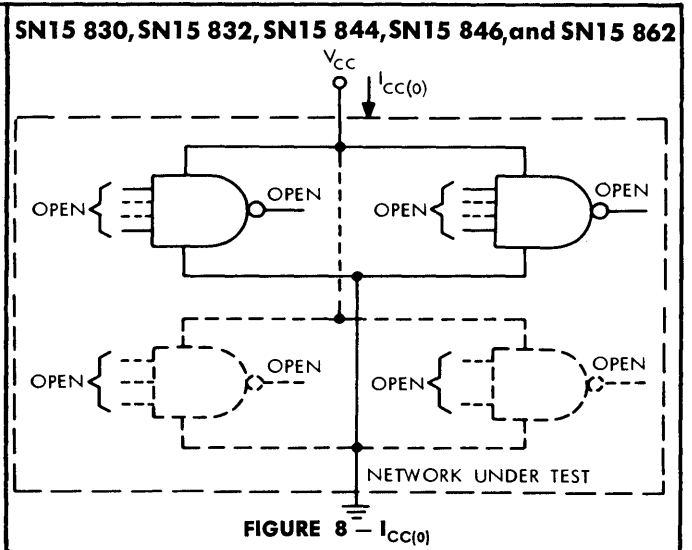
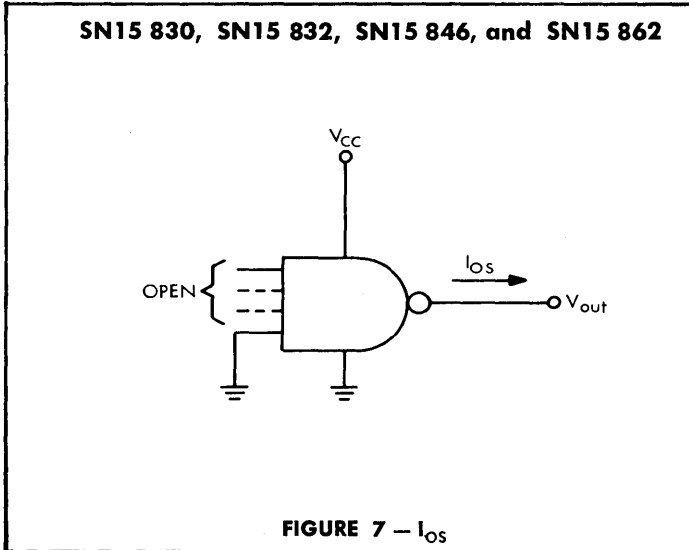
d-c test circuits †



† Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

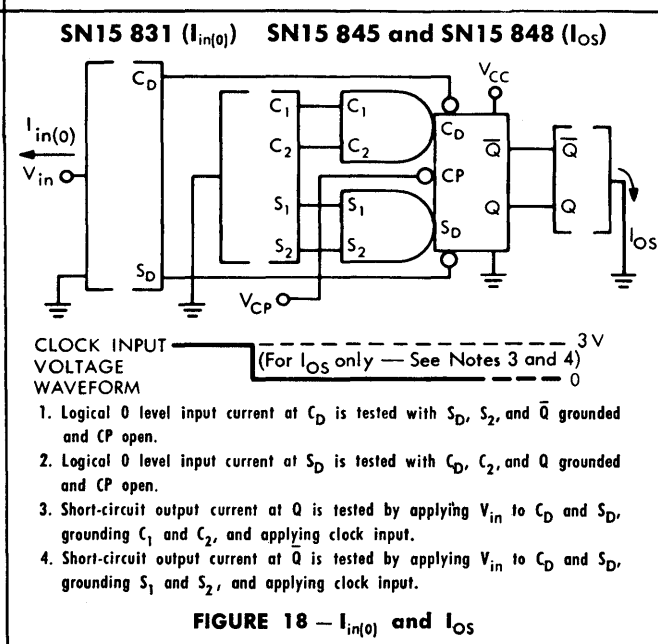
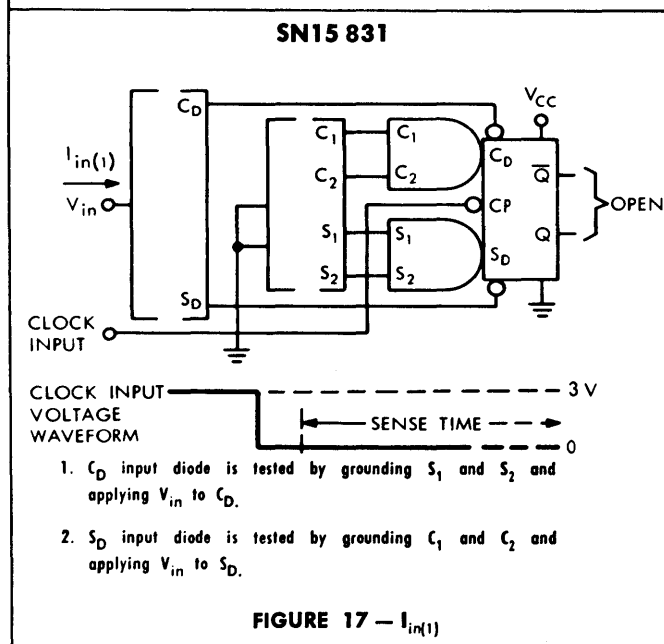
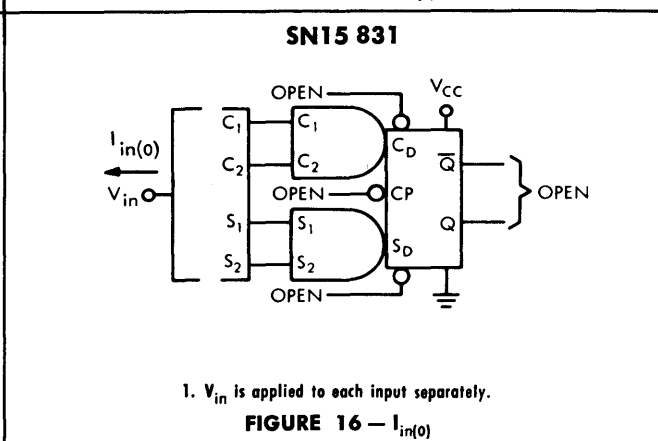
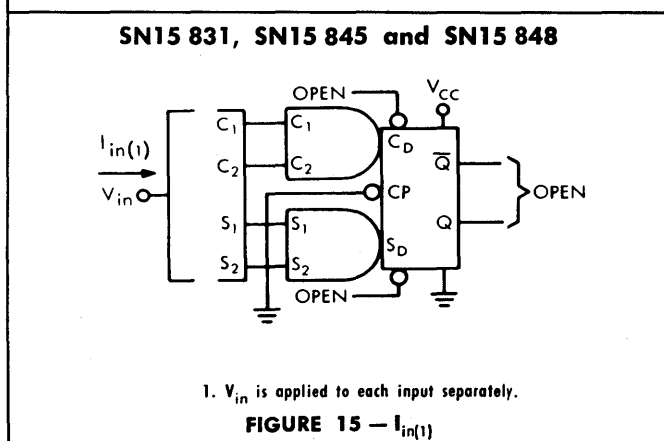
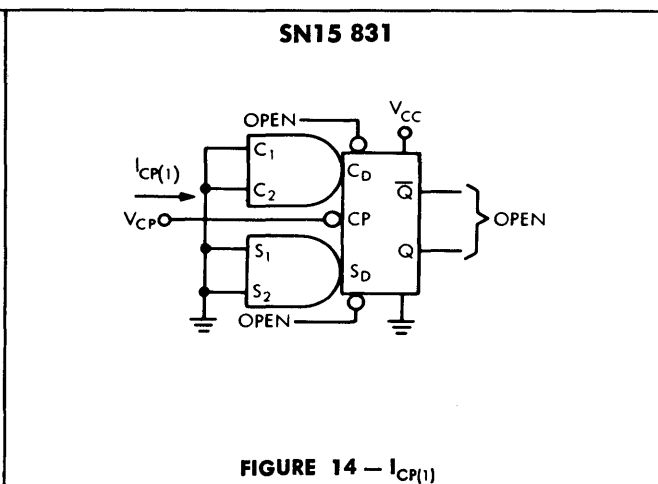
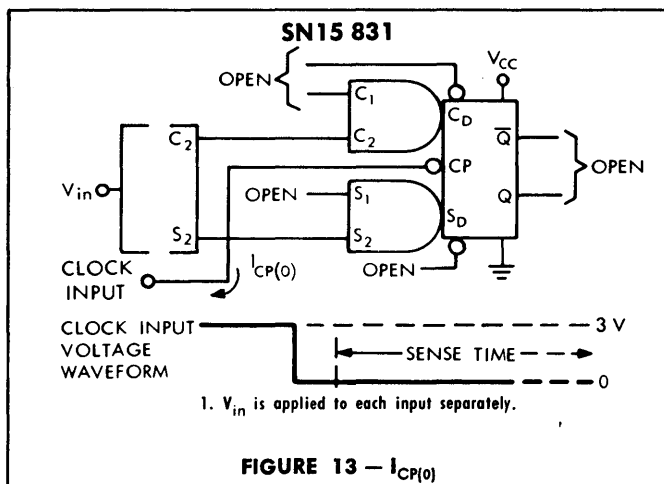
d-c test circuits<sup>†</sup> (continued)



<sup>†</sup> Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

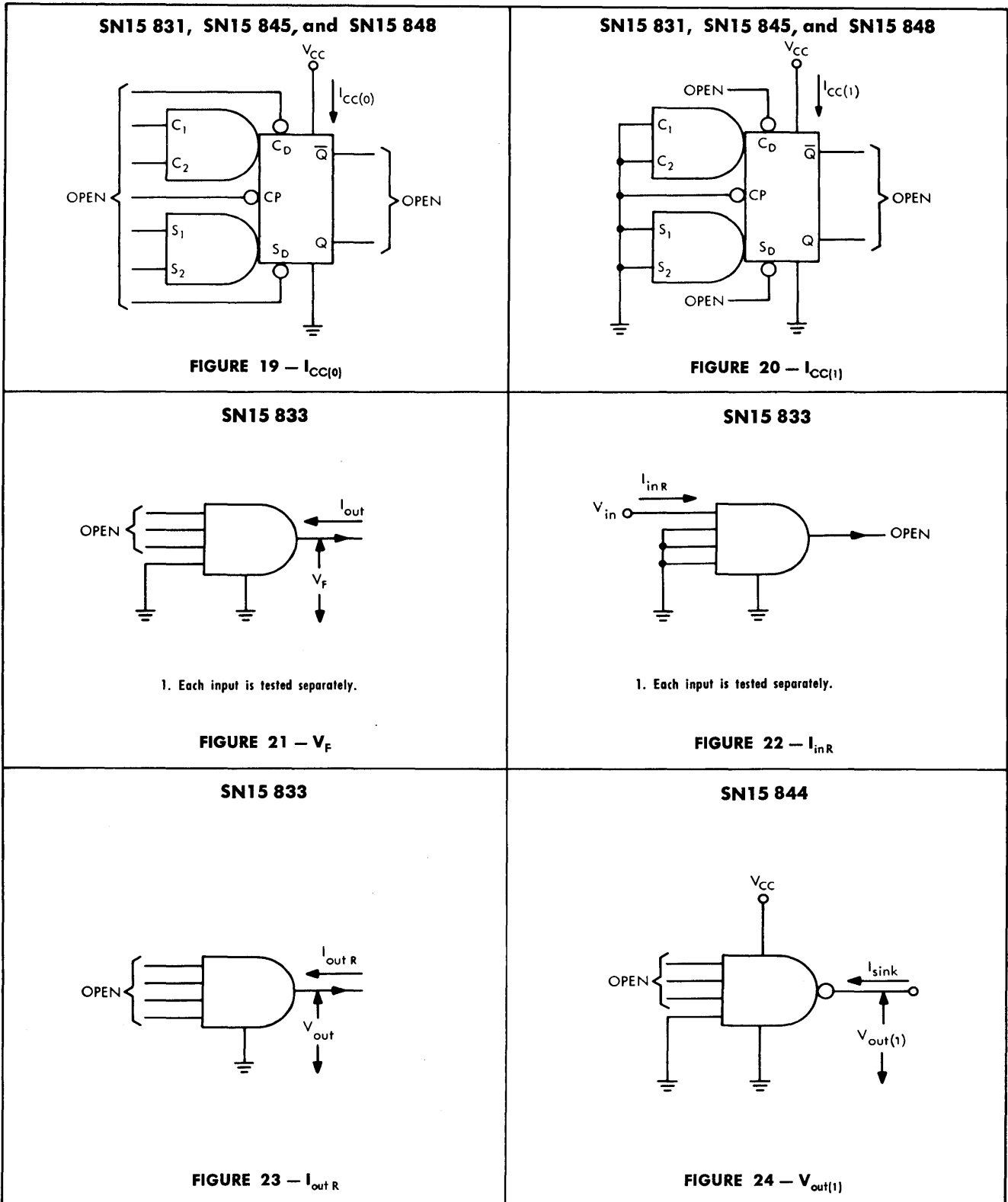
**d-c test circuits<sup>†</sup> (continued)**



<sup>†</sup> Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

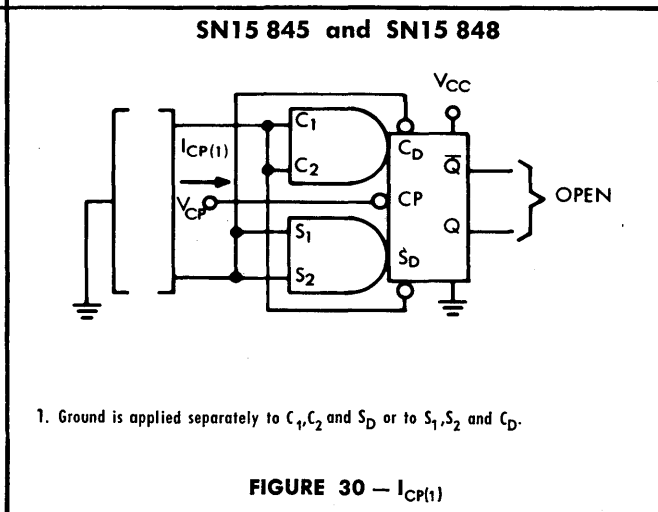
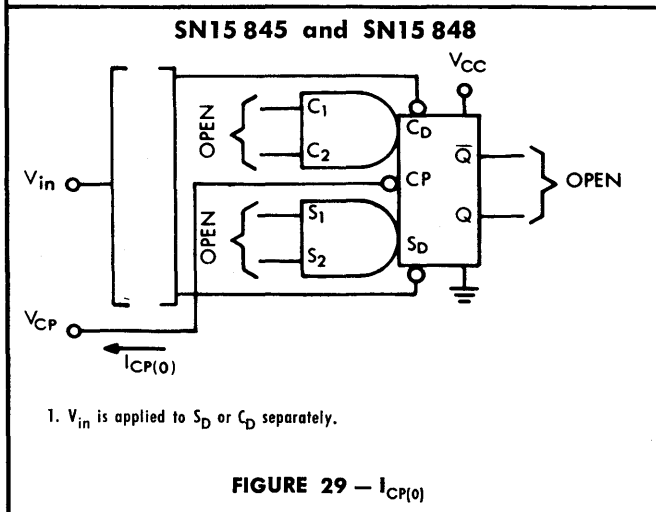
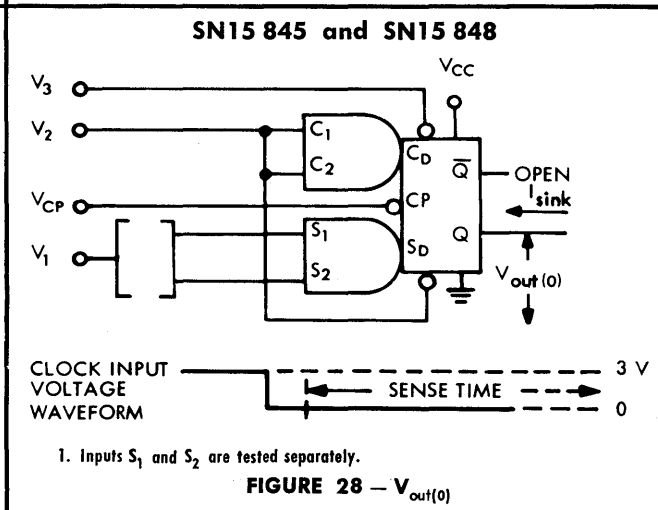
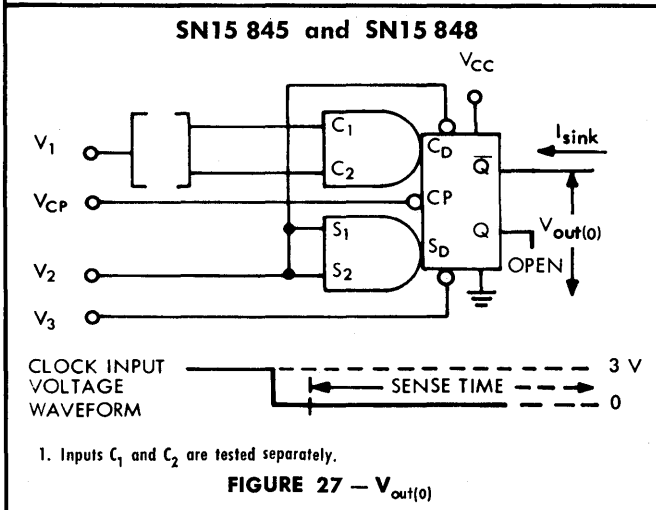
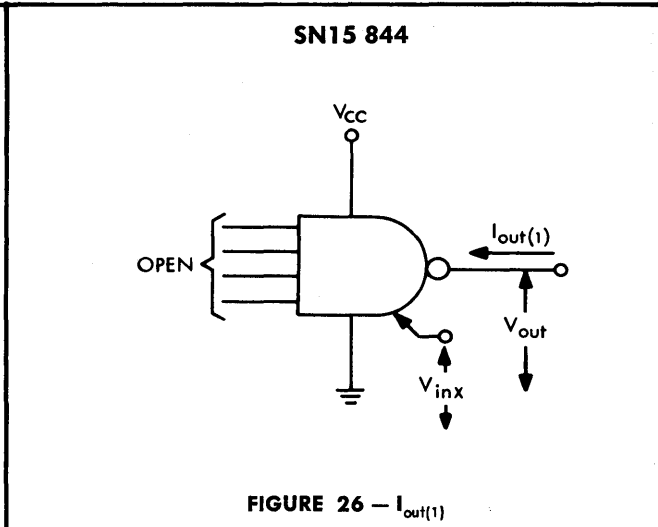
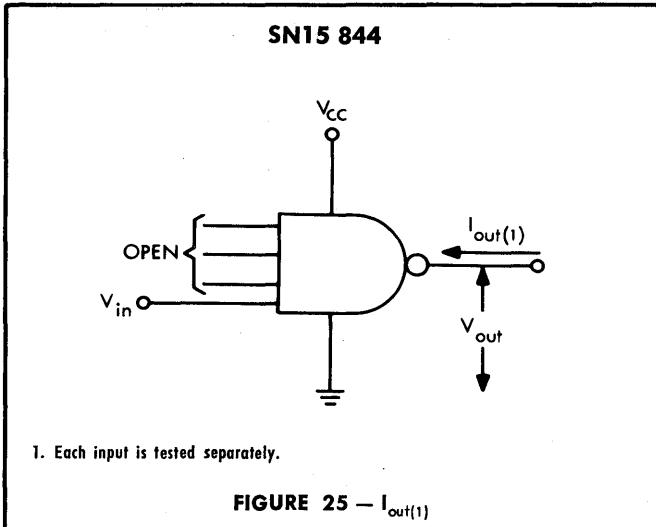
d-c test circuits<sup>†</sup> (continued)



<sup>†</sup> Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

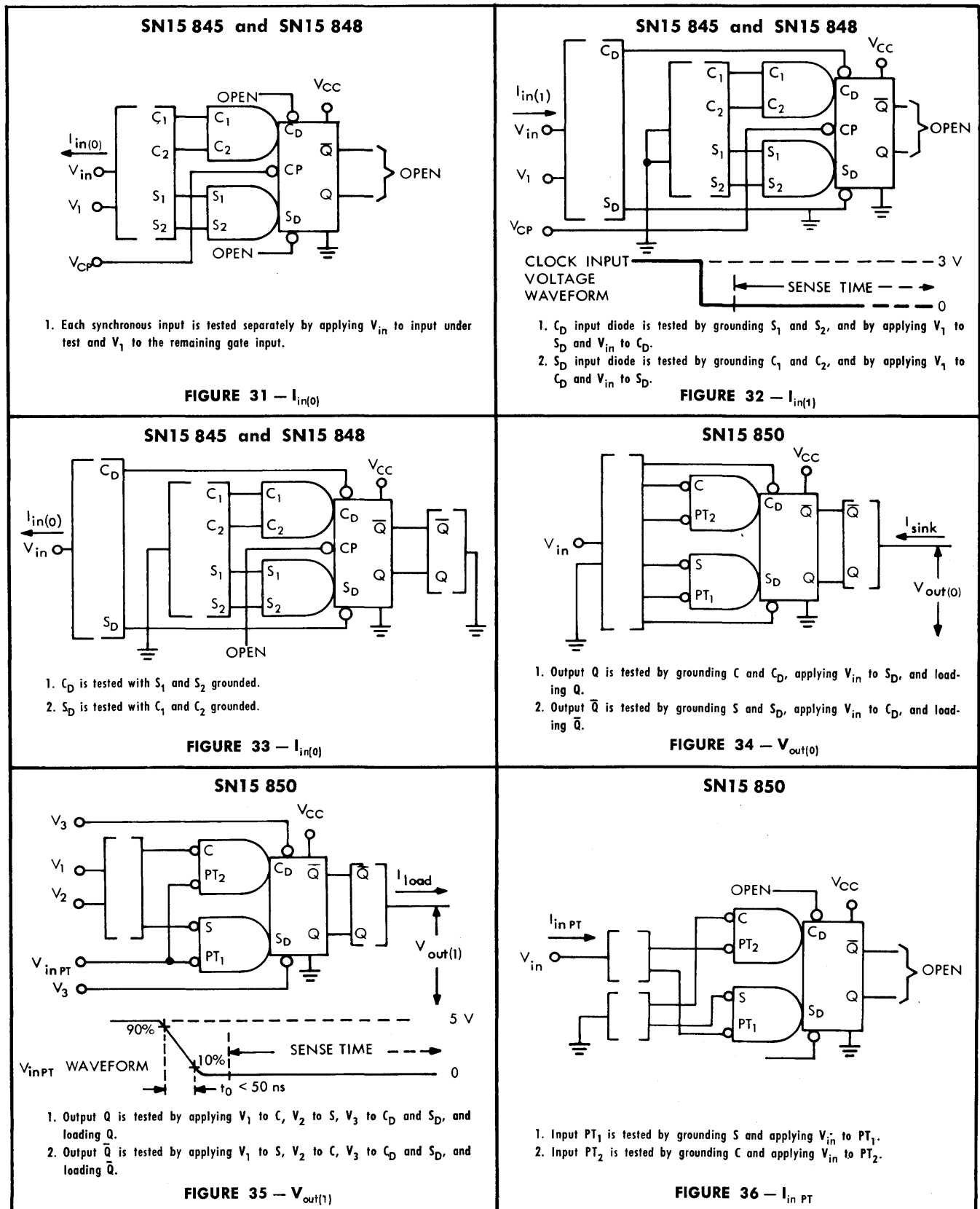
d-c test circuits † (continued)



† Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

d-c test circuits<sup>†</sup> (continued)

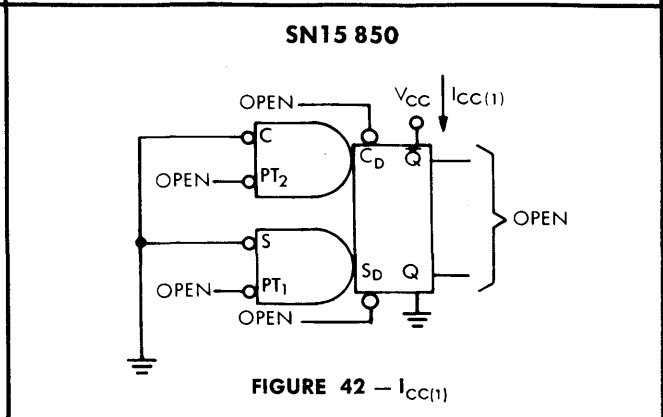
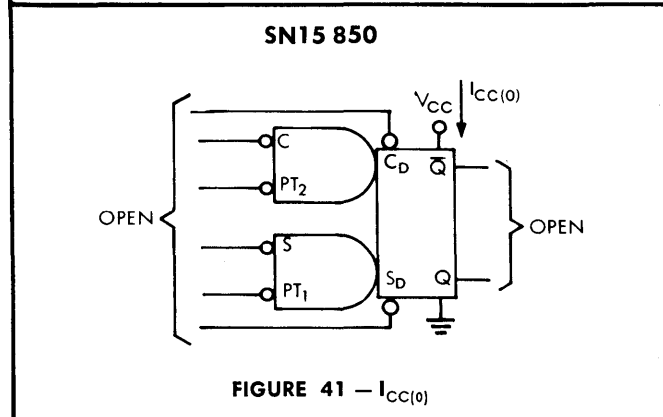
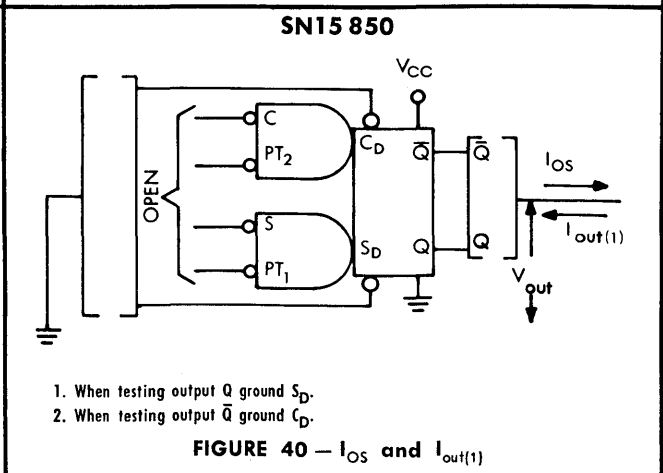
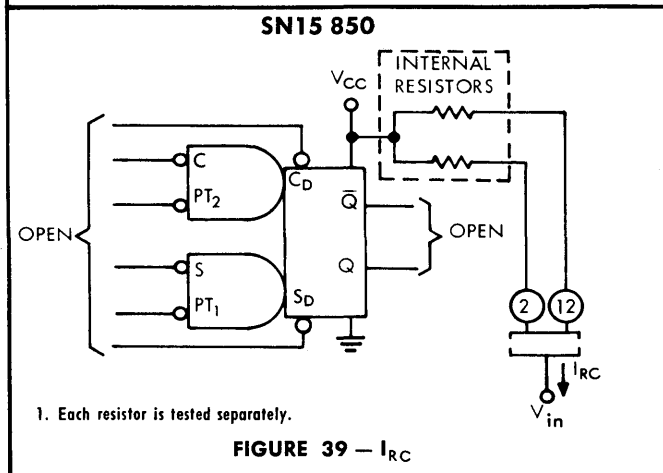
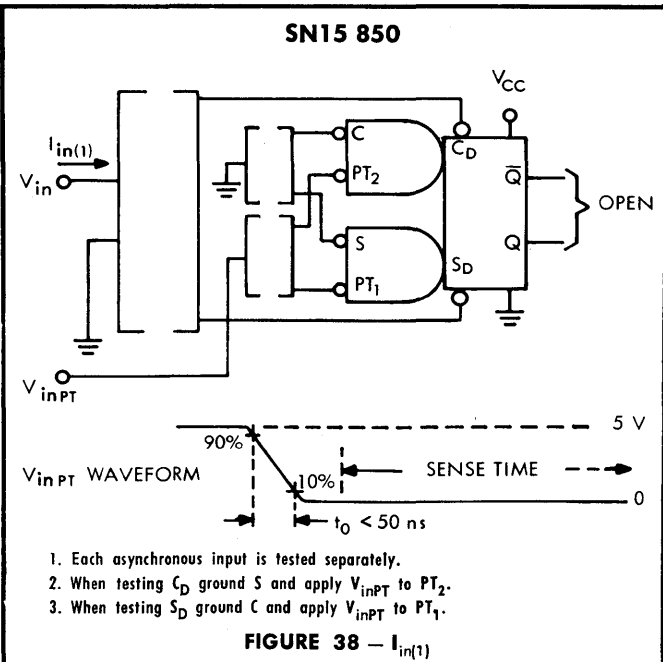
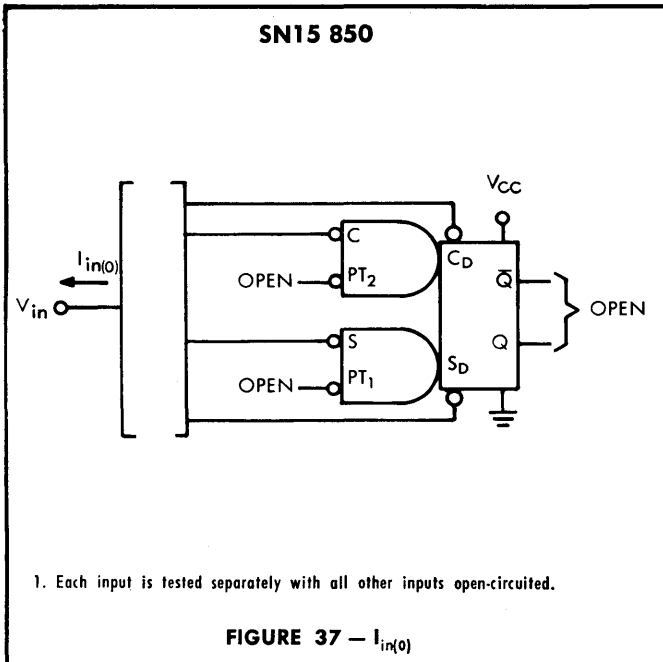


<sup>†</sup>Arrows indicate actual direction of current flow.



**PARAMETER MEASUREMENT INFORMATION**

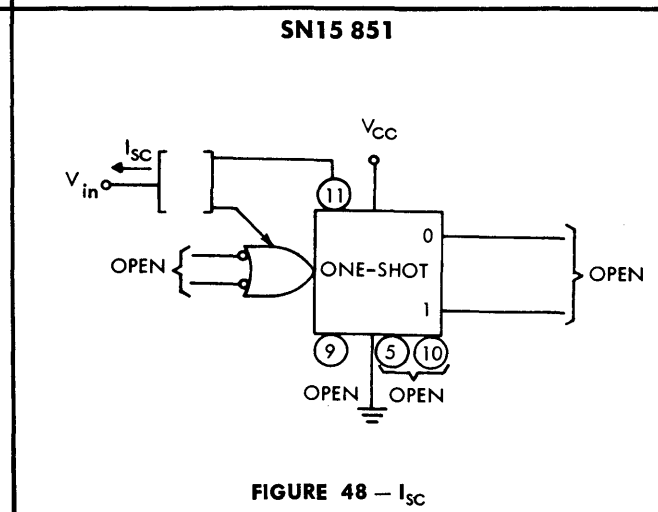
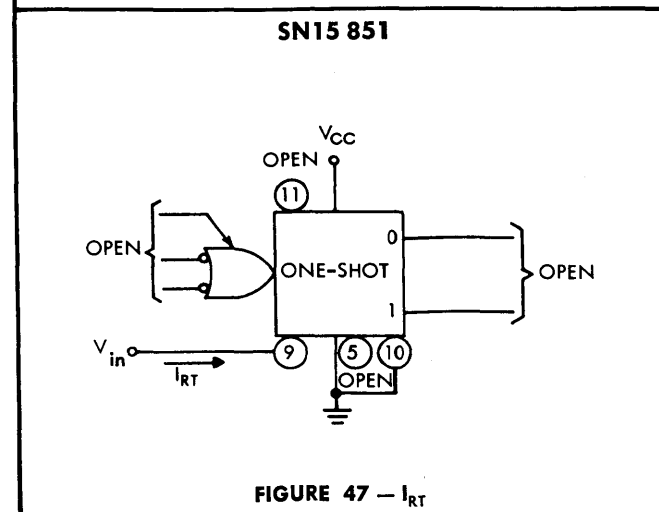
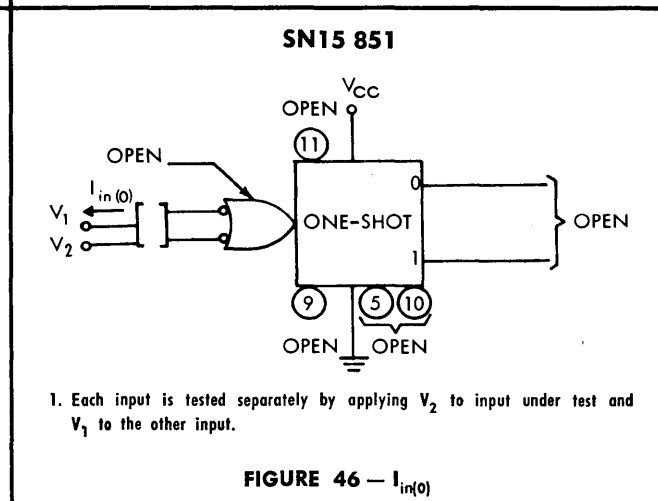
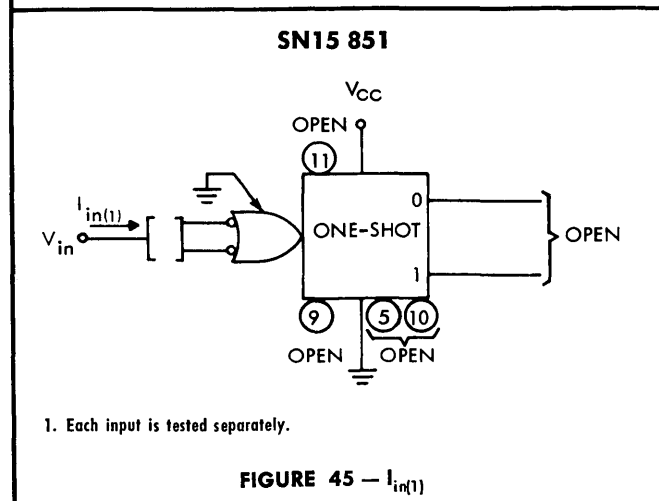
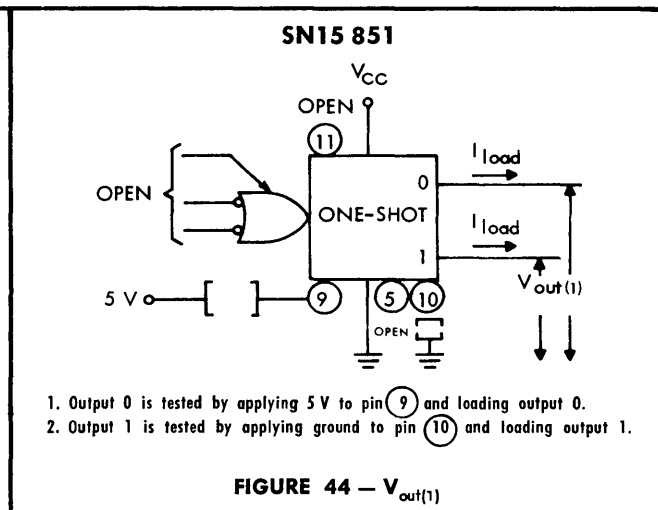
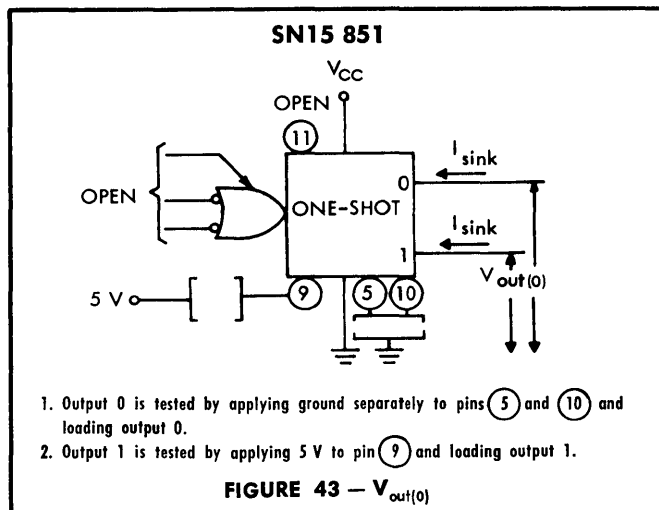
d-c test circuits<sup>†</sup> (continued)



<sup>†</sup>Arrows indicate actual direction of current flow.

**PARAMETER MEASUREMENT INFORMATION**

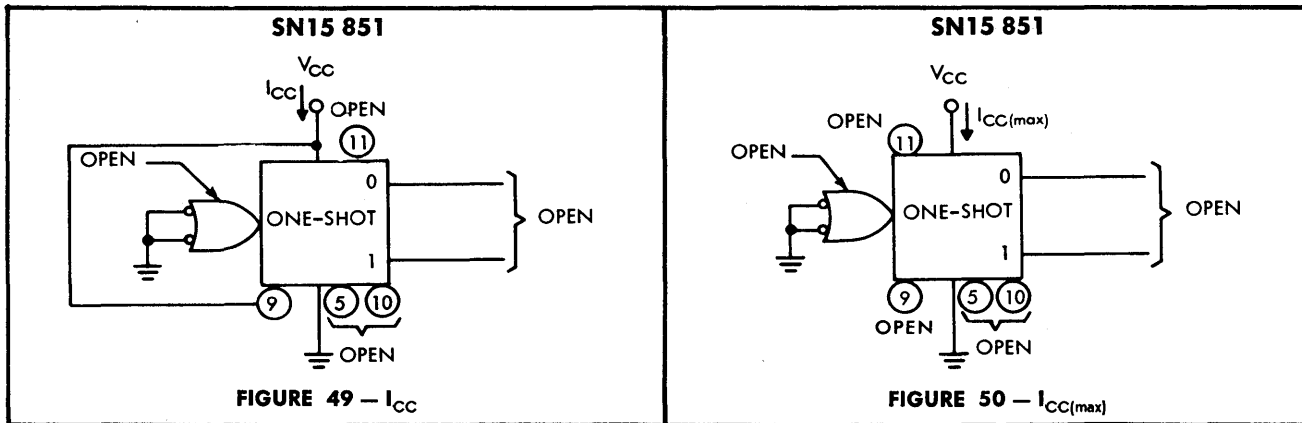
d-c test circuits<sup>†</sup> (continued)



<sup>†</sup>Arrows indicate actual direction of current flow.

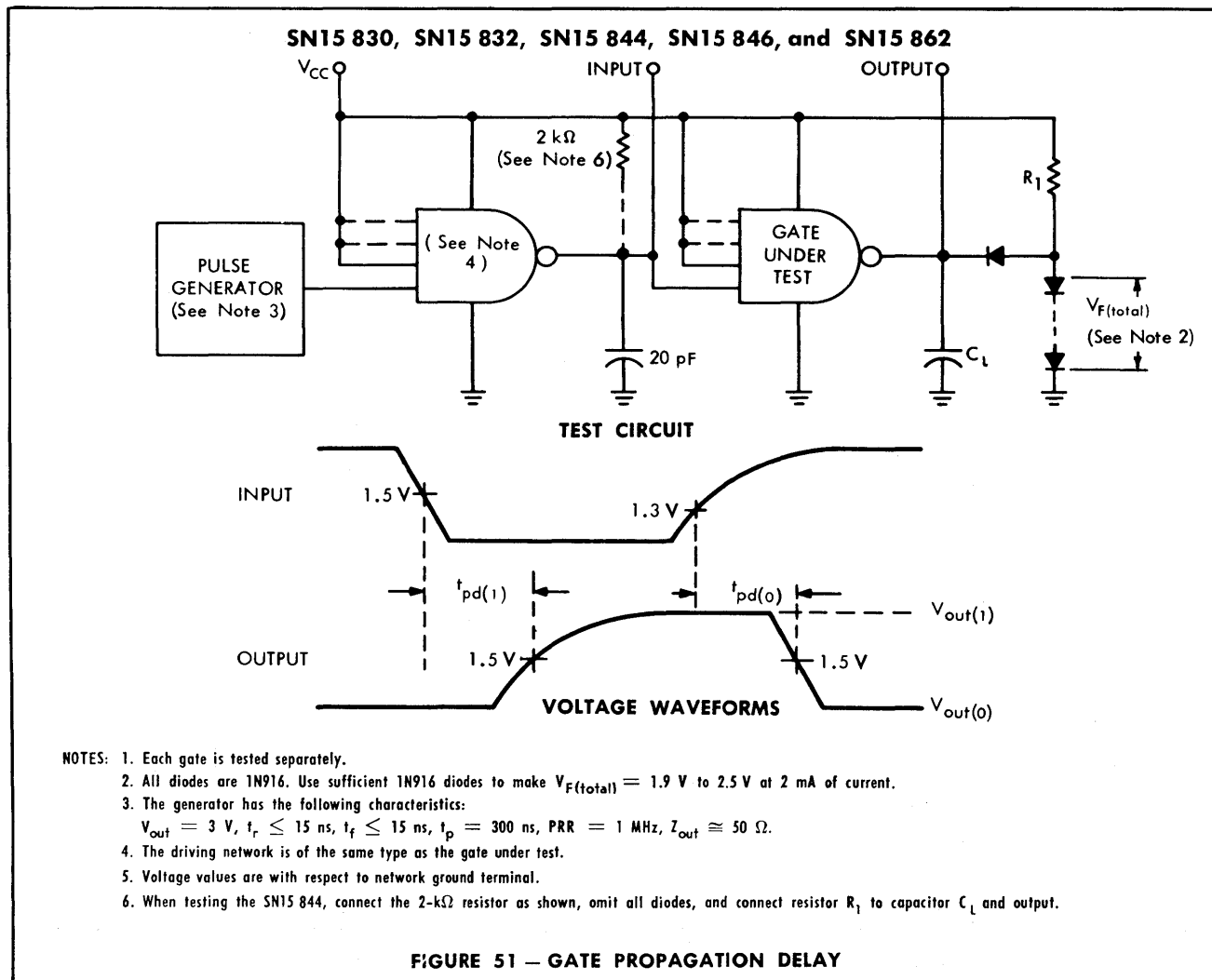
**PARAMETER MEASUREMENT INFORMATION**

**d-c test circuits<sup>†</sup> (continued)**



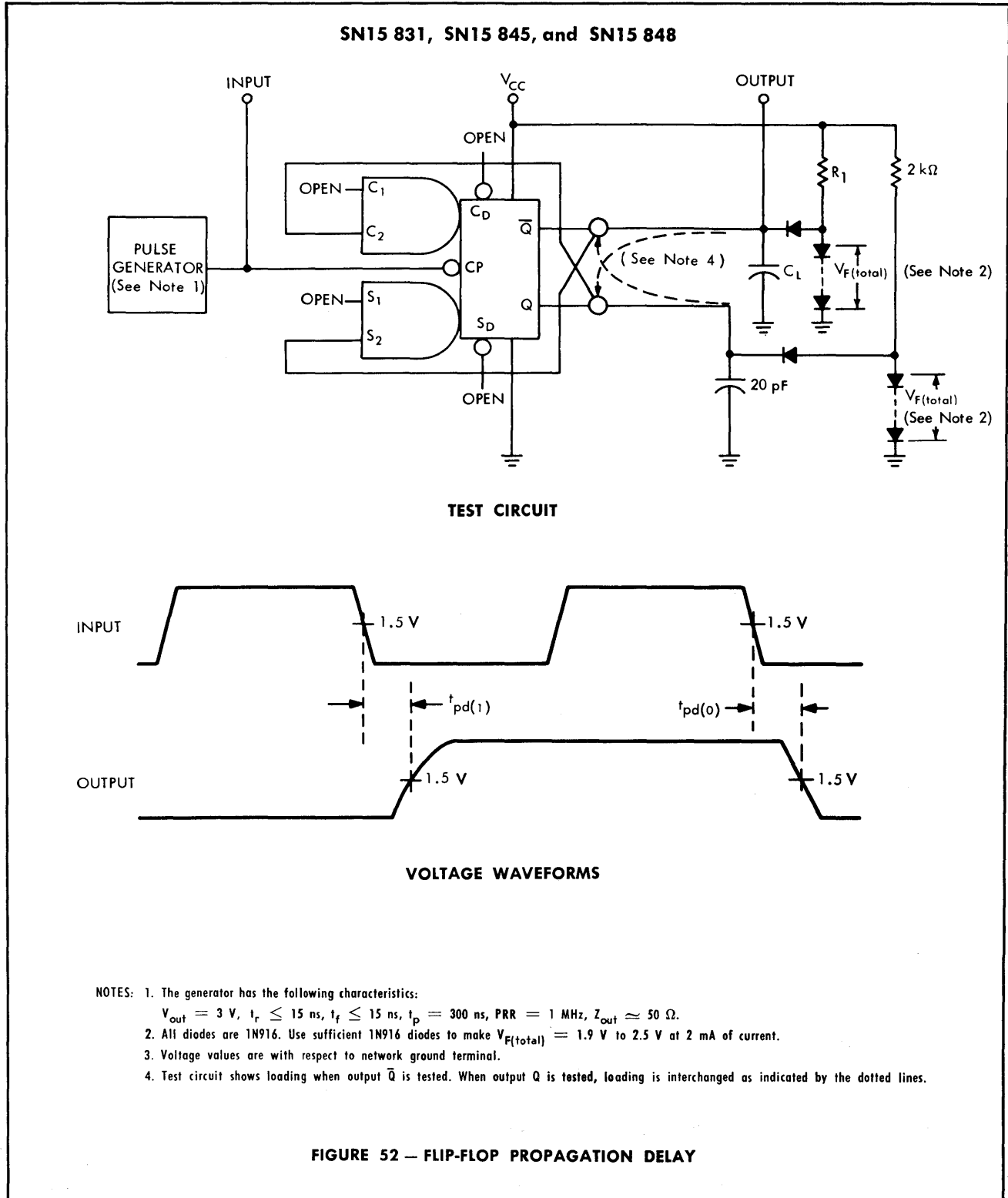
<sup>†</sup>Arrows indicate actual direction of current flow.

**switching characteristics**



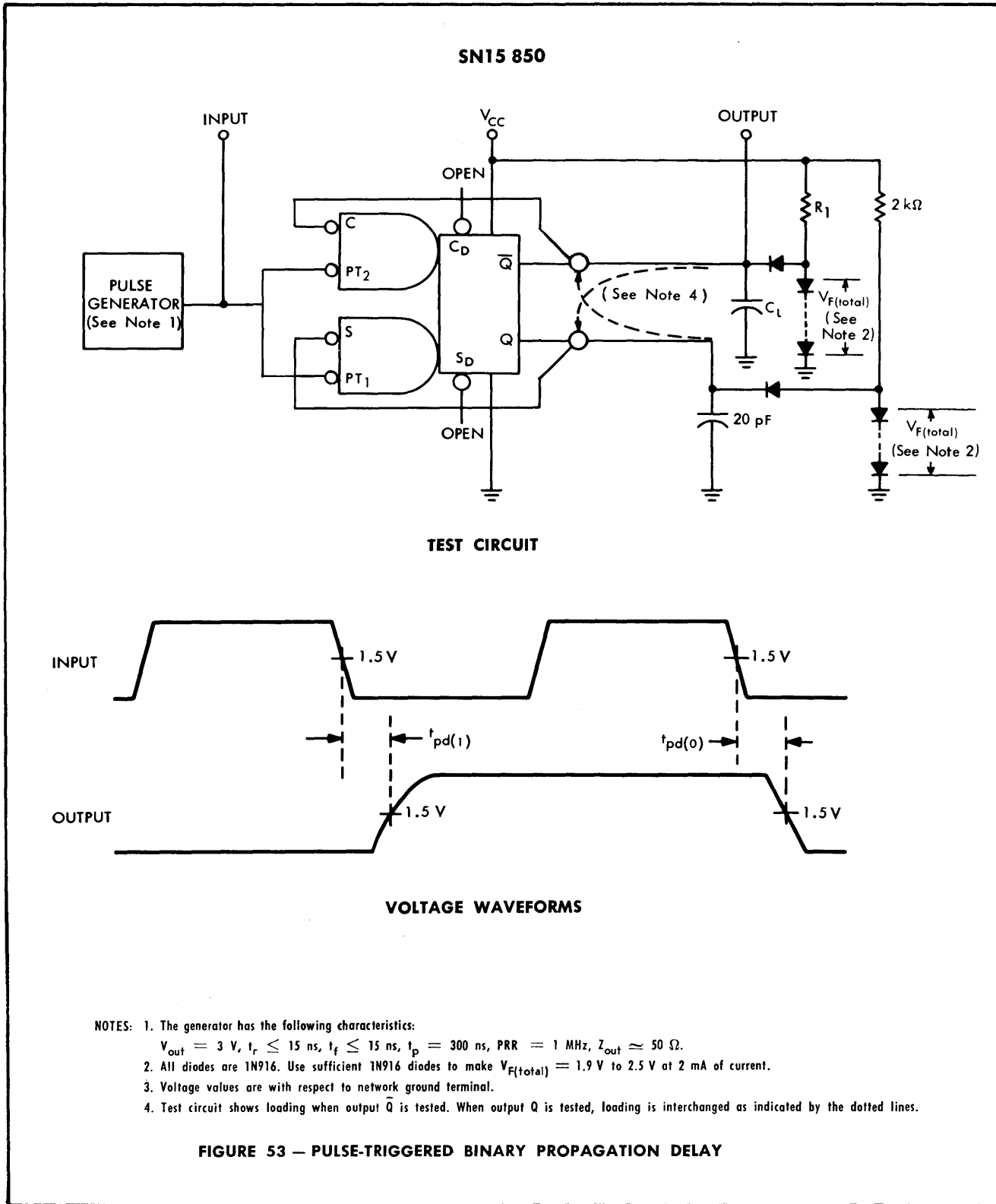
**PARAMETER MEASUREMENT INFORMATION**

**switching characteristics (continued)**

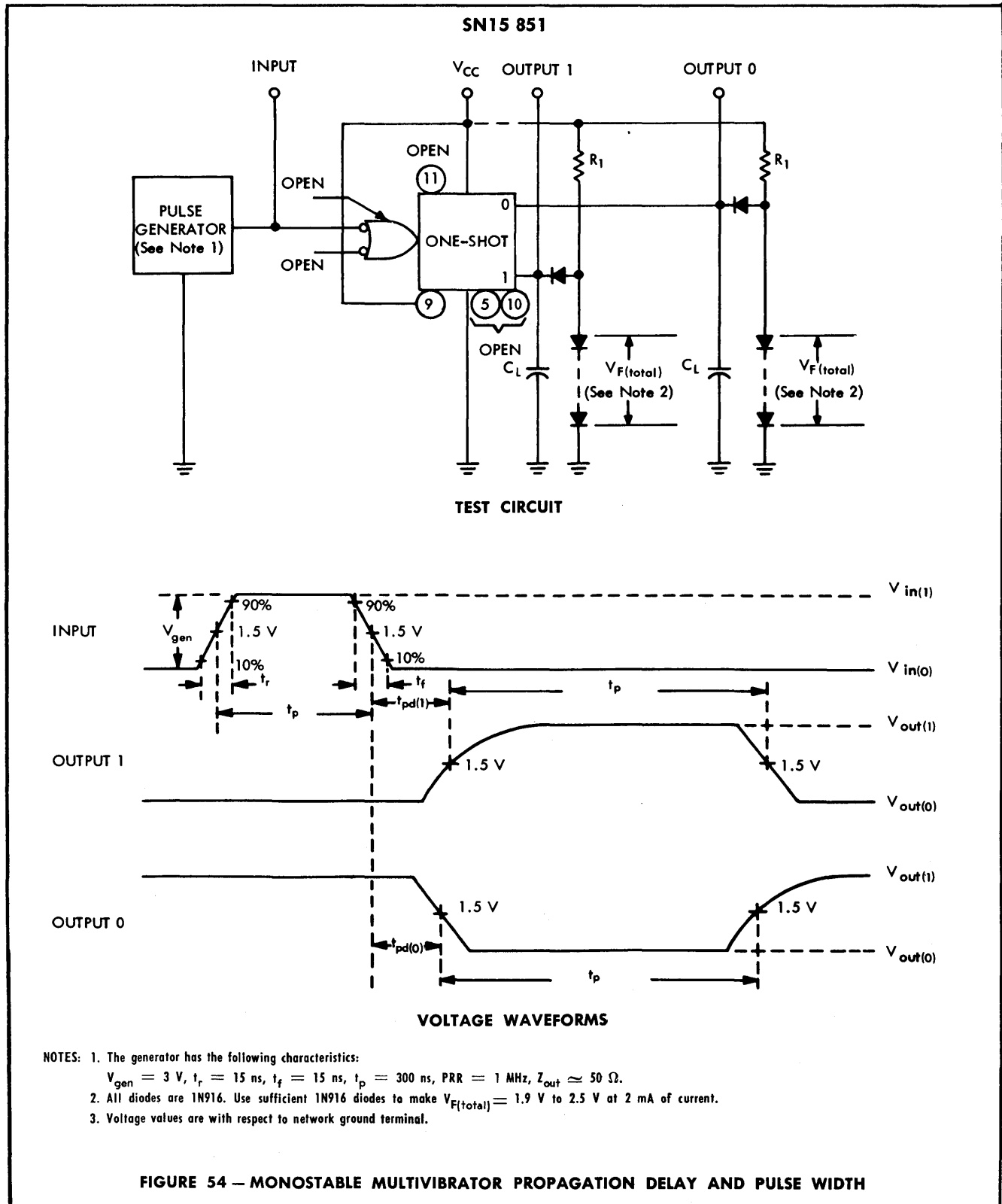


**SERIES 15830**  
**SOLID CIRCUIT<sup>®</sup> SEMICONDUCTOR NETWORKS**

switching characteristics (continued)



switching characteristics (continued)

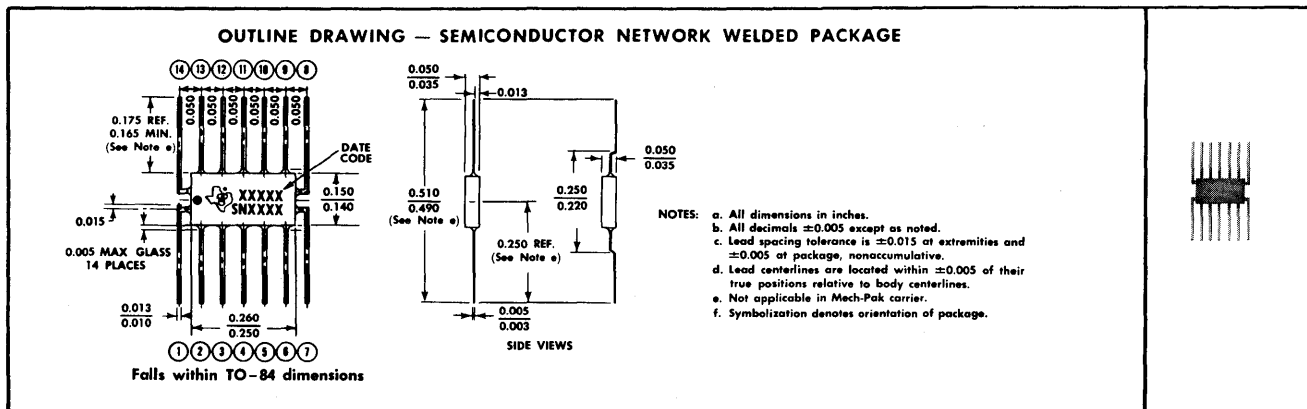


**MECHANICAL DATA**

**general**

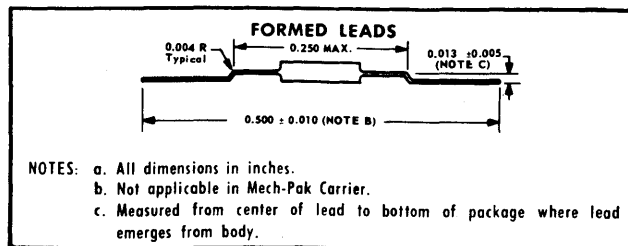
SOLID CIRCUIT semiconductor networks are mounted in a glass-to-metal hermetically sealed, welded package. Package body and leads are gold-plated F-15<sup>‡</sup> glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are

metallic and are insulated from leads and circuit. All Series 15 830 networks are available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier.



**leads**

Gold-plated F-15<sup>‡</sup> leads require no additional cleaning or processing when used in soldered or welded assembly. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Standard lead length is 0.175 inch. Networks can be removed from Mech-Pak carriers with lead lengths up to 0.175 inch.

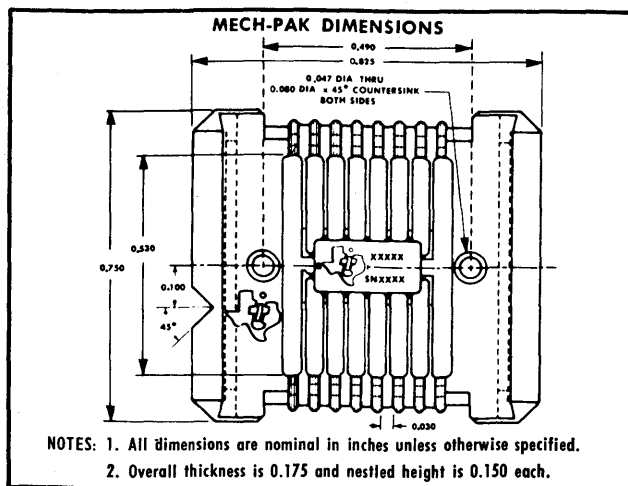


**insulator**

An insulator, secured to the back surface of the package, permits mounting networks on circuit boards which have conductors passing beneath the package. The insulator is 0.0025 inch thick and has an insulation resistance of greater than 10 megohms at 25°C.

**mech-pak carrier**

The Mech-Pak carrier facilitates handling the network, and is compatible with automatic equipment used for testing and assembly. The carrier is particularly appropriate for mechanized assembly operations and will withstand temperatures of 125°C for indefinite periods.



**ordering instructions**

Variations in mechanical configuration of semiconductor networks are identified by suffix numbers shown in a table at the right.

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
	0.175 Inch				Not Applicable			
Lead Length	No	No	Yes	Yes	No	No	Yes	Yes
Formed Leads	No	Yes	No	Yes	No	Yes	No	Yes
Insulators	None	-6	-7	-1	-2	-3	-4	-5
Ordering Suffix								

<sup>†</sup>Patented by Texas Instruments

<sup>‡</sup>F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.



**DIODE-TRANSISTOR-LOGIC SEMICONDUCTOR NETWORKS  
IN  
MOLDED PLUG-IN PACKAGES**

**description**

Series 15 830N consists of the Series 15 830 general-purpose DTL circuits mounted within a 14-pin plastic package and characterized for operation over the temperature range of 0°C to 75°C.

**features**

**LOW SYSTEM COST**

- multifunction gates offering low cost per logic function
- electrically designed specifically for monolithic integrated-circuit technology
- plug-in configuration ideal for flow-soldering techniques
- pins on 100-mil grid spacings for industrial-type circuit-boards

**PERFORMANCE**

- high speed
- high d-c noise margins
- low power dissipation
- good fan-out capability

**EASE OF DESIGN**

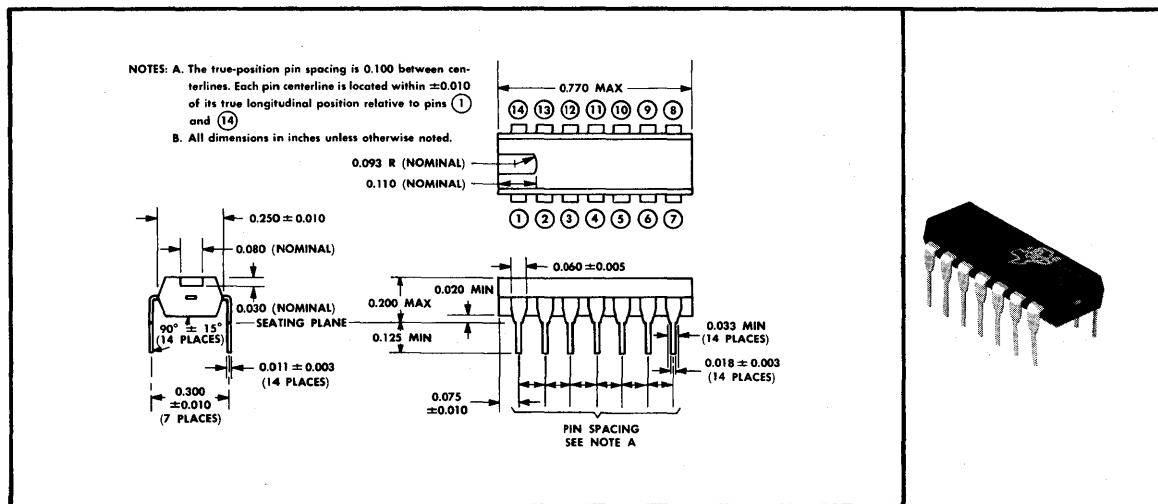
- familiar logic configuration (DTL)
- single-ended output — dot-OR logic
- complete family for design flexibility
- single power supply

**specifications, logic symbols and terminal designations**

Schematic diagrams, fan-out rules, maximum ratings, and electrical characteristics for Series 15 830N networks are identical to those of the corresponding Series 15 830 type numbers except for maximum propagation delay times‡. Terminal designations for the Series 15 830N networks are shown in this data sheet.

**mechanical data**

Series 15 830N networks are mounted on a 14-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation, and circuit performance characteristics remain stable when operated in high-humidity conditions.



<sup>†</sup>Patented by Texas Instruments

<sup>‡</sup>Maximum  $t_{pd1}$  and  $t_{pd0}$  for Series 15 830N are 5 ns higher than for Series 15 830. The increase in the typical or median value is negligible.

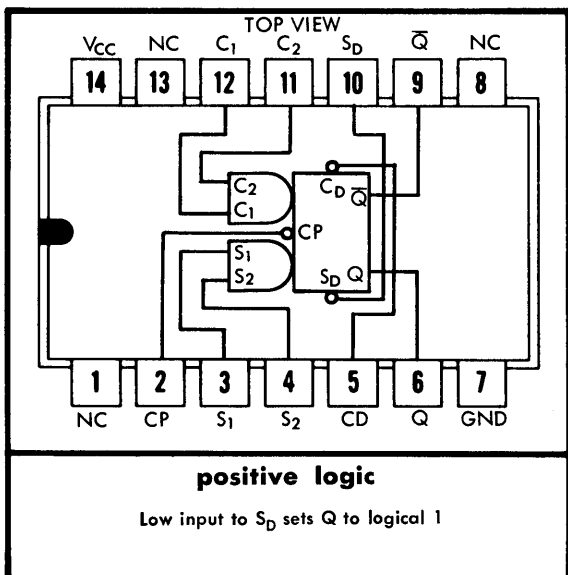




# SERIES 15 830N

## SOLID CIRCUIT<sup>®</sup> SEMICONDUCTOR NETWORKS

### SN15 831N, SN15 845N, SN15 848N MASTER-SLAVE FLIP-FLOPS



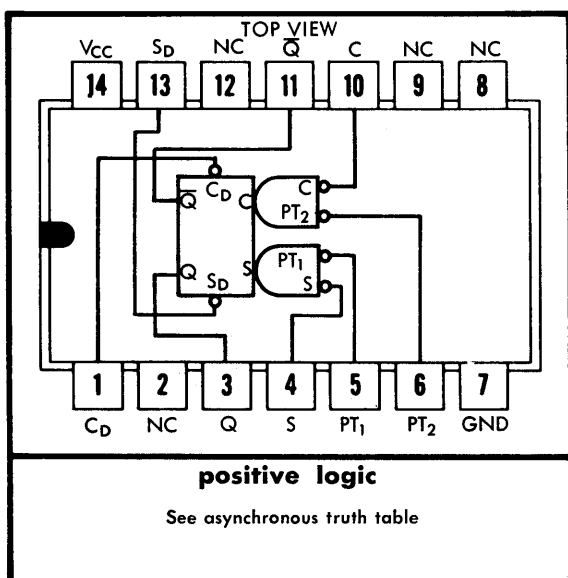
#### TRUTH TABLES

R-S MODE				
$t_n$				$t_{n+1}$
$S_1$	$S_2$	$C_1$	$C_2$	$Q$
0	X	0	X	$Q_n$
0	X	X	0	$Q_n$
X	0	0	X	$Q_n$
X	0	X	0	$Q_n$
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	Indeterminate

J-K MODE		
$t_n$		$t_{n+1}$
$S_1$	$C_1$	$Q$
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\bar{Q}_n$

- NOTES:
- $t_n$  = bit time before clock pulse.
  - $t_{n+1}$  = bit time after clock pulse.
  - X indicates that either a logical 1 or a logical 0 may be present.
  - Logical 1 is more positive than logical 0.
  - For operation in the J-K mode connect  $S_2$  to  $\bar{Q}$ , and  $C_2$  to  $Q$ .

### SN15 850N PULSE-TRIGGERED BINARY



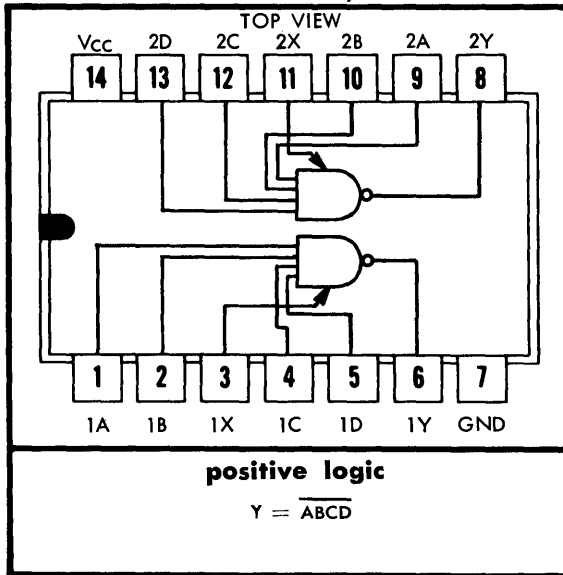
#### TRUTH TABLES

SYNCHRONOUS					
$t_n$ PULSE INPUT				$t_{n+1}$ OUTPUT	
S	C	PT <sub>1</sub>	PT <sub>2</sub>	Q	$\bar{Q}$
1	X	X	1	$Q_n$	$\bar{Q}_n$
X	1	1	X	$Q_n$	$\bar{Q}_n$
0	1	0	X	1	0
0	X	0	1	1	0
1	0	X	0	0	1
X	0	1	0	0	1
0	0	0	0	Indeterminate	

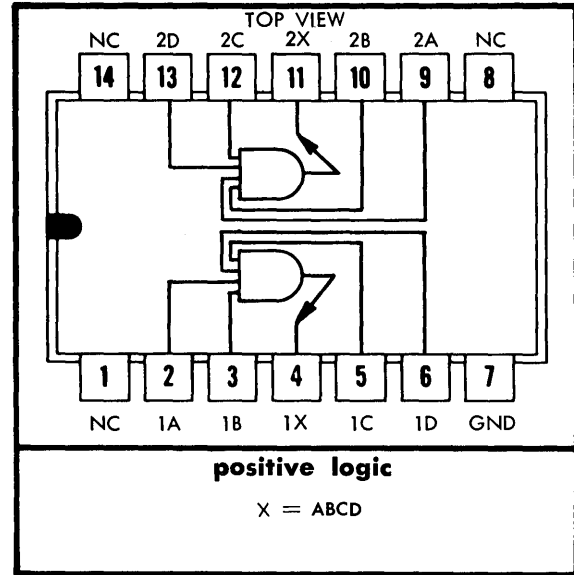
ASYNCHRONOUS			
DIRECT INPUT		OUTPUT	
$S_D$	$C_D$	Q	$\bar{Q}$
1	1	$Q_n$	$\bar{Q}_n$
0	1	0	1
1	0	1	0
0	0	1	1

- NOTES:
- X indicates that either a logical 1 or a logical 0 may be present.
  - Logical 1 is more positive than logical 0.
  - Logical states shown for pulse inputs  $PT_1$  and  $PT_2$  indicate that a transition to that state has just occurred.
  - Truth tables reflect individual conditions at the inputs. Either direct input may be used to inhibit its corresponding pulse input.

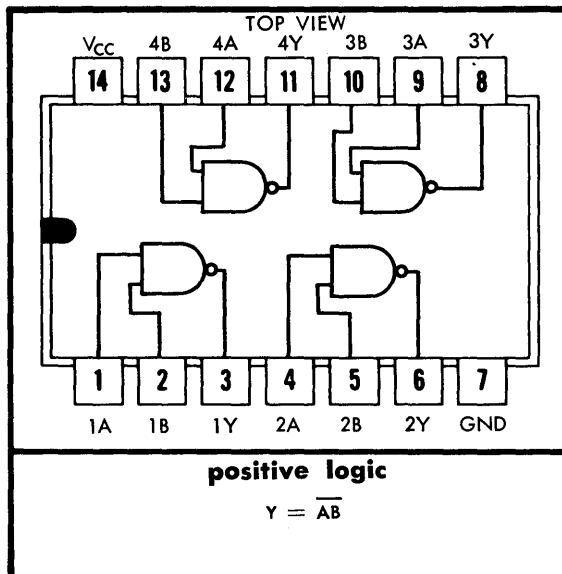
**SN15 830N, SN15 832N (BUFFER), SN15 844N (POWER)**  
**DUAL 4-INPUT NAND/NOR GATES**



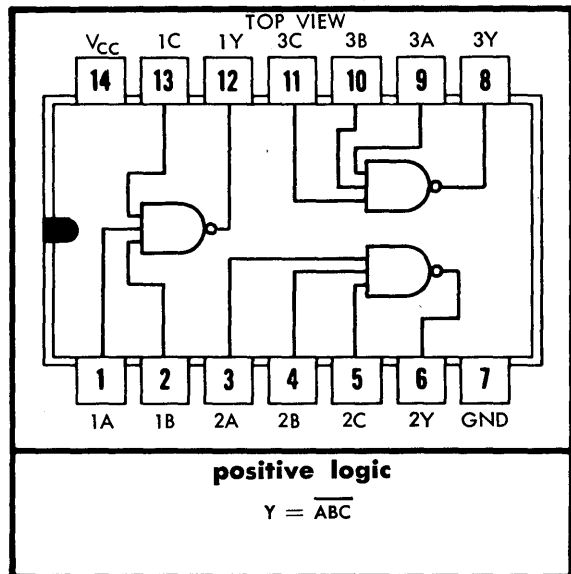
**SN15 833N**  
**DUAL 4-INPUT EXPANDER**



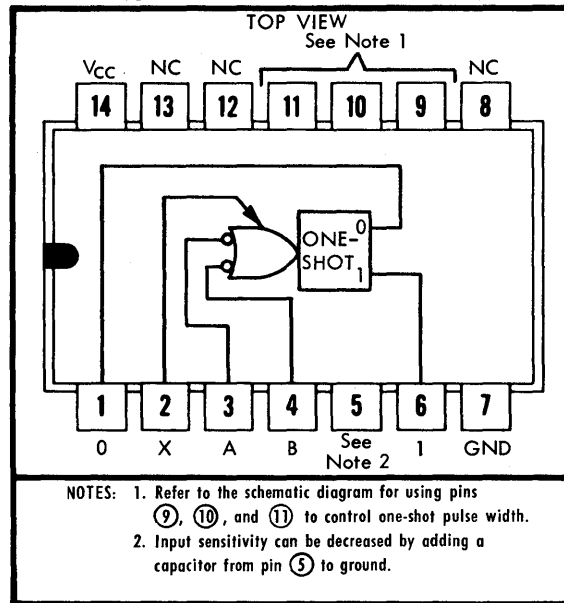
**SN15 846N**  
**QUADRUPLE 2-INPUT NAND/NOR GATE**



**SN15 862N**  
**TRIPLE 3-INPUT NAND/NOR GATE**



**SN15 851N  
MONOSTABLE MULTIVIBRATOR**





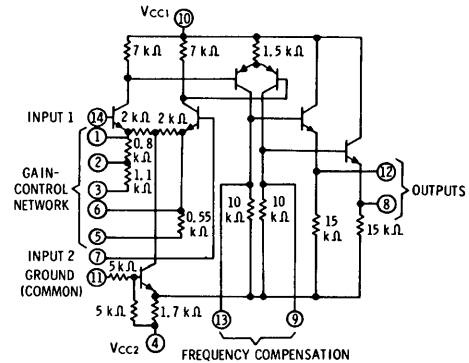
**SERIES 72 SEMICONDUCTOR-NETWORK GENERAL-PURPOSE AMPLIFIER**  
for application as

- Comparator
- Level Detector
- Differential Amplifier
- Voltage Regulator
- Military & Industrial Control Systems
- Analog-to-Digital Converters
- Analog Computers

**description**

The SN723, offering differential inputs and differential emitter-follower outputs, incorporates a resistance network in the emitters of the input stage to facilitate gain adjustment. From the wide range of total resistance available, a particular value may be selected by connecting the resistor-network pins in a configuration which produces the desired gain. Maximum-gain configuration is with pin ① shorted to pin ⑥.

The SN723, one of Texas Instruments Series 72 catalog line of linear integrated circuits, offers higher reliability, lower cost, smaller size, and lower weight than equivalent discrete-component circuits. Each Series 72 device is a monolithic semiconductor structure comprising diffused resistors and both n-p-n and p-n-p transistors.



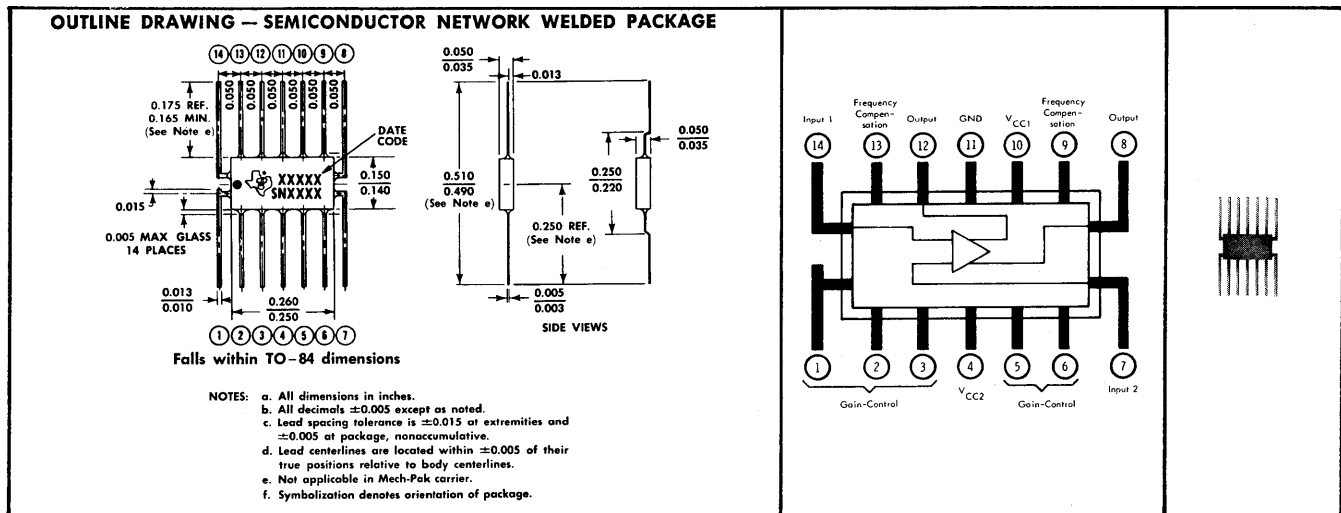
NOTE: Component values shown are nominal.  
**SCHEMATIC DIAGRAM**

**mechanical data**

The SN723 is mounted in a glass-to-metal hermetically sealed welded package meeting TO-84. Leads are gold-plated F-15<sup>‡</sup> glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. The SN723 is available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier. See Ordering Instructions.

**ORDERING INSTRUCTIONS**

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5



<sup>†</sup>Patented by Texas Instruments.

<sup>‡</sup>F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 24% nickel, and 17% cobalt.



# TYPE SN723

## GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltages (See Note 1): $V_{CC1}$ . . . . .	+15 V
$V_{CC2}$ . . . . .	-15 V
Differential Input Voltage . . . . .	$\pm 6$ V
Input Voltage (Either Input, See Note 1) . . . . .	$\pm 10$ V
Duration of Short-Circuit Output Current . . . . .	5 s
Continuous Total Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 2) . . . . .	300 mW
Operating Free-Air Temperature Range . . . . .	0°C to 70°C
Storage Temperature Range . . . . .	-65°C to 150°C

- NOTES: 1. These voltage values are with respect to network ground.  
 2. Derate linearly to 220 mW at 70°C free-air temperature at the rate of 1.8 mW/deg.

### electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>§</sup>	MIN	TYP	MAX	UNIT
$V_{DI}$ Differential-input offset voltage			4	15	mV
$\alpha_{VDI}$ Differential-input offset voltage temperature coefficient	$T_A = 0^\circ\text{C to } 70^\circ\text{C}$		10		$\mu\text{V/deg}$
$V_{CMO}$ Common-mode output offset voltage			600		mV
$I_{in}$ Input current			6.5		$\mu\text{A}$
$I_{DI}$ Differential-input offset current			1	4	$\mu\text{A}$
$V_{OM}$ Maximum peak-to-peak output voltage	Differential output, $f = 1 \text{ kc/s}$		20		V
	Differential output, $f = 1 \text{ kc/s}$ , $T_A = 0^\circ\text{C to } 70^\circ\text{C}$	15			V
$V_{CMIM}$ Maximum common-mode input voltage			$\pm 5$		V
$A_{VD}$ Differential voltage gain	$f = 1 \text{ kc/s}$		3000		
	$f = 1 \text{ kc/s}$ , $T_A = 0^\circ\text{C to } 70^\circ\text{C}$	1250			
	$f = 1 \text{ kc/s}$ , pins ① and ② open		120		
	$f = 1 \text{ kc/s}$ , pin ① shorted to pin ②, pin ③ open		800		
	$f = 1 \text{ kc/s}$ , pin ② shorted to pin ③, pins ① and ④ open		440		
	$f = 1 \text{ kc/s}$ , pin ③ shorted to pin ④, pins ① and ② open		300		
	$f = 1 \text{ kc/s}$ , pin ② shorted to pin ④, pin ① open		620		
CMRR Common-mode rejection ratio	$f = 1 \text{ kc/s}$		80		dB
BW Bandwidth (-3 dB)		60	150		kc/s
$Z_{in}$ Input impedance	$f = 1 \text{ kc/s}$	4	10		$\text{k}\Omega$
$Z_{out}$ Output impedance	$f = 1 \text{ kc/s}$		250		$\Omega$
$P_T$ Total power dissipation			100		mW

<sup>§</sup>Unless otherwise noted, test conditions are:

$V_{CC1} = +12 \text{ V}$ ,  $V_{CC2} = -12 \text{ V}$ ,  $V_{DI}$  applied, no external loading; pin ① grounded, pin ② shorted to pin ③, and pins ④, ⑤, ⑥, ⑦ and ⑧ open.

### letter symbol and parameter definitions

- $V_{DI}$  That d-c voltage which must be applied between the input terminals to obtain zero-differential-output voltage. The application of this voltage balances the amplifier.
- $V_{CMO}$  That d-c voltage level which exists between either output terminal and ground when the outputs are balanced.
- $I_{in}$  The current into either input of the amplifier.
- $I_{DI}$  The difference in the currents into the two input terminals when the output is balanced.
- $V_{OM}$  The maximum peak-to-peak output voltage swing that can be obtained without clipping when the output is balanced.
- $V_{CMIM}$  The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.
- CMRR The ratio of the differential-mode voltage gain to the common-mode voltage gain.
- BW The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.
- $Z_{in}$  The impedance between either input terminal and ground with the other input terminal a-c grounded and the output balanced.
- $Z_{out}$  The impedance between the output terminal and ground when the output is balanced.

# TYPE SN723 GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

## TYPICAL CHARACTERISTICS§

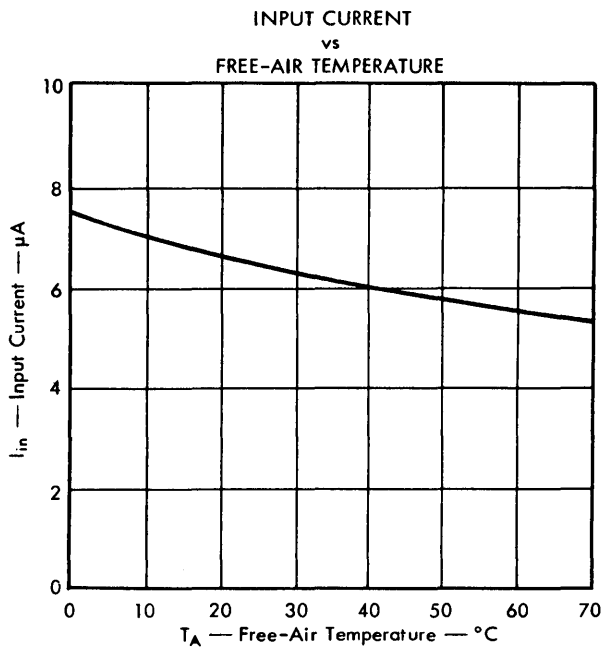


FIGURE 1

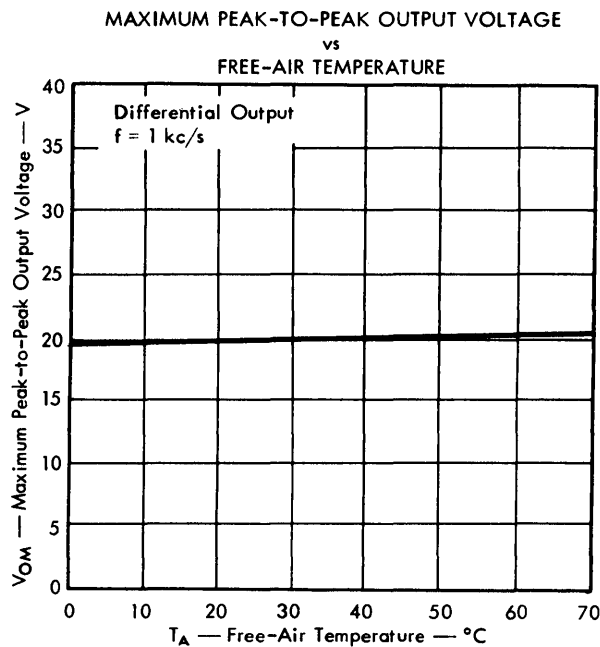


FIGURE 2

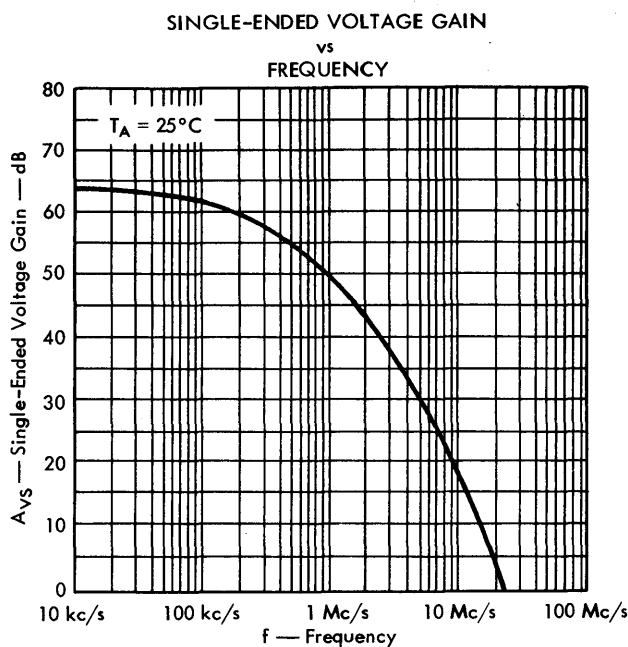


FIGURE 3

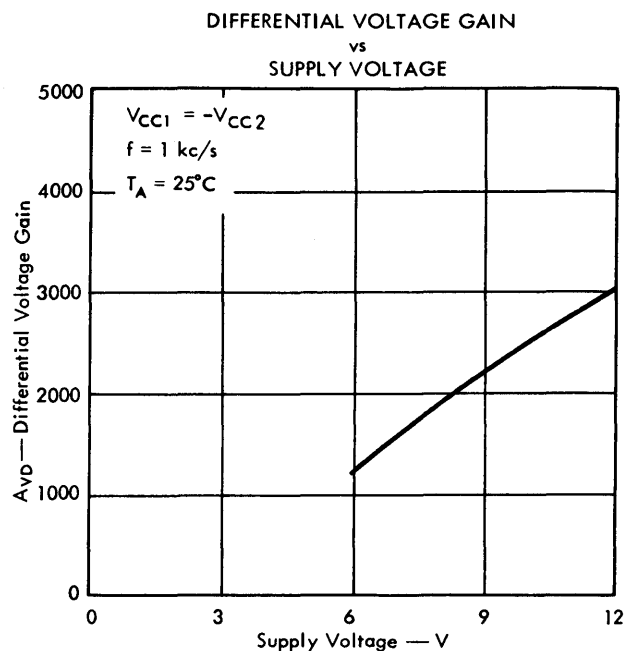


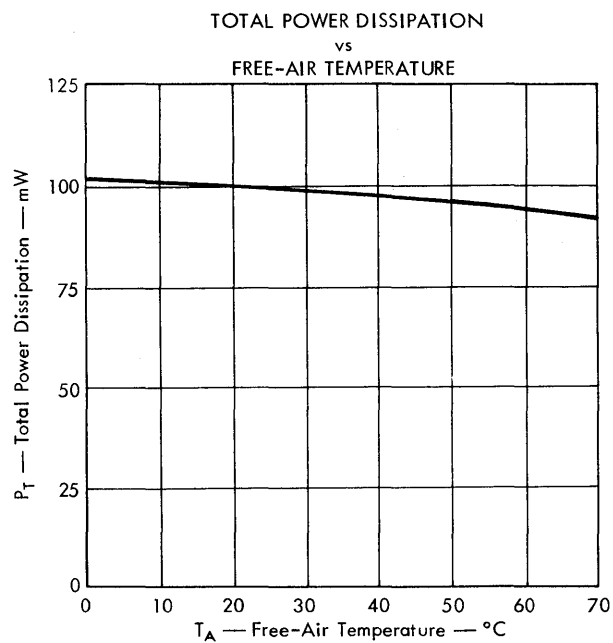
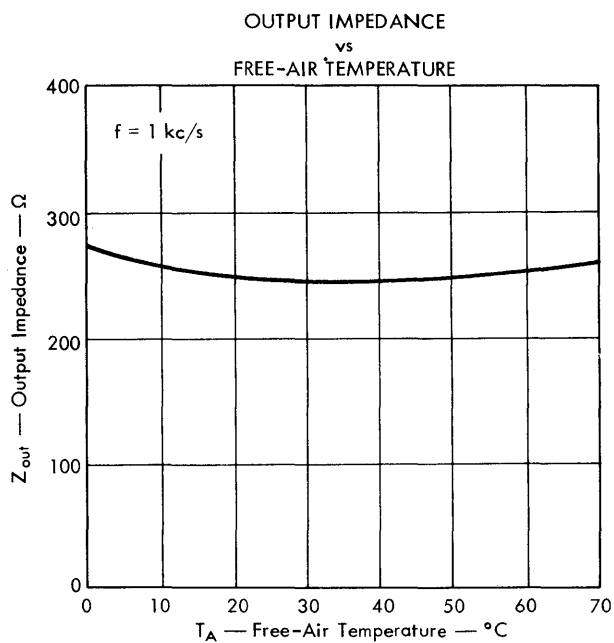
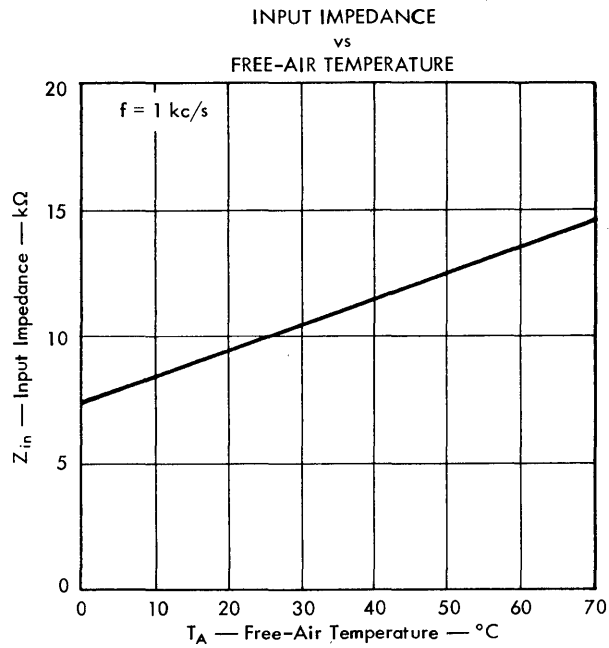
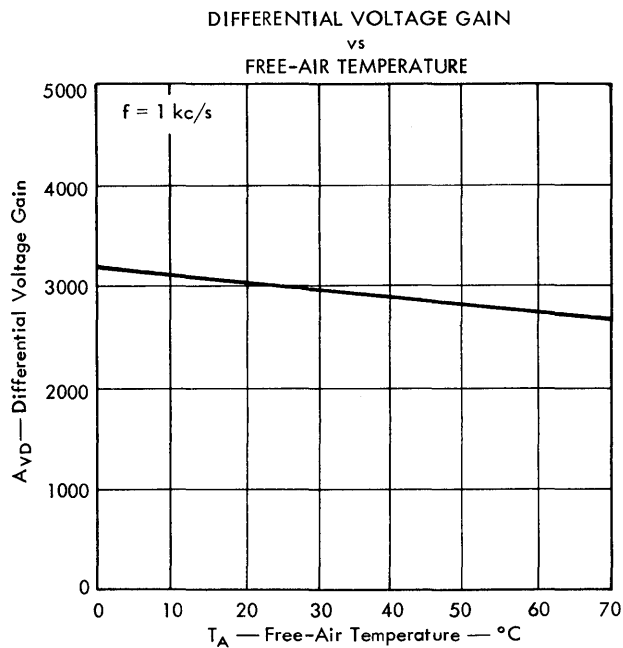
FIGURE 4

§Unless otherwise noted, test conditions are:

$V_{CC1} = +12\text{ V}$ ,  $V_{CC2} = -12\text{ V}$ ,  $V_{D1}$  applied, no external loading; pin ① grounded, pin ① shorted to pin ⑥, and pins ②, ③, ⑤, ⑨ and ⑬ open.

# TYPE SN723 GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

## TYPICAL CHARACTERISTICS§



§Unless otherwise noted, test conditions are:

$V_{CC1} = +12\text{ V}$ ,  $V_{CC2} = -12\text{ V}$ ,  $V_{DI}$  applied, no external loading, pin ⑪ grounded, pin ① shorted to pin ⑥, and pins ②, ③, ⑤, ⑨ and ⑬ open.

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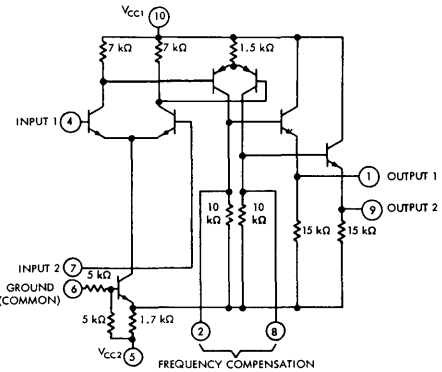
**SERIES 72 SEMICONDUCTOR-NETWORK GENERAL-PURPOSE AMPLIFIER**  
for application as

- Comparator
- Level Detector
- Differential Amplifier
- Voltage Regulator
- Military & Industrial Control Systems
- Analog-to-Digital Converters
- Analog Computers

**description**

The SN7231L offers differential inputs and differential emitter-follower outputs. Two stages of differential amplification are used to provide high gain at frequencies up to 1 MHz. A high degree of component matching, which assures stable operation over the temperature range of 0°C to 70°C, is achieved by the monolithic construction.

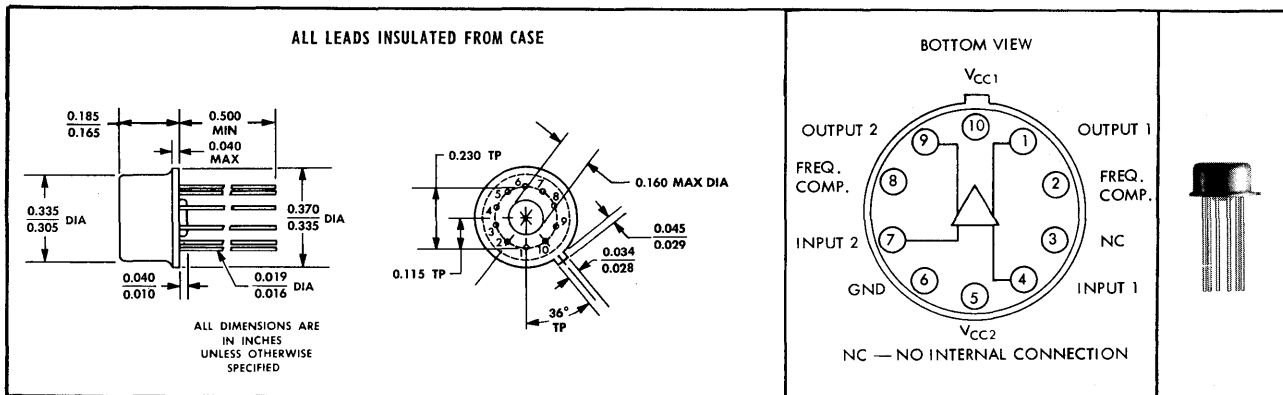
The SN7231L, one of Texas Instruments Series 72 catalog line of linear integrated circuits, offers higher reliability, lower cost, smaller size, and lower weight than equivalent discrete-component circuits. Each Series 72 device is a monolithic semiconductor structure comprising diffused resistors and both n-p-n and p-n-p transistors.



NOTE: Component values shown are nominal.  
**SCHEMATIC DIAGRAM**

**mechanical data**

The SN7231L package outline is same as JEDEC TO-100 except for diameter of standoff.



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply Voltages (See Note 1): $V_{CC1}$	.....	+ 15 V
$V_{CC2}$	.....	- 15 V
Differential Input Voltage	.....	± 6 V
Input Voltage (Either Input, See Note 1)	.....	± 10 V
Duration of Short-Circuit Output Current	.....	5 s
Continuous Total Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 2)	.....	300 mW
Operating Free-Air Temperature Range	.....	0°C to 70°C
Storage Temperature Range	.....	-65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground.  
2. Derate linearly to 220 mW at 70°C free-air temperature at the rate of 1.8 mW/deg.

†Patented by Texas Instruments





# TYPE SN7231L

## GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS§	MIN	TYP	MAX	UNIT
V <sub>DI</sub> Differential-input offset voltage			4	15	mV
α <sub>VDI</sub> Differential-input offset voltage temperature coefficient	T <sub>A(1)</sub> = 70°C, T <sub>A(2)</sub> = 0°C		10		μV/deg
V <sub>CMO</sub> Common-mode output offset voltage			600		mV
I <sub>in</sub> Input current			6.5		μA
I <sub>DI</sub> Differential-input offset current			1	4	μA
V <sub>OM</sub> Maximum peak-to-peak output voltage	Differential output, f = 1 kHz		20		V
	Differential output, f = 1 kHz, T <sub>A</sub> = 0°C to 70°C	15			V
V <sub>CMIM</sub> Maximum common-mode input voltage			±5		V
A <sub>VD</sub> Differential voltage gain	R <sub>S</sub> = 50 Ω, f = 1 kHz		3000		
	R <sub>S</sub> = 50 Ω, f = 1 kHz, T <sub>A</sub> = 0°C to 70°C	1250			
CMRR Common-mode rejection ratio	R <sub>S</sub> = 50 Ω, f = 1 kHz		80		dB
BW Bandwidth (-3 dB)		60	150		kHz
Z <sub>in</sub> Input impedance	f = 1 kHz	4	1		kΩ
Z <sub>out</sub> Output impedance	f = 1 kHz		250		Ω
P <sub>T</sub> Total power dissipation			100		mW

§Unless otherwise noted, test conditions are: V<sub>CC1</sub> = +12 V, V<sub>CC2</sub> = -12 V, V<sub>DI</sub> applied, no external loading and pin ⑥ grounded.

### letter symbol and parameter definitions

- V<sub>DI</sub> That d-c voltage which must be applied between the input terminals to obtain zero-differential-output voltage. The application of this voltage balances the amplifier.
- α<sub>VDI</sub> Temperature coefficient averaged over the specified temperature range and defined by the equation:
- $$\alpha_{VDI} = \frac{(V_{DI} @ T_{A(1)}) - (V_{DI} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}}$$
- V<sub>CMO</sub> That d-c voltage level which exists between either output terminal and ground when the outputs are balanced.
- I<sub>in</sub> The current into either input of the amplifier.
- I<sub>DI</sub> The difference in the currents into the two input terminals when the output is balanced.
- V<sub>OM</sub> The maximum peak-to-peak output voltage swing that can be obtained without clipping when the output is balanced.
- V<sub>CMIM</sub> The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.
- CMRR The ratio of the differential-mode voltage gain to the common-mode voltage gain.
- BW The range of frequencies within which the open-loop voltage gain is within 3 dB of the mid-frequency value.
- Z<sub>in</sub> The impedance between either input terminal and ground with the other input terminal a-c grounded and the output balanced.
- Z<sub>out</sub> The impedance between either output terminal and ground when the output is balanced.

# TYPE SN7231L GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

## TYPICAL CHARACTERISTICS §

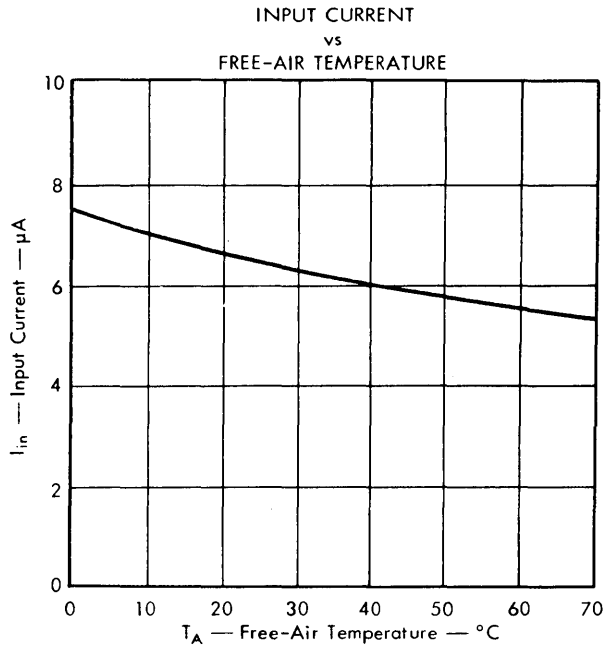


FIGURE 1

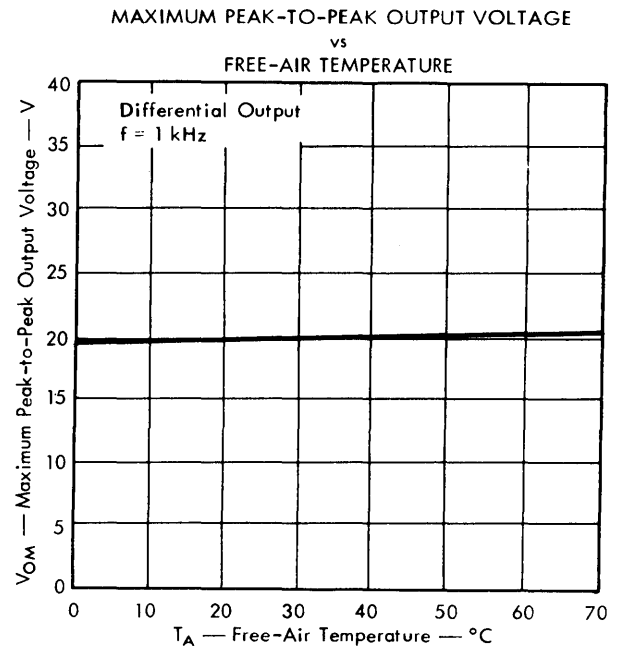


FIGURE 2

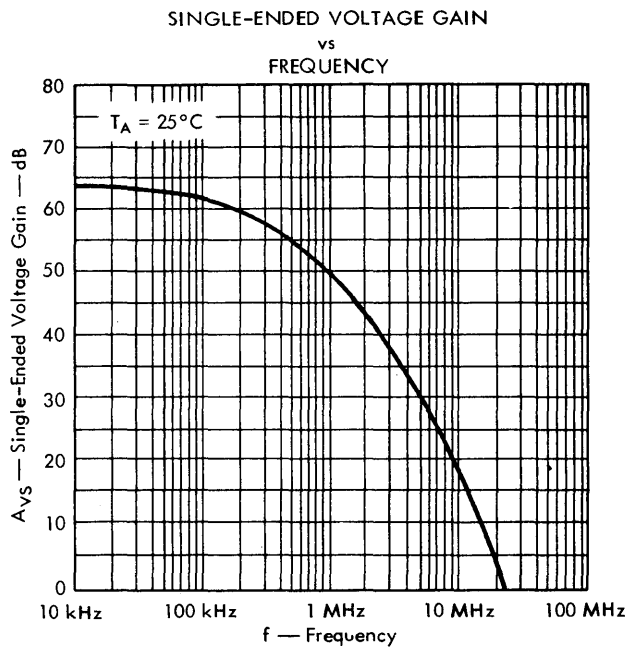


FIGURE 3

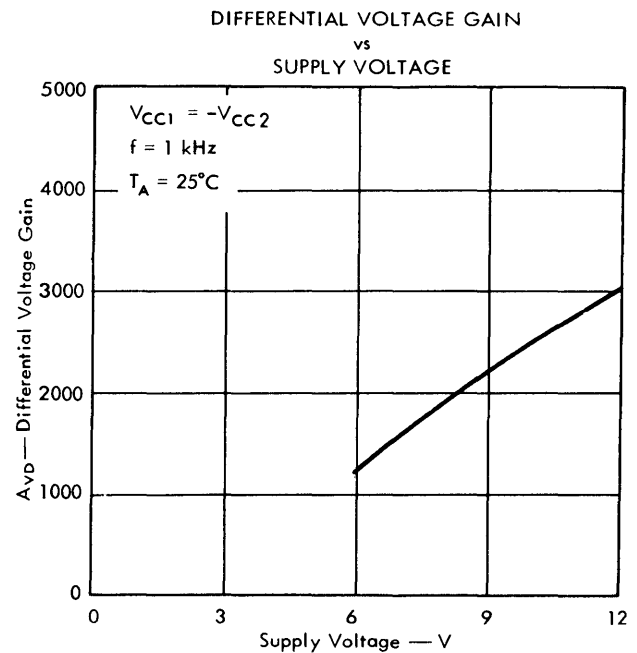


FIGURE 4

§Unless otherwise noted, test conditions are:  $V_{CC1} = +12\text{ V}$ ,  $V_{CC2} = -12\text{ V}$ ,  $V_{DI}$  applied, no external loading and pin 6 grounded.

# TYPE SN7231L

## GENERAL-PURPOSE DIFFERENTIAL AMPLIFIER

### TYPICAL CHARACTERISTICS §

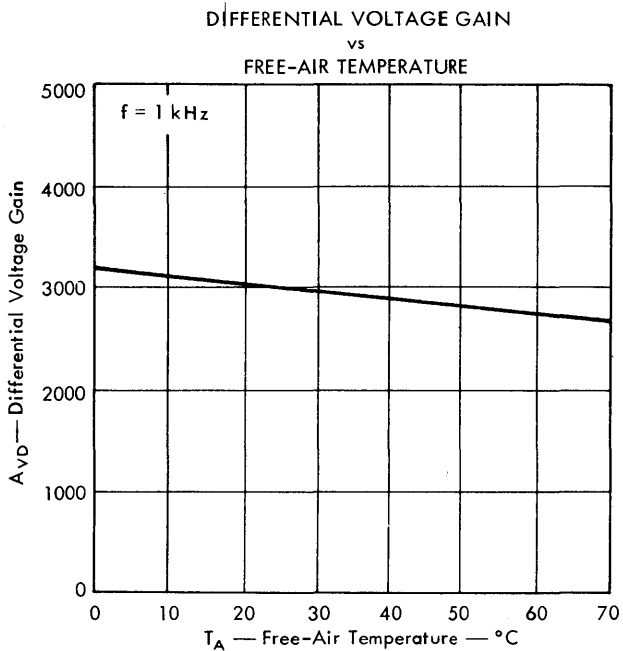


FIGURE 5

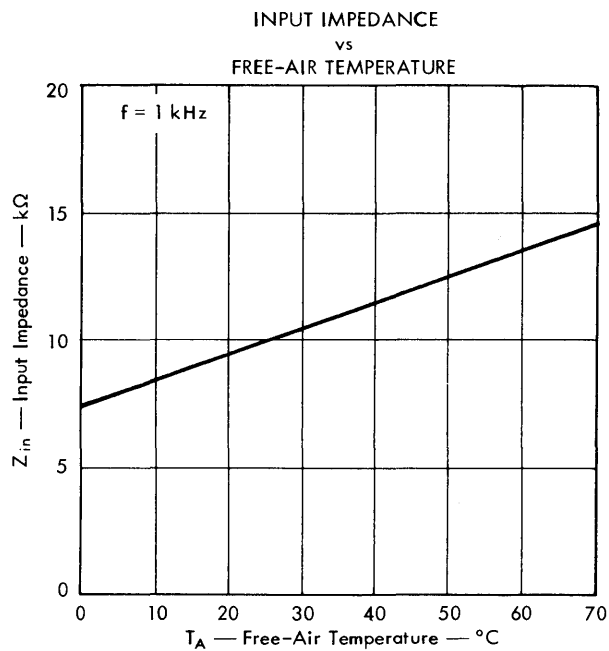


FIGURE 6

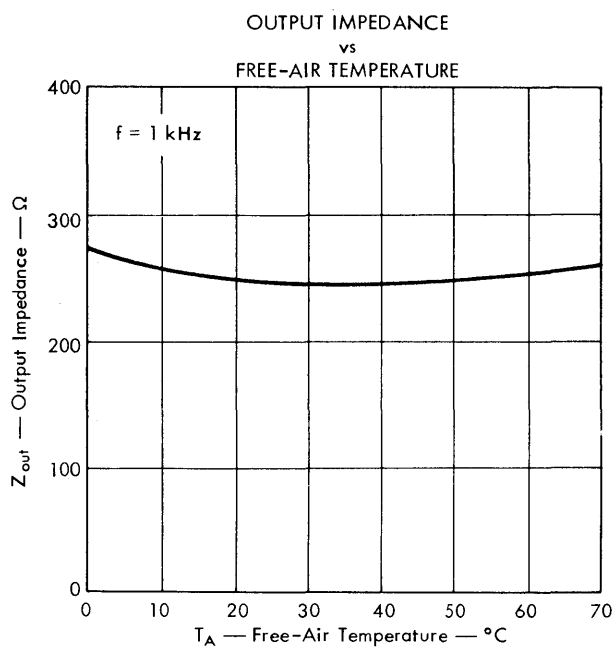


FIGURE 7

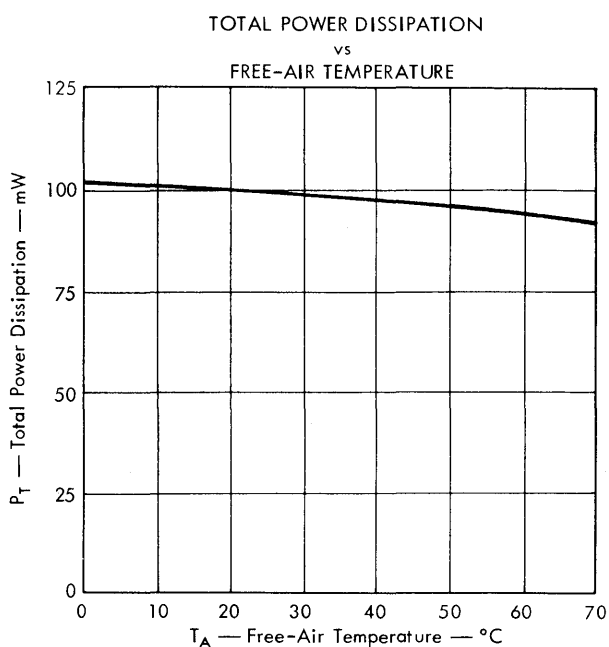


FIGURE 8

§Unless otherwise noted, test conditions are: V<sub>CC1</sub> = +12 V, V<sub>CC2</sub> = -12 V, V<sub>D1</sub> applied, no external loading and pin ④ grounded.

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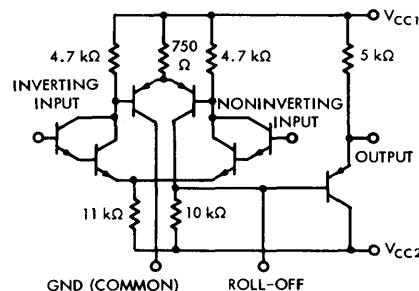
**SERIES 72 SEMICONDUCTOR-NETWORK GENERAL-PURPOSE AMPLIFIERS**  
for application as

- Buffer Amplifier
- Differentiator
- Integrator
- Multivibrator
- Level Detector
- Summing Amplifier

**description**

Each of these networks is a general-purpose operational amplifier consisting of two differential-gain stages and a single-ended emitter-follower output. The input stage utilizes Darlington-connected n-p-n transistors for high input impedance.

The SN724 and SN724L, two of Texas Instruments Series 72 catalog line of linear integrated circuits, offers higher reliability, lower cost, smaller size, and lower weight than equivalent discrete component circuits. Each Series 72 device is a monolithic semiconductor structure comprising diffused resistors and both n-p-n and p-n-p transistors.



NOTE: Component values shown are nominal.

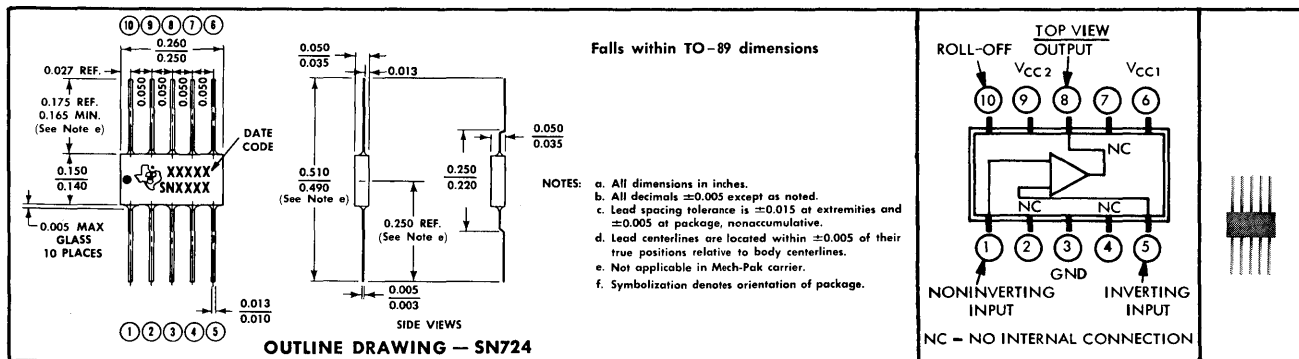
**SCHEMATIC DIAGRAM**

**mechanical data**

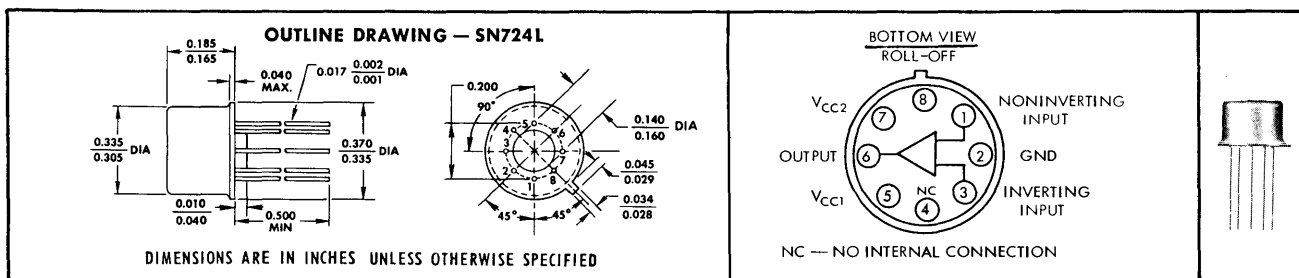
The SN724 operational amplifier is mounted in a glass-to-metal hermetically sealed welded package meeting TO-89. Leads are gold-plated F-15<sup>‡</sup> glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. The SN724 is available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier. See Ordering Instructions.

**SN724 ORDERING INSTRUCTIONS**

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5



The SN724L package outline is same as JEDEC TO-76 except for case height.



<sup>†</sup>Patented by Texas Instruments.

<sup>‡</sup>F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

TYPES SN724, SN724L  
BULLETIN NO. DL-S 668376, MARCH 1966



# TYPES SN724, SN724L

## GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltages (See Note 1): $V_{CC1}$	+ 15 V
$V_{CC2}$	-15 V
Differential Input Voltage	12 V
Common-Mode Input Voltage	$\pm 10$ V
Operating Free-Air Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground.

### electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>§</sup>	MIN	TYP	MAX	UNIT
$V_{DI}$ Differential-input offset voltage			15		mV
	$T_A = 0^\circ\text{C to } 70^\circ\text{C}$			40	mV
$\alpha_{VDI}$ Differential-input offset voltage temperature coefficient	$T_A = 0^\circ\text{C to } 70^\circ\text{C}$		30		$\mu\text{V/deg}$
$I_{in}$ Input Current			110	500	nA
$I_{DI}$ Differential-input offset current			44		nA
	$T_A = 0^\circ\text{C}$		18		nA
	$T_A = 70^\circ\text{C}$		70		nA
$V_{OM}$ Maximum peak-to-peak output voltage	$f = 1 \text{ kc/s, } T_A = 0^\circ\text{C to } 70^\circ\text{C}$	8			V
	$f = 1 \text{ kc/s}$		12		V
	10 k $\Omega$ load, $f = 1 \text{ kc/s, } T_A = 0^\circ\text{C to } 70^\circ\text{C}$	6			V
	10 k $\Omega$ load, $f = 1 \text{ kc/s}$		11		V
$V_{CMIM}$ Maximum common-mode input voltage			$\pm 5$		V
$A_V$ Voltage gain	$f = 1 \text{ kc/s, } T_A = 0^\circ\text{C to } 70^\circ\text{C}$	400			
	$f = 1 \text{ kc/s}$		1200		
CMRR Common-mode rejection ratio	$f = 1 \text{ kc/s, } T_A = 0^\circ\text{C to } 70^\circ\text{C}$		55		dB
BW Bandwidth (-3 dB)		60	140		kc/s
$Z_{in}$ Input impedance	$f = 1 \text{ kc/s}$	250	800		k $\Omega$
$Z_{out}$ Output impedance	$f = 1 \text{ kc/s}$		300		$\Omega$
$P_T$ Total power dissipation	No input signal, no external load		120		mW

<sup>§</sup>Unless otherwise noted test conditions are:  $V_{CC1} = +12 \text{ V}$ ,  $V_{CC2} = -12 \text{ V}$ , ground and  $V_{DI}$  applied; roll-off terminal open, no external loading. The unused input is grounded for all tests except when common-mode characteristics are under test.

### letter symbol and parameter definitions

$V_{DI}$	That d-c voltage which must be applied between the input terminals to obtain zero-output voltage referenced to ground. The application of this voltage balances the amplifier.
$I_{in}$	The current into either input of the amplifier.
$I_{DI}$	The difference in the currents into the two input terminals when the output is balanced.
$V_{OM}$	The maximum peak-to-peak output voltage swing that can be obtained without clipping when the output is balanced.
$V_{CMIM}$	The maximum common-mode voltage that can be impressed on the input terminals while maintaining differential operation.
CMRR	The ratio of the differential-mode voltage gain to the common-mode voltage gain.
BW	The range of frequencies within which the voltage gain is within 3 dB of the mid-frequency value.
$Z_{in}$	The impedance between either input terminal and ground with the other input terminal a-c grounded and the output balanced.
$Z_{out}$	The impedance between the output terminal and ground when the output is balanced.

# TYPES SN724, SN724L GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

## TYPICAL CHARACTERISTICS§

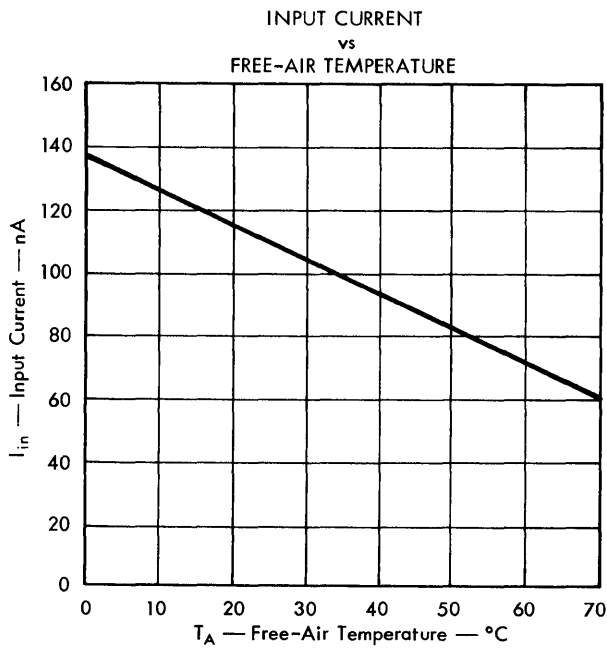


FIGURE 1

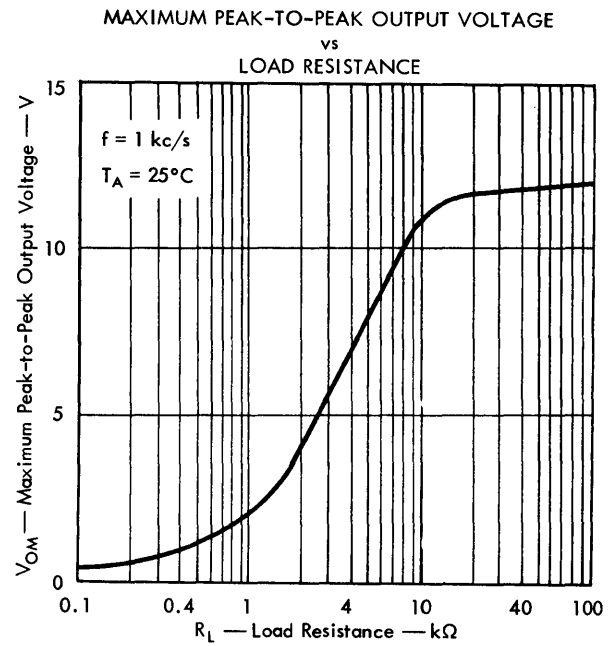


FIGURE 2

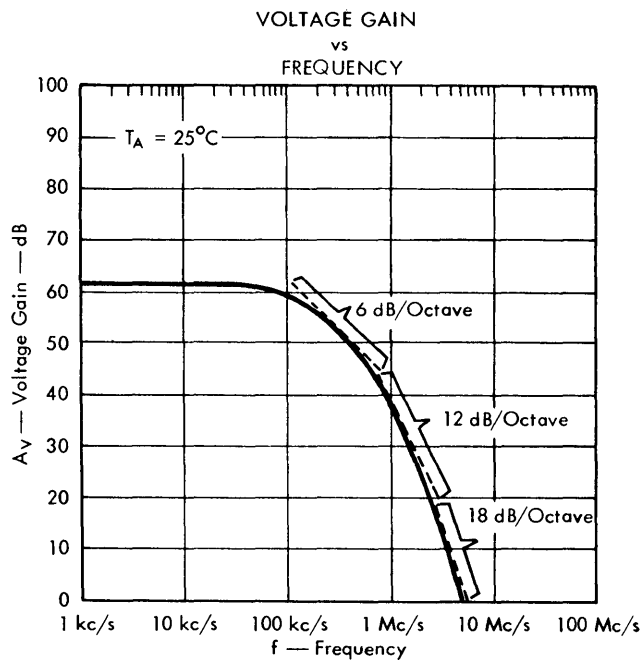


FIGURE 3

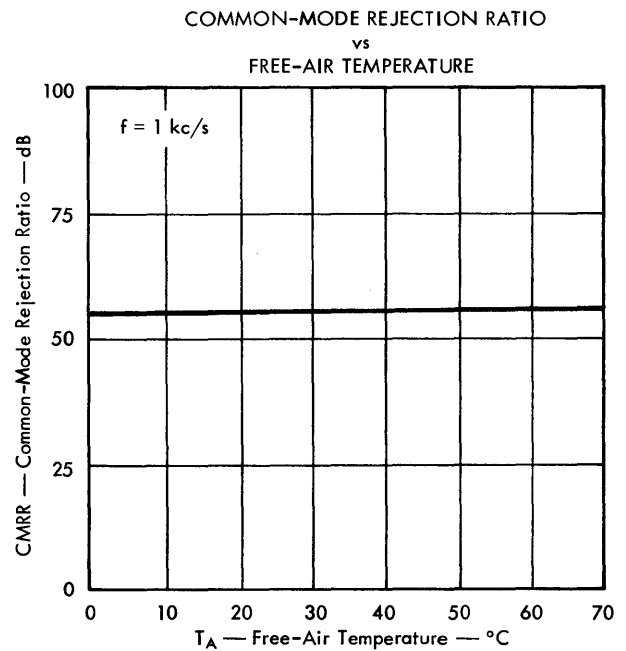


FIGURE 4

§ Unless otherwise noted test conditions are:  $V_{CC1} = +12$  V,  $V_{CC2} = -12$  V, ground and  $V_{DI}$  applied; roll-off terminal open, no external loading. The unused input is grounded for all tests except when common-mode characteristics are under test.

# TYPES SN724, SN724L GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

## TYPICAL CHARACTERISTICS§

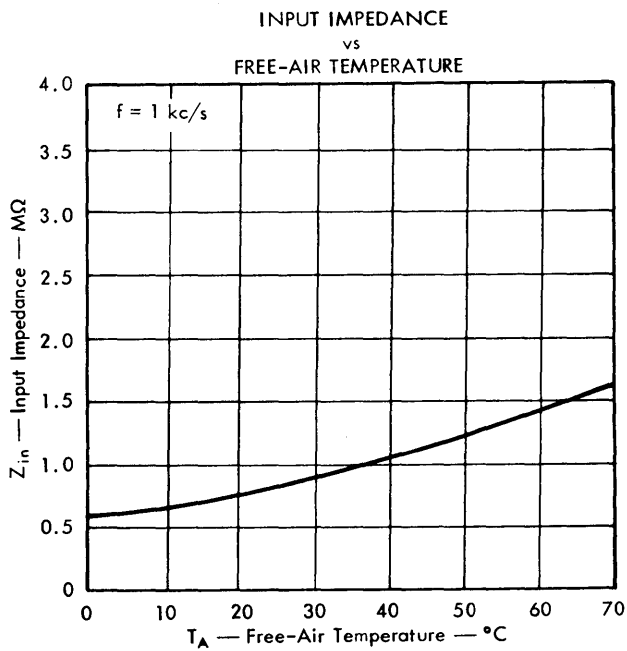


FIGURE 5

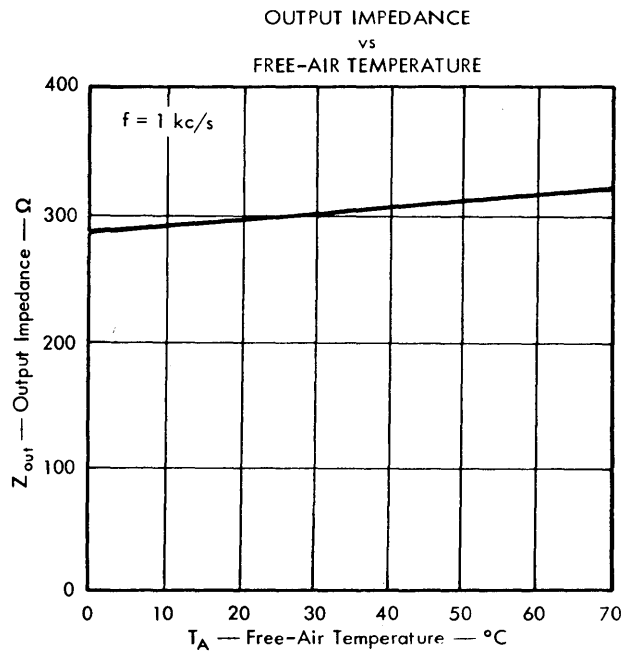


FIGURE 6

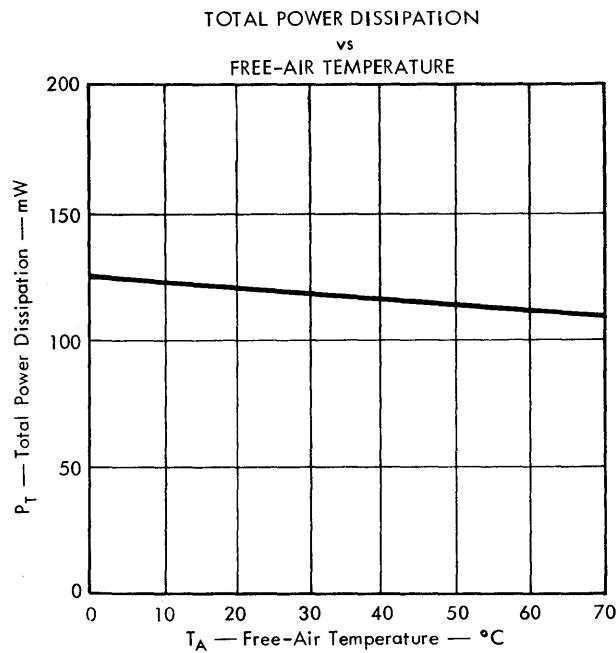


FIGURE 7

§Unless otherwise noted test conditions are:  $V_{CC1} = +12\text{ V}$ ,  $V_{CC2} = -12\text{ V}$ , ground and  $V_{DI}$  applied; roll-off terminal open, no external loading. The unused input is grounded for all tests except when common-mode characteristics are under test.

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**SERIES 75 HIGH-SPEED SENSE AMPLIFIERS  
 FOR CONVERSION OF  
 COINCIDENT-CURRENT MEMORY READ-OUT TO SATURATED-DIGITAL LOGIC LEVELS**

**application**

The SN7500, SN7501, and SN7502 are designed to detect bipolar magnetic-core-memory signals and convert them to logic levels compatible with standard diode-transistor logic (DTL) or transistor-transistor logic (TTL). Definitive specifications are provided for operating characteristics over the temperature range of 0°C to 70°C.

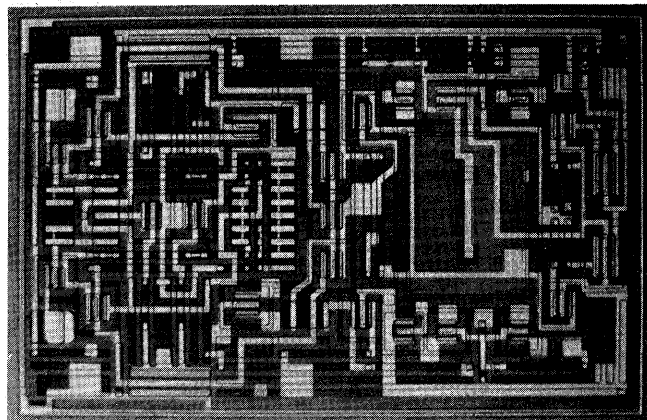
**features**

**PERFORMANCE**

- perform both time and amplitude signal discrimination
- adjustable input-threshold voltage level
- extremely narrow region of threshold voltage uncertainty
- good fan-out capability
- typical differential input to logic-output propagation delay time of 50 ns
- fast overload recovery time

**EASE OF DESIGN**

- choice of output circuit function
- TTL or DTL drive capability
- standard logic supply voltages



**TYPE SN7500 CIRCUIT BAR**

**description**

The SN7500 and SN7502 are sense amplifiers with one-shot-output circuits. The SN7500 features a double-ended output with high fan-out capability. The SN7502 features a variable-threshold differential-input circuit, externally controlled output pulse width, and a single-ended output capable of performing dot-OR logic.

The SN7501 is a sense amplifier with flip-flop output circuit. It also features a variable-threshold differential-input circuit. Functions of the internal R-S flip-flop include direct reset and complementary outputs.

All three networks incorporate a strobe input so that threshold detection will occur when the signal-to-noise ratio is at a maximum.

	CONTENTS	Page
DESIGN CHARACTERISTICS . . . . .		8502-8503
DEFINITIVE SPECIFICATIONS:		
TYPE SN7500 (ONE-SHOT OUTPUT) . . . . .		8504-8505
TYPE SN7501 (FLIP-FLOP OUTPUT) . . . . .		8506-8507
TYPE SN7502 (ONE-SHOT OUTPUT) . . . . .		8508-8509
D-C TEST CIRCUITS . . . . .		8510-8511
SWITCHING TIME CIRCUITS AND VOLTAGE WAVEFORMS . . . . .		8512-8513
TYPICAL APPLICATIONS . . . . .		8514-8515
TYPICAL CHARACTERISTICS . . . . .		8515
MECHANICAL DATA . . . . .		8516

†Patented by Texas Instruments





# TYPES SN7500, SN7501, SN7502

## SENSE AMPLIFIERS WITH DIGITAL-LEVEL OUTPUTS

### design characteristics

Series 75 sense amplifiers have been designed for use with coincident-current memory systems. The sense amplifiers detect bipolar differential-input signals from the memory and provide the interface circuitry between the memory and the logic section. The low-level pulses originating in the memory are transformed into logic levels compatible with the logic section.

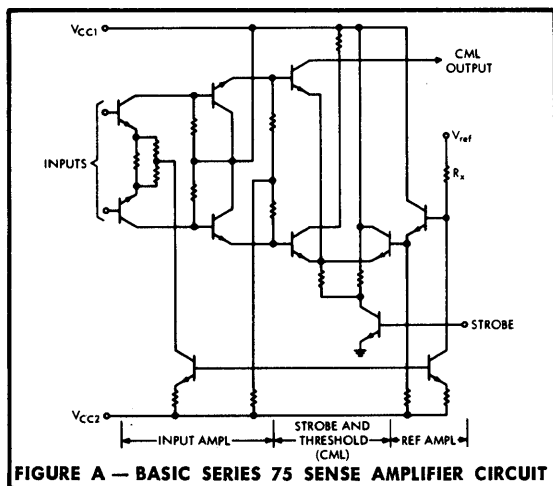
A distinct feature of these amplifiers is the extremely narrow region of uncertainty of the threshold circuit. This is accomplished by the high over-all gain coupled with a regenerative output stage. The threshold level of the design is well-defined and any change in this level due to temperature or external reference control can be readily predicted.

A strobe or enable gate is included in the design so the threshold detector can be enabled when the signal-to-noise ratio is a maximum during the system read cycle and inhibited during the write cycle.

The output circuits are designed to be compatible with the available DTL and TTL integrated logic circuits and are characterized for operation with these devices.

### circuit operation

The basic Series 75 sense amplifier circuit is shown in figure A.



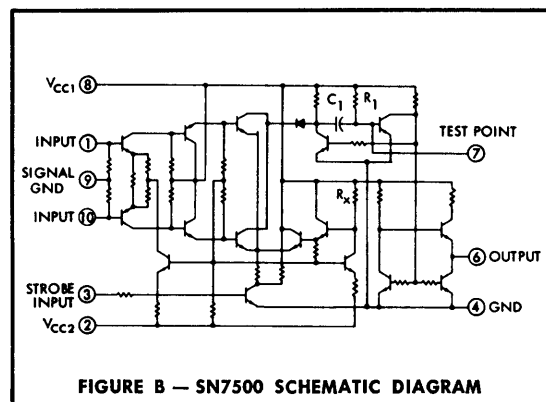
The differential-amplifier outputs are used as inputs for a current-mode-logic (CML) circuit. The reference voltage for the CML circuit is determined by the reference amplifier which is common-mode coupled to the input amplifier through the current sources. This common-mode loop stabilizes the reference-amplifier output voltage with respect to the input-amplifier output voltage. The design voltage levels are such that the reference voltage is positive with respect to the amplifier output voltage levels by an amount directly related to the threshold voltage. The result is that the CML output voltage is high if no differential-input voltage is present. A differential-input voltage large enough in amplitude to swing one amplifier output voltage more positive than the reference voltage will switch the CML circuit, thus causing a negative voltage transient at the CML output. The strobe transistor enables or inhibits action of the CML circuit.

### input threshold voltage

Since the input threshold voltage is related to the reference-amplifier output voltage, the threshold voltage, developed across resistor  $R_x$  (figures A and B) in the SN7500, can be made externally adjustable by providing a method to vary the reference-amplifier input voltage. The reference input terminal ( $V_{ref}$ ) is provided on the SN7501 and SN7502 to allow external generation of the reference voltage.

### SN7500

The SN7500 sense amplifier with one-shot output requires no external components for operation in a conventional 2- $\mu$ s memory. The circuit is shown in figure B.



The SN7500 incorporates a one-shot to provide regeneration and to extend the output pulse width. The pulse width is established internally by the time constant of the  $R_1C_1$  combination. To minimize the external circuitry, sense-line terminations to a signal ground are included in the design. Since these resistors are fabricated using standard diffusion processes, they will exhibit a temperature coefficient of approximately  $\pm 0.2$  percent per centigrade degree. Match of the two termination resistors is nominally 2 percent.

The threshold voltage of the SN7500 is nominally 17 mV, a value chosen to be compatible with most coincident-current memories in the 2- $\mu$ s range. The threshold reference voltage ( $V_{ref}$ ) is generated internally to eliminate the need for external components.

The output is an inverting, double-ended (totem-pole) circuit providing capability for sinking load current or supplying source current. This output will drive high-capacitance loads with good rise and fall times with little degradation in output waveform.

### SN7502

The SN7502 is very similar to the SN7500 in function and design, except that external components are utilized to increase the flexibility of the circuit. Figure C shows the circuitry for the SN7502.

# TYPES SN7500, SN7501, SN7502 SENSE AMPLIFIERS WITH DIGITAL-LEVEL OUTPUTS

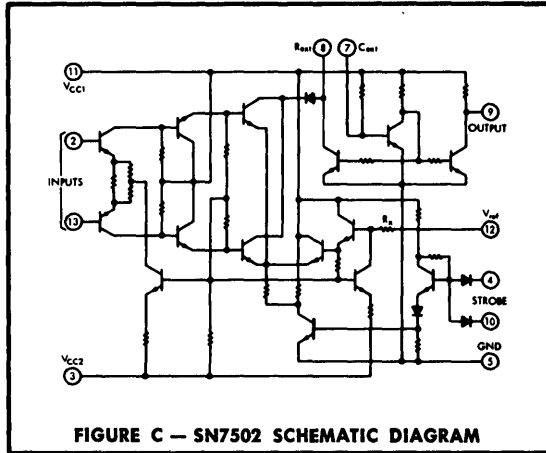


FIGURE C — SN7502 SCHEMATIC DIAGRAM

Unlike the SN7500, the output-pulse width of the SN7502 can be varied by  $C_{ext}$  and the input-threshold-voltage level can be adjusted by  $V_{ref}$ . Dual DTL strobe inputs increase strobing flexibility and an inverting, single-ended output stage is used to provide a wired-OR output capability. The SN7502, when connected to operate with minimum output pulse width, can be used in the 1- $\mu$ s memory range.

## SN7501

The SN7501 sense amplifier offers maximum flexibility. The device includes a flip-flop with a direct reset capability and complementary outputs. The flip-flop is "set" by a differential input greater than the input-threshold-voltage level which may be adjusted by the external  $V_{ref}$  supply. Figure D shows the circuit for the SN7501. The flip-flop output circuit can be used as a temporary data storage element.

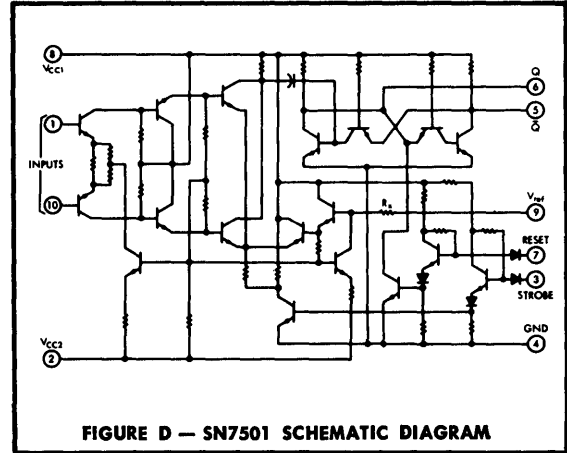


FIGURE D — SN7501 SCHEMATIC DIAGRAM

Both the stored information and its complement appear in the flip-flop after reading from the memory and are available as inputs to the logic section.

### output drive capability

The output circuits for the SN7500, SN7501, and SN7502 feature the ability to both sink or supply load current. This capability permits direct use with both DTL- and TTL-type loads.

### input current requirements

Input current requirements reflect worst-case conditions for  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  and  $V_{CC1} = +5\text{ V}$ ,  $V_{CC2} = -5\text{ V}$ , and  $V_{in}$  as indicated in the table.

#### INPUT CURRENT REQUIREMENTS

TYPE	INPUT	$V_{in}$	$I_{in}$ (MAX)
SN7500	Strobe	2.6 V	2.5 mA
SN7501	Strobe or Reset	5 V	5 $\mu$ A
		0 V	-1.6 mA
SN7502	Strobe	5 V	5 $\mu$ A
		0 V	-1.6 mA

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

#### Supply Voltages:

$V_{CC1}$	.....	+7 V
$V_{CC2}$	.....	-7 V
$V_{ref}$	.....	+7 V

Strobe and Reset Input Voltages . . . . . +6 V

Operating Free-Air Temperature Range . . . . .  $0^\circ\text{C}$  to  $70^\circ\text{C}$

Storage Temperature Range . . . . .  $-65^\circ\text{C}$  to  $150^\circ\text{C}$

NOTE: Voltage values are with respect to network ground terminal.

### logic definition

Standard POSITIVE LOGIC with the following definitions is used for specifying digital-level signals:

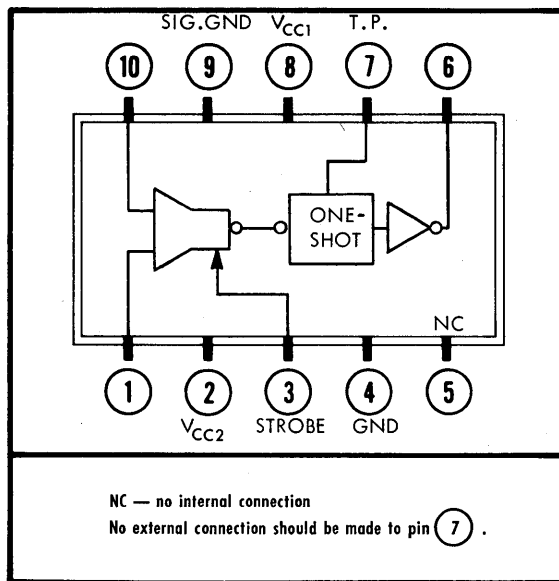
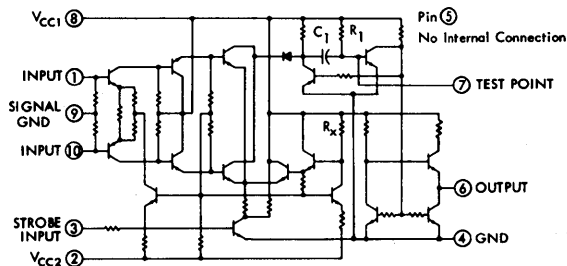
LOW VOLTAGE = LOGICAL 0

HIGH VOLTAGE = LOGICAL 1

# TYPE SN7500

## SENSE AMPLIFIER WITH ONE-SHOT OUTPUT

### schematic



### recommended operating conditions

Supply Voltages:	$V_{CC1}$	.....	+5 V
	$V_{CC2}$	.....	-5 V
Strobe Input Voltages:	Logical 0 Level	.....	0 to +0.5 V
	Logical 1 Level	.....	+2 V to +5 V

### electrical characteristics (unless otherwise noted, $V_{CC1} = +5 V$ , $V_{CC2} = -5 V$ , $T_A = 0^\circ C$ to $70^\circ C$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$V_T$ Differential-input threshold voltage (see note 1)	1		10		30	mV
		$T_A = 25^\circ C$	10	17	30	mV
$V_{CMF}$ Common-mode-input firing voltage (see note 2)		$T_A = 25^\circ C$ Strobe Input: $V_{inS} = 2.6 V$ Common-Mode Input Pulse: $t_r = t_f = 50 ns$ , $t_{p(in)} = 150 ns$		2		V
$V_{out(1)}$ Logical 1 output voltage	2	$I_{load} = -8 mA$	2.6			V
$V_{out(0)}$ Logical 0 output voltage	3	$I_{sink} = 8 mA$			0.4	V
$I_{in(1)S}$ Logical 1 level strobe-input current	4	$V_{inS} = 2.6 V$		1.2	2.5	mA
$r_{inD}$ Differential-input d-c resistance	6	Supply voltages are not applied	150	200	300	$\Omega$
$I_{CC1}$ $V_{CC1}$ supply current	7			15		mA
$I_{CC2}$ $V_{CC2}$ supply current	7			-10		mA

†Signal-ground terminal is open.

NOTES: 1. The differential-input threshold voltage ( $V_T$ ) is defined as that pulse or d-c input voltage ( $V_{in}$ ) just sufficient to cause the output to switch. For testing and correlation purposes a d-c input voltage is desirable.

2. Common-mode-input firing voltage is the common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the output to switch. The specified common-mode-input signal is applied with a strobe-enable signal present.

# TYPE SN7500

## SENSE AMPLIFIER WITH ONE-SHOT OUTPUT

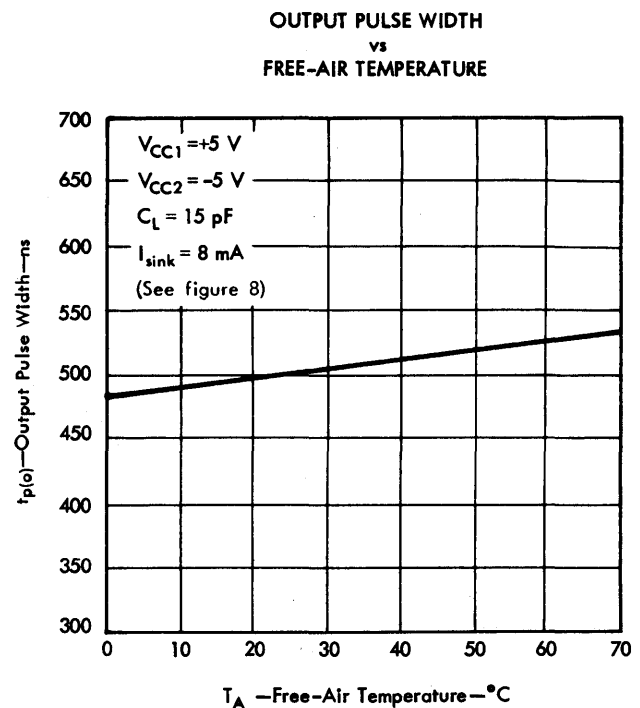
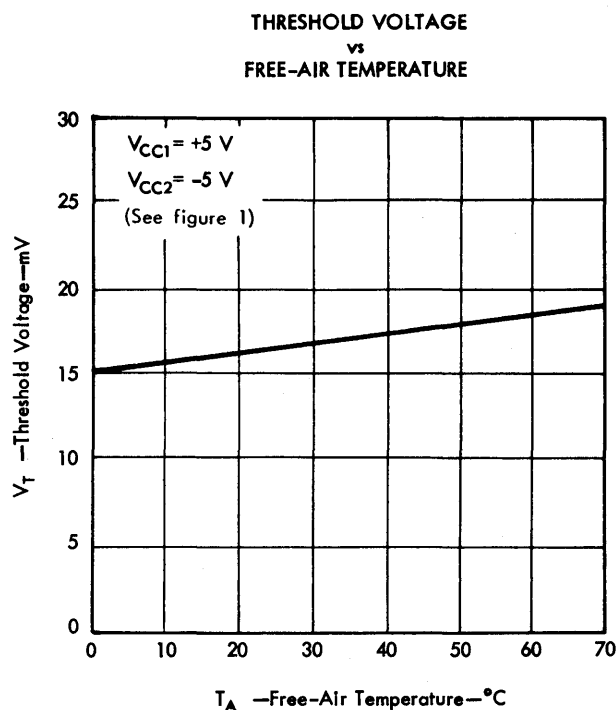
switching characteristics,  $V_{CC1} = +5\text{ V}$ ,  $V_{CC2} = -5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$t_{pd(0)D}$ Propagation delay time to logical 0 level (differential input-to-output)	8	$V_{inD} = 50\text{ mV}$ , $C_L = 15\text{ pF}$ , $I_{sink} = 8\text{ mA}$		50	125	ns
$t_{pd(0)S}$ Propagation delay time to logical 0 level (strobe input-to-output)	9	$V_{inD} = 50\text{ mV}$ , $C_L = 15\text{ pF}$ , $I_{sink} = 8\text{ mA}$		45	100	ns
$t_{p(0)}$ Logical 0 output pulse width	8	$V_{inD} = 50\text{ mV}$ , $C_L = 15\text{ pF}$ , $I_{sink} = 8\text{ mA}$	200	500	800	ns
$t_{orD}$ Differential-input overload recovery time (see note 1)		<i>Differential Input Pulse:</i> $V_{inD} = 2\text{ V}$ , $t_r = t_f = 20\text{ ns}$		20		ns
$t_{orCM}$ Common-mode-input overload recovery time (see note 2)		<i>Common-Mode Input Pulse:</i> $V_{inCM} = \pm 2\text{ V}$ , $t_r = t_f = 20\text{ ns}$		20		ns
$t_{cyc(min)}$ Minimum cycle time		$t_{pS} = 100\text{ ns}$		1.5		$\mu\text{s}$

†Signal-ground terminal is open

- NOTES: 1. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input overload signal prior to the strobe-enable signal.  
2. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

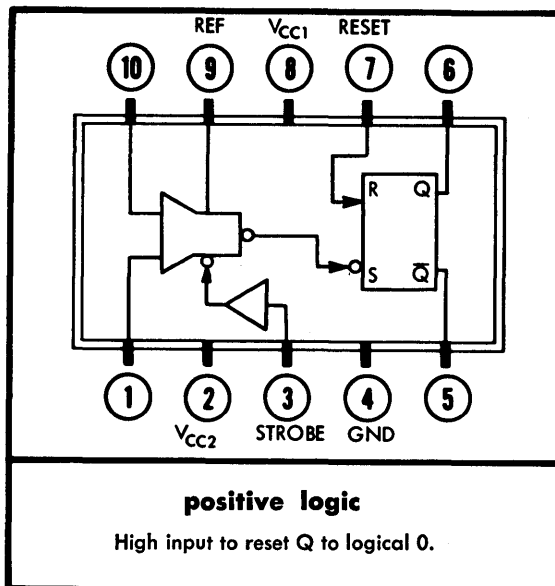
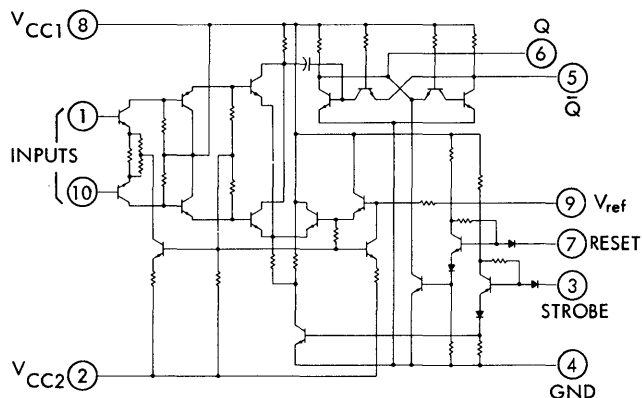
### TYPICAL CHARACTERISTICS



# TYPE SN7501

## SENSE AMPLIFIER WITH FLIP-FLOP OUTPUT

### schematic



### recommended operating conditions

Supply Voltages:	$V_{CC1}$	.....	+5 V
	$V_{CC2}$	.....	-5 V
	$V_{ref}$	.....	+3.8 V to +5 V
Strobe and Reset Input Voltages:	Logical 0 Level	.....	0 to +0.8 V
	Logical 1 Level	.....	+2 V to +5 V

### electrical characteristics, $V_{CC1} = +5 V$ , $V_{CC2} = -5 V$ (unless otherwise noted, $T_A = 0^\circ C$ to $70^\circ C$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$V_T$ Differential-input threshold voltage (see note 1)	1	$T_A = 0^\circ C$	12	20		mV
		$T_A = 25^\circ C$	14	20		mV
		$T_A = 70^\circ C$	14	24		mV
$V_{CMF}$ Common-mode input firing voltage (see note 2)		$T_A = 25^\circ C$ Strobe Input: $V_{ins} = 2.6 V$ Common-Mode-Input Pulse: $t_r = t_f = 50 ns$ , $t_p = 150 ns$		2		V
$V_{out(1)}$ Logical 1 output voltage	2	$I_{load} = -1 mA$	2.6			V
$V_{out(0)}$ Logical 0 output voltage	3	$I_{sink} = 4 mA$			0.4	V
$I_{in(1)}$ Logical 1 level strobe or reset input current	4	$V_{in} = 5 V$			5	$\mu A$
$I_{in(0)}$ Logical 0 level strobe or reset input current	5	$V_{in} = 0$			-1.6	mA
$Z_{inD}$ Differential-input impedance (see note 3)		$f = 1 kHz$		5		k $\Omega$
$I_{CC1}$ $V_{CC1}$ supply current	7			18		mA
$I_{CC2}$ $V_{CC2}$ supply current	7			-10		mA
$I_{ref}$ $V_{ref}$ supply current	7			2.5	3	mA

† $V_{ref} = +4 V$

- NOTES: 1. The differential-input threshold voltage ( $V_T$ ) is defined as that pulse or d-c input voltage ( $V_{in}$ ) just sufficient to cause the output to switch. For testing and correlation purposes a d-c input voltage is desirable.
2. Common-mode-input firing voltage is the common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the output to switch. The specified common-mode-input signal is applied with a strobe-enable signal present.
3. The differential-input impedance parameter is shown for reference only. This input impedance will not appreciably shunt a low impedance sense-line termination.

# TYPE SN7501

## SENSE AMPLIFIER WITH FLIP-FLOP OUTPUT

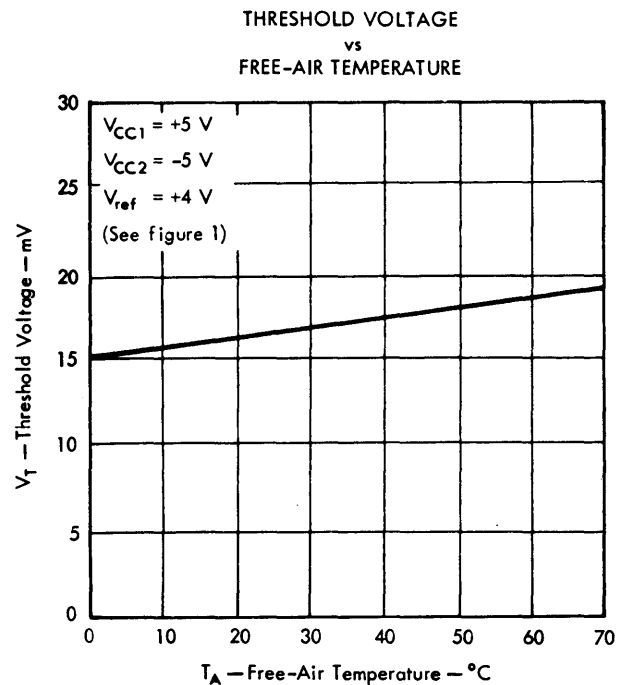
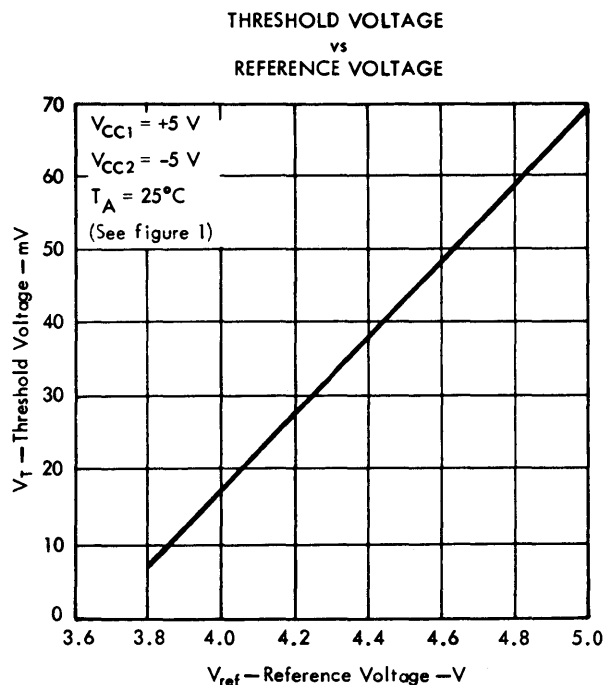
switching characteristics,  $V_{CC1} = +5\text{ V}$ ,  $V_{CC2} = -5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$t_{pd(1)D}$ Propagation delay time to logical 1 level (differential input to output)	8	$V_{inD} = 30\text{ mV}$ , $C_L = 15\text{ pF}$ , $I_{load} \leq -10\text{ }\mu\text{A}$		45	75	ns
$t_{pd(0)D}$ Propagation delay time to logical 0 level (differential input to output)	8	$V_{inD} = 30\text{ mV}$ , $C_L = 15\text{ pF}$ , $I_{sink} = 4\text{ mA}$		45	75	ns
$t_{pd(1)R}$ Propagation delay time to logical 1 level (reset input to output)	8	$V_{inD} = 30\text{ mV}$ , $C_L = 15\text{ pF}$ , $I_{load} \leq -10\text{ }\mu\text{A}$		20	75	ns
$t_{pd(0)R}$ Propagation delay time to logical 0 level (reset input to output)	8	$V_{inD} = 30\text{ mV}$ , $C_L = 15\text{ pF}$ , $I_{sink} = 4\text{ mA}$		20	75	ns
$t_{pd(1)S}$ Propagation delay time to logical 1 level (strobe input to output)	9	$V_{inD} = 30\text{ mV}$ , $C_L = 15\text{ pF}$ , $I_{load} \leq -10\text{ }\mu\text{A}$		45	75	ns
$t_{pd(0)S}$ Propagation delay time to logical 0 level (strobe input to output)	9	$V_{inD} = 30\text{ mV}$ , $C_L = 15\text{ pF}$ , $I_{sink} = 4\text{ mA}$		45	75	ns
$t_{orD}$ Differential-input overload recovery time (see note 1)		<i>Differential Input Pulse:</i> $V_{inD} = 2\text{ V}$ , $t_r = t_f = 20\text{ ns}$		20		ns
$t_{orCM}$ Common-mode input overload recovery time (see note 2)		<i>Common-Mode Input Pulse:</i> $V_{inCM} = \pm 2\text{ V}$ , $t_r = t_f = 20\text{ ns}$		20		ns
$t_{cyc(min)}$ Minimum cycle time		$t_{pS} = 100\text{ ns}$ , $t_{pR} = 100\text{ ns}$		0.7		$\mu\text{s}$

$$\dagger V_{ref} = +4\text{ V}$$

- NOTES: 1. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.  
2. Common-mode-input overload recovery time is the time necessary for the device to recover from the specified common-mode-input overload signal prior to the strobe-enable signal.

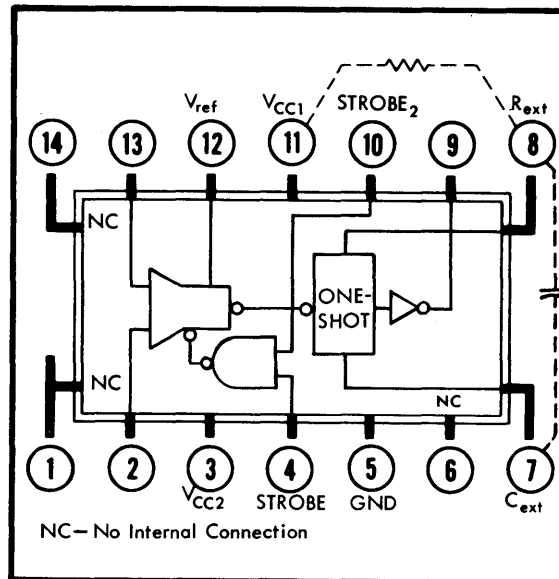
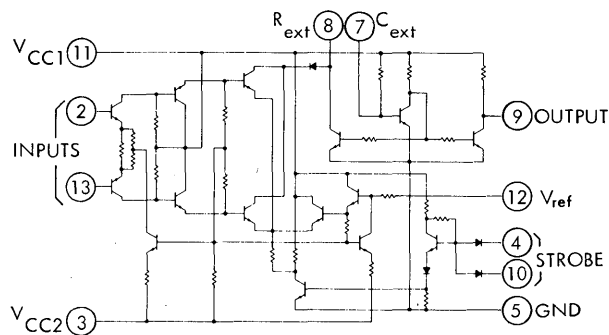
### TYPICAL CHARACTERISTICS



# TYPE SN7502

## SENSE AMPLIFIER WITH ONE-SHOT OUTPUT

### schematic



### recommended operating conditions

Supply Voltages:	$V_{CC1}$	.....	+5 V
	$V_{CC2}$	.....	-5 V
	$V_{ref}$	.....	+4.3 V to +5 V
Strobe Input Voltages:	Logical 0 Level	.....	0 to 0.8 V
	Logical 1 Level	.....	+2 V to +5 V
Value of External Resistor and Capacitor:	$R_{ext}$	.....	2 k $\Omega$ $\pm$ 5%
	$C_{ext}$	.....	47 pF minimum

### electrical characteristics, $V_{CC1} = +5 V$ , $V_{CC2} = -5 V$ (unless otherwise noted, $T_A = 0^\circ C$ to $70^\circ C$ )

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$V_T$ Differential-input threshold voltage (see note 1)	1	$C_{ext} = 47$ pF, $T_A = 0^\circ C$	14	24		mV
		$C_{ext} = 47$ pF, $T_A = 25^\circ C$	17	24		mV
		$C_{ext} = 47$ pF, $T_A = 70^\circ C$	17	27		mV
$V_{CMF}$ Common-mode input firing voltage (see note 2)		$C_{ext} = 47$ pF, $T_A = 25^\circ C$ Strobe Input: $V_{inS} = 2.6$ V Common-Mode Input Pulse: $t_r = t_f = 50$ ns, $t_p = 150$ ns		2.5		V
$V_{out(1)}$ Logical 1 output voltage	2	$I_{load} = -150$ $\mu A$	2.6			V
$V_{out(0)}$ Logical 0 output voltage	3	$I_{sink} = 15$ mA			0.4	V
$I_{in(1)}$ Logical 1 level strobe input current	4	$V_{in} = 5$ V			5	$\mu A$
$I_{in(0)}$ Logical 0 level strobe input current	5	$V_{inS} = 0$		-1.1	-1.6	mA
$z_{inD}$ Differential-input impedance (see note 3)		$f = 1$ kHz		5		k $\Omega$
$I_{CC1}$ $V_{CC1}$ supply current	7			15		mA
$I_{CC2}$ $V_{CC2}$ supply current	7			-8		mA
$I_{ref}$ $V_{ref}$ supply current	7			2.5	3	mA

†  $V_{ref} = +4.5$  V and  $R_{ext} = 2$  k $\Omega$

- NOTES: 1. The differential-input threshold voltage ( $V_T$ ) is defined as that pulse or d-c input voltage ( $V_{in}$ ) just sufficient to cause the output to switch. For testing and correlation purposes a d-c input voltage is desirable.
2. Common-mode-input firing voltage is the common-mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the output to switch. The specified common-mode-input signal is applied with a strobe-enable signal present.
3. The differential-input impedance parameter is shown for reference only. This input impedance will not appreciably shunt a low-impedance sense-line termination.

# TYPE SN7502

## SENSE AMPLIFIER WITH ONE-SHOT OUTPUT

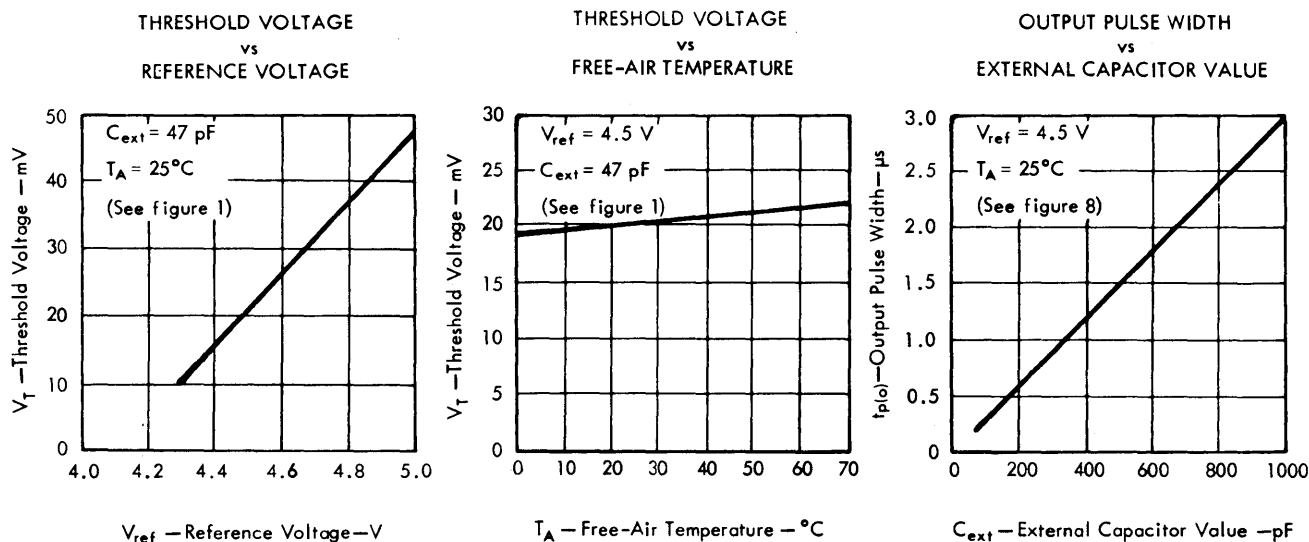
switching characteristics,  $V_{CC1} = +5\text{ V}$ ,  $V_{CC2} = -5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$t_{pd(0)D}$ Propagation delay time to logical 0 level (differential input-to-output)	8	$V_{inD} = 30\text{ mV}$ , $C_L = 15\text{ pF}$ , $I_{sink} = 15\text{ mA}$		60	100	ns
$t_{pd(0)S}$ Propagation delay time to logical 0 level (strobe input-to-output)	9	$V_{inD} = 30\text{ mV}$ , $C_L = 15\text{ pF}$ , $I_{sink} = 15\text{ mA}$		50	100	ns
$t_{p(0)}$ Logical 0 output pulse width	8	$V_{inD} = 30\text{ mV}$ , $I_{sink} = 15\text{ mA}$	150		300	ns
$t_{orD}$ Differential-input overload recovery time (see note 1)		Differential Input Pulse: $V_{inD} = 2\text{ V}$ , $t_r = t_f = 20\text{ ns}$		20		ns
$t_{orCM}$ Common-mode input overload recovery time (see note 2)		Common-Mode Input Pulse: $V_{inCM} = \pm 2\text{ V}$ , $t_r = t_f = 20\text{ ns}$		20		ns
$t_{cyc(min)}$ Minimum cycle time		$t_{ps} = 100\text{ ns}$		1.5		$\mu\text{s}$

† $V_{ref} = +4.5\text{ V}$ ,  $R_{ext} = 2\text{ k}\Omega$  and  $C_{ext} = 47\text{ pF}$

- NOTES: 1. Differential-input overload recovery time is the time necessary for the device to recover from the specified differential-input-overload signal prior to the strobe-enable signal.
2. Common-mode input overload recovery time is the time necessary for the device to recover from the specified common-mode-input-overload signal prior to the strobe-enable signal.

### TYPICAL CHARACTERISTICS§



§ $V_{CC1} = +5\text{ V}$ ,  $V_{CC2} = -5\text{ V}$ , and  $R_{ext} = 2\text{ k}\Omega$ .

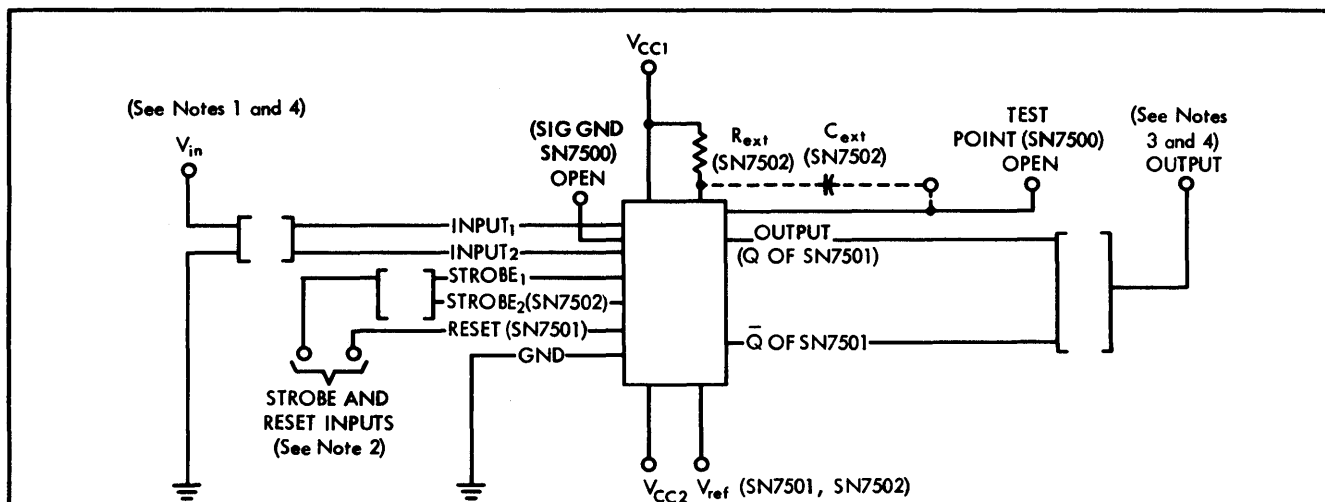


# TYPES SN7500, SN7501, SN7502

## SENSE AMPLIFIERS WITH DIGITAL-LEVEL OUTPUTS

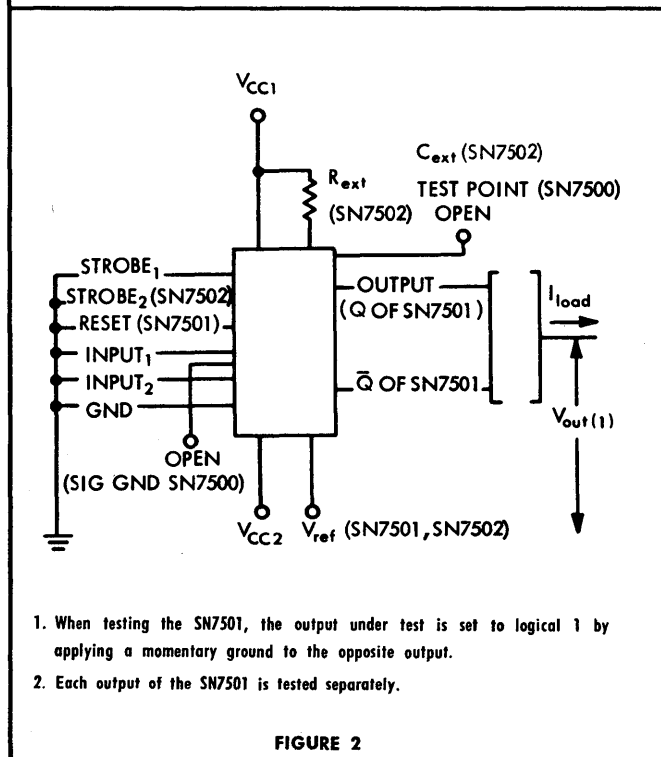
### PARAMETER MEASUREMENT INFORMATION

#### d-c test circuits†



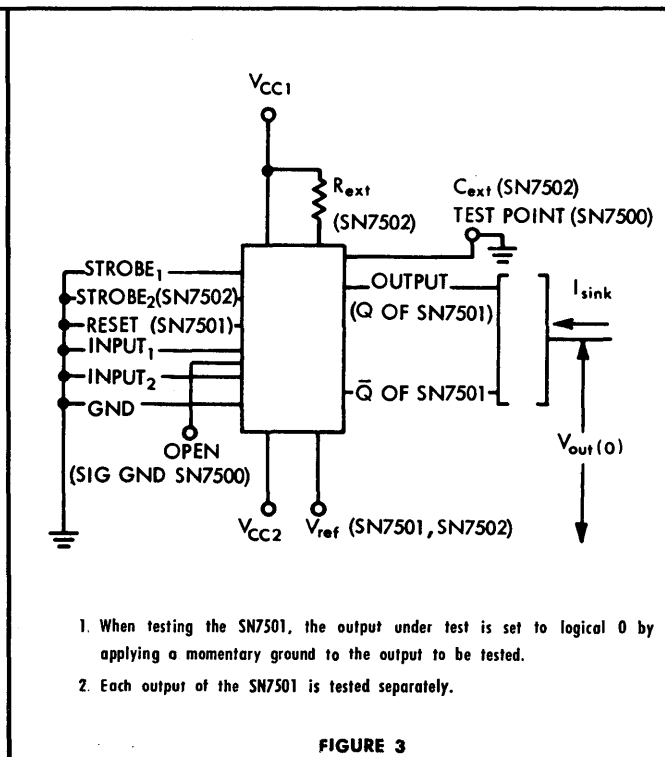
1. Both inputs are tested with voltages of the same polarity.
2. Strobe and reset input pulses are as shown in figure 8.
3. Both outputs are tested.
4. The differential-input threshold voltage ( $V_T$ ) is defined as that pulse or d-c input voltage ( $V_{in}$ ) just sufficient to cause the output (or outputs) to switch. For testing and correlation purposes a d-c input voltage is desirable.

FIGURE 1



1. When testing the SN7501, the output under test is set to logical 1 by applying a momentary ground to the opposite output.
2. Each output of the SN7501 is tested separately.

FIGURE 2



1. When testing the SN7501, the output under test is set to logical 0 by applying a momentary ground to the output to be tested.
2. Each output of the SN7501 is tested separately.

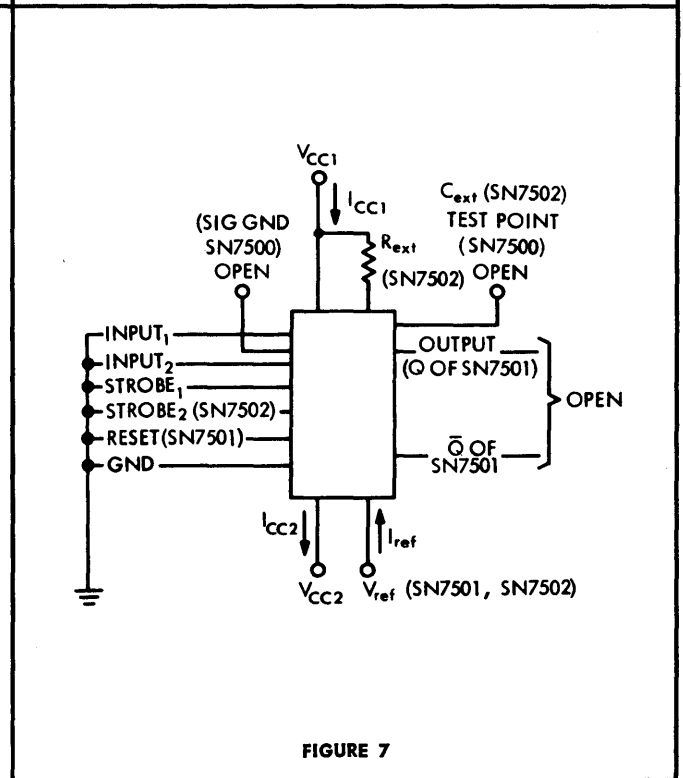
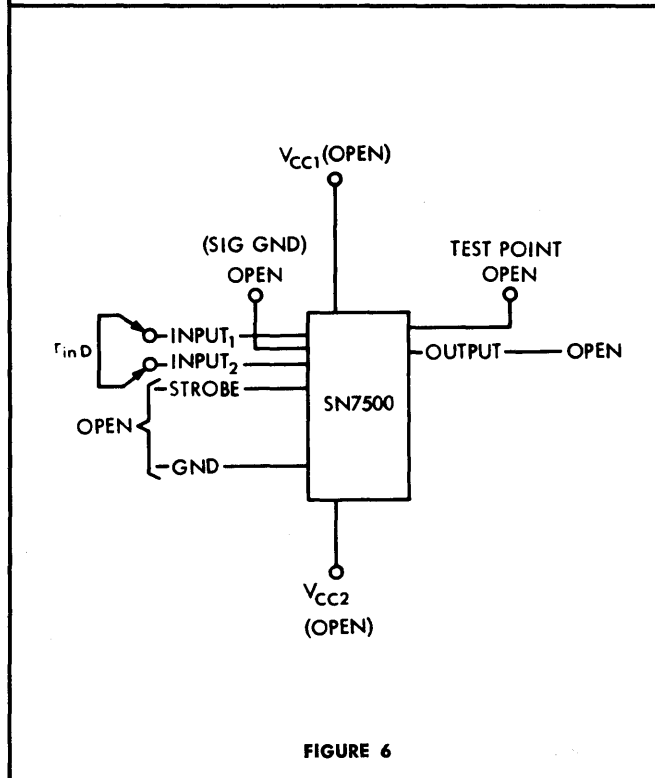
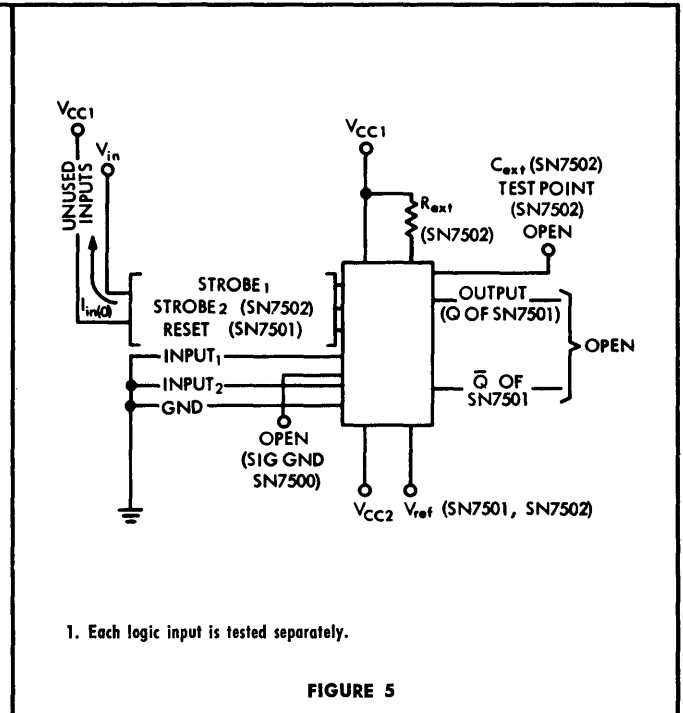
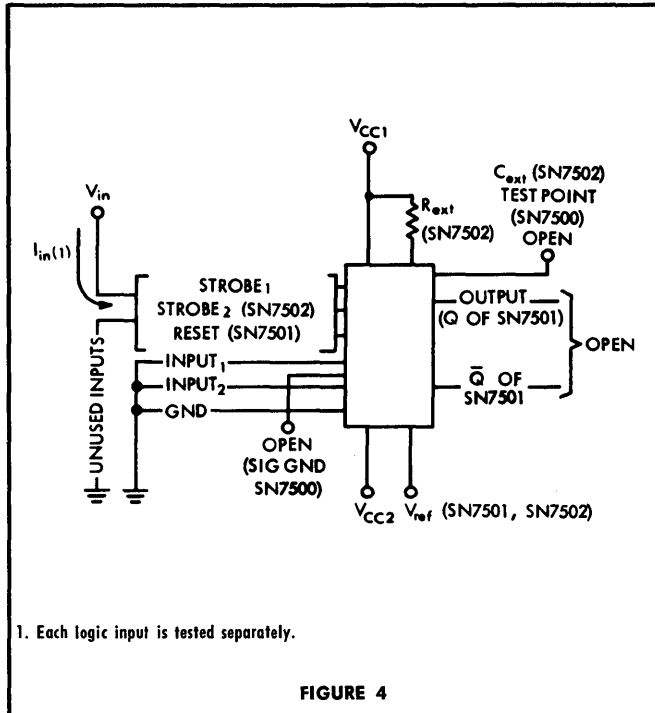
FIGURE 3

†Arrows indicate actual direction of current flow.

# TYPES SN7500, SN7501, SN7502 SENSE AMPLIFIERS WITH DIGITAL-LEVEL OUTPUTS

## PARAMETER MEASUREMENT INFORMATION

### d-c test circuits† (continued)



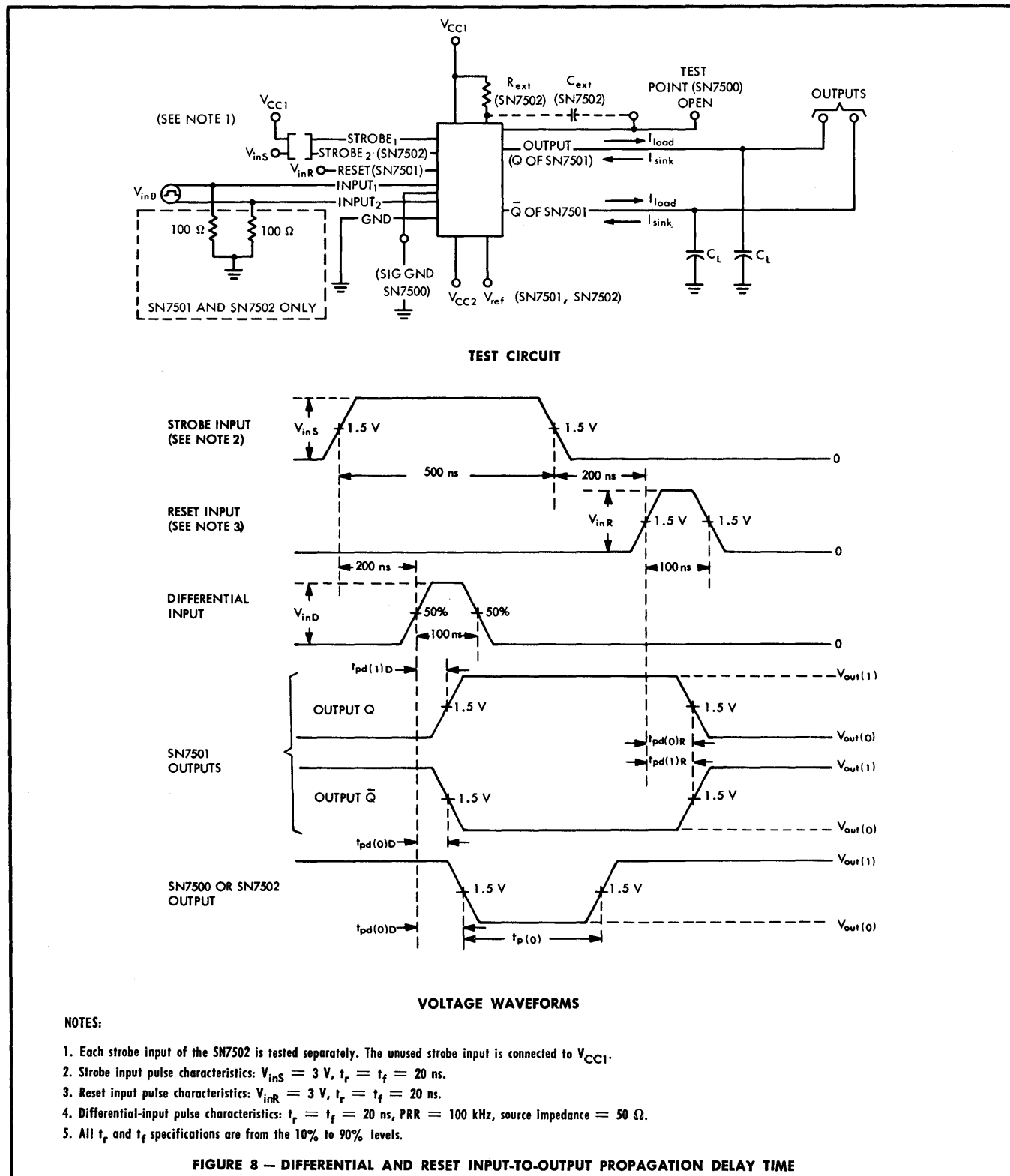
†Arrows indicate actual direction of current flow.

# TYPES SN7500, SN7501, SN7502

## SENSE AMPLIFIERS WITH DIGITAL-LEVEL OUTPUTS

### PARAMETER MEASUREMENT INFORMATION

#### switching characteristics†

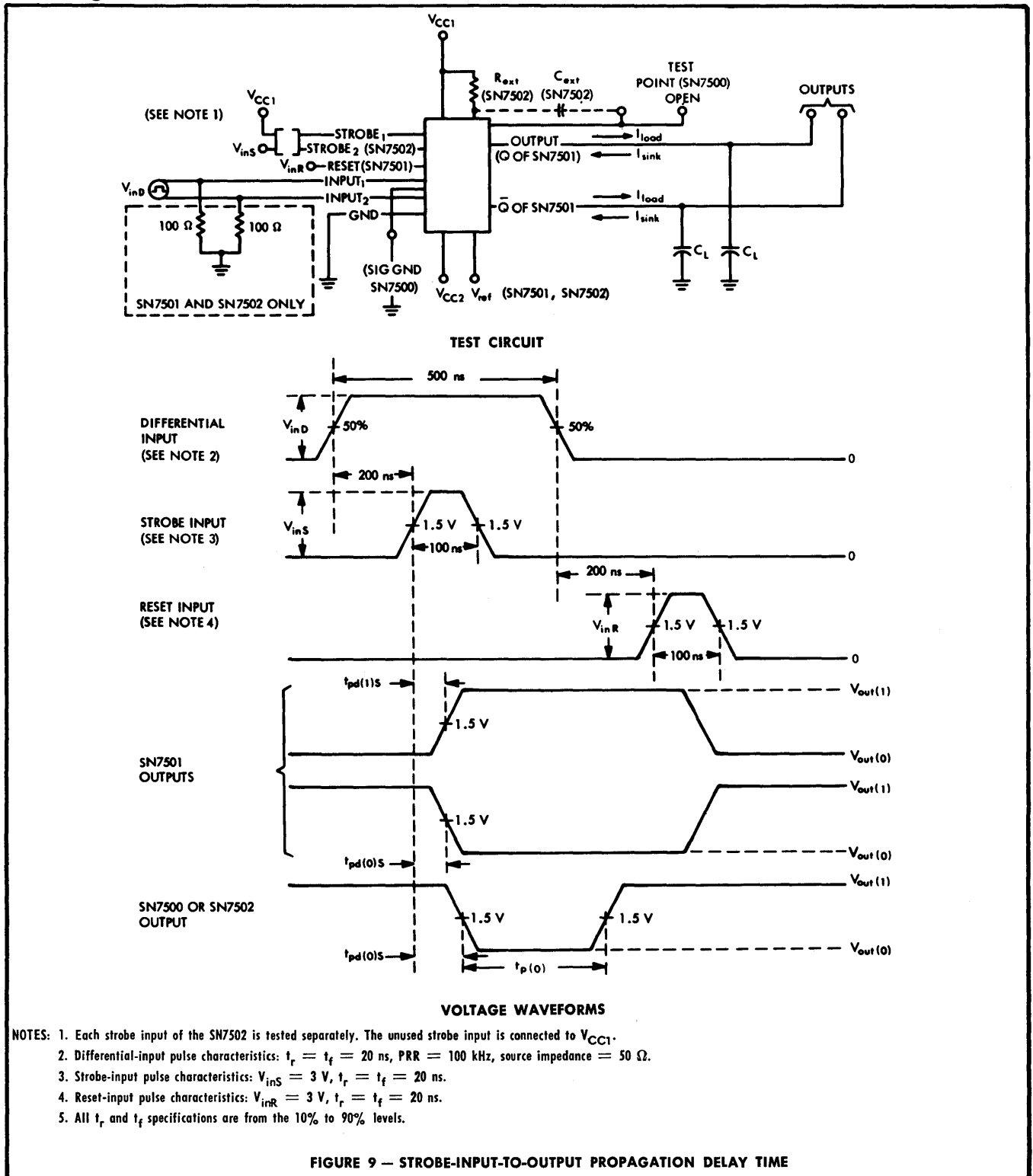


†Arrows indicate actual direction of current flow.

# TYPES SN7500, SN7501, SN7502 SENSE AMPLIFIERS WITH DIGITAL-LEVEL OUTPUTS

## PARAMETER MEASUREMENT INFORMATION

### switching characteristics† (continued)



†Arrows indicate actual direction of current flow.

# TYPES SN7500, SN7501, SN7502

## SENSE AMPLIFIERS WITH DIGITAL-LEVEL OUTPUTS

### TYPICAL APPLICATION DATA

#### coincident-current memory application

This application fully utilizes the flexibility of the SN7501 in a typical coincident-current memory design. See figure 10.

One SN7501 sense amplifier is used to read-out the information from one plane (up to 4096 cores) of the memory, representing one bit in a stored word. A word is read-out by reading one bit from each plane in parallel. A location is selected by coincident currents in appropriate x and y address lines. Cores in the "one" state switch to the "zero" state causing voltage pulses on their sense lines. Cores in the "zero" state do not switch but cause smaller amplitude voltage pulses on their sense lines. The sense amplifiers discriminate between these pulses representing stored logical "ones" and stored logical "zeros."

Since read-out is destructive, the information destroyed by read-out must be rewritten into the memory if it is to be retained for future use. A memory usually incor-

porates an inhibit register for this purpose. An important advantage of the SN7501 is that it contains a flip-flop that can be used as the inhibit register for its plane. "Ones" read from the memory "set" the flip-flops while "zeros" leave the flip-flops in their initial state. After read-out, therefore, the flip-flops of the SN7501's contain the information that was stored in the selected location. Since both outputs of the SN7501 flip-flops are brought out, both the selected word and its complement are available for use in the logic. The word thus stored in the SN7501's is available for use with the logic and for feedback to the inhibit drivers until a reset pulse clears the register prior to the next word read-out.

The variable-threshold capability of the SN7501 further extends its usefulness by allowing an optimum setting of the threshold level for a particular memory design. The threshold levels of the SN7501's in a memory may be adjusted either individually or in parallel.

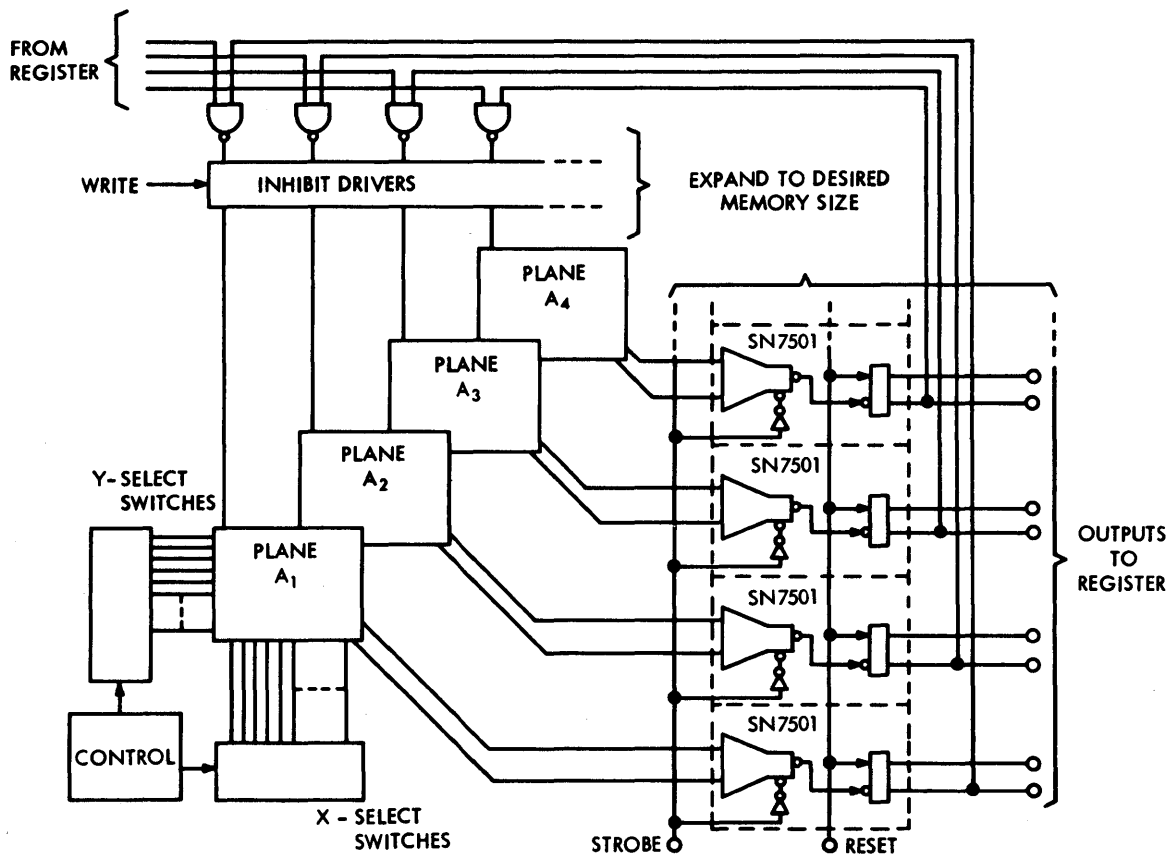


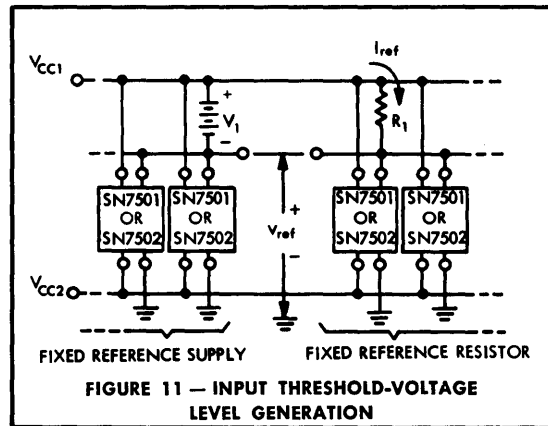
FIGURE 10 — COINCIDENT-CURRENT MEMORY USING SN7501 SENSE AMPLIFIERS

# TYPES SN7500, SN7501, SN7502 SENSE AMPLIFIERS WITH DIGITAL-LEVEL OUTPUTS

## TYPICAL APPLICATIONS

### variable threshold adjustment

The differential-input-threshold-voltage levels of the SN7501 or SN7502 may be adjusted for optimum memory performance by varying the amplitude of  $V_{ref}$ .  $V_{ref}$  should be derived from  $V_{CC1}$  or generated with respect to  $V_{CC1}$  rather than with respect to ground. (See figure 11) Any variations in  $V_{CC1}$  or  $V_{ref}$  will then cause minimal changes in the input-threshold-voltage level.



Using one of these methods, adjust  $V_{ref}$  to obtain the desired threshold voltage.  $R_1$  may be calculated as:

$$R_1 = \frac{V_{CC1} - V_{ref}}{I_{ref}}$$

This may apply for one sense amplifier or several sense amplifiers connected to the  $V_{ref}$  supply.  $V_1$  can be measured and fixed. Some bypassing may be necessary at the  $V_{ref}$  terminal to eliminate noise problems where long leads are used.

### SN7502 dot-OR capability

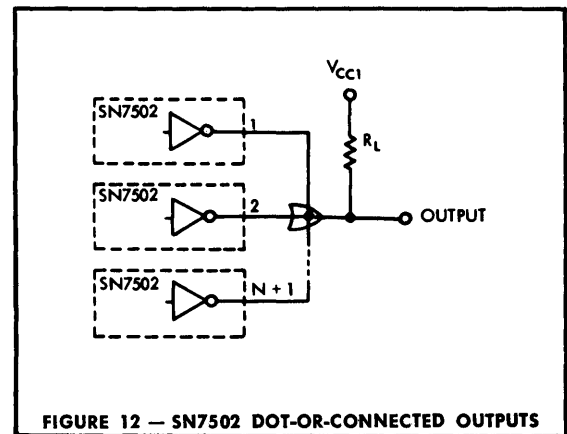
This application utilizes the output current sink capability of the SN7502 to perform the dot-OR function. The internal output load resistor of the SN7502 is approximately 7.5 k $\Omega$ . The output sink current is conservatively specified at 15 mA for a maximum  $V_{out(0)}$  of 0.4 V. For

this maximum  $V_{out(0)}$  the nominal internal load current for the SN7502 is computed as follows:

$$\frac{V_{CC1} - V_{out(0)}}{R_L} = \frac{5 - 0.4 \text{ V}}{7.5 \text{ k}\Omega} = 0.61 \text{ mA}$$

To drive a worst-case DTL or TTL input requires a sink current capability of 1.6 mA. The remaining 13.4 mA may be used for sinking dot-OR-connected outputs. (See figure 12) Additional dot-OR connections may be made to utilize the remaining 13.4 mA of sink current up to a maximum number  $N$  of:

$$N = \frac{13.4}{0.61} = 22$$

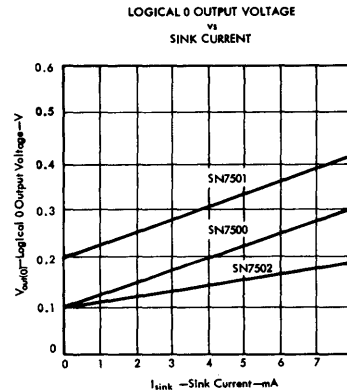
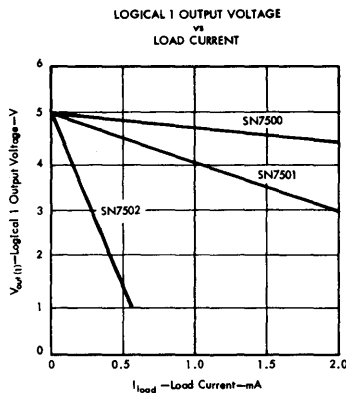


Since less than 22 outputs will normally be dot-OR-connected to each SN7502 output, the remaining current can be supplied from an external load resistor  $R_L$ . The load resistor reduces the output-voltage rise time to provide better capacitive-line driving capability. Value of the load resistor  $R_L$  may be calculated for a worst case (1.6 mA) DTL or TTL gate input load as follows:

$$R_L = \frac{4.6}{13.4 - n(0.61)} \text{ k}\Omega$$

where  $n$  = one less than the number of SN7502 outputs connected to perform the dot-OR function.

## TYPICAL CHARACTERISTICS



$S V_{CC1} = 5 \text{ V}$ ,  $V_{CC2} = -5 \text{ V}$ , and  $T_A = 25^\circ\text{C}$

# TYPES SN7500, SN7501, SN7502

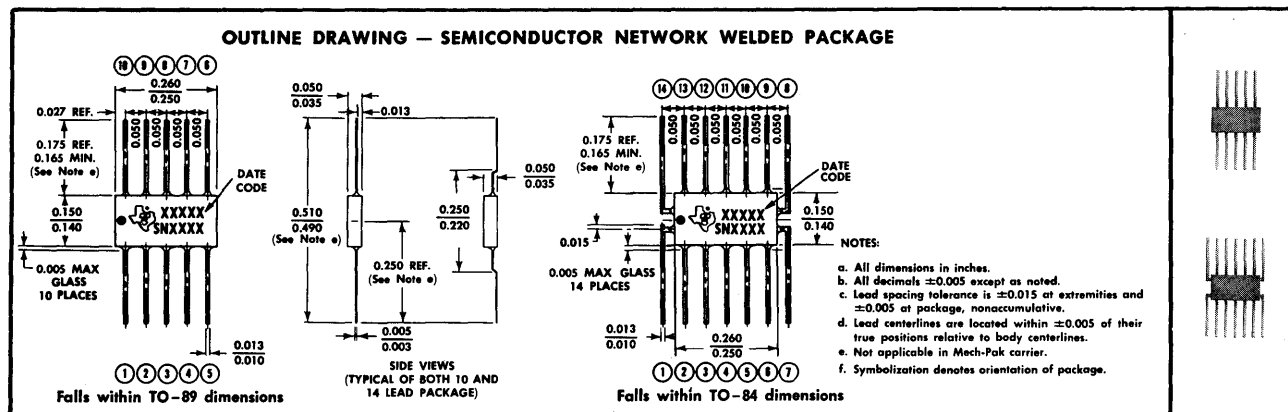
## SENSE AMPLIFIERS WITH DIGITAL-LEVEL OUTPUTS

### MECHANICAL DATA

#### general

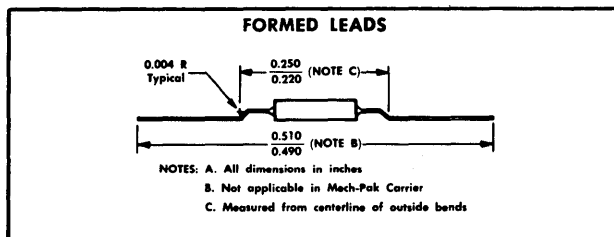
These three semiconductor networks are mounted in glass-to-metal hermetically sealed, welded packages. Package body and leads are gold-plated F-15<sup>†</sup> glass-sealing alloy. Approximate weight is

0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. All three networks are available with formed leads, insulators attached, and/or mounted in Mech-Pak carriers.



#### leads

Gold-plated F-15<sup>†</sup> leads require no additional cleaning or processing when used in soldered or welded assembly. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Standard lead length is 0.175 inches. Networks can be removed from Mech-Pak carriers with lead lengths up to 0.175 inches.

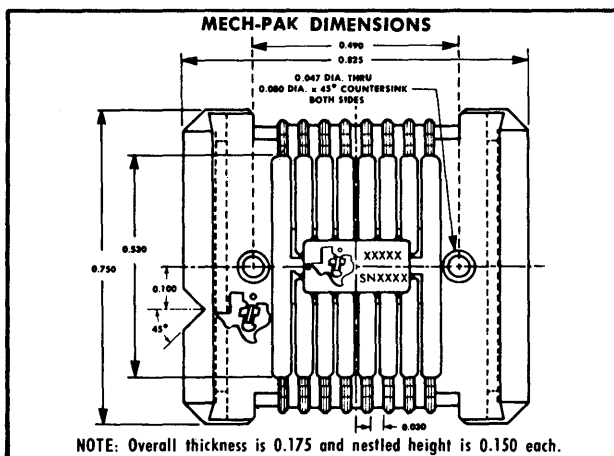


#### insulator

An insulator, secured to the back surface of the package, permits mounting networks on circuit boards which have conductors passing beneath the package. The insulator is 0.0025 inch thick and has an insulation resistance of greater than 10 megohms at 25°C.

#### mech-pak carrier

The Mech-Pak carrier facilitates handling the network, and is compatible with automatic equipment used for testing and assembly. The carrier is particularly appropriate for mechanized assembly operations and will withstand temperatures of 125°C for indefinite periods.



#### ordering instructions

Variations in mechanical configuration of semiconductor networks are identified by suffix numbers shown in a table at the right.

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
	Lead Length	Formed Leads	Insulators	Ordering Suffix	Not Applicable			
Lead Length	0.175 Inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5

<sup>†</sup>Patented by Texas Instruments

<sup>‡</sup>F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

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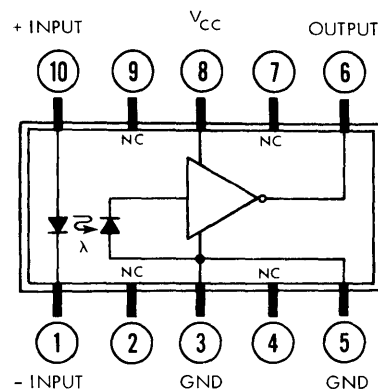
## SOLID CIRCUIT<sup>†</sup> SEMICONDUCTOR NETWORK<sup>‡</sup> AN EXPERIMENTAL OPTICALLY COUPLED DIGITAL INTEGRATED CIRCUIT

TYPE SNX1304  
BULLETIN NO. DL-S 669811, NOVEMBER 1966  
REPLACES BULLETIN NO. DL-S 657611, MAY 1965

### description

The SNX1304 is an experimental Optoelectronic Pulse Amplifier (OPA) for engineering evaluation. The OPA consists of a gallium arsenide p-n junction light emitter optically coupled to an integrated silicon photodetector feedback-amplifier circuit. The high input-output isolation of the optical coupling allows the OPA to function as a broad-band pulse transformer with response extending to zero frequency. The OPA is compatible for use with other digital integrated circuits. Applications include transmission of a-c or d-c signals across computer subsystem interfaces where circulating currents prevent interconnection of subsystem grounds, and rejection of common-mode noise at the end of a long data-transmission line.

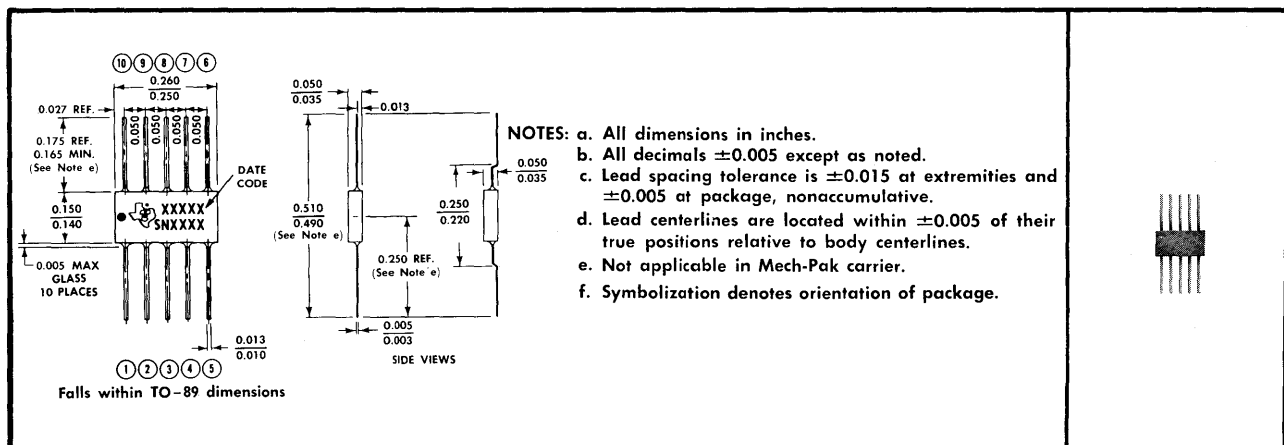
### circuit symbol and pin identification



NOTES: 1. Forward input polarity is indicated.  
2. NC — no internal connection.

### mechanical data

The SNX1304 pulse amplifier is mounted in a glass-to-metal hermetically sealed, welded package. Package outline meets JEDEC TO-89. Leads are gold-plated F-15<sup>‡</sup> glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit.



<sup>†</sup>Patented by Texas Instruments Incorporated

<sup>‡</sup>F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

PRELIMINARY DATA SHEET:  
Supplementary data will be  
published at a later date.



TEXAS INSTRUMENTS  
INCORPORATED  
SEMICONDUCTOR COMPONENTS DIVISION  
POST OFFICE BOX 5012 • DALLAS 22, TEXAS



# TYPE SNX1304

## OPTOELECTRONIC PULSE AMPLIFIER

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Input-to-Output Voltage . . . . .	$\pm 100$ V
Supply Voltage $V_{CC}$ . . . . .	+8 V
Reverse Input Voltage . . . . .	3 V
Forward Input Current . . . . .	.15 mA
D-C Fan-Out, $N_{DC}$ (See Note 1). . . . .	15
Operating Free-Air Temperature Range . . . . .	-55°C to 125°C
Storage Temperature Range . . . . .	-55°C to 125°C

### electrical characteristics

PARAMETER	TEST CONDITIONS	$V_{CC} = 3V$		$V_{CC} = 6V$		UNIT
		TYP	MAX	TYP	MAX	
$I_{in(th)}$ Forward Input Threshold Current	$V_{out} = 0.5 V, T_A = 125^\circ C$	5	10	5	10	mA
	$V_{out} = 0.5 V, T_A = -55^\circ C$	3		3		mA
$V_F$ Forward Input Voltage	$I_{in} = 1.3 I_{in(th)}, T_A = 125^\circ C$	1.1		1.1		V
	$I_{in} = 1.3 I_{in(th)}, T_A = -55^\circ C$	1.4		1.4		V
$V_{out(off)}$ "Off" Output Voltage	$I_{in} = 0, N_{DC} = 0, T_A = 125^\circ C$	2.5		5.2		V
	$I_{in} = 0, N_{DC} = 15, T_A = 125^\circ C$	2.3		5		V
	$I_{in} = 0, N_{DC} = 15, T_A = -55^\circ C$	1.9		4.2		V
$V_{out(on)}$ "On" Output Voltage	$I_{in} = 1.3 I_{in(th)}, T_A = 125^\circ C$	0.2		0.25		V
	$I_{in} = 1.3 I_{in(th)}, T_A = -55^\circ C$	0.1		0.2		V
$P_A$ Amplifier Power Dissipation (See Note 2)	$I_{in} = I_{in(th)}, N_{DC} = 0, T_A = 25^\circ C$	2.5		15		mW
	$I_{in} = 0, N_{DC} = 0, T_A = 25^\circ C$	3		20		mW

### switching characteristics

PARAMETER	TEST CONDITIONS	$V_{CC} = 3V$	$V_{CC} = 6V$	UNIT
		TYP	TYP	
$t_d$ Delay Time	$I_{in} = 1.3 I_{in(th)}, N_{DC} = 1, T_A = 25^\circ C,$ See Note 3	300	250	ns
$t_r$ Rise Time		200	150	ns
$t_s$ Storage Time		350	250	ns
$t_f$ Fall Time		250	200	ns

- NOTES: 1. One d-c load ( $N_{DC} = 1$ ) is defined by a circuit where  $C_s$  (see figure A) is selected so that the total capacitance of the test fixture, connectors, oscilloscope probe and  $C_s$  aggregates 50 pF. This rates fan-out in the same manner as Texas Instruments Series 51 networks.
2. This does not include the input power to the light-emitter diode.
3. The input pulse has the following characteristics:  $t_p = 5\mu s, t_r \leq 10 ns, t_f \leq 10 ns, f = 40 kHz$ .

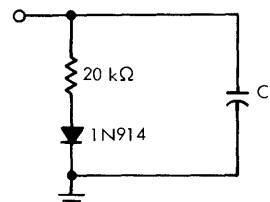
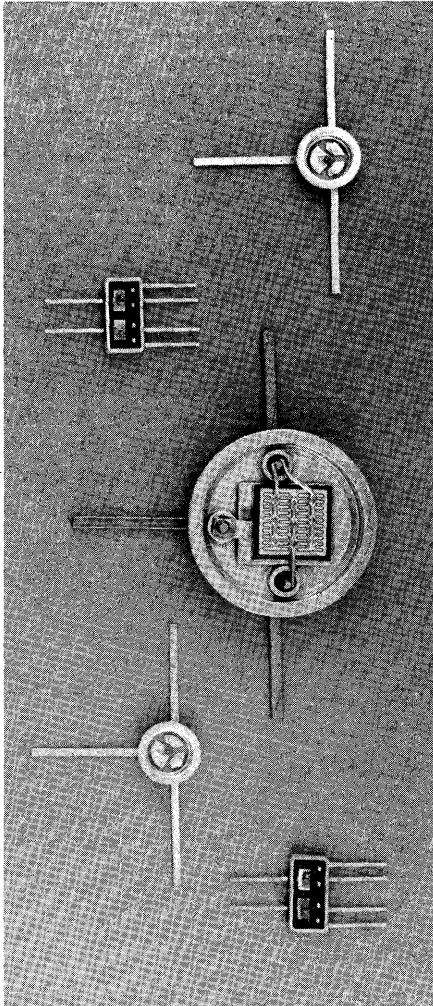


FIGURE A. D-C Load

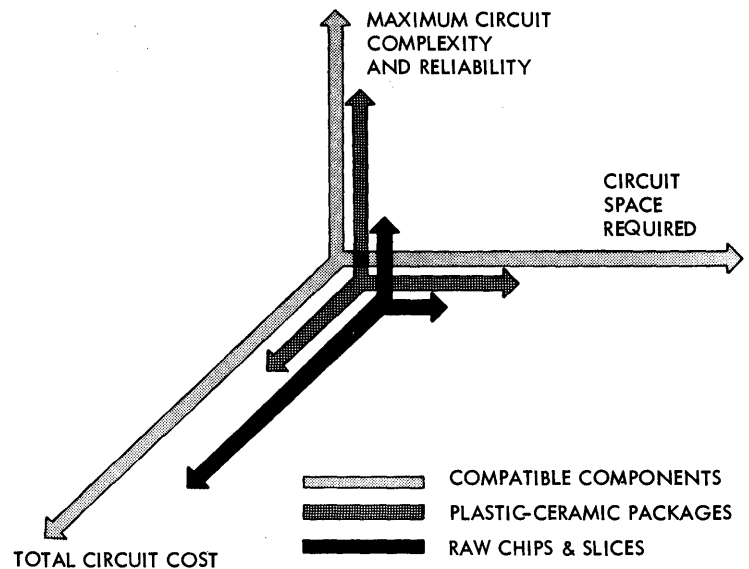
# INTERFACE COMPONENTS



Texas Instruments line of *Interface Components* has been designed to meet the broad range of requirements for military, space, industrial, and consumer applications.

*Interface Components* are available in a variety of microminiature packages described on the following pages. These packages include the *Compatible Components: TO-50, Thin-Pac, and Flat-Pac*; and the plastic-ceramic packages: *Chip-Pak, Pellet-Pak, and Flip-Channel-Pak*; the components are also available as raw chips and slices.

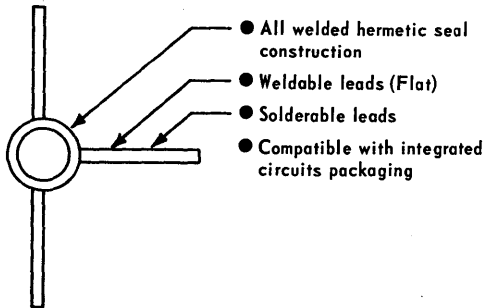
More than 5000 different silicon small-signal planar device types can be fabricated into these standard packages. Selection of the package configuration can be made by considering the requirements for reliability, size, assembly in hybrid circuits, and cost.



## WHAT ARE *COMPATIBLE COMPONENTS*?

Discrete components which are electrically and mechanically compatible with integrated circuits. TI *Compatible Components* are used to perform functions supplementary to integrated circuits. At the same time, they can be handled, tested, and assembled with the same or essentially similar techniques and tools used for integrated circuits.

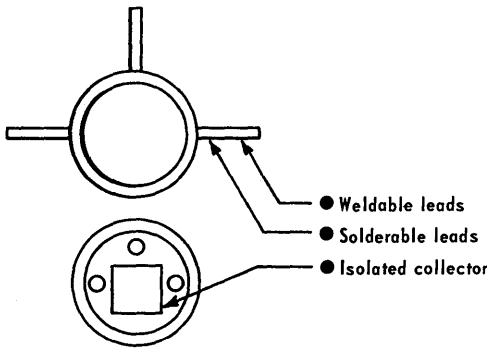
In addition, because of the form factors which are required to make components compatible with integrated circuits, most are also adaptable to circuit approaches requiring microminiature discrete components such as thin-film circuits.



- All welded hermetic seal construction
- Weldable leads (Flat)
- Solderable leads
- Compatible with integrated circuits packaging

TO-50

The **TO-50** hermetically sealed transistor package, introduced by Texas Instruments as the *µmesa*\* transistor package, is 0.210 inch in diameter and 0.050 inch thick.  
\*Trademark of Texas Instruments



- Weldable leads
- Solderable leads
- Isolated collector

THIN-PAC

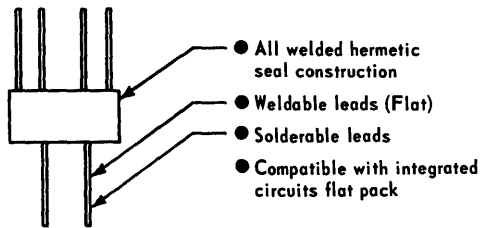
The **THIN-PAC** power transistor package was developed by Texas Instruments to meet the power requirements of miniature circuits. It offers 40 watts dissipation at 100 degrees C case temperature in a package only 0.680 inch in diameter by 0.170 inch thick.

### STANDARD COMPATIBLE COMPONENT DEVICE TYPES

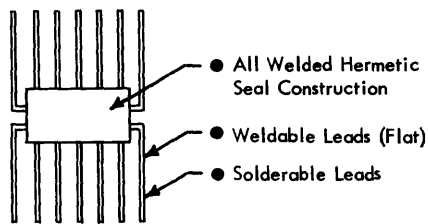
There are now more than two dozen EIA registered small-signal *Compatible Components* available from TI, plus many custom devices. Two types of compatible power transistors and a large number of diode types in miniature packages are also available.

NEAREST STANDARD*	DESCRIPTION	COMPATIBLE COMPONENT	NEAREST STANDARD*	DESCRIPTION	COMPATIBLE COMPONENT
2N929/2N2639	NPN Diff. Amp 10% Match	2N3046 Flat Pack Dual	2N929	NPN High-Gain Amp	2N2387 TO-50
2N929/2N2640	NPN Diff. Amp 20% Match	2N3047 Flat Pack Dual	2N930	NPN High-Gain Amp	2N2388 TO-50
2N929/2N2641	NPN Unmatched	2N3048 Flat Pack Dual	2N696	NPN General Purpose	2N2395 TO-50
2N930/2N2642	NPN Diff. Amp. 10% Match	2N3043 Flat Pack Dual	2N697	NPN General Purpose	2N2396 TO-50
2N930/2N2643	NPN Diff. Amp. 20% Match	2N3044 Flat Pack Dual	2N1613	NPN General Purpose	2N2389 TO-50
2N930/2N2644	NPN Unmatched	2N3045 Flat Pack Dual	2N1711	NPN General Purpose	2N2390 TO-50
2N2412/2N2805	PNP Diff. Amp 10% Match	2N3049 Flat Pack Dual	2N2243	NPN General Purpose	2N3037 TO-50
2N2412/2N2806	PNP Diff. Amp 20% Match	2N3050 Flat Pack Dual	2N1890	NPN General Purpose	2N3038 TO-50
2N2412/2N2807	PNP Unmatched	2N3051 Flat Pack Dual	2N1131	PNP General Purpose	2N2393 TO-50
2N914	NPN Driver	2N3052 Flat Pack Dual	2N1132	PNP General Purpose	2N2394 TO-50
2N2497 FET	P-Channel FET Diff. Amp 5% Match	2N3333 Flat Pack Dual	2N2904	PNP General Purpose	2N3040 TO-50
2N2497 FET	P-Channel FET Dual Unmatched	2N3336 Flat Pack Dual	New Product	NPN 10-Amp Power Switch (60 v)	2N3551 Thin-Pac
2N2222/2N2907	Complementary Pair	2N3838 Flat Pack Dual	New Product	NPN 10-Amp Power Switch (80 v)	2N3553 Thin-Pac
2N706A	NPN Switch	2N849 TO-50			
2N753	NPN Switch	2N850 TO-50			
2N743	NPN Switch	2N851 TO-50			
2N744	NPN Switch	2N852 TO-50			

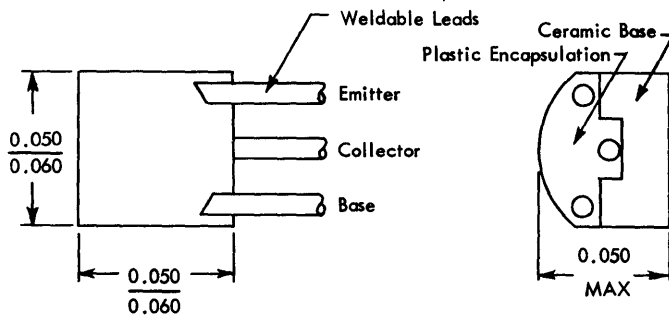
\*Single or dual where applicable



FLAT PACK



CUSTOM FLAT PACK



CHIP-PAC

The dual SCN hermetically sealed **FLAT PACK** offers component miniaturization with no compromise in electrical or mechanical characteristics. The package measures 0.250 by 0.150 by 0.050 inch.

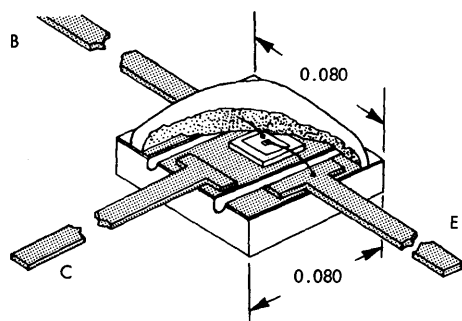
**CUSTOM FLAT PACK** configurations are also available for *Compatible Components*. Custom devices may be supplied in the 6-, 10-, or 14-lead hermetically sealed package. Four discrete planar transistors can be supplied in one **FLAT PACK** with all leads isolated. Five to six transistors in one package are possible with certain interconnections. Custom configurations are the same size as the dual SCN **FLAT PACK**.

The **CHIP-PAC** is the ultimate in discrete transistor miniaturization. Transistor chips are alloyed to a metallized ceramic base and are plastic encapsulated. The package provides a relatively high degree of environmental protection. The gold-plated leads are weldable and solderable. Standard **CHIP-PAC** devices include:

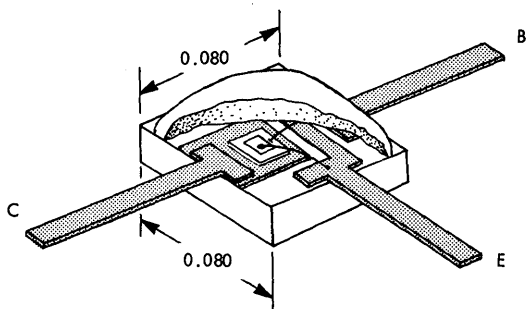
Nearest Standard	Description	CHIP-PAC
2N929	NPN Diff. Amp.	TIS22
2N930	NPN Diff. Amp.	TIS23
2N2484	NPN Diff. Amp.	TIS24

### HOW RELIABLE ARE COMPATIBLE COMPONENTS?

More than five thousand TI *Compatible Components* have been subjected to high-level step-stress tests as a part of the extensive quality and reliability testing requirements of the Component Quality Assurance Program (CQAP) for the Minuteman II Program. The program has as its goal component use-condition failure rates in the order of ten-thousandths of a percent (.000X%) per thousand hours. The program is keyed to constant product improvement, using destructive testing techniques to determine potential failure mechanisms. At TI this means that the active chips themselves, as well as the package in which the chips are contained, are undergoing constant process improvement. Tests results are analyzed, and even subtle and very obscure failure mechanisms are isolated and attacked systematically through the process improvement feedback loop. Extensive reliability data is available. Contact your TI Field Sales Engineer.



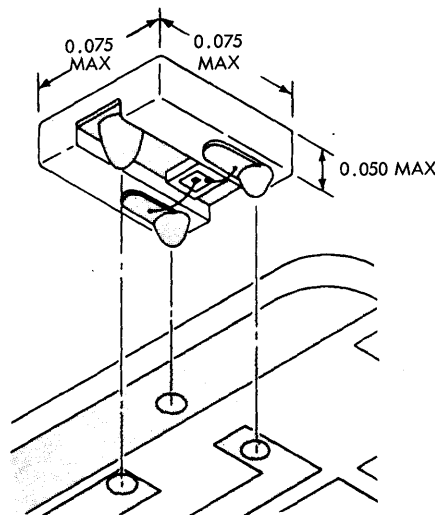
PELLET-PAK



HIGH-FREQUENCY PELLET-PAK

**PELLET-PAK** devices are low-cost fully tested micro-miniature packages available with both solderable and weldable leads designed for automated assembly. They feature a plastic sealed ceramic header and low thermal resistance. High-frequency models with low lead inductance are also available. Their environmental capabilities match those of canned transistors.

The **FLIP-CHANNEL-PAK** is specially designed for leadless automated thermal or ultrasonic bonding to film substrates. It retains all other features of the **PELLET-PAK** configuration.



FLIP-CHANNEL-PAK

### RAW CHIPS AND SLICES

Silicon transistors in raw chip and slice form have the lowest initial cost and smallest possible size. Although relatively sophisticated bonding and alloying technologies are required, substantial savings may be achieved in non-critical operations. Texas Instruments can supply any device from its broad line of silicon planar transistors in either chip or slice form.

### WHERE ARE *INTERFACE COMPONENTS* USED?

In any application requiring a high-quality miniature semiconductor. Here are some applications where TI *Interface Components* are being used today:

- Digital and analog interface circuits, for integrated circuits
- Driver circuits
- Sense amplifiers
- Thin-film circuits
- Critical differential amplifiers
- High-impedance amplifiers
- Special analog circuits
- D-c amplifiers
- Diode matrixes
- Complementary (NPN/PNP) circuits
- Power switching to 5 amps

Functionally, the devices fall into the following categories:

- Differential amplifiers (dual elements), NPN and PNP
- Low-level, low-noise amplifiers (dual elements), NPN and PNP
- Low-level switching (dual elements), NPN and PNP
- Dual drivers, NPN
- High-current driver and power switches, NPN
- Drivers (single), NPN and PNP
- High-speed switches (single) NPN
- Multiple diodes in most common configurations



