Mach IV Procurement Specification

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CONTENTS

MACH IV PROGRAM

1.0 SCOPE

1.1 This specification establishes standards for materials, workmanship, performance capabilities, identification and processing of high reliability, monolithic integrated circuits.

1.2 Intent

The intent of this document is such as to recognize that quality and reliability are *built* into, not *tested* into, a product. There is no specification or screening procedure that can substitute for inherent, built-in reliability. However, it must be realized that irrespective of lot quality, there will always be some small percentage of devices that are subject to early failure (infant mortality). A well engineered screening procedure will eliminate most, if not all, of these early failures. Secondly, the screening and acceptance testing described herein will also serve to demonstrate, with a high degree of statistical confidence, that the required levels of quality and reliability have, in fact, been built into the product.

2.0 APPLICABLE DOCUMENTS

2.1 The following specifications and standards, of the issue in effect on the date of invitation for bids or request for proposal, form a part of this specification to the extend specified herein:

2.2 Specifications

Military

MIL-M-55565	Microcircuits, Packaging of
MIL-M-38510	Microcircuits Devices, General Specification for

2.3 Standards

Military

MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
MIL-STD-883	Test Methods and Procedures for Microelectronics (dated November 20, 1969)
MIL-STD-790	Reliability Assurance Program for Electronic Parts Specification
MIL-STD-1276	Leads, Weldable, for Electronic Components Parts
MIL-STD-1313	Microelectronics Terms and Definitions
MSFC-STD-355	Radiographic Inspection Standard for Electronic Parts

Detail Specifications

SNXXXX	Detail Specification for a Particular Part Type (e.g., Manufacturer's (Data Sheet)

TEXAS INSTRUMENTS
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2.4 Precedence of Documents

For the purpose of interpretation, in case of any conflicts, the following order of precedence shall apply:

a)	Purchase Order	—The purchase order shall have precedence over any referenced specification.
b)	Detail Specification	—The detail specification shall have precedence over this specification and other referenced specifications.
c)	This Specification	—This specification shall have precedence over all referenced specifications.
d)	Referenced Specifications	—Referenced Specifications shall apply to the extend specified herein.

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2.5 Federal and/or military specifications and standards required shall be obtained from the usual government sources.

3.0 GENERAL REQUIREMENTS

The individual item requirements shall be as specified herein and in accordance with the applicable detail specification. In the event of any conflict between the requirements of this specification and the detail specification, the latter shall govern. The static and dynamic electrical performance requirements of the integrated circuits plus absolute maximum ratings and test methods shall be as specified in the detail specifications.

3.1.1 Definitions

a)	LTPD	Lot Tolerance Percent Defective shall be as defined by MIL-M-38510.
b)	λ	Lambda, stated in percent per 1000 hours as defined by MIL-M-38210.
c)	MRN	Minimum Reject Number as defined by MIL-M-38210
d)	Production Lot	For the purpose of this specification, a production lot shall be defined per MIL-M-38510.
f)	C	Acceptance number as defined by MIL-M-38510

3.1.2 Terms and Definitions

Terms and definitions shall be as defined in MIL-STD-1313.

3.1.3 Classification of Requirements

The requirements for the integrated circuits are classified herein as follows:

Requirement	Paragraph
Processing Conditioning, Testing and Screening	3.2
Qualification	3.3
Design and Construction	3.4
Marking of Integrated Circuits	3.5
Product Assurance	3.6
Workmanship	3.7
Performance Capabilities	3.8

3.2 Process Conditioning, Testing and Screening

Four levels of quality assurance for integrated circuits are provided for in this specification. Process conditioning, testing and screening shall be as specified in 4.3 and the applicable figure for the appropriate quality assurance level stated on the purchase order and defined as follows:

Prefix	Quality Assurance Process Level	Applicable Process Flow Chart
SNM	I	Figure 1
SNA	II	Figure 2
SNC	III	Figure 3
SNH	IV	Figure 4

3.3 Qualification

Vendor qualification for delivery of integrated circuits to this specification shall be as specified in paragraph 4.2.

3.4 Design and Construction

Integrated circuit design and construction shall be in accordance with the requirements specified herein and in the applicable detail specification.

3.4.1 Topography

Integrated circuits furnished under this specification shall have topography information available for review by procuring activity. The information made available shall provide sufficient data for thorough circuit design, application, performance, and failure analysis studies.

3.4.1.1 Monolithic Die Topography

An enlarged photograph or drawing (to scale) with a minimum magnification of 80 times the die (chip) size showning the topography of elements formed on the silicon monolithic die shall be available for review. This shall be identified with the specific detail integrated circuit part-type in which it is used and the applicable detail specification.

3.4.1.2 Die Intraconnection Pattern

An enlarged photograph or drawing (to scale) with a minimum magnification of 80 times the die (chip) size showing the specific intraconnection pattern utilized to intraconnect the elements in the circuit. This shall be in the same scale as the die topography 3.4.1.1 so that the elements utilized and those not being used can easily be determined.

3.4.2 Materials

Materials shall be inherently non-nutrient to fungus and shall not blister, crack, outgas, soften, flow or exhibit other immediate or latent defects that adversely affect storage, operation or environmental capabilities of integrated circuits.

3.4.2.1 Material Section

Materials selected for use in the construction of the integrated circuits shall be chosen for maximum suitability for the application. This shall include consideration of the best balance for:

a) Electrical performance

b) Thermal compatibility and conductivity

c) Chemical stability including resistance to deleterious interactions with other materials

d) Metallurgical stability with respect to adjacent materials and change in crystal configuration

e) Maximum stability with regard to continued uniform performance through the specified environmental conditions and life.

PROCESS FLOW CHART FOR LEVEL I (SNM)

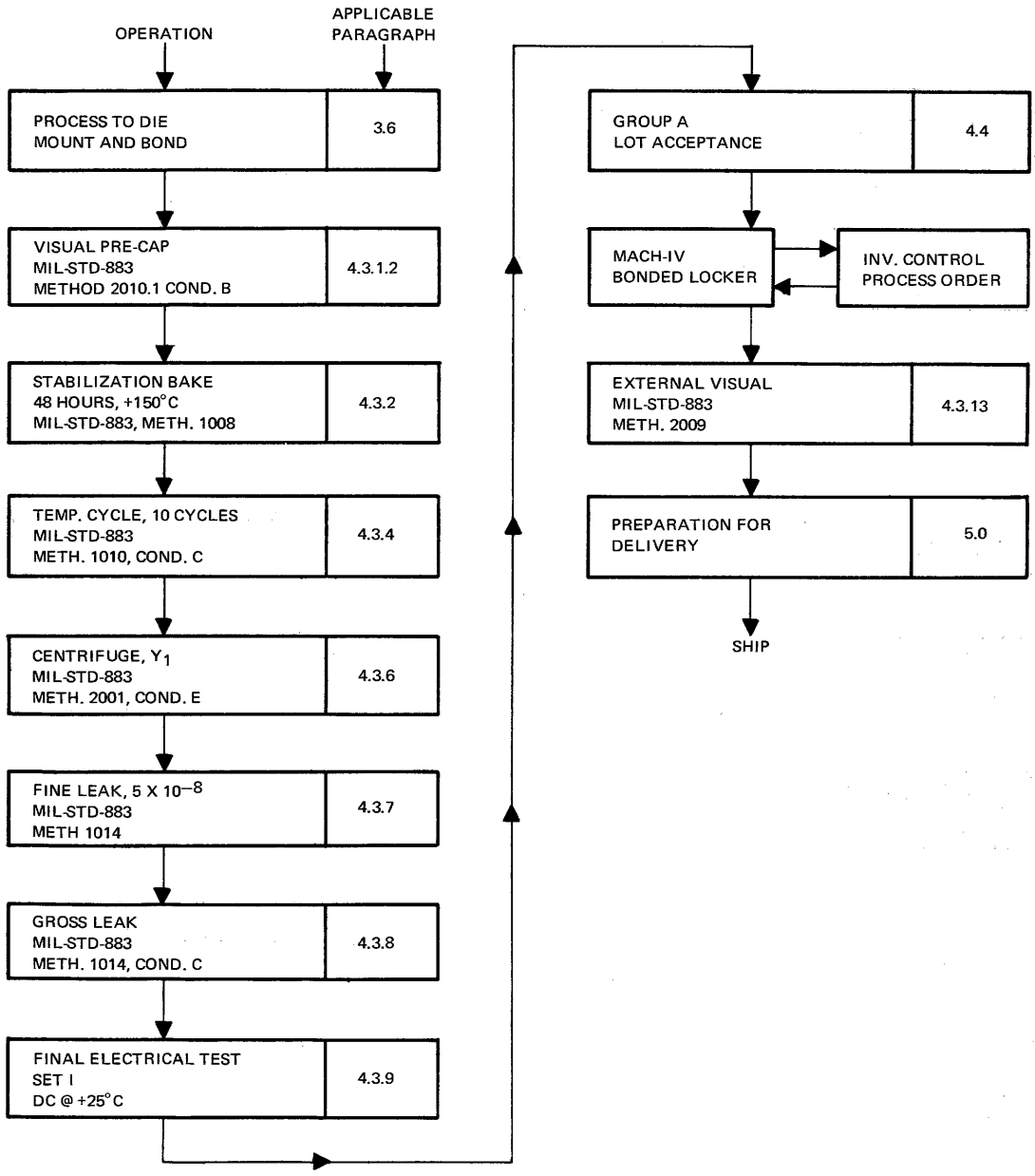

FIGURE 1

PROCESS FLOW CHART FOR LEVEL II (SNA)

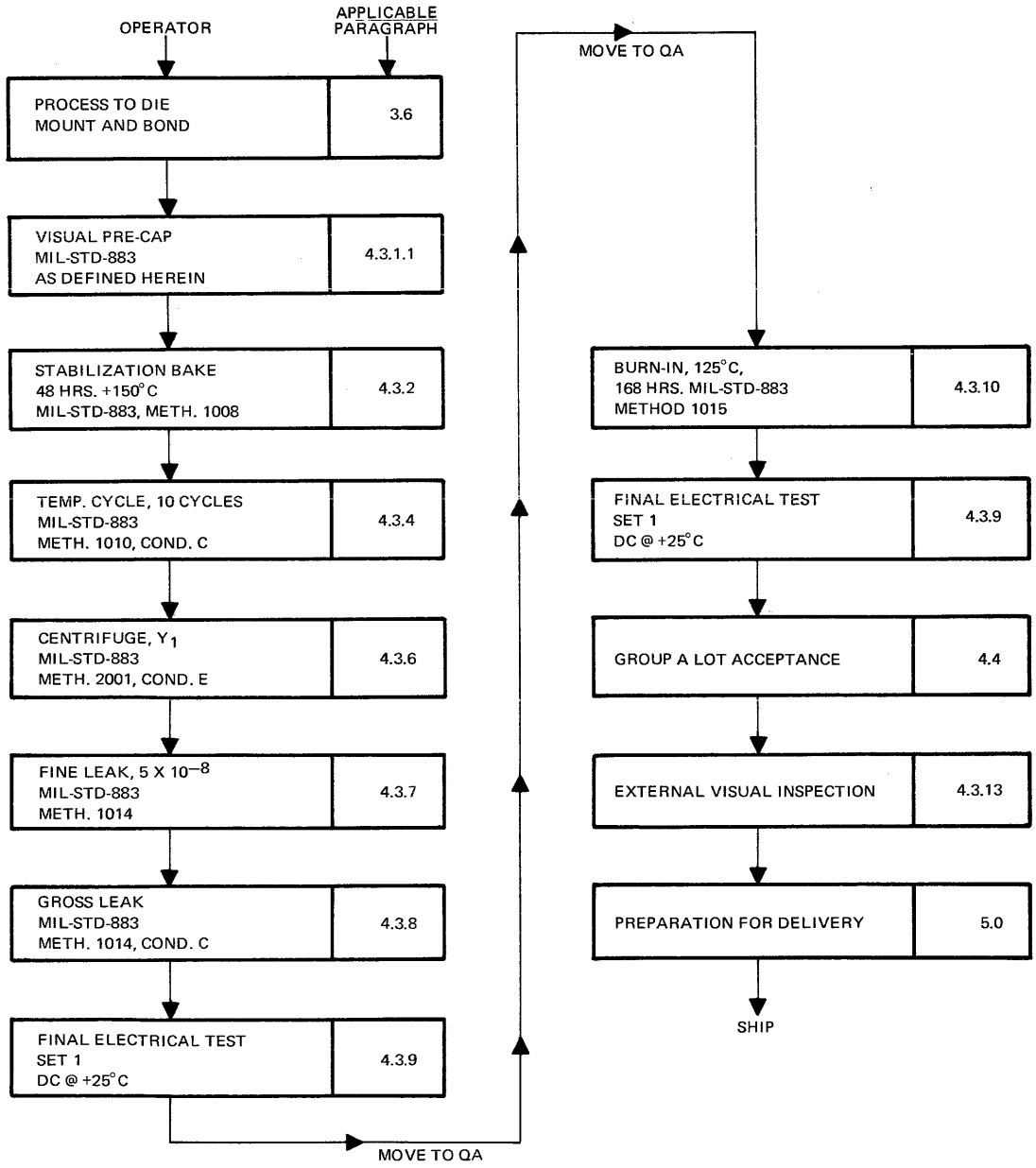

FIGURE 2

PROCESS FLOW CHART FOR LEVEL III (SNC)

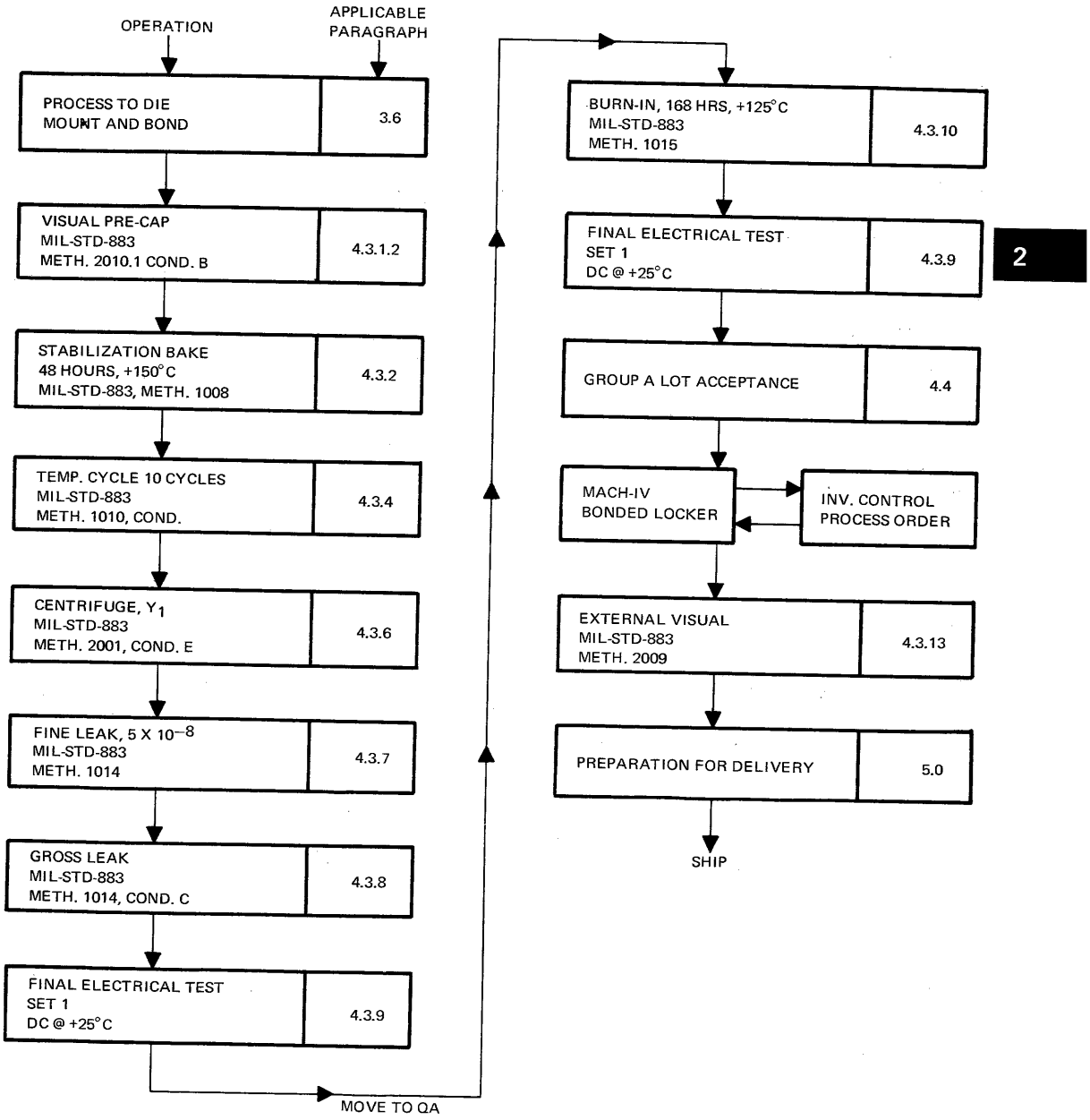

FIGURE 3

PROCESS FLOW CHART FOR LEVEL IV (SNH)

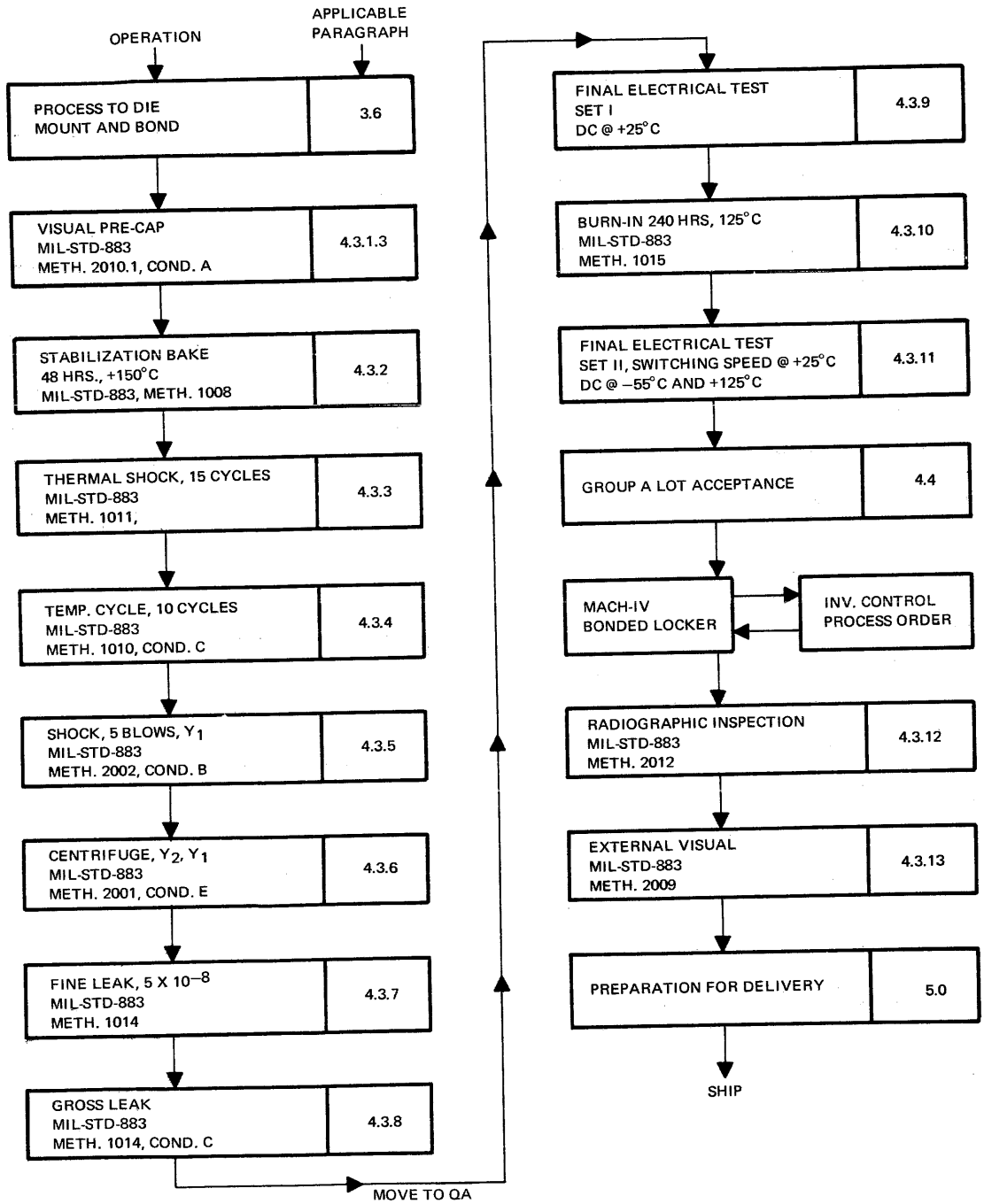

FIGURE 4

3.4.2.2 Foreign Materials

No lacquer, grease, paste, desiccant or other similar foreign encapsulant or coating material shall be included in the circuit enclosure nor applied to any part of the internal circuit assembly.

3.4.3 Mechanical

3.4.3.1 Case

Each integrated circuit shall be securely mounted and hermetically sealed within a case designed and constructed to conform to the outline and physical dimensions shown in the detailed specification. External surfaces of the integrated circuit case shall be unpainted except for markings.

3.4.3.2 Interconnections

Interconnections within the integrated circuit case shall be minimized and there shall be no wire crossovers. Circuit intraconnections by means of wire jumpers shall not be used. (See Note 6.2)

3.4.3.3 Leads

Lead material, construction, and outline shall be as specified on the detail specification and shall be capable of meeting the solderability test of MIL-STD-883, Method 20-3. (See Note 6.4).

3.4.3.3.1 Lead Size

Lead outline and dimensions shall be as specified in the detail specification.

3.4.3.3.2 Lead Surface Condition

Leads shall be free of the following defects over their entire length when inspected under a minimum of 4X magnification:

a) Foreign materials adhering to the leads such as paint, film, deposits and dust. Where adherence of such foreign materials is in question, leads may be subjected to a clean, contaminant-free (e.g., oil, dust, etc.), filtered air stream (suction or expulsion) or 88 feet per second maximum, or a wash/rinse as necessary and reinspected.

b) Nicks, cuts, scratches or other surface defacing defects which expose the base metal.

3.4.3.3.3 Lead Straightness

Leads shall be aligned within a 0.050-inch diameter, 0.050-inch length cylinder concentric to the point of lead emergence from the case and the X-axis (the axis parallel to the lead axis). Along the remaining lead length, there shall be no unspecified bend whose raduis is less than 0.10 inch and no twist whose angle is greater than 10° (ribbon leads, only).

3.4.3.3.4 Preformed Leads

Preformed leads, when specified, shall be in accordance with the detail specification. The part number of the integrated circuit shall remain as specified in the applicable detail specification or purchase order, the applicable suffix designation shall appear on the purchase order but shall not be marked on the device.

3.4.3.3.5 Carriers (Mech-Pak Carrier)

Carrier-matrix assemblies consisting of individually mounted integrated circuits shall be furnished when so specified by purchase order. The individual carrier shall have provisions for use with automatic test equipment contacts. Devices supplied "clipped-out" of the Mech-Pak Carrier shall be supplied in the Barnes Carrier type 029-188 or equivalent. (Applicable for Flat Packs only.)

3.5 Marking of Integrated Circuits

3.5.1 Legibility

All marking shall be permanent in nature and remain legible when subjected to specified operating, storage, and environmental requirements. All markings shall be insoluble in standard solvents such as trichlorethylene, water and xylene.

3.5.2 Marking Details

Marking of the integrated circuits shall be located as follows unless otherwise specified in the detail specification:

a) TO-100 (TO-5) and similar "can" cases shall be marked on the top of the case. Where space limitations exist, the side of the case may be used.

b) Flat Packs shall be marked on the top of the case. Where space limitation exists, the bottom of the package may be utilized as necessary. As a minimum the top of the package shall show the manufacturer's identification mark or symbol, the device part number, date code, and pin 1 orientation mark (where applicable).

c) Dual in-line plug-in packages shall be marked in the same manner as flat packs.

3.5.3 Required Device Marking

a) Index point indicating the starting point for numbering of leads shall be as indicated in the detail specification. The indexing point may be a tab, color dot, or other suitable indicator.

b) Manufacturer's identification mark or symbol.

c) A four or five digit alpha-numeric lot date code indicating the week of initial Group A acceptance. The date code shall be as follows:

1) EIA four digit date code, the first two numbers shall be the last two digits of the year, the last two numbers shall indicate the calendar week.

2) A Gothic letter which identifies separate lots of the same device type processed within the same calendar week. (If no more than one lot is processed through Lot Acceptance in a given calendar week, the Gothic letter may be omitted).

d) Manufacturer's part number.

e) Individual device serial number (if required)

f) A dot to indicate acceptance to Radiographic inspection

NOTE:

When a color dot is used to identify pin one, the radiographic inspection acceptance dot shall be placed on the bottom of the package.

3.6 Product Assurance

The manufacturer shall establish and maintain a reliability assurance program that complies with the basic intent of MIL-STD-790. Furthermore, it is intended that each integrated circuit delivered shall be free of any defect in design, material, manufacturing process, testing and handling, which would degrade or otherwise limit its performance when used within the specified limits.

3.6.1 Visual and Mechanical Examination

Integrated circuits shall be examined to verify that material, design, construction, physical dimensions, marking and workmanship are in accordance with the specified acceptance criteria.

3.6.2 Test Equipment

The manufacturer shall prepare and maintain a current list, by name and drawing number or other unique identification, of test equipment used in the manufacturing and testing of devices submitted for acceptance inspection under this specification. This list shall be made available to the procuring activity representative upon request.

3.6.3 Process Control

Each integrated circuit shall be constructed by manufacturing processes which are under the surveillance of the manufacturer's Quality Control department. The processes shall be monitored and controlled by use of statistical techniques in accordance with published specifications and procedures. The manufacturer shall prepare and maintain suitable documentation (such as quality control manuals, inspection instructions, control charts, etc.) covering all phases of incoming part and material inspection and in-process inspections required to assure that product quality meets the requirements of this specification. The procuring activity may verify, with the permission of and in the company of the manufacturer's designated representative, that suitable documentation exists and is being applied. Information designated as proprietary by the manufacturer will be made available to the procuring activity or its representative only with the written permission of the manufacturer.

Process control is recognized as being vital to the concept of "built-in" quality. Appendix A defines an acceptable process-control system. Devices delivered to this specification shall be manufactured in a controlled system similar to that set forth in Appendix A.

3.6.4 Production Changes

The manufacturer shall advise the procuring activity of the time at which any major change(s) in production or QC methods or documentation become effective during the period of device production for delivery against any given purchase order referencing this specification.

3.7 Workmanship

Integrated circuits shall be manufactured and processed in a careful and workmanlike manner, in accordance with the production processes, workmanship instructions, inspection and test procedures, and training aids prepared by the manufacturer in fulfillment of the reliability assurance program established by paragraph 3.6.

3.7.1 Personnel Certification

The manufacturer shall be responsible for training, testing and certification of personnel involved in producing integrated circuits. Training shall be commensurate and consistent with the requirements of this specification and in conformance to the basic intent of MIL-STD-790. Training aids in the form of satifactory criteria shall be available for operator and inspector review at any time.

3.7.2 Personnel Evaluation

The supplier shall maintain a continuous evaluation of the proficiency of personnel concerned with production and inspection. Retraining of an operator or inspector shall be required when this evaluation establishes that a degree of proficiency necessary to meet the requirements of this specification is not being exercised.

3.7.3 Rework Provisions

3.7.3.1 Rework

All rework on microcircuits manufactured under this specification shall be accomplished in accordance with paragraph 3.7.1 of MIL-M-38510 except as defined herein.

3.7.3.2 Rebonding

Rebonding of integrated circuits shall be permitted with the following limitations:

a) No scratches, open or discontinuance metallization paths or conductor patterns shall be repaired by bridging with or addition of bonded wire or ribbon.

b) Rebonding at individual bonding pad locations shall be limited to a maximum of 3 rebonds for 14 pin devices, 4 rebonds for 16 pin devices, 7 rebonds for devices with more than 16 pins, and 2 rebonds for devices with less than 14 pins.

c) Rebonding shall be limited to not more than one rebond attempt at any single bond pad location.

d) Rebonding shall be limited to level I, II and III devices only. Rebonding of level IV (class A type) devices shall not be permitted.

3.8 Performance Capabilities

The integrated circuits delivered to this specification shall be designed to be capable of meeting the environmental requirements specified in Table II. The manufacturer need not perform these tests specifically for the contract or specification, but shall provide data which demonstrates the ability of the integrated circuits to pass the environmental tests. The data shall have been generated on devices from the same generic family as the circuits being supplied to this specification, and the package configuration shall be the same as for the delivered parts. (i.e., Flat Pack, TO-100, etc.).

3.9 Quality and Reliability Assurance Program Plan

The manufacturer shall establish and implement a Quality and Reliability Assurance Program Plan that meets the intent of MIL-M-38510, Appendix A. Submission of the program plan to the procuring activity shall not be a requirement of this specification; however, the program plan shall be maintained by the manufacturer and shall be available for review by the procuring activity.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for Inspection

Unless otherwise specified in the contract or purchase order, the manufacturer is responsible for the performance of all inspection requirements specified herein. Except as otherwise specified, the manufacturer may utilize his own facilities or any commercial laboratory acceptable to the procuring activity. The procuring activity may, at its discretion, perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements.

4.1.2 Inspection at Point of Delivery

The procuring activity may, at its discretion, reinspect any or all of the delivered parts. (Excluding Group B destructive samples as defined by MIL-STD-883). All parts found to be defective and/or lacking specified documentation (such as test documentation) may be returned to the manufacturer at the manufacturer's expense.

4.1.3 Inspection Records

The manufacturer shall maintain a reliability data and records library. This library shall have on file, for review by the procuring activity, records of examination, qualification test results, variables data (when required) and all other pertinent data generated on devices manufactured to this specification.

4.1.4 Control of Procurement Sources

The manufacturer shall be responsible for assuring that all supplies and services conform to this specification, the detail specification and the manufacturer's procurement requirements.

4.1.4.1 Manufacturer's Receiving Inspection

Purchased supplies shall be subjected to inspection after receipt as necessary to assure conformance to contract requirements. In selecting sampling plans, consideration shall be given to the controls exercised by the procurement source and evidence of sustained quality conformance.

4.1.4.2 The manufacturer shall provide procedures for withholding from use all incoming supplies pending completion of required tests or receipt of necessary certification or test records and their evaluation.

4.1.4.3 The manufacturer shall initiate corrective action with the procurement source depending upon the nature and frequency of receipt of nonconforming supplies.

4.1.5 Procuring Activity Quality Assurance Representative

The procuring activity, may, at its discretion, place quality assurance representatives in the manufacturer's plant as deemed necessary to assure conformance to contract requirements in any non-proprietary phase of design, fabrication, processing, inspection, testing, and reliability of the integrated circuits being produced. The manufacturer shall provide reasonable facilities and assistance for the safety and convenience of such personnel in the performance of their duties. Inspection and test procedures shall be made available for review by the quality assurance representative.

4.2 Qualification and Quality Conformance Inspection

4.2.1 Qualification

Manufacturer's qualification shall be based on compliance with the established reliability test program requirements of paragraph 4.2.1.1 herein. The manufacturer may, at his discretion, substitute the qualification test plan of paragraph 4.2.1.2 in order to establish initial qualification. However, the substitution of parapraph 4.2.1.2 does not relieve the manufacturer from the responsibility of establishing an in-house reliability evaluation program as defined by paragraph 4.2.1.1.

4.2.1.1 Established Reliability Test Program

The manufacturer shall have an established and well defined in-house reliability program. This program shall be so designed as to demonstrate that the manufacturer's product is capable of meeting, as a minimum, the environmental and minimum life requirements listed in Table I herein. The reliability program may be modeled after the test procedure of Table I or it may take the form of a step-stress testing program similar to that defined by MIL-STD-883, Method T5006. The program shall be on-going in nature; that is, at specified intervals the manufacturer shall randomly select product that is representative of current production techniques, and subject the devices to the specified tests. Sampling shall be done on each generic family.

4.2.1.2 Qualification Test Program

In lieu of meeting the requirements of 4.2.1.1, the manufacturer may establish qualification by performing an initial, one-time qualification test in accordance with Table I herein. Qualification testing shall be performed on each generic family supplied to this specification. Upon successful completion of the qualification program, the manufacturer shall remain qualified for a period not to exceed 12 calendar months. Continued qualification shall then be based on compliance with the requirements of paragraph 4.2.1.1.

4.2.1.3.1 Procedures and Definitions

4.2.1.3.1 Sampling Procedure

Device selection for the qualification procedure of 4.2.1.1 or 4.2.1.2 shall be based on a random sampling technique. Testing shall be done on a mixture of device types that adequately represent the entire generic family. The following is a recommended mix ratio:

Gates	:	65% of total sample
Flip-Flops	:	25% of total sample
MSI	:	10% of total sample

4.2.1.3.2 Generic Family

Electrically and structurally similar devices shall be said to comprise a generic family (e.g., TTL) if they meet the following criteria:

a) Are designed with the same basic circuit-element configuration such as TTL, DTL, ECL, or Linear, and differ only in the number or complexity of specified circuits which they contain.

b) Are designed for the same supply, bias and signal voltage, and for input/output capability with each other under an established set of loading rules.

c) Are enclosed in housing (packages) of the same basic construction (e.g., hermetically sealed flat packages, dual-in-line cermaic, dual-in-line plastic) and outline, differing only in the number of active housing terminals included and/or utilized.

4.2.2 Quality Conformance Inspection (Lot Inspection)

When specifically called out on the purchase order or contract, the manufacturer shall perform the lot qualification inspections, Group B and/or Group C in Table II.

4.2.2.1 Lot Acceptance Sampling

Statistical sampling for Group B and/or Group C lot acceptance inspections shall be in accordance with MIL-M-38510 Table B-1.

Group B samples shall be selected from sub-lots that have successfully completed all of the 100% processing steps, up to and including Group A Lot Acceptance, specified on the applicable process flow chart.

4.2.2.2 Resubmission/Failed Lots

Where a lot fails any one of the sub-group qualification requirements of Table II, it may be resubmitted a maximum of one time for qualification to that particular sub-group provided an analysis is performed to determine the failure mechanism for each reject device in the sub-group, and that it is determined that the failures are due to one of the following:

a) Testing error resulting in electrical damage to devices,

b) A defect that can effectively be removed by rescreening the lot,

c) Random defects which do not reflect poor basic device designs or poor workmanship.

4.2.2.3 Early Shipments

When lot qualification inspection is being performed for a specific contract or purchase order, the accepted Group A devices that are awaiting shipment pending successful completion of Group B and/or Group C, shall be stored in the MACH IV bonded locker. Under no circumstances shall such parts be shipped prior to the successful completion of the Group B tests.

4.2.2.4 Group B Test Data

All data generated by Group B and/or Group C testing shall accompany the initial shipment of devices. This data shall consist, at a minimum, of the following:

a) Attributes data for Group B. Endpoints for the subgroups are visual per the applicable MIL-STD-883 test method.

b) Variables data for Group C subgroups 1, 2, 4, and 5. Endpoints for these subgroups shall be "critical eletrical parameters" only. These parameters are designated by an asterisk (*) on the detail specification.

4.2.2.5 Procedure In Case Of Test Equipment Failure Or Operator Error

Where an integrated circuit is believed to have failed as a result of faulty test equipment or operator error, the failure shall be entered in the test record which shall be retained for review along with a complete explanation verifying why the failure is believed to be invalid. If it is determined that the failure is invalid, a replacement integrated circuit from the same inspection lot may be added to the sample. The replacement integrated circuit shall be subjected to all those tests to which the discarded integrated circuit was submitted prior to its failure, and any remaining specified test to which the discarded integrated circuit was not subjected prior to its failure.

4.3 Quality Assurance Processing, Methods and Procedures

This section establishes the test methods and conditions to be used for the 100% processing (screening) requirements specified by the applicable process flow chart.

4.3.1 Precap Visual Inspection

Each microcircuit shall be required to pass the appropriate precap visual inspection defined as follows. Precap Lot Acceptance shall be per paragraph 4.6.

4.3.1.1 Level II devices shall be visually inspected in accordance with the criteria listed in Section 6.1.3 of this specification. Inspection procedures and equipment requirements shall be as defined in MIL-STD-883.

4.3.1.2 Level I and III devices shall be visually inspected in accordance with MIL-STD-883, Method 2010.1, Condition B as defined by Revision Notice 2 dated November 20, 1969. (See Note 6.1.2.)

4.3.1.3 Level IV devices (designated for NASA type applications) shall be visually inspected in accordance with MIL-STD-883, Method 2010.1, Condition A as defined by Revision Notice 2 dated November 20, 1969. (See Note 6.1.1.)

4.3.2 Stabilization Bake

The purpose of this test is to determine the effect on microelectronic devices of baking at elevated temperatures without electrical stress applied. Test shall be performed in accordance with MIL-STD-883, Method 1008, Condition C.

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4.3.3 Thermal Shock

The purpose of this test is to determine the resistance of the device to sudden exposure to extreme changes in temperature. Test shall be performed in accordance with MIL-STD-883, Method 1011, Condition A.

4.3.4 Temperature Cycle

This test is conducted for the purpose of determining the resistance of a part to exposures at extremes of high and low temperatures, and to the effect of alternate exposures to these extremes, such as would be experienced when equipment or parts are transferred to and from heated shelters in arctic areas. Test shall be performed in accordance with MIL-STD-883, Method 1010, Condition C, minimum of 10 cycles.

4.3.5 Mechanical Shock

The shock test is intended to determine the suitability of the devices for use in electronic equipment which may be subjected to moderately severe shocks as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation, or field operation. Test shall be performed in accordance with MIL-STD-883, Method 2002, Condition B, five blows minimum.

4.3.6 Centrifuge

The centrifuge test is used to determine the effects on microelectronic devices of a centrifugal force. This test is designed to indicate structural and mechanical weaknesses not necessarily detected in shock and vibration tests. Test shall be performed in accordance with MIL-STD-883, Method 2001, Condition E.

4.3.7 Fine Leak Test

Each integrated circuit shall be subject to a fine leak test in accordance with paragraph 4.3.7.1 or 4.3.7.2. The method shall be optional providing it is consistent with and capable of detecting the specified leak rate of the applicable process flow chart.

4.3.7.1 Helium Leak Test

Helium leak test shall be performed in accordance with MIL-STD-883, Method 1014, Condition A. Helium bomb pressure shall be 30 psig maximum, bomb time shall be 4 hours minimum.

4.3.7.2 Radiflo Leak Test

Radiflo leak test shall be performed in accordance with MIL-STD-883, Method 1014, Condition B. Krypton 85 bomb pressure and dwell time are a function of the radioactivity level and shall be selected so as to conform to the equations given in Condition B.

4.3.8 Gross Leak Test

Each integrated circuit shall be subjected to the appropriate gross-leak test of paragraphs 4.3.8.1 or 4.3.8.2. The manufacturer may, at his option, perform gross-leak testing after the Set I Final Electrical Tests of paragraph 4.3.9.

4.3.8.1 Glass to metal hermetic flat packs shall be tested in accordance with MIL-STD-883, Method 1014, Condition C, Step 2. Units will be bombed 4 hours minimum at 30 psi in FC-78. Units will then be immersed in FC-40 at +125°C ±5°C for 20 seconds minimum and observed for one large bubble or a continuous stream of small bubbles.

4.3.8.2 Glass to glass (ceramic) hermetic package shall be tested in accordance with MIL-STD-883, Method 1014, Condition C, Step 1.

4.3.9 Final Electrical Test (Set I)

Each integrated circuit shall be required to pass the electrical requirements of Subgroup 1 of the detail specification (DC @ +25°C). The manufacturer shall also perform such additional testing necessary to assure the parts will meet the temperature extreme limits.

4.3.10 Burn-In

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The burn-in screen is performed for the purpose of eliminating marginal devices, those and early life failures evidenced as time and stress dependent. Test shall be in accordance with MIL-STD-883, Method 1015, Condition D or E at 125 ± 5°C for 168 hours minimum. The bias shall be removed from the devices prior to their return to 25°C. (See Note 6.3)

4.3.11 Final Electrical Test (Set II)

Each integrated circuit shall be required to pass the electrical requirements of the detail specifications. The following tests shall be performed as a minimum: d-c at maximum and minimum rated temperatures, and switching parameters at 25°C.

The manufacturer may, when deemed necessary, elect to perform additional electrical testing over and above the requirements stated herein.

4.3.12 Radiographic Inspection (X-ray)

Test shall be performed in accordance with MIL-STD-883, Method 2012. The integrated circuit shall be required to pass a radiographic inspection to these requirements. In addition, the acceptance criteria shall meet, as a minimum, the requirements of NASA MSFC specification MSFC-STD-355.

4.3.13 External Visual Inspection

The purpose of this examination is to verify that materials, construction, marking, and general workmanship are as specified. Examination shall be in accordance with MIL-STD-883, Method 2009.

4.4 Group A Lot Acceptance

Each lot of integrated circuits shall be sampled by Quality Control to the LTPD's given below:

GROUP A ACCEPTANCE

SUBGROUP	LTPD LEVEL I & II	LTPD LEVEL III & IV
Subgroup 1 25"C, d-c	7%	5%
Subgroup 2 +125"C, d-c	7%	5%
Subgroup 3 −55"C, d-c	7%	5%
Subgroup 4 Switching Speed @ +25"C	15%	10%

NOTE: Functional tests included in d-c tests.

TABLE I
MANUFACTURERS QUALIFICATION PROCEDURE

TEST	MIL-STD-883 METHOD	CONDITIONS	LTPD
Subgroup 1			
Physical Dimensions Visual and Mechanical	2008	Condition A & B	15
Subgroup 2†			
Solderability	2003		15
Subgroup 3†			
Thermal Shock	1011	Condition B	
Temperature Cycling	1010	Condition C	
Moisture Resistance	1004	Omit step 7B and Initial Conditioning	
Critical Electrical Parameters	5004	25°C, DC	15
Subgroup 4‡			
Mechanical Shock	2002	Condition B	
Vibration Variable Freq.	2007	Condition A	
Constant Acceleration	2001	Condition E	
Critical Electrical Parameters	5004	25°, DC	15
Subgroup 5†			
Lead Fatigue	2004	Condition B2	
Fine Leak	1014	Condition A, Per Para. 4.3.7 Herein	
Gross Leak	1014	Condition C, Per Para. 4.3.7 Herein	15
Subgroup 6†			
Salt Atmosphere	1009	Condition A, Omit Initial Conditioning	15
Subgroup 7‡			
Storage Life	1008	150°C, 1000 Hrs. Minimum	
Critical Electrical Parameters	5004	25°C, DC	10
Subgroup 8‡			
Operating Life	1005	125°C, 1000 Hrs. Minimum Return to 25°C without bias	
Critical Electrical Parameters	5004	25°C, DC	10
Subgroup 9†			
Bond Strength			10 devices not
a. Thermocompressions	2011	Condition B, D	greater than 1%
b. Ultrasonic	2011	Condition B, D	defective

†Visual and/or hermetic end points hence electrical or visual rejects may be used. Reference MIL-STD-883. Method 5005, Para. 3.4.

‡Electrical end points only.

TABLE II
LOT ACCEPTANCE/PERIODIC QUALIFICATION TEST
(GROUP B/GROUP C)

GROUP B

TEST	MIL-STD-883 METHOD	CONDITIONS	LTPD LEVEL I & II	LTPD LEVEL III & IV
Subgroup 1				
Physical Dimensions Visual and Mechanical	2008	Condition A	15	10
Subgroup 2				
Marking Permanency	2008	Condition B, para. 3.2.1		
Visual and Mechanical	2008	Condition B per applicable detail specification		
Bond Strength	2011	Condition B or D 2 grams for Au bonds 1 gram for Al bonds	15	5
Subgroup 3†				
Solderability	2003		15	10
Subgroup 4†				
Lead Fatigue	2004	Conditions B2		
Fine Leak	1014	Condition A, per para. 4.3.7 of this spec.		
Gross Leak	1014	Condition C, per para. 4.3.8 of this spec.	15	10

GROUP C

Subgroup 1‡				
Thermal Shock	1011	Condition B		
Temp. Cycle	1010	Condition C		
Moisture Resistance	1004	Omit Initial Cond. & step 7B		
Critical Electrical Parameters	5004	25°C, DC	15	10
Subgroup 2‡				
Mechanical Shock	2002	Condition B		
Vibration Variable Freq.	2007	Condition A		
Constant Acceleration	2001	Condition E		
Critical Electrical Parameters	5004	25°C, DC	15	10
Subgroup 3				
Salt Atmosphere	1009	Condition A Omit Initial Conditioning	15	10
Subgroup 4‡				
High Temp. Storage	1008	150°C, 1000 Hrs.		
Critical Electrical Parameters	5004	25°C, DC	10	7
Subgroup 5‡				
Operating Life Test	1005	125°C, 1000 Hrs. Minimum		
Critical Electrical Parameters		25°C, DC	10	7

†Visual and/or hermetic end points hence electrical or visual rejects may be used. Reference MIL-STD-883. Method 5005, Para. 3.4.

‡Electrical end points only.

4.5 Certification

The manufacturer shall include a certificate of compliance with each shipment of parts. This certificate shall indicate that all specified tests and requirements of this specification have been made or met, and that the lot of devices (identified by lot and/or batch number) are acceptable. The certificate shall bear the name and signature of the manufacturer's Quality Control representative, the date of acceptance or signing, and any pertinent notes as applicable.

4.6 Precap Lot Acceptance

After each precap inspection the lot of devices shall be sampled by quality control and inspected for the specified visual criteria. The sampling plan shall be:

40X criteria – 1.0% AQL
100X criteria – 1.0% AQL

2

5.0 PREPARATION FOR DELIVERY

5.1 Final Visual Shipping Inspection

Each lot of microcircuits and its associated documentation shall be sampled by Quality Control and visually inspected for the following:

a) Scratched, nicked or bent leads

b) Damaged header (packages)

c) All test data specified in section 4.0

d) Certificate of Compliance as specified in section 4.0

e) All other pertinent documentation required and specified by this specification.

5.2 Packing Requirements

Parts shall be packed in containers of the type, size, and kind commonly used which will ensure acceptance by common carriers and safe delivery at the destination and in accordance with MIL-M-55565, Level C. The containers shall be clearly marked with manufacturer's name or symbol. The manufacturer's FEDERAL SUPPLY CODE FOR MANUFACTURER (FSCM) shall be included if applicable.

5.3 Preservation and Package Identification

The package shall be marked with the following:

The country of origin if other and U.S.A.
Procuring activity parts number
Purchase order number
Material nomenclature
Quantity
Lot number
Date code

This information shall appear on the label or shall be directly marked on each container. Method is optional.

6.0 NOTES

6.1 Precap Visual Method 2010.1

The following precap criteria may be in conflict with the circuit design topology and construction techniques of some microcircuit manufacturers. Where such a conflict does exist, the inspection criteria listed herein may be waived. (Reference paragraph 3.0 of MIL-STD-883, Method 2010.1)

6.1.1 Preseal Visual Inspection, Test Condition A (Level IV)

6.1.1.1 Paragraph 3.1.6.3 is clarified as follows:

When the criteria of 3.1.6.3(b) is in conflict with 3.1.6.3(a), the criteria of 3.1.6.3(a) shall take precedence. (Note: This clarification is with respect to die symmetry only.)

6.1.1.2 Paragraphs 3.1.1.1(a) and 3.1.1.2(a) are clarified as follows:

"Any scratch or void in the metallization that leaves less than 50 (75) percent of the original metal width undisturbed" shall be rejected. When a bi-metallization system is used (e.g. Moly-Gold) the scratch or void must penetrate entirely through the gold and expose moly or oxide.

6.1.1.3 Paragraph 3.1.4.3(c) delete: (Applicable to gold ball bonds only) "Bonds in the fillet area (or the point where metallizations exits from the bonding pad) which reduces the major distance between the bond periphery and edge of fillet to less than 50 percent of the narrowest normal width of the interconnecting metallization."

6.1.2 Preseal Visual Inspection, Test Condition B (Levels I & III)

2

6.1.2.1 Paragraph 3.2.1.7(a) delete the 40 percent perimeter requirement. (Selected devices only)

6.1.2.2 Paragraph 3.2.4.3(a) substitute the following criteria: "Bonds placed so that the wire exiting from the bond appears to come closer than two wire diameters to another wire, bonding pad, or package land, after a distance of 10 mils from the die surface.

6.1.2.3 Paragraph 3.2.4.3(c) delete. "Bonds in the fillet area (or the point where metallizations exits from the bonding pad) which do not exhibit a line of undisturbed metallization visible between the periphery of the bond and at least one side of the fillet (or one side of the connecting stripe) when viewed from above."

6.1.3 Preseal Visual Inspection, Test Condition B (Level II)

The same comments of 6.1.2 are applicable here plus the following:

6.1.3.1 Paragraph 3.2.1.1(a) change to read as follows: "Scrathces or voids in metallization exposing oxide for more than 50 percent of the lead width or alternately, a scratch or void greater than 0.5 mils in length exposing oxide."

6.1.3.2 Paragraph 3.2.1.1(b) change to read as follows:

"Any scratch in the metallization over an oxide step which leaves less than 50 percent of the original metal width undisturbed."

6.1.3.3 Paragraph 3.2.1.2(b) change to read as follows:

"Any void in the metallization over an oxide step which leaves less than 50 percent of the remaining metal undisturbed."

6.1.3.4 Paragraph 3.2.3(d) delete.

"Any crack which exceeds 1.0 mil in length inside the scribe grid or scribe line that points toward active metallization or circuit area."

6.1.3.5 Paragraph 3.2.6.1(b) change to read as follows:

"Attached gold or silicon material that appears to bridge any two unpassivated metallization areas, two package leads, or any lead to package metallization."

6.2 Interconnections

Circuit intraconnections (metallization pattern) shall be designed so that no properly fabricated connection shall experience a current density greater than 5×10^5 amperes/cm2, including allowances for worst case conductor composition, normal production tolerances on design dimensions, and nominal thickness at critical areas such as contact windows.

6.3 Burn-in Method 1015

Condition D parallel excitation or Condition E ring oscillator burn-in circuits will be used. The requirement to return the device to 25°C room ambient temperature with bias still applied should be omitted. Indications are that for most saturated logic integrated circuits the high temperature bake after bias has been removed does not allow defective devices to recover and become good.

6.4 Salt Atmosphere Test, Method 1009.

Where package design consideration necessitate (such as .75" tip-to-tip metal flat packs), there may be a conformal coating applied prior to the salt atmosphere test.

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APPENDIX A

PROCESS CONTROL SYSTEM

INTEGRATED CIRCUITS PROCESS CONTROL

The integrated circuits industry has had over seven years experience in manufacturing and represents a high volume, mass production sector of electronics. We have overcome the usual new product growing pains and learned a great deal about process control systems from our experience. This article presents the philosophy and the basic elements of a process control system which has been found to be the most practical one for integrated circuits manufacturing. It should also be applicable to any semiconductor process which must produce devices for a high reliability market.

Integrated circuits were originally developed for the aerospace market and these are still the volume users. Hundreds of thousands of integrated circuits have already been delivered for use in Minuteman and Apollo alone. At the same time, the high volume commercial and consumer market for integrated circuits is developing very rapidly. Although most of the integrated circuits from a given manufacturer are built on a single production line, there are many different types and families: digital, linear, flip flops, choppers, gates, buffers, amplifiers, double epitaxial, monolithic, hybrids, TTL, DTL, ECL—hundreds of possibilities.

The key to success in today's integrated circuits business appears to be an efficient and effective process/product control system.

PRODUCT CONTROL VS. PROCESS CONTROL

Although it is not universally understood, *product* control is not the same as *process* control. They not only have different means, but their ends are entirely different. True, under the proper conditions, they can be interfaced and made more efficient, but let us first define the terminology.

PRODUCT CONTROL

Product control is the inspection and sorting of material (product) to cull unacceptable material from the acceptable. It is the age-old task of inspection, screening, detailing, or culling. With a state-of-the-art product such as integrated circuits, this inspection will usually take the form of go-no-go checking for various defects. The end result of product control is to eliminate from succeeding steps of the process that material which the preceding steps of the process have not constructed properly. The basic element of a product control system is where the inspection station is removing most of the product which was processed improperly by the preceding manufacturing operation.

It will be noted that this inspection has no control over the *process—only the product*. If the manufacturing operation should happen to start producing 100% bad product, the inspection station would remove this product, but would not correct the basic problem.

If the results of the inspection station, in the form of yield (or loss) data is monitored, analyzed, and compared to a standard set of circumstances, action can be taken to correct any degradation of the manufacturing operation. This feedback of information effects a degree of *process control* i.e., a control over the process which is not directly concerned with removing defective product.

The feedback of product control results for process control purposes helps achieve control over processes.

Product control in the manufacturing area is composed of:

1) Manufacturing Inspection
2) Quality Control Lot Acceptance Following Manufacturing Inspections.

1. Manufacturing Inspection

This inspection is performed by production personnel to go-no-go defect criteria. Even in this least severe level of product control, the closed loop feedback is utilized. The medium for this control is the product yield report and process control management system (PCMS), which has daily and weekly management, engineering, and quality control visibility.

Examples of these controls are diffusion, bar inspection, slice electrical probe, pre-encapsulation, hermetic seal, and electrical inspections performed in the manufacturing process.

2. Quality Control Lot Acceptance Following Manufacturing Inspection

In areas more critical in nature, the manufacturing inspection described in (1) is sometimes followed by Lot Acceptance. Here, decisions are made on lots of inspected product with regard to engineering specifications and predetermined quality levels.In this medium of control, feedback is two-fold: (1) Rejected lots are immediately identified for attention and manufacturing, engineering, and quality control are alerted as to whether process or inspection changes may have taken place, (2) PCMS shows trends of the quality control results and is distributed weekly to all levels of department management. Percentages are statistically compared to past averages and significant points are noted and corrective action implemented.

Examples of such control points are QC lot acceptance at epitaxial, bar inspection, pre-encapsulation, hermetic seal and electrical testing.

It should be pointed out that this "Product Control" concept is also an Inspection Control concept. The inspectors which are checked by a lot acceptance get instant feedback if the quality of their inspection degrades. Also, through the use of reject analysis and yield reporting, excessive losses are noted and thus both acceptable and rejectable material is monitored.

PROCESS CONTROL

Process control is the activity which controls the process itself and is not directly concerned with removing the defective product, but in preventing the manufacture of defective product which aids the subsequent product controls. It was noted previously that even in the case of pure *Product Control*, some process control can be effected by the proper use of feedback tools.

In integrated circuits manufacturing at Texas Instruments, *Process Control* is provided by the following:

1) Quality Control Surveillance Points During Manufacture
2) Engineering Evaluation of Manufacturing Process
3) Manufacturing Controls
4) Failure Analysis of Discrepant Devices

1. Quality Control Surveillance Points During Manufacture

Process Controls examines the manufacturing process to point out the problem areas. For example: If thirty operators are bonding, we inspect products from all thirty operators and point out the worst three bonders to the manufacturing supervisor daily. This concentrates the supervisor's effort on the quality problem operator each day. This type of control is called operator control.

A control where the worst machine or machines are pinpointed for corrective action by repair and maintenance personnel is called machine control. Examples of such controls are: $\bar{X}$–R chart control of diffusion furnaces, visual surveillance of product from each mounting operator, bond strength tests on bonded Integrated Circuits, hermetic seal checks on lid welders.

2. Engineering Evaluation of Manufacturing Process

Engineering maintains sample or pilot analysis at several critical points of manufacture. Here, electrical parameters are measured on a lot by lot basis to maintain control at that point. An example of this is the analysis performed in diffusion to control this portion of the manufacturing process.

3. Manufacturing Controls

Regular controls by manufacturing for operator performance, line balance, inventory control, and line comparison enhance the quality of the device.

4. Failure Analysis of Discrepant Devices

Another portion of the feedback loop is through the analysis of failed devices. Regular life testing with failure analysis of test failures is performed on representative device series. In addition, device failures from selected points in the process are given to the failure analysis lab on a routine basis. By this media, *Product* and *Process Controls* can be adjusted to correct mechanisms which might not be discovered until actual application of the devices.

An analysis of the complete QC process control system is shown in the attached flow charts. These charts describe the QC Process Control System and a brief description of each control point.

The PCMS is a computerized report of the control points on a weekly basis. These control points have their trends analyzed by comparing the current percentage to past averages and calculating significant differences. Points analyzed as significantly different are further detailed as to exact defect descriptions. These points are then analyzed and corrective action developed as necessary. This weekly analysis is circulated to all levels of department management. This reporting system plus the immediate feedback which occurs "on-line" provides an effective follow-up scheme.

It should be noted that the details of this system are flexible and not essential to the basic philosophy of a composite control system. As experience is gained in the various inspection areas and as process improvements are made, it will be found advantageous to suitably modify the system to keep pace with these changes. As time passes, sample sizes will be changed; inspection points will be added and deleted; defect criteria will be made less subjective, and new defect criteria will be added to the inspection procedure. But none of these affect the basic philosophy of the product/process control system.

ADVANTAGES OF THE SYSTEM

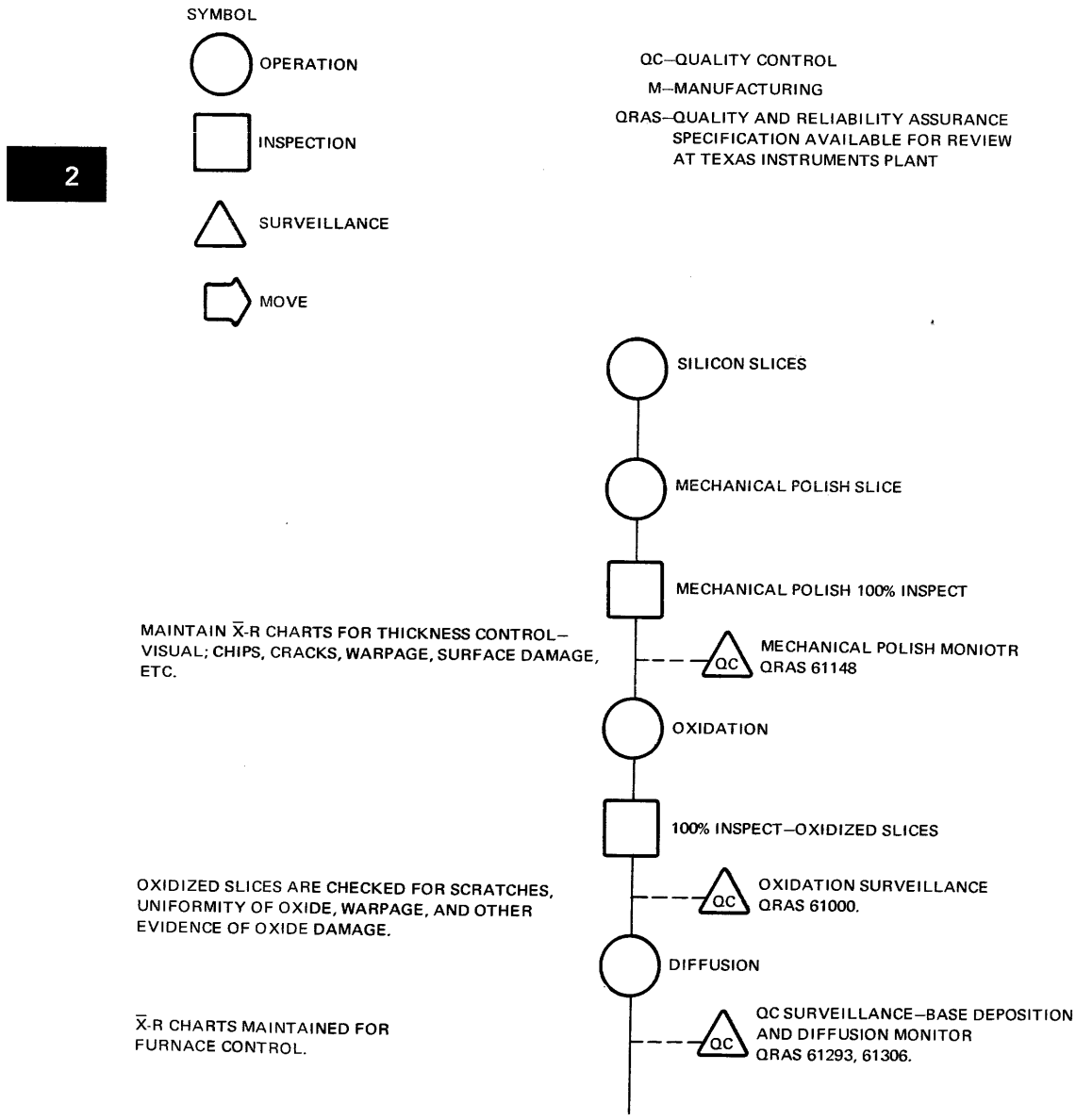
1) It is a flexible system easily adapted to changes brought about by technological improvements or by changes dictated by the system itself.
2) It is a cost optimized system in which the process or product can be stopped before unwarranted labor is expended. In addition, the system calls attention to the reason for defective product so that corrective action can be implemented.
3) The same general system can be utilized for different degrees of maturity of a product and for different degrees of criticality with regard to product requirements.
4) It combines the advantages of both the product and process control concepts.
5) There is maximum utilization of data by closing all the feedback loops with corrective action.

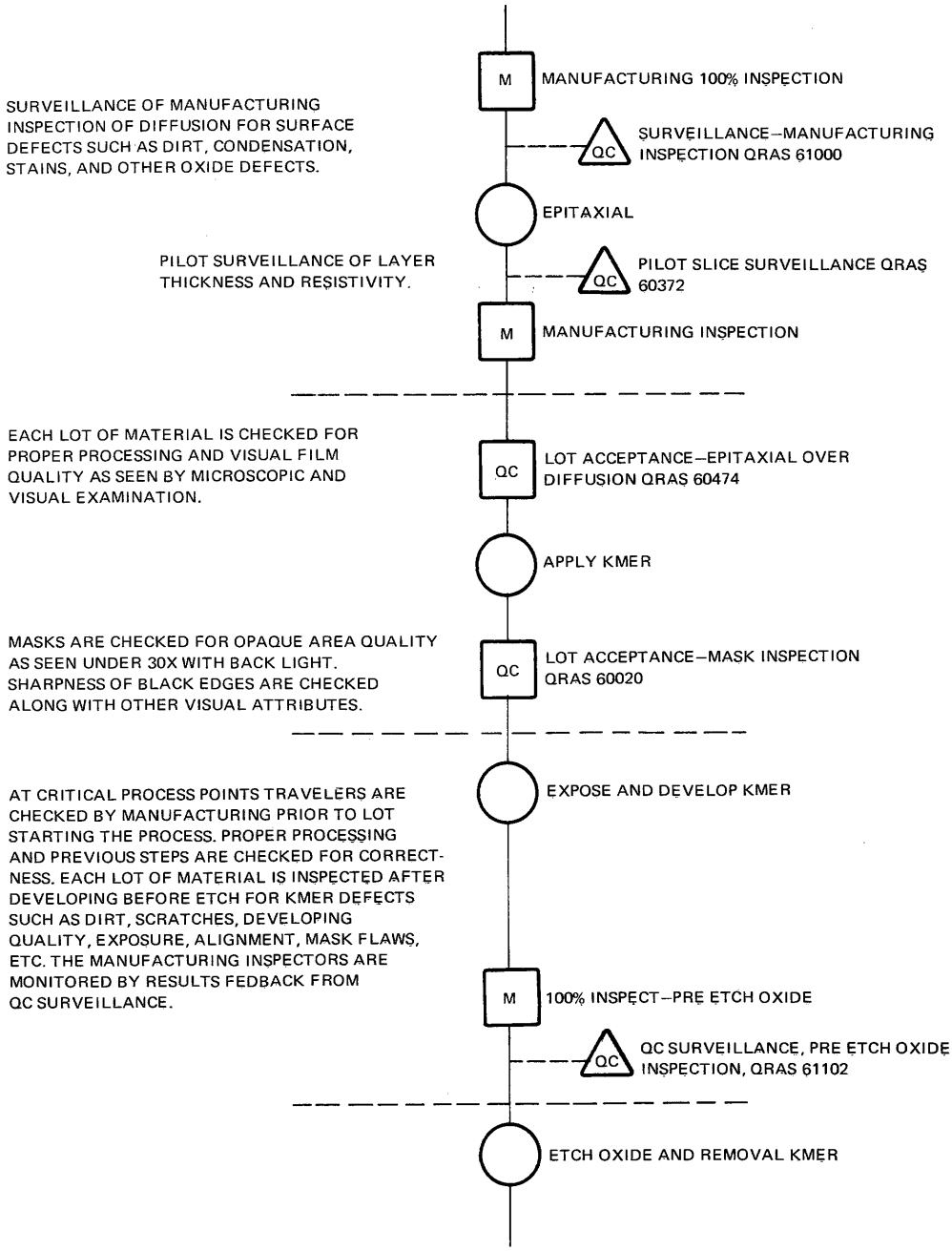
SUMMARY

Using the various elements described above to develop a composite control system for an integrated circuits process results in maximizing the efficiency of inspection and utilization of inspection data. In particular, the system offers a practical solution for interfacing these following features:

Product Control through 100% inspection and sorting.

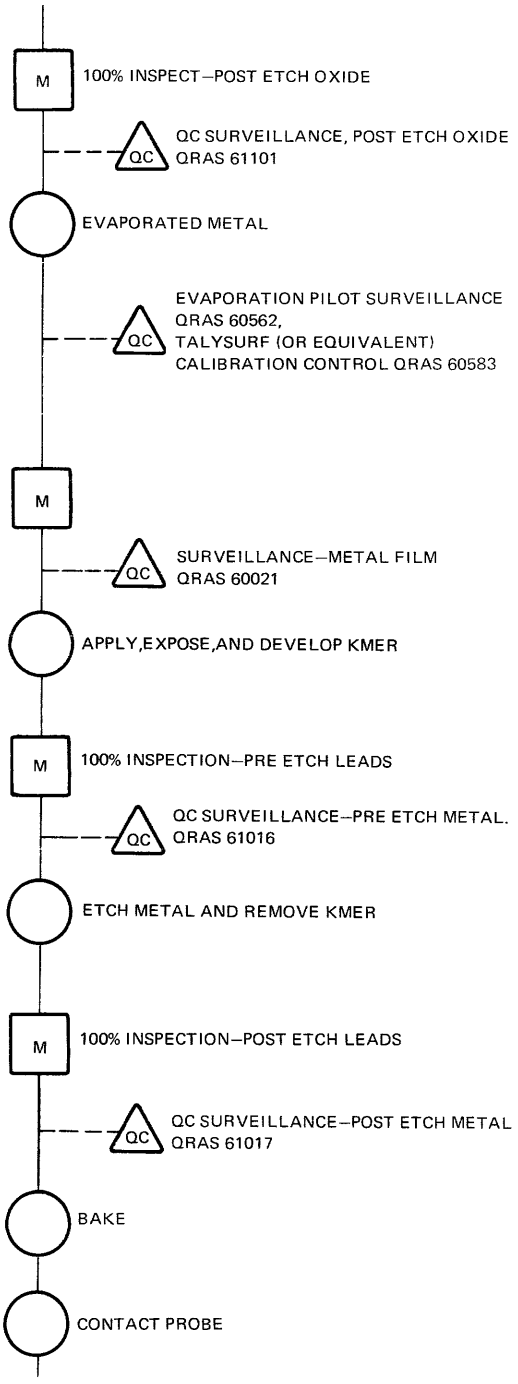
Process Control through feedback of inspection data into the process.


SYMBOL
OPERATION
INSPECTION
SURVEILLANCE
MOVE
QC–QUALITY CONTROL
M–MANUFACTURING
QRAS–QUALITY AND RELIABILITY ASSURANCE SPECIFICATION AVAILABLE FOR REVIEW AT TEXAS INSTRUMENTS PLANT
SILICON SLICES
MECHANICAL POLISH SLICE
MECHANICAL POLISH 100% INSPECT
MAINTAIN X̄-R CHARTS FOR THICKNESS CONTROL–VISUAL; CHIPS, CRACKS, WARPAGE, SURFACE DAMAGE, ETC.
QC
MECHANICAL POLISH MONIOTR QRAS 61148
OXIDATION
100% INSPECT–OXIDIZED SLICES
OXIDIZED SLICES ARE CHECKED FOR SCRATCHES, UNIFORMITY OF OXIDE, WARPAGE, AND OTHER EVIDENCE OF OXIDE DAMAGE.
QC
OXIDATION SURVEILLANCE QRAS 61000.
DIFFUSION
X̄-R CHARTS MAINTAINED FOR FURNACE CONTROL.
QC
QC SURVEILLANCE–BASE DEPOSITION AND DIFFUSION MONITOR QRAS 61293, 61306.


M
MANUFACTURING 100% INSPECTION
SURVEILLANCE OF MANUFACTURING INSPECTION OF DIFFUSION FOR SURFACE DEFECTS SUCH AS DIRT, CONDENSATION, STAINS, AND OTHER OXIDE DEFECTS.
QC
SURVEILLANCE–MANUFACTURING INSPECTION QRAS 61000
EPITAXIAL
PILOT SURVEILLANCE OF LAYER THICKNESS AND RESISTIVITY.
QC
PILOT SLICE SURVEILLANCE QRAS 60372
M
MANUFACTURING INSPECTION
EACH LOT OF MATERIAL IS CHECKED FOR PROPER PROCESSING AND VISUAL FILM QUALITY AS SEEN BY MICROSCOPIC AND VISUAL EXAMINATION.
QC
LOT ACCEPTANCE–EPITAXIAL OVER DIFFUSION QRAS 60474
APPLY KMER
MASKS ARE CHECKED FOR OPAQUE AREA QUALITY AS SEEN UNDER 30X WITH BACK LIGHT. SHARPNESS OF BLACK EDGES ARE CHECKED ALONG WITH OTHER VISUAL ATTRIBUTES.
QC
LOT ACCEPTANCE–MASK INSPECTION QRAS 60020
EXPOSE AND DEVELOP KMER
AT CRITICAL PROCESS POINTS TRAVELERS ARE CHECKED BY MANUFACTURING PRIOR TO LOT STARTING THE PROCESS. PROPER PROCESSING AND PREVIOUS STEPS ARE CHECKED FOR CORRECTNESS. EACH LOT OF MATERIAL IS INSPECTED AFTER DEVELOPING BEFORE ETCH FOR KMER DEFECTS SUCH AS DIRT, SCRATCHES, DEVELOPING QUALITY, EXPOSURE, ALIGNMENT, MASK FLAWS, ETC. THE MANUFACTURING INSPECTORS ARE MONITORED BY RESULTS FEDBACK FROM QC SURVEILLANCE.
M
100% INSPECT–PRE ETCH OXIDE
QC
QC SURVEILLANCE, PRE ETCH OXIDE INSPECTION, QRAS 61102
ETCH OXIDE AND REMOVAL KMER

EACH LOT OF MATERIAL IS INSPECTED BY MANUFACTURING AFTER OXIDE REMOVAL FOR OXIDE DEFECTS SUCH AS UNDERCUT, ALIGNMENT, INCOMPLETE OXIDE REMOVAL, DIRT, ETC.

THE MANUFACTURING INSPECTORS ARE MONITORED BY RESULTS FEDBACK FROM THE QC SURVEILLANCE.



2

THIS CHECK IS A SURVEILLANCE OF TESTING EVAPORATION PILOT SLICES TO DETERMINE METAL THICKNESS. PILOTS ARE DOUBLE CHECKED TWICE PER WEEK PER SHIFT FROM EACH EVAPORATOR. THE TALYSURF (OR EQUIVALENT) WHICH MEASURES METAL FILM THICKNESS IS CHECKED FOR CALIBRATION ONCE PER SHIFT USING STANDARDS.

SAMPLES ARE PULLED ONCE PER EVAPORATOR PER SHIFT FOR EFFECTIVENESS OF MANUFACTURING 100% INSPECTION. DEFECTS SUCH AS CONTAMINATION, SPLATTERING, FOREIGN PARTICLES, ETC, ARE MONITORED

EACH LOT OF SLICES IS INSPECTED AT METAL ETCH FOR DEFECTS SUCH AS MISALIGNMENT, OVER AND UNDER EXPOSURE, WRONG PATTERN, RESIST PEELING, ETC. THIS KMER INSPECTION IS PERFORMED BY MANUFACTURING.

THE MANUFACTURING INSPECTORS ARE MONITORED BY RESULTS FEDBACK FROM THE QC SURVEILLANCE.

EACH LOT OF MATERIAL IS INSPECTED BY MANUFACTURING AFTER METAL REMOVAL FOR DEFECTS SUCH AS INCOMPLETE METAL REMOVAL, LEADS TOUCHING SILICON OUTSIDE CONTACTS, MISALIGNMENT, PEELING LEADS, ETC.

THE MANUFACTURING INSPECTORS ARE MONITORED BY RESULTS FEDBACK FROM THE QC SURVEILLANCE.

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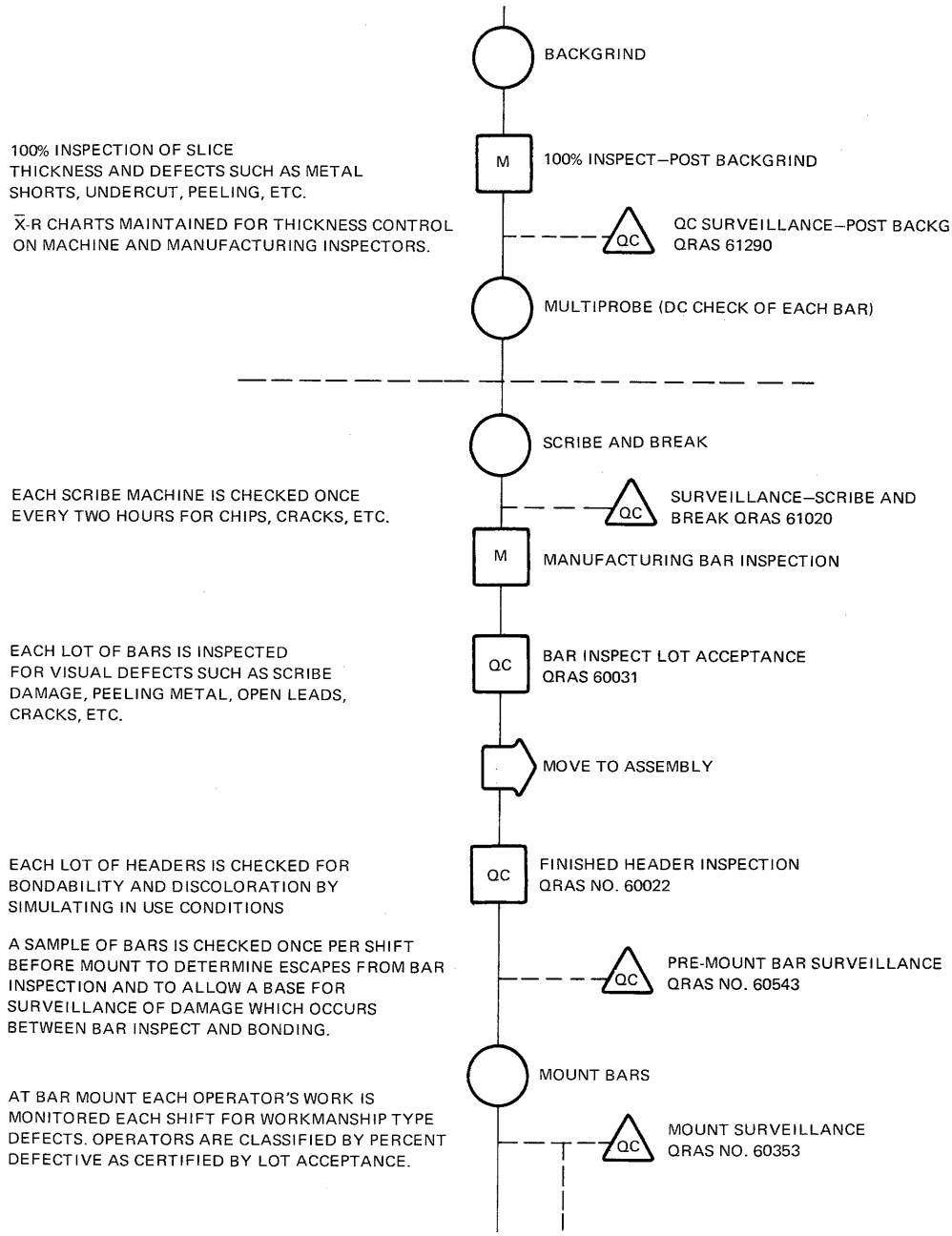
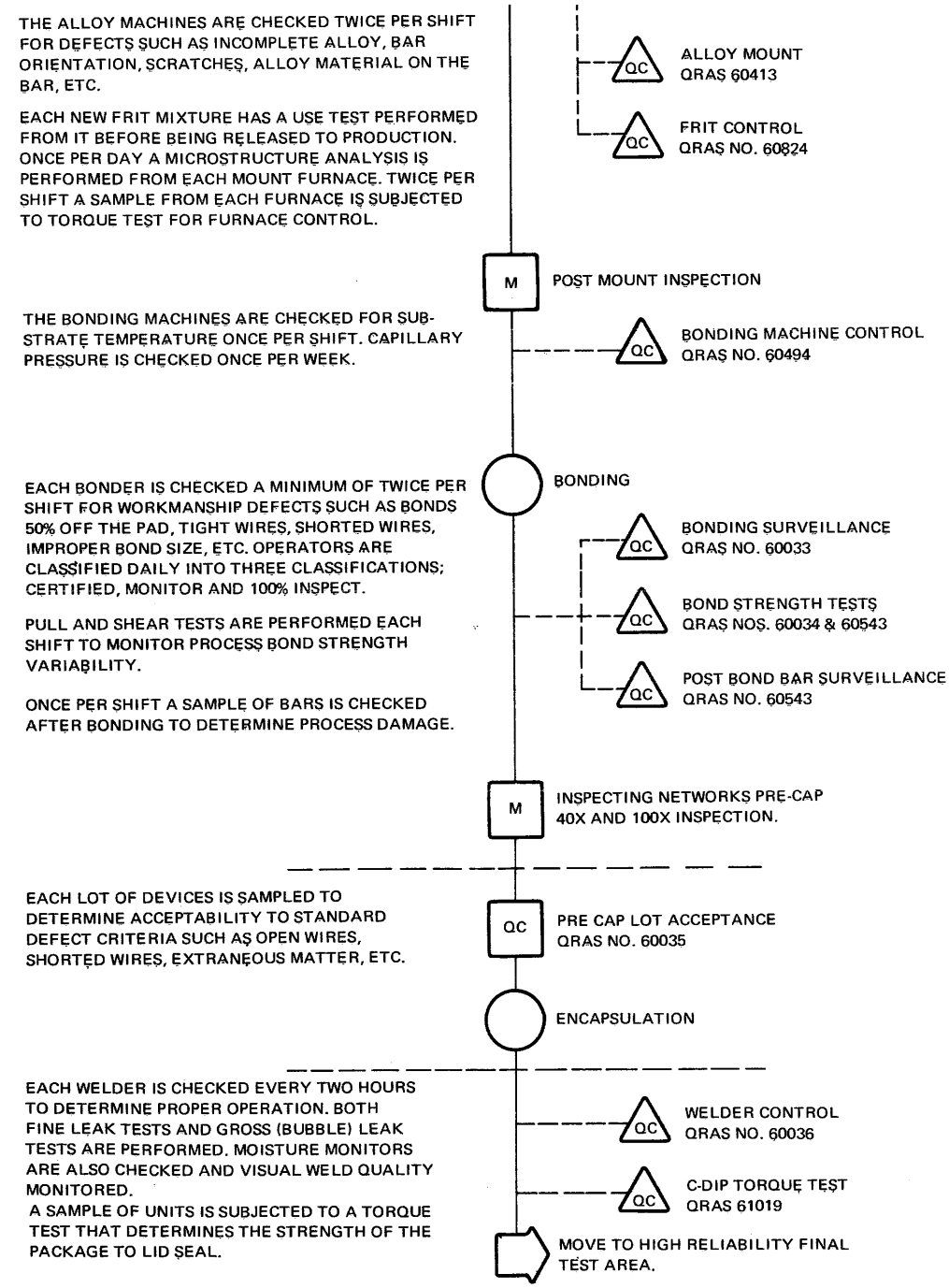

BACKGRIND
100% INSPECTION OF SLICE THICKNESS AND DEFECTS SUCH AS METAL SHORTS, UNDERCUT, PEELING, ETC.
X̄-R CHARTS MAINTAINED FOR THICKNESS CONTROL ON MACHINE AND MANUFACTURING INSPECTORS.
M
100% INSPECT–POST BACKGRIND
QC
QC SURVEILLANCE–POST BACKGRIND QRAS 61290
MULTIPROBE (DC CHECK OF EACH BAR)
SCRIBE AND BREAK
EACH SCRIBE MACHINE IS CHECKED ONCE EVERY TWO HOURS FOR CHIPS, CRACKS, ETC.
QC
SURVEILLANCE–SCRIBE AND BREAK QRAS 61020
M
MANUFACTURING BAR INSPECTION
EACH LOT OF BARS IS INSPECTED FOR VISUAL DEFECTS SUCH AS SCRIBE DAMAGE, PEELING METAL, OPEN LEADS, CRACKS, ETC.
QC
BAR INSPECT LOT ACCEPTANCE QRAS 60031
MOVE TO ASSEMBLY
EACH LOT OF HEADERS IS CHECKED FOR BONDABILITY AND DISCOLORATION BY SIMULATING IN USE CONDITIONS
QC
FINISHED HEADER INSPECTION QRAS NO. 60022
A SAMPLE OF BARS IS CHECKED ONCE PER SHIFT BEFORE MOUNT TO DETERMINE ESCAPES FROM BAR INSPECTION AND TO ALLOW A BASE FOR SURVEILLANCE OF DAMAGE WHICH OCCURS BETWEEN BAR INSPECT AND BONDING.
QC
PRE-MOUNT BAR SURVEILLANCE QRAS NO. 60543
MOUNT BARS
AT BAR MOUNT EACH OPERATOR'S WORK IS MONITORED EACH SHIFT FOR WORKMANSHIP TYPE DEFECTS. OPERATORS ARE CLASSIFIED BY PERCENT DEFECTIVE AS CERTIFIED BY LOT ACCEPTANCE.
QC
MOUNT SURVEILLANCE QRAS NO. 60353

2



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