Series 54S/74S Circuits

Schottky TTL
Previewing Three Series 54S/74S MSI Functions*

SN54S/74S181 Arithmetic/Logic Units

- Fastest and most versatile IC adder
- 20 ns typical add time for 16 bit words
- Performs all arithmetic/logic functions of a CPU
- Cascadable to N-bits
- Pin-for-pin functional equivalent of SN54/74181 ALU

SN54S/74S194 Universal Bidirectional Shift-Registers

- Industry's first fully universal 100-MHz TTL shift registers
  - Parallel broadside load
  - Shift right
  - Shift left
  - Inhibit clock (do nothing)
- Cascadable to N-bits
- Designed specifically for performing all shift functions required of high-speed accumulators employing SN74S181 ALU's

SN54S/74S157 Quad 2-Input Multiplexers

- Typical propagation delays of 2.25 ns per level at 13 mW per gate
- May be used with SN74S181 and SN74S194 to implement high-speed CPU accumulator
- Selects bused data from one of two sources
- Generates four functions of two variables (one variable is common)

* Available Mid-1971

For the Full Line of Series 54S/74S Schottky SSI, See Page 5-

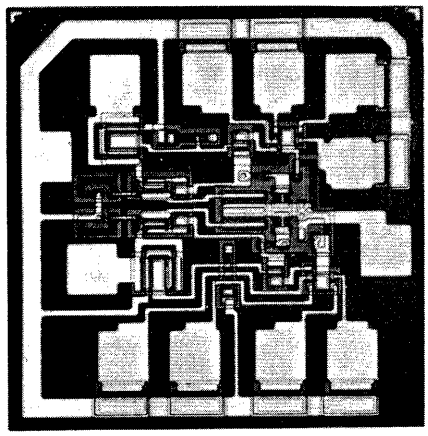
SCHOTTKY TTL

SERIES 54S/74S
SCHOTTKY-CLAMPED† TRANSISTOR-TRANSISTOR LOGIC

FOR HIGH-SPEED, HIGH-PERFORMANCE DIGITAL SYSTEMS

description

Series 54S/74S Schottky TTL circuits are implemented with full Schottky-barrier-diode clamping to achieve ultra-high speeds previously obtainable only with emitter-coupled logic, yet they retain the desirable features of, and are completely compatible with, most of the popular saturated logic circuits. Schottky TTL circuits currently offer the best speed-power product of any high-speed logic family.



Schottky-barrier-diode clamping prevents transistors from achieving classic saturation and thereby effectively eliminates excess charge storage and subsequent recovery times. These recovery times contribute significantly to overall propagation delays experienced with saturated digital-logic circuits.

Series 54S/74S circuits are completely compatible with the Series 54/74, Series 54H/74H, and Series 54L/74L TTL logic families. Ease of use and compatibility with other TTL families result in flexibility of choice within the four speed-power ranges offered (Series 54/74, 54H/74H, 54L/74L, 54S/74S) to achieve highly efficient system grading to specific performance requirements.

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Definitive specifications are provided for operating characteristics over the full military temperature range of −55°C to 125°C for Series 54S circuits and over the temperature range of 0°C to 70°C for Series 74S circuits.

features

VERY-HIGH-SPEED, LOW-POWER OPERATION

- **3-ns typical gate propagation delay time**
- **19-mW-per-gate power dissipation at 50% duty cycle — speed-power product = 57 pJ**
- **125-MHz typical J-K flip-flop maximum input clock frequency (d-c coupled)**

EASE OF SYSTEM DESIGN

- **fully compatible with Series 54/74, 54H/74H, and 54L/74L TTL (including MSI/LSI), and most DTL**
- **Schottky-diode-clamped inputs simplify system design**
- **terminated, controlled-impedance lines not normally required**
- **low output impedance: provides low a-c noise susceptability**
  drives highly capacitive loads

IMPROVED CIRCUIT PERFORMANCE

- **switching times virtually insensitive to power supply and/or temperature variations**
- **power dissipation remains relatively low at operating frequencies up to 100 MHz**
- **high fan-out: 20 54S/74S loads at the high logic level**
  10 54S/74S loads at the low logic level
- **high d-c noise margin—typically 1 volt**

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†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

SERIES 54S/74S
SCHOTTKY-CLAMPED TRANSISTOR-TRANSISTOR LOGIC

SERIES 54S/74S
FEATURING 3-ns SPEED AND 20-mW-PER-GATE PERFORMANCE
SMALL SCALE INTEGRATION (SSI)

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGES*			
	−55°C to 125°C	0°C to 70°C	Dual-In-Line		Flat	PAGE
NAND/NOR GATES						
Quadruple 2-Input Positive-NAND Gates	SN54S00	SN74S00	J	N	W	5-4
Quadruple 2-Input Positive-NAND Gates (with Open-Collector Output)	SN54S03	SN74S03	J	N	W	5-8
Hex Inverters	SN54S04	SN74S04	J	N	W	5-4
Hex Inverters (with Open-Collector Output)	SN54S05	SN74S05	J	N	W	5-8
Triple 3-Input Positive-NAND Gates	SN54S10	SN74S10	J	N	W	5-4
Triple 3-Input Positive-AND Gates	SN54S11	SN74S11	J	N	W	5-10
Triple 3-Input Position-AND Gates (with Open-Collector Output)	SN54S15	SN74S15	J	N	W	5-10
Dual 4-Input Positive-NAND Gates	SN54S20	SN74S20	J	N	W	5-4
Dual 4-Input Positive-NAND Gates (with Open-Collector Output)	SN54S22	SN74S22	J	N	W	5-8
Dual 4-Input Positive-NAND Buffers	SN54S40	SN74S40	J	N	W	5-12
Dual 4-Input Positive-NAND Line Drivers	SN54S140	SN74S140	J	N	W	5-12
AND-OR-INVERT GATES						
4-2-3-2-Input AND-OR-INVERT Gates	SN54S64	SN74S64	J	N	W	5-13
4-2-3-2-Input AND-OR-INVERT Gates (with Open-Collector Output)	SN54S65	SN74S65	J	N	W	5-13
FLIP-FLOPS						
Dual D-Type Edge-Triggered Flip-Flops	SN54S74	SN74S74	J	N	W	5-15
Dual J-K Negative Edge-Triggered Flip-Flops (80 MHz) with Preset and Clear	SN54S112	SN74S112	J	N	W	5-17
Dual J-K Negative Edge-Triggered Flip-Flops (80 MHz) with Preset	SN54S113	SN74S113	J	N	W	5-21
Dual J-K Negative Edge-Triggered Flip-Flops (80 MHz) Common Clock and Common Clear	SN54S114	SN74S114	J	N	W	5-21

*For outline drawings of all packages, see Section 1.

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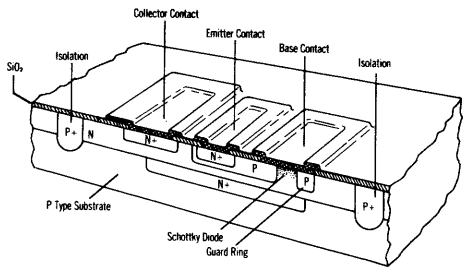
The Schottky TTL Technology

The Schottky-clamped transistor is produced utilizing conventional diffusions. The base contact opening is extended beyond the base diffusion and over the collector region. Metallization is deposited over both the base and collector regions and simultaneously serves as the transistor base contact and the SBD anode contact. The collector n-type material and the metallization then form the metal-silicon SBD structure (refer to cross-section at right).



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The Schottky TTL Technology (Continued)

The SBD is connected in parallel to the base-collector junction of the normal TTL n-p-n transistor. As the SBD has a lower forward voltage than the base-collector junction, it clamps the transistor as base drive increases, diverting most excess base current from the base-collector junction, and prevents the transistor from reaching classic saturation. Excess stored charge, which exists in usual transistor structures and which must be removed before switching occurs, does not exist in the SBD-clamped transistor.

In addition to incorporation of the SBD into popular 54/74 TTL, the Series 54S/74S Schottky TTL family employs shallower diffusion and smaller geometries which lower internal capacitances and further reduces overall propagation delays. Elimination of gold-doping simplifies processing and stabilizes switching speeds over the operating temperature range.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Output voltage (see Notes 1 and 3) . . . . . 7 V
Operating free-air temperature range: Series 54S Circuits . . . . . −55°C to 125°C
Series 74S Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This is the maximum voltage which should be applied to any open-collector output when it is in the off state.

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recommended operating conditions

	SERIES 54S CIRCUITS			SERIES 74S CIRCUITS			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	−55		125	0		70	°C

unused inputs of positive-AND/NAND gates

For optimum switching times and minimum noise susceptibility, unused inputs of AND or NAND gates should be maintained at a voltage greater than 2.7 V, but not to exceed the absolute maximum rating of 5.5 V. This eliminates the distributed capacitance associated with the floating input emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling input emitters are:

a. Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between 2.7 V and 3.5 V.
b. Connect unused inputs to a used input if maximum fan-out of the driving output will not be exceeded. Each additional input presents a full load to the driving output at a high-level voltage but adds no loading at a low-level voltage.
c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1-kΩ resistor.

input-current requirements

Input-current requirements reflect worst-case V_{CC} and temperature conditions. Each input of the multiple-emitter input transistors requires a maximum of 2 mA out of the input at a low logic level which is defined as 1 normalized load. Each input requires current into the input at a high logic level. This current is 50 μA maximum for each emitter. Currents into the input terminals are specified as positive values.

fan-out capability

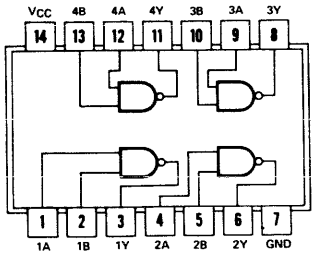
Fan-out (N) reflects the ability of an output to supply current to a number of normalized loads at a high logic level and to sink current at the low logic level. At the high logic level, each standard output is capable of supplying current to drive 20 Series 54H, 74H, 54S, or 74S loads (N_H = 20). Currents out of the output are specified as negative values. At the low logic level, each standard output is capable of sinking current from 10 Series 54H, 74H, 54S, or 74S loads (N_L = 10).

CIRCUIT TYPES SN54S00, SN54S04, SN54S10, SN54S20, SN74S00, SN74S04, SN74S10, SN74S20
POSITIVE-NAND GATES/HEX INVERTERS

Typical Propagation Time . . . 3 ns at C_L = 15 pF
Typical Power Dissipation . . . 19 mW per Gate at 50% Duty Cycle

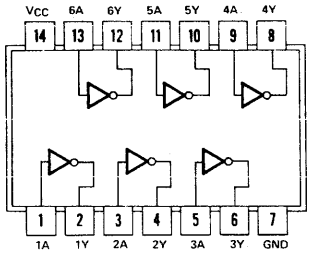
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)

SN54S00, SN74S00
QUADRUPLE 2-INPUT NAND GATES



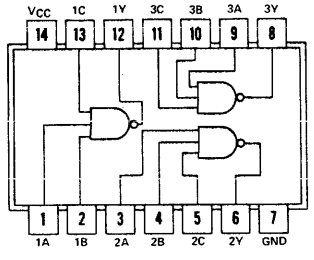
positive logic: $Y = \overline{AB}$

SN54S04, SN74S04
HEX INVERTERS



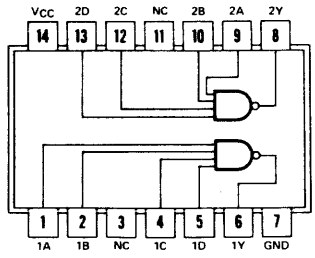
positive logic: $Y = \overline{A}$

SN54S10, SN74S10
TRIPLE 3-INPUT NAND GATES



positive logic: $Y = \overline{ABC}$

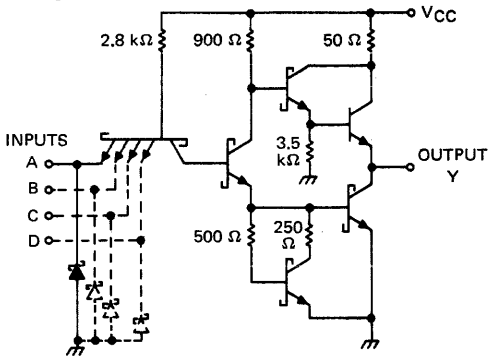
SN54S20, SN74S20
DUAL 4-INPUT NAND GATES



positive logic: $Y = \overline{ABCD}$

NC - No internal connection

schematic (each gate)



Component values shown are nominal.

recommended operating conditions

		SN54S00, SN54S04, SN54S10, SN54S20			SN74S00, SN74S04, SN74S10, SN74S20			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature, T_A		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −1 mA	V_{IL} = 0.8 V,	Series 54S	2.5	3.4		V
				Series 74S	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20 mA	V_{IH} = 2 V,				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7 V				50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−40		−100	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0 V			2.5	4	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5 V			5	9	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS¶		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	R_L = 280 Ω	2	3	4.5	ns
		C_L = 50 pF,	R_L = 280 Ω		4.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	R_L = 280 Ω	2	3	5	ns
		C_L = 50 pF,	R_L = 280 Ω		5		

¶Switching characteristic measurements are made utilizing the same test circuits as illustrated for Darlington outputs in Figure 74 of the Series 54H/74H section. The inverting-output waveform is applicable for these three circuits. In lieu of Notes 1 through 4, the following notes are applicable:

NOTES: A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 2.5 ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.
B. Inputs not under test are at 2.7 V.
C. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

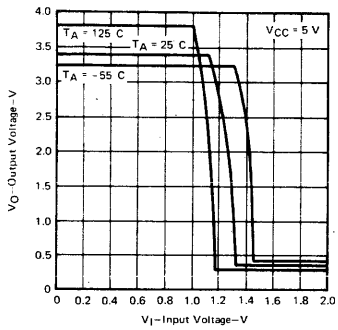

FIGURE 1

INPUT-CLAMPING-DIODE
FORWARD VOLTAGE
vs
FREE-AIR TEMPERATURE

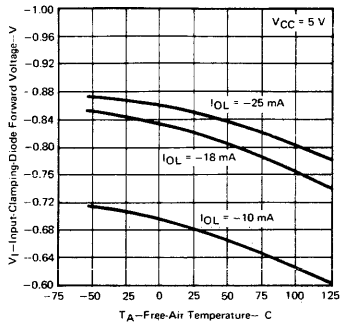

FIGURE 2

INPUT CURRENT
vs
INPUT VOLTAGE

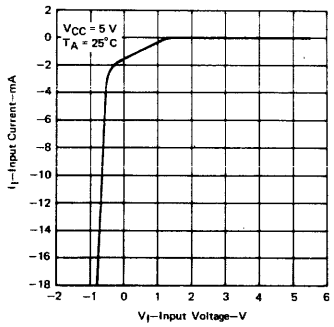

FIGURE 3

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

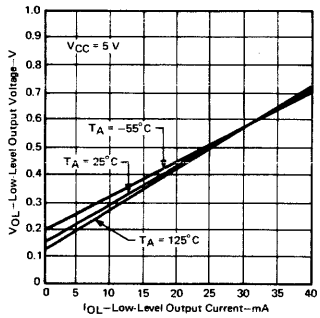

FIGURE 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

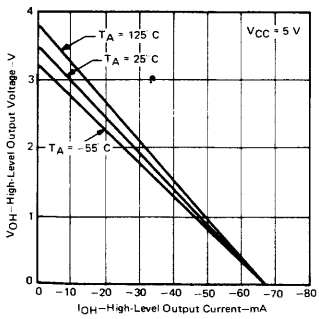

FIGURE 5

HIGH-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE

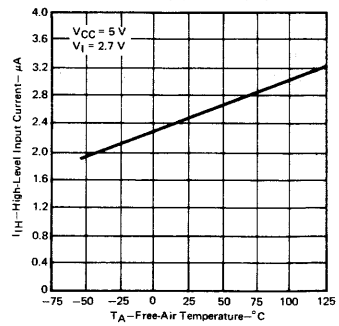

FIGURE 6

†Data for temperatures below 0°C and above 70°C is applicable to Series 54S circuits only.

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TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

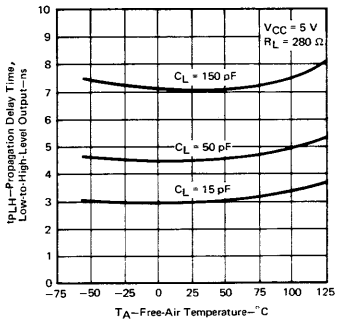


FIGURE 7

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

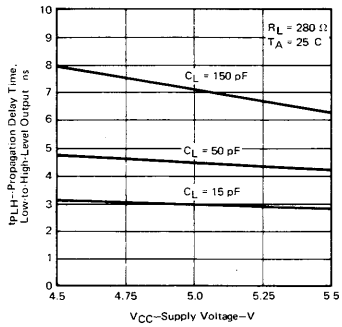


FIGURE 8

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

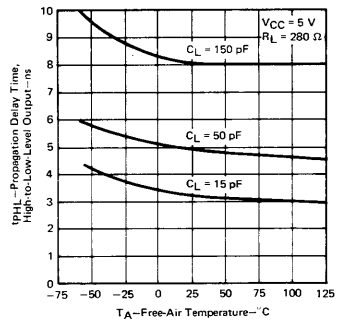


FIGURE 9

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

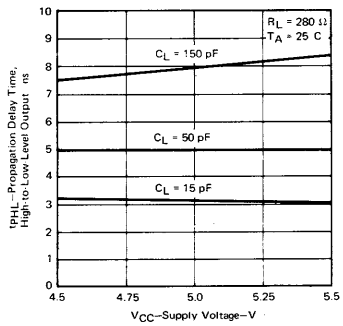


FIGURE 10

AVERAGE PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

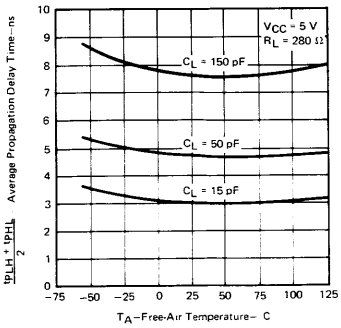


FIGURE 11

POWER DISSIPATION PER GATE
vs
FREQUENCY

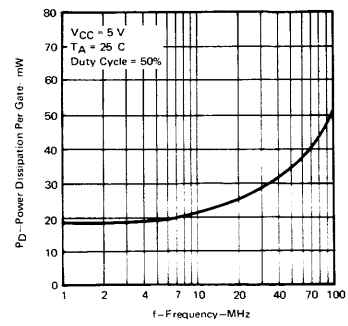


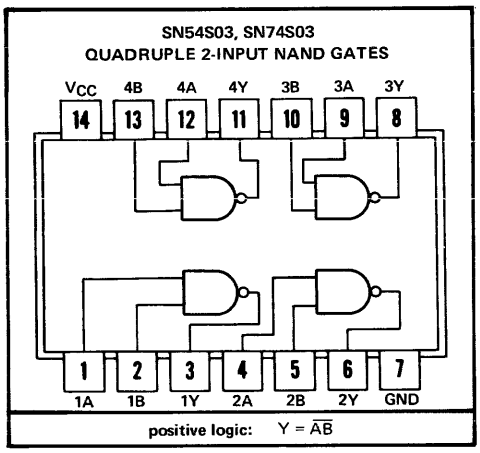
FIGURE 12

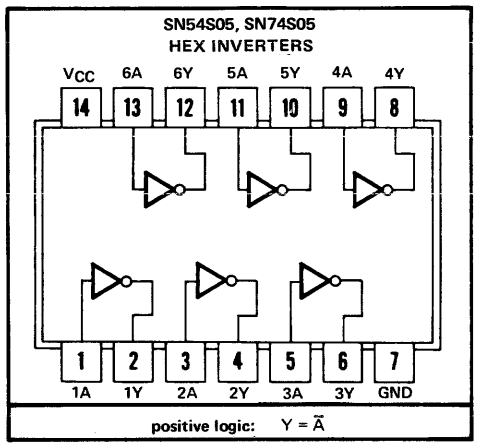
†Data for temperatures below 0°C and above 70°C is applicable to Series 54S circuits only.

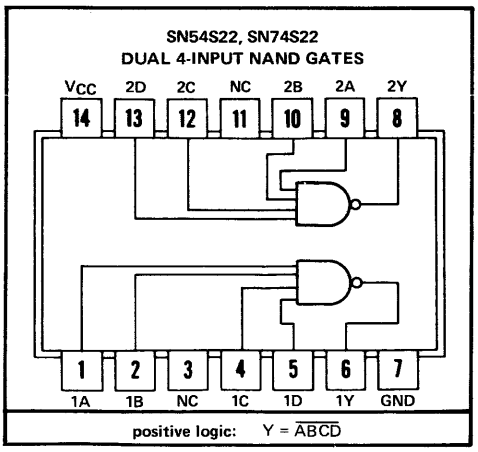
CIRCUIT TYPES SN54S03, SN54S05, SN54S22, SN74S03, SN74S05, SN74S22
POSITIVE-NAND GATES/HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

Typical Propagation Time . . . 5 ns at C_L = 15 pF
Typical Power Dissipation . . . 17 mW per Gate at 50% Duty Cycle

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)

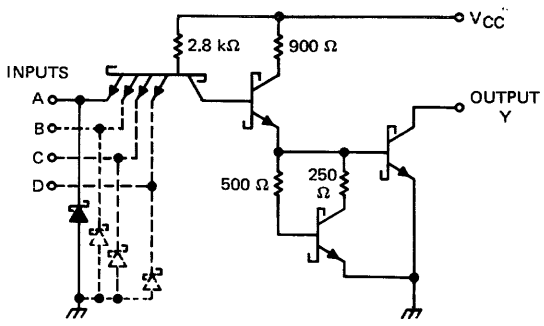






NC—No internal connection

schematic (each gate)



Component values shown are nominal.

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recommended operating conditions

	SN54S03, SN54S05, SN54S22			SN74S03, SN74S05, SN74S22			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from any output, N			10			10	
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 5.5 V	V_{IL} = 0.8 V,			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 20 mA	V_{IH} = 2 V,			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.7 V			50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.5 V			−2	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX,	All inputs at 0 V		1.5	3.3	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX,	All inputs at 5 V		5	9	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

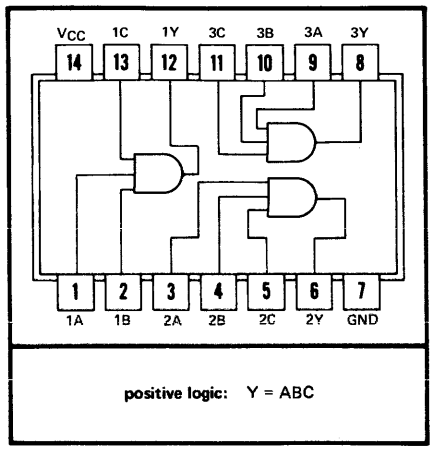
PARAMETER		TEST CONDITIONS¶		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	R_L = 280 Ω	2	5	7.5	ns
		C_L = 50 pF,	R_L = 280 Ω		7.5		
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	R_L = 280 Ω	2	4.5	7	ns
		C_L = 50 pF,	R_L = 280 Ω		7		

¶Switching characteristic measurements are made utilizing the same test circuit as illustrated for open-collector outputs in Figure 74 of the Series 54H/74H section. The inverting-output waveform is applicable for these circuits. In lieu of Notes 1 through 4, the following notes are applicable:

NOTES: A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 2.5 ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.
B. Inputs not under test are at 2.7 V.
C. C_L includes probe and jig capacitance.

CIRCUIT TYPES SN54S11, SN54S15, SN74S11, SN74S15
TRIPLE 3-INPUT POSITIVE-AND GATES

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



SN54S11, SN74S11 ACTIVE PULL-UP

- Typical Propagation Time . . . 5 ns at C_L = 15 pF
- Typical Power Dissipation . . . 32 mW per Gate at 50% Duty Cycle

SN54S15, SN74S15 OPEN-COLLECTOR

- Typical Propagation Time . . . 6 ns at C_L = 15 pF
- Typical Power Dissipation . . . 29 mW per Gate at 50% Duty Cycle

5

recommended maximum fan-out from each output

	SN54S11 SN74S11	SN54S15 SN74S15
Loads at a high logic level	20	
Loads at a low logic level	10	10

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		SN54S11 SN74S11 MIN	SN54S11 SN74S11 TYP‡	SN54S11 SN74S11 MAX	SN54S15 SN74S15 MIN	SN54S15 SN74S15 TYP‡	SN54S15 SN74S15 MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −1 mA	SN54S11	2.5	3.4					V
			SN74S11	2.7	3.4					
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 5.5 V							250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_I = 2.7 V				50			50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.5 V				−2			−2	mA
I_{OS}	Short-circuit output current §	V_{CC} = MAX		−40		−100				mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX, All inputs at 5 V			4.5	8		3.5	6.5	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX, All inputs at 0 V			8	14		8	14	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable series on the second page of this section.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

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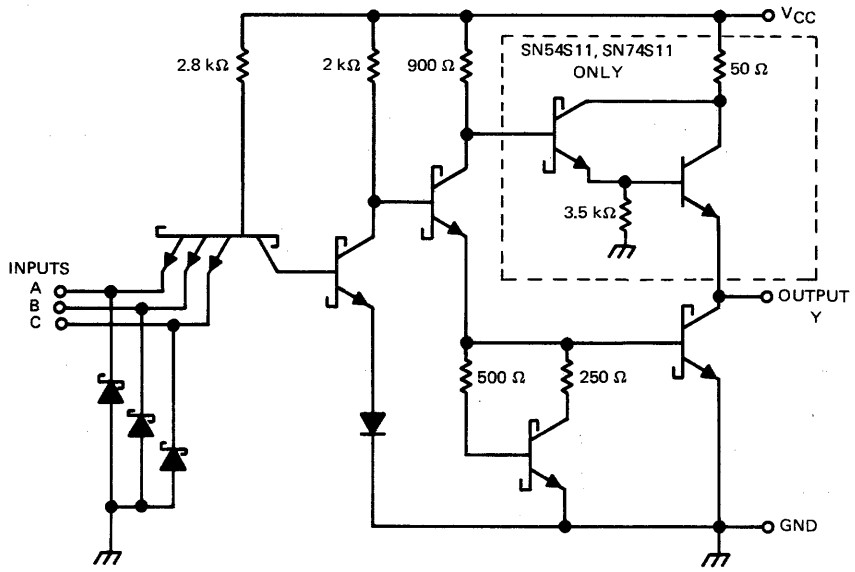
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	TEST CONDITIONS¶	SN54S11 SN74S11			SN54S15 SN74S15			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 280 Ω	2.5	4.5	7	2.5	5.5	8.5	ns
	C_L = 50 pF, R_L = 280 Ω		6			8.5		ns
t_{PHL} Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 280 Ω	2.5	5	7.5	2.5	6	9	ns
	C_L = 50 pF, R_L = 280 Ω		7.5			8		ns

¶Switching characteristic measurements are made utilizing the same test circuits as illustrated in Figure 74 of the Series 54H/74H section. The noninverting-output waveform is applicable for these circuits. In lieu of Notes 1 through 4, the following notes are applicable:

NOTES: A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 2.5 ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.
B. Inputs not under test are at 2.7 V.
C. C_L includes probe and jig capacitance.

schematic (each gate)

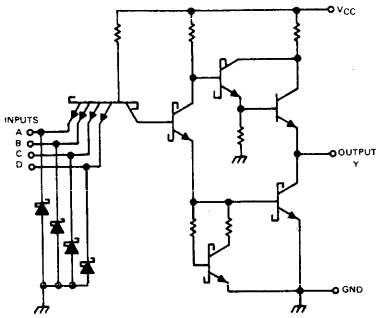


Component values shown are nominal.

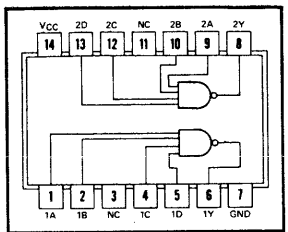
CIRCUIT TYPES SN54S40, SN54S140, SN74S40, SN74S140
DUAL 4-INPUT POSITIVE-NAND BUFFERS/LINE DRIVERS

Typical Propagation Time . . . 4 ns at C_L = 50 pF

schematic (each gate)



J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABCD}$

NC - No internal connection

recommended maximum fan-out from each output

Loads at a high logic level	60
Load at a low logic level	30

electrical characteristics over operating free-air temperature range (unless otherwise noted)

5

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −3 mA	Series 54S	2.5	3.4		V
			Series 74S	2.7	3.4		
		V_{CC} = MIN, V_I = 0.5 V, R_O = 50 Ω to GND	SN54S140 SN74S140	2			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 60 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_I = 2.7 V				100	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.5 V				−4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−50		−225	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX, All inputs at 0 V			5	9	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX, All inputs at 5 V			12.5	22	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable series on the second page of this section.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed 100 milliseconds.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 30

PARAMETER		TEST CONDITIONS¶	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 93 Ω	2	4	6.5	ns
		C_L = 150 pF, R_L = 93 Ω		6		ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 50 pF, R_L = 93 Ω	2	4	6.5	ns
		C_L = 150 pF, R_L = 93 Ω		6		ns

¶Switching characteristic measurements are made utilizing the same test circuits as illustrated for Darlington outputs in Figure 74 of the Series 54H/74H section. The inverting waveform is applicable for these circuits. In lieu of Notes 1 through 4, the following notes are applicable:

NOTES: A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 2.5 ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.

B. Inputs not under test are at 2.7 V.

C. C_L includes probe and jig capacitance.

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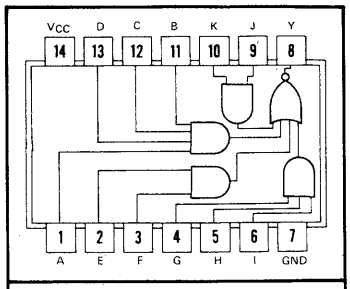
SN54S64, SN74S64 ACTIVE PULL-UP

- Typical Propagation Time . . . 3.5 ns at C_L = 15 pF
- Typical Power Dissipation . . . 39 mW at 50% Duty Cycle

SN54S65, SN74S65 OPEN-COLLECTOR

- Typical Propagation Time . . . 5 ns at C_L = 15 pF
- Typical Power Dissipation . . . 36 mW at 50% Duty Cycle

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: $\overline{ABCD + EF + GHI + JK}$

recommended maximum fan-out from each output

	SN54S64 SN74S64	SN54S65 SN74S65
Loads at a high logic level	20	
Loads at a low logic level	10	10

5

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54S64 SN74S64 MIN	TYP‡	MAX	SN54S65 SN74S65 MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 0.8 V, I_{OH} = −1 mA	SN54S64	2.5	3.4					V
			SN74S64	2.7	3.4					
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 0.8 V, V_{OH} = 5.5 V							250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 2 V, I_{OL} = 20 mA				0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX, V_I = 2.7 V				50			50	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.5 V				−2			−2	mA
I_{OS}	Short-circuit output current §	V_{CC} = MAX		−40		−100				mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX, See Note 1			7	12.5	6	11		mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX, See Note 2			8.5	16	8.5	16		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable Series on the second page of this section.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTES: 1. I_{CCH} is measured with all inputs grounded, and the outputs open.
2. I_{CCL} is measured with all inputs of one gate at 5 V, the remaining inputs grounded, and the outputs open.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	TEST CONDITIONS¶	SN54S64 SN74S64			SN54S65 SN74S65			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 280 Ω	2	3.5	5.5	2	5	7.5	ns
	C_L = 50 pF, R_L = 280 Ω		5			8		ns
t_{PHL} Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 280 Ω	2	3.5	5.5	2	5.5	8.5	ns
	C_L = 50 pF, R_L = 280 Ω		5.5			6.5		ns

¶ Switching characteristic measurements are made utilizing the same test circuits as illustrated in Figure 74 of the Series 54H/74H section. The inverting output waveform is applicable for these circuits. In lieu of Notes 1 through 4, the following notes are applicable:

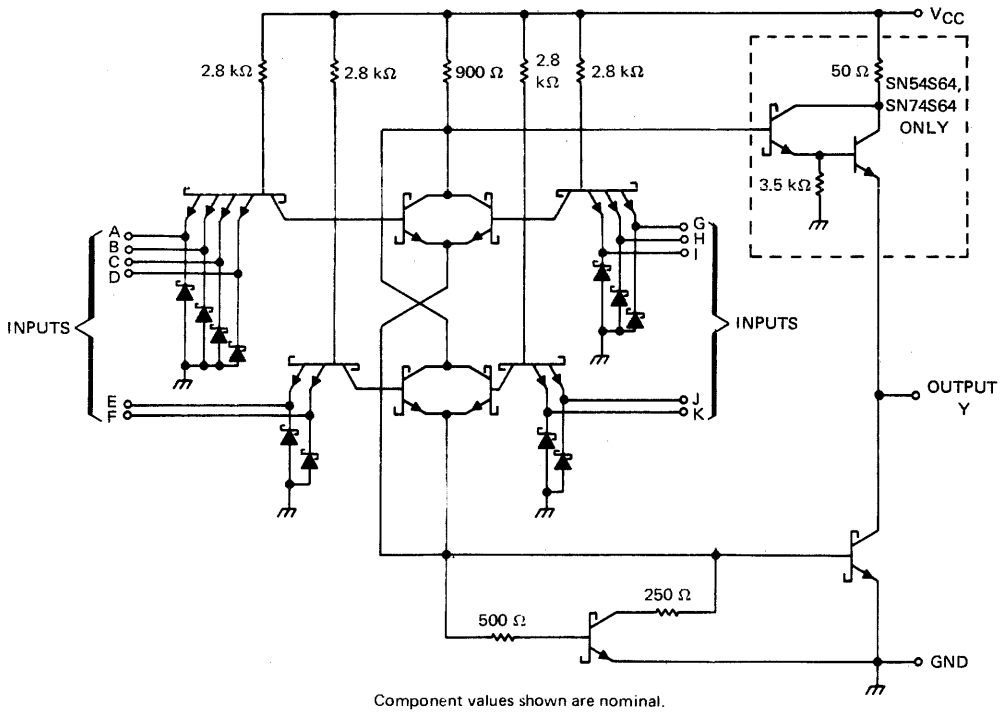
NOTES: A. The pulse generator has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 2.5 ns, PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.

B. Input pulse is applied to one input of one AND section, 2.7 V is applied to all unused inputs of that AND section, and all inputs of unused AND sections are grounded.

C. C_L includes probe and jig capacitance.

5

schematic



Component values shown are nominal.

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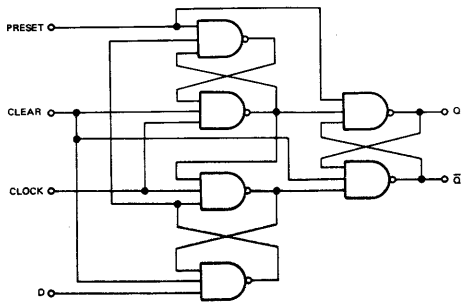
Typical Maximum Input Clock Frequency . . . 90 MHz
Typical Power Dissipation . . . 75 mW per Flip-Flop

functional block diagram (each flip-flop)



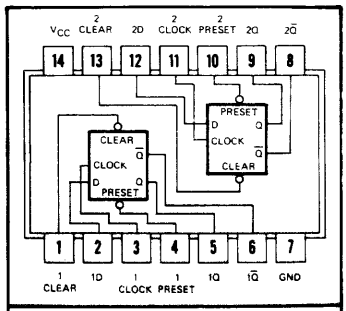
TRUTH TABLE
(Each Flip-Flop)

t_n	t_{n+1}	
INPUT	OUTPUT	
D	Q	Q̄
L	L	H
H	H	L

H = high level, L = low level

NOTES: A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic:
Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

description

These monolithic dual edge-triggered flip-flops utilize Schottky TTL circuitry to produce very-high-speed D-type flip-flops. Each flip-flop has individual clear and preset inputs, and also complementary Q and Q̄ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

These circuits are fully compatible for use with most TTL or DTL circuits. A full fan-out to 10 normalized Series 54S/74S loads is available from each of the outputs at a low logic level. At a high logic level, a fan-out of 20 is available to facilitate tying unused inputs to used inputs. Maximum clock frequency is 75 megahertz, with a typical power dissipation of 75 milliwatts per flip-flop.

The SN54S74 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74S74 is characterized for operation from 0°C to 70°C.

recommended operating conditions

		SN54S74			SN74S74			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Clock frequency, f_{clock}			70			70		MHz
Width of clock pulse, $t_{w(clock)}$			7			7		ns
Width of preset pulse, $t_{w(preset)}$			7			7		ns
Width of clear pulse, $t_{w(clear)}$			7			7		ns
Input setup time, t_{setup}	High-level data		10			10		ns
	Low-level data		12			12		ns
Input hold time, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA					−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8, I_{OH} = −1 mA		SN54S74	2.5	3.4		V
				SN74S74	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8, I_{OL} = 20 mA					0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V	D input				50	μA
			Clock or Preset				100	
			Clear				150	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V	D input				−2	mA
			Clock or Preset				−4	
			Clear				−6	
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 1				30		mA

5

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. See Figures 1 through 5 of the Series 54H/74H section for test circuits.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTE 1: I_{CC} is measured with outputs open, clock grounded, and J, K, preset, and clear at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS¶	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 280 Ω		90		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset			5		ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset			8		ns
t_{PLH}	Propagation delay time, low-to-high-level output, from clock			7		ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock			7		ns

¶Switching characteristic measurements are made utilizing the same test circuits as illustrated in Figures 6, 7, and 8 of the Series 54H/74H section, except that the input pulse rise and fall times (shown as ⩽ 7 ns) are ⩽ 2.5 ns. Information in the notes of these figures is applicable except as follows:

In Figures 7 and 8: $t_{w(clock)}$ = 10 ns.
In Figure 7: t_{setup} = 8 ns and t_w = 30 ns.
In Figure 8: t_{setup} = 8 ns and t_w = 30 ns.

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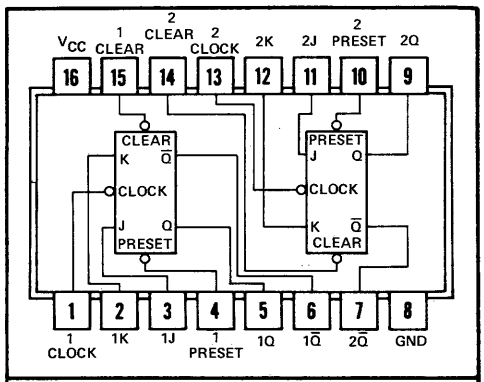
- Typical Maximum Input Clock Frequency . . . 125 MHz
- Fully D-C Coupled
- Typical Power Dissipation . . . 75 mW per Flip-Flop

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: Low input to preset sets Q to high level.
Low input to clear resets Q to low level.
Clear and preset are independent of clock.

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES: A. t_n = Bit time before clock pulse.
B. t_{n+1} = Bit time after clock pulse.

5

description

These monolithic dual J-K flip-flops feature individual J, K, clock, and asynchronous preset and clear inputs to each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the truth table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

recommended operating conditions

		SN54S112			SN74S112			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		80	0		80	MHz
Width of clock pulse, $t_{w(clock)}$		6			6			ns
Width of preset pulse, $t_{w(preset)}$		8			8			ns
Width of clear pulse, $t_{w(clear)}$		8			8			ns
Input setup time, t_{setup} (see Note 1)		3			3			ns
Input hold time, t_{hold} (see Note 2)		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTES: 1. Setup time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
2. Hold time is the interval immediately following the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −1 mA	SN54S112	2.5	3.4		V
				SN74S112	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V		J or K input			50	μA
				Clock, preset, or clear			100	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V		J or K input			−1.6	mA
				Clock			−4	
				Preset or clear			−7	
I_{OS}	Short-circuit output current§	V_{CC} = MAX,			−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3			30	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTE 3: I_{CC} is measured with outputs open, clock grounded, and J, K, preset, and clear at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS¶	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 280 Ω	80	125		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset		2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset		2	5	7	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from clock		2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock		2	5	7	ns

¶Switching characteristic measurements are made utilizing the same test circuits as illustrated for Darlington outputs in Figures 77 and 78 of the Series 54H/74H section. Information in the notes of these figures pertaining to the SN74H108 is applicable for the SN74S112, except $t_1 = t_0$ = 2.5 ns for all input pulse characteristics and the steady-state J and K input voltages are 2.7 V instead of 2.4 V.

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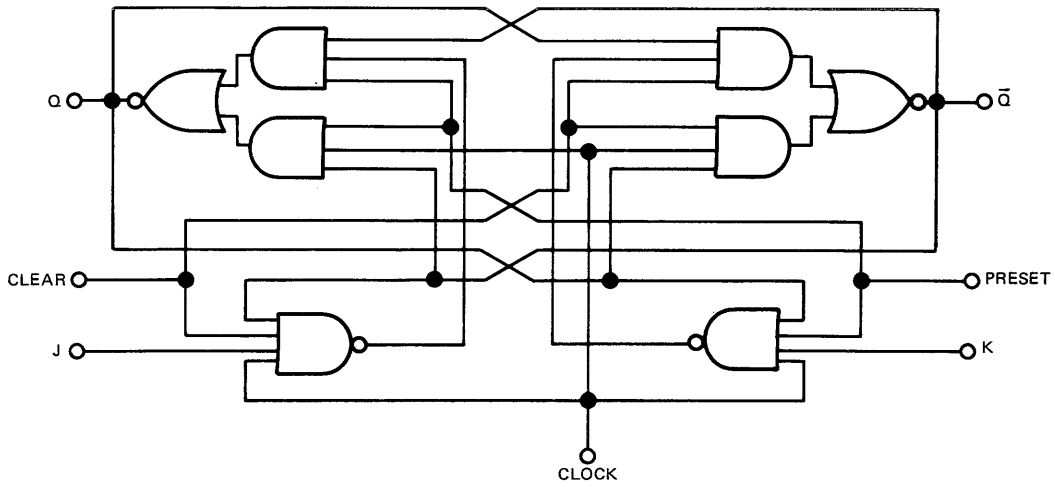
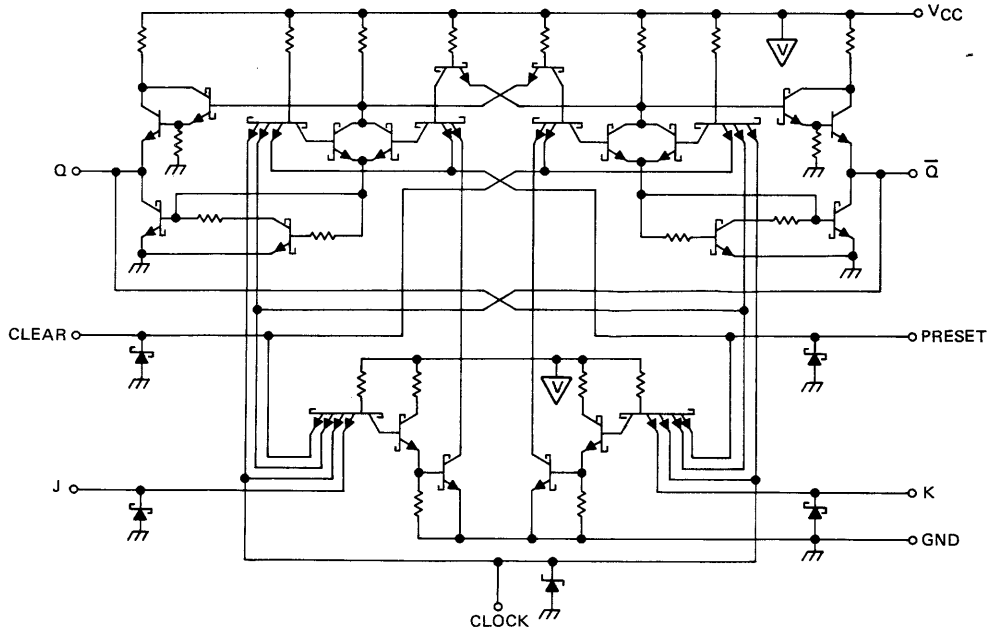
functional block diagram (each flip-flop)



5

schematic (each flip-flop)



▽ . . . V_{CC} bus

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

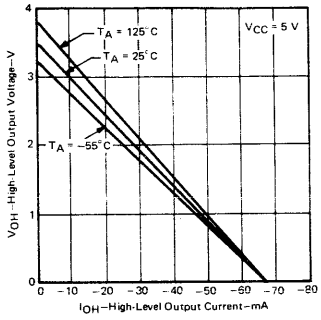


FIGURE 1

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

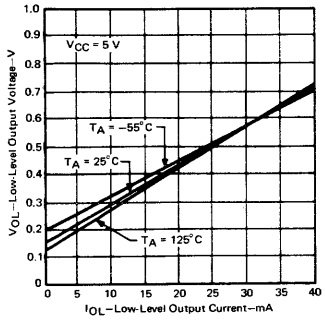


FIGURE 2

INPUT CURRENT
vs
INPUT VOLTAGE

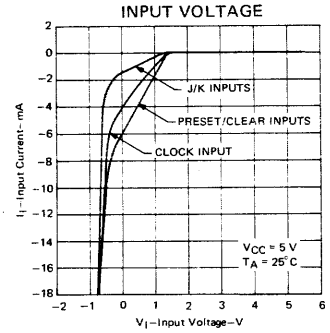


FIGURE 3

HIGH-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE

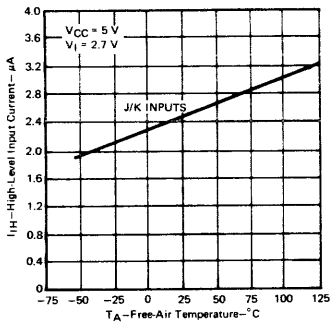


FIGURE 4

AVERAGE PROPAGATION DELAY TIME,
CLOCK TO OUTPUT
vs
FREE-AIR TEMPERATURE

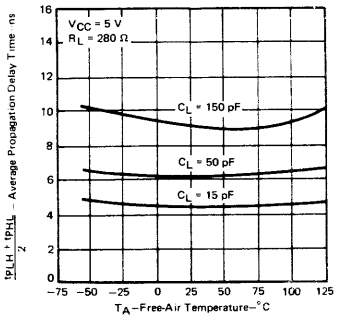


FIGURE 5

AVERAGE PROPAGATION DELAY TIME,
CLOCK TO OUTPUT
vs
LOAD CAPACITANCE

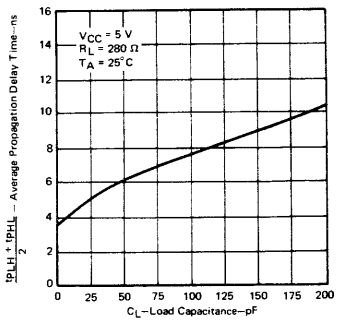


FIGURE 6

†Data for temperatures below 0°C and above 70°C is applicable to Series 54S circuits only.

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CIRCUIT TYPES SN54S113, SN54S114, SN74S113, SN74S114
DUAL J-K EDGE-TRIGGERED FLIP-FLOPS

Typical Maximum Input Clock Frequency . . . 125 MHz
Typical Power Dissipation . . . 75 mW per Flip-Flop

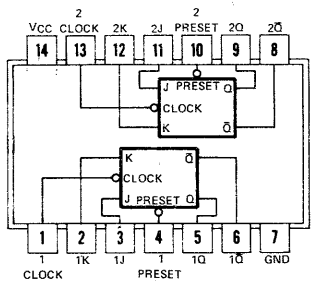
TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES: A. t_n = Bit time before clock pulse.
B. t_{n+1} = Bit time after clock pulse.

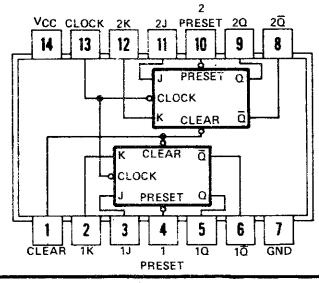
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)

SN54S113, SN74S113
DUAL PRESETTABLE FLIP-FLOPS



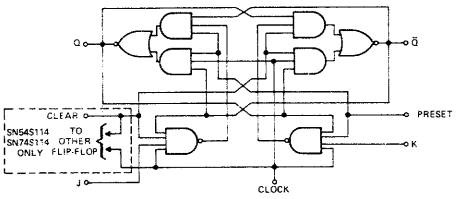
positive logic:
Low input to preset sets Q to high level
Preset is independent of clock

SN54S114, SN74S114
DUAL FLIP-FLOPS WITH
COMMON CLOCK AND CLEAR



positive logic:
Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

functional block diagram (each flip-flop)



description

The SN54S113 and SN74S113 offer individual J, K, preset, and clock inputs. The SN54S114 and SN74S114 offer common clock and common clear inputs and individual J, K, and preset inputs.

These monolithic dual flip-flops are designed so that when the clock goes high, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the truth table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

recommended operating conditions

		SN54S113 SN54S114			SN74S113 SN74S114			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		80	0		80	MHz
Width of clock pulse, $t_{w(clock)}$		6			6			ns
Width of preset pulse, $t_{w(preset)}$		8			8			ns
Width of clear pulse, $t_{w(clear)}$	SN54S114, SN74S114	8			8			ns
Input setup time, t_{setup}		3			3			ns
Input hold time, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN545113 SN74S113			SN54S114 SN74S114			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	Series 54S	2.5	3.4		2.5	3.4		V
			Series 74S	2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V	J or K input			50			50	μA
			Clock			100			200	
			Preset			100			100	
			Clear						200	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V	J or K input			−1.6			−1.6	mA
			Clock			−4			−8	
			Preset			−7			−7	
			Clear						−14	
I_{OS}	Short circuit output current§	V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3		30	50		30	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. See Figures 64 through 69 of the Series 54H/74H section for test circuits.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

NOTE 3: I_{CC} is measured with outputs open, clock grounded, and J, K, preset, and clear at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS¶	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 280 Ω	80	125		MHz
t_{PLH}	Propagation delay time, low-to-high-level output, from clear or preset		2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clear or preset		2	5	7	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from clock		2	4	7	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock		2	5	7	ns

¶ Switching characteristic measurements are made utilizing the same test circuits as illustrated for Darlington outputs in Figures 77 and 78 of the Series 54H/74H section. Information in the notes of these figures pertaining to the SN74H108 is applicable except $t_1 = t_0 = 2.5$ ns for all input pulse characteristics and the steady-state J and K input voltages are 2.7 V instead of 2.4 V.

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